2S Mobile Battery Charger with Integrated Cell Balancing

A Thesis Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

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May 2020

This Master's Thesis is dedicated to my Lord and Savior, Jesus Christ. In Him all else finds meaning and life-giving grace.

Acknowledgements

I am very grateful to all who pushed me throughout my academic career and helped foster the abilities that made this work possible. I believe behind the curtains of any success is not only hard work but the loving support of people, and I have been encouraged by so many. The constructive challenges from those closest to me have made me a better person and engineer.

Thank you to Abbey, my loving fiancée, who encouraged me so well during my toughest days. As my dearest companion and comforter, she has inspired me to not only reach the finish line of this achievement but to continue to mature to be the best person and a future husband I can be. I would not have made it to this point without you.

I want to thank my parents for years of investment and belief in me. Through their parenting, I was given a foundation that set me up to succeed not only in academics but in life. Their patience, unwavering support, and love provides an incredible model for me to follow. I hope this work makes all the Blalock engineers like my dad proud.

I have been under the wing of my advising professor, Dr. Costinett, for four years. I have learned more than I ever thought possible. I am thankful that he never allowed me to settle, and under his mentorship, I gained an new found confidence in the ability to learn and achieve. Thank you for so many hours you cared for students like me with no obligation but the care of your heart.

I want to thank my officemates, Kamal Sabi, Spencer Cochran, and Jared Walden who tackled tough questions with me and created an encouraging work environment that promoted creative innovation and professional excellence. Spencer cared for me as a loyal mentor and inspired me to grow in my faith and abilities as an engineer. I would also like to thank Texas Instrument Knoxville, especially Richard Stair and Ryan Lind, for all their help and feedback throughout my

time with this project. I consider any work with them to be a privilege and one of my greatest honors. I would like to thank Sam Brown, my best friend who stood by my side in both life and academics steadfastly. Throughout much of my education that lead to this work, I had the privilege of working with my friend Peter Pham on many projects that stretched our engineering skills. I want to also extend gratitude to so many other students who I worked with and learned so much from in Jared Baxter, Jordan Sangid, Gavin Long, Saeed Anwar, Gabriel Gabian, Andrew Foote, Taylor Short, and Ruiyang Qin. I would like to also thank the group CURENT as a whole for all the support given to its students. The University of Tennessee provided me so many opportunities to advance my education and set me up to succeed in my career, so I am very thankful to the University for all that it has done for me. Finally, I am thankful for Dana Bryson as I dedicate this work also to her in loving memory for all the kindness she gave UT students.

"Don't simply clone something. Strive to make it your own."

- *Keith Brown*

Abstract

Mobile devices and other portable electronics require fast and efficient battery charging to meet the growing energy demands of modern technology. Charging time is reduced with higher charging current, but the current is limited by allowable on-chip power losses specified by thermal constraints for small area integrated circuits (ICs). As compared to a single-cell battery system requiring a given charging time, a two-battery series-connected (2S) cell configuration increases the overall voltage and thus reduces the necessary charging current to achieve the same charging time. Today, commercially available 2S battery chargers on the market currently consist of multi-chip solutions that manage charging, battery cell balancing, battery protection, and modulation control. Those chargers tend to be bulky because of multiple, independent ICs. In this work, a switched capacitor (SC) three-level boost converter is proposed as a single-chip integrated solution to provide simultaneous charging and active balancing for 2S battery topologies. The proposed charging circuit adopts the balancing functionality inherent to switched capacitor converter (SCC) techniques with two additional low-power transistors. Converter evaluation is performed across various input voltages, charging currents, and asymmetric battery voltages. The criteria for each operating scenario is a maximum on-chip loss of 1 W, 5-20 V range at the input, and up to 6.4 A charging current. State space modeling including converter parasitics developed for simulation analysis, and a hardware prototype built using GaN FETs enabled validation of the converter models. A proposed strategy for integration is also addressed as the converter's charging and balancing capabilities are designed to meet or exceed the current market standard.

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Chapter 1

1.1 Introduction

Mobile devices are a continually advancing technology. With each new phone or tablet released on the market, there are upgrades with the latest technologies and features ranging from more intelligent processors and better cameras to larger user screens. These mobile devices utilize batteries to supply the required energy for all its systems. The battery charging time in hours, t_{charge}, is

$$t_{charge} = \frac{Q}{I_{ch}}, \tag{1.1}$$

where Q is the battery capacity in Ampere-hours and I_{ch} is the charging current in Amperes. A battery's energy capacity ($E_{capacity}$), the total Watt-hours available until a battery is fully discharged is

$$E_{capacity} = Q \cdot V_{Bat} = t_{charge} \cdot I_{ch} \cdot V_{Bat}, \tag{1.2}$$

where V_{Bat} is the battery voltage.

Mobile battery charger designs must also account for the charging cable used to recharge the batteries. The modern USB Type-C interconnect charging cables offer a maximum of 3 A of charging current [1] to support higher power devices. Table 1.1 lists the universal series bus, (USB) power adapter (PD) 3.0 profiles with example power adapter levels. The input voltage ranges from

5 V to 20 V with a maximum current of 3 A. The power for this range of inputs is 15 W to 60 W. These inputs have a limitation on the maximum I_{ch} that a charger achieves.

While increasing the charging current reduces t_{charge}, this also leads to increased conduction loss and degrades power efficiency. Power density suffers at high I_{ch} since larger magnetics are required with sufficiently high current ratings. 2S batteries (2 batteries connected in series) decrease the I_{ch} required for a comparable energy and t_{charge} as single cell batteries of the same type by doubling the battery voltage. A list of modern commercial products for 2S high current battery charging systems is in Table 1.2. Batteries in a string requires battery balancing in addition to charging.

For hand-held mobile devices, circuit area and volume are at a premium. An integrated circuit (IC) is fabricated with semiconductor fabrication technology. However, the current solution for 2S battery chargers requires multiple ICs to implement the entire system. For a battery charger compatible with a string of batteries, multiple circuit functions (each provided by a different IC) are needed. If each function requires a different IC, this large component count increases the solution size for a battery system. The Microsoft Surface Go (2018) 2S battery uses two QFN packaged ICs with the Texas Instruments (TI) BQ40Z50 (1-4S battery pack manager) and BQ25700A (buck-boost controller). The Apple iPad Pro (2017) 2S battery uses a TI TPS565158 step-down converter with other IC products from other vendors. As a reference, the TI TPS565158 step-down converter utilizes integrated MOSFETs with 26 mΩ (high-side) and 19 mΩ (low-side) on-resistances. The switching frequency ranges from 200 kHz to 1.6 MHz.

Table 1.1: USB Power Delivery 3.0 Profiles [1]

Power Adapter Level (W)	Permitted Adapter Configurations
15 W	5 V @ 3 A (15 W)
27 W	5 V @ 3 A (15 W) 9 V @ 3 A (27 W)
45 W	5 V @ 3 A (15 W) 9 V @ 3 A (27 W) 15 V @ 3 A (45 W)
60 W	5 V @ 3 A (15 W) 9 V @ 3 A (27 W) 15 V @ 3 A (45 W) 20 V @ 3 A (60 W)

Table 1.2: Commercial ICs for 2S High Current Battery Chargers

Product Name	Product Purpose	Integrated FETs On Chip?	Inductor Size	Package & Size
TI BQ40Z50	1-4S battery pack manager	No	--	QFN 4.0 x 4.0 mm
TI BQ25700A	Buck-boost controller	No	1.0, 2.2 or 3.3 µH	WQFN 4.0 x 4.0 mm
TI TPS565158	4.5V to 17V input, 6A synchronous step-down SWIFT™ converter	Yes	3.3 µH (Coilcraft MSS1048)	VQFN 3.5 x 3.5 mm
TI BQ25713	1-4S charger, 3.5-24 V_{in} 6.4A max, 96% peak efficiency (9-to-7.4V)	No	1.0 or 2.2 µH	WQFN 4.0 x 4.0 mm
TI BQ29200	Protection and balancing	No	--	VSON 3.0 x 3.0 mm

While the TI BQ25713 provides 6.4 A of charging current at high efficiency, the system using this IC has a large footprint since it requires both passives and transistors external to the chip. To combine the function of the BQ25713 IC charger with battery balancing, a separate IC like the TI BQ29200 is required. The BQ29200 provides a low-cost balancing solution and 15 mA of balance current. While it may be low-cost, the shunt dissipative balancing this chip utilizes reduces the battery charger efficiency of any 2S system that uses it. Chapter 2 investigates battery balancing and explains why it is an important function for a string of batteries.

For ICs, keeping the temperature rise at allowable levels is an important consideration. Each IC charger has a thermal limit related to the on-chip power loss. Junction to air thermal resistance, θ_{JA}, specifies how well the package-die dissipates heat (from power loss) from the surface of the part to ambient air from all possible paths on-chip. With temperatures T_J for the die and T_A for the ambient air, θ_{JA} for a chip is

$$\theta_{JA} = \frac{T_J - T_A}{P_D}. \tag{1.3}$$

From this equation, the maximum allowable on-chip loss P_D (power dissipation) that keeps the die below a particular temperature is calculated. Current products such as the BQ25713 have a θ_{JA} of 37.2 °C/W [2], and other IC chargers offer comparable values. If the power dissipation is restricted to a maximum temperature rise of 40°C, the P_D would be limited to 1 W to limit heating during charging. While thermal characteristics of larger chips handle more loss, IC chips larger than the BQ25713 increase the solution size for a system. Discrete power transistors also provide better heat dissipation, but the external footprints of the discrete power transistors would be too large for handheld mobile devices.

1.2 Summary

2S battery systems provide fast charging times without needing to operate at as high of charging current compared to single battery configurations. However, 2S batteries need additional circuitry for balancing of the battery cells. Integrating both the charging and balancing functions on a single IC would decrease the solution size for the battery system. Keeping in mind the maximum on-chip loss limited to 1 W based on temperature rise associated with θ_{JA}, a converter topology that provides charging and balancing without a large component count offers a potential benefit in performance and power density. The following chapters address the a single chip solution by exploring balancing techniques and different topologies that are used for efficient battery charging.

Chapter 2 Literature Review

There is a potential benefit to integrating both a battery charger and balancing functionality onto a single chip, so existing charging and balancing strategies are considered to explore a solution for this integration. Battery models are also reviewed to understand why balancing is necessary for a string of batteries and how they interact in a charging process. The overarching goal is to find topologies with commonalities to see if integrating the two together is possible. A background of semiconductor fabrication for ICs is also given to size transistor parasitics in terms of device area. Finally, a background of GaN devices is included to provide insight into its use in the discrete hardware prototype.

2.1 Battery Model

Before the topic of battery balancing is introduced, a review of the metrics used to determine a battery's energy and health is explored. The 2S load for a charger has two batteries, each with an equivalent model. Accounting for battery behavior is necessary because it affects the charging and balancing process.

2.1.1 Battery Energy Metrics

One of the most common battery metrics to evaluate the energy in a battery is the state of charge (SOC), the level of charge relative to its capacity. It is necessary to understand the battery capacity

because a battery's voltage potential changes depending on its SOC. SOC is measured across time in percentage points (with 100% SOC representing a battery with full capacity) [3] by

$$SOC(t) = \frac{Q(t)}{Q_{nom}} \cdot 100, \tag{2.1}$$

where $Q(t)$ is the remaining charge at any time, t. Q_{nom} is the nominal battery capacity.

Two common types of SOC estimation are Open Circuit Voltage (OCV) method [4] and the Coulomb Counting (CC) method (also known as Ampere-Hour Balancing Method) [5]. OCV methods use voltage measurements of battery cells and compare the voltages to a known data table for that battery type. SOC tables are commonly available for a battery where each SOC value corresponds to voltage level. Battery voltage, however, varies with battery health and charging current, so OCV does not always report an accurate value. Because of the flat region of the OCV curves in the mid-region, any OCV method errors may lead to a large divergence away from the accurate SOC corresponding to a battery voltage value [4]. An example of a Li-ion battery and its SOC curve is provided for a LIR18650 2600 mAh battery from EEMB. The SOC curve is shown for a range of C-rates in Figure 2.1 [6]. A C-rate measures the rate a battery is charged or discharged compared to its capacity. Starting at full capacity, battery voltage quickly drops during the initial charging process. However, the batter voltage curve has a smaller slope during the middle capacity levels before a sharp decline near battery capacity depletion.

The CC method is also common for battery balancing calculations [4]. This method solves for SOC using initial values of SOC at the initial time, t_0, where

$$SOC(t) = SOC(t_0) + \frac{1}{Q_n} \cdot \int_{t_0}^{t_0+t} I_{Battery} \cdot 100. \tag{2.2}$$

The SOC initial value usually requires an assumption of the state of the battery, so error is introduced into the method. The CC method also incurs accumulation errors across longer time

periods of measurements. In order to gain a more accurate estimate of a battery's energy, state of health (SOH) is a more useful metric. SOH is determined in equation (2.3) where

$$SOH(t) = \frac{Q_{max}(t)}{Q_{rated}} \cdot 100. \tag{2.3}$$

Q_{max} is the maximum capacity of the battery, and Q_{rated} is the rated battery capacity. SOH, the measurement of the battery's ability to provide and store power during recharge, is also measured in percentage points with 100 % denoting a battery at full health. The Depth of discharge (*DoD*) [7], the percentage of capacity that has been discharged $Q_{released}$ compared to Q_{rated}, is

$$DOD(t) = \frac{Q_{released}(t)}{Q_{rated}} \cdot 100. \tag{2.4}$$

SOC is estimated from SOH using equation (2.5) [8] where

$$SOC(t) = SOH(t) - DOD(t). \tag{2.5}$$

The Kalman Filter is an algorithm that is used to evaluate estimations for SOH as well as SOC [9]. SOH is assumed 100 % for a new battery.

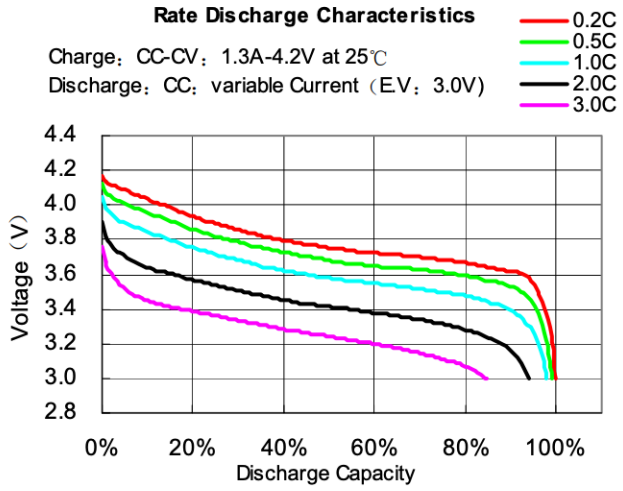

Figure 2.1: LIR18650 2600mAh SOC curve [6].

2.1.2 Specific Charge Profile for Batteries

Now that the metrics for battery energy and health have been introduced, the equivalent model of a battery is explored. The prominent type of battery used for mobile products are Lithium-Ion batteries. As Apple states, Li-ion batteries are "inside every iPhone, iPad, iPod, Apple Watch, MacBook, and Air Pods [10]." These rechargeable batteries universally weigh and cost less, and they offer better overall charging performance than other batteries such as Nickel Metal Hydride (NiMH) and Nickel-Cadmium (NiCd) [11]. The tradeoff with Li-ion batteries is the increased sensitivity to charge, temperature, and current exceeding safe values. A specific charge profile [12] [13] is employed to describe of the sensitive nature of the battery charging process. This profile adheres to three different intervals determined by the battery voltage, V_{Bat}, and its relationship to the threshold voltage, $V_{thes,}$ and the regulation voltage, V_{reg}. Battery systems are designed to never reach full discharge, so the pre-charge interval I does not occur. The maximum charge and discharge current for a Li-ion battery is 1 C, but the modern battery for portable products allows even higher constant charging currents and charging speeds because of the advancements in increased battery ion mobility [14]. Table 2.1 describes each interval of the charging process. Figure 2.2 shows the profile for the voltage and current respectively.

Table 2.1: Specific charge profile for lithium ion batteries

Charge Interval	Interval Name	Battery Voltage	Current Behavior
I	Pre-charge	$V_{Bat} < V_{thes}$	A small current $I_{pre\text{-}ch}$ is used to charge the batteries
II	Constant Current	$V_{thes} < V_{Bat} < V_{reg}$	The battery current holds constant at the charging current I_{ch}.
II	Constant Voltage	$V_{Bat} = V_{reg}$	As the constant voltage interval is engaged, the current decreases non-linearly across time.

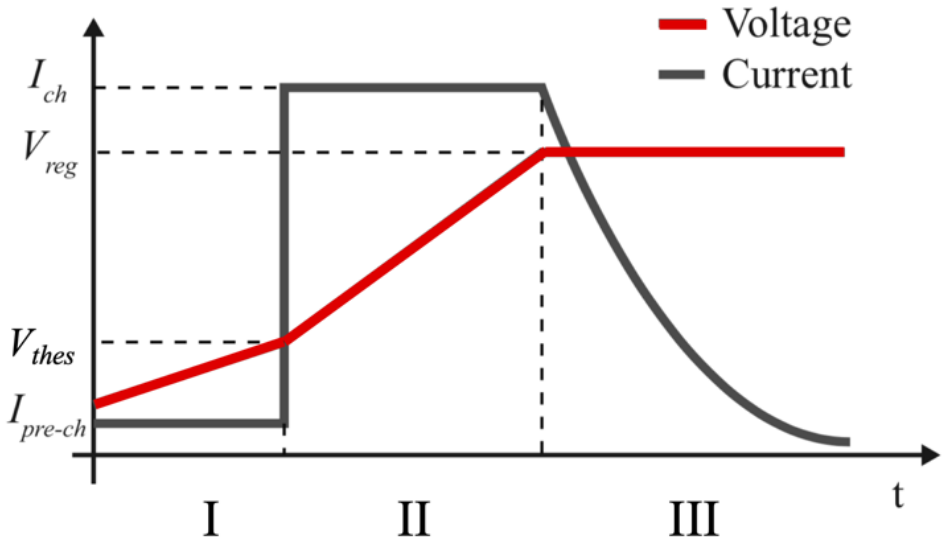

Figure 2.2: Specific charging profile for Li-ion batteries [12] [13].

2.1.3 Battery Equivalent Model

Each battery has an equivalent series resistance (*ESR*). The value of *ESR* changes depending on operating frequency and temperature. The datasheet for a battery provides estimates for a battery *ESR*. The *ESR* is a major reason the terminal voltage of a battery differs from than the OCV, and *ESR* increases over time as a battery cell SOH declines. While there is some thought that large current ripples age batteries more quickly (thus affecting *ESR*), temperature has a larger impact on battery ageing [15], [16]. However, larger current ripples increase conduction loss and therefore battery temperature as well.

An example model for battery is shown in Figure 2.3 and contains resistance, capacitance, and inductances in separate parallel branches. The parallel branches with RC networks define diffusion time constants modeling ion movement in the battery (the example in Figure 2.3 shows two branches for two diffusion time constants). The top branch contains the battery *ESR* in series with a parasitic inductance. BATP represents the positive node of the battery, and V0 represents the negative node. Depending on the frequency range for battery operation, the model can be simplified to a single *ESR* resistance for faster transient simulation runtime. To simulate the battery model, a LTspice simulation is performed that utilizes the known SOC values of a 4.2 V battery. The model is built into the sub-circuit denoted X1 in Figure 2.3. The battery is discharged at 1 C with an initial SOC of 100 %. The results are in Figure 2.4 and show the resulting battery voltage throughout the discharge process across time. The results are comparable to most SOC curves like the example shown in Figure 2.1.

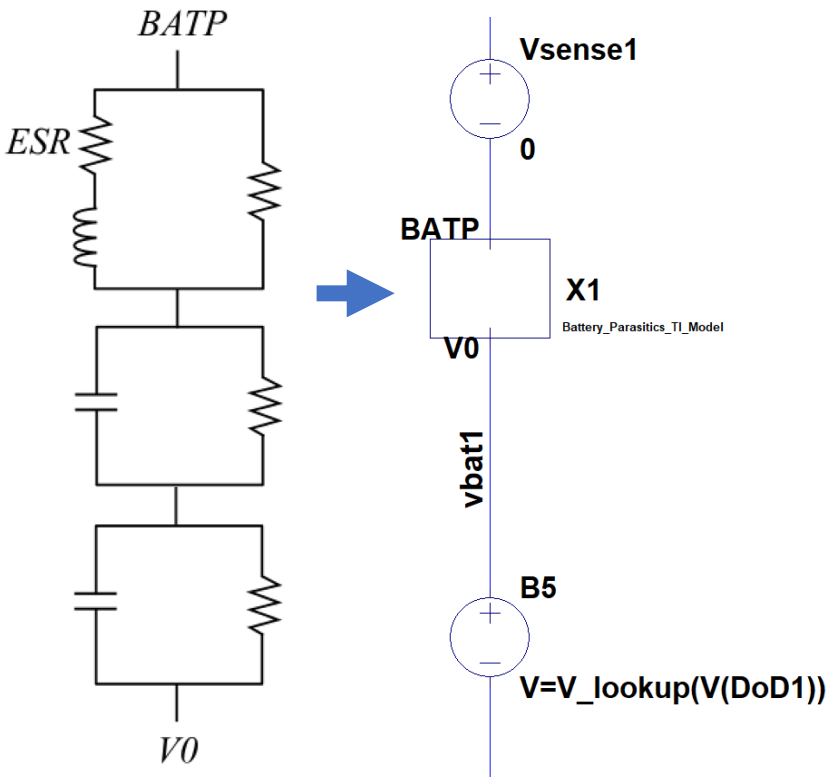

Figure 2.3: Circuit model of a battery.

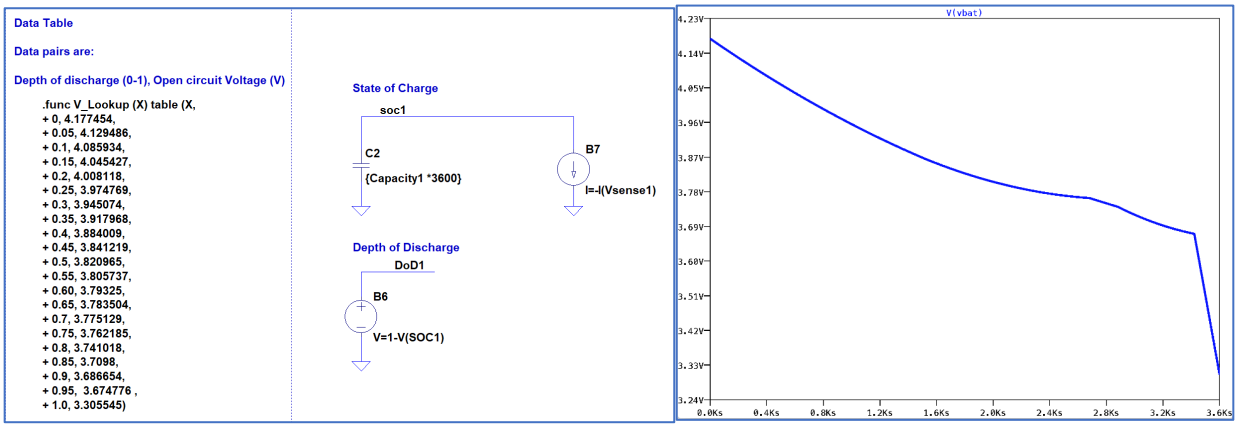

Figure 2.4: Simulated results of the battery discharge the resulting battery voltage.

2.2 Battery Balancing Techniques

Battery balancing serves a critical role in prolonging the life of a string of a batteries. Section 2.2 details why balancing is important and what types of balancing techniques exist to solve this issue.

2.2.1 Battery Balancing

There are inherent inconsistencies among identical batteries owning to the nature of the manufacturing process. These inconsistencies lead to varying internal impedances and discharging rates. Additionally, each battery is exposed to diverse environmental conditions like ambient temperatures [17], [18]. As a string of batteries cycle between the charge and discharge process, balancing the batteries to a common metric yields longer battery life and greater power capability [19]. Balancing also helps prevent overcharge (and discharge) and also saves energy because cell balancing ensures the efficient utilization of all energy throughout each battery cell in series [20]. Essentially, balanced batteries can provide energy for a longer duration of time before being replaced. A string of batteries like the 2S battery configuration needs balancing to provide its full energy capacity. If batteries work longer and more efficiently, this reduces replacement expense.

Figure 2.5 displays three stages of batteries labeled A, B, and C. Battery 2 (the bottom of the 2S configuration in all three stages) charges/discharges at a different rate than Battery 1. In stage B, current flow stops when Battery 2 is fully discharged even though there is energy remaining in Battery 1. In stage C, loss of energy occurs as Battery 1 reaches its Q_{max} first because it started charging with a non-zero capacity. When Battery 1 is fully charged, the charging process stops even though Battery 2 is not fully charged itself. Over time, this imbalance decreases charging effectiveness because the battery system has less available energy than it did before discharging.

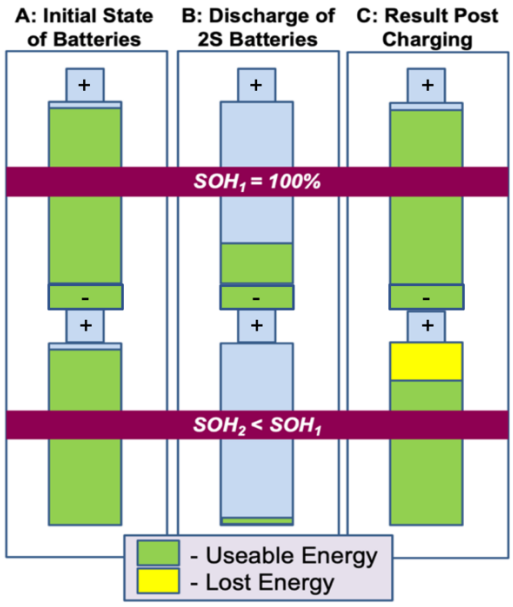

Figure 2.5: Demonstration of battery imbalance leading to lost energy for a 2S battery cell.

There are two distinct categories of battery balancing, passive and active, to prevent battery charging imbalance. Imbalance limits the available capacity of a string of batteries to its weakest cell. Passive balancing usually involves the dissipation of energy across a resistor. Here the battery with more energy dissipates its extra energy until the balancing metric used (such as SOC or SOH) is the same for both batteries [21]. However, it leads to higher power loss. Because each IC handles a limited amount of heat dissipation resulting from the P_D, it is not a suitable choice for integrated battery balancing.

Active balancing extends battery life by intelligently redistributing charge of the batteries in a multi-cell system with a sensed battery metric during either the charge or discharge process [19]. This non-dissipative balancing achieves faster balancing and more efficient battery charging. When SOH is the metric used for active balancing, this also increases battery lifetime by mitigating effects of differential aging between each battery. Some active balancing techniques require more precise control to initiate balancing which increases the required system complexity. While active

balancing requires a higher cost for additional control circuitry, this is possibly offset by the functional integration of combining the balancer and charger onto a single chip. To further investigate, topologies for active balancing are explored next.

2.2.2 Balancing Circuit Topologies

An active balancing module may be realized through several types of topologies. A half-bridge resonant circuit with continuous control [22] [23] equalizes cell voltage. Resonant converters time the switching transistors at zero current switching (ZCS) or zero voltage switching (ZVS) to decrease switching loss thus improving efficiency in many implementations [24] [25] [26]. Figure 2.6 shows E_{ov}, the overlap energy, lost in switching transitions due to the overlap of non-zero V_{ds}, the drain to source voltage of a MOSFET, and non-zero i_D, the drain current. ZVS and ZCS are soft switching techniques enabled by the controlled resonant behavior of resonant circuits.

This behavior is achieved through inductor and capacitor networks varying the current and voltage waveforms sinusoidally during a specified sub-circuit of a switching system [27]. A disadvantage of this type of converter is that voltage on the resonant elements are up to four times as large as the supply and thus the transistors require high blocking voltage. Devices rated with higher blocking voltages have higher figure of merit (FOM) which is calculated as

$$FOM = r_{ds,on} \cdot Q_g, \tag{2.6}$$

where $r_{ds,on}$ (or r_{on}) is the drain-to-source resistance when a MOSFET is turned ON with an applied V_{gs} and Q_g is the gate charge. Transistors with higher FOM lead to more power loss because of the larger parasitics present in the device. For high current applications like battery chargers, conduction loss is one of the dominant sources of loss, so lower FOM can yield lower r_{on} values (for the same Q_g as a higher FOM device) which lowers conduction loss.

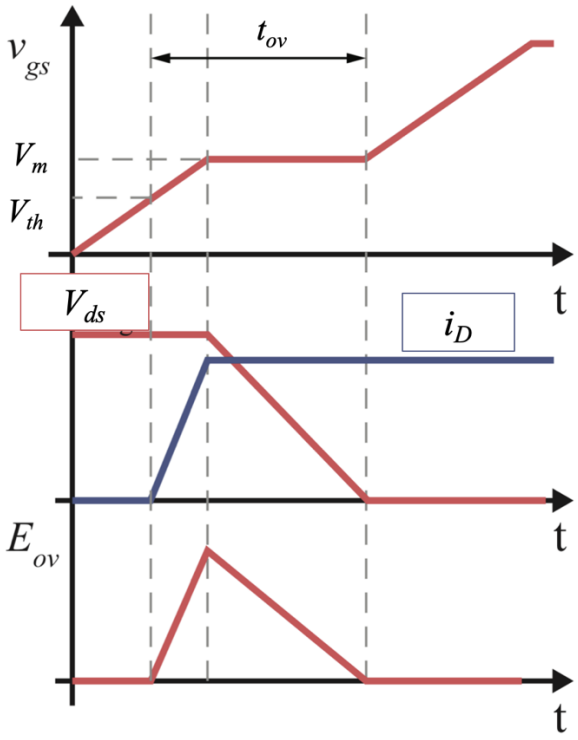

Figure 2.6: Hard switching loss.

Other active balancing techniques incorporate a transformer as the energy transfer component. There are various ways to implement the transformer for active balancing such as multi-winding or switched transformers [24]. There is ongoing research into the size reduction of transformers like reducing the required windings for cell equalization [28]. The transformers tend to be a larger magnetic components. Typically, balancing with transformers is more applicable in hybrid electric vehicles [29], and transformers in general are expensive so efforts are made to reduce the cost of implementation [30].

Another common type of circuit used for active balancing is the switched capacitor converter (SCC) [31] [32] [33]. A basic topology for a ladder-type SCC converter is shown in Figure 2.7. The switched capacitor converter utilizes a flying capacitor to redistribute charge, and it is

commonly used for cell voltage equalization. No magnetic components are required for the SCC. The modulation for the SCC (shown in a three-level configuration in Figure 2.7) has two signals g_1 and g_2 that are complementary. Over one period, g_1 turns ON for half the period. As g_1 turns off, g_2 turns ON for an equal duration as g_1 to complete the period. This mechanism of switching equalizes the battery voltage of V_{cell1} and V_{cell2} without any prior detection of battery voltage. The cell voltages are

$$V_{cell1} = V_{Bat1} + ESR1 \cdot I_{out}, \tag{2.7}$$

and

$$V_{cell2} = V_{Bat2} + ESR2 \cdot I_{out}. \tag{2.8}$$

where I_{out} is the output current, *ESR1* is the *ESR* for Battery 1, and *ESR2* is the *ESR* for Battery 2. Essentially no control is needed. A trade-off for this type of converter is longer balancing times required to equalize cell voltage [23]. If the voltage drop across the battery *ESR* is negligible, then the battery cell voltage, V_{cell}, is equal to V_{Bat}.

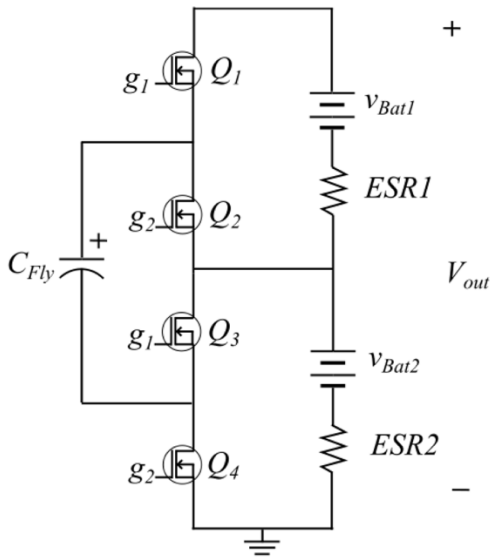

Figure 2.7: Switched capacitor converter (SCC) [31, 20] [32] [33].

More benefits of the SCC include simultaneous balancing with the charging process, no disturbing of battery protection circuitry, and ceasing the consumption of additional energy after the cells have balanced [34]. The conclusion of [34] which tested a string of six batteries states the balancing for these batteries took place in a reasonable amount of time and much faster than passive balancing strategies, but the balance time may not be as fast as other balancing topologies. While SCC balances any number of cells, each added cell requires more circuity. Every n cells in a series string needs $2n$ switches and n-1 flying capacitors. Therefore, the conversion ratio is limited to the topology structure. Longer strings add complexity in terms of providing the power for each non-ground referenced gate driver, and there reaches a point where power loss through the *ESR* of a large number of capacitors becomes significant. Each transistor only needs to block half of the cell voltage, so lower voltage rated devices are used. This decreases the FOM of the MOSFETs utilized.

SCC have an output resistance R_{eff} determined by the frequency of operation. The boundary condition is f_{crit}, the critical frequency for an SCC. At the slow switching limit (SSL) where the frequency is below f_{crit}, R_{eff} depends on the charging and discharging of the flying capacitor. The other region, the fast switching limit (FSL) , has a R_{eff} dominated by the *ESR* of the flying capacitor and the drain-to-source resistance of the transistors [35]. In FSL, R_{eff} is not dependent on frequency.

2.3 Battery Charger Topologies

DC-DC switching converters are examined in the next sections for their abilities to handle a large input range and achieve high efficiency. DC-DC switching converters are chosen over linear converters (that use a pass transistor to drop the input to a specified output voltage) because of

these traits (input voltage range and higher power efficiency) despite involving more circuit complexity.

2.3.1 Buck Converter

In conventional two-level converters such as the boost and buck that are implemented for high-current applications, transistors with small FOM are selected to reduce loss. Only two transistors are required, and each is chosen with a V_{BR}, the MOSFET breakdown voltage, that handles the full drain-to-source voltage plus a safety factor. Figure 2.8 shows the topology of a conventional two-level buck converter. Switching loss increases at high frequency, so the efficiency and power density is related to the available transistors to a designer and the operation required for the converter. As frequency increases, the conduction loss increases with regards to the current ripple on the inductor. The conversion ratio *M(D)* for a buck converter is

$$M(D_{buck}) = \frac{V_{out}}{V_{in}} = D_{buck}, \tag{2.9}$$

where D_{buck} is the duty cycle for the converter.

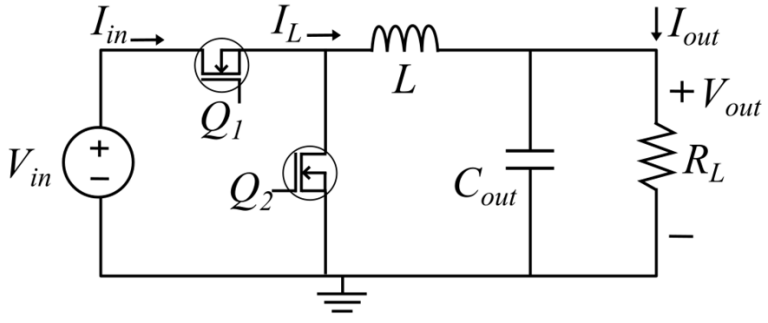

Figure 2.8: Two-level buck converter.

A buck converter implemented in an integrated application fabricated with a standard complimentary metal-oxide semiconductor (CMOS) technology is shown in [36] with its layout in Figure 2.9. The IC includes all of the converter circuitry and control, but the output current is limited to 400 mA and the output voltage to 1 V at a maximum efficiency of 53 %. Typically fully-integrated converters incorporating buck and standard CMOS fabrication have limited output capabilities because the value of the integrated inductances and capacitances are lower than larger discrete counterparts. It is difficult to make high quality factor, Q_f, integrated inductors because of the high resistivity (mΩ/square) of the metal layers making the inductor DC resistance as high as 250 mΩ/nH [37]. High current applications require external discrete energy components unless a new inductor fabrication technique is designed. Including a boost stage at the output of a buck would allow a converter to fully utilize the available inputs for USB 3.0 PD which has input voltages that are greater than the battery voltage.

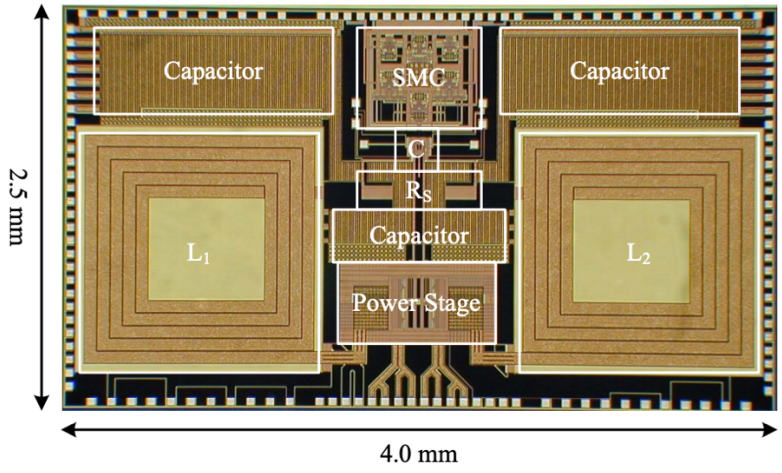

Figure 2.9: Layout of fully-integrated buck converter with integrated inductors L_1 and L_2 in [36].

2.3.2 Resonant Switched Capacitor Converter

The resonant switched capacitor converter (ReSCC) includes an inductor in series with the flying capacitor in SCC topology [38] [39]. The topology of the 3X Dickson ReSCC with an indirect resonant core operates above resonance in [39]. One of the main advantages occurs at the SSL where the charge sharing losses (caused by voltage mismatch) and R_{eff} are reduced to a minimum. In [40], ReSCC converters accomplish a minimum R_{eff} comparable to SCC but at lower frequencies. The work in [40] compares direct and indirect ReSCC topologies with SCC converters and incorporated air-core solenoid inductors of a few nanohenries. Efficiency less than 86 % is achieved at 3.35 W and an output current of 1.2 A, and the fabrication of the IC used a 0.18-µm bulk CMOS process. ReSCC direct and indirect implementations are shown in Figure 2.10 [40]. Direct topologies connect the resonant inductor permanently to the output which helps reduce inductor frequency content.

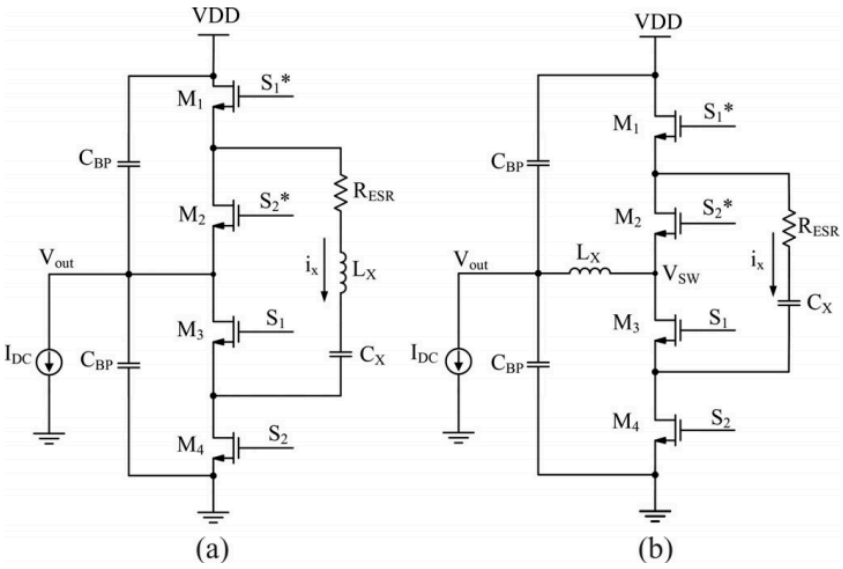

Figure 2.10: Indirect (a) and direct (b) ReSCC topologies [40].

While ReSSC also minimizes the size of the passive components, the converter experiences high peak stresses and limited voltage regulation. Other disadvantages for the ReSSC are the same ones mentioned in Section 2.2.2 like the voltage conversion ratio being limited by the converter structure. This work needs to provide a converter that can operate with a wide range of inputs based on USB 3.0 PD input specifications. High peak stresses are also a concern for IC designs, especially for small area mobile applications, because only a limited area is available for magnetics. Small-scale inductors have smaller saturation currents, so the inductor saturates at high peak stress intervals leading to large ripple, less energy storage in the component, and more loss. Additionally, higher rms currents lead to more conduction loss, so small inductors of only a few nanohenries like the air-core inductors mentioned may not be conducive to high power efficiency.

2.3.3 Flying Capacitor Multilevel Converters

The topology of a flying capacitor multilevel converter (FCMC) bears a resemblance to the previously described SCC but includes an inductor at either the input or output. Regulation of the output voltage in FCMC is possible through the control of the duty cycle. If the FCMC provides fast charging at high efficiency, the converter is possibly an option for integrating with a balancing circuit like the SCC to meet the goal of creating a single IC with both charging and battery balancing capabilities.

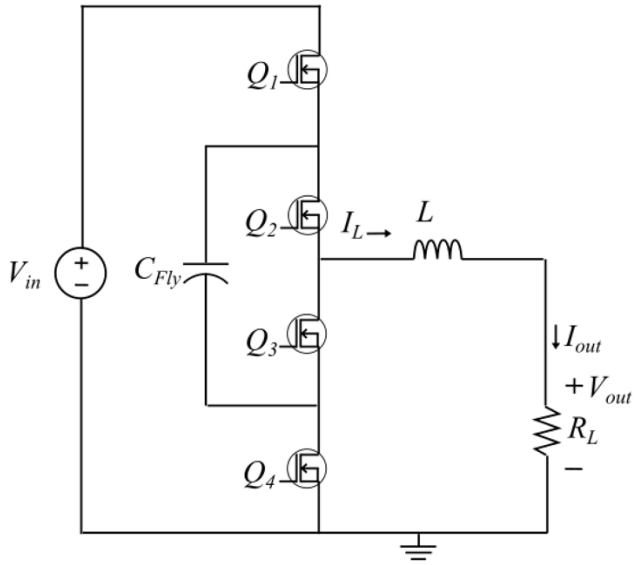

Figure 2.11: Three level FCMC buck converter [41] [42] [43].

A FCMC utilizes a flying capacitor and two additional transistors as compared to the convention two-level converter. In Figure 2.11 a FCMC three-level buck [41] [42] [43] is shown that achieves the same functionality and conversion ratio as the two-level buck converter. The modulation for the three-level topology is shown in Figure 2.12 which consists of two complementary pairs of signals.. Each of the four transistors in the three-level converter have a lower FOM than the ones in the two-level buck because each FET needs to block half of the input voltage. This is a promising result that not only facilitates increased converter efficiency but allows better integration of transistors based on the relationship between area and device parasitics discussed in Section 2.4.4. Both Q_1 and Q_2 operate with an ON-duration of $D_{buck} \cdot T_s$, but Q_2 is phased-shifted half a period.

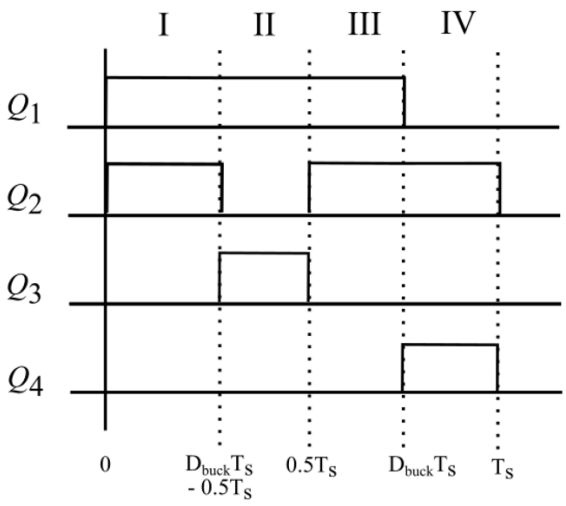

Figure 2.12: FCMC modulation for a three-level buck.

By placing the inductor at the input, the FCMC becomes a three-level boost [44] [45] [46]. The same functionality is achieved as a two-level boost converter, but the four transistors of a FCMC three-level boost are sized to half of the output voltage as opposed to the full output voltage in the two-level case. Figure 2.13 depicts a three-level boost converter. Both g_1 and g_2 operate with an ON-duration of $(1\text{-}D_{boost})\cdot T_s$. The conversion ratio for the boost is

$$M(D_{boost}) = \frac{V_{out}}{V_{in}} = \frac{1}{1 - D_{boost}}. \tag{2.10}$$

Another advantage of the FCMC is that smaller magnetics achieve the same current ripple as a two-level version [47] [48]. The maximum current ripple (for a given frequency and inductance) is determined by solving for the inductor current with a given charging current I_{out} and boost duty cycle D_{boost}. The maximum current ripple point occurs for a D_{boost} of both 25 % and 75 % according to behavior of the three-level boost as seen in [49] and Figure 2.14 where T_L is the charging time of the inductor and V_L is the inductor voltage. The inductor current ripple is defined as half of the peak-to-peak current value through the switching period.

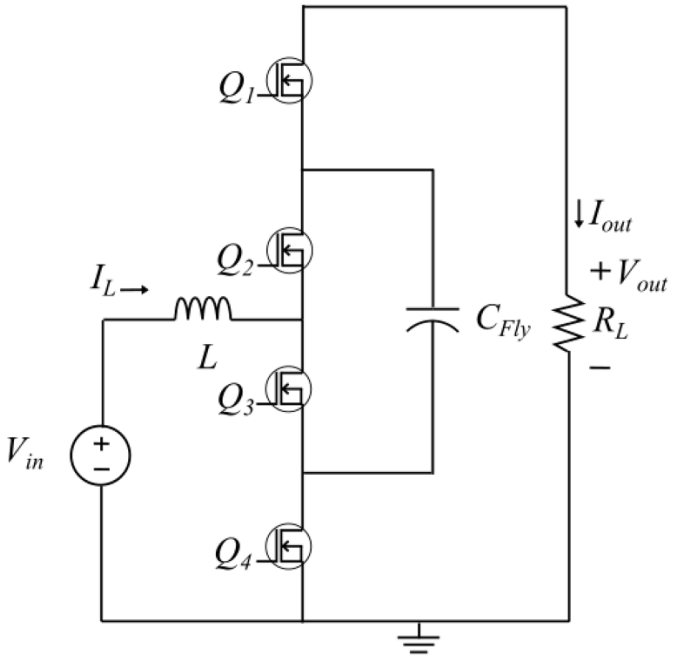

Figure 2.13: Three-level boost converter.

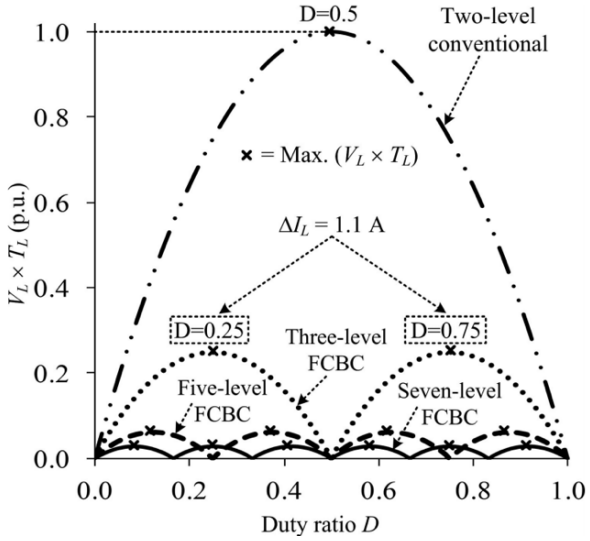

Figure 2.14: Maximum current ripple vs duty cycle [49].

As [49] indicates, the conventional two-level boost converter has a minimum inductance required for the maximum current ripple for a D_{boost} of 50 % of

$$L_{2-Levelmin} = V_L T_L \frac{1}{2\Delta i_L} = \frac{V_{out}}{2}\frac{T_s}{2}\frac{1}{2\Delta i_L} = \frac{V_{out}T_s}{8\Delta i_L}. \tag{2.11}$$

At D_{boost} = 50 % for the conventional boost, the V_L is half of the output voltage and the T_L is half of the switching period. For the three-level flying capacitor boost converter (FCBC), the minimum inductance at the maximum ripple point is

$$L_{3-Levelmin} = V_L T_L \frac{1}{2\Delta i_L} = \frac{V_{out}}{4}\frac{T_s}{4}\frac{1}{2\Delta i_L} = \frac{V_{out}T_s}{32\Delta i_L}, \tag{2.12}$$

where V_L is a quarter of the output voltage and T_L is a quarter of the switching period. A fourth of the inductance is needed for the three-level converter as compared to the two-level.

While the three-level converter operates with a smaller inductor, the other passive component, the flying capacitor (C_{fly}), can also be sized to a minimum value. Finding the minimum C_{fly} allows for better power density needed in mobile applications. A study in [48] based on the maximum voltage each transistor can handle for a three-level boost solves for the minimum flying capacitance where

$$C_{fly,min} = \frac{P_{in} \cdot D_{boost}}{\left(2V_{cfy,max} - V_{out}\right) \cdot V_{in} \cdot f_s}. \tag{2.13}$$

Later sections will address additional benefits of sizing C_{fly} to a minimum.

2.3.4 Integrated Charger-Balancer Solution

While there exists modern commercial products listed in Table 1.2 that provide balancing or charging capabilities, the goal of this work is to integrate a charger topology onto a single IC with balancing functionality. The IC must handle high current at high efficiency to allow fast charging times without exceeded the thermal constrains of the chip. The TI BQ25887 [50] is a boost-mode

charger with balancing for 2S configurations that has over 93.4 % using a 5 V adapter. VQFN package of 4.00 mm by 4.00 mm is used for this IC. However, the BQ25887 charges with 1 A current at an efficiency of 93.4 %. The maximum charging current is 2 A but at lower efficiency. The input voltage range is limited between 3.9 V and 6.2 V, and over this range the maximum balance current is 400 mA. In [51], a multi-secondary winding transformer balancing circuit is designed for a string of Li-ion batteries in electric vehicles. The controlled passive balancing uses shunt resistors, but the conclusion of this work states that high losses occur if there is a large initial voltage difference between batteries. As previously stated, passive balancing with shunt dissipation can yield higher losses. Additionally, the topology is not applicable for mobile circuit integration because the winding transformer's large size. While it has been shown in this section that there exists topologies that both balance and charge 2S batteries and even at the integrated level, a charger that still utilizes high charging current and efficient balancing needs to be addressed.

2.4 Integrated Power Converters

For the battery charger design, the eventual goal is to integrate the transistors onto an IC for mobile applications. Integrated transistors involve additional parameters in converter design as compared to its discrete counterparts. An overview of these integrated transistors, specifically those for high power applications that are used in this battery charger design, is detailed.

2.4.1 Overview of Integrated Transistors

The integration of power converters on an IC provides challenges. Energy storage components have much smaller capacitances and inductances that are integratable on-chip because of

technology limitations as discussed in Section 2.3.1. While there is research to improve the magnetics of small-scale IC components [52] [53], the charger examined in this paper only explores the integration of transistors on-chip with external connections to the capacitors and inductors as needed. Loss models for transistor parasitics in integrated power converters include an additional design parameter compared to traditional discrete models. With small areas available to design, the transistor's parasitic parameters used in the loss analysis are characterized in terms of per area or per width parameters [54]. The area of a transistor is characterized in terms of the transistor's gate channel width, W, and channel length, L_g. The area, A, of the device is characterized by

$$A = W \cdot L_g. \tag{2.14}$$

Semiconductors are fabricated on raw Silicon wafers by doping. Donor regions are called *n*-type, and acceptor regions are called *p*-type. Devices that are *n*-channel are fabricated on a *p*-type wafer by doping a Silicon wafer with *n*-type donor atoms. In general, holes are more strongly coupled to an atom's nucleus, thus electron mobility is greater than hole mobility [55]. For the semiconductor fabrication process, the active layers determine the openings in the oxide. Active layers are then doped to either a *p* or *n*-type. For example, a *n*-well process has *p*-substrate and heavily doped *n* region (the *n*-well). NMOS (*n*-channel MOS) has *n*+ regions (the drain or source) of a device that lay in the *p*-substrate. PMOS (*p*-channel MOS) has *p*+ regions that lay in the *n*-well. In general, the quality of a NMOS in a *p*-well process is not as good as the quality of a *n*-well process. The gate is created with polysilicon (poly) that is made of tiny crystalline regions of Silicon. Gate poly is highly resistive, so silicide is used to reduce its overall resistance.

The movement of carriers in a semiconductor happens through either drift and diffusion [56]. The drift current is the uniform movement of carriers in one direction in response to an electric

field. Diffusion current in semiconductors is the movement of carriers from high concentration to lower as a result of entropy. This is the type of current transfer that takes place across a *pn* junction. A *pn* junction also has a junction capacitance (depletion capacitance) that is a function of the applied voltage. A depletion region forms within the *pn* junction because of the diffusion currents producing excess minority carriers on other side of the junction and creates this capacitance [55].

2.4.2 Semiconductor Fabrication Technology

For a given semiconductor fabrication technology node (that specifies a minimum L_g for the channel), there is a maximum supply voltage V_{DD} for the process. As semiconductor technology continues to scale to smaller channel lengths, V_{DD} has scaled down accordingly [55]. Figure 2.15 shows the V_{DD} for a few technology nodes [57]. There are many advantages for scaling to a smaller technology node as each device for a respective node takes up less area leading to increased circuit density, and there is less power required because V_{DD} is smaller [56]. However, for power electronics, the maximum V_{DD} for digital circuits is often too small for high power applications to use the MOSFETs available in a technology node. For the battery charger in this work, a device that withstands a higher V_{ds} is required. Modern IC technology limits the choice of transistor to only lateral devices (where the dominant flow of current is directed horizontally). Vertical devices conventionally used in power electronics handles higher blocking voltages and current ratings [58], but they do not lend themselves to integration with other circuits on the same substrate.

				SimulatedPerformance of Inverter		
Production Year	Technology Node (nm)	Technology Type	V_{DD} (V)	Delay (ps)	Energy (fJ)	Power (μW)
1999	180	Bulk	1.8	77.2	27.5	105
2001	130	Bulk	1.2	34.7	5.20	26.1
2004	90	Bulk	1.1	26.5	2.62	13.0
2007	65	Bulk	1.1	19.8	1.72	8.58
2008	45	High-k	1.1	10.9	1.05	5.19
2010	32	High-k	0.97	9.8	0.51	2.47
2012	20	Multi-Gate	0.9	9.66	0.198	1.51

Figure 2.15: Characteristics of various technology nodes [57].

IC Process Design Kits (PDK) for computer aided design, (CAD), tools are given for a technology node. Because r_{on} increases with L_g, minimizing L_g can decrease conduction loss for a design. However, choosing the minimum L_g for a technology process presents challenges when this equivalent L_g is shorter than 1 μm. Design parameters are less straightforward with short channel effects than the long channel processes (L_g > 1 μm), and the approximations allowing simplified characterization for long channel devices is not an option for short channel ones [56]. Because of this, designers that use technology nodes with minimum channel lengths less than 1 μm often size the L_g at four to five times the minimum length for analog design. The resulting equivalent length of the transistor allows the device to be characterized without short channel effects. While this is especially important for analog circuit designers, the power transistors available in CMOS processes often offer a fixed L_g per device.

2.4.3 LDMOS

With only lateral devices available, a common selection of a MOS device that achieves higher blocking voltages than other MOS structures is an LDMOS (laterally double-diffused MOSFET). LDMOS is useful in many integrated power electronic applications [59] [60] [61]. It is one of the most prominent choices for integrated high power transistors because existing semiconductor

technologies can fabricate this device on ICs [62]. These devices include short, heavily doped backgates and long, lightly doped drift regions [55] for the drain structure that are suitable for the high-voltage application. Because the increased length and low doping of the drift region increases drain resistance, design advancements for LDMOS and its planar *pn* junction have optimized how long the drift region needs to display the tradeoffs of cost (increased area), low drain resistance, and high breakdown voltage [63] [64] [65]. A structure for LDMOS is in Figure 2.16.

The source and drain contacts are *n*+ active layers that prevent the formation of a Schottky diode at the metal-to-*n* junction. It is common to find nLDMOS structures with a butted source that includes the body contact. The *p*-body layer, also referred to as high voltage *p*-body (HVPB), under the source is selective *p*-type (*p*-type implanted region). The *p*-body is tied directly to the bulk (body) to eliminate the body effect [56]. The inversion channel underneath the gate is formed in this layer with an applied V_{gs}. Once the inversion layer is created, current flows from the *n*+ source to the high voltage *n*-well (HVNW), which is an *n*-type EPI layer (named EPI by its formation through epitaxial growth). This lightly doped layer is essentially a resistor in series with the drain, and it allows the channel to withstand higher blocking voltages. The addition of this longer and lightly doped *n*- drift region absorbs the depletion layer of the reverse-biased junction formed from the *p*-body and itself. Finally the current proceeds to flow into the heavily doped *n*-type drain drift region (NDD) layer which surrounds the *n*+ drain. Sometimes there is an additional layer called SH_N which has a higher doping level than NDD that is placed beneath it. This essentially decreases the drift region resistance.

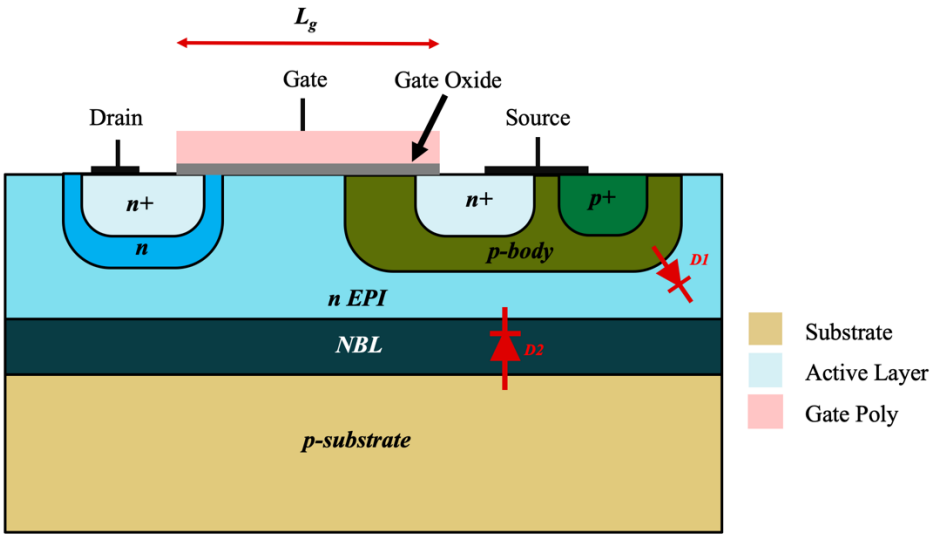

Figure 2.16: Conventional nLDMOS cross-section.

The $n+$ buried layer (NBL) increases isolation capability. This isolation tub prevents the punch through effect [66] that occurs with lower doped drift regions and reduces resistivity because of the $n+$ layer. This NBL contact ring is tied to the maximum voltage node to ensure the parasitic diode formed from the p-substrate to the NBL region as seen in Figure 2.16 never turns-on. The body contact is $p+$. A deep p-well (DPW) is added with the NBL ring to isolate the bulk if the bulk is not referenced to ground. If an additional $p+$ isolation ring (not shown Figure) is needed, this ring is tied to the lowest potential voltage node.

2.4.4 IC Transistor Parasitics In Terms of Area

The LDMOS parasitics considered are on-resistance r_{on} ($r_{ds,on}$) for conduction loss, output capacitance C_{oss} for switching loss, Q_{sw} for switching loss, and Q_g for gate charge loss (see Table 2.2). Specific values for each of these parasitic parameters are calculated using the test circuits shown in Figure 2.17 so that parasitics described above are determined for a given area.

Table 2.2: MOSFET Parasitic Parameters

Parasitic	Value	Description	Units
R_{sp}	$r_{on} \cdot A$	On-resistance per unit area	$\Omega \cdot mm^2$
$C_{oss,sp}$	C_{oss}/A	Output capacitance per unit area	F/mm^2
$Q_{g,sp}$	Q_g/A	Total gate charge per unit area	C/mm^2
$Q_{sw,sp}$	Q_{sw}/A	Switching charge per unit area	C/mm^2

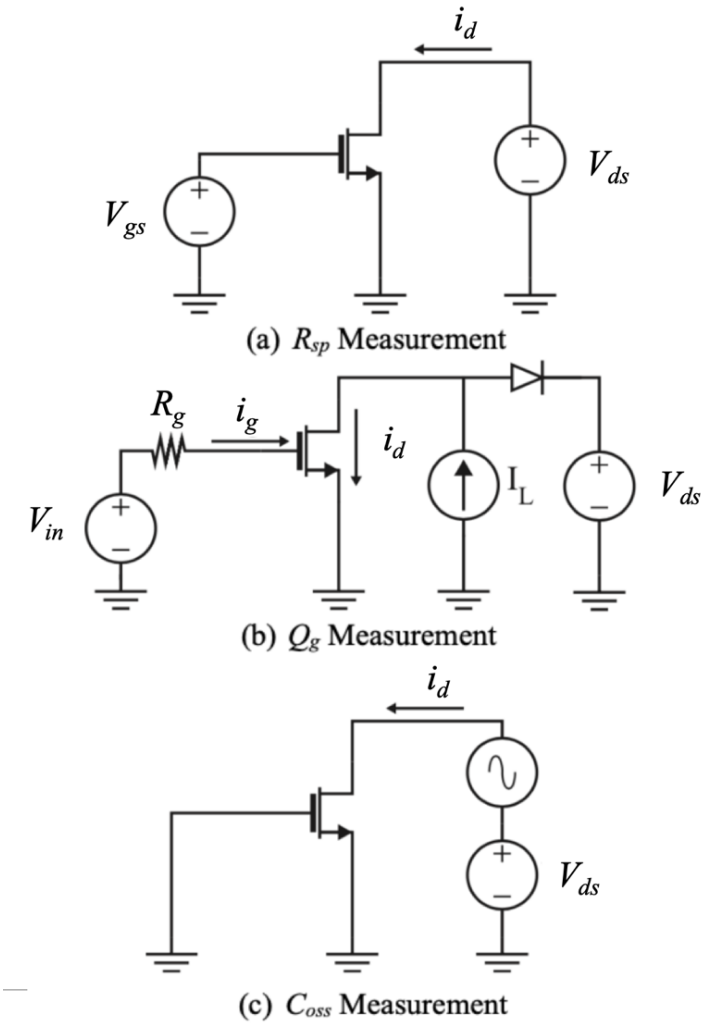

Figure 2.17: Test circuits for parasitic parameter extraction [11].

Simulation tools in Cadence are used to determine the device parameters for the available devices. The three regions of operation for a MOSFET in terms of changes to V_{gs} in this analysis are shown in Table 2.3. For the on-resistance of a MOS device, the linear (ohmic) region is evaluated. The test circuit provides a small DC bias to emulate V_{DS} (the magnitude here needs to establish the device operation in the linear region) and a V_{GS} is applied so the transistor is fully turned ON (sufficiently above the threshold voltage V_{th}). The on-resistance in the linear region (determined through the W/L_g ratio) is

$$r_{on} = \frac{1}{k'\left(\frac{W}{L}\right)(V_{gs} - V_{th})}, \tag{2.15}$$

where V_{th} is the threshold voltage. The constant k' is equal to $\mu_n C'_{ox}$ for n-channel devices. The electron mobility μ_n is typically 250μA/V^2. C'_{ox} is the capacitance of the gate oxide and equal to

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}, \tag{2.16}$$

where ε_{ox} is the permittivity of the oxide, ε_0 is the permittivity of the free space, ε_r is the relative permittivity for a dielectric, and t_{ox} is the thickness of the oxide. The thickness of the oxide t_{ox} is dependent on the technology node. Because these values are dependent on the process, the IC designer cannot change these parameters.

Table 2.3: Regions of Operation for a MOSFET

Region of Operation	Value of Gate-to-Source Voltage
Cutoff	$V_{gs} \leq V_{th}$
Linear (Triode / Ohmic)	$V_{gs} > V_{th}, \quad V_{ds} \leq V_{gs} - V_{th}$
Saturation	$V_{gs} > V_{th}, \quad V_{ds} > V_{gs} - V_{th}$

If the MOSFET V_{ds} voltage is increased to the point past the pinch-off locus where the device operates in the saturation region as seen in the *I-V* curve in Figure 2.18., the drain current i_d no longer increases linearly with increasing V_{ds} as is the case in the linear region. While saturation operation may allow the device to operate as a current source controlled by V_{gs}, this region would not be ideal for a transistor acting as a switch due to a much higher r_{on}. A device with larger W has a smaller r_{on}, and this is particularly important for charging circuits with high current applications to decrease conduction loss. Finally, for a given active area A, the specific on-resistance R_{sp} is evaluated and equivalent to

$$R_{sp} = r_{on} \cdot A. \tag{2.17}$$

For the test circuit evaluated in Figure 2.17(a), the area given to the transistor is used in simulation. Because R_{sp} varies with device area and aspect ratio (gate width divided by gate length), it is important to choose area for the test circuits close to the area used in the circuit design. One value of R_{sp} is accurate for a range of up to two to three times the device area and aspect ratio [55]. This is attributable to a variety of factors including metallization and does not account for resistance of the bond wires and package lead frame. The variance also largely depends on the layout of the device.

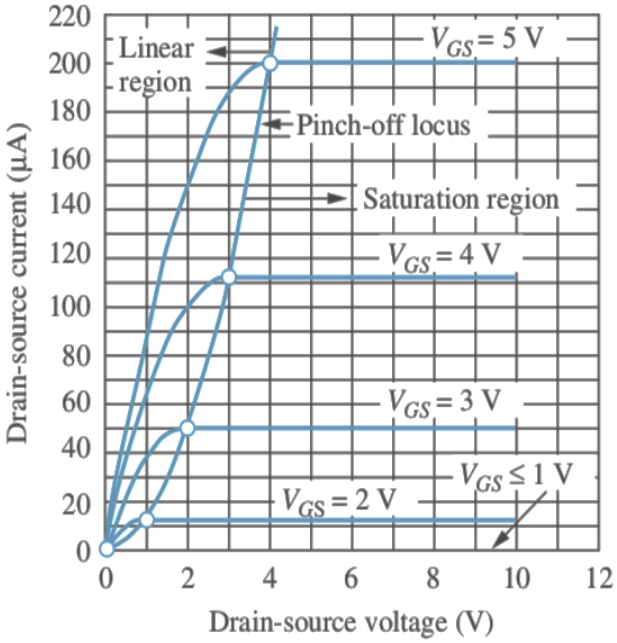

Figure 2.18: The *I-V* curves for a MOSFET device [67].

To evaluate Q_g, the charge flowing into the gate, test circuit in Figure 2.17(b) is used. A gate resistance is determined to do the calculation. As the gate is turned ON with an applied V_{gs}, the charge is calculated by observing the gate current i_g during the rise time t_{rise} for V_{gs} to rise to its maximum value.

$$Q_g = \int_0^{t_{rise}} i_g dt\,. \tag{2.18}$$

Once Q_g is calculated using the integral, the specific gate charge $Q_{g,sp}$ is

$$Q_{g,sp} = \frac{Q_g}{A}. \tag{2.19}$$

Using the same test circuit from Figure 2.17(b), the miller plateau of the transient waveform of V_{GS} is used to calculate Q_{SW} as seen in Figure 2.19. Cadence simulation tools solve for the DC

operating point and provide the value of V_{th} for a device with its respective area. The gate current is found through transient simulation using the circuit from Figure 2.17(b).

The output capacitance C_{oss} that occurs when the gate is shorted to the source is determined utilizing the final test circuit in Figure 2.17(c). C_{oss}, consisting of C_{gd} and C_{ds}, is dominated by C_{ds}. C_{ds} is the result of the reversed-biased junction between the lightly doped *n* layer (*n*-well) and the *P*-body. The parasitic capacitances are shown in Figure 2.20 of a nLDMOS without the NBL layer. This circuit operates with the device in cutoff by connecting the gate of the *n*-channel device to ground (same as source and *p*-body). In addition to the DC bias of V_{ds}, a smaller AC signal of 100 mV amplitude is applied in series with the DC source. As the input signal charges the C_{gd} and C_{ds} parasitic capacitances, the following characteristic is observed for the drain current where

$$\widehat{i_d} = C_{oss|V_{ds}} \frac{d\widehat{v_{ds}}}{dt}. \tag{2.20}$$

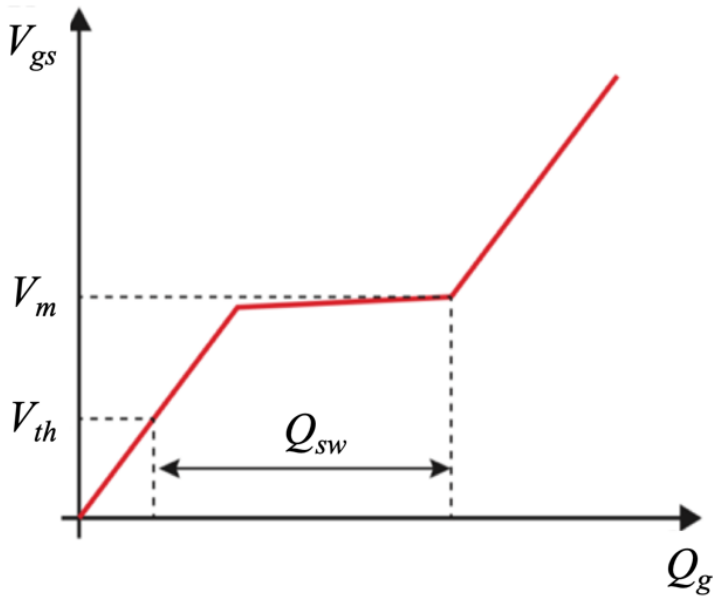

Figure 2.19: Gate charge plot and Q_{sw}.

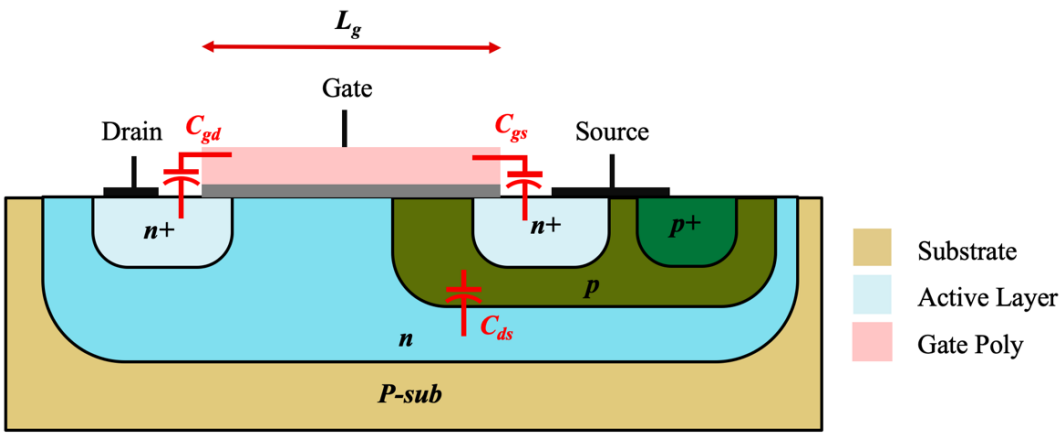

Figure 2.20: nLDMOS cross-section with parasitic capacitances.

During the test, it is important to size the AC and DC sources to not exceed the maximum V_{ds} rating. Utilizing a transient simulation, C_{oss} is solved by dividing the peaks of i_d by the derivative of V_{ds} at the corresponding time interval. The specific output capacitance is then solved in the following equation. C_{oss} is directly proportional to the MOS device's width,

$$C_{oss,sp} = \frac{C_{oss}}{A}. \tag{2.21}$$

There exists a non-linear relationship between C_{oss} and V_{ds}, but to find a more useful relationship between the two, an equivalent linear capacitance is modeled as seen in [68]. The energy $C_{eq,E}$ and $C_{eq,Q}$ are modeled in a way that equivalent capacitance is calculated linearly across V_{ds} without its normal dependence on the same voltage where

$$C_{eq,E} = \frac{2}{V_C^2}\int_0^{V_c} vC_x(v)dv\,, \tag{2.22}$$

and

$$C_{eq,Q} = \frac{2}{V_C^2}\int_0^{V_c} vC_x(v)dv\,. \tag{2.23}$$

$C_{eq,E}$ and charge $C_{eq,Q}$ allows a more accurate analysis of switching loss. These parameters, once derived in simulation, are used to model the losses of the circuit and influence design decisions regarding area.

2.5 Gallium Nitride (GaN)

For the first discrete hardware prototype, enhancement mode Gallium Nitride (GaN) devices are utilized for the battery charger's transistors that act as switches. Offering many attractive qualities for power electronics applications, GaN became commercially available in 2009 by Efficient Power Conversion Corporation (EPC) [69]. GaN is one of the wide bandgap (WBG) materials, and when GaN transistors are used in converters, they can allow better power efficiency, lower cost, less weight, and greater power density than converters using Si devices. WBG materials have a large bandgap, the range of energy difference between the conduction band and the valence band in the material. Semiconductors themselves have small bandgaps (1-4 eV) while conductors have even smaller bandgaps. However, materials with bandgaps larger than Silicon's handle higher temperatures and voltage ranges with minimal degradation. Table 2.4 offers a comparison of Silicon's bandgap with those of WBG devices like GaN and Silicon-Carbide (SiC).

Table 2.4: Comparison of Bandgap Energy in Semiconductors

Silicon (Si)	1.10 eV
Silicon-Carbide (SiC)	3.26 eV
Gallium Nitride (GaN)	3.40 eV

The GaN high-electron-mobility-transistor (HEMT) is field effect transistor, but it behaves differently than the metal-oxide-semiconductor-field-effect transistor (MOSFET). A MOSFET passes charge through a channel of doped regions between source and drain whose channel width is controlled by a gate-to-source voltage. A HEMT has a heterojunction which is a junction between two materials with different bandgaps. At this heterojunction between two different materials in this case AlGaN and GaN, a 2-dimensional electron gas (2-DEG) forms with a channel mobility of reportedly over 1000 cm^2/Vs depending on how the barrier layer is regrown as seen in [70]. To understand how the 2-DEG works at the heterojunction, see Fig. 2.21. When *n*-doped AlGaN (which has a higher Fermi level than GaN) is connected with a layer of GaN after a voltage is applied to the gate, electrons flow from the lower level of AlGaN to the top layer of GaN. Eventually, the 2-DEG growth is completed when the Fermi levels of the two materials are matched.

There are two types of HEMTs. GaN HEMT, a majority carrier device, made its first appearance in the market in "as depletion-mode transistors" [71]. However, a more beneficial type of HEMT is the enhancement mode transistor that does not require a negative bias on the gate to turn it off at converter start-up. The first enhancement-mode HEMT transistors introduced by EPC utilized GaN on Si substrates [69] and are advertised as a replacement for power MOSFETs. One of the other main advantages advertised by EPC is reduced FOM as seen in Figure 2.22 [72].

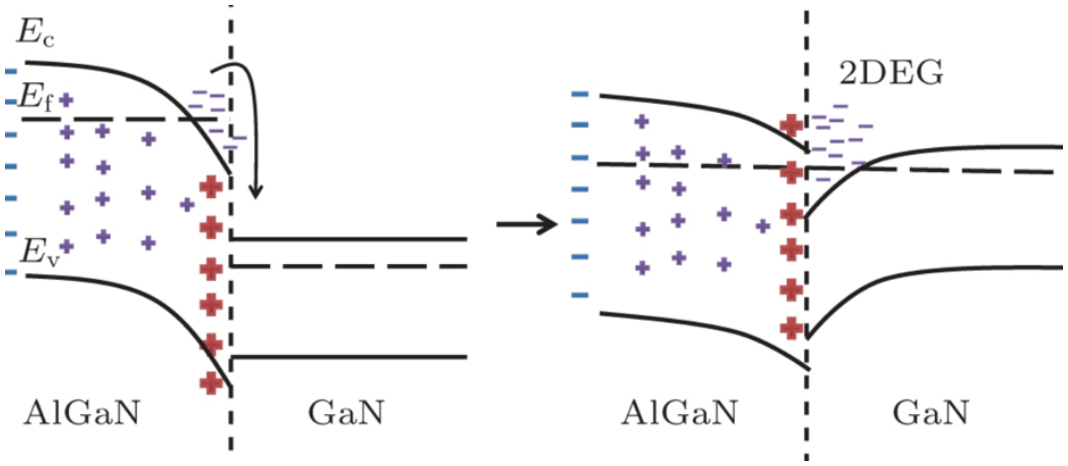

Figure 2.21: Formation of the 2-deminsional electron cloud [70].

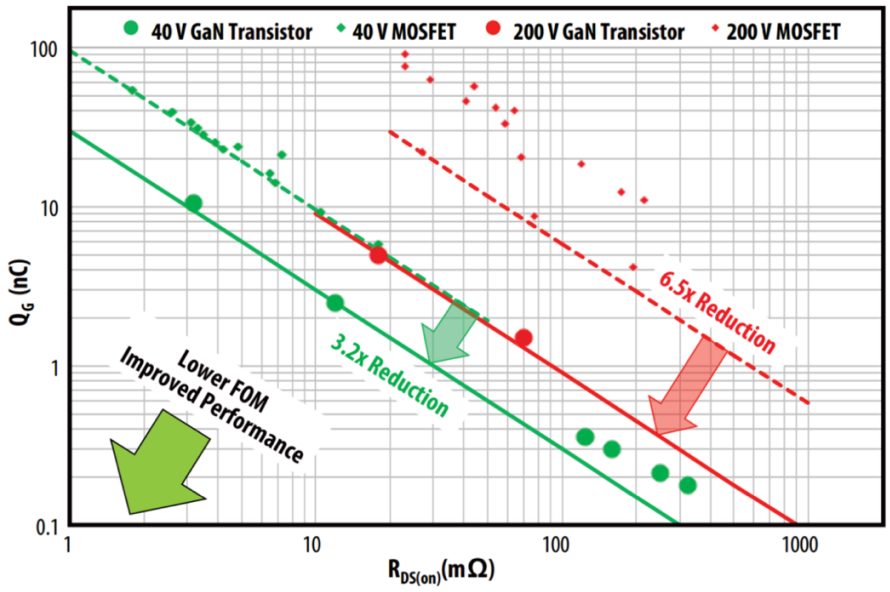

Figure 2.22: FOM Comparison between GaN and conventional Silicon MOSFET [72].

2.6 Summary

Because batteries charge and discharge at different rates, battery balancing prolongs the overall life for a string of batteries in series. To balance series connected batteries, metric estimations using OCV, SOC, and SOH help determine how to employ the proper balancing technique. A good choice to accomplish active balancing is the SCC especially for 2S batteries because only one C_{fly} *ESR* is present. The SCC using standard modulation automatically balances batteries based on the OCV method, but if a SOH sensing mechanism is utilized, the control of the SCC modulation increases the converter's balancing capabilities. Because the SCC consists of a similar structure to a FCMC, a combination of the two possibly both balances and charges 2S batteries simultaneously. This combined converter operation is further explored in Chapter 3.

Chapter 3 Proposed Design

The switched capacitor (SC) buck three-level boost converter proposed for the battery charger is shown in Figure 3.1. The converter combines a switched capacitor active balancing technique with a three-level boost topology for the 2S battery charging applications. The application of this converter is two-fold:

- Charge a 2S battery pack.
- Actively balance the individual battery cells.

Because the SC three-level boost topology uses a similar structure to an SCC that actively balances a string of cells, a combination of the two provides the two-fold application by the addition of only two small transistors. This adds minimum area to the overall circuit and contributes to the goal of reducing the number of ICs needed to implement the entire battery charger system with balancing onto one chip. Because the balance current is sizably less than the charging current, the small (mA-rated) transistors negligibly impact efficiency. Simulations and hardware testing back up this efficiency conclusion. Balancing is performed in SC mode where only balancing occurs, but it is also possible to charge and balance the batteries simultaneously with the proper modulation across a range of voltage inputs. Because only one flying capacitor is necessary to balance a 2S string of cells, conduction loss resulting from the capacitor *ESR* is minimum. As the design indicates, a small flying capacitor is chosen with sufficient voltage rating.

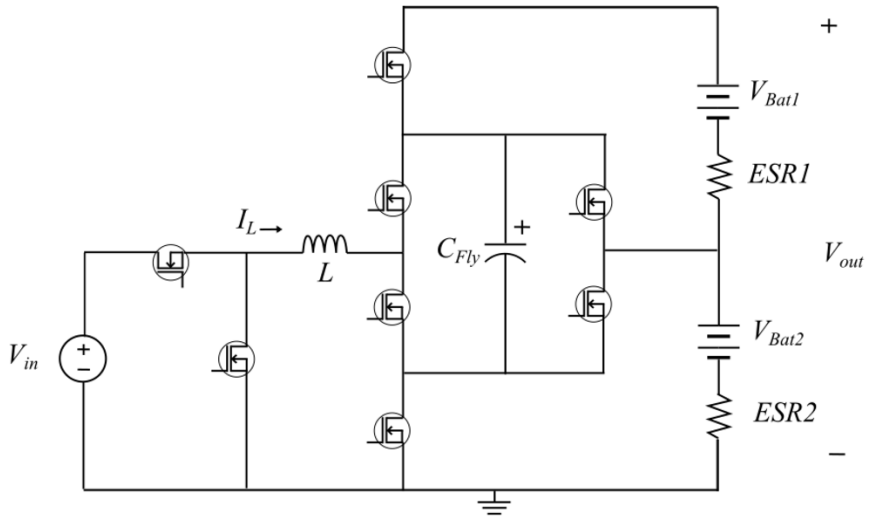

Figure 3.1: Proposed buck three-level boost converter.

After the operation of the SC buck three-level boost is reviewed and the balancing technique investigated, a discrete hardware prototype is developed in Chapter 5 to validate the modeling of the converter. Chapter 6 investigates how to implement the convert on a single IC. Figure 3.1 displays the converter topology addressed in this chapter. The conversion ratio, the ratio of the output to input, in terms of duty cycle for a buck-boost is

$$M(D) = \frac{D_{buck}}{1 - D_{boost}} \tag{3.1}$$

where D_{buck} is the duty cycle for the buck stage and D_{boost} is the duty cycle for the boost stage.

One of the typical voltage inputs to chargers is 5 V, so in a 2S battery pack with two 4.2 V batteries (8.4 V), the charger must have a voltage boosting capability from input to output. This converter uses a three-level boost topology that meets this specification and provides balancing. When V_{in} is greater than V_{out}, the boost stage is optionally utilized to include the battery balancing functionality. As D_{boost} increases when V_{in} is greater than V_{out}, D_{buck} decreases as shown in equation (3.1). Regardless of input, the flying capacitor operates with an average voltage of half the output

with standard modulation. The lower rated voltage devices (as compared to a convention two-level converter) in this design achieve a similar r_{on} as higher voltage rated devices but with less switching loss. The SC buck three-level boost also can decrease the size of magnetics in the converter with smaller ripple characteristics compared to the two-level version.

3.1 Three-Level Boost Converter Operation

The three-level boost converter achieves the same conversion as a two-level structure. The flying capacitor adds an additional energy storage component to the operation. Throughout the switching period, there are intervals where C_{fly} charges when it is in series with the inductor. During another interval, C_{fly} discharges the energy to the output. Figure 3.2 shows the proposed topology for a three-level boost. I_{Bat1} and I_{Bat2} are the charging currents for Battery 1 and 2 respectively.

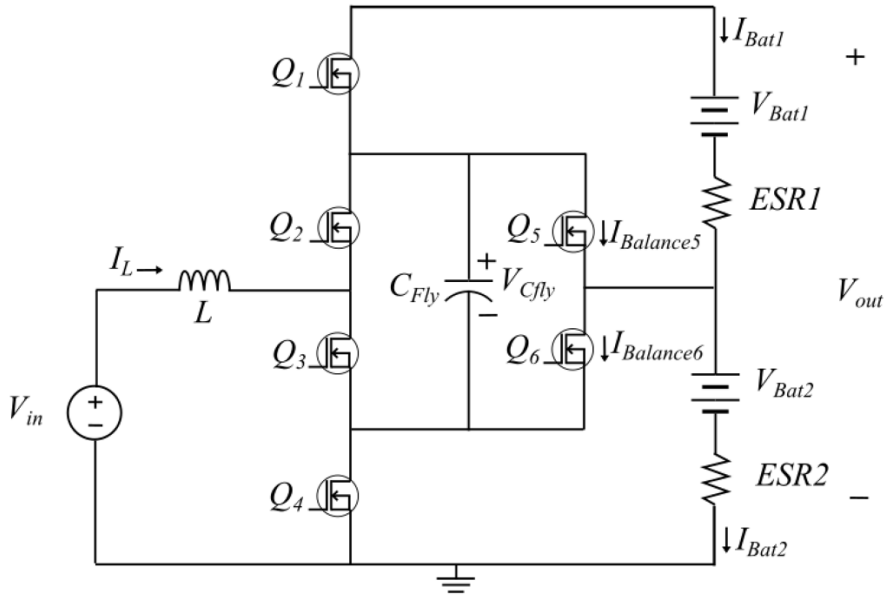

Figure 3.2: Proposed SC three-level boost converter.

3.1.1 Example of SC Three-Level Operation

To provide a demonstration of the converter's ability to boost voltage and provide charging current, an example operating point is specified in Table 3.1. Throughout this example, the buck-stage, high-side transistor conducts for the entire period, so the only switching actions that take place are in the boost stage as seen in Figure 3.3. The notation for naming the transistors in Figure 3.2 is used until otherwise stated. The example also displays the balancing capabilities.

A flying capacitor here is chosen larger than the minimum required based on equation (2.13). A large inductor is selected to make the current ripple negligible for this example. The batteries in 2S configuration each have a nominal voltage of 3.6 V and are charged at 5 A, but V_{bat2} operates with a slightly higher voltage (here it is assumed that Battery 2's SOC is slightly greater). The active balancing behavior utilizes a small negative balance current to discharge the second battery and a small positive current to charge Battery 1 until the batteries reach the same potential. Assuming steady state operation, the output voltage is 7.86 V as the batteries first begin to charge and balance. Battery voltage increases to V_{reg} as the battery is charged.

Table 3.1: Converter Parameters for Example Operating Point

Symbol	Name	Value
L	Inductor	200 μH
C_{fly}	Flying Capacitance	5 μF
C_{out}	Output Capacitance	20 μF
f_s	Switching Frequency	1 MHz
V_{in}	Input Voltage	5 V
V_{out}	Output Voltage	7.86 V
I_{out}	Charging Current	5 A

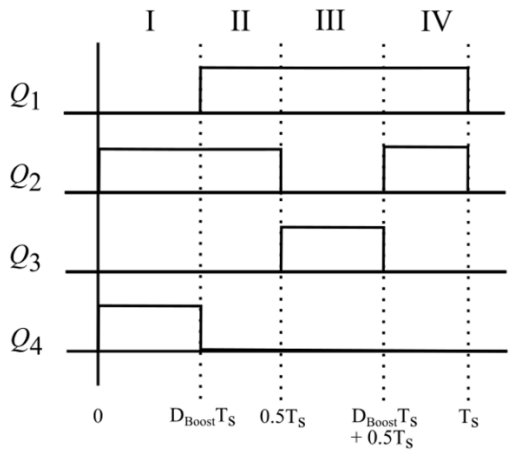

Figure 3.3: Modulation scheme for the three-level boost converter.

Throughout Chapters 3, 4, and 5, GaN transistors are used to implement the switches. Simulations and the discrete hardware prototype utilize low on-resistance EPC2024 devices, so the simulations include the parasitic loss associated with each device. However, the operational efficiency is still high. Chapter 5 provides the background for the choice of this specific GaN HEMT and the optimization that went into the prototype design. The simulations here are to familiarize the reader with the working concepts of the FCMC used in this chapter. The inductor current waveform over one period, T_s, is shown in Figure 3.4. The first noticeable trait is that the inductor current experiences a ripple that operates at twice the switching frequency. This prevents larger ripple and allows designers to use smaller passives than those required for the same application in a two-level configuration. The current ripple here is quite small at less than 2 mA. The average value of the inductor current in Figure 3.4 is as expected for a D_{boost} of 36.4 % and an output current of approximately 5 A using the average model shown in equation (3.2). The average value of the inductor current is

$$I_L = \frac{I_{out}}{(1 - D_{Boost})}. \tag{3.2}$$

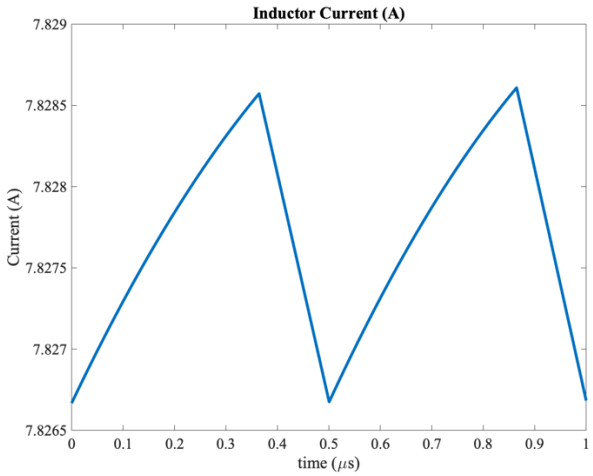

Figure 3.4: Inductor current waveform over one period, T_s.

The voltage on the flying capacitor V_{cfly} and the balance currents for each battery are shown in Figure 3.5. Notice one balance current is negative to discharge Battery Cell 2. The other balance current is positive to charge Battery Cell 1. The output current waveform is shown in Figure 3.6. The flying capacitor experiences a ripple slightly less than 600 mV peak-to-peak. The balance transistors are timed to only turn-on when it is conducive to creating the necessary polarity of balance current for each battery cell. Section 3.2 reviews the modulation of the balancing transistors. When the voltage on V_{cfly} is less than $V_{out}/2$ during the first half of the period, a discharging current flows through Battery Cell 2. When the voltage on V_{cfly} is greater than $V_{out}/2$ during the second half of the period, a charging current flows through Battery Cell 1. On account of the losses in the converter, the output current operates at slightly less than 5 A. The charging current waveform is displayed in Figure 3.6. The balance current and voltage ripple on the output capacitor is why the charging current does not appear constant. V_{cell2} experiences a smaller overall charging current than V_{cell1} to balance the batteries while charging. The equivalent circuits for the four intervals are shown in the following Figure 3.7, 3.8, 3.9, and 3.10 where V_{cell} is assumed to be equal to V_{Bat}. Note the polarity of C_{fly} in intervals I and III. Interval II is the same as IV.

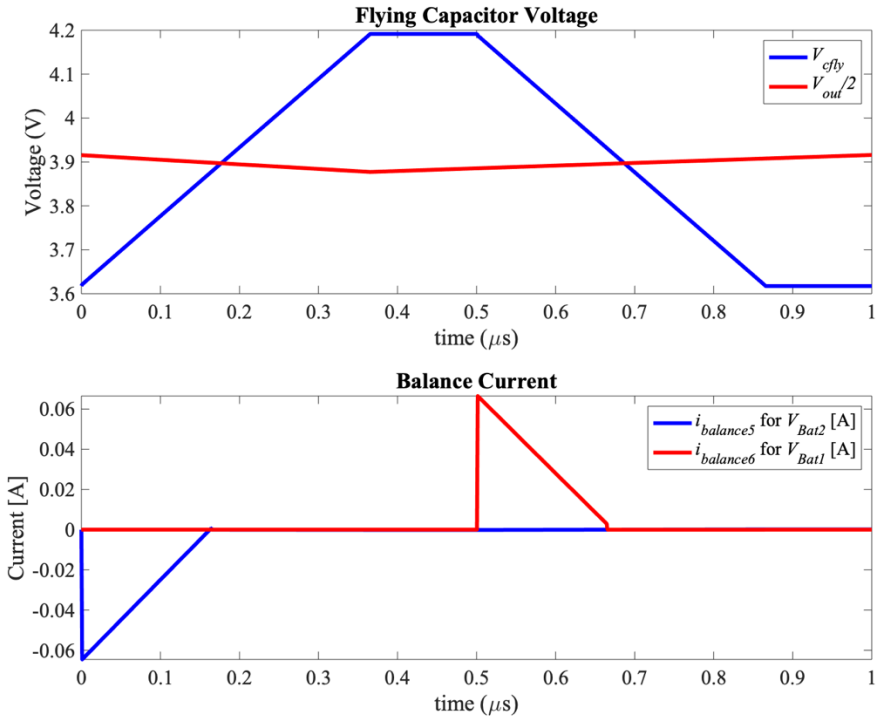

Figure 3.5: Flying capacitor voltage and balance current waveforms.

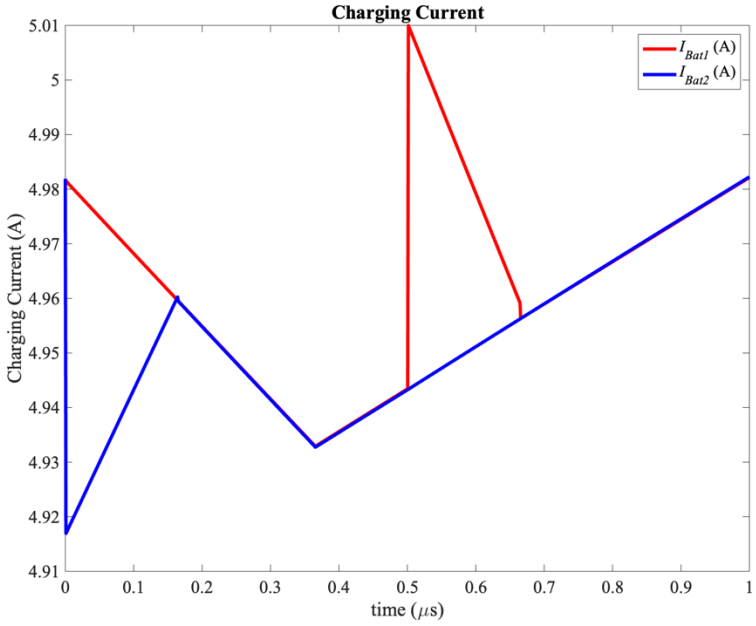

Figure 3.6: Output current through both Battery 1 and Battery 2.

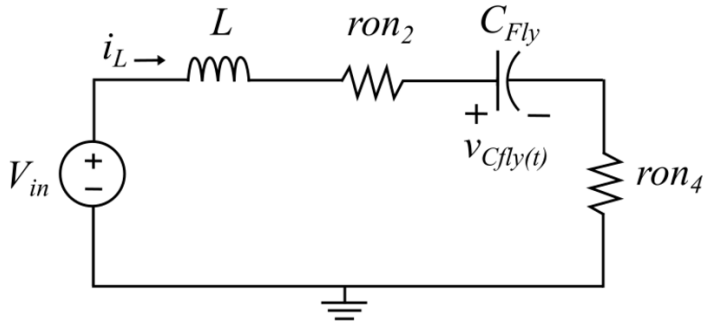

Figure 3.7: Interval I for the three-level boost converter.

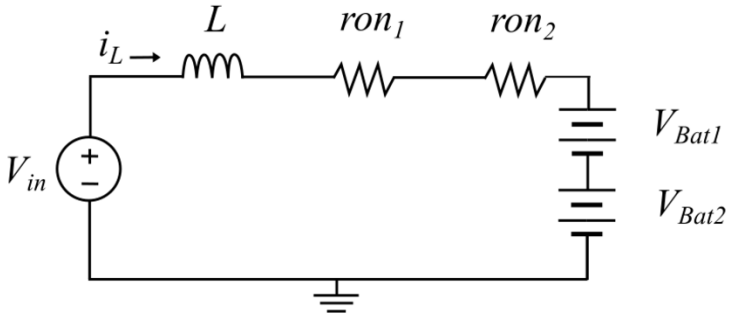

Figure 3.8: Interval II for the three-level boost converter.

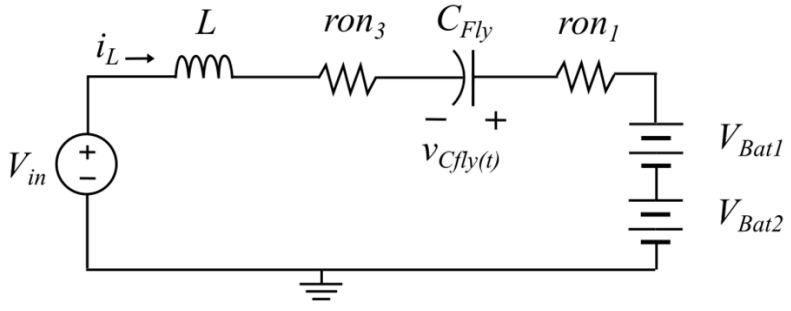

Figure 3.9: Interval III for the three-level boost converter.

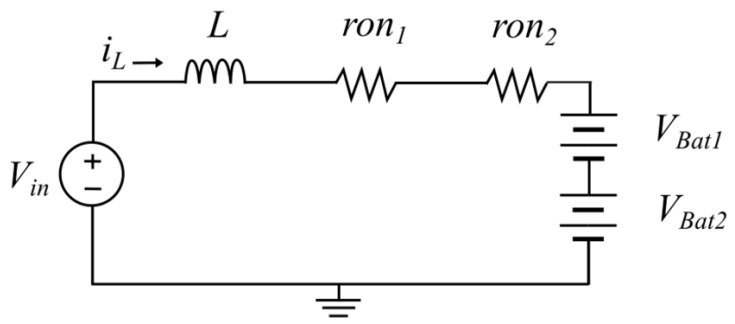

Figure 3.10: Interval IV for the three-level boost converter.

3.2 Balance Current

As previously stated, the battery balancing extends the overall life of the battery pack. As a pack charges and discharges, imbalance in the batteries leads to issues warranting protection methods. The follow section examines how the active balancing scheme in SC three-level boost converter operates.

3.2.1 Voltage Ripple on the Flying Capacitor

The balance current is directly proportional to the voltage ripple, ΔV_{Cfly}, across the flying capacitor. ΔV_{Cfly} is defined as the voltage from the peak to the median voltage,

$$\Delta V_{Cfly} = \frac{I_L}{2 \cdot C_{Fly} \cdot fs} \cdot D_{Boost}. \tag{3.3}$$

The choice of the flying capacitance must consider its effect on the balance current, and it must also exceed the minimum capacitance for the three-level topology solved for in equation 2.13.

3.2.2 Modeling Balancing Current

The total balance current of the converter is the sum of two balancing currents: $I_{Balance5}$ and $I_{Balance6}$. These are the average currents over one period that flow through the balance transistors of Q_5 and Q_6 in the topology in Figure 3.2 respectively. To enable the SCC balancing function, Q_5 is only switched ON during the ON-time of Q_4. Q_6 is only switched ON during the ON -time of Q_1. Therefore, the maximum ON-time for either balance interval is $D_{boost} \cdot T_s$. During $D_{boost} \cdot T_s$, the ripple of V_{cfly} (assuming the average V_{cfly} is $V_{out}/2$) spends approximately half of the time at a voltage more positive than the $V_{out}/2$ and the other half more negative. Here in interval I and III, the flying capacitor is either charged or discharged (depending on the polarity of C_{fly}) as it is connected in series with the inductor. Turning ON either of the balance transistors during these intervals (depending on which of the 2S batteries requires more charging) introduces a balance current to the circuit. If the average of V_{cfly} is balanced to $V_{out}/2$, then both balance transistors are turned ON at different but equally long intervals to contribute to the total balance current. This approach adds two more equivalent circuit intervals. These are denoted I-B and III-B. For the following two figures, $V_{Bat2} > V_{Bat1}$. For each balancing interval, consider the voltages across the flying capacitor and that of the batteries. It is desired for the balance current to discharge Battery 2. When $v_{cfly}(t)$ is less than the V_{bat2}, turning Q_5 ON during this time allows the balance current $I_{Balance5}$ to flow from Battery 2 and charge the flying capacitor based on the potential difference between the two where

$$i_{balance5}(t) = \frac{v_{Cfly(t)} - V_{Bat2} - i_{Cfly}(t) \cdot r_{on4}}{r_{on5}}. \tag{3.4}$$

Figure 3.11 depicts interval I-B.

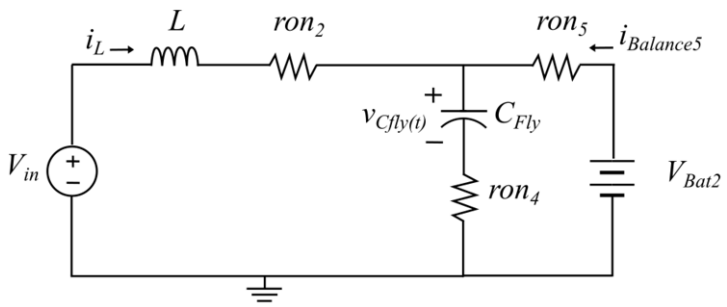

Figure 3.11: Balance interval I-B.

If the on-resistances of the power stage transistors are small, the voltage drop across the transistor is approximated to be negligible and the balance current then only depends on the balance resistance, the battery voltage, and $v_{cfly}(t)$. In interval III-B (Figure 3.12), positive balance current is needed to charge Battery 1. When $v_{cfly}(t)$ is greater than the V_{bat1}, turning Q_6 ON during this time generates a balance current $I_{Balance6}$ where

$$i_{balance6}(t) = \frac{v_{Cfly(t)} - V_{Bat2} - i_{Cfly}(t) \cdot r_{on1}}{r_{on6}}. \tag{3.5}$$

This potential difference between $v_{cfly}(t)$ and V_{Bat1} generates balance current through r_{on6} to increase the charging of Battery 1.

The larger the flying capacitor voltage ripple, the larger the difference in voltage between the battery and the flying capacitor which leads to more balancing current. The maximum flying capacitor voltage is

$$V_{Cfly,max} = \frac{V_{out}}{2} + \Delta V_{Cfly}, \tag{3.6}$$

And the maximum ripple is limited to

$$\Delta V_{Cfly} \leq V_{bat,min}. \tag{3.7}$$

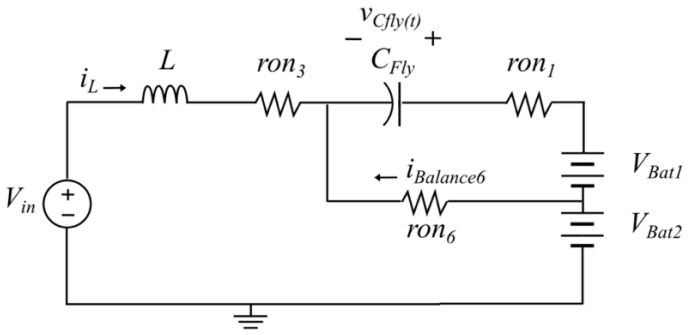

Figure 3.12: Balance interval III-B.

V_{outmax}, the voltage at max cell voltage, is derived knowing the highest possible output current. When the input voltage V_{in} is set to 5 V, the highest D_{boost} required occurs if both batteries are approximately charged to full voltage. The maximum output voltage V_{outmax} is

$$V_{outmax} = (4.2 + ESR1 \cdot I_{out}) + (4.2 + ESR2 \cdot I_{out}). \tag{3.8}$$

The minimum output voltage further restricts the maximum flying capacitor ripple. The flying capacitor voltage cannot swing negative as shown in equation (3.7), so the minimum nominal voltage of a battery determines the maximum flying capacitor voltage ripple that the system operates. The maximum possible ripple sets a boundary in the selection of C_{fly}. Balance resistance needs to be designed to be sufficiently large to keep the balance current small, so the conduction loss across the balance transistors' on-resistance negligibly impacts power efficiency.

3.2.3 Inductor Current Ripple

The current ripple of a three-level converter is simplified in Figure 3.13 over a half period followed by the equations for the inductor current ripple during interval I where

$$\Delta i_L = \frac{V_{in} - V_{cfly}(t)}{2L} \cdot D_{boost} T_s. \tag{3.9}$$

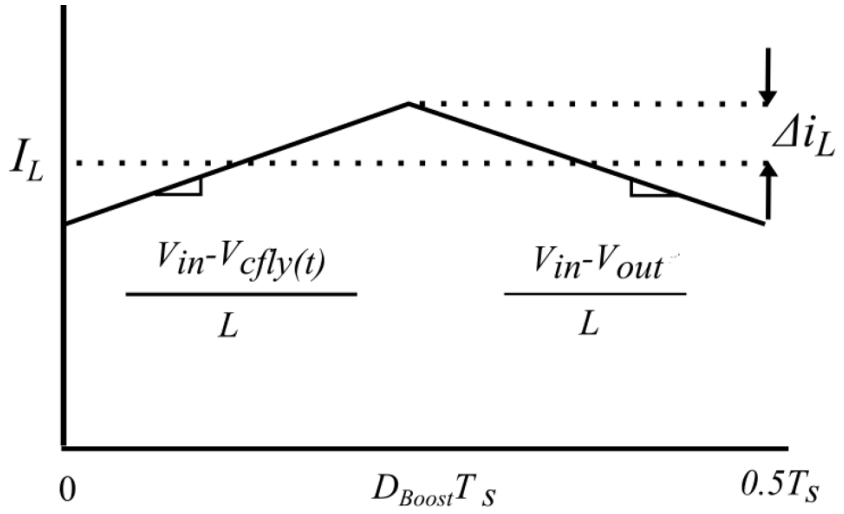

Figure 3.13: Inductor current ripple over a half-period.

The inductor current ripple during interval II is

$$\Delta i_L = \frac{V_{in} - V_{out}}{2L} \cdot (0.5 - D_{boost})T_s. \tag{3.10}$$

This behavior continues in the second half of the period as interval II has the same equivalent circuit as IV. If smaller passives are used, there exists resonant behavior of the inductor and flying capacitor in series during intervals I and III. Equation (3.9) is no longer useful because it assumes a constant inductor slope. Equation (3.10) can still be used because here the flying capacitor is not present in the sub-circuit. However, the current ripple (and therefore the I_{Lrms}) may be larger than equation (3.9) indicates if a resonant peak occurs and then falls before the conclusions of intervals I and III. Figure 5.17 has an example of this current behavior.

3.2.4 Effect of Current Ripple on Flying Capacitor Voltage

As current ripple increases, the efficiency of the converter decreases because of conduction losses. Furthermore, the inductor current ripple also has an effect on the average of V_{cfly}. As expressed in equation (3.4) and (3.5), the balance current of the converter depends on flying capacitor voltage and its ripple. To incorporate the balancing behavior described in Section 3.2.2, it is necessary that the average of V_{cfly} is approximately equal to $V_{out}/2$. Using the same operating parameters as the example in Section 3.1.1, the plot in Figure 3.14 shows how the current ripple affects the voltage differential between the V_{cfly} and $V_{out}/2$. The circuit in Figure 3.14 has buck switching transition in the first half-period (but not in the second half-period) which causes the voltage differential (discussed in Section 5.3). As ripple increases, there is a larger rms current where increases any disparity between the charging and discharging inductor current interval slopes (yielding a larger voltage differential) (Section 3.2.5). A larger inductance (yielding smaller rms currents) reduces the effect of any disparity. Other possible sources of voltage differential in fabricated circuits seen in [73] and [74] are attributed to inevitable slight variations in transistor parasitics, duty cycles, and other circuit parasitics natural to any PCB or IC like metal routing or copper traces.

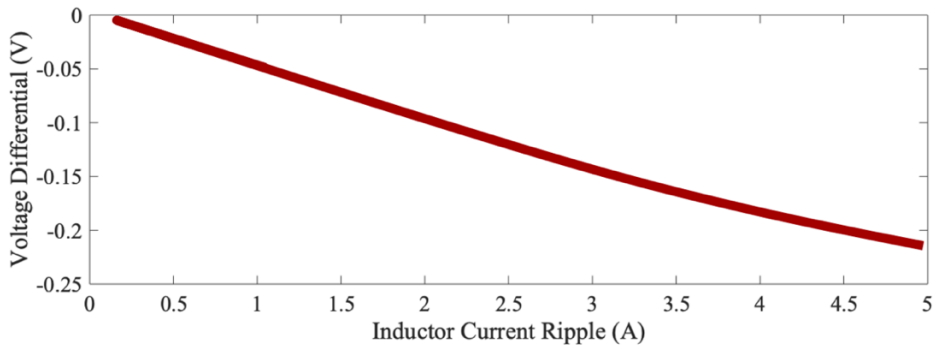

Figure 3.14: Voltage differential ($V_{cfly} - V_{out}/2$) vs. the inductor current ripple.

3.2.5 V_{cfly} Regulation Via Current Programed Mode

Instead of operating with a large inductor, a more practical solution is to apply current control to ensure the current falls and rises at equal magnitudes; this allows the flying capacitor to charge and discharge equally. One of the ways converters implement current control is through current programed mode (CPM) [27]. As discussed in [75] and [76] for a three-level buck converter, the control of the inductor current balances the flying capacitor voltage and further regulates the output. Peak offsetting mechanism (POM) [76] is utilized in these two sources to accomplish this feat. Through this additional regulation, V_{cfly} is adjusted as needed. POM makes use of two different reference currents, one for each peak that the inductor current reaches during each half period. Using the modulation in Figure 3.3, the inductor current rises with slopes m_1 and m_3 and falls with slopes m_2 and m_4 using the same operating parameters in Table 3.1. The slopes are

$$m_1 = \frac{V_{in} - V_{cfly}}{L}, \tag{3.11}$$

$$m_2 = m_4 = \frac{V_{in} - V_{out}}{L}, \tag{3.12}$$

and

$$m_3 = \frac{V_{in} - (V_{out} - V_{cfly})}{L}. \tag{3.13}$$

A disturbance to the flying capacitor voltage waveform creates a variation in slopes m_1

$$m_1 = \frac{V_{in} - (V_{cfly} + V_{cflydif})}{L}, \tag{3.14}$$

and m_3

$$m_3 = \frac{V_{in} - (V_{out} + (V_{cfly} + V_{cflydif})}{L}. \tag{3.15}$$

$V_{cflydif}$ is the difference in average voltage from $V_{out}/2$ by

$$V_{cflydif} = V_{cfly} - \frac{V_{out}}{2}. \tag{3.15}$$

An example operating point of the SC three-level boost charging 2S batteries where V_{in} = 5 V and f_s = 700 kHz is shown in Figure 3.15. Here the slope m_1 is greater than m_3. Because slopes m_2 and m_4 remain unchanged, the current no longer raises from its peak and falls to its floor during a half-period. This leads to unequal charging and discharging of C_{fly} and lowers V_{cfly} below the output of $V_{out}/2$.

By sensing the flying capacitor voltage and comparing it with the expected dc output of $V_{out}/2$, the magnitude of ΔV_{cfly} is determined. Because this adjusts the inductor current states throughout the period, and the slopes change according to ΔV_{cfly}, the ΔV_{cfly} difference is used to create two new reference current values, I_{ref1} and I_{ref2}. The new reference currents are calculated below where I_{ref1} is the peak for the shut-off of Q_4 and I_{ref2} is the peak for the shut-off of Q_3. The work in [76] details a clear example of these reference (or command) currents that are used to control the inductor current for a three-level buck, and the reference currents are

$$I_{ref1} = I_{ref} - \Delta I_{ref}, \tag{3.16}$$

and

$$I_{ref2} = I_{ref} + \Delta I_{ref}. \tag{3.17}$$

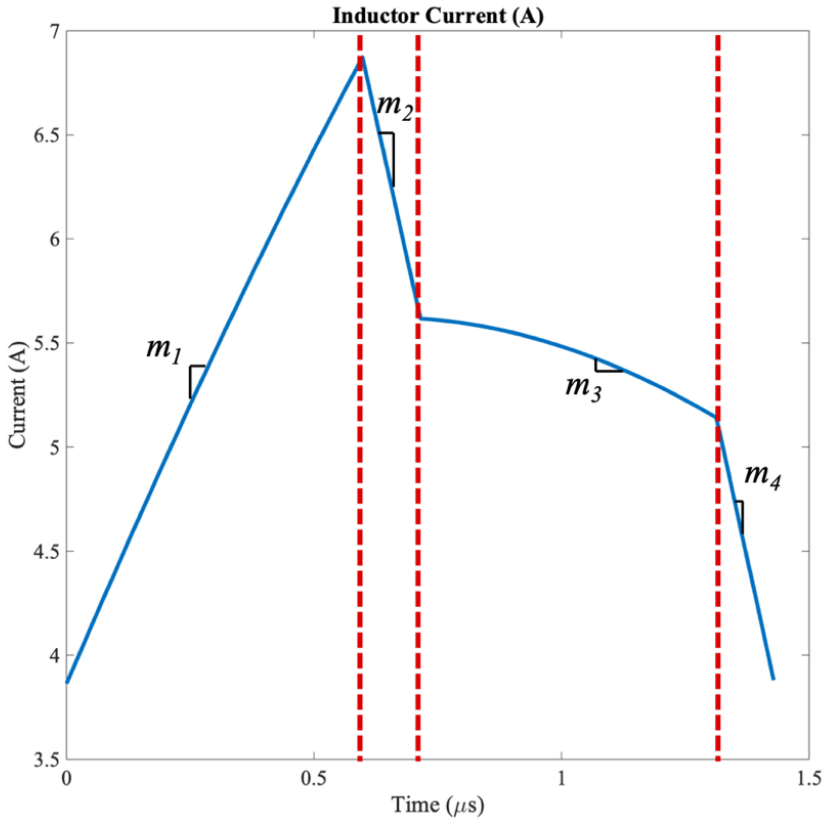

Figure 3.15: Unequal inductor current slopes through a single switching period.

Peak offsetting mechanism (POM) [76] is a possible solution to the control problem of maintaining V_{cfly} closer to $V_{out}/2$. While the proper control circuitry is not designed in this paper, the modulation is adjusted manually based on simulation and the slopes of the inductor current to push V_{cfly} to its expected dc value. While control provides benefits to converter operation, the focus of this design is on the balancing and charging operation and how to integrate the two. Other modulation solutions shown in Section 5.3 further reduce the disturbances in inductor current that bring V_{cfly} closer to $V_{out}/2$ and provide a solution to improve the current waveform (adjusting the slopes of m_1 and m_3 to be equal in magnitude) in Figure 3.15.

3.2.6 Modeling the Time Required for Battery Balancing

The charging time for the two batteries to charge to V_{reg} is

$$t_{charge} = \frac{(Q_{max} - Q_{max} \cdot SOC)}{I_{out} \cdot \eta}. \tag{3.18}$$

This is compared to the balance time. Ideally, the balance time would remain shorter than the average charging time, t_{charge}, for either battery to ensure batteries are always sufficiently balanced. The balance time, $t_{balance}$ for cases of $SOC_1 < SOC_2$ is

$$t_{balance} = \frac{(Q_{max} \cdot SOC_1 - Q_{max} \cdot SOC_2)}{I_{balance}}, \tag{3.19}$$

where $I_{balance}$ is the total balance current of the system (the total of $I_{balance5}$ and $I_{balance6}$ using the polarity reference of Figure 3.2). When $SOC_2 > SOC_1$,

$$t_{balance} = \frac{\left(Q_{max} \cdot SOC_1 - Q_{max} \cdot SOC_2\right)}{I_{balance}}. \tag{3.20}$$

Section 6.1.4 utilizes these equations for evaluation of balance current performance using an example Q_{max}, the maximum capacity of a battery.

Chapter 4 Power Loss Modeling

To further evaluate the loss models of the three-level boost converter, the following converter and transistor notation is referenced as relative to Figure 4.1.

4.1.1 Three-Level Boost Conduction Loss

One of the dominant sources of loss for the high-current battery charger using the three-level boost topology is conduction loss (assuming f_s is not too high). In each of the following equations, the power loss is calculated using the rms inductor current:

$$I_{L,rms} = I_L \sqrt{\left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)}. \tag{4.1}$$

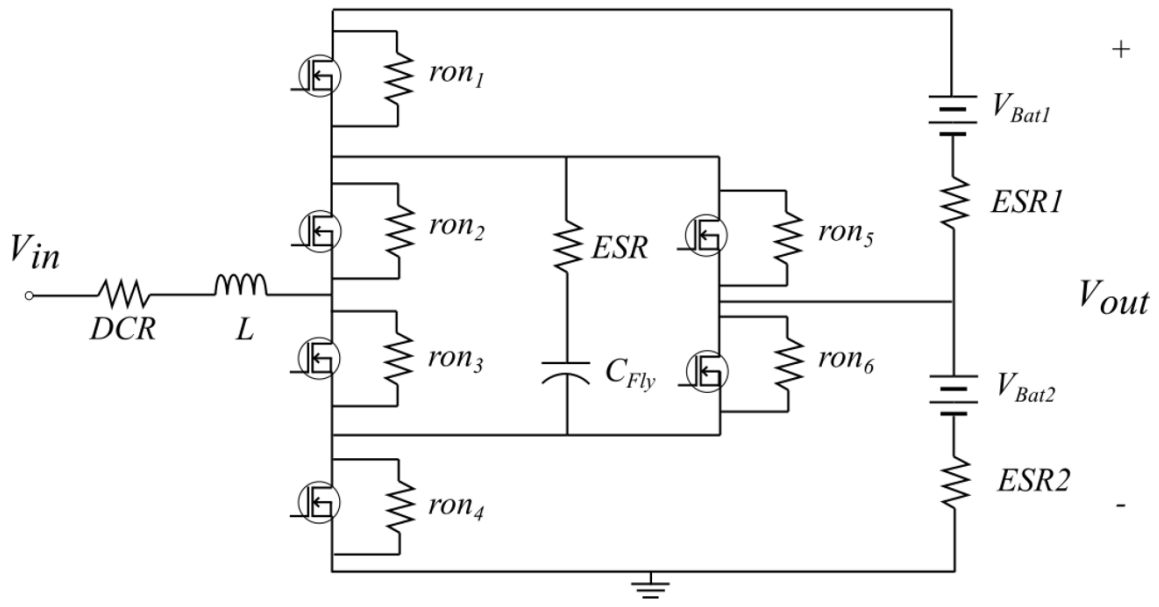

Figure 4.1: Parasitic resistances of the three-level boost converter with balancing FETs.

I_{Lrms} is also dependent on the frequency component of the inductor current ripple. This is another reason the current ripple Δi_L of the converter is a significant parameter in terms of loss. Conduction loss for the on resistance, of Q_1, Q_2, Q_3, and Q_4 are

$$P_{cond1} = I_L^2(1 - D_{boost})\left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) r_{on1}, \tag{4.1}$$

$$P_{cond2} = I_L^2(1 - D_{boost})\left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) r_{on2}, \tag{4.3}$$

$$P_{cond3} = I_L^2(D_{boost})\left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) r_{on3}, \tag{4.4}$$

and

$$P_{cond4} = I_L^2(D_{boost})\left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) r_{on4}. \tag{4.5}$$

The conduction loss through the balance resistors is small compared to the power loss in the power FETs because the balance current is negligible compared to the charging current. The conduction loss due to the on-resistance of these balancing FETs is

$$P_{cond5} = \left(\frac{V_{Cfly}(t) - V_{bat(t)}}{r_{on5}}\right)^2 \left(\frac{t_{on5}}{T_s}\right) r_{on5}, \tag{4.6}$$

and

$$P_{cond6} = \left(\frac{V_{Cfly}(t) - V_{bat(t)}}{r_{on6}}\right)^2 \left(\frac{t_{on6}}{T_s}\right) r_{on5}. \tag{4.7}$$

Though the input current of the converter is limited to 3A, the inductor current increases significantly at high D_{boost} where conduction loss dominates. A large contributor to this overall system loss is the conduction through DC resistance (DCR) of the inductor, but because the

inductor is external to the chip, the loss does not count towards the on-chip loss. The conduction loss through the inductor DCR is

$$P_{condL} = I_L^2 \left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) DCR. \tag{4.8}$$

The conduction loss through the *ESR* of the flying capacitor is

$$P_{CflyESR} = 2I_L^2(1 - D_{boost}) \left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) ESR. \tag{4.9}$$

4.1.2 Three-Level Boost Switching Loss

One of the contributors to the switching loss is the output capacitance of each power transistor during the turn off of Q_3 and Q_4. For all switching actions, there remains one switch that continues conducting while the others remain off. This transistor's V_{ds} clamps to the voltage of the flying capacitor, approximately $V_{out}/2$. Though the following equations simplify if each drain to source capacitance is equivalent, the LDMOS devices used in this charger are designed to take up a different area distribution leading to different output capacitances, so it is important to consider this in the power loss calculations described below for C_{oss} loss where

$$P_{oss3} = \frac{1}{2} \cdot \left(C_{eq3,E} + 2C_{eq2,Q} - C_{eq2,E}\right) \left(\frac{V_{out}}{2}\right)^2 f_s, \tag{4.10}$$

and

$$P_{oss4} = \frac{1}{2} \cdot \left(C_{eq4,E} + 2C_{eq1,Q} - C_{eq1,E}\right) \left(\frac{V_{out}}{2}\right)^2 f_s. \tag{4.11}$$

The following figures further examine the C_{oss} power loss by providing the equivalent circuits during the transitions where the loss takes place.

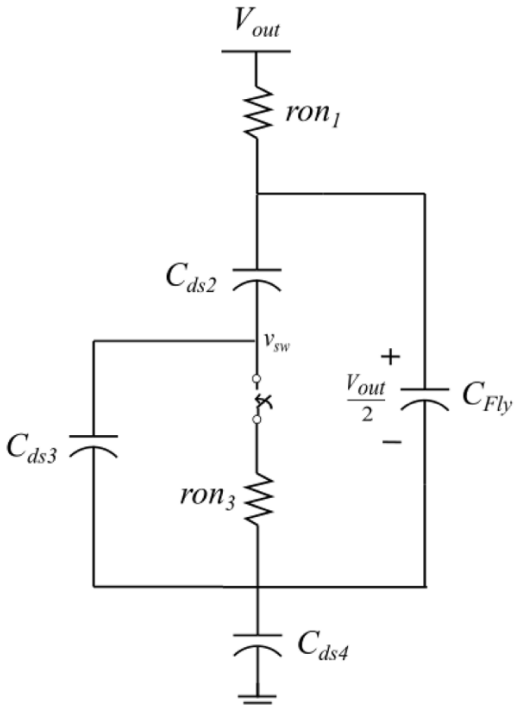

Figure 4.2: C_{oss} loss for Q_3 turn-on when $D_{boost} < 50\ \%$.

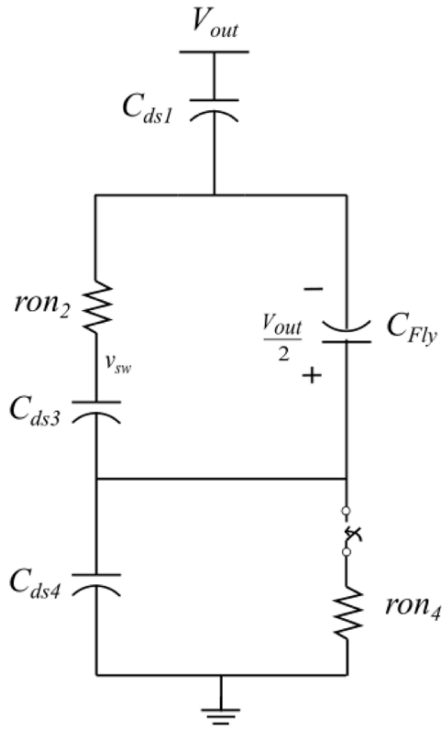

Figure 4.3: C_{oss} loss for Q_4 turn-on when $D_{boost} < 50\ \%$.

The overlap losses occur during the turn-on and turn-off transitions of transistors Q_3 and Q_4. The higher the gate drive current capability, the faster the gate capacitance charges and discharges. The overlap power losses are

$$P_{overlap3} = \frac{1}{4} V_{out} I_L \, t_{ov} f_s, \tag{4.12}$$

and

$$P_{overlap4} = \frac{1}{4} V_{out} I_L \, t_{ov} f_s. \tag{4.13}$$

The overlap time, t_{ov}, is also displayed below as

$$t_{ov} = Q_{sw} \left(\frac{1}{I_{g,on}} + \frac{1}{I_{g,off}} \right). \tag{4.14}$$

where I_g,*on* is the gate current during a transistor's turn-on transition and I_g,*off* is the gate current for the turn-off transition. The equations that determine the gate drive current are shown below, where V_m is the voltage in Figure 2.19. Drive current is dependent on the gate resistance $R_{g,on}$ in the path during turn-on and $R_{g,off}$ during turn-off where

$$I_{g,on} = \frac{V_{dr} - V_m}{R_{g,on}}, \tag{4.15}$$

and

$$I_{g,off} = \frac{V_m}{R_{g,off}} . \tag{4.16}$$

Gate charge loss occurs for every gate included in a circuit, and each gate's respective drive voltage and gate charge is utilized. The gate drive loss for the balance transistors should be small since they take up small area compared to the power transistors. The power loss resulting from the gate charge is

$$P_{gate} = V_{dr} Q_g f_s . \tag{4.17}$$

If dead times are used in converter operation, there is body diode conduction of the inductor current during each dead time interval, t_{dt}. V_f is the forward voltage of the device. Table 4.1 summarizes the losses. Body diode conduction is

$$P_{bd} = V_f I_L t_{dt} f_s \,. \tag{4.18}$$

Table 4.1: Loss Equations for a Three-Level Boost Converter

Symbol	Type of Loss	Loss Equation
P_{cond1}	Q_1 Conduction Loss	$I_L^2(1-D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on1}$
P_{cond2}	Q_2 Conduction Loss	$I_L^2(1-D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on2}$
P_{cond3}	Q_3 Conduction Loss	$I_L^2(D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on3}$
P_{cond4}	Q_4 Conduction Loss	$I_L^2(D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on4}$
P_{cond5}	Q_5 Conduction Loss	$(i_{balance5})^2\left(\frac{t_{on5}}{T_s}\right)r_{on5}$
P_{cond6}	Q_6 Conduction Loss	$(i_{balance6})^2\left(\frac{t_{on6}}{T_s}\right)r_{on6}$
P_{ov}	Overlap Loss	$\frac{1}{4}V_{out}I_L\,Q_{sw}\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
P_{Coss3}	C_{oss3} Loss	$\frac{1}{2}\left(C_{eq3,E}+2C_{eq2,Q}-C_{eq2,E}\right)\left(\frac{V_{out}}{2}\right)^2 f_s$
P_{Coss4}	C_{oss4} Loss	$\frac{1}{2}\left(C_{eq4,E}+2C_{e1,Q}-C_{eq1,E}\right)\left(\frac{V_{out}}{2}\right)^2 f_s$
P_{bd}	Body Diode Loss	$4V_f I_L t_{dt} f_s$
P_{gate}	Gate Loss	$6V_{dr}Q_g f_s$

4.1.3 Buck Stage Loss

A two-level buck stage is added with transistors Q_A and Q_B. The equations in Table 4.2 are included in the analytical models to verify simulation and hardware test results. These losses are for the two-level buck stage at the input of the battery charger. If the modulation in Figure 4.4 is used, the power loss equations related to switching are doubled. P_{CossA} happens during the turn-on of Q_A, and overlap loss occurs at the turn-on and turn-off transition of Q_B. Table 4.2 shows the power loss equations for the two-level buck stage.

Table 4.2: Two-Level Buck Stage Power Loss Equations

Symbol	Type of Loss	Loss Equation
P_{condA}	Q_A Conduction Loss	$I_L^2(D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{onA}$
P_{condB}	Q_B Conduction Loss	$I_L^2(1-D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{onB}$
P_{ov}	Overlap Loss	$\frac{1}{2}V_{in}I_L\ Q_{sw}\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
P_{CossA}	C_{ossA} Loss	$\frac{1}{2}*\left(C_{eqA,E}+2C_{eqB,Q}-C_{eqB,E}\right)(V_{in})^2 f_s$
P_{bd}	Body Diode Loss	$2V_f I_L t_{dt} f_s$
P_{gate}	Gate Loss	$2V_{dr}Q_g f_s$

4.1.4 Complete Loss Model for the Buck Three-Level Boost Converter

Table 4.3 shows the power loss equations for the two-level buck stage combined with the three-level boost. These equations are used to model the prototype built and tested in Chapter 5. The complete schematic for the SC buck three-level boost is shown in Figure 4.5. It includes balance resistors $r_{balance5}$ and $r_{balance6}$ placed in series with the balance transistors to add more resistance in the balancing path. Resistors are changed on the prototype to adjust balance current if needed. The added resistance keeps the balance current much smaller than the charging current to keep the conduction loss on the balancing transistors negligible. The balance transistors Q_5 and Q_6 have ON-times of t_{on5} and t_{on6} respectively.

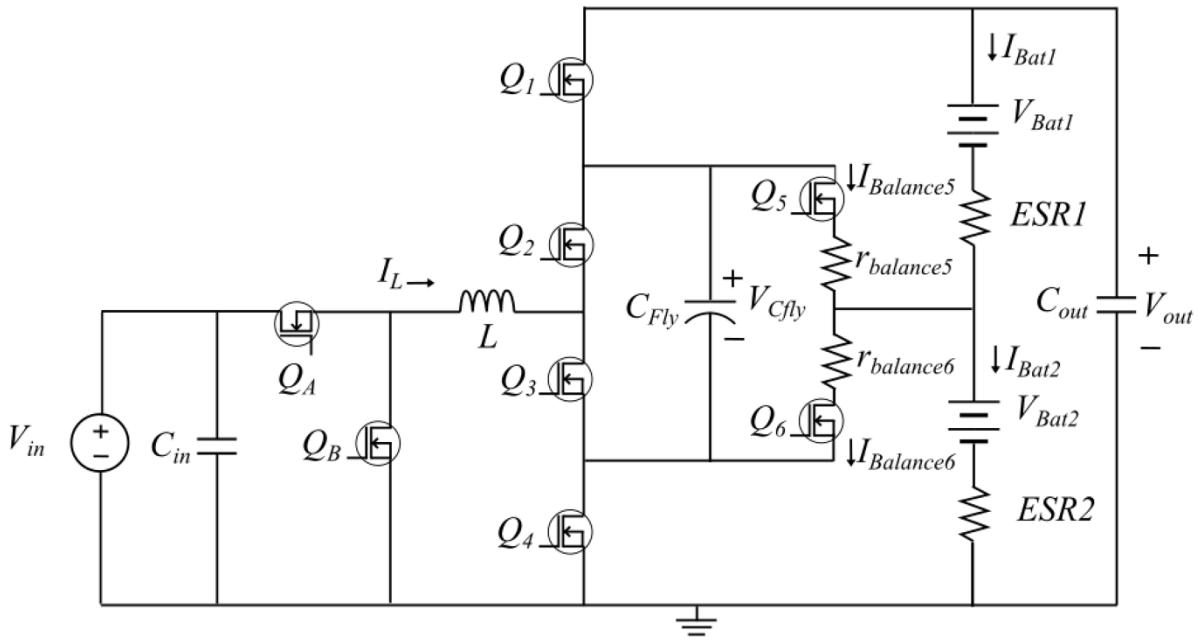

Figure 4.4: Prototype schematic of proposed SC buck three-level boost (Chapter 5).

Table 4.3: Complete Loss Model for the Proposed SC Buck Three-Level Boost Converter

Symbol	Type of Loss	Loss Equation
P_{condA}	Q_A Conduction Loss	$I_L^2(D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{onA}$
P_{condB}	Q_B Conduction Loss	$I_L^2(1-D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{onB}$
P_{cond1}	Q_1 Conduction Loss	$I_L^2(1-D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on1}$
P_{cond2}	Q_2 Conduction Loss	$I_L^2(1-D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on2}$
P_{cond3}	Q_3 Conduction Loss	$I_L^2(D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on3}$
P_{cond4}	Q_4 Conduction Loss	$I_L^2(D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)r_{on4}$
P_{cond5}	Q_5 Conduction Loss	$(i_{balance7})^2\left(\frac{t_{on5}}{T_s}\right)(r_{on5}+r_{balance5})$
P_{cond6}	Q_6 Conduction Loss	$(i_{balance8})^2\left(\frac{t_{on6}}{T_s}\right)(r_{on6}+r_{balance6})$
$P_{ov,buck}$	Overlap Loss	$\frac{1}{2}V_{in}I_L\,Q_{sw}\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
$P_{ov,boost}$	Overlap Loss	$\frac{1}{4}V_{out}I_L\,Q_{sw}\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
P_{CossA}	C_{ossA} Loss	$\frac{1}{2}*\left(C_{eqA,E}+2C_{eqB,Q}-C_{eqB,E}\right)(V_{in})^2 f_s$
P_{Coss3}	C_{oss3} Loss	$\frac{1}{2}\left(C_{eq3,E}+2C_{eq2,Q}-C_{eq2,E}\right)\left(\frac{V_{out}}{2}\right)^2 f_s$
P_{Coss4}	C_{oss4} Loss	$\frac{1}{2}\left(C_{eq4,E}+2C_{e1,Q}-C_{eq1,E}\right)\left(\frac{V_{out}}{2}\right)^2 f_s$
P_{bd}	Body Diode Loss	$6V_f I_L t_{dt} f_s$
P_{gate}	Gate Loss	$8V_{dr}Q_g f_s$

4.2 Discrete Time Loss Modeling

The previous loss model described in Section 4.1 incorporates average modeling to predict how parasitics of the components affect converter performance. To model the complete behavior of the battery charger, discrete time modeling, a technique that "aims at describing the dynamics of the sampled waveforms with no averaging step involved in the process" as defined in [77], is also used to model the converter. While average modeling is simpler mathematically, often important converter dynamics are lost in the resulting loss models. Instantaneous values of the inductor currents and capacitor voltages vary from the averaged magnitude. Solutions through discrete time modeling involve complicated mathematical representations and differential equations, so computational tools such as MATLAB and PLECS, a simulation platform for power electronics, are needed.

Once a circuit is drawn using available components in PLECS, MATLAB assigns the values for each of the components in PLECS (as coded by the user) and incorporates the specified switching modulation input, so a state space representation of the converter is extracted. This representation provides a complete set of information describing the converter system in steady state. The steady-state solution is solved directly which is a major advantage compared to other simulation software like LTspice that has lengthy simulation times because start-up transients force the converter through many cycles before steady state operation is reached [78]. The initial state can be checked for matching with the final state for each inductor current and each capacitor voltage to ensure steady state operation is reached.

State space analysis incorporates an assumption that each interval of a switching circuit can be represented as a linear circuit. The state space representation is

$$\dot{x}(t) = A_i x(t) + B_i u(t), \tag{4.19}$$

and

$$y(t) = C_i x(t) + D_i u(t), \tag{4.20}$$

where x is the state vector made of n_s converter states and u is the input vector with n_i inputs to the system. The topology-dependent matrices $A_i \in \mathbb{R}^{ns \times ns}$ and $B_i \in \mathbb{R}^{ns \times ni}$ are able to describe the converter structure. There are i intervals of the switching converter each made of an equivalent sub-circuit. Each of these intervals has a solution of

$$x(t) = e^{A_i t} x(0) + \int_0^t e^{A_i (t-\tau)} B_i u(\tau) d\tau \tag{4.21}$$

that can further described below if $u(t)$ remains constant throughout a switching interval:

$$x(t) = e^{A_i t} x(0) + A_i^{-1} [e^{A_i t} - I] B_i u_i \tag{4.22}$$

Over a single period T_s, the steady state solution X_{ss} of the system with k switching circuits is

$$X_{ss} = (I - \prod_{i=k}^{1} e^{A_i t_i})^{-1} \cdot \sum_{i=1}^{k} \left(\prod_{j=k}^{i+1} e^{A_j t_j} \right) A_i^{-1} (e^{A_i t_i} - I]) B_i u_i \,. \tag{4.23}$$

The large signal discrete-time model of a converter is shown in the function of equation (4.24). It contains the states $x[k]$, the inputs $u[k]$, the variable(s) that are controlled $c[k]$, and auxiliary variables $w[k]$. The variable k represents the samples, and the model is

$$x[k+1] = f(x[k], u[k], c[k], w[k]). \tag{4.24}$$

The large signal model linear model where Φ is the constant representing the natural response is

$$x[k+1] = \Phi \mathrm{x[k]} + \psi u[k]. \tag{4.25}$$

The small-signal where Γ is the constant representing the forced response of the converter is

$$\hat{x}[k+1] = \Phi\hat{x}[\mathrm{k}] + \psi\hat{u}[k] + \Gamma\hat{c}[k]. \tag{4.26}$$

The $c[k]$ and $w[k]$ allow the incorporation of a constraint equation to overcome a nonlinearity that inhibits proper converter modeling. The constraint equation is

$$0 = \sigma(x[k], u[k], c[k], w[k]))\,. \tag{4.27}$$

Partial derivatives are calculated to resolve for the natural and forced responses of the system that avoid issues due to nonlinearity and lead to

$$\hat{x}[k+1] = \left(\frac{\partial f}{\partial x} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial x}\right)\hat{x}[k] + \left(\frac{\partial f}{\partial u} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial u}\right)\hat{u}[k] + \left(\frac{\partial f}{\partial c} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial c}\right)\hat{c}[k]. \tag{4.28}$$

This leads to the equivalent constants Φ_{eq} and Γ_{eq} which are calculated from the equations the following equations where

$$\Phi_{eq} = \left(\frac{\partial f}{\partial x} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial x}\right), \tag{4.29}$$

and

$$\Gamma_{eq} = \left(\frac{\partial f}{\partial d} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial u}\right). \tag{4.30}$$

The large-signal model derived from discrete time modeling used to evaluate converter design. This methodology is exercised for a complete characterization of every inductor current and capacitor state in the SC buck three-level boost. The states include the equivalent drain-to-source capacitance and other parasitics that affect converter operation. The mathematical model is complex for the entire system, so only an example of the three-level boost with no parasitics is provided. The four timing intervals from Figure 3.3 are used.

A state X that includes only primary energy storage devices (the inductor current, the flying capacitor voltage, and the output voltage) is

$$X = \begin{bmatrix} i_L \\ v_{cfly} \\ v_{out} \end{bmatrix}. \tag{4.31}$$

The input of the converter is

$$u[k] = [V_{in}]. \tag{4.32}$$

The large signal model with four equivalent circuits made throughout the four switching intervals when only operating with the three-level boost is

$$\begin{gathered} x[k+1] = e^{A_4 t_4} e^{A_3 t_3} e^{A_2 t_2} e^{A_1 t_1} x[k] + \\ [e^{A_4 t_4} e^{A_3 t_3} e^{A_2 t_2} \times A_1^{-1}(e^{A_1 t_1} - I)B_1 + e^{A_4 t_4} e^{A_3 t_3} \times A_2^{-1}(e^{A_2 t_2} - I)B_2 \\ + e^{A_4 t_4} \times A_3^{-1}(e^{A_3 t_3} - I)B_3 + A_4^{-1}(e^{A_4 t_4} - I)B_4]u[k]. \end{gathered} \tag{4.33}$$

The example waveforms in Section 3.1 are generated through state space analysis. In addition, state space can model the states of every FET device C_{ds} (as seen in Figure 4.5 of the voltage waveforms across each of the four transistors in the boost stage) and other loss mechanisms such as parasitic inductances. Note the notation for Figure 4.5 references the transistor names of Figure 4.4. To model the hardware prototype in Chapter 5, parasitics of the PCB need to be included in the loss models.

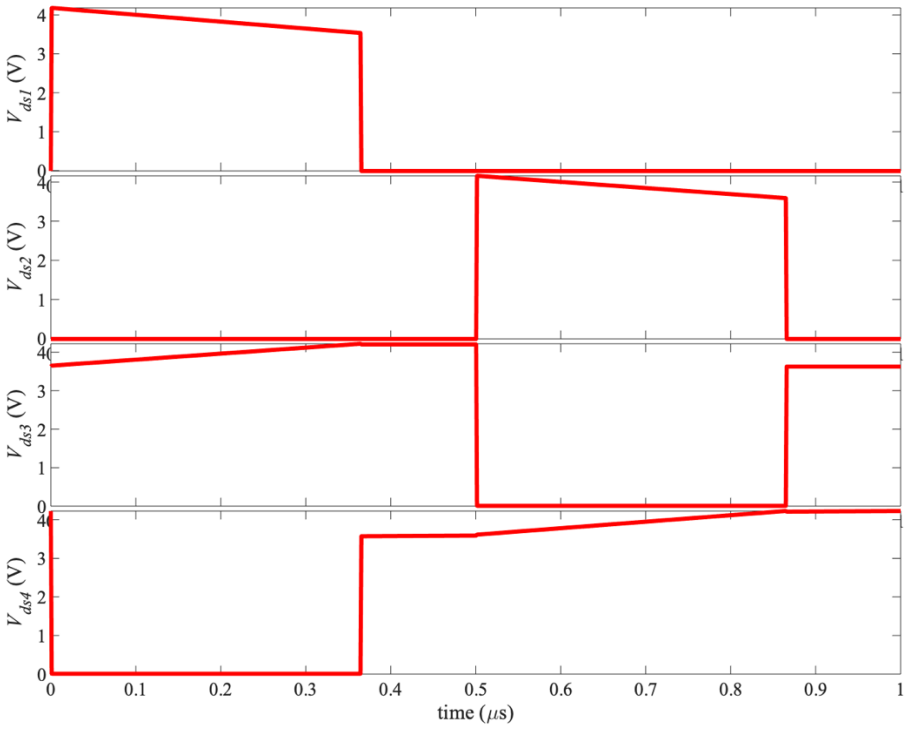

Figure 4.5: Voltages across C_{ds} observed with state space analysis.

Transient simulators such as LTspice takes over ten minutes to reach steady state with a schematic including multiple parasitics. State space analysis provides steady state solutions in seconds for comparison, so state space modeling allows for a wide range of operating points to be quickly analyzed. Average models based on the loss equations in Chapter 4 are accurate when the ripple in the converter is small. However, mobile implementation limits the size of the passives which yields a larger ripple. As the results in Chapter 5 will conclude, this discrete loss model is useful in accurately describing the converter's behavior across all operating points. However, both models are still useful in examining converter behavior. While the state space model completely models the dynamic transient behavior, the approximations of averaged loss models still provides an estimation of converter performance that is close to hardware results.

Chapter 5 Experimental Results

Using the average values (of I_L, V_{out}, V_{in}, and I_{out}) using loss equations in Section 4.1 and the state space model derived in Section 4.2, the circuit model is verified with a printed circuit board (PCB) prototype shown previously in Figure 4.4. Once this model is obtained, the converter prototype is built and tested in this chapter. Converter operation is further investigated as the design nears IC implementation.

5.1 Discrete Hardware

5.1.1 FPGA and Interface Board

To implement the converter modulation, a DE0-Nano with an Altera Cyclone IV FPGA [79] is utilized (shown in Figure 5.1). It has sufficient pins to provide the logic signals for each gate driver in the converter.

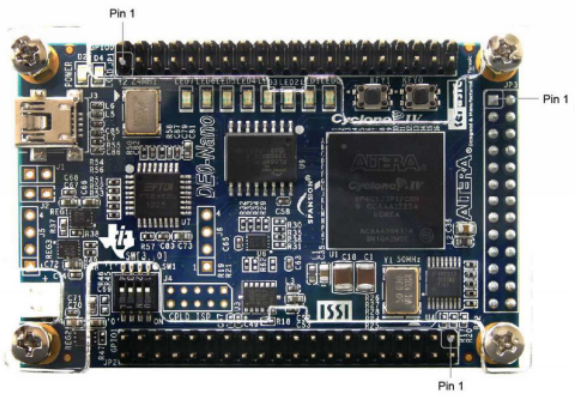

Figure 5.1: Altera Cyclone IV FPGA [79].

In Figure 5.2, the PCB of the interface board is shown. The interface board works in conjunction with the DE0-Nano to provide six separate isolated power supplies to each of the gate drivers to turn-on the transistors. Two of the power supplies on the board are referenced to ground. Each of the eight logic signals is given two paths to the DE0-Nano to provide a backup pin for programming (if necessary) as seen in Figure 5.2. The pin that is chosen for each logic path has a resistor pad that is shorted across to allow the flow of current for the signal. The entire PCB prototype and FPGA system are in Figure 5.3. The FPGA has a dead time of 5 ns based on its clock precision, and the dead time is included in all switching intervals for the hardware testing.

5.1.2 Power Stage Transistor Selection

EPC GaN devices are chosen for this project because of their switching performance and power density. The pool of GaN devices (narrowed down by investigation of parasitics) consist of EPC2023, EPC2024, and EPC2020. C_{eq_Q} is calculated using the method in [68] as discussed in Section 2.4. Table 5.1 shows the parasitics of the three EPC GAN HEMTs to be used.

Using state space analysis, the operating point in Table 3.1 is simulated. The converter operates at 6 A of charging current, a 2 μH inductor, and a flying capacitor of 5 μF. The modulation of Figure 3.3 is used. The resulting converter efficiency is analyzed and compares the performance of each of the three GaN devices in Figure 5.4. Gate charge loss is not included in that analysis because the gate charge loss is supplied from a separate power supply. The plot Figure 5.4 concludes that EPC2023 yields the most efficient converter across a range of frequencies, but EPC2024 is chosen based on device availability. It provides a similar efficiency and also has smaller gate charge loss. If gate charge loss is included in the analysis, at higher frequencies, the EPC2024 would provide the most efficient converter.

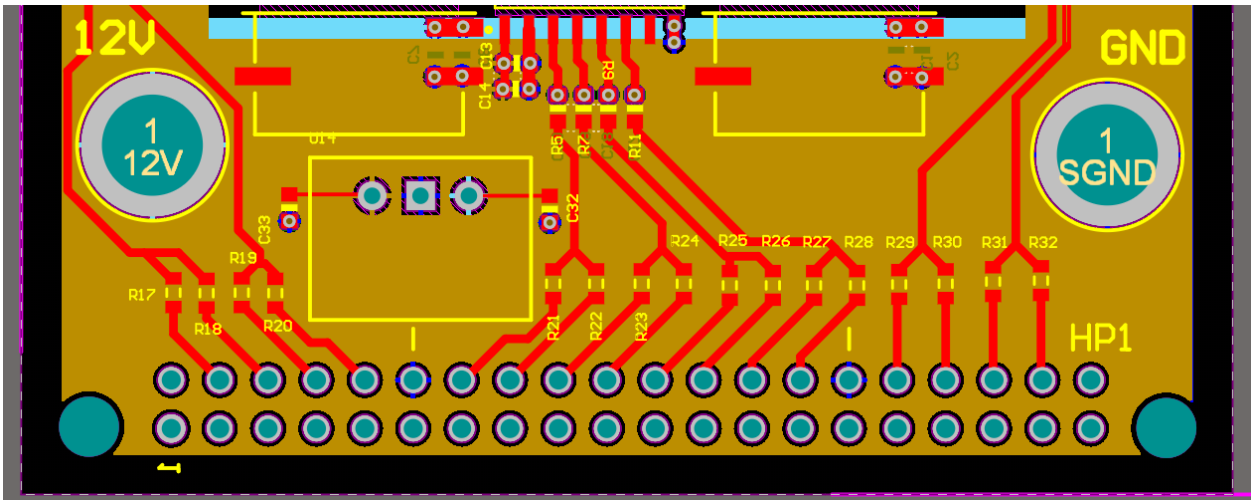

Figure 5.2: Outer Edge of PCB Layout of Interface Board and Connections to FPGA.

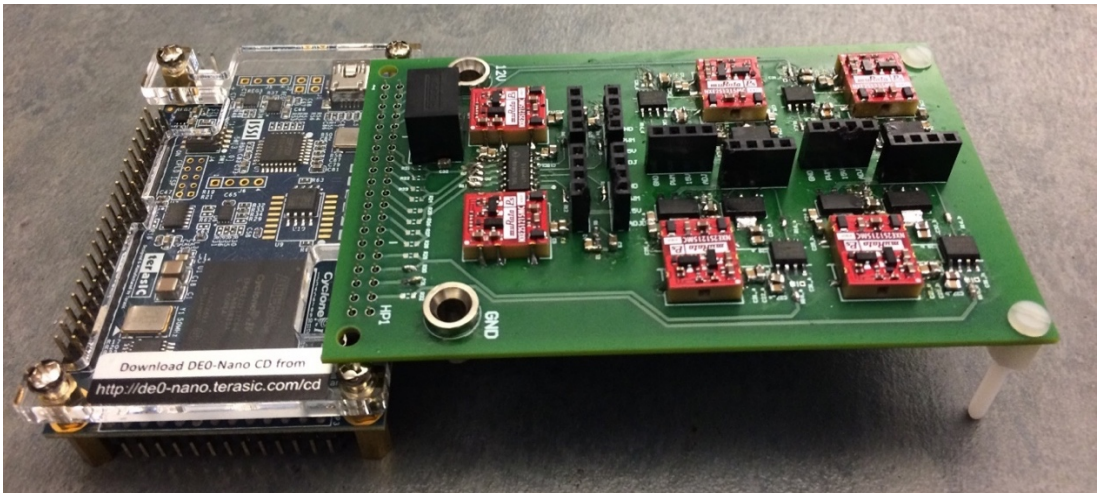

Figure 5.3: FPGA connected to the interface board with isolated supplies.

Table 5.1: Parasitics of Three EPC GaN Devices

Symbol	Name	EPC2023	EPC2024	EPC2020
V_{dsmax}	Maximum Voltage Rating for the Drain to Source Voltage	30 V	40 V	60 V
V_{gsmax}	Maximum Voltage Rating for the Gate to Source Voltage	6 V	6 V	6 V
r_{on}	Drain to Source Resistance	1.15 mΩ	1.2 mΩ	1.50 mΩ
Q_{oss}	Output Charge	30 nC	45 nC	50 nC
C_{eq_Q} (@ $V_{out}/2$)	Equivalent Charge	2300 pF	2500 pF	2250 pF
I_D	Maximum Drain Current	90 A	48 A	90 A
Q_g	Gate Charge	19 nC	18 nC	16 nC

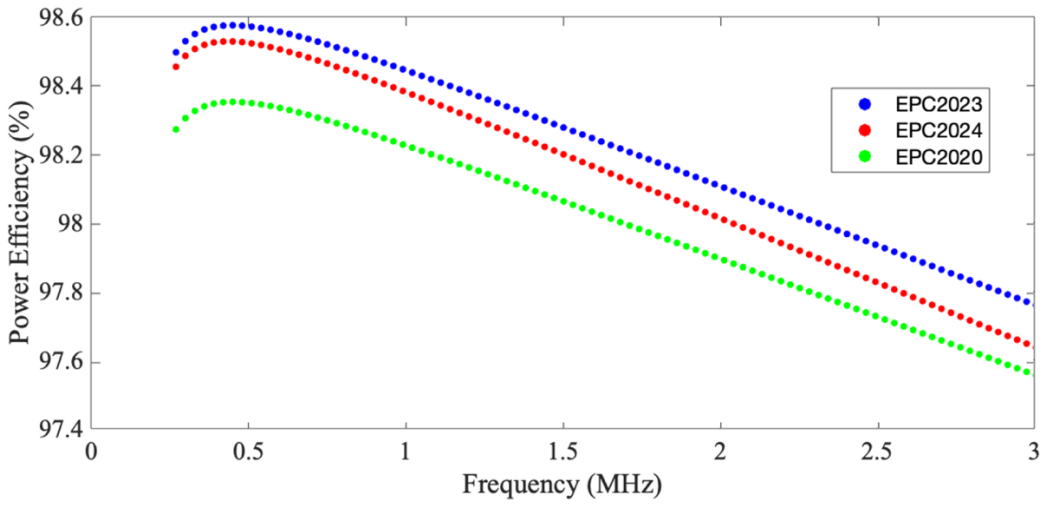

Figure 5.4: Power efficiency test for selecting EPC GaN devices.

5.1.3 Balance Transistor Selection

In order to implement the balance stage, transistors with large on-resistance and low output capacitance are needed. To adjust the equivalent resistance as needed, each balance transistor is placed in series with a pad for a surface mount resistor. To continue using GaN devices as discussed previously, the EPC8002 is chosen. EPC8002's parasitics are shown in Table 5.2. It has high on-resistance which helps keep the balance current at small magnitudes. Large balancing currents in this converter lower efficiency and increase charging time. The EPC8002 also has a low Q_{oss}, the equivalent charge, and Q_g.

5.1.4 Component Selection for Hardware Prototype

Table 5.3 lists the complete component selection for the hardware prototype for initial testing.

Table 5.2: Parasitics of EPC8002

Symbol	Name	EPC8002
V_{dsmax}	Maximum Voltage Rating for the Drain to Source Voltage	65 V
V_{gsmax}	Maximum Voltage Rating for the Gate to Source Voltage	6 V
r_{on}	Drain to Source Resistance	380 mΩ
Q_{oss}	Output Charge	6.7 pC
C_{eq_Q} (@ $V_{out}/2$)	Equivalent Charge	13 pF
I_D	Maximum Drain Current	2 A
Q_g	Gate Charge	133 pC

Table 5.3: Component Choice and Operating Parameters for Hardware Prototype

Symbol	Value	Symbol	Value
V_{in}	5 V	ESR_1	65 mΩ
V_{bat1}	4.08 V	ESR_2	65 mΩ
V_{bat2}	4.10V	ESR_{Cfly} (200 kHz)	2.7 mΩ
C_{fly}	9.1 μF	ESR_{Cfly} (500 kHz)	2.2 mΩ
L	22 μH	R_L	2.4 mΩ
R_{on} *EPC2024*	1.208 mΩ	C_{oss} *EPC2024*	2500 pF
R_{on} *EPC8002*	380 mΩ	C_{oss} *EPC8002*	13 pF
f_s	varied	$r_{balance}$	3.03 Ω
I_{out}	varied	C_{out}	23.5 μF

5.1.5 Measurement Setup

To increase the accuracy of test measurements, extra sense probes are attached to the electronic loads to eliminate the voltage drop across the probe leads. The electronic loads provide an equivalent resistance to emulate each battery. Each electronic load provides measurements for the current and voltage experienced by each battery. In addition, Kelvin connections are made for the voltage measurements on multi-meters to measure the respective values of each directly on the board. Kelvin connections eliminate the voltage drop across the leads from the sources and improve the accuracy of test measurements. An oscilloscope compatible with differential probes is used to observe circuit waveforms. PCB designs need to incorporate well-placed test points for differential probe connections for the best measurement results if voltages waveforms not referenced to ground need measurements. The hardware test setup is shown in Figure 5.5.

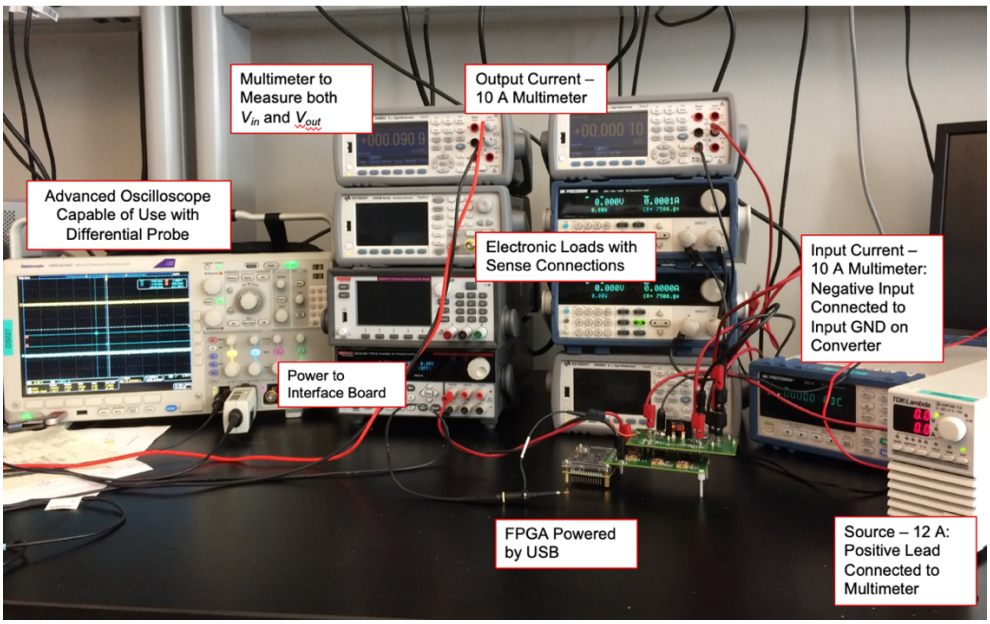

Figure 5.5: Hardware Test Setup.

5.1.6 Power Stage PCB

A PCB is manufactured for the prototype of the SC buck three-level boost converter. A top-side view of the PCB (populated with the components in Table 5.3) is shown in Figure 5.6. There are three half-bridge GaN FET gate drivers (LMG1210) to operate the six power stage transistors. Each half-bridge includes a bootstrap system to supply power to the high-side device. A single gate driver (LM5114) is provided for each of the balancing EPC8002 devices. The flying capacitor has three placements with 1210 (imperial code for 0.12 in by 0.10 in) pad sizes in a parallel configuration to reduce the equivalent capacitor *ESR*. Two 2.2 µF X7R 35 V and one 4.7 µF X7R 35 V capacitors are used to achieve an equivalent C_{fly} of 9.1 µF. The equivalent *ESR* is approximately 2.7 mΩ at 200 kHz and 2.2 mΩ at 500 kHz. The output capacitor has five placements with 0805 (0.08 in by 0.05 in) pad sizes each populated by a 4.7 µF X7R 50 V capacitor. Figure 5.7 shows a prototype side view, and Figure 5.8 details the four layer PCB layout.

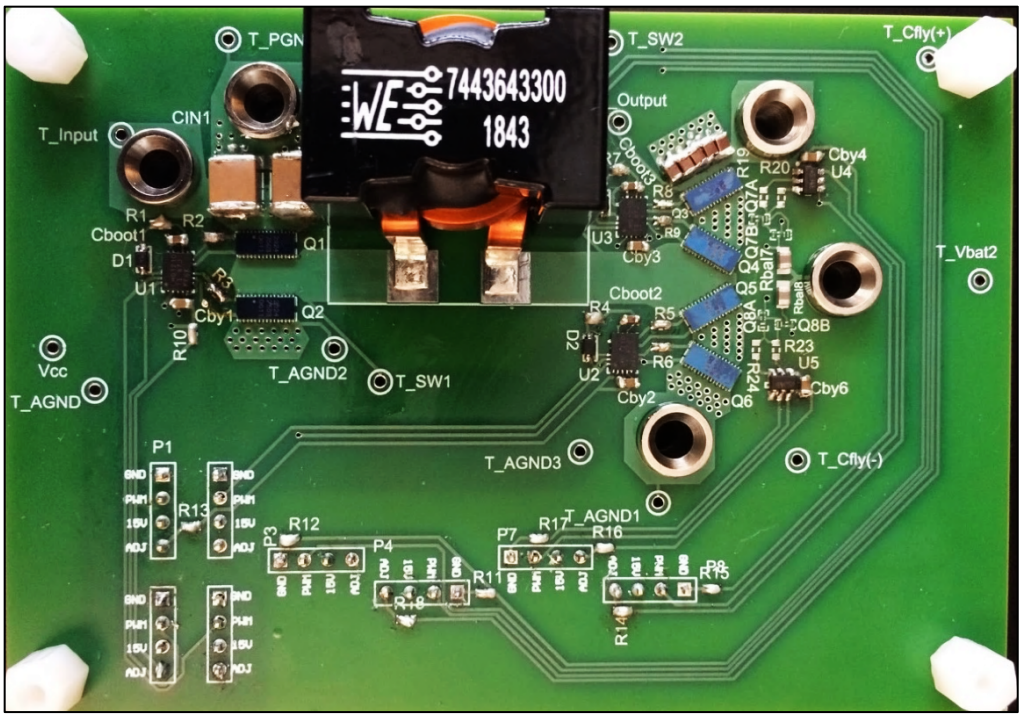

Figure 5.6: PCB prototype used to test SC buck 3L boost.

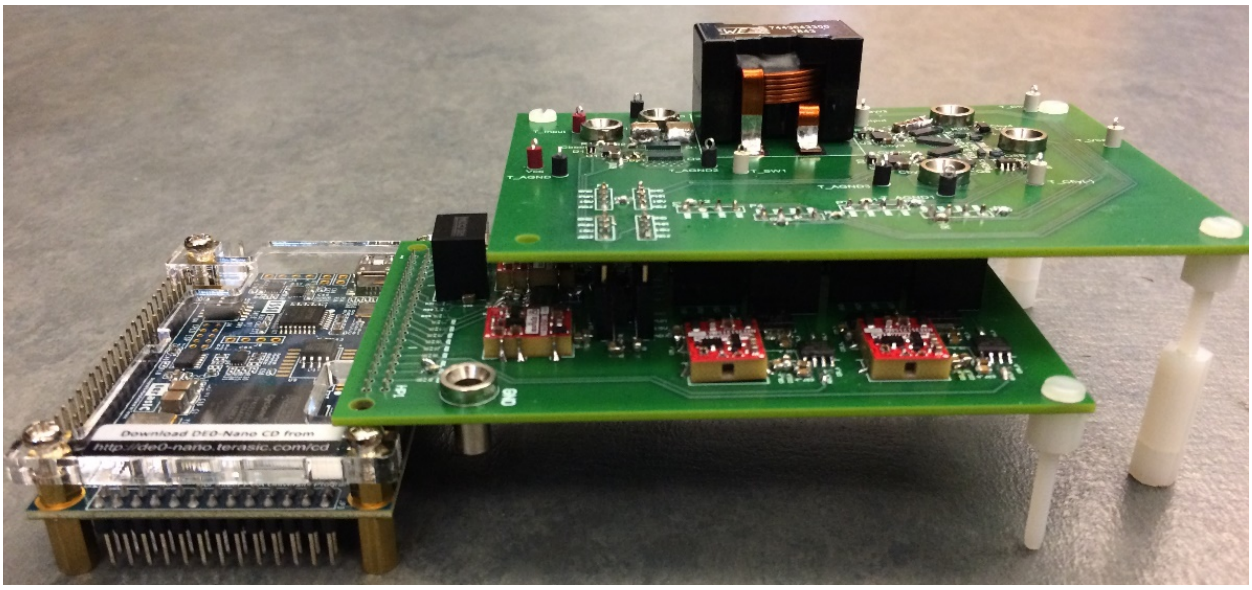

Figure 5.7: Entire system with converter PCB, interface board, and DE0-Nano (side view).

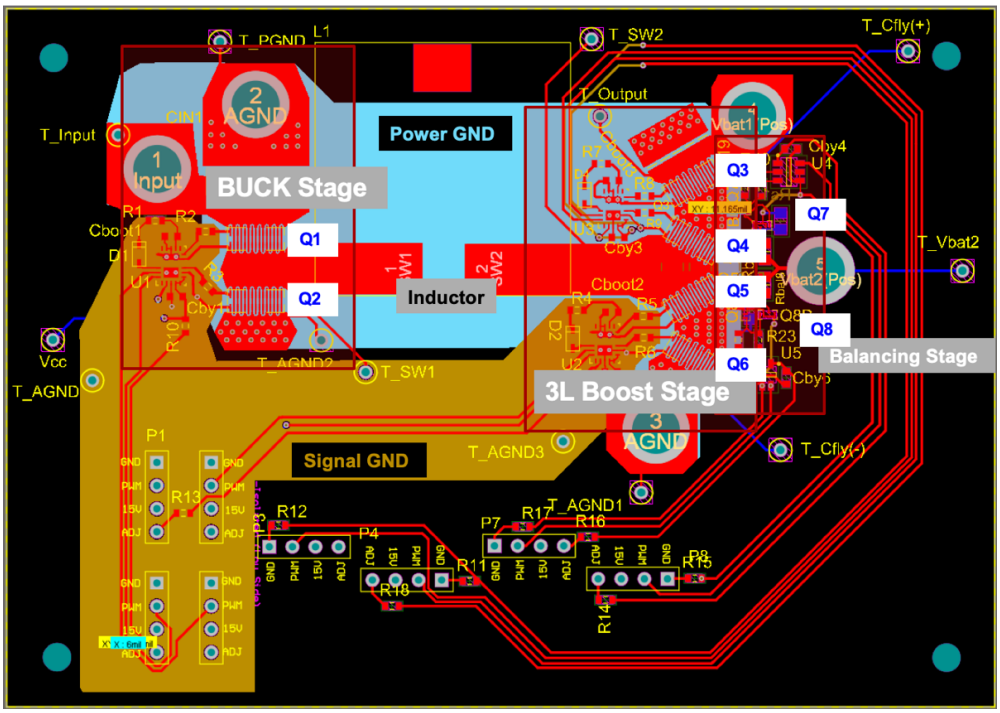

Figure 5.8: Buck three-level boost converter PCB. Top layer (Red) – top inner layer (Gold) – bottom inner layer (Light blue) – bottom layer (Blue)

5.2 Preliminary Results and Comparison

5.2.1 Hardware and Simulated Model Results

Output loads of 1.5 A, 4 A, and 6 A charging currents are tested at 200 kHz and 500 kHz. The efficiency of the system and the balance current is measured. For testing I_{out} = 1.5 A, r_{bat1} = 2.649 Ω and r_{bat2} = 2.662 Ω. The measured results for this operating point are in Table 5.4.

Experimental data are compared with analytical calculations using the average model and state space analysis in MATLAB pulling states from PLECs. It should be noted that a D_{buck} of 98.4% (200 kHz) and 96.0% (500 kHz) rather than a 100% duty cycle is used which increases D_{boost}. This is a limitation of the prototype but not the converter topology. Based on the available isolated

power supplies on the interface board and the large number of transistors, half-bridge gate drivers are chosen. However, these drivers utilize a bootstrap system to supply power to the high-side V_{gs} for each device. For this specific driver, it is calculated that the low-side device is must turn on for at least 40 ns to allow a path for the bootstrap capacitor to charge and supply power to the high-side. Therefore, these duty cycles are used. A new design should incorporate low-side single gate drivers for each device to allow D_{buck} to 100% to improve efficiency. V_{cfly} is captured in Figure 5.9 relative to V_{out}/2. CH1 is channel one, CMM is the measurement function of the oscilloscope (used to calculate half of the output voltage), and CH3 is channel three for the oscilloscope.

Table 5.4: Results for I_{out} = 1.5 A at 200 kHz and 500 kHz

	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	P_{in} (W)	P_{out} (W)	*Efficiency* (%)	*Balance Current* (mA)	I_{bat1} (A)	I_{bat2} (A)
Experiment	4.99	2.602	8.28	1.55	13.00	12.87	99.02	17.3	1.560	1.540
Average Model	5.00	2.55	8.40	1.50	12.74	12.60	98.90	15.5	1.508	1.492
State Space	5.00	2.58	8.31	1.53	12.92	12.75	98.70	13.6	1.541	1.527
Experiment	4.99	2.63	8.26	1.55	13.00	12.80	98.39	7.10	1.550	1.540
Average Model	5.00	2.56	8.40	1.50	12.82	12.60	98.30	6.80	1.503	1.497
State Space	5.00	2.60	8.31	1.53	12.99	12.74	97.99	5.60	1.536	1.530

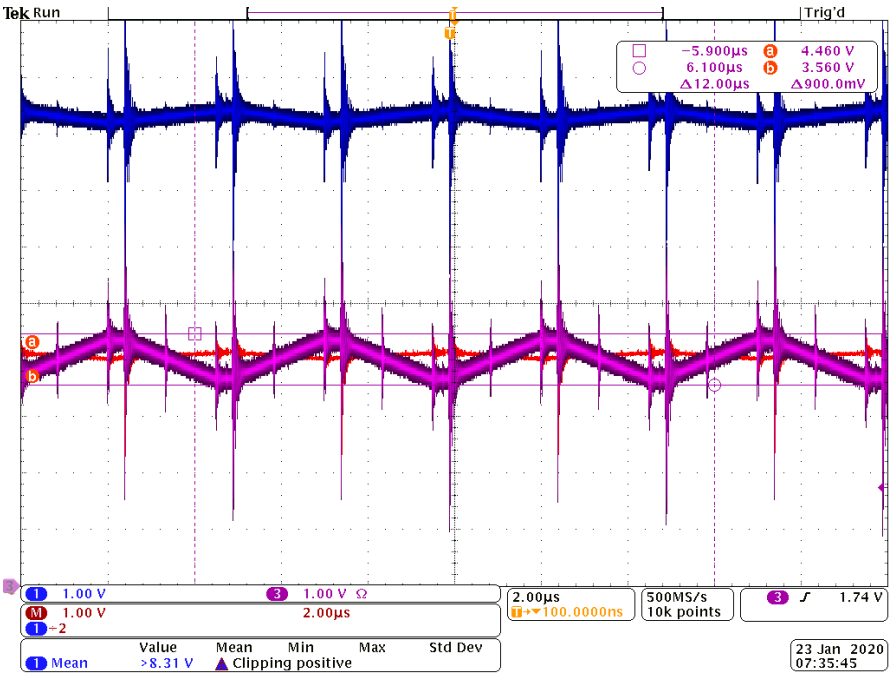

Figure 5.9: $v_{cfly}(t)$ waveform for I_{out} = 1.5 A at 200 kHz. CH1: V_{out} – CH3: $v_{cfly}(t)$ – CHM: $V_{out}/2$

Waveform measurements of the voltage across the balancing resistor are taken to show when the balancing takes place. The balance current is determined from the plots by dividing the voltage by the combination of the on-resistance of EPC8002 and the resistance of the balancing resistor. Each results table has the total balancing current that is measured using the electronic loads and confirmed via oscilloscope measurements. Each load reports a different current and the difference between the two is the net balance current. Note that the balance current decreases as switching frequency rises. The voltage drop is measured to show V_{bal6}, the voltage across the balancing resistor in series with Q_6 supplying a positive current (referenced to positive charging current) to charge Battery 1. V_{bal5}, the voltage across the balancing resistor in series with Q_5, has a negative current (referenced to positive charging current) to discharge the higher voltage Battery 2. Figure 5.10 shows the balancing waveforms.

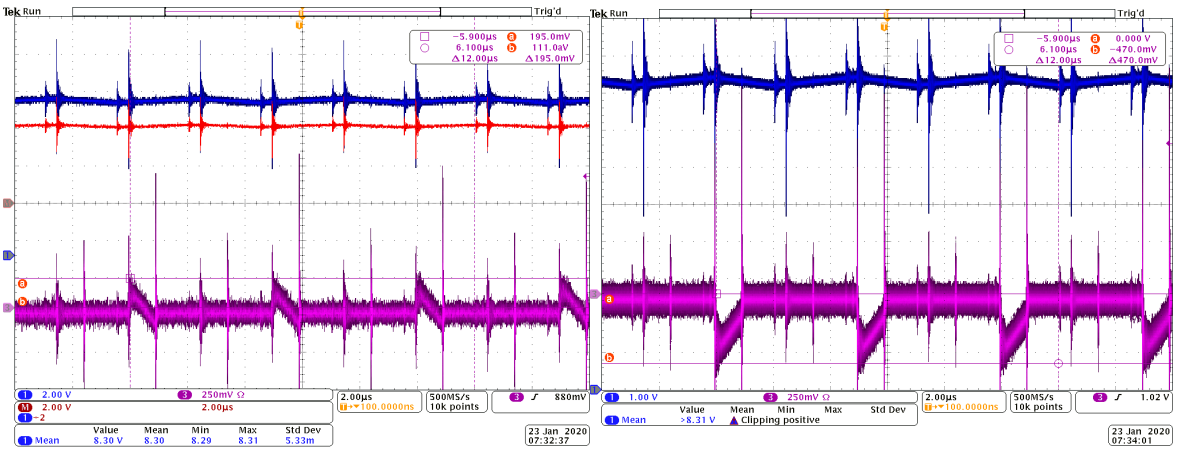

Figure 5.10: Balancing waveforms for I_{out} = 1.5 A at 200 kHz. (left) CH1: V_{out} – CH3: V_{bal6} – CMM: $V_{out}/2$ – (right) CH1: V_{out} – CH3: V_{bal5}

An approximation for the total balance current, ($I_{Balance}$), with small current ripple used by the average model is

$$I_{Balance} = \left(\frac{\frac{I_L}{2 \cdot C_{Fly} \cdot fs} \cdot D_{Boost}}{r_{balance} \cdot 2} \cdot D_{Boost} \cdot 45\ \% \right) \cdot 2. \tag{5.1}$$

Equation (5.1) assumes that V_{cfly} is averaged to $V_{out}/2$, and the time $v_{cfly}(t)$ remains above or below $V_{out}/2$ is 45 % of $D_{boost} \cdot T_s$. The approximation of 45 % of D_{boost} incorporates output ripple. This approximation takes the magnitude of the ripple, divides it by the balance resistance ($r_{balance}$), and halves the total as if the current decreases linearly to zero as seen in Figure 3.5 and Figure 5.10. The average is then solved by taking the halved total and multiplying it by the ratio of the balance time over T_s. For testing I_{out} = 4 A, r_{bat1} = 1.034 Ω and r_{bat2} = 1.039 Ω. The results are shown in Table 5.5 for both 200 kHz and 500 kHz. Figure 5.11 shows V_{cfly} captured at 200 kHz for the test point in Table 5.5 at this frequency. Followed by this is Figure 5.12 with the balance current waveforms at 200 kHz.

Table 5.5: Results for I_{out} = 4.0 A at 200 kHz and 500 kHz

	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	P_{in} (W)	P_{out} (W)	*Efficiency* (%)	*Balance Current* (mA)	I_{bat1} (A)	I_{bat2} (A)
Experiment	5.00	7.06	8.454	4.061	35.32	34.33	97.21	51.2	4.087	4.036
Average Model	5.00	6.88	8.450	4.000	34.53	33.60	97.32	48.0	4.024	3.976
State Space	5.00	7.03	8.506	4.024	35.15	34.23	97.27	47.5	4.048	4.000
Experiment	5.00	6.99	8.400	4.034	34.94	33.88	96.97	18.0	4.043	4.025
Average Model	5.00	6.94	8.400	4.000	34.68	33.60	96.88	20.9	4.006	3.994
State Space	5.00	7.05	8.509	4.026	35.25	34.25	96.86	19.0	4.035	4.016

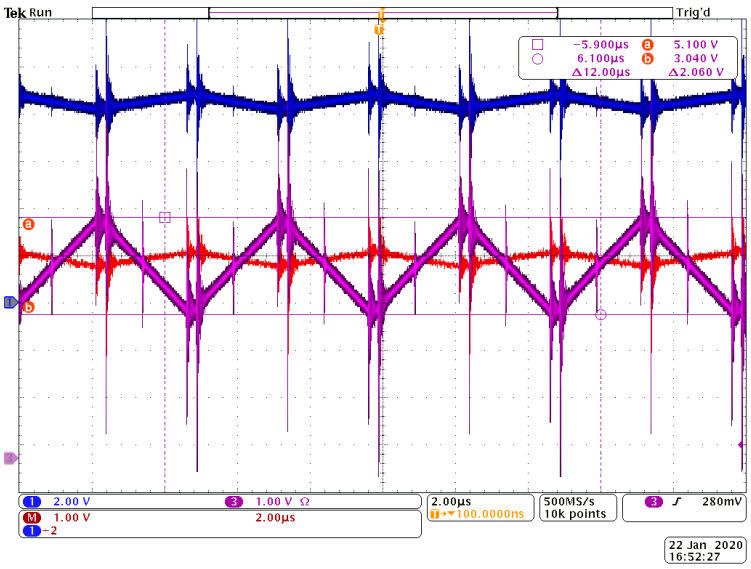

Figure 5.11: $v_{cfly}(t)$ waveform for I_{out} = 4 A at 200 kHz. CH1: V_{out} – CH3: $v_{cfly}(t)$ – CHM: $V_{out}/2$

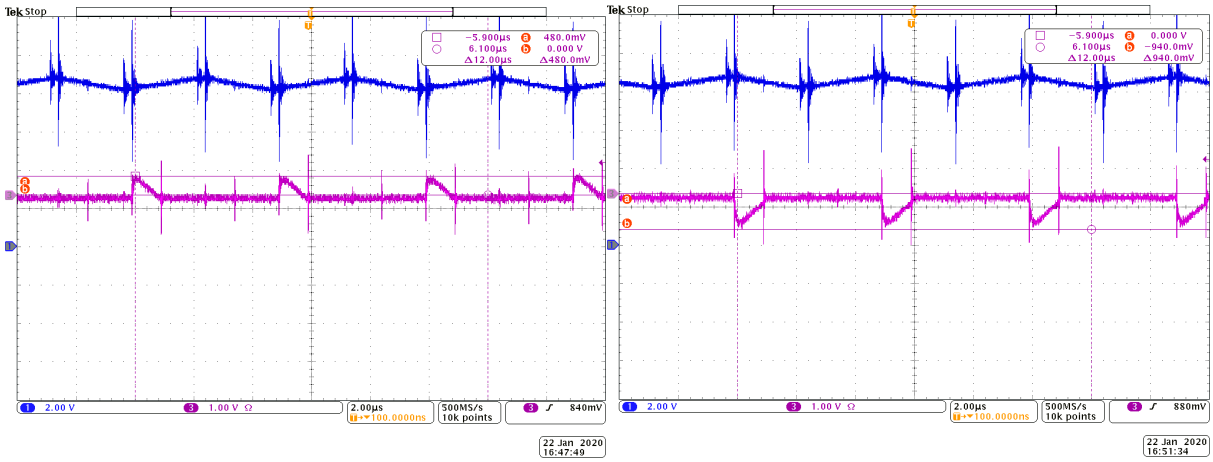

Figure 5.12: Balancing waveforms for I_{out} = 4 A at 200 kHz. (left) CH1: V_{out} – CH3: V_{bal6} – (right) CH1: V_{out} – CH3: V_{bal5}

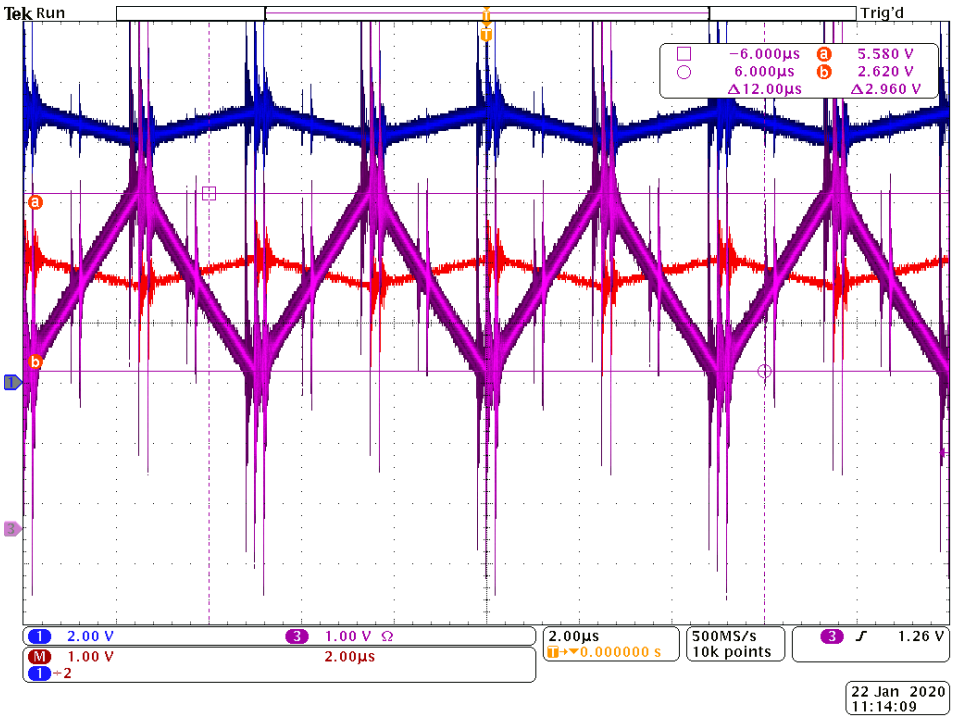

Figure 5.13: $v_{cfly}(t)$ waveform for I_{out} = 6 A at 200 kHz. CH1: V_{out} – CH3: $v_{cfly}(t)$ – CHM: $V_{out}/2$

For testing I_{out} = 6 A, r_{bat1} = 0.711 Ω and r_{bat2} = 0.7142 Ω. The results are shown in Table 5.6 for both 200 kHz and 500 kHz. Figure 5.13 shows the V_{cfly} at 200 kHz. The balance waveforms correspond to the same operating point and frequency shown in Figure 5.13. The parasitic inductance does affect the waveforms in the PCB as test points on the PCB were not properly placed for differential probing. Each node for $v_{cfly}(t)$ for the hardware prototype required wire leads to attach to the differential probe which introduced a parastic inductance in the measurement loop. Though the measurement leads are attempted to be intertwined to reduce the area of the loop to minimize the parasitic inductance where possible, the non-ideal measurement setup leads to some ringing on the converter waveforms. A future prototype if needed needs to account for better connections for differential probing. Other sources of ringing originate from parasitic inductance at the source of each power state transistor.

Table 5.6: Results for I_{out} = 6.0 A at 200 kHz and 500 kHz

	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	P_{in} (W)	P_{out} (W)	*Efficiency* (%)	*Balance Current* (mA)	I_{bat1} (A)	I_{bat2} (A)
Experiment	5.00	10.70	8.554	5.976	53.48	51.118	95.58	84.8	6.018	5.934
Average Model	5.00	10.63	8.500	6.000	53.13	51.0	96.00	82.5	6.041	5.959
State Space	5.00	10.70	8.640	5.947	53.51	51.37	95.82	80.4	5.988	5.907
Experiment	5.00	10.61	8.511	5.950	53.07	50.63	95.43	29.9	5.965	5.935
Average Model	5.00	10.68	8.500	5.961	53.30	51.0	95.58	32.0	6.017	5.994
State Space	5.00	10.72	8.640	5.950	53.72	51.6	95.40	31.4	5.966	5.934

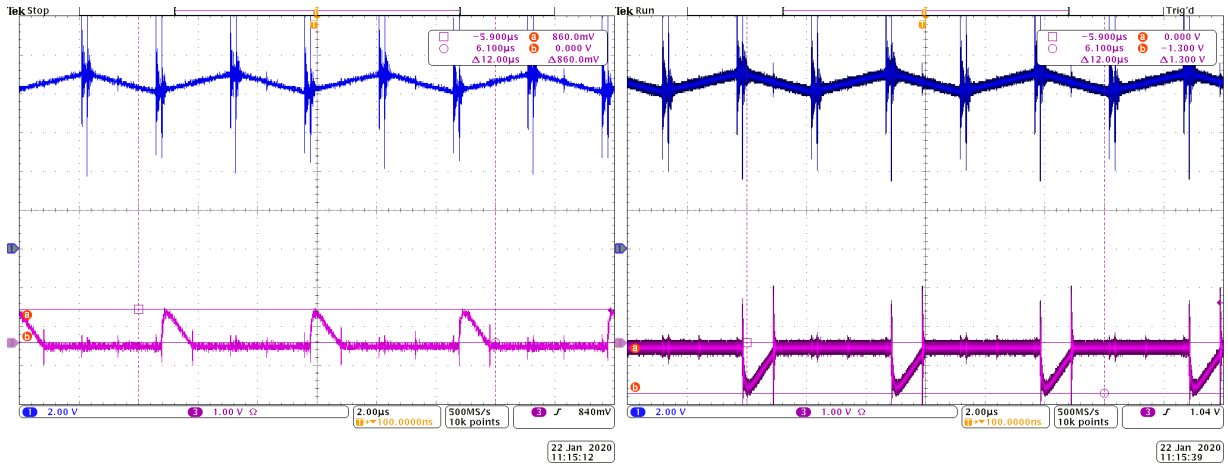

Figure 5.14: Balancing waveforms for I_{out} = 6 A at 200 kHz. (left) CH1: V_{out} – CH3: V_{bal6} – (right) CH1: V_{out} – CH3: V_{bal5}

5.2.2 Data Analysis

Additional parasitics of the PCB such as copper trace inductance are included in the calculated data. Across a range of loads and operating switching frequencies, both the average model and state space analysis report accurate predictions compared to the hardware. This adds credence that both the average and state space analysis approach an accurate model that correctly predicts the behavior of the converter. Though the average analytical model does not account for the full dynamic behavior of the model, it still provides a fast and near accurate approximation, especially at operation with small ripple. For the test results in Chapter 5, a large inductor and flying capacitor are utilized that limit the effect that ripple has on the circuit.

5.2.3 Loss Model Comparison with Hardware Results

The following plots are given to summarize the data from the simulated and hardware test results from Table 5.4, 5.5 and 5.7. In Figure 5.15, the efficiency across charging current at both 200 kHz and 500 kHz is provided. In Figure 5.16, the balance current data across charging current at both

200 kHz and 500 kHz is provided. Each plot shows the measurements from the hardware test setup, the average model equations using loss equations from Section 4.1, and state space analysis followed similar trends across charging current loads. The trend exists for 200 kHz and 500 kHz.

5.2.4 Loss Breakdown

The lowest efficiency point, I_{out} = 6 A at 500 kHz, is further analyzed to break down the power loss in Table 5.7. Gate charge loss is not included because this loss occurs in the interface board power separately from the converter prototype. In the tested frequency range with V_{in} = 5 V, conduction loss is the dominant source of loss and remains the highest across every operating point tested. The state space model provides the steady state waveforms for the operating point used in Table 5.7. The parasitic inductance of PCB traces affects converter waveforms and is incorporated in the state space model. Parasitic inductance exists because of the power loops created in layout of the PCB. Though the loops are designed to be small, a small inductance still is present affecting waveforms and estimated to be around 20 pF (for each power loop) based on comparisons between simulation and hardware results. I_L is in Figure 5.17 and V_{cfly} in Figure 5.18. Figure 5.17 displays an inductor current that experiences different slopes in each half-period. This is because the buck converter only switches during one of the half-period intervals which adds an inconsistent disturbance. However, at large inductances, the effect on the average of V_{cfly} is minimum because the peak-to-peak current ripple is small. When inductors less than 1 μH are included in the design, an alternative modulation is used that is demonstrated in Section 5.3.

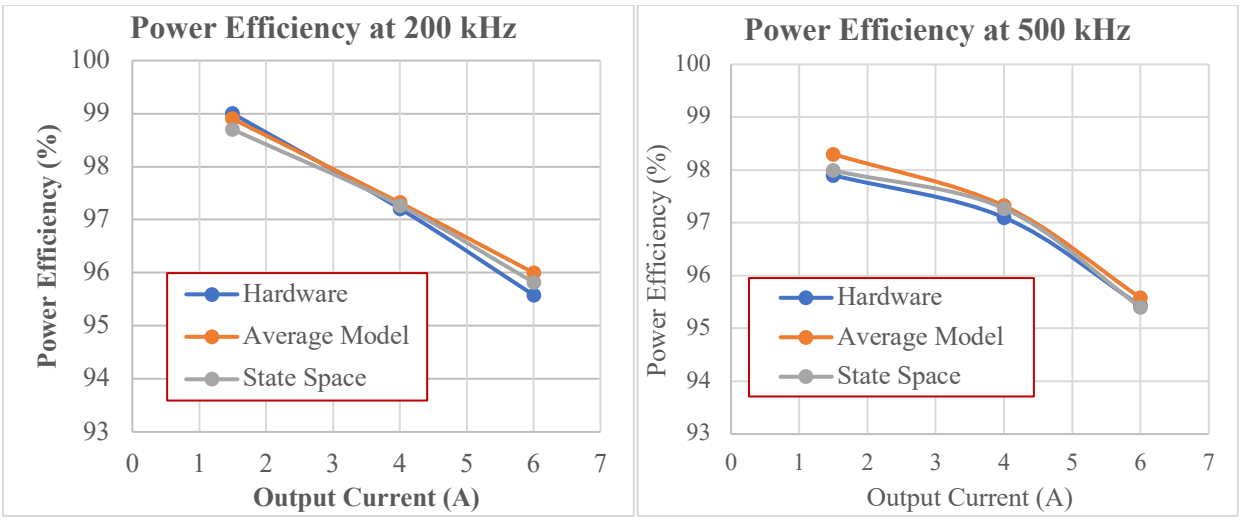

Figure 5.15: Power efficiency data at 200 kHz (left) and 500 kHz (right).

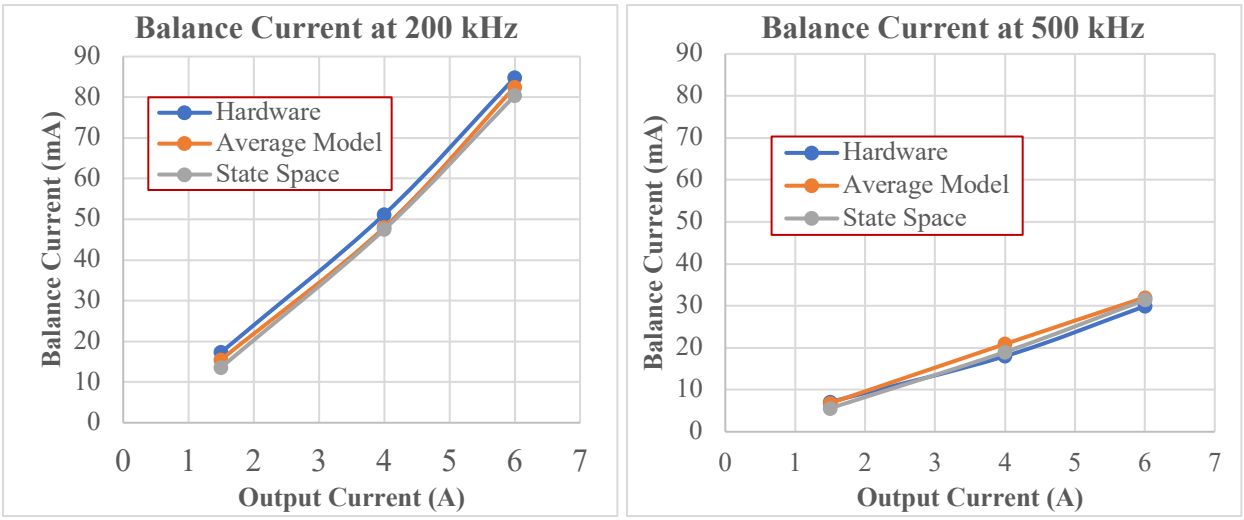

Figure 5.16: Balance current data at 200 kHz (left) and 500 kHz (right).

Table 5.7: Power Loss Examination for I_{out} = 6 A at 500 kHz (V_{in} = 5 V)

Type of Loss	Symbol	Power	Percentage of Power Loss
Conduction Loss	P_{cond}	1.770 W	76.49 %
C_{oss} Loss	P_{Coss}	76.50 mW	3.31 %
Overlap Loss	$P_{overlap}$	195.6 mW	8.45 %
Body Diode Loss	P_{bd}	208.1 mW	8.90 %

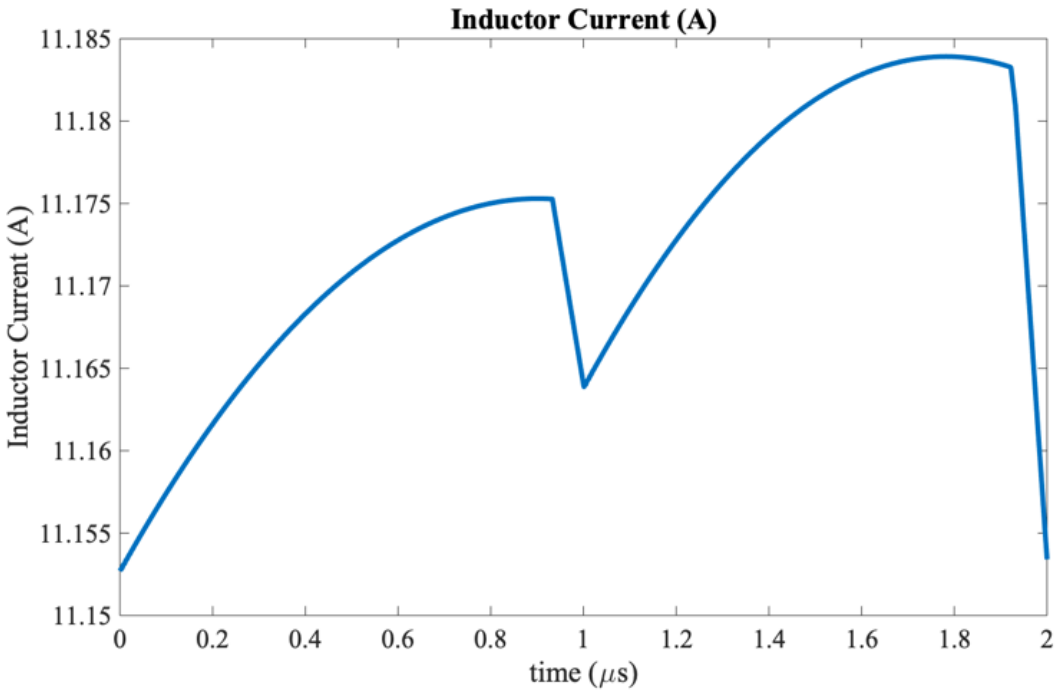

Figure 5.17: Inductor current for I_{out} = 6 A at 500 kHz (V_{in} = 5 V) from state space model.

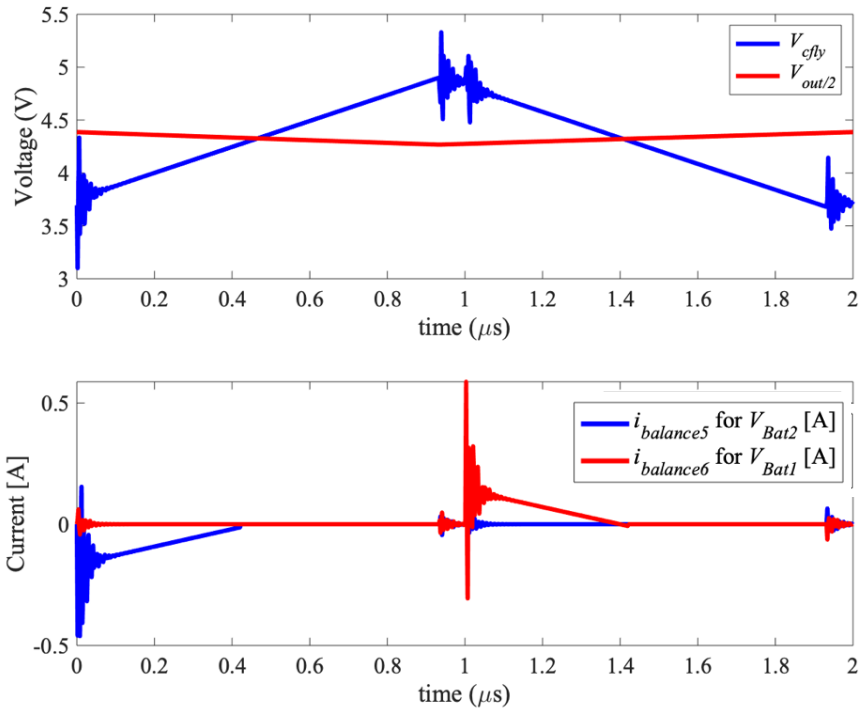

Figure 5.18: Flying capacitor voltage and balance current for I_{out} = 6 A at 500 kHz (V_{in} = 5 V) from state space model.

If the input voltage is changed to V_{in} = 20 V, P_{Coss} becomes more significant. Though it may come into a comparable range, P_{cond} remains the largest source of loss. Table 5.8 displays an example of V_{in} = 20 V operation with GaN devices, f_s = 500 kHz, D_{buck} = 40 %, D_{boost} = 20 %, and an efficiency of 97.16%. The reason this converter experiences less loss is because the I_{Lrms} is much smaller than the value for the results in Table 5.7. Also, the equivalent C_{oss} decreases as the blocking V_{ds} voltage across the transistor increases, so the GaN HEMTs at the buck stage experience a smaller C_{oss} than those at the boost stage because $V_{in} > V_{out}$. However, GaN HEMTs have higher C_{oss} than the LDMOS devices used in the IC design. As Table 5.8 concludes, conduction loss remains the largest source of loss for the SC buck three-level boost converter. Therefore, devices with smaller on-resistance should be selected to increase converter efficiency.

Table 5.8: Power Loss Examination for I_{out} = 6 A at 500 kHz (V_{in} = 20 V)

Type of Loss	Symbol	Power	Percentage of Power Loss
Conduction Loss	P_{cond}	879.5 mW	55.63 %
C_{oss} Loss	P_{Coss}	350.0 mW	22.2 %
Overlap Loss	$P_{overlap}$	286.6 mW	18.2 %
Body Diode Loss	P_{bd}	63.3 mW	4.01 %

5.3 Buck Modulation Examination via State Space

In the previous experiments, the buck stage uses the conventional two-level modulation. As the design changes its focus towards IC design, smaller passives are required leading to large ripple on energy storage components. An alternative modulation strategy when a two-level buck is added at the input stage is given in this section to provide better balancing on V_{cfly}.

5.3.1 Alternative Buck Stage Modulation

As discussed in Section 3.2.5, reducing the disturbances in the inductor current between each half-period results in V_{cfly} balanced closer to $V_{out}/2$. When $V_{in} < V_{out}$, the high-side of the two-level buck input stage is turned ON for the duration of the period (D_{buck} = 100 %). A different approach is taken when $V_{in} > V_{out}$. The required D_{buck} for the two-level input is then split in half between each half-period. Because the three-level converter experiences its current ripple at twice the switching frequency, switching the buck in this manner allows equal disturbance for each half-period which leads to better balancing on the flying capacitor. The tradeoff for this benefit is that the input buck stage experiences twice the switching loss. Another possible solution is to place a three-level buck

stage at the input instead which also has the same inductor current qualities. If a situation arises where only the buck stage is needed (Q_3 and Q_4 are held ON during the entire period), the modulation in Figure 5.19 is not used because of large switching loss. The conventional buck modulation is then used.

5.3.2 Alternative Buck Stage Evaluation with State Space Analysis

To show how the buck modulation from Figure 5.19 provides better balancing at V_{cfly} in large ripple scenarios, examine the following figures where D_{boost} = 19 %, D_{buck} = 38.8 %, V_{in} = 20 V, I_{out} = 5 A, C_{fly} = 4.7 μF, f_s = 500 kHz, and both batteries are nearly fully charged. State space is used to provide model waveforms. In Figure 5.20, conventional two-level buck modulation is used with a large inductor of 200 μH. Because the current ripple is small, V_{cfly} is still approximately balanced to $V_{out}/2$ although lower than the expected value by 32 mV. Notice the various slopes of the inductor current. This offset leads to $I_{balance6}$ not being able to achieve an equal but opposite magnitude as $I_{balance5}$.

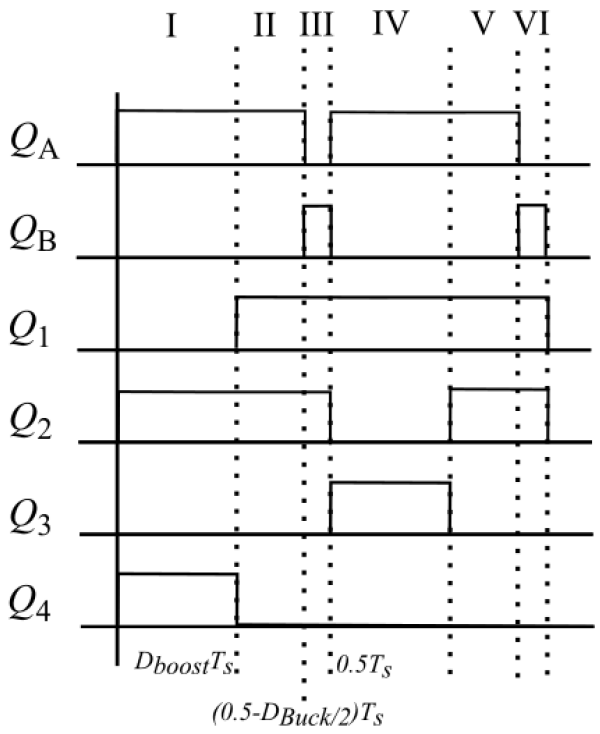

Figure 5.19: Alternative modulation for the buck three-level boost converter.

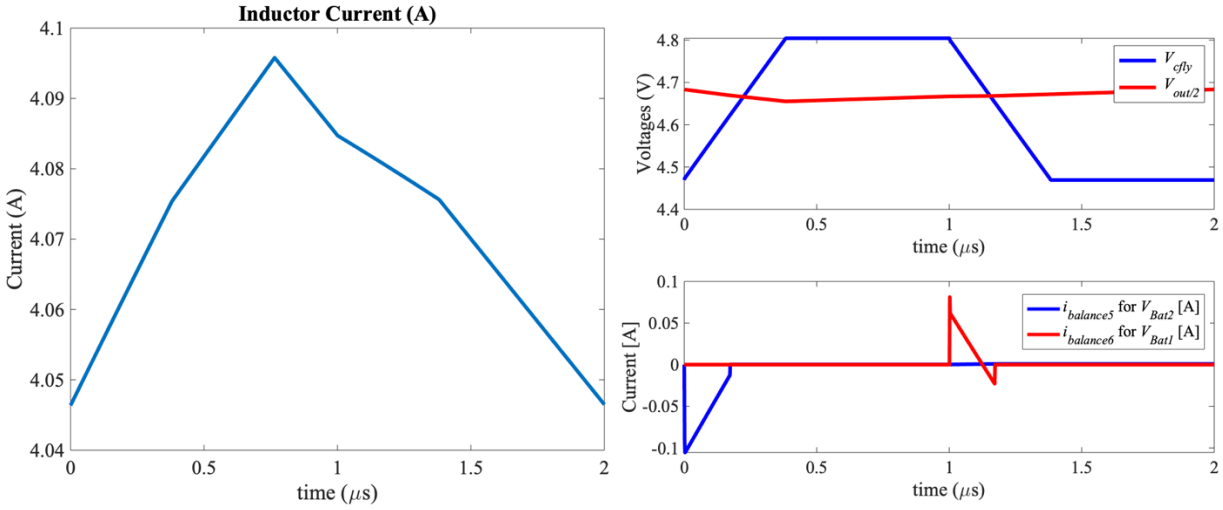

Figure 5.20: $i_L(t)$ (left) and $v_{cfly}(t)$ with balance currents (right) when L = 200 µH.

In Figure 5.21, the conventional two-level buck modulation is used, but the inductance is now 10 µH. The current ripple increases to twenty times the previous experienced in Figure 5.20. At all points, $v_{cfly}(t)$ is smaller than $V_{out}/2$. No positive balancing currents are possibly generated. An investigation of the converter balancing when only balance transistor is activated per period is done next. In Figure 5.22, only one balance transistor is activated during 45 % of the interval when balancing is possible. When only Q_5 is activated, 67.0 mA of balance current is achieved to discharge Battery 2. When only Q_6 is activated, 66.0 mA of balance current is achieved to discharge Battery 2 (which improperly discharges Battery 1, so this balancing cannot be used). If only Q_5 is activated for the entire duration of possible ON-time (while Q_6 is conducting), 69.0 mA of balance current is achieved to discharge Battery 2. In Figure 5.23, operating Q_5 for a longer amount of time actually helps push the average of V_{cfly} towards $V_{out}/2$ from the scenario, so the overall balance current remains the relatively the same as the value in Figure 5.22.

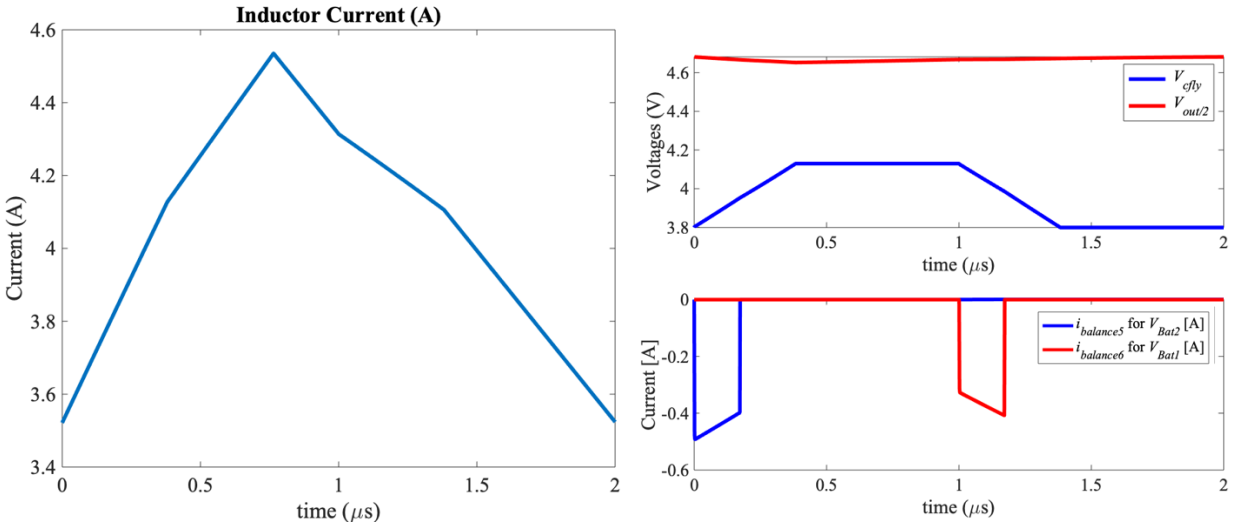

Figure 5.21: $i_L(t)$ (left) and $v_{cfly}(t)$ with balance currents (right) when L = 10 µH.

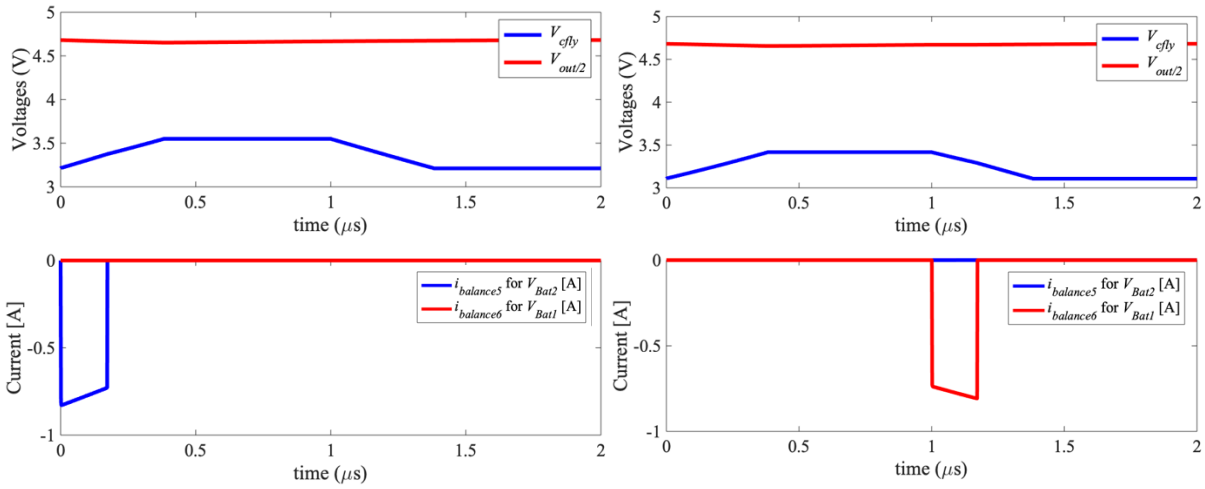

Figure 5.22: $I_{balance5}$ (left) and $I_{balance6}$ (right) modeled in state space when L = 10 µH.

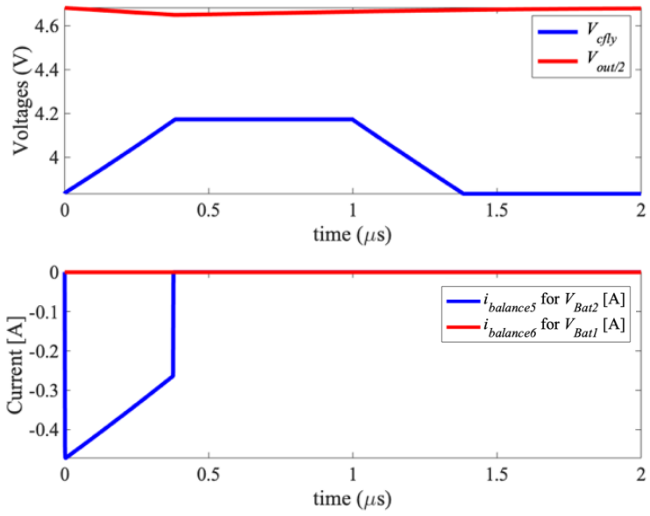

Figure 5.23: $I_{balance6}$ with an ON-duration of D_{boost}·T_s modeled in state space when L = 10 µH.

In Figure 5.24, the buck duty cycle is halved and switches at $2{\cdot}f_s$ using the modulation from Figure 5.19 using an inductance of 10 μH. Because the disturbance of the buck switching is experienced during each half period, the inductor current charges and discharges C_{fly} equally during each half period. The total balance current is 68 mA, but the efficiency of the system drops to 91.6 % from 93.41 % (with L = 10 μH and conventional two-level modulation) because of the increased switching loss. However, the EPC2024 loss models used in these salutations have higher C_{oss} loss the LDMOS devices to be used in the IC design, so the power loss increase is not as large in the IC design. The main advantage of the buck switching at $2{\cdot}f_s$ is balancing of V_{cfly} to half the output voltage. Chapter 6 demonstrates that the average of V_{cfly} maintains a value close to half the output when the inductance decreases below 10 μH (down to the range of 100's of nanohenries). As indicated in Figure 5.22 and Figure 5.23, the only balancing capability possible if $v_{cfly}(t)$ is always less than $V_{out}/2$ is when V_{bat1} is less than V_{bat2}. CPM could perhaps adjust the V_{cfly} average to that greater than $V_{out}/2$ to balance the batteries when V_{bat1} is greater than V_{bat2}, but that is not researched in this work. This work focuses on the SC integration feasibility with the three-level boost, so the alternative modulation in Figure 5.19 is used for future modeling and testing. Future work investigates if the modulation in Figure 5.19 (that aids the balancing of the average of V_{cfly} to half the output voltage) is worth the increased switching power loss. Other input structures like the three-level buck may provide the balancing of the average V_{cfly} to half the output voltage and better power efficiency than the two-level buck input stage using the alternative modulation.

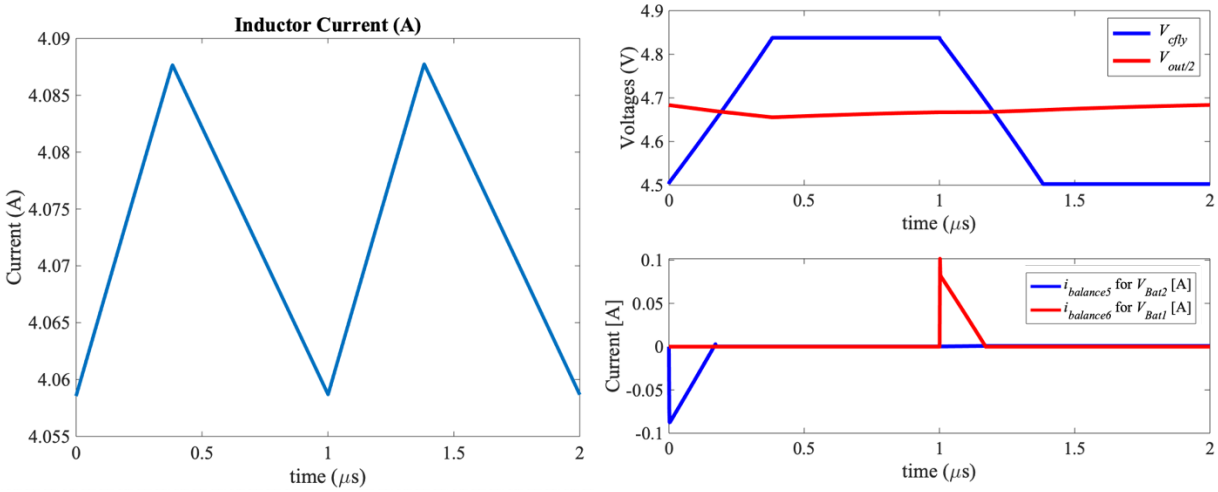

Figure 5.24: $i_L(t)$ (left) and $v_{cfly}(t)$ with balance currents (right) when L = 10 µH.

5.4 Other Battery Charging Scenarios

State space analysis is used to evaluate other battery situations that the SC buck three-level boost charger may face. The previous sections only address small voltage differentials between V_{Bat1} and V_{Bat2} where V_{Bat2} is slightly greater and both batteries are near full charge. In all the following examples, the inductance is 200 µH, C_{fly} is 2.2 µF, V_{in} = 20 V, I_{out} = 5 A, f_s = 1 MHz, and EPC2024 GaN FETs are chosen for the transistors. PCB parasitics are not included. The alternative buck modulation in Figure 5.19 is used, and D_{boost} is 15.0 %. No other parasitic losses are considered. The balancing time is 45 % of the possible time to balance ($D_{boost} \cdot T_s$). Balance resistance is 1 Ω.

5.4.1 Large Voltage Differential

Battery 2 is replaced with a new battery (assume 100 % SOC and V_{Bat2} = 4.2 V) and Battery 1 is near depletion with a current voltage of V_{Bat1} = 3.6 V. This example is shown in Figure 5.25. Balancing current of 40 mA is provided to balance the battery system, and there is no difference than previous charging tests and examples other than a 0.6 V initial voltage difference between the two batteries.

5.4.2 Battery 1 Voltage Greater Than Battery 2

A similar situation where Battery 1 is replaced with a new battery (assume 100 % SOC and V_{Bat1} = 4.2 V) and Battery 1 is near depletion with a current voltage of V_{Bat2} = 3.6 V. This example is shown in Figure 5.26. A total balance current of 40 mA is also generated

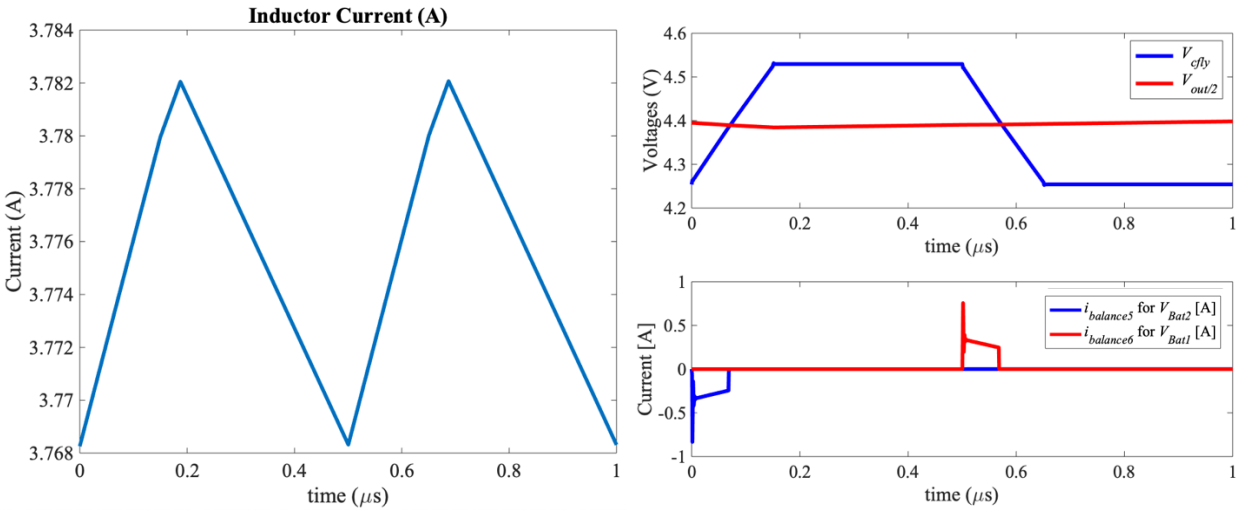

Figure 5.25: $i_L(t)$ (left) and $v_{cfly}(t)$ with balance currents (right) when $V_{Bat2} >> V_{Bat1}$.

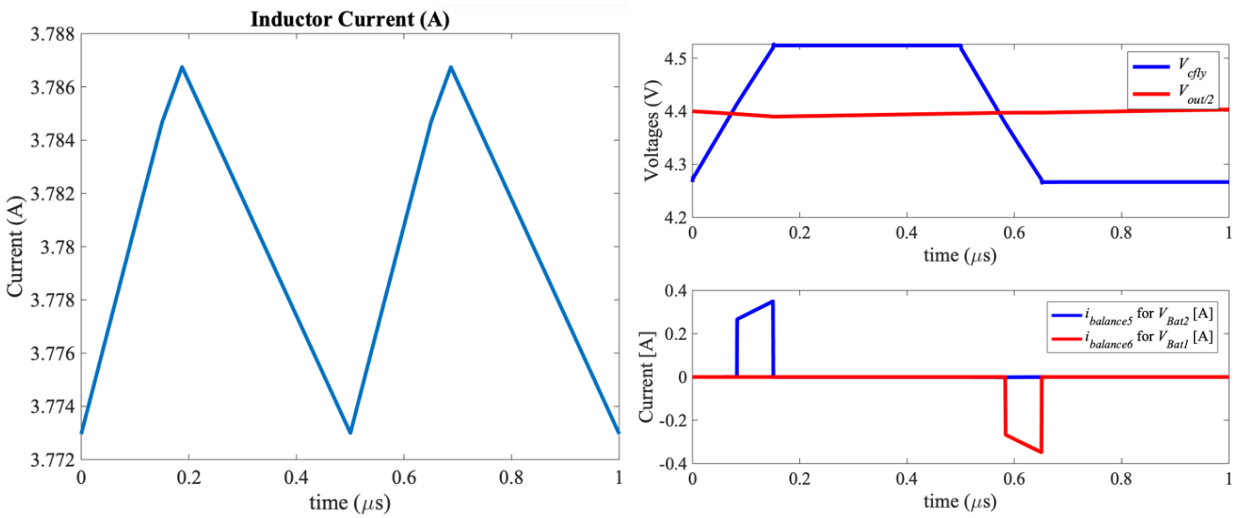

Figure 5.26: $i_L(t)$ (left) and $v_{cfly}(t)$ with balance currents (right) when $V_{Bat2} << V_{Bat1}$..

5.5 Inductor Current Control Testing

Though the PCB prototype operates in open-loop, the FPGA is manually programmed to tune the current waveform. A hardware test is conducted to prove tuning the timing interval based on inductor current evaluation pushes the average of V_{cfly} closer to $V_{out}/2$. The first test shows V_{cfly} without any tuning. Knowing 5 ns is the smallest increment of adjustment available with the Altera Cyclone IV FPGA, the second test decreases the length of interval I by 5 ns, increases the length of interval II by 10 ns, and decreases III by 5 ns to keep T_s the same. The converter operates at 95.59 % efficiency at 45 W, 5A output operating point. The frequency is 500 kHz. V_{in} = 5 V, so the inductor current is large with D_{buck} = 97.2 % and D_{boost} = 45.17 %. Since V_{out} is 8.0 V, half of the output voltage is 4.0 V. Pictured left in Figure 5.19 is V_{cfly} before tuning where the average value is of V_{cfly} 3.76 V. After adjusting the timing intervals, the average V_{cfly} is increased to 3.9 V (pictured right in Figure 5.19). V_{cfly} moving closer to $V_{out}/2$ allows for better tuning of the current waveform which allows the converter to balance batteries in all scenarios (as discussed in section 5.4). The manual FPGA offset allows increases the efficiency from 95.59 % to 95.67 %. Further tuning of the timing intervals is required to move the average of V_{cfly} to half of the output voltage.

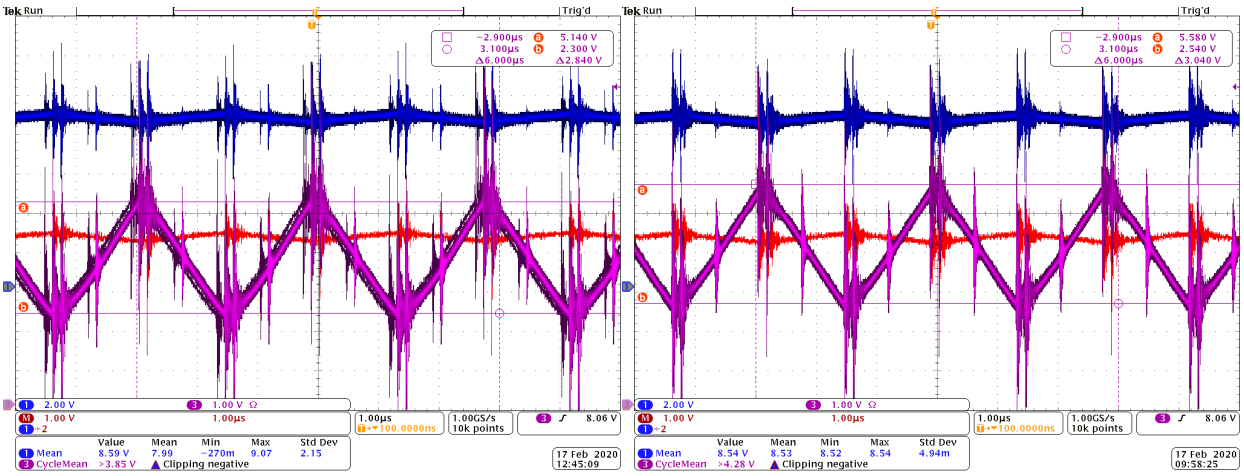

Figure 5.27: $v_{cfly}(t)$ voltage waveform for I_{out} = 5 A at 500 kHz with no tuning (left) and with tuning (right). CH1: V_{out} – CH3: $v_{cfly}(t)$ – CHM: $V_{out}/2$

5.6 Experiment Conclusions

A detailed review of the hardware prototype and component selection is provided. Experimental data gained from the use of a prototype allowed comparison with simulation and analytical loss predictions. Ultimately, the test results of the converter matched the modeled predictions from the average and state space models in both efficiency and balancing current. While the large passives included in initial hardware tests provide low variation in ripple, smaller passives are necessary for the limited area available on mobile electronics. The reason for including large passives in initial testing was to preemptively limit working variables to make possible hardware debugging more manageable. However, the PLECS model accurately includes the full dynamic behavior of the converter even with large ripple. Though Chapter 5 utilized a two-level buck input, the IC design for the input is not optimized in this work. A suggested input stage would be a two or three-level buck, and the one used in Chapter 6 design is the two-level buck with the modulation from

Figure 5.19 (validated in Section 5.3). Comparisons of the model and hardware with large ripple operation are in Chapter 6. With a working prototype and accurate models of the converter like the state space model, the design of the IC is the next step where layout and chip area become important design parameters not previously considered.

Chapter 6 IC Chip Design

6.1 SC Buck Three-Level Boost IC Design

The maximum output current for the SC buck three-level boost is derived based on the inputs given. This sets the bounds of the converter design as explained in Section 6.1.3. Next, the transistors are selected based on voltage rating. LDMOS devices are selected since they provide higher blocking voltage in each technology node. Finally, the passive components are selected accordingly. With the limited volume available for mobile charging circuitry, height is one of the most important factors in passive component selection. A 4.00 mm x 4.00 mm quad-flat no leads (QFN) 28 pin package is selected for the chip (Figure 6.1) to make IC production costs comparable to similar-sized commercial products from Table 1.2. The combined area of on-chip transistors must fit inside the die attach (cavity) area, A_{chip} = 5.76 mm^2 (2.4 x 2.4 mm).

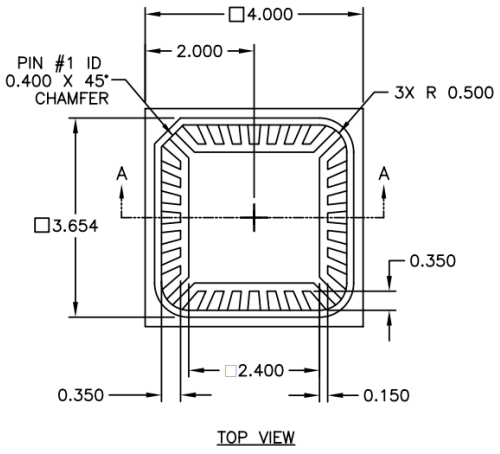

Figure 6.1: QFN package specifications [80].

The IC parameter for A_{chip} is included in Table 6.1 that illustrates the requirements the battery charger IC must meet. Though the SC buck-three level boost stage accommodates a wider operating range of USB inputs, the design process of this work investigates the simultaneous function of three-level boost and the balancing transistors and details a possible method of design on-chip. The maximum charging benefit of the SC three-level boost topology depends on a wide range of factors including the type of input stage (two or three-level buck), modulation, and the parasitics of the LDMOS devices in an available process, and the total area available for all the transistors. Area optimization is needed for the entire SC buck three-level boost to fit on a single IC that meets market standards in terms of chip size and performance. The SC three-level boost IC can potentially be used to implement a three-level buck stage as well (and use a chip for each three-level converter to implement the system), but this work focuses on the SC three-level boost and uses a two-level buck stage utilizing the alternative buck modulation in Figure 5.19.

Table 6.1: Battery Charger Requirements

Converter Parameter	Symbol	Requirement
Input Voltage	V_{in}	5 V < V_{in} < 20 V
Input Current	I_{in}	I_{in} < 3 A
Overall System Efficiency	η	η > 96 %
On-Chip Loss (Power Dissipation)	P_D	P_D < 1 W
On-Chip Area	A_{chip}	A_{chip} < 5.76 mm^2
Balance Current	$I_{balance}$	$I_{balance}$ > 15 mA

6.1.1 Loss Model in Terms of Device Area

The three-level boost converter is evaluated with the loss expressions on Table 6.2. All the loss mechanisms (and the specific device parasitics) depend on the active device area, *A,* as seen in Section 2.4. Though an input with a three-level buck converter is not explored in this work, this three-level buck is evaluated with the similar loss expressions in Table 6.3. All the loss mechanisms (and the specific device parasitics) depend on the area denoted A_1, A_2, A_3, and A_4. The balance transistors have areas A_5 and A_6.

Table 6.2: On-chip Loss Equations for a Three-Level Boost Converter (Transistors Only)

Symbol	Type of Loss	Loss Equation
P_{cond1}	Q_1 Conduction Loss	$I_L^2(1-D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_1}$
P_{cond2}	Q_2 Conduction Loss	$I_L^2(1-D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_2}$
P_{cond3}	Q_3 Conduction Loss	$I_L^2(D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_3}$
P_{cond4}	Q_4 Conduction Loss	$I_L^2(D_{boost})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_4}$
P_{ov}	Overlap Loss	$\frac{1}{4}V_{out}I_L\ Q_{sw,sp}(A_3+A_4)\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
P_{Coss3}	C_{oss3} Loss	$\frac{1}{2}*\left(C_{eq3,Esp}A_3+2C_{eq2,Qsp}A_2-C_{eq2,Esp}A_2\right)\left(\frac{V_{out}}{2}\right)^2 f_s$
P_{Coss4}	C_{oss4} Loss	$\frac{1}{2}*\left(C_{eq4,Esp}A_4+2C_{e1,Qsp}A_1-C_{eq1,Esp}A_1\right)\left(\frac{V_{out}}{2}\right)^2 f_s$
P_{gate}	Gate Loss	$V_{dr}Q_{g,sp}(A_1+A_2+A_3+A_4+A_5+A_6)f_s$

Table 6.3: On-chip Loss Equations for a Potential Three-Level Buck (Transistors Only)

Symbol	Type of Loss	Loss Equation
$P_{condbuck1}$	Q_1 Conduction Loss	$I_L^2(D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_1}$
$P_{condbuck2}$	Q_2 Conduction Loss	$I_L^2(D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_2}$
$P_{condbuck3}$	Q_3 Conduction Loss	$I_L^2(1-D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_3}$
$P_{condbuck4}$	Q_4 Conduction Loss	$I_L^2(1-D_{buck})\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_4}$
P_{ov}	Overlap Loss	$\frac{1}{2}V_{in}I_L\ Q_{sw,sp}(A_1+A_2)\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
$P_{Cossbuck1}$	C_{oss3} Loss	$\frac{1}{2}*\left(C_{eq1,Esp}A_1+2C_{eq4,Qsp}A_4-C_{eq4,Esp}A_4\right)\left(\frac{V_{in}}{2}\right)^2 f_s$
$P_{Cossbuck2}$	C_{oss4} Loss	$\frac{1}{2}*\left(C_{eq2,Esp}A_2+2C_{e3,Qsp}A_3-C_{eq3,Esp}A_3\right)\left(\frac{V_{in}}{2}\right)^2 f_s$
P_{gate}	Gate Loss	$V_{dr}Q_{g,sp}(A_1+A_2+A_3+A_4)f_s$

6.1.2 Transistor Selection

For a given semiconductor fabrication process, device selection may be limited. The potential benefit that the SC buck three-level boost provides is limited by the quality of the transistor devices at its disposal. For example, 7-V V_{ds} devices generally have lower FOM as compared to a 12-V V_{ds} device. If those two devices are the only ones available in a process and the required rating of the device is 8 V, then the design must use the 12 V device. Ideally, an 8-V device leads to better overall efficiency (8-V selection here ignores any safety factor). Lower rated voltage devices achieve a similar R_{sp} as higher voltage rated devices but with less switching power loss.

For the semiconductor CMOS process available for this design, 12-V high performance (HP) nLDMOS devices are chosen from the available transistors in the 180-nm CMOS process used in this work. The 12-V transistors exhibit the smallest parasitics of the devices that sufficiently handle the blocking voltage (V_{out}/2 plus a safety factor for voltage overshoot). The nLDMOS has a highly doped *n*-region connected to its NDD to decrease the drift region resistance. The nLDMOS device referenced to ground is non-isolated, but the top three switches of the three-level boost include an NBL pickup ring to provide isolation. This configuration includes a DPW that lets the bulk tie to the non-ground referenced source and the *p*+ isolation ring (substrate connection) tie to ground (the lowest potential node).

6.1.3 Maximum Output Current

At higher output currents, the overall output voltage increases with more voltage drop across the battery *ESR*. Conduction loss is the major contributor of loss since the inductor current flows through its DCR and through the on-resistance of three transistors at all times in the buck three-

level boost. Limiting D_{boost} limits inductor current and therefore conduction loss. The higher the D_{boost}, the greater the inductor current. To achieve the highest possible output current, D_{boost} is set to zero. The highest possible D_{buck} for whatever buck stage is used occurs at V_{in} = 20 V and yields the highest potential output current. The conversation ratio *M(D)*,

$$M(D) = \frac{I_{in}}{I_{out}}, \tag{6.1}$$

is

$$M(D) = \frac{D_{buck}}{1 - D_{boost}}. \tag{6.2}$$

The limit specification of 3 A for the input current in terms of duty cycle is

$$D_{buck} \frac{I_{out}}{1 - D_{boost}} < 3\ A. \tag{6.3}$$

The previous equations assume an efficiency of 100 %. Using these expressions, the parameters are solved across the range of V_{in} to determine the highest possible output current, $I_{out,max}$ = 6.486 A, to aid passive component selection. Figure 6.2 shows the changing parameters of D_{boost}, D_{buck}, I_L (equal to I_{out}), and V_{out}.

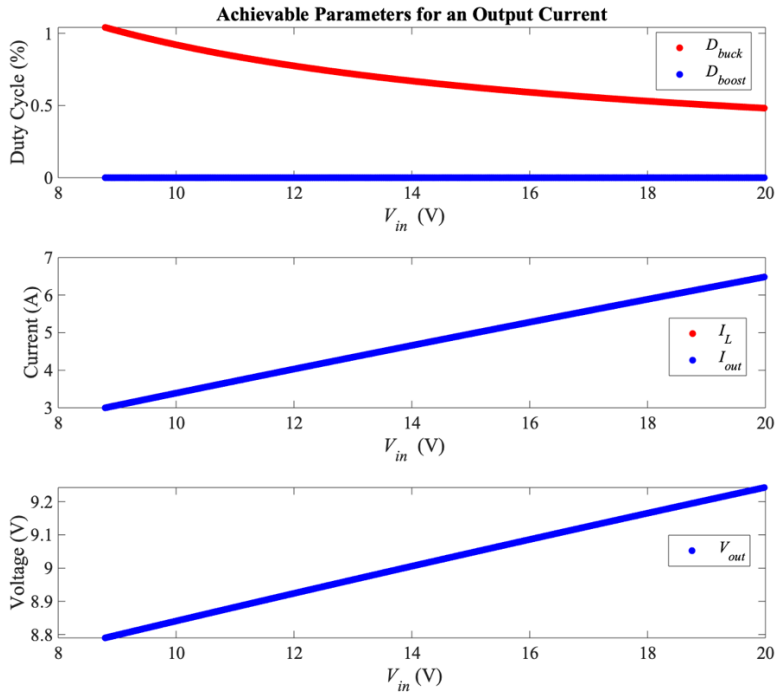

Figure 6.2: The maximum possible output current based on available inputs.

6.1.4 Selection of Flying Capacitance

In equation (3.3), an expression is given for the flying capacitor voltage ripple. However, the ripple should not exceed the minimum nominal voltage of a 4.2 V battery. 3.6 V is chosen here to represent the nominal voltage, so the maximum voltage ripple for this design is

$$\Delta V_{Cfly} \leq 3.6\,V. \tag{6.4}$$

If a different voltage is needed, the following design process is still valid. Because decreasing C_{fly} increases ΔV_{Cfly}, there is a minimum value for C_{fly}. C_{fly} must still be sized sufficiently for large inductor currents as indicated in equation (2.13) as well, and the largest currents occurs when V_{in} is greater than V_{out}. The smaller the C_{fly}, the more balance current that is generated, so minimizing C_{fly} as much as possible improves balancing performance.

The flying capacitor ripple is largest at the peak product of $D_{boost} \cdot I_L$, but there are other more constraining values to determine the minimum C_{fly}. Additionally, because power loss is dominated by conduction current and there is a finite area available in the chip to reduce r_{on}, high D_{boost} is not an option at maximum output current because of the high inductor current. A large value of D_{boost} is given (D_{boost} = 40 %) in a worse-case loss scenario to find the minimum flying capacitor that still sufficiently functions across all operating points. At D_{boost} of 40 %, it is not feasible to size the transistor small enough to keep conduction loss by itself below P_D at I_{out} = 6 A.

C_{fly} can be implemented with a single surface mount component to minimize area on the mobile circuit, and a 0603 size selection is reasonable in mobile devices. The PCB prototype incorporates multiple flying capacitors in parallel to lower the equivalent *ESR*, but this is a luxury that limited space does not always provide. Capacitors of 1 µF and 2.2 µF are available commercially for this size and sufficient voltage rating (greater than $V_{out}/2$). The minimum flying capacitance is solved using equation (2.13) and considers every possible output current. The 350 kHz switching frequency is used to increase I_{Lrms} as a pessimistic scenario.

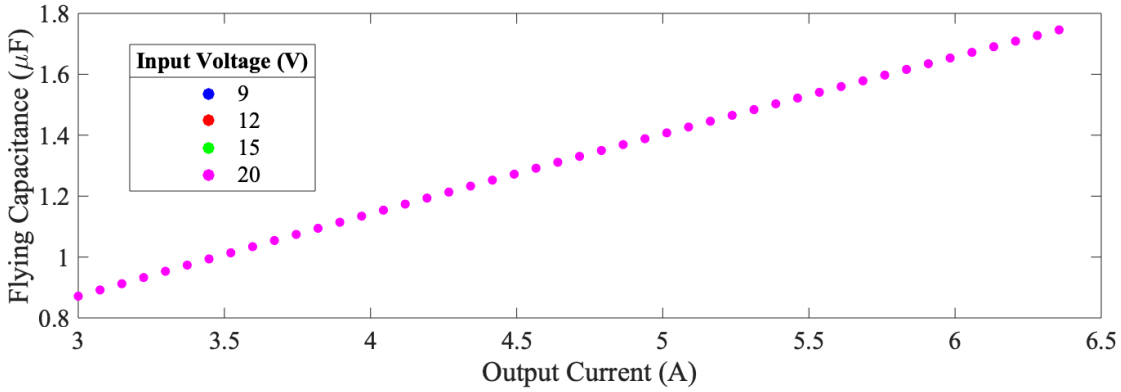

Figure 6.3: Minimum flying capacitance with $f_{s,min}$ = 350 kHz.

Based on Figure 6.3, 2.2 μF is an acceptable selection for operation that always exceeds a switching frequency of 350 kHz. If a smaller C_{fly} is desired, the C_{fly} and f_s product (inversely proportional to the voltage ripple) is examined:

$$C_{fly} \cdot f_s \geq (2.2\ \mu F)(350\ kHz). \tag{6.5}$$

The result is

$$C_{fly} \cdot f_s \geq 0.77\ \mu F \cdot kHz. \tag{6.6}$$

If a 1 μF capacitor is chosen based on Figure 6.4, it would restrict the operational frequency to be greater than 770 kHz as predicted by equation (6.6). Using this product of C_{fly} and f_s is also useful in examining the performance of the total balance current. The goal specified in Table 6.1 is to achieve a balance current greater than 15 mA based on current market balancing products. To demonstrate what this means for battery operation, consider the equations for t_{charge} and $t_{balance}$ in Section 3.2.6. If $t_{balance}$ is less than t_{charge}, the batteries are always balanced before the completion of a charging process. Using an example Q_{max} of 3 Ah, $r_{balance}$ = 1 Ω, a D_{boost} of 25 %, and a charging current of 5 A, example scenarios are addressed in Figure 6.5 of a charge differential (between the two batteries) of 1.0 % and Figure 6.6 with a 0.5% charge differential are examined. In both cases, points that have less than 15 mA of total balance current or a C_{fly} and f_s greater than the maximum are not plotted. With balancing happening simultaneously, the SOC charge differential between batteries should remain small (less than 1.0 %). Figures 6.5 and 6.6 demonstrate the effectiveness of 15 mA of balance current.

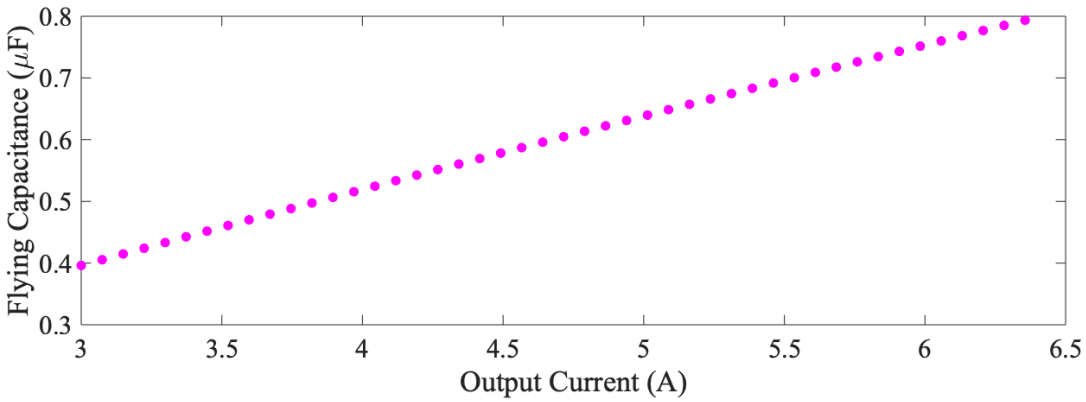

Figure 6.4: Minimum flying capacitance with $f_{s,min}$ = 770 kHz.

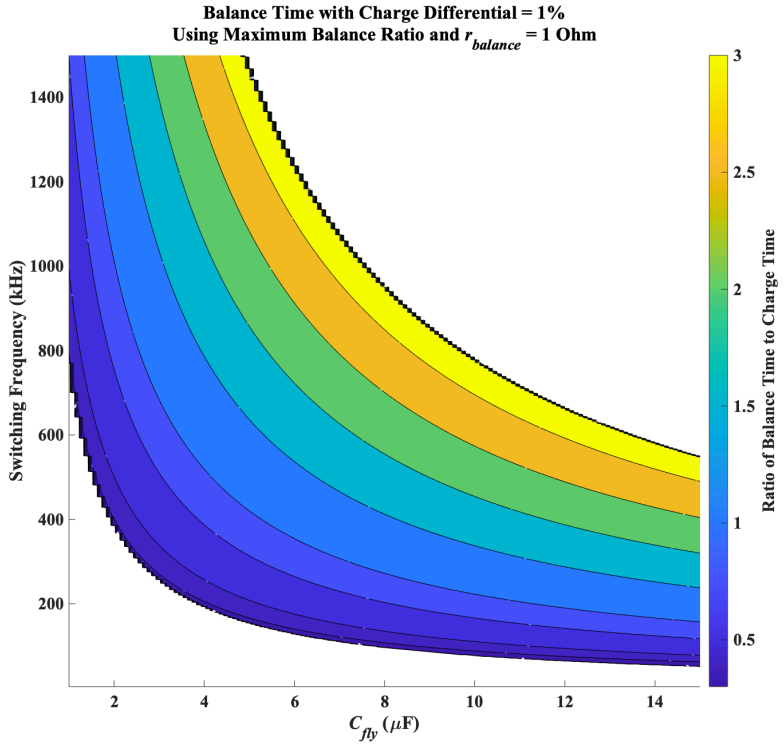

Figure 6.5: Balancing performance with SOC_1 = 41.0 % and SOC_2 = 40.0 %.

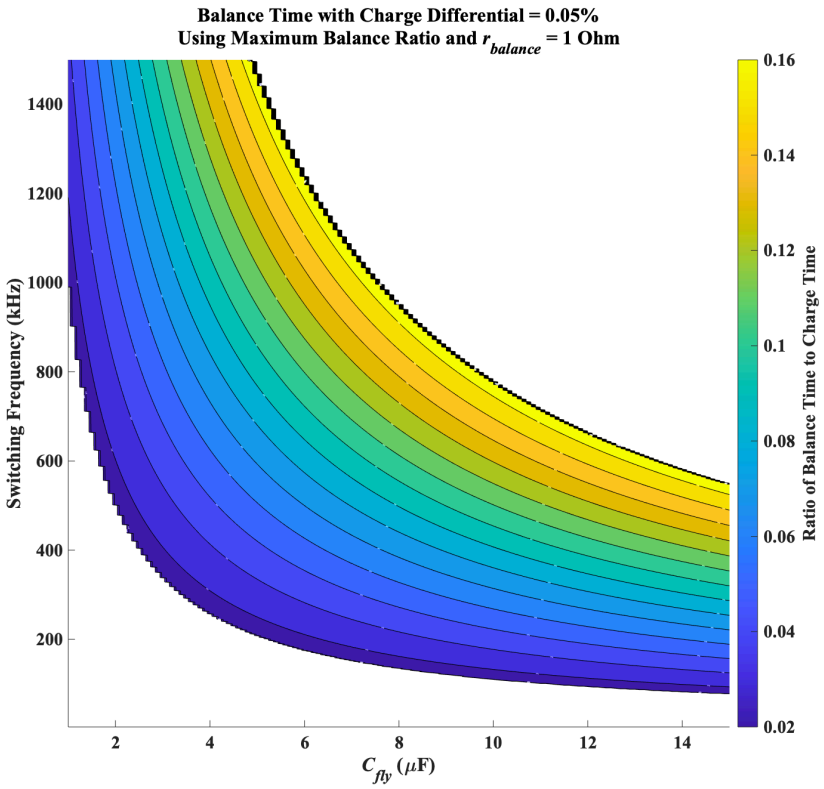

Figure 6.6: Balancing performance with SOC_1 = 41.0 % and SOC_2 = 40.95 %.

With SOC charge differentials as small as 0.5 %, there is flexibility in $r_{balance}$ selection. Though this work does not optimize the value of $r_{balance}$, there exists a $r_{balance}$ that finds the best tradeoff in power efficiency (higher $I_{Balance}$ means more conduction loss) and shorter balancing times. For the rest of the design process in this work, the 2.2 µF is selected to provide a greater range of operating frequencies.

6.1.5 Selection of Inductor

In order to fit inside a mobile device, an inductor height must not exceed 1.4 mm. QFN package ICs are around 1 mm in height, so inductors are one of the largest components on the circuit. The inductor is also limited to a planar area comparable to the IC itself, so the length and width of the

surface mount inductor is at maximum 4.3 mm. When looking at the available inductors that meet the size specifications, there exists a tradeoff between inductance (that reduces the current ripple which decreases conduction loss and provides more flying capacitor stability) and DCR.

It is assumed that the buck stage provides similar current ripple magnitudes as the three-level boost and requires an inductance solved in equation (2.13). Unless the $I_{out,max}$ is lowered so that $D_{boost} > 0$ % (and the double buck modulation is used), theoretically a three-level buck input stage could also achieve this behavior. A two-level buck using the modulation in Figure 5.19 can further reduce the required inductance for a particular ripple but at the unnecessary expense of doubling the switching loss. At maximum charging current, the loss budget is exceeded as the high conduction loss (even with reduced ripple) combines with the doubled switching loss.

The maximum current ripple Δi_{Lmax} for a given L and f_s experienced by the converter occurs at D_{buck} of 25 %. However, a constant ripple is not a constraint for this converter. The maximum I_{Lrms} and I_{Lpk} staying under the saturation threshold are used as boundary parameters instead. Therefore, the ripple is allowed to change as long as those conditions are met. Increasing f_s allows a selection of a smaller L for a given Δi_L but at the expense of increased switching and conduction loss. Therefore, for the given size restrictions, it is preferred to select the largest L that still meets power loss specifications. In Table 6.3, the top four inductors provided by circuit vendors are tabulated.

Table 6.4: List of Possible Inductors for IC

Inductor	Inductance L	DCR	I_{sat}	$I_{L,pk}$ (not a datasheet value)	I_{rms} 40°C Rise
XEL4014-221	220 nH	9.50 mΩ	18.2 A	14.00 A	12.0 A
XEL4014-331	330 nH	12.0 mΩ	14.6 A	11.23 A	9.0 A
XEL4014-561	560 nH	18.4 mΩ	11.6 A	8.92 A	7.5 A
XEL4014-781	780 nH	22.8 mΩ	9.8 A	7.54 A	6.5 A

Additional losses, such as *ACR* and core loss, are not shown in the table above but are considered. For a given frequency, the 780 nH inductor constrains the current ripple to a smaller value. However, the power loss in the inductor is quite high. Even without ripple at I_{out} = 6.486 A, the conduction loss through the DCR alone is approximately 1 W which is quite high for the system efficiency, so the 780 nH inductor is not chosen based on efficiency metrics.

The I_{rms} 40°C rise current value indicates a temperature threshold based on the operating inductor current. Mobile devices are generally designed to limit the temperature of the charging Li-ion batteries between 50-60°C, so it is good practice to select components with good thermal qualities. However, the temperature rise due to power loss is the main design criteria. At higher temperatures, DCR increases (as well as overall loss) and the nominal inductances gets smaller. Finding the inductor conducive to the highest efficiency usually results in the inductor with better thermal qualities.

Inductors are constrained to a peak inductor current I_{Lpk} that is 30 % below the saturation current. I_{Lpk} then is found for each inductor in Table 6.4. Using the average loss model for a three-level buck using the equations in Table 6.3, a frequency and area sweep for three-level buck is examined for the 560 nH inductor in Figure 6.7 and the 330 nH inductor in Figure 6.8. All points that exceed I_{Lpk} are not plotted. In order to keep the peak current below 8.92 A at maximum charge current, a frequency greater than 1 MHz is required for the 560 nH inductor. A similar characteristic occurs with the 330 nH. All plots account for inductance decreasing with L_{nom} with increasing current.

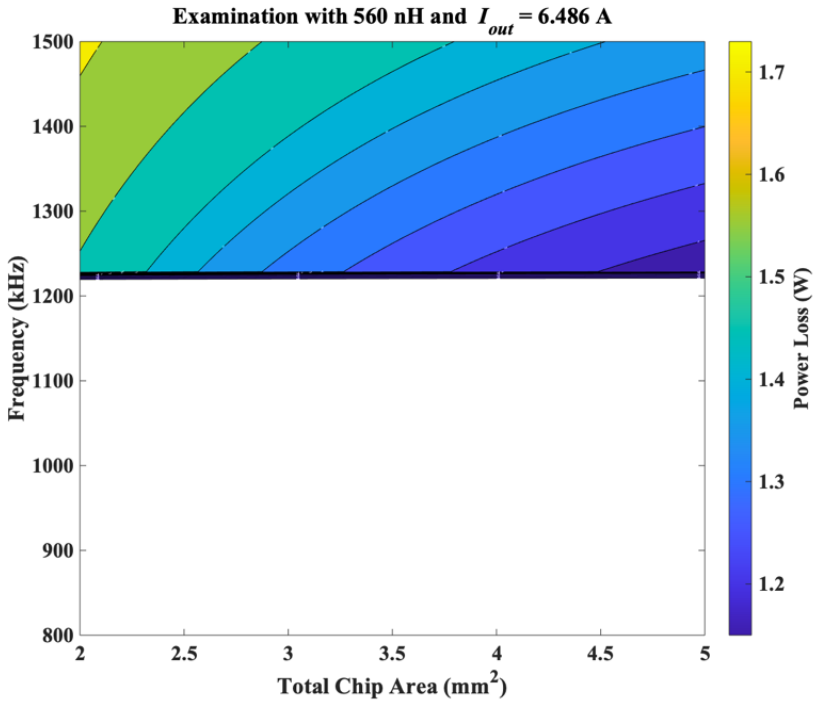

Figure 6.7: Power loss examination for three-level buck with a 560 nH inductor.

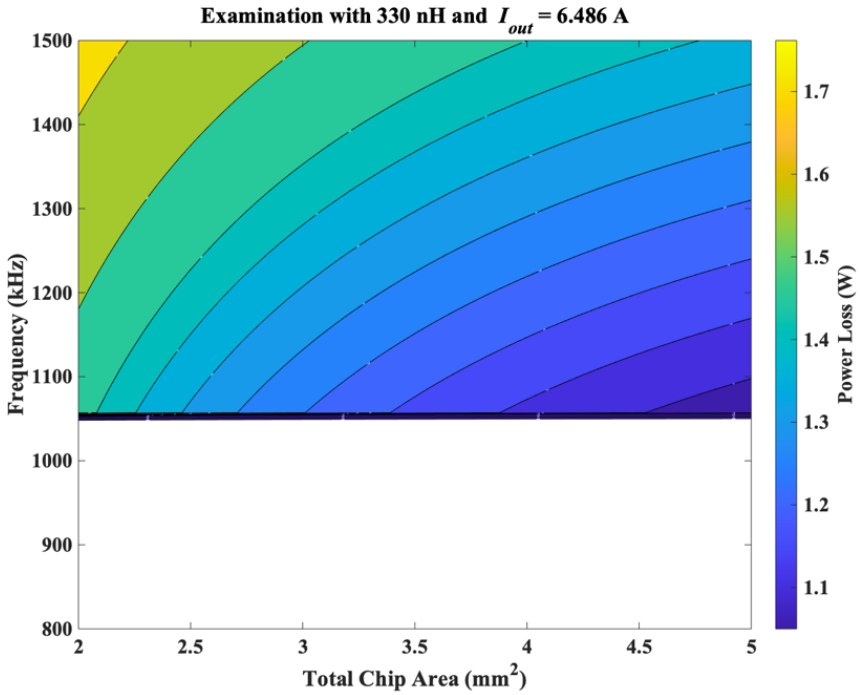

Figure 6.8: Power loss examination for three-level buck with a 330 nH inductor.

The plots conclude 330 nH yields a more efficient maximum charging system than the 560 nH inductor. The maximum *rms* current for the 330 nH inductor is 7.04 A. In Figure 6.9, the three-level buck transistor power loss in an IC using the remaining 220 nH inductor needing examination.

The conclusion of the plots and other data provided by Coilcraft reveals the 330 nH inductor leads to the most efficient operation. It has a sufficiently high saturation current and the second-lowest DCR. The XEL4014-331 also has the lowest core loss above 1 MHz (AC losses calculated according to Coilcraft's online resources). Therefore the 330 nH is chosen for the rest of the design with its maximum *rms* current of is 7.04 A.

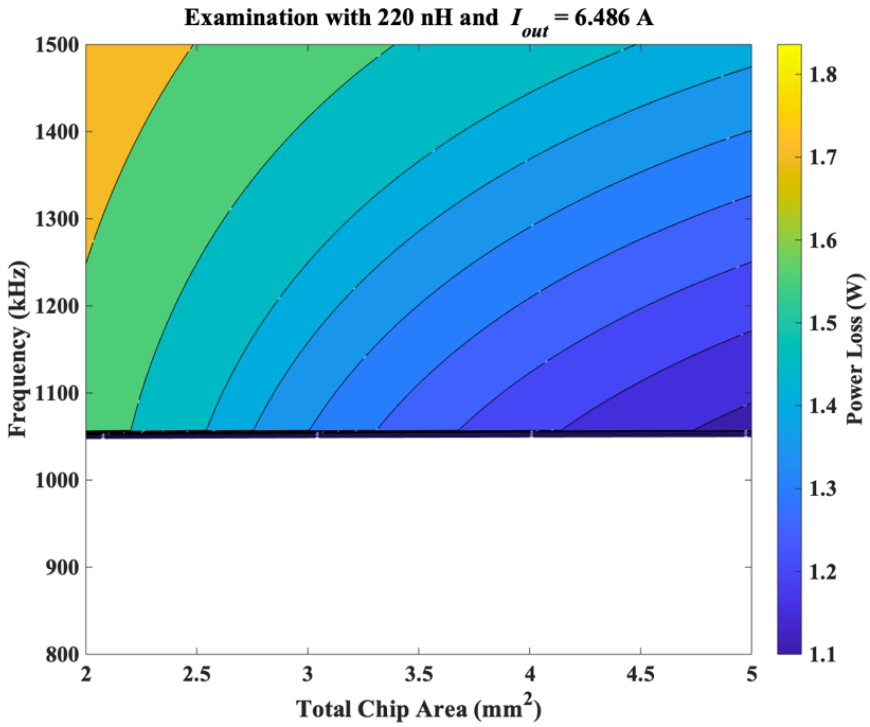

Figure 6.9: Power loss examination for three-level buck with a 220 nH inductor.

As a side-note, inductors with smaller L than 220 nH for the same height available commercially have smaller saturation currents, so this is the best choice from available products for the design. The XEL4014-331 is conducive for achieving a higher charging current while maintaining efficiency requirements. Based on three-level converter operation, only required a fourth of the inductance as compared to two-level versions, so it makes sense that 330 nH offers good performance. Other buck-boost chargers implemented with two-level structures commercially operate around 1 MHz and require inductors around 1 μH. The 330 nH inductor is approximately a fourth of that value as seen in equation (2.11) and (2.12). It should be noted that frequencies higher than 1 MHz are required when operating with maximum charging current because conduction loss needs to be reduced (with smaller current ripple). The converter may operate at lower frequencies to simultaneously balance and charge batteries which is the C_{fly} is chosen for frequencies greater than 350 kHz.

6.1.6 Minimum On-Resistance for Boost IC during Maximum Charging

For the three-level boost in this maximum charging current mode, the high-side transistors are on for most of the entire period (if not the entire duration if the input stage and ripple constraints allow). The only source of loss in the three-level boost stage here is the conduction loss through those two transistors because there is no switching action. If only the three-level boost is placed on IC, then P_D is equivalent to the conduction loss. Again, 1 W is the maximum for the on-chip loss. Boundaries are needed to simplify the design process. If the entire area is distributed between the only Q_3 and Q_4, the two transistors conducting current, the maximum on-resistance allowed is

$$P_D \geq I_{Lrms}^2 \cdot (r_{on3} + r_{on4}). \tag{6.7}$$

For maximum charging current operation, the first input stage utilizes the three-level buck. To achieve maximum charging current with a current limit of 3 A and V_{in} is 20 V. Based on the previous plots in Figure 6.9 with the 330 nH inductor and the ripple constraints based off the I_{sat} (putting the maximum ripple at 4.83 A), the minimum frequency for operation with a buck stage (with the boost's Q_1 and Q_2 on for the entire period) is 1.06 MHz. Using this maximum rms current of 7.06 A, the maximum on-resistance for each high-side device is solved using equation (6.7) as 10.09 mΩ. Based on the 12V LDMOS R_{sp} not disclosed here per TSMC's NDA, the devices are sized with the sufficiently available area to meet this requirement. Therefore, a boundary of maximum on-resistance did not further restrict design parameters (like switching frequency) since enough area is available to size the transistors for a small on-resistance. The balancing operation should be addressed next for another boundary.

6.1.7 Transistor Area Distribution

The operation where balancing occurs simultaneously with charging is limited by loss. Here switching loss is now considered. The maximum ripple to meet this specification for converter operation depends on the output current. The higher the charging current, the less ripple a converter allows. In order to include balancing with the charging operation, the boost stage is activated. Because both switching and conduction transistor parasitics depend on the active area allotted, it is now helpful to investigate what type of performance die area, A_{chip}, can provide.

Not all of A_{chip} is dedicated to the on-chip *n*LDMOS devices. Within that die area cavity, the pad frame with electrostatic discharge (ESD) protection and the seal ring for the IC must also be placed. Fortunately, large transistors sized for high-current applications do not require as extensive of ESD protection as typical for analog and digital applications with small area FETs. The

dimensions of a pad frame depend on the process, and the seal ring within the pad frame is placed a few micrometers (for the 180-nm process) from the die edge to the pad edge as well. The actual area remaining for transistors is called the "core." The core area, A_{core}, is now approximately 5.0 mm^2. Area distribution yields an optimized efficiency and space tradeoff. Using the variable r to represent a percentage of the area, A_{opt}, dedicated to high-side devices (Q_1 and Q_2), there exists an r that leads to the highest efficiency for every operating point. The limited A_{core} available for transistor sizing is one of the challenges associated with integrated high-current applications and is described by

$$A_{opt} = 2A_{high,side}r \; + \; 2A_{low,side}(1 - r) \tag{6.8}$$

6.1.8 Design Methods for Channel Width and Length

Additionally, the layout of the transistor provides additional tools to size MOSFET gate W and L_g according to the design goals of the circuit. For a transistor, the number of "fingers" of the gate poly may be adjusted. For a power transistor, the number of fingers per device might be restricted to increments of two. With nf representing the number of fingers, W_F representing the width per finger, and mi representing the number of devices in parallel, the equivalent $W_{equivalent}$ is

$$W_{equivalent} = nf \cdot W_F \cdot mi. \tag{6.9}$$

In the following figure, each device has $nf = 2$, but the layout determined for the source and drains affect the equivalent values of MOSFET W. In Figure 6.10 with $nf = 2$ and $mi = 1$, the equivalent width is

$$W_{equivalent} = (2) \cdot W_F \cdot (1) = \; 2W_F. \tag{6.10}$$

The technology used for IC design provides a thick layer of copper metal at the top interconnect level. Beneath the top metal is five equally thinner metal layers. The flow of current should be

directed through the top layer to reduce power loss due to the metal resistance. Because the thicker top metal is less resistive, it is crucial for connecting high current nodes. The metallization, the process of interconnecting the active components of an IC with metal conductors [55], needs to provide a low resistance path for current. Figure 6.11 shows two parallel single-finger MOSFETs. To understand the difference between the black and white colored contacts, a cross-sectional view of the transistor and its metallization is needed. A typical approach to metallization in a side-view cross-section of the same switch in Figure 6.11 is in Figure 6.12 with only four metal layers. Each metal bus is connected to a circuit node. Active region contacts that are black are connected to the top metal layer through vias and metallization while the white contacts are not connected to the top layer.

In Figure 6.13, an example for current flow is shown. Current moves through a finger from the top-level metal bus through the lower metal layers (connected by vias) and finally through the active region contacts (colored black). Then the current proceeds through the active layer of the drain. If the proper V_{gs} is applied, current has a path from drain to source. The current then flows to the source bus through the source active layer. This layout strategy is conducive to larger power densities to provide more active area for a given device. Area is a limited resource, especially for ICs in high-current applications. Using the active area more efficiently reduces power loss and the size of the IC package needed for implementation. Other factors, however, also limit the design from utilizing all of A_{core}. Each high voltage LDMOS requires a p+ isolation ring, and those transistors with a source not referenced to ground required an additional NBL n+ buried (pickup) and bulk (backgate) ring.

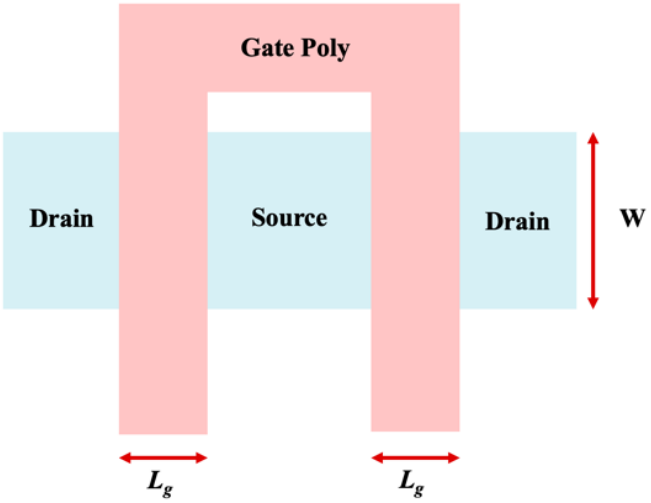

Figure 6.10: Example of a transistor layout providing twice the width.

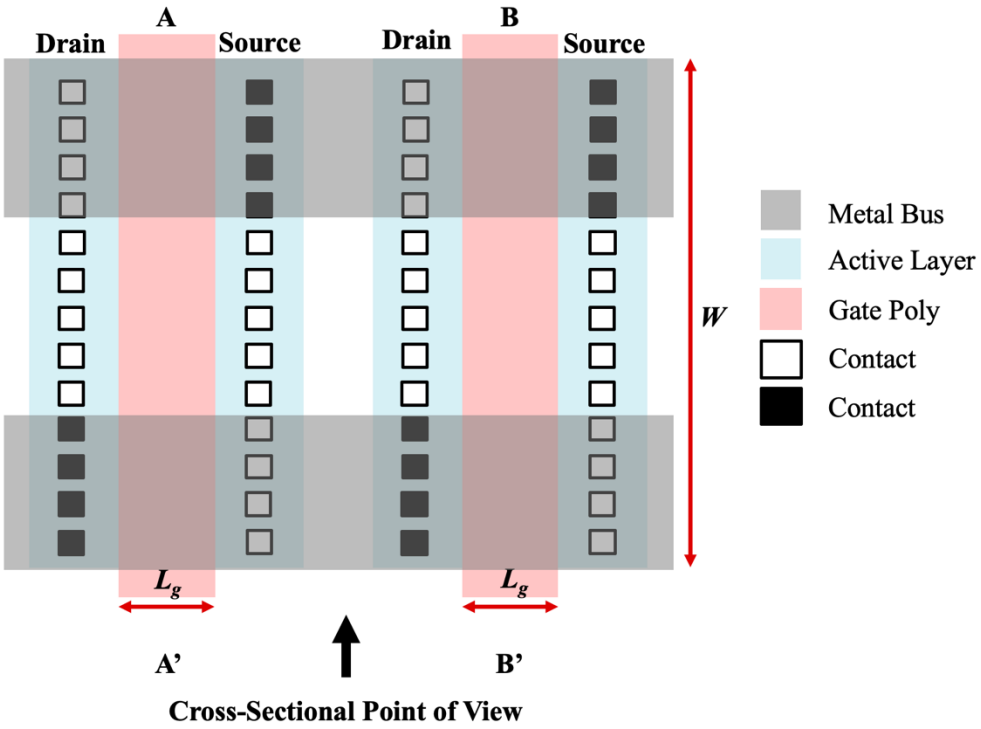

Figure 6.11: Top view two parallel MOSFETs each with a single finger.

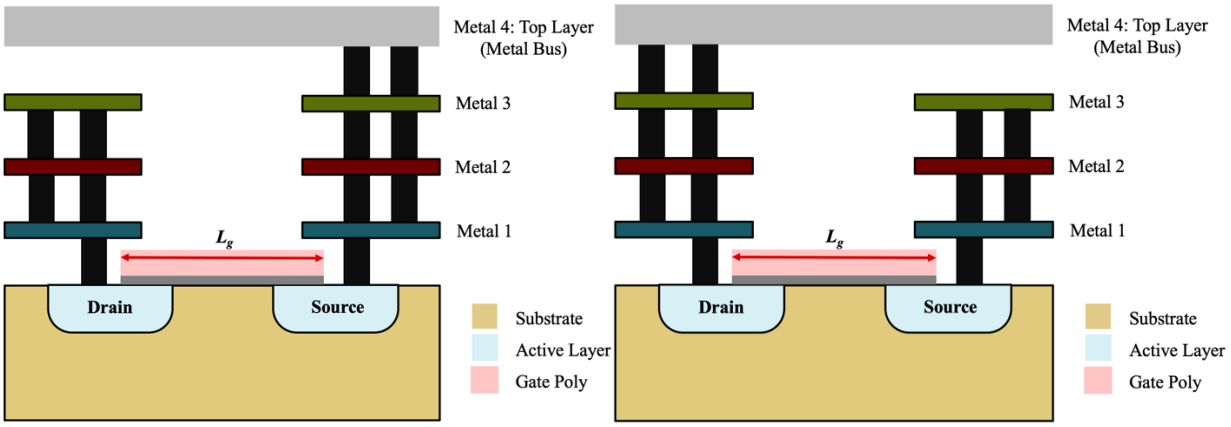

Figure 6.12: Cross-section (side view) of a single finger of the transistor in Figure 6.8. (left): side A or B - (right): side A' or B'

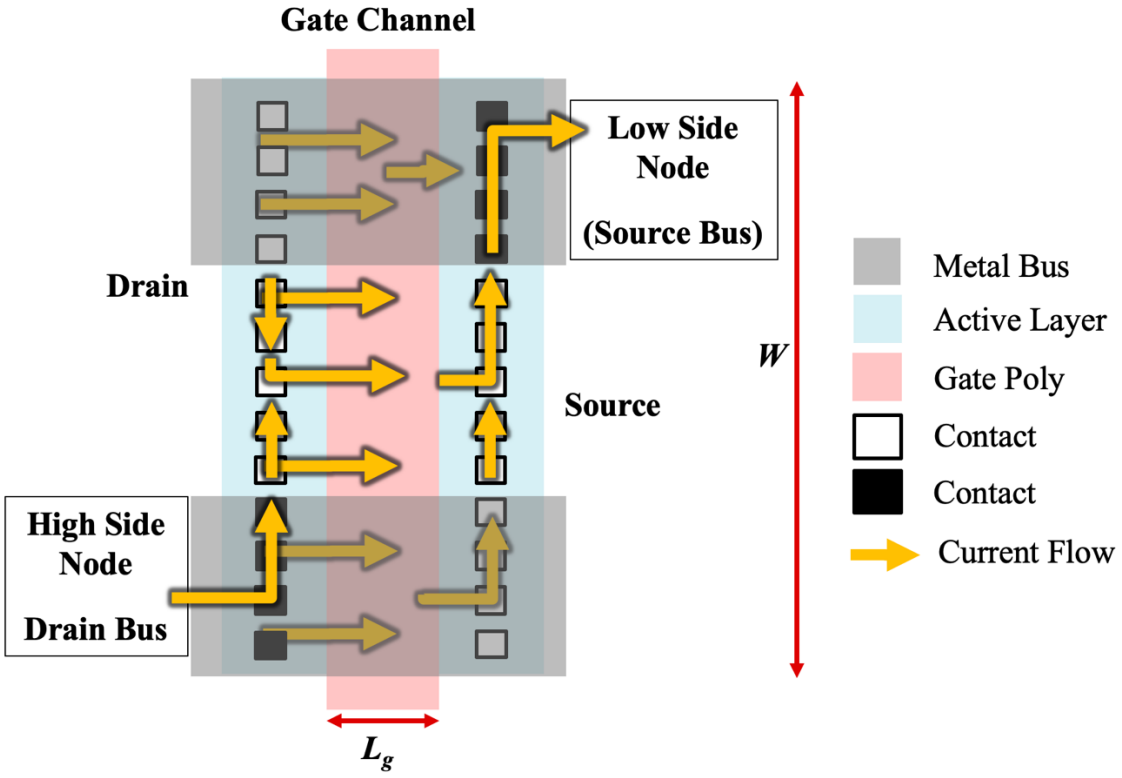

Figure 6.13: Current flow through a transistor's finger (top view).

Figure 6.14 shows a two-finger transistor with all of the isolation rings. This design specifies 300 μm as the maximum distance from any part of NBL pickup ring to the center of the device for a single transistor. The phrase "pickup ring" is generally given to the active area of guard ring encircling the perimeter of the n-type isolation tub required for nLDMOS devices with non-ground referenced source/bulk terminal connections (e.g., high-side switches). The pickup ring enables the designer to electrically tie the isolation tub to the highest potential supply voltage available to the IC, thus helping to mitigate the injection of charge during transients to the substrate (and therefore throughout the chip) while allowing the implementation of high-side switches. For a power electronics IC, the p-type bulk of a high-side FET resides within a *n*-type isolation tub. Design and utilization of pickup rings is vital to power electronics IC design thus helping to mitigate the injection. The spacing of these rings also consumes a large portion of the core region. Around one-third to one-half of the core is actually left for area, *A,* that determines the parasitics of the device. An *A* of 2 mm^2 is adopted for this IC.

Additionally, Figure 6.14 shows an example of how to connect gate fingers with region contacts (colored back) and vias. The region contacts (colored black) connect to the bottom metal layer and vias connect each metal layer used in the gate routing. Because gate poly is highly resistive, each finger is routed to a metal layer to decrease the resistance in the path of the gate signal. To show why this is important, consider the parasitic resistances and capacitances of the IC. For the gate signal V_{gs}, there is resistance through the poly and a C_{gs} that forms an *RC* network. The example *RC* network in Figure 6.15 has the resulting signal (shown in red) from a square wave input after it passes through the *RC* filter in Figure 6.16.

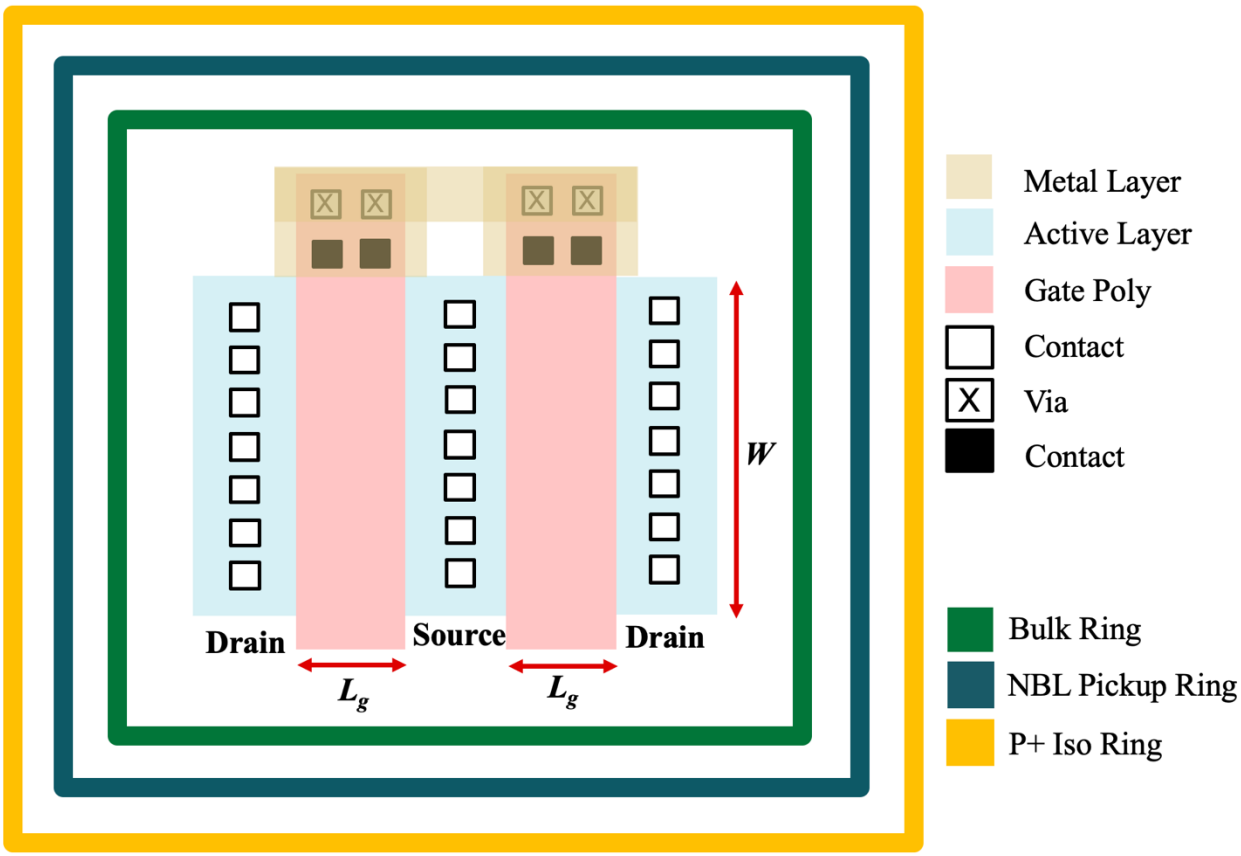

Figure 6.14: Two-finger LDMOS with a butted source and isolation rings.

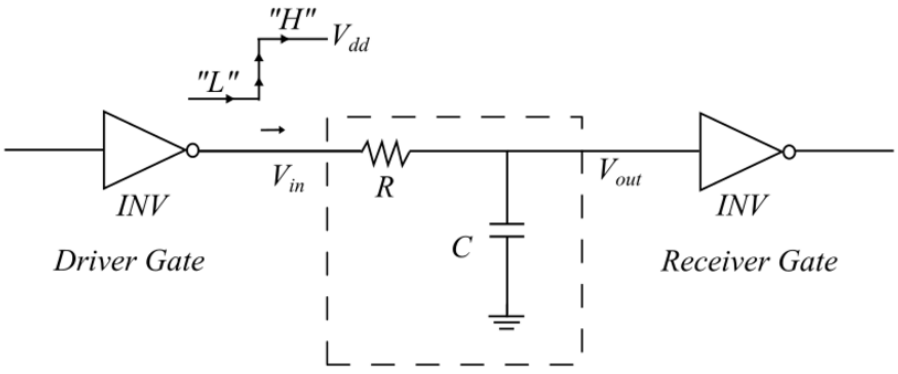

Figure 6.15: *RC* network with a driver and receiver gate.

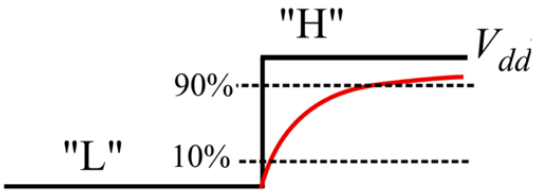

Figure 6.16: Resulting signal from a square wave input through a RC filter.

The time constant, τ, for the RC network as explained in [81] is

$$\tau = RC. \tag{6.12}$$

The time, t_r, it takes for the V_{gs} signal to rise from 10 % to 90 % final value is

$$t_r = 2.2\tau. \tag{6.13}$$

The time, t_{settle}, it takes for the V_{gs} signal to settle to its final value is

$$t_{settle} = 5\tau. \tag{6.14}$$

As the τ increases, the delay for V_{gs} to settle takes a longer duration of time. For a multi-finger FET, a large τ affects the rate at which each transistor is turned ON. Fingers close to the input gate driver will turn on faster than those farther away. Gate channels with a large τ may not even turn-on within the required time interval which affects the transistor's on-resistance and current capability. Overcurrent can damage the device permanently. Therefore, lowering τ as much as possible is important for IC function. A few ways to decrease τ is routing gate signals through metal rather than gate poly, and intelligent placement of the gate signal relative to all the receiving gate channels is crucial as well. This demonstrates that without proper layout, a converter design cannot achieve its potential intended benefit and perhaps not even properly operate on an IC.

Though the package for the IC in this work is based off process availability, other options are available that may provide better performance. Bond wire and package lead resistance are often

comparable with the on-resistance of the power FETs which hinders performance and increases on-chip loss. One solution such as the WLCSP (wafer level chip scale package) is a flip-chip technology. WLCSP routes its signals through a bumped die that is soldered directly onto a circuit pad, so bond wire resistance is removed from the system with only metallization resistance left. An example of WLCSP is provided in [82].

6.2 Operation Designs

There are multiple designs of the proposed SC buck three-level boost to investigate. The maximum charging current at 100 % efficiency has been found, but an additional design should account for the highest possible charging current that simultaneously balances batteries with at least 15 mA of balance current with an acceptable P_D. For the maximum charging current that can simultaneously balance cells under P_D, an optimized ratio, r, for the high-side switch area (A_1 plus A_2), is calculated for every frequency and D_{boost} for the selected C_{fly} and inductor (which considered inductance decreasing from L_{nom} across charging current and frequency) using MATLAB. To take full advantage of the benefits of charging and simultaneous balancing this IC provides, area needs to be optimally distributed between the FETs because of the limit of A_{core}. Operating points that produce less than 15 mA of balance current or that yield an I_{Lrms} or ΔV_{cfly} that exceed maximum limits are not considered in the following plots. Each point of operation uses the optimized area A_{opt} calculated in equation (6.8) based on the loss models for the three-level boost. Once I_{max} is found, the optimized r for that point is kept for the remainder of the scenarios. The point where maximum simultaneous charging and balancing can occur results in highest loss potential (thus needing the optimized area to maximize peak performance).

6.2.1 Current Ripple Evaluation for Buck Three-Level Boost Operation

The buck (two-level with double frequency modulation) and boost are used together in the design verification in Chapter 6. With the buck three-level boost scheme, the inductor current ripple behaves differently as opposed to either just a buck or boost topology. To demonstrate, examples are provided with f_s = 1 MHz, V_{in} = 20 V, and I_{out} = 6 A. In Figure 6.17, D_{buck} (41.3 %) is greater than D_{boost} (10 %) and the double frequency modulation is used (so the D_{buck} is split equally between each half period). The inductor current ripple at that operating point is

$$\Delta i_L = \frac{-V_{out}}{2L} \cdot (0.5 - \frac{D_{buck}}{2}) T_s. \tag{6.15}$$

In Figure 6.18, half of the total D_{buck} (32.3 %) is less than D_{boost} (30 %) with the double frequency modulation used. Here the inductor current ripple calculation is not as straightforward. Because the inductor current begins to fall after $D_{buck/2} \cdot T_s$ is reached, equation (6.15) cannot be used. Ideally, the ripple could be calculated without a sub-circuit where V_{cfly} affects the inductor voltage, V_L. An approximation can be made that V_{cfly} is averaged to $V_{out}/2$. Then the inductor current ripple during the time duration $D_{buck/2} \cdot T_s$ is

$$\Delta i_L = \frac{V_{in} - \frac{V_{out}}{2}}{2L} \cdot (\frac{D_{buck}}{2}) T_s. \tag{6.16}$$

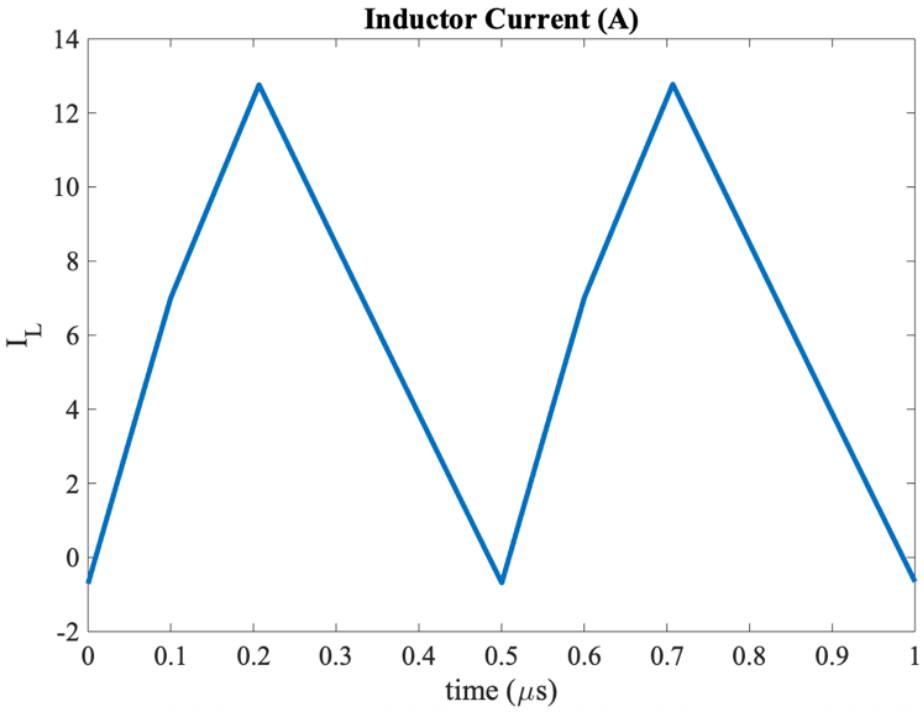

Figure 6.17: Example of $D_{buck/2} > D_{boost}$ for double buck modulation.

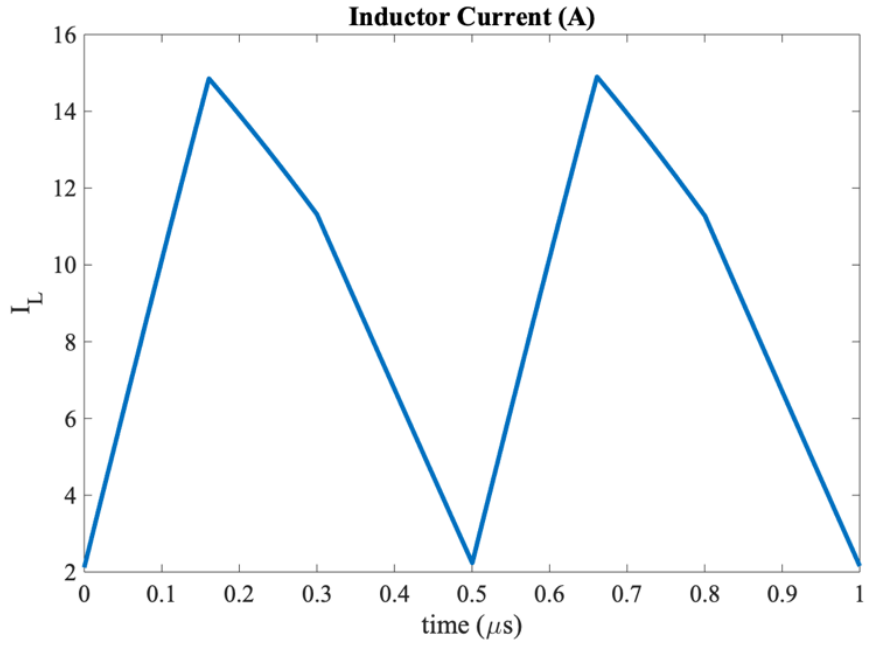

Figure 6.18: Example of $D_{buck/2} < D_{boost}$ for double buck modulation.

If a three-level buck converter is placed at the input, a similar current ripple evaluation is conducted. When D_{boost} = 0, the range of D_{buck} that takes place for every output current is shown in Figure 6.19. When the charging current rises above 6 A, D_{buck} is greater than 50 %. As D_{boost} increases for balancing operation capability, D_{buck} moves to a smaller ratio comparatively per output current. If D_{boost} is at least 10 %, then the D_{buck} remains below 50 % for output currents greater than 4 A. Using this approach, the current slopes can be re-calculated. If D_{buck} is greater than 50 %, the following equations would not apply. When D_{boost} is less than Dbuck, the ripple is

$$\Delta i_L = \frac{-V_{out}}{2L} \cdot (0.5 - D_{buck}) T_s. \tag{6.17}$$

When D_{boost} is greater than Dbuck, the ripple is

$$\Delta i_L = \frac{V_{in} - \frac{V_{out}}{2}}{2L} \cdot (D_{buck}) T_s. \tag{6.18}$$

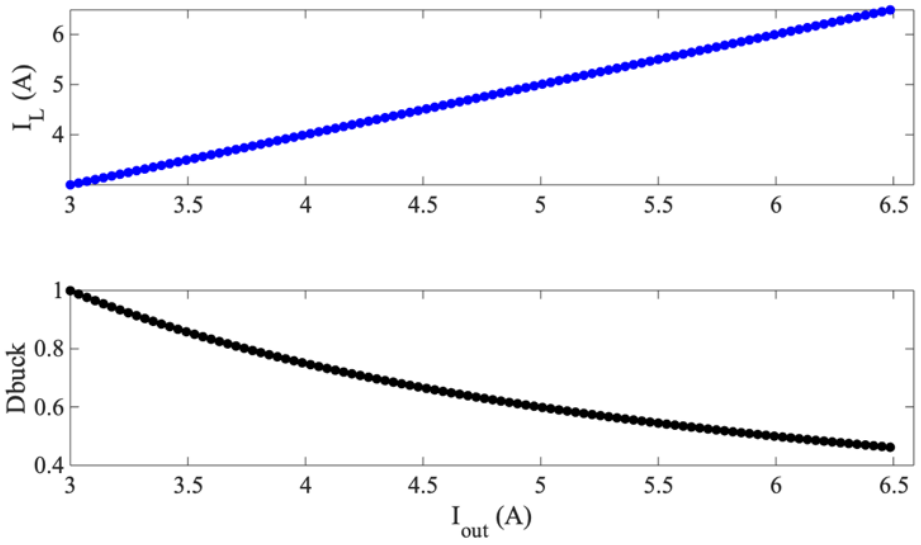

Figure 6.19: D_{buck} for every output current load when D_{boost} is set to zero.

Throughout the analysis, D_{boost} can be no greater than approximately 31.5 % to prevent I_{Lpk} from being reached. Because three-level buck hardware is not implemented, the maximum charging current while simultaneously balancing moves forward with the two-level buck using modulation from Figure 5.19.

6.2.2 Hardware Verification of Loss Models

Lowering the balance resistance increases balance current, though this begins to lower efficiency. Frequency and D_{boost} are also other parameters that affect balancing but at the trade-off of efficiency. Optimization is required to find this maximum charging current point that has a P_D of less than 1 W. Before this is done, analysis of hardware and current loss models is re-examined with small current ripple. Refining the models allows for possible optimization later.

The operating point in Table 6.5 is tested with the hardware prototype from Chapter 5 (using GaN FETs), the average model, and the state space representation of the converter. Waveforms for the hardware prototype and state space simulation are shown in Figure 6.20, 6.21, 6.22, and 6.23. While C_{fly} is 2.2 µF, the only inductor available was the 200 nH XEL4030-201MEC. This inductor has a low 2.15 mΩ DCR and a saturation current of 22 A, but it has a height of 3.2 mm (too high for use in mobile devices). The electronic load is set to r_{bat1} = 0.9981 Ω (V_{bat1} = 4.19 V plus the *ESR* drop) and r_{bat1} = 0.9983 Ω (V_{bat2} = 4.2 V plus the *ESR* drop).

Table 6.5: Results for I_{out} = 4.5 A at 800 kHz (D_{boost} = 25 % , D_{buck} = 35 %)

	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	P_{in} (W)	P_{out} (W)	*Efficiency* (%)	*Balance Current* (mA)	I_{bat1} (A)	I_{bat2} (A)
Experiment	20.0	2.225	9.09	4.5488	44.5	41.49	93.24	25.1	4.557	4.540
Average Model	20.0	2.174	9.00	4.50	43.48	40.95	94.18	28.0	6.041	5.959
State Space	20.0	2.179	9.03	4.525	43.69	40.85	93.25	29.6	4.538	4.501

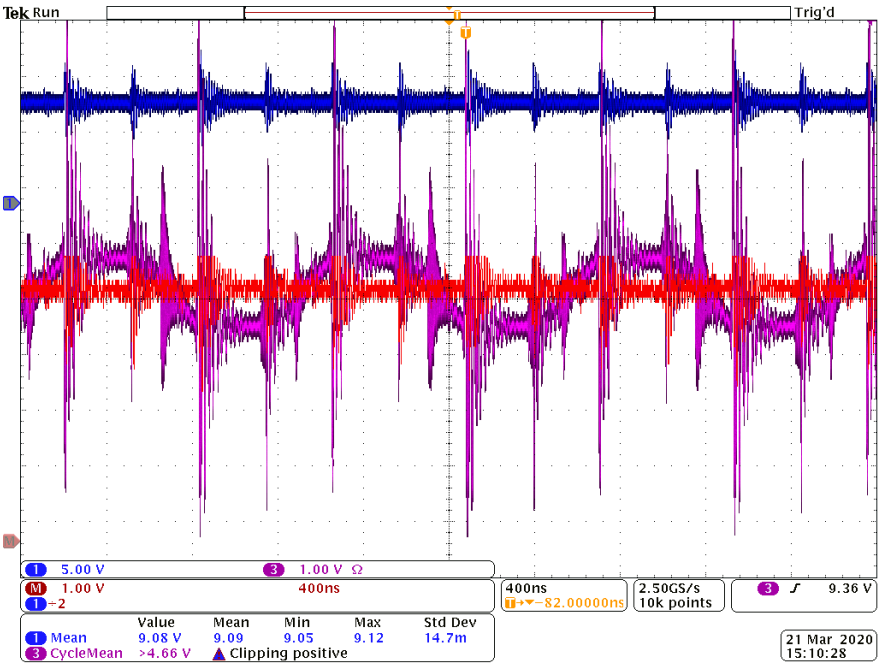

Figure 6.20: $v_{cfly}(t)$ waveform for I_{out} = 4.5 A at 800 kHz. CH1: V_{out} – CH3: $v_{cfly}(t)$ – CHM: $V_{out}/2$

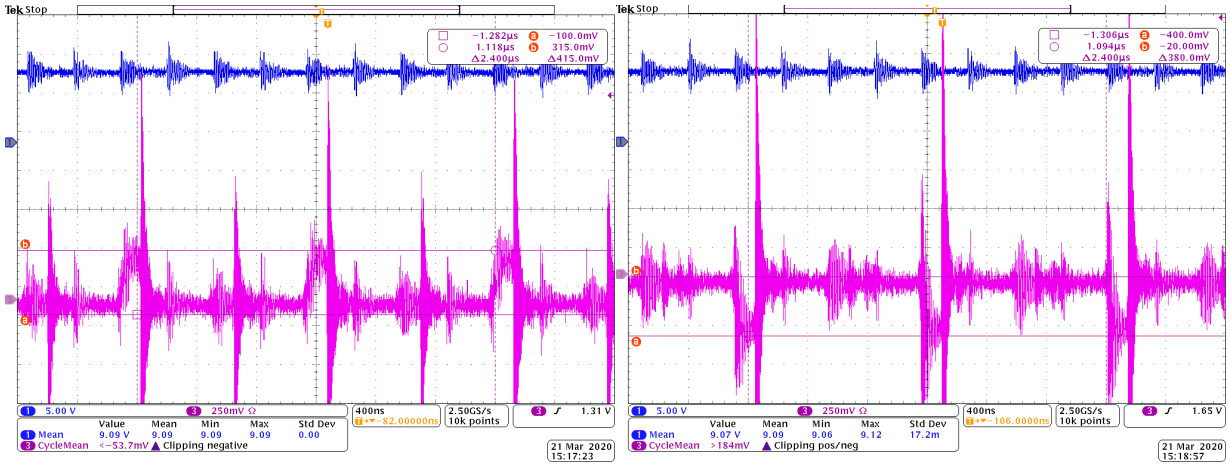

Figure 6.21: Balancing waveforms for I_{out} = 4.5 A at 800 kHz. (left) CH1: V_{out} – CH3: V_{bal6} – (right) CH1: V_{out} – CH3: V_{bal5}

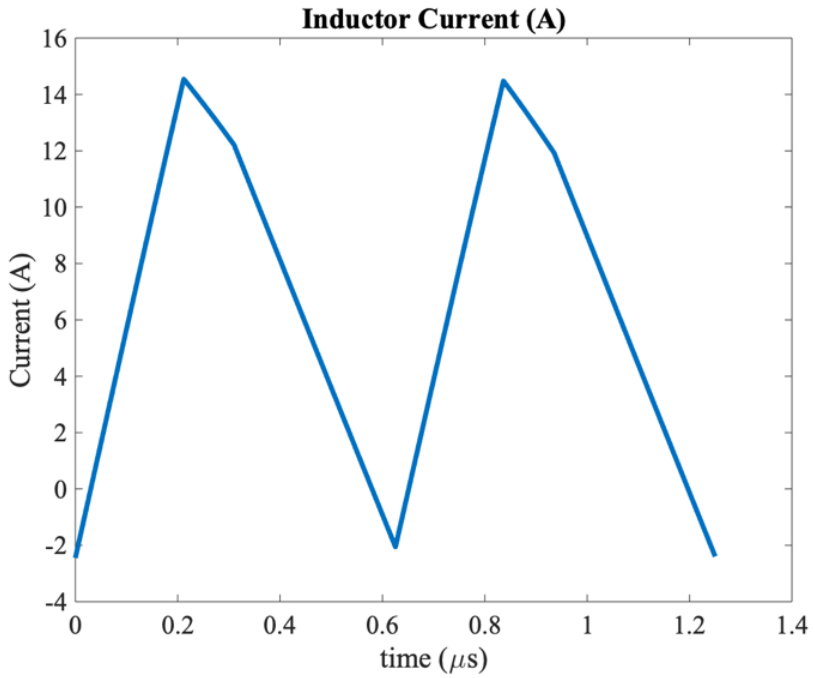

Figure 6.22: State space inductor current waveforms for I_{out} = 4.5 A at 800 kHz.

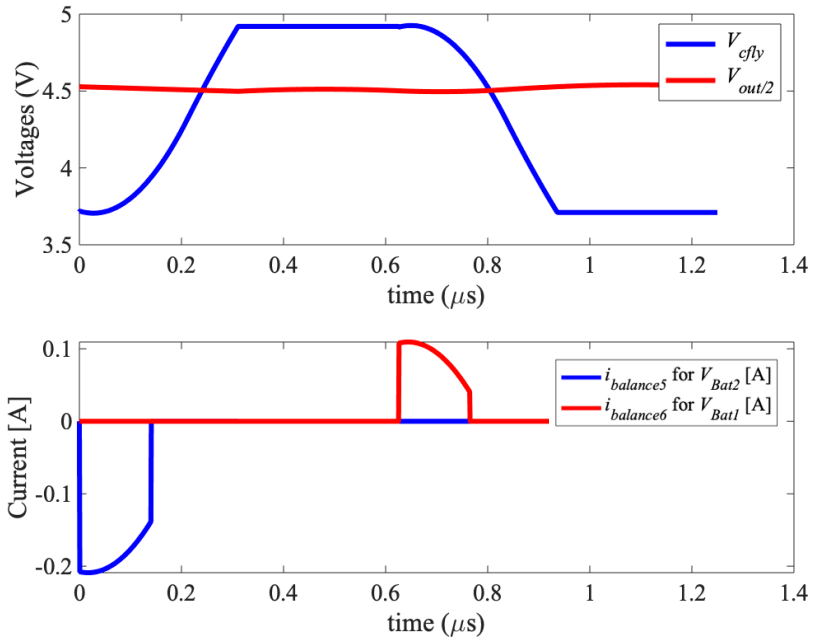

Figure 6.23: State space flying capacitor voltage and balance current waveforms for I_{out} = 4.5 A at 800 kHz.

Both loss models (state space and average) approximate the hardware well. However, this is because of an adjustment to the average model. As seen in the previous balancing figures, balance current no longer takes the shape of a triangle. The approximation in equation (5.1) is no longer valid. Adjusting the balance current characteristic approximation for that of a rectangle yields the expected balance current which is done with

$$I_{balance} = \left(\frac{\frac{I_L}{2 \cdot C_{Fly} \cdot fs} \cdot D_{Boost}}{r_{balance}} \cdot D_{Boost} \cdot 45\ \% \right) \cdot 2. \tag{6.19}$$

While this helps provide fast estimation with the average model, state space analysis must now be utilized to more accurately characterize the model.

The experimental V_{cfly} experiences a peak-to-peak ripple of about 1.2 V. Though V_{cfly} is close to $V_{out}/2$, state space reports a differential of 150 mV between V_{cfly} and the $V_{out}/2$ which is similar

to but slightly larger than the prototype result. The PCB layout is designed with a long path between the positive and negative connection for the inductor. This leads to larger parasitic inductances than other circuits loops that are intentionally minimized further. More parasitic inductance at the switch node allows for greater overall power inductance and decreases ripple, so the prototype L is larger than 200 nH. To understand the waveform of $v_{cfly}(t)$, consider the resonance between C_{fly} and L during the intervals that charge/discharge C_{fly}. The resonant frequency f_0 [27] for the LC network is

$$f_0 = \frac{1}{2\pi\sqrt{C_{fly} \cdot L}}. \tag{6.20}$$

The value for f_0 in Chapter 5 was 112 kHz using the larger passives. Using C_{fly} of 2.2 µF and an inductor of 330 nH (200 nH is used in hardware validation), f_0 becomes 186.8 kHz (or 240 kHz with a 200 nH inductor). Therefore, as operating frequency gets closer to f_0, more resonant behavior is experienced by V_{cfly}. Using as large an inductor as possible allows a smaller f_0. The state space model examines the $v_{cfly}(t)$ waveform with different T_s. The operating conditions other than the frequency are used from Table 6.5. The following two figures (6.24 and 6.25) show four plots of $v_{cfly}(t)$ at f_s of 2 MHz, 1.2 MHz, 400 kHz, and f_0 = 240 kHz. Figure 6.25 shows the fully resonant behavior of $v_{cfly}(t)$, and the ripple on C_{fly} becomes large at this small of a frequency. This resonant behavior actually increases the actual $I_{Balance}$. Future work is needed to optimize C_{fly} against the minimum in equation (2.13) and f_s to increase balance performance. Increasing f_0 is necessary then.

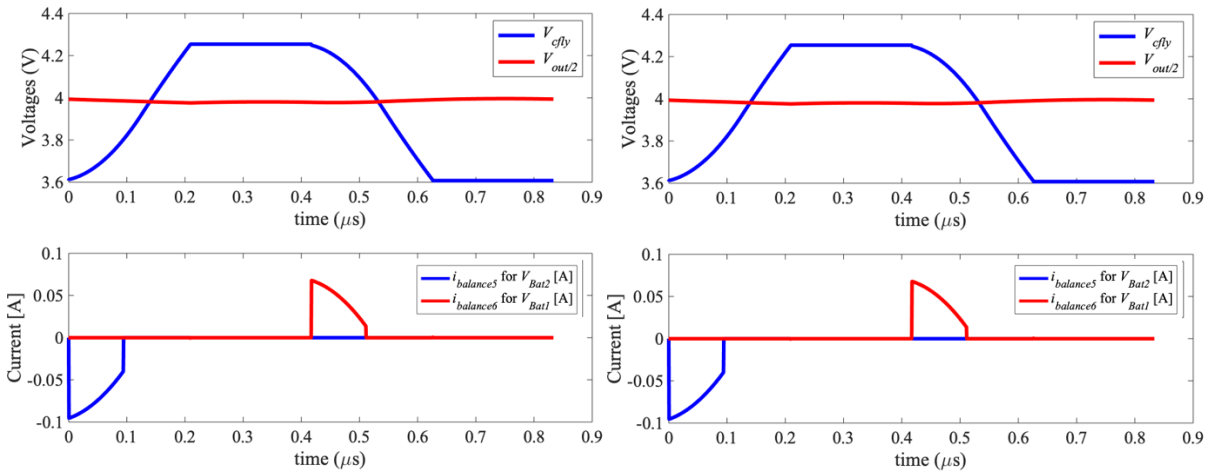

Figure 6.24: $v_{cfly}(t)$ and balance current waveforms for I_{out} = 4.5 A at 2 MHz (left) and at 1.2 MHz (right).

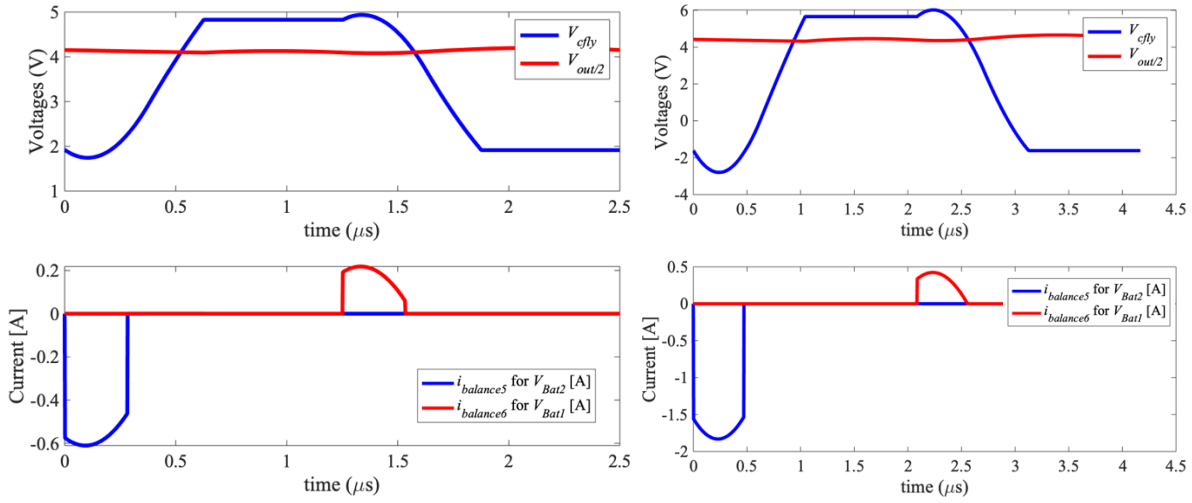

Figure 6.25: $v_{cfly}(t)$ and balance current waveforms for I_{out} = 4.5 A at 400 kHz (left) and at f_0 = 240 kHz (right).

For the operation in Table 6.6, τ_L is still around 10 μs but T_s is 2 μs, so f_s is just over double of f_0. The non-uniform behavior of the slope of V_{cfly} is therefore more noticeable at 500 kHz than the converter in Table 6.5. The balance currents are smaller because I_{out} = 1.5 A with V_{in} = 5 V. Other parameters are D_{buck} (96 %), D_{boost} (46.38 %), r_{bat1} = 2.864 Ω (V_{bat1} = 4.19 V plus the *ESR* drop), and r_{bat1} = 2.865 Ω (V_{bat2} = 4.2 V plus the *ESR* drop). The waveforms for $v_{cfly}(t)$ are shown in Figure 6.26, and the voltage across the balance resistors is shown in Figure 6.27. State space inductor current, flying capacitor voltage, and balance current waveforms for I_{out} = 1.5 A at switching frequency of 500 kHz are shown in Figure 6.28 and Figure 6.29 respectively. Table 6.6 displays a power efficiency variance between hardware and loss models. Normally, further testing could pin-point the reason for this variance. However, the balance current behavior and waveform characteristics of state space still follow hardware results well. It is possible that the efficiency variance is due to a large parasitic resistance introduced to the circuit when a small inductor (smaller than the pad) is soldered onto a pad through the use of a large solder blob. Solder has a higher resistivity, so a poor inductor connection to the pads (increasing resistance of inductor path) is a possible culprit.

Table 6.6: Results for I_{out} = 1.5 A at 500 kHz (D_{boost} = 46.38 % , D_{buck} = 96 %)

	V_{in} (V)	I_{in} (A)	V_{out} (V)	I_{out} (A)	P_{in} (W)	P_{out} (W)	*Efficiency* (%)	*Balance Current* (mA)	I_{bat1} (A)	I_{bat2} (A)
Experiment	5.0	2.805	8.72	1.52	14.03	13.2	94.36	36.5	1.536	1.450
Average Model	5.0	2.710	8.80	1.50	13.55	13.20	97.42	35.9	1.518	1.482
State Space	5.0	2.910	9.00	1.51	14.55	14.14	97.18	37.3	1.568	1.531

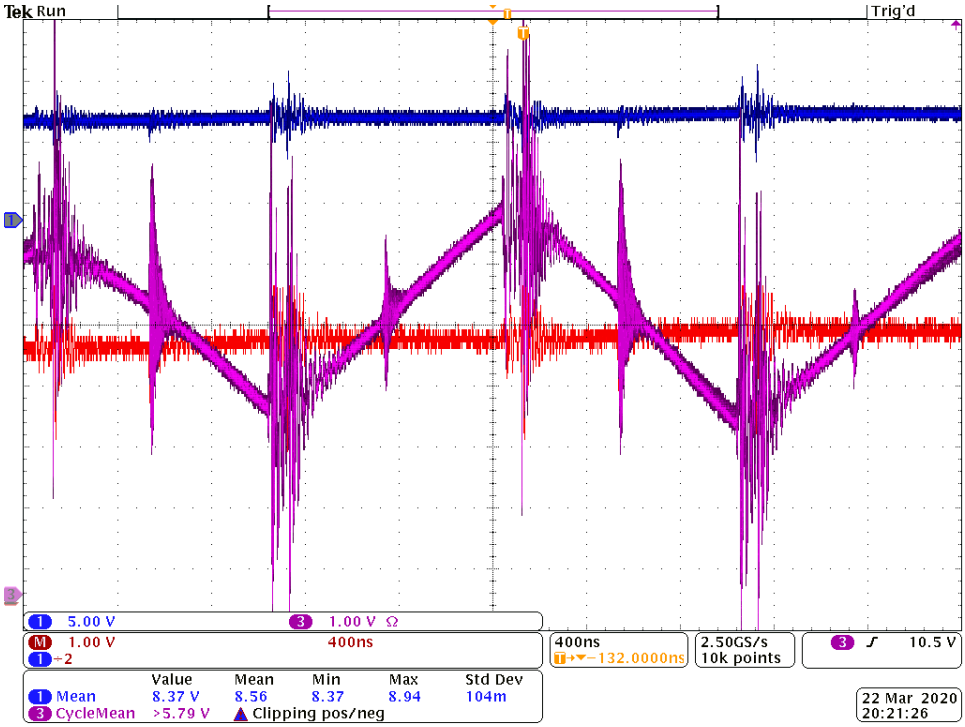

Figure 6.26: $v_{cfly}(t)$ waveform for I_{out} = 1.5 A at 500 kHz. CH1: V_{out} – CH3: $v_{cfly}(t)$ - CHM: $V_{out}/2$

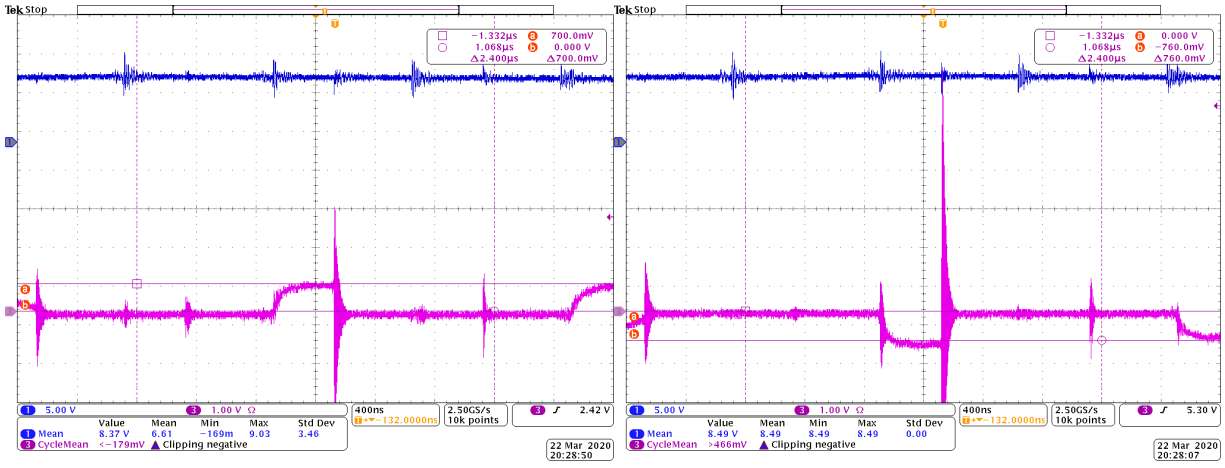

Figure 6.27: Balancing waveforms for I_{out} = 1.5 A at 500 kHz. (left) CH1: V_{out} – CH3: V_{bal6} – (right) CH1: V_{out} – CH3: V_{bal5}

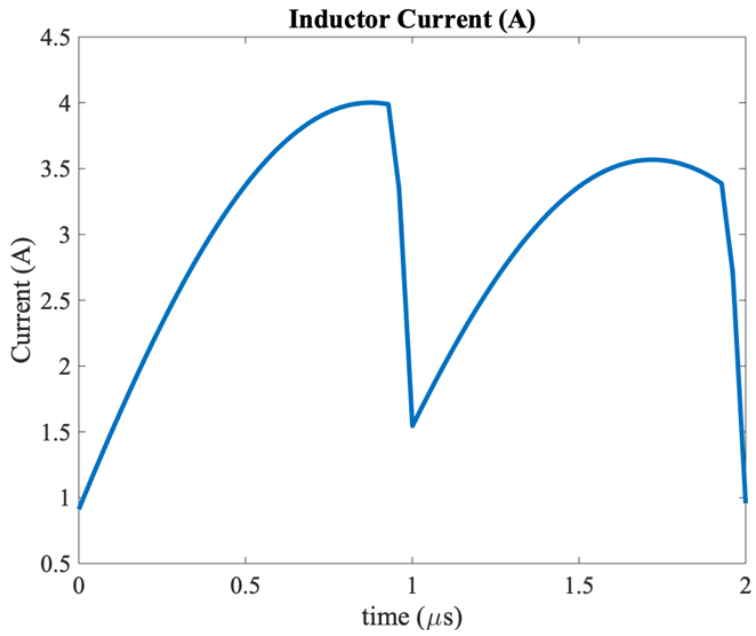

Figure 6.28: State space inductor current waveform for I_{out} = 1.5 A at 500 kHz.

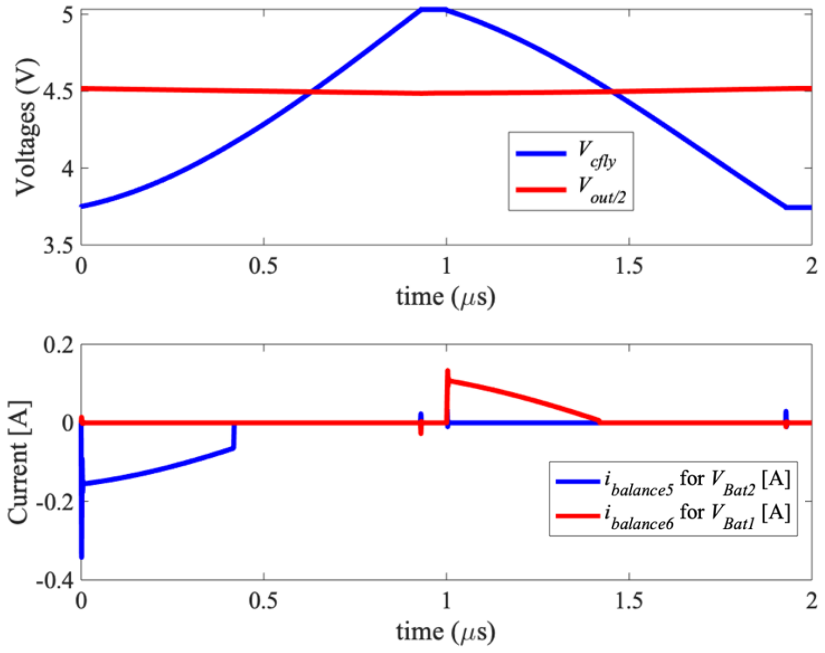

Figure 6.29: State space $v_{cfly}(t)$ and balance current waveforms for I_{out} = 1.5 A at 500 kHz.

The average model is able to predict balance current fairly well because of the shape of the waveform, but state space is the model that follows the true behavior of the waveform without having to adjust any parts of the model.

6.2.3 Maximum Operation Point of Simultaneous Charging and Balancing

Now that the both models have shown the ability to estimate operation of the SC buck three-level boost, these models are used to find the maximum charging current that can also simultaneously balance batteries. The average model can quickly sweep through thousands of operating points within a few seconds, so the average model is used to survey a wide range of points to narrow the search. The state space model, which is much faster than other transient simulators but takes time to sweep through this many operating points, is then used to examine the narrowed range. The converter analyzed is the SC buck three-level boost with the modulation from Figure 5.19, the inductor of 330 nH, and a C_{fly} of 2.2 µF. The plots do not record data where the maximums of I_{Lrms} current, the ΔV_{Cfly}, or the I_{Lpk} are exceeded or if less than 15 mA of $I_{Balance}$ is achieved. The optimized ratio, r, is calculated for every frequency and D_{boost}. A_{core} of 2 mm^2 is used.

As Figure 6.30 indicates, there is not a single point for I_{out} = 6.0 A that has a P_{loss} less than 1 W. The same is true for I_{out} = 5.25 A in Figure 6.31. For balancing functionality to take place with the available area for the IC package described in Section 6.1.7, it is necessary to move to an operating point that provides a lower charging current per P_D constraints. Figure 6.32 shows the power loss examination at I_{out} = 5.0 A. The balance current examination using the average model at I_{out} = 5.0 A is shown in Figure 6.33. Only balance current measurements that exceed 15 mA are plotted.

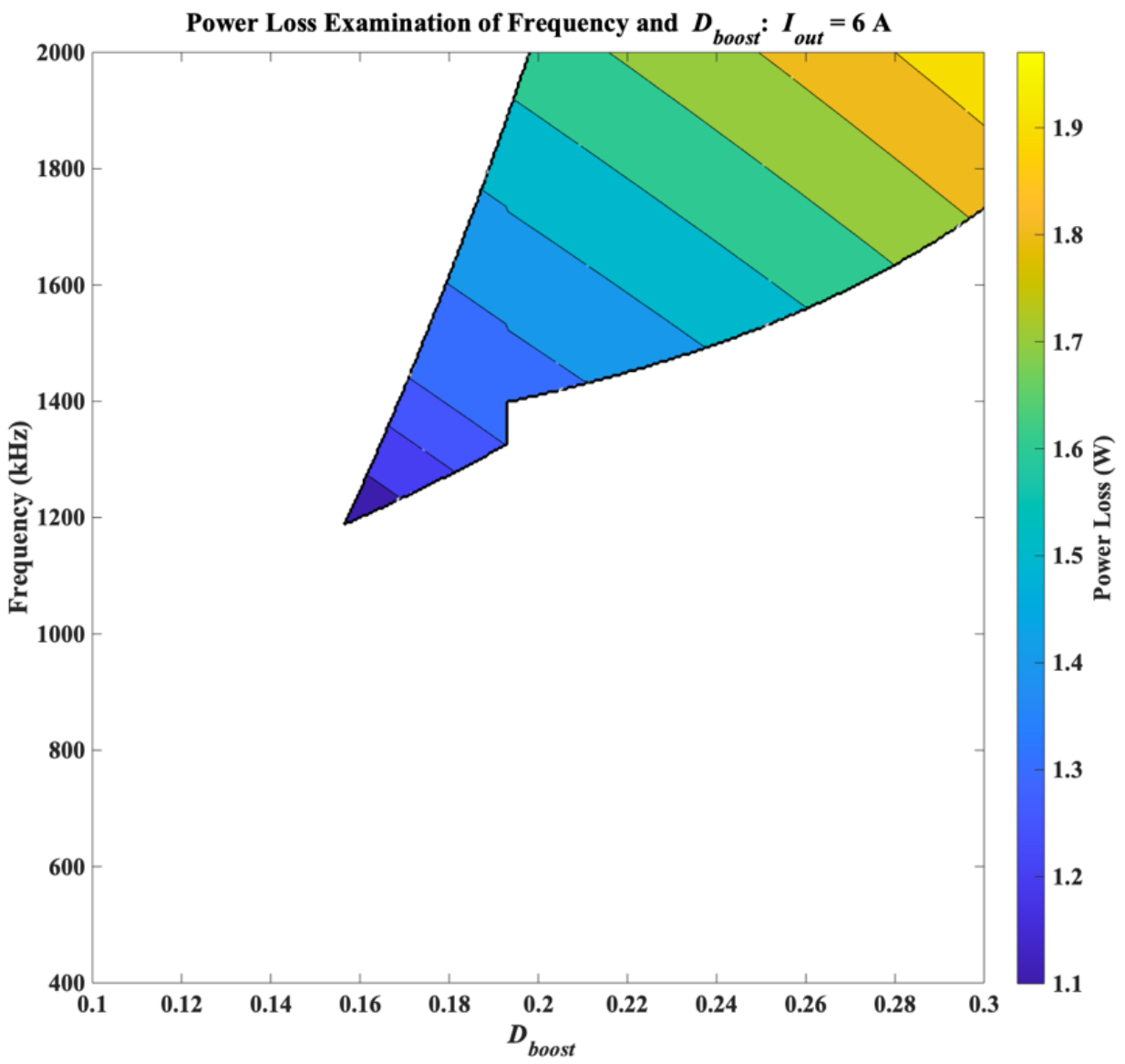

Figure 6.30: Power loss examination at I_{out} = 6.0 A

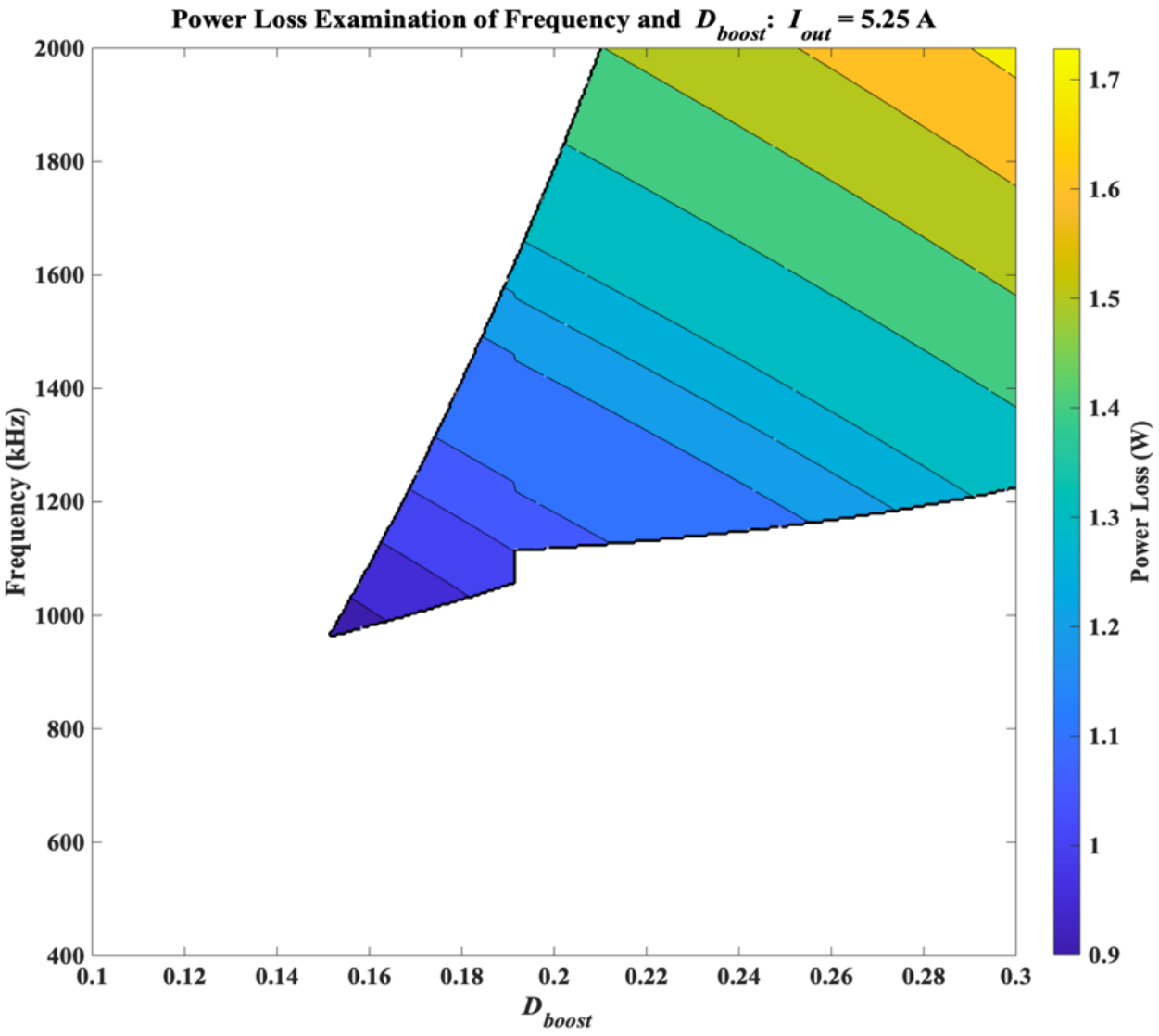

Figure 6.31: Power loss examination using the average model at I_{out} = 5.25 A.

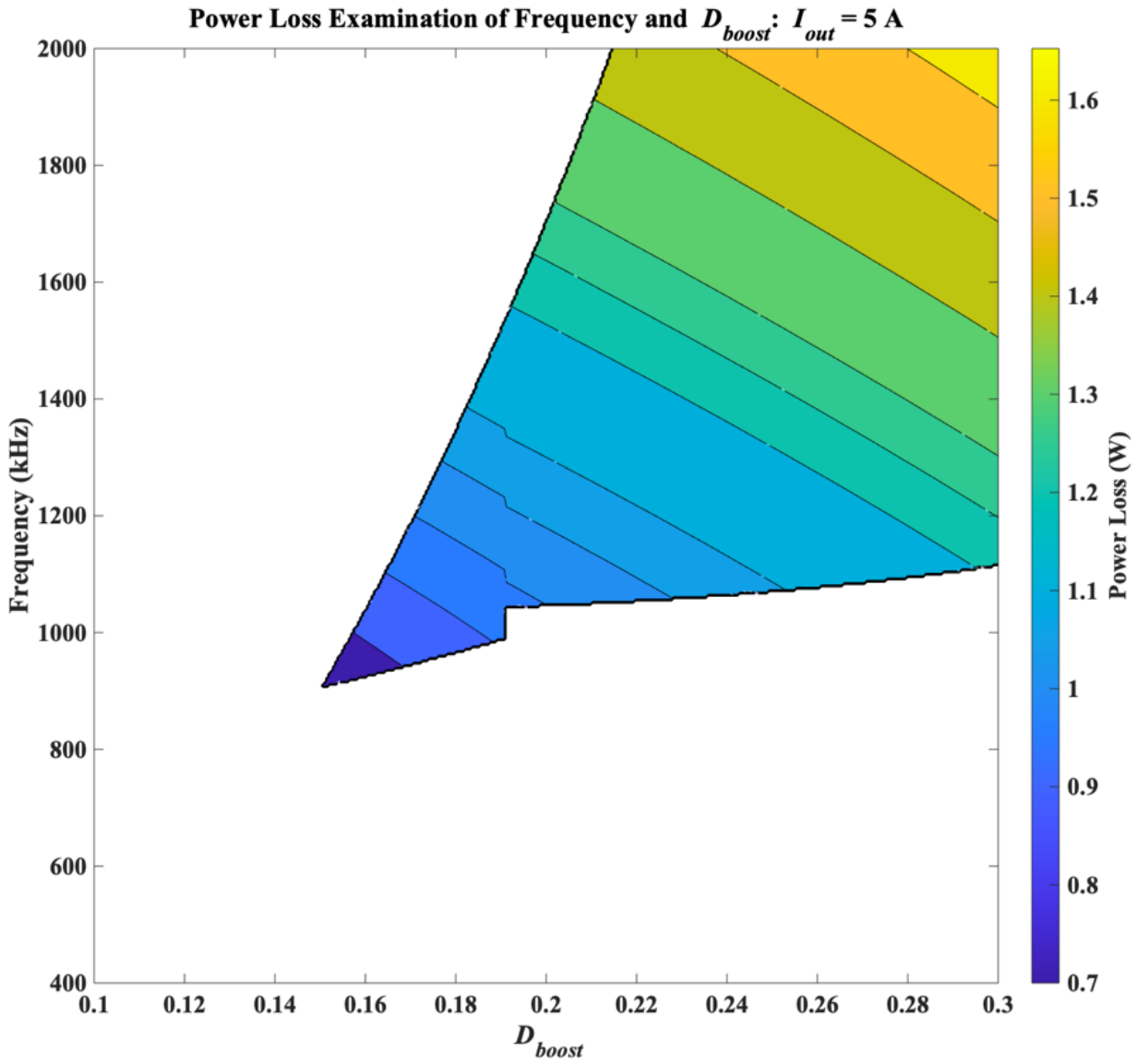

Figure 6.32: Power loss examination using the average model at I_{out} = 5.0 A.

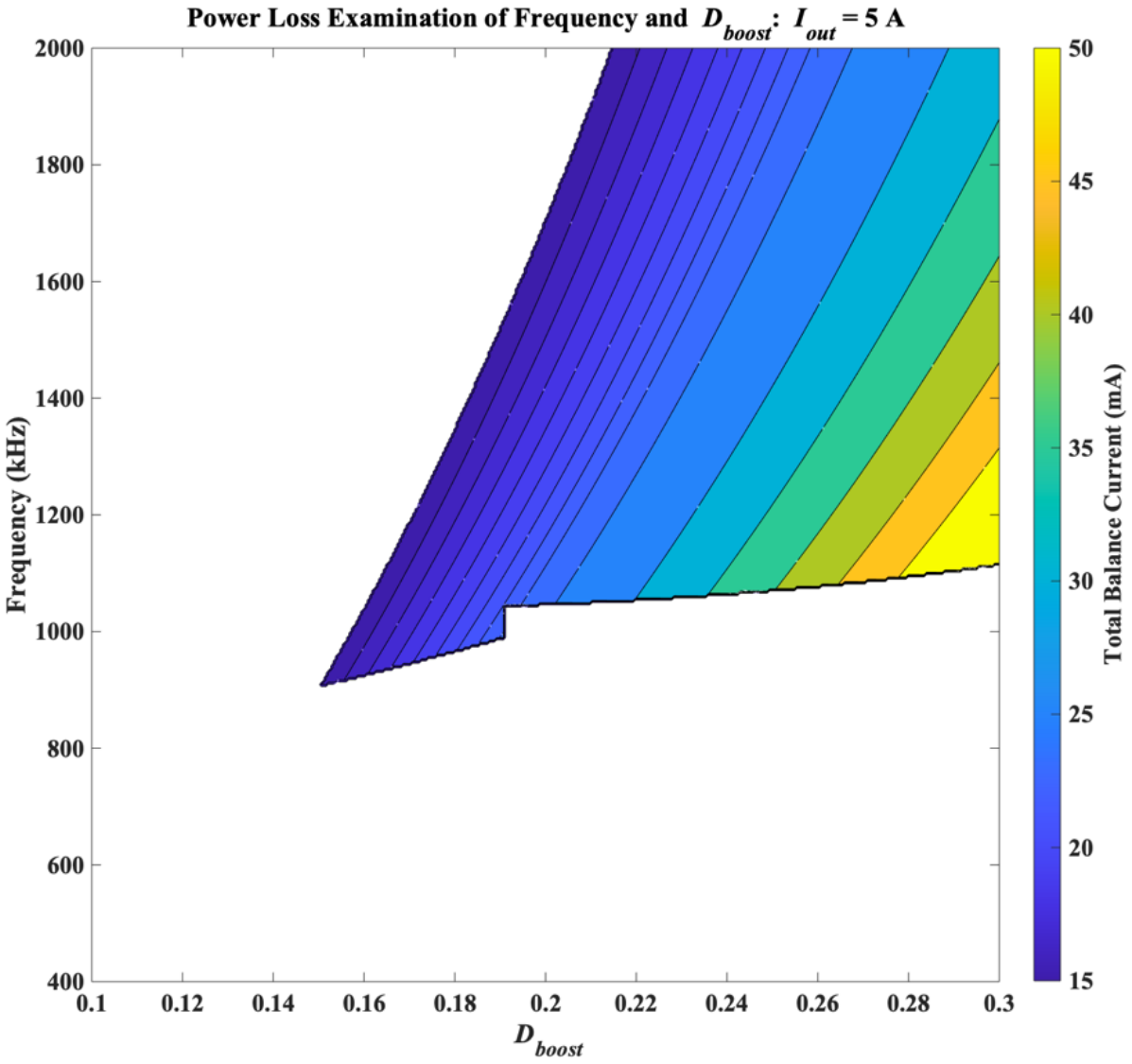

Figure 6.33: Balance current examination using the average model at I_{out} = 5.0 A.

Finding the overlap these two plots shows the available operating points that still provide over 15 mA of balance current and less than 1 W of P_D. There is a small window useable for balancing operation at 5.0 A charging current. This is the approximately the highest possible current that still achieves balancing, but further optimization is needed to provide a definite solution. In the plot of Figure 6.33, over 15 mA of balance current is achievable at 1.050 MHz and D_{boost} = 19.0 %. Here r is 75 %. Because this area distribution also meets the requirements for the minimum on-resistance required to achieve the highest I_{out}, this area distribution is kept for the remainder of the design. Using the state space model, a narrowed sweep is done from 1 MHz to 1.2 MHz across every D_{boost} from 18 to 20 %. The plot is displayed in Figure 6.34 and contains the resulting balance current at that interval.

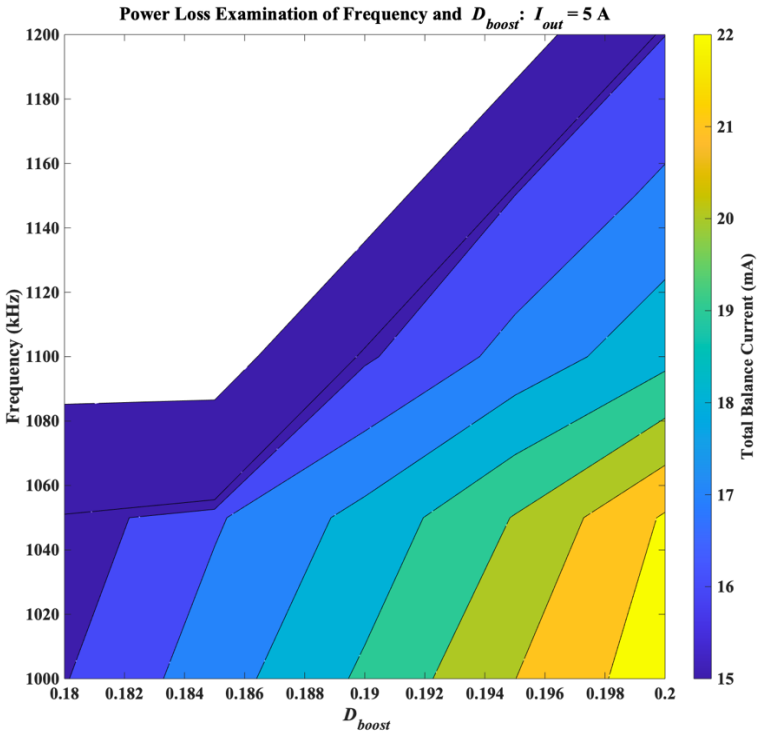

Figure 6.34: Balance Current examination using state space model at I_{out} = 5.0 A.

To validate this design, a single operating point is examined with I_{out} = 5.0 A, f_s = 1.050 MHz, and D_{boost} =19.0 % by state space analysis. The high side transistors are given 75 % of the total chip area to maximize efficiency at this operating point. The result is shown in Figure 6.35 and Figure 6.36. This operation matches up with both the state space and average model sweep. Over 18 mA of $I_{Balance}$ and the P_D for IC remains under 1 W. In both models, only the loss of the transistors is counted towards the 1 W limit.

If the limit of the peak inductor current is ignored, the balance current is shown in Figure 6.37 where the balance transistors have a $r_{balance}$ of 300 mΩ. All points below 850 kHz remain below P_D of 1 W. 500 mA of balance current is achieved at a smaller frequency. Though $r_{balance}$ is not optimized in the work, if conduction loss through the balance transistors is allowed to increase without the chip exceeding 1 W of P_D, then the adjustment of $r_{balance}$ can yield high balance currents. The SC buck three-level boost is capable of more than 15 mA of balance current.

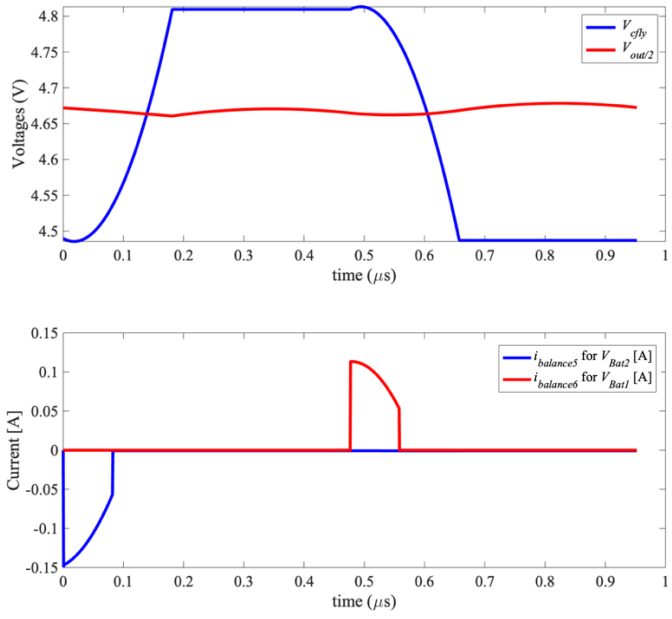

Figure 6.35: State space $v_{cfly}(t)$ and balance current waveforms for I_{out} = 5.0 A at 1050 kHz.

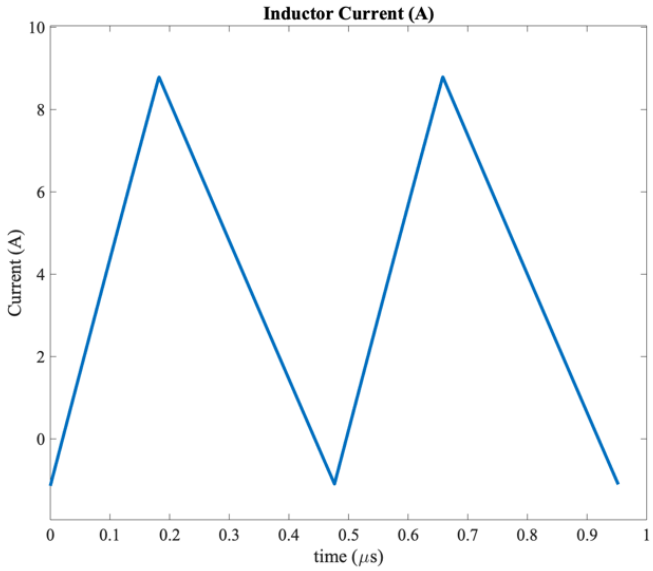

Figure 6.36: State space inductor current waveforms for I_{out} = 1.5 A at 500 kHz.

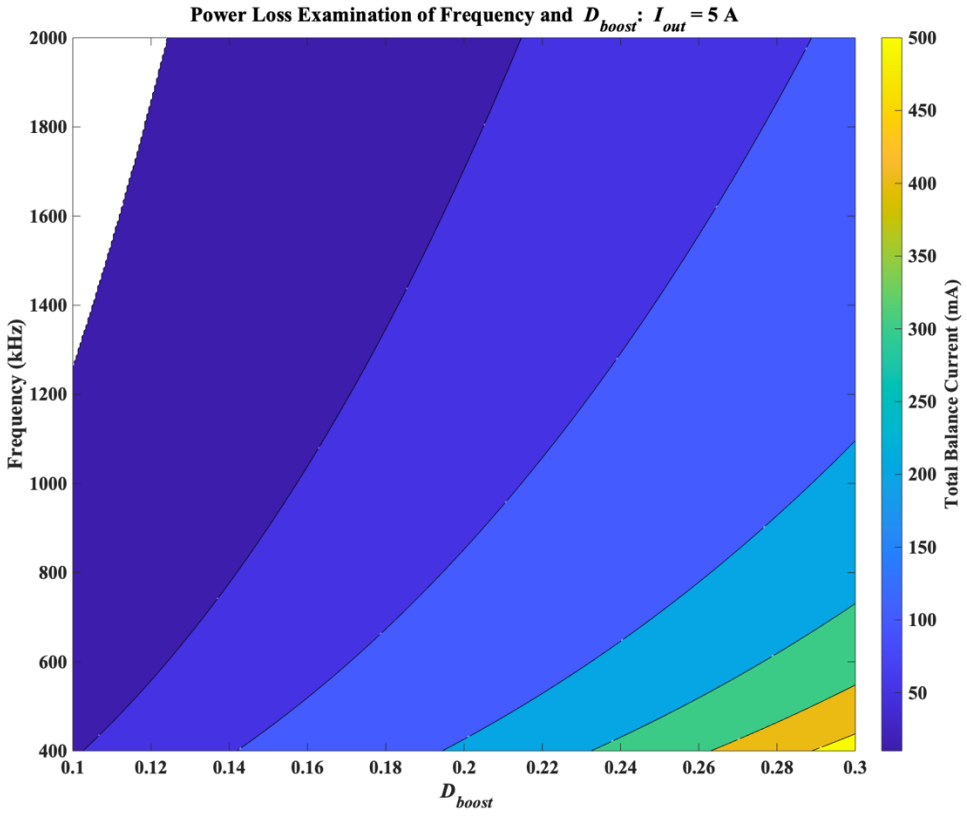

Figure 6.37: Balance current levels ignoring the limit of inductor current and $r_{blalance}$ = 300 mΩ.

6.3 Summary

In this chapter, design analysis for an IC for mobile battery chargers is examined. The area A_{core} and the parasitics of the transistors sets a limit on the potential of the SC buck three-level boost converter. Layout (physical design) is critically important to maximize the area for devices while minimizing transistor parasitics for this high-current application. Though balancing is not yet possible at the maximum charging current without exceeding P_D = 1 W with the transistors available in the process at hand, balance current greater than 15 mA is possible for 5 A charging current on an IC that contains the three-level boost (four power transistors), the gate circuitry, and the two balance transistors. The allowable die area is constrained to that of commercial state-of-the-art mobile applications. State space modeling is a valuable resource used in this work to closely predict the resonant behavior of the small energy storage components utilized in the converter. The design followed the requirements in Table 6.1 with passives sized accordingly for mobile applications. Chip area is distributed between the transistors to prevent operation from exceeding P_D. Average modeling, though not as accurate as the state space model, is useful in narrowing the field of operating points for further investigation with state space analysis. The result is a converter that provides a maximum charging current comparable with other commercial IC products for 2S batteries in Table 1.2 and that can also simultaneously charge and balance batteries when the input voltage is 20 V and the charge current is 5 A. Some level of balancing is possible for all operating points less that yield less than 5 A of charge current.

Chapter 7 Conclusions

Mobile devices are ever prevalent in the modern world. With each mobile device advancing with intricate applications to meet consumer needs, mobile electronics require more power-efficient charging capabilities than ever before. Consumers still desire rapid charge times, so battery charging technology that can quickly recharge batteries but still provide required energy is critical. Many vendors are moving towards 2S battery chargers because increasing the battery system voltage (compared to a single battery cell system) reduces the amount of charging current it takes to achieve a particular charge time. However, battery strings with multiple batteries in series require balancing to prolong battery life and maximize the energy utilization of the batteries throughout the charging process. Instead of a multi-chip system to provide all the complex functions required to properly charge and balance batteries in a 2S configuration, a single chip solution is proposed using the SC three-level boost converter. A buck input stage can be added to incorporate a larger input voltage range.

7.1 Contributions

This thesis explored the design of the SC three-level boost converter as a integrateable mobile battery charging topology with balancing capability. The operation of the converter utilizes only two additional transistors (from the conventional three-level boost charging structure) that only require milliamps of current rating to interact with the flying capacitor to balance the batteries. Additionally, one fourth of the inductance is required for the charger as compared to other

commercial charging products with two-level topologies. A wide range of operating points is explored based on the input of the USB Type-C standards. Parameters such as modulation, passive sizing, frequency limits, and transistor sizing are investigated with the goal of achieving sufficient balancing current at the highest possible charging current without exceeded the maximum on-chip loss.

The voltage of the flying capacitor is determined to have a major effect on the balancing operation. The larger the voltage ripple on the flying capacitor, the larger the magnitude of the total balance current. Battery balancing is possible when either Battery 1 or 2 has the greater SOC if the average of the flying capacitor voltage over one switching period is near half of the output voltage. Because the average of the flying capacitor can be less than expected because of parasitics and unequal disturbances between each half-period from input stage switching, manual tuning of the inductor current is shown to adjust the magnitude of the flying capacitor voltage. A hardware prototype using the alternative buck modulation (for the input stage) where the buck duty cycle is halved and switched at twice the frequency allows experimental verification of the average and state space models for charger and balancer operations. State space models are verified to more accurately describe converter behavior when the smaller passives (required for small area mobile applications) are used leading to large ripple operation.

Because only a limited area is available on-chip based on the maximum chip size that is still marketable (4.00 mm x 4.00 mm) and transistor isolation is needed for LDMOS devices not referenced to ground, efficient layout design and area distribution is required for the battery charger to offer its full benefit. Layouts not conducive to high power efficiency limit the maximum achievable charging current that can simultaneous balancing because of the chip power dissipation limits. Through the state space models verified through experiment, the battery charger has the

potential to operate with 6.4 A charging current comparable to other IC chargers on the market. The SC three-level boost IC with a buck input stage can also provide charging current up to 5 A that has both balancing and charging capability without exceeding the power dissipation limits of an IC based on the thermal resistance for a QFN package.

7.2 Recommended Future Work

While the area distribution for optimizing transistors is accomplished, there is room to further investigate the optimization of all the converter parameters to maximize the performance in terms of power efficiency, balance current, and power density. Other high-efficiency, high-voltage semiconductor fabrication processes that can provide transistors with smaller parasitics may be available in the near future.

Further work is required to investigate the input stage of the converter and how it should operate. Additionally, a current program control method increases the converter's ability to set the value of the flying capacitance voltage. There could be potential benefits for the SC three-level boost to operating away from half the output voltage in terms of increasing the balance current. Semiconductor research and even other layout design improvements could provide more benefit for the converter. The entire buck three-level boost converter could be integrated onto a single chip.

Bibliography

[1] STMicroelectronics, "USB Power Deliever and Type C," APEC, 2016.

[2] T. Instruments. BQ25713. [Online]. Available: http://www.ti.com/product/BQ25713.

[3] W. Y. Chang, “State of Charge Estimation for LFP Battery Using the Hybrid Method,” Applied Mechanics and Materials, vol. 431, pp. 221–225, 2013.

[4] J. Rivera-Barrera, N. Muñoz-Galeano, and H. Sarmiento-Maldonado, “SoC Estimation for Lithium-ion Batteries: Review and Future Challenges,” Electronics, vol. 6, no. 4, p. 102, 2017.

[5] 4. A. Nugroho, E. Rijanto, F. D. Wijaya and P. Nugroho, "Battery state of charge estimation by using a combination of Coulomb Counting and dynamic model with adjusted gain," 2015 International Conference on Sustainable Energy.

[6] EEMB, "https://www.eemb.com/battery/rechargeable-battery/li-ion-battery/cylindrical-type.html".

[7] S. Charfi, A. Atieh, M. Chaabene and M. Haj-Ahmad, "Exploiting DOD set value to manage the operation of a diesel generator in a hybrid renewable system," 2017 8th International Renewable Energy Congress (IREC), Amman, 2017, pp. 1-4.

[8] S. Chowdhury, M. N. Bin Shaheed and Y. Sozer, "An Integrated State of Health (SOH) Balancing Method for Lithium-Ion Battery Cells," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 5759-5763.

[9] M. Murnane and A. Ghazel, "A Closer Look at State of Charge (SOC) and State of Health (SOH) Estimation Techniques for Batteries," Analog Devices, 2017.

[10] "Apple," [Online]. Available: https://www.apple.com/batteries/.

[11] Gabian, Gabriel Alejo, "High-current integrated battery chargers for mobile applications. " Master's Thesis, University of Tennessee, 2017. http://trace.tennessee.edu/utk_gradthes/4874.

[12] M. Liu, C. Zhao, J. Song and C. Ma, "Battery Charging Profile-Based Parameter Design of a 6.78-MHz Class E^2 Wireless Charging System," in IEEE Transactions on Industrial Electronics, vol. 64, no. 8, pp. 6169-6178, Aug. 2017.

[13] H. Newe, S. Deters and R. Saiju, "Analysis of Electrical Charging Characteristics of Different Electric Vehicles Based on the Measurement of Vehicle-specific Load Profiles," NEIS 2019; Conference on Sustainable Energy Supply and Energy Storage Systems, Ha.

[14] D.-K. N. A. Editors. (2016) A designer's guide to lithium (Li-ion) battery charging. [Online]. Available: https://www.digikey.com/en/articles/techzone/2016/ sep/a-designer-guide-fast-lithium-ion-battery-charging.

[15] S. De Breucker, K. Engelen, R. D'hulst and J. Driesen, "Impact of current ripple on Li-ion battery ageing," 2013 World Electric Vehicle Symposium and Exhibition (EVS27), Barcelona, 2013, pp. 1-9.

[16] M. J. Brand, M. H. Hofmann, S. S. Schuster, P. Keil and A. Jossen, "The Influence of Current Ripples on the Lifetime of Lithium-Ion Batteries," in IEEE Transactions on Vehicular Technology, vol. 67, no. 11, pp. 10438-10445, Nov. 2018.

[17] Y. Zheng, M. Ouyang, L. Lu, J. Li, X. Han and L. Xu, "On-line equalization for lithium-ion battery packs based on charging cell voltages: Part 1. Equalization based on remaining charging capacity estimation," J. Power Sources, vol. 247, pp. 676-686, 2014.

[18] J. Gallardo-Lozano, E. Romero-Cadaval, M. I. Milanes-Montero and M. A. Guerrero-Martinez, "Battery equalization active methods," J. Power Sources, vol. 246, pp. 934-949, 2014.

[19] Z. Wangbin, H. Jun, C. Haitao, L. Huiying, W. Chunyu and L. Minghao, "An Active Balance Circuit Applied to Lithium Ion Battery Packs," 2018 IEEE 4th International Conference on Control Science and Systems Engineering (ICCSSE), Wuhan, China, 2018.

[20] Z. H. Cai, G. F. Liu, and J. Luo, "Research state of charge estimation tactics of nickel-hydrogen battery," in Proceedings of the International Symposium on Intelligence Information Processing and Trusted Computing (IPTC '10), pp. 184–187, Huanggang, C.

[21] Y. Shi, K. Smith, R. Zane and D. Anderson, "Life prediction of large lithium-ion battery packs with active and passive balancing," 2017 American Control Conference (ACC), Seattle, WA, 2017, pp. 4704-4709.

[22] J. Ouyang, P. Zhang, S. Wang and H. Li, "Active balancing charging module with continuous and controllable isolation for battery management system," 2017 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Haining, 2017, pp. 1-4.

[23] D. D. Arnaudov, K. Y. Kishkin and K. Kroičs, "Single-ended Resonant Inverter for Active Balancing System," 2019 IEEE 60th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 2019.

[24] L. Rui, W. Lizhi, H. Xueli, D. Qiang, and Z. Jie, "A review of equalization topologies for lithium-ion battery packs," in 2015 34th Chinese Control Conference (CCC), 2015, pp. 7922–7927.

[25] Y. Shang, C. Zhang, N. Cui, and J. M. Guerrero, “A Cell-to-Cell Battery Equalizer With Zero-Current Switching and Zero-Voltage Gap Based on Quasi-Resonant LC Converter and Boost Converter,” IEEE Transactions on Power Electronics, vol. 30, no. 7.

[26] Lee, Yuang-Shung; Guo-Tian Cheng, "Quasi-Resonant Zero-Current-Switching Bidirectional Converter for Battery Equalization Applications," Power Electronics, IEEE Transactions on, vol.21, no.5, pp.1213,1224, Sept. 2006.

[27] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, New York: Kluwer AcademicPublisher, 2004.

[28] Sang-Hyun Park; Ki-Bum Park; Hyoung-Suk Kim; Gun-Woo Moon; Myung-Joong Youn, "Single-Magnetic Cell-to-Cell Charge Equalization Converter With Reduced Number of Transformer Windings," Power Electronics, IEEE Transactions on , vol.27, no.6, pp.2900,2911, Ju.

[29] CholHo Kim, Hong-Sun Park, ChongEun Kim. Charge Equalization Converter with Parallel Primary Winding for Series Connected Lithium-Ion Battery strings in HEV[C]. The 7th International Conference on Power Electronics. EXCO, Daegu, Korea, 2007:795-800.

[30] B. Gerislioglu, F. Ozturk, A. E. Sanli and G. Gunlu, "The multi-windings forward structure battery balancing," 2014 11th International Conference on Electronics, Computer and Computation (ICECCO), Abuja, 2014, pp. 1-4.

[31] H. Kutkut, "A modular non dissipative current diverter for EV battery charge equalization," Applied Power Electronics Conference and Exposition, Anaheim, CA, 1998, pp. 686-690.

[32] D. Lundquist, "System and method to facilitate voltage balancing in a multi-cell battery," US6624612 B1, Sep. 23, 2003.

[33] Z. Pan, L. Liu, Y. Du, Y. Shi and X. Yang, "Low-Loss Switched Capacitor Voltage Balancing Circuit and Its Design Considerations," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 882-888.

[34] C. Pascual and P. T. Krein, "Switched capacitor system for automatic series battery equalization," Proceedings of APEC 97 - Applied Power Electronics Conference, Atlanta, GA, USA, 1997, pp. 848-854 vol.2.

[35] M. D. Seeman and S. R. Sanders, “Analysis and optimization of switched-capacitor dc-dc converters,” in 2006 IEEE Workshops on Computers in Power Electronics, July 2006, pp. 216–224. 15.

[36] M. A. Rojas-Gonzlez, J. Torres, and E. Snchez-Sinencio, “Design of a fully-integrated buck voltage regulator using standard cmos technology,” in 2012 IEEE 3rd Latin American Symposium on Circuits and Systems (LASCAS), Feb 2012, pp. 1–4. 11.

[37] M. Steyaert, T. V. Breussegem, H. Meyvaert, P. Callemeyn, and M. Wens, “Dc-dc converters: From discrete towards fully integrated cmos,” in 2011 Proceedings of the ESSCIRC (ESSCIRC), Sept 2011, pp. 42–49.

[38] K. Kesarwani, R. Sangwan and J. T. Stauth, "Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation," in IEEE Transactions on Power Electronics, vol. 30, no. 12, pp. 6966-6977, Dec. 2015.

[39] S. Li, N. Zhang, S. Zheng, W. Xie and K. Smedley, "A Dickson Resonant Switched-capacitor Converter with "Indirect" Resonant Core and Continuous Conversion Ratio," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019.

[40] K. Kesarwani, R. Sangwan and J. T. Stauth, "Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation," in IEEE Transactions on Power Electronics, vol. 30, no. 12, pp. 6966-6977, Dec. 2015.

[41] V. Yousefzadeh, E. Alarcon and D. Maksimovic, "Three-level buck converter for envelope tracking applications," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 549-552, March 2006.

[42] D. Reusch, F. C. Lee and M. Xu, "Three level buck converter with control and soft startup," 2009 IEEE Energy Conversion Congress and Exposition, San Jose, CA, 2009, pp. 31-35.

[43] F. Li, R. Hao, H. Lei, X. You, C. Ke and J. Wang, "Non-Inverting Three-Level Buck-Boost Converter for Wide Voltage Range Application," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 4870-4875.

[44] A. B. Ponniran and M. A. N. B. Kasiran, "Parameters design evaluation in 3-level flying capacitor boost converter," 2017 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE), Langkawi, 2017, pp. 195-199.

[45] Z. Liao, Y. Lei and R. C. N. Pilawa-Podgurski, "Analysis and Design of a High Power Density Flying-Capacitor Multilevel Boost Converter for High Step-Up Conversion," in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4087-4099, May 2019.

[46] Y. Tan, C. Lam, S. Sin, M. Wong and R. P. Martins, "Design and Control of An Integrated 3-Level Boost Converter under DCM Operation," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, 2018, pp. 1-5.

[47] V. Yousefzadeh, E. Alarcon and D. Maksimovic, "Three-level buck converter for envelope tracking applications," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 549-552, March 2006.

[48] A. Ponniran, K. Orikawa and J. Itoh, "Minimum flying capacitor for N-level capacitor DC/DC boost converter," 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 1289-1296.

[49] A. B. Ponniran, K. Orikawa and J. Itoh, "Minimum Flying Capacitor for N-Level Capacitor DC/DC Boost Converter," in IEEE Transactions on Industry Applications, vol. 52, no. 4, pp. 3255-3266, July-Aug. 2016.

[50] T. Instruments, "https://www.ti.com/product/BQ25887," [Online].

[51] K. Vitols, "Redesign of passive balancing battery management system to active balancing with integrated charger converter," 2014 14th Biennial Baltic Electronic Conference (BEC), Tallinn, 2014, pp. 241-244.

[52] N. Sturcken et al., "A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer delivering 10.8A/mm2," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 400-402.

[53] H. K. Krishnamurthy, V. Vaidya, S. Weng, K. Ravichandran, P. Kumar, S. Kim, R. Jain, G. Matthew, J. Tschanz, and V. De, “20.1 a digitally controlled fully integrated voltage regulator with on-die solenoid inductor with planar magnetic core in 14nm tri-gate cmos,” in Solid-State Circuits Conference (ISSCC), 2017 IEEE International. IEEE, 2017, pp. 336–337.

[54] T. Takayama and D. Maksimovi, “A power stage optimization method for monolithic dc-dc converters,” in 2006 37th IEEE Power Electronics Specialists Conference, June 2006, pp. 1–7.

[55] A. Hastings, "The art of analog layout." Prentice Hall, 2006.

[56] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Hoboken, New Jersey: John Wiley & Sons, Inc., 2019.

[57] International technology roadmap for semiconductors, [Online]. Avaliable: http:// www.itrs.net/, Oct. 2015.

[58] EPC, “What is GaN,” https://epc-co.com/epc/GalliumNitride/WhatisGaN.

[59] M. Shrivastava, "Drain Extended Tunnel FET—A Novel Power Transistor for RF and Switching Applications," in IEEE Transactions on Electron Devices, vol. 64, no. 2, pp. 481-487, Feb. 2017.

[60] Disney, D.; Park, I.L.Y.; Lin, W.C.; Kim, J. High-voltage IC technologies for AC/DC power conversion. In Proceedings of the IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, 1–4 June 2015; pp. 142–145.

[61] Kojima, J.; Matsuda, J.; Kamiyama, M.; Tsukiji, N.; Kobayashi, H. Optimization and analysis of high reliability 30–50 V dual RESURF LDMOS. In Proceedings of the 13th IEEE International Conference on Solid-State and Integrated Circuit Technology, Hangzhou.

[62] D. Brisbin, P. Lindorfer, P. Chaparala, “Substrate current independent hot carrier degradation in NLDMOS devices” National Semiconductor Corporation, 2006.

[63] E. P. Hema, G. Sheu, M. Aryadeep, E. D. Kurniawan, S. M. Yang and P. A. Chen, "Optimization of NLDMOS structure for higher breakdown voltage and lower On-

Resistance," 2014 IEEE 8th International Power Engineering and Optimization Conference (PEOCO2014), L.

[64] K. Nakamura, Y. Kawaguchi, K. Karouji, K. Watanabe, Y. Yamaguchi, A. Nakagawa, “Complementary 25 V LDMOS for analog applications based on 0.6ɜm BICMOS Technology”, BCTM 2000, pp. 94-97.

[65] Y. C. Kao and E. D. Wolley, "High-voltage planar p-n junctions," in Proceedings of the IEEE, vol. 55, no. 8, pp. 1409-1414, Aug. 1967.

[66] N. Mohan, T. M. Undeland and W. P. Robbins, Power Electronics: Converters, Applications, and Design, John Wiley & Sons, Inc., 1995.

[67] R. C. Jaeger and T. N. Blalock, "Microelectronic Circuit Design," McGraw-Hill, 1997.

[68] D. Costinett, D. Maksimovic, and R. Zane, “Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies,” IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 985–995, Feb 2015. 11, 22.

[69] A. Lidow, “Is it the end of the road for silicon in power conversion?” Efficient Power Conversion (EPC), Tech. Rep., 2011. 19, 21.

[70] A. Lidow, "Is it the end of the road for silicon in power conversion?," in 6th International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg/Germany, 2010.

[71] Y. Attia and M. Youssef, "GaN on silicon E-HEMT and pure silicon MOSFET in high frequency switching of EV DC/DC converter: A comparative study in a nissan leaf," 2016 IEEE International Telecommunications Energy Conference (INTELEC), Austin, TX, 2016.

[72] “Enhancement-mode gallium nitride technology,” Efficient Power Conversion (EPC), 2017, technology Brief: TB001. xii, 20, 21.

[73] F. Chunmei, L. Jun, and V. G. Agelidis, "A novel voltage balancing control method for flying capacitor multilevel converters," in Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE, 2003, pp. 1179-1184 Vol.2.

[74] R. Ling and Z. Shu, "A piecewise sliding-mode controller for three level buck DC-DC converters," 2016 Chinese Control and Decision Conference (CCDC), Yinchuan, 2016, pp. 643-648.

[75] L. Lu, A. Prodić, G. Calabrese, G. Frattini and M. Granato, "Current Programmed Mode Control of Multi-Level Flying Capacitor Converter Near Zero-Ripple Current Region," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA.

[76] L. Lu, S. M. Ahsanuzzaman, A. Prodic, G. Calabrese, G. Frattini and M. Granato, "Peak offsetting based CPM controller for multi-level flying capacitor converters," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX.

[77] L. Corradini, D. Maksimovic, P. Mattavelli and R. Zane, Digital Control of High-Frequency Switched-Mode Power Converters, Hoboken, New Jersey: John Wiley & Sons, Inc., 2015.

[78] J. A. Baxter and D. J. Costinett, "Converter Analysis Using Discrete Time State-Space Modeling," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp. 1-8.

[79] Terasic Technologies, "DE0-Nano Development and Education Board," [Online]. Available: http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=139&No=593&PartNo=4.

[80] Quick-Pack. Open cavity packages. [Online]. Available: http://www.icproto.com/ cap-ic-open-cavity-qfn.html.

[81] E. J. Kennedy, Operational Amplifier Circuits, New York, NY: Holt, Rinehart, and Winston, Inc., 1988.

[82] T. Instruments. NanoStart and NanoFreet 300 μm solder bump wafer chip-scale package application. [Online]. Available: http://www.ti.com/lit/an/sbva017/sbva017.pdf.

Vita

Quillen Blalock was born in Marietta, Georgia but raised in Knoxville, Tennessee from an early age. He attended the University of Tennessee as an undergraduate. He worked at Siemens Molecular Imaging his junior year to complete a Co-Op experience, and he also began undergraduate power electronics research his junior year as well. He lead a team for his senior design project which created a sleep apnea monitor and detection system for infants in ICU. He served as a president of a collegiate ministry his senior year and continues serving with his church, Sevier Heights Baptist. He graduated cum laude with a bachelor's degree in Electrical Engineering in May 2018,

Quillen accepted a graduate research assistantship under Dr. Daniel Costinett through the Wide Bandgap Traineeship as he pursued his Master of Science degree. He was also awarded the Bodenheimer Fellowship throughout his master's studies. During his time as a student, he researched magnetic design and alternative strategies to fabricate inductors to realize geometries conducive to high-Q before focusing on the battery charger-balancer proposed in his Master's Thesis. After graduation, he plans to stay in Knoxville and work as an Analog Designer for Texas Instruments.