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Analysis and Characterization of Single-Poly Floating Gate Devices in 0.35um PDSOI Process

A Thesis
Presented for the
Master of Science
Degree

The University of Tennessee, Knoxville

Chandra Sekhar Acharyulu Durisety
December 2002

A

tribute to

my parents Adharvana Charyulu and Aparna Devi

and brother Sankhyayana Charyulu

Acknowledgements

I have no words to convey the depth of my gratitude to my advisor Dr. Benjamin J. Blalock for his confidence and faith in me. I wish to thank him for his patience, support and freedom he has given me throughout the work. I would like to express to him my deep gratitude for keeping me focussed, his helping hand in times of need and for allocating his precious time with thoughtful discussions. A special portion of my gratitude goes to my Thesis Committee for their precious comments.

I am thankful to Mr.Rick Kuhlman in developing the wonderful Labview programs, which were very crucial in the completion of this thesis. I wish to thank Mr.Todd Preston for building me the test boards.

Finally, it would be remiss if I did not offer my thanks, love and gratitude to my family. Especially to my Dad and Mom who made a hard decision by approving my interest to restart my education. Also to my friends Kalcy, Chasa, Anki Reddy and Chesp, who encouraged me by helping financially and mentally to continue my education, after a long break from undergraduation. I thank Venkatesh Srinivasan for his time consuming and detailed efforts in reviewing the first draft. I would like to thank Brian Dufrene, Stephen Terry, James Vandersand and all those who helped me in the completion of this work.

A hearty greetings to you all, in helping me reach my "**1st mile stone**" to my ambition. I love you all.

Abstract

The purpose of this thesis is to demonstrate a single-poly Floating Gate Device (FGD) in 0.35μm Partially Depleted Silicon On Insulator (PDSOI) process for use in analog circuits for post process trimming. Floating gate devices with different aspect ratios have been fabricated to facilitate this behavioral study in PDSOI process. Fundamentals of floating gate devices, the advantages and disadvantages of PDSOI compared to bulk CMOS with respect to single-poly floating gate devices are discussed. Various experiments on behavior and performance of threshold voltage have been conducted and its variation with programming/erasing time and amplitude has been analyzed. The single-poly FGD's on-resistance variation and hysteresis behavior with threshold voltage has been documented. A mathematical relation between FGD's on-resistance and threshold voltage has been experimentally derived. Intrinsic data retention has been estimated through extrapolation of experimental data. A process independent MATLAB simulation model has been successfully developed for understanding the threshold voltage time dependence characteristics. And finally, this work has shown that programmable or post-process trimmable analog circuits can be implemented in SOI using single-poly FGDs as programmable resistive elements. A SOI programmable beta-multiplier current reference has been successfully demonstrated using the single-poly FGD as a resistive element.

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Chapter 1

Introduction

Programmable devices are essential components for reconfigurable systems which form the backbone of System-On-a-Chip (SOC) applications. Since the early 1960's, there has been a tremendous effort to develop semiconductor nonvolatile memories. A semiconductor nonvolatile memory offers a better solution from the standpoint of key issues such as speed, cost, complexity, density (no. of bits/area), reliability, ease of programmability, and physical area/volume. These nonvolatile memories are classified into various types depending on the available technology (Programmable Read Only Memories PROMs), customer requirements (Electrically Erasable PROM EEPROMs), and the market and price considerations (Flash EEPROMs). The first programmable nonvolatile semiconductor memories were PROMs that used UV rays for erasing. These were replaced by EEPROMs driven by customer requirements like In-System-Programmability (ISP, that utilized +/-12V power supplies then readily available on most commercial printed circuit boards). These were in vogue for more than a decade until recently replaced by Flash EEPROMs. Flash EEPROMs offer higher densities and faster programmability with reduced power consumption thus prompting their widespread use in portable consumer markets. Recently the Multi Level Charge Storage (MLCS) mechanism [17] further increased the density of these Flash EEPROMs. Though there is a vast difference in programming/erasing techniques in all of these different memory devices, their common denominator, however is the Floating Gate Device (FGD).

1.1 Why the need for Floating Gate Device?

This chapter gives an introduction to the Floating Gate Device structure and its characteristics used in this work. EEPROMS, one of the basic memory components, are used to store the BIOS and the configuration details in applications spanning from simple add-on cards in personal computers to complex boards used in ATM Routers. These devices should be able to retain data even without power for long durations owing to a very low charge loss per day. Present day industry standards [7] require EEPROMs to have a data retention of 10yrs. Due to growing importance to reconfigurability, there is a demand for reprogramming of these devices, paving the way towards the development of UV-PROMs and EEPROMs. Since EEPROMs are electrically reconfigurable, they are more widely used compared to their predecessors. The first EEPROMs used doubly-poly process as demonstrated by Kahng and Sze [1]. Since EEPROMs are designed for reconfiguration, the endurance characteristics also play a crucial role in defining the characteristics. An endurance of 10^7 cycles is one of the characteristics of a good EEPROM.

1.2 What is a Floating Gate Device?

An electrically isolated gate terminal of a MOS transistor is commonly referred to as a Floating Gate, while the entire structure is referred as the Floating Gate Device (FGD). In the mid 1960's, this was made possible by using multi-poly layer fabrication processes, compared to the standard single-poly processes used for most of the integrated circuit fabrication today. The gate of the regular MOS transistor is replaced by a thick conducting metal layer sandwiched between a thin oxide layer at the bottom and the thick oxide layer

at the top. This cross-section is shown in the Figure 1.1. Since the conducting metal (the actual charge storage medium) is completely encased by insulator, this structure can be used as a long-term memory element. The charge on the conducting metal can be modulated by adjacent conductors by changing the number of electrons stored on the isolated floating gate. Depending on whether the charge is added or removed from the conducting metal plate, the procedure is referred as Programming or Deprogramming/Erasing, respectively.

1.3 Applications of the FGD

The FGD forms the fundamental building block in the binary data storage elements like EPROMS and EEPROMs. This technology provides the ease of reprogrammability compared to the traditional fuse trimming technology. It can also be used for neural networks [34-35], offset trimming in operational amplifiers [5], design of low-voltage operational amplifiers [9], reprogrammable reference current generators [3], continuous-time filters/amplifiers [52] and low supply voltage designs [8-9]. Thus the FGD is applicable to both digital and analog systems. To enhance analog and digital systems in the future, this work demonstrates a single-poly FGD on SOI, the technology of choice for

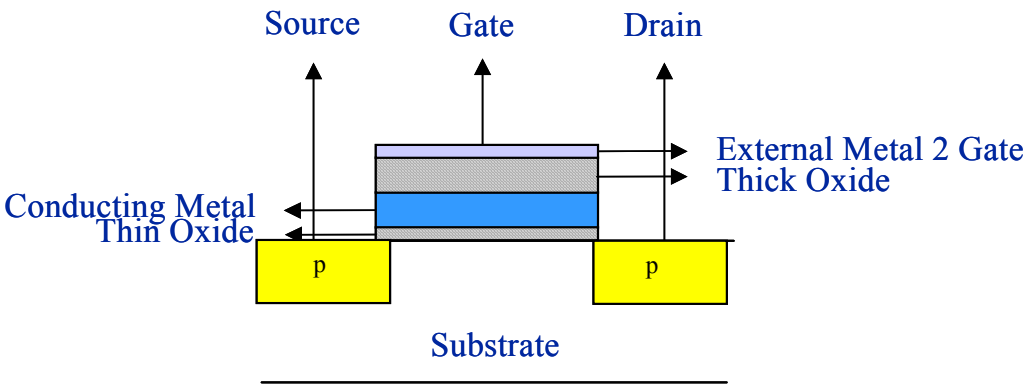


Figure 1.1: Basic Floating Gate Structure

the semiconductor industry according to the International Roadmap for Semiconductors [53].

1.4 Overview

Currently the FGD is widely used in EEPROMs [40-45] and also in neural networks [46-50]. This literature shows that double-poly layer processes were widely used in the construction of the FGD. A double-poly process, in comparison to standard single-poly processes, requires more processing steps, mask layers, higher cost of fabrication, and may have lower yield. Later, the FGD was fabricated using a MOS transistor and a capacitor [18]. In 1994, Ohsaki [2] developed a new structure for making the FGD using two MOS transistors in a standard bulk CMOS single-poly process.

The primary purpose of this thesis is to characterize FGDs in a 0.35μm PDSOI process, that were developed using the Ohsaki [2] single-poly structure architecture. In addition, a MATLAB model has been developed to simulate the programming/erasing characteristics for a given FGD.

With the growing usage of EEPROMs, the characterization of the FGD is also gaining prominence as seen from the development of IEEE standards for such characterization practices [7]. A literature survey shows that single-poly FGD's have been developed in CMOS processes but not in PDSOI. This thesis concentrates on the characterization of the single-poly FGD in a 0.35μm PDSOI process and provides examples in improving the performance of the existing designs. As said earlier, the literature survey showed that

the FGDs have been primarily used in the memory arena and neural networks. Chapter 2 gives details regarding the basic structure of the single-poly FGD in PDSOI process, various programming, deprogramming and reading methodologies. Chapter 3 is devoted to the analysis and characterization of PDSOI single-poly FGD parameters such as threshold voltage, on-resistance, and temperature coefficient to facilitate their use in analog circuits. Chapter 4 briefly analyzes the memory characteristics of the SOI single-poly FGD, such as Data retention, Endurance characteristics and demonstrates the use of single-poly FGDs in analog applications. Chapter 5 discusses the MATLAB simulation model developed for analyzing the time dependence characteristics of the single-poly FGDs and compares the simulation and experimental results. Finally, Chapter 6 summarizes the unique contributions of this thesis followed by future work.

Chapter 2

Basic Cell Structure and Physics of Operation

The first few sections in this chapter focus on the basic structure of the single-poly FGDs developed in PDSOI process and the various configurations like programming, deprogramming, and sensing. The latter sections compare the different methodologies for configuring the single-poly FGD's.

2.1 Basic structure of single-poly FGD

The basic structure of the single-poly FGD in bulk CMOS process is shown in Figure 2.1. The source, body and drain of the PMOS transistor form the 'control gate' of the FGD, while the source and drain of the NMOS transistor form the 'source' and 'drain' of the FGD, respectively. The single-poly FGD structure in a PDSOI process is shown in

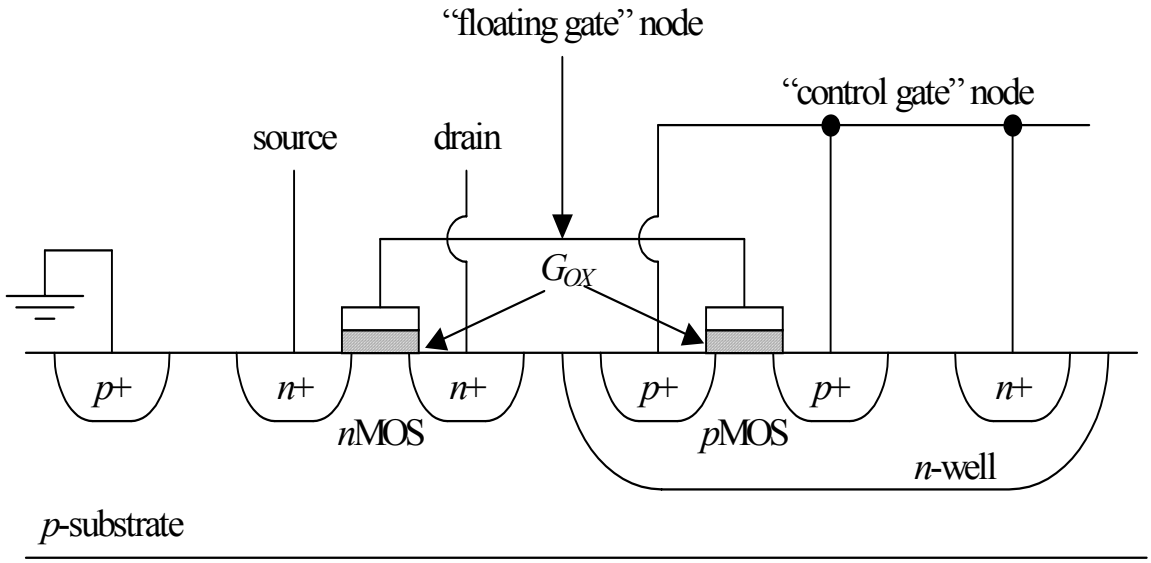


Figure 2.1: Basic Structure of FGD in bulk CMOS process

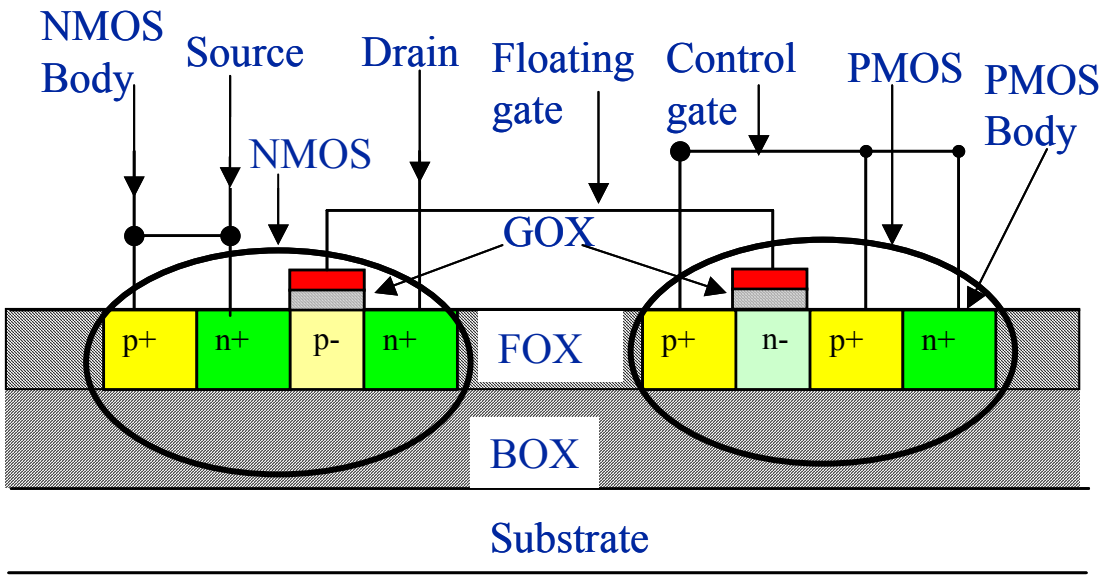


Figure 2.2: Basic Structure of single-poly FGD in PDSOI process

Figure 2.2. This cross-section is similar to the CMOS inverter except that the gate terminal is floating. The terminal assignments are similar between the two processes. The capacitance associated with each PMOS and NMOS gate form a capacitive voltage divider between the control gate and the source/drain of the single-poly FGD. Since the common gate (floating gate) is left unconnected, there is no discharge path for the charge present on the floating gate. By application of a high electric field at either the 'control gate' or the 'source' and 'drain' of the FGD, electrons can be tunneled through the NMOS gate oxide (GOX) onto or off of the floating gate [2]. Holes can also be used for tunneling as demonstrated in [2]. Since the mobility of the electrons is higher than holes, the field necessary to move the electrons onto/off the floating gate is less than that required to move the holes [2], [4]. Hence electrons are generally chosen for the charge transfer mechanism. The primary difference between bulk CMOS FGDs and PDSOI FGDs is the presence of a buried oxide layer (BOX) isolating the substrate from the transistors. For

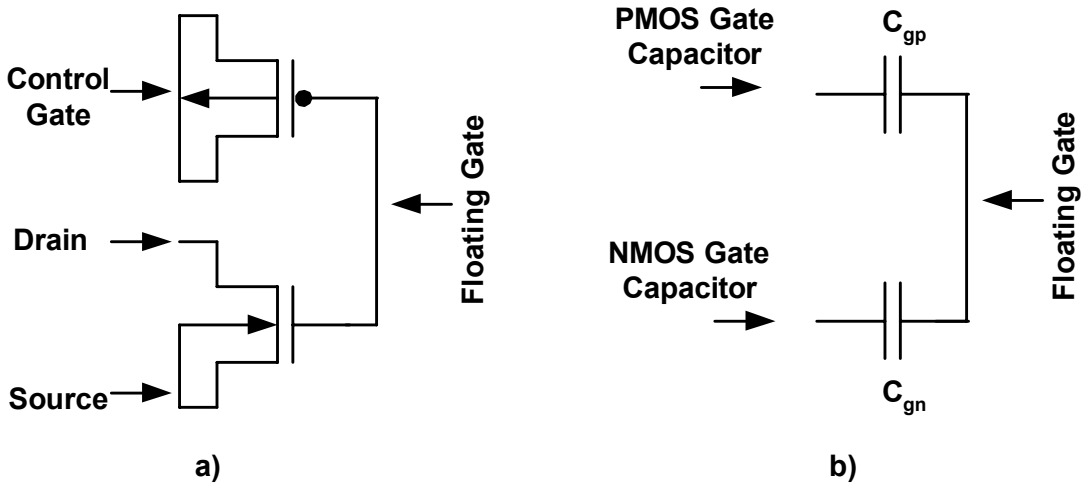


Figure 2.3: General FGD schematics a) Transistor level b) Equivalent Capacitive network

clarity, both the transistor level and equivalent capacitor network schematics for the single-poly FGD are provided in Figure 2.3.

2.2 Modes of Operation

The scope of this thesis addresses three modes of operation of the single-poly FGD: (a) programming, (b) deprogramming/erasing, and (c) sensing or reading.

2.2.1 Programming Mode

The schematic for programming the single-poly FGD is shown in Figure 2.4. The programming mode injects the charge (electrons through the NMOS GOX) onto the floating gate subsequently increasing the threshold voltage of the single-poly FGD. This charge injection mechanism used in this work is known as Fowler-Nordhiem (FN) Tunneling [7]. The simplified schematic for programming is shown in the Figure 2.5.

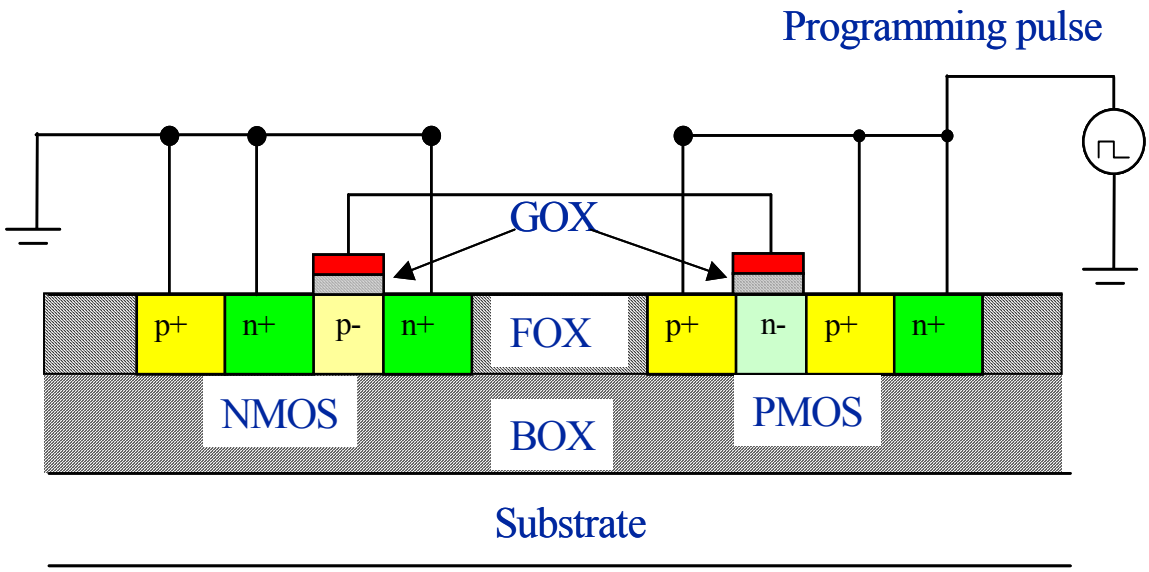


Figure 2.4: Schematic for Programming Operation

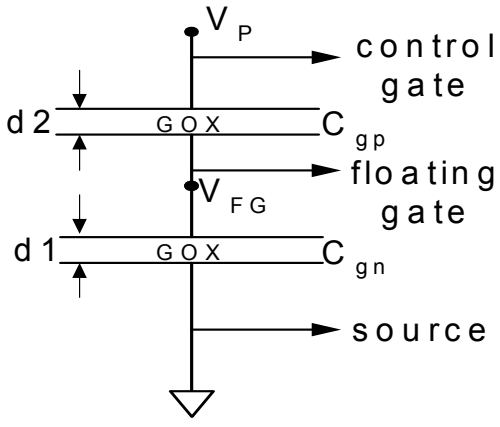


Figure 2.5: Capacitors in series

The single-poly FGD's threshold voltage (V_{TH}) is defined as the NMOS threshold voltage as seen from the control gate. To achieve the required potential at the floating gate to induce FN tunneling during programming, C_{gn} needs to be smaller than C_{gp} to maximize V_{FG} for a given V_P and vice-versa during erasing. For the single-poly FGD structure used in this work, this would require that the gate area (Wn X Ln) of the NMOS to be less than the PMOS gate area (Wp X Lp). When the programming pulse (V_P) is applied to the control gate, V_P is divided down based on the capacitor divider network:

$$V_{FG} = \left(\frac{C_{GP}}{C_{GP} + C_{GN}}\right) \times V_P = \left(\frac{1}{1 + \frac{C_{GN}}{C_{GP}}}\right) \times V_P \qquad 2.1$$

The large potential at the floating gate attracts the electrons from the n+ diffusions of the NMOS transistor, which get trapped on the floating gate causing a shift in the FGD's threshold voltage. From the FN Tunneling equation (discussed in Section 2.3.2), it can be observed that the programming current density through GOX is negligible for normal operating voltages. Hence FN tunneling is not observed during regular MOS transistor operation. The minimum field necessary across the NMOS GOX of the FGD for FN tunneling is 6.4MV/cm [5]. The long-term reliability (constant field) suggests the applied field to be within 7MV/cm [4], but a field as high as 10MV/cm is applied during this work, since the field is momentary (applied for a few μ seconds).

2.2.2 Deprogramming/Erasing Mode

The schematic for deprogramming is shown in Figure 2.6. During deprogramming, an erase pulse is applied to the drain/source terminals to attract the electrons present on the

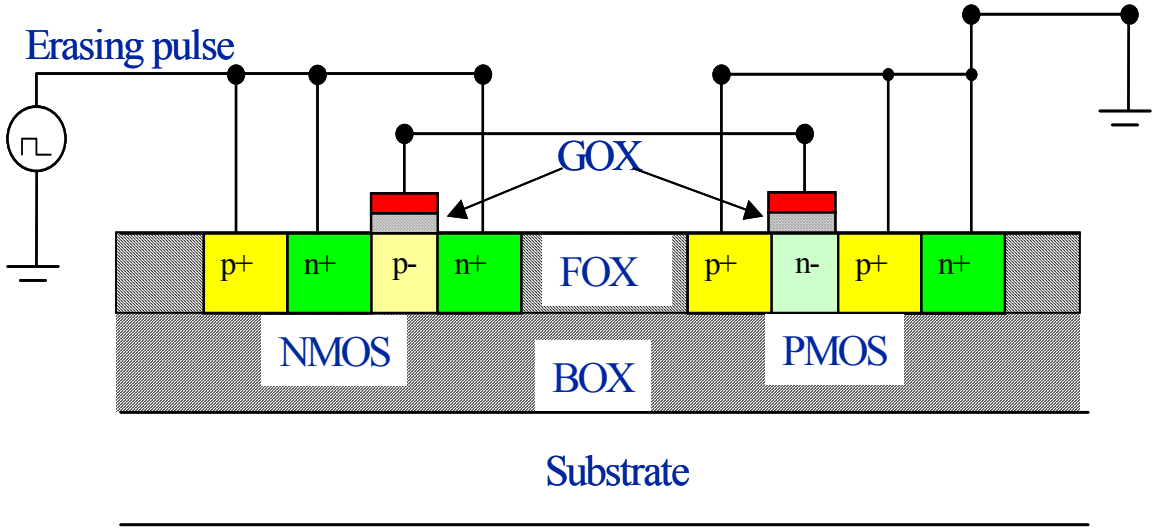


Figure 2.6: Schematic for Deprogramming Operation

floating gate to tunnel back through the NMOS gate oxide and into the NMOS channel region (given sufficient amplitude deprogramming pulse), thereby reducing the FGD's threshold voltage. The physics for both programming and deprogramming modes is concisely discussed in Section 2.3.2.

2.2.3 Sensing/Reading Mode

The sensing/reading mode is used for extracting the desired data from the single-poly FGD. This was tested using the HP4145B (Semiconductor Parameter Analyzer) in conjunction with Labview. During this mode, the FGD can be treated as a regular transistor, and the parameters of interest such as threshold voltage or on-resistance are extracted. The schematic for this mode is shown in Figure 2.7.

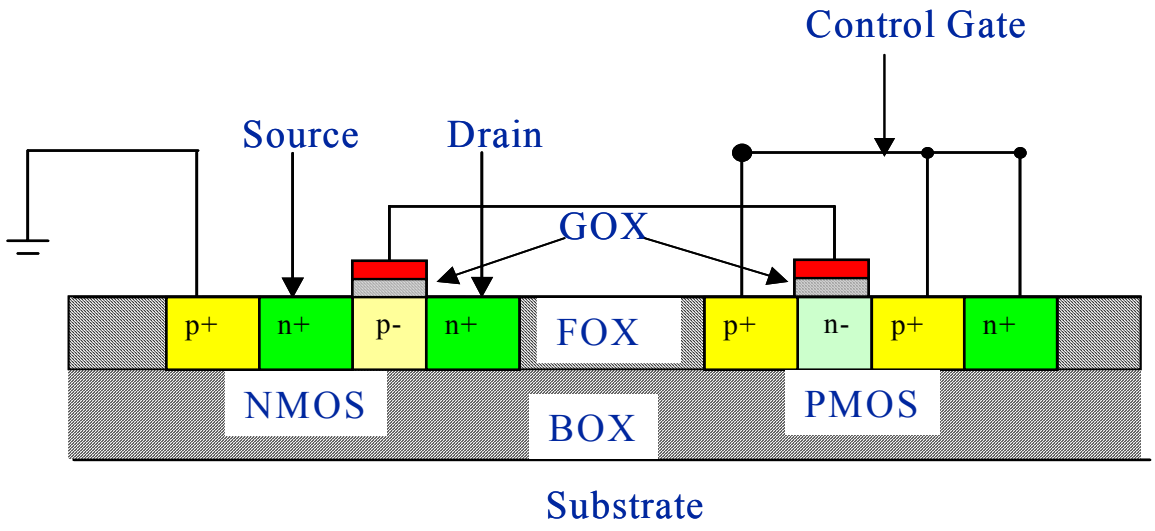


Figure 2.7: Schematic for Sensing/Reading Mode

2.3 Physics of Operation

There are two commonly used charge transfer mechanisms to program/deprogram the FGDs: (a) Channel Hot Electron injection (CHE) and (b) Fowler-Nordhiem Tunneling (FN tunneling).

2.3.1 Channel Hot Electron Injection (CHE)

This method is also known as Hot Carrier Injection (HCI) or impact ionization. The principle of operation is that charge carriers in the inversion channel of a normal MOS transistor, if sufficiently excited, pierce through the gate oxide and get trapped on the floating gate [17]. Though there are different procedures to excite electrons to cross the energy barrier associated with the gate oxide, acceleration of electrons by application of a lateral electric field (for example, V_{DS} applied to a MOSFET) is the hot electron injection technique widely used when dealing with EEPROMs. This technique requires pulsing the

drain with a sufficiently high amplitude V_{DS} pulse, such that electrons near the drain side of the NMOS inversion layer (formed by biasing the control gate) may tunnel through GOX onto the floating gate. The tunneling rate cannot be accurately predicted with this technique. This mechanism needs large number of charge carriers in the inversion layer so as to increase the charge trapped onto/off the floating gate, thereby changing the V_{TH}. The use of hot-hole injection is another similar technique but is very inefficient due to the small quantities of charge transfer onto/off the floating gate compared to HCI. This technique may not be applicable to the devices manufactured using modern processes due to the inclusion of lightly doped drain (LDD) structures during fabrication. LDD structures help counteract the short channel effects as the device feature sizes continue to shrink [4].

2.3.2 Fowler-Nordhiem Tunneling (FN tunneling)

Fowler-Nordhiem tunneling is a non-linear programming/erasing technique introduced by Fowler and Nordhiem in 1928. During programming/erasing, the field present on the floating gate excites the charge in the inversion layer to tunnel through the gate oxide onto/off the floating gate. The primary difference between the CHE and FN tunneling is that the CHE uses much higher current from the programming pulse while the FN tunneling requires higher voltage (higher V_P) from programming pulse. The ease of implementation associated with high-voltage pulse generation on-chip (e.g. using charge pump circuits [11-12]), coupled with low power requirements, prompted the decision to use FN tunneling in this work.

Fowler-Nordhiem Tunneling is described by:

$$J = A \times E^2 \times \exp\left(-\frac{E_0}{E}\right) \quad 2.2$$

Where constants A = 2μA/(v-cm)^2 and E_0 = 2.38 x 10^8 V/cm (for SiO_2), while J is the current density and E is electric field across the oxide.

Referring to the Figure 2.5,

$$V_{FG} = \frac{V_p}{d1 + d2\left(\frac{A_1}{A_2}\right)} \quad 2.3$$

Where d1 and d2 denote the oxide thickness, while A_1 and A_2 denote the areas of the capacitor plates of the NMOS and PMOS respectively. From Equation 2.1 and Equation 2.3, it can be understood that C_{gn} needs to be smaller than C_{gp} to improve tunneling. This principle is the basis for all of the configuration mechanisms used throughout this thesis. The low electric field required to cause tunneling through the gate oxide is the primary reason for adopting this technique.

When a sufficiently large electric field is applied across the polysilicon-SiO_2-Si structure, electrons in the silicon conduction band see an energy barrier whose width is dependent upon the applied field. Figure 2.8 shows energy band diagram of the Si/SiO_2 interface with a without applied field [7]. At sufficiently high fields, the width of the barrier becomes small enough for electrons to tunnel through the silicon conduction band into the oxide

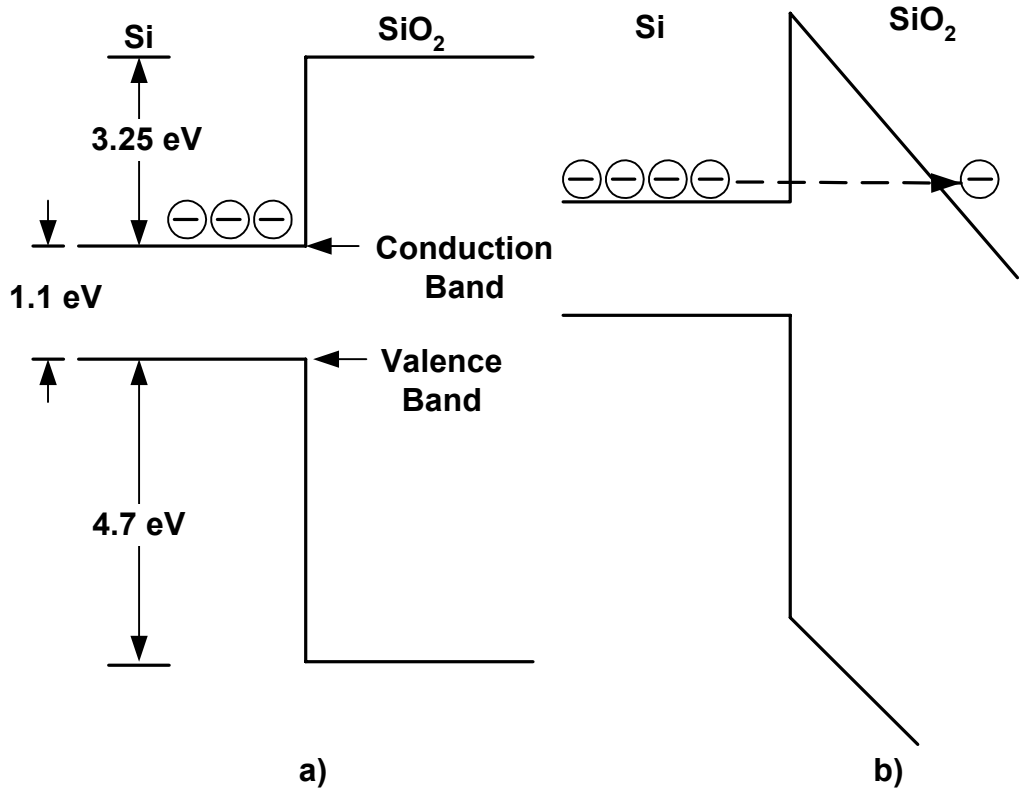


Figure 2.8: Energy band diagram of Si/SiO_2 interface a) with b) without applied field

conduction band. This principle was observed by Fowler and Nordhiem for the case of electrons tunneling through the vacuum barrier. Lenzlinger and Snow described this mechanism for oxide tunneling [37].

Chapter 3

Analysis and Characterization of SOI Single-Poly Floating Gate Device

This chapter discusses the characterization procedures for the estimation and analysis of various performance parameters associated with the single-poly FGDs fabricated in 0.35μm PDSOI process. Early sections in this chapter discuss the dependence of the single-poly FGD's threshold voltage (V_{TH}) on parameters such as programming/erasing (p/e) duration and p/e pulse amplitude, followed by the on-resistance (R_{on}) variation with V_{TH} and p/e duration, hysteresis of the FGD's R_{on}, and the temperature coefficient (TC) of the SOI single-poly FGD's V_{TH}. Characterization of devices with different gate capacitance ratios (C_{gp}/C_{gn}) are compared and analyzed. The C_{gp}/C_{gn} ratios of the SOI single-poly FGDs used during this characterization effort range from 1/4 to 4 and are listed in Table 3.1. Each FGD uses a gate length of 0.4μm.

Table 3.1: SOI single-poly FGD sizing (PMOS vs. NMOS and C_{gp}/C_{gn} ratios) included in this study

Device No.	**PMOS(W/L, μm/μm)**	**NMOS(W/L, μm/μm)**	**C_{gp}/C_{gn}**
1	1.8/0.4	0.9/0.4	2
2	3.6/0.4	0.9/0.4	4
3	0.9/0.4	1.8/0.4	1/2
4	3.6/0.4	1.8/0.4	2
5	7.2/0.4	1.8/0.4	4
6	0.9/0.4	3.6/0.4	1/4
7	1.8/0.4	3.6/0.4	1/2
8	1.8/0.4	7.2/0.4	1/4

The definitions of the commonly used terms in this thesis will now be reviewed.

Programming/Erasing pulse: a single pulse with a given peak-peak amplitude and frequency (pulse duration). This is generated using the HP33120 signal generator and the MC34072 dual operational amplifier. Additional details are provided in Appendix B. Figure 3.1 shows an ideal programming/erasing pulse.

Pulse amplitude: the peak-peak (pk-pk) value of the programming/erasing pulse.

Pulse duration: the duration of the pulse width at the p/e pulse amplitude. Both the pulse amplitude and pulse duration are illustrated in Figure 3.1.

Before presenting the experimental results of this work, it is appropriate to comment on the experimental procedure. During these experiments on the SOI single-poly FGD, the p/e pulse amplitudes were not kept constant between FGDs used for comparison (refer to Section 3.3) purposes. The primary purpose of this thesis, however is to evaluate the versatility of the single-poly FGD in a PDSOI process as a regular transistor, resistive element, or memory element so that FGD can be used in designing high performance or specialized circuits. Ideally the p/e pulse amplitude should be maintained constant for comparison purposes between FGDs.

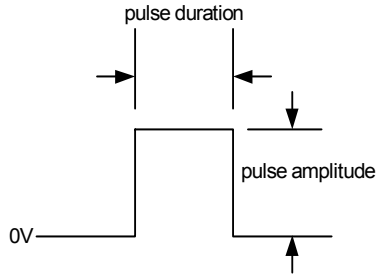


Figure 3.1: Ideal programming/erasing pulse

But, it is important to realize that if a constant pulse amplitude is used for FGDs with different C_{gp}/C_{gn} ratios, the device with smaller C_{gp}/C_{gn} ratio needs longer time duration p/e pulses for achieving a comparable shift in V_{TH}. Instead if the pulse amplitude used throughout the experiment is increased, the V_{TH} shift in the devices with large C_{gp}/C_{gn} ratio reaches saturation even for small p/e pulse widths. When large p/e pulse amplitudes are applied, the V_{TH} shift can be reduced by reducing the p/e pulse duration (width). The p/e pulse duration cannot be reduced beyond a limit set by the function generator (HP33120A) used as the signal source and the slew rate of the operational amplifier (MC34072) in this work driving the FGD control gate. Hence, different pulse amplitudes have been used for different devices in this thesis.

3.1 Threshold voltage vs. programming/erasing duration

This section discusses the variation of the single-poly FGD's V_{TH} with p/e duration for a given pulse amplitude. Figures 3.2 and 3.3 show the I_D versus V_{CG} characteristics of a SOI single-poly FGD. This is to demonstrate the regular MOS transfer characteristics of the single-poly FGD. Each curve in Figure 3.2 and Figure 3.3 represents a measured transfer characteristic when the device is programmed to a different V_{TH}. In Figure 3.2, the initial V_{TH} of the device (#6) is approximately -2.1V. When a single 11.0V amplitude programming pulse is applied, it shifts the V_{TH} of the device to -2.0V. This curve is labeled as 'pulse #2' in the Figure 3.2. The last curve (indicated by 'pulse #32') shows that the single-poly FGD is operating in enhancement-mode with a V_{TH} of 2.1V. Throughout this experiment, the programming pulse amplitude and the other biasing conditions are maintained constant. To achieve an almost linear shift in V_{TH} between programming

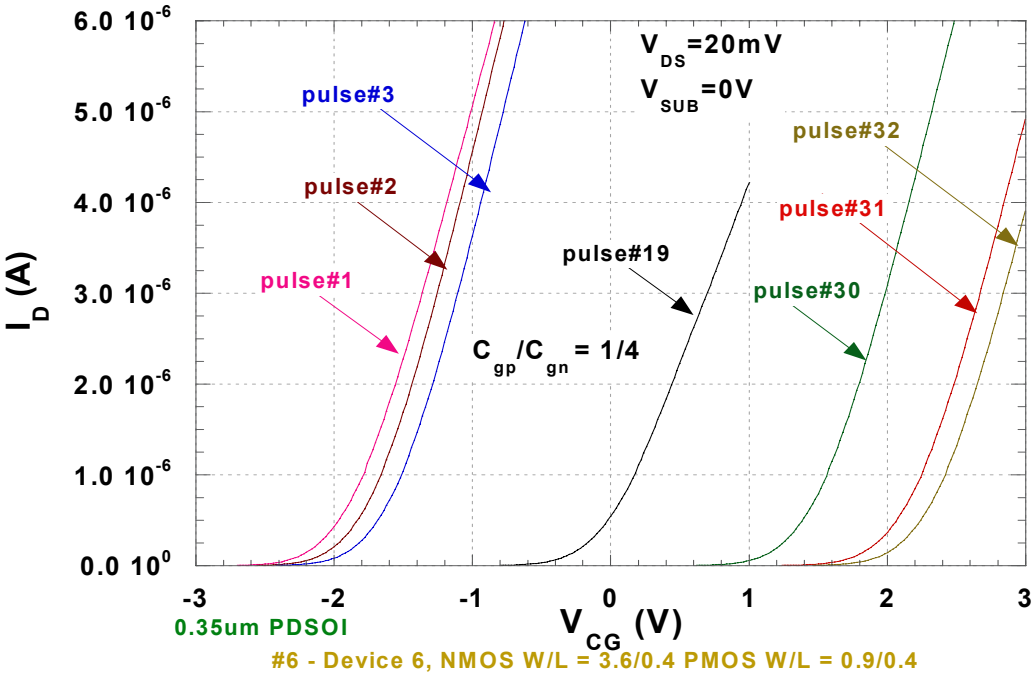


Figure 3.2: Programming I_D-V_{CG} curves of FGD #6 using 11V pulses

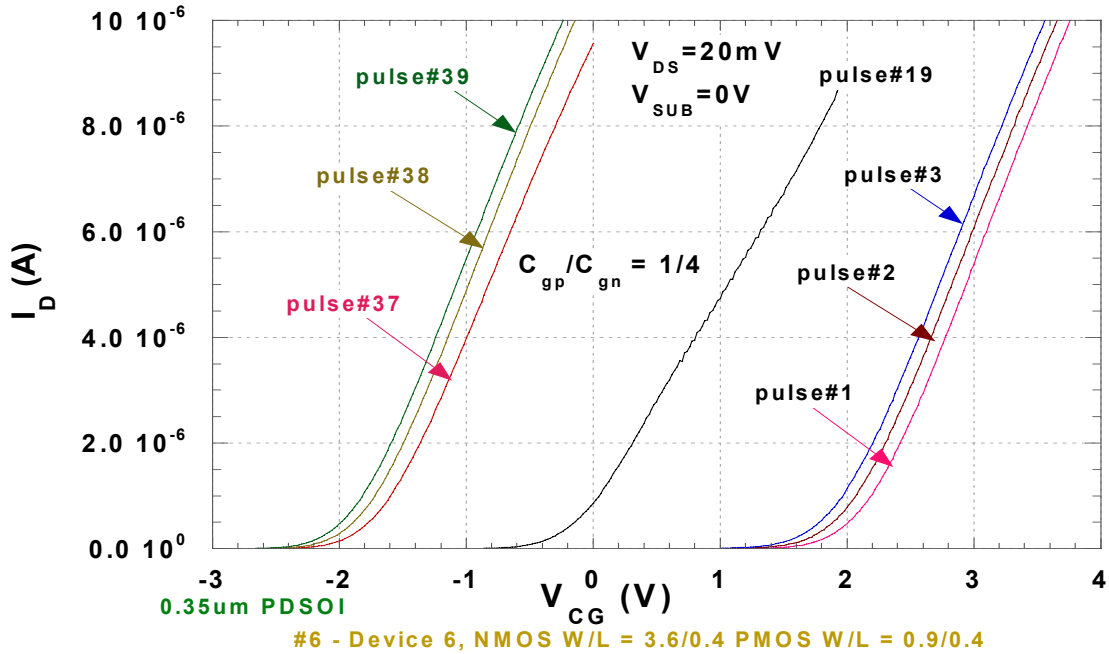


Figure 3.3: Deprogramming I_D-V_{CG} curves of FGD #6 using 12.8V pulses

pulses, the pulse duration is varied across pulses. The more a given FGD is programmed, the longer the individual programming pulse durations need to be, in order to maintain similar shift in V_{TH}. In other words, FGD #6 required 11.0V amplitude pulses with 15μsec. pulse duration for a V_{TH} shift of 240mV from -1.97V to -1.73V. But after a series of 30 programming pulses is applied, a 100μsec. duration pulse (same amplitude, 11V) could generate a V_{TH} shift of only 160mV from 2.13V to 2.29V. These observations were made when the device is being programmed from depletion-mode to the enhancement-mode. A similar experiment was conducted while deprogramming the same device from V_{TH}=2.29V to V_{TH}=-2.0V and the results are shown in Figure 3.3. Results with different C_{gp}/C_{gn} ratios are available in Appendix A. This demonstrates the SOI single-poly FGD's capability to function as a regular MOSFET both in enhancement and depletion modes. Figure 3.4 shows that the FGD V_{TH} saturates for a given pulse

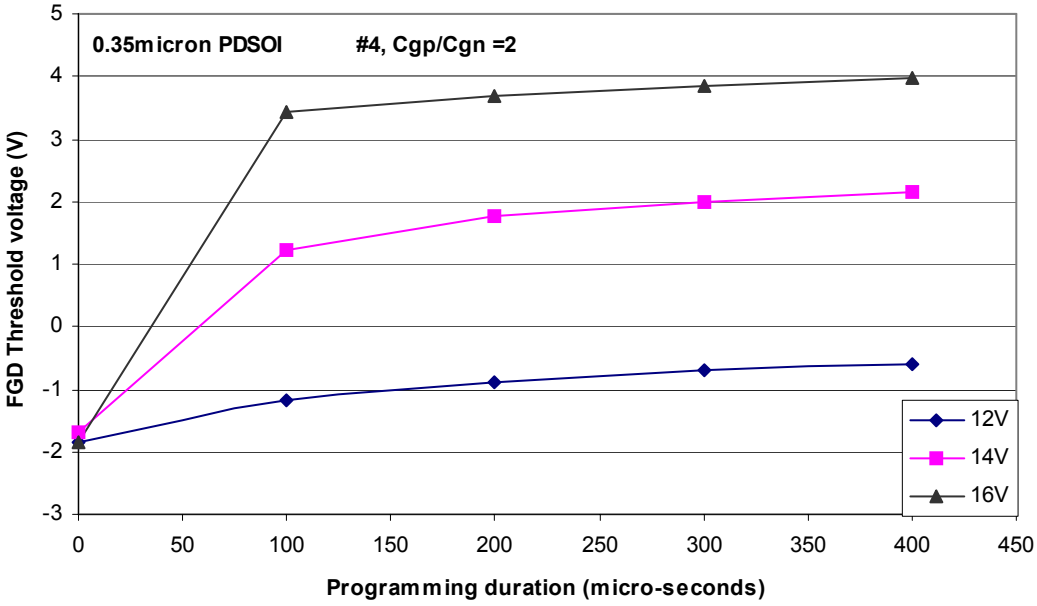


Figure 3.4: Measured FGD V_{TH} variation for different pulse amplitudes applied to FGD #4

amplitude during programming likely due to the charge build-up on the floating gate. As the device is programmed/erased, the charge tunnels onto/off the floating gate which counteracts the potential available on the floating gate to cause tunneling. Hence for a given pulse amplitude, there is an upper limit on the V_{TH}. As the FGD approaches the limits of programmability, it becomes increasingly difficult to further enhance/deplete the floating gate. Then, higher pulse amplitudes are required for further p/e, implying that the programmable V_{TH} range increases with an increase in pulse amplitude and vice versa. For example, the total V_{TH} shift was measured to be 4.34V when 12V amplitude pulses were applied, compared to 9.79V when 15V amplitude pulses were used. This results from the variation in the injection current density due to changes in the field potential applied to the control gate. As the FGD is continually programmed/erased, some of the p/e charge gets trapped in the insulator medium (NMOS gate oxide of the single-poly FGD) while tunneling. This is often referred to as trap-up. This causes permanent damage to the gate oxide. During this work, trap-up was overcome by increasing the pulse amplitude. The tunneling rate can be increased by increasing the pulse amplitude, but it is a trade off between programming speed and the endurance characteristic, (discussed later in Chapter 4) i.e., with the increase in the pulse amplitudes, SiO_2 will continually become more damaged. Section 2.3 reviewed the physics of operation for these FGDs and the upper and lower limits of the field that can be applied to the control gate. These limits are given by [4, 18]

$$6.4\frac{MV}{cm} \le E_F \le 10\frac{MV}{cm} \Rightarrow 6.4\frac{MV}{cm} \times T_{OX} \le V_{P/E} \le 10\frac{MV}{cm} \times T_{OX} \qquad 3.1$$

where T_{ox} is the gate oxide thickness of the process, $V_{P/E}$ denotes p/e pulse amplitude, and E_F represents the field applied across the NMOS gate oxide of the single-poly FGD.

For a given pulse amplitude, the total shift in the FGD V_{TH} depends on the total pulse duration. For example, 19 pulses totaling 165μsec. duration caused a shift of 2.3V in FGD #6 during erasing from 2.3V down to 0.0V. Aslo a single 165μsec. wide pulse caused a similar shift in V_{TH} if the pulse amplitude remained constant. Referring to the two sets of programming pulses in Figure 3.5, the shift in FGD V_{TH} is the same for both cases. This shows that the FGD V_{TH} shift is dependent on the total pulse duration for a given pulse amplitude. As seen from the Figure 3.6, the V_{TH} variation trend remains the same for a FGD (#5 in this case) with a different shape factor (different C_{gp}/C_{gn} ratio). Interestingly the V_{TH} variation with time duration trend is observed for different pulse amplitudes. For example, 3 different pulse amplitudes (12V, 14V and 16V) were applied to two different FGDs (#4 and #5) and the same trend was observed. (see Figure 3.4 and Figure 3.6).

It can be concluded that (a) for a given V_{TH}, the SOI single-poly FGD behaves as a regular MOS transistor with respect to its transfer characteristic, (b) there are limits on the programmable/erasable V_{TH} for a given pulse amplitude (the single-poly FGD has an upper limit on the V_{TH} during programming, and vice-versa), (c) for a given pulse amplitude, the FGD V_{TH} saturates with programming/erasing pulse duration, and (d) shift in V_{TH} depends on the total pulse duration for a given pulse amplitude.

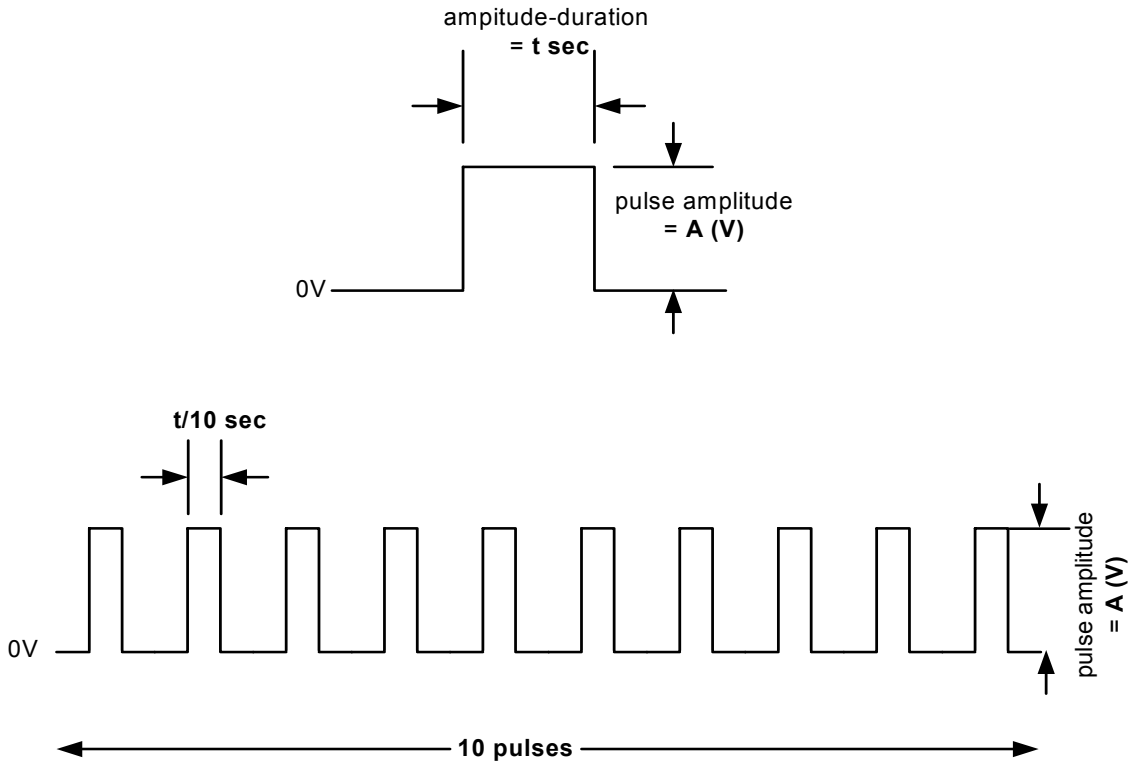


Figure 3.5: Illustration of one pulse and multiple pulses with same total duration

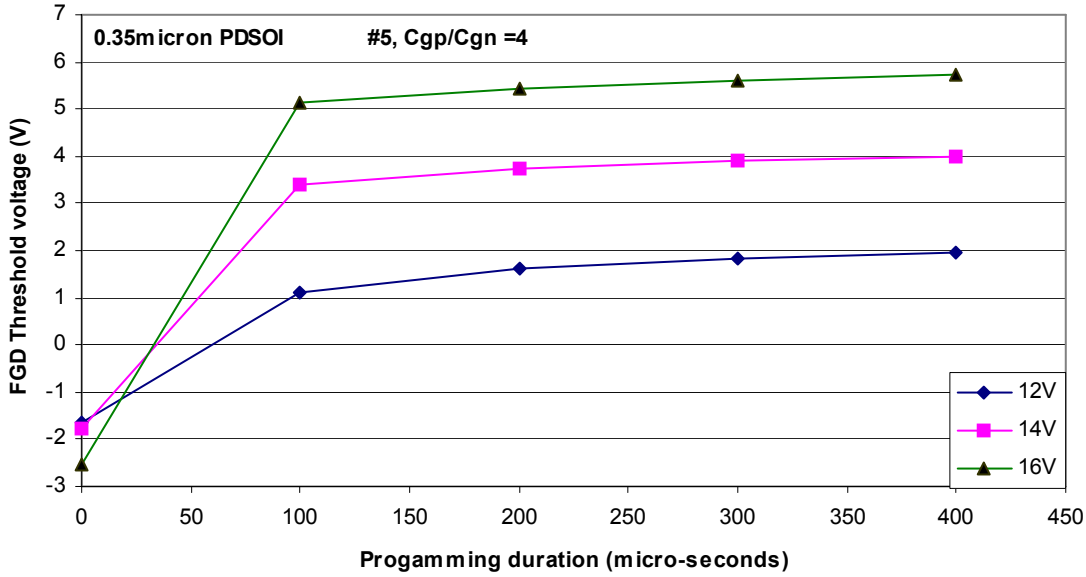


Figure 3.6: Measured FGD V_{TH} variation for different pulse amplitudes applied to FGD #5

3.2 Temperature Coefficient (TC) of the Threshold Voltage

According to [4], the V_{TH} temperature sensitivity (TC x V_{TH}) of a typical n-type MOSFET is -2.4mV/° C. Figure 3.7 shows the V_{TH} variation with temperature from 25° C to 125° C, when the single-poly FGD #4 is configured in both enhancement (positive V_{TH}) and depletion-mode (negative V_{TH}). This experiment started with the assumption that dV_{TH}/dT remains independent of V_{TH}. The device is initially programmed to 2.6V. Threshold voltage is measured at five close-in temperatures centered around every primary temperature point of interest. This enhances the accuracy of measurement results (a local derivative must be calculated). The slope of each curve gives the threshold voltage sensitivity for a given FGD V_{TH}. The results show that the V_{TH} sensitivity does not remain constant for different threshold voltages. Instead, the threshold voltage temperature sensitivity decreases with V_{TH} value.

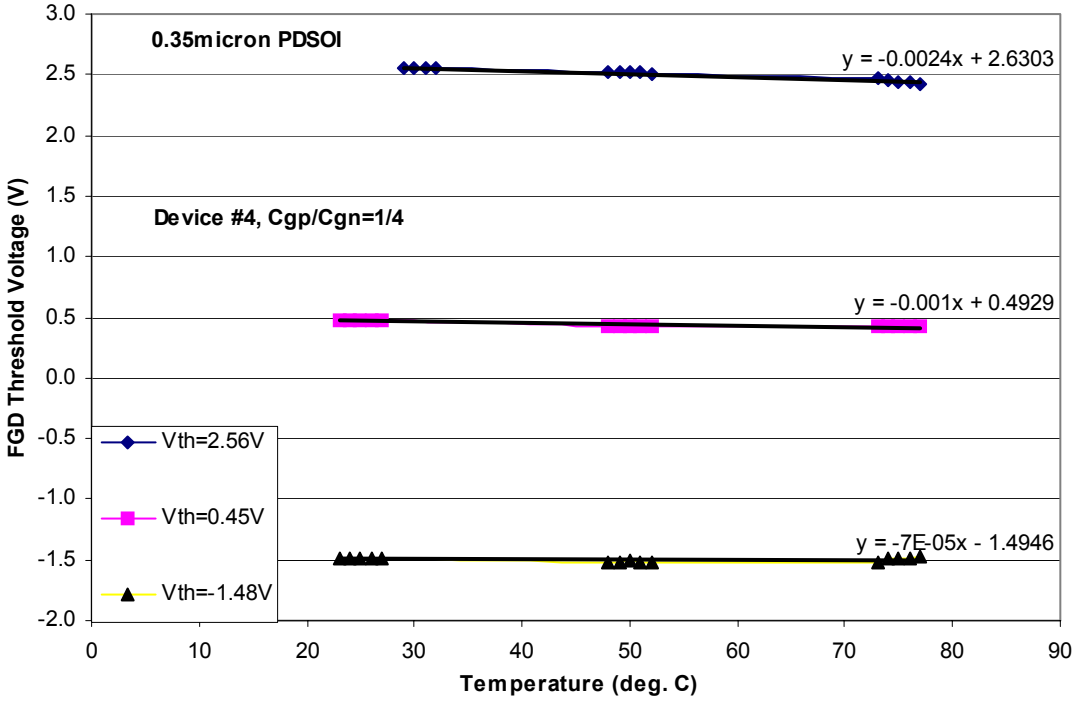


Figure 3.7: V_{TH} sensitivity with Temperature

Table 3.2 shows the V_{TH} sensitivities for different C_{gp}/C_{gn} ratios at different threshold voltages. This feature of different V_{TH} sensitivities for different threshold voltages can be taken advantage of while designing temperature independent reference generators like a beta-multiplier current reference, i.e. the device can be programmed to the V_{TH} with desired TC, as to obtain the desired system level TC (normally Zero). Figure 3.8 shows the variation of TC with V_{TH} for a single-poly FGD at 50° C.

From these experiments, it can be concluded that (a) threshold voltage sensitivity decreases with V_{TH} (b) FGD can be used in designing programmable TC circuits.

Table 3.2: V_{TH} sensitivities for enhancement and depletion modes and C_{gp}/C_{gn} ratios

FGD V_{TH} (V)	**FGD No.**	**Cgp/Cgn**	**V_{TH} sensitivity (dV_{TH}/dT) mV/°C**
2.56	4	2	-2.40
1.69	4	2	-2.20
0.45	4	2	-1.00
-0.60	4	2	-0.60
-1.48	4	2	-0.07
-2.50	4	2	-0.70
2.94	6	1/4	-3.00
2.54	4	2	-2.30
2.00	5	4	-2.20
1.30	5	4	-2.80
-0.75	5	4	-0.90
-1.16	4	2	-0.4
-1.6	4	2	-1.00
1.57	5	4	-2.60

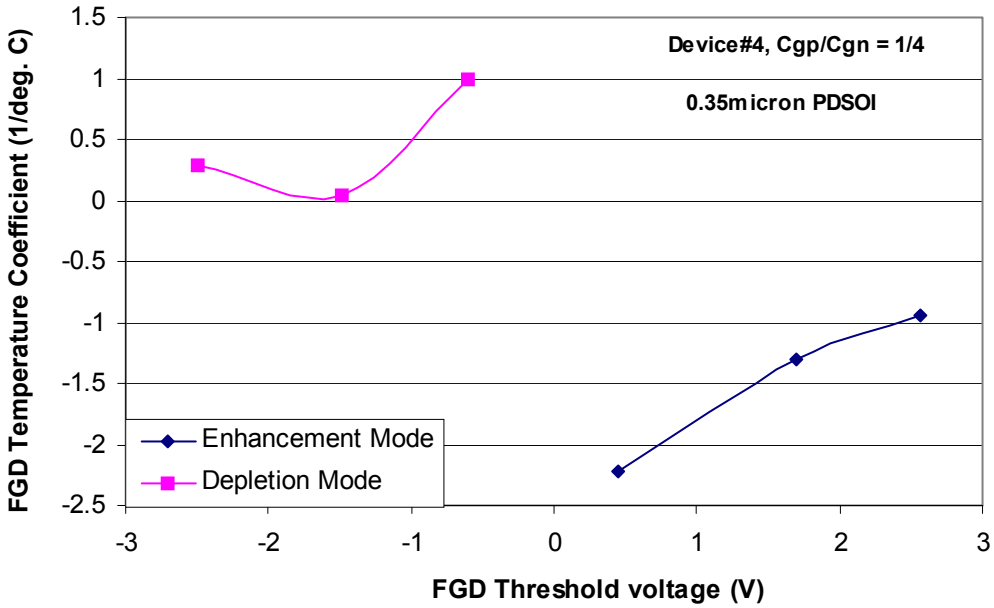


Figure 3.8: Temperature co-efficient vs. Threshold voltage of the FGD at 50° C

3.3 On-resistance variation with Threshold Voltage

This section deals with the dependence of on-resistance on the threshold voltage offered by the single-poly FGD when operating in depletion mode. The purpose behind this experiment was to evaluate the single-poly FGD as a resistive element and its characteristic variation with V_{TH} and programming duration. Figure 3.9 shows the variation of R_{on} while the V_{TH} of the devices is varied from -2.0V to 0.0V. The on-resistance varies almost inversely with threshold voltage for both the devices (#5, #6). Similarly Figure 3.10 shows that erasing the FGD from 0.0V also shows a similar relationship between the R_{on} and V_{TH}.

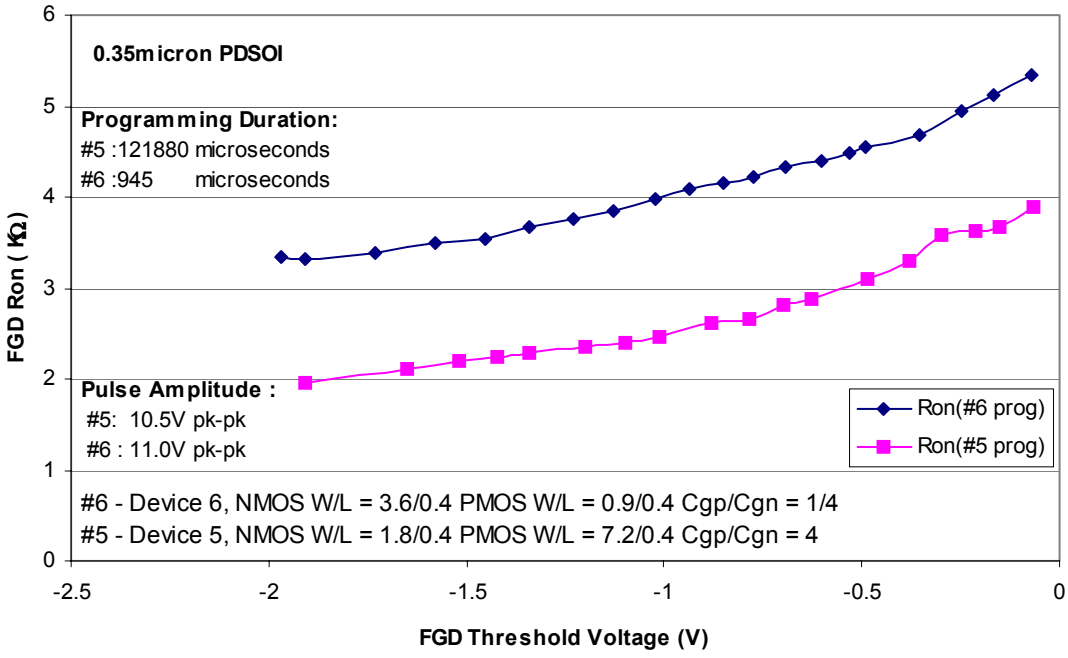


Figure 3.9: Measured FGD R_{on} vs. V_{TH} for FGD (#5, #6) during programming

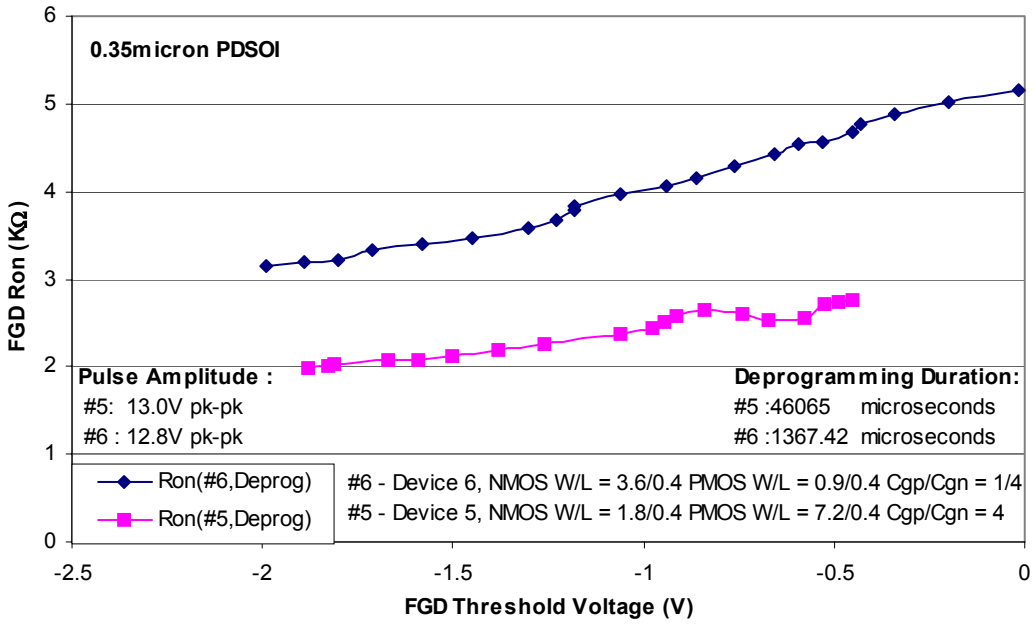


Figure 3.10: Measured FGD R_{on} vs. V_{TH} for FGD (#5, #6) during erasing

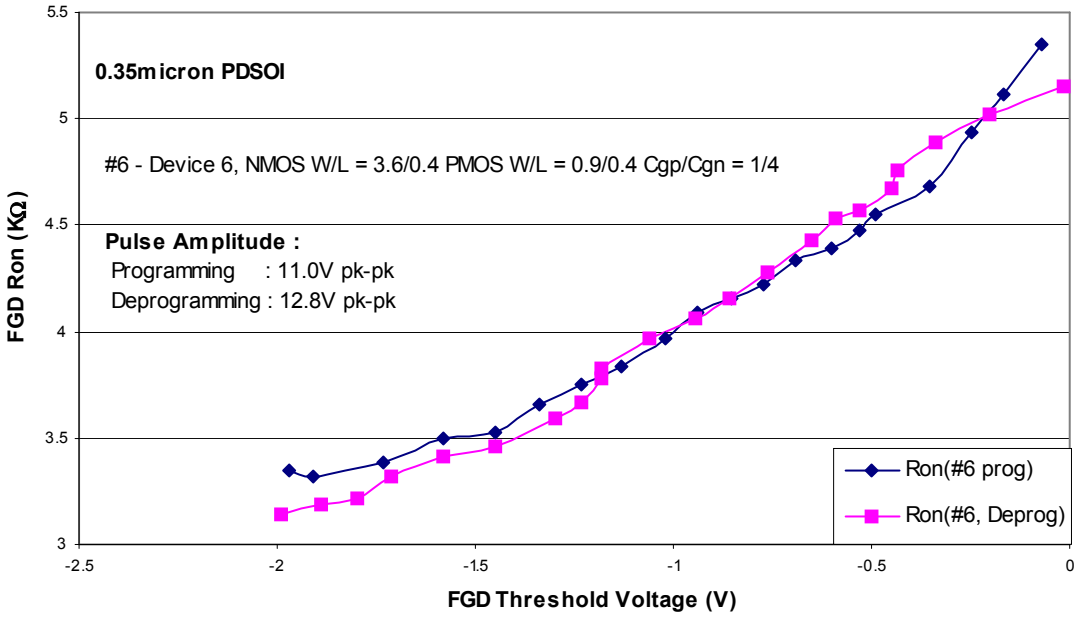


Figure 3.11: Hysteresis of On-Resistance vs. Threshold voltage (#6)

Figure 3.11 displays the response of the FGD (device #6) during both programming and erasing, and therefore hysteresis of R_{on}. Hysteresis defines the history dependence of a characteristic in a system, i.e. dependence of the current behavior based on the past behavior. The primary reason for the non-linearities observed in both of these curves might be because both the threshold voltage and the on-resistance parameter values are extracted manually from I-V curves. Hysteresis graphs for devices with different shape factors are available in Appendix A. A simple mathematical relation has been experimentally derived between the R_{on} and V_{TH} using a curve fitting approach:

$$R_{on}' = (1.09 \times V_{TH}) + R_{on} \qquad 3.2$$

Where R_{on}' is the desired on-resistance, V_{TH} is the threshold voltage at the desired on-resistance (V_{TH} <0), and R_{on} is the known on-resistance. If the present R_{on} and the desired R_{on} are known, then V_{TH} at the desired R_{on} can be calculated and the FGD can

Table 3.3: Single-Poly FGD's R_{on} vs. C_{gp}/C_{gn} ratio

Device No.	Cgp/Cgn	Resistance (Kilo Ohms)
4	2	< 2.2
5	1/2	< 3.6
6	4	< 4.0
7	1/4	< 5.1

be configured to the appropriate V_{TH} to get the desired R_{on}. The graph depicts a maximum error of 3.8% in R_{on} from the mathematical relation derived above. This shows that the hysteresis is very small for the R_{on} with threshold voltage. Table 3.3 gives the range of resistance values that can be offered by different SOI single-poly FGDs.

In conclusion, (a) a mathematical relation between the on-resistance and the thresold voltage has been extracted experimentally, (b) there is an upper limit on the R_{on} i.e. the R_{on} of the single-poly FGD depends on V_{TH} and it was determined that there is an upper limit on the V_{TH} , and (c) single-poly FGD satisfies the relation between R_{on} and V_{TH} of regular MOS transistor.

In summary, (a) there are limits on the threshold voltage of the FGD for a given pulse amplitude, (b) shift in threshold voltage depends on the total pulse duration, (c) dV_{TH}/dT of the single-poly FGD decreases with V_{TH}, (d) a mathematical relation has been extracted between the on-resistance and threshold voltage, and (e) there is a limit on the range of on-resistance offered by the single-poly FGD. The next chapter characterizes the SOI single-poly FGD as a memory element and demonstrates a practical application.

Chapter 4

Memory Characterization and Applications of the FGD

FGDs have been primarily used as the nonvolatile memory elements since the 1960's. The primary characterization parameters of the nonvolatile memory elements are data retention and endurance. The literature search did not show any evidence of the fabrication of single-poly FGDs in PDSOI process. The chapter starts with the estimation and analysis of Data Retention, followed by a discussion on the advantages and disadvantages of using single-poly FGDs as memory and resistor elements in analog applications. Later, as a practical application, a programmable beta-multiplier current reference circuit is presented, using the single-poly FGD as a resistive element in SOI. Due to the practical complexity of implementation, endurance is yet to be determined.

4.1 Data Retention

Retention failure refers to the inability of the floating gate to retain stored charge over a wide range of temperature variations and operating voltages. There are two types of data retention: (a) Intrinsic (b) Extrinsic [7]. Intrinsic data retention is the innate capability of the cell [17]. Normally, the intrinsic data retention is 100's or 1000's of years. Extrinsic data retention is a function of endurance and the applied electrical/mechanical stress [17]. The electrons get tunneled through the gate oxide during programming/erasing. Some of the electrons get trapped in the tunnel oxide, building up a negative charge in the insulator medium, thereby causing permanent impact on the electric field at the floating gate and the tunneling current density. The various data loss mechanisms caused by this include

electron transport to and from the floating gate through oxide defects, compensation of stored charge by ionic contamination in the tunnel, and intrinsic mechanisms that cause even non-defective cells to lose charge over time [7,17]. Other than these, programming/ erasing pulse amplitudes may disturb the stored charges resulting in retention failure. Figure 4.1 shows the intrinsic data retention characteristics of the SOI single-poly FGD. It is clearly seen that the charge loss is logarithmic in nature. The procedure for the estimation of intrinsic data retention will now be described: The EEPROM would be configured to a specific threshold voltage and exposed to 85°C. Later the threshold voltage of the device is measured at regular intervals of time. To estimate the data retention, a V_{TH} variation window must be considered. The window size determines the best and worst-case scenario i.e. a smaller window size gives a longer data retention while a larger window size gives smaller data retention value. The window size of 1V

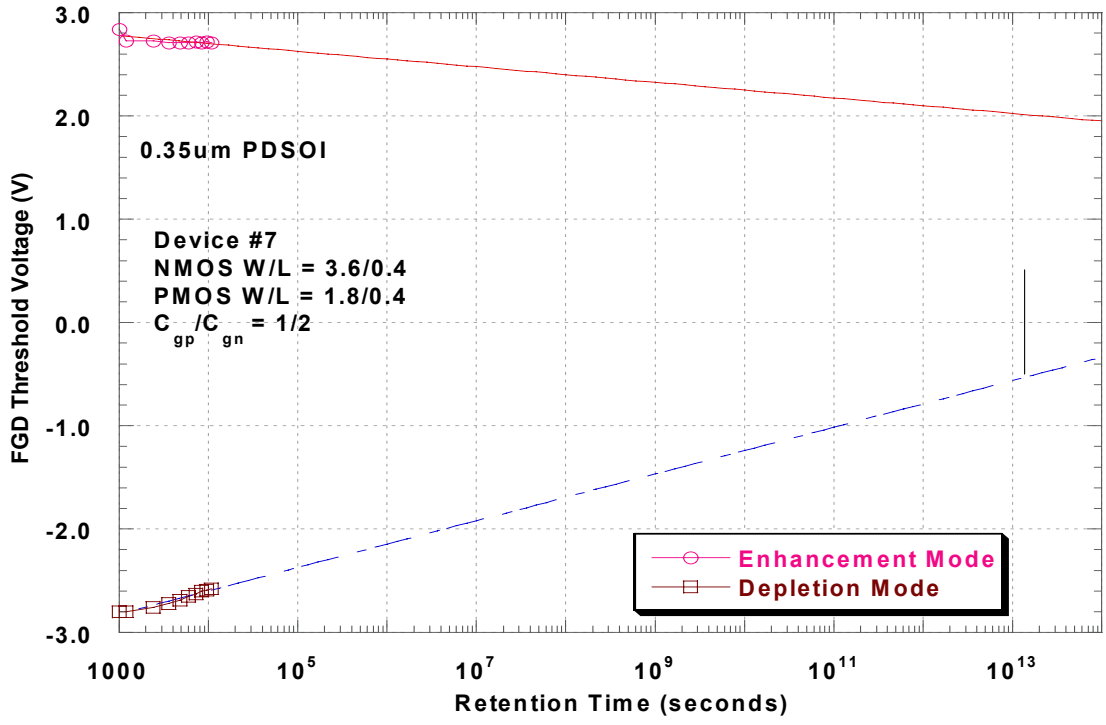


Figure 4.1: Data Retention Estimation using extrapolation

can be considered as the worst case. This window is based on the allowable margins for V_{TH} variation due to charge loss. In this thesis, a V_{TH} variation window size of 1V (-0.5V to 0.5V) is selected [24]. The experimental data is logarithmically extrapolated till it meets this window. The intercept on the X-axis (time in units of seconds), where the experimental extrapolated line meets the V_{TH} variation window, provides the data retention estimate. The data retention for the FGD (device#7) shown in the Figure 4.1 is estimated to be 317,098 years. One of the reasons for achieving such a high data retention time is because of the absence of charge leakage in PDSOI process. The main reason for the upper limit on the data retention and endurance characteristic is the charge trapping onto the floating gate. One possible solution to overcome charge trapping in the oxide is using higher field strength for erasing several cycles so as to make sure the trapped charge is removed. But not all the trapped charge can be removed because there is an upper limit on the allowable erase pulse amplitude without damaging the device. Endurance characterization is a time extensive procedure of alternatively programming and erasing for large number of cycles, making it difficult to implement with the current setup and is beyond the scope of this work. However, it is a topic of future work.

4.2 FGD Failure Mechanisms

The reasons for the failure of a FGD generally are (a) Oxide breakdown, and
(b) Endurance limit of the oxide [7]. The two basic modes of failure mechanisms in EEPROMs are classified as (a) Data Retention, and (b) Endurance Characteristic [17].

The floating gate contains a level of charge that determines the logic stage of the memory cell. Charge is transferred onto or from the floating gate crossing the insulator medium

(SiO_2), depending on the mode of operation through the transfer mechanisms discussed in Chapter 2. During programming/erasing all the charge that has sufficient energy for tunneling does not reach the floating gate or the drain/source terminals respectively. Some of the charge gets trapped in the SiO_2 insulator medium during tunneling [7], which degrades the quality of the SiO_2. The failure modes “data retention” and “endurance” characteristics result from this insulator degradation process. Oxide breakdown is caused by severe damage to the oxide layer of either of the PMOS/NMOS transistors of the FGD structure. This is caused by the application of large potential at the gate. This can typically happen during the programming/erase process or when the device gets exposed to a huge electrostatic potential. Endurance limit can be defined as “The measure of product life in terms of the number of data rewrites” [7]. This specification is primarily used for industrial applications. The endurance is a result of the damage to the insulator medium caused by the electrical stresses during programming/erasing. Lower endurance limits can be expected for devices with thin oxides because of the impact ionization [7]. Though the thin oxide layer helps in reducing the programming/erasing pulse amplitude necessary for tunneling, it impacts the endurance characteristic of the memory element. Hence it is a trade off between the endurance and the programming/erasing pulse amplitude. The following subsections discuss the limitations of single-poly FGDs when used as a memory element and resistive element.

4.2.1 Limitations/Disadvantages as a memory element

There are four primary limitations in using the single-poly FGD as a memory element.

(a) There is a lower limit on the thickness of the oxide layer (5nm). The thickness of the oxide layer plays a major role while establishing the minimum and maximum potential

limits applicable to the device without destroying it. (b) When the single-poly FGD is used in circuit designs, the device needs to be isolated from the system, if programming/ erasing is needed. (c) There are lower and upper limits for the pulse amplitudes while programming/erasing. These form the minimum pulse amplitude that can initiate FN tunneling and the minimum potential applicable to the control gate terminal without destroying the device. These limits are given by Equation 3.1. (d) Extra silicon area is needed for the control circuitry.

4.2.2 Limitations/Disadvantages as a resistive element

Figure 4.2 shows the schematic of the single-poly FGD as a resistive element. The switch helps the single-poly FGD to toggle between the two modes of operation i.e between programming/erasing and active resistor. When the switch is connected to the DC voltage source V_{PGM}, the device can be programmed to desired resistance R_{on} of the FGD by altering the V_{TH}.

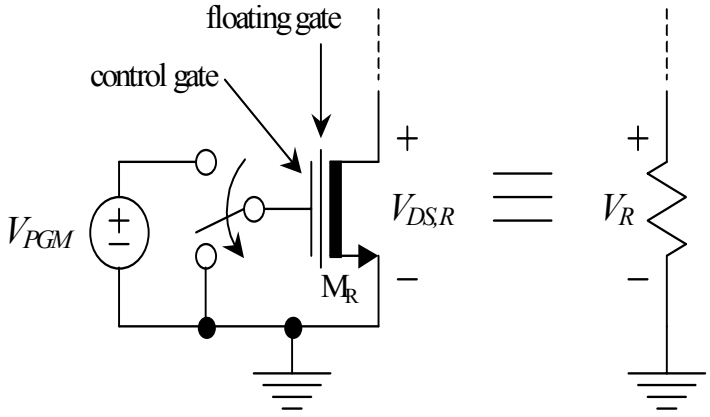


Figure 4.2: Schematic of FGD as a resistive element

The limitations of using the single-poly FGD as a resistive element are now listed. (a) The aspect ratio of the FGD defines the range (upper and lower limits) of the resistances offered by the device. (b) The accuracy or the resolution of the programmable resistance depends on the accuracy of the *control circuit*[1] that configures the single-poly FGD. (c) Care should be taken while designing circuits with FGDs, since the high amplitude programming/erasing pulses might damage portions of the circuit. (d) Extra silicon area is required for the control circuit.

4.2.3 Advantages of single-poly FGDs as memory elements

The advantages of using single-poly FGDs as memory elements are: (a) these devices are highly nonvolatile (shown by the high data retention), and (b) No special/extra mask layers are needed for fabrication

4.2.4 Advantages of single-poly FGDs as resistive elements

The advantages of using single-poly FGDs as resistive elements are: (a) The FGD as an active resistor requires much less silicon area than passive resistors. (b) Post fabrication reconfigurability/tuning is available to the designer, without requiring expensive techniques such as laser trimming.

4.3 Single-poly FGDs and their applications

This section discusses using the single-poly FGD as a programmable resistive element in a basic current reference circuit, a building block for analog circuits and systems. A

1.The circuit that can autoconfigure the single-poly FGD to the desired threshold voltage within the desired limits of precision.

primary design challenge associated with analog circuit design is transistor mismatch (such as threshold voltage mismatch) and poor absolute accuracy of passive components such as resistors. Mismatch can be minimized somewhat by careful layout techniques like common centroid structures. But the single-poly FGD provides the flexibility to trim a transistor's threshold voltage or on-resistance to the required accuracy without specialized (expensive) processing. The next subsection demonstrates the SOI single-poly FGD as a resistive element within a current mirror for an analog current reference circuit, the "beta-multiplier."

4.3.1 Beta-multiplier current reference (BMCR)

A reference current source based on beta-multiplier circuit topology [4] implemented in 0.35μm PDSOI process as a part of the mixed signal design library was used for verifying the single-poly FGD as a programmable resistive element. The schematic of this beta-multiplier is shown in Appendix A. The reference current source was designed for 10μA. The functionality of the BMCR was verified with a 22KΩ 1% metal-film resistor. Later it was replaced by the single-poly FGD as a resistive element. The single-poly FGD's on-resistance is programmed in such a way as to attain certain margin in the I_{ref} (+/-5μA from the I_{ref}). These results are shown in Table 4.1. This shows the unique feature of developing post-process user trimmable reference current source. This is the first of its kind to be developed in SOI process. This programmable resistance feature of the single-poly FGD might be of tremendous advantage in the circuits that need good accuracy in resistance values like ADC's, reference sources and operational amplifiers etc.

Table 4.1: Programmable beta-multiplier current reference

FGD V_{TH} (mV)	On-resistance ($k\Omega$)	I_{ref} (μA)
-166	28.5	5.25
-263	28	6.03
-407	22.6	8.70
-434	20.7	11.4
-515	19.3	16.2

The advantages of this design are: (a) Post-Process trimmable reference current sources could be designed, (b) significant saving in silicon area, and (c) The resolution and precision of reference voltage/current depends on the precision of the programmability. The main disadvantage in using this single-poly FGD as a resistive element is to isolate the device when it needs to be programmed/erased.

4.4 Advantages of PDSOI processes to bulk CMOS processes

The advantages of using PDSOI processes for implementing single-poly FGDs compared to bulk CMOS processes will now be presented: (a) The reverse breakdown voltage of the n-well to p-substrate diode in the bulk CMOS technology cross-section inhibits the programming pulse amplitude that may be applied to the single-poly FGD. PDSOI, however, does not have this constraint thanks to the thick buried oxide isolating the transistor body from the substrate, and (b) Substrate leakage is virtually eliminated because of the isolation between the body and the substrate. This improves the data retention of the SOI FGDs compared to bulk CMOS FGDs.

Chapter 5

Model Simulation and Discussion

This chapter describes the development of a simulation model for analyzing the programming/erasing time dependence characteristics of the single-poly FGD. The first part of this chapter discusses the various equations that are used in the development of the model while the latter part compares the experimental and the simulation trends. Some of the values for the process dependent parameters used in the simulation model were not available, hence an alternative approach is followed for result comparison. Later this model is applied to various processes and the simulation results are given in Appendix A. This demonstrates the ease of portability of this model to various processes. These simulation results can be used for estimation of FGD threshold voltage variation with programming/erasing pulse amplitude and duration.

5.1 Model Development

This is a simplified and first order approximation model of the single-poly FGD's threshold voltage dependence on programming/erasing pulse amplitude and duration. This model is based on the capacitive divider network shown in Figure 5.1. The basic tunneling current density for Fowler-Nordhiem tunneling can be obtained from Equation 2.2.

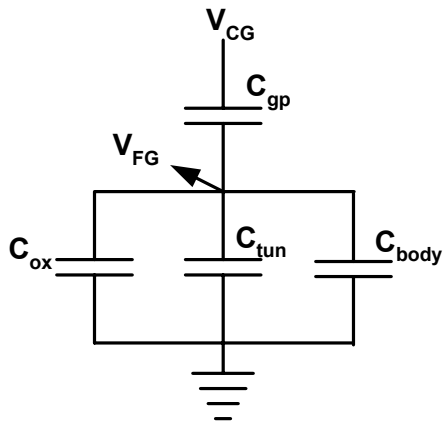


Figure 5.1: Capacitor network of the FGD

The floating gate voltage is effected by negative charge programmed onto the floating gate and is given by:

$$V_{fg} = V_{cg} \times \left[K_w + \frac{Q_{FG}}{V_{cg} \times (C_{tun} + C_{body} + C_{gp})} \right] \quad 5.1$$

where V_{fg} is the potential of the floating gate, V_{cg} is the applied programming pulse amplitude, C_{gp} is the gate capacitance offered by the PMOS, C_{tun} is the gate capacitance of the NMOS, C_{body} is the body capacitance offered by the NMOS, Q_{FG} is the charge built up because of the programming pulse, and parameter K_w is the capacitor ratio described by

$$K_w = \frac{C_{gp}}{C_{tun} + C_{body} + C_{gp}} \quad 5.2$$

The body capacitance offered by the PDSOI processes (C_{body}) is much less than the body capacitance offered by the bulk CMOS processes.

Similar expression for erasing is given by

$$V_{fg} = V_d \times K_e - \frac{Q_{fg}}{C_{tun} + C_{body} + C_{gp}} \quad 5.3$$

where K_e indicates

$$K_e = 1 - \frac{C_{tun}}{C_{tun} + C_{body} + C_{gp}} \quad 5.4$$

The final expression for the time dependency is derived from the differential equation

$$\frac{dQ_{fg}}{dt} = A_{tun} \times J_{tun} \quad 5.5$$

where A_{tun} indicates tunneling area (gate area of the NMOS within the single-poly FGD) and J_{tun} indicates the tunneling current density. From the above equations the FGD's threshold voltage time dependency while programming can be derived from [17,51] to be

$$V_{TH}(t) = \left[(V_{THi} + V_{prog}) - \left[\left[\frac{B}{\ln((A \times B \times t) + E_{prog})} \right] \times \left(\frac{1}{K_w} \right) \right] \right] \quad 5.6$$

where

$$E_{prog} = \exp\left[\frac{B}{Kw \times (V_{prog} + V_{THi} - V_t(0))} \right] \quad 5.7$$

and

$$A = \left[\frac{A_{tun} \times \alpha}{X_{tun} \times (C_{gp} + C_{tun} + C_{body})} \right] \quad 5.8$$

with

$$B = \beta \times X_{tun} \quad 5.9$$

where $V_{TH}(t)$ denotes the threshold voltage of the single-poly FGD for a programming pulse width (refer Chapter 3 for definition) of t seconds, V_{THi} is the threshold voltage of the neutral (no programming/erasing) cell, $V_t(0)$ is the threshold voltage at time 't=0s', and the α and β are Fowler-Nordhiem tunneling parameters. Similarly, the threshold voltage time dependence equation for erasing is described by

$$V_{TH}(t) = V_{THi} - \left(\frac{K_e}{K_w} \times V_d\right) + \left[\left[\frac{B}{\ln((A \times B \times t) + E_{erase})}\right] \times \left(\frac{1}{K_w}\right)\right] \quad 5.10$$

where

$$E_{erase} = \exp\left[\frac{B}{V_d \times K_e - (Kw \times V_{THi}) + (V_t(0) \times K_w)}\right] \quad 5.11$$

where parameter V_d refers to the erasing pulse amplitude. All the other parameters are as defined earlier. By coding these expressions into a software tool such as MATLAB, a single-poly FGD simulator is attained that readily predicts the programming/easing behavior of a given single-poly FGD.

5.2 Simulation Results

This section describes the SOI single-poly FGD simulation results, including comparison with measured trends. Equation 5.6 and Equation 5.10 have been used to generate the simulated waveforms for different FGD dimensions and shape factors. There is limited information available related to Fowler-Nordhiem tunneling parameter values, thus

complicating the simulation process. Since the tunneling parameter values are not available for this process (PDSOI 0.35μm), the following procedure was followed: A random device's experimental results are taken and the parameter values are predicted such that the results match well. This procedure is repeated with another device with different aspect ratio and the average values of the parameters are taken as reference parameter values. These parameter values are used in the simulation process and the simulated trends are compared against the experimental trends.

It has been observed that the parameter values of α =1.88μA/(V-cm)^2 and

β = 60MV/cm (The values as per the [3] are α = 2μA/(v-cm)^2, β = 238MV/cm). The Figure 5.2 - Figure 5.6 show the comparison between the simulation results and the experimental results. From the graphs, it is clear that there is a good match between simulation and experimental trends.

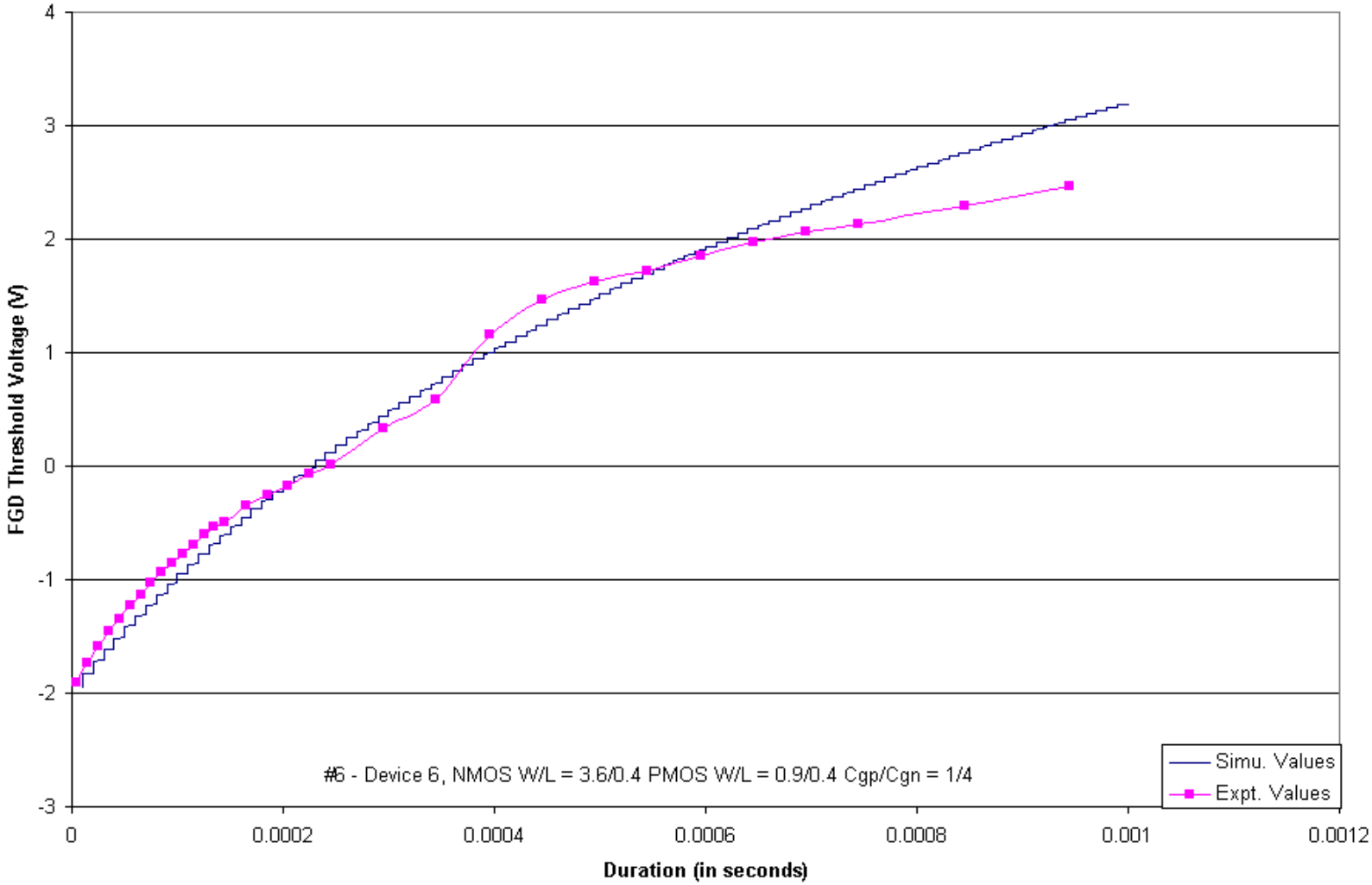


Figure 5.2: Comparison between experimental and simulated trends (FGD #6) during programming

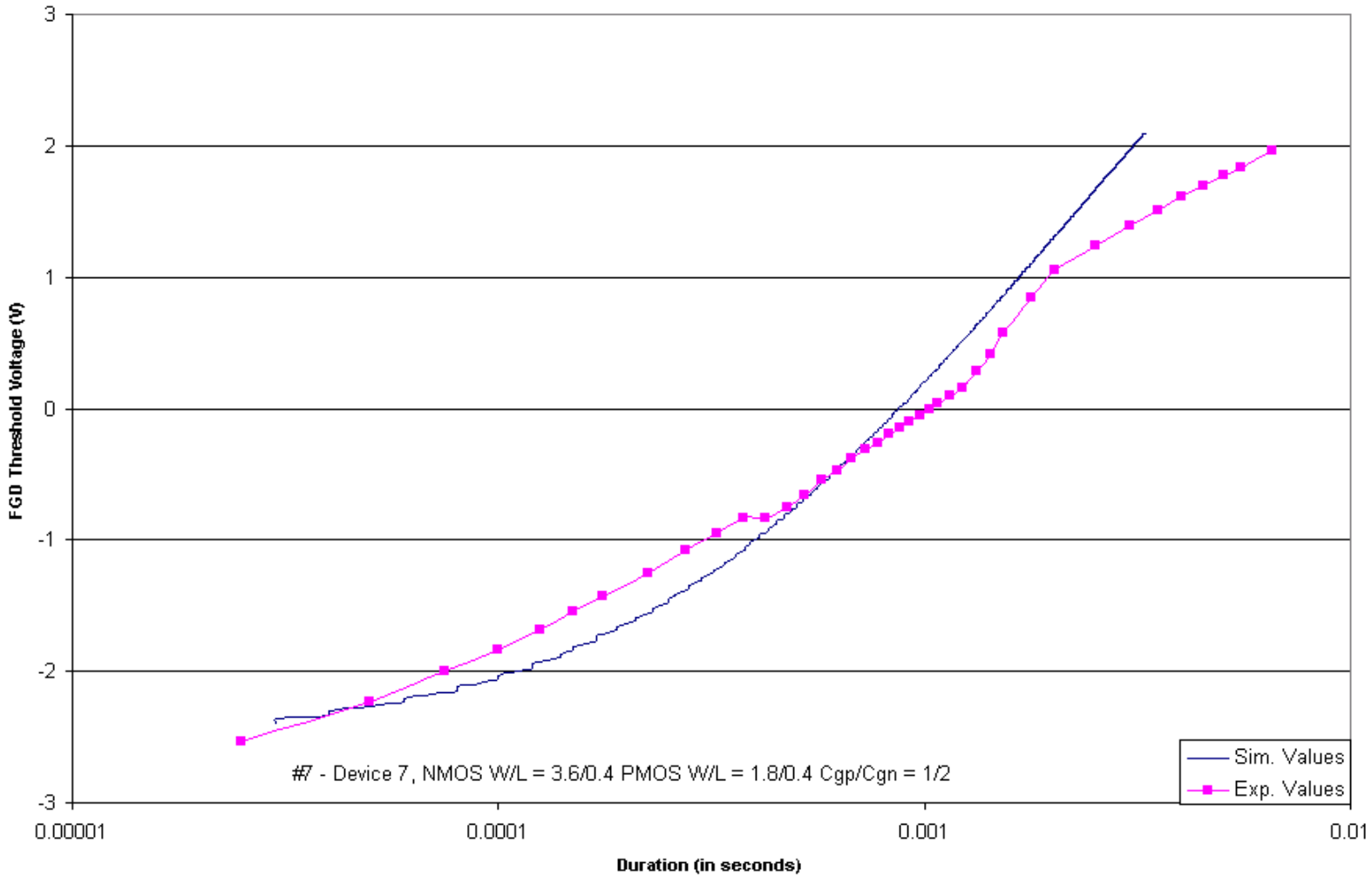


Figure 5.3: Comparison between experimental and simulated trends (FGD #7) during programming

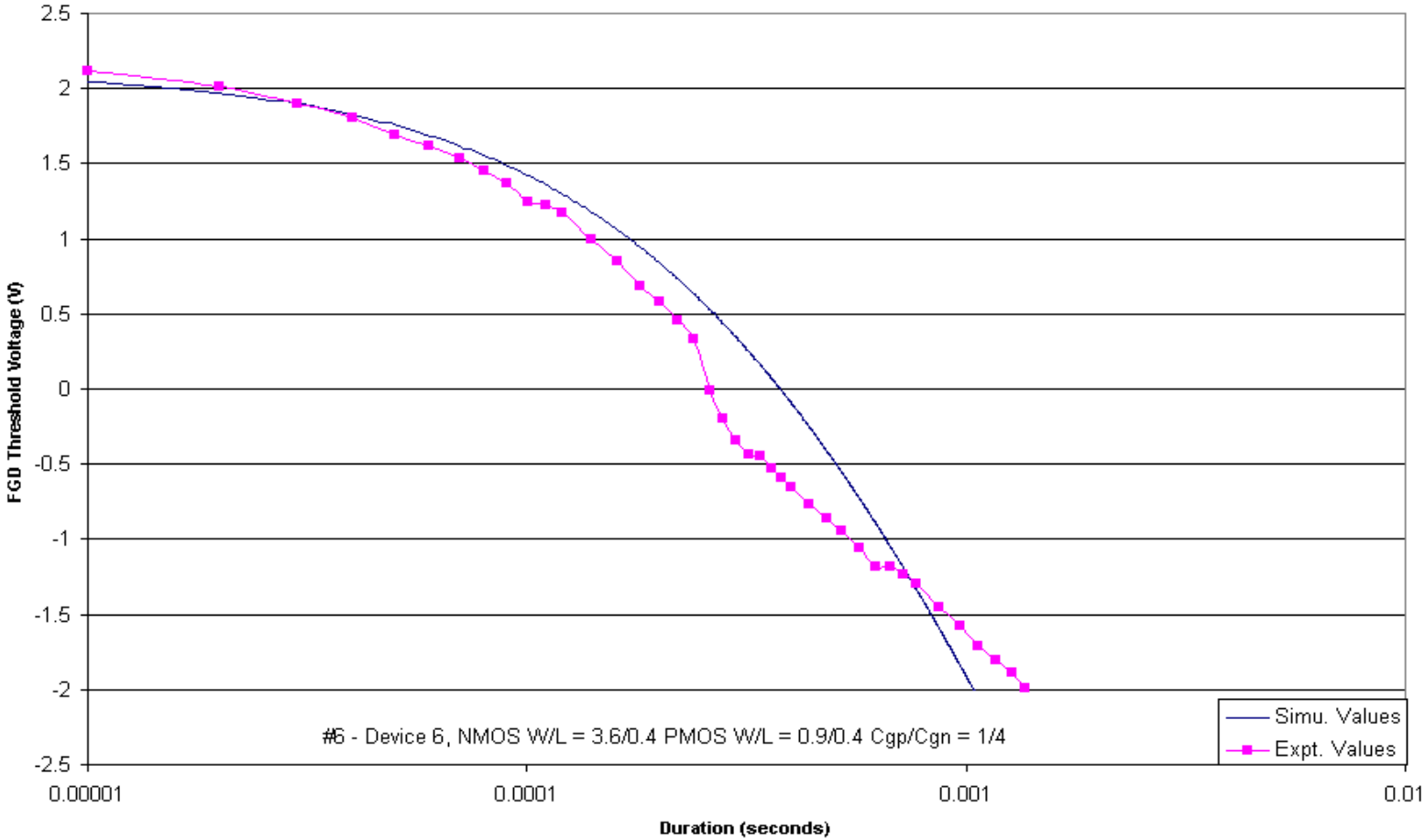


Figure 5.4: Comparison between experimental and simulated trends (FGD #6) during erasing

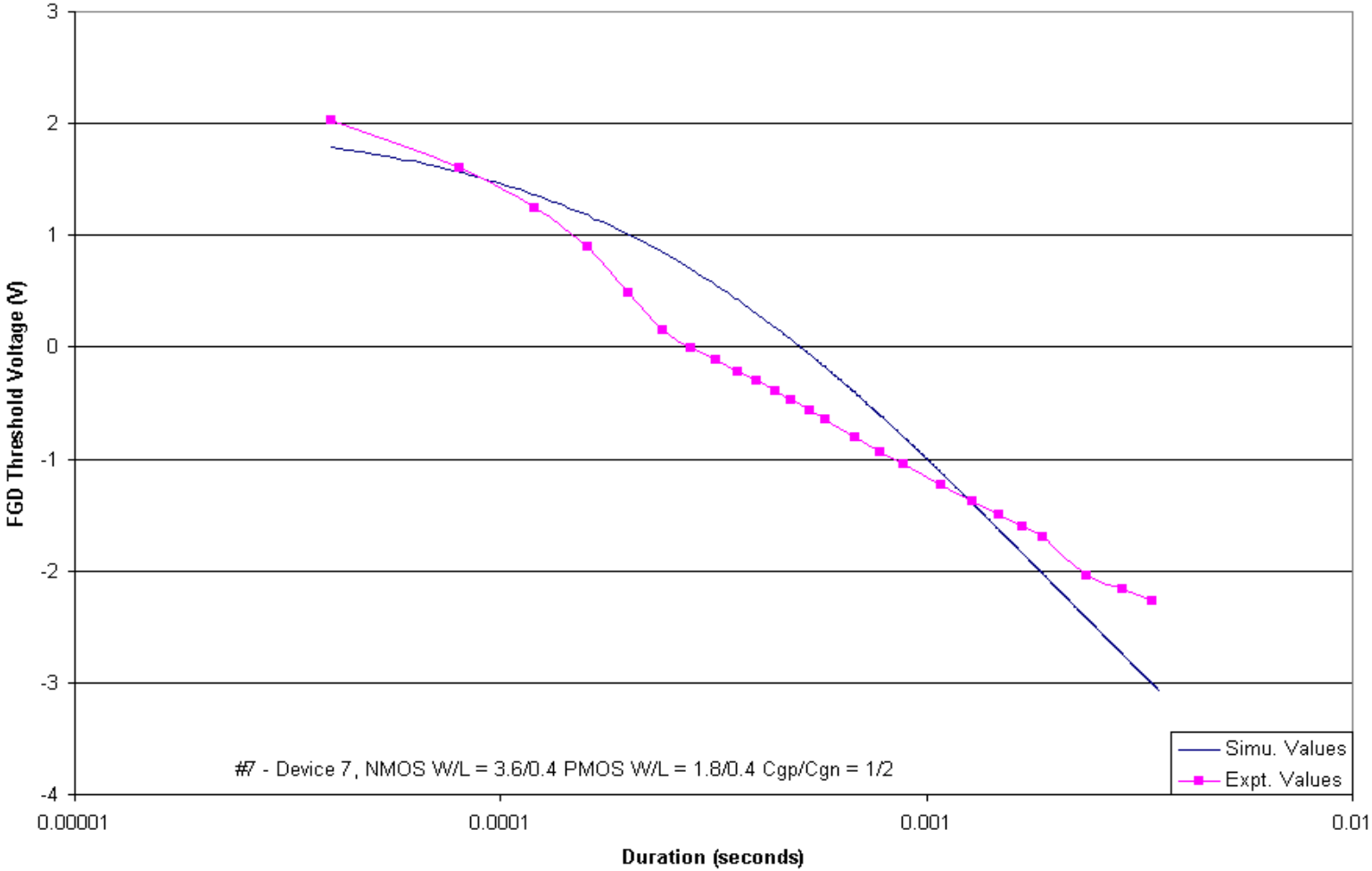


Figure 5.5: Comparison between experimental and simulated trends (FGD #7) during erasing

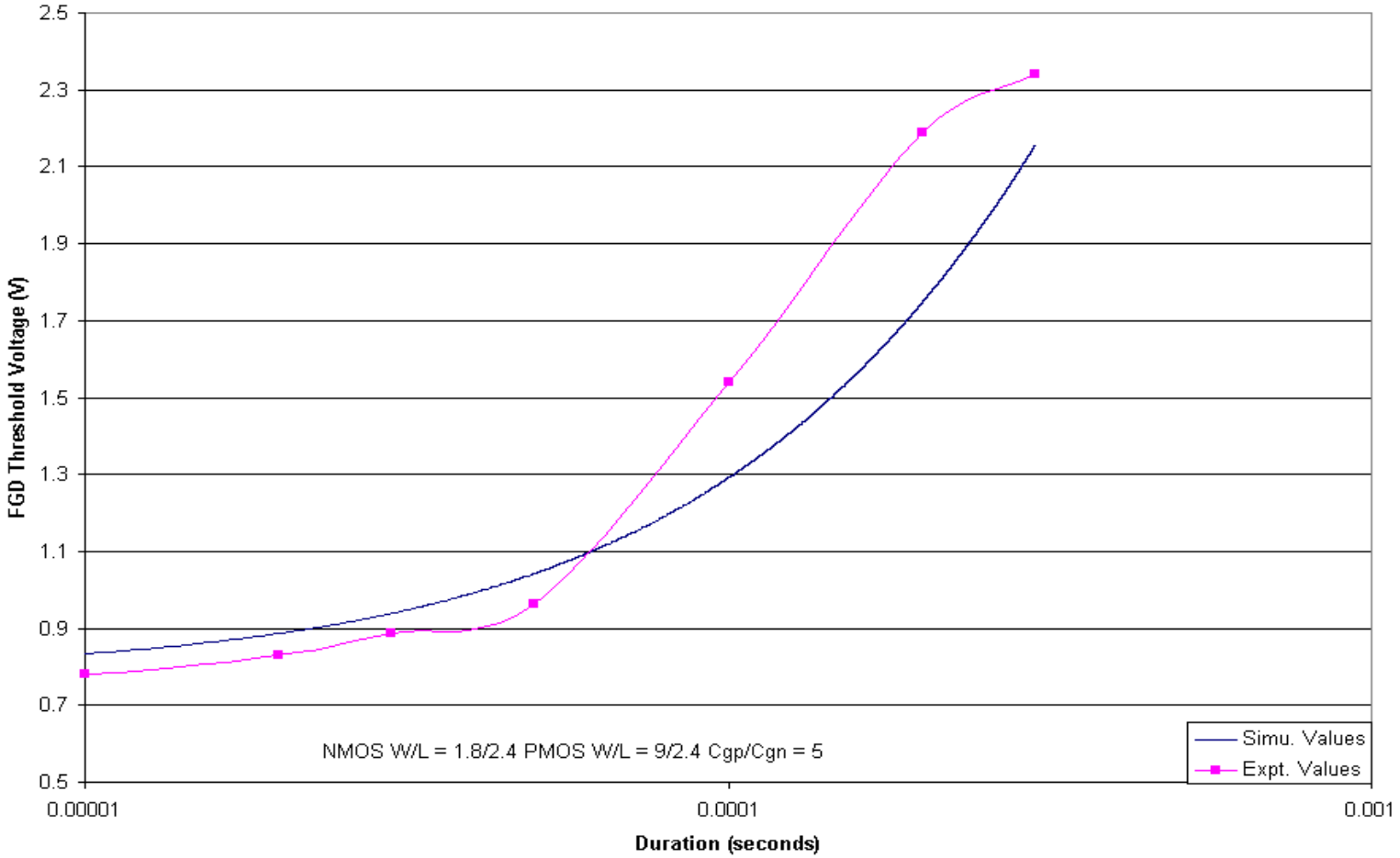


Figure 5.6: Comparison between experimental and simulated trends in HP 0.5um process during programming

Similar comparison has been made in HP 0.5μm process and results match well as in the PDSOI process. Results for different transistor dimensions in PDSOI process are put in the Appendix A. The primary source of mismatch between the results is the selection of Fowler-Nordhiem tunneling parameters. Secondly, the second order effects [51] such as: a) Depletion in the channel b) Deep depletion under the tunnel oxide and c) Hole flow into the substrate are not considered in the model. On the other hand, there is a contribution of error factor associated with the manual measurement of threshold voltage. The errors from the manual measurement can be eliminated by automating the entire process. The errors from the channel can be eliminated by extracting the C-V curves for the single-poly FGD's and integrating the capacitance variation into the model. The variation in the tunnel capacitance directly impacts the K_e and K_w parameters, which have a considerable impact. The model developed in this thesis does not incorporate the dynamic capacitance variation.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis presents the characterization methodologies and results of the single-poly FGDs fabricated in a 0.35μm PDSOI process. The measured behavioral trends of these SOI single-poly FGDs agree well with the theory developed for double-poly FGDs fabricated in bulk CMOS processes [17]. A mathematical relation between on-resistance and threshold voltage of the single-poly FGD has been experimentally determined and verified. It was observed that the threshold voltage's temperature sensitivity (dV_{TH}/dT) decreases as the device is erased from enhancement-mode to the depletion-mode. Data retention for the single-poly FGD has been determined to be approximately 317,098 years. And lastly, a process independent MATLAB simulation model has been developed for predicting the programming/erasing behavioral trends for a given FGD. This simulation tool facilitates the design optimization of a single-poly FGD for a specific application.

This work has shown that programmable or post-process trimmable analog circuits can be implemented in SOI using single-poly FGDs as programmable resistive elements. A SOI programmable beta multiplier current reference has been successfully demonstrated using the single-poly FGD as a resistive element.

6.2 Future work

The future work can be broadly classified into 2 categories: (a) characterization setup, and (b) system level designs using FGDs.

A characterization system is needed that can automatically configure the single-poly FGD to a desired threshold voltage within the desired limits of precision. This would dramatically reduce the significant time investment demanded by the experimental nature of this work. The next step in this process would be to include design an on-chip circuitry in SOI that can generate the necessary pulses to program/erase the FGD. This would enable fully integrated systems to be developed in SOI utilizing single-poly FGDs.

A spice model for the single-poly FGD would help designing circuits using these versatile devices. The literature survey has showed that noise analysis was never done on these devices, neither double-poly nor single-poly FGDs in bulk CMOS or in SOI processes. These steps complete the characterization process of the single-poly FGDs in PDSOI process.

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Appendices

Appendix A: Graphs

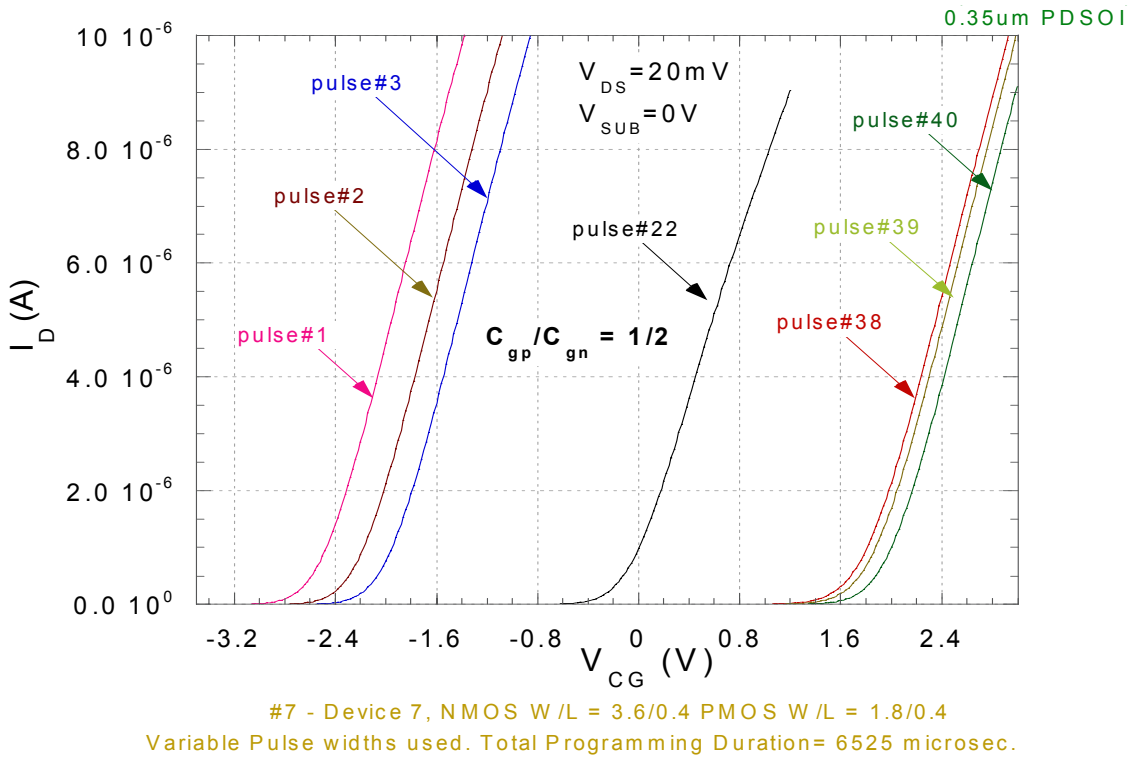


Figure A.0.1: MOS transistor functionality of the single-poly FGD (during programming)

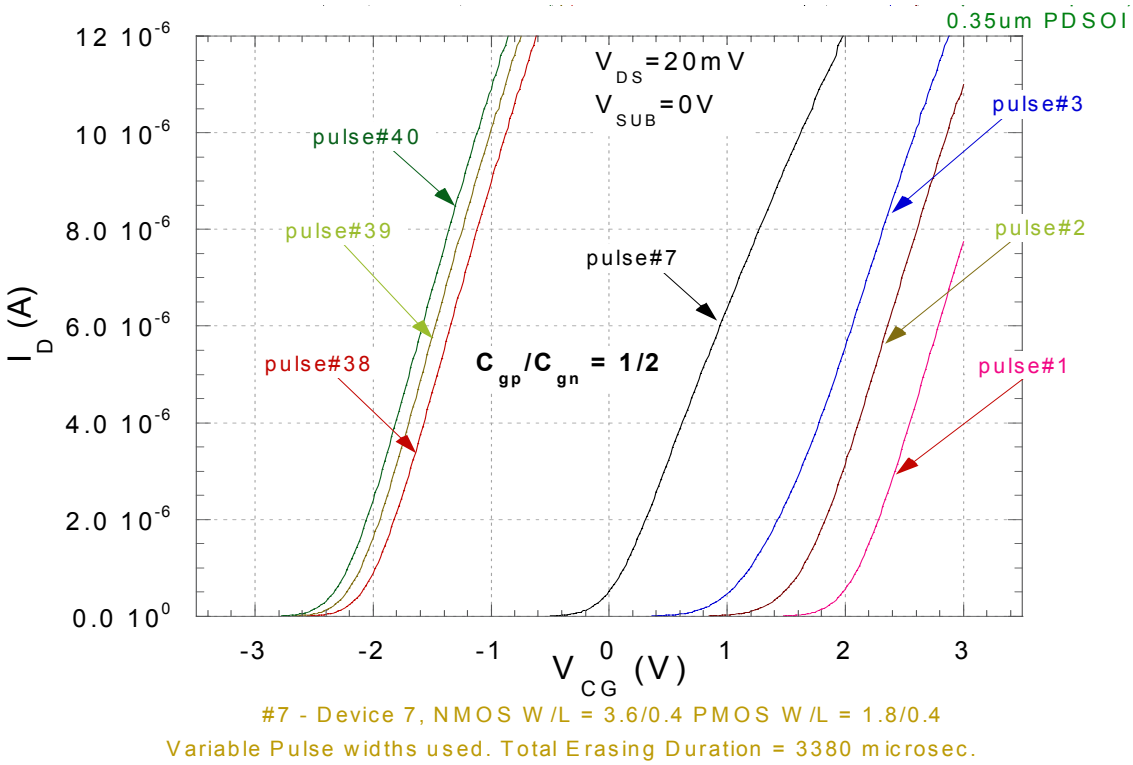
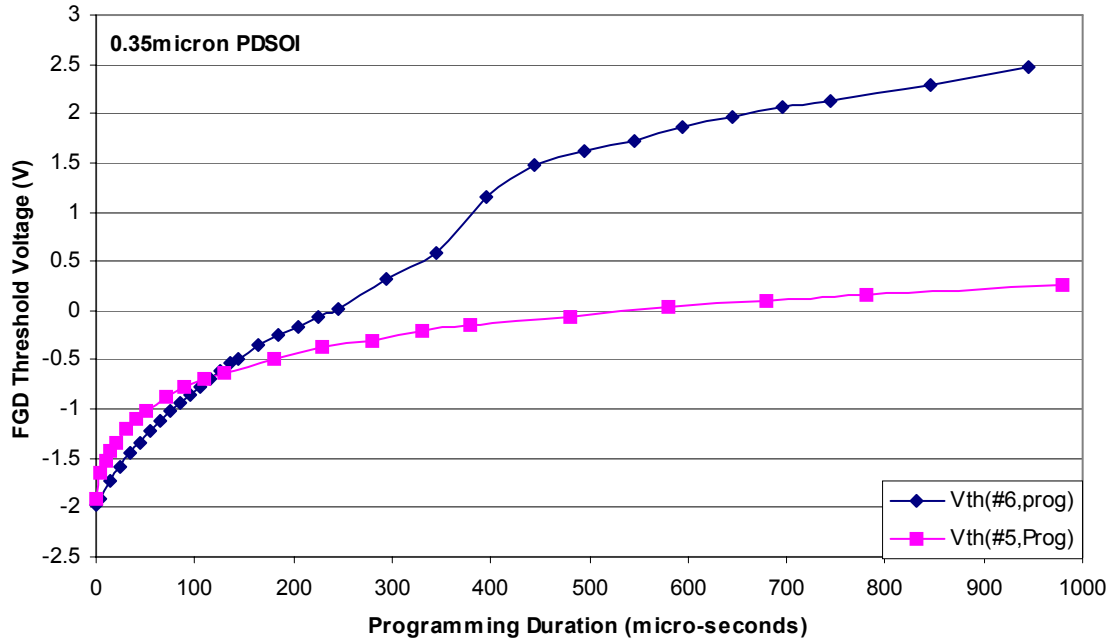


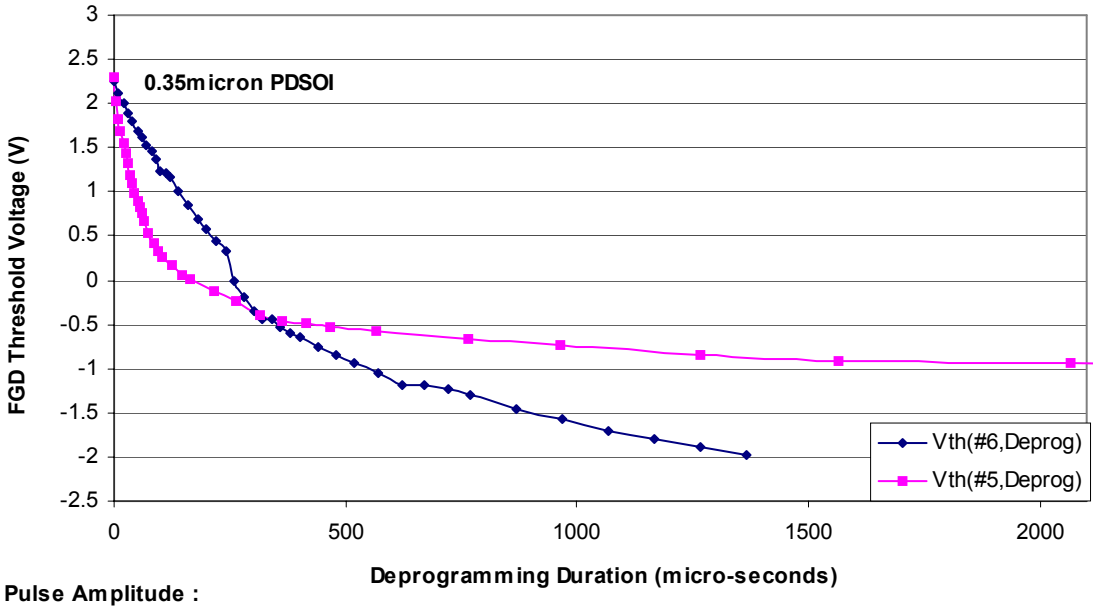
Figure A.0.2: MOS transistor functionality of the single-poly FGD (during erasing)



Pulse Amplitude :
#5: 10.5V pk-pk
#6 : 11.0V pk-pk

#6 - Device 6, NMOS W/L = 3.6/0.4 PMOS W/L = 0.9/0.4 Cgp/Cgn = 1/4
#5 - Device 5, NMOS W/L = 1.8/0.4 PMOS W/L = 7.2/0.4 Cgp/Cgn = 4

Figure A.0.4:Threshold voltage variation during programming for #5, #6.



Pulse Amplitude :
#5: 13.0V pk-pk
#6 : 12.8V pk-pk

#6 - Device 6, NMOS W/L = 3.6/0.4 PMOS W/L = 0.9/0.4 Cgp/Cgn = 1/4
#5 - Device 5, NMOS W/L = 1.8/0.4 PMOS W/L = 7.2/0.4 Cgp/Cgn = 4

Figure A.0.5: Threshold voltage variation during deprogramming for #5, #6.

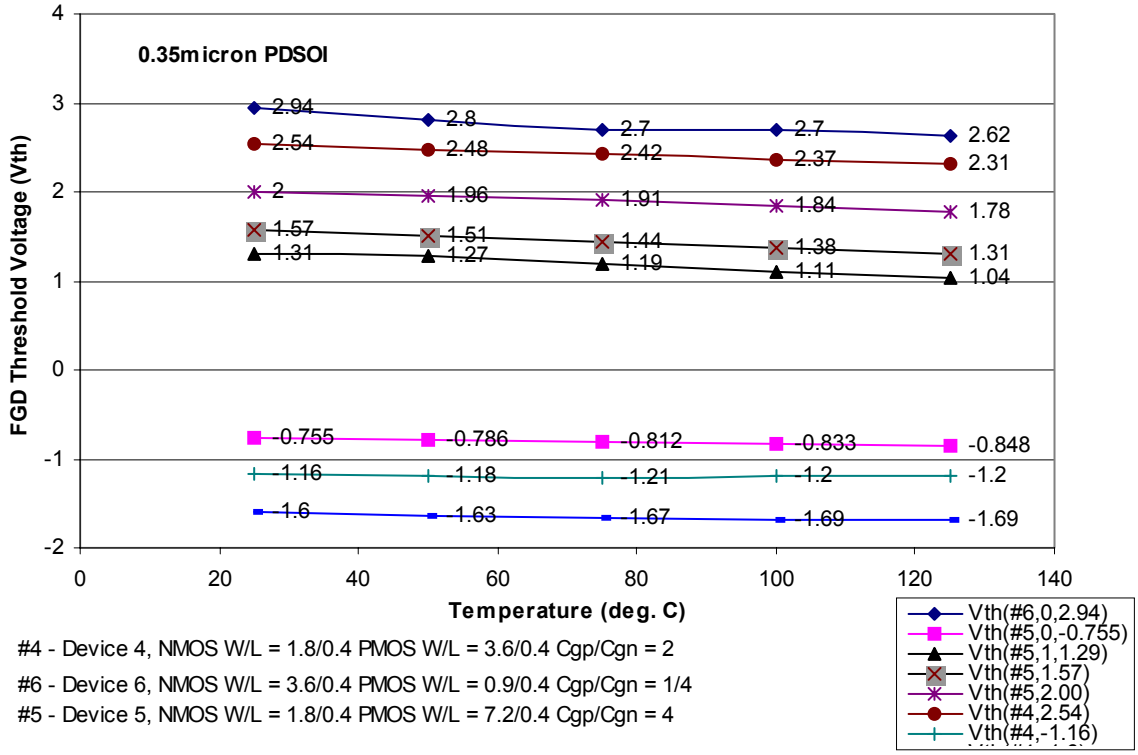
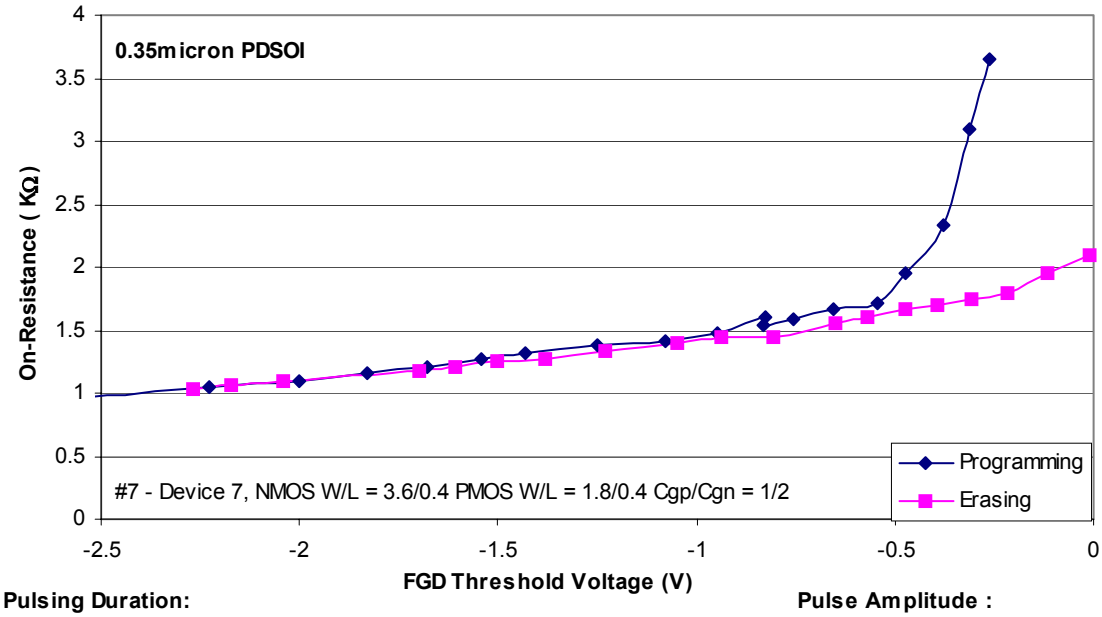


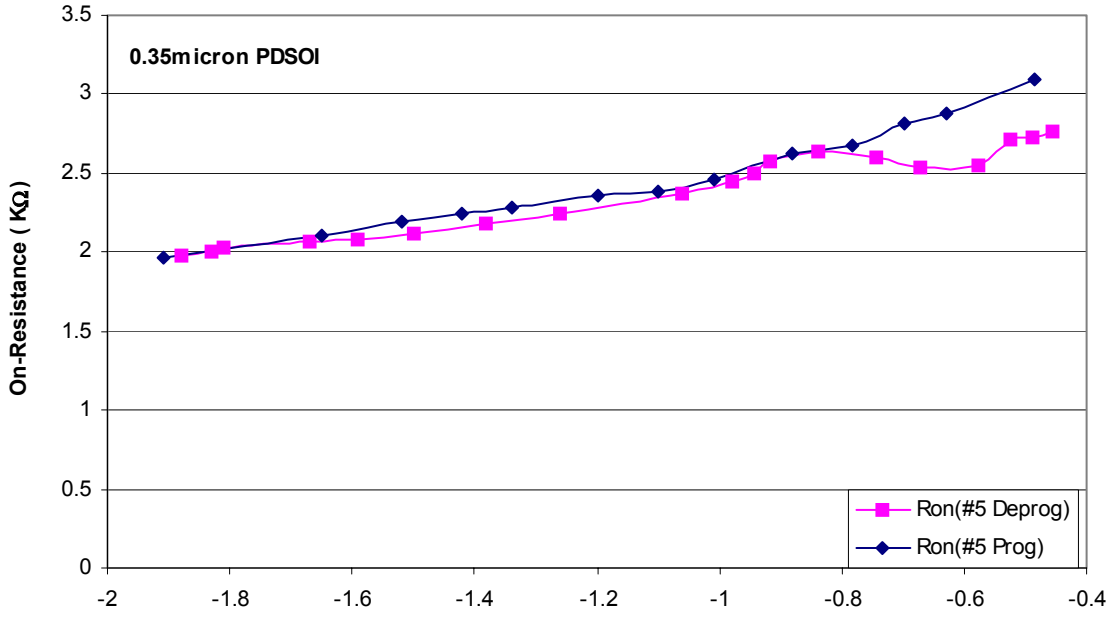
Figure A.0.6: Threshold Voltage Variation vs. Temperature



Pulsing Duration:
Programming :7170 microseconds
Deprogramming :6525 microseconds

Pulse Amplitude :
Progra: 12.0V pk-pk
Deprog: 15.0V pk-pk

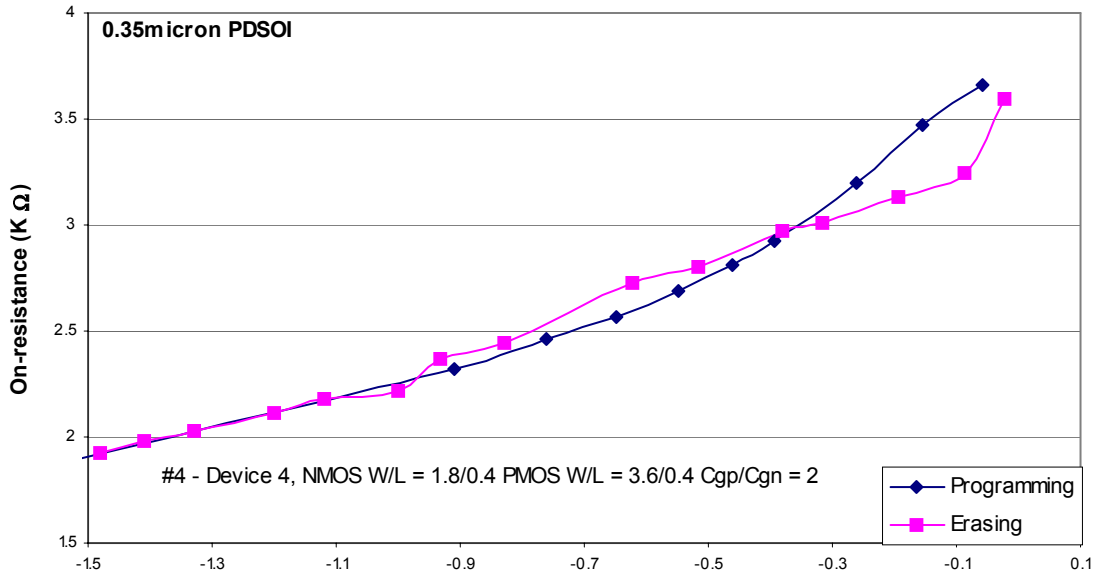
Figure A.0.7: Hysteresis of on-resistance vs. threshold voltage for Device#7



Pulse Amplitude :
Programming : 10.5V pk-pk
Deprogramming : 13.0V pk-pk

#5 - Device 5, NMOS W/L = 1.8/0.4 PMOS W/L = 7.2/0.4 Cgp/Cgn = 4

Figure A.0.8: Hysteresis of on-resistance vs. threshold voltage for #5



Pulsing Duration:
Programming : 7170 microseconds
Deprogamming : 21830 microseconds

Pulse Amplitude :
Progra: 13.0V pk-pk
Depro : 15.0V pk-pk

Figure A.0.9: Hysteresis of on-resistance vs. threshold voltage for #4

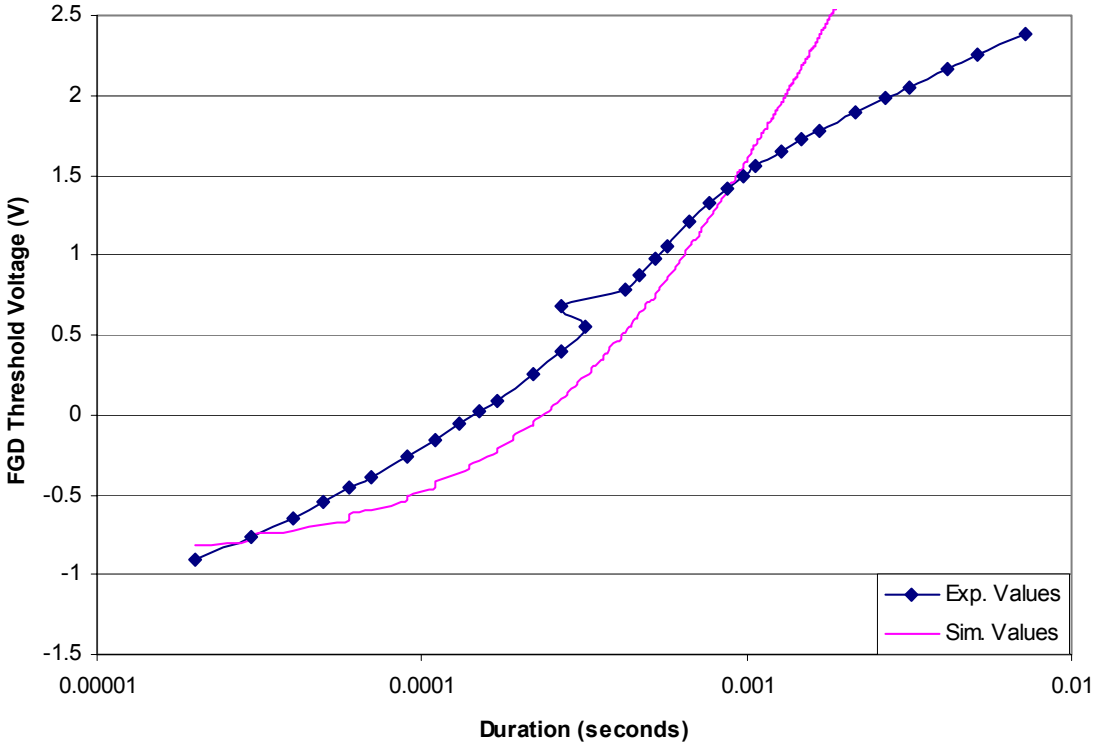


Figure A.0.10: Comparison between experimental and simulated trends (FGD #4) during programming

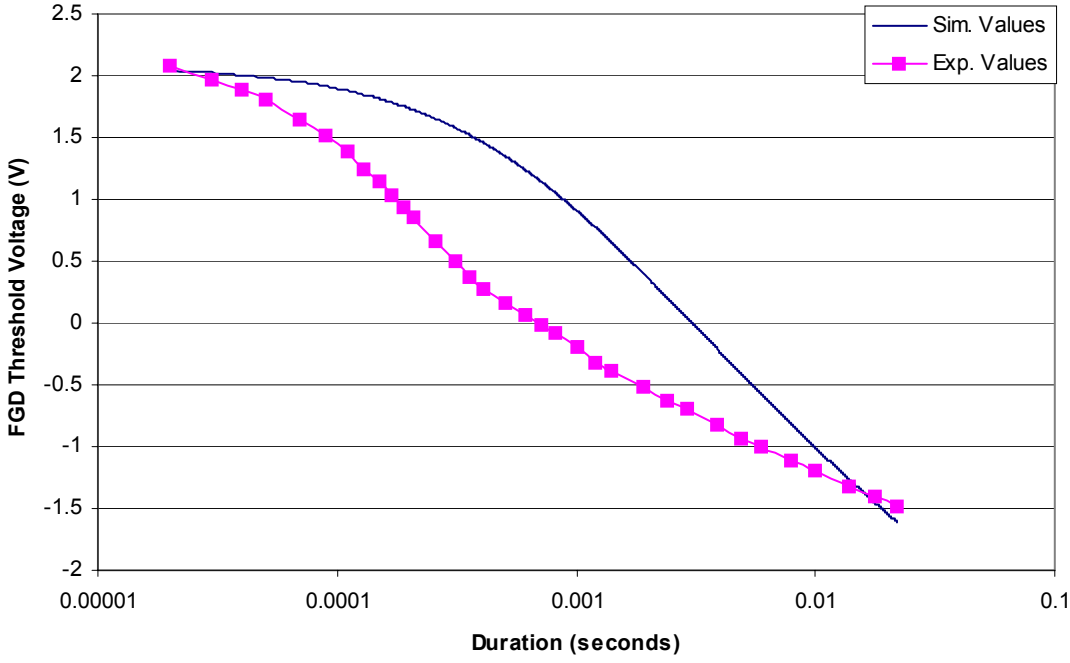


Figure A.0.11: Comparison between experimental and simulated trends (FGD #4) during erasing

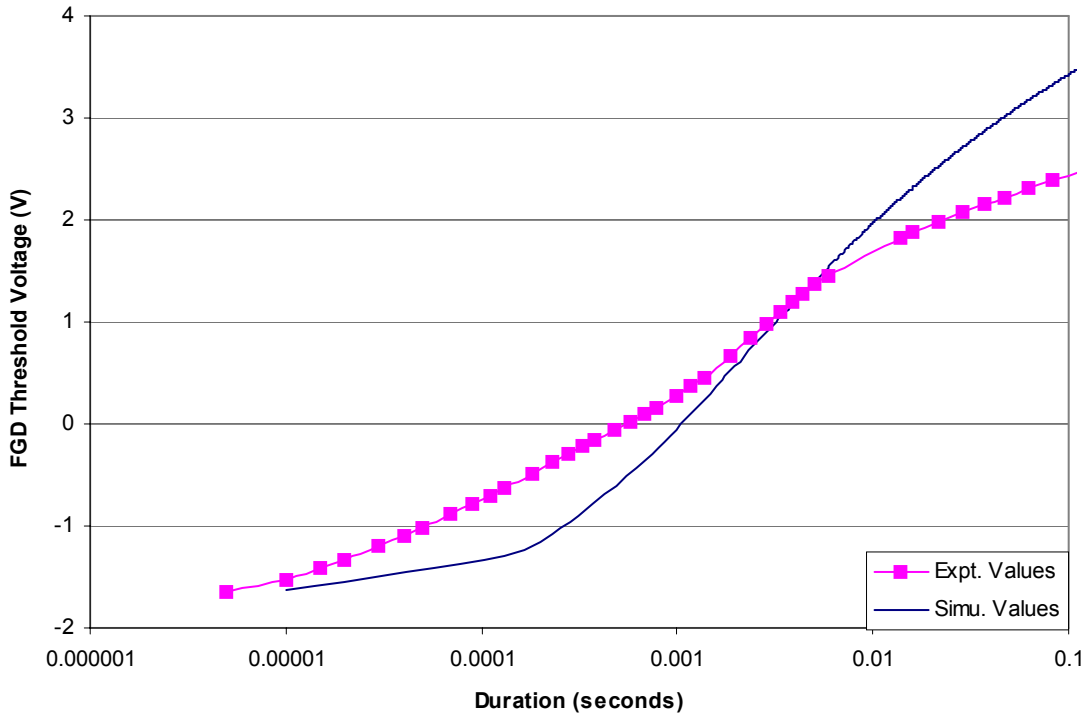


Figure A.0.12: Comparison between experimental and simulated trends (FGD #5) during programming

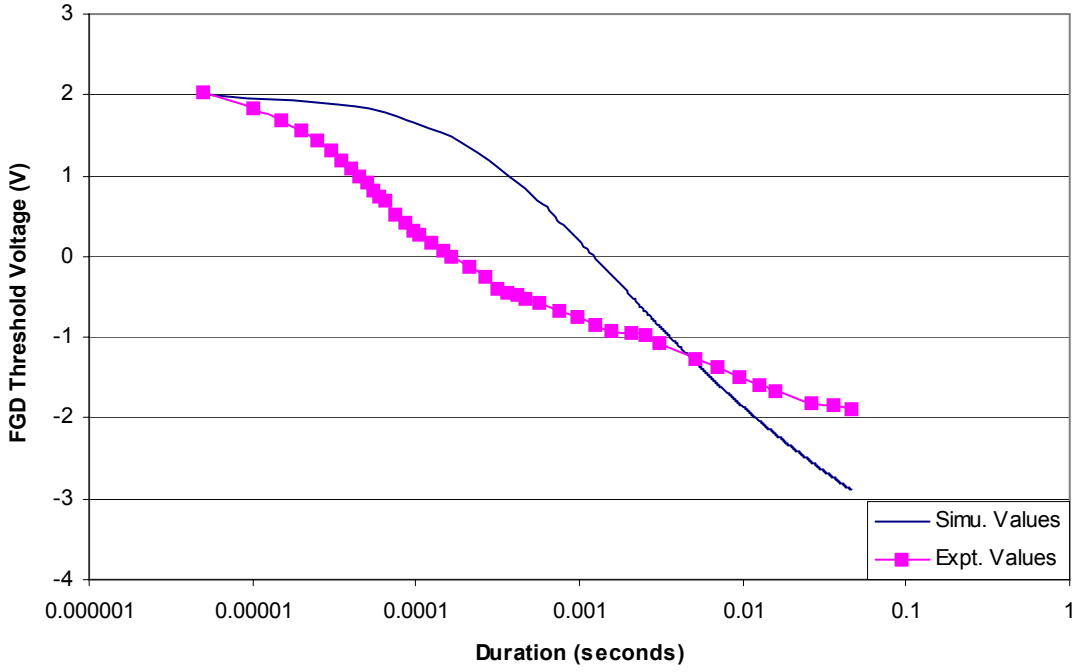


Figure A.0.13: Comparison between experimental and simulated trends (FGD #4) during erasing

A.1: Programmable Beta multiplier Schematic

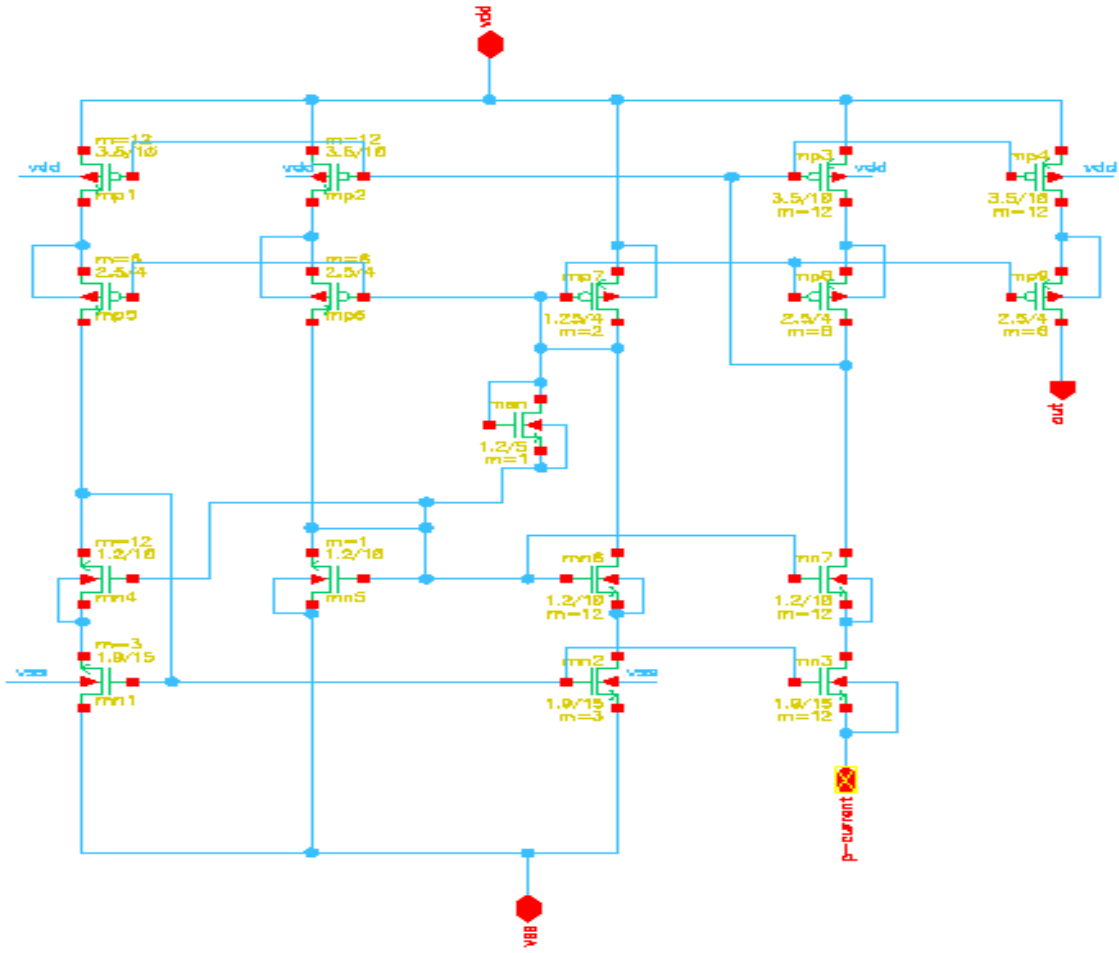


Figure A.1.1: Schematic of Programmable Beta Multiplier

A.2: Microphotographs

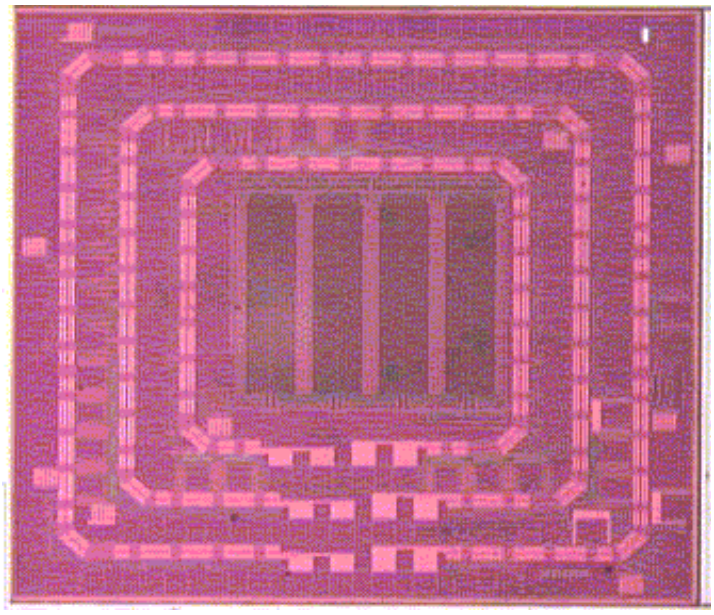


Figure A.2.1: Microphotograph of the Entire Chip

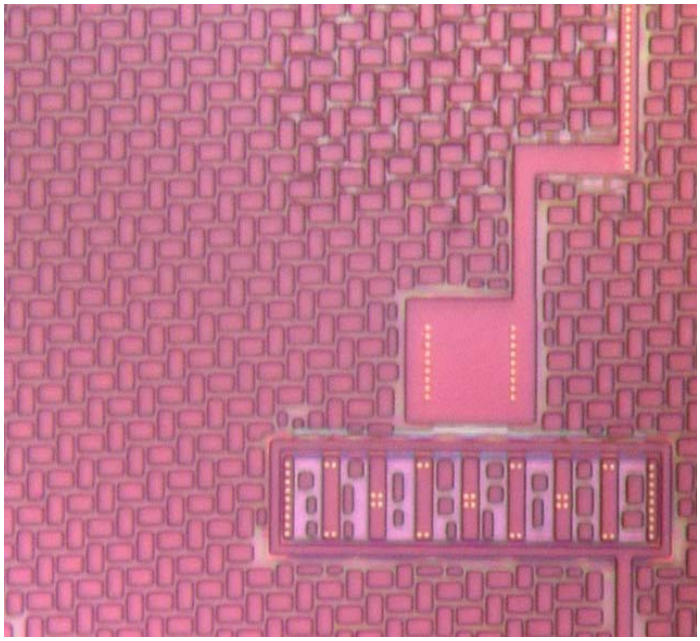


Figure A.2.2: Microphotograph of a single-poly Floating Gate Device

Appendix B: Test Board and Experimental Setup

B.1: Verification Process

The verification process can be classified as (a) Test board development, and (b) Labview code development. This work has been done with the help of undergraduate students. The entire test setup is shown in Appendix Figure B.2.1 and discussed in detail in Section B.3. The next two sections briefly describe the test board and the lab view code used in this verification process.

B.2: Test Board Description

The test board setup consists of 2 boards: Board1 and Board2. These are shown in Appendix Figure B.2.2 and Appendix Figure B.2.3. Board1 is used for selecting the desired single-poly FGD from the 8 different FGDs available on the Chip. Board2 is used to switch between programming, erasing, sensing/reading and beta-multiplier modes.

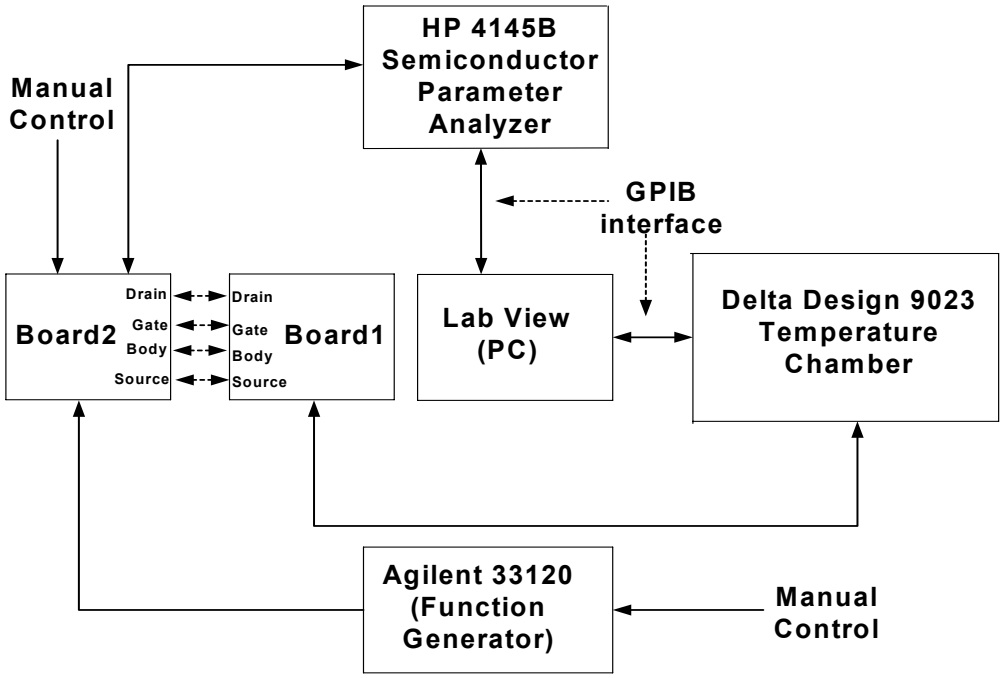


Figure B.2.1: Test Setup for the Single-Poly FGD

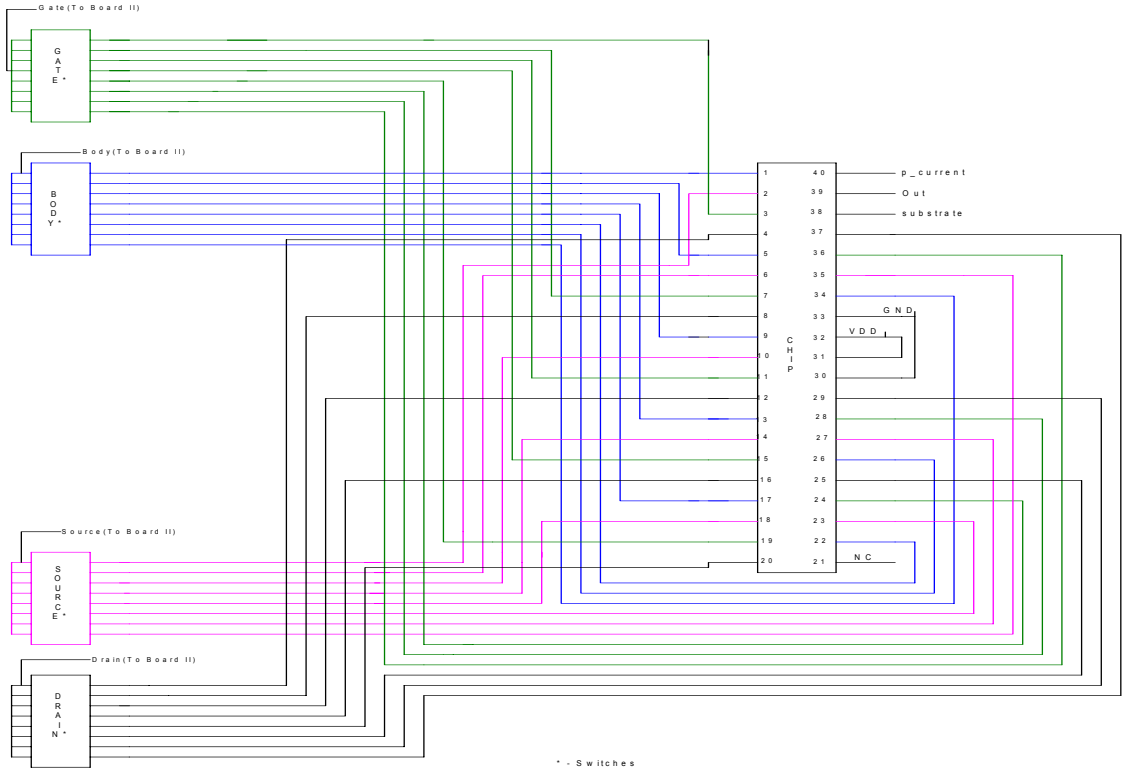


Figure B.2.2: Board schematic

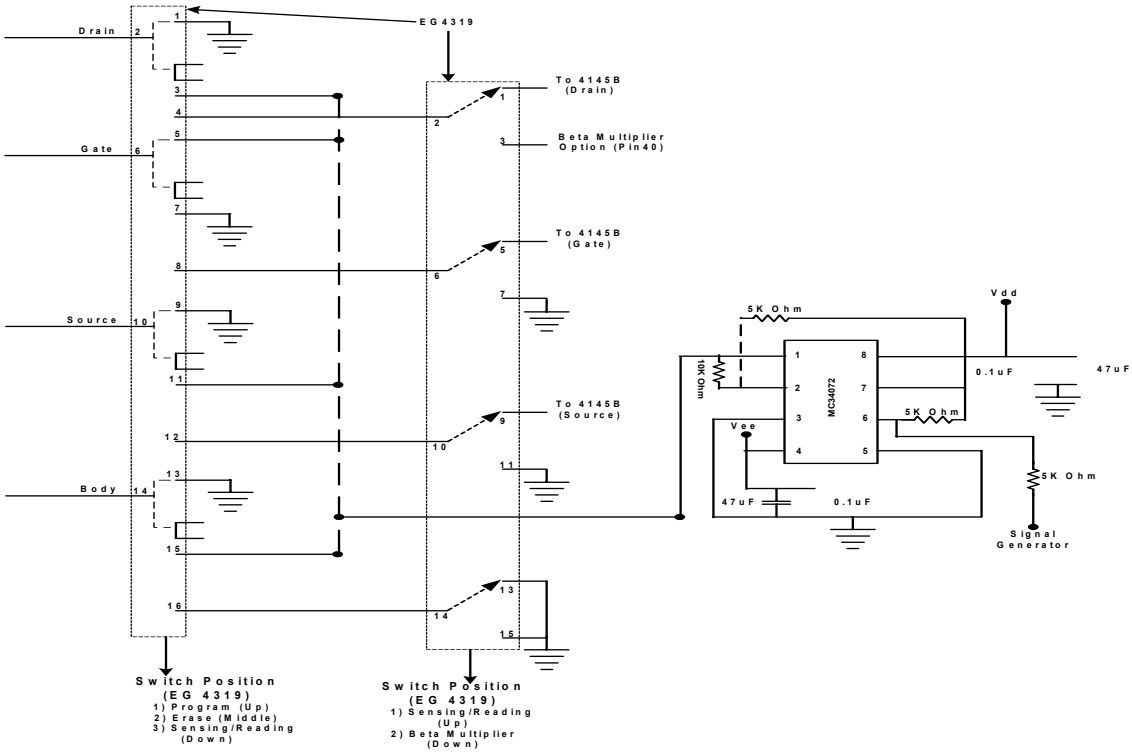


Figure B.2.3: Board2 schematic

The four switches (Drain, Gate, Source and Body shown in Appendix Figure B.2.2) are used to select the respective terminal of the desired single-poly FGD from a set of 8 FGDs. The first three modes available in Board2 are discussed in Chapter 2. The beta-multiplier mode is used in the Chapter 4 for testing the programmable beta-multiplier current reference. The schematics of this board are illustrated in the Appendix Figure B.2.3. Board2 generates the required pulses necessary for programming/erasing the single-poly FGD.

The lab view programs were developed by another undergraduate student to extract the basic I-V curve data (threshold voltage and on-resistance measurement), data retention and for the estimation of TC. An FGD prototype characterization setup (set of 2 boards) has been developed. The primary reason for the design of two test boards is that Board1 (contains the D.U.T, i.e. single-poly FGD) would be exposed to the controlled temperature while the Board2 is available outside the temperature chamber for the controlling the modes of operation.

B.3: Experimental Setup

The entire test setup is shown in Appendix Figure B.2.1. It consists of 2 test boards, HP4145B (Semiconductor Parameter Analyzer), Agilent 33120 (Function Generator), Delta Design 9023 (Temperature Chamber), and a personal computer (for running Labview programs).

The verification procedure starts with the selection of the desired single-poly FGD on Board1. Later appropriate mode of operation is selected on Board2. If the

programming/erasing mode is selected, the pulse amplitude and the frequency should be carefully selected in the function generator. The output from the function generator is amplified by the control circuit in the Board2 using the Motorola MC34072 operational amplifier. The amplified signal drives the D.U.T in Board1. If the characterization mode is selected in Board2, the D.U.T is automatically connected to HP4145B for characterization. In the beta-multiplier mode, the single-poly FGD is connected as a resistive element to the beta-multiplier circuit.

The labview program controls the HP4145B and the temperature chamber while the modes of operation of the single-poly FGD are manually selected through various switches. For the case of temperature measurements, Delta Design9023 temperature chamber was used. This is also controlled through the lab view program using the GPIB interface. The entire test setup is automated except for the selection of specific single-poly FGD on Board1 and the mode of operation on Board2. This automated test setup has minimized the manual errors and eliminated extensive manual intervention required for most of the experiments.

Appendix C: MATLAB SIMULATION MODEL

C.1: Programming Time Dependence Model

% This is to estimate the threshold voltage variation with programming/erasing programming pulse amplitude and duration.This part is for the estimation of delta Vth variation. Refer Pg.145 and Pg.134 from "Nonvolatile Semiconductor Memory.

%General Parameters

Let the aspect ratio of NMOS be 2/1, while the PMOS be 8/1. Then the Cgp/Cgn of the FGD be 4/1;

```
clc
clear
% ----------Honeywell 0.35u parameters from MOSIS----------

beta     = 0.6e10;              % Fowler-Nordhiem Tunneling Parameter
alpha    = 1.88e-6;             % Fowler-Nordhiem Tunneling Parameter
%----------Device/Process parameters----------
Xtun     = 80e-10;              % Tunneling Cross-section
                                % This is acutally the Gate-Oxide thickness.
B        = beta*Xtun;           % Fowler-Nordhiem Tunneling Constant
% ----------Capacitance values ----------
Eox      = 35.1345e-12;         % This should be in F/m.
```

```
Tox      = Xtun;                % Thickness of gate oxide.
Cdash_ox = Eox/Tox;


 ----------Transistor Gate Capacitance values----------
% PMOS Transistor (Wp/Lp)
Wp       = 0.9e-6;
Lp       = 0.4e-6;
Cpp      = Cdash_ox*Wp*Lp;
% NMOS Transistor (Wn/Ln)
Wn       = 3.6e-6;
Ln       = 0.4e-6;
Ctun     = Cdash_ox*Wn*Ln;
Atun     = Wn*Ln;
% Total Capacitance (Ctot)
Cgbo     = 3e-10;               % Gate to body capacitance
                                % obtained from the SPICE model files
Cbody    = Cgbo*Ln;
Ctot     = Cpp+Ctun+Cbody;
% ----------------------Kw, Ke Parameters -------------------
Kw       = Cpp/Ctot;
Ke       = 1 - (Cbody/Ctot);
% ----------------------Programming/Erasing Parameters ------
Vprog    = 11.0;                % Programming pulse amplitude
Vti      = 22.7;                % Threshold voltage of neutral cell
```

```
Vt_zero  = -2.0;                % Threshold voltage at time 0
tstart   = 5e-6;                % Start of the simulation time
tend     = 1e-3;                % End of simulation time

gend     = 1e-3;                % End of plotting the graph
% ------------------------Formulae and Calculations -----------
for i = 1:2
  E1_den   = Kw*(Vprog+Vti-Vt_zero);
  E1       = exp(B/E1_den);
  t        = linspace(tstart,tend,1000);
  A        = (Atun*alpha)/(Xtun*Ctot);
  result   = B./(Kw.*(log(A.*B.*t + E1)));
  if (i == 1)
    semilogx(t,Vti+Vprog-result,'-.')
    y1 = [t; Vti+Vprog-result];
    fid = fopen('d6_prog.txt','w');
    fprintf(fid,'%3.5f %3.5f\n',y1);
    fclose(fid)
  end
  grid on ;
  axis([tstart gend -4 10]);
  hold on;
  Vprog = Vprog + 2;
end
```

```
x_val = 1e-6*[0 5 15 25 35 45 55 65 75 85 95 105 115 125 135 145 165 185 205 225 245
                295 345 395 445 495 545 595 645 695 745 845 945];
y_val = [-1.97 -1.91 -1.73 -1.58 -1.45 -1.34 -1.23 -1.13 -1.02 -0.937 -0.852 -0.774 -0.693
          -0.603 -0.532 -0.489 -0.353 -0.247 -0.168 -0.0723 0.016 0.329 0.587 1.16 1.47
            1.63 1.72 1.86 1.97 2.07 2.13 2.29 2.47];
semilogx(x_val,y_val,'*')
leg = legend('Vprog(simu) = 11.0V','Vprog(expt) = 11.0V');
xlabel(' Time (in seconds)');
ylabel(' Threshold Voltage (Vth in Volts)');
```

C.2: Deprogramming/Erasing Time Dependence Model

```
% Let the aspect ratio of NMOS be 2/1, while the PMOS be 8/1. Then the Cgp/Cgn of the
FGD be 4/1;

clc
clear
% ----------Honeywell 0.35u parameters from MOSIS----------
beta     = 0.6e10;              % Fowler-Nordhiem Tunneling Parameter
alpha    = 1.88e-6;             % Fowler-Nordhiem Tunneling Parameter
%----------Device/Process parameters----------
Xtun     = 80e-10;              % Tunneling Cross-section
                                % This is acutally the Gate-Oxide thickness.
B        = beta*Xtun;           % Fowler-Nordhiem Tunneling Constant
```

```
% ---------------Capacitance values ------------------------
Eox      = 35.1345e-12;          % This should be in F/m.
Tox      = Xtun;                 % Thickness of gate oxide.
Cdash_ox = Eox/Tox;
% --------------Transistor Gate Capacitance values----------
% PMOS Transistor (Wp/Lp)
Wp       = 0.9e-6;
Lp       = 0.4e-6;
Cpp      = Cdash_ox*Wp*Lp;
% NMOS Transistor (Wn/Ln)
Wn       = 3.6e-6;
Ln       = 0.4e-6;
Ctun     = Cdash_ox*Wn*Ln;
Atun     = Wn*Ln;
% Total Capacitance (Ctot)
Cgbo     = 3e-10;                % Gate to body capacitance
                                 % obtained from the SPICE model files
Cbody    = Cgbo*Ln;
Ctot     = Cpp+Ctun+Cbody;
% ----------------------Kw, Ke Parameters -------------------
Kw       = Cpp/Ctot;
Ke       = 1 - (Cbody/Ctot);
% ----------------------Programming/Erasing Parameters ------
Vti      = 32.0;                 % Threshold voltage of neutral cell
```

```
Vt_zero  = 2.12;                % Threshold voltage at time 0
Verase   = 12.8;                % Erasing Pulse Amplitude
tstart   = 10e-6;               % Start of the simulation time
tend     = 1.367e-3;            % End of simulation time
gend     = 1.367e-3;            % End of plotting the graph
% ----------------------Formulae and Calculations ----------
for i = 1:1
  E2_den   = (Verase*Ke) + (Kw*Vt_zero) - (Kw*Vti);
  E2       = exp(B/E2_den);
  t        = linspace(tstart,tend,1e3);
  A        = (Atun*alpha)/(Xtun*Ctot);
  result   = B./(Kw.*(log(A.*B.*t + E2)));
  final    = Vti - (Verase*Ke/Kw) + result;
  if (i == 1)
    semilogx(t,final,'-.')
    y1 = [t; final];
    fid = fopen('d6_erase.txt','w');
    fprintf(fid,'%3.8f %3.8f\n',y1);
    fclose(fid)
  end
  grid on ;
  axis([tstart gend -8 4]);
  hold on;
  Verase = Verase + 2;
```

```
end
x_val = 1e-6*[0 10 20 30 40 50 60.03 70.06 80.09 90.14 100.19 110.24 120.27 140.3
                160.3 180.3 200.3 220.3 240.33 260.31 280.31 300.31 320.31 340.34
                360.37 380.4 400.43 440.43 480.43 520.43 570.43 620.43 670.43
                 720.43 770.43 869.93 969.43 1068.93 1168.43 1267.9 1367.43];
y_val = [2.26 2.12 2.01 1.9 1.8 1.69 1.62 1.54 1.45 1.37 1.24 1.22 1.17 1 0.851 0.685
          0.583 0.453 0.332 -0.0138 -0.202 -0.34 -0.432 -0.451 -0.531 -0.591 -0.654
         -0.763 -0.859 -0.942 -1.06 -1.18 -1.18 -1.23 -1.3 -1.45 -1.58 -1.71 -1.8 -1.89
         -1.99];
semilogx(x_val,y_val,'*')
leg = legend('Veras(simu) = 12.8V','Veras(expt) = 12.8V');
xlabel(' Time (in seconds)');
ylabel(' Threshold Voltage (Vth in Volts)');
```

Vita

Mr.Chandra Sekhar Acharyulu Durisety was born on June 26, 1976 in Nuzvid, a small town in the state of Andhra Pradesh, India. He did his primary education at St.Ann's English Medium High School, Nuzvid. He completed his secondary education at Andhra Muslim Sahakara Junior College, Guntur, after which he joined Birla Institute of Technology and Sciences, Pilani, 5th best University in India.

Later he joined Wipro Infotech Ltd, Global R & D, Bangalore as a VLSI Design Engineer and got promoted to Sr.VLSI Design Engineer in 1999. His expertise include implementing networking protocols in FPGA's. He lead a 4 member team to develop the generic Utopia core for interfacing ATM and Physical layers, before leaving Wipro. Later he joined CMOS Chips Inc., Santa Clara, CA as Member Technical-ASIC and contracted to Toshiba America Electronic Components (TAEC), San Jose. During his work, he developed various verilog models for memory blocks, shell scripts for test process automation and developed methodologies and strategies for the system level verification of designs targeted for FPGAs. His research interests include analog circuit design, developing algorithms for VLSI design and mixed signal designs. His interest in Analog VLSI was the driving force behind leaving his job for higher education. After joining Mississippi State University, he joined Dr. Benjamin Blalock's group as a Graduate Research Assistant. He plans to pursue his Ph.D in Electrical Engineering under the guidance of Dr.Benjamin J. Blalock.