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HYBRID PHASE-LOCKED LOOP SYNCHRONOUS VIDEO DETECTOR
FOR TELEVISION RECEIVER

A Thesis
Presented for the
Master of Science
Degree
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Hiroyuki Iga
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ABSTRACT

A new hybrid Phase-Locked Loop (PLL) synchronous video detector for a television receiver was developed. It contains a new hybrid PLL using a conventional analog PLL synchronous video detector. It has three modes, namely, the analog PLL mode in the initial step, the hybrid PLL continuous (C) mode in the intermediate step, and the hybrid PLL sample and hold (S/H) mode in the last step. The new detector with the precise sample and hold function eliminates the phase fluctuation caused by the heavy ghost signal with a power ratio to the main signal larger than -15 dB. The ghost signal is a reflected signal by a high building or other large object and results in the double-image interference. Thus, the new detector helps to reduce the ghost signal, enabling the ghost reduction system to function better.

Only the hybrid PLL was analyzed, since the remaining part of the detector can be designed by conventional methods. Design equations were derived from this study, and the results given by these equations were close to those obtained from the computer analysis. FORTRAN and ACSL (Advanced Continuous Simulation Language) were used for the computer analysis.

From a specified set of possible physical conditions and the results obtained through the analysis, a stable and practical hybrid PLL was obtained. The required resolution of the detector's A/D converter was 8 bit/V, and that of its D/A was 16

bit/V. Its output phase jitter for moderate input signal-to-noise ratio (37 dB) was 0.091 deg for the C mode and 0.26 deg for the S/H mode. Its pull-in time for the C mode was 97 ms for 500.0 kHz step frequency change. Its pull-in time for the S/H mode was 1.2 ms for 10.0 kHz step frequency change. Its output phase drift for an input signal-to-noise ratio of 37 dB was 1.0 deg for the S/H mode. This value is considerably smaller than the phase fluctuation of the corresponding analog PLL because of the heavy ghost (delay of 10 μ s and phase of 180 deg). This conventional analog PLL has a phase fluctuation of 11.5 deg or 3.6 deg, depending upon the characteristics of the PLL. Improved phase fluctuation makes the detector more practical and satisfactory, especially in eliminating ghost interference.

The parameter values shown in this study are only for one example. However, for any set of given conditions, the suitable parameter values to realize a specific hybrid PLL synchronous video detector can be obtained from the equations derived in this study and the computer analysis.

TABLE OF CONTENTS

CHAPTER	PAGE
I. INTRODUCTION	1
II. REVIEW OF PHASE-LOCKED LOOPS	4
Phase-Locked Loop	4
Analog Phase-Locked Loops	4
Linear Model	4
Acquisition and Tracking Parameters	10
Linear Model with Additive Noise	12
Digital Phase-Locked Loops	14
III. APPLICATION OF PLL IN TELEVISION VIDEO DETECTORS . . .	16
Analog PLL Synchronous Video Detectors	16
Disadvantage of Analog PLL Synchronous	
Video Detectors	22
IV. PROPOSED HYBRID PLL SYNCHRONOUS VIDEO DETECTOR	26
Overview of the Proposed Detector	26
Configuration and Operation	27
V. LINEAR ANALYSIS OF PROPOSED PLL	33
Linear Models	33
Linear Model of Original Analog PLL	33
Linear Model of Hybrid PLL	36
Stability Analysis	41
Output Phase Jitter	48
Effect of A/D Quantization Noise	48
Effect of D/A Quantization Noise	61

CHAPTER	PAGE
Effect of Input Noise	66
Computer Analysis and Discussion	73
Output Phase Drift in Hold Period	80
VCO Input Jitter	82
Effect of A/D Quantization Noise	82
Effect of D/A Quantization Noise	84
Effect of Input Noise	84
Computer Analysis and Discussion	87
Jitter of Integration Path in Loop Filter	92
Tracking Performance	98
Comparison	101
VI. SUMMARY AND CONCLUSIONS	103
Summary	103
Conclusions	104
LIST OF REFERENCES	107
VITA	108

LIST OF TABLES

TABLE	PAGE
3.1. Composite phase ϕ	24
5.1. Phase margin of hybrid PLL	46
5.2. Gain margin of hybrid PLL	46
5.3. Overshoot of hybrid PLL	47
5.4. Stability of original analog PLL	47

LIST OF FIGURES

FIGURE	PAGE
2.1. Basic block diagram of the PLL	5
2.2. Linear model of the analog PLL	8
3.1. Block diagram of analog PLL video detector	17
3.2. Basic block diagram of a television receiver with the PLL video detector	19
3.3. Overall IF response of the television receiver with the PLL video detector	21
3.4. Envelope of IF signals	23
3.5. Vector representation	23
3.6. Generated carrier phases and detected waveforms . . .	24
4.1. Block diagram of hybrid PLL synchronous television video detector	28
4.2. Timing chart of SWs	29
5.1. Bode plot of open-loop transfer function of original analog PLL	35
5.2. Linear model of hybrid PLL	37
5.3. Actual television horizontal signal, sample period, and hold period	40
5.4. Hybrid PLL model for stability analysis	42
5.5. Nyquist plots of open-loop transfer functions	49
5.6. Discrete model to analyze the output phase jitter caused by the A/D quantization noise	50

FIGURE	PAGE
5.7. Continuous model to analyze the output phase jitter caused by the A/D quantization noise	55
5.8. Bode plot of the transfer function $H_q(j\omega)$ from the A/D quantization noise to the output phase	57
5.9. Continuous model to analyze the output phase jitter caused by the D/A quantization noise	62
5.10. Bode plot of the transfer function $H_q(j\omega)$ from the D/A quantization noise to the output phase	64
5.11. Continuous model to analyze the output phase jitter caused by the input noise	68
5.12. Bode plot of the transfer function $H_n(j\omega)$ from the input to the output	70
5.13. Output phase jitter versus A/D resolution	75
5.14. Output phase jitter versus input SNR (The effect of pre-alias filter)	77
5.15. Output phase jitter versus D/A resolution	79
5.16. Output phase jitter versus input SNR (The effect of sample and hold mode)	81
5.17. Bode plot of the transfer function $H_q(j\omega)$ from the A/D quantization noise to the VCO input	83

FIGURE	PAGE
5.18. Bode plot of the transfer function $H_n(j\omega)$ from the input to the VCO input	85
5.19. VCO input jitter and corresponding output phase drift versus A/D resolution	88
5.20. VCO input jitter and corresponding output phase drift versus D/A resolution	89
5.21. VCO input jitter and corresponding output phase drift versus input SNR	91
5.22. Discrete model to analyze the jitter of the integration path in the digital loop filter caused by the input noise	93
5.23. Integration path jitter and corresponding output phase drift versus input SNR	97
5.24. Characteristic of phase/frequency detector	100

LIST OF ABBREVIATIONS

ABBREVIATIONS	DEFINITIONS
A	Analog
ACSL	Advanced continuous simulation language
ALF	Analog loop filter
AM	Amplitude modulation
Amp.	Amplifier
APLL	Analog phase-locked loop
A/D	Analog to digital converter
C mode	Hybrid PLL continuous mode
CRT	Cathode ray tube
D	Digital
Det.	Detector
DLF	Digital loop filter
DPLL	Digital phase-locked loop
D/A	Digital to analog converter
FM	Frequency modulation
H	Hold
HPLL	Hybrid phase-locked loop
H Sync.	Horizontal synchronization
IC	Integrated circuit
IF	Intermediate frequency
LD	Lock detector
LF	Loop filter

ABBREVIATIONS	DEFINITIONS
LPF	Low-pass filter
PD	Phase detector
PF	Pre-alias filter
PLL	Phase-locked loop
PS	Phase shifter
S	Sample
SC	Sequence controller
SNR	Signal-to-noise ratio
SW	Switch
S/H mode	Hybrid PLL sample and hold mode
VCO	Voltage-controlled oscillator
VHF	Very high frequencies

CHAPTER I

INTRODUCTION

Digital techniques have been widely applied to various engineering fields, because they have features that analog techniques do not have. One of the most important features is that a digital system can store the information without decay and process it more exactly than its analog counterpart.

Digital techniques have been recently applied to the television industry. They are used in the video (baseband) stage of television receivers to add such new features as still picture (stop motion) and ghost (multi-image) interference reduction [1]. However, only analog techniques are used in the intermediate frequency (IF) stage because the IF frequency is too high to be processed by digital techniques. The IF frequencies of television receivers in U.S.A. and Japan are 45.75 MHz and 58.75 MHz, respectively [2], [3]. The video detector located between the IF stage and the video stage also uses only analog techniques.

Since ghost interference is a very serious problem for terrestrial broadcasting systems, ghost reduction systems have been researched and developed. Though linearly detected ghosts can be canceled in the video stage by a linear filter such as transversal filter, the following two factors degrade the performance of a conventional ghost reduction system in the video stage [1]. One is the non-linearity of analog multipliers in the

transversal filter. The other is the non-linearity of the video detector. The former is expected to be solved by an all digital transversal filter in the near future. Though the latter can be solved by a perfect synchronous video detector for broadcasting station use, it is too expensive to be used in the television receiver.

The most advanced video detector available in television receivers uses phase-locked loop (PLL) techniques [4], [5], [6], and is called a PLL synchronous video detector. It is a linear detector, as long as the phase of the carrier signal is not affected by heavy ghosts. However, once the phase of the carrier signal is over-modulated by the heavy ghost signal, with a power ratio to the main signal larger than -15 dB, the PLL follows the over-modulated phase and does not maintain constant phase. Thus, it is not a linear detector any longer in such circumstances, and the detected heavy ghost can not be canceled by conventional technology [1].

If the PLL in the detector operates in the period of the least fluctuated phase and holds its output phase in the rest of the video signal period, it generates the correct carrier, and the linearly detected video signal is obtained. This method needs the following two functions. One is to detect the period of the least fluctuated phase. The other is to hold the PLL operation as exactly as possible. Fortunately, the former is not always necessary because the horizontal synchronization signal, where

over-modulation due to heavy ghosts normally does not occur, can be used for the PLL operation instead of detecting the least fluctuated phase period. The latter is indispensable and requires a precise ~~hold circuit that analog circuits can hardly realize.~~

The objective of this thesis research is to improve the phase fluctuation and the linearity of a PLL synchronous video detector under the existence of heavy ghosts by applying digital techniques to its PLL.

CHAPTER II

REVIEW OF PHASE-LOCKED LOOPS

Phase-Locked Loop

Phase-locked loop (PLL) has been used in the communication system since the nineteen-twenties [7]. The basic and important function of a PLL is to synchronize its output with its input not only in frequency but also in phase. The PLL consists of a phase detector (PD), loop filter (LF), and voltage-controlled oscillator (VCO) as shown in Figure 2.1. One input of the PD is the input signal of the PLL, $r(t)$, and the other is the VCO output signal, $c(t)$. The PD detects the phase difference between $r(t)$ and $c(t)$ and gives the result $e(t)$ to the LF. The LF, which is a first-order low-pass filter, rejects undesirable high frequency components in $e(t)$ and gives the result $v(t)$ to the VCO.

Analog Phase-Locked Loops

Every component of the analog phase-locked loop (APLL) is analog type. The APLLs have been studied since the nineteen-twenties [7]. One of the most basic linear models and the important equations will be introduced here.

Linear Model. The PD in the linear model is an analog multiplier called a four-quadrant multiplier. To simplify the discussion, assume that both the input signal $r(t)$ and the VCO output signal $c(t)$ are sine-waves with the same frequency ω ,

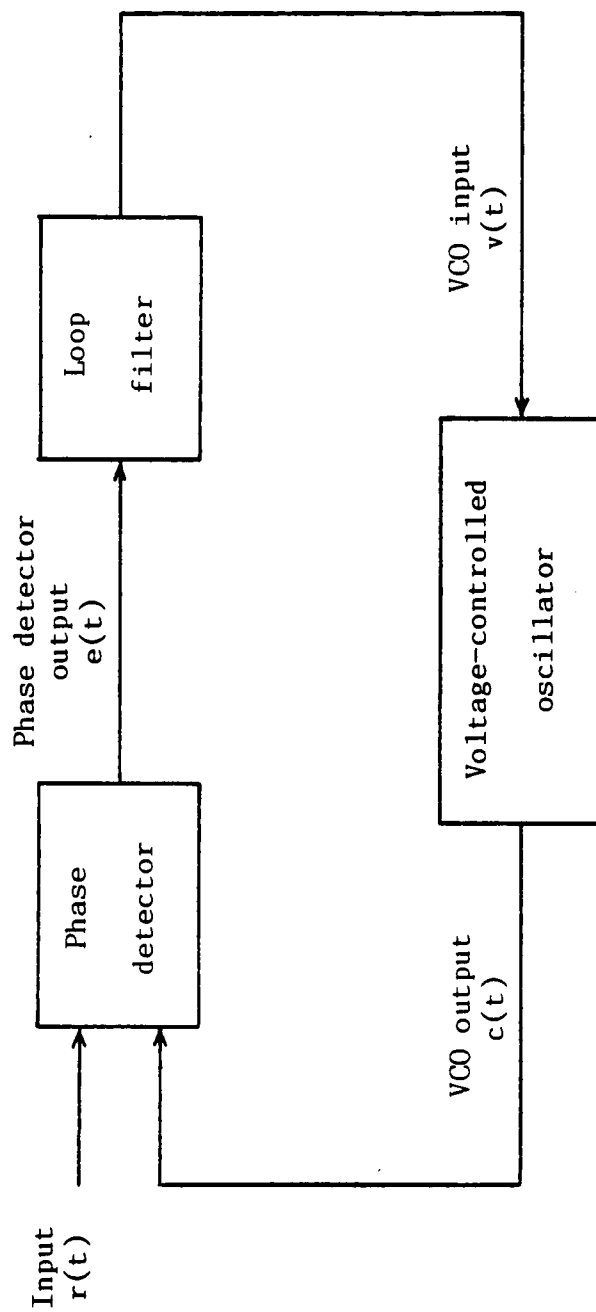


Figure 2.1. Basic block diagram of the PLL.

$$r(t) = \sqrt{2} A_r \sin\{\omega t + \theta_r(t)\} \quad (2-1)$$

$$c(t) = \sqrt{2} A_c \cos\{\omega t + \theta_c(t)\} \quad (2-2)$$

where A_r and A_c are the amplitudes, and $\theta_r(t)$ and $\theta_c(t)$ the phases of $r(t)$ and $c(t)$, respectively. The PD multiplies these two signals, so its output signal $e(t)$ is expressed as

$$e(t) = A_r A_c [\sin\{\theta_r(t) - \theta_c(t)\} + \sin\{2\omega t + \theta_r(t) + \theta_c(t)\}]. \quad (2-3)$$

Since the second high frequency component is nearly completely filtered out by the LF, only the first low frequency component is taken into consideration. Furthermore, using the approximation, $\sin\theta_e = \theta_e$ for $\theta_e < 1$ rad, the first component is approximated as

$$e(t) = K_d \theta_e(t) \quad V \quad (2-4)$$

where

$$K_d = A_r A_c \quad V/\text{rad} \quad (2-5)$$

$$\theta_e(t) = \theta_r(t) - \theta_c(t) \quad \text{rad.} \quad (2-6)$$

Although this approximation generates a 16 % error for $\theta_e = 1$ rad, it is considered to be valid especially in this engineering field. Parameters K_d and $\theta_e(t)$ are called phase-detector gain and phase error, respectively. By using Laplace transform, Equations (2-4) and (2-6) are expressed as

$$E(s) = K_d \theta_e(s) \quad V \quad (2-7)$$

$$\theta_e(s) = \theta_r(s) - \theta_c(s) \quad \text{rad.} \quad (2-8)$$

The LF is usually a first-order low-pass type, and its transfer function $F(s)$ in Laplace transform is expressed as

$$F(s) = (1 + \tau_2 s) / (\tau_1 s) \quad (2-9)$$

or

$$F(s) = (1 + \tau_2 s) / \{1 + (\tau_1 + \tau_2)s\}. \quad (2-10)$$

The former is called the transfer function of the active filter, and the latter the passive filter, where $\tau_1 s$ and $\tau_2 s$ are called time constants. Thus, its output signal $V(s)$ in Laplace transform is given by

$$V(s) = E(s)F(s) \quad V. \quad (2-11)$$

Since the VCO generates a sine-wave with frequency ω which varies according to its input signal $v(t)$, the Laplace transform of the output phase $\theta_c(s)$ is expressed as

$$\theta_c(s) = V(s)K_0/s \quad \text{rad} \quad (2-12)$$

where K_0 is called VCO gain rad/s/V. Figure 2.2 shows the linear model of the analog PLL. This figure contains additive noise $N'(s)$ which is assumed zero for the present discussion.

The open-loop transfer function $T(s)$ and the closed-loop phase transfer function $H_p(s)$ are obtained from Equations (2-7) through (2-12)

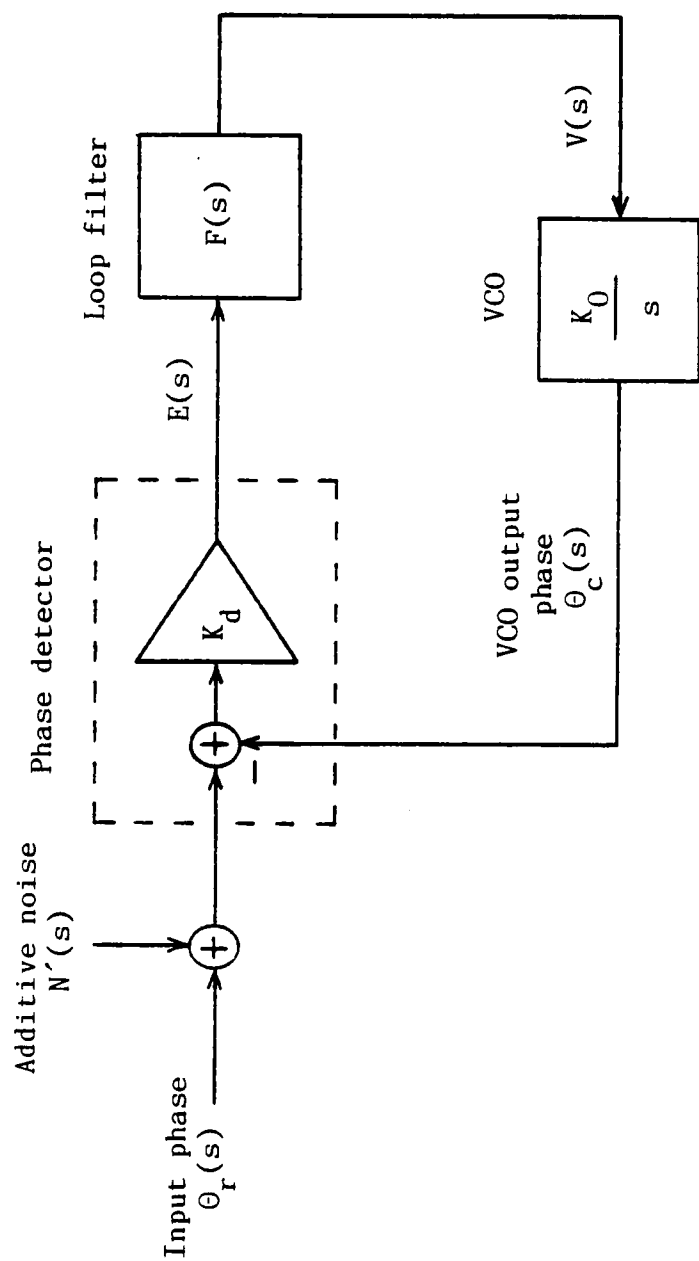


Figure 2.2. Linear model of the analog PLL.

$$T(s) = KF(s)/s \quad (2-13)$$

$$H_p(s) \equiv \Theta_c(s)/\Theta_r(s) = T(s)/(1 + T(s)) \quad (2-14)$$

$$K = K_d K_0 \quad 1/s \quad (2-15)$$

where K is called loop gain. From Equations (2-9), (2-13), and (2-14), the closed-loop phase transfer function for the active filter is given by

$$H_p(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2-16)$$

where

$$\omega_n = (K/\tau_1)^{\frac{1}{2}} \quad \text{rad/s} \quad (2-17)$$

$$\zeta = (\tau_2/2)(K/\tau_1)^{\frac{1}{2}}. \quad (2-18)$$

ω_n and ζ are called natural frequency and damping factor, respectively. From Equations (2-10), (2-13), and (2-14), the closed-loop phase transfer function for the passive filter is given by

$$H_p(s) = \frac{\omega_n(2\zeta - \omega_n/K)s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2-19)$$

where

$$\omega_n = \{K/(\tau_1 + \tau_2)\}^{\frac{1}{2}} \quad \text{rad/s} \quad (2-20)$$

$$\zeta = 0.5\{K/(\tau_1 + \tau_2)\}^{\frac{1}{2}}(\tau_2 + 1/K). \quad (2-21)$$

Most practical PLLs satisfy the condition

$$K \gg \omega_n, \quad (2-22)$$

and these PLLs are called high-gain PLLs. If this condition is satisfied, Equation (2-19) can be approximated to (2-16).

Furthermore, most practical PLLs satisfy the conditions

$$\tau_1 \gg \tau_2 \quad (2-23)$$

$$\tau_2 \gg 1/K, \quad (2-24)$$

so Equations (2-20) and (2-21) can be approximated to (2-17) and (2-18), respectively. This approximation means that most high-gain PLLs with passive loop filters can be approximated to the same PLLs with active loop filters.

Acquisition and Tracking Parameters. Important parameters of acquisition and tracking process are introduced here for further discussion. The following equations and some descriptions are quoted from reference [6].

The frequency range within which the PLL is statically stable is called the hold range $\Delta\omega_h$ rad/s.

$$\Delta\omega_h = \infty \quad (\text{theoretically for the active filter}) \quad (2-25)$$

$$= K \quad (\text{for the passive filter}) \quad (2-26)$$

The frequency range within which the PLL locks within single phase fluctuation is called the lock range $\Delta\omega_L$ rad/s.

$$\Delta\omega_L \approx 2\zeta\omega_n \quad (2-27)$$

The time required for the lock-in process is called the lock-in time T_L s.

$$T_L \approx 1/\omega_n \quad (2-28)$$

The frequency range within which the PLL locks slowly with a lot of phase fluctuations is called the pull-in range $\Delta\omega_p$ rad/s.

$$\Delta\omega_p = \infty \quad (\text{for the PLL with active filter}) \quad (2-29)$$

$$\approx 2.55(\zeta\omega_n K)^{\frac{1}{2}} \quad (\text{for high-gain PLL}) \quad (2-30)$$

The time required for the pull-in process is called the pull-in time T_p s

$$T_p \approx \Delta\omega^2 / (2\zeta\omega_n^3) \quad (2-31)$$

where $\Delta\omega$ is the initial (angular) frequency difference between the input and the output.

The frequency range within which the PLL is dynamically stable is called the pull-out range $\Delta\omega_{po}$ rad/s.

$$\Delta\omega_{po} \approx 1.8\omega_n(\zeta + 1) \quad (2-32)$$

Linear Model with Additive Noise. The additive noise in the linear PLL model shown in Figure 2.2 (pp. 8) is introduced here.

Generally, the input signal $r(t)$ and the input noise $n(t)$ come from some band-pass filter which has symmetrical bandwidth B_1 with center angular frequency $\omega (= 2\pi f)$, so the input noise $n(t)$ can be expressed as

$$n(t) = \sqrt{2} \{n_1(t) \times \sin \omega t + n_2(t) \times \cos \omega t\}. \quad (2-33)$$

It can be assumed that the in-phase noise component $n_1(t)$ and the quadrature noise component $n_2(t)$ are two low frequency random processes which are Gaussian, stationary, and statistically independent. Thus, they have the zero mean and the same variance given by

$$\overline{n_1(t)^2} = \overline{n_2(t)^2} = \overline{n(t)^2}/2 = \sigma^2/2 \quad \text{rad}^2. \quad (2-34)$$

By the same procedure which yields Equation (2-4), the phase detector output signal $e(t)$ with additive noise $n(t)$ is given by

$$e(t) = K_d \{\theta_r(t) - \theta_c(t) + n'(t)\} \quad V \quad (2-35)$$

where the last term is the noise component and is expressed as

$$n'(t) = \{-n_1(t) \times \sin \theta_c(t) + n_2(t) \times \cos \theta_c(t)\} / A_r \quad \text{rad}. \quad (2-36)$$

Thus, the linear model of the additive noise is given by

Figure 2.2 (pp. 8). $N'(s)$ in Figure 2.2 (pp. 8) is the Laplace transform of Equation (2-36).

The variance of this noise component, σ'^2 , is given by

$$\sigma'^2 = \sigma^2 / (2A_r^2) \quad \text{rad}^2. \quad (2-37)$$

On the other hand, the signal-to-noise ratio of the input signal, $(\text{SNR})_i$, is defined by

$$(\text{SNR})_i = A_r^2 / \sigma^2. \quad (2-38)$$

From Equations (2-37) and (2-38),

$$\sigma'^2 = 1 / \{2(\text{SNR})_i\} \quad \text{rad}^2 \quad (2-39)$$

is obtained.

The variance of the output phase, $\sigma_{\theta_c}^2$, is calculated by the following integration.

$$\sigma_{\theta_c}^2 = \int_{-\infty}^{\infty} S_n(j2\pi f) |H_p(j2\pi f)|^2 df \quad \text{rad}^2 \quad (2-40)$$

where $H_p(j2\pi f)$ is the closed-loop phase transfer function given by Equation (2-16) or (2-19), and $S_n(j2\pi f)$ is the power spectrum of the input noise given by

$$S_n(j2\pi f) = \sigma'^2 / B_i \quad \text{rad}^2/\text{Hz} \quad (2-41)$$

where B_i means the IF bandwidth. From substituting Equation (2-41) into (2-40),

$$\sigma_{\theta_c}^2 = 2\sigma'^2 B_L / B_i \quad \text{rad}^2 \quad (2-42)$$

is obtained. B_L is called noise bandwidth and is defined by

$$B_L = \int_0^{\infty} |H_p(j2\pi f)|^2 df \quad \text{Hz.} \quad (2-43)$$

In addition, from substituting Equation (2-39) into (2-42),

$$\sigma_{\theta c}^2 = B_L / \{B_i (\text{SNR})_i\} \quad \text{rad}^2 \quad (2-44)$$

is obtained. Furthermore, the substitution of Equation (2-16) or (2-19) into (2-43) yields the following noise bandwidth B_L of the PLL with active or passive loop filter, respectively.

$$B_L = 0.5\omega_n (\zeta + 0.25/\zeta) \quad \text{Hz (active filter)} \quad (2-45)$$

$$B_L \approx 0.5\omega_n (\zeta + 0.25/\zeta) \quad \text{Hz (passive filter)} \quad (2-46)$$

Digital Phase-Locked Loops

Any phase-locked loop containing a digital circuit can be called a digital PLL (DPLL). DPLLs have been intensively researched since the nineteen-sixties for the following three purposes [7]. The first is to stabilize its performance. The second is to improve its performance and reliability. The last is to reduce its size and cost and to improve its productivity by integrating it into one or more integrated circuits (ICs). For the first and second purposes, some analog block (for example, the PD, the LF, or the VCO in the analog PLL) is replaced by a digital circuit according to its application. This approach has been

studied since the nineteen-sixties [7], and these PLLs are called hybrid PLLs (HPLLs). For the last purpose, every block of the PLL is realized by digital components, a microprocessor and software. This approach has been studied since the nineteen-seventies [7], and these PLLs are called all-digital PLLs.

CHAPTER III

APPLICATION OF PLL IN TELEVISION VIDEO DETECTORS

Analog PLL Synchronous Video Detectors

The function of a television video detector is to demodulate the television Intermediate Frequency (IF) signal and detect the baseband video signal. Recently, the phase-locked loop (PLL) has been applied in television video detectors [4], [5]. These detectors are realized only by analog components and called analog PLL synchronous video detectors. Figure 3.1 shows its block diagram. To simplify the explanation of the block diagram, assume that the input signal $r(t)$ is an amplitude modulated (AM) IF signal expressed as

$$r(t) = (1 + k s(t)) \sin(\omega t) \quad (3-1)$$

where $s(t)$ is the baseband video signal accompanied with the frequency modulated (FM) sound signal, $\sin(\omega t)$ is the carrier of the IF signal, and k is the modulation index. The input signal $r(t)$ is fed into two analog multipliers. One is called the quadrature detector that is the same as the phase detector in the PLL which is shown in Figure 2.1 (pp. 5). The other is called the in-phase detector. It multiplies the input signal $r(t)$ by the IF carrier $\sin(\omega t)$ generated by the PLL. Then, the low-pass filter rejects the undesirable 2ω component and produces the demodulated output signal $s(t)$. This circuit acts as a synchronous detector

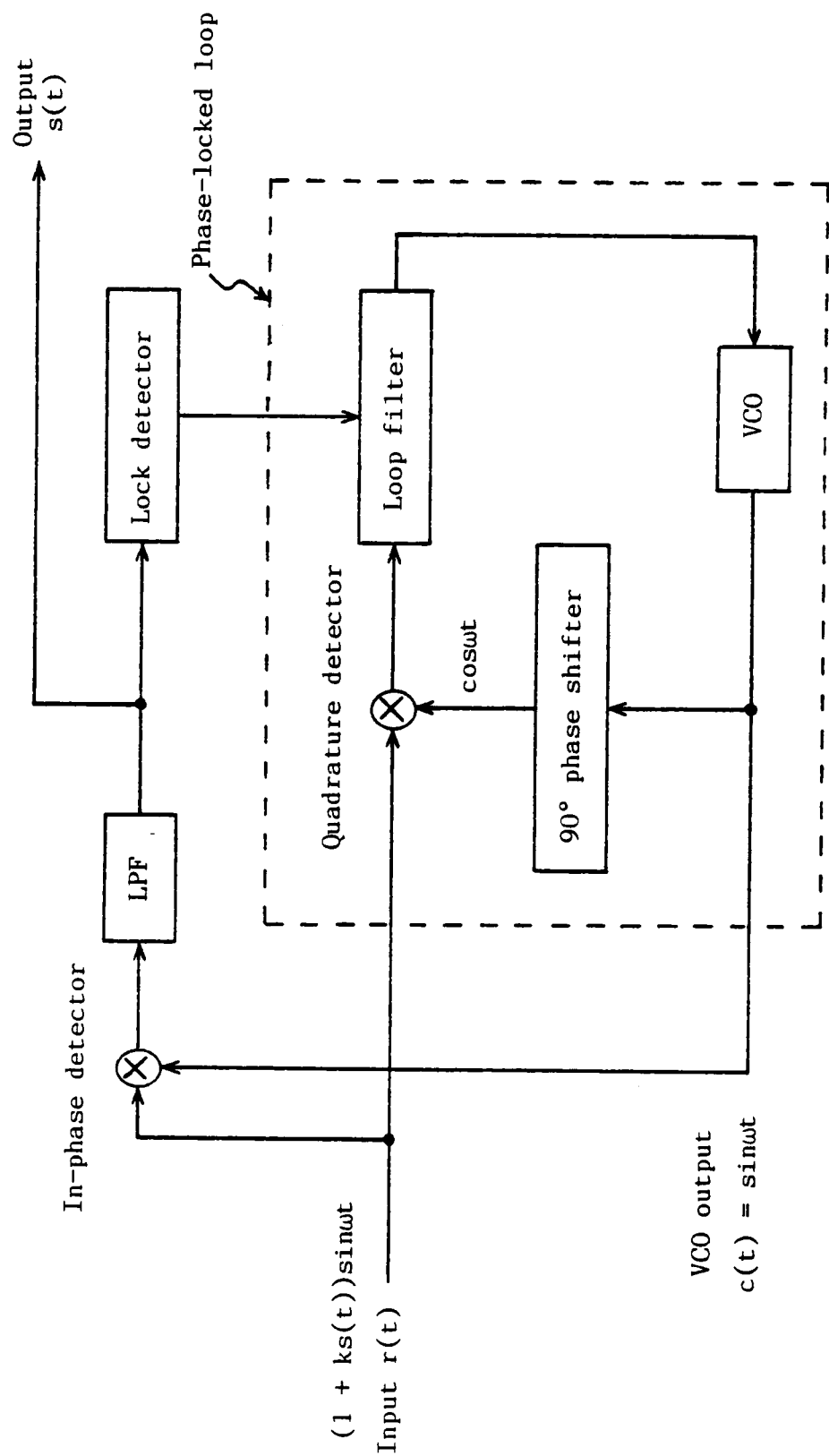


Figure 3.1. Block diagram of analog PLL video detector.

when the PLL generates the correct IF carrier. Although the lock detector is not an essential component for the analog PLL detector, it is essential for the hybrid PLL detector which will be proposed later. Before the PLL finishes synchronizing its output with its input (when it is in the un-lock state), its output signal contains little constant component. Thus, the mean of its output signal is nearly equal to zero. After the PLL finishes the synchronization (when it is in the lock state), the output signal contains a detectable constant component. Therefore, the lock detector can detect the lock state and the un-lock state by examining the mean of the PLL output signal [4]. When it detects the un-lock state, a wide-band loop filter is used to widen the pull-in frequency range. When it detects the lock state, a narrow-band loop filter is used to reduce the phase jitter of the generated carrier.

Before discussing advantages of the analog PLL synchronous video detector, a basic block diagram of a television receiver with a PLL synchronous video detector should be introduced (Figure 3.2). The following descriptions are from reference [2]. The tuner selects a desired channel, amplifies the selected signal, and converts the incoming RF (54 MHz to 890 MHz) signal into the IF signal (45.75 MHz) by superheterodyne technique. The IF amplifier amplifies the IF signal and adjusts the shape of its spectrum for the demodulation. The overall IF response of the television receiver with a PLL synchronous video detector is shown

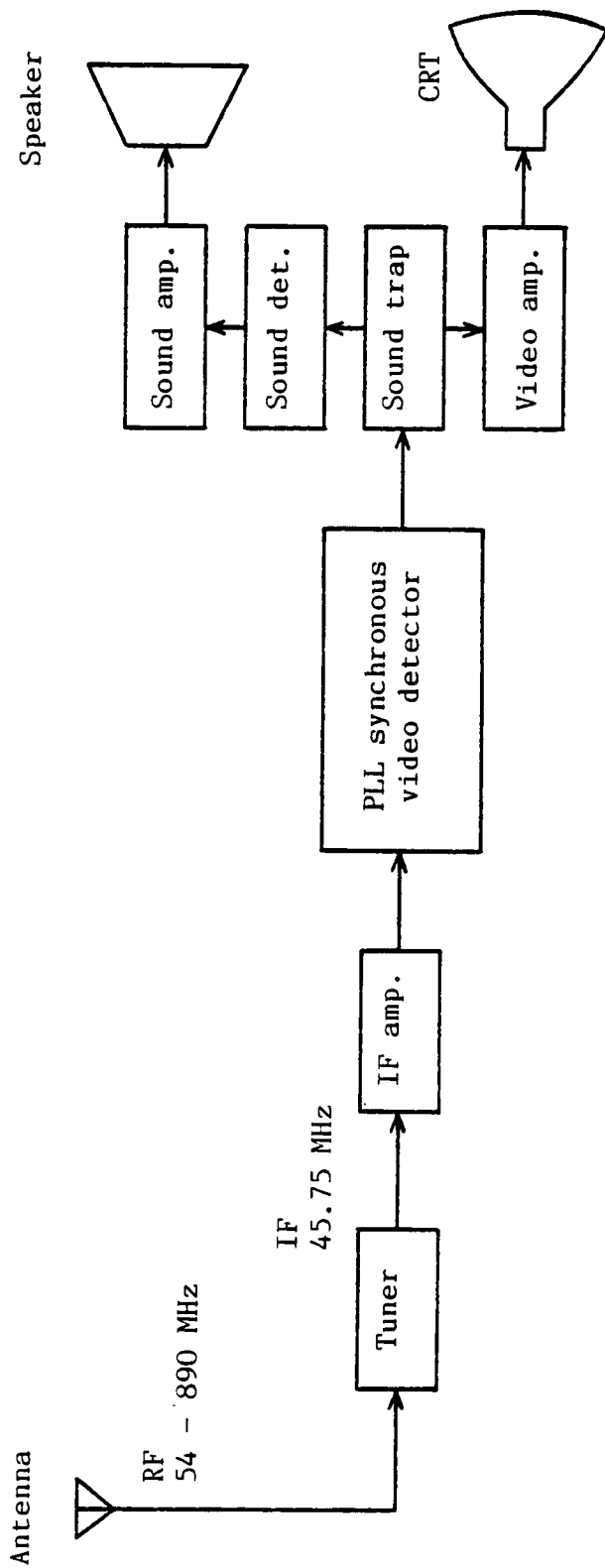


Figure 3.2. Basic block diagram of a television receiver with the PLL video detector.

in Figure 3.3. Since the locally generated frequency in the tuner is placed above the incoming RF signals by an amount equal to the IF frequency, the frequency component of the IF signal is reversed. Thus, the frequency axis in Figure 3.3 is drawn backward. The levels of the ripples outside the desired IF signal are not clearly specified so that the important response for the desired IF signal and the carrier signals can be realized at a low cost. The sound carrier is suppressed in order to reduce the crosstalk generated in the detector. The detector detects the baseband video signal accompanied with the FM sound signal. The sound trap picks up the FM sound signal. This sound signal is demodulated, amplified, and fed into the speaker. The remainder is the baseband video signal, which is amplified and fed into the cathode ray tube.

When the PLL generates the correct IF carrier, this detector acts as a synchronous detector. Its linearity, which is much better than that of conventional detectors such as the envelope detector and the quasi synchronous detector, yields the following two advantages [4], [5]:

- (1) the reduction of the crosstalk among the picture IF carrier, the color subcarrier, and the sound IF carrier shown in Figure 3.3;

- (2) the reduction of the cost by using the PLL synchronous video detector for detecting not only the baseband video signal but also the FM sound signal.

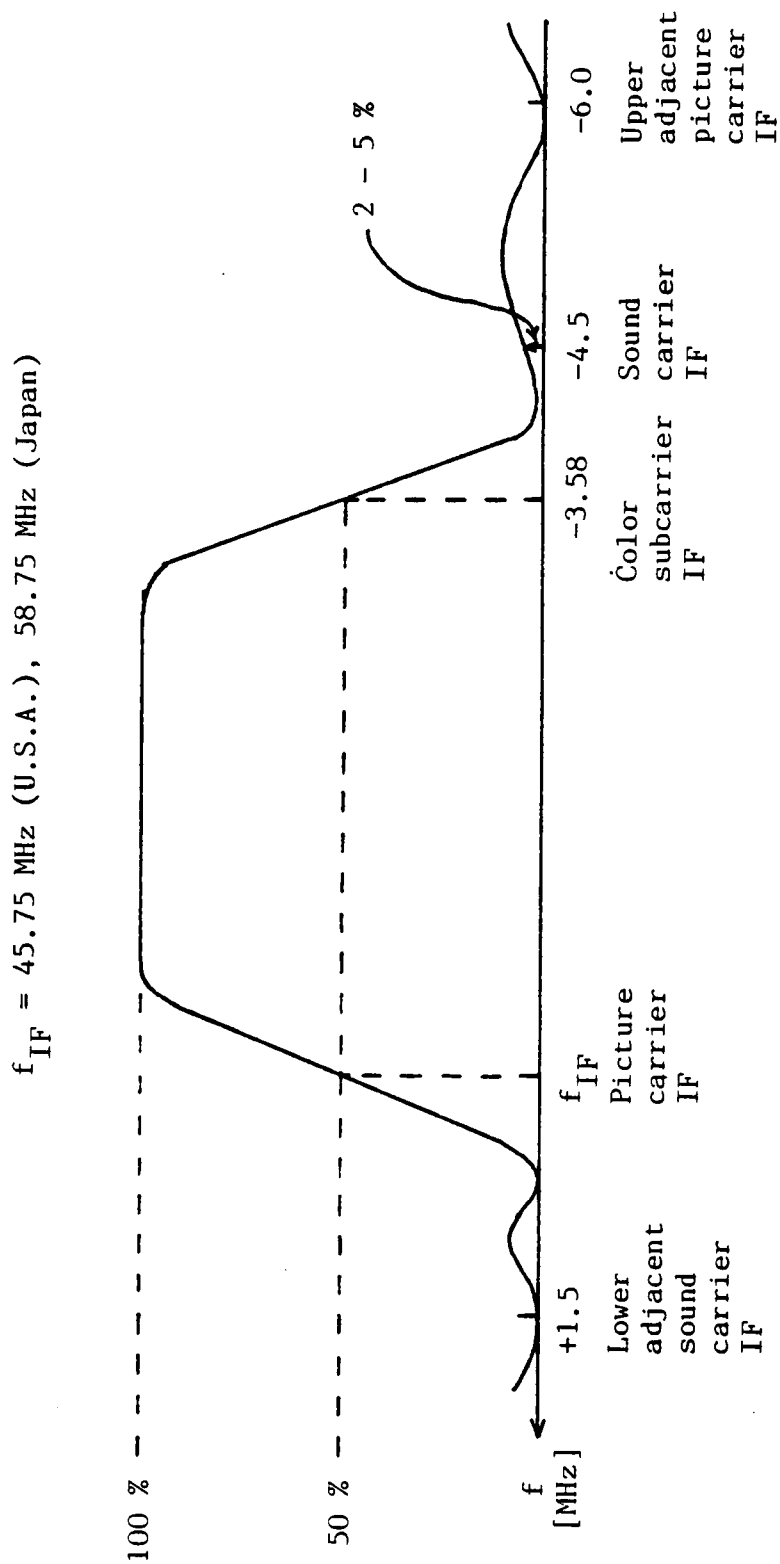


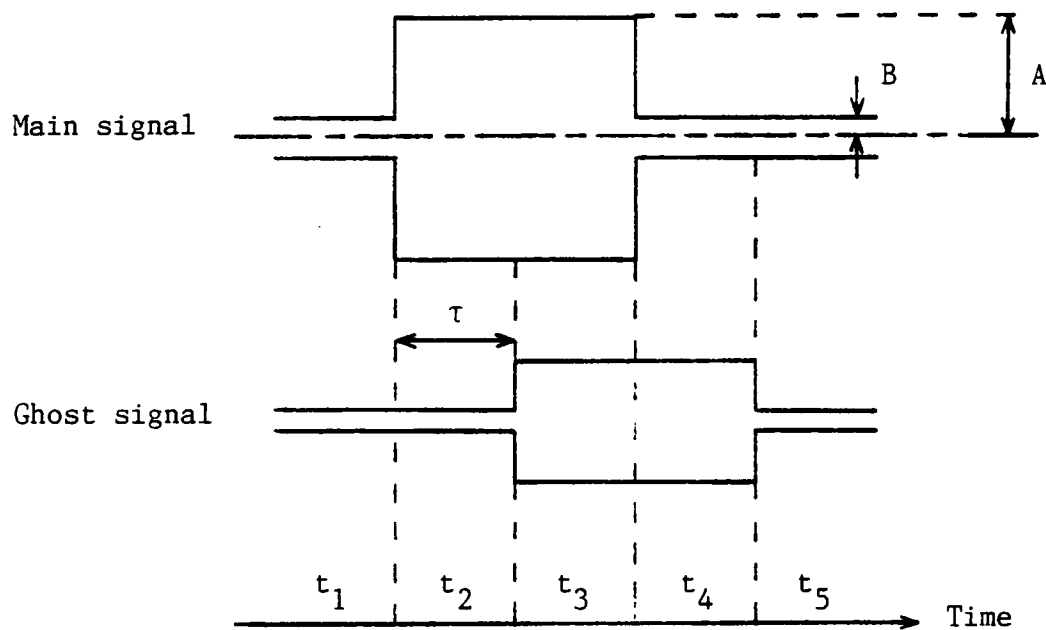
Figure 3.3. Overall IF response of the television receiver with the PLL video detector.

Disadvantage of Analog PLL Synchronous Video Detectors

When heavy ghost interference exists, the analog PLL synchronous video detector can not maintain the linearity any longer. Thus, the detected ghost is not linear distortion any longer and can not be canceled by the linear equalizer in the video stage. Since the received signal via a terrestrial broadcasting system almost always suffers ghost interference, this non-linearity problem should be solved.

This problem is explained by using Figures 3.4 through 3.6 and Table 3.1. These figures and table are from reference [8]. Figure 3.4 shows the envelope of the two IF signals. One is the main signal, and the other is the ghost signal with delay τ . The original video signal is a square waveform which is affected more than any other waveform by the non-linearity of the detector. Since the television signal is negatively modulated, the relative amplitude of the black level and the white level are 75 % and 12.5 %, respectively. The composite signal, the addition of the main signal and the ghost signal, is fed into the video detector. Figure 3.5 shows their vector representation. The phase θ and ϕ express the phase difference of the ghost signal and the composite signal from the main signal, respectively. Define $m(t)$ as the ratio of the amplitude of the ghost signal to the main signal. Then, the following equation is obtained.

$$\sin\phi = m(t) \times \sin(\theta - \phi) \quad (3-2)$$



Black level: $A = 0.75$, white level: $B = 0.125$,
video signal: square.

Figure 3.4. Envelope of IF signals.

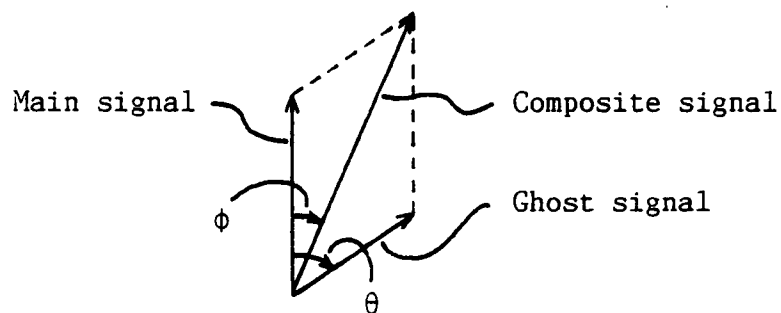
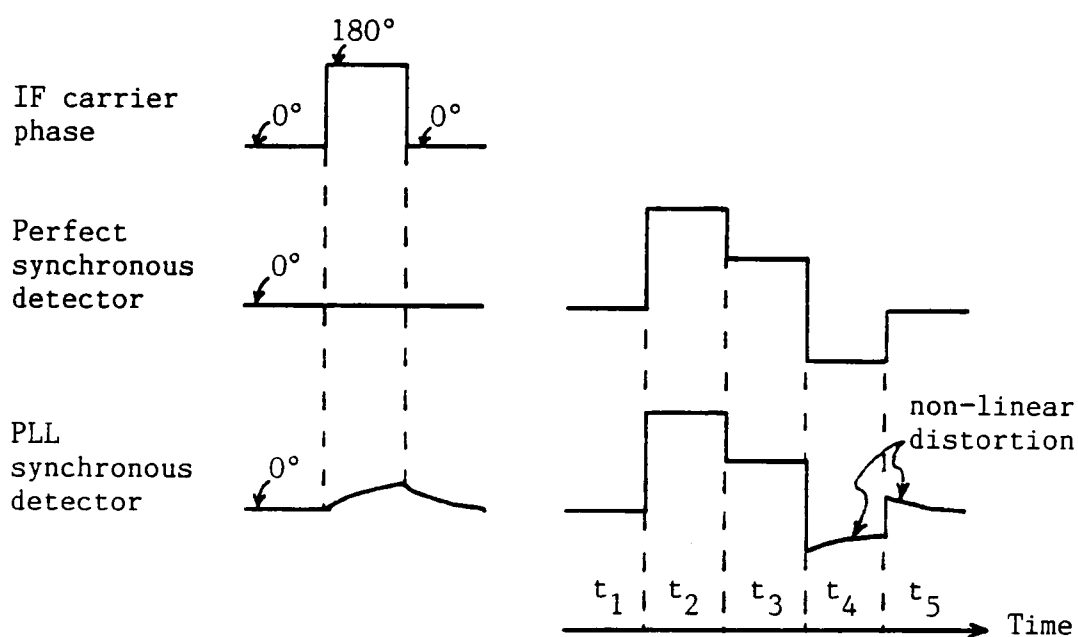


Figure 3.5. Vector representation.

Table 3.1. Composite phase ϕ .

Ghost * phase θ	Time period				
	t_1	t_2	t_3	t_4	t_5
0°	0°	0°	0°	0°	0°
90°	26°	4.8°	26°	72°	26°
180°	0°	0°	0°	180°	0°

* The power ratio of the ghost signal to the main signal is -6 dB.



(a) Generated carrier phases.

(b) Detected waveforms.

Figure 3.6. Generated carrier phases and detected waveforms.

where $m(t)$ is the variable with respect to the time, even if the ghost is stable. Assume that the power ratio of the ghost signal to the main signal is -6 dB. Then, from Equation (3-2), Table 3.1 is obtained. It shows the phase of the composite signal, ϕ , with respect to time t and the phase of the ghost signal, θ . The phase ϕ shows a complicated variation.

To simplify the discussion, assume $\theta = 180$ deg. Then the composite IF carrier has two values of phase as shown in Table 3.1. One is the normal phase (0 deg), and the other is the temporal reverse phase (180 deg). This phenomenon is often called the over-modulation caused by the ghost interference. When the ghost interference is larger than -15 dB, this phenomenon occurs [1]. Figure 3.6 shows the generated carrier phase and the detected waveforms in the case of a -6 dB, 180 deg ghost. Since the PLL tries to follow the temporal change of the IF carrier phase, the generated carrier phase varies like the time-constant curve shown in Figure 3.6 (a). Since this phase variation depends upon the signal level of the waveform, the detected waveform suffers the non-linear distortion shown in Figure 3.6 (b). This problem can be eliminated by narrowing the bandwidth of the loop filter, but there is a practical limit. The more narrow the filter is, the more difficult it is for the PLL to follow the frequency jitter which normally occurs in the VCO, the oscillator in the tuner, and the input signal.

CHAPTER IV

PROPOSED HYBRID PLL SYNCHRONOUS VIDEO DETECTOR

Overview of the Proposed Detector

The proposed PLL synchronous video detector is obtained by applying digital techniques to the conventional analog PLL. It contains digital blocks as well as conventional analog blocks, so it should be called a hybrid PLL synchronous video detector. A wide-band analog loop filter is used only at the initial step of the PLL operation to realize the wide pull-in range. An initial step, for example, is channel-change or power-on. A narrow-band digital loop filter is used at the intermediate step and the last step. The PLL stays on all the time at the intermediate step to speed up the pull-in process. Then, at the last step, it stays on and off periodically. In other words, it samples the stable phase and holds the operation during the period of fluctuated phase. A horizontal synchronization pulse can be used as the sampling signal, because it has the maximum amplitude (100 %) and suffers the least phase fluctuation caused by the ghost. By this sample and hold operation, this hybrid PLL generates a stable IF carrier with negligibly small phase drift during the hold period. It is the digital circuits that can realize the sample and hold operation without signal decay. Thus, the proposed hybrid PLL synchronous video detector solves the disadvantage of the analog PLL synchronous video detectors.

Configuration and Operation

Figure 4.1 shows the proposed hybrid PLL synchronous video detector. It consists of the conventional analog PLL synchronous video detector shown in Figure 3.1 (pp. 17) and digital signal processing blocks. The digital signal processing blocks consist of four switches (SWs), a pre-alias filter (PF), an analog to digital converter (A/D), a digital loop filter (DLF), and a digital to analog converter (D/A). To simplify the discussion, assume that the input signal $r(t)$ and the VCO output signal $c(t)$ are sine-waves.

$$r(t) = \sqrt{2} A_r \sin\{\omega_r t + \theta_r(t)\} \quad (4-1)$$

$$c(t) = \sqrt{2} A_c \sin\{\omega_c t + \theta_c(t)\} \quad (4-2)$$

where A_r and A_c are the amplitudes, ω_r and ω_c are the angular frequencies, and $\theta_r(t)$ and $\theta_c(t)$ are the phases.

At the initial step, for example channel-change or power on, the input frequency ω_r differs from the VCO frequency ω_c . Then, the lock detector (LD) detects the un-lock state, and the sequence controller (SC) connects SW3 to the hold (H) contact and SW1, SW2, and SW4 to the analog (A) contacts. Figure 4.2 (a) shows the timing chart of these SWs. Then, the conventional analog PLL becomes active and finishes the pull-in and the lock-in processes. Thus, this initial step is called the analog PLL mode. During this mode, the value zero is fed into the DLF input via SW3, and

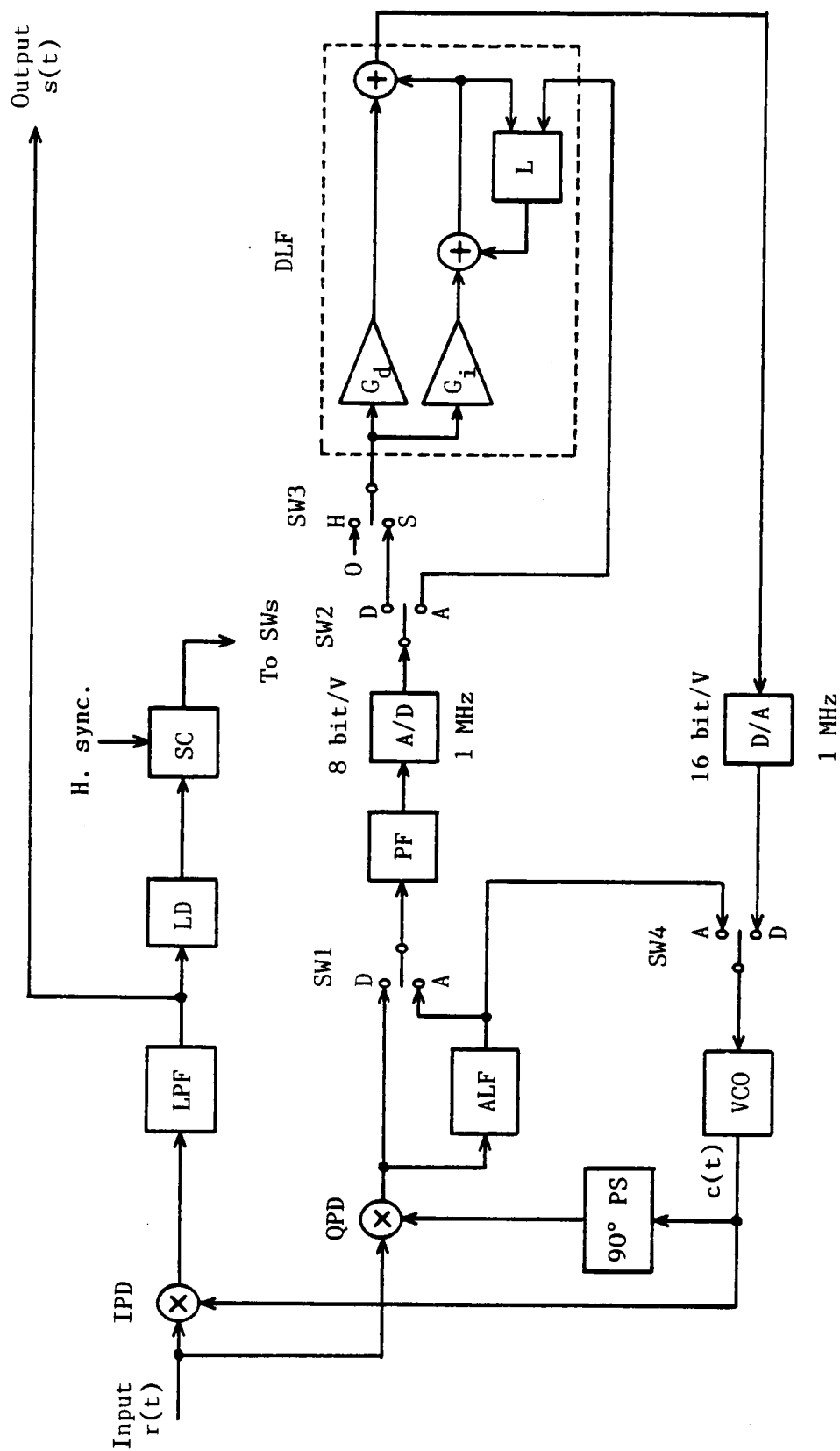
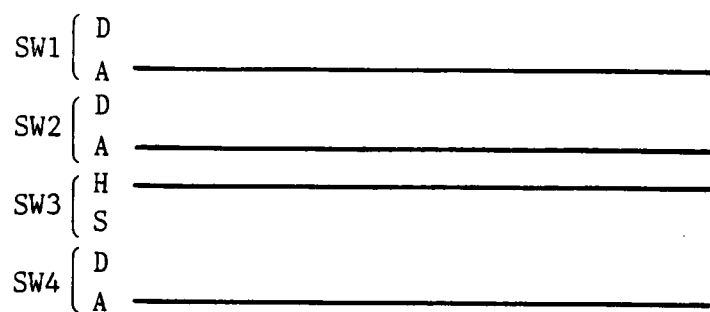
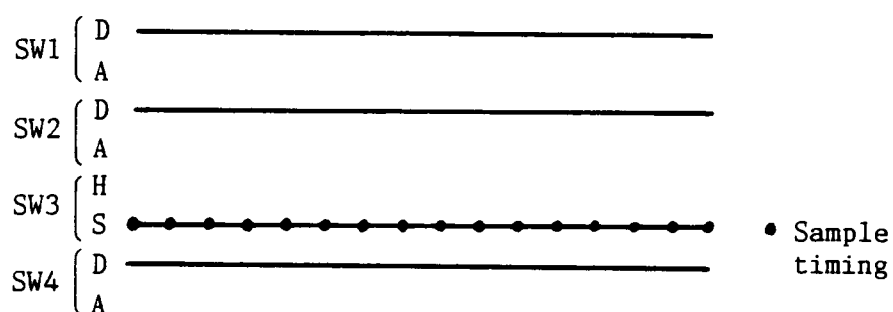


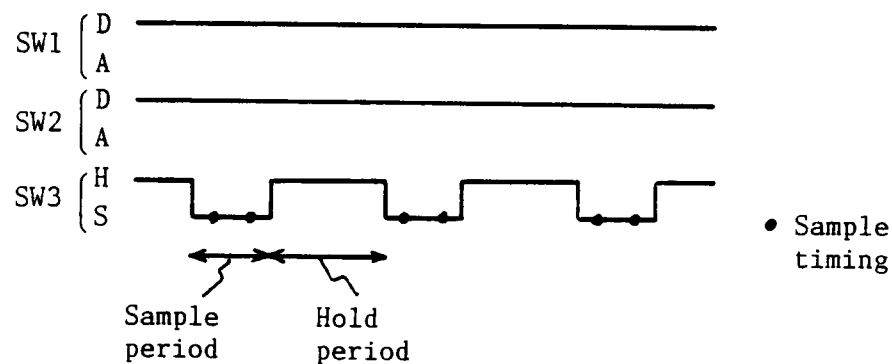
Figure 4.1. Block diagram of hybrid PLL synchronous television video detector.



(a) Analog PLL mode.



(b) Hybrid PLL continuous mode (C mode).



(c) Hybrid PLL sample and hold mode (S/H mode).

Figure 4.2. Timing chart of SWs.

the VCO input voltage is stored in the latch (L) of the DLF via SW1, the PF, the A/D, and SW2. A wide-band analog loop filter (ALP) should be used to accommodate tracking of a wide frequency range.

Then, the LD detects the lock state, and the SC connects SW3 to the sample (S) contact and SW1, SW2, and SW4 to the digital (D) contacts during some fixed time called the intermediate step. Figure 4.2 (b) shows the timing chart of these SWs in this step. The DLF is always connected to the A/D, and the hybrid PLL operates continuously. Thus, this step is called the hybrid PLL continuous mode, abbreviated to C mode. At the beginning of the C mode, the DLF output is basically the same as the ALP output because the VCO input voltage has been stored in the latch (L) of the DLF during the previous analog PLL mode. However, the constant offsets of the PF, the A/D, and the D/A cause a slight difference between the VCO input at the end of the previous mode and the VCO input at the beginning of this C mode. Thus, these voltage offsets cause frequency offset Δf_{off} . It has to be smaller than a half of the clock frequency f_{ck} so that the hybrid PLL can absorb it in the C mode. That is, the following Nyquist condition has to be satisfied.

$$\Delta f_{\text{off}} < f_{\text{ck}}/2 \quad (4-3)$$

The PF, which may be a first-order RC low-pass filter, must reject the undesirable 2ω component as well as the aliasing noise. Since

the PF affects the loop stability by its phase-lag, its cut-off frequency f_p should be chosen carefully. Anyway, f_p must be far lower than 2ω .

$$f_p \ll 2\omega \quad (4-4)$$

The DLF is called an integration type digital filter, and its transfer function $F(z)$ in z -domain is expressed as

$$F(z) = G_d + G_i/(1 - z^{-1}). \quad (4-5)$$

The first term and the second term are called the direct path and the integration path, respectively. The integration path contains the latch (L). It is shown in CHAPTER V that $F(z)$ is obtained from applying bilinear transformation to a conventional narrow-band analog loop filter.

After the C mode, the SC begins to connect SW3 to the sample (S) contact in the horizontal synchronization (H. Sync.) period and to the hold (H) contact in the remainder of the video signal period. Other SWs remain as they were. That is, they are connected to the D contacts. Figure 4.2 (c) shows the timing chart of these SWs. This is the last step called the hybrid PLL sample and hold mode, abbreviated to S/H mode. The value zero is fed into the DLF during the hold period so that the DLF can hold its output. Though the DLF must have enough bits to avoid quantization error, it can be easily integrated into one integrated circuit (IC) because of its simplicity and relatively

low speed (1 MHz). The D/A resolution (16 bit/V, 1 MHz) is much finer than the A/D resolution (8 bit/V, 1 MHz) because the quantization error of the D/A directly causes the phase drift in the hold period. The A/D resolution, the D/A resolution, and the phase drift are analyzed in CHAPTER V. The hybrid PLL in the S/H mode is designed to have the capability of following the phase change and the slight frequency change which may occur in normal circumstances.

CHAPTER V

LINEAR ANALYSIS OF PROPOSED PLL

Linear Models

The proposed hybrid PLL is the heart of the proposed video detector. Only the linear model of the proposed hybrid PLL is analyzed here, since other parts of the detector have been widely studied and can be designed by conventional methods [4], [5]. Since the hybrid PLL is based on a narrow-band analog PLL, both the hybrid and analog analyses will be shown for the purposes of comparison and design.

Linear Model of Original Analog PLL. The linear model of the original analog PLL is introduced in CHAPTER II. Figure 2.2 (pp. 8) shows its linear model. The following set of parameters can be considered typical of narrow-band analog PLLs.

The loop gain K is

$$K = 1.0 \times 10^7 \quad 1/s. \quad (5-1)$$

The narrow-band loop filter is an active type, and its transfer function $F(s)$ is given by the following equations.

$$F(s) = (1 + \tau_2 s) / (\tau_1 s) \quad (2-9)$$

$$\tau_1 = 9.9 \times 10^{-3} \quad s \quad (5-2)$$

$$\tau_2 = 1.0 \times 10^{-4} \quad s \quad (5-3)$$

The VCO gain K_0 is calculated from reference [4].

$$K_0 = 2.1 \times 10^7 \quad \text{rad/s/V} \quad (5-4)$$

By substituting Equations (5-1) and (5-4) into (2-15), the phase detector gain K_d is given by

$$K_d = 1/2.1 \approx 0.476 \quad \text{V/rad.} \quad (5-5)$$

Figure 5.1 shows the Bode plot of the open-loop transfer function $|T(j\omega)|$ obtained from substituting Equations (5-1), (2-9), (5-2), and (5-3) into (2-13) and setting $s = j\omega$.

The natural frequency ω_n and damping factor ζ are obtained from Equations (2-17) and (2-18), respectively.

$$\omega_n = 31.8 \quad \text{krad/s} \quad (5-6)$$

$$\zeta = 1.59 \quad (5-7)$$

The lock range $\Delta\omega_L$ and the lock-in time T_L are obtained from Equations (2-27) and (2-28), respectively.

$$\Delta\omega_L \approx 101 \quad \text{krad/s} \quad (5-8)$$

$$T_L \approx 31.4 \quad \mu\text{s}$$

Since the loop filter is the active type, the hold range $\Delta\omega_h$ and the pull-in range $\Delta\omega_p$ are theoretically infinite as shown by Equations (2-25) and (2-29), respectively.

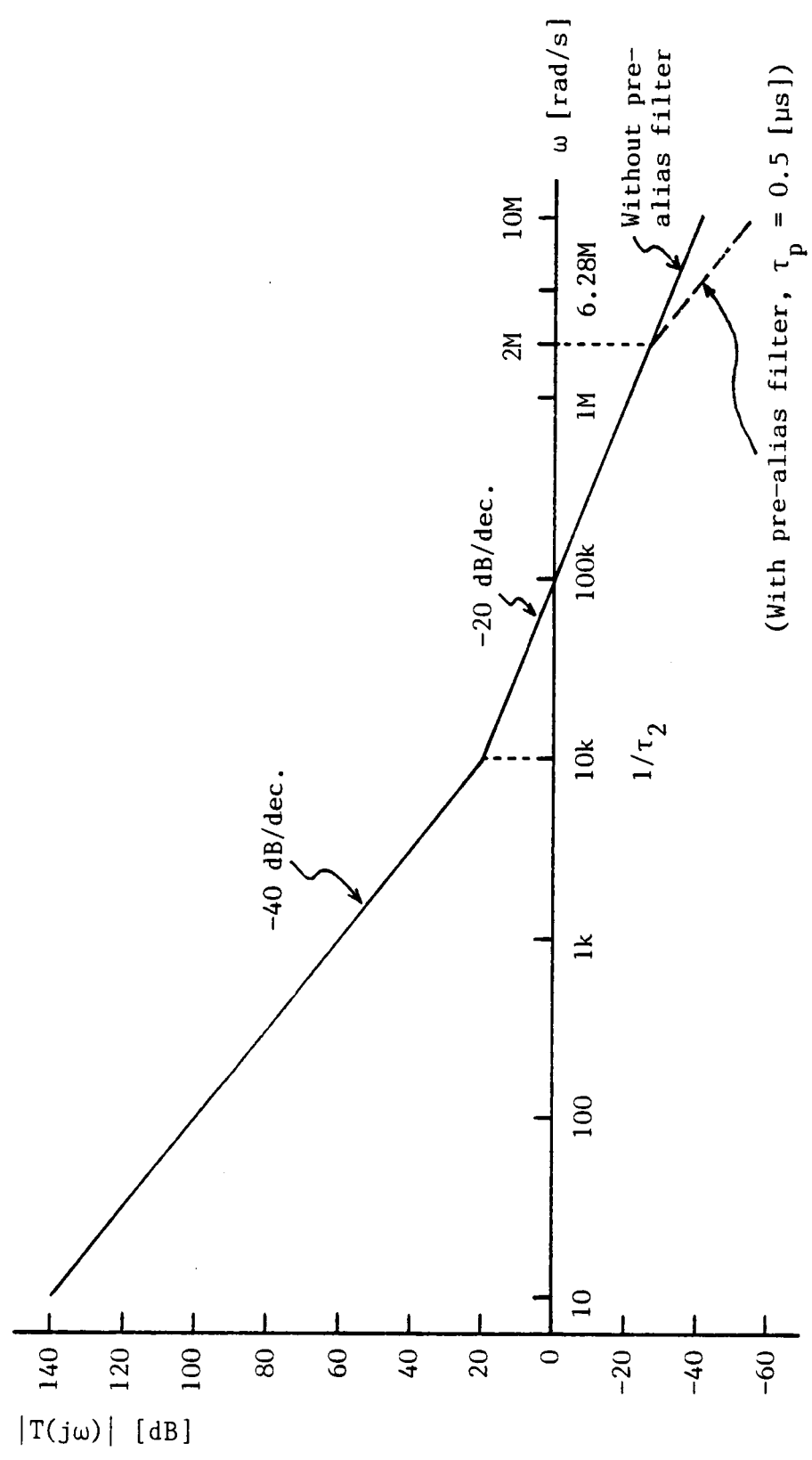


Figure 5.1. Bode plot of open-loop transfer function of original analog PLL.

Linear Model of Hybrid PLL. Figure 5.2 shows the linear model of the proposed hybrid PLL. The phase detector (PD) and the VCO are the same as those of the original analog PLL shown in Figure 2.2 (pp. 8).

The pre-alias filter (PF) is a first-order RC low-pass filter, and its transfer function $P(s)$ in Laplace transform is expressed as

$$P(s) = 1/(1 + \tau_p s) \quad (5-9)$$

$$\tau_p = 0.5 \times 10^{-6} \text{ s.} \quad (5-10)$$

It is clear from Figure 5.1 that τ_p must be smaller than 10^{-5} s to avoid closed-loop instability. Additional discussion about the τ_p is given later.

The clock is indispensable for all digital blocks including the A/D, the digital loop filter (DLF), the delay, and the D/A. Its frequency f_{ck} is given by

$$f_{ck} = 1/T = 1.0 \text{ MHz} \quad (5-11)$$

where T is the clock period. According to the resolution analysis given later, the A/D and the D/A need 8-bit/V and 16-bit/V resolution, respectively. A clock frequency of 1 MHz is adequate for the A/D and can also be considered suitable for the 16-bit/V D/A. From Equation (4-3), the following condition is obtained.

$$\Delta f_{off} < 0.5 \text{ MHz} \quad (5-12)$$

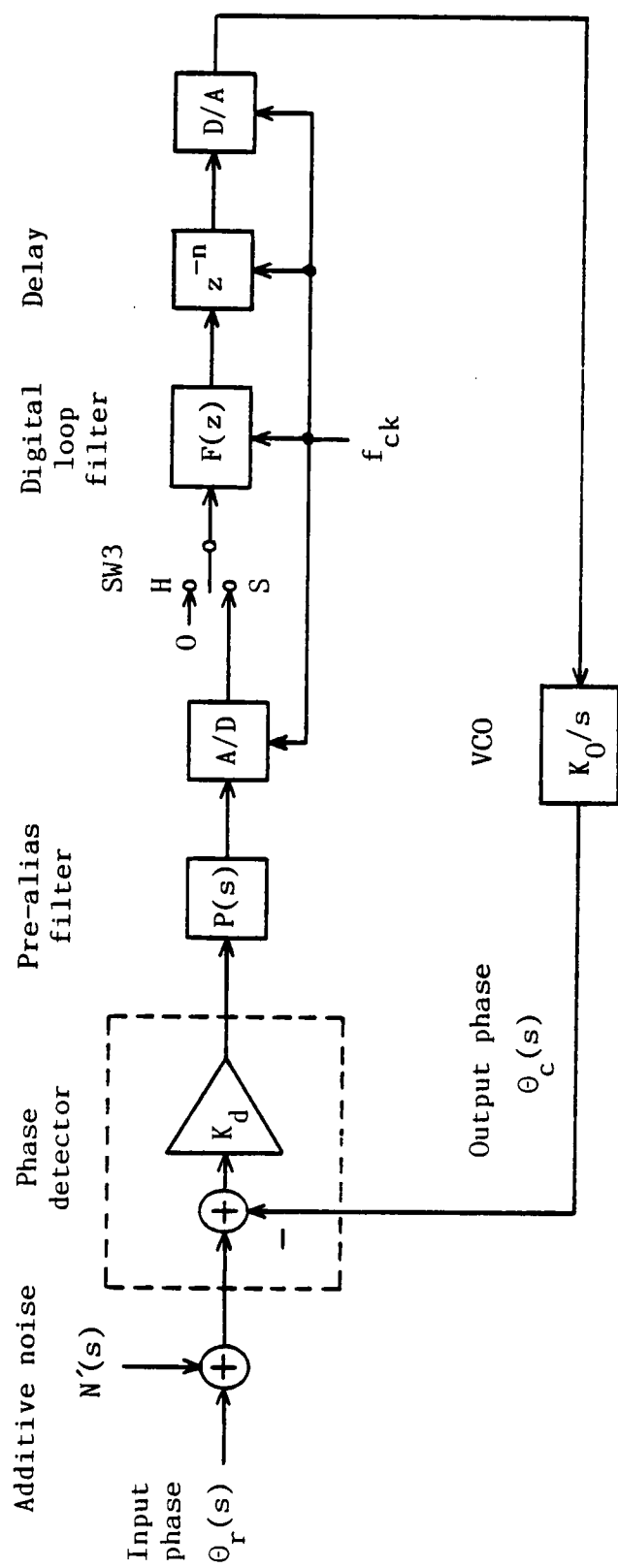


Figure 5.2. Linear model of hybrid PLL.

where Δf_{off} is the frequency offset caused by a constant offset in the digital blocks. Thus, the following condition, which the constant offset must satisfy, is obtained from Equations (5-4) and (5-12).

$$\text{The constant offset} < 2\pi\Delta f_{\text{off}}/K_0 = 0.150 \quad \text{V} \quad (5-13)$$

This condition is easy to realize in practice.

The cut-off frequency of the original analog closed-loop transfer function given by Equation (2-16) is located near the natural frequency ω_n (≈ 5 kHz) given by Equation (5-6) [6], and it is much lower than the clock frequency of 1 MHz. Thus, by applying a bilinear transformation

$$s = \frac{2}{T} \frac{z - 1}{z + 1} \quad (5-14)$$

to Equation (2-9), the following transfer function of the DLF, $F(z)$, is obtained.

$$F(z) = K_f(z - z_0)/(z - 1) \quad (5-15)$$

$$= G_d + G_i z/(z - 1) \quad (5-16)$$

where

$$K_f = (2\tau_2 + T)/(2\tau_1) = 0.010151515 \quad (5-17)$$

$$z_0 = \frac{(2/T)\tau_2 - 1}{(2/T)\tau_2 + 1} = 0.990049751 \quad (5-18)$$

$$G_d = K_f z_0 = 0.010050504 \quad (5-19)$$

$$G_i = K_f(1 - z_0) = 1.01010102 \times 10^{-4} \quad (5-20)$$

The delay z^{-n} represents the total delay required by the digital blocks. Since each digital component (the A/D, the multiplier in the DLF, the adder in the integration path of the DLF, the adder at the output of the DLF, and the D/A) needs one clock,

$$n = 5. \quad (5-21)$$

Figure 5.3 shows the actual horizontal television signal [2], the sample period, and the hold period. The horizontal blanking period (10 μ s) is chosen as the sample period (t_s), because the sample period must be longer than the loop delay (5 μ s). It consists of the front porch, the back porch, and the horizontal sync. pulse period. The modulated amplitude of the each porch and that of the sync. pulse are 75 % and 100 %, respectively. The larger amplitude suffers less phase fluctuation caused by the ghost interference. Thus, if the delay could be reduced to less than the horizontal sync. period (5 μ s), for example, 2 μ s, the horizontal sync. pulse period would be chosen as the sample period rather than the horizontal blanking period. The exact hold period should be the remainder, that is, the active horizontal period (53.5 μ s), but the value 50 μ s is chosen as the hold period (t_h)

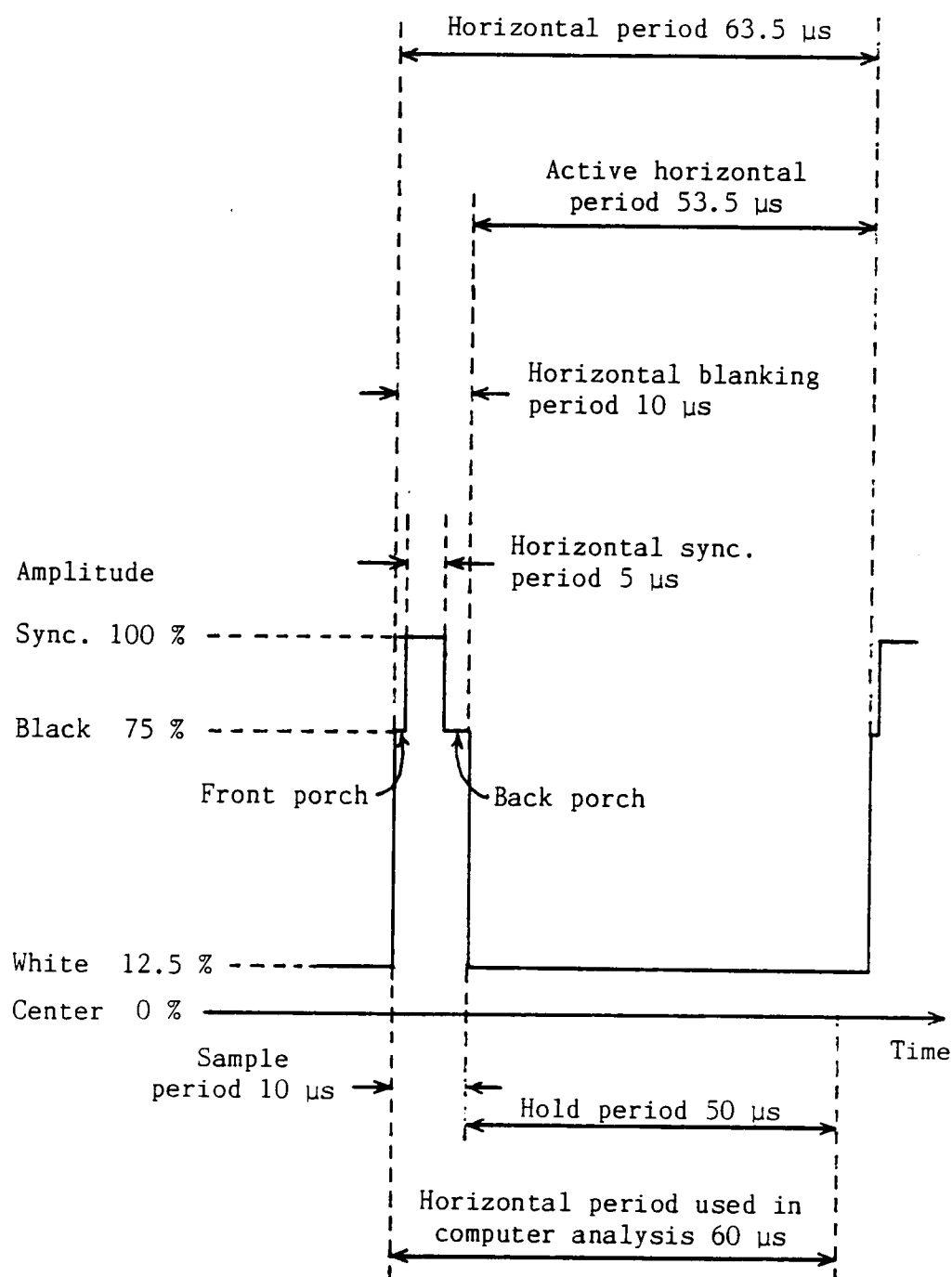


Figure 5.3. Actual television horizontal signal, sample period, and hold period.

in order to simplify the computer analysis. Therefore, the horizontal period used in the computer analysis is the addition of the sample period ($t_s = 10 \mu s$) to the hold period ($t_h = 50 \mu s$), that is, $60 \mu s$.

Stability Analysis

The stability of the hybrid PLL in the C mode is analyzed by the model shown in Figure 5.4. The A/D is represented by an ideal sampler with clock period T s. Let $u(t)$ be the input signal of the ideal sampler, then according to reference [9], its output signal in Laplace transform, $U^*(s)$, is defined by

$$U^*(s) = \sum_{k=0}^{\infty} u(kT) \exp(-kTs). \quad (5-22)$$

Using $U^*(s)$, the input signal $U(s)$ and the output of the PLL, $\Theta_c(s)$, are given by

$$U(s) = G_1(s) \{ \Theta_r(s) - G_3(z) G_2(s) U^*(s) \} \quad (5-23)$$

$$\Theta_c(s) = G_3(z) G_2(s) U^*(s) \quad (5-24)$$

where

$$G_1(s) = K_d P(s) \quad (5-25)$$

$$G_3(z) = F(z) z^{-n} \quad (5-26)$$

$$G_2(s) = \frac{1 - \exp(-Ts)}{s} \frac{K_0}{s}. \quad (5-27)$$

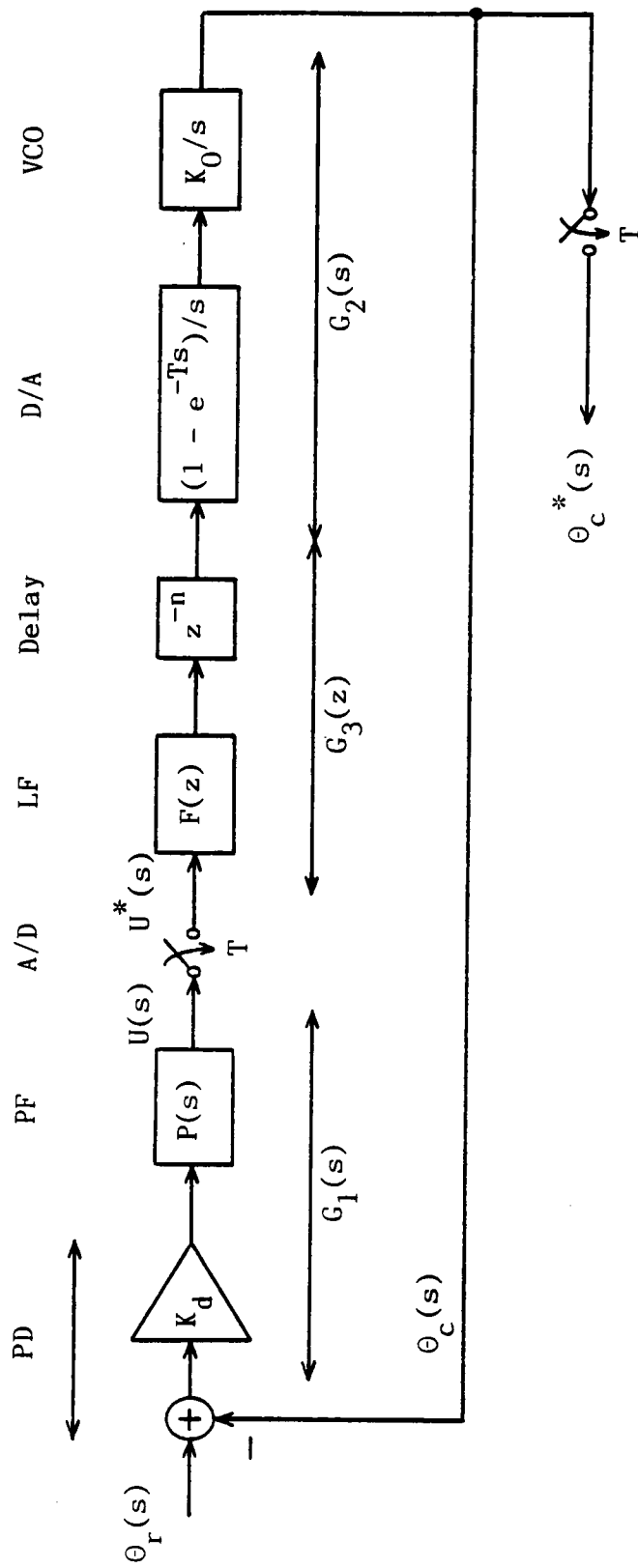


Figure 5.4. Hybrid PLL model for stability analysis.

The first factor of $G_2(s)$ represents the D/A realized by a zero-order hold. From Equations (5-23) and (5-24), it can be shown that

$$\theta_c^*(s) = \frac{G_2^*(s)G_3(z)\overline{G_1\theta_r}^*(s)}{1 + \overline{G_1G_2}^*(s)G_3(z)} \quad (5-28)$$

This is the same as

$$\theta_c(z) = \frac{G_2(z)G_3(z)\overline{G_1\theta_r}(z)}{1 + \overline{G_1G_2}(z)G_3(z)} \quad (5-29)$$

Thus, the open-loop transfer function $T(z)$ is expressed as

$$T(z) = \overline{G_1G_2}(z)G_3(z) \quad (5-30)$$

where $\overline{G_1G_2}(z)$ is obtained from applying z -transformation to $G_1(s)G_2(s)$, and $G_3(z)$ is obtained from substituting Equation (5-15) into (5-26). That is,

$$T(z) = KK_p K_f \frac{(z - b_p)(z - z_0)}{z^n(z - a_p)(z - 1)^2} \quad (5-31)$$

where

$$a_p = \exp(-T/\tau_p) \quad (5-32)$$

$$K_p = T + \tau_p(a_p - 1) \quad (5-33)$$

$$b_p = \{a_p T + \tau_p(a_p - 1)\}/K_p. \quad (5-34)$$

Parameters K , K_f , and z_0 are given by Equations (2-15), (2-17), and (5-18), respectively.

Figure 5.1 (pp. 35) shows the absolute value of the open-loop transfer function of the original analog PLL. Open-loop gain is 0 dB at $\omega = 100$ krad/s. Since this frequency is much lower than the clock frequency ($2\pi/T \approx 6.28$ Mrad/s), the stability of the hybrid PLL can be analyzed by applying bilinear transformation to the open-loop transfer function $T(z)$ given by Equation (5-31). Thus, by applying the bilinear transformation

$$z = \frac{1 + (T/2)w}{1 - (T/2)w} \quad (5-35)$$

to Equation (5-31), the following open-loop transfer function in w -domain is obtained.

$$T_w(w) = K \frac{(1 + \tau_2 w)(1 - (T/2)w)^{(n+1)}(1 + b'(T/2)w)}{\tau_1 w^2 (1 + (T/2)w)^n (1 + a'(T/2)w)} \quad (5-36)$$

where

$$a' = (1 + a_p)/(1 - a_p) \quad (5-37)$$

$$b' = (1 + b_p)/(1 - b_p). \quad (5-38)$$

Let $w = j\omega$ in Equation (5-36), then the following equations giving the amplitude and the phase of the transfer function are obtained.

$$|T_w(j\omega)|^2 = K^2 \frac{(1 + (\tau_2\omega)^2)(1 + (T\omega/2)^2)(1 + (b'T\omega/2)^2)}{\tau_1^2\omega^4(1 + (a'T\omega/2)^2)} \quad (5-39)$$

$$\begin{aligned} \arg(T_w(j\omega)) = & -\pi - (2n + 1)\arctan(T\omega/2) + \arctan(\tau_2\omega) \\ & + \arctan(b'T\omega/2) - \arctan(a'T\omega/2) \end{aligned} \quad (5-40)$$

In Equation (5-40), the second term represents the phase lag caused by the loop delay, and the third represents the phase lead by the loop filter, and the forth and the last represent the effect of the pre-alias filter. The phase margin is obtained from adding π to Equation (5-40).

By using the parameters introduced in this chapter, that is, $K = 1.0 \times 10^7$ 1/s, $\tau_1 = 9.9 \times 10^{-3}$ s, and $\tau_2 = 1.0 \times 10^{-4}$ s, the following results are obtained. Table 5.1 shows the phase margin calculated from Equation (5-40). The gain margin and the overshoot of the step response are obtained from computer analysis and shown in Table 5.2 and 5.3, respectively. The results from the original analog PLL are also shown in Table 5.4 for comparison. From these results, it follows that:

- (1) The loop delay affects the stability more than the time constant of the pre-alias filter (PF).
- (2) The increase of the overshoot caused by the PF is not negligible in the case of a practical delay of 5 μ s.
- (3) The original analog PLL must be very stable in order to design the hybrid PLL.

Table 5.1. Phase margin of hybrid PLL.

Time constant of PF τ_p [μ s]	Delay [μ s]		
	0	3	5
$1/(2\pi)$	80.5°	63.4°	51.9°
0.5	78.6	61.4	50.0
1.0	75.7	58.6	47.1

Table 5.2. Gain margin of hybrid PLL.

Time constant of PF τ_p [μ s]	Delay [μ s]		
	0	3	5
$1/(2\pi)$	-29.2 dB	-12.5 dB	-9.6 dB
0.5	-29.1	-11.9	-8.1
1.0	-27.4	-11.3	-7.6

Table 5.3. Overshoot of hybrid PLL.

Time constant of PF τ_p [μ s]	Delay [μ s]		
	0	3	5
$1/(2\pi)$	7 %	9 %	20 %
0.5	7	9	23
1.0	7	11	28

Table 5.4. Stability of original analog PLL.

Phase margin	Gain margin	Overshoot
84.3°	∞ dB	7 %

Therefore, the suitable time constant of the PF, τ_p , is $1/(2\pi) \mu s$ or $0.5 \mu s$. Further analysis proves $0.5 \mu s$ to be suitable. Figure 5.5 shows the Nyquist plots of the original analog PLL and the hybrid PLL with a delay of $5 \mu s$ and $\tau_p = 0.5 \mu s$.

Output Phase Jitter

One of the most important characteristics of the hybrid PLL is the existence of output phase jitter. Suitable values of parameters such as the resolution of the A/D, the resolution of the D/A, and the time constant of the PF are chosen through this analysis for the C mode. In addition, further analysis is done to prove that these values are suitable for the S/H mode.

Effect of A/D Quantization Noise. The resolution of the A/D, in other words, the word length of the A/D, is chosen so that the output phase jitter caused by its quantization noise will stay within the practical limit.

First, discrete analysis is used. It uses the discrete model and z-transformation. Then, continuous analysis is used. It uses the continuous model and Laplace transformation.

Figure 5.6 shows the discrete model. The pre-alias filter and the loop delay are omitted to simplify the analysis. The input phase is assumed to be zero. The quantization noise in Laplace transform is designated $N_q(s)$. Then, the input of the A/D, $U(s)$, and the output of the PLL, $\theta_c(s)$, are expressed as

$$U(s) = N_q(s) - K_d F(z) G_2(s) U^*(s) \quad (5-41)$$

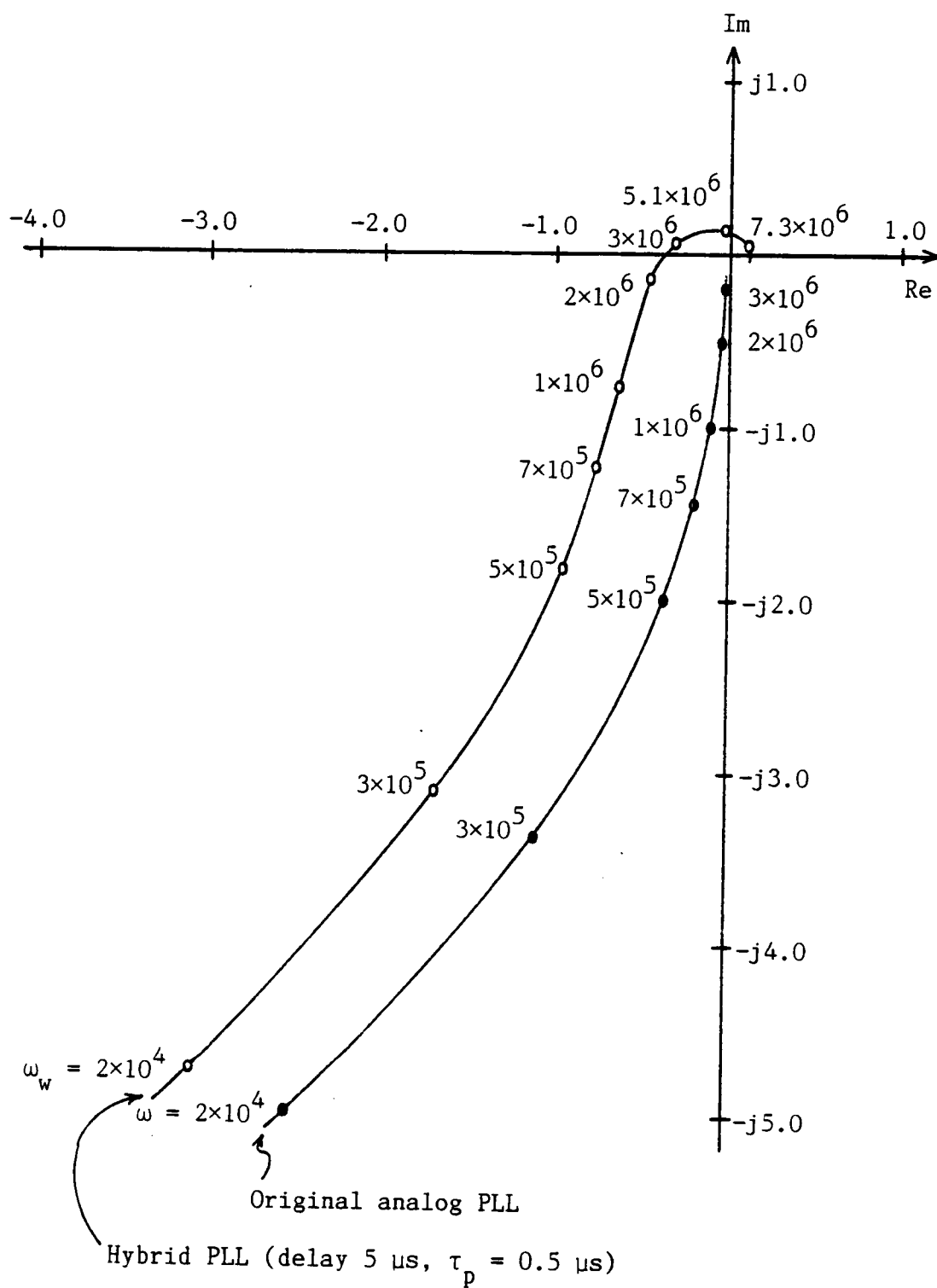


Figure 5.5. Nyquist plots of open-loop transfer functions.

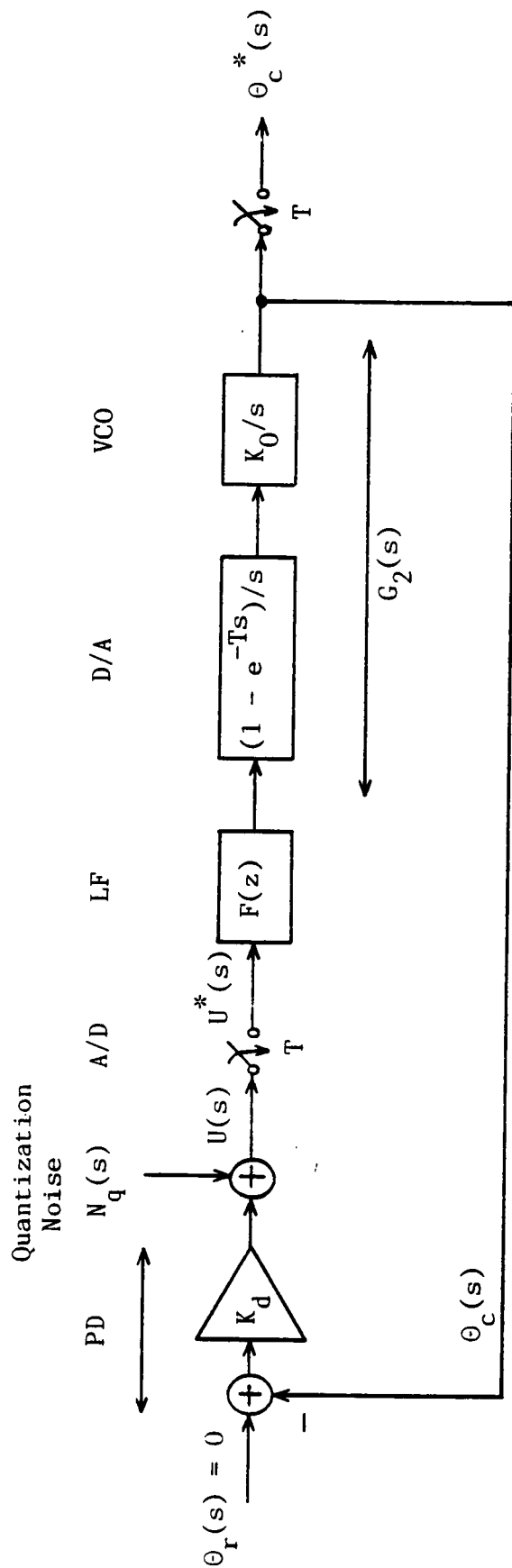


Figure 5.6. Discrete model to analyze the output phase jitter caused by the A/D quantization noise.

$$\Theta_c(s) = F(z)G_2(s)U^*(s) \quad (5-42)$$

where $F(z)$, $G_2(s)$, and $U^*(s)$ are given by Equations (5-15), (5-27), and (5-22), respectively. From Equations (5-41) and (5-42), it can be shown that

$$H_q(z) \equiv \frac{\Theta_c(z)}{N_q(z)} = \frac{F(z)G_2(z)}{1 + K_d F(z)G_2(z)} \quad (5-43)$$

where $G_2(z)$ is obtained from applying z -transformation to $G_2(s)$.

Thus,

$$H_q(z) = K_0 K_f T \frac{z - z_0}{(z - \alpha)(z - \beta)} \quad (5-44)$$

where K_f and z_0 are given by Equations (5-17) and (5-18), respectively, and

$$\alpha + \beta = 2 - K K_f T \quad (5-45)$$

$$\alpha\beta = 1 - K K_f T z_0. \quad (5-46)$$

Since the condition

$$T = 10^{-6} \ll 10^{-4} = \tau_2 \quad (5-47)$$

is satisfied, Equations (5-45) and (5-46) are approximated to

$$\alpha + \beta \approx 2 - \varepsilon \quad (5-48)$$

$$\alpha\beta \approx 1 - \varepsilon \quad (5-49)$$

where

$$\varepsilon \equiv KT\tau_2/\tau_1. \quad (5-50)$$

Thus,

$$\alpha \approx 1 \quad (5-51)$$

$$\beta \approx 1 - \varepsilon. \quad (5-52)$$

On the other hand, the variance of output phase jitter, $\sigma_{\theta c}^2$, is calculated from the following integration [9].

$$\sigma_{\theta c}^2 = \frac{T}{2\pi} \int_{-\pi/T}^{\pi/T} S_q(\exp(j\omega T)) |H_q(\exp(j\omega T))|^2 d\omega \quad \text{rad}^2 \quad (5-53)$$

where $S_q(\exp(j\omega T))$ designates the power spectrum of the quantization noise. This is the constant given by

$$S_q(\exp(j\omega T)) = 2^{-2k}/(12) \quad \text{V}^2/\text{Hz} \quad (5-54)$$

where k designates the word length of the A/D per Volt. From substituting Equation (5-54) into (5-53) and using a new variable Ω expressed as

$$\Omega = \omega T, \quad (5-55)$$

the following equations are obtained.

$$\sigma_{\theta c}^2 = \frac{2^{-2k}}{12} \frac{T}{2\pi} \int_{-\pi}^{\pi} |H_q(j\Omega)|^2 d\Omega \quad (5-56)$$

$$|H_q(j\Omega)|^2 = C\{A/(1 - v\cos\Omega) + B/(1 - w\cos\Omega)\} \quad (5-57)$$

where

$$C = (K_0 K_f T)^2 \quad (5-58)$$

$$A = (v - u)/(v - w) \quad (5-59)$$

$$B = (w - u)/(w - v) \quad (5-60)$$

$$u = 2z_0/(1 + z_0^2) \quad (5-61)$$

$$v = 2\alpha/(1 + \alpha^2) \quad (5-62)$$

$$w = 2\beta/(1 + \beta^2). \quad (5-63)$$

From substituting Equation (5-57) into (5-56) and using the following integration from reference [10],

$$\int_{-\pi}^{\pi} 1/(1 - v\cos\Omega) d\Omega = 2\pi/(1 - v^2)^{\frac{1}{2}}, \quad (5-64)$$

$$\sigma_{\theta c}^2 = 2^{-2k}/(12) \times (K_0 K_f T)^2 \times D/E \quad (5-65)$$

$$D = (1 + \alpha\beta)z_0^2 - 2(\alpha + \beta)z_0 + 1 + \alpha\beta \quad (5-66)$$

$$E = (1 - \alpha\beta)(1 - \alpha^2)(1 - \beta^2) \quad (5-67)$$

are obtained. In addition, from using Equation (5-47),

$$D/E \approx 2z_0/\{(1 - \alpha\beta)(1 + \alpha + \beta + \alpha\beta)\} \quad (5-68)$$

is obtained. Finally, from Equations (5-48), (5-49), and (5-68), the following output phase jitter $\sigma_{\theta_c}^2$ is obtained.

$$\sigma_{\theta_c}^2 \approx 2^{-2k}/(12) \times (K_0 K_f T)^2 \times 1/(2\epsilon) \quad (5-69)$$

$$\approx \frac{2^{-2k}}{12} \frac{1}{2} \frac{K_0}{K_d} \frac{\tau_2}{\tau_1} T \quad \text{rad}^2 \quad (5-70)$$

Equation (5-70) is the final result obtained by discrete analysis. Since this analysis is based on the discrete model, it requires complicated calculation. The following continuous analysis, based on the continuous model, gives the same result and requires less calculation than the discrete analysis.

Figure 5.7 shows the continuous model for analyzing output phase jitter caused by A/D quantization noise. Compared to the discrete model shown in Figure 5.6 (pp. 50), this model includes the pre-alias filter (PF). The quantization noise $N_q(s)$ is added at the output of the PF. Its power is $2^{-2k}/(12) V^2$, and its power spectrum $S_q(j2\pi f) V^2/\text{Hz}$ is constant between $-1/(2T)$ and $1/(2T)$.

$$S_q(j2\pi f) = \frac{2^{-2k}}{12} T \quad \text{for } -1/(2T) \leq f \leq 1/(2T) \quad (5-71)$$

$$= 0 \quad \text{otherwise} \quad (5-72)$$

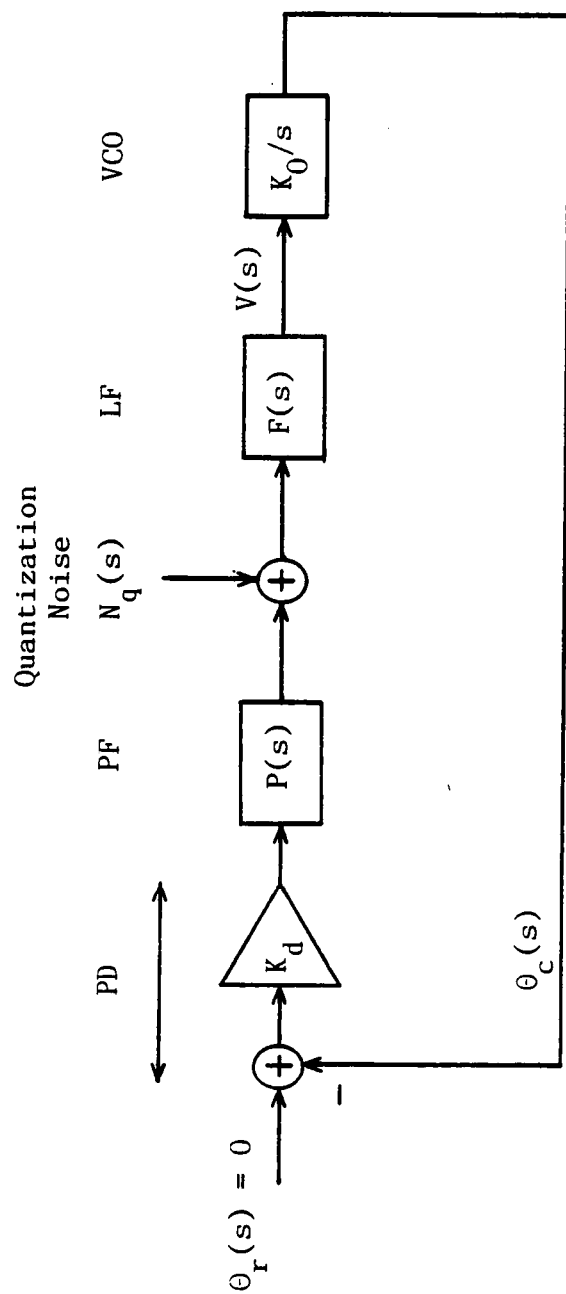


Figure 5.7. Continuous model to analyze the output phase jitter caused by the A/D quantization noise.

The transfer function $H_q(s)$ from the quantization noise $N_q(s)$ to the output phase $\Theta_c(s)$ is given by

$$H_q(s) \equiv \frac{\Theta_c(s)}{N_q(s)} = \frac{K_0 F(s)/s}{1 + K_d K_0 P(s) F(s)/s} \quad (5-73)$$

From substituting Equations (2-9) and (5-9) into (5-73), it follows that

$$H_q(s) = \frac{K_0(1 + \tau_2 s)(1 + \tau_p s)}{\tau_1 s^2(1 + \tau_p s) + K_0 K_d(1 + \tau_2 s)} \quad (5-74)$$

If $\tau_p = 0$, then

$$H_q(s) = \frac{1}{K_d} \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (5-75)$$

The second factor is the same as given by Equation (2-16). The natural frequency ω_n and the damping factor ζ are given by Equations (2-17) and (2-18), respectively. Since $1/\tau_2$ and ω_n are much smaller than $1/\tau_p$, Equation (5-74) can be approximated to (5-75) from zero to $1/\tau_p$ rad/s. Figure 5.8 shows the Bode plot of $|H_q(j\omega)|$ given by Equation (5-74). It can be approximated to a first order low-pass filter with cut-off frequency ω_n ($= 31.8$ krad/s). In addition, the effect of the PF is negligible because $1/\tau_p$ is much higher than ω_n . Thus, the approximated transfer function given by Equation (5-75) can be used for further analysis.

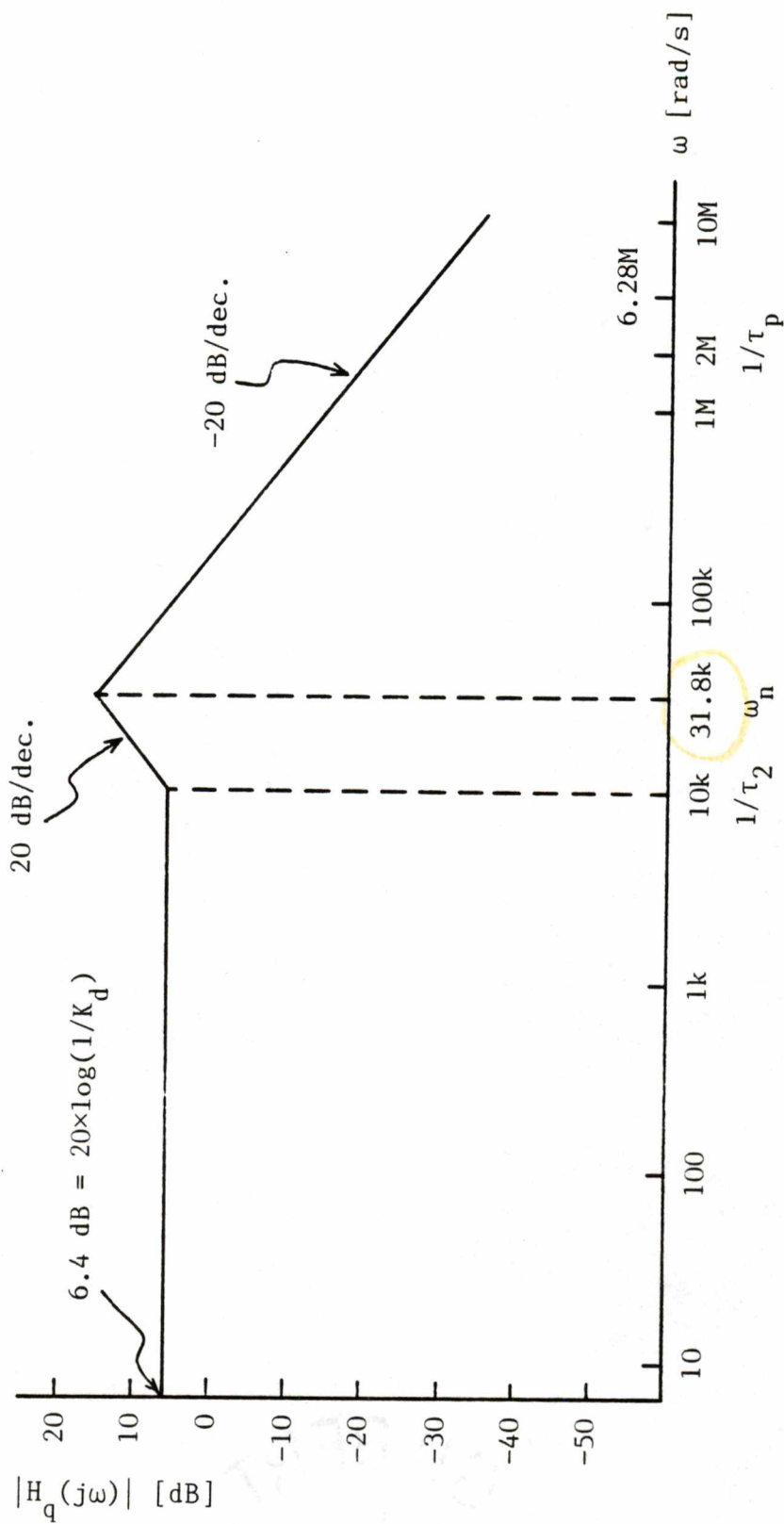


Figure 5.8. Bode plot of the transfer function $H_q(j\omega)$ from the A/D quantization noise to the output phase.

In order to generalize further calculations, Equation (5-75) can be expressed as

$$H_q(s) = \delta \frac{s + \gamma}{(s + \alpha)(s + \beta)} \quad (5-76)$$

where

$$\delta = 2\zeta\omega_n/K_d \quad (5-77)$$

$$\gamma = \omega_n/(2\zeta) \quad (5-78)$$

$$\alpha + \beta = 2\zeta\omega_n \quad (5-79)$$

$$\alpha\beta = \omega_n^2. \quad (5-80)$$

The variance of the output phase jitter, $\sigma_{\theta c}^2$, is calculated by the following integration.

$$\sigma_{\theta c}^2 = \int_{-\infty}^{\infty} S_q(j2\pi f) |H_q(j2\pi f)|^2 df \quad \text{rad}^2 \quad (5-81)$$

where $S_q(j2\pi f)$ designates the power spectrum of the quantization noise given by Equations (5-71) and (5-72). Then,

$$\sigma_{\theta c}^2 = \frac{2^{-2k_T}}{12} \int_{-1/(2T)}^{1/(2T)} |H_q(j2\pi f)|^2 df \quad (5-82)$$

is obtained. If the frequency is higher than $1/(2T)$ ($= 0.5$ MHz), the transfer function $H_q(j2\pi f)$ can be approximated to zero. Thus, Equation (5-82) can be approximated to

$$\sigma_{\theta c}^2 \approx \frac{2^{-2k_T}}{12} \int_{-\infty}^{\infty} |H_q(j2\pi f)|^2 df. \quad (5-83)$$

On the other hand, from Equation (5-76),

$$|H_q(j\omega)|^2 = A/(\omega^2 + \alpha^2) + B/(\omega^2 + \beta^2) \quad (5-84)$$

where

$$A = \delta^2(\gamma^2 - \alpha^2)/(\beta^2 - \alpha^2) \quad (5-85)$$

$$B = \delta^2(\gamma^2 - \beta^2)/(\alpha^2 - \beta^2) \quad (5-86)$$

are obtained. From using Equations (5-83) through (5-86) and the following formula [10],

$$\int_0^{\infty} 1/(\omega^2 + \alpha^2) d\omega = \pi/(2\alpha), \quad (5-87)$$

the following integration is obtained.

$$\int_0^{\infty} |H_q(j\omega)|^2 d\omega/(2\pi) = \frac{\delta^2(\alpha\beta + \gamma^2)}{4\alpha\beta(\alpha + \beta)} \quad (5-88)$$

Finally, from substituting Equation (5-88) into (5-83) and using Equations (5-77) through (5-80),

$$\sigma_{\theta c}^2 \approx \frac{2^{-2k} T}{12} \frac{\zeta \omega_n}{K_d^2} \{1 + 1/(4\zeta^2)\} \quad (5-89)$$

is obtained. In addition, Equation (5-7) shows $\zeta = 1.59$, so

$$1 \gg 1/(4\zeta^2) = 0.0989. \quad (5-90)$$

Thus, Equation (5-89) can be approximated further, and

$$\sigma_{\theta c}^2 \approx \frac{2^{-2k} T}{12} \frac{\zeta \omega_n}{K_d^2} \quad (5-91)$$

$$= \frac{2^{-2k}}{12} \frac{1}{2} \frac{K_0}{K_d} \frac{\tau_2}{\tau_1} T \quad \text{rad}^2 \quad (5-92)$$

is obtained. This equation is the same as given by Equation (5-70). From substituting $K_0 = 2.1 \times 10^7$ rad/s/V, $K_d = 0.476$ V/rad, $\tau_1 = 9.9 \times 10^{-3}$ s, $\tau_2 = 1.0 \times 10^{-4}$ s, and $T = 1$ μ s into Equation (5-92),

$$\sigma_{\theta c}^2 \approx 2^{-2k} \times 1.86 \times 10^{-2} \quad \text{rad}^2 \quad (5-93)$$

is obtained. Since the digital loop filter uses a high clock frequency, its transfer function can be obtained from applying bilinear transformation to the original analog loop filter transfer function. Thus, simple continuous analysis yields the same approximate result as obtained from the discrete analysis. Therefore, the continuous analysis is often used rather than the discrete analysis hereafter.

Effect of D/A Quantization Noise. The resolution of the D/A, which is determined by the word length of the D/A, is chosen so that the output phase jitter caused by its quantization noise will stay within a practical limit.

Figure 5.9 shows the continuous model. The loop delay is omitted to simplify analysis. The input phase is assumed to be zero. The quantization noise $N_q(s)$ is added at the output of the LF, with a power of $2^{-2m}/(12) V^2$, where m designates the word length of the D/A per Volt. The power spectrum $S_q(j2\pi f) V^2/Hz$ is constant between $-1/(2T)$ and $1/(2T)$. Thus,

$$S_q(j2\pi f) = \frac{2^{-2m}}{12} T \quad \text{for } -1/(2T) \leq f \leq 1/(2T) \quad (5-94)$$

$$= 0 \quad \text{otherwise.} \quad (5-95)$$

Then, the transfer function $H_q(s)$ from the quantization noise $N_q(s)$ to the output phase $\Theta_c(s)$ is given by

$$H_q(s) \equiv \frac{\Theta_c(s)}{N_q(s)} = \frac{K_0/s}{1 + K_d K_0 P(s) F(s)/s} . \quad (5-96)$$

From substituting Equations (2-9) and (5-9) into (5-96), it follows that

$$H_q(s) = \frac{K_0 \tau_1 s (1 + \tau_p s)}{\tau_1 s^2 (1 + \tau_p s) + K_0 K_d (1 + \tau_2 s)} . \quad (5-97)$$

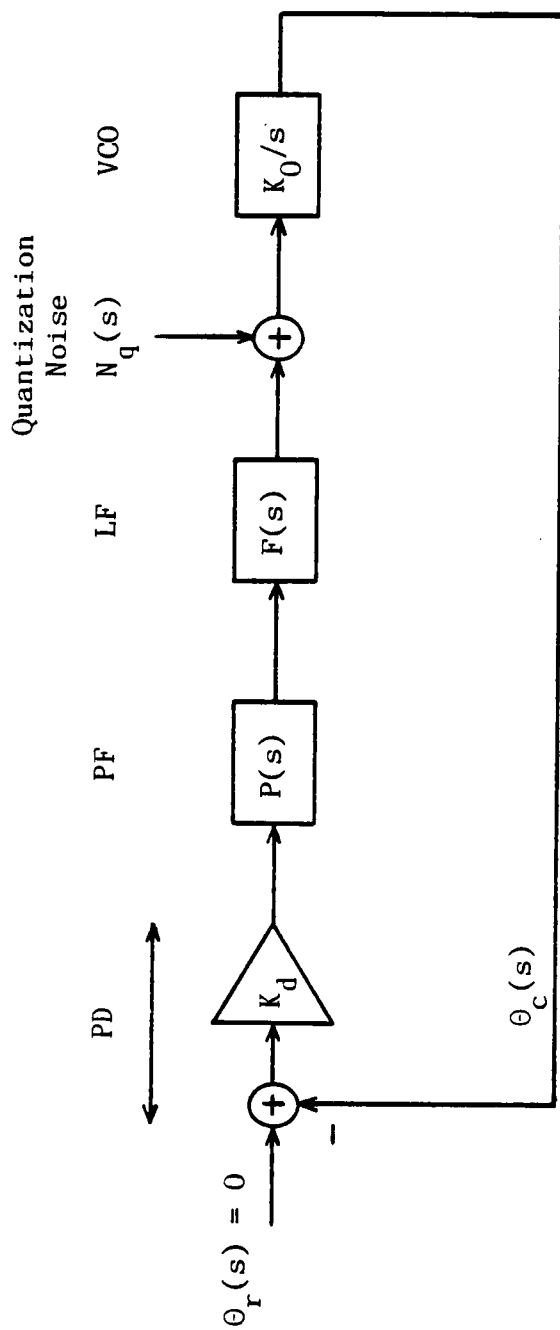


Figure 5.9. Continuous model to analyze the output phase jitter caused by the D/A quantization noise.

If $\tau_p = 0$, then

$$H_q(s) = K_0 \frac{s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (5-98)$$

Since $1/\tau_2$ and ω_n are much lower than $1/\tau_p$, Equation (5-97) can be approximated to (5-98) from zero to $1/\tau_p$ rad/s. Figure 5.10 shows the Bode plot of $|H_q(j\omega)|$ given by Equation (5-97). It can be approximated as a band-pass filter with ± 20 dB slopes and a center frequency of ω_n ($= 31.8$ krad/s). Its peak is given by

$$\max |H_q(j\omega)| = |H_q(j\omega_n)| = K_0/(2\zeta\omega_n) = 46.4 \quad \text{dB} \quad (5-99)$$

Since the cut-off frequency of the PF ($= 1/\tau_p = 2$ Mrad/s) is much higher than ω_n , the effect of the PF is negligible. Thus, the approximate transfer function given by Equation (5-98) can be used for further analysis. Equation (5-98) can be expressed as

$$H_q(s) = \delta \frac{s + \gamma}{(s + \alpha)(s + \beta)} \quad (5-100)$$

where

$$\delta = K_0 \quad (5-101)$$

$$\gamma = 0 \quad (5-102)$$

$$\alpha + \beta = 2\zeta\omega_n \quad (5-103)$$

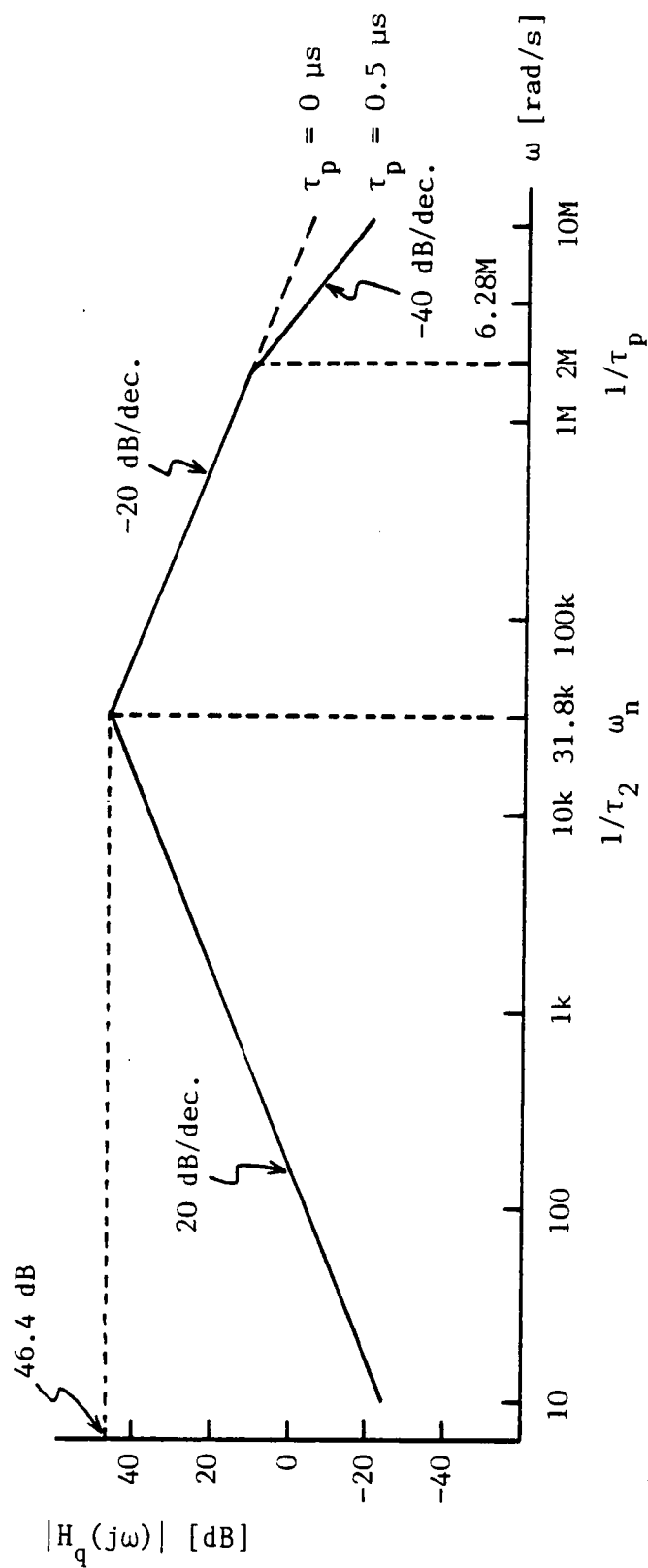


Figure 5.10. Bode plot of the transfer function $H_q(j\omega)$ from the D/A quantization noise to the output phase.

$$\alpha\beta = \omega_n^2 \quad (5-104)$$

The variance of the output phase jitter, $\sigma_{\theta c}^2$, is calculated by the following integration.

$$\sigma_{\theta c}^2 = \int_{-\infty}^{\infty} S_q(j2\pi f) |H_q(j2\pi f)|^2 df \quad \text{rad}^2 \quad (5-105)$$

where $S_q(j2\pi f)$ is the power spectrum of the quantization noise given by Equations (5-94) and (5-95). From the same calculation procedures and approximations as discussed in the previous A/D quantization noise analysis,

$$\sigma_{\theta c}^2 \approx \frac{2^{-2m} T}{12} \frac{K_0^2}{4\zeta\omega_n} \quad (5-106)$$

$$= \frac{2^{-2m}}{12} \frac{1}{2} \frac{K_0}{K_d} \frac{\tau_1}{\tau_2} T \quad \text{rad}^2 \quad (5-107)$$

is obtained. Compared to Equation (5-92), Equation (5-106) has inverted τ_1 and τ_2 . From substituting $K_0 = 2.1 \times 10^7$ rad/s/V, $K_d = 0.476$ V/rad, $\tau_1 = 9.9 \times 10^{-3}$ s, $\tau_2 = 1.0 \times 10^{-4}$ s, and $T = 1$ μ s into Equation (5-107),

$$\sigma_{\theta c}^2 \approx 2^{-2m} \times 1.82 \times 10^2 \quad \text{rad}^2 \quad (5-108)$$

is obtained.

Furthermore, it can be shown that the discrete analysis yields the same result given by Equation (5-107).

Effect of Input Noise. It is necessary to specify the frequency bandwidth of the input noise in order to discuss its effect. Assume that the input noise is Gaussian, stationary, and white noise. Thus, the magnitude of its Fourier spectrum is similar to the overall IF response shown in Figure 3.3 (pp. 21). It is asymmetric with respect to the picture IF carrier. Then, in order to simplify further analysis, assume that the power spectrum of the noise at the input of the hybrid PLL synchronous video detector, $S_n(j2\pi f)$, is symmetric and defined by the following equations.

$$S_n(j2\pi f) = \text{constant} \quad \text{for } f_{IF} - B_i/2 \leq f \leq f_{IF} + B_i/2 \quad (5-109)$$

$$= 0 \quad \text{otherwise} \quad (5-110)$$

where B_i means the IF bandwidth, and

$$B_i = 6 \quad \text{MHz.} \quad (5-111)$$

Additional noise higher in frequency than the picture carrier IF makes results a little more pessimistic than would actually be obtained. The maximum frequency of the noise at the input of the phase detector in the linear model, $f_{n', \max}$, is a half of the IF bandwidth B_i . That is,

$$f_{n', \max} = B_i/2 = 3 \quad \text{MHz.} \quad (5-112)$$

Thus, the power spectrum of the input noise in the linear model, $S_n(j2\pi f)$, is defined by

$$S_n(j2\pi f) = \sigma'^2/B_i \quad \text{for } -B_i/2 \leq f \leq B_i/2 \quad (5-113)$$

$$= 0 \quad \text{otherwise} \quad (5-114)$$

where σ'^2 designates the input phase noise given by Equation (2-37). Since $B_i/2$ is six times higher than the Nyquist frequency ($= f_{ck}/2 = 0.5$ MHz), the hybrid PLL suffers aliasing noise.

Instead of analyzing the discrete model, the continuous model shown in Figure 5.11 is analyzed. It approximates the discrete model very well within the Nyquist frequency, if the aliasing noise is properly considered.

The output phase jitter of the analog PLL, σ_A^2 , is calculated by the following integration.

$$\sigma_A^2 = \int_{-\infty}^{\infty} S_n(j2\pi f) |H_n(j2\pi f)|^2 df \quad \text{rad}^2 \quad (5-115)$$

where $H_n(s)$ designates the transfer function from the input noise $N'(s)$ to the output phase $\theta_c(s)$. From substituting Equations (5-113) and (5-114) into (5-115),

$$\sigma_A^2 = \frac{\sigma'^2}{B_i} \int_{-B_i/2}^{B_i/2} |H_n(j2\pi f)|^2 df \quad \text{rad}^2 \quad (5-116)$$

is obtained. In addition, the transfer function is expressed as

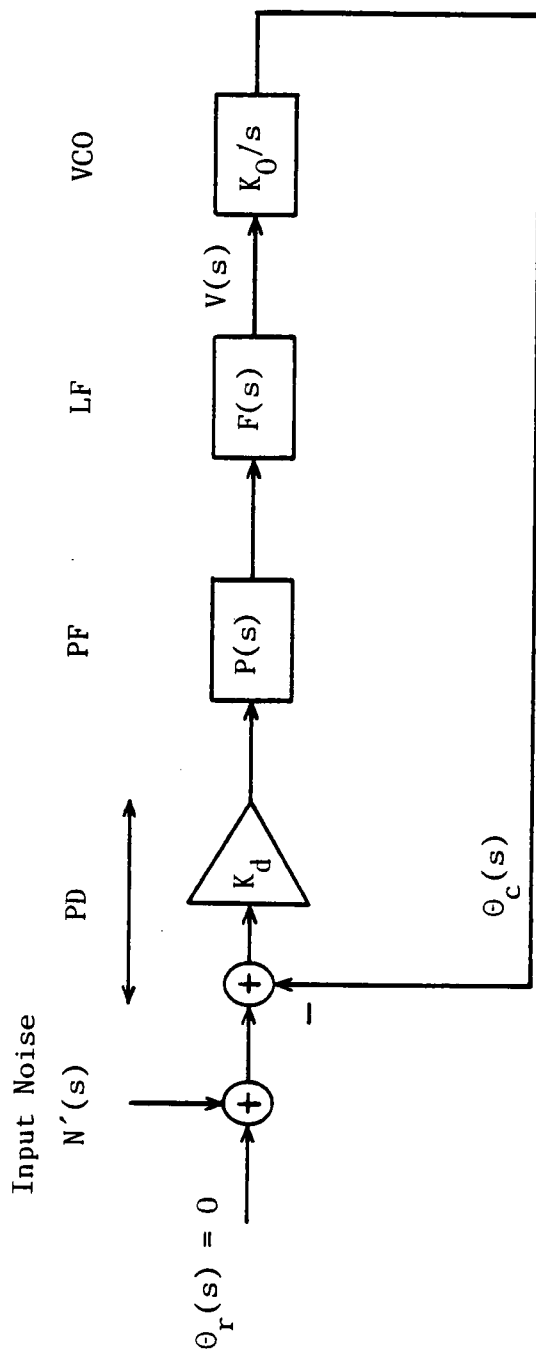


Figure 5.11. Continuous model to analyze the output phase jitter caused by the input noise.

$$H_n(s) \equiv \frac{\Theta_c(s)}{N'(s)} = \frac{K_0 K_d P(s) F(s) / s}{1 + K_0 K_d P(s) F(s) / s} \quad (5-117)$$

From substituting Equations (2-9) and (5-9) into (5-117), it follows that

$$H_n(s) = \frac{K_0 K_d (1 + \tau_p s)}{\tau_1 s^2 (1 + \tau_p s) + K_0 K_d (1 + \tau_2 s)} \quad (5-118)$$

If $\tau_p = 0$, then

$$H_n(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = H_p(s). \quad (5-119)$$

This is the same as the closed-loop phase transfer function given by Equation (2-16). Since $1/\tau_2$ and ω_n are much lower than $1/\tau_p$, Equation (5-118) can be approximated to (5-119) from zero to $1/\tau_p$ rad/s. Figure 5.12 shows the Bode plot of $|H_n(j\omega)|$ given by Equation (5-118). It can be approximated as a first-order low-pass filter with cut-off frequency ω_n ($= 31.8$ krad/s). Since the cut-off frequency of the PF ($= 1/\tau_p = 2$ Mrad/s) is much higher than ω_n , the effect of the PF is negligible for the analog PLL. Thus, Equation (5-116) becomes

$$\sigma_A^2 \approx \frac{\sigma'^2}{B_i} \int_{-\infty}^{\infty} |H_p(j2\pi f)|^2 df = \frac{2\sigma'^2 B_L}{B_i} \text{ rad}^2. \quad (5-120)$$

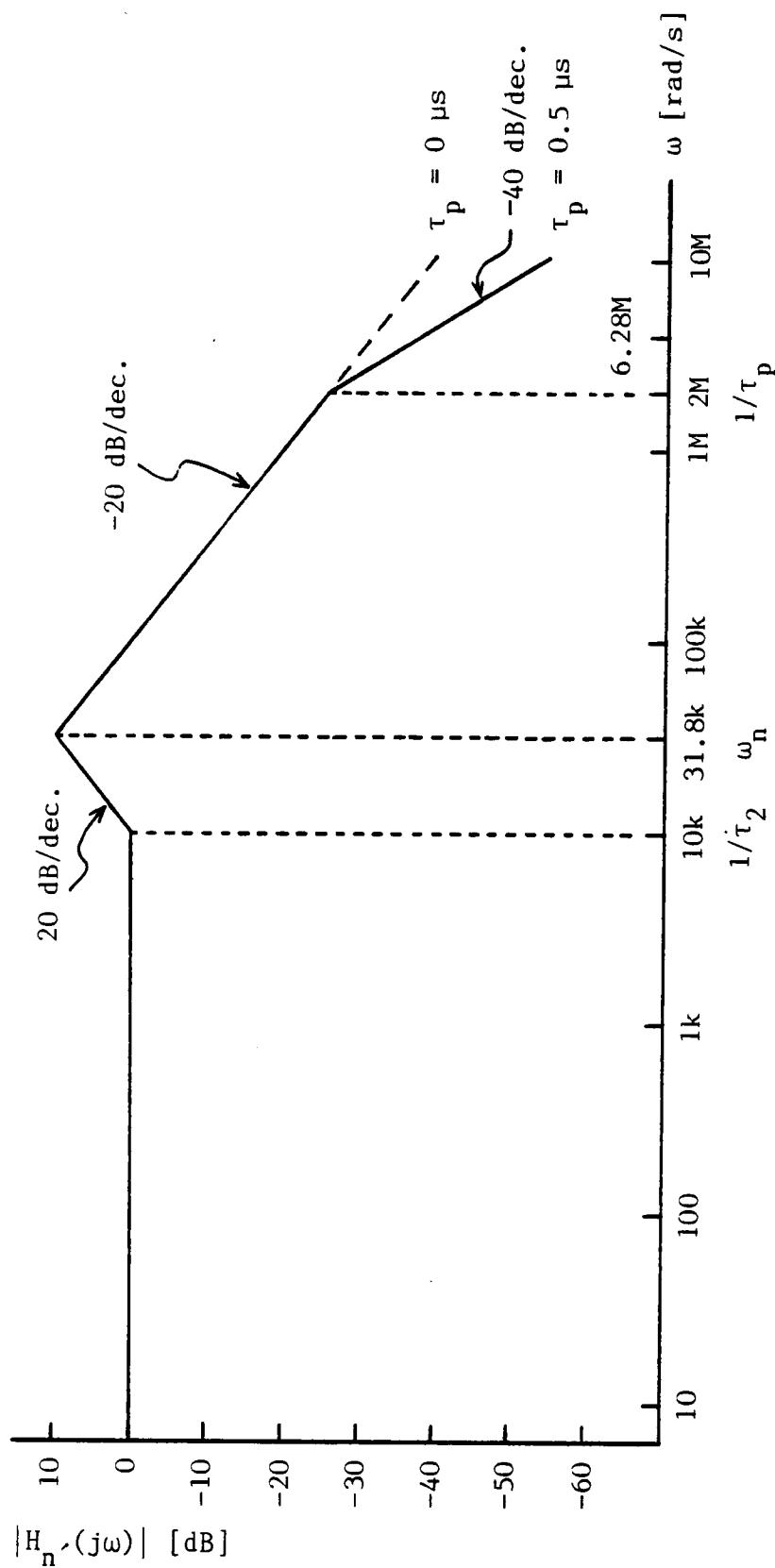


Figure 5.12. Bode plot of the transfer function $H_n(j\omega)$ from the input to the output.

This is the same result given by Equation (2-42). Thus, from Equation (2-44),

$$\sigma_A^2 = B_L / \{B_i (\text{SNR})_i\} \quad \text{rad}^2 \quad (5-121)$$

is obtained. Since the substitution of Equations (5-6) and (5-7) into (2-45) yields

$$B_L = 27.8 \quad \text{kHz}, \quad (5-122)$$

Equation (5-121) becomes

$$\sigma_A^2 = 4.63 \times 10^{-3} / (\text{SNR})_i \quad \text{rad}^2. \quad (5-123)$$

The output phase jitter of the hybrid PLL, σ_H^2 , is calculated by the following approximation.

$$\sigma_H^2 \approx \int_{-f_{ck}/2}^{f_{ck}/2} S_{n'H}(j2\pi f) |H_n(j2\pi f)|^2 df \quad \text{rad}^2 \quad (5-124)$$

where $H_n(j2\pi f)$ is given by Equation (5-118), and $S_{n'H}(j2\pi f)$ is the power spectrum of the input noise (original noise along with aliasing noise). Since the maximum frequency of the original input noise is six times higher than the Nyquist frequency, $S_{n'H}(j2\pi f)$ can be approximated to a constant. That is,

$$S_{n'H}(j2\pi f) \approx \frac{\sigma'^2}{B_i} \frac{B_i}{f_{ck}} C_p \quad \text{for } -f_{ck}/2 \leq f \leq f_{ck}/2 \quad (5-125)$$

$$= 0 \quad \text{otherwise.} \quad (5-126)$$

The first factor is the original component as shown in Equation (5-113). The second factor shows the increase of noise caused by the aliasing effect. The last factor C_p designates the reduction of noise by the pre-alias filter (PF). It is defined by

$$C_p \equiv \int_{-B_i/2}^{B_i/2} |P(j2\pi f)|^2 df. \quad (5-127)$$

From substituting Equation (5-9) into (5-127),

$$C_p = \arctan(\pi\tau_p B_i) / (\pi\tau_p B_i) \quad (5-128)$$

is obtained. Then, from substituting Equations (5-125) and (5-126) into (5-124),

$$\sigma_H^2 \approx \frac{\sigma'^2}{B_i} \frac{B_i}{f_{ck}} C_p \int_{-f_{ck}/2}^{f_{ck}/2} |H_n(j2\pi f)|^2 df \quad \text{rad}^2 \quad (5-129)$$

is obtained. Since $|H_n(j2\pi f)|$ is approximated to $|H_p(j2\pi f)|$ given by Equation (5-119), Equation (5-129) becomes

$$\sigma_H^2 \approx \frac{\sigma'^2}{B_i} \frac{B_i}{f_{ck}} C_p \int_{-\infty}^{\infty} |H_p(j2\pi f)|^2 df \quad \text{rad}^2. \quad (5-130)$$

Thus, from substituting Equation (5-120) into (5-130),

$$\sigma_H^2 \approx \frac{2\sigma'^2 B_L}{B_i} \frac{B_i}{f_{ck}} C_p = \sigma_A^2 \frac{B_i}{f_{ck}} C_p \quad \text{rad}^2 \quad (5-131)$$

is obtained. In addition, from substituting $B_i = 6$ MHz, $f_{ck} = 1$ MHz, and $\tau_p = 0.5$ μ s into Equation (5-131),

$$\sigma_H^2 \approx \sigma_A^2 \times 6 \times 0.1555 = \sigma_A^2 \times 0.933 \quad \text{rad}^2 \quad (5-132)$$

is obtained. If $\tau_p = 1/(2\pi)$ μ s, then

$$\sigma_H^2 \approx \sigma_A^2 \times 6 \times 0.4163 = \sigma_A^2 \times 2.50 \quad \text{rad}^2. \quad (5-133)$$

Therefore, $\tau_p = 1/(2\pi)$ μ s is proved to be insufficient.

Computer Analysis and Discussion. First of all, the criterion of the output phase jitter ~~must be determined~~. Since the television signal is modulated by vestigial sideband modulation (VSB) [11], the output signal of the detector, $y(t)$, is expressed as

$$y(t) = 2 \times \text{LPF}[\{s(t)\cos\omega t + s'(t)\sin\omega t\} \times \cos(\omega t + \theta_e)] \quad (5-134)$$

$$= s(t)\cos\theta_e + s'(t)\sin\theta_e \quad (5-135)$$

where $s(t)$ and $s'(t)$ are the in-phase and quadrature components of the video signal, respectively, ω is the carrier angular frequency, θ_e is the output phase error, and the symbol $\text{LPF}[]$ represents the function of a low-pass filter. The first and second terms in Equation (5-135) are the desired in-phase signal and the undesired quadrature signal, respectively. The criterion is that the output phase error stays under 1 deg in the case of a moderate input signal-to-noise ratio (about 40 dB). That is,

$$\theta_e \leq 1 \text{ deg for } (\text{SNR})_i \approx 40 \text{ dB} \quad (5-136)$$

From Equation (5-135), it follows that the 1 deg output phase error generates 0.015 % desired signal error and 1.75 % undesired quadrature signal. The same criterion is applied to the standard deviation of the output phase jitter. That is,

$$\sigma_{\theta_c} \leq 1 \text{ deg} = 0.0175 \text{ rad for } (\text{SNR})_i \approx 40 \text{ dB} \quad (5-137)$$

Every analysis except the tracking performance uses the same phase detector, loop filter, and VCO. That is, the following parameters are fixed: $K = 1.0 \times 10^7 \text{ 1/s}$, $K_0 = 2.1 \times 10^7 \text{ rad/s/V}$, $K_d = 1/2.1 \approx 0.476 \text{ V/rad}$, $\tau_1 = 9.9 \times 10^{-3} \text{ s}$, $\tau_2 = 1.0 \times 10^{-4} \text{ s}$, $f_{ck} = 1 \text{ MHz}$, $B_i = 6 \text{ MHz}$, $t_s = 10 \text{ } \mu\text{s}$, and $t_h = 50 \text{ } \mu\text{s}$.

In addition, it is assumed that the loop filter has infinite word length. Furthermore, the amplitude of the input signal designated by A_r in Equation (2-1) is assumed to be one. Then, from Equations (2-37) and (2-38), it follows that

$$\sigma'^2 = \sigma^2/2 \quad (5-138)$$

$$(\text{SNR})_i = 1/\sigma^2 \quad (5-139)$$

Figure 5.13 shows the relationship between the resolution of the A/D and the output phase jitter for the C mode. The pre-alias filter is not used in this analysis. Variable parameters are the input signal-to-noise ratio and the loop delay. Theoretical lines

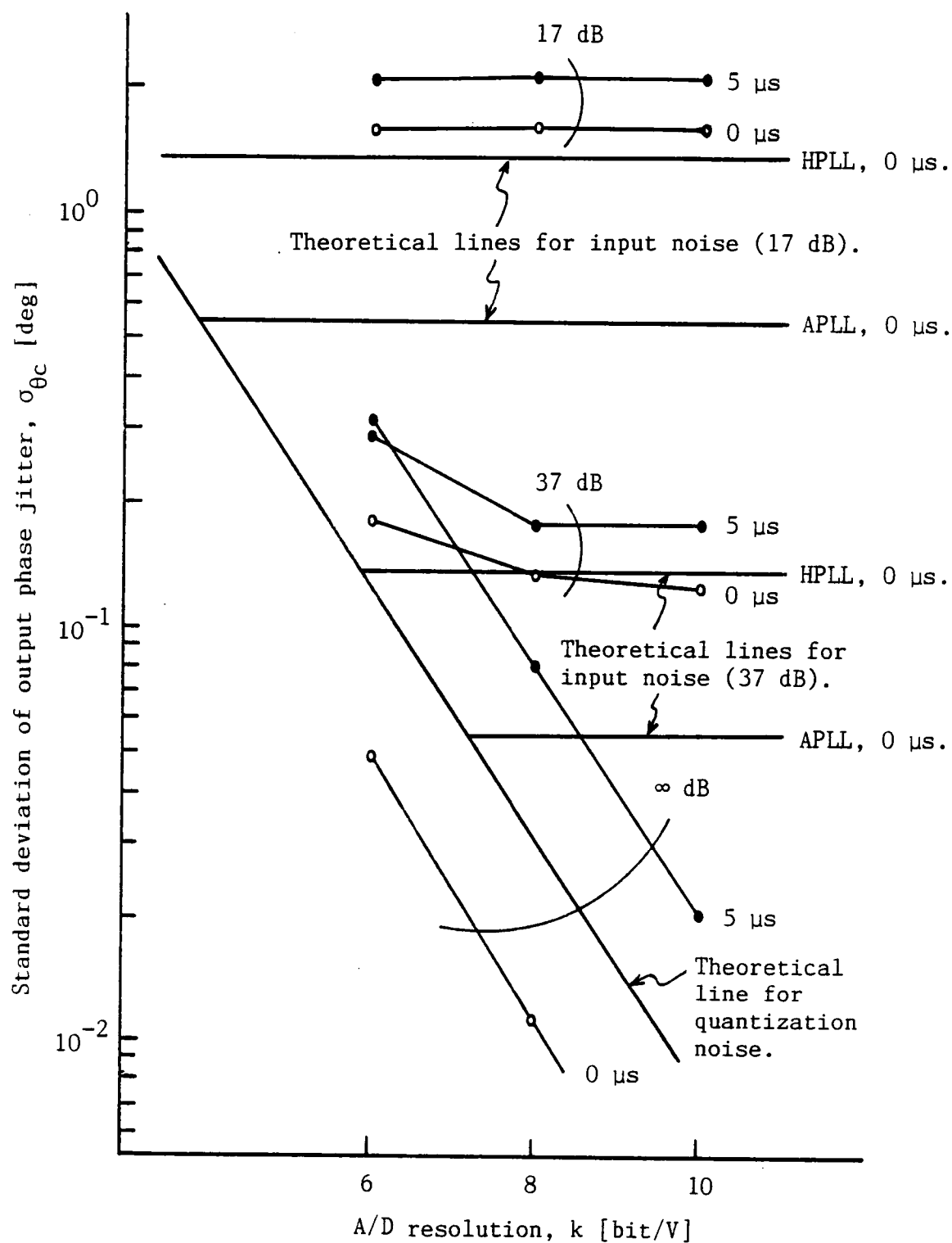


Figure 5.13. Output phase jitter versus A/D resolution.

for the input noise of the analog PLL (APLL) and the hybrid PLL (HPLL) are obtained from Equations (5-120) and (5-131) with $C_p = 0$, respectively. The theoretical line for the quantization noise is obtained from Equation (5-93). Every theoretical line is obtained from the model with zero loop delay. Every result by computer analysis is close to the corresponding theoretical line. It is observed that the loop delay increases the output phase jitter. The 6-bit/V A/D contributes more output phase jitter than the 8-bit/V A/D under a moderate signal-to-noise ratio of 37 dB. Thus, the following results are obtained from this analysis.

- (1) The 8-bit/V A/D is desirable.
- (2) It is desirable to use some pre-alias filter.

Figure 5.14 shows the relationship between the input SNR and the output phase jitter for the C mode. The resolution of the A/D is 8 bit/V, and the loop delay is 5 μ s. The variable parameter is the time constant of the pre-alias filter (PF), τ_p . Theoretical lines are obtained from Equations (5-132) and (5-133). The results for $\tau_p = 0.5$ and $1/(2\pi)$ μ s are close to the corresponding theoretical lines when the input SNR is less than 37 dB. The PF with $\tau_p = 0.5$ μ s reduces the output phase jitter more than the PF with $\tau_p = 1/(2\pi)$ μ s. However, the results for $\tau_p = 1$ μ s, which are not given in the figure for the purpose of simplicity, are almost the same as those for $\tau_p = 0.5$ μ s. The reason is that the increase of the output phase jitter by the phase lag of the PF dominates the decrease of the output phase jitter by the reduction

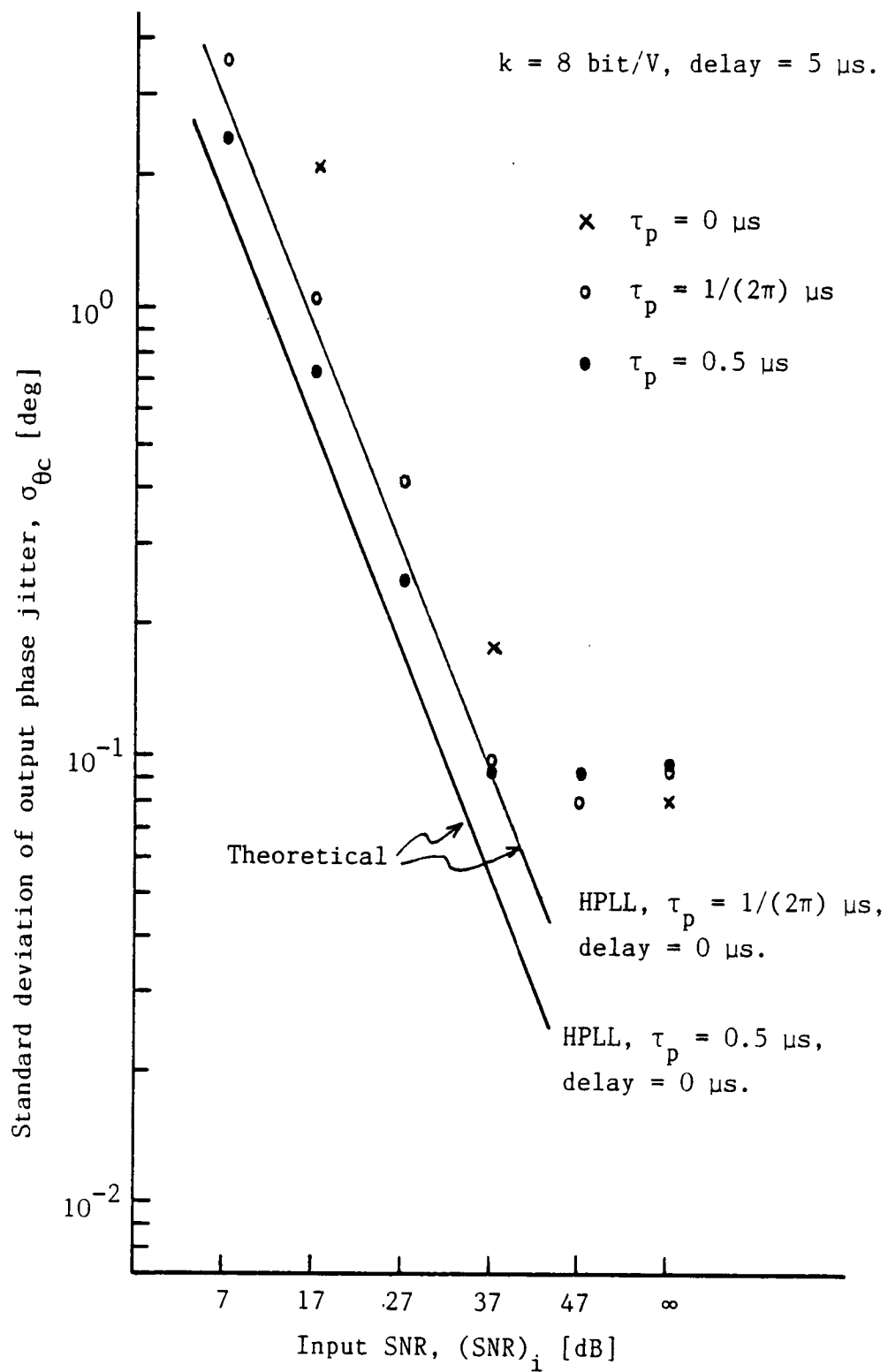


Figure 5.14. Output phase jitter versus input SNR.
(The effect of pre-alias filter)

of aliasing noise. The output phase jitter remains constant (≈ 0.1 deg) when the input SNR is more than 37 dB. The reason is that the A/D quantization noise in the closed-loop generates a kind of limit cycle. Thus, it can be considered that the 8-bit/V A/D is better than the 6-bit/V A/D, and the following results are obtained from this analysis.

- (1) The 8-bit/V A/D is desirable.
- (2) The desirable time constant of the PF is $0.5 \mu\text{s}$.

Figure 5.15 shows the relationship between the resolution of the D/A and the output phase jitter for the C mode. The resolution of the A/D is 8 bit/V. The loop delay is $5 \mu\text{s}$. The time constant of the PF is $0.5 \mu\text{s}$. The variable parameter is the input SNR. Theoretical input noise lines and quantization noise line are obtained from Equation (5-132) and (5-108), respectively. The results, except for the case of infinite input SNR, are close to the theoretical lines. If the input SNR is infinite, and if the D/A resolution is more than 14 bit/V, then the output phase jitter remains constant (≈ 0.1 deg). A kind of limit cycle mentioned earlier is considered as the cause. Since the results obtained from the 12-bit/V D/A are very close to the criterion, it is insufficient. Thus, the following results are obtained.

- (1) At least a 14-bit/V D/A is necessary.
- (2) The output phase jitter remains constant (≈ 0.1 deg) when the input SNR is more than 37 dB.

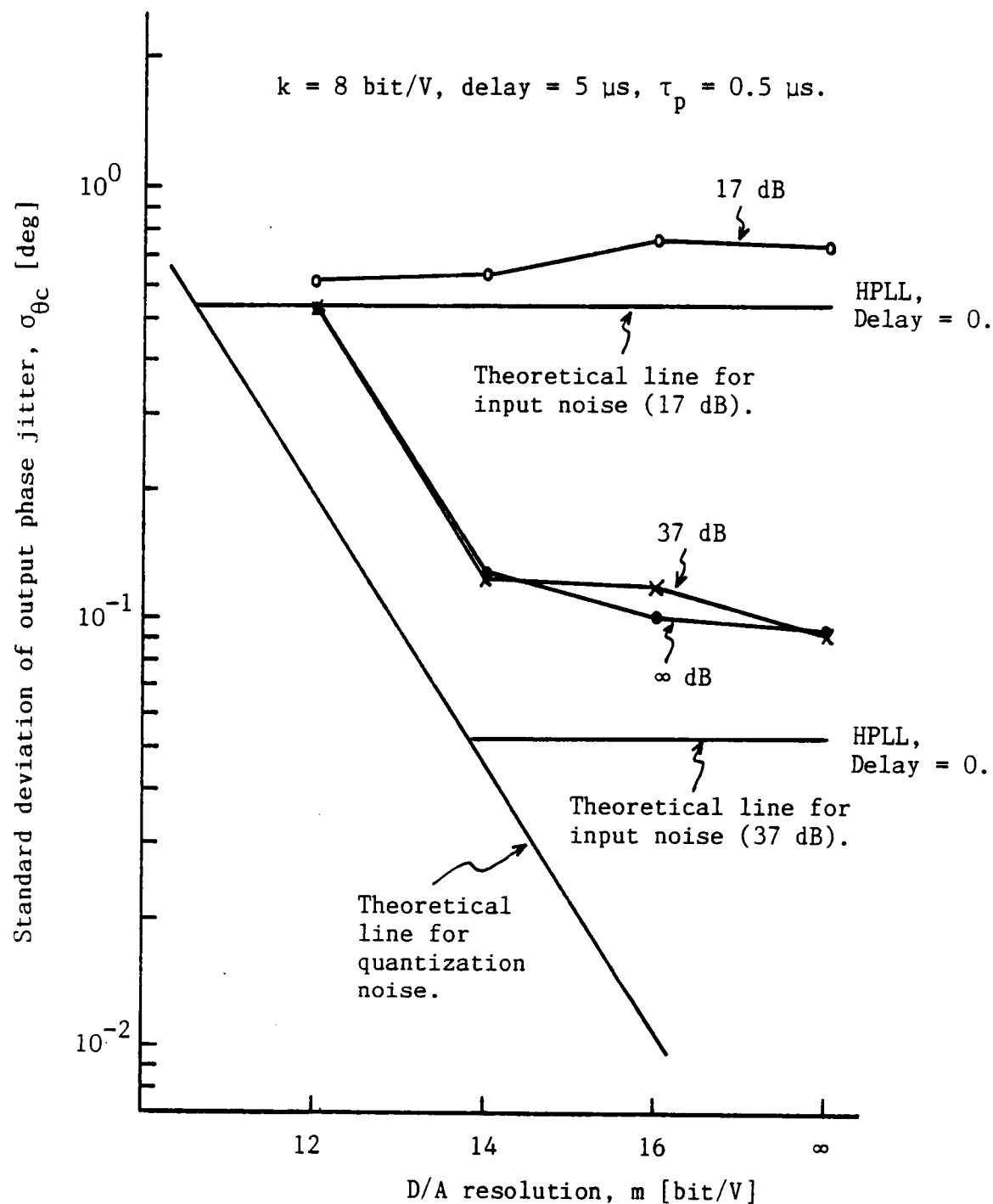


Figure 5.15. Output phase jitter versus D/A resolution.

All results shown so far are obtained from the C mode analysis. Figure 5.16 shows the effect of the S/H mode. The resolution of the A/D and the D/A are 8 and 16 bit/V, respectively. The loop delay is 5 μ s. The time constant of the PF is 0.5 μ s. The sample period and the hold period are 10 and 50 μ s, respectively. The S/H mode shows more output phase jitter than the C mode, but it satisfies the criterion.

Output Phase Drift in Hold Period

Voltage error at the VCO input causes output phase drift during the hold period. The phase drift is the same as the phase error, and it reaches a maximum at the end of each hold period. Thus, it must stay under some limit, say, specified by Equation (5-136). On the other hand, the following equation is easily obtained.

$$v_e = \theta_d / (K_0 t_h) \quad V \quad (5-140)$$

where v_e V designates the voltage error at the VCO input, and θ_d rad designates the output phase drift. From substituting $\theta_d \leq 1$ deg = 0.0175 rad, $K_0 = 2.1 \times 10^7$ rad/s/V, and $t_h = 50$ μ s into Equation (5-140),

$$v_e \leq 1.67 \times 10^{-5} \text{ V for } (\text{SNR})_i \approx 40 \text{ dB} \quad (5-141)$$

is obtained.

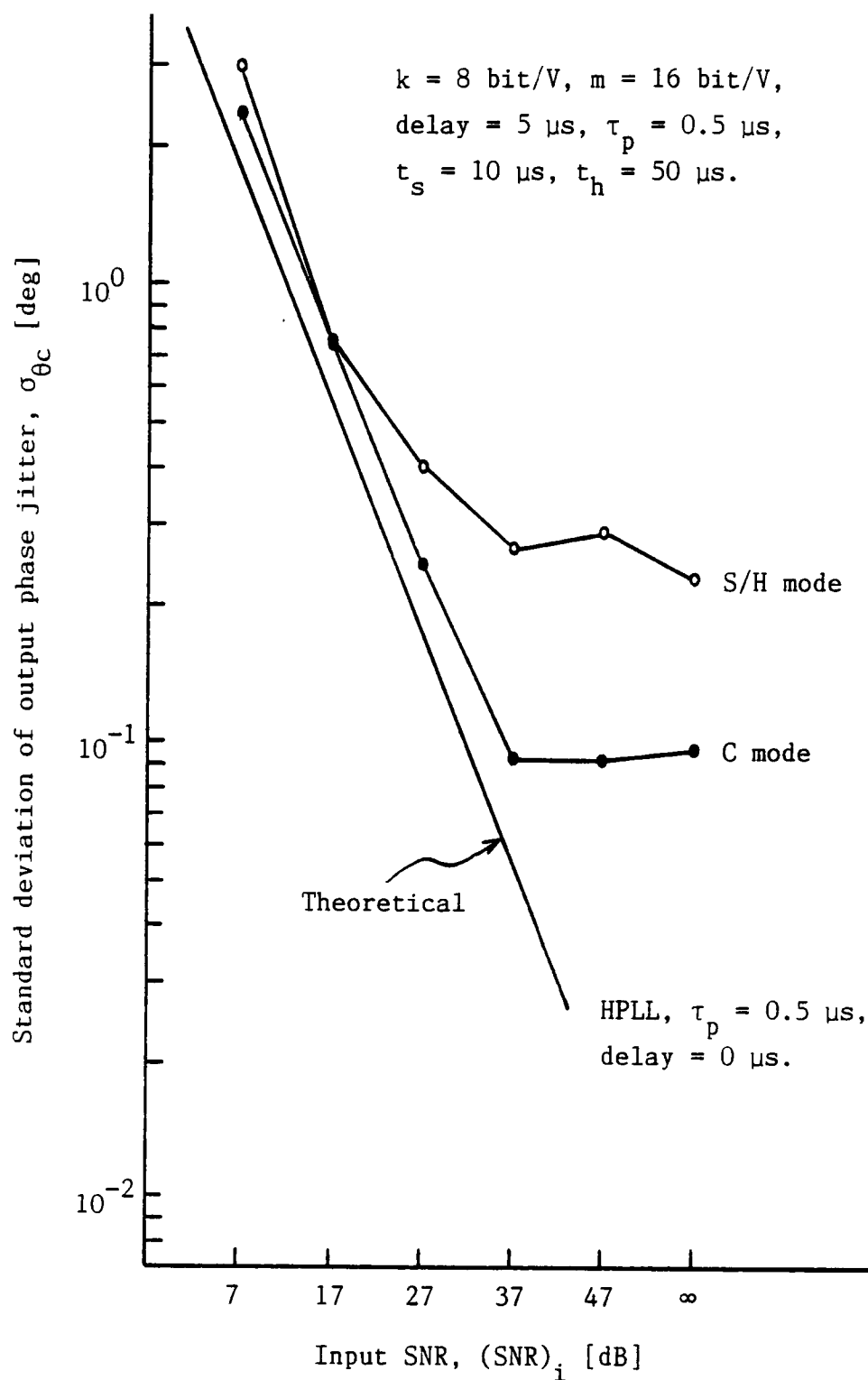


Figure 5.16. Output phase jitter versus input SNR.
(The effect of sample and hold mode)

The maximum output error caused by a m -bit/V D/A is $2^{-(m+1)}$ V. Let $m = 16$, then it is equal to 7.63×10^{-6} V. Let $m = 14$, then the error is 3.05×10^{-5} V. Therefore, the 16-bit/V D/A satisfies the criterion, but the 14-bit/V D/A does not.

VCO Input Jitter

The VCO input jitter for the C mode is analyzed here. This analysis gives a pessimistic value of the VCO input jitter for the S/H mode. Since the procedure for this analysis is almost the same as discussed in the output phase jitter analysis, detailed discussion is omitted.

Effect of A/D Quantization Noise. The model is shown in Figure 5.7 (pp. 55). The transfer function $H_q(s)$ from the quantization noise $N_q(s)$ to the VCO input $V(s)$ is given by

$$H_q(s) = \frac{s(1 + \tau_2 s)(1 + \tau_p s)}{\tau_1 s^2(1 + \tau_p s) + K_0 K_d(1 + \tau_2 s)} \quad (5-142)$$

Figure 5.17 shows its Bode plot. Since ω_n and $1/\tau_2$ are much lower than $1/\tau_p$, the effect of τ_p is negligible. So, let $\tau_p = 0$, then

$$H_q(s) = \frac{\tau_2}{\tau_1} \frac{s(s + 1/\tau_2)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (5-143)$$

This equation may be approximated by a constant gain of τ_2/τ_1 over

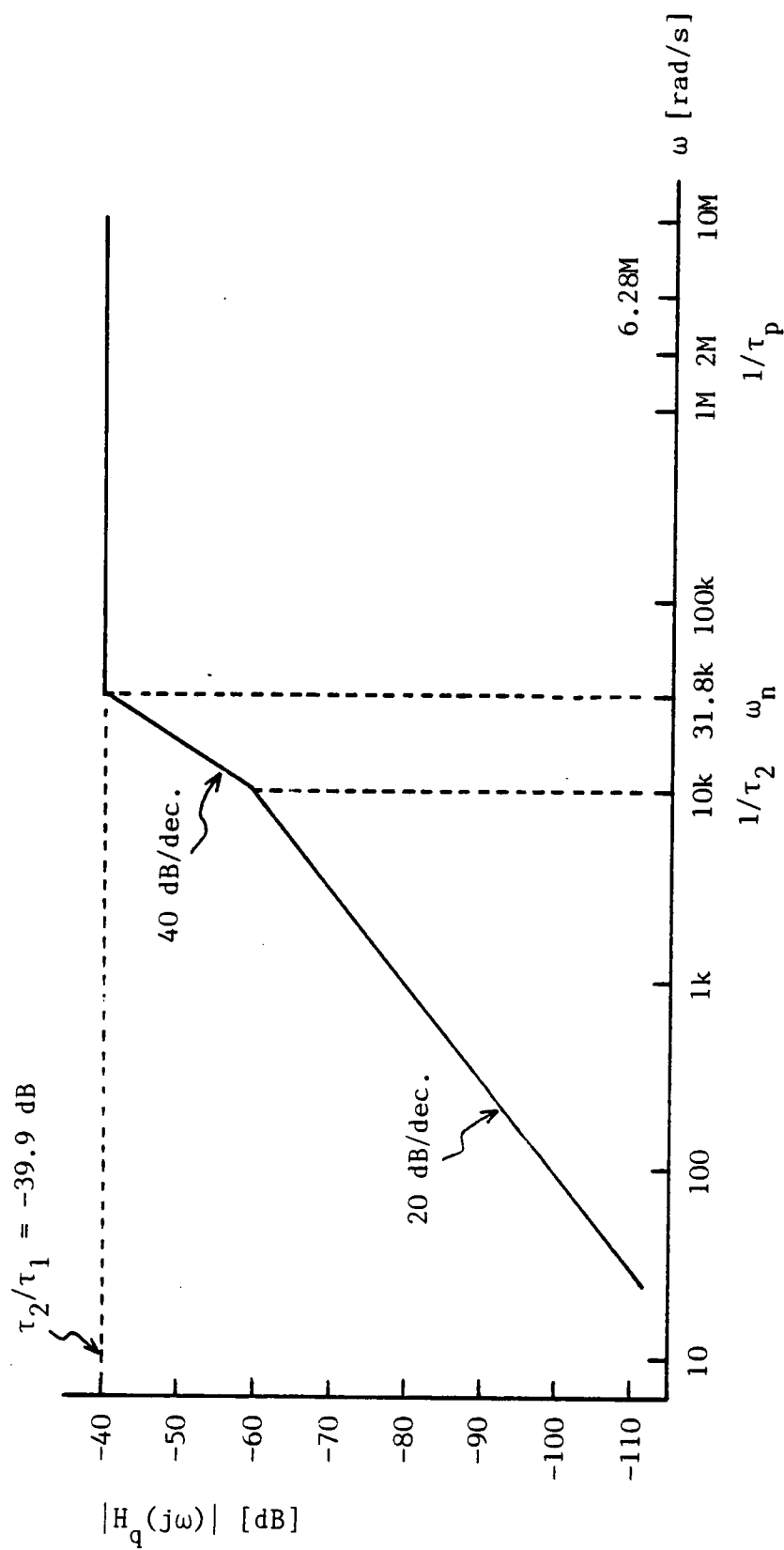


Figure 5.17. Bode plot of the transfer function $H_q(j\omega)$ from the A/D quantization noise to the VCO input.

the frequencies of interest. Then, from Equations (5-71), (5-72), (5-81), and this constant gain approximation,

$$\sigma_v^2 \approx (\tau_2/\tau_1)^2 \int_{-1/(2T)}^{1/(2T)} \frac{2^{-2k}}{12} T df = (\tau_2/\tau_1)^2 \frac{2^{-2k}}{12} \quad (5-144)$$

is obtained, where k designates the word length of the A/D per Volt. Let $\tau_1 = 9.9 \times 10^{-3}$ s and $\tau_2 = 1.0 \times 10^{-4}$ s, then

$$\sigma_v^2 \approx 1.02 \times 10^{-4} \times 2^{-2k}/(12) \quad v^2. \quad (5-145)$$

Effect of D/A Quantization Noise. Since the D/A output is directly fed into the VCO, the VCO input jitter is equal to the power of the D/A quantization noise. That is,

$$\sigma_v^2 = 2^{-2m}/(12) \quad v^2 \quad (5-146)$$

where m designates the word length of the D/A per Volt.

Effect of Input Noise. The model is shown in Figure 5.11 (pp. 68). The transfer function $H_n(s)$ from the input noise $N'(s)$ to the VCO input $V(s)$ is given by

$$H_n(s) = \frac{K_d s(1 + \tau_2 s)}{\tau_1 s^2(1 + \tau_p s) + K_0 K_d(1 + \tau_2 s)}. \quad (5-147)$$

Figure 5.18 shows its Bode plot. Since ω_n and $1/\tau_2 \ll 1/\tau_p$, the frequency characteristic of Equation (5-147) may be approximated

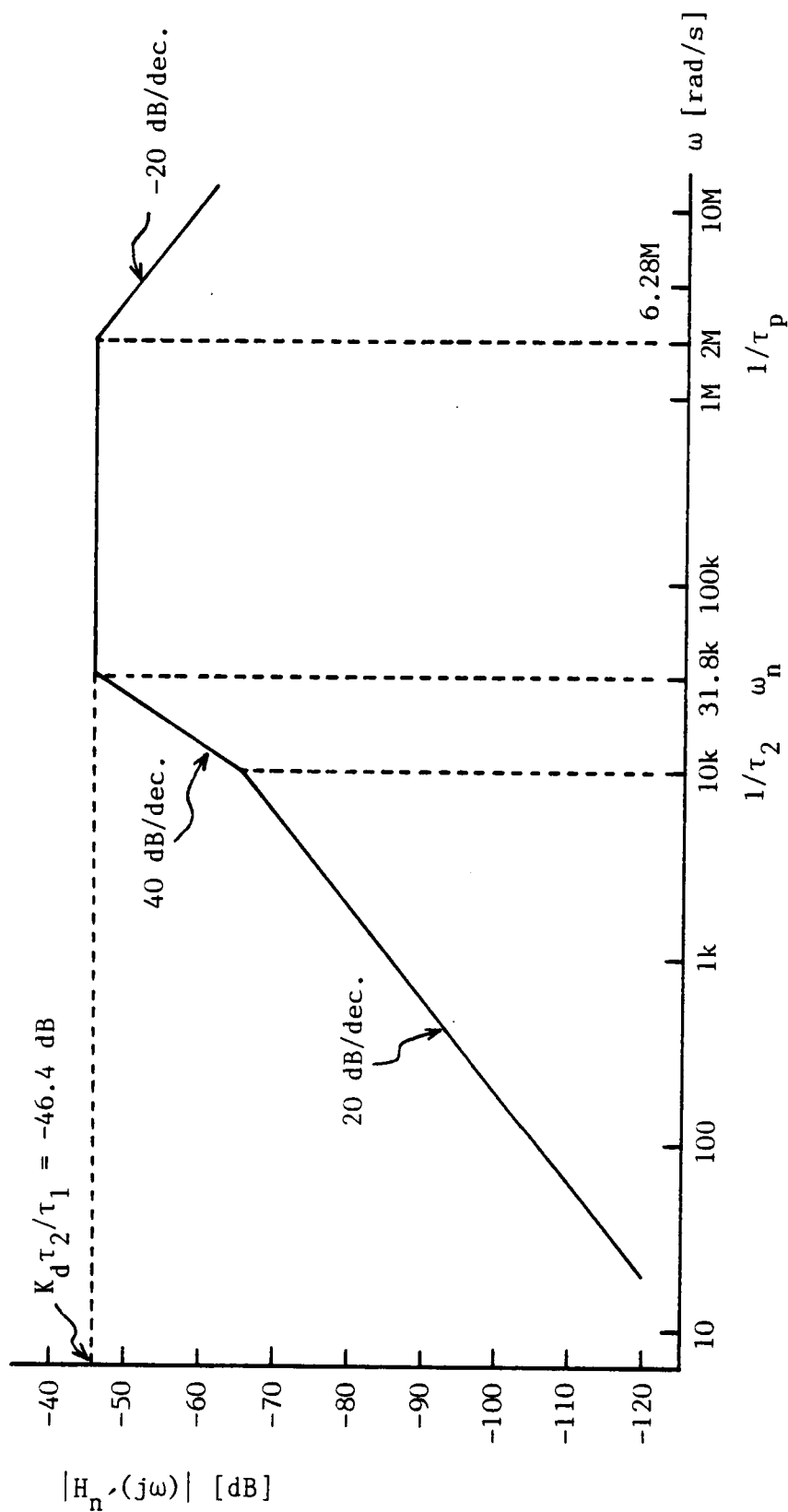


Figure 5.18. Bode plot of the transfer function $H_n(j\omega)$ from the input to the VCO input.

by that of a wide-band low-pass filter with gain $K_d\tau_2/\tau_1$ and cut-off frequency $1/\tau_p$. If there is no pre-alias filter (PF), Equation (5-147) may be approximated by a constant gain of $K_d\tau_2/\tau_1$ over the frequencies of interest. When the frequency characteristic of a transfer function is that of an all-pass filter or a wide-band low-pass filter with cut-off frequency near the Nyquist frequency, the VCO input jitter of the hybrid PLL is close to that of the analog PLL.

The VCO input jitter without the PF, σ_v^2 , is obtained from substituting $H_n = K_d\tau_2/\tau_1$ into Equation (5-116) and using (5-138) and (5-139). That is,

$$\sigma_v^2 \approx (K_d\tau_2/\tau_1)^2 \times \sigma'^2 = (K_d\tau_2/\tau_1)^2 / \{2(\text{SNR})_i\} \quad \text{V}^2. \quad (5-148)$$

Let $\tau_1 = 9.9 \times 10^{-3}$ s, $\tau_2 = 1.0 \times 10^{-4}$ s, and $K_d = 1/2.1$ V/rad, then

$$\sigma_v^2 \approx 1.16 \times 10^{-5} / (\text{SNR})_i \quad \text{V}^2. \quad (5-149)$$

The VCO input jitter with the PF, σ_v^2 , is obtained from multiplying Equation (5-148) by (5-128). That is,

$$\sigma_v^2 \approx C_p (K_d\tau_2/\tau_1)^2 / \{2(\text{SNR})_i\} \quad \text{V}^2. \quad (5-150)$$

Let $\tau_p = 0.5$ μ s and $B_i = 6$ MHz, then $C_p = 0.156$. Then

$$\sigma_v^2 \approx 1.81 \times 10^{-6} / (\text{SNR})_i \quad \text{V}^2. \quad (5-151)$$

Computer Analysis and Discussion. Figure 5.19 shows the relationship between the resolution of the A/D and VCO input jitter for the C mode. The loop delay is 5 μ s. Variable parameters are the input SNR and the time constant of the prealias filter (PF). Theoretical lines for the input noise are obtained from Equations (5-149) and (5-151). The theoretical line for the quantization noise is obtained from Equation (5-145). All results by the computer analysis are close to the corresponding theoretical lines. The results of the 8-bit/V A/D slightly exceed the criterion value of 1.67×10^{-5} V for $(\text{SNR})_1 \approx 40$ dB, which results in an output phase drift of 1 deg. However, these results can be considered as satisfactory because the values calculated from the C mode analysis are more pessimistic than those given by the S/H mode analysis. The reason comes from the noise reduction effect of the integration path in the digital loop filter, and it will be discussed later.

Figure 5.20 shows the relationship between the resolution of the D/A and VCO input jitter for the C mode. The resolution of the A/D is 8 bit/V. The loop delay is 5 μ s. The time constant of the PF is 0.5 μ s. The variable parameter is the input SNR. Theoretical lines for the input noise and the quantization noise are obtained from Equations (5-151) and (5-146), respectively. The results except for the case of infinite SNR are close to the theoretical lines. If the input SNR is infinite, and if the D/A resolution is more than 14 bit/V, then the VCO input phase jitter

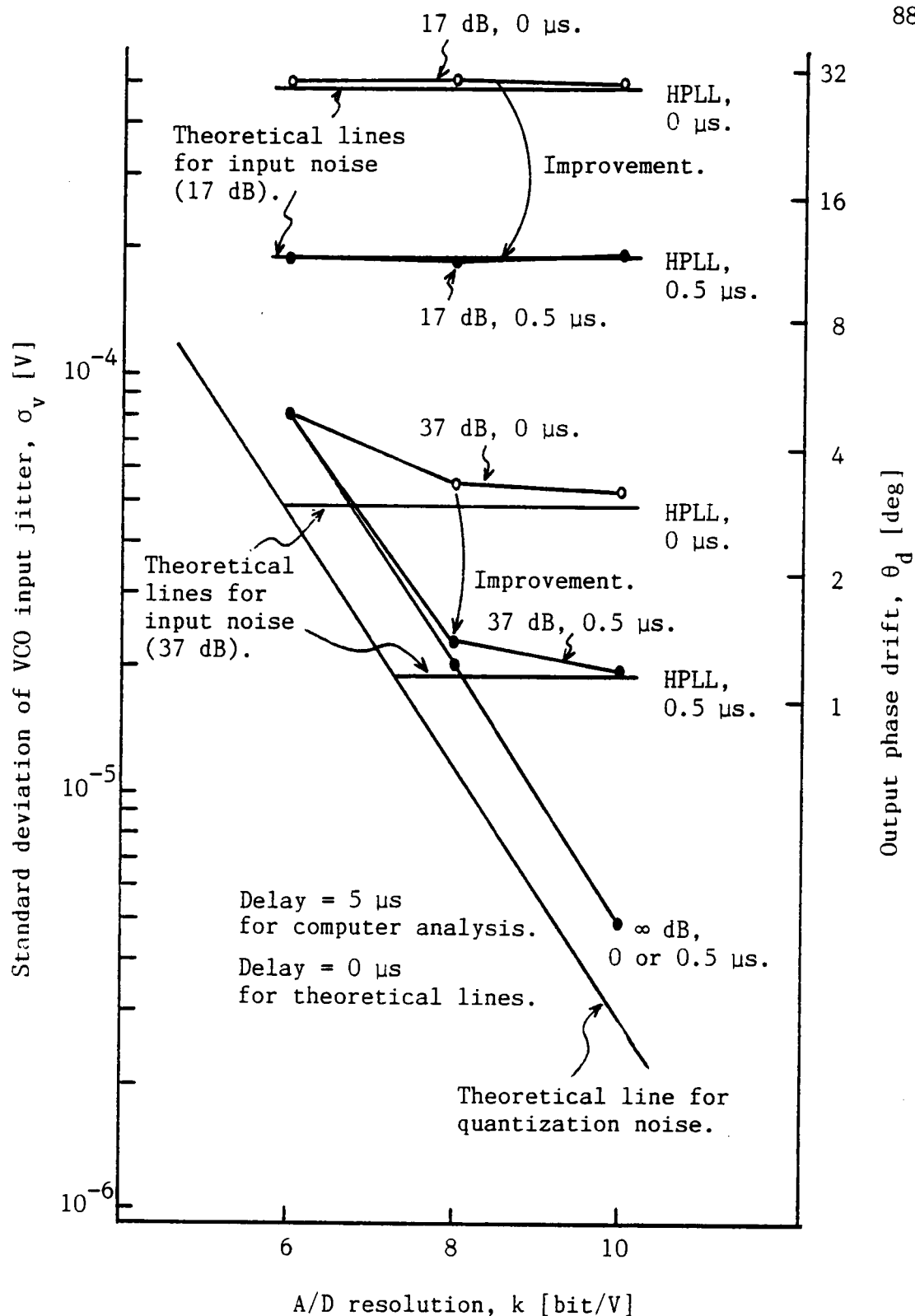


Figure 5.19. VCO input jitter and corresponding output phase drift versus A/D resolution.

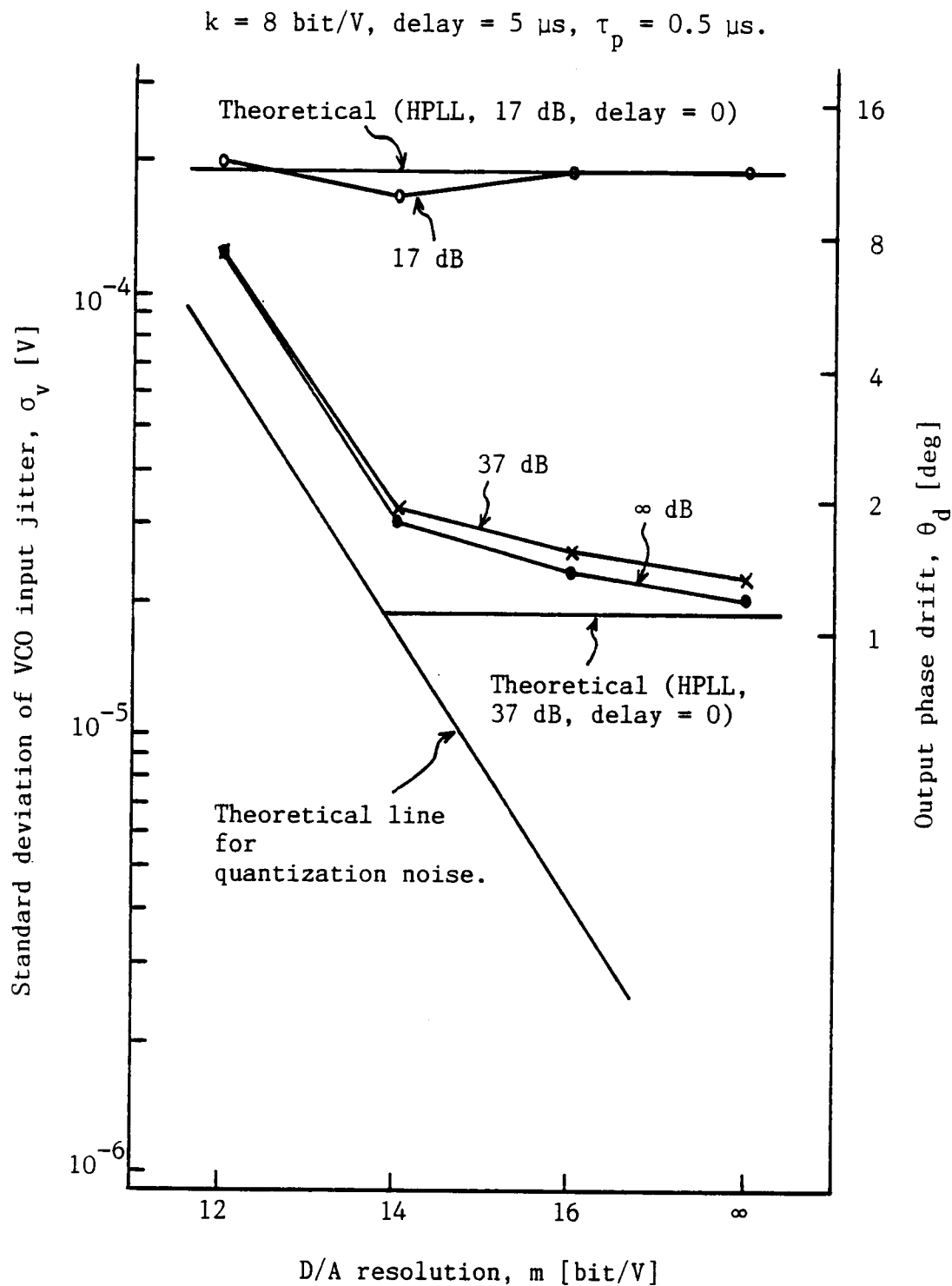


Figure 5.20. VCO input jitter and corresponding output phase drift versus D/A resolution.

remains constant ($\approx 2 \times 10^{-5}$ V). The reason is that the A/D quantization noise in the closed-loop generates a kind of limit cycle.

Figure 5.21 shows the effect of the S/H mode. The resolution of the A/D and the D/A are 8 and 16 bit/V, respectively. The loop delay is 5 μ s. The time constant of the PF is 0.5 μ s. The sample and hold periods are 10 and 50 μ s, respectively. The reason the VCO input jitter remains constant at high input SNR is that the A/D quantization noise in the closed-loop generates a kind of limit cycle. The results of the C mode at low input SNR are very close to the theoretical line given by Equation (5-151). The S/H mode shows less VCO input jitter than the C mode. Since the variance of the direct path in the digital loop filter (DLF) is much larger than that of the integration path in the DLF, the VCO input jitter in the sample period becomes larger than that in the hold period. In addition, the VCO input jitter of the S/H mode is the same as that of the C mode during the sample period. Thus, the VCO input jitter of the S/H mode can be smaller on the average than that of the C mode. The jitter of the integration path will be analyzed later. The results for the S/H mode satisfy the criterion of 1.67×10^{-5} V for $(\text{SNR})_i \approx 40$ dB, which results in an output phase drift of 1 deg.

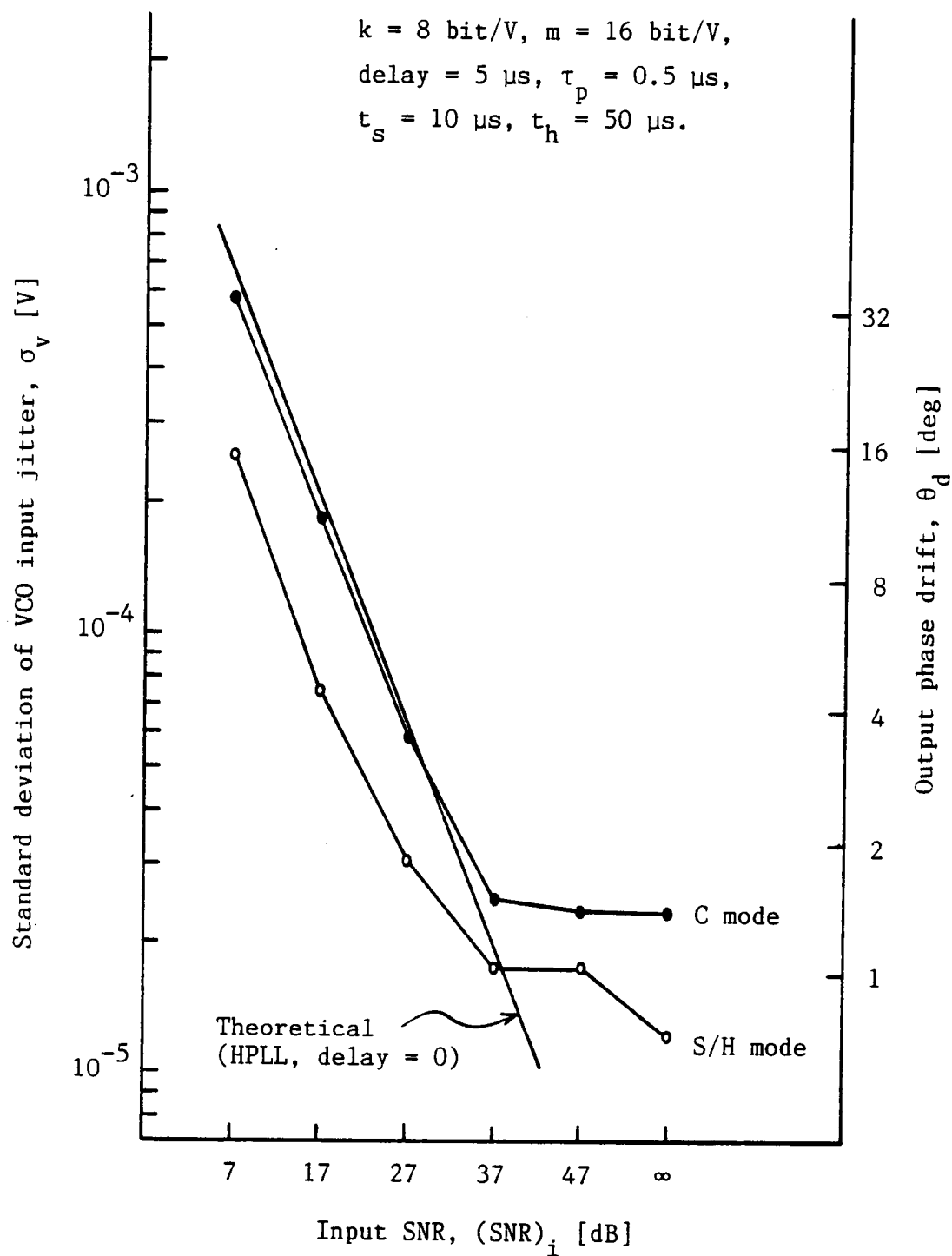


Figure 5.21. VCO input jitter and corresponding output phase drift versus input SNR.

Jitter of Integration Path in Loop Filter

Figure 5.22 shows the discrete model for analyzing the jitter of the integration path in the digital loop filter (DLF) caused by input noise. The pre-alias filter (PF) is omitted to simplify the calculation. Using the A/D output signal in Laplace transform, $U^*(s)$, defined by Equation (5-22), the input signal $U(s)$ is given by

$$U(s) = K_d \{N'(s) - F(z)G_2(s)U^*(s)\} \quad (5-152)$$

where $N'(s)$ designates the input noise, $F(z)$ defined by Equations (5-15) through (5-20) designates the DLF, and $G_2(s)$ defined by Equation (5-27) designates the D/A and the VCO. From Equations (5-152) and (5-27), it can be shown that

$$U(z) = \frac{K_d N'(z)}{1 + K_d F(z)G_2(z)} \quad (5-153)$$

$$G_2(z) = K_0 T / (z - 1). \quad (5-154)$$

The maximum frequency of the input noise, $f_{n,\max}$ ($= 3$ MHz), defined by Equation (5-112), is much higher than the Nyquist frequency of 0.5 MHz. Thus the power spectrum of the input noise with the aliasing effect, $S_n'(\exp(j\omega T))$, is close to the power of the original input noise. That is

$$S_n'(\exp(j\omega T)) \approx \sigma'^2 \quad \text{rad}^2/\text{Hz}. \quad (5-155)$$

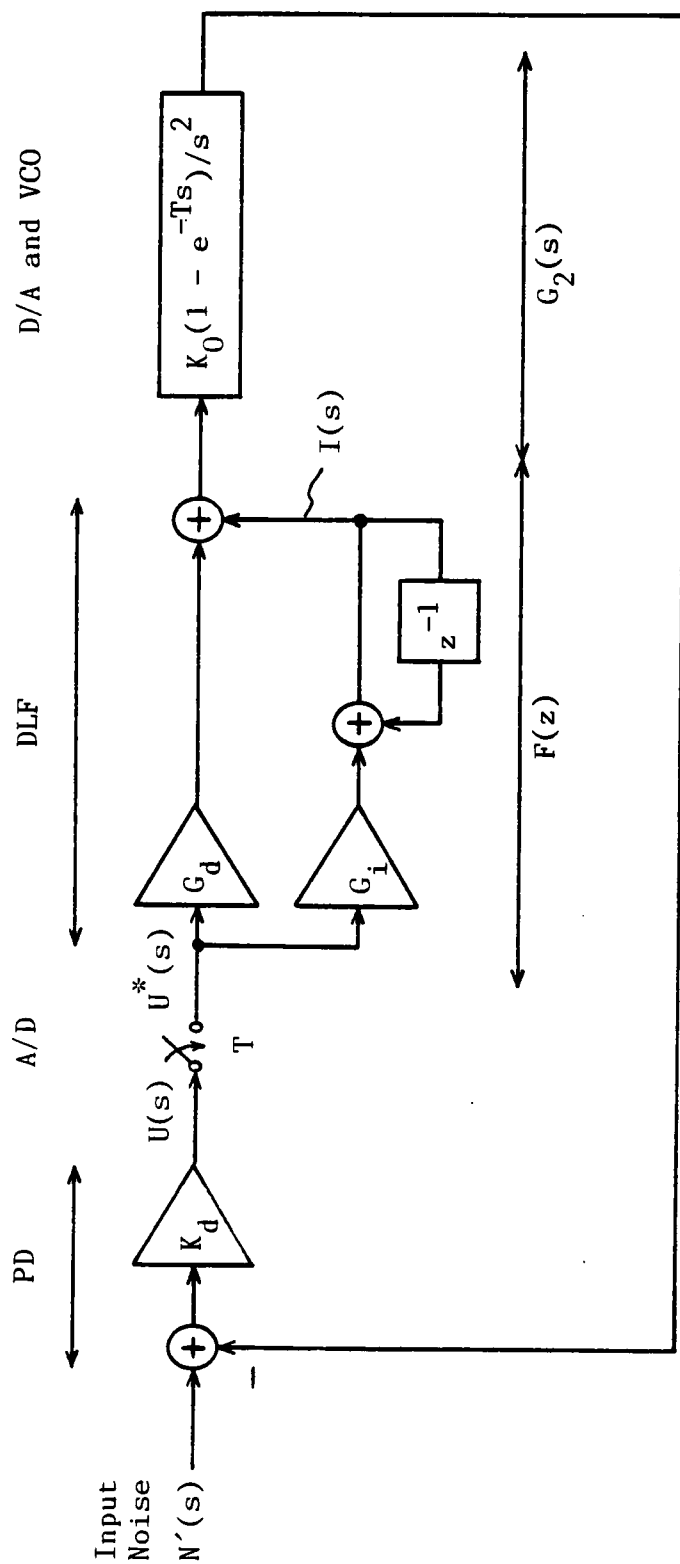


Figure 5.22. Discrete model to analyze the jitter of the integration path in the digital loop filter caused by the input noise.

In other words, the sum of the input noise and its aliasing components produces uncorrelated white noise similar to quantization noise.

In addition, the output of the integration path in the DLF, $I(z)$, is expressed as

$$I(z) = \frac{G_i}{1 - z^{-1}} U(z). \quad (5-156)$$

Thus, from substituting Equations (5-153) and (5-154) into (5-156), the following transfer function $H_n(z)$ is obtained.

$$H_n(z) \equiv \frac{I(z)}{N'(z)} = K_f K_d (1 - z_0) \frac{z(z - 1)}{(z - \alpha)(z - \beta)} \quad (5-157)$$

where

$$\alpha \approx 1 \quad (5-158)$$

$$\beta \approx 1 - \epsilon \quad (5-159)$$

$$\epsilon \equiv K_0 K_d T \tau_2 / \tau_1. \quad (5-160)$$

Thus, Equation (5-157) is approximated to

$$H_n(z) \approx \frac{K_d T}{\tau_1} \frac{z}{z - \beta}. \quad (5-161)$$

On the other hand, the variance of the jitter of the

integration path, σ_i^2 , is calculated from the following integration (also see Equation (5-53)).

$$\sigma_i^2 = \frac{T}{2\pi} \int_{-\pi/T}^{\pi/T} S_n(\exp(j\omega T)) |H_n(\exp(j\omega T))|^2 d\omega \quad v^2 \quad (5-162)$$

From substituting Equations (5-155) and (5-161) into (5-162) and using the new variable Ω defined by Equation (5-55), the following equation is obtained.

$$\sigma_i^2 \approx \frac{\sigma'^2 P}{2\pi} \int_{-\pi}^{\pi} \frac{1}{1 - w \cos \Omega} d\Omega \quad (5-163)$$

where

$$P = \frac{(K_d T / \tau_1)^2}{1 + \beta^2} \quad (5-164)$$

$$w = 2\beta / (1 + \beta^2). \quad (5-165)$$

By Equation (5-64), Equation (5-163) becomes

$$\sigma_i^2 \approx \sigma'^2 \times (K_d T / \tau_1)^2 \times 1 / \{\epsilon(2 - \epsilon)\} \quad (5-166)$$

$$\approx \sigma'^2 \times (K_d T / \tau_1)^2 \times 1 / (2\epsilon). \quad (5-167)$$

Substituting Equation (5-160) into (5-167),

$$\sigma_i^2 \approx \sigma'^2 \frac{K_d T}{2K_0 \tau_1 \tau_2} \quad v^2 \quad (5-168)$$

is obtained. Finally, substituting $K_0 = 2.1 \times 10^7$ rad/s/V, $K_d = 0.476$ V/rad, $\tau_1 = 9.9 \times 10^{-3}$ s, $\tau_2 = 1.0 \times 10^{-4}$ s, and $T = 1.0$ μ s into Equation (5-168),

$$\sigma_i^2 \approx 1.14 \times 10^{-8} \times \sigma_v^2 \quad \text{V}^2 \quad (5-169)$$

is obtained.

Since the transfer function $H_n(\exp(j\omega T))$ approximated by Equation (5-161) is an all-pass type with a little attenuation at high frequency, the pre-alias filter (PF) reduces the jitter. The jitter-reduction by the PF is roughly estimated as a C_p value of 0.156, where C_p is defined by Equation (5-128).

Figure 5.23 shows the jitter of the integration path. The resolution of the A/D and the D/A are 8 and 16 bit/V, respectively. The loop delay is 5 μ s. The time constant of the PF is 0.5 μ s. The sample and hold periods are 10 and 50 μ s, respectively. The results at low input SNR stay between the theoretical line given by Equation (5-169) and the line with the effect of the C_p . Since the output signal of the integration path at high input SNR contains very low frequency components, its jitter tends to be constant at high input SNR. The reason is that the A/D quantization noise in the closed-loop generates a kind of limit cycle. The jitter (standard deviation) of the integration path is much smaller than that of the VCO input shown in

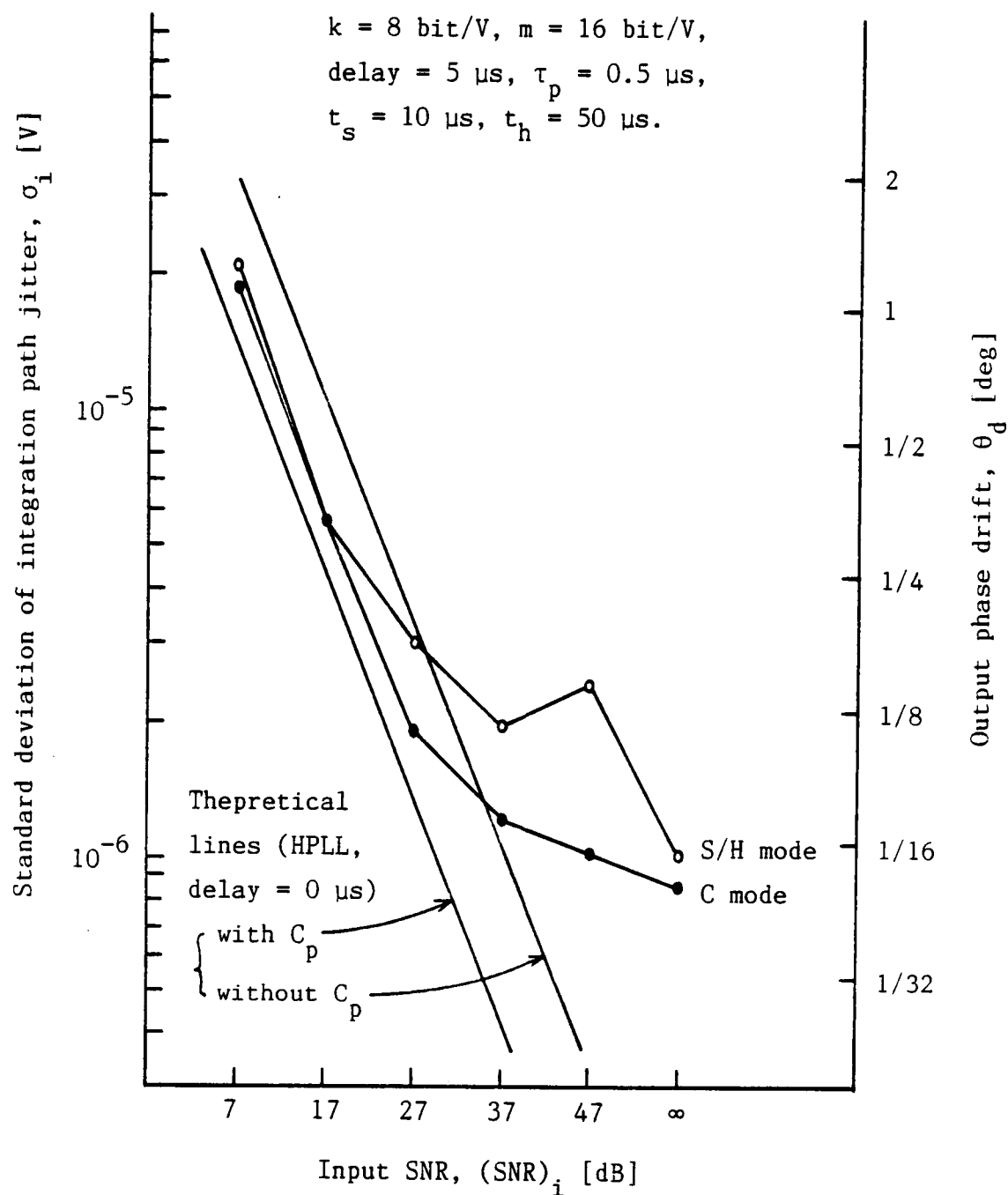


Figure 5.23. Integration path jitter and corresponding output phase drift versus input SNR.

Figure 5.21 (pp. 91) because the integrator reduces the jitter of the noise.

Tracking Performance

So far, the steady state and the phase step response have been analyzed to study the jitter and the stability, respectively. In addition, the ramp response (in other words, the frequency step response or the pull-in process) is also taken into consideration here.

At the initial step (for example, power-on or channel-change), the analog PLL is active, and it is designed to realize enough pull-in range.

At the intermediate step, the hybrid PLL in the C mode is active. Since its gain is infinite at zero frequency, the pull-in range is theoretically infinite as shown by Equation (2-29). Most important in this step is the pull-in time T_p for the maximum frequency offset Δf_{off} caused by the constant voltage offset in the digital blocks. Equation (2-31) gives a good approximation because the hybrid PLL in the C mode is well approximated as an analog PLL. From substituting $\Delta\omega = 2\pi \times 500 \times 10^3$ rad/s (the maximum frequency offset given by Equation (5-12)), $\zeta = 1.59$, and $\omega_n = 31.8 \times 10^3$ rad/s into Equation (2-31),

$$T_p \approx 96.5 \quad \text{ms} \quad (5-170)$$

is obtained. This value is small so that the PLL can finish the pull-in process quickly.

At the last step, the hybrid PLL in the S/H mode is active. The PLL in this mode must follow the frequency fluctuation caused by the VCO frequency jitter, the frequency jitter of the oscillator in the tuner, and the frequency jitter of the source signal. Its level can be considered far less than 10 kHz. This is because a 10 kHz offset carrier is used by some Japanese broadcasting stations in order to increase the practical number of VHF channels (90 - 220 MHz in Japan, 54 - 216 MHz in U.S.A.).

It is too difficult to obtain the analytic equation for the tracking process in the S/H mode, but a computer analysis gives the numerical result. The phase error in the phase step response or in the steady state is so small that a simple adder may represent the phase detector (PD) in the previous analyses. However, the phase error in the step frequency response is so large that the non-linear PD should be used in this analysis. Thus, the model used in this analysis is the same as used in the previous analyses except the PD. Instead of the characteristic of the original PD given by Equation (2-3), the characteristic shown in Figure 5.24 is used because it fits the simulation language (Advanced Continuous Simulation Language) and simplifies the analysis. The phase detector in this analysis is a kind of phase/frequency detector and results in a faster pull-in process than the original PD.

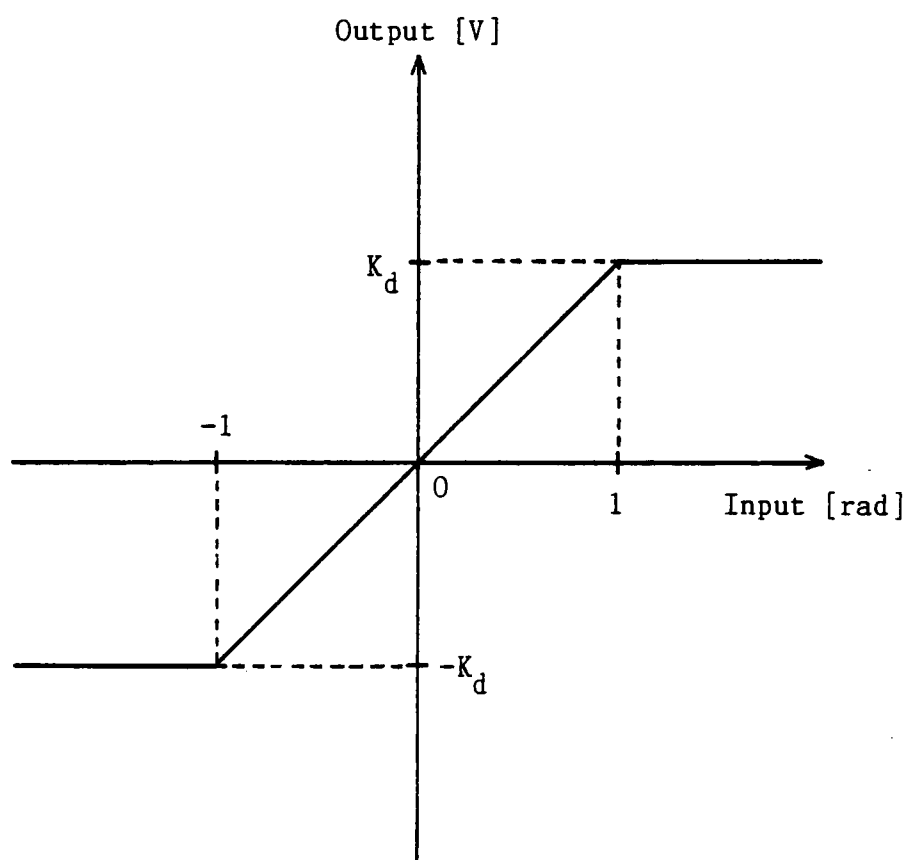


Figure 5.24. Characteristic of phase/frequency detector.

The parameters are the same as used in the previous analyses. the resolution of the A/D and the D/A are 8 and 16 bit/V, respectively. The loop delay is 5 μ s. The time constant of the PF is 0.5 μ s. The sample period and the hold period are 10 and 50 μ s, respectively. When the step frequency change is 10 kHz, the computer analysis shows that the pull-in time is 1.2 ms. The pull-in time used here is defined as the time which the PLL needs to follow the step frequency change and reduce the phase error to less than 1 deg. The time, 1.2 ms, can be considered relatively short, and a frequency step change as high as 10 kHz rarely happens. Therefore, it is considered that the PLL in the S/H mode has satisfactory tracking performance.

Comparison

The phase fluctuation of the conventional analog PLL caused by a heavy ghost is analyzed, and the phase drift of the hybrid PLL is compared to the results given by this analog PLL analysis.

To simplify analysis, assume that an amplitude limiter is placed before the PD input so that the PD will have a constant amplitude gain. Then, the response of the analog PLL for over-modulation caused by a heavy ghost is the same as the step response of the corresponding second-order system. Consider a heavy ghost with a delay of 10 μ s and a phase of 180 deg. This ghost is a typical example. That is, the over-modulated IF carrier with a duration of 10 μ s is fed to the PD.

First, consider the analog PLL, which has the same natural frequency ω_n and damping factor ζ as the hybrid PLL. Equations (5-6) and (5-7) show $\omega_n = 31.8$ krad/s and $\zeta = 1.59$, respectively. The step response is about 0.2 for a second-order system with $\zeta = 1.59$ and $t = 1/\omega_n$ [12]. If the time t is less than $3/\omega_n$, linear interpolation gives a good approximation. The over-modulation period, $10 \mu\text{s}$, is equal to $0.32/\omega_n$. Thus, the over-modulation results in a phase fluctuation of 11.5 deg ($= 0.32 \times 0.2 \times 180 \text{ deg}$). The phase drift of the hybrid PLL (1 deg) is much smaller than this result (11.5 deg).

Second, consider an analog PLL which has the same pull-in time and damping factor as a hybrid PLL in the S/H mode. This is an analysis for the analog PLL with a more narrow-band loop filter. The new natural frequency ω_n' of 10.1 krad/s is obtained from substituting the results from the tracking performance analysis (the pull-in time T_p of 1.2 ms , initial angular frequency difference $\Delta\omega$ of $2\pi \times 10$ krad/s, and damping factor ζ of 1.59) into Equation (2-31). Then, $10 \mu\text{s}$ is equal to $0.10/\omega_n'$. Thus, the over-modulation results in a phase fluctuation of 3.6 deg ($= 0.1 \times 0.2 \times 180 \text{ deg}$). The phase drift of the hybrid PLL (1 deg) is smaller than this result (3.6 deg).

Therefore, it is proved that the proposed hybrid PLL eliminates the phase fluctuation caused by heavy ghost interference.

CHAPTER VI

SUMMARY AND CONCLUSIONS

Summary

A new hybrid PLL synchronous video detector for a television receiver was developed. It contains a new hybrid PLL using a conventional analog PLL synchronous video detector. It eliminates the phase fluctuation caused by heavy ghosts and enables the ghost reduction system to function better.

Attributes of the hybrid PLL including the stability, the output phase jitter, the output phase drift, the VCO input jitter, the jitter of integration path, and the tracking performance were studied. The remaining parts of the detector have well known characteristics and can be designed by conventional methods. Design equations were derived from this study, and the results given by these equations were close to those obtained from the computer analysis. From these results and the possible physical conditions, a stable hybrid PLL with the following set of parameters was obtained:

loop gain, $K = 1.0 \times 10^7$ 1/s;

VCO gain, $K_0 = 2.1 \times 10^7$ rad/s/V;

PD gain, $K_d = 1/2.1 \approx 0.476$ V/rad;

time constants of the digital LF,

$\tau_1 = 9.9 \times 10^{-3}$ s, $\tau_2 = 1.0 \times 10^{-4}$ s;

clock frequency, $f_{ck} = 1.0$ MHz;

loop delay, 5 clocks ($= 5 \mu\text{s}$);
time constant of PF, $\tau_p = 0.5 \mu\text{s}$;
resolution of A/D, 8 bit/V;
conversion rate of A/D, 1 MHz;
resolution of D/A, 16 bit/V;
conversion rate of D/A, 1 MHz;
sample period, $t_s = 10.0 \mu\text{s}$;
hold period, $t_h = 50.0 \mu\text{s}$.

The following satisfactory results were obtained from this PLL:

phase jitter (standard deviation) for input SNR = 37 dB,
0.091 deg for C mode, 0.26 deg for S/H mode;
output phase drift for input SNR = 37 dB,
1.0 deg for S/H mode (For the heavy ghost with its delay of
10 μs and its phase of 180 deg, the corresponding analog
PLL shows phase fluctuation of 11.5 deg or 3.6 deg,
depending upon the characteristics of the PLL.);
pull-in time of C mode,
97 ms for 500.0 kHz step frequency change;
pull-in time of S/H mode,
1.2 ms for 10.0 kHz step frequency change.

Conclusions

The characteristics of a hybrid PLL with specified parameters for a television video detector were obtained from linear analysis. The detector's performance was considered to be

satisfactory. These parameters and the corresponding performance represent only one example. For any given set of conditions, the suitable parameters can be obtained from the equations derived in this study and by using the computer analysis. Further research is to study and evaluate the hardware performance of the developed synchronous detector.

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