MODELING AND SPICE IMPLEMENTATION OF SILICON-ON-INSULATOR (SOI) FOUR GATE (G4FET) TRANSISTOR

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Md Sakib Hasan

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DEDICATION

This dissertation is dedicated to my parents,

Zahir Uddin Ahmed

and

Shirin Akhter Lovely.

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ABSTRACT

As the device dimensions have reduced from micrometer to nanometer range, new bulk silicon devices are now facing many undesirable effects of scaling leading device engineers to look for new process technologies. Silicon-on-insulator (SOI) has emerged as a very promising candidate for resolving the major problems plaguing the bulk silicon technology. G^4FET [G4FET] is a SOI transistor with four independent gates. Although G^4FET has already shown great potential in different applications, the widespread adoption of a technology in circuit design is heavily dependent upon good SPICE (*Simulation Program with Integrated Circuit Emphasis*) models. CAD (Computer Aided Design) tools are now ubiquitous in circuit design and a fast, robust and accurate SPICE model is absolutely necessary to transform G^4FET into a mainstream technology.

The research goal is to develop suitable SPICE models for G^4FET to aid circuit designers in designing innovative analog and digital circuits using this new transistor. The first phase of this work is numerical modeling of the G^4FET where four different numerical techniques are implemented, each with its merits and demerits. The first two methods are based on multivariate Lagrange interpolation and multidimensional Bernstein polynomial. The third numerical technique is based on multivariate regression polynomial to aid modeling with dense gridded data. Another suitable alternative namely multidimensional linear and cubic spline interpolation is explored as the fourth numerical modeling approach to solve some of the problems resulting from single polynomial approximation.

The next phase of modeling involves developing a macromodel combining already existing SPICE models of MOSFET (metal–oxide–semiconductor field-effect transistor) and JFET (junction-gate field-effect transistor). This model is easy to implement in circuit simulators and

provides good results compared to already demonstrated experimental works with innovative G^4FET circuits. The final phase of this work involves the development of a physics-based compact model of G^4FET with some empirical fitting parameters. A model for depletion-all-around operation is implemented in circuit simulator based on previous work. Another simplified model, combining MOS and JFET action, is implemented in circuit simulator to model the accumulation mode operation of G^4FET.

TABLE OF CONTENTS

Chapter 1 – Introduction 1

1.1 Motivation 1

1.2 Research Goal 5

1.3 Dissertation Overview 6

Chapter 2 - Literature Review 7

2.1 Previous Works on G^4FET 7

2.2 Previous Works on Numerical Modeling 10

2.3 Previous Works on Macromodels 13

2.4 Previous Works on Physics-based Compact Modeling 15

Chapter 3 - Device Structure and Operating Mechanism of G^4FET 21

3.1 Multiple Independent Gate Silicon-On-Insulator (SOI) Transistor 21

3.2 G^4FET Device Structure 23

3.3 Principle of Operation 24

3.4 Effect of Gate Bias on Conduction Path 26

3.5 Chapter Summary 29

Chapter 4 - Numerical Modeling of G^4FET 30

4.1 Overview 30

4.2 Numerical Method 1 (Multivariate Lagrange Interpolation Polynomial Model) 31

4.2.1 Model Formulation 31

4.2.2 Model Validation 34

4.2.2.1 An *n*-Channel G^4FET Simulated with TCAD Sentaurus (Device 1) 34

4.2.2.2 Experimental Data from an *n*-Channel G^4FET (Device 2) 37

4.2.2.3 A *p*-Channel G^4FET Simulated Using TCAD Sentaurus (Device 3) 39

4.2.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4) 42
4.2.2.5 Incorporation of Device Geometry 45
4.2.2.6 First Order Characteristics i.e. Transconductance and Drain Output Resistance 46
4.2.3 Implementation in Circuit Simulator *46*
4.2.4 Results from G^{4}FET Circuit Simulation *49*
4.3 Numerical Method 2 (Multidimensional Bernstein Polynomial Model) 52
4.3.1 Model Formulation *52*
4.3.2 Model Validation *53*
4.3.2.1 An *n*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 1) 53
4.3.2.2 Experimental Data from an *n*-Channel G^{4}FET (Device 2) 55
4.3.2.3 A *p*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 3) 57
4.3.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4) 58
4.3.2.5 Incorporation of Device Geometry 60
4.3.2.6 First Order Characteristics i.e. Transconductance and Drain Output Resistance 60
4.4 Numerical Method 3 (Multivariate Regression Polynomial Model) 63
4.4.1 Model Formulation *63*
4.4.2 Model Validation *65*
4.4.2.1 An *n*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 1) 65
4.4.2.2 Experimental Data from an *n*-Channel G^{4}FET (Device 2) 69
4.4.2.3 A *p*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 3) 72
4.4.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4) 76
4.4.2.5 Modeling of Device Geometry 79
4.4.2.6 First Order Characteristics (Device Transconductance and Drain Output Resistance) 81
4.4.3 Circuit Simulator (SPICE and Spectre^{TM}) Implementation *83*
4.4.4 Results from G^{4}FET Circuit Simulation *84*
4.5 Numerical method 4 (Multidimensional Linear and Cubic Spline Interpolation Model) 86
4.5.1 Model Formulation *87*
4.5.1.1 Linear Spline Model 87
4.5.1.2 Cubic Spline Model 88

4.5.2 Model Validation *89*

4.5.2.1 An *n*-Channel G⁴FET Simulated Using TCAD Sentaurus (Device 1) 89

4.5.2.2 Experimental Data from an *n*-Channel G⁴FET (Device 2) 91

4.5.2.3 A *p*-Channel G⁴FET Simulated with TCAD Sentaurus (Device 3) 93

4.5.2.4 Experimental Data from a *p*-Channel G⁴FET (Device 4) 95

4.5.2.5 Incorporation of Device Geometry 96

4.5.2.6 Validation of First Order Characteristics i.e. Device Transconductance and Output Drain Resistance 97

4.5.3 Implementation in Circuit Simulator *99*

4.5.4 Results from G⁴FET Circuit Simulation *100*

4.5.4.1 Negative Differential Resistance (NDR) LC oscillator: 100

4.5.4.2 High Voltage Differential Amplifier 101

4.5.4.3 Four-Quadrant Analog Multiplier: 102

4.6 Chapter Summary 109

Chapter 5 - Macromodel of G⁴FET 111

5.1 Motivation 111

5.2 Model Formation 111

5.3 CAD Implementation for Circuit Design 113

5.3.1 Negative Differential Resistance Circuit: *114*

5.3.2 Differential Amplifier: *115*

5.3.3 Four Quadrant Analog Multiplier : *116*

5.3.4 Multi-Threshold Inverter: *122*

5.3.5 Universal and Programmable Gate: *122*

5.3.6 Full Adder: *124*

5.4 Chapter Summary 127

Chapter 6 – Physics-Based Compact Model of G⁴FET 128

6.1 Motivation 128

6.2 Depletion All Around (DAA) Model 128

6.2.1 Model Formulation *129*

6.2.2 Model Validation *131*

6.3 Front Surface Accumulation Model 134

6.3.1 Model Formulation *135*

6.3.2 Model Validation *136*

6.4 Chapter Summary 139

Chapter 7 - Conclusion and Future Work 140

7.1 Original Contributions 140

7.2 Dissertation Summary 142

7.3 Future Works 143

References 145

Vita 160

LIST OF TABLES

Table 4.1: Geometry, Doping and Biasing for an *n*-Channel G^4FET 35

Table 4.2: Geometry, Doping and Biasing for a *p*-Channel G^4FET 40

Table 4.3: Computational Complexity of Lagrange Model 48

Table 4.4: Computational Complexity of Regression Model 83

Table 4.5: Comparison Between Experimental and Simulation Results for DC Transfer Characteristics of Configuration 1 106

Table 4.6: Comparison Between Experimental rand Simulation Results for DC Transfer Characteristics of Configuration 2 106

Table 5.1: Comparison Between Experimental and Simulation Results (Macromodel) for DC Transfer Characteristics of Analog Multiplier (Configuration 1) 119

Table 5.2: Comparison of Experimental and Simulation Results (Macromodel) for DC Transfer Characteristics of Analog Multiplier (Configuration 2) 119

Table 5.3: Truth Table of a Full Adder 126

LIST OF FIGURES

Figure 1.1: Moore's Law dictating transistor counts in microprocessor over the years [9]. 2

Figure 1.2: Change of direction in gate length scaling from 2013 to 2015 ITRS report [13]. 3

Figure 1.3: Possible alternatives for extending Moore's law 4

Figure 3.1: Three layers of SOI wafer. 21

Figure 3.2: Cross-sectional schematic of a fully depleted (FD) SOI device. 22

Figure 3.3: Cross-sectional schematic of a partially depleted (PD) SOI. 22

Figure 3.4: 3-D Schematic of a G^4FET structure. 25

Figure 3.5: G^4FET structure: (a) cross section and (b) top view. 25

Figure 3.6: Electron density in the top silicon film at V_{TG} = 0 V, V_{BG} = 0 V and V_{JG} = 0 V. 27

Figure 3.7: Electron density in the top silicon film at V_{TG} = -3 V, V_{BG} = 0 V and V_{JG} = 0 V. 27

Figure 3.8: Electron density in the top silicon film at V_{TG} = 0 V V_{BG} = -3 V V_{JG} = 0 V. 27

Figure 3.9: Electron density in the top silicon film at V_{TG} = -3 V, V_{BG} = -3 V and V_{JG} = 0 V 28

Figure 3.10: Electron density in the top silicon film at V_{TG} = 0 V, V_{BG} = 0 V and V_{JG} = -1 V 28

Figure 3.11: Electron density in the top silicon film at V_{TG} = 3 V, V_{BG} = 0 V and V_{JG} = 0 V. 28

Figure 3.12: Electron density in the top silicon film at V_{TG} = 3 V, V_{BG} = 10 V and V_{JG} = 0 V. ... 29

Figure 4.1: Drain current versus drain-source voltage from TCAD data and Lagrange model for different orders of V_{DS} for an *n*-channel G^4FET. 36

Figure 4.2: Relative errors between TCAD data and Lagrange model for different orders of V_{DS} for an *n*-channel G^4FET. 36

Figure 4.3: Isolines of test data and model for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment with order of V_{DS} fixed at 8. 37

Figure 4.4: Drain current versus top-gate voltage from experimental data and Lagrange model for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2). 38

Figure 4.5: Relative errors in model prediction for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2)..... 38

Figure 4.6: Comparison between isolines of test data and Lagrange model for different bottom-gate voltages ranging from -4 V to 4 V in 2 V increment with the model order for V_{TG} fixed at 7 (Device 2)..... 39

Figure 4.7: Drain current versus source-drain voltage from TCAD data and Lagrange model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3). 41

Figure 4.8: Relative errors between TCAD data and Lagrange model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3). 41

Figure 4.9: Drain current versus source-drain voltage for different junction-gate voltages ranging from 0 V to 4 V in 1 V increment and corresponding mean relative error (Device 3)..... 42

Figure 4.10: Comparison of I_D-V_{TG} between experimental data and Lagrange model for different orders of V_{TG} for a *p*-Channel G^{4}FET (Device 4). 43

Figure 4.11: Relative errors between experimental data and Lagrange model for different orders of V_{TG} for a *p*-Channel G^{4}FET (Device 4). 44

Figure 4.12: Comparison between isolines of test data and model (10^{th} order V_{TG}) for different junction-gate voltages ranging from 0.6 V to 1.8 V in 0.4 V increment arranged from top to bottom (Device 4). 44

Figure 4.13: Comparison of drain current versus drain-source voltage between TCAD data and Lagrange model of test geometry for different orders. 45

Figure 4.14: Relative errors between TCAD data and Lagrange model of test geometry for different orders. 46

Figure 4.15: Comparison of $g_m - V_{TG}$ between experimental data and Lagrange model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4). 47

Figure 4.16: Comparison of r_{out} - V_{DS} between TCAD data and Lagrange model for different orders of V_{DS} for an *n*-channel G^{4}FET (Device 1). 47

Figure 4.17: Behavioral model of an *n*-channel G^{4}FET. 49

Figure 4.18: (a) A conventional two-terminal JFET NDR device, (b) a four-terminal G^{4}FET NDR device. 50

Figure 4.19: A simplified symbol of G^{4}FET NDR. 50

Figure 4.20: An LC oscillator using G^4-NDR. 51

Figure 4.21: (a) Output from SPICE simulator (769 kHz signal with 2.47 $V_{p\text{-}p}$ amplitude), (b) experimental result (768 kHz with 2.5 $V_{p\text{-}p}$ amplitude). 51

Figure 4.22: Drain current versus drain-source voltage from TCAD data and Bernstein model for different orders of V_{DS} in an *n*-channel G^{4}FET (Device 1). 54

Figure 4.23: Relative errors between TCAD data and Bernstein model for different orders of V_{DS} for an *n*-channel G^{4}FET (Device 1). 55

Figure 4.24: Drain current versus top-gate voltage from experimental data and Bernstein model for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2). 56

Figure 4.25: Relative errors between experimental data and Bernstein model for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2). 56

Figure 4.26: Comparison of I_D-V_{SD} between TCAD data and Bernstein model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3). 57

Figure 4.27: Relative errors between TCAD data and Bernstein model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3). 58

Figure 4.28: Comparison of I_{SD}-V_{TG} between experimental data and Bernstein model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4). 59

Figure 4.29: Relative errors between experimental data and Bernstein model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4). 59

Figure 4.30: Drain current versus drain-source voltage from TCAD data and Bernstein model of different orders for test geometry. 61

Figure 4.31: Relative errors between TCAD data and Bernstein model for test geometry. 61

Figure 4.32: Transconductance versus top-gate voltage from experimental data and Bernstein model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4). 62

Figure 4.33: Output resistance versus drain-source voltage from TCAD data and Bernstein model for different orders of V_{DS} for an *n*-channel G^{4}FET (Device 1). 63

Figure 4.34: Comparison of I_{DS}-V_{DS} between TCAD data and regression model for different orders of V_{DS} with order of V_{BG} fixed at 3 for an *n*-channel G^{4}FET. 66

Figure 4.35: Relative error between TCAD data and regression model for different orders of V_{DS} with V_{BG} fixed at 3 for an *n*-channel G^{4}FET. 67

Figure 4.36: Comparison of I_{DS}-V_{DS} between TCAD data and regression model for different orders of V_{DS} with order of V_{BG} fixed at 4 for an *n*-channel G^{4}FET. 67

Figure 4.37: Relative error between TCAD data and regression model for different orders of V_{DS} with order of V_{BG} fixed at 4 for an *n*-channel G^{4}FET. 68

Figure 4.38: Comparison between isolines of test data and regression model (order of V_{DS}, V_{BG}, V_{TG}, V_{JG} respectively 10, 4, 5 and 5) for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment arranged from bottom to top. 68

Figure 4.39: Comparison of I_{DS}-V_{TG} between experimental data and regression model for different orders of V_{TG} with the order of V_{BG} and V_{JG} fixed at 2. 70

Figure 4.40: Relative error between experimental data and regression model for different orders of V_{TG} with the order of V_{BG} and V_{JG} fixed at 2. 70

Figure 4.41: Comparison of I_{DS} -V_{TG} between experimental data and regression model for different orders of V_{TG} with the order of V_{JG} and V_{BG} fixed at 2 and 4, respectively. 71

Figure 4.42: Relative error between experimental data and regression model for different orders of V_{TG} with the order of V_{JG} and V_{BG} fixed at 2 and 4, respectively. 71

Figure 4.43: Comparison between isolines of test data and regression model (order of V_{BG}, V_{TG}, V_{JG} respectively 3, 8 and 2) for different bottom-gate voltages ranging from -4 V to 4 V in 2 V increment arranged from bottom to top. 72

Figure 4.44: Comparison of I_{SD}-V_{SD} between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 4 for a *p*-channel G^4FET. 73

Figure 4.45: Relative error between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 4 for a *p*-channel G^4FET. 74

Figure 4.46: Comparison of I_{SD}-V_{DS} between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 5 for a *p*-channel G^4FET. 74

Figure 4.47: Relative error between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 5 for a *p*-channel G^4FET. 75

Figure 4.48: Comparison between isolines of test data and regression model for different junction-gate voltages ranging from 0 V to 4 V in 1 V increment (Device 3). 75
Figure 4.49: Comparison of I_{SD}-V_{TG} between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 3. 77
Figure 4.50: Relative error between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 3. 77
Figure 4.51: Comparison of I_{SD}-V_{TG} between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 6. 78
Figure 4.52: Relative error between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 6. 78
Figure 4.53: Comparison between isolines of test data and regression model for different junction-gate voltages ranging from 0.2 V to 1.4 V in 0.4 V increment (Device 4). 79
Figure 4.54: Comparison of drain current versus drain-source voltage between TCAD data and regression model for different orders of V_{DS} for test geometry. 80
Figure 4.55: Relative errors between TCAD data and regression model for different orders of V_{DS} for test geometry. 80
Figure 4.56: Comparison between TCAD data and regression model of isolines for different widths ranging from 0.3 to 0.5 µm in .05 µm increment arranged from bottom to top. 81
Figure 4.57: Comparison of g_m–V_{TG} between experimental data and regression model for different orders of V_{TG} and V_{JG} for a p-channel G^{4}FET (Device 4). 82
Figure 4.58: Comparison of r_{out} - V_{DS} between TCAD data and regression model for different orders of V_{DS} and V_{BG} for an n-channel G^{4}FET (Device 1). 82
Figure 4.59: (a) Output from SPICE simulator, (b) experimental result. 84

Figure 4.60: Schematic of high voltage G^4FET differential amplifier (Q 1,2: 0.3 µm ×10/2.4 µm, V_{JG} = 0 V, V_{BG} =0 V; Q 3,4: 0.35 µm ×2 /10 µm, V_{JG} = 0 V, V_{BG} = 0 V; Q 5,6: 0.3 µm×10/2.4 µm, V_{JG} =V_{DD}, V_{BG} = 0 V). 85

Figure 4.61: Output of G^4FET Differential amplifier (0.97 V_{p-p} compared to experimental value of 1 V_{p-p}) in non-inverting unity gain configuration (V_{DD} = 10 V, V_{in} = 1 V_{p-p} square wave with 6 V offset). 86

Figure 4.62: Comparison between isolines of test data and linear spline model (Device 1) for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment. 90

Figure 4.63: Comparison between isolines of test data and cubic spline model (Device 1) for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment. 91

Figure 4.64: Comparison between isolines of test data and linear spline model (Device 2) and relative error for varying bottom-gate voltages from -4V to 4V in 2V increment arranged from bottom to top. 92

Figure 4.65: Comparison between isolines of test data and cubic spline model (Device 2) and relative error for varying bottom-gate voltages from -4 V to 4 V in 2 V increment arranged from bottom to top. 93

Figure 4.66: Comparison of I_{SD} - V_{SD} between TCAD test data and linear spline model (Device 3) for different junction-gate voltages ranging from 0 V to 4 V. 94

Figure 4.67: Comparison of I_{SD} - V_{SD} between TCAD test data and cubic spline model (Device 3) for different junction-gate voltages ranging from 0 V to 4 V. 94

Figure 4.68: Comparison between test data and linear spline model isolines (Device 4) for variation in junction-gate voltages from 0.2 V to 1.8 V in 0.4 V increment arranged from top to bottom. 95

Figure 4.69: Comparison between test data and cubic spline model isolines (Device 4) for variation in junction-gate voltages from 0.2 V to 1.8 V in 0.4 V increment arranged from top to bottom. 96

Figure 4.70: Comparison between TCAD data and cubic spline model of isolines for different widths ranging from 0.3 to 0.5 μm in .05 μm increment arranged from bottom to top..... 97

Figure 4.71: Comparison of $g_m - V_{TG}$ between TCAD data and cubic spline model for an *n*-channel G^{4}FET (Device 1). 98

Figure 4.72: Comparison of $r_{out} - V_{DS}$ between TCAD data and cubic spline model for an *n*-channel G^{4}FET (Device 1). 98

Figure 4.73: Behavioral model of an *n*-channel G^{4}FET for spline interpolation..... 99

Figure 4.74(a) Output from circuit simulator (b) Experimental result. 100

Figure 4.75: Output of amplifier (1.03 $V_{p\text{-}p}$ compared to experimental value of 1 $V_{p\text{-}p}$) in non-inverting unity gain configuration (V_{DD} = 10 V, V_{in} = 1 $V_{p\text{-}p}$ square wave with 6 V offset). 101

Figure 4.76: Configuration 1 of analog multiplier using G^{4}FET. 103

Figure 4.77: Configuration 2 of analog multiplier using G^{4}FET. 103

Figure 4.78: DC transfer characteristics for configuration 1 (W = 0.35 μm, L = 10 μm, V_{DD} = 10 V, I_{bias} = 15 μA, V_{bias1} = 1.7 V, V_{bias2} = -1.8 V, R_L = 500 kΩ); (a) measurement results reproduced from [37], (b) simulation results using cubic spline model. 104

Figure 4.79: DC transfer characteristics for configuration 2 (W = 0.35 μm, L = 5 μm, V_{DD} = 5 V, I_{bias} = 10 μA, V_{bias1} = 0 V, V_{bias2} = -3 V, R_L = 500 kΩ); (a) measurement results reproduced from [37], (b) simulation results using cubic spline model. 105

Figure 4.80: Product of a 20 Hz, 1 V_{p-p} sinusoidal-wave with 500 Hz, 1 V_{p-p} square-wave (W = 0.3 µm x 10, L = 2.4 µm, V_{DD} = 3.5 V, V_{SS} = -3.5 V, I_{bias} = 35 µA, V_{bias1} = 2 V, V_{bias2} = -2.5 V, R_L = 100 kΩ); (a) measurement results, (b) simulation results using cubic spline model. 107

Figure 4.81: Product of a 10 Hz, 4 V_{p-p} triangular-wave with 200 Hz, 4 V_{p-p} square-wave (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 15 µA, V_{bias1} = 0 V, V_{bias2} = -3.5 V, R_L = 200 kΩ); (a) measurement results, (b) simulation results using cubic spline model. 108

Figure 5.1: Output of NDR LC oscillator; (a) measurement result, (b) simulation result. 114

Figure 5.2: Amplitude Modulated(AM) signal; (a) measurement result, (b) simulation result.. 115

Figure 5.3: High voltage differential amplifier output from the macromodel simulation. 116

Figure 5.4: DC transfer characteristics for configuration 1 (W = 0.35 µm, L = 10 µm, V_{DD} = 10 V, I_{bias} = 15 µA, V_{bias1} = 1.7 V, V_{bias2} = -1.8 V, R_L = 500 kΩ); (a) measurement results reproduced from [7], (b) simulation results using the macromodel. 117

Figure 5.5: DC transfer characteristics for configuration 2 (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 10 µA, V_{bias1} = 0 V, V_{bias2} = -3 V, R_L = 500 kΩ); (a) measurement results reproduced from [7], (b) simulation results using the macromodel. 118

Figure 5.6: Product of a 20 Hz, 1 V_{p-p} sinusoidal-wave with 500 Hz, 1V_{p-p} square-wave (W = 0.3 µm x 10, L = 2.4 µm, V_{DD} = 3.5 V, V_{SS} = -3.5 V, I_{bias} = 35 µA, V_{bias1} = 2 V, V_{bias2} = -2.5 V, R_L = 100 kΩ); (a) measurement results, (b) simulation results using the macromodel. 120

Figure 5.7: Product of a 10 Hz, 4 V_{p-p} triangular-wave with 200 Hz, 4 V_{p-p} square-wave (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 15 µA, V_{bias1} = 0 V, V_{bias2} = -3.5 V, R_L = 200 kΩ); (a) measurement results, (b) simulation results using the macromodel. 121

Figure 5.8: Schematic of a multi-threshold Inverter. 123

Figure 5.9: Output of a multi-threshold inverter. 123

Figure 5.10: Symbol of a G^4FET programmable gate. 124
Figure 5.11: Output of a programmable gate. 125
Figure 5.12: Schematic of the G^4FET full adder. 125
Figure 5.13: Output from the full adder. 126
Figure 6.1: Schematic of the cross-section of a G^4FET in depletion all around operation..... 129
Figure 6.2: Comparison between test data and model for different junction-gate voltages, with both the top-gate and the bottom-gate biased at 0 V. 132
Figure 6.3: Comparison between test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 0 V and -3 V, respectively. 132
Figure 6.4: Comparison between test data and model for different top-gate voltages, with the junction-gate and the bottom-gate biased at 0 V and -3 V, respectively. 133
Figure 6.5: Comparison between test data and model for different top-gate voltages, with the junction-gate and the bottom-gate biased at -1.5 V and -3 V respectively. 133
Figure 6.6: Comparison between test data and model for different bottom-gate voltages, with both the junction-gate and the top-gate biased at 0 V. 134
Figure 6.7: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 2.5 V and 0 V, respectively. 137
Figure 6.8: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 3 V and 0 V, respectively. 137
Figure 6.9: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 3.5 V and 0 V, respectively. 138
Figure 6.10: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 4 V and 0 V, respectively. 138

Figure 6.11: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 4.5 V and 0 V, respectively. 139

Chapter 1 – Introduction

1.1 Motivation

Transistor is the key active component in practically all modern electronics and it is considered as one of the greatest technological inventions of the 20th century [1]. The ability to be mass-produced using a highly automated process resulting in a very low per-transistor cost has cemented its supreme role in the modern world. The invention of the first transistor at Bell Laboratories was named an IEEE Milestone in 2009 [2]. Although the first patent of a field-effect transistor was filed in 1926 [3], the real world transistor revolution actually started with the invention of bipolar junction transistor in 1948 which revolutionized the field of electronics by a rapid replacement of vacuum tubes as active elements in electronic devices. In contrast to the bulky, unreliable and excessive power consuming electronic circuits made with vacuum tubes, transistors provided a low-power, lightweight, faster and reliable alternative. Although over a billion discrete transistors are produced every year [4], the vast majority of transistors are now produced in integrated circuits introduced in 1958 independently by Jack St. Clair Kilby [5] and Robert Norton Noyce [6]. The amazing technological advancements in the semiconductor industries have been dictated by the desire to achieve Moore's law [7]. In 1965, Gordon Moore stated that the number of transistors in integrated circuit (IC) would double every year which he later, in 1975, revised as a doubling in every two years. Moore's law has been the main driving factor during the last 50 years for the enhancement of device performances primarily through smaller feature size and larger chips. The cost per transistor and the switching power

consumption per transistor went down, while the memory capacity and speed went up. Over the years, transistor sizes have decreased from tens of microns in the early 1970s to 10 nanometers in 2017 [8] with a corresponding million-fold increase in transistors per unit area as shown in Figure 1.1. The vast majority of applications now has bulk silicon device as the active element in VLSI (very large scale integration) and ULSI (ultra large scale integration) circuits.

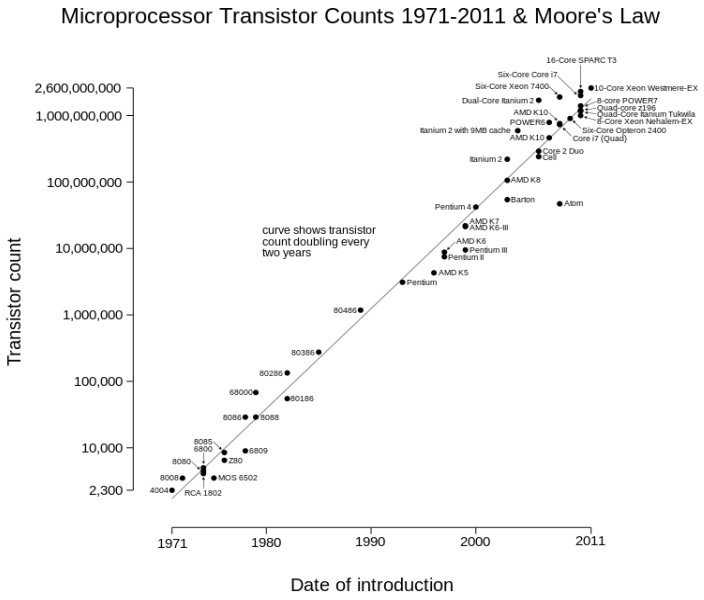


Figure 1.1: Moore's Law dictating transistor counts in microprocessor over the years [9].

However, bulk silicon devices are now faced with some fundamental physical limits. Some of the non-idealities such as subthreshold conduction, gate oxide leakage and reverse-biased junction leakage can no longer be ignored since they can potentially consume more than half of the total power in modern high-performance VLSI chips [10]. The increase in doping concentration has reduced carrier mobility due to impurity scattering resulting in transconductance degradation. With the increased proximity of drain and source electrodes, drain has started to play

a vital role in channel formation causing the threshold voltage roll-off due to DIBL (drain induced barrier lowering) and a decrease in output resistance affecting analog circuit design. The scaling of switching time has slowed down since the interconnect capacitance has started to become a larger portion of total capacitance. With the very thin gate oxide of today, the leakage from quantum mechanical tunneling is increasing the power consumption and adversely affecting transistor operation. These problems are making conventional scaling less feasible as can be observed from the change of direction in ITRS road map from 2013 to 2015 in Figure 1.2.

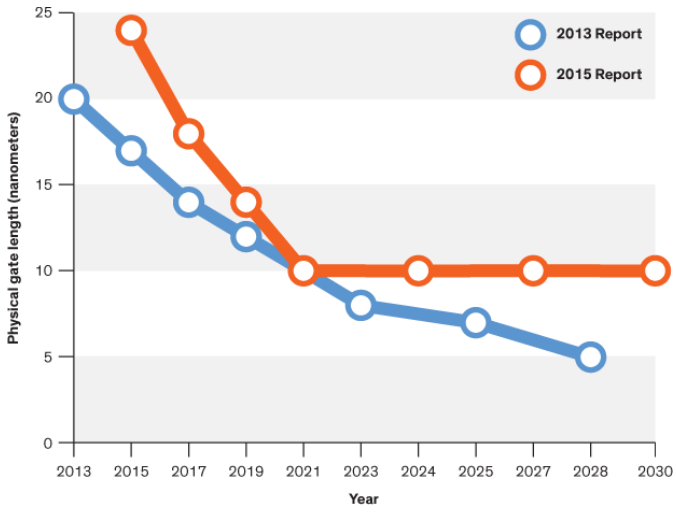


Figure 1.2: Change of direction in gate length scaling from 2013 to 2015 ITRS report [13].

Researchers have been looking for new process technologies which can solve the problems associated with bulk silicon scaling and enable the semiconductor industry to extend Moore's law in the foreseeable future as shown in Figure 1.3. A promising candidate is silicon-on-insulator (SOI) technology with its long list of reported advantages[11]. It has a lower parasitic capacitance due to isolation from the bulk silicon resulting in lower power consumption at matched performance. SOI transistors have shown reduced short channel effect, better subthreshold swing

and the ability to handle higher voltage and higher temperature, compared to bulk CMOS [12]. Lower leakage currents due to isolation increases the power efficiency. It has a lower temperature dependence and is suitable for radiation hardened application with the need for reduced redundancy. It prevents latch-up by the complete isolation of the *n*- and *p*-well structures and enables implementation with a smaller chip area. Major companies, including IBM, AMD and Freescale, began manufacturing microprocessors using SOI substrates in the early 2000's heralding its entrance into the mainstream semiconductor industry.

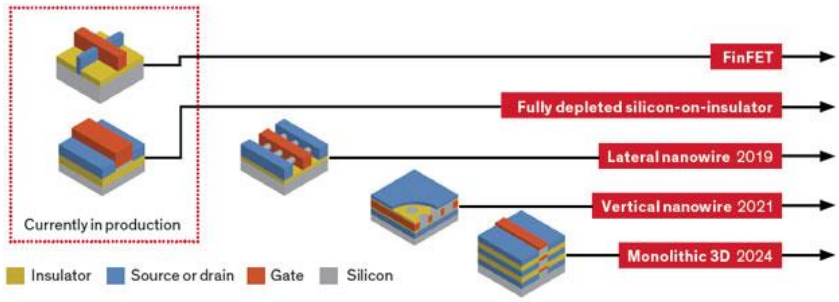


Figure 1.3: Possible alternatives for extending Moore's law [13].

In SOI technology, each transistor can have more than one gate. Experiments with different variations in gate configuration have been done and have resulted in a wide array of multi-gate transistors [14] such as wrapped-gate transistor, "double-gate transistor, "FinFET, 'tri(ple)-gate transistors', 'gate-all-around transistors' etc. However, the number of independent gates can be extended to four in SOI technology and it was named MOSJFET [15] or four gate field effect transistor (G^4FET) [16] . G^4FET retains the advantages of SOI technology and offers exciting new opportunities for analog and mixed-signal applications, quaternary logic functions and electrostatically formed nanowire with superior conduction properties.

The widespread use of a technology in circuit design is heavily dependent upon good SPICE models for CAD tools which are now ubiquitous in circuit design. Sophisticated models for existing transistors integrated with CAD tools have enabled designers worldwide to design excellent circuits which are in a large part responsible for the technology boom of the last 50 years. Since G^4FET is a relatively new technology, a fast, robust and accurate SPICE model is absolutely necessary for aiding circuit designers to transform G^4FET into a mainstream technology.

1.2 Research Goal

The goal of this research effort is to develop robust, accurate and efficient SPICE model for G^4FET and implement it as a circuit building block in commercial simulators. The existence of four independent gates makes this modeling work particularly challenging.

In this work, four different numerical models have been developed and implemented in commercial circuit simulator, each with its own pros and cons. The results have been compared with both TCAD Sentaurus from Synopsys® and with experimental results. In addition, a macromodel is developed combining already existing SPICE models of MOSFET and JFET. Moreover, two physics-based compact modeling approaches have also been adopted to model particularly useful conduction mechanisms.

The research goal can be summarized as developing the following models:

1. Development and CAD implementation of four numerical models:
    A. Multivariate Lagrange interpolation polynomial model,
    B. Multidimensional Bernstein polynomial model,
    C. Multivariate regression polynomial model,

D. Multidimensional spline interpolation model.

2. Development of a macromodel combining existing JFET and MOSFET models.
3. Development of a physics-based compact model.

1.3 Dissertation Overview

This dissertation is divided into seven chapters. The limitation of bulk-CMOS technology and the need for multi-gate SOI technology are explained in Chapter 1. The evolution of G^4FET and the necessity of suitable SPICE models are also discussed in Chapter 1. Previous analytical and modeling works on G^4FET and other transistors are discussed in Chapter 2. The device structure and operating mechanism of G^4FET are discussed in Chapter 3. The methodology and results of four numerical modeling approaches (Lagrange, Bernstein, Regression and Spline) are discussed in Chapter 4. The macromodel of G^4FET combining existing transistor models is explored in Chapter 5. Two physics-based modeling approaches for SPICE implantation are discussed in Chapter 6. Conclusions and future works are summarized in Chapter 7.

Chapter 2 - Literature Review

2.1 Previous Works on G^{4}FET

G^{4}FET, a relatively new member in the SOI multi-gate device family, was first reported in 2002 [15]. This unique SOI transistor combines MOSFET and JFET transistor actions in a single silicon body. Due to this combination of MOSFET and JFET functionality, this transistor was called a MOSJFET [15]. It was also named G^{4}FET [16] since it has four independent functional gates.

Extraction methods for threshold voltage, mobility and subthreshold swing in the linear region were demonstrated in [17]. The experimental results from a partially-depleted (PD)-SOI G^{4}FET showed the dependence of these parameters on different gate biases. In addition to the experimental results, numerical simulation is important for understanding the several conduction mechanisms inside the transistor and 3-D simulations were performed to shed light on the role of multiple gates [18]. A non-uniform doping profile was used to reproduce the channel characteristics of fabricated devices.

In [19], various operation modes of G^{4}FETs were analyzed based on measured current-voltage, transconductance and threshold characteristics. The optimization of important device parameters such as threshold voltage, subthreshold swing, mobility using particular combination of gate biasing was also shown. Volume and interface conduction mechanism were clarified using numerical simulation. The unique ability of switching using any of its four independent gates was also discussed.

The charge coupling between front, back and lateral junction-gates was considered and a 2-D analytical relationship for the fully-depleted body potential was derived in [20]. This work was extended in [21] and a closed form front-interface threshold voltage expression was derived as a function of the back and the lateral gate voltages for different back interface conditions such as accumulation, depletion and inversion.

The subthreshold operating region of G^4FET was explored in [22] and it showed better subthreshold swing compared to conventional bulk MOSFET. There is a flexibility of adjusting the subthreshold slope of MOS gates or junction-gates using the remaining gate biases.

A very interesting application of G^4FET is the formation of quantum wire. The quantum wire can be electrostatically formed when the conducting channel is surrounded by depletion regions induced by vertical MOS and lateral JFET gates [23]. In this unique conduction mechanism named depletion-all-around (DAA), majority carriers flow in the volume of the silicon film far from the silicon/oxide interfaces. The control of lateral gates on the conduction channel can be adjusted by changing biases on the vertical gates. There is a reduced sensitivity of the channel to the oxide and interface defects, low subthreshold swing, high g_m/I_D ratio, high mobility, low noise, and high immunity to ionizing radiation [24].

The fully-depleted version of the G^4FET was introduced and its characteristics were systematically investigated in [25]. This work demonstrates that the thinning-down of the silicon film enhances vertical coupling between the front and the back gates and reduces the horizontal coupling between the lateral gates. As a consequence, the direct influence of the lateral junction-gates on the body potential distribution is reduced.

The operation and performance of G^4FET was presented from the low voltage to the high voltage regime [26]. Devices fabricated in 0.35 μm 3.3 V partially-depleted SOI process are shown

to have a breakdown voltage of 15 V, excellent subthreshold swing, and high mobility. Low-frequency noise characteristics of G^4FET were reported in [27]. A comparison of noise power spectral density between surface and volume conduction was presented and its dependence on biasing conditions was explored. A charge sheet model has been recently proposed to analyze the transistor characteristics of fully-depleted G^4FETs [28]. Here, surface accumulation behavior, drain current and gate capacitance of fully-depleted G^4FET are modeled analytically.

In [29], a mathematical model is developed to determine the subthreshold swing of thin-film fully-depleted G^4FET. A mathematical model of potential distribution has been derived considering three dimensions of a fully-depleted *p*-channel G^4FET in [30]. A physics-based mathematical model is proposed in [31] to determine the accumulation layer thickness in thin film fully depleted G^4FETs. Another mathematical model is developed in [32] to determine the 3-D potential distribution of a fully-depleted G^4FET. Based on the exact solution of the Poisson equation, a new two-dimensional model of potential and threshold voltage for the fully-depleted G^4FET was developed in [33].

Several innovative analog and digital circuit applications of G^4FET have been reported over the years. A complementary pair of G^4FETs can exhibit negative differential resistance (NDR) due to the JFET functionality of its lateral gates. LC oscillator and Schmitt trigger circuits were experimentally demonstrated using G^4FET NDR device [34].

G^4FETs can operate under higher voltages compared to bulk silicon MOSFET counterparts using the same process technology. High voltage current mirror and differential amplifier based on G^4FET were experimentally demonstrated in [35].

The four gates of G^4FETs can be utilized to make innovative circuits with reduced transistor count. A novel four quadrant analog multiplier topology was demonstrated in [36] with

only four transistors at its core. Two different configurations, using different combination of gate inputs are shown. A G^4FET based temperature-compensated voltage reference circuit, without the use of the standard bandgap architecture, was demonstrated using standard 3.3 V/ 0.35 μm partially-depleted PD-SOI process [37].

In the arena of digital circuits, the independent multi-gate functionality helps reduce the transistor count per logic function and enhances design flexibility. Novel G^4FET based logic-circuits such as adjustable-threshold inverter, real-time reconfigurable logic gates and DRAM cell were experimentally demonstrated [38]. In [39], the G^4FET was demonstrated as a universal and programmable logic gate that can lead to the design of more efficient logic circuits. A new full adder design based on the G^4FET utilizing only three transistors and two inverters is proposed.

The operation of the G^4FET can be interpreted as a complex four-input switching process and can be used for the computation of multiple-input threshold logic functions using a single device. Leveraging these unique capabilities a novel threshold logic family capable of efficient computation of complex logic functions was reported recently [40].

2.2 Previous Works on Numerical Modeling

Numerical models offer an alternative to the physics-based analytical models for rapid, accurate device modeling. The approach is to develop a methodology which takes measured or simulated data as input and then based on these empirical results, accurately reproduces the complex nonlinear behavior of the semiconductor devices. In most cases, they are equally applicable to different types of transistors such as MOSFET, MESFET, HEMT, DGFET etc. fabricated using various process technologies.

The most commonly used methods utilize look-up table and quadratic or higher order polynomials for interpolation between data points. The authors in [41] use a table-based approach for the empirical modeling of FETs in circuit simulators to address the specific requirements of analog circuit design, such as accuracy in reproducing small-signal parameters, large signal nonlinearities, subthreshold characteristics, substrate effects, short-channel effects, and voltage dependent capacitances. A table lookup model for MOSFETs consisting of a main table and a coarse 3-D sub-table to incorporate substrate effects. and a table to interpolate between channel length was implemented in SPICE 3 to overcome the inadequacies of analytical models in representing short channel effects [42].

An approach to dynamic MOSFET modeling, which is especially suited for the simulation of low-voltage mixed signal circuits was reported [43]. The model is based on the interpolation of terminal charges and conductive currents with physically motivated functions such as piecewise polynomial and/or exponential splines based on transient current/voltage data obtained through measurement or simulation of the devices.

A general *n*-dimensional first order continuous table model was proposed in [44]. Each table model was shown to reproduce the exact behavior of the DC current expressions of two basic physical device models; the Ebers-Moll bipolar transistor model and the GLASMOST MOSFET model with high accuracy and less evaluation times than advanced physical CAD device models.

Authors in [45] developed simple interpolation methods to construct any current table from a small basis set of tables for variation of width, length and temperature. Quadratic B-splines with not-a-knot boundary conditions were used for length and temperature interpolation, whereas simple scaling along with decomposition of channel was done for width variation to take narrow width non-idealities into consideration.

The table lookup approach was first applied for simulation of digital circuits in the timing simulator MOTIS [46], which has been developed at Bell Laboratories in 1975. The timing simulator provides timing information on the propagation of signals through MOS digital circuits.

A blending function combining exponential and polynomial interpolation for the accurate evaluation of the MOSFET drain current in the transition region between weak and strong inversions was implemented in [47]. This model offers several interpolation methods in the table model providing the model user with a flexibility to choose based on the required simulation speed, memory consumption and accuracy. Implementation of the model in circuit simulation showed good results in DC, transient, and AC analyses.

Table data has also been used to model devices for RF simulation [48]. In this model, the device characteristics of GaAs FET devices are determined by state functions which define nonlinear relationships for the 3-terminal lumped elements. An array of s-parameters, measured over a wide range gate and drain biases, is used to determine these state functions. Good prediction of high-order harmonics has made this model suitable for RF simulations.

In [49], this Bernstein approximation technique is extended to multidimensional variation diminishing interpolation and applied to DC current and intrinsic charge modeling of the MOSFET to increase simulation efficiency. Information about device operating point is extracted by functional reconstruction from stored data during transient simulation. The formulation of the numerical model preserves continuity and monotonicity facilitating the convergence in Newton-Raphson algorithm for solving the differential circuit equations.

Monotonic Piecewise Cubic Interpolation was used in [50] to determine the MOSFET operating point using stored table value generated by a 2-D device simulator. In [51], the quadratic fits were used to model triode region whereas linear fits were used for the saturation region.

However, it resulted in a discontinuity in the device conductance during the transition from triode to saturation region.

Authors in [52] used a tableau-style spline formulation using quadratic splines ensuring continuity of the function and its derivative and presented a new data-compression scheme for polynomial spline coefficient storage. The splines were optimized to reduce the number of segments and preserve the monotonicity of the model equations.

A three dimensional table lookup MOSFET model was presented in [53] showing good accuracy and short computation time. A conversion table was adopted for logarithmic operation to capture the weak inversion effect with log-linear characteristics. In another work on table method [54], a methodology of generating compact and accurate first order table model for highly nonlinear multidimensional behavior was demonstrated.

2.3 Previous Works on Macromodels

The number of elements in today's integrated circuit can range from several dozens to hundreds of millions. If each individual element is modeled separately, the simulation run time will be prohibitively long. Macromodels are used to simplify circuits in a way so that the desired behavioral characteristics remain the same for all practical purposes while the computational time gets substantially reduced.

Important circuit blocks like operational amplifiers and comparators are usually employed in simulators using their macromodels. The need for macromodel in IC subsystem design is discussed in [55]. The authors in [56] developed a macromodel for integrated circuit (IC) operational amplifiers (op amp) with an excellent pin-for-pin representation. The model uses

common elements available in most circuit simulators. This macromodel is a factor of more than six times less complex, an order of magnitude faster and less costly compared to op amp models at the electronic device level.

Logic simulation and macromodels have also been developed for digital logic blocks ([57], [58]). A behavioral multiport macromodel for the input buffers of digital integrated circuits is presented in [59] which offers comparable accuracy and improved efficiency compared to the transistor-level models. A macromodel for integrated-circuit comparators, capable of providing up to an order of magnitude reduction in CPU time and matrix size for CAD, was reported in [60].

A lumped parameter macromodel was derived from transistor characterization data to use in SPICE analyses for predicting the single-event upset thresholds for Texas Instruments SIMOX(Separation by IMplantation of OXygen) SOI SRAMs [61].

Physico-chemical model of the ISFET (ion-sensitive field-effect transistor) was developed in [62] using a behavioral macromodel that can be used in commercial SPICE programs. The proposed macromodel was shown to operate satisfactorily even under subthreshold conditions. The main goal was to get rid of the drawbacks associated with developing built-in models such as the availability of the program source, a deep knowledge of the code subroutines and structure, and the requirement of compiling the entire program for a new model implementation.

An empirical macromodel for a *p*-channel floating-gate MOS synapse transistor simulation consisting of a transistor and controlled sources was proposed in [63]. The model did not use the channel potential in its description enabling its application in any SPICE circuit simulator.

In [64], an improved SPICE macro-model for the LDMOS (laterally diffused MOS) device was proposed with better performance compared to existing BSIM3 models in both DC and AC regions. Verilog-A modules consisting of standard elements make this model simulator

independent. The model used an adapted JFET to model the drift region resistance and shorted PMOS transistors for modeling the capacitance behavior of the drift region. SPICE macro-modeling techniques have also been used in [65] for the compact simulation of single electron circuits.

2.4 Previous Works on Physics-based Compact Modeling

A number of works have been performed over the years on physics-based modeling of transistors. Gummel in [66] developed a model based on finite difference method for solving the model equations to provide information about internal parameters such as potential and electric field distribution along with terminal characteristics. This approach was modified in [67] using a new discretization technique for ensuring convergence. Building upon Scharfetter-Gummel algorithm, Slotboom [68] proposed a new model using two new artificial variables for linearization of the differential equations facilitating implementation in CAD programs.

Early pioneers Pao and Sah came up with the classic double integral drain current expression and explored different characteristics of the transistor action [69, 70]. However, these formulas are computation intensive and CAD implementation required a simplified model. Brews in [71] proposed a charge sheet model which compresses the inversion layer into a conducting plane of zero thickness.

With the scaling down of MOSFET, it gradually became apparent that in addition to linear and saturation regions, a third region of operation, namely, subthreshold conduction could no longer be ignored especially for low-leakage circuits. The subthreshold region is usually defined as the intermediate region between weak and strong inversion, where weak inversion starts when

the minority and the majority carrier concentrations at the surface are equal and the onset of strong inversion, typically known as threshold, occurs when the minority carrier concentration at the surface is equal to the majority carrier concentration in the bulk semiconductor. In [72], authors reconsidered the basic charge relationships to give a new formulation of the theory of the device for model characterization in a more general manner, and with greater accuracy than previously achieved. The contribution of the mobile channel charge to the silicon surface potential was taken into account and the model covered from sub-threshold to strong inversion conduction.

In [73], the effect of drain voltage on the subthreshold operation as the channel length becomes shorter, the effect of substrate bias on both the shift in and the slope of the subthreshold curves, and the effect of temperature on the subthreshold current characteristics are discussed and incorporated into a one-dimensional model. In [74], the dependence of channel current in subthreshold operation upon drain, gate, and substrate voltages is formulated in another model. It also points out the fact that two-dimensional effects can cause dramatic increases in the drain conductance. In [75], an analytical model was presented for unifying the existing models for both short and long channel MOSFETs.

Methods and results of a three-dimensional numerical model of small geometry MOSFETs were reported in [76]. The necessity of three-dimensional simulation as opposed to two-dimensional calculations is discussed and size effects in short and narrow channel enhancement and depletion FETs are analyzed. In [77], two-dimensional simulations were used to determine the relationship between the drain-induced barrier lowering and the punchthrough and a quasi one-dimensional Poisson equation was solved to find the onset voltage of the punchthrough . Also, a semi-empirical model, MOS3, was developed and installed into the circuit simulation program SPICE2.G.

Initially MOSFETs were not the first choice for analog circuit design. However, during the 70's, improved noise performance, device matching, and frequency response have resulted in analog MOSFET circuits with performance comparable to or better than that of bipolar counterparts. This required a better small signal model for CAD implementation and the authors in [78] presented a first-order and a second-order large signal MOSFET models and derived corresponding small signal models. The small-signal model parameters are related to operating-point bias and the IC process used to fabricate the devices.

The SPICE2 program provided three built-in MOS transistor models, known as the first generation models [79]. The first one is the Level-1 model with its fairly simple expressions similar to the often used square law current equation and is suitable for preliminary analysis. This is mostly based on the works of Shichman and Hodges [80].The Level-2 model dived deeper into detailed device physics but still had some problems with small geometry transistors and convergence issues. The Level-3 model was an attempt to merge physics-based approach with empirical parameter fitting and started the semi-empirical modeling approach for reproducing device characteristics. The authors in [81] developed the now famous 'Berkeley Short-channel IGFET Model (BSIM)' based upon AT&T Bell Laboratories' CSIM (Compact Short-channel IGFET Model) with substantial enhancements [82]. This was the beginning of the second generation of SPICE models.

Among the factors influencing conduction, mobility and recombination-generation need to modeled appropriately for faithful reproduction of experimental data. The dependence of carrier mobility on electric field, temperature and doping density has been analyzed by different authors. In [83], Canali et al. presented experimental data for electron and hole drift velocity in silicon for

high electric fields up to 6×10^4 V/cm and wide temperature range from 300 to 430 K and proposed an analytical expression based on curve fitting to describe the experimental data. An analytical expression of electron and hole mobilities in silicon based on experimental data was reported in [84] which is valid for wide range of temperature and doping concentration.

A concentration dependent mobility expression for different dopant materials such as boron, phosphorus and arsenic in silicon was proposed in [85]. A unified model known as 'University of Bologna mobility model' was proposed by Reggiani [86, 87] incorporating dependences on doping, temperature and electric field.

The carrier generation and recombination depend on temperature and carrier density. Hall [88] and Shockley-Read [89] independently established a universal expression for carrier-recombination and generation. The dependence of carrier lifetime, the most important parameter for determining the rate of recombination-generation, on temperature and electric field was analyzed in [90].

With the advent of silicon-on-insulator (SOI), new compact models exploring different flavors of this new technology were reported. In [91], a physics-based SPICE model called BSIMPD is developed for application of partially-depleted SOI technologies in deep-submicron CMOS designs. The model was developed on top of the industry-standard bulk-MOSFET model BSIM3v3 ensuring scalability and robustness while capturing SOI-specific dynamic behaviors such as built-in floating body, self-heating and body-contact models.

Depending on dimension and bias, SOI MOSFET may operate in different modes i.e. body-contacted mode, partially depleted mode and fully depleted mode. A model has to incorporate a smooth transition between the modes of operation. The authors in [92] describe a unified framework to model the floating-body effects of various SOI MOSFET operation modes.

A surface-potential based multi-gate FET (MG-FET) compact model called BSIM-MG was reported in [93] for mixed-signal design applications. This model included effect of finite body doping on the electrical behavior of MGFETs and used a field penetration length model for short channel effects. It also included several physical effects such as poly-depletion effect and quantum-mechanical effect (QME). The continuity of terminal currents and charges was ensured for mixed-signal design. The authors also reported a similar BSIMIMG model for independent multi-gate operation in [94].

A process/physics-based compact model for non-classical MOSFETs having ultra-thin Si bodies (UTB) is discussed in [95]. The discussed model is essentially a compact Poisson–Schrodinger solver, including short-channel effects, and can be used for modeling nanoscale FD-SOI MOSFETs and generic double-gate (DG) devices.

An analytic potential compact model was developed for symmetric DG MOSFETs without the charge sheet approximation to account for the "volume inversion" [96, 97]. A similar model has been developed for surrounding-gate (SG) MOSFETs [98]. Based on these works, a unified analytic drain–current model is presented for various kinds of multiple-gate (MG) MOSFETs, including quadruple-gate (QG), triple-gate (TG), Π-gate, and Ω-gate MOSFETs in [99].

Recently, surface potential based modeling, namely SP and PSP models have gained prominence for accurate modeling of scaled down transistors. In [100], a symmetric linearization method was reported for developing a core compact model of certain multiple-gate transistors without charge-sheet approximation resulting in a form very similar to a standard PSP MOSFET model.

Authors in [101] reported a surface potential based approach for modeling partially-depleted (PD) SOI MOSFET. This model retains the physics-based formulation and scalability of

standard PSP while capturing SOI specific effects by including floating body simulation capability, parasitic body currents and capacitances. It also included a body resistance for accurate characterization and simulation of body-contacted SOI devices. A complete surface-potential-based compact model of dynamically depleted (DD) SOI MOSFETs was presented in [102].

EKV(Enz Krummenacher Vittoz) approach of device modeling [103] has also become popular over the years, especially for analog circuit design. In [104], a design oriented charge-based model based on EKV formalism for undoped DG MOSFETs under symmetrical operation was presented.

Chapter 3 - Device Structure and Operating Mechanism of G^4FET

3.1 Multiple Independent Gate Silicon-On-Insulator (SOI) Transistor

G^4FET is a multiple independent gate transistor fabricated in silicon-on-insulator (SOI) technology. In this technology, a layered silicon-insulator-silicon substrate is used in place of a conventional bulk silicon substrate. The addition of silicon dioxide as the insulator just above the substrate and below the top silicon layer provides better isolation, prevents latch-up and reduces parasitic capacitance. This oxide layer is called the buried oxide (BOX). The topmost thin film of silicon on top of the buried oxide is the active region where all devices are fabricated. This is called epi/top Si layer. The bottom thick silicon layer is called the substrate or handle wafer. Figure 3.1 shows the layers of the SOI wafer.

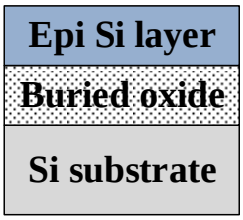


Figure 3.1: Three layers of SOI wafer.

There are two types SOI wafers: 1) fully-depleted (FD) and 2) partially-depleted (PD) SOI. The difference lies in the thickness and the doping density of the top silicon layer. The film

thickness and the doping concentration in FDSOI is such that the film gets fully depleted without any biasing just due to work function difference, as shown in Figure 3.2.

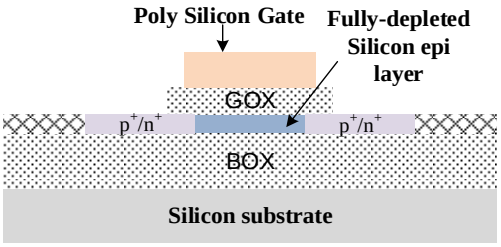


Figure 3.2: Cross-sectional schematic of a fully-depleted (FD) SOI device.

On the other hand, PDSOI has a slightly thicker Si film compared to FDSOI. Thus the epi silicon layer does not get fully depleted and there is a neutral region with mobile charge carriers at the center of the film as shown in Figure 3.3.

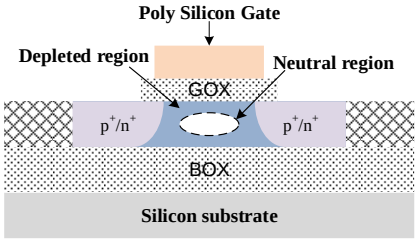


Figure 3.3: Cross-sectional schematic of a partially-depleted (PD) SOI.

Since the top-gate needs to support less depletion charge in FDSOI, it can trigger a rapid increase in inversion charges and provide a higher switching speed. The depletion charge is limited by the buried insulator layer and this reduction in depletion capacitance results in a substantial improvement of the subthreshold swing that can go down to the minimum theoretical value of 60 mV/decade for MOSFET at room temperature. The better subthreshold properties enable FD SOI

transistors to operate at lower gate bias with lower power consumption. Another short channel effect plaguing modern MOSFETs is threshold voltage roll off which is substantially reduced in FDSOI. However, PDSOI operates in an intermediate stage between the bulk and the FDSOI transistor. Its body is not fully depleted, but suitable biases applied at gate can deplete the entire body free of mobile carriers. In addition, PDSOI provides both volume and surface conduction. Therefore, depending on application, decision has to be made as to which one is more appropriate.

3.2 G^{4}FET Device Structure

G^{4}FETs can be fabricated using standard partially or fully-depleted SOI (PD/FD-SOI) process. It has four independent gates for modulating channel conduction. There are two lateral junction-gates which act like JFET gates and two vertical oxide gates which act like MOS gates. This transistor has also been called MOSJFET [15] since it combines both metal-oxide-semiconductor field-effect transistor (MOSFET) and junction field-effect transistor (JFET) actions in a single silicon island.

G^{4}FET is a majority carrier device. A regular *p*-channel SOI MOSFET with two body contacts on the opposite sides of the channel works as a *n*-channel G^{4}FET. The *p*+ doped source and drain of the MOSFET now function as lateral junction-gates. They are used like JFET gates to control the channel conduction width. The top oxide gate works like a classical MOS gate whereas the buried oxide along with the substrate biasing acts as a bottom-gate. These vertical gates are used to create the accumulation/depletion/inversion of free carriers in the silicon epi layer near the top and the bottom oxide interfaces. The body contacts are highly doped to make Ohmic contact with the channel and are used as the source and the drain for the *n*-channel G^{4}FET. An

accumulation/depletion-mode *n*-channel G^4FET is thus realized from an inversion-mode, *p*-channel MOSFET. Similarly, a *p*-channel G^4FET can be constructed from a conventional SOI *n*-channel MOSFET. Figure 3.4 shows the 3-D schematic structure of an *n*-channel G^4FET.

The cross section and the top view of the device are shown in Fig 3.5(a) and Figure 3.5 (b), respectively. The channel length and the channel width of the SOI MOSFET become the channel width and the channel length of the G^4FET, respectively. It is evident that no specialized fabrication procedure is necessary for this device.

3.3 Principle of Operation

The existence of four independent gates provides a multitude of possible combinations of gate biases, each giving rise to a unique conduction mechanism. The vertical gates can be inverted/depleted/ accumulated whereas the junction-gates are reverse biased in varying degrees for controlling the width of conduction channel. The flow of the drain current is perpendicular to the conventional MOSFET current flow. There can be three conduction paths, namely, 1) top surface conduction near gate oxide interface, 2) bottom surface conduction near buried oxide interface and 3) volume conduction inside the body away from vertical oxide interfaces. Depending on various applications, the specific components can be turned on or off using appropriate gate biases. In most application, the top-gate is accumulated and the transistor works as an accumulation mode MOSFET with two junction-gates providing JFET like control on the conduction channel. However, it is also possible to operate the vertical gates in depletion/inversion and this particular conduction mechanism, named depletion all around (DAA) has been shown to have very promising characteristics [24].

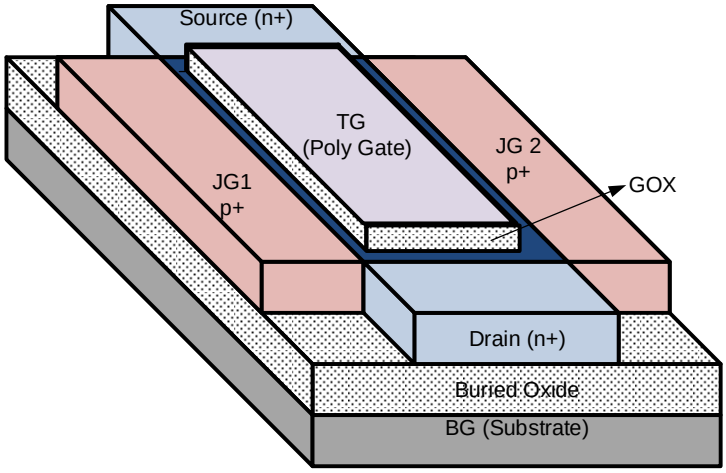
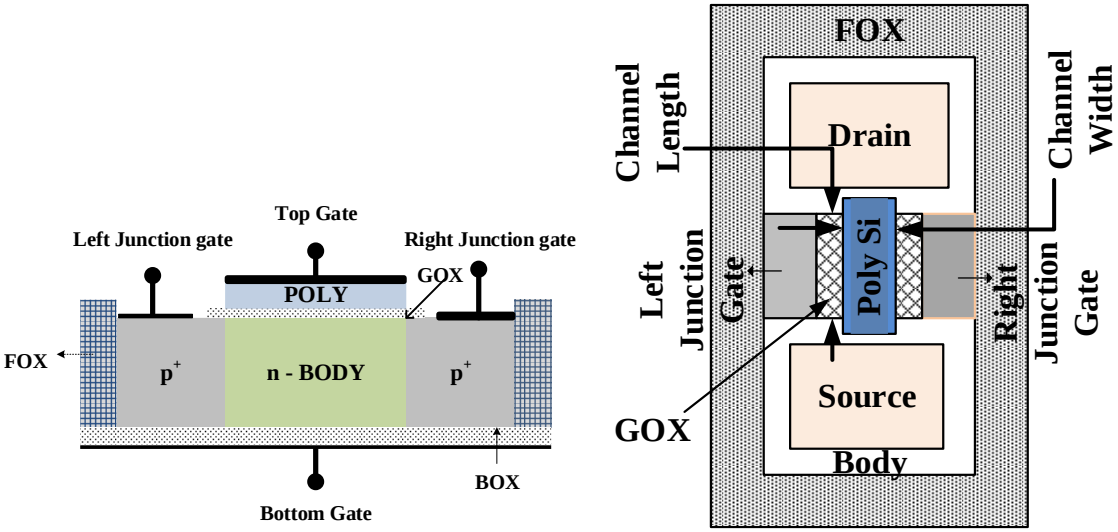


Figure 3.4: 3-D Schematic of a G^{4}FET structure.



(a) (b)

Figure 3.5: G^{4}FET structure: (a) cross section and (b) top view.

3.4 Effect of Gate Bias on Conduction Path

Numerical simulation in TCAD Sentaurus is used to visually demonstrate the effects of different gate biases on the conduction path. A three dimensional *n*-channel G^4FET structure is created using Sentaurus Structure Editor and simulated using Sentaurus Device. The cross section halfway along the channel length is used here to demonstrate the effect of lateral and vertical biases on conduction path. The channel conduction depends on the concentration of electrons inside the channel which is shifted by different gate biases. Here, V_{TG} is the top-gate voltage, V_{BG} is the bottom-gate voltage and V_{JG} is the junction-gate voltage applied at both junction gates which are connected together.

Figure 3.6 shows the electron concentration for keeping all the biases at 0 V. As the top-gate goes from 0 to -3 V, as shown in Figure 3.7, the conduction region gets vertically pushed down. Similar effect is shown for bottom-gate inversion in Figure 3.8 where the channel gets vertically pushed up as bottom-gate is biased at -3 V. Figure 3.9 shows the combined inversion effect of vertical gates when a narrow wire like conduction path is created at the center away from both oxide surfaces.

Figure 3.10 shows the effect of lateral depletion with both junction-gate reverse biased at -1 V. The channel now becomes narrower as lateral region near junction-gates gets depleted of free carriers.

Figure 3.11 shows the effect of accumulation at top-gate when V_{TG} = 3 V is applied. A thin layer of high electron density is formed near the oxide surface. Figure 3.12 shows the case when both the top and the bottom-gates are accumulated. In these two cases, the transistor provides both surface and volume conduction.

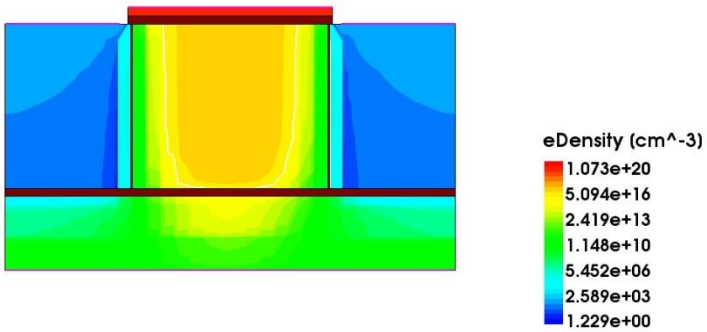


Figure 3.6: Electron density in the top silicon film at V_{TG} = 0 V, V_{BG} = 0 V and V_{JG} = 0 V.

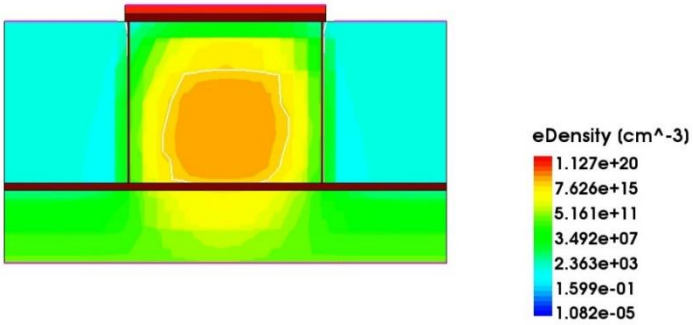


Figure 3.7: Electron density in the top silicon film at V_{TG} = -3 V, V_{BG} = 0 V, V_{JG} = 0 V.

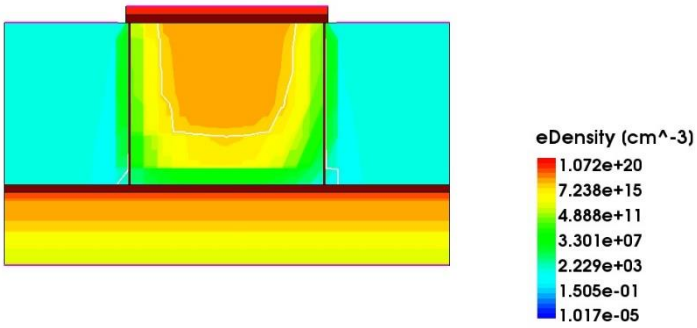


Figure 3.8: Electron density in the top silicon film at V_{TG} = 0 V V_{BG} = -3 V V_{JG} = 0 V.

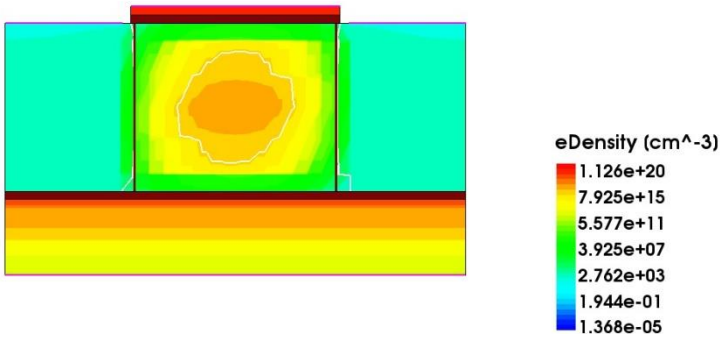


Figure 3.9: Electron density in the top silicon film at V_{TG} = -3 V, V_{BG} = -3 V, V_{JG} = 0 V.

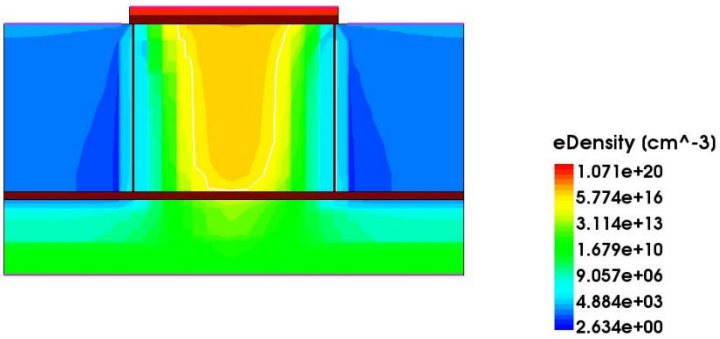


Figure 3.10: Electron density in the top silicon film at V_{TG} = 0 V, V_{BG} = 0 V and V_{JG} = -1 V.

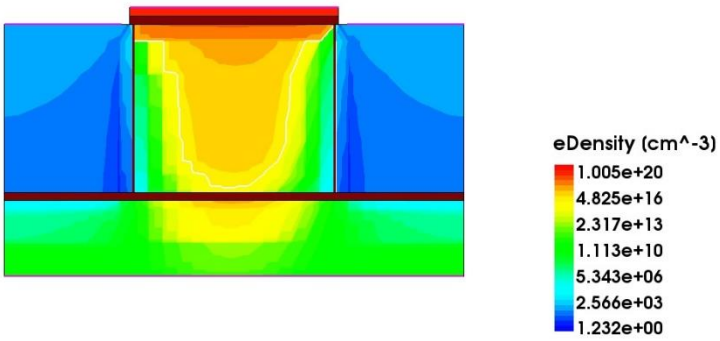


Figure 3.11: Electron density in the top silicon film at V_{TG} = 3 V, V_{BG} = 0 V and V_{JG} = 0 V.

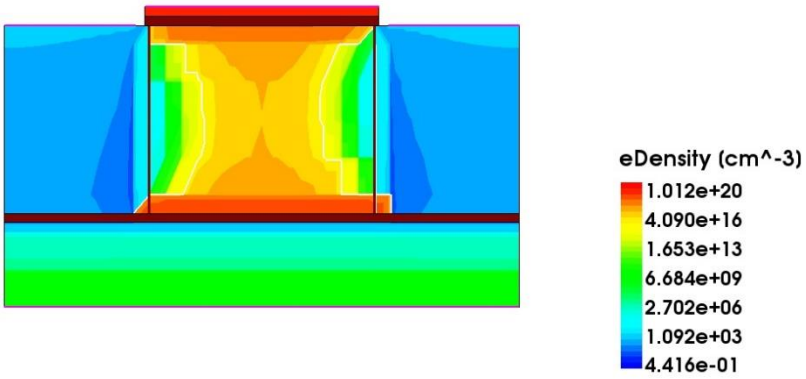


Figure 3.12: Electron density in the silicon film at V_{TG} = 3 V, V_{BG} = 10 V and V_{JG} = 0 V.

3.5 Chapter Summary

This chapter describes the physical structure of a G^{4}FET transistor and its formation from a conventional SOI MOSFET is outlined. The added flexibility of G^{4}FET can be obtained without any significant modification in the conventional SOI technology. The multiple independent gates provide G^{4}FET with several possible operating conditions which are explained with the aid of numerical simulation.

Chapter 4 - Numerical Modeling of G^4FET

4.1 Overview

Analytical models are important for understanding the underlying physics of the semiconductor devices. Nowadays, in the highly scaled down semiconductors, a number of physical phenomena, such as high-field mobility, carrier velocity saturation, gate oxide tunneling, drain induced barrier lowering and hot carrier effect dictate the semiconductor device characteristics. The physical phenomena are highly nonlinear in nature and their exact solution requires solving a set of coupled nonlinear differential equations, namely (i) Poisson, (ii) electron continuity and (iii) hole continuity equations. In today's small dimensional structure, quantum mechanical effect also has to be taken into consideration requiring coupled solution of Schrodinger's equation as well. G^4FET configuration requires a 3-D solution which makes it much harder and more time consuming. A closed form analytical expression, even in piecewise form, becomes almost impossible without a number of approximations.

Numerical modeling is another way of device modeling that gets rid of the above-mentioned problems. Different numerical methods have been explored over the years for modeling devices based on available data and are discussed in section 2.2. In this work, four different numerical models have been developed and implemented in commercial simulators for modeling G^4FETs. These methods are: 1) multivariate Lagrange interpolation polynomial model, 2) multidimensional Bernstein polynomial model, 3) multivariate regression polynomial model and 4) multidimensional linear and cubic spline interpolation model and are described in the following sections.

4.2 Numerical Method 1 (Multivariate Lagrange Interpolation Polynomial Model)

The first numerical model is the multivariate Lagrange interpolation polynomial which was proposed in [105]. Available data from TCAD simulation and experimental results have been used to develop numerical models for capturing the current-voltage (*I-V*) characteristic of a G^4FET. Given a set of distinct points (x_i,y_i), there is a unique polynomial of the least degree which, at each point x_i, provides the corresponding value y_i. This interpolating polynomial can be evaluated using Lagrange polynomial, Neville's algorithm or Newton polynomial. A single expression is derived for predicting the device characteristics over the entire region of device biasing inside the interpolation range.

4.2.1 Model Formulation

The model formulation involves determining a polynomial for fitting a set of chosen data points. Both simulation and experimental results are used for obtaining these training data set. For this one-dimensional case, a polynomial *f(x)* of degree *m* is developed, such that,

$$y_i = f(x_i) \tag{4.1}$$

for a chosen set of (*m+1*) data points (x_0,y_0),….(x_i,y_i),….,(x_m,y_m). Here, *f*(x) is the desired interpolation polynomial and the data points are called the node points for interpolation.

The Lagrange interpolation polynomial is denoted by *L*(*x*) with degree *m* which satisfies the condition that $L(x_i) = y_i$ for $i = 0, 1, \ldots, m$. It can be written as a linear combination of basis polynomials, $l_i(x)$ as,

$$L(x) = \sum_{i=0}^{m} l_i(x) y_i \tag{4.2}$$

where, the Lagrange basis polynomial $l_i(x)$ is given by,

$$l_i(x) = \frac{(x-x_0)(x-x_1)\ldots(x-x_{i-1})(x-x_{i+1})\ldots(x-x_m)}{(x_i-x_0)(x_i-x_1)\ldots(x_i-x_{i-1})(x_i-x_{i+1})\ldots(x_i-x_m)} = \prod_{j=0, j\neq i}^{m} \frac{(x-x_j)}{(x_i-x_j)} \quad (4.3)$$

The form of basis polynomial indicates that at each interpolating point $x = x_i$, $l_i(x) = 1$ and all the other basis polynomials $l_j(x) = 0$ ($j \neq i$). Consequently, at each node point x_i, $L(x_i) = y_i$, and error at node point becomes zero which is a very desirable property of Lagrange polynomial. The basis polynomial does not depend on the dependent variable.

The Lagrange polynomial can be extended for two dimensional cases as follows,

$$L(x, y) = \sum_i l_i(x)(\sum_j l_j(y) f(x_i, y_j)) \quad (4.4)$$

where, the basis polynomials $l_i(x)$ and $l_j(y)$ are expressed as shown in Equation (4.3). This demonstrates that the Lagrange polynomial can be written in a recursive fashion. For more than two variables, the Lagrange polynomial can be expanded in the same manner as in Equation (4.4). For four independent variables, it can be written as,

$$L(u, v, w, x) = \sum_i l_i(u)(\sum_j l_j(v)(\sum_k l_k(w)(\sum_l l_l(x) f(u, v, w, x)))) \quad (4.5)$$

If the variables (u, v, w and x) in equation (4.5) are replaced with V_{DS} (drain-to-source voltage), V_{TS} (top-gate-to-source voltage), V_{BS} (bottom-gate-to-source voltage), and V_{JS} (junction-gate-to-source voltage), the drain current can be expressed in the form of Lagrange polynomials as follows,

$$I_{DS}(V_{DS}, V_{TS}, V_{BS}, V_{JS}) = \sum_i l_i(V_{DS})(\sum_j l_j(V_{TS})(\sum_k l_k(V_{BS})(\sum_l l_l(V_{JS}) f(V_{DS}, V_{TS}, V_{BS}, V_{JS})))) \quad (4.6)$$

Interpolating polynomial is susceptible to Runge's phenomenon i.e. oscillation, especially at the edges of an interval which increases in magnitude with polynomials of high degree over a set of equidistant interpolation points. The oscillation can be minimized by using nodes that are

distributed more densely towards the edges of the interval. One possible choice for generating non-uniform grid for this purpose is using Chebyshev nodes.

For n^{th} order interpolation between an arbitrary interval [a,b], Chebyshev node x_i (i = *0,1,2,…,n*) is defined as,

$$x_i = \frac{1}{2}(a+b) + \frac{1}{2}(b-a)\cos(\frac{2i-1}{2n}\pi) \tag{4.7}$$

For the variable of the highest order, available data points closest to Chebyshev nodes have been used for the development of Lagrange model instead of a uniform node set.

The order of the Lagrange polynomial is represented by the highest power of the independent variable and depends on the number of data points taken corresponding to that variable. If the order of an independent variable x is denoted by O_x and the number of sample points used for interpolation is n_x then,

$$O_x = n_x - 1 \tag{4.8}$$

In this work, polynomial models are used for at most four variable functions. If the order of the variables V_{DS}, V_{TG}, V_{BG}, V_{JG} are O_{DS}, O_{TG}, O_{BG} and O_{JG}, respectively, then the total number of terms (N_{terms}) in the final expression will be,

$$N_{terms} = (O_{DS}+1)(O_{TG}+1)(O_{BG}+1)(O_{JG}+1) \tag{4.9}$$

The number of required additions and multiplications for evaluating the polynomial for a particular set of V_{DS}, V_{TS}, V_{BS}, and V_{JS} will dictate the speed of the circuit simulation. If the total number of additions/subtractions is N_{add} and the total number of multiplications is N_{mul} then,

$$N_{add} = (O_{DS}+1)(O_{TG}+1)(O_{BG}+1)\big(O_{JG}+1\big) - 1 = N_{terms} - 1 \tag{4.10}$$

and

$$N_{mul} = \frac{(O_{DS}+1)(O_{TG}+1)(O_{BG}+1)\big(O_{JG}+1\big)(O_{DS}+O_{TG}+O_{BG}+O_{JG})}{2} - N_{add} \tag{4.11}$$

which, after minor algebraic simplification becomes,

$$N_{mul} = N_{terms} \times ((\sum_{i=DS,TG,BG,JG} O_i \ )/2 \text{ -1}) \text{ +1} \quad (4.12)$$

This dependence dictates that the complexity of the model will increase with an increase in the order which will reduce the simulation speed and increase the memory requirement.

4.2.2 Model Validation

G^{4}FET models based on Lagrange polynomial are developed from experimental and TCAD Sentaurus training data for both *p*-channel and *n*-channel transistors. The order of the polynomial is determined by the number of data points used to develop the model. Then the model is validated using a comparison of current-voltage characteristics between another set of test data and model prediction.

4.2.2.1 An *n*-Channel G^{4}FET Simulated with TCAD Sentaurus (Device 1)

An *n*-channel G^{4}FET was designed and simulated in TCAD Sentaurus. Table 4.1 gives the device geometry, doping levels and biasing conditions applied in generating the training data. Here, V_{JG} is the voltage applied at both left and right junction-gates. The junction-gates were tied together during the simulations. The training data are used to develop a Lagrange polynomial model of the drain current, I_D as a function of four independent variables V_{DS}, V_{TG}, V_{BG} and V_{JG} according to the method described in section 4.2.1. The order of top-gate voltage V_{TG}, bottom-gate voltage V_{BG} and junction-gate voltage V_{JG} are chosen to be 5, 5 and 10, respectively.

Table 4.1: Geometry, Doping and Biasing for an *n*-Channel G^{4}FET

Geometry (μm)		**Doping Concentration (cm^{-3})**		**Terminal Voltage (V)**	
Length	1.5	Epi silicon	2.0x10^{17} (Phosphorus)	Top-gate (V_{TG})	0 to 5 V in 0.5 V increment
Width	0.4	Poly gate	10^{20} (Boron)	Bottom-gate (V_{BG})	0 to -15 V in 3 V decrement
Gate oxide thickness	.01	Both junction-gate	2.0x10^{20} (Boron)	Left junction-gate (V_{JG})	0 to -5 V in 0.5 V decrement
Buried oxide thickness	0.1	Source	10^{20} (Phosphorus)	Right junction-gate (V_{JG})	0 to -5 V in 0.5 V decrement
Active epi silicon layer thickness	0.1	Drain	10^{20} (Phosphorus)	Drain sweep (V_{DS})	0 to 5 V in 0.05 V increment

The drain current versus the drain-source voltage and the corresponding relative errors from TCAD data and Lagrange model are shown in Figures 4.1 and 4.2, respectively for a test biasing condition (V_{BG} = 0 V, V_{TG} = 3.5 V and V_{JG} = 0 V). The effect of model order on predictive accuracy is shown by changing the order of V_{DS} from 5 to 25. The Chebyshev nodes for different orders are shown in the independent axis. The extrapolation of model behavior outside the modeling range is also shown. As evident from this figure, the accuracy improves with the increase in the order resulting in a reduction in mean relative error.

In Figure 4.3, the junction-gate voltage, V_{JG} has been varied from 0 to -4 V with the top-gate voltage fixed at 3.5 V and for each of the junction-gate bias TCAD data and model predictions are superimposed. The order of V_{DS} is chosen to be 8 and from the corresponding mean relative error, it is shown that the model fits reasonably well for all the isolines.

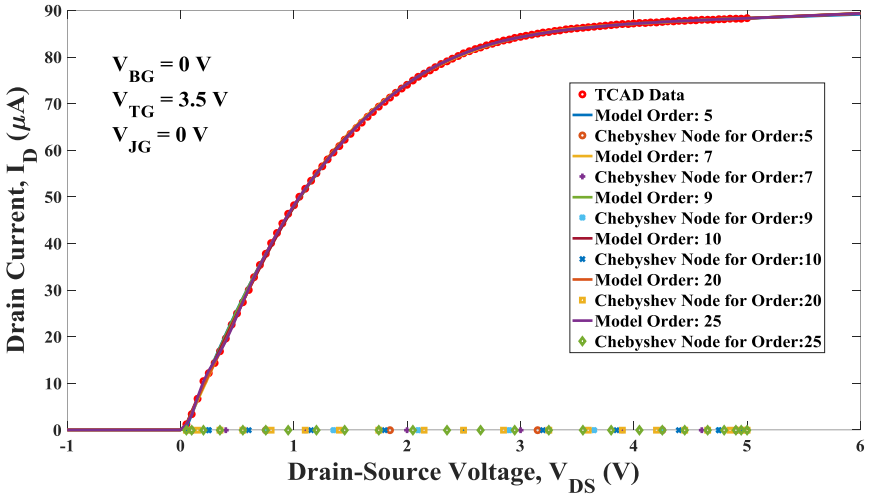


Figure 4.1: Drain current versus drain-source voltage from TCAD data and Lagrange model for different orders of V_{DS} for an *n*-channel G^{4}FET.

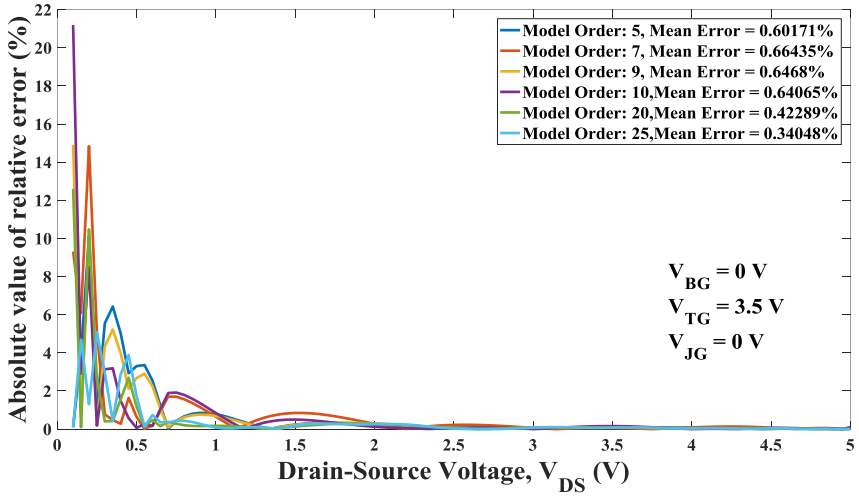


Figure 4.2: Relative errors between TCAD data and Lagrange model for different orders of V_{DS} for an *n*-channel G^{4}FET.

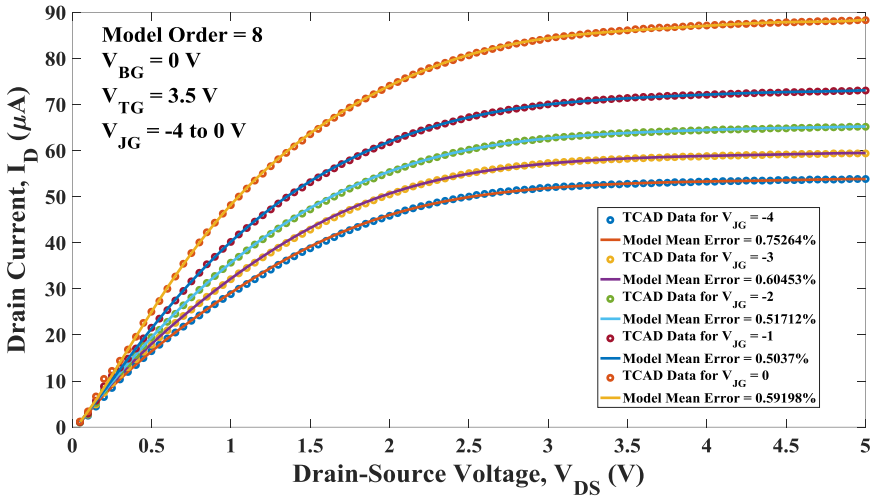


Figure 4.3: Isolines of test data and model for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment with order of V_{DS} fixed at 8.

4.2.2.2 Experimental Data from an *n*-Channel G^{4}FET (Device 2)

Device 2 is an *n*-channel transistor and has been fabricated in a conventional partially-depleted SOI (PDSOI) technology. The width and length of the device are 0.4 µm and 0.9 µm, respectively. Lagrange polynomial interpolation is used to model the current-voltage characteristics of the device from experimental data.

For the model development, the drain source voltage V_{DS} was fixed at 50 mV, the bottom-gate voltage V_{BG} was swept from -5 V to 5 V in 2 V increment, the junction-gate voltage was swept from -4 V to -1 V in 1 V increment while the top-gate voltage was swept from -3 V to 3 V in 0.05 V increment. Both junction-gates were tied together for all the measurements. The developed Lagrange polynomial model of the drain current, I_D as a function of three independent variables V_{TG}, V_{BG} and V_{JG}, based on this data, was then tested against a different set of experimental data.

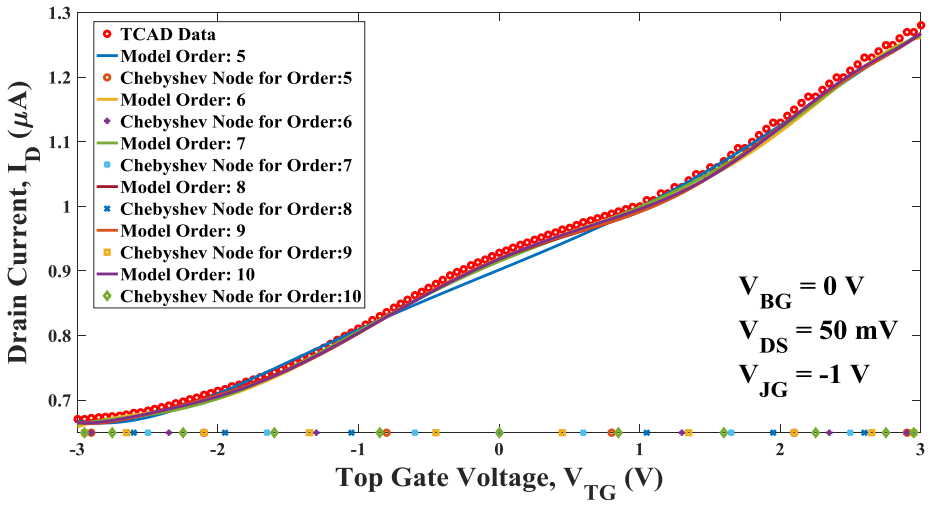


Figure 4.4: Drain current versus top-gate voltage from experimental data and Lagrange model for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2).

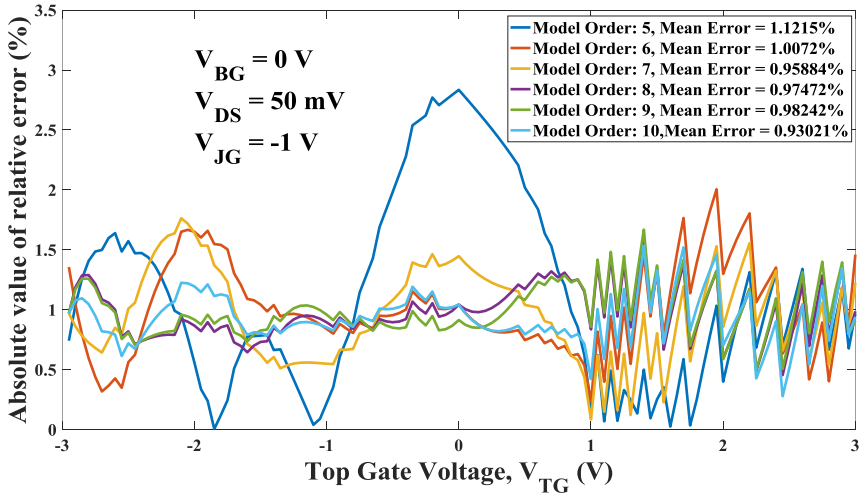


Figure 4.5: Relative errors in model prediction for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2).

For a particular test bias (V_{BG} = 0 V, V_{DS} = 50 mV and V_{JG} = -1 V), the drain current versus the top-gate voltage and the corresponding relative errors are shown in Figure 4.4 and Figure 4.5, respectively. Here, the order of V_{TG} has been changed from 4 to 10 while keeping the order of V_{BG} and V_{JG} fixed at 5 and 3, respectively. The model shows excellent fit with the test data, especially for order 7 or higher.

In Figure 4.6, isolines for different bottom-gate voltage V_{BG} are shown with their respective relative errors. Here, V_{BG} has been changed from -4 V to 4 V in 2 V increment and for its five different values, model predictions are superimposed on experimental data. The mean error for each biasing condition indicates excellent fitting.

4.2.2.3 A *p*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 3)

A *p*-channel G^{4}FET has been designed using TCAD Sentaurus. The device geometry, the doping levels and the biasing conditions used for model development are shown in Table 4.2.

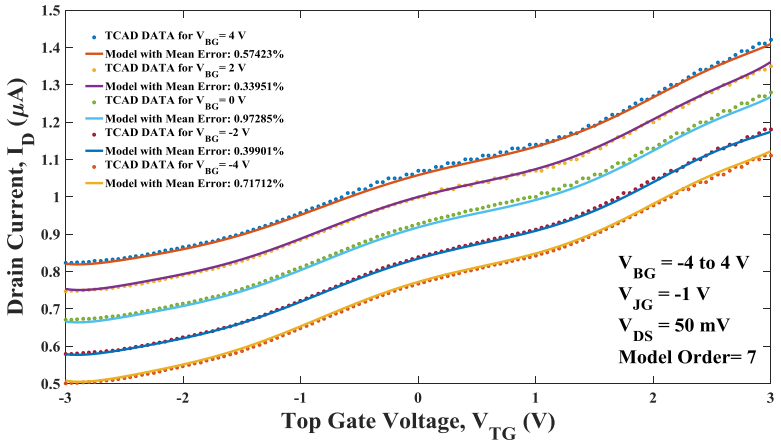


Figure 4.6: Comparison between isolines of test data and Lagrange model for different bottom-gate voltages ranging from -4 V to 4 V in 2 V increment with the model order for VTG fixed at 7 (Device 2).

Table 4.2: Geometry, Doping and Biasing for a *p*-Channel G^{4}FET

Geometry (μm)		**Doping Concentration (/cm^3)**		**Terminal Voltage (V)**	
Length	1.5	Epi silicon	2.0×10^{17} (Boron)	Top-gate (V_{TG})	0 to -5 V in 0.5 V decrement
Width	0.4	Poly gate	10^{20} (Phosphorus)	Bottom-gate (V_{BG})	0 to 15 V in 3 V increment
Gate oxide thickness	.005	Both junctions	2.0×10^{20} (Phosphorus)	Left junction-gate(V_{JG})	0 to 5 V in 0.5 V increment
Buried oxide thickness	0.1	Source	2.0×10^{20} (Boron)	Right junction-gate (V_{JG})	0 to 5 V in 0.5 V increment
Active epi silicon layer thickness	0.1	Drain	2.0×10^{20} (Boron)	Source-drain sweep (V_{SD})	0 to 5 V in 0.05 V increment

Here, V_{JG} stands for the voltage applied at both the junction-gates since the junction-gates were tied together for all the simulations. Based on the TCAD data, the Lagrange polynomial model is developed for the drain current, I_D as a function of four independent variables V_{SD}, V_{TG}, V_{BG} and V_{JG} following the method described in section 4.2.1. Here, the order of V_{TG}, V_{BG} and V_{JG} are kept fixed at 4. The order of V_{SD} has been swept from 5 to 10 to observe the effect of order on model accuracy. The developed model was then validated against a set of test data. The drain current versus the source-drain voltage and the corresponding relative errors are shown in Figure

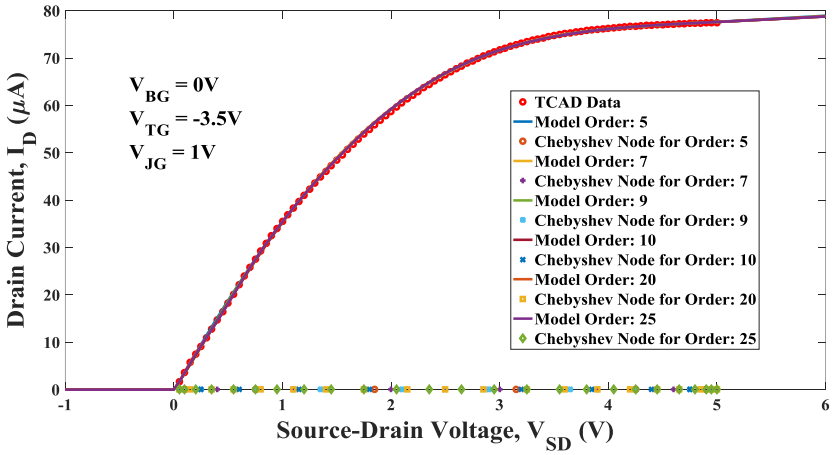


Figure 4.7: Drain current versus source-drain voltage from TCAD data and Lagrange model for different orders of V_{SD} for a *p*-Channel G^{4}FET (Device 3).

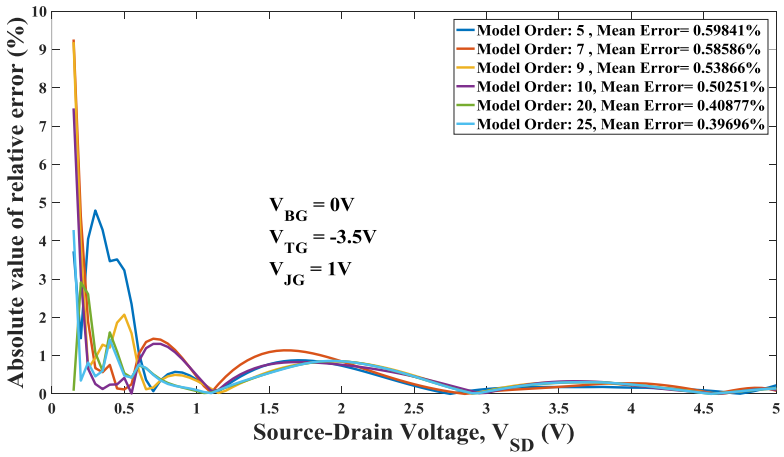


Figure 4.8: Relative errors between TCAD data and Lagrange model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3).

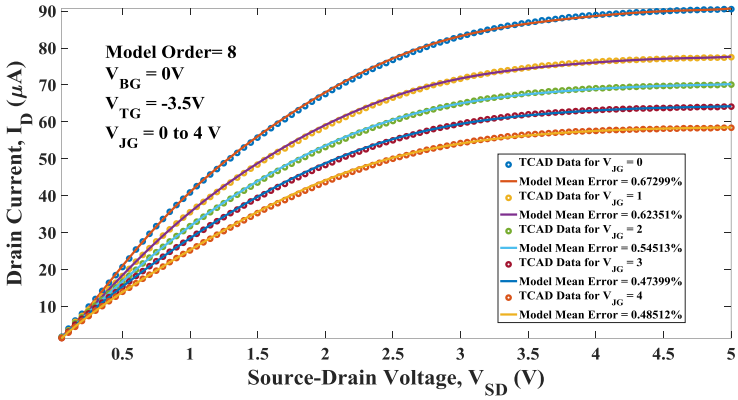


Figure 4.9: Drain current versus source-drain voltage for different junction-gate voltages ranging from 0 V to 4 V in 1 V increment and corresponding mean relative error (Device 3).

4.7 and 4.8, respectively for a particular test bias (V_{BG} = 0 V, V_{TG} = -3.5 V and V_{JG} = 1 V). It is evident from these figures that as the order of the model is increased, the error is reduced and the approximation gets better. The rate of improvement gradually slows down with an increase in the model order.

Figure 4.9 shows isolines for five different values of junction-gate bias V_{JG}. The top and bottom-gate bias are fixed at -3.5 V and 0 V, respectively while the junction-gate bias is swept from 0 to 4 V. The model order for V_{SD} is fixed at 8 and the corresponding mean error for each isoline demonstrates good fitting.

4.2.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4)

A *p*-channel G^{4}FET was fabricated in a conventional 0.35 µm partially-depleted SOI (PDSOI) technology with a width of 0.35 µm and a length of 3.4 µm. For the model development, the source-drain voltage V_{SD} was fixed at 50 mV, the bottom-gate voltage V_{BG} was fixed at 0 V, the junction-gate voltage V_{JG} was swept from 4 V to 0 V in -0.4 V decrement and the top-gate

voltage was swept from -3.3 V to 0 V in 0.003 V increment. Based on this data, the Lagrange model of the drain current, I_D as a function of two independent variables V_{TG} and V_{JG} is developed and then tested against a different set of experimental data. The drain current versus the top-gate voltage and the corresponding relative errors for a particular test bias (V_{SD} = 50 mV, V_{BG} = 0 V, V_{JG} = 1.4 V) are shown in Figure 4.10 and Figure 4.11, respectively. Here, the order of V_{JG} is kept fixed at 10 and the order of V_{TG} has been increased from 4 to 10.

Isolines for different junction-gate bias, V_{JG} are shown in Figure 4.12. Here, V_{JG} has been changed from 0.6 to 1.8 V in 0.4 V increment. The current decreases as the reverse bias in junction-gate increases. The small mean errors for all the isolines demonstrate good fitting with the data.

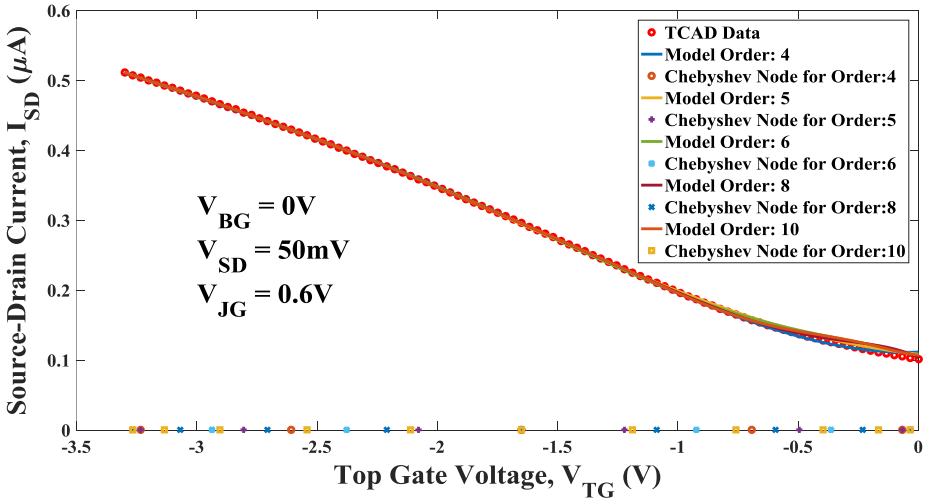


Figure 4.10: Comparison of I_D-V_{TG} between experimental data and Lagrange model for different orders of V_{TG} for a *p*-Channel G^{4}FET (Device 4).

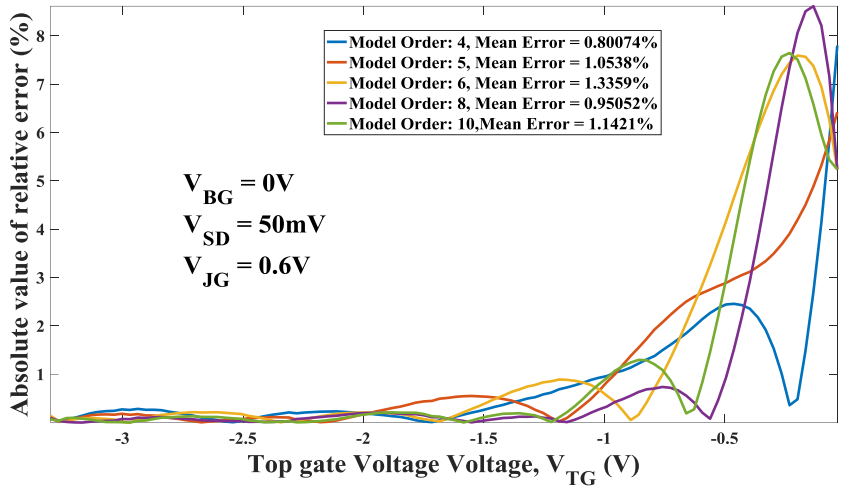


Figure 4.11: Relative errors between experimental data and Lagrange model for different orders of V_{TG} for a *p*-Channel G^{4}FET (Device 4).

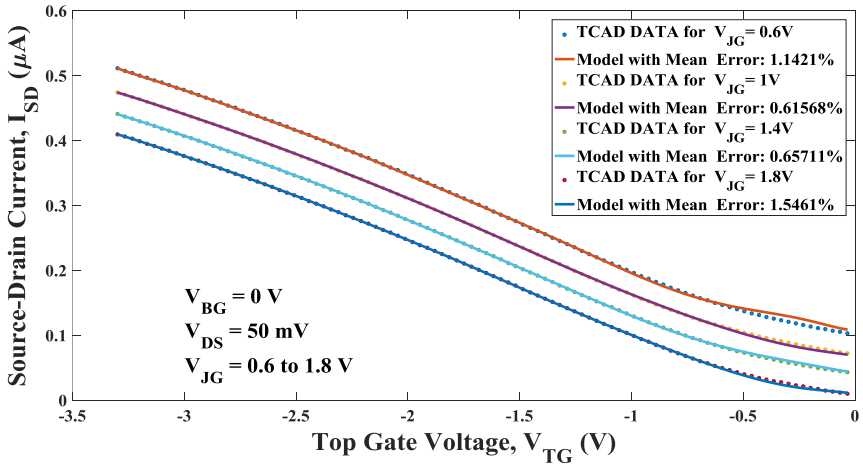


Figure 4.12: Isolines of test data and model (10th order V_{TG}) for different junction-gate voltages ranging from 0.6 V to 1.8 V in 0.4 V increment arranged from top to bottom (Device 4).

4.2.2.5 Incorporation of Device Geometry

The effect of device geometry can be incorporated in these models by considering width and length as independent variables in addition to the bias voltages. An *n*-channel G^{4}FET was simulated in TCAD Sentaurus for different widths (W) and lengths (L) with W being swept from 0.25 µm to 0.5 µm and L being swept from 0.8 µm to 1.8 µm, respectively.

Based on these data, multivariate Lagrange polynomial model is developed for drain current as a function of W, L and V_{DS}. Then the model was verified against a test device within this geometry range. Figure 4.13 and Figure 4.14 show the current-voltage characteristics and corresponding relative error for different model orders.

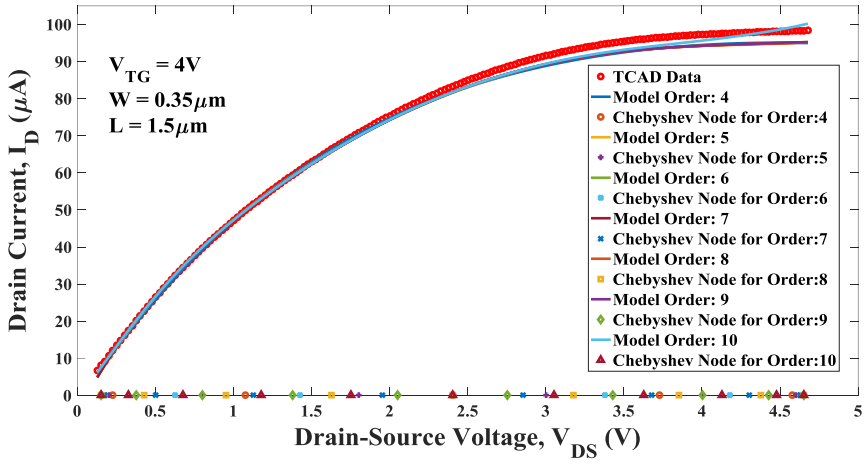


Figure 4.13: Comparison of drain current versus drain-source voltage between TCAD data and Lagrange model of test geometry for different orders.

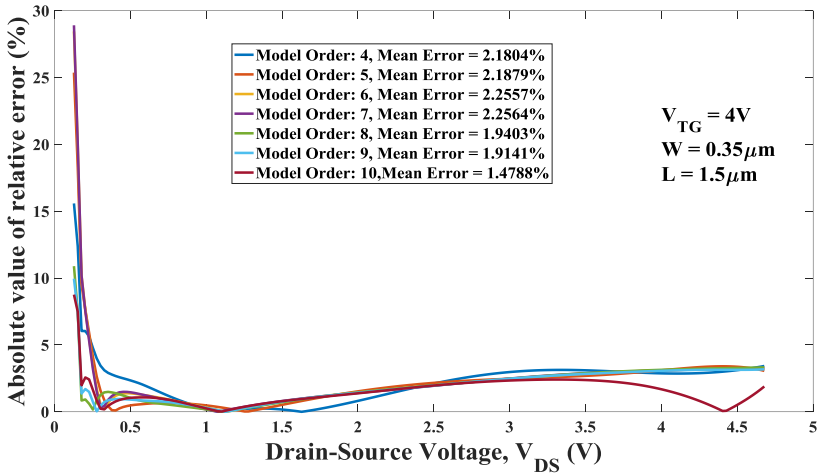


Figure 4.14: Relative errors between TCAD data and Lagrange model of test geometry for different orders.

4.2.2.6 First Order Characteristics i.e. Transconductance and Drain Output Resistance

First order characteristics such as transconductance and drain output resistance are crucial for transient simulation in SPICE simulators. In Figure 4.15, the transconductance versus the top-gate voltage is shown for Device 4 using different orders of the Lagrange model. Output drain resistance versus drain-source voltage for Device 1 is shown in Figure 4.16 for different orders of the Lagrange model where the y axis is shown in logarithmic scale. As these figures show, an increase in the model order improves the first order matching.

4.2.3 Implementation in Circuit Simulator

Based on the multivariate Lagrange polynomial model, both *n*-channel and *p*-channel G^4FET SPICE models have been developed. G^4FET has been modeled as a behavioral current

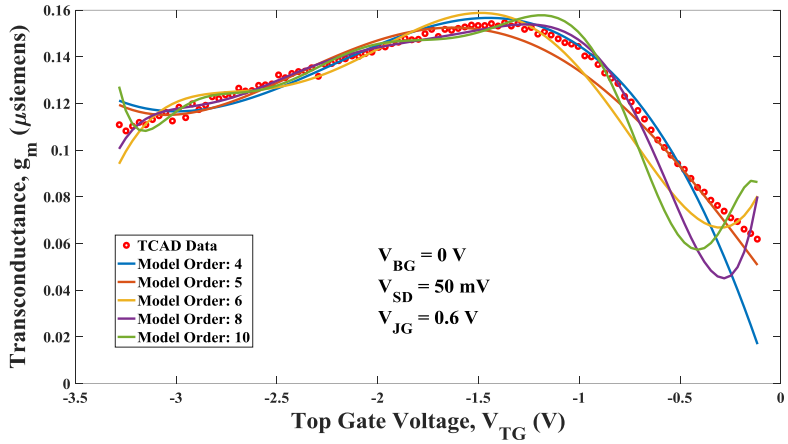


Figure 4.15: Comparison of $g_m - V_{TG}$ between experimental data and Lagrange model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4).

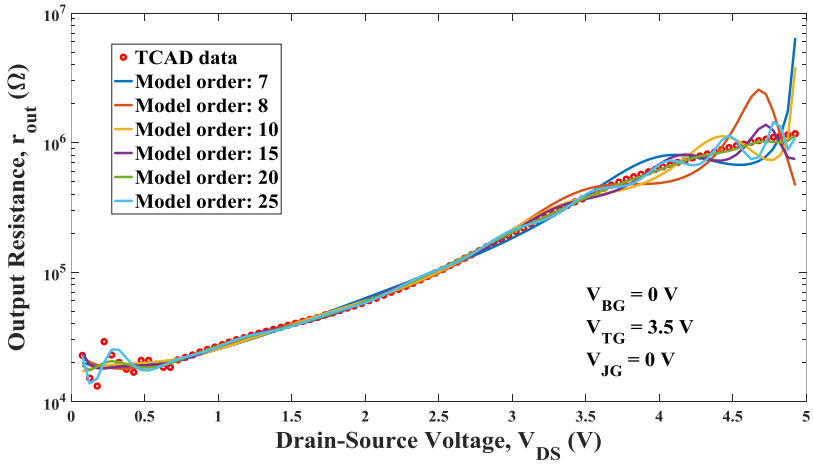


Figure 4.16: Comparison of r_{out} - V_{DS} between TCAD data and Lagrange model for different orders of V_{DS} for an *n*-channel G^{4}FET (Device 1).

source between the drain and the source terminals and its current is modeled as a function of the terminal voltages $V_{TS,}$ V_{BS}, V_{JS} and V_{DS} (Figure 4.17) and implemented as a sub-circuit. This block can be implemented in a SPICE simulator for simulating any circuit containing both *n*-channel and *p*-channel G^{4}FETs.The developed model has also been implemented in Cadence^{TM} which uses Spectre simulator. The behavioral model for Cadence^{TM} implementation is written in Verilog A.

Most simulators use Newton-Raphson algorithm which requires continuous functions with continuous first derivatives. Since Lagrange polynomials are infinitely continuous, they satisfy

Table 4.3: Computational Complexity of Lagrange Model

Device 1(*n*-channel G^{4}FET)			
Order of V_{DS}	Total Number of Terms (N_{terms})	Total Number of Required Addition/ Subtraction (N_{add})	Total Number of Required Multiplication (N_{mul})
4	1125	1124	10126
5	1350	1349	12826
6	1575	1574	15751
7	1800	1799	18901
8	2025	2024	22276
9	2250	2249	25876
10	2475	2474	29701
Device 3 (*p*-channel G^{4}FET)			
Order of V_{SD}	Total Number of terms (N_{terms})	Total number of required addition/ subtraction (N_{add})	Total number of required multiplication (N_{mul})
4	625	624	4376
5	750	749	5626
6	875	874	7001
7	1000	999	8501
8	1125	1124	10126
9	1250	1249	11876
10	1374	1374	13751

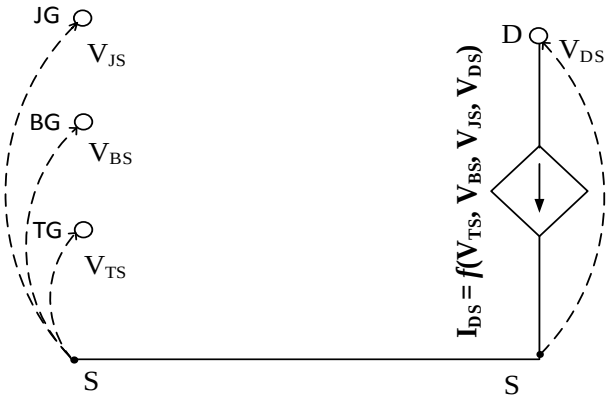


Figure 4.17: Behavioral model of an *n*-channel G^{4}FET.

these requirements nicely. The computational complexity for the host simulator program depends heavily on the evaluation of the polynomial model for each set of four terminal voltages. A list of required terms, additions and multiplications for the developed model for Device 1 (*n*-channel G^{4}FET) and Device 3 (*p*-channel G^{4}FET) is shown in Table 4.3. The order of the independent variables V_{TG}, V_{BG} and V_{JG} are 4, 8 and 4, respectively for Device 1 while for Device 3 all three variables have a fixed order of 4. The increase in order usually (but not always) improves the accuracy but it comes with sharp increase in computational cost as evident from Table 4.3.

4.2.4 Results from G^{4}FET Circuit Simulation

A negative differential resistance (NDR) circuit has been simulated with the developed model. The schematic of the conventional, two-terminal NDR device, known as "lambda diode" [106], is shown in Figure 4.18(a). The G^4-NDR is obtained by replacing the JFETs with complementary G^4-FETs as shown in Figure 4.18(b) with the junction-gates being tied together.

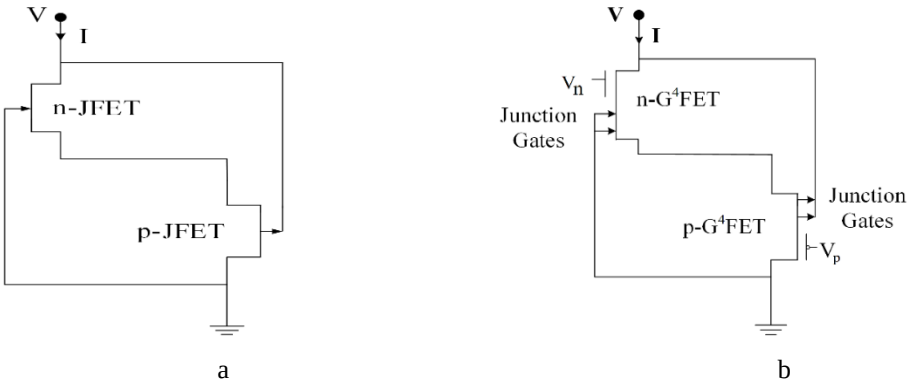


Figure 4.18: (a) A conventional two-terminal JFET NDR device, (b) a four-terminal G^{4}FET NDR device.

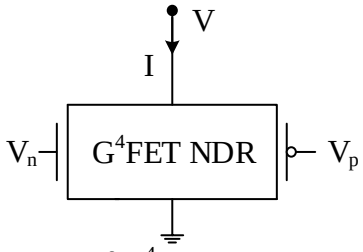


Figure 4.19: A simplified symbol of G^{4}FET NDR.

This innovative NDR device has four terminals, the extra two-terminals being the top-gates of the *n*-channel and the *p*-channel G^{4}FETs, driven by the voltages V_n and V_p, respectively. A simplified schematic is shown in Figure 4.19. In the conventional lambda structure, the NDR parameters such as peak/valley voltages and peak current are functions of the pinch-off voltages, V_T and the transconductance, g_m of each JFET which are fixed for a chosen pair of JFETs. However, in the G^{4}FET, V_T and g_m with respect to the junction-gates can be modulated by the MOS front gate. As a result, the parameters of a G^4-NDR device can be controlled by both V_n and V_p, which leads to a significant improvement in functionality compared to the lambda diode.

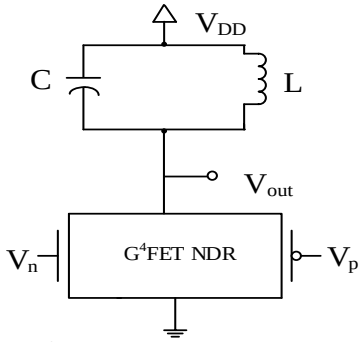
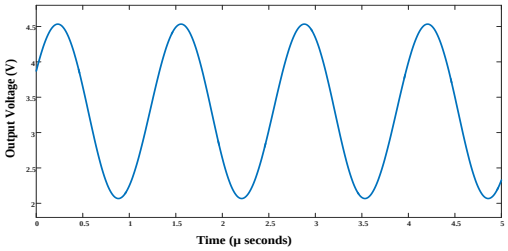
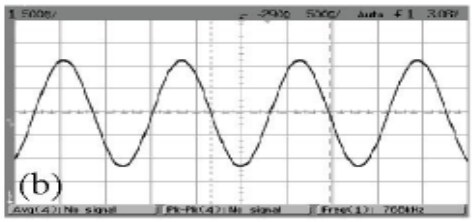


Figure 4.20: An LC oscillator using G^4-NDR.

A G^4-NDR loaded with an LC tank works as an LC oscillator (Figure 4.20). In [34], this oscillator has been demonstrated with V_{DD} = 3.3 V, L = 0.4 mH, C = 110 pF, f_{out} = 768 KHz, and $V_{out,pp}$ = 2.5 V. This circuit has been simulated with the developed SPICE model and the result is shown in Figure 4.21. The simulated oscillator output has a 2.47 V peak-to-peak amplitude with a frequency of 769 kHz compared to the experimental result of 2.5 V peak-to-peak amplitude with a frequency of 768 kHz with a relative error of 1.2 % in signal amplitude.



(a)



(b)

Figure 4.21: (a) Output from SPICE simulator (769 kHz signal with 2.47 V_{p-p} amplitude), (b) experimental result (768 kHz with 2.5 V_{p-p} amplitude).

4.3 Numerical Method 2 (Multidimensional Bernstein Polynomial Model)

Although Lagrange polynomials reproduce zeroth order characteristics such as *I-V* characteristics reasonably well, they do not always preserve the shape of the function with adequate precision which can cause problems while incorporating the model into a circuit simulator. One possible alternative is to use Bernstein polynomial instead of Lagrange polynomial.

4.3.1 Model Formulation

To capture the current-voltage characteristic of a G^4FET, Multivariate Bernstein polynomials are used to derive the numerical models from the available data set. Bernstein polynomial of degree *n* associated with function *f(x)* on interval [*a*, *b*] is defined as,

$$B_n(f;x) = \frac{1}{(b-a)^n}\sum_{i=0}^{n}\binom{n}{i}(x-a)^i(b-x)^{n-i}f(x_i) \tag{4.13}$$

where $\binom{n}{i}$ is the binomial coefficient and,

$$x_i = a + i(\frac{b-a}{n}),\ i = 0,1,2,\ \ldots,\ n \tag{4.14}$$

is an evenly distributed set of points in the interval [a, b].

Equation (4.13) can be re-written as,

$$B_n(f;x) = \sum_{i=0}^{n} B_{n,i}f(x_i) \tag{4.15}$$

where $B_{n,i}$ = Bernstein Basis Polynomial = $\frac{1}{(b-a)^n}\sum_{i=0}^{n}\binom{n}{i}(x-a)^i(b-x)^{n-i}$

Bernstein polynomial is not an interpolating function. Rather it is an approximation of the function *f(x)* and with the increase in degree *n*, it converges uniformly to *f(x)*. The extension to multidimensional case is similar to the Lagrange method described in section 4.2.1.

The modeling procedure starts with a set of available data from either an experiment or a simulation. The basis polynomial for each independent variable is calculated using equation (4.15) and then these polynomials are inserted into equation (4.6).

4.3.2 Model Validation

G^4FET models based on multivariate Bernstein polynomial approximation are developed from experimental and TCAD Sentaurus training data for both *n*-channel and *p*-channel transistors. The order of the polynomial is determined by the number of data points used to develop the model. Then the current-voltage characteristics predicted by the model are validated against another set of test data.

4.3.2.1 An *n*-Channel G^4FET Simulated Using TCAD Sentaurus (Device 1)

An *n*-channel G^4FET has been designed using TCAD Sentaurus. The device geometry, doping levels and biasing conditions are given in Table 4.1. V_{JG} is the voltage applied at both junction-gates. Based on the *I-V* data obtained from TCAD, Bernstein polynomial models are developed for the drain current, I_D as a function of four independent variables V_{DS}, V_{TG}, V_{BG} and V_{JG} following the method described in section 4.3.1. The order of V_{DS} has been changed to observe the effect of the order on the model accuracy.

For a test biasing condition (V_{BG} = 0 V, V_{TG} = 3.5 V and V_{JG} = 0 V), the drain current versus the drain-source voltage characteristics and the corresponding relative errors are shown in Figure 4.22 and Figure 4.23, respectively. As these figures show, the increase in model order reduces error and improves the approximation. Although the accuracy is less than its Lagrange counterpart, it is better at preserving monotonicity of the function. The Chebyshev interpolation nodes are shown in the independent axis. The extension of the model behavior outside the data range is also shown.

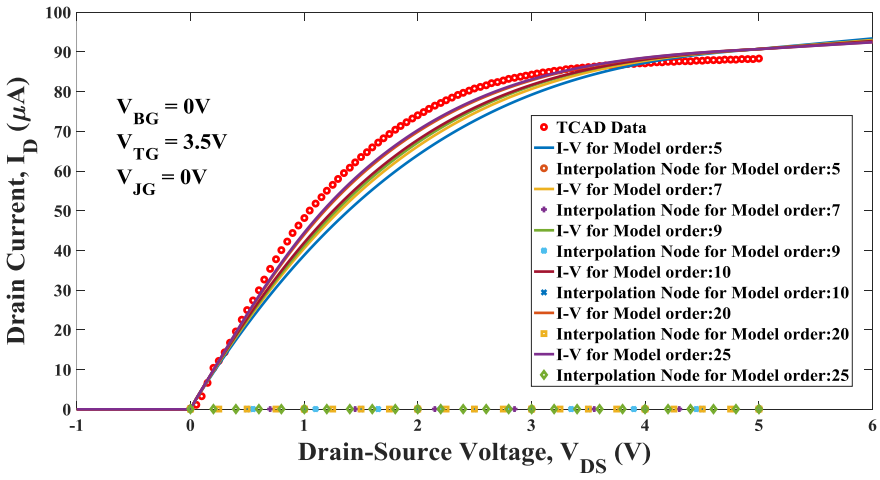


Figure 4.22: Drain current versus drain-source voltage from TCAD data and Bernstein model for different orders of V_{DS} in an *n*-channel G^{4}FET (Device 1).

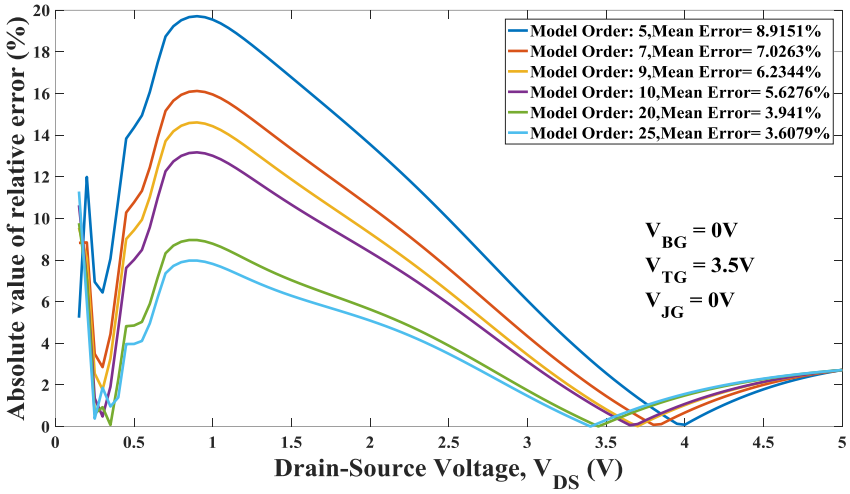


Figure 4.23: Relative errors between TCAD data and Bernstein model for different orders of V_{DS} for an *n*-channel G^{4}FET (Device 1).

4.3.2.2 Experimental Data from an *n*-Channel G^{4}FET (Device 2)

Multivariate Bernstein polynomial was used to model an *n*-channel G^{4}FET from experimental data. The device was fabricated in a conventional partially-depleted SOI (PDSOI) technology with a width of 0.4 µm and a length of 0.9 µm. Both junction-gates were tied together for simplicity.

The biasing condition for obtaining training data set was described in section 4.2.2.2. The developed Bernstein polynomial model of the drain current, I_D as a function of three independent variables V_{TG}, V_{BG} and V_{JG} was then tested against a different set of experimental data. For a particular test bias (V_{BG} = 0 V, V_{DS} = 50 mV and V_{JG} = -1 V), the drain current versus the top-gate voltage and the corresponding relative errors are shown in Figure 4.24 and Figure 4.25, respectively. The Chebyshev nodes are used as interpolation sites and they are shown in the independent axis.

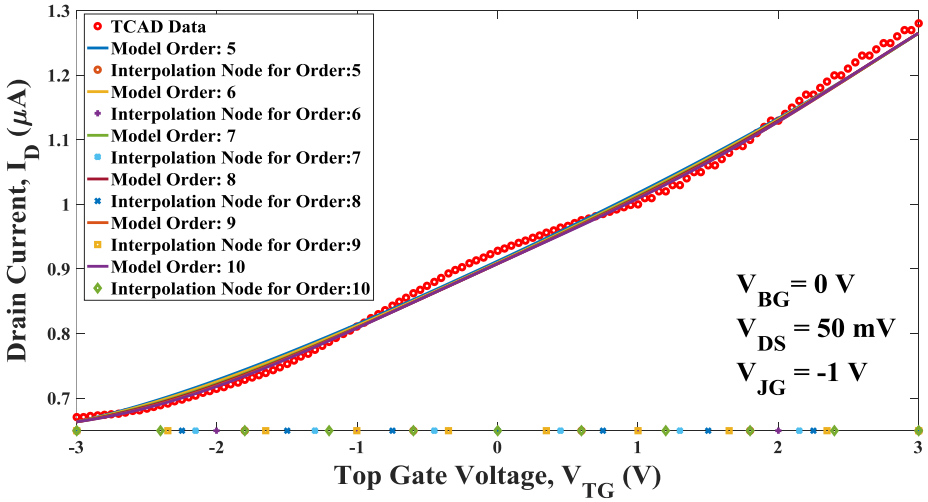


Figure 4.24: Drain current versus top-gate voltage from experimental data and Bernstein model for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2).

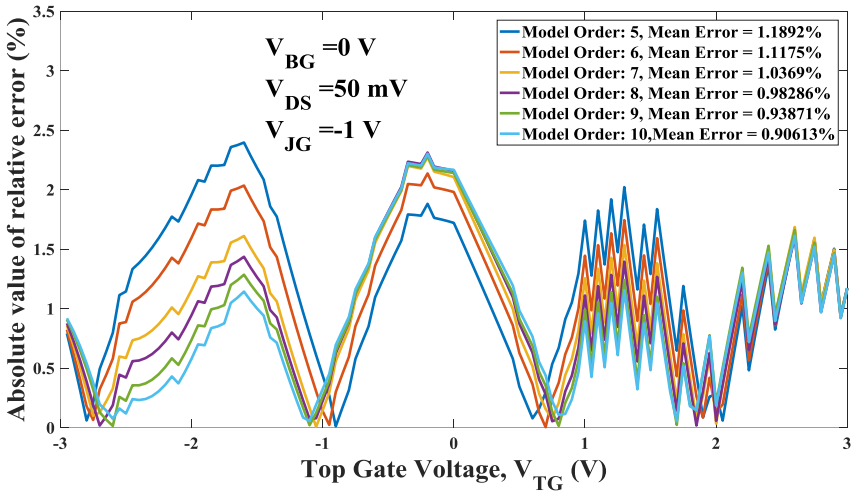


Figure 4.25: Relative errors between experimental data and Bernstein model for different orders of V_{TG} for an *n*-channel G^{4}FET (Device 2).

4.3.2.3 A *p*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 3)

A *p*-channel G^{4}FET has been designed using TCAD Sentaurus. The device geometry, the doping levels and the biasing conditions used for model development are shown in Table 4.2. Here, V_{JG} stands for the voltage applied at both the junction-gates since the junction-gates were tied together for all the simulations. Based on the TCAD data, the Bernstein polynomial model is developed for the drain current, I_D as a function of four independent variables V_{SD}, V_{TG}, V_{BG} and V_{JG} following the method described in section 4.3.1. The order of V_{SD} is varied to observe the effect of order on model accuracy. The drain current versus the source-drain voltage and the corresponding relative errors are shown in Figure 4.26 and Figure 4.27, respectively for a particular test bias (V_{BG} = 0 V, V_{TG} = -3.5 V and V_{JG} = 1 V).

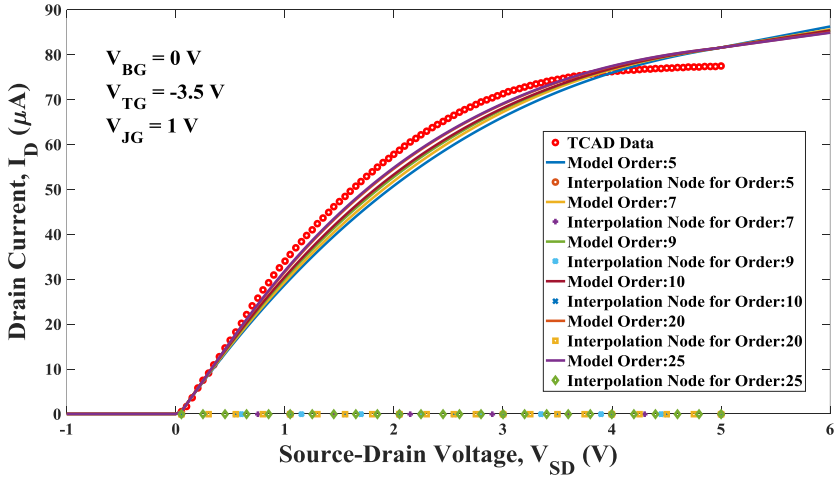


Figure 4.26: Comparison of I_D-V_{SD} between TCAD data and Bernstein model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3).

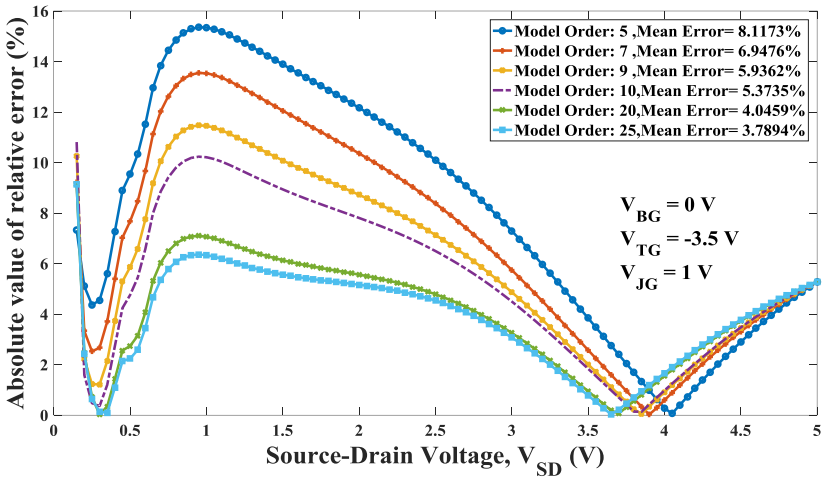


Figure 4.27: Relative errors between TCAD data and Bernstein model for different orders of V_{SD} for a *p*-channel G^{4}FET (Device 3).

It is evident from these figures that as the order of the model is increased, the error is reduced and the approximation gets better. The Chebyshev nodes are used as interpolation sites and are shown in the independent axis. The model is extrapolated to show its operating behavior outside the modeling range.

4.3.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4)

A *p*-channel G^{4}FET was fabricated in a conventional 0.35 µm partially-depleted SOI (PDSOI) technology with a width of 0.35 µm and a length of 3.4 µm. The source-drain voltage V_{SD} was fixed at 50 mV, the bottom-gate voltage V_{BG} was fixed at 0 V, the junction-gate voltage V_{JG} was swept from 4 V to 0 V in -0.4 V decrement and the top-gate voltage was swept from -3.3V to 0 V in 0.003 V increment. The Bernstein polynomial model of the drain current, I_D as a function of two independent variables V_{TG} and V_{JG} is developed using these training data and tested against a different set of experimental data.

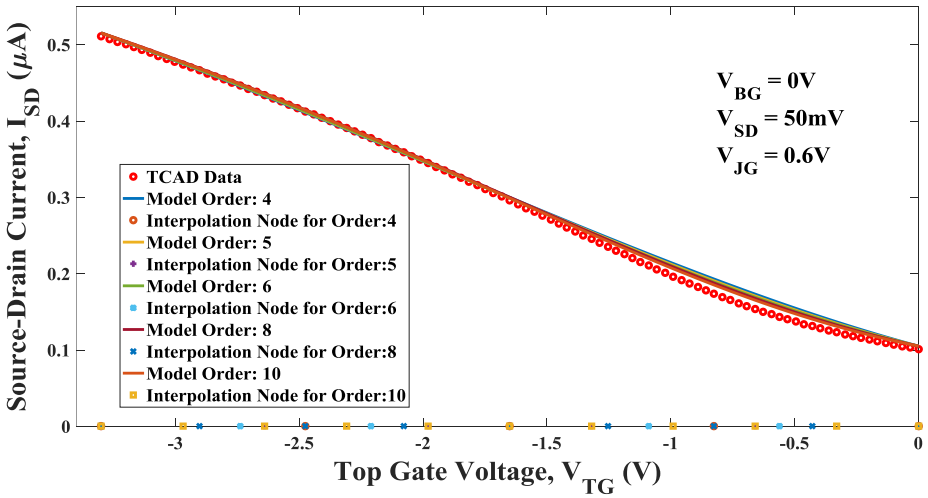


Figure 4.28: Comparison of I_{SD}-V_{TG} between experimental data and Bernstein model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4).

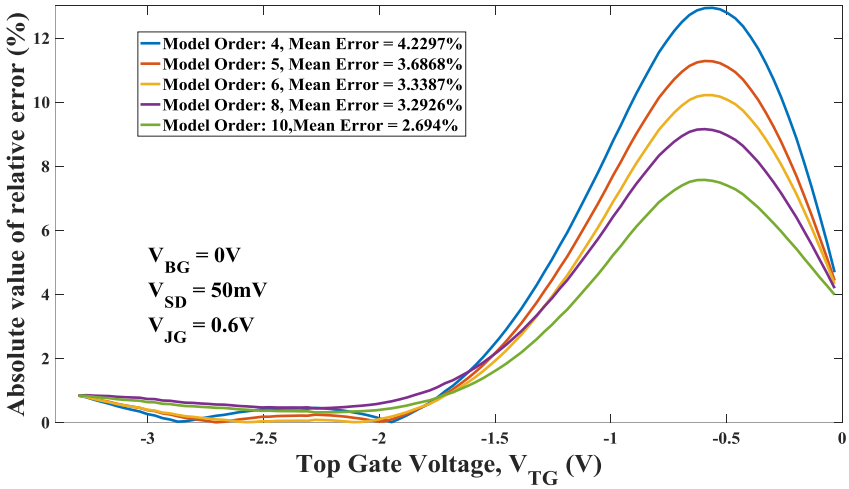


Figure 4.29: Relative errors between experimental data and Bernstein model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4).

The drain current versus the top-gate voltage and the corresponding relative errors for a particular test bias (V_{SD} = 50 mV, V_{BG} = 0 V, V_{JG} = 0.6 V) are shown in Figure 4.28 and Figure 4.29, respectively. Here, the order of V_{TG} has been increased from 4 to 10 to observe the effect of order on model accuracy. As the figures show, the model accuracy improves with an increase in the order of the independent variable.

4.3.2.5 Incorporation of Device Geometry

The geometrical features such as width and length of the transistors can be considered as independent variables and by including these variables in the final drain current expression in addition to the bias voltages, their effect, can be incorporated in the model. Here, an *n*-channel G^4FET was designed and simulated in TCAD Sentaurus with width (*W)* swept from 0.25 µm to 0.5 µm in 0.05 µm increment and length (*L*) swept from 0.8 µm to 1.8 µm in 0.2 µm increment.

A Bernstein polynomial model for drain current as a function of *W*, *L* and V_{DS} is developed based on these data. The model is verified against a test device within the training geometry range and the results are shown in Figure 4.30 and Figure 4.31. Here, the top-gate voltage is kept fixed at 4 V, the width and the length are 0.35 µm and 1.5 µm, respectively. The figures demonstrate a substantial reduction in error with the increase in the model order.

4.3.2.6 First Order Characteristics i.e. Transconductance and Drain Output Resistance

Although the Bernstein models of the same order have less accuracy compared to the Lagrange models, they are better in preserving the shape of the function i.e. concavity/convexity,

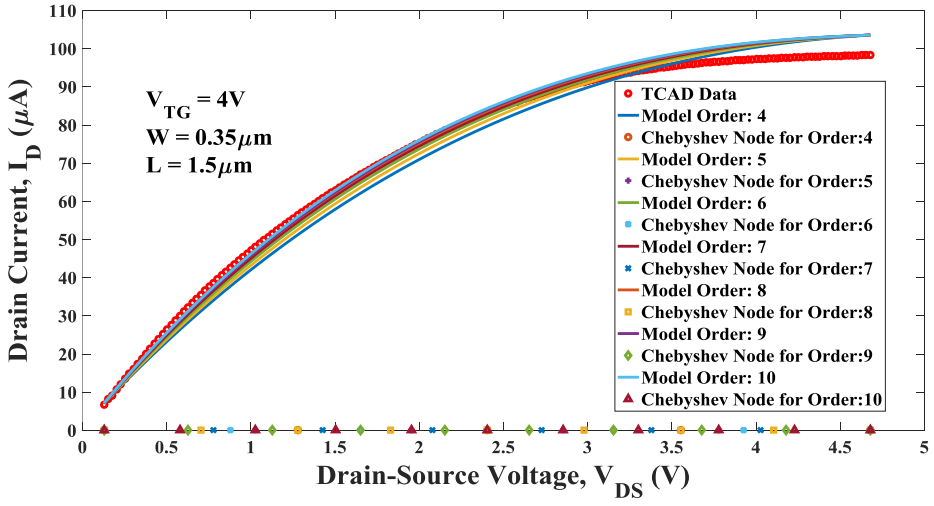


Figure 4.30: Drain current versus drain-source voltage from TCAD data and Bernstein model of different orders for test geometry.

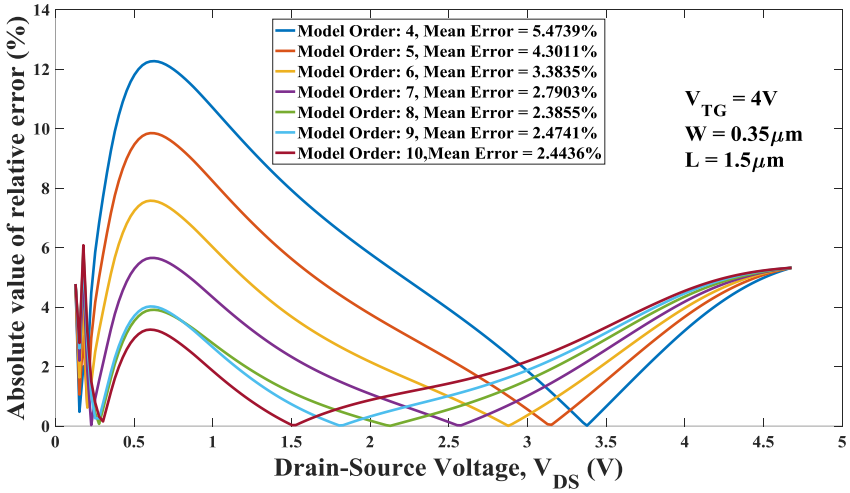


Figure 4.31: Relative errors between TCAD data and Bernstein model for test geometry.

monotonicity etc. and provide better first order characteristics such as transconductance and drain output resistance which play an important role in SPICE circuit simulators. A comparison between experimental data and Bernstein model for the transconductance versus top-gate voltage for Device 4 is shown in Figure 4.32. Here, bottom-gate voltage, source-drain voltage and junction-gate voltage are fixed at 0 V, 50 mV and 0.6 V respectively.

A comparison between TCAD data and different orders of Bernstein model for drain output resistance versus drain-source voltage for Device 1 is shown in Figure 4.33 where the vertical axis is shown in logarithmic scale. Here, the bottom-gate voltage, the top-gate voltage and the junction-gate voltage are fixed at 0 V, 3.5 V and 0 V, respectively.

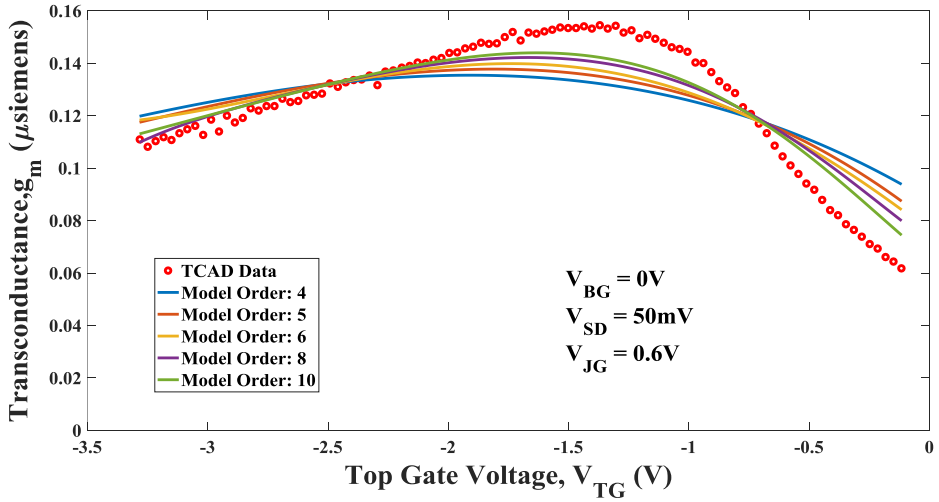


Figure 4.32: Transconductance versus top-gate voltage from experimental data and Bernstein model for different orders of V_{TG} for a *p*-channel G^{4}FET (Device 4).

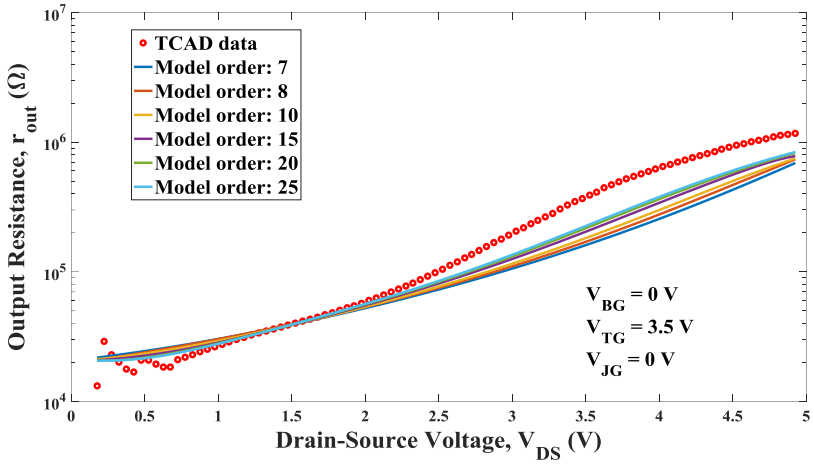


Figure 4.33: Output resistance versus drain-source voltage from TCAD data and Bernstein model for different orders of V_{DS} for an *n*-channel G^{4}FET (Device 1).

4.4 Numerical Method 3 (Multivariate Regression Polynomial Model)

In the previous two methods described in section 4.2 and 4.3, the increase in accuracy requires a denser grid resulting in a higher order Lagrange/ Bernstein model with concomitant slowing down of simulation speed. In addition, model terms are fixed, cannot be simplified and allow only integer exponents. One way of solving these problems is the use of multivariate regression analysis. In this approach, the order of the final model does not solely depend on the number of sample points. Model developer has the flexibility of picking specific model terms and consequently, with some prior knowledge of device behavior, model can be simplified to a great extent. Besides, non-integer exponents can be implemented as well.

4.4.1 Model Formulation

In this approach, a polynomial regression model is first chosen consisting of suitable model terms. Then the coefficients of this regression model are estimated for least square error. The total

number of terms in the model is chosen by user, not predetermined by the number of sample points. This model also allows non-integer exponents. With some prior knowledge of the expected behaviour of the devices, simplified model can be developed.

The coefficients of a polynomial regression model are calculated using traditional linear least squares techniques. Once the multivariate polynomial model has been specified, the problem is broken down to the estimation of the vector **x** for the linear system of equations as follows,

$$A*\mathbf{x} = \mathbf{y} \tag{4.16}$$

where *A* is the matrix of model terms of independent variables evaluated at chosen data points, ***x*** is the vector of unknown coefficients and ***y*** is the vector of known dependent variable.

For this estimation to have a unique solution, the matrix ***A*** should be both nonsingular and have more rows than columns. Problems with fewer rows than columns are underdetermined and one needs to acquire more data if the number of data points is fewer than the coefficients to be estimated.

Assuming that ***A*** is an $m \times n$ matrix, with $m>n$, this system can be solved through different approaches. A pivoted QR decomposition is used in this work which is quite efficient and numerically stable.

The order of the regression polynomial is represented by the highest power of the independent variable. It can be chosen by the model developer corresponding to that variable, independent of the number of data points taken. If the order of the variables V_{DS} (drain to source voltage), V_{TS} (top-gate voltage), V_{BS} (bottom-gate voltage) and V_{JS} (junction-gate voltage) are O_{DS}, O_{TS}, O_{BS} and O_{JS}, respectively, then the total number of terms (N_{terms}) in the final expression will be,

$$N_{terms} = (O_{DS} + 1)(O_{TS} + 1)(O_{BS} + 1)(O_{JS} + 1) \tag{4.17}$$

The number of required additions and multiplications for evaluating the model polynomial for a particular set of model terms containing V_{DS}, V_{TS}, V_{BS}, and V_{JS} will dictate the speed of the circuit simulation. If the total number of additions/subtractions is N_{add} and the total number of multiplications is N_{mul} then,

$$N_{add} = (O_{DS} + 1)(O_{TS} + 1)(O_{BS} + 1)(O_{JS} + 1) - 1 = N_{terms} - 1 \quad (4.18)$$

$$N_{mul} = N_{terms} \times ((\sum_{i=DS,TS,BS,JS} O_i \ )/2 \text{ -1}) \text{ +1} \quad (4.19)$$

Due to this dependence, the complexity of the model will increase with an increase in the order resulting in a slowdown of the simulation speed. With prior knowledge of the device characteristics, the model developer may select a few model terms of suitable orders for capturing essential behavior without choosing all possible combinations of model terms up to a given order and substantially reduce the complexity of the model.

4.4.2 Model Validation

Current-voltage data for different bias values have been gathered from both experiment and TCAD Sentaurus for both *p*-channel and *n*-channel G^{4}FET transistors. Models for these devices are formulated using multivariate regression polynomial model. Then the current-voltage characteristics predicted by the model are tested against another set of test data.

4.4.2.1 An *n*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 1)

Device 1 is an *n*-channel G^{4}FET designed and simulated using TCAD Sentaurus. The device geometry, the doping levels and the biasing conditions are shown in Table 4.1. Based on the *I-V* data extracted from TCAD, a multivariate regression polynomial model is developed for

the drain current, I_{DS} as a function of four independent variables V_{DS}, V_{TG}, V_{BG} and V_{JG} following the method described in section 4.4.1. Different values are used for the order of V_{DS} and V_{BG} in the model equation to observe the effect of varying order on model accuracy. For a particular bias (V_{BG} = 0 V, V_{TG} = 2.25 V and V_{JG} = -1 V), the drain current versus the drain-source voltage characteristics and the corresponding relative error are shown in Figure 4.34 and Figure 4.35, respectively. The order of V_{TG} and V_{JG} are kept fixed at 4, the order of V_{BG} is chosen to be 3 and the order of V_{DS} is changed from 6 to 10 to show the effect of increasing order on model characteristics. Figure 4.35 demonstrates that the error is decreasing from 0.90738% to 0.88305% to 0.84004% as we increase the order from 6 to 8 to 10. For Figure 4.36 and Figure 4.37, the order of bottom-gate voltage has been changed from 3 to 4. In Figure 4.38, isolines are shown for different values of V_{JG} ranging from 0 V to -4 V, where the order of four independent variables,

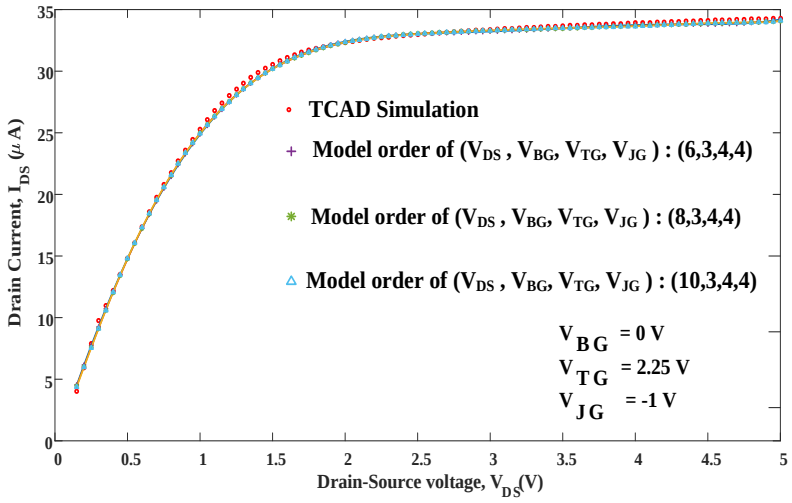


Figure 4.34: Comparison of I_{DS}-V_{DS} between TCAD data and regression model for different orders of V_{DS} with order of V_{BG} fixed at 3 for an *n*-channel G^{4}FET.

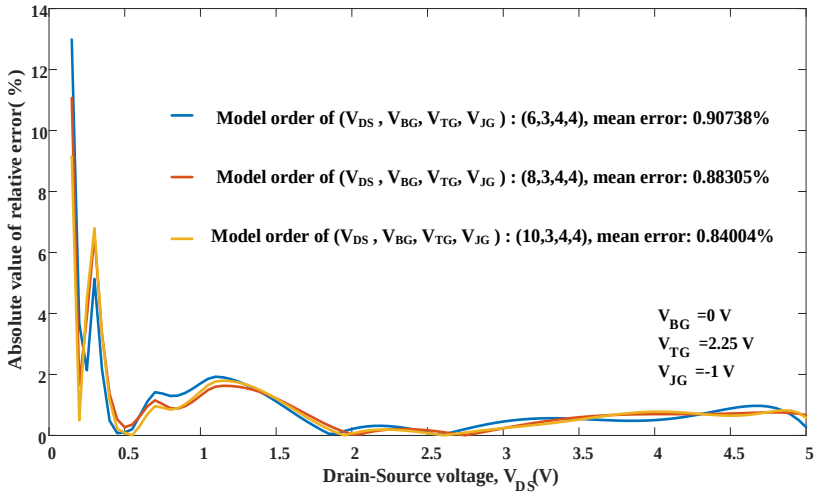


Figure 4.35: Relative error between TCAD data and regression model for different orders of V_{DS} with V_{BG} fixed at 3 for an *n*-channel G^{4}FET.

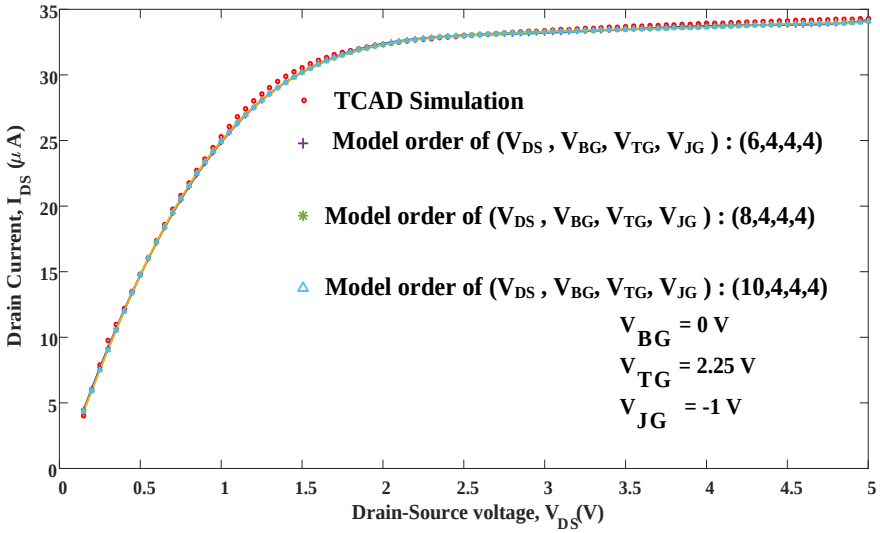


Figure 4.36: Comparison of I_{DS}-V_{DS} between TCAD data and regression model for different orders of V_{DS} with order of V_{BG} fixed at 4 for an *n*-channel G^{4}FET.

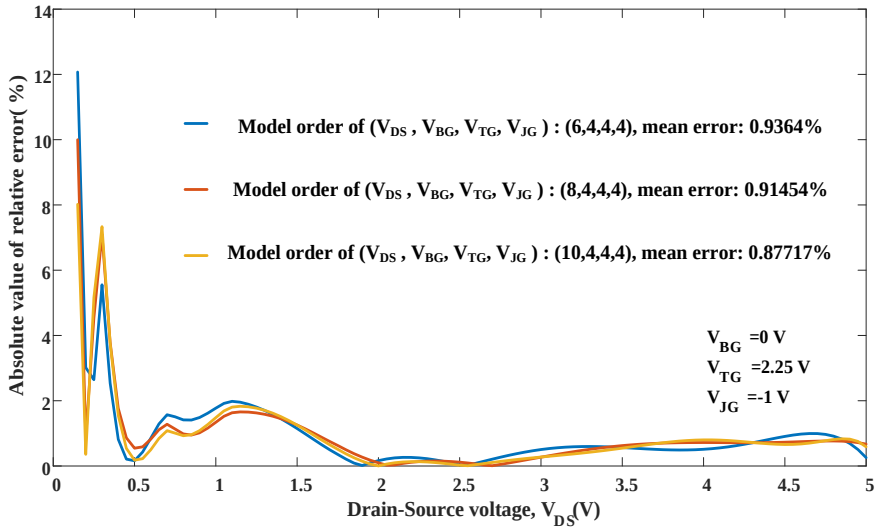


Figure 4.37: Relative error between TCAD data and regression model for different orders of V_{DS} with order of V_{BG} fixed at 4 for an *n*-channel G^{4}FET.

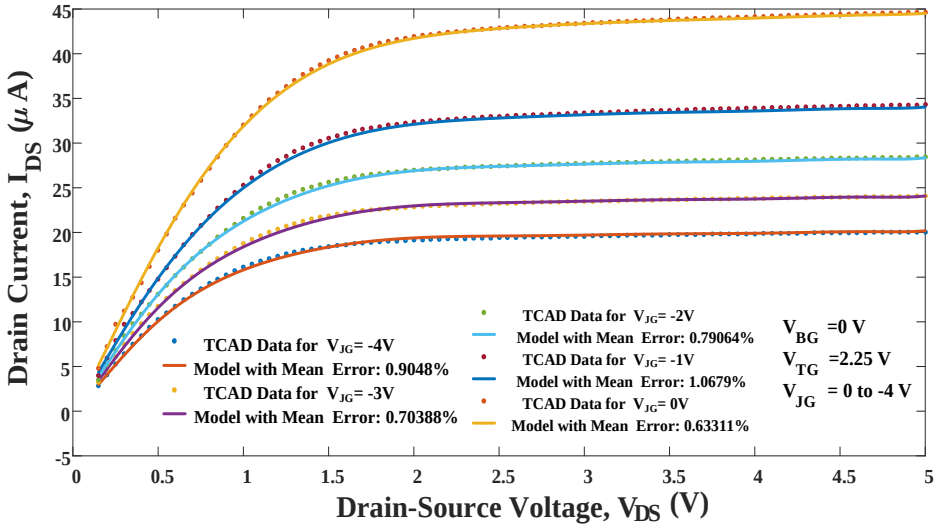


Figure 4.38: Comparison between isolines of test data and regression model (order of V_{DS}, V_{BG}, V_{TG}, V_{JG} respectively 10, 4, 5 and 5) for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment arranged from bottom to top.

V_{DS}, V_{BG}, V_{TG} and V_{JG} are kept as 10, 4, 5 and 5, respectively, in the model equation. From the graph and the values of corresponding mean relative error, it is clear that the model fits reasonably well for all the isolines.

4.4.2.2 Experimental Data from an *n*-Channel G^{4}FET (Device 2)

An *n*-channel G^{4}FET was fabricated in a conventional partially-depleted SOI (PDSOI) technology with a width of 0.4 µm and a length of 0.9 µm. The experimental data acquired from this device is used to generate regression polynomial model. Here again, both junction-gates are tied together for simplicity.

For data generation, the top-gate voltage V_{TG} was swept from -3 V to 3 V in 0.05 V increment, the junction-gate voltage V_{JG} was swept from -4 to -1 V in 1 V increment and the bottom-gate voltage V_{BG} was swept from -5 V to 5 V in 2 V increment. The drain-source voltage, V_{DS} was fixed at 50 mV. Based on this data, a regression polynomial model is used to express the drain current, I_D as a function of three independent variables V_{TG}, V_{BG} and V_{JG}. The model was then tested against a different set of experimental data.

Figure 4.39 to Figure 4.42 show the drain current versus the top-gate voltage and the corresponding relative error for a particular test bias (V_{BG} = 0 V, V_{DS} = 50 mV and V_{JG} = -1 V). Here, the order of V_{TG} and V_{BG} are varied for observing the effect of model order on accuracy. As expected, the error is reduced with an increase in the model order. Figure 4.43 shows the isolines for different V_{BG} values with corresponding relative error. The order of variables V_{BG}, V_{TG} and V_{JG} are selected as 3, 8 and 2, respectively for creating the isolines. The graph and the values of relative error show that the model agrees reasonably well with experimental data.

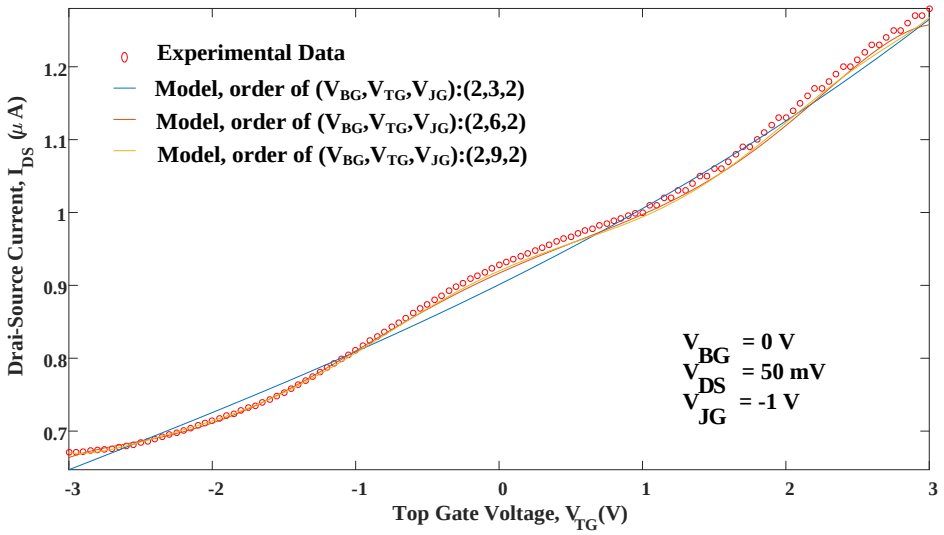


Figure 4.39: Comparison of I_{DS}-V_{TG} between experimental data and regression model for different orders of V_{TG} with the order of V_{BG} and V_{JG} fixed at 2.

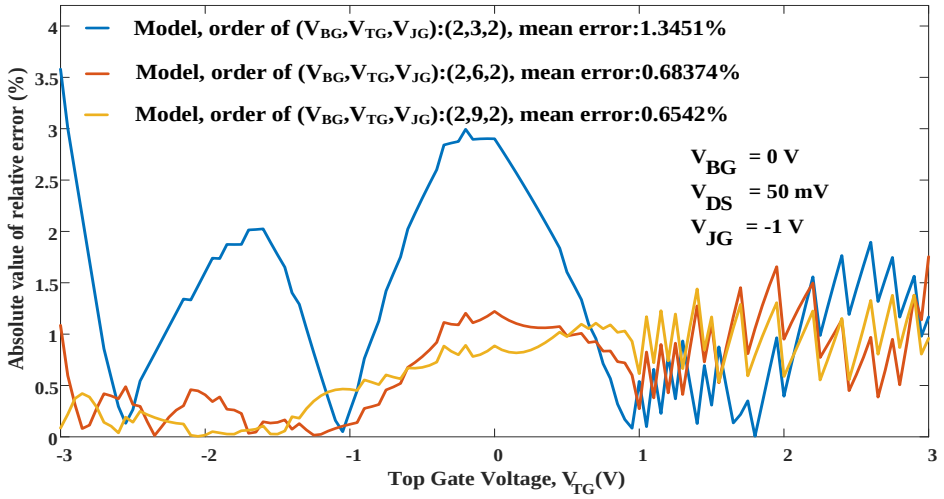


Figure 4.40: Relative error between experimental data and regression model for different orders of V_{TG} with the order of V_{BG} and V_{JG} fixed at 2.

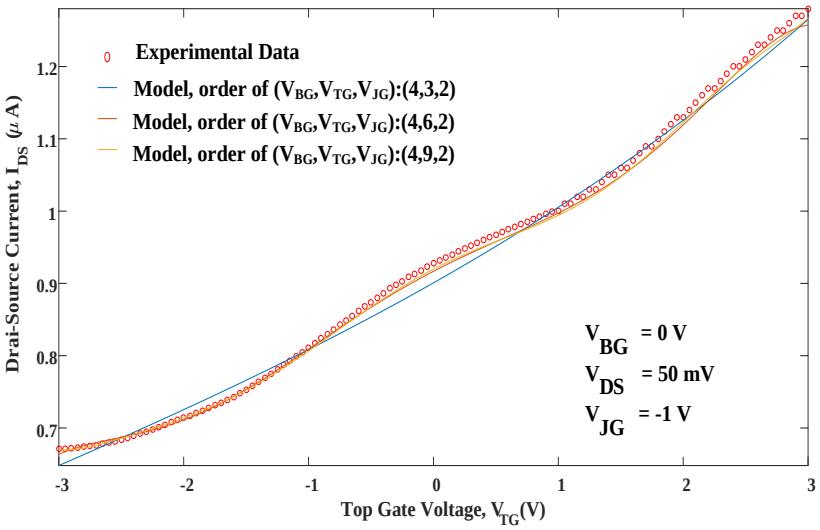


Figure 4.41: Comparison of I_{DS} -V_{TG} between experimental data and regression model for different orders of V_{TG} with the order of V_{JG} and V_{BG} fixed at 2 and 4, respectively.

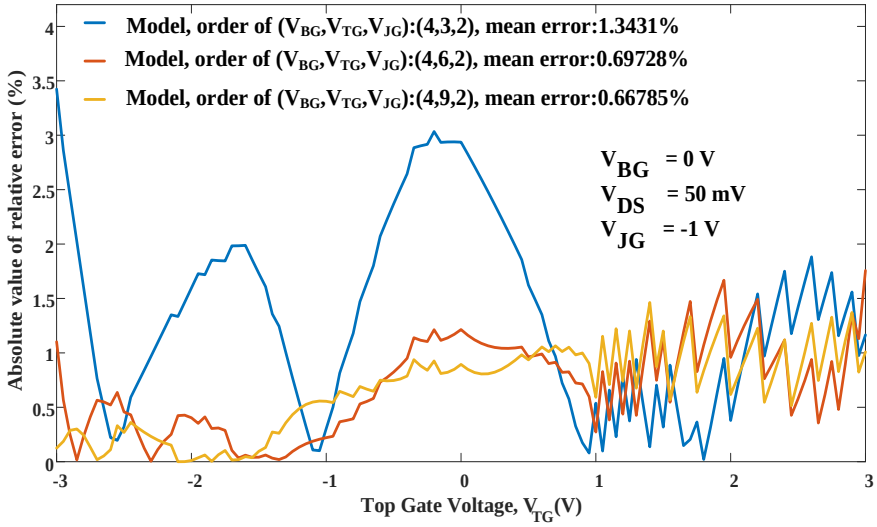


Figure 4.42: Relative error between experimental data and regression model for different orders of V_{TG} with the order of V_{JG} and V_{BG} fixed at 2 and 4, respectively.

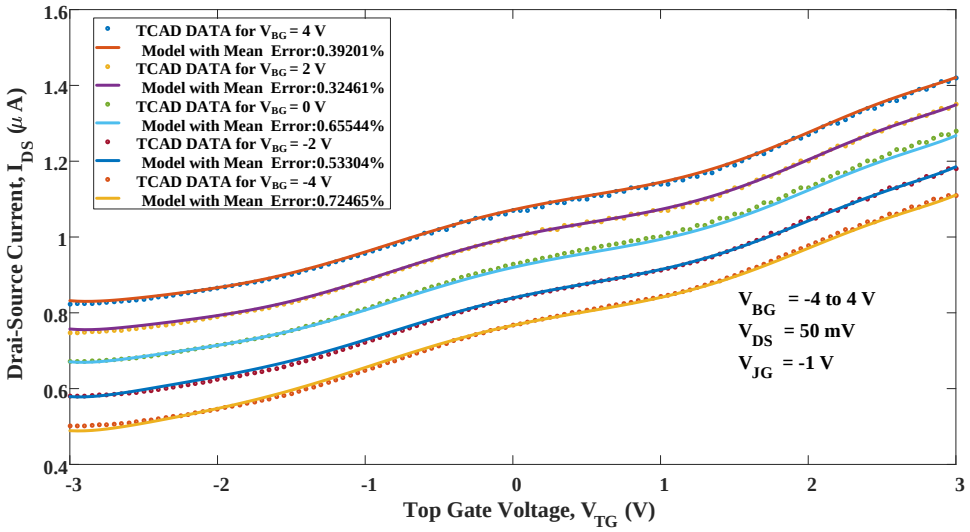


Figure 4.43: Comparison between isolines of test data and regression model (order of V_{BG}, V_{TG}, V_{JG} respectively 3, 8 and 2) for different bottom-gate voltages ranging from -4 V to 4 V in 2 V increment arranged from bottom to top.

4.4.2.3 A *p*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 3)

A *p*-channel G^{4}FET has been built and simulated with TCAD Sentaurus. The device geometry, the doping levels in different regions and the biasing conditions used for model development are given in Table 4.2. Here, V_{JG} stands for the voltage applied at both the junction-gates since the junction-gates were tied together for all the simulations. Based on the *I-V* data extracted from TCAD, a multivariate regression polynomial model is developed for the drain current, I_D as a function of four independent variables V_{SD}, V_{TG}, V_{BG} and V_{JG}.

A set of independent test data is used to validate the developed model. The drain current versusthe source-drain voltage and the corresponding relative error are shown in

Figure 4.44 to Figure 4.47, for a particular test bias (V_{BG} = 0 V, V_{TG} = -2.25 V and V_{JG} = 2 V). Here, the order of V_{BG} and V_{JG} are kept fixed at 4 and 5, respectively. The order of V_{SD} has

been changed from 6 to 10 and the order of V_{TG} has been changed from 4 to 5 to observe the effect of order on model accuracy.

Isolines for different values of V_{JG} are shown in Figure 4.48. In this figure, the order of V_{SD}, V_{BG}, V_{TG} and V_{JG} have been chosen to be 10, 4, 5 and 5, respectively. The top-gate and the bottom-gate are biased at -2.25 V and 0 V, respectively. The junction-gate voltage is swept from 0 V to 4 V. From the graph and the corresponding mean relative error values, it is clear that the model matching is quite good for different biasing conditions.

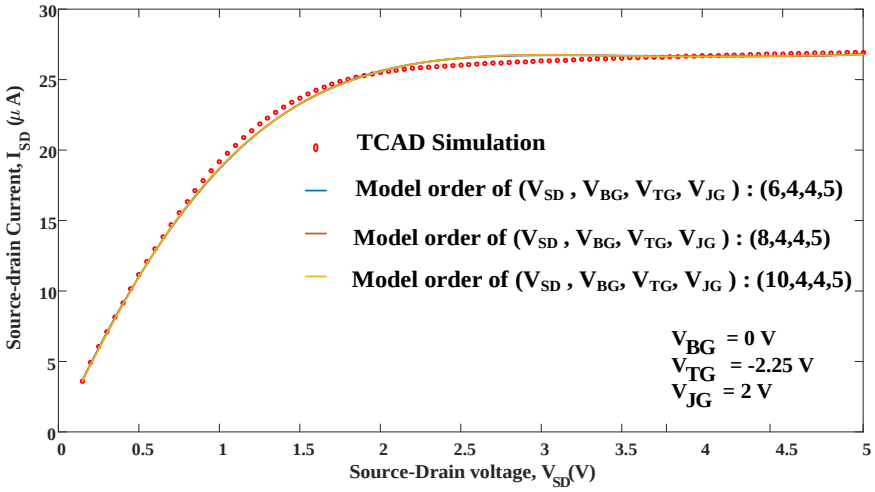


Figure 4.44: Comparison of I_{SD}-V_{SD} between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 4 for a *p*-channel G^{4}FET.

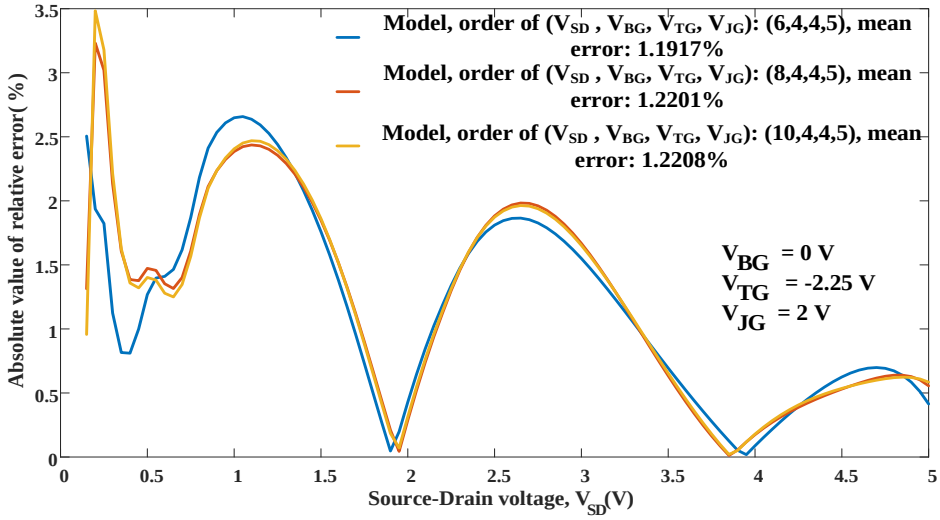


Figure 4.45: Relative error between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 4 for a *p*-channel G^{4}FET.

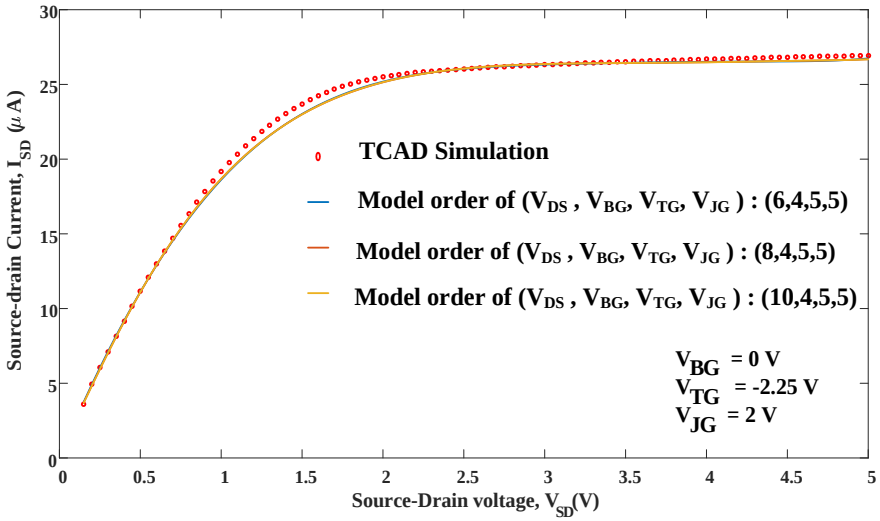


Figure 4.46: Comparison of I_{SD}-V_{SD} between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 5 for a *p*-channel G^{4}FET.

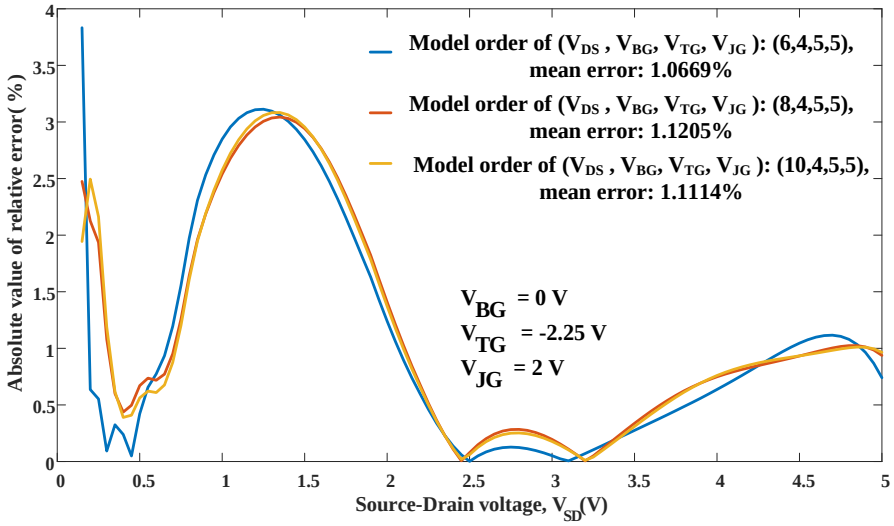


Figure 4.47: Relative error between TCAD data and regression model for different orders of V_{SD} with order of V_{TG} fixed at 5 for a *p*-channel G^{4}FET.

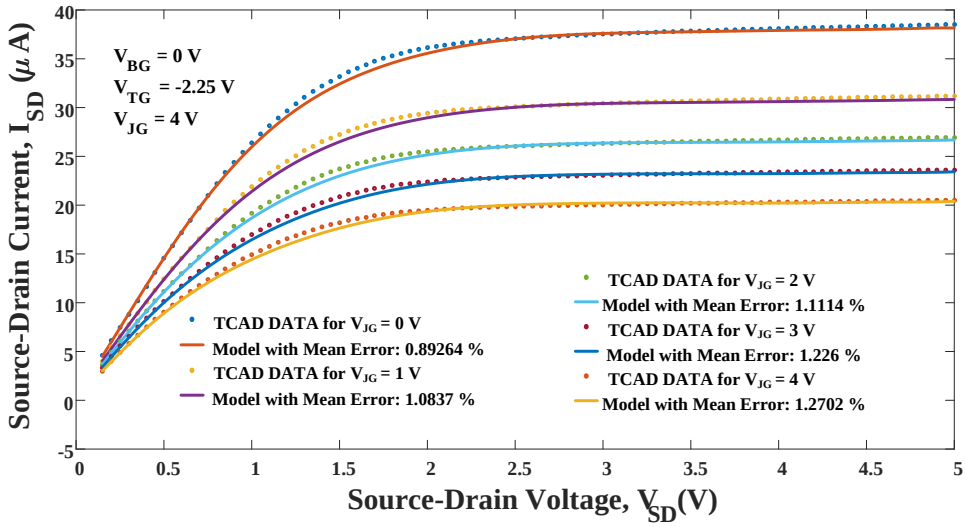


Figure 4.48: Comparison between isolines of test data and regression model for different junction-gate voltages ranging from 0 V to 4 V in 1 V increment (Device 3).

4.4.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4)

Device 4 is a *p*-channel G^{4}FET fabricated in a conventional 0.35 µm partially-depleted SOI (PDSOI) technology with a width of 0.35 µm and a length of 3.4 µm. Experimental source-drain current data were acquired for a range of biasing conditions. The source-drain voltage V_{SD} was fixed at 50 mV, the bottom-gate voltage V_{BG} was fixed at 0 V, the junction-gate voltage V_{JG} was swept from 4 V to 0 V in -0.4 V decrement and the top-gate voltage V_{TG} was swept from -3.3 V to 0 V in 0.033 V increment. Using these data, a regression polynomial model is developed to express the source-drain current, I_{SD} as a function of two independent variables V_{TG} and V_{JG}. The model is then verified against a different set of test data. The source-drain current versus the top-gate voltage and the corresponding relative error for a particular test bias (V_{SD} = 50 mV, V_{BG} = 0 V, V_{JG} = 1 V) are shown in Figure 4.49 to Figure 4.52. Here, the order of V_{JG} and V_{TG} are varied to show the effect of order on model accuracy.

Figure 4.53 shows isolines for different values of V_{JG} with the order of V_{TG} and V_{JG} fixed at 9 and 6, respectively. The bottom-gate voltage and the source-drain voltage are fixed at 0 V and 50 mV. The junction-gate bias is swept from 0.2 V to 1.4 V in 0.4 V increment. As evident from the graphs and corresponding errors, the regression model matches very well with experimental data for all the isolines.

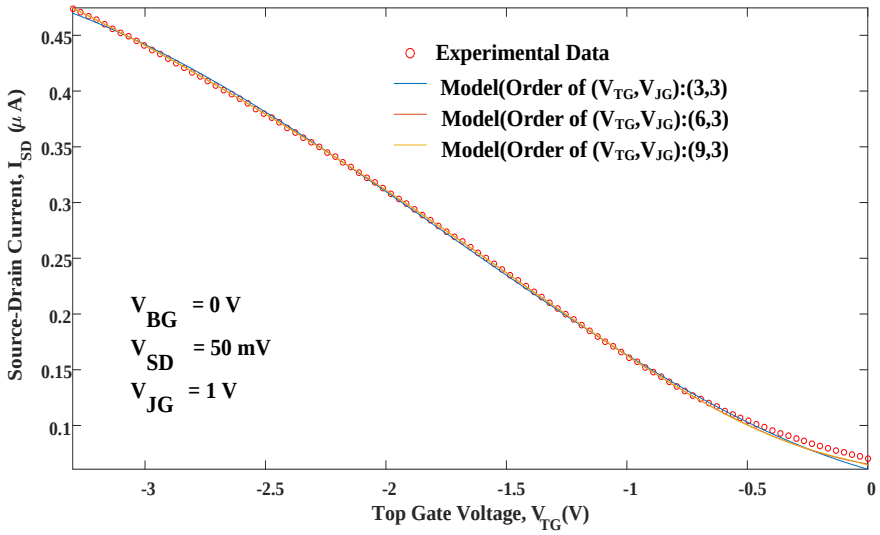


Figure 4.49: Comparison of I_{SD}-V_{TG} between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 3.

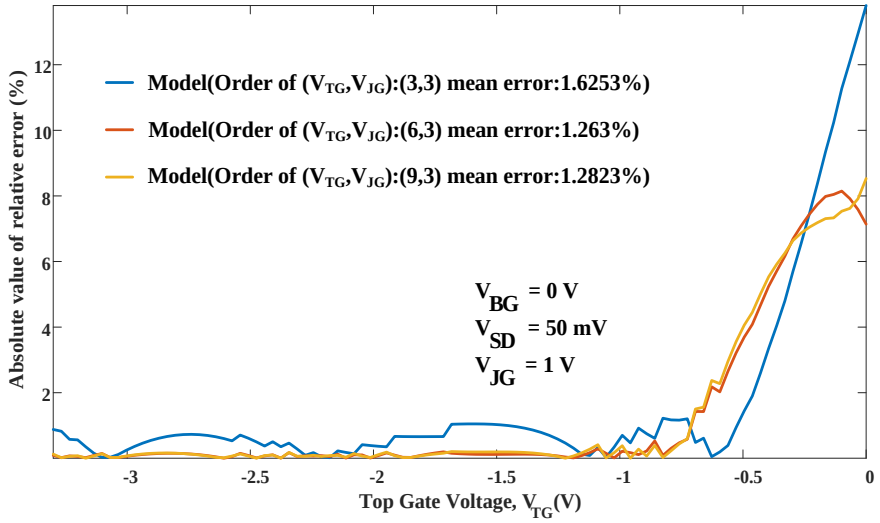


Figure 4.50: Relative error between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 3.

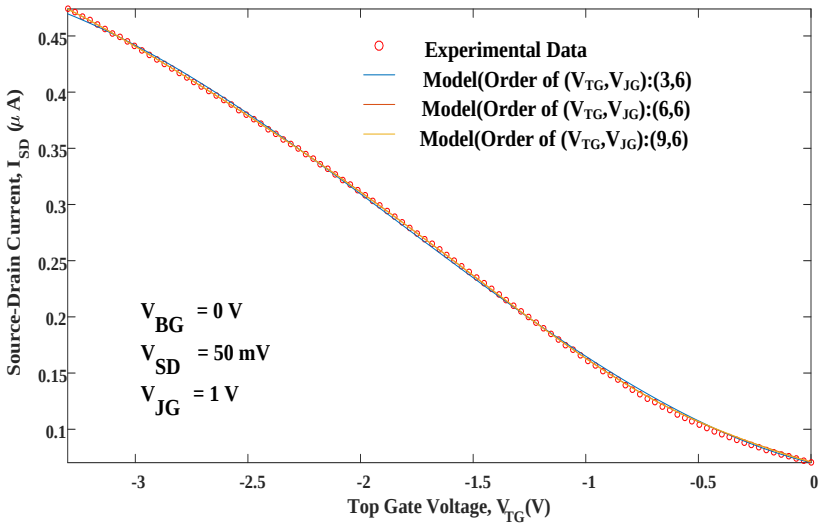


Figure 4.51: Comparison of I_{SD}-V_{TG} between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 6.

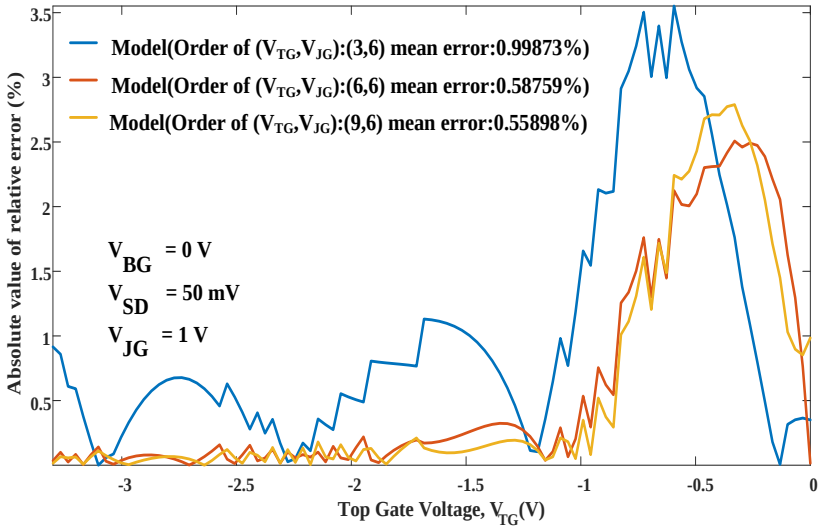


Figure 4.52: Relative error between p-G^{4}FET experimental data and regression model for different orders of V_{TG} with the order of V_{JG} fixed at 6.

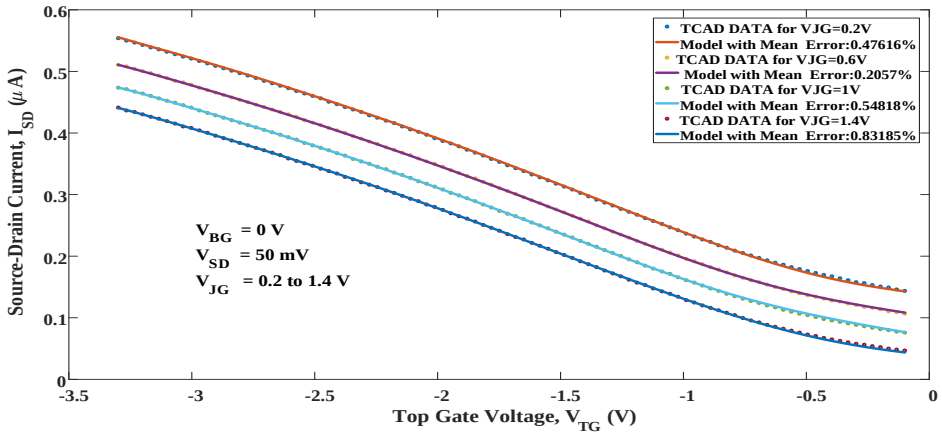


Figure 4.53: Comparison between isolines of test data and regression model for different junction-gate voltages ranging from 0.2 V to 1.4 V in 0.4 V increment (Device 4).

4.4.2.5 Modeling of Device Geometry

Geometric dimensions i.e. width, length and epi silicon thickness of G^{4}FET can be treated as independent variables similar to the terminal voltages. Then the resulting regression model will include additional model terms including geometric variables. Here, an *n*-channel G^{4}FET *I-V* data is obtained from TCAD Sentaurus for different widths (*W*) and lengths (*L*) with *W* and *L* being swept from 0.25 µm to 0.5 µm and from 0.8 µm to 1.8 µm, respectively. Then multivariate regression polynomial model is used to develop an expression for drain current as a function of V_{DS}, *W* and *L*.

This model is validated using data from a different test device within the training geometry range. The current-voltage characteristics and corresponding relative errors are shown in Figure 4.54 and Figure 4.55. The top-gate bias is fixed at 4 V and length and width are chosen to be 1.5 µm and 0.35 µm. Isolines for different width are shown in Figure 4.56. The mean relative error shows good matching for all the isolines.

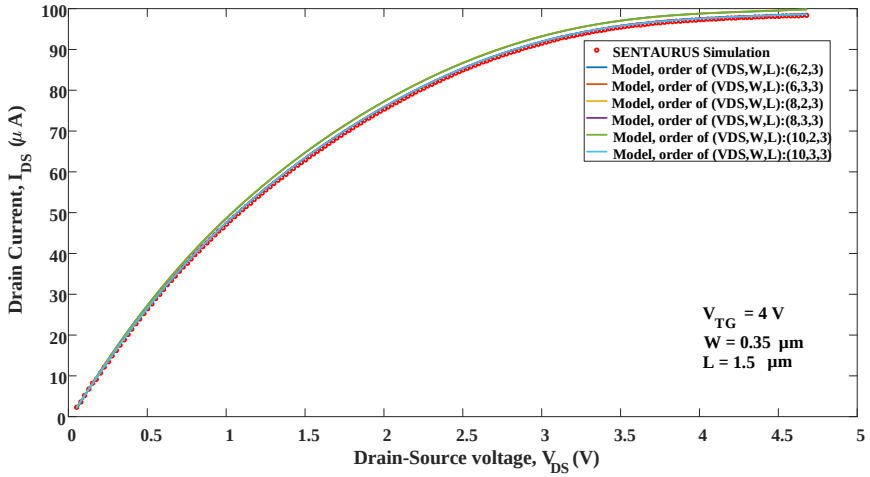


Figure 4.54: Comparison of drain current versus drain-source voltage between TCAD data and regression model for different orders of V_{DS} for test geometry.

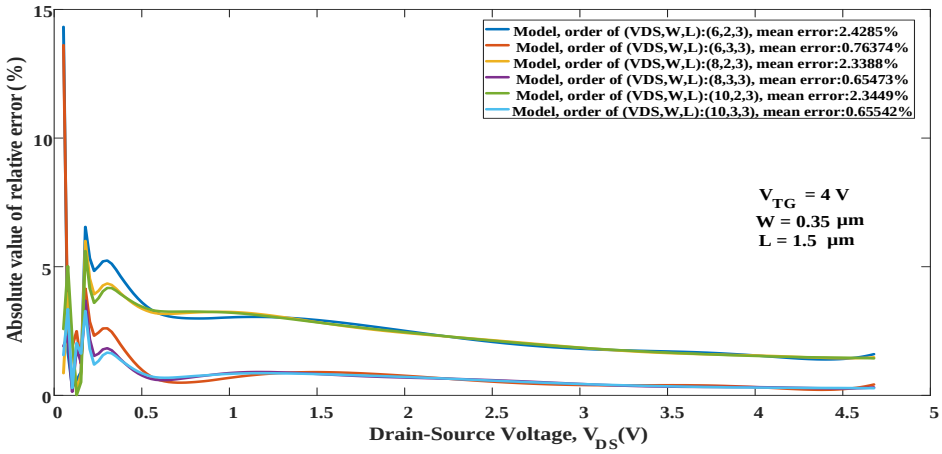


Figure 4.55: Relative errors between TCAD data and regression model for different orders of V_{DS} for test geometry.

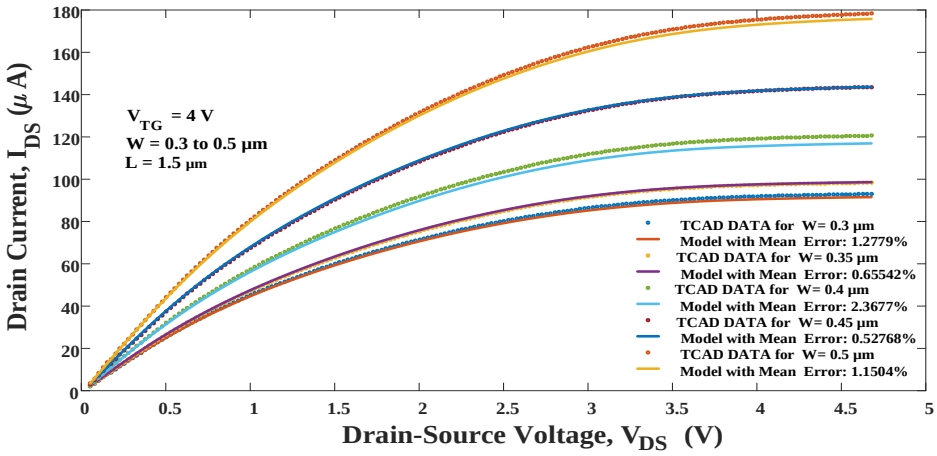


Figure 4.56: Comparison between TCAD data and regression model of isolines for different widths ranging from 0.3 to 0.5 µm in .05 µm increment arranged from bottom to top.

4.4.2.6 First Order Characteristics (Device Transconductance and Drain Output Resistance)

To show the continuity and smoothness of current-voltage curve, plots of first order characteristics such as transconductance and drain output resistance are shown in Figure 4.57 and Figure 4.58, respectively. Figure 4.57 shows a comparison between the experimental data and the regression model of different orders for transconductance versus top-gate voltage for Device 4. Figure 4.58 shows the drain output resistance versus the drain-source voltage for different model orders with vertical axis in logarithmic scale.

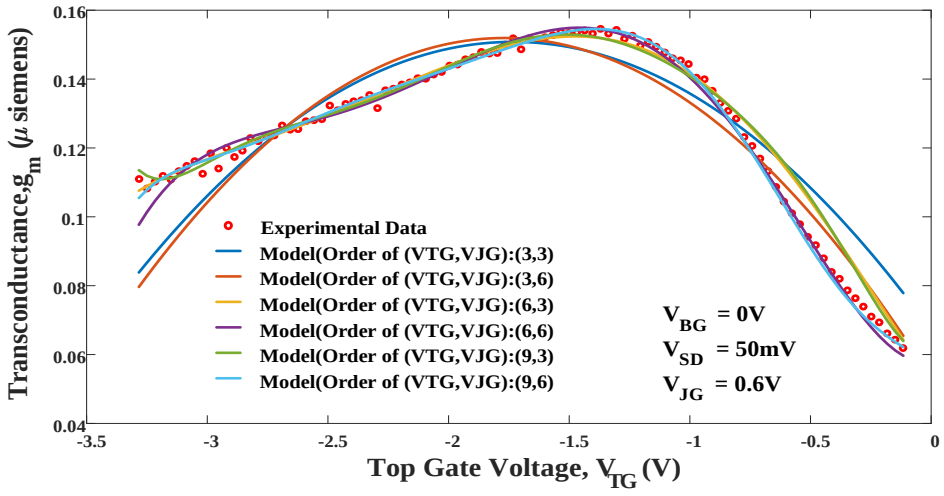


Figure 4.57: Comparison of g_m–V_{TG} between experimental data and regression model for different orders of V_{TG} and V_{JG} for a *p*-channel G^{4}FET (Device 4).

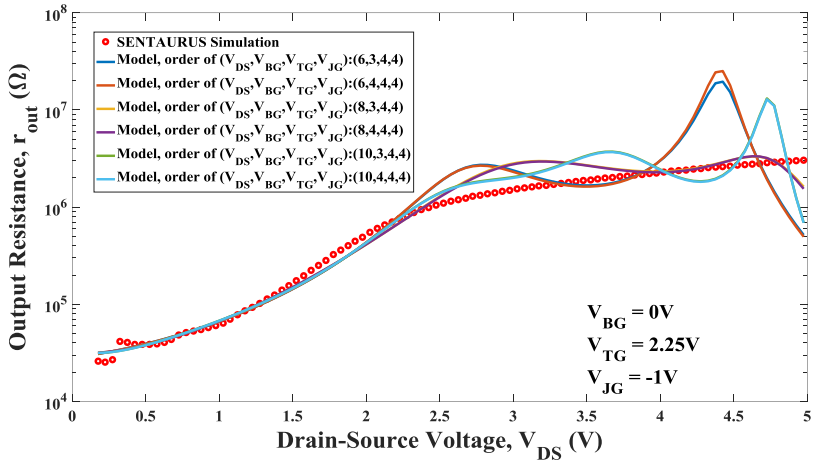


Figure 4.58: Comparison of r_{out} - V_{DS} between TCAD data and regression model for different orders of V_{DS} and V_{BG} for an *n*-channel G^{4}FET (Device 1).

4.4.3 Circuit Simulator (SPICE and Spectre™) Implementation

Models of both *n*-channel and *p*-channel G⁴FETs have been created using multivariate regression polynomial for circuit simulator implementation. G⁴FET transistor has been modelled as a sub-circuit containing a behavioural current source between its drain and source terminals and its current is modelled as a function of the terminal voltages V_{TS}, V_{BS}, V_{JS} and V_{DS} (Figure 4.17). This block can be implemented in a SPICE simulator for simulating any circuit using G⁴FET. Here, the junction-gates are tied together for simplicity.

The developed model has also been implemented in Cadence™ which uses Spectre™ simulator. The behavioral model for Cadence™ implementation has been written in Verilog A.

Table 4.4: Computational Complexity of Regression Model

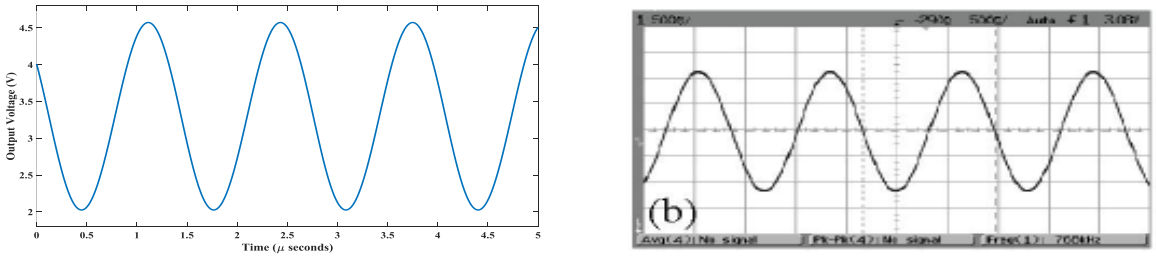
Order of V_{DS}	**Order of V_{BG}**	**Total Number of Terms (N_{terms})**	**Total Number of Required Addition/ Subtraction (N_{add})**	**Total Number of Required Multiplication (N_{mul})**
4	3	500	499	3251
6	3	700	699	5251
8	3	900	899	7651
4	5	750	749	5626
6	5	1050	1049	8926
8	5	1350	1349	12826

Most simulators solve a system of circuit equations using Newton-Raphson algorithm which requires a continuous function with continuous first derivative. The regression polynomial is infinitely continuous and it satisfies these requirements nicely. The computational burden on the

host simulator program depends heavily on the evaluation of the regression polynomial for each set of four terminal voltages. A list of required terms, additions and multiplications for the developed model for Device 1 (*n*-channel G^{4}FET) is shown in Table 4.4. Here, the order of the independent variables V_{TG} and V_{JG} are kept fixed at 4. An increase in order usually improves the accuracy accompanied with a sharp increase in computational cost as evident from Table 4.4.

4.4.4 Results from G^{4}FET Circuit Simulation

The developed model is used to simulate two circuits containing G^{4}FETs. The first one is a LC oscillator using negative differential resistance (NDR) circuit made of G^{4}FETs. It was described in section 4.2.4. A G^4-NDR with a LC tank load works as an LC oscillator (Figure 4.20). This oscillator circuit has been previously demonstrated [34] with V_{DD} = 3.3 V, L= 0.4 mH, C = 110 pF.



a b

Figure 4.59: (a) Output from SPICE simulator, (b) experimental result.

The developed model is written in VerilogA to simulate this circuit using SPECTRE^{TM} simulator in Cadence^{TM} and the result is shown in Figure 4.59. It shows good agreement with the experimental result [35]. The simulated oscillator output has 2.54 V peak-to-peak amplitude with

a frequency of 763 kHz compared to the experimental result of 2.5 V peak-to-peak amplitude with a frequency of 768 kHz with a relative error of 1.6 % in amplitude.

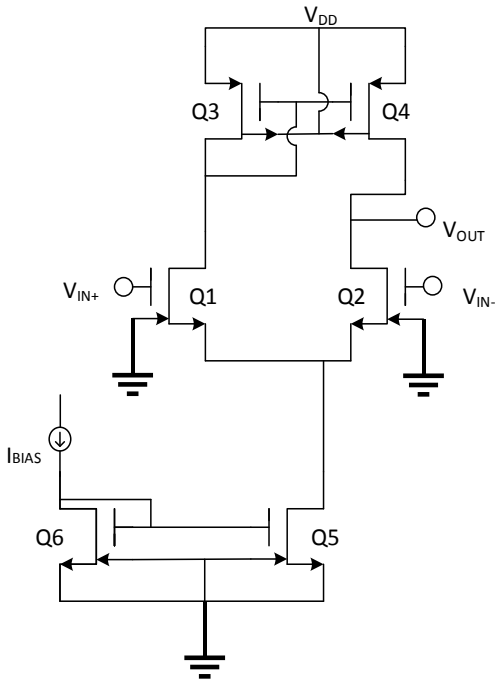


Figure 4.60: Schematic of high voltage G^{4}FET differential amplifier (Q 1,2: 0.3 µm ×10/2.4 µm, V_{JG} = 0 V, V_{BG} =0 V; Q 3,4: 0.35 µm ×2 /10 µm, V_{JG} = 0 V, V_{BG} = 0 V; Q 5,6: 0.3 µm×10/2.4 µm, V_{JG} =V_{DD}, V_{BG} = 0 V).

The second circuit is a high voltage differential amplifier first demonstrated in [36]. It is simulated using a SPICE simulator. Compared to regular MOSFETS, G^{4}FETs can sustain much higher voltages in the same process technology. The circuit has a current mirror for biasing, designed using two *n*-channel G^{4}FETs and a differential pair, implemented using a pair of *n*-channel G^{4}FETs. A pair of *p*-channel G^{4}FETs is used as active load. The schematic is shown in Figure 4.60. Here, the junction-gates are connected together and shown as a single gate and the unused bottom-gate is not shown for simplification.

The high voltage (HV) differential amplifier in [36] is used in a non-inverting unity gain configuration to an input of 1 V peak-to-peak square wave of 1 KHz frequency. The circuit has been simulated with the developed regression model and the result in Figure 4.61 with an output of 0.97 V_{p-p} shows good agreement with the experimental result of 1 V_{p-p} with a relative error of 3%.

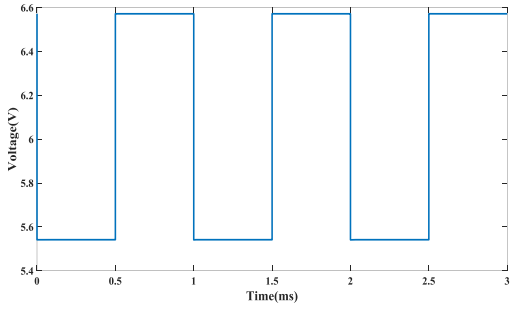


Figure 4.61: Output of G^{4}FET Differential amplifier (0.97 V_{p-p} compared to experimental value of 1 V_{p-p}) in non-inverting unity gain configuration (V_{DD} = 10 V, V_{in} = 1 V_{p-p} square wave with 6 V offset).

4.5 Numerical Method 4 (Multidimensional Linear and Cubic Spline Interpolation Model)

Spline interpolation is a special case of interpolation where the interpolant is a piecewise polynomial called spline. This method is often preferable to interpolation using a single high degree interpolant polynomial used in the previous three model derivations. For a regular monotonic data set, low degree spline polynomials can reduce error and avoid Runge's phenomenon i.e. occurrence of oscillation between points, especially at the boundary, when high degree polynomials are used. In this section, multidimensional linear and cubic spline polynomials

are used for the model development. Multivariate spline formulation has been chosen for modeling G^4FET since it can ensure continuity of the function and its derivatives, retain monotonicity, provide accurate results and can be developed from measured or simulation data without difficult analytical expression [107, 108].

4.5.1 Model Formulation

4.5.1.1 Linear Spline Model

Given n points in the plane, (x_k, y_k), $k = 1,2, \ldots, n$ with distinct x_k's, there is a unique polynomial in x of degree less than n whose graph passes through the points. If two successive points are (x_k,y_k) and (x_{k+1}, y_{k+1}), then the kth interval between these two points can be interpolated using a straight line. Therefore, for n data points, we will have $n-1$ piecewise straight lines. Three quantities, k, s and δ are now defined. The interval index k is such that, $x_k \leq x < x_{k+1}$. The local variable, s is $s = x - x_k$. The first divided difference is $\delta_k = (y_{k+1} - y_k)/(x_{k+1} - x_k)$. The interpolant can be written in terms of these quantities as,

$$P(x) = y_k + s\delta_k \tag{4.20}$$

The piecewise linear interpolant is simple to develop but it has a first order continuity problem. It is a continuous function of x, but its first derivative, $P'(x)$, is not continuous. The derivative has a constant value, δ_k, on each subinterval and jumps at the breakpoints. Hence, instead of linear spline, most popular spline applications use piecewise cubic spline interpolation polynomials with continuous derivatives.

4.5.1.2 Cubic Spline Model

Let, h_k denote the length of the kth subinterval i.e. $h_k = x_{k+1} - x_k$; then, $\delta_k = (y_{k+1} - y_k)/ h_k$. Let, d_k denote the slope of the interpolant at x_k i.e. $d_k = P'(x_k)$.

The cubic spline polynomial on the interval $x_k \leq x \leq x_{k+1}$, can be written in terms of local variables $s = x - x_k$ and $h = h_k$ as,

$$P(x) = \frac{3hs^2 - 2s^3}{h^3} y_{k+1} + \frac{h^3 - 3hs^2 + 2s^3}{h^3} y_k + \frac{s^2(s-h)}{h^2} d_{k+1} + \frac{s(s-h)^2}{h^2} d_k \quad (4.21)$$

This is a cubic polynomial that satisfies four interpolation conditions; two on the function values and two on the derivative values so that,

$P(x_k) = y_k$, $P(x_{k+1}) = y_{k+1}$, $P'(x_k) = d_k$, $P'(x_{k+1}) = d_{k+1}$

Now the values of d_k's can be estimated to make sure that second derivative is also continuous and this added constraint leads to the condition

$$h_k d_{k-1} + 2(h_{k-1} + h_k) d_k + h_{k-1} d_{k+1} = 3(h_k \delta_{k-1} + h_{k-1} \delta_k) \quad (4.22)$$

If knots are equally spaced, equation (4.22) becomes

$$d_{k-1} + 4d_k + d_{k+1} = 3\delta_{k-1} + 3\delta_k \quad (4.23)$$

The above approach applied at each interior knot x_k, $k = 2, \ldots, n-1$ will provide $n-2$ equations involving the n unknowns d_k. A different "not-a-knot" approach is used near the ends of the interval. A single cubic polynomial is used on the first two subintervals, $x_1 \leq x \leq x_3$, and on the last two subintervals, $x_{n-2} \leq x \leq x_n$. With the two end conditions included, n linear equations result in n unknowns. Solution of this system of linear equation gives the desired estimates of d_k.

The same analysis can be extended for multiple dimensions using tensor product formulation. The interpolated value at a desired point is based on a cubic interpolation of the values at neighbouring knot points in each respective dimension. Any number of variables can be chosen

for multidimensional spline interpolation. In this work, V_{DS} (drain-source voltage), V_{TG} (top-gate voltage), V_{BG} (bottom-gate voltage), V_{LJG} (left junction-gate voltage) and V_{RJG} (right junction-gate voltage) have been used as independent terminal voltages for spline interpolation. Also, the geometric variables W (width) and L (length) are included in one model as independent variables to show the inclusion of device geometry in the modeling process. Of course, depending on the application, one might choose to use the same modeling approach using different variables such as terminal capacitances, temperature etc.

4.5.2 Model Validation

Experimental and TCAD Sentaurus data of the current-voltage characteristics have been obtained for both *p*-channel and *n*-channel G^{4}FET transistors. Spline interpolation technique has been used on these data to model corresponding devices. Predictions from the model are then tested against another set of test data.

4.5.2.1 An *n*-Channel G^{4}FET Simulated Using TCAD Sentaurus (Device 1)

Device 1 is an *n*-channel G^{4}FET created in TCAD Sentaurus. Table 4.1 includes the information pertinent to test data i.e. device geometry, the doping levels and the biasing conditions for this device. Lateral junction-gates are tied together for this validation and V_{JG} here denotes the common voltage applied at both junction-gates. Multivariate linear spline and cubic spline models for device 1 have been generated using these *I-V* data extracted from TCAD. Here, the drain current, I_{DS} is a function of four independent variables V_{DS}, V_{TG}, V_{BG} and $V_{JG.}$

In Figure 4.62 and Figure 4.63, isolines are shown for different values of junction-gate voltages ranging from -4 V to 0 V, while keeping the bottom substrate voltage V_{BG} fixed at 0 V and top-gate voltage fixed at 2.25 V for linear and cubic spline model, respectively. The reverse bias depletion from junction-gate reduces conduction channel width as well as increases effective top-gate threshold voltage. Thus, the drain current gradually decreases as this reverse bias increases on the junction-gates. The bottom-gate is depleted and the top-gate is accumulated for this bias. Therefore, the current is mostly due to an accumulated *n*-channel near the top oxide gate surface. From the graph and the values of corresponding mean relative error, it is clear that the model fits reasonably well for all the isolines. A comparison between Figure 4.62 and Figure 4.63 shows a significant improvement in the accuracy at the cost of additional computational complexity, as we move from linear to cubic spline.

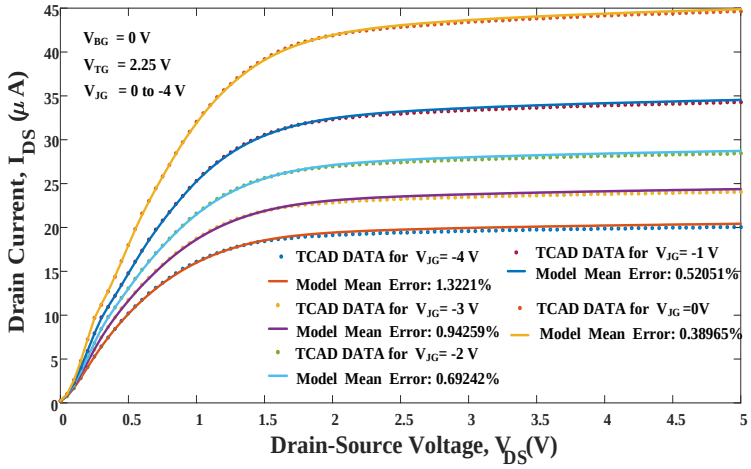


Figure 4.62: Comparison between isolines of test data and linear spline model (Device 1) for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment.

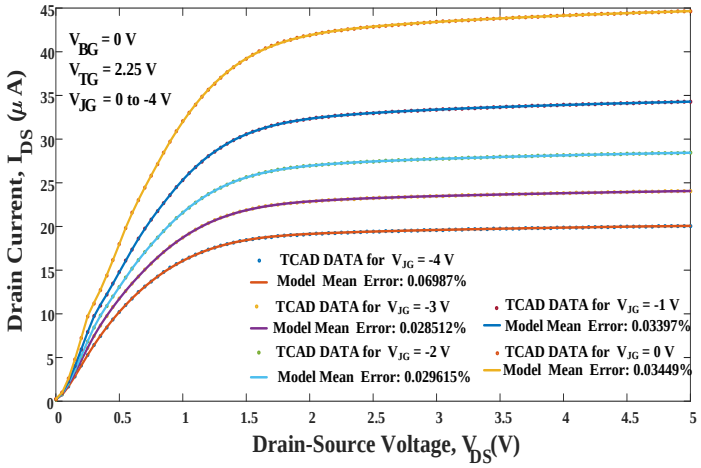


Figure 4.63: Comparison between isolines of test data and cubic spline model (Device 1) for different junction-gate voltages ranging from -4 V to 0 V in 1 V increment.

4.5.2.2 Experimental Data from an *n*-Channel G^{4}FET (Device 2)

A conventional partially-depleted SOI (PDSOI) technology was used to manufacture an *n*-channel G^{4}FET with a width of 0.4 µm and a length of 0.9 µm. The experimental current-voltage data from this device is used to build a linear and a cubic spline interpolation models. The lateral junction-gates are tied together with a common voltage.

The test data was generated with the top-gate voltage V_{TG} being swept from -3 V to 3 V in 0.05 V increment, the bottom-gate voltage V_{BG} being swept from -5 V to 5 V in 2 V increment, the junction-gate voltage V_{JG} being swept from -1 to -4 V in 1 V decrement and the drain-source voltage, V_{DS} was fixed at 50 mV. Spline interpolation technique is then used to model I_{DS} as a function of three independent variables V_{TG}, V_{BG} and V_{JG}. A set of experimental data using different biasing conditions within the training data range is used for model verification.

Figure 4.64 and Figure 4.65 show the isolines for different V_{BG} values with corresponding relative error for linear spline and cubic spline model, respectively. The junction-gates are reverse

biased at -1 V and drain-source voltage, V_{DS} is kept 50 mV. The bottom-gate voltage is swept from -4 V to 4 V in 2 V increment. The range of the top-gate voltages starts with inversion, goes through depletion and ends in strong accumulation. The graphs and the values of relative error show reasonably good agreement between the model prediction and the experimental data for both linear spline and cubic spline models.

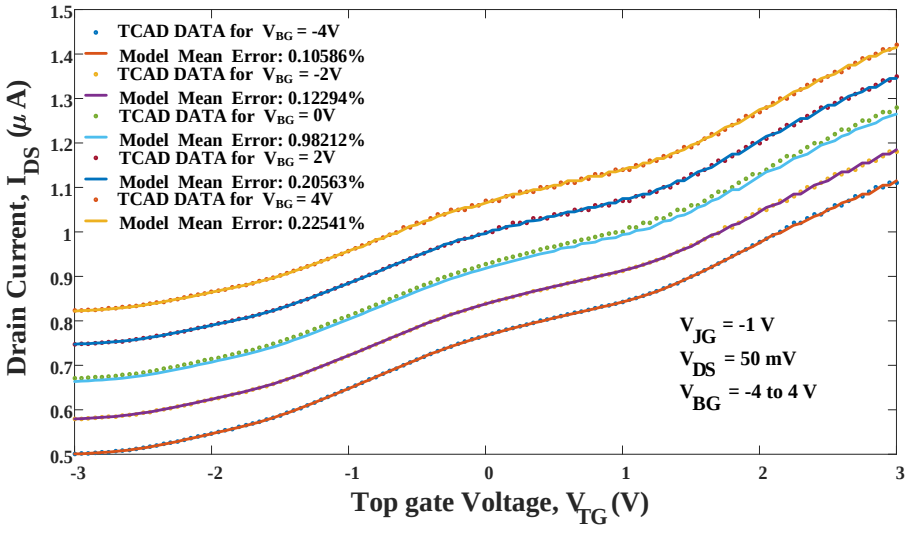


Figure 4.64: Comparison between isolines of test data and linear spline model (Device 2) and relative error for varying bottom-gate voltages from -4V to 4V in 2V increment arranged from bottom to top.

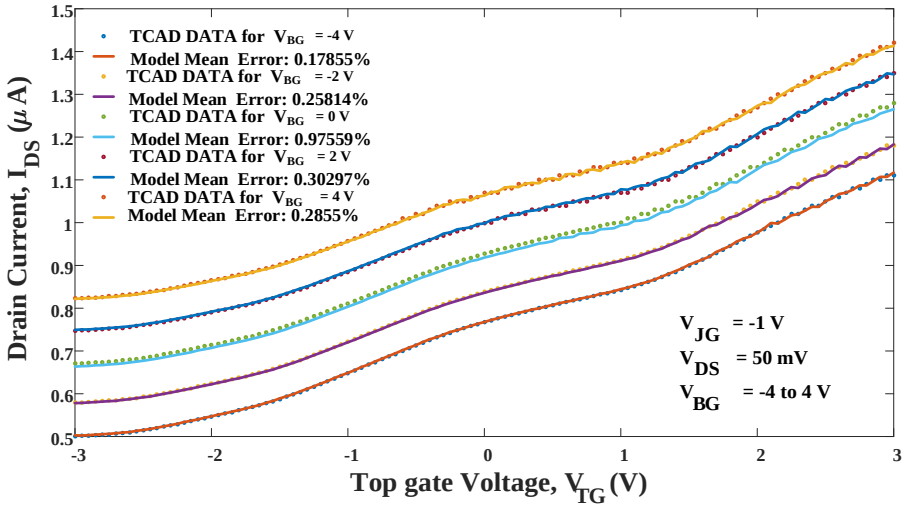


Figure 4.65: Comparison between isolines of test data and cubic spline model (Device 2) and relative error for varying bottom-gate voltages from -4 V to 4 V in 2 V increment arranged from bottom to top.

4.5.2.3 A *p*-Channel G^{4}FET Simulated with TCAD Sentaurus (Device 3)

Device 3 is a *p*-channel G^{4}FET built and simulated with TCAD Sentaurus. The biasing voltages used for model development along with the device geometry and the doping levels in different regions are given in Table 4.2. Here, V_{JG} is the voltage applied at both the junction-gates. Linear and cubic spline models have been used on these I-V data to develop drain current, I_{SD} as a function of four independent variables V_{SD}, V_{TG}, V_{BG} and V_{JG}. A set of test data taken under different bias conditions is used for validation of the developed model.

Isolines of drain current versus source-drain voltage for different values of V_{JG} are shown in Figure 4.66 and Figure 4.67 for linear and cubic spline model, respectively. The top- and the bottom-gate were biased at -2.25 V and 0 V, respectively. The current gradually decreases as the reverse bias increase at the junction-gates from 0 V to 4 V. From the graphs and the corresponding

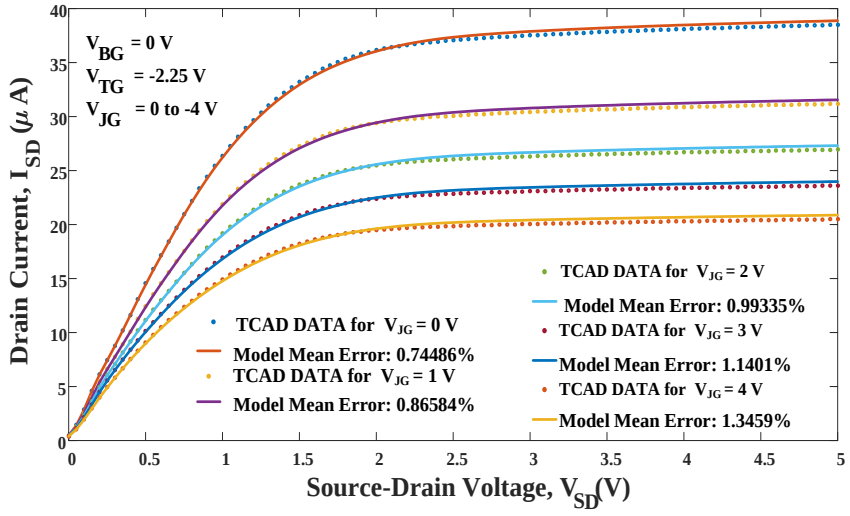


Figure 4.66: Comparison of I_{SD} - V_{SD} between TCAD test data and linear spline model (Device 3) for different junction-gate voltages ranging from 0 V to 4 V.

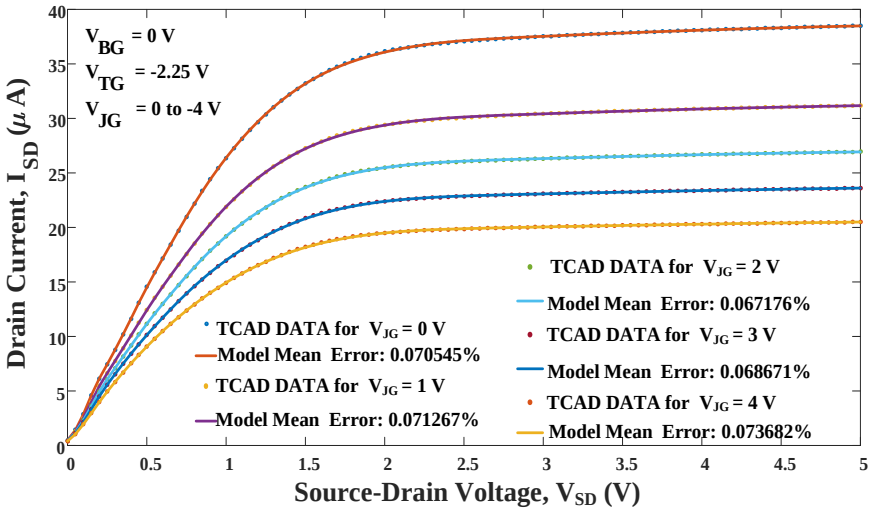


Figure 4.67: Comparison of I_{SD} - V_{SD} between TCAD test data and cubic spline model (Device 3) for different junction-gate voltages ranging from 0 V to 4 V.

mean relative error values, it is clear that the model prediction is quite good and a significant accuracy improvement can be observed going from linear to cubic spline model.

4.5.2.4 Experimental Data from a *p*-Channel G^{4}FET (Device 4)

A *p*-channel G^{4}FET fabricated in a conventional 0.35 µm PDSOI technology with a width of 0.35 µm and a length of 3.4 µm is used as the fourth device for model verification. The source-drain voltage V_{SD} was fixed at 50 mV, the bottom-gate voltage V_{BG} fixed at 0 V and the junction-gate voltage V_{JG} was changed from 4 V to 0 V in -0.4 V decrement and the top-gate voltage V_{TG} was swept from -3.3 V to 0 V in 0.033 V increment. Based upon these data, linear and cubic spline models are developed to express the source-drain current, I_{SD} as a function of two independent variables, V_{TG} and V_{JG}. An independent set of test data is then used to test the predictive ability of

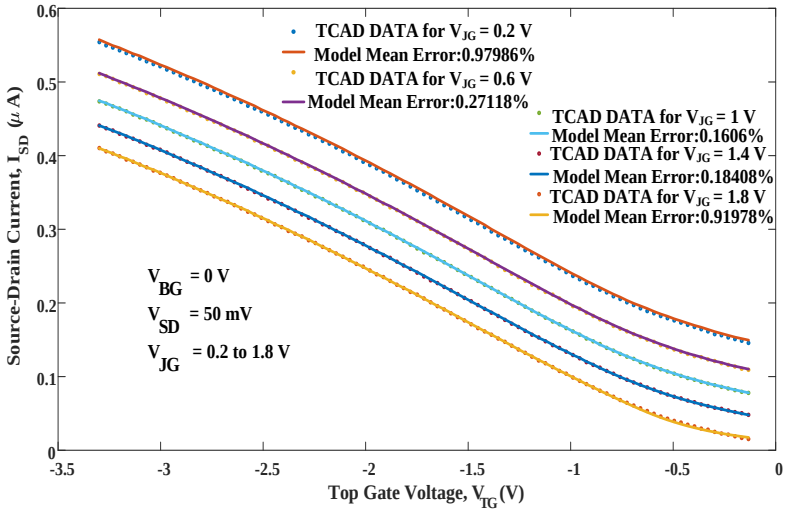


Figure 4.68: Comparison between test data and linear spline model isolines (Device 4) for variation in junction-gate voltages from 0.2 V to 1.8 V in 0.4 V increment arranged from top to bottom.

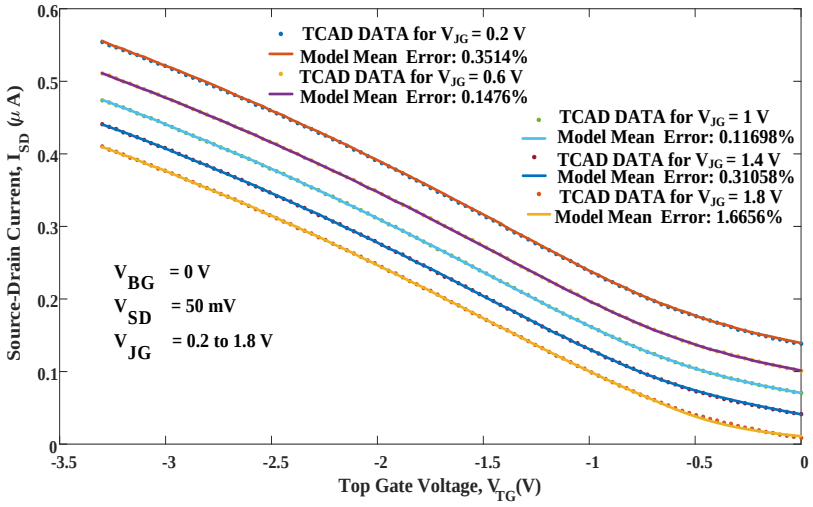


Figure 4.69: Comparison between test data and cubic spline model isolines (Device 4) for variation in junction-gate voltages from 0.2 V to 1.8 V in 0.4 V increment arranged from top to bottom.

this model. Figure 4.68 and Figure 4.69 show the isolines for five different reverse bias junction-gate voltage ranging from 0.2 V to 1.8 V for linear and cubic spline model, respectively. Here, the source-drain voltage and the bottom-gate voltage were fixed at 50 mV and 0 V, respectively. The graphs and corresponding mean relative errors show that the matching between the model and the test data is quite good for all the isolines.

4.5.2.5 Incorporation of Device Geometry

Spline model can be extended to include additional variables like geometric dimensions i.e. width, length and epi silicon thickness. This extended model including variations in device geometry provides highly desired flexibility to a circuit designer. Here, an *n*-channel G^{4}FET with the same doping conditions and epi silicon thickness as Device 1 was designed in TCAD Sentaurus and current-voltage characteristics were measured for different widths (W) and lengths (L) with W

and L being swept from 0.25 µm to 0.5 µm and from 0.8 µm to 1.8 µm, respectively. Using these data, cubic spline models are developed to find drain current as a function of V_{DS}, W and L.

A different test device inside the training geometry range was used to verify the model. Figure 4.70 shows the comparison between the test data and the cubic spline model for different widths. As evident from the figure, the matching is quite good across different geometries.

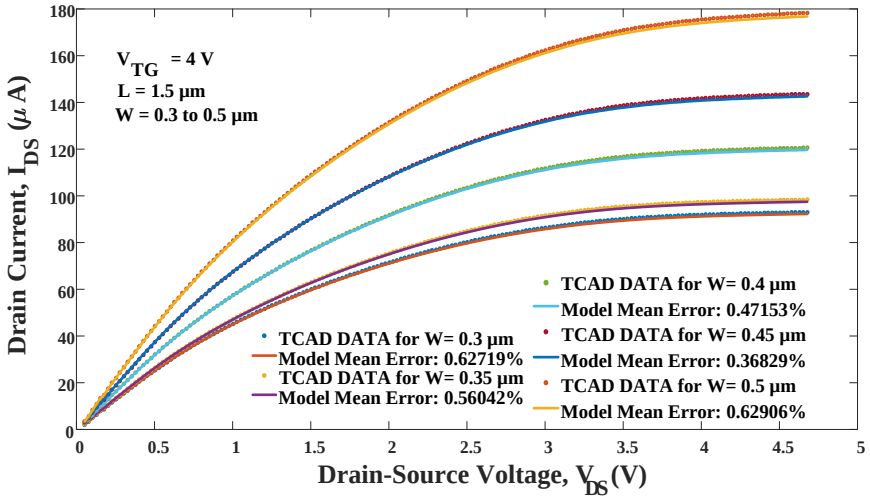


Figure 4.70: Comparison between TCAD data and cubic spline model of isolines for different widths ranging from 0.3 to 0.5 µm in .05 µm increment arranged from bottom to top.

4.5.2.6 Validation of First Order Characteristics i.e. Device Transconductance and Output Drain Resistance

First order characteristics such as transconductance and drain output resistance are crucial for ensuring the continuity and smoothness of *I-V* characteristics. Plots of transconductance and drain output resistance are shown in Figure 4.71 and Figure 4.72, respectively for cubic spline model. Here, the vertical axis is in logarithmic scale. As evident from these figures, the cubic

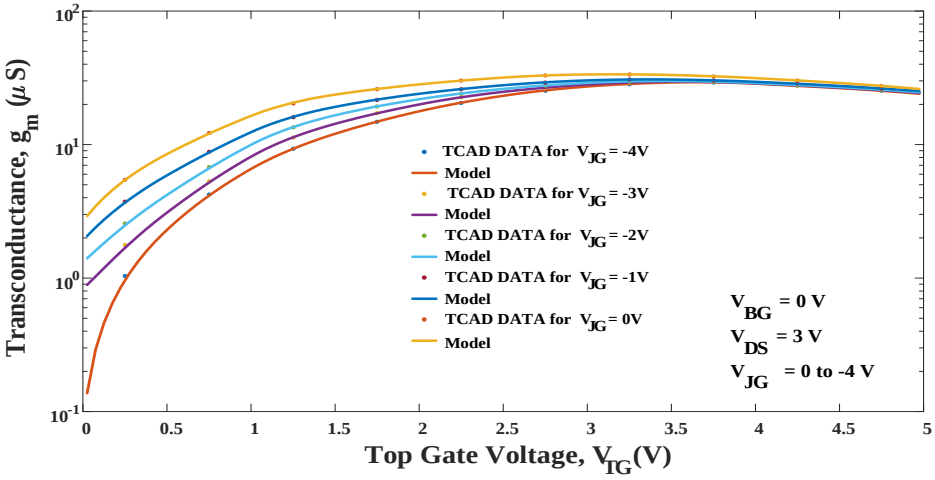


Figure 4.71: Comparison of g_m – V_{TG} between TCAD data and cubic spline model for an *n*-channel G^{4}FET (Device 1).

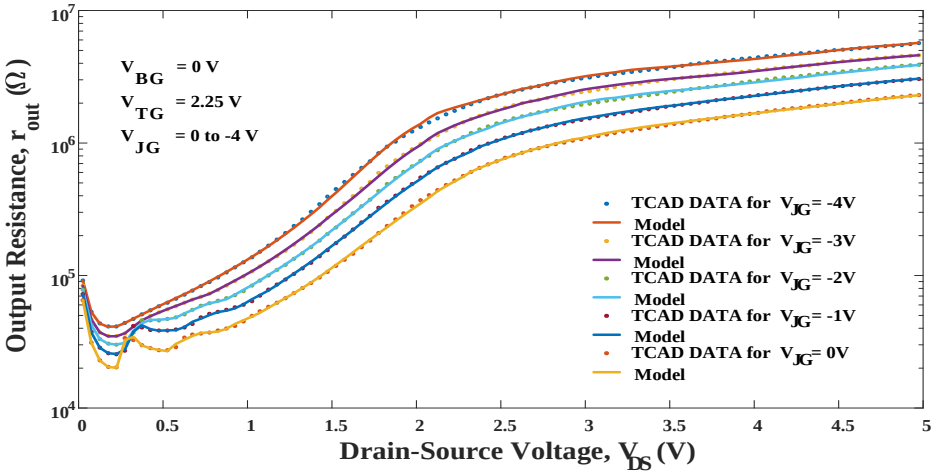


Figure 4.72: Comparison of r_{out} – V_{DS} between TCAD data and cubic spline model for an *n*-channel G^{4}FET (Device 1).

spline interpolation is reasonably accurate in retaining the first order characteristics which renders this model particularly suitable for analog circuit simulation.

4.5.3 Implementation in Circuit Simulator

Multivariate linear and cubic spline models of G^{4}FETs have been implemented in a circuit simulator. The model represents G^{4}FET transistor as a dependent current source between the drain and the source terminals and its current is controlled by the terminal voltages V_{TS}, V_{BS}, V_{LJS}, V_{RJS} and V_{DS} (Figure 4.73). This block is implemented using VerilogA in Cadence™ for circuit simulation using SPECTRE™ simulator. Other variables such as device geometric parameters or temperature can also be included in the model.

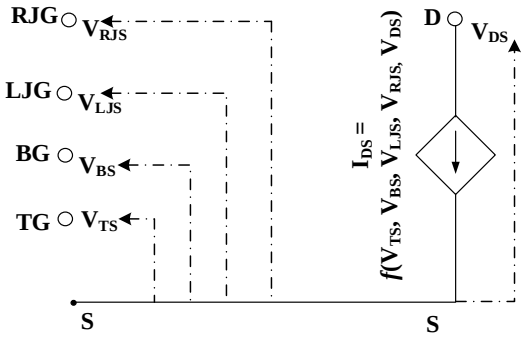


Figure 4.73: Behavioral model of an *n*-channel G^{4}FET for spline interpolation.

The performance and convergence of the simulation rely heavily on the continuity of function values and their first derivatives. The defining model equation of an element has to ensure that the transition between different operating regions does not compromise this continuity. In addition, the resulting equations have to preserve monotonicity so that no part of the equation

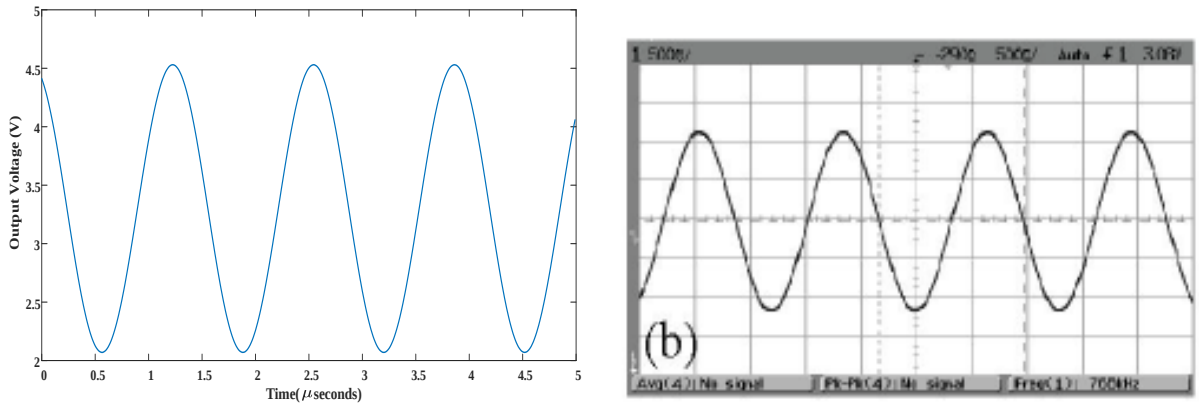
results in non-physical outcome such as negative conductance. These negative slope regions pose difficult problems for small-signal and DC transfer analysis which are extensively used in analog circuit design. The cubic spline model with continuity up to second order solves these problems and hence it is particularly suitable for this implementation. All the circuit simulation results in the following section are generated using this model.

4.5.4 Results from G^{4}FET Circuit Simulation

The developed model is used to simulate three innovative G^{4}FET circuits which are described in the following sections.

4.5.4.1 Negative Differential Resistance (NDR) LC oscillator:

The first implementation is an LC oscillator using negative differential resistance (NDR) circuit made of G^{4}FETs. This circuit was described in section 4.2.4.



a b

Figure 4.74(a) Output from circuit simulator, (b) experimental result.

Figure 4.20 shows a G^4-NDR connected to a LC tank load which works as an LC oscillator. It was experimentally demonstrated [34] with V_{DD} = 3.3 V, L= 0.4 mH, C = 110 pF. The models, developed using multivariate cubic spline, are implemented in VerilogA for circuit simulation using SPECTRE™ simulator in Cadence™ and the result is shown in Figure 4.74(a). The simulated oscillator output has 2.46 V peak-to-peak amplitude with a frequency of 761 kHz compared to the experimental result of 2.5 V peak-to-peak amplitude with a frequency of 768 kHz with a relative error of 1.6 % in amplitude.

4.5.4.2 High Voltage Differential Amplifier

G^4FETs are capable of handling much higher voltages compared to regular MOSFETS using the same process technology. The second circuit utilizes this capability to build a high voltage differential amplifier [36]. The circuit was described in section 4.4.4.

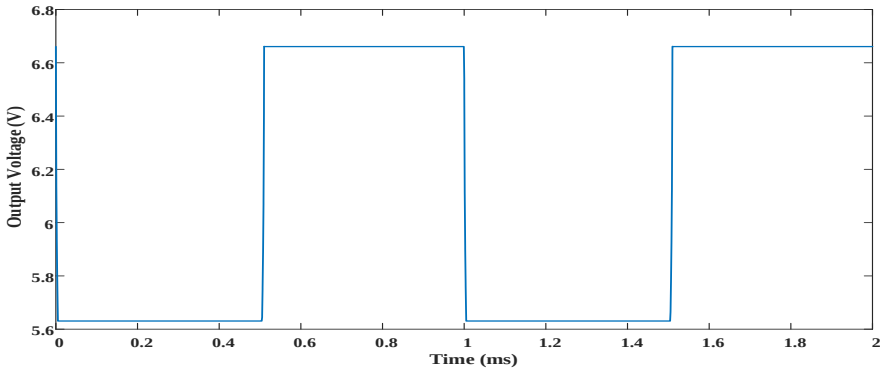


Figure 4.75: Output of amplifier (1.03 $V_{p\text{-}p}$ compared to experimental value of 1 $V_{p\text{-}p}$) in non-inverting unity gain configuration (V_{DD} = 10 V, V_{in} = 1 $V_{p\text{-}p}$ square wave with 6 V offset).

The high voltage differential amplifier in [36] works as a non-inverting unity gain amplifier to a square wave input of 1 KHz frequency and 1 $V_{p\text{-}p}$ amplitude. The circuit has been simulated

with the cubic spline interpolation being used for modelling both *n*-channel and *p*-channel G^4FETs. The result in Figure 4.75 with an output of 1.03 V_{p-p} is reasonably close to the experimental result of 1 V_{p-p} with a 3% relative error.

4.5.4.3 Four-Quadrant Analog Multiplier:

The independent multi-gate current modulation capability of G^4FET can be used to design analog multiplier with only four transistors at its core. Two different configurations were experimentally demonstrated in [36]. Both of them have multiplier core made of four G^4FETs biased by a constant current sink and loaded by same resistors R_L which convert the differential output current to a differential output voltage. However, the input is different for these two cases. As shown in Figure 4.76, configuration 1 has one input V_{in1} at the top-gate and other input V_{in2} at the junction-gates, which are tied together. In configuration 2, shown in Figure 4.77, the junction-gates are independent and two differential input voltages V_{in1} and V_{in2} are connected to two lateral junction-gates, whereas the top-gate, in this configuration, is biased at a constant voltage.

Figure 4.78 and Figure 4.79 show DC transfer characteristics for configuration 1 and 2, respectively. For different $V_{in2,}$ V_{in1} is swept between -1.5 and 1.5 V and the corresponding simulation results qualitatively match with the experimental outputs. The linearity is maintained for different input conditions and the gain is very similar. Table 4.5 and Table 4.6 show a comparison between the experimental results and the simulation output for configuration 1 and configuration 2, respectively. The model is developed based on TCAD data, which causes some deviation from measurement results.

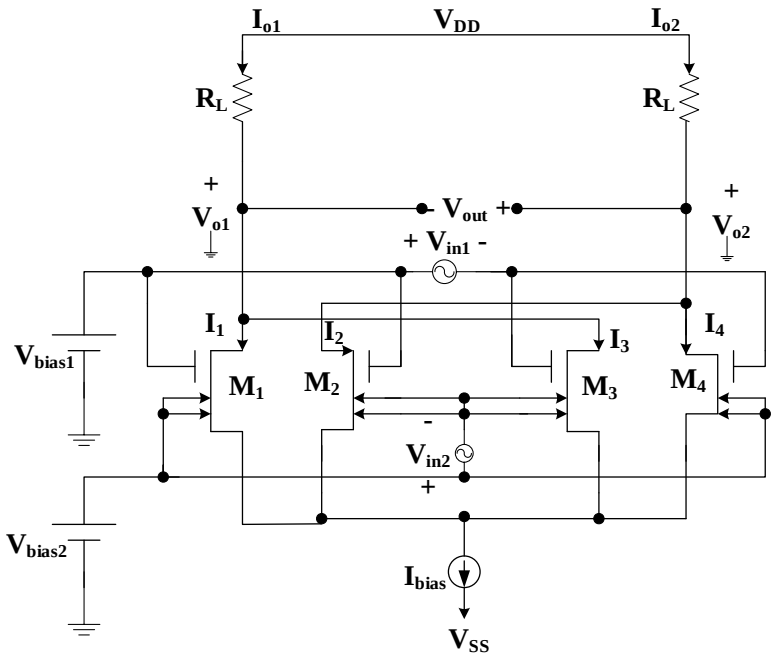


Figure 4.76: Configuration 1 of analog multiplier using G^{4}FET.

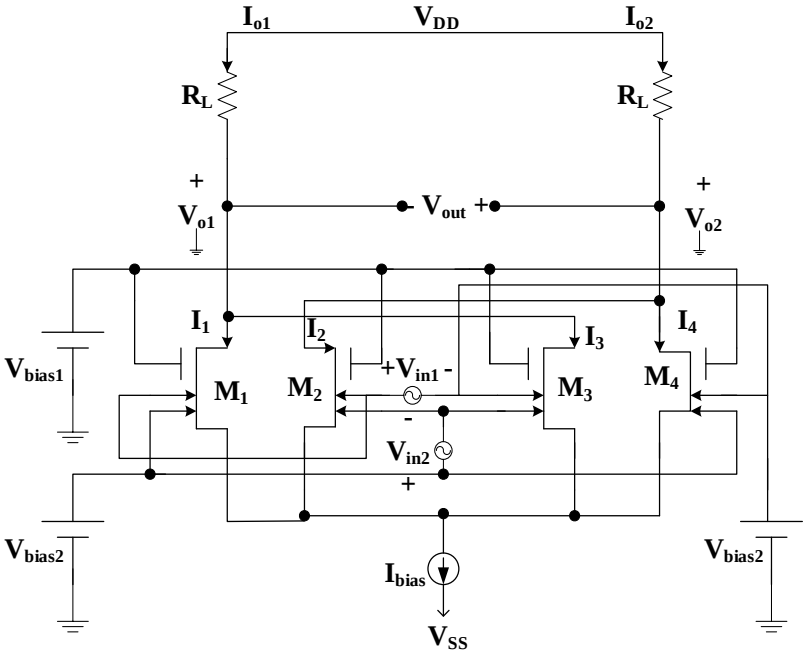
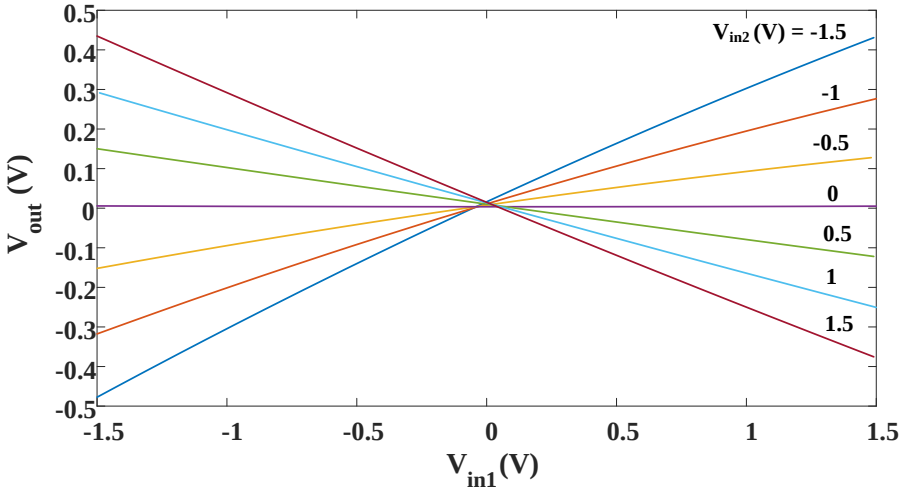
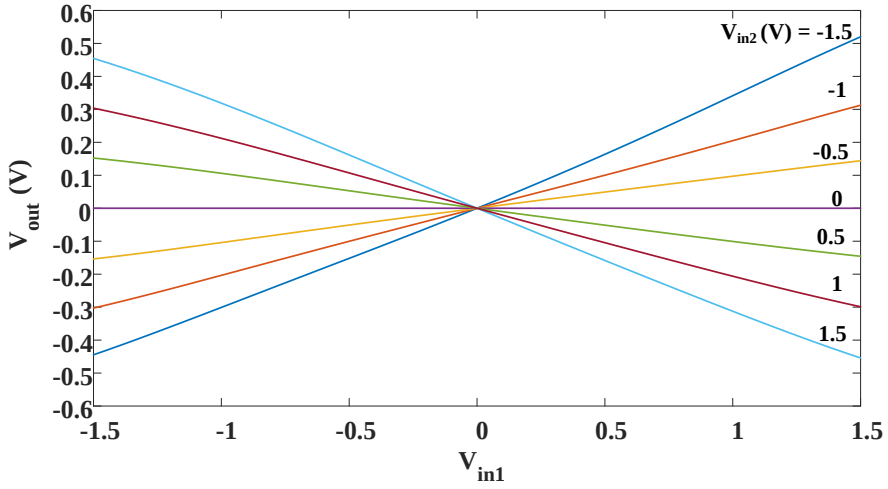


Figure 4.77: Configuration 2 of analog multiplier using G^{4}FET.

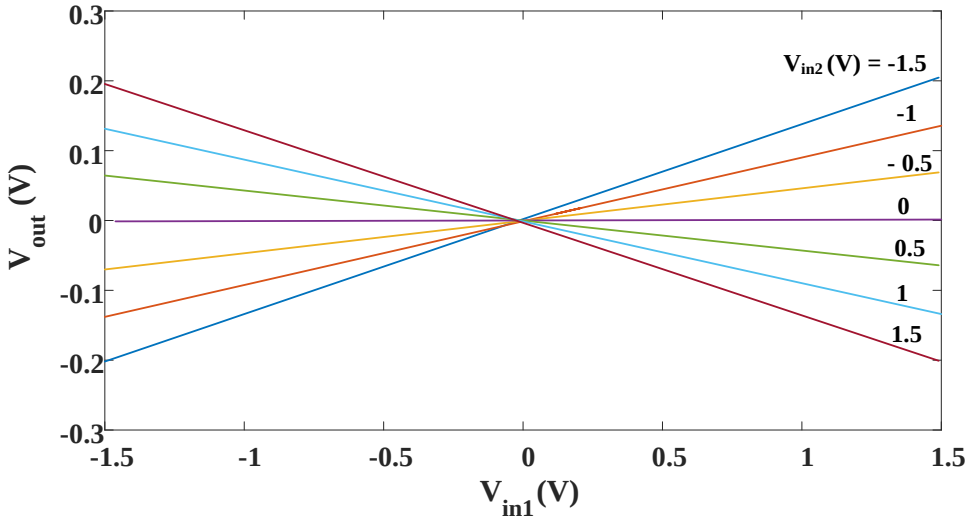


(a)

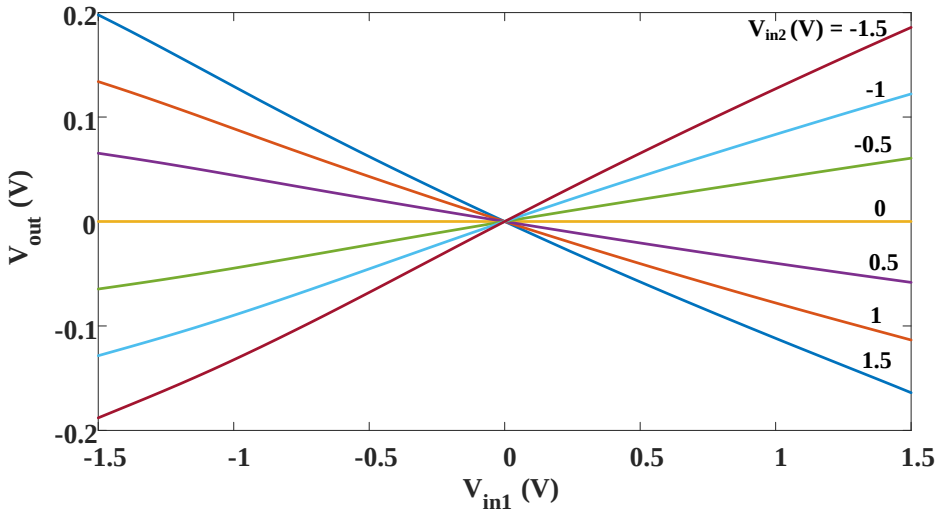


(b)

Figure 4.78: DC transfer characteristics for configuration 1 (W = 0.35 µm, L = 10 µm, V_{DD} = 10 V, I_{bias} = 15 µA, V_{bias1} = 1.7 V, V_{bias2} = -1.8 V, R_L = 500 kΩ); (a) measurement results reproduced from [37], (b) simulation results using cubic spline model.



(a)



(b)

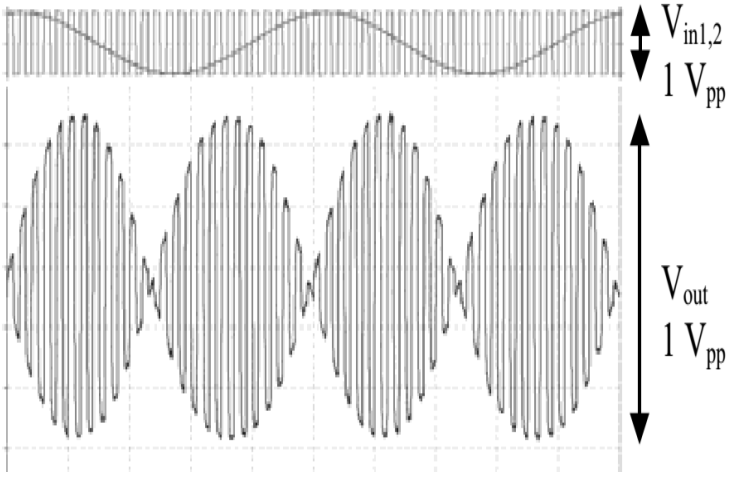
Figure 4.79: DC transfer characteristics for configuration 2 (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 10 µA, V_{bias1} = 0 V, V_{bias2} = -3 V, R_L = 500 kΩ); (a) measurement results reproduced from [37], (b) simulation results using cubic spline model.

Table 4.5: Comparison Between Experimental and Simulation Results for DC Transfer Characteristics of Configuration 1

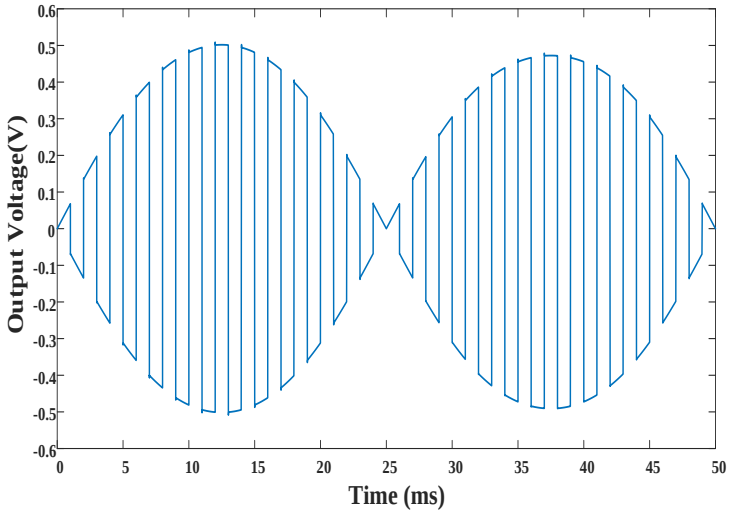
V_{in2} (V)	Peak-to-Peak Variation in V_{out} (V)		Relative Error (%)
	Experimental Results	Simulation Results	
-1.5	0.911	0.965	5.927552
-1	0.594	0.615	3.535354
-0.5	0.281	0.298	6.049822
0	0	0	0
0.5	0.273	0.298	9.157509
1	0.544	0.602	10.66176
1.5	0.813	0.909	11.80812

Table 4.6: Comparison Between Experimental and Simulation Results for DC Transfer Characteristics of Configuration 2

V_{in2} (V)	Peak-to-Peak Variation in V_{out} (V)		Relative Error (%)
	Experimental Results	Simulation Results	
-1.5	0.408	0.374	8.333333
-1	0.274	0.251	8.394161
-0.5	0.139	0.125	10.07194
0	0	0	0
0.5	0.129	0.124	3.875969
1	0.265	0.247	6.792453
1.5	0.398	0.361	9.296482

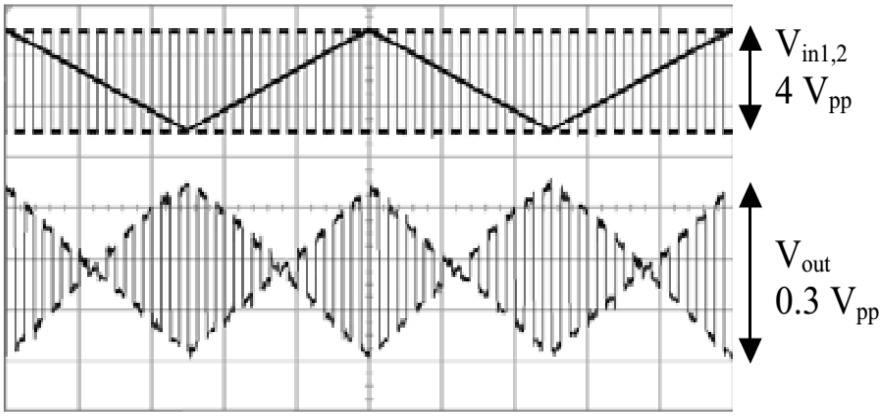


(a)

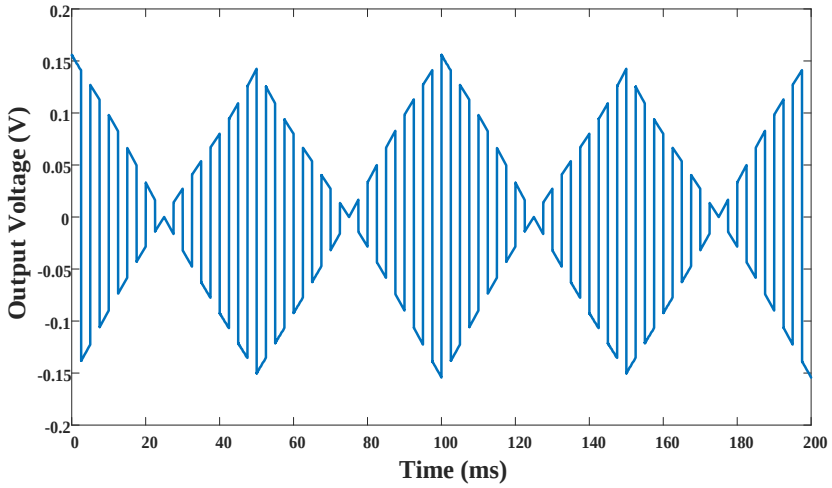


(b)

Figure 4.80: Product of a 20 Hz, 1 $V_{p\text{-}p}$ sinusoidal-wave with 500 Hz, 1 $V_{p\text{-}p}$ square-wave (W = 0.3 µm x 10, L = 2.4 µm, V_{DD} = 3.5 V, V_{SS} = -3.5 V, I_{bias} = 35 µA, V_{bias1} = 2 V, V_{bias2} = -2.5 V, R_L = 100 kΩ); (a) measurement results, (b) simulation results using cubic spline model.



(a)



(b)

Figure 4.81: Product of a 10 Hz, 4 $V_{p\text{-}p}$ triangular-wave with 200 Hz, 4 $V_{p\text{-}p}$ square-wave (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 15 µA, V_{bias1} = 0 V, V_{bias2} = -3.5 V, R_L = 200 kΩ); (a) measurement results, (b) simulation results using cubic spline model.

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Figure 4.80 shows the result for configuration 1 as an analog multiplier where the inputs are a 20 Hz, 1 V_{p-p} sinusoidal-wave and a 500 Hz, 1V_{p-p} square-wave. The simulation result using the cubic spline model in Figure 4.80(b) shows good matching with the experimental result in Figure 4.80(a). The peak-to-peak output voltage in simulation is 1.0176 V compared to the measurement result of 1 V, with a relative error of 1.76 %.

Configuration 2 was also used as an analog multiplier with two different input signals; a 10 Hz, 4 V_{p-p} triangular-wave and a 200 Hz, 4 V_{p-p} square-wave. Configuration 2 has a reduced gain compared to configuration 1, but it has a higher input voltage swing capability. Figure 4.81(a) and Figure 4.81(b) show the experimental and the simulation results, respectively. As the figures show, there is a reasonable agreement between the experimental and the simulation results. The peak-to-peak output voltage in simulation is 0.3101 V compared to the measurement result of 0.3 V, with a relative error of 3.37 %

4.6 Chapter Summary

In this chapter, four different numerical models of G^4FET transistor are developed and their validity for current-voltage characteristics prediction and circuit simulator implementation is demonstrated. This provides circuit designers with a potential tool to design new and efficient circuits with G^4FETs. A total number of seven variables, including the four independent gate voltages and geometric parameters have been used in different phases of model implementation showing the flexibility of this modeling approach. Other variables such as height of epi-silicon layer, terminal capacitances, temperature etc. can be incorporated using these methods to extend

model's functionality. The explored modeling approaches are not restricted to G^4FET or SOI transistors and may be used to model any new multi-gate device.

Chapter 5 - Macromodel of G^{4}FET

5.1 Motivation

The numerical models, as described in chapter 4, work well inside the operating range used for model development. However, owing to five independent terminals, the resulting expression gets cumbersome as more accuracy is desired. The inclusion of geometric variables and terminal capacitances as independent variables would significantly increase computational cost. Inclusion of other variables such as epi silicon thickness, temperature etc. would increase model complexity furthermore. A simplified model based on device operating principle and existing SPICE models can be helpful to circumvent most of these problems. G^{4}FET was also called MOSJFET [15] for combining the functionality of MOSFET and JFET transistors. Since, well developed robust, fast and reliable models of both MOSFET and JFET transistors are already available, a macromodel combining these existing models is desirable from a circuit designer's perspective.

5.2 Model Formation

G^{4}FET combines MOS and JFET actions by supporting both surface and volume conduction. The top and the bottom oxide gates provide MOS action whereas the lateral junction-gates work like JFET. The threshold voltage of the top and the bottom-gates are influenced by the junction-gate voltage. It can be considered as a combination of two MOSFETs (surface conduction) working in parallel with a JFET (volume conduction).

The analytical relationship between the junction-gates and the oxide gates has been derived in [21]. Let the top-gate threshold voltage be V_{TH} and the bottom-gate voltage causing the onset

of accumulation and inversion at the bottom-gate are V_{BG}^{acc} and V_{BG}^{inv}, respectively. Some of the terms used in the model are introduced below:

$$\text{Junction-gate capacitance},\ C_{JG} = {\varepsilon_{Si}}/{W}$$
$$\text{Top oxide capacitance},\ C_{ox1} = {\varepsilon_{ox}}/{t_{ox1}}$$
$$\text{Bottom oxide capacitance},\ C_{ox2} = {\varepsilon_{ox}}/{t_{ox2}}$$

Three constants based on device geometry, α, β and γ are defined as,

$$\alpha = \frac{2\sqrt{2}}{\tanh(\frac{2\sqrt{2}t_{Si}}{W})}$$
$$\gamma = \frac{2\sqrt{2}}{\sinh(\frac{2\sqrt{2}t_{Si}}{W})}$$
$$\beta = \frac{{\gamma C_{JG}}/{C_{ox1}}}{1 + {\alpha C_{JG}}/{C_{ox2}}}$$

Other terms include,

$$\varphi_F = -V_T \ln\left(\frac{N_d}{n_i}\right)$$
$$\varphi_b = \frac{E_g}{2} + V_T \ln\left(\frac{N_d}{n_i}\right)$$
$$V_P = \varphi_b - \frac{qN_dW^2}{8\varepsilon_{Si}}$$

Here, W is the width of the transistor, t_{si} is the silicon film thickness, t_{ox1} is the top oxide thickness, t_{ox2} is the buried oxide thickness, $V_T = kT/q$ is the thermal voltage, N_d is the donor concentration in the body, n_i is the intrinsic carrier concentration, ε_{si} is the permittivity of silicon, and ε_{ox} is the permittivity of silicon dioxide.

The onset voltage of accumulation and inversion for the bottom-gate, V_{BG}^{acc} and V_{BG}^{inv}, can be expressed [21] as,

$$V_{BG}^{acc} = V_{FB2} + (\gamma - \alpha)\frac{C_{JG}}{C_{ox2}}(V_{JS} - V_P) \quad (5.1)$$

$$V_{BG}^{inv} = V_{FB2} + \left(1 + \alpha\frac{C_{JG}}{C_{ox2}}\right)2\varphi_F - (\gamma - \alpha)\frac{C_{JG}}{C_{ox2}}(V_P) + \left(1 + \gamma C_{JG}/C_{ox2}\right)V_{JG} \quad (5.2)$$

The back gate may be accumulated, depleted or inverted. When the bottom-gate is in inversion i.e. $V_{BG} < V_{BG}^{inv}$,

$$V_{TH} = V_{FB1} - \gamma\left(\frac{C_{JG}}{C_{ox1}}\right)(2\varphi_F + V_P) - \alpha\left(\frac{C_{JG}}{C_{ox1}}\right)(V_{JG} - V_P) \quad (5.3)$$

When the bottom-gate is depleted i.e. $V_{BG}^{inv} < V_{BG} < V_{BG}^{acc}$,

$$V_{TH} = V_{FB1} - \beta(V_{BG} - V_{FB2}) + (\gamma - \alpha)\left(\frac{C_{JG}}{C_{ox1}} + \beta\frac{C_{JG}}{C_{ox1}}\right)(V_{JG} - V_P) \quad (5.4)$$

When the bottom-gate is in accumulation i.e. $V_{BG} > V_{BG}^{acc}$,

$$V_{TH} = V_{FB1} + (\gamma - \alpha)\left(\frac{C_{JG}}{C_{ox1}}\right)(V_{JG} - V_P) \quad (5.5)$$

Here, V_{FB1} and V_{FB2} are the flat band voltages of the top-gate and the bottom gates, respectively.

Based on the above relationships among different gates, a macromodel is created combining the MOSFET and the JFET models. However, accumulated back gate provides a shunt leakage conduction path which is undesirable for most practical applications. Therefore, it is assumed that the back gate is never accumulated and the condition for depleted or inverted back surface is considered. In the model, the top conduction is modeled using a MOSFET and the volume conduction is modeled using a JFET. However, instead of a constant threshold MOSFET, the subcircuit allows for threshold voltage modification using the relationship described above.

5.3 CAD Implementation for Circuit Design

Six different analog and digital circuits have been simulated using the macromodel. These include 1) negative differential resistance circuit, 2) high voltage differential amplifier, 3) four-

quadrant analog multiplier, 4) multiple threshold inverter, 5) G^4FET as a universal and programmable logic gate and 6) G^4FET full adder circuit.

5.3.1 Negative Differential Resistance Circuit:

Complementary G^4FETs can be combined to work as a negative differential resistance block as described in section 4.2.4. Figure 4.20 shows a G^4-NDR connected to a LC tank load which works as an LC oscillator. It was experimentally demonstrated with V_{DD} = 3.3 V, L= 0.4 mH, C = 110 pF [34]. The simulation output is 2.45 $V_{p\text{-}p}$ compared with the experimental result of 2.5 $V_{p\text{-}p}$ with a relative error of 2 % as shown in Figure 5.1.. The extra two terminals, V_n and V_p provide additional functionality and are used for amplitude modulation as shown in Figure 5.2.

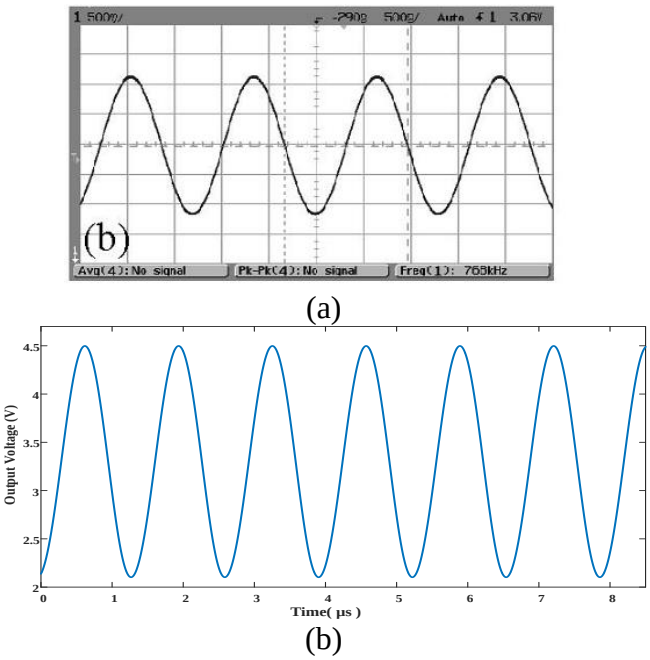
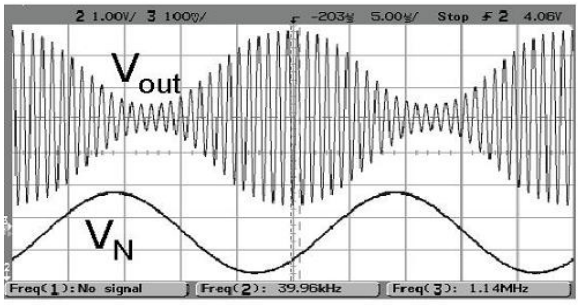
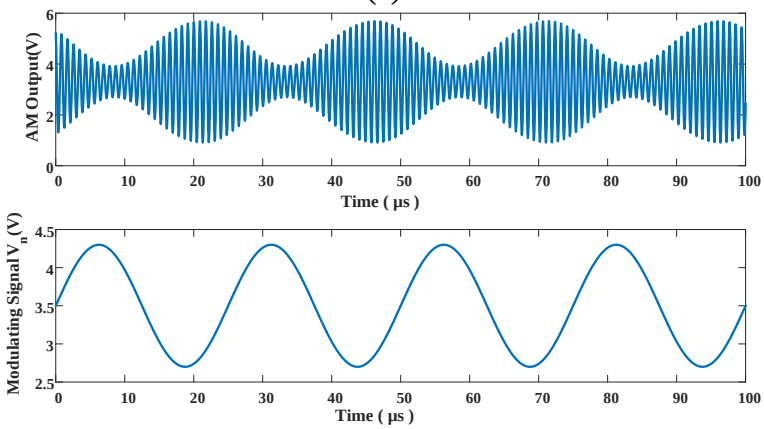


Figure 5.1: Output of NDR LC oscillator; (a) measurement result, (b) simulation result.



(a)



(b)

Figure 5.2: Amplitude Modulated(AM) signal; (a) measurement result, (b) simulation result.

5.3.2 Differential Amplifier:

G^4FET can be used to build high voltage differential amplifier circuit. This circuit, described in section 4.4.4, was simulated using the macromodel. The simulation result is shown in Figure 5.3. The output of the non-inverting amplifier is 0.98 V peak-to-peak compared to the experimental result of 1 V peak-to-peak with a 2% relative error.

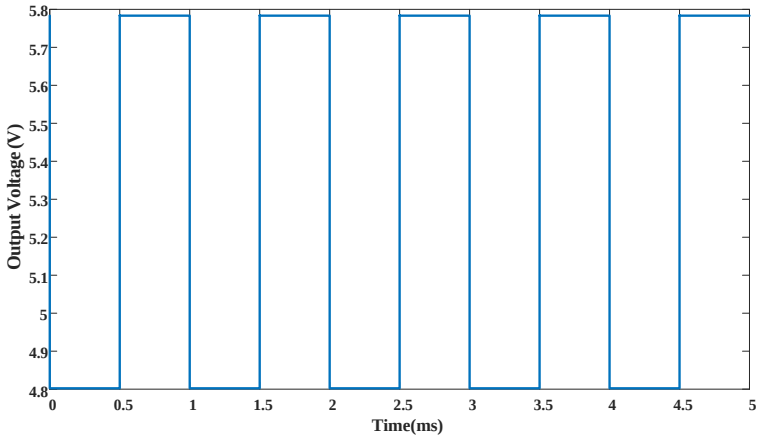


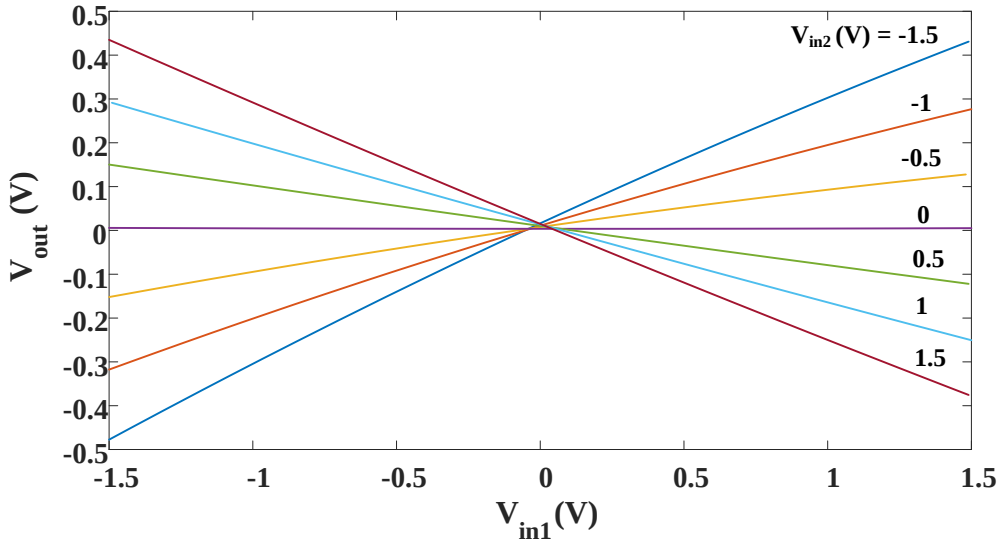
Figure 5.3: High voltage differential amplifier output from the macromodel simulation.

5.3.3 Four Quadrant Analog Multiplier :

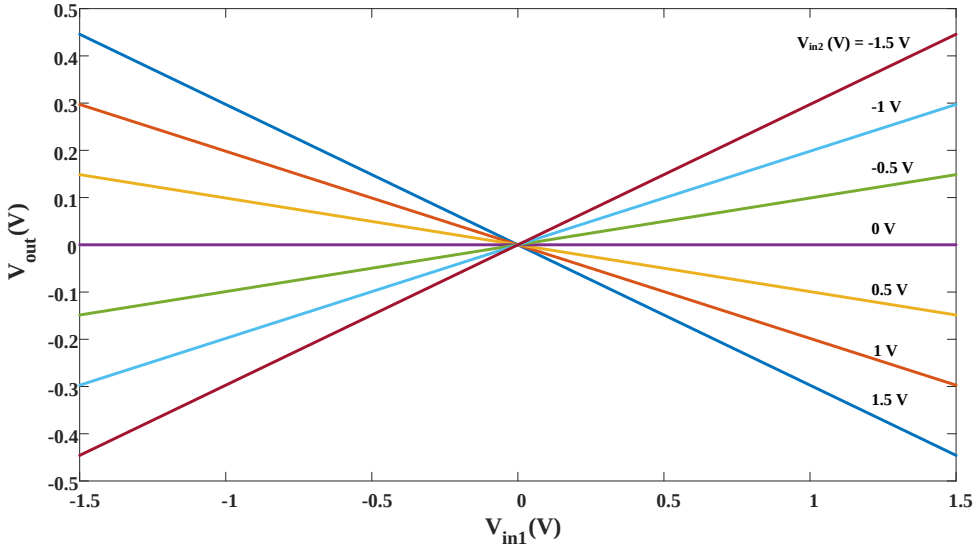
A four-quadrant analog multiplier is a very interesting application of G^4FET where the multiplier core has been shown to be built with only four transistors. Two configurations of these circuits and their working mechanisms were described in section 4.5.4.3.

The macromodel was used to simulate both the configurations. DC transfer characteristic for configuration 1 and configuration 2 are shown in Figure 5.4 and Figure 5.5, respectively. The measurement results are shown in Figure 5.4 (a) and simulation results obtained using the macromodel are shown in Figure 5.4 (b). Table 5.1 and Table 5.2 give a quantitative comparison between measurement and simulation results for configuration 1 and 2, respectively.

Figure 5.6 shows the result for configuration 1 as an analog multiplier where the inputs are a 20 Hz, 1 V_{p-p} sinusoidal-wave and a 500 Hz, 1 V_{p-p} square-wave. The simulation result using the macromodel in Figure 5.6 (b) shows good matching with the experimental result in Figure 5.6(a). The peak-to-peak output voltage in simulation is 1.0025 V compared to the measurement result of 1 V, with a relative error of 0.25 %.

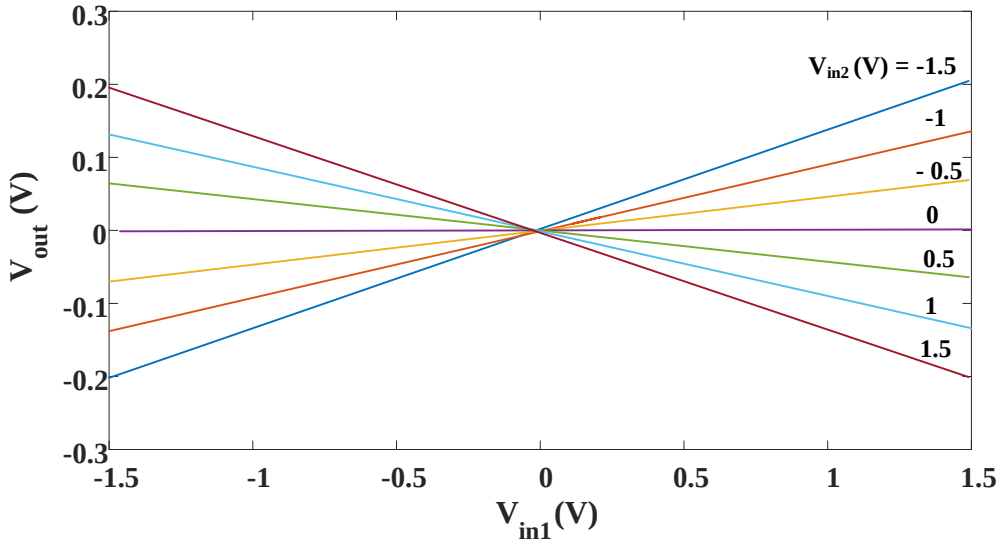


(a)

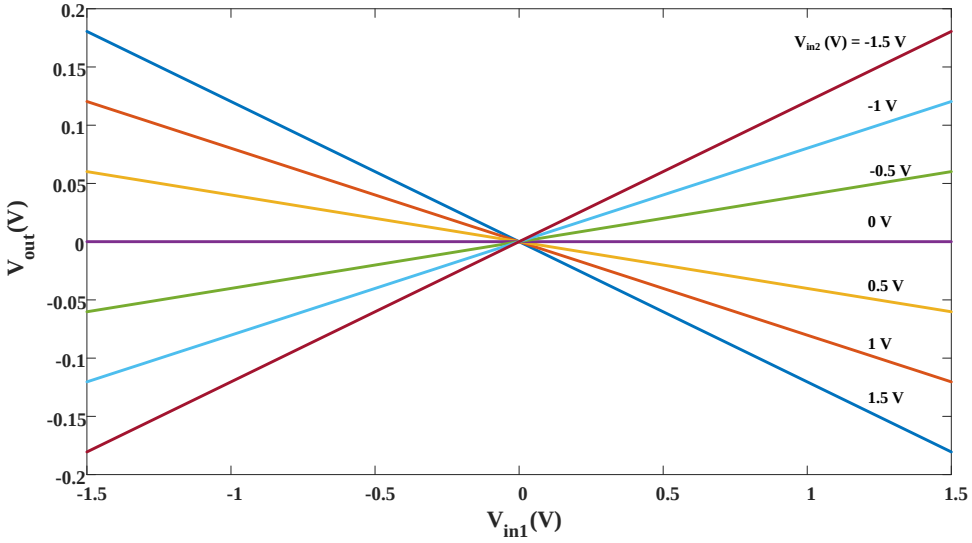


(b)

Figure 5.4: DC transfer characteristics for configuration 1 (W = 0.35 µm, L = 10 µm, V_{DD} = 10 V, I_{bias} = 15 µA, V_{bias1} = 1.7 V, V_{bias2} = -1.8 V, R_L = 500 kΩ); (a) measurement results reproduced from [7], (b) simulation results using the macromodel.



(a)



(b)

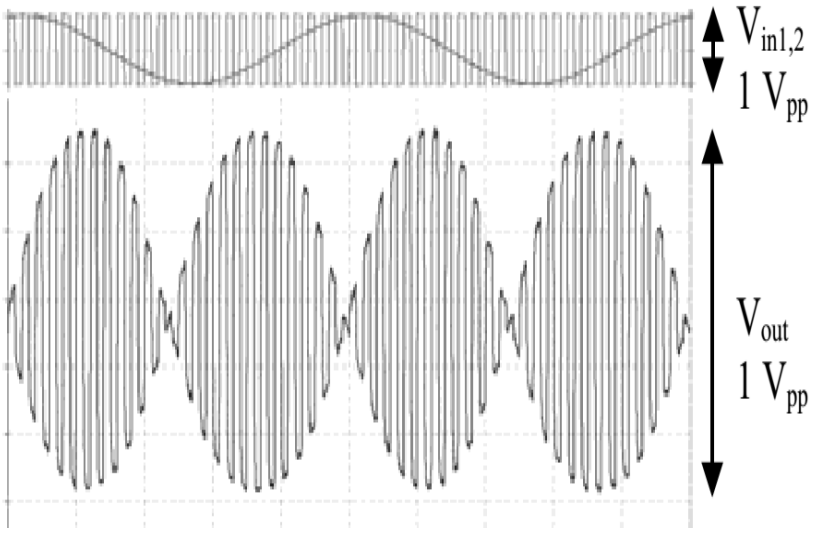
Figure 5.5: DC transfer characteristics for configuration 2 (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 10 µA, V_{bias1} = 0 V, V_{bias2} = -3 V, R_L = 500 kΩ); (a) measurement results reproduced from [7], (b) simulation results using the macromodel.

Table 5.1: Comparison Between Experimental and Simulation Results (Macromodel) for DC Transfer Characteristics of Analog Multiplier (Configuration 1)

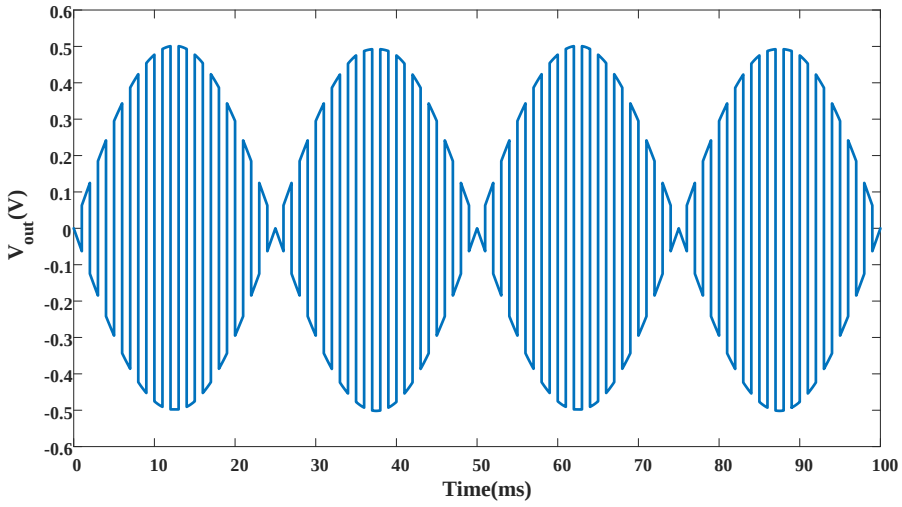
V_{in2} (V)	Peak-to-Peak Variation in V_{out} (V)		Relative Error (%)
	Experimental Results	Simulation Results	
-1.5	0.911	0.892	2.08562
-1	0.594	0.594	0
-0.5	0.281	0.297	5.69395
0	0	0	0
0.5	0.273	0.297	8.791209
1	0.544	0.594	9.191176
1.5	0.813	0.892	9.717097

Table 5.2: Comparison of Experimental and Simulation Results (Macromodel) for DC Transfer Characteristics of Analog Multiplier (Configuration 2)

V_{in2} (V)	Peak-to-peak variation in V_{out} (V)		Relative error (%)
	Experimental results	Simulation results	
-1.5	0.408	0.361	11.51961
-1	0.274	0.241	12.0438
-0.5	0.139	0.12	13.66906
0	0	0	0
0.5	0.129	0.12	6.976744
1	0.265	0.241	9.056604
1.5	0.398	0.361	9.296482

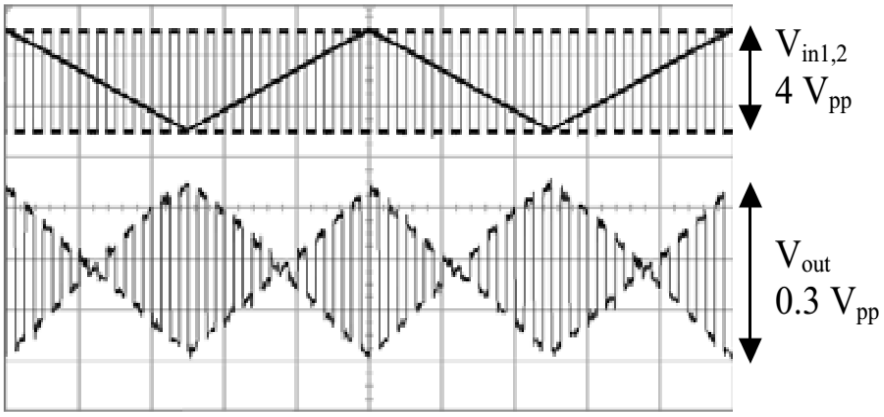


(a)

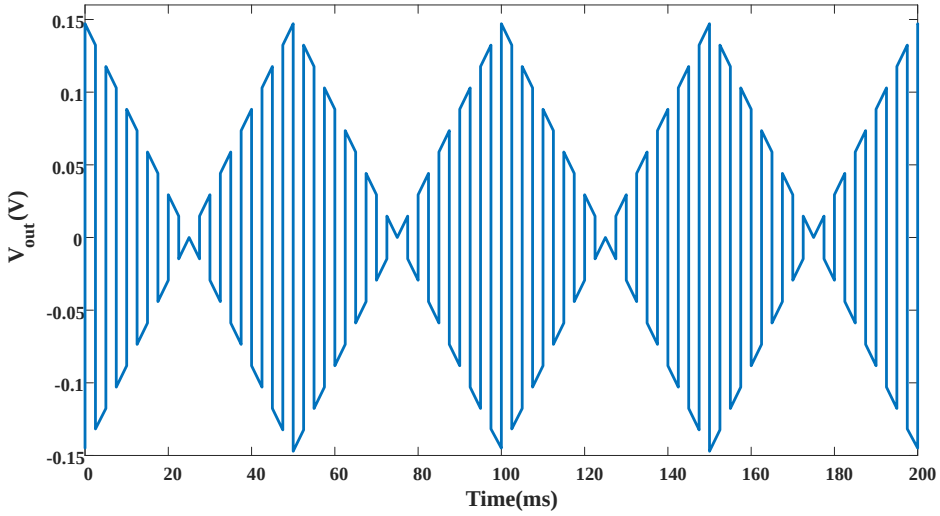


(b)

Figure 5.6: Product of a 20 Hz, 1 $V_{p\text{-}p}$ sinusoidal-wave with 500 Hz, 1$V_{p\text{-}p}$ square-wave (W = 0.3 µm x 10, L = 2.4 µm, V_{DD} = 3.5 V, V_{SS} = -3.5 V, I_{bias} = 35 µA, V_{bias1} = 2 V, V_{bias2} = -2.5 V, R_L = 100 kΩ); (a) measurement results, (b) simulation results using the macromodel.



(a)



(b)

Figure 5.7: Product of a 10 Hz, 4 $V_{p\text{-}p}$ triangular-wave with 200 Hz, 4 $V_{p\text{-}p}$ square-wave (W = 0.35 µm, L = 5 µm, V_{DD} = 5 V, I_{bias} = 15 µA, V_{bias1} = 0 V, V_{bias2} = -3.5 V, R_L = 200 kΩ); (a) measurement results, (b) simulation results using the macromodel.

Configuration 2 was also used as an analog multiplier with two different input signals; a 10 Hz, 4 V_{p-p} triangular-wave and a 200 Hz, 4 V_{p-p} square-wave. This configuration has a reduced gain compared to configuration 1, but it has a higher input voltage swing capability. Figure 5.7(a) and Figure 5.7(b) show the experimental and the simulation results, respectively. As the figures show, there is a reasonable agreement between the experimental and the simulation results. The peak-to-peak output voltage in simulation is 0.294 V compared to the measurement result of 0.3 V, with a relative error of 1.95 %.

5.3.4 Multi-Threshold Inverter:

G^4FET can be used to build interesting digital circuits as well. The multiple gates offer plenty of opportunities for innovative digital designs. In [38], a multi-threshold inverter has been demonstrated. The schematic is shown in Figure 5.8. The top-gate works as a conventional MOS gate whereas the junction-gate bias is used to change the threshold of the inverter. Three different thresholds for different junction-gate combinations are obtained. The macromodel reproduces the results in [38] quite well as shown in Figure 5.9. Different threshold curves for varying the junction-gate voltages are shown as A, B and C.

5.3.5 Universal and Programmable Gate:

G^4FET can be used as a real-time reconfigurable logic gate as demonstrated in [38]. The schematic of a programmable logic gate is shown in Figure 5.10. Here, the left and the right junctions act as inputs and the top-gate acts as controller. Based on the value of the top-gate

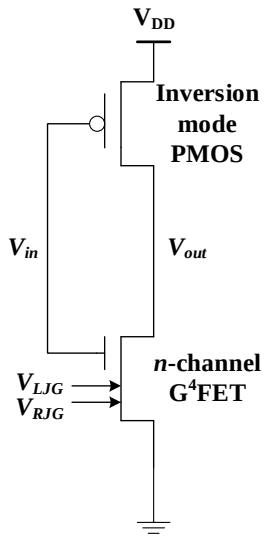


Figure 5.8: Schematic of a multi-threshold Inverter.

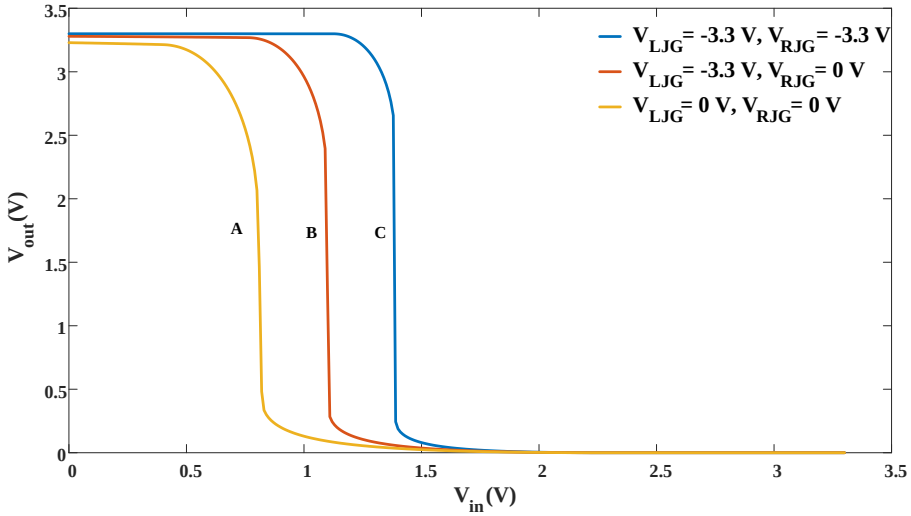


Figure 5.9: Output of a multi-threshold inverter.

voltage, this can function as either NAND or NOR gate. Hence, in principle, G^{4}FET is a universal gate, since any logic function can be computed using it.

Figure 5.11 shows the results for a programmable gate using the macromodel. The output is a NAND function, $V_{out} = \overline{V_{RJG}.V_{LJG}}$, when $V_{INV,A} < V_{TG} = 0.9\ V < V_{INV,B}$. The output is a NOR function, $V_{out} = \overline{V_{RJG} + V_{LJG}}$, when $V_{INV,B} < V_{TG} = 1.2\ V < V_{INV,C}$. The results show excellent matching with the experimental results reported in [38].

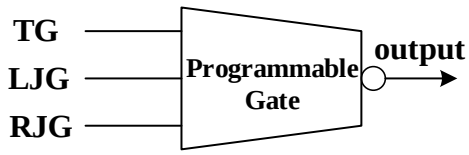


Figure 5.10: Symbol of a G^{4}FET programmable gate.

5.3.6 Full Adder:

A full adder circuit was demonstrated in [39] using only 3 G^{4}FET transistors and 2 inverters. This drastically reduces the number of transistor count and paves the way for more compact arithmetic logic operation circuits. Figure 5.12 shows the schematic of the proposed design. The circuit has been simulated using the macromodel and the output is shown in Figure 5.13. The full adder functionality for all the possible combinations from the truth table in Table 5.3 is demonstrated.

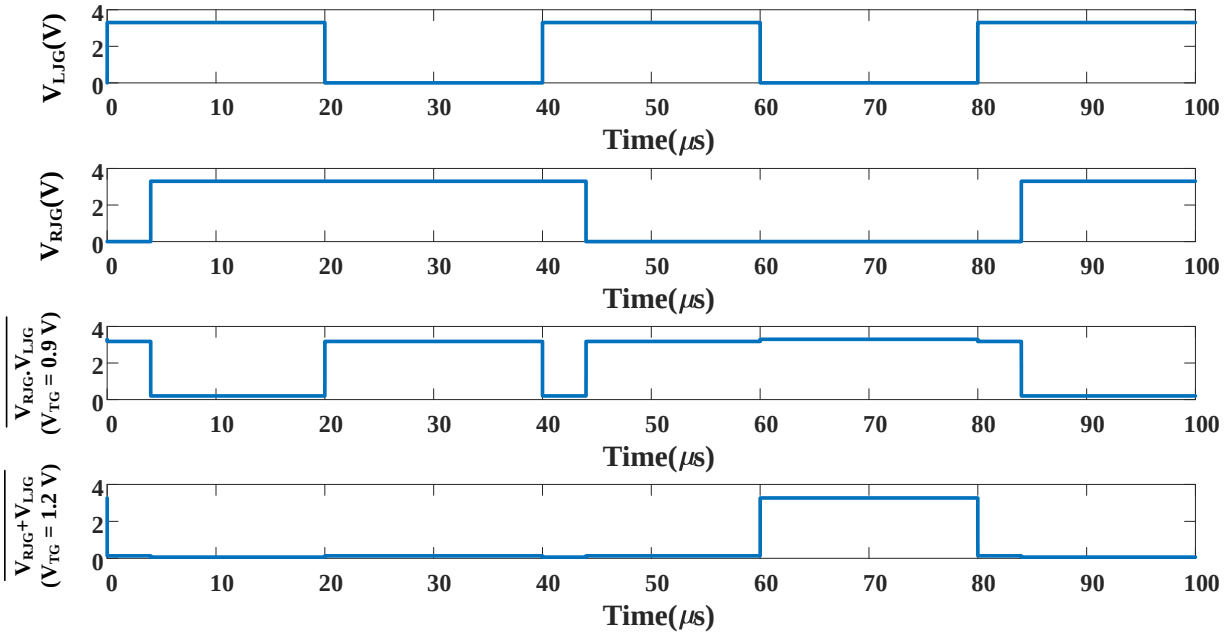


Figure 5.11: Output of a programmable gate.

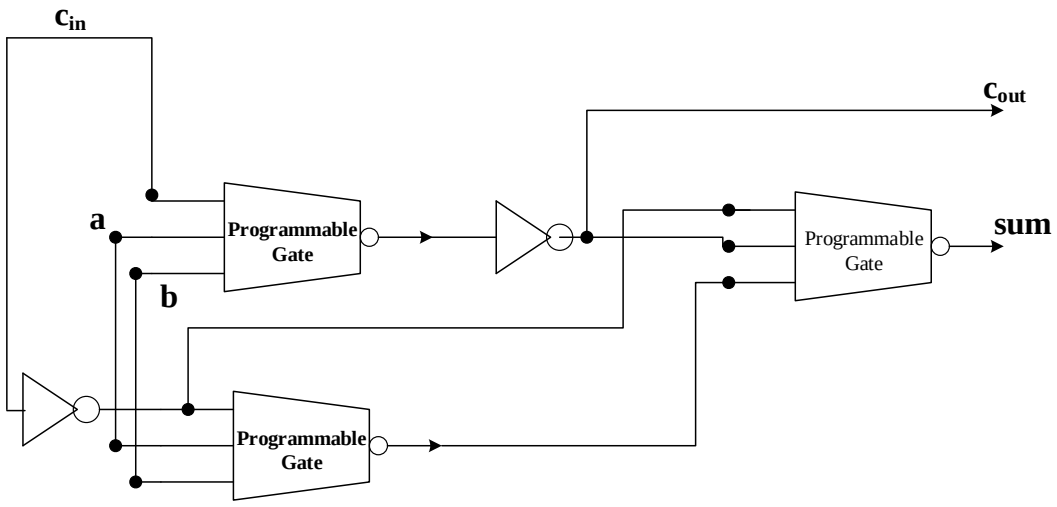


Figure 5.12: Schematic of the G^4FET full adder.

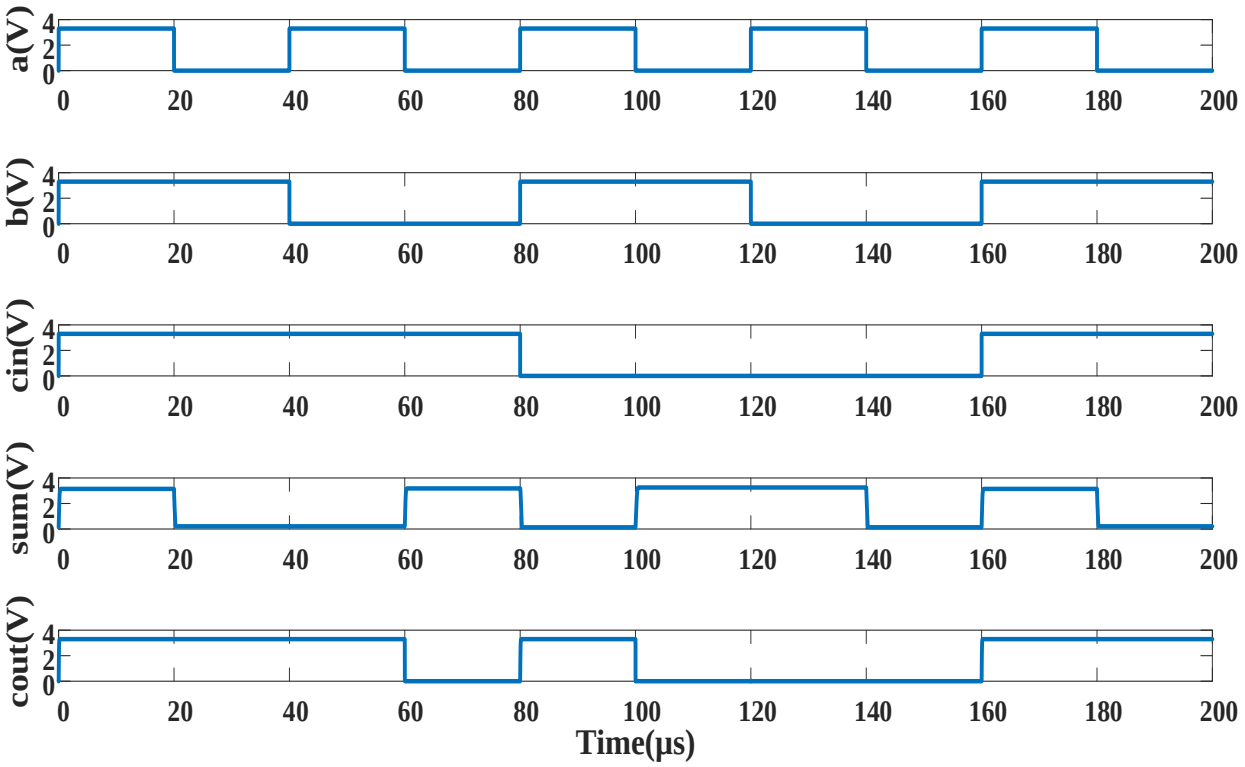


Figure 5.13: Output from the full adder.

Table 5.3: Truth Table of a Full Adder

a	b	c_{in}	Sum	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

5.4 Chapter Summary

The macromodel of G^4FET captures some of the underlying physics of G^4FET operation and effectively combines MOSFET and JFET functionalities into a single model. The existence of robust, stable and accurate of MOSFET and JFET SPICE models facilitate faster implementation in circuit simulator. The model has been successful in reproducing a number of experimental G^4FET circuits; both analog and digital. In this work, the macromodel has been developed with Level 1 and Level 2 SPICE models. Further improvement can be accomplished using BSIM model with optimized parameters.

Chapter 6 – Physics-Based Compact Model of G^4FET

6.1 Motivation

A fully physics-based model of a transistor requires solving a system of coupled non-linear differential equations. This quickly becomes impractical for simulating modern integrated circuits with a large number of transistors for the steep rise in cost in terms of speed and memory requirements. However, a simplified model, based on suitable assumptions, with minimum number of fitting parameters, can be readily implemented in circuit simulators. As outlined in section 2.4, a lot of works has gone into this approach of transistor modeling. G^4FET, with its four independent gates, provides different operating regions depending on its gate biases and thus, developing a compact model becomes very challenging. Based on its working mechanism and desired operating region, two models with their CAD implementation are described in this chapter.

6.2 Depletion All Around (DAA) Model

For a particular range of gate biases, G^4FET offers a conduction mechanism known as depletion-all-around (DAA) operation. When the top- and the bottom-gates are either depleted or inverted, a narrow wire like conduction path is formed in the center of the channel surrounded on all sides by depletion regions which is graphically illustrated in Figure 3.9. This operation mechanism provides many benefits such as high mobility, high transconductance, better subthreshold properties, excellent radiation hardness and high g_m/I_d ratio. A CAD implementation is done based on the physical modeling outlined in [24].

6.2.1 Model Formulation

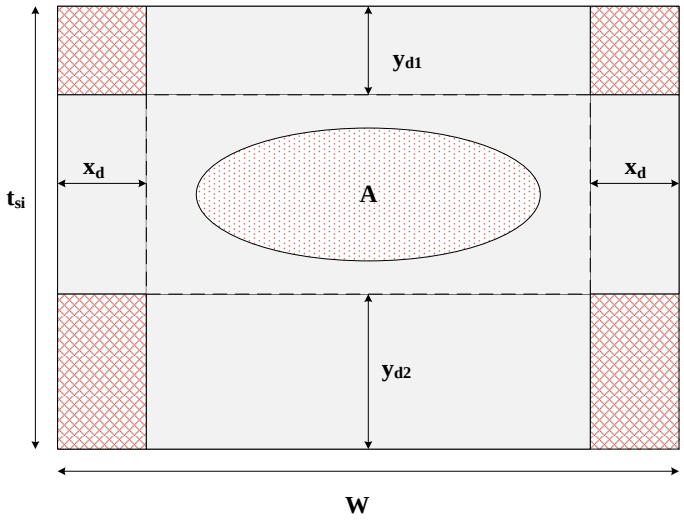


Figure 6.1: Schematic of the cross-section of a G^{4}FET in depletion all around operation.

When the transistor is operating in DAA mode above threshold and in non-saturation, the vertical and the horizontal depletion regions surround a conduction path of area A in the center. The depletion widths induced by the front and the back gates are denoted by y_{d1} and y_{d2}, respectively. The lateral depletion width is denoted by x_d, assuming equal voltage applied at both junctions. The center conduction path A is a neutral region where the carrier density, n can be assumed to be equal to body doping density, N_D. The lateral and the vertical depletion depths can be expressed [109] as,

$$x_d = \sqrt{\frac{2\epsilon_{Si}(V - V_{JG} + \varphi_b)}{qN_D}} \tag{6.1}$$

The vertical depletion widths for surface depletion are,

$$y_{d1} = \left(\frac{\epsilon_{Si}}{C_{ox1}}\right)\left[-1 + \sqrt{1 + \frac{2C_{ox1}^2(V - V_{TG} + V_{FB1})}{qN_D\epsilon_{Si}}}\right] \tag{6.2}$$

$$y_{d2} = \left(\frac{\epsilon_{Si}}{C_{ox2}}\right)\left[-1 + \sqrt{1 + \frac{2C_{ox2}^2(V - V_{BG} + V_{FB2})}{qN_D\epsilon_{Si}}}\right] \quad (6.3)$$

The vertical depletion widths for surface inversion can be expressed as,

$$y_{d1,2} = \sqrt{\frac{2\epsilon_{Si}(V - V_{JG} - 2\varphi_F)}{qN_D}} \quad (6.4)$$

C_{ox1} and C_{ox2} are the capacitances of the front gate oxide and the buried oxide, respectively; φ_F is the body Fermi potential, V is the channel potential varying between drain and source, N_D is the body doping concentration, ϵ_{Si} is the permittivity of Silicon and $V_{FB1,2}$ are the flat band voltages of the top- and the bottom-gates, respectively.

The inversion threshold for the top- and the bottom-gates can be formulated [109] as,

$$V_{T1} = V_{FB1} + \left(2\varphi_F + V_{JG}\right) - \frac{2\epsilon_{Si}qN_D(V - V_{JG} - 2\varphi_F)}{C_{ox1}} \quad (6.5)$$

$$V_{T2} = V_{FB2} + \left(2\varphi_F + V_{JG}\right) - \frac{2\epsilon_{Si}qN_D(V - V_{JG} - 2\varphi_F)}{C_{ox2}} \quad (6.6)$$

Then the drain current can be expressed [24] as,

$$I_D = \frac{q\mu_n N_D}{L}\int_0^{V_D} A(V)dV \quad (6.7)$$

In the ideal case with no interaction between the lateral and the vertical gates, the conduction area, A would be simply $(W - 2x_d)(t_{Si} - y_{d1} - y_{d2})$. However, due to the charge sharing between the lateral and the vertical gates, the area A is elliptical which is a little less than this rectangular area. The exact calculation, based on maintaining charge neutrality in the region requires solving two dimensional Poisson equation which is not feasible for CAD implementation. An empirical fitting parameter, δ can be used to account for this change in shape from rectangular to elliptical to express A as,

$$A = (W - 2x_d)(t_{Si} - y_{d1} - y_{d2}) - \delta * 2x_d * (y_{d1} + y_{d2}) \quad (6.8)$$

This model is implemented in Cadence™ using VerilogA. The integral is evaluated using the loop functionality with trapezoidal rule and is valid for non-saturation. With the increase in channel potential, the sectional area *A* gradually decreases and after it becomes zero, equation 6.7 is no longer applicable. The channel gets pinched-off and the transistor enters into saturation where the current remains the same.

6.2.2 Model Validation

The current-voltage characteristics is validated against TCAD data from [24]. The junction-gates are tied together and keeping two gate biases fixed, the third bias is changed and the resulting matching is shown.

In Figure 6.2, both the top- and the bottom-gate voltages are fixed at 0 V and the junction bias is changed from 0 to -1.5 V. The same procedure is done in Figure 6.3, except the bottom-gate voltage is changed to -3 V.

In Figure 6.4, the junction- and the bottom-gate voltages are fixed at 0 V and -3 V. The top-gate bias is changed from 0 V to -3 V. The same procedure is done in Figure 6.5, except the junction-gate voltage is changed to -1.5 V. In Figure 6.6, the bottom-gate is swept while keeping both the top-gate and the junction-gate fixed at 0 V. The mean relative error suggests reasonably good matching for different bias conditions.

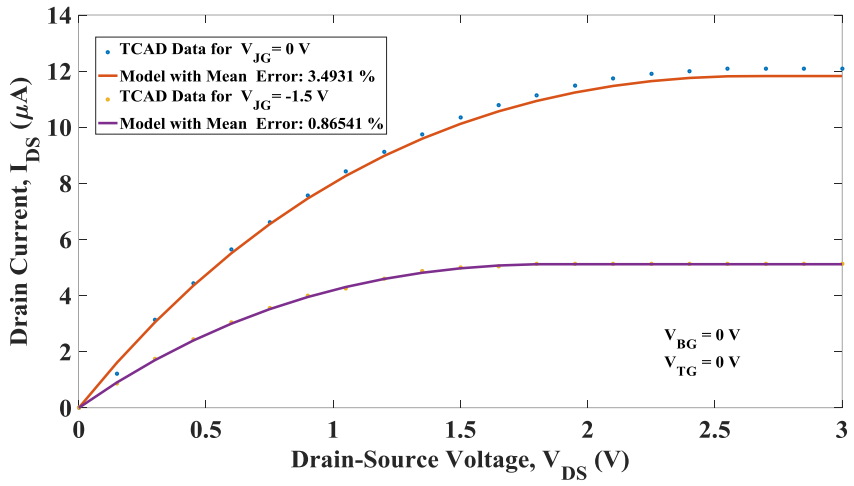


Figure 6.2: Comparison between test data and model for different junction-gate voltages, with both the top-gate and the bottom-gate biased at 0 V.

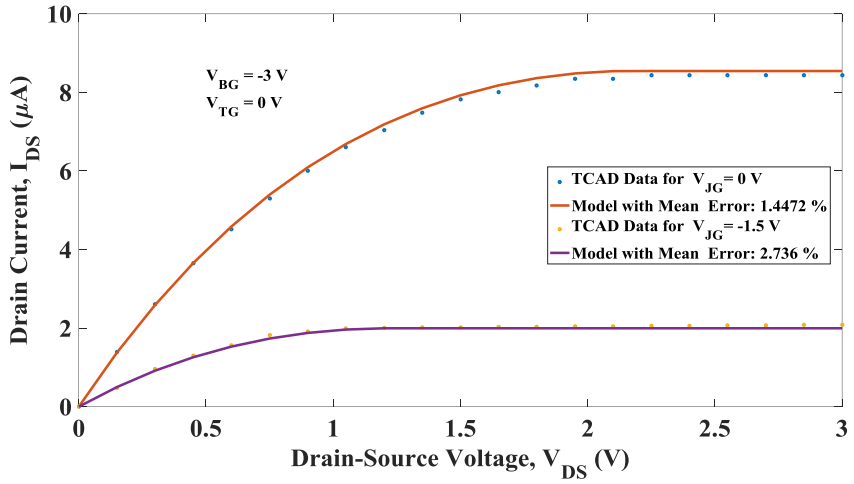


Figure 6.3: Comparison between test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 0 V and -3 V, respectively.

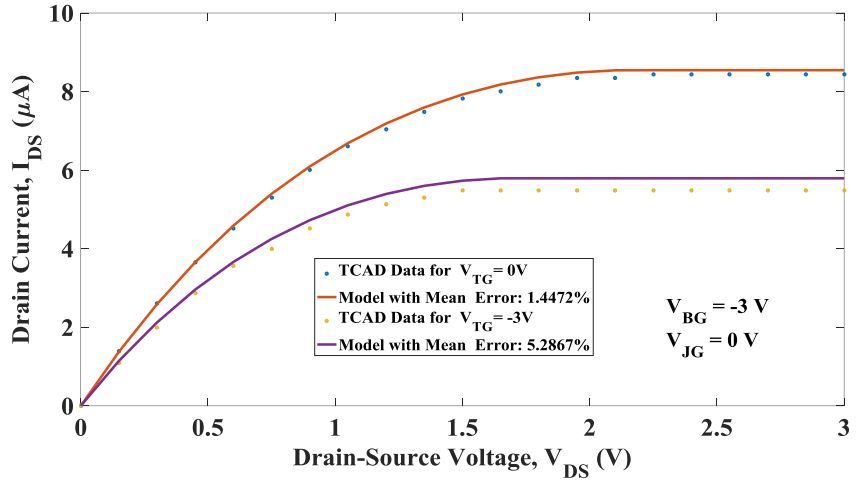


Figure 6.4: Comparison between test data and model for different top-gate voltages, with the junction-gate and the bottom-gate biased at 0 V and -3 V, respectively.

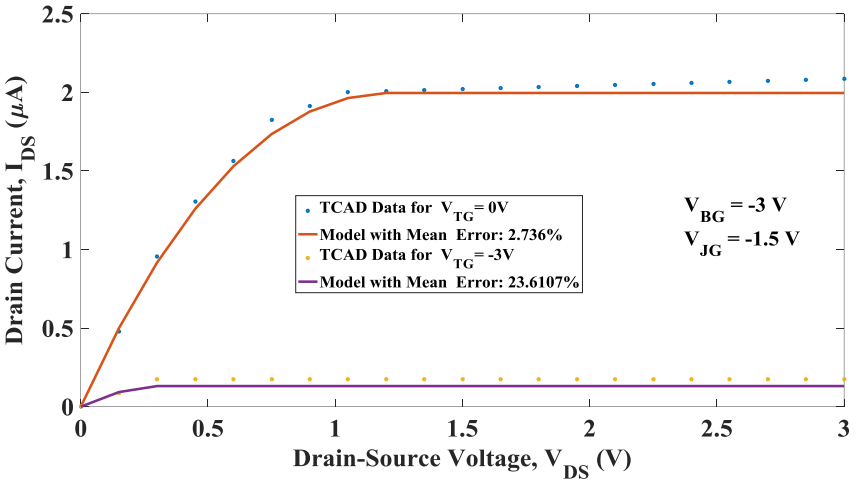


Figure 6.5: Comparison between test data and model for different top-gate voltages, with the junction-gate and the bottom-gate biased at -1.5 V and -3 V respectively.

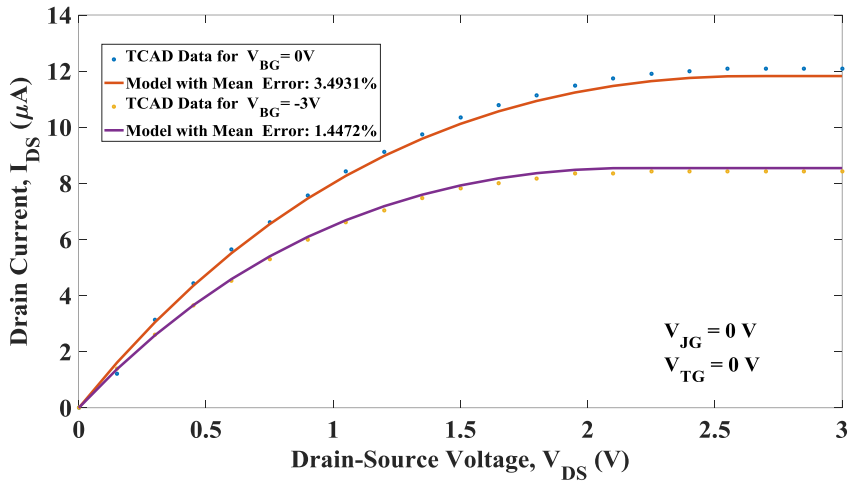


Figure 6.6: Comparison between test data and model for different bottom-gate voltages, with both the junction-gate and the top-gate biased at 0 V.

6.3 Front Surface Accumulation Model

For many applications of G^{4}FET such as analog multiplier, high voltage differential amplifier etc. the front surface needs to be accumulated and in that case, the accumulation layer adjacent to front gate oxide-semiconductor surface provides most of the current. The depletion all around model is not suitable for this operation.

In this section, a method is developed for emulating the behavior of a G^{4}FET working in this front surface accumulation mode using an accumulation mode MOSFET with a threshold voltage dependent on other gate biases. The volume conduction is also included using a JFET like conduction path.

6.3.1 Model Formulation

A number of terms is used in developing the model and most of these terms were introduced in section 5.2. The bottom-gate may be accumulated, depleted or inverted. However, the accumulated back gate provides a shunt leakage conduction path which is undesirable for most applications. Therefore, it is assumed that the back gate is never accumulated and only the condition for depleted or inverted back surface is considered. For these conditions, the top-gate accumulation threshold voltage, V_{TH} can be modeled as a function of other gate biases [21].

When the bottom-gate is in inversion i.e. $V_{BG} < V_{BG}^{inv}$

$$V_{TH} = V_{FB1} - \gamma\left(\frac{C_{JG}}{C_{ox1}}\right)(2\varphi_F + V_P) - TH_{mod} * \alpha\left(\frac{C_{JG}}{C_{ox1}}\right)(V_{JG} - V_P) \quad (6.9)$$

When the bottom-gate is depleted i.e. $V_{BG}^{inv} < V_{BG} < V_{BG}^{acc}$

$$V_{TH} = V_{FB1} - \beta(V_{BG} - V_{FB2}) + TH_{mod} * (\gamma - \alpha)\left(\frac{C_{JG}}{C_{ox1}} + \beta\frac{C_{JG}}{C_{ox1}}\right)\left(V_{JG} - V_P\right) \quad (6.10)$$

An extra parameter, 'TH_{mod}', standing for 'threshold modifier', is included for empirical fitting. The accumulation mode MOSFET Drain-current expression I_{DM} is similar to Shichman-Hodges equation [80] with some modification.

For triode region i.e. $V_{DS} < V_{TG} - V_{TH}$,

$$I_{DM} = K_p\left(1 + W_{mod} * V_{JG}\right) * \left(\frac{1}{(V_{TG} - V_{FB1})^{\theta}}\right)\left((V_{TG} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right)(1 + \lambda_M * V_{DS}) \quad (6.11)$$

For saturation region i.e. $V_{DS} \geq V_{TG} - V_{TH}$,

$$I_{DM} = \frac{1}{2}K_p\left(1 + W_{mod} * V_{JG}\right)\left(\frac{1}{(V_{TG} - V_{FB1})^{\theta}}\right)(V_{TG} - V_{TH})^2\,(1 + \lambda_M * V_{DS}) \quad (6.12)$$

The additional parameters are W_{mod} (junction-gate affect in conduction area shrinkage), θ (vertical field mobility affect) and λ_M (channel length modulation).

Similarly, there are two equations based on linear and saturation region for drain current I_{DJ} in JFET [110]. For linear region,

$$I_{DJ} = (\frac{2I_{Dss}}{V_P^2})(V_{JG} - V_P - \frac{1}{2}V_{DS})V_{DS}\left(1 + \lambda_J * V_{DS}\right) \quad (6.13)$$

For saturation region,

$$I_{DJ} = I_{Dss}(1 - \frac{V_{JG}}{V_P})^2\left(1 + \lambda_J * V_{DS}\right) \quad (6.14)$$

Here, I_{DSS} is the maximum saturation current and λ_J is the channel length modulation parameter for JFET. Then, the total drain-source current of the G^{4}FET will be,

$$I_{DS} = I_{DM} + I_{DJ} \quad (6.15)$$

6.3.2 Model Validation

For different top-gate bias, the junction-gate voltage has been swept from -3 V to 0 V and the resulting drain current versus drain-source voltage model data is tested against TCAD simulation data. In Figure 6.7, the top-gate voltage is fixed at 2.5 V and the junction-gate voltage is swept from -3 V to 0 V. The maximum error in this range is from V_{JG} = -1 V with 5.5825 %. In Figure 6.8, the top-gate bias is moved up to 3 V resulting in increased current for all four different junction-gate biases. The mean error has improved for this bias condition with the maximum error of 4.77 %.

In Figure 6.9, the top-gate voltage is biased at 3.5 V and the junction-gate is varied from -3 V to 0 V. The fit is reasonably good with the maximum error occurring for V_{JG} = 0 V with 4.6941 %. The isolines for different junction-gate bias for V_{TG} = 4 V is shown in Figure 6.10. The matching is similar as the previous figure with the maximum error of 4.842 % occurring at the junction-gate bias of 0 V. Figure 6.11 shows the isolines for 4.5 V at top-gate when the front surface is very

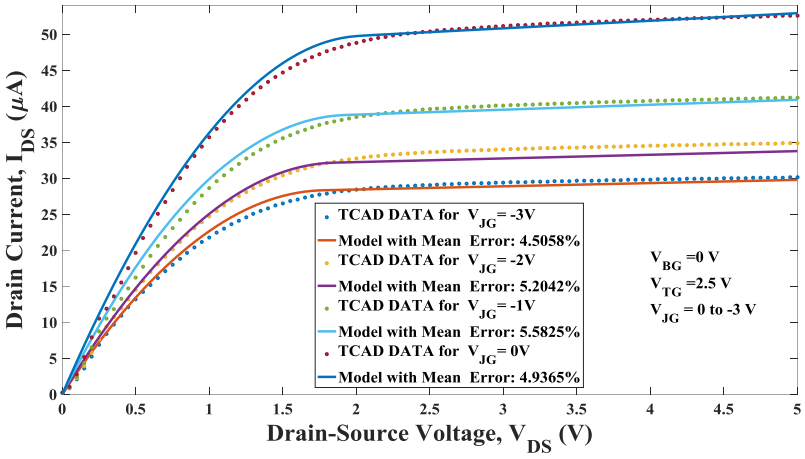


Figure 6.7: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 2.5 V and 0 V, respectively.

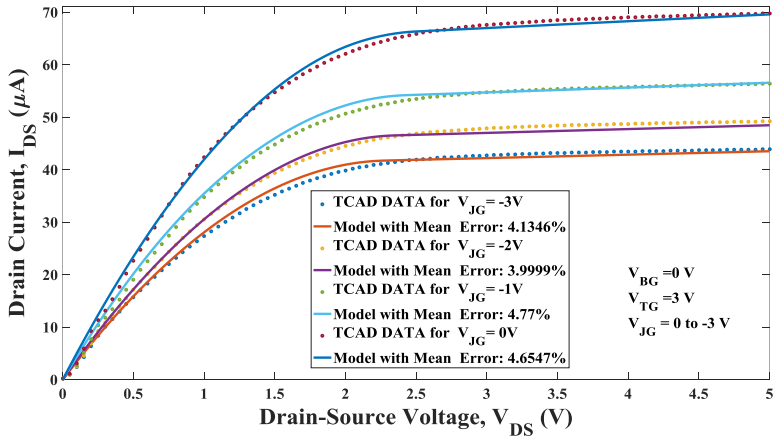


Figure 6.8: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 3 V and 0 V, respectively.

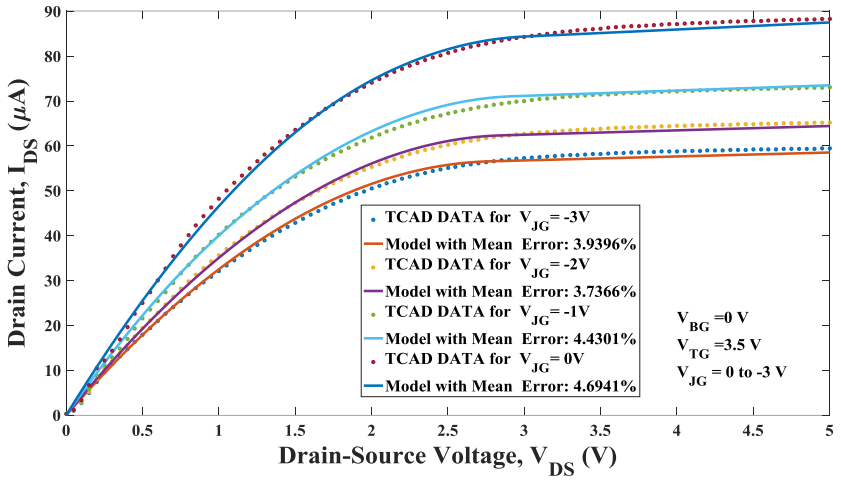


Figure 6.9: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 3.5 V and 0 V, respectively.

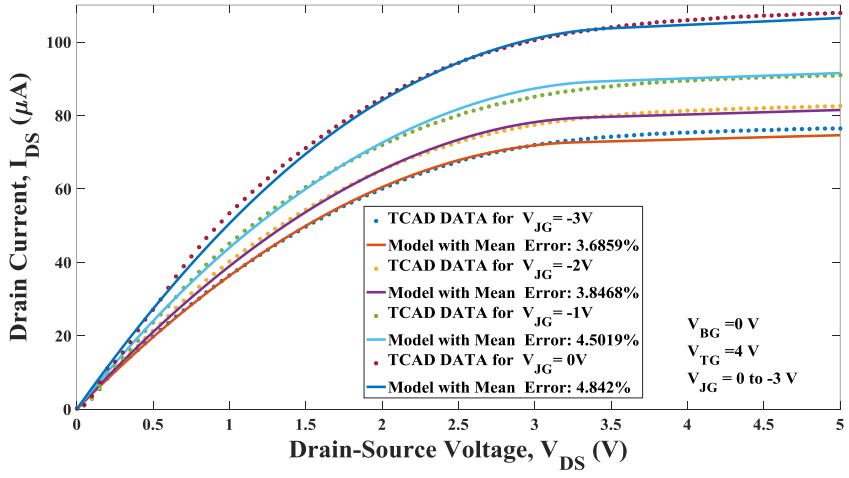


Figure 6.10: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 4 V and 0 V, respectively.

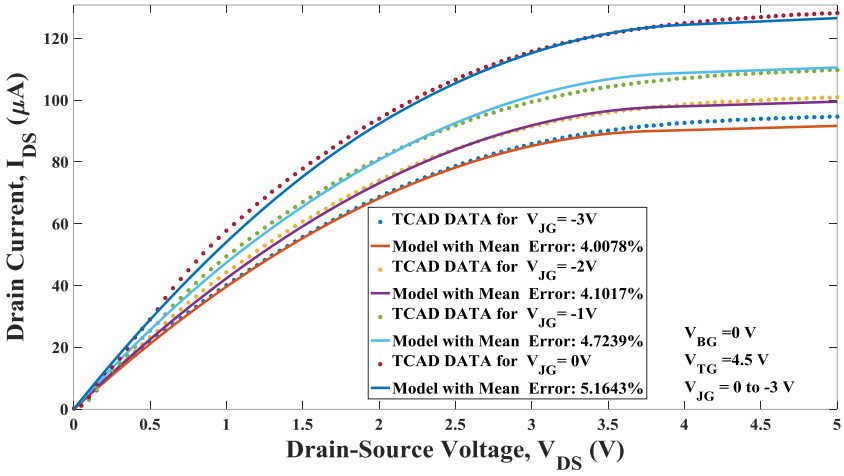


Figure 6.11: Comparison between isolines of test data and model for different junction-gate voltages, with the top-gate and the bottom-gate biased at 4.5 V and 0 V, respectively.

strongly accumulated. The matching is slightly worse compared to Figure 6.8 and Figure 6.9 with the maximum error of 5.1643 %.

6.4 Chapter Summary

Two compact models of G^{4}FET based on different gate biasing conditions are implemented in circuit simulator. The first model is built upon the working principle when the transistor is biased to operate in depletion-all-around condition. The second model is used to predict the transistor characteristics when the top-gate is accumulated, which is also used in several G^{4}FET applications. The same approach can be taken to develop higher order models with more fitting parameters for further improvement of the accuracy.

Chapter 7 - Conclusion and Future Work

7.1 Original Contributions

G^4FET is a relatively new member of the silicon-on-insulator family and was first reported in 2002 [15]. Several works have been done so far to model the working mechanism of the device. In [21], the threshold potential of the top-gate was derived as a function of remaining gate voltages with full depletion approximation and an assumption of parabolic potential distribution between lateral gates. A charge control method was used in [24] to derive the drain current equation under depletion all around operation using a single fitting parameter. A surface potential based non-linear solution of drain current and gate capacitance was formulated in [28] for accumulated top-gate condition.

However, to really utilize the novel properties of G^4FET, a suitable SPICE model is essential. Until now, no significant work has been done for SPICE implementation of G^4FET. This work includes three different approaches towards modeling G^4FET for circuit implementation. The first approach is numerical modeling, which uses experimental data for determining a reliable expression for device characteristics. Four different approaches have been outlined, each with its own merits and demerits.

The first approach is a multivariate Lagrange polynmial interpolation model in which Chebyshev nodes are used to improve the accuracy and reduce oscillation. The second numerical model is based on multidimensional Bernstein polynomial approximation. This approach is not as accurate as Lagrange's method, but it is better at preserving shape of the original data, which may be significant for some analog applications.

However, both these models have one problem. The order of the model increases with chosen data points which make the dual requirement of good accuracy and small computational time very difficult to achieve. The third method provides a solution in the form of multivariate regression polynomial model. Both *n*-channel and *p*-channel transistors have been modeled using the method and verification with experimental data using circuit implementation is also demonstrated.

The last numerical method is the multivariate linear and cubic spline interpolation model. The first three numerical methods use a single polynomial to represent the entire biasing region of the transistor. However, single polynomials are prone to sudden oscillation and local noise or irregularities can affect global behavior. Spline or piecewise interpolation solves these problems. Both linear and cubic spline models are used in this work to develop the model. Cubic spline models are used in several circuit implementations.

Apart from numerical modeling, a different macromodel approach is also pursued. This approach originates from the observation that G^4FET combines MOSFET and JFET action in a single silicon body. Therefore, already existing standard SPICE models of MOSFET and JFET are combined in a subcircuit with suitable modification to emulate G^4FET characteristics. This model is easily implemented in circuit simulator, quite fast and has successfully reproduced the results from a multitude of experimentally demonstrated analog and digital circuits.

The third approach was CAD implementation of simplified physics-based compact model. Two such models are shown. The first work is based on the analytical work in [24] and covers the biasing condition known as depletion all around. However, it is limited to this biasing regime and not applicable for situation where the top-gate is accumulated with available surface conduction. This mode of operation is very useful in certain applications such as analog multiplier, high voltage

differential amplifier etc. A second model compact model combining basic MOSFET and JFET equations with suitable fitting parameters is proposed to account for surface accumulation behavior.

Therefore, the original contributions of this research can be summarized as:

- Successful SPICE implementation of G^4FET model and verification using experimental results.
- Model formulation and SPICE implementation of four different numerical models for G^4FET, namely, 1) multivariate Lagrange polynomial interpolation model, 2) multivariate Bernstein polynomial approximation model, 3) multivariate regression polynomial model and 4) multivariate linear and cubic spline interpolation model.
- Development of a macromodel of G^4FET combining existing models of MOSFET and JFET transistors and implementation in circuit simulator for simulating innovative analog and digital circuits. Model verification using comparison between simulation and experimental results.
- Development of two simplified physics-based compact models for CAD implementation suitable for different biasing conditions. Verification of the current voltage characteristics using comparison between TCAD data and model prediction.

7.2 Dissertation Summary

The main goal of this work was to develop SPICE models for G^4FET. Three different approaches have been adopted to achieve this goal. The first approach is the numerical method

which constitutes the bulk of this work. This approach is used to develop four different numerical models for both *n*-channel and *p*-channel G^4FET from both TCAD and experimental data which are implemented in circuit simulator. The second approach uses a macromodel combining MOSFET and JFET models based on the underlying physical operation of G^4FET. This model has been implemented in circuit simulator and successfully reproduces results from several innovative analog and digital applications. The third approach involves developing two simplified compact models with suitable model parameters to account for two different operating conditions of G^4FET.

The challenges associated with extreme scaling of bulk silicon MOSFET has driven researchers to look for 'end-of-roadmap' devices. G^4FET with its unique configuration and functionality may prove to be a suitable transistor for the next generation circuit design. SPICE models developed in this work can help designers to come up with innovative circuits with higher speed, smaller footprint and lower power consumption.

7.3 Future Works

Different modeling approaches have been developed and implemented in this dissertation. Still, there is room for further contributions in the CAD model development of a G^4FET. Some possible future works are mentioned below:

1. Extending the numerical models to include temperature, terminal capacitance, epi silicon thickness, noise model etc.
2. Inclusion of higher level MOSFET and JFET models in the macromodel for better accuracy.

3. A physics-based compact model valid under all possible operating conditions with suitable parameter extraction methodology.

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Vita

Md Sakib Hasan was born in Comilla, Bangladesh in 1986. He received his B.Sc. degree in Electrical and Electronics Engineering from Bangladesh University of Engineering and Technology in 2009 and Ph.D. degree in Electrical Engineering from the University of Tennessee at Knoxville in August, 2017. During his graduate study, he was involved in semiconductor device modeling and IC design for sensor applications. He is interested in modeling new emerging devices to meet the scaling challenge faced by semiconductor industry. He will join as a Post-Doctorate Research Associate in the 'Secure and Efficient NanoElectronic Computer Architectures (SENECA)' group in the department of Electrical Engineering & Computer Science at the University of Tennessee upon approval of his OPT application.