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I am submitting herewith a thesis written by Stephen Wesley Milam entitled "Development of a Wideband Amplifier for Use in a Measurement System for the Detection of Prebreakdown Pulses in Solid Dielectrics." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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DEVELOPMENT OF A WIDEBAND AMPLIFIER FOR USE IN
A MEASUREMENT SYSTEM FOR THE DETECTION OF PREBREAKDOWN
PULSES IN SOLID DIELECTRICS

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ABSTRACT

A high-gain wideband amplifier was needed for a system that measures prebreakdown pulses in solid dielectrics. This paper describes the development of an amplifier for this pulse measurement system.

The amplifier has a voltage gain of 99 (40 dB) and a bandwidth extending from 130 Hz to 115 MHz. The small-signal rise time of the amplifier is 3.2 ns and the rise time is 4.4 ns for a 1-Volt pulse into a 50 ohm load.

Designs for wideband amplifiers developed over the last ten years were reviewed, and a configuration was selected and modified for this application. Circuit biasing was described, and extensive AC and noise analyses were conducted. The results of these analyses were compared with those obtained from a computer model for the circuit. The circuit was fabricated and experimental results are included along with suggestions for improving the design.

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CHAPTER 1

INTRODUCTION

Application of Wideband Amplifiers in the Measurement of Prebreakdown Pulses in Dielectric Materials

High performance measurement systems often contain amplifiers that can limit the overall bandwidth of the system. Two such systems are the one developed by Wintenberg et al.¹ and the one described by Dorris². The bandwidth is limited in each system by the bandwidth of the voltage amplifiers used. In the Wintenberg system, an 80 MHz voltage amplifier limits the system bandwidth to 54 MHz, and in the Dorris system an 80 MHz amplifier is a limiting factor in the system's 30 MHz bandwidth. Both of these systems are used in research requiring the measurement of prebreakdown pulses in dielectric materials. This research aims to discover the mechanism that causes water treeing in solid dielectrics.

Eichhorn defines treeing as "an electrical breakdown phenomenon[,]...that type of damage which progresses through a dielectric section under electrical stress so that, if visible, its path resembles the form of a tree."³ He notes that "treeing has been observed to occur in all solid organ-

ic dielectrics tested and was observed in paper/oil insulation systems many years ago. Treeing may or may not be followed by complete electrical breakdown of the dielectric section in which it occurs, but in solid extruded dielectrics it is the most likely mechanism of electrical failures that do not occur promptly but rather appear to be the result of an aging process."

Although much research has been conducted on treeing, "there is insufficient understanding or agreement among researchers to present very much of the subject as fact."³ The importance of the phenomenon is that it "relates to the future performance of many miles of polyethylene-insulated power cables currently in underground service."

Since water treeing entails the motion of water, which has a high dielectric constant, as well as any ionic impurities contained in it (notably sodium), detectable signals may be produced.⁴ These signals include current pulses that correspond to either the motion of charged particles in the water as it flows into new cavities in a water tree or charge flow in the ground electrode to accommodate energy changes in the polyethylene being observed. These energy changes result from changes, caused by water motion, in the dielectric constant of the polyethylene section under study.

Reproduction of the current pulses described above requires wideband, low-noise measurement systems. "Pulses of

interest may have risetimes less than 10 ns, durations less than 50 ns, and peak amplitudes lower than 1 μA ."⁵

Design Requirements

The system used by Wintenberg et al. to measure the small current pulses had two main components. The first was a preamplifier with a gain of 5000 V/A and an 87 MHz bandwidth, and it was followed by an amplifier with a voltage gain of 100 and a bandwidth of 80 MHz. The system bandwidth was approximately 54 MHz and its gain was 500 V/mA. The preamplifier had an rms (root-mean-squared) input noise current of 25 nA.

Improving this measurement system would require an amplifier with a bandwidth greater than 80 MHz. An amplifier bandwidth of 100 MHz would extend the bandwidth of the system to 60 MHz, where the preamplifier, not the main amplifier, would be the limiting factor. The rms noise voltage at the input of the amplifier would have to be significantly less than 125 μV ($5000 \text{ V/A} * 25 \text{ nA}$) so that the sensitivity of the system would not be reduced, and the input and output impedances of the amplifier had to match the 50 Ω characteristic impedance of the system.

Other requirements for the amplifier included the ability to drive at least ± 1 Volt into a 50 Ω load and a gain nonlinearity of no more than 5%.

Thesis Organization

A review of wideband amplifiers appropriate for this thesis application is conducted and summarized in Chapter 2. The search focuses on amplifiers developed within the past decade, and is divided according to the devices used in the fabrication process. The main groups of devices studied are heterojunction bipolar transistors, silicon bipolar transistors, gallium arsenide MESFETs, and silicon MOS transistors.

In Chapter 3 the design considerations leading to the selection of a wideband amplifier configuration for further development are presented, and the modifications to produce the final amplifier design are delineated.

An extensive analysis of the final amplifier developed is carried out in Chapter 4. The biasing is described and expressions are developed which represent the frequency response and the noise characteristics. The circuit is modelled using PSpice and results from this model are compared to the results from the hand calculations. Finally, the printed circuit board layout is designed.

A summary of the experimental results is contained in Chapter 5. These results are then compared to those predicted in Chapter 4.

Chapter 6 lists conclusions and suggested improvements. It also describes the effect of the developed amplifier on the measurement system described in Chapter 1.

CHAPTER 2

REVIEW OF LITERATURE

Before designing a fast amplifier, recent work in developing amplifiers that operate from DC to high frequencies was investigated. DC-coupled wideband amplifier designs created over the past decade can be grouped into four main classifications: 1) GaAs/AlGaAs heterojunction bipolar transistor amplifiers, 2) silicon bipolar amplifiers, 3) GaAs MESFET amplifiers, and 4) silicon MOS amplifiers. The characteristics associated with each class of amplifier are described below.

Several of the terms used to evaluate the amplifiers should be defined. Unless otherwise noted, the term "gain" refers to s_{21} , the square root of the power gain, as defined by DeLurio and Hadley⁶ and covered in detail in Hewlett-Packard application note 95.⁷ s_{21} is equivalent to voltage gain if the source and load impedances (Z_s and Z_L , respectively) are identical to the reference impedance (Z_0). Otherwise the voltage gain (A_v) can be found from

$$A_v = s_{21} * \frac{Z_L}{Z_s} * \frac{Z_0 + Z_s}{Z_0 + Z_L} . \quad (2.1)$$

"Stability" refers to stability against oscillations, and "noise figure" is defined as the ratio of the total output noise power to the output noise power due to the source. The noise figure can be deceptive since it can be altered by changing the source resistance without changing the equivalent noise of the amplifier, so equivalent noise voltages and currents are given when available.

Heterojunction Bipolar Transistors

The first class of wideband amplifiers consists of amplifiers employing GaAs/AlGaAs heterojunction bipolar transistors (HBTs). HBTs have several advantages over Si bipolar transistors (BTs), including low base resistance, reduced base-emitter capacitance and electron transit time, and higher Early voltage.⁸ Also, the cutoff frequency of HBTs is greater than that of Si BTs.⁹ The HBT has many advantages over a field-effect transistor (FET) as well, including high f_T (cutoff frequency), ability to handle large currents, high transconductance, low output conductance, low $1/f$ noise, directly-controllable breakdown voltage, and large voltage amplification values.⁸ The base-emitter on-voltage of the HBT is approximately 1.5 V. This voltage, higher than the 0.8 V base-emitter on-voltage for Si BTs, can eliminate the need for the level-shift diodes in some

configurations.¹⁰ The Early voltage for these devices is usually above 100 V, and values of the DC current gain, h_{fe} , are generally around 10 or 20 for fast transistors, but devices have been fabricated with h_{fe} over 1000.

The majority of the HBT designs reported were compact, two-stage amplifiers as shown in Figure 2-1. Yamauchi and Ishibashi first presented this design in 1987 with a 4 GHz bandwidth and 11 dB gain,¹⁰ and the following year they presented the same design with the improved characteristics of 8.5 GHz bandwidth and 12 dB gain.¹¹ These improvements were attained through the use of HBTs with a near-ballistic collection structure, or ballistic collection transistors (BCTs). These transistors have higher cutoff frequencies (50 GHz for the ones used in this design) and higher power gains than the HBTs used in the first circuit, and they are biased at higher collector voltages ($V_{CE} = 3$ V) than the original HBTs. The authors adjusted the doping profile of the transistors so that the f_T versus V_{CE} curve peaked at a higher value of V_{CE} ($V_{CE} = 2.5$

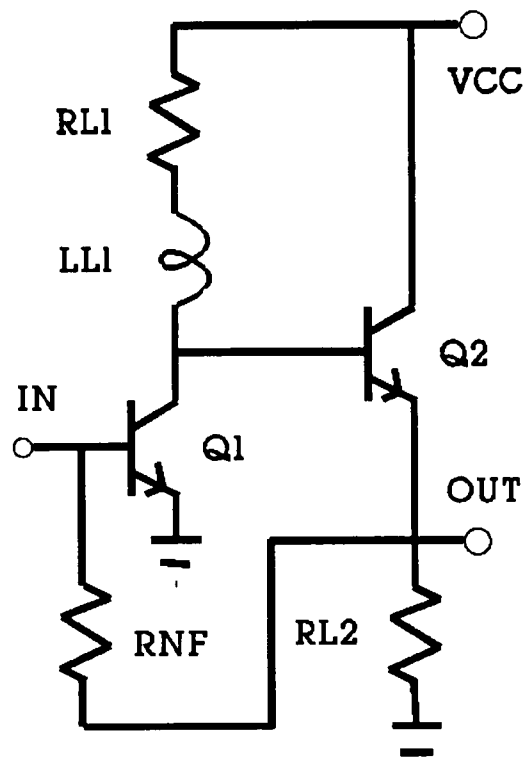


Figure 2-1. Heterojunction bipolar transistor circuit.

V), which was optimized for a circuit with a 5 V power supply. Thus, the f_T at the operating point of the circuit was 70 GHz, a very high value that approached the authors' previously reported high value of 105 GHz.¹² The inductance L_{L1} was included to create a peaking effect in the frequency response, and in their simulation the peaking increased the bandwidth from 7 GHz to 10 GHz.

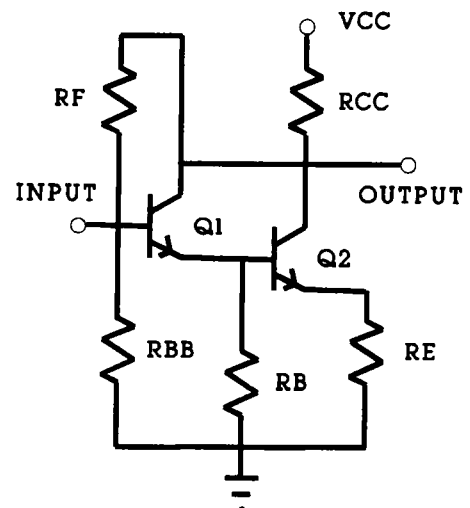


Figure 2-2. Darlington connected HBT amplifier.

In 1989, two Darlington connected feedback amplifiers were introduced (Figure 2-2). One, presented by Topham et al.,¹³ has a 12 dB gain with a 3 GHz bandwidth. It uses transistors with an f_T of 40 GHz, and the input-output-ground pad layout is the same as that of a discrete transistor, implying that this design could easily be incorporated into other circuits as a gain block. The other amplifier, designed by Koboyashi et al.,¹⁴ boasts an 11 dB gain with a -3 dB frequency of 10 GHz using a simpler MMIC (monolithic microwave integrated circuit) technology than is used for most other high speed circuits. Koboyashi et al.'s transistors have f_T 's in the 20-30 GHz range and h_{fe} 's between 50 and 100. The Darlington configuration has the advantages of both high input impedance and current gain.

Slightly more complicated circuits have also been described. For example, Nakajima, Yamauchi, and Ishibashi described a differential amplifier (Figure 2-3) that uses HBTs to achieve a 20 dB gain with a 9 GHz bandwidth.⁹ Also, Ishihara et al. characterized a differential amplifier,¹⁵

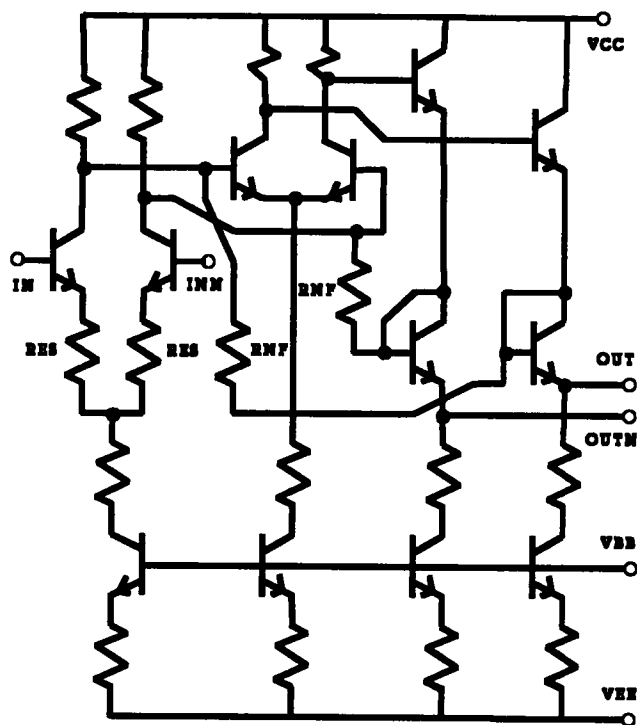


Figure 2-3. HBT differential amplifier.

which, along with a 9 GHz bandwidth, realizes a controllable gain between 8 and 20 dB (Figure 2-4). One of the main features of their amplifier is the use of parallel feedback transistors: the feedback network is not purely resistive, but contains a transistor as well as a resistor. The authors explain that this method not only yields a broader band-

width, but also gives greater control over the output DC levels.

The highest reported f_T of the HBTs was 70 GHz (by Nakajima, Yamauchi, and Ishibashi⁹), while the other f_T values ranged from 17 to 50 GHz.

Silicon Bipolar Transistors

Many designers have employed silicon bipolar transistors in the fabrication of wideband amplifiers. These designs require very fast transistors, and Morii, Taniguchi, and Fukushima reviewed seven of the fastest discrete low-noise transistors available in 1989.¹⁶ The f_T 's of these devices range from 2.3 to 10.0 GHz, and their h_{fe} 's range from 40 to 150. Their noise analysis shows that the base spreading resistance, r_{bb} , was between 2 Ω and 98 Ω for these devices, and in most cases was around 15 Ω , which means that most of these devices are appropriate for low noise work.

The simplest Si BT design presented is a pair of Darlington-connected transistors with resistive feedback.¹⁷ The designers present a whole family of monolithic amplifiers, of which the highest performance is a gain of 12 dB with more than 3 GHz bandwidth and a 6 dB noise figure. Several three-stage designs have also been described, including one discrete design¹⁸ consisting of a

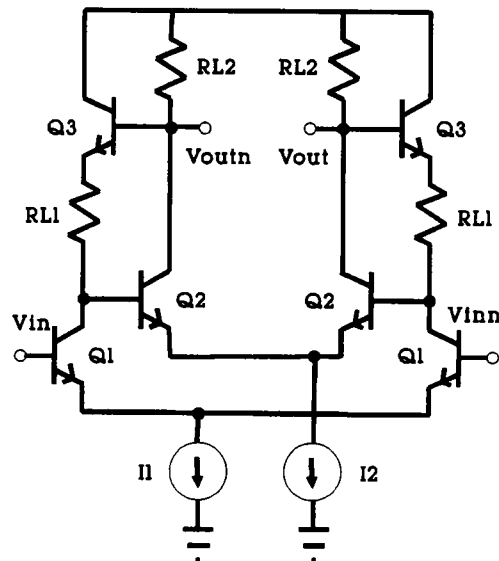


Figure 2-4. HBT controllable gain differential amplifier.

common-collector front end and a common-emitter stage inside a feedback loop with an emitter follower output stage. The authors cite removing the effect of the Miller capacitance and reducing the influence of the base spreading resistance as reasons for selecting a common-collector as the input stage. The resulting circuit has a 100 MHz bandwidth and an input equivalent noise current less than 2 pA/rt Hz. A slightly different configuration¹⁹ uses a common-emitter as the input stage followed by a Darlington pair with multiple feedback loops. Different bias points produced a 1 GHz bandwidth with 32 dB of power gain and a 6 pA/rt Hz input equivalent noise current or a 3 GHz bandwidth with a power gain of 26 dB and a 5 pA/rt Hz equivalent noise current. The small die and single power supply needed for the circuit allowed these amplifiers to be put into standard microwave transistor packages.

Other amplifiers used a common-emitter front end followed by a common-collector. Ohara et al.²⁰ employ this configuration with shunt-series feedback and an emitter follower output stage yielding a 22 dB gain with a 2 GHz bandwidth and 3.5 dB noise figure, while Meyer and Blauschild use it with a common-emitter output stage²¹ to yield a bandwidth measured as 184 MHz and a transresistance of 7.45 k Ω (Figure 2-5). Meyer and Blauschild use shunt-series feedback around all three stages of the preamplifier and point out the advantages of using a common-emitter front end over

a cascode input stage, namely that the Miller capacitance of Q1 dominates the input capacitance so that the circuit is relatively insensitive to capacitive loading at the input.

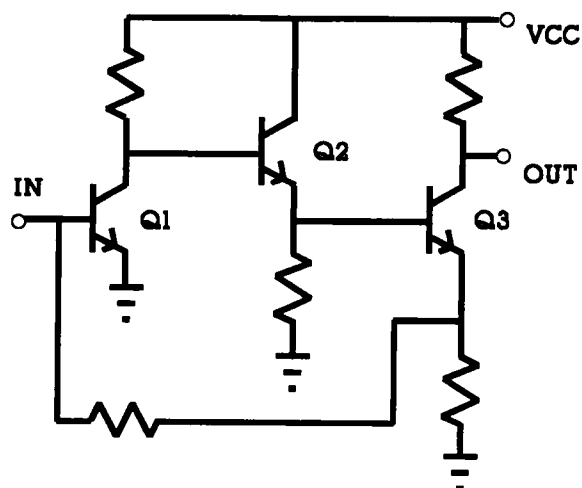


Figure 2-5. Transresistance amplifier using Si bipolar transistors.

Ohara et al. improved their own design the following year,²² reporting a 23 dB gain with a 3.7 GHz bandwidth, although this design had a 4.5 dB noise figure. They discuss their approach to dealing with the problem of coupling the output signal back to the input through the power line, namely that the power supply line for the IC (integrated circuit) was separated and attached to different terminal pads on the chip for each amplifier stage of more than 20 dB gain.

Utilizing multiple feedback loops, Meyer and Blauschild also present a three-stage design,²³ which possesses a 700 MHz bandwidth with 18 dB gain and a 4.4 dB noise figure (Figure 2-6). Its basic topology is a common-emitter front end followed by a Darlington connected output stage. Four years later, Signetics Corporation introduced the same circuit as the low-priced NE5205,⁶ with a gain of 20 dB, a 600

or 650 MHz bandwidth (depending on the packaging), and a 6 dB noise figure for a 50-ohm system. They explain the function of the four feedback loops within the amplifier and give advice on methods for mounting uhf chips to a circuit board. The circuit and its multiple feedback technique are based on a

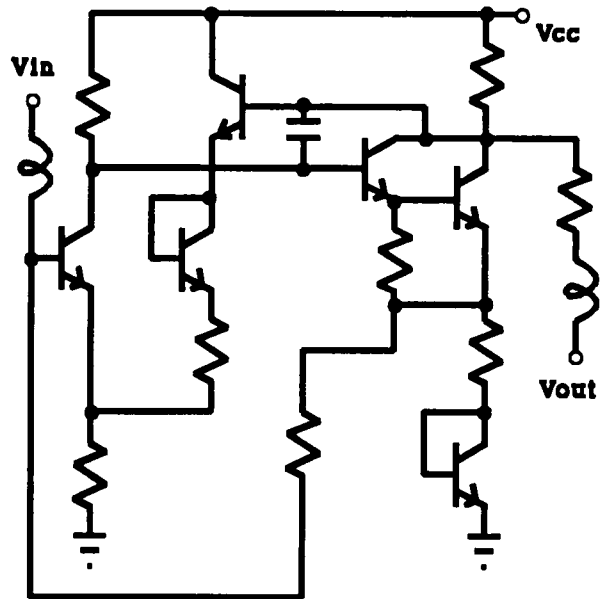


Figure 2-6. Bipolar transistor design using multiple feedback loops.

design presented in 1977 by Chan and Meyer,²⁴ which attained a 20 dB gain with a 250 MHz bandwidth.

Recently, Ishihara and Konaka published a three-stage design that achieved a 30 dB gain with a bandwidth of 3.5 GHz through the use of a peaking technique and two feedback methods.²⁵ The input stage has a common-emitter cascaded with a common-collector inside a parallel feedback circuit designed to yield wide bandwidth, low input impedance, and low noise characteristics. Since this configuration has a tendency to oscillate, the authors performed extensive analysis to ensure its stability. The output stage, a cascade of two emitter follower stages, incorporates a parallel feedback transistor in its feedback loop, providing more

gain and a broader bandwidth than a more conventional feedback circuit. An adjustable peaking circuit was included to increase the bandwidth further and avoid any parasitic oscillation due to excess peaking.

Two four-stage amplifiers have been produced as well. One of them²⁶ is realized as a common-collector front end feeding a common-emitter and then a common-base stage (in a cascode configuration) with an emitter follower output stage, and it has a frequency response with a single pole at 100 MHz. The wide bandwidth is facilitated by the common-collector input stage, which greatly decreases the effect of Miller capacitance, emitter-base capacitance, and base spreading resistance on the frequency response.

The other four-stage design is an automatic gain control (AGC) preamplifier²⁷ that has the same topology as the previous circuit except that the two common-base stages are connected in parallel, driving two emitter follower output stages, which are summed and fed back to the input, resulting in a 220 MHz AGC amplifier with an equivalent input noise current of 3 pA/rt Hz. The maximum transimpedance of the preamplifier is 18 k Ω . The advantages listed by the designers include the ability to use a fixed gain amplifier as the main amplifier and the absence of a large gain requirement for the main amplifier since the preamplifier transimpedance was so high.

An alternative to these types of designs is to use both Si BTs and GaAs MESFETs in the amplifier circuit, as Hullett and Moustakas have done.²⁸ They assert that the optimum noise performance is achieved by using a GaAs MESFET in the first stage of a (transimpedance) preamplifier since these devices have a "high transconductance and low capacity." These characteristics render the thermal noise of the feedback resistor the dominant factor in determining the noise performance of the amplifier. The authors point out the advantages of having the input device (in a common-source configuration) driving a shunt feedback stage instead of a common-base stage. Both stages have low input impedance but the shunt feedback stage contributes more to the loop gain, allowing a larger feedback resistor to be used and providing more stability to the design. A third stage is also added, a common-source with series feedback, and the authors demonstrate how to optimize the design for maximum bandwidth and for minimum noise, with the results of either an open-loop voltage gain of 41 (32 dB) and 285 MHz bandwidth, using a 5.1 k Ω feedback resistor, or a gain of 161 (44 dB) and 112 MHz bandwidth using a 51.1 k Ω feedback resistor (which reduces the thermal noise contribution of the feedback resistor).

In 1982, Moustakas et al. provided an analysis of the differences between using a bipolar junction transistor (BJT) and a MESFET, both fabricated in GaAs, as the input

device in an optical transimpedance preamplifier.²⁹ Their original circuit consisted of a common-source MESFET input stage followed by two common-emitter stages, the first with shunt and the second with series feedback. When a BJT was substituted for the input MESFET in this 200 MHz amplifier, the result was an increase of only 1.5 dB in the input equivalent noise current, and when the amplifiers were equalized to 400 MHz, the amplifier with the BJT input device had a noise penalty of only 1 dB. Their analysis took into account only the frequency-independent (white) component of the noise.

GaAs MESFETs

Wideband amplifiers have also been successfully fabricated exclusively from GaAs MESFETs. The advantages in using GaAs as a semiconductor include "weak-field mobility and maximum drift velocity [which] are, respectively, 5 and 2 times greater than in Si. Other important features are the large forbidden band width and the negative differential conductivity."³⁰ Robert Pucel³¹ summarizes the advantages and disadvantages of GaAs integrated circuits and compares them to silicon ICs. He explains the importance of using monolithic circuits, where "all active and passive circuit elements or components and interconnections are formed into the

bulk, or onto the surface, of a semi-insulating substrate by some deposition scheme." The benefits of using monolithic circuits were that they provide a less expensive method of producing many identical circuits, that without wire bonding the circuits are also more reliable, that the circuits are smaller and without many of the parasitics that inhibit the wideband response, and that circuits with different functions can be integrated on a single chip. He also cites some drawbacks to the monolithic approach, which include a small device/chip area ratio, the difficulty encountered in adjusting a circuit for purposes of either optimizing or debugging it, the problem of excessive crosstalk, and an inability to integrate high power sources, but he suggests methods of dealing with these obstacles.

After comparing silicon and gallium arsenide based on their utility as a substrate material, Pucel concludes that for high-frequency and/or high-power applications, GaAs was the substance of choice. Some of his reasons are that the resistivity of semi-insulating silicon was too low and that the carrier mobility of silicon is less than one sixth the carrier mobility of gallium arsenide. SOS (silicon-on-sapphire) technology offers a solution to the first problem by using sapphire, which has a resistivity greater than semi-insulating GaAs and much greater than semi-insulating silicon, as the substrate material. Pucel lists this fact, coupled with the considerations that silicon technology is

older and more well-developed than gallium arsenide technology and that the MESFET technology developed with GaAs could be employed with silicon also, as reasons to continue the evolution of silicon technology, but he still preferred GaAs for high-frequency, high-power roles. Pucel also explains several technical factors concerning monolithic design and presents a summary of the state-of-the-art circuits in 1981.

In 1978 Van Tuyl introduced a GaAs MESFET amplifier that had a 17.5 dB midband voltage gain and 4 GHz bandwidth, with an equivalent input noise voltage of 6.6 nV/rt Hz (17.2 dB noise figure).³² The design basically consists of a common-source input driving a source follower output stage. The output is fed back through an FET configured as a variable resistor into the gate of a MESFET whose drain and source are connected in parallel with the input transistor. The active feedback technique adds more gain to the feedback loop (and thus to the loop transmission) than purely resistive feedback, while the RC combination in the feedback path produces a zero, and thus a variable peaking effect, in the frequency response. The same topology without the RC network in the feedback loop (shown in Figure 2-7) was presented in 1981 by Hornbuckle and Van Tuyl³³ in four different cascaded combinations with common-source output drivers. These combinations include a three-stage cascaded amplifier exhibiting approximately 23 dB of voltage gain with almost 2

GHz bandwidth, two two-stage cascaded amplifiers (18 dB voltage gain with 1.5 GHz bandwidth, and 12 dB voltage gain with 4 GHz bandwidth) with different gate widths for the output drivers, and a single-stage design utilizing inductor peaking to improve the bandwidth to 5 GHz (for 10.5 dB gain). The noise figure measured at 1.5 GHz for two of the amplifiers is roughly 19 dB but the corner frequency

of the $1/f$ noise is rather high, between 30 and 100 MHz.

Other variations on the same basic topology were suggested by Hornbuckle³⁴ in 1981, yielding voltage gains between 10 and 32 dB with unity gain bandwidths from 3.5 to 4.5 GHz.

The noise figures given for two of these amplifiers (for 50 Ω input termination) are 16.4 and 16.8 dB (measured at 1.5 GHz) with a low-frequency noise corner around 100 MHz.

Imai et al. in 1983 introduced a circuit³⁵ designed to overcome the problems with noise figure and input match encountered by Hornbuckle and Van Tuyl. Their solution was to use resistive instead of active feedback with virtually the same circuit (common-source input driving a source follower with a common-source output driver). The authors also employ an FET with a larger gate width in the input stage to

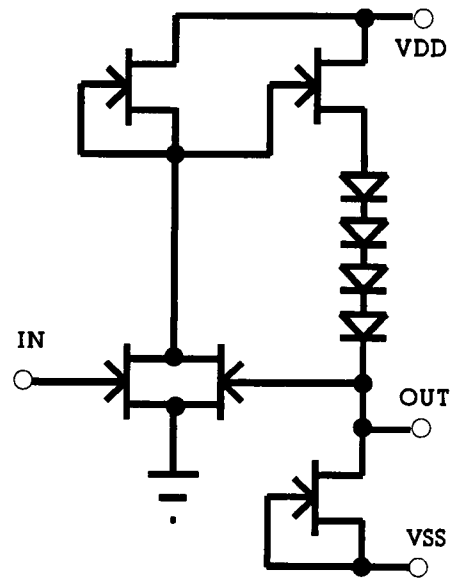


Figure 2-7. Single-stage cascode circuit.

improve both the noise figure and the bandwidth. Two amplifiers were fabricated with slightly different resistor values, with the characteristics of 9.6 dB gain and 4 GHz bandwidth for one amplifier, and 12.4 dB gain and 3 GHz bandwidth for an amplifier with the resistor values doubled (approximately). The first amplifier had a 7.2 dB noise figure at a frequency of 1 GHz. The following year Imai et al. published designs for amplifiers with improved gain.³⁶ This improvement was achieved by cascading stages that used a combination of resistive and active feedback. They were also able to reduce the noise figure by adjusting the gate widths of the devices in the first stage. The preamplifier produced had a gain of 22 dB with a 2.5 GHz bandwidth and a 5.6 dB noise figure at 1 GHz. An AGC amplifier that had a 45 dB gain with a 1.6 GHz bandwidth was also described. In 1985, the same authors presented three amplifiers³⁷ based on the 1983 design. A preamplifier with the same topology as before was described with the improved characteristics of 13 dB gain, 3 GHz bandwidth, and a 4.8 dB noise figure due to the increased gate width of the input transistor. A second preamplifier was designed by cascading two of the other preamps together with an inductor between the stages and active feedback in the second stage. This circuit had 22 dB gain, a 2.7 GHz bandwidth, and a 5.6 dB noise figure. The interstage inductor was chosen so as to locate the resonant peak just above the normal corner frequency of the amplifier. A

four-stage main amplifier was designed in the same fashion, yielding a 36 dB gain with a 1.5 GHz bandwidth.

Another amplifier based on Hornbuckle and Van Tuyl's design was submitted in 1986 by Cheng et al.,³⁸ but the device used in the fabrication of their amplifier was an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ junction field-effect transistor (JFET) since the characteristics of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ prevent the fabrication of MESFETs. The circuit is basically the same as the one shown in Figure 2-7 except that no feedback was used. The resulting amplifier exhibited a maximum voltage gain of 12 dB. While a measured bandwidth is not reported, an estimated value for the cutoff frequency of 7.8 GHz is given. The authors predict that a gain of 20 dB could be achieved with this circuit but cite problems with breakdown and the quality of the wafer as hindering the attainment of those results.

Williams and LeBlanc present a hybrid IC amplifier,³⁹ modelled after Hornbuckle and Van Tuyl's design, which addresses the problem of fashioning a non-integrating high-sensitivity receiver. The main difficulties the authors cite are that the previous gain elements had a voltage gain so low that, when used in conjunction with a large feedback resistor, the input capacitance of the receiver and the parasitic capacitance associated with the feedback resistors generally employed integrated the signal. One way they suggest to overcome this obstacle is to use a micro-FET

in the feedback path instead of the large resistor used by other designers. This feedback loop is positioned around three gain stages like the one shown in Figure 2-7, and a source follower serves as the output stage. Another approach employed to solve the parasitic capacitance problem is to use this capacitance as a part of the feedback element, which the authors do in a hybrid circuit with a feedback integrator. The gain and bandwidth characteristics of these amplifiers were not published with the designs since the authors were primarily concerned with high sensitivity, but they suggest that the circuits could be useful at speeds over 100 Mbit/s.

The common-source/source follower circuit was used in 1988 by Ohkawa⁴⁰ to build a preamplifier for an optical receiver. In designing his circuit, Ohkawa performed extensive analysis on the effect of stray capacitances as well as parasitic resistance associated with inductors on both circuit frequency response and noise characteristics. By including these elements in computer simulations, he demonstrates that stray capacitance tends to decrease bandwidth and increase noise, and that the effect of stray capacitance from inductor to ground is not as severe as that of stray capacitance in parallel with the inductor. He states that the effect of stray capacitance in this circuit (with approximately 7 GHz bandwidth) could be disregarded by prudent arrangement of the inductors on the monolithic chip, but

that in the future, as circuits attain bandwidths above 10 GHz, the effect of these stray capacitances must be taken into account. Ohkawa's design was composed of three cascaded gain stages: the first two like that of Figure 2-7 with a common-source as the output stage. He employed resistive loading at the drain of the active devices and used active loads for the source follower stages. The first stage has a shunt RL feedback network, and all of the MESFETs used in the gain stages had inductors connected to their gates for a peaking effect. The results of this configuration were a 6.5 GHz 3 dB down bandwidth, transimpedance gain of 57 dB, and an average input equivalent noise current density of 15.5 pA/rt Hz. Ohkawa states that inductor peaking caused a 20 percent increase in bandwidth according to his simulation. He does not explain how he calculated the transimpedance gain in decibels, but apparently his reported gain corresponds to a transimpedance of 700 Volts/Amp.

The latest modification to the Figure 2-7 circuit was made in 1990 by Kikuchi et al.⁴¹ in the following way: an RL network is used for the load of the common-source stage, an inductor couples this stage to the source follower stage, and an inductor is added to the drain and a capacitor added to the source of the source follower stage to create a large peaking effect. Also, resistive instead of active feedback is employed. The preamplifier fabricated is comprised of two of the circuits like that of Figure 2-7 and a common-

source output driver, and had a gain of 19 dB with a 3 dB bandwidth of 8.6 GHz and an average equivalent input noise current of 20.9 pA/rt Hz.

A slight variation on this popular design was introduced by Archambault et al. in 1987.⁴² A resistor is used as feedback around three inverter/source follower stages and an output buffer (source follower) to form a transimpedance amplifier, which the authors maintain has a higher cutoff frequency but lower midband gain than a conventional voltage amplifier-equalizer combination. The biggest difference between this design and the others is that this design implements simple resistive loads instead of active loads, which Archambault et al. attribute to resistors adding only Johnson (thermal) noise to the system while active loads also contribute noise characteristic of FETs. The result is an amplifier with at least 90 MHz bandwidth, a 40 dB signal-to-noise ratio and a dc transimpedance of 100 k Ω .

In 1987 Collieran and Abidi proposed a cascode circuit⁴³ in order to improve the gain while maintaining a high bandwidth, and in 1988 they compared the circuit with two transimpedance designs.⁴⁴ They point out that the two-stage configuration of a cascode (single stage depicted in Figure 2-8) offers advantages over both the one- and three-stage inverter combinations required inside a feedback loop to obtain negative feedback. The cascode design offers more gain-bandwidth product inside the loop than a single inver-

ter but less phase shift, with the associated stability problems, than three inverters within the loop would generate.

The cascode configuration also yielded a frequency response preferable to that of the common source configuration since the

authors were able to adjust the three poles un-

til they were roughly equal to each other, achieving a maximally flat response. However, since this scheme includes four FETs with their corresponding delays in each feedback loop, an R-C network was inserted at the source of the feedback transistor to control the peaking and guarantee the stability of the circuit. As a result, the design showed a 26 dB gain with a -3 dB bandwidth of 3.2 GHz. The noise figure was under 6 dB to 1 GHz and 8 dB at the maximum bandwidth.

In 1990, Imai et al. developed a slightly different cascode amplifier.⁴⁵ Their version features a cascode configuration with resistive instead of active feedback, and uses two source follower stages as the output drivers. The loads for these drivers, instead of being connected to the

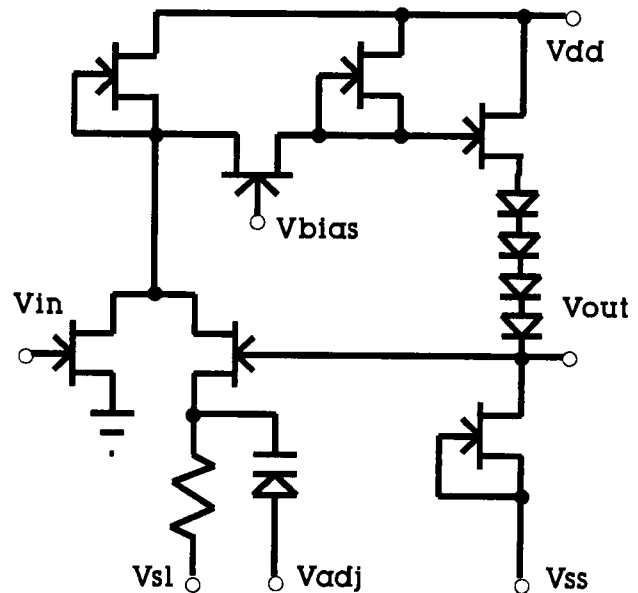


Figure 2-8. Cascode circuit.

negative power supply terminal as were those of a circuit they used for comparison, are connected to the drain of the input FET. This formation not only provides additional feedback for the circuit, but also increases the bandwidth, according to the authors. They devised this circuit to provide a noise figure sufficient for a front-end component, as they noted that previous work had not yielded a wideband direct-coupled amplifier with those noise characteristics. The results of their work were a 20 dB midband gain, 3 dB bandwidth of 10 GHz, and a noise figure less than 4.2 dB from 0.5 to 10 GHz.

A general purpose operational amplifier fabricated from GaAs MESFETs was introduced by Scheinberg⁴⁶ in 1987. He points out the similarity between GaAs MESFETs and silicon n-channel JFETs and suggested the possibility of borrowing JFET topologies for MESFET designs, but cites a lack of operational amplifiers constructed solely from either device. His design employs a differential input stage that is followed by a level shifter and a second gain stage. The level shifter is based on a MESFET current mirror, which the author claims yields a high power supply rejection ratio (and thus a wide range of possible power supply voltages, +/- 5-9 V) as well as temperature compensation for the circuit. The resulting amplifier has an open-loop voltage gain of 60 dB (at 100 kHz), input offset voltage of +/- 28 mV, and a gain-bandwidth product between 150 and 500 MHz,

depending on the compensation capacitor used. The biggest problem encountered was the presence of low frequency oscillations, which appeared at the inverting input of the amplifier, although the author claims they were due to the substrate material and not the circuit design.

Two other differential designs have been presented in addition to those discussed. Spargo and Abidi⁴⁷ published a design for a monolithic variable gain amplifier with a gain range of 9 dB per stage, for an overall gain up to 30 dB, a bandwidth of 1.2 GHz, and a noise figure of 19 dB from 100 MHz to 1 GHz. Their design uses over 45 MESFETs and over 25 diodes, one of the most complicated designs described. Larson et al.⁴⁸ developed a differential amplifier with a typical voltage gain of 22 dB and a measured bandwidth of 500 MHz with a 150 fF load, but they estimated that with a load of 50 fF, which they assert is more typical for an IC environment, the bandwidth would be at least 4 GHz. Their work is aimed at producing consistently low offset voltages, which is advantageous when manufacturing flash analog-to-digital converters.

One of the simplest receiver circuits reported was one realized by Lai et al.,⁴⁹ consisting of a MODFET (modulation-doped field-effect transistor) configured as a common-source with a source resistor. The novel feature of the circuit is the device used, a pseudomorphic $\text{In}_{0.60}\text{Ga}_{0.40}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ channel MODFET, which yielded results of a 15.3 GHz band-

width for a 33 Ω input impedance and 6.4 GHz for a 100 Ω input impedance.

Another uncomplicated circuit, presented by Petersen et al.,⁵⁰ consists of a common-source FET with series and shunt feedback and attained a voltage gain of 10 dB (within 1 dB) from 500 MHz to 2 GHz with a DC gain of 12 dB, and the 3 dB bandwidth is about 1.8 GHz. The circuit includes a terminal used to alter the gate bias, and when properly set a noise figure of 2 dB with a gain of 9 dB was obtained.

Ohkawa et al. also published a hybrid circuit⁵¹ involving only common-source stages. They commented that previous GaAs amplifiers had been designed without taking into account the junction capacitance of an optical detector, an important consideration if the amplifier is to be used in an optical receiver. They claim to have reduced parasitic inductance and stray capacitance in the design and fabrication of the chip which, in conjunction with their compensation for the detector junction capacitance, yielded an overall circuit operating at 5.6 Gbit/s. The amplifier alone has a bandwidth of 8.2 GHz with a gain of 15 dB. The amplifier consists of three resistively loaded common-source stages, the first and third with shunt feedback while the second stage has both shunt and series feedback. The series feedback contains resistance, a peaking capacitance, and a diode used to help compensate for the detector junction capacitance.

In 1987 Minasian developed an amplifier⁵² consisting of two common-source stages cascaded, and although his discussion focuses on adjusting the device gate width for optimum sensitivity, he reports that a 4 Gbit/s optical preamplifier has been obtained. The first gain stage contains shunt feedback, supplying the gain and helping to ensure the broad bandwidth of the circuit, while the second stage has series feedback, close to unity gain, and provides the 50 Ω output impedance. Minasian acknowledges that this topology has been used before⁵³ but the previous circuit's frequency response did not extend down to DC.

Kasper et al. also presented a hybrid two-stage cascaded common-source amplifier,⁵⁴ which had series feedback in the second stage and no feedback in the first stage. An inductor is included at the gate of the second stage to provide peaking in the frequency response. The bandwidth of the preamplifier alone was not reported, but when cascaded with an avalanche photodiode which has a gain-bandwidth product of 60 GHz and four wide-band commercial amplifiers with 3 dB bandwidths of 7 GHz along with an equalizer the overall frequency response extends to 6.9 GHz.

Barry Manz in 1986⁵⁵ described a commercially available circuit manufactured by ANADIGICS. The monolithic amplifier, model AD25001, was one of ANADIGICS' first two products and was designed for use in the field of fiber optics: operation to DC allows direct coupling to the input detec-

tor. The amplifier provides a 22.0 ± 0.3 dB gain to 1 GHz with a 3 dB bandwidth of 2.5 GHz. The article lists a noise figure of 5.5 dB but does not give the measurement frequency.

Arnaud et al.⁵⁶ designed an amplifier using a technology compatible on the same die with digital integrated circuits. It consists of essentially the same topology as the highly-utilized Figure 2-7 circuit, with a resistively loaded common-source/source follower combination using shunt feedback and a second source follower as an output driver. This circuit employs an inductor in series with the gate of the input FET to provide peaking in the frequency response, thus attaining 8.5 dB voltage gain with a 3 dB bandwidth of 8 GHz. The measured noise figure was around 7 dB in the range from 300 MHz to 8 GHz.

Silicon MOS Transistors

The fourth category of broadband amplifiers is that of amplifiers fabricated from silicon MOS devices. Fraser et al. presented an NMOS preamplifier in 1983 that had a voltage gain of 180 (45 dB) and a bandwidth of about 170 MHz.⁵⁷ The amplifier is made up of a cascode input stage followed by a source follower, two common-source stages, and another source follower as the output stage. An active feedback

loop is taken from the gate of the output stage, and is fed through a source follower and a common-gate stage back to the gate of the input stage. The noise performance achieved was less than they had anticipated, and the authors suggest that may be due to their incomplete knowledge of noise sources in short-channel MOSFETs.

Three amplifier circuits were introduced by Abidi et al. in 1984.⁵⁸ The first one incorporates three inverters with multiple feedback loops and achieves 22 dB gain with a 3 dB bandwidth of 920 MHz. The second has four pairs of transistors connected by shunt feedback and has an overall feedback loop as well as a voltage-controlled gain function. This amplifier has a gain which ranges from 0 to 35 dB corresponding to a bandwidth of 650 MHz. At the high end of the gain range peaking occurred, which the authors suggest is due to inductance in the bonding wires from the chip to ground. The third amplifier described has an inverter with shunt feedback as the input stage followed by two shunt-feedback pairs with voltage-controlled gains (like those in the second amplifier) with a source follower as the output stage. This configuration yielded a 720 MHz bandwidth, but the resulting gain was not listed. Abidi⁵⁹ later improved the characteristics of the third amplifier so that its frequency response extends to 1.26 GHz with a 20 dB gain. He also discusses briefly the role of silicon MOS technology, pointing out that with the technological advances in MOS

fabrication, it was becoming competitive in speed with Si BT and GaAs MESFET circuits and remaining superior in its "low cost and high yield manufacturability." He hints that silicon MOS technology would be appropriate for merging analog and digital circuitry on a single chip, a function needed, for example, in fiber optics signal regeneration at high data rates. MOS technology would be especially suitable for this application when all the circuitry needed for a regenerator could be integrated into just one or two chips.

Steininger and Swanson report a single chip containing an optical receiver sub-system⁶⁰ that operated at 50 Mb/s. The preamp for the system is fabricated as three cascaded common-source stages with active loads fed back through a resistively-biased MOSFET, yielding a 60 MHz bandwidth with the advantages of process and temperature insensitivity.

In 1987 Toh and Meyer introduced a circuit⁶¹ that uses submicron-channel MOS technology, usually employed for digital purposes, in a method designed to produce low-noise, impedance-matched circuits. Their design also consists of three common-source stages that implemented multiple feedback loops, including both active and resistive shunt-shunt feedback circuits. The results were a gain of over 16 dB with a 758 MHz bandwidth and an average noise figure of 6.7 dB from 10 MHz to 758 MHz.

In the same year Jindal et al. demonstrated a 50 dB gain with a 1 GHz bandwidth for an NMOS AGC amplifier,⁶² although the noise figure was 11 dB. Certain considerations such as "a number of device level improvements...to suppress several high-frequency noise mechanisms in the FET," and "substrate bias...to reduce parasitics and channel thermal noise" were made in the interest of improving performance. The topology is composed basically of cascode/source follower stages with shunt feedback cascaded in a variable-gain configuration. Three different input stages were modelled and compared on the basis of which one yielded the optimum noise performance.

CHAPTER 3

DESIGN CONSIDERATIONS - SELECTION OF THE WIDEBAND CONFIGURATION

Introduction

The purpose in developing this amplifier is to improve a measurement system, as discussed in Chapter 1. The amplifier was needed to increase system bandwidth without degrading the other system parameters. Therefore the circuit should have a gain of 100 and a bandwidth of 100 MHz or greater. Since the amplifier would be the second stage of the system, noise performance was important but would not have the strict requirements of the preamplifier. The amplifier was to have a characteristic impedance of $50\ \Omega$ at the input and the output, and should be able to drive at least ± 1 volt into a $50\ \Omega$ load. A gain nonlinearity of no more than 5% was required as well.

In this chapter the type of transistor to be used is selected from the types used in designs described in Chapter 2. Then a specific wideband configuration using the selected transistor type is chosen from those reviewed to use as a basis for the development of an amplifier that would meet the specifications outlined above.

Design Considerations

Monolithic vs. Discrete Design

Most of the designs reviewed in Chapter 2 are monolithic circuits, and their prominence suggests that monolithics offer better wideband performance than discrete or hybrid integrated circuits. However, since the processing cost for the first chip produced is very high for monolithic circuits, they are much more cost effective when a large number of circuits are fabricated. Since only one circuit was required for this application and the budget for the project was rather limited, a monolithic implementation was not an option. Another obstacle to using monolithic technology for this project was the long turn-around time required for IC fabrication, and the output drive specification may have dictated either the use of discrete transistors as output drivers or some other type of buffering.

There were, however, many aspects of monolithic circuits which made them very attractive for a circuit with the requirements listed above. Some devices used to design the amplifiers reviewed in Chapter 2 had cutoff frequencies over an order of magnitude greater than the best discrete devices found for this circuit, and a monolithic design should give the designer greater control over parameters that typically vary from device to device and over parasitic capacitances that frequently plague discrete designs. A monolithic

circuit would not have the propagation delays associated with the longer traces required for a discrete amplifier, and all of the components would be thermally coupled.

Transistor Selection

Several designers compared GaAs and Si devices. Pucel³¹ favors GaAs technology for monolithic circuits but believes SOS technology will play its major role in the frequency range below 2 GHz. Moustakas, Hullett, and Stephens note that "little noise penalty is incurred by using readily available bipolar junction transistors in place of GaAs MESFETs in the first stage of broadband optical preamplifiers."²⁹ When restricted to a discrete design, the variety and availability of silicon bipolar transistors as opposed to HBTs or GaAs MESFETs made them an attractive design device.

Although a wide variety of silicon MOS transistors was also available, there were certain advantages to using bipolar transistors. Many of these are summarized in a tutorial paper on MOS operational amplifier design by Gray and Meyer⁶³, including: "the maximum transistor open circuit voltage gain g_m/g_o is much lower for MOS transistors than for bipolar transistors", the open circuit voltage gain for MOS transistors varies with drain current at the current levels needed in high-speed amplifiers, "one mismatch component present in MOS devices which is not present in bipolar tran-

sistors is the mismatch in the threshold voltage itself... [which] results in a constant offset component which is bias current independent", "MOS devices display relatively high $1/f$ noise", and "the output voltage swing [of a CMOS complementary source follower class AB output buffer stage] is limited by the gate-source voltage of the output transistors."

Gray and Meyer note that bipolar transistors could be used for the output stages of MOS amplifiers to improve the voltage swing and decrease the output resistance. They also point out that MOS amplifiers generally have high slew rates compared to bipolar amplifiers.

With all of these factors taken into consideration silicon bipolar transistors were chosen for this application.

In order for the circuit to meet its specifications, which were outlined at the beginning of this chapter, the transistors used in its fabrication required very high cutoff frequencies (f_T 's) and low associated capacitances. Morii, Taniguchi, and Fukushima¹⁶ review several silicon bipolar transistors that met these qualifications. The transistors selected had SOT-23 (surface mount) packages. The absence of leads protruding from the board would help reduce crosstalk, parasitic capacitances and inductances. The NPN transistors selected for use in the amplifier under development included the 2SC3585 made by NEC¹⁶, and the MMBR901L and MMBR571L, both Motorola devices, while the

BSR12PH, made by Philips and equivalent to Motorola's MPS3640, was selected as the PNP transistor. A major drawback to the use of these transistors was their low breakdown voltages. V_{CE0} , the collector-emitter breakdown voltage, was only 10 Volts for the 2SC3585 and the MMBR571L, 12 Volts for the BSR12PH, and 15 Volts for the MMBR901L. This parameter placed limits on the range of power supply voltages which would ensure safe operation of the circuit. The voltage selected was ± 5.5 Volts, which virtually assured that no dangerous voltage could appear across the junctions of these transistors, but at the same time placed limits on the dynamic range of the amplifier.

Selection of the Wideband Configuration

After evaluating the merits of the various transistor types in the previous section it seemed that the best choice for a configuration would be one of the silicon bipolar amplifiers.

In selecting a Si BT configuration from the ones reviewed, high priority was given to the minimization of the propagation delay around the feedback loop. Many of the circuits reviewed were monolithic circuits, so the length of the signal path around their feedback loops might be only a few microns. However, in a discrete circuit the length of the signal path can quickly approach values on the order of one wavelength at frequencies greater than 100 MHz. Thus

propagation delay through the feedback loop becomes a serious consideration in a discrete amplifier.

Another criterion used in the selection process was the voltage gain. For the amplifier to have an overall voltage gain of 100, each stage must have a significant gain (approaching 10, or 20 dB). Optimum low-noise design dictates that most of the gain should be placed in the first stage of the amplifier, so a common-emitter configuration is preferred for the input transistor.

The two four-stage designs,^{26,27} besides having three or four active devices and the associated propagation delays in their feedback loops, had common-collector input stages and thus were unsuitable for this application. Other designs^{17,19} had so little gain that the amplifier would need a minimum of three stages cascaded together to produce the required gain.

The remaining designs were all based on a common-emitter input driving a common-collector stage. Thus the number of active devices in the feedback loop and the output driver configuration were used to evaluate these designs.

Both of Meyer and Blauschild's designs^{21,23} have at least three active devices inside a feedback loop and use a common-emitter stage as an output driver, which has a higher output resistance and greater signal distortion than an emitter follower.⁶⁴ Ishihara and Konaka²⁵ also use a common-emitter output driver, as do Chan and Meyer.²⁴

The design by Ohara et al.²⁰ was selected as it has only a common-emitter and common-collector stage inside the feedback loop, a common-emitter input configuration, and an emitter follower as the output driver (Figure 3-1). This configuration thus has all of the characteristics outlined previously. The high gain of the common-emitter input stage is preferred for low-noise work and generates sufficient gain (23 dB) with only two gain stages inside the feedback loop.

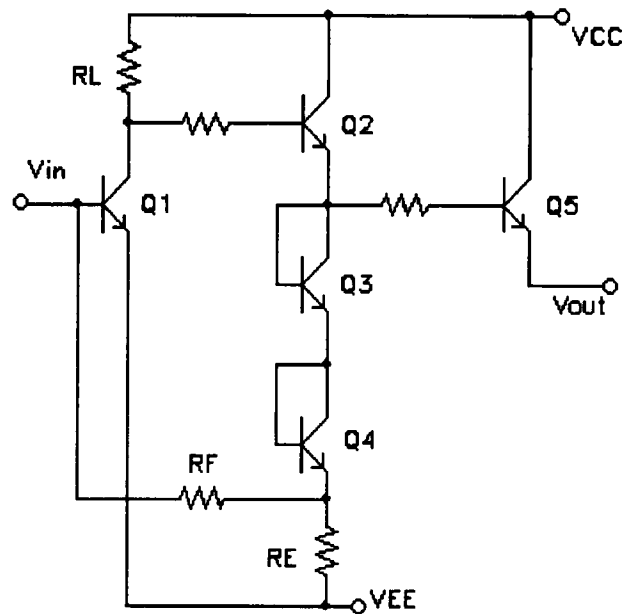


Figure 3-1. Wideband configuration presented by Ohara et al.

These two stages generate only minimal propagation delays in the feedback loop, promoting a wideband response. The emitter follower provides an output stage with low distortion and low output resistance. Figure 3-1 shows that the output driver is not in the feedback loop, which means its linearity is not stabilized by the feedback. The advantage in this configuration is that the number of active devices in the feedback loop is kept to a minimum. Analysis is carried

out in Chapter 4 to ensure that significant gain nonlinearities do not result from this configuration.

Another consideration was the number of stages to use in obtaining the gain of 100 from the circuit. An important factor in this analysis is the bandwidth required from each stage to give a 100 MHz bandwidth for the whole amplifier. Fitchen⁶⁵ gives the formula for this computation as

$$f = f_h * (2^{1/n} - 1)^{1/2} , \quad (3.1)$$

where f is the overall amplifier bandwidth, f_h is the bandwidth of a single stage, and n is the number of stages in cascade. Algebraic manipulation gives

$$f_h = f * (2^{1/n} - 1)^{-1/2} \quad (3.2)$$

for the bandwidth of a single stage.

Instead of attempting to include a 10 GHz gain-bandwidth product in a one-stage amplifier a cascade design of two stages, each like the one by Ohara et al., was selected. Each was to have a gain of 10 and would require a bandwidth of approximately 160 MHz. This 1.6 GHz gain-bandwidth product for one stage would be much more manageable than a 10 GHz figure, although the two stages would need to be well isolated from each other to avoid high-frequency pickup and crosstalk between stages. Another disadvantage to using a

single stage was that if feedback were used to obtain a gain of 100 the open loop gain would have to be much larger than 100, increasing the complexity of the single stage and the difficulty in preventing oscillations, as more gain blocks would be necessary within the feedback loop.

Another possibility was to divide the circuit into three stages, each with a gain of approximately 5 and a bandwidth of 200 MHz. This configuration still required a gain-bandwidth product of 1 GHz from each stage, which did not seem much less demanding than the 1.6 GHz needed from a two-stage design while dictating another stage, or about fifty percent more circuitry and board space. Comparing the one-, two-, and three-stage options, the 10 GHz gain-bandwidth product required for a one-stage design seemed too high. The two- and three-stage designs needed roughly the same gain-bandwidth per stage but the three-stage design required fifty percent more circuitry and board space. Thus a two-stage design was selected.

Modifications to the Selected Configuration

In implementing the Ohara circuit for the purpose described above, some changes were incorporated. When driving a negative output pulse the output transistor would be turning off, affording very little of the drive current necessary to drive a 50 Ω load. To remedy this situation, a class AB output stage was used to give improved drive for

these negative pulses. When utilizing this type of output stage in a discrete design, inability to thermally couple the output drivers with the diode-connected transistors used to bias them could result in thermal runaway. Since the drivers were biased only by the voltage across their base-emitter junctions, heating due to current flow could shift their characteristic current/ voltage curves, increasing the collector current corresponding to the given voltage across their junctions. To prevent this effect from occurring, a small resistor was added in series with the emitter of each of the output devices so that any increase in current through these transistors would cause a voltage increase across the resistors, decreasing the voltage across the transistor junctions and checking the thermal runaway.

With the large gain required, biasing became a problem as any small DC shift at the input would cause large output swings and alter the bias point of the circuit. An RC network was added in series with the emitter of the input transistor (Figure 3-2) to decrease the DC gain (increasing the DC stability) and help set the bias point of the circuit. When the circuit was fabri-

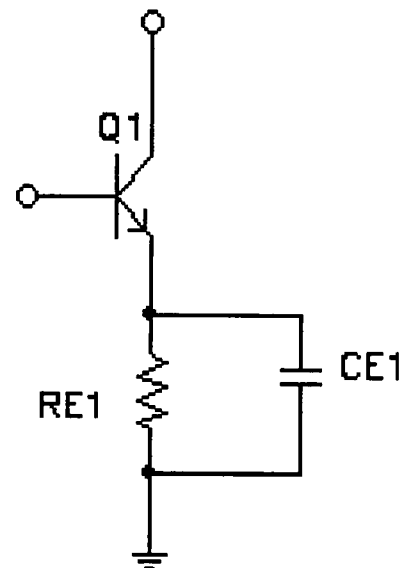


Figure 3-2. RC network in series with input transistor.

cated initially, any difference in the output DC level of the first stage would cause current to flow through R_{S2} (Figure 3-3) and change the bias levels of the second stage. To prevent this effect a capacitor, C_{S2} , was added between the two stages, AC coupling

them and preventing any DC current from flowing through R_{S2} and upsetting the bias levels.

To increase the dynamic range at the output of the circuit the placement of the second-stage feedback resistor was changed (Figure 3-3). The dynamic range of the second stage was limited principally by the dynamic range at the collector of the input transistor, Q10. Decreasing the DC level of this transistor's base allowed its collector to swing farther in the negative direction before its response became nonlinear. The circuit was biased so that the current through the feedback resistors was negligible, so the feedback resistor should be connected to a point with as low a DC level as possible without compromising the loop trans-

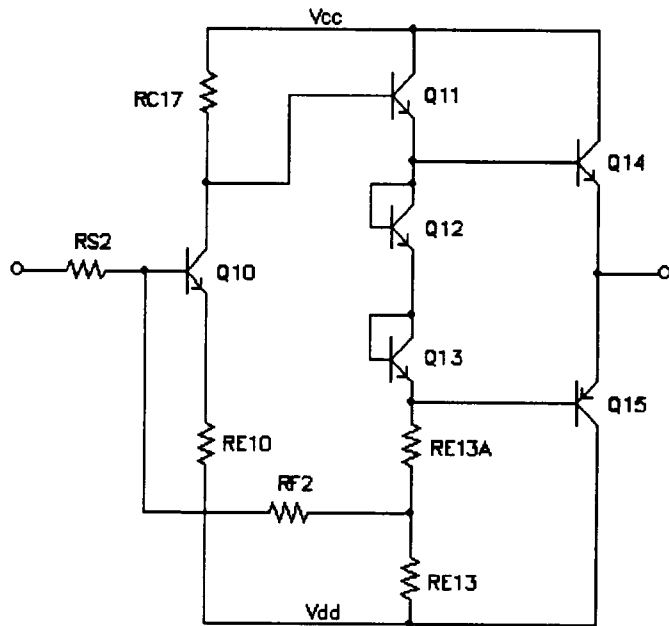


Figure 3-3. Simplified second stage schematic.

mission. Moving the connection point below diodes Q12 and Q13 decreased the DC level at the second stage input by twice the voltage drop across a diode, about 1.5 Volts.

In order to DC couple the two stages, the DC level at the output of the first stage had to be the same as that at the input of the second stage. Since one side of the first-stage feedback resistor was biased at DC ground (if the input voltage had no DC offset), the other side of the resistor was used to bias the emitter of Q2 at ground. Q3, a transistor connected as a diode (Figure 3-4), was included so that the output of the first stage would be biased below ground by twice the voltage across a diode.

The inclusion of resistor R_{E13A} with R_{E13} (Figure 3-3) permitted greater flexibility in setting the second-stage output DC level and increasing overall dynamic range. Increasing the ratio of R_{E13A} to R_{E13} increased the output DC level and boosted the dynamic range but decreased the effectiveness of the feedback in the circuit, so values were

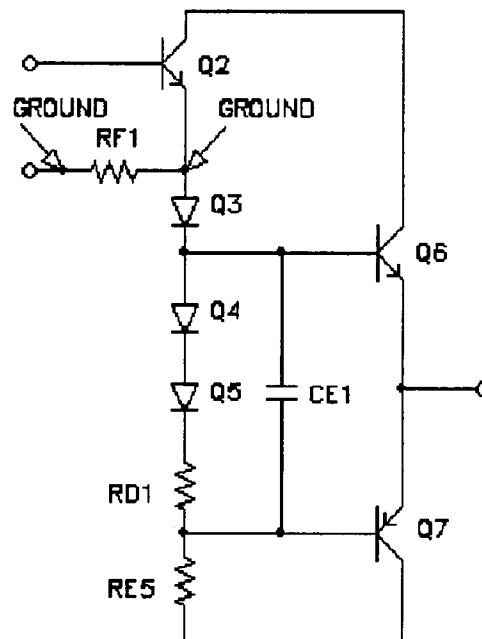


Figure 3-4. Position of diode Q3 for biasing.

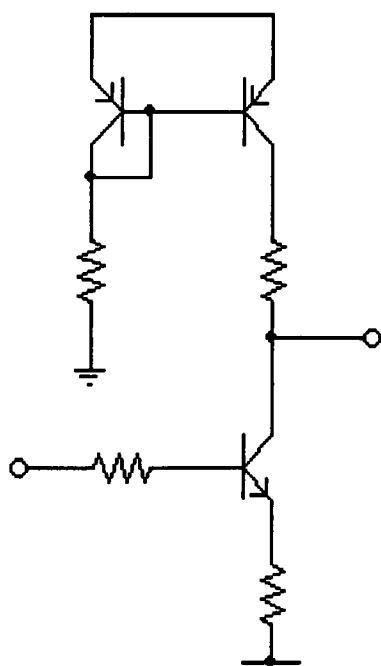


Figure 3-5. Current source configuration for both stages.

used which compromised between these two effects.

A current source (Figure 3-5) was added to the collector of the input transistor in both the first and second stages which increased the open loop gain of the circuit and aided in its biasing by setting the collector currents for the input transistors. The current source selected was a current mirror designed with two PNP transistors, which provided a relatively stable current with a minimum number of transistors.

The resistor was left in series with the current source which slightly increased the impedance in the collector of the common-emitter stage. Since any capacitance at the collector of the input transistor would reduce the bandwidth of the circuit, the resistor in series with the current source helped to isolate the output capacitance of the current source from the collector of the input transistor. The resistor remained small enough so as not to compromise the dynamic range of the circuit, especially in the second stage, where the dynamic range requirements were stricter.

A resistor was added in series with the input of each stage to help set the closed loop voltage gain (i.e. R_{F2}/R_{S2}

in Figure 3-3). To avoid termination problems associated with the input impedance becoming large at very low or very high frequencies a resistor was added in parallel to the input of the circuit as well.

Finally, a capacitor was added in parallel with the diodes and resistor used to bias the output drivers in each stage (Figure 3-4). These elements, if unbypassed, would cause differences in gain for positive and negative pulses. The diodes themselves are nonlinear devices and would detract from the linearity of the circuit.

Modifications that compromised the low-frequency response of the amplifier were described earlier in this chapter. Since the amplifier was originally intended to be DC-coupled the effect of these modifications should be considered.

One reason that AC coupling was not detrimental to the performance of the amplifier was that the system for which this amplifier was developed² already had two high-pass filters with corner frequencies at approximately 30 kHz. Component values were selected so that the low frequency corners caused by the R_{E1}/C_{E1} , R_{E10}/C_{E10} , and R_{S2}/C_{S2} combinations were all at 100 Hz. Therefore the amplifier would not degrade the system's low-frequency response.

CHAPTER 4

AMPLIFIER ANALYSIS

The analysis performed for this circuit has been subdivided into several sections. First, the DC analysis, or biasing, of the circuit was carried out to define the operating point of the circuit. Next, the values determined in the DC analysis were utilized in an AC analysis, calculating the frequency response and stability of the amplifier, and the gains calculated in this analysis were then used to characterize the noise in the system. A model for the circuit was developed (using PSpice) and evaluated, and the results from PSpice were compared to the calculated results. Finally, a printed circuit board layout was designed.

Biasing Considerations

First Stage

The first stage of the circuit, depicted in Figure 4-1, was relatively easy to bias. The dynamic range required at the output of the first stage was merely 0.2 Volts peak-to-peak because the second stage had a gain of 5 when driving a 50 Ω load, and since the two stages were joined by a cou-



pling capacitor there was no specific DC level required at the output. The calculated DC output level of the first stage was actually -1.54 V.

A relatively low value, 4.5 mA, was selected for the collector current in Q1 to minimize the shot noise in the transistor.

The dynamic range was limited in the positive direction because large positive voltages at the collector of Q1 would cause the collector of Q9 to be driven above its base, moving the transistor outside the region of linear operation. Specifically,

$$V_{C1max} = V_{B9} - I_{C9} * R_{C9} = 4.51 - (0.0045 * 604) = 1.79 \text{ V.} \quad (4.1)$$

This value assured that the collector of Q9 would never be driven higher than its base.

The maximum positive voltage attainable by the output of the first stage was

$$V_{O1max} = V_{C1max} - V_{be2} - V_{be3} - V_{be6} - V_{RE6} = -0.51 \text{ V.} \quad (4.2)$$

The limit on the dynamic range in the negative direction could have been determined in one of two ways. The ratio of R_{F1} to R_{E5} set a limit such that if all of the collector cur-

rent for Q3 was coming from R_{F1} (Q2 turned off), the voltage across R_{E5} would be

$$V_{RE5min} = \frac{(-V_{EE1} - 3*V_{be3}) * R_{E5}}{R_{F1} + R_{D1} + R_{E5}} \quad (4.3)$$

$$= \frac{(5.3 - 2.25) * 560}{536 + 12 + 560} = 1.54 \text{ V.}$$

The minimum output voltage, if this were the limiting factor, would be

$$V = V_{EE1} + V_{RE5min} + V_{be7} + V_{RE7} \quad (4.4)$$

$$= -5.3 + 1.54 + 0.75 + 0.036 = -2.97 \text{ V.}$$

The other factor that limited the voltage drive in the negative direction was how low the collector of Q1 could go before Q1 went into a region of nonlinear operation. If the collector was not allowed to go below the base voltage, it would be at 0 Volts at the maximum negative drive and the output voltage would be

$$V = V_{C1} - V_{be2} - V_{be3} - V_{be6} - V_{RE6} \quad (4.5)$$

$$= 0 - 0.75 - 0.75 - 0.75 - 0.036 = -2.29 \text{ V.}$$

Thus the collector of Q1 limits V_{O1min} to -2.29 Volts.

The dynamic range of the first stage was therefore 1.78 Volts, the difference between the values found in Equations 4.2 and 4.5, but was limited to 1.50 Volts peak-to-peak for a symmetrical sine wave since it could not drive as far below its -1.54 Volt DC level as it could drive above it.

The collector currents for the transistors in the first stage are listed in Table 4-1.

Table 4-1. First-stage transistor bias currents.

Transistor	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9
Current (mA)	4.5	6	6	6	6	9	9	4.5	4.5

Second Stage

The main differences in the biasing of the first and second stages resulted from the dynamic range requirements of the second stage (shown in Figure 4-2), namely the ability to drive a 2 Volt peak-to-peak signal into a 50 Ω load.

The signals entering the second stage were ten times as large as those in the first stage, so more collector current was required in Q10 than in Q1 to provide enough high-frequency voltage swing.

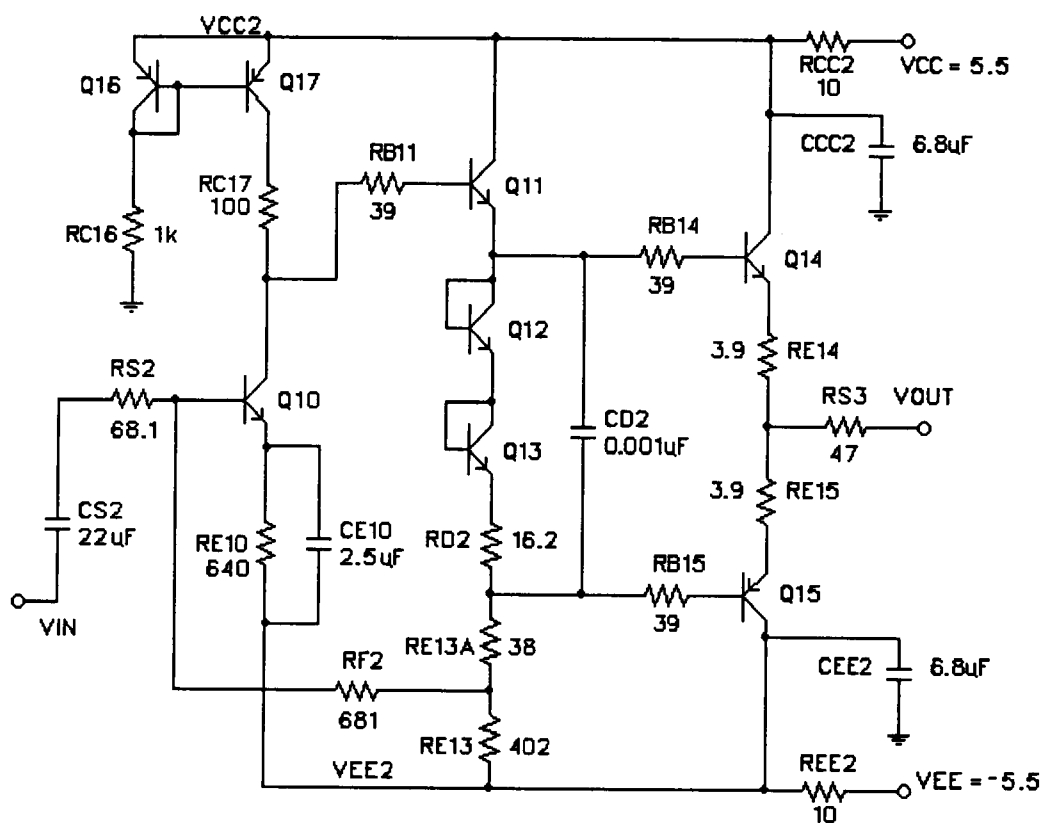


Figure 4-2. Schematic diagram for second stage.

Since the output was not AC coupled it was necessary to design the second stage so that the output DC voltage was 0 Volts.

The dynamic range computations for the second stage were analogous to those used for the first stage. In the positive direction the limit was determined by the maximum voltage achievable in linear operation by the collector of Q17 (see Equation 4.1),

$$V_{C10max} = V_{B17} - I_{C17} * R_{C17} = 4.36 - (0.0075) * (100) = 3.61 \text{ V.} \quad (4.6)$$

Hence the maximum limit was (see Equation 4.2)

$$V_{O2max} = 2.02 \text{ V.} \quad (4.7)$$

For a negative output pulse, the voltage across R_{E13} could have been no less than

$$\begin{aligned} V_{RE13min} &= \frac{(V_{B10} - V_{EE2}) * R_{E13}}{R_{F2} + R_{E13}} = \frac{[-1.23 - (-5.10)] * 402}{681 + 402} \quad (4.8) \\ &= 1.44 \text{ V,} \end{aligned}$$

which limits the negative swing of the output to

$$V = V_{EE2} + V_{RE13min} + V_{RE13Amin} + V_{be15} + V_{RE15} = -2.82 \text{ V.} \quad (4.9)$$

Under this condition all of the current flowing through R_{E13} would come from R_{F2} , not R_{E13A} , so $V_{RE13Amin}$ was 0 Volts. Alternately, the maximum negative swing allowed at the collector of Q10 would limit the output to (see Equation 4.4)

$$V = V_{C10} - V_{be11} - V_{be14} - V_{RE14} = -2.82 \text{ V}, \quad (4.10)$$

which was the limiting factor since this voltage matched the one found in Equation 4.9. The dynamic range at the output of the second stage is therefore 4.84 Volts, but the lack of positive range limited its ability to reproduce a sine wave to 4.04 Volts peak-to-peak, which translated to 2.0 Volts peak-to-peak when driving a 50 Ω load.

The transistor bias currents for the second stage are listed in Table 4-2.

AC Analysis

First Stage

The first step in developing a mathematical model for the circuit was calculating the loop gain. This calculation was accomplished by opening the loop at the base of Q1 and initially neglecting the low-frequency corner due to the combination of R_{E1} and C_{E1} . The open-loop impedance, Z_{iol} , looking into the base of Q1 was found to be (excluding r_{b1} ,

Table 4-2. Second-stage transistor bias currents.

Transistor	Current
Q10	7.5 mA
Q11	8 mA
Q12	8 mA
Q13	8 mA
Q14	16 mA
Q15	16 mA
Q16	7.5 mA
Q17	7.5 mA

the ohmic resistance in the base)

$$Z_{io1} = \frac{\beta_1 * r_{e1}}{1 + s * \beta_1 * r_{e1} * C_{M1}}, \text{ where} \quad (4.11)$$

$$C_{M1} = C_{be1} + C_{be1} * \frac{Z_{C1}}{r_{e1}}, \quad (4.12)$$

which represented the total capacitance across the base-emitter junction due to the Miller capacitance combined with the base-emitter capacitance. Z_{C1} was the impedance seen by the collector of Q1, represented as

$$Z_{C1} = (R_{C9} + r_{o9}) \parallel (R_{B2} + r_{b2} + Z_{io2}), \quad (4.13)$$

and s was a variable that modelled the dependence of this impedance on frequency. s was defined as

$$s = j * 2 * \pi * f, \quad (4.14)$$

where j was an imaginary number defined as the square root of -1 and f was the signal frequency expressed in Hertz. The variable s will be used throughout the remainder of these calculations as a convenient way to express frequency dependence.

The output impedance of the current source transistor Q9 was modeled as a resistance, r_{o9} , found by dividing the Early voltage of the transistor by the collector current, which gives $4.2 \text{ k}\Omega$.

Z_{io2} represented the open-loop impedance looking into the base of Q2 and was determined to be

$$Z_{io2} = \frac{\beta_2 * r_{e2}}{1 + s * \beta_2 * r_{e2} * c_{be2}} + \beta_2 * Z_{E2}, \text{ where} \quad (4.15)$$

$$Z_{E2} = [3 * r_{e3} + R_{D1} + (R_{E5} \parallel Z_{i7})] \parallel Z_{i6}. \quad (4.16)$$

Z_{E2} represented the impedance at the emitter of Q2. Z_{i6} and Z_{i7} stood for the impedances looking into the bases of Q6 and Q7, respectively,

$$Z_{i6} = r_{b6} + \frac{\beta_6 * (r_{e6} + R_{E6} + R_{S2})}{1 + s * (R_{B6} + r_{b6} + 2 * r_{e3} + R_{D1} + R_{E5}) * C_{bc6}} \quad (4.17)$$

and

$$Z_{i7} = r_{b7} + \frac{\beta_7 * (r_{e7} + R_{E7} + R_{S2})}{1 + s * (R_{B7} + r_{b7} + R_{E5}) * C_{bc7}} \quad (4.18)$$

Their values were large enough that R_{B6} and R_{B7} could be ignored. The poles due to the time constant products $\beta_6 * r_{e6} * C_{bc6}$ and $\beta_7 * r_{e7} * C_{bc7}$ were omitted from these expressions since their frequencies were above 800 MHz. R_{C6} and R_{C7} were left out of the resistor sums in the denominators of these high-frequency poles since they were bypassed at low frequencies by C_{C6} and C_{C7} , respectively.

The open-loop gain from the input to the base of Q1 could then be calculated as (r_{b1} was insignificant compared to Z_{i01})

$$A_1 = \frac{Z_{i01} \parallel (R_{F1} + Z_{E2})}{R_{S1} + Z_{i01} \parallel (R_{F1} + Z_{E2})}, \quad (4.19)$$

the gain from the base to the collector of Q1 was

$$A_2 = \frac{Z_{C1}}{r_{e1}}, \quad (4.20)$$

and the gain from the collector of Q1 to the emitter of Q2 was

$$A_3 = \frac{\beta_2 * Z_{E2}}{(R_{B2} + r_{b2} + Z_{i02}) * (1 + s/\omega_{p2})} , \text{ where} \quad (4.21)$$

$$\omega_{p2} = \frac{1}{C_{bc2} + \frac{C_{bc2}}{1 + \frac{Z_{E2}}{r_{e2}}}} * \frac{1}{\frac{(V_{A1} + R_{B2} + r_{b2})}{I_{C1}} || \beta_2 * (r_{e2} + Z_{E2})} \quad (4.22)$$

was the pole frequency associated with the emitter follower and due primarily to the base-collector capacitance. A_3 had a value of 0.981 and was thus ignored in further calculations (it only changed the other values by two percent).

The gain calculation back to the base of Q1 from the Q2 emitter yielded (R_{GEN} , the output resistance of the generator, was assumed to be 50 Ω)

$$A_4 = \frac{(R_{GEN} + R_{S1}) || Z_{i01}}{R_{F1} + [(R_{GEN} + R_{S1}) || Z_{i01}]} , \quad (4.23)$$

so the loop gain was found to be

$$T_1 = A_2 * A_4 \quad (4.24)$$

$$= \frac{Z_{C1} * [(R_{GEN} + R_{S1}) || Z_{i01}]}{r_{e1} * \{R_{F1} + [(R_{GEN} + R_{S1}) || Z_{i01}]\}}$$

with a midband value of 58.6, and is shown in Figure 4-3.

The gain of the output stage could be calculated in more than one way. To determine whether or not leaving the output stage out of the feedback loop caused any significant gain nonlinearities, the large-signal gains were calculated as a worst case gain. For a positive input pulse the characteristics of the output PNP transistor would determine the response and for a negative input pulse the NPN transistor would determine the response. The small-signal response is shown later for comparison.

The open-loop large-signal gain from the emitter of Q2 to the output of the first stage (using R_{S2} as the load resistor) was calculated as follows. The gain for a negative input pulse was divided into two components, the gain to the emitter of Q3,

$$A_{5na} = \frac{[2*r_{e3} + R_{D1} + (R_{E5} || Z_{i7})] || Z_{i6}}{r_{e3} + [2*r_{e3} + R_{D1} + (R_{E5} || Z_{i7})] || Z_{i6}}, \quad (4.25)$$

and the gain from the emitter of Q3 to the output,

$$A_{5nb} = \frac{\beta_6 * R_{S2}}{R_{B6} + r_{b6} + \beta_6 * (r_{e6} + R_{E6} + R_{S2})} \frac{1}{1+s/\omega_{p6}}, \quad (4.26)$$

where

First Stage Loop Transmission

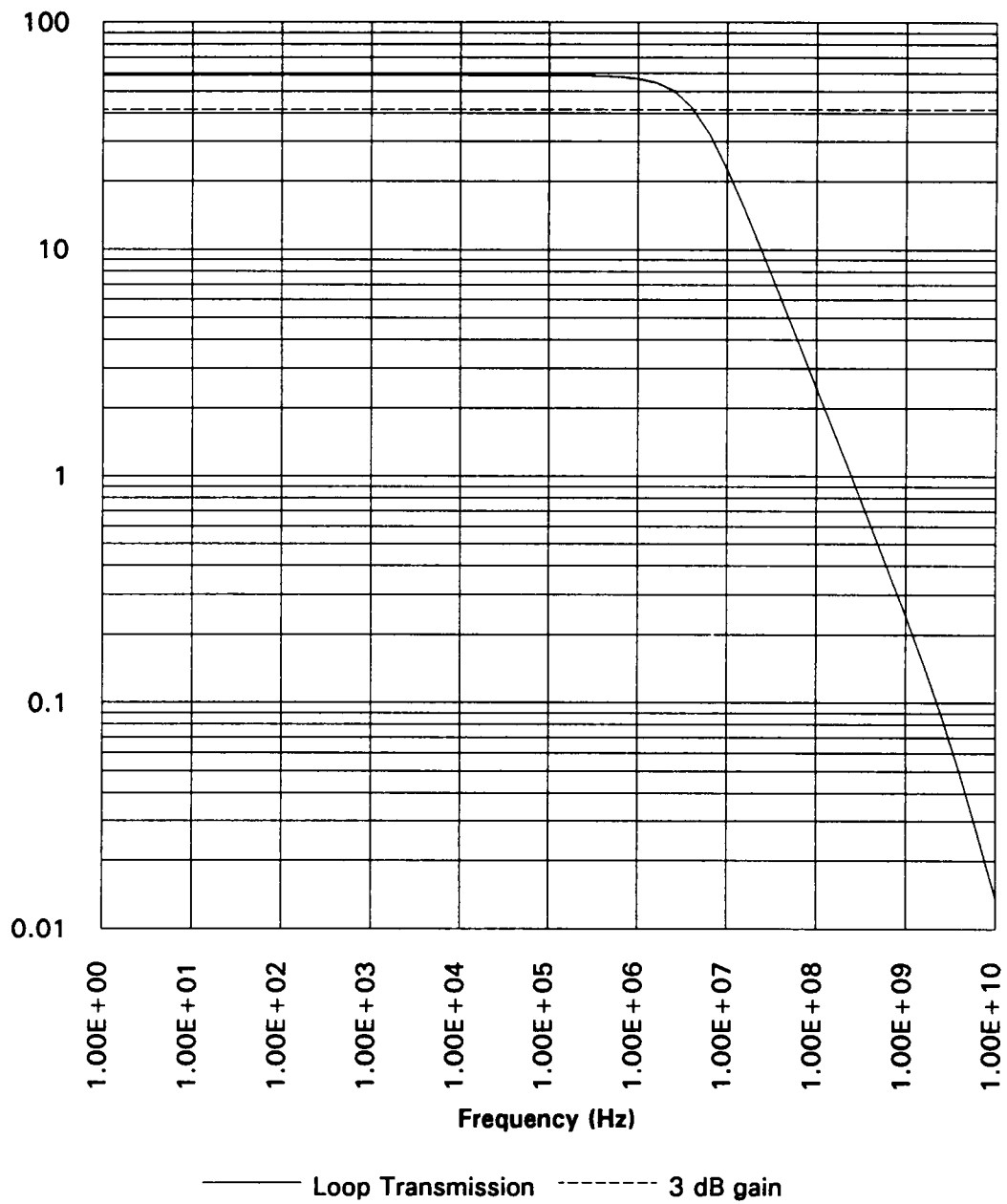


Figure 4-3. First stage loop transmission.

$$\omega_{p6} = \frac{1}{C_{bc6}} * \frac{1}{(r_{b6} + R_{B6} + Z_{D1} + R_{E5}) \parallel \beta_6 * (r_{e6} + R_{E6} + R_{S2})} . \quad (4.27)$$

A_{5na} had a value of 0.991 at low frequency, so it was insignificant. A_{5nb} was approximately 0.909 so it was included in the final results, and ω_{p6} corresponds to a pole at approximately 260 MHz due principally to the interaction of R_{E5} and C_{bc6} .

These terms combined to yield

$$A_{5N} = \frac{R_{S2}}{(r_{e6} + R_{E6} + R_{S2}) * (1 + s/\omega_{p6})} , \quad (4.28)$$

since R_{B6} and r_{b6} were much smaller than the other quantities in Equation 4.26.

Similarly, for a positive input pulse the large-signal gain was divided into the gain to resistor R_{E5} ,

$$A_{5pa} = \frac{A_{5na} * (R_{E5} \parallel Z_{i7})}{2 * r_{e3} + R_{D1} + (R_{E5} \parallel Z_{i7})} , \quad (4.29)$$

and the gain from R_{E5} to the output,

$$A_{5pb} = \frac{\beta_7 * R_{S2}}{R_{B7} + r_{b7} + \beta_7 * (r_{e7} + R_{E7} + R_{S2})} \frac{1}{(1 + s/\omega_{p7})} , \quad (4.30)$$

where

$$\omega_{p7} = \frac{1}{C_{bc7}} * \frac{1}{(r_{b7} + R_{B7} + R_{E5}) \parallel \beta_7 * (r_{e7} + R_{E7} + R_{S2})} . \quad (4.31)$$

A_{5pa} had a value of 0.95 and so it was included in the calculation, although including A_{5na} in the numerator affected its value by less than 1 percent so A_{5na} was omitted from this equation. A_{5pb} had a low-frequency value of 0.909 with ω_{p7} corresponding to a frequency of 170 MHz.

Equations 4.29 through 4.31 were incorporated into one formula, yielding

$$A_{5p} = \frac{0.95 * R_{S2}}{(r_{e7} + R_{E7} + R_{S2}) * (1 + s/\omega_{p7})} \quad (4.32)$$

since R_{B7} and r_{b7} were much smaller than the other quantities in Equation 4.30.

These expressions were then combined to generate an expression for the closed-loop gain from the input to the output of the first stage. For a negative input pulse,

$$A_{v1n} = \frac{A_1 * A_2 * A_{5N}}{1 + T_1} \quad (4.33)$$

$$= \frac{[Z_{io1} \parallel (R_{F1} + Z_{E2})] * Z_{C1} * R_{S2}}{(1+T_1) [R_{S1} + Z_{io1} \parallel (R_{F1} + Z_{E2})] (r_{e1}) (r_{e6} + R_{E6} + R_{S2}) (1+s/\omega_{p6})} ,$$

and for a positive input pulse,

$$A_{c1p} = \frac{A_1 * A_2 * A_{5p}}{1 + T_1} \quad (4.34)$$

$$= \frac{[Z_{io1} || (R_{F1} + Z_{E2})] * Z_{C1} * R_{S2}}{(1+T_1) [R_{S1} + Z_{io1} || (R_{F1} + Z_{E2})] (r_{e1}) (r_{e7} + R_{E7} + R_{S2}) (1+s/\omega_{p7})} .$$

These gains are depicted graphically (without making the simplifying assumptions mentioned earlier) in Figure 4-4.

Obviously, any difference in the gains A_{5N} and A_{5p} would result in nonlinearities. To minimize these nonlinearities, r_{e3} and R_{D1} were kept small compared to R_{E5} and the capacitor C_{D1} was included to short circuit these elements above a frequency determined by the interaction of C_{D1} with R_{D1} , r_{e4} , and r_{e5} . It was apparent from Equation 3.48 that A_{5na} and A_{5pa} would be identical above this frequency even though their magnitudes were small enough that they affected the overall transfer function by less than two percent. The magnitudes of A_{5nb} and A_{5pb} were well matched since β_6 and β_7 were approximately equal, but the bandwidth of A_{5pb} was less than that of A_{5nb} since c_{bc7} was greater than c_{bc6} .

The small-signal gain of the output stage was calculated as

$$A_{5ss} = \frac{R_{S2}}{R_{S2} + \left(\frac{R_{B6} + r_{b6}}{\beta_6} + \frac{r_{e6}}{1+s*r_{e6}*c_{bc6}} + R_{E6} \right) || \left(\frac{R_{B7} + r_{b7}}{\beta_7} + \frac{r_{e7}}{1+s*r_{e7}*c_{bc7}} + R_{E7} \right)} \quad (4.35)$$

First Stage Closed-Loop Gains

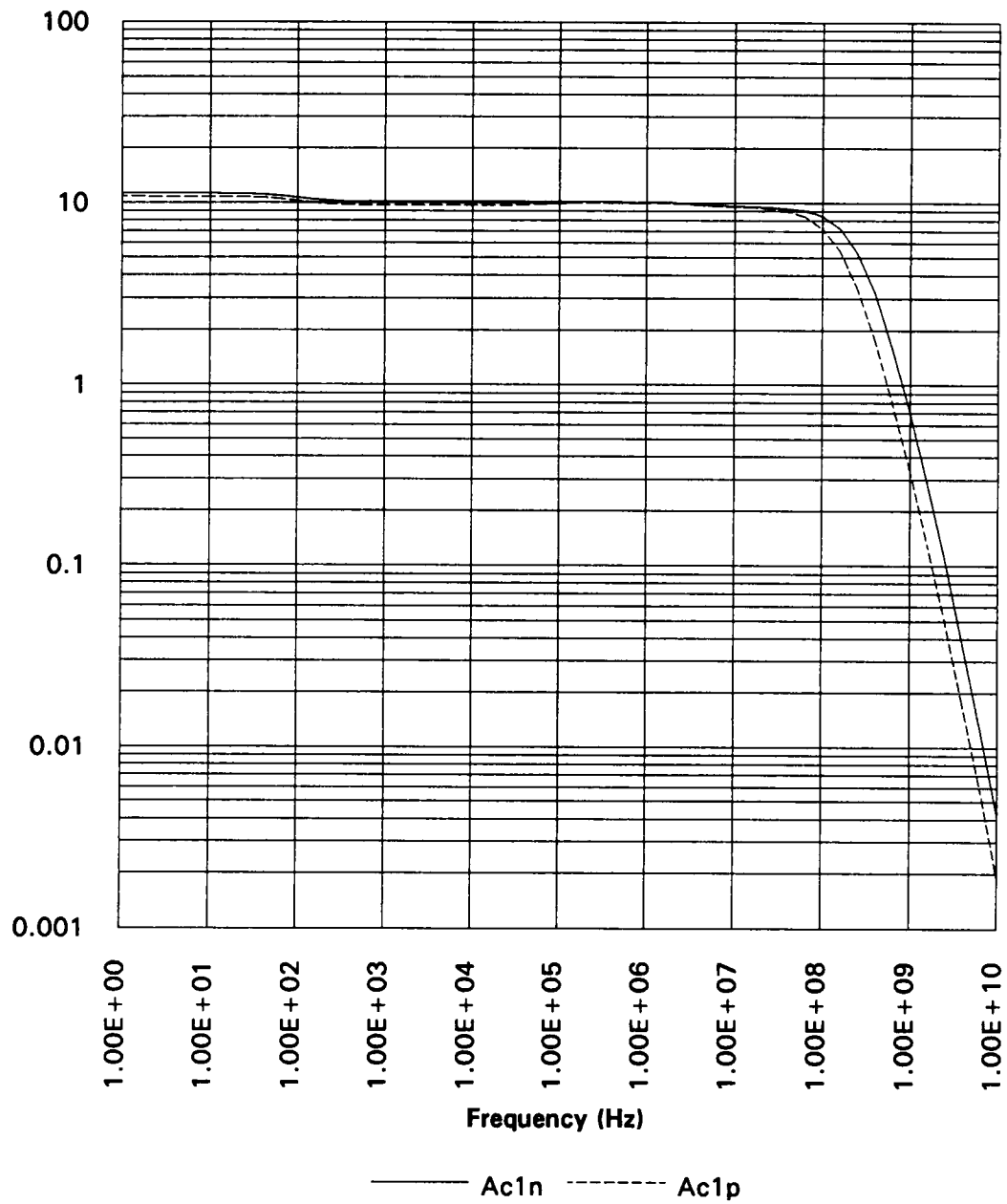


Figure 4-4. First stage closed-loop gains.

and had a pole at a frequency

$$\omega_{5ss} = R_{E5} * (C_{c6} + C_{c7}) . \quad (4.36)$$

When this expression (which had a midband gain of 0.947) was used in place of A_{5N} in Equation 4.33, the resulting function had a bandwidth of 220 MHz.

The input impedance of the amplifier, shown in Figure 4-5, was established as

$$Z_{ic} = (R_{S1} + \frac{r_{b1} + Z_{io1}}{1 + T_1}) || R_1 . \quad (4.37)$$

Second Stage

Due to the different configuration of the second stage the calculations had a few deviations but overall the equations characterizing the second stage were similar to their first stage counterparts. Except for changes in the subscripts, the first few equations were identical to those of the first stage (Equations 4.11-4.13) and are listed below.

$$Z_{io10} = \frac{\beta_{10} * r_{e10}}{1 + s * \beta_{10} * r_{e10} * C_{M10}} , \quad (4.38)$$

$$C_{M10} = C_{be10} + C_{bc10} * \frac{Z_{C10}}{r_{e10}} , \text{ and} \quad (4.39)$$

Input Impedance (Ohms)

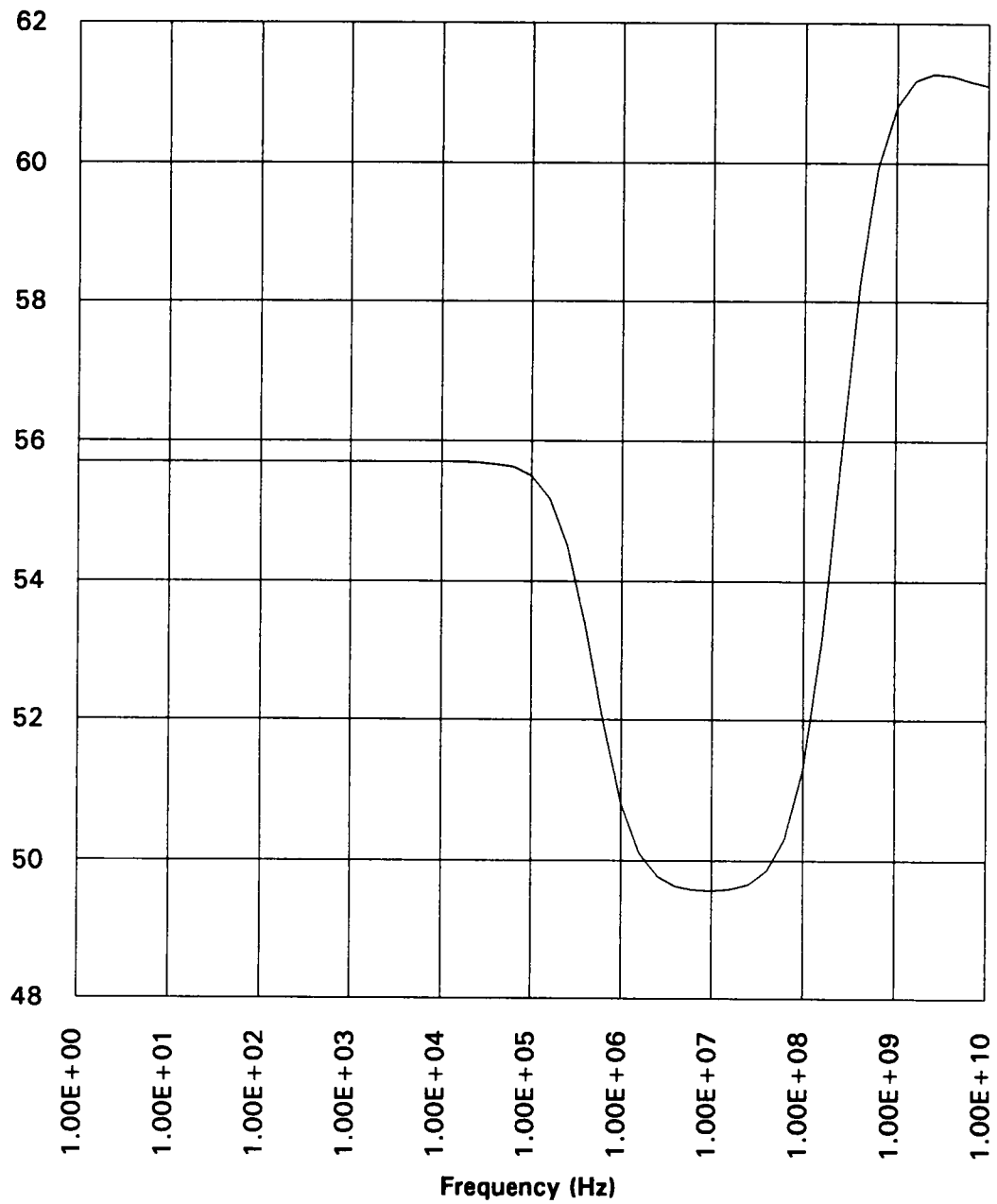


Figure 4-5. First stage input impedance.

$$Z_{C10} = (R_{C17} + r_{o17}) \parallel (R_{B11} + r_{b11} + Z_{io11}) . \quad (4.40)$$

The open-loop impedance looking into the base of Q11 was slightly different than that of Q2 (Equation 4.15) since there was one less diode and one more resistor in series with the emitter of Q11, and

$$Z_{io11} = \frac{\beta_{11} * r_{e11}}{1 + s * \beta_{11} * r_{e11} * C_{be11}} + \beta_{11} * Z_{E11} , \text{ where} \quad (4.42)$$

$$Z_{E11} = \frac{2 * r_{e12} + R_{D2} + R_{E13A} + R_{E13}}{1 + s * C_{D2} * (2 * r_{e12} + R_{D2})} . \quad (4.43)$$

The different feedback connection simplified somewhat the calculation of A_6 , the open-loop gain from the input to the base of Q11, compared to A_1 (Equation 4.19):

$$A_6 = \frac{Z_{io10} \parallel (R_{F2} + R_{E13})}{R_{S2} + Z_{io10} \parallel (R_{F2} + R_{E13})} , \quad (4.44)$$

but the gain from the base to the collector of Q10 required only subscript changes from Equation 4.20, yielding

$$A_7 = \frac{Z_{C10}}{r_{e10}} . \quad (4.45)$$

The gain from the collector of Q10 to the emitter of Q11 was

$$A_8 = \frac{\beta_{11} * Z_{E11}}{R_{B2} + r_{b2} + Z_{io2}} , \quad (4.46)$$

which had a magnitude of 0.991 and could be ignored.

The gain from the emitter of Q11 back to the base of Q10 was

$$A_9 = \frac{(Z_{O1} + Z_{S2}) \parallel Z_{io10}}{R_{F2} + [(Z_{O1} + Z_{S2}) \parallel Z_{io10}]} , \text{ where} \quad (4.47)$$

$$Z_{S2} = \frac{1 + s * R_{S2} * C_{S2}}{s * C_{S2}} , \text{ and} \quad (4.48)$$

Z_{O1} was determined by taking the parallel combination of the output impedance through Q6, Z_{o6} , and the output impedance looking through Q7, Z_{o7} .

$$Z_{o6} = R_{E6} + \frac{r_{e6}}{1 + s * r_{e6} * C_{bc6}} + \frac{r_{b6} + R_{B6}}{\beta_6} + \frac{Z_A}{\beta_6 * (1 + T_1)} , \quad (4.49)$$

$$Z_{o7} = R_{E7} + \frac{r_{e7}}{1 + s * r_{e7} * C_{bc7}} + \frac{r_{b7} + R_{B7}}{\beta_7} + \frac{Z_B}{\beta_7 * (1 + T_1)} , \text{ and} \quad (4.50)$$

$$Z_{O1} = Z_{o6} \parallel Z_{o7} . \quad (4.51)$$

Z_A and Z_B were defined as

$$Z_A = \frac{(r_{o9} + R_{C9})}{\beta_2} \parallel r_{o1} \parallel R_{F1} \parallel (Z_{D1} + R_{E5} \parallel Z_{I7}) \quad (4.52)$$

and

$$Z_B = R_{E5} \parallel Z_{D1} + [Z_{i6} \parallel R_{F1} \parallel \frac{(r_{o9} + R_{C9})}{\beta_2} \parallel r_{o1}] \quad (4.53)$$

Although the equations given above were rather complex, Z_{O1} could be modelled accurately as the parallel combination of R_{E6} and r_{e6} with R_{E7} and r_{e7} . Z_{O1} was small compared to Z_{S2} and could be ignored in Equation 4.47.

The loop gain for the second stage was therefore

$$T_2 = A_7 * A_9 \quad (4.54)$$

$$= \frac{Z_{C10} * (Z_{S2} \parallel Z_{iO10})}{r_{e10} * [R_{F2} + (Z_{S2} \parallel Z_{iO10})]} \quad .$$

Its midband gain was 44.5 and its graph is shown in Figure 4-6.

As with the first stage, the large-signal gain from the emitter of Q11 to the output was found by two methods. For a negative input pulse (which would require a positive pulse into the first stage if the two were connected) the gain to the output was (Equation 4.28)

$$A_{10N} = \frac{R_{S3} + R_L}{r_{e14} + R_{E14} + R_{S3} + R_L} \quad (4.55)$$

Second Stage Loop Transmission

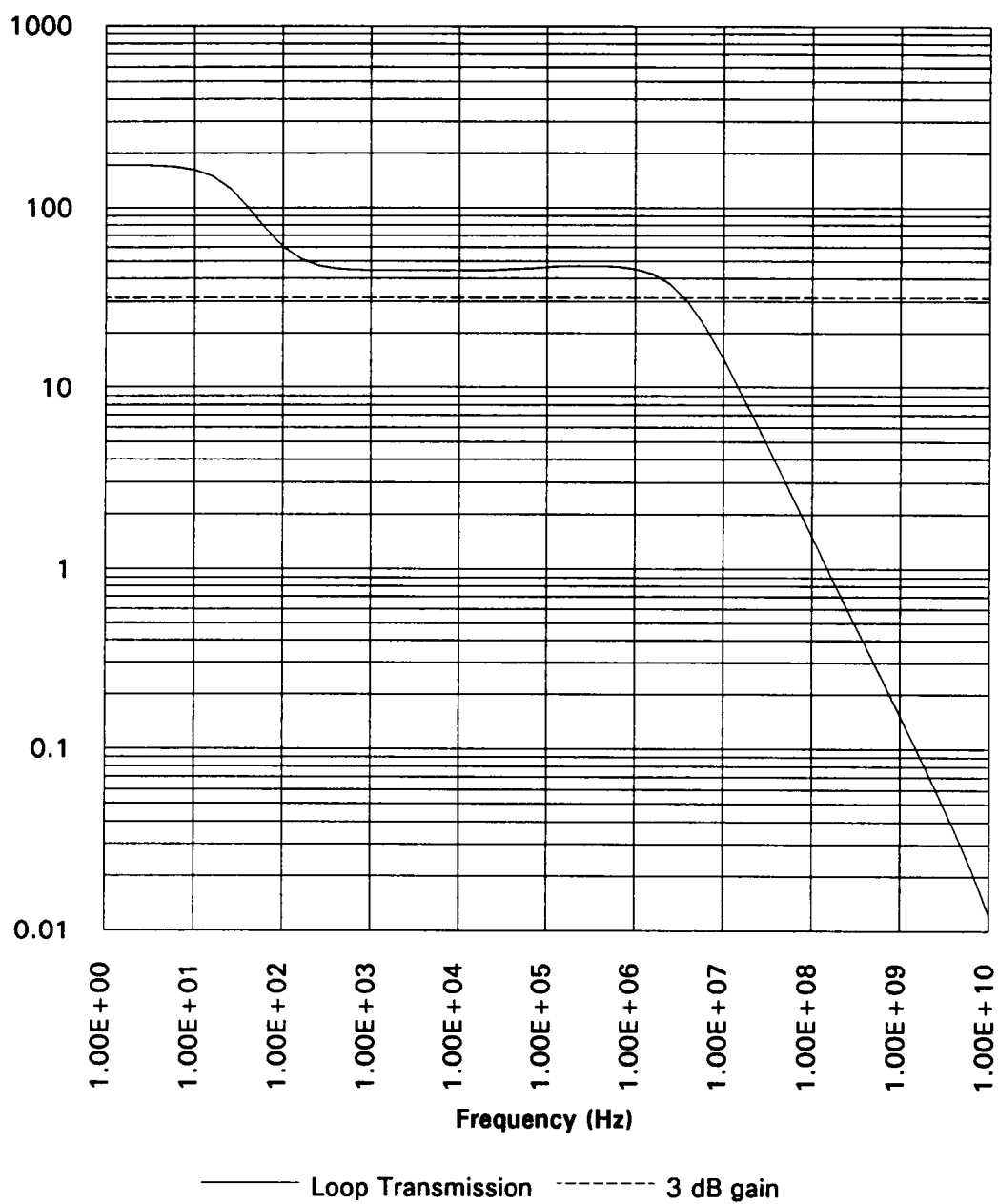


Figure 4-6. Second stage loop gain.

The large-signal gain for a positive input pulse was divided into two components, the gain from the emitter of Q11 to the resistance composed of resistors R_{E13A} and R_{E13} , denoted A_{10pa} , and the gain from there to the output, denoted A_{10pb} .

$$A_{10pa} = \frac{R_{E13A} + R_{E13}}{2 * r_{e12} + R_{D2} + R_{E13A} + R_{E13}} , \quad (4.56)$$

or approximately 0.955, since

$$r_{e12} = r_{e13} = \frac{V_{T-}}{I_{C12}} , \text{ and} \quad (4.57)$$

$$A_{10pb} = \frac{\beta_{15} * (R_{S3} + R_L)}{R_{B15} + r_{b15} + \beta_{15} * (r_{e15} + R_{E15} + R_{S3} + R_L)} . \quad (4.58)$$

The combination of Equations 4.56 and 4.58 produced

$$A_{10p} = A_{10pa} * A_{10pb} . \quad (4.59)$$

Using these results expressions were derived for the large-signal closed-loop gain from the input to the output of the second stage,

$$A_{c2n} = \frac{A_6 * A_7 * A_8 * A_{10N}}{1 + T_2} \quad (4.60)$$

$$= \frac{[Z_{io10} || (R_{F2} + R_{E13})] * Z_{C10} * (R_{S3} + R_L)}{[R_{S2} + Z_{io10} || (R_{F2} + R_{E13})] * r_{e10} * (r_{e14} + R_{E14} + R_{S3} + R_L) * (1 + T_2)}$$

for a negative input to the second stage, and

$$A_{c2p} = \frac{A_6 * A_7 * A_8 * A_{10p}}{1 + T_2} \quad (4.61)$$

$$= \frac{[Z_{io10} || (R_{F2} + R_{E13})] * Z_{C10} * (R_{S3} + R_L) * A_{10pa}}{[R_{S2} + Z_{io10} || (R_{F2} + R_{E13})] * r_{e10} * (r_{e15} + R_{E15} + R_{S3} + R_L) * (1 + T_2)}$$

for a positive second-stage input. These results are presented in Figure 4-7.

The small-signal gain of the output stage was calculated by changing the subscripts from Equations 4.35 ("6" became "14" and "7" became "15") and had a pole at a frequency

$$\omega_{10ss} = (R_{E13} + R_{E13A}) * (C_{c6} + C_{c7}) . \quad (4.62)$$

When this expression (which had a midband gain of 0.968) was used in place of A_{5N} in Equation 4.33, the resulting function had a bandwidth of 135 MHz.

The output impedance for the second stage was calculated similarly to the first stage (in Equations 4.49 and 4.50).

Second Stage Closed Loop Gains

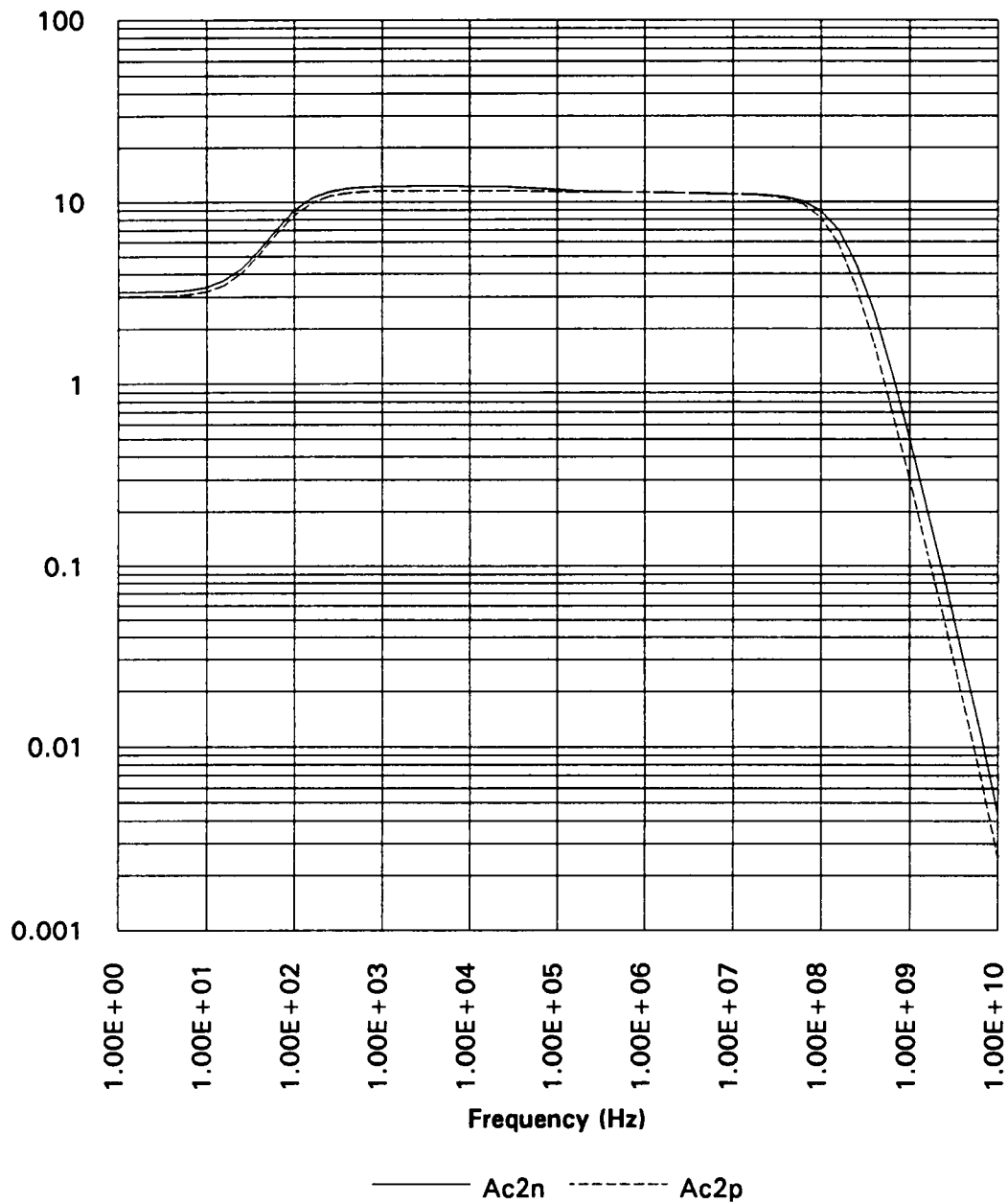


Figure 4-7. Second stage closed-loop gains.

$$Z_{o14} = R_{E14} + \frac{r_{e14}}{1 + s * r_{e14} * C_{be14}} + \frac{R_{B14} + r_{b14}}{\beta_{14}} + \frac{Z_{D2} + [R_{E13A} + (R_{E13} || R_{F2})]}{\beta_{14} * (1 + T_2)} , \quad (4.63)$$

$$Z_{o15} = R_{E15} + \frac{r_{e15}}{1 + s * r_{e15} * C_{be15}} + \frac{r_{b15} + R_{B15}}{\beta_{15}} + \frac{R_{E13A} + R_{E13} || R_{F2}}{\beta_{15} * (1 + T_2)} , \quad (4.64)$$

and these terms combined to give

$$Z_{OUT} = R_{S3} + (Z_{o14} || Z_{o15}) . \quad (4.65)$$

Since the parallel combination of Z_{o14} and Z_{o15} was less than 4Ω and R_{S3} was 47Ω , the midband value of the amplifier's output impedance was within two percent of 50Ω .

Low Frequency Response

The analysis thus far has overlooked the effects of the AC coupling achieved through capacitors C_{E1} , C_{E10} , and C_{S2} . Although a high-frequency model can be computed ignoring these capacitors, their effect at low frequencies should be considered.

Many of the equations modelling the first stage frequency response were corrected by replacing r_{e1} with Z_{E1} , where

$$Z_{E1} = r_{e1} + \frac{R_{E1}}{1 + s * R_{E1} * C_{E1}} . \quad (4.66)$$

This substitution can be made in Equations 4.11 and 4.12. The adjusted first stage closed-loop gains and input impedance are shown in Figure 4-8 and Figure 4-9, respectively.

Similarly, the second stage equations were corrected by replacing r_{e10} with Z_{E10} , where

$$Z_{E10} = r_{e10} + \frac{R_{E10}}{1 + s * R_{E10} * C_{E10}} . \quad (4.67)$$

This change affected Equations 4.36 and 4.37 and hence the closed-loop gains of the second stage.

Capacitor C_{s2} was employed because of the difficulty encountered in keeping the emitters of Q6 and Q7 at roughly the same DC level as the base of transistor Q10. Differences in these voltages caused DC currents in R_{s2} and thus problems in controlling the DC level at the output of the circuit. The capacitor formed a high pass network with resistor R_{s2} which was modelled by Z_{s2} in Equation 3.59.

Overall Response

The calculated overall large-signal gains for the amplifier were

$$A_{cn} = A_{c1n} * A_{c2p} , \quad (4.68)$$

for a negative input to the amplifier, and

Corrected First Stage Closed Loop Gains

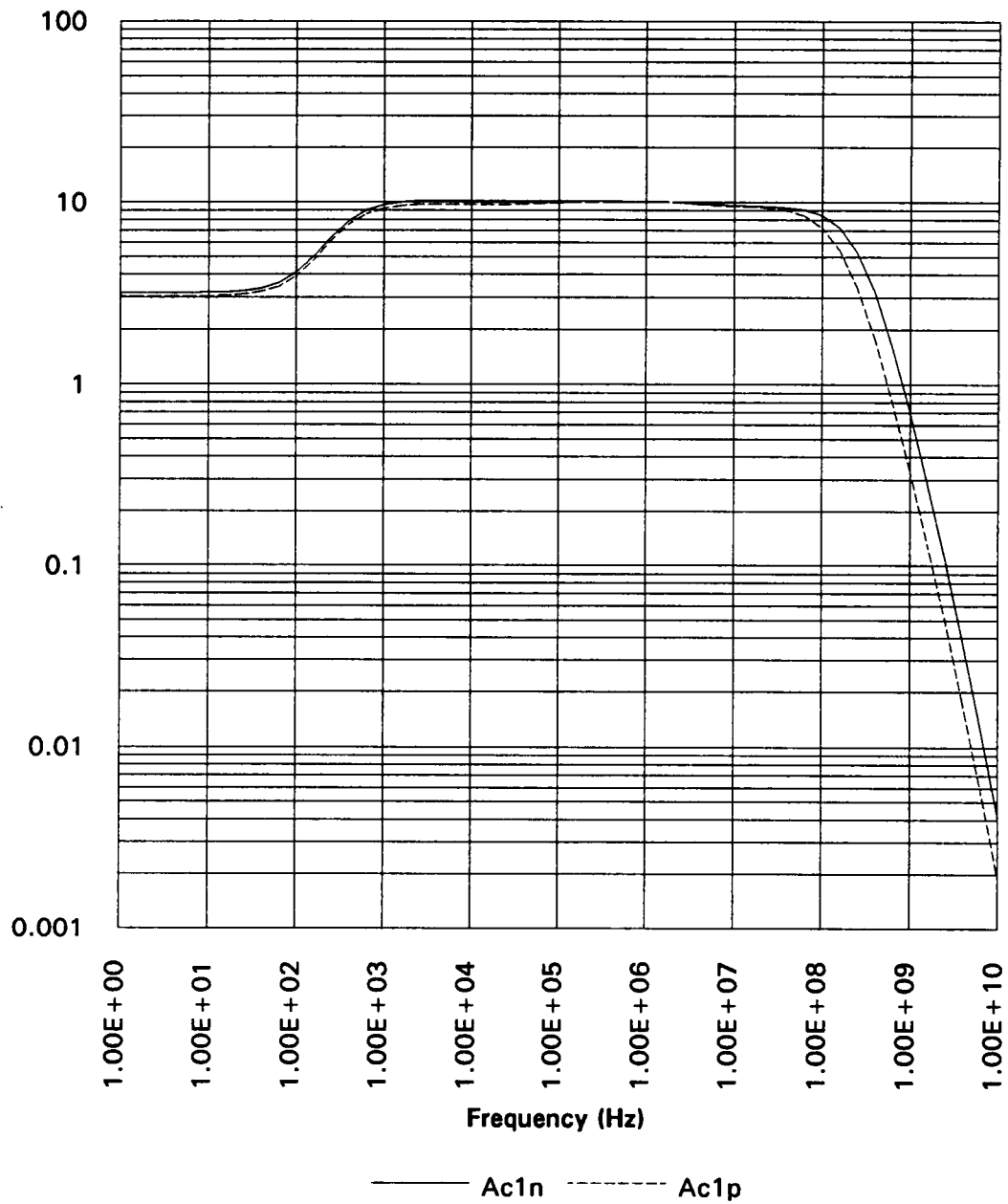


Figure 4-8. Corrected first stage closed-loop gains.

Corrected Input Impedance

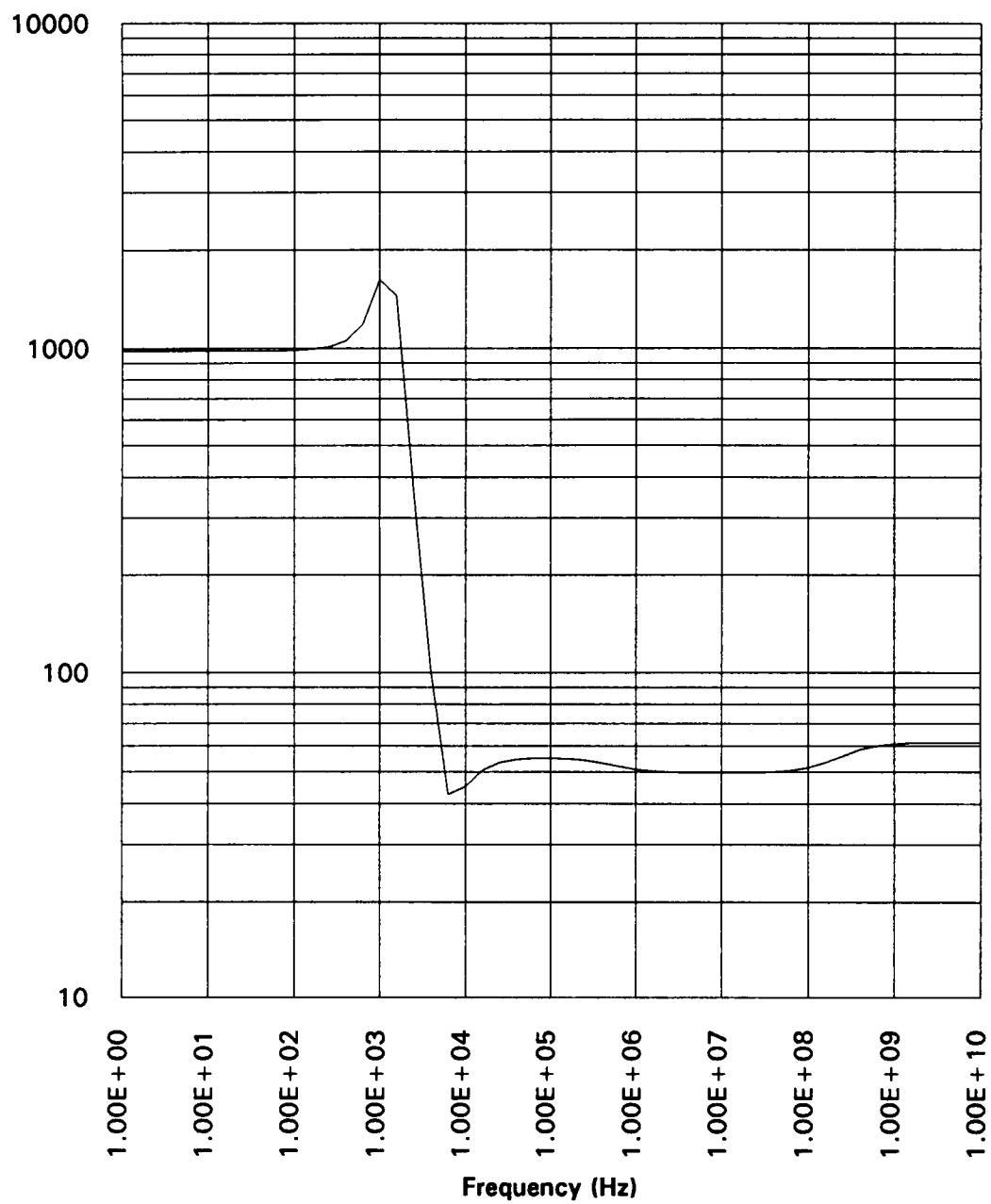


Figure 4-9. Corrected first stage input impedance.

$$A_{cp} = A_{c1p} * A_{c2n}, \quad (4.69)$$

for a positive input to the amplifier. These gains are pictured in Figure 4-10, which shows that the gains for positive and negative inputs were well-matched. The midband value of the overall gain was 105 and the 3 dB bandwidth was about 80 MHz with a rolloff of 80 dB per decade. The small-signal gain (A_{css}) is also shown in Figure 4-10. Its midband gain is 110 and it has a 98 MHz bandwidth.

The ratios of the large-signal gain for a positive input to that for a negative input at various frequencies were logged in Table 4-3 along with the percent distortion due to this difference. The distortion was calculated by averaging the gains for positive and negative inputs and finding the difference between either A_{cn} or A_{cp} and this average gain.

Noise Analysis

The noise analysis was conducted by considering the contribution of each element of the circuit, using the gain formulas derived in the AC analysis section to refer the individual contributions to the output, and adding all of the resulting output-referred noise powers together.

The noise source models used in this analysis were

Overall Closed-Loop Gains

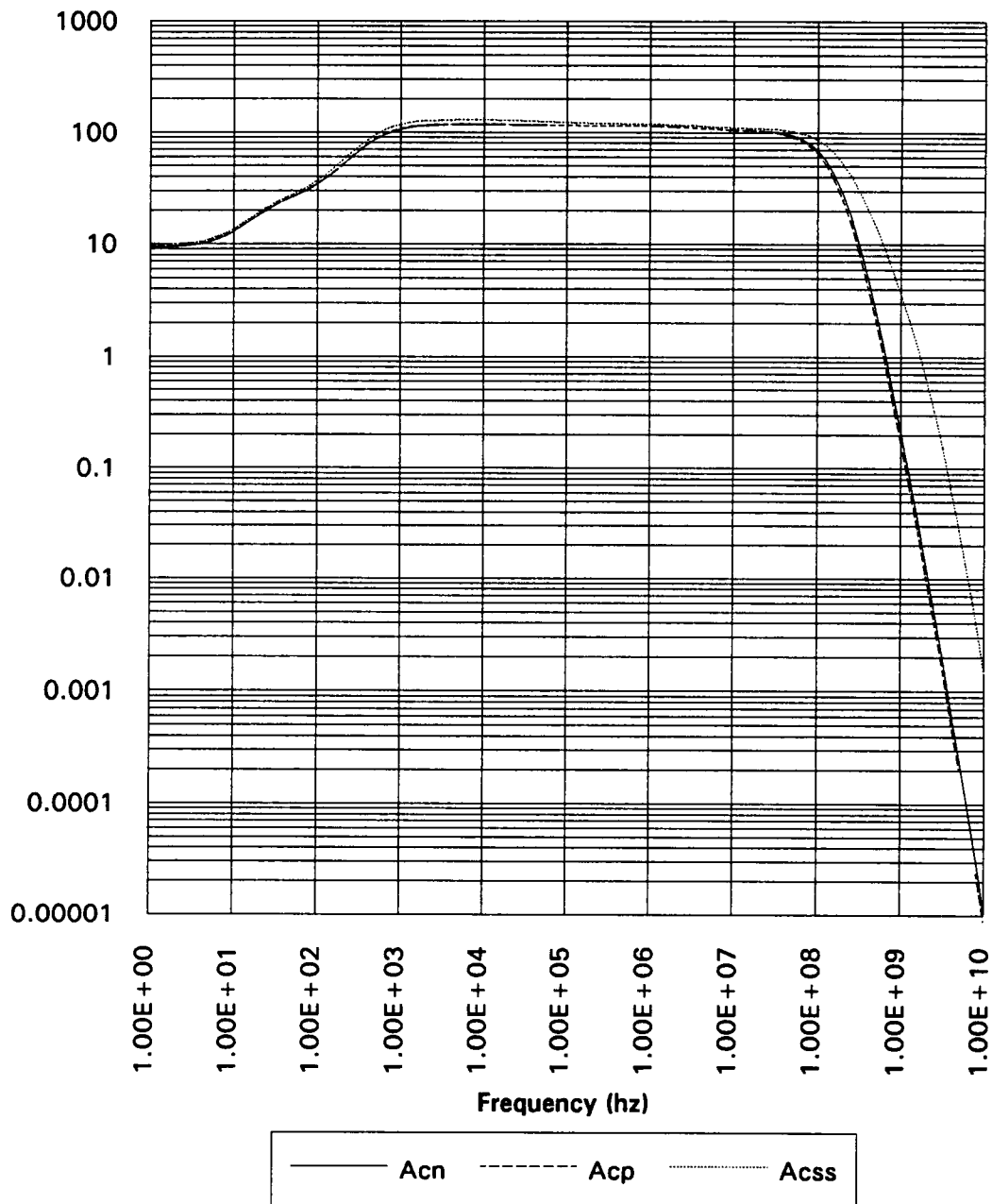


Figure 4-10. Overall closed-loop gains.

Table 4-3. Differences in gain for positive and negative inputs.

Frequency	Gain Ratio	Distortion
10 Hz	1.0176	0.87 %
100 Hz	1.0144	0.71 %
1 kHz	1.0118	0.59 %
10 kHz	1.0110	0.55 %
100 kHz	1.0017	0.09 %
1 MHz	1.0000	0.00 %
10 MHz	0.9981	0.09 %
100 MHz	0.9384	3.18 %
1 GHz	0.7953	11.4 %
10 GHz	0.7901	11.7 %

taken from a book by Gray and Meyer⁶⁴ and are summarized below. Resistors produce thermal noise, represented as either a voltage source in series with the resistor or a current source in parallel with the resistor. The voltage source had a mean square value

$$v^2 = 4 * k * T * R * BW, \quad (4.70)$$

where k was Boltzmann's constant, $8.62 * 10^{-5}$ eV/K, T was temperature, R was the value of the resistor, and BW was the bandwidth. Since the bandwidth multiplier was common to all equivalent noise voltages and currents considered in this analysis, it was implied in the calculations and not included in the formulas until noise powers were added together at the output. Although the bandwidth discussed throughout the analysis so far has been determined as the frequency at which the transfer function falls 3 dB below its midband value, this value is not the one used in noise analysis. Since this noise analysis integrates across white noise, which has a flat frequency spectrum, it would yield accurate results only if the transfer function dropped abruptly to zero at the bandwidth. The majority of these gain functions had a single-pole rolloff, which decreased at 20 dB per decade. When the product of white noise and a function of this type is integrated, the result is larger by a factor of 1.571 (or $\pi/2$) than the product of the midband value and the

bandwidth. Thus, for these calculations, a noise bandwidth that was 1.57 times as large as the 3 dB bandwidth was used. The bandwidths listed in tables were still the 3 dB bandwidths, however.

At room temperature,

$$4kT = \frac{4(8.62 * 10^{-5})(1.6 * 10^{-19} \text{ V-C})(273 \text{ K})}{K} \quad (4.71)$$

$$= 1.51 * 10^{-20} \text{ V-C.}$$

Room temperature was assumed for all calculations. The current source had a mean square value

$$i^2 = \frac{4kT * BW}{R} . \quad (4.72)$$

The bipolar transistor model used three noise sources. First, the DC current flowing through the collector produced shot noise directly proportional to this collector current, depicted by a current source connected from the collector to the emitter of the transistor with a value

$$i^2 = 2 * q * I_c * BW, \quad (4.73)$$

where q was the charge of one electron, $1.6 * 10^{-19} \text{ C}$, and I_c was the collector current. The base resistance r_b of the

transistor had thermal noise represented by a voltage source in series with the base which had a value calculated from Equation 3.81 using r_b as the resistance. The base current exhibited shot noise also, modelled by a current source connected from the base to the emitter with a value

$$i^2 = 2 * q * I_B * BW. \quad (4.74)$$

Flicker noise and burst noise are generally included in the noise models for bipolar transistors, but since these components are dominant at low frequencies the wide bandwidth of this circuit rendered them insignificant.

Capacitors and inductors made no contribution to the total noise of the circuit unless they had a parasitic resistance associated with them that produced thermal noise.

First Stage

The noise sources in the first stage were calculated, referred to the output of the first stage, and then added together before referring them to the output of the second stage.

First consider the resistor R_{S1} . It was lumped together with r_{b1} since they were represented as two voltage sources connected in series. Their noise voltage was multiplied by the full gain of the amplifier, A_{c1n} (or A_{c1p} , Equations 4.33-4.34), and thus produced a component

$$v_{RSI}^2 = 4kT * (R_{S1} + r_{b1}) * \frac{(R_{S1} + r_{b1} + Z_{io1})^2}{(R_{GEN} + R_{S1} + r_{b1} + Z_{io1})^2} * A_{v1n}^2 \quad (4.75)$$

at the output of the first stage. The gain was squared since noise powers, not voltages, were being addressed. A factor was added to the calculation that took into account the resistance looking back into the generator, which was unnecessary in computing A_{v1n} .

The current source representing the base current shot noise in Q1 drove an impedance

$$z_{b1} = Z_{io1} \parallel r_{b1} + [(R_{GEN} + R_{S1}) \parallel (R_{F1} + Z_{E2})] \quad (4.76)$$

so that at the output of the first stage

$$v_{IB1}^2 = 2q * I_{B1} * z_{b1}^2 * \frac{(A_2 * A_3 * A_{3N})^2}{(1 + T_1)^2} \quad (4.77)$$

since only the gain from the base of Q1 to the output was required.

The equivalent noise current source for the collector current drove an impedance consisting of the output resistance of Q1 in parallel with the series combination of Z_{C1} (Equation 4.13) and Z_{E1} (from Equation 4.66, excluding r_{e1}), and experienced the gains A_3 and A_{3N} divided by one plus the loop gain to the output, so that

$$v_{IC1}^2 = 2q \cdot I_{C1} \cdot \left[\frac{V_{A1}}{I_{C1}} \parallel (Z_{C1} + Z_{E1} - r_{e1}) \right]^2 \cdot \frac{(A_3 \cdot A_{5N})^2}{(1 + T_1)^2} \quad (4.78)$$

Another significant noise source was the feedback resistor, R_{F1} . Its equivalent noise voltage appeared at the emitter of Q2 (in series with R_{F1}) and thus underwent a gain of A_{5N} producing

$$v_{RF1}^2 = 4kT \cdot R_{F1} \cdot \frac{Z_{E2}^2}{(R_{F1} + Z_{E2})^2} \cdot A_{5N}^2 \quad (4.79)$$

at the output of the first stage.

The equivalent noise current source associated with R_{E1} drove an impedance composed of C_{E1} in parallel with R_{E1} and the impedance looking into the emitter of Q1, which formed a low-pass network with a corner frequency below 100 Hz. The BW multiplier for this source was lower by a factor of about 10^6 than those for the other noise sources in the circuit, so the contribution of this source was neglected.

In the analysis of the noise contribution of the current source consisting of Q8, Q9, and R_{C8} , all of the thermal noise components were grouped at the node where the bases of the two transistors were connected. Their equivalent noise voltage was calculated as

$$v_{RCS}^2 = 4kT \cdot \left(\frac{R_{C8} \cdot r_{e8}}{R_{C8} + r_{e8}} + \frac{r_{b8} \cdot \beta_9 \cdot r_{e9}}{\beta_9 \cdot r_{e9} + R_{C8}} \parallel \frac{\beta_8 \cdot r_{e8}}{\beta_8 \cdot r_{e8}} + r_{b9} \right), \quad (4.80)$$

which was multiplied by a gain to the collector of

$$A_{11} = \frac{Z_{i9}}{r_{b1} + Z_{i9}} \frac{r_{o1}}{r_{e1}}, \text{ where} \quad (4.81)$$

$$Z_{i9} = \frac{\beta_9 * r_{e9}}{1 + s * \beta_9 * r_{e9} * C_{M9}} \text{ and} \quad (4.82)$$

$$C_{M9} = C_{bc9} + \frac{C_{bc9} * (R_{C9} + r_{o1})}{r_{e9}}. \quad (4.83)$$

This product was then added to the thermal noise of R_{C9} and referred to the output to give

$$V_{CS}^2 = (V_{RCS}^2 * A_{11}^2 + \frac{V_{RC9}^2 * r_{o1}^2}{(r_{o1} + r_{e9} + R_{C9})^2}) * \frac{(A_3 * A_{5N})^2}{(1 + T_1)^2}. \quad (4.84)$$

The noise due to R_{B2} and due to r_{b2} were combined into one sum and applied to the collector of Q1, in series with R_{B2} , giving

$$V_{RB2}^2 = 4kT * \frac{(R_{B2} + r_{b2}) * (\beta_2 * Z_{E2})^2}{[\beta_2 * Z_{E2} + r_{o1} || (R_{C9} + r_{e9})]^2} \frac{(A_3 * A_{5N})^2}{(1 + T_1)^2} \quad (4.85)$$

at the output.

The impedance seen by the noise current source for I_{C2} was equal to r_{o2} in parallel with both Z_{E2} and the impedance seen looking into R_{F2} from the emitter of Q2. The noise

source underwent a gain of A_{5N} to the output of the first stage:

$$v_{IC2}^2 = 2q * I_{C2} * \left\{ \frac{r_{o2} || Z_{E2} || \left[\frac{R_{F1} + (R_{GEN} + R_{S1}) || (r_{b1} + Z_{i01})}{(1 + T_1)^2} \right]} \right\}^2 * A_{5N}^2. \quad (4.86)$$

Since Q3, Q4 and Q5 were connected as diodes (bases shorted to collectors), the powers from the noise current sources for their base and collector currents were added together. Each of these current sources drove an impedance formed by the parallel combination of r_{e3} and c_{be3} (the values for Q3 were used since these values were the same for all three transistors, except that the capacitance was slightly higher for the PNP device), but c_{be3} was omitted from this analysis since the corner frequency associated with this combination was over 50 GHz. The noise from the base currents was also ignored since it made up less than two percent of the total when combined with the collector current noise. With a gain of A_{5nb} to the output,

$$v_{I3}^2 = 2q * I_{C3} * (r_{e3})^2 * (A_{5nb})^2, \text{ and} \quad (4.87)$$

$$v_{I4,5}^2 = 2q * 2 * I_{C3} * (r_{e3})^2 * (A_{5nb})^2. \quad (4.88)$$

From these equations it appeared that the noise sources should have been combined since they had the same gain to

the output, but v_{I3}^2 had the bandwidth of A_{5nb} while the bandwidth of $v_{I4,5}^2$ was restricted by the corner frequency determined by C_{D1} and the sum of R_{D1} , r_{e4} , and r_{e5} .

The equivalent noise voltages due to r_{b4} , r_{b5} , R_{D1} , and R_{E5} were also referred to the output producing

$$v_{RE5}^2 = 4kT * R_{E5} * \frac{Z_{RE5}^2}{(R_{E5} + Z_{RE5})^2} * (A_{5N})^2, \text{ where} \quad (4.89)$$

$$Z_{RE5} = Z_{I7} || Z_{I6} || (R_{F1} + R_{S1} + R_{GEN}) || \frac{r_{o1}}{\beta_2} || \frac{R_{C9} + r_{o9}}{\beta_2}, \text{ and} \quad (4.90)$$

$$v_{D1}^2 = 4kT * (r_{b4} + r_{b5} + R_{D1}) * (A_{5N})^2. \quad (4.91)$$

The bandwidth for Equation 4.91 was the same as that of Equation 4.89, and Equation 4.90 assumed that Z_{D1} , r_{e3} , r_{e2} , r_{b2} and R_{B2} were small compared to the other impedances.

Finally, to calculate the noise generated by the driver stage the impedances looking into the bases of transistors Q6 and Q7 found in Equations 4.17 and 4.18 were used. Employing these terms, the expressions for noise from the driver stages at the output were

$$v_{Q6}^2 = [2q * I_{B6} * Z_{IB6}^2 + 4kT * (R_{B6} + r_{b6})] * A_{5nb}^2 \quad (4.92)$$

and

$$v_{Q7}^2 = [2q * I_{B7} * Z_{IB7}^2 + 4kT * (R_{B7} + r_{b7})] * A_{5pb}^2, \text{ where} \quad (4.93)$$

$$Z_{IB6} = \frac{\beta_6 * r_{e6} * [R_{E6} + R_{E7} + r_{e7} + \frac{(r_{b7} + R_{B7} + Z_{D1} + R_{B6} + r_{b6})}{\beta_7}]}{\beta_6 * r_{e6} + R_{E6} + R_{E7} + r_{e7} + \frac{r_{b7} + R_{B7} + Z_{D1} + R_{B6} + r_{b6}}{\beta_7}}, \text{ and (4.94)}$$

$$Z_{IB7} = \frac{\beta_7 * r_{e7} * [R_{E7} + R_{E6} + r_{e6} + \frac{(r_{b6} + R_{B6} + Z_{D1} + R_{B7} + r_{b7})}{\beta_6}]}{\beta_7 * r_{e7} + R_{E7} + R_{E6} + r_{e6} + \frac{r_{b6} + R_{B6} + Z_{D1} + R_{B7} + r_{b7}}{\beta_6}}. \quad (4.95)$$

Thus

$$v_{IC6}^2 = 2q * I_{C6} * [r_{o6} || R_{S2} || (R_{E7} + Z_{o7})]^2 \quad (4.96)$$

$$v_{IC7}^2 = 2q * I_{C7} * [r_{o7} || R_{S2} || (R_{E6} + Z_{o6})]^2 \quad (4.97)$$

The next task was the calculation of the magnitudes and bandwidths of the gain expressions used to find the noise powers at the output due to each of the individual components. These figures are summarized in Table 4-4 below.

The third and fourth entries in Table 4-4 have asterisks by their gain values because the magnitudes were not flat across their bandwidths. Peaking occurred in these functions and will be discussed later.

These results were used to calculate the individual components of the noise power at the output of the first stage, which are presented in Table 4-5 below. The second column was calculated using adjusted bandwidths for the first stage gains, which reflected the effects of the second

Table 4-4. Magnitude and bandwidth of gain expressions used to calculate first stage output noise voltages.

	Gain	Bandwidth
A_{c1n}	10.11	160 MHz
z_{b1}	85.6	2.6 MHz
$\frac{A_2 * A_3 * A_{5N}}{1 + T_1}$	40.1*	187 MHz
$\frac{A_3 * A_{5N}}{1 + T_1}$	0.015*	160 MHz
A_{5N}	0.901	316 MHz
A_{11}	741	
A_{5nb}	0.901	316 MHz
A_{5pb}	0.860	158 MHz

stage's 120 MHz bandwidth. These figures more accurately predict the noise contribution of each component to the total.

The noise figures obtained for the output of the first stage were next multiplied by the closed loop gain of the second stage to find the total noise at the output. It was obvious after calculating the first stage output-referred noise that some of the components were insignificant compared to others and could be omitted from further computations. Included in this list were v_{ib12} , v_{ic1}^2 , v_{CS}^2 , v_{RB2}^2 , and $v_{i3,4,5}^2$. The other values were multiplied by the second stage

Table 4-5. Noise powers of first stage noise components referred to the output of the first stage.

	Noise Power (V^2)	Using Output BW
V_{RS1}^2	$8.53 * 10^{-9}$	$4.78 * 10^{-9}$
V_{IB1}^2	$6.87 * 10^{-11}$	$6.87 * 10^{-11}$
V_{IC1}^2	$1.73 * 10^{-6}$	$1.96 * 10^{-7}$
V_{RF1}^2	$6.87 * 10^{-10}$	$2.39 * 10^{-10}$
V_{CS}^2	$4.65 * 10^{-8}$	$2.33 * 10^{-8}$
V_{RB2}^2	$1.68 * 10^{-10}$	$1.92 * 10^{-11}$
V_{IC2}^2	$2.15 * 10^{-8}$	$2.70 * 10^{-9}$
V_{I3}^2	$1.45 * 10^{-11}$	$5.06 * 10^{-12}$
$V_{I4,5}^2$	$2.91 * 10^{-11}$	$1.01 * 10^{-11}$
V_{RE5}^2	$7.82 * 10^{-14}$	$2.73 * 10^{-14}$
V_{D1}^2	$5.92 * 10^{-14}$	$5.92 * 10^{-14}$
V_{Q6}^2	$3.24 * 10^{-10}$	$2.29 * 10^{-10}$
V_{IC6}^2	$5.15 * 10^{-11}$	$1.79 * 10^{-11}$
V_{Q7}^2	$3.24 * 10^{-10}$	$2.29 * 10^{-10}$
V_{IC7}^2	$5.15 * 10^{-11}$	$1.79 * 10^{-11}$
Total	$1.81 * 10^{-6}$	$2.28 * 10^{-7}$

gain, which had a magnitude of 11.4 over a bandwidth from 400 Hz to 120 MHz. They were then combined with the noise components from the second stage, which were calculated next.

Some of the gains used to calculate the noise powers at the output of the first stage had peaks outside the bandwidth of the amplifier since the loop gain did not attenuate them at these high frequencies. The noise affected by these gains was therefore multiplied by a large bandwidth, resulting in some high noise powers. In a more accurate mathematical model for the circuit, more poles would be present to attenuate the gain and filter the noise at high frequencies. In order to reflect this condition, the noise powers were recalculated ignoring these high-frequency peaks, and the results were compiled in Table 4-6.

This recalculation decreases the noise in the second column of Table 4-6 (that limited by the output bandwidth) by almost an order of magnitude and the unadjusted noise power at the output of the first stage by over an order of magnitude.

Second Stage

Since the configuration of the second stage was so similar to that of the first, the computation of the output-referred noise could be simplified somewhat. The second-stage components corresponding to those in the first stage,

Table 4-6. Noise powers at the output of Stage 1 ignoring the effects of high frequency gain peaks.

	Noise Power (V^2)	Using Output BW
V_{RS1}^2	$8.53 * 10^{-9}$	$4.78 * 10^{-9}$
V_{IB1}^2	$6.87 * 10^{-11}$	$6.87 * 10^{-11}$
V_{IC1}^2	$4.07 * 10^{-10}$	$2.29 * 10^{-10}$
V_{RF1}^2	$6.87 * 10^{-10}$	$2.39 * 10^{-10}$
V_{CS}^2	$4.60 * 10^{-8}$	$2.31 * 10^{-8}$
V_{RB2}^2	$3.99 * 10^{-14}$	$2.25 * 10^{-14}$
V_{IC2}^2	$6.66 * 10^{-12}$	$3.96 * 10^{-12}$
V_{I3}^2	$1.45 * 10^{-11}$	$5.06 * 10^{-12}$
$V_{I4,5}^2$	$2.91 * 10^{-11}$	$1.01 * 10^{-11}$
V_{RES}^2	$7.82 * 10^{-14}$	$2.73 * 10^{-14}$
V_{DI}^2	$5.92 * 10^{-14}$	$5.92 * 10^{-14}$
V_{Q6}^2	$3.24 * 10^{-10}$	$1.13 * 10^{-10}$
V_{IC6}^2	$5.15 * 10^{-11}$	$1.79 * 10^{-11}$
V_{Q7}^2	$3.24 * 10^{-10}$	$1.13 * 10^{-10}$
V_{IC7}^2	$5.15 * 10^{-11}$	$1.79 * 10^{-11}$
Total	$5.70 * 10^{-8}$	$2.86 * 10^{-8}$

which had a negligible contribution to the total noise, were disregarded. In general, the second stage of a well-designed circuit would not contribute appreciably to the overall noise since the noise sources in the first stage would be subject to a significantly higher gain, in this case by a factor of about ten.

The components analyzed for noise contribution in the second stage were R_{S2} , I_{C10} , R_{F2} , I_{C11} , R_{S3} , the current source, and the output drivers, Q14 and Q15. Most of these components had first stage analogs so the gain formulas were calculated easily by changing the appropriate subscripts. The exceptions were: R_{S2} , since the previous stage's output impedance was negligible, unlike the 50 Ω impedance of the generator seen by the first stage; R_{F2} , since it was connected differently than R_{F1} was in the first stage; and R_{S3} , which had no first stage equivalent. The noise from R_{S3} appeared directly at the output and was assigned the system bandwidth.

The equations involving only subscript changes from the first stage analysis were

$$v_{IC10}^2 = 2q * I_{C10} * \left[\frac{V_{A10}}{I_{C10}} \parallel (Z_{C10} + Z_{E10} - r_{e10}) \right]^2 * \frac{(A_s * A_{10N})^2}{(1 + T_2)^2}, \quad (4.98)$$

$$v_{CS2}^2 = (v_{RCS2}^2 * A_{12}^2 + \frac{v_{RC17}^2 * r_{o10}^2}{(r_{o10} + r_{o17} + R_{C17})^2}) * \frac{(A_s * A_{10N})^2}{(1 + T_2)^2}, \text{ where} \quad (4.99)$$

$$V_{RCS2}^2 = 4kT * \left(\frac{R_{C16} * r_{e16}}{R_{C16} + r_{e16}} + \frac{r_{b16} * \beta_{17} * r_{e17}}{\beta_{17} * r_{e17} + R_{C16} || \beta_{16} * r_{e16}} + r_{b17} \right), \quad (4.100)$$

$$A_{12} = \frac{Z_{i17}}{r_{b10} + Z_{i17}} \frac{r_{o10}}{r_{e17}}, \text{ where} \quad (4.101)$$

$$Z_{i17} = \frac{\beta_{17} * r_{e17}}{1 + s * \beta_{17} * r_{e17} * C_{M17}}, \text{ and} \quad (4.102)$$

$$C_{M17} = C_{bc17} + \frac{C_{bc17} * (R_{C17} + r_{o10})}{r_{e17}}. \quad (4.103)$$

Also,

$$V_{IC11}^2 = i_{IC11}^2 * \left(\frac{V_{A11}}{I_{C11}} || Z_{E11} || \frac{(R_{C17} + r_{o17})}{\beta_{11}} || r_{o10} \right)^2 * \frac{(A_s * A_{10N})^2}{(1 + T_2)^2}, \quad (4.104)$$

$$V_{Q14}^2 = [2q * I_{B14} * Z_{IB14}^2 + 4kT * (R_{B14} + r_{b14})] * A_{10nb}^2, \quad (4.105)$$

$$V_{Q15}^2 = [2q * I_{B15} * Z_{IB15}^2 + 4kT * (R_{B15} + r_{b15})] * A_{10pb}^2, \text{ where} \quad (4.106)$$

$$Z_{IB14} = \frac{\beta_{14} * r_{e14} * [R_{E14} + R_{E15} + r_{e15} + \frac{(r_{b15} + R_{B15} + Z_{D2} + R_{B14} + r_{b14})}{\beta_{15}}]}{\beta_{14} * r_{e14} + R_{E14} + R_{E15} + r_{e15} + \frac{r_{b15} + R_{B15} + Z_{D2} + R_{B14} + r_{b14}}{\beta_{15}}}, \quad (4.107)$$

$$Z_{IB15} = \frac{\beta_{15} * r_{e15} * [R_{E15} + R_{E14} + r_{e14} + \frac{(r_{b14} + R_{B14} + Z_{D2} + R_{B15} + r_{b15})}{\beta_{14}}]}{\beta_{15} * r_{e15} + R_{E15} + R_{E14} + r_{e14} + \frac{r_{b14} + R_{B14} + Z_{D2} + R_{B15} + r_{b15}}{\beta_{14}}}; \quad (4.108)$$

$$v_{IC14}^2 = 2q * I_{C14} * [r_{o14} || (R_{S3} + R_L) || (R_{E15} + Z_{o15})]^2 \text{ and} \quad (4.109)$$

$$v_{IC15}^2 = 2q * I_{C15} * [r_{o15} || (R_{S3} + R_L) || (R_{E14} + Z_{o14})]^2 . \quad (4.110)$$

The equations that differed from the first stage were

$$v_{RS3}^2 = 4kT * R_{S3} , \quad (4.111)$$

$$v_{RF2}^2 = 4kT * R_{F2} * \frac{Z_{RF3}^2}{(R_{F2} + Z_{RF3})^2} * A_{10N}^2 , \text{ where} \quad (4.112)$$

$$Z_{RF3} = R_{E13} || \{ R_{E13A} + (R_{B15} + Z_{i15}) || (R_{B14} + Z_{i14}) || [r_{o10} || (R_{C17} + r_{o17})] \} \quad (4.113)$$

and

$$v_{RS2}^2 = 4kT * (R_{S2} + r_{b10}) * A_{c2n}^2 , \quad (4.114)$$

and the noise at the output of the first stage was referred to the output through a gain of A_{c2n} :

$$v_{STG1}^2 = v_{SUM}^2 * (A_{c2n})^2 , \quad (4.115)$$

where v_{SUM}^2 stood for the sum of the noise powers at the output of the first stage.

The gain and the bandwidth of the gains used in the preceding computations are listed in Table 4-7 below, and the noise powers referred to the output were tabulated and listed in Table 4-8. The total output referred noise, $3.76 * 10^{-6}$ Volts², corresponds to an equivalent input noise voltage of $2.83 * 10^{-10}$ Volts² or 1.41 nV/rt Hz, calculated using an overall gain of 115.3 and a bandwidth of 90 MHz.

Table 4-7. Magnitude and bandwidth of gain expressions used to calculate second stage output noise voltages.

	Gain	Bandwidth
A_{c2n}	11.4	126 MHz
$\frac{A_g * A_{10N}}{1 + T_2}$	0.02*	120 MHz
A_{10N}	0.977	309 MHz
A_{10nb}	0.977	309 MHz
A_{10pb}	0.921	200 MHz

Table 4-8. Noise powers referred to the output of the second stage.

	Noise Power (V^2)	Ignoring Peaks
V_{RS2}^2	$3.19 * 10^{-8}$	$3.19 * 10^{-8}$
V_{IC10}^2	$1.92 * 10^{-6}$	$3.38 * 10^{-10}$
V_{RF2}^2	$3.93 * 10^{-9}$	$3.93 * 10^{-9}$
V_{CS2}^2	$1.03 * 10^{-7}$	$1.45 * 10^{-8}$
V_{IC11}^2	$2.87 * 10^{-10}$	$3.23 * 10^{-14}$
V_{Q14}^2	$3.74 * 10^{-10}$	$3.74 * 10^{-10}$
V_{IC14}^2	$1.07 * 10^{-10}$	$1.07 * 10^{-10}$
V_{Q15}^2	$2.16 * 10^{-10}$	$2.16 * 10^{-10}$
V_{IC15}^2	$1.07 * 10^{-10}$	$1.07 * 10^{-10}$
V_{RS3}^2	$1.33 * 10^{-10}$	$1.33 * 10^{-10}$
V_{STG1}^2	$2.96 * 10^{-5}$	$3.72 * 10^{-6}$
Total	$3.17 * 10^{-5}$	$3.76 * 10^{-6}$

Circuit Simulation

The circuit was modelled with PSpice using the model listing in Appendix 1. The model included all of the components shown in the circuit schematics of Figures 4-1 and 4-2.

The first elements necessary for accurate circuit modelling were reliable transistor models. These models were obtained using the PARTS program contained in PSpice, which returned PSpice parameters for devices when supplied with the appropriate information from the data sheets⁶⁶. The transistors selected for use in the amplifier were 2SC3585, the MMBR571L, the MMBR901L (all NPNs), and the BSR12 (a PNP device). The data provided for these transistors are summarized in Table 4-9 below.

The PSpice model for the MMBR571L was found in the following way. For bipolar transistors, the first screen in the PARTS program determines I_S , X_{TI} , and E_G , the PSpice model parameters representing saturation current, its temperature coefficient, and the activation energy, respectively. The determination of these values is made from data describing the saturation characteristics of the transistor, which were not included on the MMBR571L data sheets. Therefore the value for I_S was determined by experimentally measuring the collector current as a function of the base-emitter voltage over several decades and extrapolating the

Table 4-9. Data sheet parameters for transistors.

	2SC3585	MMBR571L	MMBR901L	BSR12
V_{CBO} (V)	20	20	25	12
V_{CEO} (V)	10	10	15	12
V_{EBO} (V)	1.5	3	3.0	4.0
I_{Cmax} (mA)	35	80	30	80
P_D (mW)	200	200	350	225
h_{FE} typ.	100	50-300	30-200	30-120
C_{obo} (pF)	0.3	0.9	1.0	3.5
C_{ibo} (pF)	-	2.3	-	3.5
f_T (GHz)	10.0	8	4	0.5

curve to $V_{bc} = 0$ Volts, where the corresponding current was the saturation current for the transistor, which was 1.5×10^{-15} Amperes for the MMBR571L. PSpice offered the standard values of 3 and 1.11 for XTI and EG, respectively, and these quantities were used for the model.

The next screen in the PARTS program determines VAF, the forward Early voltage, from a plot of h_{oe} , the small-signal output admittance, versus the collector current with the collector-emitter voltage held constant. Again this curve was not available from the data sheets provided, but this information could be obtained from a curve tracer. PARTS returned a value of 38.73 for VAF.

The PARTS program then used an h_{FE} (forward DC beta) versus collector current curve at a constant collector-emitter voltage to calculate the parameters BF, ISE, NE, IKF, NK, and XTB. BF represented the maximum forward beta of the transistor and NE was the emission coefficient associated with ISE, the base-emitter saturation current. IKF was the current where the forward beta curve began to roll off, NK was the roll-off slope exponent, and XTB was the temperature coefficient associated with the forward beta. As the data sheets had a beta value for only one collector current, experimentally-determined values were again used to generate the needed parameters. The curve tracer did not yield precise values for collector currents below 0.2 mA, which according to the data was above the low-current beta rolloff, so with the resultant parameters PSpice may be unable to accurately model low-current performance. However, since the transistors in this amplifier were biased well above 0.2 mA the model should be sufficient for this application. XTB was left at the normal value of 1.5 recommended in the PSpice manual.⁶⁶

Collector-base capacitance was also modelled by the PARTS program. Using a V_{cb} (reverse collector-base junction voltage) versus C_{ob0} (open circuit output capacitance) curve, the parameters CJC, VJC, MJC, and FC were approximated, representing the zero-bias collector-base junction capacitance, junction potential, grading coefficient, and the

coefficient for the onset of forward-bias depletion capacitance, respectively. For FC the standard value of 0.5 was employed, and the capacitance curves included with the data sheets were used to estimate the remaining parameters. The documentation⁶⁶ notes that some extra capacitance should be included across the base-collector junction in the circuit model to simulate the extra capacitance contributed by the package.

The capacitance across the base-emitter junction was modelled as well. The V_{eb} versus C_{ibo} curve (reverse emitter-base junction voltage versus open circuit input capacitance curve) allowed PARTS to generate CJE, VJE, and MJE, the zero-bias emitter-base junction capacitance, junction potential, and grading coefficients. Again, the required curve was included with the data sheets so these values were easily determined. The documentation⁶⁶ also recommends that extra capacitance should be included across the base-emitter junction in the circuit model to account for packaging effects.

To model storage time effects, PARTS used a collector current versus storage time plot (I_c versus t_s) at a constant collector-emitter voltage to produce the parameter TR. Only the data sheets for the BSR12 had storage time information, so values of TR for the other transistors were estimated.

The last parameters modelled by PARTS for the bipolar transistors had to do with gain bandwidth. Given a curve representing unity gain bandwidth versus collector current (f_T versus I_C) at a constant collector-emitter voltage the program calculated values for TF, ITF, XTF, and VTF. TF is the ideal forward transit time. ITF models the effects of high collector currents on the gain bandwidth. VTF is a parameter that models the dependency of the forward transit time on the collector-emitter voltage, and XTF is the coefficient for this dependency. The current gain-bandwidth versus collector current plot in the data sheets made the determination of these parameters simple.

The results predicted by PSpice are listed in Table 4-10 below. Important characteristics of the amplifier that were modelled with PSpice were the gain, bandwidth, rise

Table 4-10. PSpice predictions for circuit characteristics.

Parameter	Stage 1	Stage 2	Overall
Gain	9.27	10.97	101.7
Bandwidth	340 MHz	215 MHz	141 MHz
Nonlinearity	0.2 %	1.1 %	1.1 %
Rise Time	1.27 ns	2.76 ns	2.94 ns
Gain mar.	18.4 dB	36.1 dB	-
Phase mar.	40.1 deg.	85.8 deg.	-

time, linearity, and stability (phase margin) of the circuit. The results of the hand calculations were included in Table 4-11 for comparison, but since the hand calculations yielded a loop transmission with a dominant pole, which caused a lower predicted but higher gain, the gain and phase margins were not very useful. A plot of the overall transfer function for the circuit generated by PSpice was included as Figure 4-11.

The linearity of the circuit was determined by measuring the gain for values of input pulses ranging from 20 μ V to 20 mV and dividing the variation from the midband gain by the midband gain. The second stage exhibited greater nonlinearity than the first due to the drive requirements of the output. The maximum nonlinearity occurred when the output was driving ± 2 Volts into its 100 Ω load.

The rise times were measured for the same range of

Table 4-11. Hand calculation predictions for circuit characteristics.

Parameter	Stage 1	Stage 2	Overall
Gain	9.6	11.1	105.5
Bandwidth	179 MHz	129 MHz	81 MHz
Rise Time	2.0 ns	2.7 ns	4.3 ns
Phase mar.	~ 90 deg.	~ 90 deg.	-

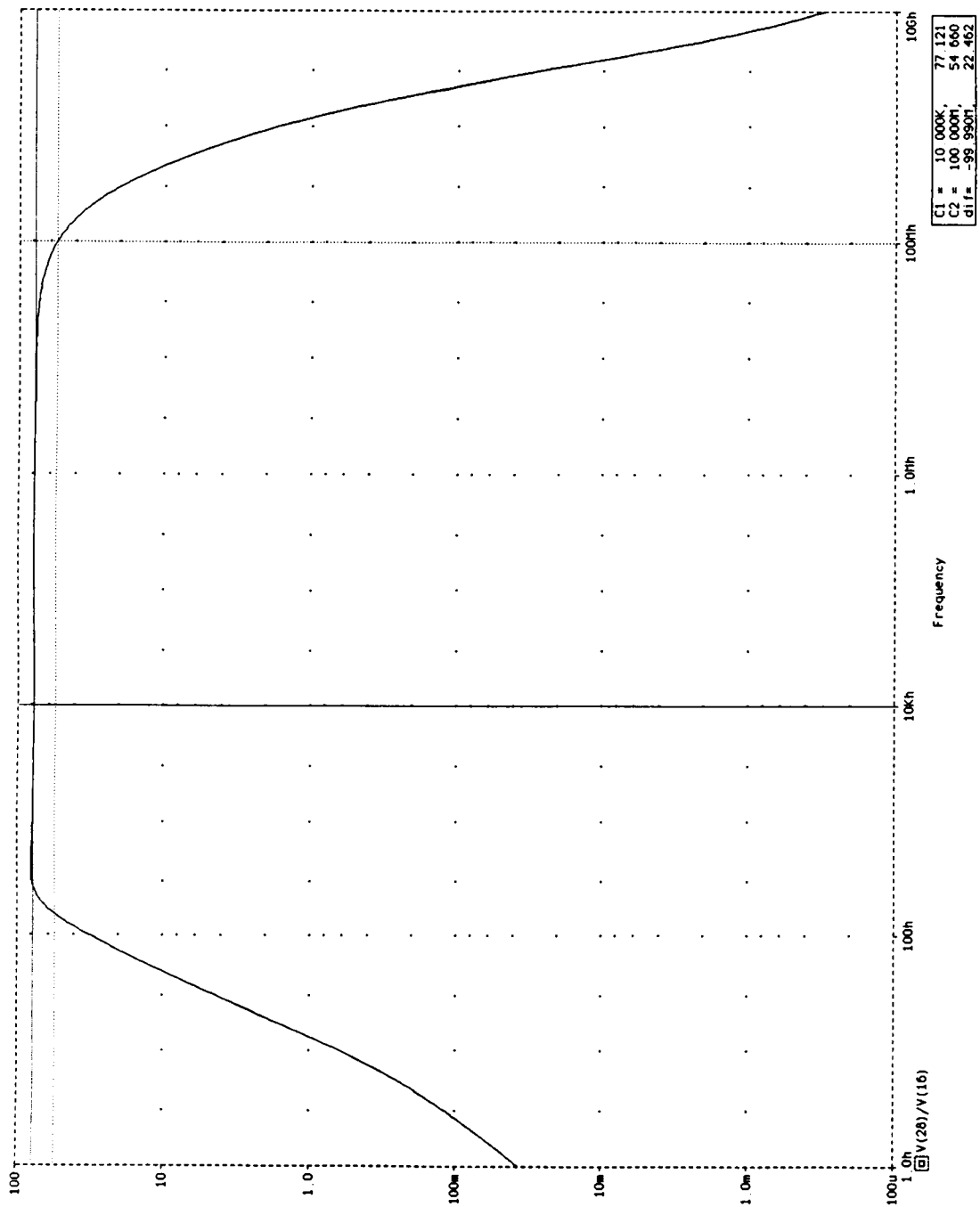


Figure 4-11. PSpice predicted overall transfer function.

input values, and the worst-case rise times were given for each stage and for the whole amplifier. These times were adjusted so as not to reflect the rise times of the input pulses or previous stages. This was done by squaring the rise time, subtracting the square of the rise time of the input signal, and taking the square root of this difference. The input signal used in the PSpice simulation had a 1.0 ns rise time. The small-signal rise times measured were 1.12 ns for the first stage, 2.16 ns for the second stage, and 2.41 ns for both stages together.

The gain and phase margins were computed by disconnecting resistors R_{F1} and R_{F2} from the bases of Q1 and Q10, respectively, and connecting them to a network approximating the impedance seen at the nodes to which R_{F1} and R_{F2} had been connected. The network was configured like the elements Q1, Q8, Q9, R_{C8} , R_{C9} , R_{E1} , and C_{E1} in Figure 4-1 with a resistor equivalent to $R_{S1} + R_{GEN}$ connected from the base of Q1 to ground.

The loop transmission for each stage was then found by dividing the voltage across the appropriate equivalent resistance by the voltage at the base of either Q1 or Q10. When this gain ratio decreased to unity, the phase difference between the two points was measured and subtracted from 180 degrees, yielding the phase margin. At the frequency where the two nodes became 180 degrees out of phase, the

adjusted gain from the input to the output side was measured and converted to decibels. This value was the gain margin.

PSpice also performed a detailed noise analysis of the circuit. A graph of the power spectral density of the output-referred noise predicted by PSpice is given in Figure 4-12, which has a midband value of $1.76 * 10^{-14}$ Volts²/Hz. This value translated to 133 nV/rt Hz at the output and 1.31 nV/rt Hz at the input, and these equivalent noise voltages are shown in Figure 4-13. Thus the PSpice noise prediction for the input equivalent noise voltage matches the value obtained in the hand calculations, 1.41 nV/rt Hz, to within 10%.

Circuit Layout

The circuit layout for this project was done by hand and is depicted in Figure 4-14. Some important considerations taken into account while designing the layout were: 1) to make all feedback loops physically short, thereby reducing phase shift, 2) to have a large ground plane running throughout the layout, 3) to keep the connecting pads for the collectors of transistors Q1 and Q10 small and clear the ground plane around them, reducing stray capacitance at these critical nodes, and 4) to keep bypass capacitors physically close to the nodes where large voltage and/or

Pspice Noise Analysis Results

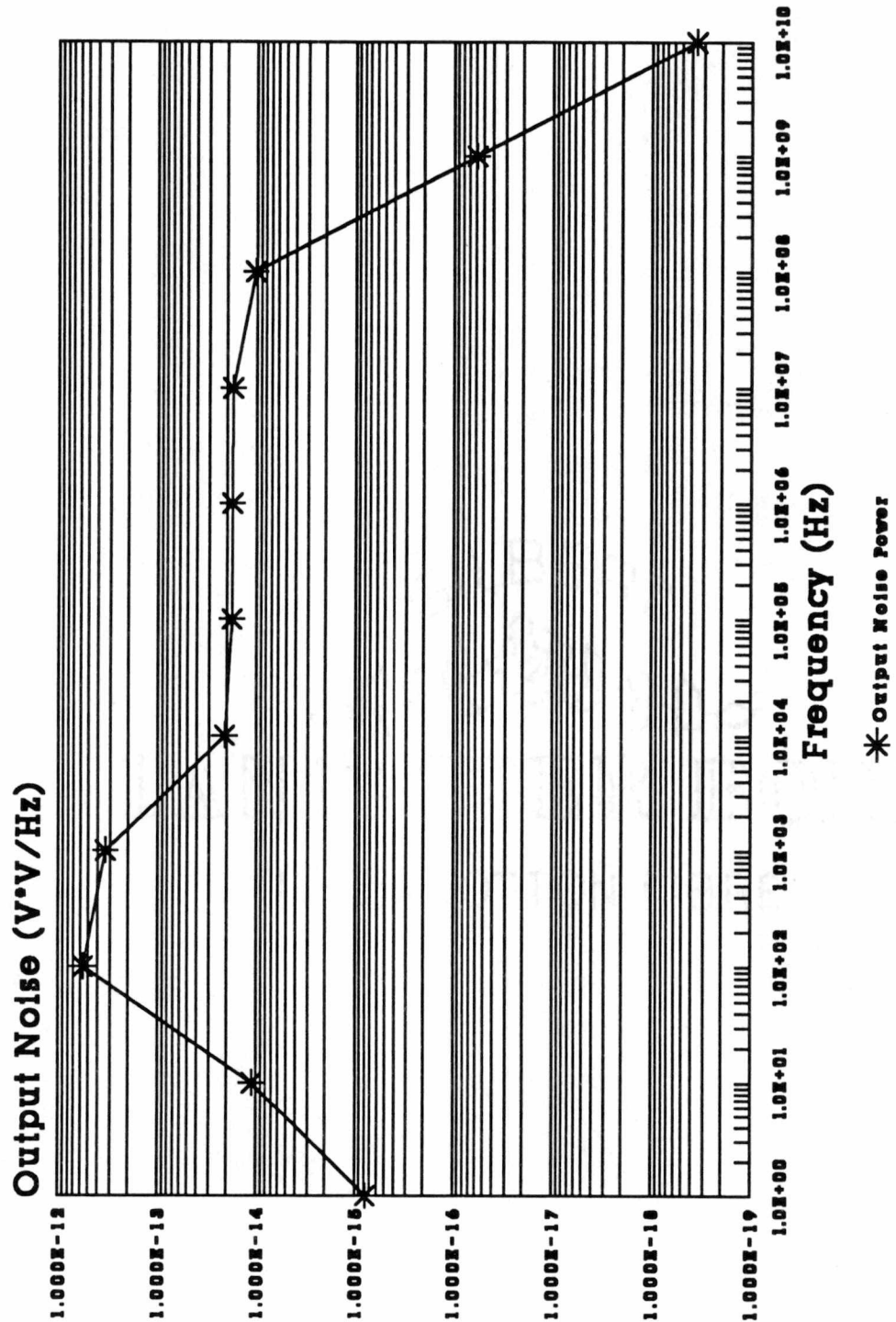


Figure 4-12. Output noise power spectral density predicted by PSpice.

PSpice Noise Analysis Results

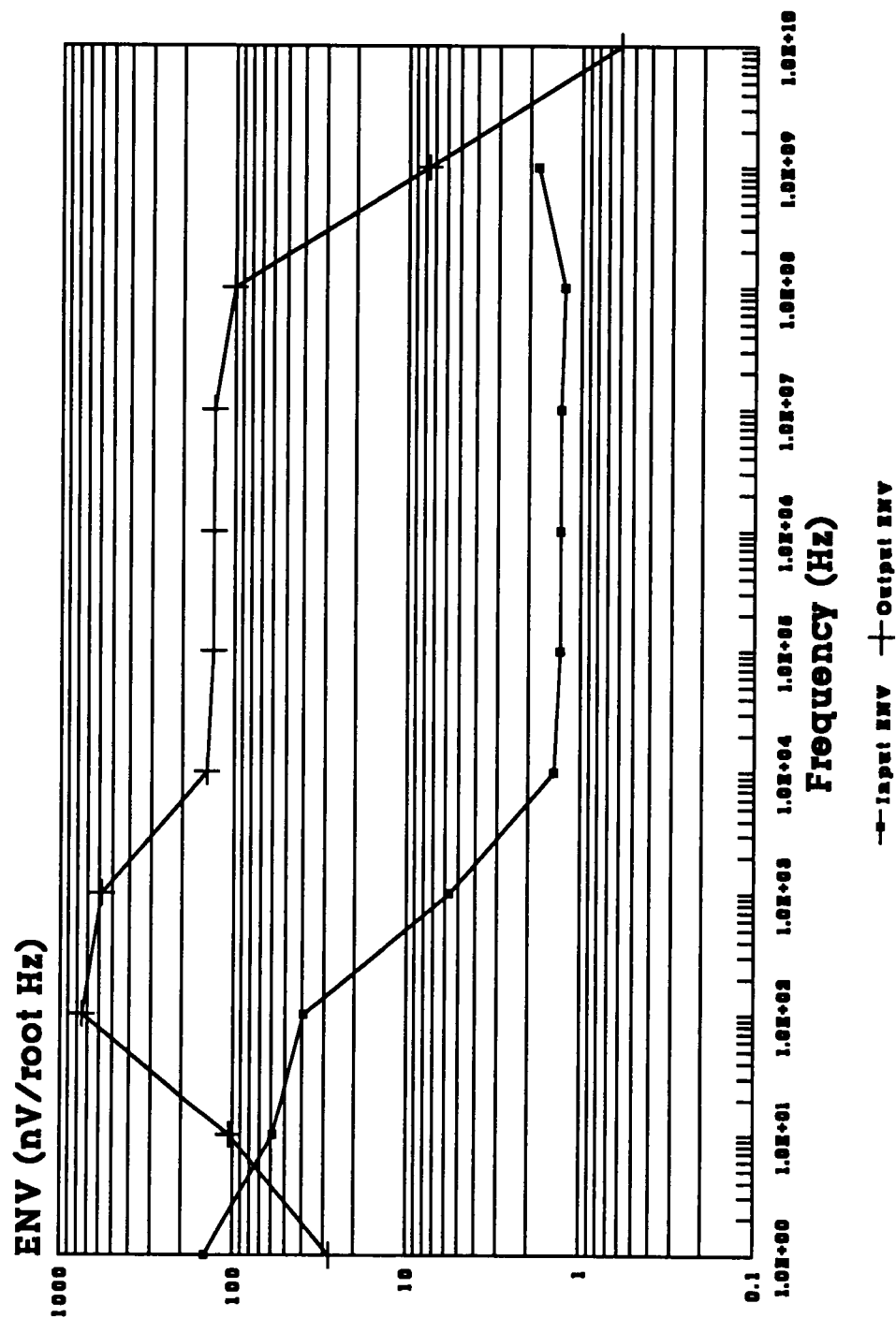


Figure 4-13. Input and output equivalent noise voltages predicted by PSpice.

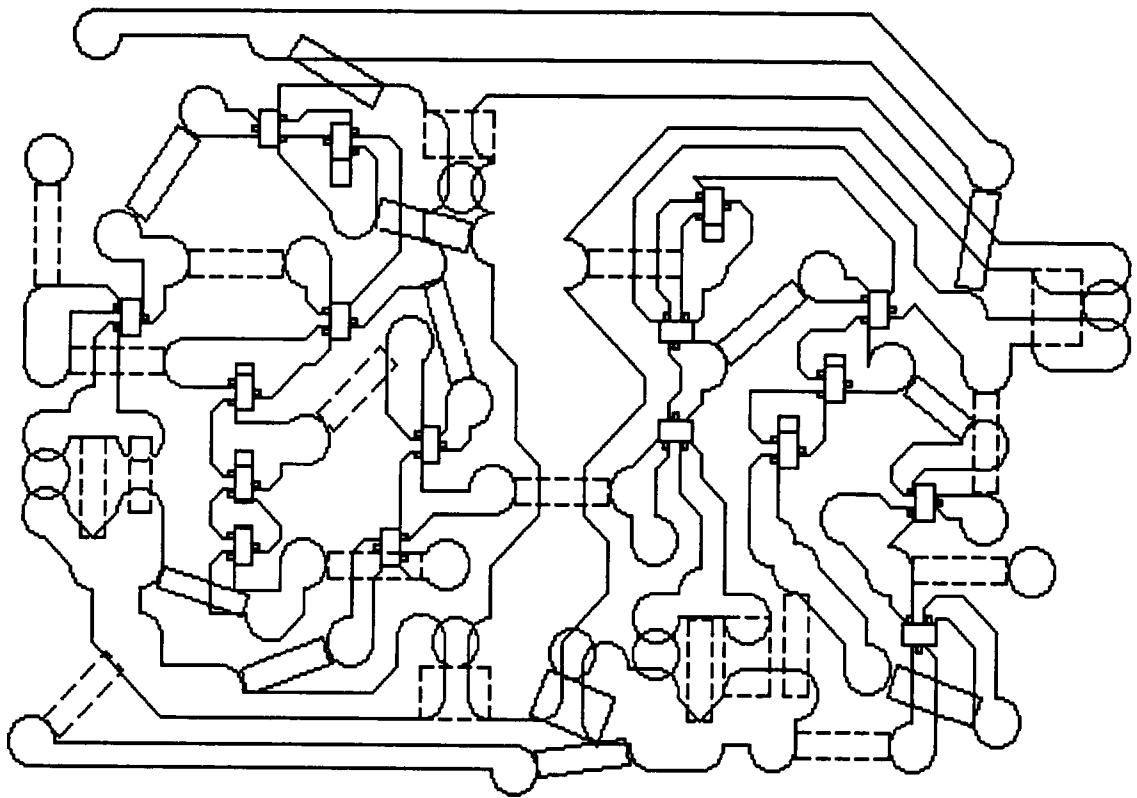


Figure 4-14. Printed circuit board layout.

current spikes would appear.

The "footprints", or models, used for the various components in planning the layout were determined as follows. The model for the surface mount transistors was taken from the data sheet for the 2SC3585 NEC, where the dimensions of the surface mount package were listed as 2.9 x 1.5 mm. One side of the transistor had two pads with the center of each pad located 0.5 mm from its respective end of the case, and the opposite side had a third pad centered along it. The pads extended out 0.65 mm from the body of the transistor. This footprint was then scaled so that 2 mm was equivalent to one side of a square on graph paper with five squares to the inch, yielding a scaling factor of about 2.5. This scale was very convenient in that the double-sided copper boards obtained for etching were approximately the length of one piece of paper (8.5 inches) when converted to this scale. The boards were 152 mm long and were cut to widths between 90 and 100 mm.

On this scale, a standard resistor was assigned pads two squares (4 mm) in diameter with centers six squares (12 mm) apart. The pads for a capacitor, also two squares in diameter, had centers that were usually four squares (8 mm) apart. Pads for ceramic disc capacitors were spaced five squares (10 mm) apart. The traces laid out were all at least one square (2 mm) wide and separated from other traces and pads by a minimum of 0.5 squares (1 mm).

The feedback path for the first stage was a loop through the elements R_{B2} , $Q2$, R_{F1} , and $Q1$, and these components were positioned such that the total length of the traces connecting them was only 16 squares (32 mm), minimizing the propagation delay for the feedback signal. The remainder of the first stage was laid out around the feedback path. The pads for the connections at the collector of $Q1$, from R_{C9} and R_{B2} , were positioned as close to each other as possible with a total area just over eight squares (32 mm²) to reduce the effects of stray capacitance at this critical node. The connections at the other end of resistors R_{C9} and R_{B2} were kept small for the same reason. The elements in series with the emitter of $Q1$, R_{E1} and the two C_{E1} capacitors, were positioned near $Q1$ to diminish any resistance or inductance at the emitter due to long traces which could quickly reduce the loop transmission. Since large capacitors often have poor high-frequency characteristics, a smaller capacitor was included in parallel with the large capacitors so that improving the low-frequency response with large capacitors did not compromise the wide bandwidth of the system or decrease its stability. This practice was employed in bypassing emitter resistors R_{E1} and R_{E10} as well as in bypassing the positive and negative power supplies for both the first and second stages.

The largest currents and fastest voltage swings in the first stage were anticipated through the elements R_{C6} , $Q6$,

Q7, and R_{C7} , so the bypass elements for the power supplies were positioned as close to R_{C6} , for the positive supply, and R_{C7} , for the negative supply, as possible. Long connecting traces between these components could generate parasitic capacitances coupling signals to the rest of the circuit.

The second stage layout was very similar to that of the first stage. The feedback path, through R_{B11} , Q11, Q12, Q13, R_{F2} , and Q10, was slightly longer than the one in the first stage, measuring eighteen squares (36 mm), and had the extra propagation delay associated with two diode-connected transistors.

The major difference between the layout of the first and second stages was that the second stage did not allow for the addition of R_{C17} , the second-stage equivalent of R_{C9} in the first stage. At the time the layout was designed, both resistors were thought unnecessary but it seemed R_{C9} would be more likely to be needed so a space was left for it. As a result, the pad associated with the collector of Q10 had an area less than 5.5 squares (22 mm²), which would result in very little stray capacitance.

Another difference between the two stages was the way the feedback resistor was connected. In the second stage, pads were included so that R_{F2} could be connected from the base of Q10 to either R_{E13} or R_{S3} at the output. The connection to R_{S3} was provided so that the output transistors

could be stabilized by the feedback loop in case linearity became a problem.

As with the first stage, an attempt was made to bypass the power supplies as close as possible to resistors R_{C14} and R_{C15} to prevent any large voltage swings from being transmitted to the rest of the circuit.

CHAPTER 5

EXPERIMENTAL RESULTS

Introduction

Without a doubt, the most difficult aspect of this project was designing a viable layout of the circuit. In order to avoid high-frequency oscillations, assistance was gleaned from experienced designers, usually in the form of procedures that were not generally accepted. This chapter summarizes techniques employed in the implementation of a stable high-frequency amplifier and includes performance characteristics for the amplifier and techniques used to measure them. The complete circuit diagram is included in Figures 5-1 and 5-2.

Printed Circuit Board Fabrication

A double-sided copper board was used to make the printed circuit (PC) board. The boards used measured 6" x 3.5-4". The width varied slightly since the boards were cut from a larger board. The layout was photocopied and reduced to 40% of its original size. Carbon paper was used to

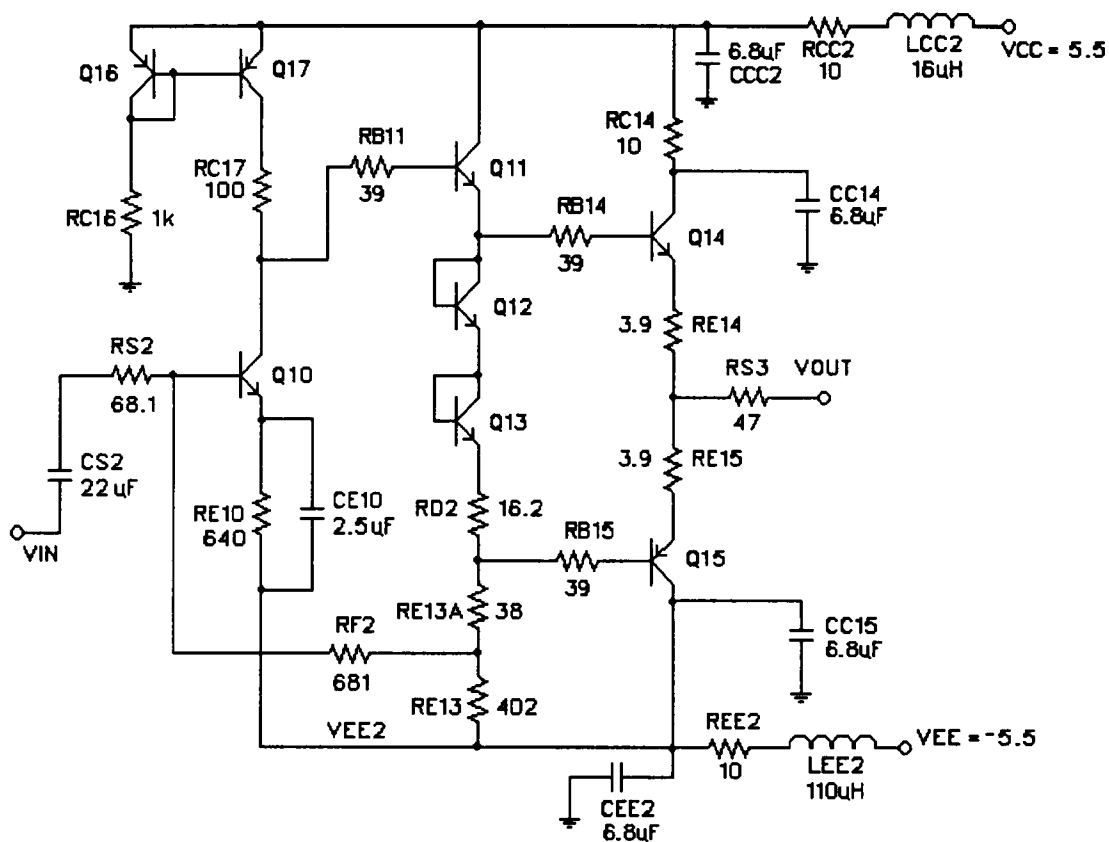


Figure 5-2. Complete second stage circuit schematic.

transfer the layout to the board, and the complete layout was traced with a resist ink pen. The reverse side of the board was completely coated with resist ink in order to leave a ground plane on the component side of the board. Next the board was immersed in a PCB (printed circuit board) etchant solution of ferric chloride until etched and then rinsed. The resist ink was removed with isopropyl alcohol.

This method of producing a PC board is very inexpensive but has certain drawbacks. The resist ink pen did not have a fine point, so the placement of the lines and pads on the board was inconsistent and the layout was not produced precisely. The results, however, were adequate for this project. Also, the resist ink did not seal out the etchant completely. Since all of the traces and pads in the layout were wider than the resist pen, resist lines were laid down side by side to form the traces, and in a circular pattern to form the pads. Although no gaps were observable to the naked eye, after etching, the surface of the remaining copper appeared rough in spots, especially on some of the pads. Examination under a microscope revealed pitting in the copper, apparently from etchant that leaked through the resist ink. Experimentation revealed that two or three coats of resist ink applied in a smooth (i.e. long lines) pattern with an etching time of approximately twenty minutes minimized the pitting effects. The pitting is likely to increase the resistivity of the copper traces and perhaps

affect stray inductance and capacitance, but these effects were not modelled and the results appeared satisfactory for this application.

After etching the board, holes were drilled for the component leads and a Dremel tool was used to grind away a region (roughly 1 cm in diameter) around these holes on the component side of the board. On the first prototype boards these regions were etched away but drawing around these regions with the resist pen resulted in increased pitting of the ground plane, especially close to the etched regions. In addition to increasing the resistivity of the ground plane, the pitting hindered soldering to the ground plane in some areas. Therefore, on the final board the regions were ground away instead of etched.

Circuit Enclosure and Connections

An enclosure was needed to minimize the pickup of external signals by the amplifier. Since the circuit board was double-sided, it was necessary to purchase an aluminum box (no source for copper boxes was found), which had removable panels on two sides, providing easy access so that once mounted, the circuit would not be removed from and returned to the box repeatedly. Although boxes came in several sizes, the box closest to the size of the circuit board

measured four inches by five inches by six inches. The box length matched the length of the board well, but the box width left about an inch of space on either side of the circuit board, with approximately two inches of open space above and below the board.

The board was mounted to the box using two L-shaped brass brackets, which were secured by screws to both the circuit board and the box, although later it was determined that the circuit performed optimally when the bracket was not screwed into the box at the input end. An insulated BNC connector was employed to bring the input signal to the circuit through a hole drilled in one end of the box, and an uninsulated BNC connector was used in the same manner for the output signal. The input signal was taken from the insulated BNC connector to R_{S1} by means of a one-and-a-half inch piece of RG-132 cable to keep any pickup from being fed directly into the input. One end of the ground shield from the cable was soldered to the ground lug from the insulated BNC and the other was connected to the ground plane at the same place where R_1 was attached to it. To provide an even sturdier tie to ground, the ground lug was also connected to the ground plane with an inch-long piece of 14-gauge wire.

The ground lug for the output connector was soldered directly to the ground plane on the top (component side) of the board. The signal was taken to the output BNC by soldering R_{S3} from its connection with R_{E6} and R_{E7} straight to

the output connector instead of to the pad provided on the layout. The resistor leads were left about an inch and a half long in order to connect the resistor in this manner, which could be subject to pickup and would increase the inductance in series with the output, but no desirable alternatives were discovered.

Separate power and ground wires were used for the first and second stages to diminish the possibility of high frequency signals travelling from the output back to input by means of the power lines. These wires ran out of the box through two separate holes drilled in its side. All six power lines (two positive power lines, two negative, and two ground lines) were multi-stranded. The positive line to the first stage was twelve inches long, while the one to the second stage was slightly over eight inches long. The negative supply line to the first stage was about seven inches long, the one to the second stage ten inches long. Both ground lines were roughly seven inches long.

When attaching the power and ground lines to the circuit board, an attempt was made to find the optimum connection point. The lines were touched to the board in various places and the point producing the least oscillation at the output was selected for connection. The first stage ground lead was attached to the ground plane on the top (component side) of the board near the capacitors for the negative power supply, and the ground lead for the second stage was

connected to the bottom (solder side) of the board immediately under the ground lug for the output BNC connector. The negative power bus on the circuit board offered few options for connecting the negative power supply leads, so the leads were soldered directly to the bus. The positive power supply leads were soldered to the positive power bus, with the first stage lead soldered as close to the input as possible and the second stage lead soldered as close to the output as possible.

Layout Modifications

Several modifications were needed after the printed circuit board had been etched, and instead of etching a new board each time a revision was needed, the changes were implemented by cutting traces, rearranging parts, or some similar technique.

The first alterations to the layout were made necessary by biasing problems. It was hoped that the previously-discussed measures designed to deal with thermal runaway would be unnecessary, but initial testing showed unacceptably high currents in the output drivers of both stages. In an attempt to more accurately match the junction voltages of Q4 and Q5 to Q6 and Q7, a PNP transistor was substituted for Q5 so that both the Q4-Q5 pair and the Q6-Q7 pair contained

one NPN and one PNP transistor. Since the PNP transistor had a different pinout than the NPN for which the layout was designed, the emitter tab was soldered to the pad where the base and collector of the NPN had been, and the base and collector tabs were both soldered to the pad where R_{B7} was attached.

The components R_{D1} , R_{E6} , and R_{E7} (Figure 5-1) were added as an additional means of controlling the thermal runaway. In order to include R_{D1} in the circuit, the pad connecting the emitter of Q4 and the emitter of Q5 was cut, leaving a space one or two millimeters wide. One lead of R_{D1} was bent to run along the body of the resistor so that both leads ended up at the same end of the resistor only a few millimeters apart. The resistor then stood straight up off the board when soldered across the small gap between Q4 and Q5.

The traces connecting the pads for the emitters of Q6 and Q7 to R_{S2} were cut in a similar fashion and R_{E6} and R_{E7} were soldered across these gaps. R_{E14} and R_{E15} were soldered across corresponding gaps created in the output of the second stage, and R_{D2} was attached from the emitter pad of Q13 to the pad for R_{F2} .

Another alteration was required when it was discovered that the layout had been designed so that the emitter and collector instead of the base and collector of Q16 were connected together. To remedy this problem, the emitter tab of Q16 was soldered to the emitter pad of Q17, and the base

and collector tabs for Q16 were soldered to the base pad of Q17. At first this was done in the original location for Q16 (approximately 11 mm from Q17) but the collector currents observed in Q16 and Q17 were poorly matched. When Q16 was moved closer to Q17 (about 2 mm away) to improve the thermal coupling between the two, the collector currents were much more comparable.

To incorporate R_{C17} (which was not originally included in the layout) into the circuit, a cut was made between the collector pad for Q17 and the pad for R_{B11} and R_{C17} was soldered across this gap. The proximity of Q17 to R_{B11} made this task difficult, but it was necessary for the minimization of stray capacitance at this important node.

C_{S2} was another element not included in the initial design and thus omitted from the layout. One lead of resistor R_{S2} was pulled from its hole and soldered to one side of C_{S2} . The other side of C_{S2} was put into the hole abandoned by R_{S2} .

A similar adjustment was made to allow for R_{E13A} , which, like C_{S2} , was not in the original design and layout. To connect the ends of R_{F2} and R_{E13} , the ends were pulled from the circuit board and soldered to each other and to one end of R_{E13A} just above the board. The other end of R_{E13A} was then soldered into the hole originally intended for R_{E13} . This arrangement resulted in a "tepee" of resistors protruding from the board, which increased the possibility of unwanted

pickup and transmission, but it appeared to be the best solution short of etching another board.

A further modification to the circuit board involved drilling holes from the ground plane on one side of the board to the ground plane on the opposite side and soldering pins from one side through the holes to the other. Three of these holes (excluding the hole for the mounting screw) were located at the edge of the board closest to the output connector and two others connected the top and bottom of the board at the input end. In the middle of the board this connection was accomplished through several of the bypass capacitors that were soldered to ground on both sides of the board.

In addition to using separate power lines for the first and second stages, the positive and negative power buses were cut on the printed circuit board to further isolate the two stages and prevent relatively large fluctuations on the power lines for the output stage from being transmitted back to the input stage where they could cause large oscillations. Similarly, the ground plane was cut on both the top and bottom of the board so that any currents flowing in the ground plane for the second stage would not disturb the first stage.

Circuit Stabilization and Troubleshooting

Since there were many components extending out of the board on both sides, some degree of shielding was necessary to prevent any pickup in the first stage of signals transmitted by the second stage and vice versa. The double-sided copper board used to make the PC board was cut into pieces to be used as shields. On the bottom, or solder side, of the board a portion of the ground plane runs almost completely across the board between the first and second stages of the amplifier. One of the copper shields was soldered to this part of the ground plane, which was the ground plane used for the first stage of the amplifier. Ideally, the shield would extend all the way from one side of the box to the other and up to the removable panel, completely shielding one stage from the other. This shield came within five millimeters of each side and within about ten millimeters of the panel across the bottom of the box. Since the ground plane did not extend completely across the board, a notch was required in the shielding plate so that the power buses were not shorted out. All of these gaps and openings were bothersome, as each presented the potential for signals to be transmitted from one stage to the other.

Shielding on the top, or component side, of the board was more complicated since there were many more elements filling the space above the board. R_{s2} and C_{s2} connected the

first and second stages, so putting a single shield across the board was impossible. To isolate the first stage from the second stage, two shields, each reaching halfway across the box, were soldered to the top of the board. A small gap was left between them for R_{S2} and C_{S2} to connect the first stage to the second. Larger gaps, one of them over fifteen millimeters, were left between these shields and the sides and top of the box, but since the ground plane extended completely across this side of the board no notches were required in these shields. The ground plane to which these shields were connected was the first-stage ground plane. In order to further shield the output stage from the input, shields were soldered along the edges of the circuit board, parallel to the sides of the box. These shields were both soldered to the second stage ground plane and came to within roughly one centimeter of the other shields and the end of the box. The overall effect of these shields was to create a smaller copper box around the output stage of the amplifier roughly three inches by three inches. However, with the top open the circuit was extremely sensitive to movement of things such as hands or the aluminum panel over the output of the circuit, so a strip of copper about an inch wide was soldered across the two side shields so that it covered the components associated with the output driver, namely R_{B14} , R_{B15} , R_{C14} , R_{C15} , and R_{S3} . The result was that the circuit

became much more stable against objects moving in the vicinity of the output circuitry.

Several times while working on the circuit it was discovered that overshoot and oscillations on the output pulse were there because the input pulse had overshoot and oscillations. The pulse generator delivered a clean pulse when it was not loaded down, so apparently the input of the amplifier was improperly terminated. To prevent the input impedance from becoming large at high frequencies, R_1 (Figure 5-1) was positioned in parallel with the input, setting a maximum value for the input impedance.

One of the most useful mechanisms for ridding the circuit of oscillations was the use of bypass capacitors. These capacitors were employed in several places throughout the circuit as described below. To decrease the nonlinearities associated with the diodes Q4, Q5, Q12, and Q13 in the circuit, a $0.001 \mu\text{F}$ capacitor was connected across Q4, Q5, and R_{D1} and another was connected across Q12, Q13, and R_{D2} in the second stage. The diodes were included for biasing purposes, but as the current flowing through them changed, their resistances (r_c 's) would also change (inversely with current) and thus produce a variable gain. With the capacitor connected across them, the diodes and resistor were shorted above a certain frequency determined by the product of the capacitor and the sum of R_{Dn} and the r_c 's of the

diodes. This frequency was approximately 8 MHz for both stages.

Perhaps the most important bypassing done was with the capacitors connected to the collectors of the driver transistors, Q6, Q7, Q14, and Q15. These transistors experienced the largest voltage swings and current fluctuations of any transistors in their respective stages, so proper bypassing of these devices was crucial to the success of the circuit. For fast signals, all of the high frequency current needed by the transistors would ideally be supplied by the bypass capacitors. To facilitate this procedure the capacitors had to be positioned to provide the shortest possible return path for these high frequency signals. In the output stage, one end of the capacitor was soldered directly to the lead of the collector resistor, either R_{C14} or R_{C15} , and the other end was soldered to the ground plane as close as possible to the ground lug of the output connector. The high frequency signals then had to pass through a loop consisting only of the bypass capacitor, driver transistor, emitter resistor, and R_{S3} on the circuit board. The loop consisting of C_{C14} , Q14, R_{E14} , and R_{S3} covered a distance of only about two inches on the circuit board, but due to the placement of R_{C15} the loop containing C_{C15} , Q15, R_{E15} , and R_{S3} covered a distance closer to four and a half or five inches on the board. These distances do not include any transit delays incurred in the output connector cable and any at-

tached electronics. For the input stage it was not as easy to find the optimum point of connection since fast signals would pull current through R_{S2} and R_{F2} , including these elements in its path to ground. One bypass capacitor was soldered to R_{C7} and then to the ground plane right next to R_{C7} , which was also where the ground lead from the power supply to the first stage was connected. The other capacitor was soldered from the lead of R_{C6} to the ground plane beside it. This point was next to where the shield between the first and second stages was soldered down, so it provided a solid ground.

A $0.001 \mu F$ capacitor was also connected across the base-emitter junctions of Q16 and Q17, which formed the current source for the second stage. This capacitor's purpose was to hold the base-emitter voltages constant so that the current source would provide a stable DC current. Any variations in the current through these transistors would pass through R_{C17} and show up as voltage change at the collector of Q10. This voltage change would then be passed straight to the output.

Although the layout was first designed so that C_{E1} and C_{E10} would be connected across R_{E1} and R_{E10} , respectively, this scheme tended to be subject to oscillations. When these capacitors were connected from the emitters of the transistors to the ground planes, the amplifier was much less likely to oscillate. The reason was probably that any fast sig-

nals at the output would cause ripples on the negative supply lines, and these ripples would be passed directly to transistors Q1 and Q10 through C_{E1} and C_{E10} , respectively. As previously discussed, connecting the emitter capacitors to the ground plane near the input of each stage, and thus near the input transistor and its emitter resistor, had much the same effect as creating the smallest possible loop with the collector bypass capacitors at the output of each stage.

While working with the amplifier any physical movement of the lines from the power supply to the box could either encourage or suppress oscillations at the output. Any AC current flowing in the power lines was detrimental since it must have flowed through the decoupling resistor in series with the power line and produced oscillations that would then be transferred to the input of the amplifier. To alleviate this problem inductance was added, in series with the decoupling resistors, to all of the power lines. The negative supply lines showed the greatest sensitivity to being moved, so each one was wrapped around a toroid almost 2.5 centimeters in diameter. Four turns around the toroid for the negative supply to the first stage produced a measured inductance of $75 \mu\text{H}$, and for the second stage five turns yielded an inductance of $110 \mu\text{H}$. The toroids were located inside the box and as close to the circuit as possible so that any inductance or capacitance between other power lines outside the box would be neutralized. The inductors used

for the positive power leads and the ground wires consisted of ferrite cylinders with two and one half turns of wire threaded through them and had measured values between 15 and 20 μH .

A curious technique for fighting parasitic oscillations was employed when the circuit was built up initially and each stage was being tested separately. Oscillations were often present at the output of each stage and several different methods were used to combat their effect, usually touching different points in the circuit with a finger or attaching bypass capacitors in various locations. One of the most effective means of alleviating the oscillations was to touch the collector of either Q1 or Q10, depending on which stage was being worked on, with the lead of a wooden pencil. Touching the pencil to the collector of the input transistor would typically decrease the amplitude of the oscillations at the output of that stage by at least an order of magnitude. Further investigation showed that touching the pencil to other nodes in the circuit had little effect on the oscillations. Several possible substitutions for the pencil were examined with varying success. Adding any capacitance to the collector of the input transistor eliminated the oscillations at the expense of circuit bandwidth, which the pencil had not compromised. The best alternative found was a wire soldered to either R_{C9} or R_{B2} (R_{B11} for the second stage) and trimmed to the proper length.

This trimming was done by measuring the frequency of the oscillations observed at the output and calculating the value of one quarter wavelength of a signal of this frequency. The stub was cut slightly longer than this calculated value and then trimmed little by little until the oscillations disappeared. The reason for the success of this technique was not immediately apparent. When a signal appeared at one end of the stub, the stub looked like a transmission line. When the signal reached the end of the stub, it encountered an open circuit that reflected the signal back. When the signal reached the other end, it added to the signal at the collector of Q1 (or Q10). For this effect to cancel out oscillations it was necessary for the signal at the initial end of the stub to have changed 180 degrees by the time the reflection returned. 180 degrees corresponds to half of a wavelength so if the signal traversed a quarter-wavelength stub twice, the signal at the initial end would have changed 180 degrees and the two would cancel each other out.

Some drawbacks to this technique were that the stub could serve as an antenna sending signals straight into the collector of Q1 or Q10 where they would be passed to the output, and that when the circuit was moved or the stub itself was touched, the stub would vibrate back and forth for a few seconds causing oscillations at the output, which were probably also due to pickup in the stub. This problem

was addressed by using coaxial cable, which shielded the stubs so that pickup was not a hindrance, for the stubs instead of bare wires. Using a coaxial cable raised the issue of adding capacitance at this critical node, since capacitance between the stub and its ground shield would adversely affect circuit bandwidth. A compromise was made for the second stage stub by using RG-58 cable, which was stiffer and more difficult to work with than the RG-132 used in the first stage, since the RG-58 cable had less capacitance per foot than the narrower RG-132 cable. The capacitance added to the second stage had more potential for damage since the signals at the collector of Q10 would be ten times as large as those at the collector of Q1 and would require much more current to drive the same capacitance.

Experimental Data

Since the amplifier was designed to amplify fast pulses, much of the data collected related to the pulse response of the amplifier. For example, the rise and fall times for both positive and negative pulses were well-characterized, as shown in Figures 5-3 and 5-4, respectively. The rise times were measured from the time the pulse reached 10% of its final height to the time it reached 90% of its final height, and the fall times were a 90% to 10% measurement.

Positive Pulse Rise and Fall Times

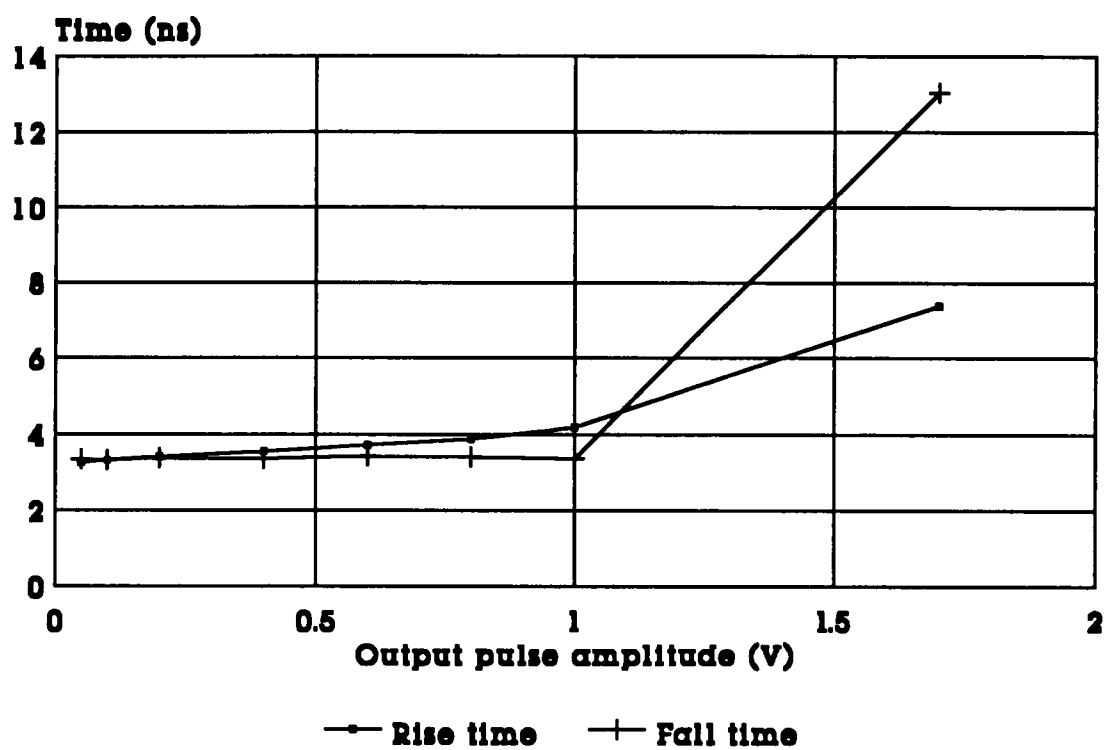


Figure 5-3. Rise and fall time data for positive pulses.

Negative Pulse Rise and Fall Times

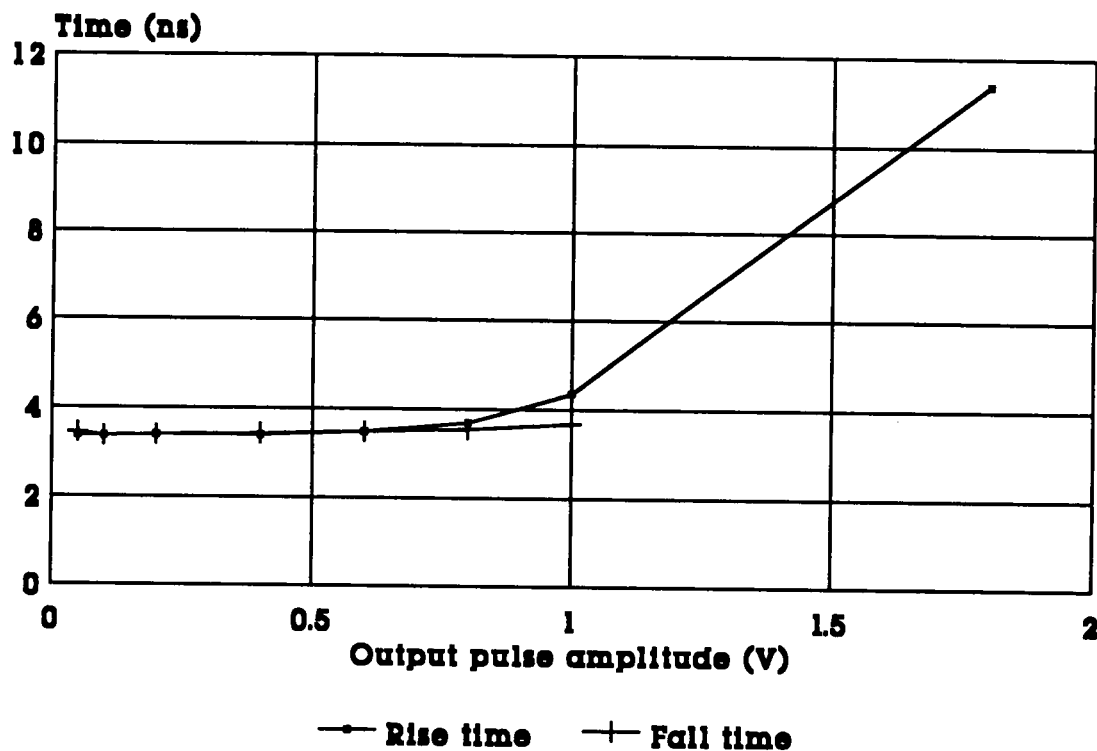


Figure 5-4. Rise and fall time data for negative pulses.

Positive Pulse Overshoot

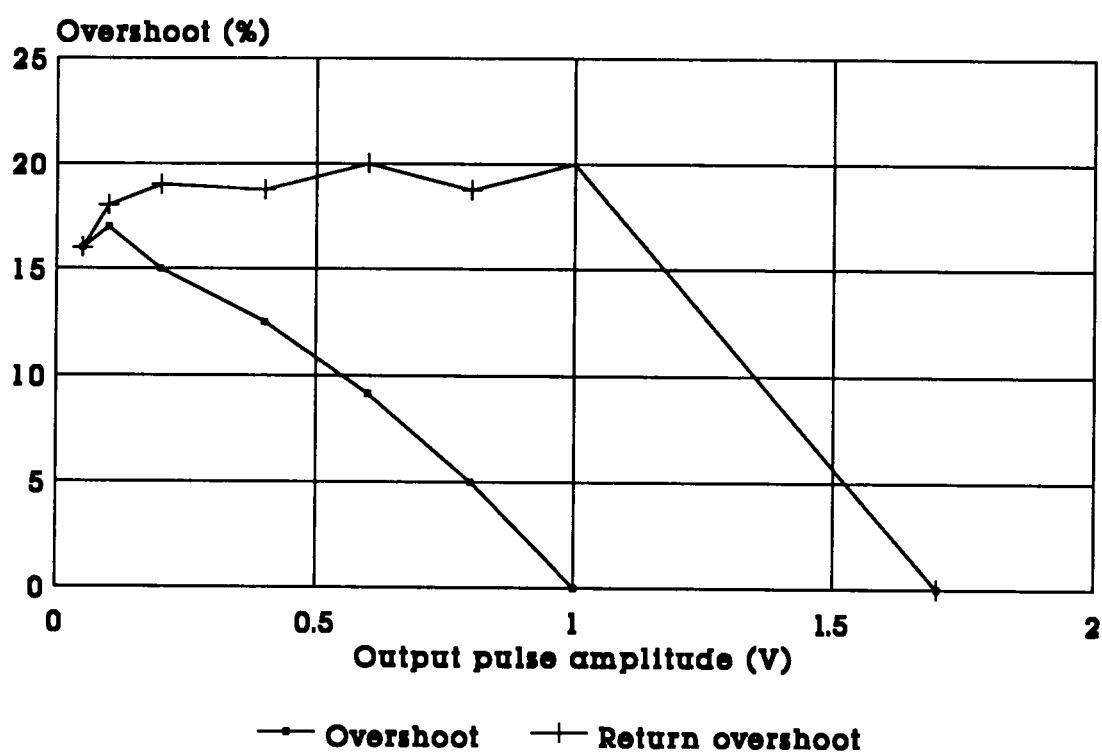


Figure 5-5. Overshoot data for positive pulses.

Negative Pulse Overshoot

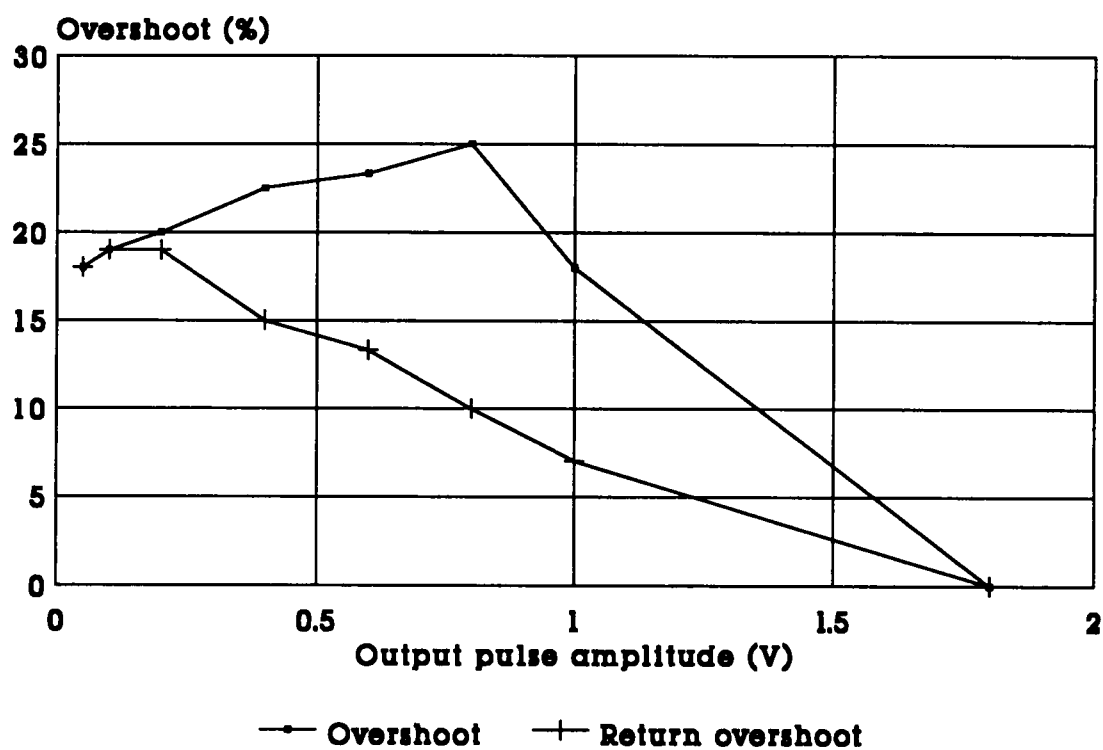


Figure 5-6. Overshoot data for negative pulses.

The overshoot results for both positive and negative pulses are included in Figures 5-5 and 5-6. The overshoot was measured as a percent of the final pulse height, and the return overshoot was measured on the falling edge of the pulse. Data were taken for these characteristics up to the 1 Volt drive specification into 50 Ω , as well as one data point at the maximum output pulse height that the amplifier could drive in either direction, which was 1.7 Volts for a positive pulse and 1.8 Volts for a negative pulse. Even though the amplifier was capable of driving farther than its limit of ± 1 Volt into 50 Ω , Figures 5-3 and 5-4 make it obvious that the circuit did not meet its specifications when driving an output pulse larger than 1 Volt. As a matter of fact, the fall time for a 1.8 Volt negative pulse was 71.9 ns, so large that it could not be included in the plot with the rest of the values and still retain any useful scale. Equation 4.7 predicts that with a 50 Ω output resistance and a 50 Ω load, any positive output pulse larger than 1.0 Volt would push the amplifier into a region of nonlinear operation, and Equation 4.9 determines that the amplifier could not drive below -1.4 Volts (into 50 Ω).

To visualize the performance of the amplifier more accurately, several pictures were taken of the output pulses. Figure 5-7 shows a positive output pulse at the full dynamic range, 1 Volt. This pulse had negligible overshoot, probably since transistor Q10 was running out of drive

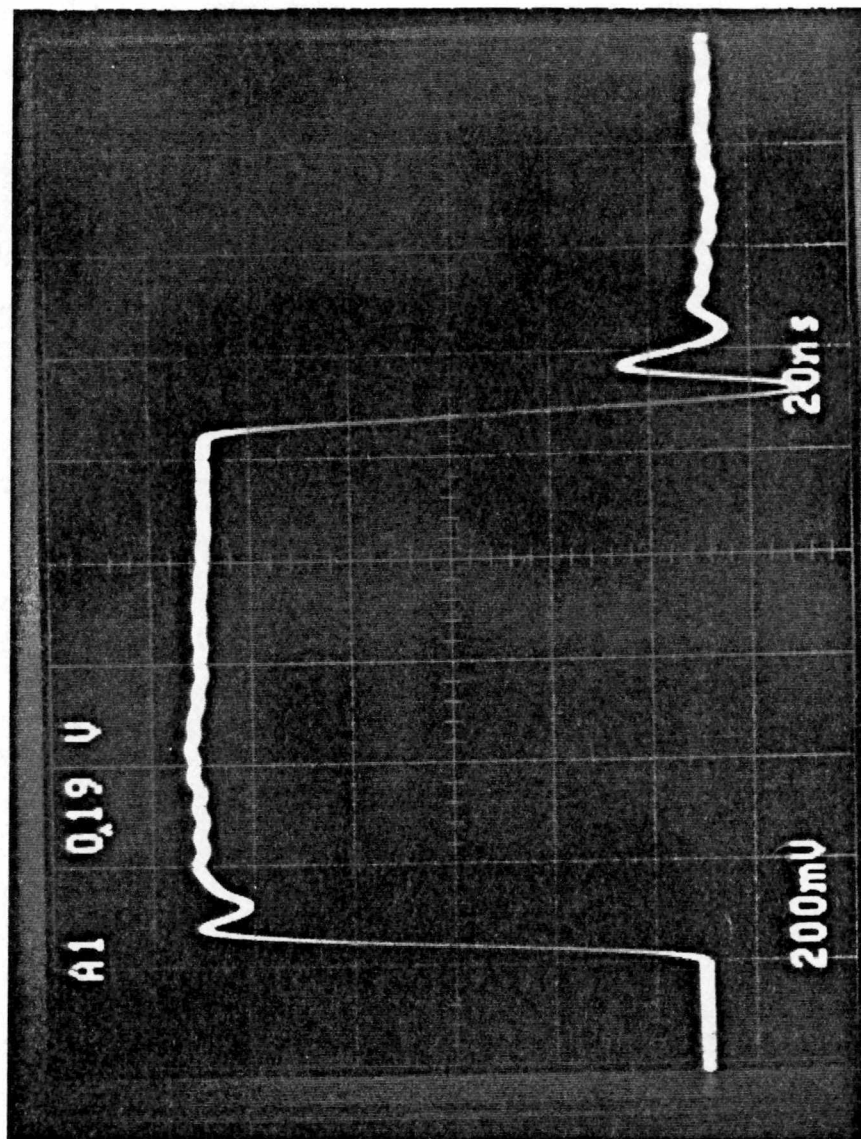


Figure 5-7. Positive 1-Volt output pulse.

current as its collector approached the positive rail. It did have 8 or 9% undershoot before settling to its final value, and the shape of the pulse was not as smooth as might be expected. Apparently the input impedance of the amplifier did not look like 50 Ω at very high frequencies, and this termination mismatch altered the shape of the input pulse, which translated to a misshapen output pulse as well.

Figure 5-8 shows the same pulse with the time scale expanded to show the rise time of the pulse, which was 4.34 ns.

A negative pulse at the full dynamic range of the output is depicted in Figure 5-9 and its rise time, 4.52 ns, is shown in Figure 5-10. This pulse had 20% overshoot and 15% undershoot.

Another set of pictures was taken well inside the dynamic range of the amplifier, where the output voltage was 500 mV. These pulses were more typical of the operation of the amplifier. Figure 5-11 shows a positive pulse with an amplitude of 500 mV. Its overshoot was approximately 13% and its undershoot was 14%. The rise time, pictured in Figure 5-12, was 3.50 ns. A negative 500 mV pulse is shown in Figure 5-13 with a 22% overshoot and 20% undershoot. Figure 5-14 reveals a rise time of 3.38 ns for the negative pulse. The larger overshoots and undershoots for negative pulses were due to the larger collector current flowing in Q10 for a negative output. The larger current was able to charge any capacitance at the collector quickly, yielding a

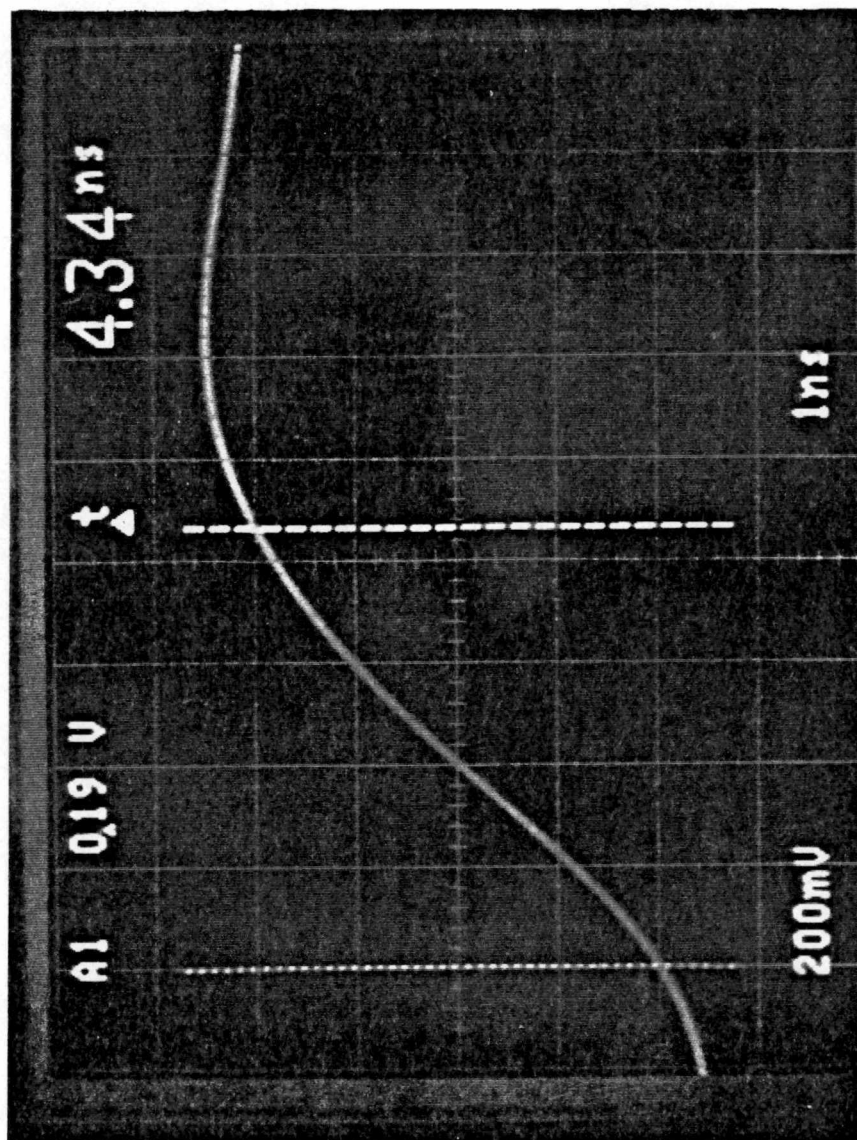


Figure 5-8. Rise time for positive 1-Volt pulse.

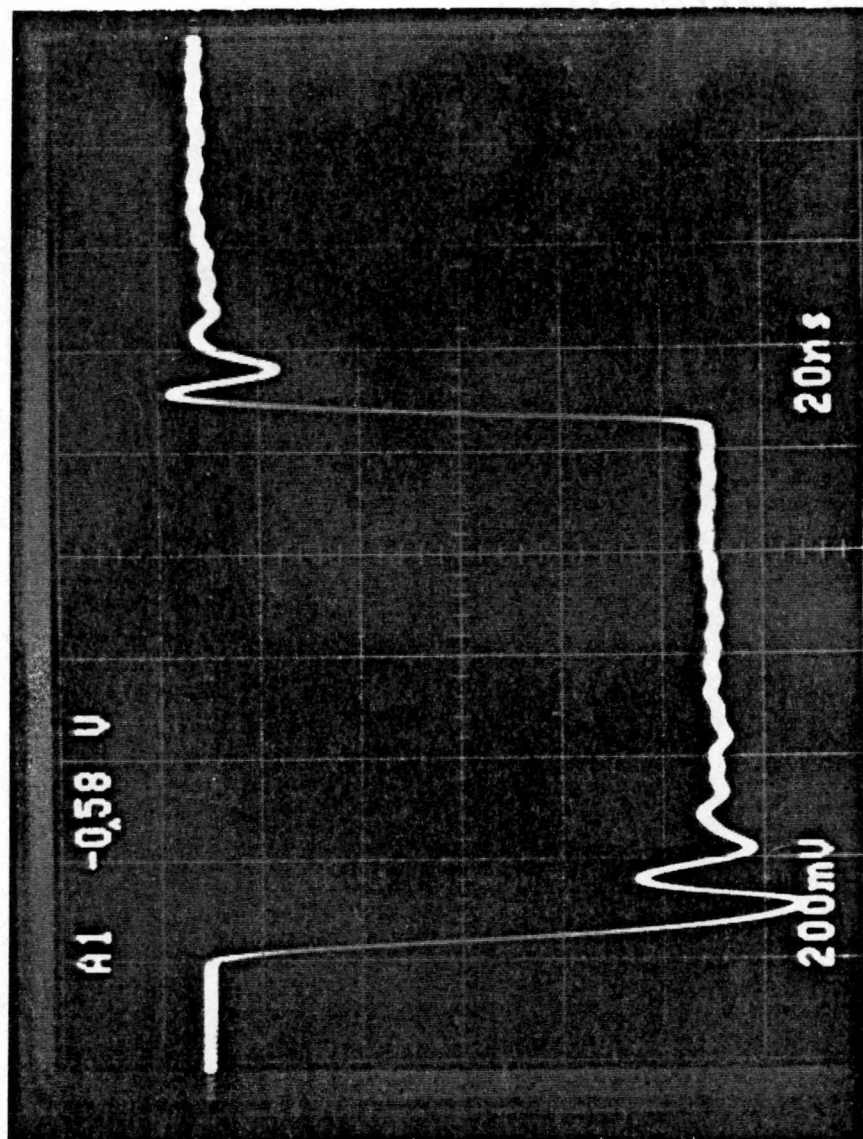


Figure 5-9. Negative 1-Volt output pulse.

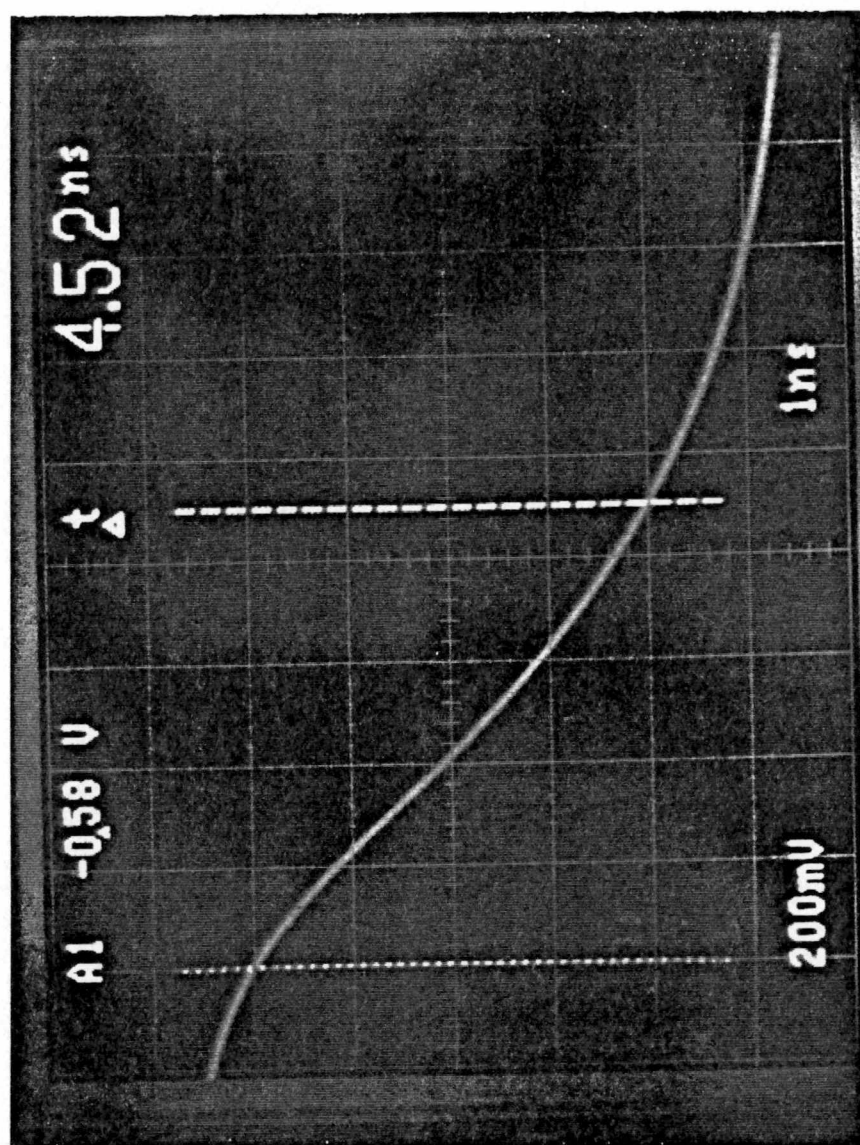


Figure 5-10. Rise time for negative 1-Volt pulse.

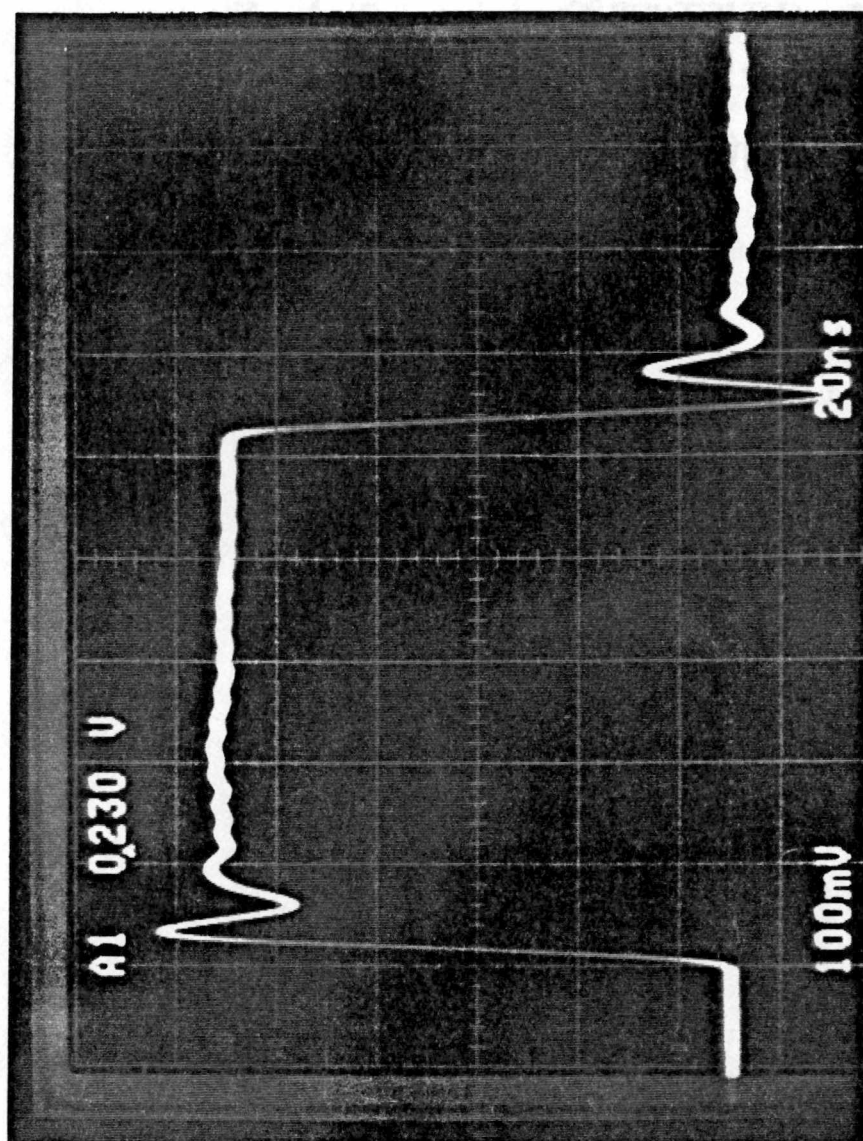


Figure 5-11. Positive 500 mV pulse.

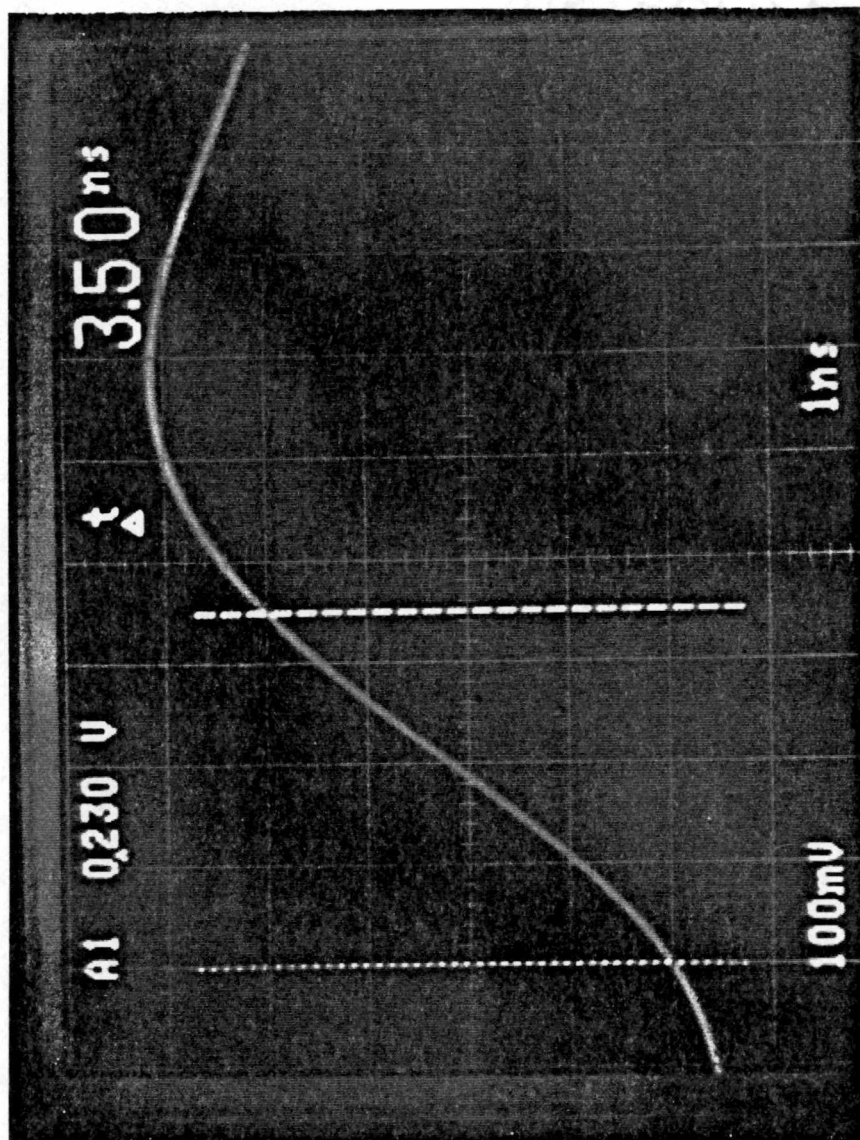


Figure 5-12. Rise time for positive 500 mV pulse.

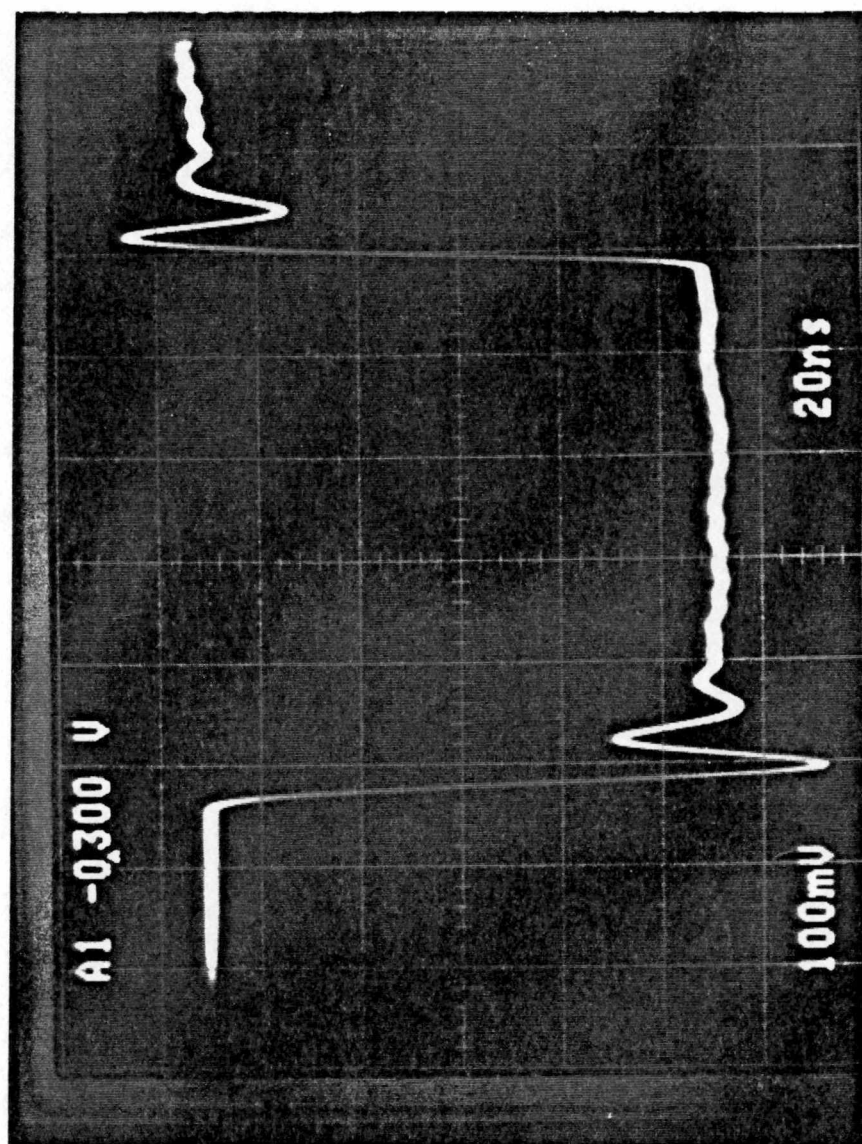


Figure 5-13. Negative 500 mV pulse.

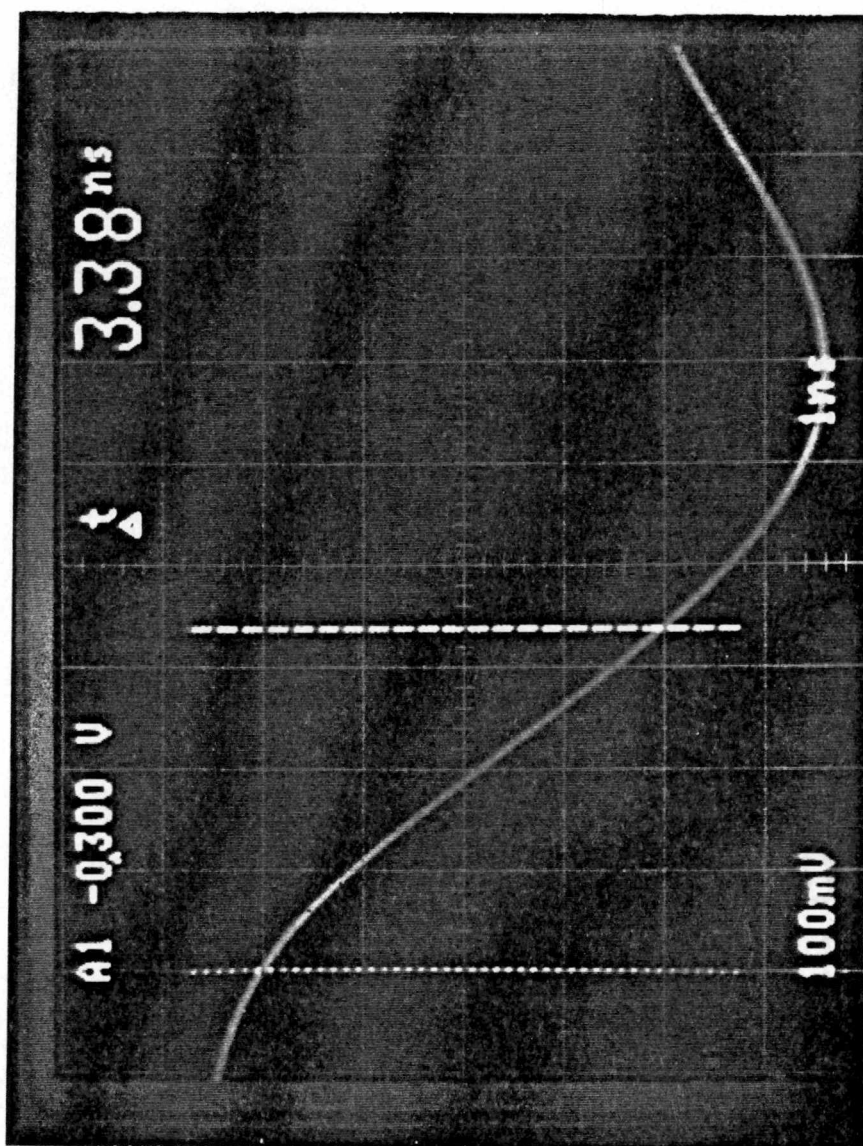


Figure 5-14. Rise time for negative 500 mV pulse.

reduced rise time but larger overshoot.

Positive and negative small-signal pulses are displayed in Figures 5-15 and 5-16, respectively. These pulses had an amplitude of 50 mV and rise times under 4 ns. The overshoots were 28% for the positive pulse and 15% for the negative pulse. The 10 mV/division scale for these photographs showed the noise level at the output, which was about 4 mV peak to peak.

Figure 5-17 shows one method of determining the impulse response of the circuit. The input pulse was made as narrow as possible while maintaining the full amplitude of the output pulse. The input pulse width was around 6.25 ns, as any narrower pulse would cause the output pulse to begin decreasing before it reached its maximum height.

Data were also collected to characterize the frequency response of the amplifier. These data are plotted in Figure 5-18, which shows a transfer function with a midband value of about 49.5 and a bandwidth between 115 and 120 MHz. The low-frequency cutoff was at approximately 130 Hz. The midband value of the voltage gain was close to 50, not 100, since the measurement was made across the 50 Ω load. At around 80 MHz there was also a peak that is not seen in the calculated plot of Figure 4-10. The calculated gain of 52.8 (half of 105.5) was a little higher than the experimental gain, but the actual bandwidth was higher than expected, 115 MHz when 80 MHz was predicted, so the system gain-bandwidth

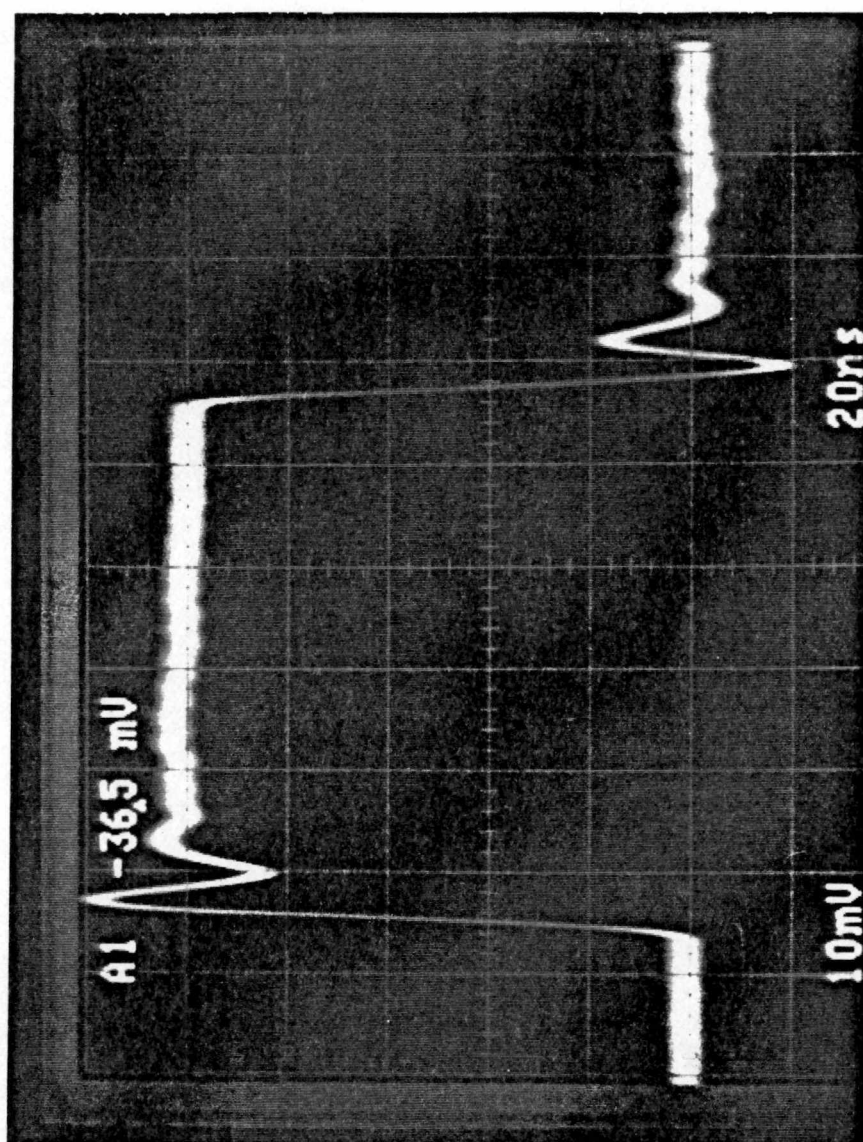


Figure 5-15. Positive 50 mV pulse.

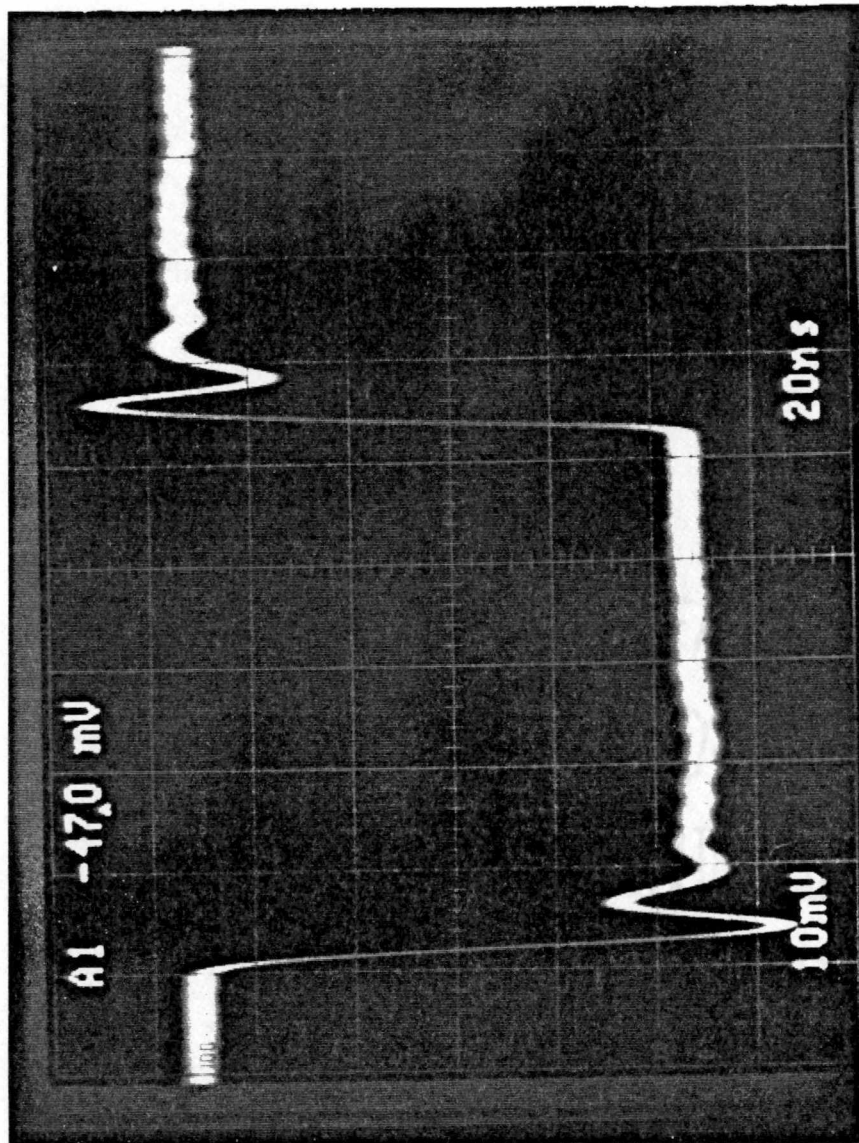


Figure 5-16. Negative 50 mV pulse.

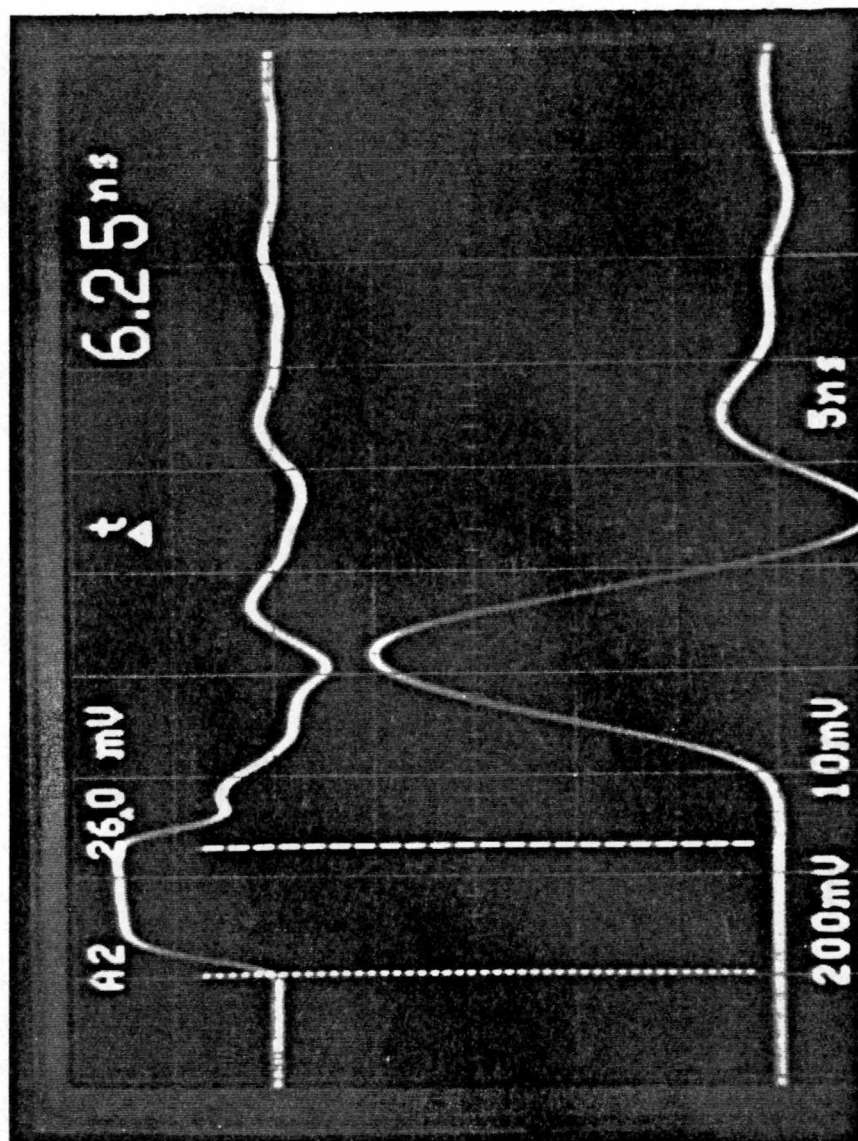


Figure 5-17. Circuit impulse response.

Frequency Response

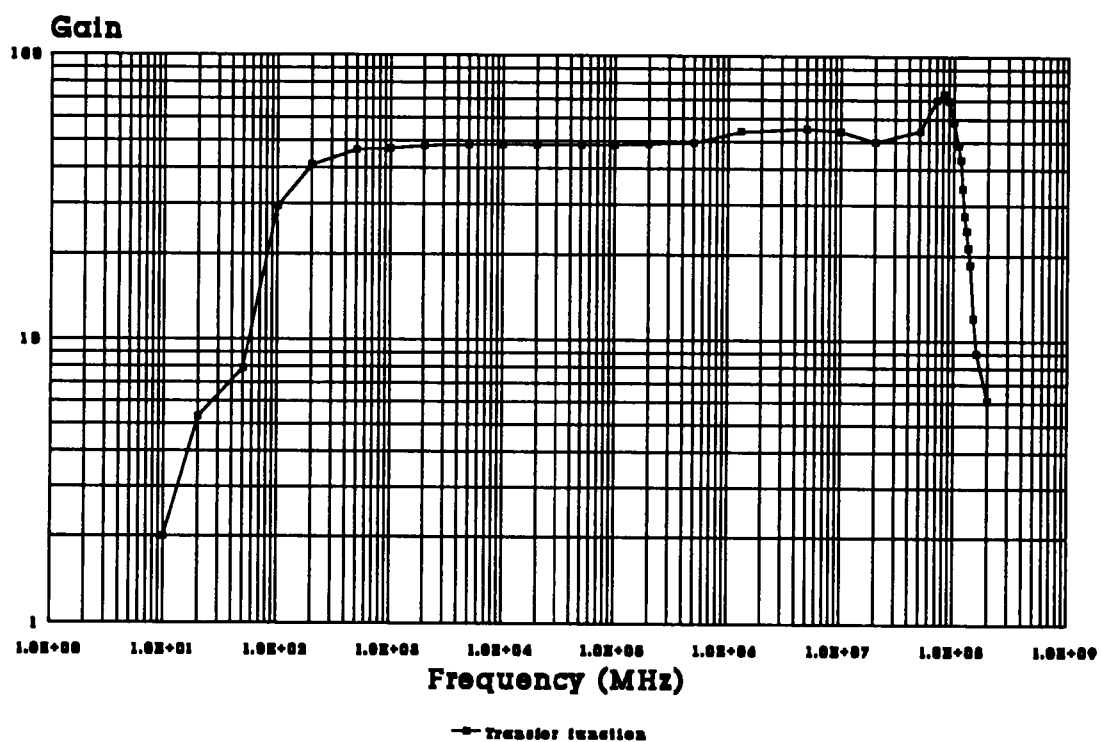


Figure 5-18. Experimental frequency response plot.

product of 5.7 GHz (driving a 50 Ω load) was better than the expected 4.2 GHz gain-bandwidth.

It was more difficult to obtain an experimental measurement of the noise performance of the circuit. One method of measuring the output noise was to use a true RMS meter. A 50 Ω terminator was connected to the input of the amplifier and a cable was fed from the output of the amplifier into the meter where it was terminated in 50 Ω . The meter read 0.27 millivolts RMS, but adjustments were made to that figure before it was used for comparison. First of all, the bandwidth of the meter was only 10 MHz so the noise had to be extrapolated out to the 120 MHz bandwidth of the amplifier, which was done by multiplying by the square root of the ratio of these two bandwidths. When modified by this factor (3.46) the output noise voltage was

$$V_{Omeas} = (0.27 \text{ mV}) * \frac{(120 \text{ MHz})^{0.5}}{(10 \text{ MHz})^{0.5}} = 0.935 \text{ mV}. \quad (5.1)$$

Next, the noise contribution of the 50 Ω terminator at the input was subtracted out. This noise was found by multiplying the resistor noise voltage, 0.868 nV/rt Hz, by the gain of the amplifier and the square root of the bandwidth yielding

$$V_R = (0.868 \text{ nV/Hz}^{1/2}) * (49.5) * (120 \text{ MHz})^{0.5} = 0.471 \text{ mV}. \quad (5.2)$$

The noise due to the 50 Ω resistor at the input was removed by finding the square root of the difference between the squares of the values found in Equations 5.1 and 5.2, as shown below:

$$V_{Oadj} = (V_{Omeas}^2 - V_R^2)^{0.5} = 0.808 \text{ mV.} \quad (5.3)$$

The equivalent noise voltage at the output is found by dividing V_{Oadj} by the square root of the bandwidth:

$$V_{oenv} = \frac{V_{Oadj}}{(120 \text{ MHz})^{0.5}} = 73.8 \text{ nV/Hz}^{1/2}, \quad (5.4)$$

and the equivalent noise voltage at the input was

$$V_{ienv} = \frac{V_{oenv}}{49.5} = 1.49 \text{ nV/Hz}^{1/2}. \quad (5.5)$$

This figure was very close to the value of 1.41 nV/Hz^{1/2} calculated for the circuit and slightly above PSpice's predicted value of 1.31 nV/Hz^{1/2}.

Alternate attempts to estimate the noise in the circuit included feeding the output into a spectrum analyzer while the input was terminated with 50 Ω . The spectrum analyzer did not have enough gain to measure the noise, and the resulting plot was a power spectral density that was flat across the bandwidth of the amplifier with a magnitude of

$10^{-14} \text{ V}^2/\text{Hz}$, which was the maximum sensitivity of the spectrum analyzer. Thus this measurement only provided an upper limit on what the noise could be,

$$V_{Omax} = (10^{-14} \text{ V}^2/\text{Hz})^{0.5} * (120 \text{ MHz})^{0.5} = 1.10 \text{ mV}, \quad (5.6)$$

which was not much more than the value calculated in Equation 5.1. Another method employed to determine the noise performance of the amplifier was to examine the output on an oscilloscope. With the scope intensity turned to its maximum value, the largest noise pulses appeared to be about 3.6 mV from peak to peak. To convert this reading to an estimated rms value it was divided by 5, yielding 0.72 mV, which was less than the value obtained in Equation 5.1 by 23%. Since the scope reading was subject to the sensitivity of the eye and the spectrum analyzer apparently could not pick up the output noise of the circuit, the reading obtained from the RMS meter was trusted as the most accurate measure of the noise performance of the circuit.

CHAPTER 6

CONCLUSIONS

Results

The goal of this project was to develop an amplifier that had a voltage gain of 100 and a 100 MHz bandwidth or greater. The amplifier was to be able to drive a pulse (either positive or negative) with an amplitude of up to 1 Volt into a 50 Ω load and was to have a gain nonlinearity of no more than 5%.

The characteristics of the amplifier that was developed included a voltage gain of 99 and a bandwidth extending from 130 Hz to 115 MHz, giving a gain-bandwidth product of 11.4 GHz. Linearity tests showed that for output pulses ranging from 0.1 Volts to 1.0 Volts in both the positive and negative directions, the maximum nonlinearity in the gain was a reduction by 3.2% of the average gain. The maximum increase in the gain was 2.1% over its average value. The gain of output pulses with amplitudes less than 0.1 Volts could not be measured accurately enough to perform linearity calculations (this process involved measuring input pulses with amplitudes less than 2 mV).

The rise times for 1-Volt output pulses were 4.34 ns (positive output) and 4.52 ns (negative output), and the small-signal rise times were 3.26 ns (positive output) and 3.37 ns (negative output). When the 1 ns rise time of the pulse generator was subtracted out, the values were as shown in Table 6-1.

This amplifier can be placed directly into the measurement system discussed in Chapter 1. The system would retain its gain of 500 V/mA and the bandwidth would be extended to 64 MHz, with a low-frequency corner at 130 Hz. The rms input noise voltage of the amplifier was 16 μ V, only 0.13% of the rms output noise voltage of the preamplifier. Therefore this amplifier will not degrade the noise performance of the system and will improve the system's frequency response.

Table 6-1. Rise time data.

	Pos. pulse	Neg. pulse
Large signal (1 V)	4.22 ns	4.41 ns
Small signal (0.05 V)	3.10 ns	3.22 ns

Improvements

Although this project yielded favorable results several areas could be improved. The greatest improvement in performance would result from the implementation of this design as a monolithic circuit. Although the expense of the first circuit would be considerably higher, a monolithic design would be much more advantageous from a manufacturing standpoint since it would be very reproducible. Instead of needing extensive changes to suppress parasitic oscillations, each circuit produced would be identical and ready to use. This approach would involve considerable design and modeling to insure that the prototype worked properly, but if many of these amplifiers were to be produced then the time and expense should be justified.

Several improvements that would further enhance the circuit's performance could have been made on the present amplifier had time permitted. Thermal coupling throughout the circuit would help stabilize its bias currents. Coupling was achieved by placing the appropriate transistors near each other in the layout, but many more efficient methods exist, such as bonding the appropriate transistors together. The transistors for which this coupling would be most beneficial were the current source pairs Q8/Q9 (Figure 5-1) and Q16/Q17 (Figure 5-2), and the diode output driver

combinations Q4/Q5/Q6/Q7 and Q12/Q13/Q14/Q15. Fabricating a monolithic circuit would also facilitate thermal coupling.

Another change that would be relatively simple to implement is to decrease the value of resistor R_1 (Figure 5), which was used to limit the input impedance of the amplifier at very low and very high frequencies. This modification would improve the input termination, reducing the overshoot and ringing associated with the pulse response.

Using a smaller box to house the circuit could also improve its stability against oscillations. When the amplifier was being tested and one lid was removed from the box, oscillations would sometimes change amplitude and/or frequency depending on the height the lid was held above the box. These observations indicated that the box was acting as a cavity in which RF signals were being transmitted by some of the components of the circuit. Reducing the size of this cavity by using a smaller box would help prevent pickup of stray signals by the other components in the circuit.

A computer-aided layout would probably enhance amplifier performance as well. Laying out the circuit by hand afforded only loose control over parameters like trace width and pad size. A more sophisticated method of etching the board would decrease pitting and other effects associated with the rudimentary process employed for this project. Any future layout should also use footprints that are more closely matched to the transistors. The ones used in this

design were all measured from the 2SC3585, which was slightly larger than the other transistors even though all supposedly had an SOT-23 package. This alteration would simplify assembly of the board.

Other improvements could be implemented, which would involve redesigning the circuit. The dynamic range of the circuit could be increased by increasing the power supply voltages, which were set at ± 5.5 Volts. Other measures would have to be taken simultaneously to protect the transistors against these higher voltages. New transistors could possibly be found, or may be attainable in integrated circuit technology, which has adequate high-frequency characteristics as well as larger breakdown voltages. If no such transistors were available, protection circuitry could be added to guard against the breakdown of these elements.

Impact of the Project

The amplifier developed did not have as much gain-bandwidth as many of the integrated circuits reviewed in Chapter 2. However, it has a very wide bandwidth and a corresponding high gain-bandwidth product for a discrete circuit. As discussed before, a monolithic implementation of this circuit would have many advantages over the discrete design, so why should a discrete design be considered?

As mentioned earlier, the cost for integrated circuits is high (compared to discrete circuits) if only one circuit is required for the application. Also, an integrated circuit design must be shipped for fabrication, demanding a long turn-around time, unless the designer has a clean room at his disposal. The discrete circuit, on the other hand, has time constraints determined mainly by the time required to acquire transistors (probably a couple of days) and to etch a printed circuit board, which will depend on the facilities available to the designer.

Thus this discrete amplifier should be a benefit to a designer with a modest budget and strict time constraints who needs a small number of circuits for an application. It is hoped that the design information contained in this paper will greatly reduce the time required to fabricate a discrete wideband amplifier for a purpose like the one described above.

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LIST OF REFERENCES

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APPENDIX

PSpice Program Listing for Voltage Amplifier

Voltage Amplifier

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RS1    16    1    51
Q1      2    1    3  SC3585
RE1     3   52   986
CE1     3   52   1.6UF
Q8      4    4   51  BSR12
RC8     4    0   991
Q9     31    4   51  BSR12
RC9     31    2   604
RB2     2    5    39
Q2     51    5    6  SC3585
Q3      6    6    7  MMBR901
Q4      7    7    8  MMBR571
Q5     45   45    8  BSR12
RED1    45    9   12
RE5     9   52   560
RB6     7   10    39
Q6     39   10   37  MMBR571
RE6     37   12    3.9
RC6     51   39    20
CC6     39    0   6.8UF
RB7     9   14    39
Q7     40   14   38  BSR12
RE7     12   38    3.9
RC7     40   52    20
CC7     40    0   6.8UF
CS2     12   30   22UF
RS2     30   15   68.1
RF1     1    6   536
Q10     42   15   19  SC3585
RE10    19   54   390
CE10    19   54   22UF
Q16     20   20   53  BSR12
RC16    20    0   560
Q17     18   20   53  BSR12
RC17    18   42   100
RB11    42   21    10
Q11     53   21   22  MMBR571
Q12     22   22   23  MMBR901
Q13     23   23   41  MMBR901
RED2    41   24   16.2
RE13A   24   32   38.3
RE13    32   54   402
RB14    22   25    39
Q14     35   25   33  MMBR901
RE14    33   27    3.9
RC14    53   35    10
CC14    35    0   0.01UF
RB15    24   29    37

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Q15 36 29 34 BSR12
 RE15 34 27 3.9
 RC15 36 54 10
 CC15 36 0 0.01UF
 RF2 15 32 681
 RS3 27 28 47
 RL2 28 0 50

LP1 100 55 18.5UH
 RP1 55 51 10.2
 CP1 51 0 68UF
 LP2 200 56 75UH
 RP2 56 52 10.2
 CP2 52 0 68UF
 LP3 100 57 16UH
 RP3 57 53 10.2
 CP3 53 0 68UF
 LP4 200 58 110UH
 RP4 58 54 10.2
 CP4 54 0 68UF

* Power supplies

VCC 100 0 5.5

VEE 200 0 -5.5

*Transistor models

.MODEL SC3585 NPN BF=120 BR=2.3 RB=14 RC=5 RE=0.3 TF=18PS
 +TR=15PS CJE=2P CJC=0.8P XCJC=0.25 IS=8.3E-15 ISE=1.3E-11
 +NF=1.15 VAF=33 VAR=9 NE=3 IKF=60E-3 IK=15M

.model MMBR571 NPN(Is=10f Xti=3 Eg=1.11 Vaf=38.73 Bf=105.1
 +Ise=97.7f Ikf=.441 Nk=.5 Xtb=1.5 Br=1 Isc=0 Nc=2 Ikr=0 Rc=0
 +Cjc=2.138p Mjc=.2949 Vjc=.5273 Fc=.5 Cje=2.684p Mje=.5158
 +Vje=.8366 Ne=1.729 Tr=10n Tf=12.7p Itf=62.26m Xtf=1.275
 +Vtf=10)

.model MMBR901 NPN(Is=220E-18 Xti=3 Eg=1.11 Vaf=74.32
 +Bf=84.91 Ise=90.08f Ne=1.695 Ikf=.2277 Nk=.5026 Xtb=1.5
 +Br=1 Isc=0 Nc=2 Ikr=0 Cjc=2.429p Mjc=.3333 Vjc=.75 Fc=.5
 +Cje=5p Mje=.3333 Vje=.75 Tr=10n Tf=8p Itf=22.84m Xtf=10
 +Vtf=25)

.model BSR12 PNP(Is=1.5f Xti=3 Eg=1.11 Vaf=20.18 Bf=101.5
 +Ise=15.04f Ne=1.413 Ikf=72.6m Nk=.5187 Xtb=1.5 Br=1
 +Isc=1.5f Nc=1.962 Ikr=1.24 Rc=2.37 Cjc=2.465p Mjc=.1588
 +Vjc=.3668 Fc=.5 Cje=2.477p Mje=.236 Vje=.5427 Tr=40.58n
 +Tf=140p Itf=.3 Xtf=10 Vtf=10)

*Generator

VIN 16 0

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+ AC 100.0E-6 0
+ PWL(
+ 5.000000E-09 0.000000E+00
+ 6.000000E-09 2.000000E-02
+ 1.500000E-08 2.000000E-02
+ 1.600000E-08 -2.000000E-02
+ 2.500000E-08 -2.000000E-02
+ 2.600000E-08 2.000000E-02
+ 3.500000E-08 2.000000E-02
+ 3.600000E-08 -2.000000E-02
+ 4.000000E-08 -2.000000E-02
+)
.OPTIONS LIMPTS=501 RELTOL=0.00001
.TRAN/OP 0.1NS 35NS
.ac dec 20      1      10.000g ; *ipsp*
.TF V(28) VIN
.PROBE
.END

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VITA

Stephen Wesley Milam was born in Knoxville, Tennessee on April 6, 1967. He grew up in Knoxville and graduated from Farragut High School in June, 1985. He enrolled at The University of Tennessee in September, 1985 and received the degree of Bachelor of Science in Electrical Engineering in May, 1989. After entering the graduate program at The University of Tennessee in May, 1989, he received a Master of Science in Electrical Engineering degree in December, 1992.

He is currently enrolled in the graduate program of the Georgia Institute of Technology, and he likes to spend his spare time on the volleyball court.