Reliability Analysis of Nanocrystal Embedded High-k Nonvolatile Memories

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To my dear family

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ABSTRACT

The evolution of the MOSFET technology has been driven by the aggressive shrinkage of the device size to improve the device performance and to increase the circuit density. Currently, many research demonstrated that the continuous polycrystalline silicon film in the floating-gate dielectric could be replaced with nanocrystal (nc) embedded high-k thin film to minimize the charge loss due to the defective thin tunnel dielectric layer.

This research deals with both the statistical aspect of reliability and electrical aspect of reliability characterization as well. In this study, the Zr-doped HfO_2 (ZrHfO) high-k MOS capacitors, which separately contain the nanocrystalline zinc oxide (nc-ZnO), silicon (nc-Si), Indium Tin Oxide (nc-ITO) and ruthenium (nc-Ru) are studied on their memory properties, charge transportation mechanism, ramp-relax test, accelerated life tests, failure rate estimation and thermal effect on the above reliability properties.

C-V hysteresis result show that the amount of charges trapped in nanocrystal embedded films is in the order of nc-ZnO>nc-Ru>nc-Si~nc-ITO, which might probably be influenced by the EOT of each sample. In addition, all the results show that the nc-ZnO embedded ZrHfO non-volatile memory capacitor has the best memory property and reliability. In this study, the optimal burn-in time for this kind of device has been also investigated with nonparametric Bayesian analysis. The results show the optimal burn-in period for nc-ZnO embedded high-k device is 5470s with the maximum one-year mission reliability.

TABLE OF CONTENTS

Chapter			Page
1	INTRODUCTION……		1
	1.1	Challenges in the Nano Era……..	1
	1.2	Nanocrystal Embedded High-k Dielectric Thin Film…….....	3
	1.3	Fabrication of the Nanocrystal Embedded ZrHfO Nonvolatile Memories…….....	4
	1.4	Burn-In Procedure…….....	7
		1.4.1 Infant Mortality…….	7
		1.4.2 Cases and Physical Experimental Results……	11
		1.4.3 Optimal Burn-In Model……	15
		1.4.4 Summary……...	23
2	CHARGE TRAPPING AND DETRAPPING MECHENISMS FOR NANOCRYSTAL EMBEDDED HIGH-K NONVOLATILE MEMORIES.....		25
	2.1	Capacitance-Voltage Characteristics……	25
	2.2	Relaxation Current……	27
	2.3	Relaxation Current Decay Rate…….	30
3	BREAKDOWN MECHAISMS……		35
	3.1	Ramp-Relax Measurement	35
	3.2	Breakdown Mechanism of Single-Layer Nanocrystal Embedded ZrHfO Thin Film……...	35
	3.3	Breakdown Mechanism of Dual-Layer Nanocrystal Embedded ITO ZrHfO Thin Film……...	40

4 TEMPERATURE INFLUENCE ON CHARGE TRAPPING/DETRAPPING MECHANISM OF NANOCRYSTAL ZINC OXIDE / INDIUM TIN OXIDE EMBEEDED HIGH-K THIN FILM…… 48

4.1 Temperature Influence on I-V Characteristics…….. 48

4.1.1 nc-ZnO Embedded ZrHfO Capacitor……... 48

4.1.2 nc-ITO Embedded ZrHfO Capacitor…… 52

4.2 Temperature Influence on Charge Transportation Mechanism…… 54

4.2.1 nc-ZnO Embedded ZrHfO Capacitor……... 54

4.2.2 nc-ITO Embedded ZrHfO Capacitor…… 55

4.3 Temperature Influence on C-V Hysteresis Characteristics……... 58

4.4 Temperature Influence on G-V Characteristics…… 62

4.5 Temperature Influence on Charge Retention Efficiency…….. 64

4.5.1 nc-ZnO Embedded ZrHfO Capacitor……... 64

4.5.2 nc-ITO Embedded ZrHfO Capacitor…… 66

4.6 Temperature Influence on the Breakdown Mechanism…… 69

5 OPTIMAL BURN-IN TIME…… 72

5.1 Hazard Rate Function Estimation……. 73

5.2 Accelerated Life Test…… 75

5.3 Optimal Burn-In Time…….. 76

6 SUMMARY AND CONCLUSIONS……... 82

REFERENCES……. 85

VITA…… 95

LIST OF FIGURES

FIGURE		PAGE
1	Schematic diagram of a MOSFET……..	2
2	Cross-sectional views of (a) single- and (b) dual-layer nanocrystal embedded ZrHfO capacitors……..	5
3	Traditional bathtub curve……	9
4	Modified bathtub curve……...	9
5	Eventually increasing failure rate function……..	11
6	Current gain versus base-emitter voltage (V_{be}) with the collector emitter ($V_{ce} = 3.0V$) for the same sample before and after CPVS……...	13
7	Optimized burn-in temperature for constant burn-in loss……...	14
8	*C-V* curves for nanocrystals embedded ZrHfO films at -6 to 6V sweep range……	26
9	Relaxation current decay with time of nc-Ru and nc-ITO embedded ZrHfO films and the corresponding control sample……	29
10	Relaxation current decay with time of nc-Si embedded ZrHfO films and the corresponding control sample……	29
11	Relaxation current decay with time of nc-ZnO embedded ZrHfO films and the corresponding control sample……	30
12	Relaxation current normalized to polarization vs. gate voltage release time of various embedded and non-embedded dielectrics (log-log scale)……..	32
13	Ramp-relax test curves of various nanocrystals embedded high-*k* films……	37
14	Time-dependent dielectric breakdown curves of nc-ZnO embedded ZrHfO high-k film stressed at different V_g's……	39

15 (a) J_{ramp}-V_g and (b) J_{relax}-V_g curves of a single-layer nc-ITO embedded ZrHfO capacitor measured with the two-step ramp-relax method…….. 42

16 (a) J_{ramp}-V_g and (b) J_{relax}-V_g curves of a dual-layer nc-ITO embedded ZrHfO capacitor measured with the two-step ramp-relax method…….. 44

17 *C-V* curves of (a) single- and (b) dual-layer nc-ITO embedded ZrHfO capacitors before and after first and second breakdowns…… 46

18 Time-dependent dielectric breakdown curves of single- and dual-layer nc-ITO embedded ZrHfO high-*k* film stressed at -6V……. 47

19 *J-V* curves of MOS capacitors with nc-ZnO embedded ZrHfO at 25°C, 75°C and 125°C, respectively……. 50

20 *I-V* curve of the nc-ZnO embedded MOS capacitor measured (a) from 0V to -5V and (b) from 0V to +5V……... 51

21 *J-V* curve of the nc-ITO embedded MOS capacitor measured (a) from 0V to +6V and (b) from 0V to -6V……... 53

22 (a) Fitting of Schottky relationship under the positive V_g condition and (b) fitting of the Frenkel-Poole relationship under the negative V_g condition at 25°C, 75°C, and 125°C…… 57

23 *C-V* hysteresis curves for (a) control sample at 25°C
(b) nc-ZnO embedded ZrHfO at 25°C
(c) nc-ZnO embedded ZrHfO at 75°C, and
(d) nc-ZnO embedded ZrHfO at 125°C……... 61

24 *G-V* curves of capacitors in the backward sweep direction at 25°C, 75°C and 125°C, respectively……... 63

25 (a) Charge retention characteristic of ZnO embedded high-*k* thin film under different temperatures…….. 65

(b) same as (a) with time on the logarithm scale…….

26 (a) Charge retention characteristic of nc-ITO embedded high-k thin film under different temperatures 68

(b) same as (a) with time on the logarithm scale…….

27 J_{ramp}-V_g and J_{relax}-V_g curves at different temperatures……. 71

28 The *J-t* curve example for the lifetime test…….. 77

29 Estimated hazard rate function…… 80

30 Conditional reliability of accomplishing different mission time……. 81

31 Achieving different mission reliabilities for mission time = 1 year…… 81

LIST OF TABLES

TABLE		PAGE
1	Gate structures and fabrication conditions……..	6
2	Percentages of deeply trapped and loosely trapped charges for nanocrystal embedded samples after the first 20 seconds……..	34
3	The lifetime data (time to failure) set for the nc-ZnO embedded ZrHfO capacitor……..	78

CHAPTER 1

INTRODUCTION

As the channel length and gate oxide thickness of MOSFETs scale down, the thickness of the silicon dioxide (SiO_2) gate dielectric has to be decreased accordingly. When the thickness of SiO_2 is below 1.2 nm, its leakage current becomes unacceptably high and the device's reliability is a major concern. The schematic diagram of a MOSFET is shown in Figure 1. A proper high-k dielectric material can solve these problems. In addition, high-k materials have also been used to in the nanocrystal embedded high-density nonvolatile flash memory, the next generation for the memory devices, to improve the programming efficiency [1-4]. One concern is that tight reliability margins may limit the miniaturization of nano-scale IC products. Therefore, there is an urgent need to investigate the reliability of nano devices in the early design stages. A brief description of some critical issues in the present semiconductor industry is presented in the next sections.

1.1 Challenges in the Nano Era

Recently, the technologies for today's design and manufacturing tend to move from the realm of micro- to nano-scale. The scaled technology raises new challenges for reliability analysis. Kuo [5] pointed out that there appear to be four major challenges related to nano electronics that currently face the field of reliability:

(1) Identification of the failure mechanisms

(2) Enhancement of the low yield in nano products

(3) Management of the scarcity and secrecy of available data

(4) Preparation of reliability practitioners and researchers for keeping up with the nano era.

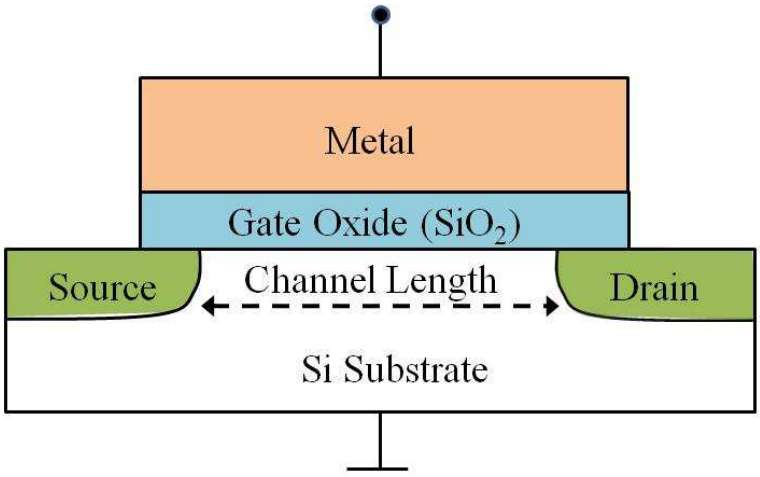


Figure 1. Schematic diagram of a MOSFET

The second challenge makes production extremely expensive. Thus, how to improve the efficiency and reduce cost of burn-in process will still be one of the major key research topics in the future. Another new challenging issue of burn-in process is the scarcity of data. This phenomenon makes it almost impossible to use traditional reliability analysis tools and statistical inference to make accurate predictions. To deal with this situation, Kuo [5-6] pointed out that Bayesian approach will be applied more widely than ever before.

To deal with limited data, Chien and Kuo [7] used Dirichlet distribution, one of the famous models for non-parametric Bayesian analysis, to establish a non-parametric Bayes approach to decide system burn-in time. Arjas and Gasbarra [8] proposed a non-parametric Gibbs sampler model to estimate the hazard rate function. This technique will be most beneficial to the following cases: (1) sampling is expensive, (2) the burn-in cost is high, and (3) only limited knowledge is available about the device under test (DUT); all the three cases often happen in the semiconductor industry. A Bayesian burn-in procedure was developed by Kwon and Keats [9] for limited failure populations. Meanwhile, Tseng and Peng [10] and Tseng

et al. [11] proposed an integrated Wiener process to obtain the optimal burn-in policy without sufficient amount of time-to-failure data.

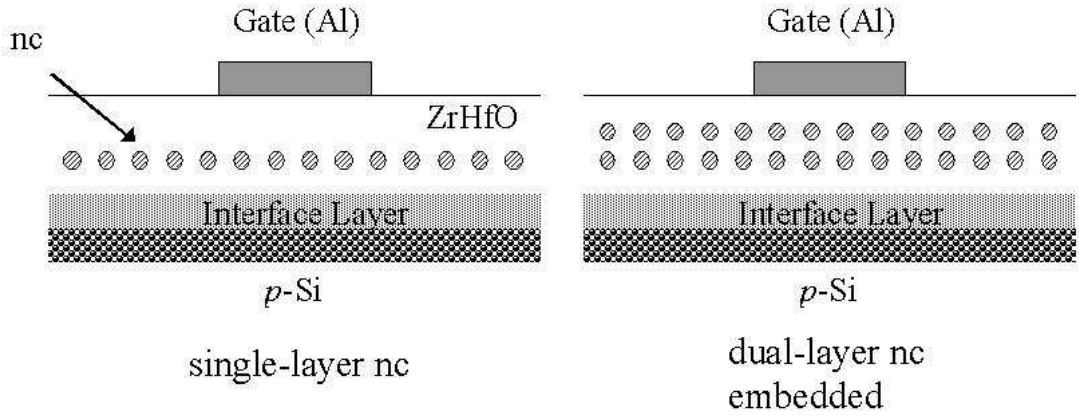
1.2 Nanocrystal Embedded High-k Dielectric Thin Film

When the CMOS device is scaled down to the nano size, the thickness of the silicon dioxide (SiO_2) gate dielectric layer must be reduced drastically, e.g., to 1.2 nm with the channel length below 45 nm [12]. With this kind of thin film, the leakage current becomes very high and the dopant is easily diffused to the channel region to deteriorate the device performance and reliability [12-14]. The above problems can be solved by using a high-*k* dielectric film to replace the SiO_2 film. However, the conventional high-*k* materials, such as ZrO_2 and HfO_2 have potential reliability problems because of their low crystallization temperatures, e.g., <600˚C [1]. The Zr-doped HfO_2 (ZrHfO) high-*k* film has been proved to have better bulk and interface layer properties, such as a higher crystallization temperature, a larger effective *k* value, and a lower interface state density [15-18]. The Zr-doped HfO_2 film has been prepared into sub 1 nm EOT thickness film [15, 19]. The high-*k* film has also been used as a great dielectric material in memory devices [1]. For example, the conventional poly-Si floating-gate nonvolatile memory (NVM) includes a continuous poly-Si thin film in the SiO_2 gate dielectric as the charge-retaining medium. However, it is prone to lose all charges with the formation of a single leakage path in the tunnel oxide layer. The nanocrytals embedded SiO_2 structure can eliminate the above problem because one leaky path in the tunnel oxide can only drain charges stored in a few nanodots [20]. When the SiO_2 layer is replaced with a high-k film, the opportunity of forming a leaky path is reduced because a physically thick layer can be

used. Nanocrystalline Si, SiGe, Ru, ITO, ZnO have been dispersed in high-k as the electron- or hole-trapping media [1, 4, 21]. Most of the studies on the nanocrystals embedded high-*k* memory devices are focused on how to increase the charge trapping density with various types of materials [22-23]. There is little understanding on the reliability of this kind of device, which is critical to the practical application. In this paper, authors investigated failure mechanism using the current relaxation measurements and breakdown phenomena. The MOS capacitors including the nc-ZnO, -Ru, -Si, -ITO (Indium Tin Oxide) embedded ZrHfO high-*k* dielectric are used as the example for the study.

1.3 Fabrication of the Nanocrystal Embedded ZrHfO Nonvolatile Memories

In this paper, the Zr-doped HfO_2 (ZrHfO) dielectric was used because of its excellent dielectric properties, such as the low leakage current, high crystal temperature, thin interface layer, and low interface density of states. Figure 2 shows the basic structure of the single- and dual-layer nanocrystals embedded high-k thin film. All samples were deposited on the HF pre-cleaned *p*-type Si (100) wafer (doping concentration at 10^{15} cm^{-3}) and the $ZrHfO_2$ film was deposited by reactive sputtering using a Hf/Zr (88:12 wt%) composite target in an Ar/O_2 (1:1) mixture at 5m Torr and room temperature. For the single-layer nanocrystal embedded samples, the sputter powers of $ZrHfO_2$ film and nanocrystal for nc-Ru, -ITO, -Si and -ZnO embedded capacitors were (100, 80), (100, 80), (100, 100) and (60, 60) respectively. The as-deposited embedded layers were amorphous. However, they were crystallized into the nanocrystalline form after the post-deposition annealing (PDA). The detail preparation conditions are shown in Table 1.



(a) (b)

Figure 2. Cross-sectional views of (a) single- and (b) dual-layer nanocrystal embedded ZrHfO capacitors

Table 1. Gate structures and fabrication conditions

Sample	Post-deposition annealing temperature (°C)/gas	Post-metal annealing temperature (°C)/gas	Equivalent oxide thickness (EOT) (nm)
nc-Ru embedded	950/(N_2/O_2 1:1)	250/(N_2/H_2)	9
nc-ITO embedded	950/(N_2/O_2 1:1)	250/(N_2/H_2)	8.6
control sample for nc-Ru and nc-ITO	950/(N_2/O_2 1:1)	250/(N_2/H_2)	10
nc-Si embedded	950/(N_2)	300/(N_2/H_2)	10
control sample for nc-Si	950/(N_2)	300/(N_2/H_2)	10
nc-ZnO embedded	800/(N_2)	200/(N_2/H_2)	7.8
control sample for nc-ZnO	800/(N_2)	200/(N_2/H_2)	6

1.4 Burn-In Procedure

Burn-in is the most widely used technique to improve the reliability of products before they are sold to the consumers. However, it is well known that burn-in process is costly. How to determine the optimal burn-in period and improve the burn-in procedure have been intensively studied during the past 20 years. Moreover, in the last decade, we can see that excitement and interest in smaller and lighter consumer products has driven the need to reduce package size. That is, to find the optimal burn-in environment conditions for each IC generation is another important issue.

1.4.1 Infant Mortality

The purpose of the burn-in process is to weed out the "infant mortalities" and improve the reliability of products. Typically, during the burn-in process, the temperature will be chosen at $110^{\circ}C$ and supply voltage is 30% higher than normal condition [24]. Burn-in process can be performed under three different levels: die-level burn-in, wafer-level burn-in and package burn-in. In this section, we will discuss several definitions of infant mortality and some new burn-in process.

It is widely believed that many products, particularly silicon integrated circuits, exhibit bathtub-shape failure rate function. In the literature, properties of the optimal burn-in time have been studied under this assumption. The traditional bathtub-shape failure rate function is defined as follows:

$$r(t)=\begin{cases}\text{strictly decreases, if } 0\le t\le t_1\\ \text{a constant, if } t_1\le t\le t_2\\ \text{strictly increases, if } t_2\le t\end{cases} \tag{1}$$

where t_1 and t_2 are the change points of $r(t)$. An example of bathtub-shape failure rate function is presented in Figure 3. Traditional bathtub-shape curve divided the component life into three stages. The first stage is known as infant mortality period. In this stage, we have a decreasing failure rate (DFR). The second stage is called the normal operating life. In this stage, we have a constant failure-rate period (CFR). The last stage is a period of wearout with an increasing failure rate (IFR) because of aging.

Another famous failure rate model is called the modified bathtub-shape failure rate function, defined as follows:

$$r(t)=\begin{cases}\text{strictly increases, if } 0 \le t \le t_0\\ \text{strictly decreases, if } t_0 \le t \le t_1\\ \text{a constant, if } t_1 \le t \le t_2\\ \text{strictly increases, if } t_2 \le t\end{cases} \tag{2}$$

where t_1, t_2 and t_3 are the change points of $r(t)$. An example of the modified bathtub-shape failure rate function is presented in Figure 4. The modified bathtub-shape failure rate function can be obtained from the mixture of strong component (main distribution) and that of weak component (freak distribution) [25]. Recently, there have been many burn-in researches based on the concept of the mixture of distributions. However, Klutke et al. [26] pointed out that the assumption of traditional or modified bathtub-shape failure rate function is restrictive for burn-in research.

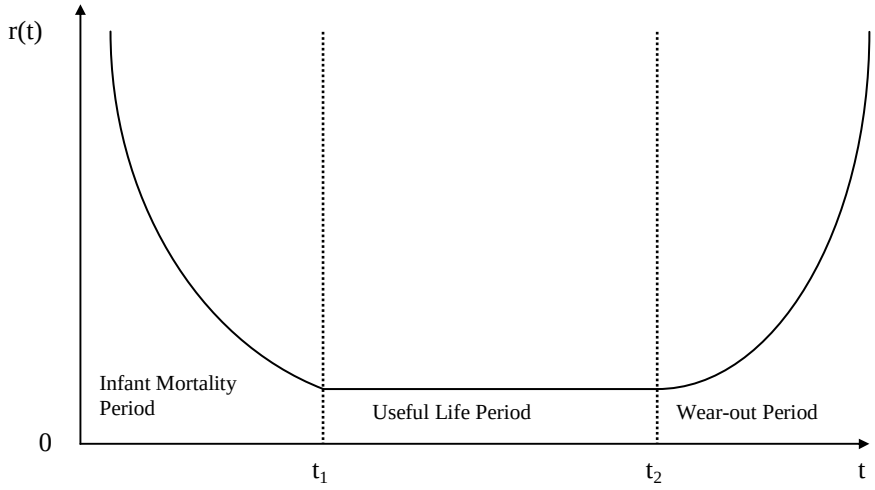


Figure 3. Traditional bathtub curve

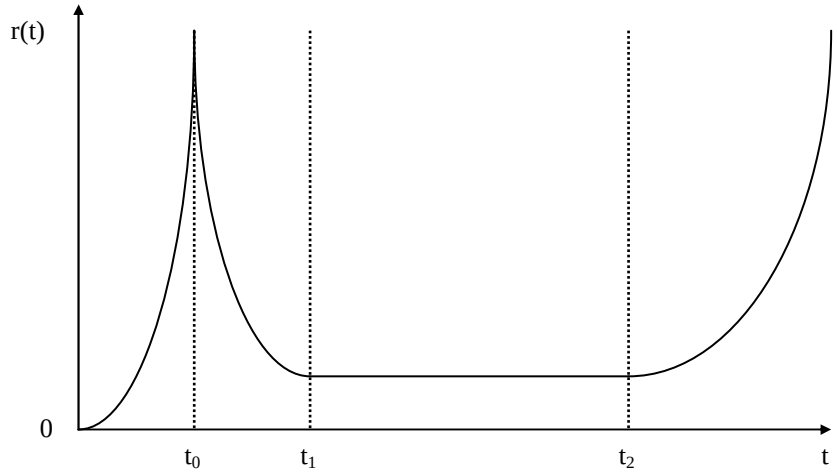


Figure 4. Modified bathtub curve

A new concept of eventually IFR was introduced by Mi [27], and the optimal burn-in time for various objectives was studied, such as [28-32] and [33]. A failure rate function $r(x)$ is called eventually IFR if there exists $0 \le x_0 < \infty$ such that $r(x)$ is strictly increasing in $t > x_0$. For the eventually increasing failure rate function $r(x)$, the definitions of the first and second wear-out points t^* and t^{**} are as follows:

$$\begin{aligned} t^* &= \inf\{t \ge 0 : r(x) \text{is nondecreas ing in } x \ge t\} \\ t^{**} &= \inf\{t \ge t^* : r(x) \text{is strictly increases in } x \ge t\} \end{aligned} \tag{3}$$

Obviously, $0 \le t^* \le t^{**} \le x_0 < \infty$; the traditional and modified bathtub-shape failure rate functions are both the special cases of the eventually IFR. An example of the eventually IFR function is shown in Figure 5.

In fact, some underlying lifetime distributions have a unimodal (hump) failure rate function [34], for example, lognormal distribution, or inverse Gaussian distribution. Among all the different failure rate functions, Baskin [35] suggested the Akaike Information Criterion (AIC) or the root-mean-square criterion for selection of the best model.

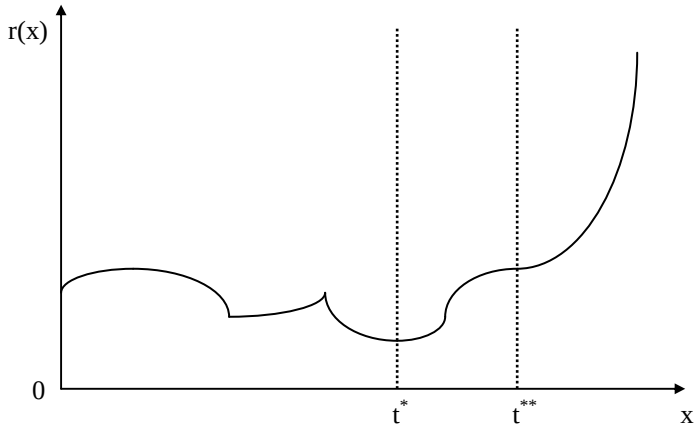


Figure 5. Eventually increasing failure rate function

1.4.2 Cases and Physical Experimental Results

Generally, the silicon integrated circuits have extremely high rate of infant mortality. Burn-in has been the most popular technique to recognize and partially eliminate the infant mortality failures. During the last five years, engineers have been trying new materials to replace the traditional silicon based device that have better results after burn-in test and looking for the optimal burn-in environment conditions for each generation. In order to improve the competitiveness with other opponents, lots of research work has been focus on the burn-in cost reduction techniques.

(a) New Materials

Besides the traditional silicon based device, InGaP/GaAs heterojunction bipolar transistors (HBTs) have attracted much attention because they have better uniformity and reliability after the burn-in procedure. InGaP/GaAs HBTs are widely used in high frequency and mid power application. In the early stage of developing

InGaP/GaAs HBTs, beryllium (Be) was a very popular candidate for doping the base layer because of its high hole concentration. However, Be diffusion under the current stress will cause the rapid degradation of Be-doped HBTs. In recent research, HBTs with carbon-doped base layers are very popular due to its lower diffusivity with respect to beryllium. And it allows carbon-doped HBTs to avoid the base dopant outdiffusion leading to better reliability properties. The early increase of the dc current gain β (burn-in effect) due to the electrical stress of carbon-doped InGaP/GaAs HBTs has been intensively studied recently for example [36-40].

InGaP/GaAs HBTs featuring a carbon doped base material grown by metalorganic chemical vapor deposition show the so-called burn-in effect, which consists of an initial increase in the current gain when the device is normally biased at room temperature [41]. Mimila-Arroyo [41] has shown that the burn-in effect observed in InGaP/GaAs HBTs can be explained by the following two processes: (1) a bias dependent passivation of recombination centers located in the emitter region resulting in a decrease of the base diffusion current that is stable at room temperature, and (2) an increase of the emitter-base recombination current that will be adjusted permanently as a function of the emitter-base bias.

It has been proved in Chong et al. [42] that the current gain (β) increases at the opposite extremes of base-emitter voltage (V_{be}) greater than 1.75 V. To substantially suppress the burn-in effect observed in InGaP/GaAs HBTs, a constant period of voltage stress (CPVS) with $V_{be} = 2.0V$ and $V_{ce} = 3.0V$ (collector-emitter voltage) for 5 minutes is proposed as shown in Figure 6 [43].

To eliminate the burn-in effect in carbon-doped InGaP/GaAs HBTs, Su et al. [44] proposed the Hydrogen lateral diffusion by annealing at low temperature. After

the thermal annealing has been applied at 480 $^{\circ}C$ for 30 minutes, the current gain variation caused by the electrical stress decreased from 42.7% to 2.6%.

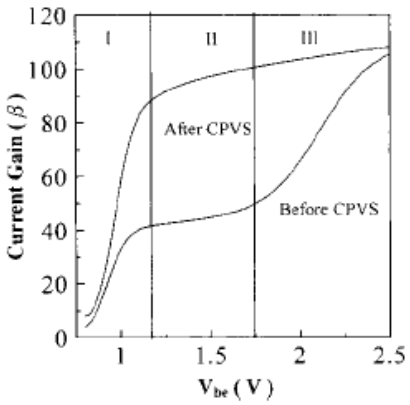


Figure 6. Current gain versus base-emitter voltage (V_{be}) with the collector emitter ($V_{ce} = 3.0V$) for the same sample before and after CPVS [43]

(b) Burn-In Environment

To achieve high-performance microprocessor and memories, transistor scaling is a very primary key. Each 30% reduction in CMOS IC technology node scaling has: (1) reduced the gate delay by 30% which increases the maximum clock frequency of 43% (2) doubled the device density (3) reduced the parasitic capacitance by 30% (4) reduced energy and active power per transition by 65% and 50 %, Vassighi et al. [45].

However, Semenov et al. [46] showed that under normal operating condition, the increase in junction temperature is estimated as 1.45 X/generation and this may result in positive feedback leading to thermal runaway during the burn-in process. Vassighi et al. [47] and Semenov et al. [46, 48] have shown the optimal stressed temperature in a burn-in environment is significantly reduced with technology scaling. Vassighi et al. [47] and Semenov et al. [46] have also shown that to maintain a

constant post burn-in yield loss, the optimal burn-in temperature should be decreased at least by $10^{\circ}C$ for each technology generation and the optimal burn-in temperature for each generation is shown in Figure 7 [46].

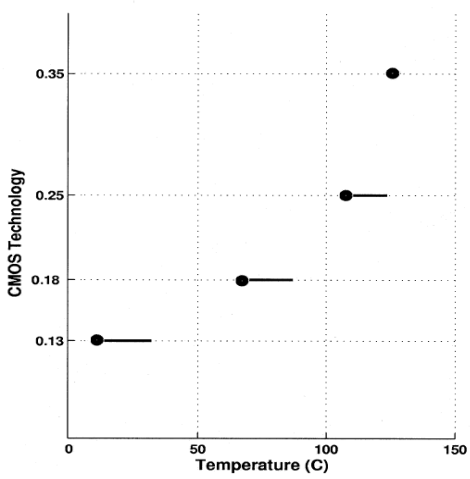


Figure 7. Optimized burn-in temperature for constant burn-in loss [46]

(c) Burn-In Test Cost Reduction Techniques

In this section, how to improve burn-in procedure will be discussed. Burn-in process is costly so how to reduce to the cost generated during burn-in process is one of the key research topics. Lee et al. [49] and Sabade & Walker [50] tried to find out the defective chips before burn-in process. Therefore, the more defective chips they find out, the less chips will be sent to the burn-in test. Sabade and Walker [50] proposed the median of absolute deviations (MAD) of the I_{DDQ} as the criterion to

weed out the defective chips. Rosen et al. [51] developed a simulate model and robust design can be performed to optimized the burn-in procedure. Another burn-in reduction screen, presented by [52], was based on the subset of measurements from the wafer sort data. This subset was identified by the Principal Component Analysis using the die that passed all the tests.

Intel Corporation proposed the new criterion: unit level predict yield (ULPY) and showed that it is approximately twice as efficient as wafer level methods at highlighting die with high defect latent density. Moreover, most of the dies with low ULPY scores will fail at sort and those do not are shown to have higher failure rates at burn-in. This simple measure is defined as

$$ULPY = \sqrt{xyYield \times LocalYield} \tag{4}$$

where *xyYield* is the yield of the specific *x*-*y* die location within the lot and *localYield* is the neighbouring die yield. How to find the optimal schedule of the burn-in oven is another research topic to reduce the burn-in procedure. Sung et al. [54] considered the problem of scheduling a single burn-in oven in the final test. In this paper, they assumed each job belongs to one of a fixed number of families and the release time of the jobs are different from one another. The authors proposed a dynamic programming algorithm to find the optimal schedule, which can minimize the maximum completion time. Monch et al. [55] consider the schedule problem for a single burn-in oven which is a batch processing machine with restricted capacity. The due dates of all jobs are assumed the same and the objective is to minimize the sum of the absolute deviations of completion times from the due date. Deng et al. [56] present

a polynomial time approximation scheme to minimize the total completion time for the burn-in scheduling problem.

1.4.3 Optimal Burn-In Model

Burn-in is a wildly used approach to improve the quality of products pre-sale. However, burn-in is usually costly and increases the manufacturing cost, so how to determine the optimal length of the burn-in procedure is a major issue. In this section, several methods to obtain the optimal burn-in time with different objective functions will be discussed.

(a) Minimize Cost

In the business world, money is everything. This is why in the study of burn-in the cost criterion is often used to obtain the optimal burn-in time. Recently, several cost models are presented.

Model 1

In many burn-in research, system failures have been divided into two types: one is Type I failure (or minor failure), which can be easily removed during burn-in process, and the other is Type II failure (or catastrophic failure), which can only be removed by a complete repair and the burn-in process has to be stopped. Let p and 1-p be the probability of Type II failure and Type I failure when the unit fails respectively. The average cost during the burn-in time b, $C(b)$, can be expressed by [57]

$$C(b)=\frac{1}{\int_b^\infty \overline{G}(t)dt}\left\{\left[c_f+c_m\left(\frac{1}{p}-1\right)\right]-\left[\left(c_f-c_s\right)+\left(\frac{1}{p}-1\right)\left(c_m-c_{sm}\right)\right]\times G(b)+c_0.\int_0^b \overline{G}(t)dt\right\} \qquad (5)$$

where c_0, c_f, c_m, c_s and c_{sm} denote the cost-rate for operating the burn-in procedure, replacement cost, minimal repair cost, shop complete repair cost and shop minimal repair cost respectively. $G(t)$ and $\overline{G}(t)$ denote the CDF and the survival function of the waiting time until the first type II failure of a new unit.

Some research, such as [58-61] pointed out that to determine the optimal burn-in time, we should also consider the warranty policy when the product is sold. Sheu and Chien [60] proposed three cost models under different warranty policies, presented as Model 2-4.

Model 2

This model contains five costs: C_0 = the manufacturing cost per unit without burn-in; C_1 = the fixed setup cost of burn-in per unit; C_2 = the cost per unit time of burn-in per unit; C_3 = the minimal repair cost per Type I failure during burn-in, and C_4 = the extra cost incurred when a failure occurs during the warranty, regardless of the failure type. Let $C(T,\tau)$ denote the expected total cost per unit sold, for a general repairable product with burn-in time τ and warranty period T. In the failure-free policy, the manufacturer is responsible for all the repair and replacement costs during the warranty interval [0, T]. Then for the failure-free policies with renewing, the expected total manufacturing cost per unit for products with burn-in time τ can be expressed by

$$v(\tau)=\frac{C_0+C_1+C_2\cdot\int_0^{\tau}\overline{G}(u)du+C_3\cdot\left(\frac{1}{P}-1\right)\cdot G(\tau)}{\overline{G}(\tau)} \tag{6}$$

where p denotes the probability the Type II failure occurs and $\overline{G}(t)$ is defined as the survival function of the time to the first Type II failure of the product without burn-in.

The expected total warranty cost per unit sold with burn-in time τ and warranty period T, $w(T,\tau)$, is given by

$$w(T,\tau)=\frac{\overline{G}(\tau)-\overline{G}(\tau+T)}{\overline{G}(\tau+T)}\left\{(C_3+C_4)\left(\frac{1}{P}-1\right)+[C_4+v(\tau)]\right\} \tag{7}$$

and $C(T,\tau)=v(\tau)+w(T,\tau)$.

Model 3

In this model, we consider the failure-free non-renewing policy. The expected total cost per unit sold $C(T,\tau)$ and the expected total manufacturing cost per unit for products $v(\tau)$ is the same as in Model 2. But the expected total warranty cost per unit sold $w(T,\tau)$ is now defined as

$$w(T,\tau)=\left\{[C_4+v(\tau)]+(C_3+C_4)\left(\frac{1}{P}-1\right)\right\}V_\tau(T) \tag{8}$$

where $V_\tau(T)$ denotes the number of replacement during [0,T].

Model 4

Besides the failure-free-policy cases, Sheu and Chien [60] also proposed a cost model under the rebate policy and the assumption that the amount of rebate is a linear function of the Type II failure time t. Again, the expected total cost per unit sold

$C(T,\tau)$ and the expected total manufacturing cost per unit for products $v(\tau)$ is the same as in Model 2. The only part of this model different from Model 2 is the expected total warranty cost per unit sold $w(T,\tau)$, defined as

$$w(T,\tau)=\frac{(C_3+C_4)\left(\frac{1}{P}-1\right)T\left[\overline{G}(\tau)-\overline{G}(\tau+T)\right]+k\cdot C_p\left\{T\overline{G}(\tau)-(1-\alpha)\cdot T\overline{G}(\tau+T)-\alpha\int_0^T T\overline{G}(\tau+t)dt\right\}}{T\overline{G}(\tau)} \quad (9)$$

where C_p denotes the sales price and α is a constant between [0,1]

Model 5

The total expected cost during the burn-in time t_b and the warranty period t_w given by

$$Cost(t_b)=C_1+C_2Nt_b+C_3NF(t_b)+C_4N\left[F(t_b+t_w)-F(t_b)\right] \quad (10)$$

was considered by Perlstein [59] as the objective function to obtain the optimal burn-in time by Bayesian method. In this cost model, C_1 is the fixed setup cost per batch of N products; C_2 the time dependent cost for burn-in per unit per unit time; C_3 lost opportunity cost of products which failed through burn-in and C_4 is the cost of field repairs that occur during the warranty period of the system. In the Bayesian paradigm, uncertainty with respect to the distribution parameters is modelled using a multivariate prior probability distribution, $g(\underline{\theta})$. In the last two terms of this model, $F(t)=\int_{\underline{\theta}}F(t|\underline{\theta})\,g(\underline{\theta})\,d\underline{\theta}$, where $F(t|\underline{\theta})$ denotes the CDF of products in the batch and $\underline{\theta}$ represents the parameters of the life distribution.

(b) Maximize Reliability

Yield and reliability are two primary factors in semiconductor manufacturing. By using yield and reliability modeling as the foundation for developing effective stress burn-in, semiconductor manufacturers can provide high-quality products to customers. Therefore, some reliability models have been applied to obtain optimal burn-in time.

Model 1

Kim et al. [62] proposed yield loss and yield gain expressions; related them with the reliability model of semiconductor devices in order to determine the burn-in time. They assumed that the gate-oxide damage is the leading defect mechanism. The proposed expressions of yield loss, yield gain and reliability are as shown in the equations below:

$$Y_{loss} = Y\left(1 - Y^{\frac{\upsilon}{1-\upsilon}}\right) \text{ and } Y_{gain} = Y\left[Y^{-\Phi\left(\left(1/(1-\upsilon)^2\right)-1\right)} - 1\right] \tag{11}$$

$$R = Y^{\frac{1}{(1-u)^2-1}} \tag{12}$$

where υ is the damage incurred during burn-in, u is the damage incurred during operation, Φ is the ratio of the critical area to the total area and Y is the yield before burn-in.

Model 2

Barnett and Singh [63-64] identified another two important indicators to optimize yield during burn-in: (1) local region yield of the die (2) the number of

repairs performed on the die. Let $\lambda_L(t)$ be the average number of latent defects per chip, and α be the defect clustering parameter. Then the post-burn-in reliability yield can be modelled as follows:

$$R(t)=\left[1+\frac{\lambda_L(t)}{\alpha}\right]^{-\alpha} \tag{13}$$

Defining λ_K as the average number of killer defects per chip and γ as a constant on the order of 0.01-0.02, one can express the wafer probe yield, Y_K (the probability that a chip has zero killer defects), and the reliability yield, Y_L (the probability that a chip survives burn-in given that it passed wafer probe testing), as follows [65]:

$$Y_K=\left[1+\frac{\lambda_K}{\alpha}\right]^{-\alpha} \text{ and } Y_L=\left[1+\gamma\left(1-Y_K^{1/\alpha}\right)\right]^{-\alpha} \tag{14}$$

Barnett et al. [66] verified the above integrated yield-reliability model by using burn-in data from 77,000 microprocessor unit manufactured by IBM Microelectronics. In addition, Barnett et al. [67] extended the above yield-reliability model to estimate the burn-in fall-out of repaired and un-repaired memory die.

Traditionally, reliability modelling is separate from yield modelling. However, for new technologies, it is important to find the relationship between reliability and yield to predict and improve the reliability during the early production stage [68]. Unfortunately, it is impossible to obtain the explicit expression for the relationship between reliability and yield unless the defect density distribution is selected. Kim & Kuo [69-70] derived the following explicit yield-reliability relationship under 5 different defect density distributions:

$$\begin{cases} \ln R_{Poisson}(t) = \gamma_t \ln Y_{Poisson} \\ R_{negative\,binomial}^{-(1/\alpha)}(t) - 1 = \gamma_t \left(Y_{negative\,binomial}^{-(1/\alpha)} - 1 \right) \\ \ln\left(1 - 2\lambda_\gamma R_{uniform}(t)\right) = \gamma_t \ln\left(1 - 2\lambda_y Y_{uniform}\right) \\ \ln\left(1 - \lambda_\gamma \sqrt{R_{Murphy}(t)}\right) = \gamma_t \ln\left(1 - \lambda_y Y_{Murphy}\right) \\ R_{Seeds}^{-1}(t) - 1 = \gamma_t \left(Y_{Seeds}^{-1} - 1 \right) \end{cases} \tag{15}$$

where α is the defect clustering parameter, λ_y is the mean number of fatal defects in a device and λ_γ is the average number of reliability defects per device.

(c) Maximize The Percentile Life

Reliability is often defined as the probability a system operates without failure under the expected environment conditions for a predetermined mission time. However, sometimes we would like to continuous to use the system beyond the specific time. That is, the system is expected to be operational as long as it functions. For example, artificial satellites or space explorers are used for as long as they function without major failure [71]. Therefore, the objective of this situation is to maximize a measure of the system durability without a specific time period.

There are two appropriate criteria for this purpose: (1) average life and (2) percentile life. However, when the variance of a system is high, using the average life as the measure will be considerably limited [71]. Kim and Kuo [72] showed that the optimal system design for maximizing the system reliability for a mission time is, in fact, the same as the one for the maximizing the percentile life at some failure probability.

(d) Maximize The Steady State Availability

In some cases, like power supplies for a hospital or an electric security system, there are some reliability characteristics such as system availability, probability of accomplishing a mission, which are much more important than the economic consideration. The steady state availability of the system under the burn-in time *b*, is given by [73]

$$A(b) = \frac{\int_0^\infty \overline{G}_b(t)dt}{\int_0^\infty \overline{G}_b(t)dt + \left[\int_0^\infty r(b+t)\overline{G}_b(t)dt\right]\upsilon_1 + (\upsilon_2 - \upsilon_1)} \tag{16}$$

where $\overline{G}_b(t)$ and $r(t)$ denote the survival function of the time length from 0 to the first Type II failure of a burn-in system and the failure rate of a system respectively. υ_1 and υ_2 are the means of a minimal repair time and unplanned replacement caused by the Type II failure.

(e) New Indicators

Besides all the objective functions mentioned above, some studies tried to develop new criteria to determine the optimal burn-in time. Block et al. [74] considered a residual coefficient of variation that balances mean residual life with residual variance. Let X_t be the residual lifetime of the component which has survived for *t* units of time. $\mu(t)$ and $\sigma(t)$ denote the expected value and standard deviation of X_t. Then the optimal burn-in time can be obtained by minimizing the coefficient of variation defined as $CV(t) = \frac{\sigma(t)}{\mu(t)}$.

1.4.4 Summary

Burn-in is a wildly used tool to weed out the early failure. This section provides the review of the published work concerning burn-ins during these years. It is believed that there are some unpublished research performed by the industry and some published work not included because they are inadvertently overlooked or not strongly related to the topics of this review.

In the predictable future, scarcity of available data for the nano products is going to be the major issue to the statistical inference of burn-in procedure. Most of methods to determine the optimal burn-in policy in the literature nowadays are efficient only if a sufficient amount of time-to-failure data is available. Kuo [5] predicted that the Bayesian approach will be even more frequently applied in the nano era as product life cycles based on new technologies become even shorter and it is almost impossible to obtain enough data before a new product requires reliability assessment. The other way to deal with this problem is to predict reliability using the computer-aided tools, based on the physical properties of the nano systems.

CHAPTER 2

CHARGE TRAPPING AND DETRAPPING MECHENISMS FOR NANOCRYSTAL EMBEDDED HIGH-K NONVOLATILE MEMORIES

2.1 Capacitance-Voltage Characteristics

The capacitance-voltage (C-V) characteristics of the nanocrystals embedded samples are shown in Figure 8. The C-V curves were measured from the accumulation region to the inversion region and back to the accumulation region in the range of (-6V, 6V, -6V). They all show counterclockwise hysteresis behavior, which means net charges trapping in the gate dielectric structure. It is obvious that the charge storage capacity is influenced by the type of the embedded nanocrytalline material. However, the charges injection and trapping efficiencies are also related to the gate stack's physical thickness or EOT. The results show that the amount of charges trapped in nanocrystal embedded films is in the order of nc-ZnO>nc-Ru>nc-Si~nc-ITO, which was influenced by the embedded nanocrystal and the EOT of each sample, but the effects of nanocrystal and EOT cannot be directly distinguished from one to the other from Figure 8. In other words, the charge-trapping ability of each nanocrystal cannot be compared only depends on the C-V curves. To further investigate the strength of trapping charges, the relaxation behavior needs to be discussed.

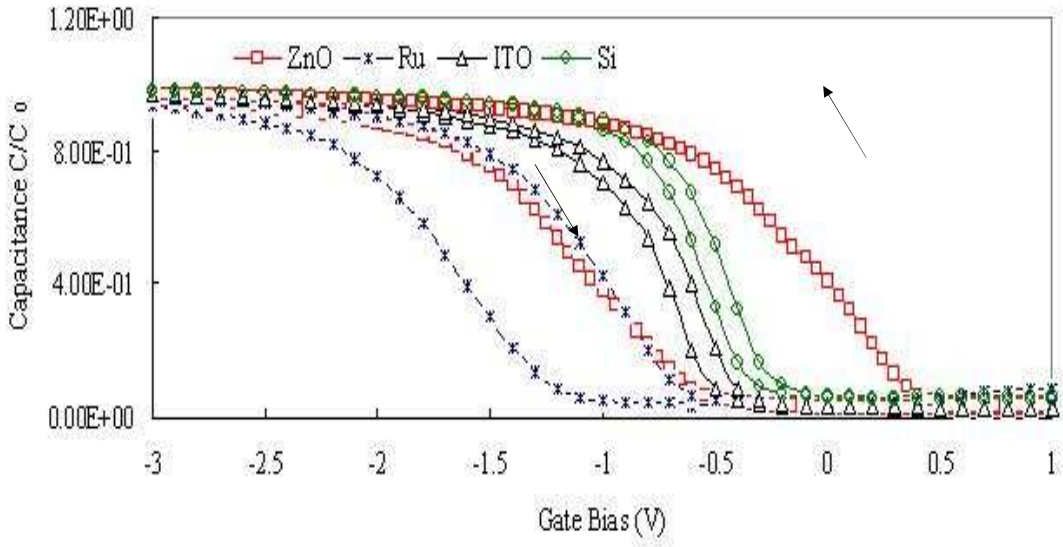


Figure 8. *C-V* curves for nanocrystals embedded ZrHfO films at -6 to 6V sweep range [103]

2.2 Relaxation Current

The leakage current ($I_{leakage}$) in this paper is defined as the current leaking through the capacitor when a gate voltage (V_g) is applied. The relaxation current (I_{relax}) is the current leaking through the capacitor after the release of an applied V_g. $I_{leakage}$ and I_{relax} are of opposite directions provided the dielectric film is intact. The reversible charge trapping at the energetically shallow site is much more pronounced in the high-*k* dielectric than in SiO_2 [75]. The I_{relax} is contributed by two mechanisms: detrapping of trapped charges and dielectric polarization/relaxation, which occur simultaneously and are difficult to differentiate [75-76].

Figures 9-11 shows the decay of the relaxation current with time of various nanocrystals embedded and control samples. Each sample was stressed at a V_g of -6V for 120 seconds and the I_{relax} was measured immediately after the removal of V_g. The I_{relax}-*t* curve of each nanocrystal embedded sample was compared with that of the corresponding control sample, since these embedded samples were prepared under different conditions. Several conclusions can be summarized from Figure 9-11. First, initial relaxation currents of nc-Ru -ITO and -Si embedded films are larger than that of their corresponding control film. However, the initial relaxation current of nc-ZnO embedded capacitor does not show the same property because of its excellent ability to trap charges deeply. Second, the I_{relax} decay rate is dependent on the embedded nanocrystalline material. Third, it takes a longer time for the I_{relax} of the embedded films (except the nc-ZnO embedded sample) to reach the final value than their corresponding control film. For nc-Ru, -ITO and -Si embedded capacitors, the charge storage capacity are much larger than that of the control samples [1, 4, 77], so the extra I_{relax} must be released from the embedded nanocrystals. However, the high I_{relax}

of the embedded film is not directly related to the amount of charges stored in the nanocrystals. For example, the initial I_{relax}'s of the nc-Ru, -ITO and -Si embedded samples were only 1.98, 1.78 and 2.04 times those of their corresponding control samples. However, their I_{relax} decay rates are not related to the initial I_{relax}'s. Figure 9-10 shows that the times required for the I_{relax}'s of the nc-Ru, -ITO and -Si embedded films to reach the same I_{relax}'s of their corresponding control samples are about 6s, 8s, 30s, respectively. Therefore, charges can be trapped to the embedded nanocrystals deeply or loosely depending on the material properties.

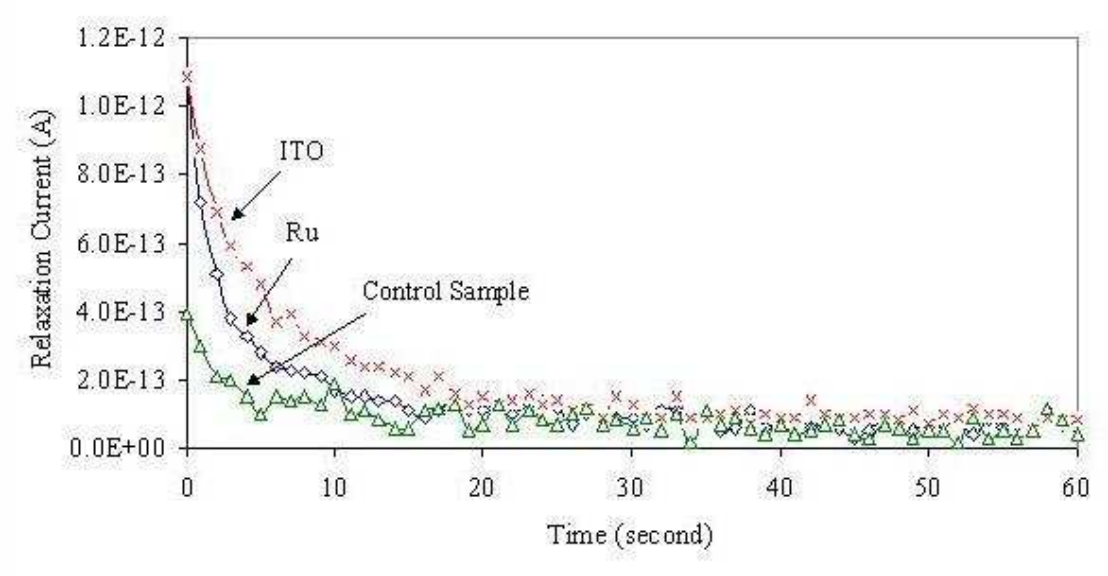


Figure 9. Relaxation current decay with time of nc-Ru and nc-ITO embedded ZrHfO films and the corresponding control sample [103-104]

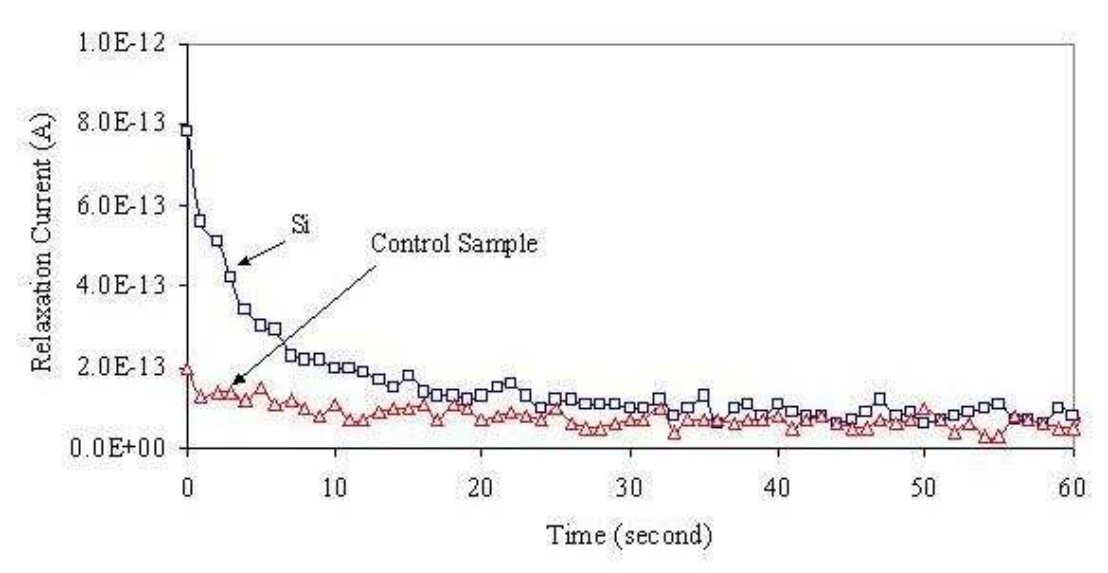


Figure 10. Relaxation current decay with time of nc-Si embedded ZrHfO films and the corresponding control sample [103-104]

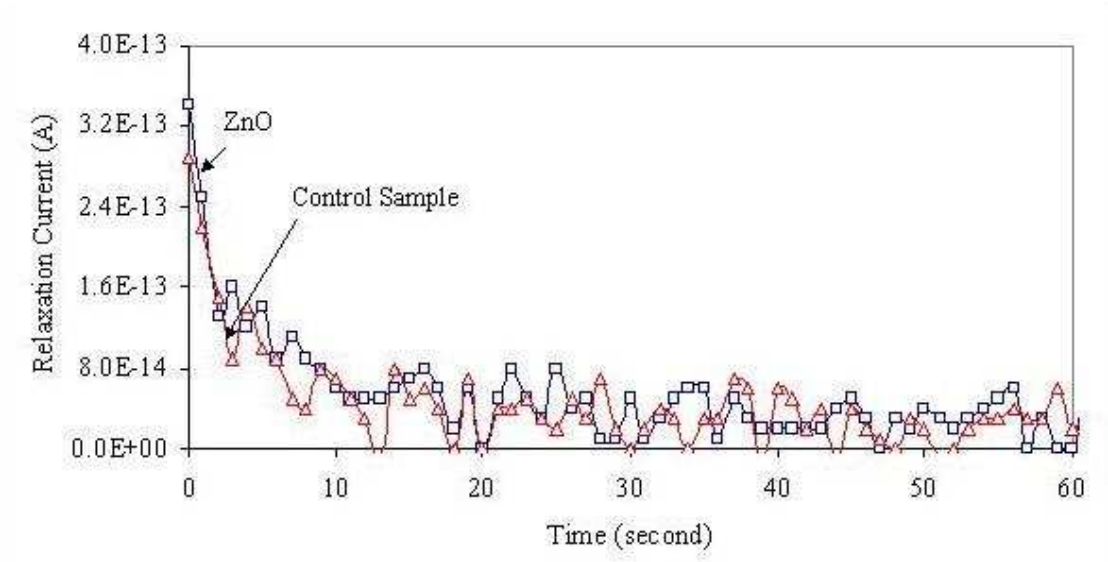


Figure 11. Relaxation current decay with time of nc-ZnO embedded ZrHfO films and the corresponding control sample [103-104]

2.3 Relaxation Current Decay Rate

The relaxation current decay rate of a dielectric layer can be expressed by the Curie-von Schweidler Law [78]:

$$J / P = at^{-n} \tag{17}$$

where J is the relaxation current density (A/cm^2), P is the total polarization or surface charge density (V • nF/ cm^2), t is time in second, a is a constant, and n is a real number between 0 and 1. Figure 12 shows the log (J/P) vs. log t of 4 kinds of nanocrystals embedded ZrHfO films as well as the non-embedded ZrHfO, SiO_2, HfO_x and TaO_x films [79]. In Figure 12, the n values of nanocystals embedded samples are much lower than 1, e.g., 0.77, 0.58, 0.54 and 0.64 for nc-Ru, -ITO, -ZnO and -Si embedded samples, respectively. These n values are not consistent with the prediction in refs. [80] and [81], which should be close to 1. In fact, the n value represents the

decreasing rate of the relaxation current. The small *n* values observed in nanocsrytal embedded capacitors indicate that the I_{relax} decreases slowly with time because the charges trapped by the embedded nanocrystals are probably stronger than those trapped by the bulk high-*k* film does. By assuming that all ZrHfO films in the embedded samples of Figure 12 have the same charge decay rate, the strength of charge holding of the nanocrystalline material decreases in the order of nc-ZnO > nc-ITO > nc-Si > nc-Ru.

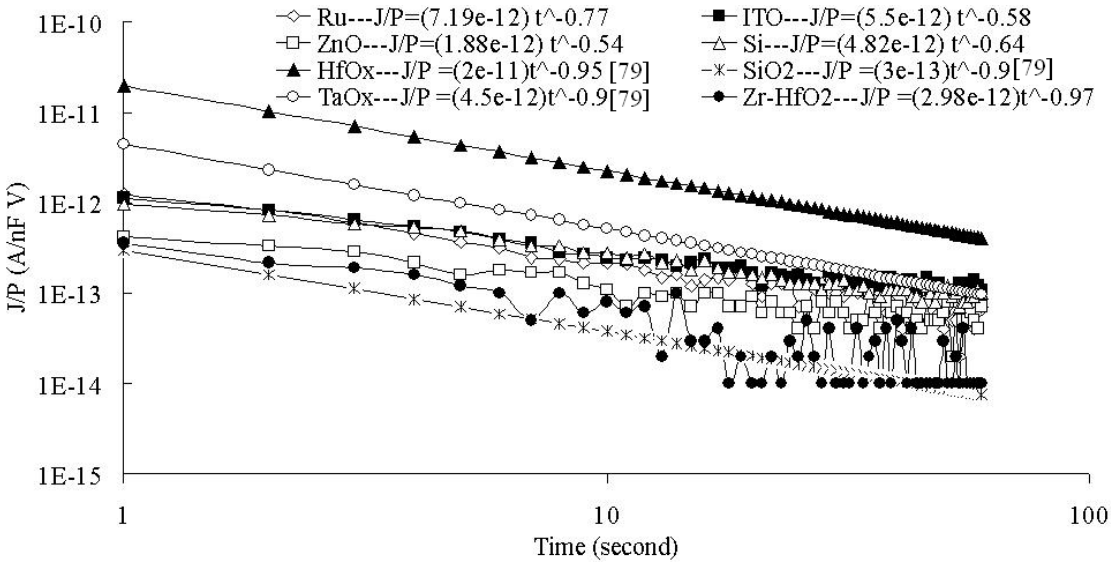


Figure 12. Relaxation current normalized to polarization vs. gate voltage release time of various embedded and non-embedded dielectrics (log-log scale) [103-104]

By using the approximation of a two-dimensional oxide sheet charge located away from the interface, the number of initial trapped charges can be estimated by [82]

$$N = \gamma \times (C_{ox} / q) \times (-\Delta V_{FB}) \tag{18}$$

where C_{ox} is the capacitance at accumulation, q is the electron charge, ΔV_{FB} is the flatband voltage shift, and γ is a correction factor, which can be estimated by the ratio of the sum of control and tunnel oxide equivalent oxide thickness (EOT) to the control oxide EOT [20]. In addition, the equations obtained in Figure 12 can be used to calculate the number of those loosely trapped charges released during a certain time period. The difference between the initial trapped and loosely trapped charges would be considered as the deeply trapped charges. Table 2 shows the percentages of deeply trapped and loosely trapped charges for 4 kinds of nanocrystal embedded samples

after the first 20 seconds. The ability to strongly hold charges is in the order of nc-ZnO > nc-Si > nc-Ru > nc-ITO.

Table 2. Percentages of deeply trapped and loosely trapped charges for nanocrystal embedded samples after the first 20 seconds [103]

nanocrystal	deeply trapped %	loosely trapped %
Ru	78.5%	21.5%
ITO	57.5%	42.5%
Si	85.8%	14.2%
ZnO	93.6%	6.4%

CHAPTER 3

BREAKDOWN MECHAISMS

3.1 Ramp-Relax Measurement

The breakdown mechanism of these embedded films can be investigated by using a ramp-relax measurement method proposed by [81]. To perform this experiment, a negative gate voltage ($-V_g$) is applied to the high-*k* MOS capacitor on a *p*-type silicon wafer. The leakage current density, J_{ramp}, is detected with the increase of $-V_g$ and the applied voltage is released for a short time and the relaxation current density J_{relax} is measured at a very small V_g, e.g., 0.1V. Repeat this procedure until the dielectric layer breaks at a large $-V_g$ (J_{ramp} increases abruptly). For a metal oxide high-*k* film, due to the polar structure of the high-*k* film, the polarity of the J_{relax} should be opposite to that of the J_{ramp} before the high-k film is broken. However, after the high-*k* stack is totally broken, the J_{relax} shows the same polarity as the J_{ramp} [83]. The polarity change of the J_{relax} was successfully used to detect the breakdown sequence of the ultra thin high-*k* stack. In this study, the ramp-relax method was used to investigate the breakdown phenomenon of the four nanocrystals embedded ZrHfO samples.

3.2 Breakdown Mechanism of Single-Layer Nanocrystal Embedded ZrHfO Thin Film

Figure 13 shows the J_{ramp}-V_g and J_{relax}-V_g curves of these capacitors. The J_{ramp}-V_g curve of each sample is composed of three sections. The first section starts from 0V to ~ -5V. In this section, the J_{ramp} increases with $-V_g$ very slightly and smoothly

because charges gradually stack in the bulk high-*k* to form a spot-connected breakdown path [84]. Once the spot-connected path is realized, the curve enters the quasi-breakdown section. In this section, the J_{ramp} increases with $-V_g$ faster and the leakage current gradually increases due to the existence of a small number of the connected paths. When the J_{ramp} jumps abruptly and becomes very large afterward because the film becomes conductive, the J_{ramp}-V_g curve comes to the third section, complete breakdown. However, the polarity of J_{relax} did not change with the breakdown of the sample, which is different from the breakdown phenomenon of the non-embedded high-*k* film [83]. This means the relaxation current still exists even after the high-*k* part of the sample becomes conductive. Since the embedded nanocrystals are conductors or semiconductors, they are more difficult to breakdown than the surrounding dielectric material. Therefore, the failure of the nanocrystals embedded high-*k* film results from the ZrHfO film. Figure 13 shows that the breakdown voltage (V_{BD}) increases in the order of nc-ITO ~ nc-Si < nc-Ru < nc-ZnO. Since these samples were prepared from different process conditions, they contain different bulk and interface layer thicknesses and properties. It is difficult to compare contributions of different nanocrystals to the breakdown strengths.

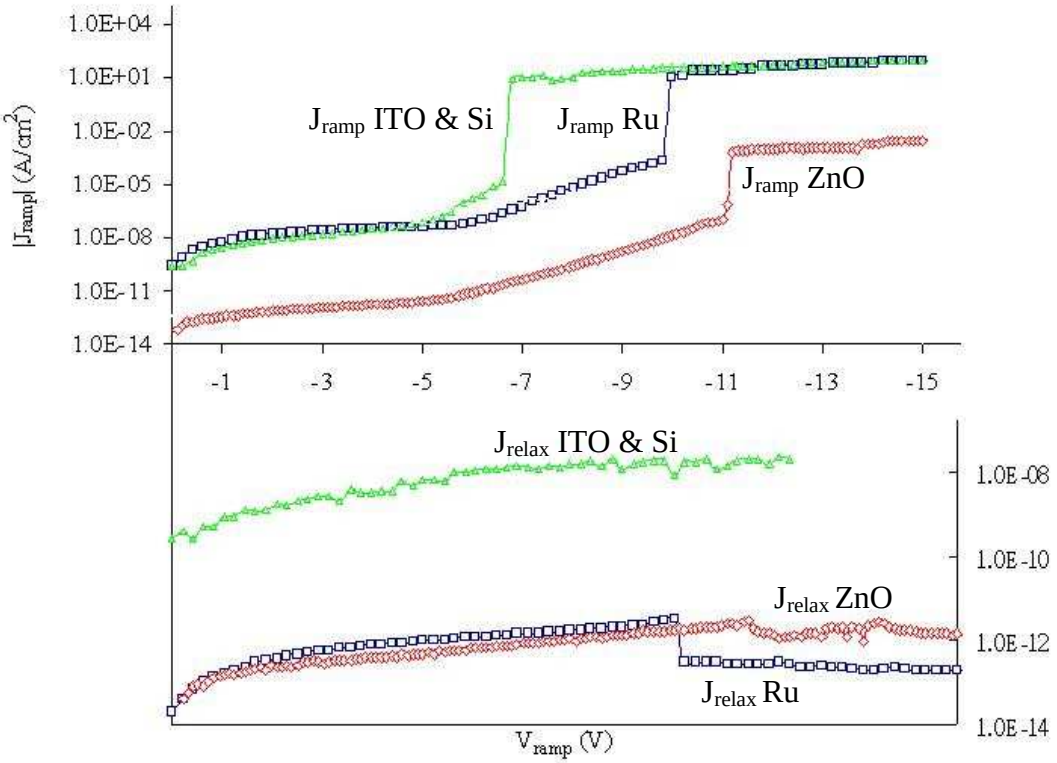


Figure 13. Ramp-relax test curves of various nanocrystals embedded high-*k* films [103]

Figure 14 shows the time-dependent dielectric breakdown (TDDB) of nc-ZnO embedded capacitors under constant voltage stress (CVS) at V_g = -9V, -8.5V, and -8V and room temperature. These capacitors break at 38s, 135s and 707s, respectively. In each test, the leakage current decreases quickly first and then very slowly. The decrease of leakage current at the beginning can be attributed to the Coulomb blockade effect due to charges trapped to nc-ZnO sites. With the increase of the stress time, charges are gradually stacked to form the spot-connected path. Eventually a conductive path is established and the leakage current increases abruptly. For the non-embedded high-k films, the capacitors fail much faster than the nanocrystals embedded capacitors, e.g., at 6s, 32s, and 80s under V_g= -9V, -8.5V, and -8V bias conditions, respectively. Here, only V_g=-8V curve is shown in Figure 5. The leakage current does not drop quickly at the beginning of the stress time, which shows the lack of the Coulomb blockade effect

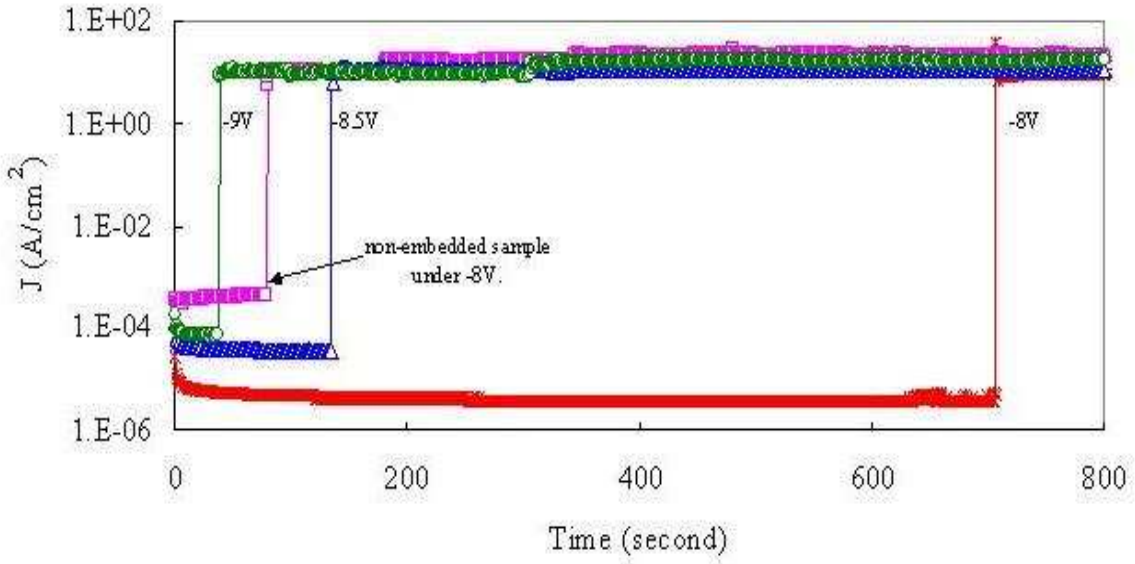


Figure 14. Time-dependent dielectric breakdown curves of nc-ZnO embedded ZrHfO high-k film stressed at different V_g's [104]

3.3 Breakdown Mechanism of Dual-Layer nc-ITO Embedded ZrHfO Thin Film

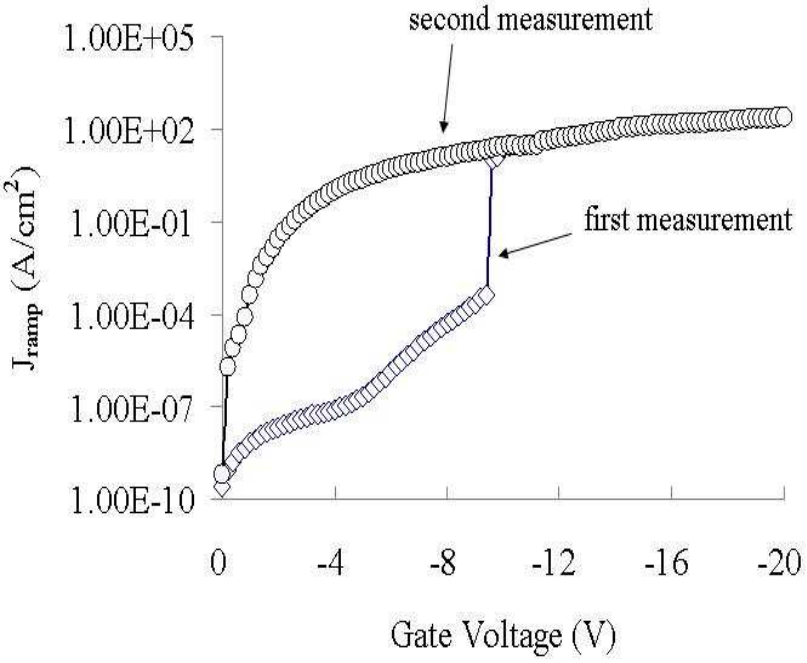
The single nc-ITO embedded ZrHfO capacitor, i.e., the tri-layer structure (ZrHfO/nc-ITO/ZrHfO) has been successfully demonstrated to have excellent holes trapping/retention characteristic. Lin and Kuo [85] also showed that the charge trapping capacity of the dual-layer nc-ITO embedded ZrHfO was more than doubled that of the dual-layer nc-ITO embedded ZrHfO. The second embedded nc-ITO layer could also improve the data programming speed. In this section, we investigated the failure mechanism of the single- and dual-layer nc-ITO embedded Zr-doped HfO_2 thin films.

The breakdown mechanism for the nc-ITO embedded high-*k* thin film can also be examined by using the ramp-relax measurement method. The two-step breakdown phenomenon was obtained in both single- and dual-layer nc-ITO embedded ZrHfO thin films. To investigate the breakdown mechanism of the nc-ITO embedded high-*k* dielectric in detail, the authors applied the ramp-relax method and performed a two-step ramp-relax measurement. First, the measurement was performed until the first breakdown was observed. Second, the measurement was repeated until a larger V_g was reached.

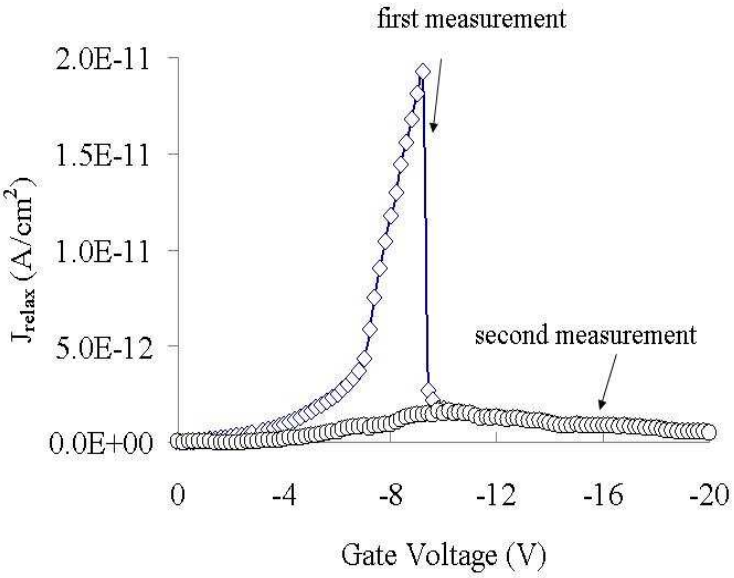
Figure 15 (a) shows the J_{ramp}-V_g curves of single-layer nc-ITO embedded capacitors under room temperature on the logarithm scale. The J_{ramp}-V_g curve from the first measurement can be composed of three sections. The first section starts from 0V to ~ -4V. In this section, the J_{ramp} increases slowly and smoothly with the increase of -V_g, because charges start to trap to the embedded high-*k* stack and the spot-connected breakdown path gradually forms [84]. Once the spot-connected path is formed, the curve enters the quasi-breakdown section [84, 86]. In this section, the

leakage current increases faster with the increase of $-V_g$ due to the existence of a small number of the connected paths. The breakdown of the high-*k* stack occurs when the J_{ramp} jumps abruptly and becomes very large afterward because the film becomes conductive [84]. The leakage current became much larger in the second measurement. This is because after the first breakdown, there existed a certain number of conductive paths in the capacitor, which resulted in the large leakage current in the second measurement. The J_{ramp}-V_g curve from the first measurement breaks at -9.5V, and there is no obvious breakdown phenomenon observed in the J_{ramp}-V_g curve from the second measurement. The J_{ramp}-V_g curve for the non-embedded sample is very similar to Figure 15 (a) with a larger breakdown voltage, i.e., at -11.8 V.

Figure 15 (a) and (b) are the J_{ramp}-V_g and J_{relax}-V_g curves from the two-step ramp-relax measurement, respectively. During the first measurement, when the breakdown occurs in the J_{ramp}-V_g curve, the J_{relax}-V_g curve drops abruptly. However, the relaxation does not change its polarity after the first and second breakdown, which is different from the breakdown phenomenon of the non-embedded high-*k* film [83]. This means the relaxation current still exists even after the high-*k* part of the sample becomes conductive. Since the embedded nc-ITO is a conductor, it's more difficult to breakdown than the surrounding ZrHfO dielectric material. Therefore, the failure of the nc-ITO embedded high-*k* film is due to the breakdown of the ZrHfO portion. For the non-embedded sample, J_{relax} changes its polarity from positive to negative after the first breakdown and keeps negative during the second measurement.



(a)

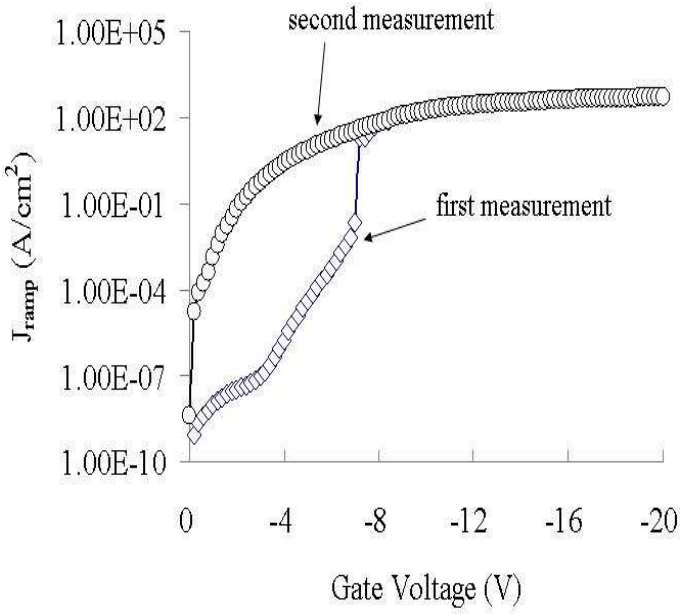


(b)

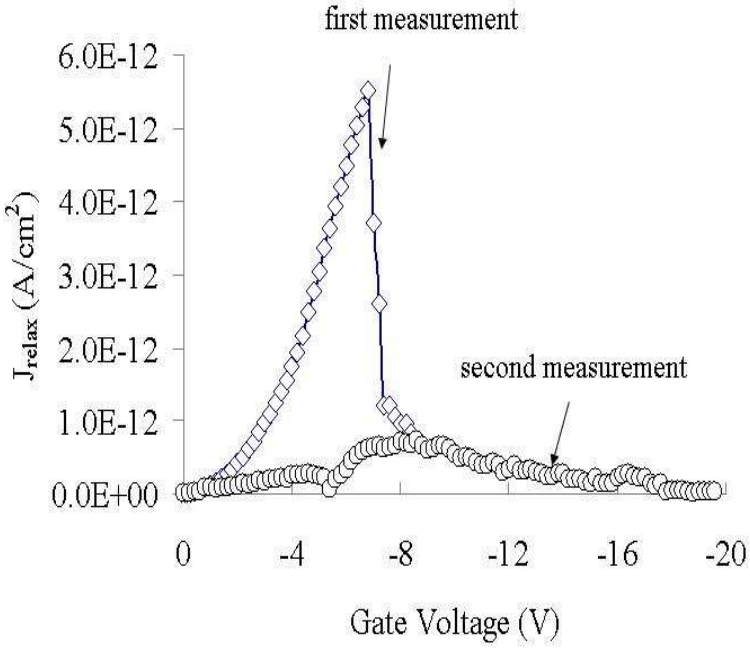
Figure 15. (a) J_{ramp}-V_g and (b) J_{relax}-V_g curves of a single-layer nc-ITO embedded ZrHfO capacitor measured with the two-step ramp-relax method [87]

The same two-step ramp-relax method was applied to the dual-layer nc-ITO embedded sample as shown in Figure 16 (a) and (b). The J_{ramp}-V_g curves are very similar to those in Fig. 16 (a) except a smaller breakdown strength, i.e., at -7.2 V. Before the first breakdown, the J_{ramp} of the dual-layer nc-ITO embedded sample is higher than that of the single-layer nc-ITO embedded sample. In other words, the addition of the extra nc-ITO layer increased the leakage current and decreased the breakdown strength because charges can pass through the dielectric portion easier.

The J_{relax}-V_g curves of Fig. 16 (b) are similar to those of Fig. 15 (b), i.e., the J_{relax} dropped sharply when the first breakdown occurred. However, the polarity did not change. The existence of the relaxation current is contributed by the nc-ITO and its interfaces.



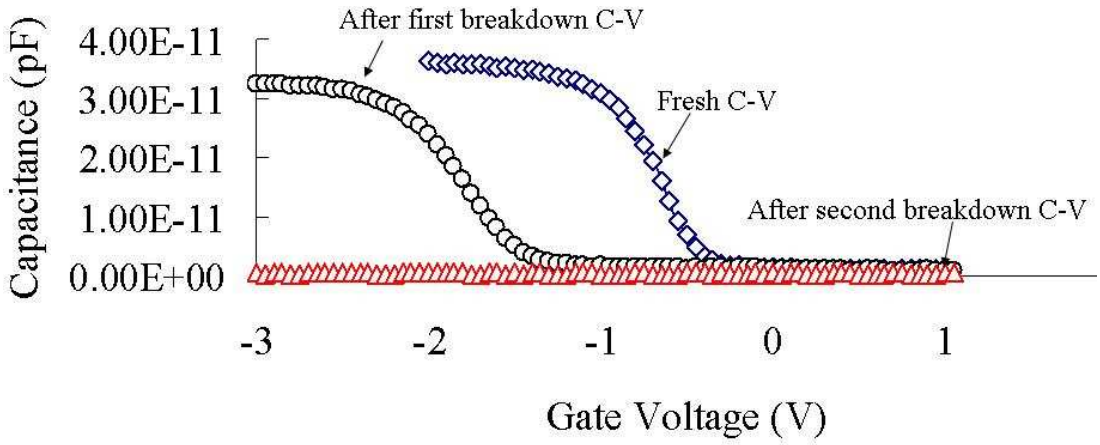
(a)



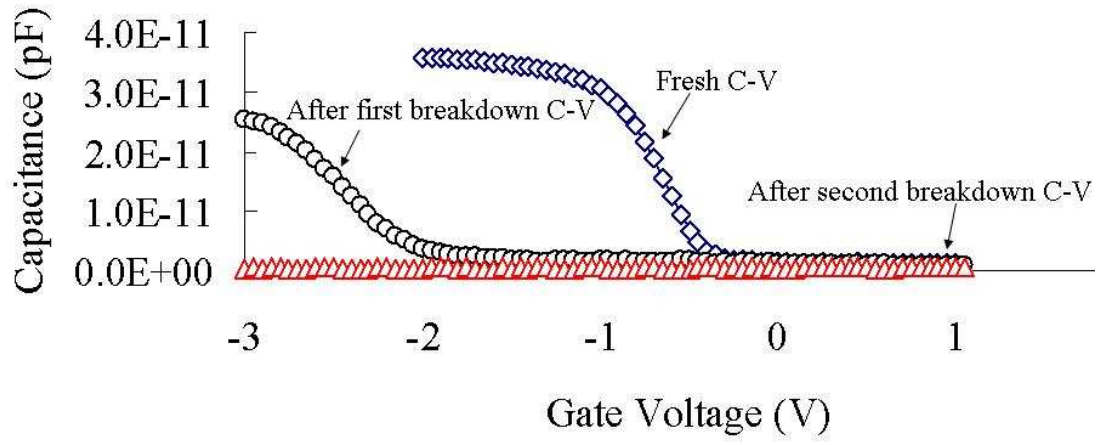
(b)

Figure 16. (a) J_{ramp}-V_g and (b) J_{relax}-V_g curves of a dual-layer nc-ITO embedded ZrHfO capacitor measured with the two-step ramp-relax method [87]

Figure 17 shows the C-V curves of the nc-ITO embedded samples under different breakdown situations. First, a fresh C-V curve was measured in a small voltage sweep range, i.e., from -2V to 1V at 1MHz. After the first and second breakdowns were detected with the two-step ramp-relax method, the corresponding C-V curves were measured from -3V to 1V at 1MHz. After the first breakdown, both the single- and dual-layer nc-ITO embedded samples still showed the dielectric characteristics except smaller capacitances than those of the fresh sample's capacitances. The existence of the dielectric property indicates that the high-*k* dielectric was not totally broken after the first breakdown. However, after the second breakdown, the whole nc-ITO embedded film became conductive and lost the capacitor's characteristics. For both nc-ITO embedded capacitors, the C-V curves shifted to the negative V_g direction after the first breakdown. This can be attributed to a large amount of holes trapped in the embedded nc-ITO site.



(a)



(b)

Figure 17. C-V curves of (a) single- and (b) dual-layer nc-ITO embedded ZrHfO capacitors before and after first and second breakdowns [87]

Figure 18 shows the time-dependent dielectric breakdown (TDDB) of nc-ITO embedded capacitors under constant voltage stress (CVS) at V_g = -6V and room temperature. The leakage current increases with the increase of the layer number of the embedded nc-ITO. The dual-layer nc-ITO embedded capacitor breaks at 4142s while the control sample and single-layer nc-ITO embedded sample does not break after 10 hours. Therefore, the accumulation of charges in the nc-ITO related sites may be responsible for the breakdown of the high-*k* stack.

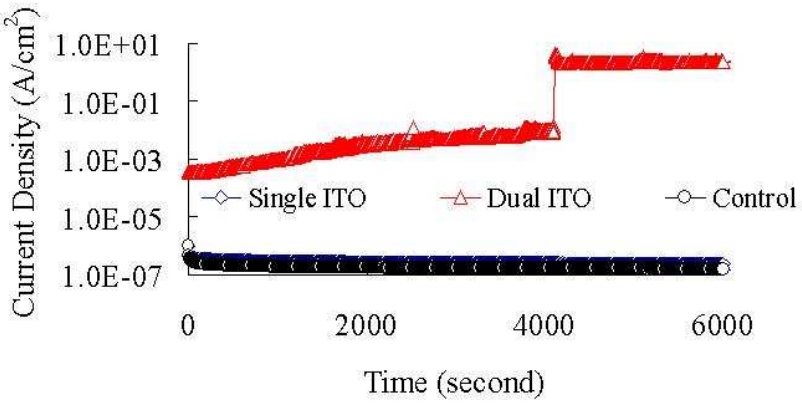


Figure 18. Time-dependent dielectric breakdown curves of single- and dual-layer nc-ITO embedded ZrHfO high-*k* film stressed at -6V [87]

CHAPTER 4

TEMPERATURE INFLUENCE ON CHARGE TRAPPING/DETRAPPING MECHANISM OF NANOCRYSTAL ZINC OXIDE EMBEEDED HIGH-K THIN FILM

The results shown in previous sections have been demonstrated that both ZrHfO/nc-ZnO /ZrHfO and ZrHfO/nc-ITO /ZrHfO tri-layer structures can trap a large number of charges with a long retention time. In addition, the nc-ZnO and nc-ITO embedded ZrHfO film had a large charge holding capability with large breakdown strength. However, most reliability studies on nonvolatile memories are done at room temperature. The influence of temperature on the memory function is important. In this chapter, authors investigated the temperature influence on some of the important reliability issues of the nc-ZnO and nc-ITO embedded ZrHfO MOS capacitor.

4.1 Temperature Influence on I-V Characteristics

4.1.1 nc-ZnO Embedded ZrHfO Capacitor

Figure 19 shows the J-V_g (leakage current density vs. gate voltage) curves of the nc-ZnO embedded ZrHfO capacitors measured from -5V to +5V at 25°C, 75°C, and 125°C, separately. The 25°C curve contains an obvious negative differential resistance (NDR) peak due to the Coulomb blockade effect [4], which can be reduced at high temperature [88-89]. In addition, Figure 19 shows the leakage current increases with the increase of the temperature when +/-V_g is large. However, the 75°C and 125°C curves do not show NDR peaks. Figure 19 also shows that for each curve,

there is a transition V_g above which the leakage current is positive and below which the current is negative. This is due to the competitive hole-trapping and -detrapping mechanism. At the large -V_g, holes are injected and retained at the nc-ZnO site while at the small -V_g, they are released back to the Si substrate [90]. The magnitude of transition V_g decreases with the increase of the temperature, i.e., -4.65V, -4V and -3.7V at 25°C, 75°C and 125°C, respectively. For the *p*-type wafer, it is easier to accumulate a larger number of high energy holes at the Si/dielectric interface and to inject them to the nc-ZnO site at the high temperature than at the low temperature, which shows up as the former's larger transition -V_g than the latter.

Figure 20 shows *J*-*V* curves of the nc-ZnO embedded capacitor under different temperatures in the log-lin scale. The gate voltage was swept from 0 to -6V in Figure 20 (a) and 0 to +6V in Figure 20 (b). Below -1.5V, a hole accumulation is formed; above 1.5V, an electron-rich inversion layer is established. The tunneling current rapidly increases at a large gate voltage (V_g). Both figures show the leakage current is not strongly dependent on the temperature. Figure 20 (a) exhibits more temperature dependence than Figure 20 (b).

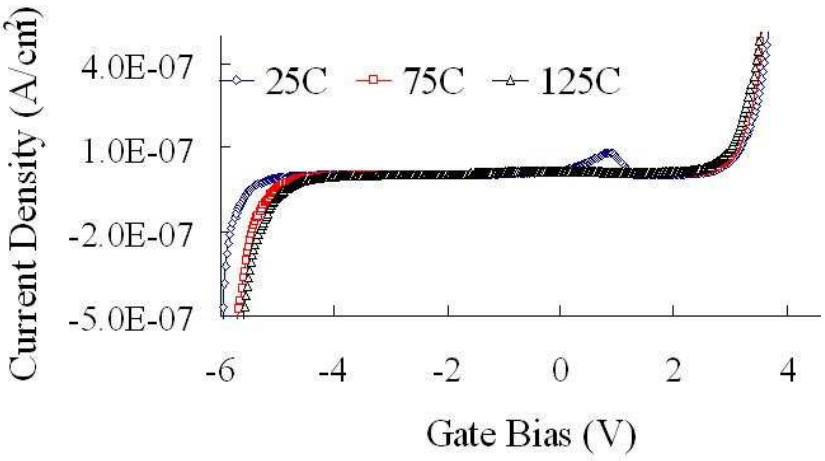
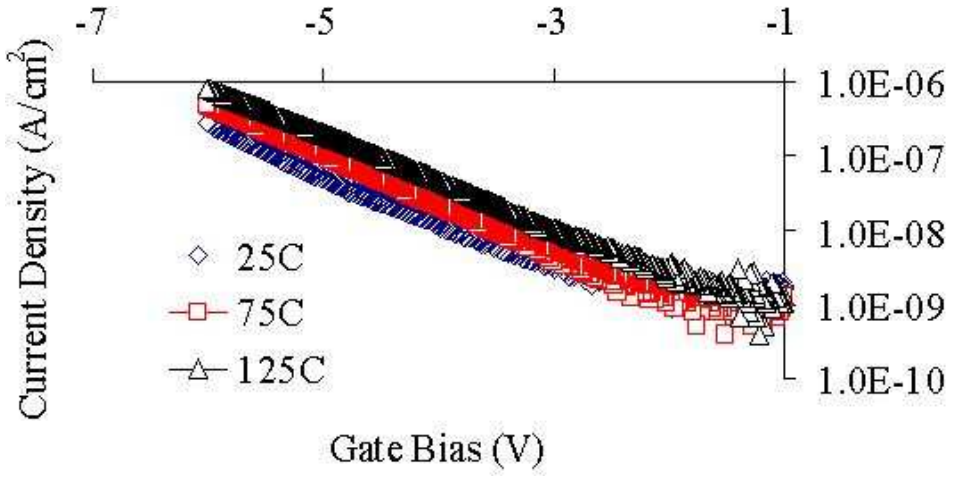
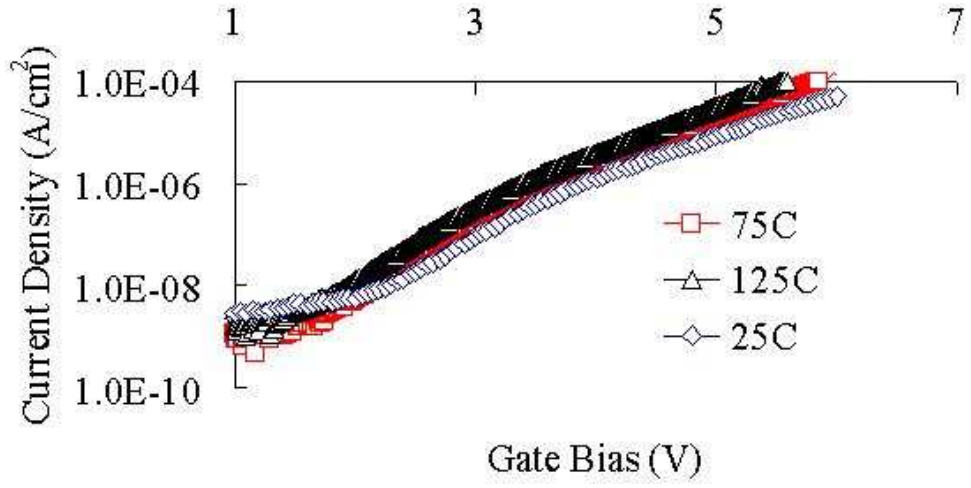


Figure 19. *J-V* curves of MOS capacitors with nc-ZnO embedded ZrHfO at 25°C, 75°C and 125°C, respectively [91]



(a)

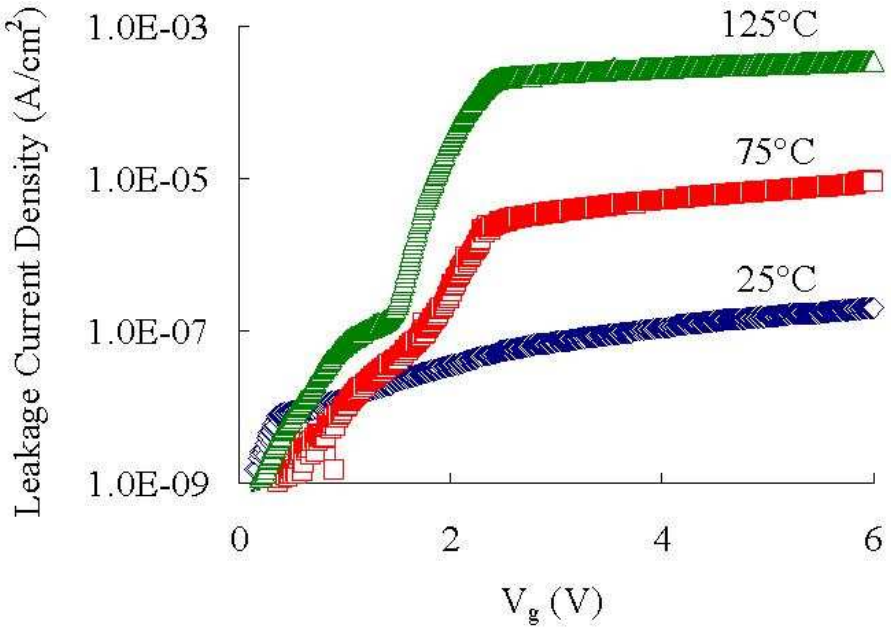


(b)

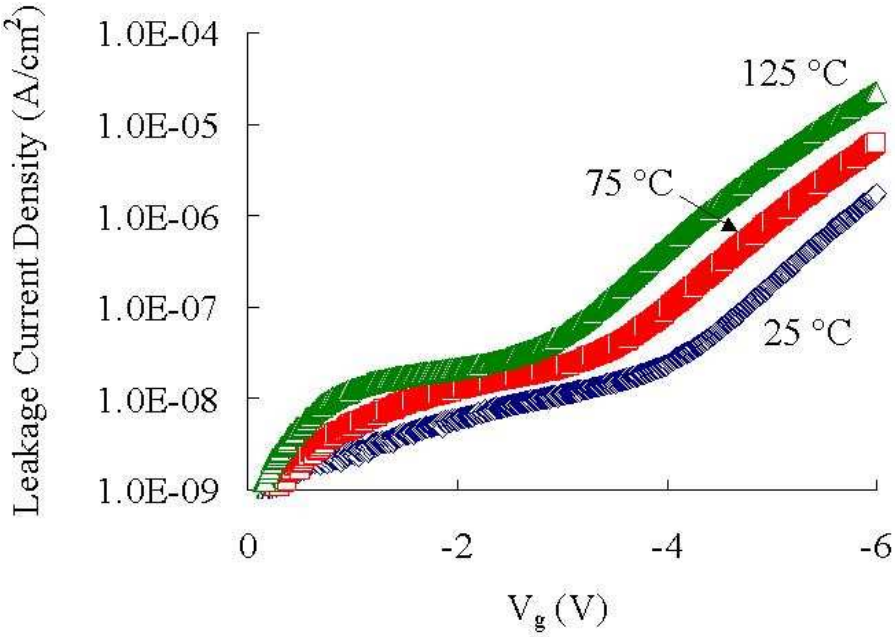
Figure 20. I-V curve of the nc-ZnO embedded MOS capacitor measured (a) from 0V to -5V and (b) from 0V to +5V [91]

4.1.2 nc-ITO Embedded ZrHfO Capacitor

The thermal effect of the charge transport mechanism of the nc-ITO embedded sample was also studied. Figure 21 shows the *J–V* curves of the nc-ITO embedded capacitor under different temperatures in the log-lin scale. The gate voltage was swept from 0 to +6V in Fig. 21(a) and 0 to -6V in Fig. 21(b). Above +2V, an electron-rich inversion layer is formed; below -3V, a hole accumulation layer is established. However, under positive gate voltage, the increase of the leakage current will be constrained by the minority carrier concentration in the inversion region for p-type Si substrate. This is because at high positive V_g, the inversion region becomes almost intrinsic and the leakage current cannot significantly increase with the increase of the gate voltage. Fig. 21(a) also shows that the increase of the leakage current will be constrained at higher V_g under higher temperature, i.e., 1.9V, 2.2V and 2.3V at 25°C, 75°C and 125°C, respectively.



(a)



(b)

Figure 21. J-V curve of the nc-ITO embedded MOS capacitor measured (a) from 0V to +6V and (b) from 0V to -6V [92]

4.2 Temperature Influence on Charge Transportation Mechanisms

4.2.1 nc-ZnO Embedded ZrHfO Capacitor

For the nanocrystal embedded HfO thin film, one of the major charge transport mechanisms is Fowler–Nordheim (F–N) tunneling [99-100], which can be expressed by the following equation [101]:

$$J \sim E_i^2 \exp\left[-\frac{4\sqrt{2m}(q\Phi_B)^{3/2}}{3qhE_i}\right] \tag{19}$$

where E_i is the electric field, m is the effective mass, Φ_B is the barrier height, q is the charge of one electron and h is the Plank constant. From the above equation, F-N tunneling is considered as temperature independent. Moreover, the F-N tunneling takes place in much lower programming voltage in ZrHfO than SiO_2. The onset of the F-N tunneling depends on the electron barrier height [99-100], and the barrier height between ZrHfO and Si is 1.5 eV, much smaller than that of SiO_2 (3.5 eV). That is, the leakage current shows little temperature dependence under positive gate voltage because the major charge transport mechanism is F-N tunneling. During the “erase state,” the barrier height becomes larger, i.e., 3.4 eV, which makes the leakage current smaller than that in the writing state. The higher barrier height can effectively suppress the charge transport with the F-N tunneling mechanism and the leakage current becomes temperature dependent earlier and more obvious than that of the writing state. In other words, under negative gate voltages, leakage current exhibits more temperature dependence since more charges will transport with the Frenkel-Poole or Schottky emission mechanism.

4.2.2 nc-ITO Embedded ZrHfO Capacitor

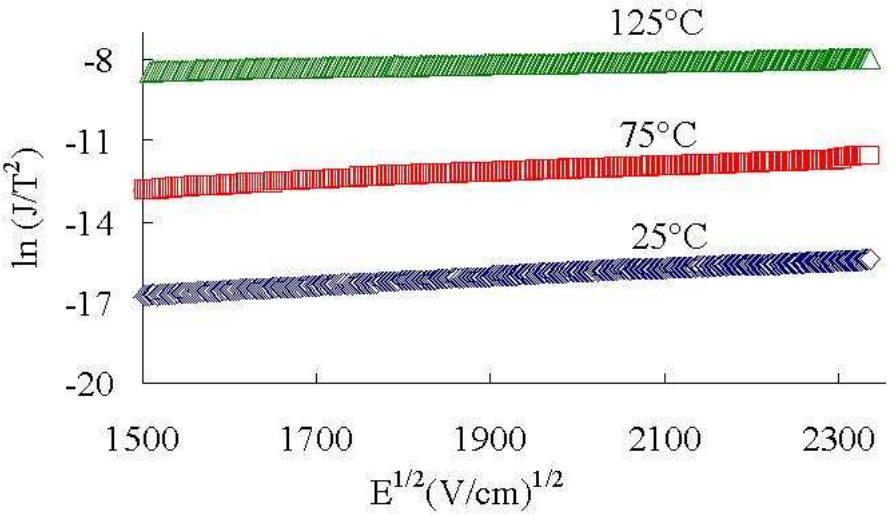
Both Figure 21(a) and (b) show that the leakage current density increases with the increase of temperature, which is consistent with the Frenkel-Poole or Schottky emission mechanism. In addition, the magnitude of the leakage current under negative bias is smaller than that of the positive bias. Since the barrier height of the hole between $HfSiO_x$ and Si is larger than that of the electron, i.e., 3.4 eV vs. 1.5 eV, the leakage current density in Fig. 21(a) is higher than that in Fig. 21(b) under the same magnitude of V_g. Previously, it was reported that the charge transports through the HfO_2 film may follow the Frenkel-Poole (F-P) mechanism or the Schottky emission as well [108-109], as shown in equation (20) and (21), respectively.

$$J \sim E \times \exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/\pi\varepsilon}\right)}{kT}\right] \tag{20}$$

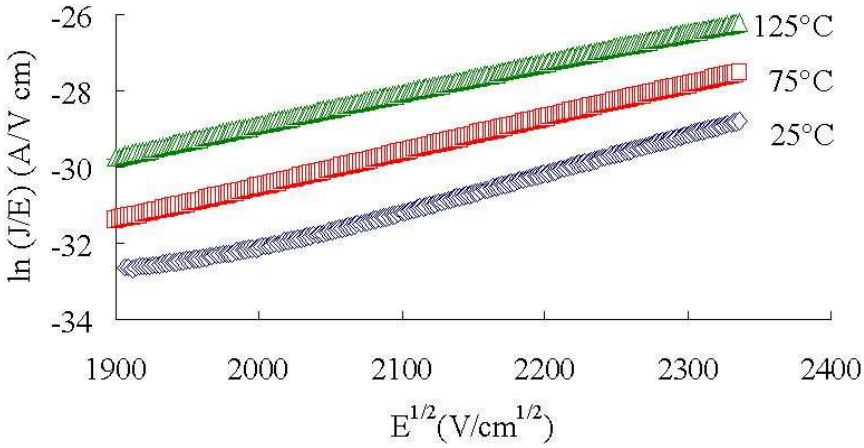
$$J = A \times T^2 \exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/\pi\varepsilon}\right)}{kT}\right] \tag{21}$$

where E is the electric field, T is the temperature, ε is the insulator dynamic permittivity, m is the effective mass, Φ_B is the barrier height, and q is the charge of one electron. From the above equations, Schottky emission mechanism is more dependent on the temperature than F-P conduction mechanism. Figure 21 (a) shows that the Schottky emission is suitable for the leakage of current under the positive V_g bias condition. Figure 21(b) shows that the F-P conduction mechanism is applicable for the negative V_g bias condition. The $\ln(J/T^2)$ vs. $E^{1/2}$ curves (Schottky emission fitting plot) and $\ln(J/E)$ vs. $E^{1/2}$ curves (F-P fitting plot) are shown in Figure 22. The result shows that the onset of the Schottky emission dominates the charge transportation mechanism at $V_g > 2.5$V. Since the $Si/HfSiO_x$ conduction band offset is

much smaller than the valence band offset, i.e., 1.5V vs. 3.4V, the Schottky emission mechanism is more pronounced than the F-P conduction mechanism under positive V_g [108]. However, under the negative V_g, the Schottky emission mechanism is overwhelmed by the F-P conduction due to the large valence band offset between Si and $HfSiO_x$.



(a)



(b)

Figure 22. (a) Fitting of Schottky relationship under the positive V_g condition and (b) fitting of the Frenkel-Poole relationship under the negative V_g condition at 25°C, 75°C, and 125°C [92]

4.3 Temperature Influence on C-V Hysteresis Characteristics

Figure 23 shows the *C-V* hysteresis curves of (a) the control sample at 25°C and the nc-ZnO embedded sample at (b) 25°C, (c) 75°C, and (d) 125°C, separately. All samples were measured from -6V to +6V, i.e., the forward sweep, and then back to -6V, i.e., the backward sweep. The control sample has a very small hysteresis, which indicates the negligible charge trapping capacity of the ZrHfO film in this sweep range. However, the nc-ZnO embedded sample shows a much larger *C-V* hysteresis. The flat band voltage difference (ΔV_{FB}) between the forward curve and the backward curve can be used as a reference of the memory window. ΔV_{FB}'s of Figure 23 (b), (c), and (d) curves are 1.24V, 1.45V, and 1.61V at 25°C, 75°C, and 125°C, separately. The corresponding charge trapping densities (Q_{ot}'s) are 3.24×10^{12}, 3.87×10^{12}, and 4.3×10^{12} cm^{-2}, respectively, estimated from the following equation:[15]

$$Q_{ot} = \frac{C_{FB} \times \Delta V_{FB}}{q} \tag{20}$$

where q is the electron charge and C_{FB} is the flatband capacitance. It has been observed that the retention efficiency of the nc-ZnO embedded ZrHfO thin film decreases with the increase of the temperature [93]. The capacitor lost 22.8%, 28.1% and 38% of originally stored charges at 25°C, 75°C and 125°C, respectively after release the stress V_g for 10,000s. These lost charges were probably loosely trapped in the embedded high-*k* layer. Otherwise, the remaining charges, which were strongly trapped, were difficult to lose unless the temperature is high.

In general, the Fermi level and the interface properties of the MOS structure are sensitive to the temperature [94]. Figure 23 (b) and (c) show that in the forward sweep direction, the *C-V* curve at 25°C almost overlaps with that at 75°C. Since the substrate is *p*-type, the location and shape of the forward sweep curve are determined

by the amount of holes trapped in the gate dielectric at the starting V_g, i.e., -6V, and the subsequent hole-release mechanism during the reduction of -V_g. The overlap of these two curves means both above processes were not affected by temperature between 25°C and 75°C. However, the slope of the *C*-*V* curve of the nc-ZnO embedded sample in the depletion region is less sharp than that of the control sample. This may be contributed by the larger interface states between the embedded ncZnO layer and the surrounded high-*k* dielectric material [95]. On the other hand, in the backward sweep direction, the 75°C curve shifts to the more positive V_g direction than the 25°C curve, which means the increase of electron trapping in the gate dielectric layer with the increase of the temperature. The high substrate temperature favours the formation of the electron-rich inversion layer and increases the kinetic energy. Both factors favour electron injection into the gate dielectric layer. Therefore, the large ΔV_{FB} of the 75°C sample compared with the 25°C sample is contributed by the increase of electron trap not hole trapping.

When the temperature is raised from 75°C to 125°C, both the forward and backward *C*-*V* sweep curves shift toward the negative V_g direction, as shown in Figure 23 (c) and (d). The negative shift of V_{FB} in the forward sweep direction is due to the increase of the number of hole trapped in the gate dielectric layer at V_g = -6V. In the backward sweep direction, the V_{FB} at 125°C is less positive than that at 75°C. This indicates the amount of electrons trapped in the gate dielectric decreases from 75°C to 125°C. It is due to the deterioration of the dielectric layer. Since all the backward curves of the ZnO embedded sample shift toward the positive V_g direction compared with that of the control sample, electrons were trapped to the gate dielectric layer at V_g = 6V independent of the previous hole trapping history during forward sweep.

Therefore, the large ΔV_{FB} of the 125°C sample is contributed by both electron and hole trapping mechanisms. Separately, the backward sweep curve of the 125°C sample in Figure 23 (d) shows an obvious shoulder from V_g = -0.4V to -1.6V in the region of weak accumulation. This is due to the existence of a set of near interface traps (NITs) whose lifetime and capture cross-section do not respond to the 1MHz measurement frequency at the lower temperature [94]. These NITs are located close to the conduction band edge and have strong influence on the mobility of the carrier in the inversion layer [94, 96].

Figure 23 (b), (c), and (d) shows that in the backward sweep direction, the capacitance of the nc-ZnO embedded sample decreases with the increase of the magnitude of $-V_g$. At V_g = -6V, the capacitances are 3.51×10^{-11}, 3.46×10^{-11}, and 2.7×10^{-11} at 25°C, 75°C and 125°C, separately. This is due to the increase of the leakage current of the gate dielectric with the increase of temperature, as shown in Figure 19, which has been discussed in detail in ref. 97.

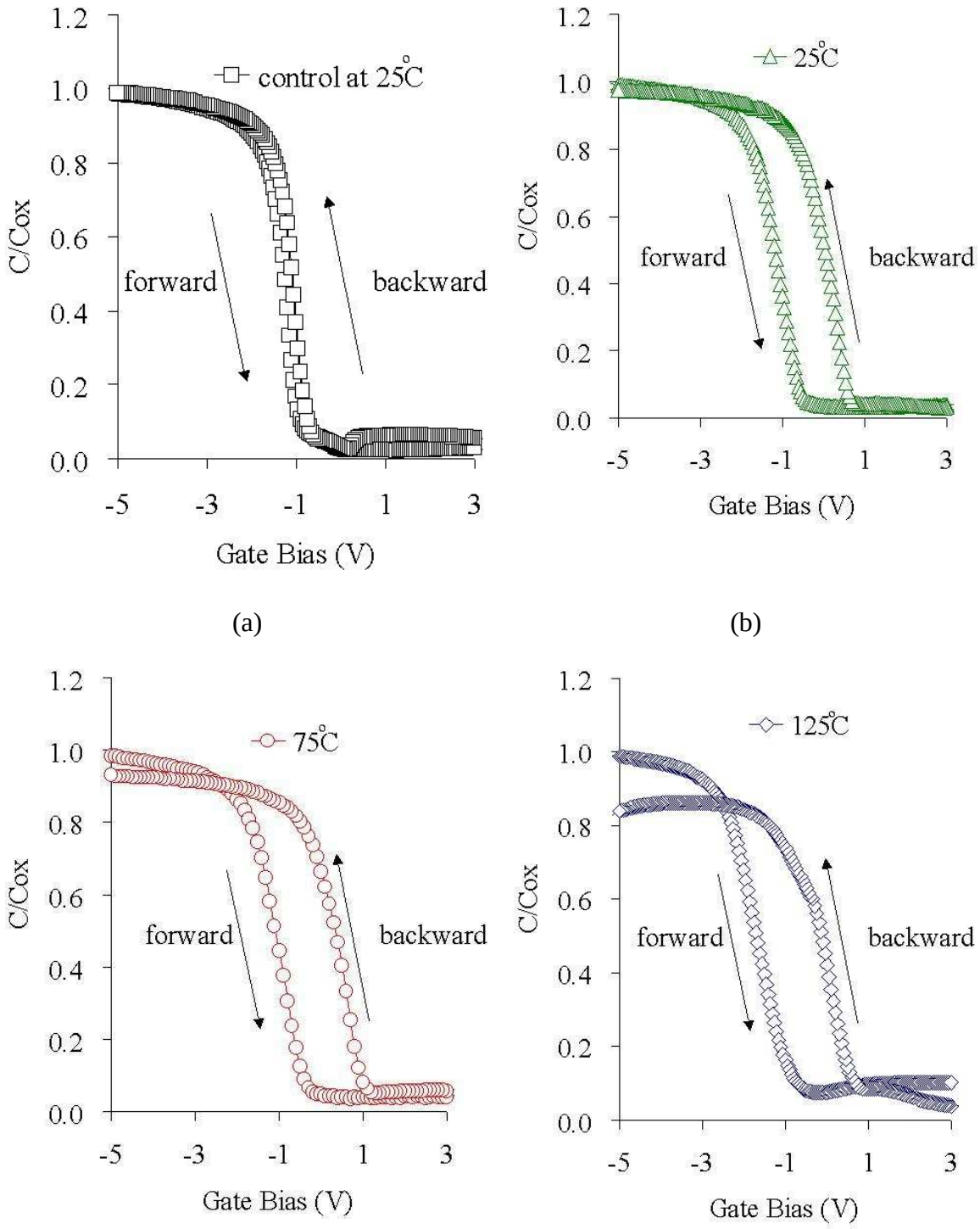


Figure 23. *C-V* hysteresis curves for (a) control sample at 25°C, (b) nc-ZnO embedded ZrHfO at 25°C, (c) nc-ZnO embedded ZrHfO at 75°C, and (d) nc-ZnO embedded ZrHfO at 125°C [91]

4.4 Temperature Influence on G-V Characteristics

The *C-V* curve shape in the depletion region is greatly influenced by the interface states, which are sensitive to the temperature. Figure 24 shows the G-V_g (conductance-gate voltage) curves corresponding to the backward *C-V* curves in Figure 23 (b), (c), and (d). The peak conductance is located at the voltage near the flat band voltage in the depletion region [98]. The peak in the conductance curve is due to the slow carrier capture rate of the embedded nc-ZnO, which comes from the reduction of the minority carrier density at the Si/tunnel ZrHfO interface. The embedded nc-ZnO cannot keep pace with the measurement frequency of 1MHz, which results in the energy loss. Thus, the conductance peak and the largest energy loss occur at the flat band voltage. For the 125°C *C-V* curve, there is a valley at V_g = -0.75V, which corresponds to the lowest conductance point. It does not occur in the lower temperature curves because the NITs are more responsive to the measurement frequency at the high temperature [98]. The hump at V_g = 0.8 V in the 125°C G-V_g curve is contributed by the interface states. Figure 24 also shows that when the V_g is lower than V_{FB}, the conductance of the capacitor increases with the temperature. This is consistent with the trend of leakage current change with temperature in Figure 19.

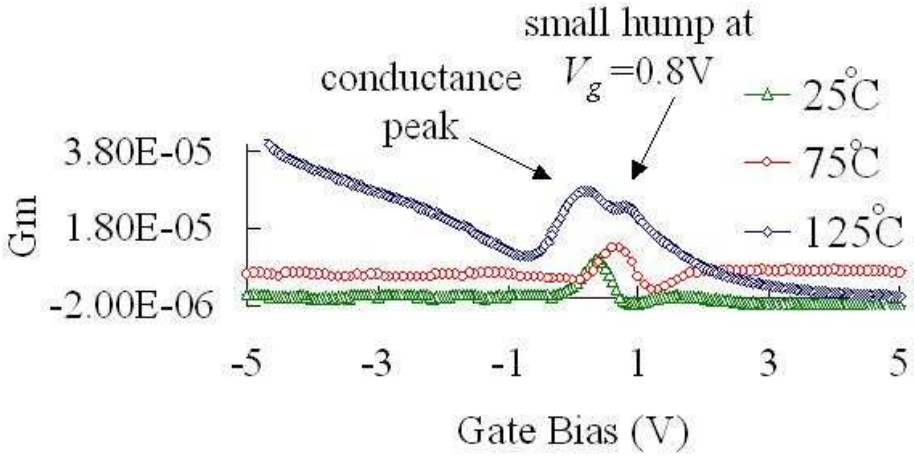


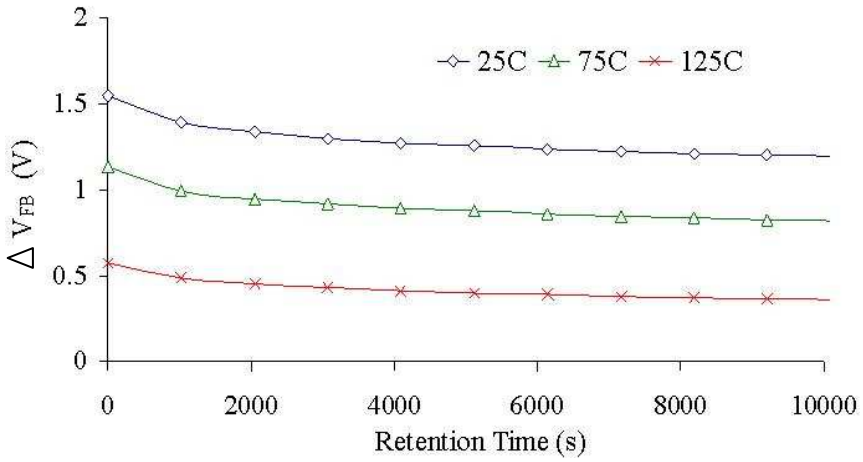
Figure 24. *G-V* curves of capacitors in the backward sweep direction at 25°C, 75°C and 125°C, respectively [91]

4.5 Temperature Influence on Charge Retention Efficiency

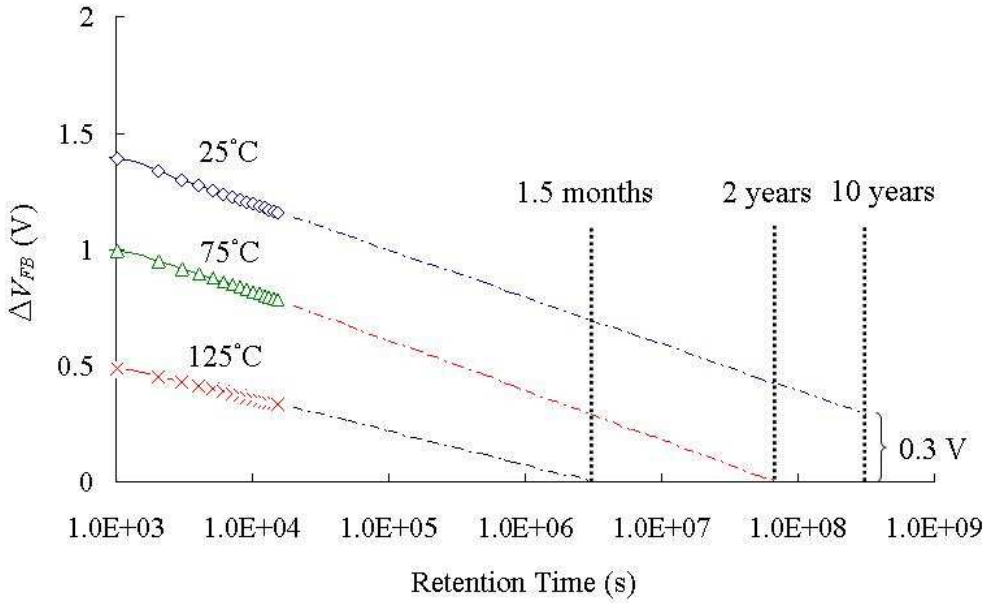
4.5.1 nc-ZnO Embedded ZrHfO Capacitor

The charge retention efficiency of the nc-ZnO embedded capacitor was studied with the following method. First, a V_g was applied to the capacitor for a period of time to trap charges to the dielectric structure. Second, after releasing the V_g, the *C-V* curve was measured in a small V_g range, i.e., -2V to +1V. Third, the *C-V* measurement step was repeated every 1000s. Only negligible charges were injected into or removed from the capacitor during the *C-V* measurements because of the small V_g range. The flat band voltage, V_{FB}, calculated from the *C-V* curve reflects the capacitor's charge retention state

The flat band voltage shift can be expressed as a function of the retention time (*t*), as shown in Figure 25 (a). The electron charge-retention characteristics of the nc-ZnO embedded capacitor were measured at different temperatures after +6V, 90s "write" stress. The magnitude of the charge storage decreased with the increase of temperature. This can be attributed to electron-trapping possibilities at the nc-ZnO layer reduces due to the increased electron thermal energy at elevated temperature [102]. In addition, the dielectric's conductance increases with the increase of temperature, which also can contribute to the leakage of the stored charges to the Si wafer. After 10,000 s, the capacitor lost 22.8%, 28.1% and 38% of originally stored charges at 25°C, 75°C and 125°C, respectively. Figure 25 (b) shows the same figure as Figure 25 (a) but the time is on the logarithm scale. The result shows that the nc-ZnO embedded ZrHfO high-*k* film will gradually lose the nonvolatile property as the temperature increases. In other words, the electron-trapping capability for the embedded nc-ZnO decreases with the increase of the temperature.



(a)



(b)

Figure 25. (a) Charge retention characteristic of ZnO embedded high-*k* thin film under different temperatures, (b) same as (a) with time on the logarithm scale [93]

4.5.2 nc-ITO Embedded ZrHfO Capacitor

The temperature effect on the charge retention efficiency of the nc-ITO embedded capacitor was studied with the following method. First, a gate bias (V_g) was applied to the capacitor for a period of time to trap charges to the dielectric structure. Second, after releasing the V_g, the *C-V* curve was measured in a small V_g range, i.e., -2V to +1V. Third, the *C-V* measurement step was repeated every 1800s. Only negligible charges were injected into or removed from the capacitor during the *C-V* measurement because of the small V_g range. The flat band voltage, V_{FB}, was calculated from the *C-V* curve to reflect the capacitor's charging state. The flat band voltage shift (ΔV_{FB}), which is defined as V_{FB} (after stress release for a period of time) - V_{FB} (before stress), is expressed as a function of the time (t), as shown in Figure 26 (a) after releasing the 1s V_g = -8V stress conditions at different temperatures. First, the magnitude of the memory window increases with the increase of the temperature, i.e., 0.64V, 1.14V, and 1.21V at 25°C, 75°C, and 125°C, respectively. In contrast, the control sample has negligible memory windows, e.g., ΔV_{FB} =0.03V and 0.3V at 25°C and 75°C, respectively under the same sweeping conditions. All trapped charges in the control sample were lost after 28 hours at 75°C. The initial increase of the memory window in the nc-ITO embedded sample is mainly due to the change in the Fermi level and the interface properties. Compared with the room temperature stress condition, the elevated temperature provides the additional energy to holes to overcome the barrier height for easier reaching the nc-ITO site. The ΔV_{FB} - t curves in Fig. 26 (a) is consisted of two sections: quick loss of charges at t < 3600 seconds followed by the slow loss of the remaining charges after a long period of time. The first section is due to the detraping of the loosely trapped charges; the second section

is due to the release of the strongly trapped charges. The initial charge decay rate and the loss of the trapped charges increase with the increase of temperature, i.e., 27.6%, 45.7% and 71.5% at 25°C, 75°C and 125°C, respectively after one hour. After 10 hours, the capacitor lost 34.8%, 64% and 92% of the total trapped charges at 25°C, 75°C and 125°C, respectively. This is because the conductance of the dielectric material increases with the increase of the temperature, which facilitates the leakage of the charges to the Si wafer. Therefore, temperature not only influences those loosely-trapped but also strongly-trapped charges. Figure 26 (b) shows the same data as Fig. 26 (a) but with the time on the logarithm scale extrapolated lifetime. At 25°C, 61% of the stored charges were lost after 10 years. However, at high temperatures, the loss of the charge increased drastically. For example, at 75°C, all stored charges were lost after 270 days and at 125°C the time was shortened to 1.67 days.

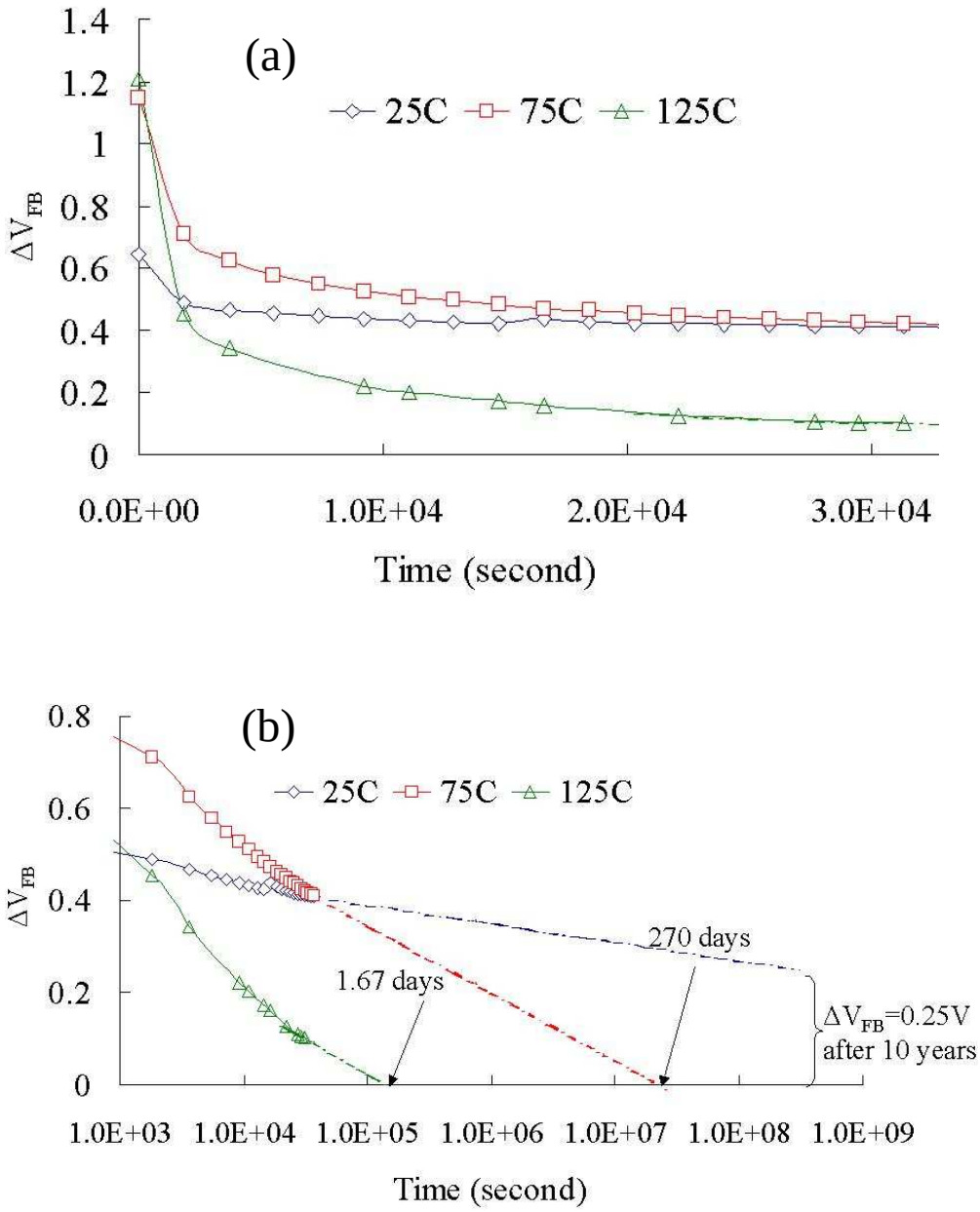


Figure 26. (a) Charge retention characteristic of nc-ITO embedded high-k thin film under different temperatures, (b) same as (a) with time on the logarithm scale [92]

4.6Temperature Influence on the Breakdown Mechanism

The thermal effect of breakdown mechanism for the nc-ZnO embedded high-*k* thin film can also be examined with the ramp-relax measurement method. Here, authors applied the same ramp-relax method to investigate the breakdown phenomena of nc-ZnO embedded high-*k* capacitors at different temperatures. Figure 27 shows the J_{ramp}-V_g and J_{relax}-V_g curves of capacitors at 25°C, 75°C, 125°C and 175°C. The 25°C J_{ramp}-V_g curve is composed of three sections. First, the J_{ramp} increases slowly and smoothly with the increase of -V_g from 0V to -5V. In this region, charges start to trap to the embedded high-*k* stack and at the same time, the spot-connected breakdown path gradually forms [84]. In the second section, the quasi-breakdown initiates where spot-connected paths begin to be realized [84, 86]. In this section, the leakage current increases faster with the increase of -V_g due to the existence of a small number of the connected paths. In the third section, the complete breakdown occurs after the film becomes conductive and the J_{ramp} becomes very large. Compared with the 25°C J_{ramp}-V_g curve, the smooth transition of the curve in section 1 at 75°C or 125°C is not obvious, i.e., ends before -2 volt. The short period of the smooth section shows that the increase of temperature provides enough energy for charges to form the spot-connected path fast.

The breakdown strength, V_{BD}, of the capacitor can be identified with the abrupt jump of the J_{ramp}. Nc-ZnO embedded ZrHfO high-k thin film has been demonstrated to have a larger V_{BD} than the non-embedded ZrHfO sample [103-104]. Moreover, the breakdown strength of the nc-ZnO embedded sample is dependent on the temperature, e.g., in the order of 25°C, 75°C, 125°C, and 175°C. The J_{ramp}– V curves exhibit no temperature dependence at small gate voltages because a hole

accumulation layer is formed. At higher gate voltages, more charges transport through the Frenkel-Poole or Schottky emission, which makes the leakage current more temperature dependent. Since ZnO is semiconductor, it is more difficult to breakdown than the surrounding dielectric material. Therefore, the failure of the nc-ZnO embedded high-*k* film at room temperature is from the breakdown of the bulk ZrHfO [103-104].

The change of the polarity in J_{relax} is dependent on the temperature. This is different from the breakdown phenomenon of the non-embedded high-*k* film. When the non-embedded ZrHfO stack breaks down, the polarity of J_{relax} will change immediately. However, the polarity of the J_{relax} does not change after breakdown of the nc-ZnO embedded high-*k* film, which means the nc-ZnO is not broken. This phenomenon occurs at 25°C. At 75°C, the J_{ramp}-V_g curve breaks at -10.1 V while the polarity change in the J_{relax}-V_g curve occurs at -18.3 V. At 125°C, the J_{ramp}-V_g curve breaks at -9.2 V while the polarity change in the J_{relax}-V_g curve occurs at -12.7 V. Eventually, at 175°C, the J_{ramp}-V_g curve breaks at the same V_g as that of the polarity change in the J_{relax}-V_g curve, i.e., -6.8 V. Therefore, the nc-ZnO breakdown requires a much larger V_g than that of the bulk high-*k* film. The difference between the two breakdown V_g's decreases with the increase of the temperature. When the temperature is high enough, e.g., 175°C, the nc-ZnO and the bulk high-*k* break at the same V_g.

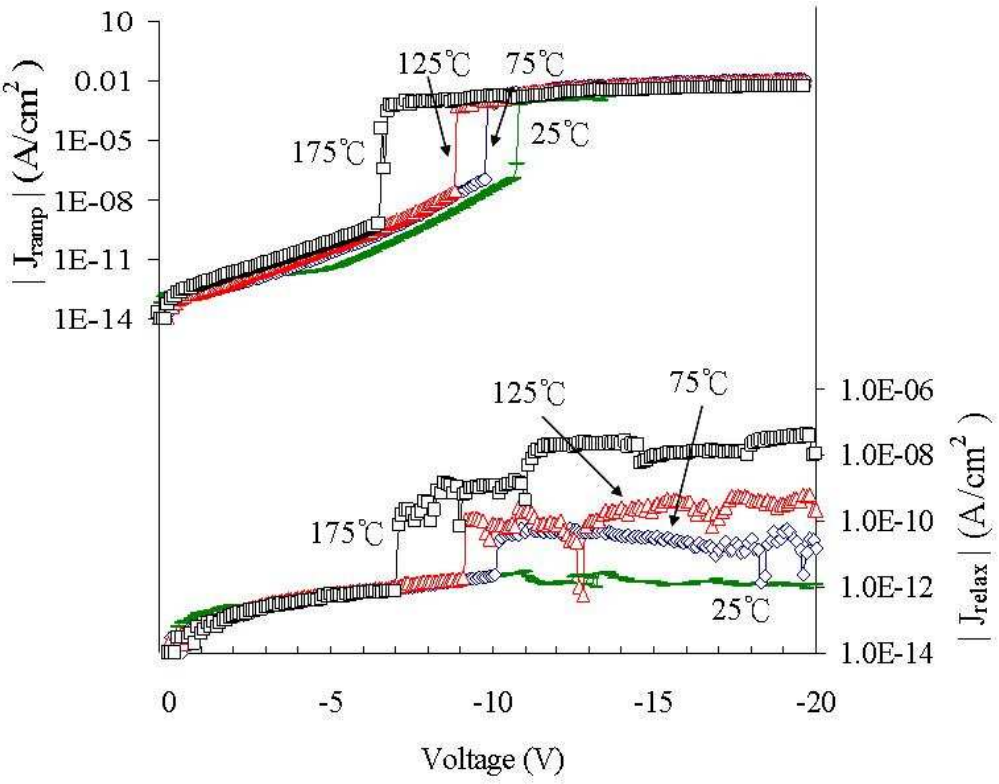


Figure 27. J_{ramp}-V_g and J_{relax}-V_g curves at different temperatures [93]

CHAPTER 5

OPTIMAL BURN-IN TIME

In this section, the optimal burn-in time of the nc-ZnO embedded high-k device is obtained. Burn-in is a widely used method to weed out the defect items before the product is shipped to the customer. To perform the burn-in process, items are put on an accelerated life test for a certain time period *b*, called the burn-in period. Those that survive the burn-in process can be released for field use. The burn-in time *b* can be determined by some criterion. Many researches applied different objective functions for optimization and then showed that an optimal burn-in time, b^*, indeed existed. Minimal cost is the most widely used objective function to determine the optimal burn-in time for IC devices, and more and more cost factors have been considered, such as repair cost, replacement cost and warranty policies. However, in the nano era, the calculation of these cost factors will become more difficult because of the short product life cycle and limited data. Yield and reliability, on the other hand, are two primary factors in semiconductor manufacturing. By using yield and reliability modeling as the foundation for developing effective stress burn-in, semiconductor manufacturers can provide high-quality products to customers. Therefore, some reliability concepts have been applied to obtain optimal burn-in time. In this study, the optimal burn-in times were obtained under two objective functions: 1. maximize the reliability with a given mission time, proposed by Mi [105], and 2. achieve the mission reliability.

5.1 Hazard Rate Function Estimation

It is widely believed that many products, particularly silicon integrated circuits, exhibit bathtub-shape failure rate function. Traditional bathtub-shape curve divided the component life into three stages. The first stage is known as infant mortality period. In this stage, we have a decreasing failure rate (DFR). The second stage is called the normal operating life. In this stage, we have a constant failure-rate period (CFR). The last stage is a period of wearout with an increasing failure rate (IFR) because of aging.

Consider the simple n right censored survival data $\{(X_j, \delta_j); 1 \le j \le n\}$, where X_j is the time that the jth individual was last seen and $\delta_j = \begin{cases} 1, & \text{failed} \\ 0, & \text{censored} \end{cases}$. To find the approximation of the hazard rate function, the non-parametric Bayesian approaches proposed by Arjas and Gasbarra [8] was applied:

The hazard rate function, $\{\lambda_t; t \ge 0\}$, was defined as a simple jump process structure:

$$\lambda(t) = \sum_{i \ge 0} 1_{\{T_i < t \le T_{i+1}\}} \lambda_i \tag{21}$$

where $1_{\{\}}$ is the indicator function, $0 < T_1 < T_2 < \ldots$ is an increasing sequence of jump times and $\lambda_i > 0$ are the corresponding levels of the piecewise constant hazard rate. T_1, T_2, … form a time-homogeneous Poisson process with parameter μ, $\lambda_0 \sim Gamma(\alpha_0, \beta_0)$ and $\lambda_i \sim Gamma(\alpha, \beta_i), \beta_i = \frac{\alpha}{\lambda_{i-1}}$.

Let $\left\{\left(T_k^i, \lambda_k^i\right),\ 0 \le k \le m_i\right\}$ be the value of $\left(T_k, \lambda_k, m\right)$ after the ith iteration, where m is the number of jumps in the hazard rate. Then we can sample from the following distributions [8]:

$$\begin{aligned} T_k^{i+1} \sim\ & p\left(T_k \mid T_0^{i+1}, \lambda_0^{i+1}, ..., T_{k-1}^{i+1}, \lambda_{k-1}^{i+1}, \lambda_k^i, T_{k+1}^i, \lambda_{k+1}^i, ..., T_{m_i}^i, \lambda_{m_i}^i, \text{data}\right) \\ & \propto \exp\{-Y\left(T_{k+1}^i\right)\left(\int_{T_{k-1}^{i+1}}^{T_k} \lambda_{k-1}^{i+1} ds + \int_{T_k}^{T_{k+1}^i} \lambda_k^i ds\right) \\ & - \sum_{X_j \in (T_{k-1}^{i+1}, T_{k+1}^i]} \int_{T_{k-1}^{i+1}}^{X_j} \lambda_{k-1}^{i+1} ds - \sum_{X_j \in (T_{k-1}^{i+1}, T_{k+1}^i]} \left(\int_{T_{k-1}^{i+1}}^{T_k} \lambda_{k-1}^{i+1} ds + \int_{T_k}^{T_{k+1}^i} \lambda_k^i ds\right) \\ & - \int_{T_{k-1}^{i+1}}^{T_k} \mu ds + \int_{T_k}^{T_{k+1}^i} \mu ds\} \times \left(\lambda_{k-1}^{i+1}\right)^{\#\left\{X_j \in (T_{k-1}^{i+1}, T_k\ ], \delta_j = 1\right\}} \times \left(\lambda_k^i\right)^{\#\left\{X_j \in (T_k\ , T_{k+1}^i], \delta_j = 1\right\}} \times \mu^2 \end{aligned} \tag{22}$$

and

$$\begin{aligned} \lambda_k^{i+1} \sim\ & p\left(\lambda_k \mid T_0^{i+1}, \lambda_0^{i+1}, ..., T_{k-1}^{i+1}, \lambda_{k-1}^{i+1}, T_k^{i+1}, T_{k+1}^i, \lambda_{k+1}^i, ..., T_{m_i}^i, \lambda_{m_i}^i, \text{data}\right) \\ & \propto Gamma\left(\lambda_k; \alpha, \beta_k^{i+1}\right) \times Gamma\left(\lambda_{k+1}^i; \alpha, \frac{\alpha}{\lambda_k}\right) \times \left(\lambda_k\right)^{r_k} \\ & \times \exp\left\{-Y\left(T_{k+1}^i\right) \times \int_{T_k^{i+1}}^{T_{k+1}^i} \lambda_k ds - \sum_{X_j \in \left(T_k^{i+1},\ T_{k+1}^i\right)} \int_{T_k^{i+1}}^{X_j} \lambda_k ds\right\} \end{aligned} \tag{23}$$

where $Y(t) = n - \sum_{j=1}^{n} 1_{\{X_j < t\}}$ is the number of the individuals at risk at time t, $\#A$ denotes the cardinality of set A, and $r_k = \sum_{T_k^{i+1} < X_j < T_{k+1}^i} \delta_j$. Then a good approximation of the hazard rate function can be obtained from the above algorithm.

5.2 Accelerated Life Test

The modern products nowadays are designed to operate for years without failure. Estimating the time-to-failure distribution or long-term performance of the component becomes very difficult. Only few units will fail during the test at normal use conditions. Thus, accelerated life tests (ALTs) are used wildly in industries to obtain the reliability data of the product. ALTs are usually performed under high levels of stress, such as high temperature, voltage or pressure. The burn-in process in this study was a voltage stress accelerated life test. To collect the time-to-failure data, the constant voltage stress tests were performed on the nc-ZnO embedded ZrHfO capacitor. The accelerated voltage stress was 7.5V. In the CVS tests, the jump of leakage current at the moment of breakdown can be clearly identified. To estimate the lifetime of the product with the accelerated life test, the acceleration factor needs to be obtained. Assuming that voltage dependence of the device lifetime follows exponential law, the voltage acceleration factor (AF_v) can be expressed by Qin and Bernstein [106]:

$$AF_v = e^{[\gamma(V_A - V_O)]} \tag{24}$$

where γ is the acceleration coefficient, V_A is the accelerated voltage and V_O is the operating voltage. In this research, $\gamma = 7$ is chosen based on the results from Qin [106] and Wu [107]. Then the acceleration factor can be calculated as $AF_v = e^{[7(7.5-6)]} = 36315.5$. In other words, one hour in the burn-in process equals 36315.5 hours under normal operation conditions.

5.3 Optimal Burn-In Time

In this section, the hazard rate function will be estimated based on the model discussed in the previous section. The lifetime data were obtained from the nc-ZnO embedded ZrHfO nonvolatile memory prepared by Thin Film Nano & Microelectronics Research Laboratory. The memory device was stressed under a constant voltage stress i.e., 7.5V for 15,000 seconds and the leakage current was measured every second. The failure was defined as the abrupt increase of the leakage current. The typical J-t curve of the lifetime test is shown in Figure 28. In each lifetime test, the leakage current decreased quickly first and became stable. The phenomenon was discussed in Chapter 2. The decrease of leakage current at the beginning can be attributed to the Coulomb blockade effect due to charges trapped to nc-ZnO sites. With the increase of the stress time, charges are gradually stacked to form the spot-connected path. Eventually a conductive path is established and the leakage current increases abruptly. The lifetime data collected from this kind of device are listed in Table 3.

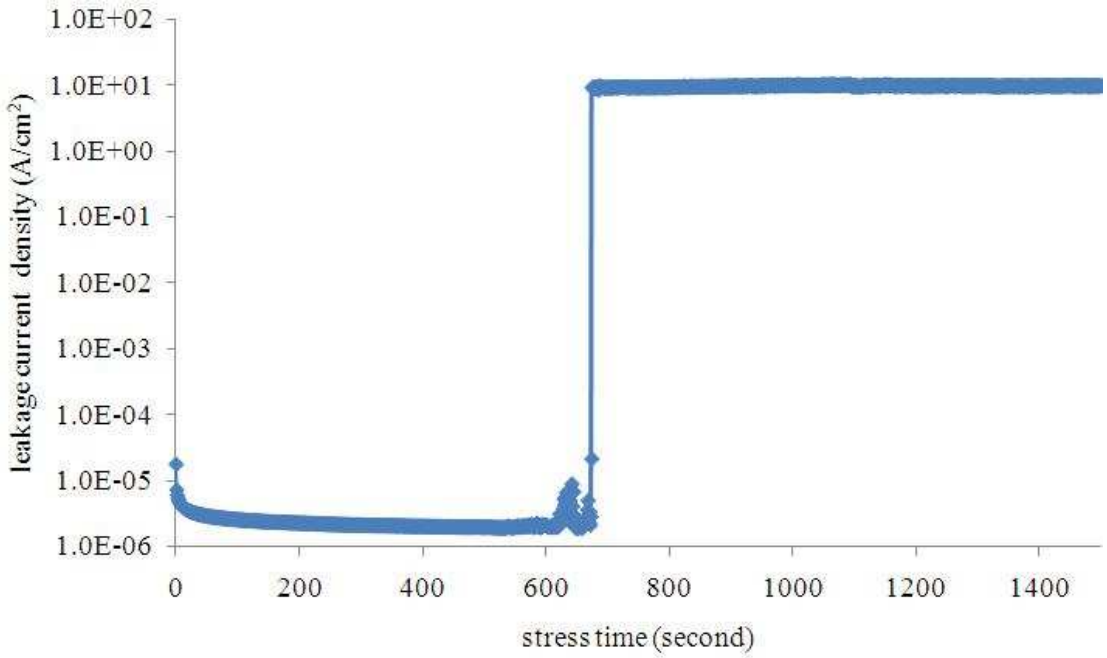


Figure 28. The J-t curve example for the lifetime test

Table 3. The lifetime data (time to failure) set for the nc-ZnO embedded ZrHfO capacitor

No.	stress level =7.5V
	time to failure
1	2
2	2
3	8
4	82
5	95
6	182
7	196
8	198
9	920
10	1369
11	15000
12	15000

The estimated hazard rate function is plotted in Figure 29. The DFR was observed before 1500s and the hazard rate becomes almost constant afterwards. To determine the optimal burn-in time, Mi [105] proposed the maximizing the reliability of a burn-in item to survive a mission time. Let the hazard rate function of a component be $h(t)$ and the component is required to accomplish a mission time, τ. Then the reliability of completing the mission is $S(\tau)$, where S is the survival function of the component. After the burn-in process, the conditional reliability of accomplishing the mission can be expressed by

$$\frac{S(b+\tau)}{S(b)} = e^{-\int_{b}^{b+\tau} h(t)dt} \tag{25}$$

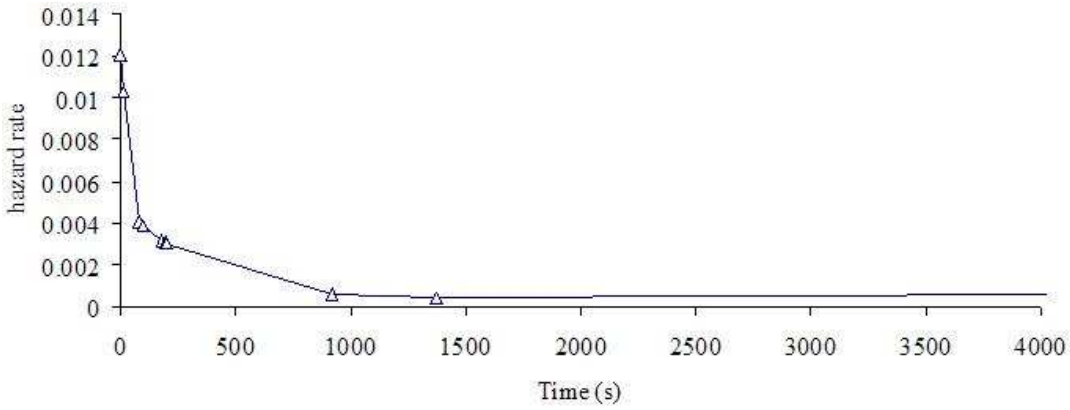


Figure 29. Estimated hazard rate function

The optimal burn-in time of the nc-ZnO embedded ZrHfO memory device can be obtained such that the above conditional reliability will be maximized.

The numerical results are shown in Figure 30. When τ =6 months, 1 year or 2 years, the conditional reliability will reach its maximum at *t* = 5867s, 5470s and 5206s with maximal reliability = 99.7%, 99.4% and 98.7%, respectively. The optimal burn-in time can be estimated to achieve the mission reliability [108-109]. Let the mission reliability be R_m, we have $R_m = h(b+\tau) - h(\tau)$. Figure 31 shows the optimal burn-in time under different mission reliabilities with τ =1 year. When R_m=99%, 95% or 90%, the mission reliability will be reached at *t* = 2597s, 1077s and 533s, respectively.

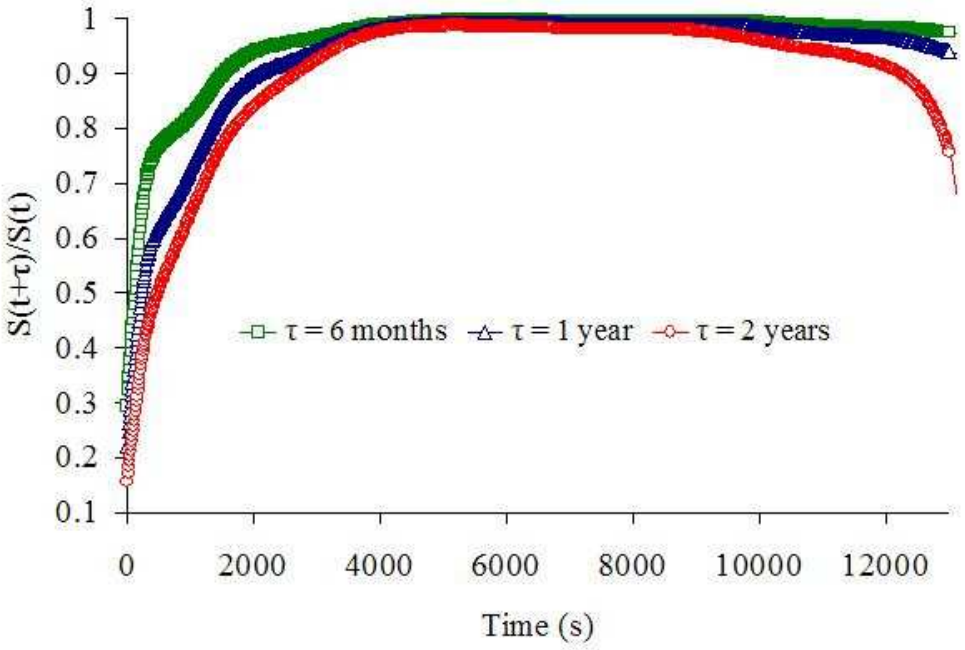


Figure 30. Conditional reliability of accomplishing different mission time

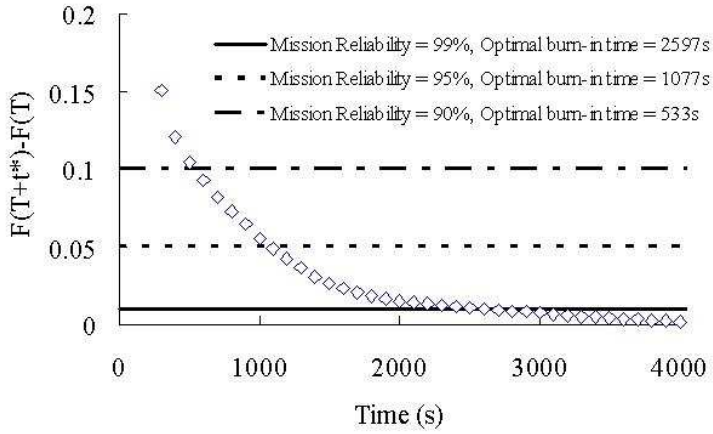


Figure 31. Achieving different mission reliabilities for mission time = 1 year

CHAPTER 6

SUMMARY AND CONCLUSIONS

Nanocrystal embedded high-k stack can successfully replace the conventional poly-Si floating-gate nonvolatile memory. Different charge storage media, i.e., nc-ZnO, nc-ITO, nc-Ru, and nc-Si have been studied and compared in this research. The nanocrystal embedded ZrHfO high-k thin film was prepared with RF sputtering process in the one-pump down process without breaking the vacuum. In this study, the reliability issues of this kind of dielectric structure have been investigated through monitoring the C-V hysteresis characteristics, current relaxation process, breakdown phenomena, charge transportation mechanisms, retention properties, temperature effect and lifetime analysis.

Large C-V hysteresis was detected in four different kinds of nanocrystals, i.e., nc-Si, - ITO, -Ru, and -ZnO, embedded ZrHfO high-k films. It is difficult to compare the charge storage capacities of these samples because they have different physical thicknesses or EOTs. Relaxation currents of the nanocrystals embedded high-k dielectric films were measured and compared. A larger gate voltage provides a higher initial relaxation current than the lower gate voltage does. The relaxation behavior does not seem to be influenced by the initial applied gate voltage. Different nanocrystals held charges at different strengths, i.e., in the order of nc-ZnO > nc-Si > nc-Ru > nc-ITO. The inconsistence between the magnitude in the hysteresis and charge holding strength show that the charge trapping strength of a nanocrystal material cannot be compared only by C-V curves. That is, to investigate the charge holding capability in the nc-embedded films with different EOTs, C-V curves and relaxation behavior are both required; the former is used to calculate the total number

of initially trapped charges and the number of loosely trapped charges can be obtained from the latter. The relaxation current was contributed by the loosely trapped charges, which is less than half of the originally trapped charges. The nanocrystal material influences not only the charge storage capacity but also the charge holding time.

For the single-layer nanocrystal embedded ZrHfO capacitor, the breakdown phenomenon can be investigated by using the ramp-relax method or time-dependent dielectric breakdown method. The result of the ramp-relax method shows that the breakdown of the sample was due to the breakdown of the bulk high-k film instead of the nanocrystals, which was demonstrated from the lack of polarity change of the relaxation current. The breakdown mechanisms of the single- and dual-layer nc-ITO embedded ZrHfO capacitors have also been investigated using the two-step ramp-relax and the time-dependent dielectric breakdown methods. The hole trapping capacity became more than double with the addition of the extra nc-ITO layer. The charge transport mechanism of the nc-ITO embedded ZrHfO stack followed the F-N tunneling relationship. The J_{ramp}-V_g, J_{relax}-V_g, and C-V curves of the nc-ITO embedded capacitors before and after the first breakdown step were measured. The complete breakdown of the capacitor cannot be simply identified from the abrupt jump of the leakage current. The addition of the nc-ITO increased the leakage current and made the complete high-k stack easier to break down.

The temperature effects on memory functions of the nc-ZnO and nc-ITO embedded ZrHfO capacitor have been studied. For the nc-ZnO embedded ZrHfO capacitor, the high temperature suppressed the Coulomb blockage effect in the J-V curve. The C-V hysteresis phenomenon became obvious with the increase of temperature from 25°C to 125°C. For the p-type wafer, in the accumulation region,

the hole trapping efficiency became obvious at the high temperature, e.g., 125°C. However, in the inversion region, the electron trapping effect was detected at 25°C. The interface quality is sensitive to temperature. In the depletion region, the C-V curve slope decreased with the increase of temperature. A valley in the G-V curve was observed at 125°C but not at 25°C or 75°C due to the former's interface states. The NITs are responsible for the low conductance in the 125°C curve. Therefore, the sample temperature affects the memory functions through changes of carrier generation, carrier kinetic energy, and dielectric conductance. The results of the retention efficiency test show that after releasing the gate stress, i.e., at +6V for 90s, for 10,000s, about 22.8%, 28.1% and 38% of the originally trapped charges were lost at 25°C, 75°C, and 125°C, respectively. Moreover, under room temperature, the nc-ZnO embedded ZrHfO high-k sample can retain charges for more than 10 years with memory window = 0.3V. However, the charge retention capability decreases with the increase of the temperature i.e., the lifetime decreased to 2 years at 75°C and 1.5 months at 125°C, separately. Therefore, the retention efficiency for the nc-ZnO decreases with the increase of the temperature. In addition, the capacitor's breakdown strength decreased with the increase of the temperature in the order of 25°C, 75°C, 125°C and 175°C. For the nc-ITO embedded sample, the initial memory window increased with the increase of temperature. However, the charge storage capacity decreased with the increase of temperature. After releasing the stress for 10 hours, the loss of the trapped charges were 34.8%, 64% and 92% at 25°C, 75°C and 125°C, respectively due to the increase of thermal energy of the trapped charge and the electric conductivity of the high-k film. The charge retention capability decreased with the increase of temperature, i.e., ΔV_{FB} = 0.25V after 10 years at 25°C, 0V after

270 days at 75°C, and 1.67 days at 125°C. The charge transportation mechanism follows the Schottky emission mechanism in the positive V_g range and the and F-P conduction mechanism in the negative V_g range due to the different conduction and valence band offsets between Si and HfSiOx.

Finally, the lifetime analysis of the nc-ZnO embedded high-k nonvolatile memory device was performed with non-parametric Bayesian approach. This research applied the nonparametric Bayesian method to estimate the hazard rate function of the nc-ZnO embedded high-k device. The optimal burn-in time was determined with two different objective functions. The 99% mission reliability after one year can be achieved with a 2597s burn-in procedure. In addition, the maximal reliability, 99.4%, after one year can be achieved with the 5470s burn-in time.

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