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TEMPERATURE DEPENDENT ANALYTICAL MODELING, SIMULATION AND CHARACTERIZATIONS OF HEMTS IN GALLIUM NITRIDE PROCESS

A Dissertation
Presented for the
Doctor of Philosophy
The University of Tennessee, Knoxville

Hasina F. Huq

August 2006

DEDICATION

This dissertation is dedicated to my parents

A.K. Fazlul Huq

and

Showkat Ara Huq

Although from far away, I still feel their presence.

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ABSTRACT

Research is being conducted for a high-performance building block for high frequency and high temperature applications that combine lower costs with improved performance and manufacturability. Researchers have focused their attention on new semiconductor materials for use in device technology to address system improvements. Of the contenders, silicon carbide (SiC), gallium nitride (GaN), and diamond are emerging as the front-runners.

GaN-based electronic devices, AlGaN/GaN heterojunction field effect transistors (HFETs), are the leading candidates for achieving ultra-high frequency and high-power amplifiers. Recent advances in device and amplifier performance support this claim. GaN is comparable to the other prominent material options for high-performance devices.

The dissertation presents the work on analytical modeling and simulation of GaN high power HEMT and MOS gate HEMT, model verification with test data and device characterization at elevated temperatures. The model takes into account the carrier mobility, the doping densities, the saturation velocity, and the thickness of different layers. Considering the GaN material processing limitations and feedback from the simulation results, an application specific AlGaN/GaN RF power HEMT structure has been proposed. The doping concentrations and the thickness of various layers are selected to provide adequate channel charge density for the proposed devices. A good agreement between the analytical model, and the experimental data is demonstrated.

The proposed temperature model can operate at higher voltages and shows stable operation of the devices at higher temperatures. The investigated temperature range is from 100^0K to 600^0K. The temperature models include the effect of temperature variation

on the threshold voltage, carrier mobility, bandgap and saturation velocity. The calculated values of the critical parameters suggest that the proposed device can operate in the GHz range for temperature up to 600^0K, which indicates that the device could survive in extreme environments. The models developed in this research will not only help the wide bandgap device researchers in the device behavioral study but will also provide valuable information for circuit designers.

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ACRONYMS AND ABBREVIATIONS

BJTs	bipolar junction transistors
CVD	chemical vapor deposition
DC	direct current
DARPA	Defense Advanced Research Projects Agency
FOM	figures of merit
f_T	the unity current gain cut-off frequency
GaN	gallium nitride
g_m	the peak DC transconductance
HFETs	heterojunction field effect transistors
HEV	hybrid electric vehicle
HEMTs	high electron mobility transistors
HBTs	heterojunction bipolar transistors
I_{dmax}	maximum drain current
IC	integrated circuits
LED	light-emitting diodes
MOS	metal oxide semiconductor
MODFETs	modulation doped field effect transistors
MOSFETs	metal oxide semiconductor field effect transistors
MESFETs	metal-semiconductor field effect transistors
RF	radio frequency
Si	silicon
SOI	silicon-on insulator
SiC	silicon carbide
TEGFET	two dimensional gas field effect transistors
V_{th}	threshold voltage
WBG	wide bandgap

CHAPTER 1. INTRODUCTION

Wide bandgap (WBG) semiconductors have some special material properties, which are exceptionally suitable for high performance and high temperature device applications. WBG semiconductors can be used in extreme conditions where Si-based devices cannot be used. Electric breakdown field of silicon carbide (SiC), gallium nitride (GaN), and diamond is higher than that of Si because of the wider bandgap. With this high electric breakdown much higher doping levels can be achieved. So, the device layers can be made thinner than Si at the same breakdown voltage levels. The resulting SiC, GaN, diamond devices are thinner than their Si counterparts, and they have smaller on-resistances. As the breakdown voltage increases, higher doping level can be applied to WBG semiconductors.

1.1 BACKGROUND

Research is being conducted for a high-performance building block for high frequency and high temperature applications that combine lower costs with improved performance and manufacturability. Significant technical advances are occurring for the development of WBG semiconductor materials and system designs to address these new needs. One of the major demands of advanced technology is that the electronics that operates and controls functional systems must survive in extreme environments.

WBG semiconductors based electronic devices show tremendous potential for microwave power electronics applications [1-4]. SiC based MOSFET, GaN-based AlGaN/GaN heterojunction field effect transistors (HFETs), diamond based electronic

devices such as field effect devices (FEDs) are the leading candidates for achieving ultra-high frequency and high-power amplifiers. Recent advances in device and amplifier performance support this claim. GaAs-based power devices have been very reliable workhorses at high frequencies especially microwave spectrum. However, their power performances have already been pushed close to the theoretical limit. In terms of power density, about 1 W/mm at 10 GHz would be the state of art performance for GaAs power p-HEMTs [5, 6]. For many years, silicon carbide (SiC) has been widely touted as a potential candidate, but unfortunately it does not appear to be a truly microwave technology in terms of its carrier mobility. With technological and cost advantages over competing SiC, GaN and diamond based family of semiconductors have quickly gained the center attention.

1.2 WIDE BANDGAP SEMICONDUCTORS

With the development of the wireless communications, telecommunications, data communications and aerospace systems, the demand for solid-state power amplifiers has been continually increasing over the last decade [7, 8]. The requirements include aspects of high power level, high efficiency, high linearity and high operating frequency and the relative importance of each of these features is application specific. One major trend is the continuous demand for more power at higher frequencies. Unfortunately, the existing technologies have struggled to sustain the higher demand. Under such circumstance, wide bandgap semiconductors with an order of magnitude or so higher breakdown voltage along with excellent thermal properties began to emerge. The main WBG semiconductors and some related issues are discussed below.

1.2.1 DIAMOND TECHNOLOGY

Diamond is intrinsically suited for high-speed, high- power and high-temperature (up to 1000°C) operation. It is viewed as the ultimate semiconductor. However, diamond faces significant processing hurdles that must be overcome before it can be commercially used for power electronic devices.

The diamond research group at Vanderbilt University has designed, fabricated, characterized, and analyzed diamond-based Schottky diodes fabricated by plasma-enhanced chemical vapor deposition for high-power electronics applications. The exiting chemical vapor deposition (CVD) technique permits process of diamond in a more controlled way.

Advanced field emission devices (FEDs) have the potential to carry current densities higher than present silicon diffusion barrier devices, resulting in the need for fewer devices and a smaller power electronic device. Besides it will have very low losses and are excellent conductors of heat; thus, there will be no need for expensive and unreliable water-cooling systems.

Figure 1.1 shows that diamond based devices are now a step closer to applications. However, diamond power devices are not expected to be abundant for another 20–50 years [7]. As shown in Figure 1.2, different diamond research groups are now fabricating diamond based field effect transistors.

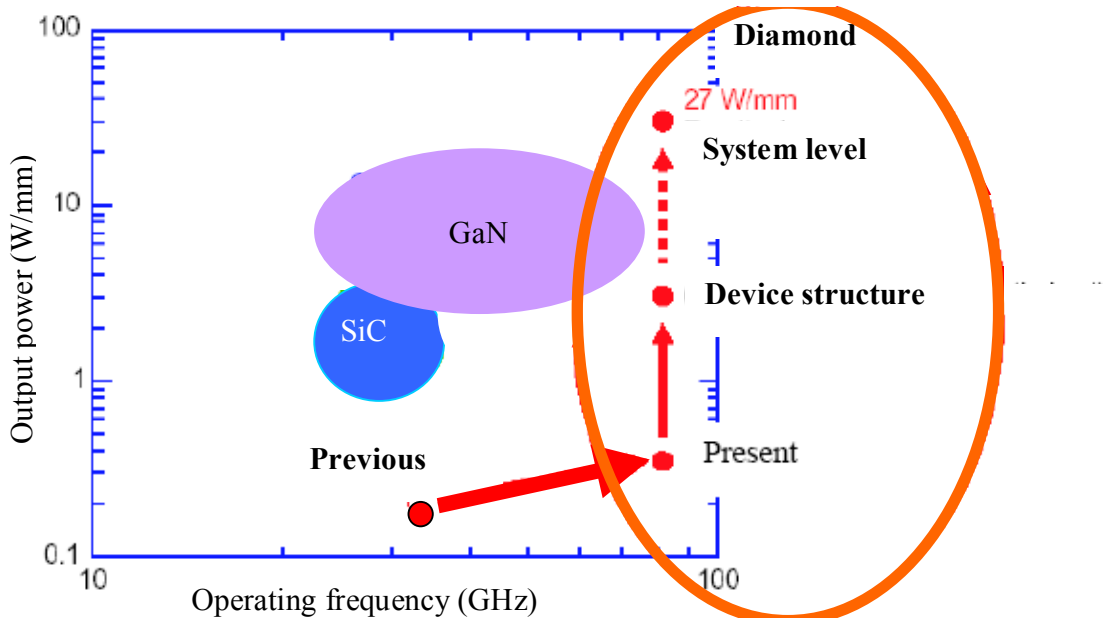
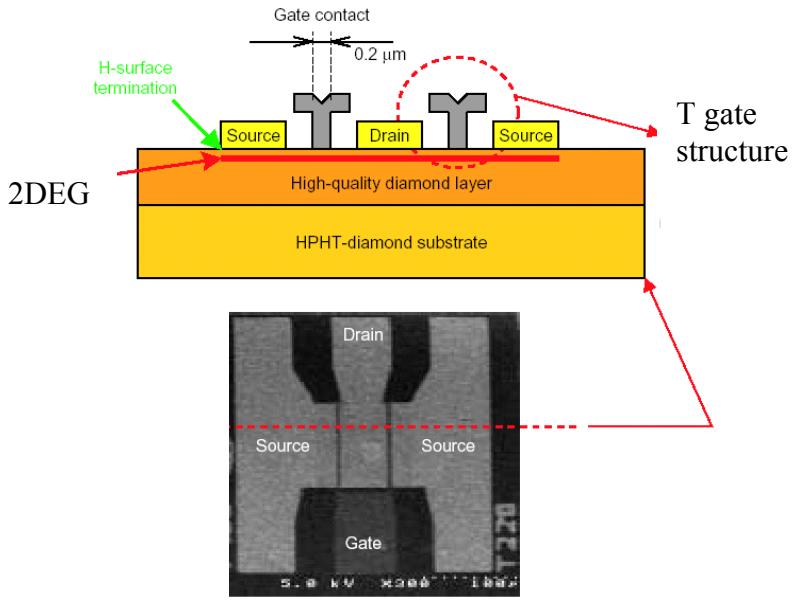


Figure1.1: Diamond devices: a step closer to applications [7]



Diamond FET device

Figure 1.2: Fabricated diamond field effect transistor [7]

The main advantages of diamond-based devices for semiconductor industry can be summarized as follows:

- 5 to 10 times higher current density than current devices
- High reverse blocking voltage
- Low conduction losses and fast switching speed
- Capability to withstand high radiation levels
- Higher-temperature operation and superior heat dissipation
- Larger power flow and voltage control devices
- Dramatic reduction in complexity
- Improved reliability and reduced cost
- Reduced or eliminated need for transformation and voltage upgrades
- Reduced capital costs
- Reduced or eliminated snubber circuits (reduction in device size)

Research on Diamond Devices: Presently, most of the diamond research has been in the following areas:

- Micro-patterned diamond micro-tips on films (mold technique)
- Diamond electron field emitter two/three terminal devices
- Diode: power diodes, laser diode, self-align gated diamond emitter diode (silicon-on insulator (SOI) process)
- Triode: self-aligned gated diamond emitter triode
- Transistors: diamond field effect transistor
- Core structure: (CVD diamond) Gate, anode
- Field emitter geometry

- Emitter array configuration
- Diamond cathode
- Silicon-on-insulator micro-electromechanical systems
- Vertical and lateral diamond emitter with nanometer-scale (5-nm) diamond tip

Challenges: Diamond technology

- Hardest material and needs even higher temperatures for processing
- For FED devices, thin gate and high current density causes failure
- Local heating and leakage current
- For FEDs which use arrays of thousands, major problem to make sure all the tips are turned on

1.2.2 SILICON CARBIDE TECHNOLOGY

Electronics systems based on SiC devices show substantial improvements in efficiency, reliability, size, and weight even in harsh environments. Therefore, they are especially attractive for high-voltage, high-temperature, high efficiency, or high-radiation uses, such as military, aerospace, and energy utility applications [7]. SiC is used for power devices such as Schottky diodes, JFETs, and MOSFETs, as well as MESFETs (metal-semiconductor field effect transistors) and blue LEDs.

SiC based device properties are superior to present Si devices:

- Can operate at high temperatures (up to 350°C)
- Have high thermal conductivity (3X silicon)
- Higher breakdown (blocking) voltages (>10X silicon)

- Low switching losses
- Can operate at high switching frequencies (>250 kHz)

Challenges in applications of SiC:

- Material is more expensive than Si
- New circuits, passive components, gate drivers are needed to take advantage of SiC properties

Although SiC technology will be substitutes for some of the Si devices, it is impossible to do a chip-to-chip replacement due to the challenges in applications of SiC based devices. Device testing and modeling are also needed for the new circuits and systems.

1.2.3 GALLIUM NITRIDE TECHNOLOGY

The advantages of SiC over Si have been investigated for many years. It is only in the past decade that serious attention has been given to other wide bandgap semiconductors for use in research. The gallium nitride technology has established itself as extremely important for third generation opto-electronics. This has created new markets in green LED traffic signals, full color outdoor displays and promises the next great advance in lighting [5].

GaN, one of the first III–V-compound semiconductors has been studied in the early 1960s. First epitaxial growth of GaN by halide vapor phase epitaxy was reported in 1969 [3]. A single crystalline GaN substrate is very rare. GaN films were typically deposited on sapphire substrates. Lately GaN growth on SiC is also reported. But the

interest declined in the early 1980s due to several severe problems. One of the major problems is that; the GaN films suffered from a very high n-type background carrier concentration and no p-type doping could be achieved. In the late 1980s high quality GaN films on sapphire substrates were reported in a two-step growth process, which resulted in a dramatic improvement of both the structural and the electrical properties of the GaN films [4].

A broad range of GaN electronic devices has been realized, including high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs), bipolar junction transistors (BJTs), Schottky and pin rectifiers and metal oxide semiconductor field effect transistors (MOSFETs). The advantage and disadvantage of GaN technology and related issues are discussed in the next chapter.

1.3 IMPORTANT PARAMETERS OF WBG SEMICONDUCTORS

Each semiconductor material has a unique bandgap. The bandgap helps to estimate how many electrons/holes contribute to the electric current. Those whose bonds are weak have small energy bandgaps; those with strong bonds have high bandgaps. For a conductor like copper, the forbidden band does not exist, and the energy bands overlap. For an insulator, on the other hand, this band is so wide that the electrons need a lot of energy to move from the valence band to the conduction band. For semiconductors, the gap of the forbidden band is smaller than for an insulator. Some semiconductors are classified as “wide-bandgap” semiconductors because of their wider bandgap. Silicon has a bandgap of 1.12 eV and is not considered a wide-bandgap semiconductor. The bandgaps of WBG semiconductors are typically three times or more that of Si.

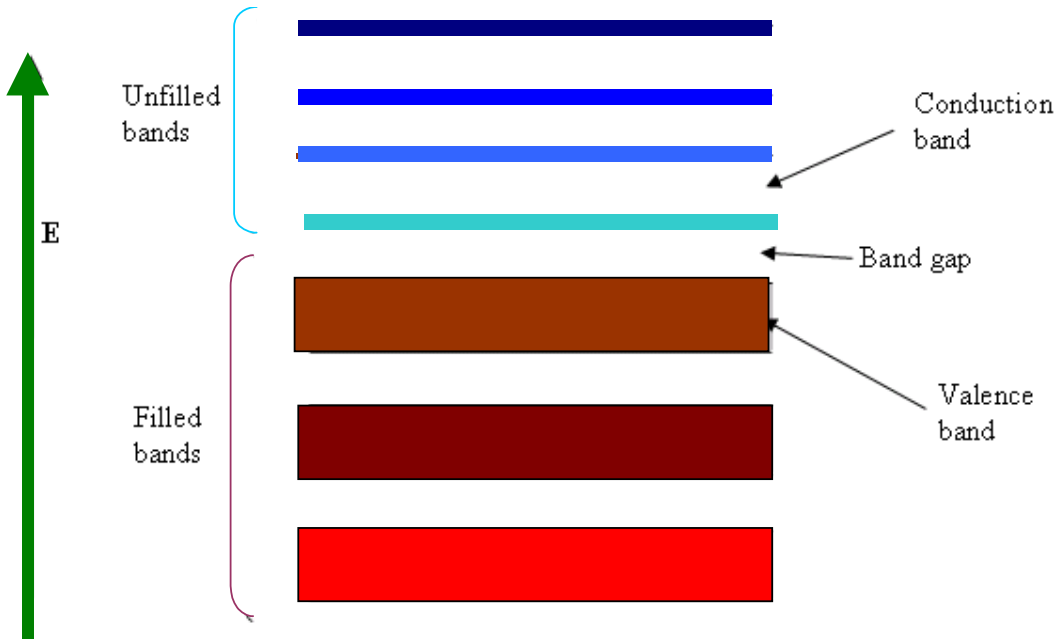


Figure 1.3: Semiconductor band structure [42]

Figure 1.3 shows a band structure of semiconductor. The conductivity of an intrinsic (pure) semiconductor is strongly dependent on the bandgap. The only available carriers for conduction are the electrons which have enough thermal energy to be excited across the bandgap, which is defined as the energy level difference between the conduction band and the valence band. From Fermi-Dirac statistics the probability of these excitations occurring is proportional to:

$$\exp\left(\frac{-E_g}{kT}\right)$$

where:

E_g is the bandgap energy (eV)

k is Boltzmann's constant ($1.3806503 \times 10^{-23}$ m^2 kg s^{-2} K^{-1})

T is temperature (^{0}K)

The most important parameters of WBG semiconductors are given below:

- Mobility (limits the device operating frequency)
- High saturated carrier drift velocity (limits the device speed)
- High radiation tolerance (limits the device operating temperature)
- Specific on-resistance (responsible for switching and conduction losses)
- Thermal conductivity (control size of the cooling system)
- Electric breakdown field (limits voltage operating range)
- Bandgap (large bandgap yields low thermal generation leakage currents)

1.4 ADVANTAGE: WBG SEMICONDUCTORS

Wide bandgap semiconductor materials have superior electrical characteristic compared with Si. Electronic devices based on wide bandgap semiconductor materials will likely result in substantial improvements in the performance of power and RF electronics systems in terms of higher blocking voltages, efficiency, and reliability, as well as reduced thermal requirements. Some of these characteristics are listed for the most popular wide bandgap materials and Si in Table 1.1. The table shows that diamond has the best electrical and mechanical material properties. SiC is suitable for high power applications, and GaN is suitable for high frequency applications. The resulting device and system benefits are summarized in Table 1.2.

Table 1.1: Physical characteristics of Si and the important wide bandgap semiconductors [2]

Property	Target	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap E_g, (eV)	↑	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, ε_r	↑	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field, E_c (kV/cm)	↑	300	455	2500	2200	2000	10000
Electron mobility, μ_n (cm^2/V·s)	↑	1500	8500	500	1000	2000	2200
Hole mobility, μ_p (cm^2/V·s)	↑	600	400	101	115	850	3800
Thermal conductivity, λ (W/cm·K)	↑	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity, v_{sat} ($\times 10^7$ cm/s)	↑	1	1	2	2	2.2	2.7

Table 1.2: Advantages of wide bandgap devices

Material properties	Device characteristics	System benefits
High bandgap energy High breakdown electric field High thermal conductivity High saturated e- drift velocity High radiation tolerance	High breakdown voltage High current density High operational temperature High switching frequency Low power losses	Large power capacity High efficiency, reliability Less cooling requirements Reduced volume of passive components, good compactness

WBG semiconductors can be used in extreme conditions where Si-based devices cannot be used. Electric breakdown field of SiC, GaN and diamond is higher than that of Si because of its wider bandgap.

The switching frequency of the devices is also limited because of the heat generated by the devices, primarily the switching losses. Higher-frequency operation is preferred because of smaller filtering requirements, less audible noise, and smaller passive components. The outputs of high-frequency power converters are smoother, and a small filter would be sufficient to filter the harmonics. Additionally, with high frequency, the size of the passive components decreases, so there is an overall gain in size and weight. Moreover, with higher frequency, the converters could work at an inaudible frequency range, which would be comfortable for the user.

To further explore the possible performances of these materials, some commonly known figures of merit are listed in Table 1.3. In this table, the numbers have been normalized with respect to Si; the larger the number, the better a material's performance in the corresponding category. GaN devices are focused mainly on opto-electronics and radio frequency applications. Some of the potential applications of WBG electronics are in hybrid electric vehicle (HEV), spacecraft, utility system, mining, aircraft and nuclear power station. Figure 1.4 shows the possible areas of WBG electronics application.

Figure 1.5 shows the main systems benefits of the WBG semiconductors. The figure indicates a smaller, cheaper and better quality system solution compared to present Si based system. Figure 1.6 gives an overview for the possible applications of WBG-based devices in communication industries.

Table 1.3: Main figures of merit for WBG semiconductors compared with Si

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81000
BFM	1.0	14.8	125.3	223.1	186.7	25106
FSFM	1.0	11.4	30.5	61.2	65.0	3595
BSFM	1.0	1.6	13.1	12.9	52.5	2402
FPFM	1.0	3.6	48.3	56.0	30.4	1476
FTFM	1.0	40.7	1470.5	3414.8	1973.6	530449
BPFM	1.0	0.9	57.3	35.4	10.7	594
BTFM	1.0	1.4	748.9	458.1	560.5	1426711

JFM: Johnson's figure of merit, a measure of the ultimate high-frequency capability of the material

BFM: Baliga's figure of merit, a measure of the specific on-resistance of the drift region of a vertical field effect transistor (FET)

FSFM: FET switching speed figure of merit

BSFM: Bipolar switching speed figure of merit

FPFM: FET power-handling-capacity figure of merit

FTFM: FET power-switching product

BPFM: Bipolar power handling capacity figure of merit

BTFM: Bipolar power switching product

Source: Ref. [2].

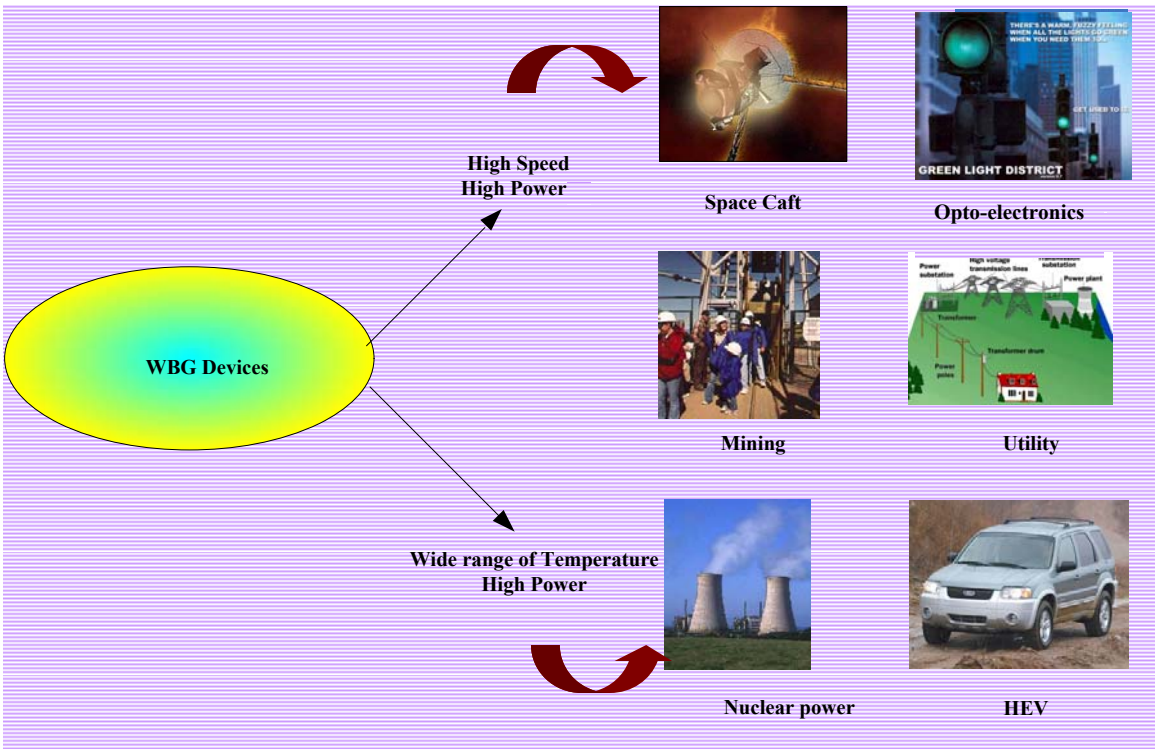


Figure 1.4: The possible areas of WBG electronics application (Md. Hasanuzzaman, PhD Dissertations, Univ. of Tennessee, Knoxville, 2004)

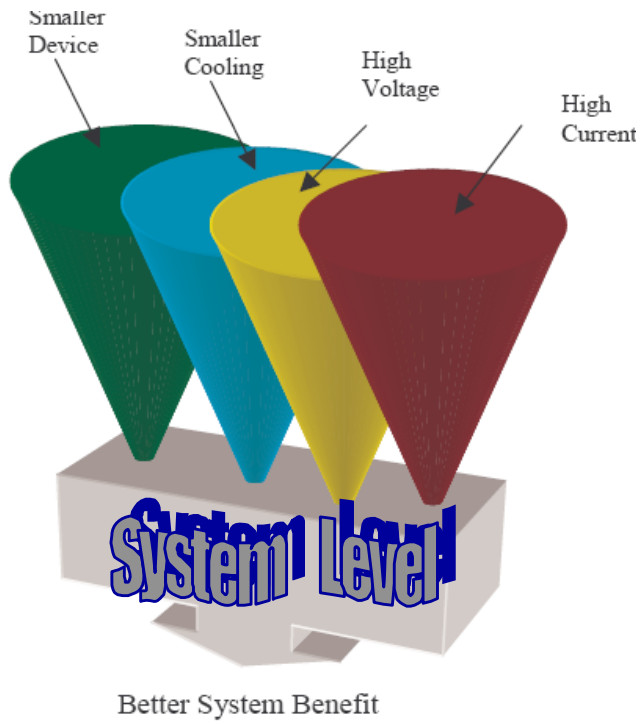


Figure 1.5: The systems benefits of the WBG semiconductors

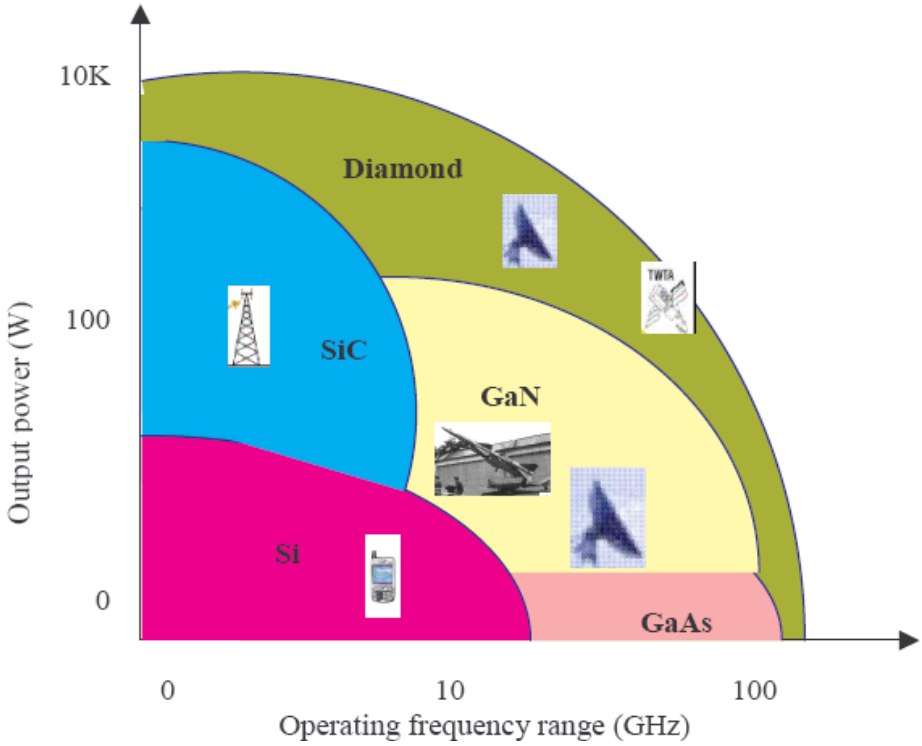


Figure 1.6: Comparison of wide bandgap electronics for communications industry [7]

1.5 CHALLENGES FOR WBG SEMICONDUCTOR TECHNOLOGY

Although Si semiconductor technology is highly developed, the fabrication of WBG semiconductors technology is not a one-to-one duplication of Si semiconductors. The implementation of WBG material system is not chip-to-chip replacement. New device structures, processing technology, and electric circuits are required in order to take advantage of new semiconductor materials. Therefore, a series of issues need to be resolved before WBG devices gain widespread use in electronic applications.

Cost: High cost is one barrier limiting the development of WBG based devices. Currently, the price of SiC devices is 5–10 times that of Si devices [7, 8]. GaN and diamond based devices are not yet commercially available.

Material availability and quality: The best-quality wafer of WBG semiconductors is not commercially available to date.

Device design and fabrication: All the basic process steps of WBG devices have been demonstrated, but many problems remain to be dealt with such as to minimize parasitic substrate resistance, high-temperature, surface charges and surface states of WBG semiconductors and related defects.

Device packaging technology: High-temperature, high power density packaging techniques are required to take full advantage of WBG semiconductors capabilities. The materials and processing technology are critical factors that dominate the cost of WBG based devices and influence their market prospects.

1.6 RESEARCH OBJECTIVES

In recent years much research effort has been conducted in the field of HEMT. GaN based devices specially HEMTs have attracted a lot of interest in this regards. Based on the gate structure, two types of AlGaN/GaN HEMTs can be classified:

(1) Schottky gate

(2) MOS gate.

Due to some fabrication disadvantages of MOS gate HEMT, more research efforts have been devoted to Schottky gate HEMT. But efforts have been made to solve the fabrication problem, and it is apparent that solution is near.

The objectives of the current research are:

- To provide an extensive study on the wide bandgap semiconductor materials
- To evaluate a suitable material for high power HEMT used in millimeter wave application
- To develop an improved analytical model for the self-aligned HEMT with metal oxide gate
- To develop temperature model for the self-aligned HEMT. The investigated temperature range is from 100^0K to 600^0K
- To characterize the extended model of GaN based HEMTs and MOS gate HEMTs
- To validate the simulation results and experimental data with numerical simulation using Medici^{TM}, Sentaurus^{TM} etc.
- Testing and characterization of the HEMT

An analytical temperature model based on modified charge control equations is developed for the proposed device. The temperature effect on saturation current, cut-off frequency, and transconductance behavior determines the device behavior in extreme environments. The analysis of the proposed model shows that the device demonstrates significant degradation at elevated temperatures. Preliminary results from the temperature model and the measured data at room temperature demonstrate the feasibility of the developed model. The calculated values of the critical parameters suggest that the proposed device can operate in the GHz range for temperatures up to 600^0K, which indicates that the device could survive in extreme environments. The proposed temperature model based on GaN/AlGaN material systems also has superior high frequency characteristics even at higher temperatures. GaN and related materials (especially AlGaN) have recently attracted a lot of interest in this regard. The prime motivation for developing the proposed model of AlGaN/GaN microwave power device is to demonstrate its inherent ability to operate at much higher temperature. The proposed temperature model operates at higher voltages and show stable operation at higher temperatures.

Most of the works of MOS gate HEMTs concentrate on fabrication and experimental characterization. Not much work has been devoted to the analytical modeling and simulation of these devices. The research work includes the calculation of threshold voltage and Vg_{max} of HEMTs and MOS gate HEMT, examine the effect of different device and material parameters on V_{th} and $V_{gmax,}$ using modified analytical model, to predict the temperature dependency of V_{th} and current-voltage characteristics of HEMT and MOS gate HEMT. A reliable device model is very important in device design

as well as predicting the behavior of existing devices. For a device design engineer, analytical model is the first tool to be used. The analytical model can give the designer a rough, if not very accurate, idea about the behavior of the device to be designed. As a second step of the design process, the numerical simulation software tool such as Medici™, Sentaurus™, Davinci™, Dessis™, and Atlas™ etc can be used.

1.7 OUTLINE OF THE DISSERTATION

There are three main parts in this dissertation. The first part is about the temperature modeling techniques suitable for HEMTs in GaN process. The second part is focused on the testing, characterization, and parameter Extraction approach for HEMTs. The third part is about the industry standard device simulation techniques to validate the results. The research described in this dissertation seeks to address the key problems in developing HEMT RF power devices in GaN.

The research in GaN HEMT and MOS gate MODFET modeling, characterization and model development is presented in seven chapters. The dissertation is organized as follows:

Chapter 1 gives an overview of the status of the current research trends for wide bandgap based electronics. This chapter has the information on semiconductors such as silicon carbide (SiC), gallium nitride (GaN), and chemical vapor deposition (CVD) diamond. The advantages as well as the challenges involved in the processing of these materials are discussed in detail in comparison to today's silicon-based devices.

Chapter 2 presents an overview of the history of HEMTs, GaN material and related issues. First, the basic concepts of HEMTs and MOS gate HEMTs are described. Next, a discussion of physical and electrical properties of GaN is presented. Finally, problem statements of the GaN based device and a review of the main GaN research groups in the United States are presented.

Temperature model for HEMTs is presented to evaluate the device performance across the temperature range of 100^0K to 600^0K in chapter 3. The results obtained from the analytical modeling and experimental measurements are discussed. This chapter also discusses the temperature dependent parameters and temperature related issues used in the study.

Chapter 4 presents the research work on MOS gate based HEMT device modeling. An improved analytical modeling approach of a MOS gate HEMT in AlGaN/GaN is presented. Finally, the results obtained from the analytical and experimental results are compared with the industry standard device simulator.

Chapter 5 contains the industry standard numerical simulation results using device simulator Medici^{TM}, and Sentaurus^{TM}. Some of the simulation results are compared to the analytical and experimental results. Among the simulations, some of them are illustrative of device physics and behavior, while others are used to examine the dependence of device and material parameters on device performance.

Chapter 6 presents the measurement, characterization and extraction of the analytical model parameters of GaN HEMT transistor. First, the different measurement test setup and systems are described. Then, the measured data and figures are presented

for the GaN HEMTs model. Finally, the small signal parameter extraction procedures are described.

In chapter 7, the conclusions of the dissertation are drawn and some recommendations are suggested for future work.

The appendices at the end of the dissertation provide the following additional information:

Appendix A contains the MATLAB programs for the analytical modeling of GaN based HEMTs. Appendix B contains the Medici™ simulation codes for the analytical modeling of III-V semiconductors based HEMTs. Appendix C summarizes the Sentaurus™ simulation codes for the analytical modeling of GaN based HEMTs. Appendix D provides information on fabrication steps of GaN based HEMTs.

CHAPTER 2. LITERATURE SURVEY

2.1 HISTORY OF HEMT

HEMT (High Electron Mobility Transistors) is also known as MODFET (Modulation Doped Field Effect Transistor), (Two Dimensional Electron Gas Field Effect Transistor) TEGFET, and HFET (Heterojunction Field Effect Transistor). HEMT is basically a heterojunction device, which uses two-dimensional electron or hole gas trapped in quantum well as carrier. These carriers are far from the influence of the dopant atoms, thus less affected by Columbic interaction with ionized dopant atoms. This along with the fact that the carrier movement is confined in only two dimensions, results in surprisingly high electron/hole mobility. HEMT was invented in the beginning of 1980s. For the same gate length, a HEMT device is able to offer much more speed than a MOSFET. Also, HEMT offers much better noise figure than MOSFET, which is a very important consideration in high-speed circuit and system applications [9, 10-14]. HEMT devices show higher mobility that should lead to lower noise figures. GaAs/AlGaAs HEMT was the first HEMT fabricated. Later, HEMT has been fabricated using different materials. AlGaAs has almost perfect lattice match with GaAs for all the concentration of Al. Thus, high quality epitaxial layer of AlGaAs can be grown on top of GaAs substrate.

2.2 BASIC MODULATION DOPED STRUCTURE

There is a way to avoid the mobility penalty at high doping concentrations. This is called modulation doping. Modulation doping is a concept that creates a two-dimensional electron gas with high carrier mobility. The basic structure consists of a doped wide-

bandgap semiconductor adjoining a narrow-bandgap semiconductor**.** Figure 2.1 shows a typical structure of a HEMT. There exists discontinuity in both the conduction band and the valence band at the heterointerface. Electrons diffuse from highly doped layer to undoped layer. The electrons are trapped in the quantum well formed in the channel that is approximately triangular in shape. Carriers originating from their parent dopants in the wide-gap material transfer to the narrow-gap material due to the availability of states at lower energy. Band bending results as a consequence of the charge transfer. Free electron gas is created in the narrow-gap material at the boundary between the two semiconductors (Figure 2.2).

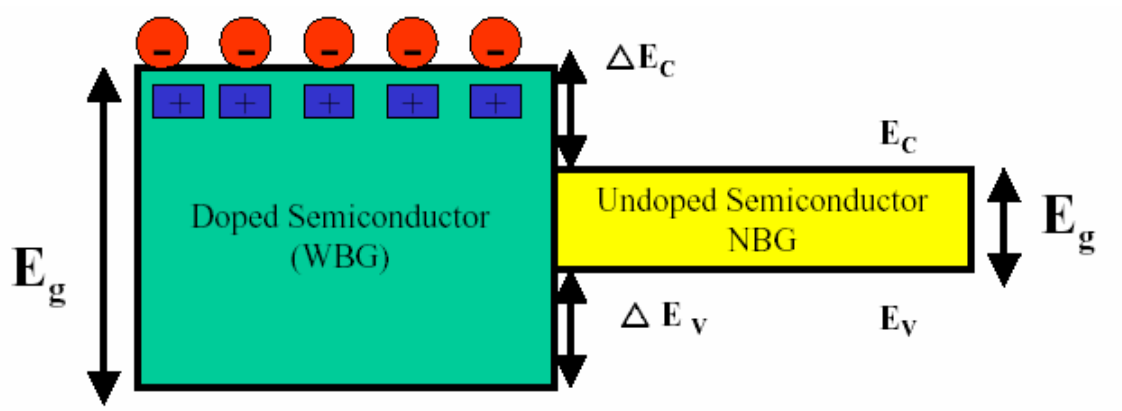


Figure 2.1: Basic modulation-doped structure

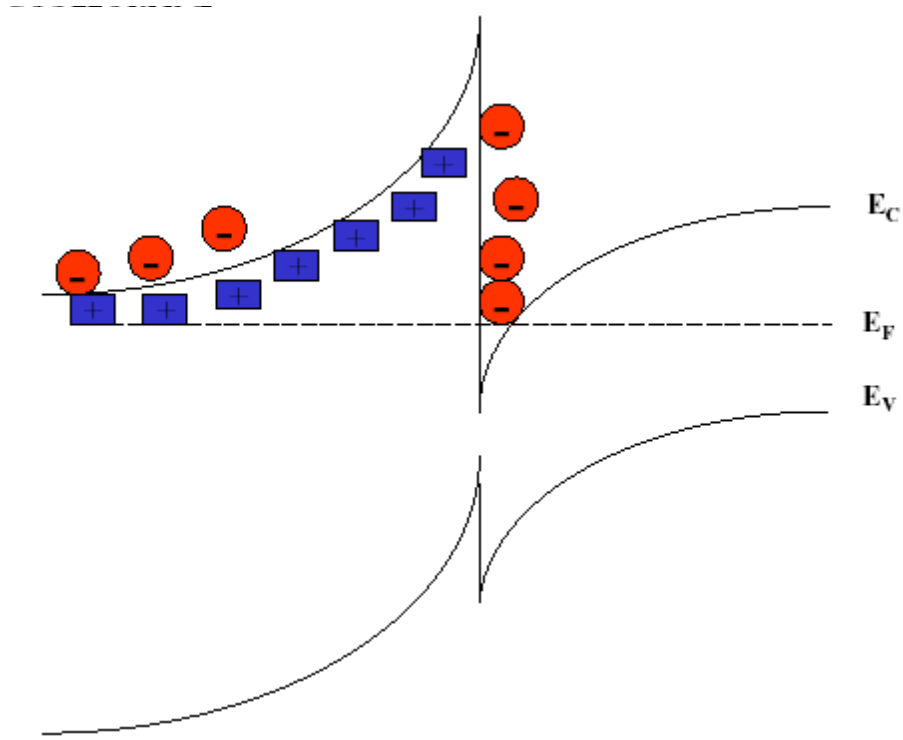


Figure 2.2: Band diagram of basic modulation-doped structure

Electrons are spatially separated from donors thereby reducing ionized impurity scattering. The ratio of $\Delta Ec / \Delta Ev$ depends on the material system. Free electron gas is created in the narrow-gap material at the boundary between the two semiconductors. Electrons are spatially separated from donors thereby reducing ionized impurity scattering. Separation between electrons and donors can be further enhanced with the introduction of a spacer layer (Figure 2.3). Thus, mobilities can be increased greatly in modulation-doped heterostructures. Figure 2.4 shows the band diagram of the modulation-doped structure with a spacer layer.

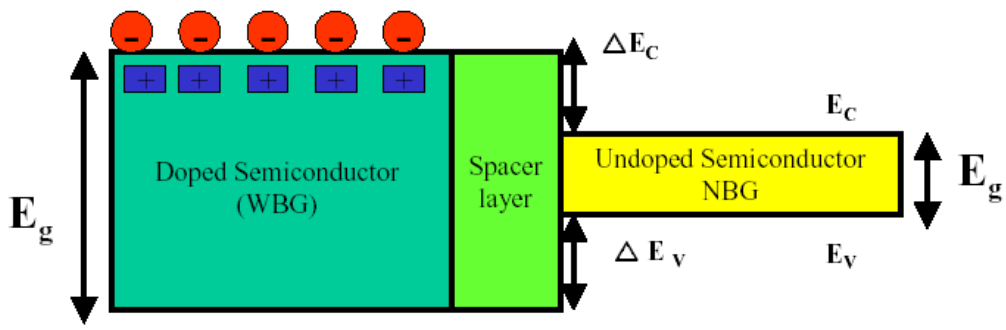


Figure 2.3: Modulation-doped structure with spacer layer

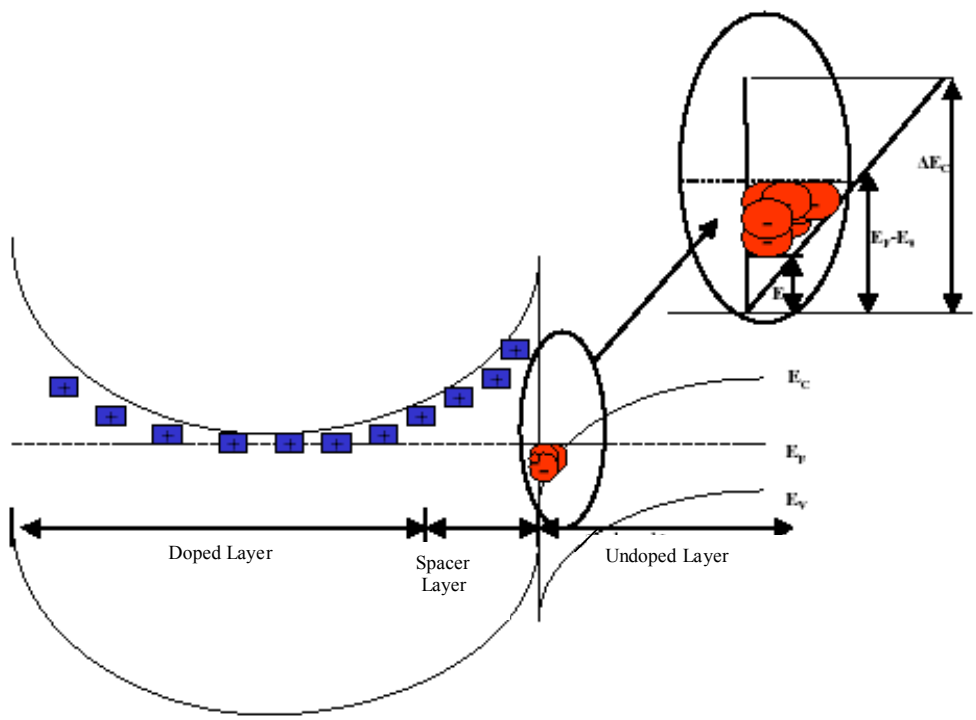


Figure 2.4: Band diagram of the modulation-doped structure with spacer layer

2.3 WHY GALLIUM NITRIDE (GAN)?

The III-nitride semiconductors have plenty of promise for applications in opto-electronic devices such as light emitting diodes (LED), laser diodes, and photo detectors in blue and UV region [15-17]. On the other hand, GaN-based electronic devices constitute the leading candidate for simultaneously realizing ultra-high frequency and ultra-high power amplifiers. This claim is supported by recent advances in device and amplifier performances that are in turn made possible by the relentless improvements in heterostructure synthesis [18-23]. Figure 2.5 illustrates the electronic properties of GaN-based devices. These properties give the following advantages for the GaN-based systems:

- High power density
- Multi-octave bandwidth
- High efficiency
- Linearity

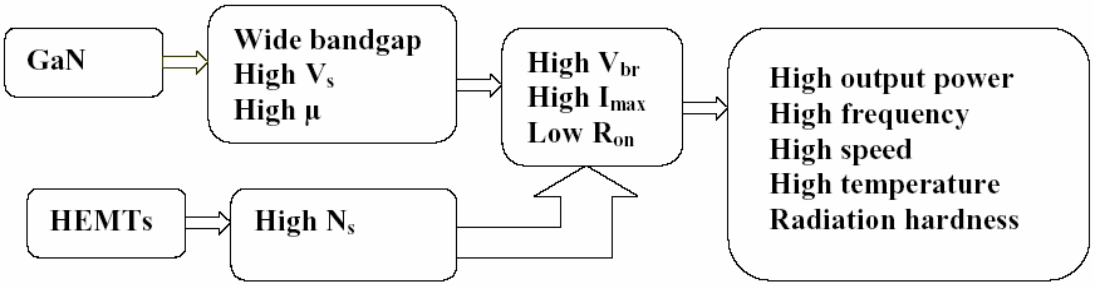


Figure 2.5: Electronic properties of GaN based devices.

While so far GaN has been explored for opto-electronic and RF applications, it offers significant advantages for power-switching devices because of the availability of band engineering in III-nitride materials. In fact, the on-going development of GaN-based devices for opto-electronic and RF applications allows the natural extension of this technology into the power electronics field. In comparison of another wide bandgap semiconductor SiC, the availability of band engineering for III-nitride materials allows device operation at higher speed and at much higher current hence higher power density [24-30]. Dr. Umesh Meshra from the University of California, Santa Barbara, published an article on GaN Based transistors in IEEE Spectrum, May, 2002 (Figure 2.6). In the article, it was mentioned that GaN based devices are the toughest transistor yet. GaN is comparable to the other prominent material options for power devices. GaN-based devices can be fabricated over either sapphire or SiC substrates to take advantage of higher thermal conductivity. However, there are problems associated with this material that make it difficult to build high-voltage devices. The technical problems such as potential device failure due to current collapse and unstable output are observed when voltage exceeded 50V [30]. The extremely large electrical field spike can cause local Schottky barrier breakdown at a much lower applied drain voltage. AlGaN/GaN, AlGaInN/GaN, AlGaInN/InGaN power devices grown on different semiconductor materials have demonstrated much larger output power, have become promising for high power amplifications and switching applications [17, 31-35]. In power devices, the use of wide bandgap semiconductors not only increases the output power but also extends temperature tolerance and radiation hardness of the circuits. Recently, some AlGaN/GaN structures useful for several hundred volts power switching have been proposed [36-39].

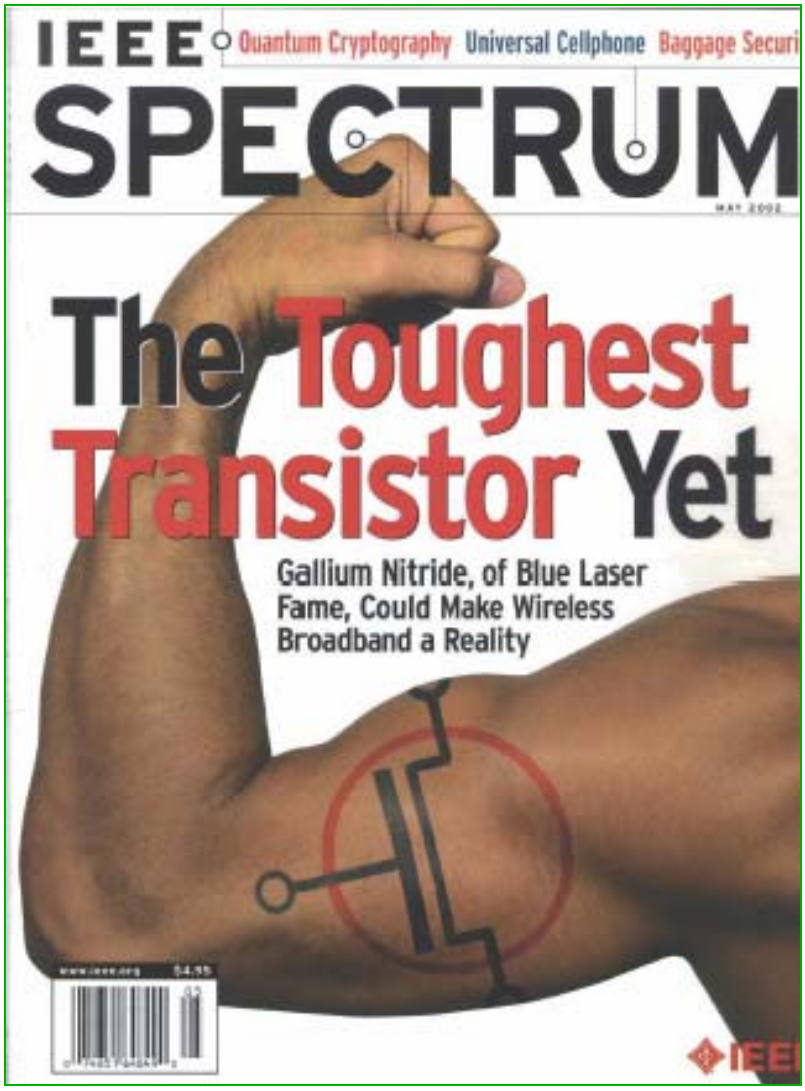


Figure 2.6: GaN based transistors are the toughest transistors: IEEE Spectrum, May 2002

2.4 GaN DEVICE TECHNOLOGY

The markets for laser printing, optical storage, high-brightness LEDs, general illumination, and wireless base stations can clearly benefit from GaN-based devices. Other GaN device markets that have yet to be developed, or are in their infancy, are medicine, memory applications, and power electronic devices (see Table 2.1).

GaN-based semiconductor materials have attracted a great deal of interest in power, RF and opto-electronics devices. Figure 2.7 shows the commercial sales opportunities for GaN-based devices. The commercial sales opportunities of GaN are increasing exponentially, and it is expected that after 2010 the market will be greater than $5 billion. Figure 2.8 shows the current technology limitations and some potential improvements of GaN based devices over GaAs based devices [40-44].

Table 2.1: GaN device market [8]

Devices			
	Lasers	LED	UV detectors
	Optical storage	Traffic lights	Flame detectors
Optical device applications	Laser printers	Video displays	Analytical equipment
	Military	Miniature lamps	Pollution monitor
	Medical	Automotive lamps	Ozone monitor
		General illumination	
Electrical device applications	Power transistors	Integrated circuits	
	Cellular base station	Microwave circuits	
	Power electronic converters	Cellular infrastructure	
	Radar and microwave		

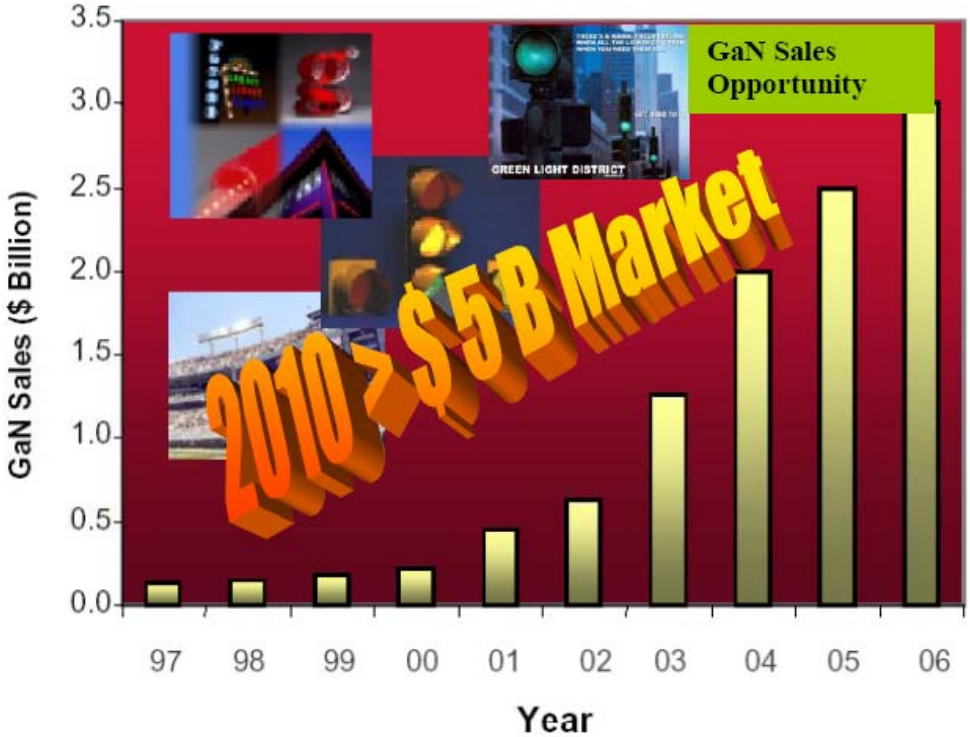


Figure 2.7: Commercial opportunities for GaN [44]

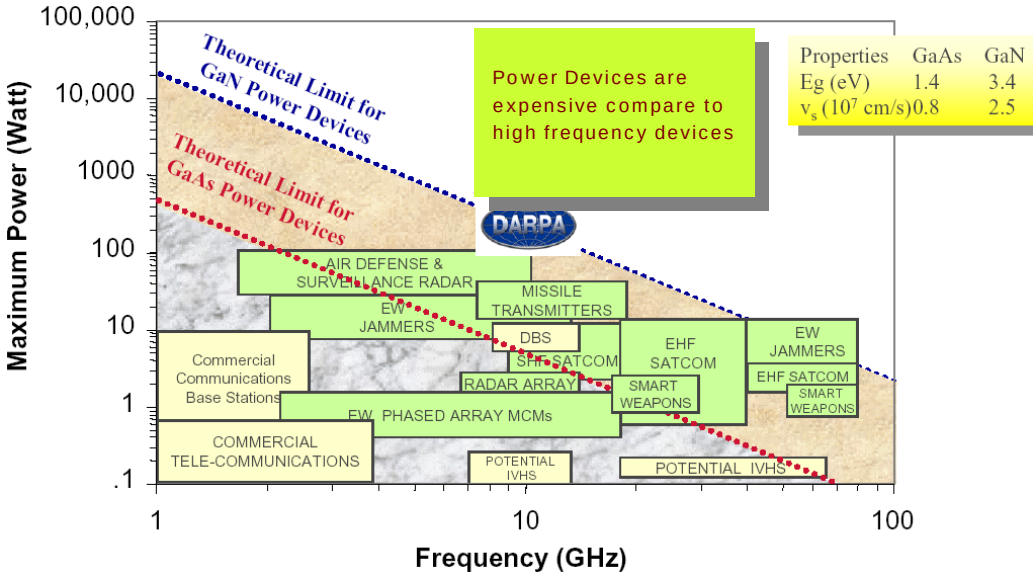


Figure 2.8: Current technology limitations and potential improvements [44]

GaN based power devices offer much higher output power level as well as higher operating frequency range. Defense Advanced Research Projects Agency (DARPA) is providing funding for research in GaN technology. Researchers focus their attention to design smart weapons, air defense, radar, missile, and transmitters in GaN material system.

In GaN technology, all of the following processing steps and fabrication techniques are possible now.

- Material Processing

  Epitaxial Growth

  Dopant Activation

  Oxide formation

  Interface Engineering

- Device Fabrication

  Schottky Diodes

  HEMTs, MOS-HEMTs

  BJTs

- Applications

  Circuit Design

  System Integration

Figure 2.9 shows the basic steps of device fabrication. At present, material processing and device fabrication of the wide bandgap materials are in primitive stage. As mentioned earlier, GaN device fabrication is possible now. So it is the pathway to success.

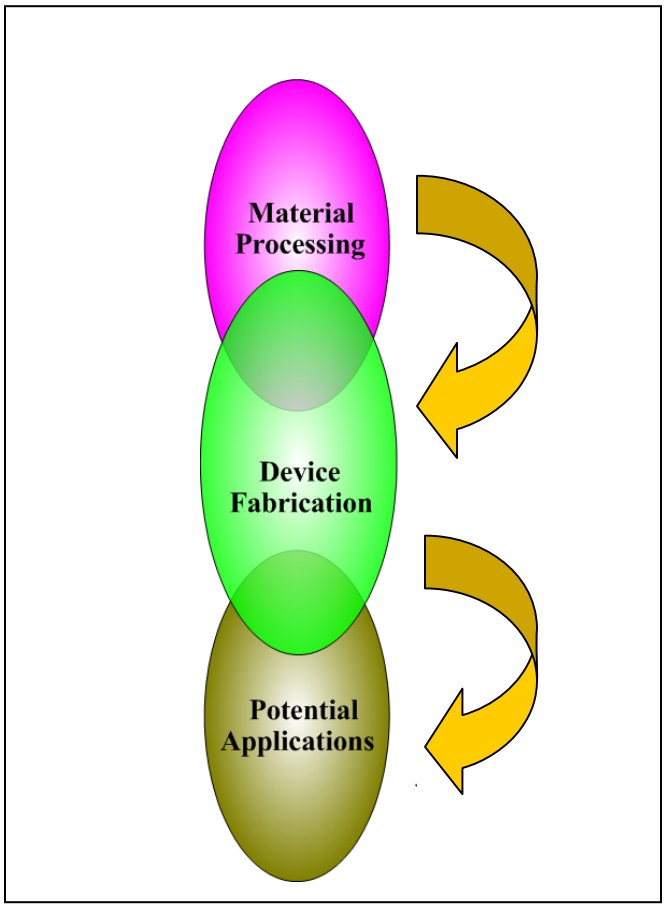


Figure 2.9: Device fabrication and design flow [46]

The basic steps of GaN manufacturing process are shown in Figure 2.10. GaN substrates with large enough diameter do not exist for growing GaN channels; the largest GaN substrates obtained so far are 1.7 cm × 1 cm [33]. Sapphire and SiC are the most popular substrate materials used currently. Sapphire is cheaper for GaN growth than SiC. But the low thermal conductivity presents a serious challenge for packaging of high power devices.

Long term reliability may be considered due to thermally induced stress on the contacting pads, which also serve as the heat-conducting path. On the other hand SiC has lower lattice mismatch with GaN or AlN and 10 times higher thermal conductivity [44]. Even then, thick GaN substrates are not commercially available. As a consequence, GaN wafers are more expensive than SiC wafers. In the nucleation technology of low-Al content AlGaN layers, it is necessary to "calibrate" each new boule of sapphire, to find appropriate nucleation conditions.

Figure 2.11 shows that 40%-45% of the total cost of GaN devices comes from the GaN material, 50%-55% from the process and packaging, and 5%-10% from testing. The prospect of some GaN based devices are summarized here:

Schottky diodes: Some high power Schottky diodes have been reported [45-47]. The comparison of GaN Schottky diodes with SiC Schottky and Si pn diodes at similar blocking voltages show a performance advantage of the GaN Schottky diode. The GaN Schottky diodes capable of operating in the 300–700V range with low turn-on voltage (0.7 V) [22,34, 48].

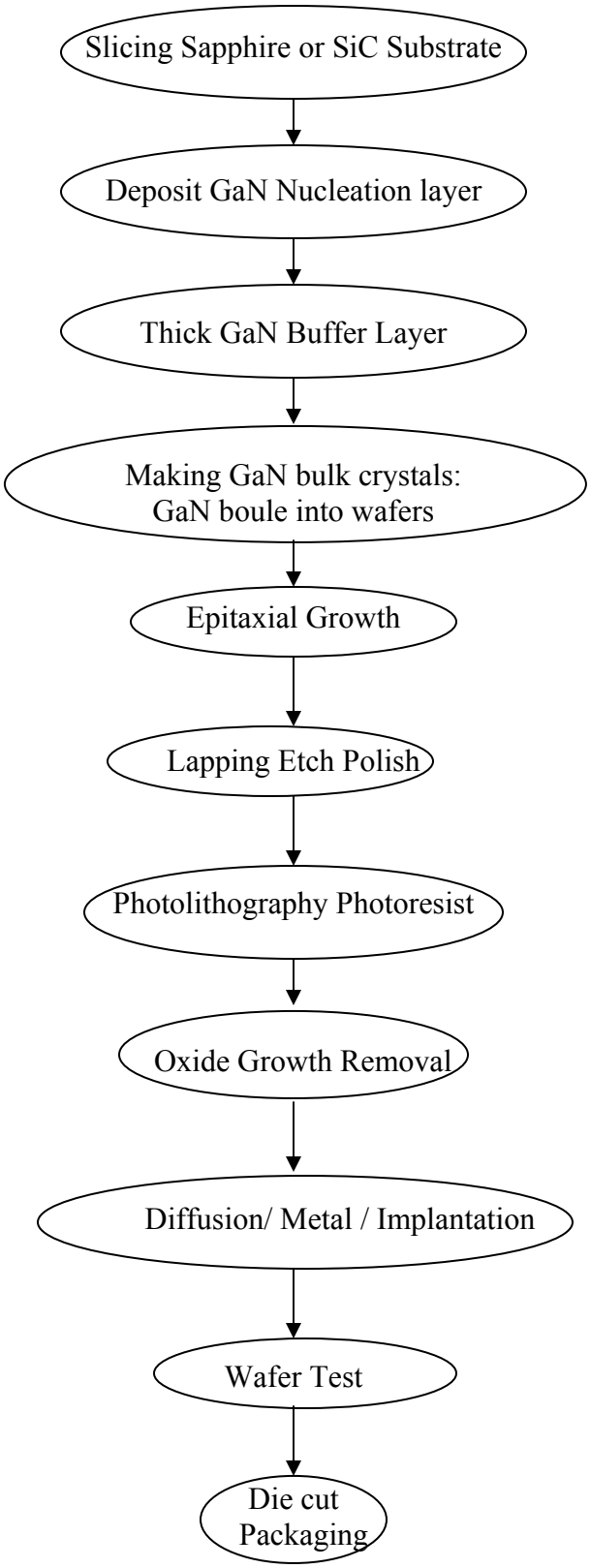


Figure 2.10: The basic steps of GaN manufacturing process [47]

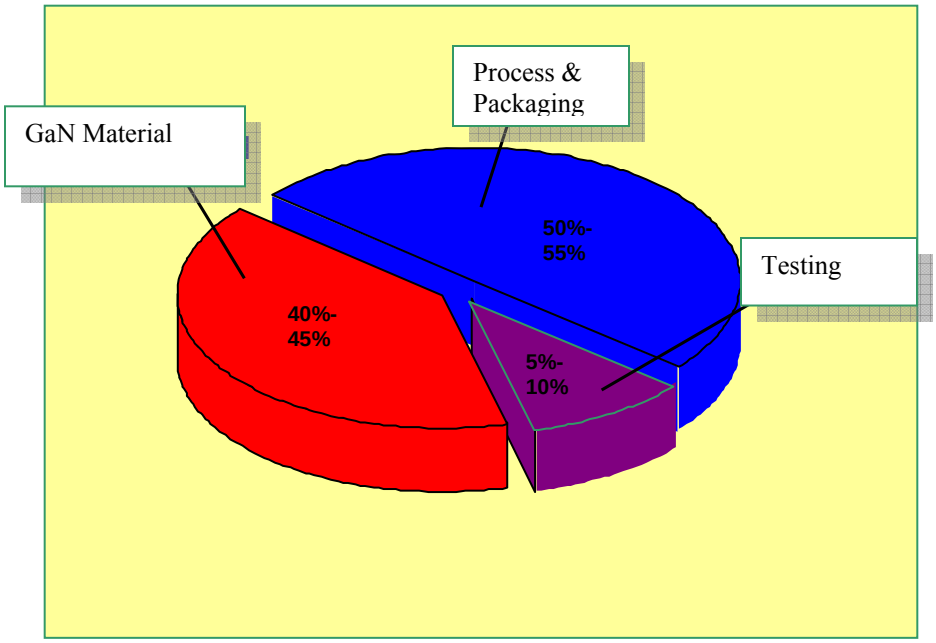


Figure 2.11: Typical cost breakdown for GaN devices [47].

Bipolar devices: GaN based bipolar devices are particularly interesting for high current applications such as microwave power amplifiers in the l~5 GHz range, powers > l00 W and operating temperatures > 425^{0}C. The devices show very promising direct current characteristics. Figure 2.12 shows the trend of current gain for nitride HBTs [34]. The only disadvantage is the electronic properties of p-GaN. A large contact resistance and a high sheet resistance are responsible for the poor quality base.

Unipolar devices: Though unipolar devices (AlGaN/GaN HFETs) have set the state of the art for microwave power and noise performance, it is recognized that significant work remains for these technologies to become viable.

Figure 2.13 shows the main technical strategy of GaN based devices. It includes the comprehensive effort such as application of knowledge and experience from GaAs MMIC community as well as leverage from emerging GaN commercial developments.

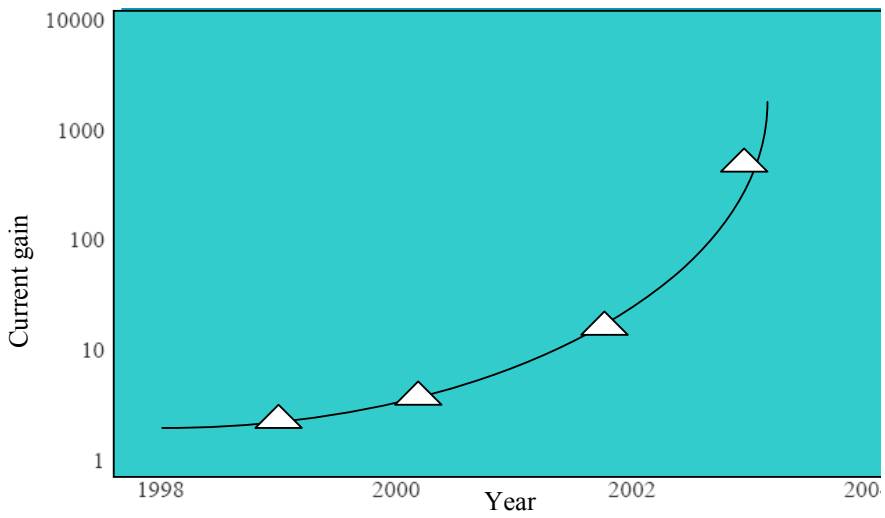


Figure 2.12: Trend of current gain for nitride HBTs [52]

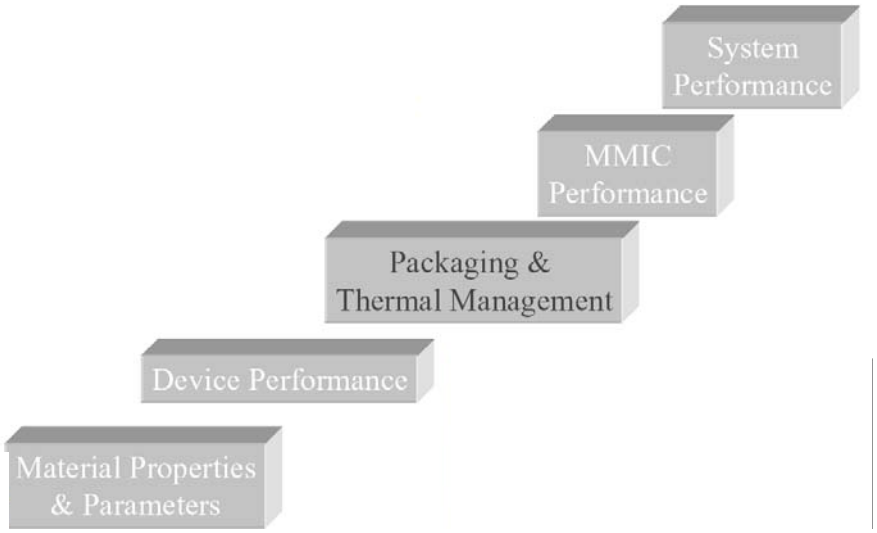


Figure 2.13: The main technical strategy for GaN [47]

2.4.1 SYSTEM BENEFIT

GaN based devices promise to provide high power density (> 1 W/mm), multi-octave bandwidth, high efficiency (> 50%), linearity, low noise figures and low phase noise. GaN is a strongly polar material [48, 52]. It leads to sheet charge accumulation on the end faces of crystal. So the total channel charge can be roughly four or five times higher than the AlGaAs/GaAs HEMT [49, 50-52,]. The results are important in realizing the device for high power and high speed applications.

The strain induced piezoelectric and spontaneous polarization charges have profound effects on device structures. In heterojunction devices such as FETs where strain and heterointerfaces are present, the polarization charges play an important role in device operation. As such, polarization affects device operation in all nitride based devices, particularly HEMTs, and thus must be taken into consideration in device design and analytical modeling. As mentioned above, polarization charge arises from two sources: piezoelectric effects and the difference in spontaneous polarization between AlGaN and GaN. Variations in composition, surface roughness, or strain distribution can alter the local distribution of polarization induced sheet charge density. Overall, compared with SiC devices, GaN-based devices on SiC substrates can

- Operate at even higher temperatures
- Have smaller on-state resistance
- Have higher operation current
- Operate at higher switching speed
- Have better reverse recovery characteristics

- Low thermal impedance (Grown on SiC substrates)
- High electron mobility
- High sheet carrier concentration at hetero interface
- High breakdown field

2.4.2 PROSPECTS OF AlGaN//GaN HEMTS

The HEMTs characteristics can be classified into DC and RF based on critical parameters, reliability, and uniformity. The critical parameters are the maximum drain current, the threshold voltage, the peak DC transconductance, breakdown voltage and output conductance. The gate geometry scaling on DC characteristics is also important. GaN HEMTs show negative resistance at high voltage and current. It is because of self-heating of the devices due to the poor thermal conductivity of sapphire [52].

The first AlGaN/GaN high electron mobility transistors (HEMTs) were demonstrated by Asif Khan *et al,* in 1994 [52]. Devices with 0.25 μm gate length showed a current density of 60 A/mm and a transconductance of 27 mS/mm. But no microwave power performance had been reported. Today state-of-the-art AlGaN/GaN HEMTs and amplifiers exhibit an output power density as high as 11 W/mm [36, 52] and a total output power of 51 W [47], respectively. AlGaN/GaN HFET materials on either sapphire or silicon carbide substrates now routinely demonstrate two-dimensional electron properties of over 1×10^{13} cm^{-2} carrier density and over 1500 $cm^2/V\cdot s$ mobility. Figure 2.14 summarizes the research publication time line for GaN FETs, HBTs, and conventional HBTs.

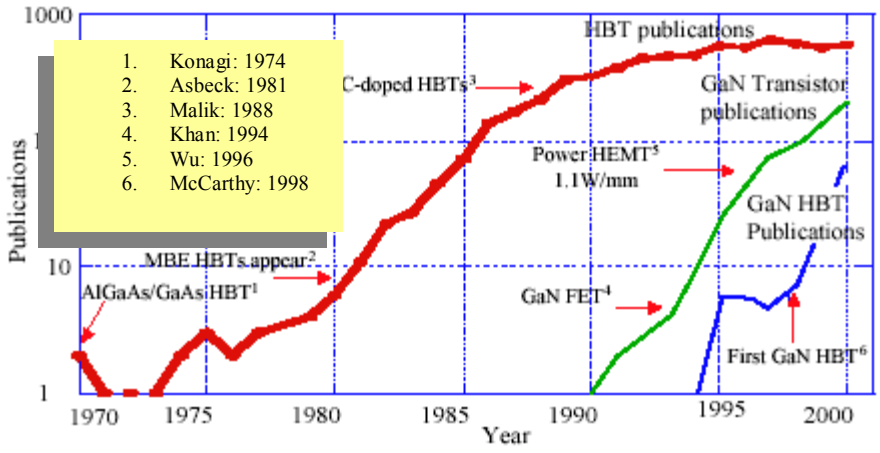


Figure 2.14: The number of INSPEC citations per year [52]

Figure 2.14 shows the number of INSPEC citations per year in a semi-log plot for conventional HBTs (red line), GaN HEMTs (green line), and GaN HBTs (blue line). A few selected points of interest for this time line are indicated above [52].

2.4.3 HEMT WITH OXIDE GATE

Research efforts have been driven to design and fabricate oxide gate HEMT for better performance. Most of the HEMTS made in the early days used GaAs and AlGaAs. But neither GaAs nor GaN has a native oxide. To utilize SiO_2 as the gate oxide of the HEMT device, one has to use silicon in the device. As a result, MOS gate HEMT has been fabricated by growing SiO_2 on the top of GaN/AlGaN heterostructure. But, there are still some problems of growing oxide in the MOS gate GaN/AlGaN HEMTs. MOS gate HEMT has number of advantages over the traditional Schottky gate HEMT. Some of the main characteristics are listed below:

- MOS gate HEMT has much smaller leakage current than that of Schottky gate HEMTs
- MOS gate HEMT is capable of accepting wider range of gate voltage swing than Schottky gate HEMT
- The transconductance is almost constant in saturation region
- MOS gate HEMT has much higher threshold voltage than Schottky gate HEMTs
- MOS gate HEMT offers much higher cut-off frequency
- MOS gate HEMT shows very high input resistance
- The operating range of gate voltage of MOS gate HEMT can be controlled by varying the thickness of the oxide layer

2.4.4 PROBLEM STATEMENT

GaN faces several challenges in the effort to produce semiconductor materials for electronics devices:

Substrates that are difficult to produce: Sapphire substrates, which are the most common, have a severe lattice mismatch with GaN, which leads to defects in the GaN layer. Silicon carbide used as a substrate has a much better lattice match, but has different thermal expansion properties than GaN, which leads to cracking. The ideal substrate to use would be bulk GaN crystals. Unfortunately, large single crystals of GaN are extremely difficult to make, requiring high temperatures (1800°C) and pressure (2 GPa). Other substrates such as $LiAlO_2$ [32], $LiGaO_2$ [33], Si [34] and AlN are also being investigated. The Si substrate is the cheapest and has the potential of integrating GaN

opto-electronics with Si devices. However, the growth of GaN on these substrates is still a new area.

GaN does not have a native oxide, which is required for MOS devices. For GaN, more studies are under way to find a suitable oxide; without it, GaN MOS devices are not possible.

High-temperature material growth process: It was found that serious deficiency of N atoms was induced on the GaN and AlGaN surfaces during various kinds of device processing such as high-temperature annealing, plasma cleaning, plasma etching and deposition of metal and insulation.

Defect proneness: Many failure mechanisms are related to trapping of hot electrons in the buffer and donor layer adjacent to the channel or on the surface. The large lattice mismatch and difference in thermal expansion coefficients between substrate and GaN films result in a high degree of stress, and therefore, a high density of defects is generated at the substrate/epitaxial film interface; these defects propagate into the growing film. Besides, additional works are still required to solve surface and interface related problems such as the gate leakage, trapping effects, etc.

Low hole mobility: The hole mobility in GaN is approximately 200 $cm^2/V/s$ especially in HBT devices [52]. The electronic property of p-GaN constitutes the poor base current, resulting in a high base resistance.

Other defects: The undoped GaN is n-type and usually has a high free electron concentration (10^{17} - 10^{18} cm^{-3}) at room temperature [52]. The dominant donor has not been identified; there is an intrinsic defect (nitrogen vacancy). In the nucleation technology of low-Al content AlGaN layers, it is necessary to "calibrate" each new boule

of sapphire, to find appropriate nucleation conditions [51, 52]. The high-Al content nucleation however seems to be largely insensitive to the surface finish of the substrate.

2.5 GAN RESEARCH GROUPS

The GaN research groups are undergoing significant growth as they move into exciting GaN based research areas. New collaboration with universities and industries are always welcomed throughout the world. Most of the research groups have strong collaboration and many exciting research projects under way. The main GaN research groups in the United States are:

- The University of South Carolina
- Sandia National Laboratories, NM
- The University of Nebraska, Lincoln
- University of Florida, Gainesville
- Microelectronics Center of North Carolina
- The University of Michigan, Ann Arbor
- University of California, Santa Barbara, CA
- Cornell University, NY
- Cree, Inc
- Defense Advanced Projects Research Agency
- Power Electronics Branch, Naval Research Laboratory Washington, D.C.
- The University of Tennessee, Knoxville

CHAPTER 3. MODELING OF ALGaN/GaN MOS GATE HEMT

In this chapter the analytical model for the MOS gate HEMT structure is discussed in AlGaN/GaN process. The verification of the model using experimental data is considered. MOS gate HEMT is described in section 3.1. The device structure for the proposed model of MOS gate HEMT structure is discussed in section 3.2, model formulation is described in section 3.3, the simulation results and analysis are discussed in section 3.4 and 3.5 respectively.

3.1 MOS GATE HEMTS

As promising candidates for future microwave power devices, GaN-based high-electron mobility transistors (HEMTs) have attracted much research interest [53-56]. An investigation of the operation of AlGaN/GaN n-type self-aligned MOSFET with modulation doped GaN channels is presented. GaN does not have a native oxide, which is required for MOS devices. For GaN, more studies are underway to find a suitable oxide; without it, GaN MOS devices are not possible. Liquid phase deposited (LPD) SiO_2 is used as the insulating material for the proposed device. To achieve the MOS gate structure there have been recent studies of various insulator on GaN including SiO_2, Si_3N_4, AlN, Ga_2O_3, Ta_2O_5, Si_3N_4, Sc_2O_3 [56]. An analytical model based on modified charge control equations is developed. The investigated critical parameters of the proposed device are the maximum drain current *(I_{dmax}),* the threshold voltage *(V_{th}),* the

peak DC trans-conductance *(g_m),* breakdown voltage *(V_{br}),* and unity current gain cut-off frequency *(f_T).*

3.1 DEVICE STRUCTURE

Figure 3.1 shows the cross-sectional schematic of the AlGaN-GaN 2DEG MOS gate HEMT structure. The device structure consists of 1 μm thick GaN quantum well channel separated by 10nm of undoped $Al_{0.35}Ga_{0.65}N$ spacer layer from 10nm thick n-type $Al_{0.35}Ga_{0.65}N$ supply layer. The function of the undoped spacer layer is to reduce impurity scattering. The proposed device consists of a Metal-SiO_2-n-Si (MOS) section. The structure of the device is shown with drain and source electrodes as ohmic contacts. The SiO_2 layer is about 50-100 nm thick and can be grown by the liquid phase deposition (LPD) process, which is a low temperature, low cost and reliable method [56].

A buffer layer can be grown on a SiC/Sapphire substrate. The composition of the layer controls the size of band discontinuity and quantum well formed in the heterointerface [58, 59, 60]. Also, the buffer layer, which acts as a virtual substrate, helps better confinement of the carriers in the quantum well.

AlGaN/GaN HFET materials on either sapphire or silicon carbide substrates now routinely demonstrate two-dimensional electron properties of over $1\times10^{13}cm^{-2}$ carrier density and over 1500 $cm^2/V.s$ mobility. These combined with materials' properties (compared in Table 3.1) of a high saturation electron velocity of 2.7×10^7 cm/s and a high breakdown field of over 3 MV/cm point to even better performance [57].

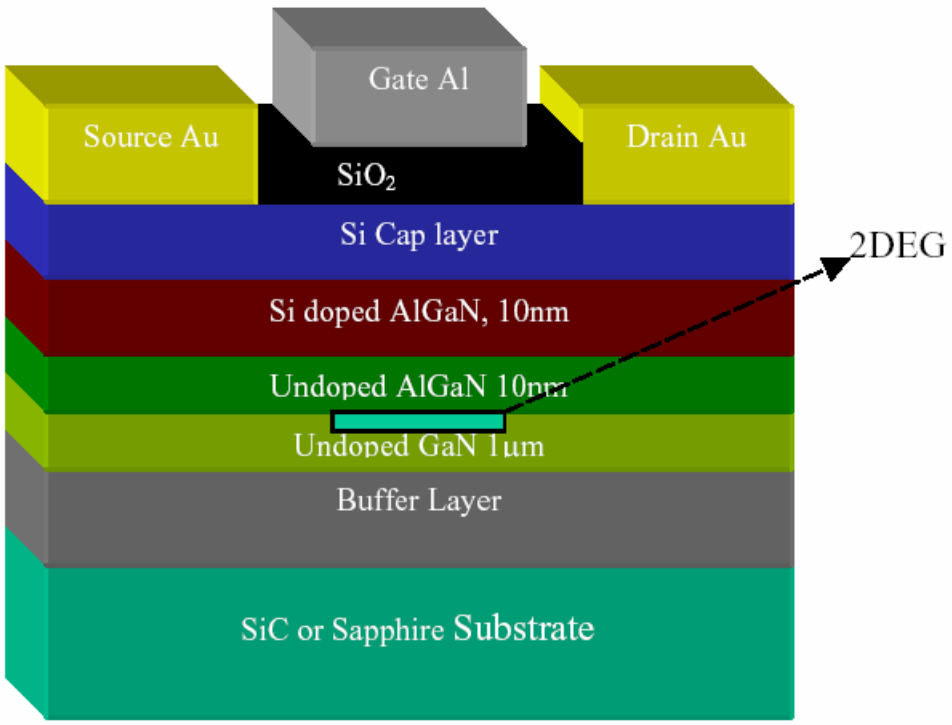


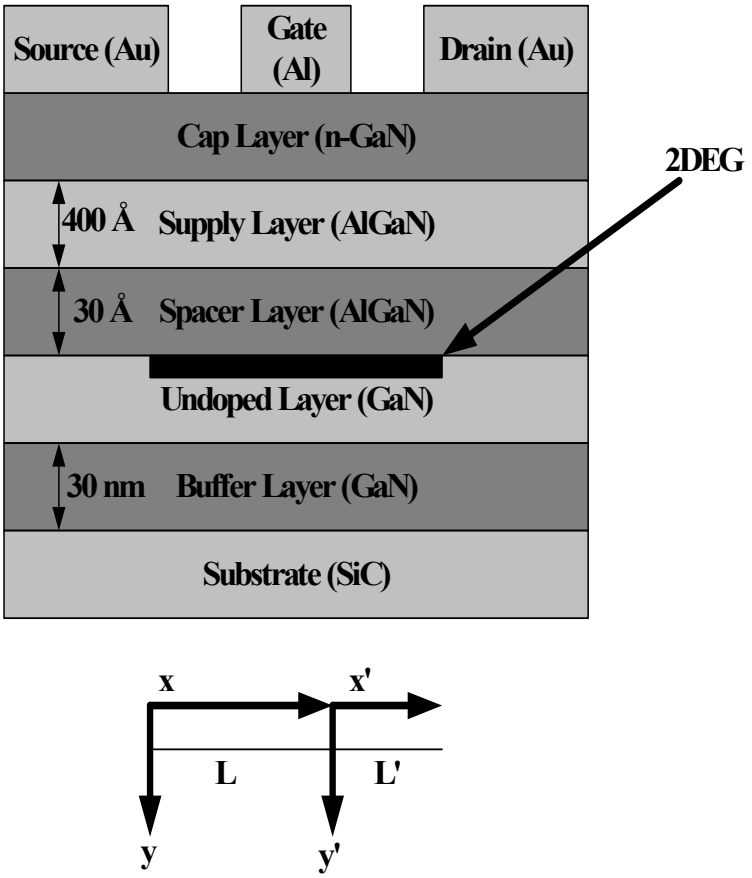
Figure 3.1: Structure of MOS Gate AlGaN/GaN HEMT

Table 3.1: Physical properties and device figures of merit [41]

	Band Gap (eV)	**Break down electric field (MV/cm)**	**Max Mobility (cm^2/Vs)**	**Velocity ($x10^7$)**	**Di-electric const.**
Diamond	5.45	10	3800 (Hole)	1	5.7
SiC	3.27	3.0	1000 (electron)	2.0	9.7
GaN	3.4	2.5	2000 (electron)	2.5	8.9
Si	1.12	0.3	1400 (electron)	1.0	11.8

Johnson's figure of merit (JFM) is used to compare power and frequency limits of a semiconductor. JFM of GaN is comparable to the other prominent material option for power devices [41]. However, devices based on GaN/AlGaN material systems have superior high frequency characteristics due to higher carrier density and mobility resulting from modulation doping.

The concentration of 2DEG is controlled by the application of gate voltage. HEMT structure is realized by implementing source and drain contacts as shown in figure 3.1. The doping concentrations and thickness of various layers are selected to provide adequate channel charge density. Figure 3.2 shows the approach of the proposed model. In the proposed model, the channel conductance in the saturation region and the parasitic resistance due to the undoped buffer layer are considered.



x and x' are the axis variable in the direction of current flow in the channel

y and y' are the axis variable in the direction perpendicular to the current flow in the channel

L is length of the low field region

L' is length of the high field region

Figure 3.2: Approach of proposed model

3.3 MODEL FORMULATION

In the present work, an analytical model is developed to characterize the performance of the proposed device. The effect of drain source parasitic resistances, thickness of each layer, doping concentration has been included. The cap layer effect is included in the capacitance calculation. But mobility variation, voltage dependence of the Fermi level has not been included. A threshold voltage for MOS gate HEMT has been reported in [13]. Here, the threshold voltage expression for an n-channel device has been derived without considering the effect of the cap layer.

The energy levels in the quantum well channel and the electron wave function inside and outside the quantum well are evaluated by self-consistently solving Schrödinger and Poisson's equations [14]. The gate voltage is expressed as:

$$V_G = V_{FB} + Q_d / C_{ox} + \Psi_s \tag{3.1}$$

The equivalent or total capacitance, C_{eq} can be given by,

$$1/C_{eq} = (d_d + d_i + \Delta d)/\varepsilon_2 + d_s/\varepsilon_{Si} + 1/C_{ox} \tag{3.2}$$

d_s= width of the cap layer (Å),

The equation for the threshold voltage without considering the cap layer is given in [6,7]:

$$V_{THn} = \phi_m - \chi_2 - \Delta E_c/q + E_{f0}/q - Q_{ox}/C_{ox} - qN_2 d_d / C_{ox} - qN_2 d_d^2 / 2\varepsilon_2 \varepsilon_0 \tag{3.3}$$

where, ϕ_m = gate metal work function (V)

χ_2 = The electron affinity of the supply layer (V)

ΔE_c = The conduction band offset (eV)

E_{f0} = The Fermi level at room temperature (eV)

Q_{ox} =The fixed oxide charge (coulomb)

C_{ox} = The gate oxide capacitance (pf)

N_2 = The supply layer doping (cm^{-3})

The drain current is obtained by using velocity-field dependence in Ref: [8],

$$I_D = G_0\left[V_G - V(z) - V_{th}\right]\left[1 - \exp\left(-\mu\xi_z / v_s\right)\right] \tag{3.4}$$

where, v_s are the saturation drift velocity, ξ_z is the electric field, μ is the low field mobility, and G_0 is given by:

$$G_0 = C_d v_s\left(L_1 + a * L_2\right) \tag{3.5}$$

where, L_1 is the width of the rectangular well, L_2 is the thickness of the supply layer, a* is the fringe factor, respectively. The unity current gain cut-off frequency f_T, the current voltage and the transconductance characteristics are obtained by following Chang and Fetterman's analytical model [14].

For a gate voltage exceeding a critical value, the AlGaN layer is not fully depleted. There is conducting current in the AlGaN layer, which causes the

transconductance to be suppressed The device structure consists of 1 μm thick GaN quantum well channel separated by 10 nm of undoped $Al_{0.35}Ga_{0.65}N$ spacer layer from 10 nm thick n-type $Al_{0.35}Ga_{0.65}N$ supply layer. The function of the undoped spacer layer is to reduce the impurity scattering. A 30 nm GaN buffer layer can be grown on a SiC/Sapphire substrate. The concentration of 2DEG is controlled by the application of gate voltage. The 2DEG channel is divided into two regions: low-field region $0 \le x \le L_1$, and the high-field region, $L_1 \le x \le L_2$, as shown in Figure 3.2. In this proposed model, the drain resistance is considered constant in the whole region. Actually, in the saturation region, there is a higher field region near the gate end, which causes the drain resistance to increase.

The extended model includes the channel conductance in the saturation region by solving the two-dimensional Poisson equation and the parasitic resistance due to the undoped GaN buffer layer. The small-signal parameters, transconductance, gate capacitance, and channel conductance are calculated for microwave performance. The drain current is given in [14] by,

$$I_D = qn_S(x)Zv(x) \tag{3.6}$$

where Z is the gate width and $v(x)$ the electron drift velocity.

The Gaussian Standing Wave (GSW) equation for velocity-field dependence is

$$v = v_S\left(1 - e^{-\zeta/\zeta_C}\right) \tag{3.7}$$

where v_S is the saturation drift velocity, μ the low-field mobility and $\xi_c = v_s/\mu$. The drain current equation can be written as follows:

$$I_D \int_{t_0}^{t_L} \frac{dt}{t^2 \ln(1-t)} = -\xi_C L G_0 \tag{3.8}$$

where,
$$t_0 = \frac{I_D}{G_0\left(V_G - V_{T0} - I_D R_S\right)} \tag{3.9a}$$

and
$$t_L = \frac{I_D}{G_0\left(V_G - V_{T0} - V_D + I_D R_D\right)} \tag{3.9b}$$

where, R_S is the source contact resistance and the resistance from the source to channel, R_D is the drain resistance.

The above equations describe the output *I-V* characteristics of HEMT's before saturation. To obtain saturation current and voltage, following boundary conditions are applied:

$$g_D = \partial I_D / \partial V_D$$

$$g_D = 0$$

At saturation, equation 3.9b can be expressed as follows

$$t_{L,sat} = \frac{I_{DS}}{G_0\left(V_G - V_{T0} - V_{DS} + I_{DS} R_D\right)} = 1 \tag{3.10}$$

Taking the derivative, the saturation transconductance is given by,

$$g_{ms} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{I_{DS}}{V_G - V_{T0} + \xi_C L \ln\left(1 - t_{0S}\right)} \tag{3.11a}$$

The gate capacitance in the saturation region is defined by,

$$C_G = \frac{\partial Q_S}{\partial V_G} \tag{3.11b}$$

Considering the infinite electric field and the electron drift velocity the potential at $x = L_1$ is,

$$V_{L1} = V_G - V_{T0} - \frac{I_C}{G_0} \tag{3.12}$$

where I_C is the current in the 2DEG channel.

The 2DEG channel current is considered only in the above equations. The channel current-voltage relation in the low field region, according to [14], is given by

$$L_1 = \frac{I_C C_2(t_0)}{\xi_C G_0} \tag{3.13}$$

where C_2 and G_0 is defined in [14]. In the extended model $x' = x - L_1$ is considered. For the high-field region, $0 \le x' \le L_2$, one needs to solve the two-dimensional Poisson equation

$$\frac{\partial^2 V(x', y')}{\partial x'^2} + \frac{\partial^2 V(x', y)}{\partial y^2} = -\frac{qN_D(y)}{\varepsilon_2} \tag{3.14}$$

The equation subjects to the following boundary conditions:

$$(a)\quad V(0, y)) = V_G + \frac{q}{\varepsilon_2}\left(\int_0^d N_D(y)dy - \frac{I_C}{qZv_S}\right)\cdot y - \frac{q}{\varepsilon_2}\int_0^y\int_0^y N_D(y)dy\,dy$$

$$(b)\quad \frac{\partial V}{\partial x'}(0, d) = \xi_0$$

$$(c)\quad V(x', 0) = V_G$$

$$(d)\quad \frac{\partial V}{\partial y}(x', d) = -\frac{I_C}{\varepsilon_2 Z v_S}$$

Boundary condition *(a)* ensures the continuity of the potential across the interface of the two regions. In the low field region, $x \le L_1$, it is assumed that in the depletion region the x component of the electric field is a slow-varying function and hence $\partial^2 V/\partial x^2 \approx 0$, and get condition *(a)*. One needs to make an assumption $\xi = \xi_0$ at in condition *(b)*, for the 2DEG channel. The electron drift velocity at $x' = 0$ is v_S and ξ_0 is infinite. But it is

physically not possible. For practical purpose it is assumed that ξ_0 is the electric field at which the electron velocity v reaches the value $0.99v_S$ in the high-field region. For condition *(c)* the metal gate is treated as an equipotential plane. Condition *(d)* shows that the y component of the electric field is discontinuous at the hetero-interface due to 2DEG.

3.4 SIMULATION RESULTS

There exists a conducting path in supply layer parallel to the channel. Due to this parallel conduction, the device transconductance goes down. The parallel conduction is not expected for normal HEMT operation. As a result, HEMT operation is usually restricted within the gate voltage range. The transconductance of the proposed device is smaller than the AlGaN/GaN HEMTs. This is because of the greater distance between the gate and the drain. The distance is due to the oxide layer thickness. This device offers small gate capacitance due to the dielectric constant of SiO_2. The oxide layer is also responsible for higher negative threshold voltage. The parameters used in the calculations are listed in Table 3.2.

Table 3.2: Materials parameters of the proposed model

Temperature	300°K	**Channel Width (Z)**	75μm
Spacer Layer Thickness (d_i)	10 nm	**Saturation Velocity (v_s)**	2.5×10^7 cm/sec
Supply Layer Doping (N_d)	2×10^{18} cm^{-3}	**Conduction Band Offset (ΔE_C)**	1.2 eV
Dielectric Constant of Supply Layer	$8.2\varepsilon_0$	**Electron mobility**	16×10^2 cm^2/V-sec

The output *I-V* characteristics with a 50nm SiO_2 layer are illustrated in Figure 3.3. The maximum source drain current is about 800mA/mm. Figure 3.4 shows the saturation current as a function of gate voltage. The transconductance decreases with the increase of gate length. The unity current gain cut-off frequency characteristic is shown in Figure 3.5. The maximum transconductance is about 200 mS/mm for the proposed device as shown in Figure 3.6. Figure 3.7 shows that the cut-off frequency (20-120 GHz) falls sharply with an increase in the gate length.

High transconductance is essential for high frequency. GaN possesses very attractive features such as high breakdown field ($5x10^6$ V/cm) [52] and extremely high peak saturation electron velocity ($3x10^6$ cm/s). Since it has high electron mobility, the proposed device offers lower on-state resistance [61, 62]. The high voltage capability of AlGaN/GaN HEMTs with gate-to-drain spacing of 1-2 μm offers a breakdown voltage of ~50 - 100 V [10] with the high channel current mentioned here.

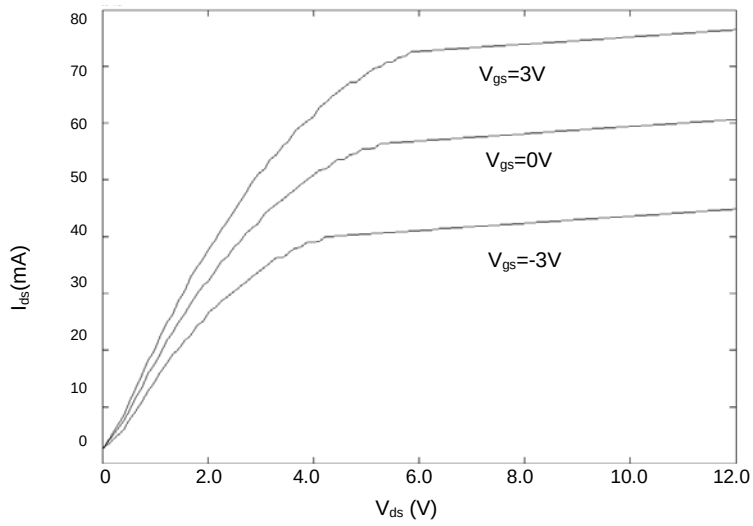


Figure 3.3: I_{ds}-V_{ds} characteristics of AlGaN/GaN MOS HEMT

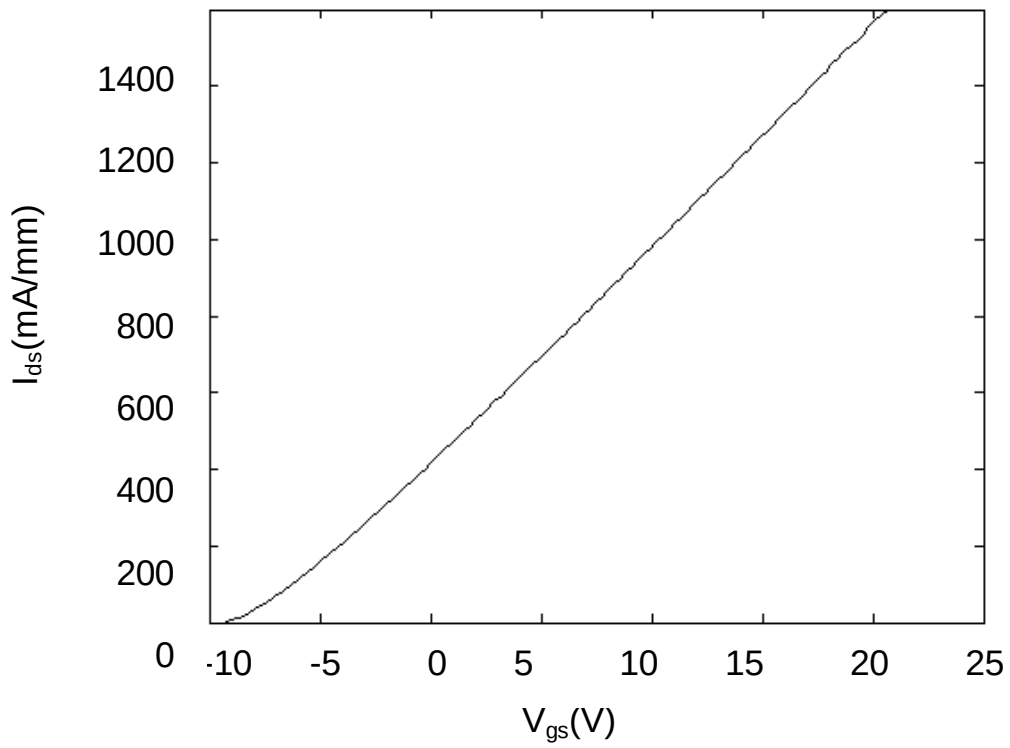


Figure 3.4: Comparison of the saturation current as a function of gate voltage

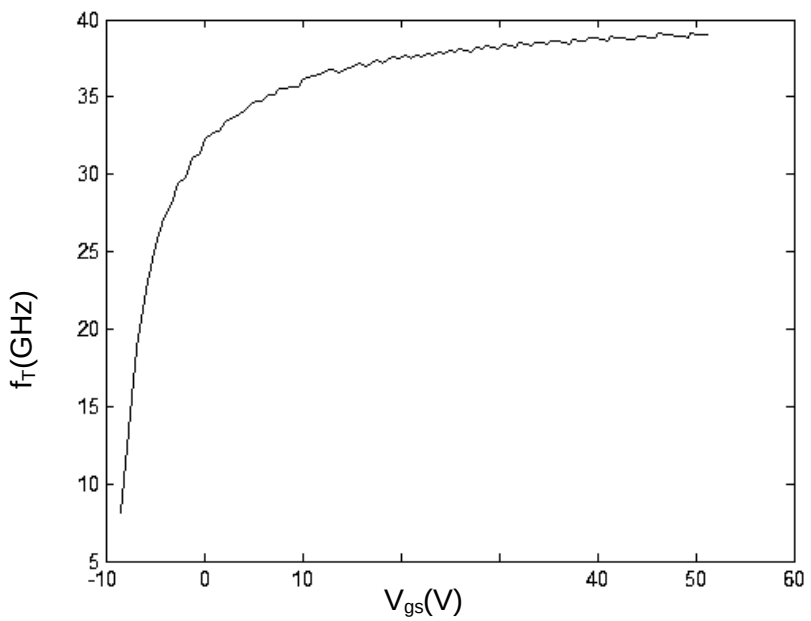


Figure 3.5: f_t-V_{gs} chracteristics at 300^0K

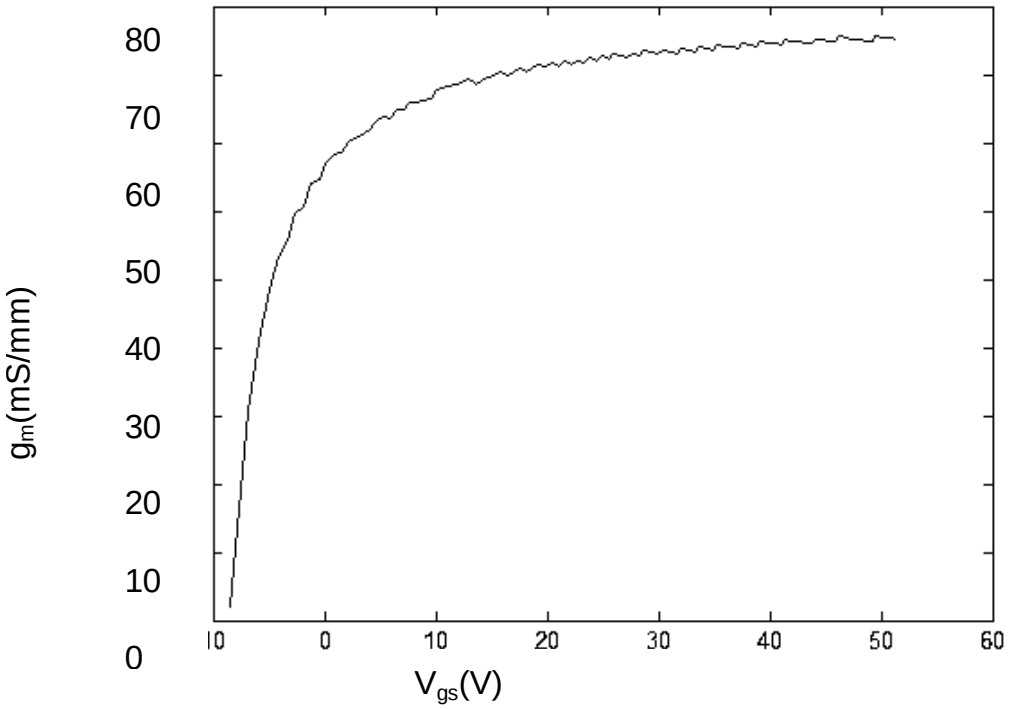


Figure 3.6: g_m-V_{gs} characteristics at 300^0K

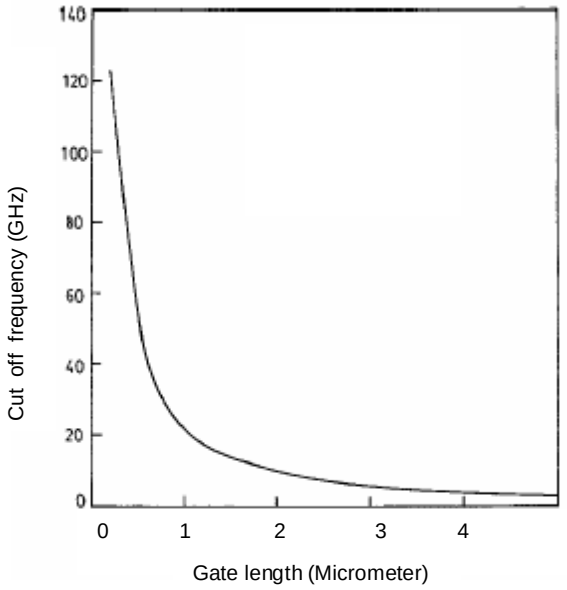


Figure 3.7: Variation of cut-off frequency with gate length

3.5 CONCLUSION

In this chapter, the results obtained from analytical model and simulations have been shown. The results so obtained are in close agreement with the experimental data. The effect of piezoelectric polarization is not considered here. AlGaN/GaN is an ideal heterostructure for achieving higher saturation velocity due to its energy band structure. GaN is a strong polar material. It leads to sheet charge accumulation on the end faces of crystal. So the total channel charge can roughly be four or five times higher than that of AlGaAs/GaAs HEMT [53]. The results are important in realizing the device for millimeter-wave and microwave frequency applications. Besides the electrical performance, the device represents its viability in power applications. To make proper use of the high voltage capability, the device must not be thermally limited. GaN HEMTs can be grown on SiC with a thermal conductivity of 3.3 W/cm·K [61]. GaN also has an advantage over GaAs in this regard, with thermal conductivities up to 2.0 W/cm·K for GaN versus 0.46 W/cm·K for GaAs. The high breakdown field and good thermal conductivity allow these devices to be used in high efficiency Class B push/pull amplifiers at full power rating [61].

CHAPTER 4. TEMPERATURE MODEL OF HEMT

The prime motivation for developing the proposed model of AlGaN/GaN microwave power device is to demonstrate its inherent ability to operate at much higher temperature. The analysis and simulation results on the transport characteristics of the HEMT structure is compared with the previously measured experimental data at room temperature. The calculated critical parameters suggest that the proposed device could survive in extreme environments. The device structure for the proposed model of HEMT structure is discussed in section 4.1, model formulation is described in section 4.2, the simulation results and analysis are discussed in section 4.3 and 4.4 respectively.

4.1 DEVICE STRUCTURE

High Electron Mobility Transistors (HEMTs) based on wide bandgap III-V nitrides and their alloys are useful as they offer (a) higher breakdown voltage due to its large bandgap (b) better thermal performance due to higher thermal conductivity and (c) superior frequency performance due to improved low field mobility and saturation velocity [53,63-67]. GaN based devices have attracted a great deal of interest in power, RF and opto-electronic devices [68]. HEMT, represent the third generation of compound semiconductor transistors provides several improvements over silicon technology [69]. With the high breakdown electric field much higher doping levels can be achieved in GaN based devices [45]. Thus, the device layers can be made thinner than Si at the same breakdown voltage levels [45].

One of the key issues for the development of microwave power HEMTs is the junction temperature. The large RF power density generated in these devices causes considerable self-heating. The effect of temperature on reliability is very important. The carrier mobility and saturation velocity reduces with the increasing temperature with resulting in degradation of DC performance [70-73]. Both short and long term reliability are key elements, which also reflect the need to rapidly calculate the temperature profile in a particular design. The extended model presented in this chapter includes the effects of temperature variation (100^0K-600^0K) on the energy gap, doping concentration, the carrier mobility and the saturation velocity. The model is verified at room temperature by comparing simulation results with previously measured experimental data reported in [68, 70, 73]. The model presented here includes the effects of temperature on the channel conductance in the saturation region and the parasitic resistance due to the undoped buffer layer. The approach shows better agreement with the experimental data.

This chapter presents design and analysis of a novel two-dimensional modulation-doped field-effect transistor (2D HEMT) in AlGaN-GaN material system for microwave and millimeter wave applications. Figure 4.1 shows the device structure. The device incorporates a quantum well channel for enhancement of carrier mobility. Modulation doping provides a separation of mobile charge carriers from ionized donors resulting in very high carrier mobility.

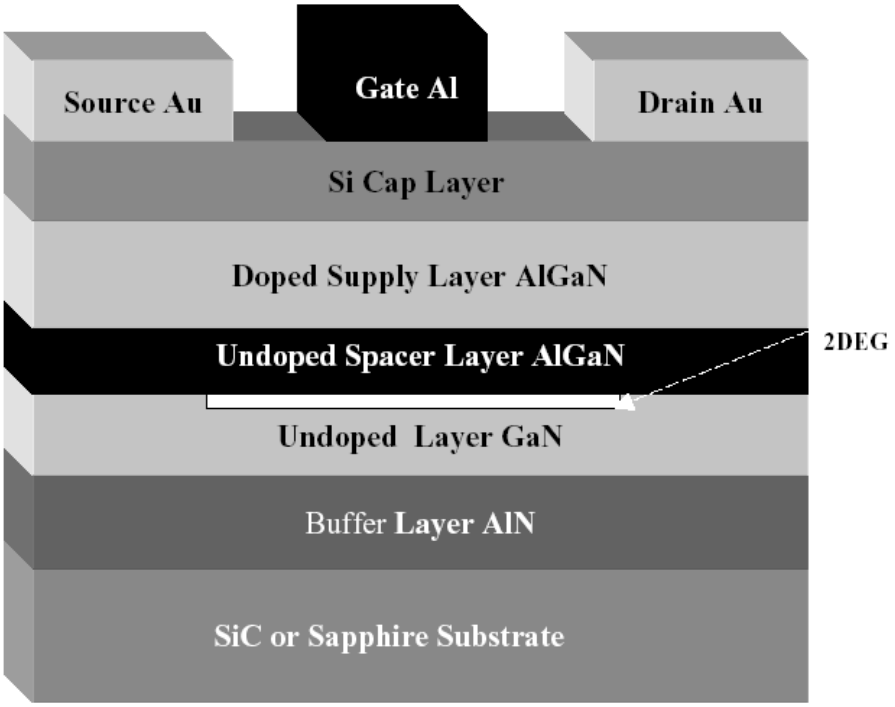


Figure 4.1: Device structure of the AlGaN/GaN HEMT.

Device schematic, charge distribution and energy band diagram for an n-channel HEMT is shown in Figure 4.2. In this figure, d_d, the width of supply layer is defined as the distance from the silicon interface to the supply layer/spacer layer interface. The charge accumulated in the metal gate due to the applied gate voltage V_{gs} is compensated by part of the charge in the depletion region of the supply layer. This charge is termed as Q_d. The rest of the charge in the depletion region is compensated by the charge in the two dimensional electron gas (2DEG) and a small charge due to the depletion layer formed in GaN channel. The device structure consists of 1 μm thick $Al_{0.35}Ga_{0.65}N$ quantum well channel separated by 30 Å of undoped $Al_{0.35}Ga_{0.65}N$ spacer layer from 400 Å thick n-type $Al_{0.35}Ga_{0.65}N$ supply layer. The function of the undoped spacer layer is to reduce the

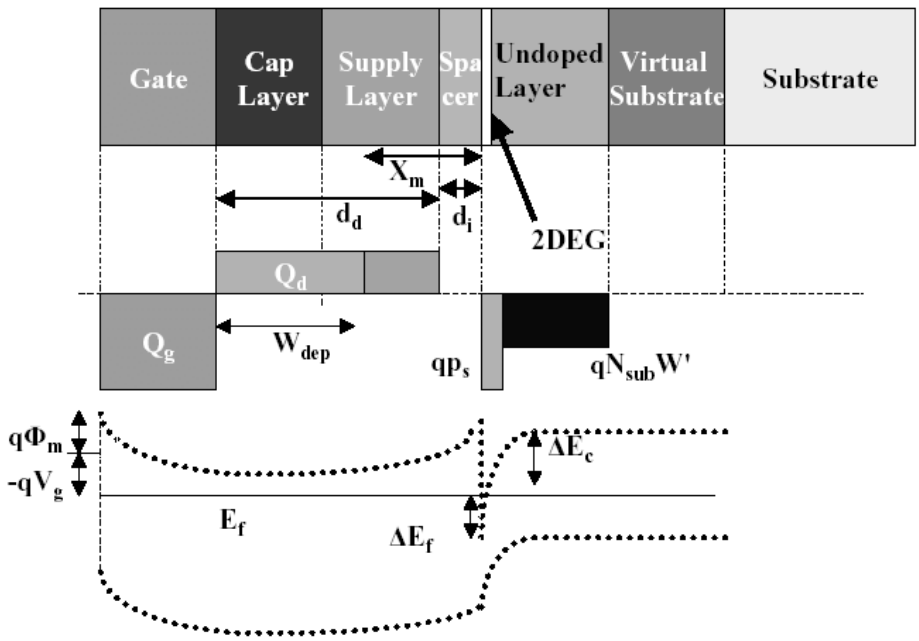


Figure 4.2: Device schematic, charge distribution and energy band diagram of the MOS gate n channel HEMT, used in the modified model

impurity scattering. The structure of the device is shown with drain and source electrodes as ohmic contacts. An AlN or GaN buffer layer can be grown on a SiC/Sapphire substrate. The composition of the layer controls the size of band discontinuity and quantum well formed in the heterointerface [72]. The concentration of 2DEG is controlled by the application of the gate voltage. HEMT structure is realized by implementing source and drain contacts. The doping concentrations and thickness of various layers are selected to provide adequate channel charge density.

4.2 MODEL FORMULATION

In general, the current in the saturation region is assumed to remain constant for the sake of simplicity [71]. In fact the drain current continues to increase in the saturation

region [71,75]. To explain this behavior, the channel conductance in the saturation region and the parasitic resistance due to the undoped buffer layer are considered. The two-dimensional Poisson equation is solved subject to some boundary conditions:

$$\frac{\partial^2 V(x',y')}{\partial x'^2} + \frac{\partial^2 V(x',y)}{\partial y^2} = -\frac{qN_D(y)}{\varepsilon_2} \tag{4.1}$$

Boundary condition ensures the continuity of the potential across the interface of the two regions. The 2DEG channel is divided into two regions: low-field region $0 \le x \le L_1$, and the high-field region, $L_1 \le x' \le L_2$. At $x = L_1$, the electric field is very high and the potential, V_{L1}, at $x = L_1$, is [71],

$$V_{L1} = V_G - V_{T0} - \frac{I_C}{G_0} \tag{4.2}$$

In the low field region, $x \le L_1$, it is assumed that in the depletion region the x component of the electric field is a slow-varying function and hence $\partial^2 V/\partial x^2 \approx 0$, and high-field regions, the electron drift velocity at $x' = 0$ is v_s and ξ_0 is very high. The voltage across the high-field region, $L_1 \le x' \le L_2$, therefore is given by

$$V(x',0) = V_G .$$

The term G_0 in Equation (2) is expressed as:

$$G_0 = \frac{Z v_s \varepsilon_2}{d} ,$$

V_G is the gate voltage, V_{T0} is the threshold voltage, I_C is the current in the 2DEG channel, Z is the gate width, $d = \Delta d + d_s + d_i + d_d$, Δd is the moment distance of the electrons from the heterointerface, d_s is the thickness of the cap layer, d_i is the thickness of the supply

layer, d_d is the thickness of the spacer layer, ε_1 and ε_2 are the permittivity of the supply layer and the cap layer respectively.

The charge densities of the two-dimensional electron gas (2DEG) can be expressed as a function of doping as well as spontaneous and piezoelectric polarization effects [73].

$$N_d\,(x) = N_s\,(x) + N_{pz}\,(x) \tag{4.3}$$

where N_s (x) is the sheet charge density due to the doping and N_{pz} (x) is the piezoelectrically induced polarization sheet charge. The drain current is given by,

$$I_D = qN_d(x)Zv(x) \tag{4.4}$$

where Z is the gate width and $v\,(x)$ the electron drift velocity.

The equivalent or total capacitance per unit area, C_{eq} is given by,

$$\frac{1}{C_{eq}} = \frac{\Delta d + d_i + d_d}{\varepsilon_2} + \frac{d_s}{\varepsilon_1} \tag{4.5}$$

Temperature dependency of energy gap (eV) for GaN is given in [74]:

$$E_g\,(T) = Eg\,(0) - 7.7x\,10^{-4}\,x\,T^2/\,(T+600) \tag{4.6}$$

The temperature-dependent mobility ($cm^2/V/s$) is reported in [74]

$$\mu_n\,(T) = -8.7\,x\,10^{-5}\,T^2 - 0.4T + 411 \tag{4.7}$$

The temperature dependent conduction band discontinuity is given by the following equation

$$\Delta E_c\,(T) = 0.65\,x\,\Delta E_g\,(T) \tag{4.8}$$

where ΔE_g is the difference in the bandgaps for AlGaN/GaN system. The Fermi level is expressed as $E_F = -q(\phi(0) - \phi(W)) + E_{F0}$ is reported in [75] where E_{F0} is the position of the Fermi energy with respect to the conduction band in the bulk GaN and $\phi(0) - \phi(W)$ is the total band bending. The temperature dependent threshold voltage is given by

$$V_{th}(T) = \phi_b(T) - \frac{\Delta E_c}{q}(T) - \frac{qN_d(T)d_1^2}{2\varepsilon_1} + \frac{\Delta E_{f1}}{q}(T) \tag{4.9}$$

To determine temperature dependent microwave performance, the transconductance and gate capacitance in the saturation region are very important. The saturation transconductance is given by,

$$g_{ms}(T) = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{I_{DS}(T)}{V_G - V_{th}(T) + \xi_C L \ln(1 - t_{0S})} \tag{4.10}$$

The unity current-gain frequency is then given by,

$$f_T(T) = \frac{g_{ms}(T)}{2\pi C_G} \tag{4.11}$$

The gate capacitance in the saturation region is defined by,

$$C_G = \frac{\partial Q_S}{\partial V_G}$$

where,

$$t_{os}(T) = \frac{I_{DS}(T)}{G_0\left(V_G - V_{th}(T) - V(x) + I_{DS}(T)R_D\right)},$$

$V(x)$ is the channel voltage and Q_s is the total charge in the channel. Many material parameters are the function of temperature and a number of empirical relationships have been obtained from the experimental data [68, 70, 75, 76]. Schrödinger's equation and Poisson's equation are solved simultaneously to evaluate and characterize the performance of these devices. The parameters used in the calculations are listed in Table 4.1.

4.3 SIMULATION RESULTS

Preliminary results from the analytical model and the measured data at room temperature presented in [68, 75] demonstrate the feasibility of the developed model. The output current voltage characteristics at room temperature are compared with the experimental data in Figure 4.3. In Figure 4.4, the output characteristics of HEMT show that saturation region starts at higher I_{ds} values at lower temperature. Due to high mobility at low temperatures, the current increases very quickly with the increment of V_{ds} in thelinear region. As the temperature goes up, mobility decreases. Figure 4.5 shows the effect of temperature on saturation current as a function of the gate voltage. The temperature effect on the cut-off frequency and transconductance behavior as a function of the gate voltage are presented in Figures 4.6 and 4.7 respectively. The analysis of the proposed model shows that the device demonstrates significant degradation at elevated temperature. The cut-off frequency falls sharply with an increase in the temperature. A small change in the threshold voltage due to the temperature variation causes a significant change in the output current.

Table 4.1: Materials parameters of the proposed device

Temperature	100-600 K	**Channel Width (Z)**	75μm
Polarization Induced Charge	~ $2x10^{13}$ cm^{-3}	**Saturation Velocity (v_s)**	1.66 ~ $2.6x10^7$ cm/sec
Supply Layer Doping (N_d)	$2x10^{18}$ cm^{-3}	**Schottky Barrier Height (ϕ)**	1~ 1.2 eV
Dielectric Constant of Supply Layer	$8.2\varepsilon_0$	**Electron Mobility**	4500-400 cm^2/V-sec

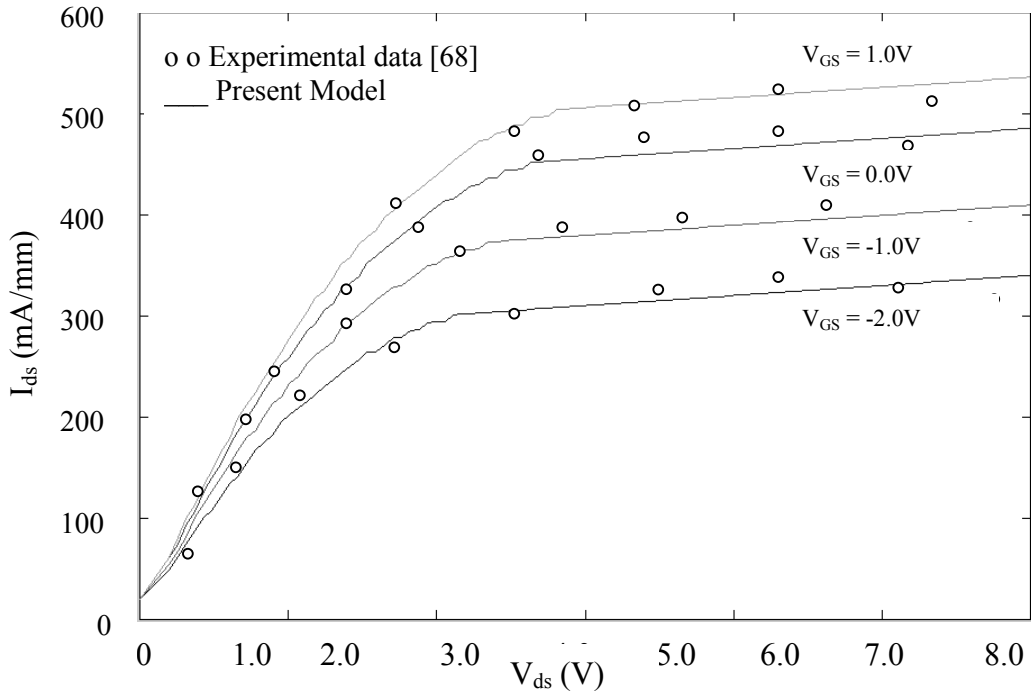


Figure 4.3: Current-voltage characteristics of AlGaN/GaN HEMT (300 ^{0}K)

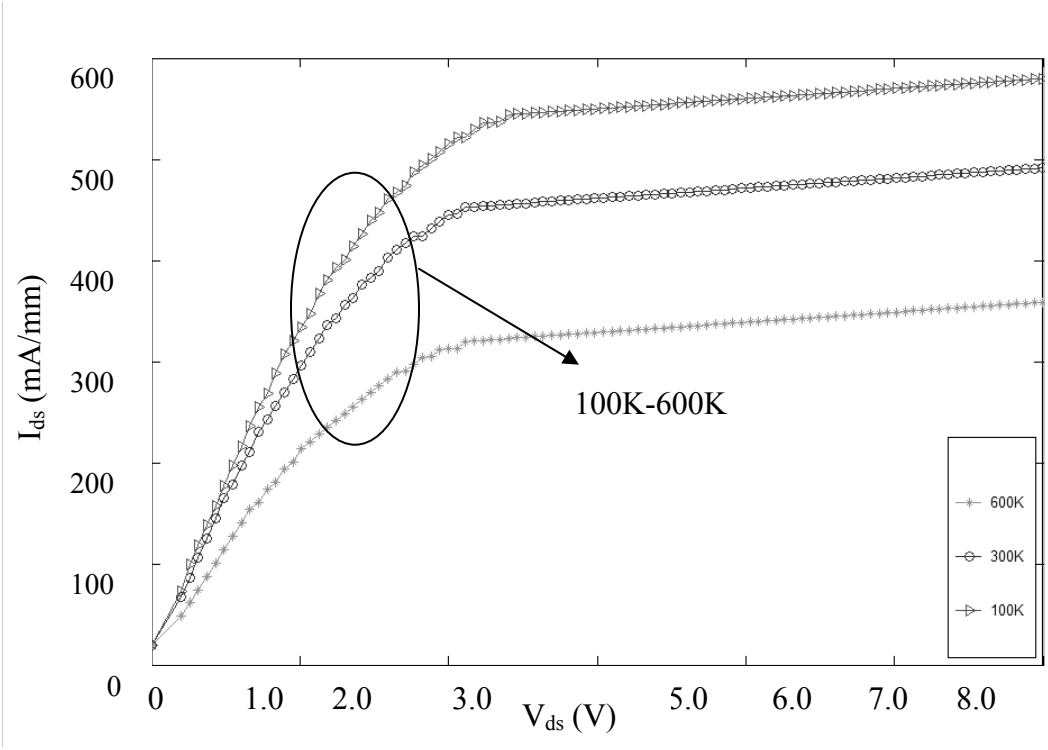


Figure 4.4: Temperature effect on the current-voltage characteristics (V_{gs} = 0.0V)

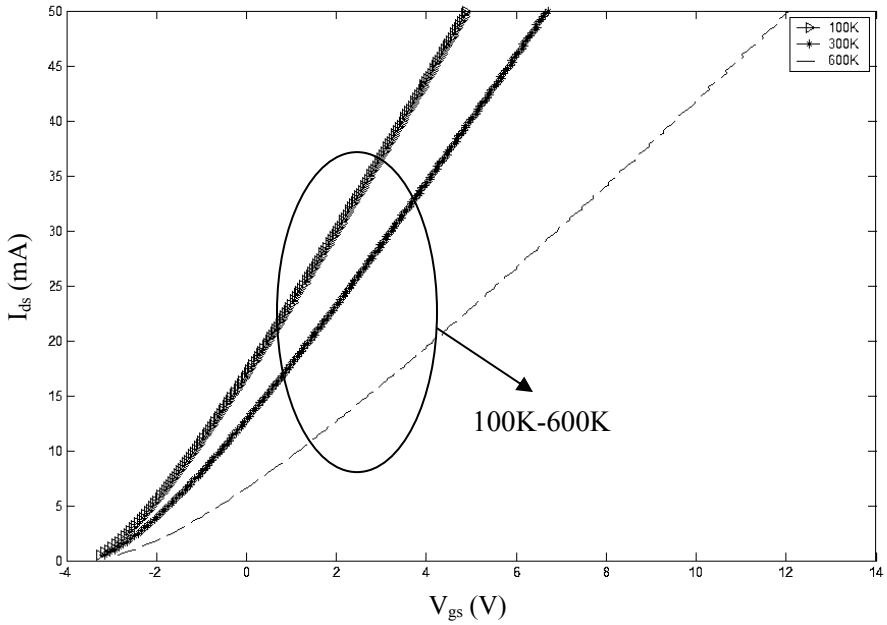


Figure 4.5: Effect of temperature on saturation current

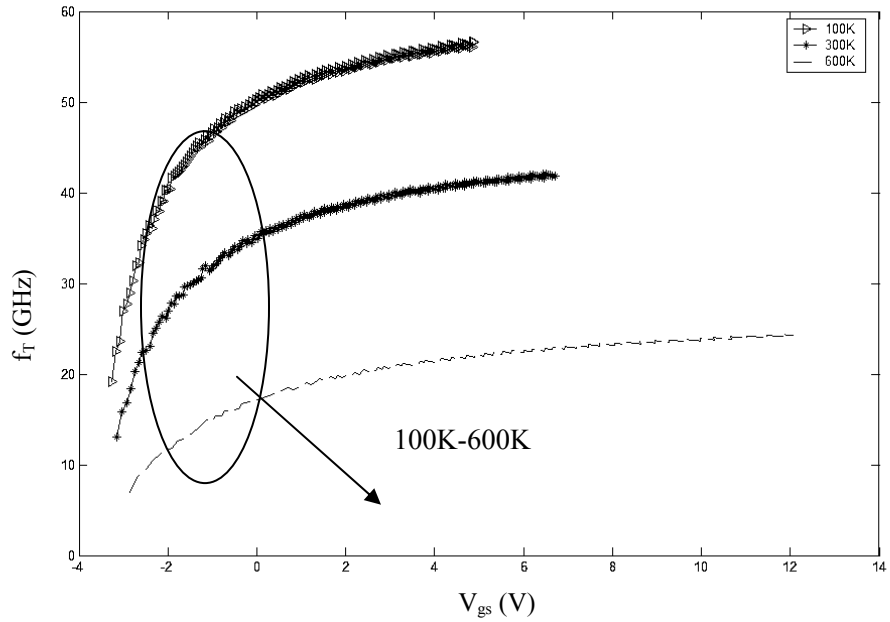


Figure 4.6: Temperature effect on unity gain cut-off frequency

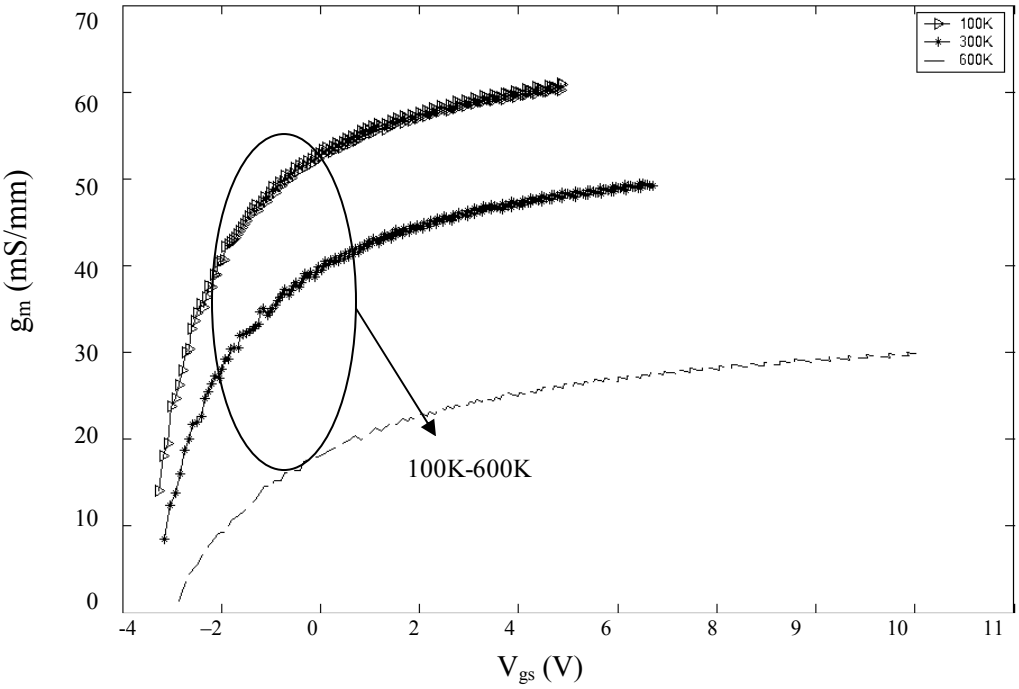


Figure 4.7: Temperature effect on transconductance characteristics

4.4 CONCLUSIONS

The proposed model demonstrates its viability in high power and high temperature applications. The calculations show that the proposed device performs stable operation at high current levels (~550 mA/mm) and can operate in the GHz range for temperature up to 600K. Operation of GaN HEMT at low temperature produces a substantial enhancement in device performance over room temperature. GaN HEMTs can be grown on SiC taking the advantage of its thermal conductivity [77-80]. Significant system benefits are anticipated for GaN based devices; however, there are many material and device challenges for them.

CHAPTER 5. TESTING AND CHARACTERIZATION OF THE HEMT

Measurement, testing, and characterization are the most critical steps to develop a reliable device model. This chapter focuses on the electrical and structural characterization of AlGaN/GaN heterostructures grown by metal organic chemical vapor deposition (MOVCD) to understand the formation of 2DEGs induced by spontaneous and piezoelectric polarization. Many different extraction methods have been developed. The appropriate methodology depends on the model and on the way the model is used. Proper test setup provides reliable data for parameter extraction. In the following sections, testing, characterization and parameter extraction of a GaN HEMT transistor are discussed.

5.1 TEST DEVICE STRUCTURE

The investigated epitaxial GaN layers, AlGaN/GaN heterostructures are grown by MOVCD process on SiC Substrates. A high temperature undoped GaN buffer layer with a thickness of about 2-4 μm is deposited before the growth of AlGaN. The piezoelectric polarization and the spontaneous polarization induced charges are responsible for the sheet carrier density. Modulation doping close to the AlGaN/GaN hetero-interface induces carriers in the undoped channel region. Even at the interfaces of intentionally undoped AlGaN/GaN heterostructures with high structural quality the formation of a 2DEG can be expressed because of free carrier background concentration. The electron sheet carrier concentration at room temperature is about 6.2×10^{13} cm^{-2}**.** Again very high

sheet carrier concentrations are observed if the Al-content is increased [81]. Free electrons have a tendency to compensate the high positive polarization induced sheet charge at the interface for N-face material. The maximum sheet carrier concentration located at these interfaces of the nominally undoped structures can be expressed as follows [81]:

$$n_S(x) = \frac{+\sigma(x)}{e} - \left(\frac{\varepsilon_0 \varepsilon(x)}{de^2}\right)\left[e\phi_b(x) + E_F(x) - \Delta E_C(x)\right] \tag{5.1}$$

The amount of the piezoelectric polarization in the direction of the *c*-axis can be determined by the following equation [81]:

$$P_{PE} = e_{33}\varepsilon_z + e_{31}\left(\varepsilon_x + \varepsilon_y\right) \tag{5.2}$$

The spontaneous polarization along the *c*-axis of the wurtzite crystal is as follows:

$$P_{SP}(x) = \left(-0.052x - 0.029\right) C/m^2 \tag{5.3}$$

In the absence of external electric fields, the total macroscopic polarization of a GaN or AlGaN layer is the sum of the spontaneous polarization in the equilibrium lattice and the strain-induced or piezoelectric polarization. Because of the sensitive dependence of the spontaneous polarization on the structural parameters, there are some quantitative differences in the polarization for GaN and AlN. Table 5.1 and Table 5.2 show the material parameters of the GaN test device. Table 5.1 includes spontaneous polarization, piezoelectric and dielectric constants of AlN, GaN, and InN [81]. Table 5.2 shows stress, polarization, electric field, sheet charge density, and sheet carrier density of relaxed and strained Ga-face and N-face AlGaN/GaN heterostructures.

Table 5.1: Material parameters of nitride material systems [81]

Wurtzite	**P_{sp}**	**e_{33} (C/m^2)**	**e_{31} (C/m^2)**	**e_{15} (C/m^2)**	**ε_{11}**	**ε_{33}**
AlN	-0.081	1.55	-0.58	-0.48	9.0	10.7
GaN	-0.029	1.0	-0.36	-.33	9.5	10.4
InN	-0.032		-0.57			

Table 5.2: Material parameters of the GaN test device [81]

Top/Bottom Layer	**Face**	**Stress**	**P_{sp} 10^{-6} (C/cm^2)**	**P_{pe} 10^{-6} (C/cm^2)**	**σ 10^{-6} (C/cm^2)**	**E 10^6 (V/cm)**	**n_s 10^{13} (cm^{-2})**
AlGaN/GaN x=0.3	Ga	Relaxed	-4.5	0	1.6	1.36	0.83
	N	Relaxed	4.5	0	-1.6	-1.36	
AlGaN/GaN x=0.3	Ga	Tensile	-4.5	-1.1	2.7	6.8	1.51
	N	Tensile	4.5	1.1	-2.7	-6.8	
AlGaN/GaN x=0.3	Ga	Compress	-2.9	0.97	-2.5	-2.29	1.42
	N	Compress	2.9	-0.97	2.5	2.29	

Variations in composition, surface roughness, or strain distribution will alter the local distribution of polarization induced sheet charge density. However, the total sheet charge, which is associated with the change of polarization across the interface region, will be very nearly equal to that present at an abrupt interface. The simulation results are based on the analytical model presented in chapter 3 and chapter 4. The AlGaN layer of the HEMT test device is considered as an undoped layer. The piezoelectric and spontaneous polarization induced charges are used to explain the very high sheet carrier concentration. The calculated maximum current density versus the current concentration experimentally determined is compared.

5.2 TEST SETUP FOR DC MEASUREMENTS

A custom DC measurement system was used to facilitate the DC characterization of GaN HEMT test device (Figure 5.1). DC characterization includes the measurement of device output characteristics (I_{ds} *vs* V_{ds}) and transfer characteristics (I_{ds} *vs* V_{gs}). These GaN HEMTs demonstrate excellent DC capabilities and can cause electric fields up to 3 MV/cm in group III-nitride crystal. For achieving design success it is very important to develop an accurate empirical and analytical model of the device. This research involves characterization, test and analytical model development of the GaN HEMT. The small-signal model can be extracted from different parameters under various bias conditions. Cascade Microtech Summit Probe series manual probe station was used for two primary measurement tasks: measurement of the output and the transfer characteristics of the test device. The overall measurement system is controlled using a laptop with a custom-design LabVIEW program. This program automates a number of functions by allowing

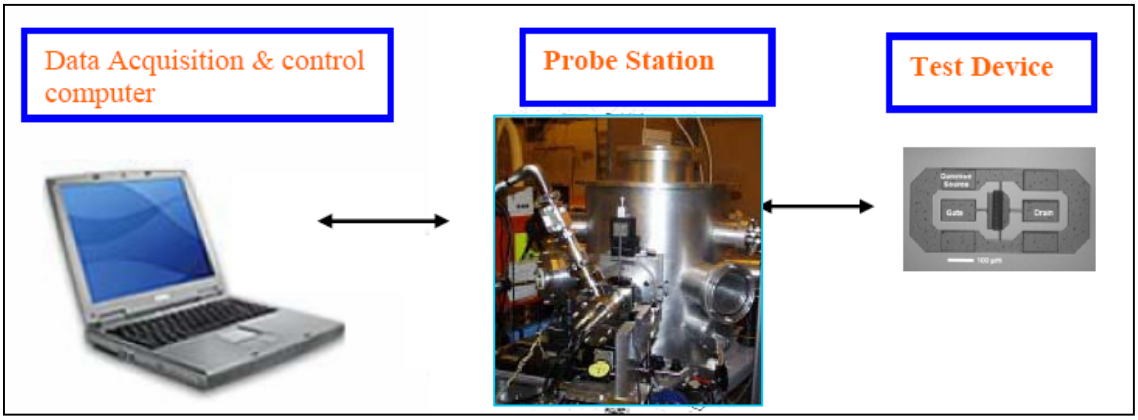


Figure 5.1: Test Setup for DC Measurements

the user to setup the experiment, initiate the program, and leave the unit to collect, display and save the measured data. The user selects the different bias conditions and graphical setup for the proper execution of the DC characterization. The output data is stored in a spreadsheet format allowing direct import into Excel graphing software.

5.3 CHIP LAYOUT

Figure 5.2 shows cross sectional schematic of the tested GaN device. The device structure consists of 2-4 µm thick GaN quantum well channel separated by 25 nm of undoped AlGaN. The GaN layer is grown on a SiC substrate. The composition of the layer controls the size of the band discontinuity and quantum well form in the heterointerface. In Figure 5.3 chip layout with dimensions are shown with dimensions. The yellow regions are dummy blocks. Each block has twelve devices with different gate length and width. The four transistors in the right most side are dummy transistors. Figure: 5.4(a) shows the layout of each device; 5.4(b) shows layout of TLM (Transfer

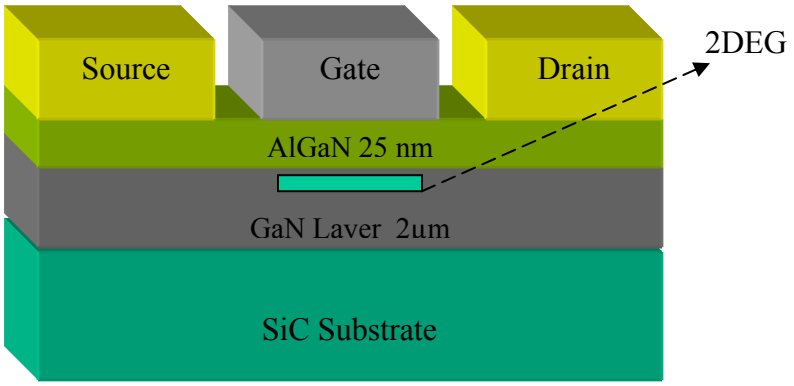


Figure 5.2: Cross sectional schematic of the tested GaN HEMT

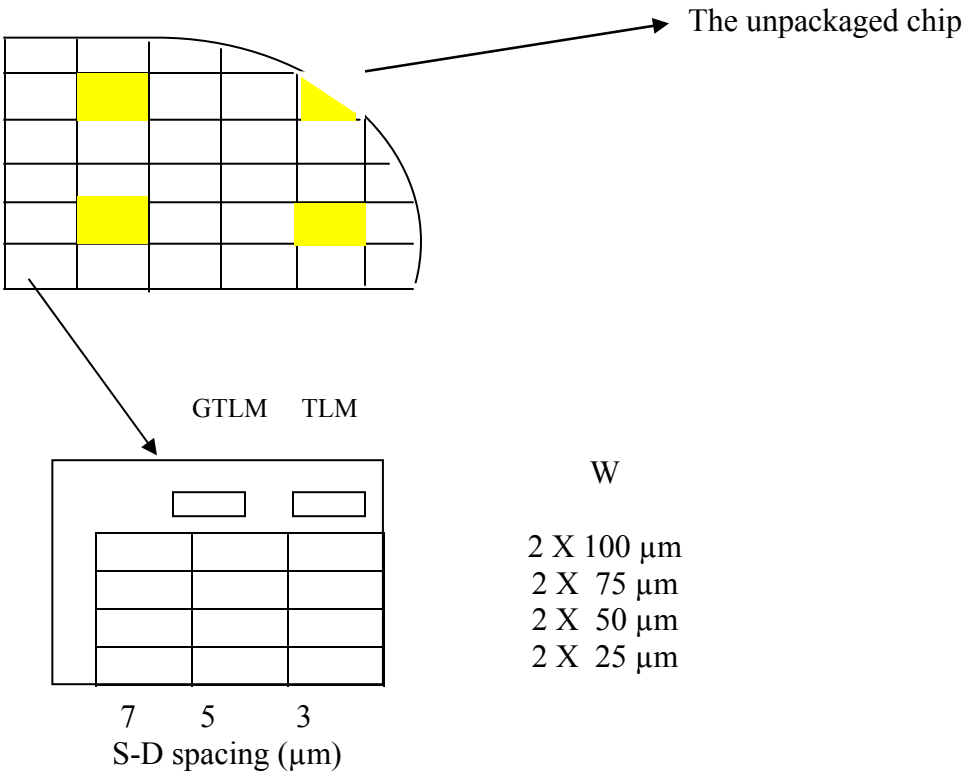
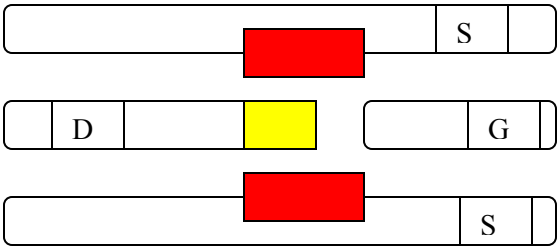


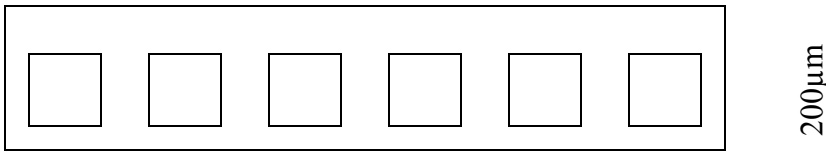
Figure 5.3: Chip layout with dimensions



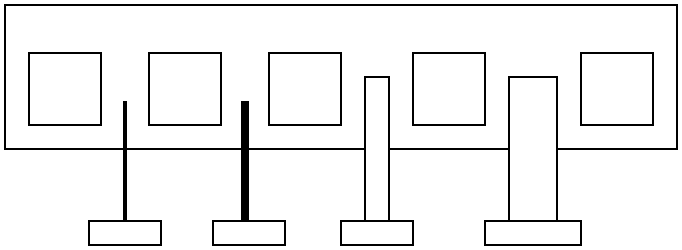
(a) Two parallel HEMTs

TLM: Transfer Length Method

GTLM: Gate Transfer Length Method



(b) TLM: Sheet resistance



(c) GTLM: HEMT with varying gate length

Gate length of 10 µm, 20 µm, 40 µm, 60 µm, 80 µm, and 100 µm.

S-G = 10 µm
D-G = 10 µm

Figure: 5.4(a) Layout of each block, (b) Layout of TLM (c) Layout of GTLM

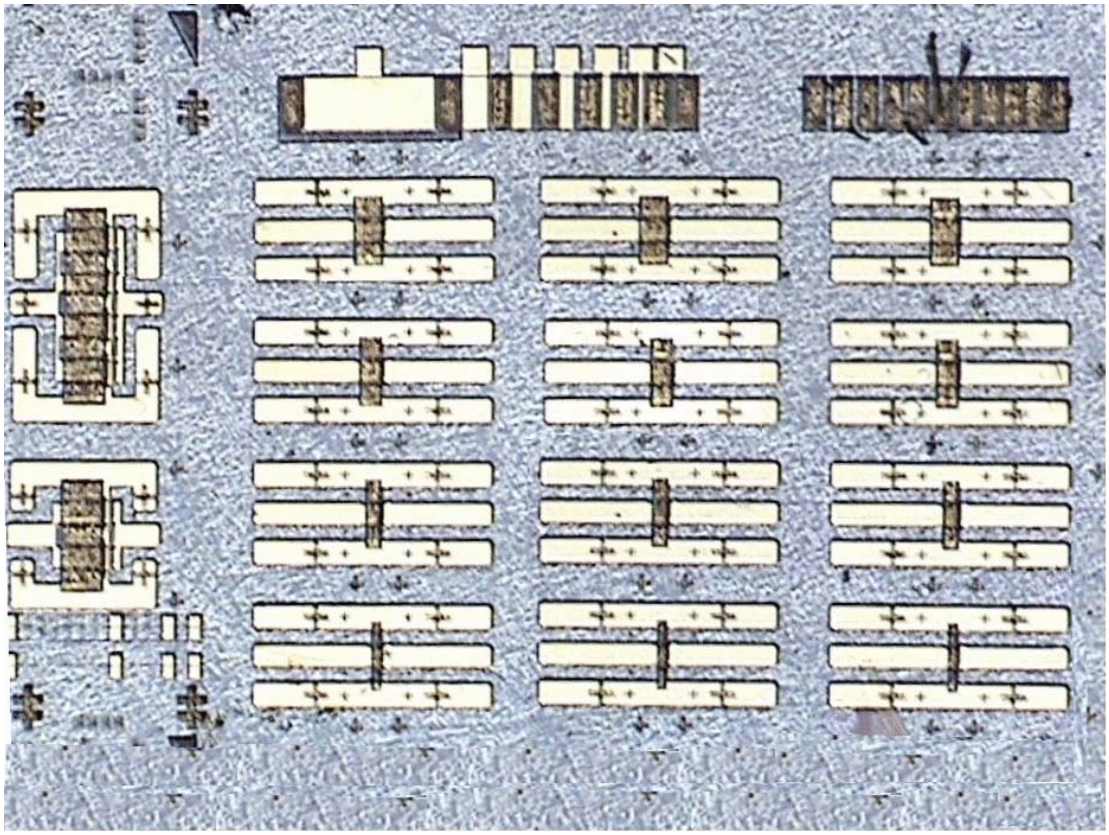


Figure 5.5: Microscopy image of AlGaN layers grown on GaN with varying gate length by MOCVD process.

Length Method); and 5.4(c) shows the layout of GTLM with a gate length of 10 μm, 20 μm, 40 μm, 60 μm, 80 μm, and 100 μm. The source-gate and drain-gate separation is 10 μm. Microscopy image of AlGaN/GaN HEMTs grown on SiC with varying gate length by MOCVD process is shown in Figure 5.5.

5.4 DATA AND RESULTS

The transfer characteristics are measured at different V_{ds} values from 5V to 15V. The transfer characteristics at V_{ds}=15V are shown in Figures 5.6 – 5.9.

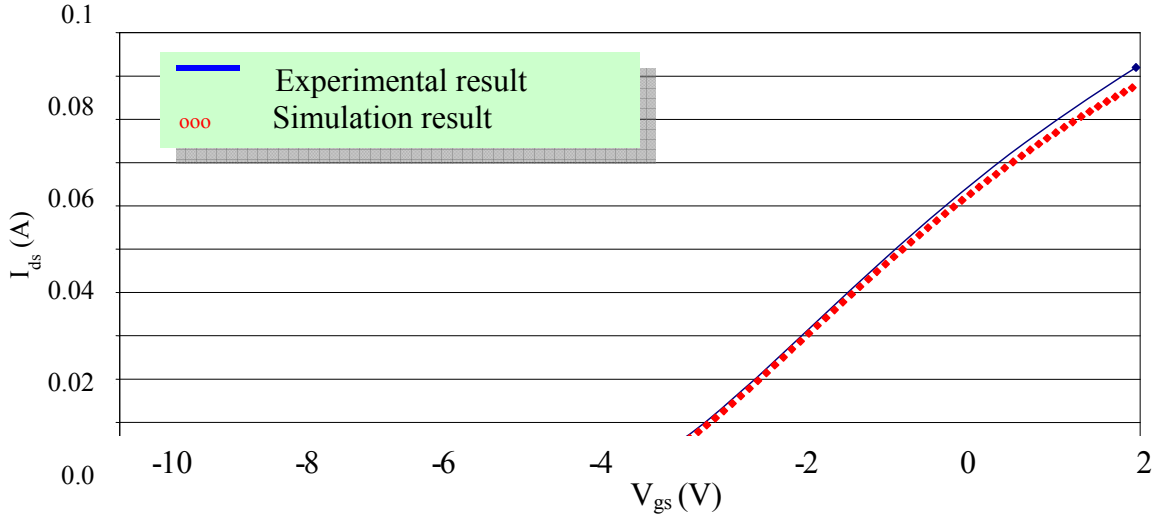


Figure 5.6: Output current as a function of gate voltage in saturation region (V_{ds} =15V, W/L = 200μm/5μm)

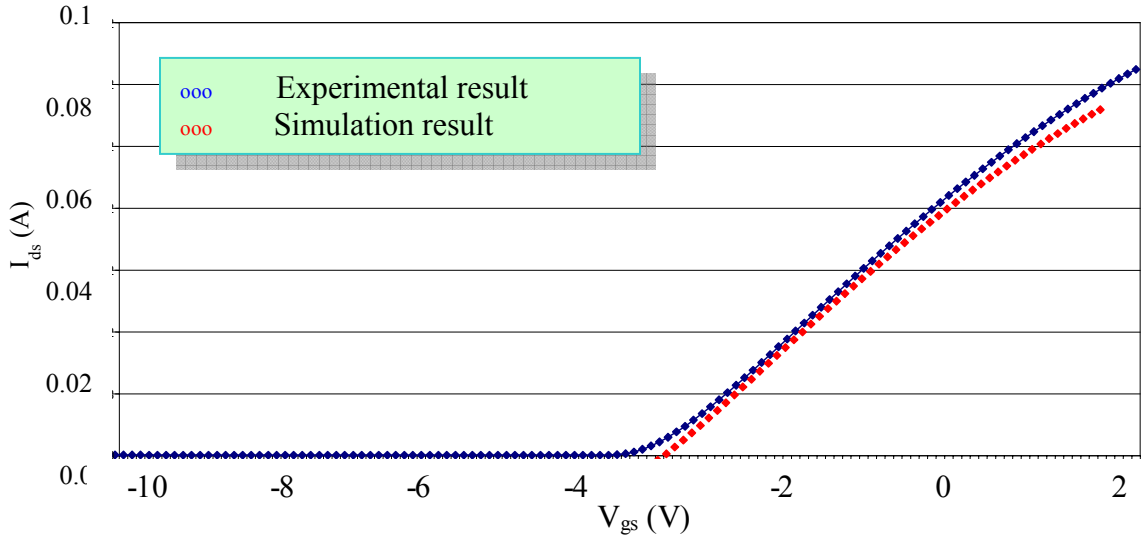


Figure 5.7: Output current as a function of gate voltage in saturation region (V_{ds} =15V, W/L = 200μm/7μm)

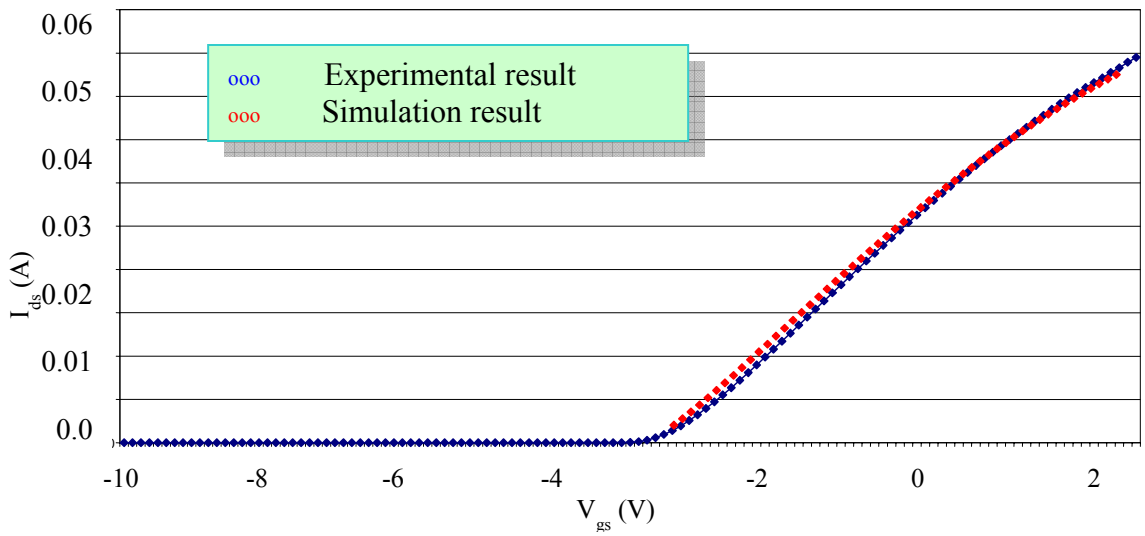


Figure 5.8: Output current as a function of gate voltage in saturation region (V_{ds} =15V

W/L = 100μm /5μm)

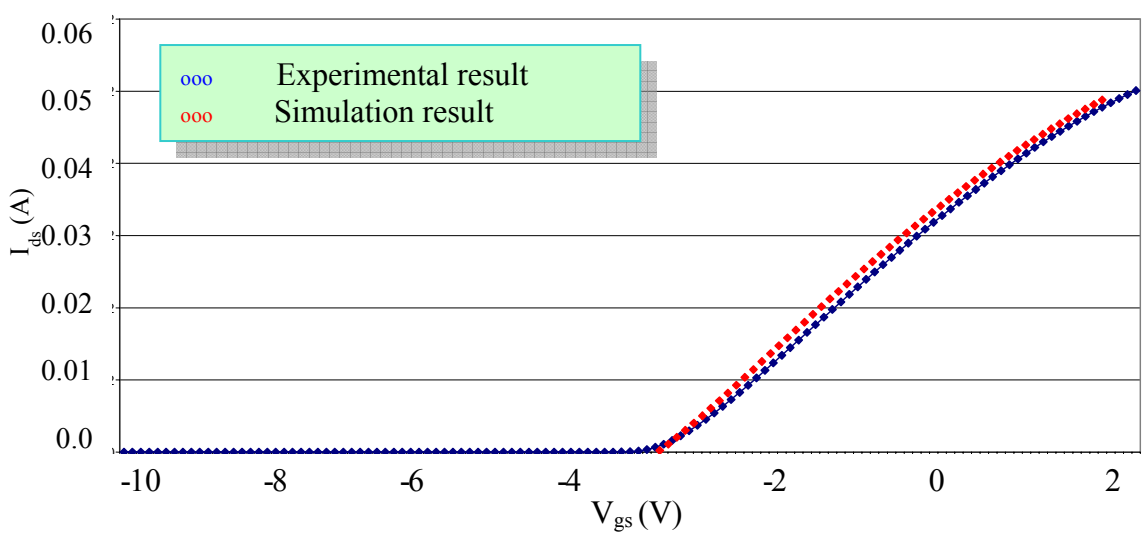


Figure 5.9: Output current as a function of gate voltage in saturation region (V_{ds} =15V,

W/L = 100μm /7μm)

The simulations are in good agreement with the measurements. The transfer curve shows different slopes and threshold voltage values for different V_{ds} and different *W/L* ratios.

It is known that piezoelectric effects can exert a substantial influence on charge density and electric field distributions in strained zincblende semiconductors. At the interfaces of intentionally undoped AlGaN/GaN heterostructures with high structural quality, the formation of a 2DEG can be expected because of the free carrier background concentration in the active GaN and the AlGaN barrier layers or carrier injection from metal contacts.

The electron effective mass in GaN is $0.22*m_0$; that is about three times higher than the effective electron mass in GaAs, and as a result the low-field mobility of bulk GaN is much less than that of GaAs. GaN has a larger peak electron velocity, larger saturation velocity, higher thermal stability, and a larger band gap, very suitable for the use as channel material in microwave power devices. Further contributing to the outstanding performance of AlGaN/GaN based HEMTs is the ability to achieve two-dimensional electron gases (2DEG) with sheet carrier concentrations of 10^{13} cm^{-2} or higher close to the interface without intentionally doping.

The measured output characteristics of the GaN HEMT test device are shown in Figures 5.10 – 5.13 at room temperature. The drain current starts to increase for a gate voltage just below – 3.6V. Due to the resistance in the drift region and high carrier density in the channel, the transfer characteristics are usually measured at V_{ds}=15V. However, to compare the dependence of the threshold voltage on the drain voltage, transfer characteristics are measured at room temperatures with different V_{ds} values.

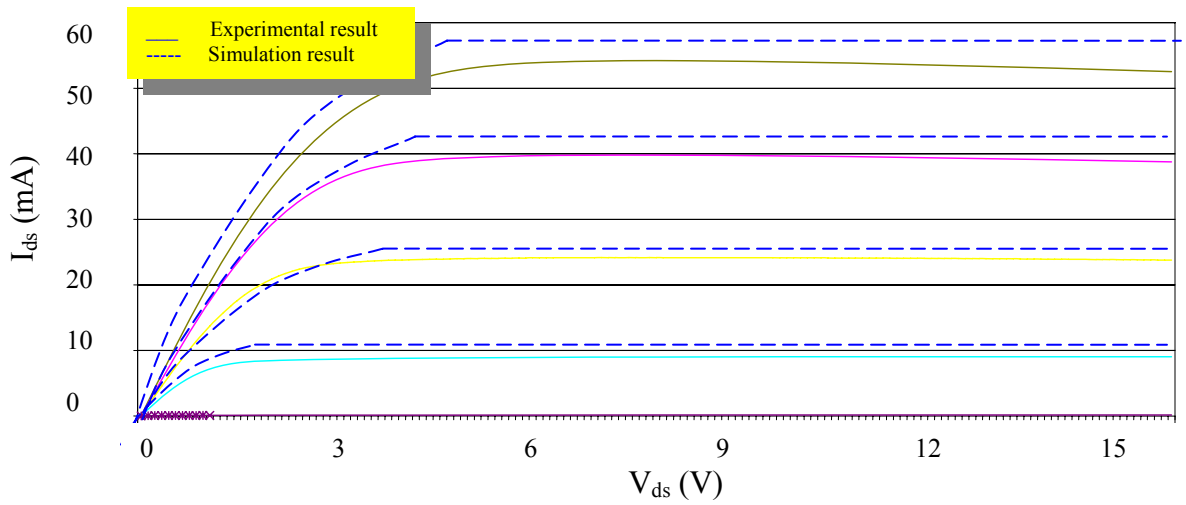


Figure 5.10: Drain current as a function of drain voltage

(W/L =100 µm/5µm, V_{gs} from 0V to -4V)

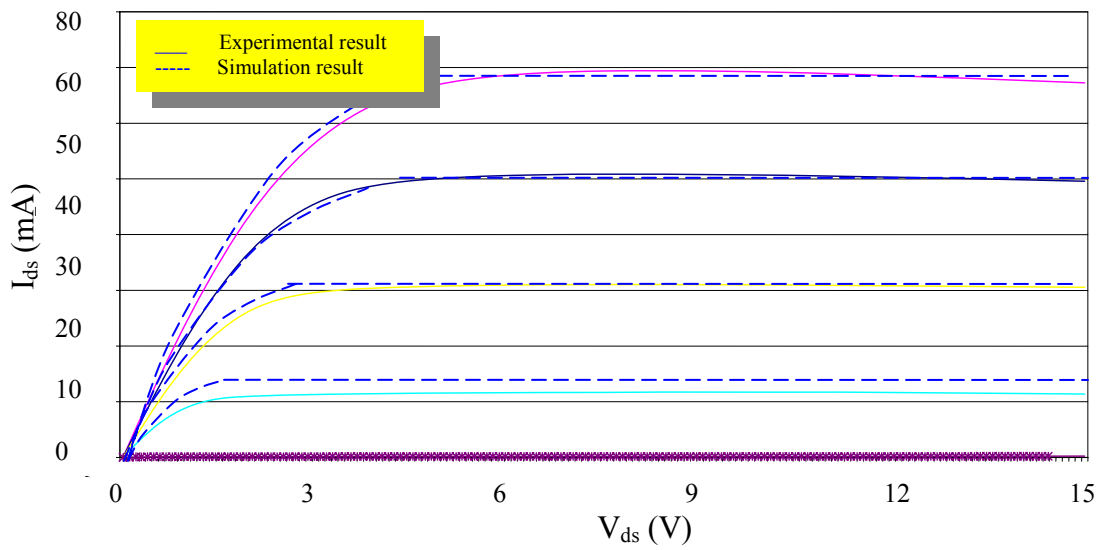


Figure 5.11: Drain current as a function of drain voltage

(W/L=200µm /7µm V_{gs} from 0V to -4V)

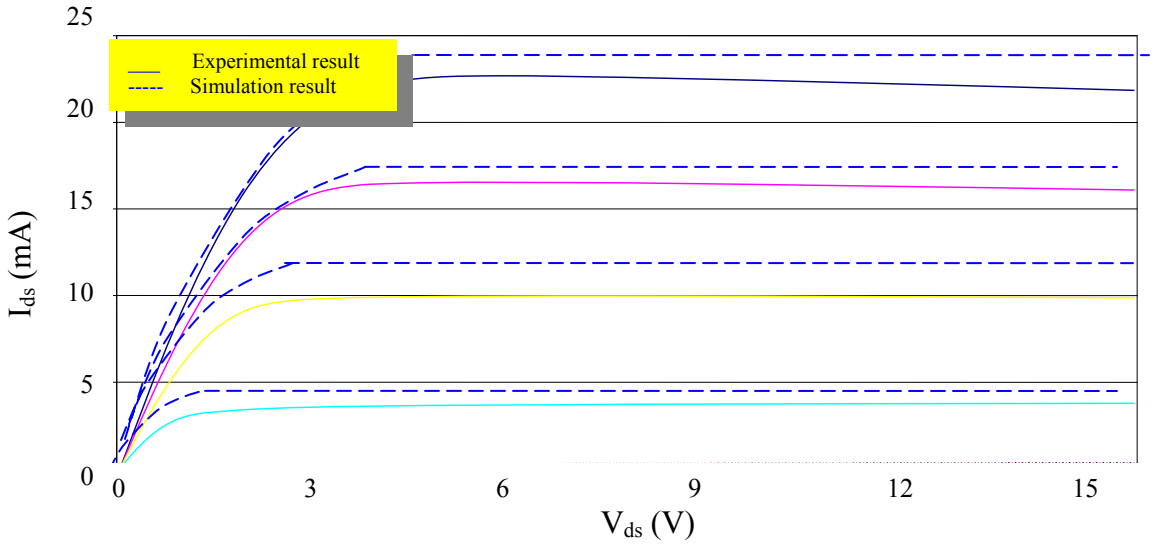


Figure 5.12: Drain current as a function of drain voltage

(W/L = 100μm/5μm, V_{gs} from 0V to -4V)

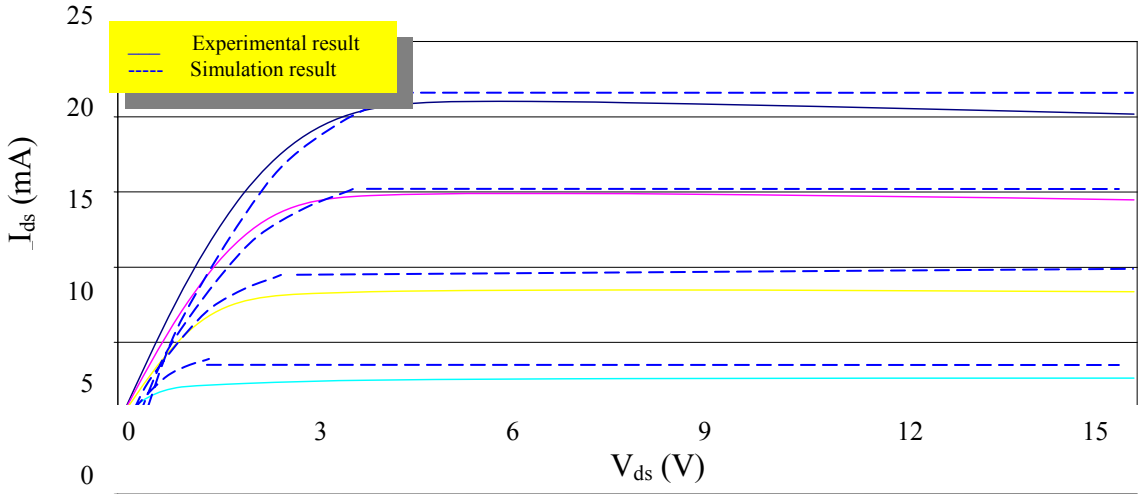


Figure 5.13: Drain current as a function of drain voltage

(W/L= 100 μm/7μm, V_{gs} from 0V to -4V)

The calculated value of the threshold voltage from the figures is -3.6V, which agrees with the calculated value from the analytical model. The drain currents at the saturation region rises to a value of about 25mA at V_{gs}=-4V and at V_{ds}=7V. The figures show the DC simulated and experimental output characteristics of HEMTs in GaN process for V_{gs} values varying from 0V to –4V in 1V steps. The agreement between the experimental and the simulation data is found very close. The output current from the experimental data decreases at saturation due to the effect of self-heating process. The results show that the presence of interface charges and traps is directly responsible for the observed current collapse. GaN based HEMTs are complicated device with multiple interferences. The interfaces play an important role in device operation. However, in the simulation not all the interfaces charges or traps are taken into consideration. A tangent is drawn at the linear region of the drain current characteristic to calculate the on-resistance. From the slope of the tangent, the calculated on-resistance, $R_{DS\text{-}ON}$ is obtained to be about 14Ω at a gate voltage of -4V. The value of the on-resistance varies as the gate voltage is increased.

5.5 SMALL SIGNAL ANALYSIS

Small signal model which is independent of amplitude, is a common analysis method to describe the non linear behavior of a device. GaN based HEMT transisitors used in electronic circuits, generally involve small time-varying signals carried over a DC bias point. The HEMT transistor small-signal AC model is a linear approximation to the exponential transfer curve around a DC operating point in the forward-bias region.

Figure 5.14 shows the small-signal equivalent circuit of a GaN HEMT. In this figure, gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} represent charging effect in depletion region; drain-source capacitance C_{ds} is small and its influence is insignificant. Capacitance C_{dsd} and resistance R_{dsd} represent model dispersion of *I-V* characteristic due to trapping effects in channel. Figure 5.15 shows the cross sectional schematic and the band diagram of a GaN HEMT including the trapping effects.

$$C_{\mathrm{gd}} = \frac{\partial\left(Q_{\mathrm{g}} + Q_{\mathrm{d}}\right)}{\partial V_{\mathrm{gd}}} \tag{5.3}$$

$$C_{\mathrm{gs}} = \frac{\partial\left(Q_{\mathrm{g}} + Q_{\mathrm{d}}\right)}{\partial V_{\mathrm{gs}}} \tag{5.4}$$

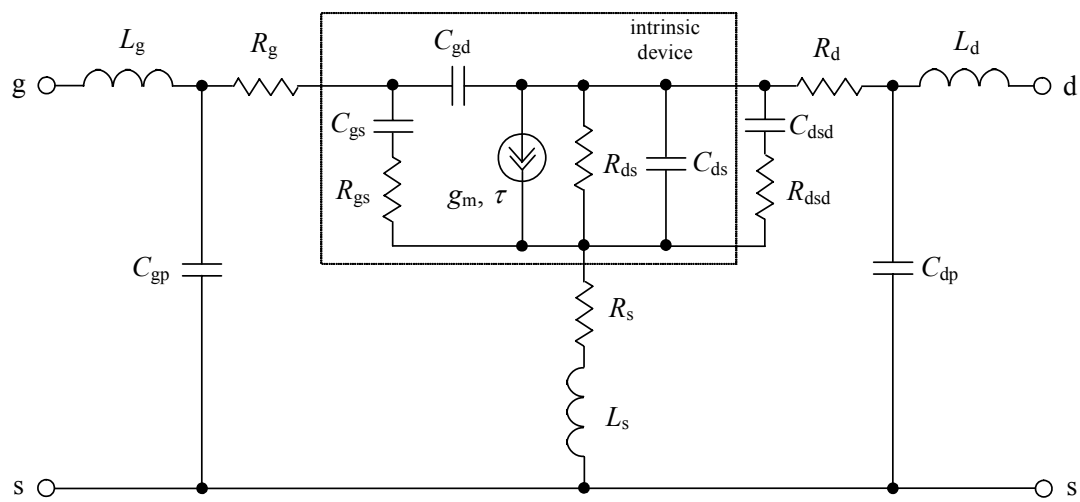


Figure 5.14: Small-signal equivalent circuit of GaN HEMT

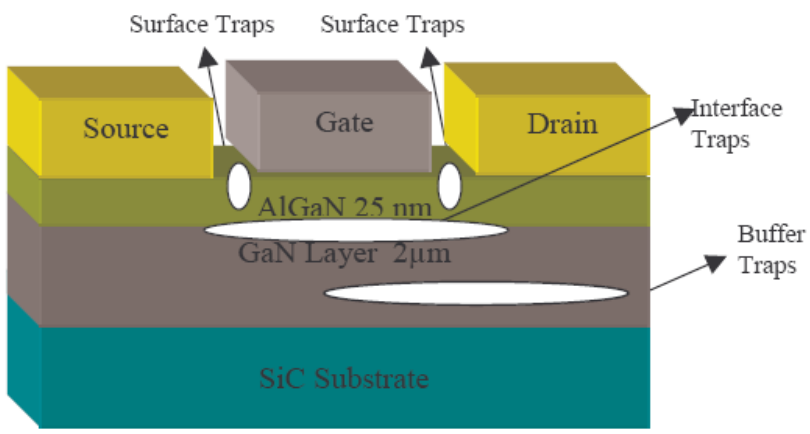


Figure 5.15: Cross-sectional schematic of GaN HEMT including the trapping effects

Determination of equivalent circuit parameters: To determine intrinsic circuit parameters, it is best to use Y-parameters for intrinsic device:

$$Y = \begin{bmatrix} \dfrac{j\omega C_{gs}}{1+j\omega\tau_g} + j\omega C_{gd} & -j\omega C_{gd} \\ \dfrac{g_m \exp(-j\omega\tau)}{1+j\omega\tau_g} - j\omega C_{gd} & \dfrac{1}{R_{ds}} + j\omega\left(C_{ds}+C_{gd}\right) \end{bmatrix} \tag{5.6}$$

where gate constant

$$\tau_g = R_{gs} C_{gs} \tag{5.7}$$

τ - effective channel carrier transit time

From real and imaginary parts of intrinsic Y-parameters:

$$C_{gd} = -\frac{\operatorname{Im} Y_{12}}{\omega} \tag{5.8}$$

$$C_{gs} = -\frac{\operatorname{Im} Y_{11} - \omega C_{gd}}{\omega}\left[1 + \left(\frac{\operatorname{Re} Y_{11}}{\operatorname{Im} Y_{11} - \omega C_{gd}}\right)^2\right] \tag{5.9}$$

$$C_{ds} = \frac{\operatorname{Im} Y_{22} - \omega C_{gd}}{\omega} \tag{5.10}$$

$$R_{gs} = \frac{\operatorname{Re} Y_{11}}{\left(\operatorname{Im} Y_{11} - \omega C_{gd}\right)^2 + \left(\operatorname{Re} Y_{11}\right)^2} \tag{5.11}$$

$$g_m = \sqrt{\left(\operatorname{Re} Y_{21}\right)^2 + \left(\operatorname{Im} Y_{21} + \omega C_{gd}\right)^2} \cdot \sqrt{1 + \left(\omega C_{gs} R_{gs}\right)^2} \tag{5.12}$$

$$R_{ds} = \frac{1}{\operatorname{Re} Y_{22}} \tag{5.13}$$

$$\tau = \frac{1}{\omega}\sin^{-1}\left(\frac{-\omega C_{gd} - \operatorname{Im} Y_{21} - \omega C_{gs} R_{gs} \operatorname{Re} Y_{21}}{g_m}\right) \tag{5.14}$$

A rigorous testing as well as characterization is carried out on a GaN HEMT transistor test device. SPICE parameters can be extracted from the measurements and a SPICE model for the HEMT transistor can be developed. The models developed in this research will not only help the GaN device researchers in the device behavioral study but will also provide a SPICE model for circuit designers.

CHAPTER 6. NUMERICAL SIMULATION

In this chapter, the numerical device simulators Medici™ and Sentaurus™ are performed. Some of the simulation results are used to examine the dependence of device and material parameters on device performance. Other simulations are compared to the analytical results obtained in previous chapters. The overall goal of the simulator is to analyze the behavior of the designed device as well as replicate processing steps under different biasing conditions.

6.1 INTRODUCTION TO MEDICI™

The Medici™/ Sentaurus™ device simulator allows the designer to import device models into the circuit simulations [82]. Then the designer can use the simulator to analyze the basic semiconductor equations of the circuit and characterize the device design under various biasing conditions.

All of the analysis will allow the designer to optimize the IC designs that are being developed. However the device simulators cannot replace design. These results should be used to reinforce or refute results taken from analytical models, hand calculations, and experimental results. Thus the simulation results are helpful for understanding of device physics and behavior.

Medici™ is an industry standard simulator used to predict the electrical characteristics of two-dimensional structures. On the other hand Sentaurus™ is used to predict the electrical characteristics of three-dimensional structures. The simulators are

capable of solving Poisson's equations, continuity equations, and energy balance equations.

It is also able to perform steady state, transient, and ac small signal analyses [82, 83]. Medici™ takes voltage bias at the electrode and uses that to determine the current at each terminal. A few of the devices that the software is capable of simulating include: diode, BJT, MOSFET, JFET, MESFET, HBT, IGBT, CCD, and GTO. Some of the capabilities of the simulator are as follows:

1) Determining *I-V* characteristics, gain and speed of transistors and diodes,
2) Understanding internal device operation through carrier temperature, field, carrier, and potential,
3) Analyzing and understanding breakdown mechanisms,
4) Refining device designs in order to achieve optimal performance, and
5) Investigating failure mechanisms (leakage paths and hot electron effects).

The output *I-V* characteristic is illustrated in Figure 6.1. The transfer characteristic of the HEMT device is shown in Figure 6.2. The simulator tries to solve each and every voltage bias at the electrode to determine the current at each terminal.

In the figures, the broken lines indicate that Medici™ is unable to calculate some of the voltage bais points for a specific current level due to its internal system limitations. The cross sectional schematic with potential regrid of the III-V based HEMT is shown in Figure 6.3. The different colors indicate the different layers of the HEMT device.

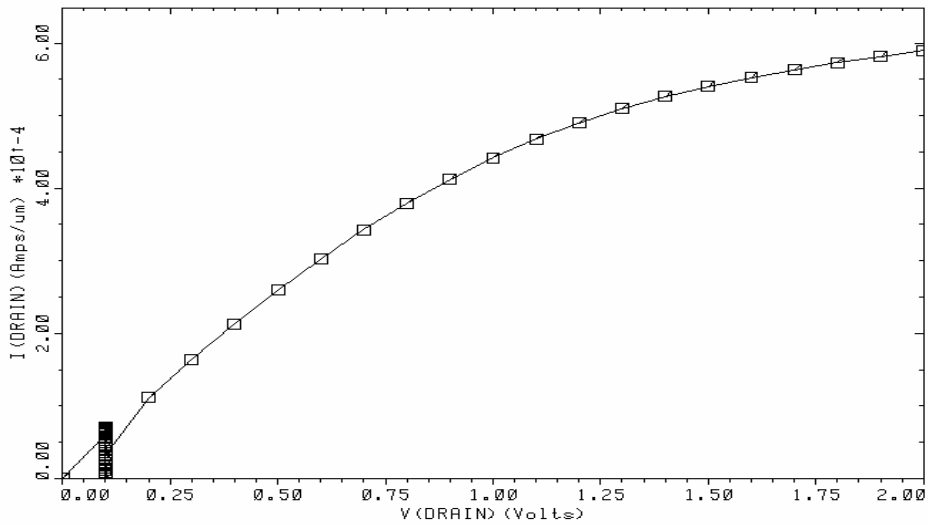


Figure 6.1: Output characteristics III-V based HEMT

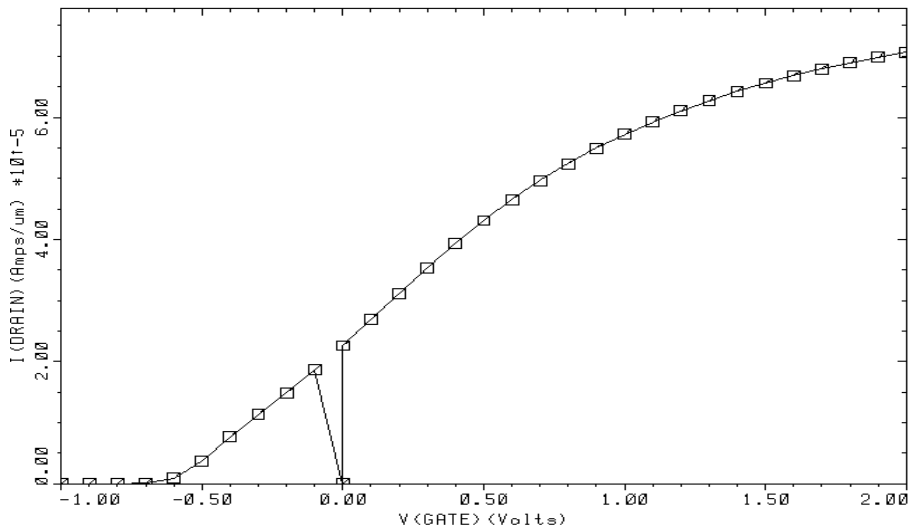


Figure 6.2: Transfer characteristics III-V based HEMT

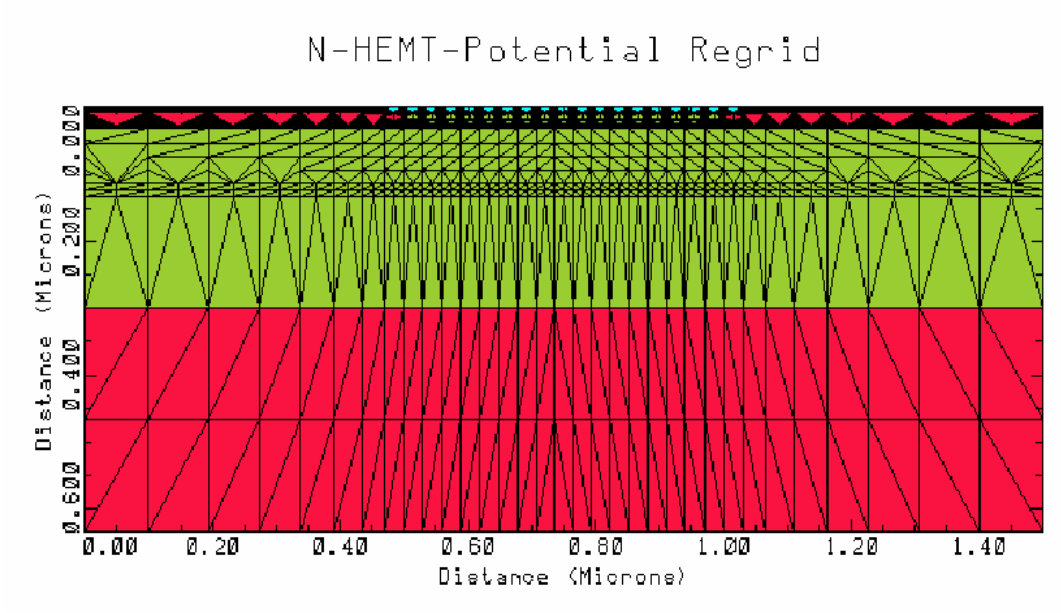


Figure 6.3: Two dimensional device structure of III-V based HEMT from Medici™

6.2 INTRODUCTION TO SENTAURUS™

The comprehensive Sentaurus™ device simulator includes two dimensional and three dimensional simulation that bridges the needs of development and manufacturing engineers by optimizing size of the solid-state devices. It can be used to improve the new technologies and explore a broad range of process and device alternatives, and provides a mechanism to optimize parametric yield in manufacturing [84].

The section provides simulation results and related issues from Sentaurus™ device simulator. The simulation environment is optimized for the heterostructure field-effect transistors (HFETs) in GaN material system. The wide bandgap based

semiconductors, especially III–nitride groups, require some adjustments to ensure accurate simulation results [85]. The spontaneous and piezoelectric polarization effects are considered for the proposed device structure.

Sentaurus^{TM} Structure Editor and Sentaurus^{TM} Workbench are used to simulate the device. The DC characteristics of the transistor are simulated and compared with the experimental results.

The simulated device structure is shown in Figure 6.4 that includes a 25 nm AlGaN barrier and a 2 μm GaN bulk layer grown on SiC substrate. The source–gate and gate–drain separations used are 1.5 μm and 2.4 μm, respectively, and the gate length is set to 1.1 μm. Preliminary results from the Sentaurus^{TM} simulator are shown in this section. Figure 6.4 shows the cross sectional schematic of the GaN based HEMT with carrier profile. The output current voltage characteristic at room temperature is shown in Figure 6.5 at V_{ds} = 10V. Figure 6.6 shows the effect of gate voltage on saturation current. A comparison between the measured and interpolated transfer characteristics is shown in the figures. Good agreement is obtained between analytical calculation, simulation and experimental results. The numerical simulation result from the proposed model has shown higher values of output current compare to that of experimental result. However, the analytical and the numerical simulation results for HEMT devices have suggested that the trap effects and high voltage, in fact dominate the leakage current of the HEMT device.

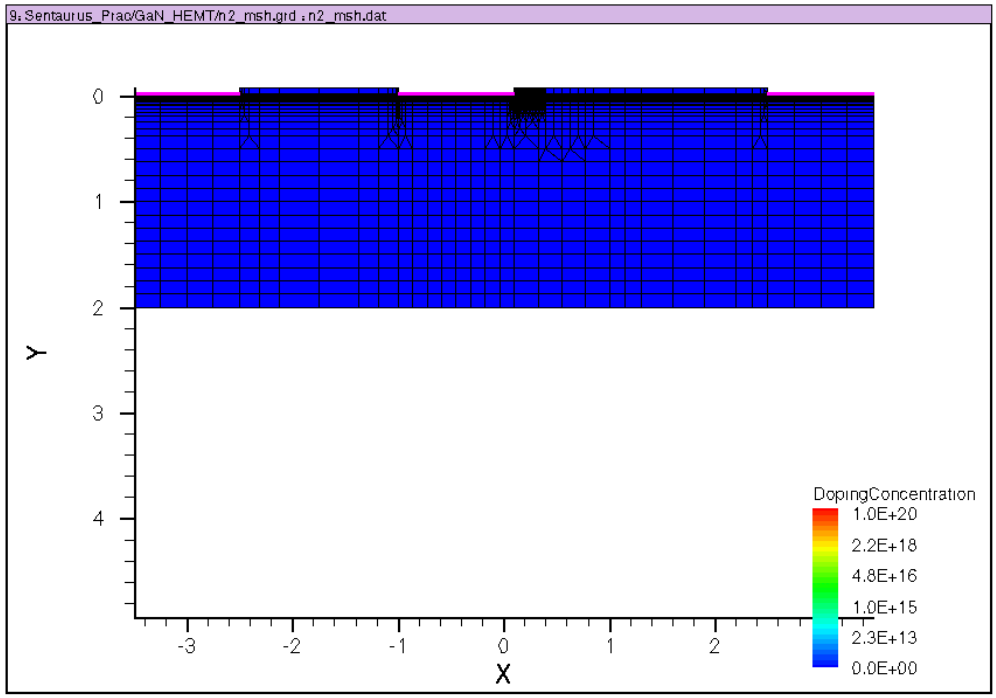


Figure 6.4: The cross sectional schematic of the GaN based HEMT with carrier profile

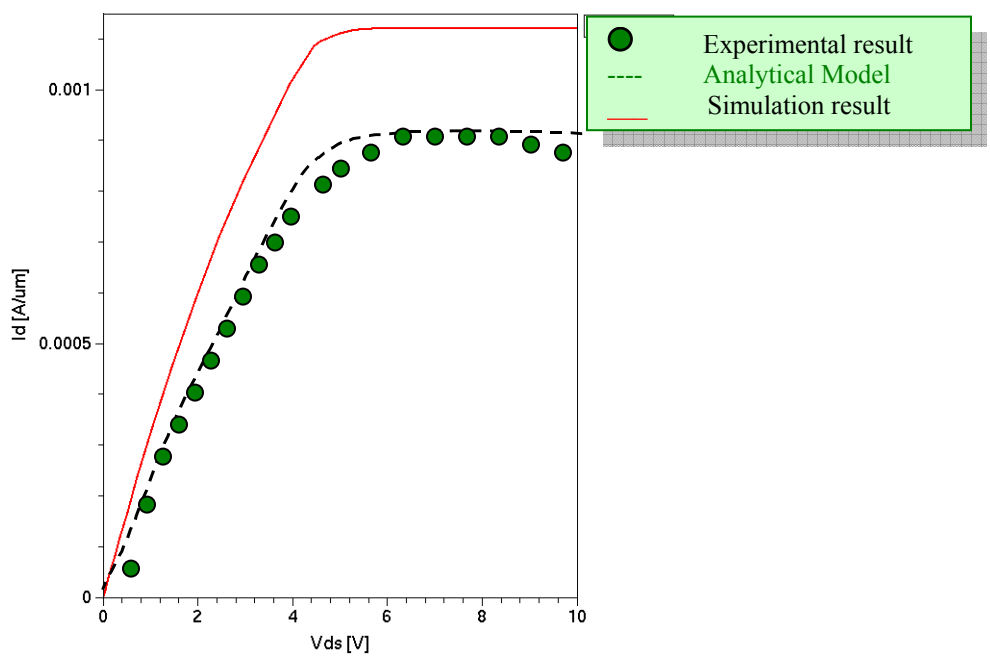


Figure 6.5: Output characteristic of GaN based HEMT from Sentaurus^{TM} simulation

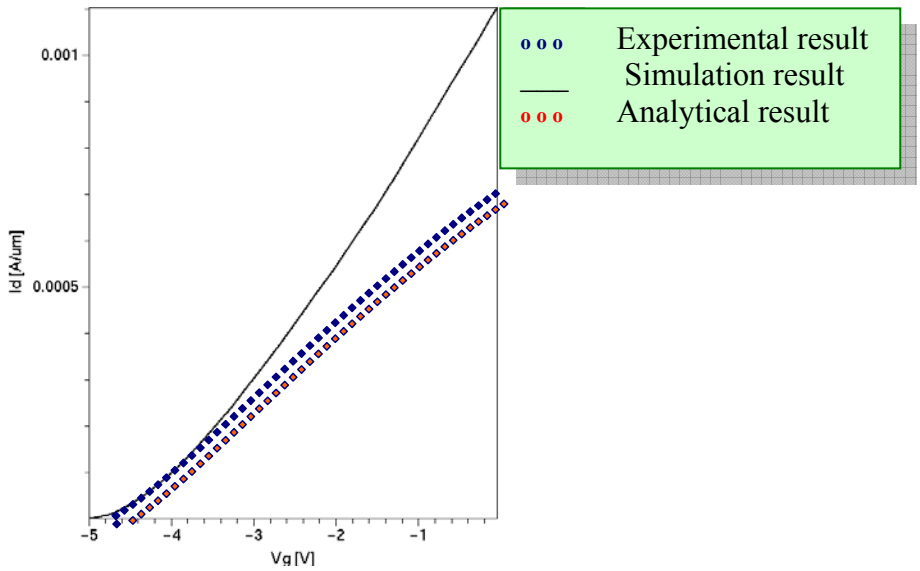


Figure 6.6: Transfer characteristic of GaN based HEMT from Sentaurus^{TM} simulation

The self-heating is a local increase in crystal temperature due to the trap electrons. The data obtained from the experimental results agrees more closely to the analytical simulation data. The numerical simulation shows higher values of output current. The current is suppressed by an amount due to the effect of carrier confinement in the devices. Output characteristics with different types of static interface trap and charge densities are considered in the analytical modeling. But in the numerical simulation the trap effects are not considered. It is mainly responsible for the higher current levels.

CHAPTER 7: CONCLUSIONS

Gallium nitride (GaN) based devices are expected to have a greater impact on high temperature and high-speed electronics. Much work is being done with GaN for RF electronics, and some of these results will help to improve power electronics too. But it seems that GaN devices will not replace Si devices. Most likely it is useful for specialized application at high power, high temperature, high speed applications (radar/satellite) [53]. One of the potential applications of the high frequency RF electronics is in communications industries. Transportation industries are looking for reliable switching devices for high temperature operation [36]. At present the use of silicon-based power devices are largely limited because of the intrinsic material parameters and the internal heat generation of the power switches. Hence, there is a great need for acceptance of the wide bandgap semiconductor in automotive electronics as well as in communications industries [52]. RF and power HEMTs in GaN system are still in a developmental stage; therefore, there is a good opportunity to study, design, fabricate and test a HEMT in GaN. There is always a need for reliable device model to study the device behavior and evaluate its characteristics. A good model can predict the device behavior quite accurately and design requirements can be implemented with low tolerance.

7.1 SUMMARY

In this study, limitations of the wide bandgap material processing and device fabrications are investigated. Three major wide bandgap materials (SiC, GaN and diamond) are studied and material for the commercial GaN based HEMTs fabrication is

assessed. MOS gate HEMT structure is identified, and a new modeling technique is developed. The achievement of the research can be summarized as follows:

Analytical modeling for MOS gate HEMT structure: *(Published Micro Electronics Journal (MEJ),* Volume 37, Issue 7, July 2006, Pages 579-582*)* An investigation of the operation of AlGaN/GaN n type self-aligned MOSFET with modulation doped GaN channels is presented. Liquid phase deposited (LPD) SiO_2 is used as the insulating material. An analytical model based on modified charge control equations is developed. The analysis and simulation results on the transport characteristics of the MOS gate HEMT structure is compared with the previously measured experimental data. The calculated values of f_T *(*20–30 GHz) suggest that the operation of the proposed device effectively has sufficiently high current gain cut-off frequencies over a wide range of drain voltage, which is essential for high-power performance at microwave frequencies.

Temperature model for HEMT: *(Published in International Journal of Infrared and Millimeter Waves (IRMMW) November, 2005.)* An analytical model for the HEMT in GaN has been developed that has taken the temperature effects on the device behavior. The temperature dependent related parameters of the HEMTs are also investigated. The proposed model can operate at higher voltages and shows stable operation at higher temperatures. The investigated temperature range is from 100^0K–600^0K. The simulated results indicate that the device demonstrates significant degradation at elevated temperature. The simulation results match very well with the measured data.

Temperature effect on extended model for HEMT structure: *(published in International Semiconductor Device Research Symposium (ISDRS), Washington DC,*

December 7-9, 2005 and submitted to Journal of Solid State Electronics.) A temperature depended extended model for HEMT structure has also been developed. The channel conductance in the saturation region and the parasitic resistance due to the undoped GaN buffer layer are considered. The investigated critical parameters of the proposed device are the maximum drain current, the threshold voltage, the peak DC transconductance, breakdown voltage and unity current gain cut-off frequency. The simulation results match reasonably with the measured data.

Numerical Simulation of HEMTs: In this research, an analytical model for HEMTs has been developed. The two dimensional device simulation tool Medici^{TM} is used to simulate the III-V material system. The three dimensional device simulator Sentaurus^{TM} is used to simulate the AlGan/GaN HEMTs. Thus, more realistic device structure is formed and more detailed device inside is visualized using the device simulation tools.

Test and characterization of GaN HEMTs: HEMT test devices fabricated in GaN have been tested and characterized at room temperature.

7.2 FUTURE WORK

Numerical Solution: One of the major future works would be the numerical simulation of the devices structure using the device simulator like Sentaurus^{TM} at different temperatures ranging from 100^0K to 600^0K. Thus, clear picture of the charge transport and electric field strength will be available for complete analysis at elevated temperatures. Once the simulation results are satisfactory, the device needs to be fabricated and to be tested and characterized. Several generations of fabrication and

characterization of the test device are required to improve the model and thus establish the model as a universally acceptable one.

Temperature Effect on Quantum Well Calculation: The proposed model equations do not include the effect of temperature on quantum well calculations. A temperature dependent charge control model can be developed taking into account the quantum mechanical distribution of electrons in the channel. Instead of using a constant charge concentration in quantum well, a quantum well model, which includes the variation of the energy levels with temperature, can be used. Better estimation of the shape of the quantum well, electric field distribution, is needed to obtain more accurate results from the analytical model.

Parameter extraction and SPICE model development: HEMT test devices fabricated in GaN can be tested and characterized at different temperature range for high power RF applications. The capacitances measurement as well as the switching characteristics can also be carried out for the test device. The parameters for circuit simulation can be extracted from the experimental data. Thus, a SPICE model for the GaN based HEMTs can be developed.

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APPENDICES

APPENDIX A. MATLAB SIMULATION

```
%find Idsat-Vg
clear all;

    i=0;
    for z=.001:.01:1
        i=i+1;
        Z(i)=z;
        i
        int=0;
        for t=1:-.00001:z
            F=1/(t^2*log(1+t));
            int=int+F*(-.00001);
        end
        Int(i)=int;
        if abs(Int)==inf
            Int(i)=0;
        else
        end
        c3=0;
        for t=1:-.00001:z
            F1=1/(t^3*log(1+t));
            c3=c3+F1*(-.00001);
        end
        C3(i)=c3;
        if abs(C3)==inf
            C3(i)=0;
        else
        end

    end
    n=i;
    %figure(4)

    %semilogy(Z,Int,Z,C3)
%    grid on



    %Parameters

    L=0.7e-4; % HEMT gate Length
    W=30e-4; %Gate width
    dd=300e-8; % Width of the supply layer
    di=40e-8; % Width of the spacer layer
    a=0.125e-12;
    e2=13.95; % Permittivity of SiGe
    e0=8.854e-14;% Permittivity of Free Space
    q=1.6022e-19; % Eelctron Charge
    deld=(a*e2*e0)/q;
```

```
    tox=50e-7; % Oxide Thickness
    eox=3.9; % Permittivity of SiO2

    for vt=2.50:-.02:2.44; % Threshold voltage for different
Temperature

    if vt==2.50 % When T=400K
        mu=150
       vs=4e6;

    elseif vt==2.48 % When T=300K
        mu=500
   vs=4e6;
    elseif vt==2.46 % When T=200K
        mu=1500

     vs=4e6;
    elseif vt==2.44 % When T=100K
        mu=10000
vs=4e6;
    end
    %Capacitance Calculation
    Cox=(eox*e0)/tox;
    Ceq=1/(((dd+di+deld)/(e2*e0))+(1/Cox));

    %Calculate G & k
    G=Ceq*vs*W;


    Rs=12; % Source resistance
    Rd=12; % Drain Resistance
    m=0;

    for Idsat=-1e-5:-5e-5:-1e-2
        m=m+1;
        k=(vs*L*G)/(mu*Idsat);
        for j=1:n;
            dif=abs(k-Int(j));
            Dif(j)=dif;
        end
        [Difm,l]=min(Dif);
        t0s=Z(l);
        Vg(m)=vt+Idsat*Rs+(Idsat/(t0s*G));
        IDsat(m)=abs(Idsat);
        vg=vt+Idsat*Rs+(Idsat/(t0s*G)); % to calculate gm
        gm(m)=Idsat/(vg-vt+((vs/mu)*L*log(1+t0s)));

    end


    figure(5)
    if vt==2.50
        plot(Vg,-IDsat*1e3,'b')
```

```
        Axis([-1.5,2.5,-5,0]);
        xlabel('V_G')
        ylabel('I_D_s_a_t')

        hold on;
    elseif vt==2.48
        plot(Vg,-IDsat*1e3,'r')

        Axis([-1.5,2.5,-5,0]);

    elseif vt==2.46
        plot(Vg,-IDsat*1e3,'g')

        Axis([-1.5,2.5,-5,0]);

    elseif vt==2.44
        plot(Vg,-IDsat*1e3,'k')

        Axis([-1.5,2.5,-5,0]);
        legend('T=400 K','T=300 K','T=200 K','T=100 K')

    end

    figure(6)
    if vt==2.50
        plot(Vg,gm*1e3,'b')
          xlabel('V_G')
        ylabel('g_m_s')


        hold on;
    elseif vt==2.48
        plot(Vg,gm*1e3,'r')


        elseif vt==2.46
        plot(Vg,gm*1e3,'g')

    elseif vt==2.44
        plot(Vg,gm*1e3,'k')

      legend('T=400 K','T=300 K','T=200 K','T=100 K')

    end

end



clear all;

    vt=2.50
        Idsat=-0.4e-3;
        mu=150;
```

```
vs=4e6;
L=0.7e-4;
Z=30e-4;

k=-1*(vs*L)/mu;
dd=300e-8;
di=40e-8;

a=0.125e-12;
e2=13.95;
e0=8.854e-14;
q=1.6022e-19;
deld=(a*e2*e0)/q;
tox=50e-7;
eox=3.9;
%Capacitance
Cox=(eox*e0)/tox;
Ceq=1/(((dd+di+deld)/(e2*e0))+(1/Cox));

G=Ceq*vs*Z;


vg=1.0
Rs=12;
Rd=12;

i = 0;
Ids = 0;
Vds = 0;
Idst=0;
Id=0;
in = -1e-5;
for vd = -1e-3: -.02: -1.2
    i= i + 1;
    Vds(i)=vd;
    i

    dif1=1;
    j=0;
    Iend=-1.5e-2;


   Ip=0;
    for Id = in: -1e-5: Iend

        j=j+1;
        %index=i+j*1000
        IRs = Id*Rs;
        IRd = Id*Rd;
        vend = vd-IRd;

        int = 0;
        for v = IRs: -.0001: vend
```

```
                den = vg-vt-v;
                if den~=0 & Id/(G*(vg-vt-v))~=0

                    F =1/(log(1+(Id/(G*(vg-vt-v)))));
                    int = int + (F * (-.0001));

                else
                end
            end

                dif = abs(int-k);


               if dif < .1
                    if dif1 > dif;
                        I = Id;
                        Ip = Id;
                    else
                        I = Ip;
                    end
                else
                    I = Ip;
                end

                dif1 = dif;

        end

        in = I;
        Ids(i) = I;
        Idst=Ids;


    end
    for j=1:1:60
        i=j;
        if Ids(i)>Idsat
            Ids1(i)=Ids(i);
        else
            Ids1(i)=Idsat;
        end
    end

    IT4=Ids1*1000;

%*************************************************
   vt=2.48
        Idsat=-0.7e-3;
        mu=500;



         vs=4e6;
```

```
L=0.7e-4;
Z=30e-4;
%mu=1000;
k=-1*(vs*L)/mu;
dd=300e-8;
di=40e-8;

a=0.125e-12;
e2=13.95;
e0=8.854e-14;
q=1.6022e-19;
deld=(a*e2*e0)/q;
tox=50e-7;
eox=3.9;
%Capacitance
Cox=(eox*e0)/tox;
Ceq=1/(((dd+di+deld)/(e2*e0))+(1/Cox));

G=Ceq*vs*Z;


vg=1.0
Rs=12;
Rd=12;

i = 0;
Ids = 0;
Vds = 0;
Idst=0;
Id=0;
in = -1e-5;
for vd = -1e-3: -.02: -1.2
    i= i + 1;
    Vds(i)=vd;
    i

    dif1=1;
    j=0;
    Iend=-1.5e-2;


   Ip=0;
    for Id = in: -1e-5: Iend

        j=j+1;
        %index=i+j*1000
        IRs = Id*Rs;
        IRd = Id*Rd;
        vend = vd-IRd;

        int = 0;
        for v = IRs: -.0001: vend

            den = vg-vt-v;
```

```
                if den~=0 & Id/(G*(vg-vt-v))~=0

                    F =1/(log(1+(Id/(G*(vg-vt-v)))));
                    int = int + (F * (-.0001));

                else
                end
            end

                dif = abs(int-k);


               if dif < .1
                    if dif1 > dif;
                        I = Id;
                        Ip = Id;
                    else
                        I = Ip;
                    end
                else
                    I = Ip;
                end

                dif1 = dif;

        end

        in = I;
        Ids(i) = I;
        Idst=Ids;


    end
    for j=1:1:60
        i=j;
        if Ids(i)>Idsat
            Ids1(i)=Ids(i);
        else
            Ids1(i)=Idsat;
        end
    end

    IT3=Ids1*1000;



%****************************************
 vt=2.46
        Idsat=-0.8e-3;
        mu=1500;



         vs=4e6;
```

```
L=0.7e-4;
Z=30e-4;
%mu=1000;
k=-1*(vs*L)/mu;
dd=300e-8;
di=40e-8;

a=0.125e-12;
e2=13.95;
e0=8.854e-14;
q=1.6022e-19;
deld=(a*e2*e0)/q;
tox=50e-7;
eox=3.9;
%Capacitance
Cox=(eox*e0)/tox;
Ceq=1/(((dd+di+deld)/(e2*e0))+(1/Cox));

G=Ceq*vs*Z;


vg=1.0
Rs=12;
Rd=12;

i = 0;
Ids = 0;
Vds = 0;
Idst=0;
Id=0;
in = -1e-5;
for vd = -1e-3: -.02: -1.2
    i= i + 1;
    Vds(i)=vd;
    i

    dif1=1;
    j=0;
    Iend=-1.5e-2;


   Ip=0;
    for Id = in: -1e-5: Iend

        j=j+1;
        %index=i+j*1000
        IRs = Id*Rs;
        IRd = Id*Rd;
        vend = vd-IRd;

        int = 0;
        for v = IRs: -.0001: vend

            den = vg-vt-v;
```

```
                if den~=0 & Id/(G*(vg-vt-v))~=0

                    F =1/(log(1+(Id/(G*(vg-vt-v)))));
                    int = int + (F * (-.0001));

                else
                end
            end

                dif = abs(int-k);


               if dif < .1
                    if dif1 > dif;
                        I = Id;
                        Ip = Id;
                    else
                        I = Ip;
                    end
                else
                    I = Ip;
                end

                dif1 = dif;

        end

        in = I;
        Ids(i) = I;
        Idst=Ids;


    end
    for j=1:1:60
        i=j;
        if Ids(i)>Idsat
            Ids1(i)=Ids(i);
        else
            Ids1(i)=Idsat;
        end
    end

    IT2=Ids1*1000;



    %*************************************************************
vt=2.44
         Idsat=-0.95e-3;
         mu=10000;

         vs=4e6;
    L=0.7e-4;
    Z=30e-4;
```

```
%mu=1000;
k=-1*(vs*L)/mu;
dd=300e-8;
di=40e-8;

a=0.125e-12;
e2=13.95;
e0=8.854e-14;
q=1.6022e-19;
deld=(a*e2*e0)/q;
tox=50e-7;
eox=3.9;
%Capacitance
Cox=(eox*e0)/tox;
Ceq=1/(((dd+di+deld)/(e2*e0))+(1/Cox));

G=Ceq*vs*Z;


vg=1.0
Rs=12;
Rd=12;

i = 0;
Ids = 0;
Vds = 0;
Idst=0;
Id=0;
in = -1e-5;
for vd = -1e-3: -.02: -1.2
    i= i + 1;
    Vds(i)=vd;
    i

    dif1=1;
    j=0;
    Iend=-1.5e-2;


   Ip=0;
    for Id = in: -1e-5: Iend

        j=j+1;
        %index=i+j*1000
        IRs = Id*Rs;
        IRd = Id*Rd;
        vend = vd-IRd;

        int = 0;
        for v = IRs: -.0001: vend

            den = vg-vt-v;
            if den~=0 & Id/(G*(vg-vt-v))~=0
```

```
                    F =1/(log(1+(Id/(G*(vg-vt-v)))));
                    int = int + (F * (-.0001));

                else
                end
            end

                dif = abs(int-k);


               if dif < .1
                    if dif1 > dif;
                        I = Id;
                        Ip = Id;
                    else
                        I = Ip;
                    end
                else
                    I = Ip;
                end

                dif1 = dif;

        end

        in = I;
        Ids(i) = I;
        Idst=Ids;


    end
    for j=1:1:60
        i=j;
        if Ids(i)>Idsat
            Ids1(i)=Ids(i);
        else
            Ids1(i)=Idsat;
        end
    end

    IT1=Ids1*1000;
clear all;
x=.5;
y=.75;
q=1.6e-19;
dd= 250e-8;
di=40e-8;
ds=50e-8;
a=.125e-12;
e0=8.85418e-14;
e2=11.7+4.5*x;
eox=3.9;
esi=11.7;
tox=50e-7;
```

```
deld=(a*e2*e0)/q;
Cox=(eox*e0)/tox;
Ceq= 1/(((dd+di+deld)/(e2*e0))+(ds/(esi*e0))+(1/Cox)) % Total
Equivalent Capcitance
phim = 4.1;
ki3002= 4.05-.05*x;
kisi=4.05; % Electron affinity of Si at 300K
Qox=q*1e11;
N2=5e17;
Nsi=5e8;
del_Ev=0.5*(.84-.53*y);% According to People & Beans Equation

mv=(0.81-0.47*x);

T=300;
k=8.6174e-5;
Eg02=1.17-.896*x+.396*power(x,2);
Eg3002=Eg02-(((4.73e-4)*T^2)/(T+636));
Nv3002=(4.82e15)*((mv)^1.5)*T^1.5

i=0;

for T=100:450
    i=i+1;

Eg02=1.17-.896*x+.396*power(x,2);
Eg2=Eg02-(((4.73e-4)*T^2)/(T+636)); %  Bandgap of SiGe at T degree
Kelvin
Nv2=(4.82e15)*((mv)^1.5)*T^1.5
ki2=ki3002+.5*(Eg3002-Eg2);
del_Ef=-.000112*T+.0336;


Temp(i)=T;
Vth(i)=phim-ki2-Eg2+del_Ev-del_Ef -
(Qox/Cox)+((q*(N2*dd+Nsi*ds))/Cox)+(((q*N2*(dd^2)))/(2*e2*e0))+(((q*Nsi
*(ds^2)))/(2*esi*e0))+(((q*N2*(dd*ds)))/(esi*e0));
VTH=Vth


end
figure(15)
plot(Temp,Vth,'r');
grid on;
```

APPENDIX B. MEDICI™ SIMULATION

```
TITLE GAAS HEMT

MESH
X.M WIDTH=.8 H1=.1 H2=.03
X.M WIDTH=.4 H1=.03 H2=.03
X.M WIDTH=.8 H1=.03 H2=.1
Y.M WIDTH=.4 N.SPACES=3
Y.M WIDTH=2.45 N.SPACES=40
Y.M WIDTH=0.3 N.SPACES=3
Y.M WIDTH=0.7 N.SPACES=2

REGION NAME=BLANK OXIDE
REGION NAME=BODY SILICON Y.MIN=3.15
REGION NAME=SRC SILICON Y.MAX=2.85 X.MAX=.4
REGION NAME=DRN SILICON Y.MAX=2.85 X.MIN=1.6
REGION NAME=NSILI SILICON X.MIN=.4 X.MAX=1.6 Y.MIN=.4 Y.MAX=.9
REGION NAME=GRAD GAAS X.MIN=.4 X.MAX=1.6 Y.MIN=.9 Y.MAX=1.4
X.MOLE=0.0 X.END=.5
REGION NAME=EQ GAAS X.MIN=.4 X.MAX=1.6 Y.MIN=1.4 Y.MAX=2.15
X.MOLE=0.5 X.END=.5
REGION NAME=SPACR GAAS X.MIN=.4 X.MAX=1.6 Y.MIN=2.15 Y.MAX=2.35
X.MOLE=0.4 X.END=.4
REGION NAME=CHANL SILICON Y.MIN=2.35 Y.MAX=2.85
REGION NAME=BFR GAAS Y.MIN=2.85 Y.MAX=3.15  X.MOLE=0.4 X.END=.4

ELECT NAME=SOURCE X.MAX=.4 Y.MAX=.4
ELECT NAME=DRAIN X.MIN=1.6 Y.MAX=.4
ELECT NAME=GATE X.MIN=.8 X.MAX=1.2 Y.MAX=.2
ELECT NAME=SUBST BOTTOM

COMMENT Specify Doping
PROFILE REGION=BODY N.TYPE CONC=1E2 UNIF
PROFILE REGION=CHANL P.TYPE CONC=1E2 UNIF
PROFILE REGION=NSILICONLI N.TYPE CONC=4E17 UNIF
PROFILE REGION=SRC N.TYPE CONC=2E20 UNIF
PROFILE REGION=DRN N.TYPE CONC=2E20 UNIF
PROFILE REGION=SPACR N.TYPE CONC=1E2 UNIF
PROFILE REGION=GRAD N.TYPE CONC=4E18 UNIF
PROFILE REGION=EQ N.TYPE CONC=8E17 UNIF
PROFILE REGION=BFR N.TYPE CONC=1E3 UNIF
```

```
FILL ^NP.COL SET.COL C.SILICON=2 C.GAAS=3

COMMENT Generate plot of device structure
PLOT.2D FILL  GRID
+ TITLE= "DVEX9 HEMT Device Structure"

MODELS CONSRH AUGER ANALYTIC
COMMENT Initial solution
SYMB NEWT CARR=0
SOLVE V(DRAIN)=0.1 V(GATE)=0.2
SYMB NEWT CARR=1
SOLVE
$ Do some plots
$PLOT.1D X.ST=0.5 X.END=0.5 Y.ST=-1 Y.EN=1 DOPING
 $+ LOG TITLE= "Channel Doping & Electrons Device ON"
$PLOT.1D X.ST=0.5 X.END=0.5 Y.ST=-1 Y.EN=1
$+ ELECT LOG UNCH COL=2
$LABEL LABEL=Electrons COL=2 X=0.1 Y=1e11
$LABEL LABEL=Doping X=0.1 Y=1e3

$PLOT.1D X.ST=0.5 X.EN=0.5 Y.ST=-1 Y.EN=1 COND TOP=1 BOT=-2
$+ NEG TITLE= "DVEX9 Band Structure Device ON"
 $PLOT.1D X.ST=0.5 X.EN=0.5 Y.ST=-1 Y.EN=1
 $+ VAL UNCH NEG
 $PLOT.1D X.ST=0.5 X.EN=0.5 Y.ST=-1 Y.EN=1
 $+ QFN UNCH NEG COL=2
 $LABEL LABEL=Cond X=0.1 Y=0.6
 $LABEL LABEL=Qfn X=0.1 Y=0.05
 $LABEL LABEL=Val X=0.1 Y=-1.2
 $PLOT.2D FILL BOUND
 $+ TITLE= "DVEX9 Current Density"
  $PLOT.2D X.PLANE=0.5 fill
  $+ TITLE= "DVEX9 Current, Potential"

  $CONTOUR J.TOTAL MIN=1e-3 FILL
  $CONTOUR POT

  COMMENT Calculate the gate characteristics.
  SOLVE ELEC=GATE VSTEP=0.15 NSTEP=20
  PLOT.1D X.AX=V(GATE) Y.AX=I(DRAIN) POINTS
  + TITLE= "DVEX9 Gate Characterics of HEMT Device"
```

APPENDIX C. SENTAURUS™ SIMULATION

Computation of interface charges

```
!(
set q 1.602e-19
set x @x@
set strainRelax @strainRelax@
# Enforce correct range for strainRelax
if ($strainRelax>1) {set strainRelax 1}
if ($strainRelax<0) {set strainRelax 0}

# Mole fraction dependent spontaneous polarization
set Psp_AlN [expr -8.1e-6/$q]
set Psp_GaN [expr -2.9e-6/$q]
set Psp_AlGaN [expr $x*$Psp_AlN + (1-$x)*$Psp_GaN]
set DPsp [expr $Psp_GaN - $Psp_AlGaN]

# Mole fraction dependent piezoelectric polarization
set e33i [expr ($x*1.46e-4 + (1 - $x)*0.73e-4)/$q]
set e31i [expr ($x*(-0.60e-4) + (1 - $x)*(-0.49e-4))/$q]
set c13i [expr $x*108 + (1 - $x)*103]
set c33i [expr $x*373 + (1 - $x)*405]

set straini [expr (1-$strainRelax)*($x*(3.189 - 3.112)/($x*3.112 + (1-$x)*3.189))]
set Ppz_AlGaN [expr 2*$straini*($e31i - $c13i/$c33i*$e33i)]
set DPpz [expr -$Ppz_AlGaN]
set intCharge [expr $DPsp + $DPpz]

# Reporting
puts "* Spontaneous polarization for AlGaN: [format %1.2e [expr $q*$Psp_AlGaN]]
(C/cm^2)"
puts "* Piezopolarization for AlGaN: [format %1.2e [expr $q*$Ppz_AlGaN]] (C/cm^2)"
puts "*   Total AlGaN Polarization: [format %1.2e [expr $q*($Psp_AlGaN +
$Ppz_AlGaN)]] (C/cm^2)"

puts "\n*   Total GaN Polarization: [format %1.2e [expr $q*$Psp_GaN]] (C/cm^2)"

puts "\n* Int. charge due to spontaneous polarization variation: [format %1.2e [expr
$q*$DPsp]] (C/cm^2)"
puts "* Int. charge due to piezopolarization variation: [format %1.2e [expr $q*$DPpz]]
(C/cm^2)"
puts "*   Total interface charge: [format %1.2e [expr $q*$intCharge]] (C/cm^2)"

)!
```

```
Electrode {
      { Name="gate"   Voltage=0 Schottky  Barrier=1.5}
      { Name="source" Voltage=0 Resist=1 }
      { Name="drain"  Voltage=0 Resist=1 }
}

File {
         * Input files
      Grid    = "@grid@"
      Doping    = "@doping@"
      Parameter = "@parameter@"

         * Output files
      Current = "@plot@"
      Plot    = "@tdrdat@"
      Output  = "@log@"
}

Physics {
         Hydro(eTemp)
      Mobility (DopingDep eHighfieldsaturation(CarrierTempDrive) hHighfieldsaturation
)
      EffectiveIntrinsicDensity (Nobandgapnarrowing)
      Fermi
      Recombination(SRH)
      RecGenHeat
         Aniso(Poisson)
}

Physics (Material="GaN") {
      Traps (
         (Acceptor Level Conc=5e17 EnergyMid=1.0 EnergySigma=0 FromMidBandGap
          eXSection=1e-15 hXSection=1e-15)
      )
}

Physics (Material="AlGaN") {
      Traps (
         (Acceptor Level Conc=5e17 EnergyMid=1.0 EnergySigma=0 FromMidBandGap
          eXSection=1e-15 hXSection=1e-15)
      )
}
```

```
Physics (MaterialInterface="AlGaN/GaN") {
   Charge(Conc=!(puts $intCharge)!)
}

Physics (MaterialInterface="AlGaN/Nitride") {
   Charge(Conc=!(puts [expr $Psp_AlGaN + $Ppz_AlGaN])!)
   Traps (
        (Donor Level Conc=3.5e13 EnergyMid=0.2 FromMidBandGap)
   )
}

Plot {
      Potential Electricfield/Vector
      eDensity hDensity
      eCurrent/Vector hCurrent/Vector
      TotalCurrent/Vector
      SRH Auger Avalanche
      eMobility hMobility
      eQuasiFermi hQuasiFermi
      eGradQuasiFermi hGradQuasiFermi
      eEparallel hEparallel
      eMobility hMobility
      eVelocity hVelocity
      DonorConcentration Acceptorconcentration
      Doping SpaceCharge
      ConductionBand ValenceBand
      BandGap Affinity
      xMoleFraction
      eTemperature hTemperature
      eTrappedCharge hTrappedCharge

         DeepLevels

         PE_Polarization/vector
      PE_Charge
}

Math {
         Extrapolate
      Iterations=16

         Digits=6
      ErrRef(electron) = 1E5
      ErrRef(hole) = 1E5
```

```
        RHSmin=1e-10
        RHSmax=1e30

        CDensityMin=1e-30

        DirectCurrentComputation

        RelTermMinDensity = 1e4
}

Solve {
        Coupled (Iterations=100000 LinesearchDamping=0.001)  {Poisson}
        Coupled (Iterations=100) {Poisson Electron Hole}

        ****************************************************************
        * Zero bias plot
        ****************************************************************
        * Plot(FilePrefix="Zero_Bias")
        ****************************************************************
        # initial gate voltage Vgs=0.0V
        Poisson
        Coupled { Poisson Electron }
        Coupled { Poisson Electron Hole eTemperature }
        Save (FilePrefix="IdVd_vg0")

        # second gate voltage Vgs=-2.0V
        Quasistationary
        (InitialStep=0.1 Maxstep=0.1 MinStep=0.01
        Goal { name="gate" voltage=-2 } )
        { Coupled { Poisson Electron Hole eTemperature } }
        Save(FilePrefix="IdVd_vg1")

        # third gate voltage Vgs=-3.0V
        Quasistationary
        (InitialStep=0.1 Maxstep=0.1 MinStep=0.01
        Goal { name="gate" voltage=-3 } )
        { Coupled { Poisson Electron Hole eTemperature } }
        Save(FilePrefix="IdVd_vg2")

        ****************************************************************
        * IdVd curve with Vg=0 V
        ****************************************************************
        Load(FilePrefix="IdVd_vg0")
        * NewCurrent="IdVd_Vg0_" NewCurrent="IdVd_vg0_"
```

```
Quasistationary (
	InitialStep=1e-3 Minstep=1e-7 MaxStep=0.05 Increment=1.5
	Goal {Name="drain" Voltage=10}
) {
	Coupled {Poisson Electron Hole eTemperature}
}

*****************************************************************
* IdVd curve with Vg=-2 V
*****************************************************************
Load(FilePrefix="IdVd_vg1")
* NewCurrent="IdVd_Vg2_"
NewCurrent="IdVd_vg1_"

Quasistationary (
	InitialStep=1e-3 Minstep=1e-7 MaxStep=0.05 Increment=1.5
	Goal {Name="drain" Voltage=10}
) {
	Coupled {Poisson Electron Hole eTemperature}
}

*****************************************************************
* IdVd curve with Vg=-3 V
*****************************************************************
Load(FilePrefix="IdVd_vg2")
* NewCurrent="IdVd_Vg2_"
NewCurrent="IdVd_vg2_"

Quasistationary (
	InitialStep=1e-3 Minstep=1e-7 MaxStep=0.05 Increment=1.5
	Goal {Name="drain" Voltage=10}
) {
	Coupled {Poisson Electron Hole eTemperature}
}
*****************************************************************
* IdVg curve with Vd=10 V
*****************************************************************
NewCurrent="IdVg_Vd10_"
Quasistationary (
	InitialStep=0.02 Minstep=1e-7 MaxStep=0.05 Increment=1.5
	Goal {Name="gate" Voltage=-5}
) {
	Coupled {Poisson Electron Hole eTemperature}
}}
```

APPENDIX D. DEVICE FABRICATION STEPS

AlGaN/GaN HEMTs can be fabricated in the following steps:

- Growth of the semiconductor epitaxial and insulator layers
- Photolithography for ohmic contacts opening
- Ohmic contacts metallization
- Thermal annealing of ohmic contacts
- Photolithography for device isolation levels
- Reactive ion etching or ion implantations
- Contact or e-beam lithography for gate opening
- Gate metallizatiom
- Substrate thinning and slot via formation
- Back side metallization
- Dicing and packaging

VITA

Hasina F Huq was born in Dhaka, Bangladesh in 1974. Ms. Huq is a Ph.D. candidate in the Department of Electrical and Computer Engineering at the University of Tennessee, Knoxville. She obtained her M.S. degree in Electrical Engineering from the Virginia Polytechnic Institute and State University, Blacksburg in 2002. She had her B.S. degree in Electrical Engineering from the Bangladesh University of Engineering and Technology, in 1999. Ms. Huq was awarded Bangladesh Government Merit Scholarship from 1985 to 1990. She has ten papers published in international conferences and journals. Her research interests include wide bandgap (WBG) semiconductor materials and device technology, electronics, SoC, Biosensor and VLSI design.