

Protection of Grid-Tied and Islanded Systems with High Penetration of Inverter-Based Resources

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ABSTRACT

This dissertation proposes protection solutions to challenges introduced in power systems with high penetration of renewable energy sources. The distinct protection challenges that emerge in both islanded and grid-tied systems are explored.

For islanded systems, the main protection challenge relates to the low-short circuit currents of inverter-based resources (IBRs). As a solution, a novel approach that addresses the root problem is proposed that can increase the short-circuit contribution of a generic voltage source converter. The proposed design allows the inverter to provide sustained short-circuit current to achieve fuse-relay and relay-to-relay coordination. Adaptive relaying for microgrid protection in islanded and grid-tied mode is analyzed. An adaptive relay adjusts the relay curves based on the available generation and the network topology. The model-adaptive relay is validated in hardware and hardware-in-the-loop (HIL) and was deployed at EPB control center microgrid. A power amplifier is designed to interface protective relays with protective relays, which is used to evaluate the model-adaptive relay in the laboratory.

For grid-tied systems, this dissertation explores the impact of voltage dips in wind turbine doubly fed induction generator (DFIG) and photovoltaic (PV) systems while also presenting solutions to improve their low-voltage ride through (LVRT) capabilities. The development of a real-time simulator is validated against a physical DFIG testbed. The DFIG machine model is compared with physical measurements during balanced and unbalanced grid conditions. The validated model is then used to study the DFIG system during symmetrical and asymmetrical voltage sags and to evaluate LVRT strategies. Hardware modifications are applied to significantly increase the reactive power support of PV inverters and demonstrates that increasing the semiconductor's current rating allows the PV inverter to ride through faults while enhancing their reactive power support during voltage sags. Through detailed electrothermal simulations, this design is shown to be capable of injecting three-times the inverter rated current for enough time to comply with established LVRT requirements.

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CHAPTER 1
VSC DESIGN TO ENABLE OVERCURRENT PROTECTION IN MICROGRIDS

Abstract: In microgrids, inverter-based resources (IBRs) control their short-circuit contribution close to their rated current, which is insufficient to reliably protect microgrids using legacy distribution overcurrent protection. Although numerous approaches for microgrid protection have been suggested, to date an economically, commercially available relay that effectively addresses the challenges of microgrid protection has not been developed. As a practical solution, this work addresses the root problem by increasing the short-circuit contribution of a generic voltage-source converter (VSC) to leverage existing legacy protective devices for microgrid protection. Using experimental results and electrothermal simulations, this research contributes to the state of the art by demonstrating that only a few inverter components must be overrated to significantly increase the short-circuit current contribution during faults. The proposed and tested design provides sustained short-circuit current to achieve fuse-relay and relay-to-relay coordination. Additional contributions of this chapter include the development of a novel inverter control that addresses challenges posed by saturable inductors during high-current operation. This chapter demonstrates the feasibility of increasing the short-current from inverters, enabling the utilization of legacy overcurrent protective devices for inverter-based microgrids in islanded mode. Portions of this chapter has been previously published in [8].

This dissertation is organized as follows: Chapter 1 proposes a novel approach that addresses the root problem by increasing the short-circuit contribution of a generic Voltage-Source Converter. Chapter 2 explores adaptive relaying for microgrid protection in islanded and grid-tied mode. Chapter 3 presents a power amplifier designed to interface protective relays with protective relays, which is used to evaluate the model-adaptive relay in the laboratory. Chapter 4 presents the development of a real-time simulator which was validated against a physical DFIG testbed. Chapter 5 applies hardware modifications to significantly increase the reactive power support of PV inverters. This chapter demonstrates that increasing the semiconductor's current rating allows the PV inverter to ride through faults while enhancing their reactive power support during voltage sags.

1.1. Introduction

Microgrids have been identified as a critical component of the energy grid of the future. In the past years, microgrid deployments have increased significantly both in the US and worldwide [1,3]. A microgrid is defined as a coordinated group of distributed energy resources (DER) that service a set of loads through a distribution system with the capability to operate grid-connected or islanded operation. Microgrids promote the use of renewable energy sources such as solar and wind power, and offer benefits such as continuous power, improved power quality, and increased reliability [1]. A distribution system that adopts microgrids brings generation closer to the load, allowing customers to maintain power supply in the event of grid faults. However, microgrid resilience can be compromised if they are not properly protected in the event of faults within their own boundaries [1,2].

Although microgrids are commissioned at the distribution level, available distribution protection devices, such as reclosers, relays, and fuses, are not suitable for microgrid protection because they depend on the magnitude of the fault current [1]. Although numerous approaches for microgrid protection have been suggested [1, 2], this research has not led to the development of an economically viable, commercially available relay that effectively addresses the challenges of microgrid protection [1]. Many authors conclude that the main protection challenge for microgrids arises from the limited short circuit current of inverter-based resources (IBRs) [1, 2, 4, 7]. This research addresses the root problem by increasing the short-circuit contribution of the inverter. Although the approach of increasing the fault contribution of IBRs has been proposed before as a solution to the microgrid protection challenges, current approaches are cost-prohibitive because they operate on the assumption that the whole inverter unit must be overrated [5, 7, 25-27, 43]. Using experimental results and electrothermal simulations, this research contributes to the state of the art by demonstrating that only a few inverter components must be overrated to significantly increase high-short-circuit current contribution during faults. Additional contributions of this chapter include the small-signal model of a three-phase voltage source inverter (VSI) considering the inductor saturation, as well as the development of a novel

inverter control that addresses the challenges posed by saturable inductors during high-current operation.

This chapter presents experimental results demonstrating that overrating the current rating of the semiconductor as well as the current sensor (CT), while keeping all other components at their rated power, is sufficient to increase the short-circuit contribution of the three-phase inverter. The presented modifications allow an inverter prototype with components designed for 1.0 p.u. of nominal current to provide more than 3.0 p.u. of fault current for enough time to enable the use of legacy overcurrent protection devices. The power module is oversized to maintain safe operation temperatures during the faulted condition. Other modifications include the current transducer because it is necessary to measure higher currents that maintain closed-loop control during faults. This approach is much more cost-effective compared to oversizing the entire unit or installing differential protection [1,2,6,8], making it more likely to be adopted at scale.

This work shows that overrating the grid filter to accommodate the overloading condition is not necessary because the fault duration is relatively short. However, at currents that exceed the rated current, the core of the inductive grid filter saturates. This saturation introduces nonlinearities that must be accounted for in the vector control to maintain stable operation. This chapter presents a control method considering saturable inductors for maintaining closed-loop stability during normal operation as well as fault conditions.

The proposed modifications for increasing fault contribution of inverters bring several advantages: 1) it enables the use of legacy distribution protective devices such as fuses, breakers, and reclosers; 2) it enables fuse-relay coordination and coordination between primary and backup relays; 3) it is cost-effective, as only a few components need to be overrated while the rest of the inverter components remain at their normally rated power; 4) it does not require a dedicated or additional unit, as the energy storage inverter (ESI) or photovoltaic (PV) inverter can be modified to provide higher fault current. Moreover, an inverter with an overrated current rating device presents lower losses and lower thermal requirements during normal operating conditions, which increases the efficiency of the inverter and reduces its cooling requirements.

1.2. Literature Review

Despite the numerous advantages of microgrids, there are several technical challenges related to their protection [1,2,4]. There is a consensus in the literature that one of the main challenges for protecting microgrids arises from the significant variation in fault current, which drastically changes between operating mode of the microgrid. In grid-connected mode, fault currents are very high due to the utility grid's contribution, while fault currents have significantly lower magnitudes when the microgrid operates in islanded mode [4,5,8]. For instance, during grid-tied operation, the short circuit current ratio is between 10-50 p.u. During islanded operation, the available short-circuit current can be as low as 1.2 p.u. [4-7]. Such a large difference makes coordination of existing distribution protection difficult and often unattainable [7]. Fuses are particularly affected because of their inverse characteristics; in some cases, fuses protecting the lateral feeders will not melt during faults that occur in islanded operation [1]. Furthermore, the latest revision of the IEEE 1547 standard allows PV inverters to immediately disconnect when the grid voltage is under the 50% threshold, which introduces additional challenges for microgrid protection in islanded mode [12].

Table 1.1-1.2 present a comparison of the advantages and disadvantages of conventional methods, and Table 1.3 of non-conventional methods applied to microgrid protection. In summary, adaptive protection and differential protection are two promising approaches for protecting inverter-based microgrids. However, both approaches introduce different challenges. Adaptive protection typically requires a central unit that updates the settings of overcurrent relays for correct tripping based on current system conditions. While this approach has the potential to be used in future microgrids, it requires the construction of an extensive and robust communication network. This can be a significant challenge, especially in islanded microgrids where the communication infrastructure can be compromised [31,33]. Differential protection is the most effective commercially available solution to overcome the challenges of protecting microgrids during islanded operation. This method is practically unaffected by both the small fault current from inverter-based resources (IBRs) and the variable fault current from grid-tied to islanded operation. However, line differential protection is a very expensive solution because it requires a relay

to be installed at every node of a protection zone, which may be unfeasible due to the high number of nodes in a microgrid.

Additionally, it requires high bandwidth communication and cannot be linked through high latency communication technologies. Lastly, line current differential relays are typically equipped with backup relays, such as directional overcurrent relays, which suffer the drawback of being insensitive to low fault currents [1,4]. Negative sequence protection uses negative sequence elements to detect and clear asymmetrical grid faults. However, this approach is challenging in real applications because it requires accurate measurement of negative sequence currents. Commercial IBRs are typically controlled to maximize positive sequence currents and minimize negative sequence currents [13,29]. Furthermore, microgrids serve single-phase loads and include single-phase generation, therefore, applying this protection method is challenging as the negative sequence varies throughout the day.

An admittance relay has been proposed for microgrid protection in both modes of operation [14]. However, coordinating these relays can be difficult in microgrids with a relatively small distribution line. This limitation may be exacerbated in the case of high-impedance faults. Other methods include voltage protection [15]; however, this approach relies on communication links.

Recently, a wavelet transformation method was proposed [16]. The drawback of this method is that when applied in a radial distribution system, coordination between upstream and downstream protection can be challenging because the relays sense the same fault current. Traveling wave approaches have been proposed [23, 24]; however, these methods require high sampling frequency and may not be applicable for microgrids with short distribution lines. There have been proposals to increase the fault contribution in microgrids through the installation of a dedicated fault current source or the oversizing of certain units such as flywheels [25,26] or supercapacitors [27].

Table 0.1
Microgrid protection conventional approach

Method	Advantages	Disadvantages	References
Overcurrent	• Widely used, low-cost and simple. • Enables relay-fuse, relay-relay coordination. • Does not require communication.	• Insensitive to low fault currents from IBRs. • Fault current may depend on the intermittent generation. • Large variability between grid-tied and islanded operation. • Coordination is very difficult or unattainable.	[1][2][6][27]
Differential	• Unaffected by low fault current levels from IBRs.	• Very expensive: should be installed at every node of a protection zone, otherwise the line current differential protection incorrectly trips during normal operation. • Requires high bandwidth communications. • Requires overcurrent backup protection in the event of communication failure. • Errors and mismatches between the current transformers are a challenge.	[1][11][5][19]
Impedance	• Unaffected by the small fault current of inverter-based generation. • Unaffected by variable short-circuit capacities (islanded/grid-tied).	• Measured impedance can be adversely impacted by the fault behavior of IBRs units. • Impedance calculation challenging because lines in microgrids are usually small. • Challenges when detecting high-impedance faults.	[1,14]
Negative Sequence	• Independent of load angle and fault resistance. • Reliable option for detecting unbalanced faults in microgrid with synchronous generators.	• Commercial IBRs are typically controlled to maximize positive sequence current and minimize negative sequence currents. • Negative sequence in the current is negligible for unbalanced faults on PV based generation. • Negative sequence current resulting from load unbalance can be significant in microgrids.	[18][13][39]

Table 0.2
Microgrid protection conventional approach

Directional Overcurrent	Allows coordination of protective devices for different microgrid paths.	• Low fault current is a main adverse effect on overcurrent relay sensitivity. • Requires forward and reverse coordination. • Adaptive settings may be required for microgrid applications.	[28][30]
Frequency	• Does not depend on magnitude and direction of fault current.	• Challenging in low inertia systems to differentiate severe load transients from fault conditions because inrush currents can produce voltage and frequency drops. • Does not allow coordination	[7][31]
Undervoltage	• Does not depend on magnitude and direction of fault current.	• Does not allow coordination. • Insufficient to detect where the fault is located. • The method is vulnerable during transient high resistance fault and difficult in coordination for low voltage dip.	[15,28-29]

Table 0.3
Microgrid protection non-conventional approach

Method	Advantages	Disadvantages	References
Adaptive Relaying (Centralized)	• Allows for adjustment of protection settings based on system conditions.	• Centralized Adaptive Relaying requires extensive and robust communication network. • Currently, modern digital relays limit the settings groups to less than 10, which hinders the range of adaptability.	[10][31][32]
Adaptive Relaying (Communication-less)	• Adjustments of protection settings relaying on local information without communication.	• Difficult to accurately detect and locate faults within the microgrid. • Limited coordination: Communication-less adaptive relaying relies on the individual devices to make decisions about how to respond to changes in the power system. This can lead to suboptimal coordination between devices,	[9][33]
Travelling wave	• Unaffected by the small fault current of inverter-based generation.	• High sampling frequency (at least 256kHz) and may not be applicable for microgrids with short distribution lines • Challenging implementation in small microgrids with low line impedances	[23][24]
AI-Based	• Relies on fault signatures to detect to distinguish faults.	• Requires large datasets for training purposes which are typically unavailable and may be affected by bias or errors in data	[17,20,21,22,44]

Although this approach would enable the adoption of traditional overcurrent protection, it is cost prohibitive. Other suggested methods are based on advance signal processing and artificial intelligence (AI) [21,22,44]. These schemes extract information about the fault signatures to train an AI-based scheme to distinguish and identify the fault. However, these methods have the drawback of requiring large datasets for training purposes which are typically unavailable and may be affected by bias or data errors. Newer approaches propose modifying the control loops of the inverter to inject pre-defined harmonics into the microgrid during the fault condition [19]. Although this method can assist the protection devices to identify and detect the fault in the feeder, it does not solve the challenge of the fuses, which are the first line of defense to protect the laterals against short circuits.

The literature shows that most of the proposed protection methods passively tackle the negative effects caused by the low-fault contribution of IBRs. However, there have been no studies that propose IBR modifications to enhance the short-circuit capabilities. The proposed modifications can be implemented in an ESI or PV inverters, which makes it different from solutions previously proposed which require a dedicated unit to provide high current during faults. This research presents inverter modifications to increase short-circuit current capabilities with the objective of enabling legacy overcurrent protection for inverter-based microgrids.

1.3. Commercial Protection Schemes Applied to Microgrids

Table 1.4 summarizes the protection schemes used in multiple real-world microgrid projects in North America. Traditional overprotection methods are used for protecting real-world microgrids because of their advantages, including low-cost and complexity and coordination between fuses and relays and backup relays. This type of protection is effective to protect the microgrid when it operates in grid-tied mode. Overcurrent protection is found in commercial microgrids such as the EPB control center in Chattanooga, CERTS microgrid, and Santa Rita Microgrid. Because this type of protection is not effective during islanded operation, CERTS and Santa Rita Jail microgrids treat faults during islanded operation as second contingencies leading to the shutdown of the entire microgrid [24].

Differential overcurrent can be found in the following microgrids: the Illinois Institute of Technology (IIT) microgrid–USA and British Columbia Institute of Technology (BCIT) microgrid–Canada. The IIT microgrid implements a comprehensive hierarchical protection scheme, which is described in detail in [52]. This microgrid has online differential relays coordinated in four levels, as shown in Fig. 1.1. The first level (green boxes) protects faults at the load laterals. The second level clears faults impacting the line section between the laterals (blue boxes). A feeder protection provides backup protection for the first and second level in case of communication failures (purple boxes). Overcurrent relay protection is utilized in coordination to provide backup for the other three levels. Adaptive protection is utilized to account for the variability in the short circuit current (purple boxes). The last protection is responsible for protecting the microgrid against external (red boxes) faults and acts as a backup protection for the other three levels. This last level includes overcurrent (50), overvoltage (57), undervoltage (27) and frequency (87) protection elements. This protection scheme sheds light into the complexity and associated cost of protecting microgrids using line differential protection. As a reference, the cost of differential protection for the same manufacturer is more than double that for a high-end directional overcurrent relay that includes communication-assisted tripping [1].

1.4. Fault Contribution from Commercial IBRs

Table 1.5 summarizes the fault characteristics for photovoltaic inverters (PV) and Energy Storage Inverters (ESI). These results were obtained from the few published works on the subject [47-51]. ESI provide a fault contribution that ranges from 1.0 p.u. to 1.8 p.u. ESI inverters produce negative and zero sequence; however, the availability of zero sequence depends on the interfacing transformer type. PV inverters provide a very limited fault current that typically ranges from 1.0 p.u to 1.15 p.u. PV inverters do not provide zero or negative sequence currents although the lack of short circuit current from inverter-based generation is the main concern for microgrid protection in island mode. The lack of negative sequence and zero sequence from grid following inverters may negatively impact the protection of asymmetrical faults, such as line to ground (LG) and line to Line (LL). Table 1.6 and Table 1.7, present the short-circuit contribution from leading commercially available energy storage and PV inverters. These tables shows that the fault contribution

of the commercial battery storage depend on the inverter manufacturer and ranges between 1.0 and 1.8 p.u. PV inverters limit their current to less than 1.0 p.u.

1.5. Summary Literature Review

Microgrids have been identified as a critical component for improving power reliability, increasing energy system efficiency, and enabling higher integration of renewable energy sources. However, this resilience may be lost if the microgrid is not properly protected during short-circuit faults that occur within its own boundaries. The consensus in the literature is that the limited short-circuit current contribution from inverter-based generation causes many of the challenges when protecting microgrids in islanded operation. Commercial inverter manufacturers typically control their fault current contribution to close to the nominal load current, which hinders the application of reliable and cost-effective overcurrent protection for inverter-based microgrids. Fuses are particularly affected because of their inverse characteristics; in some cases, fuses protecting the laterals will not melt for faults during islanded operation.

Line differential protection is the most effective way to protect microgrids in both islanded and grid-tied operation. However, line differential protection is a very cost-prohibitive solution because it requires a high bandwidth communication as well as relay installation at every node of a protection zone, which may be unfeasible due to the high number of nodes in a microgrid. Lastly, line current differential relays are typically equipped with backup relays, such as directional overcurrent relays, which suffer the drawback of being insensitive to low fault currents. Adaptive protection has been widely explored in the literature as a promising technique that enables the use of overcurrent relays in microgrids. Adaptive protection is an online process which modifies the preferred protective responses and correlates them to a change in system conditions. However, adaptive protection requires the construction of an extensive and robust communication network. Furthermore, relay manufacturers limit the adaptability range to the settings groups available in the device, which is typically seven.

Table 0.4
Microgrid protection used in the US

Project name/location	Voltage	Generation mix	Protection features
EPB Control Center/Chattanooga TN	12.47 kV	PV: 1.3 MW ESI: 1.0 MW (1 MWh)	Overcurrent elements (52) 30T, 50T, 100T (Fast acting fuses)
Duke Energy Mount Holly MG/ Mount Holly NC	12.47 kV	PV: 50 kW ESI: 240 kW (500kWh)	Undervoltage (27), overvoltage (59), frequency (81), directional overcurrent (67).
University of California Microgrid, San Diego (CA)—USA		PV: 3 MW Fuel cell: 3 MW Gas turbines: 2 x 13.5 MW Steam turbine: 3 MW	Line current differential (87), impedance (21), directional overcurrent (67)
Consortium for Electric Reliability Technology Solutions Microgrid, Columbus (OH)—USA	0.48 kV	Inverter-Based Natural Gas Turbine: 60 kW	symmetrical component-based scheme overvoltage (59), undervoltage (27), frequency (81), and directional overcurrent (67).
Santa Rita Jail Microgrid, Dublin (CA)—USA	0.48 kV	PV: 1.5 MW Wind: 5 × 2.3 kW Wind ESI: 2.0 MW (4.0 MWh) Fuel Cell: 1.0 MW Diesel Generators: 2 MW	directional overcurrent (67) Overcurrent for grid-connected undervoltage (27) overvoltage (59) frequency (81).
Borrego springs MG, US	25 kV	PV: 700 kW ESI: 500 kW (1500 kWh) Diesel Generator: 1.8 MW	Voltage-restrained protection scheme
British Columbia Institute of Technology (BCIT), Canada	12.47 kV	PV: 300 kW Wind: 2x5 kW ESI: 550 kWh Steam Turbine: 250 kW	Line current differential (87)
Oncor and Irvine Smart Grid, US	12.47 kV	PV: 3.7 MW ESI: 2MW (500 kWh) Natural Gas: 13.5 MW Steam Turbine: 5.6 MW	Adaptive overcurrent protection Communication-assisted digital relays with adaptive settings
Illinois Institute of Technology (IIT)—USA	4.16 kV	PV: 300 kW Wind: 8 kW ESI: 500 kWh Diesel generator: 8 MW Gas Turbine: 4 MW	Line current differential (87) for feeders and laterals

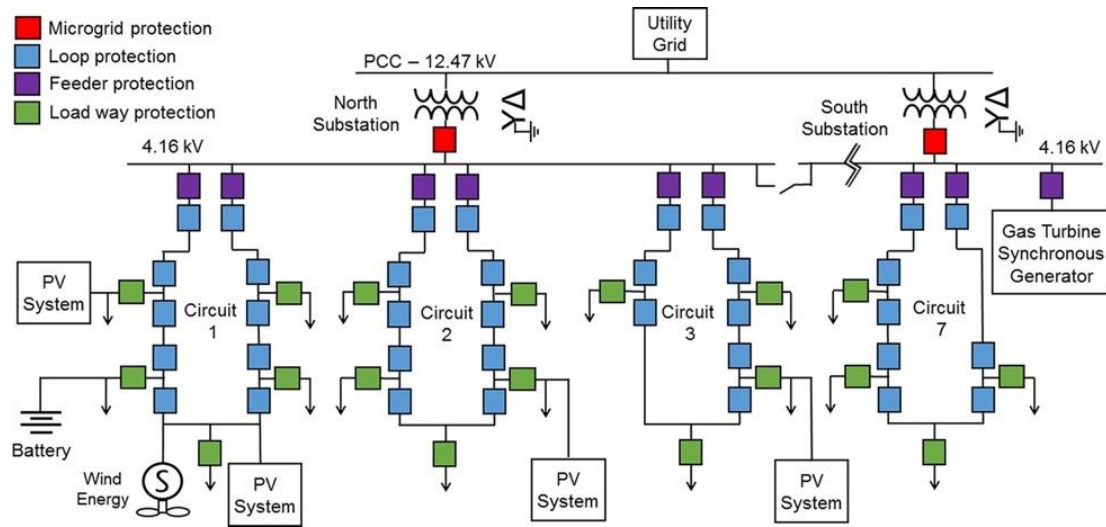


Figure 0.1: Illinois Institute of Technology (IIT)–USA protection using hierarchical protection-based line differential relays [52].

Table 0.5
Fault contribution and sequences of ESI and PV inverters [47-51]

Inverter Type	Rating (kVA)	Phases	Voltage (V)	Transformer	Negative sequence	Zero sequence
ESI	9	three	208	no	yes	yes
ESI	100	three	480	delta to wye	yes	no on wye side
ESI	5.5	single	208	no		
ESI	5	single	240	no		
ESI	5	single	240	no		
PV	24	three	480	no	no	no
PV	24	three	480	no	no	no
PV	3.2	single	208	no	no	no

Table 0.6
Fault contribution from commercial ESI inverters

Brand	Model	Power (kW)	Voltage (V)	Nominal Current (A)	Fault Current (A)	Ratio
Oztek	OZpcs-RS40	40	480	50	63	1.3
Dynapower	Micro Power System	125	480	150	213	1.4
SMA	Sunny Boy Storage 2.5	2.5	280	10.5	19	1.8
Firmer	React2-uno-5.0-tl	5.0	280	22	22	1.0

Table 0.7
Fault contribution from commercial PV inverters

Brand	Model	Power Rating (kW)	Voltage rating (V)	Nominal Current (A)	Fault Current (A)	Ratio of Fault to Nominal
ABB	PRO-33.0-TL-OUTD	33	480	50.3	50.3	1
ABB	TRIO-27.6-TL-OUTD	28	480	45	46	1.02
FIMER	PVS-60-TL	62	480	80	92	1.15
SMA	STP 30000TL-US-10	30	480	36.2	36.2	1.00
SMA	STP 50-US-40	50	480	60.2	64	1.06
SMA	STP 12000TL-20	12	280	17.4	17.4	1.00

The available literature shows that most of the protection methods proposed passively tackle the negative effects caused by the low-fault contribution of IBRs. However, there has been no studies that propose modifications to the IBR at hardware and control levels to enhance its short-circuit capabilities. The following sections explore the inverter modifications to increase its short-circuit current capabilities with the objective of enabling legacy overcurrent protection for inverter-based microgrids.

1.6. VSC Design with Increased Short-Circuit Current System Description and Methodology

Fig. 1.2 shows the proposed inverter with increased short-circuit current contribution; this diagram includes the hardware and control contributions of this chapter. The proposed inverter design consists of a classic two-level voltage-source inverter (VSI) connected to the grid through an inductive filter. This is a typical topology found in PV and ESS inverters. The inverter's semiconductor is overrated to accommodate the overloaded current condition maintaining the junction temperature below the maximum values specified by the manufacturer. The other inverter components, such as the filter, and dc-link capacitors were not changed and remained at their nominal current rating. In this study, it is assumed that a stiff dc-source is established in the dc-side of the inverter, consequently, the dynamics from the dc input is not studied in this work. The inverter is vector controlled as a grid forming device with a classical cascaded control with an inner current control loop and an external voltage loop.

This figure also includes the control contributions of this work, which consist of the decoupling terms for the dq channels considering the non-linear characteristic of the saturable inductors, and the proposed control that recalculates the controller gains considering the inductor saturation. This approach utilizes a fit function to estimate the remaining inductance based on the operating current, and the Butterworth polynomial to optimize the closed loop eigenvalue locations.

Fig. 1.3 shows the time current curves (TCC) for the primary relay, backup relay, and fuses. To evaluate protection coordination using the overcurrent principle, fuses at the end of the circuit and two SEL 651 reclosers are used for primary and backup protection. The fuses' current ratings are 25% greater the nominal load current which is typical practice in protection design. A three-phase circuit breaker applies the faults at the end of the lines, this circuit breaker closes to apply symmetrical and asymmetrical faults and receives the trip signals from the SELS 651 R.

1.7. Electrothermal Modelling

This section develops an electrothermal model to estimate the temperature response of the normally rated device and the overrated device. This model will be used in later sections to study the dynamic response of the junction temperature of the rated device and overrated device during high current operation (during a short circuit) to guarantee that the junction temperature remains under the safety limits; for silicon that temperature is typically 150 °C.

The power losses can be divided into conduction and switching losses of the IGBTs and their associated anti-parallel diodes. Switching losses happen during the turn ON and turn OFF transients and are proportional to the switching frequency $1/T_o$, the collector current i , and blocking voltage V_{dc} [34, 35].

The conduction loss can be calculated with the saturation voltage drop V_{CE} and the collector current i , multiplied by the instantaneous duty ratio τ . For this study τ corresponds to sinusoidal PWM (SPWM). The set of equations to calculate the inverter losses are presented in Table 1.8.

Fig. 1.4 presents the information for both the normally rated (current) semiconductor die with one with overrated current rating used in this study. As shown, the following parameters are sensitive to the collector current: V_{CE} , V_T , E_{on} , E_{off} . During high current operation, the increased collector current influences these parameters, which rapidly increases the conduction and switching losses, which further increases the junction temperature.

A quick inspection shows that the overrated module has lower V_{CE} compared to the normally rated device, which translates to lower conduction losses, which are dominant at high currents. The thermal impedances of the rated and overrated devices are shown in Fig. 1.5. These figures show that for the same package, the device with overrated current has superior electrical and thermal characteristics.

Equation (3.1) shows the fit equation for approximating thermal impedance. The resulting thermal impedance for the IGBTs and diodes are presented in (1.1-1.5). The curve fitting was done by minimizing the root mean square error. The accumulative percentage error is 2.2% for the 30 A device and 1.1% for the 10 A device. Fig. 1.6 shows the Foster thermal network used to model the thermal circuit for the IGBT and diode. A four-layer model was chosen because it provides a better dynamic response compared to a single layer network [35].

$$Z_{jc(t)} = \sum_{i=1}^4 \gamma_i \left(1 - e^{(-t/R_{thi}C_{thi})} \right) \quad (1.1)$$

$$Z_{th_IGBT(10A)} = 1.943 \left(1 - e^{-\frac{t}{(0.051)}} \right) + 0.096 \left(1 - e^{-\frac{t}{(0.00067)}} \right) + 0.329 \left(1 - e^{-\frac{t}{0.002}} \right) + 1.431 \left(1 - e^{-\frac{t}{(0.755)}} \right) \quad (1.2)$$

$$Z_{th_diode(10A)} = 2.813 \left(1 - e^{-\frac{t}{(0.051)}} \right) + 0.14 \left(1 - e^{-\frac{t}{(0.00067)}} \right) + 0.476 \left(1 - e^{-\frac{t}{0.002}} \right) + 2.071 \left(1 - e^{-\frac{t}{(0.755)}} \right) \quad (1.3)$$

The thermal impedance for the overrated IGBTs and diodes are presented in (1.4-1.5).

$$Z_{th_IGBT(30A)} = 0.005 \left(1 - e^{-\frac{t}{(0.056)}} \right) + 0.150 \left(1 - e^{-\frac{t}{(0.004)}} \right) + 0.435 \left(1 - e^{-\frac{t}{(0.763)}} \right) + 0.593 \left(1 - e^{-\frac{t}{(0.0563)}} \right) \quad (1.4)$$

$$Z_{th_diode(30A)} = 1.136 \left(1 - e^{-\frac{t}{(0.057)}} \right) + 0.005 \left(1 - e^{-\frac{t}{(0.0046)}} \right) + 0.842 \left(1 - e^{-\frac{t}{(0.774)}} \right) + 0.318 \left(1 - e^{-\frac{t}{(0.005)}} \right) \quad (1.5)$$

Fig. 1.7 shows an important comparative graph that depicts the power losses in p.u. using the developed electrothermal model; these results were validated using the manufacturer's electrothermal simulators [36],[37]. The normally rated device for the prototype inverter used in this study has ratings of 10 A, 600 V, and the overrated device has ratings of 30 A, 600 V which corresponds to three times the rated current of the inverter. These devices are easily interchangeable as they come in the same 25-pin SDIP. To demonstrate the scalability of the proposed method, the same figure shows a similar comparison with devices used in a larger inverter. For the full-scale inverter, the rated device is a 50A, 1200V device and the overrated device is a 150A, 1200V device. Similarly, both devices use the same Econo3 package. As shown, for both the prototype and full-scale semiconductors, overrating the current rating is a required for high current operation as devices with higher current rating have lower switching and conduction losses, which combined with their better thermal impedance, result in lower junction temperatures for the diode and IGBT. During normal operation, the device with overrated current rating also presents lower losses and lower temperature in the junction, which improves the efficiency of the inverter and reducing its cooling requirements.

1.8. Vector Control Considering Saturable Inductors

The previous section presented simulation results that indicate that replacing the semiconductor allows the inverter to provide sufficient current to enable utilization of fuses in islanded microgrid operation allows coordination with overcurrent relays. However, at currents higher than the rated currents, the core of the inductive grid filter saturates, which introduces nonlinearities that must be accounted for in the vector control for stable operation. This section shows that the employment of conventional vector control in the inverter with saturable inductors brings serious issues regarding the current control performance. This is because traditional vector controllers are developed considering linear and constant inductance. However, in systems with saturable inductors, the inductances are asymmetrical and nonlinear [46]. Neglecting the inductor saturation at high-current operation can make the closed-loop unstable [38].

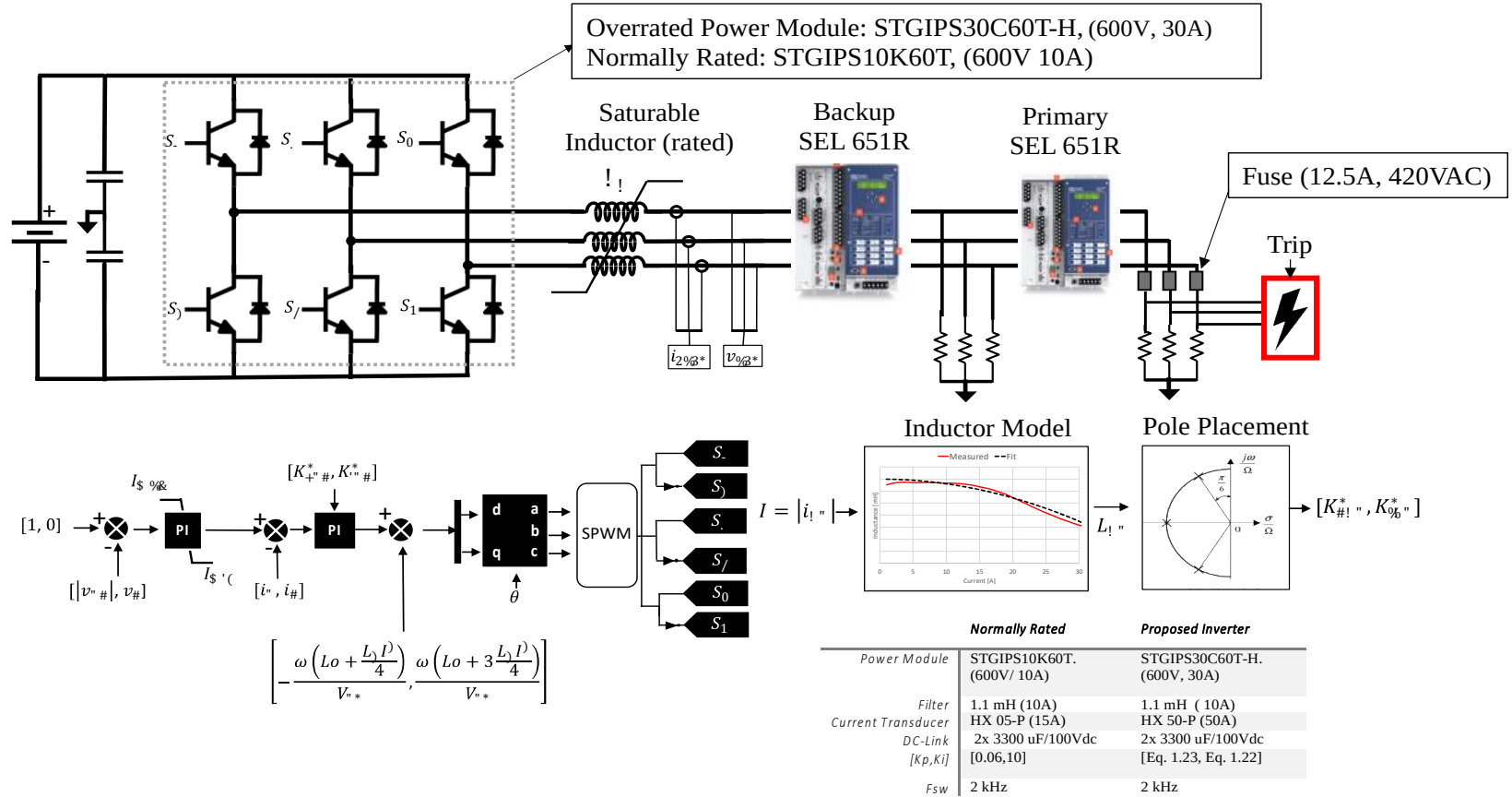


Figure 0.2: Experimental setup for evaluating ac faults in three-phase inverters. Rated device (STGIPS10K60T, 600V/ 10A). Overrated device (STGIPS30C60T-H, 600V, 30A). 1.1mH-10A Inductive grid filter.

Table 0.8
Power losses equations for diodes and IGBTs

	SWITCHING	CONDUCTION
IGBT	$\frac{1}{T_o} \sum (E_{on} + E_{off}) \frac{i}{I_{nom}} \frac{V_{dc}}{V_{nom}}$	$V_{CE}(T_{IGBT}, i) i \tau(t)$
DIODE	$\frac{1}{T_o} \sum (E_{rec}) \frac{i}{I_{nom}} \frac{V_{dc}}{V_{nom}}$	$(V_{To}(T_{diode}) + r_T(T_{diode})i) i \tau'(t)$
$\tau(t)$	$\frac{1}{2} (1 + m \sin(\omega t + \phi))$	$\frac{1}{2} (1 - m \sin(\omega t + \phi))$

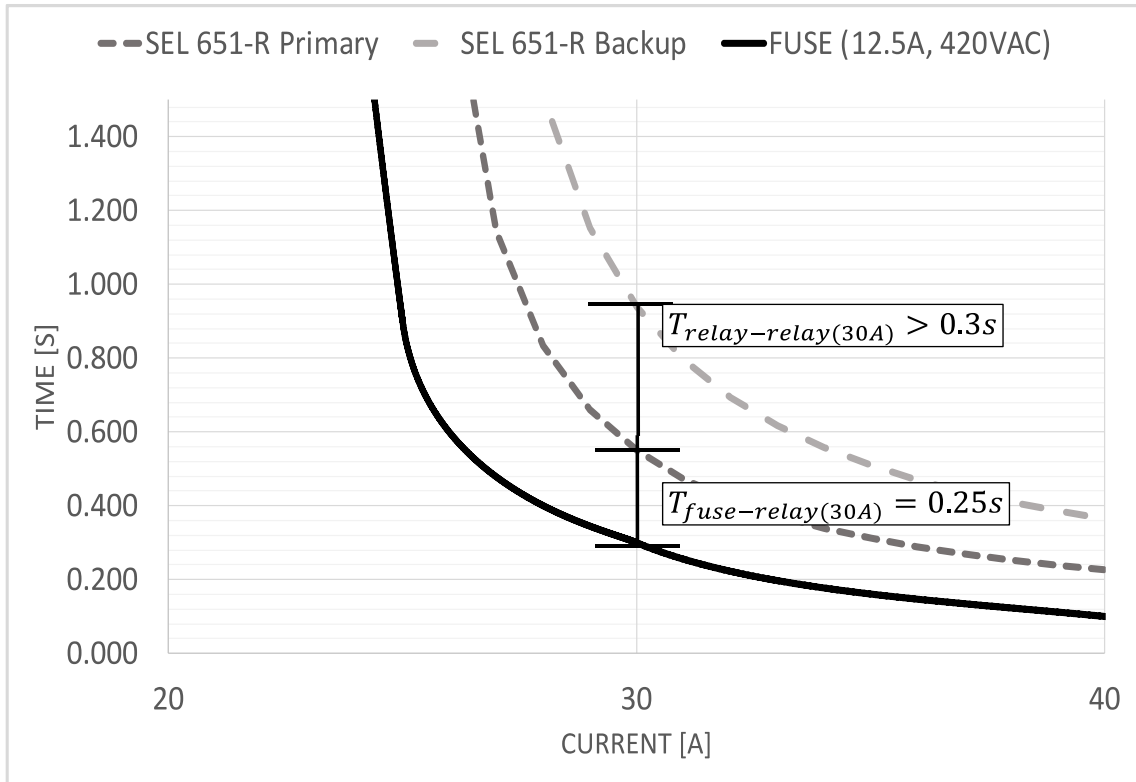


Figure 0.3: TCCs for the 12.5A fuse. SEL 651R used as primary and backup relay. The CTs for both relays are 50-1 ratio. The pickup for the primary relay is 0.46 with a time dial of 1.5. The backup relay has a pickup of 0.5 with a time dial of 2.5. U5 curve for 51 protections is used for primary and backup relay.

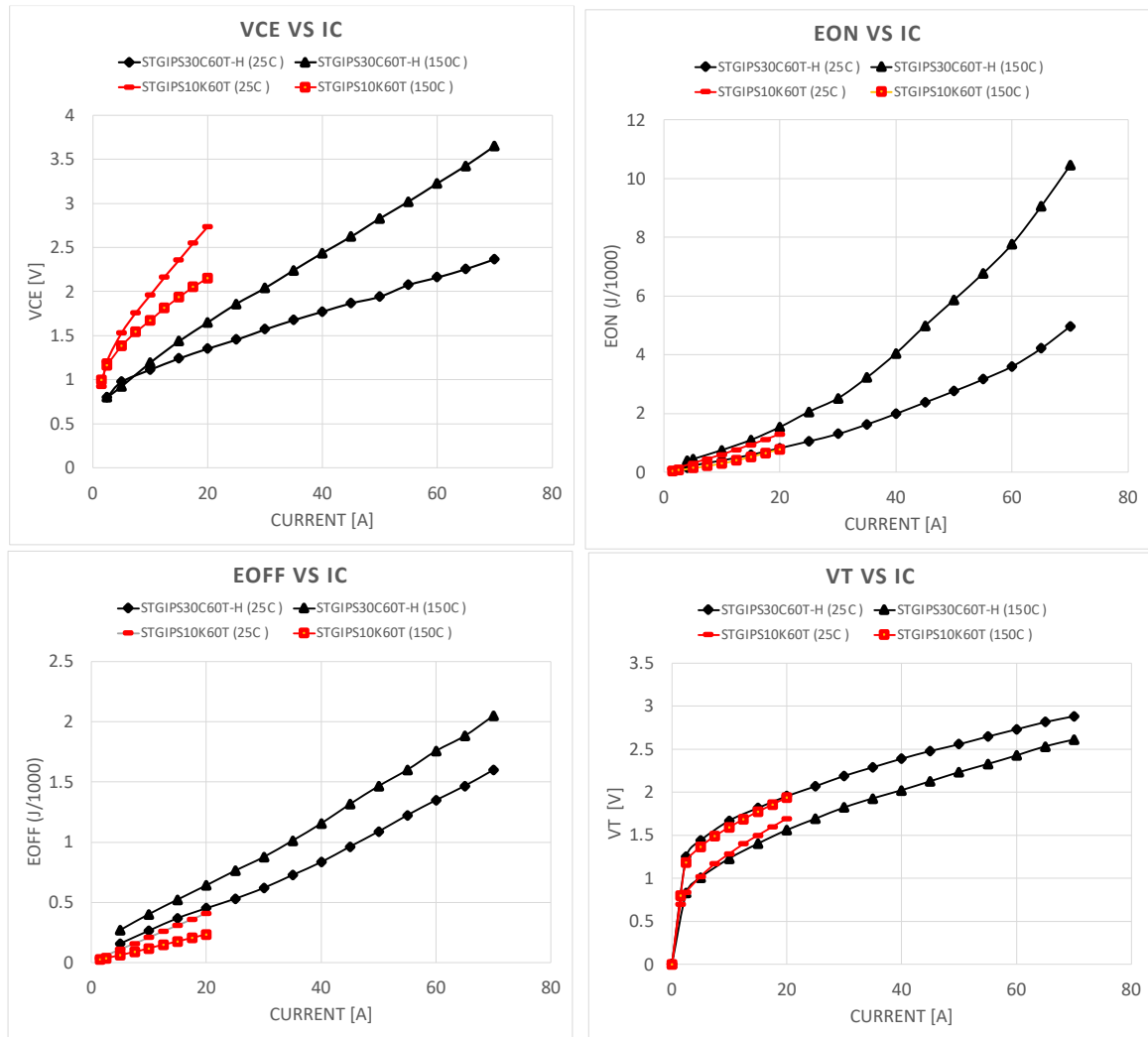


Figure 0.4: ST intelligent modules used in the study. Rated device (STGIPS10K60T, 600V/ 10A). Overrated device (STGIPS30C60T-H, 600V , 30A). The Inverter rated current is 10A.

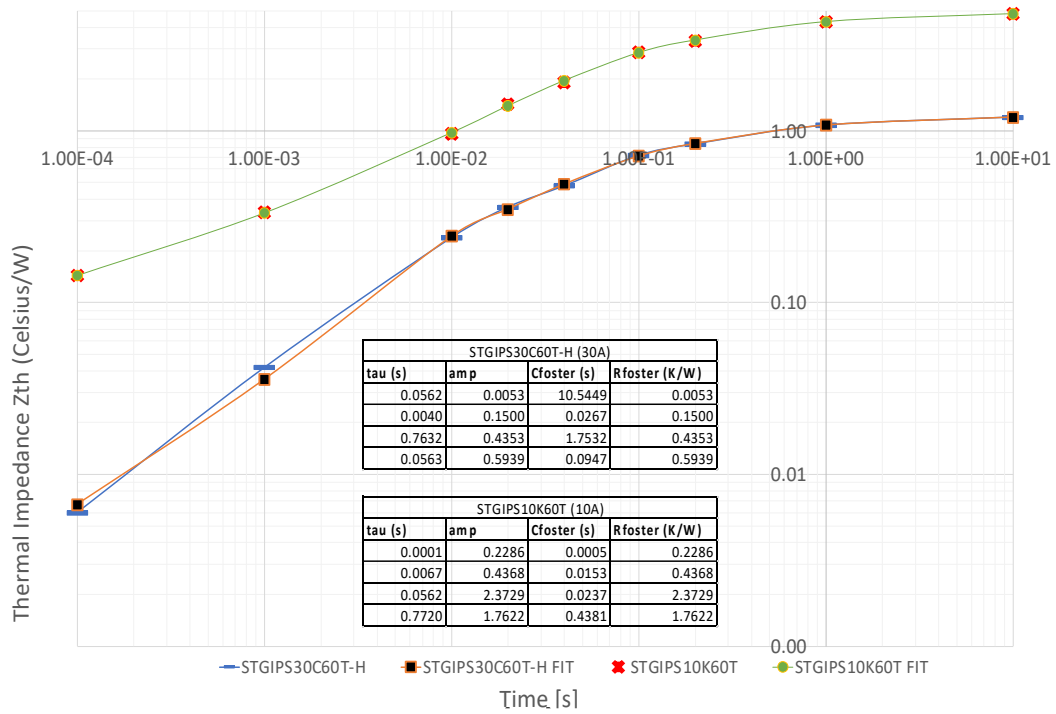


Figure 0.5: Thermal impedance and fit using Foster RC network for the prototype 600 V/10 A module and 600 V/30 A module.

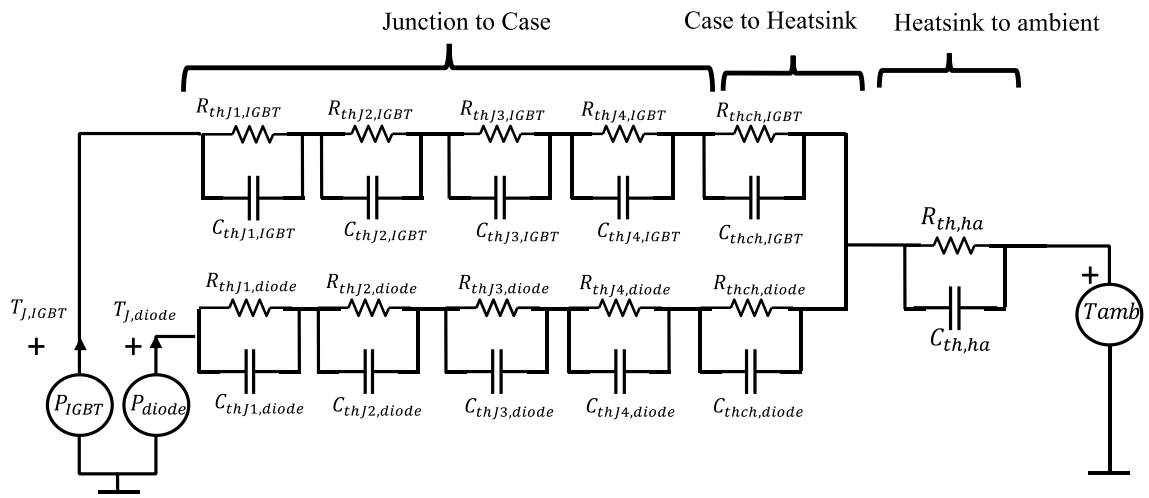


Figure 0.6: Foster thermal network of IGBT and diode

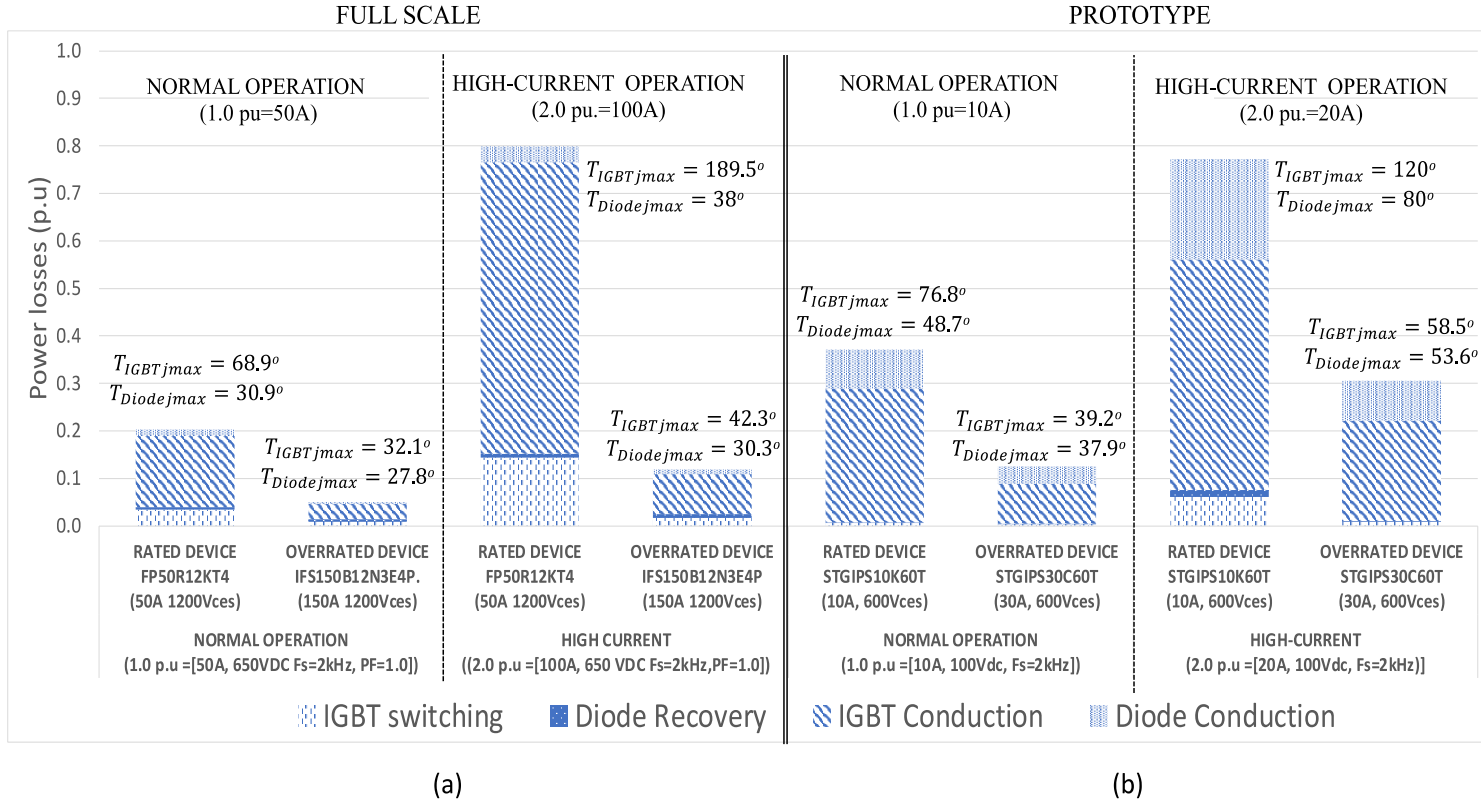


Figure 0.7: Conduction and switching losses for semiconductor used in prototype and full-scale prototype.

The following sections present the control challenges introduced by saturable inductors, derives the small signal model and decoupling terms for the vector control, and presents a control method to tune the current controllers to maintain stability during normal and fault condition.

1.9. Modelling Saturable Inductors

In saturable inductors, the flux increment per current increment rapidly decreases as the operating current magnitude increases [38, 42]. This phenomenon is called saturation of the magnetic core. In Fig. 1.8 the corresponding inductance-current characteristics of the ferrite inductors used in this chapter is shown. The inductor cores were characterized using a DPG10 Power Choke Tester. As shown in the figure, due to the core saturation, the available inductance decreases as the magnitude of the current increases. The inductance of the ferrite core drops until it reaches 0.6 mH at 35 A, which is a reduction of about 45% compared to the initial inductance of 1.1 mH. The Appendix in this dissertation shows the saturation characterization for other silicon steel and ferrite cores obtained from DPG10 Power Choke Tester. This chapter uses the results of the ferrite core as typically found in power electronic applications. Ferrite cores are utilized for higher frequency applications because they have lower losses at high frequency; however, their core saturates at lower flux density

Equation (1.6) has been used in the literature to describe the nonlinear inductor in a polynomial form [38-39], where i is the instantaneous current flowing through the inductor ($i = I \sin \omega t + \delta$), and L_o is the inductance at zero current, and L_n a constant term that can be adjusted to fit the saturation characteristics of the inductor. This fit equation will be used later in this chapter to derive the vector control considering saturable inductors.

$$L_s = L_o + L_2 i^2 + L_4 i^4 \quad (1.6)$$

For validating the fit equation, the even, second-order polynomial is used for the ferrite core. The parameters of the even order polynomials L_o , L_2 are needed to be specified to fit the measurements presented in Fig 1.8. The fit method consisted of minimizing the root

mean square error (RMSE) using the generalized reduced gradient (GRG) nonlinear engine in Excel.

For the ferrite core, the estimated value of L_o and L_2 are 1.1 mH and -0.4mH. A good agreement with the second order polynomial was obtained with a RMSE is 0.02 and the correlation R is 0.98. Fig. 1.9 and Fig.1.10 show the model validation of the fit equation (1.6) against physical measurements from the nonlinear inductor for the grid-filter in the prototype inverter. The validation was done by increasing the phase-a current in the prototype inverter from 0 to 30A to capture both the linear and nonlinear regions of the inductor. The measured current is then compared against a circuit model simulated in Simulink. The simulation circuit implements (1.6) and includes the resistance of the circuit, which was measured with a multimeter and was equal to 0.25Ω . Details of the simulation circuit can be found in the Appendix. To quantify the deviation between the measurements and the model estimated currents, the same criteria as in [63] is used by calculating the following expression:

$$Error_{\%} = \left| \frac{I_{measured} - I_{model}}{I_{measured}} \right|_{100} \leq 10\% \quad (1.7)$$

where I is the inductor current. The model is declared valid if more than 85% of the samples do not exceed 10% of deviation allowed for a wide range of operation. Fig. 1.11 shows the experimental error and the average error between the fit function and physical measurements. The estimation for the inductor by the second-order polynomial fit is very good, with an error between the model and measurement below 10% for 95% of data points with an average error of 5%.

Fig. 1.12 presents the open loop response of a three-phase inverter employing saturable inductors during normal conditions and high-current operation. At the nominal current, the three-phase currents are sinusoidal with a fundamental frequency of 60 Hz. However, during high-current operation, the inductance of each phase varies with the associated phase current, leading to introduction of a fifth and seventh harmonics in the three phases. In the dq reference frame, these harmonics are present as a sixth harmonic, see Fig. 1.13.

From protection standpoint, the current distortion is not a major concern as the protection acts on the magnitude of the current. However, from a control perspective, the inductance value is critical as it determines the poles of the system which are required to effectively tune the integral and proportional gains. As the inverter control operates in closed-loop for normal and fault conditions, it is important to account nonlinearities of the inductance to guarantee the closed-loop stability during normal and fault conditions.

1.10. **Stability Control of Classical Control with Saturable Inductors**

Fig. 1.14 shows the effects of not retuning the controller gains when the inductors are deeply saturated. The gains of the proportional integral (PI) controller remained constant, and the time delay was captured by a first order Padé approximation and set as 200 μ s to account for the delays of the analog to digital converter (ADC) input, the digital output card, and the FPGA processing time. Notice that for the nominal inductance, the open-loop transfer function meets the stability criteria of phase margin greater than 40 degrees and a gain margin of 8 dB. Fig. 1.14 shows that the phase and gain margin are significantly reduced as the available inductance is decreases caused by the saturation. Reducing the phase and gain margin causes the control to start oscillating and eventually to become unstable. The step response, which included in the same figure, shows an undamped response when the inductance is nominal. However, with a deeply saturated inductor, the step response is undamped with high overshoots. If the inductance continues to drop the closed-loop control would become unstable.

This section derives the small signal model in dq of the three-phase inverter considering the nonlinearities of the inductor. The objective is to analytically obtain the current transfer function and the decoupling terms to properly tune the controller considering the effects of the core saturation.

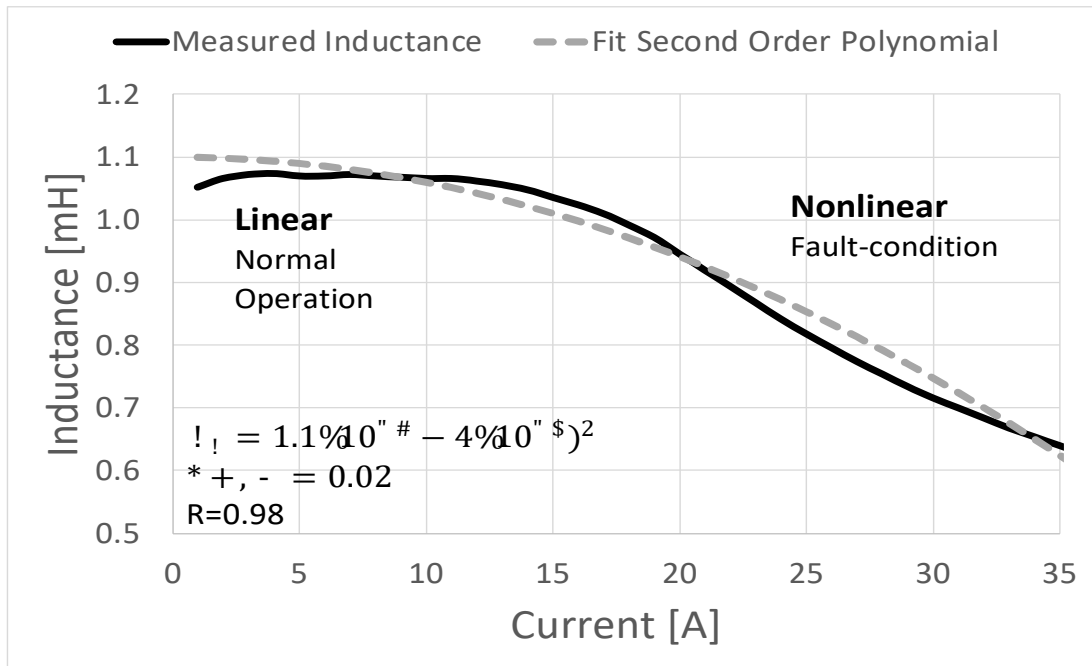


Figure 0.8: Experimental characteristic of the nonlinear inductor used in this work. Inductor characterized at room temperature using DPG10 Power Choke Tester.

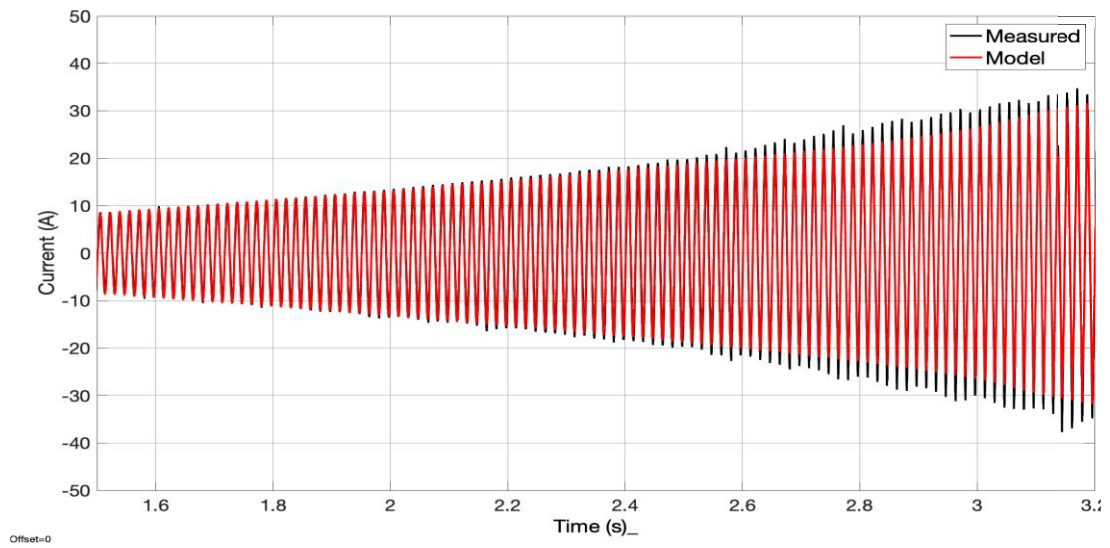
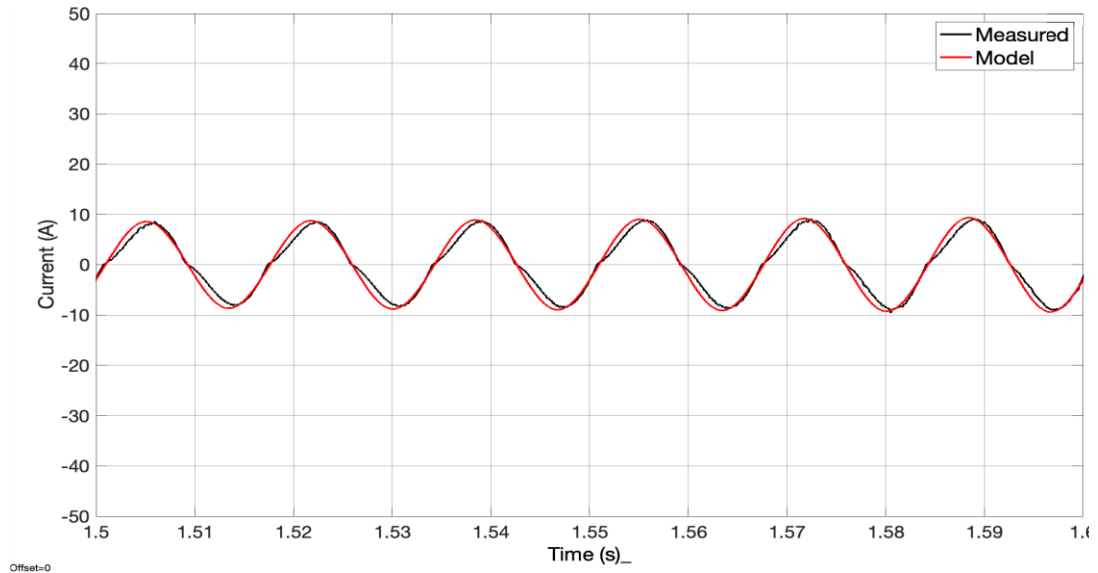
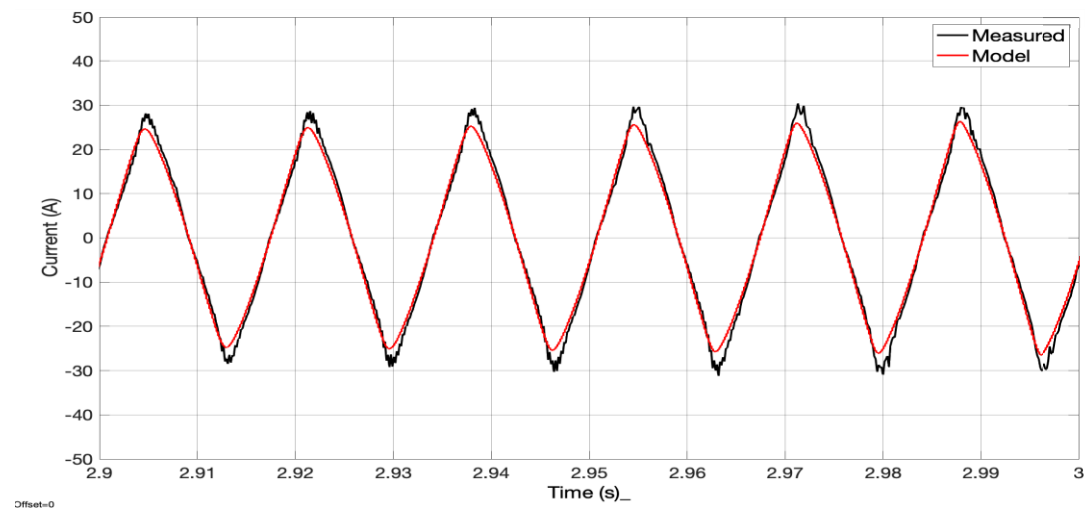


Figure 0.9: Ferrite core model validation with second order polynomial fit. Current ramp from 0 to 30 A to validate the model for both the linear and nonlinear regions of the inductor.



(a)



(b)

Figure 0.10: Ferrite core model validation with second order polynomial fit.
(a) linear region (b) nonlinear region

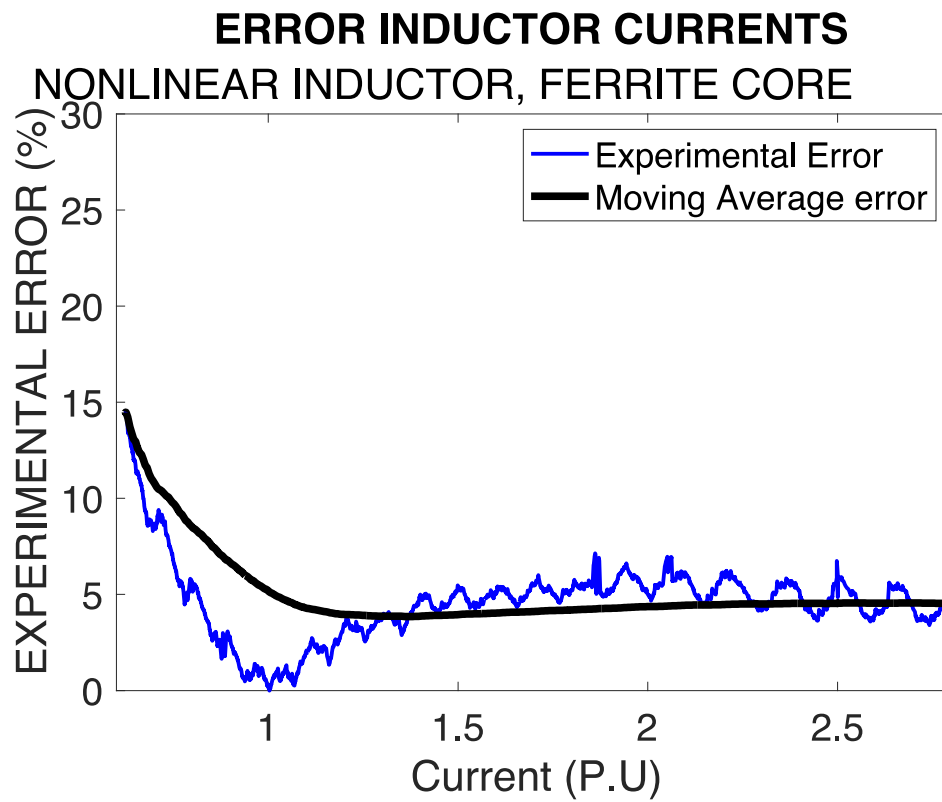


Figure 0.11: Ferrite core model validation with second order polynomial fit (1.6).

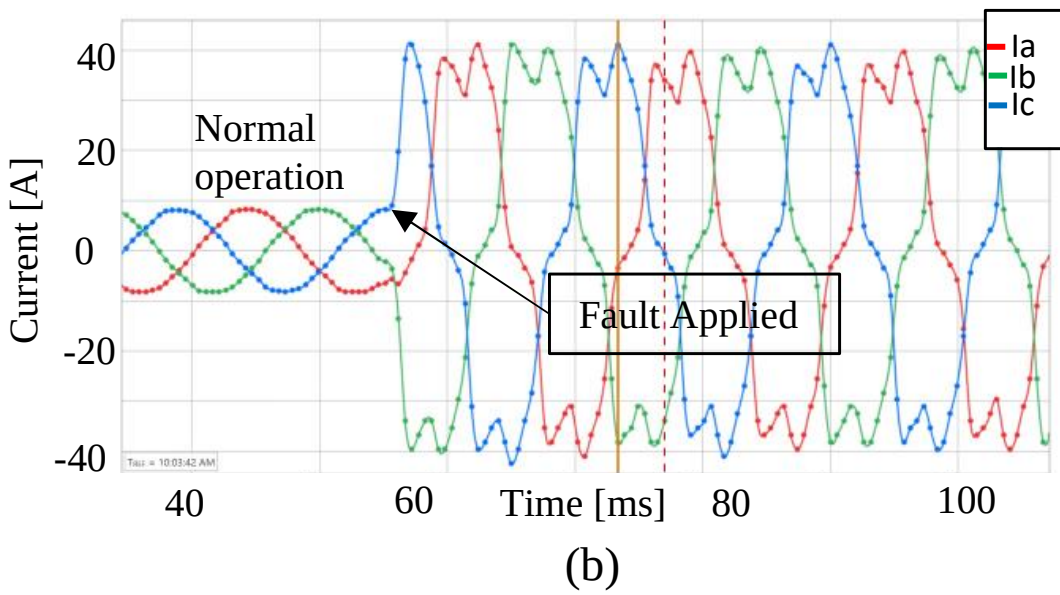
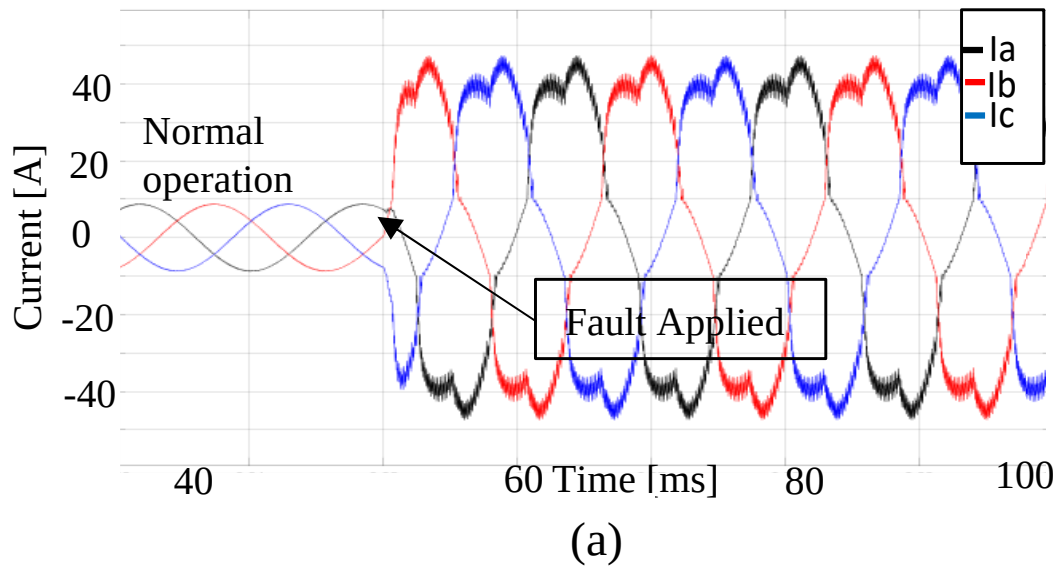
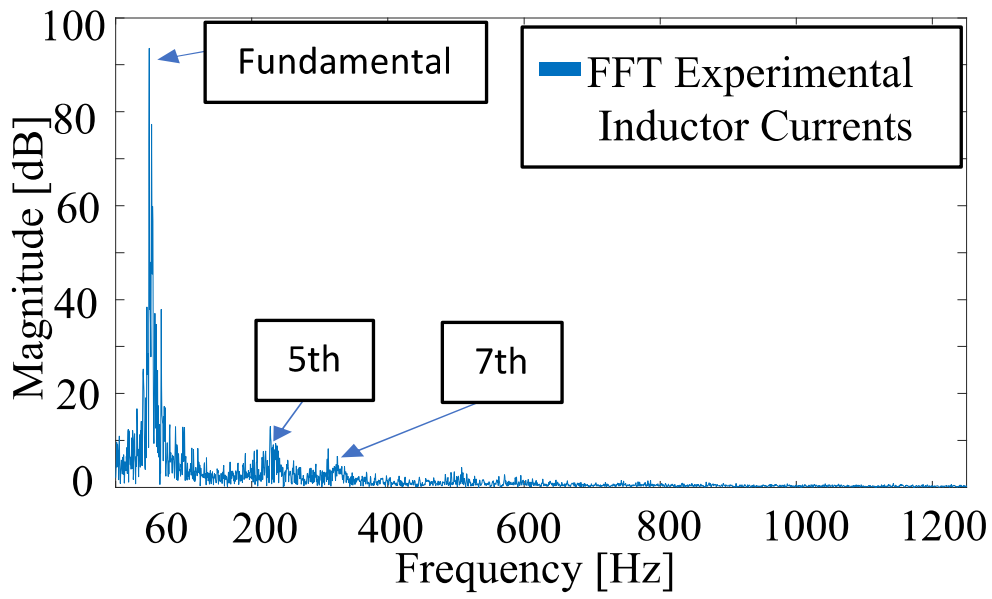
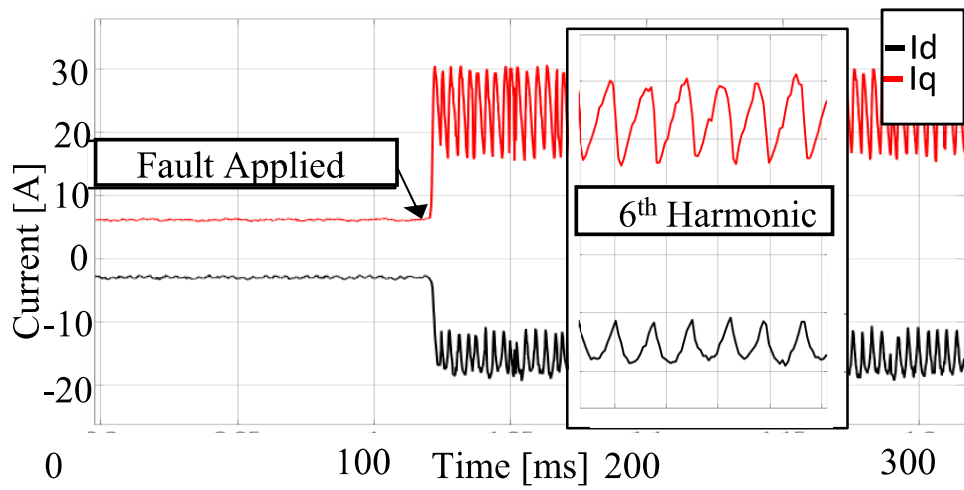


Figure 0.12: Open-loop response of inverter using saturable inductors. (a) Simulated waveforms. (b) Experimental waveforms captured from SEL 651R.



(a)



(b)

Figure 0.13: Open-loop response of inverter using saturable inductors. (a) Fast-Fourier Transform of experimental currents. (b) Control signals in synchronous reference frame

1.11. Vector Control Considering Saturable Inductors

The flux linkage λ in a three-phase converter can be described as:

$$\lambda_{abc} = L_{abc} i_{abc} \quad (1.8)$$

The current controller for the three-phase inverter is implemented in the synchronous reference frame. Then, the inductor matrix in abc -frame needs to be transferred to the dq -frame. Equation (1.9) is obtained by substituting the second-order fit equation (1.6) into (1.8).

This methodology is scalable and can calculate the settings for complex networks with multiple distributed DERs in the system. It was demonstrated through experimental and hardware-in-the-loop results, that the proposed model-adaptive relay effectively protected the laterals against short-circuit faults in the microgrid during islanded operation. In this section, a lateral protected with a 50A fuse was instead protected with the model-adaptive relay. As shown, the model-adaptive relay enables use of overcurrent protection in microgrids. However, this method is not immune to the low short-circuit currents from IBR. For instance, to protect a lateral with the 100A fuse, it would be needed at least 200-300A of short-current current, which is not achievable with the commercial IBRs installed in the microgrid, which limit their current to 1.2 p.u. Other limitations of adaptive relaying are that its reliability relies on a reliable communication network.

$$\lambda_{abc} = \begin{bmatrix} L_o + \sum_{n=1}^{\infty} L_{2n} i_a^{2n} & 0 & 0 \\ 0 & L_o + \sum_{n=1}^{\infty} L_{2n} i_a^{2n} & 0 \\ 0 & 0 & L_o + \sum_{n=1}^{\infty} L_{2n} i_a^{2n} i_c^4 \end{bmatrix} \quad (1.9)$$

where $i_a = I \sin(\theta)$, $i_b = I \sin(\theta - 2/3 \pi)$ and $i_c = I \sin(\theta + 2/3 \pi)$.

The elements of the abc -frame inductor matrix in (1.9) are nonlinear and relate to the instantaneous current flowing through the inductor. To linearize the equations, the following assumptions are made.

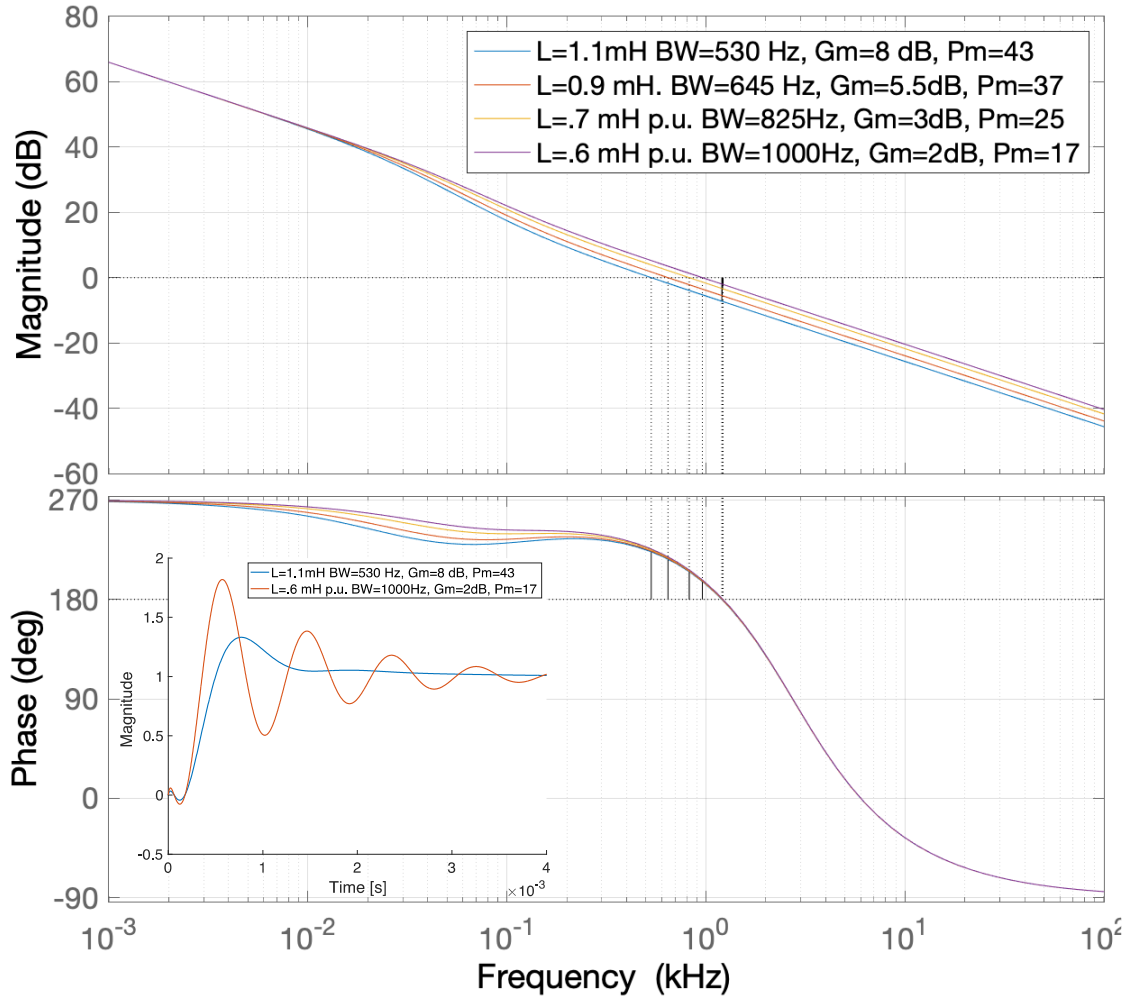


Figure 0.14: Bode plot for different inductance values due to core saturation effect of the ferrite core. Controller gains ($K_p=0.06$, $K_i=10$, Current Sensor Gain=10)

The first assumption is that the three-phase current is balanced without a zero-sequence component. The second assumption is that the currents only contain positive sequence fundamental frequency components. The flux linkage can be expressed in the synchronous reference frame as.

$$\lambda_{dq} = T_{abc/dq} L_{abc} T_{dq/abc} i_{dq} \quad (1.10)$$

Solving (1.10) for a fourth-order polynomial using the code provided in the Appendix, the flux linkage equations are given by:

$$\lambda_d = i_d \left(L_0 + 3 \frac{L_2 I^2}{4} + 5 \frac{L_4 I^4}{8} + I^4 L_4 \cos \frac{6\omega t}{16} \right) + i_q I^4 L_4 \sin(6\omega t)/16 \quad (1.11)$$

$$\lambda_q = i_q \left(L_0 + \frac{L_2 I^2}{4} + \frac{L_4 I^4}{8} - I^4 L_4 \cos \frac{6\omega t}{16} \right) - i_d I^4 L_4 \sin(6\omega t)/16 \quad (1.12)$$

Equations (1.11) and (1.12) are nonlinear coupling terms between the direct and quadrature axis. However, these terms can be linearized on the known operating point current since the magnitude of the cross-coupling terms are very small comparing with the DC equivalent inductance. With this approximation, the flux linkage equations are given by:

$$\lambda_d = i_d \left(L_0 + 3 \frac{L_2 I^2}{4} + 5 \frac{L_4 I^4}{8} + I^4 L_4 \cos \frac{6\omega t}{16} \right) \quad (1.13)$$

$$\lambda_q = i_q \left(L_0 + \frac{L_2 I^2}{4} + \frac{L_4 I^4}{8} - I^4 L_4 \cos \frac{6\omega t}{16} \right) \quad (1.14)$$

The equivalent flux linkage can be further simplified by adopting a second-order polynomial. The second order polynomial provides a very good approximation.

$$\lambda_d = i_d (L_0 + 3 * L_2 I^2 / 4) \quad (1.15)$$

$$\lambda_q = i_q (L_0 + L_2 I^2 / 4) \quad (1.16)$$

These equations show that there are no coupling terms between the direct and quadrature axis components. The equivalent d-axis inductance is only related to $3L_2 I^2 / 4 + L_0$ and

the q-axis equivalent inductance to $L_0 + L_2 I^2/4$. The equivalent inductance is related to the peak current I , which is the operating point of the approximate linearization of the nonlinear control system [153]. The next section will apply this approximated inductance in the dq synchronous reference control of a three-phase power converter.

1.12. VSC Vector Control Considering Saturable Inductors

This section derives the small signal model of the inverter which considers the saturation of the grid filter inductors. As shown in Fig. 1.15, the three-phase voltage source converter (VSC) is connected to the point of common coupling (PCC) through the grid filter. The equations of the three-phase inverter with connection to the grid, with the average state model and the external elements of the circuit are given by equations (1.17) and (1.18).

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc} - \begin{bmatrix} v_N \\ v_N \\ v_N \end{bmatrix} \quad (1.17)$$

$$\frac{d}{dt} v_{dc} = \frac{1}{C} (I_{DCBATT} - I_{DCf}) \quad (1.18)$$

The inductor voltage is related with flux linkage for a three-phase inductor as:

$$\vec{v}_{abc} = \frac{d}{dt} \vec{\lambda}_{abc} = L \frac{d}{dt} \vec{i}_{abc} \quad (1.19)$$

Applying Kirchhoff's current law (KCL) to the circuit of Fig. 1.15.

$$L \frac{d}{dt} \vec{i}_{abc} = \frac{d}{dt} \vec{\lambda}_{abc} = \vec{v}_{abc} - r \vec{i}_{abc} - \vec{d}_{abc} v_{dc} + \vec{v}_N \quad (1.20)$$

Assuming a perfect balanced system, the zero sequence can be neglected.

$$\begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \vec{\lambda}_{dq} + \frac{d}{dt} \vec{\lambda}_{dq} = \vec{v}_{dq} - r \vec{i}_{dq} - \vec{d}_{dq} v_{dc} \quad (1.21)$$

The current loop transfer function is derived by the small signal model, which applies small variations around the operation point.

$$\tilde{i}_d = \frac{-\tilde{d}_d V_{dc} + \omega \tilde{i}_q L_q}{(sL_d + r)} \quad (1.22)$$

$$\tilde{i}_q = \frac{-\tilde{d}_q V_{dc} - \omega \tilde{i}_d L_d}{(sL_q + r)} \quad (1.23)$$

The q and d axis inductances are defined as follows.

$$L_d = L_o + 3 \frac{L_2 I^2}{4} \quad (1.24)$$

$$L_q = L_o + \frac{L_2 I^2}{4} \quad (1.25)$$

The d and q channels are coupled by the terms $\omega \tilde{i}_q L_q$ and $\omega \tilde{i}_d L_d$; these terms are inconvenient to independently control the d and q channels. A way to simplify this is to introduce decoupling terms, such as the one used in [58]. The coupling between channels is shown in Fig. 1.16. The decoupling terms are introduced in Fig. 1.17 to eliminate the coupling between channels, and this results in a first order transfer function with a pole defined by the point of operation and the passive elements of the grid filter. The following equations show that the nonlinear inductance influences the poles of the current control and the decoupling terms.

$$\frac{\tilde{i}_d}{\tilde{d}_d} = \frac{V_{dc}}{(sL_d + r)} = \frac{V_{dc}}{\left(s \left(L_o + 3 \frac{L_2 I^2}{4}\right) + r\right)} \quad (1.26)$$

$$\frac{\tilde{i}_q}{\tilde{d}_q} = \frac{V_{dc}}{(sL_q + r)} = \frac{V_{dc}}{\left(s \left(L_o + \frac{L_2 I^2}{4}\right) + r\right)} \quad (1.27)$$

Fig. 1.18 shows the block diagram of the small signal model for the dq current control loop, where G_{cdqi} is the transfer functions of the current controllers, β_{di} , β_{qi} are the gains associated with the sensing of the currents, which are defined as first-order anti-aliasing filters. G_{PWMi} is the gain of the sinusoidal PWM (SPWM) modulator. The equivalent inductance is related to the peak current I , which is the operating point of the approximate linearization of the nonlinear control system [153]. The small signal model of G_{PWMi} is defined by equation (1.28), in which the effect of the delay produced by its implementation and the sampling and data processing are considered [59].

$$G_{PWMi} = \frac{1}{2V_{pp}} (e^{-s(1-D)T_s} + e^{-s(D)T_s}) \quad (1.28)$$

This transfer function depends on the peak-to-peak amplitude of the triangular PWM signal (V_{pp}), the duty cycle D , which in this case is considered as the average value of one switching cycle ($d = 0.5$), and the maximum delay time T_s . The delay time is replaced by the second order Padé approximation, where $\alpha = 0.5T_s$ and T_s is the maximum delay time. (1.29) [60].

$$e^{-s(D)T_s} \approx \frac{1 - \alpha s}{1 + \alpha s} \quad (1.29)$$

The current controllers are designed by utilizing the open loop transfer function (1.30) and (1.31). Notice that the core saturation introduces a pole that depends on the operation point of the inverter and the fit constant L_2 .

$$T_{id} = \beta_d G_{cd} G_{PWM} \frac{V_{dc}}{\left(s \left(L_o + 3 \frac{L_2 I^2}{4} \right) + r \right)} \quad (1.30)$$

$$T_{iq} = \beta_q G_{cq} G_{PWM} \frac{V_{dc}}{\left(s \left(L_o + \frac{L_2 I^2}{4} \right) + r \right)} \quad (1.31)$$

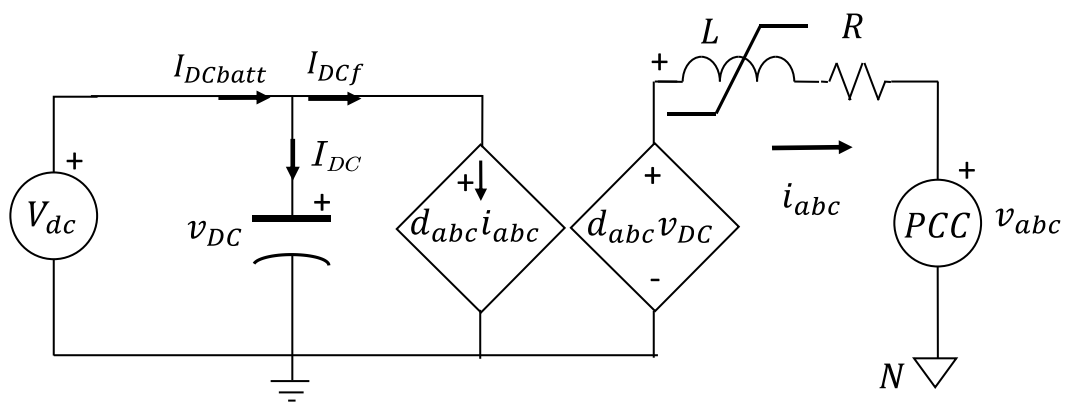


Figure 0.15: Inverter schematic in the abc frame considering nonlinear inductor

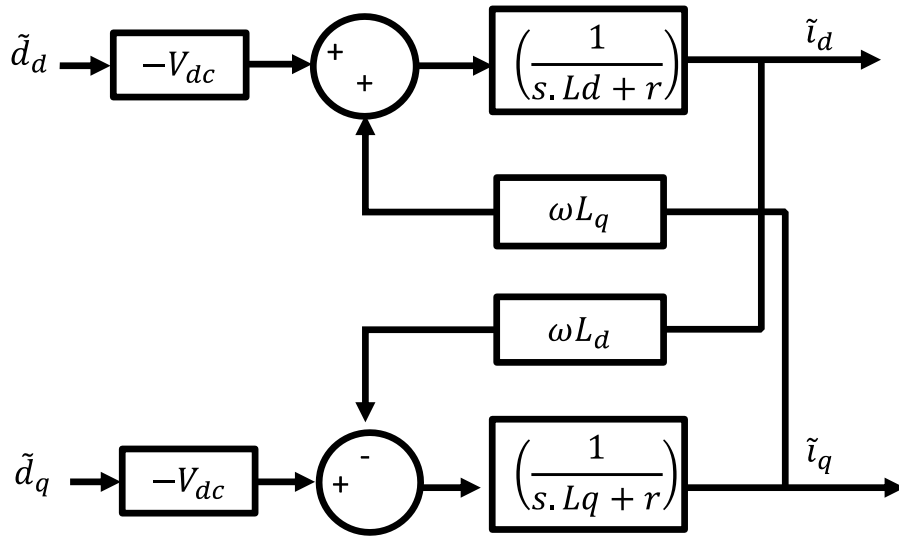


Figure 0.16: Small signal model of the inverter in dq coordinates.

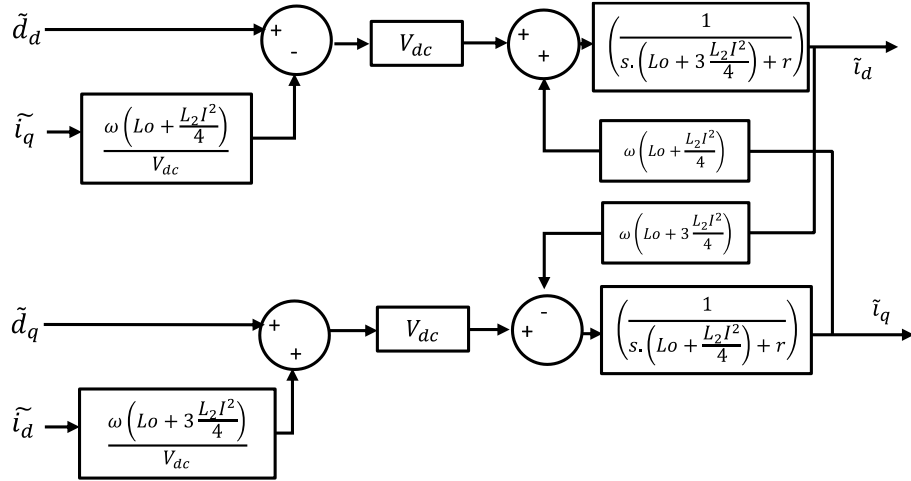


Figure 0.17: Small signal model of the inverter in dq coordinates including decoupling terms considering saturable inductors.

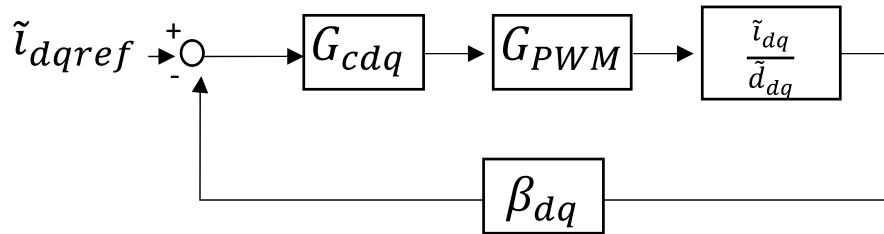


Figure 0.18: inverter current control loop in dq

1.13. Proposed Current Controller Considering Inductor Saturation

This section presents the method to calculate the control gains considering the saturable inductors. The proposed method consists of retuning the integral and proportional gains considering the available inductance in the grid filter. This method first estimates the grid filter inductance for the dq -channels for the given operating current using (1.24) and (1.25). Then, a Butterworth polynomial is adopted to optimize the closed loop eigenvalue locations [40,41]. This Butterworth polynomial locates the eigenvalues uniformly in the left-half s -plane on a circle with radius ω , with its center at the origin. The Butterworth polynomial receives as inputs the inductance value L_{dq} , the system delay α , and the desired bandwidth for the current controller ω , which is typically 8 to 10 times smaller than the switching frequency. The third order Butterworth polynomial can be expressed as:

$$s^3 + (1 + 2\zeta)\omega s^2 + (1 + 2\zeta)\omega^2 s + \omega^3 \quad (1.33)$$

where ω is the bandwidth of the current controller, which is set ten times lower than the switching frequency, and ζ is a constant that influences the damping response. The time delay is captured by a first order Padé approximation (1.29).

The open loop transfer function of the current loop can be expressed as:

$$T_{idq} = \beta \left(\frac{1 - \alpha s}{1 + \alpha s} \right) \left(K_p + \frac{K_i}{s} \right) \left(\frac{V_{dc}}{sL_{dq} + R} \right) \quad (1.34)$$

Where β is the gain for the current sensor, K_p the proportional gain, K_i the integral gain, R the inductor resistance and L_{dq} are the d-axis and q-axis inductances (1.23) and (1.24).

The closed loop transfer function for the current control is obtained using the current open-loop transfer function (1.30-3.31) and the second order Padé approximation (1.29)

$$G_{id} = \frac{(V_{dc}(\alpha - s) * (K_i + K_p s))}{s^3 L_{dq} + s^2 r + s \alpha r - s \beta K_i V_{dc} + s^2 L_{dq} \alpha - s^2 \beta K_p V_{dc} + s \beta K_p \alpha V_{dc} + K_i \beta \alpha V_{dc}} \quad (1.35)$$

The controller gains K_{pi} are obtained by comparing the coefficients in the Butterworth polynomial (1.33) with the denominator of the closed-loop transfer function, (1.35).

$$K_i = \frac{\omega^3 L_{dq}}{\beta \alpha V_{dc}} \quad (1.36)$$

$$K_p = \frac{\omega^2 L_{dq}(1 + 2\zeta) + \beta K_i V_{dc} - \alpha r}{\beta \alpha V_{dc}} \quad (1.37)$$

Fig. 1.19 shows the Bode plot of the current open loop transfer function (1.34). The constant ζ is set to one, and the bandwidth of the controller is set to $\omega = 2\pi 600$ rad/s. The Bode plot shows the efficacy of the proposed adaptive controller gain method, which guarantees the phase margin greater than 40 degrees and the gain margin above 8 dB for all the operating points. This provides a solution to the challenges previously presented in the Bode plot of Fig. 1.14, where it was shown that phase and gain margins decreased as the inductor saturates. With the proposed controller, the stability margins are maintained regardless of the of inductor saturation. The step response shows the same response when the inductor is in the linear region and when it is deeply saturated. The proposed controller is computationally lightweight and can be easily implemented in the same inverter microcontroller.

1.14. Experimental Results

The experimental results are divided into three sections. The first section presents results that showcase the limits of normally rated semiconductors under high short-circuit current operation. Following this test, a semiconductor with overrated current rating is tested to show that it can safely provide high short circuit current. For this first section, the inverter current control is disabled to decouple its dynamics, and the inverter operates in open loop control. The second section addresses a comparison between the proposed control that consider the core saturation against a fixed PI controller during fault conditions. The third

section presents a coordination study using the proposed energy storage inverter (ESI). The fuse-relay coordination tests are divided in i) fuse-blowing scheme, ii) primary backup coordination and iii) backup relay coordination.

1.14.1. Normally Rated Power Module

The first tests consist of evaluating the short-circuit limitations of an inverter with a semiconductor rated at the inverter current rating. For this section, the inverter is isolated from the current controller, and the control for the inverter is open loop. The inverter with the rated device is controlled to provide 1.25 p.u. (typical for PV inverters), 1.5 p.u., 2.0 p.u. and 3.0 p.u. [12.5, 15, 20 and 30] Arms. The maximum short-circuit current allowed is controlled by the saturation block of the voltage controller, $[i_{max}, i_{min}]$ in Fig. 1.20.

As shown in Fig. 1.20(a) and Fig. 1.21(a), the normally rated device can withstand faults up to 1.25 p.u. For this fault, the increase in temperature in the IGBT junction compared to pre-fault state is small ($\Delta T = 30\text{ }^{\circ}\text{C}$). In other words, this device can provide this fault current even during high temperature operations without overheating the die. Fig. 1.20(c) and Fig. 1.21(c) show that the normally rated device can provide twice its rated current; however, the temperature swing is 100°C . With this temperature swing, the device would exceed maximum operating temperature (150°C) if the initial temperature of the junction is greater than 50°C . Finally, the inverter with rated device is set to provide 3.0 p.u. of fault current. As seen in Fig. 1.20(d), the device had a catastrophic failure after 0.25 seconds. Fig. 1.21(d) shows that the device rapidly surpasses the maximum junction temperature ($t=0.15\text{ s}$), after which the device is permanently damaged.

1.14.2. Overrated Current Module

The tests with the normally rated device show that although the rated device can provide 2.0 p.u, the initial junction temperature must be lower than $50\text{ }^{\circ}\text{C}$, which is not a realistic constraint for real applications. To increase the fault contribution of the inverter, the rated

semiconductor is replaced with a semiconductor with overrated current rating to provide higher current during faults. The other inverter components remain at their rated power.

Fig. 1.20(e)-(f) shows the experimental results with the overrated semiconductor when the inverter provides 2.0 p.u. and 3.0 p.u. of fault current. Fig. 1.21(e)-(f) presents their corresponding simulated thermal response. As shown, the semiconductor with overrated current rating provides higher fault currents while keeping the device within established safety margins. This device can withstand 2.0 p.u. of fault current with a maximum $\Delta T = 20\text{ }^{\circ}\text{C}$, and 3.0 p.u. with a maximum $\Delta T = 40\text{ }^{\circ}\text{C}$. These results indicate that inverters with larger semiconductors can provide high fault current even when the initial junction temperature is high.

1.15. Coordination Grading Time

Table 1.9 illustrates the effects of different short-circuit currents in the protection coordination between relays and fuses. For short-circuit currents of 1.25 p.u., which is typical for PV inverters, neither the fuse nor the primary or backup relays operate in less than 10s. A similar result was obtained for short-circuit currents of 2.0 p.u. Finally, at currents greater than 3.0 p.u., the fuse melts rapidly in 0.26 seconds, and the protection coordination is maintained with the primary and backup reclosers, which trip in 0.6s and 0.85s, respectively. These results indicate that a minimum of 3.0 p.u. of fault current is required to maintain overcurrent coordination. Although it is possible to modify the relay's setting to trip at lower currents, this would make maintaining the grading margins very narrow. For fuses and relays, the recommended grading margin is 0.25, for relay to relays, 0.3s is standard [45]. The grading time is defined as the time margin between the TCC curves of fuses and relays, or between relays and relays. This time must be greater than 0.25 for digital relays to prevent simultaneous tripping.

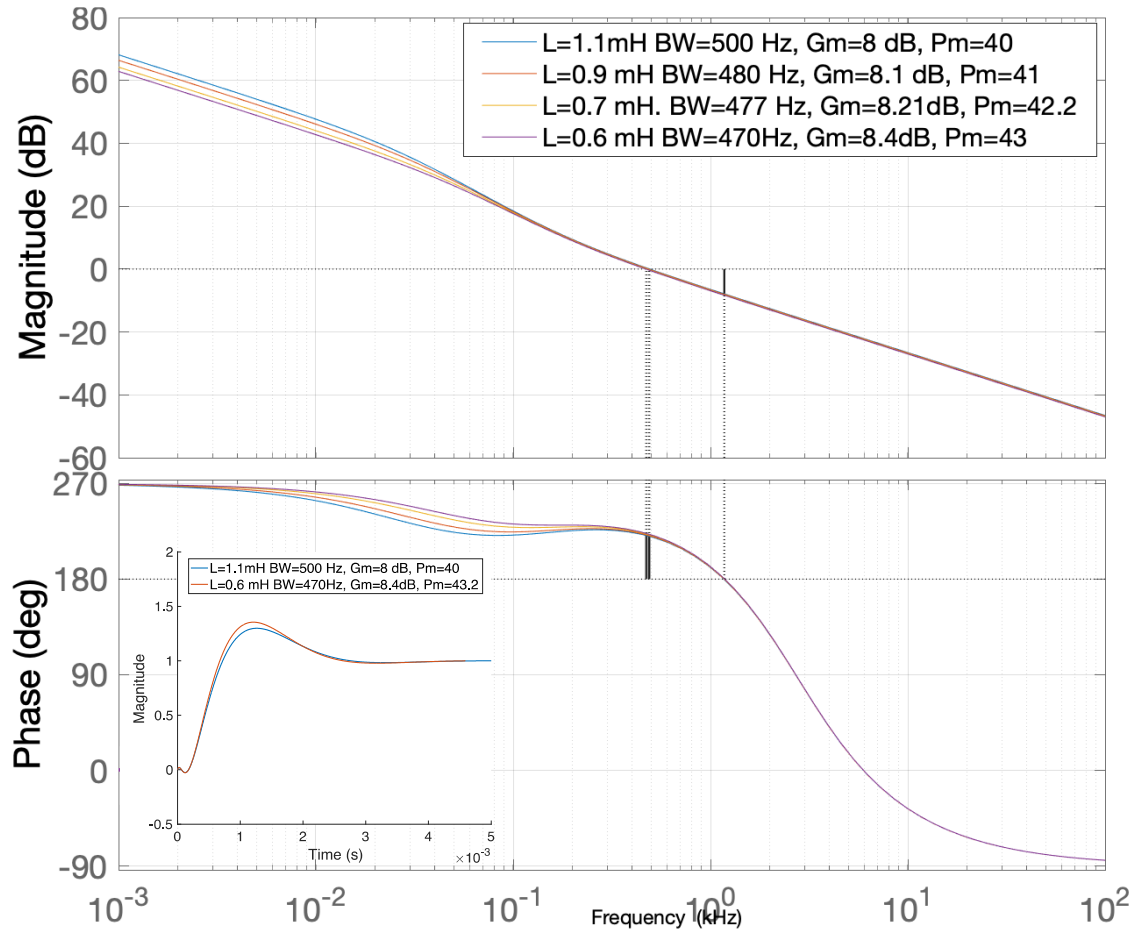


Figure 0.19: Bode plot for different inductance values due to core saturation effect of the ferrite core. PI gains calculated using the proposed controller which considers the core saturation.

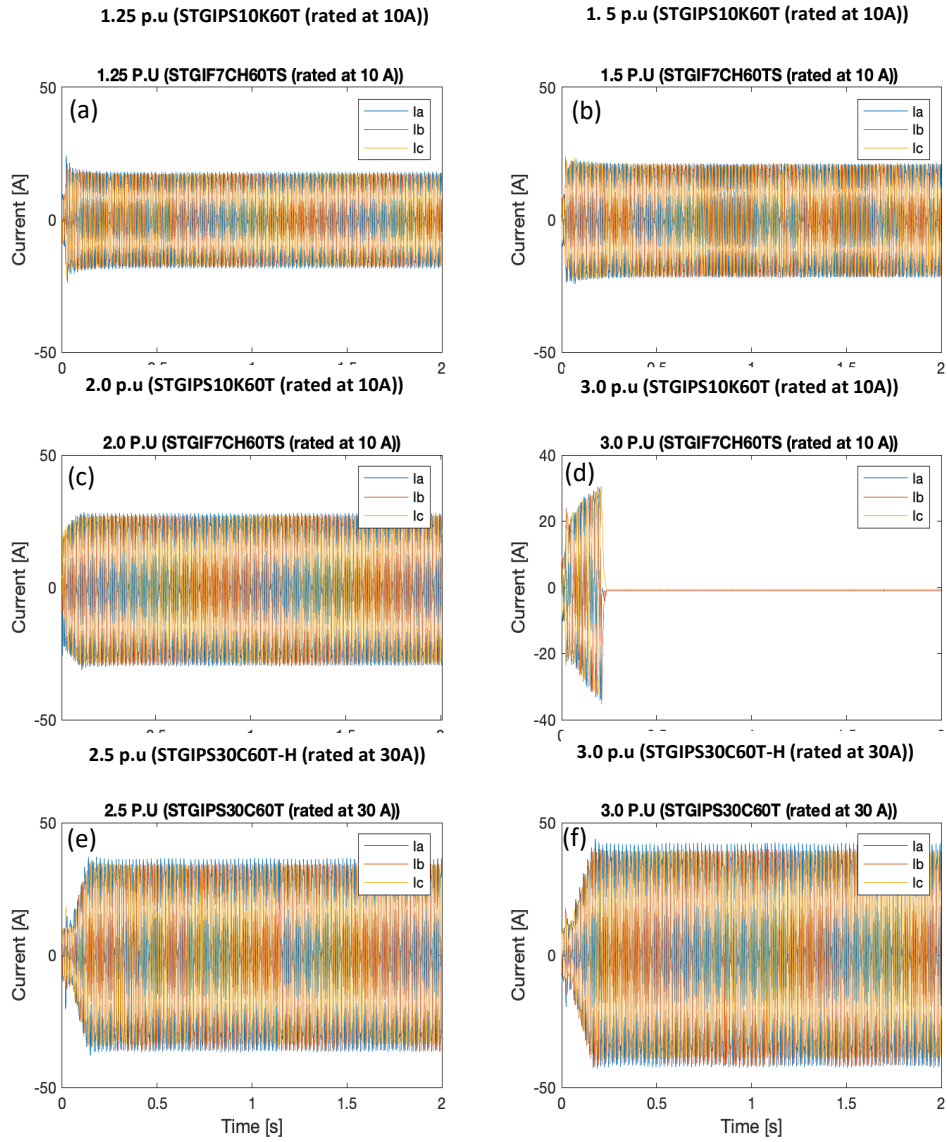


Figure 0.20: Experimental results. Rated device: (a) 1.25 p.u, (b) 1.5 p.u, (c), (d) 2.0 p.u. (d) 3.0 p.u. Overrated device: (e) 2.5 p.u. (f) 3.0 p.u.

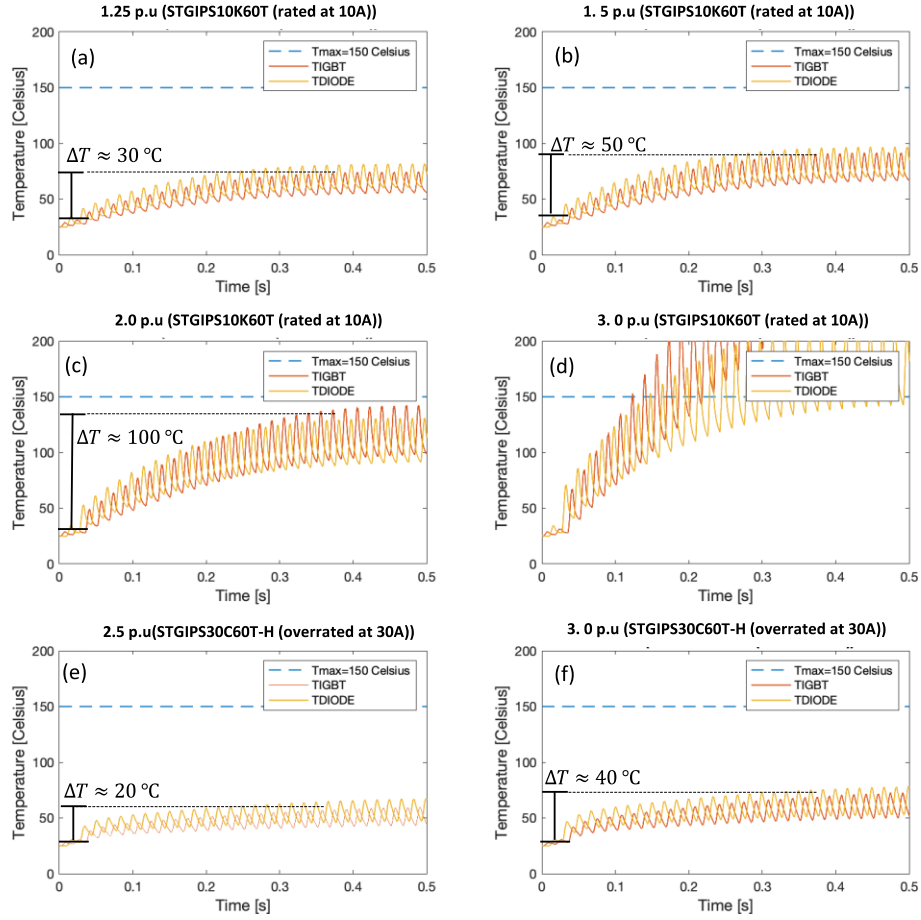


Figure 0.21: Electrothermal simulation: Rated device: (a) 1.25 p.u, (b) 1.5 p.u, (c), (d) 2.0 p.u. (d) 3.0 p.u. Overrated device: (e) 2.5 p.u. (f) 3.0 p.u

1.16. Experimental Results: Proposed PI with adaptive control gains vs classical control

This section presents experimental results that compare the dynamic response of the proposed control, which considers inductor saturation, against a conventional control with fixed PI gains. Three types of faults were evaluated to validate the stability of the controls: line to ground, line-to-line, and three-phase faults (LG, LL, 3-phase (LLLG)). This section utilizes the prototype inverter with an overrated semiconductor device and a normally rated grid-filter inductor.

Fig. 1.22 and Fig. 1.23 present experimental results of the proposed inverter subjected to for a three-phase fault. Fig 1.22 shows the results using a conventional PI controller with fixed PI gains, and Fig. 1.23 shows the results using the proposed controller. As shown, a controller with fixed PI present severe oscillations when the fault is applied. As previously discussed, the inductor saturation reduces the phase and gain margin of the current control, which reduces the stability margin causing overshoots and oscillations when the inverter operates at high current. Fig. 1.23 shows the results with the proposed controller, at the bottom of this figure is the calculation of the proportional and integral gains, which are adjusted to maintain the stability criteria during high current and normal operation. This figure also shows a smooth transition during normal operation to fault condition and no oscillations during high-current operation.

Fig. 1.24 and Fig. 1.25 show experimental results for a line to line (LL) faults. Fig 1.24 shows the results using a conventional PI controller with fixed PI gains, and Fig. 1.25 shows the results using the proposed controller. Line-to-line faults also present oscillations when the fault is applied as the control cannot properly regulate the currents when the core saturates. Fig. 1.25 shows that the proposed controller provides a good regulation and a stable operation during faults. The control signals of Fig. 1.24 and Fig. 1.25 show that a negative sequence current with a frequency at 120 Hz is present during asymmetrical faults. This negative sequence is introduced due to the severe imbalance in the voltage caused by the asymmetrical faults.

Finally, Fig. 1.26 and Fig. 1.27 show experimental results for a line to ground (LG) faults. Fig. 1.26 shows that with a conventional controller, the faulted phase presents oscillations at high current operation. Fig. 1.27 shows that the proposed controller effectively provides a good regulation and a stable operation during faults. The 120 Hz signal in dq coordinate is introduced due to the severe imbalance in the voltage caused by the asymmetrical faults.

1.17. Coordination Study Using Proposed Inverter

This section presents the coordination study using the proposed inverter design and control. Fuse-relay and relay-relay coordination are evaluated to determine if full protection coordination is achievable in an islanded system. The coordination study is performed for high impedance LG, LL, and 3-phase faults. The time current curves (TCC) for the primary relay, backup relay, and fuses were presented in Fig. 1.3. To maintain coordination, the fuse-relay grading margin was set to 0.25 seconds, and the relay-to-relay margin was set to be greater than 0.3s.

Fig. 1.28-1.30 shows the fault current recorded by the SEL 651R, which captured the overcurrent event and the clearing time for the fuses located at the end of the line. Fig. 1.28 shows the results for a line to ground fault in phase c. For the LG fault, the fuse cleared the faults in 17 cycles. Fig. 1.29 shows a LL fault applied at the end of the line. The fault cleared first in phase-c in 14 cycles and then in phase-a at 17 cycles. This difference in time can be explained by different fuse melting times. Finally, a three-phase fault was applied at the end of the line, see Fig. 1.30. Like the LL fault, the fuse melting times are different, and the three-phase fault becomes an LL fault after 14 cycles. The fault was finally cleared in all phases after 16 cycles. As shown, the proposed inverter design effectively provided enough current to clear the fuses for LG, LL, and 3-phase faults.

Fig. 1.31-1.33 shows the events for the fuse-relay coordination considering LG, LL and 3-phase faults, respectively. The fuse-relay coordination considers that the fuses fail to clear the fault and the primary relay must isolate the event. As shown, for all faults, the primary

relay maintained the coordination and effectively cleared the faults maintaining a grading time of at least 0.25s.

Fig. 1.34-Fig 1.36 show the results for the primary relay to backup relay coordination considering LG, LL and 3-phase faults, respectively. This test considers the worst-case scenario, where neither the fuses or the primary relay cleared the fault, and that backup relay must protect the system. As shown, the backup relay effectively cleared all faults maintaining the grading margin, which validates that the proposed inverter design allows full coordination in the test system for different types of faults. Table 1.10 summarizes the tripping time in cycles for all the tests. The presented coordination study demonstrates that the proposed inverter design provides high and sustained short-circuit current to enable the fuse-relay and relay-relay coordination, which is a promising step to enable adopting legacy overcurrent protection for islanded microgrids.

1.18. **Conclusion**

In response to the challenges of protecting inverter-based microgrids, this chapter proposed an inverter designed to provide sustained high-current contribution during faults. Increasing the current from IBRs allows microgrid projects to leverage legacy distribution protection devices in islanded microgrids. This chapter demonstrated through experimental results that few modifications are needed for the inverter to provide more than 3.0 p.u. of short-circuit current. 3.0 p.u. proved to be the minimum current that allows full protection coordination while maintain grading margins between fuses and relays. This work also addressed the challenges of controlling inverters with deeply saturated inductors, which is necessary when operating the inverter at high-current using a normally rated inductor. An online method to calculate the proportional and integral gains based on the available grid-filter inductance was derived and validated in hardware. Additionally, this work analytically derived the current transfer function and decoupling terms considering saturable inductors. The proposed design provided sufficient fault current to enable fuse-relay coordination in microgrids operating in islanded mode. The proposed modification increases the fault contribution of IBRs, paving a promising path forward to use conventional distribution overcurrent protection in islanded microgrids.

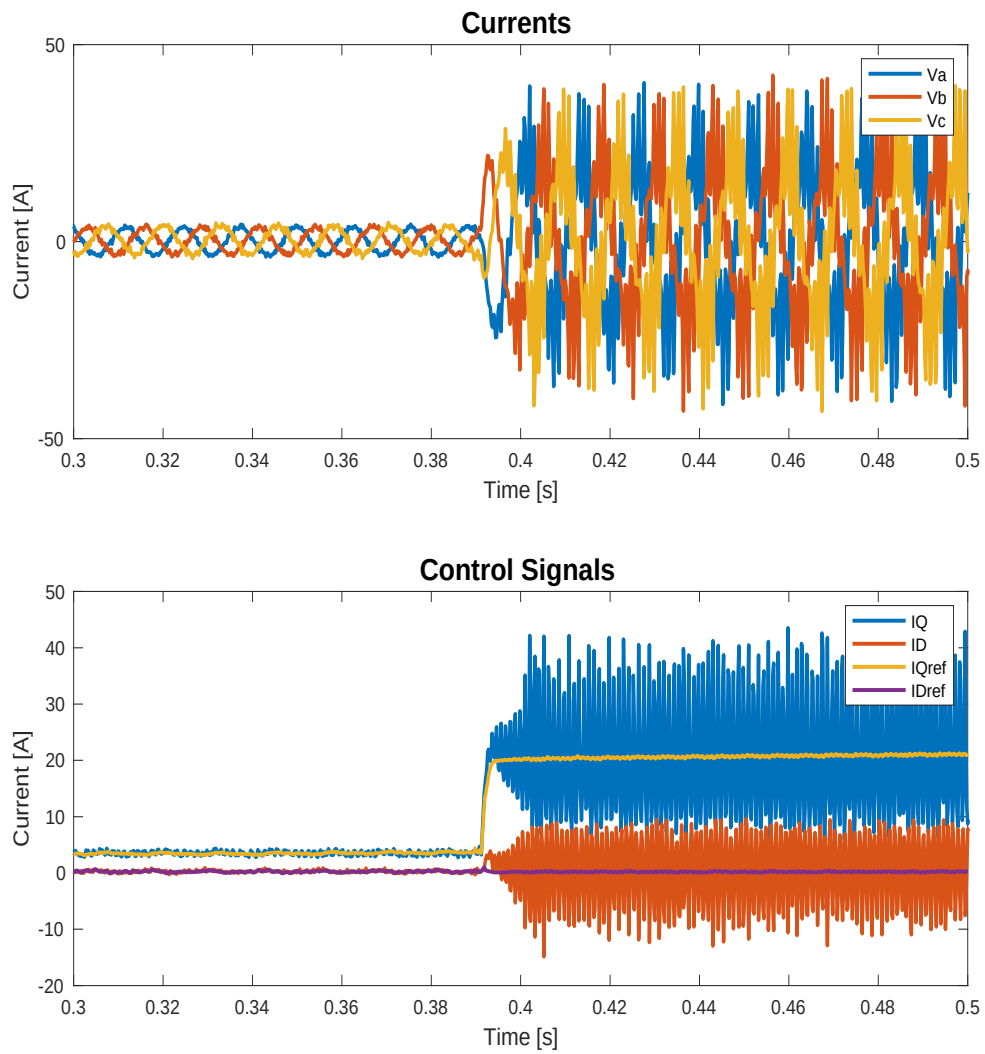
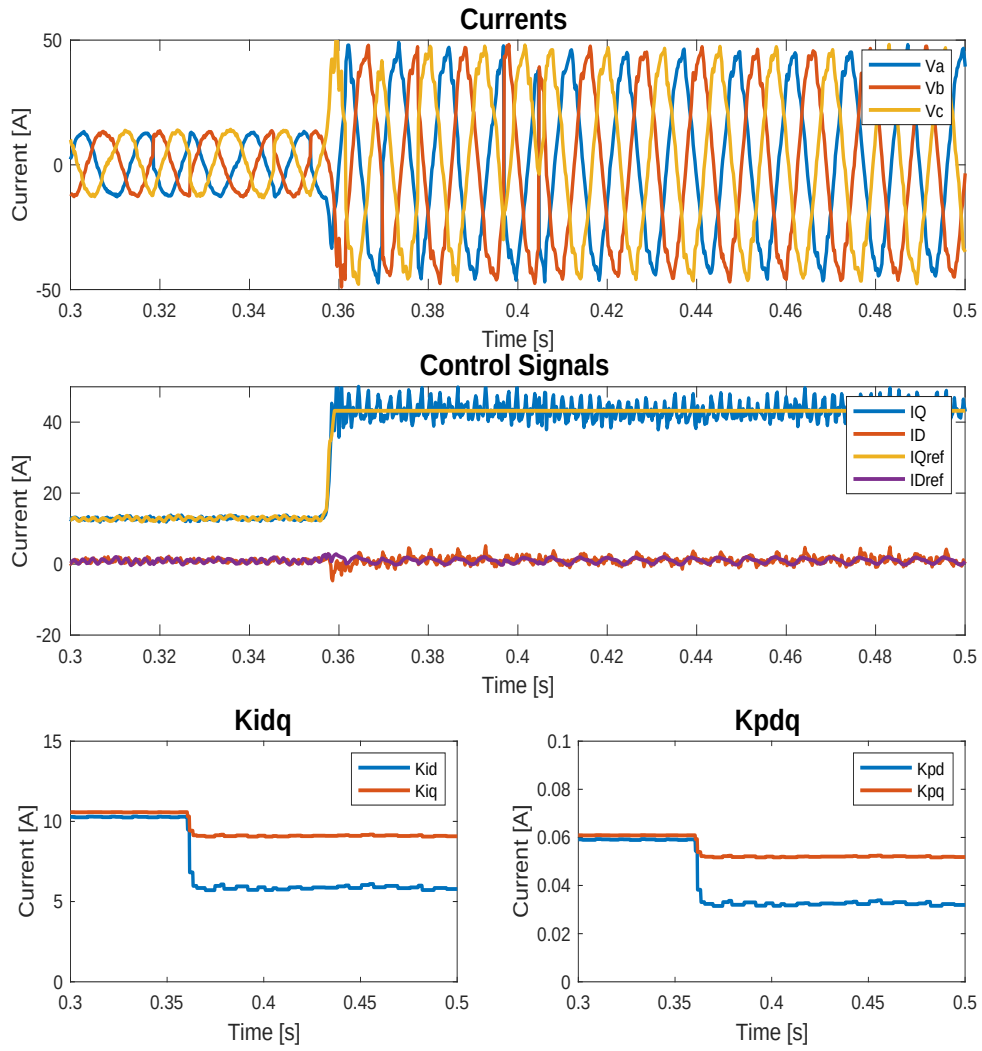


Figure 0.22: Experimental results. 3-ph faults with conventional PI controller.



(b)

Figure 0.23: Experimental results. 3-ph faults with proposed adaptive PI control

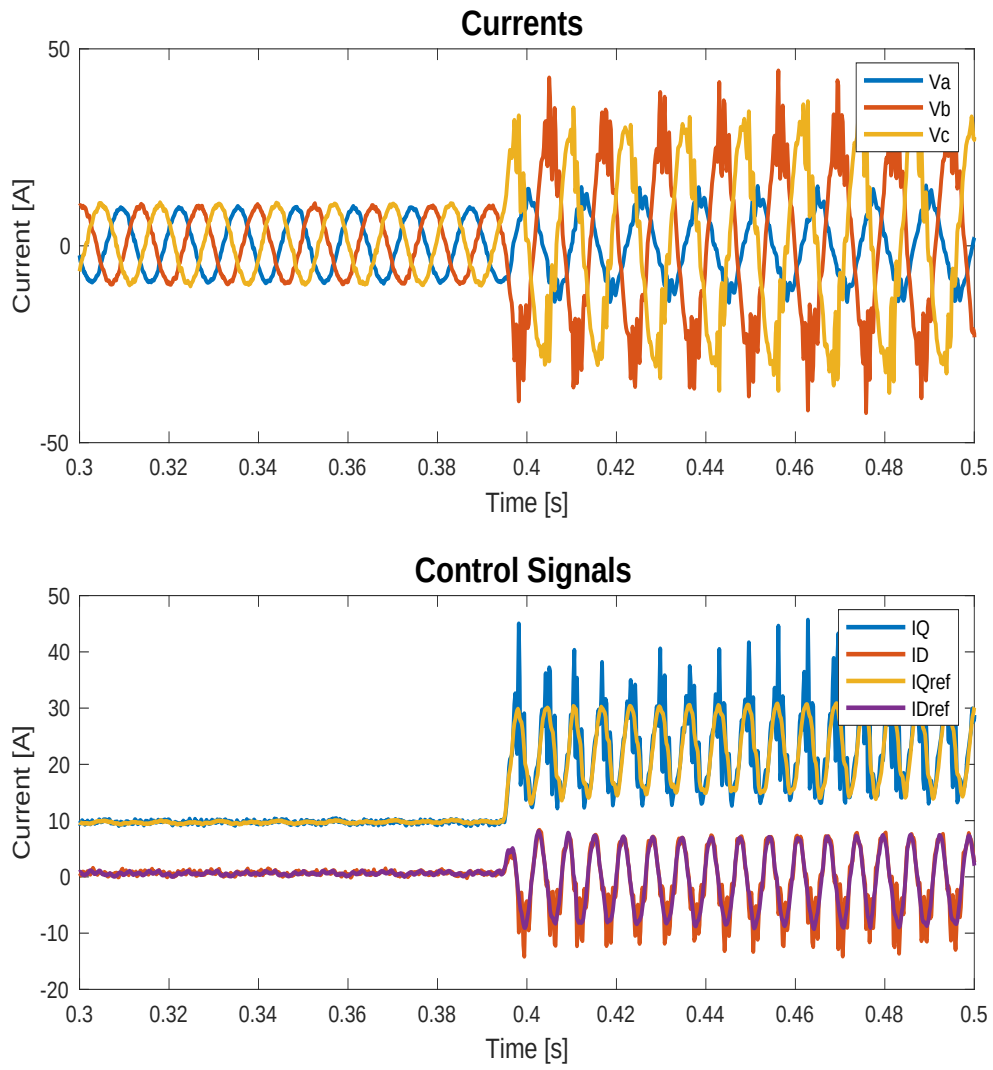


Figure 0.24: Experimental results. LL faults with conventional PI.

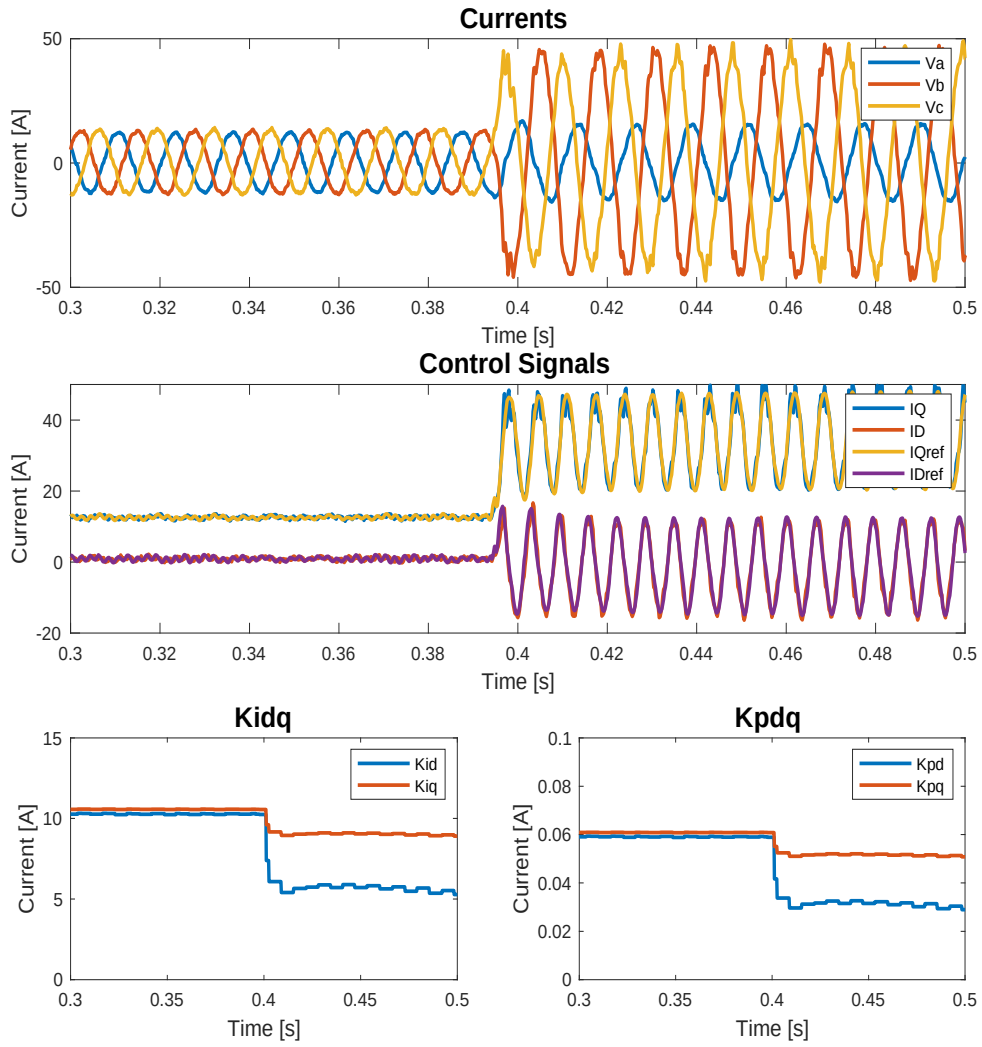


Figure 0.25: Experimental results. LL faults with proposed adaptive PI control

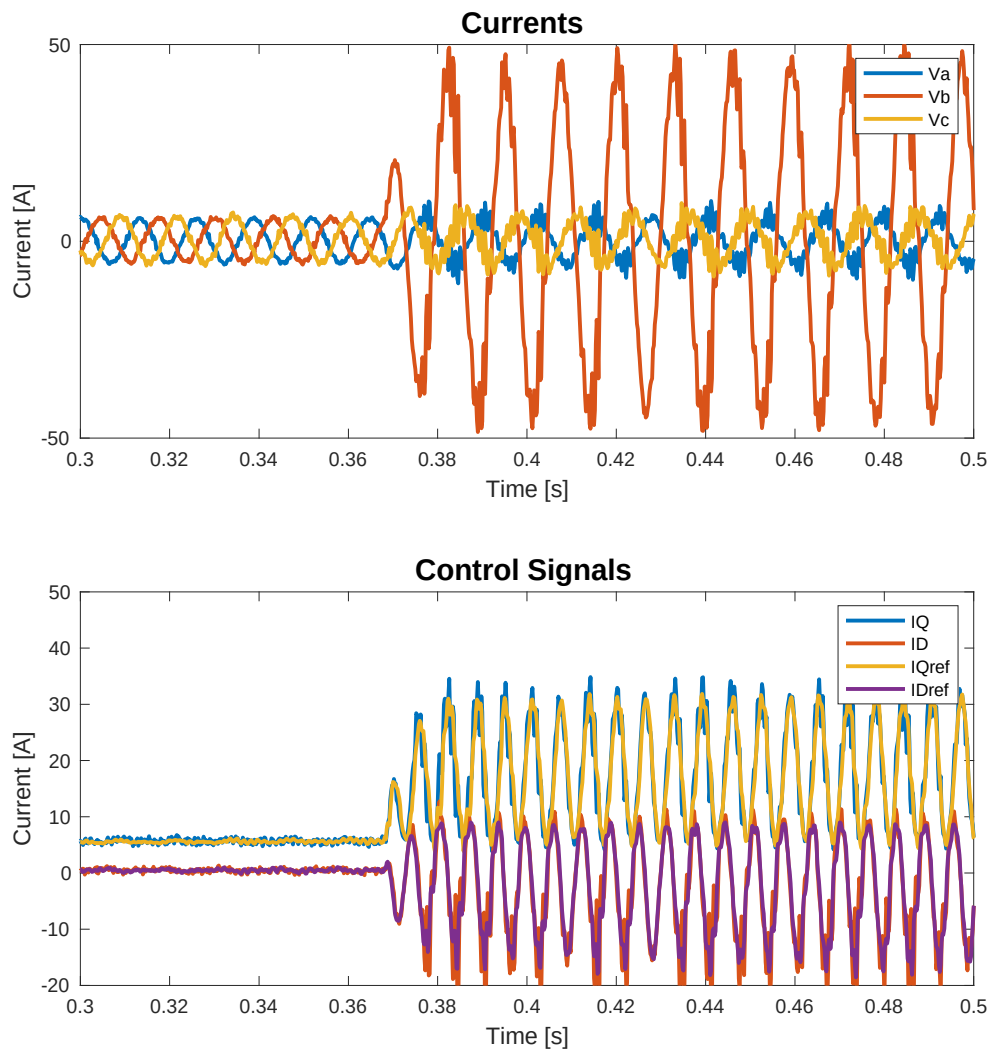
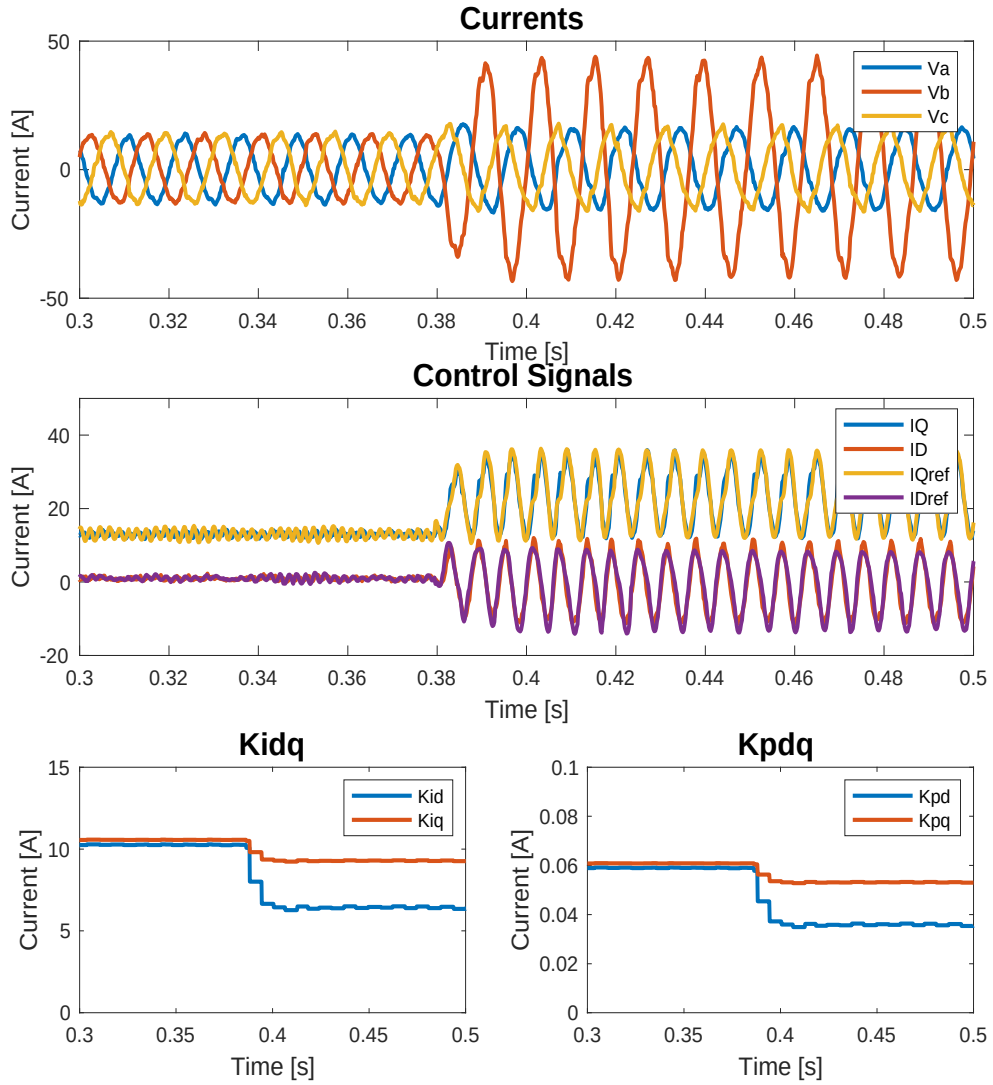


Figure 0.26: Experimental results. LG faults with conventional PI.



(b)

Figure 0.27: Experimental results. LG faults with proposed adaptive PI control.

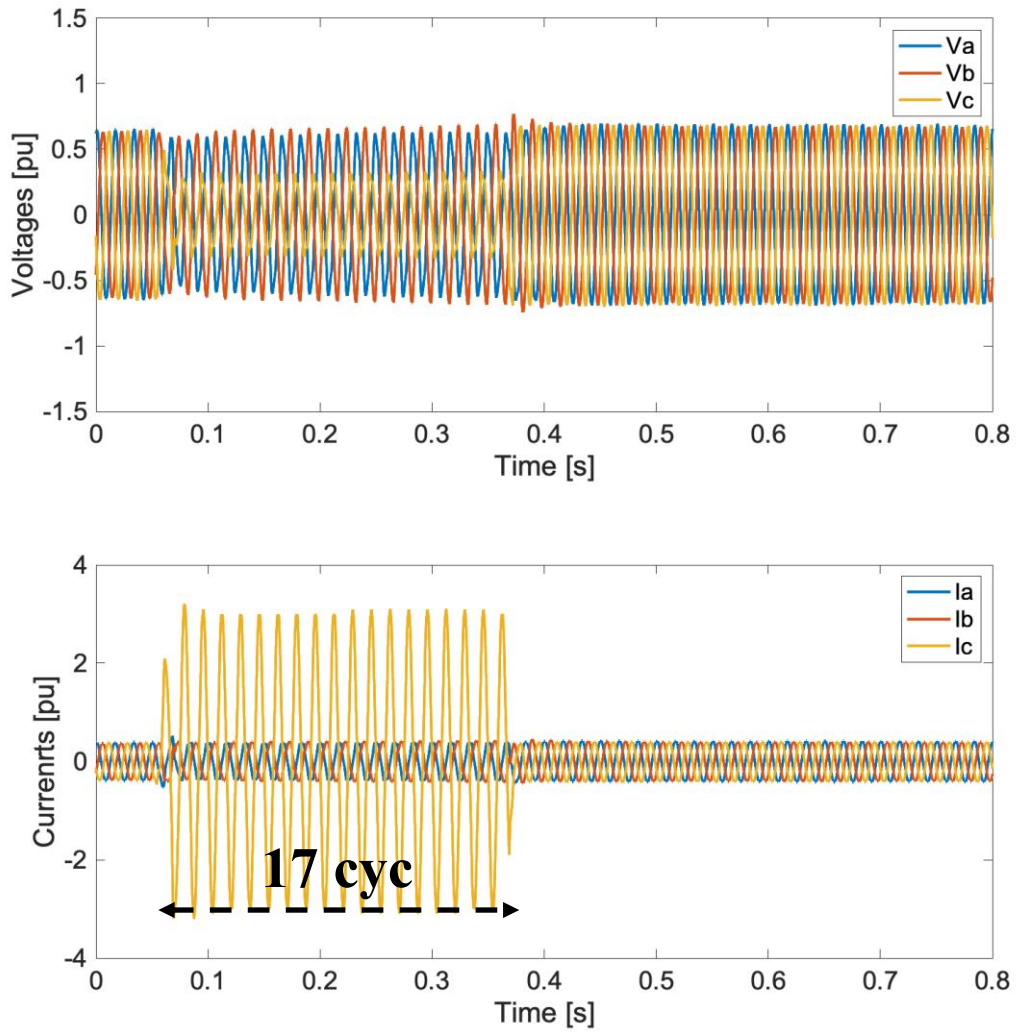


Figure 0.28: Fuse clearing times for line-to-ground faults.
Experimental results read from SEL 651 (128 samples).

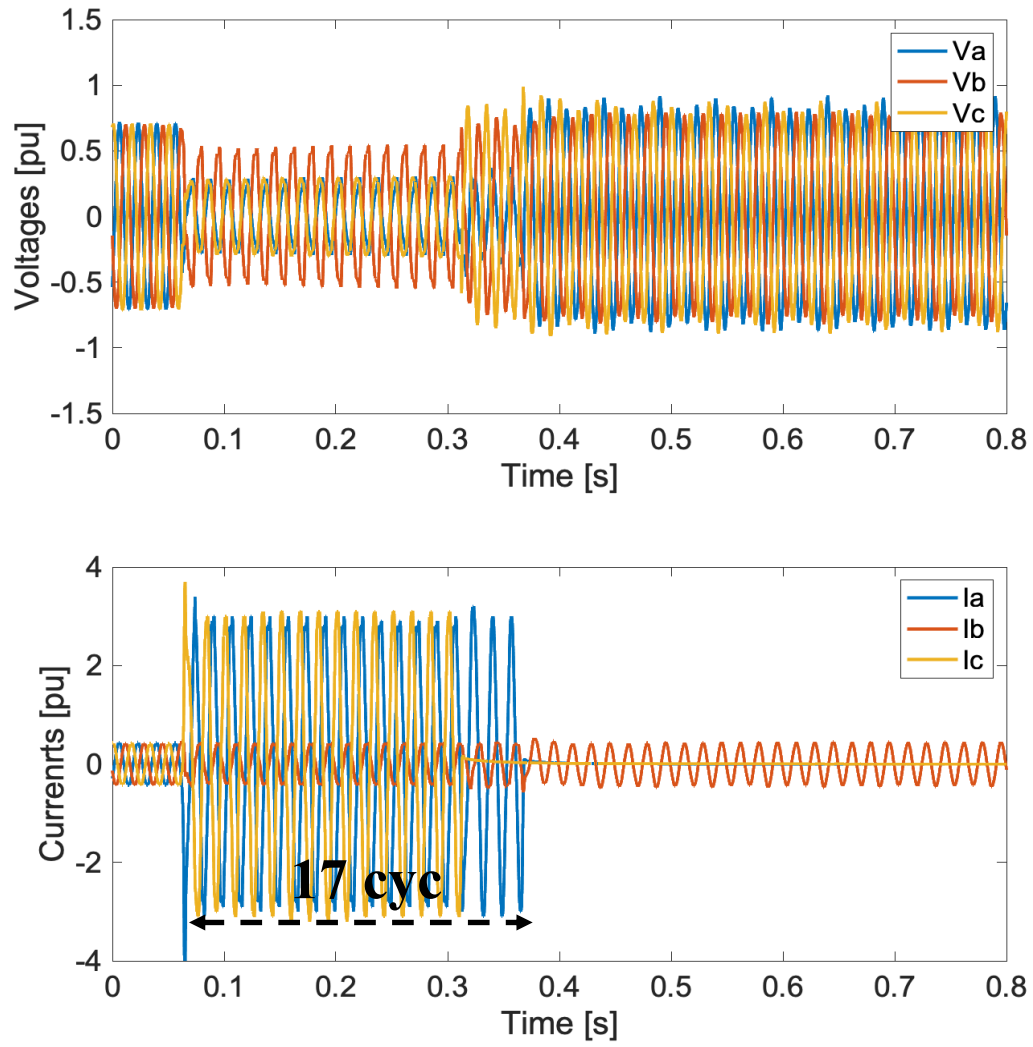


Figure 0.29: Fuse clearing times for line-to-line faults.
Experimental results read from SEL 651 (128 samples).

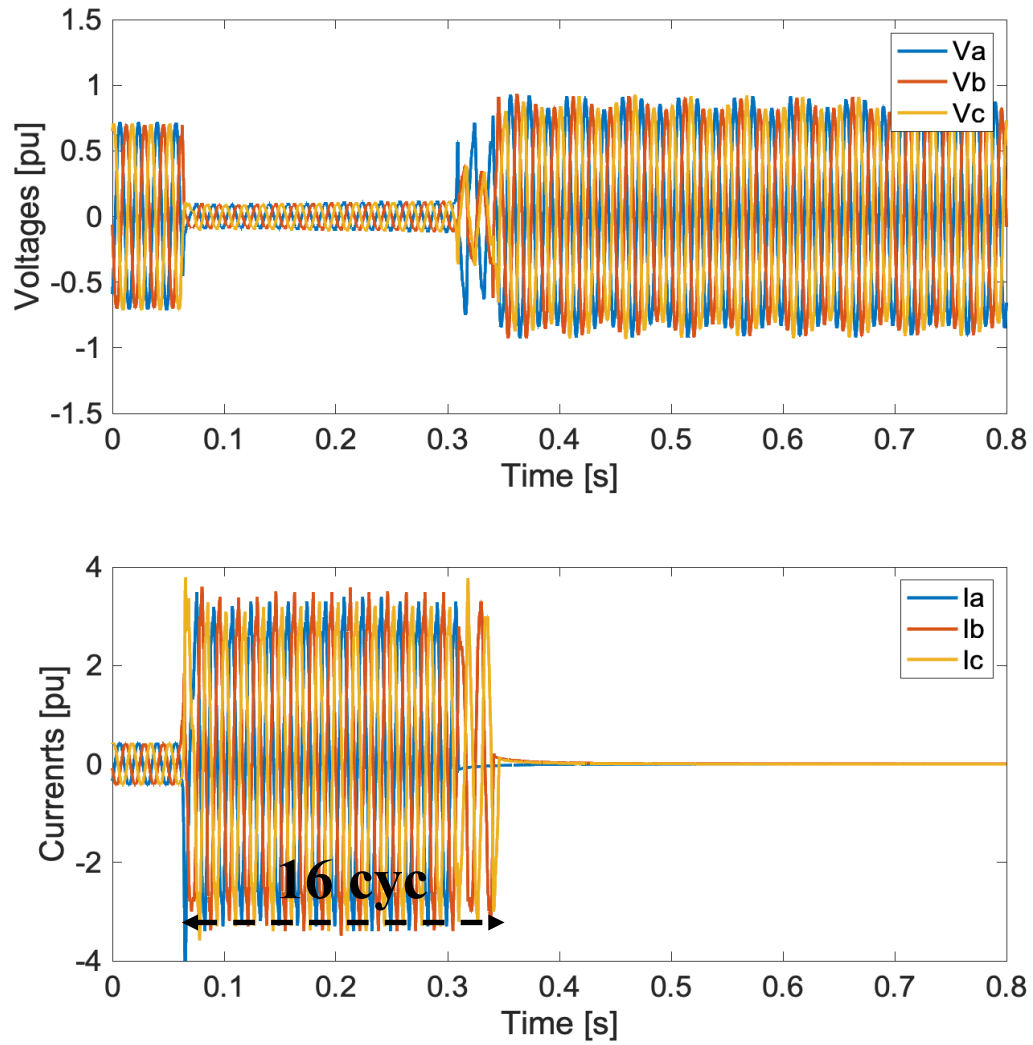


Figure 0.30: Fuse clearing times for 3-ph faults.
Experimental results read from SEL 651 (128 samples).

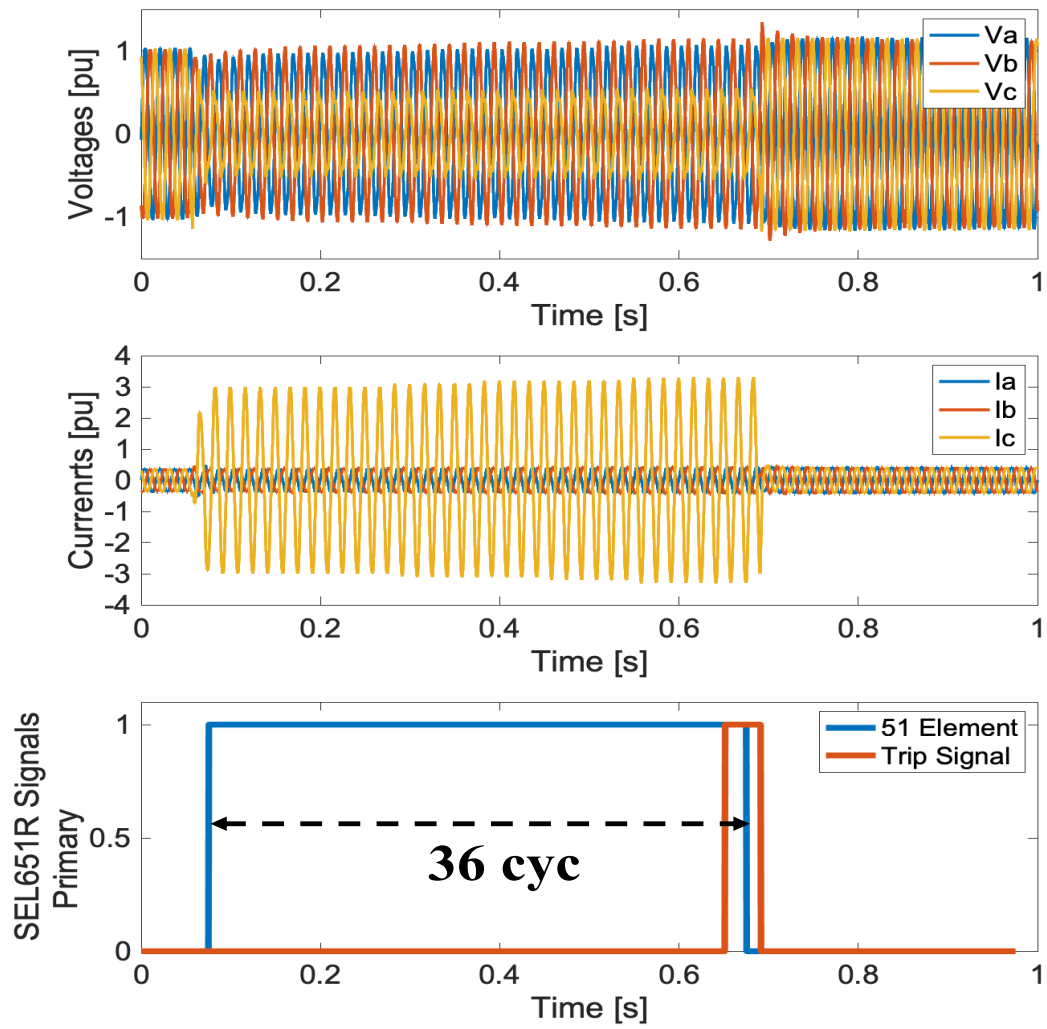


Figure 0.31: Primary relay clearing times for line-to-ground faults.
Experimental results read from SEL 651 (128 samples).

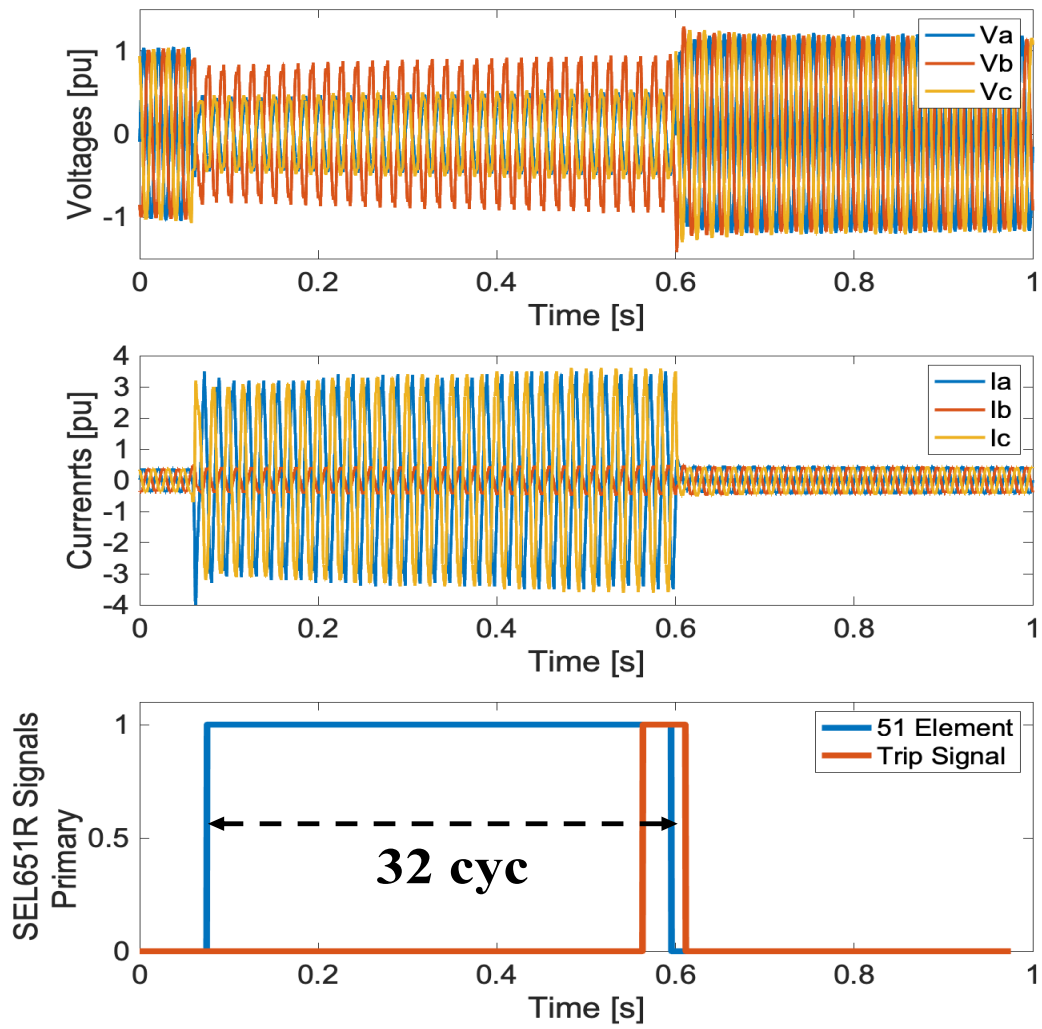


Figure 0.32: Primary relay clearing times for line-to-line faults.
Experimental results read from SEL 651 (128 samples).

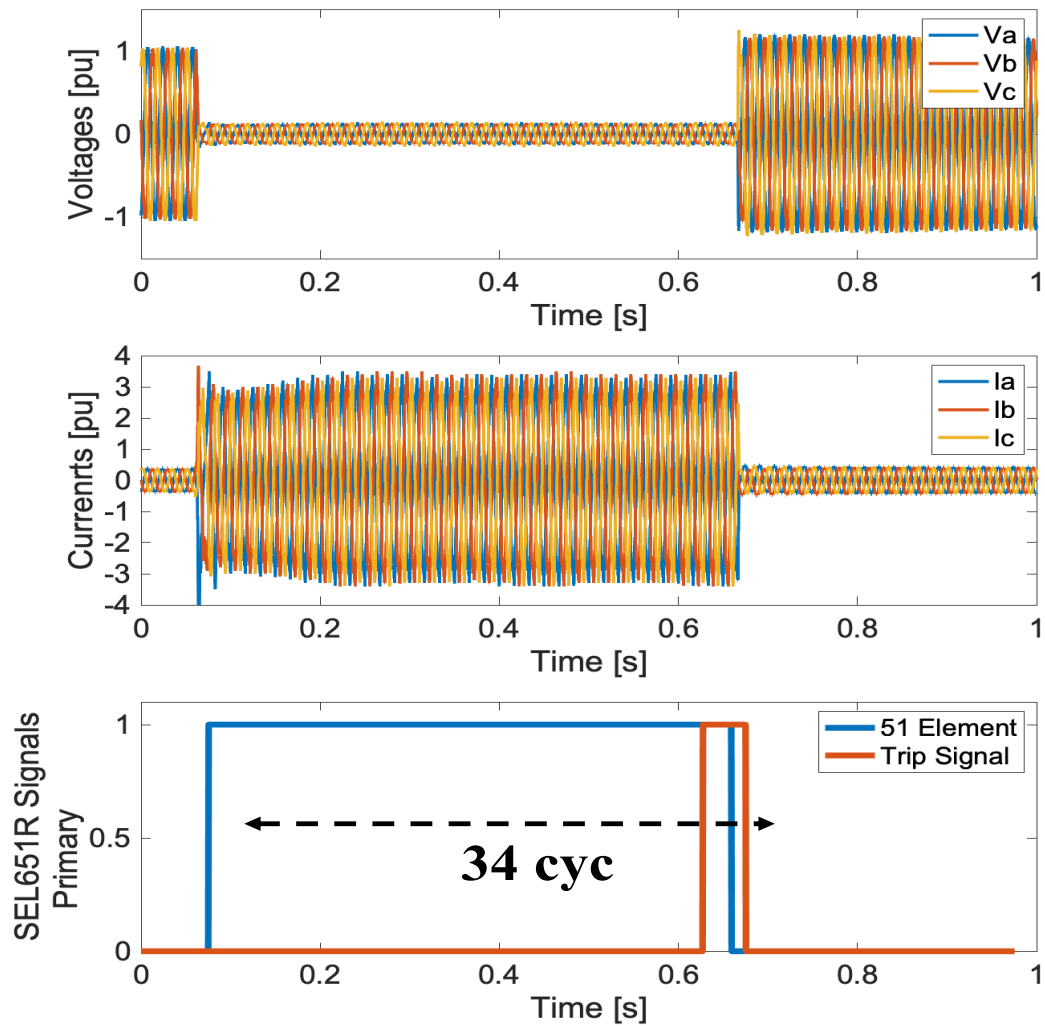


Figure 0.33: Primary relay clearing times for 3-ph faults.
Experimental results read from SEL 651 (128 samples).

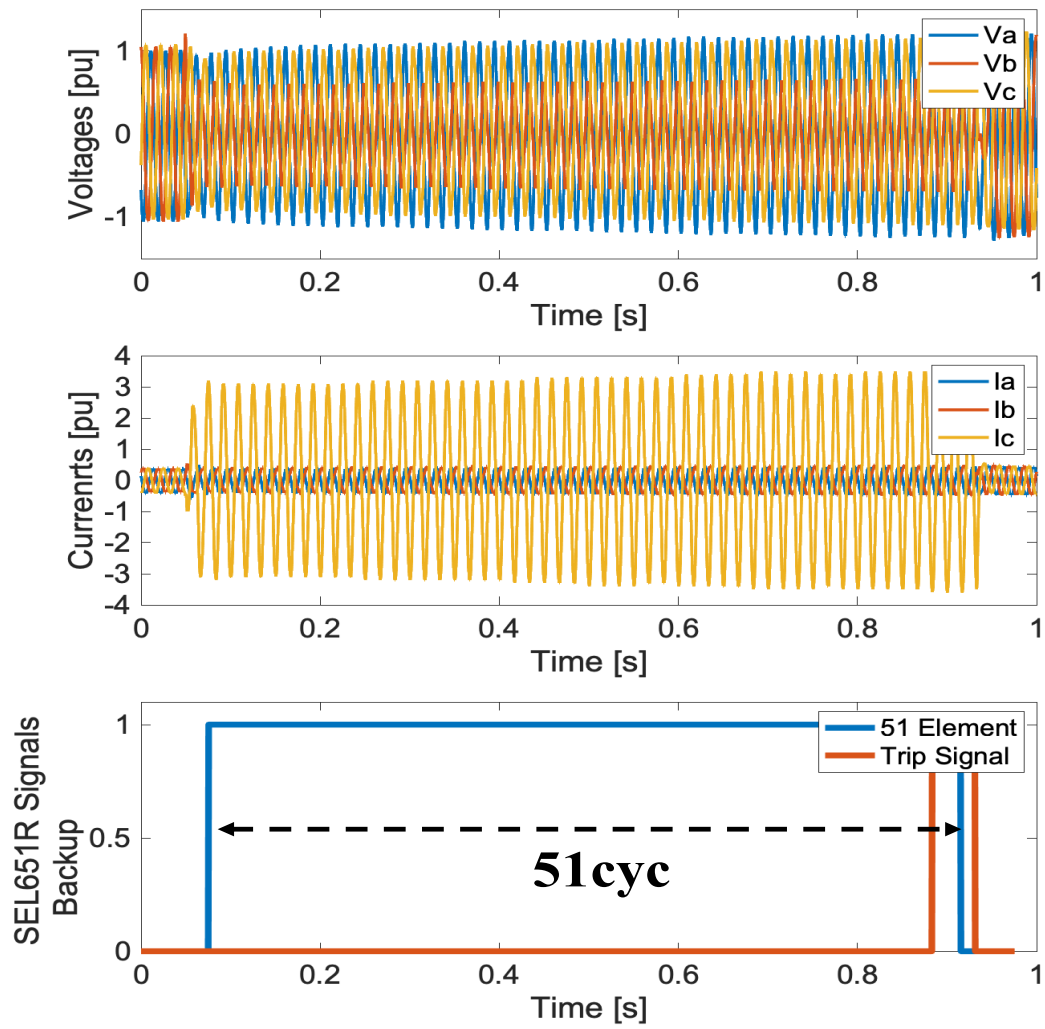


Figure 0.34: Backup relay clearing times for line-to-ground faults.
Experimental results read from SEL 651 (128 samples).

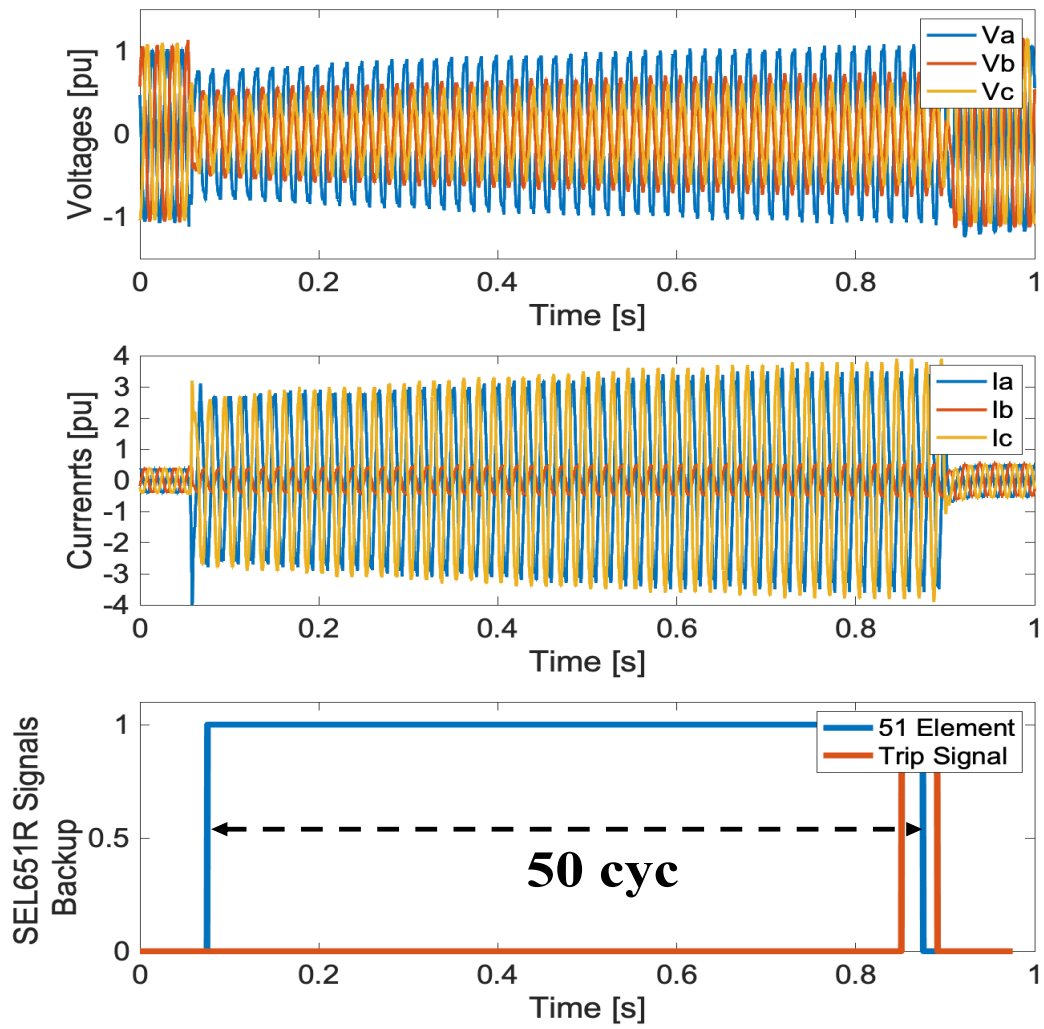


Figure 0.35: Backup relay clearing times for line-to-line faults.
Experimental results read from SEL 651 (128 samples).

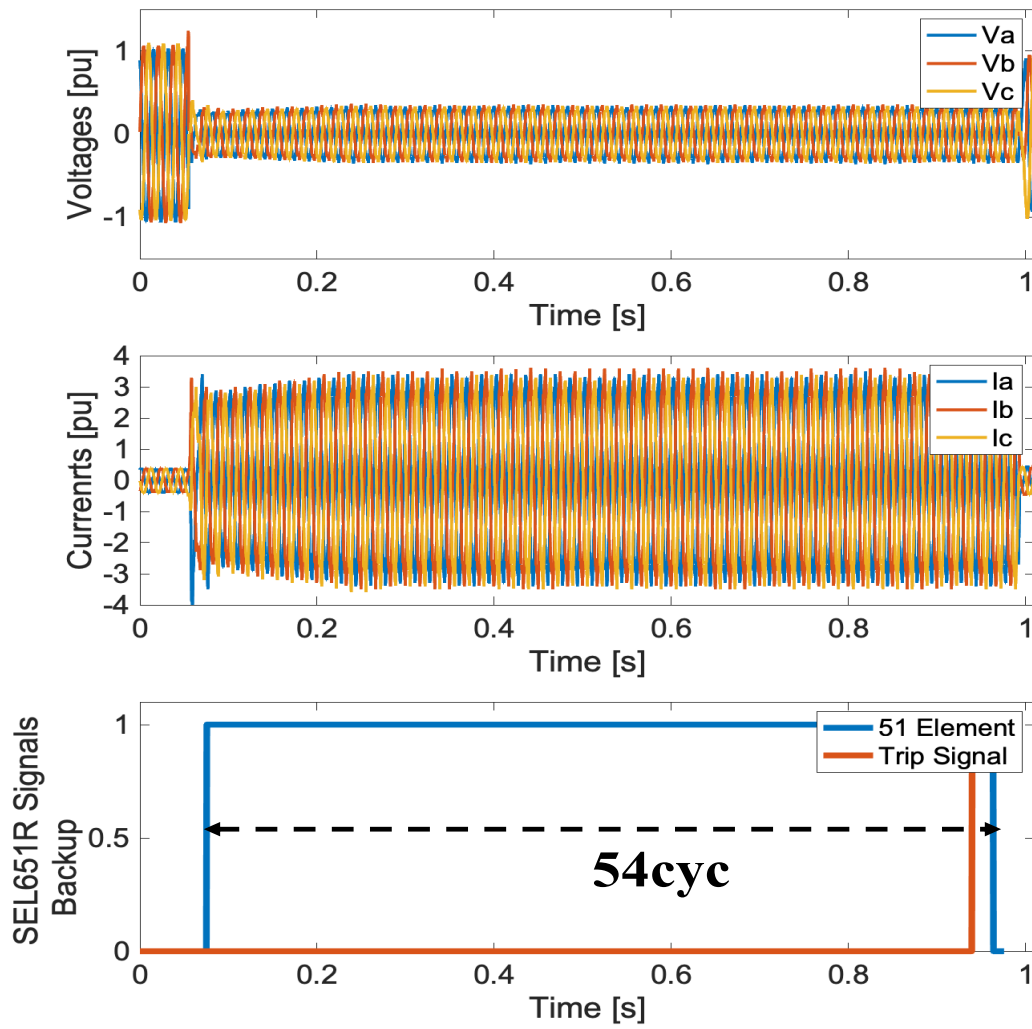


Figure 0.36: Backup relay clearing times for 3-ph faults.
Experimental results read from SEL 651 (128 samples).

Table 0.9
Tripping time for different short-circuit Magnitudes

Fault Current (p.u)	Fuse melting time (s)	Trip time primary relay (s)	Trip time backup relay(s)
1.25	>10	>10	>10
2.0	>10	>10	>10
3.0	0.26	0.56	0.9

Table 0.10
Coordination study

Fault Type	Fuse melting time (cycles) [a,b,c]	Trip time primary relay (cycles)	Trip time backup relay(cycles)
LG	[0,0,17]	36	51
LL	[17,0,14]	32	50
3-Phase	[15,16,16]	34	54

CHAPTER 2
MICROGRID PROTECTION CASE STUDY, ADAPTIVE RELAYING

Abstract: This chapter presents the application of the model-adaptive relay to protect a microgrid in islanded and grid-tied mode. The model-adaptive relay is designed to adjust the relay curves based on the available generation and the network topology. The proposed method runs a real-time model of the microgrid and gathers information from the network to calculate the available short-circuit current in the specified node. The fault current from the model is then used for the adaptive algorithm to calculate the relay settings, considering coordination with the downstream fuses and upstream reclosers. The model-adaptive relay was validated in Hardware-in-the-Loop (HIL), in a hardware testbed, and was deployed in at the Electric Power Board microgrid in East-Tennessee. Portions of this chapter has been previously published in [150].

2.1. Introduction

Adaptive protection is a promising technique that enables the use of overcurrent relays in microgrids. Adaptive protection can be defined as an online process which modifies the preferred protective responses and correlates them to a change in system conditions or requirements in a timely manner through control or signaling [9-10]. Table 1.3 in Chapter 1 showed a summary for the different approaches in Adaptive Relaying, which can be broadly categorized in centralized, decentralized, or hybrid approaches [10-14,31-34]. The central approach uses a central unit to monitor the state of the system and reconfigures the relays to adjust the tripping time. The decentralized approach utilizes local information, such as frequency and voltage, to identify the microgrid status and adapt the relay settings accordingly. Hybrid approaches use a central controller to identify large network modifications, and local information to identify loss of generation or islanded operation.

This work proposes a model-adaptive relay that continuously adapts the relay settings based on the network configuration and the available short-circuit current. The main novelty of the proposed model adaptive relay is that it continuously runs in real-time a short-circuit study to programmatically calculate the relay setting. The short-circuit study is based on the results obtained from a power system model which runs locally on a Field Programmable Gate Array (FPGA) in real time. The fault current from the model is then

used for the adaptive algorithm to calculate the relay settings, considering coordination with the downstream fuses and upstream reclosers. The power system model is updated through a communication network (DNP3 or Modbus) to capture the status of field devices, such as reclosers and online generators. This automatization simplifies the programming of the relays while also eliminating the need of multiple settings groups, which is typically four to seven in commercial protective devices. This methodology is scalable and can calculate the settings for complex networks with multiple Distributed Energy Resources (DERs) in the system. The proposed method was validated in Hardware-in-the-Loop, in a hardware testbed as well as field deployed in a real microgrid owned by EPB.

2.2. Control Center EPB microgrid

This section presents simulation results that showcase the challenges of implementing overcurrent protection schemes in inverter-based microgrids. A real microgrid located in Chattanooga, Tennessee is used as a case study to illustrate the challenges of microgrid protection using overcurrent elements. The Simulink model of the EPB microgrid is presented in Fig 2.1. The EPB microgrid operates at 12.47 kV and consists of 1.3 MW of PV generation and 1 MWh of energy storage. The PV farm consist of 22 Yaskawa 60T inverters; each has a power rating of 60 kW. Each Yaskawa 60T is composed of 3 maximum power point (MMPT) trackers, each of which has a maximum output current of 68 A. Its fault current contribution is 64 A, as specified in its datasheet [15]. A total of 22 Yaskawa 60T inverters are connected in parallel to a 480V/12.47kV transformer. The islanding operation is enabled by a 1 MWh Tesla Megapack, which regulates the voltage and frequency of the microgrid. The specifications of the inverter are not public, and it is assumed a 2.0 p.u. fault current can be provided by the battery storage inverters. The microgrid laterals are protected by Positrol® Fuse Links rated at 30 T, 50 T and 100 T amperes. Intellirupters are installed along the 12.47 kV distribution line, with one placed inside the microgrid. The intellirupters use directional overcurrent elements with inverter time overcurrent curves for detecting short-circuit faults in the forward and reverse directions. The Intellirupter in the microgrid has two setting groups, one for grid-tied operation and a more sensitive curve for islanded operation.

For this study the interest is in the 100T fuse, which requires a high fault current to start melting. Fig. 2.2 shows the TCC curves for the 100 A fuse, and the Intellirupter that protects the feeder. This Intellirupter protects the microgrid using two TCC profiles, one for grid tied and another for islanded operation. The TCC curve for the Intellirupter is U4 for both profiles. For the grid-tied operation, the pick-up current is 600 A with a time dial (TD) of 0.78. For islanded operation, the pickup current is 70 A with a TD=0.42. Because of the low short circuit fault from the IBRs, in island mode the Intellirupter was configured to trip before the fuse. Although this protection scheme will isolate the fault, tripping the Intellirupter leaves all the loads in the microgrid without power. To showcase the challenges of protecting a lateral power line with fuses in microgrids, a three-phase fault was introduced in lateral 25 which is protected by a 100 A fuse. During grid-tied application, the substation provides high fault current (2800 A), and the fault is quickly cleared by the fuse in less than 0.04 seconds. For grid-tied operation, the Intellirupter upstream provides backup protection. During islanded operation, the maximum combined fault contribution from the PV inverters and the energy storage is 144 A. Because of this low current, the 100 A fuse will not melt, as shown in Fig 2.2.

Fig. 2.3. Shows the simulated current waveforms from the ES and PV inverters when a three-phase fault is introduced at $t=0.25$ s in the lateral 25. As seen in the figure, the three-phase fault causes an immediate current pulse of short duration which is caused by the passive inductive loads in the microgrid. The short-circuit surge decays in less than $40\text{ }\mu\text{s}$ and has no significant energy to be useful for protection purposes. During the fault, the current control of the PV inverter regulates the current to be 1 p.u, which is set by the saturation of the dc link control loop. During the fault, the grid forming inverter is unable to regulate the voltage, and the voltage controller saturates to 2.0 p.u in 0.2 seconds following the integration of the error. Notice that the irradiance has a small effect on the available fault contribution from the PV. For very low irradiance (less than 50 W/m^2), the fault contribution of the 1.3 MW farm is 110 A. For a sunny day ($>500\text{ W/m}^2$), the fault contribution increases to 144 A.

2.3. Model Adaptive Relay

The adaptive relay has multiple building blocks which are shown in Fig. 2.4. The main modules of the model-adaptive relay are 1) real-time power system simulator, 2) communication module, 3) short-circuit analysis module, and 4) relay module. All these modules run on a single Kynthex-7 FPGA included in the NI-CRIO 9039. The real time model is updated to reflect the status of the Point of Common Coupling (PCC) switch of the microgrid, configuring the model to operate as grid tied or islanded mode. The PCC status can be obtained through a DNP3 register in the Intellirupter. This register was set by the EPB. The power system model runs the following models in real time on LabVIEW FPGA: 1) PV inverter, including controls and average model of the power converter, 2) physics-based model of PV farm, 3) Impedance LR line sections. The substation is modelled as a three-phase grid in series with an LR section. The LabVIEW Code for the model-adaptive relay is included in the Appendix.

The equations of the three-phase PV inverter with connection to the grid, with the average state model and the external elements of the circuit are given by equations (2.1) and (2.2).

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc} \quad (2.1)$$

$$\frac{d}{dt} v_{dc} = \frac{1}{C} (I_{DCPV} - I_{DC}) \quad (2.2)$$

Where i_{abc} are the inverter output currents, v_{abc} the voltage at the point of connection, d_{abc} the duty cycle, L and R the grid filter inductance and resistance, v_{dc} the DC-link voltage I_{DCPV} the PV panel output current and I_{DC} the inverter DC current. The control for the PV inverter is designed using (2.3).

$$\frac{\tilde{i}_{dq}}{\tilde{d}_{dq}} = \frac{V_{dc}}{(sL_{dq} + r)} \quad (2.3)$$

SUBSTATION 46 kV/12.47kV

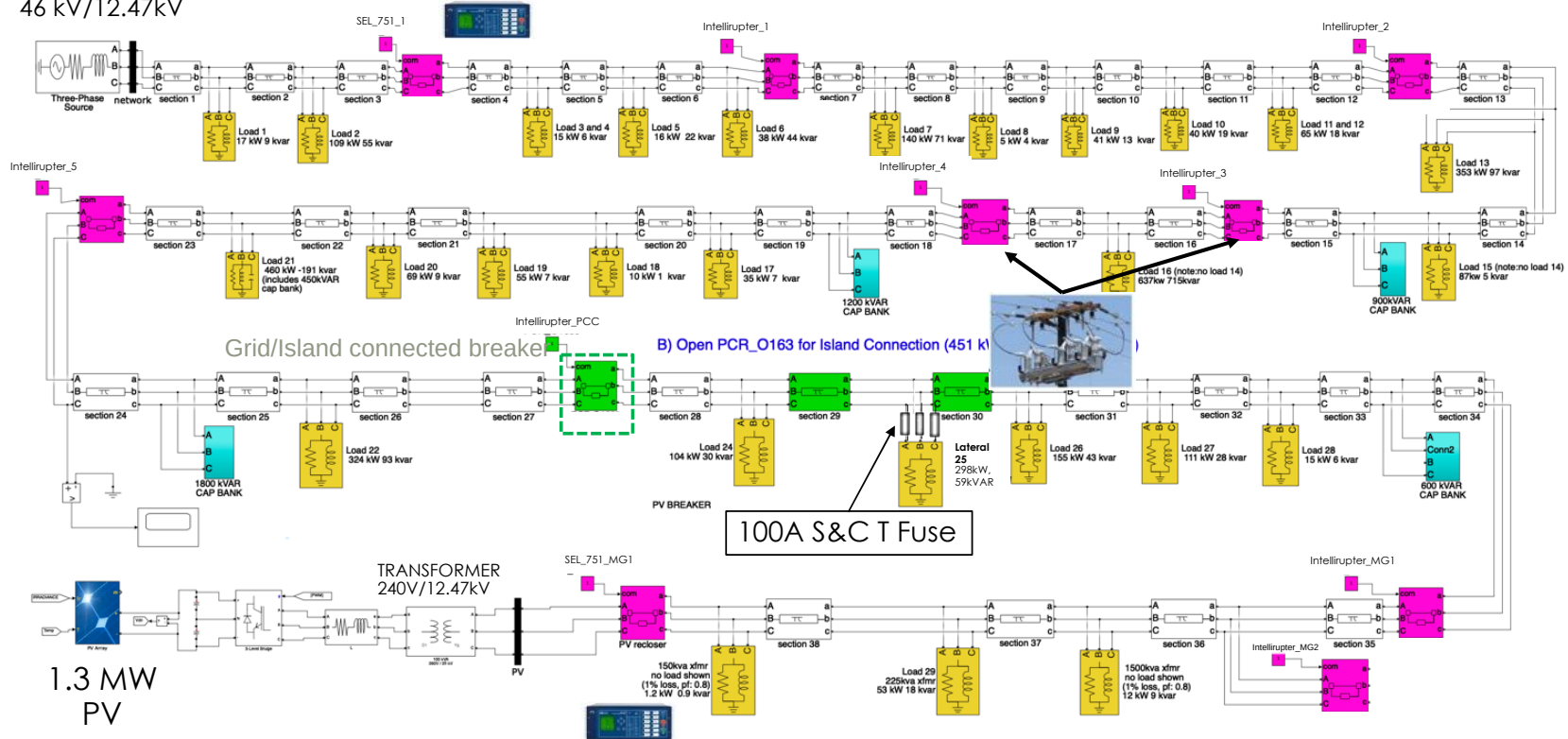


Figure 2.1: EPBs distribution feeder including Riverside substation and control center microgrid. Green dashed line encloses the microgrid.

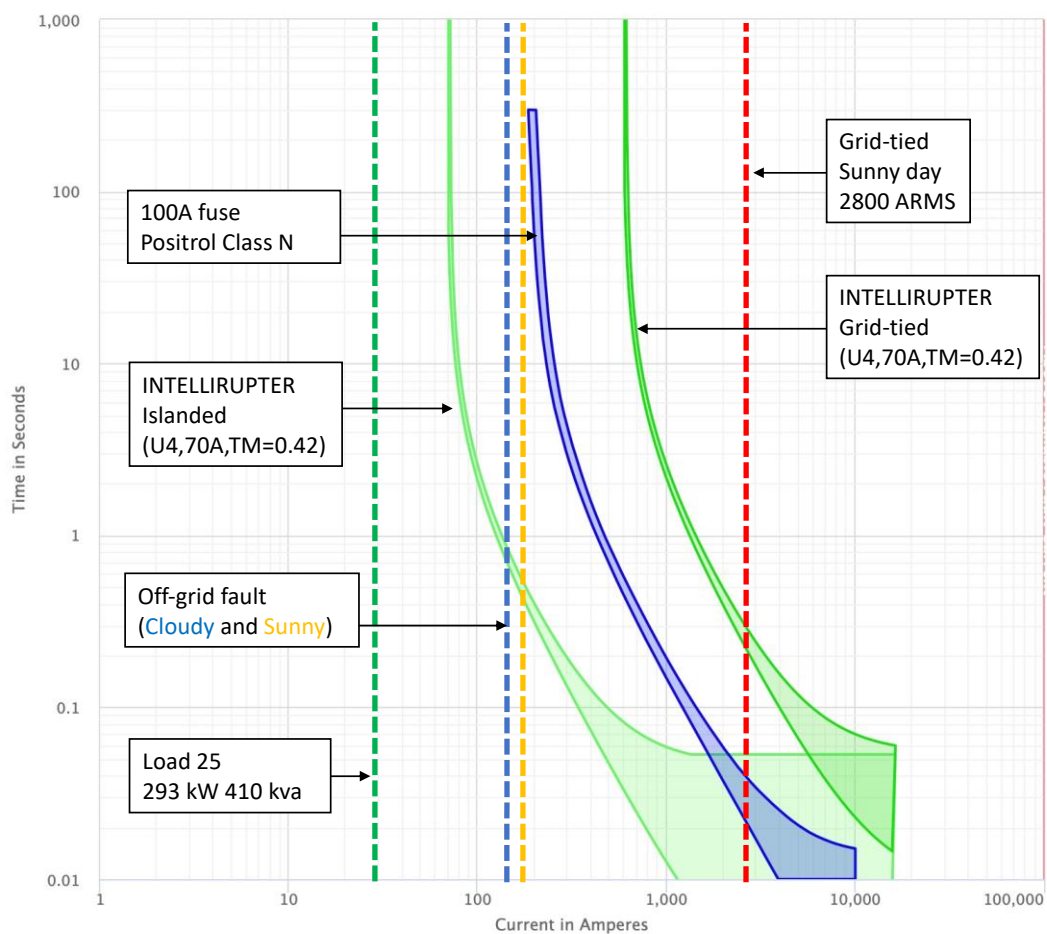


Figure 2.2: TCC curves for S&C Interllirupter and 100A S&C Positrol fuse.

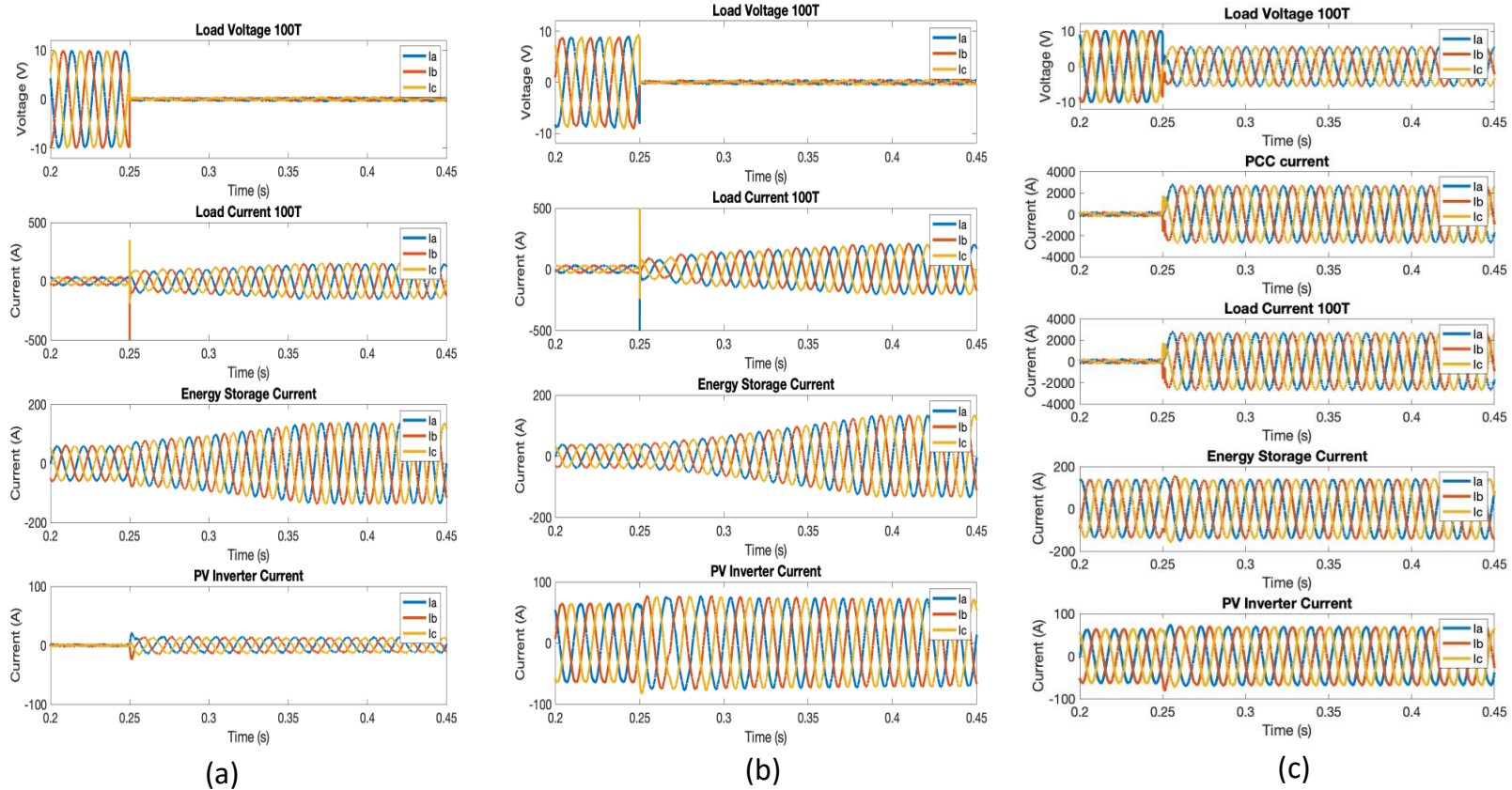


Figure 2.3: (a) Islanded mode low-irradiance day. (b) Islanded mode high irradiance. (c) Grid-tied high-irradiance.

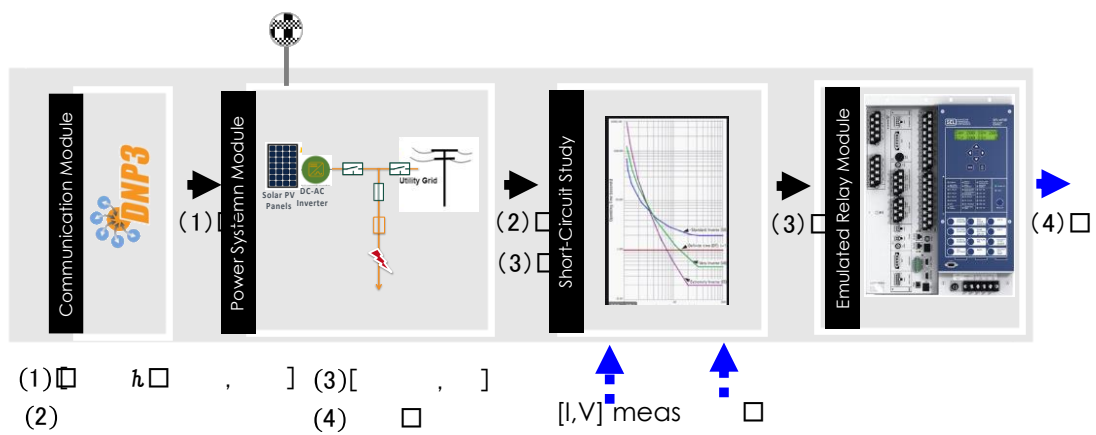


Figure 2.4: Model adaptive relay Modules

A resistive-inductive (LR) line section was programmed to account for the impedance between the substation and the PCC. The LR section has as an input the voltage at the input terminal of the inductor V_{Lin} , the current through the inductor I_L , the inductance resistance r_L , and the inductance L in Henries. The output voltage is calculated through (2.4):

$$V_{out} = V_{Lin} - r_L I_L - \frac{dI_L}{dt} L \quad (2.4)$$

To estimate the generation from the 1.3MW PV farm a physics-based PV array model was programmed, this model described by the following equations,

$$I_{PV} = \left(I - I_0 \left[\exp \left(\frac{V + R_s I}{V_t a} \right) - 1 \right] - \frac{V + R_s I}{R_p} \right) \quad (2.5)$$

where I is the current generated by the incident light, I_0 is the saturation current of the array, $V = N_s kT / q$ is the thermal voltage of the array with N_s cells connected in series. If the array is composed of N_p parallel connections of cells, the photovoltaic and saturation currents may be expressed as: $I = I_{cell} N_p$, $I_0 = I_0 N_p$. R_s is the equivalent series resistance of the array, and R_p is the equivalent parallel resistance [53].

The last block is the short-circuit module, which adapts the tripping time based on the user preference. This module receives short-circuit current from the power system module and the instantaneous load from the communication module. The pickup is calculated by multiplying the load by a constant σ . To maintain coordination, the adaptive relay receives the trip time at the available fault current from the upstream recloser and downstream fuses.

Finally, the user specifies the desired trip time for the relay $t(s)$. This information is fed into (2.6), which is the IEC TCC curve, which is used to calculate the Time Multiplier Setting (TMS).

The TMS and pickup are the settings to be programmed in the relay to determine the TCC

curve. The protection philosophy is to guarantee the user specified trip time regardless of the available short-circuit current.

$$TMS = \frac{t(s) \left(\left(\frac{I}{\sigma I_{load}} \right)^\alpha - 1 \right)}{k} \quad (2.6)$$

where σ is set to 1.25, $\alpha=2$ and $k=80$ to represent the IEC extremely inverse curve.

2.4. Experimental Results

Fig. 2.5 shows the TCC curves for the upstream and downstream fuses protecting a line lateral, as well as the curves calculated by the model-adaptive relay. Two fault current contributions are evaluated (144 A and 300 A), and for two pickup currents 50 A and 70 A. The 144 A current is the fault current during islanded mode on a sunny day. The 300 A is the contribution when the diesel backup generator is online. The pickup reflects changes in the load during the day. For this example, the user established a trip time of 0.8 s. This information is used together with the available fault current and the pickup to calculate the TMS. The grading time to maintain fuse-relay coordination is set to 0.3 s. As seen in the figure, the model adaptive relay adjusts the TCC curves based on the available generation and load in the lateral. Regardless of the generation, the trip time for all cases is 0.8 s. Notice that for the grid-tied operation, the adaptive relay is programed as a fuse-blow scheme.

Fig. 2.6 shows the hardware and HIL testbed used to test the model-adaptive relay [54-55]. The HIL consists of an Opal-RT 4510 running the full microgrid model. The hardware setup, shown in the same figure, consists of a low voltage testbed that incorporates power hardware-in-the-loops models to emulate PV inverters, diesel generators, energy storage devices, and wind turbines. The hardware testbed is a platform that allows the integration of real protective devices, low-power inverters, loads and line sections. This testbed includes line impedances boards to emulate line sections between the microgrid and the substation. Fig. 2.7. shows one of these line-sections, where each one has impedance of $L = 345 \mu H$ and $R_L = 27.0 m\Omega$, ($X/R = 5$), and it is used to represent the physical

impedance between the laterals in the microgrid and the impedance from the PCC to the substation. The impedance boards limit the current from the grid which is important when performing protection studies. The impedances are scaled down to represent in per unit the real microgrid system using the p.u. transformations presented in [56-57]. Fig. 2.7(b) shows the model validation of the LR lines (2.4) against physical measurements. For this validation (2.4) was implemented to run in real-time in an CRIO 9039 and the *abc* currents are compared against measurements in real-time. A fault in the physical and virtual system was introduced and compared. As shown, good agreement between the model and measurements was obtained.

Fig. 2.8(a, b) shows the Hardware in the Loop (HIL), and Fig. 2.8(c, d) shows the experimental results for the model-adaptive relay when operating in islanding and grid tied modes. These graphs include the *dq* control signals of the PV inverter and the DC-link voltage response during the fault. In Fig. 2.8(a) a three-phase fault was applied in the HIL platform at $t=5.0$ s during islanded operation. Running in the background, the adaptive relay receives the status of the PCC switch and based on the available generation, determines the settings of the relay. For this test, the available fault current is 144 A and the breaker trips in 0.8 s, as specified by the user. Fig. 2.8(c) shows the same three phase fault applied in the hardware testbed. Notice that control signals of the PV inverter have similar dynamics to that in simulation. Similarly, the breaker tripped in 0.8 s. Fig. 2.8(b) shows the HIL results when the microgrid is grid-tied. For this experiment, the model-adaptive relay changes to a fuse-blow scheme and the trip time corresponds to the fuse protecting the lateral as the grid provides a large fault contribution and the 50T fuse clears after just 0.02 s. Fig. 2.8(d) shows the results obtained from the hardware testbed. Because the grid emulator in the hardware testbed has a thermal limitation, the available fault current is limited. During grid tied operation, the fuse takes more time to blow and finally opens in 0.16 s. For this case the model-adaptive relay was also set in the fuse-blow scheme.

Fig. 2.9(a) shows the field deployment package of the model-adaptive relay. The package consists of 1) CRIO 9039, 2) uninterruptible power supply. 3) industrial computer, which is the gateway for remote access. 4) G&W Rogowski coils which provide the current

measurements and voltage measurements for the model-adaptive relay. The model-adaptive relay was deployed at EPB's microgrid in Chattanooga. The model adaptive was mounted on a commercial utility pole located next to the 1.3 MG solar farm.

Fig. 2.9 (b) shows a 3D aerial representation of the model adaptive relay installation. The adaptive relay works in observation mode, which means that it receives real power system signals from the sensors, but it does not have any control of the distribution protective relay.

2.5. Conclusion

The experiments with the model-adaptive relay showed that a lateral in an inverter-based microgrid could be protected using the overcurrent principle. The presented model-adaptive relay is composed of a real-time power system simulator, a communication module, and a short-circuit analysis module, which continuously run to programmatically adjust the TCC curves in the relay.

This automatization simplifies the programming of the relays while also eliminating the need of multiple settings groups. This methodology is scalable and can calculate the settings for complex networks with multiple distributed DERs in the system. It was demonstrated through experimental and hardware-in-the-loop results, that the proposed model-adaptive relay effectively protected the laterals against short-circuit faults in the microgrid during islanded operation. In this section, a lateral protected with a 50 A fuse was instead protected with the model-adaptive relay. As shown, the model-adaptive relay enables use of overcurrent protection in microgrids. However, this method is not immune to the low short-circuit currents provided by IBRs. For instance, to protect a lateral with the 100 A fuse, it would need at least 200-300 A of short-current current, which is not achievable with the commercial IBRs installed in the microgrid, which limit their current to 1.2 p.u. Other limitations of adaptive relaying are that its reliability relies on a reliable communication network.

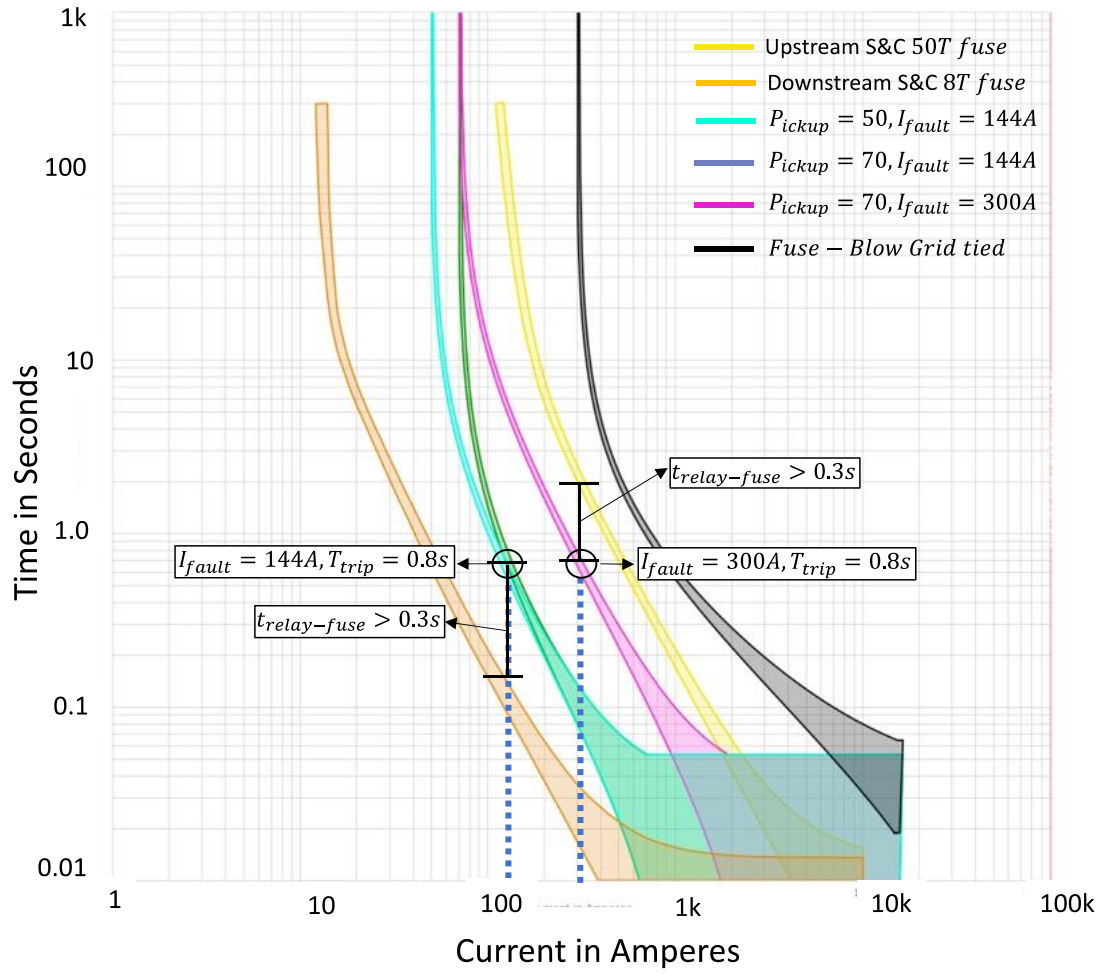


Figure 2.5: TCC curves for adaptive relay and S&C 100A Positrol fuse.

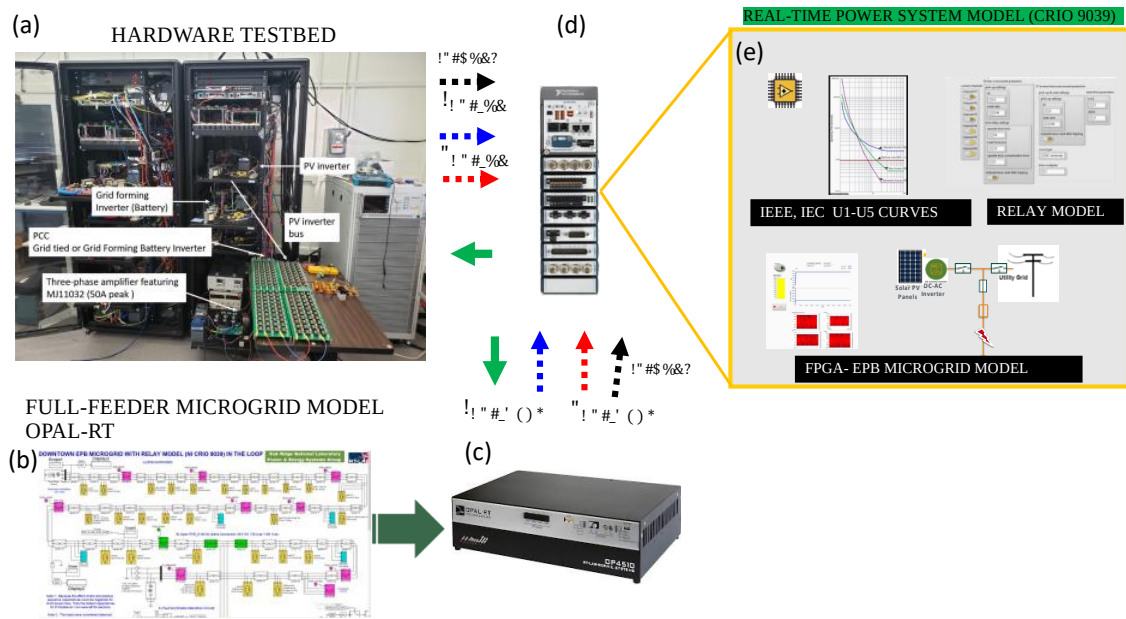


Figure 2.6: Laboratory testing and field deployment of the model-adaptive relay (a) hardware testbed. (b) EPB Microgrid model, RT-Lab (c) OPAL-RT 4510 (d) CRIO 9039 (e) FPGA models

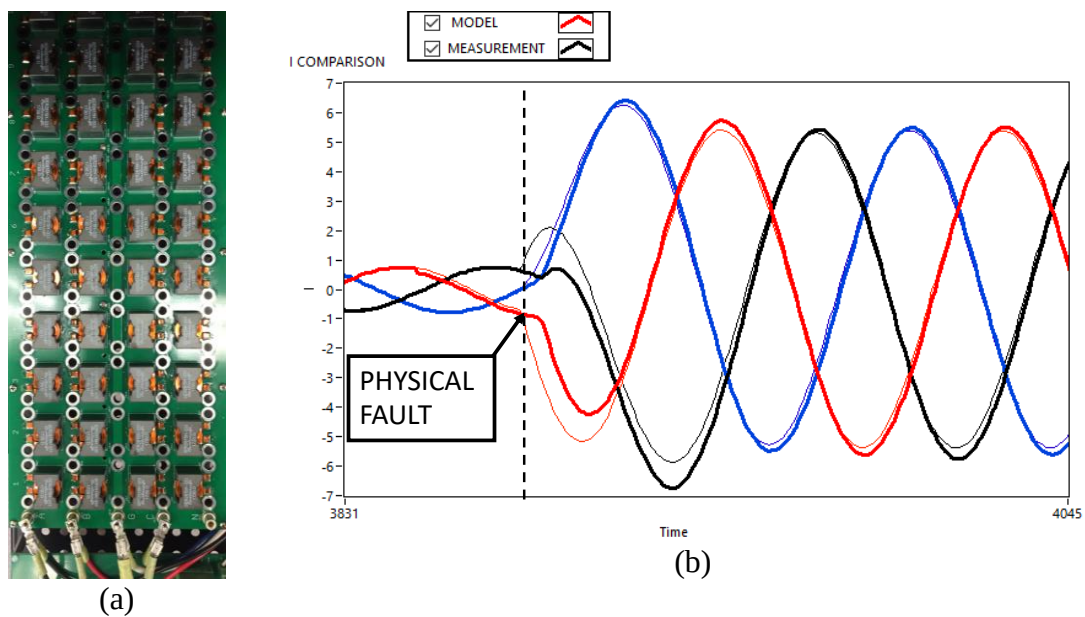


Figure 2.7: (a) line-impedance boards, (b) validation of Eq. (2.4) against measurements from impedance board.

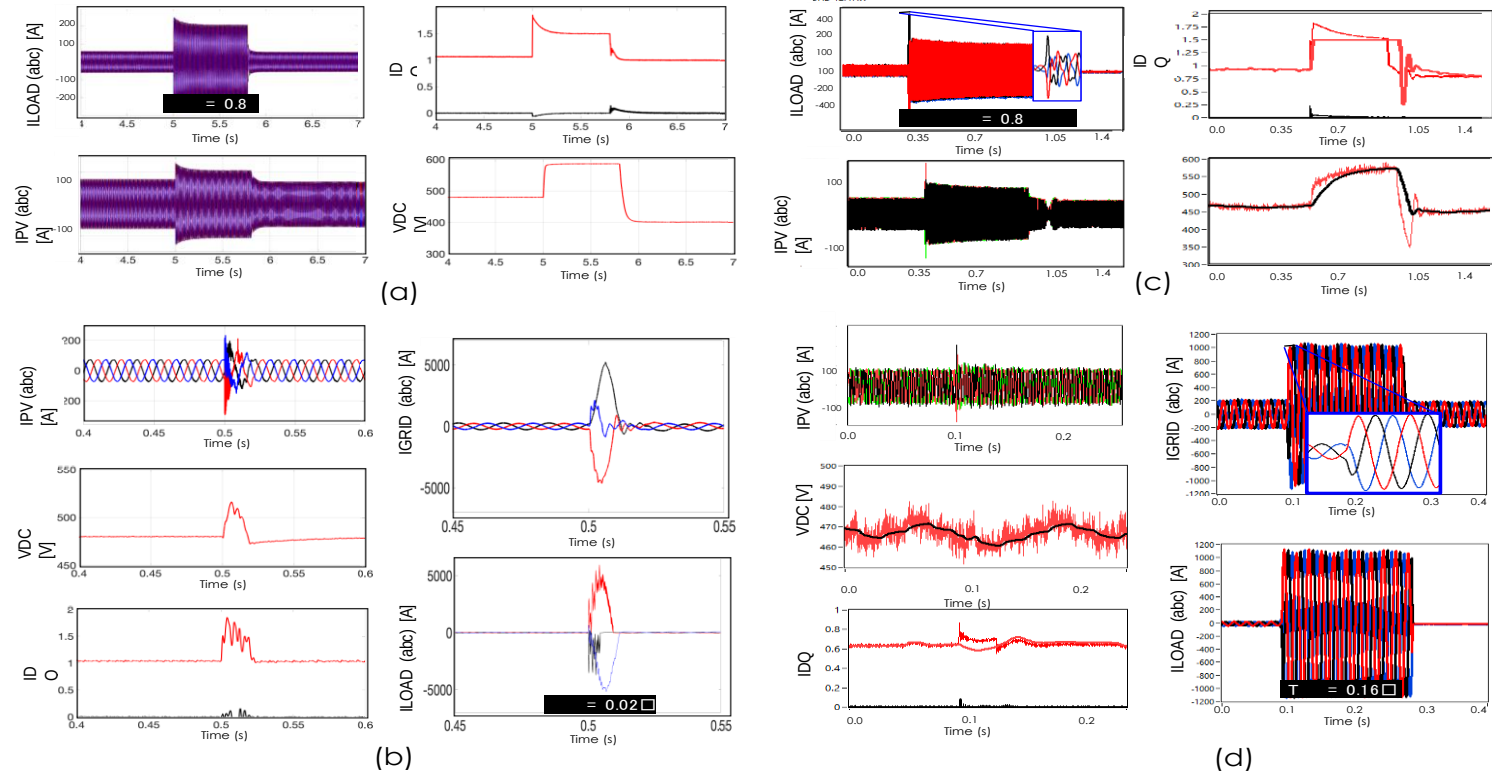
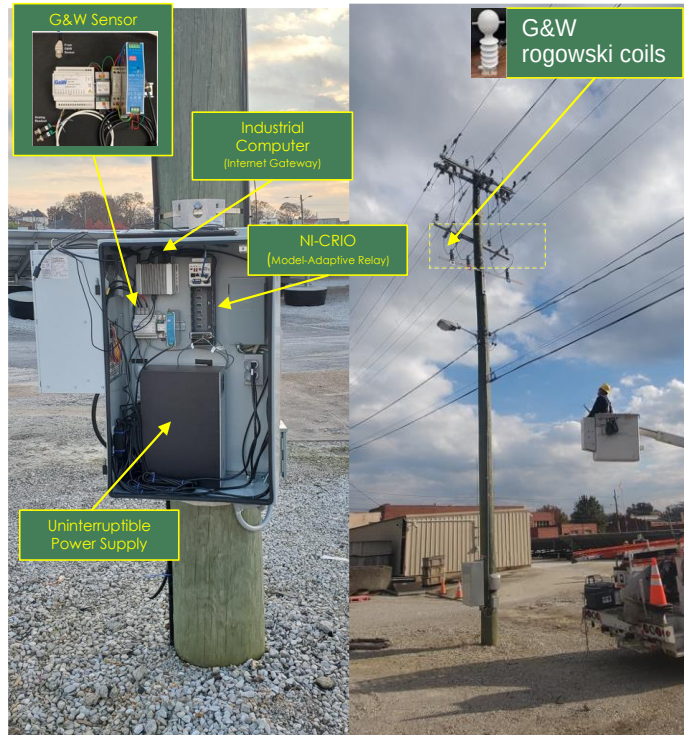


Figure 2.8: Laboratory testing of the model-adaptive relay, 3-phase fault, and tripping time for. (a) Island mode tested in HIL, (b) grid tied tested in HIL, (c) Island hardware results, (d) grid tied hardware results.

MODEL-ADAPTIVE RELAY FIELD DEPLOYMENT PACKAGE



(a)

3D VIEW OF MICROGRID LOCATION



(b)

Figure 2.9: Field deployment package at EPB control center microgrid. (a) field deployment package, consisting of CRIO 9039, uninterruptible power supply, industrial computer, and G&W Rogowski coils which provide the current measurements and voltage measurements for the model-adaptive relay. (b) EPB control central microgrid with commissioned model-adaptive relay.

CHAPTER 3
**DEVELOPMENT OF THREE-PHASE AMPLIFIER TO INTERFACE REAL-
TIME SIMULATORS WITH RELAYS IN THE LOOP**

Abstract: This section presents a prototype of a simple and cost-effective design using a high-power monolithic power amplifier that allows the relay in-the-loop connectivity for protection and control applications using a real-time simulator. This low-cost amplifier interface increases the number of protective relays in-the-loop connected with the real-time simulator, expanding the scalability of protection devices that could be tested. The amplifier control design was developed in *abc* coordinates and utilizes integral and proportional-resonant controllers to provide a good tracking of both the fundamental component as the dc component that might be present during fault conditions. To validate the prototype, the current signals and tripping time of a relay interfaced with the current amplifier were compared against a reference relay connected to the low-voltage interface. Both protective relays were set with a U3 Very Inverse time overcurrent curve. The experimental results exhibited similar behaviours for the breaker currents, validating the amplifier interface prototype. Portions of this chapter have been previously published in [151].

3.1. Introduction

This section presents the control design and hardware verification of a three-phase current amplifier used for testing relay protection systems with real-time simulators. The amplifier control is designed to represent virtually any type of fault and operating condition in a power system, including transients in line to ground, line to line and three-phase faults. The designed prototype provides a maximum current of 10 A maintaining low current distortion. This current is sufficient to test a variety of protective devices, including relays and reclosers. To evaluate the performance of the control and current amplifier, a simple simulation of a line to ground fault was developed and executed on an OP4510 real-time simulator. The relay (SEL-451) under test was set and interfaced with the proposed current amplifier through the relay's secondary voltage/current connectors (usually connected to current and potential transformers). This experiment was validated by comparing the record events generated by the SEL-451 relays connected to the proposed current amplifier with the results obtained from another SEL-451 relay connected to the low-level interface.

Real-time simulator and hardware-in-the-loop testing of protective relays have been widely addressed in previous literature [58-64]. The published literature utilizes proprietary power amplifiers [58-61] or relay's low-level interface [63-64]. For instance, [63-64] investigate the behavior of adaptive protection schemes in relays interfacing the real-time simulated analog signals through the relay's low-level interface by using voltage and current gains in their real-time power system models. The voltage and current gains were calculated by using the scaling factors collected from relay's instruction manuals and using the ratios of current and potential transformers [63-64]. Other authors [58-62] achieve the amplification of the low-level current output from the real-time simulator using proprietary current amplifiers, that results in an expensive alternative for the real-time simulator testbeds, particularly when more than one protective device needs to be connected in-the-loop.

The literature regarding current amplifier for testing relays is divided into linear amplifiers [68], Pulse Width Modulation (PWM) converters [69][70], and hybrid topologies [69]-[70]. The current amplifier presented in this chapter is the first prototype of a three-phase current amplifier that uses the high-power amplifier OPA541. This amplifier uses a class AB amplifier and was chosen for this application because of its high current output, low-cost, low current distortion and reduced size when compared to PWM converter that required bulky passive filters.

The contribution of this section is the complete design of a low-cost, low-distortion three-phase current amplifier that increases the number of protective relays that can be connected in the loop with real-time simulators. This article addresses the experimental verification for various faults present in power systems as well the relay in-the-loop validation. The proposed three-phase current controlled amplifier is an effective way of testing complex protection schemes that require large numbers of protective relays in-the-loop connected to the real-time simulator.

3.2. Materials and Methods

3.2.1. Testbed

The validation of this proposed amplifier interface was validated at a testbed shown in Fig. 3.1. The low-level and amplifier interface was connected to an OP4510 real-time simulator.

The experimental method was based on comparing the low-level and amplifier interfaces with SEL-451 relays in-the-loop. The low-level and secondary phase currents were connected to the low-level (relay's front side) and high-level (relay's backside) inputs, respectively. The simulation of the whole power system in real-time during the relay tests was performed by integrating the circuit and RT-LAB project created in Matlab®/Simulink® and RT-LAB® software.

The function of the current amplifier is to convert a voltage signal generated by the real-time simulator to a current source applied to the protective relay under test. Fig. 3.2 shows the amplifier controller receives voltage and current reference signals from the OP510 real-time simulator, as well as from the measured currents and voltages. The measured currents are scaled using the HX 05-P transducer transfer function and filtered using a Low Pass Filter (LPF) tuned at 1200 HZ. The output of the closed-loop control is set to the positive pin of the amplifier through the NI-9263 analog output card. This voltage generates a voltage drop across the resistor terminal to draw the current specified by the real-time model on the OP4510 real-time simulator. The I/O configuration for the data acquisition and control is shown in Figure 3.2-(g).

3.3. Control Design

The closed-loop control is implemented in the *abc* frame. This controller has the advantage of not requiring phase-locked loop (PLL) or reference frame transformations [74]. Integral Resonant (IR) regulators were added to the current loop to provide zero-steady state error while maintaining low current distortion. The resonant compensator was tuned at the grid frequency to track the fundamental component of the current. The integral gain was used to track dc signals present during the fault conditions, and to limit the bandwidth of the controller [68]. For this project, a bandwidth of 1200 Hz was established in the current control loop to represent dynamics up to the 20th harmonic.

The open open-loop transfer function of the current controller using integral-resonant controller is defined by (3.1), where G_{OAMP} is the amplifier gain, K_i is the integral gain, K_{60} is the resonant gain at 60 Hz, ω_c is the cutoff frequency, ω_o is equal to $2\pi 60$ and s is the Laplace variable.

$$T_o(s) = \left(\frac{G_{OAMP}}{R} \right) \left(\frac{K_i}{s} + \frac{K_{60} 2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \right) \quad (3.1)$$

Fig. 3.3 shows the results of including feed-forward technique together with resonant controllers in the current controller. Fig. 3.3(a) shows that the integral controller is insufficient to provide zero-steady state error between the control signal and the measured current. When the feed-forward is activated, the steady state error is reduced but the tracking at the fundamental frequency is still inadequate; see phase *c* in Fig. 3.3(b).

When resonant controllers are used without activating the feed-forward, the steady state error at the fundamental frequency is effectively reduced, however the control does not perform well during fast transitions, see phase *a* in Fig. 3.3(c). Fig. 3.3(d) shows that combining integral, resonant controllers together with feed-forward techniques is an effective way to reduce the steady-state error while maintaining an accurate tracking during fast transitions.

Fig. 3.4 presents the experimental verification for different types of grid events. These events were obtained from the DOE/EPRI Disturbance Library [75], which include events such as recloser tripping due a tree branch, faults caused by trucks hitting poles and short-circuits created by wild animals. This figure superimposes the three-phase reference currents with the measured three-phase currents. For this test, the SEL 451 relay remained disconnected to study the dynamics and accuracy of the designed controller.

As shown, the designed amplifier and control accurately tracks the current reference for these grid events. The steady-state error between the reference current and the measured current is negligible, and the total distortion of the current remains below 2% during pre-fault, and fault state. The power spectra for these grid events are presented in Fig. 3.5. For this figure the currents were per-unitized by using the magnitude of the dominant harmonic excluding the fundamental. As shown, the amplifier effectively represented all the currents for a wide range of frequencies.

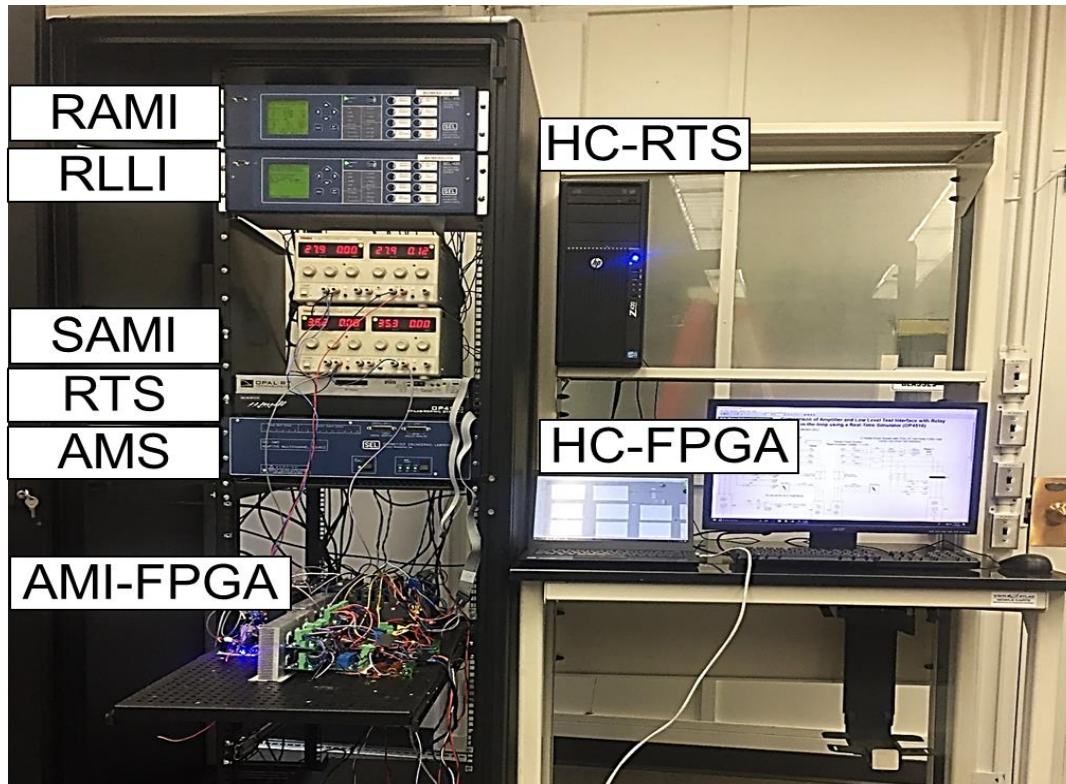


Figure 3.1: Control and Hardware diagrams. RAMI: Relay with amplifier interface, RLLI: Relay with Low-Level interface, SAMI: Source for amplifier interface, RTS: Real-time simulator, AMS: Adaptive multichannel source, AMI-FPGA: Amplifier interface with field-programmable gate array, HC-RTS: Host computer for real-time simulator, HC-FPGA: Host computer for field-programmable gate array

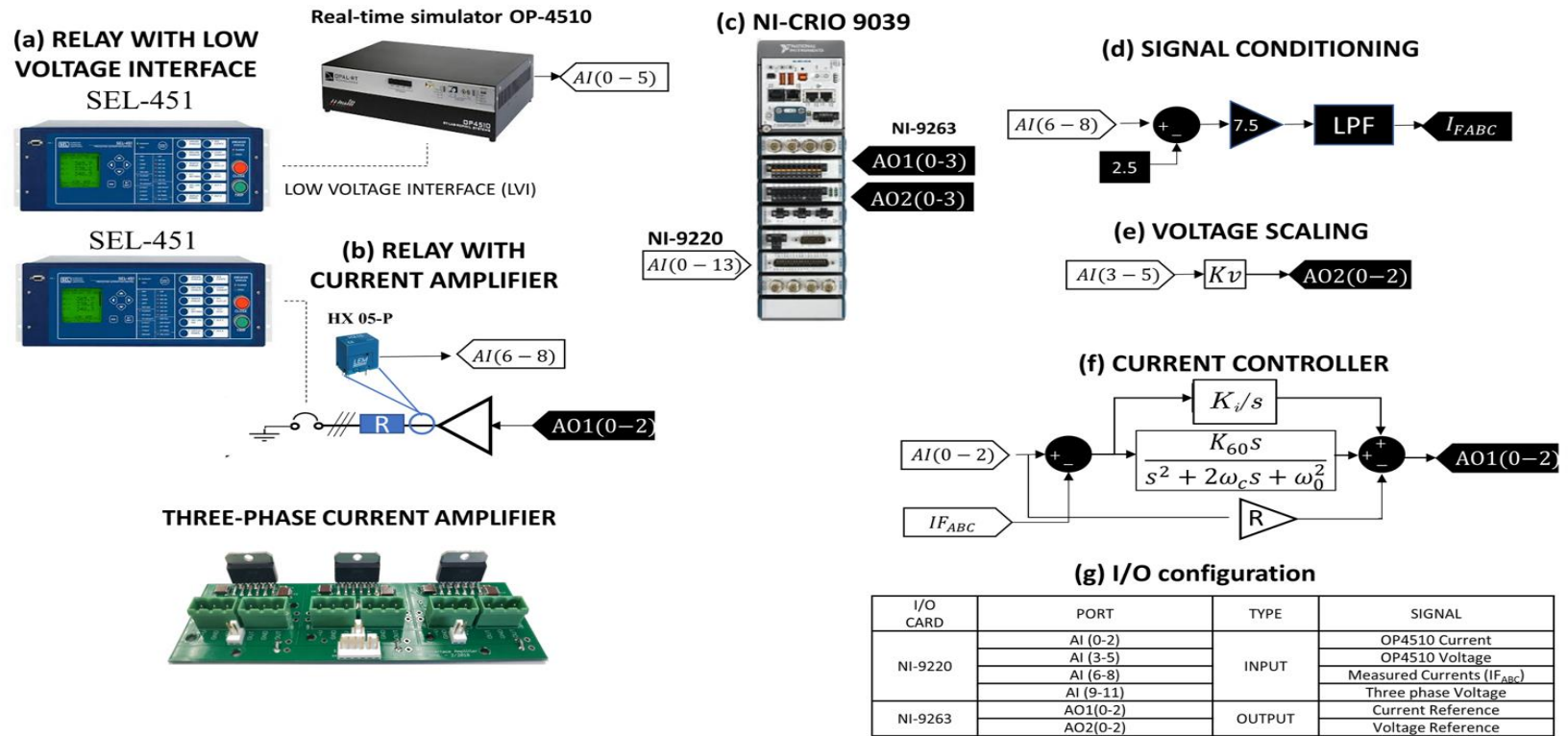


Figure 3.2: Control and hardware diagrams

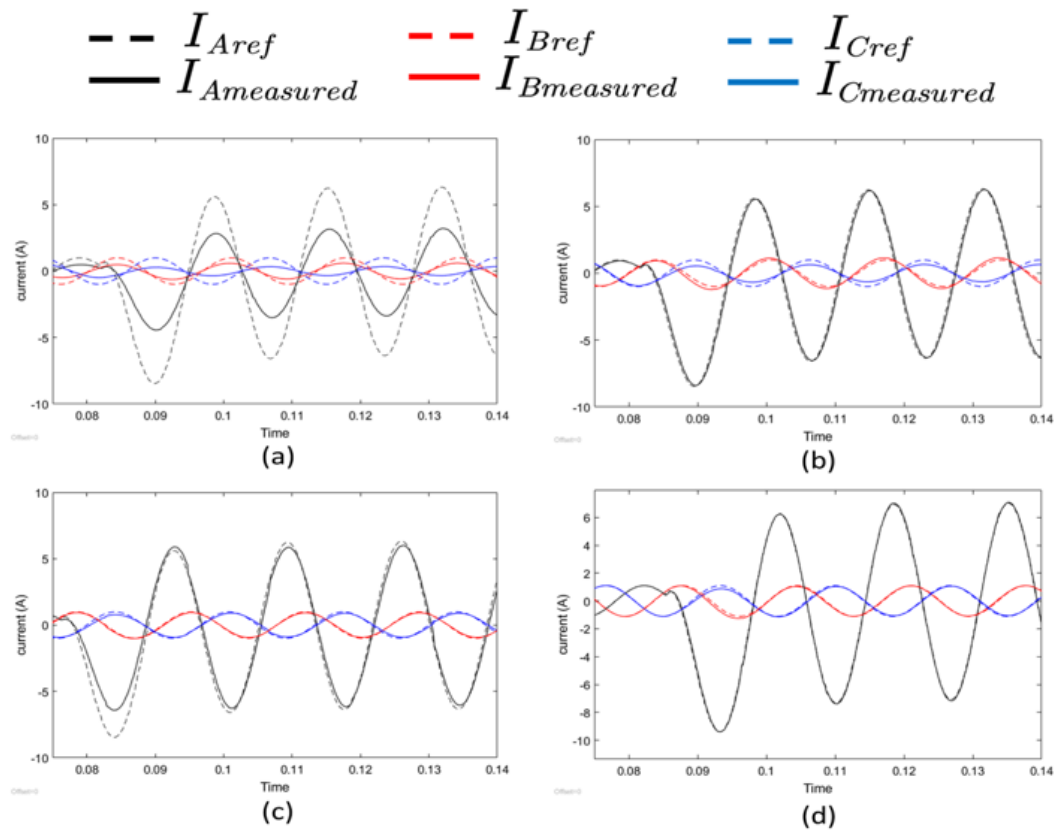


Figure 3.3: Controller techniques current regulation comparison. (a) PI, (b) feed-forward, (c) Integral-Resonant, (d) Integral-Resonant with feed-forward

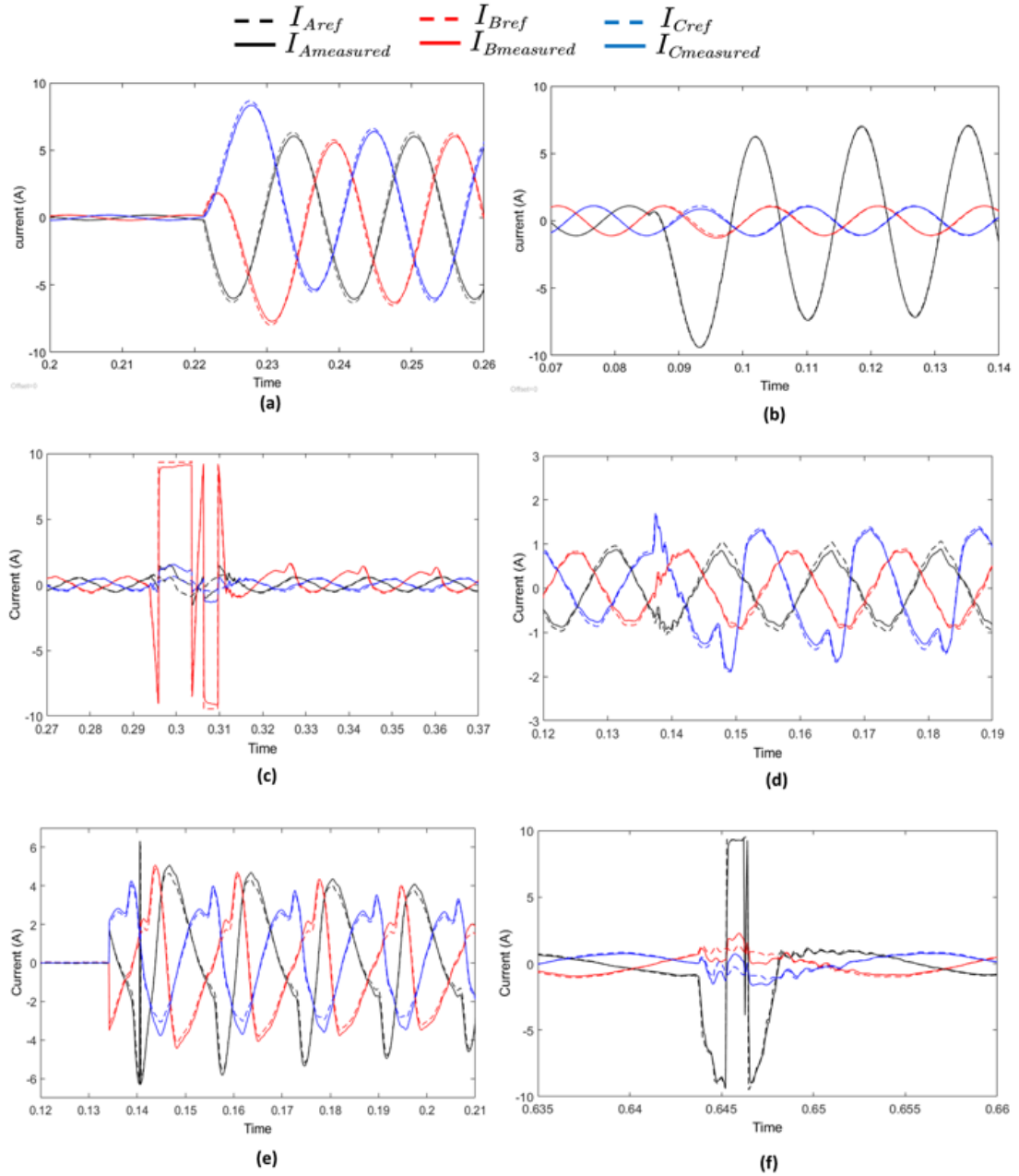


Figure 3.4: Power systems faults: (a) symetrical three-phase fault. (b) Phase-a to ground fault. (c) Pickup load after lightning strike. (d) Recloser trip because of tree branch. (e) Fault caused by a truck hitting a pole. (f) Fault caused by a squirrel. Events files from DOE/EPRI Disturbance Library [75].

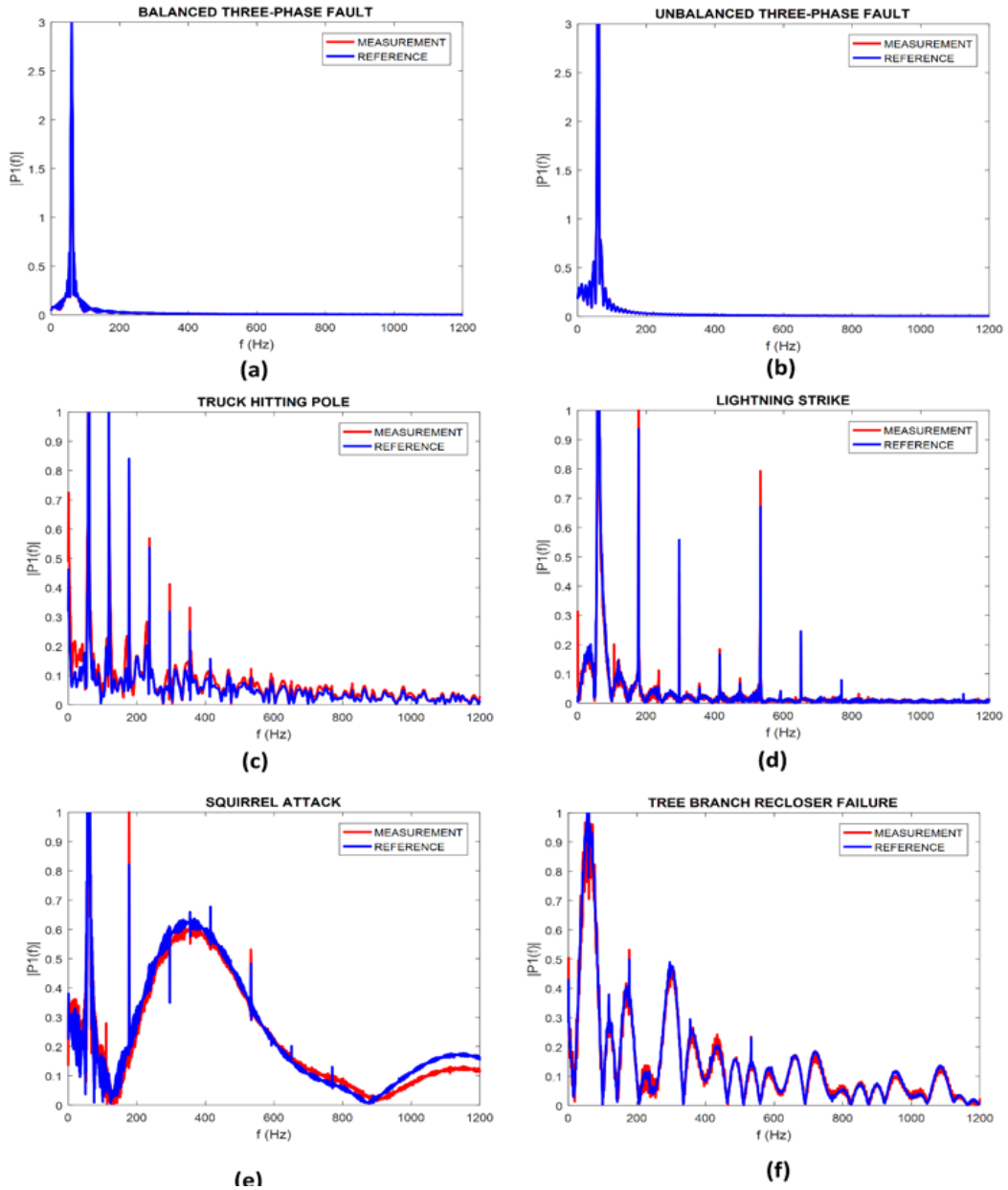


Figure 3.5: Fast Fourier transform (FFT) for: (a) balanced three-phase fault. (b) Phase-a to ground fault. (c) Pickup load after lightning strike. (d) Recloser trip because of tree branch. (e) Fault caused by a truck hitting a pole. (f) Fault caused by a squirrel. Events files from DOE/EPRI Disturbance Library [75]

3.4. Twin Power System and Relay in the Loop

This section shows the power system simulation utilized to emulate faults in real-time. This emulation consists of two identical electrical grids given by a utility source, breaker, transmission line, and load. This electrical grid was based on a radial power system at 3.8 kV phase-to-neutral voltage.

The real-time simulations for both power systems were run at the same time with a 50 μ s time step. The twin-power systems for the amplifier and low-level test interface is shown in Fig. 3.6 and Fig. 3.7. During the real-time tests, a phase-to-ground fault located at the end of the transmission lines were simulated. In the RT-LAB project, the gains of current (1/30000) and voltage (1/6000) sensors were set. During the real-time tests, a phase-to-ground fault located at the end of the transmission lines were simulated. The real-time simulation tests were set to be stopped at 200 s., and the fault block was triggered at 100 s. by the signal generated by the “Fault Block Signal Circuit”.

set with an U3 Very-inverse time curve, time dial setting (TDS) of 6 sec., and relay current pickup (I_P) of 1 A. Based on the U3 Very-inverse time curve from SEL 451 relay’s manual, the theoretical relay time (T_R) in cycles can be calculated by (3.2).

$$T_R = 60 \times TDS \times \left(0.0963 + \frac{3.88}{(I/CTR/I_P)^2 - 1} \right) \quad (3.2)$$

The SEL-451 relays wired with the OP4510 real-time simulator, and the low-level and amplifier interfaces were set with identical general and overcurrent settings. The current transformer ratio (CTR) setting was set at 400. The inverse time overcurrent settings were

3.5. Results and Discussion

In this study, the phase-to-ground fault was simulated in real-time and the high-resolution record events from the SEL-451 relays with the low-level, Fig. 3.6, and amplifier Fig. 3.7 interfaces were collected. The measured relay times had shown similar values, indicating the relays with low-level and amplifier interfaces had similar behaviors for the phase-to-ground fault. The SEL-451 relays wired with the OP4510 real-time simulator, and the low-level and amplifier interfaces were set with identical general and overcurrent settings. The current transformer ratio (*CTR*) setting was set at 400. The inverse time overcurrent settings were set with an U3 Very-inverse time curve, time dial setting (*TDS*) of 6 s, and relay current pickup (I_P) of 1 A.

The measured relay times in cycles for the relay with the low-level and amplifier interfaces were 668.9 and 670.9 cycles, respectively indicating the relays with low-level and amplifier interfaces had similar behaviors for the phase-to-ground fault. The experimental percentage error for the relay with the low-level interconnection was -0.62% and for the relay amplifier interface was -0.33%. These small errors indicate that the amplifier interface is a valid alternative to test protective relays. The amplifier interface is a useful tool to test the relay's backbone and sensor network, something that cannot be accomplished with the low-level interface.

3.6. Conclusions

In this chapter a low-cost three-phase amplifier interface for protective devices was developed and validated satisfactorily for the simulation of a phase-to-ground fault, using the state-of-the-art real-time digital simulation. The low-level and amplifier interfaces with the relays in-the-loop had shown similar tripping times and current shape behaviors from the high-resolution recorded events. The amplifier interface sensed the secondary currents instead of the low-level analog signals, offering the possibility for future connectivity with different relay vendors and secondary current ranges (from 0.5 to 10 A).

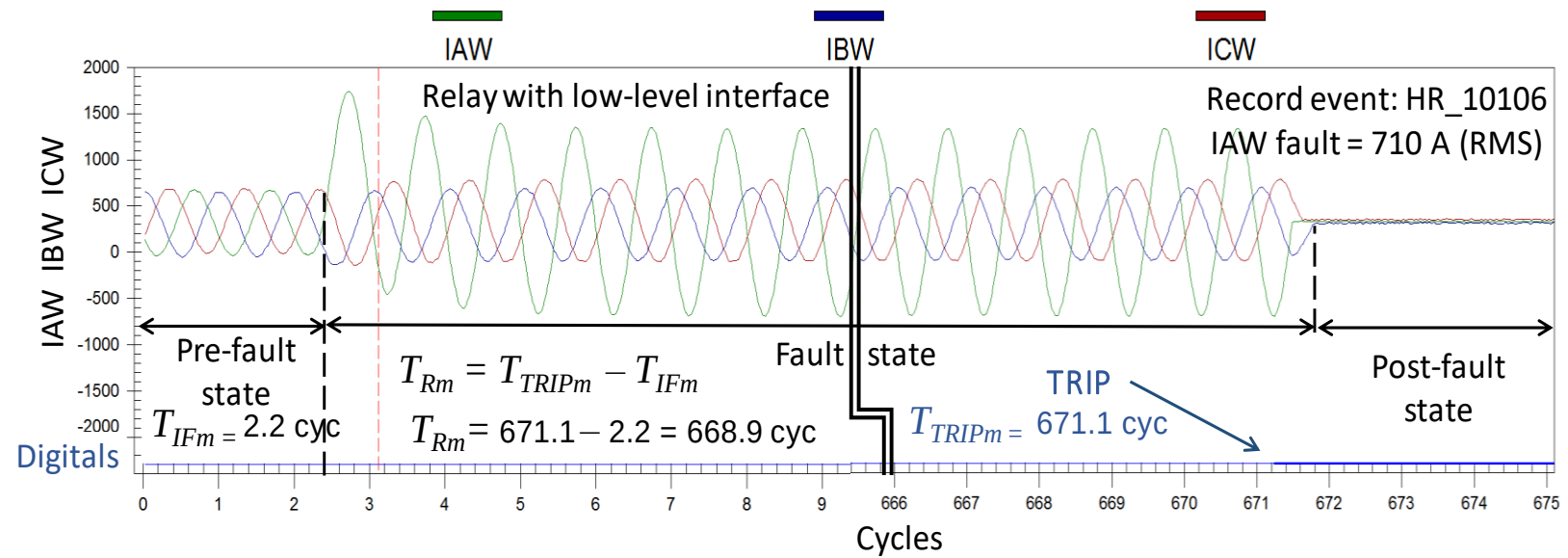
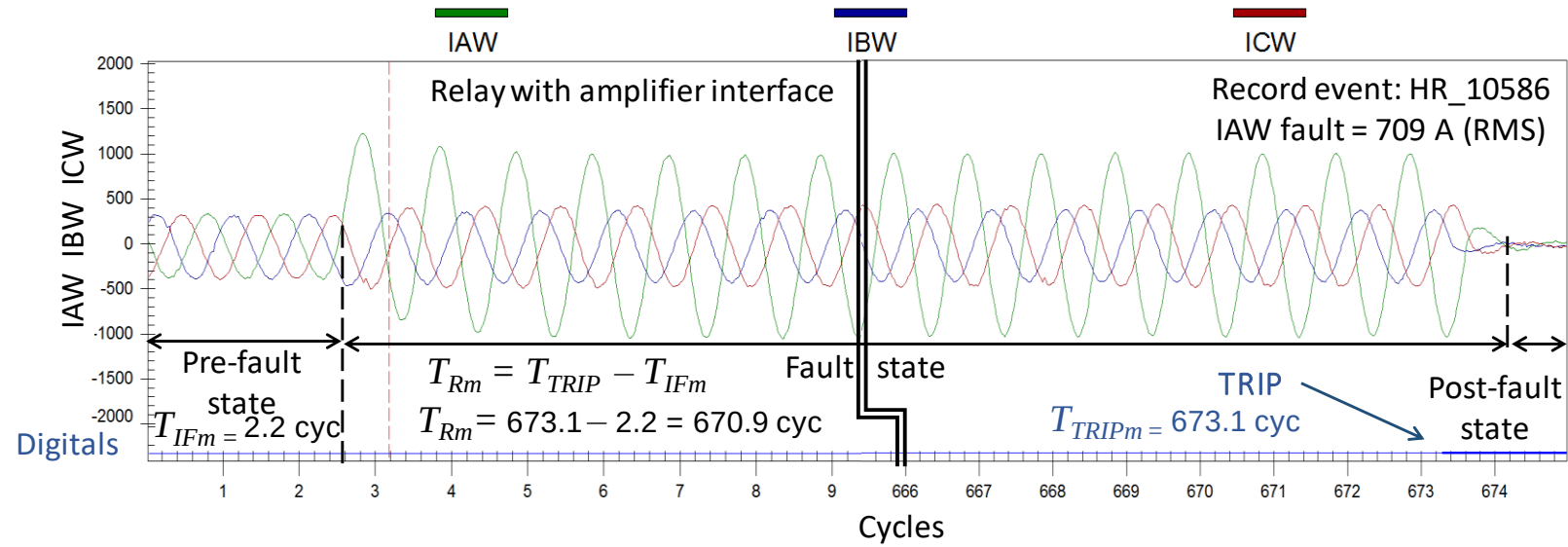


Figure 3.6: SEL-451relay measured currents with low-level interface.



(b)

Figure 3.7: SEL-451relay measured currents with proposed amplifier interface.

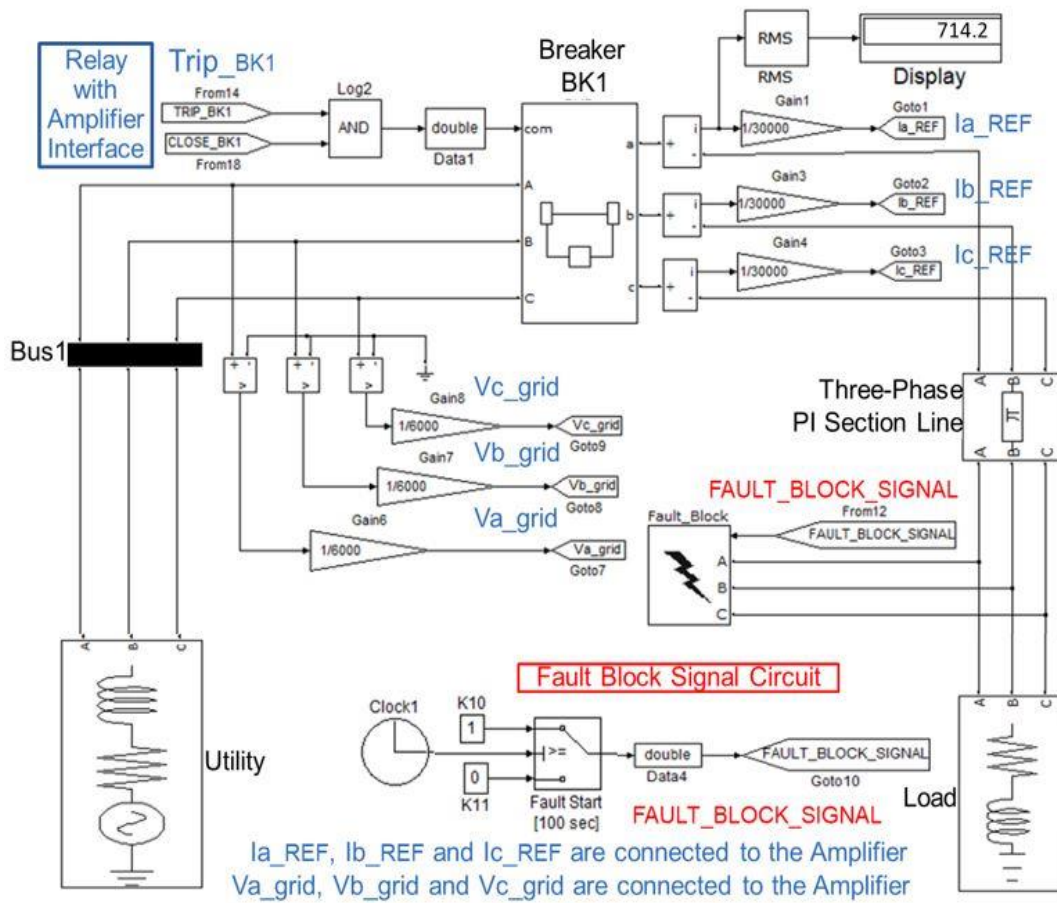


Figure 3.8: Power system for relay with amplifier interface.

In addition, this proposed amplifier interface with FPGA modules presents a low-cost alternative compared with actual relay testing devices used as amplifier interfaces with real-time simulators.

The current amplifier for use in protective relays was described. Resonant controllers tuned at the grid fundamental frequency were used to reduce the steady-state error between the control signal and the measured current while maintaining low current distortion. The performance of the current amplifier and control was verified experimentally in the time domain. The results show that the proposed design offers a cost-effective way to test protective devices for single-phase-to-ground, two-phase-to-ground, and three-phase faults.

CHAPTER 4
GRID-TIED DOUBLY-FED INDUCTION GENERATORS (DFIGS)
REAL-TIME MODELLING AND MODEL VALIDATION AND RESPONSE
DURING VOLTAGE SAGS

Abstract: This section presents the development and the model validation of a real-time (RT) emulator of a doubly fed induction generator (DFIG) wind turbine system. This model was developed and validated against physical measurements to accurately represent the operation of the grid tied DFIG during balanced and unbalanced operation, and to study the dynamic response of the machine during voltage sags. This section describes the required discrete models for real-time emulation of the DFIG, which were implemented on a field programmable gate array (FPGA), including: the dynamic model of the DFIG, rotor side converter (RSC), grid side converter (GSC), and aerodynamic and mechanical models. Previous work on real-time simulation of DFIGs have assumed that the generator model is valid over a wide range of operating speeds and for multiple grid voltage unbalances. However, this assumption has not been tested in the literature, which limits the accuracy of results obtained in both simulations and in hardware-in-the-loop (HIL) applications. To address this gap in the literature, this section presents a preliminary model validation of the DFIG with iron losses and demonstrates the limitations of the model in accurately representing a physical DFIG machine under grid unbalanced operation. This section first addresses the model validation by comparing the emulated stator and rotor currents against physical measurements under 0.5%, 2% and 4% grid voltage unbalance for speed ranging from the sub-synchronous to hyper-synchronous operation. Secondly, the DFIG model is used to study the response of the machine during voltage sags and unbalances. Finally, this section implements Low-Voltage Ride Through (LVRT) strategies to mitigate the rotor and stator overcurrent during voltage sags. This work also includes key implementation aspects of the hardware-testbed utilized for the model validation, which consists of a DFIG machine connected to a partial-scaled four-quadrant back-to-back power converter. The proposed discrete-time models, implementation methodology, and validation against hardware, results in a cost-effective, open-code platform to study grid-connected DFIG wind turbine system during normal operation and during grid events.

4.1. Introduction

Doubly fed induction generators (DFIGs) have been broadly used in variable speed wind energy conversion systems due to their competitive cost, durability, flexible power control,

and variable speed capacity using a partial-scaled converter [76]. These advantages have made the DFIG one of the leading technologies in the wind turbine sector as well as the most installed variable speed wind turbine in the United States [76-78]. Due to its preeminence as a renewable energy technology, combined with grid codes requiring increased capability during voltage and frequency grid events [79-81], it is becoming increasingly important for the research community and the industry to have a better understanding of the grid-connected DFIG systems' operations during various grid conditions. However, applied research on a full-scale utility system is limited due to prohibitive costs and safety concerns. Laboratory testbeds are an alternative to study full-scale systems [82-84]. These designs offer a reliable representation of the DFIG system. However, this approach also presents inhibiting factors including high cost, high complexity, long development times, and steep associated learning curve. Commercial real-time simulators, including RTDS, OPAL-RT, StarSim, Plexim and Typhoon, remove many technical barriers and reduce development times but can still be prohibitively expensive [85-87]. These solutions provide pre-built models, automatic code generation capability, and human machine interface (HMI), enabling rapid prototyping and testing of power systems and power electronics systems. Although these simulators are a powerful auxiliary platform to hardware implementation that allow to study and simulate systems in real-time, they require proprietary hardware and licensing, and the validity of the models is typically not published. In the face of these many challenges of studying systems in real-time, one economically accessible and technically proficient option is to implement the discrete models directly on Digital Signal Processors (DSPs) or Field Programmable Gate Arrays (FPGA). This approach removes some of the mentioned barriers while permitting the access of intermediary variables that are not typically available in pre-built, commercial models. Some authors have taken this approach to emulate real-time wind energy systems. For example, researchers in [89] implemented the electrical and mechanical discrete models of the DFIG and the permanent-magnet synchronous generator (PMSG) on a real-time computer Nexcom NISE 3140. Authors in [88] developed a real-simulation DFIG wind turbine to evaluate interconnection challenges, where a 7-bus grid was simulated in RTDS and the wind system is deployed on a DSP cluster. In [90], the authors compiled

into C-code a complete DFIG system and executed on PC-cluster real-time simulator. Although these papers address the discrete-modeling and implementation for real-time applications, critically, they lack details regarding the validity of the implemented models, which can limit the reliability of the obtained results.

Performing a real-time simulation using a validated model is critical to obtain accurate results in simulations and in applications that involve hardware-in-the-loop (HIL). HIL applications can be divided in power-hardware-in-the-loop (PHIL) and control-hardware-in-the-loop (CHIL). In PHIL, real power devices and systems interact with the real-time models of power elements and control systems in a closed-loop simulation [91]. In CHIL, a controller embedded on an external processor exchanges control signals with the real-time computer through the low-voltage high-speed I/O. Real-time models can interface through the low-voltage interface of protective equipment to perform protection studies. These approaches have been applied to photovoltaic systems [91] and for testing adaptive protection schemes in distribution systems [94] and DFIGs [94,95]. The discrete real-time models presented in this chapter have been interfaced with power amplifiers, validating their functionality for PHIL applications, examples of this can be found in [109] and [110].

As presented, extensive research has been done on real-time modelling and simulation, and its application in PHIL and CHIL. However, the published papers in real-time simulations typically do not provide details about the validity of the models. If the models used in real-time simulations are not accurate representations of the real system, their utility as a replacement for research purposes is severely limited. Focusing on DFIGs [95-97], only a few papers address the model validation against physical hardware. For example, authors in [95] present a comparison of the DFIG model for three-phase voltage dips and unbalanced voltages for a 3 MW DFIG. Authors in [96] present a DFIG model validation of a laboratory scale DFIG for voltage sags. Although some of these studies do use field data to validate the DFIG machine, the validation is limited to power quality issues. The full-range validation of the DFIG has been overlooked in the literature.

As a preliminary step in addressing this gap in knowledge, this chapter presents a validation of the DFIG model against a scaled-down DFIG. The model selected for this study is the $\alpha\beta$ model oriented with the rotor angles, which is commonly used to study DFIG operation. The iron losses were included in the model used for the validation because low-power machines like the one used for this study are lossy in comparison with full-rated machines. This work makes several contributions to the literature. First, it provides a wide characterization range of the DFIG model with iron losses against the physical measurements from the sub-synchronous to hyper-synchronous operation and during unbalanced conditions. This wide speed range validation is an important step towards revealing the limits in which the DFIG model remains representative. Second, all the models required to emulate the DFIG system are described in detail. Third, five implementations of the DFIG are compared in terms of FPGA resource utilization and execution time. Important aspects of the hardware testbed developed for verification purposes are also addressed, including the control for the rotor and stator converter and start-up sequence algorithms. Finally, this work also presents a novel and robust algorithm to calibrate the encoder without the use of integrators.

4.2. Discrete Models

The DFIG dynamic model describes the behavior of the machine in steady state as well the evolution of the electric variables during transients [76]. The review of literature shows four different reference frames that are used to express the electric variables of the DFIG: the $\alpha\beta\gamma$ oriented with the stator or rotor angles, synchronous (dqo), and natural frame dynamic models [98]. These models can be represented in matrix form using currents or fluxes as state variables. Because the logic resources on the FPGA are limited, it is critical to find a machine model that uses the fewest resources as possible while providing an accurate representation of the machine dynamics [101]. Appendix 1 show the computer implementations of the DFIG models used in this chapter. Fig. 4.1 shows a benchmark between these models in terms of execution time and FPGA slices utilization. For this comparison, the compilation results of four independent compilations were averaged, and neither the compiler nor the code were optimized in any way. Fig. 4.1 shows that the

chosen reference frame and the state-variable representation impact the model execution time and FPGA logic requirements. Although the DFIG $\alpha\beta$ model that uses the fluxes as state variables is proven to be efficient for real-time applications, it does not take into consideration the core loss, which is considerable in low power machines such as the one utilized in this study. Neglecting the iron losses in low power machines introduces substantial errors in the estimation of the rotor and stator currents. To provide a model as close as possible to the real machine, the iron loss is introduced in the model. As shown in Fig. 4.1, introducing the iron losses increases the loop time execution to 60 μ s and requires 15% of the logical resources in the Xilinx Kintex-7 7K325T FPGA. For MW machines, the losses can be neglected, and a more efficient model can be used instead. Fig. 4.2 shows the computer implementation of a DFIG dynamic model that include iron losses and the one used in this study [100].

4.3. Discrete Model: Back-to-Back

Different types of converter topologies have been proposed for wind applications; however, the most common choice for the DFIG is the back-to-back converter [101]. The back-to-back model consists of a grid-side converter (GSC) and rotor-side converter (RSC.) The size of the power converter for DFIG applications typically does not exceed 25-35% of the machine's nominal power. Fig. 4.3. shows an average model for a back-to-back converter. Applying Kirchhoff's law on the circuit of Fig. 4.3. and choosing currents as state-variables, the average model of the GSC is represented by (4.1), the RSC by (4.2), and the DC-link circuit by (4.3):

$$\frac{d}{dt} \begin{bmatrix} i_{Fa} \\ i_{Fb} \\ i_{Fc} \end{bmatrix} = \frac{R_f}{L_f} \begin{bmatrix} i_{Fa} \\ i_{Fb} \\ i_{Fc} \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \frac{1}{L_f} \begin{bmatrix} v_n \\ v_n \\ v_n \end{bmatrix} - \frac{V_{DC}}{L_f} \begin{bmatrix} d_{Fa} \\ d_{Fb} \\ d_{Fc} \end{bmatrix} \quad (4.1)$$

$$\frac{d}{dt} \begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} = \frac{R_r}{L_r} \begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} + \frac{R_r}{L_r} \begin{bmatrix} v_{ra} \\ v_{rb} \\ v_{rc} \end{bmatrix} + \frac{1}{L_r} \begin{bmatrix} v_n \\ v_n \\ v_n \end{bmatrix} - \frac{V_{DC}}{L_r} \begin{bmatrix} d_{ra} \\ d_{rb} \\ d_{rc} \end{bmatrix} \quad (4.2)$$

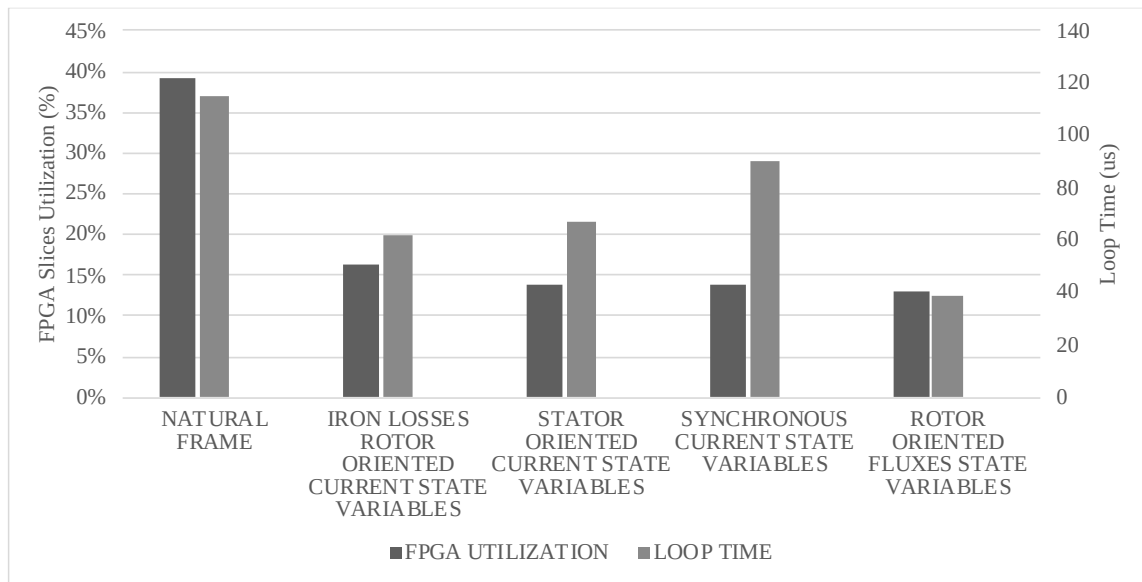
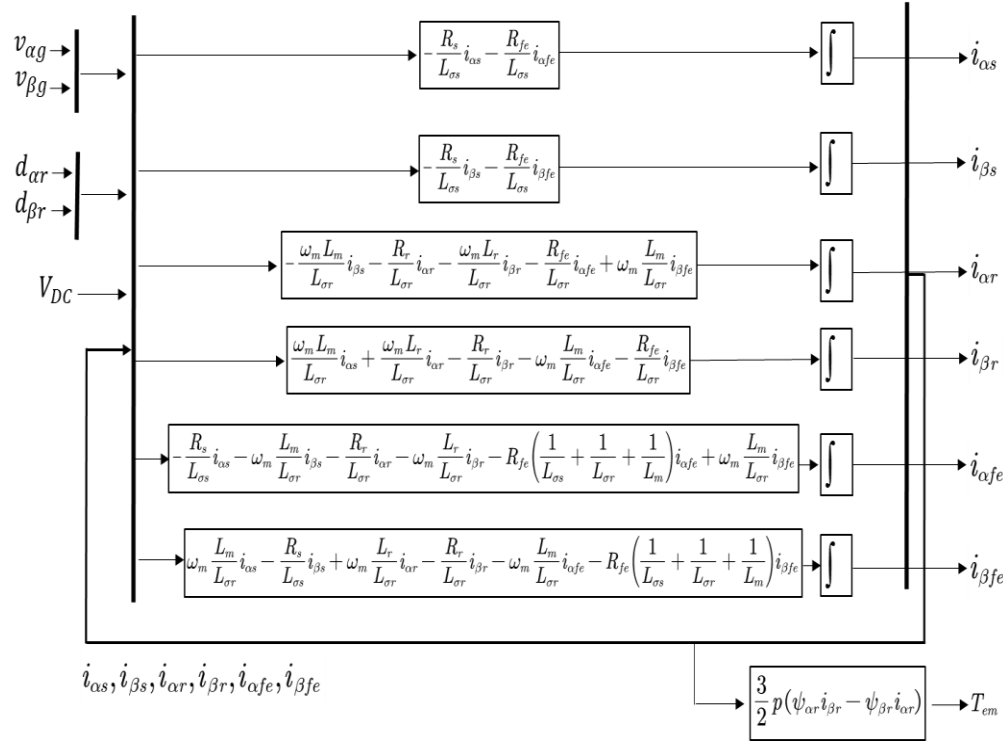
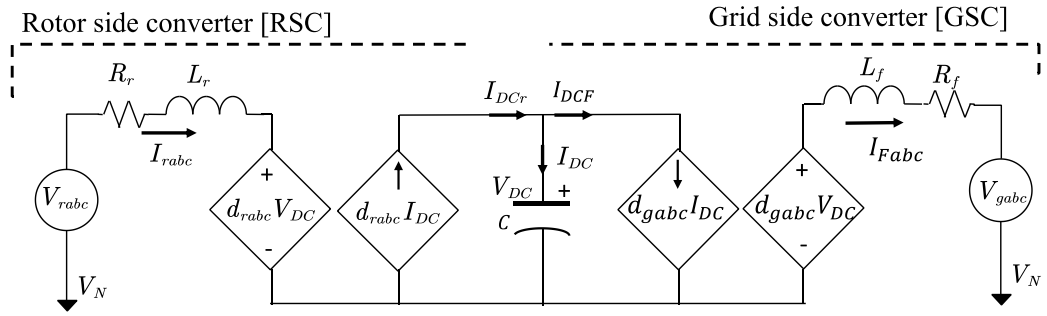


Figure 4.1: FPGA utilization and loop time for different DFIG machine models.



$v_{\alpha g}$ = alpha grid voltage; $v_{\beta g}$ = beta grid voltage; $d_{\alpha r}$ = alpha duty cycle of rotor; $d_{\beta r}$ = beta duty cycle of rotor; V_{DC} = DC-link voltage; R_s = stator resistance; R_{fe} = iron loss resistance; R_r = rotor resistance; θ = leakage coefficient; L_s = stator self-inductance; $L_{\sigma r}$ = rotor leakage inductance; $L_{\sigma s}$ = stator leakage inductance; L_m = mutual inductance; ω_m = rotor frequency; $\Psi_{\alpha r}$ = alpha rotor flux linkage; $\Psi_{\beta r}$ = beta rotor flux linkage; $\Psi_{\beta s}$ = beta stator flux linkage; p = pole pairs; $i_{\alpha s}$ = alpha stator current; $i_{\beta s}$ = beta stator current; $i_{\alpha r}$ = alpha rotor current; $i_{\beta r}$ = beta rotor current; $i_{\alpha fe}$ = alpha iron loss current; $i_{\beta fe}$ = beta iron loss current; T_{em} = electromagnetic torque.

Figure 4.2: Computer implementation of the DFIG considering iron loss [76].



V_N = neutral voltage; V_{rabc} = a, b, c phase rotor voltages; R_r = rotor resistance; L_r = rotor self-inductance; I_{rabc} = a, b, c phase rotor currents; d_{rabc} = a, b, c phase duty cycles of rotor controller side; V_{DC} = DC-link voltage; I_{DC} = DC-link current; I_{DCr} = DC-link current of rotor; I_{DCF} = DC-link current of grid filter; C = circuit capacitance; d_{gabc} = a, b, c phase duty cycle of grid controller side; I_{Fabc} = a, b, c phase grid filter currents; L_f = grid filter inductance; R_f = grid filter resistance; V_{gabc} = a, b, c phase grid voltages

Figure 4.3: Average model for a back-to-back converter.

$$\frac{d}{dt} V_{DC} = \frac{1}{C} \left([d_{ra} \ d_{rb} \ d_{rc}] \begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} - [d_{Fa} \ d_{Fb} \ d_{Fc}] \begin{bmatrix} i_{Fa} \\ i_{Fb} \\ i_{Fc} \end{bmatrix} \right) \quad (4.3)$$

where i_{Fa} , i_{Fb} and i_{Fc} are grid side converter currents; i_{ra} , i_{rb} and i_{rc} are rotor currents; R_f is the grid filter resistance; R_r is the rotor resistance; L_r is the rotor self-inductance; L_f is the grid filter inductance; v_{ga} , v_{gb} and v_{gc} are phase grid voltages, v_{ra} , v_{rb} and v_{rc} are phase rotor voltages; v_n is the neutral voltage; V_{DC} is the DC-link voltage; d_{Fa} , d_{Fb} , d_{Fc} are the duty cycles of the grid side controller; d_{ra} , d_{rb} , d_{rc} are the duty cycles of the rotor, and C is the DC-link capacitance.

Fig. 4.4 shows the implementation of the average model for the back-to-back converter which was programmed on a LabVIEW FPGA to emulate the power converter. This model receives the control modulating signals from the GSC (V_{gscabc}) and RSC (V_{rscabc}), the grid voltages (V_{gabc}), and rotor currents (I_{rabc}) and the initial charge of the capacitor (V_{DC0}). The outputs of this model are the DC-link voltage (V_{DC}) and GSC currents (I_{Fabc}).

Previously developed mechanical models include complex models of six masses or three masses [101]. However, the two-mass model is the simplest and provides reasonable accuracy. Assuming a perfect rigid low speed shaft, the two-mass train model is reduced to a one-mass drive train model. The resulting governing equation [105] is represented by (4.4):

$$\frac{d\omega}{dt} = \frac{p}{J} (T_{WT} - T_{EM}) \quad (4.4)$$

where ω is rotor speed in rad/s, p is the pole pairs, J is the inertia, T_{WT} is mechanical torque of wind turbine, and T_{EM} is the electromagnetic torque.

The mechanical output power that could be extracted from a three-blade wind turbine is given by,

$$P_{WT} = \frac{1}{2} \rho \pi R_{WT}^2 C_p(\beta, \lambda) v_{wind}^3 \quad (4.5)$$

where P_{WT} is the mechanical output power of the turbine in watts, ρ is the air density in kg/m^3 , R_{WT} is the blade radius of wind turbine in m, C_p is the performance coefficient of wind turbine, β is the blade pitch angle in degrees, λ is the tip speed ratio of the wind turbine blade, v_{wind} is the wind speed in m/s.

The performance coefficient of turbine (C_p) can be approximated by

$$C_p(\beta, \lambda) = 0.5176 \left(\frac{116}{\lambda_i} - 0.4\beta - 5 \right) e^{\frac{-21}{\lambda_i}} + 0.0068\lambda \quad (4.6)$$

and

$$\lambda = R_{WT} \frac{\omega_m}{v_{wind}} \quad (4.7)$$

$$\frac{1}{\lambda_i} = \frac{1}{\lambda - 0.08\beta} - \frac{0.035}{\beta^3 + 1} \quad (4.8)$$

4.4. DFIG Hardware Testbed Design

This section describes the hardware testbed used to verify the dynamic behavior of the DFIG model. Fig. 4.5(a) and (b) show the control and interconnections of the hardware testbed, which consists of a Motor Solver DFIG generator, a Viewpoint back-to-back converter, grid filters, and a permanent magnet (PM) driver used to emulate the wind model. The power converter controller was implemented on a NI-cRIO 9039 platform, where eight I/O modules were installed. The input analog card (AI) NI-9229 is mainly used for control purposes, the analog output card (AIO) NI-9381 provides the current reference to the Keithley 2268 power supply, which controls the PM driver. The digital output card (DIO) NI-9401 is primarily used for relay control and for PWM signals. The analog output card provided the current reference to the dc power supply, which controls the dc motor driver.

4.5. DFIG Vector Control

The power converter control applies a vector control strategy to independently regulate the active and reactive power from the grid [83, 102-104]. This classic strategy is based on using the power converters of Fig. 4.6, Fig. 4.7, that are composed of the rotor and grid side controllers, respectively.

The RSC controls the speed of the machine and the stator reactive power. In this case, the grid voltage orientation (GVO) was chosen as the reference frame orientation due its superior stability during voltage dips and unbalances compared with the classic field oriented or direct torque control. The RSC has two cascaded PI controllers Fig. 4.6 . The outer loops regulate the speed of the machine and the stator reactive power, the inner loops control the rotor current references. The current transfer functions for the rotor converter are defined by low frequency poles that depend on the passive elements of the induction machine, and it is defined by (9).

$$\frac{\tilde{I}_{rdq}}{\tilde{d}_{rdq}} = \frac{V_{DC}}{R_r + L_r \sigma s} \quad (4.9)$$

where σ is the leakage coefficient and s is the slip defined as $\sigma = 1 - L_m^2/L_m L_s$, with L_m defined as the magnetizing inductance and L_s the stator inductance.

The GSC keeps a constant dc-link voltage regardless of the magnitude or direction of the power flow as shown in Fig. 4.7. The reactive power reference is kept zero to ensure unity power factor.

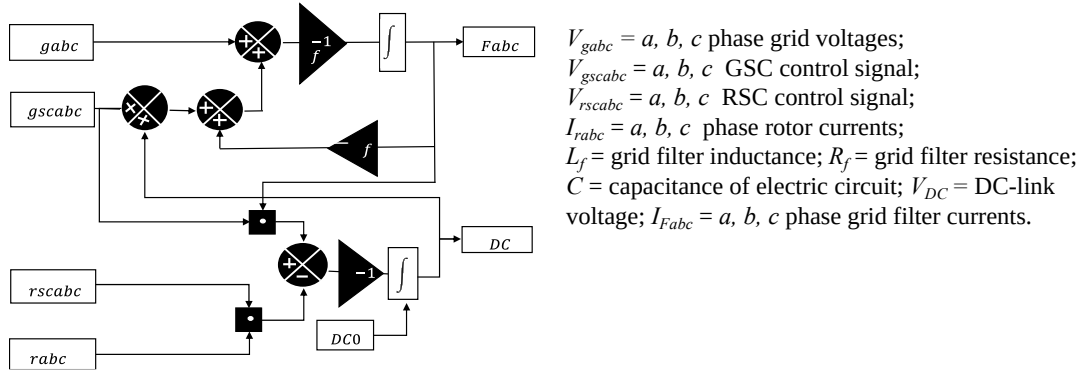
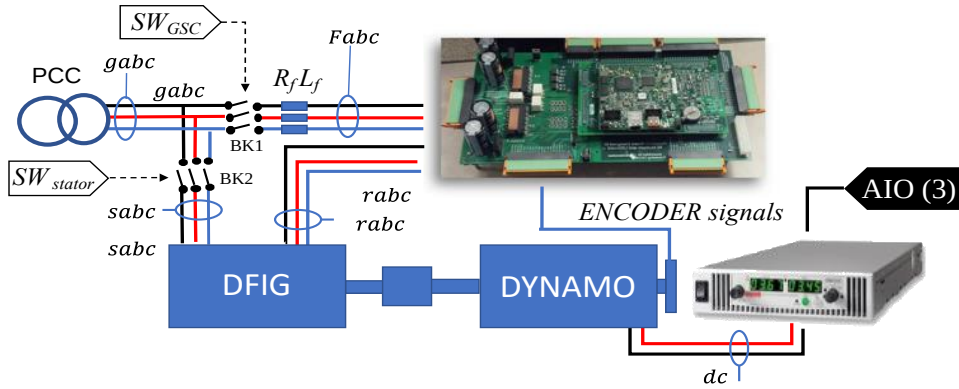
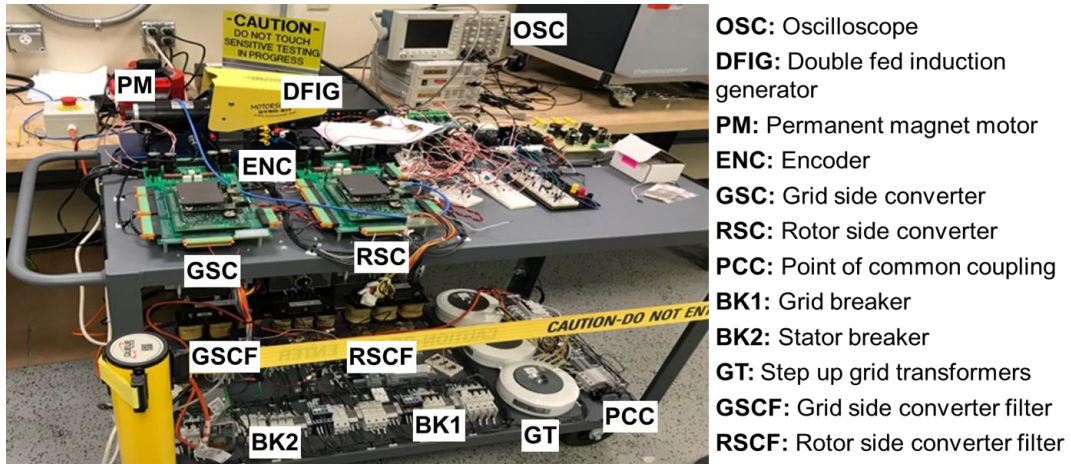


Figure 4.4: FPGA implementation of back-to-back converter

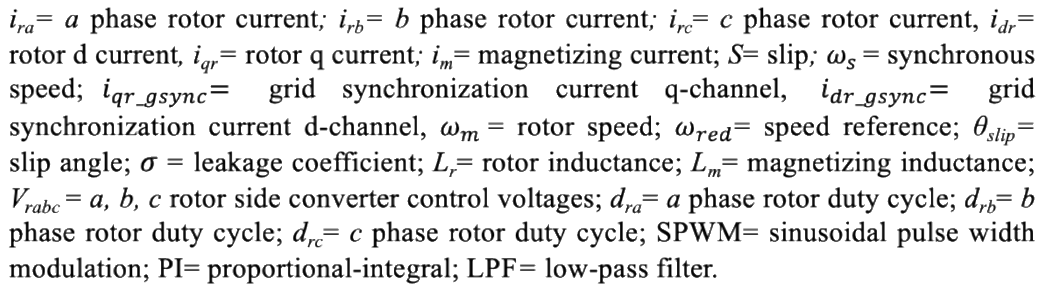


(a) Electrical schematic of DFIG testbed

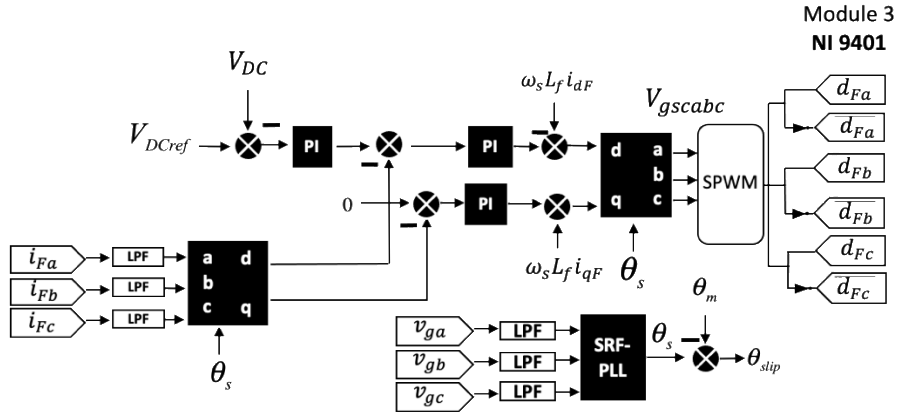


(b) DFIG Hardware testbed

Figure 4.5: Doubly-Fed induction generator testbed



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i_{Fa} = a phase grid filter current; i_{Fb} = b phase grid filter current; i_{Fc} = c phase grid filter current; V_{DC} = DC-link voltage; V_{DCref} = DC-link voltage reference; ω_s = grid angular speed; v_{ga} = a phase grid voltage; v_{gb} = b phase grid voltage; v_{gc} = c phase grid voltage; θ_s = grid angle; L_f = grid filter inductance; V_{gscabc} = a, b, c grid side converter control voltages; i_{dF} = d current, i_{qF} = q current; d_{Fa} = a phase grid filter duty cycle; d_{Fb} = b phase grid filter duty cycle; d_{Fc} = c phase grid filter duty cycle; LPF = low-pass filter; PI = proportional-integral; SPWM = sinusoidal pulse width modulation; SRF-PLL = synchronous-reference frame phase locked loop.

Figure 4.7: Vector control grid-side converter.

Using the vector control presented in [83], the current transfer functions are defined by low frequency poles that depend on the grid filter parameters, and it is represented by (4.10).

$$\frac{\tilde{I}_{Fdq}}{\tilde{d}_{Fdq}} = \frac{V_{DC}}{R_f + L_f s} \quad (4.10)$$

where R_f is the grid filter resistance and L_f is the grid filter self-inductance.

Table 4.1 presents the gains for the PI controllers that were calculated using the Butterworth polynomial, where $\omega_{DC} = \omega_{speed} = \omega_{oc}/10$ and ω_{oc} is ten times lower than the switching frequency, $f_s = 2$ kHz. This method optimizes the closed-loop eigenvalue locations and locate the eigenvalues uniformly in the left-half s-plane on a circle with radius ω_{oc} [102].

In Eq. 4.11 $\vec{V}_{s\alpha\beta}$ is the stator voltage in $\alpha\beta$, $\vec{I}_{s\alpha\beta}$ the stator currents in $\alpha\beta$, $\vec{\psi}_{s\alpha\beta}$ the stator flux and R_s the stator resistance. To provide an alternative to pure integrators, this work proposes to estimate the stator flux by introducing a -90° phase in the measured induced stator voltages, which can be done by using the rotational transformation of (4.13).

$$\vec{\psi}_{s\alpha\beta} = \vec{V}_{s\alpha\beta} e^{-i\pi/2} \quad (4.12)$$

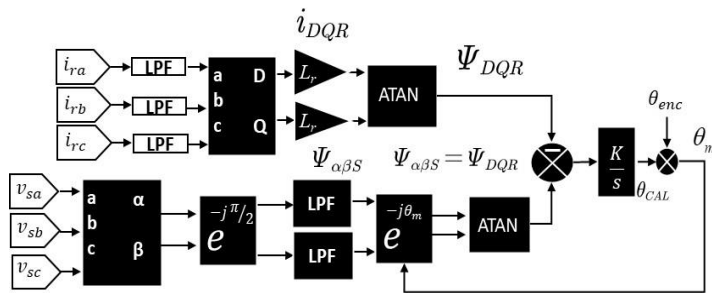
$$\psi_{\alpha} = V_{s\alpha} \cos(-\pi/2) - V_{s\beta} \sin(-\pi/2) \quad (4.13)$$

$$\psi_{\beta} = V_{s\alpha} \sin(-\pi/2) - V_{s\beta} \cos(-\pi/2)$$

Fig. 4.8. shows the proposed encoder calibration. The rotor flux in the DQ reference frame is estimated according to the block diagram. The stator flux is estimated by multiplying the stator voltage in $\alpha\beta$ by the rotational transformation. This algorithm yields the calibration angle (θ_{CAL}) required to correct the phase displacement between the estimated fluxes. When the calibration is finished, the algorithm is disabled and θ_{CAL} is added as a constant to the measured encoder angle (θ_{enc}). Fig. 4.9, shows the experimental results using the proposed method, see the clean estimation of the angles and the resulting angle calibration.

Table 4.1.
Proportional-integral control gains

Current Regulators of Grid Side Controller		Current Regulators Rotor Side Controller	
$k_{pdq} = 2\sqrt{2} \omega_{oc} L_f - R_f$	$k_{idq} = \omega_{oc}^2 L_f$	$k_{pdq} = 2\sqrt{2} \omega_{oc} \sigma L_r - R_r$	$k_{idq} = \omega_{oc}^2 \sigma L_r$
Voltage Regulator of Grid Side Controller		Speed Regulator of Rotor Side Controller	
$k_{pdq} = 2\sqrt{2} \omega_{dc} C$	$k_{idq} = \omega_{dc}^2 C$	$k_{pdq} = 2\sqrt{2} \omega_{speed} J/p$	$k_{idq} = 2 \omega_{speed}^2 J/p$
k_{pdq} = proportional gain, k_{idq} = integral gain, ω_{oc} = bandwidth current controller [rad/s], ω_{speed} = bandwidth speed controller [rad/s], L_f = grid filter inductance [H], R_f = grid filter inductance resistance [Ω], L_r = rotor inductance [H], R_r = rotor inductance resistance [Ω], J = generator inertia [kgm ²], p = pole pairs, σ = loss coefficient, C = DC-link capacitance [F]			



i_{ra} = a phase rotor current; i_{rb} = b phase rotor current; i_{rc} = c phase rotor current, LPF = low-pass filter; L_r = rotor self-inductance; v_{sa} = a phase stator voltage; v_{sb} = b phase stator voltage; v_{sc} = c phase stator voltage; i_{DQR} = rotor dq current, θ_m = mechanical rotor angle; θ_{enc} = encoder angle; θ_{CAL} = calibration angle; $\Psi_{\alpha\beta S}$ = $\alpha\beta$ stator flux linkage; Ψ_{DQR} = DQ rotor flux linkage; S = slip; K = gain.

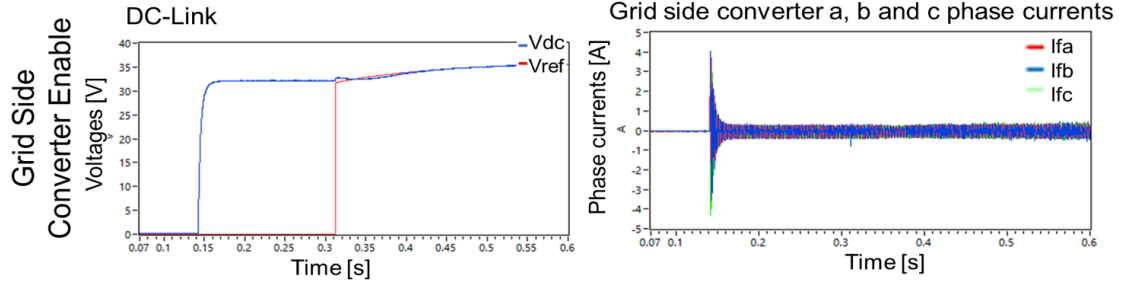
Figure 4.8: Proposed encoder calibration algorithm.

4.6. Experimental Results: DFIG Start-up Sequence

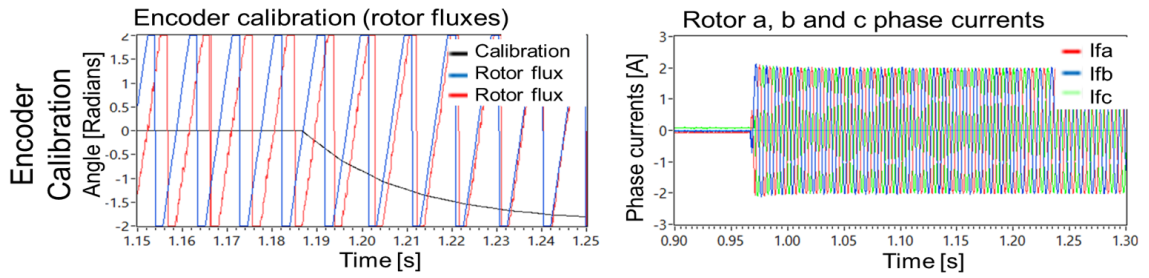
DFIG machines require a complex startup sequence because the reduced power converter only permits the machine to be controlled at speeds near synchronism, where the rotor demands a lower voltage. As described in [105,106], the startup sequence is mostly carried out by the rotor converter while the grid converter imposes a constant DC-link voltage. Fig. 4.9 shows the experimental results of the most relevant signals of the startup process for DFIG machine model. The sequence starts with Fig. 4.9(a), where the DC-link is pre-charged through the freewheel diodes of the insulated-gate bipolar transistor. Then, the GSC contactor is closed, and the grid converter starts regulating the DC-bus. In Fig. 4.9(b), the rotor side converter is activated, and the dynamo accelerates the machine to near synchronism condition (1800 RPMs). Then, the current reference is set in the d -channel of rotor converter current controller to induce voltage in the stator, after which the encoder algorithm is activated to align the zero position of the rotor. A detailed description of the proposed encoder calibration algorithm is addressed in the next section. In Fig. 4.9(c), the grid synchronization is activated, which modifies the rotor current references to match the stator magnitude and phase to the grid voltage. Finally, the stator contactor closes, and rotor converter controls starts controlling the generator speed, as shown in Fig. 4.9(d).

4.7. Experimental Results: DFIG Model Validation

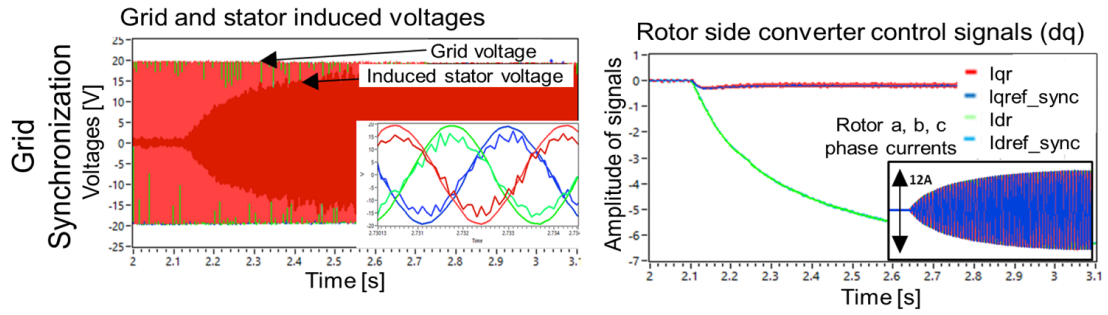
This section validates the stator and rotor currents of the DFIG machine model against physical measurements. To verify the model, the DFIG model receives the RSC average control and the grid voltage. The model outputs are the electromagnetic torque which is applied to the mechanical model to solve for the speed, rotor current and stator current. For the DFIG machine model the estimated generator passive parameters are $R_s = 0.65 \, \Omega$ (average stator resistance of three phases), $L_{ls} = 2.4 \, \text{mH}$ (stator leakage inductance), $R_r = 1.2 \, \Omega$ (average rotor resistance of three phases), $L_{lr} = 3.5 \, \text{mH}$ (rotor leakage inductance), $L_M = 4 \, \text{mH}$ (magnetizing inductance), $R_{fe} = 15 \, \Omega$ (iron core loss resistance), $U_{turn \, ratio} = 1.58$ (effective turn ratio), power rating=250VA.



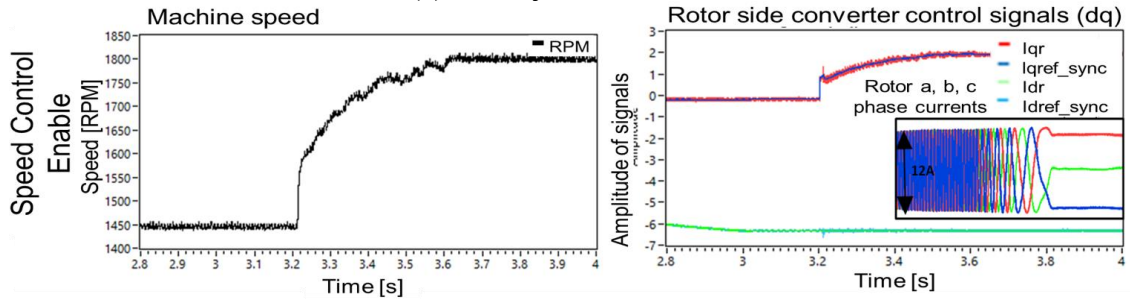
(a) GSC startup.



(b) Encoder calibration.



(c) Grid synchronization.



(d) Speed controller enabled.

Figure 4.9: Experimental results of the startup sequence.

These parameters were estimated using the non-load test and locked rotor tests. Fig. 4.10 shows a snapshot of the measured and emulated stator and rotor currents are plotted in *abc*. Fig. 4.10(a). and Fig. 4.10(b). plot the stator and rotor currents when the grid voltages have a 0.5% unbalance, which corresponds to the unbalance of at the point of connection. A quick inspection shows that at the vicinity of the synchronous speed (1.0 p.u.) the model is in good agreement with the measurements.

4.8. Experimental Results: Positive Sequence Validation

To provide a more comprehensive range of validation, this section shows the model validation of the positive sequence when the generator sweeps from sub-synchronous to hyper-synchronous operation under balanced grid conditions. The positive sequence validation provides information about the power exchange between the stator and the grid, and a correct estimation of this sequence is very important for a precise power flow analysis. To quantify the deviation between the measurements and the model estimated currents, article uses the same criteria as in [95] where the following expression is used:

$$Error_{\%} = \left| \frac{I_{measured} - I_{model}}{I_{measured}} \right| .100 \leq 10\% \quad (4.14)$$

where I is either the stator or rotor currents positive sequence in per unit. The model is declared valid if more than an 85% of the samples do not exceed 10% of deviation allowed for a wide range of operation. Fig. 4.11 shows the rotor current results when the stator voltages have a small unbalance (0.5%). As seen in the figure, the error for the rotor current is low for all speeds and all the datapoints are below 10% threshold with an average error is 1.67%. This section only presents the rotor currents for 0.5% grid voltage unbalance because for the other two cases [2%, 4%] the rotor currents remained practically unchanged.

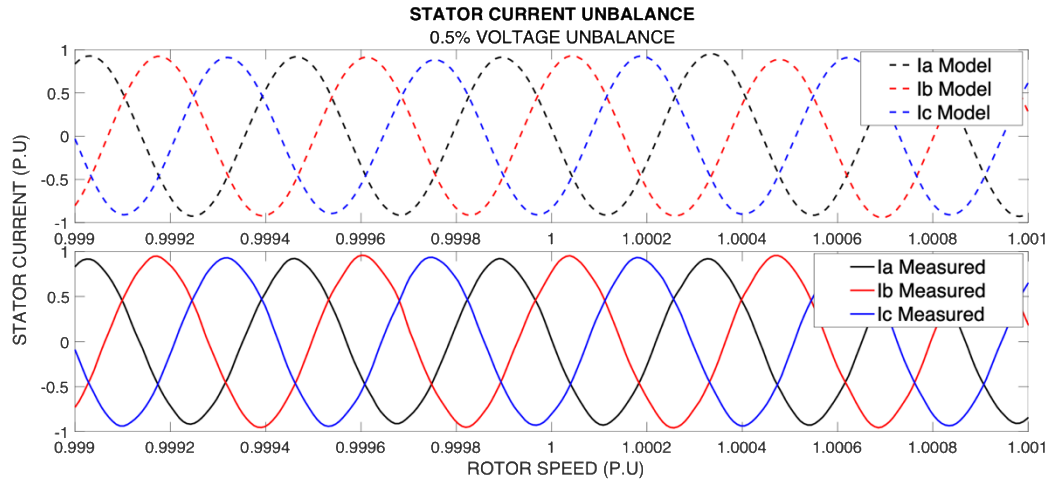
Fig. 4.12. shows the positive sequence of the stator currents when the grid voltages have a 0.5%, 2% and 4% imbalance. The voltage imbalance is introduced by connecting resistors

in series with the phase A at point of connection, and the DFIG model receives the voltage from sensors located after the resistor to be subject to the same voltage imbalance. As observed in the figure, the error depends on the operation speed of the machine and the amount of unbalance in the grid voltages, and the higher the unbalance and the speed the higher the deviation between the model and measurements. For 0.5% and 2% unbalance, all the datapoints remained under the 10% threshold with an average error of 0.75% and 5.22% respectively. Although the error is higher when the voltages are severely unbalanced (4%), 90.5% of the datapoints remained under the specified deviation with an average error of 7.6%. Therefore, concluding that the stator positive sequence and rotor currents are valid under a wide range of speeds and grid voltage unbalances.

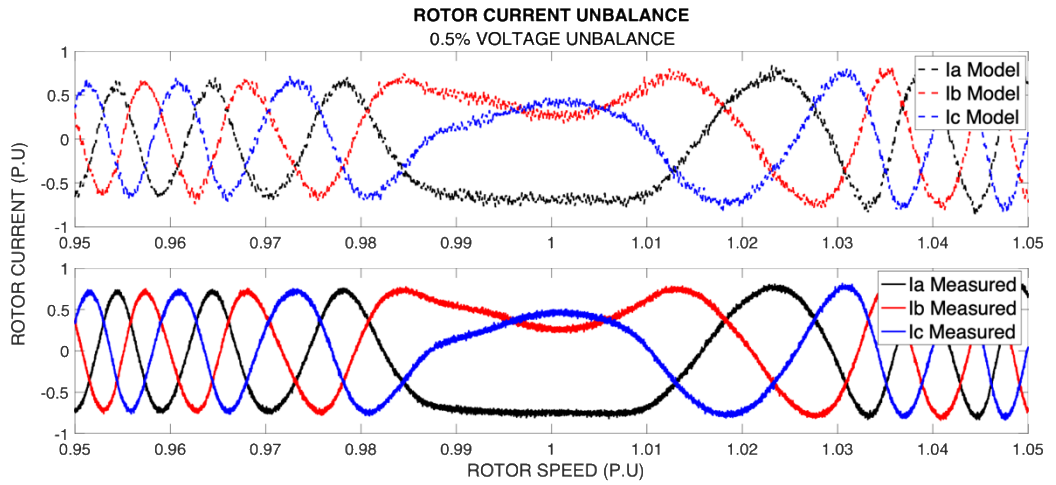
4.9. Experimental Results: Negative Sequence Validation

This section presents a comparison between the estimated and measured unbalance in the stator calculated through the IEEE definition [105]. Following similar methodology as in the previous section, a wide range of validation is presented, where the amount of unbalance in the stator current is calculated from the sub-synchronous to the hyper-synchronous speed for 0.5%, 2% and 4% grid voltage unbalance. A proper estimation of the amount of unbalance in the stator currents is important since unbalanced currents create unequal heating on the stator windings, which may increase winding temperature degrading the insulation reducing life expectancy of the winding. Unbalanced currents also create torque pulsations on the shaft resulting in mechanical stress that also reduces the life expectancy of the wind turbine shaft [99, 106, 107]. The amount unbalance in the rotor current was not calculated because no negative sequence or oscillations were present in this current.

As seen in Fig. 4.13, the DFIG dynamic model can represent unbalanced currents, and as expected, the amount of unbalance is dependent on how severe the grid unbalance is. A quick inspection in *abc* coordinates shows that the estimated and measured unbalance current is similar for all tested grid unbalances, see Fig. 4.13(b,d,f).



(a) Stator currents



(b) Rotor currents

Figure 4.10: DFIG model with iron losses against measurements for rotor and stator currents for 0.5% unbalanced grid conditions.

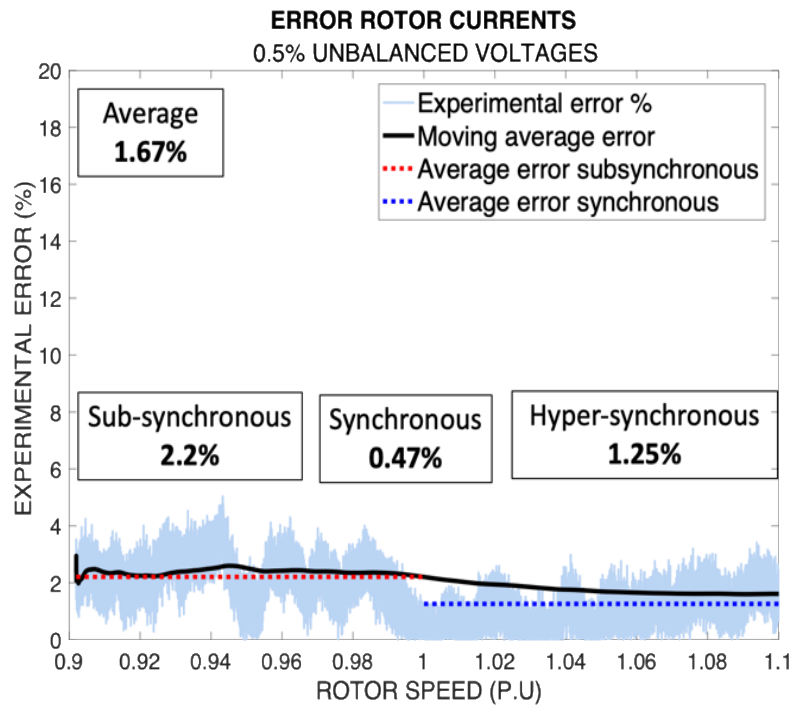
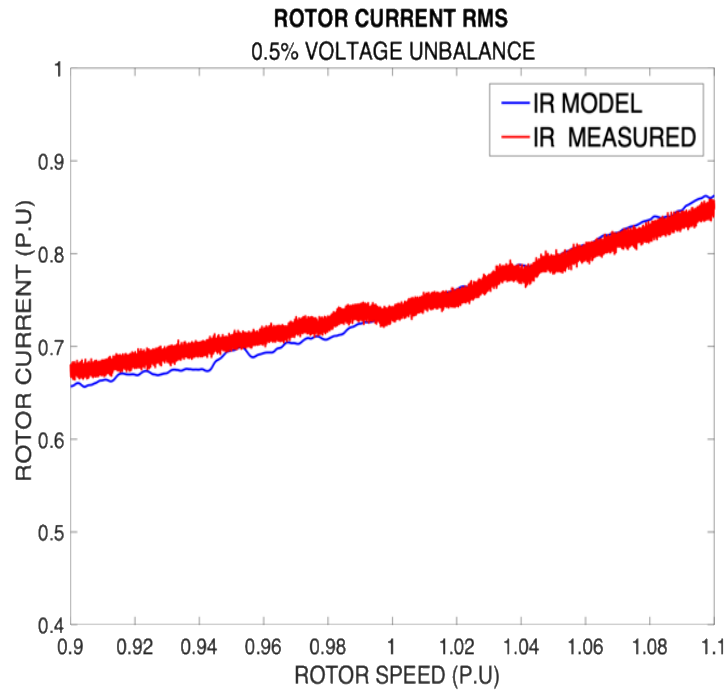
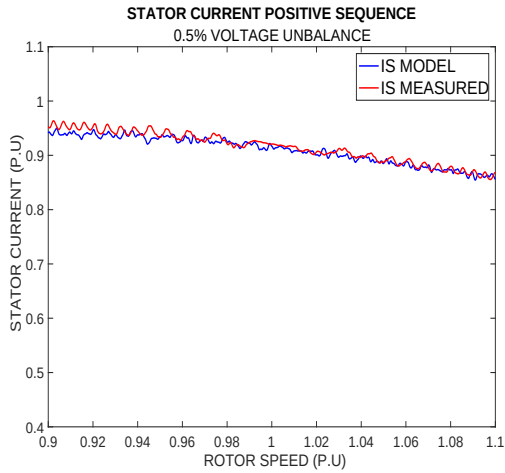
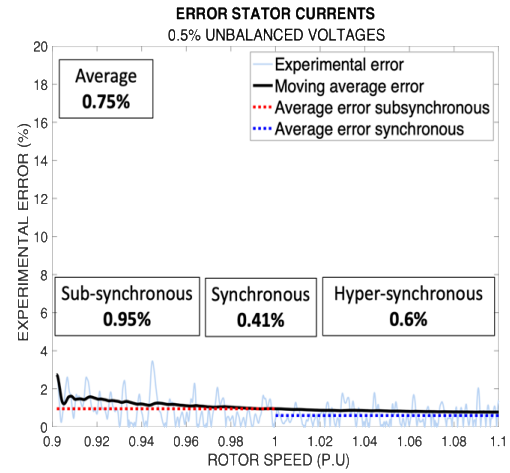


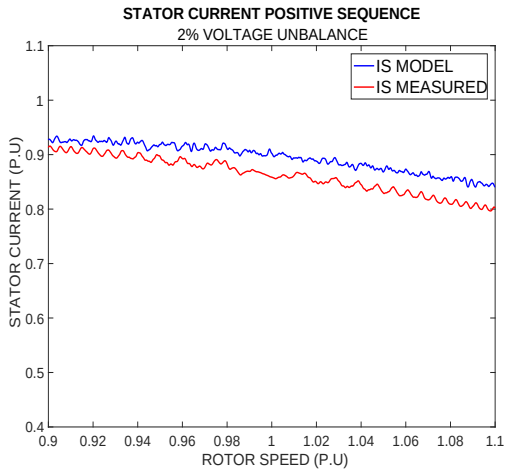
Figure 4.11: Close-loop machine model validation of DFIG rotor currents under 0.5% grid unbalanced conditions.



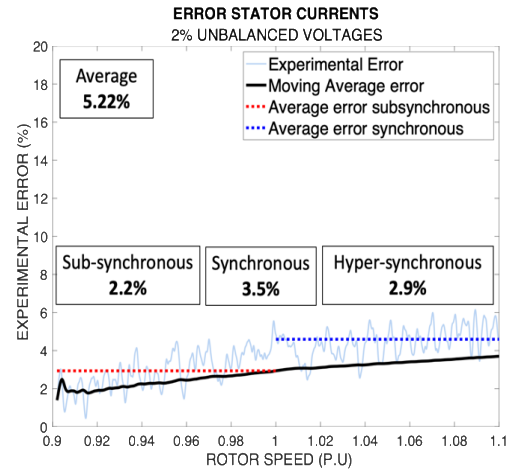
(a) Stator currents under 0.5% grid unbalance



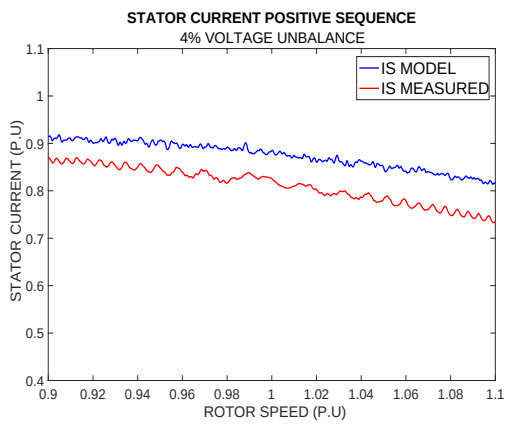
(b) Stator current error under 0.5% grid unbalance



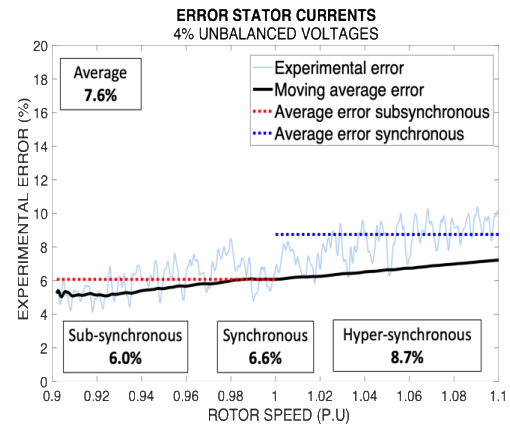
(c) Stator currents under 2% grid unbalance



(d) Stator current error under 2% grid unbalance

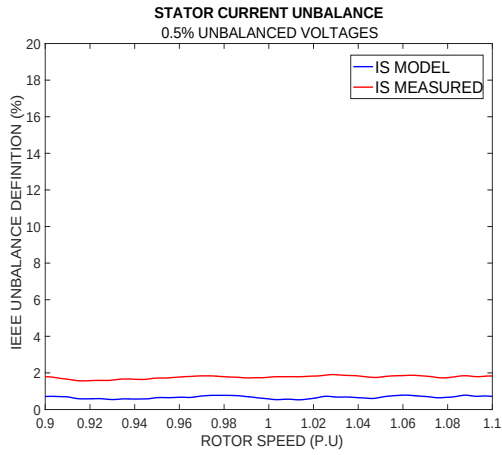


(e) Stator currents under 4% grid unbalance

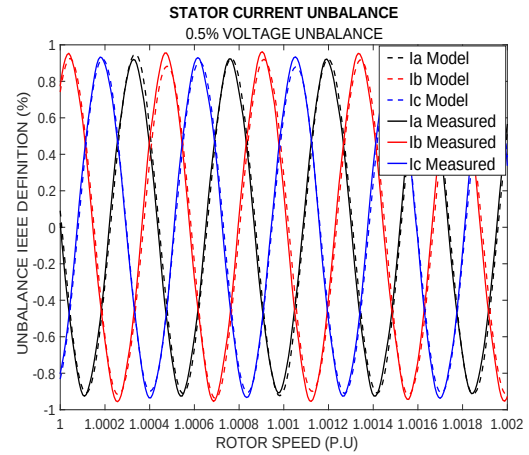


(f) Stator current error under 4% grid unbalance

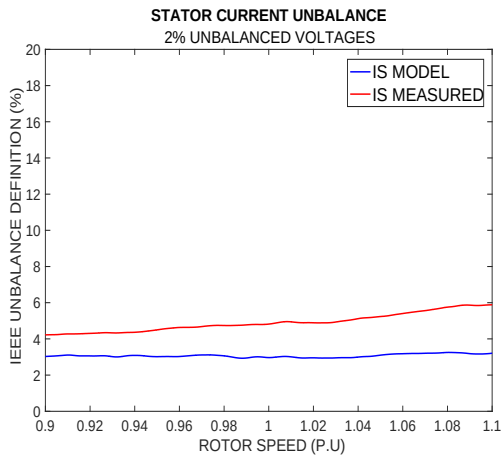
Figure 4.12: Machine model validation of DFIG with iron losses for balanced grid conditions



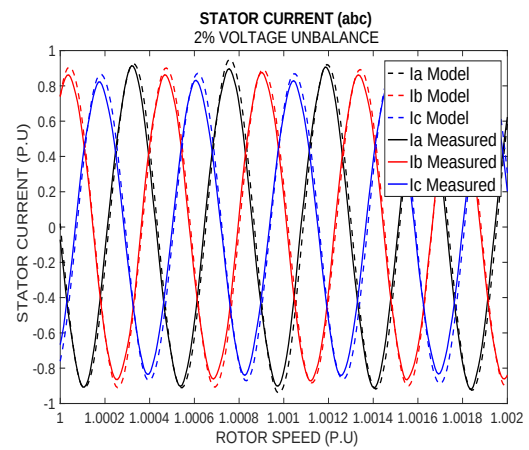
(a) Stator currents unbalance under 0.5% grid unbalance



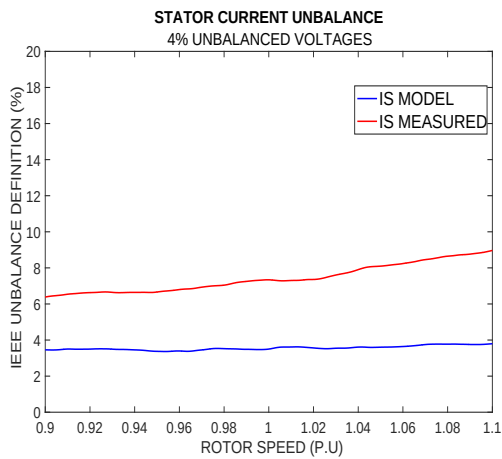
(b) (abc) stator currents under 0.5% grid unbalance



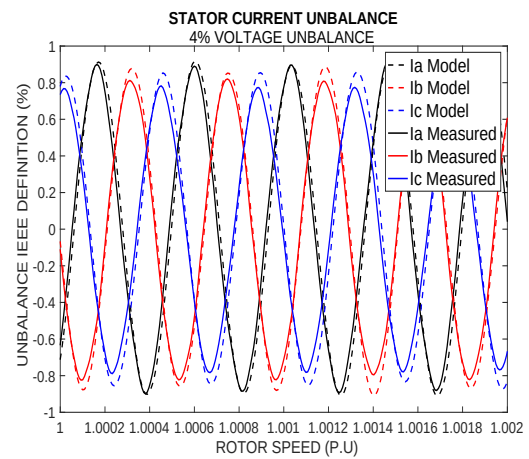
(c) Stator currents unbalance under 2% grid unbalance



(d) (abc) stator currents under 2% grid unbalance



(e) Stator currents unbalance under 4% grid unbalance



(f) (abc) stator currents under 4% grid unbalance

Figure 4.13: Machine model validation of DFIG with iron losses for balanced grid conditions.

The amount of unbalance in the stator current calculated using the IEEE definition show that the percentage of unbalance is underestimated by the model for all the tested grid unbalances, refer to Fig 4.13 (a,b,e). The discrepancy may be the result of physical imbalances in the stator and rotor windings, which would result in different parametrization per phase. For reference, the models that are widely used in the literature such as dqo and $\alpha\beta$ reference frames, as well as the model validated in this chapter, assume perfectly balanced windings. Estimating the machine parameters per-phase is cumbersome.

4.10. Symmetrical Voltage Sags

This section uses the developed and validated real-time simulator to evaluate the behavior of the induction generator during symmetrical voltage dips, and studies two feasible solutions to reduce the effects of voltage dips in the DFIG. The first strategy uses pitch control to reduce the speed of the generator during voltage dips. The second strategy, inspired by [121], modifies the rotor controller to provide zero electromagnetic torque during a fault.

Current regulations require that wind farms must have Low Voltage Ride-Through (LVRT) capabilities. This feature allows wind turbines to remain connected to the power grid during periods of low voltage (e.g., voltage dips), preventing a sudden shortage in the production of active power that could lead to instabilities in the power grid [111]. Fig. 4.14 shows the limits of voltage on which the wind turbine must remain connected to the grid [112]. In the U.S, the FERC Order No. 661 defines the time in which wind turbines should remain without tripping. Wind turbines should have continuous operation for grid voltages at 90% the rated line voltage and should ride through fault for 0.65s for a minimum voltage at 15% the rated line voltage [114]

One of the main competitive advantages of the DFIG is that it provides variable speed with a small and economic power converter. However, this advantage becomes a disadvantage when the DFIG is subjected to a sudden drop in the stator voltage, because a scaled power converter may not be able to take a control action required to control the rotor currents and speed during transients [115]. The effect of voltage dips in induction generators has been

broadly studied [115]-[120]. As presented in the literature, there have been studies to accurately predict the voltages and currents when the machine is subjected to a voltage dip. Various studies have designed protection systems to mitigate the negative effects of these perturbations in the induction machine. Fig. 4.15 shows a bar chart with simulation results that the overvoltage and overcurrent depend on the depth of the voltage dip. In the U.S., the DFIG system must be designed to operate during severe voltage dips limited by FERC order No. 661, which most severe effects are high currents in the stator and rotor circuits.

Figure 4.16 shows the effects of voltage dips in the generator without protection systems. The simulated voltage dip is delimited by FERC Order No. 661. The most relevant effects in the induction machine are the following:

1. A decrease in the stator voltage reduces both the stator and rotor flux, see Fig. 4.17.
2. Reduced fluxes cause the electromagnetic torque to decrease.
3. The reduction in the electromagnetic torque limits the speed controllability of the wind turbine. As shown in Fig. 4.16(f). This increases the error and is amplified by the speed controller PI, leading to an increase in the rotor current reference, Fig. 4.16(c) and (d).
4. The rotor currents and stator currents can reach up to four times their nominal value, as shown in Figure 4.16(d). The rotor voltage experiences a peak during the fault which could destroy the power electronics switches.
5. The DC-Link overvoltage may increase above its designed value as shown in Figure 4.16(c).

4.11. DFIG LVRT Solutions

Two main solutions are presented in the literature to enhance the LVRT capacity of the DFIG wind turbine [121]-[122]: Passive methods include crowbar protection, blade pitch angle control, energy capacitor system and energy storage inverter (ESI). The crowbar protection method has been widely studied. This protection system limits the overcurrent in the rotor that are present during fault conditions [123]-[124]. The crowbar could be resistive or active [115].

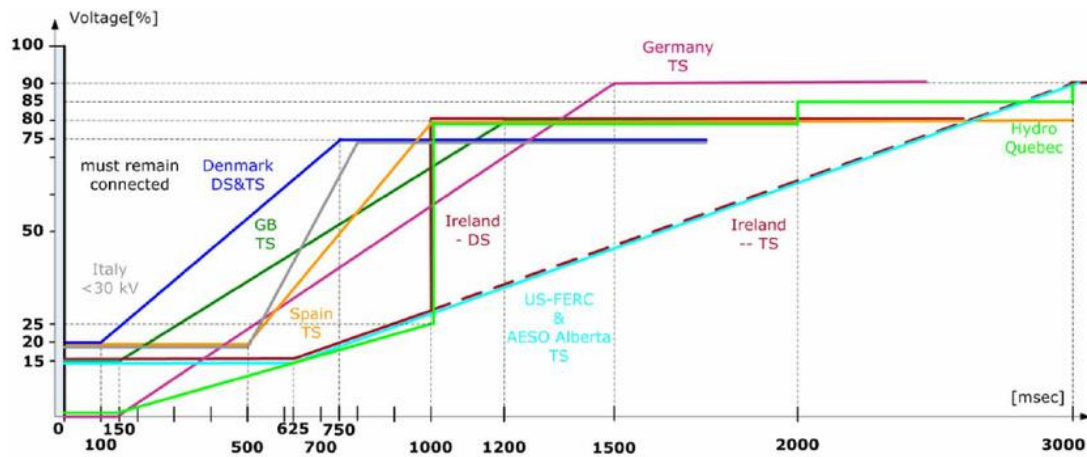


Figure 4.14: LVRT profiles for different countries [152].

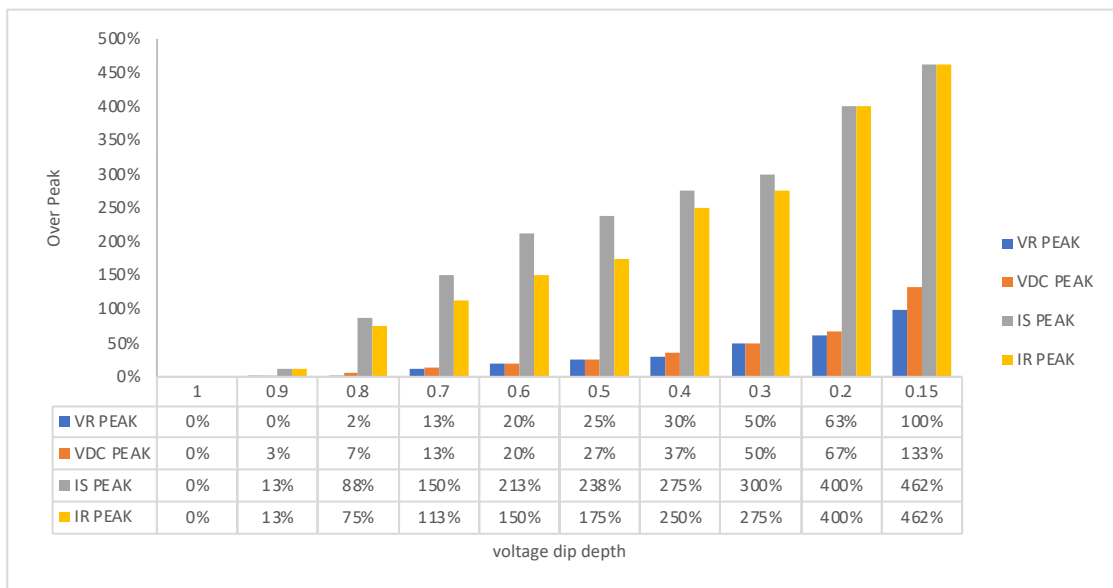


Figure 4.15: Overcurrents and overvoltages during voltage dips. Rotor and stator currents peak values increase with the dip depth. Results from developed real-time simulator.

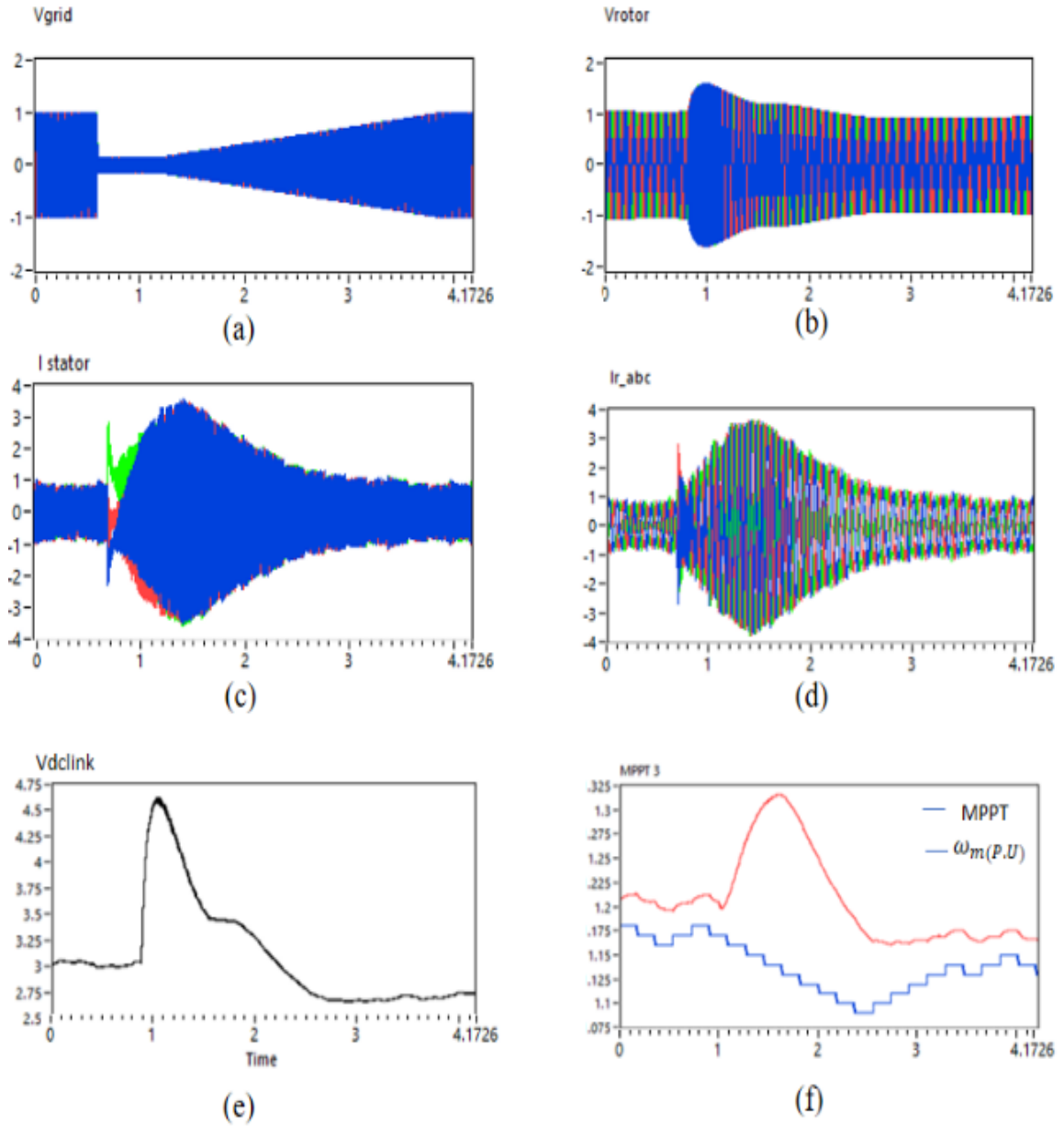


Figure 4.16: Effects of voltage dips DFIG wind turbine without countermeasures. (a) stator voltage follows profile FERC Order No. 661. (b) rotor voltages. (c) stator currents. (d) rotor currents. (e) DC link. (f) MPPT reference and rotor speed. All quantities are in p.u and the x-axis is the time in seconds.

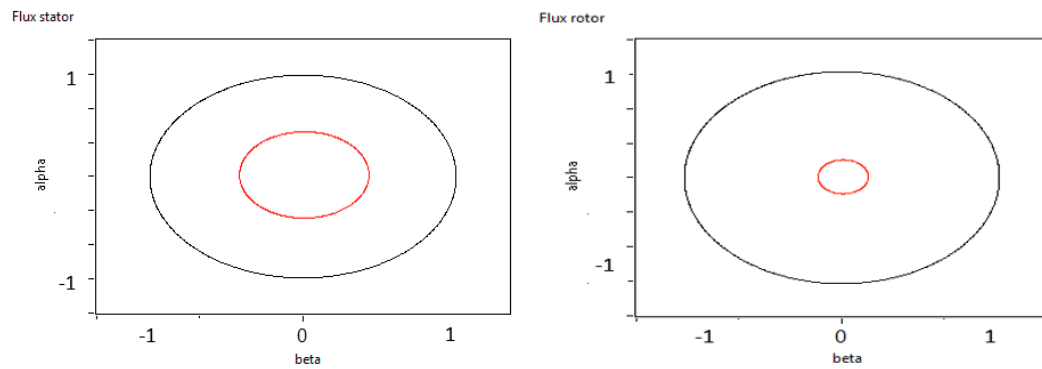


Figure 4.17: Steady state stator and rotor flux after (red line) and before (black line) 0.15 voltage dip.

The crowbar is an effective solution to limit rotor currents; however, as noted in [104], it involves additional investments, energy dissipations by crowbar resistors, and partial loss of control to active and reactive power outputs. Another issue is that when the crowbar is activated, the DFIG will absorb a large amount of reactive power leading to a further grid voltage degradation [122]. Active methods use the control of the rotor converter to mitigate the impact of voltage faults [121]-[125]. This strategy aims to reduce rotor current transients of the induced electromagnetic force in the rotor circuit by controlling the RSC. However, as pointed out in [121], these control strategies raise concerns due their high complexity, and they are not implemented in the industry.

To mitigate the adverse effects of voltage dips in DFIG machine, this section evaluates two different strategies. The first uses the pitch control to limit the speed of the generator. The second modifies the rotor converter to provide zero torque during fault conditions. These strategies are selected because they enhance the LVRT capacity of the DFIG wind turbine, without the need of additional protections such as crowbar.

Fig. 4.18 presents the dynamics of the DFIG during a fault when the pitch controller is used as a protection mechanism. The pitch effectively reduces the speed of the generator, shown in Fig. 4.18(f), and limits the overcurrent present in the stator and rotor circuits. However, this strategy does not reduce the overvoltage in the DC-link, and an improper design can lead to a sudden drop in active power that might affect the stability of the power grid.

Fig. 4.19 shows the second alternative [121], which consists of transforming the energy generated during the dip into kinetic energy, rather than dissipate it in a crowbar. The control strategy in the rotor converter is to set torque zero during the fault, allowing the wind generator to increase speed accumulating kinetic energy. After the fault is cleared, the increased kinetic energy can be transformed into electric power and sent to the grid helping to clear the fault. This technique effectively reduces the overcurrent in the stator and rotor; however, the speed of the rotor and the wind turbine can increase above its rated value, and pitch control becomes necessary to protect the wind generator from over-speeding.

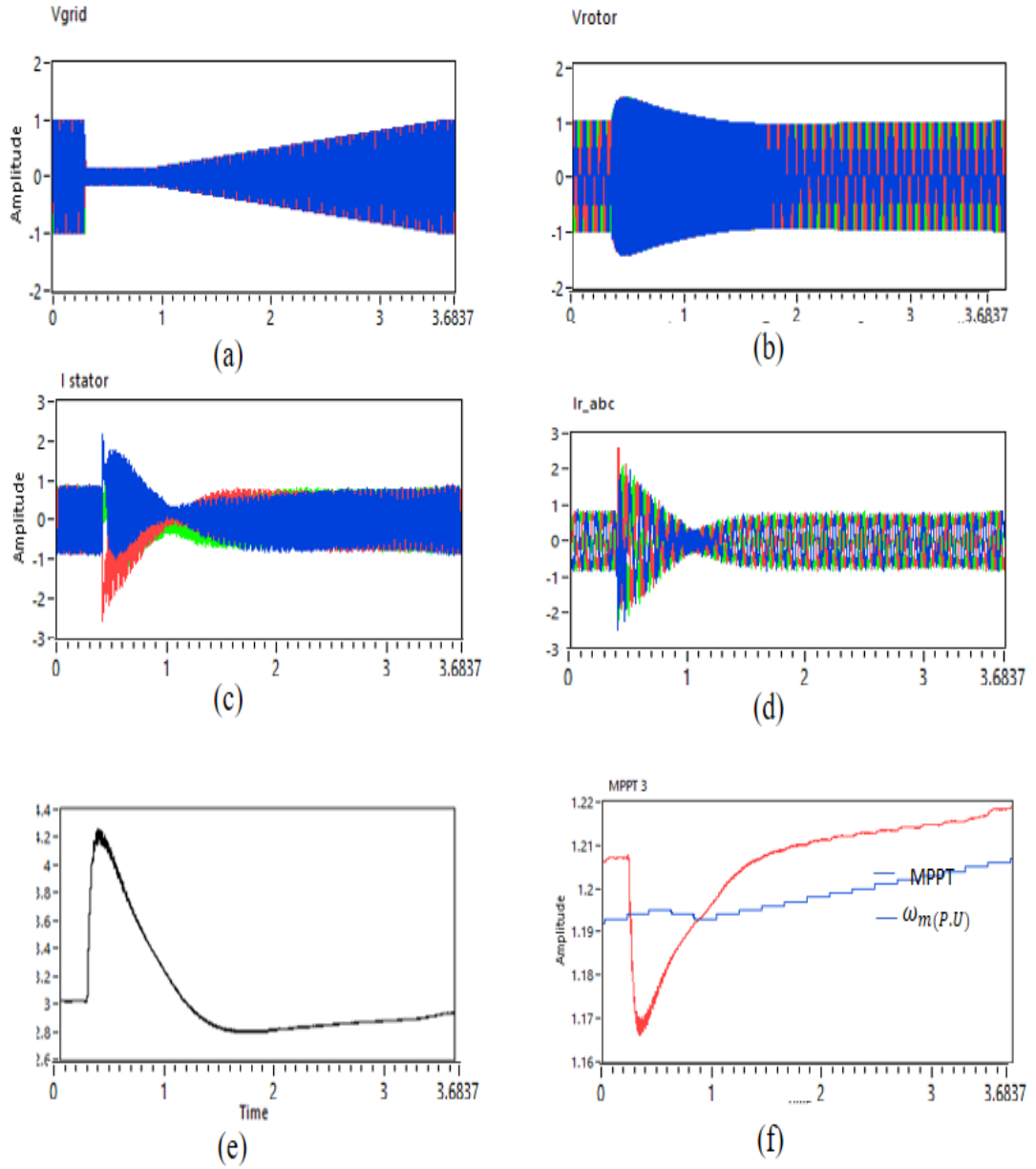
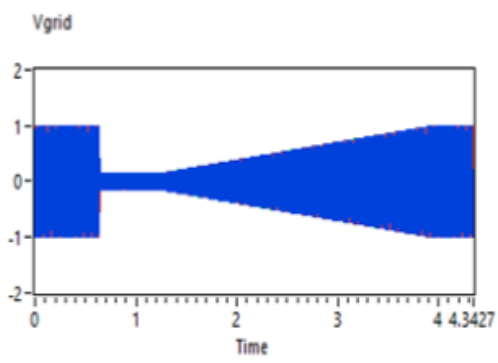


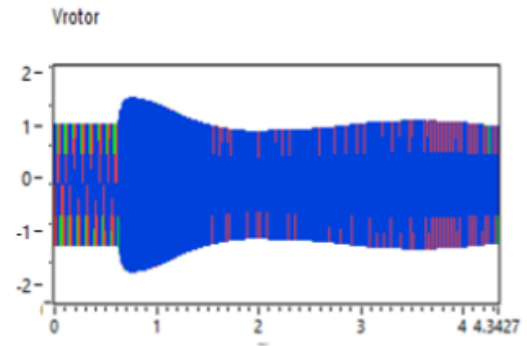
Figure 4.18: First strategy: blade pitch control. (a) stator Voltage, (b) rotor voltages. (c) stator currents. (d) rotor currents. (e) Vdc link. (f) MPPT reference and rotor speed. All quantities are in p.u. and the x-axis is the time in seconds.

4.12. Asymmetrical Voltage Sags

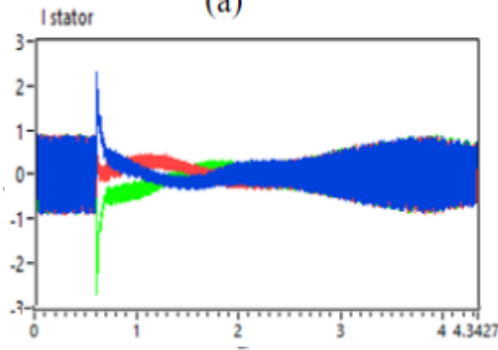
The previous section discussed the effect of symmetrical voltage dips. This section uses the real-time simulator to study the negative effect of voltage imbalances in the DFIG wind turbine. An unbalanced condition in an electric power system is often caused by unbalanced loads, unbalanced system faults, circuit breaker malfunctions, and open phases. Asymmetrical voltage faults, like single-line-to-ground short circuit, is the most common electric fault in the electric network [115]. Currently in the U.S., there is no relevant requirement related with voltages imbalances for wind turbines [113]. However, NERC recommends PRC-024 to define the performance requirements for unbalanced as well as balanced faults. It is important to note that severe unbalances are not typical in grid tied DFIG as grid standards across the globe have specified the suitable limit for voltage unbalance for wind. These standards generally vary between 1% and 2% [127]. The main effects of voltage imbalances observed during simulation are unbalanced currents, oscillations in the fluxes and in the DC-link, see Fig. 4.20-4.21. The most adverse effect of voltage unbalances is the oscillations in the electromagnetic torque that could reduce the lifetime of the wind turbine. Imbalances in the stator voltages can affect the stability of the control. Fig. 4.22 shows a comparison between two typically used reference frame orientations, Stator Flux Orientation (SFO) and Stator Voltage Orientation (SVO). The SFO estimates the flux using and align the d-axis to it. The second option aligns the q-axis with the stator voltage and delays 90 degrees the d-axis. Both techniques are similar if the stator voltages are balanced, however during asymmetrical voltage dips the flux oscillates notably causing an inadequate angle estimation if SFO is used. However, SVO calculates the angle using a phase locked loop (PLL) that considers only the positive sequence of the voltage. Various control objectives can be implemented to reduce these effects, including a) mitigation of stator active and reactive power oscillations, b) reduction of ripple in the electromagnetic torque, c) reduction of the rotor current oscillation, d) reduction of RMS value in rotor currents. For instance, some authors [128,132] proposed to modify the RSC to decrease oscillations in the electronic torque while the GSC is used to cancel oscillations in the DC-link when the DFIG is subjected to asymmetrical voltage dips.



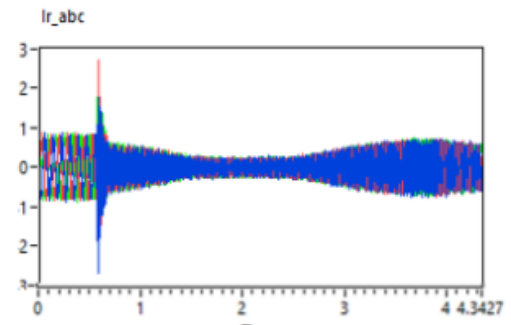
(a)



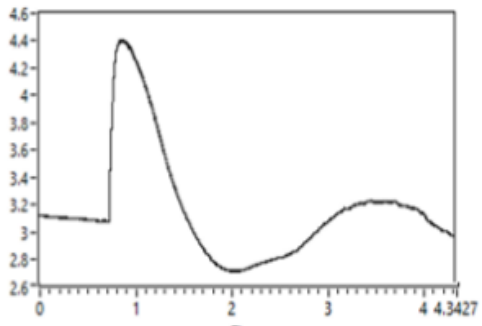
(b)



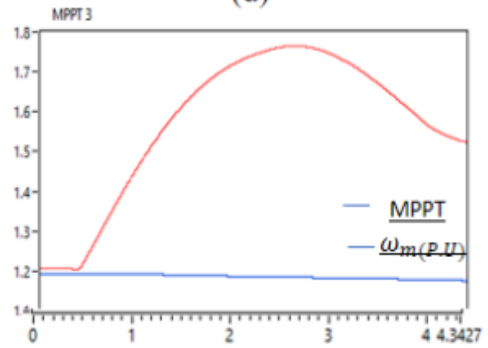
(c)



(d)



(e)



(f)

Figure 4.19: Second strategy: zero torque control. (a) stator voltage. (b) rotor voltages. (c) stator currents. (d) rotor currents. (e) Vdc link. (f) MPPT reference and rotor speed. All quantities are in p.u. and the x-axis is the time in seconds.

4.13. Conclusions

This chapter presented the development and the model validation of a real-time emulator of doubly fed induction generator (DFIG) wind turbine system. The code of the real-time DFIG dynamic model with iron losses, back-to-back model, mechanical model, and aerodynamic model were addressed in detail. The proposed discrete-modelling approach for real-time applications provides a flexible platform that can be utilized for analyzing and testing grid-connected DFIG systems. The discrete-time modeling and the implementation process results in a platform-independent model that is suitable for the application on any RT platform, such as RT computers, or programmable digital devices like DSPs or FPGAs.

The model validation was presented under different grid unbalances and for speeds ranging from the sub-synchronous to hyper-synchronous operation. These preliminary results showed that the DFIG model provides a good representation of the generator stator and rotor current positive sequence over a wide operating range and grid unbalances. However, the model underestimated the amount of unbalance in the stator currents, an error that increased relative to the grid unbalance. This discrepancy may be the result of asymmetries in the windings of the machine used for this study. Further research with a larger machine is necessary to further verify the validity of the model under unbalanced conditions.

Simulations demonstrate that the developed real-time simulator can be used to study the complex dynamics of the DFIG operating under balanced and unbalanced voltages, as well the dynamic response of the machine under symmetrical and asymmetrical voltage sags. This hardware based real-time simulator is a flexible and reliable platform that can be utilized to test control strategies before their implementation in real hardware. Finally, all the models used for the real-time simulator were uploaded in a public repository and are available to the public [133].

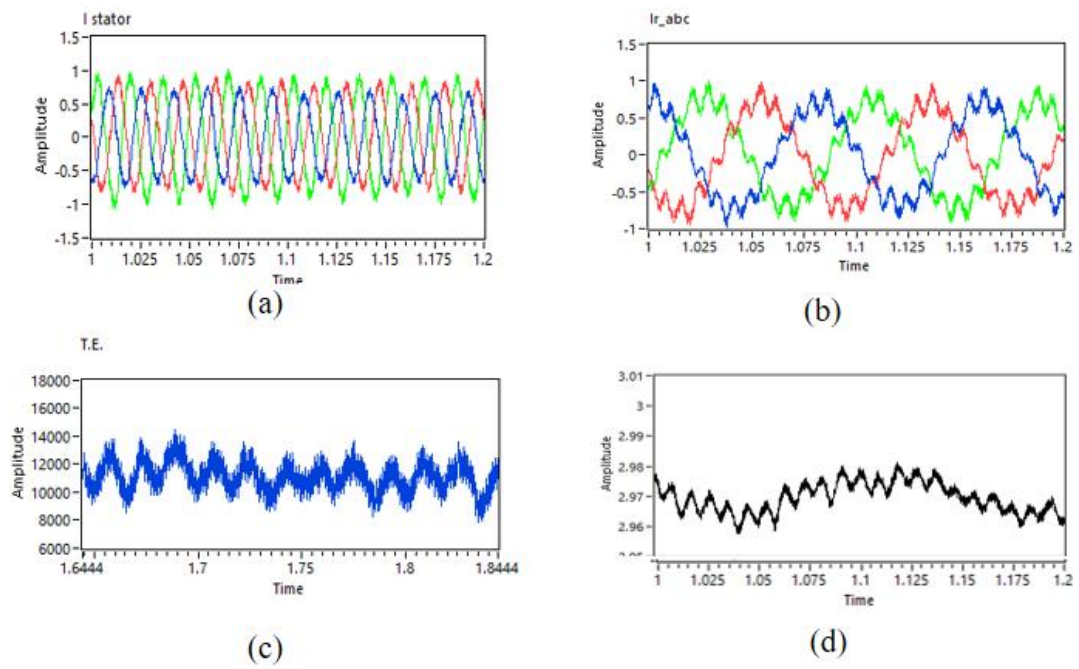


Figure 4.20: Effects voltage unbalance DFIG (a) Stator current (p.u), (b) Rotor current (p.u). (c) Electromagnetic torque (N.m). (d) Vdc link (p.u). X-axis is the time in seconds.

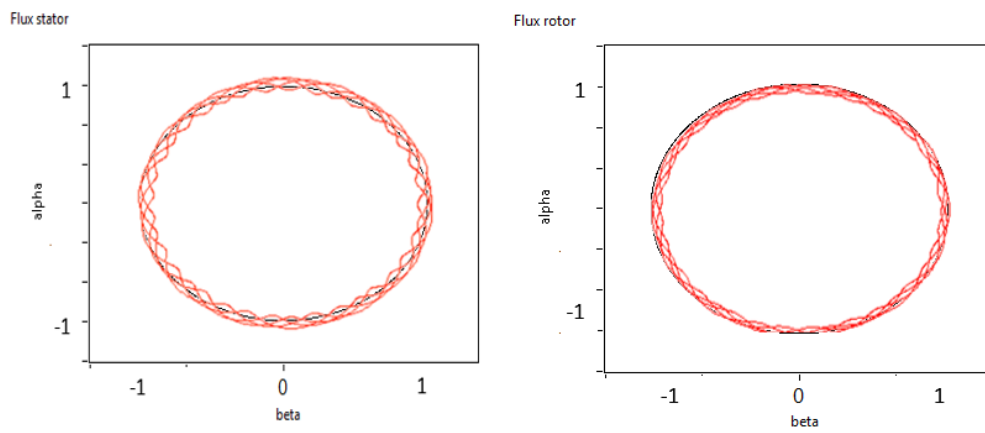


Figure 4.21: Steady state stator and rotor flux after (red line) and before (black line) 2% grid voltage imbalance.

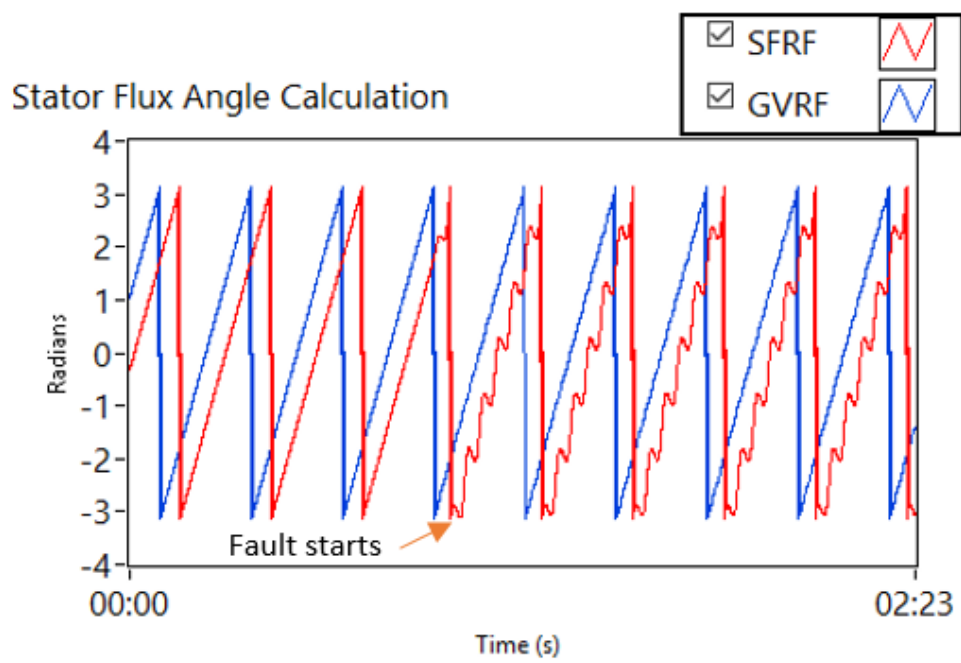


Figure 4.22: Estimation of stator flux during heavy voltage imbalance using GVRF and SFRF.

CHAPTER 5
PV INVERTER DESIGN WITH ENHANCED REACTIVE POWER
SUPPORT

Abstract: This section proposes to apply the hardware modifications presented in chapter 1 to a grid-tied photovoltaic (PV) inverter. Increasing the current from PV inverters will allow it to ride through faults while enhancing their reactive power support during voltage sags. The proposed design consists of oversizing the semiconductor current rating to allow transferring the energy from the dc side to the ac side during voltage sags. This modification maintains the stability of the dc-link voltage during voltage sags of different magnitudes while significantly enhancing the ancillary service capabilities that the inverter can provide. Oversizing the power semiconductors brings the additional benefit of improving the inverter efficiency, significantly reducing the conduction losses during both normal operation and grid fault conditions. Through electrothermal simulations it is shown that the proposed design is capable of injecting three-times the inverter rated current for enough time to comply with the low-voltage ride through requirements (LVRT) requirements established by IEEE 1547, 2018. Furthermore, the enhanced current capability allows the inverter to provide additional reactive power support during grid events.

5.1. Introduction

High penetration of distributed grid-tied PV inverters brings concerns about the voltage and frequency regulation. Short-duration voltage sags that last a few milliseconds can take PV inverters offline for a few minutes. As shown in [134], PV tripping during faults may create cascading effects in the transmission grid in areas where there is a high penetration of PV installations. Grid operators manage transients by static compensation techniques e. g., static synchronous compensator (STATCOM), which adopt large inductive/capacitive arrangement to provide reactive power injection to compensate for the voltage sag/swell. Although this has been proven efficient for high power centralized generators, these solutions are not feasible when high number of independent distributed generation are present.

Based on IEEE 1547, PV inverters should remain connected during low-voltage sags of different magnitudes [135]. Because PV inverters limit their current injection to about (1.0.

p.u. to 1.2 p.u.) of their rated current during voltage sags, this limited current injection creates an energy imbalance between the ac and the dc side [136], [137]. Because the inverter cannot transfer all the power available to the grid, the power surplus flows through the dc-link capacitor bank, which increases the dc-link voltage. Increasing the dc-link voltage moves the current-voltage (I-V) curve close to the open-circuit voltage (V_{oc}) of the panels and reduces the power injected from the panels. To tackle this problem, conventional low-voltage ride through (LVRT) methods limit the output current and disable the Maximum Power Point Tracking (MPPT) during the fault to compensate for the energy surplus [138]. For instance, the authors in [139], propose a low-voltage ride through (LVRT) technique for a 20% voltage sag. To maintain stability, they propose to disable the MPPT while the first stage boost converter is set to operate with a fixed duty cycle. However, as noticed in [140], the downside of this method is that the duty cycle depends on the magnitude of the voltage sag. During severe voltage sags, the boost converter may shift from continuous to discontinuous mode, introducing fluctuations to the dc-link. Other authors have proposed a more traditional approach such as crowbar circuits [141], dynamic resistors, or DC-choppers to dissipate power from PV that cannot be supplied to the grid [142]. Other methods include storing the energy surplus using supercapacitors or other energy storage devices. These methods avoid the unnecessary dissipation of renewable energy by storing the surplus energy during a fault and then release it back to the grid after the fault clearance. This energy storage can provide additional functions such as reactive power support and flicker compensation by maintaining the inverter DC-link voltage constant. Authors in [140] propose a design to provide LVRT during voltage sags while keeping the MPPT in operation. During the sag, the authors tackle the problem of energy unbalance by harvesting DC-link excess energy into the battery. Although this method maintains stability and operation at the MPPT, the method can only be applied to hybrid inverters, which require expensive batteries and additional power electronics. Furthermore, energy storage has a much shorter lifetime than the PV components, and additional routines are needed in its daily operation. Other challenges include the applicability of this method if the battery is fully charged, which may be a desirable condition for microgrid applications to prepare the inverter for unintentional islanding condition.

This section proposes a different approach which has not been addressed previously in the literature, which consists of oversizing the current rating of the semiconductor module to allow the PV inverter to inject the surplus energy back to the grid during voltage sags. With this method the power balance is maintained, and the voltage in the dc-link capacitor is nearly constant while the PV supplied inverter operates at its MPP. Furthermore, increasing the inverter current rating significantly increases the ancillary services the inverter can provide. This is important during voltage dips events as it would be desirable to inject as much reactive power to the grid to support the voltage recovery process. The authors of this work have demonstrated with experimental results that oversizing the semiconductor and the current transducer is sufficient to significantly increase the fault contribution of energy storage inverters [143]. As an extension to this previous work, this work applies a similar methodology to PV inverters to improve their low-voltage ride through capabilities.

The advantages of the proposed method are: 1) enhanced ancillary support during voltage sags; 2) higher use of renewable energy as all active power is injected back to the grid during voltage sags; and 3) sag-depth independent LVRT and stable dc-link voltage control with MPPT during sags. The proposed solution is cost effective compared with solutions that incorporate energy storage because only a few inverter components are required to be oversized. Based on [143, 144], the proposed method would increase the cost of the inverter by ~8.7%. This additional cost can be offset because devices with higher current capability have better thermal characteristics and lower losses than devices rated at lower currents. This added benefit improves the efficiency of the inverter and may reduce the cooling requirements of the inverter.

5.2. Voltage Sags on PV inverters

Fig. 5.1 shows a simplified diagram to illustrate the energy imbalance during a voltage sag applied to a three-phase PV inverter. It is assumed that the PV inverter is operating at the maximum power point (MPP), and that the inverter has the same power rating as the PV array. Fig. 5.1(a) shows that during normal condition, the PV inverter maximizes the energy injected to the grid, and the power injected to the grid is equal to the power at the MPP

minus the inverter losses, which are neglected in this work. Because the energy balance is maintained during normal operation, the DC-link voltage is constant and there is no power through the capacitor during steady state operation. Fig. 5.1(b) illustrates the power imbalance that is created when a voltage sag of magnitude δ is applied, where $\delta = 0$ means zero voltage at the point of common coupling (PCC). Because the PV inverter current is limited to 1.0. p.u., the inverter cannot inject all the power from the PV panels back to the grid. The only path for the surplus power from the PV panels is the inverter's dc-link capacitor. Because the voltage in the capacitor is the integral of the current, this excess current is integrated increasing the voltage in the dc-link. Fig. 5.1(e) plots the power through the capacitor for different voltage dip magnitudes; the power through the capacitors increases as the voltage sag deepens. Finally, Fig. 5.1(c) shows the inverter reaching a new equilibrium point. Here, the DC-link voltage corresponds the voltage in the I-V curve that balances the power between the ac and dc side.

Fig.5.1(d) shows that the dc-link voltage depends on the magnitude of the voltage sag. To calculate the dc link voltage, the current that flows through the capacitor during a voltage sag must be known. Applying Kirchhoff's Current Law (KCL) to the dc-link circuit of Fig. 5.1(a)

$$I_C = I_{PV} - I_{ac_dc} \quad (5.1)$$

where I_C is the current through the DC-link capacitor, I_{PV} is the current from the PV array, and I_{ac_dc} the inverter side dc current. Assuming a lossless inverter, and that the power rating of the inverter is equal to the PV array maximum power $P_{inv} = P_{MPPT}$, the maximum rms ac current I_{ac_max} of the inverter can be calculated by (2), where V_{phn} is nominal ac phase voltage and P_{MPPT} the maximum power point of the PV array.

$$I_{ac_max} = \frac{P_{MPPT}}{3V_{phn}} = \frac{P_{MPPT}}{3\delta V_{phn}} \quad (5.2)$$

Based on this maximum current allowed by the inverter, the maximum current that can go through the dc side can be calculated using (5.3).

$$I_{ac_dc} = \delta \frac{I_{ac_max} V_{phn}}{V_{dc}} \quad (5.3)$$

Where V_{dc} is the dc-link voltage. As mentioned, during voltage sags, the inverter current is regulated to I_{ac_max} to ~ 1.0 pu. However, I_{ac_dc} decreases as the dc-link capacitor charges, moving the PV panel out of the MPP. The current available from the PV array can be calculated using (5.4) [145],

$$I_{PV} = \left(I - I_0 \left[\exp \left(\frac{V + R_s I}{V_t a} \right) - 1 \right] - \frac{V + R_s I}{R_p} \right) \quad (5.4)$$

where I is the current generated by the incident light, I_0 is the saturation current of the array, $V = N_s kT / q$ is the thermal voltage of the array with N_s cells connected in series. If the array is composed of N_p parallel connections of cells, the photovoltaic and saturation currents may be expressed as: $I = I_{cell} N_p$, $I_0 = I_0 N_p$. R_s is the equivalent series resistance of the array, and R_p is the equivalent parallel resistance.

Finally, the dc-link capacitor voltage can be obtained by combining (5.2-5.4). Notice that the dc-link voltage is needed to calculate the current from the panels, this dependency can be easily implemented in simulation software with a feedback loop or a time-delay.

$$V_{DC} = \frac{1}{C} \int \left(\left(I_{PV} - I_0 \left[\exp \left(\frac{V + R_s I}{V_t a} \right) - 1 \right] - \frac{V + R_s I}{R_p} \right) - I_{ac_dc} \delta \right) dt \quad (5.5)$$

Fig. 5.1(d) shows the validation of (5.5) by comparing it with the full model of the PV inverter simulated in Matlab Simulink, where a good fit was obtained validating the analytical expression.

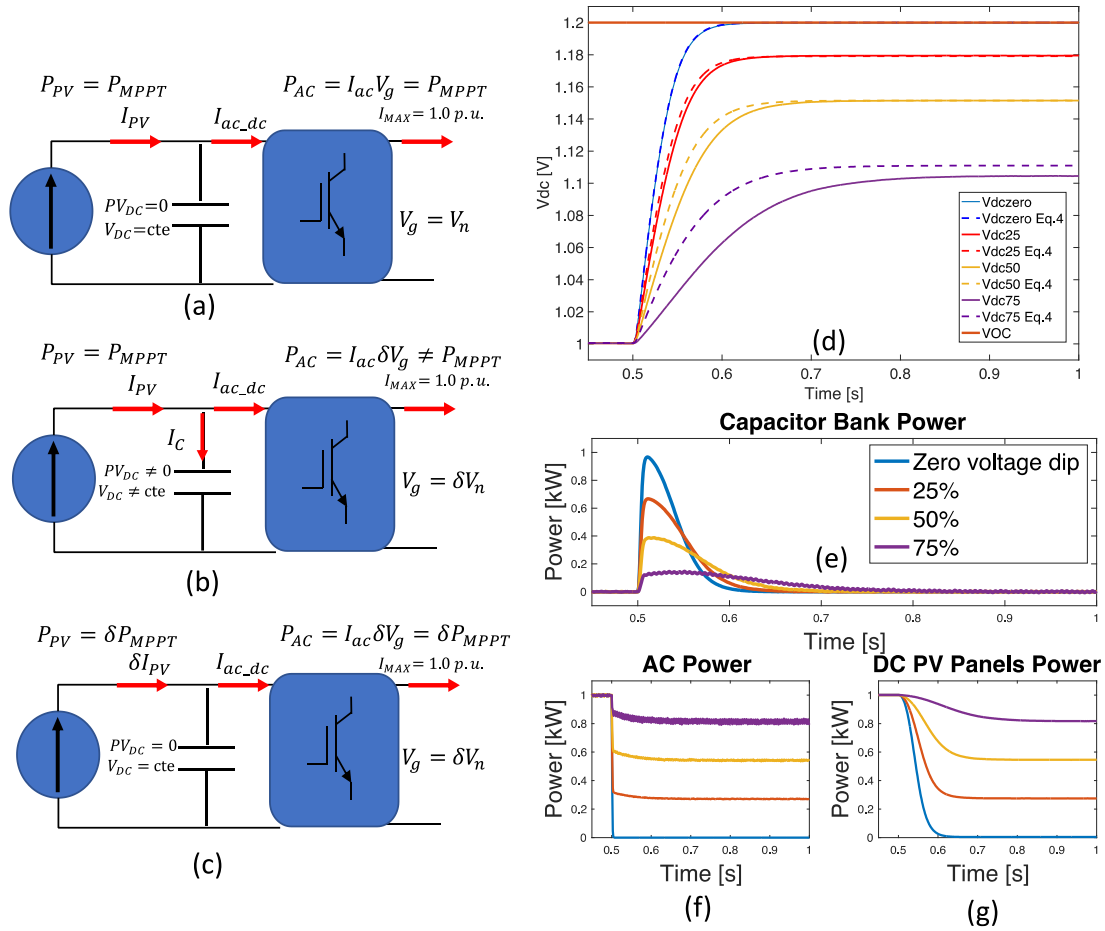


Figure 5.1: PV inverter power during sags. (a) normal operation, (b) immediately during a voltage sag, (c) after reaching new power balance setpoint, (d) dc-voltage for different voltage dip magnitudes, (e) capacitor bank power, (f) ac power, (g) PV power.

5.3. LVRT of Commercial Inverters

This section evaluates the LVRT response of a commercial inverter under different voltage dips. Fig 5.2 shows the Category III LVRT curves of the IEEE 1547 2018 revision. There are three main operating zones: I) continuous operation for voltages between 0.88-1.1 p.u, II) Mandatory operation for voltages between 0.5 and 0.88 p.u. III) Momentary cessation for voltages lower than 0.5 p.u. Fig. 5.3 shows the experimental testbed and Fig 5.3 shows experimental results obtained from a 24kW, 480V three-phase commercial PV inverter. For this test, the PV inverter was subject to four voltage dips: $\delta = [90,70,50,40]\%$. The voltage dip was programmed in a 100kW regenerative grid emulator NHR 9410. Fig. 5.3 shows the 480V hardware testbed used for obtaining the experimental results with the experimental inverters. Fig. 5.4 shows the LVRT response of the three-phase, 480V Fronius Symo Advanced 24kW. Fig. 5.4(a) shows the results for a voltage dip of 90%. Here, the inverter does not trip and has continued operation as specified by the regulation. For a 70% dip the inverter trips two seconds after the fault was applied. Similarly, for a 50% dip the inverter remains connected for 2 seconds before tripping. Finally, when for a voltage dip lower than 50%, the inverter quickly disconnects after 7 cycles, or approximately 130ms. These results show the challenges introduced by commercial PV inverters. Firstly, the inverter current injection during fault is very limited and remains regulated close to the pre-fault. Secondly, the inverter quickly disconnects in few cycles for low grid voltages, such as the one caused by nearby grid faults. This lack of current injection during events limits the ancillary services the inverter can provide and makes short-circuit protection challenging for networks with high penetration of PV generation.

5.4. Proposed Design to Enhance Grid Support During Voltage Sags

The previous section described some of the challenges of riding through faults with PV inverters, which include overvoltage on dc-link voltage caused by power imbalances and limited current contribution of PV inverters during voltage sags. As a solution, this section proposes to oversize the power module (IGBTs and freewheeling diodes) to inject the available PV energy from the dc-side to the ac-side during the voltage sags.

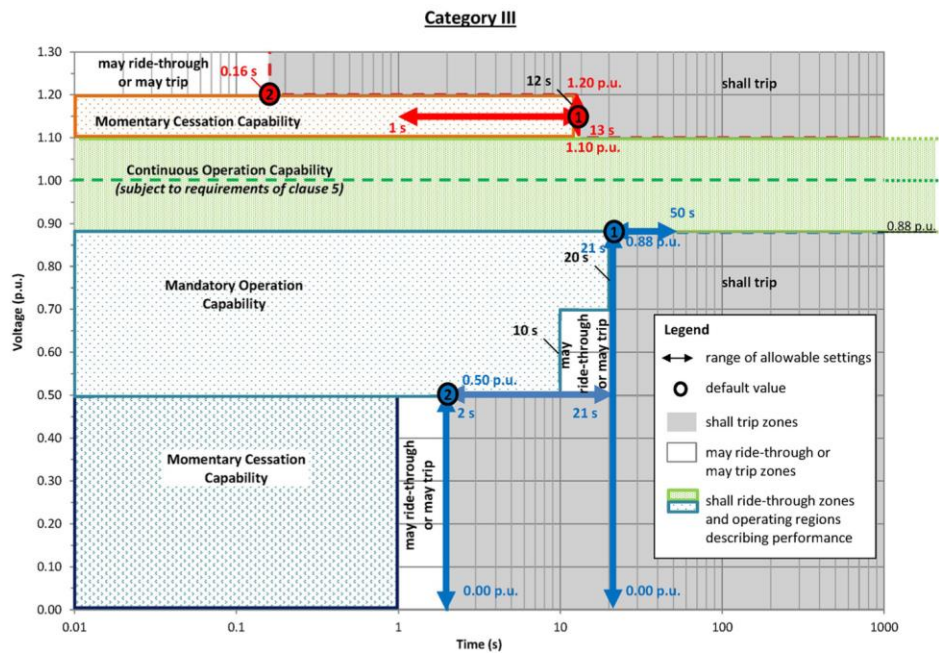


Figure 5.2: DER response for abnormal voltages and voltage ride-through requirements for DERs, Category II, IEEE 1547, 2018 [135].

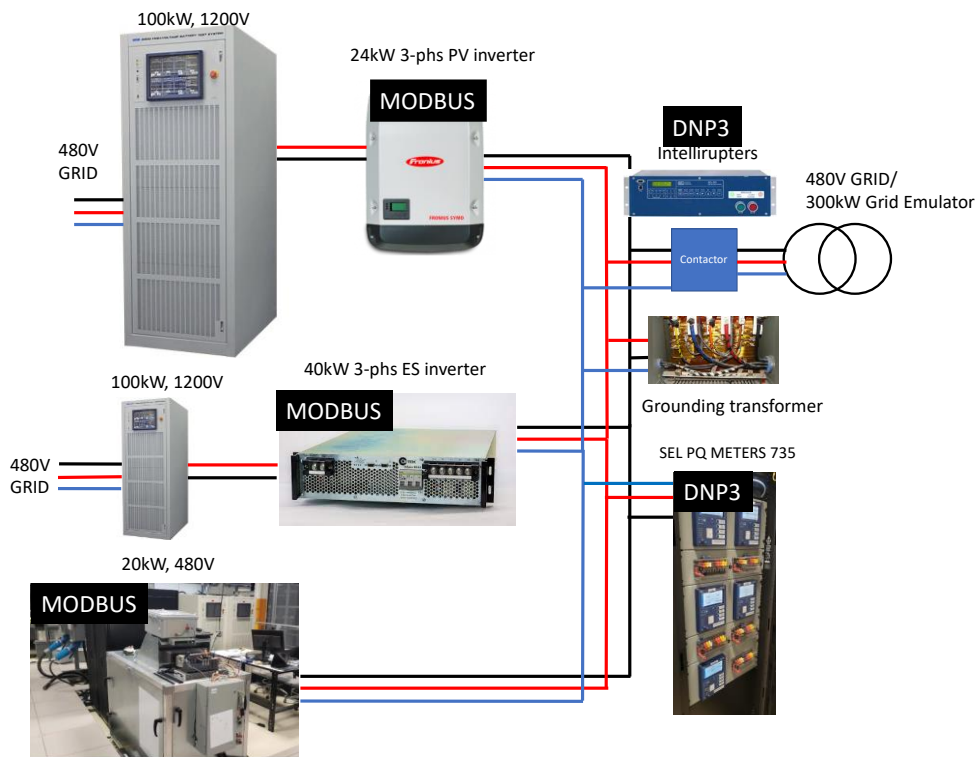


Figure 5.3: ORNL Microgrid Testbed. Consisting of PV inverter, energy storage inverter, synchronous machines, metering and protective devices connected to a 300kW grid emulator. Only PV inverter, PV emulator and grid emulator were used for this research.

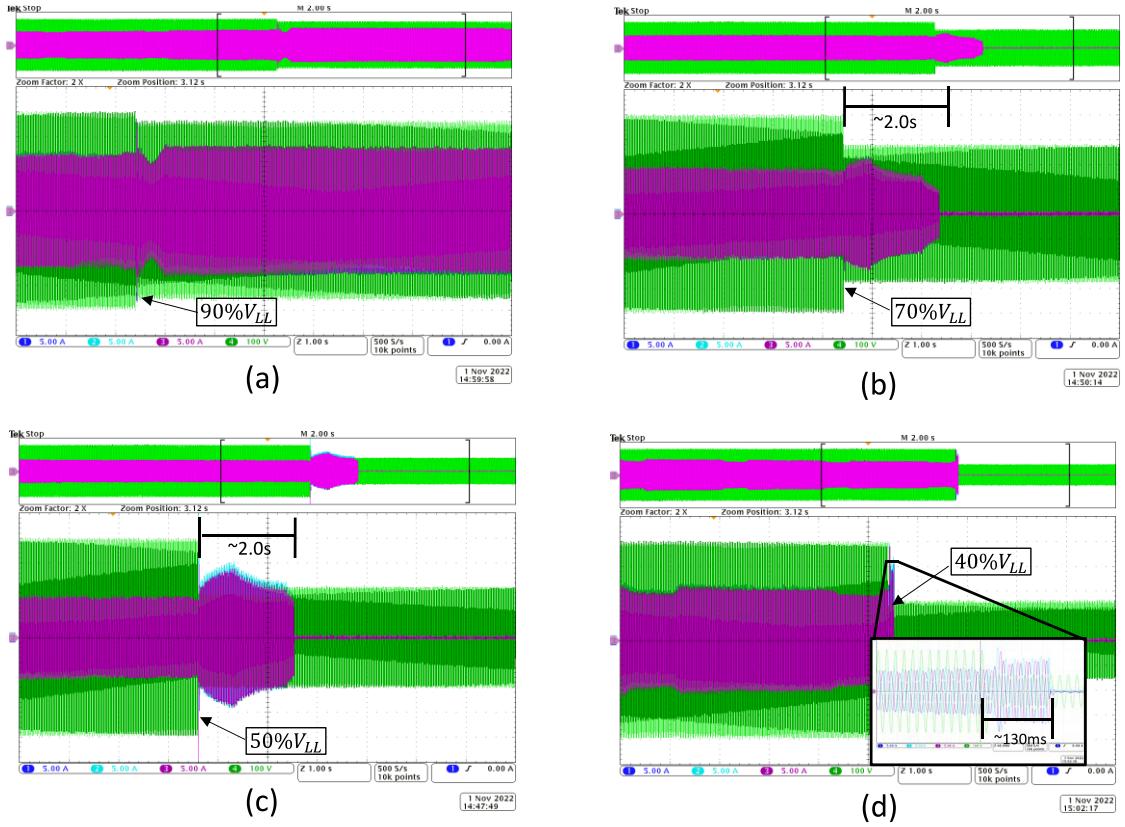


Figure 5.4: LVRT response of commercial PV inverter for a [90%,70%,50%,40%] voltage dip, where 100% is equal to normal operation.

This section follows a similar methodology as the one introduced by the authors in Chapter 3 and applies the proposed modification on a PV inverter. Increasing the current contribution from the inverter would maintain the power balance during voltage sag, allowing the dc-link would remain regulated at the MPPT. More importantly, the inverter with overrated current would provide additional current back to the grid to support the grid recovery.

Equation 5.2 shows that for a voltage dip of 50% ($\delta = 0.5$), the inverter should inject twice its nominal current $2I_{ac_max}$ to transfer all the dc-power back to the grid. Fig. 5.5 shows simulation results that show the efficacy of this method for a voltage dip of 50%. Fig. 5.5(a) shows the result limiting the current of the inverter to 1.1 p.u., and Fig. 5.5(b) shows the results limiting the current to 2.0 p.u. The saturation of the dc-link controller was increased from 1.0 to 2.0 to increase the maximum current allowable [143]. Fig. 5.5(a) shows that limiting the current to 1.1 p.u. causes an energy imbalance between the inverter active power and the dc-power from the PV panels. The excess current flows through the capacitor bank, which is integrated increasing the dc-link voltage. For this simulation, the MPPT was disabled for the duration of the sag to prevent erroneous setpoints during the voltage recovery. Fig. 5.5(b) shows that increasing the current capability allows the inverter to inject all the current back to the grid, maintaining inverter power balance, and the dc-link voltage constant with the PV panel at its MPP.

5.5. Power Losses During Reactive Power Support

This section develops an electrothermal model to estimate the temperature response of the power module during low voltage ride through. In an inverter, the power losses can be divided into conduction and switching losses of the IGBTs and their associated anti-parallel diodes. For sinusoidal PWM (SPWM), the power losses for the IGBT as [145, 146,149].

$$P_{IGBTCond} = V_{TO}I \left(\frac{1}{2\pi} + \frac{m_a \cos(\phi)}{8} \right) + R_{CE}I^2 \left(\frac{1}{8} + \frac{m_a \cos(\phi)}{3\pi} \right) \quad (5.6)$$

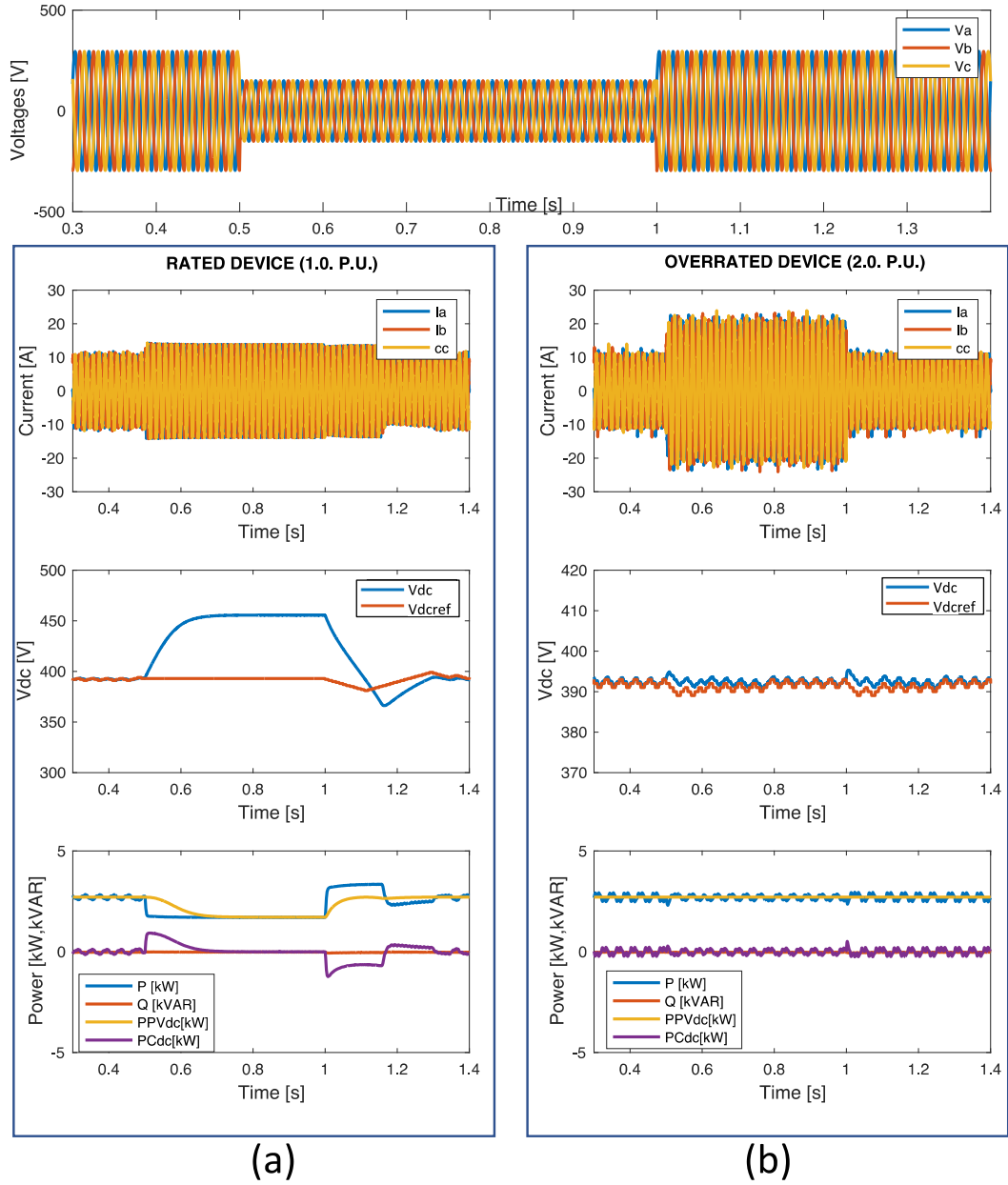


Figure 5.5: Simulation results. (a) PV inverter with maximum ac current rated at 1.0. p.u., (b) inverter with proposed overrated power module to provide maximum ac current of 2.0. p.u.

The power losses for the diode and the switching losses can be calculated using (5.7), and the switching losses using (5.8) [145, 146, 149].

$$P_{DiodeCond} = V_{FO} I \left(\frac{1}{2\pi} - \frac{m_a \cos(\phi)}{8} \right) + R_{AK} I^2 \left(\frac{1}{8} - \frac{m_a \cos(\phi)}{3\pi} \right) \quad (5.7)$$

$$P_{SW} = \frac{(E_{on_peak} + E_{off_peak}) f_{sw}}{\pi} \quad (5.8)$$

where the IGBT on-state resistance $R_{CE} = \Delta V_{CE} / \Delta I_C$ and diode on-state resistance $R_{AK} = \Delta V_{FM} / \Delta I_{FM}$. V_{CE} is the IGBT collector emitter voltage, I_C collector current, and V_{FM} is the diode forward voltage and I_{FM} diode forward current. ϕ is the phase angle between the inverter's output voltage and current, m_a is the pulse width modulation (PWM) amplitude modulation index. E_{on_peak} and E_{off_peak} are the switching turn on and turn off energies. Notice that the conduction losses (5.6) and (5.7) depend on the power factor $\cos(\phi)$; this is shown graphically in Fig. 5.6. This figure shows that the power losses shift from the IGBT to the diode as the power factor decreases. This graph shows that considering the effect of the power factor is very important for properly sizing the semiconductors required for inverters that provide reactive power support. The diodes in a power module have worse thermal characteristics than the IGBT (higher thermal resistance), which can limit the amount of reactive power the module can provide.

For instance, the normal rated power modules used in this research have a thermal resistance of the IGBT junction to case, $R_{thJC} = 3.8^\circ\text{C}/\text{W}$, while thermal resistance for the diode $R_{thJC} = 5.5^\circ\text{C}/\text{W}$. Fig. 5.7 shows that oversizing the semiconductor reduces both the power losses and junction temperature during both normal operation and fault conditions. During normal operation the overrated device improves the efficiency of the inverter and may reduce the cooling requirements of the inverter. The overrated semiconductor also allows injecting the additional active power back to the grid required to maintain the energy balance during voltage dips while allowing the inverter to provide additional reactive power to the grid for grid support.

5.6. Electrothermal Simulations of Proposed PV Inverter

This section presents electrothermal simulations that show that the inverter design with overrated current can increase the grid support capabilities of the inverter, while allowing the dc-link capacitor to operate at its MPP during voltage sags. Electrothermal simulations were performed to study the junction temperature of the IGBT and diode during grid sags, and to guarantee that they stay under the design limits, which is typically 150 °C for silicon devices. It was shown in Chapter 1 that a power module rated at 1.0. p.u, can inject twice its rated current; however, the junction temperature of the device rapidly increases and could exceed the thermal limits of the device. For this reason, it is required to oversize the power module to safely provide fault current. Note that the grid-filter and dc-link can remain at rated power without damage due to the short duration of grid fault events.

Fig. 5.8 shows electrothermal simulation results for the inverter with an overrated power module. The module was overrated to three times the nominal current (30 A) to allow it to ride through deeper grid faults to comply with more stringent grid codes. Additionally, an overrated module can provide additional reactive support during faults. This figure also compares the power losses and junction temperature for a PV inverter providing reactive power support during a 50% voltage dip. As shown that the inverter with a power module with overrated current rating can provide additional power support without exceeding the maximum temperature of the junction. Fig 5.9 shows the results for 3.0 p.u. of reactive power support while maintaining the power balance and the dc-link regulated at the panels MPP. Notice that during only during grid events such as voltage dips the inverter injects additional current back to the grid, which limits the thermal cycles in the power device and the stress on the other inverter components.

5.7. Conclusions

This section proposed hardware modifications for a three-phase grid-tied PV inverter to ride through faults while enhancing its reactive power support during voltage sags. The proposed design oversized the power module current rating to maintain power balance during voltage sags and to increase the reactive power support during grid faults. The

advantages of the proposed method are: 1) enhanced ancillary support during voltage sags; 2) sag-depth independent LVRT and stable dc-link voltage control with MPPT during sags. Additionally, it was shown that devices with higher current capability have better thermal characteristics and lower losses than devices rated at lower currents. This improves the efficiency of the inverter and may reduce the cooling requirements of the inverter during normal operation. Future work includes testing the proposed modifications in a hardware prototype.

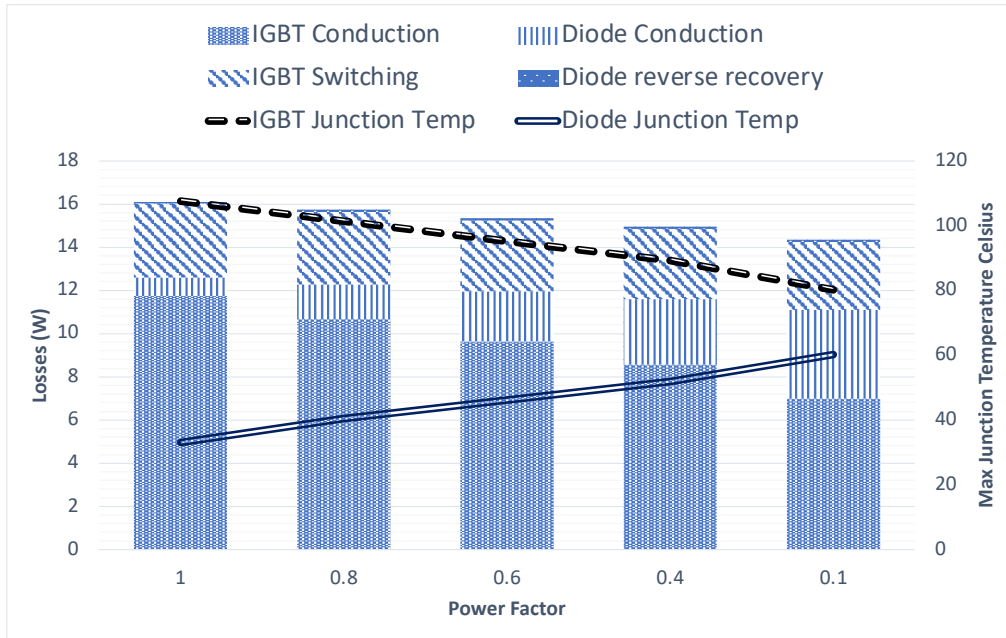


Figure 5.6: Effects of power factor on power losses of diode and IGBT. Maximum temperature of diode and IGBT for different power factors. $V_{DC} = 400V$, modulation index=1, $T_{amb} = 25\text{ }^{\circ}\text{C}$.

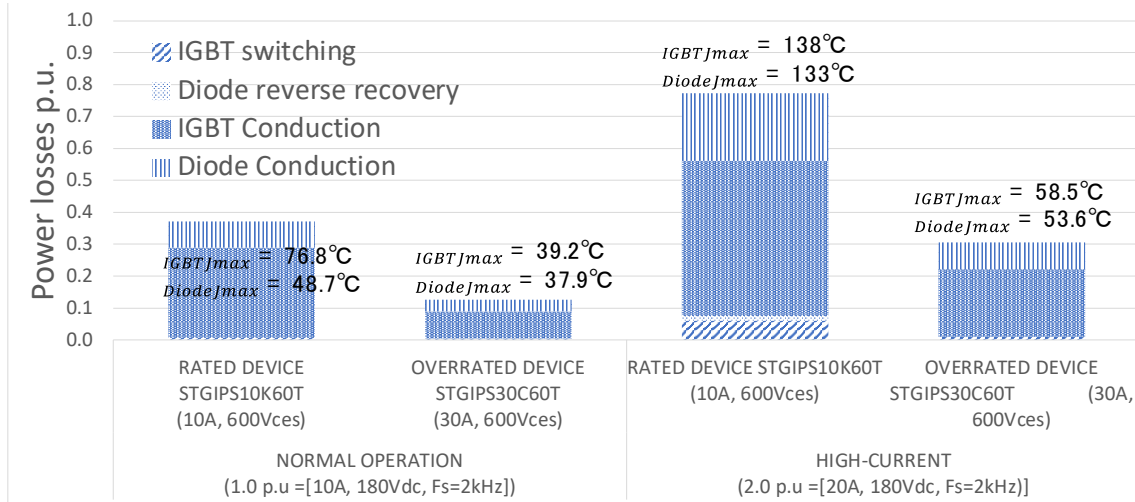


Figure 5.7: Power losses comparison. Rated vs. overrated device [148].

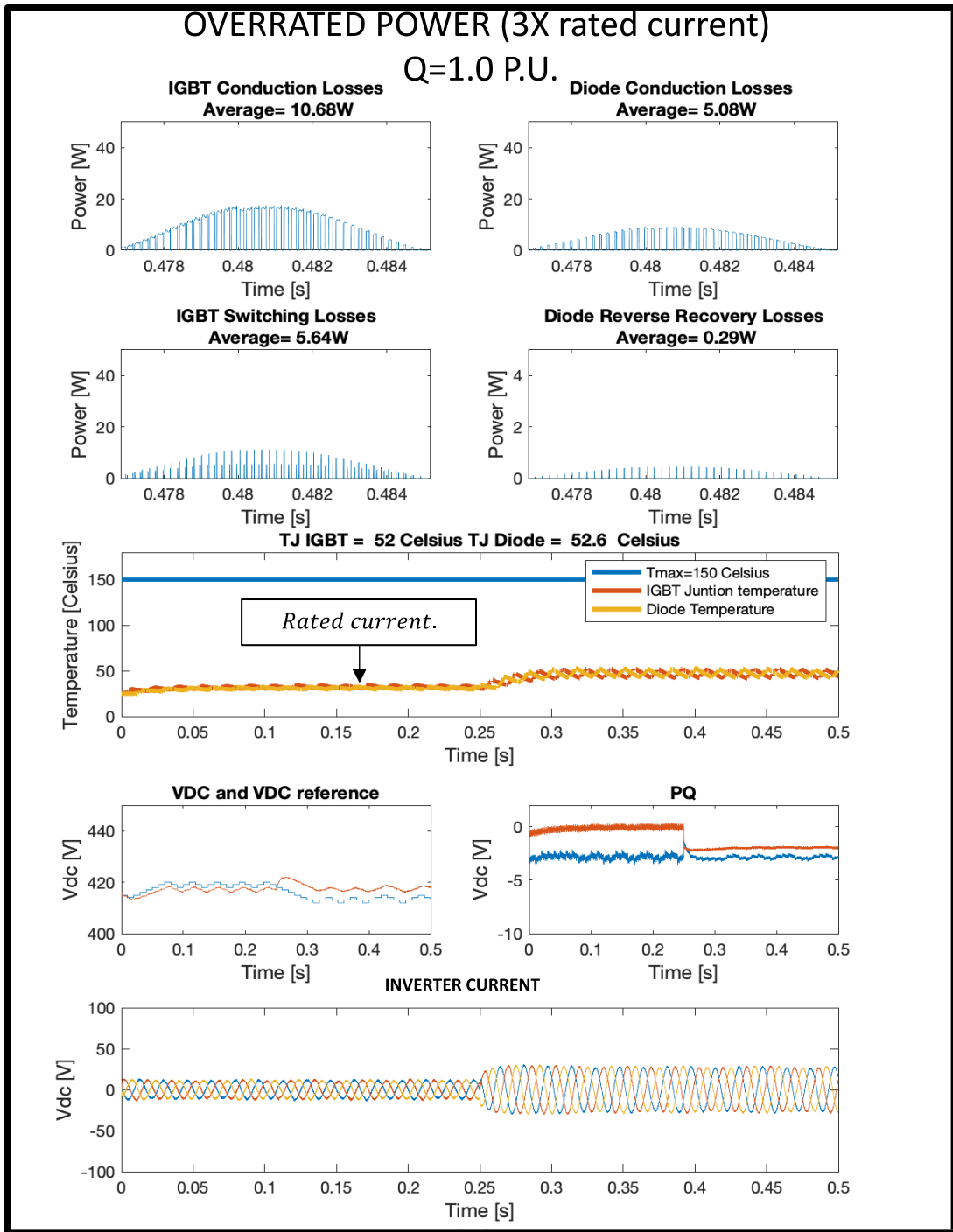


Figure 5.8: Electrothermal simulations of PV inverter under a voltage dip of 50%. Power module with overrated current. Module providing 1.0 p.u. of reactive power.

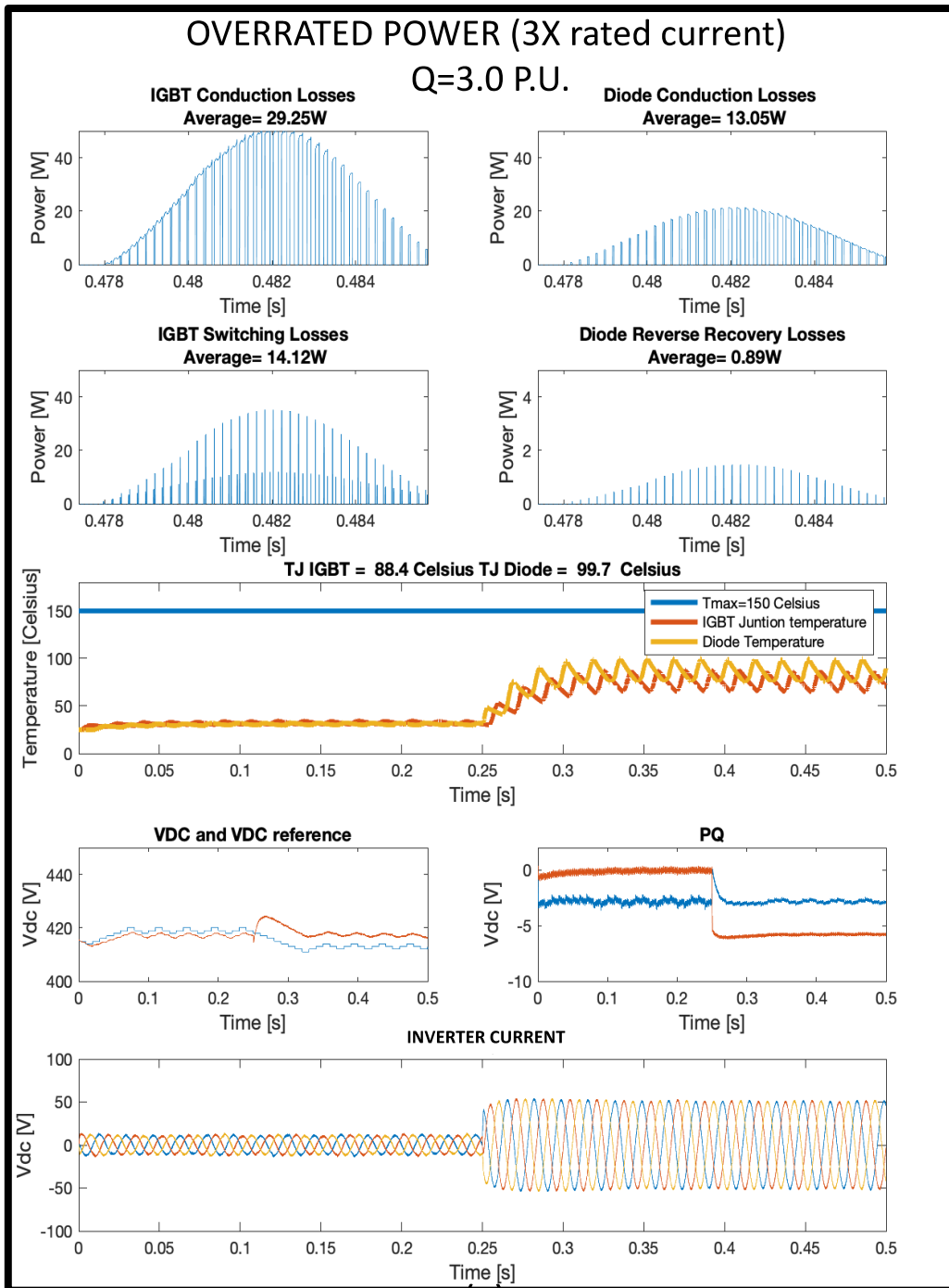


Figure 5.9: Electrothermal simulations of PV inverter under a voltage dip of 50%. Power module with overrated current. Module providing 3.0 p.u. of reactive power during grid sag.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

This dissertation proposes and validates a variety of solutions to protection problems in the modern electrical grid. Specifically, through simulations and hardware validation, this dissertation provides solutions to improve the integration of renewable energy technologies in the grid. The present research also addresses the limitations of existing protection methods in inverter-based microgrids, which is a significant hurdle facing the field.

In response to the challenges posed by islanded systems, Chapter 1 addresses the root problem of the low-short circuit current of IBRs by increasing the short-circuit contribution of a generic voltage source converter. The proposed inverter design shows that replacing the semiconductor and the current transducer is sufficient to increase the short-circuit contribution three-fold. Experimental validation shows that a prototype inverter with an overrated semiconductor can safely provide more than 3.0 p.u. of fault current during ac-faults. Electrothermal simulations showed that the junction temperature of the overrated IGBT and parallel diodes remains under the safety margins established by the manufacturer. Because of the short duration of faults, the dc-link capacitors and grid-filter do not have to be oversized to account for the overload condition. The prototype inverter was integrated with commercially available overcurrent protection to demonstrate full protection coordination for an islanded system. Three-phase, line to line and single-phase faults were applied to validate a wide range of faults present in power systems. Experimental results showed that a minimum of 3.0 p.u. of fault current is required to enable full overcurrent coordination while maintaining a grading margin of 0.25s between relays and 0.3s between fuses and relays. This preliminary research is a promising advance in the field as it shows the utilization of existing, reliable, and affordable overcurrent protection for inverter-based microgrids.

Chapter 1 also addressed the challenges of controlling inverters with deeply saturated inductors, which is necessary when operating the inverter at high-current using a normally rated inductor. In hardware experiments, inductor saturation reduced the phase and gain margin of the current control, which affects the control stability causing overshoots and oscillations when the inverter operates at high current. As a solution, this chapter presents an online method (near real-time) to adapt the proportional and integral gains based on the

available grid-filter inductance was derived and validated in hardware. The proposed approach utilizes a fit function to estimate the remaining inductance based on the operating current, and the Butterworth polynomial to optimize the closed loop eigenvalue locations. This method allows the inverter to provide stable fault current during symmetrical and asymmetrical faults.

Chapter 2 presents an adaptive relaying solution for microgrid protection in islanded and grid-tied mode. This chapter shows the application of adaptive relay in a real microgrid operated by EPB in Chattanooga. The model-adaptive relay is designed to adjust the relay curves based on the available generation and the microgrid topology. This chapter shows that although adaptive relaying provides a solution to the highly variable short circuit current in microgrids, it is not immune to the low short-circuit currents provided by IBRs. For instance, to protect a lateral with the 100 A fuse, it would need at least 200-300 A of short-circuit current, which is not achievable with the commercial IBRs installed in the microgrid. Other limitations of adaptive relaying are that its reliability relies on complex communication network. The model-adaptive relay was validated in Hardware-in-the-Loop (HIL), in a hardware testbed, and was deployed in the Electric Power Board microgrid in Chattanooga, Tennessee.

For-grid tied systems, Chapter 4 and Chapter 5 evaluate two popular renewable energy technologies: Type-3 wind turbines based on Double-Fed Induction Generators (DFIGs) and three-phase PV inverters. Chapter 4 presents the development and the model validation of a real-time emulator of doubly fed induction generator (DFIG) wind turbine system. The code of the real-time DFIG dynamic model with iron losses, back-to-back model, mechanical model, and aerodynamic model were addressed in detail. The model validation was presented under different grid unbalances and for speeds ranging from the sub-synchronous to hyper-synchronous operation. These results showed that the DFIG model provides a good representation of the generator stator and rotor current positive sequence over a wide operating range and grid unbalances. However, the model underestimated the amount of unbalance in the stator currents, an error that increased relative to the grid unbalance. The real-time simulator was then used to study the behavior of the DFIG during

voltage sags, as well to study solutions to enhance their low-voltage ride through capabilities. The DFIG models are available to the public in an open Gitlab repository [133].

Chapter 5 proposes increasing the current capability from a PV inverter to allow it to ride through faults while enhancing their reactive power support during voltage sags. The proposed design consists of oversizing the semiconductor current rating to allow transferring the energy from the dc side to the ac side during voltage sags. This modification maintains the stability of the dc-link voltage during voltage sags of different magnitudes while significantly enhancing the ancillary service capabilities that the inverter can provide. Oversizing the power semiconductors brings the additional benefit of improving the inverter efficiency, significantly reducing the conduction losses during both normal operation and grid fault conditions. Through electrothermal simulations it is shown that the proposed design is capable of injecting three-times the inverter rated current for enough time to comply with the low-voltage ride through requirements (LVRT) requirements established by current grid standards. The advantages of increasing the current from PV inverters are: 1) enhanced ancillary support during voltage sags; 2) sag-depth independent LVRT and stable dc-link voltage control with MPPT during sags. Additionally, it was shown that devices with higher current capability have better thermal characteristics and lower losses than devices rated at lower currents. This improves the efficiency of the inverter and may reduce the cooling requirements of the inverter during normal operation.

6.1. Contributions

This dissertation explored a wide range of issues for power systems with high penetration of renewables, including protection for islanded systems, and ancillary support provided by grid-tied wind and PV systems. The main contributions of this work include the following:

- Experimentally validation of an inverter with increased and sustained short-circuit contribution with the objective of enabling the use of legacy distribution protection in microgrid.

- Analytical derivation of the vector control in the synchronous reference frame considering saturable inductors. The transfer function for the current controller and decoupling terms are derived considering the non-linearities of the inductor.
- Development of a novel inverter control that addresses challenges posed by saturable inductors during high-current operation.
- Simple and cost-effective amplifier design using a high-power monolithic power amplifier that allows the relay in-the-loop connectivity for protection and control applications using a variety of real-time simulator.
- Model validation of the DFIG with iron losses and demonstrates the limitations of the model in accurately representing a physical DFIG machine under grid unbalanced operation. This is accomplished by comparing the emulated stator and rotor currents against physical measurements under 0.5%, 2% and 4% grid voltage unbalance for speed ranging from the sub-synchronous to hyper-synchronous operation.
- Novel method to calculate the stator flux by done through the $\alpha\beta$ rotational transformation, eliminating the need for pure integrators.
- Novel hardware modifications for a three-phase grid-tied PV inverter to enhance its reactive power support during voltage sags.

6.2. Recommendations for Future Studies

Using a prototype inverter, in Chapter 1 it was demonstrated using a prototype inverter the feasibility of increasing the inverter short-circuit contribution. The following future work is recommended to extend this conclusion to higher power inverters.

- Evaluate the feasibility of the proposed modifications with a higher-power inverter operating at 480V.
- Develop detailed analysis to investigate the effects of short-duration, high currents in the inverter's passive components.
- Evaluate enhanced short-circuit contribution when the inverter is operating at high temperatures.

- Evaluate applicability of proposed modifications with MOSFETs and silicon carbide (SiC) devices.
- Evaluate additional power converter topologies, including three-phase inverter with a dc-dc converter between the energy storage and the dc-link.
- Characterize the ferrite and silicon steel cores operating at higher temperatures.

Chapter 4 performed the model validation of DFIG models used in real-time simulators. Future work is required to extend this conclusion to higher-power machines.

- Extend this work with a larger more representative machine.
- Validate the DFIG model during symmetrical and asymmetrical voltage dips.
- Study methods for estimating leakage inductance, magnetizing inductance, and iron losses considering machines with asymmetrical windings.
- Develop DFIG models that can account for imbalances of the phase windings.

Chapter 5 proposed an PV inverter with enhanced ancillary services support. This work demonstrated the feasibility of increasing the reactive support of PV inverters through electrothermal simulations. The following research is recommended to validate the applicability of the method for real applications.

- Conduct hardware demonstration using a representative inverter operating at 480V.
- Demonstrate enhanced LVRT during asymmetrical faults.
- Evaluate the proposed hardware modifications considering a dc-dc converter between the PV array and the dc-link.
- Consider the impacts of the inductor saturation during high-current, grid support operation.

PUBLICATIONS

M. Ferrari and L. M. Tolbert, "Inverter Design with High Short-Circuit Fault Current Contribution to Enable Legacy Overcurrent Protection for Islanded Microgrids," *2022 IEEE Power & Energy Society General Meeting (PESGM)*, 2022, pp. 1-5, doi: 10.1109/PESGM48719.2022.9917188.

M. Ferrari, E. C. Piesciorovsky and L. M. Tolbert, "Real-Time Emulation of Grid-Connected DFIG Wind Energy System with Model Validation from Sub-synchronous to Hyper-synchronous Operation under Unbalanced Conditions," *2022 IEEE Power & Energy Society General Meeting (PESGM)*, 2022, pp. 01-05, doi: 10.1109/PESGM48719.2022.9916807.

M. Ferrari, A. Sundararajan, N. Shepard, J. Smith and B. Ollis, "Microgrid Communications Using the Open-Source Open Field Message Bus (OpenFMB) Framework Applied to a 480V, 100kW Laboratory Microgrid," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-5, doi: 10.1109/PEDG54999.2022.9923215.

M. Ferrari, A. Sundararajan, N. Shepard, J. Smith and B. Ollis, "Microgrid Communications Using the Open-Source Open Field Message Bus (OpenFMB) Framework Applied to a 480V, 100kW Laboratory Microgrid," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-5, doi: 10.1109/PEDG54999.2022.9923215.

M. Ferrari, A. Sundararajan, N. Shepard, J. Smith and B. Ollis, "Microgrid Communications Using the Open-Source Open Field Message Bus (OpenFMB) Framework Applied to a 480V, 100kW Laboratory Microgrid," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-5, doi: 10.1109/PEDG54999.2022.9923215.

M. Ferrari, B. Park and M. M. Olama, "Design and Evaluation of a Model-Free Frequency Control Strategy in Islanded Microgrids with Power-Hardware-in-the-Loop Testing," *2021 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*, 2021, pp. 1-5, doi: 10.1109/ISGT49243.2021.9372219.

M. Ferrari, E. C. Piesciorovsky, T. Smith and J. Hambrick, "Cost-Effective Three-Phase Current Amplifier Interface for Real-time Simulator with Relays in-the-Loop," *2019 North American Power Symposium (NAPS)*, 2019, pp. 1-5, doi: 10.1109/NAPS46351.2019.9000320.

M. Ferrari, M. Orendorff, T. Smith and M. A. Buckner, "OPEN-CODE, REAL-TIME EMULATION TESTBED OF GRID-CONNECTED TYPE-3 WIND TURBINE SYSTEM WITH HARDWARE VALIDATION," *2019 IEEE Applied*

Power Electronics Conference and Exposition (APEC), 2019, pp. 66-70, doi: 10.1109/APEC.2019.8722049.

M. Ferrari, "Evaluation of Harmonic Detection Algorithms for Active Power Filter based on Voltage and Current Detection Methods," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2018, pp. 1-8, doi: 10.1109/PEDG.2018.8447737.

M. Ferrari and M. A. Buckner, "Comparison of Doubly-Fed Induction Generator Machine Models for Real-Time Simulations," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2018, pp. 1-5, doi: 10.1109/PEDG.2018.8447730.

Liu, G., Ollis, T.B., **Ferrari, M.F.** et al. Distributed energy management for networked microgrids in a three-phase unbalanced distribution network. *Front. Energy* (2022). <https://doi.org/10.1007/s11708-022-0851-7>

Liu, G.; **Ferrari, M.F.**; Ollis, T.B.; Tomsovic, K. An MILP-Based Distributed Energy Management for Coordination of Networked Microgrids. *Energies* **2022**, *15*, 6971. <https://doi.org/10.3390/en15196971>

Liu, G.; Ollis, T.B.; **Ferrari, M.F.**; Sundararajan, A.; Tomsovic, K. Robust Scheduling of Networked Microgrids for Economics and Resilience Improvement. *Energies* **2022**, *15*, 2249. <https://doi.org/10.3390/en15062249>

P. E. Neil Shepard, A. Sundararajan, **M. Ferrari** and B. Ollis, "Real-Time Hardware-in-the-Loop Testbed to Evaluate FLISR Implemented with OpenFMB," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-5, doi: 10.1109/PEDG54999.2022.9923270.

A. Sundararajan, M. Olama, **M. Ferrari**, B. Ollis and G. Liu, "A Data Quality-Aware Framework to Reliably Forecast Photovoltaic Generation and Consumer Load for an Improved Resilience of Microgrids," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-6, doi: 10.1109/PEDG54999.2022.9923109.

Piesciorovsky, EC, **Ferrari Maglia, MF**. Comparison of high-speed adaptive and nonadaptive backup overcurrent protection on fuse feeders with sensors. *Int Trans Electr Energ Syst*. 2019; 29:e2812. <https://doi.org/10.1002/etep.2812>

REFERENCES

CHAPTER 1

- [1] A. Hooshyar and R. Iravani, "Microgrid Protection," *Proceedings of the IEEE*, vol. 105, no. 7, pp. 1332-1353, Jul. 2017, doi: [10.1109/JPROC.2017.2669342](https://doi.org/10.1109/JPROC.2017.2669342).
- [2] M. W. Altaf, M. T. Arif, S. N. Islam, and M. E. Haque, "Microgrid Protection Challenges and Mitigation Approaches—A Comprehensive Review," *IEEE Access*, vol. 10, pp. 38895-38922, 2022, doi: [10.1109/ACCESS.2022.3165011](https://doi.org/10.1109/ACCESS.2022.3165011).
- [3] "Microgrid Deployment Tracker Q22-Projects and Trends in the Global Microgrid Market by Region, Segment, Business Model, and Top States and Countries," *Guidehouse Insights*, Apr. 2022.
- [4] A. Dagar, P. Gupta, and V. Niranjana, "Microgrid protection: A comprehensive review," *Renewable and Sustainable Energy Reviews*, vol. 149, pp. 1364–0321, 2021, doi: [10.1016/j.rser.2021.111401](https://doi.org/10.1016/j.rser.2021.111401).
- [5] Z. Chen, X. Pei, M. Yang, L. Peng, and P. Shi, "A novel protection scheme for inverter-interfaced microgrid (IIM) operated in islanded mode," *IEEE Trans. Power Electron*, vol. 33, no. 9, pp. 7684-7697, Sep. 2018.
- [6] E. Sortomme, S. S. Venkata, and J. Mitra, "Microgrid protection using communication-assisted digital relays," *IEEE Trans. Power Del*, vol. 25, no. 4, pp. 2789-2796, Oct. 2010.
- [7] H. J. Laaksonen, "Protection principles for future microgrids," *IEEE Trans. Power Electron*, vol. 25, no. 12, pp. 2910-2918, Dec. 2010.
- [8] M. Ferrari and L. M. Tolbert, "Inverter Design with High Short-Circuit Fault Current Contribution to Enable Legacy Overcurrent Protection for Islanded Microgrids," in *2022 IEEE Power & Energy Society General Meeting (PESGM)*, 2022, pp. 1-5,. doi: [10.1109/PESGM48719.2022.9917188](https://doi.org/10.1109/PESGM48719.2022.9917188).
- [9] L. Che, M. Khodayar, and M. Shahidehpour, "Adaptive protection system for microgrids: Protection practices of a functional microgrid system," *IEEE Electrific. Mag*, vol. 2, no. 1, pp. 66-80, Mar. 2014.
- [10] G. Kaur and K. U. R. Anupama Prakash, "A critical review of Microgrid adaptive protection techniques with distributed generation, Renewable Energy Focus," vol. 39. pp. 99-109, 2021. doi: [10.1016/j.ref.2021.07.005](https://doi.org/10.1016/j.ref.2021.07.005).
- [11] T. S. Ustun, C. Ozansoy, and A. Zayegh, "Modeling of a centralized microgrid protection system and distributed energy resources according to IEC 61850-7-420," *IEEE Trans. Power Syst*, vol. 27, no. 3, pp. 1560-, Aug. 1567.
- [12] "IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, vol. 1, pp. 1-138, Apr. 2018, doi: [10.1109/IEEESTD.2018.8332112](https://doi.org/10.1109/IEEESTD.2018.8332112).

- [13] E. Casagrande, "A differential sequence component protection scheme for microgrids with inverter-based distributed generators," *IEEE Trans. Smart Grid*, vol. 5, no. 1, pp. 29-37, Jan. 2014.
- [14] M. Dewadasa, A. Ghosh, G. Ledwith, and M. Wishart, "Fault isolation in distributed generation connected distribution networks," *IET J. Gener. Transm. Distrib.*, vol. 5, no. 10, pp. 1053-1061, Apr. 2011
- [15] H. Al-Nasseri, M. Redfern, and F. Li, "A voltage based protection for micro-grids containing power electronic converters," in *Proc. IEEE Power Eng. Soc. Gen. Meeting*, Jun. 2006, pp. 1–7.
- [16] S. A. Saleh, "Signature-coordinated digital multirelay protection for microgrid systems," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4614-4623, Sep. 2014
- [17] Q. Yang and J. Li, "Simon Le Blond, Cheng Wang, Artificial Neural Network Based Fault Detection and Fault Location in the DC Microgrid," *Energy Procedia*, vol. 103, pp. 129-134, 2016, doi: [10.1016/j.egypro.2016.11.261](https://doi.org/10.1016/j.egypro.2016.11.261).
- [18] H. Muda and P. Jena, "Superimposed Adaptive Sequence Current Based Microgrid Protection: A New Technique," *IEEE Transactions on Power Delivery*, vol. 32, no. 2, pp. 757-767, Apr. 2017, doi: [10.1109/TPWRD.2016.2601921](https://doi.org/10.1109/TPWRD.2016.2601921).
- [19] Z. Chen, X. Pei, M. Yang, L. Peng, and P. Shi, "A novel protection scheme for inverter-interfaced microgrid (IIM) operated in islanded mode," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7684-7697, Sep. 2018.
- [20] M. Uzair, L. Li, J. G. Zhu, and M. Eskandari, "A protection scheme for AC microgrids based on multi-agent system combined with machine learning," in *29th Australasian Universities Power Engineering Conference (AUPEC)*, 2019, pp. 1-6, doi: [10.1109/AUPEC48547.2019.211845](https://doi.org/10.1109/AUPEC48547.2019.211845).
- [21] S. Kar and S. R. Samantaray, "A fuzzy rule base approach for intelligent protection of microgrids," *Electr. Power Compon. Syst.*, vol. 43, no. 18, pp. 2082-2093, 2015.
- [22] Q. Liu, T. Liang, and V. Dinavahi, "Deep learning for hardware-based real-time fault detection and localization of all electric ship MVDC power system," *IEEE Open J. Ind. Appl.*, vol. 1, pp. 194-204, 2020, doi: [10.1109/OJIA.2020.3034608](https://doi.org/10.1109/OJIA.2020.3034608).
- [23] N. Fischer, V. Skendzic, R. Moxley, and J. Needs, "Protective relay traveling wave fault location," in *Proc. 11th IET Int. Conf. Develop. Power Syst. Protect*, 2012, pp. 1–3.
- [24] A. D. 'ko X. Li and G. Burt, "Traveling wave-based protection scheme for inverter-dominated microgrid using mathematical morphology," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2211-2218, Sep. 2014.
- [25] N. Jayawarna, C. Jones, M. Barnes and N. Jenkins, "Operating MicroGrid Energy Storage Control during Network Faults," *2007 IEEE International Conference on System of Systems Engineering*, San Antonio, TX, USA, 2007, pp. 1-7, doi: [10.1109/SYSESE.2007.4304254](https://doi.org/10.1109/SYSESE.2007.4304254).

- [26] F F. van Overbeeke, "Fault current source to ensure the fault level in inverter dominated networks," *CIREN 2009 - The 20th International Conference and Exhibition on Electricity Distribution - Part 2*, Prague, 2009, pp. 1-13.
- [27] K. O. Oureilidis and C. S. Demoulias, "A fault clearing method in converter-dominated microgrids with conventional protection means," *IEEE Trans. Power Electron*, vol. 31, no. 6, pp. 4628-4640, Jun. 2016.
- [28] E. C. Piesciorovsky, T. Smith, and T. B. Ollis, "Protection schemes used in North American microgrids," *Int Trans Electr Energ Syst*, p. 30 12461, 2020, doi: [10.1002/2050-7038.12461](https://doi.org/10.1002/2050-7038.12461)
- [29] R. Mohanty, P. Chen, L. A. Tuan, and A. Narula, "Challenges in Protection of Converter Dominated Medium-Voltage Microgrids," in *2019 IEEE PES Innovative Smart Grid Technologies Europe (ISGT-Europe*, 2019, pp. 1-5,. doi: [10.1109/ISGTEurope.2019.8905739](https://doi.org/10.1109/ISGTEurope.2019.8905739).
- [30] H. H. Zeineldin, H. M. Sharaf, D. K. Ibrahim, and E. E. A. El-Zahab, "Optimal Protection Coordination for Meshed Distribution Systems With DG Using Dual Setting Directional Over-Current Relays," *IEEE Transactions on Smart Grid*, vol. 1, no. 1, pp. 115-123, Jan. 2015, doi: [10.1109/TSG.2014.2357813](https://doi.org/10.1109/TSG.2014.2357813).
- [31] M., "Khederzadeh "Adaptive setting of protective relays in micro-grids in grid-connected and autonomous operation," in *Proc. IET International Conf. on Developments in Power System Protection*, 2012, pp. 1–4.
- [32] M. A. Zamani, A. Yazdani, and T. S. Sindhu, "A communication-assisted protection strategy for inverter based medium voltage micro-grids," *IEEE Trans. Smart Grid*, vol. 3, pp. 2088-2099, Dec. 2012.
- [33] C. Liu, Z. Chen, and Z. Liu, "A communication-less overcurrent protection for distribution system with distributed generation integrated," in *3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG*, 2012, pp. 140-147,. doi: [10.1109/PEDG.2012.6253992](https://doi.org/10.1109/PEDG.2012.6253992).
- [34] . G. K. Bechtold and E. B. Rudnyi, *Fast Simulation of Electro- Thermal MEMS: Efficient Dynamic Compact Models*. New York: Springer, 2007.
- [35] L. R. GopiReddy, L. M. Tolbert, B. Ozpineci, and J. O. P. Pinto, "Rainflow Algorithm-Based Lifetime Estimation of Power Semiconductors in Utility Applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3368-3375, Jul. 2015, doi: [10.1109/TIA.2015.2407055](https://doi.org/10.1109/TIA.2015.2407055).
- [36] "Infineon Online Power Simulation Platform, available at." [Online]. Available: <https://www.infineon.com/cms/en/tools/landing/iposim-infineon-online-power-simulation-platform/>
- [37] S.T., [Online]. Available: <https://www.st.com/en/embedded-software/stsw-powerstudio.html>

- [38] “Linearized Modeling and Controller Design of the Nonlinear Inductors in $\alpha\beta$ -frame,” in *20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe*, 2018, pp. 1–9
- [39] E. Casagrande, “A differential sequence component protection scheme for microgrids with inverter-based distributed generators,” *IEEE Trans. Smart Grid*, vol. 5, no. 1, pp. 29-37, Jan. 2014.
- [40] G. Dong, “Sensorless and Efficiency Optimized Induction Machine Control with Associated Converter PWM Modulation Schemes,” Ph.D. dissertation, Tennessee Technological University, 2005.
- [41] Ruscio and David, “On Tuning PI Controllers for Integrating Plus Time Delay Systems”,” *Modeling, Identification and Control*, vol. 31. 4, pp. 145–164, 2010.
- [42] Özkan and A. M. Hava, “Current Control of Single-Phase VSC Systems With Inductor Saturation Using Inverse Dynamic Model-Based Compensation,” *IEEE Transactions on Industrial Electronics*, vol. 66, no. 12, pp. 9268-9277, Dec. 2019, doi: [10.1109/TIE.2019.2892682](https://doi.org/10.1109/TIE.2019.2892682).
- [43] “Grid Modernization, Protection. National Renewable Energy Laboratory.” [Online]. Available: <https://www.nrel.gov/grid/protection.html>
- [44] M. Bakkar, S. Bogarra, F. Córcoles, A. Aboelhassan, S. Wang, and J. Iglesias, “Artificial Intelligence-Based Protection for Smart Grids,” *Energies*, vol. 15, p. 4933, 2022, doi: [10.3390/en15134933](https://doi.org/10.3390/en15134933).
- [45] “Commercial Power System Protection - Schneider Electric.” [Online]. Available: [https://www.se.com/ww/en/tools/npag-online-re14y/pdf/B3-Industrial and Commercial Power System Protection.pdf](https://www.se.com/ww/en/tools/npag-online-re14y/pdf/B3-Industrial%20and%20Commercial%20Power%20System%20Protection.pdf)
- [46] Z. Özkan and A. M. Hava, “Inductor Saturation Compensation in Three-Phase Three-Wire Voltage-Source Converters Via Inverse System Dynamics,” *IEEE Transactions on Industrial Electronics*, vol. 69, no. 5, pp. 4309-4319, May 2022, doi: [10.1109/TIE.2021.3084155](https://doi.org/10.1109/TIE.2021.3084155).
- [47] S. Gonzalez, N. Gurule, M. J. Reno, and J. Johnson, “Fault Current Experimental Results of Photovoltaic Inverters Operating with Grid- Support Functionality,” in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC & 34th EU PVSEC)*, Waikoloa Village, HI, 2018, pp. 1406–1411.

CHAPTER 2

- [48] N. S. Gurule, J. Hernandez-Alvidrez, M. J. Reno, A. Summers, S. Gonzalez, and J. Flicker, “Grid-forming Inverter Experimental Testing of Fault Current Contributions,” in *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 2019, pp. 3150-3155,. doi: [10.1109/PVSC40753.2019.8980892](https://doi.org/10.1109/PVSC40753.2019.8980892).

- [49] N. S. Gurule, J. Hernandez-Alvidrez, R. Darbali-Zamora, M. J. Reno, and J. D. Flicker, "Experimental Evaluation of Grid-Forming Inverters Under Unbalanced and Fault Conditions," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial*.
- [50] T. Harzig, H. A. Al Hassan and B. M. Grainger, "Symmetrical Component Model for a Transformerless, Grid-Tied Current Controlled Inverter under Unbalanced Conditions," *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, Canada, 2019, pp. 1-6, doi: 10.1109/COMPEL.2019.8769663.
- [51] X. Du and R. Wang, "Control strategy of negative sequence current for the grid-connection converter under the unbalanced grid condition," *2015 34th Chinese Control Conference (CCC)*, Hangzhou, China, 2015, pp. 9066-9071, doi: 10.1109/ChiCC.2015.7261074.
- [52] J. Shiles, "Microgrid protection: An overview of protection strategies in North American microgrid projects," *IEEE Power & Energy Society General Meeting*, pp. 1-5, 2017, doi: [10.1109/PESGM.2017.8274519](https://doi.org/10.1109/PESGM.2017.8274519).
- [53] M. G. Villalva, J. R. Gazoli, and E. R. Filho, "Modeling and circuit-based simulation of photovoltaic arrays," in *2009 Brazilian Power Electronics Conference*, 2009, pp. 1244-1254,. doi: [10.1109/COBEP.2009.5347680](https://doi.org/10.1109/COBEP.2009.5347680).
- [54] M. Ferrari, B. Park, and M. M. Olama, "Design and Evaluation of a Model-Free Frequency Control Strategy in Islanded Microgrids with Power-Hardware-in-the-Loop Testing," in *2021 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*, 2021, pp. 1-5,. doi: [10.1109/ISGT49243.2021.9372219](https://doi.org/10.1109/ISGT49243.2021.9372219).
- [55] M. Ferrari, E. C. Piescorovsky, T. Smith, and J. Hambrick, "Cost-Effective Three-Phase Current Amplifier Interface for Real-time Simulator with Relays in-the-Loop," in *2019 North American Power Symposium (NAPS)*, Wichita, KS, USA, 2019, pp. 1-5,. doi: [10.1109/NAPS46351.2019.9000320](https://doi.org/10.1109/NAPS46351.2019.9000320).
- [56] D. Beeman, "Short-Circuit-Current Calculating Procedures"," in *Beeman, Donald (ed.). Industrial Power Systems Handbook. McGraw-Hill. pp. see esp, vol. 38–41, 1955, pp. 52–55.*
- [57] W. D. Jr. and Stevenson, *Elements of power system analysis*, 3rd ed. New York: McGraw-Hill, 1975.

CHAPTER 3

- [58] D. K. Xue, R. Guan, J. Li, A. Taylor, and X. Zhang, "RTDS-based HIL testing platform for complex modern electricity transmission systems," *The Journal of Engineering*, vol. 2018, no. 15, pp. 1315-1320, 2018.

- [59] M. S. Almas, R. Leelarui, and L. Vanfretti, "Over-current relay model implementation for real-time simulation & Hardware-in-the-Loop (HIL) validation," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, QC, 2012, pp. 4789–4796.
- [60] B. S. Rigby, "Closed-loop testing of an overcurrent relay using a real-time digital simulator," in *2004 IEEE Africon. 7th Africon Conference in Africa (IEEE Cat. No.04CH37590)*, Gaborone, 2004, vol. 2, pp. 783–788.
- [61] R. Liu, R. Sun, and M. Tania, "Hardware-in-the-loop relay testing in dominion's black start plan," in *2017 IEEE Power & Energy Society General Meeting*, Chicago, IL, 2017, pp. 1–5.
- [62] Liu and H. K. Hoidalén, "An adaptive inverse time overcurrent relay model implementation for real-time simulation and hardware-in-the-loop testing," in *13th International Conference on Development in Power System Protection 2016 (DPSP)*, Edinburgh, 2016, pp. 1–6.
- [63] E. C. Piesciorovsky and N. N. Schulz, "Comparison of Non-real-time and Real-time Simulators with Relays in-the-loop for Adaptive Overcurrent Protection," *Electric Power Systems Research*, vol. 143, pp. 657–668, 2017, doi: [10.1016/j.epsr.2016.10.049](https://doi.org/10.1016/j.epsr.2016.10.049).
- [64] E. C. Piesciorovsky and N. N. Schulz, "Fuse Relay Adaptive Overcurrent Protection Scheme for Microgrid with Distributed Generators," *IET Gen, Trans and Distrib*, vol. 11, no. 2, pp. 540–549, 2017.
- [65] E. C. Piesciorovsky and N. N. Schulz, "Comparison of Programmable Logic and Setting Group Methods for adaptive overcurrent protection in microgrids," *Electric Power Systems Research*, vol. 151, pp. 273–282, 2017, doi: [10.1016/j.epsr.2017.05.035](https://doi.org/10.1016/j.epsr.2017.05.035).
- [66] "OPA541 datasheet." [Online]. Available: <http://www.ti.com/lit/ds/symlink/opa541.pdf>
- [67] M. Ferrari, "GSC control strategy for harmonic voltage elimination of grid-connected DFIG wind turbine," in *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, Milwaukee, WI, 2014, pp. 185–191.
- [68] F. Mistlberger and R. Koch, "Class-AB high-swing CMOS power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 7, pp. 1089–1092, Jul. 1992.
- [69] K. S. Ling, A. M. Gole, P. G. McLaren, and R. A. Wachal, "A PWM current amplifier for testing protective relay," in *Proc. IEEE CCECE*, Winnipeg, MB, Canada, 2002, pp. 218–223.
- [70] R. Marcal, R. Rodrigues, C. Fortunato, L. S. Martins, and V. F. Pires, "A Power Amplifier System for Testing of Distance Relay Operating Characteristic," in *12th International Power Electronics and Motion Control Conference*, Portoroz, 2006, pp. 1757–1761.

- [71] G. R. Walker, "A Class B switch-mode assisted linear amplifier," in *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1278-1285, Nov. 2003, doi: 10.1109/TPEL.2003.818825.
- [72] G. Gong, H. Ertl, and J. W. Kolar, "Novel Tracking Power Supply for Linear Power Amplifiers," *IEEE Transactions on Industrial electronics*, vol. 55, no. 2, Feb. 2008.
- [73] Z. Stanislav, "High efficiency, linear current amplifier for testing protective relays," in *2014 IEEE International Energy Conference (ENERGYCON)*, Cavtat, 2014, pp. 544–549. doi: [10.1109/ENERGYCON.2014.6850479](https://doi.org/10.1109/ENERGYCON.2014.6850479).
- [74] J., *Lewis Blackburn Symmetrical Components for Power Systems Engineering*. New York: Marcel Dekker, 1993.
- [75] Pqmon.epri.com. (2019). *DOE/EPRI Disturbance Library*. [online] Available at: <https://pqmon.epri.com/> [Accessed 30 Jun. 2019].

CHAPTER 4

- [76] G. Abad, J. López, M. A. Rodríguez, L. Marroyo, and G. Iwanski, "Doubly Fed Induction Machine: Modeling and Control for Wind Energy Generation Applications. Book, Chapters 1-15." Wiley-IEEE Press, 2011. [Online]. Available: <https://ieeexplore.ieee.org/book/6047757>.
- [77] "Global Wind Report 2021 | Global Wind Energy Council", *Global Wind Energy Council*, 2021, [Online]. Available: <https://gwec.net/global-wind-report-2021/>.
- [78] G. F. Gontijo, "Modeling, Control, and Experimental Verification of a DFIG With a Series-Grid-Side Converter With Voltage Sag, Unbalance, and Distortion Compensation Capabilities," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 584-600, Jan. 2020, doi: [10.1109/TIA.2019.2946950](https://doi.org/10.1109/TIA.2019.2946950).
- [79] Federal Energy Regulatory Commission (FERC), United States of America. Docket no. RM05-4-000 Order no. 661. Interconnection for Wind Energy, pp. 1-85, Jun. 2, 2005, [online]. Available: <https://www.ferc.gov/industries-data/electric/electric-transmission/generator-interconnection/standard-interconnection-0>.
- [80] R. H. Yang and J. X. Jin, "Unified Power Quality Conditioner With Advanced Dual Control for Performance Improvement of DFIG-Based Wind Farm," *IEEE Transactions on Sustainable Energy*, vol. 12, no. 1, pp. 116-126, Jan. 2021, doi: [10.1109/TSTE.2020.2985161](https://doi.org/10.1109/TSTE.2020.2985161).
- [81] D. Wenzhong, E. Muljadi, and W. Wang, "Comparison of Standards and Technical Requirements of Grid Connected Wind Power Plants in China and the United States. National Renewable Energy Laboratory of the U.S," *Department of Energy, Report*, p. 5 00-64225, Sep. 2016, doi: [10.2172/1326717](https://doi.org/10.2172/1326717).
- [82] O. A. Morfin, R. Ruiz-Cruz, and L. AG, "Torque controller of a doubly-fed induction generator impelled by a DC motor for wind system applications," *IET Renew. Power Gener*, vol. 8, no. 5, pp. 484–497, 2014, doi: [10.1049/iet-rpg.2012.0291](https://doi.org/10.1049/iet-rpg.2012.0291).

- [83] P. Pena, J. C. Clare, and G. M. Asher, "Doubly fed induction generator using back-to-back PWM converters and its application to variable-speed wind energy generation," *IEE Proc., Electr. Power Appl.*, vol. 143, no. 3, pp. 231–241, 1996, doi: [10.1049/ip-epa:19960288](https://doi.org/10.1049/ip-epa:19960288).
- [84] H. Dehnavifard, M. A. Khan, and P. S. Barendse, "Development of a 5-kW Scaled Prototype of a 2.5 MW Doubly-Fed Induction Generator," *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 4688–4698, Nov. 2016, doi: [10.1109/TIA.2016.2591512](https://doi.org/10.1109/TIA.2016.2591512).
- [85] M. E. Iranian, M. Mohseni, S. Aghili, A. Parizad, H. R. Baghaee, and J. M. Guerrero, "Real-Time FPGA-based HIL Emulator of Power Electronics Controllers using NI PXI for DFIG Studies," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: [10.1109/JESTPE.2020.3023100](https://doi.org/10.1109/JESTPE.2020.3023100).
- [86] L. Ibarra, A. Rosales, P. Ponce, A. Molina, and R. Ayyanar, "Overview of Real-Time Simulation as a Supporting Effort to Smart-Grid Attainment", *Energies*, vol. 10, no. 6, p. 817, 2017.
- [87] H. Shao, "Design and application of RTDS & GH Bladed co-simulation research platform for DFIG wind turbine," in *8th Renewable Power Generation Conference (RPG 2019)*, 2019, pp. 1–8, doi: [10.1049/cp.2019.0366](https://doi.org/10.1049/cp.2019.0366).
- [88] A. Benigni, F. Adler, D. Fetzer, A. Monti, and R. DeDoncker, "Real-time simulation of a doubly fed induction generator wind turbine on a new DSP based hardware platform," in *15th European Conference on Power Electronics and Applications*, Lille, France, 2013. doi: [10.1109/EPE.2013.6634687](https://doi.org/10.1109/EPE.2013.6634687).
- [89] F. Huerta, R. L. Tello, and M. Prodanovic, "Real-Time Power-Hardware-in-the-Loop Implementation of Variable-Speed Wind Turbines," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1893–1904, 2017, doi: [10.1109/TIE.2016.2624259](https://doi.org/10.1109/TIE.2016.2624259).
- [90] L. Pak and V. Dinavahi, "Real-Time Simulation of a Wind Energy System Based on the Doubly-Fed Induction Generator," *IEEE Transactions on Power Systems*, vol. 24, no. 3, pp. 1301–1309, Aug. 2009, doi: [10.1109/TPWRS.2009.2021200](https://doi.org/10.1109/TPWRS.2009.2021200).
- [91] Craciun, B.-I.; Kerekes, T.; Sera, D.; Teodorescu, R.; Brandl, R.; Degner, T.; Geibel, D.; Hernandez, H. Grid integration of PV power based on PHIL testing using different interface algorithms. In *Proceedings of the IECON 2013—39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria, 10–13 November 2013; pp. 5380–5385
- [92] A. S. Makinen, T. Messo, and H. Tuusa, "Power hardware in-the-loop laboratory test environment for small scale wind turbine prototype," in *Proc. Eur. Conf. Power Electron*, 2014, pp. 1–10.
- [93] J. Shair, X. Xie, Y. Li, and V. Terzija, "Hardware-in-the-Loop and Field Validation of a Rotor-Side Subsynchronous Damping Controller for a Series Compensated DFIG

- System,” *IEEE Transactions on Power Delivery*, vol. 36, no. 2, pp. 698-709, Apr. 2021, doi: [10.1109/TPWRD.2020.2989475](https://doi.org/10.1109/TPWRD.2020.2989475).
- [94] V. A. Papaspiliotopoulos, G. N. Korres, V. A. Kleftakis, and N. D. Hatziaargyriou, “Hardware-In-the-Loop Design and Optimal Setting of Adaptive Protection Schemes for Distribution Systems With Distributed Generation,” *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 393-400, Feb. 2017, doi: [10.1109/TPWRD.2015.2509784](https://doi.org/10.1109/TPWRD.2015.2509784).
- [95] L. Trilla, O. Gomis-Bellmunt, A. Junyent-Ferre, M. Mata, J. S. Navarro, and A. Sudria-Andreu, “Modeling and Validation of DFIG 3-MW Wind Turbine Using Field Test Data of Balanced and Unbalanced Voltage Sags,” *IEEE Transactions on Sustainable Energy*, vol. 2, no. 4, pp. 509-519, Oct. 2011, doi: [10.1109/TSTE.2011.2155685](https://doi.org/10.1109/TSTE.2011.2155685).
- [96] S. Auddy, R. K. Varma, and M. Dang, “Field Validation of a Doubly Fed Induction Generator (DFIG) Model,” in *Proc. IEEE Electrical Power Conference*, Oct. 2007, pp. 484-489.
- [97] A. Petersson, T. Thiringer, L. Harnfors, and T. Petru, “Modeling and experimental verification of grid interaction of a DFIG wind turbine,” *IEEE Transactions on Energy Conversion*, vol. 20, no. 4, pp. 878-886, Dec. 2005, doi: [10.1109/TEC.2005.853750](https://doi.org/10.1109/TEC.2005.853750).
- [98] A. Veltman, D. W. J. Pulle, and R. W. Doncker, “Fundamentals of Electric Drives.” Power Systems, Book, Springer, pp. 1-357, 2007. [Online]. Available: <https://link.springer.com/book/10.1007/978-1-4020-5504-1>.
- [99] G. F. Gontijo, “Modeling, Control, and Experimental Verification of a DFIG With a Series-Grid-Side Converter With Voltage Sag, Unbalance, and Distortion Compensation Capabilities,” *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 584-600, Jan. 2020, doi: [10.1109/TIA.2019.2946950](https://doi.org/10.1109/TIA.2019.2946950).
- [100] N. Karakasis, E. Tsioumas, N. Jabbour, A. M. Bazzi, and C. Mademlis, “Optimal Efficiency Control in a Wind System With Doubly Fed Induction Generator,” *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 356-368, Jan. 2019, doi: [10.1109/TPEL.2018.2823481](https://doi.org/10.1109/TPEL.2018.2823481).
- [101] M. Ferrari and M. A. Buckner, “Comparison of Doubly-Fed Induction Generator Machine Models for Real-Time Simulations,” in *9th IEEE International Symposium on Power Electronics for Distributed Generation Systems*, Charlotte, NC, 2018, pp. 1–5. doi: [10.1109/PEDG.2018.8447730](https://doi.org/10.1109/PEDG.2018.8447730).
- [102] P. B. Modeling, “Control and Analysis of A Doubly Fed Induction Generator Based Wind Turbine System With Voltage Regulation.” Master thesis. Tennessee Technological University, 2011. [Online]. Available: <https://www.tntech.edu/engineering/pdf/cesr/ojo/Bijaya.pdf>
- [103] D. Zhou, Y. Song, and F. Blaabjerg, “Modern control strategies of doubly-fed induction generator based wind turbine system,” *Chinese Journal of Electrical Engineering*, vol. 2, no. 1, pp. 13–23, 2016.

- [104] G. Yuan, C. J. and Y. Li, "Vector Control and Synchronization of Doubly Fed Induction Wind Generator System," in *4th International PEMC Conference Proceedings*, Xi'an, China, Aug. 2004, pp. 1–5. [Online]. Available: <https://ieeexplore.ieee.org/document/1375838>
- [105] A. Thakallapelli, S. Kamalasadan, K. M. Muttaqi, and M. T. Hagh, "A Synchronization Control Technique For Soft Connection of Doubly Fed Induction Generator Based Wind Turbines to the Power Grids," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5277-5288, Sep. 2019, doi: [10.1109/TIA.2019.2917654](https://doi.org/10.1109/TIA.2019.2917654).
- [106] K. Günther, P. Tourou, and C. Sourkounis, "Alternative start-up and control of a DFIG-DCM laboratory test bench for wind energy applications," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 2389-2395,. doi: [10.1109/IECON.2017.8216402](https://doi.org/10.1109/IECON.2017.8216402).
- [107] M. Ferrari, "GSC control strategy for harmonic voltage elimination of grid-connected DFIG wind turbine," in *International Conference on Renewable Energy Research and Application (ICRERA)*, Milwaukee, WI, USA, 2014, pp. 185-191,. doi: [10.1109/ICRERA.2014.7016554](https://doi.org/10.1109/ICRERA.2014.7016554).
- [108] P. Pillay and M. Manyage, "Definitions of Voltage Unbalance," *IEEE Power Eng. Rev. Mag*, vol. 21, no. ue 5, pp. 50-51, May 2001.
- [109] M. Ferrari, B. Park, and M. M. Olama, "Design and Evaluation of a Model-Free Frequency Control Strategy in Islanded Microgrids with Power-Hardware-in-the-Loop Testing," in *2021 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*, 2021, pp. 1-5,. doi: [10.1109/ISGT49243.2021.9372219](https://doi.org/10.1109/ISGT49243.2021.9372219).
- [110] M. F. Maglia, M. M. Olama, and B. Ollis, "Hardware-in-the-loop Testing of Signal Temporal Logic Frequency Control in a Microgrid," in *2020 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*, 2020, pp. 1-5,. doi: [10.1109/ISGT45199.2020.9087664](https://doi.org/10.1109/ISGT45199.2020.9087664).
- [111] A. Thomas, *Wind Power in Power Systems*. New York: Wiley, 2005.
- [112] F. Iov, A. D. Hansen, P. Sørensen, and N. A. Cutululis, "Mapping of grid faults and grid codes," *Risø Nat. Lab., Tech. Univ. Denmark*, Roskilde, Denmark, Jul. 2007.
- [113] D. Gao, "Comparison of Standards and Technical Requirements of Grid-Connected Wind Power Plants in China and the United States", NREL September, Technical Report., 2016.
- [114] "Interconnection for wind energy," United States of America Federal Energy Regulatory Commission, Dec. 2005, Docket No. RM05-4-001, Order No. 661-A. [Online]. Available: www.ferc.gov/EventCalendar/Files/20051212171744-RM05-4-001.pdf (Accessed on: 2014-11-01)
- [115] G. Abad, J. López, M. A. Rodríguez, L. Marroyo, and G. Iwanski, "Doubly Fed Induction Machine: Modeling and Control for Wind Energy Generation Applications.

- Book, Chapters 1-15.” Wiley-IEEE Press, 2011. [Online]. Available: <https://ieeexplore.ieee.org/book/6047757>.
- [116] X. Zhang, Q. Li, S. Yang, Z. Xie and R. Cao, "Response and Protection of DFIG System under Grid Fault," *2010 Asia-Pacific Power and Energy Engineering Conference*, Chengdu, China, 2010, pp. 1-5, doi: 10.1109/APPEEC.2010.5448355.
 - [117] J. Morren and S. W. H. Haan, "Ridethrough of Wind Turbines with Doubly-Fed Induction Generator During a Voltage Dip. IEEE TRANSACTIONS ON ENERGY CONVERSION," vol. 20, no. 2. Jun. 2005.
 - [118] C. Rahmann, H.-J. Haubrich, L. Vargas, and M. B. C. Salles, "Investigation of DFIG with Fault Ride-Through Capability in Weak Power Systems."
 - [119] Tao Sun. *Power Quality of Grid-Connected Wind Turbines with DFIG and Their Interaction with the Grid*. Institute of. Denmark: Energy Technology Aalborg University, 2004.
 - [120] H.-J. Haubrich, L. Vargas and M. B. C. Salles, C. Rahmann. Investigation of DFIG with Fault Ride-Through Capability in Weak Power Systems. International Conference on Power Systems Transients (IPST2009) in Kyoto, Japan June 3-6, 2009
 - [121] D. Xie, Z. Xu, L. Yang, J. Østergaard, Y. Xue and K. P. Wong, "A Comprehensive LVRT Control Strategy for DFIG Wind Turbines With Enhanced Reactive Power Support," in *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3302-3310, Aug. 2013.
 - [122] M. Ezzat and M. Benbouzid, "Sm Mueen, Lennart Harnefors. Low-Voltage RideThrough Techniques for DFIG-Based Wind Turbines: State-of-the-Art Review and Future Trends," *IEEE IECON*, pp. 7681-7686, Nov. 2013.
 - [123] M. Rahimi and M. Parniani, "Efficient control scheme of wind turbines with doubly fed induction generators for low-voltage ride-through capability enhancement," *IET Renewable Power Generation*, vol. 4, n°3, pp. 242-252, 2010.
 - [124] F. K. A. Lima, A. Luna, P. Rodriguez, E. H. Watanabe and F. Blaabjerg, "Rotor Voltage Dynamics in the Doubly Fed Induction Generator During Grid Faults," in *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 118-130, Jan. 2010, doi: 10.1109/TPEL.2009.2025651.
 - [125] J. Liang; W. Qiao and R.G. Harley, "Feed-forward transient current control for low-voltage ride-through enhancement of DFIG wind turbines," *IEEE. Trans. Energy Conversion*, vol. 25, n°3, pp. 836-843, September 2010.
 - [126] L. Xu and Y. Wang, "Dynamic Modeling and Control of DFIG-Based Wind Turbines Under Unbalanced Network Conditions," in *IEEE Transactions on Power Systems*, vol. 22, no. 1, pp. 314-323, Feb. 2007, doi: 10.1109/TPWRS.2006.889113.

- [127] W. E. Vanço, F. B. Silva and J. R. B. A. Monteiro, "A Study of the Impacts Caused by Unbalanced Voltage (2%) in Isolated Synchronous Generators," in *IEEE Access*, vol. 7, pp. 72956-72963, 2019, doi: 10.1109/ACCESS.2019.2919298.
- [128] J. Kearney, M. F. Conlon and E. Coyle, "The integrated control of the rotor side and grid side converters in a DFIG to reduce both power and torque pulsations during network voltage unbalance conditions," *2009 44th International Universities Power Engineering Conference (UPEC)*, Glasgow, UK, 2009, pp. 1-5.
- [129] L. Fan, H. Yin and R. Kavasseri, "Negative sequence compensation techniques of DFIG-based wind energy systems under unbalanced grid conditions," *2009 IEEE Power Electronics and Machines in Wind Applications*, Lincoln, NE, USA, 2009, pp. 1-6, doi: 10.1109/PEMWA.2009.5208402.
- [130] V. -T. Phan and H. -H. Lee, "Performance Enhancement of Stand-Alone DFIG Systems With Control of Rotor and Load Side Converters Using Resonant Controllers," in *IEEE Transactions on Industry Applications*, vol. 48, no. 1, pp. 199-210, Jan.-Feb. 2012, doi: 10.1109/TIA.2011.2175883.
- [131] J. Hu, "Hailiang Xu; Yikang He, "Coordinated Control of DFIG's RSC and GSC Under Generalized Unbalanced and Distorted Grid Voltage Conditions," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 7, pp. 2808, 2819, Jul. 2013.
- [132] M. Ferrari, "GSC control strategy for harmonic voltage elimination of grid-connected DFIG wind turbine," *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, Milwaukee, WI, USA, 2014, pp. 185-191, doi: 10.1109/ICRERA.2014.7016554.
- [133] M. Ferrari, "DFIG models for real-time simulations, available at." [Online]. Available: https://code.ornl.gov/f4e/labview-based-dfig-real-time-simulator/-/milestones?sort=start_date_asc

CHAPTER 5

- [134] Y. Yang, P. Enjeti, and F. Blaabjerg, "Wide-scale adoption of photo- voltaic energy: grid code modifications are explored in the distribution grid," *IEEE Industry Applications Magazine*, vol. 21, no. 5, pp. 21-31, Sep. 2015.
- [135] "IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," in *IEEE Std 1547-2018*, 2018.
- [136] A. Hooshyar and R. Iravani, "Microgrid Protection," in *Proceedings of the IEEE*, vol. 105, no. 7, pp. 1332-1353, July 2017, doi: 10.1109/JPROC.2017.2669342.
- [137] S. Gonzalez, N. Gurule, M. J. Reno, and J. Johnson, "Fault Current Experimental Results of Photovoltaic Inverters Operating with Grid- Support Functionality," in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)*, Waikoloa Village, HI, 2018, pp. 1406–1411.

- [138] M. Mirhosseini, J. Pou, and V. G. Agelidis, "Single- and two-stage in-verter-based grid-connected photovoltaic power plants with ride-through capability under grid faults," *IEEE Transactions on Sustainable Energy*, vol. 6, no. 3, pp. 1150-1159, Jul. 2015.
- [139] M. Easley, S. Jain, and M. B. Shadmand, "Computationally efficient distributed predictive controller for cascaded multilevel impedance source inverter with LVRT capability," *IEEE Access*, vol. 7, pp. 35731-35742, Jul. 2019.
- [140] M. Talha, S. R. S. Raihan, and N. A. Rahim, "A Grid-tied PV Inverter with Sag-severity-independent Low-voltage Ride Through, Reactive Power Support, and Islanding Protection," *Journal of Modern Power Systems and Clean Energy*, vol. 9, no. 6, pp. 1300-1311, Nov. 2021.
- [141] C. T. Lee, C. W. Hsu, P. T. Cheng, "A low-voltage ride-through technique for grid-connected converters of distributed energy resources," *IEEE Trans. Ind. Appl.*, 2011, vol. 47, no. 4, pp. 1821-1832.
- [142] N. H. Saad, A. A. El-Sattar, A.E.-A. M. Mansour, "Improved particle swarm optimization for photovoltaic system connected to the grid with low voltage ride through capability," *Renew. Energy*, 2016, 85, pp. 181-194.
- [143] M. Ferrari and L. M. Tolbert, "Inverter Design with High Short-Circuit Fault Current Contribution to Enable Legacy Overcurrent Protection for Islanded Microgrids," *2022 IEEE Power & Energy Society General Meeting (PESGM)*, 2022, pp. 1-5.
- [144] *IHS ISUPPLI Teardown analysis of solar inverter, identifying the cost-reduction opportunities* (no date) *AltEnergyMag*. Available at: <https://www.altenergymag.com/article/2012/01/ihs-isuppli-teardown-analysis-of-solar-inverter-identifying-the-cost-reduction-opportunities/997/> (Accessed: February 4, 2023).
- [145] M. G. Villalva, J. R. Gazoli and E. R. Filho, "Modeling and circuit-based simulation of photovoltaic arrays," *2009 Brazilian Power Electronics Conference*, 2009, pp. 1244-1254.
- [146] 3-Phase Motor Control Demonstration Board featuring IGBT intelligent. Available at: <https://www.st.com/resource/>
- [147] Bechtold, J. G. Korvink, E. B. Rudnyi, *Fast Simulation of Electro- Thermal MEMS: Efficient Dynamic Compact Models*, Springer, New York, 2007.
- [148] "ST-power studio 1.2.", [online]. Available at <https://www.st.com/en/embedded-software/stsw-powerstudio.html>
- [149] Y. Liu, L. M. Tolbert, P. Kritprajun, J. Dong, L. Zhu, J. Hambrick, K. P. Schneider, K. Prabakar, "Aging Effect Analysis of PV Inverter Semiconductors for Ancillary Services Support," *IEEE Open Journal of Industry Applications*, vol. 1, 2020, pp. 157-170.

- [150] M Maximiliano Ferrari, Travis Smith, Neil Shepard¹, Aditya Sundararajan, Drew Herron , Emilio Piesciorovsky, Isabelle Snyder, Ben Ollis, Josh Hambrick, Chris Sticht, Mike Marshall, " Real-Time Model-Adaptive Relaying Applied to Microgrid Protection," *2023 IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*, Washington, DC, USA
- [151] M. Ferrari, E. C. Piesciorovsky, T. Smith and J. Hambrick, "Cost-Effective Three-Phase Current Amplifier Interface for Real-time Simulator with Relays in-the-Loop," *2019 North American Power Symposium (NAPS)*, Wichita, KS, USA, 2019, pp. 1-5, doi: 10.1109/NAPS46351.2019.9000320.
- [152] D. Gao et al. "Comparison of Standard and Technical Requirements of Grid-Connected Wind Power Plants in China and the United States". Technical Report. NREL September 2016.
- [153] S. -F. Chou, X. Wang, H. Matsumori, T. Shimizu and F. Blaabjerg, "Linearized Modeling and Controller Design of the Nonlinear Inductors in $\alpha\beta$ -frame," 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, 2018, pp. P.1-P.9.

APPENDIX

• NONLINEAR INDUCTOR MODELING

This section shows a method to estimate the impedance using a three-phase converter. The only hardware modification is that a linear inductor (that saturates at 40A) is used as a grid filter, and the nonlinear inductor to characterize becomes the load. The computer implementation shown in Fig. A1 is implemented in the real-time layer to for an online estimation of the inductance. The voltages are measured at the terminals of the nonlinear inductor. For the test, the terminals of the inductors are short-circuited. The voltage across the inductor is set using open loop control in the inverter, where the d-channel voltage V_d is set as a ramp from 0 to 0.7, which corresponds to a current of 0 to 30 A in the ac side. Slowly increasing the current from zero it's important to prevent oscillation in the currents.

By measuring ac voltages and currents, the estimation can be performed as follows:

$$V_{abc} = 3r_f i_{abc} + 3i\omega_s L_f i_{abc} \quad (\text{A.1})$$

From a power balance analysis

$$r_f = \frac{P_{ac}}{3|I_{ac}|^2} \text{ and } L_f = \frac{Q_{ac}}{3\omega_s |I_{ac}|^2}. \quad (\text{A.2})$$

The active and reactive powers to be measured in the experiment are three-phase and calculated as presented in Fig. A.1. Low pass filters are also applied to the voltages and currents, but no phase compensation is required since they are both tuned at the same cutoff frequency.

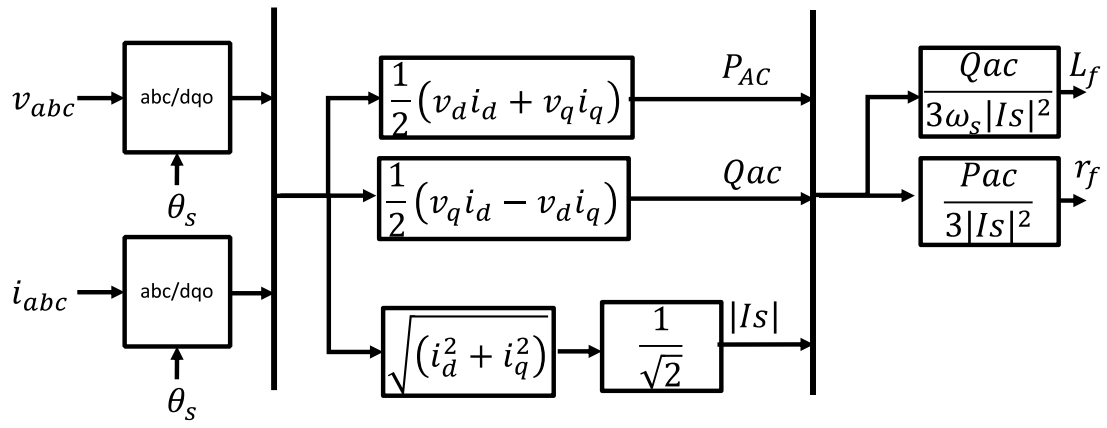
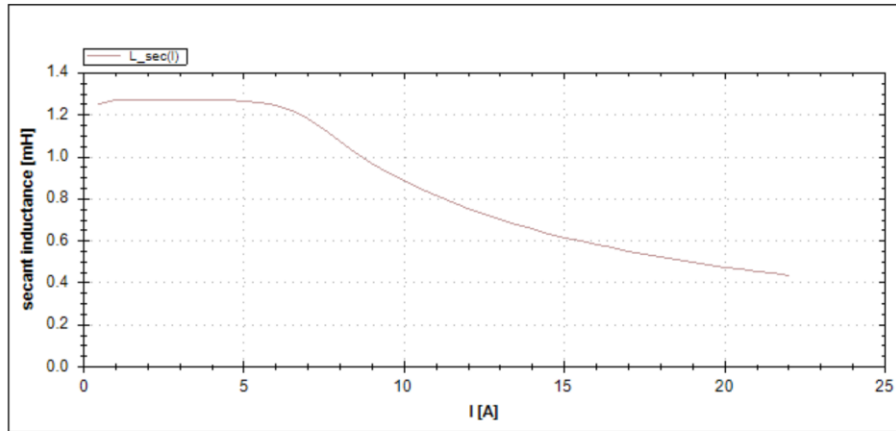


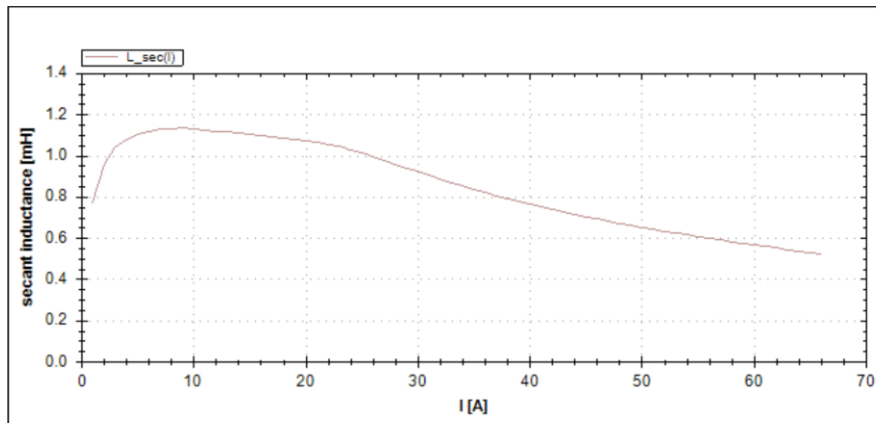
Figure A.1: Grid filter inductance and resistance estimation by three-phase P_{ac} and Q_{ac} calculation.

D.U.T.: coilcraft 1mH
Inspector:
Date: 2/9/2022 3:58:47 PM
Parameters: 25 A / 50 V / 7000 (196) μ s
Resistance [Ohm]: 0.0532



(a)

D.U.T.: Silicon Steel 1mH
Inspector:
Date: 2/9/2022 4:14:04 PM
Parameters: 70 A / 50 V / 7000 (718) μ s
Resistance [Ohm]: 0.0436



(b)

Figure A.2: Grid filter inductance and resistance estimation (a) Ferrite core,(b) Steel Core.

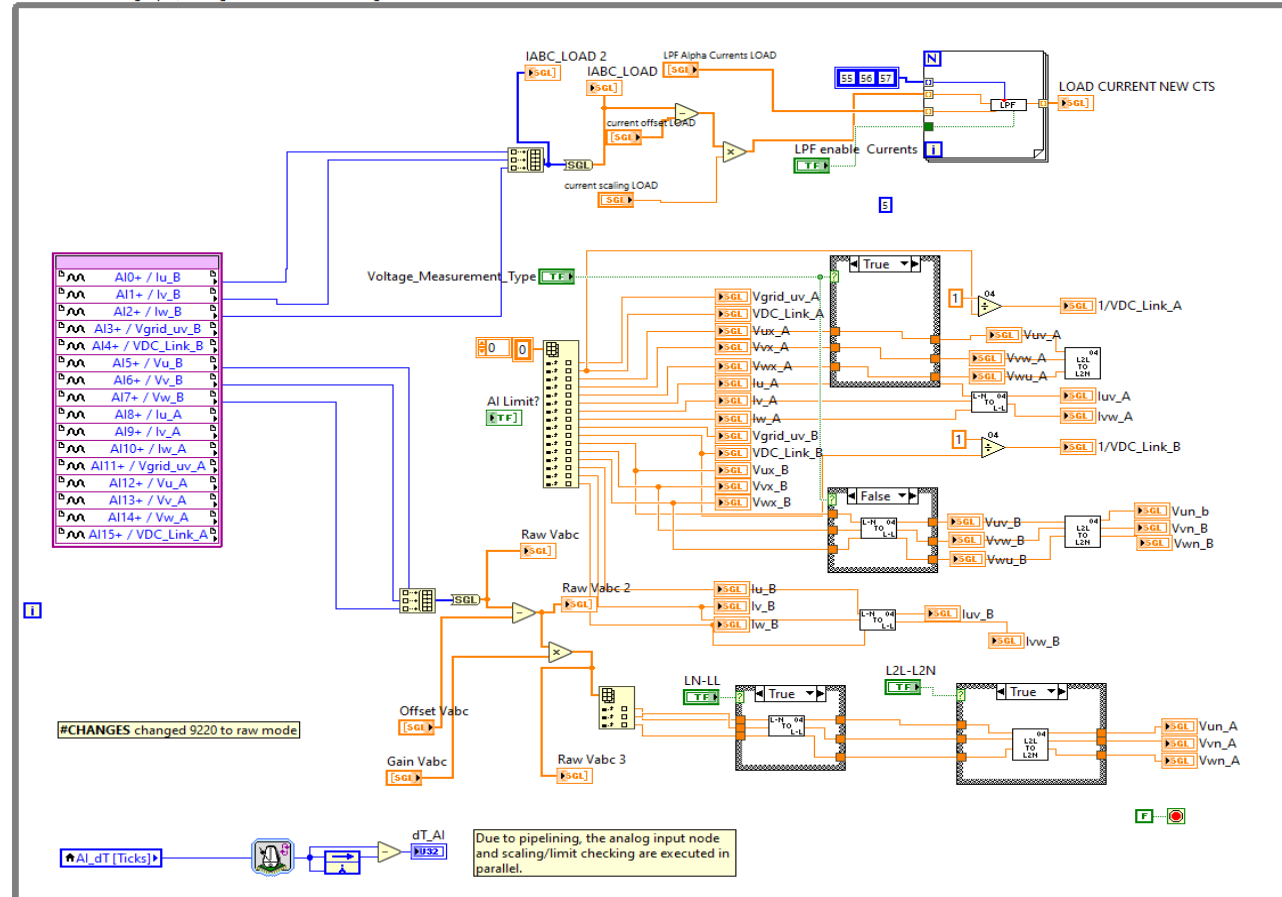


Figure A.3: LabVIEW FPGA Data Acquisition of voltages and currents

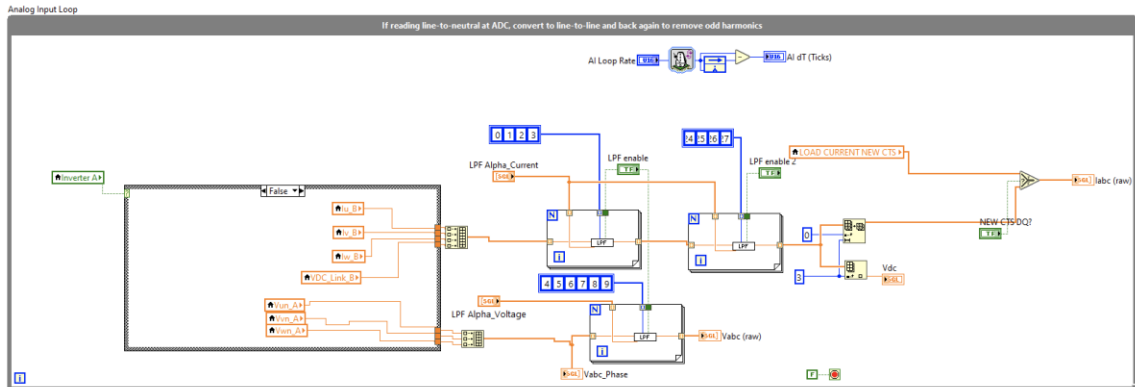


Figure A.4: LabVIEW FPGA Low Pass Filtering

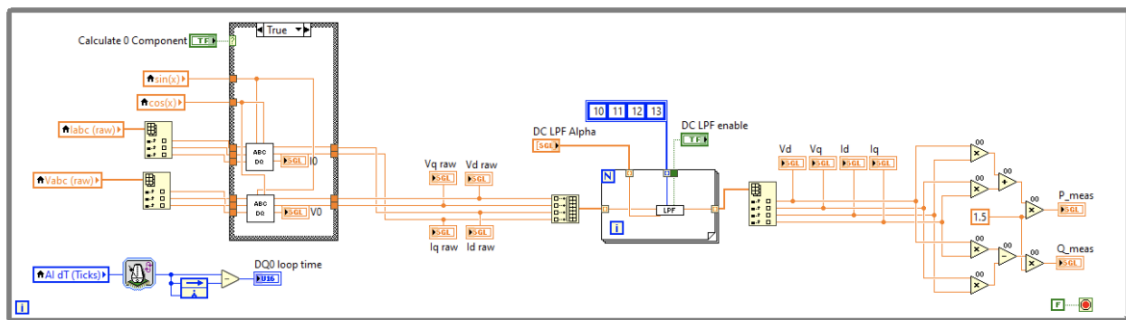


Figure A.5: LabVIEW FPGA Clarke-Parke transformations

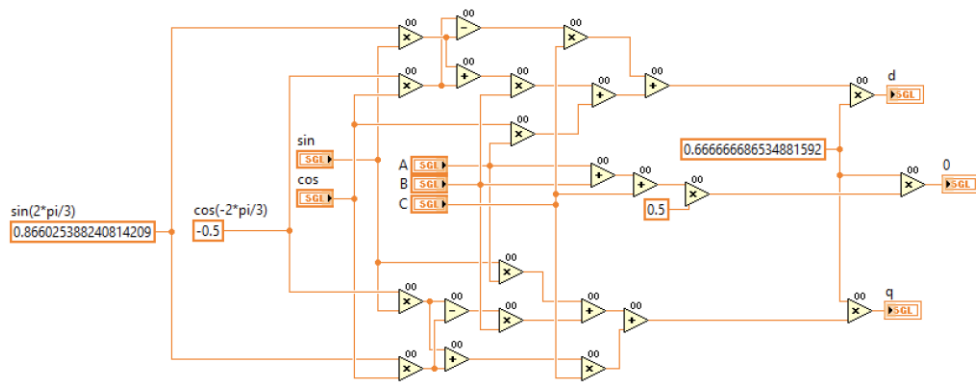


Figure A.6: LabVIEW FPGA Clarke-Parke transformations 2

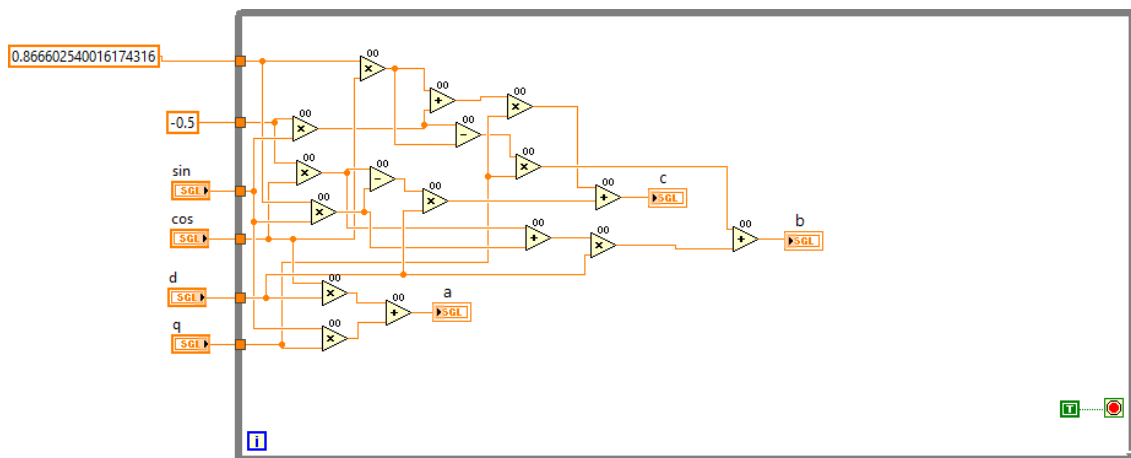


Figure A.7: LabVIEW FPGA Clarke-Parke transformations 3

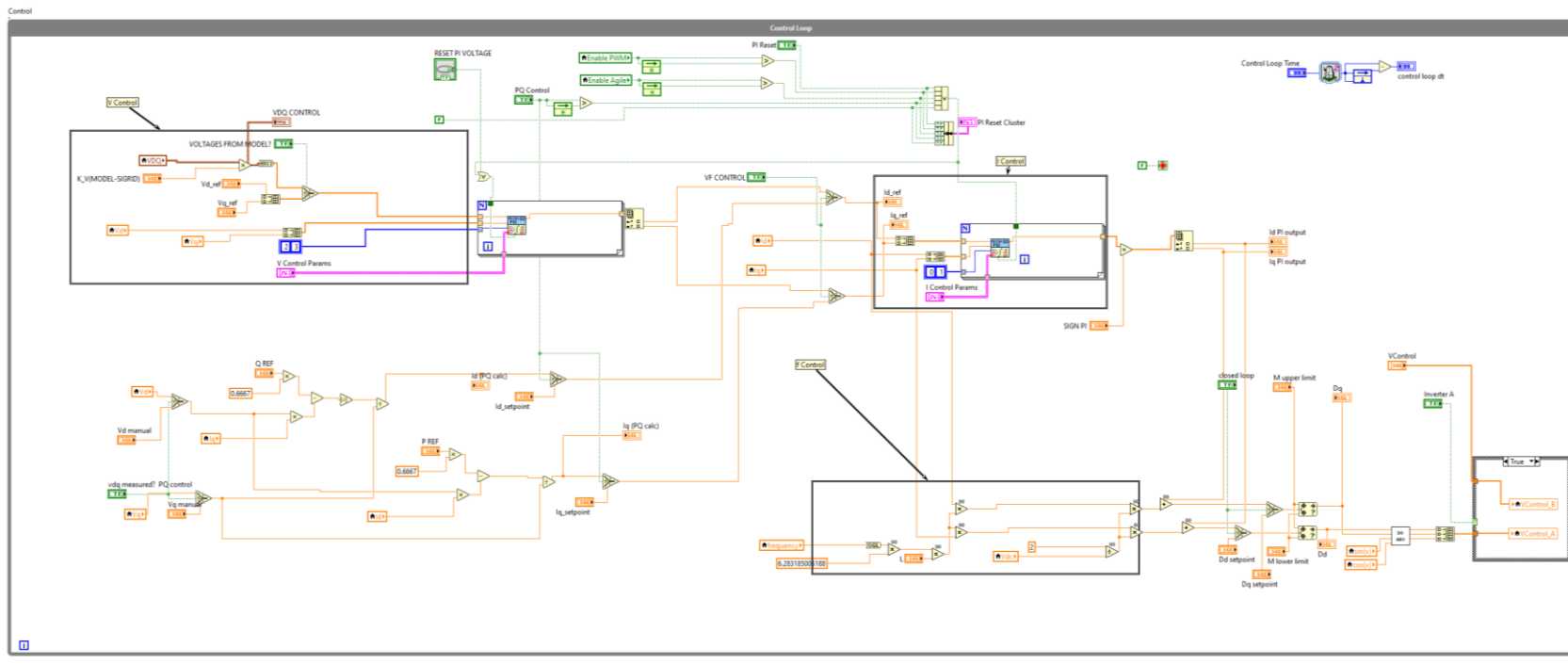


Figure A.9: Vector Control VSC

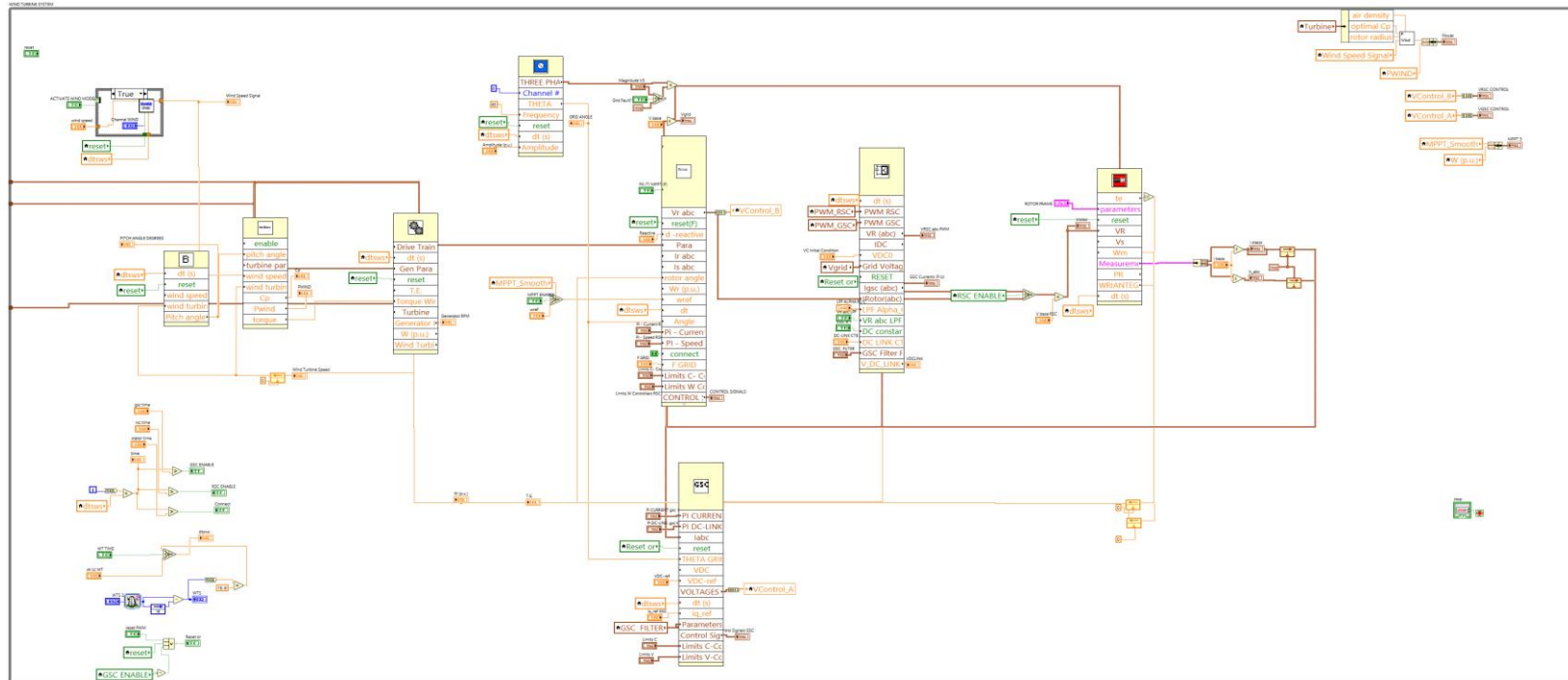


Figure A.10: DFIG real-time simulator

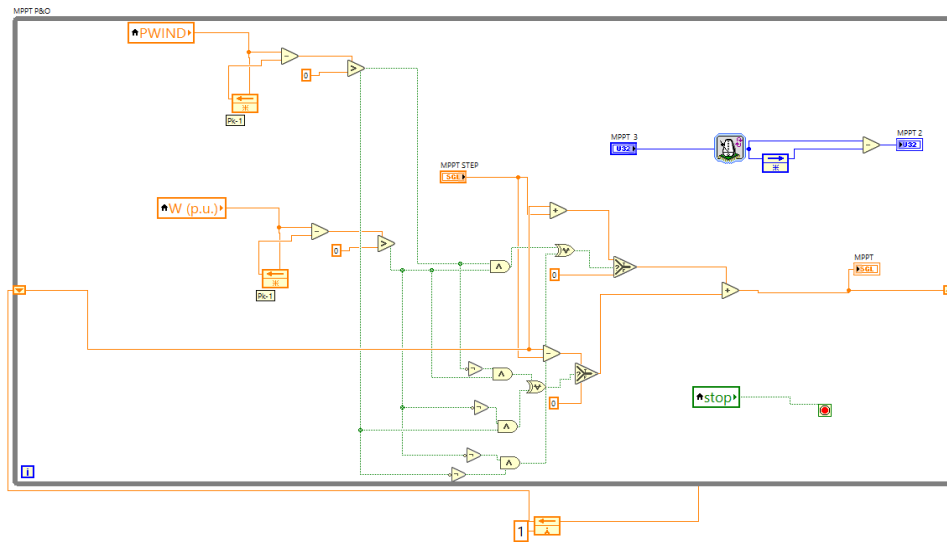


Figure A.11: DFIG real-time simulator. (a) Mechanical and electrical models. (b) Maximum Power Point Perturb and Observe. (c) PWM

```

syms theta Lo L2 L4 L6 labc l Labc Labc2 La_n1 Lb_n1 Lc_n1 La_n2 Lb_n2 Lc_n2 Labc_n1 Labc_n2 La_n3 Lb_n3 Lc_n3
deri w a b c d L1 L3 La_no Lb_no Lc_no Labc_no Labc_n11 Id Iq w t Iz s

%T=Clarke-Park transformation
T=sqrt(2/3)*[cos(w*t), cos(w*t-2/3*pi),cos(w*t+2/3*pi);-sin(w*t), -sin(w*t-2/3*pi),-sin(w*t+2/3*pi)];

%T=Inverse Clarke-Park transformation
Tinv=transpose(T);

%T=Three-phase currents
labc=[I*cos(w*t);I*cos(w*t-2*pi/3);I*cos(w*t+2*pi/3)];

%T=Fit equation polynomial

Labc=[Lo,0,0;0,Lo,0;0,0,Lo];

La_no=(L1*(I*cos(theta)));
Lb_no=(L1*(I*cos(theta-2*pi/3)));
Lc_no=(L1*(I*cos(theta+2*pi/3)));

La_n1=L2*(I*cos(theta))^2;
Lb_n1=L2*(I*cos(theta-2*pi/3))^2;
Lc_n1=L2*(I*cos(theta+2*pi/3))^2;

La_n2=L3*(I*cos(theta))^3;
Lb_n2=L3*(I*cos(theta-2*pi/3))^3;
Lc_n2=L3*(I*cos(theta+2*pi/3))^3;

La_n3=L4*(I*cos(theta))^4;
Lb_n3=L4*(I*cos(theta-2*pi/3))^4;
Lc_n3=L4*(I*cos(theta+2*pi/3))^4;

Labc_no=[La_no,0,0;0,Lb_no,0;0,0,Lc_no];
Labc_n1=[La_n1,0,0;0,Lb_n1,0;0,0,Lc_n1];
Labc_n2=[La_n2,0,0;0,Lb_n2,0;0,0,Lc_n2];
Labc_n3=[La_n3,0,0;0,Lb_n3,0;0,0,Lc_n3];

%Fit equation polynomial, second order

Labc_n1=Labc+Labc_n1;

%Solving

a=simplify(diff(T*Labc_n1,t)*Tinv);

b=simplify(T*Labc_n1*diff(Tinv,t));
c=simplify(T*Labc_n1*Tinv);

a*Idq+b*Idq+c*s*Idq;

aa=simplify(diff(T,t)*Labc_n1);
aaa=simplify(T*diff(Labc_n1,t));
A=simplify((aa+aaa)*Tinv);
A=simplify(b*Idq+c*s*Idq)

```

Figure A.12: Matlab code for solving second-order polynomial

Although these machine models are extensively presented in the literature, there are not studies that explicitly address the execution and use of logical resources of these models. For this reason, this section presents a benchmark that compares the use of resources of the following models in the FPGA: stator reference frame, rotor reference frame, synchronous reference frame and the natural frame. This is useful because an efficient implementation of the machine model is necessary to run the machine model in real time.

The following figures illustrate the four machine models and their implementation in the FPGA. The FPGA simulation shows the behavior of the machine variables in real time and allows for comparison between their execution performance, memory usage, and logic resources.

The equivalent model of the DFIG using the Stator Reference Frame is shown in Figure A.13, and its LabVIEW implementation in Fig. A.14. The equivalent model of the Rotor Reference Frame is shown in Figure A.15, and its LabVIEW implementation in Fig. A.16. The equivalent model of the Synchronous Reference Frame is shown in Figure A.17, and its LabVIEW implementation in Fig. A.18. Finally, Figure A.19 shows Natural Reference Frame Machine Model and Figure A.20 its LabVIEW implementation.

Table A.1 summarizes the required resources for each of the models. The natural frame model requires significantly more mathematical operators, and more trigonometrical functions than the other models, which makes it computationally intensive. The synchronous reference frame doubles the use of trigonometrical functions compared with the stator and rotor frames, and it requires the calculation of the grid and the rotor angles, which adds two additional integrators. From all the models, the rotor reference frame is the most efficient implementation of the DFIG machine.

$$\begin{aligned}
\frac{d}{dt} \begin{bmatrix} i_{\alpha s} \\ i_{\beta s} \\ i_{\alpha r} \\ i_{\beta r} \end{bmatrix} &= \begin{bmatrix} \frac{-R_s}{\sigma \cdot L_s} & \frac{\omega_m \cdot L_h^2}{\sigma \cdot L_s \cdot L_r} & \frac{R_r \cdot L_h}{\sigma \cdot L_s \cdot L_r} & \frac{\omega_m \cdot L_h}{\sigma \cdot L_s} \\ \frac{-\omega_m \cdot L_h^2}{\sigma \cdot L_s \cdot L_r} & \frac{-R_s}{\sigma \cdot L_s} & \frac{-\omega_m \cdot L_h}{\sigma \cdot L_s} & \frac{R_r \cdot L_h}{\sigma \cdot L_s \cdot L_r} \\ \frac{R_s \cdot L_h}{\sigma \cdot L_s \cdot L_r} & \frac{-\omega_m \cdot L_h}{\sigma \cdot L_r} & \frac{-R_r}{\sigma \cdot L_r} & \frac{-\omega_m}{\sigma} \\ \frac{\omega_m \cdot L_h}{\sigma \cdot L_r} & \frac{R_s \cdot L_h}{\sigma \cdot L_s \cdot L_r} & \frac{\omega_m}{\sigma} & \frac{-R_r}{\sigma \cdot L_r} \end{bmatrix} \begin{bmatrix} i_{\alpha s} \\ i_{\beta s} \\ i_{\alpha r} \\ i_{\beta r} \end{bmatrix} + \\
&+ \begin{bmatrix} \frac{1}{\sigma \cdot L_s} & 0 & \frac{-L_h}{\sigma \cdot L_s \cdot L_r} & 0 \\ 0 & \frac{1}{\sigma \cdot L_s} & 0 & -L_h \\ \frac{-L_h}{\sigma \cdot L_s \cdot L_r} & 0 & \frac{1}{\sigma \cdot L_r} & 0 \\ 0 & \frac{-L_h}{\sigma \cdot L_s \cdot L_r} & 0 & \frac{1}{\sigma \cdot L_r} \end{bmatrix} \begin{bmatrix} v_{\alpha s} \\ v_{\beta s} \\ v_{\alpha r} \\ v_{\beta r} \end{bmatrix}
\end{aligned}$$

Figure A.13: (a) Stator reference frame machine model [133].

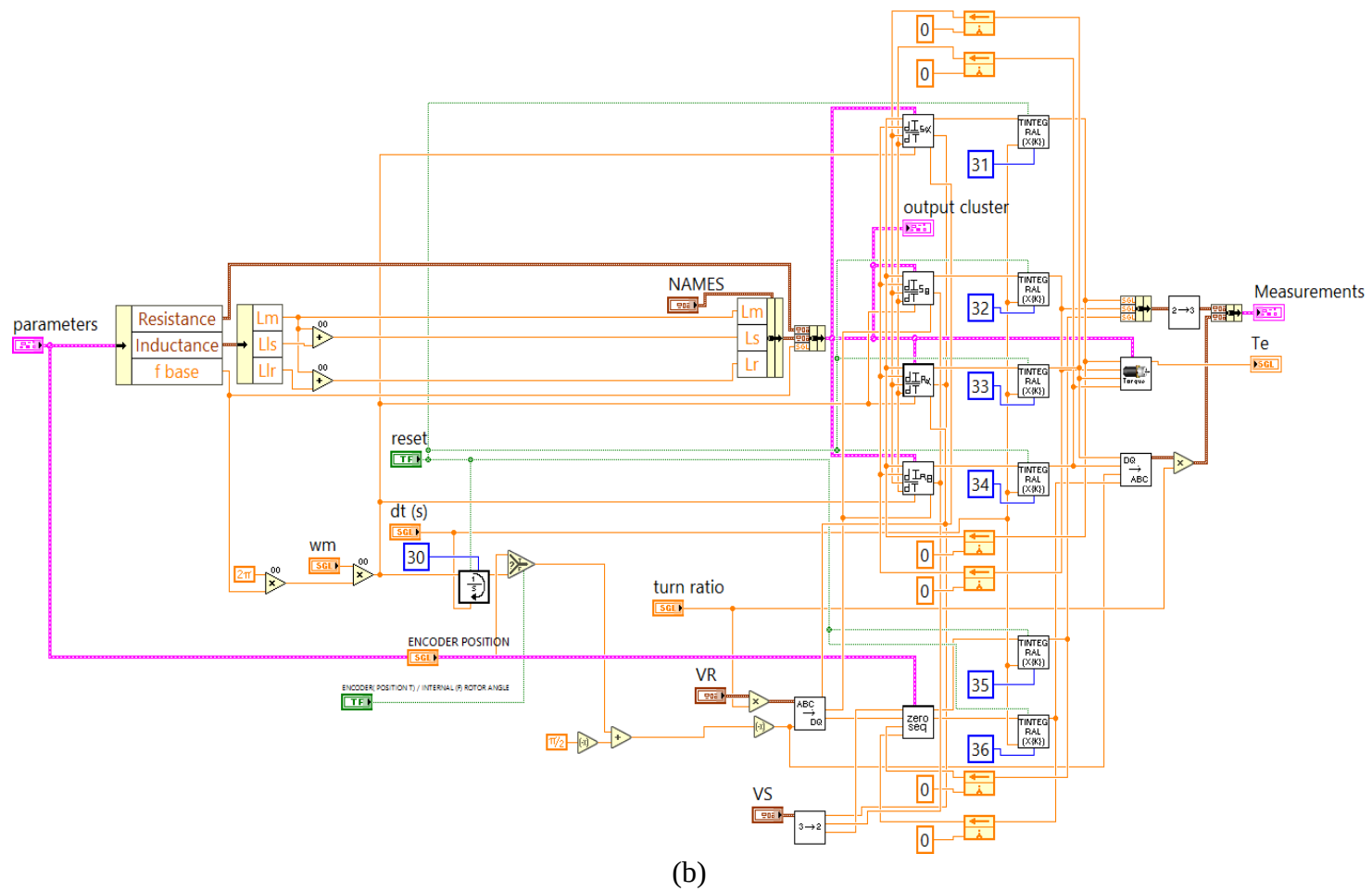


Figure A.14: FPGA implementation stator reference frame machine model.. Model available in open repository [133].

$$\frac{d}{dt} \begin{bmatrix} \psi_{\alpha s} \\ \psi_{\beta s} \\ \psi_{\alpha r} \\ \psi_{\beta r} \end{bmatrix} = \begin{bmatrix} \frac{-R_s}{\sigma L_s} & 0 & \frac{R_s L_m}{\sigma L_s L_r} & 0 \\ 0 & \frac{-R_s}{\sigma L_s} & 0 & \frac{R_s L_m}{\sigma L_s L_r} \\ \frac{R_r L_m}{\sigma L_s L_r} & 0 & \frac{-R_r}{\sigma L_r} & -\omega_m \\ 0 & \frac{R_r L_m}{\sigma L_s L_r} & \omega_m & \frac{-R_r}{\sigma L_r} \end{bmatrix} \cdot \begin{bmatrix} \psi_{\alpha s} \\ \psi_{\beta s} \\ \psi_{\alpha r} \\ \psi_{\beta r} \end{bmatrix} + \begin{bmatrix} v_{\alpha s} \\ v_{\beta s} \\ v_{\alpha r} \\ v_{\beta r} \end{bmatrix}$$

Figure A.15: Rotor Reference Frame Machine Model.

$$\frac{d}{dt} \begin{bmatrix} i_{ds} \\ i_{qs} \\ i_{os} \\ i_{dr} \\ i_{qr} \\ i_{or} \end{bmatrix} = \left(\frac{1}{sL_s L_r} \right) \begin{bmatrix} -r_s L_r & w_s s L_s L_r + w_m L_m^2 & 0 & r_r L_m & w_m L_m L_r & 0 \\ w_s s L_s L_r - w_m L_m^2 & -r_s L_r & 0 & -w_m L_m L_r & r_r L_m & 0 \\ 0 & 0 & -\frac{r_s s L_s L_r}{L_s} & 0 & 0 & 0 \\ r_s L_m & -w_m L_s L_m & 0 & -r_r L_s & -w_m L_r L_s + w_s s L_s L_r & 0 \\ w_m L_s L_m & r_s L_m & 0 & w_m L_s L_r - w_s s L_s L_r & -r_r L_s & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{r_r s L_s L_r}{L_r} \end{bmatrix} \begin{bmatrix} i_{ds} \\ i_{qs} \\ i_{os} \\ i_{dr} \\ i_{qr} \\ i_{or} \end{bmatrix} + \left(\frac{1}{sL_s L_r} \right) \begin{bmatrix} L_r & 0 & 0 & -L_m & 0 & 0 \\ 0 & L_r & 0 & 0 & -L_m & 0 \\ 0 & 0 & sL_r & 0 & 0 & 0 \\ -L_m & 0 & 0 & L_s & 0 & 0 \\ 0 & -L_m & 0 & 0 & L_s & 0 \\ 0 & 0 & 0 & 0 & 0 & sL_s \end{bmatrix} \begin{bmatrix} v_{ds} \\ v_{qs} \\ v_{os} \\ d_{dr} V_{dc} \\ d_{qr} V_{dc} \\ d_{or} V_{dc} \end{bmatrix}$$

Figure A.17: Synchronous reference frame model.

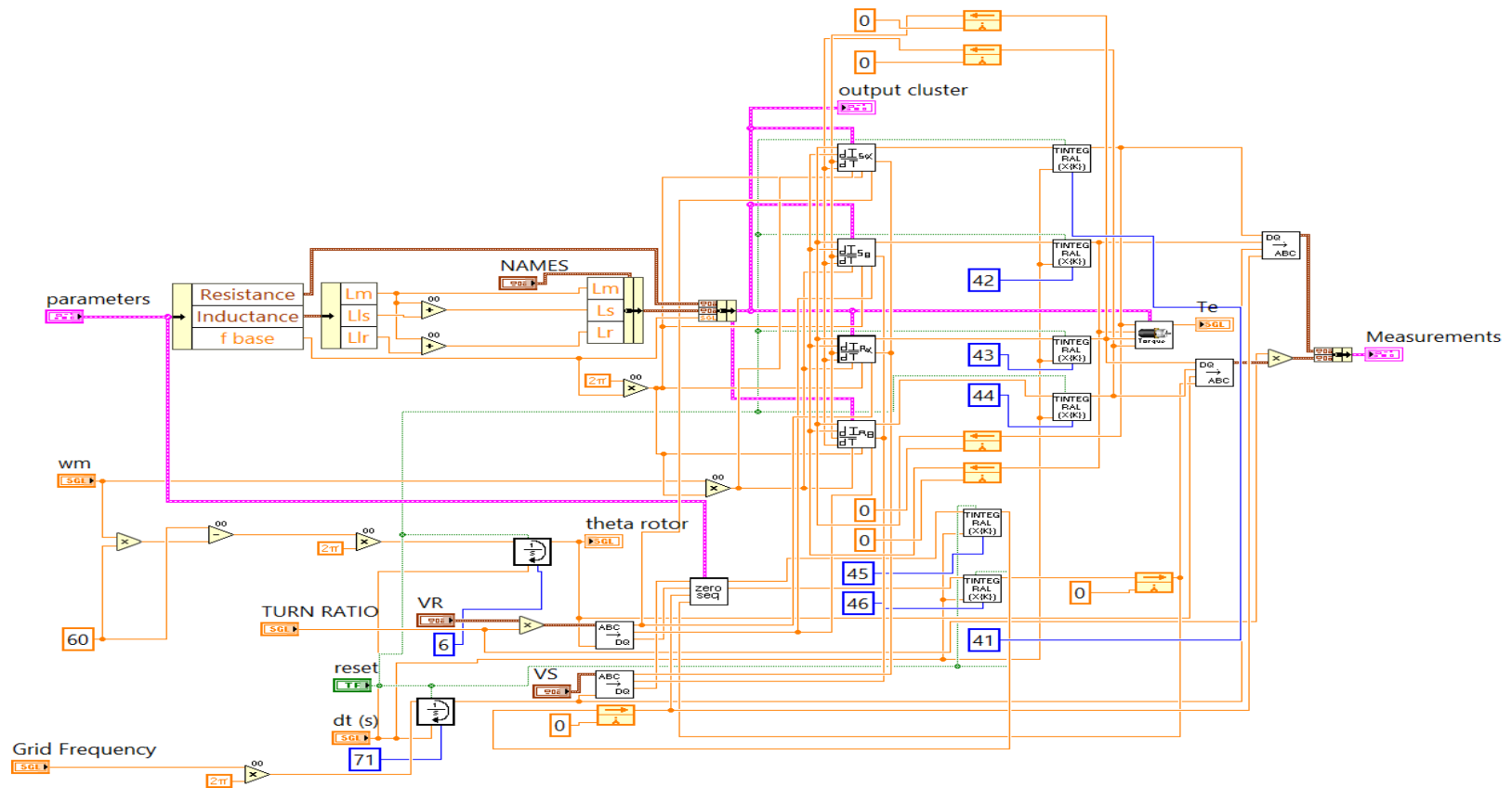


Figure A.18: Synchronous reference frame model FPGA implementation. Available at [133].

$$\begin{aligned}
\frac{d}{dt} \begin{bmatrix} \mathcal{Y}_{as} \\ \mathcal{Y}_{bs} \\ \mathcal{Y}_{cs} \end{bmatrix} &= \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} - \begin{bmatrix} r_s (L_s - L_m L_r^{-1} L_m^T)^{-1} & 0 & 0 \\ 0 & r_s (L_s - L_m L_r^{-1} L_m^T)^{-1} & 0 \\ 0 & 0 & r_s (L_s - L_m L_r^{-1} L_m^T)^{-1} \end{bmatrix} \begin{bmatrix} \mathcal{Y}_{as} \\ \mathcal{Y}_{bs} \\ \mathcal{Y}_{cs} \end{bmatrix} + \begin{bmatrix} r_s (L_s - L_m L_r^{-1} L_m^T)^{-1} L_m L_r^{-1} & 0 & 0 \\ 0 & r_s (L_s - L_m L_r^{-1} L_m^T)^{-1} L_m L_r^{-1} & 0 \\ 0 & 0 & r_s (L_s - L_m L_r^{-1} L_m^T)^{-1} L_m L_r^{-1} \end{bmatrix} \begin{bmatrix} \mathcal{Y}_{ar} \\ \mathcal{Y}_{br} \\ \mathcal{Y}_{cr} \end{bmatrix} \\
\frac{d}{dt} \begin{bmatrix} \mathcal{Y}_{ar} \\ \mathcal{Y}_{br} \\ \mathcal{Y}_{cr} \end{bmatrix} &= V_{dc} \begin{bmatrix} s_a \\ s_b \\ s_s \end{bmatrix} - \begin{bmatrix} r_r (L_r - L_m^T L_s^{-1} L_m)^{-1} & 0 & 0 \\ 0 & r_r (L_r - L_m^T L_s^{-1} L_m)^{-1} & 0 \\ 0 & 0 & r_r (L_r - L_m^T L_s^{-1} L_m)^{-1} \end{bmatrix} \begin{bmatrix} \mathcal{Y}_{ar} \\ \mathcal{Y}_{br} \\ \mathcal{Y}_{cr} \end{bmatrix} + \begin{bmatrix} r_r (L_r - L_m^T L_s^{-1} L_m)^{-1} L_m^T L_s^{-1} & 0 & 0 \\ 0 & r_r (L_r - L_m^T L_s^{-1} L_m)^{-1} L_m^T L_s^{-1} & 0 \\ 0 & 0 & r_r (L_r - L_m^T L_s^{-1} L_m)^{-1} L_m^T L_s^{-1} \end{bmatrix} \begin{bmatrix} \mathcal{Y}_{as} \\ \mathcal{Y}_{bs} \\ \mathcal{Y}_{cs} \end{bmatrix}
\end{aligned}$$

Figure A.19: Natural Reference Frame machine model.

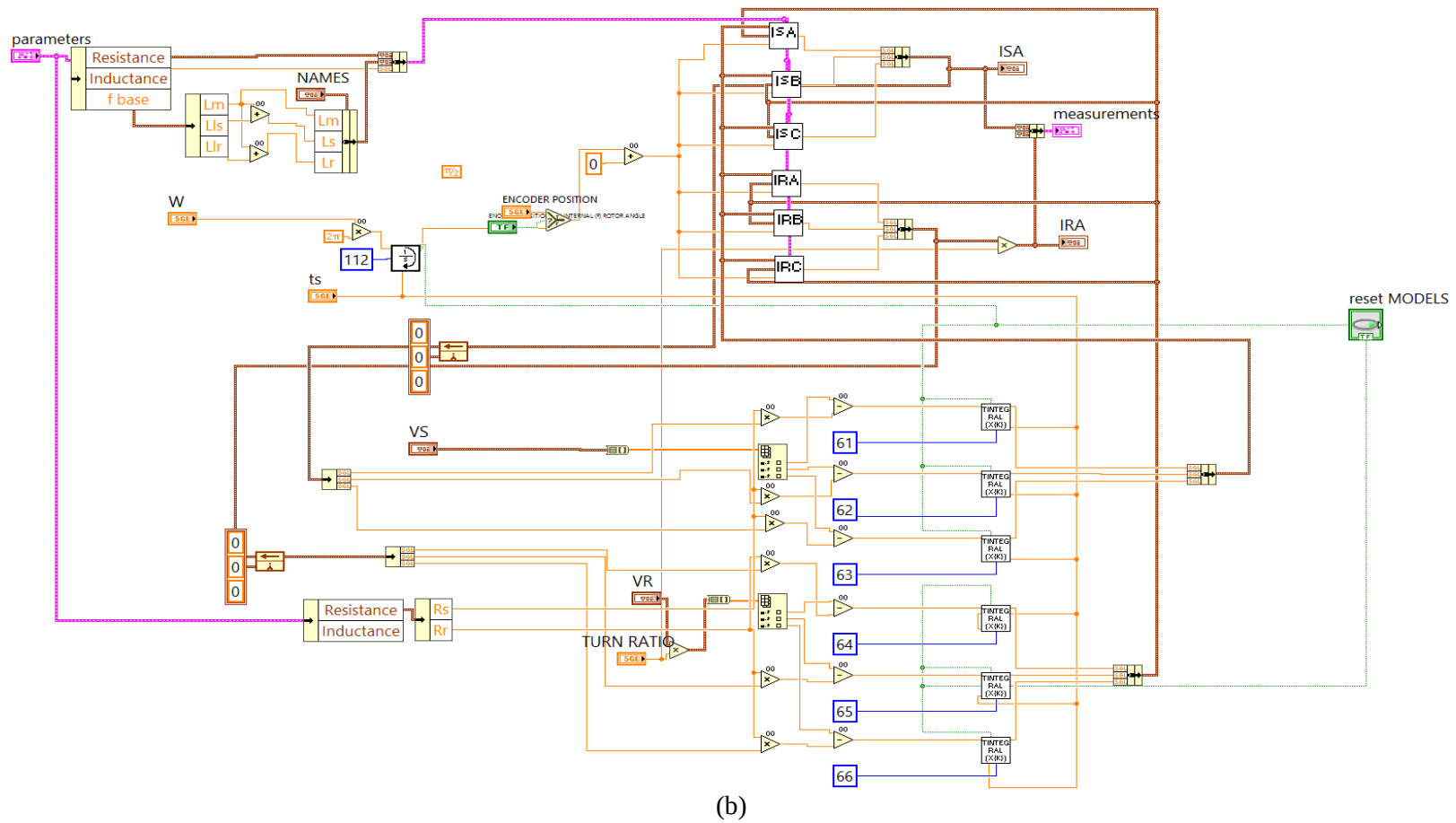


Figure A.20: Natural Reference Frame Machine Model FPGA implementation Available at [133].

Table A.1:
Requirements different DFIG models

	Synchronous	Natural	Rotor	Stator
Sine/Cosine	8	12	4	4
Integrators	8	7	7	7
Operators	120	216	50	104
Stator Angle	yes	no	no	yes
Rotor Angle	yes	yes	yes	no
Zero sequence	yes	yes	yes	yes

VITA

Maximiliano Ferrari was born in Argentina and raised in Colombia. He has degrees in Electronic Engineering, Physics and Master in Electronic System Engineering. Prior to joining the UT, he worked in Information Technology, R&D and Energy Efficiency. In June 2016, Max moved to Knoxville to pursue the Energy Science and Engineering PhD program at the Breiden Center. While a student at UT, Max was awarded with the Student Faculty Award and the McClure scholarship. In 2019 Max joined Oak Ridge National Laboratory, where he is currently working as R&D Assistant Staff Member in the Grid Systems Architecture Group. His research interests include power electronics, microgrids controls and protection.