

Design and Control of Power Converters for High Power-Quality Interface with Utility and Aviation Grids

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Abstract

Power electronics as a subject integrating power devices, electric and electronic circuits, control, and thermal and mechanic design, requires not only knowledge and engineering insight for each subarea, but also understanding of interface issues when incorporating these different areas into high performance converter design.

Addressing these fundamental questions, the dissertation studies design and control issues in three types of power converters applied in low-frequency high-power transmission, medium-frequency converter emulated grid, and high-frequency high-density aviation grid, respectively, with the focus on discovering, understanding, and mitigating interface issues to improve power quality and converter performance, and to reduce the noise emission.

For hybrid ac/dc power transmission,

- Analyze the interface transformer saturation issue between ac and dc power flow under line unbalances.
- Proposed both passive transformer design and active hybrid-line-impedance-conditioner to suppress this issue.

For transmission line emulator,

- Propose general transmission line emulation schemes with extension capability.
- Analyze and actively suppress the effects of sensing/sampling bias and PWM ripple on emulation considering interfaced grid impedance.
- Analyze the stability issue caused by interaction of the emulator and its interfaced impedance. A criterion that determines the stability and impedance boundary of the emulator is proposed.

For aircraft battery charger,

- Investigate architectures for dual-input and dual-output battery charger, and a three-level integrated topology using GaN devices is proposed to achieve high density.
- Identify and analyze the mechanisms and impacts of high switching frequency, di/dt , dv/dt on sensing and power quality control; mitigate solutions are proposed.
- Model and compensate the distortion due to charging transition of device junction capacitances in three-level converters.
- Find the previously overlooked device junction capacitance of the nonactive devices in three-level converters, and analyze the impacts on switching loss, device stress, and current distortion. A loss calculation method is proposed using the data from the conventional double pulse tester.
- Establish fundamental knowledge on performance degradation of EMI filters. The impacts and mechanisms of both inductive and capacitive coupling on different filter structures are understood. Characterization methodology including measuring, modeling, and prediction of filter insertion loss is proposed. Mitigation solutions are proposed to reduce inter-component coupling and self-parasitics.

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1 Introduction

1.1 Application background

With the growing demand on energy, sustained renewable resource, and the expansion of energy market from the centralized grid to a more decentralized grid integrating various distributed energy resources, energy conversion and grid interconnection becomes two major enabling functions. How to convert energy from its original form to the desired form and how to interface with grid for power transmission and absorption in an energy-efficient, cost-effective and customer friendly way are some of the main drives to the development of power electronic technologies, since power converters serve as the main actuation elements.

A traditional grid consists of high voltage high power transmission level and medium to low voltage distribution level. However, from applications perspective, a more generic grid can be grouped as three types: 1) traditional power grid which consists of generators, transmission lines, and load, and serves for the whole nation or local district; 2) A standalone grid providing power exclusively for a certain instrument, device, or system, such as power supply chain for a computer or a local dc and/or ac grid in an airplane or ship; 3) Artificial grid, which mimics the behavior of actual grid for research and study purpose, such as hardware test bed (HTB) using modular voltage source power converter to emulate components of a power system [1].

Owing to different application backgrounds and requirements, the interface between power converters and these three types of grids are quite different, thus must be designed fully considering their unique voltage level, current level, frequency range, and power device characteristics. In this research work, three representatives of grids, i.e. 60 Hz high voltage high power transmission grid, PWM voltage source converter emulated HTB grid, and 360 Hz~800 Hz aircraft grid, as illustrated

in Fig. 1-1, are selected and their interconnection issues with power converters are studied, aiming to enhance the power capacity and improve the power quality.

1.1.1 High power transmission grid

A typical high-power grid in US is illustrated in Fig. 1-2 [2]. Once a generating station generates electricity, the line voltage will be boosted up to hundreds of kV through a generator step-up transformer and sent through transmission lines to substations, where the line voltage is again stepped down to tens of kV and hundreds of volts for industrial and residential use.

In every second, about 8%~15% power energy is being dissipated in the grid itself, and a typical loss breakdown along the grid is shown in Table 1-1 [3]. A significant percentage of loss is from Joule loss in transmission lines due to high current flow and non-negligible line resistance. This loss also contributes to the line temperature rise, limiting the physical rating of transmission line capacity.

However, the long transmission line is desired because the energy resources supporting the electricity demand are not located near load centers. In recent years, with increasing utilization and interconnection of renewables to the power grid and ongoing demands for electric power, high power transmission is drawing tremendous attention. According to [4], the electricity generation in US is predicted to have a 24 % increase from 2015 to 2040. And in 2030, the energy demand in China will exceed 10 PWh [5]. As shown in Fig. 1-3, the worldwide renewable energy consumption is also projected to increase by an average 2.6%/year from 2012 to 2040 [4]. Meanwhile, net electricity consumption and generation worldwide rises about 1.9%/year, as shown in Fig. 1-4 [4].

To increase the power transmission and still maintain reasonable line loss, three basic approaches have been widely applied:

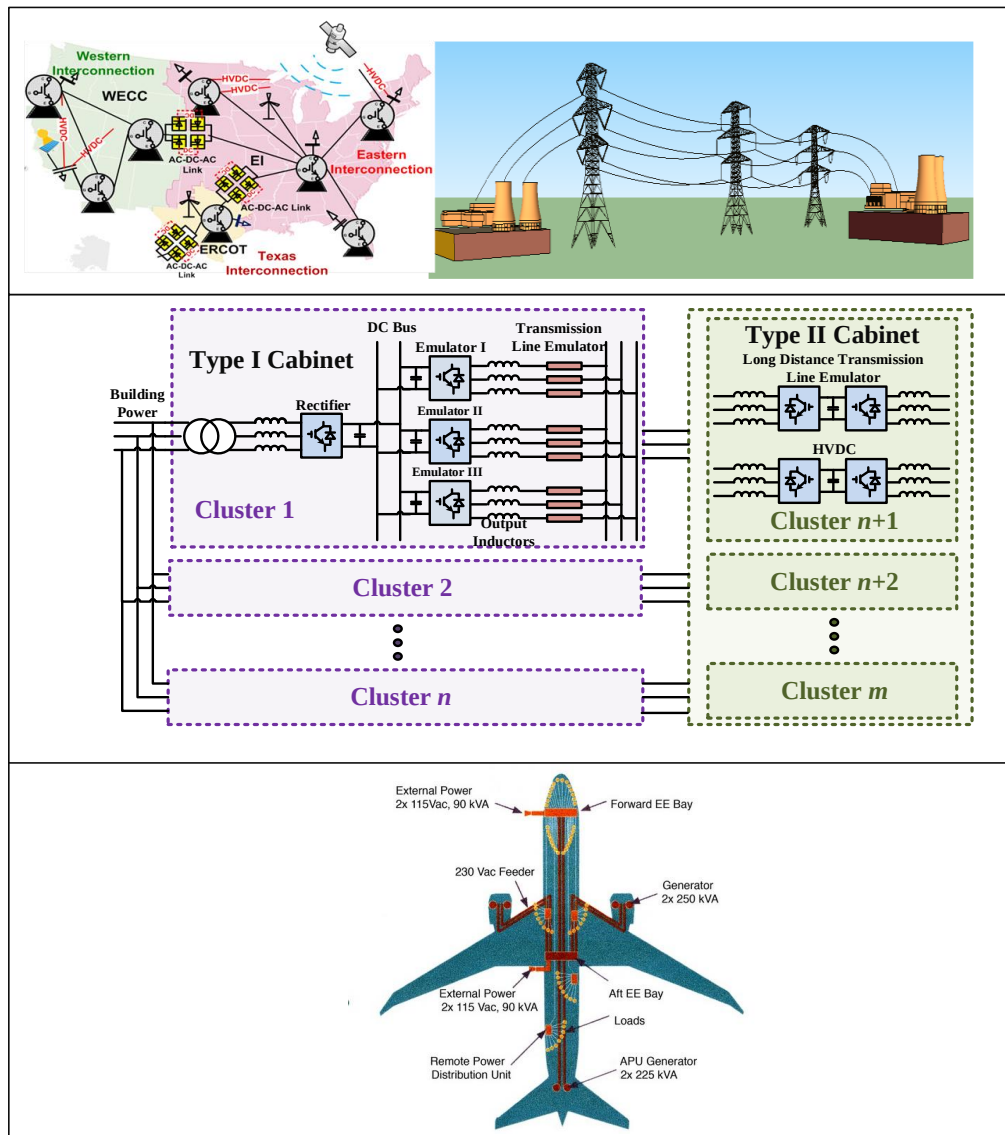


Fig. 1-1. Three types of power converters interfacing with transmission grid and aviation grid.

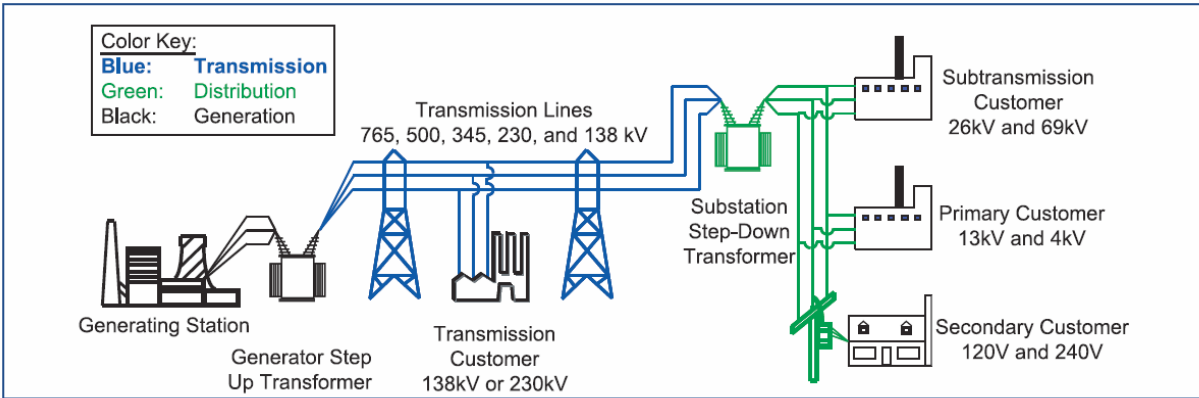


Fig. 1-2. A simplified illustration of transmission and distribution grids in US [2].

Table 1-1. Losses of transmission and distribution grids in US.

Transformer types	Power loss
Step-up transformer	1-2%
Transmission lines	2-4%
Step down transformer	1-2%
Distribution network transformers and cables	4-6%

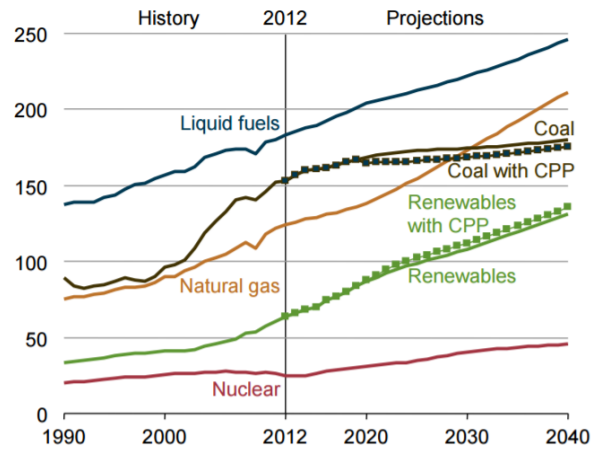


Fig. 1-3. Total world energy consumption (1990–2040) in quadrillion (10^{15}) Btu [4].

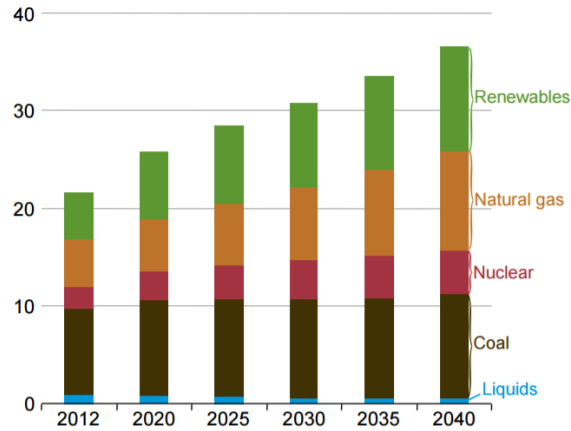


Fig. 1-4. World electricity generation by energy source (2012-2040) in trillion kilowatt-hours [4].

- 1) Further increase the line voltage of high voltage ac line (HVAC). For example, as voltage gets doubled, for a given power, line current loss will drop by 3/4. On the other hand, since active power is proportional to voltage square, line power capacity can be increased by 4 times if the same line loss is maintained. Currently, the world highest HVAC line in commission has been to 1000 kV in China. However, building a line may be prohibitive due to the new right-of-way, line towers, high voltage insulators, high voltage cables, etc.
- 2) Reduce the line impedance by using flexible ac transmission system (FACTS) devices [6], such as thyristor-controlled series compensator (TCSC), distributed static series compensator (DSSC), and unified power flow controller (UPFC) [7-10]. These power converters-based devices can insert an inductive voltage lagging line current flow by 90 degrees to behave as a negative inductance. However, high voltage insulation cost, high voltage device cost, and availability, and system reliability concern have hindered the large-scale applications of these devices in the market.
- 3) Convert and transfer the power on high voltage direct current lines (HVDC). Different from HVAC whose active power transmission is highly dependent on line impedance and influenced by grid frequency characteristics, dc power flow does not involve frequency

related effects and does not generate reactive power, thus can stably provide high power up to the line thermal limit and insulation limit. Moreover, when considering both the hardware cost and line cost, HVDC is also more economical for the overhead line when the length is above 500-600 km, as shown in Fig. 1-5. And for the submarine line, this critical length can be as short as 50 km because of expensive ac underground cable [11, 12]. ABB and Siemens have built many HVDC lines worldwide, and more than ten commercial ultra-high voltage direct current (UHVDC) projects are now commissioning or constructing in China, using UHVDC cables up to ± 1100 kV with the highest one having transmission capacity of 12 GW over 3324 km at ± 1100 kV [13, 14].

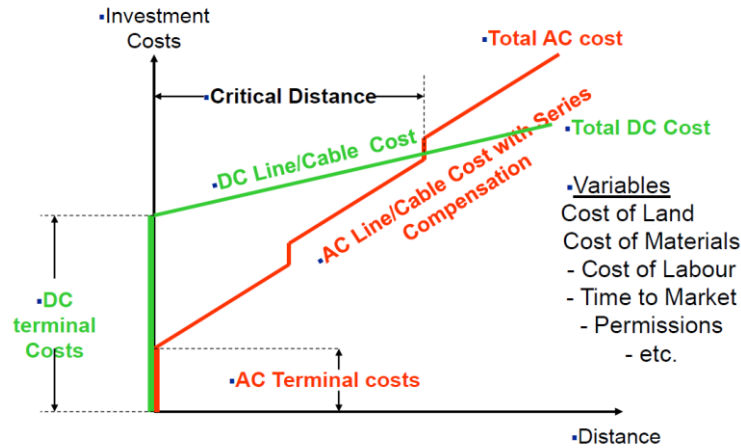


Fig. 1-5. Cost comparison of HVAC and HVDC [12].

1.1.2 Transmission line emulation

With the rising complexity in multi-nodes grid structures, multi-level control algorithms, various types of infrastructure, it is almost impossible to conduct the grid field test directly when any new control or hardware is trying to be applied to the grid system, considering both the time-consuming test procedure, and the cost and risk in unpredictable experimental field trial. Software simulation and/or hardware emulation are preferred as the first step before the actual field test.

In the early days, the down-scaled grid system was the main approach to emulate the complex grid due to multi-tie lines and time-varying and nonlinear components. In the 1920s, a miniature 400 V, 3.75 kVA ac grid consisting of down-scaled lumped transmission lines with tap adjustable resistor, inductor and capacitors arrays, low power artificial generators and loads were built by GE to investigate the ac grid power flow [15], and later a larger scale 2380 V, 200-625 kVA artificial transmission system was also built and tested to study stability and power limitation [16]. This testbed approach is still used today in different types of modern grids [17]. However, most of these testing components are not generic and configurable. Therefore, to study different power systems or even just different operation scenarios of a given system is time-consuming and costly.

With the advancement of the computer technology and digital processing, software simulation becomes the main trend of studying power system by analytically and/or numerically modeling grid components and control interface. However, owing to the complexity of components' mathematical models and their time-varying or frequency dependent nonlinearities, compromises have been made between the computation speed/resources and different levels of model accuracy and details. Different types of digital simulation tools have been developed. As listed in Table 1-2 [17], in applications of large-scale power systems with hundreds or thousands of buses and of high-level control study, where only slow electromechanical behaviors are concerned, Power System Simulation for Engineering (PSS/E) and Transient Security Assessment Tool (TSAT) are more often used, implemented with integration time step at the second level.

The electromagnetic transient program (EMTP) based simulation tools such as PSCAD/EMTDS and ATP, on the other hand, are more suitable for detailed model simulation representing their high frequency and nonlinear behaviors, thus with millisecond-level integration

step [17]. Matlab/Simulink is a generic tool to simulate smaller scale power systems and electronic circuits in different time scales. For detailed semiconductor device level simulations, Saber with varying time step and integration of netlist-based languages and hardware description languages is often the first choice.

Table 1-2. Power system and electronics simulation software [17].

Name	Time Step	Integration Method	Application
PSS/E	Fixed	Explicit Trapezoidal	Electromechanical
TSAT	Fixed	Variable	
Matlab/Simulink	Variable/Fixed	Variable	Generic
ATP, PSCAD/EMTDC, EMTP-RV (EMTP Based)	Fixed	Implicit Trapezoidal	Electromagnetic
SABER	Variable/Fixed	Variable/Fixed	Semiconductor Devices Modeling

In the 2000s, another type of simulation, hardware-in-loop (HIL) technology, as a hybrid of both digital simulations and the physical test was developed [18, 19]. It was primarily used to test the digital controller for a physical device or power converter in the design early phase by interfacing the physical controller with the simulated power converter inside the tool, thus preventing the potential hazards onto the expensive power converters due to the possible controller defects, and greatly facilitating the product development with low risk and cost, and often named as model/simulation/control HIL [20-22]. Soon, this concept was extended to study a specific power device under test (DUT) with all remaining controllers and power components of the system simulated digitally in the software and connected with the DUT through power amplifiers as the interface [23], illustrated in Fig. 1-6. The power converter-based power amplifiers link the simulated power signal from the software side with the actual power signal from the DUT side through bidirectional interface structures, thus enabling the bidirectional power flow and power level hardware-in-the-loop (PHIL) testing of a DUT. Many applications have been based on HIL

approaches such as in automotive systems, robotics, power electronics, etc. Several commercial PHIL platforms such as Real Time Digital Simulator (RTDS) from Typhoon RTDS and OPA-RT's real-time simulators [24] have been widely used in power system study and electrical equipment testing. Since they are based on expensive paralleled computation architectures using dedicated FPGAs and/or CPUs and provide proprietary component models and interface algorithms, thus are often costly [25].

Although PHIL provides a mimic system network for function verification of power electronic converters in grid applications, it has several inherent limitations. First, as described before, PHIL can only simulate a specific DUT. Its counterpart, i.e. the remainder of the system, must be virtually simulated in software. Second, the digital simulation itself is fully dependent on the numerical computation, thus is prone to suffering numerical instability and oscillation due to numerical truncation errors or interpolation with improper integration methods or discrete time steps [26]. Third, some physical non-linearity characteristics as well as field interaction like electromagnetic filed interference among electrical components are difficult to be modeled in PHIL tools and are currently only achievable from complicated 3D simulation engines such as ANSYS. A comprehensive PHIL simulation platform is not available yet and expected to be extremely costly. In addition, even if the mathematical models itself are accurate, some practical yet critical operating conditions such as communication delay and measurement error are often ignored or simplified by users.

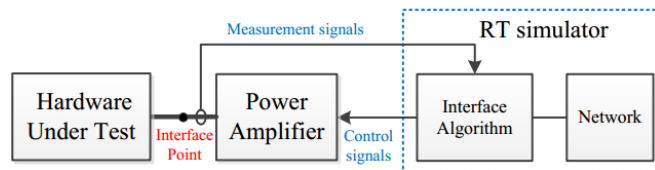


Fig. 1-6. Overall structure of power hardware in the loop [17].

In the end, the hybrid simulation cannot fully reflect the physical characteristic of the model and precise time-varying multi-factor dominant parameters, as well as the random device defect or failure. Thus, an emulation approach to bridge the gap between partial/fully simulation and actual field application, with physical models, reconfigurable functionalities, and flexible building block architecture is demanded.

An ultra-wide-area transmission network emulator, also called hardware test-bed (HTB), is being developed by CURENT center at University of Tennessee to emulate the large-scale interconnected power systems by using regenerative converters in a modular manner [1, 27-35], as shown in Fig. 1-7. Different from the above approaches, hardware emulation implements all the grid component models and controls in many down-scaled universal voltage source inverters, running the real power with suitable scaling to mimic the real grid system operation in a distributed and simultaneous parallel way. In general, each power converter is controlled by an independent digital controller (DSP) and communicated using CAN Bus, emulates a certain type of grid infrastructure such as a generator, load, wind farm etc., and joints with each other modularly. Field measurement units such as potential transformers (PTs), current transformers (CTs), frequency disturbance recorders (FDRs) and phasor measurement units (PMUs), are also installed in the emulation grid, and system level control implemented on NI LabVIEW platform serves as the grid control center [33], as shown in Fig. 1-8. With reconfigurable control modes and fast time response thanks to power electronic converters, HTB can function as a versatile platform to conduct various system studies, including measurements, monitoring, control, modeling and renewable penetration [1, 33]. Due to its hardware emulation nature, it provides more field information, demonstrates power system behaviors in different time scales, and can conveniently mimic actual communication and control hierarchy among different sub-area systems in real-time.

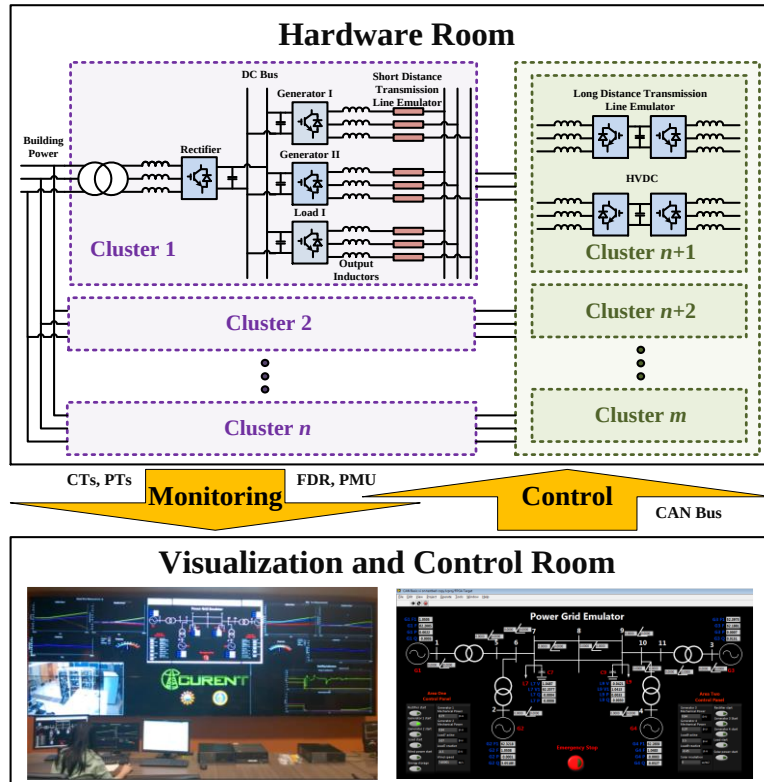


Fig. 1-7. VSI based hardware test bed [34].

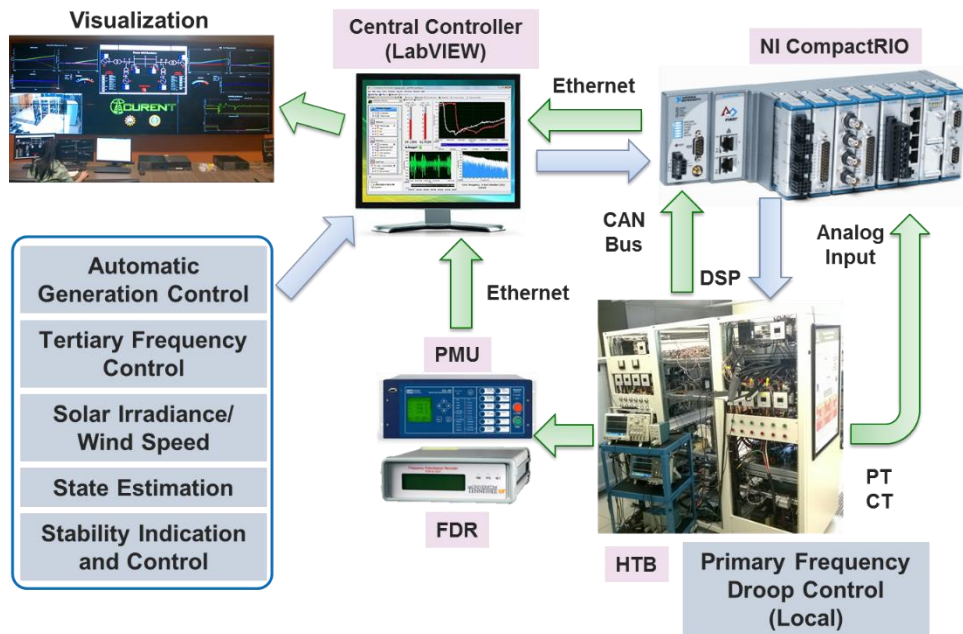


Fig. 1-8. Overall functions and components in a HTB system [33, 36].

Therefore, multi-converter based HTB grid emulation has become a promising approach in power system study and applications.

1.1.3 Special grid interface – aircraft power supply

Over the recent hundred years, technology on airplane design has gained tremendous progress. And the trend in the past decade has moved towards more electrical aircraft (MEA). Different from conventional aircraft driving by a mixture of mechanical, electrical, hydraulic, and pneumatic energy, the goal for MEA is to replace the bulky and costly nonelectric components such as hydraulic actuators driven by nonelectric power with more efficient pure electrical systems [37-40]. This also avoids the efficiency sacrifice from energy conversion and transmission, bringing various benefits in efficiency, weight, maintenance costs, reliability, and emissions. Some of the main changes are shown in Fig. 1-9.

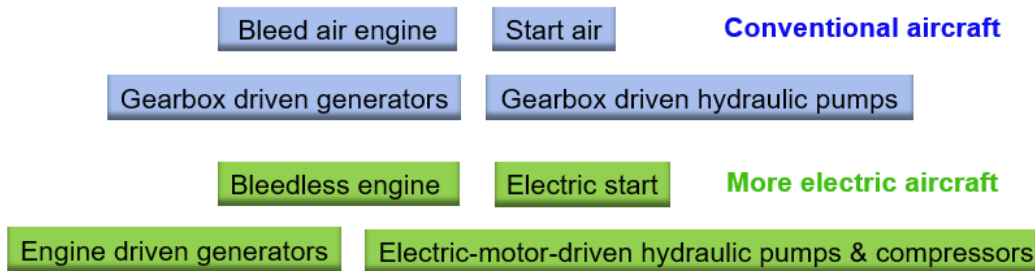


Fig. 1-9. Comparison of traditional and more electric aircraft.

Among them, a direct impact on electric power system onboard is the elimination of gearbox. Traditionally, electrical power in aircraft is generated by a synchronous generator through a variable ratio gearbox, also known as constant frequency integrated drive generator (IDG), to interface with the variable speed engine [40]. The resulting power at constant 115 Vac voltage and 400 Hz, are still very common today. Without the gearbox, the generator is directly coupled to the main engine, thus its frequency is proportional to the engine speed, leading to constant voltage variable frequency electrical power system (CVVF) [38].

Compared to the traditional aircraft grid designed at 115 Vac 400 Hz and 28 Vdc, the electrical power in MEA has multiple levels, as shown in Fig. 1-10 and Fig. 1-11. The ac voltage has two levels, 115 Vac or 230 Vac (In Boeing 787, it is 235 Vac). And ac frequency can vary from 350 Hz to 800 Hz, depending on different types of engines and aircraft. The ac grid can be used to drive the motor, electric pumps, and fans, while other loads such as lighting and avionic equipment are usually powered by dc. In addition, batteries can act as the generation source during preflight to start engine or APU, or as the backup for emergency conditions and are also connected with the dc bus. Both low voltage 28 V dc and high voltage ± 270 V dc are used in MAE, where ± 270 V is mainly due to the concern of air partial discharge at high electric field.

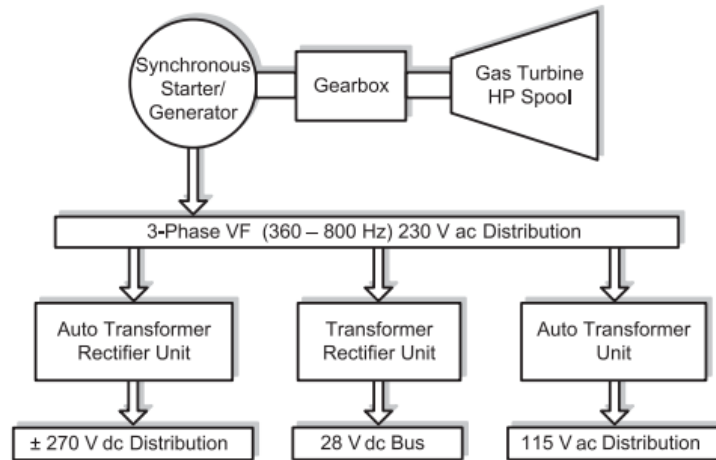


Fig. 1-10. System configuration with synchronous generator based ac generation in aircraft power system [38].

Traditionally, the 28 Vdc is converted from ac through transformer based diode rectifier unit (RTU), and 270 V bus is obtained from autotransformer rectifier unit (ATRU) such as 18-pulse phase shifted diode rectifier [41, 42]. With the advancement of power electronic devices, different types of active rectifiers are proposed in aircraft applications, A low current harmonic distortion typically less than 5% can be easily achieved with pulse width modulation and higher switching frequency, and the bulky magnetic components in ATRU can be significantly reduced [43].

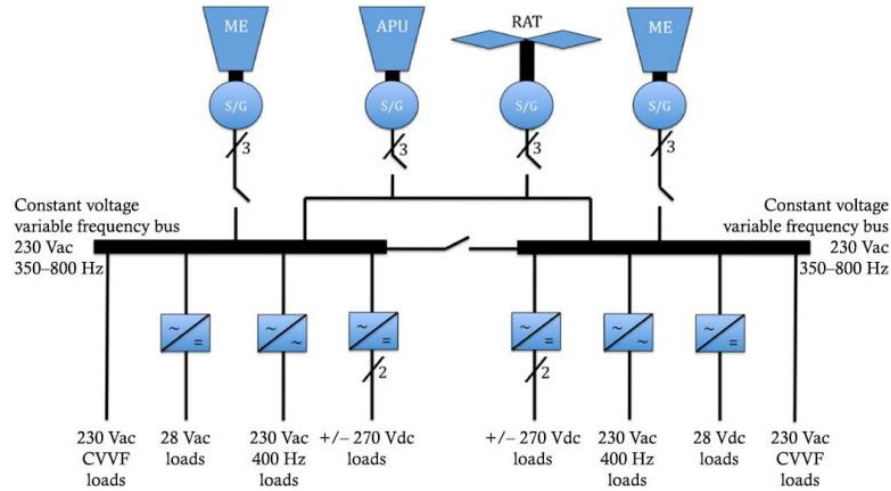


Fig. 1-11. Ac voltage levels and dc voltage levels in MEA systems [40].

As large aircraft is developing towards MEA, more electric supply are demands are required, and the electric power rating keeps increasing, as shown in Fig. 1-12, such as the Boeing 787 with 4*250 kVA generator power rating compared to Airbus 380 with 600 kVA shown in Table 1-3 [40]. And various avionics equipment and actuators are relying on power electronic converters, as discussed in [44]. Thus, the total power dissipation and the weight of the electric power converters present a significant impact on the performance and cost of whole MAE aircraft. This imposes a higher requirement on the conversion efficiency of power electronic converters and their power density.

In addition, in aircraft systems, the radio-frequency interference (RFI) and electromagnetic interference (EMI) in a broad sense from the external lighting or nearby electronics, are harmful for normal operation of aerospace equipment and radar signals, which can lead to various negative consequences and even safety issues and incidents [46-48]. Regulation and mitigation of EMI have been virtually considered in all aspects of avionics design. With more electrical power converters in MAE, EMI issues may become more severe, drawing a research premium on it.

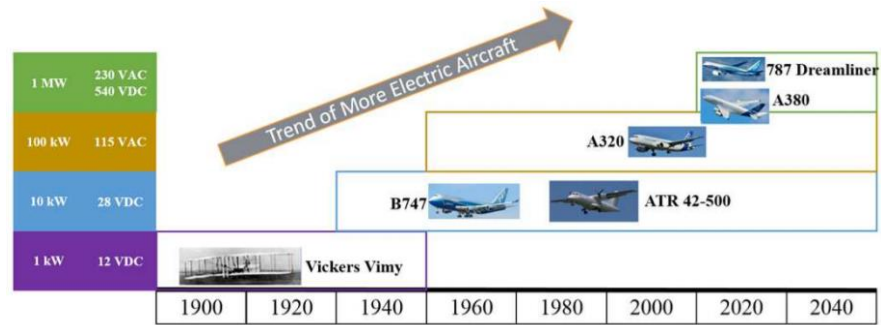


Fig. 1-12. The evolution of MEA history [45].

Table 1-3. Comparison of key electrical systems in several aircraft [40].

Aircraft	Boeing 787	Airbus 380	Airbus 350
No. engines	2	4	2
No. generator per engine	2	1	2
Gen. rating per engine	250 kVA	150 kVA	100 kVA
Gen. output voltage	235 V	115 V	230 V
No. gen. per APU	2	1	1
Gen. rating per APU	225 kVA	120 kVA	150 kVA
RAT rating	Unavailable	150 kVA	100 KVA
ECS method	Electric 4*100 kW compressors	Bleed air	Bleed air
Brake system	Electric	Hydraulic	Hydraulic
Actuation system	EHA	Conventional and EHA	Conventional and EHA

To address these demands, several design aspects from topology, device, filter design, power quality control including ac current distortion, dc bus voltage regulation, and electromagnetic noise emission, to controller design and cooling design, will be reviewed in this work. The challenge and possible approaches for improvement will be studied in this work and presented as the main body of this report.

1.2 Research challenges and motivation

Based on the literature survey, there are many uncertainties and unsolved issues in converter interface with different types of grids, for development of the cost-effective power electronic solutions to enhance power transfer capacity, development of the noise immunized, accurate and stable power transmission line emulator, and development of the high power-quality low noise-emission GaN device based high-density aircraft charger.

For hybrid ac/dc power transmission, the main challenges are:

- 1) The power capacity enhancement is a function of dc current and voltage mixture, but their relationship is not fully established.
- 2) The technical feasibility of injecting dc onto ac lines is not explored under abnormal conditions including line faults and line unbalances. A high percentage of dc current and voltage injection is also not experimentally implemented.
- 3) Saturation issue of the interface transformer between ac and dc with line unbalances is never considered and experimental verification should be conducted.
- 4) The cost-effectiveness of transferring power compared with pure HVAC and pure DC conversion solutions are not investigated.

For transmission line emulator, the main challenges are:

- 1) Feasibility of emulating transmission line using power converters and the extension capability of an emulation model to represent line characteristics of different level complexities.
- 2) Sensing and sampling noise may deteriorate the emulation accuracy especially in a PWM voltage interfaced emulation grid with many power converters.
- 3) Interaction of the transmission line emulation system and its interfaced grid impedance may cause a stability issue. A criterion to determine the stability, thus to define the impedance boundary of the line emulation should be explored.

For aircraft charger design, the main challenges are:

- 1) Topology evaluation to find a low weight, high efficiency solution that can fit the wide input voltage, dual output voltage, and GaN device based universal battery charger.
- 2) Impacts of high switching frequency, high di/dt , dv/dt on power quality control have not been clearly understood, and solutions to mitigate these impacts should also be explored.
- 3) Modeling of distortion due to device junction capacitances in three-level converters is desired to guide converter parameter selection and device selection, especially in high switching frequency converter design. Distortion mitigation is also demanded.
- 4) Fundamental knowledge on performance degradation of EMI passive filter especially in the multi-component structure is not well established. The impacts and mechanisms of both inductive and capacitive coupling on different filter structures should be better understood. Simpler modeling, prediction, and debugging of filter attenuation considering frequency dependence and parasitic coupling are desired and should be very helpful for engineering practice. Mitigation solutions to reduce parasitic coupling, self-parasitics and better utilize EMI filter to approach the ideal performance are expected.

- 5) Control and modulation schemes to better utilize the soft-switching techniques for dc-dc stage and to reduce hardware complexity.
- 6) High speed digital controller design for a two-stage charger with wide inputs and dual outputs, multiple sampling variables and control loops, and high switching frequency.

1.3 Dissertation organization

This dissertation is organized as follows:

Chapter 2 reviews the activities in power topology, control, and component design in interfacing power converters to three different grids, including the high power transmission grid, the emulated transmission grid, and the aviation grid. Interface and interaction challenges and prior efforts are summarized.

Chapter 3 presents a hybrid ac/dc architecture in interfacing the ac and dc transmission grid. Possible dc injection devices are compared and associated saturation issues when considering the line unbalance condition are analyzed. Both passive and active mitigation approaches are proposed, modeled, designed and implemented. System-level benefits compared to other transmission architectures are also studied.

Chapter 4 proposes the general emulation models and schemes of voltage source inverter based transmission line emulator and analysis the impacts and mechanism of the dc sampling noise and switching frequency noise on interconnecting the line emulator to the emulated transmission grid. Active control methods are presented to mitigate these impacts. The emulation stabilities considering different interfacing impedances between the line emulator and the grid are also analyzed.

Chapter 5 compares the different ac-dc and dc-dc topologies that can transformer the power from aircraft ac source to dc battery, and a high power density three-level two-stage GaN based

charger is proposed and designed. This chapter presents a systematic study of interfacing issues introduced by high frequency, high di/dt , dv/dt when using high speed GaN devices in aviation grid for battery charger applications. It discloses the phenomena and mechanism of the dc bias sampling error and low frequency sensing distortion, and low frequency PWM voltage and ac current distortion, and presents mitigation approaches from sampling, sensing and PWM modulation aspects. In further, it analyzes an extra power loss in three-level converters associated with device parasitics and switching transient and proposes a loss evaluation method. Finally, high-performance controller and control algorithm, power circuit design, and device cooling for GaN based high density charger are also developed.

Chapter 6 comprehensively studies the disclosed capacitive coupling and its mechanism in EMI filter and other HF filter behaviors, presents a generic coupling model for both CM and DM filters, and provides new guidelines in choose suitable filter topologies for maximizing the filter performance in bridging the connection of the power converter and the power grid. With that, it further presents several filter design approaches in mitigating both the inductive and capacitance coupling effects and presents a general winding strategy and modeling of winding capacitances considering different winding schemes to mitigate the filter self-parasitics. Overall, these efforts ensure a high performance of the high-frequency high-density filter and a low noise emission into the ac grid. Finally, a methodology that can characterize the filter attenuation and predict its insertion loss in a converter system is proposed and verified through actual power test.

Chapter 7 concludes the contributions presented in this dissertation and discusses the future work.

2 Literature Review

2.1 High-power transmission grid

2.1.1 Comparison of HVDC technologies

In the past half century, HVDC has undergone several main technology advancements, i.e. mercury-arc valves based line commutated converter (early LCC HVDC), thyristor-based line commutated current source converter (LCC or classic HVDC), two-level series connected IGBT based voltage source converter (VSC or HVDC light), multi-level modular voltage source converter (MMC, or HVDC plus). The size of HVDC converter has been reduced, and conversion efficiency of HVDC plus is also improved to 99% , approaching to that of classic HVDC, as shown in Fig. 2-1 [49]. However, three of the main challenges are still hindering the further wide applications of HVDC plus, i.e. cost, power rating and dc fault current blocking capability. According to [50], the cost of VSC HVDC converter station was 0.11 Euro /VA in 2003, while the cost for LLC HVDC converter station was about 0.08 Euro /VA in 2003. As seen in Fig. 2-2, HVDC light still has a relatively low power rating. Due to the absence of current zero crossing and consequent arc during the breaking instant as well as the low resistance in dc lines, dc breaking is difficulty and the swiftly increased high dc fault current also requiring dc breakers with fast response time. The state-of-art dc breaker solution is through solid state high power semiconductor devices. However, the cost and loss are pretty high due to the high conduction voltage drop and cost of high voltage IGBTs. ABB promoted hybrid dc breaker in 2012 with paralleling fast disconnectors to reduce the loss, still maintaining 5 ms or 2 ms fault breaking time [51-53], but its application is still limited due to high semiconductor cost and fast mechanical disconnectors. The other solution is to embed fault current limiting function into HVDC converters, such as full-bridge (FB) modular multilevel converter (MMC) and its variants [54]. FB MMC surpasses half-bridge

(HB) modular MMC in terms of dc fault blocking capability, however, it is seldom used in real applications due to the doubled device components and cost, and 2.35 times semiconductor conduction losses as well as the cost of losses if compared to the combination of HB MMC and dc breaker [55, 56].

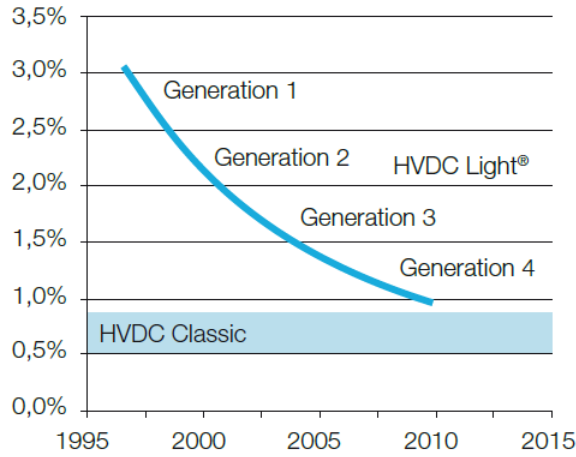


Fig. 2-1. Power loss reduction in the recent two decades [49].

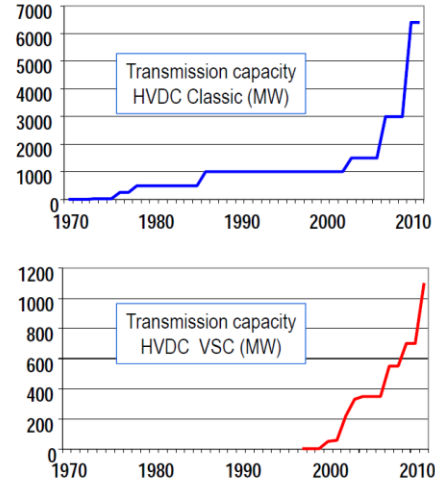


Fig. 2-2. Power rating evolution of HVDC classic and VSC [57].

2.1.2 Hybrid ac/dc

Although HVDC transmission is effective and efficient in transmitting bulk power over long distance, high investments, right-of-way cost, environment and policy constraints have hindered the pace to build new transmission lines in many countries [58-60]. This renders the efficient utilization of existing grid assets being a more urgent topic. To release the transmission limitation and congestion constrained by the existing ac grid infrastructure [58, 61], the old grid needs to be modernized.

For conventional high voltage ac (HVAC) long line transmission, the line current rating is usually far below its thermal ampacity and the line power transfer capability is determined by stability constraints instead of thermal constraints [61, 62], which leads to low power angle and

limited power transfer capability. As an alternative to new lines, the concept of hybrid ac/dc transmission was proposed [60, 63-65]. The basic idea is to load ac lines close to their thermal limits by superposing dc current onto the ac current through a dc injection device, utilizing the existing ac lines, towers, facilities and avoiding the need for new right-of-way.

One implementation scheme for the hybrid ac/dc concept is shown in Fig. 2-3. An ac double circuit is selected to form a bipolar HVDC circuit with 12-pulse line-commutated-converters (LCC). The dc injection link is indispensable for the hybrid ac/dc scheme. A zigzag transformer approach has been proposed [63, 65], which allows dc current injected through its neutral point. With equal turns of windings but opposite polarity on each phase, dc flux could be totally canceled theoretically, as long as the dc current in the three phases is evenly distributed. The voltage insulation is also considered in [66], pointing out the line insulation from line-to-ground issue once dc voltage is superposed. To avoid replacing or increasing the discs for tower insulation strings along the line, ac voltage is reduced to maintain the same peak voltage stress. To be noted, the line-to-line insulation stress is not affected by dc superposition thus no change is required for conductor clearance distance. The current ratio of dc over ac are recommended to be 1 to keep current zero crossing available, while voltage ratio is selected to be lower than 1 so that actual voltage changes its polarity twice in a cycle and may avoid the need for higher creepage distance which is required in HVDC lines [63]. However, no comprehensive quantification was conducted among different ratios, cost and capacity to provide a cost-effective design.

The focus of prior work is on the concept verification under ideal conditions as well as its feasibility in improving power system stability with fast dc power control during power swing. Little investigation is done to evaluate which topology among LCC and VSC HVDC variants is more feasible in hybrid transmission applications, considering abnormal conditions. Moreover, no

design methodology has been studied on zigzag transformers which operate as dc injection links, especially when equivalent impedances of the three lines are not exactly the same. Since dc current will not be evenly distributed under such unbalanced conditions, dc flux flowing into three phases cannot be canceled, leading to a potential magnetic saturation of the zigzag transformer and eventually a failure of the scheme.

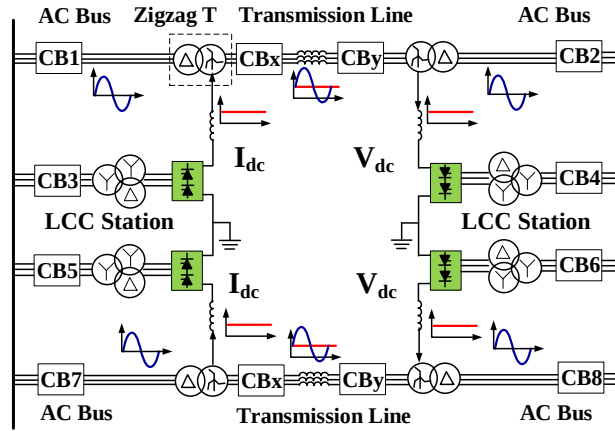


Fig. 2-3. Architecture of the hybrid ac/dc transmission system [67].

2.1.3 Upgrading HVAC to pure HVDC

In addition to the hybrid ac/dc transmission system, there is another transmission architecture, which upgrades the existing HVAC line into a pure DC line. This pure HVDC solution was intensively studied. In this case, two end HVDC converters need to take full power, but the interface between ac and dc through zigzag transformers is not required. This pure HVDC solution was intensively studied by Cigre, STRI, EPRI, and ABB [68-74].

Ref [73] investigated three types of dc conversion: 1) conversion from single circuit lines to pure dc lines; 2) conversion from two-circuit tower lines to partial ac partial dc line, forming another type of hybrid ac/dc transmission; 3) conversion from double circuit lines to pure dc lines.

Different options of line configuration and dc polarity setting are possible because the sustainable dc voltage is related to the conductor size and circuit configuration.

Different current modulations to convert ac line to dc line were also studied. In addition to the conventional bipolar operation of HVDC converters, ref [69, 73] proposed the tripolar bridge configuration to fully utilize the double circuit lines, by intermittently pushing the two outmost conductors overloading for several minutes and alternating them in turn, to maintain the average power loading within thermal limits, as given in Fig. 2-4. Another VSC HVDC modulated dc conversion scheme was also proposed using a bipolar configuration with the help of thyristors on the receiving end to switch the current direction of the middle pole conductor [75], shown in Fig. 2-5.

Although dc current can be pushed to thermal limits, the dc voltage determination is very complicated. Four limiting factors have been considered in [73], including conductor surface gradient, earth surface gradient, insulation creepage length, mid-span electrical clearance from conductor or tower to the ground. It is said that ceramic based ac insulators have much lower pollution flashover strength to support normal operating dc voltage than the case under ac voltage, due to the electrostatic precipitator effect of constant dc field which attracts dirt particles from the ambient air onto insulator surface [71]. Therefore, ac insulators should be replaced with composite suspension types in dc conversion [71]. In addition, excessive voltage gradient at the conductor surface will cause corona, leading to audible noise and radio interference, which is higher in the dc case, especially in fair weather [71]. Although it shows that this is not the main limiting factor, these environmental effects should be fully considered [73]. Such effects in a single circuit horizontal configuration is provided in Fig. 2-6.

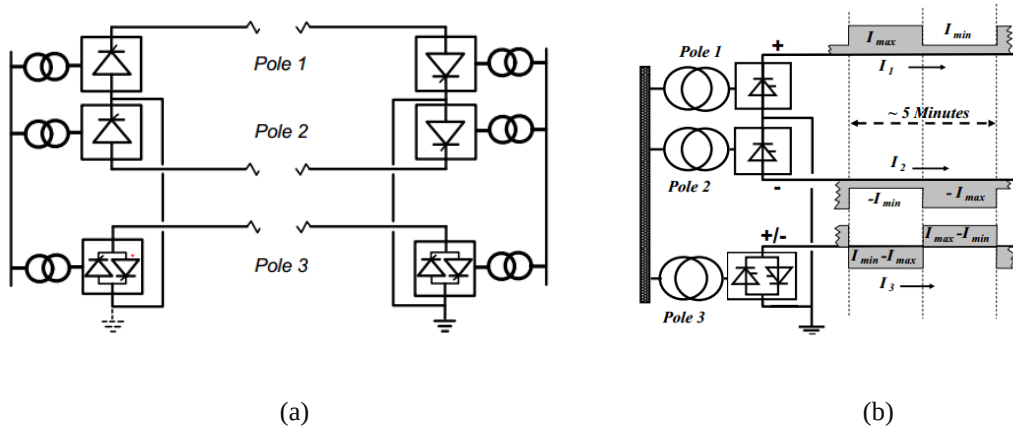


Fig. 2-4. Converting ac lines to dc line option 1. (a) tripolar LCC-HVDC tripolar configuration. (b) dc current modulation via a bipolar and a monopole structure with bidirectional valves. [69, 73]

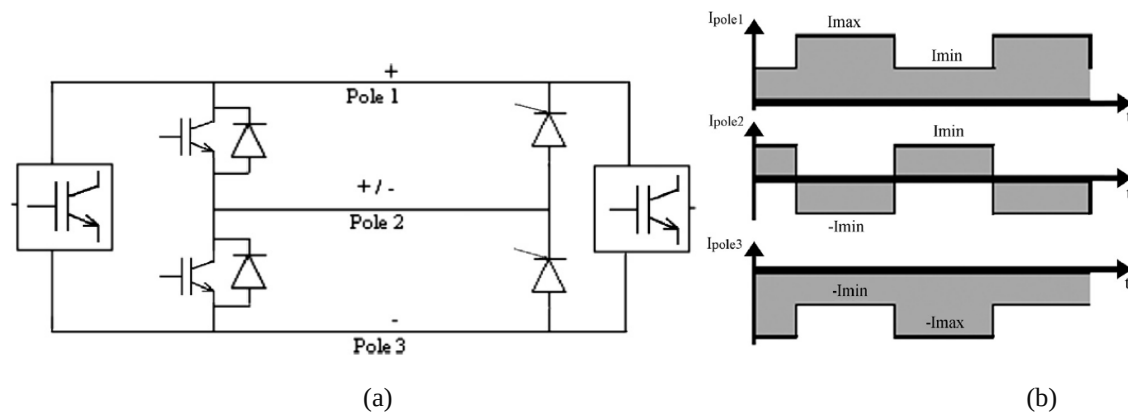


Fig. 2-5. Converting ac lines to dc line option 2. (a) VSC-HVDC tripolar configuration. (b) dc current modulation scheme [75].

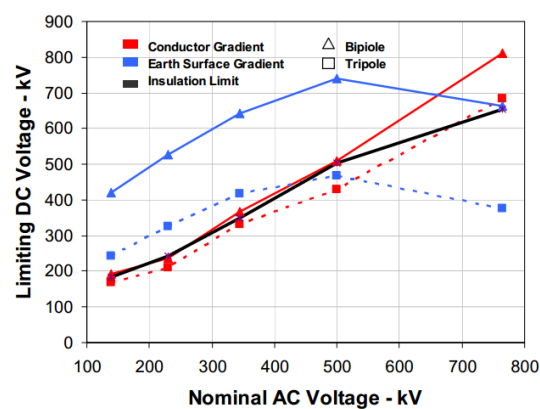


Fig. 2-6. Allowable dc voltage on ac lines as a function of three limiting factors [73].

Under a given power capacity, this pure dc scheme may be more expensive than the hybrid scheme, considering its full converter rating and possible insulation strings replacement due to dc corona and field effects. But it can achieve higher power capacity for given lines.

2.2 Transmission line emulator

As listed in Fig. 2-7, different types of grid components have been developed in the HTB platform, including basic components such as generator emulator [76], passive load emulator and induction motors [31, 77], and components for high renewable penetration study such as wind turbine emulators [30], solar PV emulator [78], energy storage emulator [79], battery emulator [80], RTDS interfaced grid emulator [81], and HVDC emulator [82]. Different short circuit fault emulators are also developed [29, 83].

Among all the above emulators, ac transmission line emulator is a vital and special element, since it functions as a bridge to interconnect two ac systems and fulfill the overall grid emulation task. As a backbone of the interconnected ac system, the ac transmission line emulator becomes one of the key components in HTB. The other uniqueness lies in that most of the other emulators only interface with the grid in one point and thus can be implemented within one VSI, however, line emulator has to interface with other grid components physically in both terminals, requiring at least two VSIs operating collaboratively to perform the correct line behavior emulation. This imposes challenges in converter interfacing, emulation scheme selection, emulation accuracy, control and stability of line emulation.

2.2.1 Interface algorithm

In any simulation or emulation system, interface algorithm (IA) between the target component and its surroundings is important. In PHIL systems, the most common IA is ideal transformer model (ITM) [84-89], which as shown in Fig. 2-8, breaks the connection point to the primary and secondary side of an ideal transformer. Two types of ITM can be configured: voltage type and current type. In Fig. 2-8 (a), the voltage type ITM senses the current information at the hardware side and use it to control a current source at PHIL simulator side, then the resulting voltage across the current source is utilized to control the voltage source at the hardware side. In Fig. 2-8 (b), the current type ITM uses the voltage as the input and gives the current as the output.

Because of its simplicity and lossless, ITM based IA is also widely used in offline simulation software such as Matlab. However, different from pure offline software simulation where no delay and data loss are introduced in transferring and sharing the interface information, the power amplifier as the embodiment of IA, inevitably suffer its device nonlinearity. These non-ideal factors could come from converter modulation error, power amplifier control delay, converter output regulation error, digital quantification error and conversion delay of analog-to-digital converters (ADC) and digital-to-analog converters (DAC), and high frequency noise and offset of sensing circuit. Generally, noise and offset can be filtered or suppressed by refining the circuitry, regulation tracking error can be reduced by enhancing power amplifier control gain or compensation, control delay can be reduced by increasing switching frequency and controller bandwidth, and sensing error and delay can be shrunk by adopting high speed high bit ADC and DAC. However, delay time reduction is achieved at the expense of high cost of IA amplifiers and is often constrained by limited performance of available power devices and analog devices.

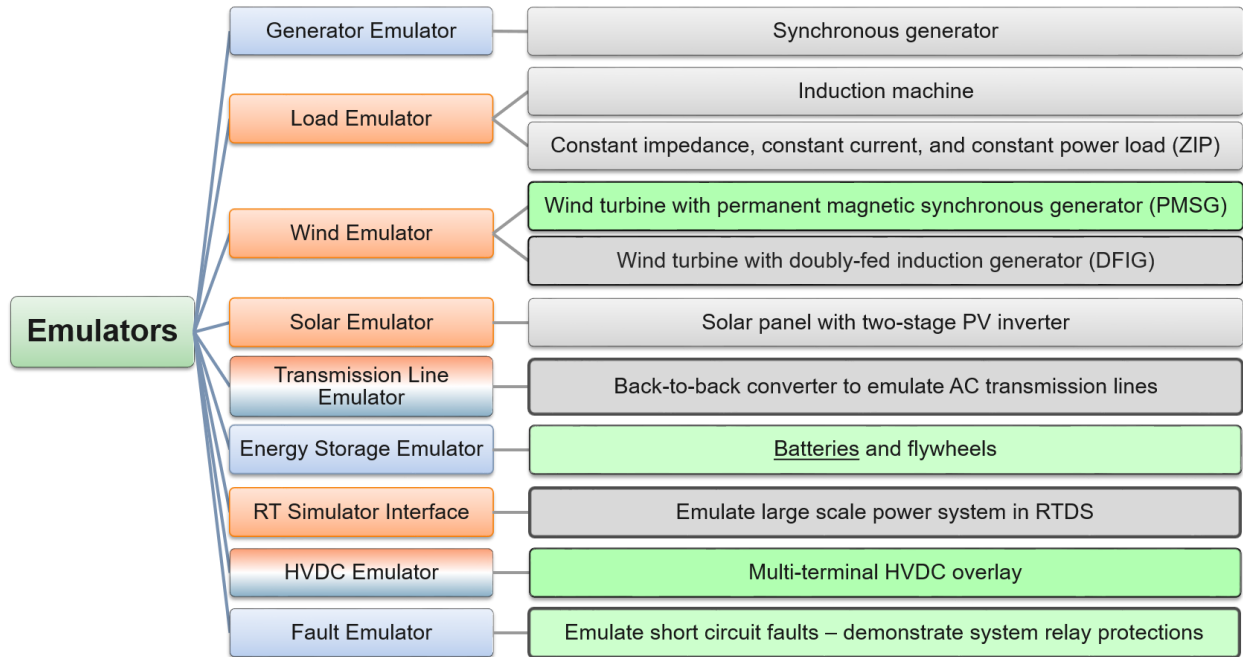


Fig. 2-7. Developed emulators in HTB based emulation grid [29-31, 76-83].

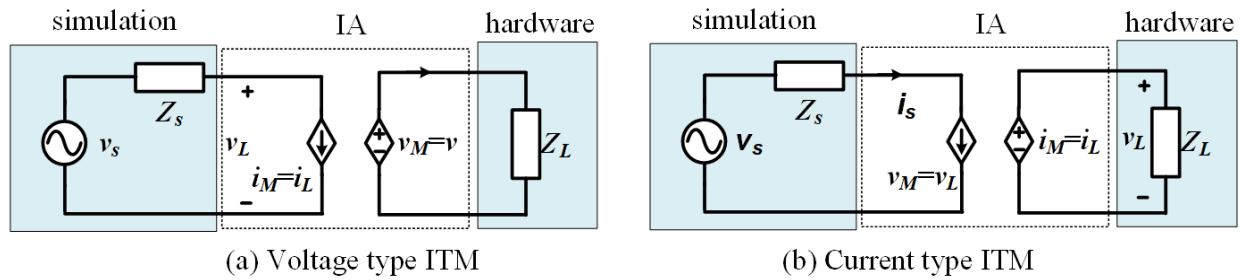


Fig. 2-8. Two types of ITM based interface algorithm in PHIL [34, 90].

These nonidealities could introduce steady state errors and cause stability problems, especially with the help of time delay [90]. In fact, IA is strongly coupled with stability. The relationship between stability and interface algorithm in PHIL simulation system has been thoroughly investigated in [90]. It is found that when TIM is used for a voltage divider circuit as shown in Fig. 2-10, PHIL system stability is determined by the ratio of simulated source impedance and external load impedance with the help of time delay as given in (2-1). In an intuitive explanation, this ratio acts as a voltage error amplification coefficient and amplifies the error from the interface amplifier step by step. This stability criterion is very similar to the well-known Middle Brook stability criterion in cascaded power converter systems derived from the Thevenin equivalent circuit.

Several improved IAs have also been proposed to reduce the impact in PHIL, such as partial circuit duplication method (PCD) [91], damping impedance method (DIM) [90], transmission line model (TLM) [92, 93], and time-variant first-order approximation (TFA) [94]. Most of these IAs derive from widely adopted largescale circuit simulation algorithms in commercial simulation tools such as companion resistive network and relaxation technique [95, 96]. However, when they are applied in PHIL, the main advantages of collecting and solving the large companion resistive network of all circuit components implicitly in simulation tools or relaxing circuit component constraint to reach desired error through multi-step iterations, do not hold anymore. Because in real time PHIL, the external hardware impedance is unknown, therefore, these IAs have to either insert physical impedance or modify the original impedance or estimate the load. Thus, compromise among simulation accuracy, stability, flexibility, and applicability has to be made.

Although no work has been done to emulate the transmission line, these basic principles in PHIL and pure simulation can be applied. In fact, the situation for IA selection is even more

complicated in converter based line emulation, since both ends of the line emulator interface with other grid components.

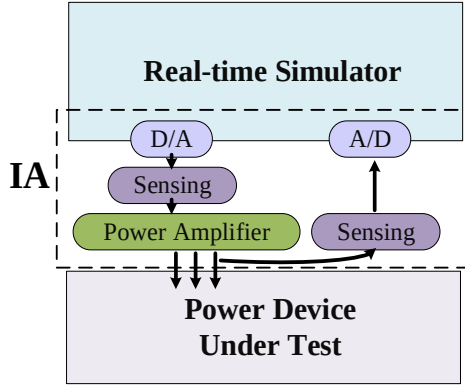


Fig. 2-9. Interface components in a HIL system.

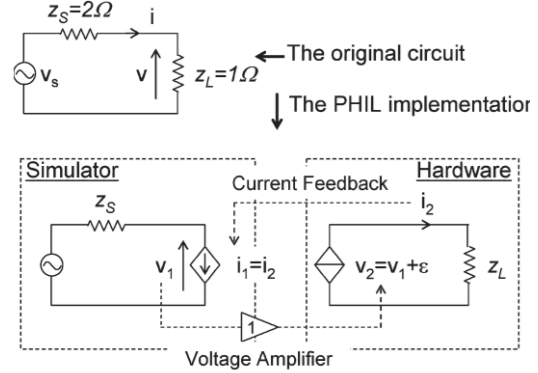


Fig. 2-10. Voltage divider circuit showing PHIL instability issues [90].

$$\frac{i_L}{V_s} = \frac{1}{1 + \frac{Z_s}{Z_L} e^{-s\Delta t}} \frac{1}{Z_L} e^{-s\Delta t} \quad (2-1)$$

Fortunately, the common ITM method is still very promising, mainly from the following observations:

The typical transient in ac power system as shown in Table. 2-1 [97], and most of the electromechanical phenomena, as often the main interest in system study, is usually below 100 Hz. Therefore, the IGBT based VSI line emulator operating at 10 kHz switching frequency can achieve the current and voltage control bandwidth up to 1 kHz. With proper VSI controller design, time delay and phase lag can be compensated within the control bandwidth [98], especially at the low frequency range of interest.

With proper sensing and sampling method in digital controller design, sensing and sampling error can be reduced, as well as conversion delay. In addition, the discretization method also plays

a key role in steady state error and stability. By selecting the proper discrete implementation of the emulation model, its stability and accuracy could also be potentially improved.

Table. 2-1 Classification of power system transients [98].

Mode	Frequency (Hz)	Event
Electromechanical Phenomena	0.001	Load frequency control
	0.01	
	0.1	
	1	Transient stability stabilizer
	10	
	10^2	Short-circuits, Sub-synchronous resonance, Harmonics, Power conversion phenomena
Electromagnetic Phenomena	10^3	Switching transients
	10^4	
	10^5	
	10^6	Traveling wave phenomena
	10^7	Transient recovery voltage

2.2.2 Stability of line emulation

Emulation stability is tightly coupled with the interface algorithms and external impedance, as already discussed in the above section. Different from other emulators, since a line emulator itself is to model an impedance, therefore, its allowable emulation range directly couples with its stability range. A guideline on its stability will help to define its working boundary and further help to extend the emulation capability and stability, therefore, is demanded.

Emulation stability is also fundamentally determined by the converter stability itself, which acts as the physical layer carrier of the emulator and is largely dependent on the controller parameter design. In a multi-converter based HTB system, the situation is similar to that in the paralleled inverter systems. The classic way to analyze this stability problem is through Nyquist Theorem in an equivalent impedance network where all inverters together their controllers are linearized to small signal models to obtain their Thevenin's or Norton's equivalences, either in a

basic structure of a voltage-controlled source in series with its output impedance interfacing a current-controlled source plus its parallel input impedance, or in a structure of current-controlled source in parallel to its output impedance interfacing with a voltage-controlled source in series with its input impedance [99-101]. Interaction of inverters is found to be strongly impacted by controller parameters, which essentially reshape the input and output impedance at the source side and load side, respectively. The interaction is severer in interfacing weak grids with non-negligible line stray impedance since the point of common coupling (PCC) voltage becomes dependent on each inverter's output impedance, and PLL and forward controller as the direct interface with PCC voltage are found sensitive in influencing inverters' interaction and stability [31, 102, 103]. Following this impedance principle, the stability of two synchronous generator emulators in HTB two area grid system was extensively investigated in s-domain small signal model [34], and the conclusion is that controllers of a voltage type emulator inverter have to help decrease emulator's output impedance to reduce interaction between each other, and PI controller together with current feed-forward is beneficial than a single integral controller. Recently, other stability analysis approaches such as passivity theory are also utilized in multi-inverter microgrid study [104-106], and improved methods are also applied to the HTB emulation system [107, 108]. These research works lay the basis for developing a stabilized inverter control for the transmission line emulator when it is inserting in multi-inverter based HTB system, however, the stability issue and interaction phenomena at the emulation level has not been well explored.

Previous emulation work mainly focused on the s domain analysis, considering the impact in the continuous domain from the controller, filter, PLL, and converter PWM delay [34, 90, 103]. In addition to these stability concerns, emulation accuracy and stability is greatly impacted by the digital implementation, discretization method and communication delay [31, 109]. To accurately

predict the stability of an emulation system, analysis in the discrete domain is preferred. In general simulation, less time step results in higher accuracy but at the expense of computation resources. As for the discretization method, backward-Euler discretization method is less accurate than the trapezoidal method due to higher truncation errors, but the choice of discretization method still depends on the waveforms types [109]. Backward-Euler has the advantage of representing piecewise linear waveforms, while the trapezoidal method is better for sinusoidal waveforms.

In addition, advanced integration methods using high order interpolating functions [31, 110, 111] or iterative algorithms can offer enhanced numerical stability but at the cost of increased computation time. This is more suitable for offline software such as Saber and Matlab/Simulink instead of real-time simulator or PHIL. However, when high frequency transient is concerned, such as in induction motor emulation [31], this type of methods such as third-order accurate Euler-trapezoidal based predictor-corrector method with twice correction [110, 111] was also adopted and showed higher transient accuracy, especially motor start-up [31].

2.2.3 Line model

As a backbone of the interconnected ac system, the ac transmission line emulator becomes one of the key components in HTB. To precisely emulate the power transfer of ac transmission lines, it is crucial to have an appropriate model and a dedicate control scheme with good dynamic performance and accuracy.

Theoretically, along the ac transmission line, its resistance, inductance, and capacitance are uniformly distributed as illustrated in Fig. 2-11. Distributed transmission line model [112]. Thus, it has infinite circuit states. Its distributed voltage and current along the line can be described in differential equations (2-2),

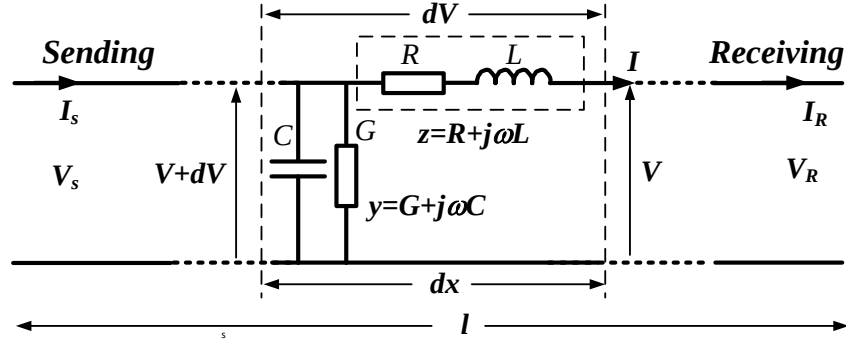


Fig. 2-11. Distributed transmission line model [112].

$$\begin{cases} \frac{\partial V(x,t)}{\partial x} = -RI(x,t) - L \frac{\partial I(x,t)}{\partial t} \\ \frac{\partial I(x,t)}{\partial x} = -GV(x,t) - C \frac{\partial V(x,t)}{\partial t} \end{cases} \quad (2-2)$$

From them, the general lossy line can be derived in (2-3), i.e. telegrapher's equations developed by Oliver Heaviside in the 1880s.

$$\begin{cases} \frac{\partial^2 V}{\partial t \partial x} = -R \frac{\partial I}{\partial t} - L \frac{\partial^2 I}{\partial t^2} \\ \frac{\partial^2 I}{\partial x^2} = -G \frac{\partial V}{\partial t} - C \frac{\partial^2 V}{\partial t \partial x} \end{cases} \quad (2-3)$$

And voltage and current any time t and any distance x from the sending end can be individually solved as (2-4),

$$\begin{cases} \frac{\partial^2 V}{\partial x^2} = LC \frac{\partial^2 V}{\partial t^2} + (RC + LG) \frac{\partial V}{\partial t} + RGV \\ \frac{\partial^2 I}{\partial x^2} = LC \frac{\partial^2 I}{\partial t^2} + (RC + LG) \frac{\partial I}{\partial t} + RGI \end{cases} \quad (2-4)$$

However, since the partial differential equation for both voltage and current are functions of time and distance, its analytical solution is difficult to be obtained, and not convenient for modeling. Two types of modeling approaches are widely used: distributed line model and lumped line model.

The distributed line model is primarily based on Bergeron's method also known as a method of characteristics which was originally applied to hydraulic problems in 1928 and later in wave surges in electricity [113]. In which, the traveling wave technique [114], developed since D'Alembert's solution [115], was used in solving Maxwell's equation mathematically for time-domain transient simulation [116]. In 1969, Dommel first applied this approach into the lossless transmission line in the development of EMTP [117], where term R and G are firstly neglected to satisfy the ideal wave equation, but later can also be compensated using lumped resistance to include the lossy line. This line model is called Bergeron's model, as given in Fig. 2-12.

In this model, electricity in terms of voltage and current is represented as an electric wave, with two key variables: the surge impedance or characteristics and the wave propagation speed. An exact solution can be obtained step by step with the method of characteristics by using the previous step history data. With that, the distributed line model can thus be represented by an equivalent two-terminal network seen from terminals. However, in this model, the history data which are stamped by the traveling time (the time current travels from one end of the line to the other) may not be snapshotted if the traveling time is not a multiple of the discrete time step (say the switching period of PWM converter in hardware emulation). Interpolation may be needed, and this adds the complexity of the emulation, not to mention other time delay introduced in the hardware implementation.

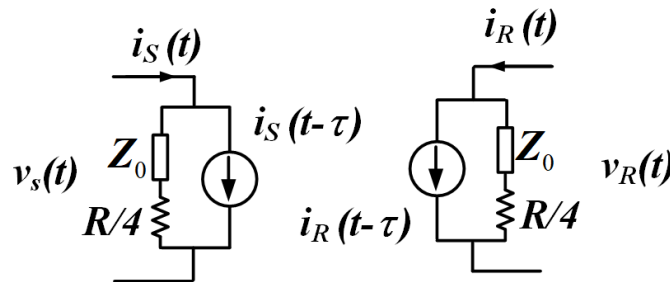


Fig. 2-12. The general Bergeron's model [122-124].

Since the advent of Bergeron's model, several EMTP type line models have been developed. The main feature different from Bergeron's model is that the frequency dependence of line parameters is incorporated into the model, to achieve higher accuracy. In addition, the lumped resistance at the end of the line is replaced by the distributed R across the line length. For these frequency-dependent models, all line parameter matrixes are first solved at many frequency points in the frequency domain with the detailed information of line and tower as inputs. Then their intrinsic response is easily obtained using curve fitting with a rational function approximation. And finally, the frequency domain (FD) solutions are converted to time domain based convolutions theory [118]. The Fourier transform and FD based approach are used in [119, 120], however, significantly increasing the computation effort. By introducing the recursive convolution technique in time domain convolution integrals [121], the computation efficiency is greatly reduced, eventually leading to two mature distributed line models used in PSCAD and EMTPDC [122-124]. However, compared to Bergeron's model with single frequency constant parameters, these models still require longer simulation time.

The distributed line models were primarily driven by investigating the damage induced by the light surge, switching surge, and transient fault current and voltage onto line, towers and breakers [113, 125], thus simulation tools with an accurate representation of high-frequency characteristics is pursued.

However, when the focus is on line's low frequency dynamics, such as line flow and power control transient, a lumped line model as shown in Fig. 2-13 using one or several cascaded PI circuits is an option.

Also, in practice, it is more convenient to use the equivalent circuit to analyze the transmission line. This leads to the lumped parameter line model, which represents the performance of the line seen from its terminal.

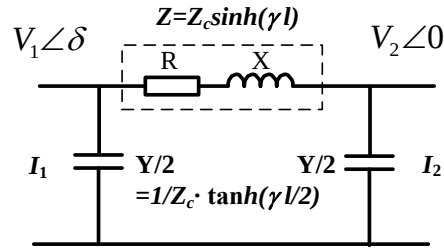


Fig. 2-13. Equivalent pi model of the single-phase long line [112].

The line can also be modeled by several sections of two-port LRC network for higher accuracy, each corresponding to a second order differential equation with inductance, capacitance, and resistance, as illustrated in Fig. 2-14.

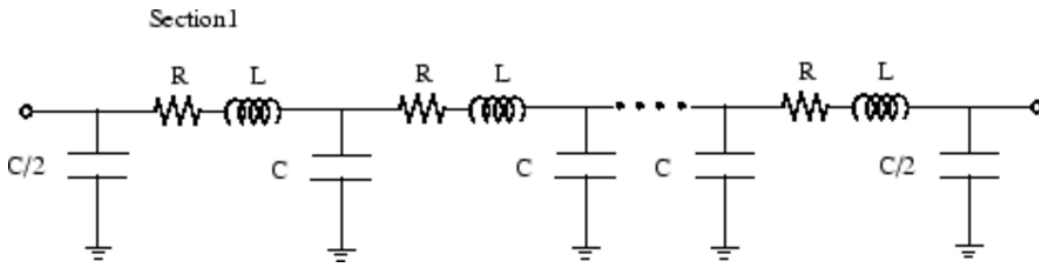


Fig. 2-14. Line model represented by multi-sections of two-port LRC network [126].

When the line length is shorter than 50 miles, it is regarded as short line and only L-R is considered. Above this length, capacitive impedance must be considered. For a long line with length above 150 miles, the general PI model for one section is

$$\begin{cases} V_1 = \cosh(\gamma l) \cdot V_2 + Z_c \sinh(\gamma l) \cdot I_2 \\ I_1 = \frac{\sinh(\gamma l)}{Z_c} \cdot V_2 + \cosh(\gamma l) \cdot I_2 \end{cases} \quad (2-5)$$

$$\begin{cases} V_1 = \cosh(\gamma l) \cdot V_2 + Z_c \sinh(\gamma l) \cdot I_2 \\ I_1 = \frac{\sinh(\gamma l)}{Z_c} \cdot V_2 + \cosh(\gamma l) \cdot I_2 \end{cases} \quad (2-6)$$

The matrix form can also be obtained as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2-7).$$

where

$$\begin{aligned} A &= \cosh(\gamma l) & B &= Z_c \sinh(\gamma l) \\ C &= \frac{\sinh(\gamma l)}{Z_c} & D &= \cosh(\gamma l) \end{aligned} \quad (2-8)$$

$Z_c = \sqrt{L/C}$, $\gamma = \alpha + j\beta = \sqrt{zy} = \sqrt{(r + j\omega L)(g + j\omega C)}$. Z_c is the characteristic impedance and γ is the propagation constant, which is frequency dependent. L and C are inductance and capacitance in per unit length.

Theoretically, the lumped line model is only accurate for short line with line length shorter than 50 miles, for which the traveling wave time is negligible.

In fact, the frequency dependent propagation constant γ and related hyperbolic correction factors may not be needed for shorter lines, but are required for longer lines, since uncompensated PI section equivalent circuit becomes less accurate as the line becomes longer, mainly due to its neglect of the uniform distribution of line parameters [122].

2.2.4 Measurement noise

Following the ITM scheme, transmission line current can be calculated from voltage measurement on two terminals. Taking the simplest scenario as the example, for a short lossless line, its lumped line model can be simplified as an inductor L . Then, its current obeys

$$i(t) = \frac{1}{L} \int (v_s(t) - v_R(t)) dt \quad (2-9)$$

In multi-converter based HTB emulation environment, this model derivation is very sensitive to voltage sampling noise. Any undesirable voltage sensing noise will induce faulty current commands and drive the emulator into the wrong track. Two types of noises are observed: 1) the

significantly high switching harmonic voltage at PCC, which is unique in the multi-interconnected converter system with only L filters, since there are no paralleled passive components to attenuate the switching voltage; 2) the dc offset noise from sensing circuit or analog/digital conversion (ADC). Unfortunately, a strong filter may be able to eliminate most of the noise, but it introduces phase delay that is not acceptable to meet emulation accuracy and bandwidth requirement.

A good sampling algorithm with correct sampling instant is therefore important for sampling quality. Typically, center-aligned (symmetrical) PWM generation is preferred for three-phase converters [127-129]. The sampling instant is in the median of the rising edge or falling edge, which naturally ensures the average value of the sampling signal and avoid noise at switching transients. Reference [128] proposes a hybrid sampling scheme for the high modulation index case in a single-phase PFC. However, unlike PFC interfacing a low distortion grid, the emulation system sees high switching noise on voltage sensing signals due to L-filter interfaced PWM converters. Moreover, these power converters, following the modular concept, are controlled independently, resulting in asynchronized PWM voltage patterns [130]. This “noisier” system with asynchronized time domains complicates the sampling and control of emulators. Analysis and possible approaches for this noisy emulation environment should be investigated.

The dc offset issue is similar to the scenario in motor control, where the motor flux feedback is estimated from the pure integration of the instantaneous ac voltage. A trivial dc drift in the voltage sampling will eventually lead to a significant high dc offset flux. Many efforts have been made in motor applications, and a literature review is found in [131]. In [132-135], different low pass filter (LPF) structures are studied to replace the integrator, which damps the dc bias to a certain level but introduces steady-state error in both phase and magnitude, especially at low frequency operation range. To compensate for this error, complicated compensation algorithms

are added [136]. Closed-loop based offset compensator is also proposed in [137] to aid the flux estimator, which however requires the flux reference information. Reference [131] further combines the dc compensation and integrator into a simplified LPF form without this information, which theoretically can achieve zero error in the specific frequency but suffers inevitable amplification of high frequency harmonics. The prior works mainly focus on the offset elimination, flux estimation accuracy, and response time at a specific stationary frequency point considering motors' variable fundamental frequency. The whole picture of the steady and dynamic performance for these controls in the full frequency spectrum is, however, missing, and consequently, it is not clear of the true impacts imposed by these controls to the original system. It is interesting to notice that the dc bias issue was never reported in HIL simulations since it is induced by measurement noise that only occurs in the real engineering world. This reflects a general difference in HTB emulation and software simulation, emphasizing the necessity of investigating the measurement issue in emulation related research and applications.

2.3 Ac interfaced aircraft power converters

2.3.1 Topologies of ac interfaced aircraft power converters

In the earlier days, transformer interfaced diode rectifier unit (RTU), and auto-transformer based ARTU using silicon thyristor were applied as the main ac front end (AFE) to converter the ac power to the dc power [138]. Bulky magnetic devices have to be applied to reduce current harmonics. With the advancement in devices and topologies, various hybrid and active rectifiers combining passive diode rectifier and switching devices are developed, to provide active harmonic controllability and allow higher switching frequency and lower passive size [43].

In [139], four active topology configurations are evaluated for aircraft motor drive in the ac-dc-ac application, covering almost the mainstream three-phase converter types, including two-

level three-phase voltage source rectifier (VSR), two-level three-phase current source rectifier (CSR), three-level Vienna-type rectifier, and three-phase ac-ac matrix converter. The matrix converter, although requires no dc link capacitor, was found with higher weight due to higher loss and larger heatsink. The two-level VSR has the simplest control, however, as a boost type rectifier, doubles switch voltage stress and converter dv/dt , compared to three-level converters. On the other hand, two-level CSR as a buck type converter results in lower dc voltage than the ac line-line peak voltage, thus it could be a possible choice in applications where device voltage stress is the main limitation, such as the current situation for GaN devices, where the maximum voltage rating is typically 600-650 V.

A typical application in aircraft power system is the battery charger to provide stable charging capability for batteries, and output voltage must be compatible with the standard dc voltage levels, i.e. 28 V and 270V. This system usually consists of two stages as illustrated in Fig. 2-15. Ac-dc PFC stage as the front-end converts ac to dc and provides an intermediate dc bus, and the back-end converter steps down and regulates the output voltage.

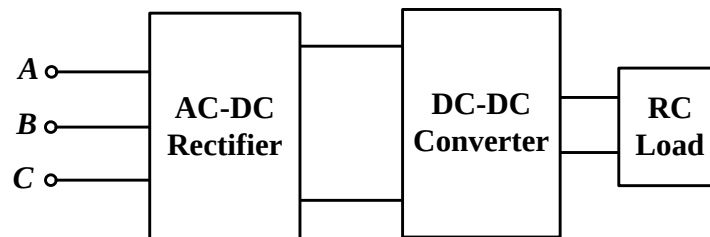


Fig. 2-15. Diagram of a two-stage power converter.

Different front-end three-phase rectifiers in charger application have been reviewed in [43]. The major group is unidirectional rectifier including passive, hybrid and active rectifiers, either in two-level structure or three-level structures. Among them, the most famous subgroup is three-level boost rectifiers, also known as Vienna-type rectifiers, consisting of two diode-switch pairs in each

phase, respectively for each half line cycle. Different phase-leg combinations have generated various variants. A comparison of two different variants was conducted in [140, 141] on power loss and package issues. With the advent of SiC device, the efficiency of the variant chosen in this work is expected to very high, possibly nearly 99% at 10 kW [43], owing to SiC diode's inherent high voltage capability and zero reverse recovery.

The power efficiency of some other bridgeless PFC in the unidirectional category was also evaluated in [142] and a two-channel interleaved Vienna-type rectifier was proposed to further reduce power loss for 3 kW design [143].

The other group is the bidirectional rectifier, which mainly includes the common two-level VSR, and three-level I type and T-type NPC rectifier [144]. These NPC converters are often used in high voltage and high power applications.

As for back-end dc-dc, the isolated power converter is the main option in battery charger design for safety concern. Phase shift full bridge, dual active bridge converters are the main options due to the ZVS capability, low switching losses, lower circulating current stress and high power handling capability [145, 146]. At lower power, LLC resonant converter is a more attractive solution with low switching loss at full voltage and load range, significantly reduced magnetic size resulting from high switching frequency operation up to MHz [147]. In addition to the above two-level dc-dc, many three-level dc-dc converters adopting the similar concept used in three-level ac-dc converters have been developed to reduce the device voltage stress, mainly differing in how to achieve the three-level and/or split the dc bus voltage to half. They can be grouped as flying capacitor and diode-clamping types [148, 149], as well as their hybrid combinations, to provide better voltage balance [150]. For each type, the output terminal formulation may also differ.

Modulation, voltage balance, and soft-start are generally the main challenging in these topologies, although different variants may feature in certain aspects.

Although most of the literature focused on either the front-end or the dc-dc stage, several papers did present the whole charger design. A 1.2 kW two-stage charger consisting of a three-level Vienna-type rectifier and LLC dc-dc converter was designed in [151] using Silicon MOSFET. It is highlighted with 99% efficiency and natural convection cooling without a heatsink. Since the rectifier only interfaces with 115 Vac voltage and 28 V dc, the intermediate dc bus voltage was chosen at only 340 V, enabling using a low voltage device. In addition, low switching frequency at 68 kHz is selected to achieve low loss target, resulting and two-level VSR are also compared, indicating low EMI filter and loss in the Vienna-type rectifier, but larger boost inductor needed due to elevated side-band switching noise below switching frequency. The design becomes more challenging when the charger interfaces with wide input voltage 115 Vac and 235 Vac, which requires ac-dc rectifier with a common dc voltage to be compatible with both ac conditions. In Vienna-type rectifier case, this dc voltage could be above 650 V, leading to potentially higher converter loss. Recently, a three-phase two-level VSR plus phase shift full bridge dc-dc was developed in the dual input application [152, 153], with dc output regulated at 28 V and 650 V intermediate dc bus. Due to high voltage stress in the two-level structure, 1200 V SiC MOSFETs instead of Si IGBTs are adopted to allow high frequency design and achieve a lower weight.

2.3.2 WBG power semiconductor device

One of the main drives for power converter advancement is ever-improving power semiconductor device technology. This is also true for aircraft power system. With the emerging and blooming of wide bandgap devices, such as SiC and GaN devices, passive and line frequency commutated TRU and ATRU can be replaced by active rectifiers. And converters can be pushed

to high switching frequency and power density, significantly reducing weight and size, due to the high switching speed, low conduction resistance and junction capacitance, as a result of the intrinsic properties in WBG devices illustrated in Fig. 2-16.

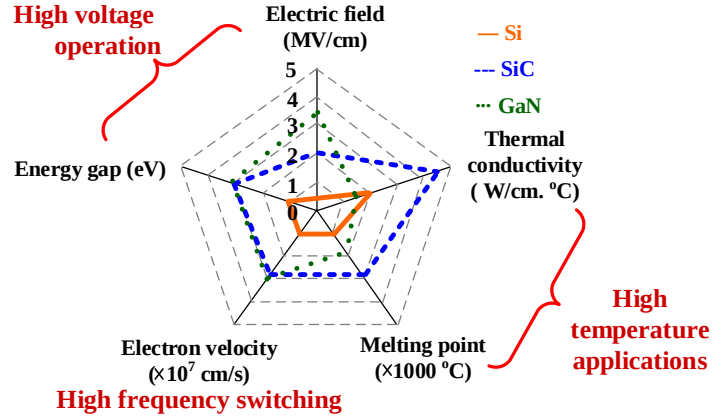


Fig. 2-16. Comparison of different types of device materials [154].

Two-level VSR can be directly applied at 650 V dc bus, by using 1200 V SiC MOSFET at 100 kHz [152], instead of the three-level rectifier with Si CoolMOS in the past [155]. Three-level rectifiers can be designed further small by pushing to even higher switching frequency such as 450 kHz if using GaN devices [156, 157] instead of 70 kHz with JFET or 68 kHz with Si devices [158]. Certain topologies with fast switching diodes suffering high voltage stress and significantly high recover recovery switching loss can be now utilized if SiC Schottky diode is used. A good example is Vienna-type rectifier.

However, the characteristics of these new WBG devices are still in investigation currently before they can be fully commercialized in products. The high dv/dt , di/dt , low profile, and high frequency operation of WBG devices impose new challenges on many aspects of converter design, such as gate driver design, power loop layout, cooling, filter design, and control design. A comprehensive understanding of the characteristics and associated effects and a reformulation of

existing design procedures developed for Si-based converters are demanded. Some of the key issues will be addressed in this dissertation.

2.3.3 Power quality control in high speed high frequency converter

Low on resistance and high switching speed have driven the research, commercialization, and application of WBG power semiconductor devices, such as SiC and GaN devices, for a more efficient and compact converter design [154, 159, 160]. However, as WBG devices are applied in practice, more design issues arise, such as the need for optimal power loop layout and device package to reduce parasitics [161, 162], thermal management for low profile devices [163], gate driver immunity to switch fast and safely [164-167]. And high di/dt and dv/dt are regarded as the main obstacles to electrical performance improvement of WBG converters. High di/dt induced ringing and overvoltage in the switching commutation loop introduce high voltage stress, extra loss, and severe radio frequency (RF) and EMI emission, thus deteriorate device lifetime and converter efficiency and cause oversize of passive filters. High dv/dt noise, on the other hand, often induces spurious gate voltage, resulting in cross-talk issue in bridge configurations. Besides, the high CM voltage transient may also cause the malfunction of gate driver ICs. Plenty of work has also been done in mitigate cross-talk through the gate driver design either actively, intelligently, or passively [166-170], and the new generation SiC MOSFETs has also been developed tackling the cross-talk issue intrinsically. Meanwhile, commercial high speed gate drivers are now marked with 100 to 200 V/ns high common mode transient immunity (CMTI) [171], significantly simplifying gate driver design with higher reliability.

However, the above progress is mainly on the power circuit design, i.e. the basic layer of WBG converter design. The impacts of high frequency, high di/dt , dv/dt on the second layer, i.e. the sensing, conditioning, and control layer, have seldom been studied.

Especially, for grid-connected inverters or power factor correction (PFC) rectifiers, power quality including current harmonics and power factor limits are required by various standards, such as IEC 61000-3-2 [172], IEEE 519-2014 [173], and DO-160E [174]. For dc-dc converter directly interfacing with local loads, such as POL or back end of a battery charger, the accurate regulation of voltage and current is also required [175, 176]. This highlights the importance of understanding the impact of the harsh operating environment on the sensing, conditioning and control layer.

In fact, it has been a rooted impression that if a converter is pushed to high switching frequency, e.g. exploiting WBG devices, it should become easier to achieve good control quality due to the higher control bandwidth and lower switching ripple.

But this is not always true. Some control challenges have been observed recently in applications of high speed and high switching frequency devices, e.g., reference [177] discussed the zero-crossing detection error in peak current control due to EMI distortion using contactless current sensor for GaN based high frequency buck, reference [178] listed several sensing distortions and conditioning circuit arrangements in 500 kHz GaN full bridge converter, and references [156, 157] illustrated device parasitics' impact on current harmonics in a high frequency three-level GaN rectifier. The prior works were more specifically focused on one aspect of the complex issue and did not provide the overall relation between harsh operation environment caused by 'high dv/dt , di/dt , high frequency' and sensing/sampling/control.

2.3.3.1 High speed high frequency harsh environment on sensing

The integrity of the current sensing signal is of vital importance for current feedback control. In a typical Si IGBT or Si MOSFET based ac converter system operating with low or medium switching frequency, e.g. 1k Hz ~ tens of kHz, and with low dv/dt or di/dt , current sensors can function properly. However, as switching frequency and speed increase, signal integrity issues

may arise. Especially when SiC and GaN devices are adopted, high dv/dt and di/dt owing to their fast switching further strengthen the noise and component stress, challenging the gate driver design, EMI filter design, as well as current sensing and sampling quality. A sensor works normally at low switching speed might get severely distorted under high-frequency high-speed conditions.

2.3.3.2 High speed high frequency harsh environment on sampling

It is also essential to guarantee the integrity of sampled feedback signals. Synchronizing analog-to-digital converter (ADC) with PWM carrier is a typical way in power electronic converters to avoid noise spikes and associated ringing of the measured signals around switching instants. Current sampling instant, in particular, should be carefully selected if THD requirement is a concern in ac-dc or dc-ac converters. A typical realization, also known as symmetrical modulation, is to align ADC sampling in the middle of a turn-on interval through triangle shape based modulation carrier. By center-aligning the timing, the average current value can be accurately acquired. Considering the time-variant duty cycle in ac/dc converters, reference [128] further alternates the sampling instant between the rising edge and falling edge of the switching ripple when duty cycle crosses 0.5 in a single-phase PFC application, to seek the longer sampling interval and leave ample time for ADC sampling-and-hold and digital conversion. Unfortunately, the single-phase approach cannot be conveniently applied for three-phase converters. Even worse, since the switching period in GaN based high frequency converters shrinks shorter, almost comparable to the sampling period of a commercial ADC, the selection of longer sampling interval becomes essential and more difficult.

2.3.3.3 Deadtime and turn-off impact on PWM voltage distortion

The distortion introduced by dead time in the voltage source converter or by overlap time in current source converter has been thoroughly studied in the past. In recent years, the effect of

device junction capacitance or snubber parasitic capacitance accompanied with dead time or overlap time, have also been presented, and their focus is on compensating the dead-time in voltage-fed motor drives [179-183] or on the overlap effect in current-fed rectifiers [184]. While most of the past work on dead-time compensation did not consider the nonlinear output capacitance, their basic schemes are still popularly adopted in recent literature. In [179-181], the dead-time distortion is treated as a voltage loss or voltage error, and this error is compensated to the voltage reference. In [182], the dead-time is modeled as a pulse error and compensated in each PWM period, and the idea is to extend or shrink the diode-clamping edge to cancel the voltage error introduced at the switching edge. Ref. [183] investigates the excessive compensation issue of the pulse-based method in motor drive applications, when considering the impact from the snubber capacitance of each IGBT module, and then corrects the dead-time compensation by comparing the actual PWM voltage and the ideal voltage on both the falling edge and rising edge. In this way, an equivalent volt-second area can be achieved by adjusting the diode-clamping intervals on both edges. Ref. [179] extends the voltage loss compensation scheme by considering a more detailed device model and adding an offline identification of key parameters in motor drive applications. Ref. [185] also adopts the voltage loss compensation scheme but further compensates the dual edges of the critical switching cycle around both zero crossing points of the ripple current. This method requires instantaneous current measurement based on the inductor voltage, introducing extra hardware and complexity. Though the voltage loss approach avoids adjusting the turning on/off edge in each switching cycle, it only provides an insufficient compensation on the duty cycle when considering the device output capacitance as will be discussed in this work.

The input current distortion caused by transistor turn-off delay can also be very problematic for converters with switching frequencies in the hundreds of kHz, especially in the vicinity of the

phase current zero-crossing. It has been reported in [155] that this distortion in the Vienna-type rectifier as shown in Fig. 2-17 is mainly due to the nonlinear output capacitance C_{oss} of the super-junction MOSFET because the voltage rise time at turn-off can be quite long within a relatively short switching cycle. This leads to a significant voltage error at the converter ac terminal, as well as corresponding current harmonics through the input boost inductor.

The super-junction Si MOSFET has a particularly nonlinear output capacitance, with a steep dropoff of several orders of magnitude at 50-100 V. The turn-off voltage slew rate is initially very low until the drain-source voltage reaches that level. As a result, a significant turn-off delay and relatively short voltage rise time are observed. Ref. [155] proposes compensating for this nonlinear turn-off delay time through curve fitting of experimental data over the whole current range. However, for enhancement-mode (e-mode) GaN devices, the turn-off delay time is very short, and the voltage rise time is the dominant component of the turn-off time [154, 186, 187]. As a result, a new compensation scheme is needed, to avoid severe distortion near zero crossings due to the nonlinear voltage rise time in e-mode GaN. In the case of the Vienna-type rectifier, the output capacitance of two diodes also participates in the turn-off commutation of each GaN FET as will be revealed in this work. Consequently, it is beneficial to find an analytical model to compensate for this nonlinear distortion, which can be adapted to different combinations of devices using their capacitance characteristic curves.

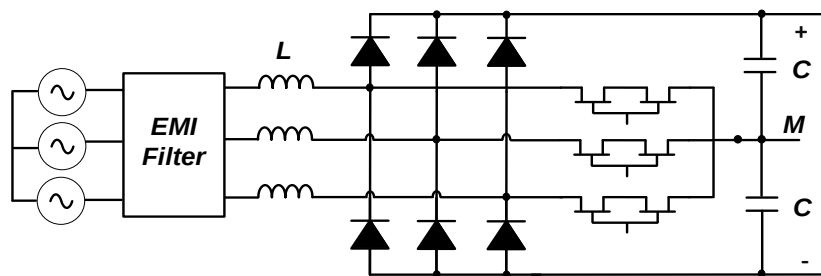


Fig. 2-17. Schematic of a GaN based three-phase Vienna-type rectifier as a PFC converter [157].

It is also important to point out the difference between dead-time in the normal half-bridge converters and turn-off delay in Vienna-type rectifiers. For dead-time related voltage distortion, the voltage error only occurs within a fixed dead-time interval, and the distortion can be determined with a voltage error vs. phase current curve [179]. However, for the turn-off distortion in Vienna-type converters, the duration is not fixed. Instead, it occupies a varying percentage of the switching cycle, due to the C_{oss} limited commutation of phase current from the main switch to the diode. As a result, the voltage distortion is determined by both the instantaneous current and the instantaneous duty cycle, thus presenting more challenges.

To regulate the dead-time induced harmonics, feedback controls are also applied [188, 189]. However, these methods require high control bandwidth and a sophisticated controller and are more applicable when the fundamental frequency and switching frequency are relatively low, such as in industrial motor drives. Nevertheless, converters, switching at hundreds of kHz generally require much higher computation speed. In addition, in an aircraft power system, the fundamental frequency can be up to 800 Hz, thus, much higher control bandwidth is thus required for harmonic reduction. With a limited computation capability in a typical DSP controller, feedforward compensation schemes are more appealing than feedback control.

2.3.4 Electromagnetic interference

Since EMI issue is crucial for industrial products in almost all applications such as utility interface, automobile, and aircraft, various and stringent international and US standards have been enacted [174, 190, 191], such as CISPR 22 & 25, FCC Part 15, MIL-STD-461D/E/F, and airborne equipment standard DO-160 E/F/G. Therefore, all converters must comply with the associated EMI standards. This drives numerous research on EMI issues. The prior work can be categorized into three main directions if following the classic circuit concept. i.e. a signal is generated from its

source and transmitted to the load through certain paths, as illustrated in Fig. 2-18. A recent review of conducted EMI mitigation techniques is also reported in [192]. Since the scope of most power electronic converter design is in near-field frequency range from 10 kHz or 150 kHz to 30 MHz, the focus of the dissertation is on the conducted emission instead of the radiated emission spanning from 30 MHz to several GHz.

At the source side, since both the common mode noise and differential mode noise are generated from the converter switching action, modeling and prediction of the source noise and source impedance are valuable for guiding the converter design, modulation, and filter design. Various analytical models have been proposed for different converter topologies. Ref. [193] considered the subintervals of switching actions, [194, 195] applied unterminated behavior model, and [196] simplified the switching devices as equivalent voltage and current sources, and [193] further approximated the source impedance using impedance masking concept. Different PWM modulation methods have also been devised to reduce the noise emission. Common voltage reduction modulation through various zero-vector arrangement was reported in [197, 198]. Instead of fixed switching frequency, random switching frequency and variable frequency modulations were also widely applied in three-phase motor drives for common mode (CM) and differential mode (DM) reduction [199-209]. Interleave modulation in phase-leg level or converter level also helps reduce DM noise [210-214]. Some special inverter topologies were also proposed for CM voltage mitigation in open-end winding motor applications, such as four phase-leg inverters and balanced inverters [215-217]. In addition, the impact of dv/dt switching speed on EMI were investigated theoretically and experimentally in IGBT, SiC, GaN converters from dc-dc to single-phase inverter and three-phase inverters [215-222]. Generally, this impact is above tens of MHz, mainly in radiated noise range.

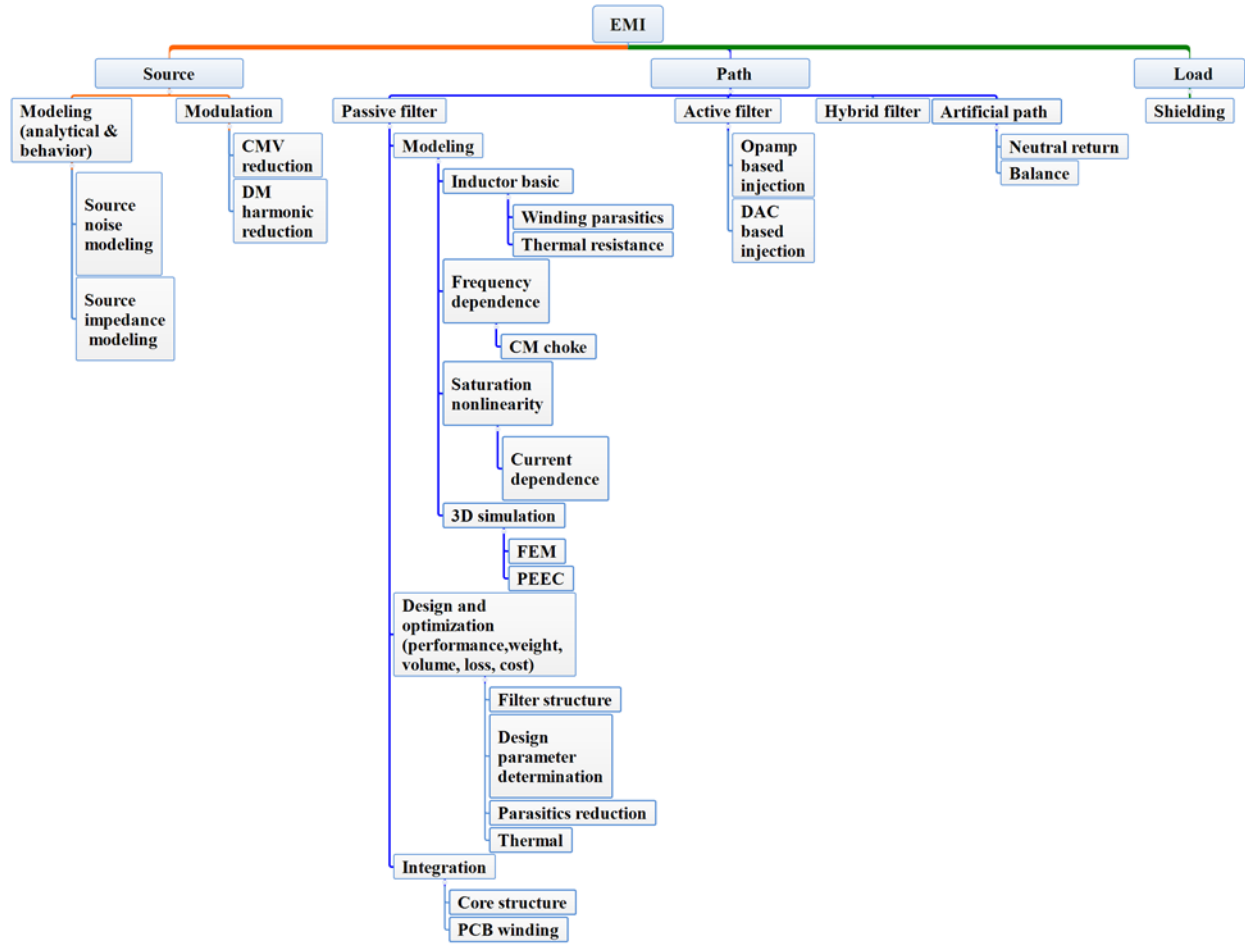


Fig. 2-18. Review of prior works in EMI filter field from the basic circuit perspective.

As shown in Fig. 2-18, the majority of EMI research was focused on noise reduction through propagation path, mainly using EMI filters to either bypass the noise current or suppress the noise voltage and block noise current. The dominant filters are made of passive inductors and capacitors, while some active solutions using semiconductor IC chips were also proposed. A lot of efforts have been in the characterizing and modeling of EMI filters, from modeling of the physical inductor's parasitic capacitance [223-227], thermal resistance [228, 229], impedance characteristics and equivalent circuit considering magnetics' frequency dependence [223, 230-236], magnetics' current dependent saturation nonlinearity [233, 237-241].

Inductive coupling and capacitive coupling of passive components in a multi-component filter are also concluded as key factors degrading filter performance [242]. However, due to the invisible and multi-branch coupling paths strongly related to component geometry and dimensions, theoretical modeling is still impossible. Thus, it is either relied on complicated and expensive 3D numerical simulation tools such as finite element method (FEM) based, method of moments (MOM) based, finite difference time domain (FDTD) based, and partial element equivalent circuit (PEEC) based solutions to predict the coupling impedance given that the filter prototype information is known [234, 243, 244], or relied on s-parameter measurement on a given filter through expensive instrument to back-calculate the coupling impedance [245].

Because of these challenges in modeling of component coupling, understanding and design knowledge here is limited. In reference [242], the effects of inductive coupling and capacitive coupling on CLC PI structure DM filter were investigated. The focus was, however, on inductive coupling, and only ground plane induced capacitive coupling was considered, which has a slight impact above 10 MHz like inductor's paralleled capacitance. [246] claimed that inductive coupling is the main problem in DM filter instead of self-parasitics, and self-parasitics is the main issue in

CM filter since coupling impact is small due to higher permeability of choke core. However, a later study on inductive coupling in CLC PI structure CM filter in [247], showed that some parasitic inductive couplings have significant impacts and the critical one is input and output loop coupling. A recent study in [248], further verified this concept from both analytical and 3D simulation results in CLC structure CM filter.

Parasitics reduction techniques to improve HF filter attenuation performance were also explored. Ref [246, 249-252] proposed equivalent parallel capacitance cancellation for CM choke with small extra capacitance in PI-shape filter and on DM inductor using small inductance in PI-shape filter, and [253, 254] controlled PCB trace length to form a negative coupling inductance to offset the ESL of capacitor branch. Inductive coupling mitigation from two-stage DM capacitors was also reported in [251, 255] by adding an extra opposite winding loop on a film capacitor and re-encapsulate in into film package. However, these methods are either effective exclusively for certain LC networks, or too sensitive in terms of passive component parameters and not easy for tuning and reproductivity. A more general and simpler approach is desired.

Winding schemes also impact parasitic capacitance of an inductor [225-227, 256-262]. The parasitic capacitance of different winding direction and wire arrangement have been modeled for single-layer or multi-layer winding inductors and transformers. The desired winding scheme should ensure the potential difference of nearby winding small. Due to higher equivalent layer-to-layer capacitance as well as its coupling and proximity effects in the multi-layer winding, a single-layer design is a commonly preferred choice.

Design optimization on physical DM and CM inductor implementation was also studied, where all design variables such as winding turns, wire size, core material and geometry, flux density margin, and temperature rise, etc. are controllable to find the optimized result in terms of

loss, weight, size, price, or thermal stress. The procedure is applied in the whole filter design, including filter stage number determination, LC parameter value determination, and inductor physical design variable optimization [263-275].

In addition to the passive filter approaches, active filter solutions are also available. They are mainly based on the detection-injection concept where the raw noise either voltage or current is sensed using direction detection circuitry, then a reversed noise either current or voltage is injected back to ensure the output line current is less noisy. Depending on the relative location of detection and injection joints, feedforward type and feedback type active filters are proposed [276-284]. And if further consider the combination of detection type and injection type [276, 282, 283], eight schemes can be derived. In addition to the detection and injection links realized by RC or coupling network, the main conditioning component in an active filter was often implemented by an op-amp chip, and a transistor buffer can be added if higher noise power is required. The challenges in low frequency bandwidth from both the power op-amp and buffer transistors as well as LRC detection-injection network, higher loss due to linear region operation of op-amp and buffer as well as some coupling transformer as detection-injection link [283], stability issues due to Op-amp compensation loop [192, 285], and reliability concern for these relative low power circuits interfaced main power lines, have greatly limited both the filter performance and application of active filters. Now, only Vicor has a commercial product using this active concept [286]. Recently, another digital realization scheme using high sampling rate ADC and DAC converters was proposed to get rid of bulky injection links and analog op-amp [287, 288]. It is interesting, however, the requirement on both sampling rate and current driving capability are currently the barrier in using this scheme for higher power and higher frequency noise mitigation. A hybrid filter solution

utilizes active filter for lower frequency and passive filter for higher frequency noise filtering was also proposed [283], reducing the design difficulty and limitation of current technology.

3 HVDC Converter Interfacing with HVAC Transmission Line

Interfacing with ac directly by dc converters is a promising approach for enhancement of power transfer capacity. The interaction of ac and dc should be properly understood. The dc injection traditionally was regarded as a hazardous attempt to the normal operation of ac transformers, now will be uniquely solved. Interfacing both forms of power flow under abnormal operating conditions is also critical and need be overcome. Eventually, to promote the proposed architecture in the field, feasibility and cost performance of this system shall be evaluated.

3.1 Main drive for hybrid ac/dc transmission

In US, the total miles of transmission lines are 190,782 in 2012 [289], and distribution miles are 5.8 million miles (2010) [290] with around 10 miles average length per line [291]. Assuming a normalized transmission capacity 201 MW-miles/MW-demand [292] and its total power capacity 1,039,062 MW (2010) [293], the normalized transmission miles can be obtained from

$$Normalized_Miles = \frac{\sum l_i P_i}{\sum P_i} = \sum l_i \frac{P_i}{\sum P_i} \subseteq [\min(l_i), \max(l_i)] \text{ as } 243,000 \text{ GW-mile}/1,039,062$$

MW=233 miles. This forms an overall normalized grid in US as illustrated in Fig. 3-1.

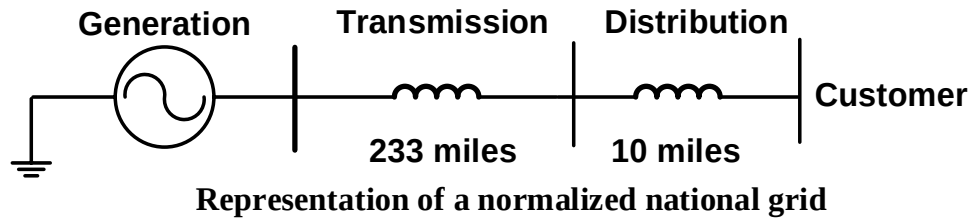


Fig. 3-1. Representation of a normalized national grid in US.

Clearly, in US, the long transmission line is dominant. Enhancing the power transfer capacity on these long transmission lines is vitally important. Fortunately, for the long transmission line, its thermal margin is far beyond the actual operating rating, mainly because of the power angle

stability constraint. Thus, the further utilization of the potential current margin is an effective way for power enhancement. Hybrid ac/dc transmission system as shown in Fig. 3-2 becomes a promising solution that combines the advantage of HVAC and HVDC. The dc current will be injected through a device into ac lines, and the line voltage will be also shifted up to enable active dc power flow.

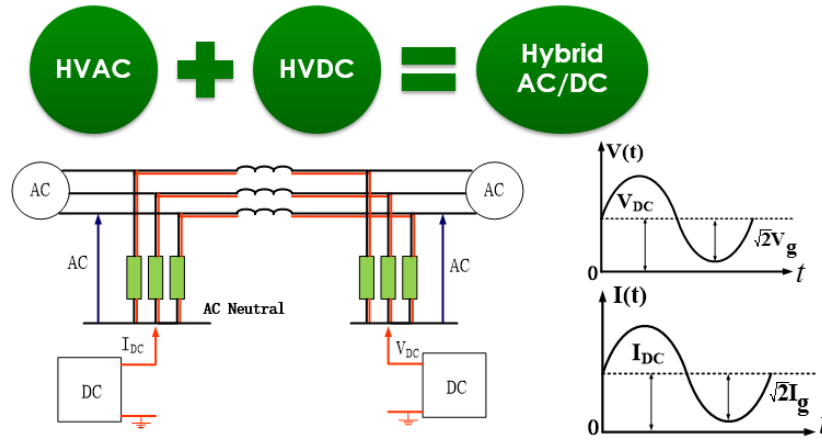


Fig. 3-2. Concept diagram of hybrid ac/dc transmission system (only unipolar is shown).

3.2 Dc current injection and saturation issue

The key component for the hybrid scheme is the dc injection device, which should provide: 1) a connection between dc and ac sources, 2) a high impedance path for ac current, and 3) low impedance for dc current. A zigzag transformer with neutral point dc injection can basically meet these requirements while avoiding dc-current bias caused saturation. A delta/zigzag transformer is shown in Fig. 3-3 (a), with two secondary windings connected in a zigzag way and reversed polarities. It can also be possible to use a normal three-phase ac transformer combined with only zigzag windings at the secondary side, as illustrated in Fig. 3-3 (b).

For ac positive and negative sequence currents in each phase, the winding voltage of two zigzag windings has 120° phase shift. Consequently, the magnetizing inductance of the phase-to-

neutral is three times of the winding inductance [67]; whereas, for zero sequence, two winding currents will cancel their fluxes due to opposite polarities, which produces a low zero-sequence inductance.

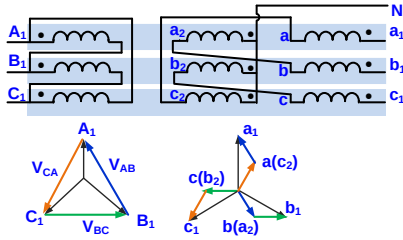
Another possible solution is through LC resonance tank, as shown in Fig. 3-4. However, the anticipated high voltage stress due to the parallel resonance and high reactive power loss prohibit this scheme.

3.2.1 Dc magnetic analysis of zigzag transformer

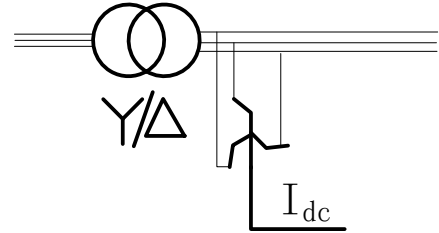
With flux cancellation and low zero sequence impedance, the zigzag transformer is ideal for dc injection through the neutral point. For secondary zigzag windings with primary side open, according to superposition theorem and Ampere's law, one can obtain

$$(H_{AC} + H_{DC})l_m = N_1(I_{ma_AC} + I_{a_DC}) - N_2(I_{mb_AC} + I_{b_DC}) \quad (3-1)$$

$$\begin{cases} H_{AC}l_m = N(I_{ma_AC} - I_{mb_AC}) \\ H_{DC}l_m = N(I_{ma_DC} - I_{mb_DC}) \end{cases} \quad (3-2)$$



(a) Structure I of a three-phase zigzag transformer



(b) Structure II of a three-phase zigzag transformer

Fig. 3-3. Connection and structures of a three-phase zigzag transformer.

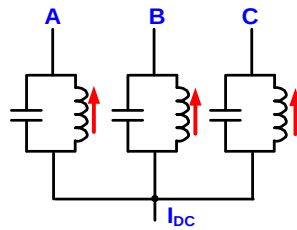


Fig. 3-4. LC parallel resonance tank to inject the dc power into ac line.

where l_m is the magnetic path length; I_{ma_AC} , I_{mb_AC} are the ac magnetizing currents of phases a and b; I_{a_DC} , I_{b_DC} are the dc currents in phases a and b; H_{AC} , H_{DC} are the ac and dc flux intensities. The flux through each limb of the three-phase magnetic core is proportional to the differential line currents

$$\begin{cases} \Phi_{a_DC} = L_{wm}(-I_{a_DC} + I_{b_DC}) \\ \Phi_{b_DC} = L_{wm}(-I_{b_DC} + I_{c_DC}) \\ \Phi_{c_DC} = L_{wm}(-I_{c_DC} + I_{a_DC}) \end{cases} \quad (3-3)$$

where L_{wm} denotes the winding inductance.

Based on Ohm's law, if the three ac lines are balanced, dc current will be evenly distributed, which guarantees cancellation of the dc flux along each limb of the magnetic core without dc saturation.

3.2.2 Dc current distribution with ac line unbalance

However, the original scheme relies on that the dc injection transformer can well performance under even dc current flow among three phases. For a practical three-phase ac transmission line, the three lines are not perfectly balanced. The impedance unbalance among three-phase conductors is inevitable as a result of length variation, temperature, sag, and degrees of transposition. Depending on the line and tower geometry, the total zero-sequence unbalance of double-circuit un-transposed lines may vary from 2% to 4% [294]. Since only resistance is involved for the steady state dc current distribution, this paper will focus on the resistance unbalance. Although resistance unbalance is relatively small, normally within 4% [294], its impact on zigzag transformer design is significant. When the three-phase ac line resistances are not equal, the total injected dc current through the neutral of the zigzag transformer will be unevenly distributed among the three lines as well as the three limbs of the zigzag transformer. Dc flux will not be canceled, potentially leading

to magnetic core saturation of the zigzag transformer and eventual failure of the hybrid ac/dc scheme. The details are shown as follows.

If the per-phase winding resistance of a zigzag transformer is $R_{za,zb,zc}$, and the ac-line resistance is $R_{a,b,c}$, as depicted in Fig. 3-5, assuming $R_{za} = R_{zb} = R_{zc} = R_z$, one can obtain the current distribution as

$$\begin{cases} I_{a_DC} = \frac{I_{DC}(R_b + 2R_z)(R_c + 2R_z)}{R_{II}'} \\ I_{b_DC} = \frac{I_{DC}(R_a + 2R_z)(R_c + 2R_z)}{R_{II}'} \\ I_{c_DC} = \frac{I_{DC}(R_a + 2R_z)(R_b + 2R_z)}{R_{II}'} \end{cases} \quad (3-4)$$

where

$$R_{II}' = (R_a R_b + R_a R_c + R_b R_c) + 4(R_a + R_b + R_c)R_z + 12R_z^2 \quad (3-5)$$

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Fig. 3-5. Zigzag windings and three-phase line resistances.

Taking a simple case as an example, if line impedance $R_a > R_b = R_c$, according to (3-4), the steady state dc current difference for limb a is

$$\Delta I_{a_DC} = -I_{a_DC} + I_{b_DC} = \frac{(R_a - R_b)(R_c + 2R_z)}{R_{II}'} I_{DC} = \frac{\Delta R_a (R_c + 2R_z)}{R_{II}'} I_{DC} \quad (3-6)$$

which can be further illustrated in Fig. 3-6, with the degree of line unbalance β defined in (3-7).

Note $R_{balance}$ is the median of the three-phase line resistances.

$$\beta = \frac{\max(R_{a,b,c} - R_{balance})}{R_{balance}} \quad (3-7)$$

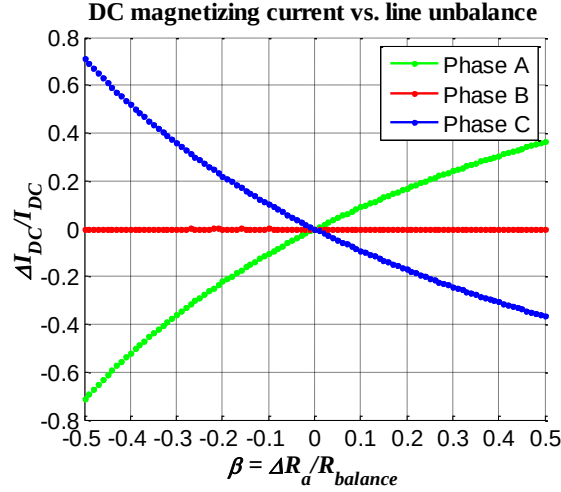


Fig. 3-6. DC magnetizing current among three-phase of the zigzag transformer with unbalanced lines.

3.2.3 Saturation analysis

As assumed above, I_{a_DC} is smaller than I_{b_DC} , which is equal to I_{c_DC} . This may cause saturation on limbs a and c . The phenomenon can be explained in Fig. 3-7, where the three-phase dc fluxes ϕ_a , ϕ_b and ϕ_c are shown respectively denoted by red, green and blue dotted line. For clarity, the flux density is indicated through line length, and only the dc flux is considered based on the superposition principle.

Assume that the windings in the three limbs have an identical coupling factor of 0.5. Originally without considering the magnetic coupling, in limb a there are two dc flux components ϕ_a and ϕ_b , by I_{a_DC} , I_{b_DC} respectively due to the zigzag winding configuration, and they are not fully canceled. The same case exists for limb c . As a result of the magnetic coupling, half of residual flux ϕ_c in limb c will flow into limbs a and b , and half of residual flux ϕ_b in limb a will flow into limbs c and b . The residual flux cancels in limb b but does not in a or c . Therefore, limbs a and c will be saturated. Moreover, since the saturation degree is proportional to the total dc current according to (6), it will restrict the amount of dc power that could be injected into the hybrid lines. If all three

lines have different resistances, all three limbs will have non-zero dc fluxes and are susceptible to saturation.

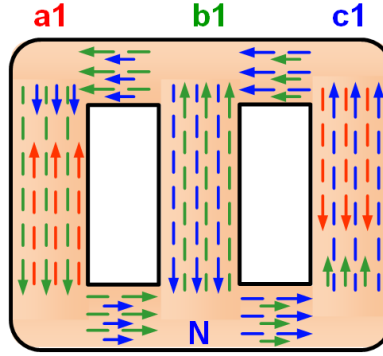


Fig. 3-7. Dc flux distribution among zigzag transformer.

3.3 Passive anti-saturation approaches

3.3.1 Dc margin approach

The equivalent circuit of delta/zigzag transformer is shown in Fig. 3-8, with two secondary windings connected in a zigzag way and reversed polarities.

To find the impedance relationship of zigzag windings, open circuit analysis is done with primary delta side open.

For positive/negative sequences current in each phase, the winding voltage of two zigzag windings have 120 degrees phase shift, so phase voltage and winding voltage follows:

$$V_{aN} = \sqrt{3}V_{aW} \quad (7)$$

And due to 120° phase shift of magnetizing current I_{ma} and I_{mb} , the magnetizing current I_m flowing through zigzag winding will be

$$I_m = \sqrt{3}I_{ma} \quad (8)$$

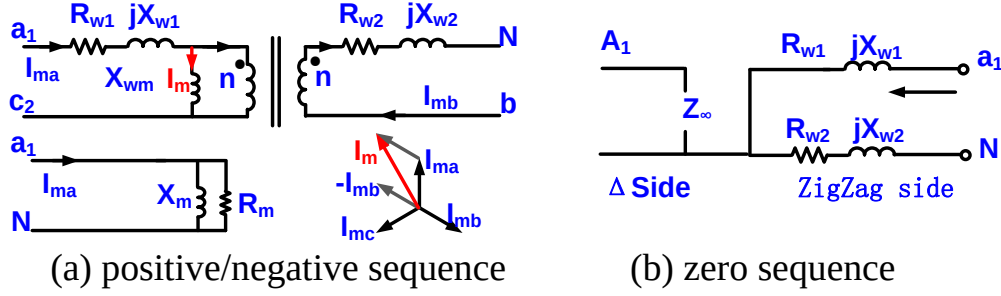


Fig. 3-8. Sequence impedances of zigzag windings.

Consequently, the magnetizing inductance of phase to neutral is three times of winding inductance L_m , given in (9). And the larger this inductance, the smaller magnetizing current, which reduces reactive power loss of the transformer. More importantly, this inductance has an influence on dc injection design.

$$X_{m_ph} = \frac{V_{aN}}{I_{ma}} = \frac{\sqrt{3}V_{wa}}{I_m / \sqrt{3}} = 3X_m \quad (9)$$

For zero sequence ac or dc, however, two winding currents will cancel out their flux due to opposite polarities, which makes low zero sequence inductance.

To avoid zigzag transformer saturation, a basic idea is to design the transformer with certain dc flux margin to tolerate dc flux created by the unbalanced dc current as shown in Fig. 3-9 and Fig. 3-10.

1) First, derive the steady dc differential ratio $\Delta I_{DC}/I_{DC}$ as a function $f(\Delta R/R)$ of the unbalanced impedance ratio, as shown in Fig. 3-6.

2) Set the maximum value of $\Delta R/R$ for a given design.

3) Set the ac magnetizing current ratio γ , e.g. around 1% for the high power transformer.

4) Determine ac flux density according to (3-8)~(3-9). The secondary side flux distribution can be determined by ac and dc magnetizing current, where subscript z denotes zigzag side winding.

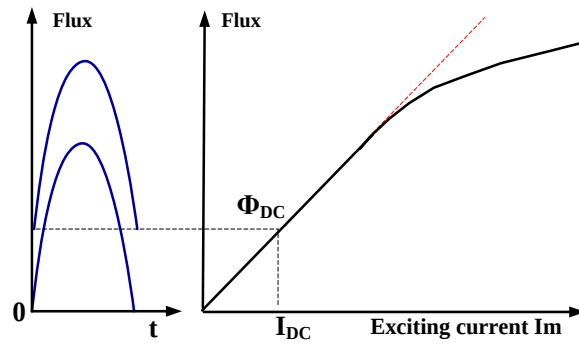


Fig. 3-9. Illustration of dc flux margin design for anti-saturation.

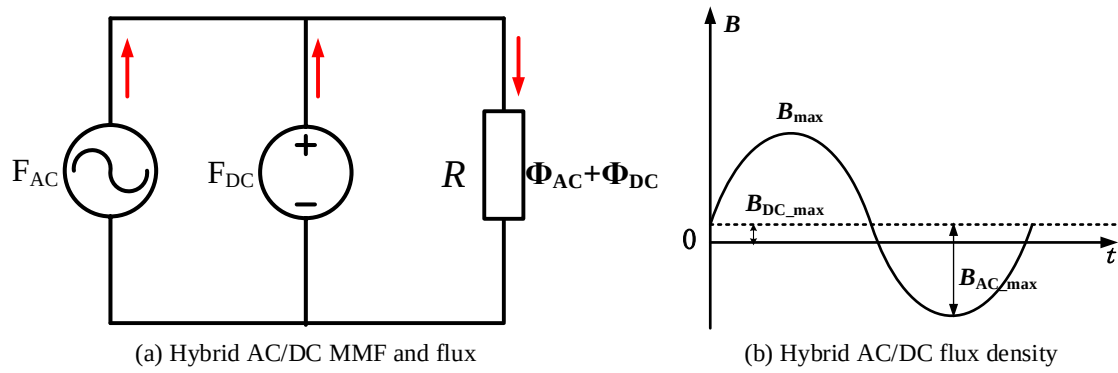


Fig. 3-10. Illustration of dc flux margin design for anti-saturation.

$$\frac{B_{DC}}{B_{AC}} = \frac{I_{zm_DC}}{I_{zm_AC}} = \frac{f(\Delta R/R) \cdot I_{DC} / 3}{\sqrt{3} \gamma \cdot I_{AC}} \quad (3-8)$$

$$B_{AC} = B_{Rate} \frac{B_{DC}}{B_{AC} + B_{DC}} \quad (3-9)$$

5) With lower B_{AC} , turns N needs to be increased to keep the same magnetizing inductance and meet magnetizing current ratio requirement. Correspondingly, certain air gap is needed, which can be calculated based on three-phase limb magnetic loop analysis, shown in Fig. 3-11 and (3-10) ~ (3-12), where R_{Ta} , R_{Tb} and R_{Tc} are yoke reluctances in the T structure and R_{ga} , R_{gb} and R_{gc} are air gap reluctances.

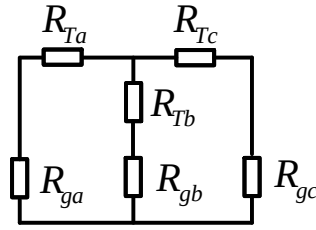


Fig. 3-11. Equivalent reluctance of three-phase three-limb transformer for secondary zigzag windings.

$$R_g = \frac{\frac{l_g}{2}}{\mu_0 A_c} \quad (3-10)$$

$$L_{zm} \approx \frac{2\mu_0 N_z^2 A_c}{l_g + \frac{MPL}{\mu_r}} \quad (3-11)$$

$$l_g = \frac{4\pi f \mu_0 N_z^2 A_c I_{zm_AC}}{V_{z_AC}} - \frac{MPL}{\mu_r} \quad (3-12)$$

6) For higher $\Delta R/R$ requirement, larger air gap may be required, and ac magnetizing current will increase a little.

However, compared to typical high-power ac transformers with peak ac flux density close to the saturation level to fully utilize magnetics, the extra margin has to be provided to accommodate any dc flux bias in this hybrid approach. This adds considerable cost to the transformer [67].

3.3.2 Experimental verification

Fig. 3-12 depicts a scaled-down zigzag transformer made of EE core using the amorphous 2605SA1 material. Its saturation flux density is 1.56 T, and the peak B_{AC} is set at 0.9 T aiming for 15% unbalance tolerance margin. Tests were conducted under rated 70 V/70 V (rms), 60 Hz ac voltage, 3 A_{rms} ac and 12 A_{dc}.



Fig. 3-12. A prototype of the three-limb three-phase zigzag transformer.

Fig. 3-13 (a) shows the unsaturated winding currents of limb *a* and *c* in primary delta-side with 10% $\Delta R/R$ unbalanced resistance in line *a*. Note that due to the difficulty in controlling the tiny air gap of the EE cores in this down-scaled prototype design, more than 15% target unbalance can be handled. When $\Delta R/R$ is higher than 30%, saturation in limb *a* and *c* occurs, where apart from the load current components of the winding currents, the magnetizing currents begin to increase greatly and become distorted, as shown in Fig. 3-13 (b). The current spike locates around 120° due to the 30° phase shift between line voltage and winding current in a delta connection.

To verify the whole scheme, a hybrid scaled down system is implemented in the lab. The configuration is shown in Fig. 3-14. The ac line is 105 V with two zigzag transformers (rated at 70V) in series at the sending end and one zigzag transformer with the only secondary side at the receiving end. A 0.5 mH ac three phase inductance is used to emulate the ac line and 20 Ω resistances as the load. Two back to back (BTB) VSC converters instead of LCCs are used to

emulate HVDC due to its simplicity and availability in the lab. The converter side ac voltage is around 80V and dc voltage is controlled to be 150V, with dc current controlled to be 12A.

The hardware prototypes are shown in Fig. 3-15 and Fig. 3-16. Fig. 3-17 shows the original ac line without and with dc power injection. Ac phase current in line A is around 3A, the phase voltage is around 60V and only small ac magnetic current flows into the receiving end zigzag windings. It can be observed that after dc power injection, the phase voltage v_a is shifted 150V above, and phase current i_a has 4A dc bias distributed from total 12A dc link current. Then this dc current component flows back into dc terminal through the receiving end zigzag windings.

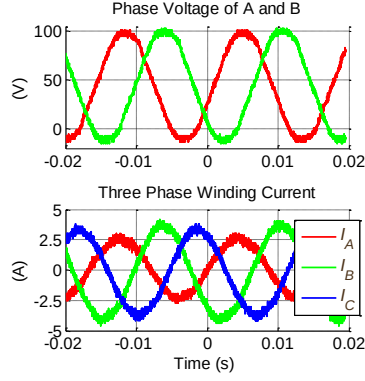
3.4 Active hybrid line impedance conditioner (HLIC) for saturation mitigation

3.4.1 HLIC concept and topology

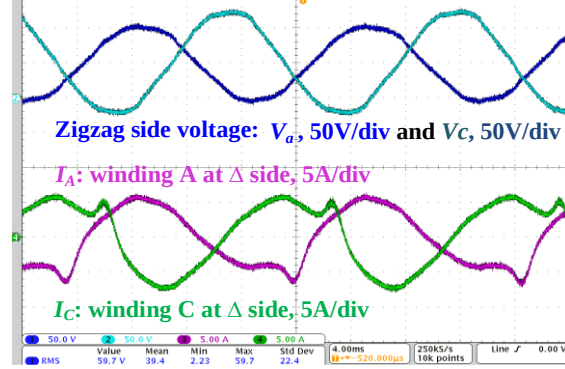
The dc tolerant transformer design is to account for the possible unbalanced lines with dedicated dc flux density margin. However, due to the physical constraint of the magnetic core, ac flux density is reduced, resulting in low utilization of the magnetic core, more winding turns and high cost. Consequently, the cost of a hybrid scheme becomes a strong function of the unbalance, making the hybrid ac/dc transmission scheme less attractive.

To avoid possible saturation of the zigzag transformer without over design, the line impedance unbalances must be mitigated. One possible solution is power converter based line impedance regulator. The existing work has been mainly on ac systems using flexible ac transmission system as reviewed in Section 2.1.2. All these solutions involve high voltage power electronics converters with relatively high cost.

Different from ac systems, line resistance becomes the key element that determines the dc power flow. Following the similar principles as in ac systems, several types of dc line resistance



(a) Winding current at delta-side with 10% $\Delta R/R$.



(b) Winding current at delta-side with 30% $\Delta R/R$.

Fig. 3-13. Test results of zigzag transformer under different line unbalance.

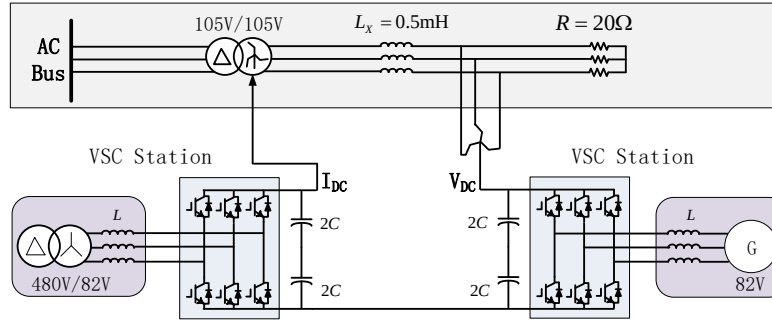


Fig. 3-14. Schematic of the scaled-down hybrid system.

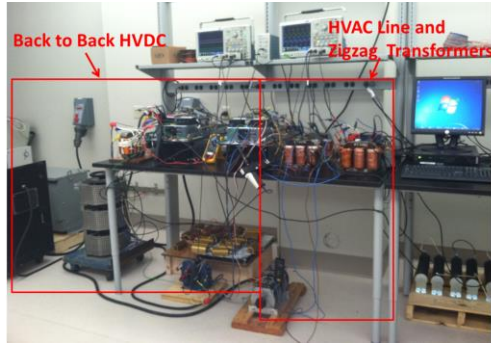
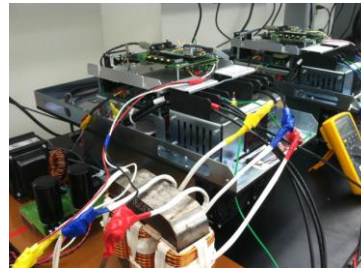


Fig. 3-15. Photo of the scaled-down hybrid system in the lab.



(a) scaled-down BTB HVDC



(b) Two Zigzag Transformers in series

Fig. 3-16. Photo of the scaled down main components.

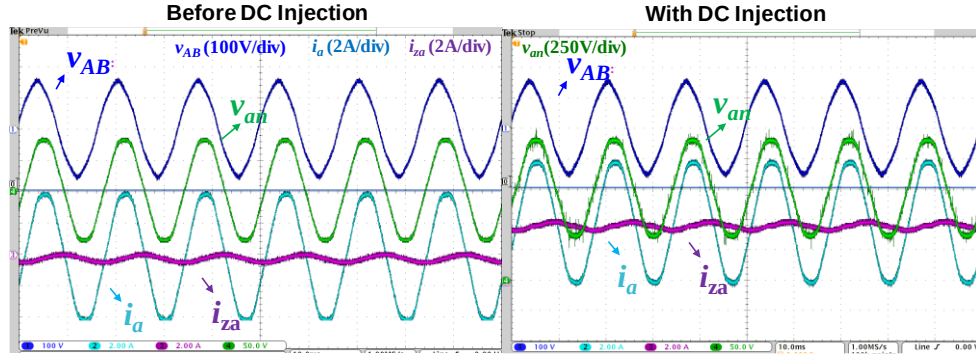


Fig. 3-17. Experimental waveforms of voltage and current with dc injection in the hybrid ac/dc line.

controllers were also proposed recently for dc systems [295, 296], including a dc-dc transformer, switched resistance network and dc voltage insertion. Like FACTS devices, these dc resistance regulators also involve power converters at high voltage. Furthermore, none of these active solutions are feasible in hybrid ac/dc systems, where the terminal voltage and current contain both dc and ac components. The switched resistance network is an exception. However, its high loss is usually not acceptable. A converter with the capability of interfacing with ac/dc simultaneously is thus required.

Three important issues need to be considered in hybrid ac/dc cases: 1) active resistance regulation, 2) low additional cost, and 3) easy implementation.

Since the zigzag transformer saturation results from uneven current distribution due to a small line resistance unbalance, the proposed scheme is to regulate the line resistance balance without impacting ac flux. Since only a small portion of line resistance needs to be compensated, an active resistance approach is more efficient and controllable. The concept is similar to a resistance-based dc power flow controller. Fig. 3-18 depicts the basic HLIC concept, where an equivalent R_X is achieved to compensate for the line unbalance by inserting a dc-current-based dc voltage source in series with the line.

The hybrid ac/dc makes the active resistance regulation different from a pure dc case. In the hybrid system, the ac voltage and current are level-shifted with dc bias. The resistance regulator must allow current and voltage in a hybrid ac/dc form. Conventional three-phase converters cannot support a hybrid voltage or current on the ac side. Direct insertion of three-phase devices into the hybrid lines also requires costly high voltage line-to-line insulation. On the other hand, the single-phase topologies such as the single-phase full-bridge (FB) converter can overcome the issues, which is adopted in this paper. Used as a buck converter, FB can be controlled as a dc/ac inverter to realize an ac voltage, and as a dc/dc converter to realize a dc voltage. Together, as shown in Fig. 3-19, a hybrid ac/dc voltage can be achieved. Besides, FB is selected over other topologies such as half-bridge topology also for higher dc voltage utilization and its voltage bi-directionality, required for the hybrid case.

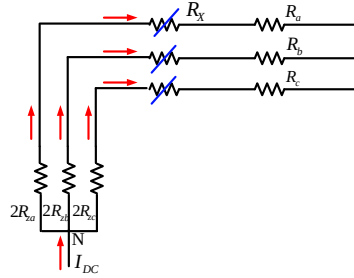


Fig. 3-18. The concept of line resistance compensation through adjustable HLIC active devices.

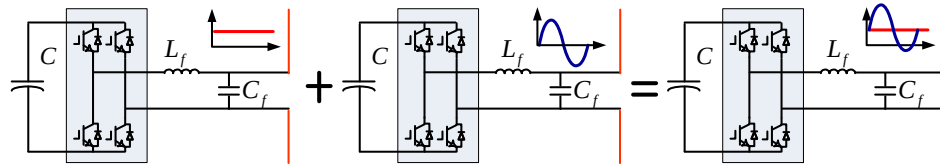


Fig. 3-19. Derivation of hybrid ac/dc voltage controllability for FB.

Based on the FB converter, the proposed topology of HLIC and its integration with a zigzag transformer as an improved dc injection link is shown in Fig. 3-20. Subsequently, the whole hybrid ac/dc transmission system after integrating three HLIC phase units is depicted in

Fig. 3-21. Each HLIC is a phase based unit, consisting of a single phase back-to-back FB converter. The FB at the zigzag transformer side is operated as a rectifier to maintain the dc-link voltage, and the hybrid line side FB is operated as a line impedance conditioner. Note that although a third winding needs to be added to the zigzag transformer secondary side, the winding will need only a small number of turns to provide low-level ac voltage needed for the HLIC rectifier. With the FB topology, HLIC can accommodate bidirectional power flow. When an equivalent positive resistance is needed, the power is absorbed back into the ac grid through the zigzag transformer; while as a negative resistance, the power is drawn from ac grid to the hybrid transmission line. The power loss in the HLIC is negligibly small in terms of the line or transformer rating, considering the low converter rating and high converter efficiency.

In principle, only two of the three lines need to have HLIC installed to regulate the line resistance unbalance, even if all three lines are unbalanced. The median line resistance can be used as the reference, and the other two line resistances can be regulated equally to the reference value. Bypass mode can also be realized. For example, if the phase *a* HLIC unit is not required, the zigzag transformer side rectifier for phase *a* can be blocked, while the hybrid line side converter can turn on two upper or lower switches to create a bypass path, as depicted in Fig. 3-22.

With the functionality of impedance conditioning, the design of the zigzag transformer no longer needs to consider margin for saturation as in [11]. Though a small extra winding in each phase is required to provide the ac voltage for conditioner units, its voltage rating is only a small percentage of the system voltage. For example, for compensating for 5% resistance unbalance, only 0.7 % voltage rating is needed, corresponding to 2 kV for a 280 kV ac and 180 kV dc hybrid line. It means the extra secondary winding turns of the zigzag transformer should be only 1% of the other two winding turns, as shown in Table 3-2 of Section 3.6.1.

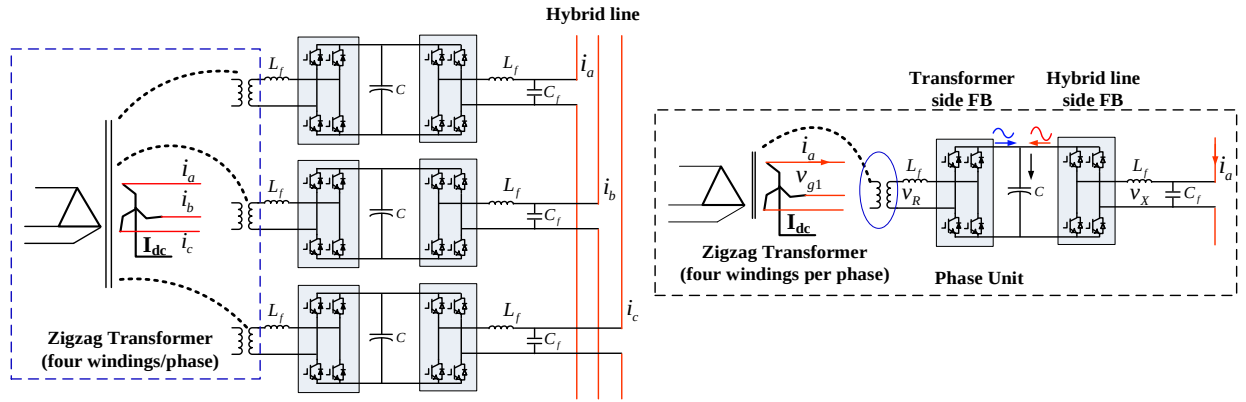


Fig. 3-20. HLIC based dc injection link and HLIC phase unit.

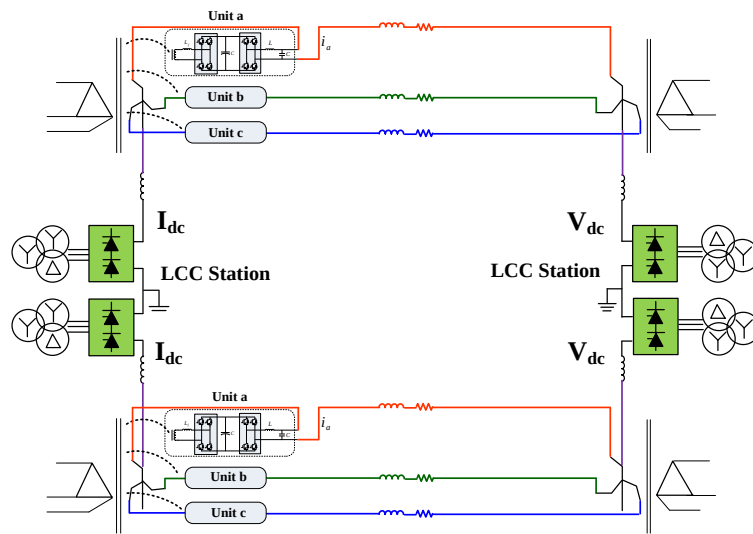


Fig. 3-21. Simplified schematic of the hybrid ac/dc system with HLIC.

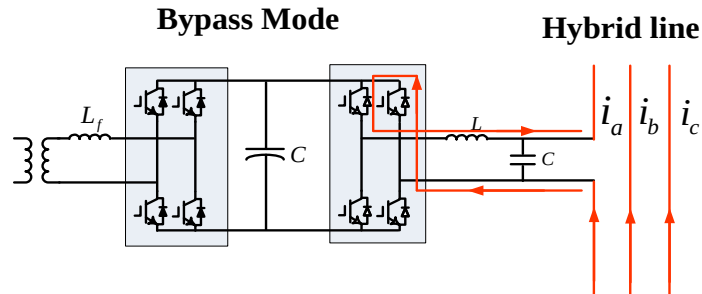


Fig. 3-22. Bypass mode of HLIC.

3.4.2 Operation and control strategy

In the hybrid system, only one set of HLIC bridges is needed to compensate the line unbalance in each phase, e.g. installed at the sending end. The rectifier and the resistance conditioner play different roles and therefore are independently controlled. Each controller adopts a two-level control strategy, as shown in Fig. 3-23.

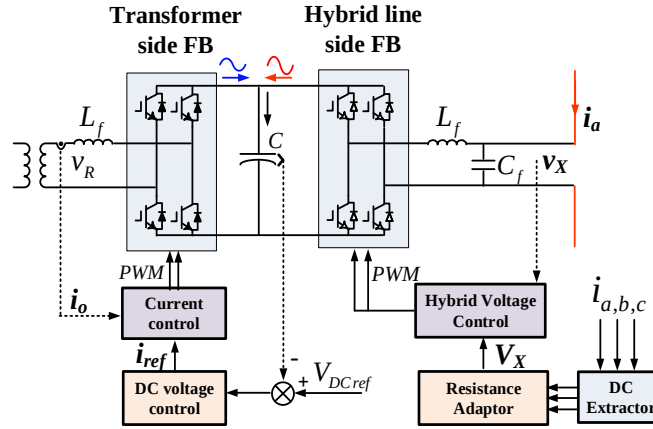


Fig. 3-23. Control scheme of the proposed HLIC. (left FB: HLIC rectifier, right FB: HLIC inverter)

Being connected in series with the hybrid line, the control target of HLIC is to regulate its terminal voltage v_x in phase with the hybrid line current i_x , by setting the voltage loop reference V_x to be the product of the sensed instantaneous line current i_x and the desired unbalance resistance, as shown in (8). Consequently, adopting HLIC inverter control, v_x will be inherently synchronized with the hybrid line current, instead of the receiving end ac grid.

On the other hand, the HLIC rectifier has to be synchronized with the ac grid voltage at the sending end by using a single-phase PLL control, to ensure unity power factor. This synchronized ac voltage comes from the fourth winding of the sending end zigzag transformer, as circled in Fig. 3-20.

The detailed control schemes are presented as below.

3.4.2.1 Resistance Estimator

The two-level control for the line-side conditioner includes the outer-level resistance estimator and an inner-level hybrid voltage controller. The resistance estimator is used to determine online the crucial information of line unbalances. In practice, real-time measurement of resistance unbalance would be difficult. A more practical way can be online estimation through an adaptive procedure. The proposed steps are:

Step 1: Extract dc components of all three lines from measured line currents by removing 50 or 60 Hz fundamental ac currents using a notch filter at 60 Hz.

Step 2: Bypass the HLIC unit in one of the three phases, whose dc current has the median value, e.g. phase *b*, or control this HLIC as zero resistance or zero voltage.

Step 3: Compare the other two-phase dc currents i_{a_DC} , i_{c_DC} with the median current i_{b_DC} to obtain the desired differential resistance R_X respectively, through the procedure shown in Fig. 3-24. For simplification, only phase *a* controller is illustrated, and the case for phase *c* is similar.

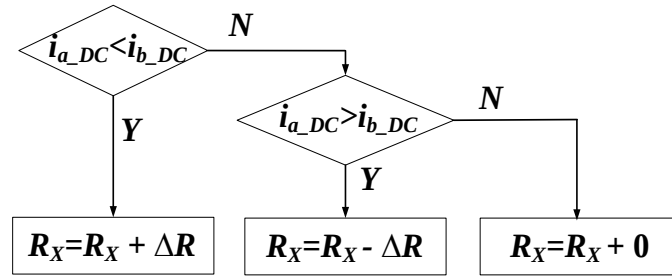


Fig. 3-24. Adaptive estimator of unbalanced line resistance.

Step 4: Calculate the hybrid ac/dc terminal voltage reference V_X for the low-level line impedance conditioner, based on (3-13), where i_X is the hybrid line current.

$$V_X = i_X \cdot R_X \quad (3-13)$$

It should be mentioned that, although the target here is to regulate the unbalanced line resistance as the baseline, HLIC provides a more powerful controllability in transmission systems.

1. It has a flexible architecture to separate the dc and ac impedance control. For example, if only the dc current component is included in the voltage reference, as given in (3-14), the dc resistance will be regulated exclusively and ac impedance inserted by HLIC will be zero. On the other hand, ac resistance or inductive/capacitive impedance can also be realized independently of dc resistance, as given in (3-15).

$$v_X = i_{X_DC} \cdot R_X \quad (3-14)$$

$$v_X = i_{X_DC} \cdot R_X + i_{X_AC} \cdot Z_{AC} \quad (3-15)$$

2. With this capability, HLIC device can be extended to regulate both dc and ac power flow of hybrid transmission lines. For example, independently of dc power flow, it can also control both active and reactive ac power flow similar to a FACTS device.

3.4.2.2 Conditioner Control

This refers to the inner-layer hybrid voltage control on the HLIC inverter side. To control the insertion voltage at LC filter terminal of HLIC, it is necessary to know the external circuit characteristics, e.g. equivalent impedance, to correctly model the control transfer function, since HLIC is in series with the hybrid line. Fortunately, both the ac and dc currents on the hybrid lines are determined by the system. As a result, the load for HLIC can be regarded as a current source with high impedance at dc and low frequencies. Subsequently, the external circuit of HLIC can be approximately modeled as an open circuit in this frequency range. Following this analysis, the control plant can be simplified as an H bridge converter with a LC filter, as illustrated in Fig. 3-25. Thus, the feedback control design of HLIC no longer depends on the external system parameters, if designed with a relatively low frequency bandwidth.

$$G_{vd}(s) = \frac{v_X}{d} = \frac{V_{DC}}{s^2 L_f C_f + 1} \quad (11)$$

Feedback control can regulate the HLIC output voltage precisely, with proportional-integral (PI) control targeting the dc voltage component, and proportional-resonant (PR) controller eliminating the fundamental ac voltage error. The control bandwidth is limited, partly to match the low frequency model validity range mentioned above, and partly because of the low phase margin in a second-order system due to the LC filter. To increase the potential control dynamics, a control combining feedback in (3-16) ~ (3-17) and feedforward control is adopted, as illustrated in Fig. 3-26.

$$G_{PI}(s) = k_p + \frac{k_i}{s} \quad (3-16)$$

$$G_{PR}(s) = 1 + \frac{2k_{th}\omega_{ch}}{s^2 + 2\omega_{ch}s + \omega_h^2} \quad (3-17)$$

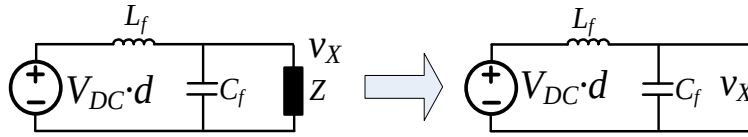


Fig. 3-25. Simplified conditioner control model in HLIC.

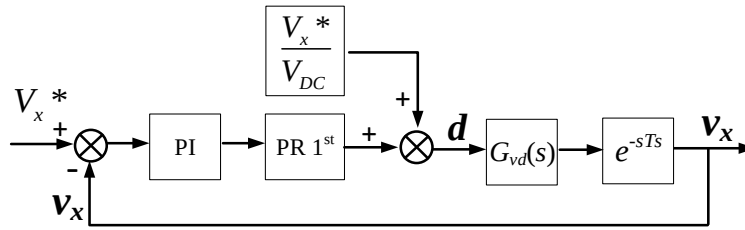


Fig. 3-26. Control diagram of single-phase conditioner in HLIC.

where ω_{ch} denotes the bandwidth of the resonance control and the resonance frequency ω_h is located at 60 Hz, and k_{th} determines the resonance gain.

The closed-loop bode plots of a scale-down conditioner prototype are provided in Fig. 3-27, illustrating the accuracy and dynamics of different control approaches. Clearly, the combined

feedback and feedforward control have the optimal performance in terms of both accuracy and dynamics.

It should also be pointed out that although the target in this context, as discussed in section III-B, is to regulate the unbalanced line resistance in terms of both ac and dc forms, it is also feasible to only control the dc resistance for saturation suppression, following the command voltage in (3-14). In that case, the PR controller can be removed to further simplify the control structure.

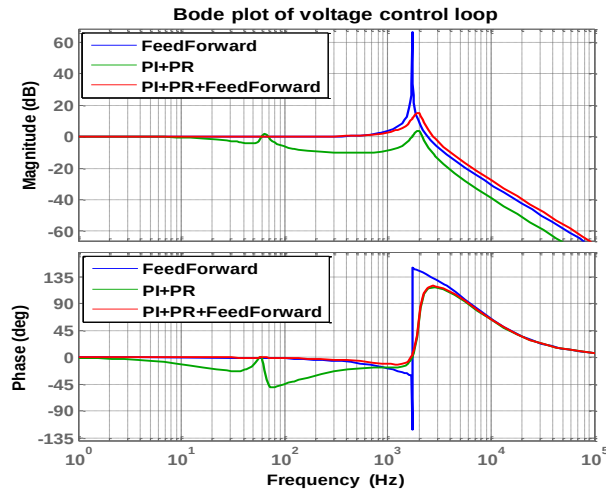


Fig. 3-27. Bode plots of three different controllers for HLIC.

3.4.2.3 Rectifier Control

Fig. 3-28 depicts the proposed control scheme for the rectifier to maintain the dc-link voltage with unity power factor. In addition to the second-order ripple power, there is also fundamental ripple in the dc-link voltage of FB, penetrating from the conditioner ac side, which will be discussed in detail later. To prevent the ripple signal from the outer dc voltage loop into the inner current loop, two series second-order notch filters with resonant frequencies at 60 Hz and 120 Hz are introduced.

A high current control loop gain should be provided in the low frequency range to avoid dc current into the ac zigzag transformer, which may be induced by the fundamental ripple power penetrating from the dc-link. Thus, a quasi-PR controller together with a PI controller is applied in the rectifier inner current control, to improve the fundamental current tracking, and to eliminate the potential dc current component respectively.

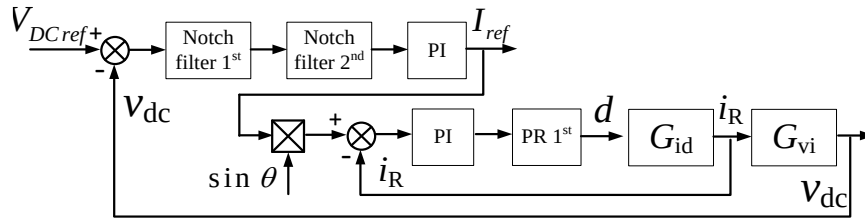


Fig. 3-28. Control diagram of single-phase rectifier in HLIC.

3.4.2.4 Discussion on Impacts from Unbanked Ac Current

Though the focus of this paper is on avoiding the dc current saturation of the zigzag transformer via the dc current balance control, it is, however, important to understand the behavior of the hybrid system and HLIC considering the possible ac current unbalance in the hybrid lines.

First, the paths of unbalanced ac current are examined. From the superposition principle, the unbalance ac current can be decomposed into positive, negative and zero sequence current. Contributed by the delta winding of zigzag transformers on both ends, zero sequence current will not penetrate into the source side or the load side and will only circulate between the neutrals of the two zigzag transformers. Additionally, this zero-sequence ac flux will be canceled, due to the reversed polarity of the two zigzag windings per limb, and no saturation will be induced.

Furthermore, according to the analysis in Section 3.2, the saturation of this transformer is mainly caused by two factors. One is the winding ac voltage which determines the ac magnetizing current. This voltage, in the transmission system, is pretty balanced, because of the stringent

standards of voltage unbalance (e.g., voltage unbalance factor is usually below 2% [297]), even though the line current might be more unbalanced. So the voltage unbalance may not cause the saturation of the zigzag transformer. The other factor is the dc magnetizing current introduced by the unevenly distributed dc current as analyzed in Section II. However, with the proposed HLIC solution, this issue can be greatly mitigated.

Finally, from the HLIC point of view, a HLIC is connected in series with each line, and regulates its fundamental terminal voltage to be in phase with the line current. There is no direct interference from the three-line unbalance to the HLIC device. In particular, since the voltage reference of HLIC is determined by the unbalanced resistance and this resistance is estimated based on the unbalanced dc current in the proposed control scheme, the unbalanced ac current will not introduce interference to the dc current balance control. In summary, the dc regulation is independent of the ac current control in the propose HLIC scheme, based on the superposition principle.

3.4.3 Selection of dc-link capacitance

To ensure the normal operation of HLIC, dc-link voltage should be maintained within an acceptable variation range, say $\pm 5\%$. Different from the selection of dc-link capacitance for normal single-phase inverters, the unique hybrid operation introduces multi-frequency power ripples, not only the second-order frequency ripple but also the fundamental frequency ripple on the dc link. Applying the instantaneous power theory for a single-phase unit shown in Fig. 3-23, at the conditioner side, one obtains

$$\begin{aligned} p_{dc_X} &= v_X i_X = \left(\frac{I_{DC}}{3} + \sqrt{2} I_{AC} \sin(\omega t + \varphi_X) \right) \times \beta R_{balance} \left(\frac{I_{DC}}{3} + \sqrt{2} I_{AC} \sin(\omega t + \varphi_X) \right) \\ &= P_{DC} + p_{r1_X} + p_{r2_X} \end{aligned} \quad (3-18)$$

$$\begin{cases} P_{DC} = \left[\left(\frac{I_{DC}}{3} \right)^2 + I_{AC}^2 \right] \beta R_{balance}, \\ p_{r1_X} = \left[\frac{\sqrt{2} I_{DC} I_{AC}}{3} \right] \beta R_{balance} \sin(\omega t + \varphi_X), \\ p_{r2_X} = -I_{AC}^2 \beta R_{balance} \cos(2\omega t + 2\varphi_X) \end{cases} \quad (3-19)$$

where v_X , i_X represent the conditioner side voltage and current; I_{DC} and I_{AC} denote the dc and ac current components of line current respectively; P_{DC} is the average dc power, and p_{r1_X} , p_{r2_X} are the 1st and 2nd order power ripple at the conditioner side.

On the rectifier side, according to power balance, the following equations hold,

$$\begin{aligned} p_{dc_R} &= v_R i_R = P_{DC} [1 - \cos(2\omega t + 2\varphi_R)], \\ p_{r2_R} &= - \left[\left(\frac{I_{DC}}{3} \right)^2 + I_{AC}^2 \right] \beta R_{balance} \cos(2\omega t + 2\varphi_R) \end{aligned} \quad (16)$$

where v_R , i_R stand for the rectifier side voltage/current. φ_X and φ_R are the phase angle at the conditioner side and rectifier side. p_{r2_R} is the 2nd order power ripple at the rectifier side.

According to the law of energy conservation, the hybrid ripple energy E_{r1_X} , E_{r2_X} , and E_{r2_R} are stored in the dc-link capacitor and L filters. L can be determined by the filtering requirement.

Thus, one obtains

$$ripple_of \left\{ \frac{1}{2} C v_{dc}^2 + \frac{1}{2} L_f i_R^2 + \frac{1}{2} L_f i_X^2 \right\} = (E_{r1_X} + E_{r2_X}) - E_{r2_R} \quad (3-20)$$

where v_{dc} is the dc link voltage with the voltage ripple Δv_{dc} .

Its derivative becomes

$$C v_{dc} \frac{dv_{dc}}{dt} + L_f i_R \frac{di_R}{dt} + L_f i_X \frac{di_X}{dt} = p_{r1_X} + p_{r2_X} - p_{r2_R} \quad (3-21)$$

Assuming $v_{dc} = V_{DC} + \Delta v_{dc}$, since Δv_{dc} mainly contains 1st and 2nd order ripples, one can

further simplify (3-21) by removing the dc bias components,

$$C v_{dc} \frac{d\Delta v_{dc}}{dt} + L_f i_R \frac{di_R}{dt} + L_f i_X \frac{di_{X_ac}}{dt} = p_{r1_X} + p_{r2_X} - p_{r2_R} \quad (3-22)$$

if defining the current ratio of the hybrid line as

$$\lambda_I = I_{DC} / 3 / \sqrt{2} I_{AC} \quad (3-23)$$

If v_{dc} is approximately simplified as constant V_{dc} , the voltage ripple can be solved as

$$\begin{aligned} \Delta v_{dc} = & \frac{\beta I_{AC}^2 R_{balance}}{\omega C V_{dc}} \left\{ -2\lambda_I \cos(\omega t + \varphi_X) - \frac{1}{2} \sin(2\omega t + 2\varphi_X) + \frac{(1+2\lambda_I^2)}{2} \sin(2\omega t + 2\varphi_R) \right\} \\ & - \frac{L_f I_{AC}^2}{C V_{dc}} \left\{ - \left(\frac{(1+2\lambda_I^2) \beta I_{AC} R_{balance}}{V_R} \right)^2 \frac{\cos(2\omega t + 2\varphi_R)}{2} + 2\lambda_I \sin(\omega t + \varphi_X) - \frac{1}{2} \cos(2\omega t + 2\varphi_X) \right\} \end{aligned} \quad (3-24)$$

where the first term is the ripple energy exchanging between two converters and the second term is the impact from filter inductors. The impact of the filter capacitor is ignored considering its low capacitance.

If $|\Delta v_{dc}| \leq 5\% V_{DC}$, the desired capacitance for a given ripple can be expressed in two terms with regards to the two above factors

$$C \geq \max \{ |C_0(t) + C_L(t)| \} \quad (3-25)$$

Where

$$C_0(t) = \frac{\beta I_{AC}^2 R_{balance}}{5\% \omega V_{DC} V_{DC_min}} \left(\begin{aligned} & -2\lambda_I \cos(\omega t + \varphi_X) - \frac{1}{2} \sin(2\omega t + 2\varphi_X) \\ & + \frac{(1+2\lambda_I^2)}{2} \sin(2\omega t + 2\varphi_R) \end{aligned} \right) \quad (3-26)$$

$$C_L(t) = - \frac{L_f I_{AC}^2}{5\% V_{DC} V_{DC_min}} \left(\begin{aligned} & - \left(\frac{(1+2\lambda_I^2) \beta I_{AC} R_{balance}}{V_R} \right)^2 \frac{\cos(2\omega t + 2\varphi_R)}{2} \\ & + 2\lambda_I \sin(\omega t + \varphi_X) - \frac{1}{2} \cos(2\omega t + 2\varphi_X) \end{aligned} \right) \quad (3-27)$$

and V_{DC_min} is the dc-link valley voltage to satisfy the ripple requirement in the worst case.

Now the phasor relationship between the two ends of the transmission line shown in Fig. 3-29 can be applied. Since the conditioner is controlled as a resistance, thus φ_X is equal to the load angle θ of the receiving end. For the zigzag transformer shown in Fig. 3-20, the fourth winding voltage v_R is in line with the primary side voltage, and ahead of the secondary phase voltage V_{g1} by 30 degrees. Thus, the following angle relationship holds,

$$\varphi_R = \angle V_{g1} + \frac{\pi}{6} = \delta + \frac{\pi}{6} \quad (3-28)$$

where δ is power angle.

From above, the current ratio has a considerable impact on dc-link voltage ripple and selection of dc capacitance. This can be clearly seen in Fig. 3-30 and Fig. 3-31, based on a sample case as given in Table 3-2, if neglecting the L_f term. On the other hand, this impact provides another metric from hardware design aspect for the final selection of hybrid ac/dc current ratio, a key system parameter.

One can also notice that ac side filters do contribute some ripple energy, hence leading to a determination factor for the capacitor selection.

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Fig. 3-29. One-line diagram of phasor relationship in a two-area transmission system.

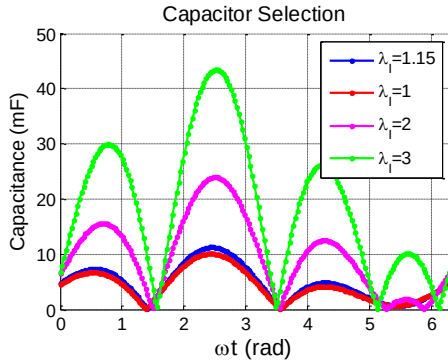


Fig. 3-30. Capacitance selection as a function of hybrid current ratio.

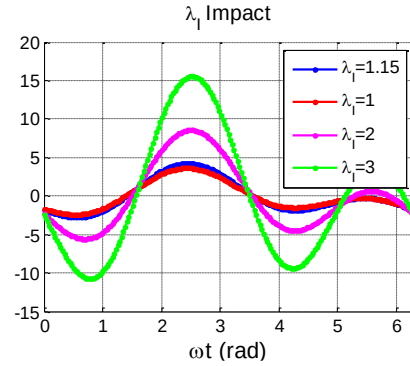


Fig. 3-31. Impact of current ratio on the first term of (3-25).

3.4.4 Implementation considerations

3.4.4.1 Installation

In a bipolar hybrid ac/dc system with double-circuit ac lines, only two sets of HLIC devices are needed for each pole and each set of HLIC only requires two phase units. Although the current

rating of the HLIC is the same as the hybrid line current, its dc voltage rating is much smaller than that of the HVDC converter or the transmission line voltage, since the injected voltage generated by HLIC is only used to compensate the voltage caused by the differential term of the unbalanced line resistance. And due to the low transmission line impedance, the voltage drop of the whole line in a typical ac system is quite low, if compared with the transmission line voltage. As shown in Table I for the sample system, HLIC converter voltage rating is only around 1.6% of the HVDC voltage rating for the simulated system. And its current rating is 1.17 times of the HVDC current. So, its power rating and size are less than 2% of the HVDC converter and power loss would be less than $2\% \times (1-98\%)$ of the HVDC power if assuming its power efficiency is 98%. Therefore, the size of HLIC is much smaller than that of the zigzag transformer.

A possible installation is to integrate this device into the zigzag transformer. Each phase unit can be mounted to the corresponding pole of the high power zigzag transformer, so no further insulation infrastructures are needed. The only inter-phase information for the purpose of line unbalance estimation in each HLIC is the phase dc current, which can be transmitted by local fiber-optic wires or local wireless communication. An alternative is a distributed modular design and installation. In that case, HLIC modules can be clamped to towers or utility poles.

3.4.4.2 Protection under external line faults

External line faults are also considered in this paper. If line to ground fault occurs, different from traditional ac grids, the fault current will have both ac and dc components. Since the zero crossing may not exist depending on the operation point and fault impedances, an ac breaker may not work in the hybrid system. A protection scheme is thus proposed: 1) HLIC operates into bypass mode once the fault is quickly detected; 2) external bypass thyristors (if equipped in HLIC) are turned on; 3) LCC-HVDC controls the dc current to zero and during this period, the ac breaker

detects the zero-crossing instant and trips the line. For line-line fault, no dc fault occurs since three lines stay at the same potential.

A simulation of single line-to-ground (SLG) fault on the hybrid lines has been conducted including HLIC in the fault path, with nominal dc current 500 A, voltage 180 kV and ac peak current 500 A, line voltage 280 kV in a 12-pulse LCC-HVDC based hybrid system. The line unbalance is assumed to be 10 %. Fig. 3-32 shows the line voltage and current during the fault transition occurring at $t = 0.11$ s. The dc component measurements of the three-phase current are also shown in Fig. 3-33, extracted through a notch filter designed at 60 Hz. Though a higher peak current is observed in phase a, the main contributor is ac fault itself. This can be explained from the waveforms of the LCC rectifier as shown in Fig. 3-34. After $t=0.11$ s, the dc fault current starts dropping, thanks to the voltage-dependent current order limit (VDCOL) function implemented in LCC-HVDC control, which regulates the current reference to 0.3 pu once it detects dc link voltage drops below 0.6 pu. In the end, the firing angle increases up to 100 degrees to pull off the energy stored in the line. In addition, since the dc reactor is on the ac fault path, ac fault current can also be reduced. As a result, the zero crossing can be ensured, hence the faulty line can be tripped safely and timely within several line cycles.

As for HLIC, its balance regulation takes action at $t=0.8$ s as shown in Fig. 3-32. When the fault current goes beyond the current protection threshold, HLIC bypass mode is activated as shown in Fig. 3-33. One should notice that the ac line fault current is tightly dependent on the system impedance and fault location. In this study, the fault location is at the sending end terminal, leading to the highest current. According to the simulation results, IGBT with 1.5 pu nominal current rating should be selected and it should be reasonable in real applications.

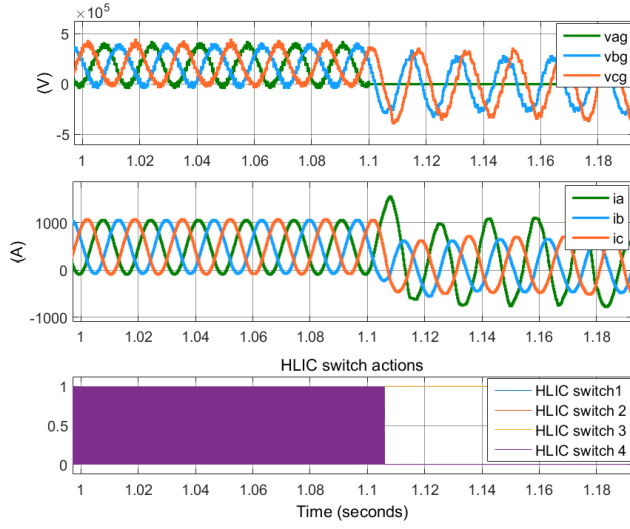


Fig. 3-32. Voltage and current in hybrid ac/dc lines under SLG fault.

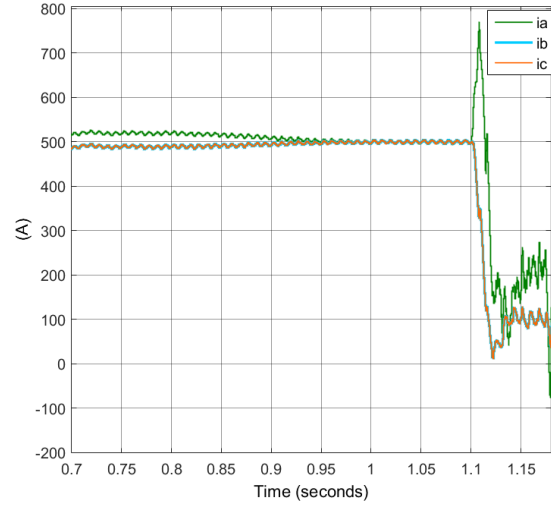


Fig. 3-33. Extracted dc current components of three lines.

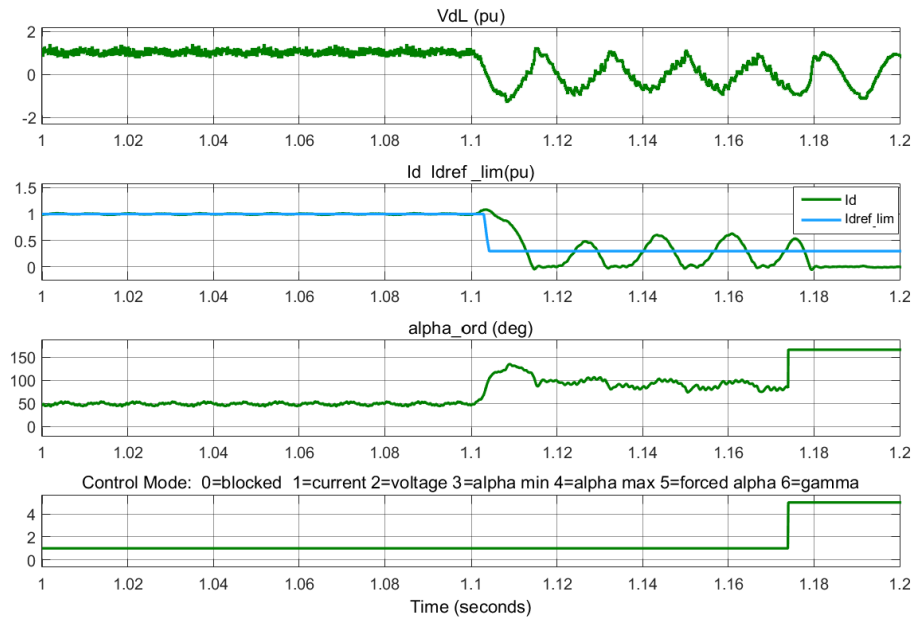


Fig. 3-34. Waveforms of LCC rectifier under SLG fault in the hybrid ac/dc system.

Another possible solution is to parallel thyristors and MOV as illustrated in Fig. 3-35, which forms a bidirectional bypass path once a fault occurs.

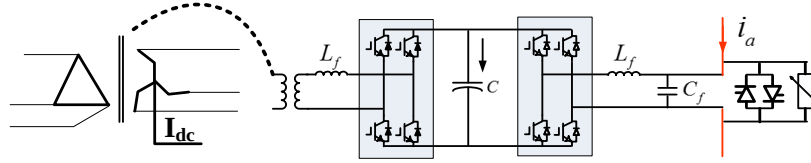


Fig. 3-35. An alternative protection bypass switch for HLIC.

3.5 Feasibility of hybrid ac/dc system

3.5.1 Architecture evaluation

Featuring N-1 reliability, a bipolar configuration in Fig. 3-36 and Fig. 3-37, shows more advantages over the monopole structure and it can also exploit the existing double ac circuits.

To implement it, three types of HVDC architectures can be adopted: LCC, VSC, and MMC. Generally, LCC has the advantage of much higher power rating and lower cost which is more suitable for bulk power application, while it needs almost 50% reactive power compensation and strong grid support in case of commutation failure of thyristors as well as bulk volume. In contrast, VSC has independent switching capability with both active and reactive power controllability and less space occupation but more cost [6, 9]. To have a fair comparison here for high power long line transmission applications, specific needs should be considered: a) hybrid ac/dc transmissions use the overhead line, which is vulnerable to ground faults especially SLG fault; b) high power transmission cares more about loss and cost, while station space may not be the priority.

For converter loss, LCC is around 0.7% switching loss, VSC is about 1.7%, and half bridge MMC (HB-MMC) is close to 1% [7, 10]. For station cost, LCC is also much lower than IGBT based VSC and MMC.

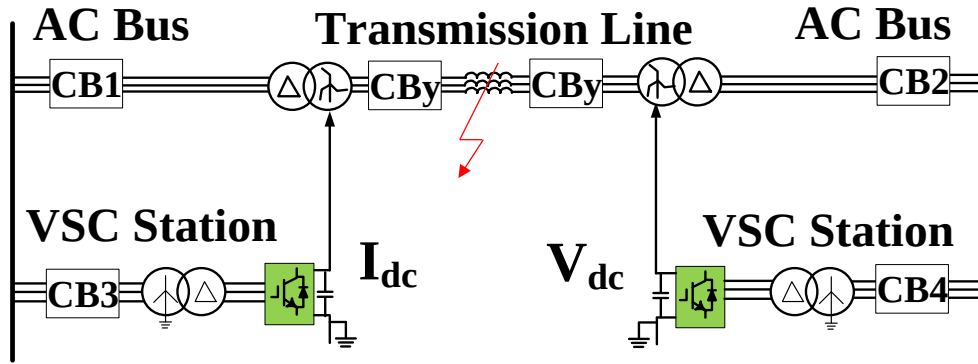


Fig. 3-36. Bipolar configuration of LCC based hybrid ac/dc system (half).

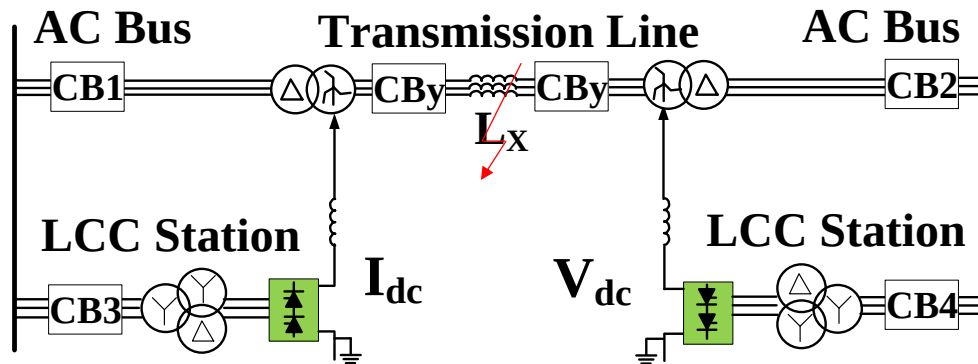


Fig. 3-37. Bipolar configuration of VSC based hybrid ac/dc system (half).

In terms of fault, since the hybrid system shares the same AC lines, both ac and dc fault will occur. As well known, the state of art of VSC and HB-MMC has no dc fault blocking ability. This is the main reason that most VSC-HVDC projects are only commissioned for submarine cable scenarios instead of overhead lines. Although emerging double-clamped HB-MMC (DHB-MMC) has fault blocking capability, its loss is still fairly high. Whereas, LCC in nature is a buck type converter which can directly control dc current, and dc short only behaves as a dramatic load variation. Although there is still certain dc current overshoot during fault with conventional PI control, further efforts can be made to enhance control dynamics with the aid of feedforward control to reduce this overshoot current. To compare the fault performance of two types of topologies, simulations are carried respectively for 12-pulse LCC and VSC based hybrid ac/dc both under phase A ground fault of the transmission line. The key parameters are shown in Table 3-1.

One should notice that for the hybrid system, both ac and dc fault current will flow through the faulty line. Fig. 3-38 shows the simulation results of LCC based system under line-ground fault. There is very small overshoot current at the fault transient $t=0.7s$. In addition, because of the extra dc inductance in the fault loop, ac fault current component is also reduced. Fig. 3-39 shows the fault performance of VSC based system. When a fault occurs at $t=0.2s$, dc fault current cannot be blocked, due to the rectifier process fed from ac grid. Thus, a dc breaker is needed for fast protection. Based on the comparison above, LCC is a better choice currently.

3.5.2 Cost comparison with passive design method

To clearly demonstrate the improvement by using HLIC solution compared to the passive dc tolerant design [67], a cost comparison methodology is provided.

Table 3-1. System parameters.

Descriptions	Values
Ac voltage	115kV/280kV
Line impedance	$0.035\Omega+j0.93$ mH/km
Length	450km
Dc voltage	180kV
Dc current	1kA

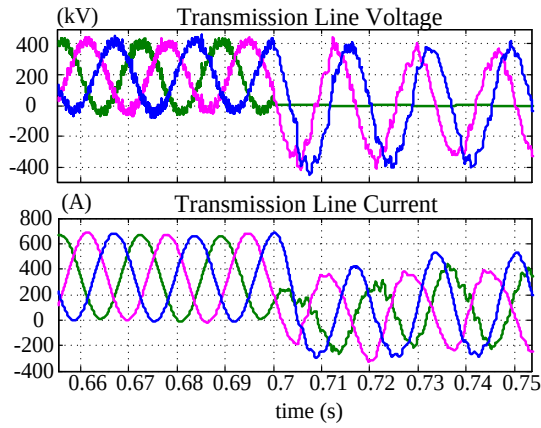


Fig. 3-38. Waveforms of LCC based hybrid line under a SLG fault.

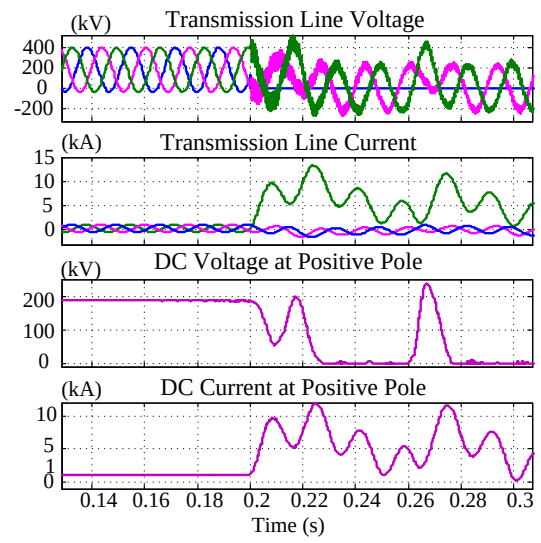


Fig. 3-39. Waveforms of VSC based hybrid line under a SLG fault.

First, the per kw cost is calculated. A typical average cost breakdown of a LCC HVDC system and the unit cost of its component are found in the literature [298-300]. To simplify the comparison, the per kW cost of the HLIC converter is assumed to be the same as that of the LCC HVDC station including the installation and control expense.

Since the zigzag transformer is not widely used and especially when it is designed to inject dc current in the hybrid system with the passive design method, its cost is not available and thus will be derived from the traditional two-winding transformer. The idea is to normalize the zigzag transformer cost to the ac transformer cost based on the ratio of its hybrid ac/dc current I_{RMS} to its ac current component I_{AC} as shown in Fig. 3-40 and equation (3-29). Three cost-impact factors are considered, i.e., voltage rating, current rating and winding turn number (in the dc tolerate design case), and their relations to the ac power are derived in (3-29).

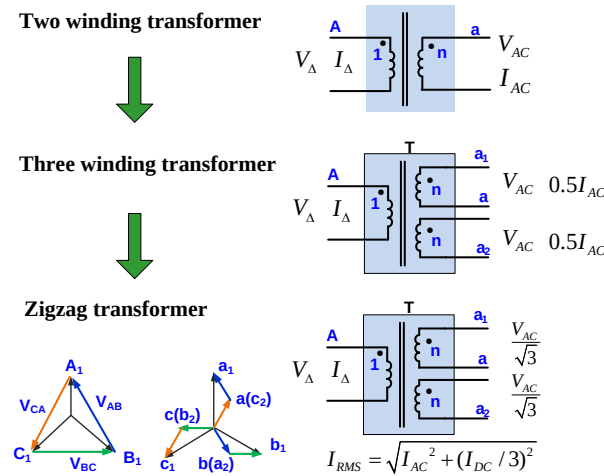


Fig. 3-40. Derivation of zigzag transformer cost.

$$k_v = \frac{1}{\sqrt{3}} \quad k_I = \frac{I_{RMS}}{0.5I_{AC}} \quad K_N = \frac{1}{K_{Bac}} = \frac{B_{AC} + B_{DC}}{B_{AC}} \quad (3-29)$$

The final per unit cost of zigzag transformer projected to that of an ac transformer is expressed

as

$$C_{U_zigzag} = C_{U_ac_trans} (0.5 + 0.5K_V K_I) K_N \quad (3-30)$$

Then, the power capacity ratio of hybrid ac/dc to the original HVAC system can be derived

as,

$$\frac{P_{AC} + P_{DC}}{P_{HVAC}} = (1 + \frac{2\lambda_V \lambda_I}{\cos \varphi}) \frac{\sin \delta_1}{(1 + \lambda_V)^2 \sin \delta_0} \quad (3-31)$$

where λ_V and λ_I are the dc voltage and current ratio of a hybrid line, respectively.

$$\lambda_V = \frac{V_{DC}}{\sqrt{2}V_{AC}} \quad \lambda_I = \frac{I_{DC}/3}{\sqrt{2}I_{AC}} \quad (3-32)$$

δ_1 is the power angle in the hybrid ac/dc system, δ_0 is the power angle in the original HVAC system,

φ is the load angle at the receiving end, and P_{AC} and P_{DC} are the ac and injected dc power, respectively in per pole per station of the hybrid system.

Considering the voltage insulation limitation V_P of the original ac line, one can obtain

$$\sqrt{2}V_{AC} + V_{DC} = V_P \quad (3-33)$$

$$P_{DC} = V_{DC} I_{DC} = \frac{3\lambda_V \lambda_I}{(1 + \lambda_V)^2 \cos \varphi} \frac{V_P^2 \sin \delta}{X} = \frac{2\lambda_V \lambda_I}{\cos \varphi} P_{AC} \quad (3-34)$$

The total apparent power VA rating of HLIC needed in per pole per station can be approximately derived as

$$P_{HLIC} = \frac{2\beta(1 + \lambda_I)^2}{m \cos \varphi} k_{line_drop} P_{AC} \quad (3-35)$$

where m is the modulation index of HLIC converters, assuming to be 0.7, and k_{line_drop} denotes the voltage ratio of the HLIC terminal voltage over the hybrid line ac voltage level, assuming to be 1% in this study.

Finally, the cost of the zigzag transformer, designed with both passive method and the active HLIC solution are compared. A case study with $\lambda_V=1$ is provided, where the remaining variables for the cost and power capacity are the line unbalance degree β and current injection ratio λ_I . However, in order to perform the cost - power capacity comparison, λ_I is adopted as the link

variable so that a cost-power capacity Pareto curve can be developed with the required power capacity ratio (28) as the x-axis. It has to be mentioned that since the power capacity has its physical limits due to the thermal rating of the transmission line, a reasonable power capacity enhancement might stay within 200% and varies for different λ_V , λ_I , and system parameters.

Fig. 3-41 shows the unit cost ratio - power capacity Pareto curve of zigzag transformer vs. LCC HVDC converter station, and Fig. 3-42 shows the cost ratio - power capacity Pareto curve of the zigzag transformer in the hybrid ac/dc system.

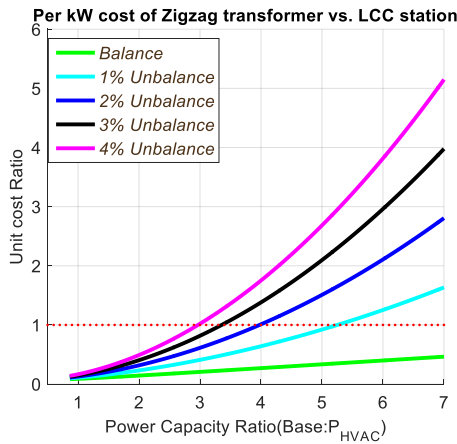


Fig. 3-41. Per kW cost of zigzag transformer vs. LCC HVDC station, with the passive design method.

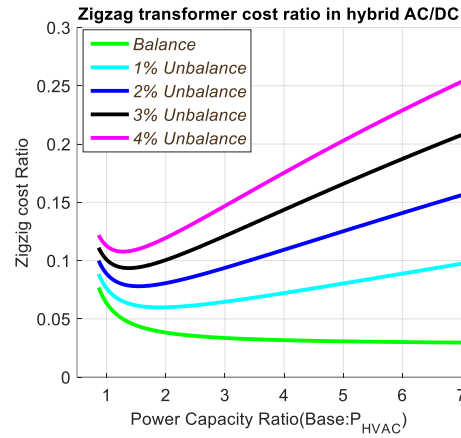


Fig. 3-42. Cost of zigzag transformer vs. hybrid ac/dc system, with the passive design method.

In contrast, using HLIC, zigzag transformer design can be greatly simplified. As shown in Fig. 3-43 its cost is no longer a function of line unbalance and is much less than that in Fig. 3-42.

Moreover, as illustrated in Fig. 3-44, the cost of three-phase HLIC devices in a hybrid ac/dc system is less than 1% in general. Furthermore, as discussed in Section 3.4, two HLICs are already

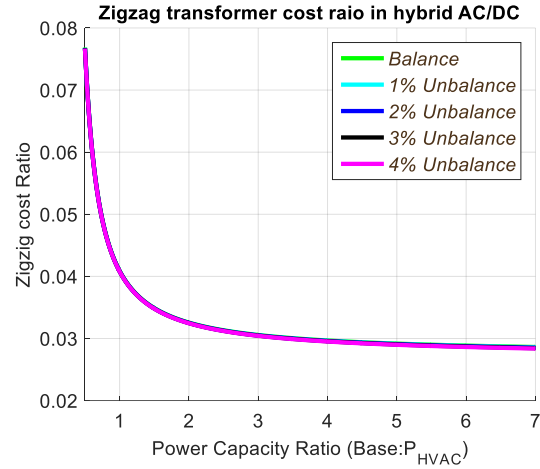
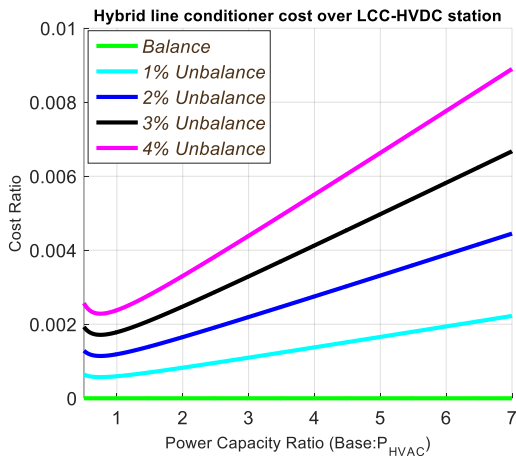
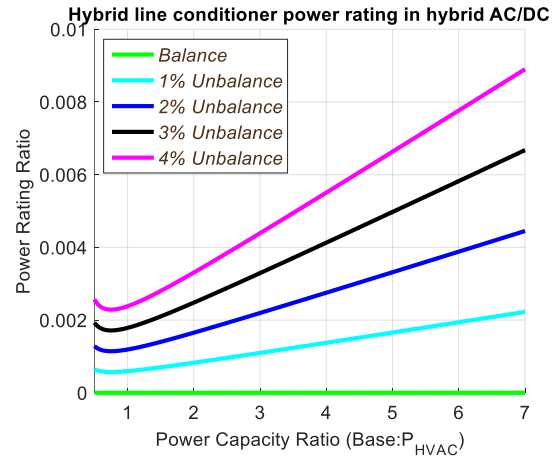


Fig. 3-43. Cost of zigzag transformer vs. hybrid ac/ds system, with the active HLIC solution.



(a) Cost of HLIC vs. LCC HVDC system, with the HLIC solution



(b) Cost of HLIC vs. hybrid ac/ds system, with the HLIC solution

Fig. 3-44. Cost of HLIC vs. LCC HVDC and vs. hybrid ac/dc.

capable of achieving the balance regulation, contributing to a further 1/3 cost reduction. Comparison of hybrid ac/dc and pure HVDC system using existing ac lines

Although there are several concerns on these two systems, e.g. voltage stress, insulation, line thermal margin, environment effect and etc., this work will only compare from the investment aspect, i.e., the converter station cost for a given power capacity target.

For both systems, the line construction cost is not accounted because of the existing line utilization. And in the hybrid ac/dc system with partial power from ac, its HVDC converter rating and cost would be lower, whereas, in the pure HVDC system, all power flows through the dc station, leading to a higher cost. On the other hand, in the hybrid system, the extra cost will be introduced by the zigzag transformer and HLIC devices. For simplicity, the cost of HLIC is neglected in this study due to its small portion of the whole system as illustrated in Fig. 30. Noticing the unit cost of the zigzag transformer has been normalized through the power scaling from the total hybrid ac/dc power to its ac power component as in (27), the total cost of the two systems are

$$C_{Hybrid} = C_{U_LCC} P_{DC} + C_{U_zigzag} P_{AC} \quad (3-36)$$

$$C_{HVDC} = C_{U_LCC} (P_{AC} + P_{DC}) \quad (3-37)$$

This leads to

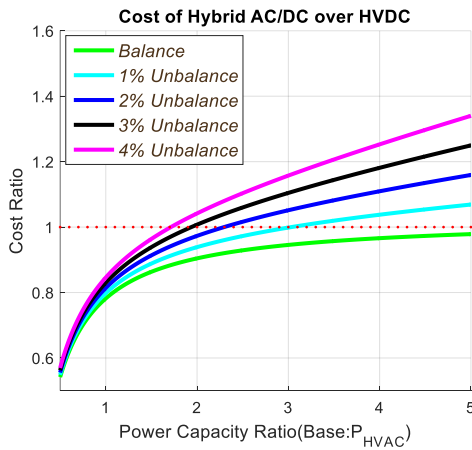
$$C_{Hybrid} \leq C_{HVDC} \Leftrightarrow C_{U_zigzag} \leq C_{U_LCC} \quad (3-38)$$

where C_{Hybrid} and C_{HVDC} are the converter station cost, and C_{U_LCC} and C_{U_zigzag} denote the per unit cost, respectively.

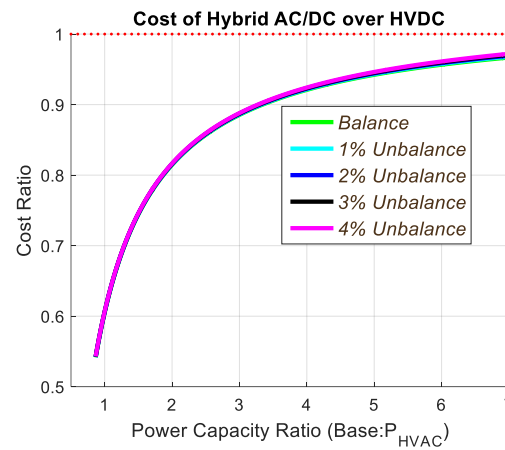
As indicated from (3-36) to (3-38), the cost ratio of the hybrid and pure HVDC systems is actually determined by the unit cost of a zigzag transformer and a LCC station. Hence, the cost of the zigzag transformer is very critical, which further highlights the importance of the HLIC approach.

With the above cost comparison methodology described above, a case study on cost comparison is carried out, assuming a dc voltage injection ratio of 1.

As demonstrated in Fig. 3-45 (a), with the passive design method, this hybrid scheme has limited beneficial range compared to pure HVDC scheme. In contrast, thanks to the HLIC, the zigzag transformer cost can be greatly reduced as given in Fig. 3-43, contributing to a hybrid ac/dc system that has much lower cost given in in Fig. 3-45 (b) for the same power transfer rating and immunes to the line unbalance.



(a) Cost of hybrid ac/dc vs. pure HVDC system using existing ac lines, with the passive design method



(b) Cost of hybrid ac/dc vs. pure HVDC system using existing ac lines, with the HLIC solution

Fig. 3-45. Cost comparison with different anti-saturation methods.

3.5.3 Comprehensive and practical evaluation of hybrid approach

The above evaluation simplifies the analysis of power capacity with dc-ac voltage ratio fixed at 1 as an example and only current ratio varied. In fact, the power ratio and cost are also dependent on voltage ratio. In addition, it is not clear how much thermal margin is used and left when increasing the power transferring capacity. To reveal the actual power capacity and cost benefits, both thermally current limit and electrically voltage insulation limit are adopted in this section, depicting a full picture of this hybrid system.

Three factors named as ac current usage ratio and dc current usage ratio, as well as the hybrid current usage ratio, are defined to show the real utilization of the existing ac lines. Firstly, V_p is used to derive the rated ac current of the pure ac line with power angle δ_0 . Then, for a hybrid line, the thermal limit is expressed as the RMS value of the hybrid ac and dc current.

$$I_{AC_rated} = \frac{V_p \sin \delta_0}{\sqrt{2} X \cos \phi} \quad (3-39)$$

$$\sqrt{I_{AC}^2 + \left(\frac{I_{DC}}{3}\right)^2} < I_{thermal} \quad (3-40)$$

Then, the ac current usage ratio is defined as the ratio of ac current in the hybrid system over the original ac line current. The dc current usage ratio is defined similarly. Finally, the hybrid current usage ratio is RMS current ratio of the two systems. According to the loadability SIL curve and empirical data, for a stability-constrained long line, the operating current is roughly less than 1/5 of its thermal rating. Therefore, the analysis for hybrid system should be limited to this range.

$$\xi_{AC} = \frac{I_{AC}}{I_{AC_rated}} = \frac{\frac{V_{AC} \sin \delta}{X \cos \phi}}{\frac{V_p \sin \delta_0}{\sqrt{2} X \cos \phi}} = \frac{\sqrt{2} V_{AC} \sin \delta}{V_p \sin \delta_0} = \frac{\sin \delta}{(1 + \lambda_v) \sin \delta_0} \quad (3-41)$$

$$\xi_{DC} = \frac{I_{DC}/3}{I_{AC_rated}} = \frac{\sqrt{2} \lambda_I \sin \delta}{(1 + \lambda_v) \sin \delta_0} \quad (3-42)$$

$$\xi_{Hybrid} = \frac{\sqrt{\left(\frac{I_{DC}}{3}\right)^2 + I_{AC}^2}}{I_{AC_rated}} = \frac{\sqrt{2} \lambda_I \sqrt{1 + \frac{1}{2 \lambda_I^2}} \sin \delta}{(1 + \lambda_v) \sin \delta_0} \leq \frac{I_{thermal}}{I_{AC_rated}} \approx 5 \quad (3-43)$$

Now, with the thermal constraint on the total hybrid current usage ξ_{Hybrid} , directly controlled voltage and current ratio λ_v and λ_I become constrained. As a result, ac current usage ratio and dc current usage ratio are also limited in the practical range. The three user-friendly usage ratios will replace the λ_v and λ_I as the evaluation index and λ_v and λ_I only play the roles internally.

A system study is made, assuming power angle can be improved from 30 degrees to 60 degrees owing to the enhanced angle stability of the hybrid system. Fig. 3-46 gives the power capacity

enhancement compared to pure HVAC line, vs. different dc and ac current usage ratio. The cost is shown in Fig. 3-47. The 3D multi-Pareto surface in terms of cost-capacity-total current thermal usage is given in Fig. 3-48. And the distribution of ac and dc power is shown in Fig. 3-49.

Thanks to the HLIC, the line unbalance is no longer an affecting factor on the hybrid system. And HLIC itself cost is very low, only several percentages of a LCC converter.

The coexistent relationship of these ratios is shown in Fig. 3-51 and Fig. 3-52.

The detailed quantified evaluation has shown that the hybrid ac/dc system have more benefits as long as proper voltage, current and power distribution are chosen. With all the information above, an optimal design is possible to be conducted.

3.6 Simulation verification

3.6.1 Line unbalance regulation

A hybrid system plus a HLIC converter are built with parameters given in Table 3-2.

Table 3-2. Hybrid ac/dc system parameters.

Parameters	Values
Line length	650 km
Line impedance	$(0.035\Omega + j0.9337\text{mH})/\text{km}$
Unbalance	5% (phase A)
Line voltage	ac: 280 kV (line); power angle 50° dc: 180 kV
Line current	ac: 612 A, dc: 1000 A
Transmission power	729 MW (189 MW ac and 540 MW dc)
Zigzag transformer	115 kV/280 kV/2 kV Turns: 170/138/138/3
Conditioner ac voltage	2.122 kV (peak)
dc link voltage	3 kV
dc link Capacitance	13 mF
Rectifier ac voltage	2 kV (RMS)

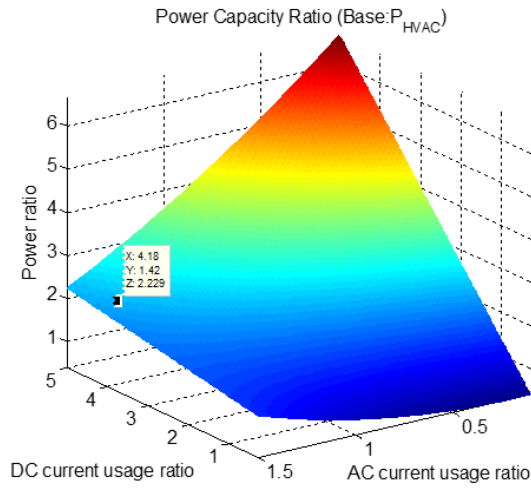


Fig. 3-46. Power capacity of hybrid ac/dc vs. dc and ac current usages.

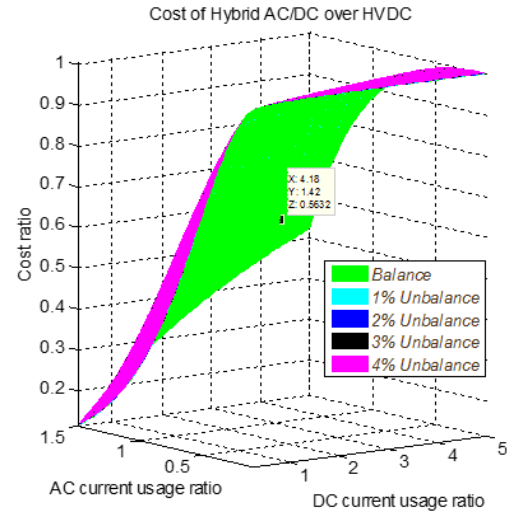


Fig. 3-47. Cost of hybrid ac/dc vs. dc and ac current usages.

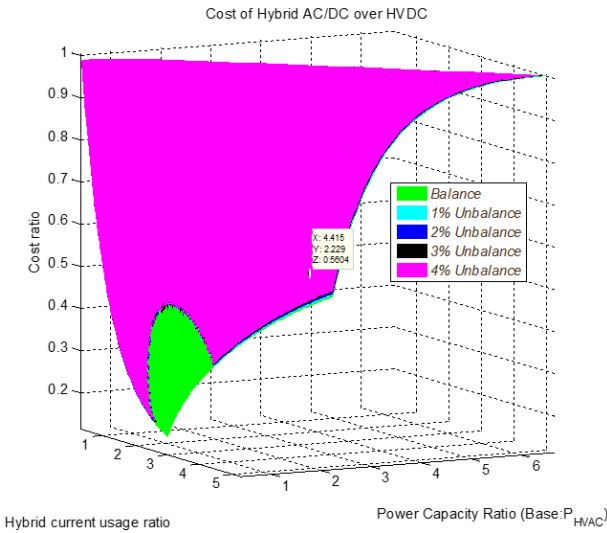


Fig. 3-48. Multi-Pareto surface in terms of cost-capacity-total current thermal usage.

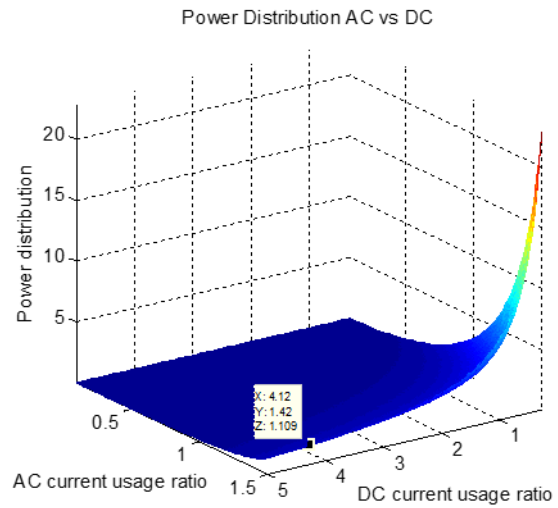


Fig. 3-49. Distribution of dc and ac power vs. dc and ac current usages.

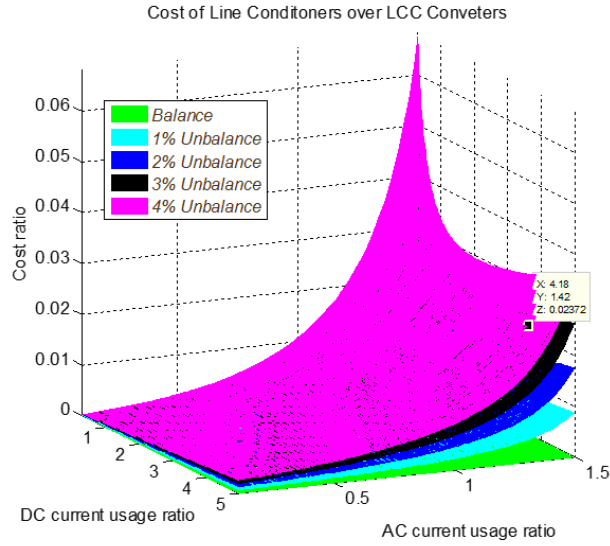


Fig. 3-50. Cost of HLIC vs. ac and dc current usages.

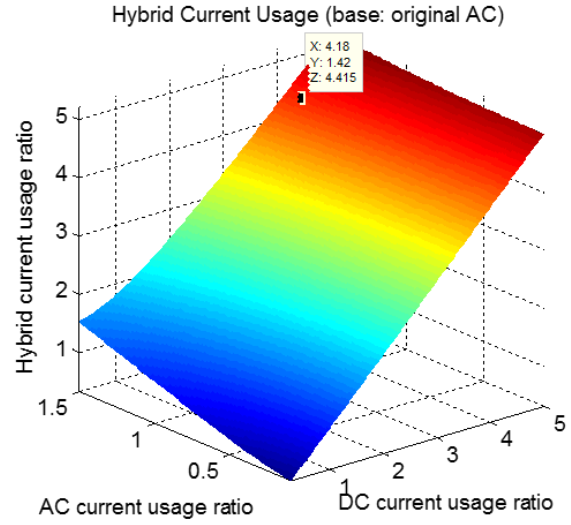
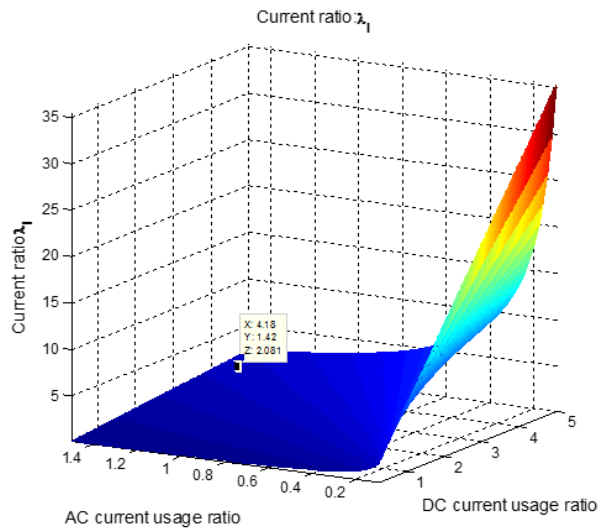
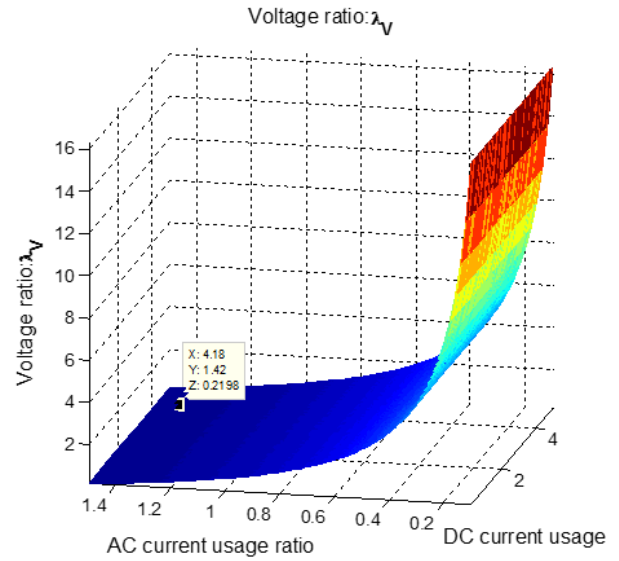


Fig. 3-51. Hybrid current usage vs. ac and dc current usages.



(a) Current ratio



(b) Voltage ratio

Fig. 3-52. Current and voltage ratios vs. ac and dc current usage ratios.

Fig. 3-53 depicts the dynamic performance of this conditioner. Initially, the dc components of hybrid line currents extracted via notch filters are not balanced due to the unbalanced line resistance in line *a*. With the designed control activated at $t=0.5$ s, the desired resistance is well regulated, and line currents are automatically equalized. The steady-state hybrid voltage and current after the desired impedance is achieved are shown in Fig. 3-54.

3.6.2 Dc-Link capacitance and dc voltage ripple

Capacitor selection based on (3-25) ~ (3-27) is shown in Fig. 3-55 under the specific system parameters. To suppress the ripple within a certain range, the maximum capacitance over a line cycle should be chosen. The difference between the red and blue curves indicates that the energy stored in ac inductors also has visible impacts on the capacitor selection. With the theoretical 11.5 mF capacitance as the peak point in Fig. 35, the dc-link voltage ripple in percentage is found to be $\pm 5.8\%$, and thus 13 mF capacitance is finally selected to ensure the maximum voltage ripple approximately at 300V ($\pm 5\%$). Simulation result for the above system is given in Fig. 3-56, showing the dc-link voltage ripple and the rectifier side current control.

3.7 Experimental verification

3.7.1 Hybrid ac/dc prototype

To verify the concept of HLIC and viability of the operation scheme, a scaled-down hybrid ac/dc laboratory system is implemented. The circuit schematic is shown in Fig. 3-57. Instead of a bipolar architecture, here only half-bipolar architecture is tested to simplify the system. The three-phase transmission line is emulated by a 1.8 mH three-phase inductor in series with three 1 Ohm resistors. The receiving end is terminated with a three-phase Y connected resistive load (neutral is not grounded) instead of another ac grid, avoiding building another ac grid in the lab. Also, to

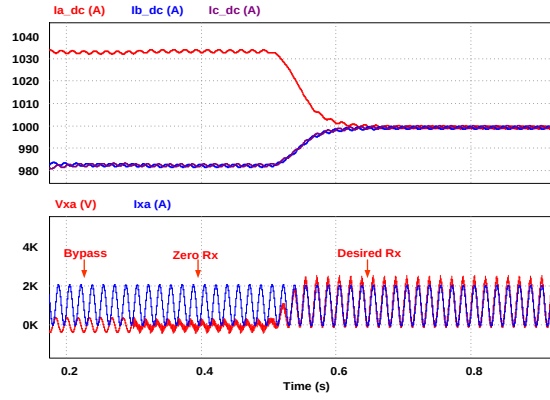


Fig. 3-53. Balance control of dc current through HLIC.

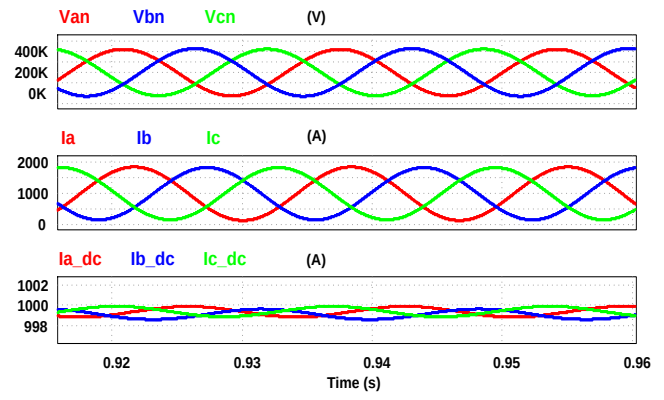


Fig. 3-54. Balanced voltage and current of three-phase hybrid lines in steady state under 5% line unbalance.

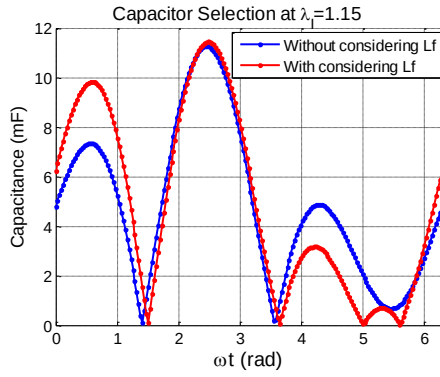


Fig. 3-55. Capacitance selection with $\delta=50^\circ$, $\theta=30^\circ$.

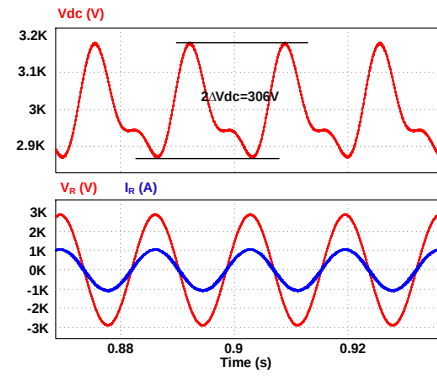


Fig. 3-56. Ripple reduction of dc-link voltage and rectifier control.

further simplify the prototype, instead of a relatively complicated Z/delta type transformer, a zigzag transformer with only zigzag windings is used at the secondary side to directly interface with the passive load. One has to mention since the dc voltage is just a common potential for the three lines, the line-to-line voltage across the passive load is still pure ac. Therefore, current flowing through the load is just the ac component, and all of the dc current in three phases will go through the neutral of the zigzag windings to HVDC converter. Furthermore, this conclusion can also be extended to other types of passive load, such as the inductive load. However, for a real hybrid ac/ds transmission system, the proposed structure in Fig. 3-21 should be adopted, and two delta/Z or Z/delta type zigzag transformers at both sending and receiving ends are necessary to interface with the two area grids.

As for the HVDC station, two back-to-back VSC converters instead of LCCs are built and operated to emulate HVDC converters due to its simplicity and availability in the lab. The test setup is demonstrated in Fig. 3-58.

To test the unbalance condition, a $0.33\ \Omega$ resistor is placed in phase *a* to mimic the line unbalance around 13% including winding resistances of two zigzag transformers. Then, a full bridge inverter is connected to a dc power supply, to operate as the HLIC device. The physical implementation of HLIC is presented in Fig. 3-59.

3.7.2 Pure dc mode test

First, the pure dc injection test without ac power flow under balanced line condition is conducted. Fig. 3-60 shows that dc current is distributed evenly among three-phase lines. Then, the operation of HLIC under the unbalanced line condition is verified as shown in Fig. 3-61. Due to the higher resistance in line *a*, its dc current is less than the other two phases in the initial period. Then unbalanced three-phase dc currents return to their balanced status again after inserting and

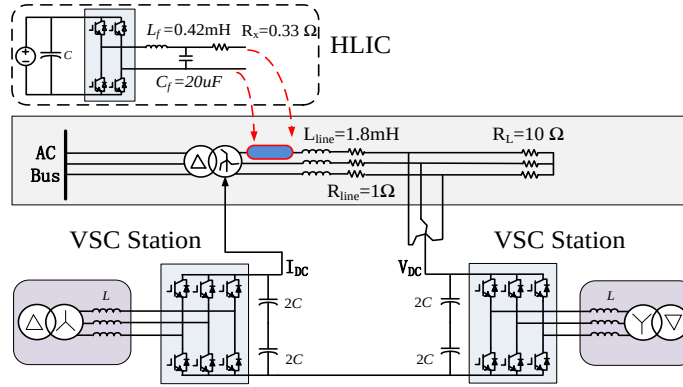


Fig. 3-57. Schematic of experimental set up for hybrid ac/dc with HLIC.

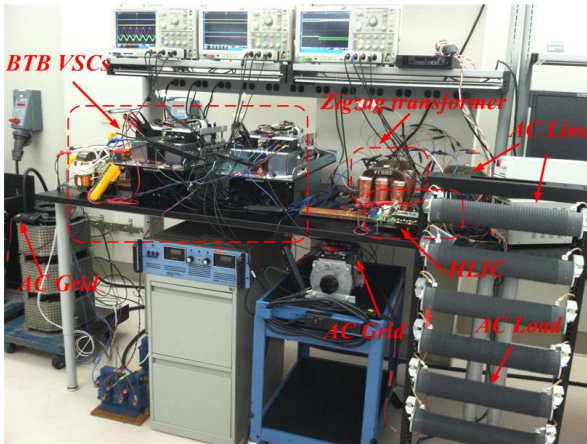


Fig. 3-58. Scaled-down prototype of the hybrid system with HLIC.

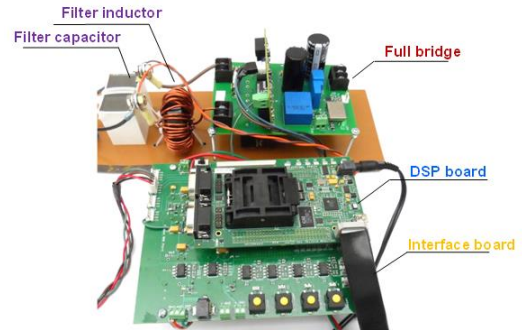


Fig. 3-59. Prototype of HLIC inverter.

enabling the HLIC control. Since phase *a* has larger resistance, HLIC in phase *a* is operated actively as a negative resistance.

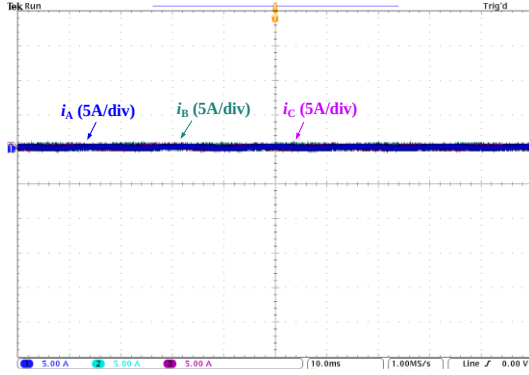


Fig. 3-60. Dc current even distribution among the three phases under balanced line condition in pure dc mode.

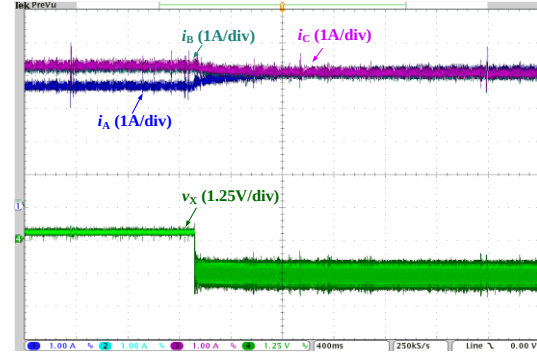


Fig. 3-61. HLIC regulation under line unbalance in pure dc mode.

3.7.3 Hybrid ac/dc mode test

To demonstrate the operation of hybrid ac/dc system, the start-up of dc injection under balanced conditions is shown first in Fig. 3-62. In sequence, first, the ac grid is operated. Then, HVDC converters build up the dc-link voltage, and finally, a desirable dc current is injected to hybrid ac/dc lines. The grid phase voltage is 30 V_{rms}, VSC dc voltage is controlled as 50 V, and dc current is regulated at 12 A. Zigzag transformers are designed at 3 A_{rms} ac and 4 A_{dc} per phase. After injecting the dc current, it is smoothly superposed into each phase line, shifting the original ac current up in each phase.

The test for the hybrid ac/dc operation under unbalanced conditions is then conducted. Shown in Fig. 3-63, once HLIC activated, phase *a* current is elevated to match the other two phases. From Fig. 3-64, *i_A* and voltage of HLIC are in phase, revealing that it indeed behaves as a resistor. The magnitudes of the three-phase currents have slight differences. It is because the impedances of other two lines in the test set-up are not exactly the same.

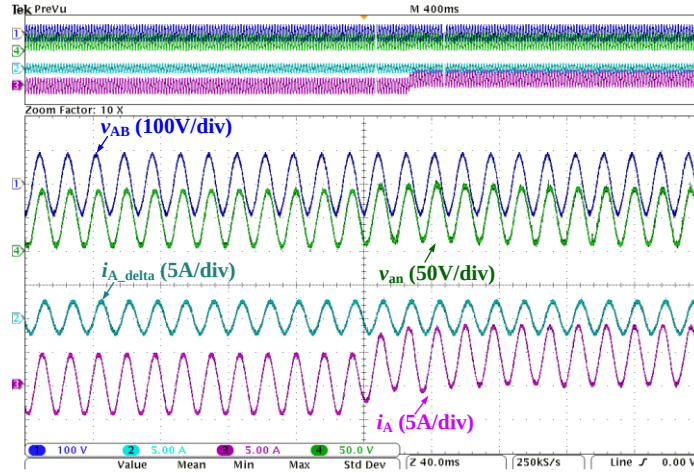


Fig. 3-62. Start-up of dc injection under hybrid ac/dc normal conditions (balanced lines).

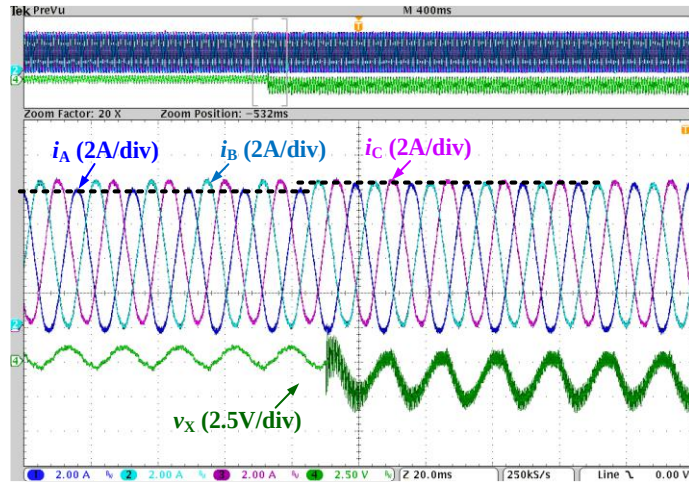


Fig. 3-63. HLIC regulation under the hybrid ac/dc operation.

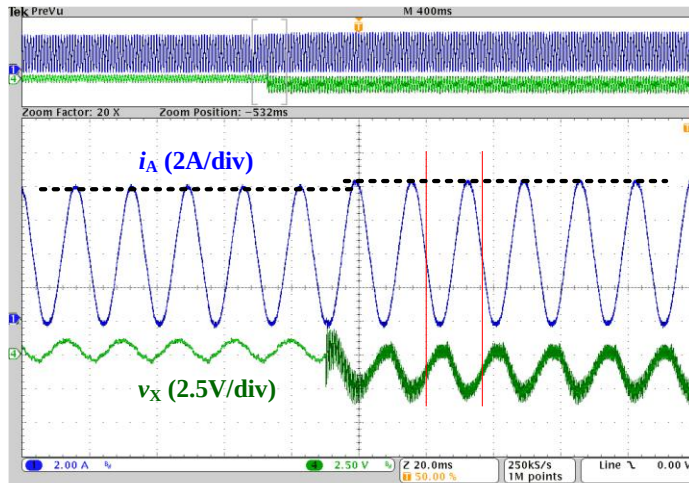


Fig. 3-64. A negative resistance emulated by HLIC in phase a .

To further verify the control, their dc components are extracted as provided in Fig. 3-65 indicating a success of line balancing function and negative resistance emulating, regardless of the aforementioned minor magnitude difference.

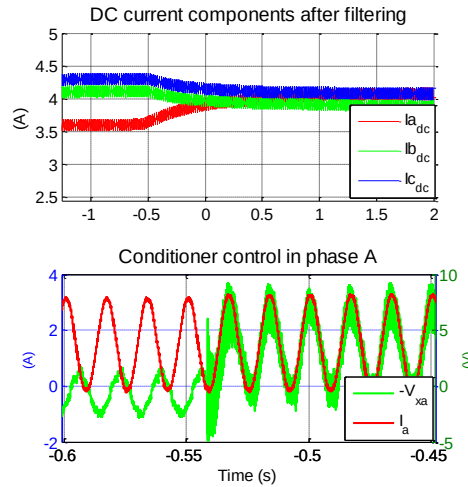


Fig. 3-65. Dc current components of hybrid line with HLIC regulation under line unbalance.
(the initial stage is in bypass mode)

3.8 Summary

Both passive and active approaches are proposed to solve the saturation problem in the hybrid interconnection of ac and dc transmission system, among which HLIC seems more promising. The merits of HLIC can be summarized as:

- Greatly reduce the cost of zigzag transformer and hybrid ac/dc system, enhancing its feasibility.
- Low voltage rating and power rating (1~2% of whole power rating) with low additional cost.
- Floated on each transmission line or integrated zigzag transformer, thus no insulation issue.
- Share the zigzag transformer to supply the ac power, no need for extra ac power sources.
- Operate autonomously with local communication, enabling easy application to power systems.
- Independent control of both ac and dc impedance, which can be served for other purposes.

The two-level control strategy of HLIC is proposed. The selection criterion of its key component, dc-link capacitance, is provided based on the power ripple analysis, which can be helpful for future hybrid ac/dc applications. Some of the practical implementation issues such as operation under abnormal conditions, installations, and fault protection scheme are addressed. The costs of HLIC and HLIC assisted zigzag transformer compared to the pure passive zigzag transformer are evaluated, and the cost of hybrid ac/dc system compared to pure dc upgrading of the existing ac lines are also studied, indicating HLIC assisted hybrid ac/dc system is a promising cost-effective transmission solution. The feasibility and effectiveness of the presented line conditioner, the system protection scheme, as well as the proposed selection criterion of dc capacitance, are verified by the simulation and/or experimental results.

4 Line Emulation Interfacing with VSC Based Grid Emulators

In power transmission systems, a transmission line is a backbone to interface with two power grids. Emulation of this type of grid infrastructure need properly deal with all potential interface issues when interconnecting the ac grids, which requires that the emulator should not only correctly model the behavior of a configurable and extensible line, but also physically interface with the ac grid in a stable manner. Additionally, when the grids themselves are also implemented by the VSC based emulator inverters, sampling issues related to PWM switched multiple converters show up and could affect the normal operation of line emulation.

4.1 Line model selection

In general, Bergeron's model can be equivalent to infinite PI sections. However, with more PI sections, the lumped model can more approximate to Bergeron model. The maximum frequency range represented by PI models is approximately

$$f_{\max} = \frac{N \cdot v}{8l} \quad (4-1)$$

Where $v = \frac{1}{\sqrt{LC}}$.

For a 300 km line with light propagation speed, this number is 125 Hz for one PI section. This simple model could be sufficient in studying the emulated power system concerning on system operation and control stability and dynamics, instead of high speed surges.

Again, as shown in (2-8), all LRC parameters in the lumped model are constants or determined by the operation line frequency for long lines. Thus, like Bergeron's model, the lumped is more suitable for low frequency dynamic simulation, with low frequency variation around fundamental grid frequency. Theoretically, the impact of frequency on line parameters such as skin effect and the long line correction can also be included in the lumped model to update its impedance in real

time. But this feature is rarely utilized in practice or in commercial EMTP type software, probably due to the facts that distributed line models are preferred when higher modeling accuracy is needed and that to model the multiple PI branches is unwieldy for real-time simulation.

On the other hand, for short lines and medium lines (shorter than 250km), since frequency impact on the line impedance is trivial, using constant frequency line parameter and fewer PI branches is feasible. This renders the hardware emulation of the ac line easier.

Since the line emulation via converter-based HTB platform is targeting for transmission level high power grid, the dynamic of the system is relatively slow and is also physically constrained by the limited control bandwidth of power converters whose phase lag can only be negligible below 100 Hz. Therefore, the frequency dependent distributed line model is unnecessary, also costly in terms of computation resources. Bergeron's model and lumped models, on the other hand, have more appeals to emulation applications.

4.2 Emulation schemes to interface two-area grid emulators

Based on the review in Section 2.2.3, the lumped parameter line model is simpler than Bergeron's model and more convenient in power system study since it uses the equivalent circuit to analyze the transmission line. For short lines and medium lines, line frequency impact is also trivial, resulting in frequency independent line models. This renders the hardware emulation of ac line easier. Two generic approaches of emulating the ac transmission line are developed based on back-to-back (BTB) voltage source converters (VSC) to represent the line from its terminal behaviors, corresponding to the phasor domain model and discrete time domain model, respectively.

4.2.1 Phasor-domain based steady-state line emulation model

If considering the physics of ac line from the power flow perspective as shown in Fig. 4-1, ac line provides a direct path for active power flow and acts as a storage tank to absorb in and transfer out the reactive power. If the terminal active and reactive power of emulation converters can be controlled the same as that in the actual ac line, then the emulation objective could be accomplished.

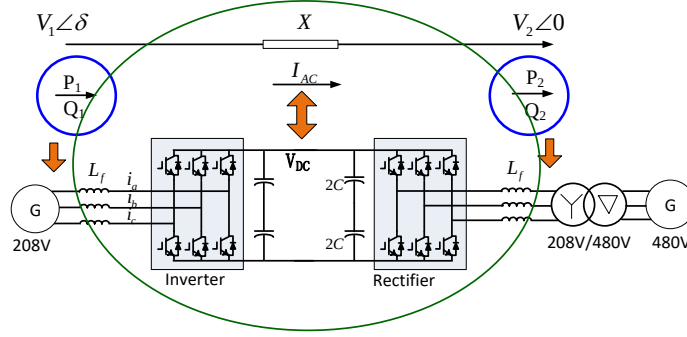


Fig. 4-1. Concept of BTB AC line emulation in phasor domain based on power flow perspective.

Thus, a simplified emulation model from this power flow perspective is proposed. First, a suitable PI model is selected and directly used to calculate the line impedance at 60Hz. Then, adopting the measured voltage at the sending and receiving ends, the transmitted active and reactive power is calculated to control the BTB converters. For a general PI model of the short line as illustrated in Section 2.2.3, the active and reactive power at two ends can be derived as [112].

$$\begin{cases} P_1 = \frac{3|A|V_1^2 \cos(\theta_B - \theta_A)}{|B|} - \frac{3V_1V_2 \cos(\theta_B + \delta)}{|B|} \\ Q_1 = \frac{3|A|V_1^2 \sin(\theta_B - \theta_A)}{|B|} - \frac{3V_1V_2 \sin(\theta_B + \delta)}{|B|} \end{cases} \quad (4-2)$$

$$\begin{cases} P_2 = \frac{3V_1V_2 \cos(\theta_B - \delta)}{|B|} - \frac{3|A|V_2^2 \cos(\theta_B - \theta_A)}{|B|} \\ Q_2 = \frac{3V_1V_2 \sin(\theta_B - \delta)}{|B|} - \frac{3|A|V_2^2 \sin(\theta_B - \theta_A)}{|B|} \end{cases} \quad (4-3)$$

Initially, a short lossless line model is selected for emulation at the time being. From above, the power reference at two ends can be simplified as

$$P_1 = \frac{3V_1V_2 \sin \delta}{X} \quad P_1 = P_2 \quad (4-4)$$

$$\begin{cases} Q_1 = \frac{3V_1(V_1 - V_2 \cos \delta)}{X} \\ Q_2 = \frac{3V_2(V_1 \cos \delta - V_2)}{X} \end{cases} \quad (4-5)$$

The control structure of BTB emulation is presented in Fig. 4-2 with a master-follower configuration. The ac line model is implanted inside the inverter, while the rectifier receives the reactive power reference Q_2 from the inverter side. Ideally, if the power loss of BTB voltage source converters is negligible, by controlling the dc link voltage at the rectifier side, the active power balance could be automatically achieved, thus no communication of active power reference P_2 is required. Each VSC is controlled under d-q coordinates and synchronized with the grid voltage by PLL. To calculate the power reference in (4-4) and (4-5), the rectifier side voltage and angle need to be sent to the inverter side controller. Different from the time domain static coordinate approach, the voltage and power signal are DC components, being relatively insensitive to the communication delay. This mechanism eliminates the time delay effects in steady state, reduces the error in power reference calculation.

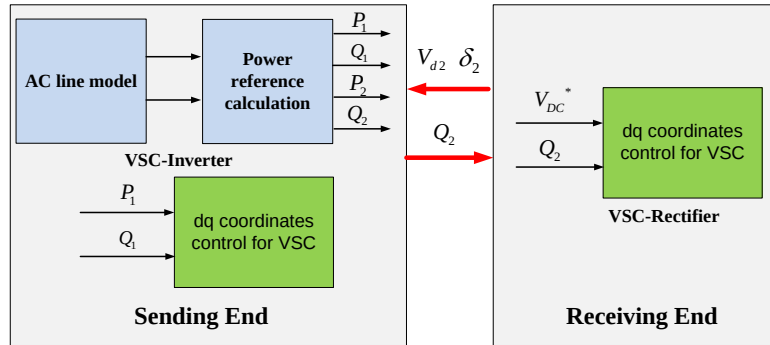


Fig. 4-2. Control scheme of BTB emulation in the phasor domain.

Owing to the real-time measurement and phase-locked-loop (PLL), voltage magnitude and power angle are tracked and updated cycle by cycle. Consequently, the power reference could be updated every line cycle. However, since the power flow based method is in the phasor domain, it only accurately reflects the steady-state power behavior of a line. In sum, this emulation is easy to be implemented, but more suitable for steady state and slow dynamic applications, such as the automatic runback application reported in [301] to push a new stable set point for HVDC. Detailed design and control of this type line emulation can be found in the author's previous work [28].

4.2.2 Time-domain based line emulation model

The time domain model based emulation, on the other hand, samples the instantaneous input voltages at both terminals and calculates the instantaneous current to be regulated based on (4-6) and (4-7), if it is a lossless line model. Therefore, it is capable of emulating fast transients and is desirable for system emulation.

$$\frac{di_{SR}(t)}{dt} = \frac{v_S(t) - v_R(t)}{L} \quad (4-6)$$

For the above simple inductor model, the trapezoidal discrete method is used to guarantee better accuracy and stability.

$$i_{SR}(k) = \frac{\tau}{2L} [v_S(k) + v_S(k-1) - v_R(k) - v_R(k-1)] + i_{SR}(k-1) \quad (4-7)$$

where τ is the discrete step size, and “S” “R” denote sending end and receiving end, respectively.

To precisely emulate the power transfer of ac transmission lines, it is crucial to have an appropriate model and a dedicate control scheme with high dynamic performance and accuracy. As illustrated in Fig. 4-3 of the proposed emulation scheme, the line model is implemented in the master VSC at the receiving end and only the reference command is sent to the follower VSC at the sending end “simultaneously”. To reduce the communication delay and avoid its side effect on dynamics and stability, 1) first, the ac interface voltages of both ends are sampled only by the

master, so that only ac current references are communicated; 2) although the line model is built in abc-coordinate to have the flexibility of representing each line individually, its ac current commands are transformed to the respective local dq-rotated-coordinate of each VSC before sending out to the follower. By conducting this ac-to-dc transformation, the current reference becomes immune to any communication delay in steady-state, which otherwise introduces around 400 us delay in the abc-coordinate and causes an undesired angle delay at two ends current, considering that $46\mu\text{s}$ is corresponding to one degree in 60 Hz systems. This control scheme also ensures the possibility to accurately model and reflect the propagation constant of the long line if Bergeron's model is implemented.

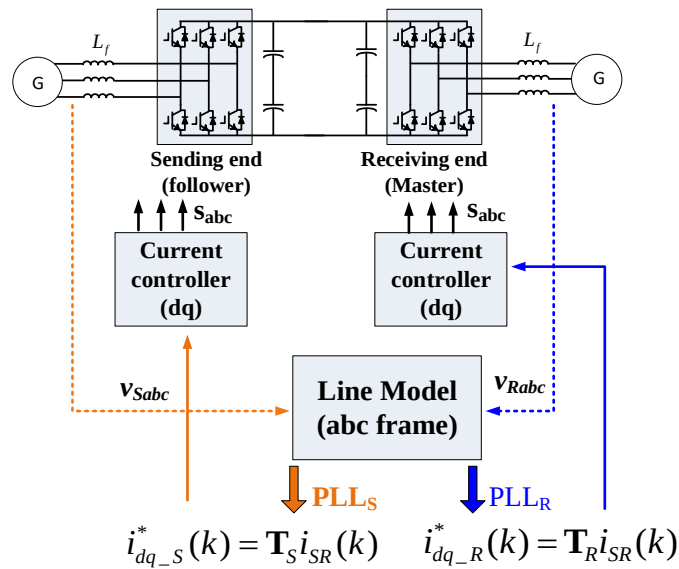


Fig. 4-3. Control scheme of time domain line emulation.

4.2.3 Extension to other line models

The above line model emulation shows how to mimic the simplest L model. It can easily extend this scheme to the short lossy line, i.e. L-R model. And it could also be extended to more complicated models, such as a general lumped PI model and distributed line model.

4.2.3.1 Extension to PI section models

First, a general PI model as shown in Fig. 4-4 (a) can be described by its terminal expression, i.e. (4-8) in the frequency domain using s transfer functions. To match the above scheme in which the measured voltage is adopted to derive the current reference, the ABCD-parameter of the two-port line model can be converted to the admittance parameter matrix, i.e. (4-9). Then, by using the trapezoidal discrete method, its resulting differential equation pair can be conveniently implemented using the above emulation system as voltage-controlled-current sources.

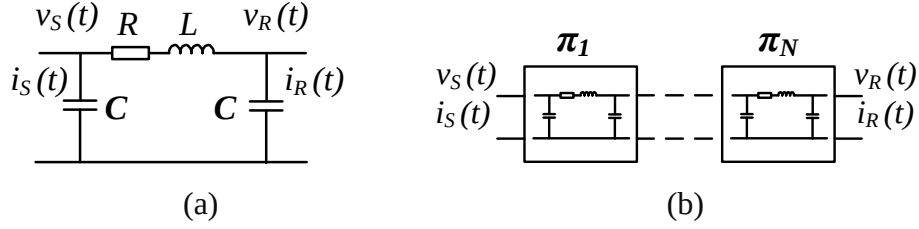


Fig. 4-4. One PI section line model. (a) one section, (b) cascaded sections.

$$\begin{bmatrix} v_S(s) \\ i_S(s) \end{bmatrix} = \begin{bmatrix} A(s) & B(s) \\ D(s) & E(s) \end{bmatrix} \begin{bmatrix} v_R(s) \\ i_R(s) \end{bmatrix} \quad (4-8)$$

$$\begin{bmatrix} i_S(s) \\ i_R(s) \end{bmatrix} = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix} \begin{bmatrix} v_S(s) \\ v_R(s) \end{bmatrix} \quad (4-9)$$

The cascaded PI models can also be extended by cascading the ABCD-matrix and follow the similar conversion procedure.

$$\begin{bmatrix} v_S(s) \\ i_S(s) \end{bmatrix} = T_1 \cdots T_N \begin{bmatrix} v_R(s) \\ i_R(s) \end{bmatrix} \quad (4-10)$$

$$\begin{bmatrix} i_S(s) \\ i_R(s) \end{bmatrix} = \begin{bmatrix} Y'_{11}(s) & Y'_{12}(s) \\ Y'_{21}(s) & Y'_{22}(s) \end{bmatrix} \begin{bmatrix} v_S(s) \\ v_R(s) \end{bmatrix} \quad (4-11)$$

4.2.3.2 Extension to distributed line model

The L-based emulation model and scheme can also be extended to distributed lines. Fig. 4-5 illustrates how the L based emulation model can be modal-equivalent to the classic distributed line model, i.e. Bergeron's model. In this case, the propagation time constant is one discrete time step, yet it can be programmed with parameters of a distributed line to implement the Bergeron's model.

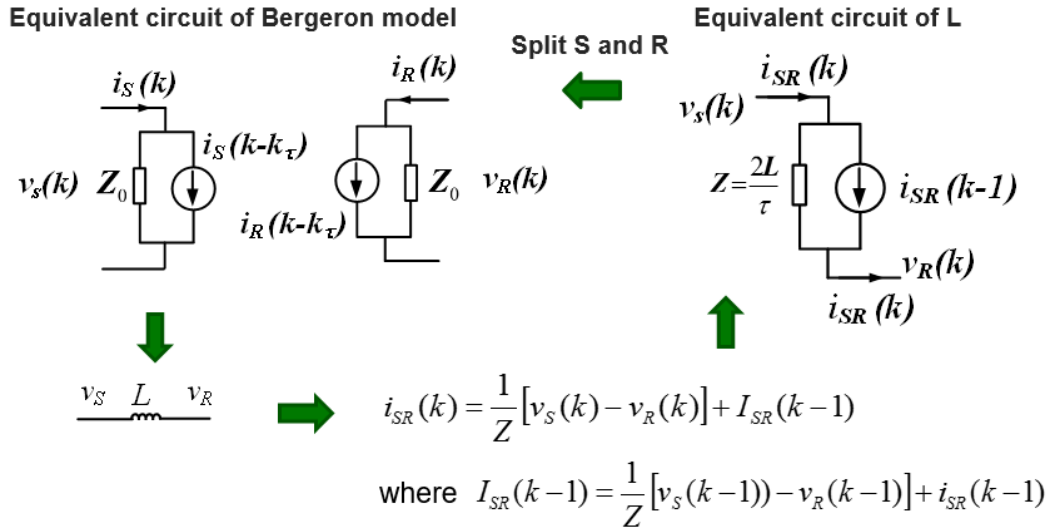


Fig. 4-5. Modal-equivalence of proposed emulation model and Bergeron's model.

4.2.4 Simulation verification

A simulation comparison using Simulink inductor model and BTB emulated L model is conducted, to verify the accuracy of the time-domain emulation model under both steady and dynamic condition. The disturbance is created by step changing the line impedance. An external equivalent series resistance (ESR) with a typical ratio of $X/R=10$ is also inserted to mimic the real transmission line.

As shown in Fig. 4-6, the sending end and receiving end currents of the emulator match very well with that of the Simulink model under all step changes for all three phases.

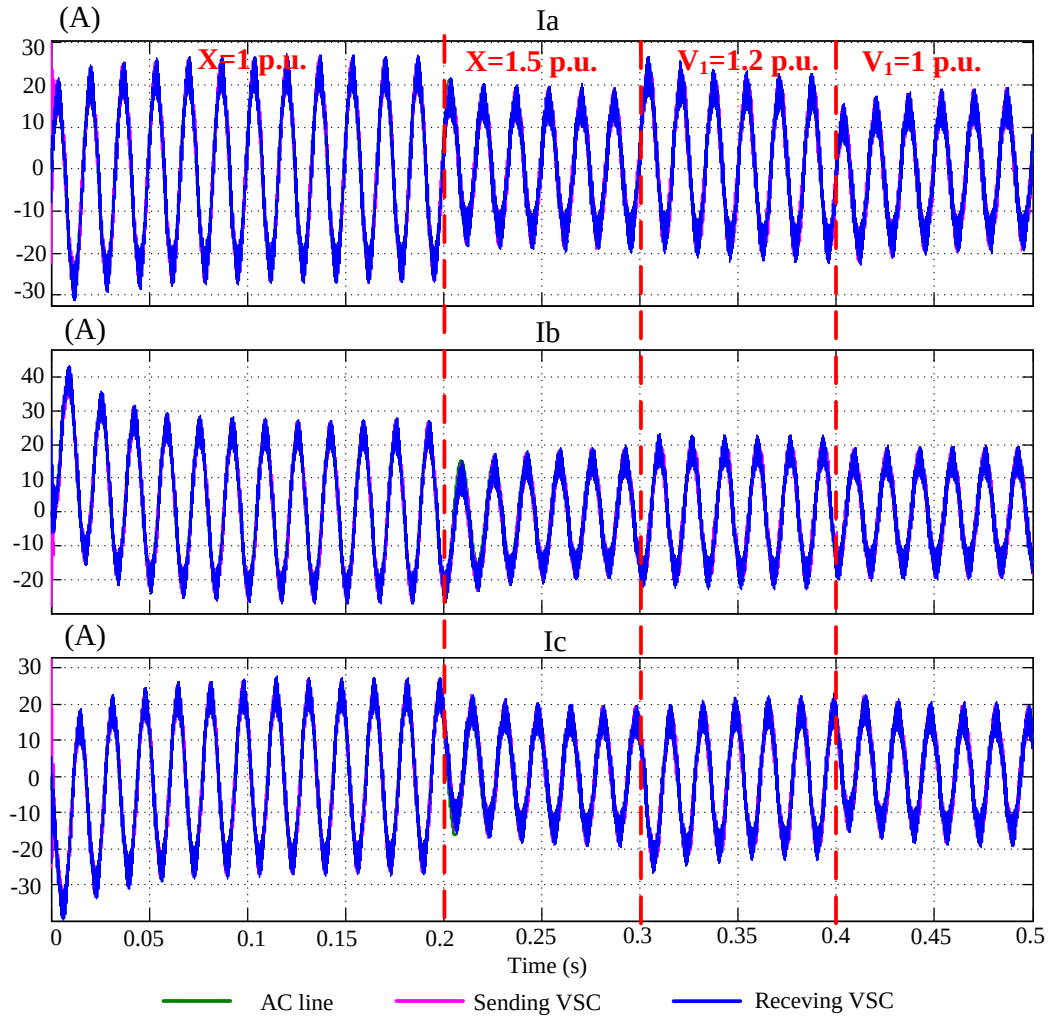


Fig. 4-6. Comparison of L model between line emulator and Simulink model.

4.2.5 Experimental verification

A system study is carried in HTB emulation platform, as shown in Fig. 4-7, which is a scaled-down Kundur two-area system. The BTB emulator is compared with three 7.5 mH physical inductors. Firstly, static emulation performance is verified. As presented in the Fig. 4-8, the emulator behaves very similarly to the physical line inductors. The current magnitudes in both cases are the same, and there is a minor difference in voltage and current angle, which may be related to the measurement error.

The transient emulation performance is also tested. A 0.1 p.u. step change of load power is set in the transient test, where generator G1, G3 and load 9 are activated. Results of active power and frequency of G1 in two cases are given in Fig. 4-9 and Fig. 4-10. The shapes of transient oscillation waveforms in both cases are quite close, while the minor mismatch may come from the measurement error in inductance value and ESR value of the inductors.

4.3 Impact of HF sensing noise of interface on line emulator and its mitigation

4.3.1 Switching harmonics in ac voltage sampling

In a multi-converter emulation system with only L filter as currently implemented in HTB system, switching harmonics cannot find a bypass path, thus are fully present at the ac terminals as illustrated in Fig. 4-11. Meanwhile, voltage sampling is key for line emulation systems. Strong filters that introduce several degrees phase delay at the fundamental frequency are thus unacceptable. With limited filtering, if following the traditional ‘one sample per switching cycle’ scheme, noticeable 2nd order harmonic will show on the sampled voltage as seen in Fig. 4-12.

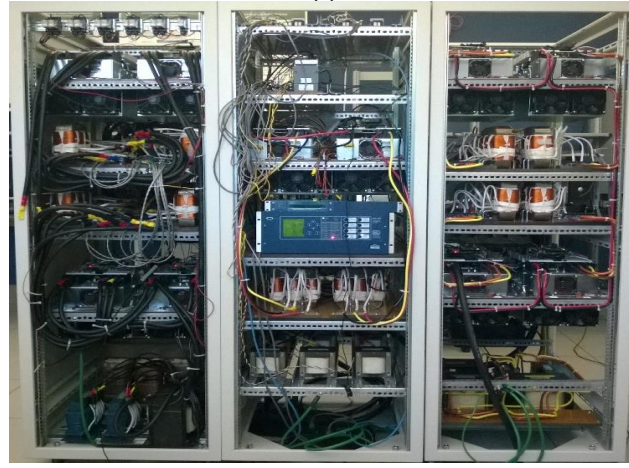
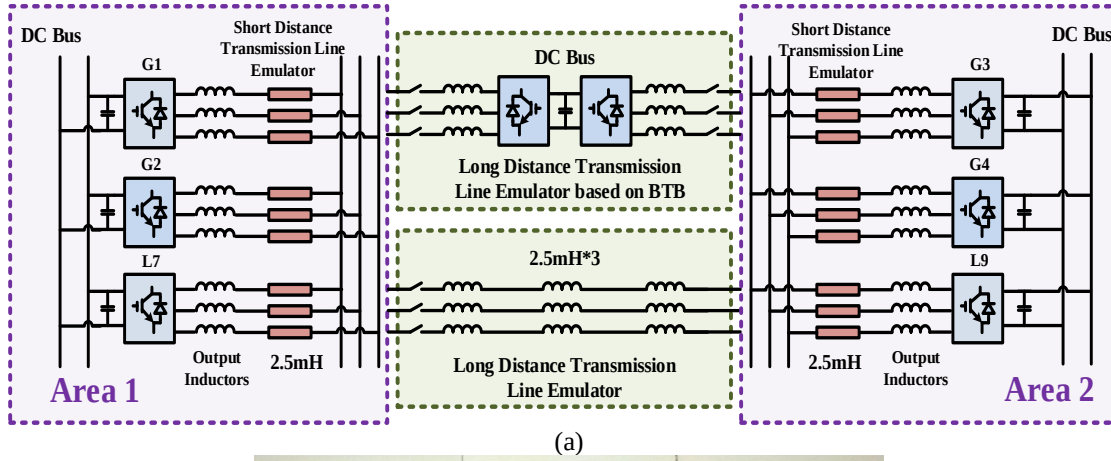


Fig. 4-7. Schematic and test bench of HTB two-area systems. (a) schematic. (b) prototype photo.

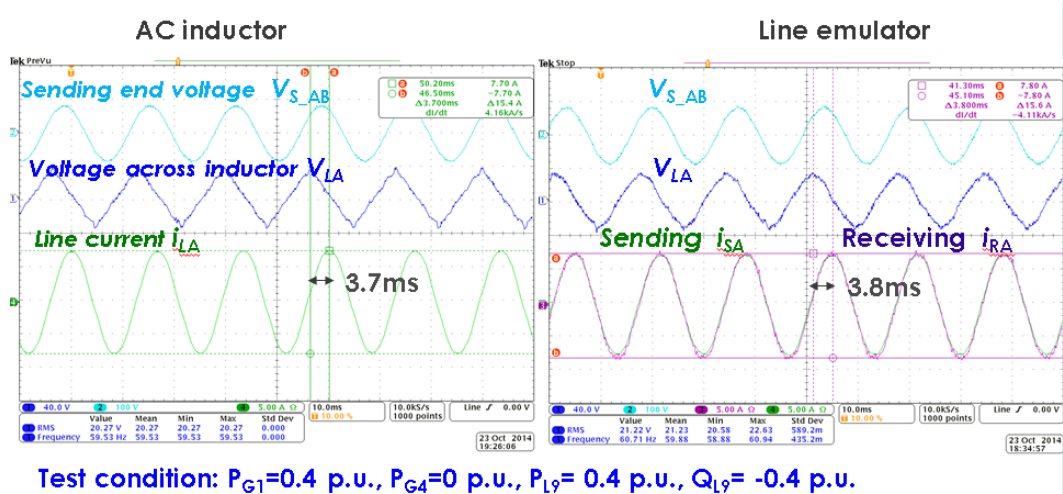


Fig. 4-8. Comparison of static performance between line emulator and physical three-phase line inductors.

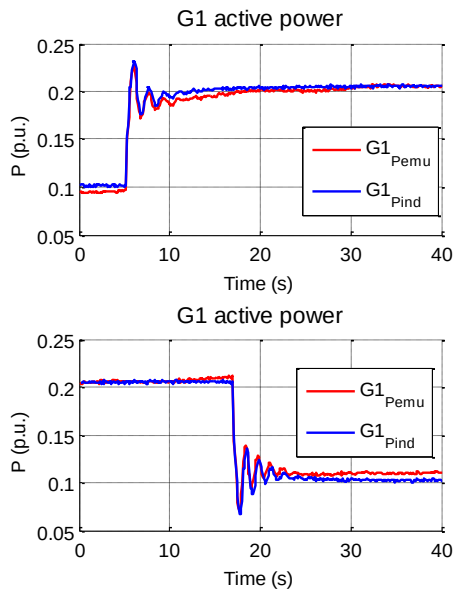


Fig. 4-9. Active power flow during power step up and down transient.

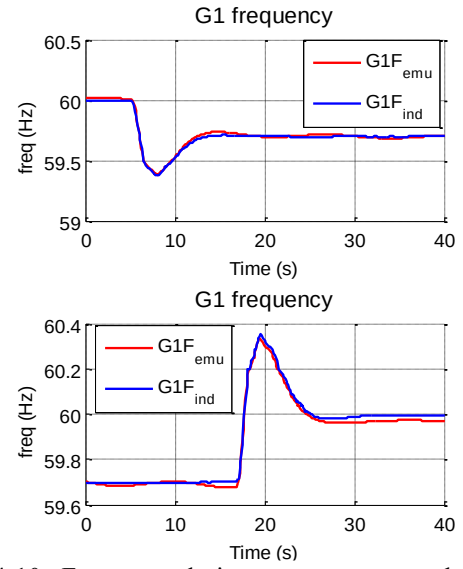


Fig. 4-10. Frequency during power step up and down transient.

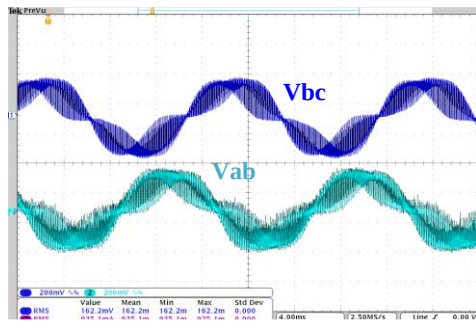


Fig. 4-11. Input ac voltages with high switching harmonic noises.

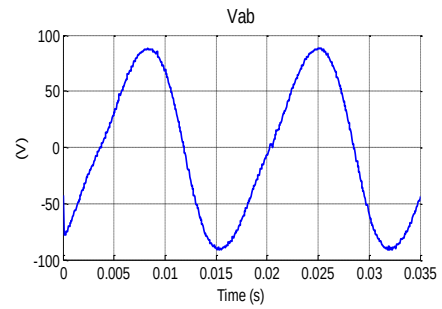


Fig. 4-12. The 2nd order ripples in the sampled line voltage.

4.3.2 Single frequency sampling

Through a close look into the sensing voltage as given in Fig. 4-13, the line voltage signal after a limited filter contains switching frequency ripples stretched along every peak and zero-crossing point. If a single sampling per cycle scheme is applied for the asynchronous PWM voltage, the sampled voltage can either be the high level or low level of the ripple voltage, as illustrated in Fig. 4-14. As a result, instead of obtaining the mean value of the switching envelope, the peak or bottom of the envelope will be sampled. Therefore, a continuous peak and bottom will form the 2nd order voltage distortion.

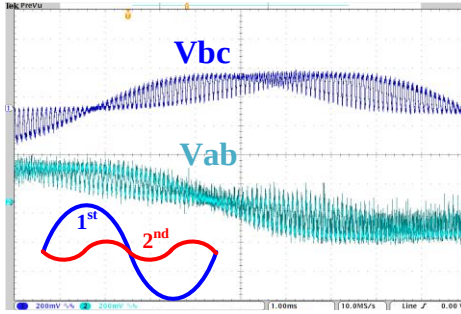


Fig. 4-13. Zoomed-in sensing voltage at the line emulator terminal.

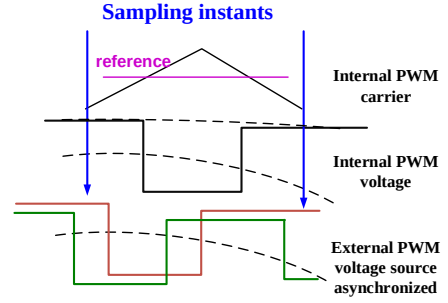


Fig. 4-14. Analysis of the sampling error in one sampling per switching cycle.

4.3.3 Doubling frequency sampling

Intuitively, increasing the sampling frequency should help mitigate this issue. The minimum sampling frequency should be double switching frequency, followed by a 2-point moving average filter to obtain the mean. However, a very low frequency deviation occurs, which is clearly seen from the phase-locked-loop (PLL) test result under dq coordinate in Fig. 4-15 (b). From the transformation relationship in (4-12), the 30 s around periodic low frequency ripple of V_d in dq coordinate reflects a small amount of $\omega_0 + \Delta\omega$ ripple in addition to the main frequency ω_0 component.

$$v = V_m \sin(\omega_0 t) + \Delta V_m \sin((\omega_0 + \Delta\omega)t) \xrightarrow{abc2dq} v_d = V_m + \Delta V_m \sin(\Delta\omega t) \quad (4-12)$$

An explanation of this effect is given in Fig. 4-16, without considering the filter or sensing delay to simplify the analysis. If the instantaneous duty cycle d of the external PWM voltage is around 0.5, both the high and low switching ripples are sampled, leading to the correct mean value. When d is far from 0.5, either higher or lower, both sampling instants in a PWM cycle may catch up the high-level or low-level noise, leading to the unexpected error. Since d is an ac signal varying in a line cycle, the resulted error should also repeat over line cycles, forming a ω_0 ripple component. However, since the external PWM VSI is not synchronized to the emulator VSI (converters are individually controlled, and filters have significant phase shift at high frequency), a slow beat frequency $\Delta\omega$ will exist, thus eventually leads to $\omega_0 + \Delta\omega$ ripple component. From testing observations, the slow period is not constant and could vary when tested at different dates.

Other possible reasons are also listed as follows: First, PWM harmonic voltage has certain sidebands and noticeable 2nd switching frequency component, thus aliasing effects may not be fully avoided with only double sampling. From the moving filter point of view, these noises are also not effectively filtered due to the limited attenuation resulting from the lowest depth $N=2$ where N is the filter order. Moreover, due to the non-uniform magnitude attenuation of front-end analog filter over the whole frequency range, the asynchronized PWM voltage sampling, and the variable duty cycles over each line cycle, voltage ripples in two adjacent switching cycles as illustrated in Fig. 4-16, are not fully cancelled in the moving average process and instead have a slight amplitude difference. Eventually, this leads to a low amplitude periodic noise along with the line cycle and introduces a low frequency oscillation in grid frequency and line power flow.

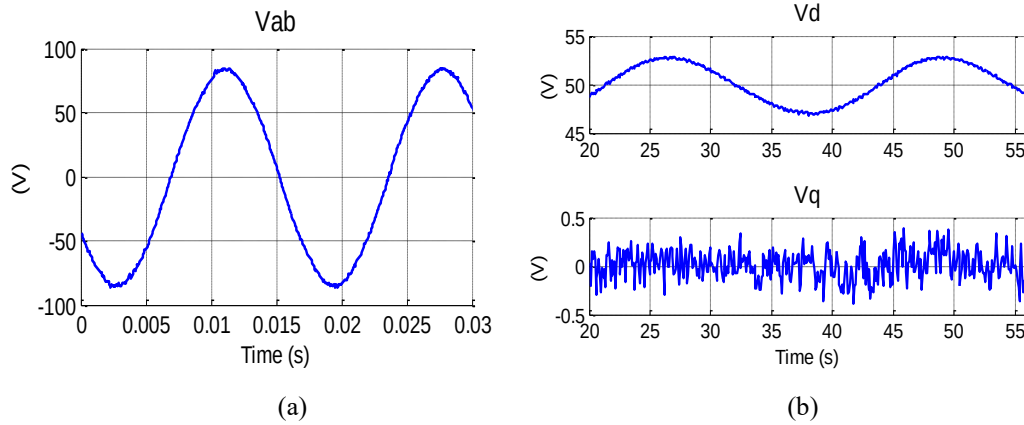


Fig. 4-15. Sampled line voltage with double sampling per switching case. (a) line voltage shape in abc coordinate. (b) low frequency variation in dq coordinate.

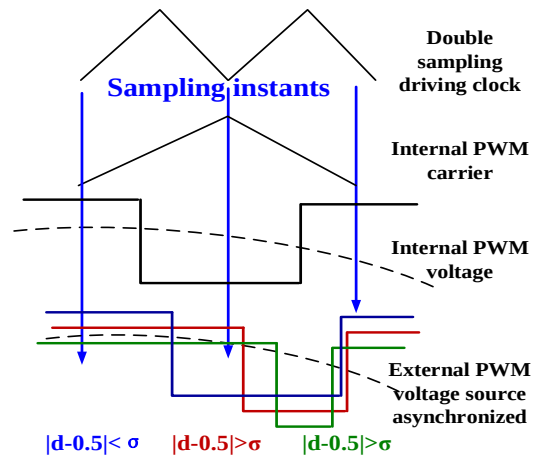


Fig. 4-16. Analysis of the sampling error in 2-point sampling per switching cycle.

4.3.4 Four times frequency sampling

Therefore, a sampling scheme with four-point per switching cycle plus $N=4$ moving average filter is proposed. As illustrated in Fig. 4-17, as long as d is within $[0.25 \ 0.75]$, in each f_s cycle, both high and low levels can be sampled twice. Then with $N=4$ moving average filter, all the $2^{\text{nd}} f_s$ ripple and part of side harmonics are filtered, as shown in Fig. 4-18. From the time-domain view, the average of four samplings per switching cycle is also more immune to the PWM voltage asynchronization and non-uniform noise attenuation. Yet, if d is higher than 0.75 or lower than 0.25, there is still chance that incomplete cancellation of the high- or low-level ripples, leading to a low beat frequency ripple as shown in the voltage V_d of Fig. 4-19, but the sampling voltage ripple is much reduced in both the sending and receiving side of the emulator.

4.3.5 Impact on transmission behavior

Originally, with the sampled noise, the 2^{nd} order ripple and the low-frequency beat ripple will be involved in the current reference calculation and cause the incorrect line emulation and oscillation behaviors in the line power flow. As shown in Fig. 4-20, the low beat frequency ripple from the doubling frequency sampling scheme is reflected in the power flow and grid frequency, which does not exist in the physical inductor line. Once the final scheme is applied, the line emulator can match the physical inductor line during the steady-state and frequency dynamic.

4.4 Impact of dc sampling bias on line emulator and offset remover

4.4.1 Offset sensitivity of pure integrator based model

As analyzed in Section 2.2.4, for the simple lossless line model, i.e. an inductor L , current reference is generated from the voltage based pure integrator, which, however, is prone to the dc drift noise on sensing or sampling signals of the interfacing ac voltage. Given any dc bias, the

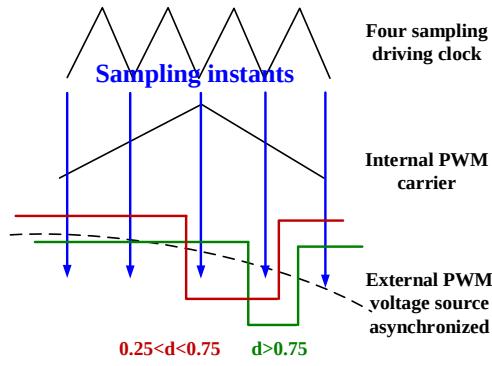


Fig. 4-17. Analysis of the sampling error in 4-point sampling per switching cycle.

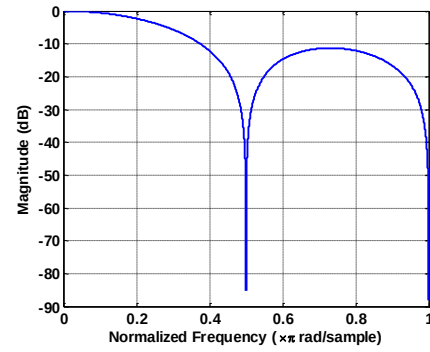


Fig. 4-18. Frequency response of $N=4$ moving average filter.

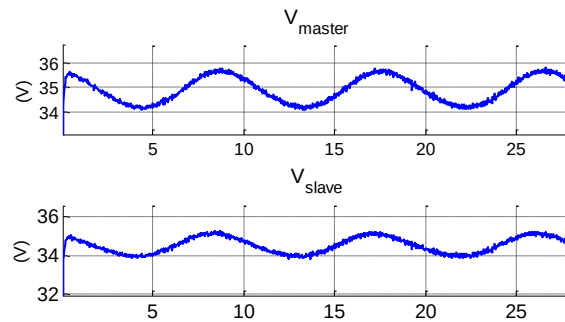
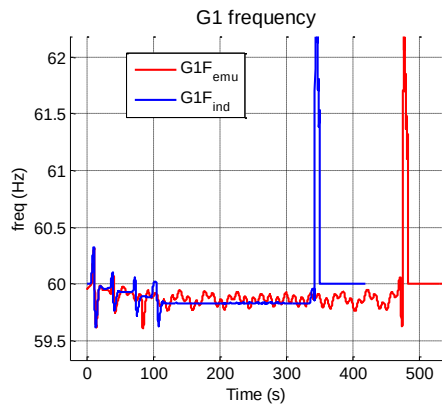
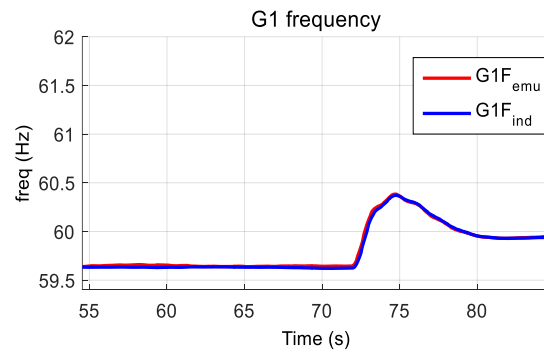


Fig. 4-19. Improved sampling voltage results with less ripples.



(a) $N=2$.



(b) $N=4$.

Fig. 4-20. Comparison of emulation accuracy between $N=2$ and $N=4$ sampling methods.

current reference would be linearly integrated to very high value, especially in the low ESR or lossless line case, as illustrated in Fig. 4-21 from an actual test.

$$L \frac{di}{dt} + iR = v_{ac} + v_{dc} \quad (4-13)$$

$$v_{dc} = L \frac{di_{dc}}{dt} \quad (4-14)$$

4.4.2 Basic concept of dc offset controller

According to testing results, this dc drift may also vary with time, therefore it cannot be easily compensated in an open loop manner. A closed-loop compensator is preferred. The proposed controller is illustrated in Fig. 4-22, which can be also regarded as a dc offset estimator.

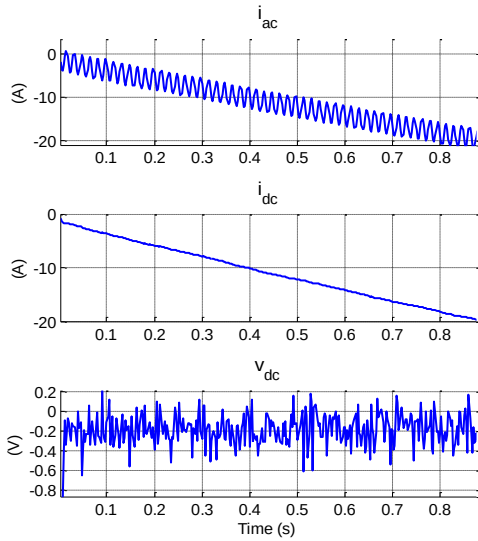


Fig. 4-21. DC current drift due to small dc bias noise.

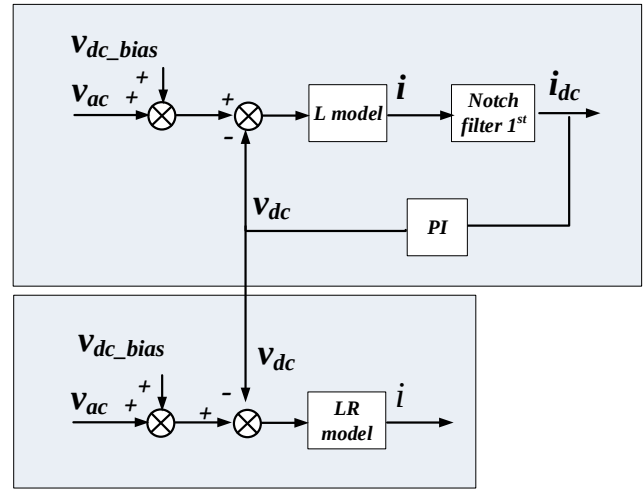


Fig. 4-22. The block diagram of proposed dc offset controller

The dc component of the output current is adopted as the feedback signal, obtained via an adaptive notch filter with its notching point designed at the line frequency. The combination of L-LR model is proposed because the lossless L model suffers the severest impact by dc bias noise, while LR model is more practical in emulating real transmission lines and also less sensitive to dc

bias. Therefore, by adopting L model as a dc bias removal loop, it provides a sensitive bias indicator to LR model emulation, enabling the better dc elimination in general cases.

A PI regulator then generates the corresponding counterpart of dc offset noise, to force the input of the integrator bias-free. The transfer function of the dc offset control loop is given as

$$G_{dc_offset_loop}(s) = \frac{\hat{v}_{dc}}{\hat{v}_{dc_bias}} = \frac{\frac{1}{SL} \cdot NF(s) \cdot PI(s)}{1 + \frac{1}{SL} \cdot NF(s) \cdot PI(s)} \approx \frac{\frac{1}{SL} \cdot PI(s)}{1 + \frac{1}{SL} \cdot PI(s)} \quad (4-15)$$

$$= \frac{k_p s + k_i}{s^2 L + k_p s + k_i} = \frac{k_p s + k_i}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

where PI parameters following the normalized second-order system design are derived as

$$\begin{cases} k_p = 2\xi\omega_n L \\ k_i = \omega_n^2 L \end{cases} \quad (4-16)$$

It is preferred to select

$$\omega_n < \omega_0 / d \quad (4-17)$$

$$\xi = 0.5 \sim 1 \quad (4-18)$$

where d is the ratio of line frequency ω_0 to corner frequency ω_n . d should be selected to achieve the desired bandwidth.

As discussed in Section 2.2.4, the prior works on dc bias control have discussed the evaluation metrics of their schemes but lack a clear picture of the performance. To give a unified metric, the function of decreasing the sensitivity of the pure integrator to its input bias is reconsidered as a high pass filter (HPF) from the frequency domain perspective. This requires offset controller to block and attenuate dc bias in the integration path but has the least impact on signals at high frequencies, so that the emulation system can be operated with zero error during the fast transients.

Following this concept, the above closed-loop dc offset control is now re-evaluated in its HPF structure. By reorganizing the whole control block diagram from the input voltage to the output current, its equivalent HPF feature is obtained as

$$\frac{\hat{i}}{\hat{v}_{ac}} = \frac{1}{1 + \frac{1}{SL} \cdot NF(s) \cdot PI(s)} \frac{1}{SL + R} \quad (4-19)$$

$$G_{HPF_LLRNF}(s) = \frac{1}{1 + \frac{1}{SL} \cdot NF(s) \cdot PI(s)} \quad (4-20)$$

If only LR model is adopted in bias controller, the following transfer function will be

$$G_{HPF_LLRNF}(s) = \frac{1}{1 + \frac{1}{SL} \cdot NF(s) \cdot PI(s)} \quad (4-21)$$

From HPF characteristic curves of two models in Fig. 4-24, both schemes can achieve unity gain and zero phase lag above the target frequency, while L-LR companion model provides extra 20 dB/dec attenuation at dc and low frequencies. This verifies the previous discussion.

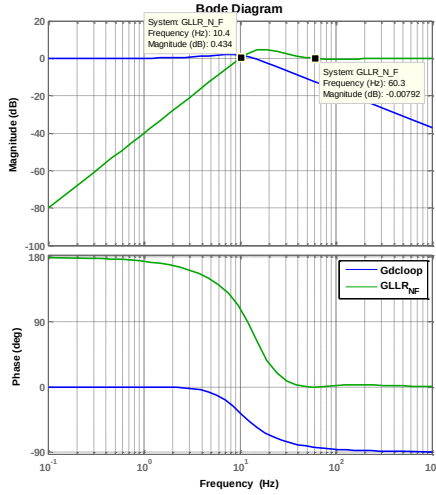


Fig. 4-23. DC offset controller.

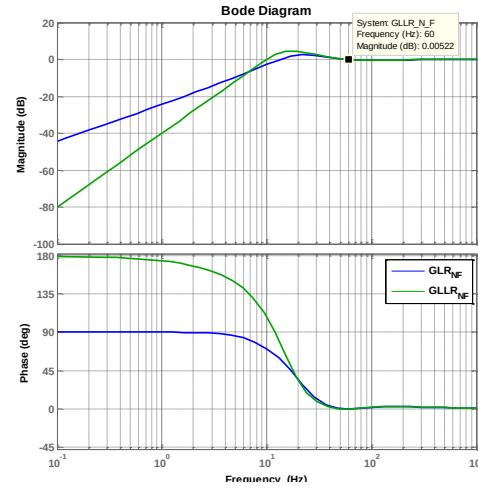


Fig. 4-24. Equivalent HPF characteristics.

4.4.3 Adaptive offset control for variable frequency operation

In the previous analysis, to extract dc bias noise, a notch filter with resonance frequency at the nominal line frequency 60 Hz is used. However, this may introduce errors in a variable frequency system or during system transients. To ensure the unity filter gain and zero phase lag at the high frequency range from HPF prospective, an adaptive notch filter is therefore implemented in the

offset controller. One simple approach is to adopt the PLL output frequency as the varying resonance frequency of the notch filter.

$$NF(s) = \frac{s^2 + \omega_r^2}{s^2 + 2\xi_r \omega_r s + \omega_r^2} \quad (4-22)$$

where, $\omega_r = \omega_{PLL}$.

As a result, it can adaptively cancel the dc offset with only input information. Another benefit from the adaptive design would be consistent offset control dynamics as determined by (4-20) under variable grid operation frequencies.

4.4.4 Controller design considering external line impedance

The above control only assumes the line emulator interfacing with the ideal ac system, where no external line impedance is considered. Now, if it connects two typical ac grids with extra serial impedances, the dc offset control loop has to be modified as depicted in Fig. 4-25. DC offset control block diagram considering external line impedances.. L_g and R_g represent the equivalent external line impedance, and $T_{cc}(s)$ denotes the emulator current control, which has approximately unity gain within the current loop bandwidth.

It is found that HPF transfer function still holds the same form as (4-21), except for an extra term, i.e. an impedance ratio L_g/L . Consequently, PI parameters should be altered as in (4-24).

$$G_{dc_offset_loop} \approx \frac{k_p s + k_i}{(1 + \frac{L_g}{L})s^2 + 2\xi\omega_n s + \omega_n^2} \quad (4-23)$$

$$\begin{cases} k_p = 2\xi\omega_n L(1 + \frac{L_g}{L}) \\ k_i = \omega_n^2 L(1 + \frac{L_g}{L}) \end{cases} \quad (4-24)$$

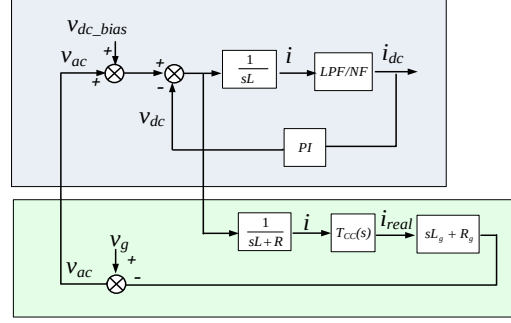
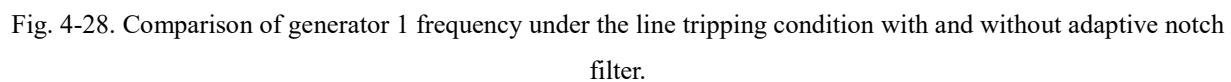
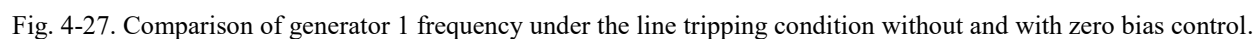
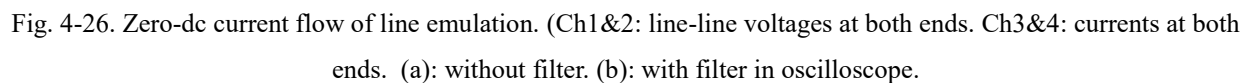


Fig. 4-25. DC offset control block diagram considering external line impedances.

4.4.5 Experimental verification

The proposed dc offset control is first verified on its static performance. As shown in Fig. 4-26, the dc current bias is fully eliminated after enabling this control.

Another emulation study is carried out to evaluate the emulation accuracy and dynamics when the line impedance suffers abrupt changes, which could happen when one set of two paralleled transmission lines is tripped, i.e. the line impedance gets doubled. A comparison is made among Simulink simulation with line inductor model and HTB tests with line emulator with and without the dc offset control. The line is modeled with a fairly high ESR, thus the steady-state dc current is low even without the dc offset control. However, as shown in Fig. 4-27, during the large signal disturbance, a high mismatch is observed when this controller is enabled as marked in green. This is due to frequency deviation from the fixed 60 Hz notch filter in the controller. Once the adaptive filter is applied as presented in section 4.4.3, results shown in Fig. 4-28 and Fig. 4-29 demonstrate a good match between simulation and HTB line emulation, as well as good dc shift suppression. To be clarified, the small ripples observed in HTB test results are measurement noises due to power converter switching operations.



A further system level performance is compared between the final emulator and the physical inductor line. Both the steady-state and dynamic power flow for two cases match quite well.



Fig. 4-29. Comparison of generator 1 active power under the line tripping condition with and without adaptive notch filter.

4.5 Interface stability of transmission line emulator

The analysis mainly focuses on the low frequency stability phenomena within controller bandwidth 1 kHz, especially below 100 Hz, which is the main interest range of power system transients. For these low frequency transmission line behaviors, control amplitude error, as well as phase leg delay are negligible. Therefore, current/voltage control transfer characteristics from the actual emulation converters are not included to simplify this analysis. Instead, this converter control level stability is tackled separately, so that the investigation of emulation accuracy and stability can concentrate on the emulation model and its interface grid, as well as the simulation step size and integration methods.

4.5.1 General emulation schemes

Before addressing the stability issues, different line emulation schemes will be briefly discussed. Typically, we can categorize ac systems configurations into three groups as listed on the left side of Fig. 4-31. In the system (a), both sending and receiving ends contain a generator,

i.e. a voltage source. In the system (b), the receiving end has only a power load, i.e. a current source. Similarly, in the system (c), the sending end is a current source. Therefore, three types of line emulation exist, i.e. (a) current/current source pair, (b) current/voltage source pair, and (c) voltage/current source pair.

To link the two-area system via a line emulator, there will be 9 combinations. However, intuitively and also for the sake of stability concern, it is better to couple the voltage source and current source, i.e. using a voltage source to interface with a current source, vice versa. Following this principle, three emulation schemes are provided in Fig. 4-32. Which scheme should be adopted is of importance to the system design, implementation, and stability. In a typical two area system, where both ends usually have generators and loads, the system (a) is more common. However, in some special operation conditions, where one end has lost all generators and has only loads, the scheme (b) or (c) should be better. Regardless of the system differences, one advantage of the scheme (a) is that since the emulator always interfaces the two ends as voltage-controlled-current-sources, only current control mode is needed, while the other two schemes may have to be combined and transitioned from one control mode to the other mode to ensure normal operation as system conditions change. For simplicity, only the scheme (a) is considered in this work.

As for the scheme (a), there are also two types of emulation schemes, i.e. the phasor domain and time domain based model. In the following sections, interface stability issues of both schemes are addressed. Similar stability analysis can also be applied to other schemes.

4.5.2 Stability issue in phasor domain based emulation

Ideally, if the current-controlled line emulator only interfaces with the ideal grid with zero impedance, then this system is robust, and no stability issue arises. However, as illustrated in the simplified equivalent two-area transmission system in Fig. 4-33, a converter based emulator is not

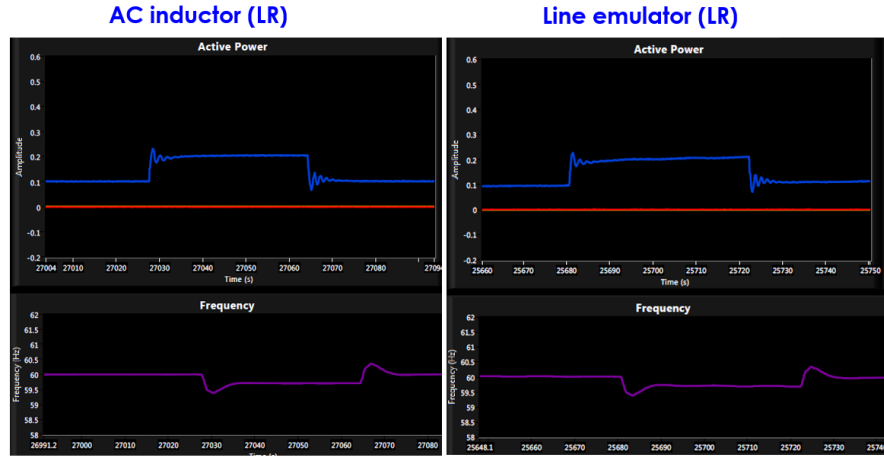


Fig. 4-30. Comparison of power flow between inductor interfaced and BTB emulator interfaced two-area systems.

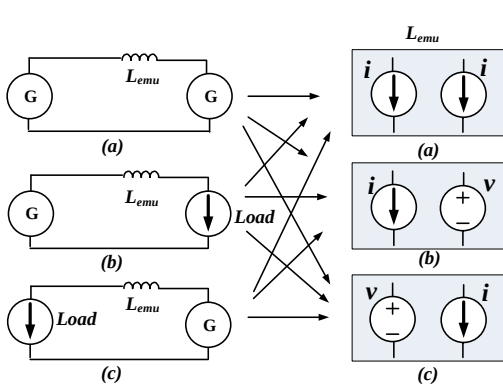


Fig. 4-31. General system configurations and emulation schemes.

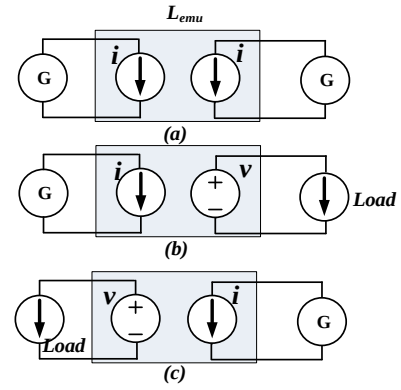


Fig. 4-32. Preferred emulation configurations.

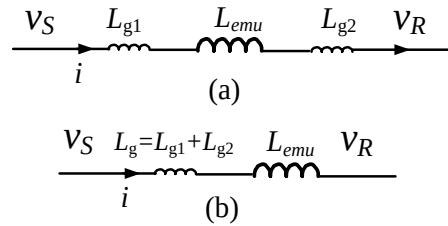
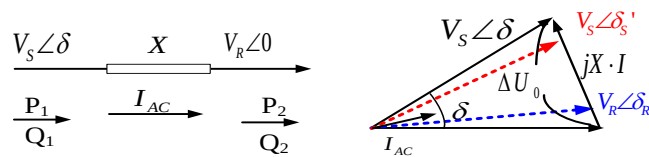


Fig. 4-33. Equivalent transmission line impedance when line emulator interfaces with two HTB grids. (a) Interface with two grids with serial impedance. (b) Simplified impedance circuit.

To better illustrate the stability issue, first, the phasor domain based model is analyzed in brief. Here, power flow at the two ends is calculated based on the steady-state phasor vectors. Therefore, only slow dynamics can be observed. Even so, if the external impedance is considered, the system may still lose stability.

$$I = \left(\frac{S_1}{V_s} \right)^* = \frac{P_1 - jQ_1}{V_s} \quad (4-25)$$

$$I_k = \frac{\Delta U_0 - jX_g I_{k-n}}{jX_{emu}} = (1 + \frac{L_g}{L_{emu}})I_0 - \frac{L_g}{L_{ref}}I_{k-n} \quad (4-26)$$



To ensure the convergence of (4-26), its eigenvalue should obey

$$\lambda = \left| \sqrt[n]{\frac{L_g}{L_{emu}}} \right| < 1 \quad (4-27)$$

which means if the external line impedance is larger than that of the emulated line, the emulation system will lose its convergence, leading to current oscillations. Moreover, due to the slow control law in the phasor domain, the stability issue is even more severe. As an example, if the impedance ratio is 0.5, but $n=20$, then λ will become 0.966, indicating a much smaller stability boundary.

4.5.3 Stability issue in time domain based emulation

The time domain based model is more useful for dynamic study. This paper will address its stability issue with three common digital implementations i.e. forward-Euler, backward-Euler, and trapezoidal discrete. Different from EMTP based software simulation, which adopts implicit discrete methods and solves full-element equations in large dimension matrices to attain better convergence and accuracy, hardware-based emulation with modular configurations focusing on real-time emulation does not know any external element information and has to rely on its real-time measurements from the interface to build up the real-time emulation models and consequently react. Thus, it has to use the current and past samplings as inputs to generate the next-step outputs due to the mechanism of PWM converter control, i.e. only explicit implementation is practical. Therefore, backward-Euler discrete will recede to forward-Euler, and trapezoidal approach need be modified as from (4-28) to (4-29) in order to correctly represent the real modeling processing.

$$i(k) - i(k-1) = \frac{\tau}{2L_{emu}} [v_{emu}(k) + v_{emu}(k-1)] \quad (4-28)$$

$$i(k) - i(k-1) = \frac{\tau}{2L_{emu}} [v_{emu}(k-1) + v_{emu}(k-2)] \quad (4-29)$$

$$v_{emu}(k) = v_s(k) - v_g(k) - v_R(k) \quad (4-30)$$

And different from (4-29) for the emulated main inductor, the voltage drop of the external physical line inductance varies instantaneously. As an analog signal, it should be modeled as

$$v_g(k) = L_g \frac{i(k) - i(k-1)}{\tau} \quad (4-31)$$

From above, the discrete differential equation is obtained as a second-order system,

$$[i(k) - i(k-1)] + \frac{L_g}{2L_{emu}}[i(k-1) - i(k-2)] + \frac{L_g}{2L_{emu}}[i(k-2) - i(k-3)] = 0 \quad (4-32)$$

And its eigenvalues are,

$$\lambda_{1,2} = \frac{-\alpha \pm j\sqrt{4\alpha - \alpha^2}}{2} \quad (4-33)$$

where,

$$\alpha = \frac{L_g}{2L_{emu}} \quad (4-34)$$

To maintain stability, the criterion is provided,

$$|\lambda| = \begin{cases} \sqrt{\alpha} & (0 < \alpha < 4) \\ \sqrt{\frac{\alpha^2}{2} - \alpha} & (\alpha > 4) \end{cases} < 1 \quad (4-35)$$

And the final solution is

$$\alpha = \frac{L_g}{2L_{emu}} < 1 \quad (4-36)$$

4.5.4 Stability issue in time domain based emulation with pure active load

In the above analysis, two ac grids are only considered as two voltage sources; however, in a typical system, there are definitely certain active loads at the receiving end, since generators are usually not assumed to take in power. To match with the experimental condition and also to illustrate the generic stability trend when connecting a load, a simple two-generator, one-active-load emulation system is configured, as shown in Fig. 4-35.

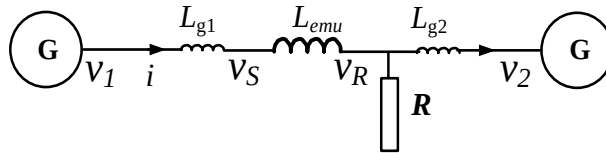


Fig. 4-35. A simple two-area system with an active load.

The discrete-time approximation procedure is similar to the above, except that the current of the rightward inductor L_{g2} now becomes

$$i_2 = i - v_R / R \quad (4-37)$$

And

$$v_R = v_1 - (L_{g1} + L_{emu}) di / dt \quad (4-38)$$

$$v_{Lg2} = L_{g2} \frac{di}{dt} - (L_{g1} + L_{emu}) \frac{d^2i}{dt^2} \quad (4-39)$$

To ensure the true stability status, it is recommended to use the symmetric secondary derivative. The final homogeneous second-order differential equation can be derived as,

$$\begin{aligned} & \left(1 + \frac{L_{g2}(L_{g1} + L_{emu})}{2L_{emu}R} \right) [i(k) - i(k-1)] + \frac{L_g}{2L_{emu}} [i(k-1) - i(k-2)] \\ & + \left(\frac{L_g}{2L_{emu}} - \frac{L_{g2}(L_{g1} + L_{emu})}{2L_{emu}R} \right) [i(k-2) - i(k-3)] = 0 \end{aligned} \quad (4-40)$$

Though the coefficient terms are a bit complicated in this case, the stability zone is actually extended, due to the resistive damping which can be perceived from the circuit perspective.

4.5.5 Experimental verification

To verify the stability analysis, four tests with the emulation line impedance step change from 10.7 mH, 5 mH, 2.5 mH, and 1mH are compared in a system as shown in Fig. 4-36, based on the scenario analyzed above. Also, with this information, the root locus of (4-40) can be obtained in Fig. 4-37. Derived system stability zone with test parameters. It marks that below 1.1 mH, line emulator will enter its instability zone. This matches the following test result. As we can see from Fig. 4-38, when inductance reduces to 1 mH, current oscillation occurs, indicating the transmission line emulation system loses its stability. Within the confined stable region, the line emulator is now extended to a multi-line system, successfully interfacing three-area system, as demonstrated in the HTB platform in Fig. 4-39.

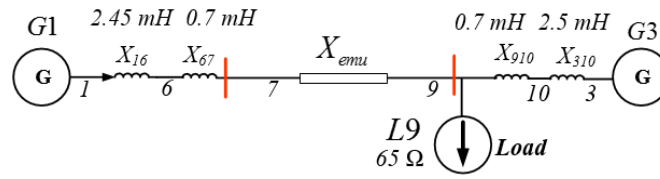


Fig. 4-36. System schematic and configuration for stability test.

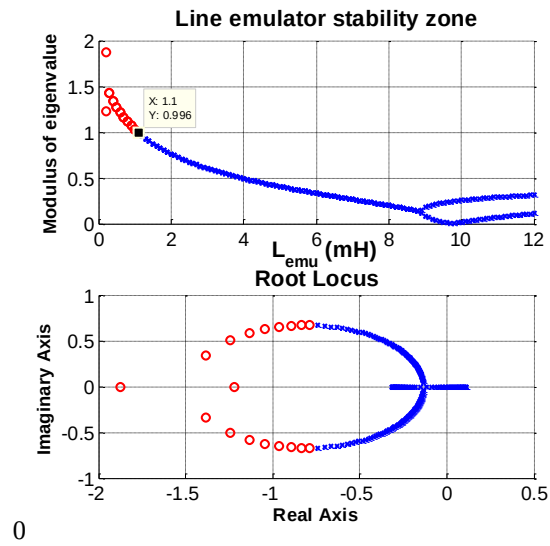


Fig. 4-37. Derived system stability zone with test parameters.

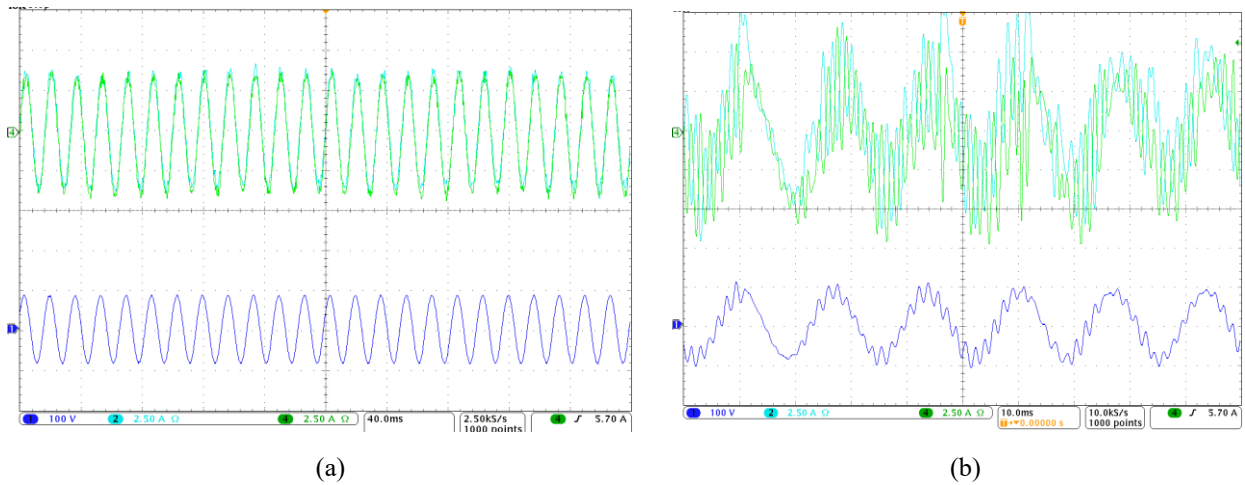


Fig. 4-38. Emulation stability test under different line inductances. (a) Emulation inductance = 2.5 mH. (b) Emulation inductance = 1 mH. Ch1: ac line current. Ch4: ac line-line voltage.

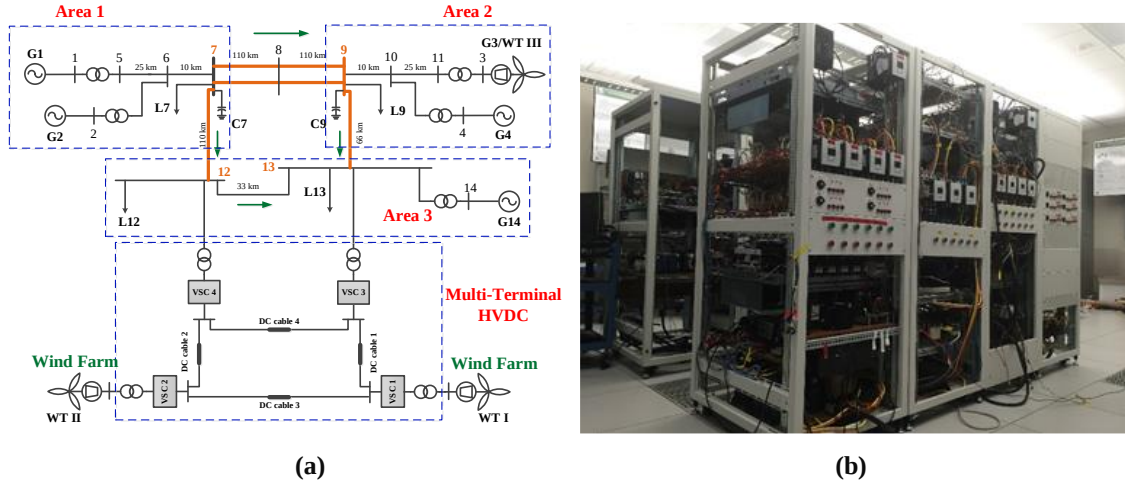


Fig. 4-39. One transmission line cluster including three back-to-back line emulators from bus 7-9, 7-12, and 9-13 in a three-area emulated power grid. (a) single-line diagram. (b) photo of the line-emulator-interfaced hardware testbed.

4.6 Summary

Interfacing VSI emulated transmission line to modular inverter based grid emulation network has been successfully achieved, through a series of control and modeling efforts.

The three-phase transmission line is simplified as a single two-port network for both lumped line and distributed line models. By using voltage-controlled current source or current-controlled voltage source principles, BTB converters can emulate the terminal behavior of three-phase lines. A steady-state focused phasor-domain line emulation approach and an instantaneous time-domain approach are analyzed and experimentally verified showing good steady and dynamic performance. The emulation approach is proved universal to general PI-section line model and distributed line model and is furnished with a dedicated communication strategy to mitigate the delay impact. Interfacing with a noisy HTB grid, it is found that both the switching frequency sensing harmonics and dc bias show significant impact on the terminal behavior of the line emulator, either introducing low frequency power ripple or shifted dc current distortion onto the terminal flow of the line emulator. These impacts need be properly mitigated by using the proposed sampling

scheme and offset controller. In addition, interfacing the external grid is not necessarily stable. The ratio of the emulated line impedance over the external line impedance that the line emulator connects with is an important stability indicator. The stability analysis for different emulation schemes, different interfaced power networks, and their corresponding stability criteria are presented, providing a good design guideline. Paralleling the active load branch in the system will help damp the interconnected line emulation system and extend the stable region and allowed impedance range of the line emulator.

5 GaN-Based Two-stage Aircraft Charger Interfacing with Aviation Grid

The charger design is complicated when its output has to provide two dc levels, both 28 V and 270 V, following the universal charger concept [302]. Both the front-end and dc-dc stage must be carefully selected, designed, optimized, and collaboratively controlled under all input and output voltage combinations, especially when high switching speed WBG devices are applied, and high density, high efficiency, and high performance are pursued.

The relation between harsh operation environment caused by ‘high dv/dt , di/dt , high frequency’ and sensing/sampling/control will be investigated, identified, and established. And associated interface challenges in WBG based high switching frequency converter will be thoroughly addressed. Principles and mitigation methods from sensing, sampling, and modulation aspects are proposed and verified.

In addition to the above control related issues, impacts of high speed high switching device on loss, thermal design, and EMI filter design in a two-stage charger converter consisting of three-phase Vienna-type PFC and three-level LLC will also be discussed.

5.1 Topology evaluation for GaN based universal charger

Based on the literature review and available GaN devices, six topologies have been reviewed in this universal charger design. First, considering wide output range and high power efficiency requirement, one stage power conversion is not favored. Two-stage architecture is more promising, as shown in Fig. 2-15.

Six topologies listed in Table 5-1 are compared. They can also be categorized into three architectures: 1) phase-modular architecture; 2) three-level boost-buck architecture; 3) two-level buck-boost-buck architecture.

As shown in Fig. 5-1, the first candidate utilizes the standard single-phase PFC, thus it has inherent advantages such as modular design capability, mature control, redundancy to single phase loss, and low voltage stress. However, the disadvantage is that it has more semiconductor devices, more filters, and transformers.

The second topology shown in Fig. 5-2 shares the advantages of modular converters, and it also reduces the passive and active devices on the secondary side. However, its disadvantages are complicated transformer design with three primary windings and two secondary windings, and interaction among three modules on the primary side. Due to the potential mutual magnetic coupling induced by the three primary side windings on one transformer, the circulating current may be unavoidable as well.

The third candidate in the phase-modular architecture is shown in Fig. 5-3. Different from the above solution, it eliminates the multi-winding transformer, but no isolation will be provided. Besides, to prevent abnormal current flow due to the interaction among three phase modules, an extra diode has to be added in each dc-link, increasing the device numbers and conduction loss. For this topology, since it shares the common intermediate dc-bus, the dc-link voltage should be at least twice the peak input voltage, which is 665 V assuming 235 Vac. This means 600 V/650 V GaN devices are not applicable.

Table 5-1. Topology candidates for a universal charger

No.	Topology
1	Phase-modular converters paralleling at isolated dc-dc converter output
2	Phase-modular converters paralleling at transformer primary side
3	Phase-modular converters paralleling at boost converter output
4	Single-switch three-phase rectifier and three-level dc-dc converter
5	Three-level boost-buck converter
6	Two-level buck-boost-buck converter

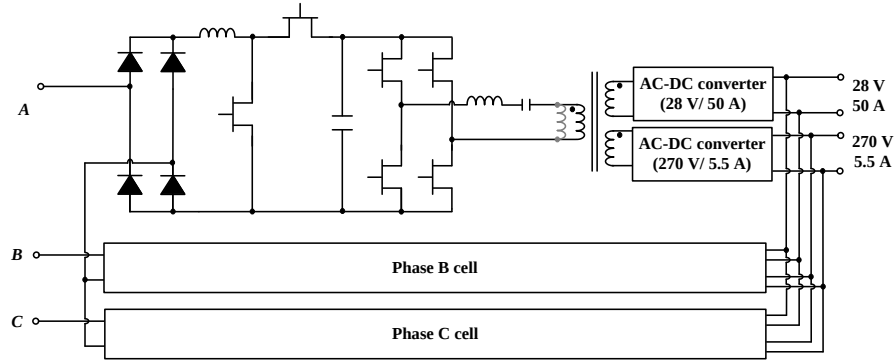


Fig. 5-1. Topology of phase-modular converters paralleling at isolated dc-dc converter output.

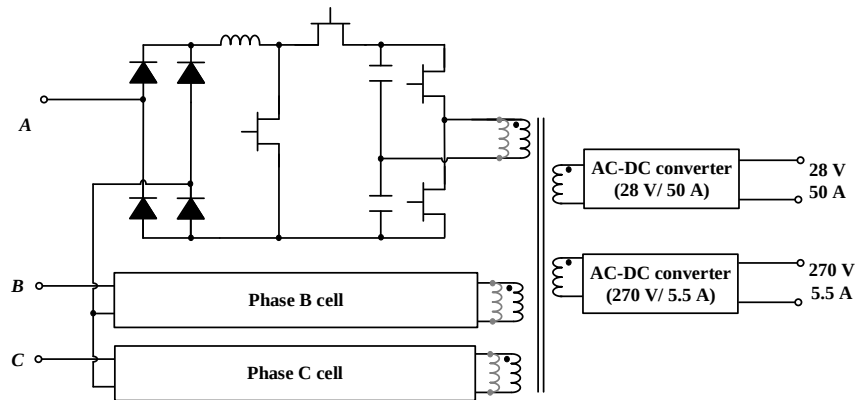


Fig. 5-2. Topology of phase-modular converters paralleling at the transformer primary side.

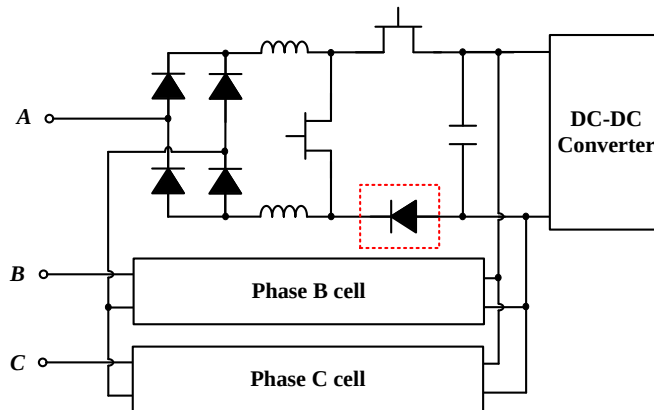


Fig. 5-3. Topology of phase-modular converters paralleling at boost converter output.

The three-phase ac-dc PFC as the front-end is also considered. Fig. 5-4 shows this single-switch solution for the ac-dc stage. Although this topology has fewer switches than traditional three-phase PFC, a large 5th harmonic in input currents is observed in Fig. 5-5, requiring large input filter in order to achieve good current quality.

Three-level PFC is also a promising solution. Fig. 5-6 shows a well-known Vienna-type PFC plus a proposed dc-dc stage with three-level dual mode Buck/LLC. The main feature for this architecture is it has only half dc voltage stress for GaN devices, and boost inductor is small, lower voltage harmonics due to the three-level structure. However, its control becomes more complicated than the other single-phase solutions or conventional three-phase rectifiers.

The last architecture is the two-level buck-boost-buck converter. It consists of a three-phase buck rectifier as input, a buck type LLC converter as output, and in between there is a boost converter. There are three control modes for this topology, as shown in Table 5-2. This converter has smaller EMI size, small voltage stress on the dc-dc side, and simpler dc-dc stage. However, high voltage stress is imposed on buck rectifier, with 499 V on the switch and 576 V on the diode. Besides, high conduction loss is consumed by the serial diodes.

Based on previous analysis, three topologies shown in Table 5-3 are selected as candidates for further evaluation and comparison. The evaluation approach is shown in Fig. 5-8. By going through the whole design procedure for each candidate topology, following the same standard, and comparing the best design results, the optimal topology can be selected. The final evaluation results are given in Table 5-4 and Table 5-5. Efficiency comparison among optimal design results of three candidate topologies., respectively, for weight and efficiency under four different voltage modes. As weight is the most important specification of this project, the three-level boost-buck topology consisting of three-level three-phase Vienna-type rectifier and there-level buck/LLC

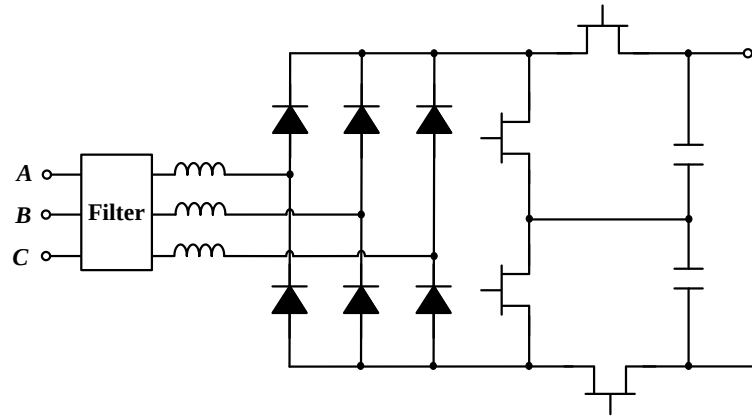


Fig. 5-4. Topology of single-switch PFC boost rectifier and three-level dc-dc converter.

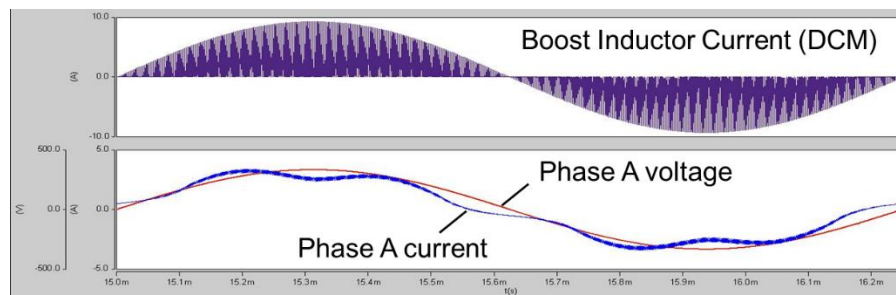


Fig. 5-5. Simulation waveforms of single-switch PFC boost rectifier.

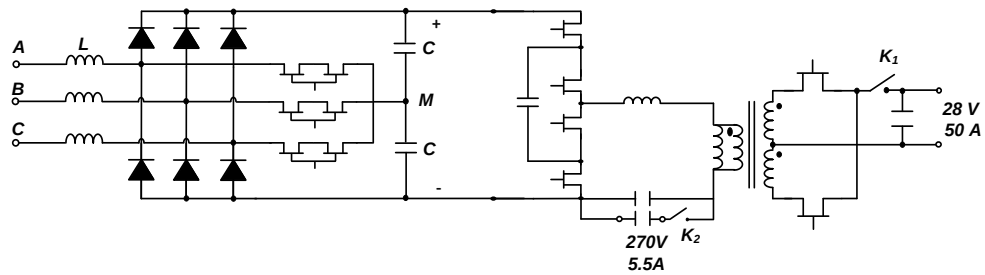


Fig. 5-6. Topology of three-level boost-buck converter.

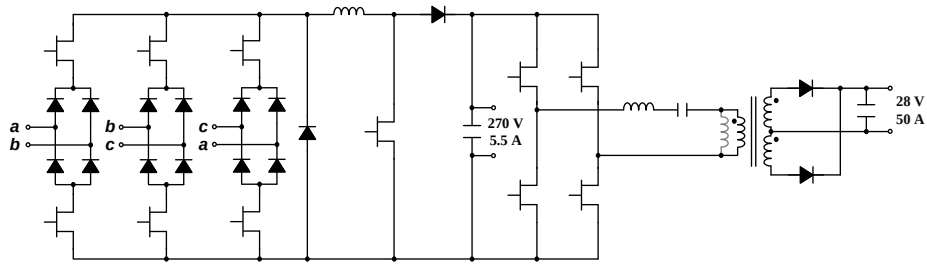


Fig. 5-7. Topology of two-level buck-boost converter.

Table 5-2. Operation mode for two-level buck-boost-buck converter.

Input	Output	Involved Circuits
235 Vac	270 Vdc	Buck
115 Vac		Buck + Boost
235 Vac	28 Vdc	Buck + LLC
115 Vac		Buck + LLC

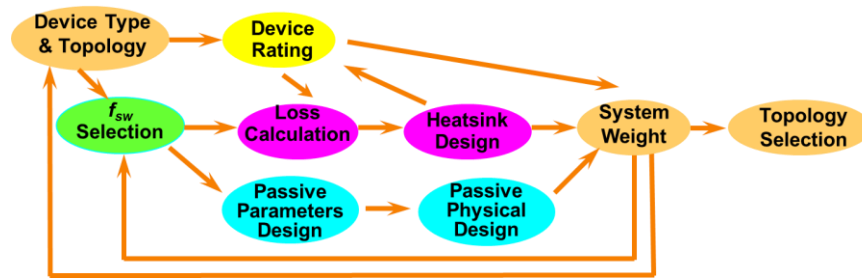


Fig. 5-8. Topology evaluation approach.

Table 5-3. Comparison of six topologies from different aspects.

Topology	Ac input filter	Transformer	Dc link passives	Control complexity	Voltage stress
Phase-modular converters paralleling at isolated dc-dc converter output				good	good
Three-level boost-buk converter		good	good		good
Two-level buck-boosst-buck converter	good	good		good	

Table 5-4. Weight comparison among optimal design results of three candidate topologies.

Topologies	Ac-dc stage	Dc-dc stage	Total
Phase-modular topology	495 g 900 kHz Transphorm GaN	333 g 1 MHz Transphorm GaN	828 g
Three-level boost-buck topology	227 g 1.2 MHz Transphorm GaN	267 g 500 kHz Transphorm GaN	494 g
Two-level buck-boost-buck topology	348 g 900 kHz Transphorm GaN	209 g 1 MHz Transphorm GaN	557 g

Table 5-5. Efficiency comparison among optimal design results of three candidate topologies.

Topologies	Voltage modes	28 V _{dc}	270 V _{dc}
Phase-modular topology	115 V _{ac}	90.4%	90.3%
	235 V _{ac}	94.7%	94.6%
Three-level boost-buck topology	115 V _{ac}	92.2%	93.9%
	235 V _{ac}	94.3%	96.1%
Two-level buck-boost-buck topology	115 V _{ac}	92.2%	95.3%
	235 V _{ac}	93.5%	96.6%

converter is finally adopted for the charger system, since it achieves the lowest weight, with power efficiency only a bit lower than the two-level buck-boost-buck topology.

It should be emphasized that these design results should be mainly for comparison study, they do not reflect the actual implementation, partially because the devices and components chosen at the early stage might not be adopted in the final optimal design of the specific converter due to component availability issue or other further improvements.

5.2 Impact, mechanism, and mitigation of sensing distortion in HF converter

As already discussed in section 2.3.3.1, high di/dt , dv/dt and high frequency in GaN based converter worsen the operation environment of sensing and sensor circuit. In this work, an in-depth exploration and analysis of the troublesome sensing distortions that often haunt power engineers will be presented, disclosing the interior correlations among unexpected power behaviors, high switching speed characteristics of WBG devices, and high-frequency hard-switching operation.

Instead of further stressing the high frequency noise itself, the focus will be on identifying how these high frequency distortions impact on the low frequency or dc feedback voltage and currents, either dc side or ac side, eventually leading to the deviated loop control track, and on mitigating these noises in different situations. Considering the well-known fact that feedback control has no rejection capability for disturbances in the feedback path, this topic is crucially important.

5.2.1 Introduction

Sensing and control signals may inevitably suffer from high frequency noises, due to capacitive coupling from high dv/dt and inductive coupling from di/dt . However, the impact from these noises was not properly considered in the past, since it was typically thinking a moderate low pass filter before the ADC would mitigate the influences of these high frequency noises on

converter control, e.g. setting filter bandwidth below half switching frequency to avoid aliasing effect. Through experimental study in this work, it reveals that in high speed GaN device applications, these high frequency ac noises could surprisingly induce nonlinear dc or low frequency shift through the sensing and conditioning circuitry and eventually lead to deviation from the nominal control track and distorted ac current, if without a proper circuit design and layout. A deeper understanding of these effects is the basis to guide the sensing design, layout and control. To address the issues of sensing in the noisy operation environment, causes of the low frequency bias and dc bias on sensing signals are firstly disclosed, of which two distortion mechanisms are mainly investigated.

5.2.2 Dc bias from analog signal isolation amplifier due to high common mode dv/dt

5.2.2.1 Origin of dc bias from analog signal isolation amplifier

Fig. 5-9 shows a typical isolated voltage/current sensing scheme in the case where isolation is mandatory. An analog isolation amplifier (iso-amp) is usually adopted to achieve the isolation between control and power domains. At the high-power side of an iso-amp, the voltage will be sampled by a resistor divider in a single-end form or by a divider pair in a differential form. And current will be sampled through a shunt resistor. Then, the isolated sensing signal is processed by downstream conditioning amplifiers and filters before transmitting to ADC. A high CM voltage isolation barrier exists between the two sides of iso-amp due to the different grounding potential. The magnitude of this CM voltage is determined by the dc link voltage and the CM impedance distribution along the whole CM path, including related grounding parasitics, transformers if existing, and the isolation capacitance of the iso-amp. The slopes of this CM voltage caused by dv/dt of the turn-on and turn-off switching transients are determined by the specific gate driver,

gate resistance, switching speed, and dc-link voltage. The turn-off dv/dt is also strongly impacted by the switching current level during switching loop commutation.

The basic structure of an analog iso-amp is shown in Fig. 5-9, where the analog input is modulated into digital format, e.g. via a sigma-delta ADC at the primary side and reconstructed to analog output via a demodulator at the secondary side. An intermediate digital isolation barrier forms the signal transmitting medium with three different types of implementation. Using optical iso-amp as an example, when a rising $v_{CM,r}$ pulse is imposed on to an iso-amp, the internal coupling capacitance of iso-amp induces CM current penetrating the barrier, and a positive differential voltage spike is generated at the output through the pull-up resistor. In addition, the turn-off pulse also induces a negative spike $v_{CM,f}$ at the output. These spikes may falsely toggle the logic level, jeopardize the DM signal and demodulate corresponding analog spikes.

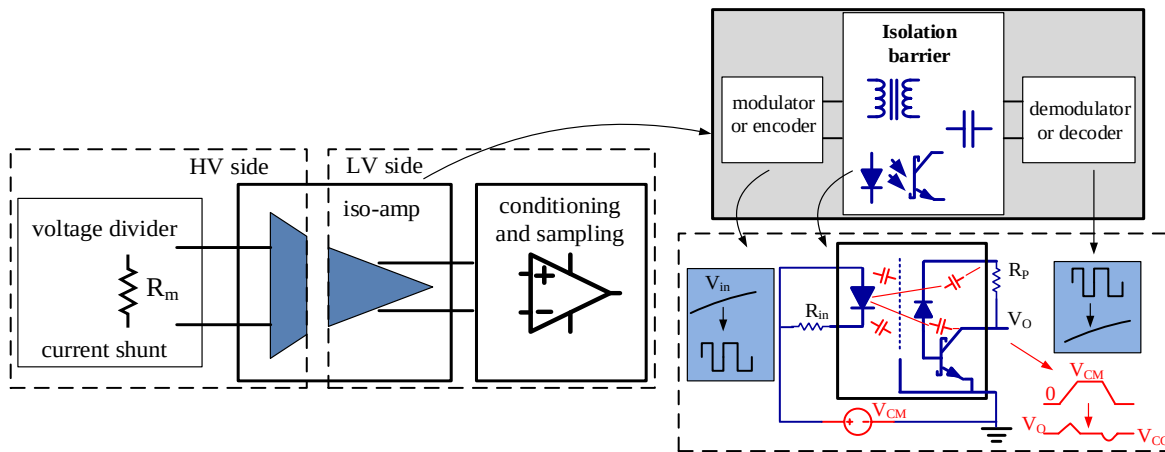


Fig. 5-9. Iso-amp function block and CM noise penetration.

$$\Delta v_{dc_out} = \int_0^{T_s} (v_{CM_r} - v_{CM_f}) dt / T_s \quad (5-1)$$

Therefore, the conclusion is a dc bias can be generated after the downstream filter as the average of the positive and negative spikes. This relationship is disclosed in (5-1). It should be noticed that the polarity of the spikes could be reversed depending on internal configurations of an iso-amp IC.

Based on a series of conducted experiments, further insights into the cause of this type of dc bias are provided.

If the turn-off dv/dt is the same as the turn-on dv/dt , it seems reasonable that a minimum induced dc bias might be expected, per (5-1). However, for a given device, the turn-on dv/dt is mainly determined by the gate drive speed, while for the turn-off, dv/dt is eventually up to the slower one between gate drive and junction capacitor charging during the turn-off commutation, which might be slower if the load current level is low. Moreover, the turn on and off of the device itself does not strictly follow the same speed. For GaN based application, this situation becomes worse. The turn-on transient for 650 V e-mode GaN device is usually less than 10 ns, and dv/dt can be above 100 kV/us, while its turn-off transient could last for hundreds of ns at ac current zero crossings [157, 186]. Thus, turn-on dv/dt becomes the primary contributor to the CMTI issue instead of the turn-off dv/dt at low current level or zero crossing. This is further confirmed from experimental results of LLC voltage sensing at two different switching frequencies of front-end PFC under the same operating conditions. As shown in Fig. 5-10, the negative spikes which are below the desired voltage sensing level as marked in dashed magenta line, are almost the same for both cases, but no positive peaks show up except for some noise.

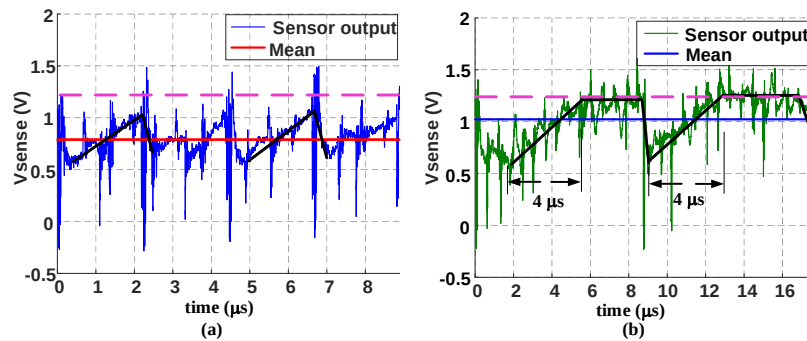


Fig. 5-10. LLC voltage sensing distortion: (a) 450 kHz PFC; (b) 450/4 kHz PFC. Black line outlines the profile of the output signal. Dashed-line is the desired voltage.

The above results highlight another important distortion factor which was not considered, i.e. the output signal rise/fall time of an iso-amp IC. Ideally, the output spike due to dv/dt should only occur at the switching transient, however, it is noticed that at both switching frequencies, output spikes linearly increase from the same negative valley. This can be explained by the output rise time of iso-amp ACPL-C87B, roughly 4 μ s [303]. In 112.5 kHz case, dv/dt related spike returns to the steady-state desired dc voltage. While in 450 kHz case, the dv/dt induced spike is reset by the next switching event before it reaches the steady state level. Therefore, some other useful conclusions can be obtained:

The speed of iso-amp, i.e. the rise/fall time impacts the sensing output distortion induced by CM spikes. More instantaneous distortions and dc bias will be induced when adopting higher switching frequency, lower speed sensing iso-amp, and higher speed devices.

Switching frequency will not impact the peak spike of an iso-amp output, yet it does impact the dc bias level, because: 1) the same noise spike pattern will be averaged over different switching periods; 2) noise spike of iso-amp may not reach the correct sensing level in one higher switching cycle. Therefore, high frequency induces more dc sensing shift.

To further demonstrate the switching frequency impact, actual sampling voltage of LLC output processed by DSP are compared at the above two frequencies. As shown in Fig. 5-11, at 450 kHz, the sampled dc voltage has much higher dc bias error than that at 112.5 kHz.

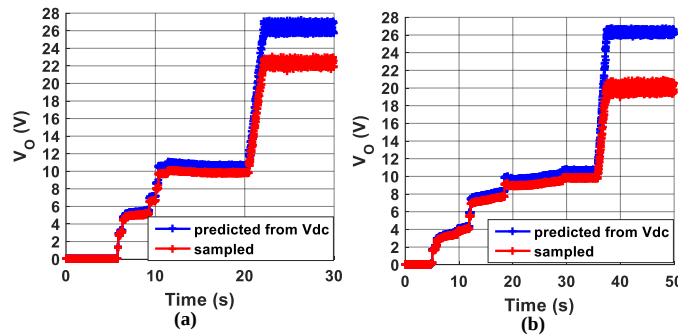


Fig. 5-11. Experimental results of LLC output voltage sampling: (a) 450/4 kHz PFC; (b) 450 kHz PFC.

5.2.2.2 Impact on feedback control

It is well known that feedback control can suppress the disturbance in the forward path but has no rejection capability in the feedback path. For a feedback closed-loop control, the controlled voltage or current will be forced by the controller to track the reference, as given in

$$V_{ref} = V_{sense} = V_{actual} + \Delta V_{dc} \quad (5-2)$$

Thus, the actually controlled voltage will be lower than the desired value as in (3), and this dc error can be even larger when dc-link voltage increases, appearing as if a nonlinear voltage dependent sampling gain exists. For a high step-down dc-dc application using WBG devices, this dc error would be unacceptable.

$$V_{actual} = V_{ref} - \Delta V_{dc} \quad (5-3)$$

5.2.2.3 Mitigation solution

Unfortunately, the CMTI of an analog iso-amp is relatively low than GaN device turn-on dv/dt and is also defined at a rough level [303, 304]. No information can be obtained in terms of different error levels vs CM voltage and dv/dt, further challenging sensing circuit design. The state-of-art commercial voltage sensing iso-amp has typical 15 kV/us CMTI [303] using optocoupler isolation, and current sensing iso-amp has up to 75 kV/us CMTI [304] using CMOS isolation. Thus, CMOS based iso-amp seems to be the better option currently, since it shows higher CMTI.

To obtain accurate voltage sampling quality in high dv/dt operation, a high CMTI current sensing iso-amp can be reconfigured for voltage sensing. However, the internal input resistance of this shunt-input iso-amp is found much lower than the voltage sensing iso-amp, e.g. 20 k Ω , thus resistance value of the voltage divider should be properly selected, considering trade-off between sensing accuracy in terms of load dependence and extra loss introduced by sensing resistors.

5.2.3 Bias from RF interference rectification in op-amp

5.2.3.1 Identification of observed sensing

In the era of silicon device with tens of kHz switching frequency, the sensing design can be quite straightforward, a moderate filter implemented in the conditioning circuit is sufficient to guarantee the integrity of feedback signals. However, when using the similar design principles in GaN based converters, the experimental results in this paper reveal that the voltage and current sensing signals along the conditioning circuitry could see a pronounced dc offset or low frequency distortion, which grows as dc bus voltage and switching frequency increases. An example of ac current sensing at 450 kHz and 112.5 kHz switching frequencies in an e-GaN Vienna-type rectifier is provided in Fig. 5-12, where the sampling signal outputted by DAC has much difference from the probe result. At higher switching frequency, this low frequency or dc shift becomes larger.

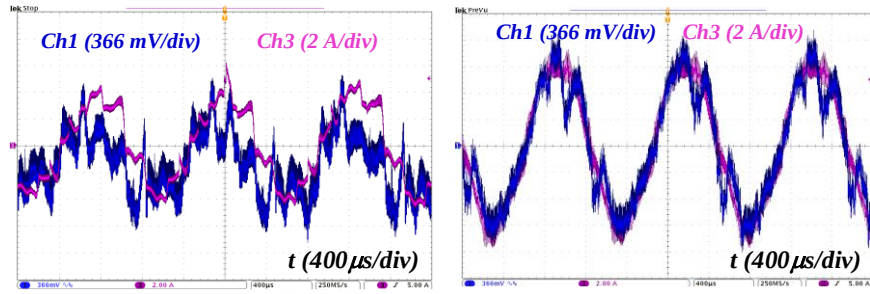


Fig. 5-12. Experimental waveforms of ac current sampling: (a) 450 kHz PFC; (b) 450/4 kHz PFC. Ch1 is the sampled signal, Ch3 is the probe result.

To identify the cause of this distortion, the output signal of the hall sensor is checked. High switching transient noises are observed in the sensor output as shown in Fig. 5-13. Since the onboard sensor is placed close to the main power loop, the noise is found induced by high di/dt of switching transients. And noise at turn-on seems more pronounced than that at turn-off, which can

be explained from the fact that at turn-off, commutation from off-device to on-device is largely determined by load current charging.

The sensor output, ADC sampling, and probe measurement are further monitored and compared. Through the comparison results, respectively from Fig. 5-14 to Fig. 5-15, both the sensor output itself and the final ADC sampling show low frequency or dc shift distortion. The complexity for this analysis is that coupled noise, as well as dc shift patterns, may be different at different operation points. However, some important observations are: 1) due to the HF noise coupled onto sensor output and its asymmetric nature as mentioned in Section 5.2.2.1, its mean value over a switching period can be shifted from the original level and falsely conveyed to the following conditioning amplifier; 2) this dc shift is thus impacted by switching frequency; 3) under certain conditions, since an offset also exists between the envelope of the sensor output and probe result, it indicates sensor itself is also affected by the HF noise. It must be also mentioned the poor quality of the ac current is due to several types of distortions to be discussed.

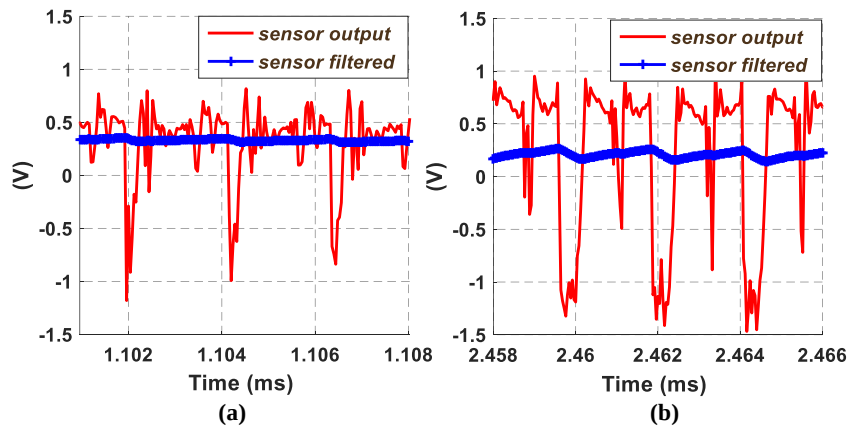


Fig. 5-13. Experimental waveforms of ac current sensor output with 450 kHz PFC. Due to 25 MHz low bandwidth probe used in the test, only the noise envelop is captured where even higher frequency oscillations are not accurate.

5.2.3.2 Origin of dc bias and low frequency distortion

Further experimental results verify that the severity of this dc distortion is determined by the amount of high di/dt induced noise picked up by signal-ground traces between sensor output and conditioning amplifier input. And the cause of this dc bias is radio frequency interference (RFI) or EMI rectification effect on operational amplifiers (op-amp) [305-312], a phenomenon seldom considered in the power converter field that the output of amplifier can induce a dc shift or low frequency response depending on the amplitude, frequency and continuity of the input coupled high frequency out-of-band noise, because of the nonlinearity of the input stage transistors. Furthermore, noise coupled at the output of an op-amp can also contribute to the input noise via its feedback path. This explains why dc shift at current sensor output was observed, as an internal op-amp exists at the output stage of the current sensor to provide desired quiescent bias [313, 314].

To ease the understanding of this rectification effect, a brief review is introduced. RFI rectification was firstly observed in naval research on the susceptibility of solid-state semiconductor devices such as transistors to microwave energy [306, 312]. Since then, the effects and mechanisms of RFI distortion on analog and digital ICs have been investigated both experimentally and theoretically, in both time domain and frequency domain [305-312]. Analog electronics, in particular, amplifiers are most susceptible to the EMI noise. Technical notes from industry have elaborated the dc bias effect on op-amp from its input transistor. The nonlinearity of a transistor has been attributed to its the transfer characteristics property, i.e. emitter-coupled BJT has stronger nonlinearity than source-coupled JFET or CMOS in terms of the exponential relation vs. the square relation [307, 311]. Although this can confirm observations that BJT based amplifiers typically have higher RFI distortion than other types, it failed to explain why this phenomenon only occurs at out-of-band frequencies and dc offset varies with RF frequencies. The frequency dependent

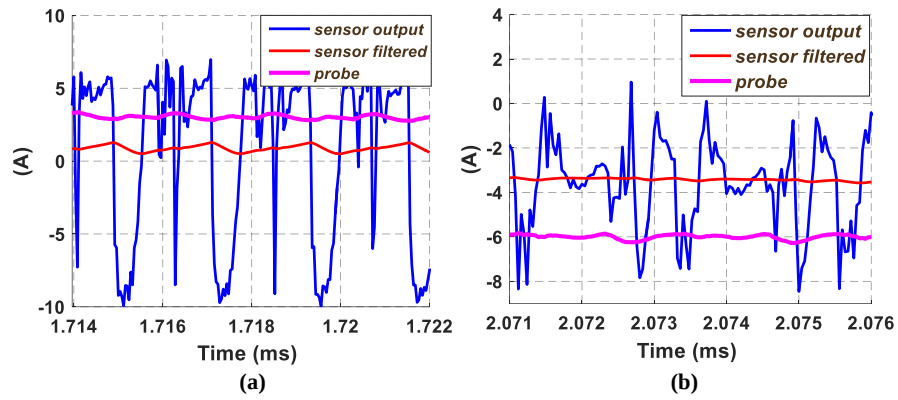


Fig. 5-14. Comparison between the sensor output and probe result at different current levels with 450 kHz PFC in the switching cycle scale.

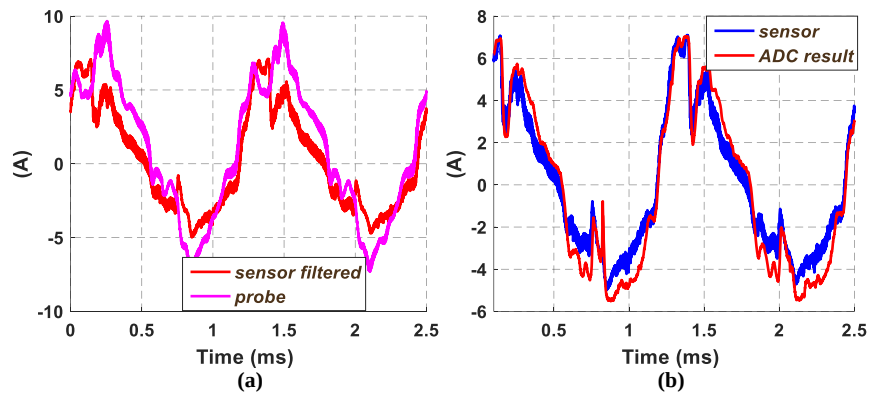


Fig. 5-15. Comparison of sensed ac current in line cycle scale with 450 kHz PFC: (a) comparison between the sensor output and the probe result; (b) comparison between the sensor output and the sampling result.

nonlinearity and dc bias level were later analytically modeled in [309] for a CMOS op-amp, indicating the parasitic capacitances C_{gs} of input differential pairs and their total source-to-ground capacitance are the determinants. The mechanism of negative feedback impact on dc bias was also revealed in [308, 309] for CMOS op-amp. It is also noticed that some of the models are only valid at low level RF input, where two transistors of the input differential pair are both in saturation region [308], while other models may be feasible for both the saturation region and the subthreshold region where large signal noise switches the transistor on and off [309].

In recent years, EMI rejection ratio (EMIRR) is standardized to evaluate the susceptibility of an amplifier to RFI [310], from which the corresponding dc bias can be estimated as (5-4). However, it is only valid at low amplitude EMI/RF [305].

$$\Delta V_{dc} = \frac{1}{10^{\left(\frac{EMIRR_{IN}(dB)}{20}\right)}} \left(\frac{V_{RF_peak}^2}{100mV} \right) \quad (5-4)$$

To further verify the RFI offset and evaluate EMIRR of the adopted op-amp OPA2227 with the cascaded inverting configuration in this work, offline tests are carried out using a signal generator and a $50\ \Omega$ cable to inject the ac EMI source. From Fig. 5-16, as RFI amplitude increases, dc shift becomes larger and occurs earlier. This offset also has nonlinear frequency characteristics. It grows larger as frequency increases from 500 kHz to 2 MHz. Then, it drops back to almost zero around 10 MHz. Test at the even higher frequency is not performed, due to measurement complexities involving reflection coefficients of input cable, PCB traces and op-amp pins.

5.2.3.3 Compound mitigation approaches

Due to the RFI susceptibility of op-amp inputs, a straightforward mitigation approach is to attenuate the EMI noise before the op-amp inverting and non-inverting pins. The built-in RC based CM and DM filter have been implemented in some commercial amplifiers [307]. However, its

filter corner frequency is usually above tens of MHz to fit general purposes, higher than the frequency range of the state-of-art GaN based power converter, thus a set of external EMI filter should be provided for converter sensing design, as shown in Fig. 5-17.

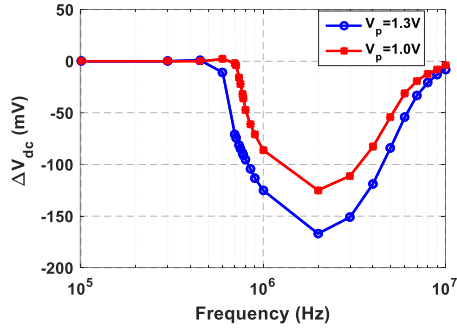


Fig. 5-16. Measured RFI dc offset in OPA2227 with cascaded inverting configuration.

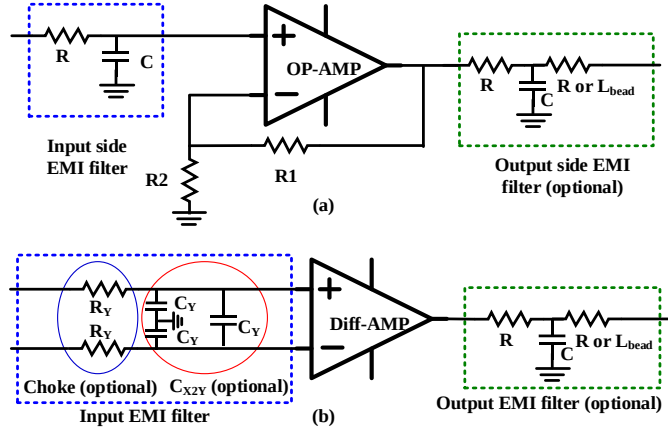


Fig. 5-17. Recommended filter approaches to mitigate amplifier RFI issue.

Unlike signal processing, power conversion deals with high voltage and current. Particularly, in GaN based converter, high di/dt , dv/dt and high frequency could likely induce strong noise coupling. Relying purely on filter itself is not effective enough to eliminate RFI noise without sacrificing sensing bandwidth. Direct control of the noise source and noise coupling path is more straightforward and effective. Taking current sensing distortion as an example, the noise at the signal interface side of the hall sensor is induced by high di/dt current circulated in the switching loop through space magnetic coupling. Given fixed di/dt , smaller power loop area generates less diffuse magnetic field, thus reduces magnetic coupling. However, less loop inductance can adversely induce higher di/dt and dv/dt [315]. In addition, if the orientation of the switching loop is arranged to be orthogonal to that of hall sensor interface loop and power supply loop, the coupling could also be reduced. Since power loop layout has been well studied in the past considering the trade-off between electrical and thermal performance, details will not be covered.

On the other hand, the emphasis of this paper is on the importance of signal loop layout for sensing design. In high density converter design, SMT hall sensor chip is preferred due to its low profile and weight. When it is placed on the power board close to converter terminals, longer traces of power supply nets and output nets are needed to interface with the control board and are prone to taking in the high di/dt noise through the magnetic field coupling and being disturbed by the induced voltage noise. Therefore, a vertical trace arrangement is proposed to minimize the area of two types of loops, and to ensure the cross section paralleled to flux orientation.

Two layout designs are provided. Compared to the design in Fig. 5-18 (a) with large VCC-GND loop and signal-GND loop on phase B and C, the improved current sensor layout for phase B and C is proposed in Fig. 5-18 (b). The first improvement is that multi-radial power lines are applied to all three sensor chips instead of the central power lines. This decouples possible noises among three-phases and ensures good power quality for each sensor. VCC lines for three sensors directly connect to the main VCC plane, and GND lines also start directly from the GND plane. In addition, all signals are embedded in the mid-layer and overlaid with power lines, to form vertical loops with minimized coupling area. And next to each sensor, reasonable size ground plane is also designed to provide a stable ground potential to each chip.

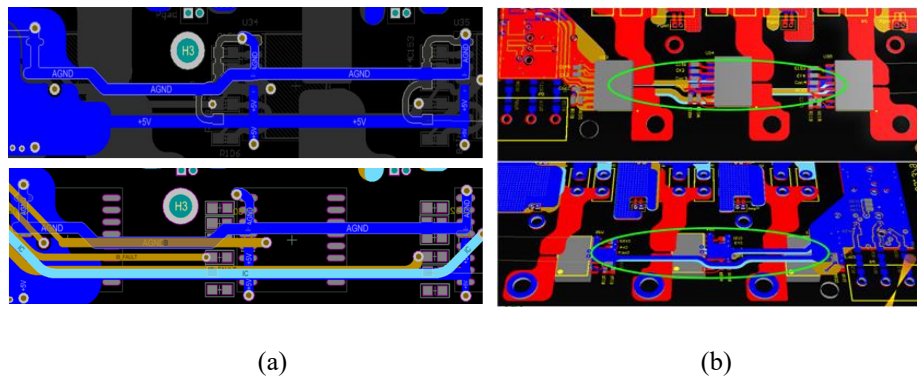


Fig. 5-18. Sensor layout comparison: (a) Large VCC-GND (upper) and signal-GND (lower) loops in the first version design. (b) Improved vertical layout from top view (upper) and bottom view (lower).

Since the magnetic strength is reversely proportional to the distance, another conservative but effective approach is to move hall sensors far away from the power loop, which is also experimentally verified at the expense of more board space.

Apart from di/dt inductive coupling noise, other noises also exist for hall sensors. For example, dv/dt capacitive coupling from high voltage side to the signal side of hall sensor IC via its isolation capacitance could also superpose significant noise onto the low-level sensor output [313, 314]. Recommendations are: 1) place hall sensors at non- dv/dt nodes, such as after filter inductors which absorb dv/dt in the first place; 2) choosing hall sensor chips with internal capacitive shielding can also avoid this type of distortion [313]; 3) adding proper filter for this HF noise is also suggested [314]. However, this alone may be ineffective, since a dc offset can still be produced if dv/dt patterns at turn-on and off are not symmetric, similarly to the mechanism disclosed in Section 5.2.2.

5.2.4 Dc bias due to RFI rectification in In-amp

Instrumentation amplifier (in-amp) is typically used for high voltage sensing where strong CM signals can be eliminated by the differential structure. However, the typical common mode rejection ratio (CMRR) of in-amps rolls off at 200 Hz, only remaining 20~30 dB at 100 kHz, and the best in-amp has only up to 20 kHz bandwidth [311]. If a strong radio frequency noise is coupled at the input and is not effectively suppressed, it can be rectified to a dc bias at the amplifier's input stage as well [312]. Similarly, effective RFI mitigation schemes are: 1) choose in-amp with higher EMI robustness; 2) add external EMI filter pair inserted at the input of in-amp using RC filter, choke, or X2Y-based capacitor, as shown in Fig. 5-17; 3) minimize both the differential-mode signal pair loop and the common-mode signal-GND loop between the sensing circuit and the in-amp.

5.2.5 Experimental verification

5.2.5.1 Dc voltage sensing due to dv/dt impact

A current iso-amp si8920 is configured to sample LLC output voltage, instead of using the prior voltage iso-amp ACPL-C87. Due to its high CMTI up to $75 \text{ kV}/\mu\text{s}$ and high speed (rise/fall time is $0.42 \mu\text{s}$), dc bias on the sensing signal is effectively suppressed over the whole operation range with two-stage 450 kHz hard-switching PFC and 850 kHz resonant LLC.

In addition, RFI rectification dc bias is also eliminated after minimizing all sensing circuit ground loops and the output differential pair loop. This is necessary as the inductive loop coupling can introduce high input voltage noise before the processing op-amp circuits as aforementioned in Section 5.2.3.

The final voltage sampling result is accurately controlled at reference value 27 V with 650 V dc-link bus voltage, as shown in Fig. 5-19, indicating significant improvement on the dc bias compared to the prior result in Fig. 5-11.

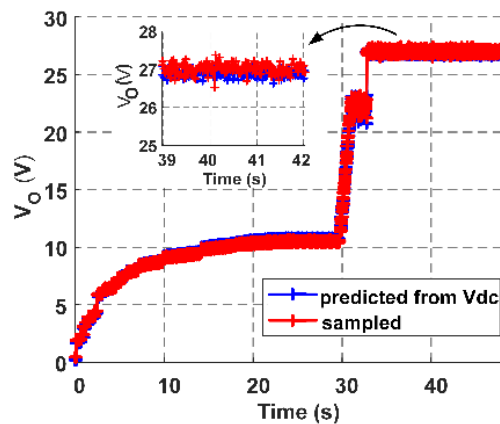


Fig. 5-19. Eliminated dc sensing shift and accurate dc regulation with the proposed sensing solution.

5.2.5.2 Ac current sensing due to RFI

To illustrate this di/dt effect and the improvement through the new layout approach, waveform comparison tested under 300 V_{dc}, 450 kHz without any compensation is provided. Fig. 5-20 (a) gives the output of sensing conditioning in the green curve and sampling result from DSP in the blue curve, with the first version layout. Disruptive distortion on the output of the current sensor was observed, compared to the result of the current probe in the pink curve. After adopting the new layout, all sensor outputs become clean, matching the actual shape of current waveforms obtained from current probes, as given in Fig. 5-20 (b). This lays a solid basis for current quality control.

The impact of current sensor distortion on current harmonic distribution is also provided in Fig. 5-21. Compared to the result with distorted current sensors, tested at 115 V_{rms} input, 600 V_{dc} output, 450 kHz, and 280 Ω load, the proposed layout improves sensor signal quality and thus reduces THD from 14% to 9% percentage points, without involving any proposed compensation [157] or sampling scheme yet.

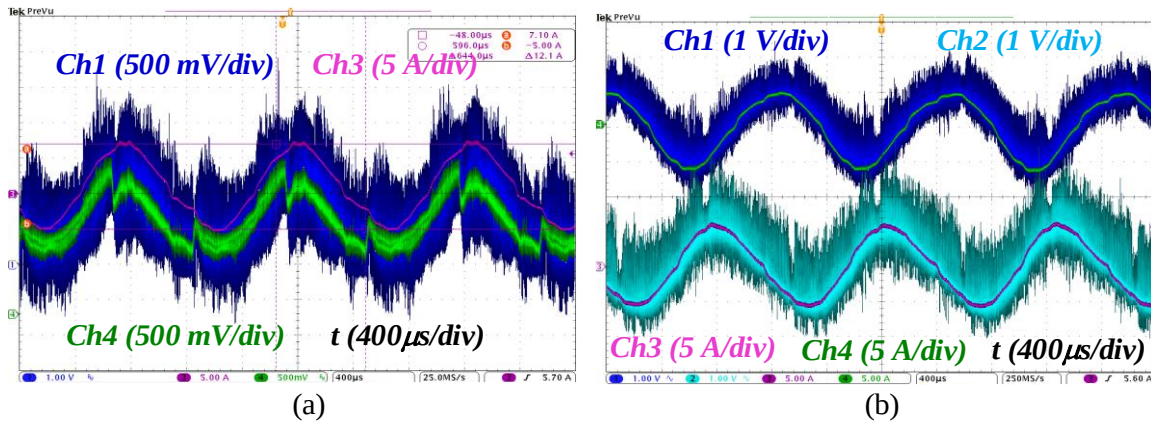


Fig. 5-20. Current sensing quality comparison from different layout schemes. (a) current sensing distortion based on the first layout. Ch1: sampled signal via DAC output; Ch3: current probe output; Ch4: conditioning output signal. (b) no sensing distortion based on the improved layout. Ch1 and Ch2 are outputs of hall sensors, Ch3 and Ch4 are outputs of current probes.

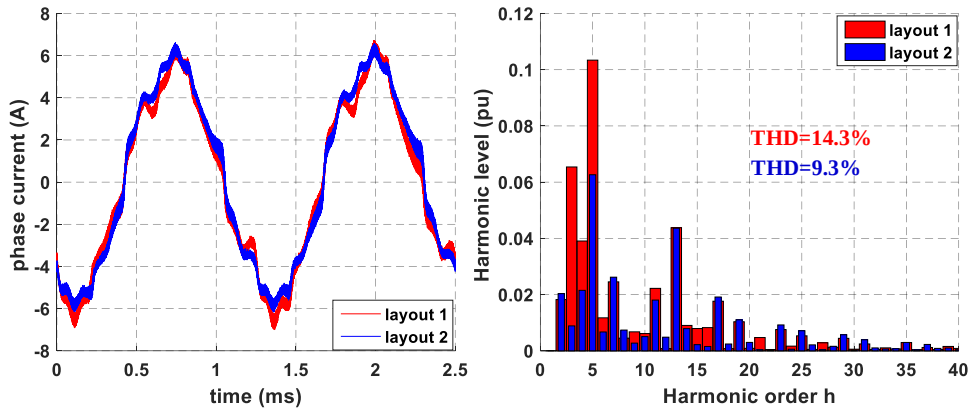


Fig. 5-21. Improved current THD with the proposed sensor layout avoiding high di/dt noise coupled from the power switching loop.

5.3 Improved sampling scheme for distortion mitigation in high frequency converter

Another challenge in applying GaN into high frequency high density ac/dc converters is sampling. It is well-known the integrity of sampled current and voltage signals is the basis for converter feedback control. However, because of high switching speed of GaN devices, high dv/dt and di/dt related transient noises and ripples are augmented in hard switching three-phase ac/dc. In addition, at high frequencies as ADC conversion time becomes relatively long, sampling timing shows sensitive impacts on current quality control.

In this section, taking three-phase Vienna-type rectifier as an example, the conflict of synchronizing sampling instants with triangle carrier-based modulation among three phases is addressed and a sector-based scheme which can be applied generally to general three-phase converters, is proposed and analyzed to avoid the switching transient noises and ripples induced by dv/dt , di/dt of high switching speed devices during hard switching operation.

5.3.1 Issues in existing sampling methods

5.3.1.1 PWM modulation implementation in DSP

Since the triangle-carrier-based modulation is widely adopted in DSP coding and acts as the synchronization source of sampling instants, the implementation of the well-known 2-stack carrier-based modulation in DSP for three-level Vienna-type converter is first presented. To avoid the negative region of the carrier, an equivalent modification can be made as shown in Fig. 5-22.

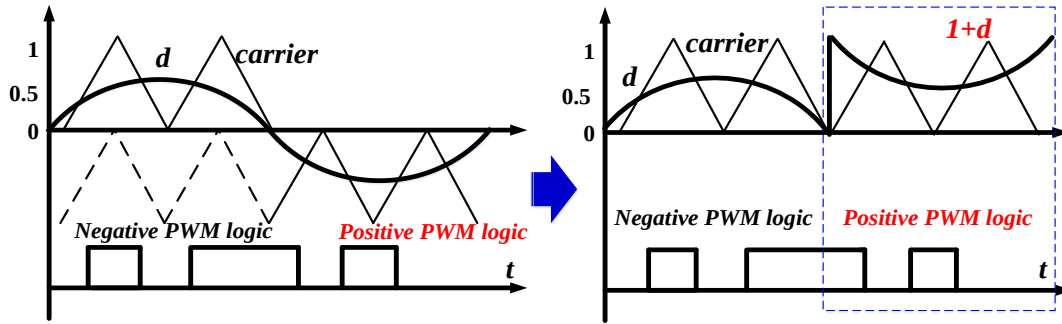


Fig. 5-22. Modulation implementation in Vienna-type rectifier.

Different from two-level converters, the comparator logic in Vienna-type converter should be toggled per half line cycle to match the phase current direction. Here, the instantaneous duty cycle d is expressed as

$$d = M \sin(\theta) \quad (5-5)$$

where M is the modulation index defined as the ratio of phase peak voltage over half dc-link

$$\text{voltage } M = \frac{V_N}{V_{DC}/2}.$$

5.3.2 Single-phase sampling strategy and synchronization issues in three-phase

Although sampling at the middle point of either turn-on or turn-off interval can both represent the averaged current as shown in Fig. 5-23, it is expected to sample at the long interval considering the relatively time-consuming ADC process in high switching converters.

From this concept, a sampling scheme for a single phase of Vienna-type rectifier is proposed, as illustrated in Fig. 5-24. If $M < 0.5$, in positive half line cycle, sampling conversion should be triggered when the carrier counter reaches its period value ($CTR = PRD$), while in the negative half cycle, sampling point should be placed at $CTR = 0$. When $M > 0.5$, this scheme can still be applied except for some modifications. As shown in Fig. 5-24 (b), in the positive half line cycle, if the instantaneous duty cycle d is higher than 0.5, sampling conversion should be reversed, i.e. triggered at $CTR = 0$; in the negative line cycle, if d is below -0.5, sampling conversion should be at $CTR = PRD$. Thus, the sampling instant is always placed at the long interval in one switching cycle.

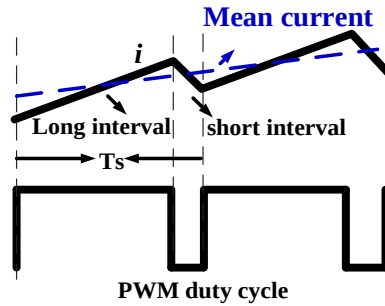


Fig. 5-23. Desired current sensing instant.

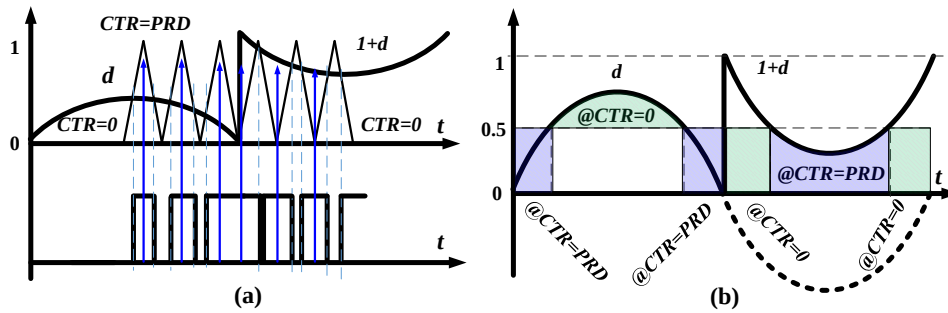


Fig. 5-24. Illustration of a basic hybrid sampling scheme for one phase of Vienna-type rectifiers: (a). $M < 0.5$; (b). $M > 0.5$.

However, when applying this scheme to three phases, three sampling instants will conflict. Taking region 1 with its phase angle $< 30^\circ$ as an example, as illustrated in the shadow region of

Fig. 5-25, phase A and B should be sampled at $CTR=PRD$, while phase C should be at $CTR=0$. Thus, three conversion instants are not the same, requiring different sampling instant monitoring, extra triggering sources and independent ADC interrupt control logic, which complicates the controller design in terms of both hardware and software.

5.3.3 Proposed sector-based method

To sample in the long interval and still accommodate to three phases, a simple sector based scheme is proposed. As shown in Fig. 5-26, a whole line cycle is now divided into six sectors. For each sector, there is only one common instant to align ADC samplings of three-phase currents, either at $CTR=ZERO$ or $CTR=PRD$, depending on its sector number. For example, when the angle is within sector 1, sampling for three phases should be placed at $CTR=0$, while for section 2, it rotates to $CTR=PRD$. Although this common sampling instant alternates between two nearby sectors, the sector partition can be easily realized using PLL angle. And there is no need to flip the sampling instants based on the instantaneous duty cycle d or modulation index M anymore. In addition, the three-phase current samplings share the same ADC triggering signal and thus can be sampled by DSP's internal ADC and processed by only one interrupt.

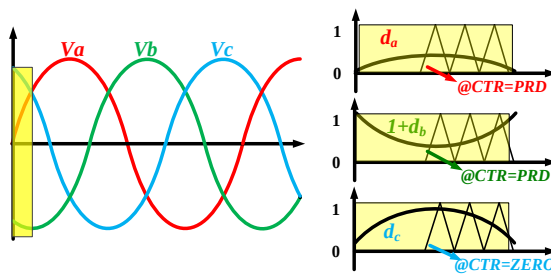


Fig. 5-25. Illustration of the sampling instant conflicts in three-phase converters with $M < 0.5$.

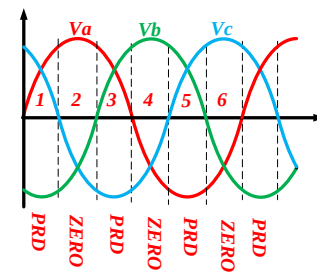


Fig. 5-26. Proposed sampling scheme for three-phase converters with carrier counter value $CTR = \text{zero or PRD}$.

It should be mentioned there is still a limitation of this proposed approach. This method cannot guarantee that all three phases are sampled at their long interval simultaneously, though it has tried to maximize this possibility. The probability analysis is clarified as below, considering different modulation indexes and line angles for three-phases. As shown in Fig. 5-27, a carrier/modulation ratio $N=13$ is asserted, and only half line cycle is plotted due to the symmetric of ac waveforms. For brevity, the analysis mainly focuses on phase A. Please also notice that in Fig. 5-27, when any of the three-phase duty cycle d_{abc} falls in the negative region, it will be shifted to $1 + d_{abc}$.

From Fig. 5-27 (a), when M is below 0.5 and line angle θ is in sector 1 and 3, the long interval for phase A in a switching cycle occurs around $CTR=PRD$. And per the sector based scheme, the sampling instant is also placed at $CTR=PRD$. However, when θ is in sector 2, the long interval for phase A in a switching cycle should be at $CTR=PRD$ which differs from the schemed triggering logic $CTR=0$. Therefore, phase A will be sampled at its short interval in this sector, whereas the other two phases will be sampled at their long intervals.

If a probability factor λ is adopted to depict the chance of sampling instant occurring in the short interval instead of the desired long interval of a switching cycle, it can be defined as the angle range with short interval sampling over the whole line cycle,

$$\lambda = \frac{\theta_{\text{short_interval_sampling}}}{360} \quad (5-6)$$

For phase A, in the case of $M < 0.5$, its short interval sampling probability is $\lambda_A = \frac{60}{180} = \frac{1}{3}$

From Fig. 5-27 (a-b), since the peak of d_a locates in sector 2, d_a will cross $d=0.5$ boundary (above this level, the long interval for phase A occurs at $CTR=0$) first in this sector, as M is increasing. Thus,

$$d_a = M \sin(\theta) = 0.5 \quad (5-7)$$

Gradually as M further increases, d_a will start going beyond $d=0.5$ boundary in sector 1 and sector 3, as shown in Fig. 5-27 (c-d). The crossing boundary angle is $\theta = 60^\circ$, where d_a crosses 0.5. Thus, the corresponding modulation index M_{th} at this condition can be derived from

$$M_{th} \sin(60^\circ) = 0.5 \quad (5-8)$$

i.e. $M_{th} = 1/\sqrt{3} = 0.577$.

Therefore, when M is above 0.5 but below 0.577 as the case in Fig. 5-27 (b), there will be two angle-segments with sampling instant at short intervals in phase A as marked. Due to the central symmetry, the short interval sampling probability factor is

$$\lambda_A = \frac{2(\theta - 60)}{180} \quad (5-9)$$

where, $\theta = \sin^{-1}(0.5/M)$.

Similarly, the case with M above 0.577 can also be analyzed. The only difference is that d_a crosses $d=0.5$ in sector 1 and 3. Thus, there will be two short-interval sampling segments in sector 1 and 3, respectively, as illustrated in Fig. 5-27 (d).

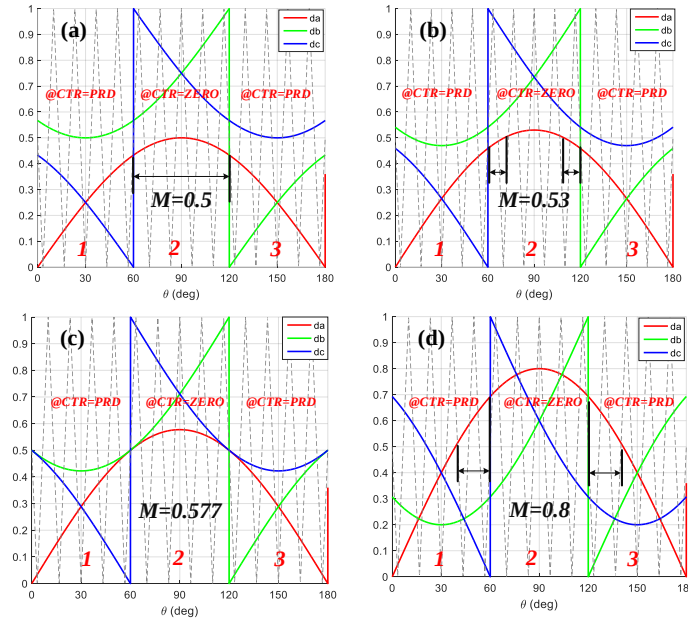


Fig. 5-27. Short intervals of the proposed sampling scheme in phase A of a Vienna-type rectifier, with carrier/modulation ratio 13.

The ratio of undesired sampling interval over the whole line cycle is finally provided in Table 5-6 and illustrated in Fig. 5-28. It is clear when the modulation index is larger than 0.5, this method can achieve even better performance.

Table 5-6. Ratio of sampling instant occurring in short switching interval in a line cycle.

M range	$M \leq 0.5$	$0.5 < M \leq 1/\sqrt{3}$	$M > 1/\sqrt{3}$
Probability	1/3	$\frac{(\sin^{-1}(\frac{0.5}{M}) - 60)}{90}$	$\frac{(\sin^{-1}(0.866M) - 30)}{90}$

Other important conclusions are: only two phases are sampled at the long interval each time; for each phase, there is always a portion of line cycle with shorter sampling interval; three phases alternate similarly. For Vienna circuit with SPWM, the worst cases occur at $M \leq 0.5$ and 1, with the maximum chance of 1/3 line cycle per phase to be sampled at the short interval; and the best case occurs at $M=0.577$ where all three phases are sampled at the long interval along a line cycle.

5.3.4 Experimental verification

A comparison with and without the proposed current sampling method is carried out, at 115 V_{rms} 800 Hz input, 600 V_{dc} output, and 450 kHz switching frequency. Fig. 5-29 shows the voltage and current waveforms with the new sampling method, and Fig. 5-30 presents the comparison results of harmonic spectra. The proposed sampling method helps reduce current THD by 3.7 percentage points in a Vienna-type rectifier. The main improvement is shown at 2nd, 3rd, and 5th.

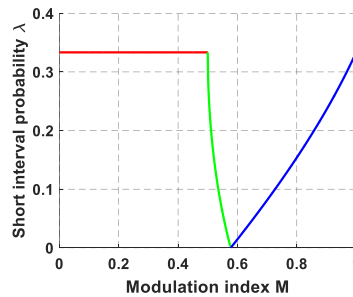


Fig. 5-28. The possibility of sampling instant occurring in short switching interval in a line cycle.

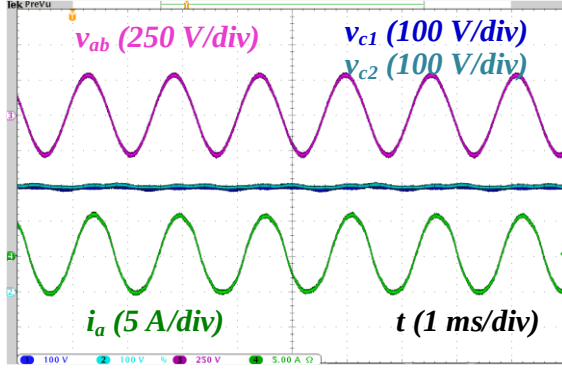


Fig. 5-29. Waveforms with proposed sampling scheme.

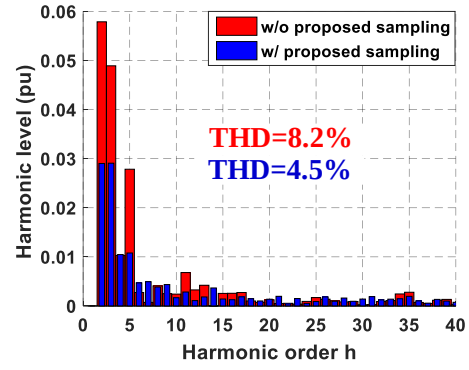


Fig. 5-30. current harmonic spectrum with and without proposed scheme.

5.4 Modeling and compensation of device parasitics' impact on ac power quality

As discussed in Section 2.3.3, device parasitic capacitance can introduce PWM voltage loss during the deadtime and turn-off, the existing approach to calculate the voltage distortion is complicated requiring instantaneous current measurement. And a sophisticated feedback control might be unacceptable in a high switching frequency converter due to limited computation time, either. A simple and effective way to analyze and compensate the distortion is thus in demand. Therefore, in this work, a feedforward type modulation compensator is then proposed to compensate this distortion, without requiring instantaneous measurements.

And for three-level converters, no analytical model on this switching frequency dependent turn-off distortion has been developed yet. Therefore, a closed-form analytical model will be proposed to predict the voltage distortion and switching frequency impact, using the subject Vienna-type rectifier as the study case.

5.4.1 Turn-off transient of a GaN device

For a GaN device, its gate driver should be as fast as possible to fully utilize the GaN device's fast switching capability and reduce switching loss. As such, the turn-on transient time is mainly

determined by the applied gate voltage, gate resistance, and the gate driver's rising speed and maximum source current.

However, even with a fast gate driver, the turn-off transient is also strongly affected by the load current. The turn-off transient of a GaN device can be divided into three stages. The first stage is turn-off delay, where the gate voltage is falling to the Miller voltage, the channel is still operating in the ohmic region, and the channel resistance is approximately R_{ds_on} . During this time, the drain-source voltage v_{ds} is near zero. The duration $t_{d,off}$ is typically very small, and no switching loss occurs during this time. The second stage is the channel turn-off time, where the gate voltage v_{gs} falls from V_{Miller} to the threshold voltage V_{th} . The duration is determined mainly by the gate driver speed. During this time, some of the load currents flow through the device's channel, operating in the lossy saturation region, and the remainder of the load current acts to displace charge in the output capacitances of both complementary devices. The third stage is the C_{oss} charge displacement time, where the device's channel is fully off, and the entire load current is used to displace charge in the C_{oss} of both complementary devices in the circuit. No overlap losses occur during this time, and all apparent energy loss is actually stored in the device's output capacitance until its next turn-on transient occurs. Because this interval is not controlled by the gate driver, it is determined solely by the relationship $dv_{ds}/dt=i/C_{oss}$. Furthermore, since C_{oss} drops nonlinearly as drain-source voltage increases, analysis of the voltage slew rate during this interval can be quite complex.

To evaluate the turn-off time distribution for the adopted 30 A//650 V GaN device GS66508P, a sweep of double pulse tests was performed across a range of operating conditions. Fig. 5-31 shows a typical turn-off transition with 10 A, and 400 V. The first interval $t_{d,off}$ is only about 7 ns, whereas the second interval is not easily distinguished from the third, thus t_{vr} is used to denote this entire voltage rising interval. The duration of these simplified two stages under different load

currents and voltages are provided in Fig. 5-32. Fig. 5-32 (a) shows that the turn-off delay interval is less than 10 ns and slightly reduced when current increases. Fig. 5-32 (b) indicates a strong inverse relationship between load current and voltage rise time at any blocking voltages.

5.4.2 Voltage distortion during turn-off

Fig. 5-33 shows a phase-leg of a Vienna-type rectifier, consisting of 650 V e-mode GaN devices Q_1 , Q_2 , and 1200 V SiC diodes D_1 and D_2 , with a positive half line cycle illustrated. During the turn-off transient, the Q_1 channel is fully shut off after a short time interval. Then, the input phase current charges the C_{oss} of Q_1 from 0 V to $V_{DC}/2$, meanwhile the top diode capacitor C_{D1} is discharged from $V_{DC}/2$ to 0 V. It is worth mentioning that although the bottom diode D_2 does not participate in the current commutation during each half line cycle, its output capacitance is indeed charged up from $V_{DC}/2$ to V_{DC} . And since all of this charge is supplied by the input current, the voltage rise time can be very long when the current is less than 6 A, especially in the zero crossing regions. Consequently, the terminal voltage of the phase-leg is affected, which causes the input current distortion.

5.4.3 Basic compensation principle

The terminal voltage distortion due to the relatively long turn-off transient cycle can be treated as a voltage loss compared to the ideal PWM voltage. Since the average of the ideal PWM voltage over one switching cycle represents the desired output voltage, a basic compensation scheme would be reshaping the actual PWM voltage so that it has the same average value as the ideal case, (i.e. the same volt-seconds over one switching cycle). This voltage error can be compensated as a pure time delay ($t_{d_off} + 0.5t_{vr}$ obtained from a series of experimental data), as in [155], or as the approach to be described in section 5.4.4. But they become less effective near the zero crossing when the device does not reach its full blocking voltage during the compensated duty cycle. An

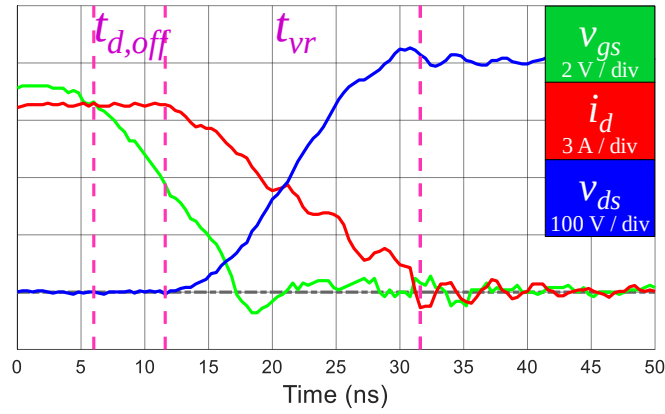


Fig. 5-31. Turn-off waveforms of a DPT of GaN GS66508P @ 400 V dc.

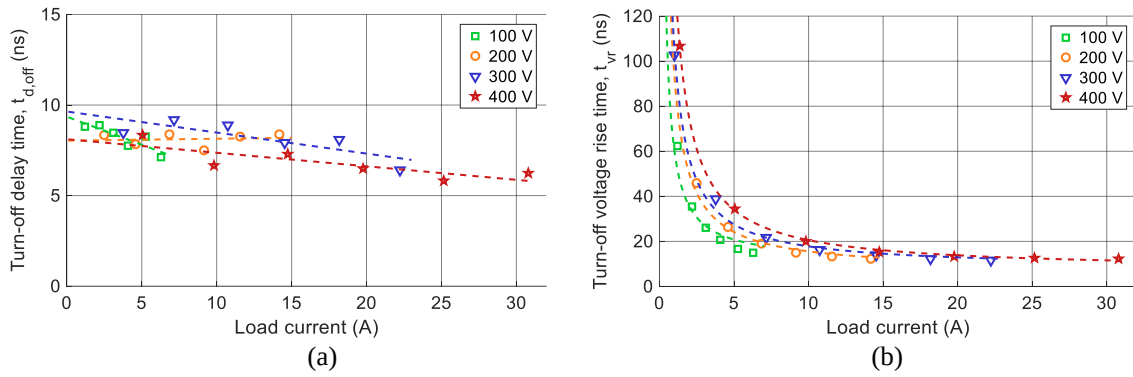


Fig. 5-32. Turn-off transient duration from DPT results of GaN Systems GS55608P, at different current and voltage conditions. (a) Turn-off delay time, (b) Turn-off current voltage rise time.

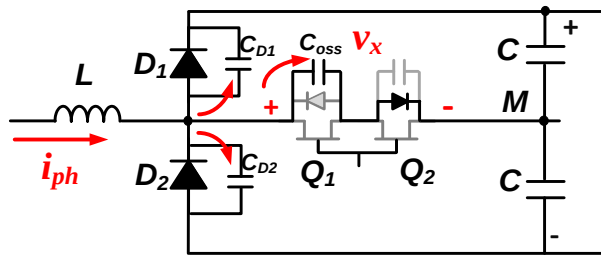


Fig. 5-33. Charging paths of output capacitances during turn-off for one phase-leg of Vienna-type PWM rectifiers.

analytical approach is, therefore, proposed in this section to accurately and conveniently model and compensate this distortion.

As shown in Fig. 5-34, the actual PWM voltage patterns during turn-off are divided into two groups based on the relationship between the peak terminal voltage V_{x_pk} and $0.5V_{dc}$, where the dashed line denotes the desired ideal PWM voltage shape and the solid line represents the actual PWM voltage shape. Clearly, this deviation between ideal and actual will result in voltage error if the PWM is not compensated. From the PFC test result and also the DPT result, the slew rate of the voltage rise can be approximately considered as a constant. So, the scheme here is to extend the turn-off interval by a certain time, so that the total voltage-second area is still equal to that of the ideal case. Thereby, a compensation scheme is proposed in Fig. 5-35, considering two cases at different current levels and charging conditions. Here, the black line is the uncompensated voltage pulse, and the red line represents the voltage rising edge of the extended turn-off interval after compensation. In the first case, the capacitance is charged quickly enough to reach $0.5V_{dc}$ before the end of the pulse. In Case 2, the current is too low to allow for the voltage to reach $0.5V_{dc}$ before the end of the pulse. However, the extended voltage pulse after compensation may in fact be long enough for v_x to reach $0.5V_{dc}$, as shown in Fig. 5-35 Case 2 (a). Therefore, it is important for the compensation algorithm to consider in which case the pulse will fit into after it is extended, and not just prior to compensation.

The approach of this scheme is to equalize the two shaded volt-second areas as shown in Fig. 5-35, and thereby compensate for the voltage error. Because the turn-off delay interval $t_{d,off}$ is far shorter than the charging interval in the current range of interest, this interval is neglected for simplicity without affecting the compensation accuracy. As previously mentioned, the slow voltage transition is mainly attributed to the low charging current during the turn-off transient.

Though it is reasonable to approximate the charging voltage as a linear rise, the nonlinear capacitances of switching devices do greatly impact the charging time and must be considered.

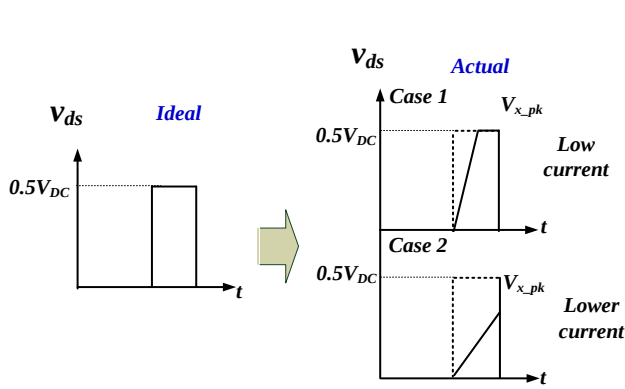


Fig. 5-34. Ideal and actual PWM voltage shape during turn-off transient.

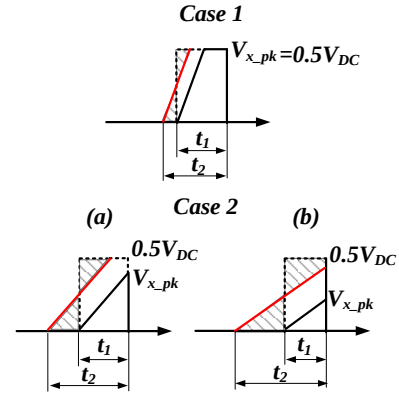


Fig. 5-35. Two voltage distortion cases associated with different current level and the proposed turn-off compensation scheme considering the voltage shape before and after compensation.

The three device capacitances can be considered in parallel during the turn-off transient and are later derived in Section 5.4.7 based on the current direction and dv/dt polarities shown in Fig. 5-33. The relationship between phase current and the voltage across these parallel nonlinear capacitances can be described by

$$i_{ph} = C_{total}(v_x) \frac{dv_x}{dt} \quad (5-10)$$

where $C_{total}(v_x)$ is the sum of the three nonlinear capacitances as a function of the switch-node voltage v_x .

During the short turn-off transient, the phase current i_{ph} can be regarded as a constant, thus

$$t_{charge} = \int_0^{V_{x_pk}} dt = \frac{\int_0^{V_{x_pk}} C_{total}(v_x) dv_x}{i_{ph}} = \frac{V_{x_pk} C_{eq}}{i_{ph}} \quad (5-11)$$

where C_{eq} is the charge-based equivalent output capacitance over the voltage range $[0, V_{x_pk}]$ for the three T-shape connected devices per phase-leg.

Based on (2), it is effective to use this charge-based equivalent capacitance to represent the nonlinear voltage-dependent $C_{total}(v_x)$. Although C_{eq} is also a nonlinear function of V_{x_pk} , it can be approximated as a constant when $V_{x_pk} = 0.5V_{DC}$. The detailed analysis will be presented in section 5.4.7.

With the above assumptions, Cases 1, 2a, and 2b from Fig. 5-34 will be analyzed in detail.

Case 1: Since the volt-second area of the two shaded areas should be equal, one can obtain

$$\frac{1}{2}k(t_2 - t_1)^2 = \frac{1}{2}k[t_1 - (t_2 - \frac{V_{DC}}{2k})]^2 \quad (5-12)$$

where k is defined as the slew rate of v_{ds} in the turn-off transition, given by

$$k = \frac{i_{ph}}{C_{eq}} \quad (5-13)$$

Thus, the desired turn-off interval extension can be calculated as

$$\Delta d = \frac{(t_2 - t_1)}{T_s} = \frac{V_{DC}C_{eq}}{4T_s} \frac{1}{i_{ph}} \quad (5-14)$$

The boundary condition between Case 1 and Case 2 is given in (5-15) and (5-16).

$$kt_1 \geq \frac{V_{DC}}{2} \quad (5-15)$$

$$d > \frac{V_{DC}C_{eq}}{2T_s} \frac{1}{i_{ph}} \quad (5-16)$$

Case 2: Here, the peak v_x is below $V_{dc}/2$. So, the boundary conditions given above are not met.

In Case 2a, which means that the peak voltage after compensation reaches $V_{dc}/2$. The shape of the charge balance for the extended pulse is the same as Case 1, leading to the same equivalence given in (5-16).

The boundary condition for this case is

$$\frac{V_{DC}C_{eq}}{4T_s} \frac{1}{i_{ph}} \leq d < \frac{V_{DC}C_{eq}}{2T_s} \frac{1}{i_{ph}} \quad (5-17)$$

In Case 2b, $kt_2 < \frac{V_{DC}}{2}$, which means that the peak voltage after compensation is still below

$V_{dc}/2$. The area equivalence becomes

$$\frac{1}{2}k(t_2 - t_1)^2 = \frac{1}{2}t_1 \left(\left(\frac{V_{DC}}{2} - k(t_2 - t_1) \right) + \left(\frac{V_{DC}}{2} - kt_2 \right) \right) \quad (5-18)$$

Solving this equation yields

$$t_2 = \sqrt{t_1 \frac{V_{DC}}{k}} \quad (5-19)$$

$$\Delta d = \frac{(t_2 - t_1)}{T_s} = \sqrt{\frac{C_{eq}V_{DC}}{T_s} \frac{d}{i}} - d \quad (5-20)$$

The boundary condition is then given as

$$t_1 < \frac{C_{eq}V_{DC}}{4i_{ph}} \quad (5-21)$$

$$d < \frac{V_{DC}C_{eq}}{4T_s} \frac{1}{i_{ph}} \quad (5-22)$$

It is evident that Case 2a can be grouped with Case 1, as the compensation equations give the same result. Therefore, the final compensation model can be described by

$$\Delta d = \frac{(t_2 - t_1)}{T_s} = \begin{cases} \frac{V_{DC}C_{eq}}{4T_s} \frac{1}{i_{ph}}, & \left(d \geq \frac{V_{DC}C_{eq}}{4T_s} \frac{1}{i_{ph}} \right) \\ \sqrt{\frac{C_{eq}V_{DC}}{T_s} \frac{d}{i_{ph}}} - d, & \left(d < \frac{V_{DC}C_{eq}}{4T_s} \frac{1}{i_{ph}} \right) \end{cases} \quad (5-23)$$

It is also worth noting that at the boundary condition between these two cases, both equations converge to the same result, with $\Delta d = d$, meaning that the duty cycle of turn-off should be doubled at this instant to compensate for the voltage error.

5.4.4 Issues with voltage error compensation

The proposed scheme compensates the duty cycle based on the pulse-based adjustments, but it is also possible to directly calculate the duty cycle compensation term based on the average voltage error (16), as in one of the conventional dead-time compensation approaches [185, 189].

$$\Delta d = \frac{\Delta V}{V_{DC} / 2} \quad (5-24)$$

However, this assumes the compensated voltage has the ideal shape, which is not realistic still due to the non-negligible C_{oss} charging time. Especially when V_{x_pk} is below the dc link voltage (or half of that in three-level converters), this compensation scheme introduces errors. The mechanism is illustrated in Fig. 5-36, where S_{bcde} is the volt-second area of the uncompensated PWM voltage, time interval a-b is the extended turn-off interval via the proposed method, and interval j-b is the result from the voltage error compensation scheme.

In Case 1, when the peak voltage V_x reaches $0.5V_{dc}$, extending the turn-off duty cycle using (5-24) effectively compensated for voltage error. The voltage loss area S_{beg} is equal to the rectangle area S_{jbgh} if the pulses are considered as ideal, or the parallelogram area S_{abef} if the actual voltage rise time is considered, and therefore the same performance is achieved as with the proposed method.

However, for either Case 2a or Case 2b, the compensation given in (5-24) always gives an insufficient extension of turn-off interval. This is because the height of S_{jbgh} with that scheme is higher than that of the proposed S_{abdf} . As V_{x_pk} gets smaller, this compensator error grows, as demonstrated below.

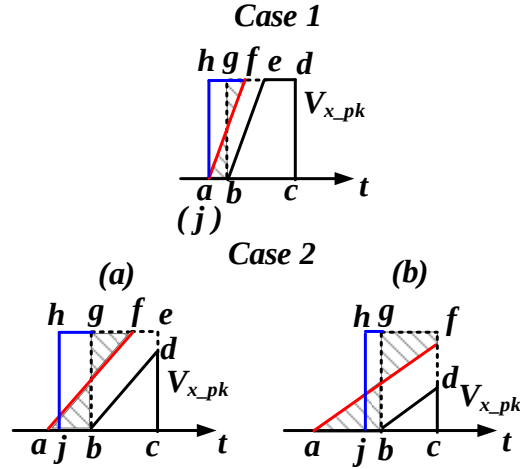


Fig. 5-36. Insufficient turn-off extension in voltage loss based compensation (blue line: voltage loss based compensation; red line: proposed compensation; black line: uncompensated case; dashed line: ideal PWM voltage).

5.4.5 Modulation compensation for SPWM and intuitive physical model

As shown in (5-23), the desired turn-off compensation term is a function of both the instantaneous phase current and the instantaneous duty cycle. Additionally, the duty cycle threshold for the boundary condition d_{th} is also a variable, requiring update each control cycle. Relying on the instantaneous d and i_{ph} to judge and update the compensation term is not robust, considering the likely current sampling noise and measurement error. Most importantly, the instantaneous compensation scheme shown in (5-23) does not reveal a clear overall picture of the duty cycle compensation over a whole line cycle, nor does it provide an effective way to evaluate the impact of different distortion factors such as switching frequency and dc voltage, or a guideline for control and modulation improvement.

In the following text, the relationship between d and i_{ph} will be exploited, to present an improved compensation scheme only related to d itself, forming the eventual modulation compensation scheme. For the sake of brevity, the case with carrier-based SPWM modulation is first analyzed. As well known, for Vienna-type rectifiers,

$$d_{on} = 1 - \frac{V_N \sin(\theta)}{V_{DC} / 2}, \quad (0 \leq \theta \leq \pi) \quad (5-25)$$

And considering the unity power factor control as the PFC target,

$$i_{ph} = i_N \sin(\theta) \quad (5-26)$$

From above, one obtains

$$d_{on} = 1 - \frac{V_N / I_N}{V_{DC} / 2} i_{ph} \quad (5-27)$$

Then, an equivalent active resistance is defined.

$$R_{target} = \frac{v}{i_{ph}} = V_N / I_N \quad (5-28)$$

where R_{target} represents the unity power factor control for a specific power rating and is sometimes called the loss-free resistance [316, 317].

Substituting (5-28) into (5-27), yields

$$d = 1 - d_{on} = \frac{R_{target}}{V_{DC} / 2} i_{ph} \quad (5-29)$$

Substituting (5-28) into (5-22), the new boundary d_{th} is derived as

$$d_{th} = \sqrt{\frac{R_{target} C_{eq}}{2T_s}} \quad (5-30)$$

Similarly, substituting (5-28) into (5-23), the final compensation equations in the SPWM case becomes

$$\Delta d = \begin{cases} \frac{R_{target} C_{eq}}{2T_s} \frac{1}{d}, & (d \geq d_{th}) \\ \sqrt{\frac{2R_{target} C_{eq}}{T_s}} - d, & (d < d_{th}) \end{cases} \quad (5-31)$$

which reveals that the distortion is physically determined by the ratio of the time constant $R_{target}C_{eq}$ to the turn-off interval.

Since R_{target} represents the equivalent input impedance of the PFC in the line frequency domain, and C_{eq} reflects the device non-ideal switching behavior in the high frequency domain, this distortion and its compensation can, therefore, be interpreted with a circuit model crossing the

whole frequency span as illustrated in Fig. 5-37. As anticipated, since the turn-off charging process is tightly related to $R_{target}C_{eq}$, an ideal modulated PWM voltage generated by the PFC on the right side of the circuit will be inevitably distorted, thus the compensation in (5-31) is needed to achieve the target ac voltage. This intuitive model together with (5-31) provides a straightforward way to evaluate the input current distortion based on the given power, voltage rating and operation frequency.

Finally, as (5-31) is only a function of d , the overall compensation for a whole line cycle can be conveniently obtained. The compensation results at 650 V dc, 1.5 kW, and 450 kHz switching frequency are shown in Fig. 5-38 and Fig. 5-39, indicating the most severe distortion around zero crossing regions.

5.4.6 Modulation compensation for SPWM plus 3rd harmonic injection

To achieve higher dc voltage utilization, space vector modulation (SVM) is preferred. A simple implementation is a carrier-based modulation with 3rd harmonic injection. In that case,

$$d_{on} = 1 - \frac{V_N \sin(\theta)}{V_{DC}/2} - V_{3h} = 1 - \frac{V_N}{V_{DC}/2} \left[\sin(\theta) + \frac{1}{4} \sin(3\theta) \right] \quad (5-32)$$

Similar to the SPWM case, with the adoption of the equivalent resistance concept, the duty cycle becomes

$$d = \frac{R_{target}}{V_{DC}/2} \left[1 + \frac{1}{4} \frac{\sin(\theta)}{\sin(3\theta)} \right] i_{ph} = \frac{2R_{target} \alpha(\theta)}{V_{DC}} i_{ph} \quad (5-33)$$

where α is the only additional term to the SPWM case and can be simplified as

$$\alpha(\theta) = \left(\frac{7}{4} - \sin(\theta)^2 \right) \quad (5-34)$$

where θ is a known variable from the PLL.

With these revisions, the compensation equations in the SVM case become

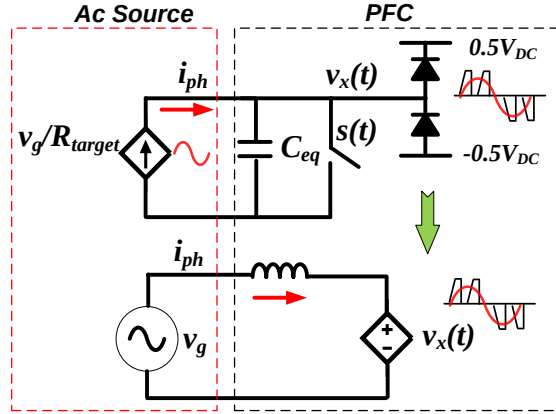


Fig. 5-37. An equivalent model of PWM voltage distortion in a unity PFC converter.

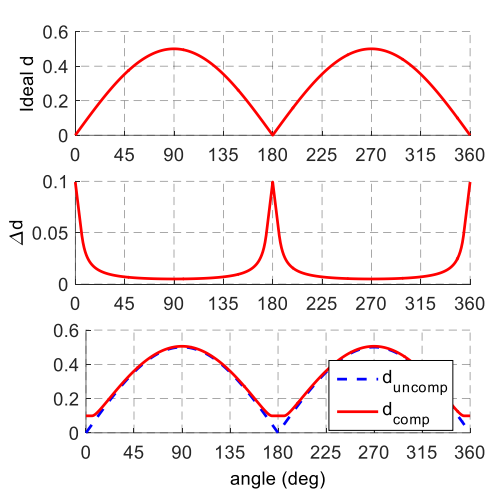


Fig. 5-38. Duty cycle compensation over a line cycle with SPWM modulation. Top: ideal (uncompensated) turn-off duty cycle; medium: compensation term; bottom: ideal turn-off duty cycle in dashed blue and compensated duty cycle in red.

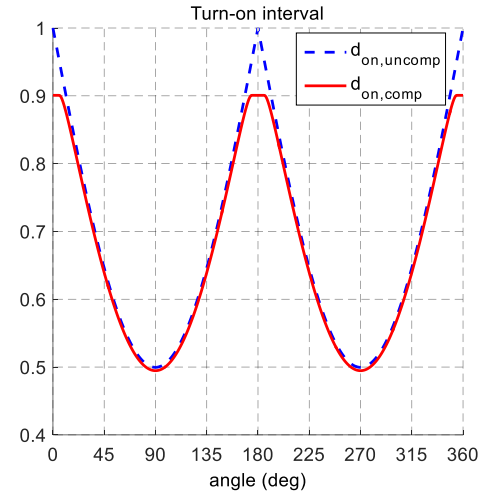


Fig. 5-39. Corresponding turn-on duty cycle before and after compensation with SPWM modulation. Ideal turn-on duty cycle in dashed blue and compensated result in red.

$$\Delta d = \begin{cases} \frac{R_{\text{target}} C_{eq}}{2T_s} \frac{\alpha(\theta)}{d}, & (d \geq d_{th}) \\ \sqrt{\frac{2R_{\text{target}} C_{eq}}{T_s} \alpha(\theta)} - d, & (d < d_{th}) \end{cases} \quad (5-35)$$

where the boundary duty cycle and angle are constants for a given power target given by

$$d_{th} = \sqrt{\frac{R_{\text{target}} C_{eq}}{2T_s} \alpha(\theta_{th})} \quad (5-36)$$

$$\theta_{th} = \sin^{-1} \left(\frac{\frac{7}{4} - \sqrt{\left(\frac{7}{4}\right)^2 - \frac{C_{eq} R_{\text{target}}}{T_s M^2}}}{2} \right) \quad (5-37)$$

Finally, the control diagram of the three-level converter can be presented as shown in Fig. 5-40.

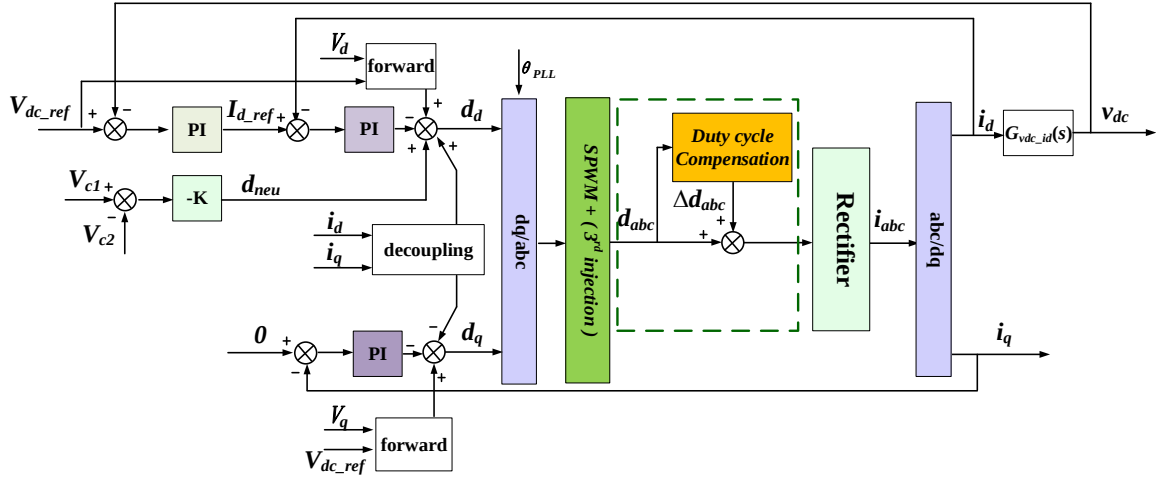


Fig. 5-40. Control diagram of three-phase PFC with the proposed modulation compensation scheme.

The duty cycle before and after compensation at 650 V dc, 1.5 kW, and 450 kHz switching frequency is provided in Fig. 5-41 and Fig. 5-42, indicating that more compensation is needed around the zero crossing regions.

5.4.7 Charge-equivalent capacitance calculation

As mentioned previously, the output capacitance of the GaN FET is not the only one involved in the turn-off charging process, because the capacitances of the two SiC diodes should also be included. However, since the junction capacitance C_{D1} is discharged from 0.5 V_{DC} to 0 V, and C_{D2}

is charged from $0.5 V_{DC}$ to V_{DC} , the instantaneous capacitances are different for each device during the transient, because they are nonlinear and voltage-dependent.

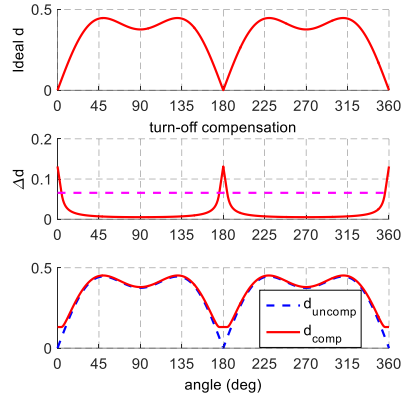


Fig. 5-41. Duty cycle compensation over a line cycle with 3rd harmonic injection. Top: ideal (uncompensated) turn-off duty cycle; medium: compensation term; bottom: ideal turn-off duty cycle in dashed blue and compensated duty cycle in red.

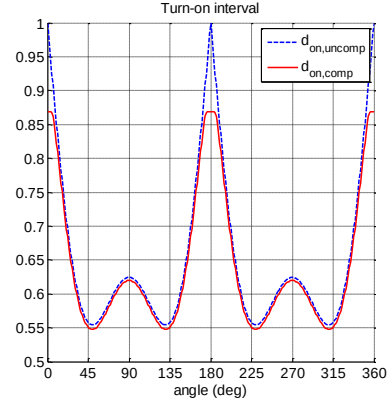


Fig. 5-42. Corresponding turn-on duty cycle before and after compensation with 3rd harmonic injection. Ideal turn-on duty cycle in dashed blue and compensated result in red.

The charge-based equivalent capacitances for the three nonlinear capacitances are thus derived based on their respective $C_{oss}(V)$ curves either from datasheet or measurement.

$$C_{eq_GaN} = \frac{\int_0^{0.5V_{DC}} C_{oss} dv_{DS}}{0.5V_{DC}} \quad (5-38)$$

$$C_{eq_D1} = \frac{\int_{0.5V_{DC}}^0 C_{D1} dv_{D1}}{0.5V_{DC}} \quad (5-39)$$

$$C_{eq_D2} = \frac{\int_{0.5V_{DC}}^{V_{DC}} C_{D2} dv_{D2}}{0.5V_{DC}} \quad (5-40)$$

The total charge-equivalent capacitance during the turn-off interval can then be calculated as

$$C_{eq} = C_{eq_GaN} + C_{eq_D1} + C_{eq_D2} \quad (5-41)$$

Fig. 5-43 shows the nonlinear characteristics of the three output capacitances. A total 434 pF equivalent capacitance is obtained for 600 V dc bus. Measurements from the slew-rate of v_{DS} and current waveforms in Fig. 5-44 result in an average of 480 pF, close to the calculation result.

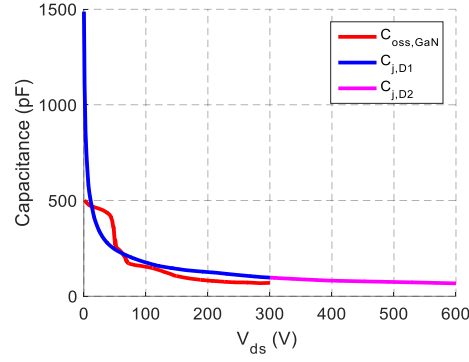


Fig. 5-43. Nonlinear capacitances of two SiC diodes and one GaN switch.

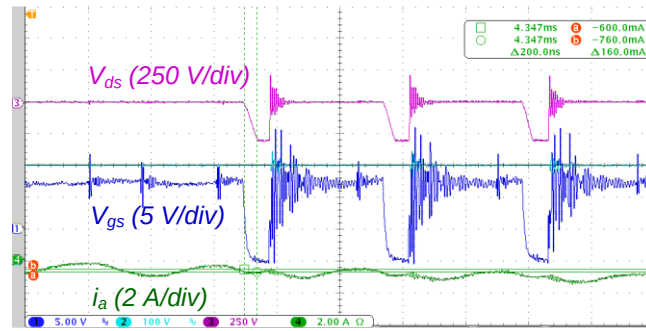


Fig. 5-44. Ac terminal voltage distortion around zero crossing and the voltage slope measurement.

The preceding discussion assumes the switch-node voltage v_{ds} eventually reaches $0.5V_{DC}$. However, when the phase current is close to zero, as shown in Fig. 5-47, the peak voltage V_x might be below $0.5V_{DC}$. Thus, each capacitance shown above now becomes a function of V_{x_pk} .

Therefore, the validity of the constant C_{eq} assumption using the above formulas must be examined. First, since the voltage changing directions of these three capacitances are different, their charge-based equivalent capacitances do not increase or decrease in the same way with respect to V_{x_pk} . For instance, as shown in Fig. 5-45, although $C_{eq,GaN}$ shows a higher value when V_{x_pk} is lower than $0.5V_{DC}$, $C_{eq,D1}$ shows the opposite trend. Secondly, the $V_{x_pk} < 0.5V_{DC}$ case only occurs for 10 degrees around the zero crossing as denoted in Fig. 5-46, which includes only around 10 switching cycles as shown in Fig. 5-47 (excluding the fully on cycles). Therefore, in this case,

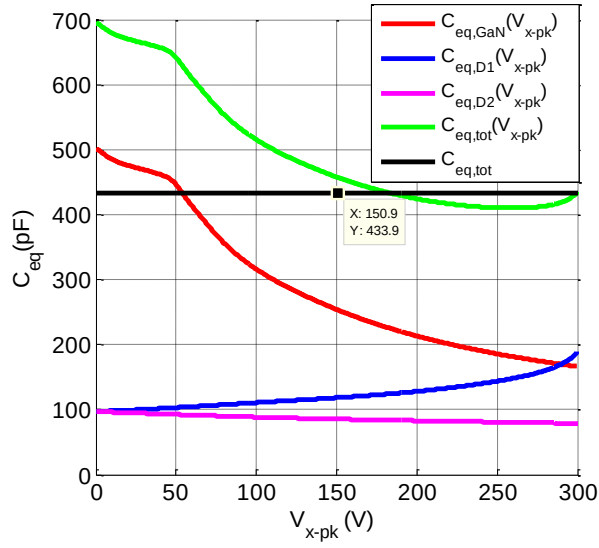


Fig. 5-45. Charge-equivalent capacitance as a function of V_{x_pk} .

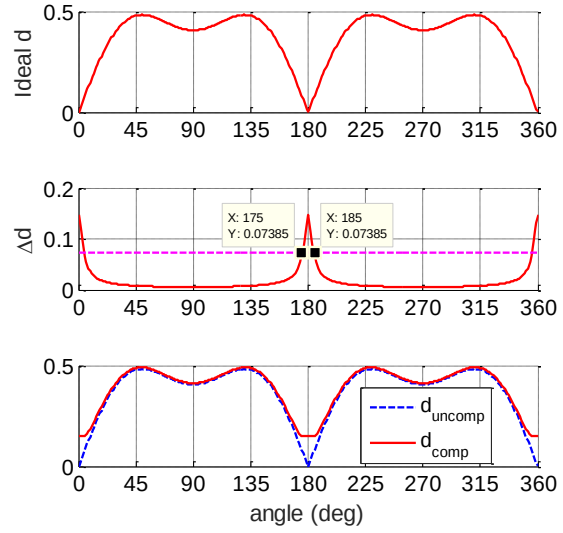
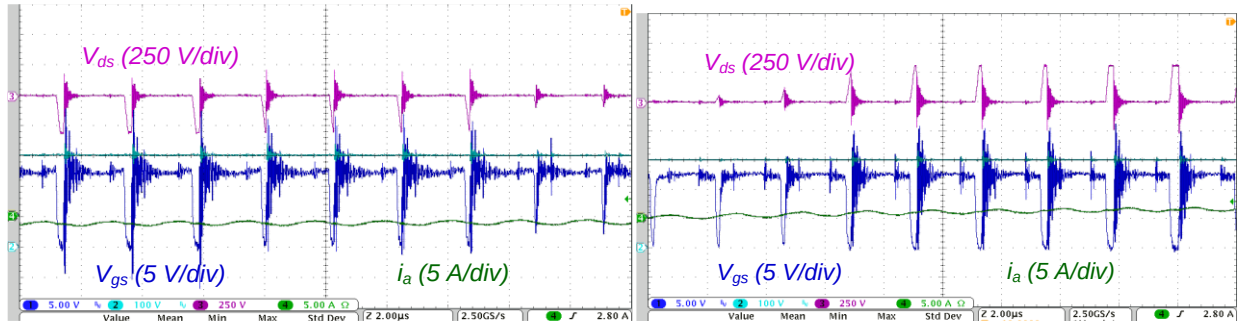


Fig. 5-46. Duty cycle compensation over a line cycle for SVM.



(a) Experimental waveforms of voltage distortion before zero crossing.

(b) Voltage distortion after zero crossing.

Fig. 5-47. Experimental waveforms of PWM voltage distortion in Vienna-type rectifier.

the nonlinear behavior of C_{eq} can be neglected. Consequently, the charge-based equivalent capacitance can be approximately regarded as a constant with $V_{x_pk} = 0.5V_{DC}$. As shown by the black line in Fig. 5-45, this approximation results in 434 pF equivalent capacitance for this case.

It has also to be mentioned that the device output capacitance is a pretty stable parameter, based on which engineers estimate the switching loss for the hard-switching circuit, dead-time selection for the resonant circuit, resonant tank design for the quasi-PWM resonant converter, and etc. It has only negligible dependence on the junction temperature, which is true not only for GaN devices [318, 319] but also for Si MOSFETs [155, 320]. Therefore, the proposed compensation scheme is immune to the operating temperature.

In addition, through the simulation study, it is found that this compensation scheme is not very sensitive to C_{oss} deviation, even considering a certain inconsistency of device output capacitances. This is probably because the majority of the volt-second loss has been compensated by this scheme from the base C_{oss} , as long as the deviation of C_{oss} is within a reasonable range. The relationship between THD improvement vs C_{oss} deviation is provided in Fig. 5-48 through a series of simulations. With 20% C_{oss} deviation, it shows that THD improvement compared to the case without compensation, only varies from 12.8 percentage points to 11.3 percentage points.

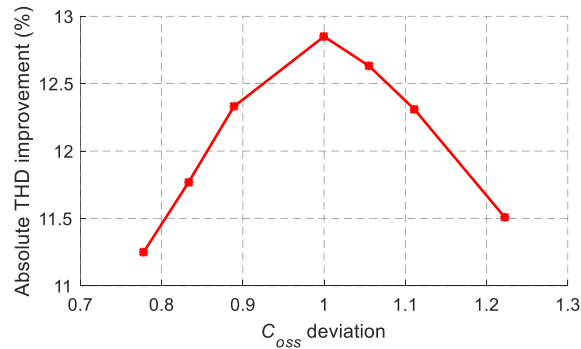


Fig. 5-48. The absolute THD reduction with the proposed compensation scheme vs the deviation of C_{oss} at 450 kHz switching frequency, 600 V_{DC}, 115 V_{AC}, and 1.3 kW Load.

If C_{oss} is far away from the datasheet value, the real value can also be obtained through actual testing as already illustrated in Fig. 5-47.

5.4.8 Implementation of dynamic compensation

In the above compensation scheme, R_{target} varies as loading condition changes. Thus, the compensation terms (5-31) and (5-35) for SPWM and SPWM+3rd injection cases, and their boundary conditions, respectively, have to be updated online. Seemingly, this adds the computation effort. Especially for the latter case, since there are one trigonometric function and one square root function in (5-37), one square root function in (5-36), and an extra variable α , implementation considerations have to be made to simplify the mathematical calculation and reduce the computation burden, if applying this scheme to a relatively lower speed DSP.

Since $\sin(\theta)$ is already a known variable from PLL park transformation, α calculation is not a concern. The concern is the boundary duty cycle d_{th} calculation. To simplify it, a quadratic polynomial curving fitting equation is adopted to update d_{th} as a function of R_{target} variation for different loading conditions as shown in Fig. 5-49. Fig. 5-50 shows a good match between the fitted equation and the analytical equation in the SPWM+3rd injection case.

$$d_{th}(x) = p_1 * x^2 + p_2 * x + p_3 \quad (5-42)$$

where x is the ratio of R_{target} change with the rated load as the base, indicating different load percentages.

In further, R_{target} can be updated in each control cycle or in a relatively slow rate to save the computation effort, from two known variables voltage V_d and current I_d in the d-q rotated frame.

$$R_{target} = \frac{V_d}{I_d} \quad (5-43)$$

With that, only the condition when $d < d_{th}$ in (5-35) needs one square root calculation. For typical DSP controllers such as TI 28x+FPU family, the computation burden of one square root is relatively low.

As one may also notice, the control target (5-28) is a steady-state instantaneous current, during the transient, there may be certain compensation inaccuracy since the target resistance will suffer transient change. If the load change is fast, then i_N will also go to the new steady-state load rapidly. The model inaccuracy in the very short control transient thus can be neglected. If the load change is relatively slow, during this transient, under d-q rotating frame, i_N or i_d will be a linearly changing “dc” variable. Under this condition, the defined R_{target} will be dynamically updated based on measured v_d/i_d under d-q frame as shown in (5-43). In fact, the link from (5-25) to (5-29) is to represent ac input voltage v as $R_{target} * i_{ph}$. As long as R_{target} is updated faster enough, the transient will be taken care of. In further, actually, the main drive for the turn-off compensation is to improve the power quality, i.e. to reduce the THD. THD, similar to power factor, is more like a steady-state disturbance index. Now that the compensation can ensure the good steady-state compensation, it helps to reduce current THD.

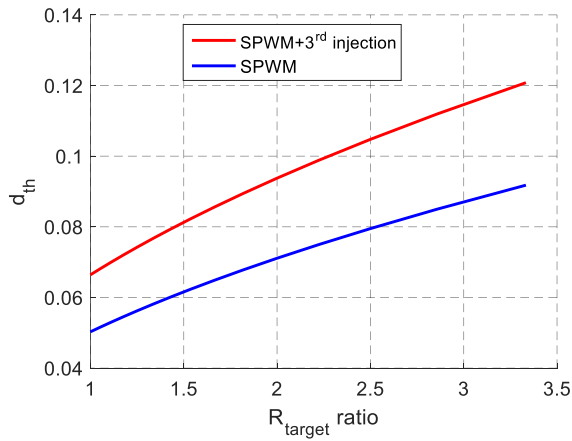


Fig. 5-49. d_{th} as a function of R_{target} change in two modulation cases.

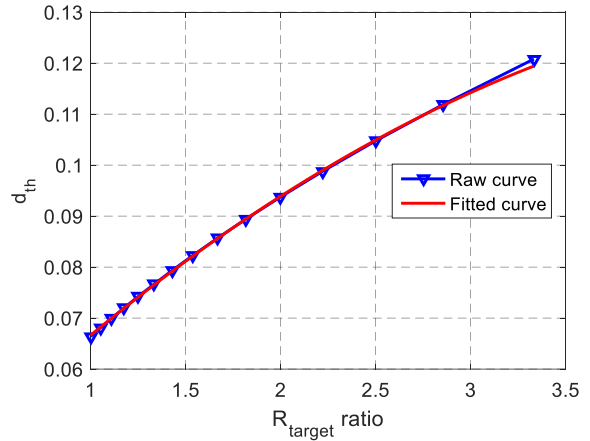


Fig. 5-50. Fitted d_{th} in SPWM+3rd injection case.

5.4.9 Impact factors on current and voltage distortion

Since the derived general modulation compensation term reveals the intrinsic relationship between the distortion and circuit parameters, the duty cycle ratio below can be a more effective index to predict the distortion impact from circuit parameters, instead of using the final THD obtained through simulations or tests as the indicator.

$$\frac{\Delta V}{V_1} = \frac{\Delta d}{d} \quad (5-44)$$

From (5-35) and (5-44), it is clear that for a given equivalent input resistance, the duty cycle loss is impacted by switching frequency, voltage-dependent junction capacitances of diodes and switches, and the instantaneous duty cycle reversely proportional to dc voltage. Therefore, influences from both f_s and dc voltage for the selected devices are studied.

From Fig. 5-51, it can be inferred that the distortion ratio will rise as f_s increases. With the assumption that the equivalent capacitance is a fixed value. Fig. 5-52 shows that the absolute distortion stays nearly the same as dc voltage increases, yet the distortion percentage becomes high, due to the reduction of the ideal duty cycle d . Fig. 5-53 shows that even if the charge-equivalent capacitance is considered for different dc bus voltages, as shown in Fig. 5-54, the change of the absolute duty cycle loss is still fairly trivial. As a result, the voltage distortion percentage still increases at higher dc voltage. Impacts of dc voltage and f_s in SVM case are shown in Fig. 5-55 and Fig. 5-56. The phase current's fundamental component is determined by the voltage difference between the ac source and the converter terminal, which is fixed for a given power. However, its harmonics are only determined by voltage distortion at the converter ac terminal assuming a harmonic-free ac source. Therefore, the current distortion is controlled purely by the dc voltage and the duty cycle loss as given below. Based on the above discussion, dc voltage and its associated capacitance dominate the current distortion.

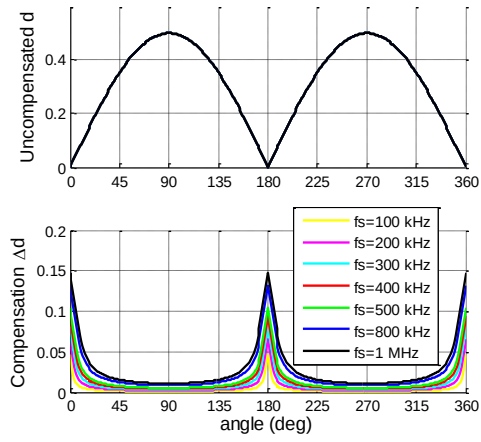


Fig. 5-51. Duty cycle compensation vs. f_s .

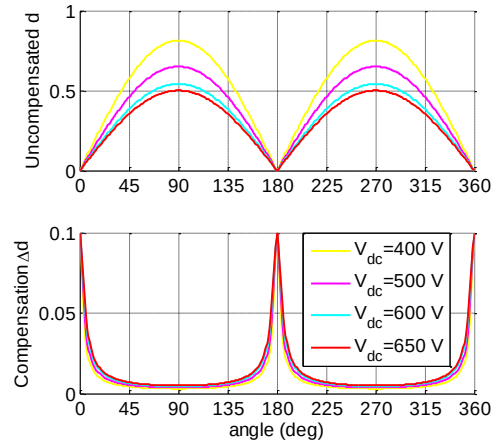


Fig. 5-52. Duty cycle compensation vs. dc link voltage.

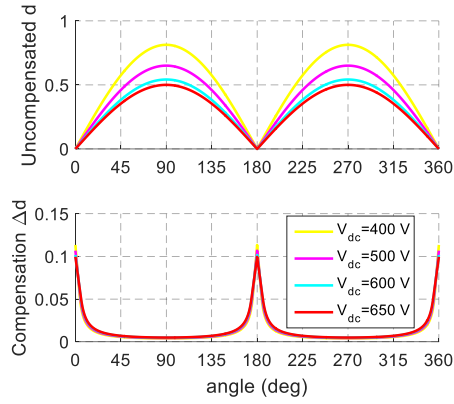


Fig. 5-53. Duty cycle compensation considering nonlinear C_{oss} .

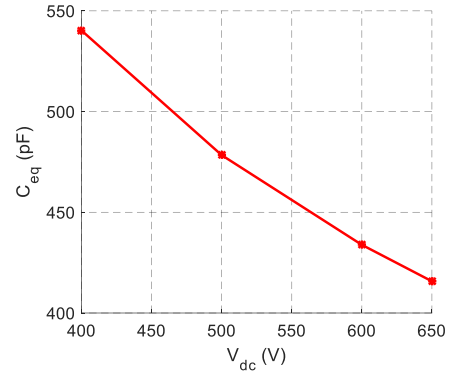


Fig. 5-54. Charge-equivalent C_{oss} vs. dc link voltage.

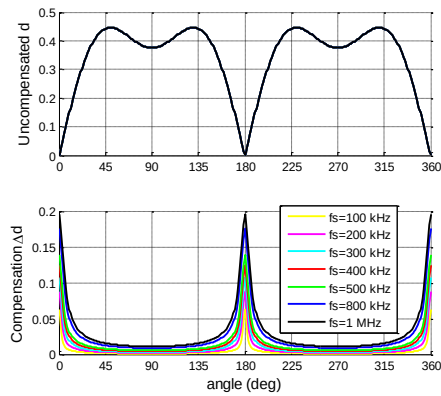


Fig. 5-55. Duty cycle compensation vs. f_s for SVM.

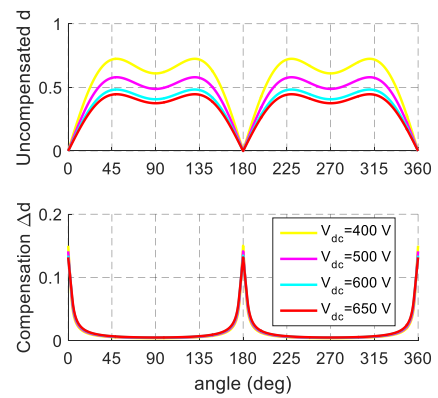


Fig. 5-56. Duty cycle compensation considering nonlinear C_{oss} for SVM.

$$\Delta i_h = \frac{0.5V_{dc}\Delta d}{Z_L} \quad (5-45)$$

Similar conclusions can also be obtained for the case with SPWM + 3rd harmonic injection.

5.4.10 Analytic modeling of turn-off voltage and current distortion

One should note that the proposed approach is valid in the absolute duty cycle form. If expressed in ac duty cycle form, the final duty cycle should be arranged as

$$d_{final} = d + \text{sign}(0 < \theta < \pi) \cdot \Delta d \quad (5-46)$$

This presented approach not only compensates the current distortion, in fact, it provides an accurate analytic model for output PWM voltage distortion as a function of dc-link voltage, ac operation point, device junctions capacitance, and converter switching frequency. The impacts of these variables can all be predicted through this model without running simulation or experimental tests.

The voltage distortion can be evaluated from the ratio of total distorted voltage (TD_V) to fundamental main voltage. Without tedious FFT calculation, it can be easily derived as (5-47), based on the simple fact that duty cycle compensation term equalizes to the distorted duty cycle. Its relationship with THD_V is given in (5-48). The only difference is that the fundamental component ΔV_1 of the compensation term ΔV_{RMS} is not regarded as harmonic.

$$TD_V = \frac{\Delta V_{RMS}}{V_{1_RMS}} = \frac{\Delta d_{RMS}}{d_{RMS}} = \frac{\Delta d_{RMS}}{M/\sqrt{2}} \quad (5-47)$$

$$THD_V = \frac{\sqrt{\sum_{h=2} V_h^2}}{V_{1_RMS}} = \frac{\sqrt{\Delta V_{RMS}^2 - \Delta V_1^2}}{V_{1_RMS}} = \sqrt{TD_V^2 - \left(\frac{\Delta V_1}{V_{1_RMS}}\right)^2} \quad (5-48)$$

Current distortion on the other hand, as illustrated in Fig. 5-57, is not only determined by voltage distortion, but also impacted by filter's frequency dependent impedance. Moreover, for three-phase three-wire converters, the current of one phase is also determined by the voltage of other two phases. Meanwhile, it is noticed that the current feedback controller also partially

suppresses the harmonics, depending on controller bandwidth and control gains at specific harmonic frequencies. Nonetheless, the harmonic current induced by phase b and c on phase a, i.e. $\Delta i_{b,a}$ and $\Delta i_{c,a}$ can be derived via the superposition law, as illustrated in Fig. 5-57.

$$\Delta i_{x,a} = \frac{1}{2} \frac{\Delta v_x}{Z_L + 0.5Z_L} \quad (x = b, c) \quad (5-49)$$

$$\Delta i_a = \Delta i_{a,a} - \Delta i_{b,a} - \Delta i_{c,a} = \frac{\Delta v_a - 0.5(\Delta v_b + \Delta v_c)}{1.5Z_L} = \frac{0.5V_{dc}(\Delta d_a - 0.5(\Delta d_b + \Delta d_c))}{1.5Z_L} \quad (5-50)$$

Let

$$\Delta d_{a,eq} = \Delta d_a - 0.5(\Delta d_b + \Delta d_c) \quad (5-51)$$

$$\Delta i_a = \frac{V_{dc} \Delta d_{a,eq}}{3Z_L} \quad (5-52)$$

Thus, for any phase, its current THD can be derived as a function of Δd_{eq} .

$$\begin{aligned} THD_I &= \frac{\sqrt{\sum_{h=2} \Delta i_h^2}}{I_1} = \frac{\sqrt{\sum_{h=2} (V_{dc} \Delta d_{eq,h})^2 / (3 \cdot 2\pi f_0 h L)^2}}{I_1} \\ &= \frac{V_{dc}}{6\pi f_0 L I_1} \sqrt{\sum_{h=2} (\Delta d_{eq,h} / h)^2} \end{aligned} \quad (5-53)$$

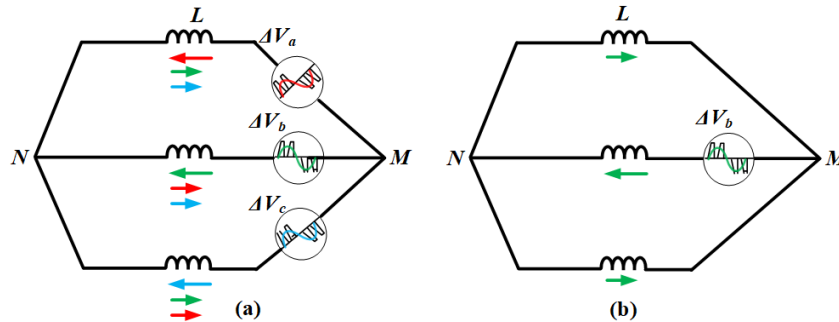


Fig. 5-57. Illustration of the harmonic current derivation based on superposition law in a three-phase converter. (a) Equivalent circuit of three-phase distortion. (b) Equivalent circuit of single phase distortion.

It should be mentioned that the distortion term (5-51) itself constrains all odd harmonics, as shown in Fig. 5-58. However, 3k orders are all removed due to the three-wire setup. And the fundamental distortion component should also be removed because feedback control has almost zero error tracking in the fundamental current. In addition, it is up to the users to determine if 5th

or 7th should consider the partial rejection from feedback control, depending on the specific control bandwidth and line frequency. In fact, from (5-53), although it seems high f_0 reduces the current THD, the dropped control bandwidth/ f_0 ratio, on the other hand, loses the harmonic rejection capability of feedback control, leaving THD_i more dependent on the voltage distortion. It is also clear that the lower-order current harmonics contribute more than the higher-order harmonics due to higher $\Delta d_{eq,h}/h$.

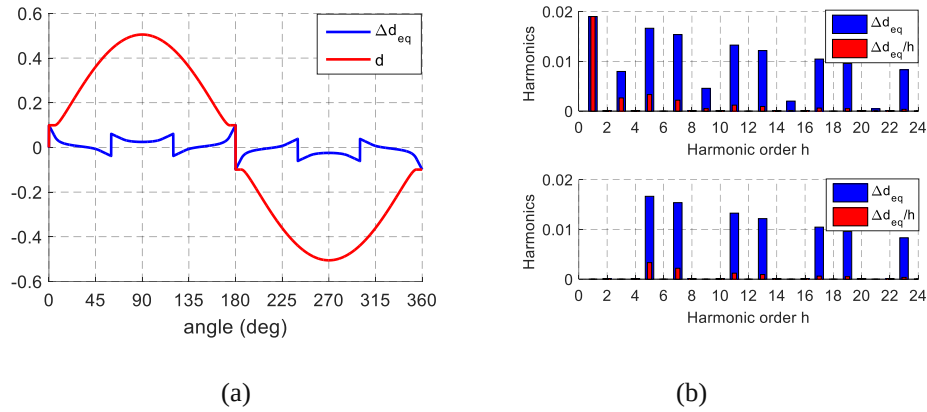
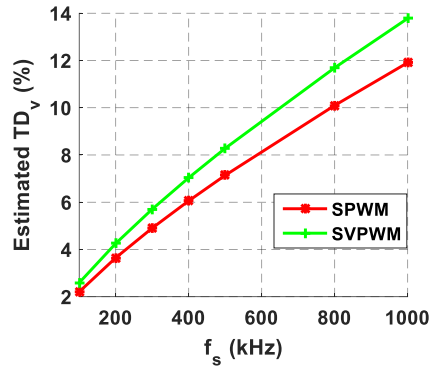


Fig. 5-58. Distorted duty cycle. (a) its waveform. (b) its harmonic spectra.

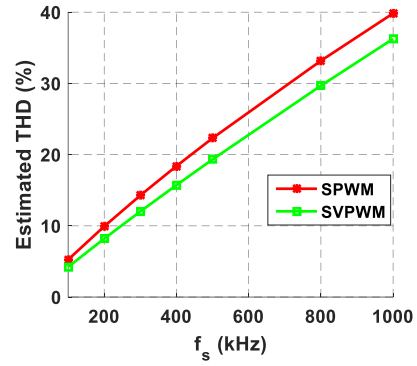
Theoretical impact of the impact vs. switching frequency on voltage and current distortion in a Vienna-type rectifier is illustrated in Fig. 5-59. For the given device and operation condition, only when the frequency is above 100 kHz, this distortion gets pronounced. Please notice that in the subject design case, the theoretical current THD without compensation is relatively high, since the fundamental current is very low, only 4.3 A_{rms}, and the result here also excludes the partial harmonic rejection from the current controller in an actual converter.

5.4.11 Simulation results

A simulation was constructed to verify this distortion phenomenon and the compensation performance, with ac input phase voltage 115 V rms, dc voltage 600 V, and 1.3 kW load. Constant output capacitances were used to simplify this simulation model. The result is shown in Fig. 5-60.



(a) Modeled terminal voltage distortion.



(b) Modeled ac current distortion.

Fig. 5-59. Modeling of the turn-off distortion vs. switching frequency for three-phase Vienna-type converters.

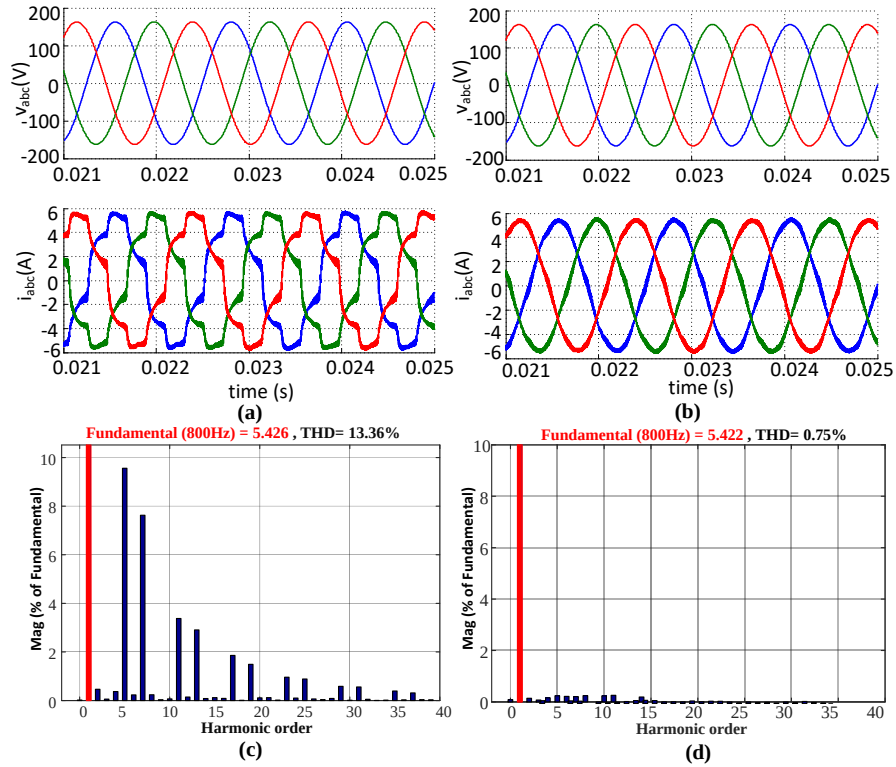


Fig. 5-60. Simulated phase voltage, current, and harmonic spectra. (a) ac side voltage and current without compensation (b) ac side voltage and current with compensation (c) phase A THD without compensation (d) phase A THD with compensation.

The dynamic performance of this compensation scheme is also verified under the load change condition. A simulation with a step-down load change from full load to half load is provided. As shown in Fig. 5-61 and Fig. 5-62, the proposed control can improve the current quality at both full load and light load, and the transient of load step change is smooth.

5.4.12 Experimental verification

The derived modulation compensation scheme was also verified through a three-phase Vienna-type rectifier prototype operating at 450 kHz with forced cooling, as demonstrated in Fig. 5-63.

5.4.12.1 Steady-state Compensation Results

Without an accurate voltage error compensation scheme, an obvious distortion was observed in the input currents, mainly consisting of $6k \pm 1$ order harmonics due to the six zero crossings of the three phases as shown in Fig. 5-64. After applying the proposed scheme, those harmonics were significantly suppressed, and the current THD was reduced from 10.3% to 3.0%.

This result also highlights the importance of the feedforward type compensation, especially for cases with moderate speed DSP controllers. The online implementation of such a modulation compensator for three phases in C code requires less than 800 ns computation time.

To further verify the accuracy of the compensation model, a comparison was made between the effective ac-terminal duty cycle $d_{effective}$ and the controller output d_{vgs} without the compensation. Here, the actual ac-terminal duty cycle is acquired from the averaged v_{ds} divided by the dc voltage, and d_{vgs} is based on the averaged gate voltage v_{gs} divided by its magnitude. From Fig. 5-65, it is clearly seen that the distortion from device capacitance causes about 0.1 maximum turn-off duty cycle loss in the zero-crossing region excluding the measurement error, which matches the desired compensation term calculated in (5-35) and Fig. 5-41.

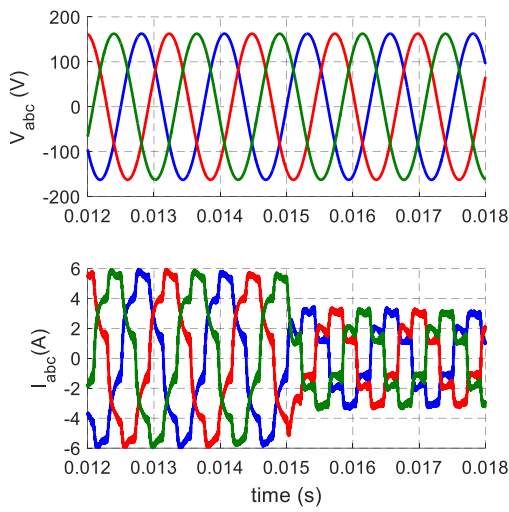


Fig. 5-61. Simulated ac input current waveforms without compensation under a load step-down change.

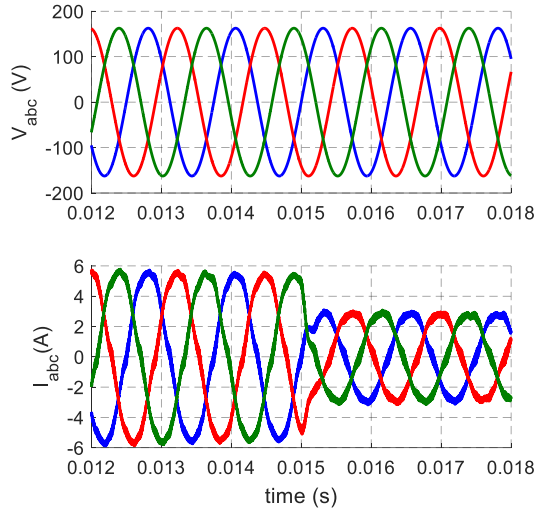


Fig. 5-62. Simulated ac current waveforms with the proposed compensation under a load step-down change.

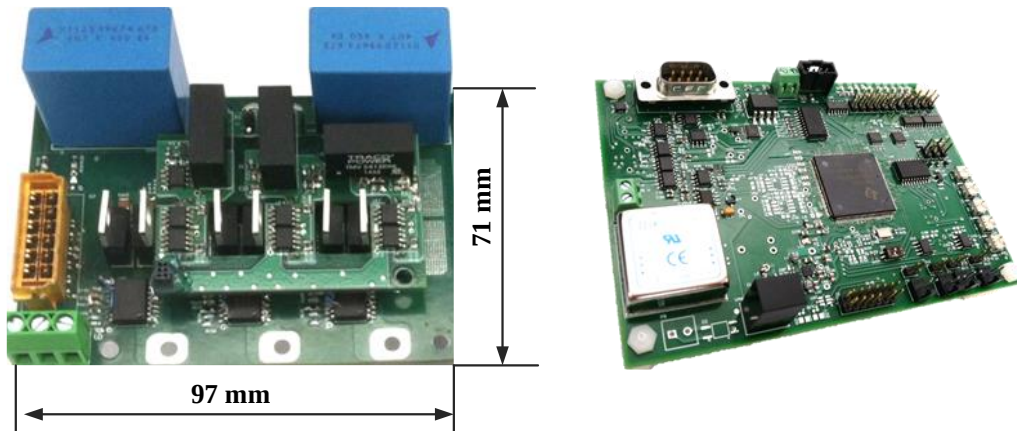
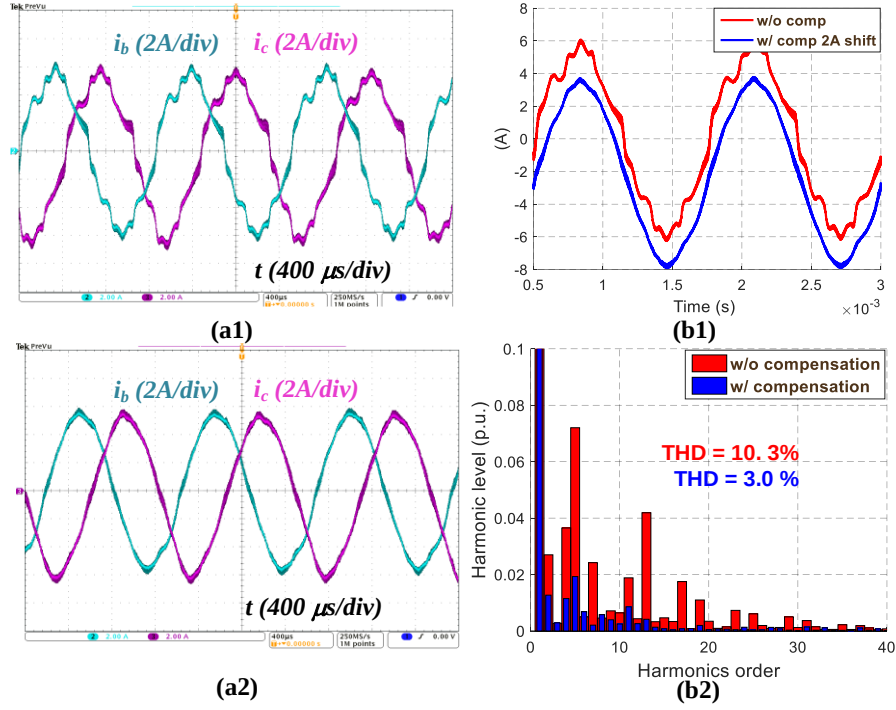


Fig. 5-63. Prototype of the three-phase three-level Vienna-type rectifier and its controller board.



(a1-a2) Experimental waveforms of i_b and i_c current without and with compensation.

(b1-b2) Comparison of i_b current without and with compensation. (blue curve in (b1) is shifted down by 2 A)

Fig. 5-64. Experimental comparison of current quality with and without the proposed compensation scheme.

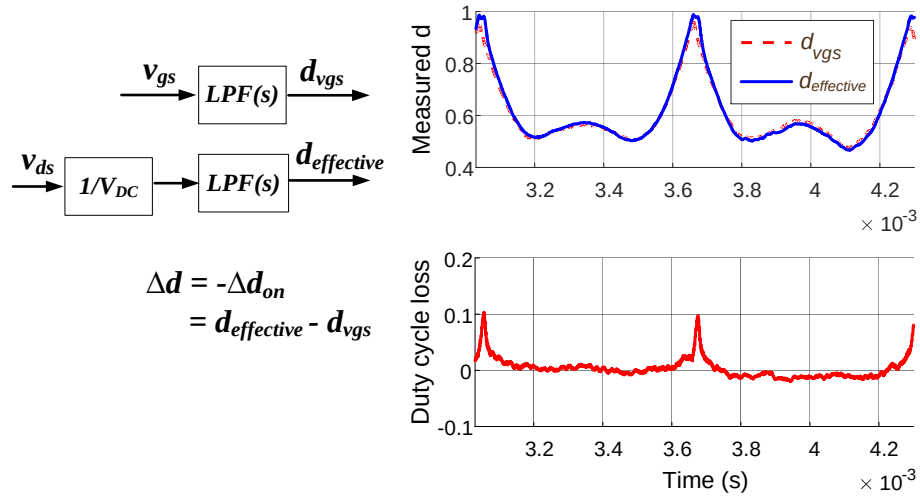


Fig. 5-65. The turn-off duty cycle loss derived from testing waveforms without compensation.

The compensation scheme was also tested at light load. Fig. 5-66 shows the input current waveform without and with the compensation. Severe distortion is observed when the compensation is not activated. Once it is enabled, the input current quality is effectively improved. A certain 2nd order harmonic is still visible due to the imperfect of dc voltage balance control. This is because the proportional gain of dc voltage balance controller should be enhanced at low load [321].

5.4.12.2 Dynamic Compensation Results

To verify the effectiveness of the proposed turn-off compensation scheme, both load step-down and step-up tests were conducted. Fig. 5-67 shows the load step-down result from 1.5 kW to 1.15 kW under 450 kHz, 115 V_{rms}, and 625 V_{DC}. Fig. 5-68 provides the load step-up result from 650 W to 1.3 kW. The transitions are smooth with good current quality for the three loading conditions. A certain 2nd order harmonic is observed in the 650 W condition, which is because of the insufficient gain of dc voltage balance controller at light load, as discussed before.

Finally, to demonstrate the impact of switching frequency on current distortion, the switching frequency was intentionally reduced to 112.5 kHz (¼ of 450 kHz). As shown in Fig. 5-69, even without compensation, the phase A current in the green curve still looks quite sinusoidal with fewer harmonics in the 6k±1 order, and its THD is only 6.2%, much less than the 450 kHz result with no compensation applied. In this case, the higher current ripple on the phase current is because of the intentionally reduced switching frequency.

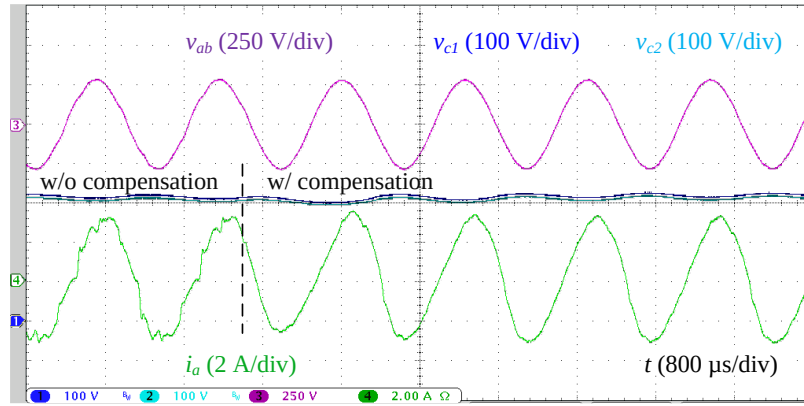


Fig. 5-66. The input current waveform without and with the proposed compensation under 650 W load condition.

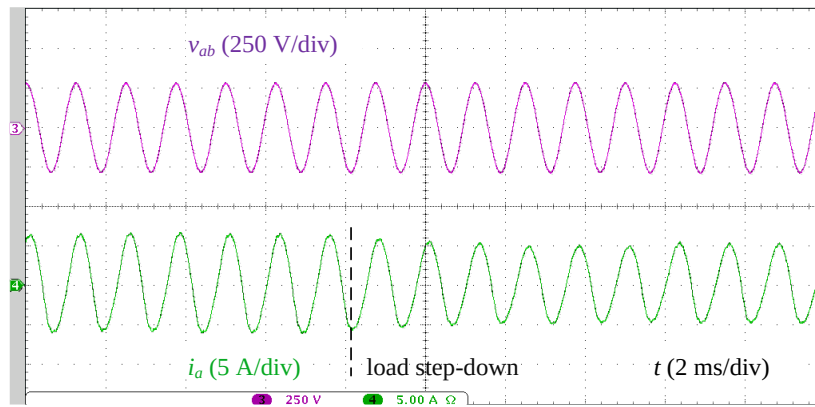


Fig. 5-67. Experimental ac input current waveforms with proposed compensation under a load step-down change.

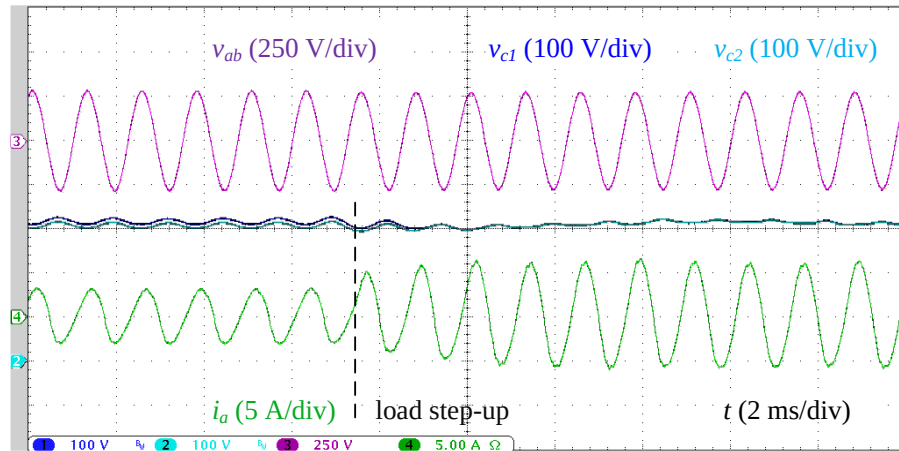


Fig. 5-68. Experimental ac input current waveforms with proposed compensation under a load step-up change.

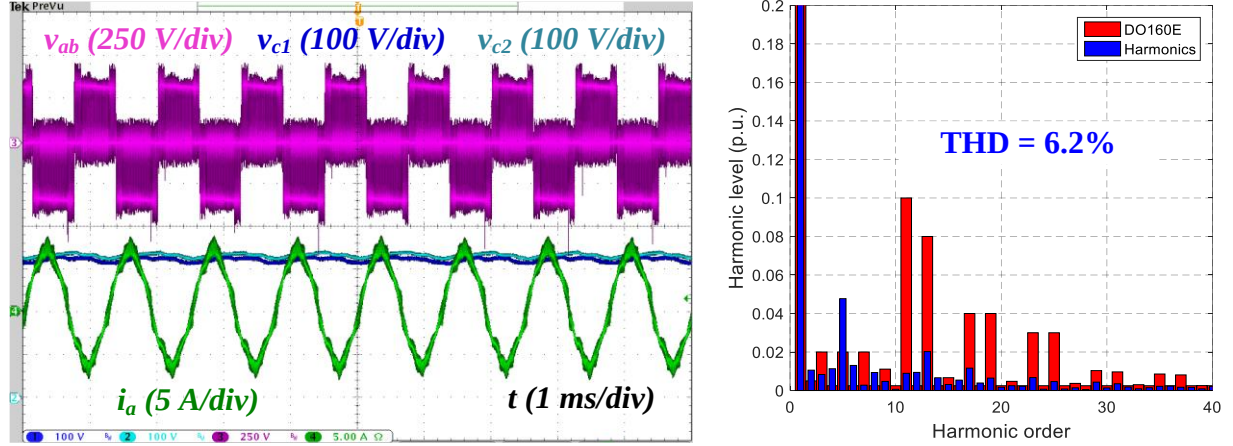


Fig. 5-69. Experiment waveforms and input current spectra when f_s is reduced from 450 kHz to 112.5 kHz, at 115 V_{AC} rms, 650 V_{DC} , and 1.5 kW load.

5.5 Impact of overlooked device parasitics on three-level converters and re-evaluation

5.5.1 Mechanism of extra device parasitics' impact on three-level converters

Three-level converters are widely used owing to half device rating, low EMI emission and low harmonics and ripples as a result of low dv/dt , and low filter size. Classic three-phase three-level converters consist of unidirectional rectifiers such as several Vienna-type variants, and bidirectional converters such as NPC converters (I-type), T-type converters, and flying capacitor based variants. Deep understanding of the switching commutation loop in these converters' operation is critical for high-efficiency, high-density, and high-reliability converter design. Benefited from it, correct switching loss estimation is also critical for power devices selection, evaluation of different topology candidates, and thermal design. Although these aspects have been studied in the past decades for three-level converters in Si converters, e.g. the analytical loss calculation for Vienna-type rectifiers in [43, 143, 155, 322] and commutation and loss analysis for T-type converters [323, 324] and for NPC converters [325-328], some important effects of other switching commutation paths and related capacitances inherent in three-level ac/dc converters

were overlooked. The cause and impacts which may be less important at the low switching frequency and speed become significant at high switching speed and switching frequency.

In this section, extra device junction capacitances and switching commutation paths in three types of classic three-level converters, including Vienna-type rectifier variants, T-type converter, and different NPC types, are presented. The effect of the extra switching commutation path and related capacitance will be disclosed. Their impact on switching loss is analyzed with a new loss calculation method proposed. The impact on voltage stress of power devices is studied.

5.5.1.1 Vienna-type rectifiers

Three famous Vienna-type rectifier variants are considered, as shown in Fig. 5-70. Variant (a) has only a single switch but two diodes conducting current per phase. Variant (b) has doubled switches but shared switching loss and shorter switching loop. Although all the semiconductors of both topologies are claimed to have half dc voltage, voltage stress of the two series diodes in either upper or lower phase leg are not directly defined in the circuit structures [141, 322, 329]. Variant (c) has fewer diodes thus lower conduction loss but full bus voltage stress on these diodes. This alternative becomes more popular thanks to the recent development of SiC Schottky diodes with high blocking voltage capability and zero reverse reversal loss.

Owing to the simplicity in topology structure, variant (c) will be studied first. And only a positive half line cycle is illustrated for brevity as shown in Fig. 5-71. In the conventional analysis, the switching commutation occurs between S_1 and D_1 . During the turn-on transient, when V_{gs} passes the gate threshold, S_1 channel begins turning on and channel current increases. Within this current rising interval, the phase current is commutated from D_1 to S_1 . When phase current is fully commutated, D_1 is blocked. Then, the junction capacitance C_{D1} of D_1 is charged by dc bus through S_1 channel, and the output capacitance C_{oss} of S_1 is also discharged from its channel.

The missing part, however, is when C_{oss} is discharged from $V_{dc}/2$ to zero, the terminal voltage also changes from V_{dc} to $V_{dc}/2$. Therefore, the joint junction capacitance C_{D2} of the bottom diode D_2 will be statically discharged via channel resistance of S_1 , resulting in extra turn-on switching loss. Since this path will not conduct current for the half line cycle, it can be easily missed.

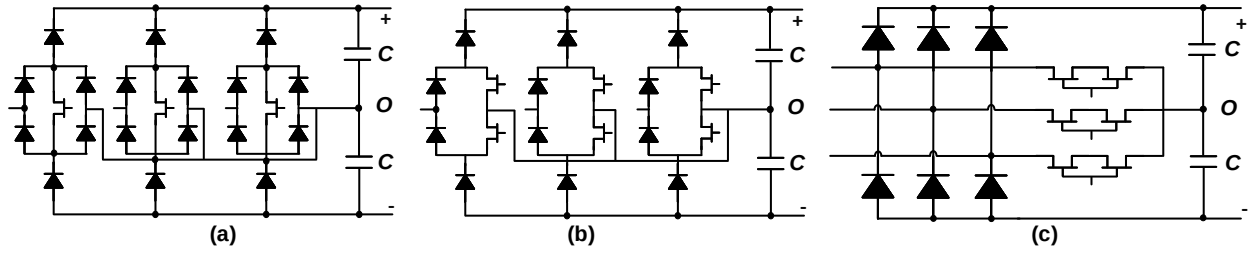


Fig. 5-70. Three common Vienna-type variants. (a) [330]. (b) [331, 332]. (c) [141, 333, 334].

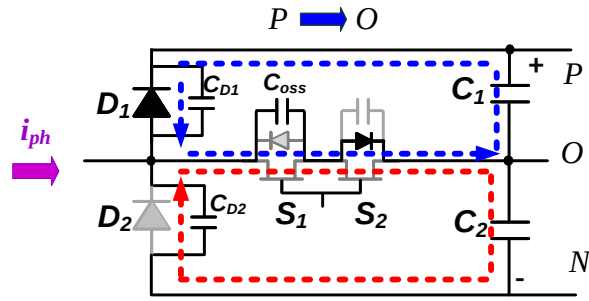


Fig. 5-71. Commutation loops with extra capacitance involved in Vienna-type three-level rectifier variant (c).

In fact, the root cause of this effect for three-level converters can be explained as follows. In three-level converters, three switching branches (positive branch, neutral branch, and negative branch) form a T connection instead of an I connection in two-level converters (positive and negative branches). In each half line cycle, although the complementary branch does not conduct current flow, the junction capacitance of this branch can be statically charged or discharged if the complementary branch sees a switching potential difference. From this sense, this capacitance C_{D2} can be regarded as a paralleled output capacitance across the main switch from the ac signal perspective, where the dc-link capacitor C_2 is shorted.

For the other two variants (a) and (b), similar analysis can be carried out. The extra capacitances involved in commutation from the positive level to the neutral level are shown in Fig. 5-72 (a) and (b). For variant (a), if with the proper balance design, the structurally undefined voltage stress for D_{LF1-} and D_{HF-} can be balanced at half V_{dc} [141, 322, 329]. Then, the voltage of D_{HF-} will maintain at $V_{dc}/2$, while the voltage of D_{LF2-} maintains at zero volt during the turn-on transition. As a result, C_{LF-} is discharged from $V_{dc}/2$ to zero volt via the main switch S_1 , and C_{LF2+} is also discharged from $V_{dc}/2$ to zero volt via the main switch S_1 . Therefore, these are the extra capacitances in addition to junction capacitances of the main switching components S_1 and D_{HF+} .

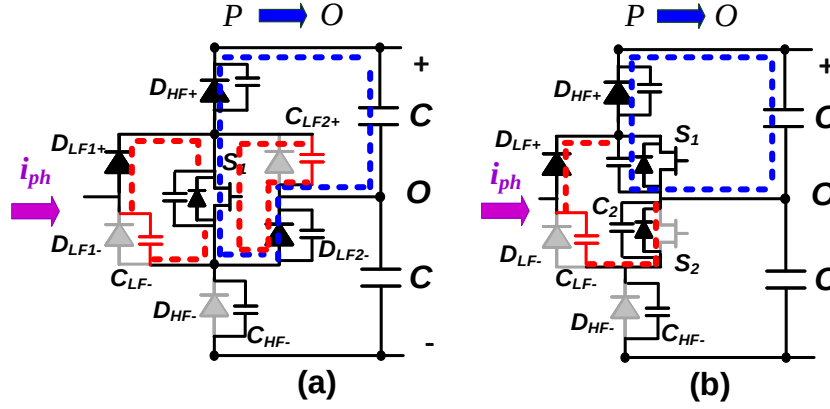


Fig. 5-72. Commutation loops with extra capacitance in Vienna-type three-level rectifier variant (a) and (b).

Similarly, for variant (b), if voltage stress for D_{LF-} and D_{HF-} can be balanced at half V_{dc} , then the voltage of D_{HF-} will maintain at $V_{dc}/2$, while the voltage of D_{LF2-} maintains at zero volt during the turn-on transition. Only junction capacitance C_{LF-} of D_{LF-} forms an extra C_{oss} capacitance to the switch S_1 . Otherwise, if blocking voltages of D_{LF-} and D_{HF-} in off-state of S_1 are not balanced, extra capacitances from C_{HF-} and C_2 will also be involved in the commutation loop, leading to more switching loss as well as voltage stress.

Since the above capacitances are all voltage-dependent, their specific C_{oss} characteristics should be included in the analytical loss calculation. Otherwise, double pulse tester (DPT)

representing the three-level structure of a phase-leg should be used, instead of the conventional DPT with only the switch/switch (S-S) or switch/diode (S-D) pair.

5.5.1.2 T-type converter

One phase leg of the T-type converter is shown in Fig. 5-73.

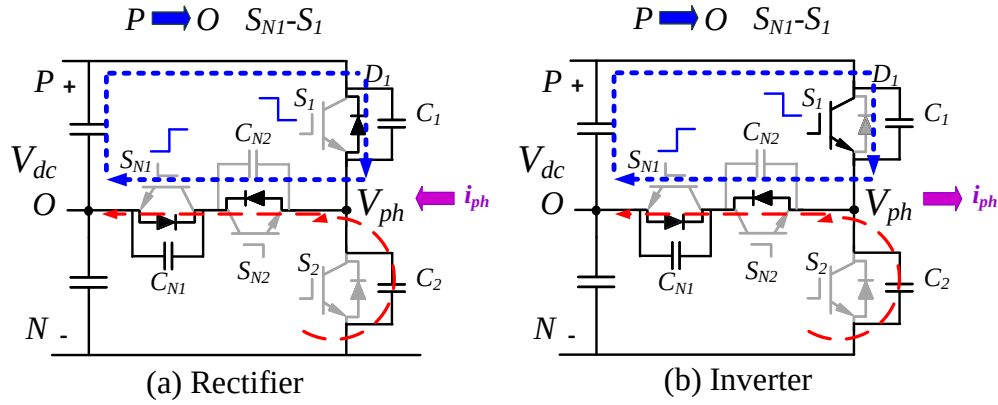


Fig. 5-73. Commutation loops with extra capacitance involved in T-type three-level converter.

Because of the replacement of two diodes with active switches from the Vienna-type rectifier, commutation of T-type converter can be current independent and in four quadrants. However, the similar capacitance effect can still be observed. Transitions from the positive level to the neutral level in both rectifier mode and inverter mode are analyzed as an example. In both cases, in addition to the conventional switching loop marked in blue, there is another discharging path from the junction capacitance C_2 of S_2 in the complementary branch to the channel of the neutral switch S_{N1} . This branch is missed in the prior literature. To compensate the missed loss in prior calculation, the voltage-dependent characteristics of C_2 should be considered.

5.5.1.3 Diode NPC (DNPC) rectifiers/inverters

The modulation schemes and switching commutation loops of DNPC have been extensively studied [325, 335]. As shown in Fig. 5-74, in inverter case with power factor (PF=1), the outer switch S_1 and clamping diode D_p are operated at high frequency (HF) to form the positive level

and neutral level for the positive half line cycle (i.e. outer mode), while S_4 and D_n form the negative level and neutral level for the negative half line cycle (i.e. outer mode). In rectifier case with $PF=-1$, the inner switch S_3 and S_1/D_1 are switched at HF to synthesize the positive level and neutral level for the positive half line cycle (i.e. the inner mode), while S_2 and S_4/D_4 are responding for the negative line cycle.

Still, there are missing device junction capacitances in the prior analysis. The inverter $PF=1$ operation which has only the outer mode is firstly analyzed, illustrated in the first quadrant. When S_1 is turned on, in addition to the classic commutation loop as marked in blue, the switching node voltage on the drain of S_3 increases from $V_{dc}/2$ to V_{dc} . As a result, a static charging current charges C_3 and C_4 of the blocked switches as well as the paralleled path C_n of the clamping diode D_n till the end of the turn-on commutation. Therefore, an extra capacitance as an equivalence of the C_3 in series with parallel C_4 and C_n should be included in the turning on loss calculation.

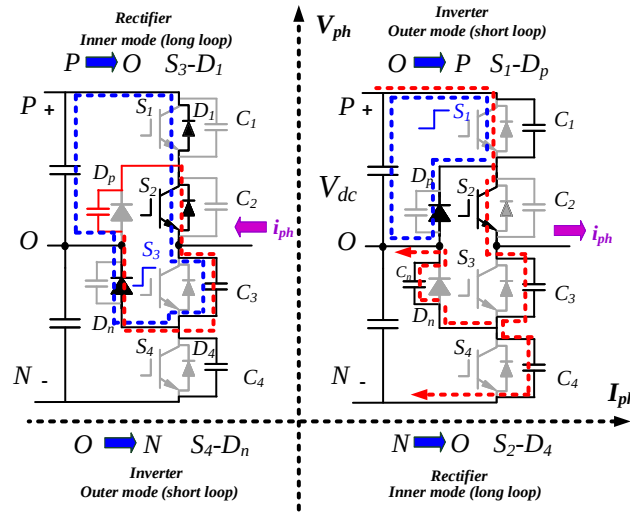


Fig. 5-74. Commutation loops with extra capacitance involved in DNPC, in the four-quadrant operation. (3rd and 4th quadrants are not shown)

Differently, rectifier $PF=-1$ operation has only inner mode modulation. Since it utilizes the inner switch S_3 as the main switch in the positive line cycle, the switching action has entered the

bottom branch. Consequently, S_3 becomes the only active switch involved in the upper branch switching loop. Meanwhile, the voltage of C_4 keeps at $V_{dc}/2$ before and after the turn-on transient thanks to D_n clamping. Therefore, C_4 and C_n do not contribute to the extra loss. However, the voltage across D_p decreases from $V_{dc}/2$ to zero during the transition. Therefore, an extra junction capacitance of D_p is introduced in this case, as marked in red. The other issues with this mode are higher voltage/current stress and switching loss because of the larger switching loop [325].

To summarize, based on the observation and analysis, the outer mode modulation in NPC during switching commutation will introduce extra static charged/discharged junction capacitance from the complementary branch, but this mode has short power loop. On the other hand, the inner mode has no such extra junction capacitance effect from the complementary branch but has one extra capacitance inside the commutation loop. In addition, this inner mode has long power loop, also owing to the extension of the communication loop into the complementary branch. Since PF=1 condition has only the outer mode, PF=-1 condition has only the inner mode, and other PF operations have the mixed modes [325], these general effects will be exerted on DNPC to different degrees as PF varies.

5.5.1.4 Active NPC (ANPC)

Because of the flexibility in controlling the clamping switches, ANPC has more freedom in modulations. Two conventional modulations are summarized in [325], i.e. the pure outer mode modulation applicable for all four-quadrants and all PFs, and pure inner mode modulation applicable for all four-quadrants and all PFs. An improved modulation was also proposed in [325], which is equivalently a combination of the inner mode and the outer mode. Since they are all rooted from the two basic modes occurring in DNPC, the aforementioned effects and conclusions are also applicable for these different modulations of ANPC. Details will not be presented.

5.5.2 Impact on power loss due to extra C_{oss} and loss re-evaluation approach from traditional DPT

5.5.2.1 Impact on loss

The extra C_{oss} has significant impacts on the switching loss. Its energy stored in the turn-off transient is dissipated in the turn-on interval, leading to extra turn-on switching loss. And the overlap time between the drain voltage and channel current is increased due to the extra displacement charging or discharging current, which concurs with the load current in the saturation interval of device switching transient. Thus, the overlap loss contributed by load current component in this saturation interval also grows higher. The extra loss is

$$P_{loss_extra} = (E_{on_Coss_extra} + E_{on_overlap_extra} + E_{off_overlap_extra}) f_s \quad (5-54)$$

5.5.2.2 Loss re-evaluation approach

To achieve correct loss calculation in a three-level converter, a straightforward solution is to build a DPT phase-leg with a three-level structure, instead of the half-bridge. However, this requires two dc power supplies, two bulky energy storage capacitors with balanced voltage, and a full revision of the widely adopted two-level DPT set up. Moreover, E_{on}/E_{off} data of commercial devices are all based on two-level DPTs. To facilitate the loss calculation taking into account of the extra loss, a method combining device C_{oss} information and conventional DPT data is proposed.

The C_{oss} related turn-on loss can be analytically calculated from the voltage-dependent extra junction capacitance in the aforementioned topologies, using measured or datasheet C_{oss} plus the stray capacitance. For simplicity, only the turn-on transition from the positive level to the neutral level in a three-level converter is analyzed.

The junction capacitance of the bottom switch C_{oss_static} is discharged from V_{dc} to half V_{dc} through the conducted channel of the natural switch. This part of energy can be derived as in

$$\begin{aligned}
E_{on_Coss_extra} &= \int_{T_s}^{T_s+T_{on}} (v_{Coss_static} - V_{dc}/2) \cdot i \cdot dt \\
&= \int_{V_{dc}/2}^{V_{dc}} v_{Coss_static} \cdot C(v_{Coss_static}) dv_{Coss_static} - \frac{V_{dc}}{2} \int_{V_{dc}/2}^{V_{dc}} C(v_{Coss_static}) dv_{Coss_static}
\end{aligned} \tag{5-55}$$

If defining the energy equivalent capacitance for this three-level case as

$$C_{eq,E} = \frac{\int_{V_{blocking}}^{2V_{blocking}} v_{ds} \cdot C(v_{ds}) dv_{ds}}{\frac{1}{2} V_{blocking}^2} \tag{5-56}$$

(5-55) can be reformed as

$$E_{on_Coss_extra} = \frac{1}{2} C_{eq,E,Coss_static} \left(\frac{V_{dc}}{2} \right)^2 - \frac{V_{dc}}{2} Q_{oss_static} \tag{5-57}$$

where Q_{oss_static} is the total charge from C_{oss_static} during this turn-on transition.

The analytical calculation of the overlap loss can be simplified as

$$E_{on_overlap} = E_{on_cr} + E_{on_vf} \approx \frac{1}{2} (t_{cr} + t_{vf_sat}) V_{DS} I_L \tag{5-58}$$

If the voltage drop of the active device is approximately linear. Here, E_{on_cr} is the overlap energy during the current rising time t_{cr} and E_{on_vf} is the overlap energy during the voltage falling interval t_{vf_sat} in the saturation region.

Although people tend to calculate this time from gate circuitry, using (5-58) is impractical because of the uncertainties of the overlap time, as it is a function of many factors, such as gate drive voltage, total charge, and temperature-dependent device transconductances. Instead, it is favorable to revisit the derivation from the output junction capacitances as the gate charging and C_{oss} discharging conduct simultaneously during the device saturation region. As will be analyzed, t_{vf_sat} can be strongly impacted by the extra C_{oss} . Therefore, additional C_{oss} not only increases the C_{oss} type loss, but also indirectly enlarges the overlap loss. The following work will show how this part of loss can be scaled from the C_{oss} information with data of conventional DPT.

The theoretical turn-on transient of the active neutral device is illustrated in Fig. 5-75. The gate voltage v_{gs} has non-flat Miller plateau for GaN or SiC WBG device, whereas, for Si device, the flat Miller plateau should be considered. The shaded area of the channel current denotes the total displacement charge in the T-shape phase leg. Different from a traditional half bridge leg consisting of Q_{oss_active} of the active device and Q_{oss_syn} of the synchronous device, an additional charge is contributed by the extra Q_{oss_static} of the bottom static device. Since current commutation and displacement charge occur after the current rising subinterval, the extra overlap loss affected by Q_{oss_static} is only generated in the following voltage falling subinterval t_{vf_sat} , and the switching loss in the short ohmic region is ignored because of the almost zero voltage and falling current.

Compared to the DPT set up of a two-level half bridge under the same device blocking voltage, the ratio of the turn-on overlap loss in this interval is

$$\frac{E_{on_vf_T}}{E_{on_vf_H}} = \frac{t_{vf_sat_T}}{t_{vf_sat_H}} \quad (5-59)$$

where the subscript T and H denote T-shape and half bridge, respectively.

From Fig. 5-75, the channel current in the current rising region and saturation region is

$$i_{chan} = g_{fs}(v_{gs} - v_{th}) \quad (5-60)$$

where g_{fs} is the large-signal transconductance of the device.

For devices with non-flat v_{gs} in the Miller plateau region such as GaN or SiC WBG devices, the total displacement charge Q_{oss_T} is derived as (5-61), whereas for Si devices, the flat Miller plateau effect should be considered and the reverse recovery charge should be excluded.

$$\begin{aligned} Q_{oss_T} &= Q_{oss_syn} + Q_{oss_active} + Q_{oss_static} \\ &= \frac{1}{2} g_{fs} \frac{dv_{gs}}{dt} t_{vf_sat_T}^2 \end{aligned} \quad (5-61)$$

leading to the saturation interval as

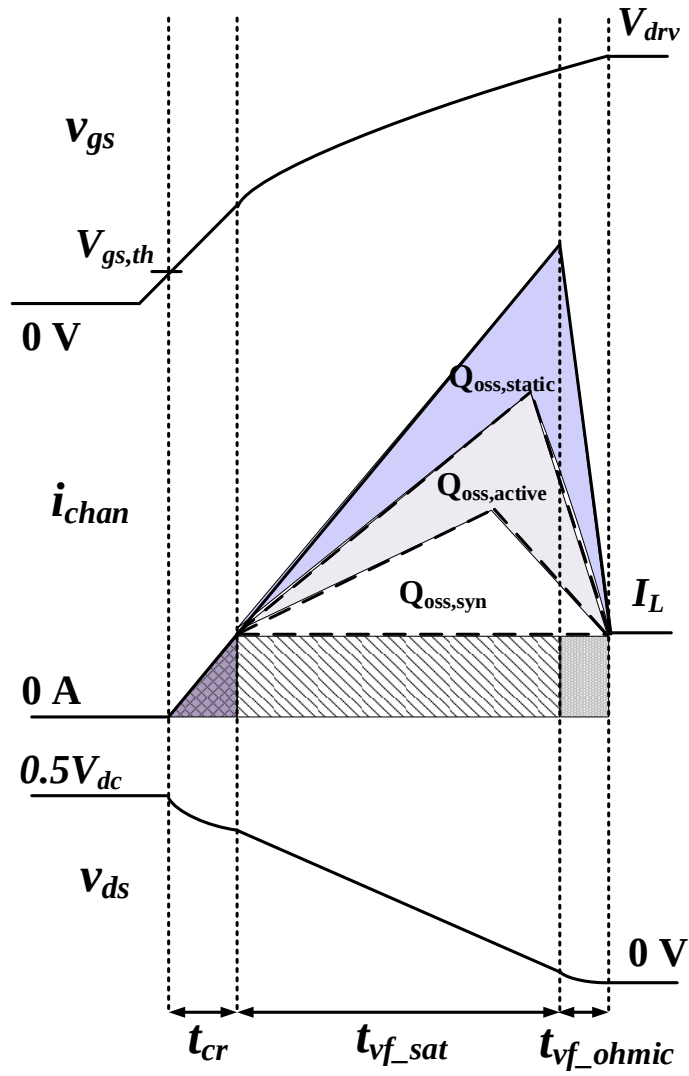


Fig. 5-75. Theoretical turn-on transient of the active neutral device.

$$t_{vf_sat_T} = \sqrt{\frac{2Q_{oss_T}}{g_{fs} \frac{dv_{gs}}{dt}}} \quad (5-62)$$

Together with (5-59) and (5-62), the overlap loss during turn-on saturation region in T-shape leg can be now scaled from the loss in a half bridge leg as

$$E_{on_vf_T} = \sqrt{\frac{Q_{oss_T}}{Q_{oss_H}}} \cdot E_{on_vf_H} \quad (5-63)$$

To obtain the $E_{on_vf_H}$, a further analysis is done to disclose the intrinsic relationship between the analytical energy calculation and DPT results.

From Fig. 5-75, one obtains

$$t_{cr} = \frac{I_L}{g_{fs} \frac{dv_{gs}}{dt}} \quad (5-64)$$

Thus, the total turn-on switching loss in a general bridge set up can be expressed as

$$E_{on} = E_{on_cr} + E_{on_vf} + E_{Coss_total} = \frac{V_{DS}}{2} \frac{1}{g_{fs} \frac{dv_{gs}}{dt}} I_L^2 + \frac{V_{DS}}{2} \sqrt{\frac{2Q_{oss}}{g_{fs} \frac{dv_{gs}}{dt}}} I_L + E_{Coss_total} \quad (5-65)$$

where E_{Coss_total} considers both the active device and energy stored in the synchronous device during the turn-off of the active device.

On the other hand, the measured E_{on} and E_{off} data from DPT are often curve-fitted well by a quadratic function

$$\begin{cases} E_{on_DPT} = k_1 I_L^2 + k_2 I_L + k_3 \\ E_{off_DPT} = k_4 I_L^2 + k_5 I_L + k_6 \end{cases} \quad (5-66)$$

By matching the two types of expressions, an interesting yet important hidden relationship between the physical and measured data is shown in

$$\begin{cases} E_{on_cr} = k_1 I_L^2 = E_{on_cr_DPT} \\ E_{on_vf} = k_2 I_L = E_{on_vf_DPT} \\ E_{Coss_total} = k_3 + k_6 = \sum E_{Coss_DPT} \end{cases} \quad (5-67)$$

where the measured constant k_6 in the turn-off transient represents C_{oss} energy of the active device dissipated during the next turn-on transient, thus is added to $E_{C_{oss_total}}$.

Therefore, $E_{on_vf_T}$ can be finally scaled from the linear term of the DPT result in a half bridge configuration

$$E_{on_vf_T} = \sqrt{\frac{Q_{oss_T}}{Q_{oss_H}}} \cdot E_{on_vf_H_DPT} \quad (5-68)$$

where the subscript T and H denote three-level and two-level, respectively.

It has to be mentioned that at higher junction temperature such as 150 °C, the lower g_{fs} and prolonged t_{vf_sat} may incur a special situation that v_{gs} reaches the driving level before the end of the saturation subinterval, and the channel current becomes saturated and flat [318]. In that case, some formulae in the above method need to be correspondingly modified, as presented in [318]. Nevertheless, for low temperature or low load current, the saturation current at the recommended driving voltage is much higher than the maximum load current, so that this special case will not generally occur.

For the turn-off transient, as already analyzed in Section 5.4.1, the channel for GaN device or Si MOSFET is usually shut off in a very short time depending on the gate driving speed and the saturation interval ends much earlier than the displacement charging interval. As a result, actual overlap loss excluding the C_{oss} energy is often much smaller compared to actual turn-on loss, and the loss impact from the static displacement charge of the extra device in this case is even smaller. In addition, the theoretical analysis of the turn-off overlap loss becomes complicated in determining the saturation time and its relationship with displacement charging. Therefore, the extra turn-off overlap loss is ignored to simplify the proposed method.

Some important conclusion can be drawn from the above analysis:

First, for GaN or SiC devices, the impact of the extra overlap loss is relatively low compared to that of the extra C_{oss} loss, owing to the high switching speed and short overlap time in these WBG devices. Another reason for this is that the overlap loss is proportional to $\sqrt{Q_{oss}}$ or $\sqrt{C_{oss}}$, while the C_{oss} loss is directly proportional to C_{oss} . Since WBG devices are expected in high switching frequency design, this type of loss will become significant for three-level converters.

Second, in certain high-current applications where the C_{oss} loss is not the dominant factor of the total switching loss, the presented loss impact could be highly determined by the extra overlap loss, especially for Si IGBT based three-level converters.

5.5.2.3 Temperature-dependent loss evaluation

To estimate the actual loss of a power converter, DPT test has been designed and tested with the specific device, gate driver, and layout under the actual junction temperature. The thermal test also requires dedicated test setup and is time-consuming. Therefore, it would be more convenient to predict and scale the temperature-dependent loss using the room temperature test result without elevating the device temperature. This also helps the converter thermal design in choosing the optimal temperature. Since the temperature correlation for GaN device is not strong in turn-off loss, a detailed analytical model is used to predict the temperature-dependent turn-on loss of GaN devices [318] and follows with a linear approximation method as shown in (5-69), using the ratio of the average temperature-dependent transconductance as the scaling factor. In this method, the assumption is made that the overlap loss mainly occurs during the voltage falling interval. Therefore, a minor error still exists due to the omission of the overlap loss during the current rising time.

$$E_{on,Tj} = \sqrt{\frac{g_{fs,25C}}{g_{fs,Tj}}} (E_{on,25C} - E_{Coss_total}) + E_{Coss_total} \quad (5-69)$$

Based on the relationship between the analytical loss and curve-fitted loss formula in Section 5.5.2.3, an improved prediction method is proposed to fulfill the loss approximation, in which the overlap loss over the current rising interval is further scaled by the reciprocal of the average transconductance ratio at two temperatures.

$$E_{on,Tj} = \frac{g_{fs,25C}}{g_{fs,Tj}} E_{on_cr,25C} + \sqrt{\frac{g_{fs,25C}}{g_{fs,Tj}}} E_{on_vf,25C} + E_{Coss_total} \quad (5-70)$$

5.5.2.4 Experimental verification

A GaN based Vienna rectifier variant (c) has been built up to verify this loss impact, with the photo shown in Fig. 5-63. Key operation parameters are 1.5 kW power, 450 kHz, 115 V_{rms}, and 650 V_{DC}. The calculated switching losses without and with considering the disclosed effect are 47.7 W and 55.6 W, respectively, as shown in Fig. 5-76, based on E_{on} and E_{off} data from a conventional half bridge DPT as reported in [186], with k₁ = 0.0214, k₂ = 0.9813, k₃ = 12.6478, k₄ = 0.0135, k₅ = - 0.0060, and k₆ = 9.0159 under 325 V_{dc} and 7 V gate drive voltage.

The energy equivalent junction capacitance of 30 A, 650 V GaN device GS66508P, as well as that of two 1200 V Cree SiC diodes, are also derived as C_{oss_GaN} = 98.0 pF, C_{SiC, D1} = 128.4 pF, C_{SiC, D2} = 222.3pF based on their operating voltage during the turn-on transient. All these capacitances are applied to estimate the loss impact for the subject issue. Additionally, heatsink coupling capacitance related loss and some other minor losses are included for both cases as the base.

As is also clearly shown, the pure turn-off loss is very small, confirming the validity of ignoring its extra loss from the statically charged device capacitance.

The actual power loss of the converter is measured using Yokogawa power analyzer PZ4000. To extract the switching loss of the converter, two efficiency measurements at different switching frequencies (450 kHz and 112.5 kHz) with other conditions the same are conducted. The actual

switching loss is extracted as 55.2 W, as given in Fig. 5-77 Fig. 5-78, based on the differential of two efficiency measurements at different switching frequencies (450 kHz and 112.5 kHz) and the fact that switching loss is proportional to switching frequency, assuming device conduction loss is fixed and boost inductor losses of two cases are almost the same. Although the actual inductors' loss can be varied at two different switching frequencies, their estimated total loss at the high fs case is only 6.0 W due to the low ac rms current and peak current. Thus, the error from the assumption is slight.

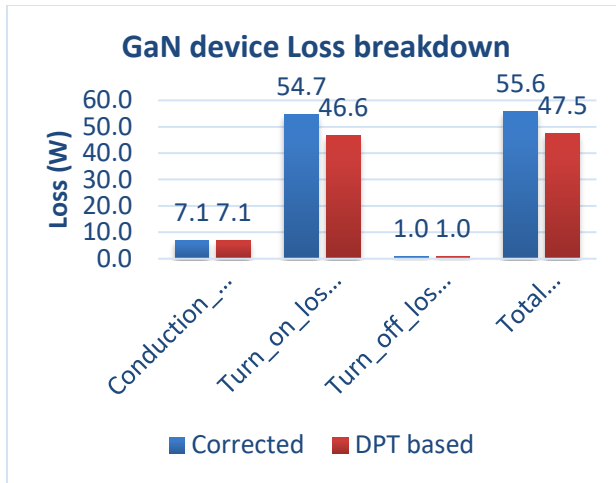


Fig. 5-76. Comparison of the device losses with and without the correction of the disclosed effect in a Vienna-type rectifier. (actual turn-off loss is negligible)

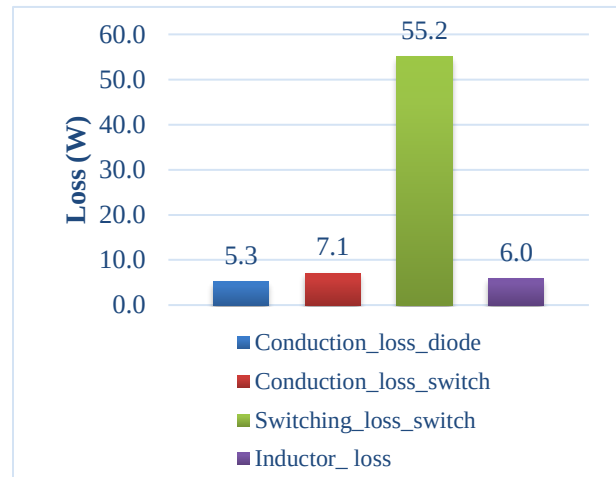


Fig. 5-77. Measured converter losses under the experimental condition 1.5 kW, 450 kHz, 115 ac input Vrms, and 650 V dc output.

It is therefore clear that the predicted switching loss after adding the extra C_{oss} is very close to the actual switching loss, and the impact from the extra C_{oss} is 8.1 W. Further breakdown shows that the extra overlap loss contribution is only 1.0 W while the C_{oss} part is 7.1 W. This is partially because of the root square of Q_{oss} ratio for overlap loss instead of the Q_{oss} ratio for the C_{oss} loss, and partially because the base overlap loss is small for high speed GaN device, especially at low load current application in the subject case.

5.5.3 Impact on device overstress due to extra power loop

In an actual converter, stray inductance from device package and PCB trace and power switching loop can resonate with the junction capacitance of the on-state device in a bridge configuration, leading to higher current stress of the active device and higher voltage stress of the synchronous device during the turn-on, and higher voltage stress of the active device during the turn-off.

Because of the extra C_{oss} of the statically charged or discharged device and the extra power loop in parallel to the main commutation loop, larger equivalent L and C will be formed, and extra commutation loop is also formed as well. Therefore, higher current/voltage stress can possibly occur for all the three devices in the T-shape phase leg of the three-level converter. This is particularly severe when using high-speed power devices, where significant di/dt and dv/dt are the main excitation source for the resonance tanks.

To alleviate this effect, more efforts should be paid to the PCB layout to minimize the multi-branch power loop, and to some better damping solutions that can damp the resonance without impacting the overlap loss too much.

5.5.4 Summary of the impact of extra C_{oss}

The disclosed C_{oss} not only impacts the switching loss, the device stress in the extra power loop, but also introduces extra distortion on ac PWM voltage and ac current, as analyzed in Section 5.4.2. It is interesting to notice that for loss evaluation, the energy-based equivalent C_{oss} should be adopted when the voltage dependence is considered, whereas for distortion evaluation and compensation, the charger equivalent C_{oss} should be used. And for the device overstress analysis, the instantaneous C_{oss} at the blocking voltage level should be the choice.

5.6 High performance controller for dual-input and dual-output GaN-based charger

5.6.1 Microcontroller selection

To match the control frequency with the high switching frequency, the control computation speed should be fast enough. And since both ac-dc PFC stage and dc-dc stage have to be regulated, the control requirement cannot be easily met by a typical DSP such as TMS320F28335. Two separated controllers might be competent, however, increasing the board weight. Thus, one central controller with high computation performance is desired. FPGA based controller is one option, however, it usually takes more development efforts compared to C language based microcontroller. Besides, it needs external analog to digital converter (ADC) chips to process the sampling signals of the charger system, including three phase voltages and currents, dc-link voltage, dc capacitor voltage, buck voltage and current, and LLC voltage and current.

After reviewing microcontroller units (MCU) from both Texas Instruments (TI) and Analog Device, the TMS320F28377D controller released in 2014 by TI is finally selected. It has two CPU cores and two programmable control law accelerators (CLA), all rated at 200 MHz system clock, as shown in Fig. 5-78. These four engines are capable of providing the equivalent of 800 MIPS.



Fig. 5-78. The computation units inside TMS320F28377D [336].

Besides, since each CPU has a dedicated trigonometric math unit (TMU) and a floating-point unit, the computation speed is further enhanced, especially when adopting the Park transformation in the rectifier control. With an average execution time of five cycles per instruction, the trigonometric calculation speed can be 5X faster. As a result, a torque loop control for the typical motor drive can be completed within 3 μ s. Furthermore, this MCU also has four internal parallel ADCs, capable of sampling 4 analog signals simultaneously and up to 20 signals in total.

5.6.2 Control strategy of two-stage charger system

To simplify the control and seek for higher efficiency for the dc-dc stage, two different control strategies, as shown in Fig. 5-79, are proposed with respect to the dual output modes.

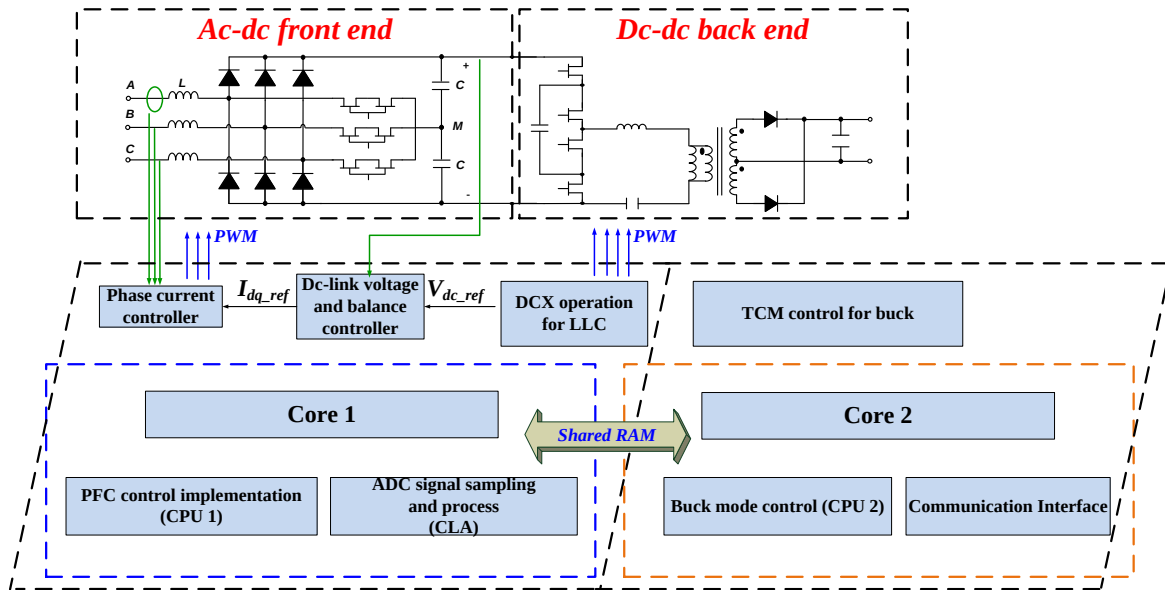


Fig. 5-79. The proposed control architecture for two-stage charger.

In 28 V output mode, LLC converter is activated. Considering the complexities of frequency modulation and synchronization control, and low power efficiency at light load due to higher switching frequency operation in the conventional LLC control, the control strategy is to operate LLC as a dc transformer and vary the dc-link voltage of front-end PFC to regulate LLC output

voltage. Since LLC only operates at its resonant frequency, both ZVS for primary side and ZCS for the secondary side can be always ensured. The control burden of this system is moved from LLC to PFC stage. PFC stage will be responsible for both voltage and current control of the battery load. The proposed scheme is shown in Fig. 5-80.

There are three control loops in the PFC stage. The outer loop regulates the charge voltage or current, the middle loop regulates the intermediate dc-bus voltage, and the inner loop is for phase current control. The control architectures are given in Fig. 5-81 and Fig. 5-82.

To simplify this controller design, the two internal loops can be modeled as a unity gain, as long as the time constant of the outer loop is shorter than that of dc-link voltage control. Thus, the control diagram becomes a proportional system as given in Fig. 5-83, and a simple integral control is sufficient.

$$W_{vdc}(s) \approx \frac{1}{1 + T_{vdc}S} \approx 1 \quad (T_{vdc} \ll T_{CV}) \quad (5-71)$$

$$G_{CV}(s) = \frac{K}{S} \quad (5-72)$$

Similar to the voltage control, the current control can be designed in a similar way. A simulation result for constant current control of battery is demonstrated in Fig. 5-84, showing good dynamics with a current step change.

When the charge operates in 270 V mode, buck converter is activated. Considering the limited variation range of dc-link voltage with 235 Vrms ac input, it is not wise to regulate the dc-link voltage for battery current and voltage control. Instead, buck converter itself is more capable of regulating its output voltage and current in a wide range. Therefore, in this mode, a strategy with fixed dc-link voltage control for front-end PFC and independent control of buck voltage and current is adopted, as illustrated in Fig. 5-85.

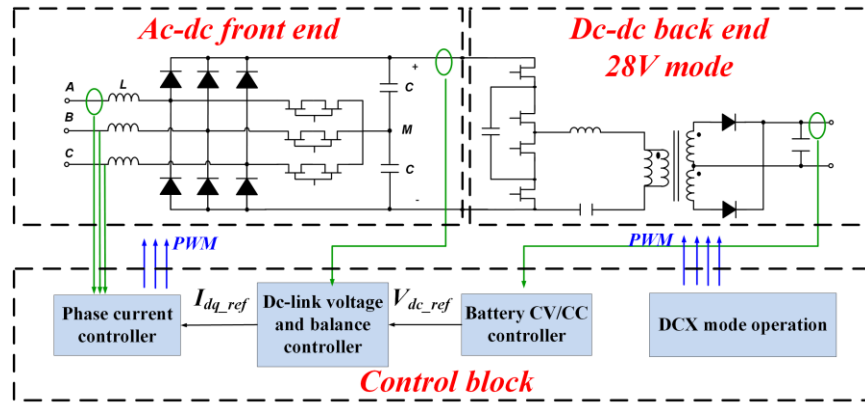


Fig. 5-80. The proposed control architecture for two-stage charger in 28 V mode.

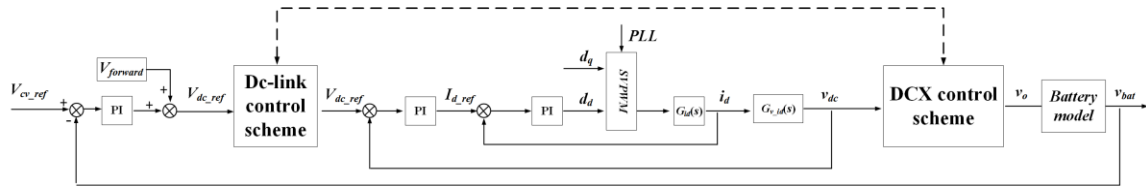


Fig. 5-81. The diagram of constant voltage control for two-stage charger in 28 V mode.

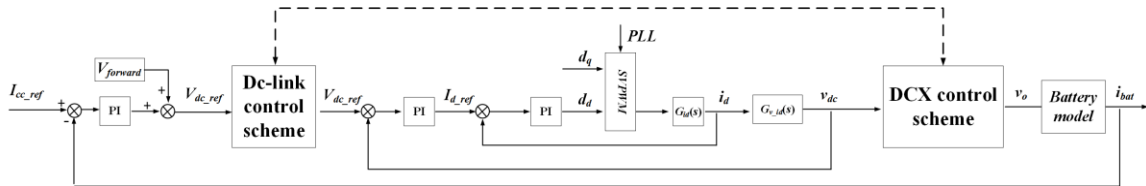


Fig. 5-82. The diagram of constant current control for two-stage charger in 28 V mode.

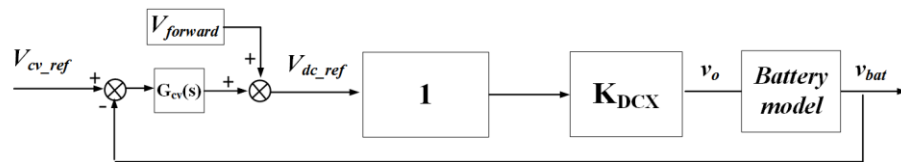


Fig. 5-83. Simplified control diagram of outer loop voltage controller for two-stage charger in 28 V mode.

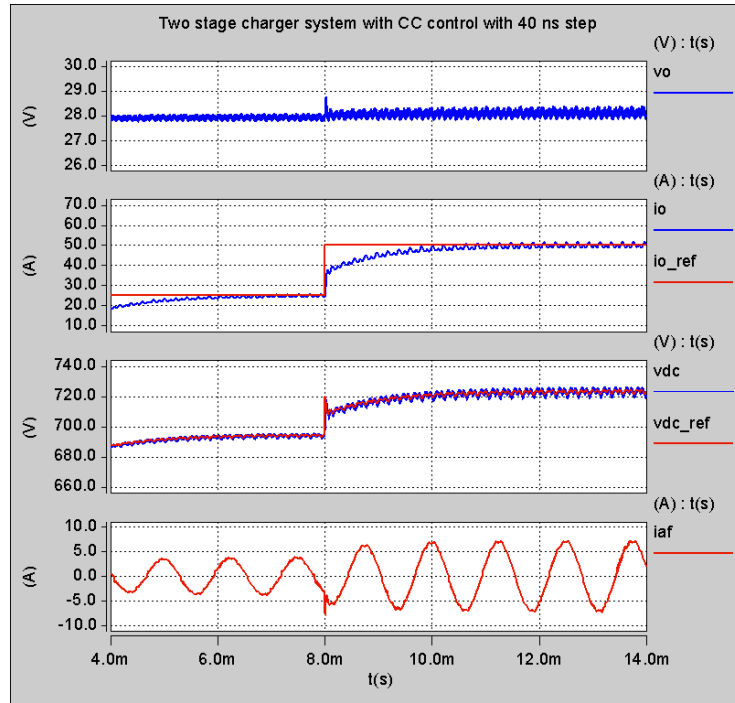


Fig. 5-84. Simulation results of constant current control for two-stage charger in 28 V mode.

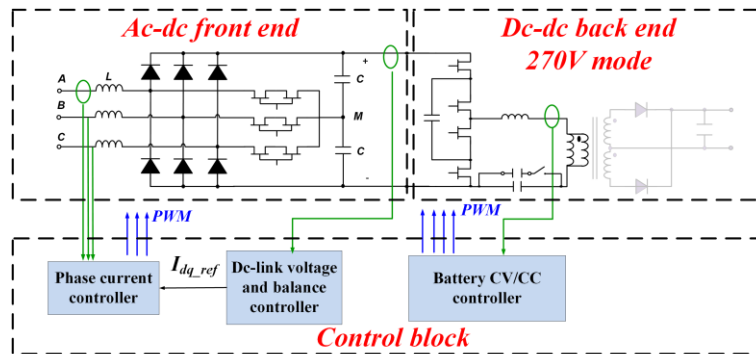


Fig. 5-85. The proposed control architecture for two-stage charger in 270 V mode.

Since Vienna-type rectifier is a non-regenerative converter, a certain of load is necessary for its normal operation. Therefore, during the pre-charge stage, not only the PFC stage will be charged via diodes of the rectifier, the dc-dc stage will be operated in the open loop first. Then, PFC actively ramps the dc-link voltage to the nominal level and buck output voltage is charged to the minimum charging level. Once the charger control is enabled afterward, buck current control will take care of the charging and transitions to voltage control if charger voltage reaches to a level closer to the threshold. During voltage mode, if the charger current is higher than the threshold, it returns to current limiting control. The state machine of the buck mode control is shown in Fig. 5-86.

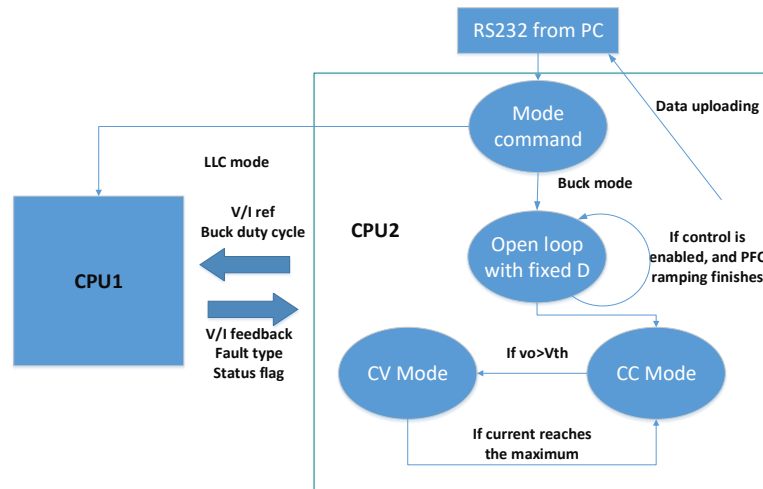


Fig. 5-86. The implementation of control state machine in 270 V mode.

5.6.3 Controller board development

Since the commercial TMS320F28377D controller kit has unnecessary functions on the board, as well as bulky connectors, its board area and weight are not optimized. A custom central controller board is designed, merging the minimum MCU system, interface and condition board together for both ac-dc and dc-dc stages.

Fig. 5-87 shows the function diagram of this central controller board, with power supply, voltage and current sampling circuits, protection circuits, and communication interfaces all in one.

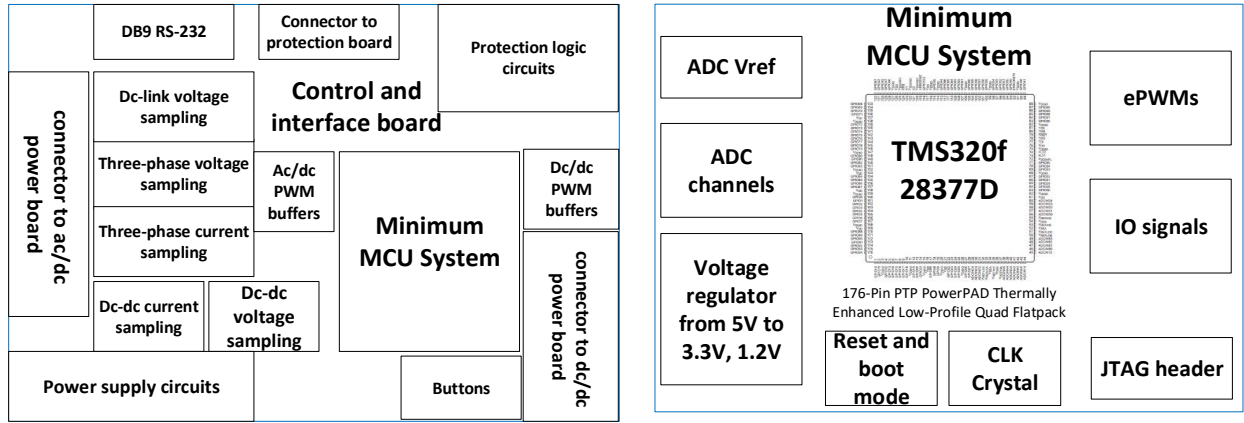


Fig. 5-87. Function blocks of the proposed central controller board.

5.7 Charger implementation and test

In Vienna-type rectifier, the two GaN switches are connected in D-S-S-G manner to form a bidirectional switch. This adds the complexity for switching loop layout. On the other hand, since this first-generation e-GaN device has to be bottom cooled, enough thermal copper area has to be retained to ensure good heat spreading. To reduce the switching loop and balance with thermal design, a vertical design is proposed. In each phase, two switches and two diodes are placed as illustrated in Fig. 5-88, where two dc-coupling capacitors are placed closer to this switching commutation loop. One has to mention that this TO-220 package diode has to be installed vertically, so it does not take the space on the PCB board to reduce the switching loop. Even so, a certain gap between components has to be carefully remained to ensure enough insulation clearance. Then, the gate drive board is vertically placed on the top of the main power board, and directly connected to G-S terminal through a short two-pole connector.

Two cutoff holes are made for rectifier diodes to go through it. Layout efforts have also been made to reduce the board area for this three-phase driver. The gate driver board is shown in Fig. 5-89, and its measured weight with components on board is 21.8 g.

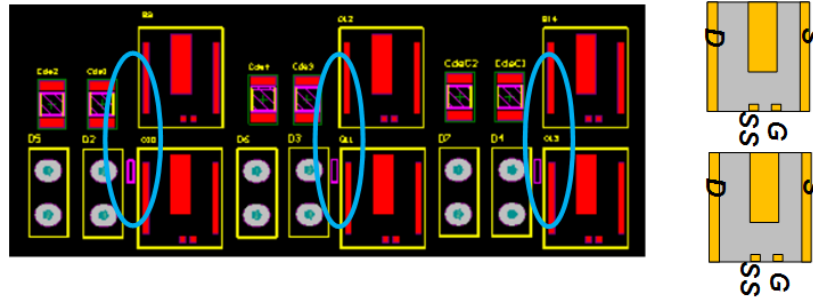


Fig. 5-88. The layout scheme of PFC power switching loop.

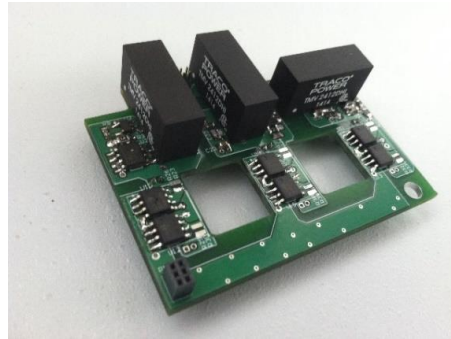


Fig. 5-89. Photo of the three-phase gate driver board of the GaN based PFC stage.

Since GaN device has a bit higher voltage drop when it conducts in the reversed direction, the switching transient mismatch for two serial switches should be reduced to avoid excessive switching type loss. When driving the device, the turn-on deviation for the two switches in one phase leg is found within 10 ns, as given in Fig. 5-90, and turn-off deviation for the two switches in one phase leg is within 6 ns. With such small deviation, their losses are negligible.

5.7.1 Thermal design for two-stage chargers

The selected GaN device has low profile surface mount package, which helps reduce the parasitic inductance but challenge cooling design. Especially, for the bottom cooled package, a dedicated cooling solution has to be applied. For the standard FR4 PCB material, heat from the device junction needs spread out from junction to case and then spread from FR4 PCB layers to thermal interface material (TIM) and heatsink, as shown in Fig. 5-91. Along the series path, many factors will impact the thermal resistance. The dominant one is PCB thermal resistance, which is

significantly determined by PCB manufacture and circuit layout. Its key contributors are listed in Fig. 5-92. To predict this resistance, FEM simulation has been used for of different types of PCB layouts [163].

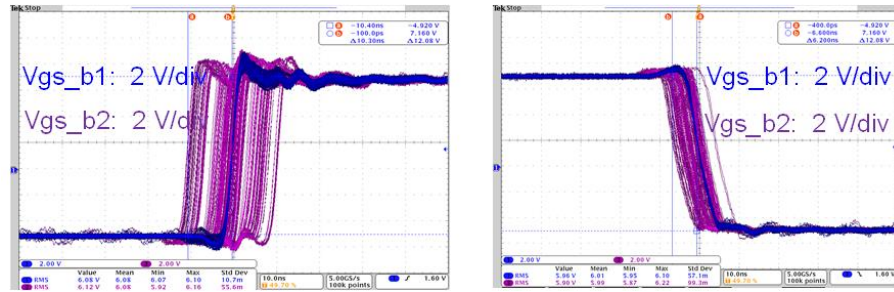


Fig. 5-90. Mismatch of turn-on and turn-off propagation delay between two unified gate drivers.

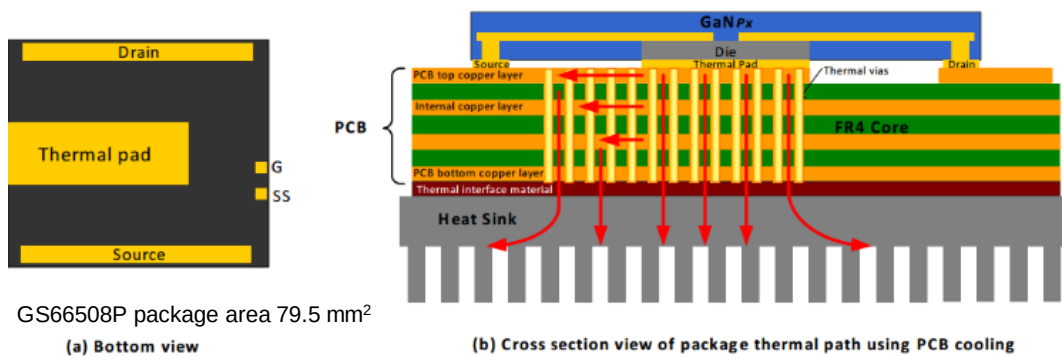


Fig. 5-91. Thermal flow of surface mount GaN Systems devices through PCB [163].

The estimated thermal resistance of TIM is about 0.83 °C/W, and the device junction-case thermal resistance is 0.5 °C/W. The required minimum heatsink thermal resistance is tightly constrained by PCB thermal resistance, as given in (5-74). Depending on the maximum temperature rise requirement, the impacts of the PCB thermal resistance on heatsink resistance can be different. Their relationship is given in Fig. 5-93 with the assumption of 60 W total loss. It shows that with a tight requirement on temperature rise, PCB cooling design has to be optimized so that the stress on heatsink can be alleviated. Thinner PCB with multi-layer design, thicker copper trace, large copper plane, and filled thermal vias are all key measures to achieve this target.

$$R_{th_HS} = \frac{125^{\circ}\text{C} / \text{W} - R_{th_jh} \cdot P_{\max} - 70^{\circ}\text{C} / \text{W}}{P_{\text{total}}} \quad (5-73)$$

$$R_{th_jh} = R_{th_jc} + R_{th_PCB} + R_{th_TIM} \quad (5-74)$$

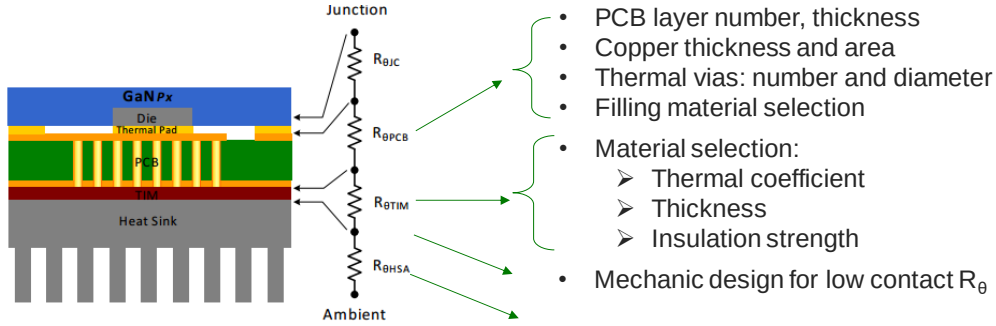


Fig. 5-92. Cooling design concept and main optimization factors for surface mount GaN devices.

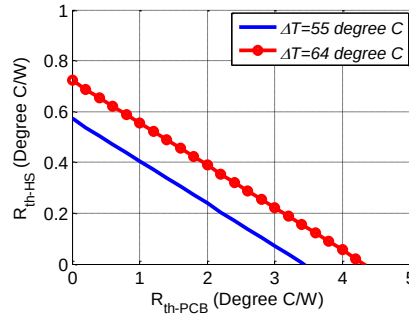


Fig. 5-93. Relationship between minimum heatsink thermal resistance and PCB thermal resistance.

The thermal resistance from the case of the device to heatsink has to be reduced for this type of bottom cooled GaN devices, since the FR4 material is not a good heatsink spreader. Hundreds of thermal vias have been designed around each GaN device, and copper planes across four PCB layers have been provided. In order to further reduce this resistance, this thickness of PCB is reduced from standard 60 mils to 40 mils. And all thermal vias are plated with copper and filled. Four mounting holes have been placed to tightly mount the heatsink beneath the board, where the thermal copper on the bottom layer is open to air and directly contact the heatsink. The commercial heatsinks have been thoroughly searched, and it turns out that an aluminum pin-fin heatsink with

2.05 inches width and length from Coolinnovations shows the lowest thermal resistance with the forced cooling and the lowest weight among several candidates.

Mechanic mounting is also crucial. The vertical placement of rectification diodes is good for switching loop minimization, however, the soldered leads of diodes are difficult to flush with the bottom surface of PCB, especially in the middle of the two diodes, i.e. phase B device area. From the earlier test result under 600 V, this causes uneven thermal stress among three-phases. Phase B device has much higher temperature rise than other phases, e.g. the source pin of phase B bottom device exceeds 100 °C in 30 s, and 20 °C higher than its drain pin, as given in Fig. 5-94. Thermal grease should be added to phase B area to improve the contact between the thermal interface material and heatsink. The improved contact greatly reduces the thermal resistance. From Fig. 5-95, the bottom phase B device temperature drops to 67.3 °C after 14 mins testing.

Forced cooling is applied for both stages. As shown in Fig. 5-96, two dc fans are installed beneath the main power board and heatsinks for two-stage GaN Systems devices, respectively.

And a customized extruded heatsink with high precision thickness is also designed for the four top-cooled EPC device on the secondary side of the LLC resonant converter, as shown in Fig. 5-97, where the unique design is that this heatsink performs cooling for both the device and the high power density planar transformer, and it also functions as a jumper for 28 V mode to conduct 1 MHz full rectified current with 50 A dc mean value between the EPC devices and the LLC output side.



Fig. 5-94. Temperature reading of GaN devices of the PFC stage without good thermal contact. Ch1: top A top source; Ch2: bottom B source; Ch3: top B source; Ch4: bottom B drain.



Fig. 5-95. Temperature reading of GaN devices of the PFC stage with good thermal contact. Ch1: top A top source; Ch2: bottom B source; Ch3: top B source; Ch4: bottom B drain.



Fig. 5-96. Heatsink and fan installation for the two-stage charger.

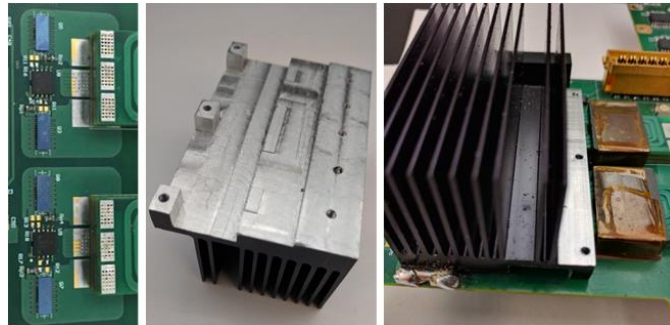


Fig. 5-97. Heatsink and fan installation for the EPC devices on the dc-dc stage.

5.7.2 Two-stage three-phase EMI filter design

5.7.2.1 Power quality and EMI requirement

DO-160 E standard is used for the aviation grid interfaced converter [174]. It requires that the leading power factor (PF) shall be greater than 0.980, and the lagging PF shall be greater than 0.70 for frequencies above 500 Hz, and follow (5.1-1) for frequencies between 360 Hz and 500 Hz,

$$PF = 2.8571e-3 * f - 0.72857 . \quad (5-75)$$

It also specifies current distortion up to 40th order in Table 5-7 specifying the percentage limit for each harmonic component. As for conducted electromagnetic emission, two limits of noise levels are given aiming at different groups of equipment. The stringent level is used for guiding this charger design.

5.7.2.2 EMI filter design

The total noise is decomposed into CM and DM noise. Since DM filter participates in CM path and may also impact the current ripple of the ac-dc converter, while CM flux is canceled in DM path, thus DM filter will be designed in the first place and then inserted into CM filter process. A simulation-based filter design approach is adopted for paper design, as shown in Fig. 5-99. The procedures are also applied to the physical implementation of EMI filters, in which all simulation data are replaced by testing data.

In the early design stage, the actual parasitic impedance of the noise propagation path is unknown since the test set up is not built yet. Therefore, a practical assumption is made for the distribution of parasitic capacitance of the ac-dc converter. It is worth mentioning that the dominant parasitics likely come from the load grounding capacitances if it has a larger size than the converter. Thus, a slight mismatch in device parasitics may not affect the final noise distribution too much.

Table 5-7. Current harmonic limits for balanced three-phase electrical equipment in DO-160 E [174].

Harmonic Order	Limits
3 rd , 5 th , 7 th	$I_3 = I_5 = I_7 = 0.02 I_1$
Odd Triplen Harmonics (h=9, 15, 21, ..., 39)	$I_h = 0.1 I_1/h$
11 th	$I_{11} = 0.1 I_1$
13 th	$I_{13} = 0.08 I_1$
Odd Non Triplen Harmonics 17, 19	$I_{17} = I_{19} = 0.04 I_1$
Odd Non Triplen Harmonics 23, 25	$I_{23} = I_{25} = 0.03 I_1$
Odd Non Triplen Harmonics 29, 31, 35, 37	$I_h = 0.3 I_1/h$
Even Harmonics 2 and 4	$I_h = 0.01 I_1/h$
Even Harmonics > 4 (h=6, 8, 10, ..., 40)	$I_h = 0.0025 I_1$

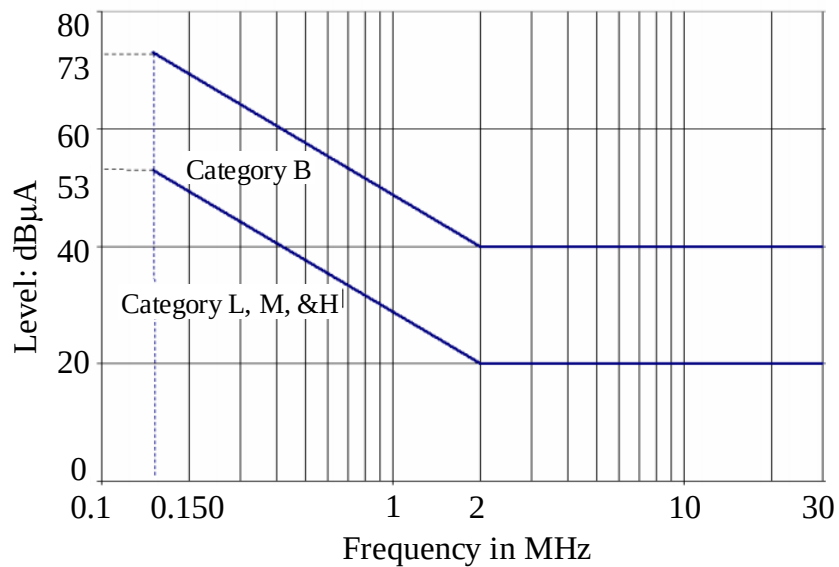


Fig. 5-98. Conducted EMI standard in DO-160E [174].

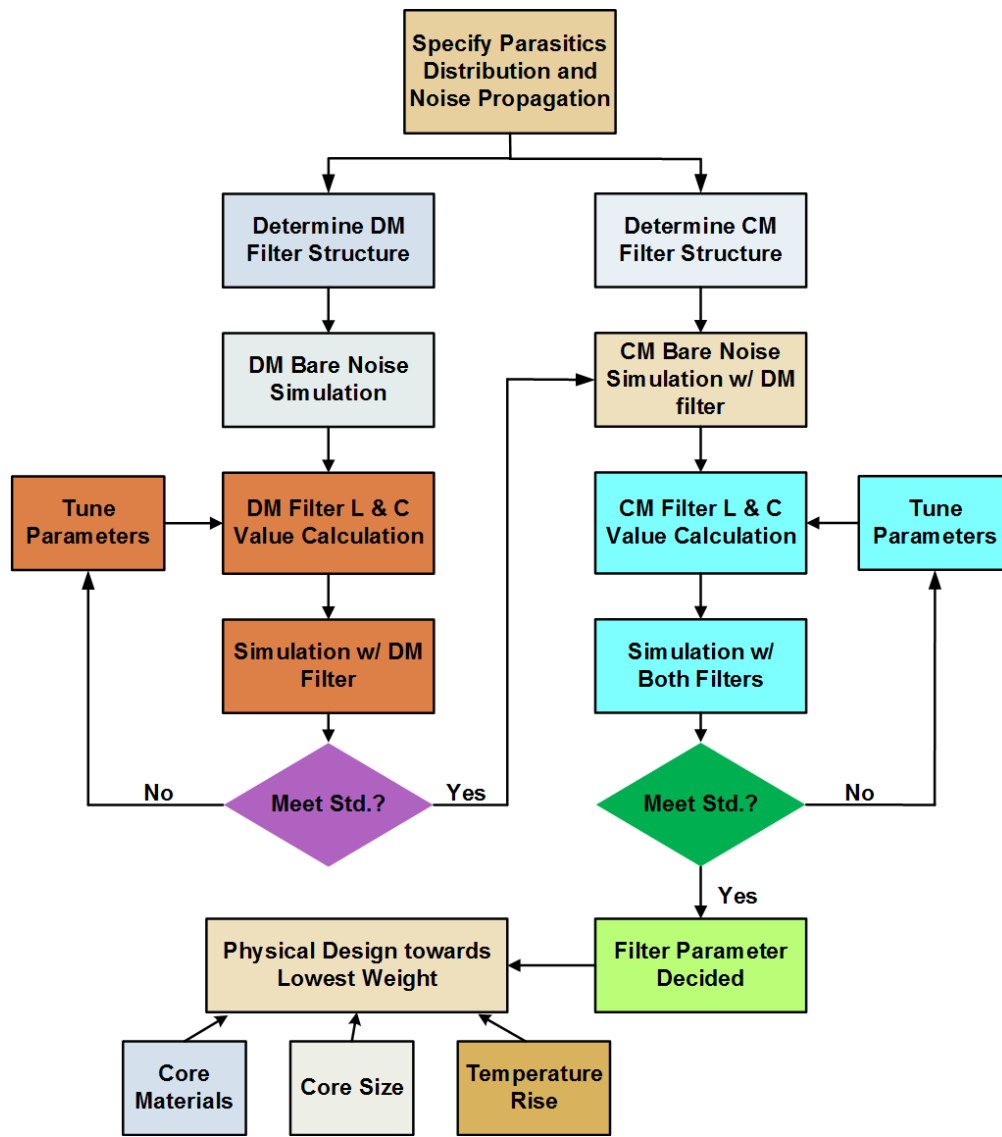


Fig. 5-99. Proposed EMI filter design procedure.

5.7.2.3 Passive filter structure

The typical passive filters are LC filter and CL filter, and they can be further combined to form a CLC filter, a LCL filter, and multi-stage filters.

To determine the suitable filter structure for a given topology, the impedance of the converter as a noise source and LISN as the load should be examined. With maximized impedance mismatching, one can achieve the best EMI filter performance with low implementation efforts.

For Vienna-type PFC, its ac terminal presents a low source impedance in the DM path, and 50 Ω RF load of LISN presents a high impedance, thus LC filter is preferred. Now that the boost inductor is in series with this DM inductor, it can be further integrated into DM filter, as illustrated in Fig. 5-100.

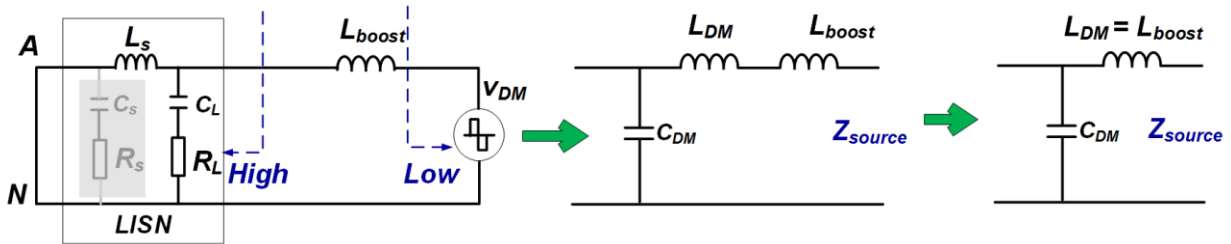


Fig. 5-100. DM filter integration with the input boost inductor.

To achieve extra 40 dB/dec attenuation and low filter size, two-stage LC filter is finally adopted, as shown in Fig. 5-101.

In the literature, LC based CM filter is often used for Vienna-type rectifier. However, since the serial 5 μ H inductor of LISN presents lower impedance in hundreds of kHz along CM path than that of the CM capacitor, a L-L divider is formed instead of a LC filter. This frequency dependent impedance of LISN deteriorates CM impedance mismatching. To maximize the impedance mismatching, a small masking choke has to be added after LC filter to mask the LISN

inductor. In [158], an extra CM capacitor is further added to form another LC filter, achieving 40 dB/dec attenuation at even higher frequency.

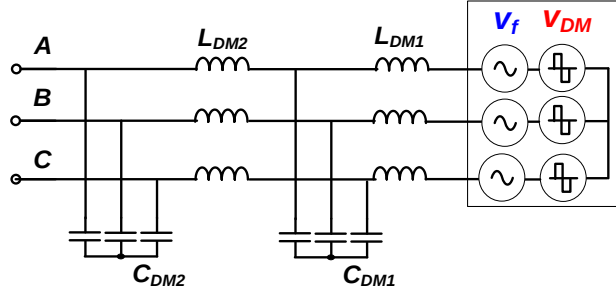


Fig. 5-101. Selected DM filter structure.

Moreover, LC filter might not be a good option when the source impedance of the converter is high. This can be explained by the simplified equivalent CM model based on Thevenin's theorem, as illustrated in Fig. 5-102, where the source impedance of PFC can be simplified as a grounding capacitance. In the case when PFC has low grounding capacitance, a high capacitive impedance will be presented in its noise source. This violates the LC filter assumption that noise source shows low impedance. Therefore, a much larger CM choke has to be added to compensate the capacitive impedance in the medium frequency range, in order to form a LC filter, as shown in Fig. 5-102 and (5-76).

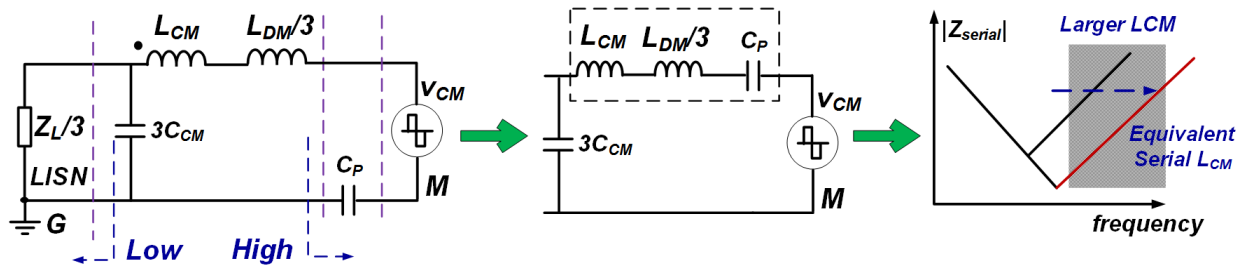


Fig. 5-102. Equivalent CM path with LC type CM filter.

$$Z_{\text{serial}} = sL_{CM} + \frac{sL_{DM}}{3} + \frac{1}{sC_P} \quad (5-76)$$

If transforming the above circuit to Norton equivalent circuit, CM noise source becomes a current type source, as shown in Fig. 5-103. It becomes much clear that LC filter only performs as a C type filter. Instead, a CL filter becomes the right choice for current noise filtering. Not only because it can better utilize the CM filtering capacitor, thus the CM inductance can be reduced, but also because it naturally has a CM choke connected with LISN, thus immune to the low inductive impedance of LISN at low frequency.

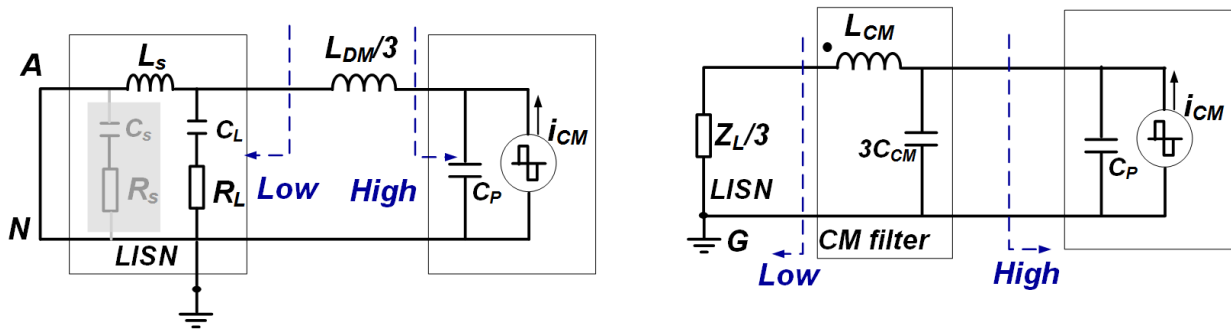


Fig. 5-103. Impact of converter source impedance on CM filter selection.

5.7.2.4 Passive filter paper design

With the selected filter structure, LC parameters can be determined. First, by measuring the bare EMI noise, the required noise attenuations for both DM and CM are obtained. It has to be mentioned, the simulated bare noise and testing results have a little mismatch, where simulated noise is a little lower. This can be explained from the facts that simulated parasitics may be different from the physical parasitics and that the simulation has not modeled the peak detector function inside the spectrum analyzer. Based on the measured bare noise, DM cutoff frequency of the two-stage LC filter is 26 kHz, and CM cutoff frequency of the two-stage CL filter is 65 kHz.

Based on DO-160 E standard, the leading PF shall be greater than 0.980, i.e. 11.4 degrees. The reactive power is limited to around 20% active power. Therefore, the maximum DM capacitance should meet the input power factor requirement. In addition, this project also specifies the total

line-to-neutral capacitance shall be less than 2.5 μF per phase. And the total CM capacitance between any of the input phases and the ground should be no more than 20 nF, restrained by the maximum allowable earth leakage current due to safety concerns.

After capacitances are selected, inductances can be designed following

$$L_{DM} = \frac{1}{C_{DM} (2\pi f_{\text{cutoff_DM}})^2} \quad (5-77)$$

$$L_{CM} = \frac{1}{3C_{CM} (2\pi f_{\text{cutoff_DM}})^2} \quad (5-78)$$

Fig. 5-104 shows the overall filter schematic, which consists of six 0.47 μF DM capacitors, six 3.3 nF CM capacitors, six 75.3 μH DM inductors for both stages, and two 0.576 mH CM chokes. To be noticed, due to coupling and resonance issues, the final filter structure and implementation has introduced a damping choke and a third stage as will be given in Section 6.7.

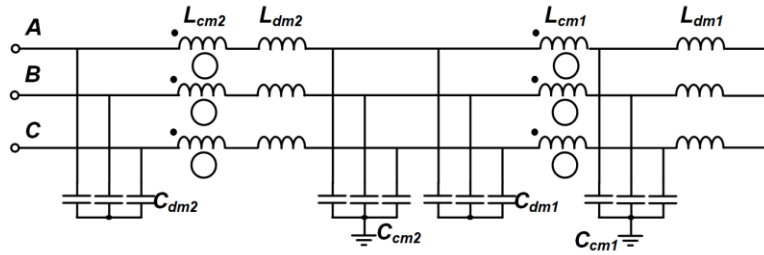


Fig. 5-104. Schematic of the proposed two-stage CM and DM filters.

5.7.2.5 Passive filter physical design

The first-stage DM filter also functions as a boost filter. It conducts all switching harmonics and requires high energy storage. In the paper design EE core with ferrite R material from Magnetics is selected. However, because of the availability issue, RM8 core with ferrite N49 material from TDK is adopted. N49 has low core loss at high frequency above 500 kHz, similar to the performance of R material and Ferroxcube 3F35. A photo of a three-phase filter is provided in

Fig. 5-105. The measured inductance is 79 μH close to the target value and its self-resonance frequency is above 6 MHz based on Fig. 5-106.

As available commercial nanocrystalline cores are only heavy cut cores, the second-stage DM inductor L_{DM2} is also redesigned. Since L_{DM2} sees much lower noise current, thus suffers mainly copper loss, a High-Flux power core from Micrometal is chosen. With a distributed air gap, high flux density, and slower permeability roll-off at high frequency, powder toroidal core is suitable for DM filters. Since the effective per turn inductance AL decreases as dc bias increases, as shown in Fig. 5-107, one has to consider the dc operation point. As a feature of ac DM inductor, its fundamental ac current swings in a line cycle, acting as a moving quasi-dc operation point for the high frequency noise. This complicates the selection of dc bias. In this baseline filter design, the peak of the fundamental current is used for simplicity. The relationship between AL and the target inductance is then determined as (5-79) and plotted in the red curve. The intersection of two curves determines the target AL and number of turns.

$$AL = L_{DM2} I^2 \frac{1}{(NI)^2} \quad (5-79)$$

The small-signal measurement of the three DM inductors shows 140 μH inductance at 450 kHz. Compared to 75 μH inductance at line peak current, a big swing exists due to the moving dc bias. A better winding scheme is proposed to reduce the parallel capacitance in Section 6.6.1.

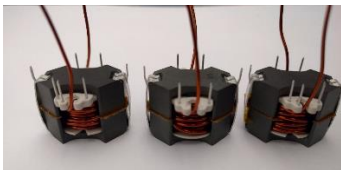


Fig. 5-105. Three first-stage DM inductors.

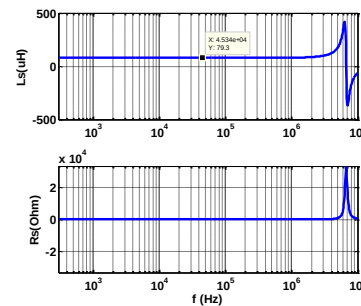


Fig. 5-106. Measured impedance of the first-stage DM inductor.

Two CM chokes are designed using Nanocrystalline core VITROPERM 500F, with type number W838. Three phase windings are designed and are placed evenly along the toroidal core.

The physical implementation is shown in Fig. 5-108. On this 1st version, 6 film capacitors were used for DM filter. Because of magnetic and capacitive coupling issues in the three-phase filter as to be analyzed in Chapter 6, the 2nd version replaces all film capacitors to ceramic types, and all the neutral lines are re-arranged to form minimum loops. In addition, capacitive shielding and damping are also added in the final version. Details are presented in Chapter 6.

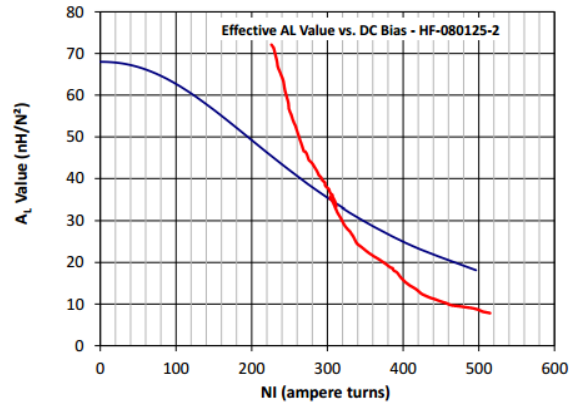


Fig. 5-107. Determination of turns number and per-turn inductance for the second-stage DM inductor.

5.7.2.6 Grounding scheme

To reduce the coupling, the whole grounding scheme is carefully devised from the original single point grounding to multi-point grounding. Since Ccm1 bypasses most of the EMI noise current, to connect the first stage Y capacitor with enclosure provides a shorter return path for noise back to the converter instead of going through the ground plane. And directly connecting the second stage filter ground to the LISN earth plane, can also avoid any noise voltage coupled from the sharing path with the much noisy first-stage grounding path.

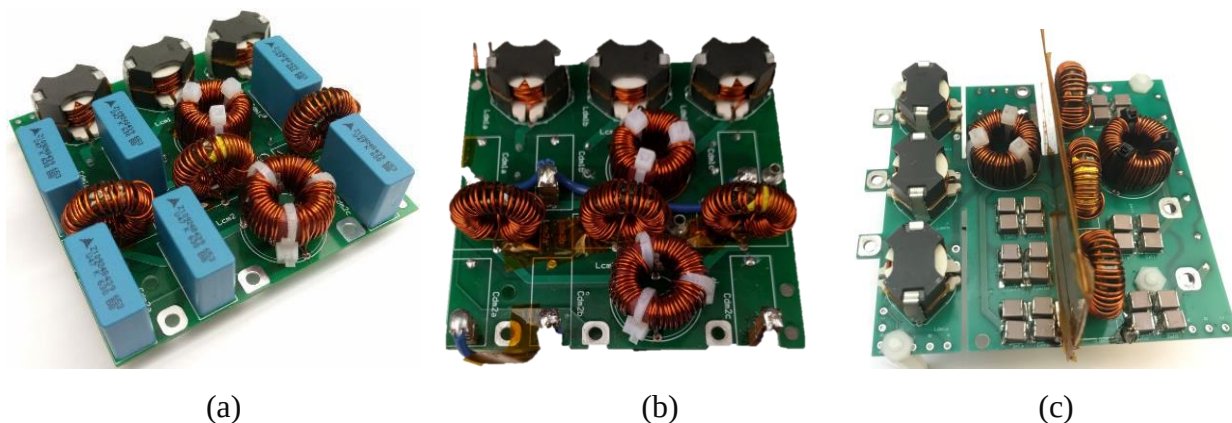


Fig. 5-108. Prototype of the EMI filter. (a) first version, (b) 2nd version, (c) final version.

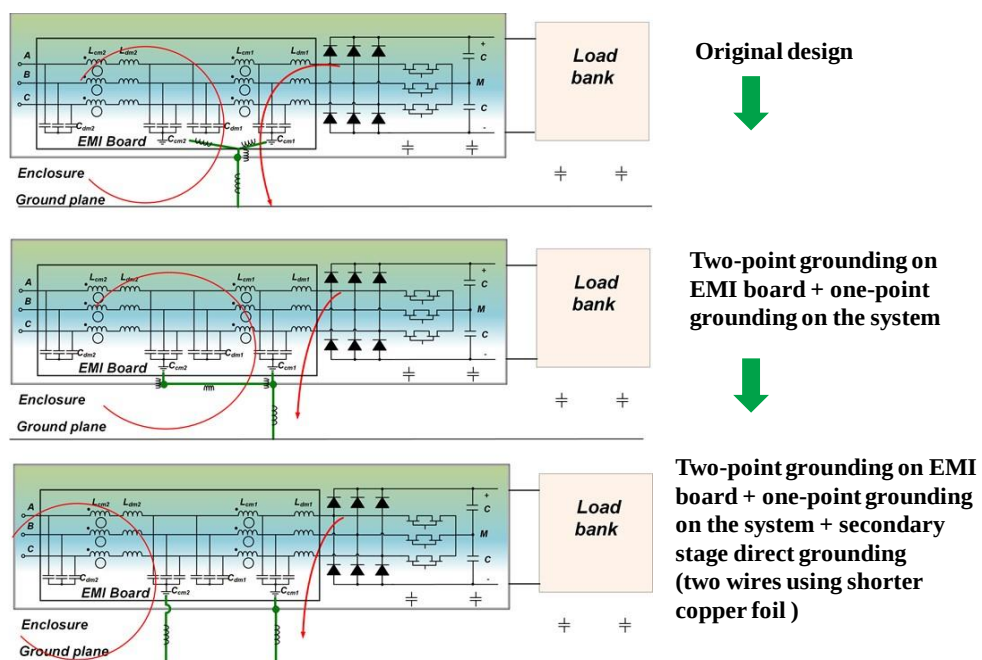


Fig. 5-109. Grounding scheme evolution.

5.7.3 Dual-mode test of GaN-based universal battery charger

5.7.3.1 Enclosure and prototype

An aluminum enclosure is designed to hold the charger and provide the inlets and outlets for air flow. As shown in Fig. 5-110 and Fig. 5-111, two fans under the bottom are used to cool the 650V ac-dc GaN devices and dc-dc GaN devices, and a fan installed on the right side is for cooling the EPC device. Six outlets are designed for piping the hot air out of the case. The air flow is constrained on the left and top side of the box to prevent the local air loop around inlets. Cord grips are adopted to fasten the power wires. A plastic screen is for displaying LED fault indicators.

The photos of the final design are shown in Fig. 5-112 and Fig. 5-113. Inside the box, converters are mounted onto the bottom case with plastic stand-offs. On top of the lid, four control buttons are mounted.

5.7.3.2 270 V mode test

Both the 115 Vac and 235 Vac input conditions have been tested to full power in this 270 V mode. Fig. 5-114 shows the ac-dc PFC stage waveforms at 115 Vac, 625 Vdc, and full Load. Fig. 5-115 gives the results under 235 Vac conditions. It is found that at low line voltage case, current THD is lower, around 3~4%, while at the high line case, current THD is higher, due to residual sampling distortion, load-dependent voltage distortion of the programmable ac power source, and lower current rating. Further improvement could be possible.

To maintain a high-quality interface with the aviation grid, power factor should be high. The measured PF at different operation conditions is listed as follows. It is 99.74% at 115 Vac, 800 Hz and even higher at 115 Vac, 360 Hz. Due to higher reactive power from DM capacitors at higher line frequency, power factor has the lowest value of 95.02% at 235Vac, 800 Hz and medium value 98.47% at 235Vac, 360 Hz.

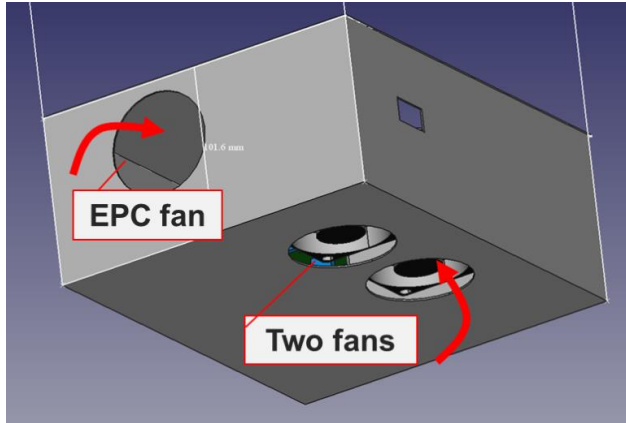


Fig. 5-110. 3D design showing the locations of fans.

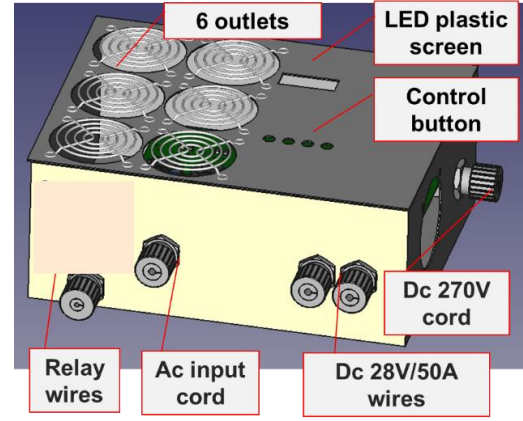


Fig. 5-111. Interface design for the enclosure.



Fig. 5-112. Enclosure photo from outside view.



Fig. 5-113. Enclosure photo from inside view.

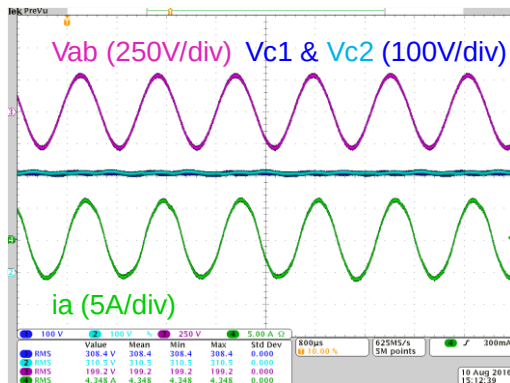


Fig. 5-114. Active front end waveforms at 115 Vac, 625 Vdc, 270 V buck mode, and full load.

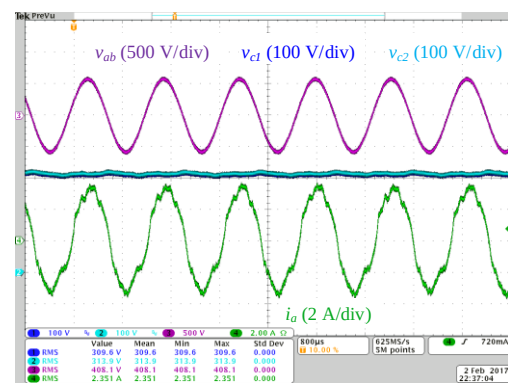


Fig. 5-115. Active front end waveforms at 235 Vac, 625 Vdc, 270 V buck mode, and full load.

The constant current control and constant voltage control have been implemented in this charger system. Fig. 5-116 demonstrates the basic operation after ac diode rectification is completed. First, the dc-link voltage is regulated by PFC to ramp to a certain dc-link voltage, so that the charger output voltage reaches the minimum level. Then, buck converter switches from the open loop control to the closed current loop control, and then transitions to the final voltage control. Fig. 5-117 shows the ac-dc waveforms at the 235 Vac input buck mode. The start-up procedure for Vienna front end and three-buck flying capacitor-based buck is verified.

5.7.3.3 28 V mode test

Similar to 270 V mode, CC and CV control are implemented in 28 V mode operation. The difference is that instead of regulating current and voltage by LLC, now PFC controls the charger output by varying the intermediate dc-link voltage. This scheme simplifies the LLC control.

In this voltage mode, the charge has been tested under 360 Hz/800Hz, 115/235 Vac, 625/650/670 Vdc, and different load conditions. Selected testing results are provided in Fig. 5-119, Fig. 5-120, Fig. 5-121, and Fig. 5-122, showing the waveforms of LLC stage under 115 Vac, 650V_{dc}, and 0.667 Ω load condition.

Fig. 5-123 shows the LLC resonant current and dc output current under 670Vdc, 235Vac, 0.55 OHM external load, 27 V condition, around 47 A output charging current.

5.7.3.4 Power efficiency and thermal test

The thermal stress of the GaN devices is evaluated. The highest surface temperature of 650 V GaN devices in the active front end is up to 60 °C as given in Fig. 5-124 and is up to 45 °C in dc-dc buck stage and is 55 °C in dc-dc LLC mode, all at full voltage and full load. Because of the measurement error of the meters and the junction resistance of device junction-to-case, a rough 10 °C increment can be assumed to estimate the device junction temperature.

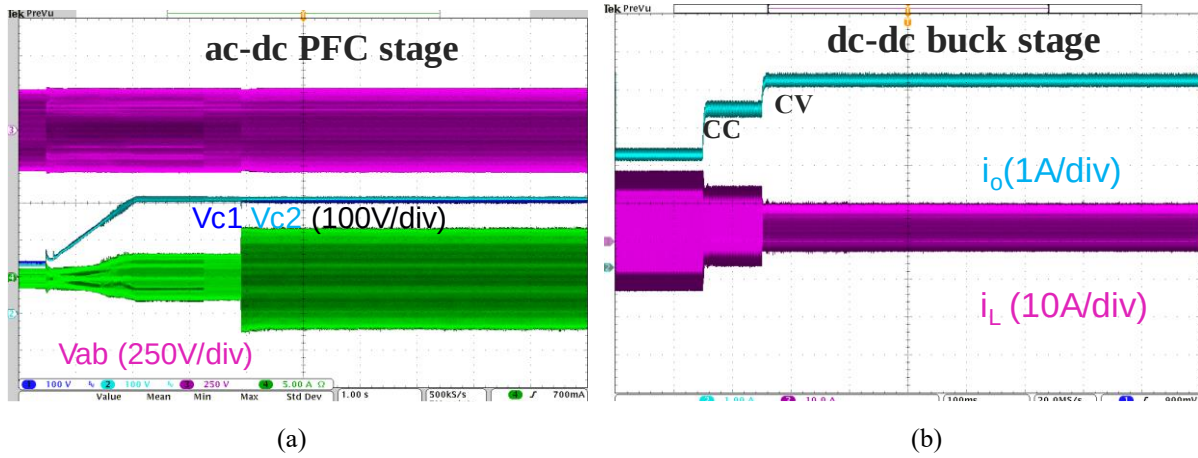


Fig. 5-116. Waveforms at 115 Vac input, buck mode. (a) ac-dc stage. (b) transition of buck constant current and constant voltage charging control.

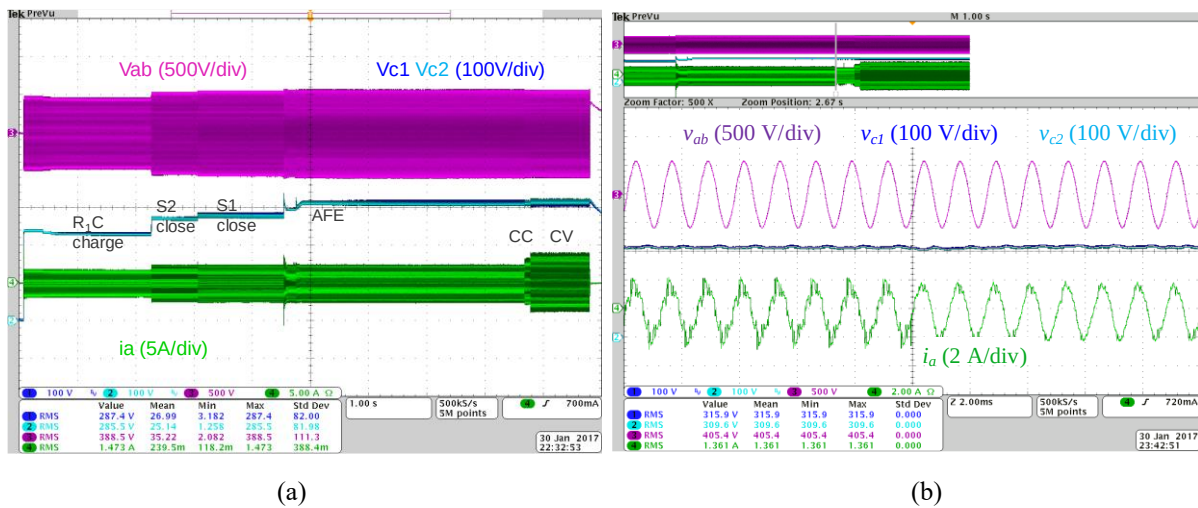


Fig. 5-117. Ac-dc stage waveforms at 235 Vac input, buck mode. (a) start up and transition of buck current and voltage control. (b) dynamic compensation of PWM voltage distortion.

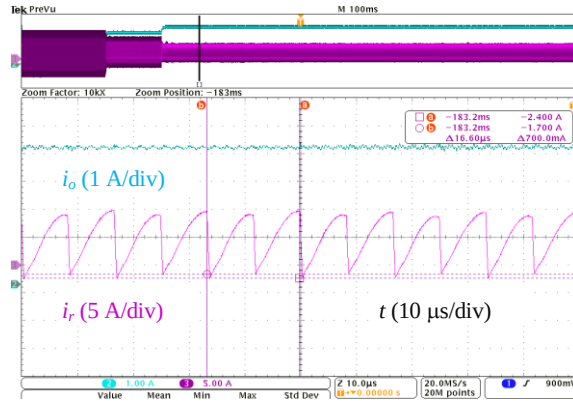


Fig. 5-118. Load current and inductor current waveforms of TCM controlled buck stage.

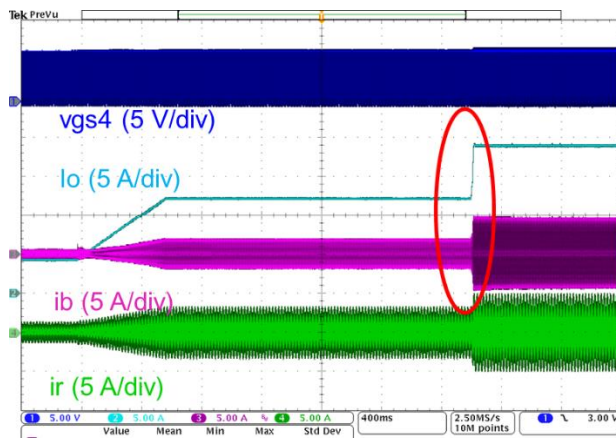


Fig. 5-119. Start-up and transition of LLC current and voltage control.

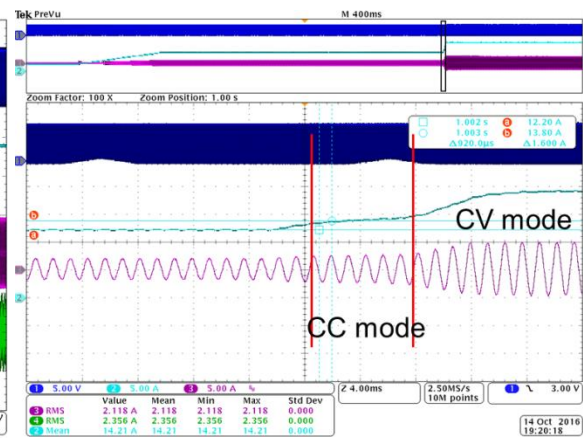


Fig. 5-120. Zoomed-in transition of LLC control.

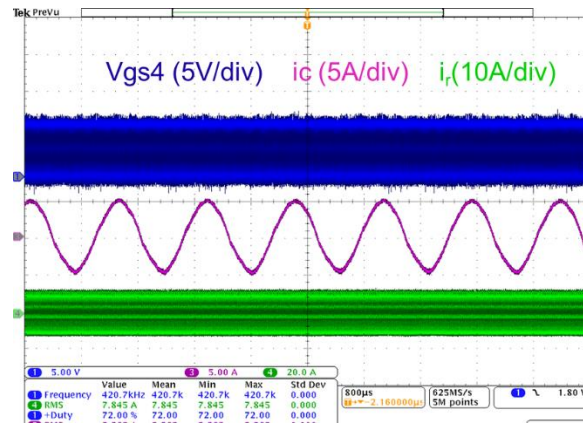


Fig. 5-121. Steady-state waveforms of LLC stage.

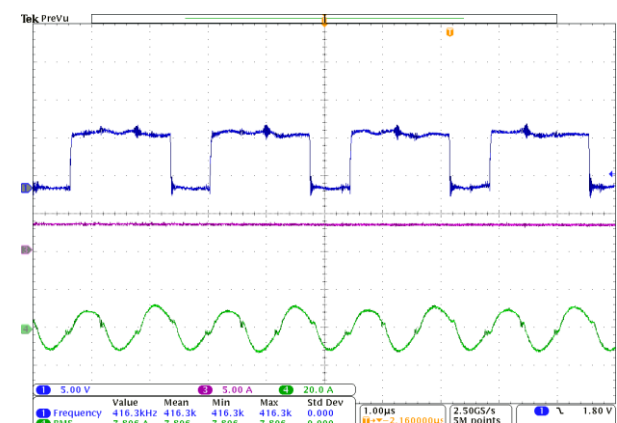


Fig. 5-122. Zoomed-in waveforms of LLC stage.

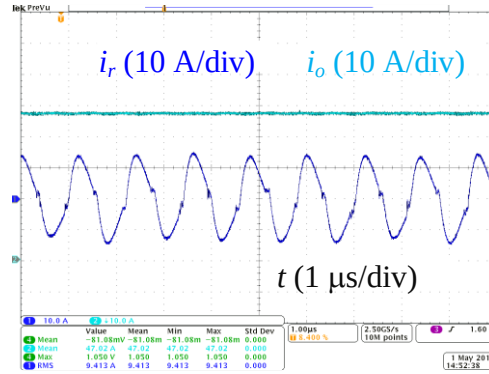


Fig. 5-123. Current waveforms of 670Vdc, 235Vac, 0.55 OHM external dc load, 27 Vo.

The secondary side EPC GaN devices in LLC mode see higher temperature, mainly due to thermal coupling from nearby 50 A mean current, 1 MHz planar transformers via PCB traces. With several thermal design iterations as discussed in Section 5.7.1, PCB surface temperature near the device is finally around 44 °C at the nominal 625 Vdc in Fig. 5-125 (a) and 54 °C at the maximum 670 Vdc in Fig. 5-125 (b), where LLC operates a dc transformer (DCX) with a fixed gain of around 24. However, due to the contact resistance, winding resistance, PCB resistance, and the device R_{dson} , the output impedance of the converter increases, leading to a slightly higher voltage drop under heavy load conditions, thus requiring even higher bus voltage to achieve 28 V regulation. Further improvement could be done through transformer turn-ratio redesign considering these effects or through variable frequency modulation of LLC instead of DCX mode. However, the latter increases the control complexity and switching loss at MHz operation.

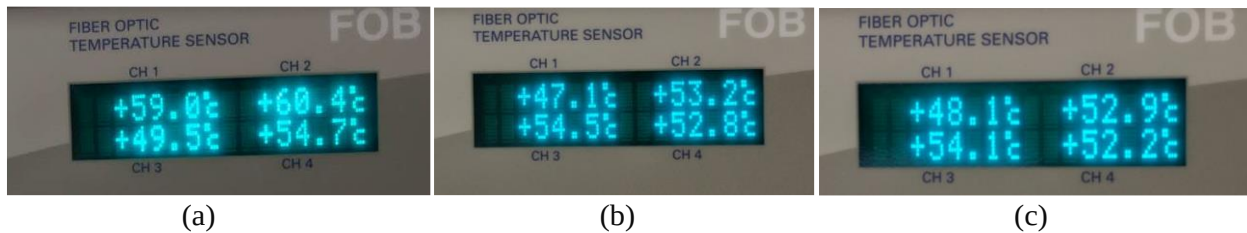


Fig. 5-124. Device temperature readings from a fiber-optic thermal meter for PFC stage at full load. (a) 115 Vac, 800 Hz, 625Vdc, 270 Vo. (b) 235 Vac, 800 Hz, 625Vdc, 300 Vo. (c) 235 Vac, 360 Hz, 625Vdc, 300 Vo. (Ch1: top A top source; Ch2: bottom B source; Ch3: bottom B drain; Ch4: bottom C source.)

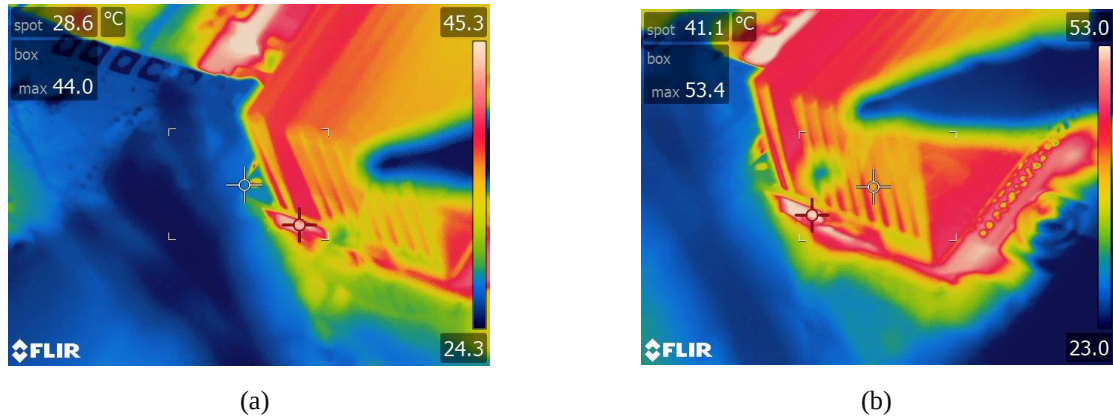
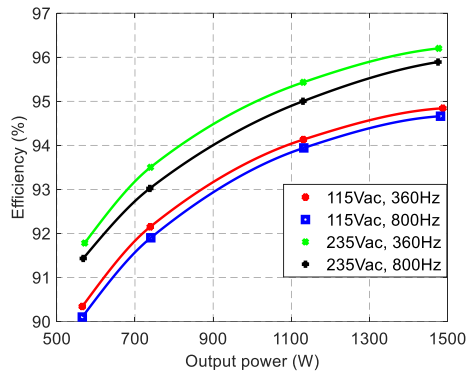


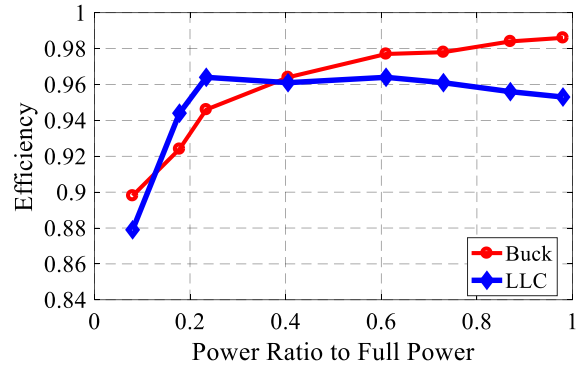
Fig. 5-125. EPC thermal image. (a) @625 Vdc, 235 Vac, 0.55 Ω . (b) @670 Vdc, 235 Vac, 0.55 Ω .

The power efficiency of the ac-dc stage is also tested at two different switching frequencies, under 800 Hz, 115 Vac input, 650 V output, and full loading condition. Its efficiency is 95.3% @450 kHz full load, and 97.9% @112.5 kHz full load. The loss difference shows that switching loss occupies the dominant portion of the total loss. Further tests at 625 V nominal voltage is shown in Fig. 5-126 (a). Dc-dc efficiency at different loads and two operation voltage modes are also shown in Fig. 5-126, where the efficiencies under light loads are measured under lower input voltage. Finally, an average-model based variable switching frequency TCM control is also proposed for the buck converter, which further improves the power efficiency.

The two-stage efficiency is measured in buck mode, as given in Fig. 5-127. The highest efficiency is 95.68 % at full load, 235Vac 360 Hz input, and 300 V output, where buck has about 99% efficiency and PFC has about 96%. It shows that light load efficiency in high output voltage case is higher than that in low output voltage case, partially because of higher duty cycle at the high output voltage and partially due to the lower switching frequency with the higher duty cycle based on the proposed variable frequency TCM control.

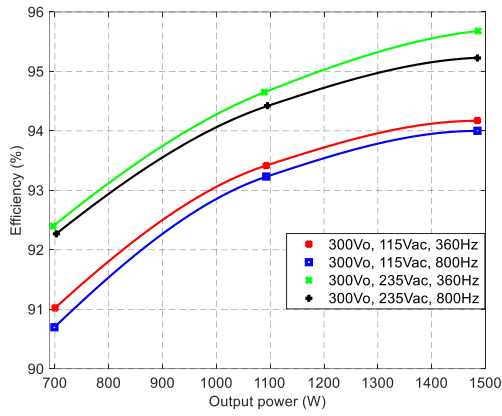


(a)

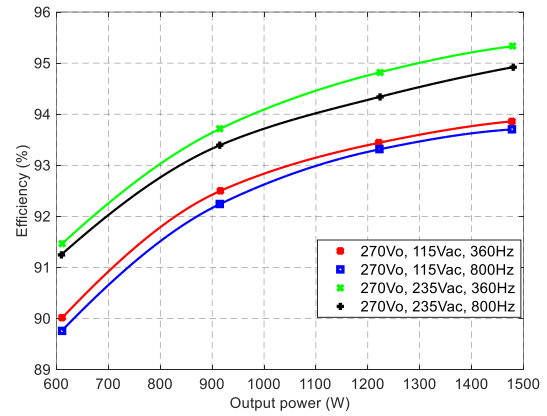


(b)

Fig. 5-126. Efficiency tests of the two-stage charger. (a) ac-dc stage. (b) dc-dc stage.



(a) 300 V output



(b) 270 V output

Fig. 5-127. Efficiency of the whole charger at different combination of input voltage and line frequency.

5.8 Summary

In high frequency high power density PFC design, current quality control is found to be challenging, due to the impacts from sampling and control delay, high dv/dt and di/dt noise, and converter parasitics. Different distortions when adopting GaN devices in this application are observed and their mechanisms are investigated and experimentally verified through sensing and sampling. Three types of sensing distortions are found strongly impacted by di/dt , dv/dt and switching frequency.

Current sensor distortion and differential voltage sensing distortion due to RFI rectification effect is identified, and the cause of that is found to be related to high di/dt inductive coupling from power loop and is mitigated by optimizing and reducing the loop area of critical signals. Isolated voltage sensing offset is found induced by limited CMTI of isolation amplifier, whose mechanism is presented. The offset is eliminated by using a current sensing isolated amplifier with much higher CMTI as a preliminary solution. However, the disclosed issue pinpoints the urgent need of industrial high CMTI voltage sensing isolation amplifiers, in order to properly using GaN devices in high frequency high speed power converters.

At high frequencies, sampling timing together with the high frequency noises shows sensitive impacts on current quality control. Traditional sampling method and moderate ADC may capture switching noises due to the comparable switching duration. An improved current sampling method aiming for three-phase converters is proposed to ensure sample in the long duty cycle interval for three-phases with the least possible switching noise, so that average currents can be sampled with least possible switching noise. This helps improve interface current quality, resulting in overall THD reduction by 4 percentage points.

Turn-off delay at low current regions is more obvious in high frequency high dc voltage converter due to the charging of device junction capacitors during device turn-off, which causes significant voltage loss and current distortion with $6k\pm 1$ order harmonics. A distortion model is proposed and used as the compensation scheme, which shows effectiveness in suppressing these harmonics, reducing current THD from 10% to 3 %.

An overlooked switching commutation loop and C_{oss} is found in three-level converters from the inactive device whose voltage potential difference is statically switching per half line cycle. Additional switching loss is induced and is dominant by C_{oss} loss in GaN converters instead of the overlap loss, owing to GaN's high switching speed. A loss prediction method is proposed so that the traditional DPT can still be used to evaluate the loss in three-level converters. The found switching loop also introduces more overcurrent and overvoltage stress for the switching devices. And it in further leads to more turn-off PWM distortion as discussed above.

Thermal improvements on PCB layout and heatsink mounting are crucial for reducing the thermal stress of bottom cooled GaN devices and weight reduction of the heatsink.

HF and high speed enhance EMI source noise at HF range. At the same time, self-parasitics and coupling can take effects at medium and HF range where switching frequency enters, degrading filter performance. These issues challenge the EMI filter design in high frequency high density converter, distortion the interface quality with grid or any power source.

A GaN-based two-stage dual-input and dual-output battery charger with an all-in-one high-performance controller is finally built and tested based on the accumulated knowledge and approaches from the research work above, accomplishing multi-functions, high density, and decent performance.

6 Parasitic Coupling Effects in EMI Filter and Passive Mitigation

In this chapter, the parasitic coupling effects including both inductive coupling and capacitive coupling are systematically studied. The significant impact of capacitive coupling in T-shape structure and its mechanism are firstly investigated and disclosed for both CM and DM filters. Combination of both effects, a general coupling theory is presented. The classic impedance mismatching theory that focuses on the main low frequency impedance characteristics of passive filter components is further extended to high frequency range considering the coupling effects, which provides an effective guideline for filter topology selection. In addition, a measurement-based frequency domain modeling approach is proposed which not only can characterize the filter transfer gain performance in 50 OHM system but also can predict the insertion loss in an actual power converter system. Then, several coupling mitigation methods are also proposed to alleviate the effect and improve the filter attenuation.

The self-parasitics of inductors also play an important role in filter performance, the parasitic capacitance of windings and cores are analytically modeled and calculated in this work, forming a generic approach. A better winding method is also proposed and experimentally verified, effectively reducing parasitics and improving filter density.

6.1 Mutual capacitive coupling

6.1.1 Capacitive coupling in LCL T-shape structure

LCL T-shape filters are often used as grid-tied power filters and used as EMI filters if interfaced with a low impedance voltage source and low impedance load based on impedance mismatching theory. Moreover, T-shape is also one of the basic unit structures in CLCL and LCLC type filters, similarly as CLC filter. Therefore, the study of this filter structure can reveal the inherent characteristics of other filter structures that share the basic unit.

In the conventional equivalent circuit analysis, only the self-parasitics of two inductor L_1 and L_2 and bypass capacitor C are considered. Other parasitic couplings from signal traces and loops are often ignored in this structure due to the high impedance at both input and output ends.

However, from the small-signal transfer gain test results as will be described later, the filter performance is much degraded compared to its ideal performance with only self-parasitics included. In this chapter, through the analysis and testing, the cause is found to be mutual capacitance coupling from the input of L_1 to the output of L_2 possibly formed by the signal traces, PCB material, and space distance. And it will illustrate how a small mutual capacitance can have a significant impact on the T-shape filter.

Fig. 6-1 (a) shows the equivalent circuit considering this mutual capacitance C_p . Two inductor impedances are defined as Z_1 and Z_2 . The transfer gain of the T-shape filter can be derived from the ratio of the output voltage over the input excitation. As clearly seen, this circuit has a delta connection from Z_1 , Z_2 to C_p . Using the Δ -Y transformation, a new equivalent circuit can be derived in Fig. 6-1 (b).

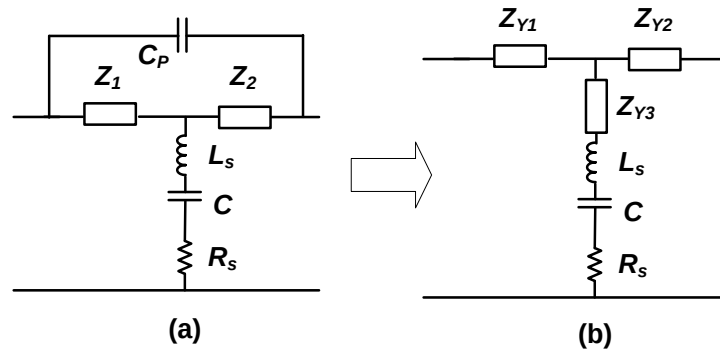


Fig. 6-1. Mechanism of capacitance coupling in T-shape filter.

The three Y-connected impedances are

$$\begin{cases} Z_{Y1} = \frac{Z_1 Z_{C_p}}{Z_1 + Z_2 + Z_{C_p}} = \frac{Z_1 Z_{C_p}}{Z_\Sigma} \\ Z_{Y2} = \frac{Z_2 Z_{C_p}}{Z_\Sigma} \\ Z_{Y3} = \frac{Z_1 Z_2}{Z_\Sigma} \end{cases} \quad (6-1)$$

Since C_p is assumed no more than several pF, $Z_{C_p} \gg Z_1$, $Z_{C_p} \gg Z_2$ at low and medium frequency, e.g., below 10 MHz. Equation (6-1) can be approximated as

$$\begin{cases} Z_{Y1} = \frac{Z_1 Z_{C_p}}{Z_\Sigma} \approx Z_1 \\ Z_{Y2} = \frac{Z_2 Z_{C_p}}{Z_\Sigma} \approx Z_2 \\ Z_{Y3} = \frac{Z_1 Z_2}{Z_\Sigma} \approx \frac{Z_1 Z_2}{Z_{C_p}} = sC_p Z_1 Z_2 \end{cases} \quad (6-2)$$

Therefore, through this transformation, the major change is an inserted impedance Z_{Y3} in series with capacitor branch. As it indicates intuitively, Z_{Y3} acts as if an inductance, thus contributes to the equivalent series inductance (ESL) of the capacitor branch, potentially degrading this bypass branch performance. Furthermore, as it will be analyzed for both CM and DM filters, this series impedance as a product of Z_1 , Z_2 , and C_p is not a linear ESL, it is strongly frequency dependent and has remarkable differences between CM and DM cases, depending on the impedance characteristics and magnitude of the two inductors L_1 and L_2 . And especially in the CM filter case, this impact becomes more significant, due to the high impedance of CM choke at low frequency.

In addition, this effect and the following analysis hold for DC EMI filter, single-phase, and three-phase EMI filter. For a balanced three-phase filter, the analysis can be projected to a single-phase structure, i.e. paralleled three-phase equivalence in CM mode, and phase-neutral equivalence or paralleled three-phase equivalence or line-line equivalence in DM mode.

Note that although this effect is illustrated in a one-line diagram with an unbalanced structure, it is easy to demonstrate the similar effect in a balanced structure. For three-phase, symmetric filters, both CM and DM filter structure by default are balanced. Whereas, for single-phase DM filter, there could be balanced or unbalanced options. However, to avoid the mix-mode noise transformation between CM and DM, it is better to use balanced structure.

6.1.1.1 Impact evaluation of capacitive coupling through three basic approaches

To evaluate the impact of this capacitive coupling, i.e. the impact on the output noise of the EMI filter, three basic approaches are presented in this work.

The first approach is from the topology perspective. As already shown in the above analysis, the equivalent circuit can be deduced from Δ -Y transformation, which has a similar impedance as the original circuit in the forward path, assuming a very small coupling capacitance. The difference is an additional Z_{Y3} in the shunt path. The impact on the filter output voltage can thus be derived from the topology change, based on Fig. 6-2.

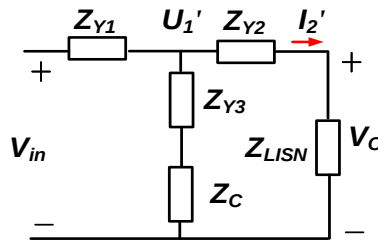


Fig. 6-2. Equivalent circuit of capacitance coupling in T-shape filter.

The original current noise at filter output is

$$I_o = \frac{U_1}{Z_2 + Z_{LISN}} \quad (6-3)$$

The new noise becomes

$$I_o' = \frac{U_1'}{Z_{Y2} + Z_{LISN}} \approx \frac{U_1'}{Z_2 + Z_{LISN}} \quad (6-4)$$

The noise ratio can be defined as filter degradation factor λ

$$\lambda = \frac{I_o'}{I_o} = \frac{U_1'}{U_1} \quad (6-5)$$

Since $Z_{Cp} \gg Z_1, Z_{Cp} \gg Z_2$, therefore the shunt path impedance is smaller than the output branch, as shown in (6-5). Therefore, the joint-node voltage U_1 and U_1' are mainly determined by the shunt path impedance above 100s of kHz.

$$\begin{cases} Z_{Y3} \approx Z_1 Z_2 / Z_{Cp} \ll Z_2 \\ Z_c \ll Z_{LISN} \\ Z_{Y3} + Z_C \ll Z_2 + Z_{LISN} \end{cases} \quad (6-6)$$

In further, λ can be deduced as

$$\lambda = \frac{I_o'}{I_o} = \frac{U_1'}{U_1} \approx \frac{Z_{Y3} + Z_C}{Z_C} \approx \frac{Z_{Y3}}{Z_C} = Z_1 Z_2 Y_{Cp} Y_C \quad (6-7)$$

It is evident a larger coupling C_p and larger filter capacitor C will aggravate the noise attenuation. From (6-7), it also justifies that reducing coupling C_p and adopting low capacitance for the T-connected capacitor will help reduce the degradation, leading to mitigation schemes presented in Section 6.5.1.

In a simplified case, if Z_1 and Z_2 are ideal inductors and Z_C is an ideal capacitor, λ can be expressed as

$$\lambda = S^4 L_1 L_2 C C_p = S^4 \frac{L_2 C_p}{\omega_1^2} \quad (\text{in } L_1 C - L_2) \quad \text{or} \quad \lambda = S^4 \frac{L_1 C_p}{\omega_2^2} \quad (\text{in } C_1 L_1 - C L_2) \quad (6-8)$$

where ω_1, ω_2 are the corner frequency of the first stage LC and second stage LC filter, respectively.

This discloses another mitigation direction in reducing the main filter components without impacting the corner frequency of the original filter. For LC-L or LC-LC filter, it is better to reduce C_p and L_2 , whereas, in CL-CL filter structure, it is wise to reduce C_p and L_1 . However, it has to be

noted that reducing inductance, in general, is not recommended if unnecessary, since it reduces the actual filter's series impedance, leading to higher noise current in the original filter without considering the coupling effect, thus limited effectiveness in reducing the degradation factor. Besides, the assumption for (6-6) may not be held under the low inductance condition.

The second approach is from the node-voltage analysis. This method is more accurate and can be extended for general filter structures, although it is not as straightforward as the topology view. As shown in Fig. 6-3, three node voltages can be defined. Two node-voltage equations associated with output node are derived as

$$\begin{cases} -Y_1 U_0 + \left(\sum Y_{T_i} \right) U_1 - Y_2 U_2 = 0 \\ -Y_{Cp} U_0 - Y_2 U_1 + \left(Y_2 + Y_{Cp} + Y_{LISN} \right) U_2 = 0 \\ \sum Y_{T_i} = Y_1 + Y_2 + Y_C \end{cases} \quad (6-9)$$

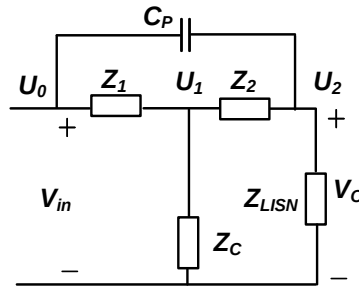


Fig. 6-3. General transfer gain analysis using node-voltage for capacitively coupled T-shape filter.

If U_1 is eliminated, the filter transfer gain ratio is

$$\frac{U_2}{U_0} = \frac{Y_1 Y_2 + Y_{Cp} \sum Y_{T_i}}{Y_1 Y_2 + Y_2 Y_{Cp} + Y_C Y_{Cp} + Y_{LISN} \sum Y_{T_i}} \quad (6-10)$$

Since $Y_{LISN} \gg Y_{Cp}$,

$$\frac{U_2}{U_0} \approx \frac{Y_1 Y_2 + Y_{Cp} \sum Y_{T_i}}{Y_1 Y_2 + Y_{LISN} Y_1 + Y_{LISN} Y_2} = \frac{Y_1 Y_2}{Y_1 Y_2 + Y_{LISN} Y_1 + Y_{LISN} Y_2} \left(1 + \frac{Y_{Cp} \sum Y_{T_i}}{Y_1 Y_2} \right) \quad (6-11)$$

Notice that the left part has nothing to do with C_p , thus the filter degrading factor, similar to the result of approach 1, can be approximated as below in the frequency range higher than the LC filter corner frequency, where $Y_C \gg Y_1$, and $Y_C \gg Y_2$.

$$\lambda = 1 + \frac{Y_{Cp} \sum Y_{T_i}}{Y_1 Y_2} \approx Z_1 Z_2 Y_{Cp} Y_C \quad (6-12)$$

The above two approaches present the analytical impact factors, providing guidelines to suppress the coupling effects. However, the simulation-based approach is also very helpful and in certain situation necessary, due to the nonlinear frequency-dependent impedance characteristics of inductors as well as the topology complexity of multi-stage filters. Details will be presented in the following sections and the general simulation approach will be abstracted in Section 6.7.

6.1.1.2 Capacitive coupling effect on T-shape CM filter

This following analysis will explore the impact of this coupling in T-shape CM filter. Since the CM choke impedance is the key factor, its characteristics will be analyzed first.

As well known, CM choke is never an ideal inductor and has very nonlinear frequency dependent impedance characteristics, due to magnetic core's complex permeability at frequency domain. At low frequency or static magnetic field, magnetic flux density B and magnetic field strength H are proportional to each other, resulting in a scalar ratio permeability. At high frequencies, due to the phase lagging of B over H , the complex permeability occurs as derived from (6-3),

$$\mu = \frac{B}{H} = \frac{B_0 e^{j(\omega t - \delta)}}{H_0 e^{j\omega t}} = \frac{B_0}{H_0} \cos \delta - j \frac{B_0}{H_0} \sin \delta = \mu' - j\mu'' \quad (6-13)$$

For a general N turn inductor without airgap, its impedance can be derived in phasor domain

$$\begin{aligned}
Z &= \frac{U}{I} = \frac{N \frac{d\phi}{dt}}{I} = \frac{N \frac{d(BA_c)}{dt}}{Hl/N} = \frac{N^2 A_c}{l} \frac{d(B_0 e^{j(\omega t - \delta)})}{H_0 e^{j\omega t} dt} \\
&= \frac{N^2 A_c}{l} j\omega(\mu' - j\mu'') = \omega \frac{N^2 A_c}{l} (\mu'' + j\mu') = R + jX
\end{aligned} \tag{6-14}$$

where l is the core magnetic length, A_c is the core cross-section area, and

$$\begin{cases} R = \omega\mu'' \frac{N^2 A_c}{l} = \omega\mu_r'' \frac{\mu_0 N^2 A_c}{l} \\ X = \omega\mu' \frac{N^2 A_c}{l} = \omega\mu_r' \frac{\mu_0 N^2 A_c}{l} \end{cases} \tag{6-15}$$

The imaginary part permeability represents the resistive impedance, while the real part becomes the inductive impedance, leading to the loss tangent factor as a measure of how much power is lost in the core and how much is stored.

$$\tan \delta = \frac{\mu''}{\mu'} = \frac{\mu_r''}{\mu_r'} \tag{6-16}$$

For a given choke, the core related resistance impedance is not only a function of imaginary permeability but proportional to frequency. Since core permeability itself is also a function of frequency, the impedance has even stronger frequency dependence. The same behavior is true for the inductive impedance. In fact, their relationship can be further deduced from (6-15) as in

$$\frac{R}{X} = \frac{\mu_r''}{\mu_r'} \tag{6-17}$$

If the permeability ratio is larger than 1, the choke is more resistive, otherwise, it is primarily inductive.

Fig. 6-4 shows the relative permeability for widely used two types of CM cores, nanocrystalline CM core and ferrite core [337]. The impedance of nanocrystalline choke becomes more resistive at much lower frequencies, e.g. tens of kHz, whereas the impedance of ferrite core is primarily inductive up to 1 MHz, and primarily resistive above 1 MHz. The fundamental difference will make the impact of this capacitive coupling also differently. However, one has also

to notice that at very high frequencies up to 30 MHz, due to the winding capacitance, the choke will inevitably become capacitive.

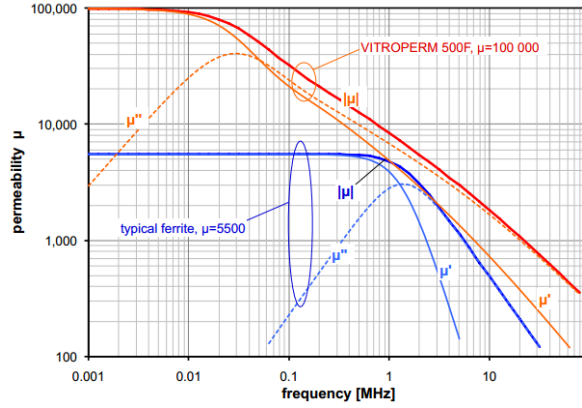


Fig. 6-4. Complex permeability of two different CM cores [337].

Then, back to the coupling issue. In the CM choke case, the choke impedance is still less than C_p impedance at low frequency range to hold the previous assumption, which will be verified later.

Z_{Y3} becomes

$$Z_{Y3} \approx j\omega C_p Z_{CM1} Z_{CM2} = j\omega C_p [R_{CM1}(\omega) + jX_{CM1}(\omega)][R_{CM2}(\omega) + jX_{CM2}(\omega)] \quad (6-18)$$

To evaluate its impact, three basic scenarios are analyzed, assuming two chokes have similar frequency characteristics owing to the same magnetic core type and winding scheme:

1). If $R \gg X$, Z_{Y3} will act approximately as a positive ESL, which is also strongly frequency dependent.

$$Z_{Y3} \approx j\omega C_p R_{CM1}(\omega) R_{CM2}(\omega) = j\omega ESL(\omega) \quad (6-19)$$

Although C_p could be very small such as pF level, this ESL is greatly amplified by the product of two CM chokes' high impedance. For example, if each choke has 3 kΩ at 1 MHz, a 1 pF coupling capacitor would be amplified by 9 million times and induce a 9 μH ESL in the CM capacitor branch!

This scenario could occur in nanocrystalline core above MHz and occur in ferrite core above several MHz, if reading from Fig. 6-3. However, for a specified core, the actual permeability curve or impedance measurement should be referred to obtain the accurate boundary.

2). If $X \gg R$, Z_{Y3} will act approximately as a negative ESL, which is less frequency dependent.

$$Z_{Y3} \approx -j\omega C_p X_{CM1} X_{CM2} \quad (6-20)$$

This scenario could occur in nanocrystalline core below 20 kHz and occur in ferrite core below MHz. Still, the actual permeability curve or impedance measurement should be referred to.

3). If R is closer to X , Z_{Y3} is a complex impedance as shown in (6-18). It will be like a frequency dependent complex impedance in series with the CM capacitor branch. And in a special case, if $R=X$, Z_{Y3} acts as a frequency dependent negative resistance.

$$Z_{Y3} \approx -2\omega C_p R_{CM1} R_{CM2} \quad (6-21)$$

This scenario could occur in nanocrystalline core from tens of kHz to several hundreds of kHz and occur in ferrite core around several MHz.

As one can also see, in general, the impact on nanocrystalline CM core is severer than that on ferrite CM core if assuming the same winding turns, due to the higher permeability in the former case. However, for a given attenuation requirement, ferrite CM choke may need more turns to obtain the same impedance, thus, the coupling impact may be enhanced. With regards to the frequency characteristics, ferrite CM choke will likely see the negative ESL effect at low frequency below MHz and positive ESL effect above MHz, whereas nanocrystalline CM choke sees the complex impedance effect and positive ESL effect in the conducted EMI frequency range.

The previous assumption on impedance ratio of CM choke and coupling capacitor has to be verified. A three-phase LCL prototype is used for this study. Two CM chokes are designed identically, with nanocrystalline core VITROPERM 500F W838 and three 3.3 nF film Y capacitors. The coupling capacitor is assumed as 1.5 pF based on the fitting between modeling and test. As

shown in Fig. 6-5, Z_p impedance is four times of choke impedance below 4 MHz, and 10 times larger below 2 MHz, Therefore, the assumption is generally valid below several MHz.

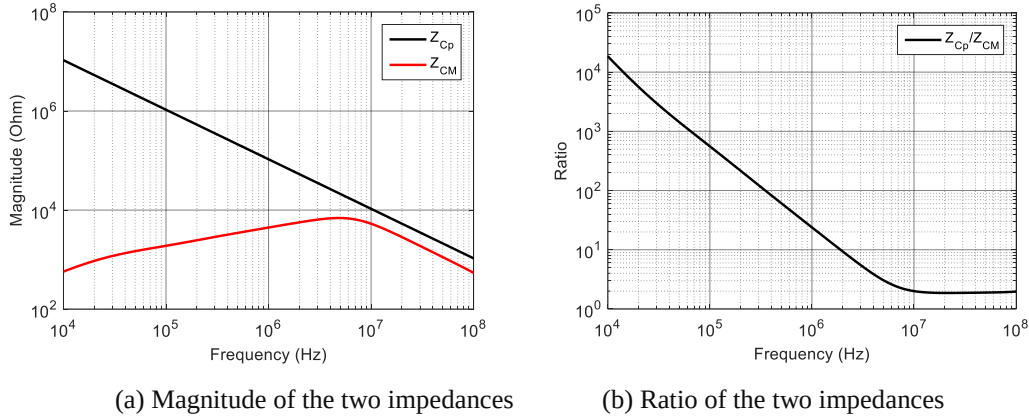


Fig. 6-5. Impedance magnitude ratio of C_p and the choke.

The impedance approximation in the above analysis is to give an explanation and better understand this coupling impact. To model and predict the filter attenuation, the actual impedance measurement will be used.

The actual relationship between R and X for the CM choke is measured as depicted in Fig. 6-6. Below 40 kHz, inductive impedance X is larger than resistive impedance R . And above 10 MHz, the capacitive impedance due to EPC dominates. In between, the dominant impedance is resistive. This matches the typical permeability curve of the CM nanocrystalline core.

Actual impedance of Z_{Y3} is shown in Fig. 6-7. From 1 MHz to 5 MHz, Z_{Y3} is mainly inductive due to dominant resistance impedance of CM choke. Below 10 kHz, Z_{Y3} is primarily negative inductive due to dominant X impedance of CM choke. From 20 kHz to 300 kHz, Z_{Y3} presents a negative resistive impedance, but its magnitude still has +40 dB/dec slope to frequency as if inductive. This result fairly matches the above analysis based on the three simplified scenarios.

In summary, regardless of the impedance components and polarities in Z_{Y3} , the most important conclusion is that for CM T-shape filter, the discovered capacitive coupling always induces a series

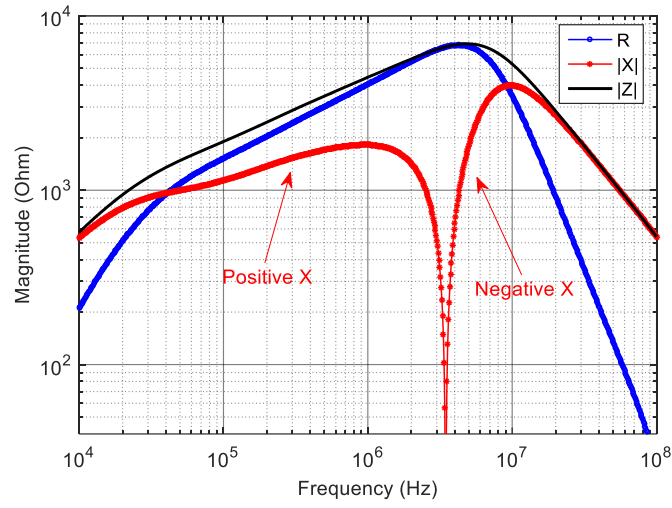
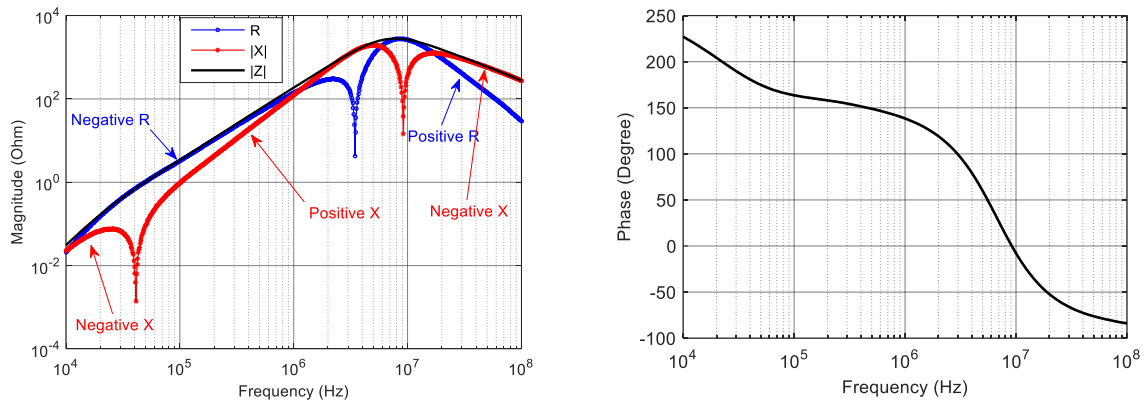


Fig. 6-6. Impedance magnitude of the choke.



(a) Magnitude and impedance breakdown

(b) Phase characteristics

Fig. 6-7. Impedance of Z_{Y3} in T-shape LCL CM filter.

“apparent inductive ESL^2 ” onto the CM capacitor branch showing +40 dB/dec slope, resulting from the product of two joint choke’s impedance as the amplification gain. This “apparent ESL^2 ” could significantly shift the corner frequency of the ideal LCL filter transfer gain to the much low frequency end, due to its high series inductive impedance at Y capacitor branch.

Using the measured filter impedance, the transfer gain of the filter can be modeled and predicted. Fig. 6-8 shows the CLC filter transfer gain along the frequencies. The actual transfer gain in the black curve is much poor than the modeling result if only considering self-parasitics as in magenta. The corner frequency occurs less than 500 kHz. After considering 1.5 pF coupling capacitance in the green curve, it matches the test result. Fig. 6-9 further shows the impact of PCB and space on the measured performance.

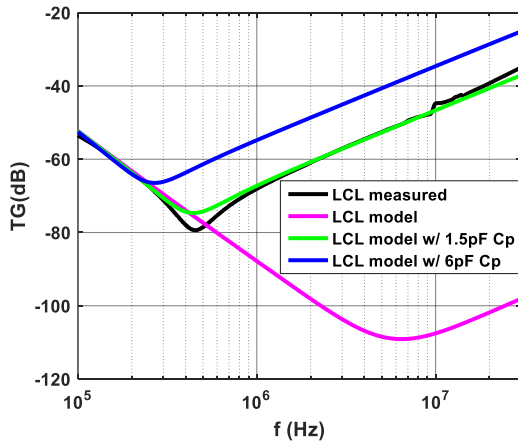


Fig. 6-8. Modeling and measured TG in LCL CM filter.

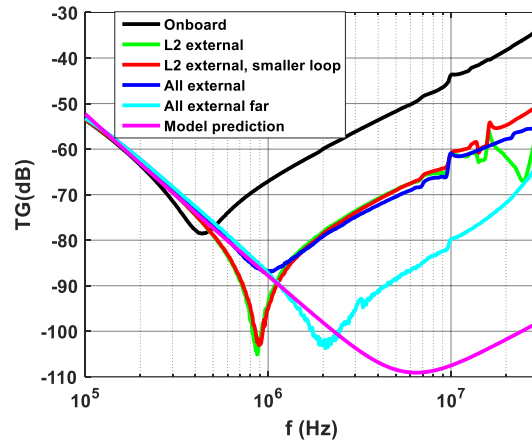


Fig. 6-9. Modeling and measured TG in LCL CM filter with different geometry arrangement.

6.1.1.3 Capacitive coupling effect on T-shape DM filter

In DM filter case, the capacitive coupling in T-shape cannot be overlooked either. Since DM inductors typically have a lower impedance than that of chokes, the assumption in (6-2) is valid at low frequency range, yielding

$$Z_{Y3} \approx j\omega C_p Z_{DM1} Z_{DM2} \approx -j\omega \cdot \omega^2 C_p L_{DM1} L_{DM2} \quad (6-22)$$

The effect is a negative frequency-dependent “ESL²” in the DM capacitor branch, less complicated than that in CM filter case, due to the relatively constant inductance at low frequencies as a result of air gap of the core. Again, a small mutual capacitance C_p can likely shift the resonance between DM capacitor and its ESL to much low frequency end.

A prototype of LCL DM filter was designed to verify this effect. RM8 core with ferrite N49 material as the L_{DM1} with 79 μH impedance and 6.9 MHz self-resonance frequency. High-flux powder core from Micrometal is adopted for L_{DM2} , with small-signal impedance 140 μH and 9.6 MHz resonance frequency.

Fig. 6-10 shows the impedance of Z_{Y3} calculated based on the measured impedance of each filter component. The magnitude slope is 60 dB/dec, and phase is -90 degrees below the self-resonant frequency of the inductor, confirming the above analysis.

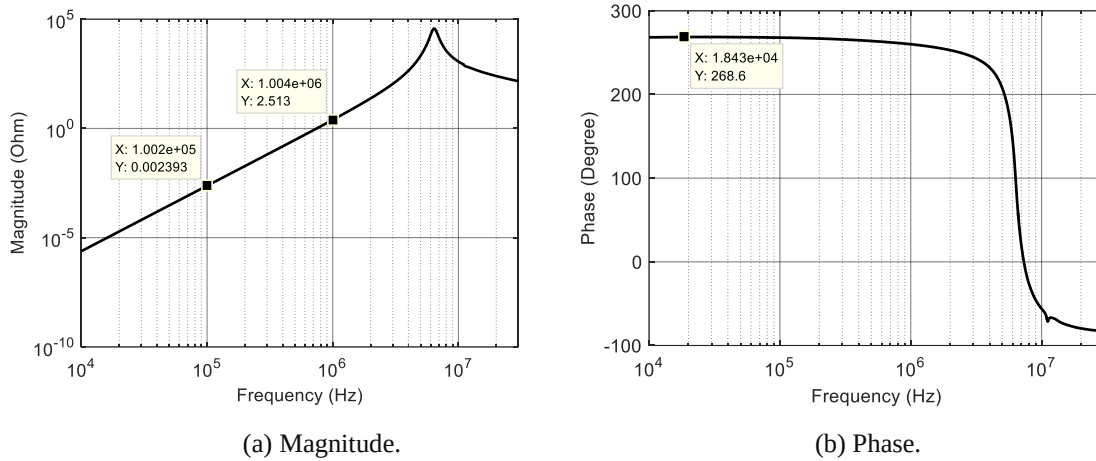


Fig. 6-10. Calculated impedance of Z_{Y3} in LCL CM filter.

6.1.2 Capacitive coupling in a general multi-component filter structure

From the above analysis, the capacitive coupling effect can be extended from a LCL T-shape structure to a generic filter structure with multi-components, as illustrated in Fig. 6-11. In this general ladder structure, N series of cascaded T-joints, in principle, can form C_{N+1}^2 parasitic

capacitances across the inductor terminals. These C_{N+1}^2 couplings can be categorized to three types: 1) N self-couplings within each T-joint; 2) 1 input-output coupling; 3) $C_{N+1}^2 - N - 1$ inter-couplings among different T-joints.

In principle, the type 2 coupling should be more critical, since it directly bridges the input and output. The other two coupling types also impact the filter performance. Theoretical analysis of the whole coupling effect using equivalent circuit approach becomes quite difficult, however, due to the complicated internal multi-T sections. Therefore, the node-voltage analysis as applied in Section 6.1.1.1 is adopted. For brevity, a two T-section filter is investigated first, since its simplified structure can demonstrate the basic pattern of the generic multiple T-section structures. This approach here can be scaled for the analysis of the multiple T-sections.

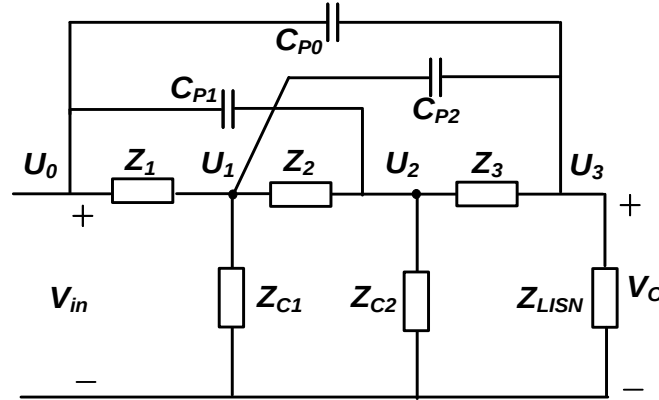


Fig. 6-11. Comprehensive capacitive coupling node-voltage circuit in a general multi-stage T-joint filter.

Three node-voltage equations can be derived for the three voltage nodes from U_1 to U_3 , as shown below. The filter transfer gain defined as the ratio of U_3 to U_0 can be easily obtained.

$$\begin{cases} -Y_1 U_0 + \left(\sum Y_{T_i}\right) U_1 - Y_2 U_2 = 0 \\ -Y_{C_{p1}} U_0 - Y_2 U_1 + \left(\sum Y_{T_i}\right) U_2 - Y_3 U_2 = 0 \\ -Y_{C_{p0}} U_0 - Y_{C_{p2}} U_1 - Y_3 U_2 + \left(\sum Y_{T_i}\right) U_3 = 0 \\ \sum Y_{T_i} = Y_1 + Y_2 + Y_{C_1} + Y_{C_{p2}} \\ \sum Y_{T_i} = Y_2 + Y_3 + Y_{C_2} + Y_{C_{p1}} \\ \sum Y_{T_i} = Y_3 + Y_{C_{p0}} + Y_{LISN} \end{cases} \quad (6-23)$$

For a general LC based low pass EMI filter, the following approximations can be used in the frequency range of interest to further simplify the solving procedure.

$$\begin{cases} (Y_{C_{p0}}, Y_{C_{p1}}, Y_{C_{p2}}) \ll (Y_1, Y_2, Y_3, Y_{C_1}, Y_{C_2}) \\ (Y_1, Y_2, Y_3) \ll Y_{LISN} \ll (Y_{C_1}, Y_{C_2}) \end{cases} \quad (6-24)$$

Another way to study this impact is through frequency domain simulation, as will be illustrated in Section 6.7.

6.1.2.1 Capacitive coupling in two-stage CM filter

Since LCLC or CLCL CM filter contains T-joint, the above capacitive coupling also affects the filtering performance of two-stage filters. A frequency domain simulation using the actual measured impedance of components in a two-stage LCLC CM filter under different coupling C_p is conducted. The result in Fig. 6-12 shows that even a very small coupling C_p 1.5pF/19 can significantly degrade the two-stage filter's attenuation by nearly 40 dB above 1 MHz.

6.1.2.2 Capacitive coupling in two-stage DM filter

And transfer gain of the two-stage LCLC filter without and with the capacitive coupling are compared in Fig. 6-13, using the filter prototype as described in Section 6.1.1.2. A 3 pF coupling C_p is assumed between the input and output terminals. Here other couplings are not included. Attenuation starts to decrease after 400 kHz. The highest degradation can be up to 80 dB.

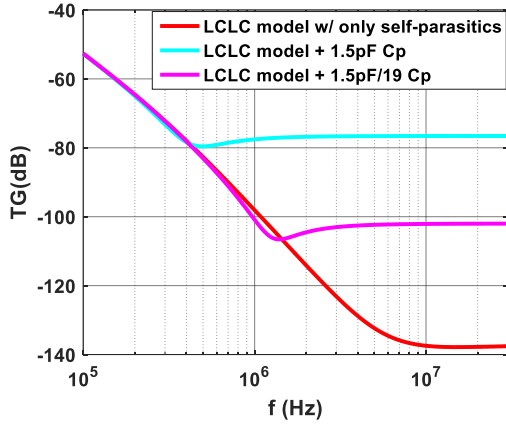


Fig. 6-12. TG curves of a two-stage LCLC CM filter with different capacitive couplings.

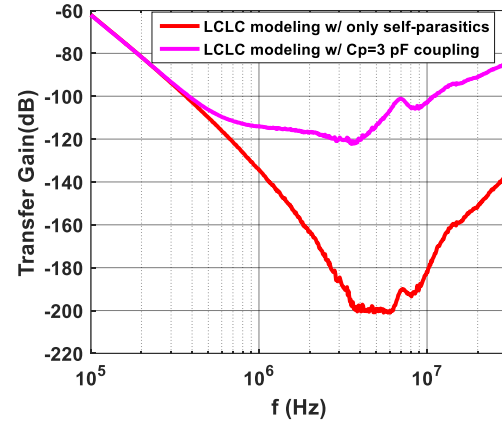


Fig. 6-13. TG curves of a two-stage LCLC DM filter without and with 3pF capacitive coupling.

6.2 Inductive coupling

Compared to the aforementioned capacitive coupling in the T-shape filter, the inductive coupling has been widely reported in the CLC π -shape filter. In this section, the impact of this coupling will be briefly reviewed as the basis for discussion in the next section.

6.2.1 Inductive coupling in CLC π -shape structure

Because of the low capacitive impedance in the input and output loops in the CLC structure, the noisy current source circulating in the input loop can induce a coupled voltage onto the output loop to be observed by LISN. This coupling, as proved to be the dominant coupling mechanism in π filters, as shown in Fig. 6-14, can be transmitted from the mutual flux of stray inductance of the PCB traces, or the loop area of the input and output loops, or the body of the two capacitors. As discussed in [247], no matter which cases, the path can be equivalently modeled with a lumped inductive coupling term M . Because of the overwhelmingly high ratio of noise current and output loop current jumping as frequency increases, a small M can deteriorate the filter attenuation starting from MHz or 100s of kHz. The impact is not only significant in the π -shape DM filter

[242], but also surprisingly high in CM filters [247], regardless of the different impedance characteristics of CM and DM inductors.

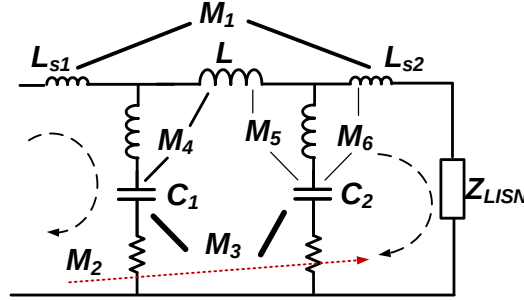


Fig. 6-14. Different inductive couplings in a π -shape DM filter.

6.2.2 Inductive coupling in other basic filter structures

Since LCLC and CLCL type multi-component filters also contain the CLC unit, these filters will also suffer from the inductive coupling effect. This is eventually extended to the partial of the general coupling theory in Section 6.4.

6.3 Duality of LCL and CLC filter structure

From the analysis of CLC filter and LCL filter structures in previous sections, one important conclusion can be drawn is that in the LCL structure, the dominant coupling effect is from inductive coupling between the input and output loops, whereas in the CLC structure the dominant coupling effect is from capacitive mutual coupling between the input and output terminals. This presents an interesting duality feature between the two basic structures T-shape and π -shape: the inductive coupling in π -shape is transformed to capacitive coupling in T-shape and the effect that one is immune to becomes the effect the other is most vulnerable to and vice versa.

6.4 General coupling theory

From the duality principles of the two basic structures, the general coupling theory can be summarized here. In a general cascaded filter structure shown in Fig. 6-15, both the inductive and capacitive couplings exist and the dominant couplings that influence the filter attenuation mostly can be marked in Fig. 6-16 using lumped components.

Other couplings, such as the paralleled capacitive coupling from the ground plane to the inductors, can be categorized into the Z impedance of the general model as the extra equivalent parallel capacitance (EPC) of inductors or ESL of capacitors. Hence these couplings are analogous to self-parasitics and have relatively minor impacts.

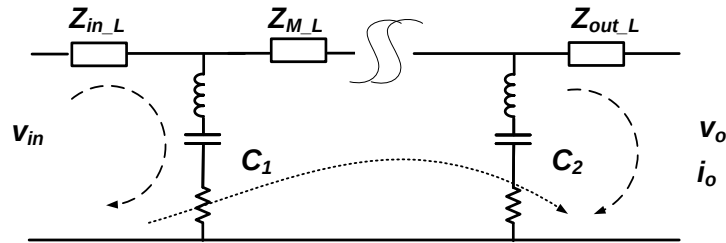


Fig. 6-15. General inductive couplings in a multi-component filter.

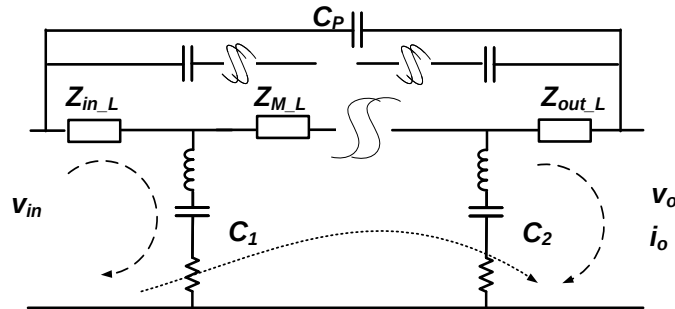


Fig. 6-16. General couplings including both capacitive and inductive effects in a multi-component filter.

6.4.1 General inductive coupling

In general, all the loop currents can induce mutual inductive coupling through the magnetic field, yielding to C_N^2 types of loop couplings. In practice, however, it has been experimentally

proved that the input and output loop have the strongest coupling effect. This can be well understood because the input loop current noise has the highest strength, and output loop current noise is far attenuated according to the filter insertion loss curve. Their coupling can be mathematically expressed in (6-25), where M is the coupling inductance. Z_{in} and Z_{out} are the total impedance of input and output loops, respectively.

$$I_{out}(s) = \frac{M \cdot I_{in}(s)}{Z_{out}} = \frac{M \cdot V_{in}(s)}{Z_{in} Z_{out}} = \frac{M \cdot V_{in}(s)}{(Z_s + Z_{in_L} + Z_{C_2})(Z_{out_L} + Z_{LISN} + Z_{C_2})} \quad (6-25)$$

If Z_s is small, for example in 50 Ω testing system or in the case of ac DM filter, (6-25) can be simplified as

$$I_{out}(s) = \frac{M \cdot V_{in}(s)}{Z_{in} Z_{out}} \approx \frac{M \cdot V_{in}(s)}{Z_{in_L} Z_{out_L}} \quad (6-26)$$

From the above two equations, several useful conclusions can be obtained. It should be noted that LISN impedance is regarded as low impedance for the coupling analysis here.

First, for the low source impedance and low load impedance system, the coupling impact can be summarized in Table 6-1 .

Table 6-1. Converter set up with low source and low load impedance.

Filter structures	Input loop impedance	Output loop impedance	Inductive coupling
CLC	low	low	highest
LCL	high	high	lowest
LCLC	high	low	medium
CLCL	low	high	medium

As a rule of thumb, for ac side DM filters, the source impedance of converters is low, unless a power filtering inductor is already included in the source side; For dc side DM filters, since noise source can be modeled as a current noise source, its source impedance is often high. For CM filters, converters with high grounding parasitic capacitance have low capacitive source impedance and have high source impedance if its grounding parasitics are low.

For low Z_s cases, to interface with CL or LC components makes difference. However, this becomes insensitive in high Z_s cases, since input loop Z_{in} is already high, regardless of CL or LC. The details are given in Table 6-2 and Table 6-3.

Table 6-2. Converter set up with high source and high load impedance.

Filter structures	Input loop impedance	Output loop impedance	Inductive coupling
CLC	high Z_s + low Z_C	low	highest
LCL	high Z_s + high Z_L	high	lowest
LCLC	high Z_s + high Z_L	low	medium
CLCL	high Z_s + low Z_C	high	lower

As a conclusion, no matter CM or DM mode or any converter source impedance condition, LCL has the least coupling effect. CLC has the highest coupling effect. LCLC or CLCL has the medium coupling effect. And CLCL can also have the lower coupling effect in high Z_s condition.

Table 6-3. Converter set up with low source and low load impedance.

Filter structures	Input loop impedance	Output loop impedance	Inductive coupling
CLC	low Z_s + low Z_C	low	highest
LCL	low Z_s + high Z_L	high	lowest
LCLC	low Z_s + high Z_L	low	medium
CLCL	low Z_s + low Z_L	high	medium

Another thing to be noticed is that in DM filters, the leakage flux from winding gets larger than CM filter due to the low permeability of the DM core, leading to more couple noise onto the output loop. However, the input-loop noise is still higher and dominant.

6.4.2 General capacitive coupling

When taking the aforementioned capacitive coupling into account, the extended coupling is summarized in Table 6-4.

Table 6-4. General dominant coupling effects in typical filter structures.

Filter structures	Inductive coupling	Capacitive coupling
CLC	highest	lowest
LCL	lowest	highest
LCLC	medium	one T-joint, high
CLCL	Medium/lower	one T-joint, high

It is highlighted that LCLC and CLCL have the combined effect. They suffer from the capacitive coupling effect due to the LCL T-joint, and from the inductive coupling effect due to coupling between the input loop and the output loop. For these cases with both coupling effects, some general behaviors can be summarized as follows.

With mutual C_p at pF level, the capacitive coupling dominates and occurs from low frequency, such as hundreds of kHz. Whereas, the inductive coupling effect in CM cases usually occurs at frequencies above MHz and could occur at hundreds of kHz in DM cases, mainly related to mutual inductance M value and filter capacitor value.

With mutual C_p at 100 fF level or less, both capacitive coupling and inductive coupling are visible and mingles together.

With mutual C_p at several fF levels, the inductive coupling dominates and can occur from MHz or 100s of kHz if mutual inductance M is less than several nH. Whereas, the capacitive coupling becomes trivial and occurs above MHz.

Although the test result of transfer gain in 50 Ω instrumental environment is different from that in real converter set-up, the general theory is valid for both scenarios.

6.4.3 Generalized filter topology selection criteria

The presented general coupling theory provides another criterion for filter topology selection, in addition to the basic impedance mismatching principle which only considers the ideal filter

impedance characteristics. Together, a suitable filter topology can be selected taking account of the main coupling impact from physical implementation.

Some of the coupling effects could be easily mitigated if choosing the right filter structure even the basic mismatching may be not perfectly met. As a result, a low effort design and decent filter attenuation can still be achieved. Of course, the best filter attenuation performance could be achieved if basic mismatching is ensured together with the least coupling either from topology nature or from coupling mitigation solutions, as will be presented in Section 6.5.

Further discussion and verification are given in Section 6.7.3.

6.4.4 Experimental verification of compound couplings

Fig. 6-17 gives comparisons of the modeled and measured transfer gain (TG) in a LCLC DM filter. When considering 6 pF C_p coupling as shown in the magenta curve, TG is significantly reduced compared to the predicted red curve with only self-parasitics modeled. Yet, it is better than the final measurement in the green curve. This indicates other coupling effects exist. After further considering 0.35 nH input-output loop inductive coupling in Fig. 6-18, attenuation at high frequency also matches. The result clearly shows that inductive and capacitive coupling effects coexist, and both have significant impacts on LCLC DM filter attenuation.

However, some mismatch is also observed around 1MHz. This is because of the remaining couplings in the three-phase set-up, as illustrated in the measured TG curves with two different loop arrangements. It is shown that this portion of attenuation is sensitive to the specific placement of DM capacitors and the area of the input and output loops.

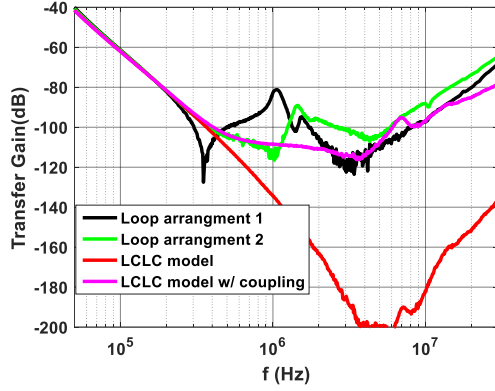


Fig. 6-17. TG in LCLC DM filter, with 6 nF C_p coupling.

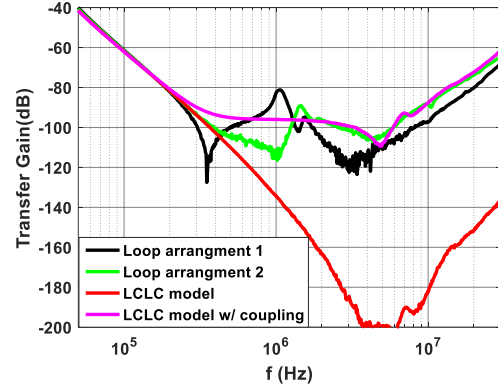


Fig. 6-18. TG in LCLC DM filter, with 6 nF C_p coupling and 0.35 nH inductive coupling.

6.5 Coupling mitigation methods

6.5.1 Capacitive coupling mitigation

From (6-2), it is obvious if the coupling C_p can be significantly reduced, the induced equivalent ESL in the capacitor branch of T-shape filter will be correspondingly reduced.

From (6-7), it is also anticipated that reducing the coupling C_p and adopting low capacitance for the T-connected capacitor can help reduce the filter degradation factor λ .

Therefore, following the above conclusions, different coupling schemes are explored, and the coupling physical mechanism is also investigated.

6.5.1.1 Investigation of physical cause of capacitive coupling

When two inductors are placed nearby on a PCB, an electrical field is built up between the two electrical components through the dielectric medium. If considering only the static field, the wires on the core is like a short connection. There will be two paralleled dielectric mediums, i.e. air and PCB material. And two paralleled coupling capacitors are formed, as shown in Fig. 6-19.

For a general FR4 PCB material, its permittivity relative to vacuum is around 4, and air permittivity is 1. Owing to the permittivity difference, the charge distribution will be different.

Higher permittivity means higher conductivity, thus attracts more electric charges and tends to induce higher capacitance. On the other hand, the capacitance is also determined by the area of the two poles. The thickness of the PCB is below 1.6 mm, resulting in an area much lower than the air. Therefore, the extra capacitances of the two will be related to the specific distance between the two inductors, and the size of the core.

To further verify the above circuit analysis and inference, a 3D FEM simulation is conducted in Ansys Maxwell. From the electric displacement field D flux shown in Fig. 6-20, it clearly shows the distribution of charge, since D is proportional to the surface charge according to Gauss's law.

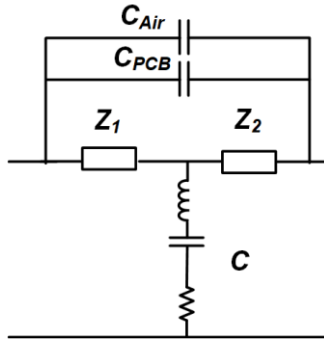


Fig. 6-19. Equivalent coupling capacitances in a T-shape filter populated on a PCB board.

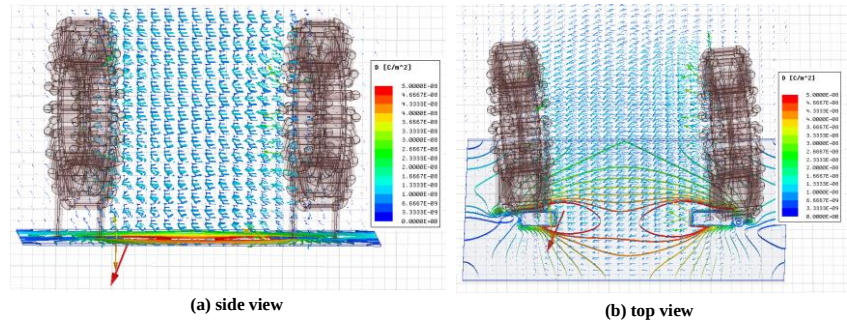


Fig. 6-20. 3D FEM simulation on two nearby toroidal ferrite core inductors.

$$\oint_A D \cdot dA = Q \quad (6-27)$$

6.5.1.2 PCB layout and shielding

Considering the aforementioned coupling paths, two basic approaches from PCB layout and shielding, respectively, are adopted to tackle this capacitive coupling issue.

The first scheme is to reduce coupling capacitance from PCB medium and layout. Replacing standard FR4 PCB materials by low permittivity dielectrics such as FR408 can help reduce C_p . However, this may slightly increase manufacture cost. Another simpler method is to reduce the

FR4 PCB contact between input and output filter terminals by creating slots to form a barrier between two inductors on the filter board, only leaving sufficient width to lay the three-phase power traces in a vertical manner via a multilayer design. Since air permittivity is roughly $\frac{1}{4}$ of the FR4 and electricity charge gathers more at high permittivity material side, therefore, PCB slits reduce displacement charges in FR4 medium and redistribute the charges more into space. A design concept is shown in Fig. 6-21 for the final filter board layout. In fact, by using multi-layer design, the vertical layout can also reduce the inter-phase coupling loops, which also benefits the inductive coupling mitigation.

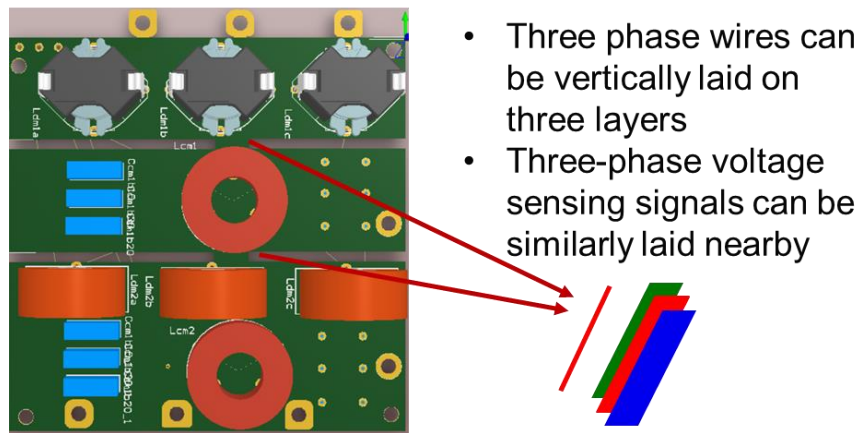


Fig. 6-21. Reduction of coupling through PCB slit and trace arrangement.

Secondly, since capacitive coupling is induced by the electrical field, another effective way to reduce this coupling is electrical shielding. Shielding design is helpful to reduce the mutual coupling capacitance through space. By inserting a metal shield between the two inductors and connecting this shield to the noise return path such as a ground plane in CM mode, it weakens the electric field penetration and provides a bypass path to the return path, as if an induced coupling capacitor exists between the inductor and the “grounded” shield. As for a CM filter, this return path is the ground plane. For a DM filter, the return path is either the neutral for a three-phase filter,

or the mid-point of the two series X capacitors for a single-phase or dc line filter with a balanced structure, or the negative line for the imbalanced case. In the case of a combined CM and DM filter, one CM shield is enough for both CM and DM shielding purposes, since the grounding joint of the Y capacitors also forms a DM neutral.

To enhance the effectiveness of the shielding, the proper material type should be selected. The primary mechanism of the shielding is the reflection, which requires mobile charge carriers on the shield surface [338]. Therefore, the shields usually tend to be electronically conductive, though it is not the scientific criterion [338]. The secondary mechanism is the absorption, which usually has electric or magnetic dipoles. The two different shielding approaches are characterized by their reflection loss and absorption loss, respectively. According to [338], reflection loss is a function of the ratio of σ_r/μ_r , and absorption is a function of the product $\sigma_r\mu_r$. And based on electrical conductivity and magnetic permeability of different materials in [338], copper is often selected for electrical shielding.

It has to be noted that for a conductive shield, eddy current could be induced under a changing magnetic field, thus the eddy current loss in principle should also be considered. However, for the T-shape filter, the leakage magnetic flux penetrating the shield in between is generally low, due to the relatively high permeability core of the two nearby inductors, especially in the CM filter case. The induced loss is therefore negligible, as confirmed later in experimental results. In some extreme low power applications, if any unnecessary loss is to be avoided, some slots can be made on the shield surface to break the eddy current loops as a typical practice.

Last but importantly, it has been observed that the shield should be inserted through the PCB board via the slits between the two inductors to achieve the most effective shielding performance, instead of being glued on the board surface.

To verify the above conclusions, a series of early comparison tests are carried out. As shown in Fig. 6-22, once PCB slits are machined, 10 dB more attenuation improvement through 800 kHz to 30 MHz is achieved for LCL T-shape filter, compared to the case without slots. Shielding schemes with high conductivity copper and high permeability magnet shielding alloy MagnetShield #274 with the similar dimensions are also conducted. An extra 10 dB around attenuation is achieved from shielding. The results also indicate that the differences from material properties have little impact on the shielding performance, at least for this unenclosed shielding structure. However, the location of shielding and the area of shielding do make differences.

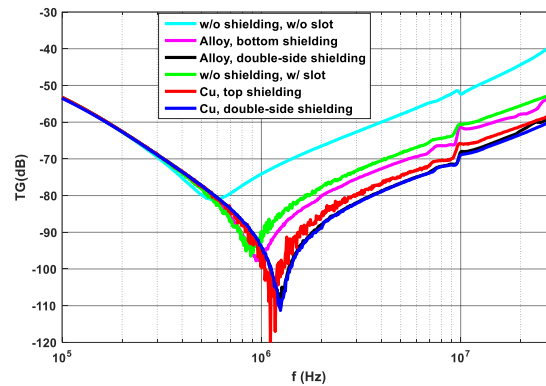


Fig. 6-22. Performance comparison of different shielding arrangements.

In addition, from Fig. 6-24 the thermal image of the filter board in a 235 V_{ac} input, 360 Hz line frequency, and 1.5 kW three-phase rectifier, the temperature of the shield is almost ambient temperature, indicating the eddy current loss induced by the leakage magnetic field is negligible.

From the above early tests on the original filter board, the top side shielding is more effective, and the bottom shielding could be removed since it may block the air flow in the subject converter system with bottom cooled GaN devices. Putting these useful observations into the revised filter board, the final testing results of LCL CM filter based on a customized RF interface board shown in Fig. 6-25 are given in Fig. 6-26. Compared to the original TG without slits, the corner frequency

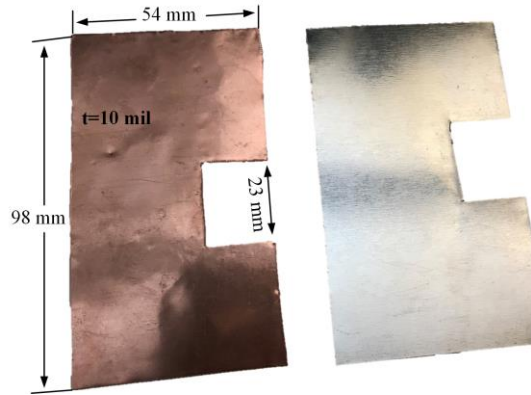


Fig. 6-23. Photo of the two different shields. Left: copper, right: MagnetShield #274.

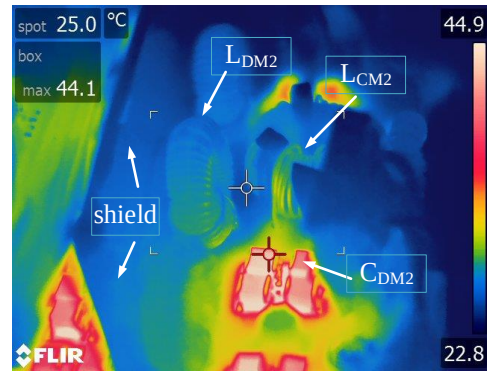


Fig. 6-24. Thermal image of the EMI filter with the proposed shield under ac-dc rectifier operation.

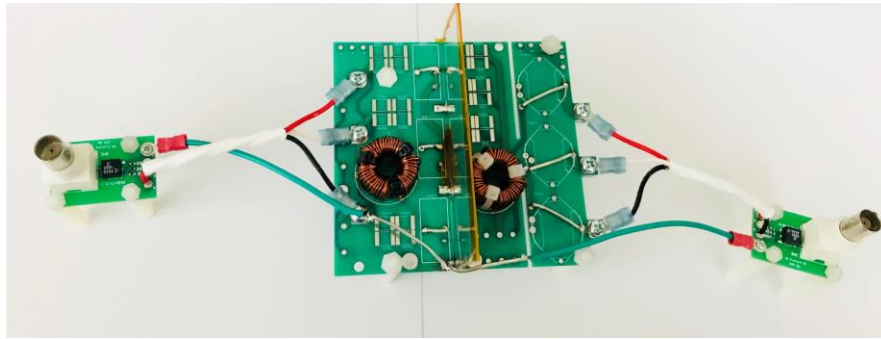


Fig. 6-25. LCL filter with customized RF interfaces on two ends for transfer gain test.

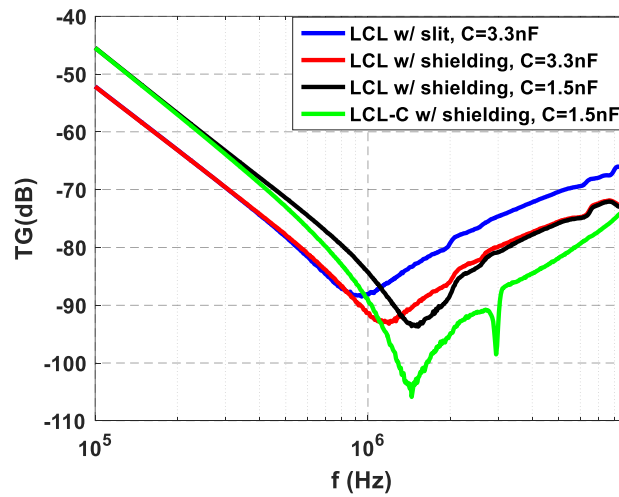


Fig. 6-26. Comparison of the transfer gain of LCL CM filter with improved shielding design.

is increased from 500 kHz to 900 kHz with just slits and is further increased to 1.5 MHz by adding the top shield.

6.5.1.3 Split capacitance to mitigate capacitive coupling

As analyzed in (6-7), once the capacitance in the T-branch is reduced, the degrading factor of filter performance is also proportionally reduced. The scheme is shown in Fig. 6-27. However, reduced capacitance negatively impacts the filter's original performance when no coupling effect is considered, especially in the CL filter structure which heavily weighs on the capacitor to filter the main noise so that L can be reduced. To compensate this side-effect, another capacitor is added after the T network to provide extra -20 dB slope. This is particularly important for HF range, due to the poor attenuation at HF resulting from capacitive coupling effect. Considering the limited total capacitance either by leakage current requirement for CM case or by power factor constraint in DM case, a scheme to split the original maximum bypass filter C into halves is finally adopted. The trade-off is that attenuation at 100s of kHz frequency will be decreased roughly by $40 \cdot \log(1.4142) = 13.8$ dB as the shunt branch capacitance is reduced by half. Of course, the split ratio can be adjusted based on the specific condition if necessary.

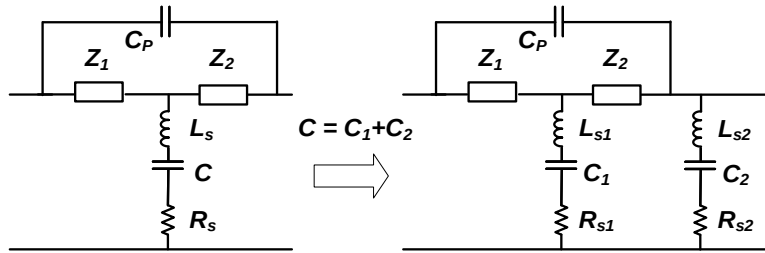


Fig. 6-27. Split capacitor scheme for coupling reduction at HF.

For a CM filter, since the EPC of a CM choke is around several pF, the added Y capacitor together with the front inductive impedance forms a LC filter at medium frequencies, and at HF performs as a C-C divider with EPC of chokes and as a RC filter with LISN.

As also illustrated from the above TG result of the LCL-C filter in Fig. 6-26, up to 15 dB higher attenuation at HF is achieved by splitting the 2nd 3.3 nF Y capacitor to two 1.5 nF, although with 7 dB less attenuation at low frequency range due to the reduced T branch capacitance. In addition, it has to be mentioned two practical side effects from the third stage may offset the benefits of the third stage capacitor. The first issue is inductive coupling because of the low-impedance output loop formed by this third capacitor and LISN load. Similar to other inductive couplings as analyzed in Section 6.2, the sensitivity of this loop coupling is strongly affected by the loop area, and general minimization methods, as well as a proposed layout, are discussed in Section 6.5.2 and 6.5.3.

The other issue is grounding for a multi-stage filter. As analyzed in [264, 339], the grounding connection of two-stage CM Y capacitors should be separately tied to the ground plane to avoid the common noise voltage induced by the impedance ground loop and the predominant noise current from the first stage Y capacitor. With the newly introduced Y capacitor at the third stage, we should also separate the ground connection from the second stage. Impact of the common grounding and the improved split grounding are compared using the transfer gain measurement of a CLCLC CM filter structure shown in Fig. 6-28 with other DM inductors also populated. Clearly, HF attenuation of the filter can be improved by 12 dB with the split grounding. Please notice that these tests are done with the proposed shielding layer already added.

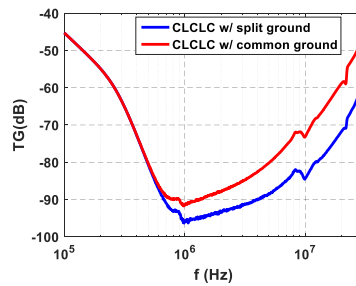


Fig. 6-28. Impact of the LISN side grounding schemes on filter performance.

6.5.2 Inductive coupling mitigation

The inductive coupling can occur between two stage capacitors owing to their ESL between stray inductances of two nearby branch, between nearby inductors, between L and C, and eventually forming the equivalent coupling between two loops, as given in Section 6.2.1.

The coupling issue is more severe in DM filter and less severe in CM filter. Firstly, CM core has higher permeability, thus has less flux leakage outside the core. Secondly, CM capacitor has low value and much smaller volume, thus less chance to be coupled and less flux induced from its low ESL.

Since coupled flux is linked through the space, proper position of the components helps. The impact from the relative position of two DM inductors on filter attenuation is studied in [242] and [244], showing effective in improving the transfer gain by 5 dB in [242] but no effect in [244].

A coupling mitigation method between two DM film capacitors in a PI filter is also proposed in [246], with an external a $\frac{3}{4}$ turn winding packaged next to the film capacitor.

Some recommendations on filter component placement and trace layout have been reported for single-phase/dc side filters [242, 244, 246], either arranging the leakage flux perpendicular to the coupling loop or minimizing the loop of DM capacitor connection by gradually shrinking the traces from two leads considering the clearance requirement. The basic principles are helpful in single-phase filter design, yet some of them are not applicable to three-phase filter, and no clear guidelines are ready for this application yet.

On the other hand, although two-stage filter has much higher attenuation and in general can reduce the inductance and size of the filter, it is vulnerable to noise coupling among LC components. The high strength noise component can impose significant coupling voltage onto the weak noise component, such as the case from first stage filter to the second stage filter. Previous

work has been focused on the coupling mechanism and mitigation methods in the single-phase or dc line filter design. There are few guidelines on how to design the three-phase EMI filter. A design that works for single-phase might not work as expected in three-phase. In this work, the coupling mechanism and coupling impact for three-phase filter performance in addition to the known knowledge are preliminarily explored, and approaches to reduce the coupling are proposed.

First, a single-phase test for a three-phase DM filter is carried out. Fig. 6-29 shows the small-signal transfer gain of this single-stage single-phase DM filter. The test result, measurement-based modeling without considering component coupling, and the ideal filter performance are compared. It is shown that during the single-phase test, three results for the single-stage filter have similar transfer gain, except that above 2 MHz, the parasitics of the L_{DM} and C_{DM} forms serial and parallel resonance, degrading the filter attenuation. Therefore, there is no coupling in the single-stage single phase filter.

Then, a three-phase test for single-stage DM filter is examined as shown in Fig. 6-30. Compared to single-phase result and three-phase modeling, the test result has about 10 dB mismatch above 2 MHz. And at 900 kHz, there is also a resonance peak. This indicates among the three-phase, there already exists some coupling as well as higher ESL.

For the two-stage filter, significant degradation is observed. From Fig. 6-31, the actual transfer gain begins to drop above 200 kHz, which is far below the desired filter gain as shown in the modeling result in red curve. The modeling result is also validated by the sum of the two stages' individual transfer gain, according to impedance mismatching principle.

First, coupling between the first-stage LC filter and second-stage DM capacitors matters. As shown in Fig. 6-32, if increasing the distance between the second-stage DM capacitor and the first-stage filter, filter attenuation can be increased by 5-10 dB from 200 kHz to 1 MHz.

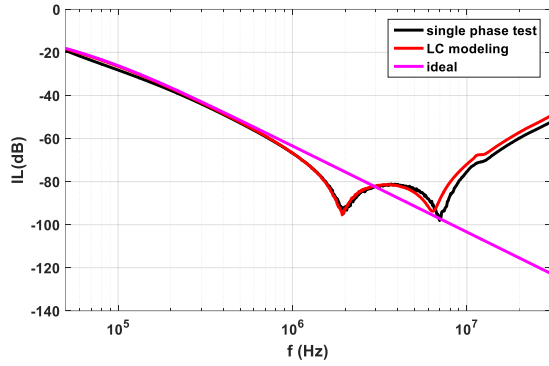


Fig. 6-29. Transfer gain test of a single-phase single-stage LC filter based on a three-phase DM filter.

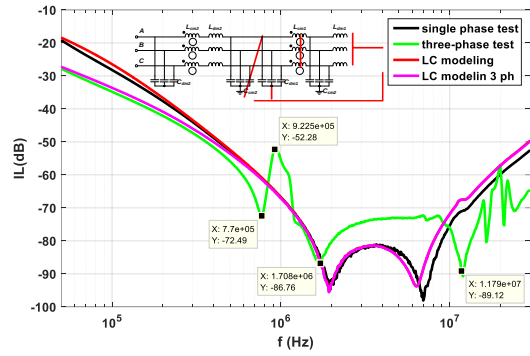


Fig. 6-30. Transfer gain test of a three-phase single-stage LC type DM filter.

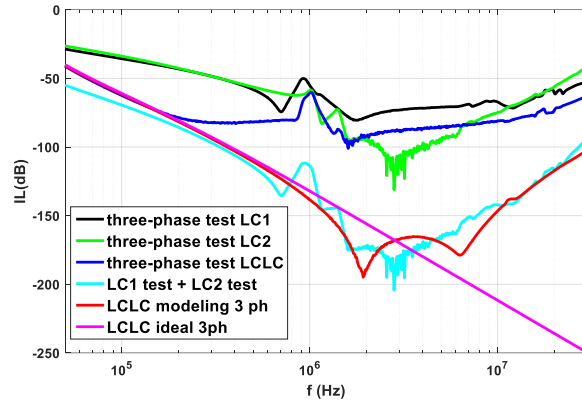


Fig. 6-31. Transfer gain comparison among three-phase two-stage LC type DM filter, its individual stages, and its measurement-based modeling.

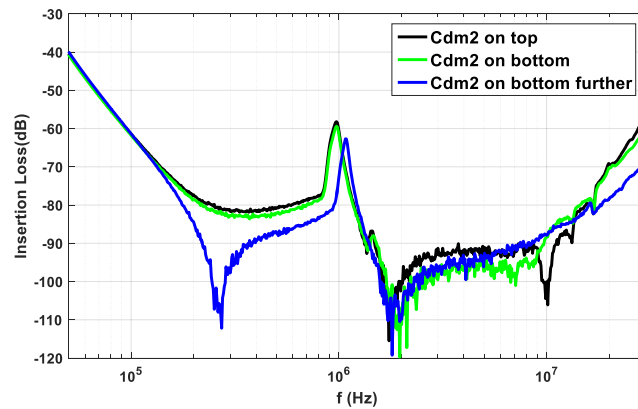


Fig. 6-32. Impact of DM capacitor location on filter transfer gain.

The position and space volume of second-stage DM capacitors also impact the strength of noise coupling. Fig. 6-33 shows a serial test by vertically placing the second-stage DM capacitors or reducing their size with low profile ceramic capacitors instead of bulky film capacitors, as illustrated in Fig. 6-34. 15 dB attenuation improvements can be obtained as shown in the blue curve.

The most critical coupling exists between the neutral branch formed by three-phase DM capacitors and first-stage LC filter, as shown in Fig. 6-35. This neutral branch is very sensitive to noise, since it parallels with $50\ \Omega$ RF terminators of three LISNs. Associated with this branch, two semi-loops should be minimized to avoid possible magnetic coupling. One is the output semi-loop formed by the inter-phase terminals and LISNs, and the other is the semi-loop formed by the inter-phase DM capacitors. Together, they form the line-to-line DM output loop. This points to the fundamental difference between single-phase DM capacitor and three-phase DM capacitor, where only one lead connects to the power terminal, and the other lead connects with other two phases to form the ac neutral. The noise flow is not directive.

The coupling noise mainly comes from the first-stage emission. It can be the leakage flux of the DM inductor, emitting from the air gaps, or it can be the noise emission through a similar neutral loop formed by inter-phase LC. When the neutral loop of second-stage DM capacitors is laid on the horizontal PCB plane, emitted noise from the first-stage LC filter will be likely coupled.

The above analysis is further verified by the transfer gain measurements, as provided in Fig. 6-36. When placing C_{dm2} vertically, the coupling area can be reduced, thus filter transfer gain marked in the black curve is improved. In addition, if C_{dm2} is replaced from film capacitors to ceramic capacitors, the transfer gain marked in the blue curve is further increased.

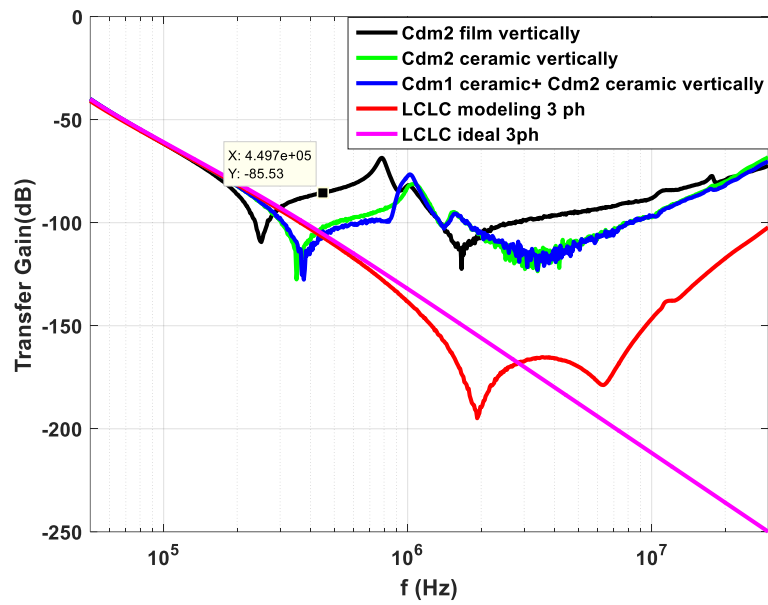


Fig. 6-33. Impact of DM capacitor position and size on the filter transfer gain.

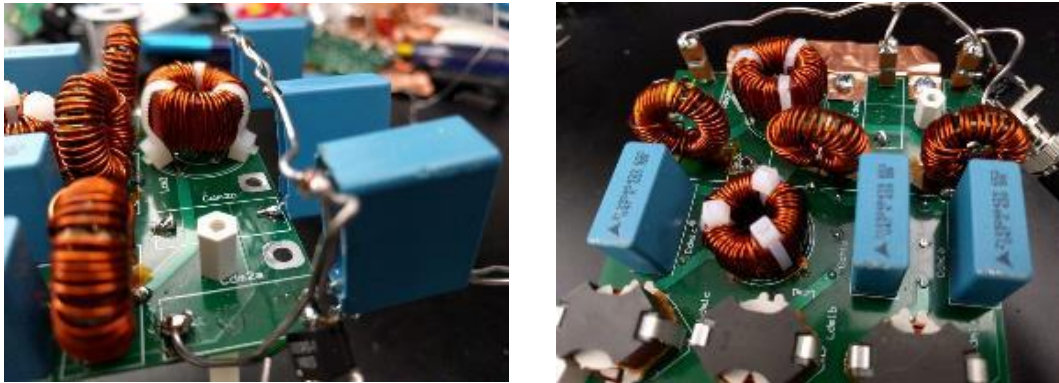


Fig. 6-34. Two vertical placements of two types of DM capacitors.

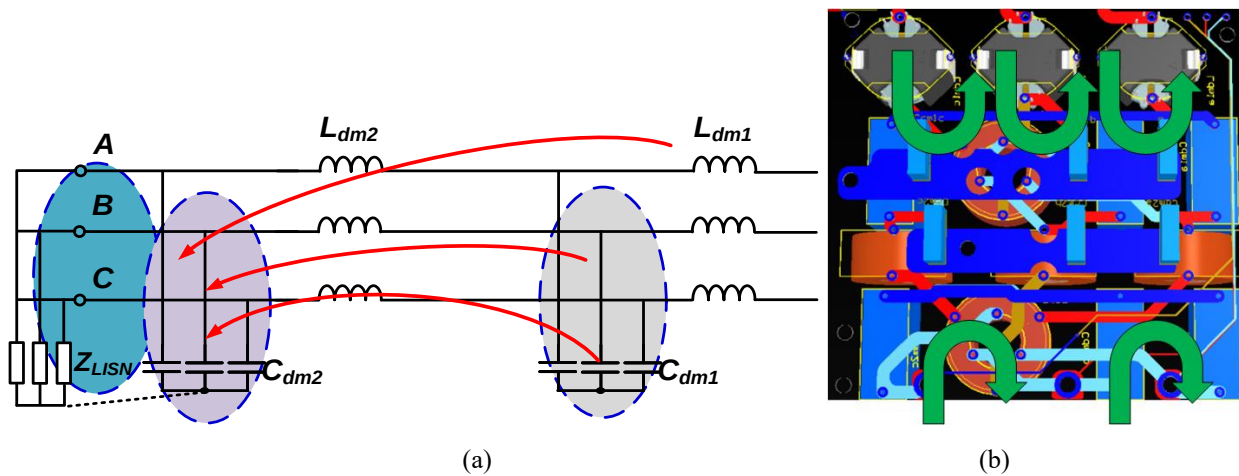


Fig. 6-35. Critical coupling paths in a three-phase DM filter. (a) Illustration in the circuit schematic. (b) Coupling loops shown on the filter PCB layout.

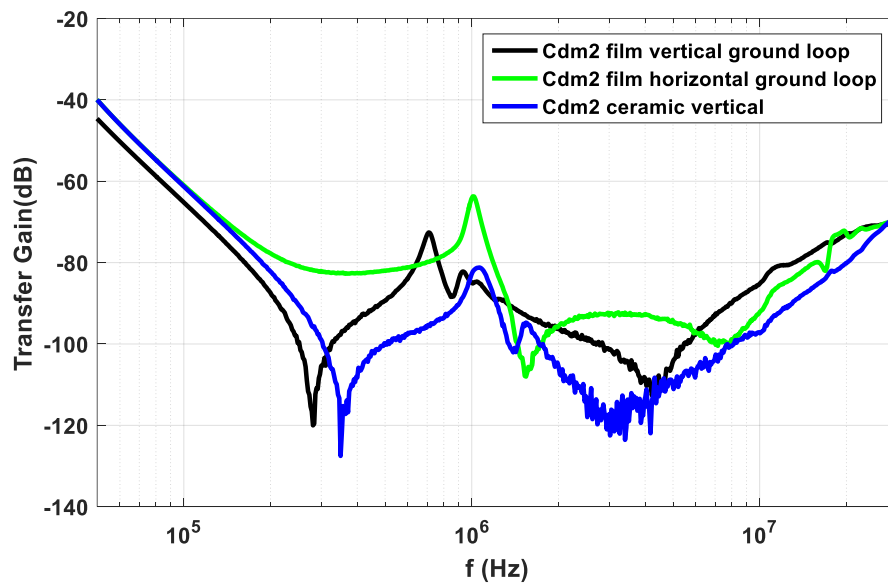


Fig. 6-36. Impact of the vertical neutral loop and filter size on transfer gain of the three-phase DM filter.

As a conclusion, both the capacitor size and two neutral vertical loops for both stages should also be minimized. A series of comparison tests on transfer gain is shown in Fig. 6-36. In the medium frequency range from 450 kHz to 1.5 MHz, where the most significant switching harmonics 1st, 2nd, and 3rd are covered, the minimized neutral vertical loop with ceramic capacitors ensures the highest attenuation. Compared to the transfer gain of the original filter design as shown in Fig. 6-37, the improvement is about 25 to 30 dB.

The vertical capacitor placement is however not very practical and mechanically robust if without a flexible PCB. Thus, the normal capacitor placement with vertical trace layout and minimized horizontal loop is proposed to obtain the similar performance. Instead of just shrinking the trace span of capacitor leads on one layer as literature suggested, the multi-layer layout is preferred. The semi-neutral-loop among three phases is minimized by folding the neutral trace back beneath the board area of per phase capacitor and then overlaying the three-phase power trace and neutral trace on four different layers. As a result, instead of an EE shape in the traditional three-phase capacitor layout, now it presents as an E shape structure, fully minimizing the semi-neutral-loop. The difference of the loop coupling effect can be evaluated from the loop inductance. In the meantime, stray inductance of the trace also matters. Therefore, the Kelvin connection should be used to minimize this type of inductance. Fig. 6-38 ~ Fig. 6-40 present the three different layout structures for three-phase DM filter capacitors, respectively. Both Q3D extraction analysis and experimental test are conducted to evaluate the total ESL across the line-line. The final scheme significantly reduces the ESL of the DM capacitors introduced by the layout.

Some other approaches can be also considered. One simple way is to change Y-connection of three DM capacitors to D-connection as shown in Fig. 6-41, so that the semi-loop formed by the

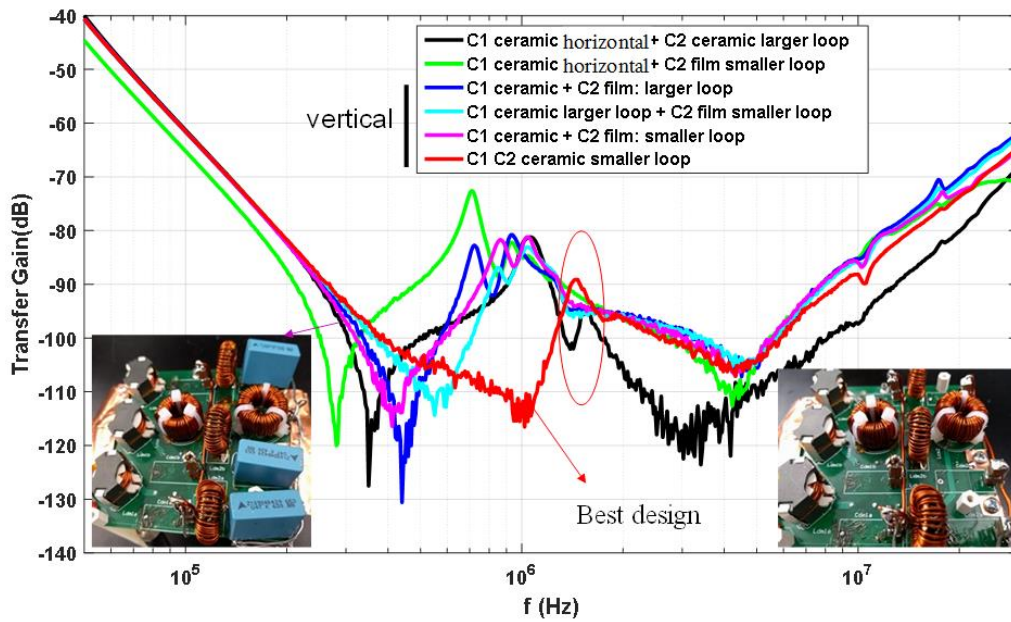


Fig. 6-37. Comparison of different neutral loop arrangements and filter size on transfer gain of three-phase DM filter.

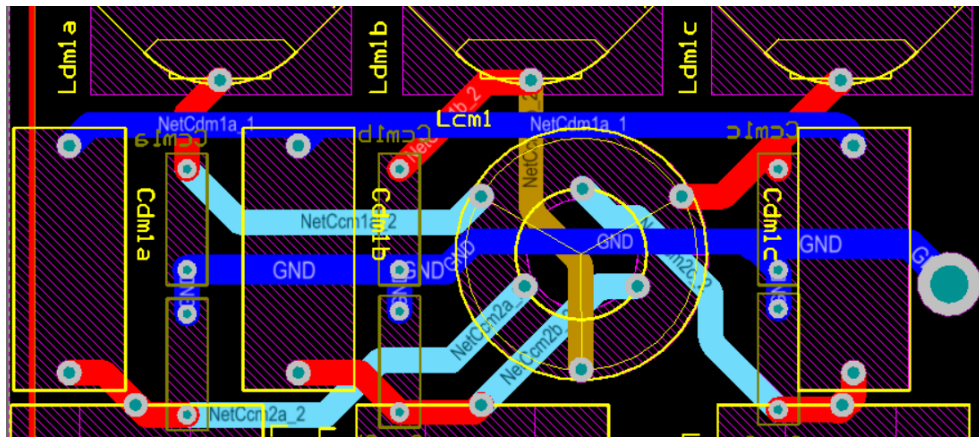


Fig. 6-38. A causal layout of three-phase DM capacitor and neutral line (large loop + Kelvin connection with less ESL from connection) results in L_{AB} 65 nH, L_{AC} 92 nH.

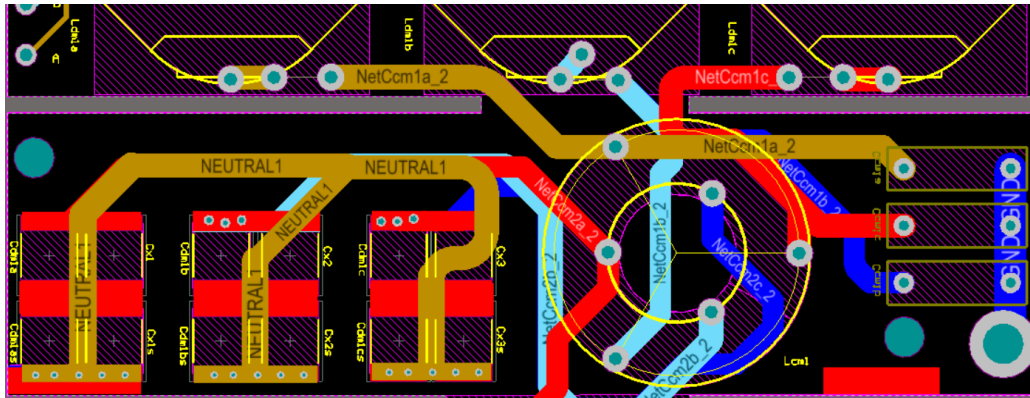


Fig. 6-39. The 2nd version layout of three-phase DM capacitor and neutral line with minimized loop yet no Kelvin connection results in L_{AB} 59 nH.

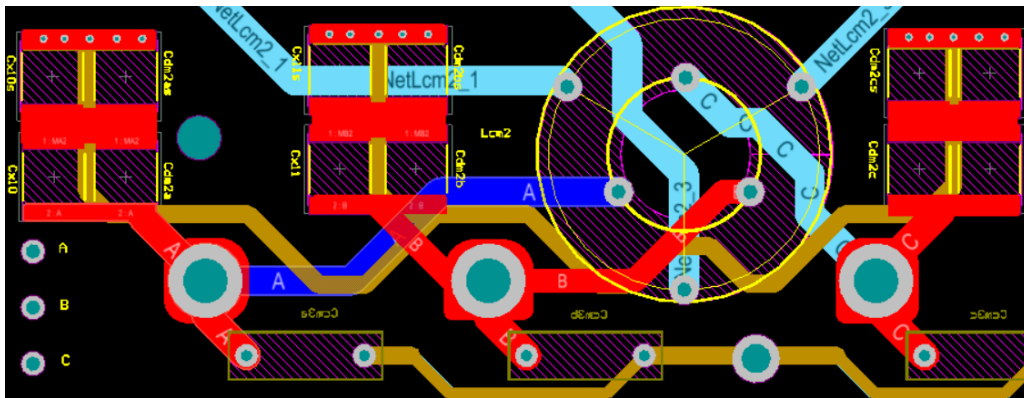


Fig. 6-40. The final layout of three-phase DM capacitors and neutral line (minimized loop + Kelvin connection) results in L_{AB} 32 nH.

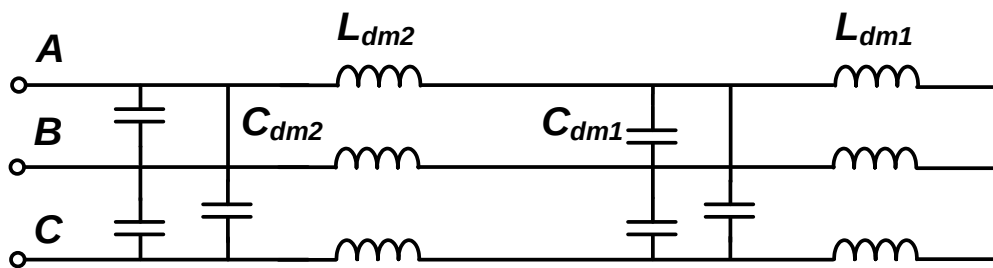


Fig. 6-41. Alternative D-connection of three-phase DM capacitors.

inter-phase neutral lines and DM capacitors can be eliminated. In this case, the output semi-loop formed by the inter-phase terminals and DM capacitors shall also be minimized, as previously analyzed. However, one concern for D-connection is that when maintaining the same equivalent phase-neutral impedance, the voltage stress of DM capacitors will be increased by 1.73X, although its current stress and capacitance are reduced to $1/3^{\text{rd}}$. In high voltage ac line filtering applications, this may greatly increase the capacitor size, ESL, and cost, especially for non 50/60 Hz (such as 800 Hz) applications.

6.5.3 Coupling mitigation through filter topology selection

From the results in Section 6.7.3, without using any special coupling mitigation methods, the CLLC filter itself shows better attenuation at HF, and not affected by capacitive coupling. However, this structure is sensitive to inductive coupling at HF as shown in Fig. 6-68 (c) in Section 6.7.3 and has low IL at LF. On the other hand, CLCL filter has poor IL at HF due to capacitive coupling, but it is immune to inductive coupling especially in low Z_s converters, and it also has much higher IL at LF. Whereas, LCLC filter, suffers the similar T-joint capacitive coupling effect as CLCL, but shows a bit better performance at HF due to the final filtering capacitor in addition to T-joint. However, once it ends with C, it will be vulnerable to inductive loop coupling.

Minimizing the loop area of power lines and ground loop is important, however, is limited by the clearance of power cables and mechanical layout space.

A simple solution that helps for CM filter is to add a minimal CM core around the three-phase cables at the output terminal of the filter, to form a single-turn CM choke and prevent noise at HF. Such an example is shown in Fig. 6-42. From the measurement result, 10 dB more attenuation is achieved.

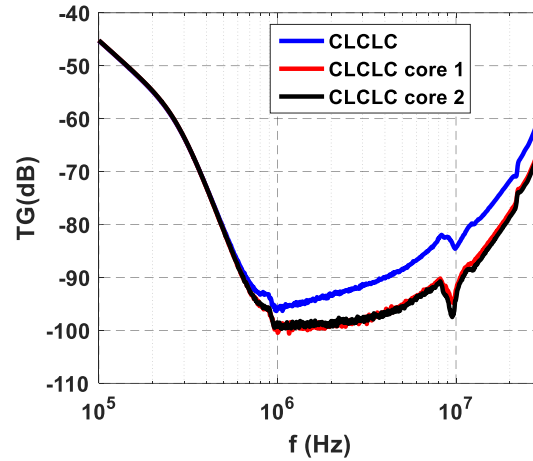


Fig. 6-42. Extra HF attenuation from 1-turn CM core on the output cable of a three-phase CM filter.

6.6 Parasitics mitigation methods

Once the dominant coupling effects are mitigated, the self-parasitics of filter components become the secondary must to be dealt with. In this section, parasitics reduction on inductors has been studied.

6.6.1 Winding scheme for parasitics reduction

6.6.1.1 Typical winding schemes

Based on literature review, four winding methods are often used in passive component design mainly for transformer, i.e. inverse winding (or U-type winding), direct winding (or foldback winding for non-toroidal core), section winding (or progressive winding), and bank winding, as shown in Fig. 6-43, respectively.

Different winding configurations have significantly different impacts on winding capacitance [256, 260-262, 340]. The inverse winding turns back the winding direction for the new layer and is referred to as the standard natural winding scheme. Direct winding follows the same winding direction for each layer, is often claimed with low capacitance owing to the voltage gradient

reduction between the ends of windings [256, 261, 340]. The section winding sectionalizes the total winding and adopts the inverse [340] or direct winding [260] per section. Since it reduces the voltage gradient between sections, winding capacitance is reduced at the penalty of less filling factor due to the existence of section walls of the bobbins [260]. The bank method is, in fact, an extreme condition of the progressive method C, where the section width is only one turn. It has the lowest potential difference between turns and between turn and cores. As a result, it shows the lowest winding capacitance and fully utilizes the winding window area. However, since each section has only one turn, with too many zigzag routes, it is difficult to fully achieve one-turn interval in practice, especially on a manually wound core. (A winding prototype using this scheme has experimented, however, resulting in a mix of single-layer design and two-layer bank winding design.) This method may be more promising in planer-transformer design via precisely controlled multilayer PCB winding.

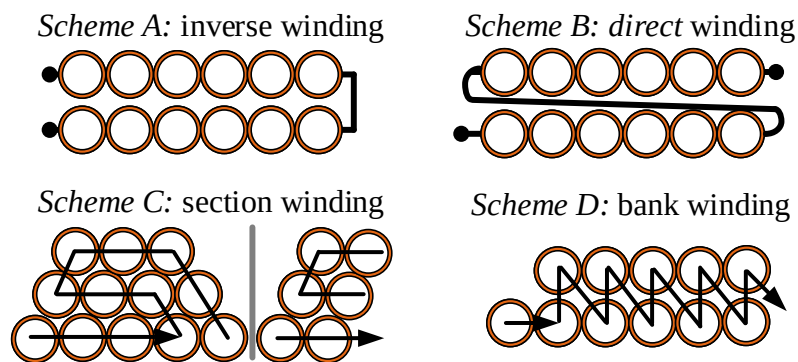


Fig. 6-43. Winding configurations of four commonly used winding schemes.

Prior studies have been mostly focusing on transformer winding schemes. When applying them to inductor design, the preferred schemes are method A and B, owing to their implementation simplicity. A comparison of two-layer winding capacitance is conducted in [256, 261, 262, 340], showing that the direct winding has lower capacitance than the inverse winding in the full two-

layer case owing to the slightly lower layer-layer capacitance. However, this conclusion does not consider the fractional layer winding design, and in fact, becomes not valid in this scenario.

Moreover, the capacitance contribution from different layers is not fully investigated. Reference [262] reviews the layer capacitance calculation methods and the multi-layer capacitance model based on the energy equivalent approach presented in [341, 342]. However, the first layer, i.e. layer-to-core capacitance, is not considered in the calculation, and the fractional layer model is included but not proper since it is projected directly based on the internal layer-layer capacitance. The first layer capacitance calculation is considered in [341, 342] and [261], however, it assumes that the start lead of the winding is connected to the screen/core, therefore not practical. The EPC calculation for an isolated core is difficult when using the energy equivalent principle. It is either improperly treated the same as the capacitance of single-layer winding with its end connected to the core/screen [342] or approximated as a plate capacitor [341] or ignored in the multi-layer winding case [342]. A more accurate EPC model considering the first layer and the outer fractional layer is therefore demanded.

In this work, the necessity of fractional-layer winding is firstly emphasized, and the two typical winding schemes in the fractional-layer winding scenario are modeled, compared in Section 6.6.1.2, and further extended to general capacitance calculation ranging smoothly from single layer to two layers. More importantly, a comprehensive EPC modeling approach considering the decoupled capacitances of layer-to-isolated core, layer-to-layer, and outer fractional layer is thereafter proposed in Section 6.6.2, with specific contributions on modeling layer-to-core and outer fractional layer capacitance. Experimental results of different winding schemes and core connection configurations are then presented in Section 6.6.3.

6.6.1.2 Proposed general winding scheme considering fractional layers

As discussed above, if multiple full layers are needed, the direct winding scheme B shows lower capacitance than the inverse winding scheme A. However, the prior work fails to consider the fractional winding case especially when the commonly favorable one-layer design cannot achieve the desired inductance, but two-layer causes overdesign and excessive EPC for a given core. Without enlarging the core size, through this work, it is found that a fractional winding design with $1 + \gamma$ layers, if wound properly, can mitigate self-parasitics, reduce the weight of filters, and introduce unnoticeable effect on HF impedance. More importantly, the method B that is better for 2-layer winding scheme induces more EPC in the majority range of the fractional winding design.

Another drive for the fractional winding design is that the ‘marginal utility’ of the extra fractional layer is quite high. As shown in (6-28), with a small extra γ winding ratio nearby 1 layer, e.g. 0.4, the increasing ratio of inductance is $(2+\gamma)*\gamma$, i.e. 96%, which enables the possibility of providing enough inductance without enlarging the core. As aforementioned, the key is to find a proper winding scheme which only induces negligible EPC increment.

$$\begin{cases} L \propto N^2 \\ \frac{L_{1+\gamma}}{L} = (1+\gamma)^2 / 1 = 1 + 2\gamma + \gamma^2 \end{cases} \quad (6-28)$$

In this report, EPC of the general winding layers considering the fractional is first analyzed using the energy equivalence concept [342] or the principle of virtual work (PVW) [343]. The general relation of the above two winding schemes A and B is firstly derived, through which a keen fraction point is found. And to achieve the best design, it is recommended to use winding method A instead of method B for $1 + \gamma$ layers. And the fractional part γ should be lower than 0.4 to achieve low EPC with only $1/20^{\text{th}}$ of the standalone full layer-layer capacitance $C_{ll,0}$. Since for most of EMI inductor design, 2 layers above windings are not suitable as will explained section

6.6.2, the analysis in this paper is focusing on the $1+\gamma$ layer, but it can be extended easily to more layers for general applications.

EPC analysis for method A, i.e. inverse method, is presented first. For the geometry of a core and winding illustrated in Fig. 6-44 (a), voltage potential vs winding x-dimension curve is firstly defined in Fig. 6-44 (b). To ease the analysis, the center is put at the end of the first layer and the potential curve of the secondary winding is mirrored to the vertical axis. And x and γ reflect the percentage of the winding length vs the circumference of one layer.

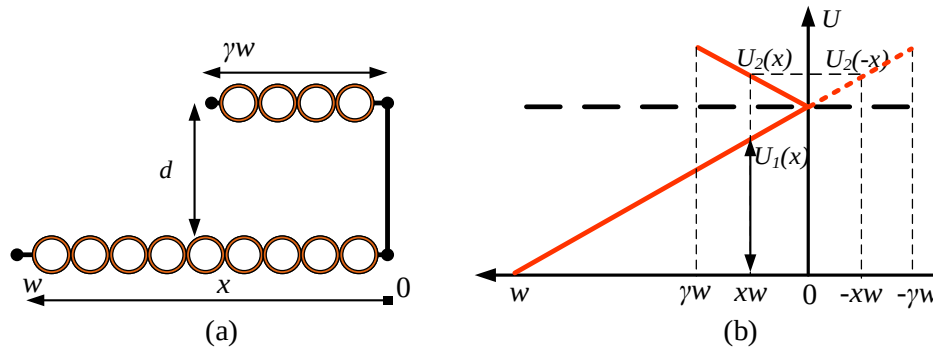


Fig. 6-44. Inverse winding scheme for $1+\gamma$ layer. (a) winding configuration. (b) voltage distribution.

From the mirrored v-x curve, it is easily to obtain the potential of the two layers at a location of x ,

$$U_2(x) = \frac{U(1+x)}{(1+\gamma)} \quad (6-29)$$

$$U_1(x) = \frac{U(1-x)}{(1+\gamma)} \quad (6-30)$$

which yields,

$$\Delta U(x) = U_2(x) - U_1(x) = \frac{2x}{(1+\gamma)} U \quad (6-31)$$

And

$$E(x) = \frac{\Delta U(x)}{d} = \frac{2xU}{(1+\gamma)d} \quad (6-32)$$

From the principle of virtual work (PVW) used centuries years ago in potential energy, kinetic and mechanic energy, in further the energy equivalent principle, the energy stored in the filed diffused in the layer-layer winding space can be presented in two forms, i.e. the energy modeled by the equivalent layer-layer capacitance projected to the whole voltage U and the accumulated energy within the layer-layer.

$$\begin{aligned}
 W &= \frac{1}{2} C_{eq,A} U^2 \\
 &= \frac{1}{2} \int_{dV} \epsilon E^2(x) dV \xrightarrow{dV=l\omega d \cdot dx} = \frac{1}{2} \int_0^\gamma \epsilon E^2(x) dx = \frac{1}{2} \frac{\epsilon l \omega}{d} \frac{4\gamma^3}{3(1+\gamma)^2} U^2
 \end{aligned} \tag{6-33}$$

Also, considering that the distance d is far smaller than the width of the winding (roughly, the perimeter of the core), the standalone or disconnected two full layer windings can be treated as a parallel plate capacitor formed by the cylindrical surface. Thus, the standalone layer-layer capacitance C_{ll} can be approximately calculated as

$$C_{ll} = \frac{\epsilon_0 \epsilon_r l \omega}{d_{ll}} \tag{6-34}$$

Therefore, the layer-layer capacitance of $1+\gamma$ layers using method A is

$$C_A = C_{eq,A} = \frac{4r^3}{3(1+\gamma)^2} C_{ll} \tag{6-35}$$

In the extreme case, if using full two-layer design, i.e. $\gamma=1$, the layer-layer capacitance is deduced to (6-36), matching the formula from literature [261, 341, 342].

$$C_A = \frac{1}{3} C_{ll} \tag{6-36}$$

For method B, a similar analysis can be made. As shown in Fig. 6-45, instead of mirroring the v-x curve of the second layer winding, a shift rightward is made to accommodate the different winding connection in method B.

The voltage potential on the 2nd layer is the same as the above, and the potential of the first layer is

$$U_1(x) = \frac{x}{(1+\gamma)} U \quad (6-37)$$

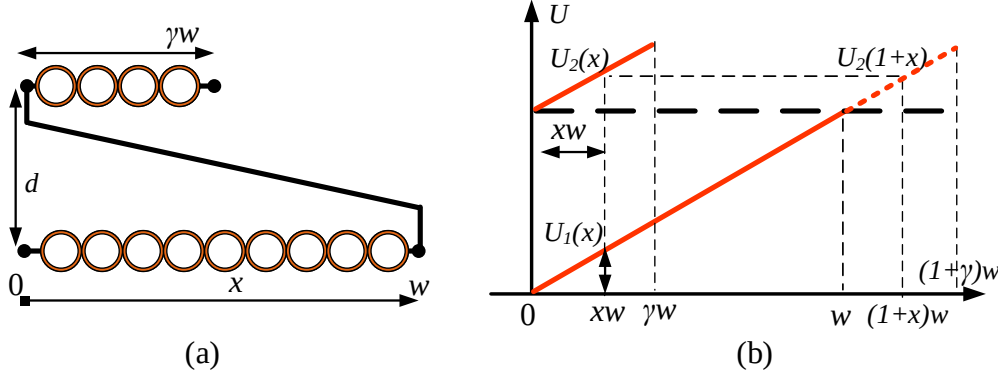


Fig. 6-45. Direct winding scheme for $1+\gamma$ layer. (a) winding configuration. (b) voltage distribution.

And E field between the two-layer winding becomes a constant in this case.

$$E(x) = \frac{\Delta U(x)}{d} = \frac{U}{(1+\gamma)d} \quad (6-38)$$

As a result,

$$\begin{aligned} W &= \frac{1}{2} C_{eq,B} U^2 \\ &= \frac{1}{2} \int_{dV} \epsilon E^2(x) dV \xrightarrow{dV=l\omega d \cdot dx} = \frac{1}{2} \int_0^\gamma \epsilon E^2(x) dx = \frac{1}{2} \frac{\epsilon l \omega}{d} \frac{\gamma}{(1+\gamma)^2} U^2 \end{aligned} \quad (6-39)$$

Therefore, the layer-layer capacitance of $1+\gamma$ layers from method B is

$$C_B = C_{eq,B} = \frac{\gamma}{(1+\gamma)^2} C_{ll} \quad (6-40)$$

Again, in the case of full two-layer design, i.e. $\gamma=1$, the layer-layer capacitance becomes (6-41), the same as reported in the literature [261, 262, 341, 342].

$$C_B = \frac{1}{4} C_{ll} \quad (6-41)$$

Then, it is interesting to compare the capacitance of the two methods. Since the first layer winding-to-core capacitance are the same for both methods and lower than the layer-layer capacitance, only the layer-layer capacitance is compared here. The evaluation of the first layer capacitance will be provided in the next section. The ratio of C_A/C_B is given by

$$\frac{C_A}{C_B} = \frac{4}{3} \gamma^2 \quad (0 \leq \gamma \leq 1) . \quad (6-42)$$

Therefore, a keen point exists. If $\gamma < \sqrt{3}/2$, $C_A < C_B$. Because of the γ^2 ratio, the smaller γ is, the lower C_A becomes. If $\gamma > \sqrt{3}/2$, $C_A > C_B$.

Fig. 6-46 (a) plots the layer-layer capacitance of both methods vs different γ . And Fig. 6-46 (b) gives the ratio curve. It is clear in the majority range, C_A is smaller than C_B . And when γ is near zero, although both C_A and C_B are close to zero, C_A can be hundreds of times smaller than C_B , significantly reducing the EPC of the inductor and push its self-resonance to HF end.

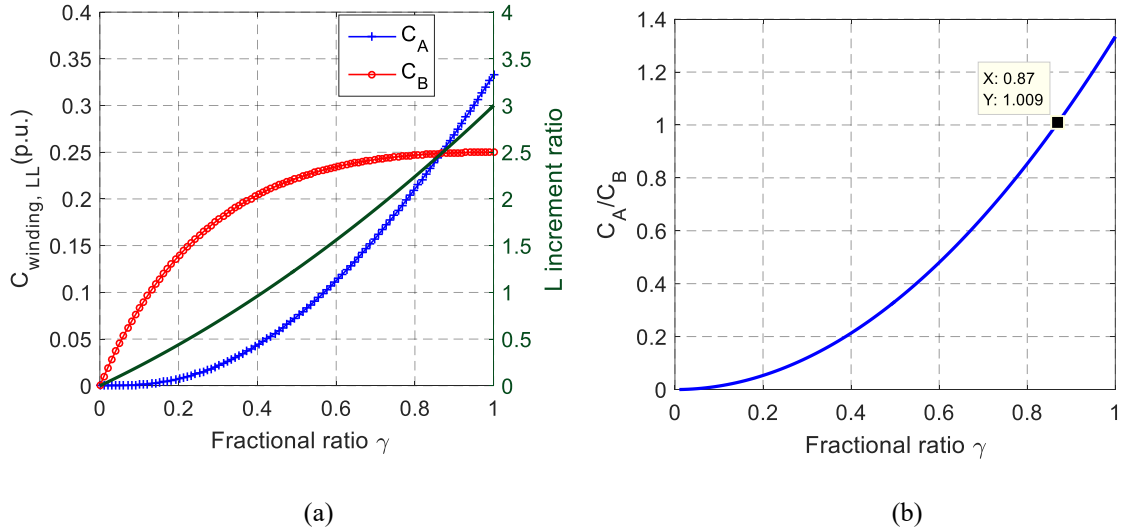


Fig. 6-46. EPC of the fractional layer for $1+\gamma$ layer. (a) EPC of two winding schemes and inductance vs fractional ratio. (b) EPC comparison of two winding schemes vs fractional ratio.

To reduce the impact of layer-to-layer capacitance but also fully utilize a given core size to achieve high power density, it is therefore recommended to wind an inductor with $1+\gamma$ layer using direct winding scheme A. The ratio γ should be determined considering the trade-off between inductance value enhancement and EPC reduction, e.g., if $\gamma < 0.4$, C_{ll} impact can be reduced to 5% below whereas filter inductance will be increased less than 96%. On the other hand, even when γ

is as high as 0.8, C_A is only $0.2C_{ll}$, still smaller than $0.25C_{ll}$ using the winding method B or smaller than a two-layer full winding design with the winding method B.

Generally speaking, method A is more feasible and efficient in terms of both core utilization and winding EPC reduction. This fulfills the incomplete understanding of the inductor winding schemes in the past.

As also observed from Fig. 6-45 and Fig. 6-44, the main reason causing the EPC difference between the two methods for $1+\gamma$ layer is that the method A has much lower layer-layer voltage difference (when $\gamma < 0.867$) which is linearly increased from zero, whereas the method B has the constant maximum voltage difference U . In the end, the layer-layer capacitance is determined by the winding voltage distribution, and the lower potential difference between layers ensures lower layer-layer EPC.

When extending the above winding scheme to a more general case with multiple windings, the preferred winding scheme is, therefore, applying the direct winding for the inner full layers and the inverse winding for the outer partial layer, due to their lower layer capacitances, respectively.

6.6.2 Generic decoupled layer capacitance model

To further gauge the reduction of layer capacitance on the total EPC, the first layer capacitance and layer-layer capacitance are explored, leading to the final comprehensive EPC model.

6.6.2.1 Review of EPC modeling

In-depth modeling work has been done on modeling winding capacitance of transformers and/or inductors in literature [223, 225, 226, 256, 257, 260, 262, 341-343], among which, [223] focuses on the individual turn-turn or turn-core capacitance, [262] considers mainly the layer-layer capacitance, [225, 226, 256, 257] give the overall capacitance by doing a step by step analytical

modeling, and [341, 342] present the modeling and calculation for different types of windings. And a review is also found in [262]. In general, two types of methods have been built for calculation of the stray capacitance, i.e. geometrical method based on the physical properties and dimensions [223, 225, 226, 256, 257], and the energy-based equivalence method [262, 341, 342], respectively.

To ensure the HF performance of EMI inductors, one-layer or two-layer is often at most. The turn-turn capacitance and turn-core capacitance cannot be ignored and are dominant in the single-layer case.

Reviewing the geometrical method, the single-layer capacitance is often modeled as the capacitance network forming by the series turn-turn C_{tt} and parallel turn-core capacitance C_{tc} [225].

The turn-turn capacitance can be derived either from Koch's method [344] or Massarini's method [225], showing slight differences in the shape of the basic cell of the turn-turn geometry and the exact path of electric flux line emitted from wires between air gaps of two adjacent turns. However, the above methods stem from the basic turn cell in a multi-layer winding structure, with $-\pi/3$ to $\pi/3$ angle-span for each turn cell. For the single-layer winding, a slight modification is made in [223, 226] with cell angle spanned from $-\pi/2$ to $\pi/2$. A comparison of some of the models is also described in [262].

The turn-to-core capacitance is derived in detail in [223]. However, it contains three complicated integration terms and is also not further linked with C_{tt} which is potentially useful for layer capacitance calculation. On the other hand, [225] simplifies the calculation as

$$C_{tc} = 2C_{tt} \quad (6-43)$$

assuming turn-to-core coating is half of the turn-to-turn coating and ignoring the extra air gap between turn-to-core and turn-to-turn.

Therefore, from this simplified model, the equivalent single-layer capacitance is derived as the impedance combination of the series C_{tt} and parallel C_{tc} capacitor network,

$$C_{l1,geo}(n) = \frac{C_{tt}}{2 + \frac{C_{tt}}{C_{l1,geo}(n-2)}} + C_{tt} \quad (6-44)$$

And it converges rapidly to

$$C_{l1,geo} = 1.366C_{tt}, \quad \text{for layer number } n \geq 10. \quad (6-45)$$

In a more general sense, if defining the ratio of C_{tc}/C_{tt} as α , the single layer capacitance becomes [257],

$$C_{l1,geo}(n) = \frac{C_{l1,geo}(n-2) \cdot C_{tt}/2}{C_{l1,geo}(n-2) + C_{tt}/2} + C_{tt}/2 = \frac{C_{tt}}{2 + \frac{C_{tt}}{C_{l1,geo}(n-2)}} + \frac{\alpha}{2} C_{tt} \quad (6-46)$$

Which converges to (6-47) faster if α is high,

$$C_{l1,geo} = \frac{\alpha C_{tt}}{4} \left(1 + \sqrt{1 + 4/\alpha} \right) = \frac{C_{tc}}{4} \left(1 + \sqrt{1 + 4/\alpha} \right) \quad (6-47)$$

From this scheme, it is also able to obtain the two-layer capacitance as

$$C_{l1,geo} = 1.83C_{tt}, \quad \text{for } n \geq 10 \text{ and } \alpha=2. \quad (6-48)$$

It also derives that three layers have lower EPC. However, as the proximity effect will be higher, leading to more ac loss, multi-layer is not recommended in high frequency applications [225]. Moreover, leakage flux could also be higher in multi-layer design, leading to more coupling issues [345]. In addition, the above calculation does not consider any nonadjacent turn-turn capacitive coupling. For tightly wound windings with many turns or multi-layers, it has been reported empirically the total EPC can be increased as a function of turn numbers [256], or 100% higher [258] because of the nonadjacent turn-turn coupling.

6.6.2.2 Decoupled layer capacitance model

Theoretically, the geometric method can be applied to the fractional winding calculation to evaluate the capacitance of the first layer as well as the whole capacitance. However, the main

issue with this method is that only the total capacitance can be obtained by solving the capacitance network. The turn-turn and turn-core impedance are coupled together, and the capacitance of each layer cannot be distinguished, either. In addition, in the partial 2nd layer case as shown in Fig. 6-47, the lumped C_{tt} - C_{tc} network becomes asymmetric and more complex than the full layer case. Therefore, it is inconvenient for the study here and not helpful in the evaluation of the EPCs of different layers in a general sense.

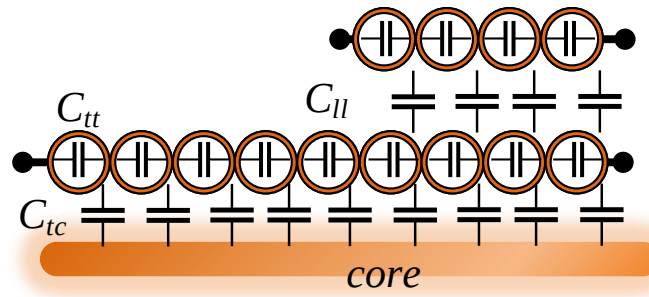


Fig. 6-47. Capacitor network of the partial layer winding.

To evaluate the first layer capacitance, the other method that equating the total energy stored in the total winding to the sum of the energy stored in each layer is adopted as given in (21). Although the original purpose of this method is to calculate the total winding capacitance, it is useful to find the relationship among the layer capacitance and to extract each layer's equivalent capacitance.

$$W_{tot} = \frac{1}{2} C_{eq} U^2 = \sum_{i=1}^{N_{layer}} \frac{1}{2} C_{i,i-1} U_{i,i-1}^2 \quad (6-49)$$

where $C_{i,i-1}$ is the equivalent capacitance between layer i and $i-1$.

Considering the linear relation between voltage difference of two adjacent layers and the turn numbers of each layer, the equivalent total capacitance in the full layer design case can be regarded as the sum of N_{layer} parallel layer capacitances projected to the whole winding, as derived in (6-50),

$$C_{eq} = \sum_{i=1}^{N_{layer}} C_{i,i-1} \frac{U_{i,i-1}^2}{U^2} = C_{1,0} \frac{U_{1,0}^2}{U^2} + \sum_{i=2}^{N_{layer}} C_{i,i-1} \frac{(n_{i-1} + n_i)^2}{\left(\sum_{1}^{N_{layer}} n_i\right)^2} = C_{1,0}' + \sum_{i=2}^{N_{layer}} C_{i,i-1}' \quad (6-50)$$

From this general capacitance equation of the full layer design, other useful formula can also be obtained.

If each layer has the even turns,

$$C_{eq} = C_{1,0} \frac{U_{1,0}^2}{U^2} + \sum_{i=2}^{N_{layer}} C_{i,i-1} \frac{4}{N_{layer}^2} \quad (6-51)$$

In further, if the same winding scheme is applied for all the layer, all the interlayer capacitance above the first layer will be the same C_{layer} based on the energy equivalence principle, yielding a well-known formula [262, 341, 342] except the first layer-to-core capacitance.

$$C_{eq} = C_{1,0} \frac{U_{1,0}^2}{U^2} + C_{layer} \frac{4(N_{layer} - 1)}{N_{layer}^2} \quad (6-52)$$

In fact, this formula can be used to guide the calculation of fraction winding on the outer layer. In this case, the top layer term has to be considered individually using the method proposed in Section 6.6.1.2, because the energy in this layer is only stored in the overlapped fractional winding space between the top layer and its beneath layer.

$$\begin{aligned} C_{eq} &= C_{1,0} \frac{U_{1,0}^2}{U^2} + \sum_{i=2}^{N_{layer}-1} C_{i,i-1} \frac{(n_{i-1} + n_i)^2}{\left(\sum_{1}^{N_{layer}} n_i\right)^2} + C_{fraction} \frac{n_i^2}{\left(\sum_{1}^{N_{layer}} n_i\right)^2} \\ &= C_{1,0}' + \sum_{i=2}^{N_{layer}-1} C_{i,i-1}' + C_{fraction}' \end{aligned} \quad (6-53)$$

Therefore, all layer capacitances are decoupled and their relationship with the total C_{eq} become clear. And a generic lumped model for an inductor can now be illustrated in Fig. 6-48. Yet, the remaining unique layer capacitance is at the first layer. Since the core surface is often coated and isolated from the winding. Therefore, its potential is unknown from the given input voltage U . Thus, the voltage potential difference $U_{1,0}$ between the core and the first layer is not straightforward.

This becomes the biggest limitation of this energy-based approach, requiring following further efforts to derive the first layer capacitance.

To evaluate the first layer capacitance under such circumstance, the isolation voltage of turn-to-core is further explored, and an analytical formula is finally derived as well as its boundary. The general approach using energy equivalence principle is again applied here for the first layer, also referred to as the arbitrary winding method.

In Fig. 6-49, the voltage difference between three nodes is marked, using the core surface as the zero-potential reference.

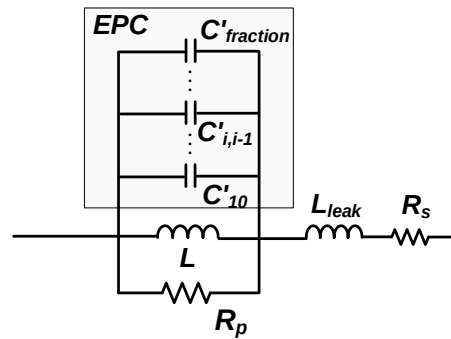


Fig. 6-48. A general parasitic model of an inductor consisting of different projected parallel winding capacitances (fully decoupled) from layer-to-core, layer-layer, and outer fractional layer.

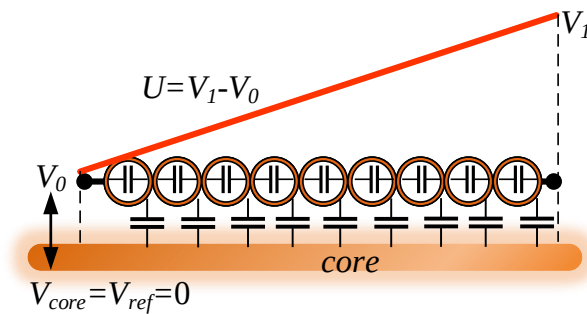


Fig. 6-49. Voltage potential distribution between the single-layer winding and the core.

Based on the energy principle, it is easy to obtain

$$C_{1,0}' = \frac{C_{lc,plate}}{3} \frac{V_0^2 + V_0V_1 + V_1^2}{U^2} = \frac{C_{lc,plate}}{3} \frac{V_0^2 + V_0V_1 + V_1^2}{(V_1 - V_0)^2} \quad (6-54)$$

$$U_{1,0} = \sqrt{V_0^2 + V_0 V_1 + V_1^2} \quad (6-55)$$

where $C_{cl,plate}$ is the capacitance based on the geometry of the core and winding using the parallel plate capacitor model, which is similar to the C_{ll} calculation in section 6.6.1.2.

$$C_{lc,plate} = \frac{\epsilon_0 \epsilon_r A}{d_{lc}} \quad (6-56)$$

Noticing that since V_0 is an unknown floated voltage, the capacitance value become undetermined. In the literature [341, 342], probably to avoid the issue, the starting end of the winding in the first layer is connected to the core or a shield or a screen. For a single-layer winding, it leads to

$$C_{1,0} = C_{1,0}' = \frac{C_{lc,plate}}{3} \frac{0 + 0_1 + V_1^2}{U^2} = \frac{C_{lc,plate}}{3} \quad (6-57)$$

In fact, in this connected case, the general capacitance formula (6-50) of multi-layer full winding can also be rewritten as (6-58), since $U_{1,0}$ now can be directly derived from the turn ratio.

$$C_{eq} = \sum_{i=1}^{N_{layer}} C_{i,i-1} \frac{U_{i,i-1}^2}{U^2} = C_{1,0} \left(\frac{n_1}{\sum_{1}^{N_{layer}} n_i} \right)^2 + \sum_{i=2}^{N_{layer}} C_{i,i-1} \left(\frac{n_{i-1} + n_i}{\sum_{1}^{N_{layer}} n_i} \right)^2 \quad (6-58)$$

From (6-58), one can derive the two-layer winding capacitance the same as reported in [261, 341, 342] for both the direct and inverse winding schemes, which also means these formulas in [261] are only valid for the winding design with core connected.

The core connected design is perhaps feasible for transformer windings where the low voltage terminal may have a fixed voltage potential and the metal core may be electrically connected, or a screen between core and winding exists and can be connected to the winding terminal [342]. However, for power electronic inductor design in series with a high frequency (HF) switching circuit and using isolated cores, these formulas are not feasible.

Anyway, in the core disconnected case, the single-layer capacitance (in which $V_1 - V_0 = U$) can be expressed as a function of the voltage difference V_0 ,

$$C_{1,0}' = \frac{C_{lc,plate}}{3} \frac{V_0^2 + V_0 V_1 + V_1^2}{U^2} = \frac{C_{lc,plate}}{3} \left(1 + 3 \frac{V_0^2 + V_0 U}{U^2} \right) \quad (6-59)$$

Since V_0 is unknown, the EPC of a single-layer winding without a screen is approximated to be the same as the case with a screen connected to low-potential end in [342]. And the layer-to-core capacitance is further ignored in the multi-layer case [262, 342]. In [341], this is also approximated as a $C_{lc,plate}$. Unfortunately, none of the work has accurately modeled and calculated this layer-to-core capacitance. Therefore, a novel approach with physical insight is proposed in this paper.

Noticing one basic geometric feature that the isolated core is always wrapped by the first layer winding, therefore the core potential should be within the start and end potential of the first layer winding. In fact, the potential difference V_0 is determined by impedance distribution between the winding impedance and the parasitic capacitive impedance of the turn-to-core, on which the geometrical method is based. Thus, a very important and useful boundary condition can be made for V_0 ,

$$k = \frac{V_0}{V_1 - V_0} \in [-1, 0] \quad (6-60)$$

which yields to

$$C_{1,0}' = \frac{C_{lc,plate}}{3} (3k^2 + 3k + 1) = \frac{C_{lc,plate}}{3} f(k) \in \frac{C_{lc,plate}}{3} \cdot \left[\frac{1}{4}, 1 \right] \quad (6-61)$$

where $f(k)$ reaches the lowest value $\frac{1}{4}$ at $k = -0.5$, and the peak at $k = 0$ and -1 , as shown in Fig. 6-50.

This means that if the potential gradient of the core surface is half of the winding voltage, the EPC will be lowest, and if it shares the same level as the start or the end of the winding, the EPC will be the highest. This conclusion is easy to understand from the energy perspective, like the inequality of arithmetic and geometric means. It also indicates the EPC, in fact, is maximized in

the case with winding start connected to the core. In further, as found from the experimental test in Section 6.6.2, winding EPC for the commonly used isolated core is very close to the minimum value when $k=-0.5$, indicating that the potential of an isolated core is roughly at the mid-level potential across the two ends of the first-layer winding.

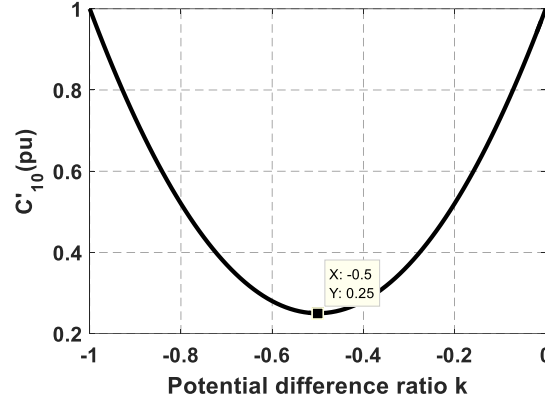


Fig. 6-50. Layer-to-core capacitance variation as a function of potential difference ratio k .

Till now, the general capacitance model in (6-53) for isolated core with N -layer winding design including the fractional layer case is fulfilled.

As a reminder, for a pure single-layer design of an inductor with the isolated core, the exact layer capacitance can be derived from the geometric model (6-45).

Now, for the fractional $1+\gamma$ layer design as illustrated in Fig. 6-51, the voltage difference across the end and the start of the first layer V_1-V_0 is lower than the total voltage U because of the turn ratio, as shown in (6-62). And k can be rearranged in (6-63).

$$V_1 - V_0 = \frac{1}{1+\gamma} U \quad (6-62)$$

$$k = \frac{V_0}{V_1 - V_0} = \frac{V_0}{U} (1+\gamma) \subseteq [-1 \ 0] \quad (6-63)$$

Applying the energy based principle again or per (6-53) and (6-63), one obtains

$$C_{eq} = C_{1,0} \frac{U_{1,0}^2}{U^2} + C_{fraction} \left(\frac{\gamma}{1+\gamma} \right)^2 = \frac{C_{lc,plate}}{3} \frac{V_0^2 + V_0 V_1 + V_1^2}{U^2} + C_{fraction} \left(\frac{\gamma}{1+\gamma} \right)^2 \quad (6-64)$$

The first term is the projected first layer capacitance with respect to the whole voltage, which can be expressed as (6-65) if substituting (6-63) into (6-64). Its relationship with the projected capacitance the when core is connected (i.e. V_0 is zero) can also be expressed in (38) by substituting k .

$$C_{1,0}' = \frac{C_{lc,plate}}{3} \frac{V_0^2 + V_0 V_1 + V_1^2}{U^2} = \frac{C_{lc,plate}}{3} \left(\frac{1}{(1+\gamma)^2} + 3 \frac{V_0^2 + V_0 U / (1+\gamma)}{U^2} \right) \quad (6-65)$$

$$C_{1,0}' = \frac{C_{lc,plate}}{3} \frac{3k^2 + 3k + 1}{(1+\gamma)^2} \subseteq \frac{C_{lc,plate}}{3} \frac{1}{(1+\gamma)^2} \cdot \begin{bmatrix} 1 & 1 \\ 4 & 1 \end{bmatrix} \quad (6-66)$$

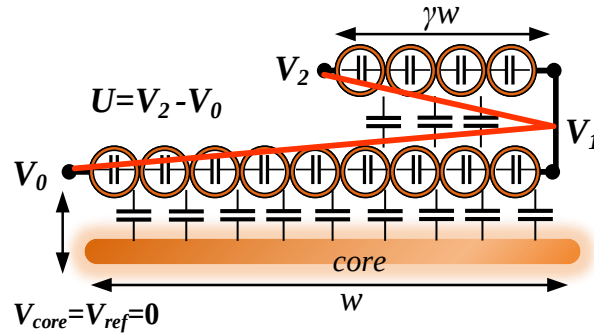


Fig. 6-51. Winding potential distribution of the $1+\gamma$ layer design with winding scheme A.

Similarly, reaches the lowest value when $k=-0.5$, i.e. when the core potential is the same as that of the middle turn in the first layer and reaches the highest value when $k=-1$ or 0 . And the derived formula is generally applicable for any γ within 0 and 1 , thus also valid for single-layer.

The second term of (6-64) is the projected fraction layer capacitance with respect to the whole voltage, which has been exactly derived in Section 6.6.1.2 considering two different winding schemes. And $C_{fraction}$, as an intermedium variable, is the equivalent capacitance with respect to the voltage difference of the fraction layer itself for a given winding scheme.

Therefore, in the fractional $1+\gamma$ layer design, the total capacitance for scheme A is

$$C_{eq} = C_{1,0}' + C_{2,0}' = \frac{C_{lc,plate}}{3} \frac{3k^2 + 3k + 1}{(1 + \gamma)^2} + \frac{4r^3}{3(1 + \gamma)^2} C_{ll} \quad (6-67)$$

For scheme B, it is

$$C_{eq} = C_{1,0}' + C_{2,0}' = \frac{C_{lc,plate}}{3} \frac{3k^2 + 3k + 1}{(1 + \gamma)^2} + \frac{\gamma}{(1 + \gamma)^2} C_{ll} \quad (6-68)$$

According to [341, 342], the effective permittivity of the dielectric may be taken as 3.5 if the winding is impregnated, and the effective distance between layer-to-layer or layer-to-core for unspaced winding are respectively

$$d_{ll} = \Delta_{ll} + 1.26d_o - 1.15d_i \quad (6-69)$$

$$d_{lc} = \Delta_{lc} + 0.5 \cdot (1.26d_o - 1.15d_i) \quad (6-70)$$

where d_o and d_e are the outer and inner wire diameters, respectively. Δ_{ll} is the layer and layer air gap which is usually small and may be ignored such as in [256], and Δ_{lc} is the distance between winding and core including the coating thickness.

The ratio of $C_{lc,plate}$ over C_{ll} can be derived based on (6-34) and (6-56),

$$\frac{C_{lc,plate}}{C_{ll}} = \frac{d_{ll}}{d_{lc}} \quad (6-71)$$

From the above results, the projected equivalent capacitance from the first layer is limited, if compared to the second layer using the winding scheme B, especially if core surface stays at the same potential as the mean of the first layer, i.e. $k = -0.5$, or core coating is much thicker than the wire coating, or insulation tape is inserted between core and winding both for EPC reduction and isolation enhancement. Therefore, the proper winding scheme which can reduce the layer capacitance plays an important role in minimizing the total EPC of an inductor.

6.6.3 Experimental verification

6.6.3.1 Fractional winding performance

Inductor prototypes made of powder core HF-080125-2 and heavy build solid magnet wire with AWG 20 was built to verify the presented scheme and analysis, as shown in Fig. 6-52. Because the core coating thickness of 0.38 mm is much higher than wire coating thickness 0.066mm, the EPC of the first layer is thus smaller than that of the second layer. This confirms the necessity of the presented work in reducing the layer capacitance.

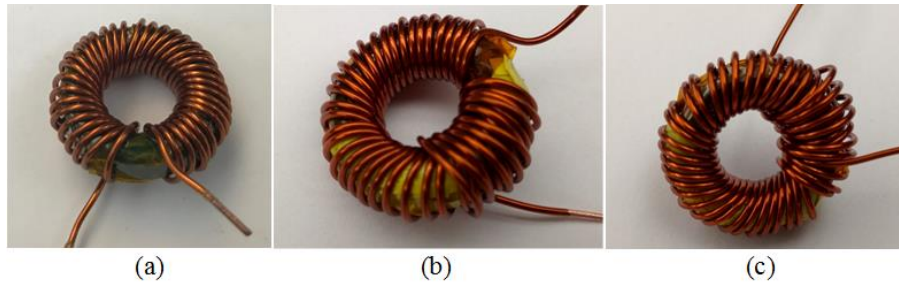
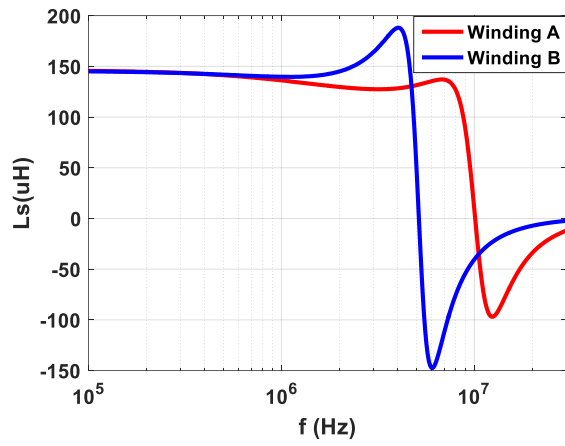


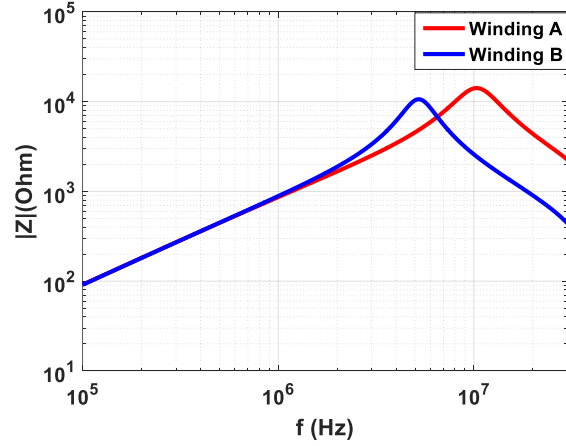
Fig. 6-52. Inductors with three winding schemes. (a) single-layer winding. (b) $1 + \gamma$ layer with winding scheme A. (c) $1 + \gamma$ layer with winding scheme B.

Two winding schemes A and B for $1 + \gamma$ layer design are compared, both with 39 turns on the first layer and the 8 turns on the second layer. As shown in Fig. 6-53, the inductances for both schemes are 141.6 μH at 450 kHz. The impedance curves show that winding scheme A has 10.48 MHz self-resonant frequency (SRF), while scheme B leads to 5.24 MHz SRF. Namely, the EPC of the inductor has been reduced to 1.63 pF, 4 times lower via scheme A, compared to scheme B.

The single-layer prototype using the same core and 38 turn wire has also been tested. Seen from Fig. 6-54, the inductance of the single layer winding is 94.55 μH and its SRF is 11.58 MHz. Compared to the fractional layer with winding scheme A, the resulted EPC of the single layer winding is 2 pF, which is much lower than the scheme B, but slightly higher than the proposed scheme A. This is because: 1) the projected capacitance from the second layer is dominant in

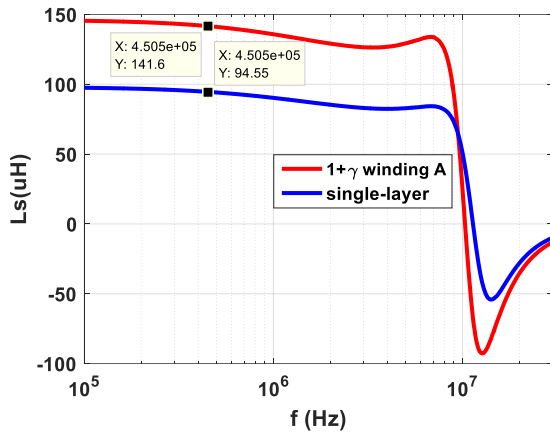


(a)

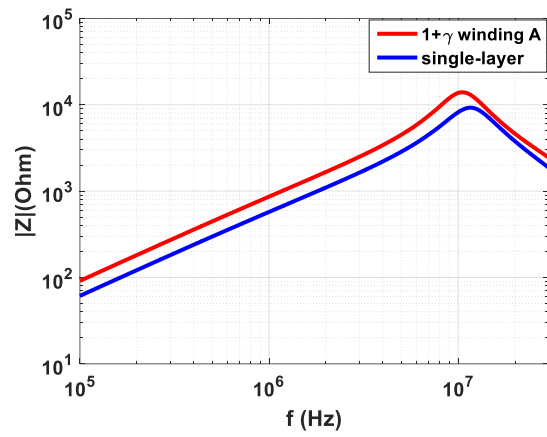


(b)

Fig. 6-53. Comparison of two winding schemes for $1+\gamma$ layer inductor. (a) Inductance. (b) Impedance.



(a)



(b)

Fig. 6-54. Comparison of single-layer and $1+\gamma$ layer winding with winding scheme A. (a) Inductance. (b) Impedance.

winding scheme B due to the thicker core coating as mentioned before; 2) the capacitance is reduced by hundred times if using scheme A with the fraction ratio $8/39=0.2$, as shown in Fig. 6-46, thus becomes negligible; 3) the projected capacitance from the first layer in scheme A (6-67) is lower than that of the single-layer winding, by a factor of $1/(1+8/39)^2=0.69$. The result shows that the fractional winding design using scheme A can accomplish higher inductance but even lower EPC, compared to single-layer design for a given core size.

6.6.3.2 Verification of layer-to-core capacitance model

To verify the proposed modeling approach for layer-to-core capacitance, three benchtop tests of single-layer winding on a powder core HF-080125-2 are compared. As shown in Fig. 6-55, in configuration (a) the core is isolated from the winding, in (b) the first turn is connected the core metal surface by peeling the coating, i.e. $k=0$, and in (c) the middle layer is connected to the core metal surface, i.e. $k=-0.5$.

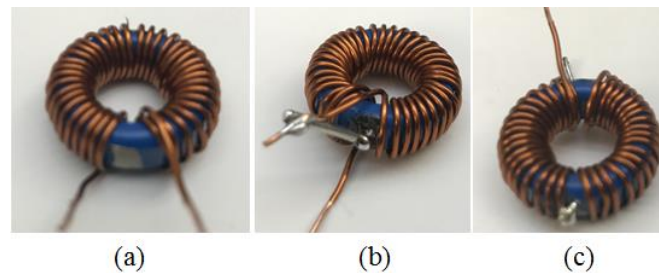


Fig. 6-55. Comparison of single-layer with different core configurations. (a) Isolated core. (b) Core connected to winding lead, $k=0$ or $k=-1$. (c). Core connected to middle turn of the winding, $k=-0.5$.

The measured impedance results from Fig. 6-56 clearly show that case (b) has the lowest SRF 5.68 MHz thus highest EPC, and case (c) has the highest SRF 11.9 MHz and lowest EPC, whereas the isolated case (a) has SRF 11.7 MHz, similar to case (c). The EPCs of three cases are 1.84 pF, 7.82 pF, and 1.78 pF, respectively. And their measured ratios are 1.03:4.38:1. Considering the

inevitable minor error in the measurement fixture and instrument, three EPCs are close to 2 pF, 8 pF and 2 pF, with the approximated ratio at 1:4:1. These results match well with the predicted ratio from the proposed model, confirming the proposed assumption on core potential and the resulting winding capacitance model. It proves the conclusion that connecting winding end to core surface results in the highest layer-to-core EPC, four times the minimum value when core potential is the medium potential across the first layer winding. It also reveals that the isolated core-winding approach as a common industrial practice, actually has roughly medium potential across the first layer winding, already leading to the minimum layer-to-core EPC.

To further verify the conclusion, repeated tests on another inductor made of powder core HF-090060-2 as shown in Fig. 6-57 are also conducted, focusing on the isolated core case (a) and the case (b) with core connected to the winding lead.

The results are shown in Fig. 6-58. The inductance of the two cases are slightly different, 26.66 μ H for the $k=0$ case and 26.42 μ H for the isolated case both at 10 kHz. The calculated EPCs from inductance and SRF are 9.6 pF and 2.4 pF, respectively. This again verifies the above conclusions.

6.7 Insertion loss prediction of EMI filters in actual converter system

Based on the previous analysis, for an actual EMI filter installed in the actual converter system, many factors can degrade its ideal performance assuming ideal and linear components. Self-parasitics change the HF behaviors of L and C once an inductor or capacitor is physically implemented. Inductive and capacitive couplings occur once the PCB layout is developed and filter components are populated. Worse more, the material properties of the magnetic core itself are nonlinear functions of frequency and dc bias. Layout, component geometry, placement, and material, etc. are all difficult to model and predict, requiring sophisticated 3D model and

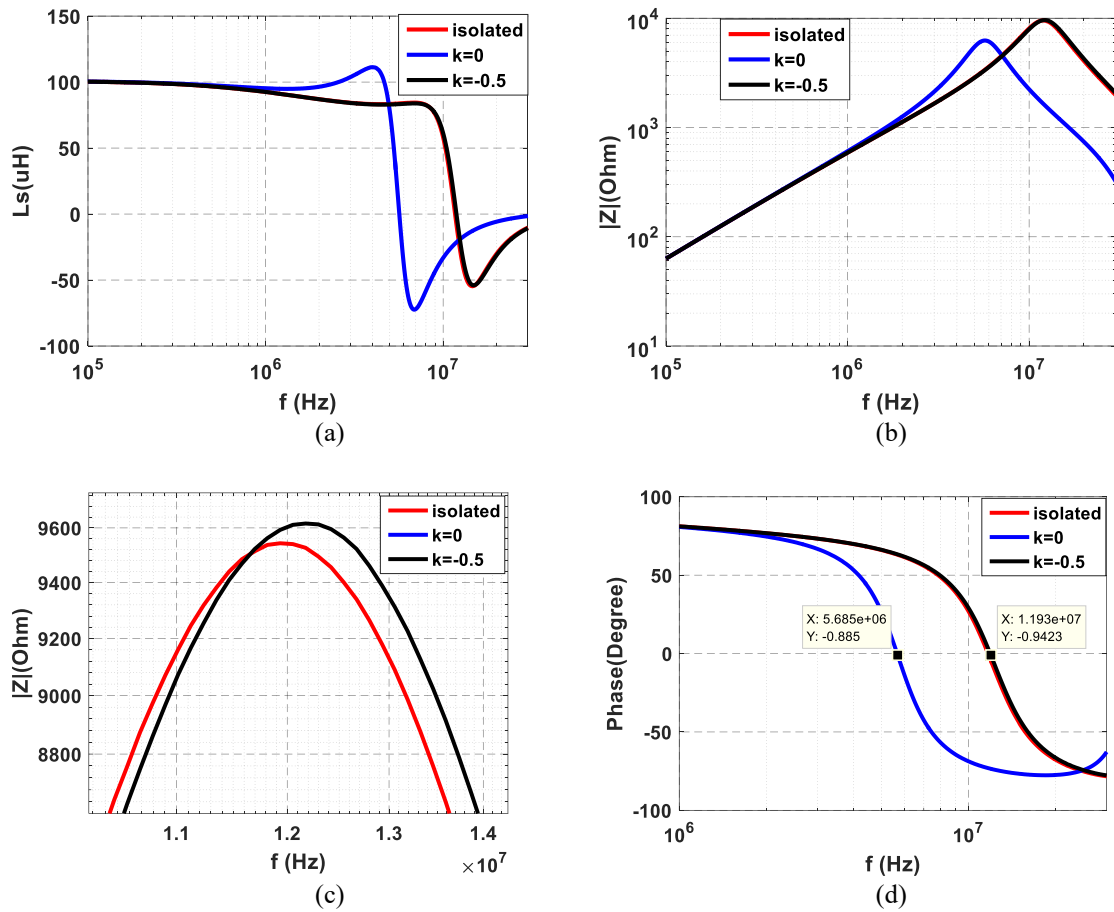


Fig. 6-56. Impedance comparison of the three core configurations. (a) Inductance curves. (b). Impedance curves (c) Zoomed-in impedance curves. (d) Phase curves.

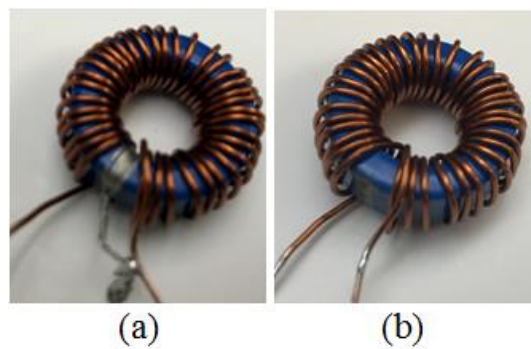


Fig. 6-57. Comparison of single-layer with two different core configurations. (a) Isolated core. (b) Core connected to winding lead, $k=0$ or $k=-1$.

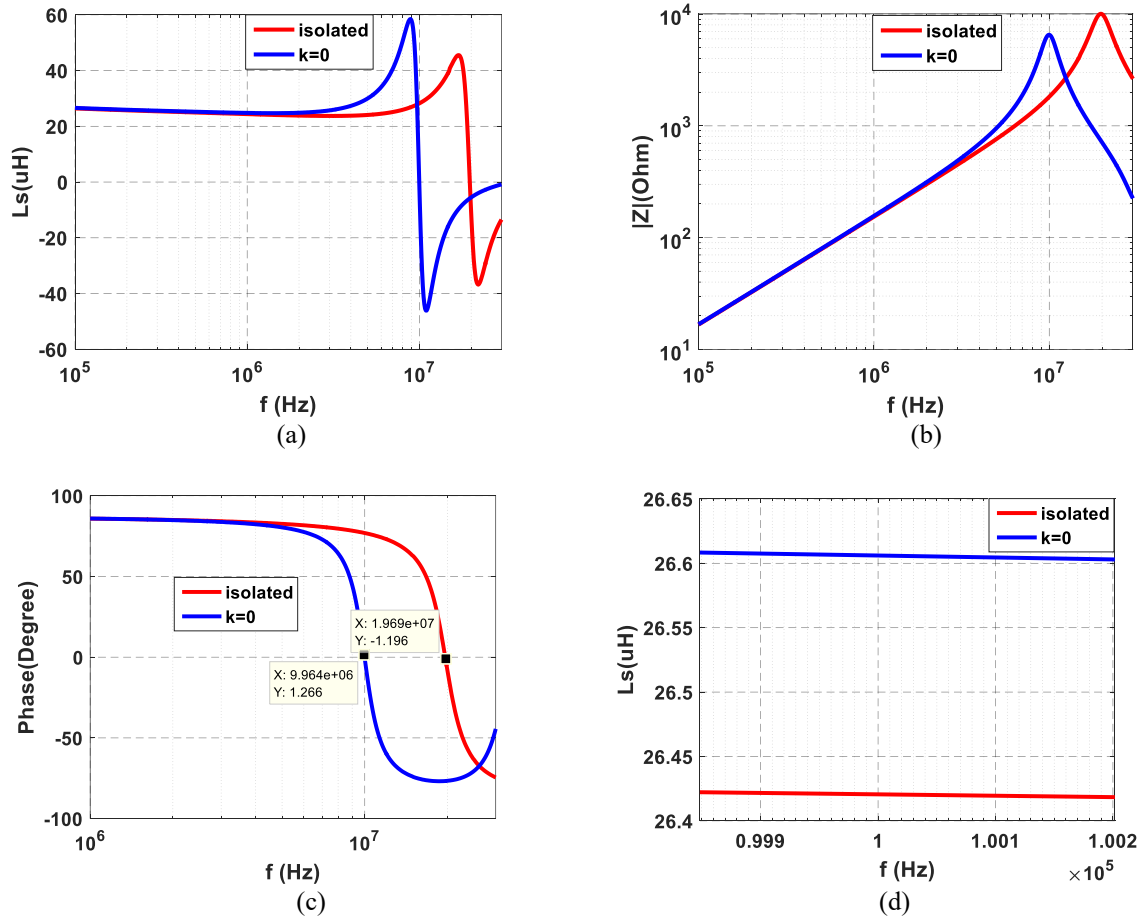


Fig. 6-58. Impedance comparison of the three core configurations. (a) Inductance curves. (b). Impedance curves. (c) Zoomed-in phase curves. (d) Zoomed-in phase inductance curves.

simulation through tedious procedures. As a result, many engineers still design the filters based on the ideal L and C model for simplicity, focusing only on the low frequency linear range. EMI filter is often comprehended as a black magic box, and debugging the EMI filter, for most of the time, still goes through the try-and-error procedure and is regarded as an art. In this section, prediction and modeling approach considering the frequency dependence, self-parasitics and couplings will be presented.

6.7.1 Characterization and prediction approach considering frequency dependence and couplings

To avoid modeling complexities and difficulties, a measurement-based approach is proposed. The basic idea is to capture all needed information from offline low signal measurements to predict the actual insertion loss in the actual power test. Five major steps are needed, as shown in the flowchart of Fig. 6-59. First, measure the impedance of inductors, capacitors, LISN, and parasitic capacitance of converter dc-mid point to the ground, using an impedance analyzer. Then, measure the transfer gain of the filter in the $50\ \Omega$ test environment using a network analyzer. Thirdly, model the filter transfer gain in $50\ \Omega$ test environment through the proposed Matlab/Simulink RF toolbox based frequency domain simulation platform, where all the circuit components are represented by their frequency dependent Z impedances using the actual measurements. With that, all the self-parasitics and frequency dependent core characteristics can be fully captured conveniently. Fourthly, compare and add necessary coupling components such as C_p or M based on the specific filter topology and the proposed general coupling theory, to match the simulated and measured curves. Till now, all the parasitics and couplings have been fully modeled in the TG simulation. Finally, transform the TG simulation to IL simulation by replacing: 1) the $50\ \Omega$ source impedance with actual grounding parasitics and other power filters if exist, 2) and $50\ \Omega$ load with actual LISN

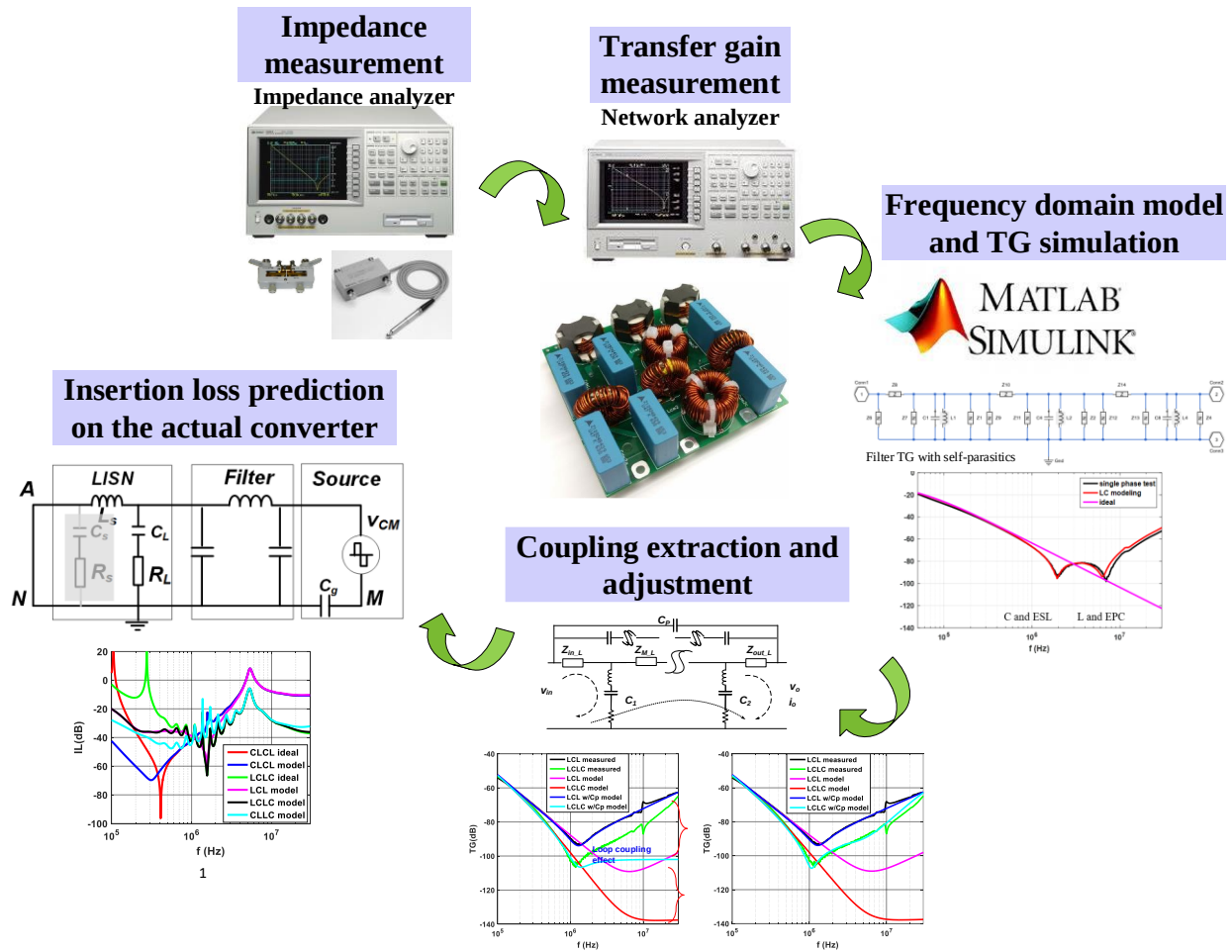


Fig. 6-59. The methodology of filter characterization procedure.

impedance. Then, co-simulated two topologies with and without the filter to obtain the final predicted IL curve.

In this approach, it is easy to include the coupling components. For example, mutual inductors can be added to model the inductive coupling, and bridge-capacitors can be used to model the capacitive coupling.

With the capability, this overall characterization approach provides a simple and fast way to model the behavior of a filter, especially for components with strong nonlinear frequency dependence such as CM chokes. By adding only several dominant couplings, the approach can already capture the main characteristics of a filter and show how significant these couplings affect the filter and what is the theoretic room for filter improvement, if comparing to the ideal filter without such couplings.

In further, by changing filter topology, adding/tuning parasitics and couplings directly in the simulated circuit, or comparing with actual filter TG measurement, the proposed approach is also very helpful for debugging and diagnosing many issues related with component design, PCB layout, and component placement, thus can greatly facilitate filter design and optimization.

6.7.2 Impedance and TG measurement

The impedance of two-stage chokes has been measured as presented in Section 5.7.2. Y capacitor is measured to be pure capacitive within 30 MHz. The impedance of LISN from Solar Electronics is given in Fig. 6-60 instead of using $50\ \Omega$ approximation, since LISN shows inductive impedance below several MHz. Special attention has to be paid on measuring converter grounding capacitance. Since the impedance analyzer from Agilent adopts auto-balancing bridge method for impedance measurement below 100 MHz, as shown in Fig. 6-61 [346], whose principle is also given in Fig. 6-62 (a) and (b), it is difficult for the auto-balancing bridge to measure the grounding

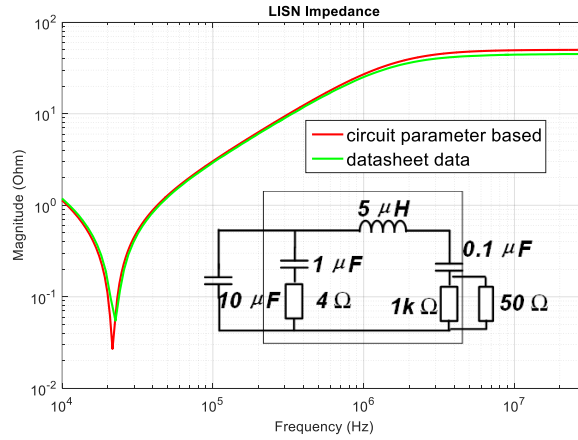


Fig. 6-60. LISN impedance.

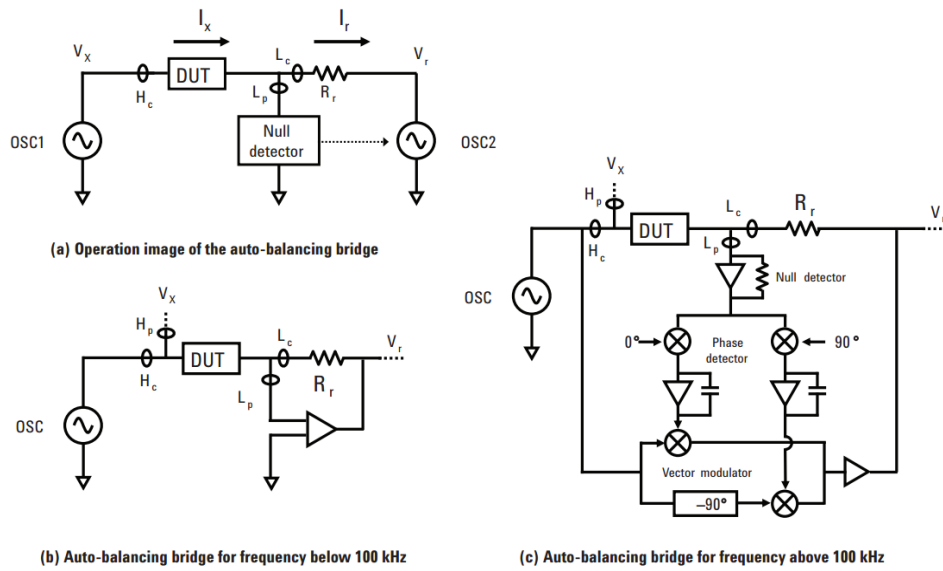


Fig. 6-61. Auto-balance method for impedance measurement [346].

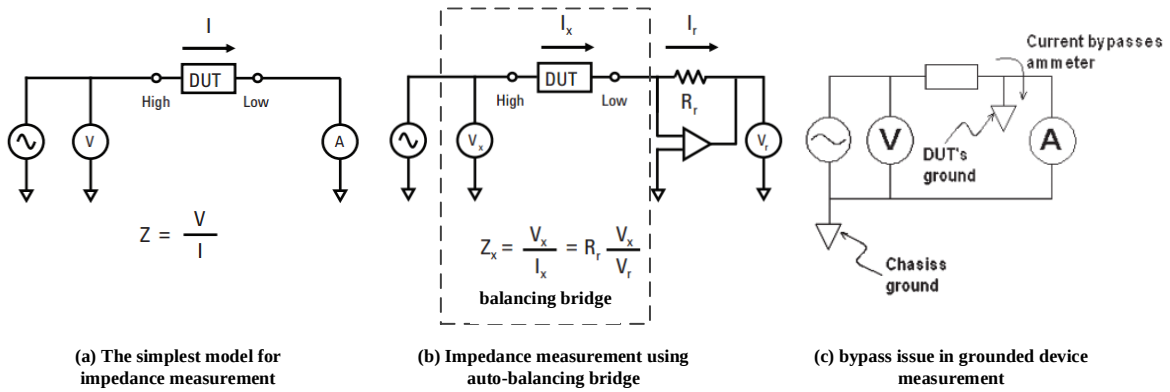


Fig. 6-62. Principle of the auto-balance method and the ground issue for impedance measurement [346].

capacitance directly. From Fig. 6-62 (c), the bridge current will bypass the ammeter due to the same grounding potential [346]. Special impedance probes such as Agilent 42941A probe kit are needed for this type of measurement [346].

The measured impedance of dc-mid point to ground capacitance is shown in Fig. 6-63.

Transfer gain curve reflects the filter attenuation characteristics and can be measured with a network analyzer. To make sure an accurate measurement is performed, the takeaways are:

1). block the CM noise path in the measurement loop to prevent the internal CM noise flow of the instrument from jeopardizing the integrity of the HF signal, as shown in Fig. 6-64. This is because most of Agilent instruments are designed with an unbalanced cable structure where the signal return line is grounded [347]. This can be solved by using two RF isolated transformer at the input port and the receiving port, as shown in Fig. 6-651. Or, high permeability nanocrystalline CM cores can be placed on the cable to form high impedance CM chokes.

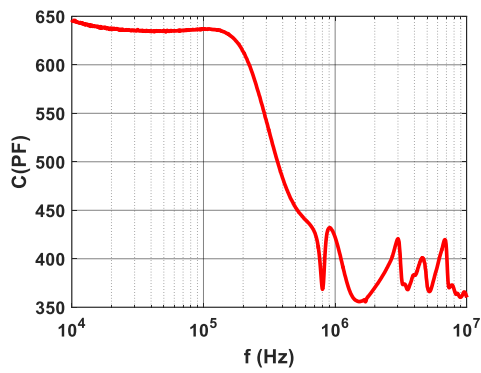
To achieve the RF isolation, proper baluns with sufficient bandwidth should be used to fit the specific EMI standard. RF balun transformers in 50 Ω system such as WBx010-1 from Coilcraft and 16315-60011 from Agilent are recommended.

2). use 50 OHM BNC cables and connectors to connect the EMI filter terminals and network analyzer instead of other connections, to avoid high frequency noise loop coupling.

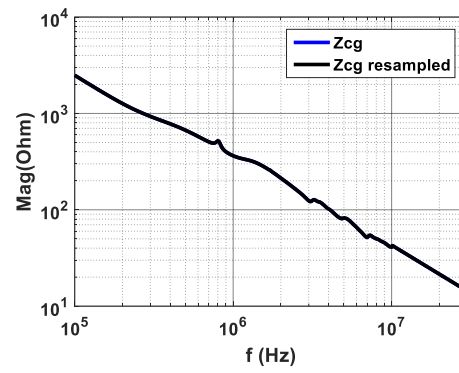
6.7.3 Insertion loss prediction on CM filter

6.7.3.1 Basics of prediction procedure

A two-stage CLCL structure CM filter base on the second version of the filter given in Fig. 5-108 (b) is modeled. Detailed implementation is described in Section 5.7.2. Based on the general coupling theory, the capacitive coupling C_p of the T-joint is estimated first using measured and



(a) Capacitance.



(b) Impedance.

Fig. 6-63. Measured ground impedance from converter dc mid-point.

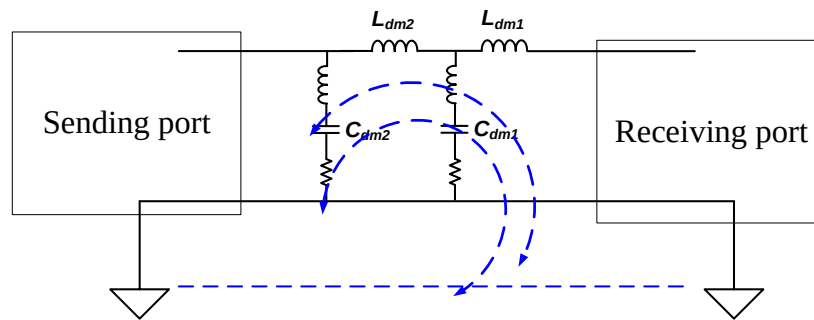


Fig. 6-64. Grounding CM issue for TG measurement.

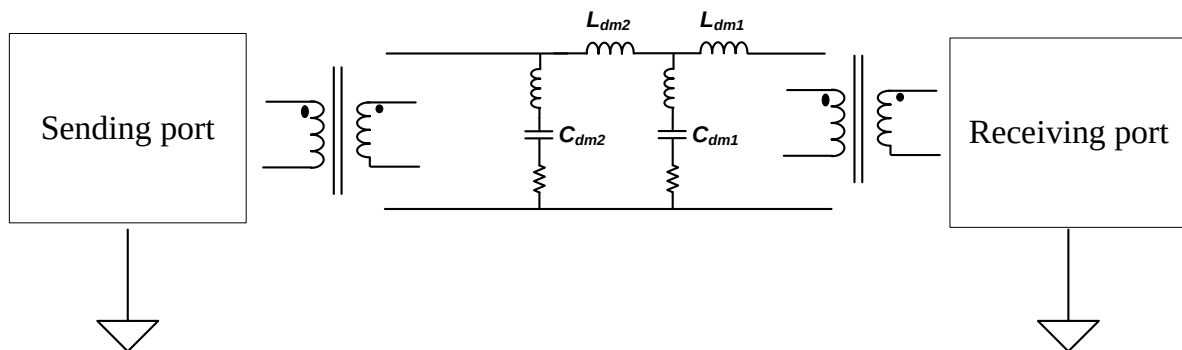


Fig. 6-65. The solution TG measurement.

simulated TG curves on a LCL structure. Although this procedure may need to sweep C_p parameter in a reasonable range in the simulation, it is fast and can be implemented automatically. As shown in Fig. 6-66, C_p is 1.8 pF. However, it should be mentioned that since this value is very small, it may vary a bit once some components are removed or populated.

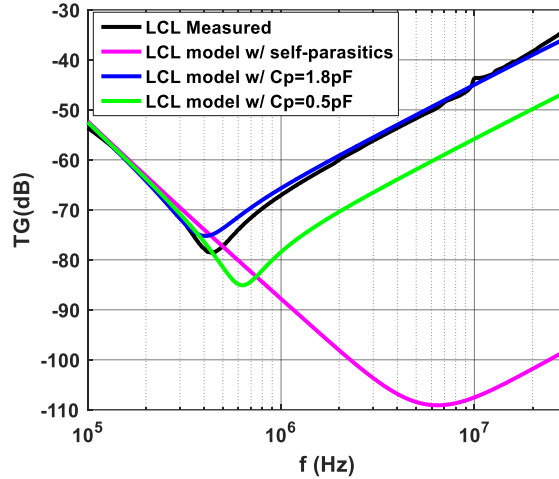


Fig. 6-66. Measured TG curves to predict C_p across LCL on the filter PCB board.

Then, rearrange the filter to the CLCL structure on both the PCB board and the simulation platform. The inductive loop coupling M can be obtained once the TG curves are matched. It is found that the positive loop coupling $M=10$ nH can match the simulated TG curve with the measured curve for the subject filter prototype as shown in Fig. 6-67. A minor mismatch is observed around 10 MHz, which could be induced by some layout parasitics and other minor couplings. Because the CLCL test and CLC test are not conducted at the same time, cable or connector arrangement difference may introduce minor deviation in the C_p value. The matching result shows 1.3 pF C_p in this case.

Once C_p and M are known, IL of the actual converter can be modeled. In addition, other common topologies such as LCL, CLC, and LCLC are also modeled and compared.

It is noticed that adding more components in the final filter prototype could alter the coupling parameter a bit such as increasing the mutual coupled capacitance. Therefore, some variation of C_p and M is expected, which can be easily tuned based the TG matching of the final filter prototype.

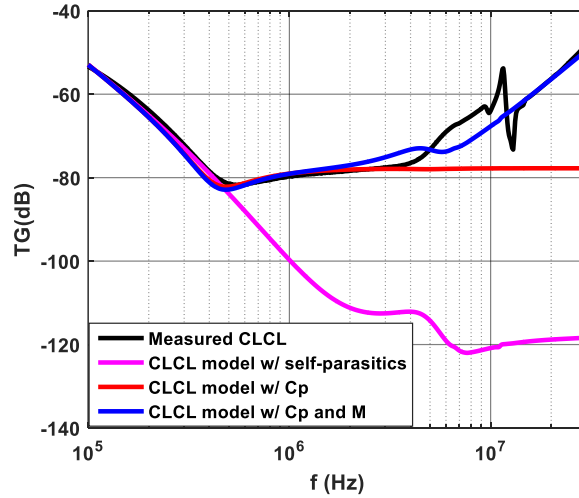
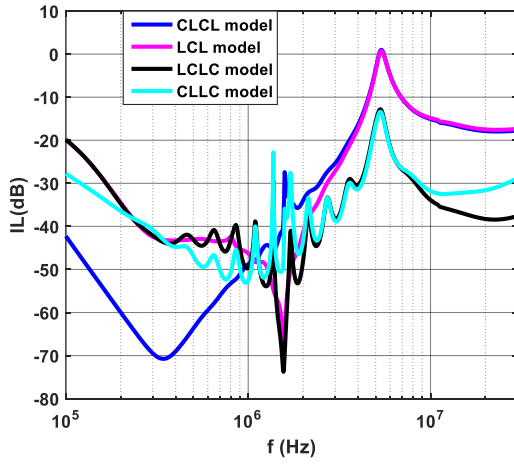


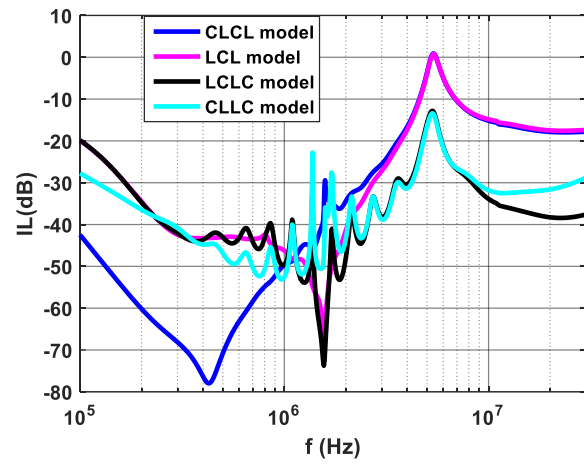
Fig. 6-67. Measured TG curves to further predict inductive coupling on the filter PCB board, $C_p=1.3$ pF, $M=10$ nH.

6.7.3.2 Impact of couplings on IL

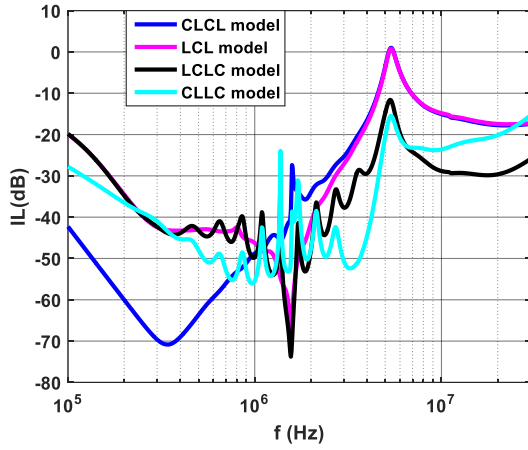
To study the sensitivity of these two couplings, Fig. 6-68 with different C_p and M are used to predict the IL curves. Clearly, C_p mainly impacts the filter topologies with the T-joint, and M mainly impacts filters with the π -shape. However, since the subject converter grounding C_g is low only at 500 pF level, CLCL and LCL filter topologies are immune to inductive coupling. Whereas, LCLC and CLLC topologies suffer performance degradation above several MHz. And CLLC has the highest degradation at HF, about 14 dB at 30 MHz when M is increased from 10 nH to 50 nH. Comparing Fig. 6-68 (a) with the sole bridge C_p between the input-output terminal and Fig. 6-68 (b) with two extra internal coupling capacitances, the main capacitive coupling effect comes from the input-output C_p . This confirms the analysis in Section 6.1.2.



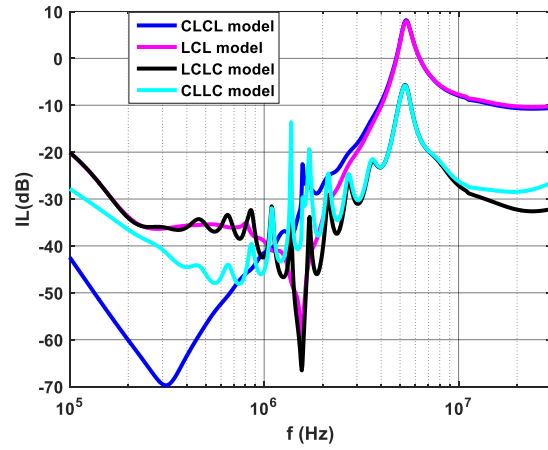
(a)



(b)



(c)



(d)

Fig. 6-68. Insertion loss prediction for different topologies under different coupling conditions. (a) $C_p=1.3$ pF, $M=10$ nH. (b) Three 1.3 pF C_p in the CLCL filter, $M=10$ nH. (c) $C_p=1.3$ pF, $M=50$ nH. (d) $C_p=3$ pF, $M=10$ nH.

From the actual power tests without and with the CM filter given in Fig. 6-69, the insertion loss of the CLCL CM filter can be obtained in Fig. 6-70. Note that only the peaks at real noise points have physical meaning. The result matches the predicted IL of CLCL filter in Fig. 6-68 (a) above 1 MHz, showing the almost 0 dB attenuation above 10 MHz. However, mismatch below 1 MHz is observed. This is eventually found caused by CM interaction between PFC and the input ac programmable power supply, as later verified on an improved EMI filter. Once the source impact is masked by a bulky choke between LISN and the ac source, 15 dB more attenuation can be achieved at PFC switching frequency 450 kHz, as seen from the testing result in Fig. 6-72.

If C_p is reduced from 1.3 pF to a lower value such as 26 times smaller and M is still 10 nH, the insertion loss of the CLCL improves by 30 dB above 10 MHz, while the LCLC gets worse due to the inductive coupling as shown in Fig. 6-72 (a). If M is further reduced to 0, IL of LCLC can be increased a lot in Fig. 6-72 (b). Other extreme conditions are also studied. Fig. 6-72 (c) shows the result when M is reduced to zero and C_p is 1.3 pF. Fig. 6-72 (d) gives the case when both M and C_p are 0. And Fig. 6-72 (e) gives the case when 1.5 pF capacitance is crossing L_{dm1} - L_{cm1} in the previous ideal case. Impacts on IL above 1 MHz can be observed, which indicates that the coupling effect of this bridge capacitance was overridden by the dominant input-output C_p coupling.

6.7.3.3 Practical CM insertion loss prediction for final EMI filter

To further increase the attenuation of CM and DM filter at HF, a third stage CM/DM cable filter with 4 turns of VAC W450 CM core and 10 turns of Micrometal HF-044147-2 DM powder core have been inserted at the ac input terminal, where L_{CM3} is outside the aluminum enclosure. Together with shielding and damping mitigation schemes, the final filter structure is presented in Fig. 6-73.

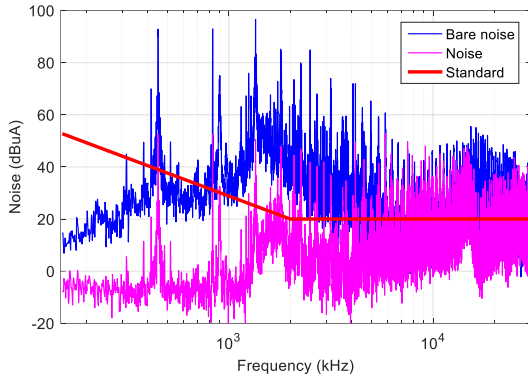


Fig. 6-69. Measured bare noise and noise after the filter in the power test.

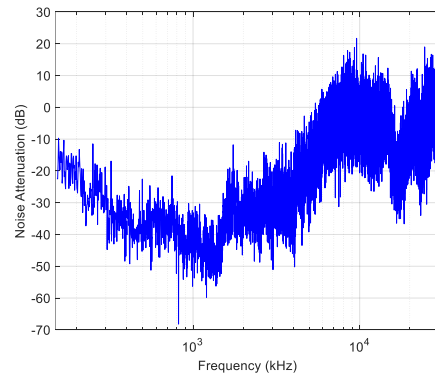


Fig. 6-70. Calculated current insertion loss from the measurements.

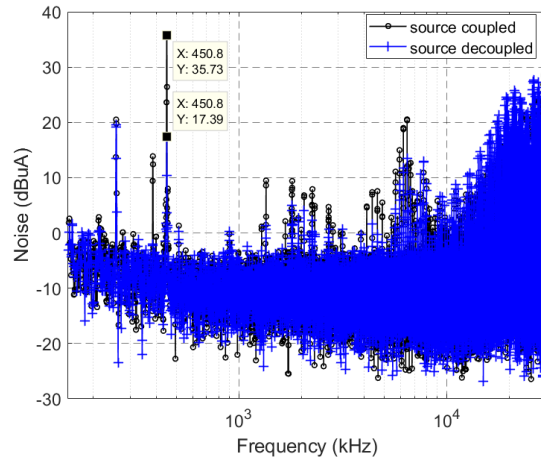
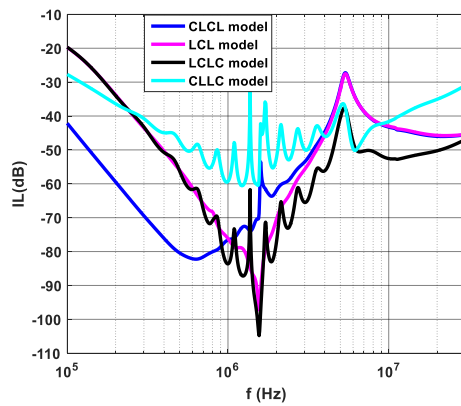
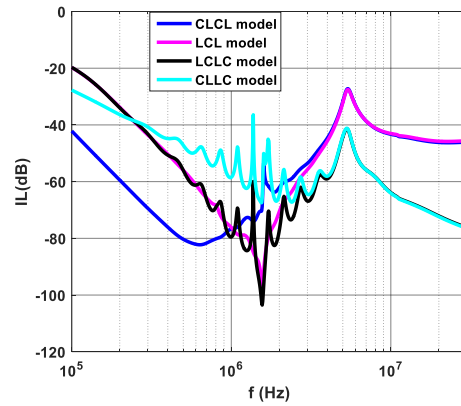


Fig. 6-71. Impact of CM noise interaction with incompletely decoupled ac power supply at $f_s=450$ kHz.



(a)



(b)

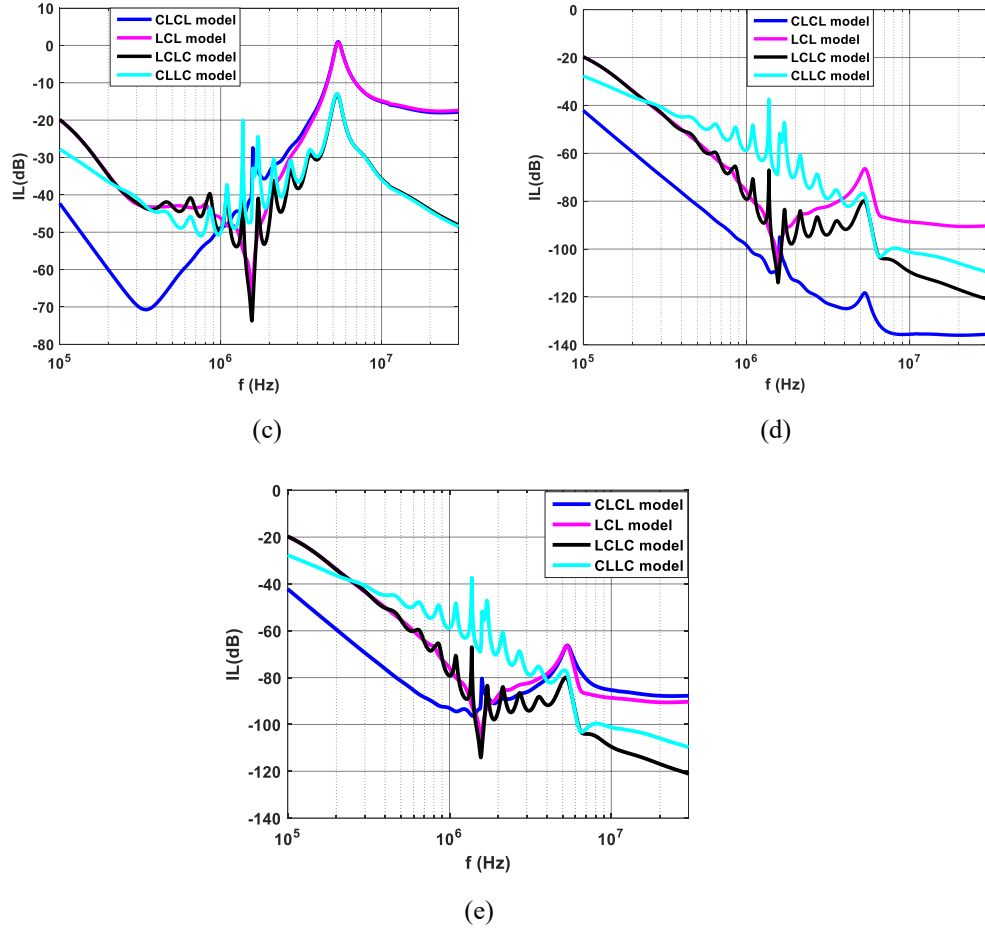


Fig. 6-72. Insertion loss prediction and study for different topologies under different coupling conditions. (a) $C_p=1.3/26$ pF, $M=10$ nH. (b) $C_p=1.3/26$ pF, $M=0$ nH. (c) $C_p=1.3$ pF, $M=0$ nH. (d) $C_p=0$ pF, $M=0$ nH. (e) $C_{p1}=1.5$ pF, $C_p=0$ pF, $M=0$ nH.

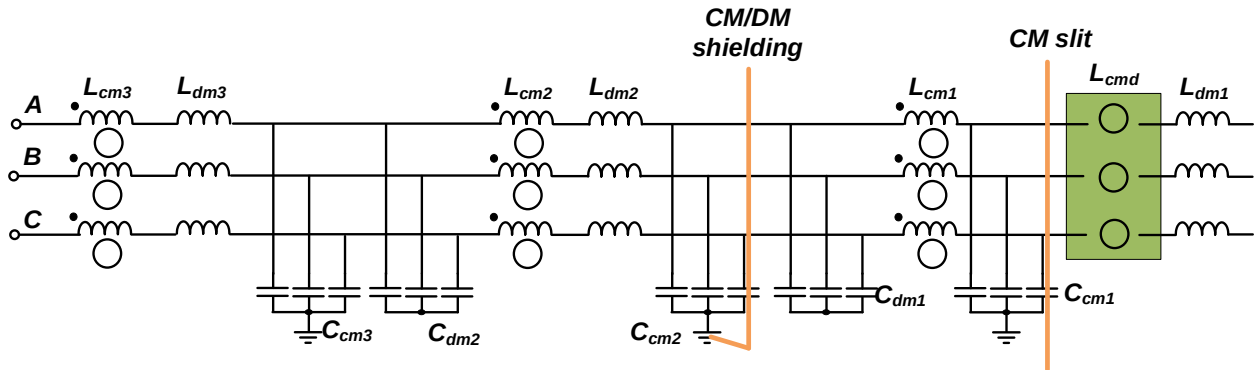


Fig. 6-73. Final adopted EMI filter topology for the three-phase battery charger.

To predict the IL of EMI filter in whole converter system, the power stage, enclosure, grounding, and filter are never independent. In fact, actual coupling and parasitic parameters for a multi-stage filter are not just generated inside a standalone filter. Instead, they are also affected by the actual converter set-up. For example, the main circuit power loop can also couple with filter output loop, and the configuration and the length of grounding cables also impact the parasitic ESL of Y capacitors. Therefore, a more detailed multi-step procedure considering the impacts of the converter implementation is proposed for a multi-stage filter, in which only one dominant coupling is extracted per each step:

- 1) install the filter into the enclosure box and measure its transfer gain without C_{cm3} before it is tied to the power stage, to extract the overall C_p coupling (notice that L_{cm3} is outside box, thus its related coupling is negligible);
- 2) measure the TG with C_{cm3} , to include the dominant M coupling (input-output coupling);
- 3) test the TG from the power board to filter, and repeat 2), so that the coupling from the inner power loop is also included;
- 4) simulate the overall filter IL in frequency domain integrating these coupling terms.

Fig. 6-74 shows the step-by-step result. First, the dominant capacitive coupling is extracted as 0.675 pF from CLCL structure as in Fig. 6-74 (a) based on the matching of simulated TG curves and measured black curve. The mismatch above 10 MHz is studied from different possible coupling or parasitic factors and turns out to be determined by a 25 pF small parasitic C_{y3} from filter terminal to the enclosure (this capacitance can be neglected later when C_{cm3} is added). Again, M coupling only has a trivial impact in this topology. Then, with C_{cm3} , from the comparison of the red curve and black curve, the ESL of cable has the highest impact above 7 MHz as shown in Fig. 6-74 (b). Due to the inevitable long grounding cable outside the charger box, measured L_g is

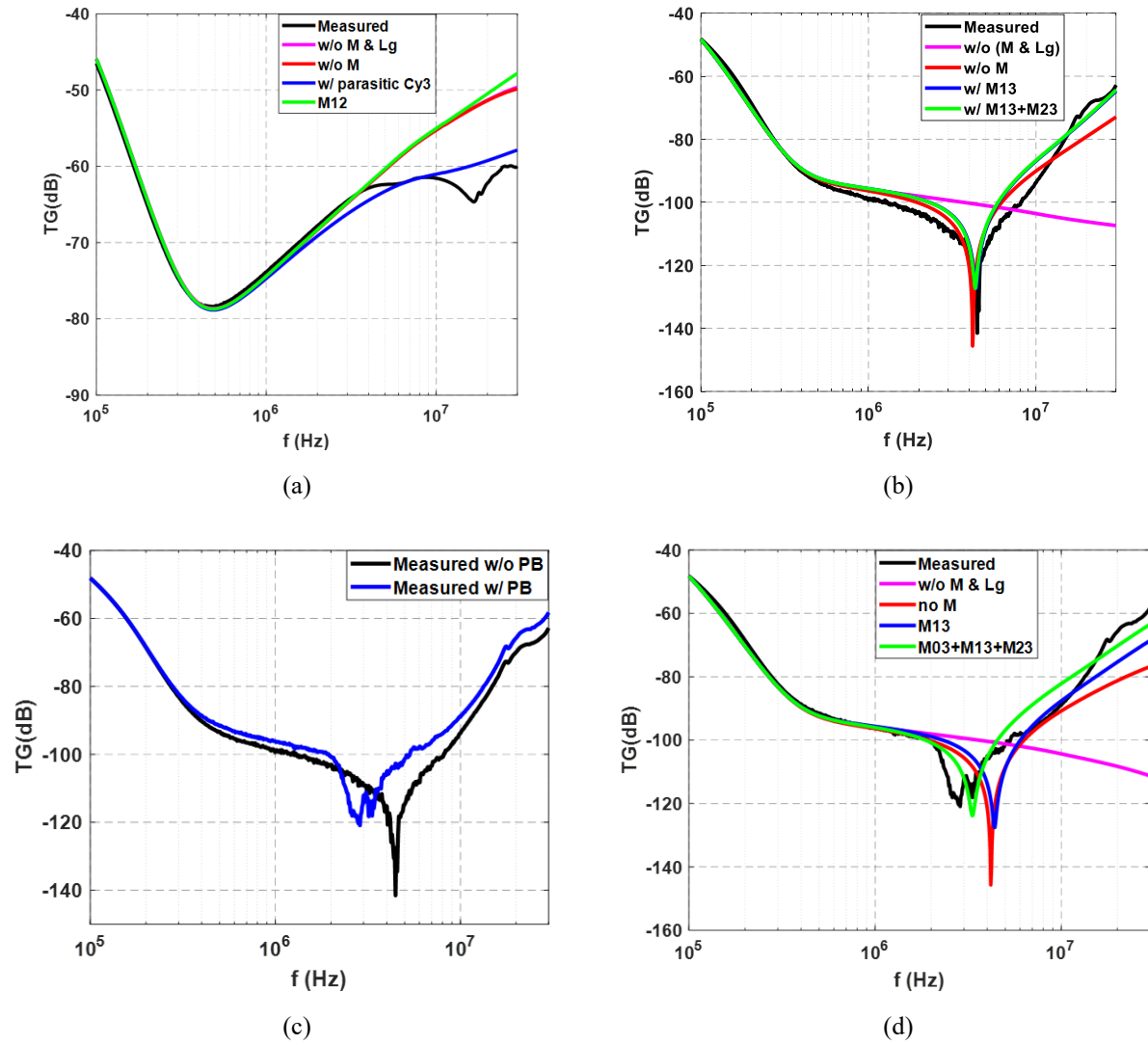


Fig. 6-74. Step-by-step extraction of parasitic couplings for insertion loss prediction. (a) C_p extraction. (b) M extraction. (c) Impact of M_{03} . (d) M_{03} extraction.

roughly 320 nH. M coupling also takes certain effect, where the input-output M_{13} overrides the other loop coupling M_{23} . M_{13} is extracted as 3 nH. Next, with the power stage connected with filter, another input loop via the grounding parasitic capacitance from power device terminal to ground/enclosure also forms an inductive coupling onto the output loop of the filter, i.e. M_{03} . Impact of this coupling is shown in Fig. 6-74 (c) and the almost matching in the green curve of Fig. 6-74 (d) indicates $M_{03}=3$ nH (at HF range, an error occurs, which could be partially from measurement error of the set-up, and partially from neglect of other couplings).

Finally, the simulated insertion loss is shown in the magenta curve of Fig. 6-75. And Fig. 6-76 gives the measured insertion loss based on the measured CM noise with and without CM filter. Since measured noise has sideband, only at actual noise frequencies, the negative envelope represents IL. It is clear the predicted IL curve almost matches the power test result along the whole conducted frequency range, except roughly 10 dB difference from 7 MHz to 30 MHz where the trend of IL curve is still right. This mismatch is partially due to the sensitive CT measurement errors in this range, and partially due to the errors gathered in the prediction procedure such as impedance measurement error and neglect of other minor couplings. Overall, the filter attenuation at this range stays around 50 dB.

6.7.4 Experimental results of EMI power test

With all above parasitic and coupling mitigation approaches, as well as a damping scheme through an inserted small CM choke to damp an undesired CM loop oscillation between L_{dm1} and grounding parasitic capacitance, EMI filter in-circuit performance has been significantly improved.

Fig. 6-77 shows selective EMI test results in the Vienna-type PFC stage before and after EMI filter mitigations. And the selective EMI test results of the two-stage charger before and after EMI filter mitigations are also presented, as shown in Fig. 6-78.

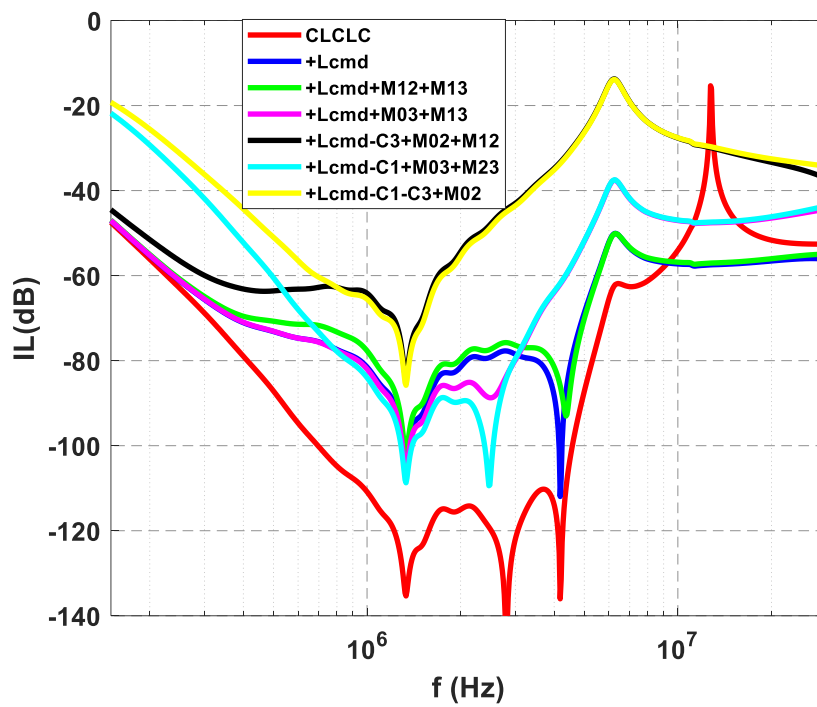


Fig. 6-75. Predicted CM IL loss with the actual converter.

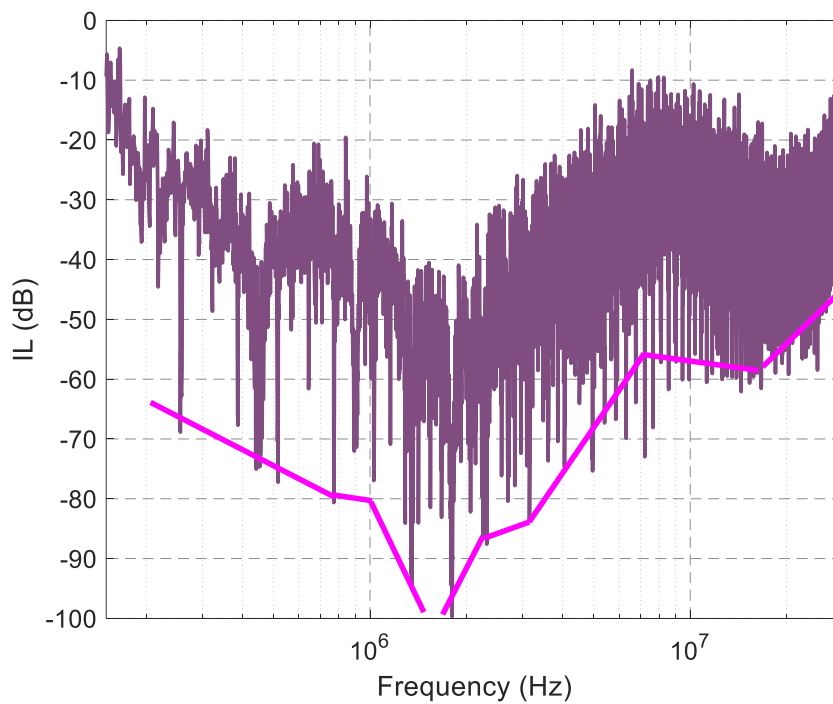
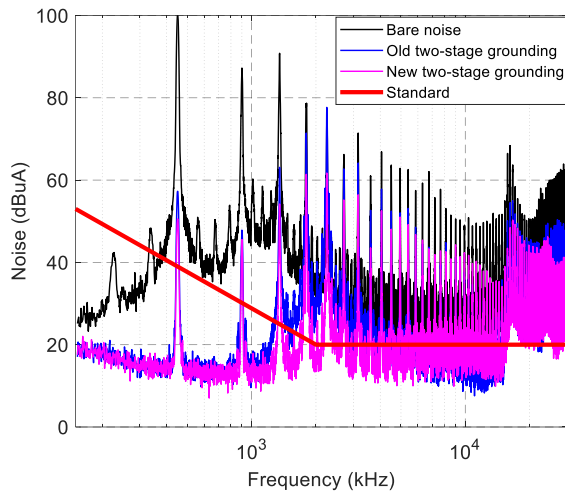
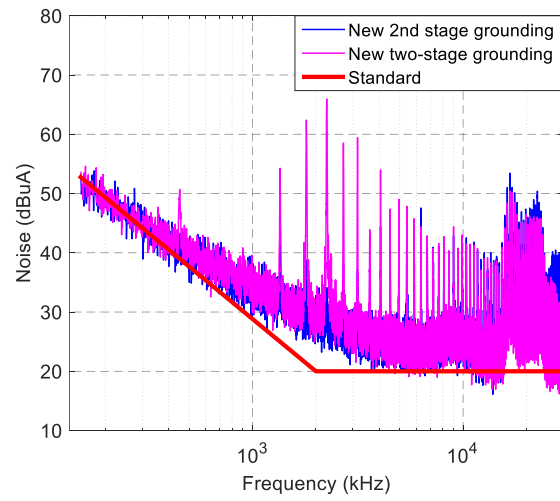


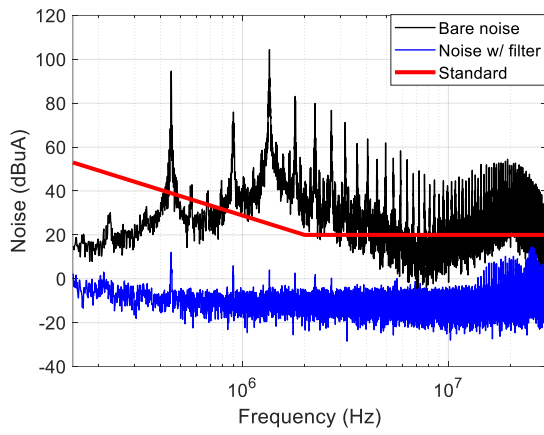
Fig. 6-76. Measured filter insertion loss from power test.



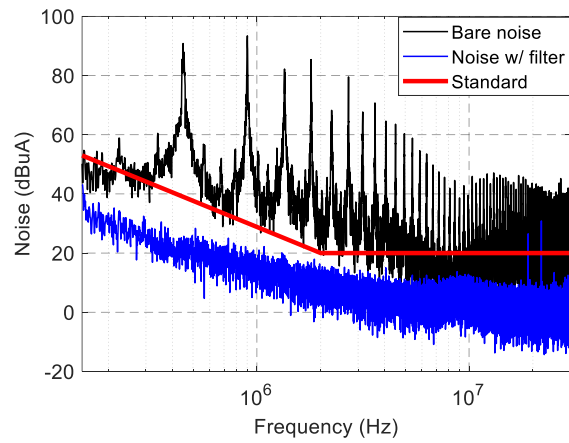
(a) CM noise at 800 Hz, 115 Vac, 650 Vdc, and full load with the original filter



(b) DM noise at 800 Hz, 115 Vac, 650 Vdc, and full load with the original filter

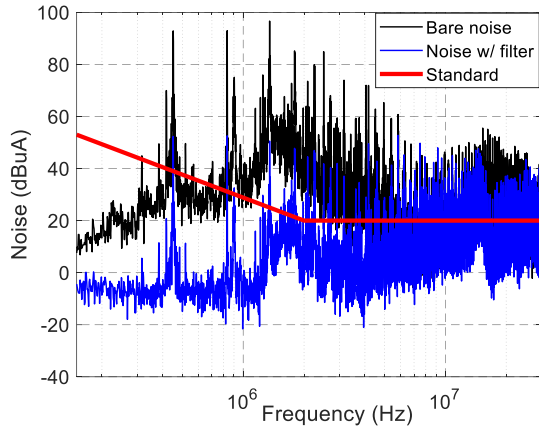


(c) CM at 800 Hz, 115 Vac, 625 Vdc, and full load with the improved filter

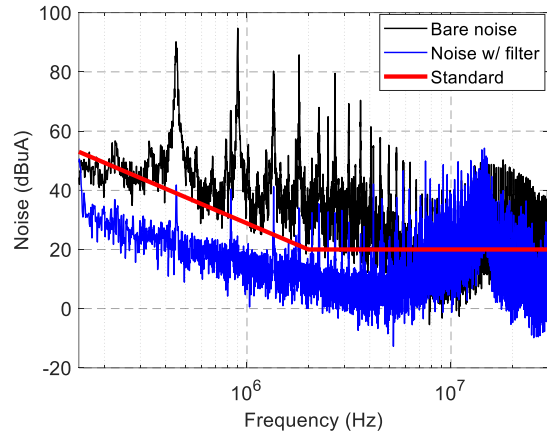


(d) DM at 800 Hz, 115 Vac, 625 Vdc, and full load with the improved filter

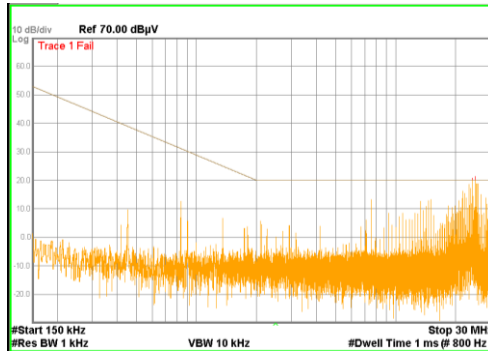
Fig. 6-77. Comparison of measured EMI noise before and after filter improvement in single PFC stage.



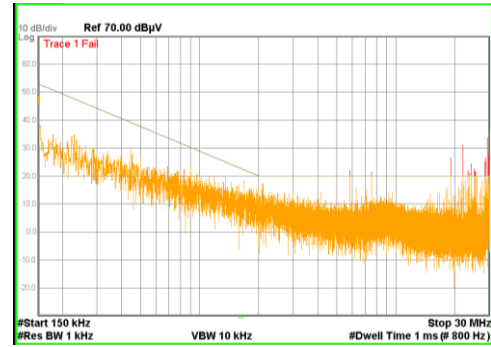
(a) CM noise at 800 Hz, 115 Vac, 660 Vdc and full LLC load with the original filter



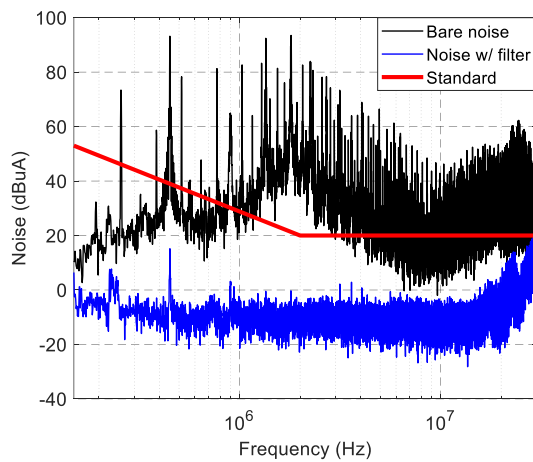
(b) DM noise at 800 Hz, 115 Vac, 660 Vdc and full LLC load with the original filter



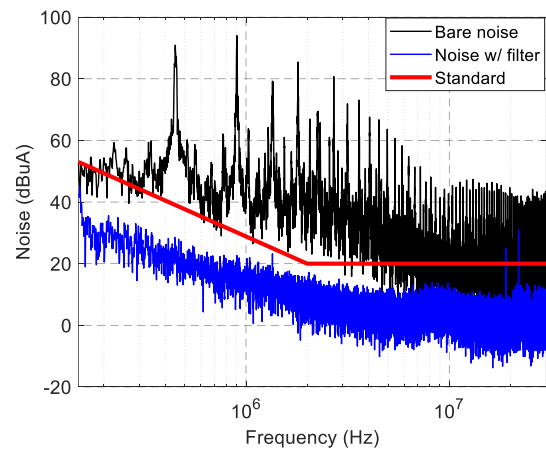
(c) CM noise at 800 Hz, 115 Vac, 670Vdc and full LLC load with the improved filter



(d) DM noise at 800 Hz, 115 Vac, 670Vdc and full LLC load with the improved filter



(e) CM noise at 800 Hz, 115 Vac, 625Vdc and full buck load with the improved filter



(f) DM noise at 800 Hz, 115 Vac, 625 Vdc and full buck load with the improved filter

Fig. 6-78. Comparison of measured EMI noise before and after filter improvement in the two-stage charger.

6.8 Summary

The seldom noticed capacitive coupling in T-shape and associated filter structure has been comprehensively studied. The mechanism of this coupling effect is analyzed and proved through different approaches. Impact of this coupling is significant both for CM and DM filters, even with a slight pF level mutual capacitance. After reviewing the inductive coupling in PI shape related filter structure, together, a duality of the two couplings is found for T-shape and PI-shape filters. The general coupling theory is then established, through which, general filter selection criteria that consider not only the traditional mismatch theory but also two dominant coupling effects have been formed for different topologies.

In further, coupling mitigation methods for both effects have been proposed. The capacitive coupling is found physically introduced by PCB material and trace coupling and space coupling. Shielding and PCB slit approaches can thus reduce this coupling capacitance. On the other hand, inductive coupling can be mitigated from PCB layout and component placement. Several good practices are proposed especially for three-phase filter design, considering its inherently more complicated structure and clearance requirement, compared to typically studied single-phase filter. Based on the general coupling theory, some topological approaches have also been proposed to mitigate or avoid certain or all coupling issues in an EMI filter.

In addition, parasitics of inductors should also be reduced once the coupling effects are mitigated. Two typical winding schemes are analyzed and a general winding scheme considering the partial outer layer is proposed and analytically modeled showing much lower EPC, 4X lower in a prototype. Meanwhile, to fully model winding scheme related EPC, a comprehensive EPC model with three types of decoupled winding layer capacitances is derived. The work has corrected some previously misunderstood knowledge on winding capacitance and winding schemes.

Based on the above work, a filter characterization and prediction approach has been established, combining the measured frequency domain impedance information of each component and coupling parameter extraction procedure. The majority of the procedure can be implemented in a frequency domain simulation, greatly simplifying the modeling effort and providing flexibility and extension capability in modeling and predicting the insertion loss of any complicated filter topologies. In the end, filter insertion loss in the actual battery charger has been predicted and fairly matches power test results along the whole conducted EMI frequency range.

An improved three-phase EMI filter has been designed and tested with the final charger under different operation modes. Its performance on both CM and DM noise reduction has been successfully demonstrated.

7 Conclusion and Future Work

7.1 Conclusion

The dissertation has presented the work in a wide range of power converter applications from high power transmission grid to low power aircraft charger, on a series of design and control issues associated with effects introduced by dc and low frequency power interfacing, high switching and high di/dt and dv/dt operation, device parasitics, and EMI filter parasitics and couplings. The main conclusions and contributions are as follows.

- Interfacing the high voltage dc converter directly with three-phase ac lines is a promising approach to form a hybrid ac/dc power transmission architecture. Analytical power transfer capacity and hardware cost as a function of ac and dc voltage and current has been established and compared with pure HVAC and pure HVDC upgrading architectures. Technical feasibility is also verified in both simulation and experimental results.
- Saturation hazard of the interface zigzag transformer between ac and dc power flow under three-line unbalances is identified, analyzed, and experimentally verified. Mitigation solutions from passive transformer design to active hybrid line impedance conditioner are proposed, including hardware design methodology and impedance control algorithms. High dc current penetration into existing ac lines is demonstrated under unbalanced line conditions. The HLIC has significantly reduced the hybrid line cost and mitigated the potential saturation issue.
- The general line modeling and emulation schemes are proposed, and the extension capability of the emulation model has been analytically presented, showing the feasibility in emulating the line represented either by a multi-section PI model or a distributed Bergeron's model.

- The impact of PWM voltage ripple in a VSI based emulation grid on sensing and sampling has been analyzed, and the resulting impacts on power behaviors of the line emulator are also described. The four-point moving average sampling method shows the best noise immunity.
- The trivial dc bias in sensing and sampling voltage has shown a high dc current bias effect on emulated line current flow. An active dc offset control using the combined L-LR model is proposed with adaptive frequency tuning ability showing zero phase delay and zero attenuation on the main power flow. The controller is devised from the HPF perspective to ensure the accuracy and dynamic performance of the line emulator during grid transients, which shows a deeper understanding compared to other prior work on dc removal control in the motor application. The interfaced grid impedance should also be included in the controller design.
- The stability issue caused by the interaction between the transmission line emulator and its interfaced grid impedance is analyzed for both the phasor domain and time domain emulation models. A criterion that determines the stability and also defines the impedance boundary of the line emulation is proposed and experimentally verified. For voltage-controlled current-source based emulation, the stability is guaranteed if the ratio of the external interfaced grid impedance over the emulated line impedance lower than a certain ratio, depending on system configurations. This analysis can also be applied to other types of emulation schemes such as current-controlled voltage-source emulation.
- The impacts of high switching frequency, high di/dt , and dv/dt on sensing and power quality control have been identified and the mechanisms are analyzed, and sensing and layout solutions to mitigate these impacts are proposed. Minimized signal loop layout is critically important and conditioning amplifiers are vulnerable to high frequency noise and responsible

for generating the dc or low frequency sensing noise. Isolation amplifier with high CMTI is desired.

- A proposed sampling method for three-phase ac-dc converters is effective in reducing the chance of picking up the switching noise and ripple in high switching frequency converters, leading to improved current sampling quality and lower current THD.
- PWM voltage distortion due to device junction capacitances in three-level converters at turn-off has been found with severe impact on current distortion. A modulation compensation method in GaN based Vienna-type rectifier is proposed considering the nonlinear device junction capacitance, and compensation errors in another possible scheme is also analyzed. Computation effort is also highly reduced to apply this scheme to dynamic loading conditions, showing good performance. Modeling of this type of distortion is analytically derived for both voltage THD and current THD using switching frequency as a variable, showing the significant impact at higher frequencies.
- The previously unnoticed device junction capacitances and commutation loops due to the non-active device in various three-level converter phase-legs are observed. The impact on switching loss, device stress and PWM voltage distortion are analyzed. It highlights the necessity of using a three-level phase leg for DPT instead of the conventional two-level double pulse tester for three-level converter loss and stress characterizing. Alternatively, a loss calculation method is proposed for three-level converters by directly using the data from the conventional two-level double pulse tester to reduce the design efforts. The relationship between the analytical loss and DPT E_{on} and E_{off} curve fitting formulas in GaN based converters is also disclosed, which further induces a more accurate temperature-dependent loss model.

- This research work establishes the fundamental knowledge on performance degradation of EMI passive filters, especially in a multi-component structure. The impacts and mechanisms of both inductive and capacitive coupling on different filter structures are presented. General coupling theory is established and fulfill the filter selection criteria together with the well-known mismatching theory. A general filter is a combination of T-shape and PI-shape elements. In T-shape structure, the inductive coupling is the dominant effect and in PI-shape structure, the capacitive coupling is found as the main effect. Combined mitigation solutions from layout to filter structure and to shielding are proposed to reduce the inter-component coupling. In addition, a general decoupled layer capacitance modeling on EMI inductors is proposed, from which a general winding scheme to reduce the self-parasitics is derived and experimentally verified. Filter characterization methodology including measuring, modeling, and prediction has shown an excellent accuracy up to 10 MHz, and it facilitates the design and debug of the multistage filter. All these efforts help push the EMI filter to approach the ideal performance in a further degree, especially at HF.
- A high speed digital controller is designed for the two-stage GaN based charger with three-phase dual ac input and dual dc output, multiple sampling variables, multiple control loops and operation modes, HMI, software protection, and operated at the high switching frequency. An all-in-one DSP control is developed with three paralleled and communicated cores and on-chip ADC and DAC, to speed up the controller computation for heavy control tasks and to reduce the controller size, cost, and complexity.
- A GaN based wide range input and dual-output battery charger with three-level PFC and dc-dc converters and the all-in-one high-performance controller are finally built and tested. The results show that in order to accomplish multi-functions, high density, and decent performance

from the merits of GaN devices, impacts from high switching frequency, high di/dt dv/dt , parasitics, and electromagnetic interference should all be well understood and addressed in the first place. The accumulated knowledge and approaches in this research have provided some thoughts and a solid base for further advancement in this area in the future.

7.2 Future work

- EMI filter design optimization

Although EMI filter has been well adopted in most of the products, its design procedure is still not optimized. The conventional filter design is too ideal, assuming the ideal inductors and LC corner frequency. The strong frequency-dependent nonlinearity on magnetic permeability has not been counted in the early design phase of a CM choke, although some modeling work on existing filters does consider this effect. Also, the strong impacts of dc and quasi-dc bias on DM inductor and capacitor are not considered either. The combination of LC is often based on the maximum C and thus is not optimized. As a result, the low size/cost/weight target and desired attenuation performance of an EMI filter are not guaranteed. The efforts and cost of late-stage trial-and-error and overdesign are huge.

Some work has been conducted on modeling the self-parasitics of filter components into design [348]. However, the coupling effects were not included. And the aforementioned nonlinearities were not considered. Further, for CM filter design, instead of continuing the conventional LC corner frequency-based approach, the combination of choke impedance and capacitance (ZC) should be adopted. As for filter optimization, the traverse of all LC combinations is a typical approach, however, possible resonances in the passive network formed by filter components and converter grounding parasitics may not be fully considered. On the other hand, adding a damping network for all components of a filter is chosen as a blind approach [263, 265].

However, this may be unnecessary. A preferred design approach would be using the design software to identify the potential resonances automatically and smartly according to the specific filter structure, then choosing the proper LC or ZC filter parameters to avoid such resonances thus eliminate unnecessary damping components to save the loss and size of the filter. The benefits and feasibility study could be a future topic.

- Design optimization of high speed WBG based converter

When applying high speed high di/dt , dv/dt WBG device for converters, traditional design methods for Si devices-based power converters becomes improper since the conventional switching model oversimplifies the switching loop commutation, neglect the insignificant parasitic impacts due to the low di/dt and dv/dt , and many HF related effects are also not obvious at low frequency range thus were often neglected in the past. Work in recent years have noticed the impacts of these new features of WBG devices on gate drive, on power loop layout, and on cooling design, but how to utilize them in the early stage converter design is not clear. Practically, the design assumes ideal component and converter models with a certain design margin and then retunes many variables based on the tested results. The state-of-art optimal design procedure often sacrifices the accuracy of the converter design models to exchange for a faster, universal, and manageable design flow, leading to aggressive and impractical designs whose performance deviates from the performance of actual converters. The work of this dissertation has addressed the parasitic of non-active impact on loss, device stress, power quality in three-level, can be added into the existing design model and can be extended to multi-level converters. The mitigation on sensing, sampling, modulation distortion can also be utilized as a measure to mask the impact of associated model nonlinearity and thus simplify the design model. The filter optimization should not only be improved as mentioned above but also be cooperated in depth with power stage design,

considering the switching frequency impact on converter loss, distortion, and on filter loss/size with frequency-dependent nonlinearity well modeled. Meanwhile, parasitic and coupling mitigation should also be leveraged as a way to mask or mitigate the impacts of these nonlinearities to simplify the design model and facilitate the design optimization.

- Device protection from converter level perspective

Protection of Si is mature, and protection of SiC devices have also been well studied in recent years and some commercial SiC gate drivers have integrated desaturation functions. As the power level of GaN based converter is rising, protection of these devices and thus the whole converter is a must in the near future. However, the study on GaN device protection is still in early exploration. Desaturation detection for GaN is not deemed as a good option due to extra switching loss and higher conduction loss involved [349]. Some work has been done on the current injected GIT GaN device, fully based on gate signal instead of desaturation approach [349], however, this may not be easy for voltage-driven type GaN devices. Another solution recently utilizes the spectrum pattern of the dc bus voltage during the shoot-through fault transient of a phase leg to detect and protect the device [350]. This can be further extended to the concept of protection from converter level based on the feature of specific converter topologies as what was done in SiC JFET Vienna-type rectifier [351, 352]. Some new schemes on GaN based converters should be explored to overcome the desaturation protection issues and suitable for the target topology. Two aspects should be considered in this area: 1) a universal protection solution is, in principle, always desired; 2) if it is not feasible currently, why not come with a topological-customized solution first?

7.3 Publication list

Journal papers

- **B. Liu**, R. Ren, F. Wang, D. Costinett, and Z. Zhang, “Study of Inductor Winding Schemes with Outer Fractional Layer via Improved Parasitic Capacitance Modeling,” *IEEE Transactions on Power Electronics*, **under review**.
- **B. Liu**, R. Ren, E. A. Jones, F. Wang, D. Costinett, and Z. Zhang, “Effects of Junction Capacitances and Commutation Loops Associated with Non-conducting Devices in Three-Level Ac/Dc Converters,” *IEEE Transactions on Power Electronics*, **under review**.
- **B. Liu**, R. Ren, E. A. Jones, F. Wang, D. Costinett, and Z. Zhang, “A Modulation Compensation Scheme to Reduce Input Current Distortion in GaN Based High Switching Frequency Three-Phase Three-level Vienna Type Rectifiers,” *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 283-298, Jan. 2018.
- **B. Liu**, X. Shi, Y. Li, F. Wang, and L. M. Tolbert, “A Line Impedance Conditioner for Saturation Mitigation of Zigzag Transformer in Hybrid Ac/Dc Transmission System Considering Line Unbalances,” *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5070-5086, July. 2017.
- **B. Liu**, Z. Zhang, E. Jones, and F. Wang, “Application of GaN in hard-switching converters: challenges and potential solutions,” *Power Electronics (A Chinese Journal)*, vol. 51, no. 9, pp. 3-13, Sept. 2017.
- S. Zhang, **B. Liu**, S. Zheng, Y. Ma, F. Wang, L. M. Tolbert, “Development of a Converter-Based Transmission Line Emulator with Three-Phase Short-Circuit Fault Emulation Capability,” *IEEE Transactions on Power Electronics*, 2018, early access.
- Y. Li, X. Shi, **B. Liu**, W. Lei, F. Wang, L. M. Tolbert, “Development, Demonstration and Control of a Testbed for Multi-Terminal HVDC System,” *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6069-6078, Aug. 2017.
- X. Shi, Z. Wang, **B. Liu**, Y. Li, L. M. Tolbert, F. Wang, “Steady-State Modeling of Modular Multilevel Converter under Unbalanced Grid Conditions,” *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7306-7324, Sept. 2017.
- R. Ren, **B. Liu**, E. A. Jones, F. Wang, Z. Zhang, D. Costinett, “Capacitor-Clamped, Three-level GaN-Based DC–DC Converter With Dual Voltage Outputs for Battery Charger Applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 841-853, Sept. 2016.
- C. Zhao, B. Trento, L. Jiang, E. Jones, **B. Liu**, Z. Zhang, D. Costinett, F. Wang, L. M. Tolbert, J. Jansen, R. Kress, and R. Langley, “Design and Implementation of a GaN-Based, 100-kHz,

102-W/in³ Single-Phase Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 824-840, Sept. 2016.

- X. Shi, **B. Liu**, Z. Wang, Y. Li, L. M. Tolbert, F. Wang, "Modeling, Control Design, and Analysis of a Startup Scheme for Modular Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7009-7024, Nov. 2015.
- X. Shi, Z. Wang, **B. Liu**, Y. Q. Liu, L. M. Tolbert, F. Wang, "Characteristic Investigation and Control of a Modular Multilevel Converter-Based HVDC System Under Single-Line-to-Ground Fault Conditions," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 408-421, Jan. 2015.

Book chapter

- F. Wang and B. Liu, (2018) GaN in AC/DC Power Converters. In: G. Meneghesso, M. Meneghini, E. Zanoni (eds) Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion. Integrated Circuits and Systems. Springer, Cham. https://doi.org/10.1007/978-3-319-77994-2_7

Conference papers

- **B. Liu**, R. Ren, F. Wang, D. Costinett, and Z. Zhang, "Capacitive Coupling in T-shape Related EMI Filters: Mechanism, Effects, and Mitigation," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2018, in press.
- **B. Liu**, E. Jones, R. Ren, Z. Zhang, F. Wang, and D. Costinett, "Extra Device Capacitance in Three-level Converters and Loss Re-evaluation via Conventional DPT Data," in *Proc. IEEE 1st Workshop on Wide Bandgap Power Devices Appl. in Asia (WiPDA-Asia)*, 2018, in press.
- **B. Liu**, R. Ren, Z. Zhang, F. Wang, and D. Costinett, "A Sampling Scheme for Three-Phase High Switching Frequency and Speed Converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2018, pp. 3031-3035.
- **B. Liu**, R. Ren, E. A. Jones, F. Wang, D. Costinett, and Z. Zhang, "A Modulation Compensation Scheme to Reduce Input Current Distortion in GaN Based High Switching Frequency Three-Phase Vienna Type Rectifiers," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2016, pp. 283-298.
- **B. Liu**, S. Zhang, S. Zheng, Y. W. Ma, F. Wang, and L. M. Tolbert, "Design Considerations of Converter Based Transmission Line Emulator," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2016, pp. 966-973.
- **B. Liu**, S. Zheng, Y. W. Ma, F. Wang, and L. M. Tolbert, "Control and Implementation of Converter Based Ac Transmission Line Emulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2015, pp. 1807-1814.

- **B. Liu**, X. Shi, F. Wang, and Y. Li, "A Line Impedance Conditioner to Improve Zigzag Transformer Based Hybrid Ac/Dc Transmission under Unbalanced Line Impedance Conditions," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2014, pp. 736-743.
- **B. Liu**, X. Shi, and F. Wang, "Feasibility Study and Design of Hybrid Ac-Dc High Power Transmission Considering Unbalanced Line Impedances," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, (APEC), 2014, pp. 350-357.
- R. Ren, Z. Zhang, **B. Liu**, H. Gui, et al. "Multi-Commutation Loop Induced Over-voltage in High Frequency and Switching Speed Three-Level Active Neutral Point Clamped Phase Leg," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2018, in press.
- S. Zhang, **B. Liu**, S. Zheng, Y. Ma, F. Wang, L. M. Tolbert, "Three-Phase Short-Circuit Fault Implementation in Converter Based Transmission Line Emulator," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2017, pp. 2914-2920.
- S. Zhang, Y. Li, **B. Liu**, X. Shi, F. Wang, "HVDC Converter Transformer Saturation in Hybrid AC/DC System Caused by Coupled Transmission Lines," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2017, pp. 411-415.
- R. Ren, **B. Liu**, E. A. Jones, F. Wang, Z. Zhang, D. Costinett, "Dual-output, three level GaN-based Dc-Dc converter for battery charger applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, (APEC), 2016, pp. 2441-2448.
- R. Ren, **B. Liu**, E. A. Jones, Z. Y. Zhang, F. Wang and D. Costinett, "Accurate ZVS boundary in high switching frequency LLC converter," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2016, pp. 1-6.
- E. A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, **B. Liu**, R. Ren, "Characterization of An Enhancement-Mode 650-V GaN HFET," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2015, pp. 400-407.
- Y. Li, X. Shi, **B. Liu**, F. Wang, L. M. Tolbert, W. Lei, "Hardware Implementation of a Four-terminal HVDC Test-bed," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2015, pp. 5363-5370.
- X. Shi, Z. Wang, **B. Liu**, Y. Li, L. M. Tolbert, F. Wang, "DC impedance Modelling of a MMC-HVDC System for DC Voltage Ripple Prediction under a Single-line-to-ground Fault," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2014, pp. 5339-5346.
- S. Jiang, W. Zhang, **B. Liu**, F. Wang, "Automatic Resonant Frequency Tracking in Unregulated LLC Resonant Converters Based on Total Resonant Current Harmonic Calculation," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE)*, 2013, pp. 4193-4198.

Patent

- **B. Liu**, L. M. Tolbert, K. L. Tomsovic, F. Wang, S. Zhang, “A versatile power electronics converter based transmission line emulator,” UT Invention Disclosure, 18121-03.

References

- [1] J. Wang *et al.*, "Regenerative power converters representation of grid control and actuation emulator," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 2460-2465.
- [2] "Final report on the August 14, 2003 Blackout in the United States and Canada-causes and recommendations," U.S.-Canada Power System Outage Task Force 2004, Available: <https://www.ferc.gov/industries/electric/indus-act/reliability/blackout/ch1-3.pdf>.
- [3] (2015). *Efficient Electrical Energy Transmission and Distribution*. Available: <http://www.iec.ch/about/brochures/pdf/technology/transmission.pdf>
- [4] EIA. (2016). *International Energy Outlook 2016 With Projections to 2040*. Available: www.eia.gov/forecasts/ieo
- [5] X. Lei. (2011). *State Grid Co. of China, Practice of HVDC Transmission Technology in China*. Available: http://www.forum-netzintegration.de/uploads/media/Vortrag_BlockIV_Dr.Lei.pdf
- [6] N. G. Hingorani, "Flexible AC transmission," *IEEE Spectrum*, vol. 30, no. 4, pp. 40-45, 1993.
- [7] D. Divan and H. Johal, "Distributed FACTS - A New Concept for Realizing Grid Power Flow Control," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 8-14.
- [8] D. Divan, R. Moghe, and A. Prasai, "Power Electronics at the Grid Edge : The key to unlocking value from the smart grid," *IEEE Power Electronics Magazine*, vol. 1, no. 4, pp. 16-22, 2014.
- [9] D. M. Divan *et al.*, "A Distributed Static Series Compensator System for Realizing Active Power Flow Control on Existing Power Lines," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 642-649, 2007.
- [10] L. Gyugyi, C. D. Schauder, S. L. Williams, T. R. Rietman, D. R. Torgerson, and A. Edris, "The unified power flow controller: a new approach to power transmission control," *IEEE Transactions on Power Delivery*, vol. 10, no. 2, pp. 1085-1097, 1995.
- [11] ABB. *Economic and Environmental Advantages*. Available: <http://new.abb.com/systems/hvdc/why-hvdc/economic-and-environmentaladvantages>
- [12] R. Rudervall, J. Charpentier, and R. Sharma. (2000). *High voltage direct current (HVDC) transmission systems technology review paper*. Available: www.abb.com
- [13] G. Tang, "Global Energy Interconnection Research Institute (GEIRI), "Very High Power Electronics for HVDC," in *Proc. IEEE Energy Conv. Congr*, 2016.
- [14] C. Xu. (2016). *A New Energy Network: HVDC Development in China*. Available: <http://cleanandsecuregrid.org/2017/01/02/a-new-energy-network-hvdc-development-in-china/>
- [15] O. R. Schurig, "A Miniature A-C. Transmission System For the Practical Solution of Network and Transmission-System Problems," *Transactions of the American Institute of Electrical Engineers*, vol. XLII, pp. 831-840, 1923.
- [16] R. D. Evans and R. C. Bergvall, "Experimental Analysis of Stability and Power Limitations," *Transactions of the American Institute of Electrical Engineers*, vol. XLIII, pp. 39-58, 1924.
- [17] L. Yang, "Tree-Phase Power Converter Based Real-Time Synchronous Generator Emulation," Ph.D. dissertation, University of Tennessee, Knoxville, 2015.
- [18] S. Lentijo, A. Monti, E. Santi, C. Welch, and R. Dougal, "A new testing tool for power electronic digital control," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, vol. 1, pp. 107-111 vol.1.
- [19] J. Zhenhua, R. A. Dougal, R. Leonard, H. Figueroa, and A. Monti, "Hardware-in-the-loop testing of digital power controllers," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, p. 6 pp.
- [20] S. Demers, P. Gopalakrishnan, and L. Kant, "A Generic Solution to Software-in-the-Loop," in *MILCOM 2007 - IEEE Military Communications Conference*, 2007, pp. 1-6.
- [21] Z. Weidong, S. Pekarek, J. Jatskevich, O. Wasynczuk, and D. Delisle, "A model-in-the-loop interface to emulate source dynamics in a zonal DC distribution system," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 438-445, 2005.
- [22] S. Werner, L. Masing, F. Lesniak, and J. Becker, "Software-in-the-Loop simulation of embedded control applications based on Virtual Platforms," in *2015 25th International Conference on Field Programmable Logic and Applications (FPL)*, 2015, pp. 1-8.
- [23] H. Li, M. Steurer, K. L. Shi, S. Woodruff, and D. Zhang, "Development of a Unified Design, Test, and Research Platform for Wind Energy Systems Based on Hardware-in-the-Loop Real-Time Simulation," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1144-1151, 2006.
- [24] OPAL-RT. *Hardware-in-the-Loop (HIL) simulation*. Available: <https://www.opal-rt.com/hardware-in-the-loop/>

- [25] M. D. O. Faruque *et al.*, "Real-Time Simulation Technologies for Power Systems Design, Testing, and Analysis," *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 2, pp. 63-73, 2015.
- [26] J. Mahseredjian, V. Dinavahi, and J. A. Martinez, "Simulation Tools for Electromagnetic Transients in Power Systems: Overview and Challenges," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1657-1669, 2009.
- [27] B. Liu, S. Zhang, S. Zheng, Y. Ma, F. Wang, and L. M. Tolbert, "Design consideration of converter based transmission line emulation," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 966-973.
- [28] B. Liu, S. Zheng, Y. Ma, F. Wang, and L. M. Tolbert, "Control and implementation of converter based ac transmission line emulation," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1807-1814.
- [29] Y. Ma, L. Yang, F. Wang, and L. M. Tolbert, "Short circuit fault emulation by shunt connected voltage source converter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 2622-2628.
- [30] Y. Ma, L. Yang, J. Wang, F. Wang, and L. M. Tolbert, "Emulating full-converter wind turbine by a single converter in a multiple converter based emulation system," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 3042-3047.
- [31] J. Wang *et al.*, "Static and Dynamic Power System Load Emulation in a Converter-Based Reconfigurable Power Grid Emulator," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3239-3251, 2016.
- [32] J. Wang *et al.*, "Static and dynamic power system load emulation in converter-based reconfigurable power grid emulator," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4008-4015.
- [33] L. Yang *et al.*, "Development of converter based reconfigurable power grid emulator," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 3990-3997.
- [34] L. Yang *et al.*, "Three-Phase Power Converter-Based Real-Time Synchronous Generator Emulation," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1651-1665, 2017.
- [35] L. Yang *et al.*, "Stability analysis of inverter based generator emulator in test-bed for power systems," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 5410-5417.
- [36] Y. Ma, J. Wang, F. Wang, and L. M. Tolbert, "Converter-based reconfigurable real-time electrical system emulation platform," *Chinese Journal of Electrical Engineering*, vol. 4, no. 1, pp. 20-27, 2018.
- [37] A. Hilal, B. Cougo, and T. Meynard, "Characterization of high power SiC modules for more Electrical Aircrafts," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 1087-1092.
- [38] Y. Jia and K. Rajashekara, "An Induction Generator-Based AC/DC Hybrid Electric Power Generation System for More Electric Aircraft," *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2485-2494, 2017.
- [39] V. Madonna, P. Giangrande, and M. Galea, "Electrical Power Generation in Aircraft: review, challenges and opportunities," *IEEE Transactions on Transportation Electrification*, pp. 1-1, 2018.
- [40] B. Sarlioglu and C. T. Morris, "More Electric Aircraft: Review, Challenges, and Opportunities for Commercial Transport Aircraft," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54-64, 2015.
- [41] S. Choi, P. N. Enjeti, and I. J. Pitel, "Polyphase transformer arrangements with reduced kVA capacities for harmonic current reduction in rectifier-type utility interface," *IEEE Transactions on Power Electronics*, vol. 11, no. 5, pp. 680-690, 1996.
- [42] A. Uan-Zo-li, R. Burgos, F. Lacaux, A. Roshan, F. Wang, and D. Boroyevich, "Analysis of New Step-up and Step-down Direct Symmetric 18-pulse Topologies for Aircraft Autotransformer-Rectifier Units," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 1142-1148.
- [43] M. Hartmann, "Ultra-Compact and Ultra-Efficient Three-Phase PWM Rectifier Systems for More Electric Aircraft," Ph.D. Dissertation, ETH Zurich, Zurich, Switzerland, 2011.
- [44] J. Bourdon, P. Asfaux, and A. M. Etayo, "Review of power electronics opportunities to integrate in the more electrical aircraft," in *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, 2015, pp. 1-6.
- [45] J. S. N. T. Magambo *et al.*, "Planar Magnetic Components in More Electric Aircraft: Review of Technology and Key Parameters for DC-DC Power Electronic Converter," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 4, pp. 831-842, 2017.
- [46] C. A. Clarke and W. E. Larse, "Aircraft Electromagnetic Compatibility," Boeing Commercial Airplane Company, FAA Technical Field Office DOT/FAA/CT-86/40, 1987.

- [47] (1995). 1374, *Electronic Systems Failures and Anomalies Attributed to Electromagnetic Interference*. Available: <https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/19960009442.pdf>
- [48] R. Prasad, "The role of EMI/EMC testing in the development of aerospace systems," in *Electromagnetic Interference and Compatibility '97. Proceedings of the International Conference on*, 1997, pp. 133-140.
- [49] ABB. *HVDC Light®-It's time to connect*. Available: <https://new.abb.com/docs/default-source/ewea-doc/hvdc-light.pdf>
- [50] L. P. Lazaridis, "Economic Comparison of HVAC and HVD Solutions for Large Offshore Wind Farms under Special Consideration of Reliability," M.S., Royal Institute of Technology, Stockholm, 2005.
- [51] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson. (2012). *The Hybrid HVDC Breaker-An innovation breakthrough enabling reliable HVDC grids* Available: https://new.abb.com/docs/default-source/default-document-library/hybrid-hvdc-breaker---an-innovation-breakthrough-for-reliable-hvdc-gridsnov2012finmc20121210_clean.pdf
- [52] J. Häfner and B. Jacobson, "Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids," in *The Electric Power System of the Future: Integrating Supergrids and Microgrids, CIGRE Symposium*, 2011.
- [53] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical Assessment of Load Commutation Switch in Hybrid HVDC Breaker," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5393-5400, 2015.
- [54] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 502-507.
- [55] G. P. Adam, S. J. Finney, and B. W. Williams, "Enhanced control strategy of full-bridge modular multilevel converter," in *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, 2015, pp. 1432-1436.
- [56] T. Jonsson, P. Lundberg, S. Maiti, and Y. J. Hafner, "Converter Technologies and Functional Requirements for Reliable and Economical HVDC Grid Design," in *Cigre2013*, Alberta, Canada, 2013.
- [57] J. R. Svensson. (2014). *ABB's HVDC and SVC Light - technology and applications*.
- [58] S. Abraham. (2002, May). *National Transmission Grid Study*. Available: <http://www.eh.doe.gov/ntgs/>
- [59] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592-602, 2009.
- [60] J. D. McCalley and V. Krishnan, "A survey of transmission technologies for planning long distance bulk transmission overlay in US," *International Journal of Electrical Power & Energy Systems*, vol. 54, pp. 559-568, 2014/01/01/ 2014.
- [61] R. Gutman, P. P. Marchenko, and R. D. Dunlop, "Analytical Development of Loadability Characteristics for EHV and UHV Transmission Lines," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-98, no. 2, pp. 606-617, 1979.
- [62] "Increasing capacity of overhead transmission lines-needs and solutions," in *Cigré*, 2010.
- [63] K. P. Basu and H. Rahman, "Feasibility Study of Conversion of Double Circuit ac Transmission Line for Simultaneous ac-dc Power Transmission," in *2005 International Conference on Power Electronics and Drives Systems*, 2005, vol. 2, pp. 972-976.
- [64] R. Lucas, N. Pahalawaththa, U. Annakkage, and J. Boys, "ac — Small power dc hybrid transmission for improving power system stability," *Electric Power Systems Research*, vol. 56, no. 1, pp. 9-15, 2000/10/05/ 2000.
- [65] H. Rahman and B. H. Khan, "Enhanced power transfer by simultaneous transmission of AC-DC: A new facts concept," in *Second International Conference on Power Electronics, Machines and Drives (PEMD 2004)*, 2004, vol. 1, pp. 186-191 Vol.1.
- [66] H. Rahman and B. H. Khan, "Power upgrading by simultaneous AC-DC power transfer in a double circuit AC line," in *2006 IEEE Power India Conference*, 2006, p. 7 pp.
- [67] B. Liu, X. Shi, and F. Wang, "Feasibility study and design of hybrid AC/DC high power transmission considering unbalanced line impedances," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 350-357.
- [68] A. Clerici, L. Paris, and P. Danfors, "HVDC conversion of HVAC lines to provide substantial power upgrading," *IEEE Transactions on Power Delivery*, vol. 6, no. 1, pp. 324-333, 1991.
- [69] A. A. Edris, L. O. Barthold, P. A. Douglas, W. H. Litzenberger, and D. A. Woodford, "Upgrading AC transmission to DC for maximum power transfer capacity," in *12th International Middle East Power System Conference*, Aswan, 2008, pp. 44-49.

- [70] K. Halsan, D. Loudon, I. Gutman, and J. Lundquist, "Feasibility of upgrading 300 kV AC lines to DC for increased power transmission capability," in *Cigre* 2008.
- [71] J. Lundkvist, I. Gutman, and L. Weimers, "Feasibility study for converting 380 kV AC lines to hybrid AC / DC lines," in *EPRI's High-Voltage Direct Current & Flexible AC Transmission Systems*, 2009.
- [72] A. Dernfalk, J. Lundquist, and I. Gutman. (2016). *Typical Approach & Case Studies of DC Insulator Dimensioning for AC to DC Line Conversion*. Available: <http://www.inmr.com/typical-approach-case-studies-insulator-dimensioning-line-conversion/>
- [73] R. Adapa, "DC Capability of AC Transmission Lines," Dec. 2008.
- [74] "GUIDE TO THE CONVERSION OF EXISTING AC LINES TO DC OPERATION," CIGRE Working Group B2.412014.
- [75] D. M. Larruskain, I. Zamora, O. Abarrategui, and A. Iturregi, "VSC-HVDC configurations for converting AC distribution lines into DC lines," *International Journal of Electrical Power & Energy Systems*, vol. 54, pp. 589-597, 2014/01/01/ 2014.
- [76] L. Yang *et al.*, "Hardware implementation and control design of generator emulator in multi-converter system," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2316-2323.
- [77] J. Wang, Y. Ma, L. Yang, L. M. Tolbert, and F. Wang, "Power converter-based three-phase induction motor load emulator," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 3270-3274.
- [78] W. Cao *et al.*, "Two-stage PV inverter system emulator in converter based power grid emulation system," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4518-4525.
- [79] J. Wang, L. Yang, C. Blalock, and L. M. Tolbert, "Flywheel Energy Storage Emulation Using Reconfigurable Hardware Test-bed of Power Converters," in *Proc. Elect. Energy Storage Appl. Technol.*, 2013.
- [80] J. D. Boles, Y. Ma, W. Cao, L. M. Tolbert, and F. Wang, "Battery energy storage emulation in a converter-based power system emulator," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2355-2362.
- [81] S. Zhang, Y. Ma, L. Yang, F. Wang, and L. M. Tolbert, "Development of a hybrid emulation platform based on RTDS and reconfigurable power converter-based testbed," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 3121-3127.
- [82] Y. Li, X. Shi, B. Liu, W. Lei, F. Wang, and L. M. Tolbert, "Development, Demonstration, and Control of a Testbed for Multiterminal HVDC System," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6069-6078, 2017.
- [83] S. Zhang, B. Liu, S. Zheng, Y. Ma, F. Wang, and L. M. Tolbert, "Three-phase short-circuit fault implementation in converter based transmission line emulator," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2914-2920.
- [84] S. Grubic, B. Amlang, W. Schumacher, and A. Wenzel, "A High-Performance Electronic Hardware-in-the-Loop Drive-Load Simulation Using a Linear Inverter (LinVerter)," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1208-1216, 2010.
- [85] A. G. Jack, D. J. Atkinson, and H. J. Slater, "Real-time emulation for power equipment development. I. Real-time simulation," *IEE Proceedings - Electric Power Applications*, vol. 145, no. 2, pp. 92-97, 1998.
- [86] S. Lentijo, S. D. Arco, and A. Monti, "Comparing the Dynamic Performances of Power Hardware-in-the-Loop Interfaces," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1195-1207, 2010.
- [87] H. J. Slater, D. J. Atkinson, and A. G. Jack, "Real-time emulation for power equipment development. II. The virtual machine," *IEE Proceedings - Electric Power Applications*, vol. 145, no. 3, pp. 153-158, 1998.
- [88] M. Steurer, C. S. Edrington, M. Sloderbeck, W. Ren, and J. Langston, "A Megawatt-Scale Power Hardware-in-the-Loop Simulation Setup for Motor Drives," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1254-1260, 2010.
- [89] D. V. Terlip, B. Kroposki, and D. Maksimovic, "A methodology for characterizing and modeling inverters for grid integration studies using Power Hardware-in-the-Loop," in *2012 IEEE Power and Energy Society General Meeting*, 2012, pp. 1-5.
- [90] W. Ren, M. Steurer, and T. L. Baldwin, "Improve the stability and the accuracy of power hardware-in-the-loop simulation by selecting appropriate interface algorithms," (in English), *Ieee Transactions on Industry Applications*, vol. 44, no. 4, pp. 1286-1294, Jul-Aug 2008.
- [91] R. Kuffel *et al.*, "Expanding an Analogue HVDC Simulator's Modelling Capability Using a Real-Time Digital Simulator (RTDS)," in *Digital Power System Simulators, 1995, ICDS '95., First International Conference on*, 1995, p. 199.

- [92] O. R. Schurig, "A miniature A-C. transmission system: For the practical solution of network and transmission-system problems," *Journal of the American Institute of Electrical Engineers*, vol. 42, no. 10, pp. 1033-1040, 1923.
- [93] S. C. Verma, H. Odani, S. Ogawa, K. Kuroda, and Y. Kono, "Real time interface for interconnecting fully digital and analog simulators using short line or transformer," in *2006 IEEE Power Engineering Society General Meeting*, 2006, p. 7 pp.
- [94] X. Wu, S. Lentijo, and A. Monti, "A novel interface for power-hardware-in-the-loop simulation," in *2004 IEEE Workshop on Computers in Power Electronics, 2004. Proceedings.*, 2004, pp. 178-182.
- [95] V. B. Dmitriev-Zdorov, "Generalized coupling as a way to improve the convergence in relaxation-based solvers," in *Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European*, 1996, pp. 15-20.
- [96] C. A. Thompson, "A study of numerical integration techniques for use in the companion circuit method of transient circuit analysis," Purdue Univ. , West Lafayette, IN Apr. 1992 1992.
- [97] A. P. S. Meliopoulos, *Power System Grounding and Transients: An Introduction*. New York: CRC Press, 1998.
- [98] T. Hwang *et al.*, "Development of HILS Systems for Active Brake Control Systems," in *2006 SICE-ICASE International Joint Conference*, 2006, pp. 4404-4408.
- [99] R. Burgos, D. Boroyevich, F. Wang, K. Karimi, and G. Francis, "On the Ac stability of high power factor three-phase rectifiers," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 2047-2054.
- [100] M. Belkhat, "Stability criteria for AC power systems with regulated loads," Ph.D. dissertation, School Electr. Comp. Eng., Purdue Univ., 1997.
- [101] B. Wen, D. Boroyevich, P. Mattavelli, Z. Shen, and R. Burgos, "Experimental verification of the Generalized Nyquist stability criterion for balanced three-phase ac systems in the presence of constant power loads," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 3926-3933.
- [102] B. Wen, D. Boroyevich, P. Mattavelli, Z. Shen, and R. Burgos, "Influence of phase-locked loop on input admittance of three-phase voltage-source converters," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 897-904.
- [103] Z. Xuan, F. Wang, W. Cao, and Y. Ma, "Influence of voltage feed-forward control on small-signal stability of grid-tied inverters," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1216-1221.
- [104] Y. Gu, W. Li, and X. He, "Passivity-Based Control of DC Microgrid for Self-Disciplined Stabilization," *IEEE Transactions on Power Systems*, vol. 30, no. 5, pp. 2623-2632, 2015.
- [105] L. Harnefors, X. Wang, A. G. Yepes, and F. Blaabjerg, "Passivity-Based Stability Assessment of Grid-Connected VSCs; An Overview," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 116-125, 2016.
- [106] X. Wang, F. Blaabjerg, and P. C. Loh, "An impedance-based stability analysis method for paralleled voltage source converters," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 1529-1535.
- [107] W. Cao, Y. Ma, and F. Wang, "Sequence-Impedance-Based Harmonic Stability Analysis and Controller Parameter Design of Three-Phase Inverter-Based Multibus AC Power Systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7674-7693, 2017.
- [108] W. Cao, Y. Ma, L. Yang, F. Wang, and L. M. Tolbert, "D-Q Impedance Based Stability Analysis and Parameter Design of Three-Phase Inverter-Based AC Power Systems," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 6017-6028, 2017.
- [109] K. Strunz, "Flexible numerical integration for efficient representation of switching in real time electromagnetic transients Simulation," *IEEE Transactions on Power Delivery*, vol. 19, no. 3, pp. 1276-1283, 2004.
- [110] A. Iserles, *A First Course in the Numerical Analysis of Differential Equations*. New York, NY: Cambridge Univ. Press, 2009.
- [111] H. E. Jordan, "Digital Computer Analysis of Induction Machines in Dynamic Systems," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-86, no. 6, pp. 722-728, 1967.
- [112] H. Saadat, *Power System Analysis*, 2nd ed. McGraw-Hill, 2002.
- [113] A. Ametani, "The history and recent trends of transient analysis in transmission lines," in *Conf. IPST2013*, Vancouver, Canada, 2013.
- [114] L. V. Bewley, *Travelling-Waves on Transmission Systems*. Wiley, 1951.

- [115] J. L. R. d'Alembert, "Investigation of the curve formed by a vibrating string, 1747," in *Acoustics: Historical and Philosophical Development*, R. B. Lindsay, Ed. Stroudsburg, PA: Dowden, Hutchinson & Ross, 1973, pp. 119-123.
- [116] A. Sommerferd, *Partial Differential Equations in Physics*. Academic Press, 1964.
- [117] H. W. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single-and Multiphase Networks," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-88, no. 4, pp. 388-399, 1969.
- [118] M. Z. Daud, "Transient behaviour modelling of underground high voltage cable systems," M.S., Dept. Elect. Comp. and Telec. Eng. , Univ. Wollongong, Australia, 2009.
- [119] J. R. Marti, "Accurate Modelling of Frequency-Dependent Transmission Lines in Electromagnetic Transient Simulations," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-101, no. 1, pp. 147-157, 1982.
- [120] L. Marti, "Simulation of transients in underground cables with frequency-dependent modal transformation matrices," *IEEE Transactions on Power Delivery*, vol. 3, no. 3, pp. 1099-1110, 1988.
- [121] A. Semlyen and A. Dabuleanu, "Fast and accurate switching transient calculations on transmission lines with ground return using recursive convolutions," *IEEE Transactions on Power Apparatus and Systems*, vol. 94, no. 2, pp. 561-571, 1975.
- [122] M. H. I. Ltd. (2018). *EMTDC User's Guide v4.6: Transient Analysis for PSCAD Power System Simulation*. Available: <https://hvdc.ca/knowledge-base/read/article/163/emtdc-user-s-guide-v4-6/v>:
- [123] A. Morched, B. Gustavsen, and M. Tartibi, "A universal model for accurate calculation of electromagnetic transients on overhead lines and underground cables," *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 1032-1038, 1999.
- [124] T. Noda, N. Nagaoka, and A. Ametani, "Phase domain modeling of frequency-dependent transmission lines by means of an ARMA model," *IEEE Transactions on Power Delivery*, vol. 11, no. 1, pp. 401-411, 1996.
- [125] J. P. Bickford and M. H. Abdel-Rahman, "Application of travelling-wave methods to the calculation of transient-fault currents and voltages in power-system networks," *IEE Proceedings C - Generation, Transmission and Distribution*, vol. 127, no. 3, pp. 153-168, 1980.
- [126] Matlab. *PI Section Line*. Available: <https://www.mathworks.com/help/physmod/sps/powersys/ref/pisectionline.html>
- [127] U. Drofenik and J. W. Kolar, "Comparison of not synchronized sawtooth carrier and synchronized triangular carrier phase current control for the VIENNA rectifier I," in *Industrial Electronics, 1999. ISIE '99. Proceedings of the IEEE International Symposium on*, 1999, vol. 1, pp. 13-19 vol.1.
- [128] D. M. V. d. Sype, K. D. Gusseme, A. P. V. d. Bossche, and J. A. A. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 649-657, 2004.
- [129] D. M. V. d. Sype, K. D. Gusseme, A. R. V. d. Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, vol. 6, pp. 4299-4305 Vol.6.
- [130] Y. Ma, L. Yang, J. Wang, X. Shi, F. Wang, and L. M. Tolbert, "Circulating current control and reduction in a paralleled converter test-bed system," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 5426-5432.
- [131] D. Stojić, M. Milinković, S. Veinović, and I. Klasnić, "Improved Stator Flux Estimator for Speed Sensorless Induction Motor Drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2363-2371, 2015.
- [132] M. Comanescu and L. Xu, "An improved flux observer based on PLL frequency estimator for sensorless vector control of induction motors," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 1, pp. 50-56, 2005.
- [133] N. R. N. Idris and A. H. M. Yatim, "An improved stator flux estimation in steady-state operation for direct torque control of induction machines," *IEEE Transactions on Industry Applications*, vol. 38, no. 1, pp. 110-116, 2002.
- [134] M. Hinkkanen and J. Luomi, "Modified integrator for voltage model flux estimation of induction motors," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 4, pp. 818-820, 2003.
- [135] J. Hu and B. Wu, "New integration algorithms for estimating motor flux over a wide speed range," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 969-977, 1998.
- [136] Y. Wang and Z. Deng, "Improved Stator Flux Estimation Method for Direct Torque Linear Control of Parallel Hybrid Excitation Switched-Flux Generator," *IEEE Transactions on Energy Conversion*, vol. 27, no. 3, pp. 747-756, 2012.

- [137] C. Lascu and G. D. Andreescu, "Sliding-mode observer and improved integrator with DC-offset compensation for flux estimation in sensorless-controlled induction motors," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 3, pp. 785-794, 2006.
- [138] A. Uan-Zo-li, R. Burgos, F. Wang, D. Boroyevich, F. Lacaux, and A. Tardy, "Comparison of prospective topologies for aircraft autotransformer-rectifier units," in *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, 2003, vol. 2, pp. 1122-1127 Vol.2.
- [139] R. Lai *et al.*, "A Systematic Topology Evaluation Methodology for High-Density Three-Phase PWM AC-AC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2665-2680, 2008.
- [140] K. M. J. Krishna and V. John, "Comparison of 3-phase, 3-level UPF rectifier circuits for high power applications," in *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2012, pp. 1-6.
- [141] J. Minibock and J. W. Kolar, "Comparative theoretical and experimental evaluation of bridge leg topologies of a three-phase three-level unity power factor rectifier," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, 2001, vol. 3, pp. 1641-1646 vol. 3.
- [142] Q. Wang, B. Wen, R. Burgos, D. Boroyevich, and A. White, "Efficiency evaluation of two-level and three-level bridgeless PFC boost rectifiers," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1909-1915.
- [143] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. M. White, and M. Kheraluwala, "Design and Implementation of a Two-Channel Interleaved Vienna-Type Rectifier With >99% Efficiency," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 226-239, 2018.
- [144] J. W. Kolar and T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems—Part I," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176-198, 2013.
- [145] A. S. Babokany, M. Jabbari, G. Shahgholian, and M. Mahdavian, "A review of bidirectional dual active bridge converter," in *2012 9th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, 2012, pp. 1-4.
- [146] J. M. Zhang, X. G. Xie, X. K. Wu, and Q. Zhaoming, "Comparison study of phase-shifted full bridge ZVS converters," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, vol. 1, pp. 533-539 Vol.1.
- [147] W. Zhang, Z. Xu, Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Evaluation of 600 V cascode GaN HEMT in device characterization and all-GaN-based LLC resonant converter," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 3571-3578.
- [148] X. Ruan, B. Li, Q. Chen, S. C. Tan, and C. K. Tse, "Fundamental Considerations of Three-Level DC-DC Converters: Topologies, Analyses, and Control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3733-3743, 2008.
- [149] X. Ruan, L. Zhou, and Y. Yan, "Soft-switching PWM three-level converters," *IEEE Transactions on Power Electronics*, vol. 16, no. 5, pp. 612-622, 2001.
- [150] H. Sheng, F. Wang, and C. W. T. IV, "A Fault Detection and Protection Scheme for Three-Level DC-DC Converters Based on Monitoring Flying Capacitor Voltage," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 685-697, 2012.
- [151] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. White, and M. Kheraluwala, "Design and implementation of interleaved Vienna rectifier with greater than 99% efficiency," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 72-78.
- [152] A. Mallik and A. Khaligh, "Intermediate DC-Link Capacitor Reduction in a Two-Stage Cascaded AC/DC Converter for More Electric Aircrafts," *IEEE Transactions on Vehicular Technology*, vol. 67, no. 2, pp. 935-947, 2018.
- [153] A. Mallik and A. Khaligh, "Maximum Efficiency Tracking of an Integrated Two-Stage AC–DC Converter Using Variable DC-Link Voltage," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8408-8421, 2018.
- [154] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, 2016.
- [155] M. Hartmann, H. Ertl, and J. W. Kolar, "On the Tradeoff Between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3137-3149, 2012.

- [156] B. Liu, R. Ren, E. Jones, F. Wang, D. Costinett, and Z. Zhang, "A compensation scheme to reduce input current distortion in a GaN based 450 kHz three-phase Vienna type PFC," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-7.
- [157] B. Liu, R. Ren, E. A. Jones, F. Wang, D. Costinett, and Z. Zhang, "A Modulation Compensation Scheme to Reduce Input Current Distortion in GaN-Based High Switching Frequency Three-Phase Three-Level Vienna-Type Rectifiers," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 283-298, 2018.
- [158] R. Lai, "Analysis and Design for a High Power Density Three-phase AC Converter Using SiC Devices," Ph. D. Dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, 2008.
- [159] H. Li *et al.*, "Design of a 10 kW GaN-based high power density three-phase inverter," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-8.
- [160] C. Zhao *et al.*, "Design and Implementation of a GaN-Based, 100-kHz, 102-W/in³ Single-Phase Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 824-840, 2016.
- [161] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1977-1985, 2014.
- [162] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1561-1568.
- [163] G. Systems. *PCB Thermal Design Guide for GaN Enhancement Mode Power Transistors*. Available: https://gansystems.com/wp-content/uploads/2018/01/GN005_PCB-Thermal-Design-Guide-Enhancement-Mode-031815.pdf
- [164] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Cross conduction analysis for enhancement-mode 650-V GaN HFETs in a phase-leg topology," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 98-103.
- [165] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An Analytical Model for False Turn-On Evaluation of High-Voltage Enhancement-Mode GaN Transistor in Bridge-Leg Configuration," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6416-6433, 2017.
- [166] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. on Power Electronics*, vol. 29, no. 4, pp. 1986-1997, 2014.
- [167] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 774-781.
- [168] Semisouth. *Silicon carbide enhancement-mode junction field effect transistor and recommendations for use*. Available: <http://www.semisouth.com>
- [169] A. Technologies. *Active Miller clamp*. Available: <http://www.avagotech.com>
- [170] Z. Zhang, J. Dix, F. Wang, B. Blalock, D. Costinett, and L. Tolbert, "Intelligent gate drive for fast switching and cross-talk suppression of SiC devices," *IEEE Trans. on Power Electronics*, vol. PP, no. 99, pp. 1-1, 2017.
- [171] SiliconLabs. (2015). *Si827x datasheet*. Available: <http://www.silabs.com/products/power/isodrivers/>
- [172] *Limits for harmonic current emissions (equipment input current ≤16 A per phase)*, 61000-3-2, 2014.
- [173] IEEE Standards Association. (2014). *IEEE 519-2014*. Available: <http://standards.ieee.org>
- [174] RTCA/DO-160 E. (2004, Dec., 2004). *Environmental Conditions and Test Procedures for Airborne Equipment*.
- [175] Intel. (2009, September). *Voltage Regulator-Down 11.1: Processor Power Delivery Design Guidelines*. Available: <https://www.intel.com/content/www/us/en/power-management/voltage-regulator-down-11-1-processor-power-delivery-guidelines.html>
- [176] XP Power. *Power Supply Technical Guide 2010/11, Technical Notes*.
- [177] M. Biglarbegian, S. J. Nibir, H. Jafarian, J. Enslin, and B. Parkhideh, "Layout study of contactless magnetoresistor current sensor for high frequency converters," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-5.
- [178] L. Xue, D. Boroyevich, and P. Mattavelli, "Driving and sensing design of an enhancement-mode-GaN phaseleg as a building block," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 34-40.
- [179] N. Bedetti, S. Calligaro, and R. Petrella, "Self-Commissioning of Inverter Dead-Time Compensation by Multiple Linear Regression Based on a Physical Model," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 3954-3964, 2015.

- [180] S. H. Hwang and J. M. Kim, "Dead Time Compensation Method for Voltage-Fed PWM Inverter," *IEEE Transactions on Energy Conversion*, vol. 25, no. 1, pp. 1-10, 2010.
- [181] C. Jong-Woo and S. Seung-Ki, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Transactions on Industry Applications*, vol. 31, no. 5, pp. 1001-1008, 1995.
- [182] D. Leggate and R. J. Kerkman, "Pulse-based dead-time compensator for PWM voltage inverters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 2, pp. 191-197, 1997.
- [183] Z. Zhang and L. Xu, "Dead-Time Compensation of Inverters Considering Snubber and Parasitic Capacitance," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 3179-3187, 2014.
- [184] B. Guo *et al.*, "Compensation of input current distortion in three-phase buck rectifiers," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 930-938.
- [185] C. Li *et al.*, "Analysis and compensation of dead-time effect considering parasitic capacitance and ripple current," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1501-1506.
- [186] E. A. Jones *et al.*, "Characterization of an enhancement-mode 650-V GaN HFET," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 400-407.
- [187] F. Wang, Z. Zhang, T. Ericson, R. Raju, R. Burgos, and D. Boroyevich, "Advances in Power Conversion and Drives for Shipboard Systems," *Proceedings of the IEEE*, vol. 103, no. 12, pp. 2285-2311, 2015.
- [188] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Harmonics mitigation of dead time effects in PWM converters using a repetitive controller," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1479-1486.
- [189] J. Yuan *et al.*, "An Immune-Algorithm-Based Dead-Time Elimination PWM Control Strategy in a Single-Phase Inverter," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3964-3975, 2015.
- [190] "Engineering practice study, results of detailed comparisons of Individual EMC requirements and test procedures delineated in major national and international commercial standards with military standard MIL-STD-461E," DoD/Industry Electromagnetic Environmental Effects Standards Committee Mar. 2001 2001.
- [191] P. D. Ewing and R. T. Wood, "Comparison of U.S. military and international electromagnetic compatibility guidance," Oak Ridge National Laboratory Aug. 2003 2003.
- [192] K. Mainali and R. Oruganti, "Conducted EMI Mitigation Techniques for Switch-Mode Power Converters: A Survey," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2344-2356, 2010.
- [193] R. Wang, H. F. Blanchette, D. Boroyevich, and P. Mattavelli, "EMI noise attenuation prediction with mask impedance in motor drive system," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2279-2284.
- [194] S. Bingyao and R. Burgos, "Assessment of switching frequency impact on the prediction capability of common-mode EMI emissions of sic power converters using unterminated behavioral models," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1153-1160.
- [195] B. Sun, R. Burgos, X. Zhang, and D. Boroyevich, "Differential-mode EMI emission prediction of SiC-based power converters using a mixed-mode unterminated behavioral model," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 4367-4374.
- [196] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI Filter Design for a 1 MHz, 10 kW Three-Phase/Level PWM Rectifier," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1192-1204, 2011.
- [197] D. Jiang, Z. Shen, and F. "Common-Mode Voltage Reduction for Paralleled Inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3961-3974, 2018.
- [198] Z. Shen, D. Jiang, J. Chen, and R. Qu, "Circulating Current Reduction for Paralleled Inverters With Modified Zero-CM PWM Algorithm," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3518-3528, 2018.
- [199] K. Borisov, H. L. Ginn, and A. M. Trzynadlowski, "Attenuation of Electromagnetic Interference in a Shunt Active Power Filter," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1912-1918, 2007.
- [200] J. Chen, D. Jiang, and X. Zhao, "A comprehensive investigation on conducted EMI reduction for variable switching frequency PWM," in *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, 2018, pp. 121-126.
- [201] D. Gonzalez *et al.*, "Conducted EMI Reduction in Power Converters by Means of Periodic Switching Frequency Modulation," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2271-2281, 2007.
- [202] D. Jiang and F. Wang, "Variable Switching Frequency PWM for Three-Phase Converters Based on Current Ripple Prediction," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4951-4961, 2013.

- [203] S. Kaboli, J. Mahdavi, and A. Agah, "Application of Random PWM Technique for Reducing the Conducted Electromagnetic Emissions in Active Filters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2333-2343, 2007.
- [204] M. Kuisma and P. Silventoinen, "Analyzing Current Ripple in Variable-Frequency Boost Converter," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 1535-1540.
- [205] Q. Li and D. Jiang, "Variable Switching Frequency PWM Strategy of Two-Level Rectifier for DC-Link Voltage Ripple Control," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7193-7202, 2018.
- [206] F. Mihali and D. Kos, "Reduced Conductive EMI in Switched-Mode DC-DC Power Converters Without EMI Filters: PWM Versus Randomized PWM," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1783-1794, 2006.
- [207] O. Trescases, G. Wei, and W. T. Ng, "A low-power DC-DC converter with digital spread spectrum for reduced EMI," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1-7.
- [208] O. Trescases, G. Wei, A. Prodic, and W. T. Ng, "An EMI Reduction Technique for Digitally Controlled SMPS," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1560-1565, 2007.
- [209] Z. Wang and K. T. Chau, "Design and Analysis of a Chaotic PWM Inverter for Electric Vehicles," in *2007 IEEE Industry Applications Annual Meeting*, 2007, pp. 1954-1961.
- [210] J. Mon, J. Gago, D. Gonzalez, J. Balcells, R. Fernandez, and I. Gil, "Reduction of EMI by combining interleaving and modulation techniques in multiconverter topology," in *2009 Compatibility and Power Electronics*, 2009, pp. 353-358.
- [211] X. Zhang, D. Boroyevich, and R. Burgos, "Impact of interleaving on common-mode EMI filter weight reduction of paralleled three-phase voltage-source converters," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 1669-1675.
- [212] X. Zhang, P. Mattavelli, D. Boroyevich, and F. Wang, "Impact of interleaving on EMI noise reduction of paralleled three phase voltage source converters," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2487-2492.
- [213] P. Zumel, O. Garcia, J. A. Cobos, and J. Uceda, "Exploring interleaved converters as an EMI reduction technique in power converters," in *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*, 2002, vol. 2, pp. 1219-1224 vol.2.
- [214] P. Zumel, O. Garcia, J. A. Cobos, and J. Uceda, "EMI reduction by interleaving of power converters," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, 2004, vol. 2, pp. 688-694 vol.2.
- [215] D. Han, W. Lee, S. Li, and B. Sarlioglu, "New Method for Common Mode Voltage Cancellation in Motor Drives: Concept, Realization, and Asymmetry Influence," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1188-1201, 2018.
- [216] D. Han, C. T. Morris, and B. Sarlioglu, "Common-Mode Voltage Cancellation in PWM Motor Drives With Balanced Inverter Topology," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2683-2688, 2017.
- [217] C. T. Morris, D. Han, and B. Sarlioglu, "Reduction of Common Mode Voltage and Conducted EMI Through Three-Phase Inverter Topology," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1720-1724, 2017.
- [218] X. Gong and J. A. Ferreira, "Comparison and Reduction of Conducted EMI in SiC JFET and Si IGBT-Based Motor Drives," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1757-1767, 2014.
- [219] D. Han, S. Li, Y. Wu, W. Choi, and B. Sarlioglu, "Comparative Analysis on Conducted CM EMI Emission of Motor Drives: WBG Versus Si Devices," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8353-8363, 2017.
- [220] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "A Case Study on Common Mode Electromagnetic Interference Characteristics of GaN HEMT and Si MOSFET Power Converters for EV/HEVs," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 1, pp. 168-179, 2017.
- [221] T. Kim, D. Feng, M. Jang, and V. G. Agelidis, "Common Mode Noise Analysis for Cascaded Boost Converter With Silicon Carbide Devices," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1917-1926, 2017.
- [222] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2393-2407, 2014.
- [223] M. Kovacic, Z. Hanic, S. Stipetic, S. Krishnamurthy, and D. Zarko, "Analytical Wideband Model of a Common-Mode Choke," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3173-3185, 2012.

- [224] J. Kuipers, H. Bruning, D. Yntema, S. Bakker, and H. Rijnaarts, "Self-Capacitance and Resistive Losses of Saline-Water-Filled Inductors," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2356-2361, 2014.
- [225] A. Massarini and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Transactions on Power Electronics*, vol. 12, no. 4, pp. 671-676, 1997.
- [226] S. W. Pasko, M. K. Kazimierczuk, and B. Grzesik, "Self-Capacitance of Coupled Toroidal Inductors for EMI Filters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 2, pp. 216-223, 2015.
- [227] Q. Yu and T. W. Holmes, "Stray capacitance modeling of inductors by using the finite element method," in *1999 IEEE International Symposium on Electromagnetic Compatibility. Symposium Record (Cat. No.99CH36261)*, 1999, vol. 1, pp. 305-310 vol.1.
- [228] J. Biela and J. W. Kolar, "Cooling Concepts for High Power Density Magnetic Devices," in *2007 Power Conversion Conference - Nagoya*, 2007, pp. 1-8.
- [229] A. Stadler, T. Stolzke, and C. Gulden, "Design and Simulation of High Power Filter Inductors with Minimized Thermal Resistance," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1-7.
- [230] H. Chen and Z. Qian, "Modeling and Characterization of Parasitic Inductive Coupling Effects on Differential-Mode EMI Performance of a Boost Converter," *IEEE Transactions on Electromagnetic Compatibility*, vol. 53, no. 4, pp. 1072-1080, 2011.
- [231] A. Eroglu, "Complete Modeling of Toroidal Inductors for High Power RF Applications," *IEEE Transactions on Magnetics*, vol. 48, no. 11, pp. 4526-4529, 2012.
- [232] M. L. Heldwein, L. Dalessandro, and J. W. Kolar, "The Three-Phase Common-Mode Inductor: Modeling and Design Issues," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3264-3274, 2011.
- [233] M. Illia, L. Koleff, and G. Griepentrog, "Non-ideal model of the common mode choke for EMI filters," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 938-944.
- [234] V. Jithesh and D. C. Pande, "A review on computational EMI modelling techniques," in *8th International Conference on Electromagnetic Interference and Compatibility*, 2003, pp. 159-166.
- [235] J. L. Kotny, X. Margueron, and N. Idir, "High-Frequency Model of the Coupled Inductors Used in EMI Filters," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2805-2812, 2012.
- [236] F. Sixdenier, O. Yade, C. Martin, A. Bréard, and C. Vollaie, "How to include frequency dependent complex permeability Into SPICE models to improve EMI filters design?," *AIP Advances*, vol. 8, no. 5, May 2018.
- [237] Y. Liu, K. Y. See, and K. J. Tseng, "Conducted EMI Prediction of the PFC Converter Including Nonlinear Behavior of Boost Inductor," *IEEE Transactions on Electromagnetic Compatibility*, vol. 55, no. 6, pp. 1107-1114, 2013.
- [238] V. Ionita, B. Cranganu-Cretu, and A. Ionita, "Object-oriented software for advanced characterization of magnetic materials," *IEEE Transactions on Magnetics*, vol. 38, no. 2, pp. 1101-1104, 2002.
- [239] J. Watson, "On the nonlinearities of inductors using linear ferrite toroidal cores," *IEEE Transactions on Magnetics*, vol. 17, no. 3, pp. 1320-1325, 1981.
- [240] C. Cuellar, A. Benabou, and N. Idir, "Characterization and Modeling of Hysteresis for Magnetic Materials Used in EMI Filters of Power Converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4911-4920, 2014.
- [241] E. Cardeffi, R. Giannetti, and B. Tellini, "Numerical characterization of dynamic hysteresis loops and losses in soft magnetic materials," *IEEE Transactions on Magnetics*, vol. 41, no. 5, pp. 1540-1543, 2005.
- [242] W. Shuo, F. C. Lee, D. Y. Chen, and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 869-877, 2004.
- [243] I. F. Kovačević, T. Friedli, A. M. Muesing, and J. W. Kolar, "3-D Electromagnetic Modeling of EMI Input Filters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 231-242, 2014.
- [244] I. F. Kovačević, T. Friedli, A. M. Musing, and J. W. Kolar, "3-D Electromagnetic Modeling of Parasitics and Mutual Coupling in EMI Filters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 135-149, 2014.
- [245] W. Shuo, F. C. Lee, and W. G. Odendaal, "Characterization and parasitic extraction of EMI filters using scattering parameters," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 502-510, 2005.
- [246] S. Wang, F. C. Lee, and J. D. v. Wyk, "A Study of Integration of Parasitic Cancellation Techniques for EMI Filter Design With Discrete Components," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 3094-3102, 2008.
- [247] H. Chen, Z. Qian, Z. Zeng, and C. Wolf, "Modeling of Parasitic Inductive Couplings in a Pi-Shaped Common Mode EMI Filter," *IEEE Transactions on Electromagnetic Compatibility*, vol. 50, no. 1, pp. 71-79, 2008.

- [248] T. Masuzawa, E. Hoene, S. Hoffmann, and K. D. Lang, "Modeling method of stray magnetic couplings in an EMC filter for a SiC solar inverter," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 2366-2371.
- [249] R. Chen, J. D. v. Wyk, S. Wang, and W. G. Odendaal, "Application of structural winding capacitance cancellation for integrated EMI filters by embedding conductive layers," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 4, pp. 2679-2686 vol.4.
- [250] M. L. Heldwein and J. W. Kolar, "Winding Capacitance Cancellation for Three-Phase EMC Input Filters," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 2062-2074, 2008.
- [251] W. Shuo, C. Rengang, J. D. V. Wyk, F. C. Lee, and W. G. Odendaal, "Developing parasitic cancellation technologies to improve EMI filter performance for switching mode power supplies," *IEEE Transactions on Electromagnetic Compatibility*, vol. 47, no. 4, pp. 921-929, 2005.
- [252] S. Wang and F. C. Lee, "Analysis and Applications of Parasitic Capacitance Cancellation Techniques for EMI Suppression," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3109-3117, 2010.
- [253] T. C. Neugebauer and D. J. Perreault, "Filters with inductance cancellation using printed circuit board transformers," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, vol. 1, pp. 272-282 vol.1.
- [254] T. C. Neugebauer and D. J. Perreault, "Filters with inductance cancellation using printed circuit board transformers," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 591-602, 2004.
- [255] W. Shuo, F. C. Lee, and J. D. v. Wyk, "Integration of parasitic cancellation techniques for EMI filter design," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, 2008, pp. 736-742.
- [256] L. Dalessandro, F. d. S. Cavalcante, and J. W. Kolar, "Self-Capacitance of High-Voltage Transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 2081-2092, 2007.
- [257] G. Grandi, M. K. Kazimierczuk, A. Massarini, and U. Reggiani, "Stray capacitances of single-layer solenoid air-core inductors," *IEEE Transactions on Industry Applications*, vol. 35, no. 5, pp. 1162-1168, 1999.
- [258] Y. Qin and T. W. Holmes, "A study on stray capacitance modeling of inductors by using the finite element method," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 1, pp. 88-93, 2001.
- [259] W. Tan, X. Margueron, T. Duquesne, and N. Idir, "An Improved Parasitic Capacitance Cancellation Method for Planar Differential Mode Inductor in EMI Filters," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1-6.
- [260] P. Thummala, H. Schneider, Z. Zhang, and M. A. E. Andersen, "Investigation of Transformer Winding Architectures for High-Voltage (2.5 kV) Capacitor Charging and Discharging Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5786-5796, 2016.
- [261] S. Weber, M. Schinkel, S. Guttowski, W. John, and H. Reichl, "Calculating parasitic capacitance of three-phase common-mode chokes," in *Proc. Power Convers. Intell. Motion*, 2005, pp. 1-6.
- [262] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant converters - a review of the calculation of the stray capacitance of transformers," in *Fortieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, 2005, vol. 3, pp. 1868-1875 Vol. 3.
- [263] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight and efficiency analysis of switched circuit topologies for modular power electronics in MEA," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 3640-3647.
- [264] Y. Maillat, R. Lai, S. Wang, F. Wang, R. Burgos, and D. Boroyevich, "High-Density EMI Filter Design for DC-Fed Motor Drives," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1163-1172, 2010.
- [265] D. O. Boillat, J. W. Kolar, and J. Mu"hlethaler, "Volume minimization of the main DM/CM EMI filter stage of a bidirectional three-phase three-level PWM rectifier system," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 2008-2019.
- [266] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive Design and Optimization of a High-Power-Density Single-Phase Boost PFC," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2574-2587, 2009.
- [267] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a Simplified Differential-Mode EMI Filter Design," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 1031-1040, 2010.
- [268] A. Roc'h and F. Leferink, "Optimization of the in situ Performance of Common Mode Chokes for Power Drive Systems Using Designable Parameters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 2, pp. 529-535, 2018.

- [269] F. Wang, W. Shen, D. Boroyevich, S. Ragon, V. Stefanovic, and M. Arpilliere, "Design Optimization of Industrial Motor Drive Power Stage Using Genetic Algorithms," in *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, 2006, vol. 5, pp. 2581-2586.
- [270] F. Wang, W. Shen, D. Boroyevich, S. Ragon, V. Stefanovic, and M. Arpilliere, "Voltage source inverter," *IEEE Industry Applications Magazine*, vol. 15, no. 2, pp. 24-33, 2009.
- [271] G. Ala *et al.*, "Computer aided optimal design of high power density EMI filters," in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, 2016, pp. 1-6.
- [272] R. Azaro, L. Ioriatti, M. Martinelli, and A. Massa, "Automatic design and optimisation of EMI filter using commercially-available components," *Electronics Letters*, vol. 43, no. 6, pp. 15-16, 2007.
- [273] B. Touré, J. L. Schanen, L. Gerbaud, T. Meynard, J. Roudet, and R. Ruelland, "EMC Modeling of Drives for Aircraft Applications: Modeling Process, EMI Filter Optimization, and Technological Choice," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1145-1156, 2013.
- [274] D. Zhang, T. Fan, P. Ning, and X. Wen, "An automatic EMI filter design methodology for electric vehicle application," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 4497-4503.
- [275] X. Zhang, D. Boroyevich, P. Mattavelli, J. Xue, and F. Wang, "EMI filter design and optimization for both AC and DC side in a DC-fed motor drive system," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 597-603.
- [276] N. K. Poon, J. C. P. Liu, C. K. Tse, and M. H. Pong, "Techniques for input ripple current cancellation: classification and implementation [in SMPS]," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1144-1152, 2000.
- [277] J. Biela, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl, and J. W. Kolar, "Passive and Active Hybrid Integrated EMI Filters," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1340-1349, 2009.
- [278] P. Cantillon-Murphy, T. C. Neugebauer, C. Brasca, and D. J. Perreault, "An active ripple filtering technique for improving common-mode inductor performance," *IEEE Power Electronics Letters*, vol. 2, no. 2, pp. 45-50, 2004.
- [279] W. Chen, X. Yang, and Z. Wang, "A Novel Hybrid Common-Mode EMI Filter With Active Impedance Multiplication," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1826-1834, 2011.
- [280] W. Chen, W. Zhang, X. Yang, Z. Sheng, and Z. Wang, "An Experimental Study of Common- and Differential-Mode Active EMI Filter Compensation Characteristics," *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 683-691, 2009.
- [281] A. C. Chow and D. J. Perreault, "Design and evaluation of a hybrid passive/active ripple filter with voltage injection," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 39, no. 2, pp. 471-480, 2003.
- [282] M. L. Heldwein, H. Ertl, J. Biela, and J. W. Kolar, "Implementation of a Transformerless Common-Mode Active Filter for Offline Converter Systems," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 5, pp. 1772-1786, 2010.
- [283] S. Wang, Y. Y. Maillet, F. Wang, D. Boroyevich, and R. Burgos, "Investigation of Hybrid EMI Filters for Common-Mode EMI Suppression in a Motor Drive System," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 1034-1045, 2010.
- [284] J. D. v. Wyk, F. C. Lee, L. Zhenxian, C. Rengang, W. Shuo, and L. Bing, "Integrating active, passive and EMI-filter functions in power electronics systems: a case study of some technologies," *IEEE Transactions on Power Electronics*, vol. 20, no. 3, pp. 523-536, 2005.
- [285] Y. Chu, S. Wang, and Q. Wang, "Modeling and Stability Analysis of Active/Hybrid Common-Mode EMI Filters for DC/DC Power Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6254-6263, 2016.
- [286] Vicor. *QuietPower® EMI Input Filter Modules*. Available: <http://www.vicorpower.com/dc-dc-filters/gpi>
- [287] J. Ji, W. Chen, and X. Yang, "Design and precise modeling of a novel Digital Active EMI Filter," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 3115-3120.
- [288] J. Ji, W. Chen, X. Yang, and J. Lu, "Delay and Decoupling Analysis of a Digital Active EMI Filter Used in Arc Welding Inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6710-6722, 2018.
- [289] EIA. *Existing Transmission Capacity by High-Voltage Size*, 2014. Available: http://www.eia.gov/electricity/annual/html/epa_08_10_a.html
- [290] NRECA. (2017, Jan. 31). *America's Electric Cooperatives: 2017 Fact Sheet*. Available: <https://www.electric.coop/electric-cooperative-fact-sheet/>
- [291] ABB. (2002). *HARD TO FIND INFORMATION ABOUT DISTRIBUTION SYSTEMS*. Available: <https://library.e.abb.com/public/91ad3a29a50978bf85256c550053db0d/Hard.To.Find.6th.pdf>

- [292] S. Sozer, "TRANSMISSION EXPANSION PLANNING TO ALLEVIATE CONGESTION IN DEREGULATED POWER MARKETS," Ph.D. dissertation, Auburn University, Auburn, Alabama, 2006.
- [293] EIA. *Existing Net Summer Capacity by Energy Source and Producer Type, 2006 through 2016*. Available: https://www.eia.gov/electricity/annual/html/epa_04_02_a.html
- [294] EPRI, *Transmission Line Reference Book-345 kV and above*, 2nd ed. Palo Alto, CA, 1982, pp. 130-140.
- [295] D. Jovcic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2535-2543, 2010.
- [296] E. Veilleux and B. T. Ooi, "Multiterminal HVDC With Thyristor Power-Flow Controller," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1205-1212, 2012.
- [297] J. B. Rossman, T. L. Laughner, A. M. Murphy, D. E. Marler, and G. L. Kobet, "Transmission voltage unbalance evaluation," in *2012 Future of Instrumentation International Workshop (FIIW) Proceedings*, 2012, pp. 1-4.
- [298] J. Green, A. Bowen, L. J. Fingersh, and Y.-H. Wan, "Electrical Collection and Transmission Systems for Offshore Wind Power," presented at the Offshore Technology Conference, Houston, Texas, U.S.A., 2007/1/1/, 2007.
- [299] R. L. Hauth, P. J. Tatro, B. D. Railing, B. K. Johnson, J. R. Johnson, and J. L. Fink, "HVDC power transmission technology assessment report," Oak Ridge National Laboratory April 1997.
- [300] K. Meah and S. Ula, "Comparative Evaluation of HVDC and HVAC Transmission Systems," in *2007 IEEE Power Engineering Society General Meeting*, 2007, pp. 1-5.
- [301] M. Marz *et al.*, "Mackinac HVDC converter automatic runback utilizing locally measured quantities," in *Cigré*, 2014.
- [302] K. J. K. E.V. Solodovnik, "System Architecture for Battery Charger Based on GaN-Based Power Devices," United States, 2017. Available: <http://www.freepatentsonline.com/y2017/0279287.html>.
- [303] Broadcom. *Precision optically isolated voltage sensor*. Available: <https://www.broadcom.com/products/optocouplers/industrial-plastic/isolation-amplifiers-modulators/isolation-amplifiers/acpl-c87b>
- [304] S. labs. *Isolated amplifier for current shunt measurement*. Available: <https://www.silabs.com/documents/public/data-sheets/si8920-datasheet.pdf>
- [305] M. B. Aimonetto and F. Fiori, "On the effectiveness of EMIRR to qualify OpAmps," in *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, pp. 40-44.
- [306] R. A. Amadori, V. G. Puglielli, and R. E. Richardson, "Prediction Methods for the Susceptibility of Solid State Devices to Interference and Degradation From Microwave Energy," in *1973 IEEE International Electromagnetic Compatibility Symposium Record*, 1973, pp. 1-17.
- [307] C. K. a. L. Counts, *A designer's guide to instrumentation amplifiers*, 3rd ed. ed. Analog Devices Inc., 2006.
- [308] F. Fiori, "A new nonlinear model of EMI-induced distortion phenomena in feedback CMOS operational amplifiers," *IEEE Transactions on Electromagnetic Compatibility*, vol. 44, no. 4, pp. 495-502, 2002.
- [309] F. L. Fiori and P. S. Croveti, "Prediction of high-power EMI effects in CMOS operational amplifiers," *IEEE Transactions on Electromagnetic Compatibility*, vol. 48, no. 1, pp. 153-160, 2006.
- [310] T. Instruments, "EMI Rejection Ratio of Operational Amplifiers," Application Report SBOA128, 2011.
- [311] W. Kester, *System applications guide*, . Analog Devices Inc., 1993.
- [312] R. E. Richardson, V. G. Puglielli, and R. A. Amadori, "Microwave Interference Effect in Bipolar Transistors," *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-17, no. 4, pp. 216-219, 1975.
- [313] Allegro. *ACS710: 120 kHz Bandwidth, High-Voltage Isolation Current Sensor IC with Integrated Overcurrent Detection*. Available: <http://www.allegromicro.com/en/Products/Current-Sensor-ICs/Zero-To-Fifty-Amp-Integrated-Conductor-Sensor-ICs/ACS710.aspx>
- [314] LEM. *LTSR: ASIC Based Closed-Loop Transducers from 6 A up to 25 A nominal with reference access*. Available: http://www.lem.com/images/stories/files/Products/P1_5_1_industry/E_CH23103.pdf
- [315] Z. Zhang, "Characterization and realization of high switching-speed capability of SiC power devices in voltage source converter," University of Tennessee, Knoxville 2015.
- [316] S. Singer, "The application of loss-free resistors in power processing circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 595-600, 1991.
- [317] S. Singer, S. Ozeri, and D. Shmilovitz, "A pure realization of loss-free resistor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 8, pp. 1639-1647, 2004.

- [318] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Temperature-dependent turn-on loss analysis for GaN HFETs," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1010-1017.
- [319] S. Wang, F. Xue, A. Q. Huang, and S. Liu, "Physics understanding of high temperature behavior of Gallium Nitride power transistor," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 324-327.
- [320] R. P. Severns and J. Armijos, *MOSPOWER applications handbook*. Santa Clara, Calif.: Siliconix, 1985.
- [321] R. Lai, F. Wang, R. Burgos, D. Boroyevich, D. Jiang, and D. Zhang, "Average Modeling and Control Design for VIENNA-Type Rectifiers Considering the DC-Link Voltage Balance," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2509-2522, 2009.
- [322] J. W. Kolar, H. Ertl, and F. C. Zach, "Design and experimental investigation of a three-phase high power density high efficiency unity power factor PWM (VIENNA) rectifier employing a novel integrated power semiconductor module," in *Applied Power Electronics Conference and Exposition, 1996. APEC '96. Conference Proceedings 1996., Eleventh Annual, 1996*, vol. 2, pp. 514-523 vol.2.
- [323] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899-907, 2013.
- [324] S.-M. Shin, J.-H. Ahn, and B.-K. Lee, "Maximum efficiency operation of Three-Level T-type inverter for low-voltage and low-power home appliances," *Journal of Electrical Engineering and Technology*, vol. 10, no. 2, pp. 586-594, 2015.
- [325] Y. Jiao and F. C. Lee, "New Modulation Scheme for Three-Level Active Neutral-Point-Clamped Converter With Loss and Stress Reduction," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 9, pp. 5468-5479, 2015.
- [326] Y. Jiao, F. C. Lee, and S. Lu, "Space Vector Modulation for Three-Level NPC Converter With Neutral Point Voltage Balance and Switching Loss Reduction," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5579-5591, 2014.
- [327] Y. Jiao, S. Lu, and F. C. Lee, "Switching Performance Optimization of a High Power High Frequency Three-Level Active Neutral Point Clamped Phase Leg," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3255-3266, 2014.
- [328] D. Andler, R. Álvarez, S. Bernet, and J. Rodríguez, "Switching Loss Analysis of 4.5-kV–5.5-kA IGCTs Within a 3L-ANPC Phase Leg Prototype," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 584-592, 2014.
- [329] J. W. Kolar, T. Friedli, and M. Hartmann, "Three-phase PFC rectifier and ac-ac converter systems—Part II, Tutorial," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2011.
- [330] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," in *Proceedings of Intelec 94*, 1994, pp. 367-374.
- [331] Y. Zhao, Y. Li, and T. A. Lipo, "Force Commutated Three Level Boost Type Rectifier," *IEEE Transactions on Industry Applications*, vol. 31, no. 1, pp. 155-161, 1995.
- [332] Y. Zhao, Y. Li, and T. A. Lipo, "Force commutated three level boost type rectifier," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, 1993, pp. 771-777 vol.2.
- [333] K. Oguchi and Y. Maki, "A multilevel-voltage source rectifier with a three-phase diode bridge circuit as a main power circuit," in *Conference Record of the 1992 IEEE Industry Applications Society Annual Meeting*, 1992, pp. 695-702 vol.1.
- [334] K. Oguchi and I. Maki, "A multilevel-voltage source rectifier with a three-phase diode bridge circuit as a main power circuit," *IEEE Transactions on Industry Applications*, vol. 30, no. 2, pp. 413-422, 1994.
- [335] D. Andler, R. Álvarez, S. Bernet, and J. Rodríguez, "Switching Loss Analysis of 4.5-kV-5.5-kA IGCTs Within a 3L-ANPC Phase Leg Prototype," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 584-592, 2014.
- [336] S. Saba and B. Fortman. *Designing the next generation of industrial drive and control systems*. Available: <http://www.ti.com/lit/wp/spry258a/spry258a.pdf>
- [337] Vacuumsmelze GmbH & Co. KG. (2016). *Nanocrystalline VITROPERM EMC Products*.
- [338] D. D. L. Chung, "Materials for electromagnetic interference shielding," *Journal of Materials Engineering and Performance*, vol. 9, no. 3, pp. 350-354, 2000/06/01 2000.

- [339] S. Wang, Y. Y. Maillet, F. Wang, R. Lai, F. Luo, and D. Boroyevich, "Parasitic Effects of Grounding Paths on Common-Mode EMI Filter's Performance in Power Electronics Systems," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3050-3059, 2010.
- [340] W. T. McLyman, *Transformer and Inductor Design Handbook*. New York: Marcel Dekker, 2002.
- [341] E. C. Snelling, *Soft ferrites: properties and applications*, first edition ed. London: Iliffe, 1969.
- [342] W. T. Duerdoth, "Equivalent capacitances of transformer windings," *Wireless Eng.*, vol. 23, pp. 161-167, Jun. 1946.
- [343] M. Zahn, *Electromagnetic field theory—A problem solving approach*. Melbourne, FL: Krieger, 2003.
- [344] J. Koch, "Berechnung der kapazität von spulen, insbesondere in schalenkernen," *Volvo Berichte*, vol. 14, no. 3, pp. 99-119, 1968.
- [345] D. Jiang, R. Lai, F. Wang, F. Luo, S. Wang, and D. Boroyevich, "Study of Conducted EMI Reduction for Three-Phase Active Front-End Rectifier," *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3823-3831, 2011.
- [346] Keysight. *Impedance Measurement Handbook-a guide to measurement technology and techniques (6th ed.)*. Available: <https://literature.cdn.keysight.com/litweb/pdf/5950-3000.pdf>
- [347] Keysight. *Balanced Circuit Measurement with an Impedance Analyzer/LCR Meter/Network Analyzer*. Available: <http://literature.cdn.keysight.com/litweb/pdf/5091-4480E.pdf>
- [348] R. Wang, D. Boroyevich, H. F. Blanchette, and P. Mattavelli, "High power density EMI filter design with consideration of self-parasitic," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2285-2289.
- [349] E. A. Jones, P. Williford, and F. Wang, "A fast overcurrent protection scheme for GaN GITs," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 277-284.
- [350] H. Li *et al.*, "Ultra-Fast Short Circuit Protection Solutions for E-mode GaN HEMTs," in *Proc. IEEE 1st Workshop on Wide Bandgap Power Devices Appl. in Asia (WiPDA-Asia)*, 2018, no. in press.
- [351] R. Lai, F. Wang, R. Burgos, D. Boroyevich, D. Zhang, and P. Ning, "A Shoot-Through Protection Scheme for Converters Built With SiC JFETs," *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2495-2500, 2010.
- [352] F. Wang, R. Lai, X. Yuan, F. Luo, R. Burgos, and D. Boroyevich, "Failure-Mode Analysis and Protection of Three-Level Neutral-Point-Clamped PWM Voltage Source Converters," *IEEE Transactions on Industry Applications*, vol. 46, no. 2, pp. 866-874, 2010.

Vita

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