Modeling and Control of a 7-Level Switched Capacitor Rectifier for Wireless Power Transfer Systems

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Abstract

Wireless power continues to increase in popularity for consumer device charging. Rectifier characteristics like efficiency, compactness, impedance tunability, and harmonic content make the multi-level switched capacitor rectifier (MSC) an exceptional candidate for modern WPT systems. The MSC shares the voltage conversion characteristics of a post-rectification buck-boost topology, reduces waveform distortion via its multi-level modulation scheme, demonstrates tank tunability via the phase control inherent to actively switched rectifiers, and accomplishes all this without a bulky filter inductor. In this work, the MSC WPT system operation is explained, and a loss model is constructed. A prototype system is used to validate the models, showing exceptional agreement with the predicted efficiencies. The modeled MSC efficiencies are between 96.1% and 98.0% over the experimental power range up to 20.0 W.

Two significant control loops are required for the MSC to be implemented in a real system. First, the output power is regulated using the modulation of the rectifier's input voltage. Second, the switching frequency of the rectifier must exactly match the WPT carrier frequency set by the inverter on the primary side. Here, a small signal discrete time

model is used to construct four transfer functions relating to the output voltage. Then, four novel time-to-time transfer functions are built on top of the discrete time model to inform the frequency synchronization feedback loop. Both loops are tested and validated in isolation. Finally, the dual-loop control problem is defined, closed form equations that include loop interactions are derived, and stable wide-range dual-loop operation is demonstrated experimentally.

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Chapter 1

Introduction

Consumer device wireless power transfer (WPT) is well established in the market. Annually released flagship smartphones are consistently equipped with the cutting-edge technology, and wireless charging has been included in their hardware suite for the past few years. From laptops and tablets to cellphones and wearables, these handheld electronics are an integral part of daily life. Elimination of charging cables yields significant benefits in terms of convenience, safety, and device longevity. These and other motivating factors have convinced more than 600 international companies to contribute to the development of WPT standards [21], resulting in greater than 3,000 WPT-certified products available on the market today [22].

1.1 Wireless Power

The generalized layout of a wireless power transfer system is shown in Fig. 1.1. Power is transferred from the DC source, V_{in}, to the load, $R_{rec,1}$. All power delivered to the load travels through the transformer comprised of wireless power coils, L_{tx} and L_{rx}. Coupling coefficient k denotes the strength of the magnetic coupling between the two inductors in the transformer.

The left and right sides of the circuit in Fig. 1.1 are the transmitter and receiver sides of the WPT system, respectively. In a traditional transformer, ferromagnetic material is generally closed through both indutances in order to amplify the magnetic coupling of the system. Here, the transformer used in wireless power avoids mechanically fastening L_{tx} to L_{rx} with core material. Thus, the transmitter (or primary) and receiver (or secondary) sides are both electrically isolated and physically decoupled. This is the fundamental operating principle of WPT systems – transformer design that enables seamless electrical power throughput without restricting the secondary side circuitry to a fixed location in physical space, i.e. a user can charge a device at a charging pad or carry the phone elsewhere without manually changing circuitry or connectors in either case.

There are various approaches when engineering a WPT system. The two most common frameworks for consumer device designs are the AirFuel™ and Qi™ standards, and while both follow the basic structure shown in Fig. 1.1, there are some notable differences. The AirFuel Resonant standard generally operates with lower coupling values: k is smaller (the system is "loosely coupled"). The fundamental operating frequency for AirFuel is 6.78 MHz,

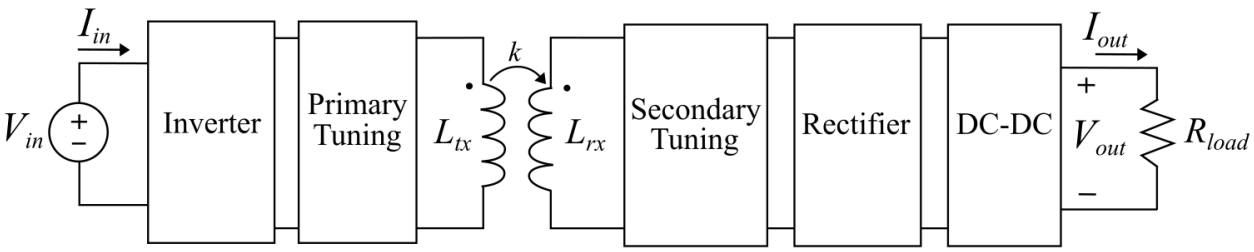


Figure 1.1: General form of a WPT system, showing power commutation from V_{in}, through L_{tx} and L_{rx}, and to $R_{rec,1}$.

Table 1.1: WPT Standards Comparison [1, 2]

	Qi™	**AirFuel**™ Resonant
Carrier Frequency	100's kHz	6.78 MHz
Magnetic Coupling	Tight, $k \uparrow$	Loose, $k \downarrow$
Receivers per Transmitter	1	Multiple
Communication	In-Band	Bluetooth®
Charging Distance	millimeters +	centimeters +

multiple devices can charge simultaneously, and the consumer benefits from a longer charging distance [1].

The Qi™ standard is a "tightly coupled" standard, meaning that the coupling value k tends to be higher. The format allows only one charging coil (L_{tx}) to one receiving coil (L_{rx}), enables in-band communications between the primary and secondary, and operates in the 100 kHz range. An overview of each standard is given in Table 1.1. Without strict adherence, the research in this thesis is conducted with reference to the Qi standard. Therefore, an overview of the Qi standard is first presented in order to give context to the designs proposed later.

1.2 Fundamental Circuit Model

The first harmonic approximation (FHA) is often used to model the primary behavior of the WPT system [23, 24]. Fig. 1.2a shows how the FHA is applied to a basic wireless power transfer system. The output of the inverter is assumed to be sinusoidal and is modeled as voltage source, v_p. The wireless power coils are again given by L_{tx} and L_{rx}, and they are magnetically coupled together by a factor of k. The transmitter and receiver coils are tuned by C_p and C_s, respectively. The capacitance values are chosen by the designer to pass power from the source to the load at the fundamental frequency while dampening all other frequencies. The resistances R_p and R_s are the equivalent series resistances of the WPT tank at the frequency defined by v_p, and $Z_{rec,1}$ is the complex load impedance that receives power.

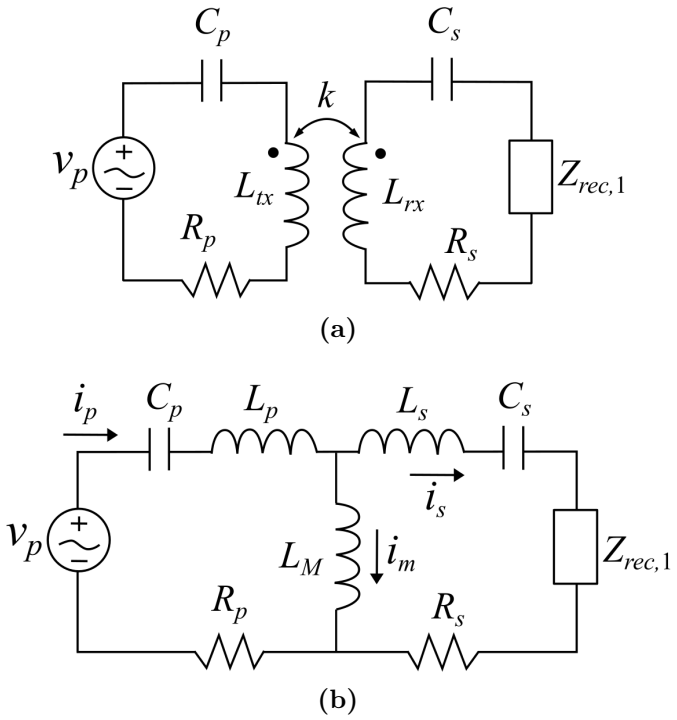


Figure 1.2: Equivalent WPT tank models: (a) k model and (b) T model.

Given the high likelihood that a user will align the transmitter and receiver coils slightly differently during each charging session, the consequent varying value of k means that a WPT system is operated with a variety of equivalent inductance values. Fig. 1.2b shows an equivalent way of modeling the same circuit, the T model. In the T model, each of the inductance values is a function of the coupling, k, and the energy stored in the magnetic field is modeled by the current flowing through L_M.

To convert between the two models, inductances L_p, L_s, and L_M are functions of L_{tx}, L_{rx}, and k. The coupled inductance is

$$L_M = k \cdot \sqrt{L_{tx} L_{rx}}, \tag{1.1}$$

and each of the line inductances are

$$L_p = L_{tx} - L_M, \tag{1.2}$$

$$L_s = L_{rx} - L_M. \tag{1.3}$$

When the coupling value is ideal ($k = 1$), the value of L_M is large and the amount of circulating magnetizing current is small ($i_m \approx 0$). When $k = 0$, $L_M = 0$ and the magnetizing path is shorted, signifying that no power will flow to the output because all current will be circulating through the shorted path ($i_s \approx 0$). In reality, the coupling will fall somewhere between these two extremes, and some current will circulate through the magnetization path

while the rest of the current delivers power to the output. Put simply, the more magnetic field shared between the coils, the greater the magnetic coupling.

The T model provides an insightful framework for understanding system tuning. As an example, take $L_{tx} = 10$ μH, $L_{rx} = 10$ μH, and $k = 0.4$. This means L_s is equal to 4.0 μH in the T model. If a designer wanted to assign C_s so that it resonates at 150 kHz with the line inductance ($L_s = 4.0$ μH), the equations dictate that $C_s = 1/(4\pi^2 f^2 L_s) = 281.5$ nF. If the coupling changes from $k = 0.4$ to $k = 0.2$ because a user changes the coil alignment, the resonant frequency also changes to $f = 1/(2\pi\sqrt{L_s C_s}) = 212.1$ kHz.

The specific resonant frequency change in this example may or may not impact the system enough to cause any type of catastrophic failure, but the mechanic illustrated here is one that designers must pay attention to. The fundamental model is predicated on the filtering characteristics of the WPT tank tuning, and if that tuning changes dramatically enough, the underlying assumption that the harmonics are negligible may fail. Furthermore, when the efficiency curves of the inverter, tank, and rectifier are considered, the alteration of k could move the WPT system to an operating point that is significantly less efficient than intended, a byproduct of the spacial freedoms inherent to WPT systems.

Given that the fundamental approximation is valid, the circuit in Fig. 1.2 is used to derive certain loading characteristics for the WPT system. If the secondary side series tuning capacitor is sized to resonate with the receiver coil (C_s with L_{rx}), then $\mathrm{Im}(Z_{rec,1}) = 0$ and $Z_{rec,1} = R_{rec,1}$. Here, equations for maximum power throughput and maximum system efficiency are derived [24]. In general, maximum power is the effect of conjugate matching [24]. For consumer device WPT, the maximum efficiency point is generally more

useful. A closed-form equation for efficiency is derived for the fundamental model, and then the derivative is taken in order to isolate the optimal value of $R_{rec,1}$ [24]. The work in [24] gives the optimal resistive load

$$R_{rec,opt} = \sqrt{R_s^2 + \frac{R_s}{R_p}(\omega L_M)^2} \qquad [24]. \tag{1.4}$$

The optimal value of $R_{rec,1}$ is a function of L_M and, thereby, a function of k. Mathematically, this is why the system efficiency of a WPT link is maximized by changing the load as the magnetic coupling varies. The optimal load often has an imaginary component, however, due to inaccurate matching of the secondary side reactive components. The derivation is expanded to find the complete impedance, $Z_{rec,1}$, that optimizes efficiency for the system in Fig. 1.2. This expression is

$$Z_{rec,opt} = \frac{j}{\omega C_s} - j\omega(L_s + L_M) + \sqrt{R_s^2 + \frac{R_s}{R_p}(\omega L_M)^2} \qquad [24], \tag{1.5}$$

and it returns the complex impedance of $Z_{rec,opt}$. To illustrate, Fig. 1.3 shows three different values of k using the tank defined by Table 1.2, where C_s is not perfectly tuned to L_{rx}. Each value of coupling results in a different optimal loading, denoted by the black x. Note also the black dot: this is $R_{rec,opt}$, the value returned by (1.4) that assumes a perfect secondary tuning. For many tank designs, the efficiency difference between the two operating points is small at high coupling values. But the deviation between $R_{rec,opt}$ and $Z_{rec,opt}$ is more significant as coupling reduces because the constant imaginary component of $Z_{rec,opt}$ becomes more

Table 1.2: Operating Point Used to Exemplify Design Space

v_p	L_{tx}	L_{rx}	C_p	C_s	R_p	R_s
19.1 V	13 μH	13 μH	750 nF	100 nF	100 mΩ	200 mΩ

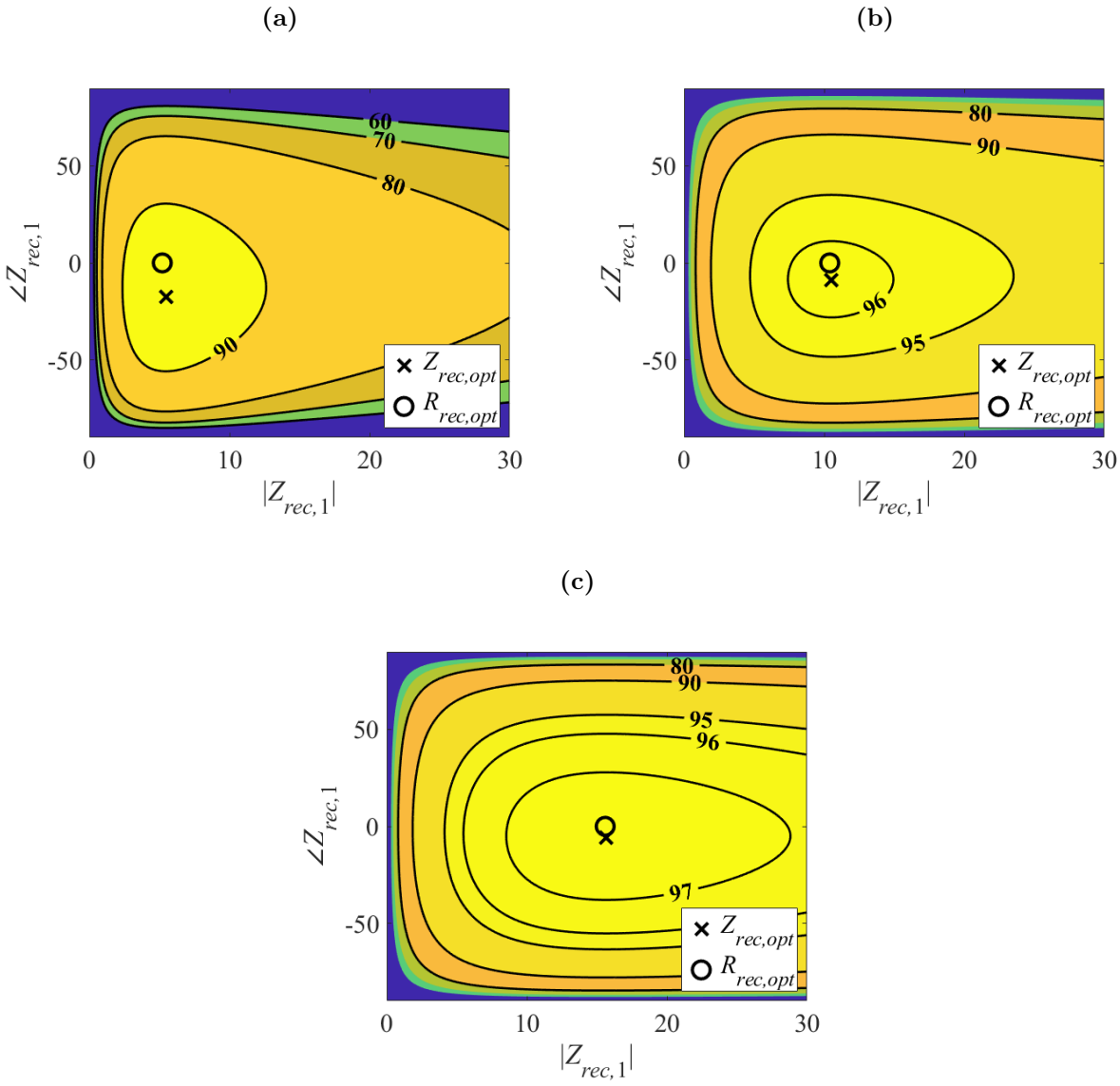


Figure 1.3: Efficiency of the WPT system given coupling values of (a) $k = 0.3$, (b) $k = 0.6$, and (c) $k = 0.9$. The optimal load is shown as a black x, and the optimal resistance ($\mathrm{Im}(Z_{rec,opt}) = 0$) is shown as a black circle (o).

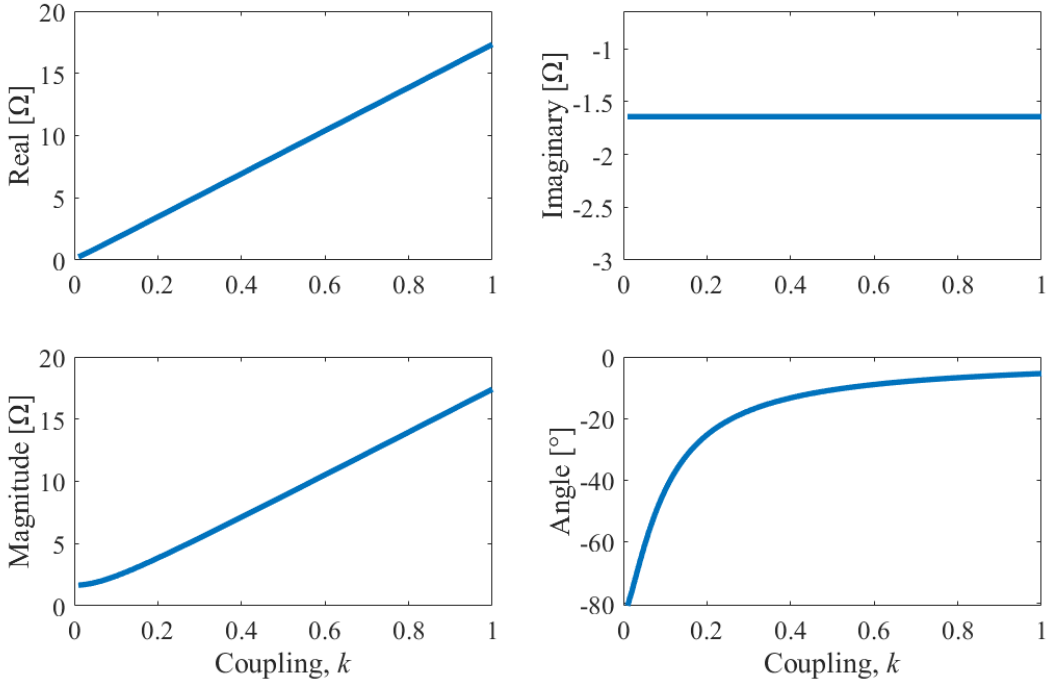


Figure 1.4: Cartesian and polar descriptions of the optimal load ($Z_{rec,opt}$) for different values of k using the tank in Table 1.2.

dominant relative to the impedance's shrinking real component. For the same example, Fig. 1.4 shows how the real and imaginary values of $Z_{rec,opt}$ vary with coupling factor.

If the WPT receiver tank is tuned perfectly to the fundamental frequency such that $|Z_{Cs}| = |Z_{Lrx}|$, then there is no imaginary component necessary to achieve optimal efficiency. In this case, a resistive load is the optimal complex impedance at $Z_{rec,1}$ [24], and the black x and dot would perfectly align for each coupling value in Fig. 1.3. In practice, perfect tuning is impossible with imperfect component values, and the amount of deviation influences the phase angle required of $Z_{rec,1}$ for maximum efficiency. Fig. 1.4 exemplifies how an "out-of-tune" tank influences the optimal loading angle of a WPT system by requiring a non-zero imaginary component to retune the coils.

1.3 The Qi™ Standard

With over 3,700 Qi-certified products available today, the Qi standard dominates the WPT consumer device market [22]. This level of availability means convenience to the end-user, as it is increasingly easy to find a compatible wireless charging location. The market relevance of the standard also means that an understanding of Qi fundamentals is essential for the researcher.

Because the Qi standard is designed to be a near-field, tightly-coupled strategy, k is assumed to be relatively high during the design process. Generally, loosely coupled strategies (like AirFuel Resonant) might operate with $k \leq \approx 0.25$, while Qi-type designs will generally

operate with $k \geq \approx 0.25$ [25–28]. The value of k is affected by the proximity of the WPT coils and the orientation of the two coils relative to one another in space [28].

This is why Qi transmitters and receivers are designed with flat, similarly-sized interfaces. The design allows the L_{tx} and L_{rx} coils to share as much magnetic field as possible by ensuring that the wireless power coils are properly oriented and in close proximity. Assuming the coils are then aligned one over the other, k is maximized, and the efficiency of the WPT system is increased. In contrast, if an obstruction creates distance between the coils, they are offset on the z-axis, or if either is rotated, the coupling decreases and the system efficiency likely follows. Power delivery and fundamental frequency are correlated under the Qi standard. Lower power Qi applications can transfer up to 5 W using frequencies from 110 to 205 kHz, while power applications of up to 120 W can leverage the frequency range of 80 to 300 kHz [1]. Because of the space constraints of thin consumer electronics and the orientation constraints of the high coupling requirement, the WPT coils in Qi systems are most often designed with a thin, disc-like shape [29, 30].

The inductances and dimensions necessary for consumer electronic WPT often result in challenges for inductors designed at Qi operating frequencies. In the 100's of kHz frequency range, wireless power coils often exhibit sizeable parasitic equivalent series resistances (ESRs), or equivalently, the coils suffer from a low quality factor, Q. The consequent conduction losses in the WPT tank are significant for Qi designs because of these constraints [31].

Qi systems enable the primary and secondary sides to communicate with one another. The communication is "in-band," meaning that the information is transmitted from one

unit to another via the same magnetic field that transmits the charging power. The digital communication signal is embedded into the power waveforms and decoded by the message recipient. Communication is useful for both ensuring a safe load is receiving the power and for real-time system-level tuning. Take a transmitter/receiver misalignment for example: k is less than ideal, and the primary side can ping the secondary side, notifying it that the perceived load is not as expected. If the secondary has the means, it can adjust its perceived electrical load to better suit the needs of the transmitter [24, 32, 33]. This type of communication adds robustness and versatility to an already useful platform.

Overall, the Qi standard leverages higher values of k to wirelessly transmit power. The operation frequencies, desired coupling values, and common space constraints tend to push Qi WPT coil designs to lower Q values. Conduction loss tends to dominate switching loss in these systems [31]. Therefore, the Qi protocol is poised to benefit from design approaches that leverage switching actions to reduce WPT coil conduction. The Qi protocol serves as a loose framework for the research in this thesis, but the prototype circuit is not subject to strict adherence to the specific implementation details of the Qi standard.

1.4 Elements of a WPT System

A basic understanding of the complete wireless power system is helpful within the discussion and derivation of WPT rectifier topics. As a complement to the rectifier work of this thesis, each segment of the fundamental WPT circuit model is briefly described in this section.

1.4.1 Fundamental Source

The fundamental circuit model is powered by the source v_p, and in a real circuit this source is an inverter. The inverter takes a DC source voltage and translates it into a periodic waveform by means of switching actions. The inverter sets both the fundamental period and consequent frequency of the entire WPT system. Therefore, an inverter is designed with the entire system in-mind and acts as both the power source and frequency source for the rest of the wireless power system.

The full-bridge type inverter is a four-switch topology that flips the polarity of a DC voltage (V_{in}) to achieve a square wave output at v_{inv}. The topology is shown in Fig. 1.5b and is featured in many wireless power works that operate in the kilohertz frequency range [3, 34–37]. The work in [34] showcases a reduction in switch count for a multi-transmitter coil wireless power system. An in-motion secondary side couples to each transmitter as it moves along the coil path, and four inverter switches are used to drive each transmitter coil in the 15.9 kHz system [34]. Another full-bridge approach marries an 85 kHz inductive power inverter with a 1 MHz capacitive power transfer inverter by designing the two supplies to share a half-bridge [36]. Some full-bridge approaches include inductors so that their output manifests as a current source to the rest of the WPT system [35].

A half-bridge is a variation of the full-bridge and only uses two switches to invert a DC source. Fig. 1.5c shows a half-bridge that uses two capacitors across V_{in}. This topology

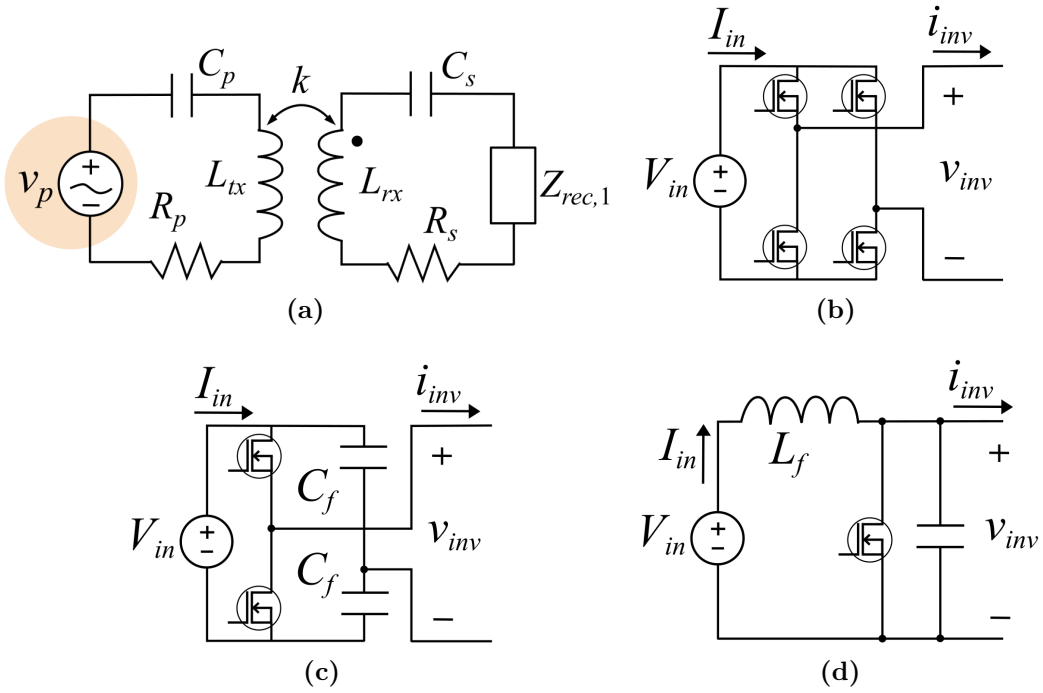


Figure 1.5: Implementation of the (a) fundamental source via a (b) full-bridge [3], (c) half-bridge [4], or (d) class-E inverter [5, 6]. Here, v_p is the fundamental component of v_{inv}.

is used in [4] in a 1 MHz capacitive power transfer system. The work in [35] uses a full-bridge component arrangement, but the two high-side devices are inductors. The current-fed 2,000 W wireless power system operates at 46.8 kHz and is calculated at 92.5 % efficient [35].

The class-E topology is often regarded as a good candidate for megahertz frequency operation due to its ability to achieve zero voltage switching and zero voltage derivative switching (ZVDS or ZDS) [28, 38–43]. Switching at 10's of kHz typically does not incur enough switching loss to dominate the loss profile. However, the class-E inverter in Fig. 1.5d has still been investigated at ≈300 kHz for inductively coupled wireless power applications [5, 6], and the work in [44] used class-E inversion and rectification in a 200 kHz system. Note that the primary side capacitor, C_p, and the transmitter coil, L_{tx}, are not pictured in any inverter topology in Fig. 1.5a, but these elements are a necessary part of the class-E topology in Fig. 1.5d.

While different, each of the inverter topologies serves the same purpose within the fundamental circuit model: power the WPT circuit as a sinusoidal source. In Fig. 1.5, each topology leverages V_{in} to create v_{inv}, and the first harmonic of v_{inv} in Figs. 1.5b-1.5d serves as v_p in a wireless power system. The inverter provides the input power to and dictates the fundamental frequency of the WPT circuit.

1.4.2 WPT Coils

The coupled coils of the wireless power system are the fundamental technology that makes WPT possible, and given that the full system power flows through the wireless power tank, a

significant amount of research goes into both coil design and tuning. However, as illustrated with the fundamental circuit model in Fig. 1.6, the conduction losses associated with R_p and R_s are the most basic hindrance to a high-efficiency wireless power setup. Within the tuned WPT tank, these parasitic ESRs are attributed almost entirely to the inductors because low ESR capacitors are relatively easy to purchase for applications near 100 kHz. At the most basic level, more coil turns means a larger inductance, but more turns also means more conduction loss (larger R_p and R_s). Improving coil design is a priority in the research community because it directly affects the viability of the WPT system [29, 30, 45–56].

Many techniques serve to characterize or improve the coils used in today's systems. The relationship between stray magnetic field and coil efficiency is characterized in [29]. The work in [45] solves for an optimal coil design with an analytical process that accounts for both ohmic loss and the skin effect. Bayesian optimization [30], multilayer flat spiral techniques [46], and numerical modeling [47] are applied to wireless power coil designs in attempts to improve the state of the art. Another technique involves leveraging non-uniform wire width in a manner that increases coil inductance more quickly than ESR. The design showcases a 1.21 times increase in quality factor when compared to the traditional approach [54].

Magnetic material is used to increase the efficiency of WPT system by increasing the coupling factor relative to the ESR components. The work in [31] analyzes a wireless power system, concludes that the losses in the WPT tank should be the focus, and then verifies a solution strategy using Litz wire and magnetic materials to improve efficiency. In [49], various types of ferrite structures are compared, and structure 4 is concluded to provide high

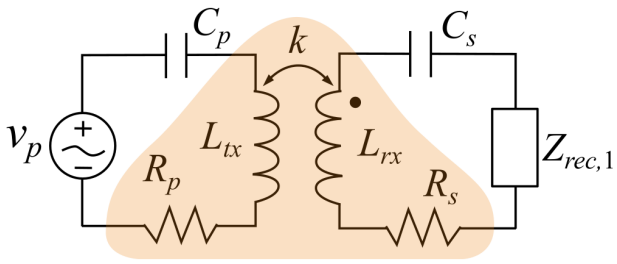


Figure 1.6: The WPT coils and their parasitic components as shown in the fundamental circuit model.

quality factor and misalignment tolerance. Soft magnetic composites are also considered for WPT applications [48]. However, much of the work with magnetic material is focused on kilowatt-level WPT [31, 48, 49], and while magnetic material is widely accepted as a useful tool for inductor design, incorporation of magnetic materials into the slim form factors of consumer devices is a non-trivial affair. Using an A10 coil during experimental verification (a coil commercially available for consumer device WPT), a soft magnetic structure is 84 % thinner than a conventional ferrite shield and reduces flux leakage by 20.9 % [57]. Another technique uses an advanced PCB structure with integrated magnetic nanocrystalline sheets, allowing ultra-thin printed coils to use magnetic material [58].

The coil link in Fig. 1.6 is the cornerstone technology that enables wireless power transfer. The coil-centric research work in the field of wireless power ultimately serves to increase the efficiency and viability of modern WPT system. Irrespective of the technological improvements, every WPT coil pair has loss mechanisms and a consequent loss profile. Understanding the loss characteristics of the coils used in a WPT system design is essential for the success of that design.

1.4.3 Tank Tuning

Impedance matching networks (IMNs) describe the topological ways of matching the WPT coils to their resonant capacitors. The compensation scheme of the fundamental circuit in Fig. 1.7a is "series-series". Because C_s is in series with L_{tx} and C_p is in series with L_{rx}, both the primary and secondary sides are said to be series compensated. There are four

dominate types of compensation: series-series (SS), series-parallel (SP), parallel-series (PS), and parallel-parallel (PP) [59]. The first descriptor always refers to the transmitter side and the second descriptor to the receiver side. For example, a PS compensation would mean that C_p is in parallel with L_{tx} and C_s is in series with L_{rx}. Fig. 1.7 shows examples of each of the four basic impedance matching network types.

Generally, series-series compensation is the most popular [24, 25, 34, 45, 59–63]. The SS design is shown to provide the lowest copper mass for a given efficiency, while PS provides the lowest operating frequency [60]. A genetic algorithm is used to find which compensation methods create the most robust WPT designs in terms of minimization of the input phase of the primary input impedance. SS and PS are cited as good candidates under this criteria [25]. The work in [59] again points to the SS design after comparing the four IMNs in terms of maximum efficiency, maximum load power transfer, load independence, k independence, and allowance of $k = 0$. The SS compensation approach to WPT is well documented in literature and serves as a sufficient tuning approach for many wireless power systems [59].

Other types of compensations schemes are sometimes used. The LCC compensation scheme includes an additional inductor and capacitor to tune either of the WPT coils [3, 64]. Combined with the control scheme in [64], the resonant frequency under this tuning is no longer a function of either the coupling coefficient or the load condition. Another approach tunes the primary and secondary sides with different IMNs. Retaining the simple one-capacitor tuning on the secondary side still leaves room for more complex tuning on the primary [35, 37, 65]. An extra capacitor on the primary side is called a CCL tuning [35], and

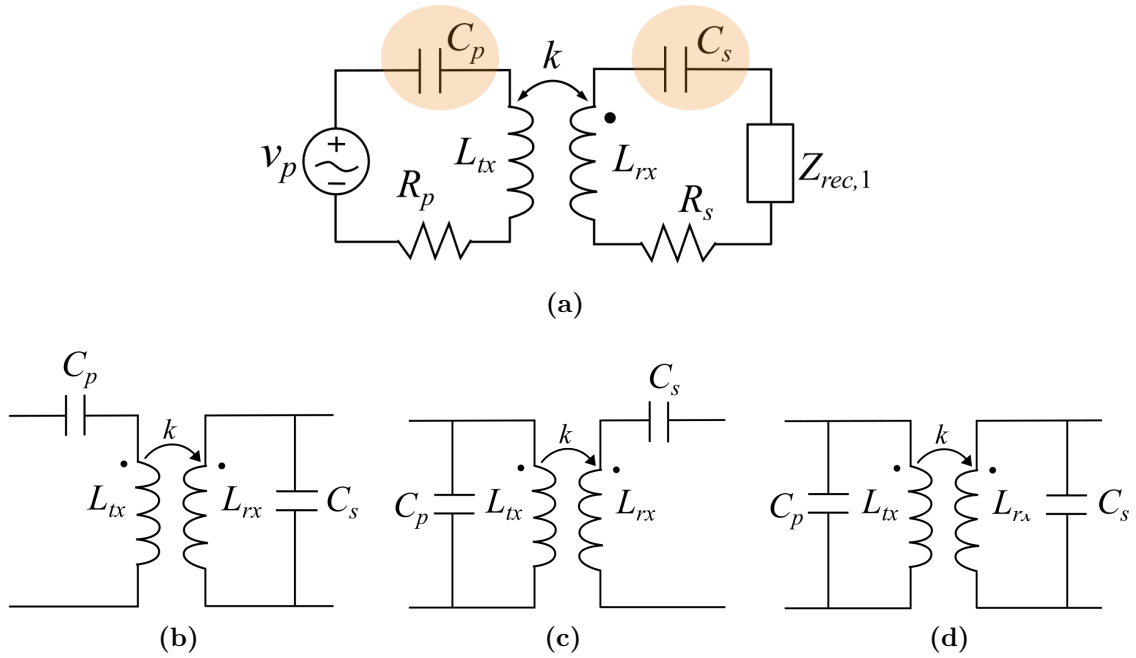


Figure 1.7: The four basic types of WPT compensation: (a) series-series (SS) as shown in the fundamental model, (b) series-parallel (SP), (c) parallel-series (PS), and (d) parallel-parallel (PP).

LCL tuning adds an single inductor [37, 65]. The LCL serves to decouple the transmitter current from the coupling value and load condition [37].

Each of these compensation schemes represents an operating space via the fundamental circuit model. While there are pros and cons to each tuning approach, characterization is possible for any of the impedance matching networks seen in literature. As an example, the series-series compensation style in Fig. 1.2a is characterized in Fig. 1.3. Generally, SS type tuning is sufficient to meet the demands placed on most WPT systems [24, 25, 34, 45, 59–63], but quantification of the design space is the most essential step to ensuring the successful implementation of a wireless charging platform.

1.4.4 Rectifier

The full wireless power system is comprised of an inverter, coupled coils, a tuning method, and a rectifier. The focus of this thesis is the WPT rectifier, depicted as a load in the fundamental model in Fig. 1.8. In the fundamental model, $Z_{rec,1}$ is the impedance presented to the WPT circuit by the rectifier. As outlined by the example in Fig. 1.3, there exist an optimal way of loading the WPT system with the rectifier impedance, highlighting the importance of considering $Z_{rec,1}$ when choosing a WPT rectification topology.

Given that the other elements of a WPT system are chosen (inverter, coils, and tuning), the rectifier is responsible for loading the system appropriately. Ideally, the rectifier presents the optimal $Z_{rec,1}$ such that the system-wide efficiency is maximized. For this reason, equivalent input impedance is an important metric for analyzing different designs.

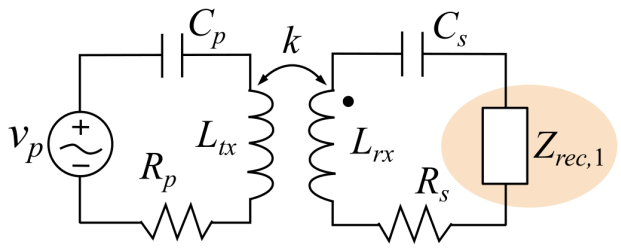


Figure 1.8: The rectifier is depicted as a load in the fundamental circuit model.

Likewise, there are other important metrics to consider during the design process. The efficiency metric is a given, as excess loss is not only inelegant but also produces heat, a poor characteristic for handheld devices. Evaluation metrics related to compactness and harmonic content are motivated in the next section.

1.5 Practical Rectifier Considerations

The consumer device architectures currently deployed in the market highlight additional challenges associated with in-device rectification design. As these devices get smaller and more power hungry, the space and loss allowances that constrain engineers get less forgiving. This section references devices currently available in the market in order to define evaluation metrics for comparing the different rectifier design approaches found in literature.

1.5.1 Compactness

Fig. 1.9 shows a breakdown of the iPhone 12 by Apple, released in late 2020. The opened cell phone, internal circuit board, and wireless power coil are shown in Figs. 1.9a-1.9c [7]. The tightly packed internal structure of the phone illustrates the density to which the power circuitry design must adhere. Furthermore, the entire iPhone 12 device is only a few millimeters thick and is comprised of multiple part layers (PCB, screen, wireless coil, mechanical case, etc.), meaning that all electrical components used must be very low-profile.

Reviewing the literature for WPT rectifier strategies reveals designs that, if implemented in a real system, likely would not be easy to fit into any form factor similar Fig. 1.9. For



(a) **(b)** **(c)**

Figure 1.9: iPhone 12 (a) breakdown, (b) circuit board, and (c) wireless charging coil [7].

example, a 11.2 W and 3.8 V wireless power system showcases 77.3% peak efficiency at $k = 0.6$ by leveraging an active rectifier and DC-DC converter [66]. However, the DC-DC converter is designed for a filter inductance of $L = 1$ μH, a part search for which returns a competitive inductor choice: ASPI-0425-1R0N-T3 by Abracon LLC [67]. This 1 μH inductor has a DCR of 12 mH and a 3A current rating (virtually no safety factor: 2.95 A = 11.2 W / 3.8 V), both of which are sufficient for the application. However, the ASPI-0425-1R0N-T3 is 2.5mm thick and has dimensions of 4mm x 4mm. For a single component, this is a very large area under the circuit density constraints implied by Fig. 1.9.

In general, this qualitative analysis motivates the use of rectification topologies that do not require large filter inductors. While including large inductances is likely possible in today's consumer devices, the size of such components makes them less competitive than other, more power dense components. For the purpose of this thesis, a metric of 'compactness' is introduced as a binary method of evaluating rectification strategies that simply denotes the presence or absence of a filter DC inductor. If a topology has a DC filter inductor, it is said to lack compactness. If a topology does not have a DC filter inductor, it is said to be compact.

1.5.2 Harmonic Content

Another circuit element currently available for purchase is the wireless power coil. Part number 760308101141 by Würth Elektronik is a high quality factor, 10 μH coil intended for wireless power applications at 150 kHz [8]. The quality factor at 150 kHz is reported at

220, signifying the potential for low-loss WPT system designs. However, the quality factor curve across a range of frequencies is shown in Fig. 1.10, and it shows how the quality factor rapidly drops off after the designed operating frequency.

The fundamental frequency of 150 kHz holds the maximum quality factor at ≈220, and the subsequent harmonics at 450 kHz, 750 kHz, and 1050 kHz show quality factors of ≈110, ≈85, and ≈50, respectively. Assuming the datasheet inductance remains constant at 10 μH, the equivalent series resistance (ESR) values at the fundamental, 3^{rd}, 5^{th}, and 7^{th} are 43 mΩ, 257 mΩ, 554 mΩ, and 1,320 mΩ, respectively. Given any significant amount of harmonic content in the tank currents, these large harmonic ESR values can cause deviation from the fundamental model by adding extraneous loss into the circuit.

A coil design with constant ESR helps to mitigate the potential harmonic losses from significantly influencing the loss profile. However, achieving a constant ESR across any significant frequency band is nearly impossible for WPT coil. Another approach is to eliminate the harmonic content of the power current conducting through the coil. In the absence of waveform distortion, the harmonic ESR values of the tank are irrelevant to the loss within the circuit. This interaction motivates rectification strategies that produce less waveform distortion. The implication of a rectifier that produces lower harmonic content is a higher overall system efficiency due to the I^2R harmonic interactions with component non-linearities like those in Fig. 1.10.

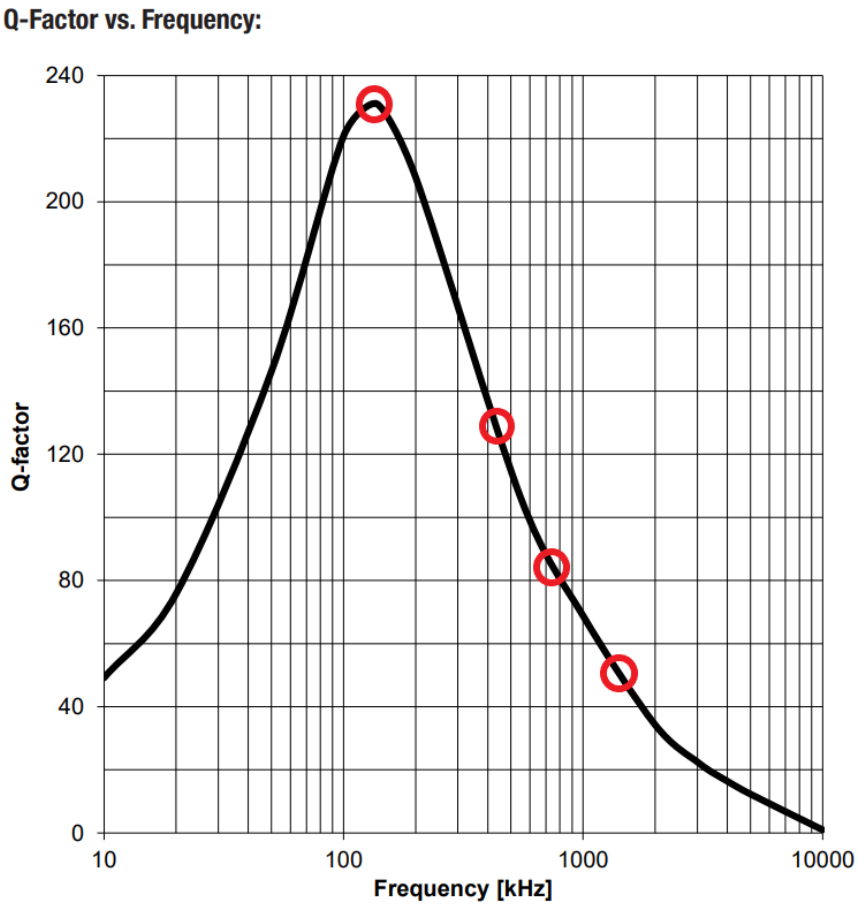


Figure 1.10: The quality factor of WPT coil part number 760308101141 verses frequency [8]

1.6 Rectifier Metrics

Finally, the fundamental model is an excellent basis for understanding the WPT system. Each of the pieces of the system is comprised of design choices that are covered in literature. The inverter, coupled coils, and tuning mechanisms are all relevant parts of a WPT system design, and are briefly covered in this chapter as a means to better understand the in-depth review of rectification strategies to follow in Chapter 2.

Metrics of evaluation are determined to help comprehensively compare each of the rectification strategies in literature. First, a high efficiency is required for any WPT rectifier. This is true for any power electronics circuit, but it is especially true here, where the converter must be packed into a small space and held in the end-user's hand. Next, the fundamental model highlights how the impedance of the rectifier influences the system-wide efficiency by influencing the steady state operating point. Therefore, rectifier's that present input impedances beneficial to the system are considered stronger candidates by this metric.

Third, a teardown of the newest iPhone available on the market illustrates the ever-tightening space and loss constraints for circuit designers. Densely packed, low-profile components are needed in order to fit inside small consumer devices. Here, inductors are non-optimal, and the metric of 'compactness' is introduced to describe the presence/absence of a DC filter inductor. Lastly, a WPT coil currently available to circuit designers exhibits dramatic quality factor fall-off after the designed operating frequency. Therefore, any rectifier capable of reducing the total harmonic distortion (THD) of the power waveforms within the tank is considered a strong candidate for use in WPT systems.

The four metrics are summarized by: efficiency, input impedance, compactness, and THD. These metrics serve as a framework for evaluating each of the rectifications strategies presented in depth in the following chapter.

Chapter 2

Literature Review

The fundamental circuit model depicts the rectification network as a simple linear impedance, but in practice, the rectifier takes an oscillating power and transform it into a DC power. The rectifier's DC output either directly charges the device battery or is first regulated and then charges the battery. In either case, the rectifier is responsible for receiving the power from the WPT tank, and in doing so, presents a load to the rest of the WPT system. As outlined in Chapter 1, the impedance presented to the system is an important quality of any WPT rectification technique. This input impedance, combined with circuit efficiency, compactness, and waveform distortion are the markers used to compare different rectification techniques.

These four markers are an important framework for highlighting a gap in the literature and the potential research gains therein. This literature review surveys multiple rectification strategies, motivating how the topology presented in Chapter 3 fills a gap in the current

knowledge-base. First, the simplest WPT rectification technique is the passively switched diode circuit.

2.1 Diode Rectifiers

Topologies that incorporate diodes are common in wireless power transfer systems [9–11, 14, 68, 69]. Passively switched rectifiers are very simple to implement and require no control circuity. The work in [9] focuses on dual-band design of the WPT tank and requires some type of rectifier for experimental verification, and a full bridge diode rectifier is chosen. During testing, the rectified DC voltage is kept constant across different values of R_{load} by tuning the inverter source voltage [9]. This test illustrates a broader concept for passive diode full bridge rectifiers: they have no control over the input impedance they present to the wireless power circuit.

The diode full bridge can only conduct such that $v_{rec} = \pm V_{out}$ as shown in Fig. 2.1. The waveforms show that the input voltage is equal to the output voltage when the current is positive, and the inverse is true when the current is negative. Insofar as the diode parasitics are negligible at the fundamental operating frequency, the rectifier's fundamental input reactance is zero [11].

Under the fundamental model, the equivalent load of an ideal diode full bridge is

$$Z_{rec,1} = R_{rec,1} = \frac{8}{\pi^2} R_{load} \quad [12], \tag{2.1}$$

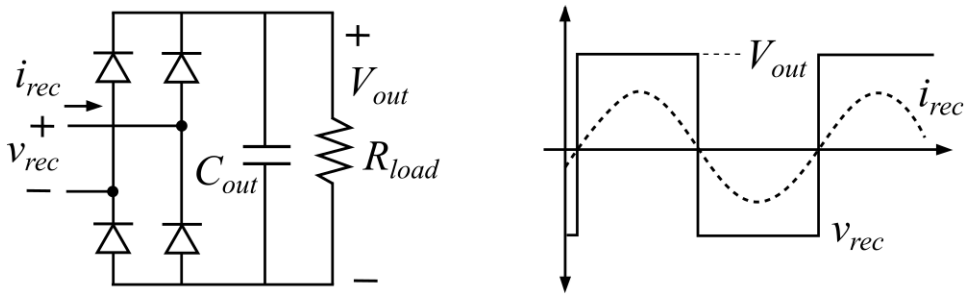


Figure 2.1: A diode full bridge rectifier and waveforms [9–11].

because the reactive component is zero. The equivalent impedance is a function of R_{load} alone [12]. Given a set of conditions (coupling value, inverter voltage, and R_{load}) the output voltage and output power are fixed values. Because R_{load} and k are not generally values directly controlled by the WPT system, the traditional control parameter is V_{in}. If a WPT circuit is optimized for maximum efficiency at a certain set of operating conditions, the inevitably varying coupling factor pushes the system to a sub-optimal operating point, requiring a change in inverter voltage to improve efficiency. The downside is that this requires communication with the transmitter and creates reliance on the primary side for power control.

2.2 Output Regulation

A common approach to WPT loading includes a regulating converter after the rectifier stage. The most conventional implementation is the diode full bridge with a DC-DC converter placed between the rectifier and the battery [12, 13]. Fig. 2.2 illustrates how the waveforms are similar to the case with no DC-DC converter, but the input voltage of the rectifier is now $v_{rec} = \pm V_{bus}$. The conversion from V_{bus} to V_{out} is set by the DC-DC converter, a buck converter in this case. In a lossless system, the input impedance of the diode full bridge now includes a duty cycle term:

$$Z_{rec,1} = R_{rec,1} = \frac{8}{\pi^2}\frac{1}{D^2}R_{load} \quad [12]. \tag{2.2}$$

This approach allows the rectifier stage to vary the real portion of its input impedance via the conversion ratio of the DC-DC module [12]. Another way to understand the impact of the DC-DC converter is to refer back to the diode full bridge equation. Effectively, the buck converter changes the R_{load} perceived by the rectifier, thereby making the impedance varied around the impedance defined in (2.1).

If a DC-DC converter is set to regulate the output voltage so that V_{out} does not change as k varies, then a resistor-loaded system operates with a constant output power irrespective of the WPT tank alignment and distance. Similarly, a voltage-loaded system (i.e. battery) may be set to regulate output current. From the perspective of the fundamental model, $Z_{rec,1}$ is changing with k so that the real power delivered to $Z_{rec,1}$ remains constant for each operating point.

Another approach replaces the traditional buck or boost converter with a switched capacitor converter (SCC) [70–76]. An SCC is applied to a system for post-rectification output voltage regulation in [73]. Conversion without a large filter inductor is advantageous, but SCC DC-DC topologies are generally limited to fixed conversion ratios, a drawback for secondary-side WPT rectification circuits [77].

This same end can be accomplished without a DC-DC converter. The work in [15] leverages an LDO to regulate the output voltage of an active full bridge rectifier. Another research work adds a single active switch and two additional diodes to a traditional diode full bridge rectifier, and adjusting the switching times of the active switch enables output control [68]. Another approach shorts the rectifier at the input ($v_{rec} = 0$) and oscillates

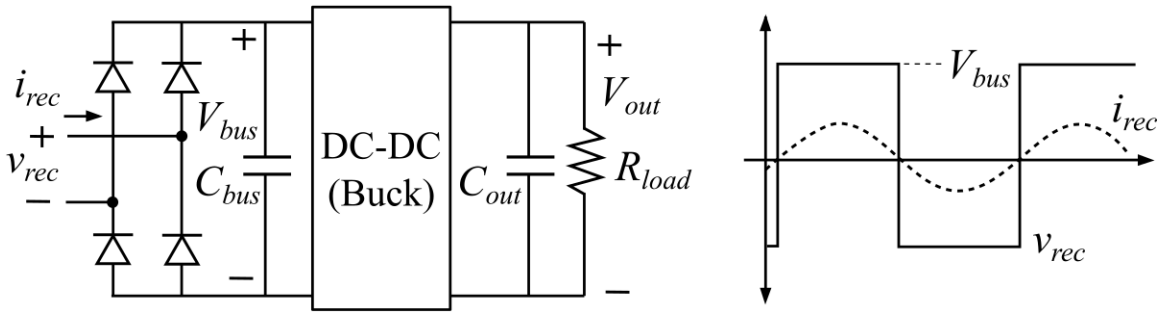


Figure 2.2: A diode full bridge rectifier with a DC-DC converter and the accompanying waveforms [12, 13].

between charging the load and circulating the power current such that the average output voltage converges to the desired regulated value [18].

One method uses the resonant regulating rectifier (R^3), a circuit that encompasses voltage multipliers and MOSFETs used to change the operating mode [14]. This rectifier is a diode-based topology that is designed based on a voltage quadrupler [14]. The approach adds three switches and turn the rectifier on and off to regulate the output. Fig. 2.3 shows the output voltage climbing due to the (x4) effect of the rectifier during the on period and slowly falling as the rectifier is disconnected during the off period. The feedback signal is a simple comparison to the voltage reference as shown in Fig. 2.3 [14].

The fundamental input impedance of the diode full bridge and buck converter topology (DFB + buck) is summarized by (2.2). Other techniques use LDOs [15], additional switching components [68], shorting intervals [18], or R^3 topologies to regulate the output voltage. Fundamentally, these approaches are doing the same things as the DC-DC converter: varying the real portion of the rectifier's input impedance, $Z_{rec,1}$, to control the power throughput. This principle of regulation influences the design of many WPT systems, and improves the system's ability to respond to various changes in tuning.

2.3 Diode Emulation Active Rectifiers

The full bridge topology can also be implemented with actively controlled switches [13, 15–18, 69]. Some implementations use a combination of passive and active switches [69],

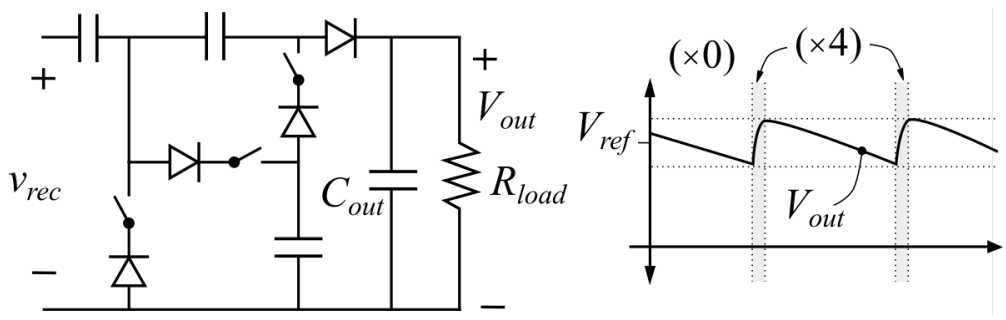


Figure 2.3: Resonant regulating rectifier based on a voltage quadrupler that regulates the output voltage via simple comparison with a reference value [14].

while others are comprised of nothing but active switches [13, 15–18]. The most common implementation for these active topologies is diode emulation [15–18, 78–85].

For an active full bridge circuit, the devices are switched on and off whenever the controller sends the appropriate signals. In contrast to a diode, active switches do not actuate based on the power circuit waveforms (unless the body diode of the MOSFET is forward biased). This control freedom enables the rectifier to conduct the secondary current using a number of different switching configurations during the course of one fundamental operating period. However, the common technique of diode emulation trades this control freedom for simplicity and actuates the switches in the same manner as a diode would actuate if it were in the circuit [15–18, 78–85].

Fig. 2.4 shows the active full bridge rectifier and the accompanying waveforms. Generally, some type of sensing circuitry is used to align the rectifier's input current with the switching actions [17]. The work in [17] defines reverse leakage current as the product of the "delayed or erroneously operated gate input signal." Reverse leakage current is the result of a switch conducting too long, and the goal of in-phase switching is to eliminate reverse leakage without blocking any forward current. The work in [17] uses an enhanced zero crossing detection circuit and a deglitching circuit to address the reverse leakage current problem. Current sensors are often applied to active rectifiers for the purpose of in-phase switching [15–17]. Often, circuits use some type of strategy to account for the propagation delays of the sensing and control circuitry in order to reduce or entirely remove reverse leakage current. These strategies include empirical delay compensation tuning [85], delay lock loops (DLLs) [78,

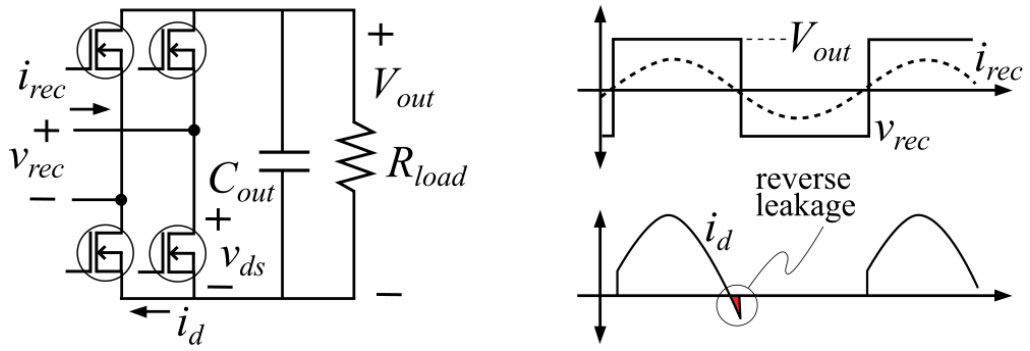


Figure 2.4: Actively switching rectifier doing diode emulation. A small switching delay results in reverse leakage loss [15–18].

80, 81], high speed comparators [82], and successive approximation register (SAR) or other algorithms for real-time calibration of switching signals [83, 84].

Some applications connect two of the switch gates to the half bridge switch nodes [78–80, 82–84, 86]. This is especially common for diode-switched synchronous rectifiers [78–80, 82–84]. In this case, the two switches with their power-circuit-connected gates do not need to be driven by control circuitry, simplifying the overall control. A control strategy is proposed in [79], where these power-circuit-connected gates are sensed and the other two gates in the full bridge are driven to match these signals. While these types of topology adjustments may simplify control, they also restrict the circuit. For instance, in [83] the low-side GaN devices have their gates tied to the half-bridge switch nodes. This means that the rectifier's output voltage cannot exceed the V_{gs} rating of the low-side devices without breaking the circuit. Therefore, this scheme is non-ideal in applications where the rectifier's DC output voltage must vary greatly. Overall, diode-switched active rectifiers exchange diode conduction losses for the reduced losses of MOSFETs, require control circuitry, and sacrifice inherent control freedoms for the purpose of simplicity, all the while maintaining the same power waveforms as diode rectifiers.

2.4 Active Rectifiers

Actively switched rectifiers enable full control of the rectifier impedance. The duty cycle and switching-delay capabilities allow the magnitude and phase of the rectifier's equivalent input impedance to be varied by the controller [26, 66, 87]. The maximum efficiency (reactance

matching) and maximum power transfer (conjugate matching) operating points do not occur at the same rectifier load condition. Furthermore, designing a rectifier for maximum efficiency at a single point disallows that same system to reach peak efficiency at other operating points unless some circuit impedance changes accordingly.

Via the fundamental model, the system-wide efficiency is shown to be a function of both the real and reactive portions of the rectifier load in

$$\eta = \frac{\omega^2 L_M^2 R_{rec,1}}{R_p((R_s + R_{rec,1})^2 + (\omega L_s - 1/\omega C_s + X_{rec,1})^2) + \omega^2 L_M^2 (R_s + R_{rec,1})} \quad [26], \tag{2.3}$$

where $Z_{rec,1} = R_{rec,1} + jX_{rec,1}$ in accordance with the fundamental model. This equation for peak efficiency complements the equation for optimal complex loading in (1.5), as they both illustrate the need for $X_{rec,1}$ in order to match a tank when $|Z_{Cs}| \neq |Z_{Lrx}|$. The rectifier controls the magnitude of its impedance by regulating V_{out} via duty cycle or some other control method [26, 66]. By varying the switching times, the rectifier establishes control of the angle of its input impedance, $\angle Z_{rec,1} = \phi_{rec,1}$.

The complex impedance and real/imaginary components all describe the same system from a different point of view:

$$Z_{rec,1}(\phi_{rec,1}, V_{out}) = R_{rec,1} + jX_{rec,1} = \frac{4}{\pi} \frac{V_{out}}{|i_s|} \Big(\cos(\phi_{rec,1}) - j \sin(\phi_{rec,1}) \Big) \quad [26]. \tag{2.4}$$

Coupled with (1.5), equation (2.4) implies that an active rectifier system is able to tune the system reactance with imaginary component $X_{rec,1}$ and regulate the power output with $R_{rec,1}$.

Ultimately, equation (2.4) shows how the rectifier is able to set $\phi_{rec,1}$ and V_{out} such that $Z_{rec,1}$ matches $Z_{rec,opt}$ in (1.5) and both $R_{rec,1}$ and $X_{rec,1}$ maximize (2.3). The phasor and complex representations of the WPT system represent the same characteristic: a synchronous rectifier is able to set its input impedance to optimize the system efficiency [26, 66].

2.5 Comparison of WPT Rectification Strategies

The types of rectifiers are summarized in terms of the fundamental circuit model in Table 2.1. The diode full bridge (DFB) always represents a single impedance, characterized by (2.1). When paired with a DC-DC converter, $|Z_{rec,1}|$ becomes variable as represented in (2.2). The buck converter sets the theoretical upper limit of $|Z_{rec,1}|$ to ∞. The DFB + SCC has the same limits as the DFB + buck, but the SCC converter generally only regulates to fixed voltage ratios [77]. These non-continuous conversion characteristics result in discrete steps in $|Z_{rec,1}|$, rendering the DFB + SCC strategy only marginally effective. The active full bridge converter (AFB) introduces phase control [26, 66], which is limited to $\pm\pi/2$ in accordance with the natural limits of passive loads. The upper limit of $|Z_{rec,1}|$ for the AFB matches the DFB impedance because this is the point of diode-emulation, where the active rectifier is switched as an in-phase square wave [15–18, 78–85]. The active full bridge reduces $|Z_{rec,1}|$ by varying its duty cycle, mimicking the step-up behavior of a DFB + boost topology [26, 66]. Finally, the active full bridge + buck topology combines the benefits of the AFB with the DC bus down-regulation capabilities of the buck converter, theoretically capable of reaching any value of $Z_{rec,1}$.

Table 2.1: Theoretical Rectifier Impedances

Topology	$\lvert Z_{rec,1}\rvert$	$\angle Z_{rec,1}$
DFB	$\lvert Z_{rec,1}\rvert = {}^{8}/_{\pi^2} R_{load}$	$\angle Z_{rec,1} = 0$
DFB + Buck	${}^{8}/_{\pi^2} R_{load} \leq \lvert Z_{rec,1}\rvert < \infty$	$\angle Z_{rec,1} = 0$
DFB + SCC	$\approx {}^{8}/_{\pi^2} R_{load} \leq \lvert Z_{rec,1}\rvert < \infty$	$\angle Z_{rec,1} = 0$
AFB	$0 \leq \lvert Z_{rec,1}\rvert \leq {}^{8}/_{\pi^2} R_{load}$	$-\pi/2 \leq \angle Z_{rec,1} \leq \pi/2$
AFB + Buck	$0 \leq \lvert Z_{rec,1}\rvert < \infty$	$-\pi/2 \leq \angle Z_{rec,1} \leq \pi/2$

[9, 12, 13, 15–18, 26, 66, 77–85]

Table 2.2: Example Tank Values

L_{tx}	L_{rx}	C_p	C_s	R_p	R_s	k	V_{in}
10 μH	10 μH	125.6 nF	125.6 nF	200 mΩ	100 mΩ	0.55	26 V

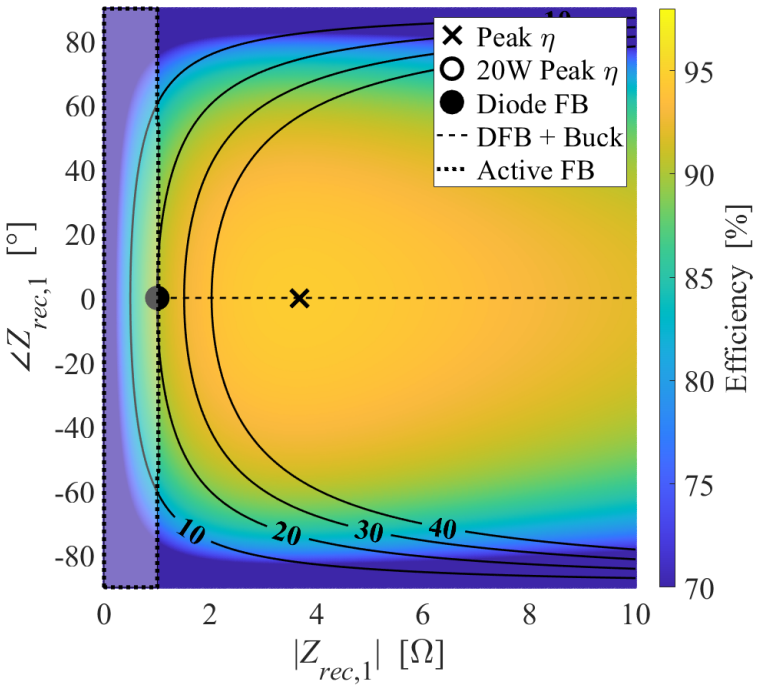


Figure 2.5: Example operating point for reference. Both sides of the WPT tank are tuned for resonance, $k = 0.55$, and $V_{in} = 26$ V

To illustrate the impedance tuning advantages and disadvantages of each topology, an example tank is given in Table 2.2. The tank is tuned so that the $L_{tx}|C_p$ and $L_{rx}|C_s$ pairs resonate at the fundamental. The example design sets $R_{load} = 1.25\ \Omega$ and $V_{out} = 5$ V so that $P_{out} = 20$ W. The resulting graph shown in Fig. 2.5 contains information about the peak efficiency point for the tank, power contours, the 20 W peak efficiency point, and operating points of various rectifications strategies. The tank is designed so that the diode full bridge loads the system at the most efficient 20 W operating point. The DFB + buck is shown as a dotted line at $\angle Z_{rec,1} = 0$, enabling the system to traverse different power levels and efficiency values while maintaining an output voltage of $V_{out} = 5$ V. For this tank design, the DFB + buck operates at the same operating point as the solo DFB, as the 20 W and 5 V design parameters are met without the need for DC bus conversion. The synchronous full bridge is denoted in Fig. 2.5 by a smaller dotted line and a translucent white region. This active rectifier is able to present impedance magnitudes up to the DFB impedance accompanied by control of $\angle Z_{rec,1}$. Finally, an AFB + buck converter is theoretically capable of reaching all the impedance values in Fig. 2.5, and therefore is not explicitly pictured.

Fig. 2.6 shows the same example operating point with variations to coupling value, input voltage, and fundamental frequency (set by the primary side). The output resistance is varied so that the output voltage remains a constant $V_{out} = 5$ V. Isolating each of these variations highlights the benefits of each rectification strategy. First, the diode full bridge is incapable of reaching the desired operating point in any of the varied cases. Across the variations, the DFB output power varies from 10.35-to-31.49 W. The strategy for regulating

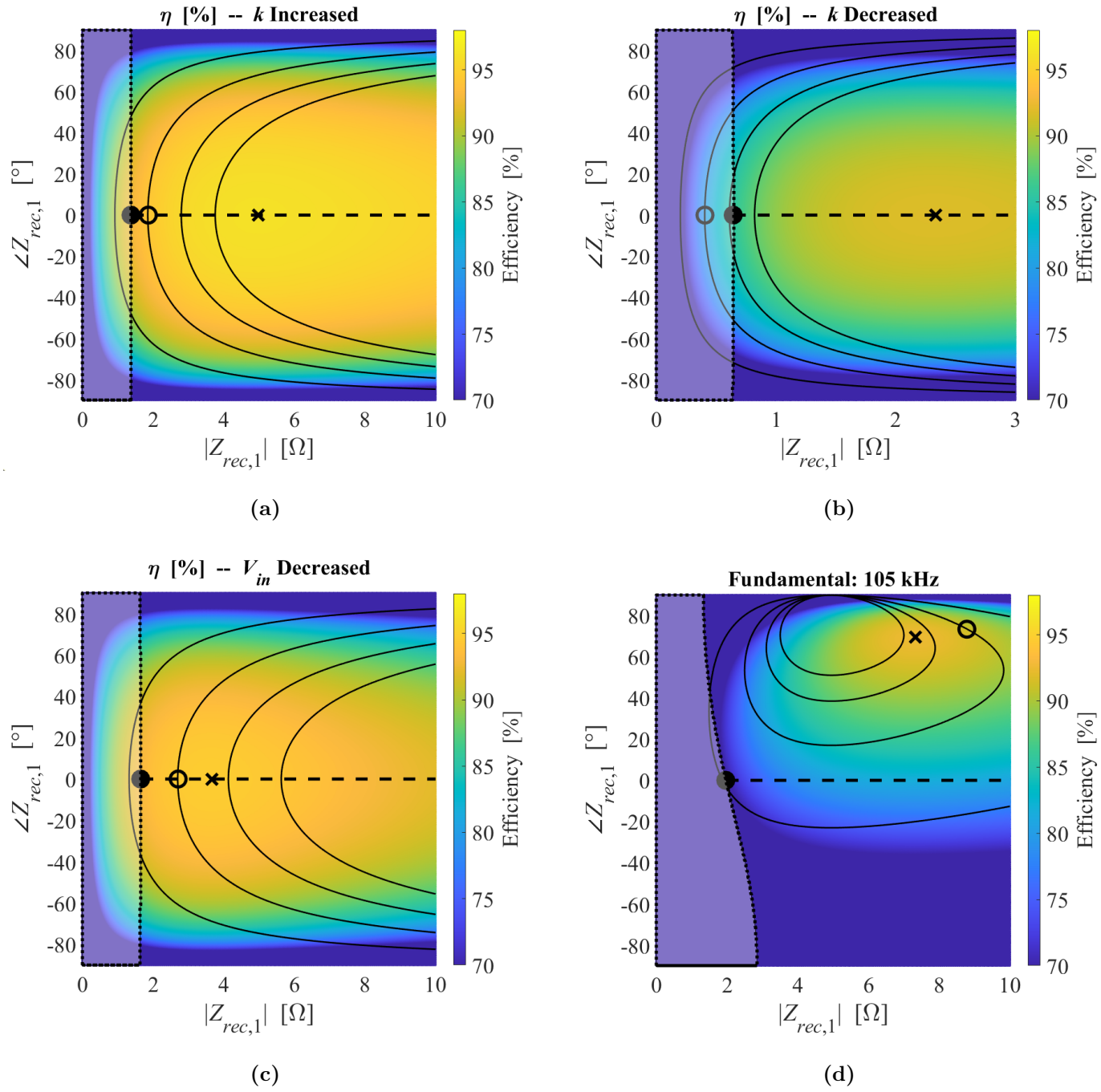


Figure 2.6: Variations of the example from Fig. 2.5 with changes of (a) increasing k to 0.75, (b) decreasing k to 0.35, (c) lowering V_{in} to 16 V, and (d) reducing the fundamental frequency to 105 kHz.

the output voltage with DFB is varying V_{in} as in [9]. However, this requires communication with the primary side, and creates dependence on an outside circuit for load regulation.

The topologies that include converters for DC bus regulation address this tuning issue [12, 13]. The DFB + buck topology is able to reach the highest efficiency 20 W power contour in two of the scenarios of Fig. 2.6. However, when k is decreased in Fig. 2.6b, the only option to reach 20 W requires V_{in} again be raised from the primary side, recreating the communication dependence. When step-up regulation and reactive impedance ($\angle Z_{rec,1}$) are not needed, this strategy is sufficient, but Figs. 2.6b and 2.6d show the shortcomings of this approach.

Finally, the active full bridge strategy exhibits control over the full impedance $Z_{rec,1}$ [26, 66], and mimics the impedance transformation of a step-up boost converter via duty cycle. The AFB pictured in Fig. 2.6b is able to regulate to the peak efficiency point, but Figs. 2.6a, 2.6c, 2.6d once again require the use of a step-down type conversion to track the most efficient point. An AFB + buck is not pictured but is able to reach any operating point in Fig. 2.6, making it the only approach capable of tracking the optimal efficiency point for the fourth example in Fig. 2.6d.

However advantageous, each of these approaches has some drawback. Those with DC-DC converters require multiple stages and often a non-compact filter inductance [88–90], thereby failing the compactness metric. Traditional DC-DC switched capacitor converters exhibit fixed conversion ratios [77], so continuous output regulation is difficult. Furthermore, full bridge rectification techniques produce anything from a square wave (DFB) to a modified square wave that includes a $v_{rec} = 0$ interval (duty modulated AFB) at the input of the

rectifier. These waveforms contain significant harmonic content, thereby reducing the system efficiency in accordance with the harmonic ESR values of WPT coils. Fig. 2.6 also shows how the duty modulated AFB is limited to the equivalent of DC-DC step-up conversion, lacking the ability to step-down the output (increase $Z_{rec,1}$).

The example in Figs. 2.5 and 2.6 illustrates the loading advantages associated with the various rectification strategies. Given that WPT platforms are used by end-consumers, the platforms must be equipped to handle a variety of non-optimal conditions, and therefore the example highlights the need for both step-up and step-down bus conversion (or the functional equivalent). The rectifier plays an important role in re-tuning the system when the operating point is non-ideal via full control of its input impedance.

Table 2.3 summarizes the benefits of each rectification approach, breaking impedance control into three sections for increased clarity. The efficiency metric is implied for each topology. Table 2.3 demonstrates the shortcomings of the literature. Generally, those methods with thorough control of $Z_{rec,1}$ sacrifice compactness, and in the case of the DFB + SCC approach, $\angle Z_{rec,1}$ is sacrificed and $|Z_{rec,1}|$ is limited. Furthermore, none of the approaches address waveform distortion.

The multi-level switched capacitor (MSC) rectifier proposed in this thesis is a highly efficiency approach to WPT secondary-side rectification. The topology addresses each metric put forth in Table 2.3, and it therefore fills a gap in the current literature. The approach showcases step-up and step-down regulation, reactance injection, requires no DC filter inductor, and leverage a low-distortion staircase waveform. For any active rectifier with the capability of real-time impedance control, multiple control loops are required

Table 2.3: Comparison of Rectification Strategies

	Compact[1]	$\lvert Z_{rec}\rvert \downarrow$	$\lvert Z_{rec}\rvert \uparrow$	$\angle Z_{rec}$	THD$\downarrow$
DFB	✓				
DFB + Buck			✓		
DFB + SCC	✓	2	2		
AFB	✓	✓		✓	
AFB + Buck		✓	✓	✓	
MSC	✓	✓	✓	✓	✓

1. "compactness" is a binary metric based on the absence of a filter inductor.
2. SCC converters have defined voltage conversion ratios, so impedance regulation is limited to discrete steps.

for implementation and consequent realization of the circuit's full benefit. The control problems are reviewed in the next section with respect to other active wireless power rectifier implementations.

2.6 Control of Active Rectifiers in WPT Systems

Active rectifiers in WPT systems are capable of increasing rectification efficiency, regulating load voltage, and providing real-time system tuning [91–94]. However, any receiver-side WPT active rectifier requires some form of sensing in order to isolate and match the carrier frequency. Switching too quickly or too slowly will cause phase drift, thereby changing the equivalent impedance of the rectifier and negatively impacting the WPT system [94, 95]. Synchronous rectifiers are also often modulated for output regulation via closed-loop output sensing [26, 66, 94]. These two issues provide an interesting dual-loop control problem for active rectifiers in wireless power transfer systems.

2.6.1 Output Regulation

Active rectifiers are capable of regulating the output load by varying their switching times [26, 66, 93]. Regulating the output is equivalent to system retuning via $Z_{rec,1}$. When an active rectifier varies any set of switch on-times, either the phase or magnitude of the rectifier's equivalent input impedance is predominantly affected. By delaying every switching time, equivalent phase is leveraged to control the output [66]. Similarly by varying the rectifier's duty cycle (or the topological equivalent), a change in the impedance magnitude is used for

regulation [26, 66]. These impedance tuning mechanisms drive the axes of Figs. 2.5 and 2.6, pushing the WPT system to the desired output characteristic.

The work in [96] proposes a modulating technique for a semi-bridgeless active rectifier that only varies the magnitude of the equivalent input impedance without affecting the switching phase within the period [96]. The work in [66] states that either a DC-DC converter or active rectifier duty cycle can be used to regulate the output. Shorting control is used to regulate the output voltage in [18], which effectively changes the rectifier impedance between some nominal value and $Z_{rec} = 0$ at a ratio that averages to the impedance necessary for the desire output voltage.

From the perspective of the fundamental circuit model, each of these approaches is accomplishing the same end by different means. Impedance $Z_{rec,1}$ is edited, re-loading the WPT system until the desired output voltage or power is achieved. The concept is well-documented in literature [18, 26, 66, 93, 96] and is not novel on its own.

2.6.2 Frequency Synchronization

Due to the electrical isolation inherent to WPT systems, the switching frequency of any WPT active rectifier must be exactly synchronized to the carrier frequency. Fig. 2.7 illustrates how some research works bypass the frequency synchronization issue by driving the primary and secondary sides by the same controller [26, 66]. Others do not address the controller at all [96, 97]. These works focus on other WPT-related issues like switch design [97],

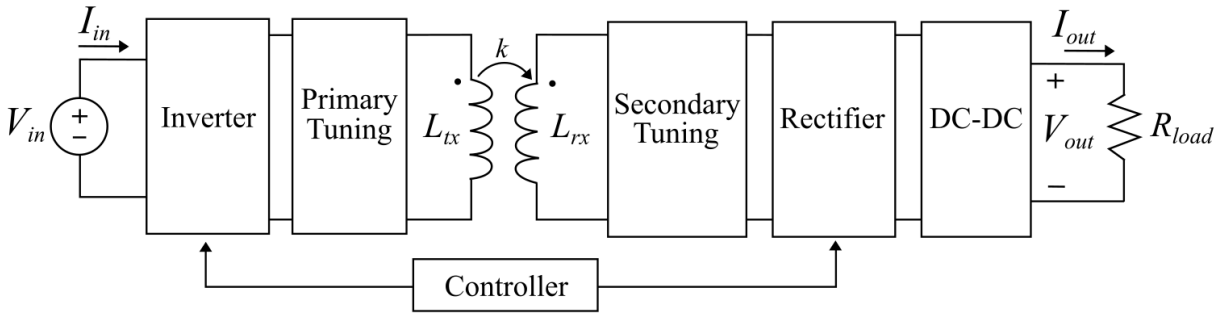


Figure 2.7: A single controller driving both sides of a WPT system.

modulation scheme [96], or WPT system tuning [26, 66] without considering the real-world problem of synchronizing frequency.

One synchronization approach is to sense the voltage across the switching devices. With the assumption that the active rectifier always switches with zero input phase, the devices are actuated with a change in voltage polarity [79, 98]. This technique relies on fast sensing to reduce conduction loss by forcing the switches to act as near-ideal diodes. A metric often used to measure how closely these techniques imitate an ideal diode is the presence of "reverse current" through the switches [79, 98]. With this approach, the active system loses the control freedom of variable switch timing, and the WPT system consequently loses a potential tuning mechanism [94].

Some techniques sense other circuit parameters like secondary current [99, 100] or secondary capacitor voltage [101]. A lower power implementation for smart watch applications senses the WPT magnetic field and uses it to generate a clock. This clock serves as a reference for synchronously switching the secondary side [102]. Control freedom is again sacrificed in these approaches because each switch is operated as an ideal diode [99–102].

Another strategy is to simplify or disregard plant dynamics [27, 103]. If the power stage model is quasi-static, a phase-lock loop (PLL) can be used to control the switching frequency [27]. This technique assumes that the high-frequency feedback effects of the power stage will not significantly influence the synchronization PLL. The trade-offs to this solution are the lower bandwidth. While a high resolution for frequency assignments may help

mitigate the negative effects of slower control response, a system without a high-frequency plant model is incapable of reliably predicting stability at high bandwidths. Experimental settling times from 110 ms to 140 ms are demonstrated for a system using a digital PLL to synchronize frequency, but no model comparison is provided for these results [103].

One other WPT system is capable of working with both 6.78 MHz and 100-205 kHz frequencies alike. It uses a clock recovery circuit, compares the sensed frequency to an internal oscillator, and chooses the correct operating mode. On the secondary side, the system uses a synchronous rectifier and a buck converter [13].

2.6.3 Dual-Loop Operation and Control Novelty

It is possible to combine frequency synchronization and output regulation without communication between the primary and secondary sides [102, 104, 105]. The work that senses the WPT magnetic field operates the switches as ideal diodes until the output crosses a threshold, and then the rectifier switches modes to withhold energy throughput [102]. In [104, 105], three signals are sensed: input voltage, input current, and output voltage. Because all control parameters are interdependent, frequency synchronization is verified when the output voltage error term goes to zero [104, 105]. These works still lack discussion of synchronization transient times and small signal predictions of loop-stability [104, 105].

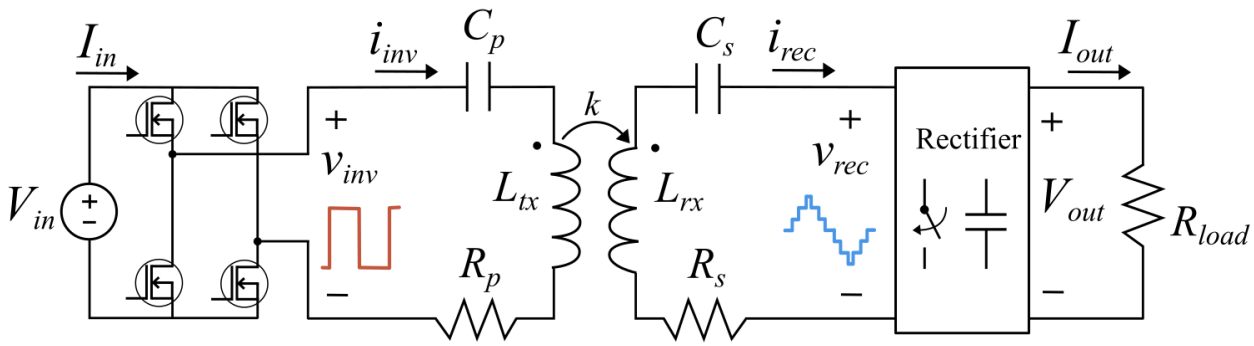
Based on the current literature, both output regulation and frequency synchronization loops have both been stably implemented in WPT systems. Furthermore, stable dual-loop operation has been demonstrated [102, 104, 105]. At present, no power circuit model for the

frequency control loop includes high-frequency plant dynamics, and there exists, therefore, an opportunity to develop a plant model to be validated for higher frequency control bandwidths. Therefore, this thesis builds upon a discrete time mathematical framework in order to develop such a plant model, and applied to the MSC, demonstrates experimental verification of such a high-bandwidth synchronization control loop.

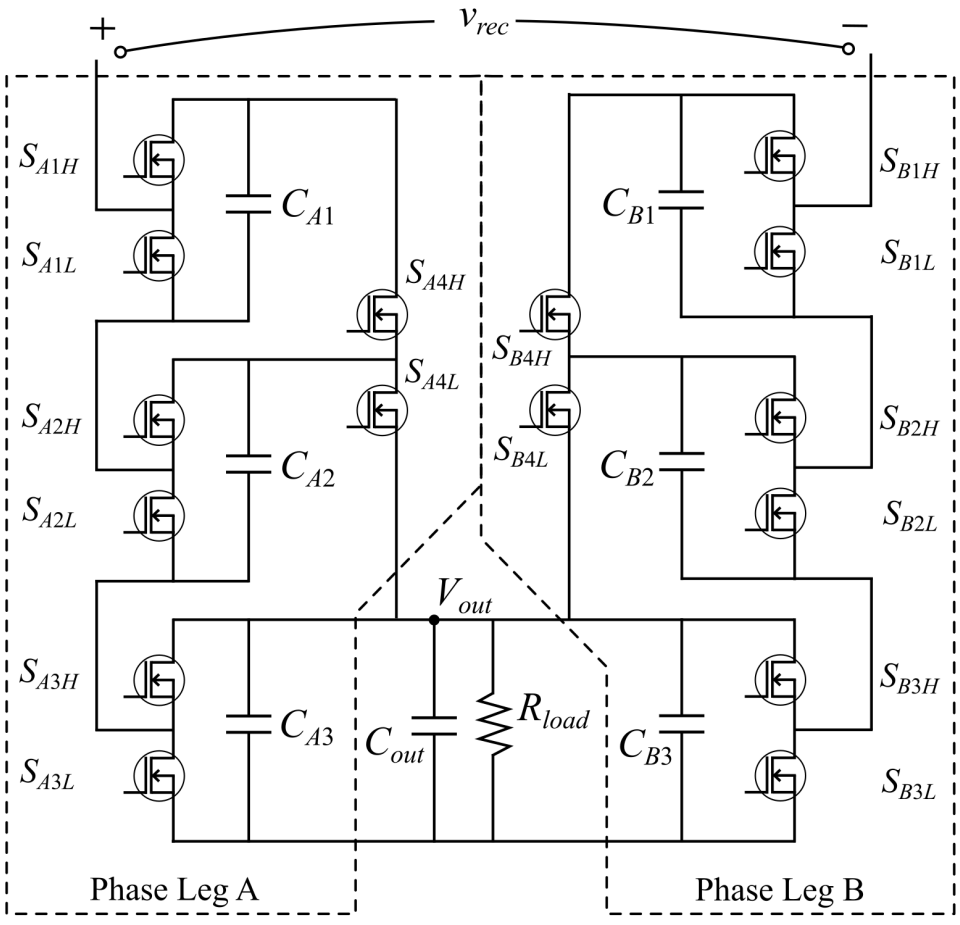
Chapter 3

Introduction to the Multi-Level Switched Capacitor Rectifier

The multi-level switched capacitor rectifier [106] brings significant benefit to a wireless power transfer system, but designing the rectifier to gain these benefits requires an understanding of the WPT system, the rectifier losses, system-loading, and rectifier control limitations. This chapter outlines the main concepts necessary for high-level design of a WPT system using the 7-level SC rectifier and includes a power loss model based on the fundamental frequency. These high-level concepts serve as the foundation for the more complex and holistic approaches to follow in subsequent chapters.



(a)



(b)

Figure 3.1: (a) The complete WPT system and (b) the proposed 7-level rectifier topology.

3.1 WPT System and Rectifier Circuit

The complete wireless power transfer system in this work is comprised of an inverter, tuned tank, and a 7-level switched capacitor rectifier. Fig. 3.1a shows an overview of the WPT network. Voltage source V_{in} is assumed ideal, and the tank is series-series compensated by C_p and C_s. Variable k is the strength of the magnetic coupling, and R_p and R_s are the at-frequency ESRs of the tuned primary and secondary coils, respectively. A full-bridge inverter is used to generate the sinusoidal (plus harmonics) input to the WPT tank. The fundamental frequency for the system is 150 kHz unless otherwise noted.

The 7-level switched capacitor rectifier is shown in Fig. 3.1b. Each of the flying capacitors (C_{A1}... C_{B3}) and the output capacitance (C_{out}) has some small ripple around their DC value, V_{out}. Switches S_{A1H} through S_{B4L} all serve to insert, remove, or balance the flying capacitors. The S_{x4x} switches (all switches with a "4" in the subscript) are called the "charge sharing" switches because their primary function is to connect the power capacitors together so that the voltages redistribute accordingly. Fig. 3.2 shows how the rectifier can be configured to pass i_{rec} without any of the flying capacitors in the path. The blue path shows the main current carrying path, and the red path shows the nodes shorted together (via the charge sharing switches) for the purpose of balancing the capacitor voltages. In Fig. 3.2, each of the seven capacitors is connected in parallel for balancing, and while it is possible for current to flow negatively through one capacitor and return through another, the typical illustration of the path of i_{rec} does not include these paths.

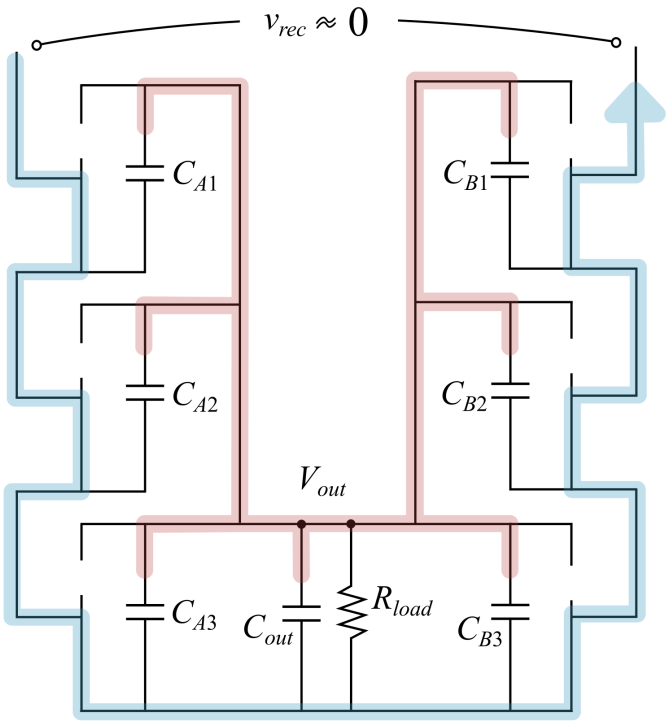


Figure 3.2: Example configuration illustrating all capacitors balancing and $v_{rec} = 0$.

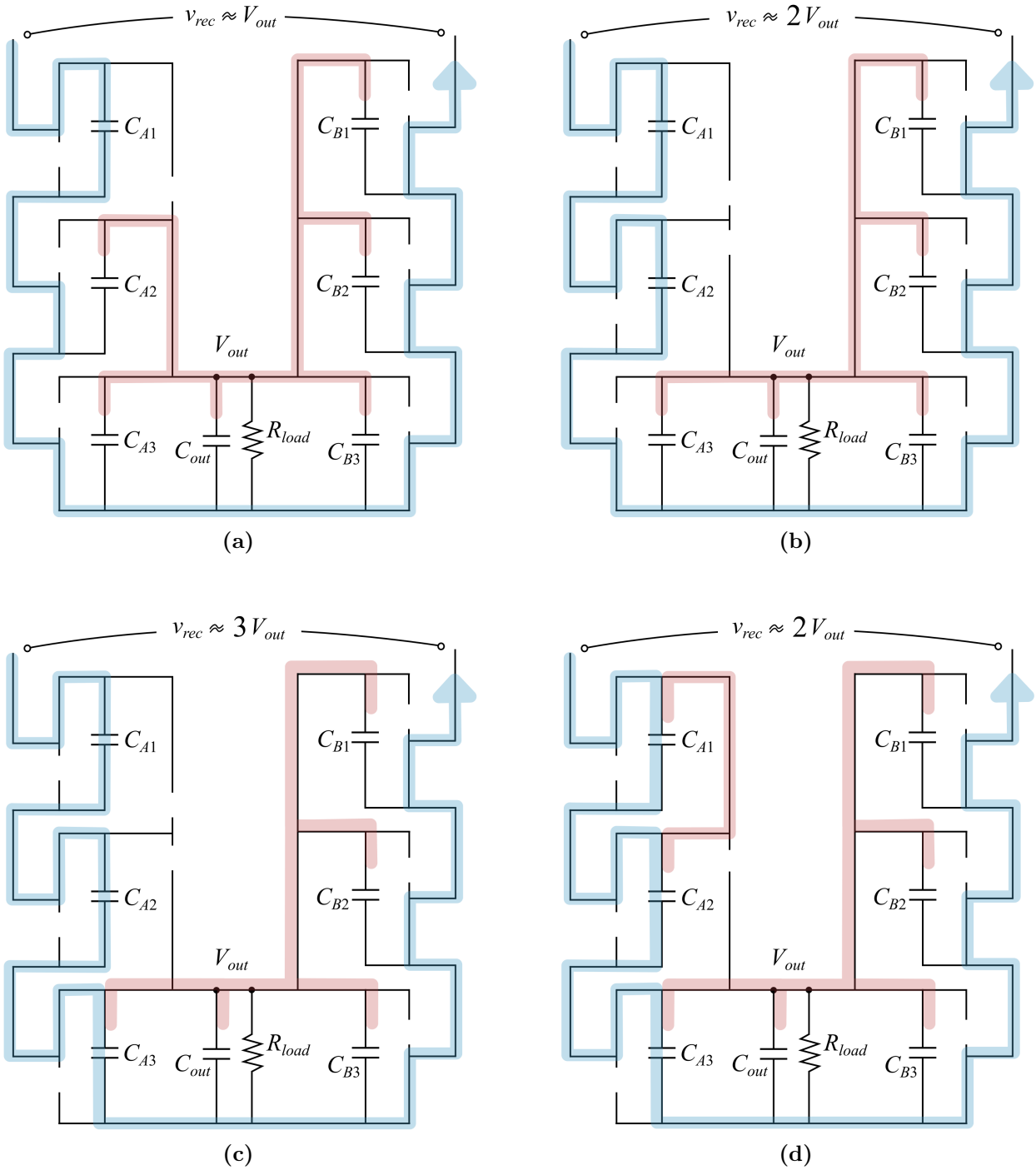


Figure 3.3: Example configurations of the 7-level switched capacitor rectifier, showing (a) $v_{rec} = 0$, (b) $v_{rec} = V_{out}$, (c) $v_{rec} = 2V_{out}$, and (d) $v_{rec} = 3V_{out}$.

Fig. 3.3 provides examples of other configurations the 7-level switched capacitor rectifier is capable of producing. Fig. 3.3b shows capacitors [C_{A2}, ... C_{B3}, C_{out}] balancing, and capacitor C_{A1} inserted into the path of the secondary current. Here, the voltage at the input of the rectifier is $v_{rec} \approx V_{out}$ because the voltage on each capacitor is $\approx V_{out}$. Figs. 3.3b and 3.3c give examples of how v_{rec} might be $\approx 2V_{out}$ or $\approx 3V_{out}$, respectively. First, C_{A2} is removed from the balancing chain and inserted into the path of i_{rec} in Fig. 3.3b. Then, C_{A3} is inserted into the path of i_{rec}, but it is kept in parallel with *phase leg B* (capacitors C_{B1}, C_{B2}, and C_{B3}) in Fig. 3.3c. Finally, Fig. 3.3d illustrates the versatility of the proposed rectifier. Similar to Fig. 3.3b, the rectifier input voltage is $v_{rec} \approx 2V_{out}$, but C_{A1} and C_{A2} are in parallel and consequently increasing v_{rec} by only V_{out}. In this case, i_{rec} is split between C_{A1} and C_{A2}. This type of functionality has ramifications in real systems when considering parasitics and loss mechanisms.

The examples in Fig. 3.3 illustrate the potential of the proposed design, but these examples are only a small portion of the possible operating conditions. The 7-level switched capacitor rectifier is a very versatile system, giving the designer substantial control freedoms to wield. Figs. 3.3a through 3.3c show the most obvious approaches to inserting capacitors into the primary conduction path in order to achieve $V_{rec} = \{0, 1, 2, 3\} \cdot V_{out}$. Fig. 3.3d shows an alternative way to implement the state $V_{rec} \approx 2V_{out}$ V, demonstrating that the rectifier is capable of a diverse set of node re-combinations to manipulate its input impedance. This control versatility is advantageous for finding more efficient implementations of the same fundamental operating point.

The basic modulation implementation shown by Figs. 3.3a through 3.3c is re-illustrated by Fig. 3.4. Here, i_{rec} is shown by an approximated sinusoidal source, and only the *phase leg A* capacitors are included. The remainder of the capacitors (*phase leg B*) are assumed to be in parallel with C_{out}. This visualization makes it easier to see how a capacitor is inserted into and removed from the conduction path of the secondary current. The four basic subintervals in Fig. 3.4 can be labeled as subintervals 1 through 4. With this notation, the subintervals coincide with the half-period graphic in Fig. 3.5.

Fig. 3.5 shows a basic stack switching scheme for the 7-level switched capacitor rectifier. The "stack" name refers to the last-in first-out (LIFO) strategy for flying capacitor insertion into the modulation scheme. In Fig. 3.5, C_{A1} is inserted at t_{02}, remains in conduction path for the entire time S_{A1H} is on, and is removed from the conduction path at t_{06}. During this time, both C_{A2} and C_{A3} are inserted into the conduction path and removed from the conduction path according to LIFO scheduling. Variable T_s is the fundamental period: $T_s = 1/150$ kHz.

This discussion highlights the most straight-forward modulation approach to controlling the 7-level switched capacitor rectifier. There are many alternative techniques to achieve the same modulations, and an example of an alternative way to achieve $V_{rec} \approx 2V_{out}$ is given in Fig. 3.3d. In general, C_{A1}, C_{A2}, and C_{A3} can be inserted into the power path anytime during the appropriate half-period. The longer each capacitor is inserted, the greater the voltage ripple (and consequent loss) on that capacitor. Adding additional switching actions enables simultaneous insertion of one capacitor and removal of another, wherein v_{rec} is unaffected. These control options describe different ways to ascertain a staircase waveform, but even more control options exist within the context of changing that staircase waveform. These

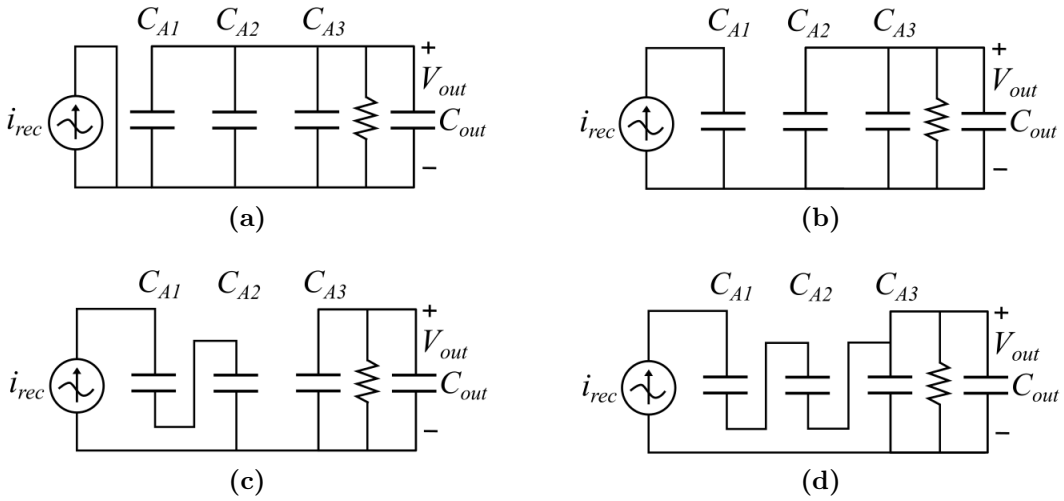


Figure 3.4: Example configurations of the 7-level switched capacitor rectifier, showing (a) $v_{rec} \approx V_{out}$, (b) $v_{rec} \approx 2V_{out}$, (c) $v_{rec} \approx 3V_{out}$, and (d) $v_{rec} \approx 2V_{out}$.

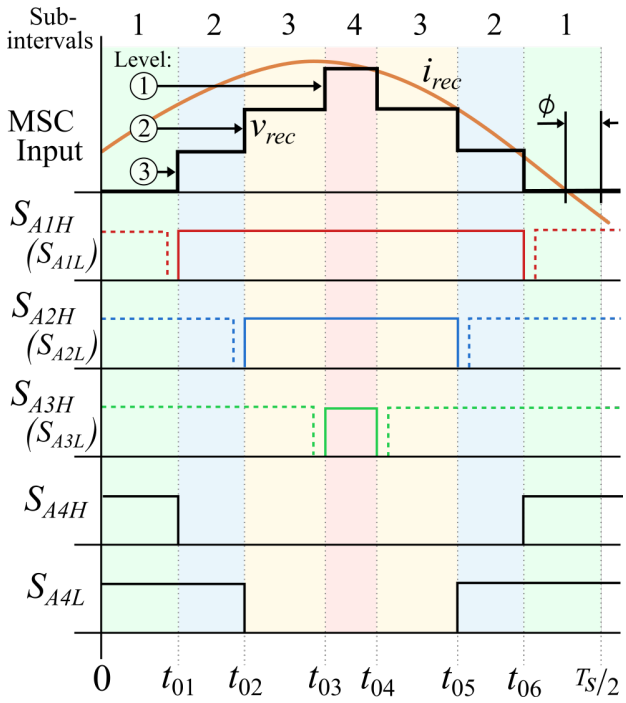


Figure 3.5: Basic stack control signal sequence for 7-level SC rectifier in one half-period. For each gate signal : Solid line: high side switches and charge sharing switches (S_{A1H}, S_{A2H}, S_{A3H}, S_{A4H}, S_{A4L}); dashed line: low side switches (S_{A1L}, S_{A2L}, S_{A3L}).

design options are explored in later sections. Next, the fundamental loss mechanisms of the WPT system are outlined to expand this baseline understanding.

3.2 Rectifier Loss Mechanisms

This section analyzes several major loss mechanisms of the proposed MSC AC-DC rectifier to better understand efficiency trade-offs when designing the system. The following loss analysis is based on the control sequence shown in Fig. 3.5 and assumes all switching devices are identical. In this section, the secondary current is assumed sinusoidal for the simplicity of this analysis. Here, the goal is to describe the dominant loss mechanisms and build intuition useful for understanding the more complex models to follow. Previous work in [12, 107] influences these derivations.

3.2.1 Conduction Loss

The conduction loss consists of two parts: the conduction loss due to the R_{dson} of the switching devices in a current path and the conduction loss induced by the flying capacitor ESRs. The total conduction loss is

$$P_{cond} = 6 \cdot I_{rms,1}^2 \cdot R_{dson} + P_{ESR,C} \tag{3.1}$$

where $I_{rms,1}$ is the RMS value of the input current i_{rec}, and $P_{ESR,C}$ is the conduction loss of the flying capacitors. There are 6 switches in the conduction path at any time irrespective of

which capacitors are inserted, so the I^2R equation is applied to each of these switch ESRs. Loss $P_{ESR,C}$ is

$$P_{ESR,C} = \sum_{x=1,2,3} I_{seg-rms,1}(x)^2 \cdot R_{ESR,C} \tag{3.2}$$

where the function $I_{seg-rms,1}$ describes the RMS value of the *segment* of i_{rec} seen by the capacitor in level $x = \{1, 2, 3\}$ and $R_{ESR,C}$ is the series resistance of each flying capacitor. The levels are defined in Fig. 3.5. This RMS value is

$$I_{seg-rms,1}(x) = f_s \, |i_{rec}|^2 \, \cdot \left((t_{0[7-x]} - t_{0x}) + \frac{\sin(2(wt_{0x} - \phi_{rec})) - \sin(2(wt_{0[7-x]} - \phi_{rec}))}{2w} \right) \tag{3.3}$$

where the $(t_{0[7-x]} - t_{0x})$ is the 'ON' time of level x as shown in Fig. 3.5 and f_s is the switching frequency. $Z_{rec,1}$ is the fundamental component of Z_{rec}, and ϕ_{rec} is the phase of the fundamental rectifier input impedance ($\phi_{rec} = \angle Z_{rec,1}$).

Low-side devices conduct larger RMS current due to longer conduction times than their high-side counterparts. Thus, there is potential to reduce the P_{cond} by asymmetrically sizing the switching devices. Additional conduction losses occur during switching dead times, caused by anti-parallel diodes of silicon MOSFETs. This diode conduction loss is minimal when the dead time is set small relative to the switching interval durations, and the losses are adequately accounted for by treating all switching waveforms as though they are linear during the short dead time.

3.2.2 Switching Loss

Gate charge loss is a product of the switching actions, but it generally manifest in the control circuit and doesn't contribute to power stage loss. That is why gate charge loss,

$$P_{gs} = 16\, V_{gs}\, Q_{gs}\, f_s, \tag{3.4}$$

often is not included in the power stage loss model. Here, V_{gs} is the gate-to-source voltage and Q_{gs} is the gate-to-source charge, available from the device datasheet.

The power stage switching loss is modeled by linearizing the dead time circuit interactions at each level change. Each rectifier level change sees one switch toggled 'ON', one toggled 'OFF', and occurs at some value of $i_{rec}(t)$. This value of current, called I_{lcn}, is assumed constant through the entire duration of the relatively short dead time. The dead time is the interval wherein the first switch has been turned 'OFF' but the second has yet to be turned 'ON'. First, given the C_{oss} of each switching device, the dead time duration (t_d), and the voltage being traversed (V_{out}), the required current to achieve ZVS is calculated by

$$I_{req} = C_{oss}\ \frac{V_{out}}{t_d}. \tag{3.5}$$

Then, the current at the instant of the level change for switching action n (I_{lcn}) is evaluated for one of four cases. The cases for a positive level change are: $I_{lcn} < 0$, $I_{lcn} < I_{req}$, $I_{lcn} = I_{req}$, or $I_{lcn} > I_{req}$. Fig. 3.6a outlines the potential cases of the positive linearized dead time, and Fig. 3.6b outlines the complimentary cases for a negative level change. For the positive

level change, if the current is the wrong polarity, then case 1 shows the diode conduction throughout the dead time. A small positive current in case 2 reduces switching loss, but still results in some hard switching. Case 3 is perfect ZVS, and case 4 is diode conduction at the positive rail. Table 3.1 summarizes the loss mechanisms associated with each case for both types of level change.

The following losses are calculated for a single level change, so the total loss must include a consideration of how many of each loss mechanism occurs by cross-referencing the operating point with Table 3.1. Turn on loss is a function of the turn on time, t_{on}, and the voltage blocked by the switch, $V_{on,n}$,

$$P_{ton,n} = \frac{1}{2} |I_{lcn}| V_{on,n} t_{on} f_s, \tag{3.6}$$

which is applied to the nth high or low side switch according to Table 3.1. Similarly, turn off loss is given by

$$P_{toff,n} = \frac{1}{2} |I_{lcn}| V_{out} t_{off} f_s, \tag{3.7}$$

where t_{off} is the turn off time of the switch. Equation (3.6) assumes that the power current/output capacitance relationship dominates the gate driver current/gate-to-drain capacitance relationship: $I_{ds}/C_{oss} \gg I_g/C_{gd}$. Diode conduction is

$$P_{Dcond,n} = V_d |I_{lcn}| t_{dc,n} f_s, \tag{3.8}$$

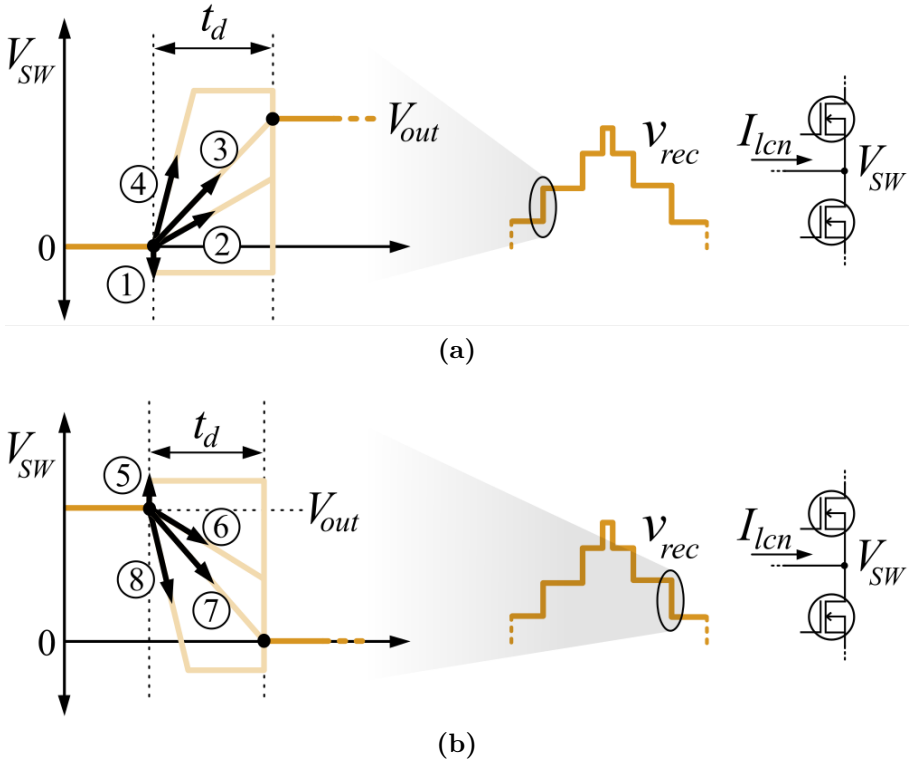


Figure 3.6: Linearized dead time for (a) positive level changes and (b) negative level changes showing the potential V_{sw} translation cases dependent on I_{lcn}.

Table 3.1: Losses Contributed by Low (LS) and High Side (HS) Switches Based on Fig. 3.6

Case	Loss Mechanism			
	Turn ON	Turn OFF	Diode Cond.	C_{oss}
1: $I_{lcn} < 0$	HS	LS	LS	HS
2: $I_{lcn} < I_{req}$	HS	LS	—	HS
3: $I_{lcn} = I_{req}$	—	LS	—	—
4: $I_{lcn} > I_{req}$	—	LS	HS	—
5: $I_{lcn} < 0$	LS	HS	HS	LS
6: $I_{lcn} < I_{req}$	LS	HS	—	LS
7: $I_{lcn} = I_{req}$	—	HS	—	—
8: $I_{lcn} > I_{req}$	—	HS	LS	—

where V_d is the diode voltage drop and $t_{dc,n}$ is the duration of diode conduction within the dead time. Finally, output capacitance (C_{oss}) loss is given by

$$P_{coss,n} = {}^1\!/_2\, C_{oss}\, V_{on,n}^2. \tag{3.9}$$

C_{oss} is a non-linear capacitance with dependence on the drain-to-source voltage. The exact energy and charge capacitor equivalents can be calculated for precision, but here it is sufficiency to approximate the value of C_{oss} from the device datasheet. Items $V_{on,n}$ and $t_{dc,n}$ are all functions of the dead time voltage transition, and they can each be calculated with the linearized dead time model and constant current, I_{lcn}. Voltage $V_{on,n}$ is calculated with

$$V_{on,n} = V_{out}\, \frac{I_{req} - I_{lcn}}{I_{req}}, \tag{3.10}$$

and the diode conduction time is calculated with

$$t_{dc,n} = t_d\, \frac{I_{lcn} - I_{req}}{I_{lcn}} \tag{3.11}$$

for cases 4 and 8 but is assumed equal to t_d for cases 1 and 5.

The constant dead-time current assumption works because the dead time is short and enables simple calculations for each of the loss mechanisms in (3.6) through (3.9). Given rectifier phase ϕ_{rec}, level change times, and current magnitude I_{rec}, the loss for each level change is calculated using and Table 3.1.

3.2.3 Charge Sharing Loss

In the MSC converter, each of the flying capacitors C_{xx} is charged by the i_{rec} during the portion of the line period where C_{xx} is inserted into the power path, resulting in a small increase in capacitor voltage Δv_{xx}. Three approximations are applied to the model: the output capacitance is large ($C_{xx} \ll C_{out}$), the ripple on each flying capacitor is $\Delta v_{xx} \ll V_{out}$, and the voltage balancing time constants are less than 1/2 the period ($\tau_{RC} < T_s/2$). Whenever one of the charge sharing switches S_{x4x} turns on, the respective flying capacitor is connected in parallel with the output capacitance C_{out}. This causes a pulsed current (time constant τ_{RC}) which equalizes the capacitor voltages through a resistive path, resulting in charging sharing loss [19]. Charge sharing loss is modeled using the generalized equivalent charge sharing circuit of Fig. 3.7.

In Fig. 3.7, if $\Delta v_{xx} = 0$, no loss occurs when the switch closes. However, if a small voltage difference is present ($\Delta v_{xx} \neq 0$), then the total charge between the two capacitors re-distributes as the two capacitor voltages equalize after the switching action. Assuming incremental voltage Δv_{xx} on flying capacitor C_{xx}, and $C_{out} \gg C_{xx}$ such that V_{out} is constant, then the charge sharing loss is

$$P_{cs,n} = {}^1\!/_2 \, C_{xx} \, \Delta v_{xx}^2 \, f_s. \tag{3.12}$$

From (3.12), the charge sharing loss, which can be significant in hard-charging SC converters, is proportional to the switching frequency, capacitance, and voltage ripple on the flying capacitors. There are six balancing actions per period, one for each flying capacitor.

Therefore, (3.12) is multiplied by 4 for the total charge sharing loss in the circuit. The voltage ripple additionally depends on the operating point and control strategy of the MSC rectifier, so the charge sharing loss is affected by both the rectifier's input phase and modulation times. An overview of the loss mechanisms and the main assumptions associated with each is listed in Table 3.2.

3.3 Stack vs. Queue Modulation

Stack modulation is previously used in Fig. 3.5 to describe the base-level operation of the 7-level switched capacitor rectifier. This section presents a second basic modulation scheme called queue modulation and characterizes the differences between the two. There are many more ways to modulate the MSC rectifier other than the stack and queue strategies, but these are a good starting point for understanding the important considerations when designing the MSC converter.

In stack charge control, the flying capacitors are charged in a stacked flow, i.e. a LIFO sequence, as demonstrated in Fig. 3.8a. The top flying capacitor (C_{A1}) inserts first and switches out last, while the bottom one (C_{3A}) inserts last, but switches out first. Since the voltage ripple on each flying capacitor is proportional to the charge sharing loss, the voltage ripples are calculated as follows.

Using stack modulation as an example, C_{1A} has total input charge $q1$ during the positive-current half-period of

$$q_1 = \int_{t_{01}}^{t_{06}} I_{rec} \sin(\omega_s t + \phi_{rec}) dt, \tag{3.13}$$

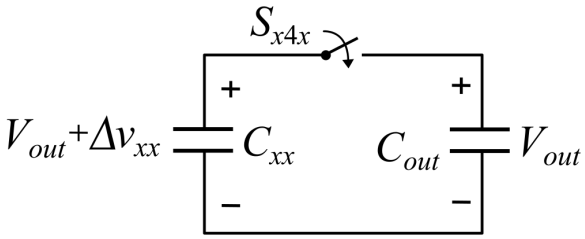


Figure 3.7: Charge sharing loss equivalent circuits in MSC rectifier: capacitor to capacitor.

Table 3.2: Summary of Fundamental Rectifier Loss Mechanisms

Loss	Equation	Noteworthy Assumptions
Switch Conduction	$P_{sw} = 6 \cdot I_{rms,1}^2 \cdot R_{dson}$	i_{rec} is sinusoidal, ignores PCB ESR
Flying Capacitor Conduction	$P_{ESR,C} = \sum_{x=1,2,3} I_{seg-rms,1}(x)^2 \cdot R_{ESR,C}$	i_{rec} is sinusoidal, ignores PCB ESR
Gate Charge Loss	$P_{gs} = 16 \cdot V_{gs} \cdot Q_{gs} \cdot f_s$	—
Charge Sharing Loss	$P_{cs,n} = 3 \cdot C_{xx} \cdot \Delta v_{xx}^2 \cdot f_s$	All switches balance with $C_{out} \gg C_{xx}$
Dead Time Loss	$P_{ton,n}$, $P_{toff,n}$, $P_{Dcond,n}$, $P_{coss,n}$	Short, linearized dead time

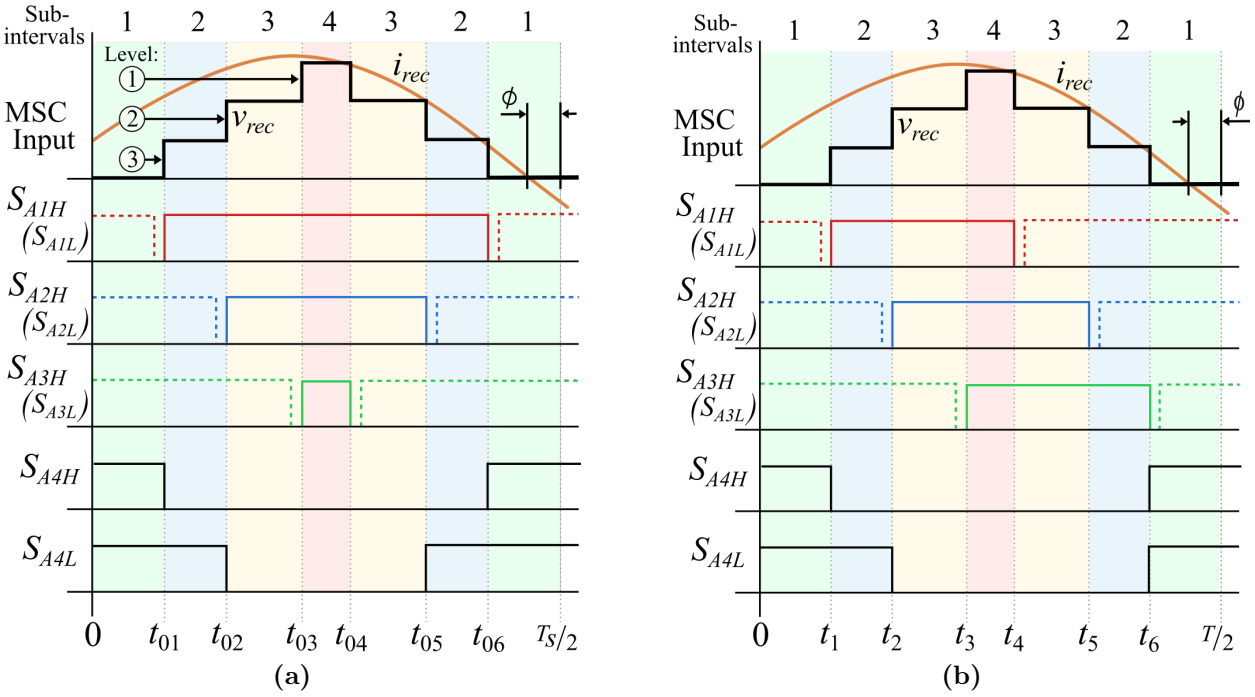


Figure 3.8: Two basic control strategies: (a) LIFO, stack modulation and (b) FIFO, queue modulation.

where ω_s is the fundamental frequency in radians. The consequent voltage ripple on C_{1A} is

$$\Delta V_{C1A} = \frac{q_1}{C_{1A}}. \tag{3.14}$$

Similarly, the voltage ripple on C_{2A} is

$$\Delta V_{C2A} = \frac{\int_{t_{02}}^{t_{05}} I_{in} \sin(\omega_s t + \phi_{rec}) dt}{C_{2A}}. \tag{3.15}$$

For the bottom module, C_{3A} is always clamped to the output capacitor, and the voltage ripple on it has two parts. First, positive charge is added when C_{3A} is charged by the input current. Second, C_{3A} is continually discharged by the load resistance. Therefore, the voltage ripple of C_{3A} is

$$\begin{aligned} \Delta V_{C3A} = \Delta V_{C3A+} + \Delta V_{C3A-} = \\ \frac{\int_{t_{03}}^{t_{04}} I_{in} \sin(\omega_s t + \phi_{rec}) dt}{C_{eq} + C_{out}} - V_{out} \left(e^{\left(\frac{Ts/2}{R_{load}(C_{eq}+C_{out})} \right)} - 1 \right). \end{aligned} \tag{3.16}$$

Here, C_{eq} is the equivalent capacitance at C_{A3}, without including the large output capacitor: $C_{eq} = C_{A3} + C_{B3}$. In reality, C_{out} could be grouped into C_{eq} as well, but it is separated under the assumption that all flying capacitors balance with a large C_{out} such that: $C_{xx} \ll C_{out}$.

Equations (3.13) through (3.16) are also derived for the queue modulation scheme shown in Fig. 3.8b. In contrast to stack control, queue modulation uses the first-in first-out strategy (FIFO) for inserting and removing capacitors into the conduction path. The charge into C_{A1}

during one half period is deposited from t_{01} to t_{04} in this case. Similarly, C_{A2} is active from t_{02} to t_{05}, and C_{A3} is calculated from t_{03} to t_{06}. Charge sharing switch S_{A4L} is turned on later to avoid shorting out C_{A2}.

Note the presence of rectifier input phase, ϕ_{rec}, in equations (3.13) through (3.16). Because Δv_{xx} is a function of total charge during the half period, varying rectifier input phase affects the charge sharing loss in each capacitor. When ϕ_{rec} is changed, the portion of i_{rec} conducted by each flying capacitor also changes, thereby influencing the voltage ripple on that capacitor. This helps to make one modulation scheme more useful than another, as one modulation scheme might be less lossy given the operating parameters.

An example design and operating point are outlined in Table 3.3, and the consequent capacitor ripples and charge sharing losses are also calculated in Table 3.3. For this example, all flying capacitors are equivalent, the output voltage is $V_{out} = 5$ V, and the output power is $P_{out} \approx 20$ W. The approximation that $C_{xx} \ll C_{out}$ is satisfied by $C_{xx} = 10\mu$ F and $C_{out} = 50\mu$ F in this example.

Table 3.3 shows that the stack modulation scheme is less efficient at the example operating point. For both stack and queue switching, the voltage ripple and consequent loss on C_{A2} does not change. This is because in either case the capacitor is inserted into the conduction path from t_{02} to t_{05}. Without changing the time of insertion, one would not expect a change in ripple or loss. The majority of the efficiency change occurs at C_{A1} because it conducts for a much smaller time with queue modulation. The loss at C_{A3} is less affected because it is in parallel with other large capacitors C_{B3} and C_{out}, resulting in less ripple.

Table 3.3: Stack vs. Queue Example Comparison

Operating Point	C_{xx}	C_{out}	ϕ_{rec}	f_s
	10μF	50μF	0°	150 kHz
	R_{load}	V_{out}	P_{out}	$\lvert i_{rec}\rvert$
	1.25 mΩ	5 V	20 W	2.5 A

t_{01}	t_{02}	t_{03}	t_{04}	t_{05}	t_{06}
1.8%	5.6%	9.8%	40.2%	44.4%	48.2%

Calculations

	Ripple [mV]		Loss [mW]	
	Stack	Queue	Stack	Queue
C_{A1}	433	480	141	173
C_{A2}	498	498	186	186
C_{A3}	-119	-126	21	24
			348	383

* Modulation times are reported as a percentage of the total period.

Note that the rectifier has an input phase of $\phi_{rec} = 0°$ in the example. While stack modulation is more efficient at this point, queue modulation is more efficient at other points. The same calculations shown in Table 3.3 are repeated in Fig. 3.9, but the rectifier input phase (ϕ_{rec}) is swept. The figure shows the total half-period loss of each modulation approach at each phase.

Above $\approx -40°$ queue modulation is the better choice. Elsewhere, stack modulation demonstrates lower loss. The plot of 'Stack 2' in Fig. 3.9 shows the same stack modulation scheme, but levels 1 and 3 are used in reverse, exposing C_{A1} to i_{rec} for a longer duration. The example in Fig. 3.9 illustrates some of the factors that influence modulation design, but it does not present an optimal approach. A more thorough exploration of optimal modulation schemes would include the affects of changing both $|i_{rec}|$ and modulation index (times t_{01} through t_{06}). The investigation may include the harmonics of i_{rec}, or the effect of additional switching actions for a given modulation index.

3.4 Impedance Control

Much of the conversation surrounding wireless power systems is phrased in terms of impedance matching, optimal loading, and coil tuning [63]. Looking at the system from an impedance perspective provides insight into how a designer can most efficiently push power through the system. The 7-level switched capacitor rectifier provides exceptional advantages to a WPT system by means of its actively controlled switching actions, i.e. real-time tunable impedance.

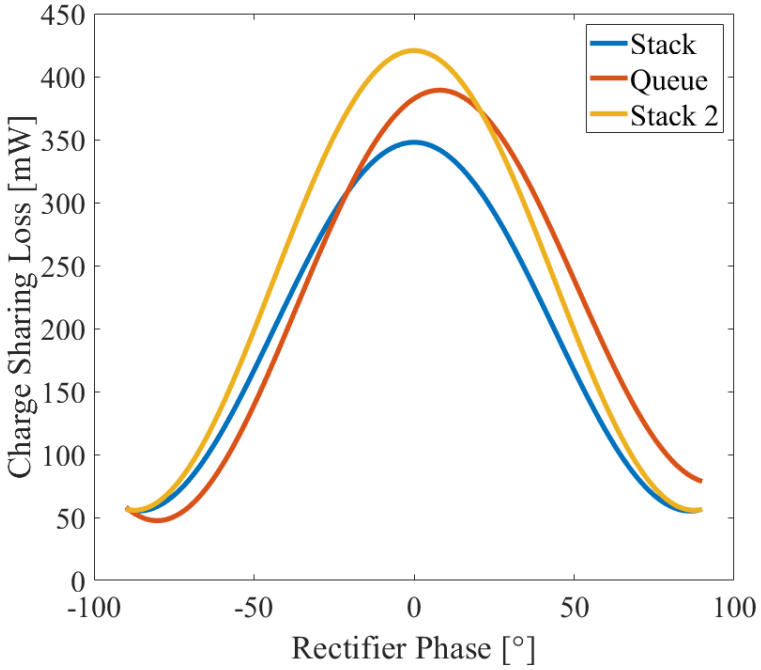


Figure 3.9: Half-cycle charge sharing loss as a function of rectifier phase for the stack and queue modulation strategies. 'Stack 2' results in the same waveform shape, but level 1 is on for the longest duration ($t_{01} - t_{06}$) with level 3 on for the shortest duration ($t_{03} - t_{04}$).

First, the MSC is able to change its modulation index by varying the 'ON' time of each level. The set of potential modulation indices is defined by digitizing a sinusoid, the implication being that mimicking a sinusoidal waveform produces less harmonic distortion. A set of sinusoidal waveforms is produced with various amplitudes. The turn-on and turn-off times of each modulation level are calculated based on the $0.5V_{out}$, $1.5V_{out}$, and $2.5V_{out}$ voltages in the sinusoid. An example of this process is shown in Fig. 3.10, where t_{01} through t_{06} are defined by the voltage levels.

Given that the amplitude of the sinusoid is varied from significantly small to significantly large, the limits of the modulation index range from zero voltage at v_{rec} (no levels active) to a square wave of value $3V_{out}$ at v_{rec}. Modulation index is given a formal definition using

$$M = \frac{|v_{rec,1}|}{V_{out}} \quad [12] \tag{3.17}$$

where $v_{rec,1}$ is the fundamental component of v_{rec}. This equation has limits

$$0 \leq M \leq 3 \cdot \frac{4}{\pi} = 3.81 \tag{3.18}$$

because $v_{rec,1} = 3.81 \cdot V_{out}$ when maximum modulation is reached at the point where v_{rec} is a $3V_{out}$ square wave. The modulation range is visualized in Fig. 3.11.

From a tuning perspective, the rectifier's ability to change M is important because affects the rectifier's input impedance. Using a fundamental model and assuming the rectifier's input phase is $\phi_{rec} = 0$, the input impedance of the rectifier is a function of both the load and

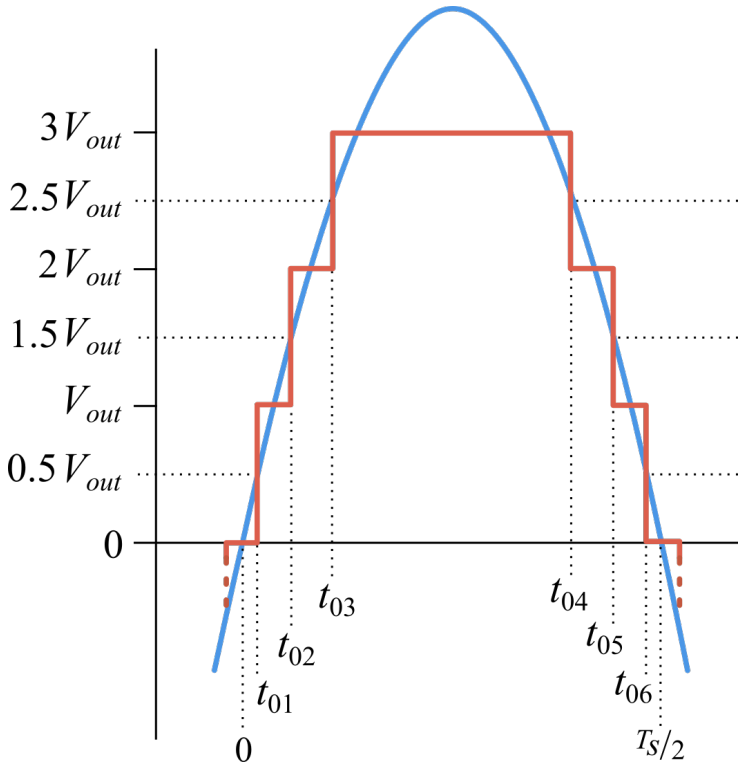


Figure 3.10: Example modulation index derivation.

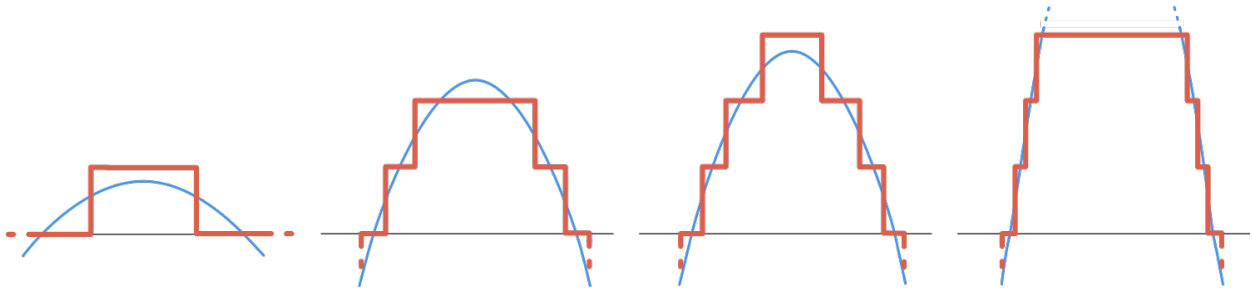


Figure 3.11: Illustration of the modulation index range and the underlying sinusoid used to generate each modulation index.

modulation index:

$$Z_{rec,1} = |Z_{rec,1}| = \frac{M^2}{2} R_{load}. \quad [12] \tag{3.19}$$

Take $R_{load} = 2.5\Omega$ for example. With the MSC's ability to change modulation index, $Z_{rec,1}$ is capable of ranging anywhere from 0Ω to 18.15Ω. This MSC characteristic exhibits a controllable conversion ratio similar to a DC-DC converter following a traditional diode rectifier. The magnitude of $Z_{rec,1}$ is controlled by the duty cycle of the DC-DC, but here it is controlled by the modulation index, M. Furthermore, many DC-DC converters can only regulate in one direction. A buck, for example, can only make the input impedance appear larger than its load, and a boost is limited to only reducing impedance. The MSC is able to do both by leveraging the full range of its modulation: an R_{load} value of 2.5 Ω enables equivalent rectifier inputs ranging from 0 Ω to 18.15 Ω.

One benefit of this modulation is the reduction of WPT tank conduction losses. The rectifier's impedance via modulation index can also be looked at in terms of voltage step-down. The largest voltage a diode rectifier can ever present at its input is V_{out}. In contrast, the MSC can present up to $3V_{out}$. This means that, for the same output power, i_{rec} can be reduced with the MSC. The step-down functionality of the MSC allows the rectifier to reduce WPT coil loss by presenting a higher input impedance to the primary side through the tank. The same power is transmitted through the tank, but conduction loss is reduced as current is smaller and voltage is higher. Tank current reduction is another way of stating that the MSC can retune the system for optimal efficiency as discussed in Sections 1.2 and 2.5.

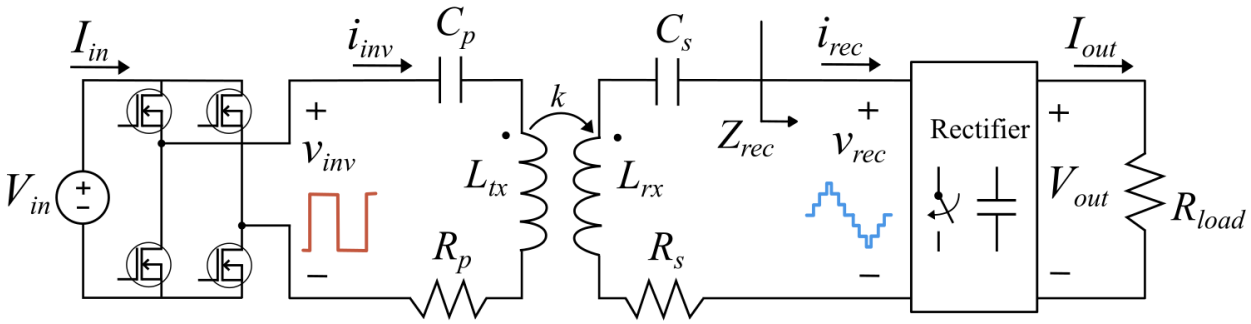


Figure 3.12: WPT system showing the rectifier input impedance, Z_{rec}.

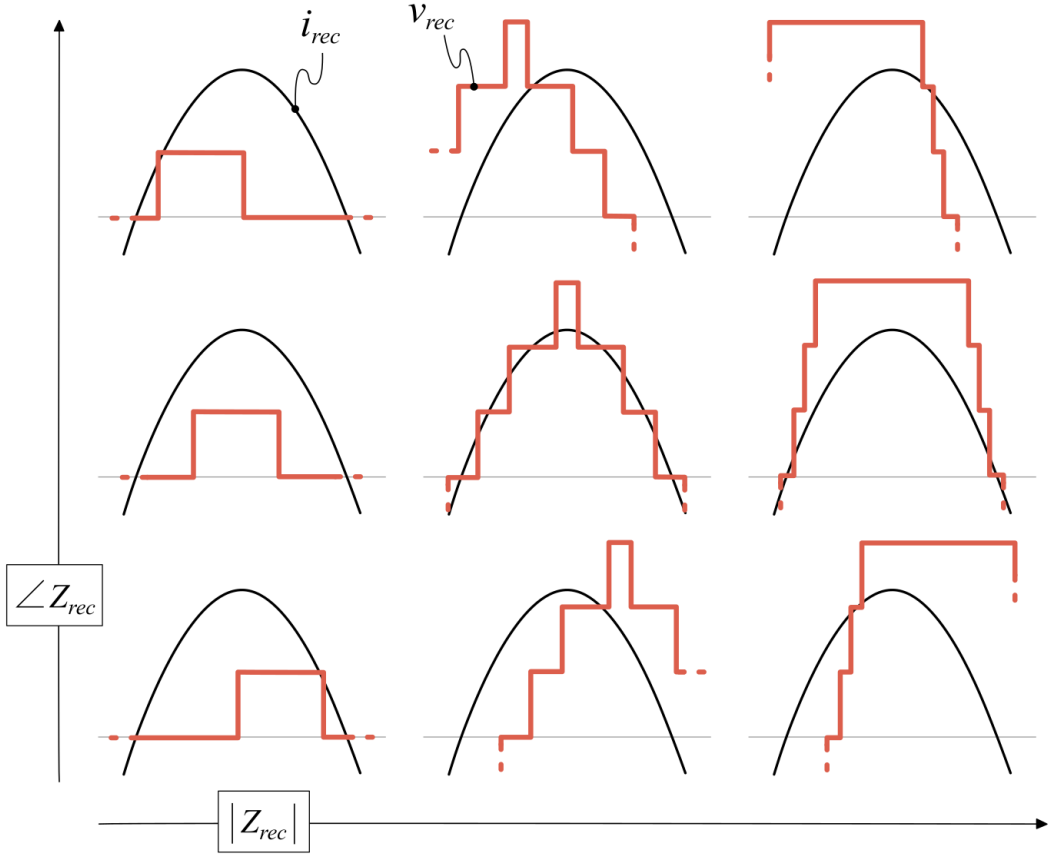


Figure 3.13: Example rectifier input impedances. Z_{rec} *magnitude* increases left to right with modulation index, and Z_{rec} *phase angle* increases top to bottom with switching time.

In reality, the input phase of the rectifier will likely be non-zero at some operating points. In this case, the fundamental model sees (3.19) altered to include the phase dependence. $Z_{rec,1}$ is given by

$$Z_{rec,1} = \frac{M^2}{2} R_{load} \cdot \cos(\phi_{rec}) e^{j\phi_{rec}}. \tag{3.20}$$

Where a passive rectifier is incapable of varying its input phase, an active rectifier has full control of its switching times. This means that an active system chooses when to switch during the period, thereby influencing the phase relationship between the rectifier's input voltage and current. As an example, i_{rec} is again assumed to be sinusoidal and fixed-phase. Fig 3.13 gives examples of how both the modulation and switching phase are leveraged to influence the waveforms at the input of the rectifier. Delaying the switching actions leads to a more capacitive phase, while advancing the switching actions leads to a more inductive phase. Fundamentally, the rectifier has control over the magnitude of its equivalent input impedance ($|Z_{rec}|$) via the modulation index, and it has control over the angle of its equivalent input impedance ($\angle Z_{rec}$) via the switching time within the period.

In summation, the 7-level switched capacitor rectifier is capable of changing its modulation index and its switching phase. The modulation index of the rectifier increases or decreases the magnitude of Z_{rec} according to the direction of change and has a range of $0 \leq |Z_{rec,1}| \leq 3.81^2 R_{load}/2$, given that $\angle Z_{rec,1} = 0$. Of course, $Z_{rec,1}$ is often not zero, and in this case the rectifier's input impedance is a function of M, R_{load}, and ϕ_{rec}. By these means, the MSC is capable of presenting a full range of complex impedances. This allows the MSC to tune its equivalent input impedance to better meet the efficiency needs of the rest of the

system. Namely, this involves lowering WPT tank current by increasing $|Z_{rec}|$ and tuning $\angle Z_{rec}$ to compensate for coil misalignment.

3.5 Switching Limits

The loss mechanisms and modulation schemes discussed for the 7-level switched capacitor architecture are constructed under certain assumptions. Switching speed and capacitor sizes cannot be arbitrarily assigned for the model assumptions to remain valid. Switched capacitor converters have slow and fast switching limits that must be considered alongside capacitance size [19, 108].

Modeling a switched capacitor converter (SCC) as an ideal voltage conversion with an output impedance shows that the equivalent output resistance is a function of frequency [19]. The work in [19] models a DC-DC switched capacitor converter as shown in Fig. 3.14a. The output resistance R_o is a power sync that contributes loss, and R_{load} is the converter load. The theoretical value of output resistance is

$$R_{th} = m \frac{1}{C f_s} \quad [19], \tag{3.21}$$

where m is a constant and a function of the specific converter under study. Efficiency increases as R_{th} decreases, and therefore an increase in the switching frequency, f_s, results in a higher converter efficiency. However, there is an upper limit to switching frequency in terms of diminishing return [19, 108]. As switching frequency increases, the benefits of

decreasing capacitor ripple are diminished, and circuit parasitics become more relevant. A limit is set by the circuit parasitics at higher switching frequencies. For instance, the MSC topology warrants that the power current conducts through $6R_{dson}$ for any operating point. Irrespective of the switching frequency, the system is always subject to the conduction losses associated with (3.1) and (3.3). These two limits are the slow switching limit (SSL) and the fast switching limit (FSL) as outlined in Fig. 3.14.

Fig. 3.14 shows how R_o changes as a function of frequency and shows where SSL and FSL manifest. For the generalized example in Fig. 3.14, the capacitor size and parasitic values are kept constant. In the low frequency SSL region, the combination of capacitor size and switching speed means the capacitors drain their charge before the next period. The time constants associated with the capacitors in the circuit are faster than the fundamental period, and the circuit is inefficient as a result of the $1/2CV^2$ losses associated with the large ripple on each capacitor. To rectify this issue, the capacitor size is increased or the switching frequency is increased.

The FSL region of Fig. 3.14 is where the combination of capacitor size and switching frequency prevents the capacitor voltages from significantly deviating from the nominal DC value. The ripple on each capacitor becomes smaller, and the loss caused by charging and draining each capacitor is drastically reduced. The fast switching limit sets the value of R_o as a function of R_{par}, a level that represents the parasitic resistance in the circuit. This includes device ESR, PCB layout, solder, etc. FSL is a function of the unavoidable conduction loss in the circuit, and it prevents R_o from becoming infinitely small and the circuit from becoming 100% efficient.

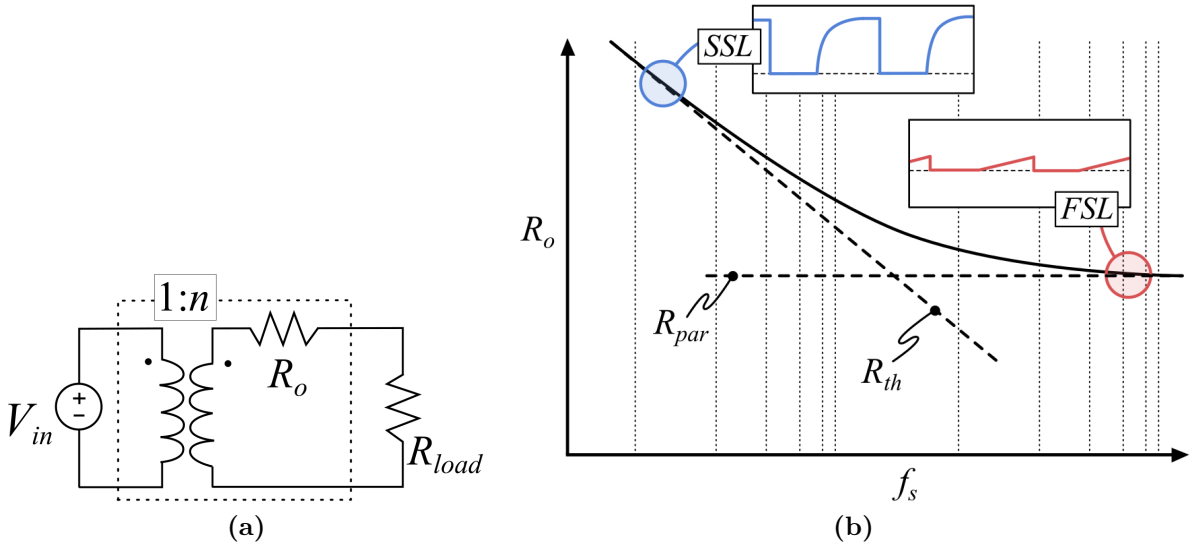


Figure 3.14: The (a) idealized switched capacitor converter model and the (b) frequency dependence of R_o showing the fast and slow switching limits. Both figures are adapted from [19].

Because the 7-level switched capacitor topology is a rectifier, the voltage ripple manifests in the opposite direction of what Fig. 3.14b illustrates. Each capacitor is charged during its insertion into the path of i_{rec} and is discharged when placed in parallel with the output. In either case, the R_{th} and R_{par} levels still apply, but they manifest slightly differently for the MSC. The switching frequency of the MSC is set by the WPT carrier, meaning that the design variable is capacitor size. Too little capacitance and the system will incur significant charge sharing loss due to large voltage ripple, so the capacitance must be large. However, to realize both charge redistribution and power flow to the output, the MSC rectifier must operate in the SSL region: the capacitors completely balance with V_{out} each 1/2 cycle. Therefore, larger capacitors increase efficiency by pushing the system into the FSL region, but an upper limit to capacitance size exists to ensure that the capacitor voltages redistribute each cycle.

To calculate this upper limit, the worst case charge redistribution is calculated to ensure that the system operates accordingly. The minimal allotted time for charge redistribution is one half period: $1/(150\text{ kHz}) \cdot {}^1\!/_2 = 3.33\ \mu$s. The worst cast charge redistribution time constant is calculated by $\tau_{wc} = (4R_{dson} + 2R_{ESR,C})C_{xx}$ because C_{A1} shorts to C_{out} through four switch ESRs and two parasitic capacitor ESRs. Therefore, designing the worst case to achieve greater than 95% charge redistribution warrants $3\tau_{wc}$ occur within 3.33 μs. Here, the equation $C_{xx} = 3.33\ \mu s\ /\ 3(4R_{dson} + 2R_{ESR,C})$ states that the upper limit for flying capacitance is: $C_{xx} = 33.1\ \mu$F.

Capacitance greater than 33.1 μF means that the charge sharing interval does not completely balance the flying capacitor voltages. This leads to the undesirable characteristic where the steady state flying capacitor voltage rises to some voltage nominally above V_{out}.

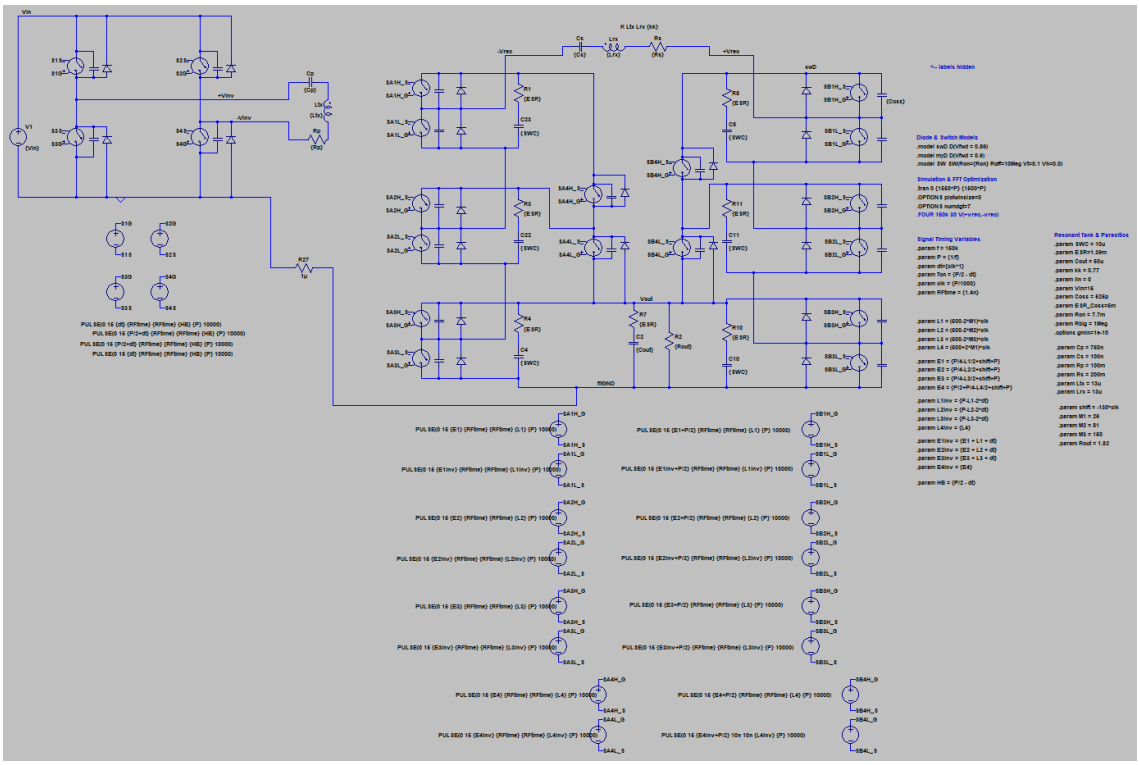
Moreover, adding capacitance pushes the system further into the FSL region. While charge sharing loss is reduced, the size of the system is increasing, lowering the power density. Furthermore, the loss savings do not scale proportionally with capacitance, leading to an area of diminishing returns in terms of efficiency verses power density for designs with very high capacitance.

3.6 Fundamental Model vs. Simulation

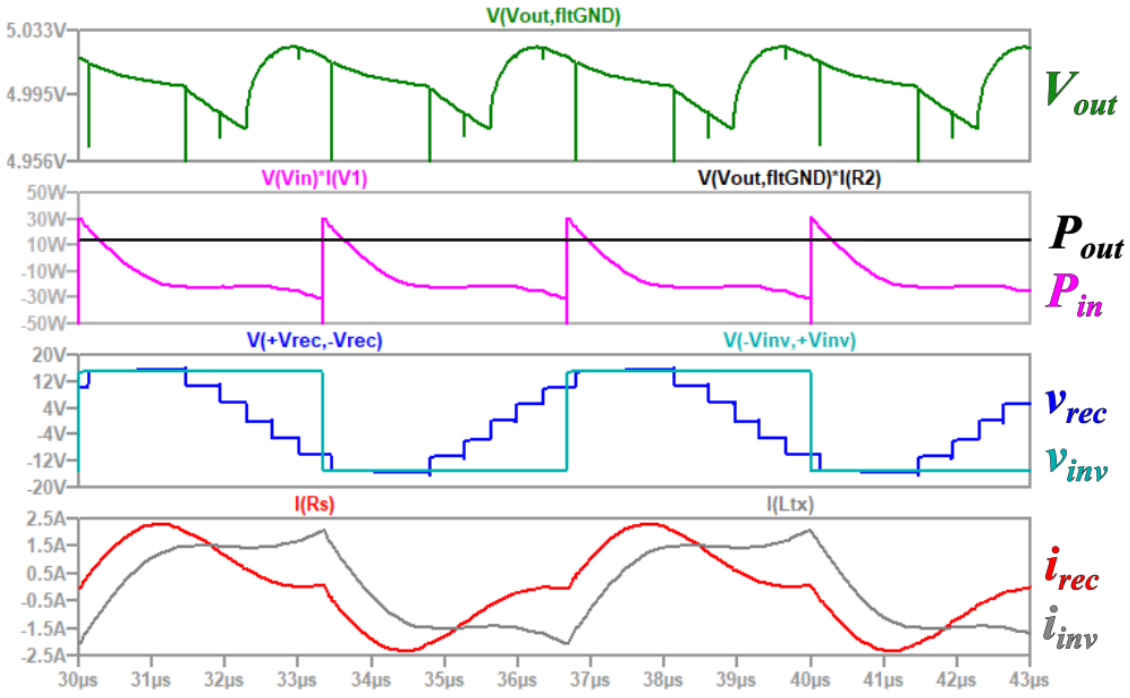
The 7-level switched capacitor model put forth in this chapter is checked against a simulation using LTspice software. The tank of either circuit is tuned according to Table 3.4. The LTspice circuit and resulting waveforms are shown in Fig. 3.15. The simulation data is pulled into MATLAB, interpolated, and evaluated. While the interpolation process does preserve the integrity of the waveforms, normalizing the time samples removes the simulated data "spikes" that, in a real system, are attenuated by parasitic components.

The LTspice simulation uses the k coupling model for the transformer, while the fundamental model used the T-network. The switches in the simulated model consist of on-state ESR, an ideal diode, and an output capacitance (with its own small ESR value). This means that turn-on and turn-off (overlap losses) are not included in the LTspice model, but diode conduction and C_{oss} loss are both included.

The calculated fundamental model is evaluated in the following manner: an operating point is chosen, and the circuit is evaluated according to the fundamental circuit. The output voltage and load are assigned, and the resulting output power and modulation index



(a)



(b)

Figure 3.15: LTspice simulation of the 7-level switched capacitor WPT system.

are extracted (modulation must adhere to $0 \leq M \leq 3.81$). Given the fundamental voltage $|v_{rec,1}|$, switching times $t_{0[1,2,3,4,5,6]}$ are calculated. The current at each switching time is used to calculate the switching loss at each instance. Finally, the output power is adjusted to include the switching losses, R_{dson} conduction losses, and capacitive ESR losses before calculating the final efficiency.

The fundamental model is initialized with $Z_{rec,1}$ and calculates the switching times thereafter. In contrast, the simulation is initialized with $t_{0[1,2,3,4,5,6]}$, and the fundamental components are calculated thereafter. The simulation is expected to give a more detailed description of the system, but its execution time is significantly longer than the model put forth in this chapter. In Table 3.4, the underlined items are those used to initialize either approach.

Table 3.4 shows good agreement with respect to the dominant fundamental components, output voltage, and modulation index. This validates the overall approach. However, the efficiencies demonstrate a mismatch of 1.3 percentage points. This comparison proves that the model is valid, but it also implies that details are missed by the calculated model. One area where the fundamental model certainly lacks resolution is that of harmonic content. Fig. 3.15b clearly shows that the simulated inverter and rectifier voltages and currents are non-sinusoidal and include distortion. This distortion affects the conduction losses of the system as well as the loss at each switching action. Fig. 3.16 shows the spectrum of i_{rec} in the LTspice simulation. The imprecision of the calculations motivates the creation of a more sophisticated model to predict the WPT system's behavior. However, there is an even larger factor motivating the creation of a more comprehensive model: establishing feedback

control requires a small signal model of the WPT system. Each of these issues is addresses in Chapter 4 where a state space model is constructed for the 7-level switched capacitor wireless power circuit.

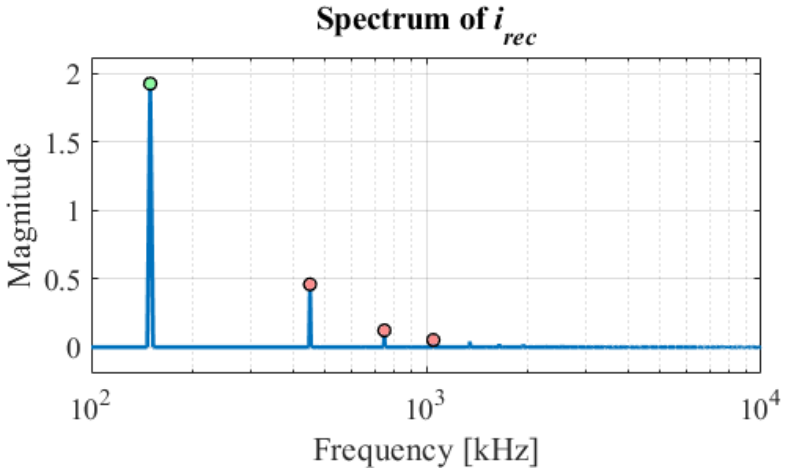


Figure 3.16: Spectrum of i_{rec} from the LTspice simulation.

Table 3.4: Fundamental Model vs. LTspice Simulation

Universal Circuit Characteristics				
L_{tx}	L_{rx}	C_p	C_s	R_p
13 μH	13 μH	750 nF	100 nF	100 mΩ
R_s	C_{xx}	C_{out}	ESR,C	V_{in}
200 mΩ	10 mF	50 mF	1.39 mΩ	15 V
C_{oss}	ESR,C_{oss}	R_{dson}	V_d	t_d
525 pF	5 mΩ	7.7 mΩ	0.86 V	T_s/1000

Results Compared		
	Fundamental	LTspice
$\lvert v_{rec,1}\rvert$	15.91 V	16.02 V
$\lvert i_{rec,1}\rvert$	1.93 A	1.92 A
$\lvert v_{inv,1}\rvert$	19.10 V	19.07 V
$\lvert i_{inv,1}\rvert$	1.88 A	1.89 A
$\lvert Z_{rec,1}\rvert$	8.23 Ω	8.32 Ω
$\angle Z_{rec,1}$	46.46°	46.05°
V_{out}	5.00 V	5.00 V
M	3.18	3.20
R_{load}	1.82 Ω	1.82 Ω
P_{in}	14.77 W	14.85 W
P_{out}	13.49 W	13.76 W
η	91.36 %	92.69 %
t_{01}	2.5 %	2.6 %
t_{02}	7.8 %	8.1 %
t_{03}	14.4 %	15.0 %

Chapter 4

State Space Modeling

State space analysis is a powerful mathematical technique that allows a designer to model the dynamics of any linear system [109]. Given that any switching interval in a power electronics circuit is is reducible to a linear subcircuit, the system is well-suited to leverage the benefits of a state space description. With multiple intervals, multiple state space descriptions need to be constructed and applied sequentially. These mathematical descriptions are combined to provide detailed insight into the steady state operation of a power electronics switched topology. Steady state waveforms that include harmonic content are created using the state space approach, detailing the non-sinusoidal voltages and currents of the system.

4.1 3-Level, Closed Form

To best explain the state space modeling technique, a 3-level synchronous rectifier is used as a less-complex example during derivation. This 3-level system operates in a similar manner

to the 7-level switched capacitor rectifier, and the conversion from the simpler model to the full model adds complexity but holds to the same basic derivation principles. The 3-level model used in this example is shown in Fig. 4.1.

The inverter of the system is a full-bridge with an ideal input source, V_{in}. The tuned WPT tanked is comprised of C_p, L_p, and R_p on the primary side and C_s, L_s, and R_s on the secondary, both of which are the same as the 7-level system. The rectifier is a full-bridge system as shown in Fig. 4.1. The output voltage is filtered by C_{out}, i_{out} is delivered to R_{load} just as in the 7-level system. The topological differences between the 3-level WPT system and the 7-level WPT system only exist in the rectifier. Otherwise, the two circuits are the same.

Fig. 4.2 shows the equivalent circuit model used to derive the differential equations of the wireless power system. The significance of Fig. 4.2 lies in the inverter model. The inverter switches are dropped and replaced by the ideal voltage source, V_{in}. Voltage v_{inv} is then assigned by simply changing the polarity of V_{in}. This simplified inverter model is effectively an ideal 2-level inverter, meaning the voltage v_{inv} can be one of two states: V_{in} or $-V_{in}$.

The rectifier is comprised of switches S_1 through S_4. These switches are configured in one of three ways at any given time. Fig. 4.3 illustrates the configurations of both the input and the rectifier stage. Switches S_1 and S_4 may be on, in which case $v_{rec} \approx v_{out}$. With switches S_2 and S_3 on, the rectifier's input voltage is approximately $-v_{out}$, and finally, the third configuration is to turn on S_3 and S_4 so that $v_{rec} \approx 0$. The on resistances of each switch prevent v_{rec} from being precisely equal to $\pm V_{out}$ and and 0. Fig. 4.3 shows the conduction path of i_{rec} in each configuration.

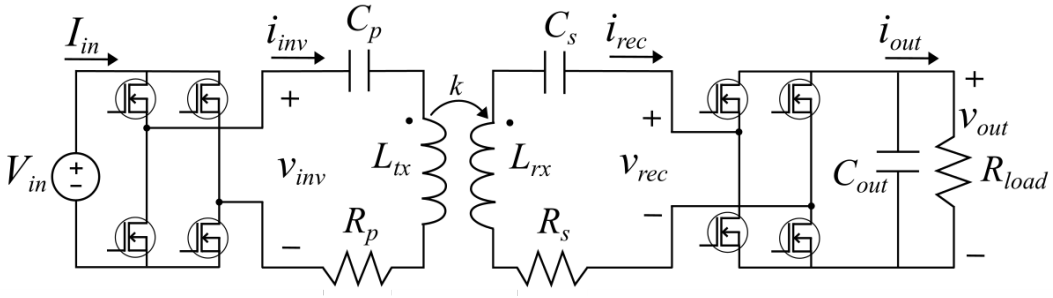


Figure 4.1: Example WPT system with a 3-level (full-bridge) rectifier.

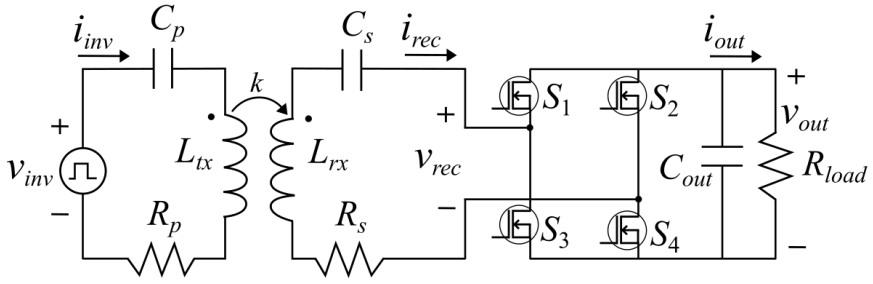


Figure 4.2: Equivalent circuit used to model the WPT system with a 3-level rectifier.

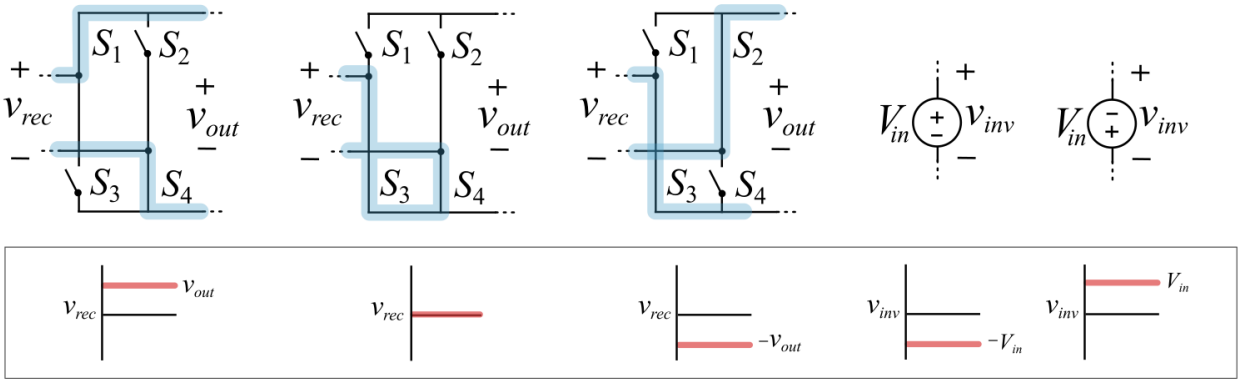


Figure 4.3: Every possible input (v_{inv}) and rectifier switch combination v_{rec}.

4.2 3-Level Circuit Operation

An example period is shown Fig. 4.4. Intervals I-IV show the positive half-cycle of the rectifier, and V-VIII show the negative half-cycle. The inverter output has positive polarity from intervals II-V and a negative polarity during VI, VII, VIII, and I. The polarities of each switch and the source V_{in} are given in Table 4.1, and the equivalent linear circuits converted from the k model to the T model for intervals I-IV are shown in Fig. 4.5. KVL and KCL equations are written for each linear circuit. Interval I is described by the following equation set:

$$-V_{in} = v_{Lp} + v_{LM} + v_{Cp} + i_{inv}R_p \tag{4.1}$$

$$v_{LM} = v_{Ls} + v_{rec} + i_{rec}R_s + v_{Cs} \tag{4.2}$$

$$v_{out} = i_{out}R_{load} \tag{4.3}$$

$$i_{inv} = i_m + i_{rec} \tag{4.4}$$

$$\dot{i}_{inv} = \dot{i}_m + \dot{i}_{rec} \tag{4.5}$$

The voltages are defined in the same polarity as the currents for all passive components, and the dot accent indicates a derivative such that $^{dx}/_{dt} = \dot{x}$. Applying the fundamental capacitor and inductor derivative equations

$$\begin{aligned} i_{inv} &= C_p\dot{v}_{Cp} \qquad & i_{rec} &= C_s\dot{v}_{Cs} \qquad & i_{out} &= C_{out}\dot{v}_{Cout} \\ v_{Lp} &= L_p\dot{i}_{inv} \qquad & v_{LM} &= L_M\dot{i}_m \qquad & v_{Ls} &= L_s\dot{i}_{rec} \end{aligned} \tag{4.6}$$

Table 4.1: 3-Level Circuit Interval Actuation

	I	II	III	IV	V	VI	VII	VIII
S_1	0	0	1	0	0	0	0	0
S_2	0	0	0	0	0	0	1	0
S_3	1	1	0	1	1	1	1	1
S_4	1	1	1	1	1	1	0	1
v_{inv}	-	+	+	+	+	-	-	-

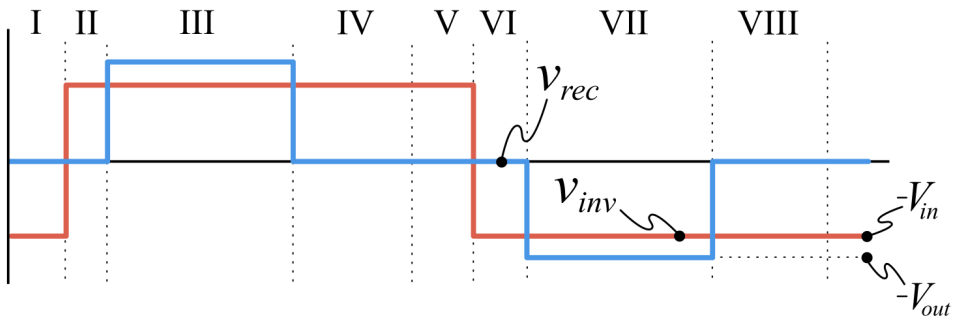


Figure 4.4: One period of v_{inv} and v_{rec} waveforms.

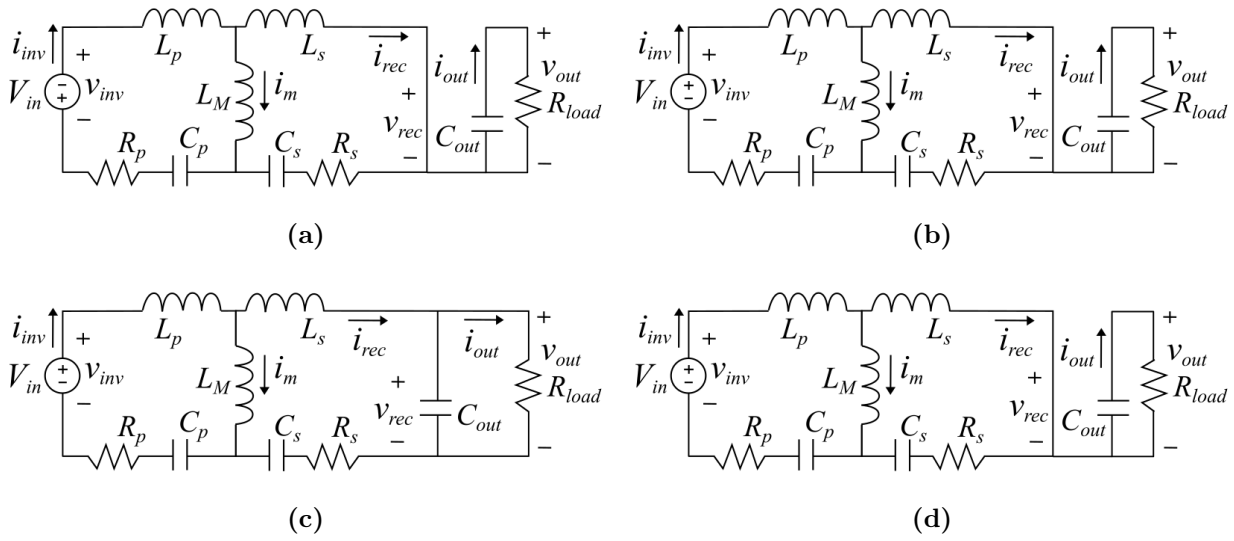


Figure 4.5: Equivalent circuits of intervals (a) I, (b) II, (c) III, and (d) IV as described in Fig. 4.4 and Table 4.1.

and realizing that $v_{rec} = 0$ during interval I, allows (4.1) - (4.5) to be written in terms of both the inductor currents and capacitor voltages and the derivatives of those inductor currents and capacitor voltages:

$$-V_{in} = L_p\dot{i}_{inv} + L_M\dot{i}_m + v_{Cp} + i_{inv}R_p \tag{4.7}$$

$$L_M\dot{i}_m = L_s\dot{i}_{rec} + 0 + i_{rec}R_s + v_{Cs} \tag{4.8}$$

$$v_{out} = C_{out}\dot{v}_{Cout}R_{load} \tag{4.9}$$

$$C_p\dot{v}_{Cp} = i_m + C_s\dot{v}_{Cs} \tag{4.10}$$

$$\dot{i}_{inv} = \dot{i}_m + \dot{i}_{rec}. \tag{4.11}$$

This set of equations is reduced such that each derivative term is described by non-derivative terms. Furthermore, either i_{inv}, i_m, or i_{rec} (and its respective derivative term) can be dropped because the three terms are not linearly independent. Essentially, if two currents are known, the third can always be described in terms of the two known values. The i_{rec} term is dropped in this example, and the five resulting equations are given by

$$\begin{aligned}\dot{i}_{inv} =& \Big(i_m L_M R_s - i_{inv}(L_M R_p + L_s R_p + L_M R_s) - \\ & v_{Cp}(L_M + L_s) - v_{Cs}L_M - V_{in}(L_M + L_s) \Big) \cdot \frac{1}{L_p L_M + L_p L_s + L_M L_s}\end{aligned} \tag{4.12}$$

$$\dot{i}_m = \Big(i_{inv}(L_p R_s - L_s R_p) - i_m L_p R_s - v_{Cp}L_s + v_{Cs}L_p - V_{in}L_s \Big) \cdot \frac{1}{L_p L_M + L_p L_s + L_M L_s} \tag{4.13}$$

$$\dot{v}_{Cp} = \frac{\dot{i}_{inv}}{C_p} \tag{4.14}$$

$$\dot{v}_{Cs} = \frac{\dot{i}_{inv} - \dot{i}_m}{C_s} \tag{4.15}$$

$$\dot{v}_{Cout} = \frac{v_{out}}{C_{out} R_{load}}. \tag{4.16}$$

The important characteristic of equations (4.13) - (4.15) is that each derivative term is described only in terms of the passive values, inductor currents, capacitor voltages, and sources. This description makes no approximations about the circuit in Fig. 4.5a and is a complete characterization of the linear system in interval I. Interval I is put forth as an example here, and any interval can be described by its differential equations in the same manner.

4.3 State Space Representation

State space is a matrix representation for linear systems. State space is a well established mathematical description. It is applied to power electronics circuits frequently, modeling the dominant dynamics. The general state space description is

$$\frac{dx}{dt} = \dot{x}(t) = Ax(t) + Bu(t), \quad [110] \tag{4.17}$$

where $x(t)$ is the time-dependant state vector, $\dot{x}(t)$ is the time derivative of the state vector, and $u(t)$ is the input vector. Matrix A contains constant values that describe how the states, $x(t)$, affect the derivative of the states, $\dot{x}(t)$. Likewise, B describes how $u(t)$ affects $\dot{x}(t)$. If

$x(t)$ is a $n\times1$ vector, then $\dot{x}(t)$ is also $n\times1$ in size, and A is a $n\times n$ square matrix. If $u(t)$ is $m\times1$, then B is a $n\times m$ matrix. This multiplication is visualized by

$$\dot{x}(t)_{n\times1} = A_{n\times n}\, x(t)_{n\times1} + B_{n\times m}\, u(t)_{m\times1}. \tag{4.18}$$

Inductor currents and capacitor voltages comprise the state vector. The 3-level rectifier example state vector is assigned as

$$x(t) = [i_{inv} \;\; v_{Cp} \;\; i_m \;\; v_{Cs} \;\; v_{out}]^T, \tag{4.19}$$

where i_{rec} is left out because it is not linearly independent of i_{inv} and i_m. The derivative of the state vector is then

$$\dot{x}(t) = [\dot{i}_{inv} \;\; \dot{v}_{Cp} \;\; \dot{i}_m \;\; \dot{v}_{Cs} \;\; \dot{v}_{Cout}]^T. \tag{4.20}$$

Notice that the elements of $\dot{x}(t)$ are the same elements solved for in (4.12) - (4.15). The state space description is a way to write equations (4.12) - (4.15) in matrix form. Aside from component values, the element not yet accounted for is V_{in}, which is an ideal constant voltage. Independent voltage and current sources comprise the input vector, and because they are treated as constants, the input vector's time-dependence is dropped: $u(t) \approx U$. For interval I, the input vector is defined as

$$U = [V_{in}] \tag{4.21}$$

because there is only one source in Fig. 4.5a. With $x(t)$, U, and $\dot{x}(t)$ defined, only matrices A and B remain in order to have a full state space description for interval I. Matrix B describes how the inputs affect the state derivatives. Equations (4.12) - (4.15) outline how each state derivative is dependent on the input V_{in}. In this way, each equation informs one of the rows of B such that

$$B = \begin{bmatrix} \frac{-L_M L_s}{L_p L_M + L_p L_s + L_M L_s} \\ 0 \\ \frac{-L_s}{L_p L_M + L_p L_s + L_M L_s} \\ 0 \\ 0 \end{bmatrix}, \tag{4.22}$$

where the values in the first and third rows are determined by equations (4.12) and (4.13), respectively. Equations (4.14), (4.15), and (4.16) do not have a term that includes V_{in}, so the corresponding indices of the input vector are set to 0. Matrix A is constructed using the same approach,

$$A = \begin{bmatrix} \frac{(L_M R_p + L_s R_p + L_M R_s)}{den} & \frac{-(L_M + L_s)}{den} & \frac{L_M R_s}{den} & \frac{-L_M}{den} & 0 \\ \frac{1}{C_p} & 0 & 0 & 0 & 0 \\ \frac{(L_p R_s - L_s R_p)}{den} & \frac{-L_s}{den} & \frac{-L_p R_s}{den} & \frac{L_p}{den} & 0 \\ \frac{1}{C_s} & 0 & \frac{-1}{C_s} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{out} R_{load}} \end{bmatrix}, \tag{4.23}$$

where $den = L_p L_M + L_p L_s + L_M L_s$. Index A_{nm} denotes the element of A in row n and column m. A_{11} is taken from (4.12) and represents how $\dot{i}_{inv}$ is affected by i_{inv} within the

differential equations. The assignment is dictated by the position of i_{inv} (index 1) within the state vector. Likewise, A_{12} is also taken from (4.12) and represents how $\dot{i}_{inv}$ is affected by v_{Cp} (index 2 in the state vector). This process is continued until the entire 5×5 A matrix is built, representing how each of the state derivatives $\dot{x}(t)$ are influenced by each of the states $x(t)$.

This completes the state space description of the 3-level rectifier WPT system for interval I. Vectors $x(t)$ and U (and consequently $\dot{x}(t)$) remain the same for all the other intervals in the system. Matrices A and B are determined by the subcircuit for any given interval and will change with the differential equations of the circuit. For this reason, subscripts are assigned to A and B to denote the interval. Intervals I through VIII in Fig. 4.4 are represented by $\{A_1, A_2, ...A_8\}$ and $\{B_1, B_2, ...B_8\}$.

The state space for each of the intervals is a closed form representation of the linear subcircuit in that interval. The model includes the dynamics of each linear component, which means all the main harmonic components are considered. Switching actions are implied within the model by changing from one interval to another in an ideal fashion, so detailed switching non-linearities are not modeled.

4.4 7-Level, PLECS

The proposed circuit's state space representation consists of the same processes presented for the 3-level converter. The inverter is modeled as a voltage source and assumed to be ideal. Each rectifier half-bridge is complimentary, aside from the charge sharing switches

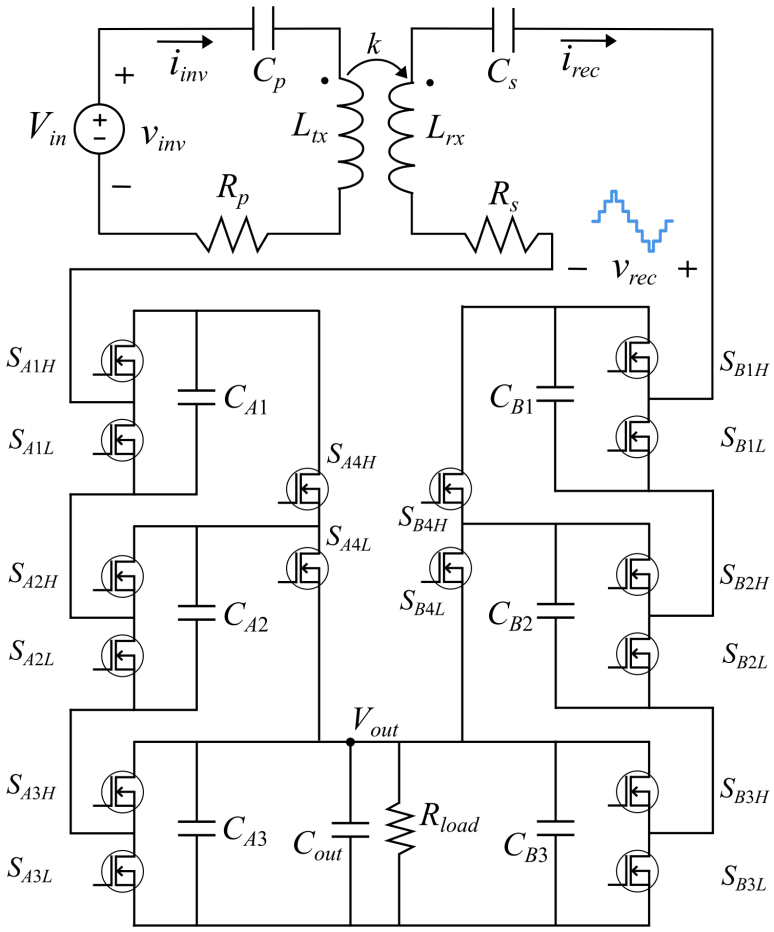


Figure 4.6: The proposed circuit as it is modeled in state space.

which may be on or off together. The proposed 7-level switched capacitor wireless power circuit is shown in Fig. 4.6 as it is modeled in state space form.

Next, the differential equations are written for the states, but in this case there are 11 states in total after the additions of C_{A1}, C_{A2}, C_{A3}, C_{B1}, C_{B2}, and C_{B3}. Because of the size of the state vector, the A and B matrices are now 11×11 and 11×1, respectively. Lastly, there are more intervals, so the amount of computation required increases rapidly as the circuit complexity increases.

It is more time-efficient to perform the state space calculations numerically than it is to derive all necessary closed-form matrices. The program PLECS is used to numerically extract the state space from each subcircuit [111]. The PLECS GUI allows the user to draw a circuit and include the switches and then pass boolean logic into the program for each switch to determine the state of that switch. If a switch is on, then the program inserts a small, defined resistance in place of the switch, and if it is off, then the system disconnects the gate and source nodes. Therefore, the numerical state space matrices extracted from PLECS account for switch conduction loss via the inclusion of on resistance. The proposed circuit as drawn in PLECS is shown in Fig. 4.7

The resistors in series with the capacitors are small values set to represent the ESR of the capacitors. The resistors in parallel with the capacitors are large values (200 Ω) that influence the circuit very little but make the numerical state space well-conditioned and allow the inverse of A to be found.

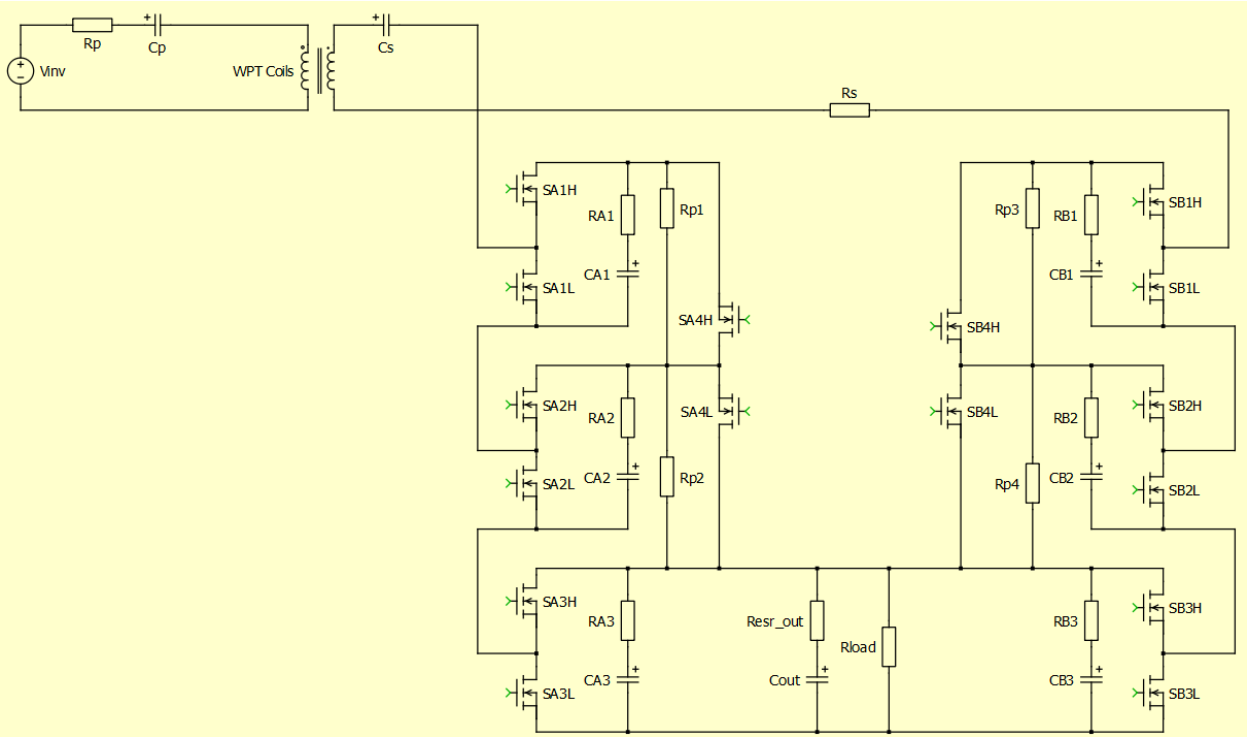


Figure 4.7: Layout of the proposed circuit in PLECS software.

4.5 Propagation Through Period and Steady State

With each interval constructed, the model must now be able to consider each of the intervals in succession. Equation (4.17) is manipulated by rearranging and inserting e^{-At}

$$e^{-At}\dot{x}(t) - e^{-At}Ax(t) = e^{-At}BU, \tag{4.24}$$

which can be simplified to

$$\frac{d}{dt}[e^{-At}x(t)] = e^{-At} \cdot BU. \tag{4.25}$$

Integrating both sides leads to

$$e^{-At}x(t) - x(0) = \int_0^t e^{-A\tau}BUd\tau, \tag{4.26}$$

and multiplying by e^{At} helps to isolate $x(t)$,

$$x(t) = e^{At}x(0) + \int_0^t e^{At}e^{-A\tau}BUd\tau. \tag{4.27}$$

Finally, the integration term is easily evaluated because U is constant:

$$x(t) = e^{At}x(0) + A^{-1}(e^{At} - I)BU. \tag{4.28}$$

Equation (4.28) is a closed-form solution for any state space system, and it is a function of only t and $x(0)$. Where a simulation program may calculate $\dot{x}(t)$, project $x(t)$ for a small

time step using $\dot{x}(t)$, and repeat, equation (4.28) is used to calculate the states without the need for fast sampling times. The closed form solution in (4.28) increases both computation speed and precision relative to a time-stepped simulation.

For a power electronics circuit with multiple intervals, the final value of the previous interval is used as the initial value for the states during the current interval. The A and B matrices change with the interval being calculated. This allows (4.28) to propagate through the entire switching period of a multi-interval control scheme. Interval I has an initial state vector of x_0, a duration of t_1, and a final value of x_1. When the circuit switches to interval II, x_1 is the initial value of the state vector, and the system propagates to x_2 over time duration t_2. Vector x_2 then initializes interval III, and the process is repeated. This allows the circuit to propagate through each state space interval in the period.

The example application of (4.28) for interval I is initialized with x_0 and given by

$$x_1 = x(t_1) = e^{A_1 t_1} x_0 + A_1^{-1}(e^{A_1 t_1} - I)B_1 U. \tag{4.29}$$

Equation (4.28) is again applied to interval II, but here it is initialized by the output of (4.29). Interval II is calculated with

$$x_2 = x(t_2) = e^{A_2 t_2} x_1 + A_2^{-1}(e^{A_2 t_2} - I)B_2 U, \tag{4.30}$$

and then x_2 is used to initialize interval III and so forth. The end of the period is signified by x_{16}, or the final value of the state vector at the end of the final interval. If $x_{16} = x_0$,

then the state vector at the beginning of the period is equal to the state vector end of the period, and the system is in steady state. A mathematical model for steady state is derived by inserting each period into the next as illustrated by (4.29) and (4.30), setting the initial state vector to the final state vector ($x_0 = x_{16}$ in this example), and simplifying the mathematical expression. The resulting solution for a 16 interval circuit is given by

$$X_{ss} = X_{ss1} = \left(I - \prod_{i=16}^{1} e^{A_i t_i}\right)^{-1} \sum_{i=1}^{16} \left(\prod_{k=16}^{i+1} e^{A_k t_k}\right) A_i^{-1}\left(e^{A_i t_i} - I\right) B_i U, \quad [112] \tag{4.31}$$

where $X_{ss} = X_{ss1}$ is the steady state state vector at the beginning of the period. Fig. 4.8 illustrates the full switching period of the 7-level WPT system, the time durations of each interval, the A and B matrices for each interval, and the notation for steady state (X_{ssn}) at each interval.

A mathematical description is obtained for the 7-level wireless power system drawn in Fig. 4.6. Any interval's linear subcircuit can be described by differential equations and then represented by state space notation, but due to the complexity of the 7-level converter, a numerical solution is extracted using PLECS. Given that $u(t) \approx U$, a closed-form solution for evaluating the state vector at any point during the interval is defined in (4.28). Given the switching durations, each interval is used to initialize the next, and steady state is defined by (4.31) when the switching period begins and ends at the same point. The state space system description and numerical solution for steady state make no approximations about each interval's linear subcircuit, and as such, include almost all circuit dynamics.

4.6 Example Operating Point

To illustrate the usefulness of this modeling approach, an example operating point is investigated. The parameter values for this example operating point are not optimized. The t_{01}, t_{02}, and t_{03} parameters are given in terms of the percentage of the total period. R_{dson} and ESR,C are the equivalent series resistances of the switches and the capacitors, respectively.

Every metric listed in Table 4.2 is an input to the state space model aside from V_{out} and η. The user defines the passive and parasitic values as well as the interval ordering and durations. The value of V_{out} is given by integrating the state vector during each interval and adding the time-weighted sum of each integrated value for the index containing v_{Cout} within $x(t)$. The average value of the state vector within interval i is given by

$$X_{avg} = \frac{A_i}{t_i}\Big[\big(e^{A_i t_i} - I\big)x_0 + A_i^{-1}\big(e^{A_i t_i} - I - A_i t_i\big)B_i U\Big]. \tag{4.32}$$

Therefore, (4.32) is executed in steady state for every interval, and then the time-weighted average of each interval yields: $V_{out} \approx v_{Cout}$. The DC value of V_{out} is listed as 5 V in Table 4.2, but the model includes what small ripple is present in the waveforms. This ripple is shown in Fig. 4.9. If A is singular and cannot be inverted, then the method in [112] is used.

The efficiency is returned by dividing the averaged input and output powers using (4.32) as well. The input current is averaged in each interval and multiplied by $\pm V_{in} t_i/T_s$, where t_i/T_s is the proportion of interval i within period T_s. The output power is calculated with

Table 4.2: Example State Space Operating Point

Parameter Values					
L_{tx}	L_{rx}	C_p	C_s	R_p	R_s
10 μH	10 μH	750 nF	100 nF	100 mΩ	200 mΩ
f_s	k	V_{out}	V_{in}	R_{load}	η
150 kHz	0.6	5 V	15 V	2.23 Ω	91.5%
t_1	t_2	t_3	$\angle(v_{inv} - v_{rec})$	R_{on}	R_C
2.6%	8.1%	15.0%	36°	10 mΩ	5 mΩ

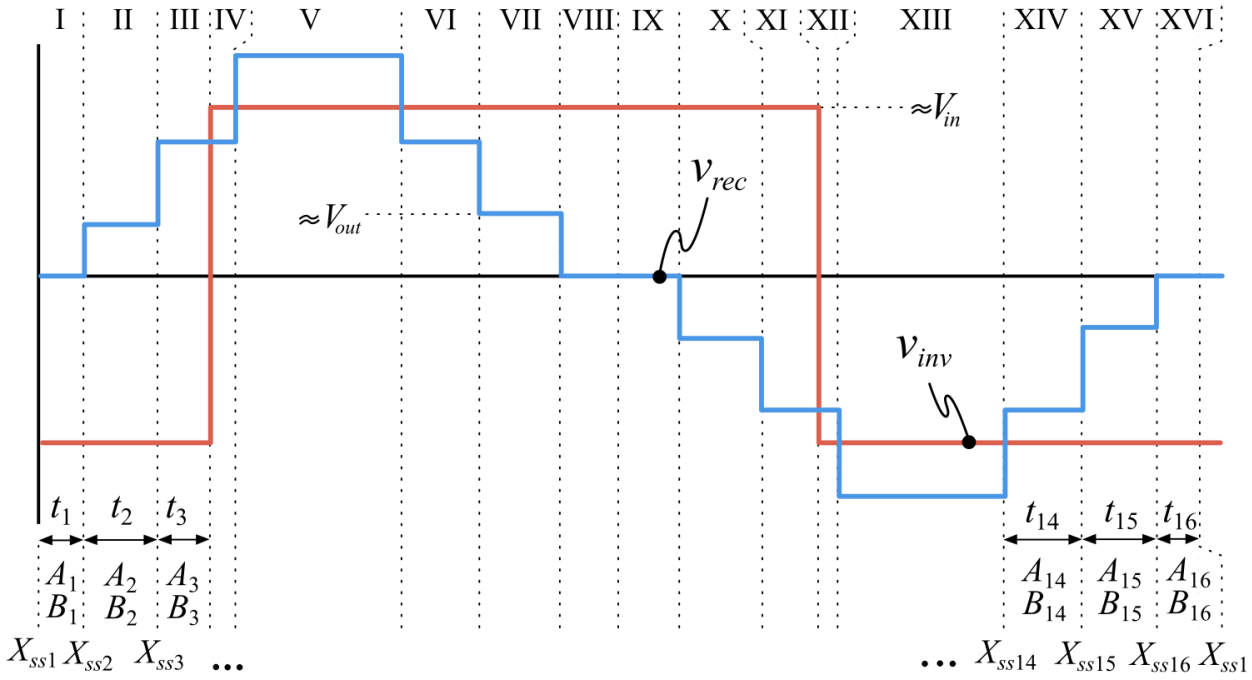


Figure 4.8: One switching period with the defined interval times, A and B matrices, and steady state $x(t)$ values.

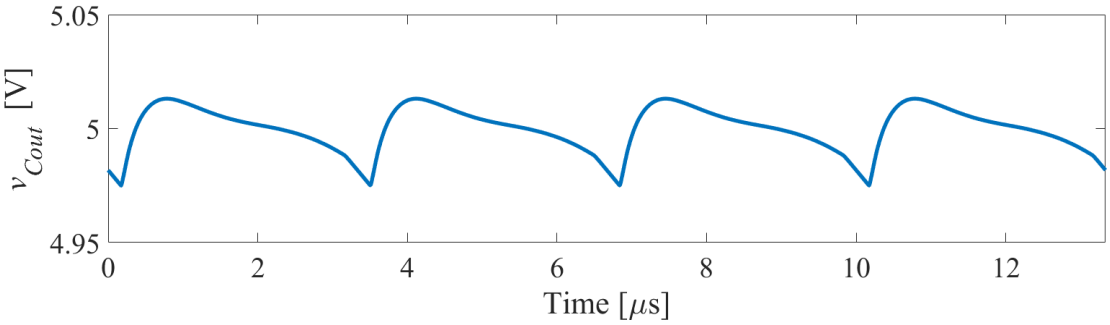


Figure 4.9: Voltage on capacitor C_{out} in state space model.

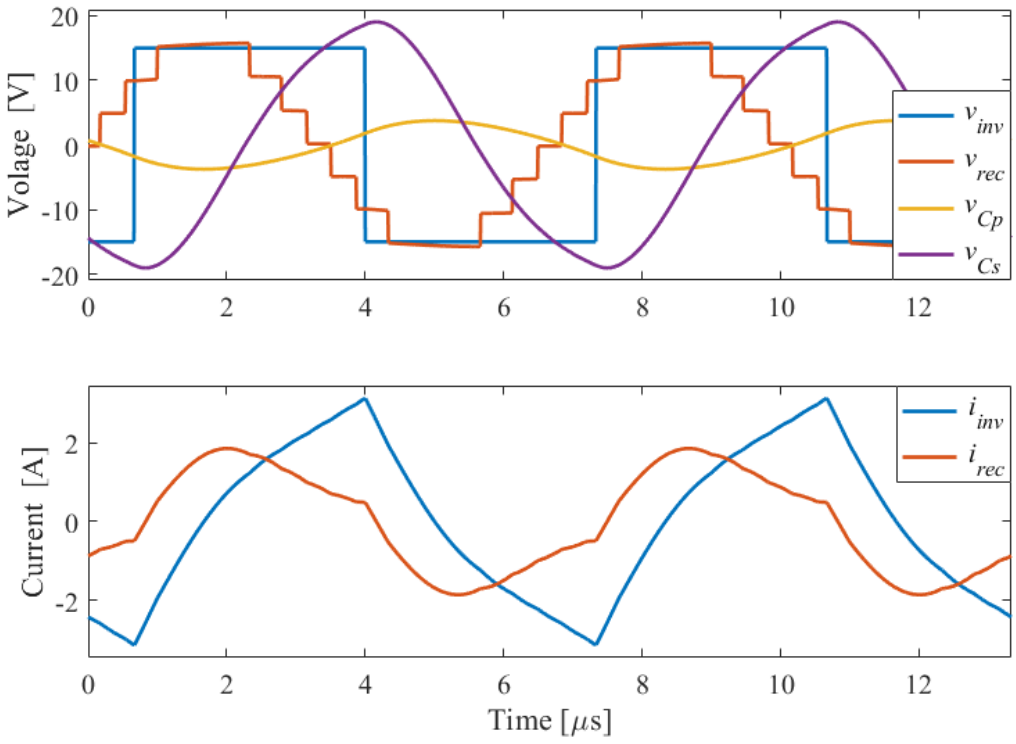


Figure 4.10: Waveforms of the state space model for the 7-level WPT system using the example operating point outlined in Table 4.2.

$P_{out} = {V_{out}^2}/{R_{load}}$. The model inherently includes all conduction and charge sharing losses. Switching loss is added after execution of the state space model by subtracting the calculated switching loss from the total output power (the traditional power electronics high efficiency assumption).

The waveforms of the operating point outlined in Table 4.2 are shown in Fig. 4.10. The 7-level inverter voltage looks as expected, with the addition of a small slope during the $v_{rec} \approx 3V_{out}$ portions of the modulation. This slope is present during each interval but is most noticeable here. It is the result of voltage across the non-ideal device ESRs and shows the level of intricacy that state space modeling captures. Another important characteristic of the model is the non-sinusoidal current waveforms. Fundamental modeling is a useful approach to wireless power, but it neglects harmonic content. State space modeling inherently includes the harmonic content of the system within the modeled waveforms.

4.7 Additional Implementations

Multiple versions of the model are constructed to better match other experimental setups. One such example is the use of a current source as a load instead of a resistor. Here, R_{load} is substituted for I_{load} and the fundamental steady state operating points are matched between the two systems. The state space now includes I_{load} in the input vector such that

$$U = \begin{bmatrix} V_{in} \\ I_{load} \end{bmatrix}. \tag{4.33}$$

Another model is built to include potential parasitic resistance and inductance. The resistive parasitics contribute to conduction loss. The inclusion of these parasitic elements influences the peak currents predicted by the model when connecting two capacitors in parallel. The parasitic resistors increase the RC time constant, and the inductors act as a filter to reduce the maximum peak current by reducing the rate of current change in any high current path [113]. Fig. 4.11 shows a PLECS model that includes many inductive and resistive parasitics.

Including parasitic elements does not change the switching times or input vector, but the size of the state vector is dramatically increased. In the case of Fig. 4.11, the state vector contains 35 elements. Each individual parasitic inductance is a history-dependent component and must be included in $x(t)$. With a state vector this long, closed-form solutions that include parasitic components are even more time-inefficient to derive, and the importance of the numerical solution technique is re-emphasized.

4.8 Model Comparison

State space modeling is a powerful approach, and it is implemented for the 7-level switched capacitor rectifier WPT system because of its advantages over the fundamental model extrapolated in Chapter 3. Fundamental modeling is built the assumption that harmonic content can be ignored, and that capacitor voltages can be modeled as DC. While these assumptions are well-founded, comparison to both a simulation and the state space model highlights the benefit of modeling without such assumptions.

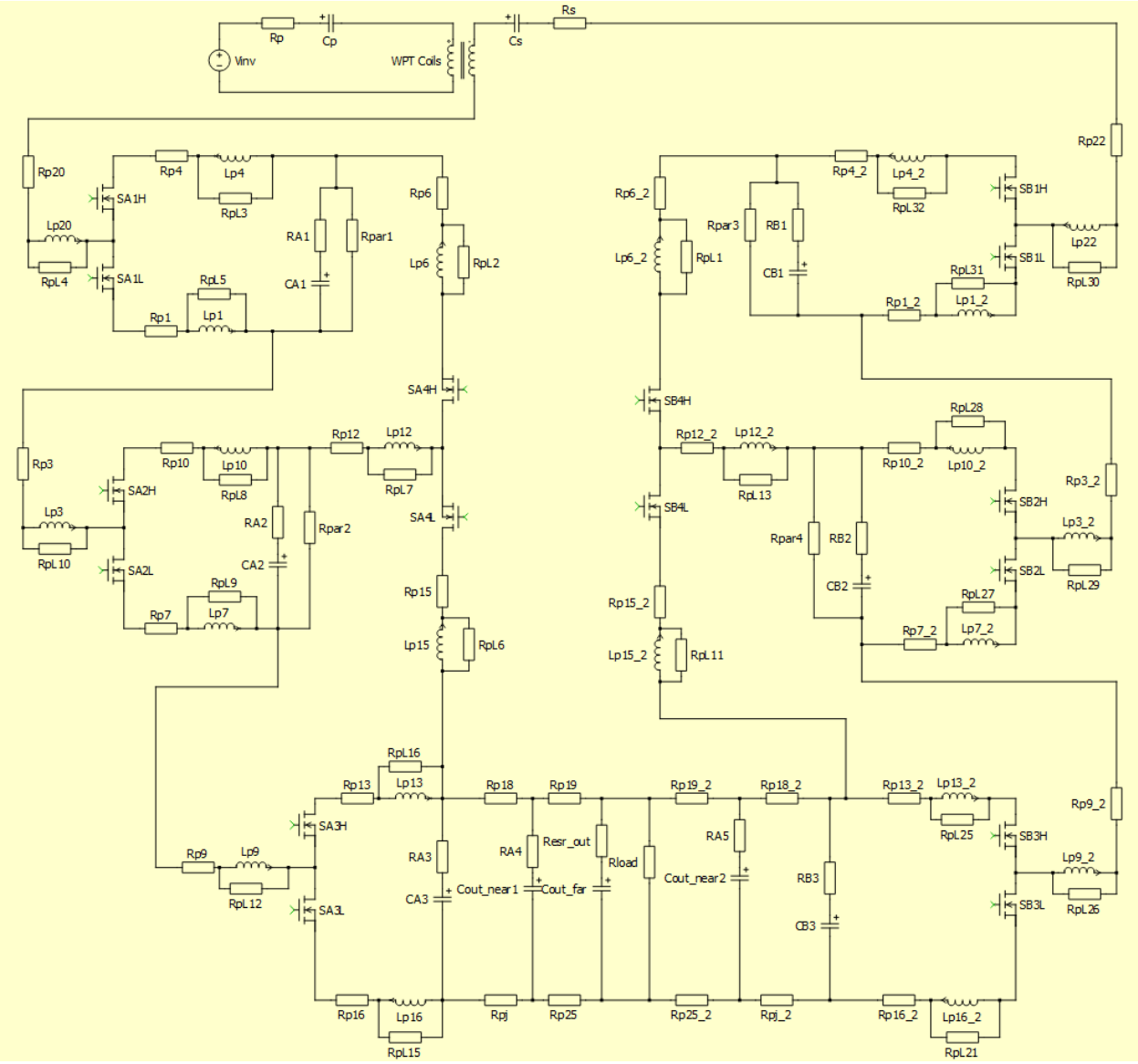


Figure 4.11: PLECS circuit layout including parasitic resistance and inductance.

First, the fundamental model ignores harmonic content within the waveforms, asserting that the majority of the loss and power delivery can be characterized by ignoring the harmonic components. This tends to be well-founded because WPT systems are generally tuned at or near the fundamental frequency. However, because the state space model is able to include every linear subcircuit, all of the dominant dynamics are present in the waveforms. This is beneficial when calculating loss. Fig. 4.12 compares the harmonic content of the fundamental, state space, and ltspice circuits using the operating point outlined by Table 3.4 at the end of Chapter 3.

Conduction loss is a function of the square of the current, meaning that divergence from an expected current is rapidly adds unmodeled loss to a system. Considering waveforms containing the full harmonic content gives a more accurate picture of conduction loss than only considering the fundamental. Furthermore, waveform distortion due to harmonic content gives a more accurate value for turn-on and turn-off current at the time of switching actions, increasing the accuracy of the switching loss predictions. Table 4.3 compares each of the two models with the simulation. Compared to the fundamental model, the state space model does a better job of precisely predicting system efficiency.

Charge sharing losses are also inherently considered in the state space model. This means that, unlike the fundamental model, no assumptions are made about each capacitor being connected to an ideal source in order to balance. The capacitors are connected in parallel with one another, and the resulting voltages are determined by the circuit while the redistribution time constants are determined by the capacitance values and any included parasitics. Because the times of redistribution are determined by the parasitics included in

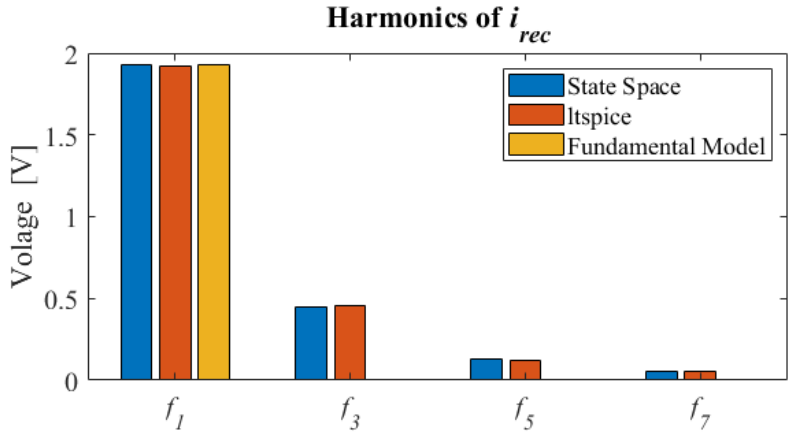


Figure 4.12: Harmonic content of i_{rec} for the fundamental model, state space model, and ltspice simulation.

Table 4.3: Models Compared with Simulation

	Fundamental	ltspice	State Space
$\lvert v_{rec,1}\rvert$	15.91 V	16.02 V	15.91 V
$\lvert i_{rec,1}\rvert$	1.93 A	1.92 A	1.93 A
$\lvert v_{inv,1}\rvert$	19.10 V	19.07 V	19.10 V
$\lvert i_{inv,1}\rvert$	1.88 A	1.89 A	1.88 A
$\lvert Z_{rec,1}\rvert$	8.23 Ω	8.32 Ω	8.32 Ω
$\angle Z_{rec,1}$	46.46°	46.05°	46.43°
V_{out}	5.00 V	5.00 V	5.00 V
M	3.18	3.20	3.18
R_{load}	1.82 Ω	1.82 Ω	1.80 Ω
P_{in}	14.77 W	14.85 W	14.88 W
P_{out}	13.49 W	13.76 W	13.70 W
η	91.36 %	92.69 %	92.28 %
t_1	2.5 %	2.6 %	2.6 %
t_2	7.8 %	8.1 %	8.1 %
t_3	14.4 %	15.0 %	15.0 %

the model, fast and slow switching limits are naturally considered by the state space model. If the system is switching too quickly, then the capacitors do not fully charge. Likewise, if the switching is too slow, then the capacitors do not retain charge. In either case, the power waveforms reveal the consequences, thereby highlighting SSL or FSL operation.

Table 4.4 summarizes the two modeling techniques in terms of assumptions. It shows how the state space model is better suited to characterize the WPT system than the fundamental model. The analysis proves the viability of using state space to represent the 7-level switched capacitor topology for power signal modeling.

While the inclusion of harmonic content, inherent consideration of switching limits within the power waveforms, and a more precise efficiency prediction are beneficial attributes, the most important reason that state space is chosen for this work is its connection to small signal modeling. State space is the foundation for building a small signal discrete time model. The 7-level switched capacitor circuit is a complex topology to control, and accurately predicting the plant behavior is an essential step in establishing stability. Section 6 expands the state space modeling approach presented here to include a small signal model, further emphasizing the importance of using state space as the foundation for modeling the power waveforms.

Table 4.4: Comparison of the Fundamental Harmonic Analysis (FHA) and State Space Modeling Approaches for the 7-Level Switched Capacitor Rectifier WPT System

	Updated Model (State Space Technique)	Original Model (FHA Analysis)
Waveforms	All Dominant Harmonics	**Assumption:** Fundamental
System Loading	All Dominant Dynamics	**Assumption:** Fundamental
Components	**Assumption:** Linear	**Assumption:** Linear
Conduction Loss	Inherently Considered	**Assumption:** Fundamental
Charge Sharing Loss	Inherently Considered	**Assumption:** High Efficiency
Switching Loss	**Assumption:** High Efficiency	**Assumption:** High Efficiency
FSL & SSL	Inherently Considered	**Assumption:** Within Range + Small Ripple

Chapter 5

Experimental Platform

A 20 W prototype system is constructed to verify the power models. The system is built with an inverter, interchangeable WPT coils, the 7-level rectifier, and voltage sensing capabilities. Each rectifier switch is driven by a bootstrap circuit level-shifted voltage source with a secondary option to connect isolated voltage sources to circumvent the bootstrap circuit. The experimental platform is also constructed with the capacity for testing control problems, and the system consequently showcases multiple FPGA controllers and phase sensing capabilities.

5.1 Prototype WPT System

The experimental setup is shown in Fig. 5.1. The circuits are designed so that the inverter and rectifier can be controlled by the same FPGA (shown in Fig. 5.1), or the two circuits can be controlled separately if necessary. The rectifier and inverter both use the half-bridge silicon module and gate driver listed in Table 5.1.

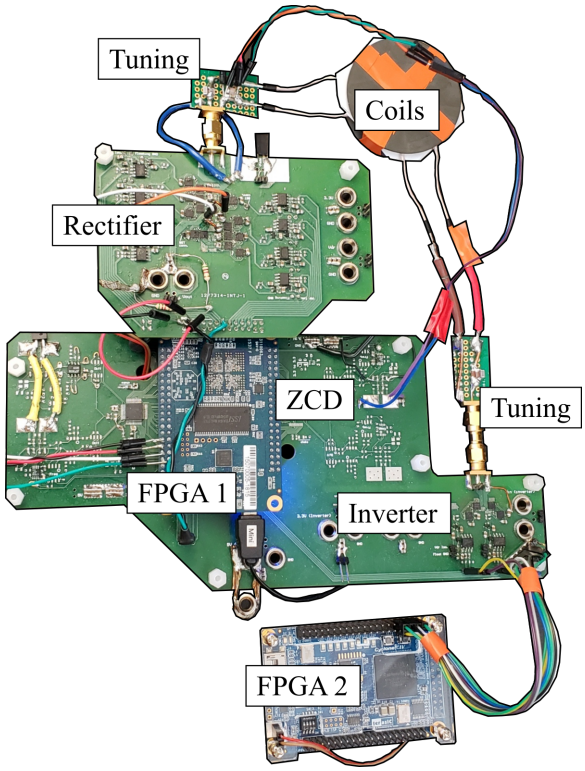


Figure 5.1: Experimental setup showing the FPGA controller, inverter, tuned WPT tank, and rectifier.

Table 5.1: System Specifications of Proposed MSC Rectifier

Component	Part	Parameter
Silicon Moduel (HB)	BSZ0910NDXTMA1	—
Gate Driver (HB)	MP1907AGQ-P	—
Isolator	SI8423BB-D-IS	—
Controller	Altera Cyclone IV	—
Transmitter Coil	760308101141	10 μH
Receiver Coil	760308101141	10 μH
Flying Capacitor	C1608JB1A226M080AC	4.42 μF*
Switching Frequency	—	150 kHz
Input Voltage	—	7-20 V
Output Voltage	—	5.0 V
Maximum Ouput Power	—	20 W

* Manufacturer's reported capacitance at 5 V DC bias.

Table 5.1 conveys that the capacitor used for each flying capacitance (C_{xx}) is 4.4 μF. The capacitor properties are 10 V, 22 μF, and 0603 size. However, the manufacturer (TDK Corporation) also provides values for the equivalent capacitance with a DC offset. At the $V_{out} = 5$ V DC offset to which each of the capacitors is subjected, the equivalent capacitance is reported as 4.42 μF. Each of the flying capacitances utilizes four of these devices in parallel, so the expected equivalent capacitance is: $C_{xx} = 4 \cdot 4.42\ \mu F = 17.68\ \mu F$. An impedance analyzer is used to measure four of the C1608JB1A226M080AC capacitors in parallel with a 5 V DC offset. The measured value is 15.66 μF with an 1.39 mΩ ESR value, and this value is used in calculations. Extending this measurement to the output capacitance with 15 capacitors yields: $C_{out} = 15/4 \cdot 15.66\ \mu F = 58.73\ \mu F$.

The transmitter and receiver coils are identical (by Würth Elektronik) and include both a ferrite and thicker wires to reduce loss. The 10 μH coils have a quality factor of $Q = 220$ at 125 kHz. The focus of this research is the MSC rectifier, and reducing extraneous system losses serves to highlight the efficiency of the proposed rectifier. The two coils are placed in alignment and secured to minimize coupling variance among different testing cases. High voltage, low ESR capacitors are used to tune the coils, and an impedance analyzer is used to measured the tuned tank.

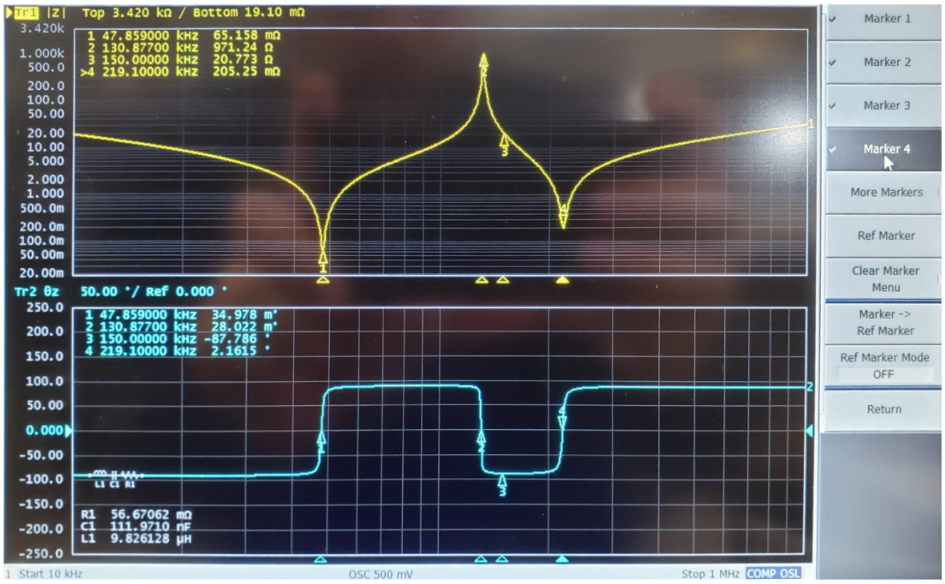
The following procedure identifies the coupling factor of the tuned coils. The primary and secondary sides are measured with the opposite side open – these open circuit tests return the values of L_{tx}, L_{rx}, C_p, C_s, R_p, and R_s. Then, the primary is measured with the secondary shorted, and the impedance analyzer is used to mark the three resonant locations. A photo of the impedance analyzer reading is shown in Fig. 5.2a. Coupling values are checked

against the closed form equations until the modeled tank impedance and the measured tank impedance show good agreement. Fig. 5.2b shows the calculated tank with a coupling of $k = 0.773$, and Table 5.2 compares the 3 resonant points and the impedance at 150 kHz to verify that the model matches the experiment.

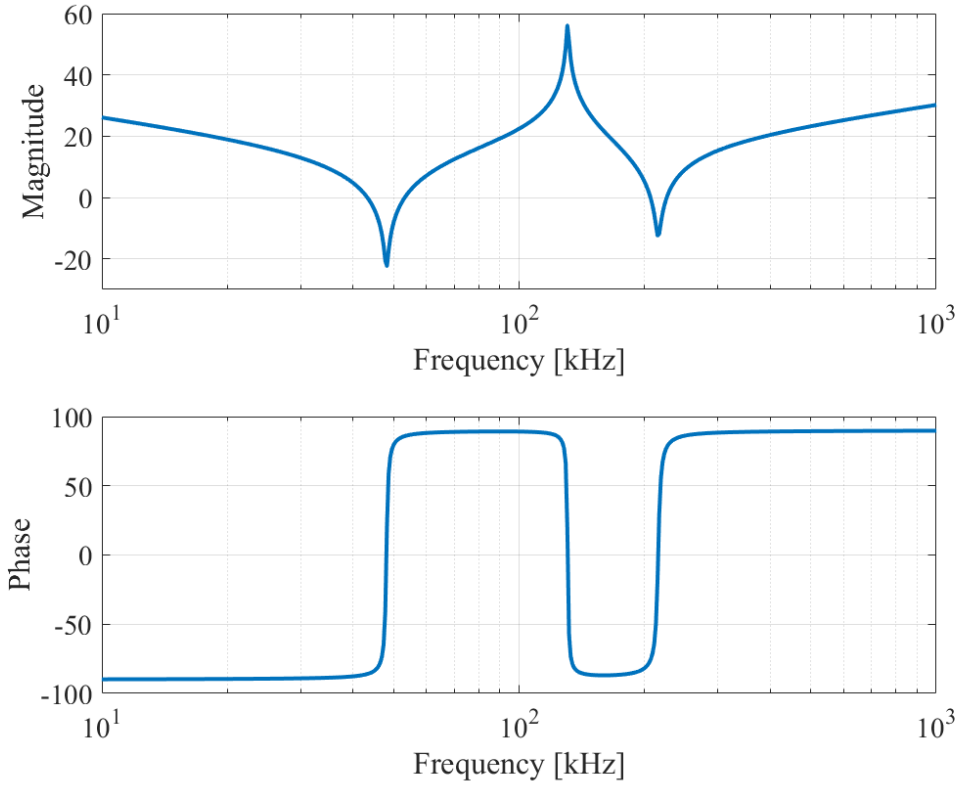
A half bridge silicone module is used as the switching device for the rectifier and inverter. The body diode conduction voltage (V_d), on resistance (R_{dson}), and output capacitance (C_{oss}) are pulled from the datasheet of the device. The output capacitance is an estimate based on the C_{oss} capacitance profile from the datasheet for the range 0-to-V_{dr}. V_{dr} is the 10 V driving voltage referenced from MOSFET gate to source.

Two tests are performed to measure the resistive components of the printed circuit boards. First, the large input capacitance is placed on a blank inverter board. Next, two of the complimentary inverter device pads are shorted with solder, and the impedance analyzer is used to measure the ESR at 150 kHz. The value returned by the impedance analyzer is called R_{inv} and models the conduction loss of the inverter PCB. In the model, parameter R_p is augmented to include R_{inv} and the R_{dson} values of each conducting switch.

Similarly, 6 series switches are shorted with solder on a blank rectifier board. The impedance analyzer is used to determine R_{rec}. This is the parasitic resistance in the PCB on the secondary side. In the model, R_s is augmented to included R_{rec} alone, as capacitor and switch ESR are already included in the state space model. Finally, Table 5.3 summarizes the measured and parasitic circuit values in the experimental platform.



(a)



(b)

Figure 5.2: The tuned tank impedance as (a) measured by the impedance analyzer and (b) calculated with the fundamental circuit.

Table 5.2: Equivalent Tuned Tank Impedance Comparison with $v_{rec} = 0$

Calculated			Measured		
Frequency kHz	Magnitude [Ω]	Phase [°]	Frequency kHz	Magnitude [Ω]	Phase [°]
48	-24.2	0	48	-23.7	0
131	60.9	0	131	59.8	0
150	19.9	-87.9	150	20.8	-87.8
215	-16.2	0	219	-13.8	2.2

Table 5.3: Properties of the Experimental Setup

Circuit Values							
C_{xx}	C_{out}	L_{tx}	L_{rx}	C_p	C_s	R_p	R_s
15.66 μF	58.73 μF	13.22 μH	13.26 μH	757.56 nF	111.76 nF	60.94 mΩ	63.41 mΩ

Noteworthy Characteristics			
V_{in}	V_{out}	P_{out}	f
7-20 V	5 V	20 W	150 kHz

Component Parasitics					
C_{oss}	R_{dson}	V_d	ESR C_{xx}	R_{rec}	R_{inv}
525 nF	7.7 mΩ	0.86 V	1.39 mΩ	41.39 mΩ	8.20 mΩ

5.2 Experimental Tank Tuning

The experimental setup is tuned according to Table 5.3. In Chapter 1, the WPT system is tuned so that the C_p/L_{tx} and C_s/L_{rx} pair resonances are both set to 150 kHz. This tuning cancels the reactive component of Z_{rec} required for optimal efficiency loading, simplifying the role of the rectifier. However, given the coupling value of the experimental system, tuning the WPT tank in this manner causes issues.

Fig. 5.3 shows the impedance presented to the inverter for both the experimental platform and the ideal tuning method. For the ideal method that cancels the reactive component, the middle resonance peak is at exactly 150 kHz as designed. The first and second harmonics, however, are very close to the subsequent resonance at higher frequency. This resonance is the outcome of $L_s + L_p$ interacting with C_p and C_s, and the resulting resonant frequency is 315 kHz. This negatively affects the platform by allowing the second and third harmonics to circulate through the primary power flow path, dramatically distorting the waveforms.

The experimental tuning places the following resonances: $[C_p, Ltx] \rightarrow 50$ kHz, $[C_s, L_{rx}] \rightarrow$ 130 kHz. More importantly, the resonance between L_s, L_p, C_p, and C_s is set at 208 kHz. This tuning helps to attenuate the harmonic content within the power waveforms. The comparison in Fig. 5.3 illustrates how the tuning approach serves to pull the high frequency resonant peak away from the harmonics.

The tank tuning is not the focus of this research, and the experimental tuning is not an optimal solution. The tuning solution put forth serves mainly to remove dynamics that would inhibit showcasing the wireless power system. Fig. 5.4 illustrates the operating area

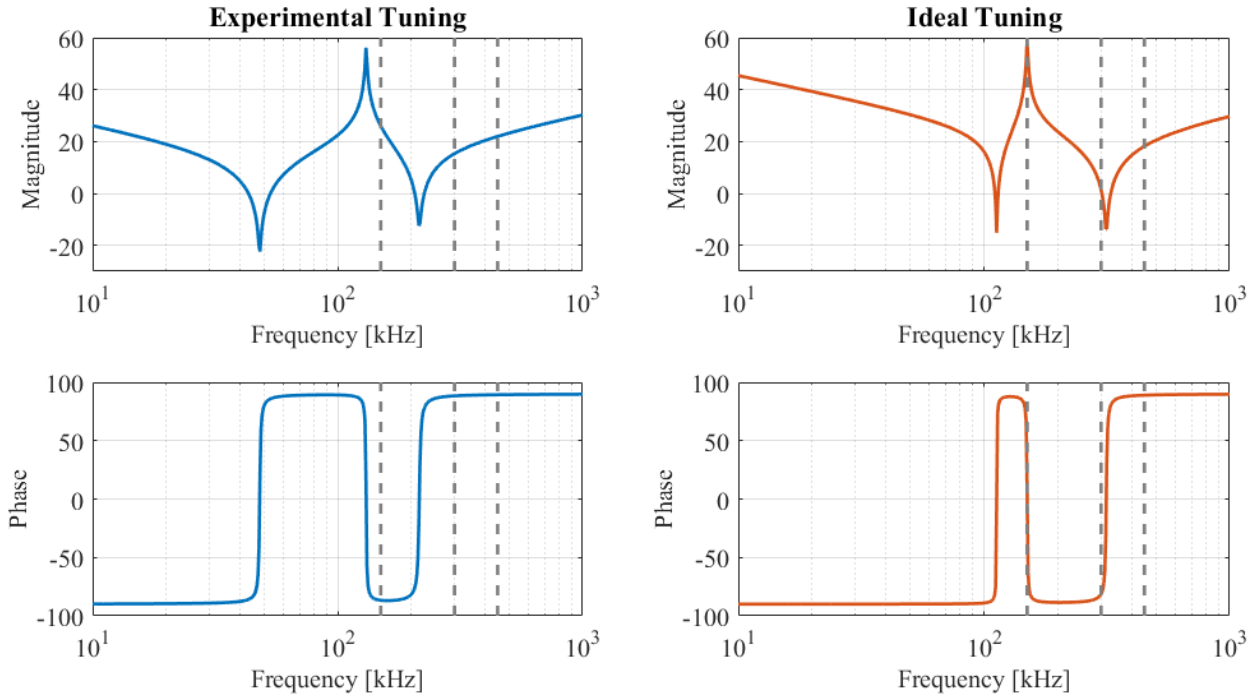
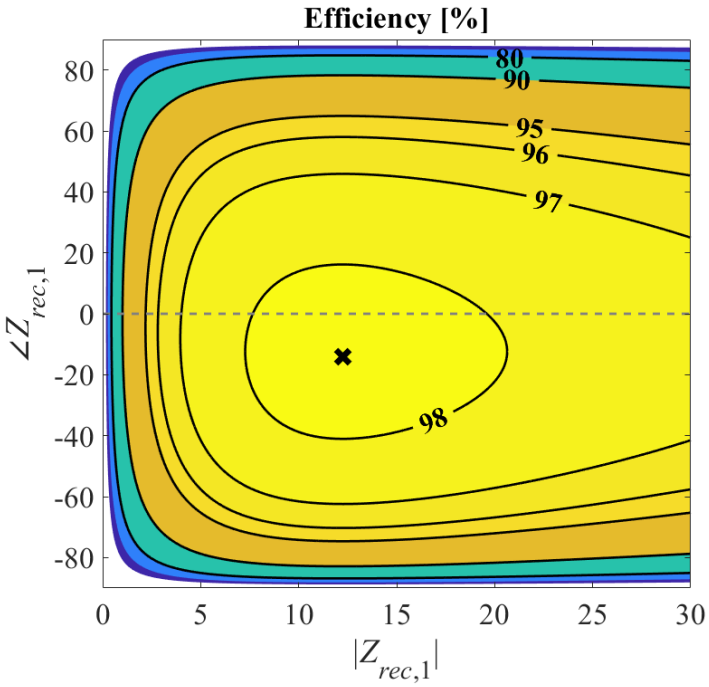
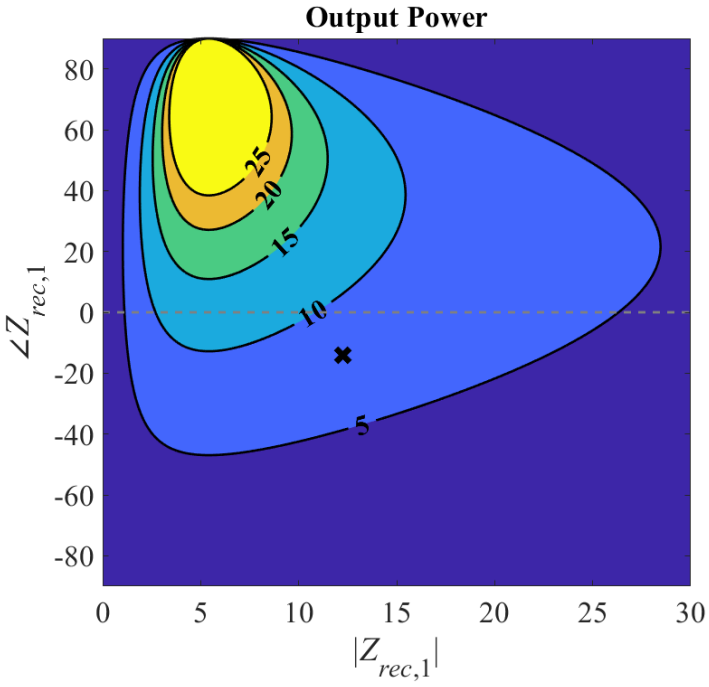


Figure 5.3: The impedance presented to the inverter with $Z_{rec} = 0$, including lines for the fundamental (150 kHz), second harmonic (300 kHz), and third harmonic (450 kHz). Both the experimental tuning (as implemented in the prototype) and the tuning that cancels the reactive component are shown.



(a)



(b)

Figure 5.4: The tank tuning of the experimental setup showing both (a) efficiency and (b) output power given the values in Table 5.3. The black x is the optimal efficiency point considering only tank conduction loss.

of the experimental tank using only the fundamental model. The peak efficiency is very high for the operating powers under test, meaning that the noteworthy features of the prototype will not be overshadowed by a poorly chosen tank design. In summary, the tank design considers harmonics and maintains a high enough efficiency at relevant powers to be used for this experimental platform.

5.3 Bootstrap Circuit

Each switch that is not ground referenced at the source requires a floating voltage for actuation. The two high side switches for the inverter require a boostrap circuit, but this circuit (shown in Fig. 5.5) is well-known and leverages the half-bridge driver and an external diode to charge the bootstrap capacitor. Bootstraping the rectifier is less straightforward, however. Six of the eight half-bridge modules are not referenced to ground, meaning that 14 of the 16 switches must operate using a floating voltage.

A generalization of each half-bridge module is shown in Fig. 5.5. The low-side switch is driven by the voltage on C_{LS}, and the high-side switch is driven by the voltage on C_{BST}. The half-bridge gate driver module (MP1907AGQ-P) has an internal bootstrap diode used to charge the bootstrap capacitor. The blue and green current paths highlight the charging routes for the low and high side driving capacitors, respectively. As shown, the low side charges continuously because the source V_{dr} is referenced to the low-side device source node. However, capacitor C_{BST} is only capable of charging when the low-side device is conducting.

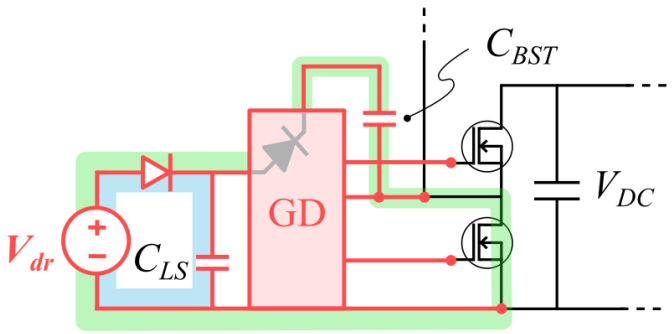


Figure 5.5: Basic boostrap circuit structure using a half-bridge gate driver module. The blue and green charging paths show how C_{LS} and C_{BST} charge, respectively.

This type of half-bridge control scheme is duplicated for the other power switches in the rectifier. One rectifier phase leg is shown in Fig. 5.6, and the boostrap circuitry is included. Power circuitry is shown in black, and the additional boostraping circuitry is shown in red. The blue and green paths illustrate how the highest level charges when both lower levels provide a path to the ground node. With this scheme, all driving capacitors are able to charge during the charge redistribution half-cycle when all low-side power switches are conducting. Each low side power switch is driven with a voltage of $V_{dr} - V_d$, and each high-side device is driven with a voltage of $V_{dr} - 2 \cdot V_d$.

The charge sharing switches are driven by the same half-bridge module, but the source of the low side charge sharing switch is never ground referenced (doing so would short the output voltage). The technique to charge the driving capacitors for the charge sharing switches is to utilize the power stage boostrap circuitry. Fig. 5.7 shows the full boostrap scheme for one rectifier phase leg. The charge sharing module charges the low-side driving capacitance through the floating boostrap capacitor for the power stage. This conduction path is shown in blue in Fig. 5.7 and requires that the high-side power switch in parallel with V_{out} be conducting. The green path shows how the charge sharing boostrap capacitor charges off the low-side capacitor when the low-side charge sharing switch is conducting.

This scheme results in driving voltages of $V_{dr} - 3 \cdot V_d$ and $V_{dr} - 4 \cdot V_d$ for the low and high side charge sharing switches, respectively. These diode drops do not result in a large negative effect because the diode drops are generally small, reduction of the driving voltage for the BSZ0910NDXTMA1 only minimally increases R_{dson} (the same would not be true of GaN devices), and the charge sharing switches are not meant to carry any significant

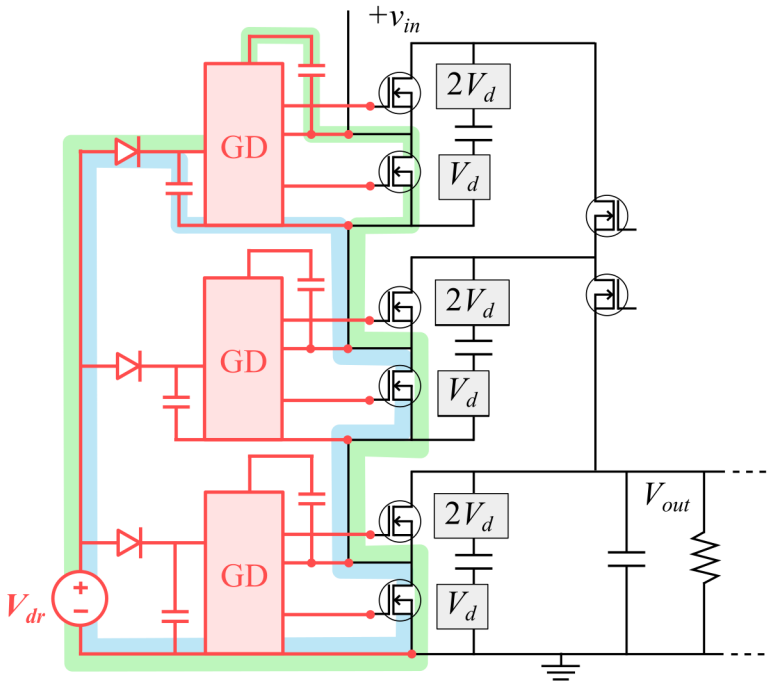


Figure 5.6: Boostrap circuit for the power switches in one rectifier phase leg. The charging paths of the highest level are shown by the blue and green lines.

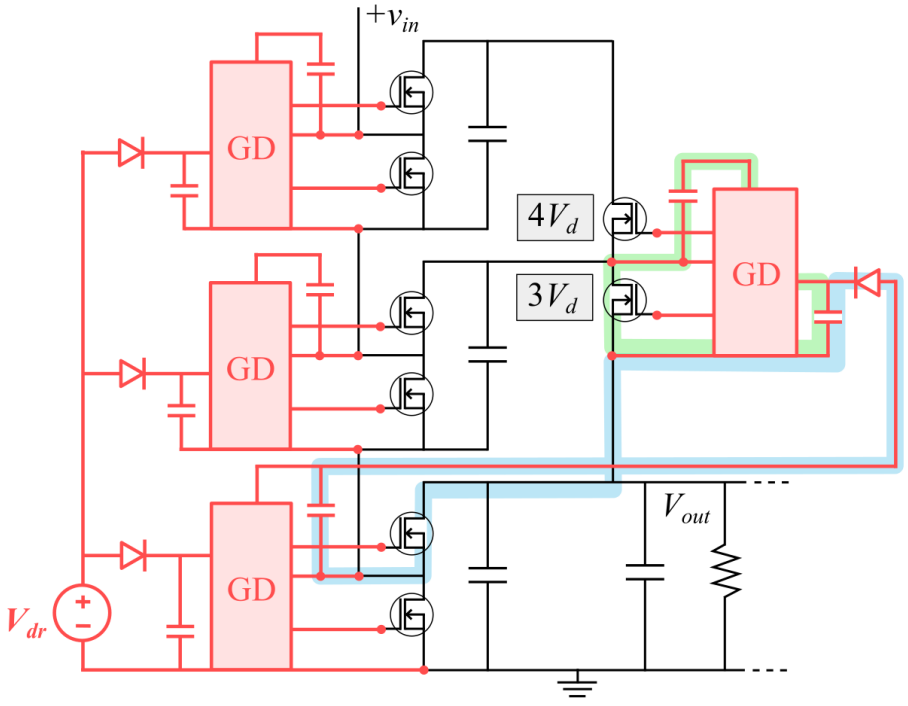


Figure 5.7: Boostrap circuit for the charge sharing switches in one rectifier phase leg.

power current. A better bootstrapping solution is to use the voltage on C_{x2} for level shifting the charge sharing switches, but the prototype is built according to Fig. 5.7 in order to separate the gate drive power from the power stage for efficiency modeling. If the topology is eventually integrated into a chip, using C_{x2} is likely the better option.

Overall, the switching scheme of the 7-level switched capacitor rectifier enables each device to be driven by a bootstrap circuit. The power switch boostrap capacitors charge in the half-period during which they are redistributing charge to the output. The charge sharing boostrap circuit charges during the portion of the period when the power switches are inserted into the path of i_{rec}. This technique allows all 16 rectifier switches to be driven by a single V_{dr} source plus a few extra diodes and capacitors, and it removes the need for any additional control overhead.

5.4 Power Stage Layout

The power stage is responsible for carrying the full power currents of the rectifier, and a close-up of the power stage portion of the layout is given in Fig. 5.8. The other circuitry that can be seen on the rectifier circuit board (upper PCB) in Fig. 5.1 is comprised of DC voltage connectors, bootstrap networks, isolators, and digital control circuitry.

Fig. 5.8 compares the rectifier power stage and a US quarter dollar to convey the compactness of the layout. Without the need for bulky DC inductance, the rectifier layout is very small. This compactness serves to reduce trace inductance and resistance, and it therefore also reduces consequent high frequency ringing and conduction loss. The dotted

white rectangle in Fig. 5.8 has an area of 27.5 mm $\cdot$ 31.4 mm = 863.5 mm^2, the thickness is 5.1 mm (including top and bottom components, excluding jumper wires), and the total volume is therefore $4,403.9$ mm^3 or $4,403.9 \cdot 10^{-9}$ m^3. At $P_{out} = 20$ W, this places the power density of the MSC at $4.54 \cdot 10^6$ W/m^3 or 74.42 W/in^3 in cubic inches. Notably, the only components on the bottom side of the board are bootstrap capacitors, so maneuvering only a few elements increases the power density to ≈ 103 W/in^3.

The 7-level SC rectifier enables output regulation without the need for a bulky filter inductance or discrete steps in voltage conversion. However, the compact layout in Fig. 5.8 only begins addressing the MSC's full potential to be a power dense topology. The experimental power density is limited by the discrete layout (however compact it may be), and a size optimization requires further miniaturization via on-chip implementation, a task outside the scope of this work.

The dense layout of the rectifier is also designed to reduce the parasitic components in the PCB. Fast switching actions mean the waveforms contain high dv/dt and di/dt, thereby amplifying the influence of the parasitics within the circuit. The power stage components are placed to consider the following elements (listed in order of importance):

1. Each flying capacitor's proximity to its respective half-bridge silicon device.

2. Loop minimization for the traces set to carry i_{rec}.

3. The charging and discharging gate drive loops.

First, the flying capacitor proximity to each half-bridge is important because the capacitors are often switched in and out of the path of i_{rec}. Inductance between the switch

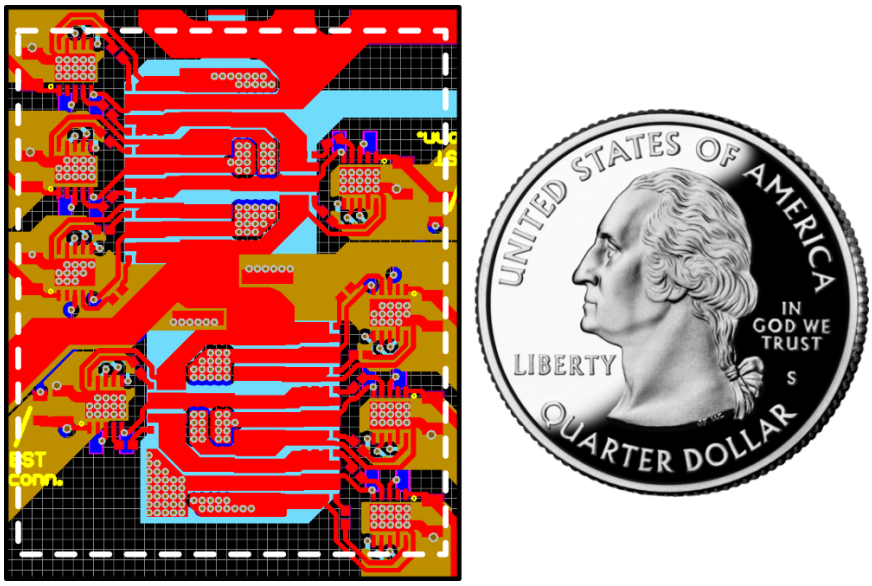


Figure 5.8: The PCB layout of the rectifier power stage with a US quarter for size reference. The white dotted line measures 31.4 mm x 27.5 mm.

node of a half-bridge and the capacitor being inserted causes large voltage spikes at the switching action. The parasitic inductance effectively disallows power current to flow for a small amount of time after a rectifier level change. When a large current is blocked, a large voltage develops, and these voltages manifest here as voltage spikes around the switching action. This parasitic is shown at the top of Fig. 5.9.

Second, the Loop minimization for the traces that carry i_{rec} is the next priority. A small loop size helps to reduce the parasitic inductance seen by i_{rec}. The magnitude of i_{rec} makes this parasitic important, as larger changes in current induce more voltage on an inductor. However, this is less important that the flying capacitor parasitic because the frequency content of i_{rec} is 150 kHz plus harmonics. The switching action associated with the flying capacitors is well-above the fundamental, and the fast insertion of a parasitic element influences the consequent voltage spikes. Here, inductance in the power path is non-ideal, but it is not being rapidly inserted into and out-of the power path, which makes reduction of these parasitics a lower priority. Another function of parasitic inductance in the power path is how it affects the coupling. This inductance sums with L_s, causing the effective coupling factor k to drop. Generally, this effect is minor because the parasitic is much smaller than the large value of L_s. The PCB pathing of i_{rec} within one phase leg is shown at the right side of Fig. 5.9.

Finally, the gate drive loops are considered in the layout. Minimizing gate inductance is valuable for reducing switching times, reducing ringing, and mitigating the risk of accidental triggering. Each gate signal is a fast switching signal and contains high frequency content. For this reason, the gate charge and discharge loops are small to reduce parasitic inductance.

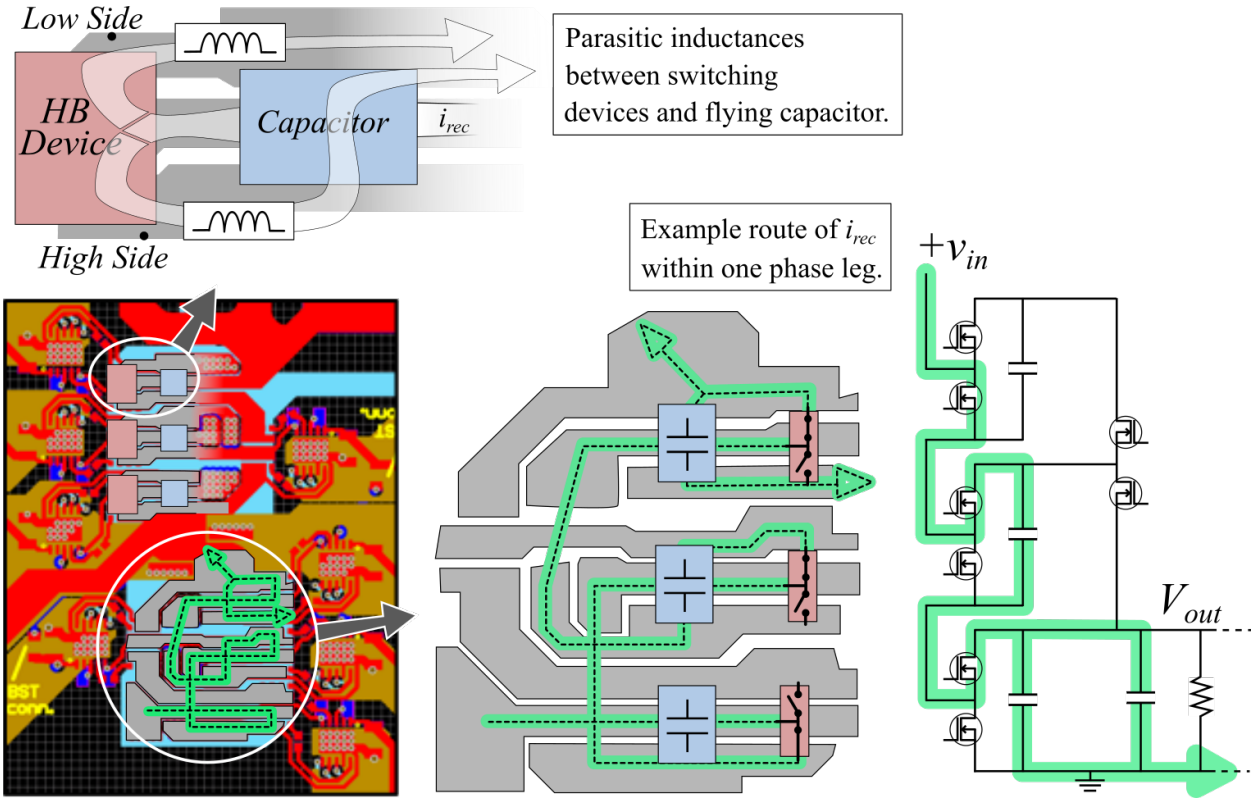


Figure 5.9: Example showing the characteristics of the power stage layout. The parasitic inductance between the switching devices and their respective flying capacitors are visualized in the upper graphic. The rightmost graphic shows an example of how the current path of i_{rec} flows through one phase leg of the PCB layout.

Furthermore, when possible, the gate traces are not placed in close proximity to any other traces associated with the power stage. This decreases their parasitic capacitance to other portions of the circuit and reduces the coupling affects between the power stage and the control circuitry. Coupling between the two can result in false triggering of the MOSFETs via a high-frequency voltage spike in the power stage.

The top of Fig. 5.9 illustrates where the main parasitic inductance manifests between the switching devices and flying capacitors. i_{rec} is diverted at the switch node through either the low or high side device. At the switching instant, i_{rec} must begin flowing through one of the parasitic inductances, causing high di/dt. The parasitic and consequent voltage spike are both kept small by the very tight layout. Fig. 5.9 also shows an example of how the circuit schematic translates to the PCB pathing. This example shows C_{x3} and C_{x2} inserted into the path of i_{rec}. Each portion of the conducting path on the PCB is laid out to be very tight so that the parasitic inductance and resistance on the green current path remain small. Here, significant inductance detunes the WPT tank, and any additional ESR causes loss.

To validate the effectiveness of the layout, the Altium PCB design is uploaded to Ansys Q3D software and analyzed for parasitic values. There are long, necessary traces that connect the rectifier to the WPT tank and to the DC load. These traces see resistances ranging from 1.1 to 4.95 $m\Omega$ and inductances from 8.85 to 16.11 nH. The rest of the layout (as pictured in Fig. 5.9 less two necessary jumper wires), have parasitic resistance values from 0.14 to 2.5 mΩ and inductances from 0.32 to 4.47 nH. The parasitics are very small relative to the device values of $6R_{dson} = 46.2$ mΩ and $L_{rx} = 13.26$ μH.

5.5 Waveforms

Fig. 5.10 shows the waveforms of the WPT system at $P_{out} = 16.97$ W. The two waveforms near the top are the rectifier input: v_{rec} and i_{rec}. The two bottom waveforms are the tank input (or inverter output): v_{inv} and i_{inv}. These waveforms are recorded with FPGA 1 driving both the rectifier and inverter. The switching times for both converters are set with the same system clock, and the entire WPT platform is running with the output unregulated in open loop. The output resistance is tweaked using an electronic load until the output voltage as required.

The operating point is taken with a DC input voltage of 15 V and a DC output voltage of 5 V. The DC currents at the input of the inverter and the output of the rectifier are recorded, and the DC-DC efficiency is calculated as 92.90 %. The oscilloscope waveform data shown in Fig. 5.10 has a sampling rate of 2.5 gigasamples/second. This data is exported onto a thumb drive and processed in MATLAB. The fundamental voltage, current, and impedance of the rectifier are calculated for comparison with the model. This operating point occurs at $|Z_{rec,1}| = 7.66\ \Omega$ and $\angle Z_{rec,1} = 25.36°$.

The waveform data is also evaluated for harmonic content. Fig. 5.11 shows the spectrum of waveform v_{rec} in Fig. 5.10. As expected when designing the modulation scheme to digitize a sinusoid, the 3$^{\text{rd}}$, 5$^{\text{th}}$, and 7$^{\text{th}}$ harmonics are significantly smaller than the fundamental component for v_{rec}. The attenuation of the first 3 harmonics is quantified by calculating the

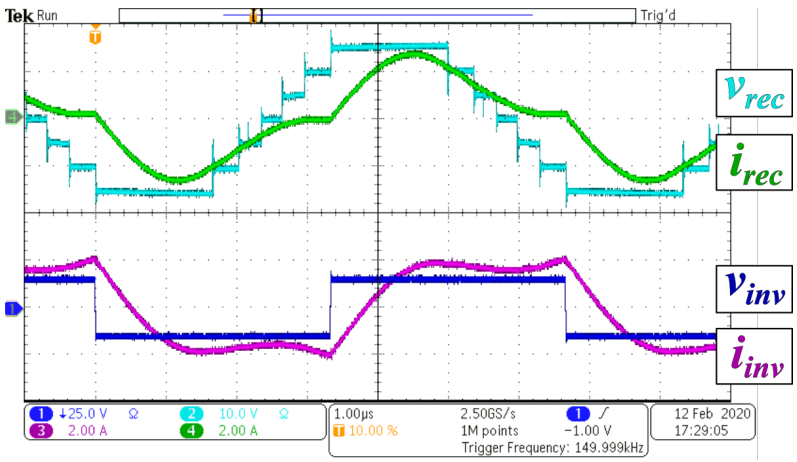


Figure 5.10: Waveforms at $P_{out} = 16.97$ W, $\angle Z_{rec,1} = 25.36°$, and $|Z_{rec,1}| = 7.66\ \Omega$.

total harmonic distortion (THD) of v_{rec}. The THD_i of a waveform is

$$\text{THD}_i(x) = 100 \cdot \frac{\sqrt{\sum_{n=2}^{i} x_n^2}}{x_1}, \tag{5.1}$$

where x_n is the RMS value of the i^{th} harmonic and x_1 is the RMS value of the fundamental component. The THD_7 accounts for the distortion through the 7^{th} harmonic of v_{rec} in Fig. 5.10 and evaluates to $\text{THD}_7 = 7.04\%$. Considering the full spectrum of v_{rec} returns $\text{THD}_\infty = 12.86\%$. The distortion is low in both cases, but it is especially low through the first few harmonics. A summary of the harmonic content in every waveform pictured in Fig. 5.10 is given in Table 5.4. The WPT tank exhibits significantly high harmonic content in all waveforms aside from v_{rec}.

Lastly, this operating point is compared to the state space model. The state space model is set up to run with the same switching times. The switching times of the inverter and rectifier voltages are implemented using a 150 MHz clock within the control FPGA, allowing for 1000 discrete edge times per fundamental period. In both the state space model and the experimental operating point, the rectifier and inverter voltage waveforms are triggered at 127 clock lengths apart ($\angle(v_{inv} - v_{rec}) = 45.7°$). The modulation index at this operating point dictates level changes at 23, 70, and 126 clocks (or $t_1 = 0.023 \cdot T_s$, $t_2 = 0.07 \cdot T_s$, and $t_3 = 0.126 \cdot T_s$). The waveforms of the experimental system and state space model are overlaid in Fig. 5.12 and show exceptional agreement, less the switching noise.

Table 5.4: Waveform Distortion in Fig. 5.10

	1^{st}	3^{rd}	5^{th}	7^{th}	THD $_7$	THD$_\infty$
v_{rec} [V]	16.97	0.97	0.73	0.20	7.04	12.86
i_{rec} [A]	2.22	0.51	0.11	0.06	23.81	23.99
v_{inv} [V]	19.01	6.33	3.79	2.71	41.36	48.23
i_{inv} [A]	2.12	0.57	0.15	0.08	27.96	28.15

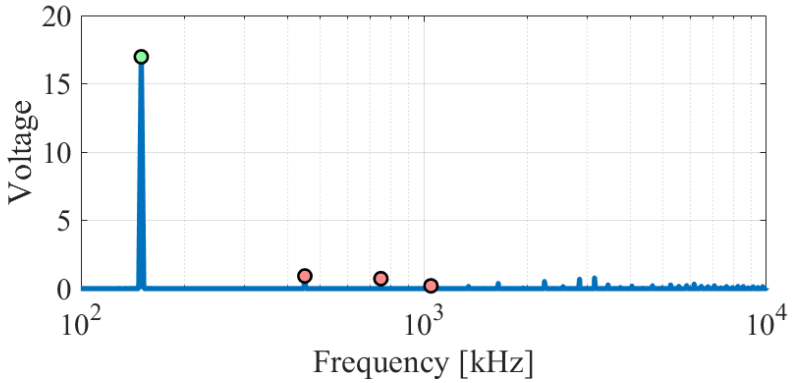


Figure 5.11: Low-harmonic spectrum of v_{rec} as pictured in Fig. 5.10. The fundamental component, and 3rd, 5th, and 7th harmonics are marked with colored circles.

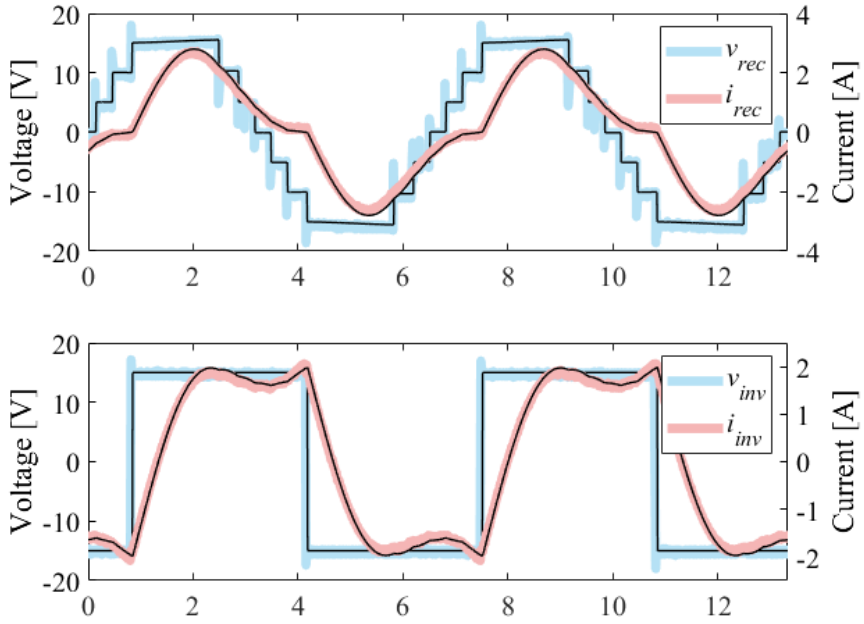


Figure 5.12: Experimental waveforms (color) overlaid with modeled waveforms (black) at $P_{out} = 16.97$ W.

5.6 Power Sweep - Model Comparison

A sweep of steady state points is performed to further illustrate the operation of the experimental platform. The coupling remains constant at $k = 0.773$ for all operating points. The switching times of the rectifier and the value of the electronic load are both edited for each test point. The resulting test points each occur at a different fundamental rectifier impedance, $Z_{rec,1}$, but all still meet the $V_{out} = 5$ V criterion. First, the fundamental circuit model is used to convey where the experimental operating points occur within the general operating space. Fig 5.13 shows the experimental points overlaid on the efficiency and power graphs of the fundamental model. Input voltage V_{in} is fixed at 15 V, so the operating space is traversed using rectifier impedance (varying modulation index and input phase angle). The trajectory of impedances is not the strict optimal, but it is near the highest efficiency trajectory based on the fundamental model of the WPT tank.

The experimental data is then compared point-for-point with the state space model including switching loss mechanisms. The switching times of the experimental waveforms are matched with the switching times of the state space model. Given no discrepancy between the efficiencies of the two platforms, the output resistance would be the same for both. However, small deviations in efficiency dictate that the experimental and modeled R_{load} values differ slightly to ensure that $V_{out} = 5$ V for both.

Each experimental point is again processed in MATLAB, and Fig. 5.14a contrasts the efficiencies of the experimental and modeled points verses output power. The experimental results almost exactly match the trend of the model in Fig. 5.14a, and the efficiency peaks

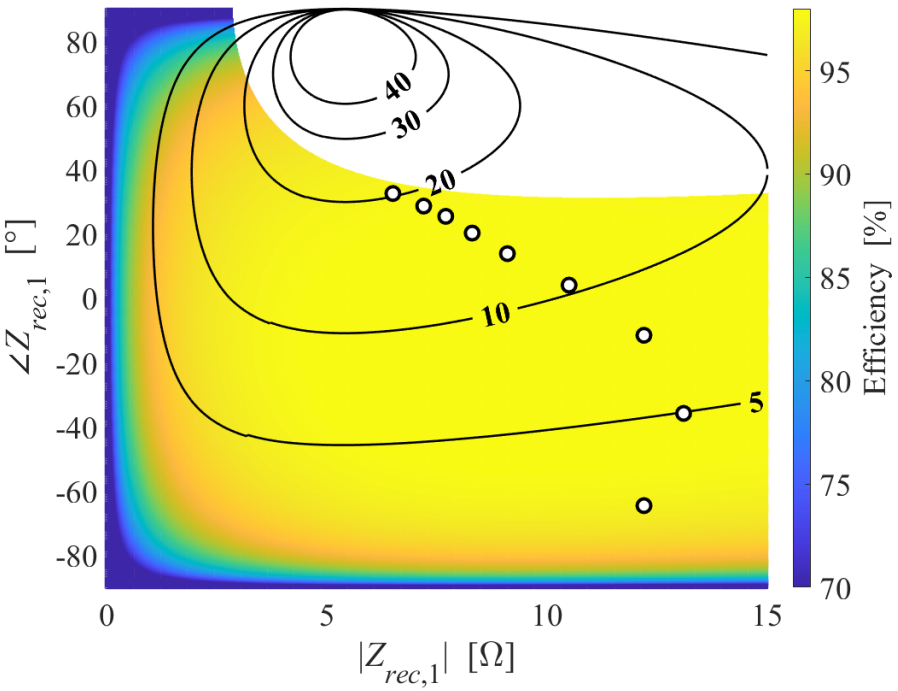
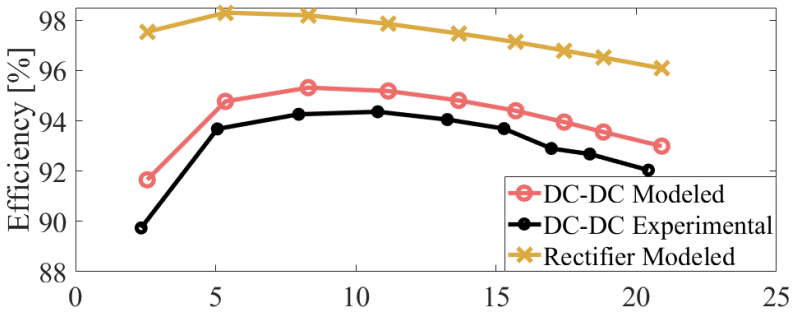
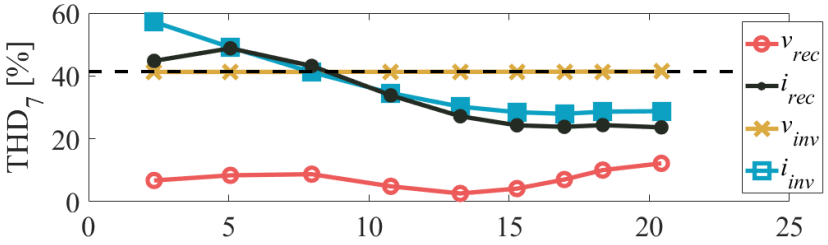


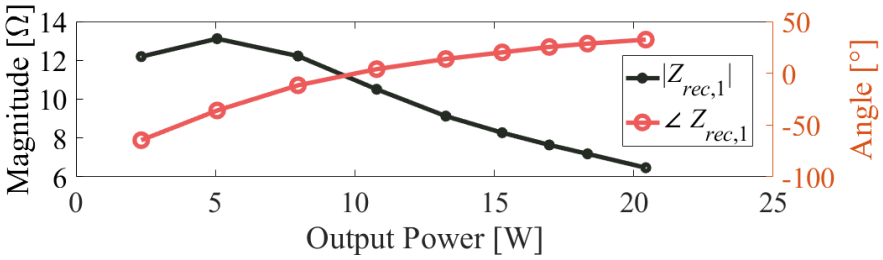
Figure 5.13: Experimental data points overlaid on fundamental model in terms of Z_{rec} to aid in visualizing how the rectifier is able to traverse the operating region. The white area denotes the space where the MSC cannot operate ($M > 3.81$), and the black lines are output power contours.



(a)



(b)



(c)

Figure 5.14: The experimental data points (a) compared to the (state space) modeled DC-DC efficiency, (b) in terms of distortion, and (c) in terms of the fundamental impedance. The black dashed line in (b) is the THD_7 of a square wave for comparison.

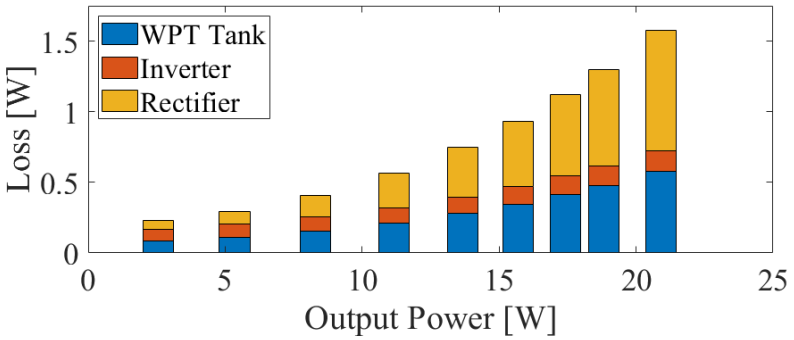


Figure 5.15: Loss distribution as predicted by the state-space-based model for the range of output powers from 2.47 W to 20.97 W.

around 10 W as predicted. However, the experimental results are lower than predicted by the model. The modeled rectifier efficiency is consistently high, but the accuracy of the rectifier model is in question given the discrepancies between the DC-DC modeled and tested.

Fig. 5.14c illustrates the same data as Fig. 5.13 but reduces a dimension, making it easier to interpret. Notably, Fig. 5.14b reports high levels of distortion. The v_{rec} waveform showcases low THD_7 due to the MSC rectifier's switching scheme, but the other three WPT tank waveforms are significantly distorted. While the distortion of the system is predicted by the state space model, the components are assumed to be linear. This assumption must be investigated in order to weigh the impact of harmonic content above the fundamental frequency.

5.7 Component Non-Linearities

Each circuit component is modeled as a single value, and the parasitic resistances are modeled at 150 kHz. These values are found as outlined earlier in Table 5.3, but here the impedance analyzer is once again used to find the harmonic ESR values of various components. The parameters that most significantly deviate from their 150 kHz ESR at higher frequencies are the tuned WPT tank, and the rectifier PCB board. Table 5.5 outlines the fundamental ESR value (150 kHz) as well as the 3^{rd} and 5^{th} harmonic ESR values. Especially for the WPT coils, the harmonic resistance is significantly larger than the fundamental resistance.

The datasheet of the 760308141 coil helps to explain the impedance analyzer measurement. The coils are designed for peak quality factor at the fundamental frequency, but

Table 5.5: Harmonic ESR Values

	ESR_1	ESR_3	ESR_5
R_p	78.6 mΩ	354.1 mΩ	924.3 mΩ
R_s	73.1 mΩ	356.9 mΩ	932.7 mΩ
R_{rec}	45.4 mΩ	54.4 mΩ	60.5 mΩ

Fig. 5.16 shows that the quality factor quickly falls off thereafter. Therefore, significant 3^{rd} and 5^{th} current components will cause additional loss according to the ESR_3 and ESR_5 values.

The experimental data is assessed again, but the higher harmonic ESR values are considered. After the full circuit model is computed, the harmonic components are calculated from the waveforms. The additional losses due to ESR_3 and ESR_5 are added to the loss profiles of the WPT tank and rectifier. The additional losses are calculated using $I_n^2(ESR_n - ESR_1)$, where n is the harmonic number and I_n is the RMS value of the n^{th} harmonic current. This results in six additional loss mechanisms: the 3^{rd} and 5^{th} primary current paired with R_p and 3^{rd} and 5^{th} secondary current with R_s and R_{rec}. The additional loss reduces the total output power, and the adjusted model is compared to the experimental results in Fig. 5.17. Including these losses results in a much more accurate efficiency prediction, and Fig. 5.17b illustrates just how much additional loss is contributed by ESR_3 and ESR_5. Here, the predicted rectifier efficiencies are bound from 96.1%-to-98.0%. These results validate the loss model of the WPT circuit and prove that coil non-linearities must be considered for this experimental setup.

5.8 SHE Modulated Experiments

Here, the observations concerning coil and PCB non-linearities are extrapolated even further. While approximating the efficiency by adding the harmonic loss to the end of the circuit model is sufficient, it is even better to avoid creating the waveform distortion to begin

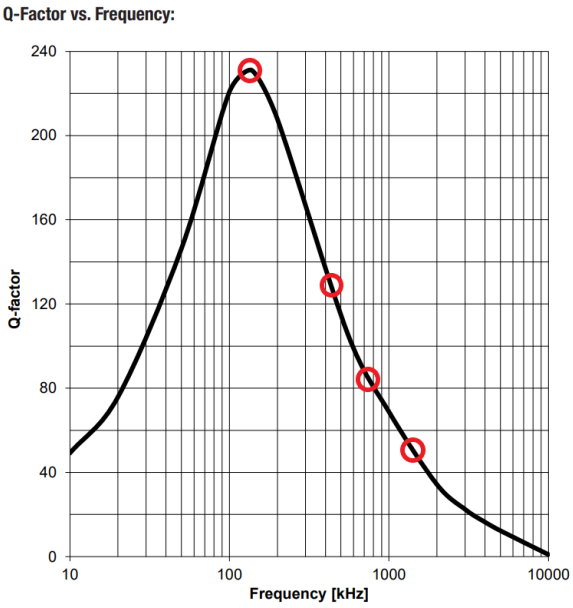


Figure 5.16: Quality factor of the WPT coils used on the primary and secondary sides [20]. The fundamental, 3^{rd}, 5^{th}, and 7^{th} are marked for reference.

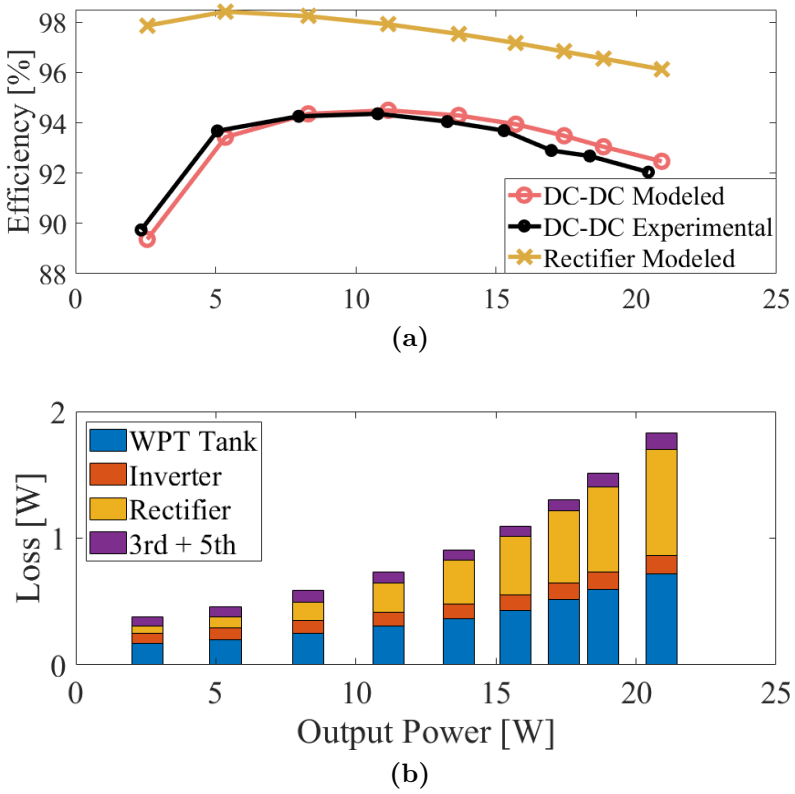


Figure 5.17: The (a) efficiency comparison and (b) loss distribution including an adjustment for additional harmonic loss due to component non-linearities. In Fig. 5.17b, the purple is the additional loss caused by ESR_3 and ESR_5

with. If the WPT waveforms have little distortion, then any device non-linearities become irrelevant.

The rectifier is well-suited to reduce distortion, but as shown in Fig. 5.14b, the other tank waveforms are highly distorted through the 7^{th} harmonic. To address this, the inverter is switched using selective harmonic elimination (SHE) [114]. The switching is implemented so that the 3^{rd}, 5^{th}, and 7^{th} components are attenuated. The switching scheme complements the harmonic attenuation of the rectifier input voltage and results in dramatically reduced distortion for the current waveforms as well.

Another experimental waveform example is shown in Fig. 5.18. The inverter has 12 level changes per period instead of the 2 within a square waveform. Therefore, the inverter has more switching loss compared to the previous experiment. Furthermore, the input voltage (V_{in}) is increased so that the fundamental component ($v_{inv,1}$) matches with the previous experiment. Aside from these two changes, the experiments are run in the same manner.

The resulting THD levels are much lower. Table 5.6 holds the harmonic content of each waveform shown in Fig. 5.18. The harmonic content of v_{rec} changes very little (comparing to Table 5.4 because the rectifier is modulated in the exact same manner as in the previous test. However, the distortion values of i_{rec}, v_{inv}, and i_{inv} are much lower. Each showcases a very small THD value through the 7^{th}, and the current waveform THDs are both 7.03% when including noise. The inverter voltage, however, still has significant distortion past the 7^{th} harmonic, which is to be expected given that the SHE modulation scheme is only designed to attenuate through the 7^{th}. The experimental and modeled waveforms are again compared and shown to have good agreement in Fig. 5.21.

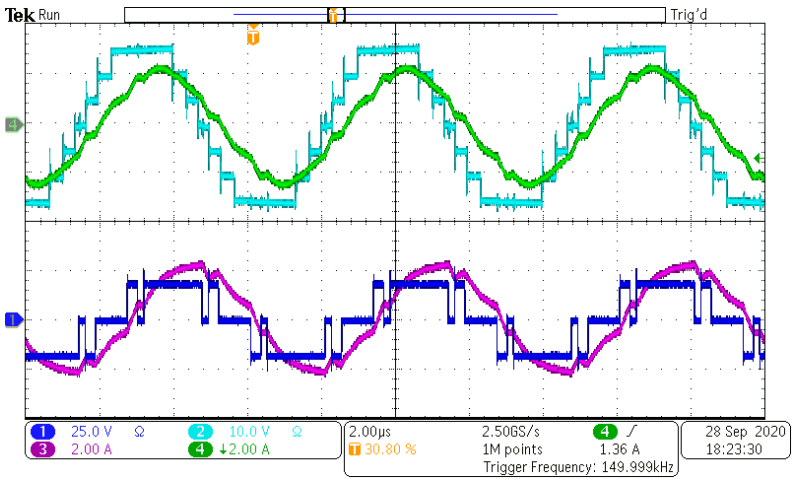


Figure 5.18: Experimental waveforms switched to reduce distortion at $P_{out} = 17.1$ W.

Table 5.6: Waveform Distortion in Fig. 5.10

	1^{st}	3^{rd}	5^{th}	7^{th}	THD $_7$	THD_∞
v_{rec} [V]	16.91	1.01	0.68	0.23	7.32	12.67
i_{rec} [A]	2.21	0.08	0.03	0.01	3.85	7.03
v_{inv} [V]	18.76	0.37	0.05	0.11	2.05	45.25
i_{inv} [A]	2.11	0.05	0.03	0.01	2.66	7.03

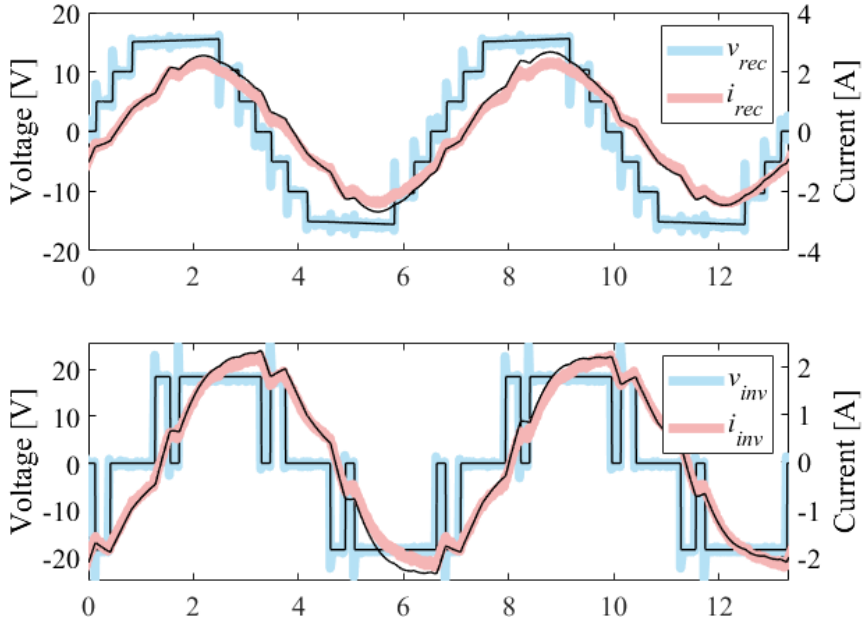


Figure 5.19: Experimental waveforms (color) overlaid with modeled waveforms (black) at $P_{out} = 17.07$ W.

The model is updated to include the additional switching actions of the inverter, and the modeled and experimental power sweeps are compared in Fig. 5.21. The efficiency predictions show exceptionally good agreement in Fig. 5.21a, and the distortion levels of the WPT tank are kept very low throughout the entire test in Fig. 5.21b. The rectifier efficiency predictions are bounded from 96.2% to 97.9%, and the highest value of THD_7 is found in v_{rec} at the highest power: 12.46%. This is because the modulation index is increasing with power as shown in Fig. 5.20, meaning that this high power test point is where v_{rec} most resembles a square wave. Fig. 5.21c shows virtually no additional loss due to the non-linearities of the tank at the 3^{rd} and 5^{th} harmonics. This not only validates the discussion from Section 5.7 but also suggests a compelling way to control a WPT system, given that the need for near-coil filtering is mitigated by the reduction in waveform distortion.

Finally, Fig. 5.22 shows a comparison between the square wave modulated results and the SHE modulated results. The experimental SHE modulated results incur higher switching loss and are therefore lower efficiency at low power. The higher switching loss is the combination of more switching actions and a higher DC bus voltage on the inverter side. Interestingly, the efficiencies are comparable, meaning that the difference between increased switching loss and decreased harmonic loss is small. This means that with the exact same hardware, modulating the primary side to marry the low distortion of the MSC rectifier, results in THD reduction without a significant drop in efficiency. This result is compelling by itself, but given the significant increase in switching loss, this also motivates the potential use of a multi-level inverter in future work (to reduce switching loss while hopefully maintaining reduced distortion).

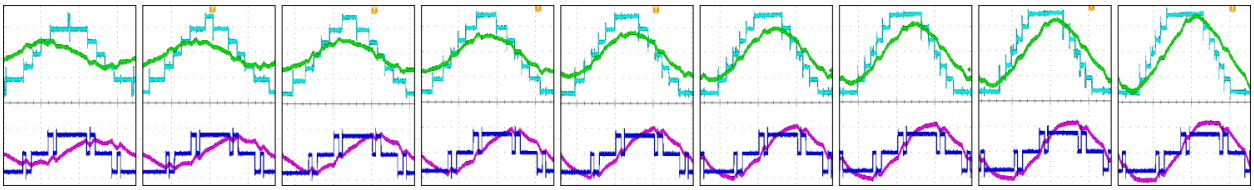


Figure 5.20: Waveforms of the low THD power sweep (from low to high power) using SHE modulation at the inverter.

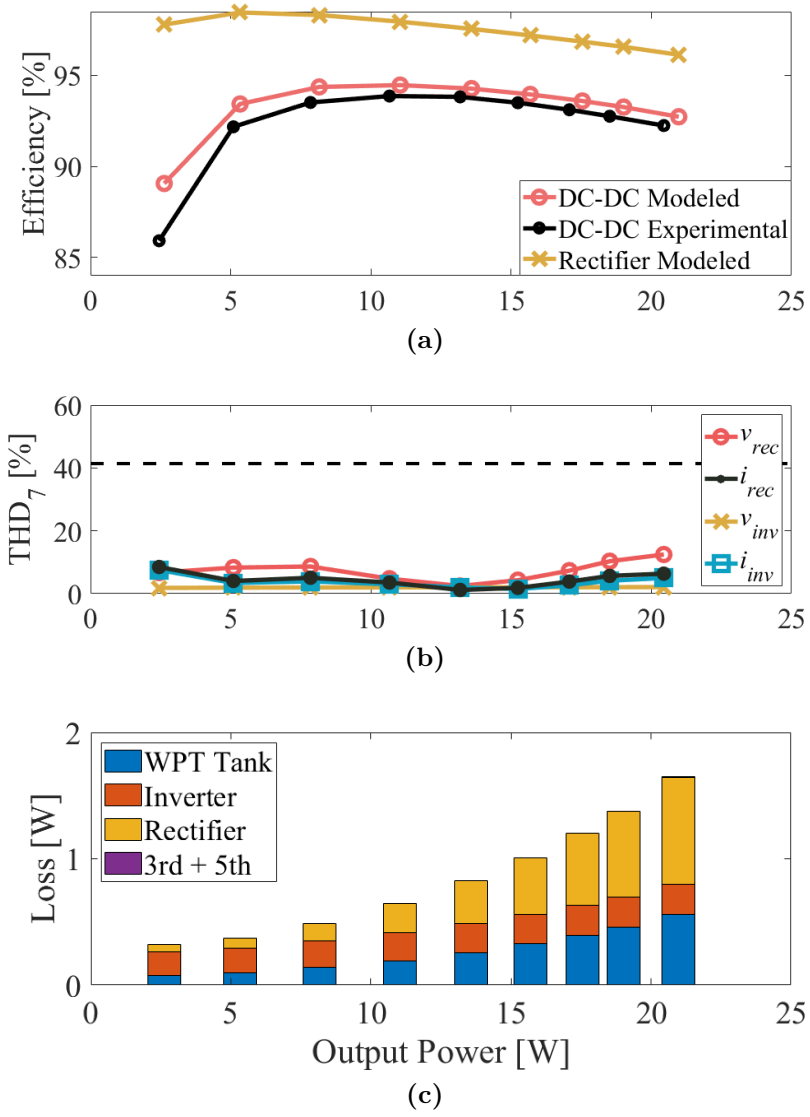


Figure 5.21: The (a) efficiency comparison, (b) distortion, and (c) loss distribution for the SHE modulated test set.

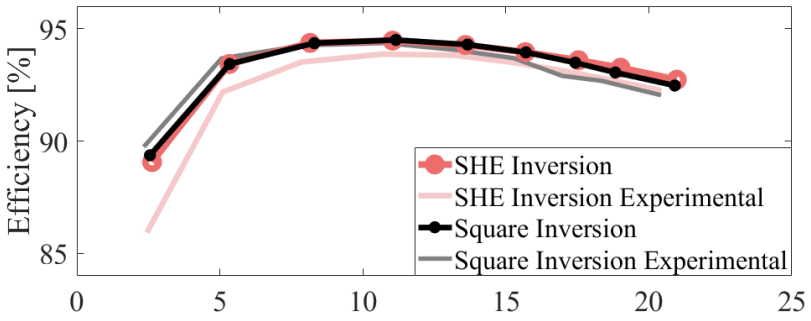


Figure 5.22: Comparison of experimental data sets with (a) inverter square wave modulation and (b) inverter SHE modulation.

Chapter 6

Discrete Time Modeling

The wireless power system must switch at a frequency that matches the carrier frequency. Furthermore, the 7-level rectifier is capable of varying its impedance to regulate the output voltage. Each of these requires a small signal model for the 7-level WPT system, and this chapter leverages the state space model derived in Chapter 4 to build the necessary transfer functions for each feedback control problem.

Active WPT rectification requires that the secondary circuitry sense the fundamental frequency generated by the transmitter and switch the rectifier at the same frequency. Phase lock loops (PLLs) are often leveraged for applications that require frequency synchronization [27, 103]. In wireless power, however, it is common to design for low synchronization bandwidth, thereby circumventing the need to consider the affect that the power stage has on the synchronization control loop [103]. In this chapter, the affect of the power stage is characterized, allowing the control loop to be stabilized at higher bandwidth. Furthermore, complete characterization of the plant is useful when establishing dual-loop

control wherein both the output regulation and frequency synchronization loops operate simultaneously. The output regulation loop is derived in the next section, followed by the novel linear projection technique applied to the frequency synchronization plant model.

6.1 Output Transfer Functions

The state space model is expanded to include small signal models of the WPT circuit in Fig. 4.6. First, the small signal state space representation of (4.17) is given by

$$\hat{x}[n+1] = N\hat{x}[n] + F_q\hat{t}[n], \quad [110] \tag{6.1}$$

where $\hat{x}[n]$ and $\hat{t}[n]$ are small variations around the state vector and interval times, respectively. Sample $[n+1]$ occurs after the n^{th}, and N is the natural response of the system, or how $\hat{x}[n]$ affects $\hat{x}[n+1]$. Likewise, F_q is the forced response of the system, or how $\hat{t}[n]$ affects $\hat{x}[n+1]$.

The natural response of the system is derived by leveraging the $e^{A_i t}x_0$ term in (4.28). This term describes how the current state vector affects the future state vector. Multiplying some state vector x_0 by $e^{A_i t_i}$ is equivalent to propagating x_0 through the undisturbed interval i for time t_i. The natural response matrix for the MSC WPT system is

$$N = \prod_{i=16}^{1} e^{A_i t_i}, \tag{6.2}$$

which describes the total change during one period by considering all 16 intervals through which the states must propagate.

The forced response matrix, F_q, measures the response to some perturbation in time, $\hat{t}$. Here, the perturbation in time is a control action that varies the durations of some intervals. Each rectifier switching edge can actuate to change either the on-time of that modulation level (1, 2, or 3) or the phase of the rectifier. The set of time perturbations that can potentially act on the system is $\{\hat{t}_{m1}, \hat{t}_{m2}, \hat{t}_{m3}, \hat{t}_p\}$. Fig. 6.1 aids in visualizing these control actions and where each occurs with respect to the steady state rectifier voltage.

For a phase shift perturbation to occur, each of the six switching actions within a half period must be actuated simultaneously. In Fig. 6.1, the six red arrows indicate how these control perturbations manifest. The zoomed in level change shows that the red right-to-left arrow manifests as an increases in the duration of interval II relative to the steady state point, X_{ss2}. Each of the modulation perturbations only requires two control actuations per half period. In Fig. 6.1, one level 3 actuation ($\hat{t}_{m3}$) is zoomed in, showing that the blue left-to-right arrow means the duration of interval I is increased. The other level 3 arrow is in the opposite direction, and it can be interpreted to mean that the duty cycle of that level is increasing or decrease as the level is modulated. For $\hat{t}_{m2}$ and $\hat{t}_{m1}$, the middle and top levels are modulated, respectively.

There is a different forced response matrix F_q for each time perturbation that acts on the system. The set of possible control actions is $q = \{m1, m2, m3, p\}$, and the correlated control perturbations are $\hat{t}_q = \{\hat{t}_{m1}, \hat{t}_{m2}, \hat{t}_{m3}, \hat{t}_p\}$. Therefore, the subscript in F_q indicates the type of control action: F_{m1}, F_{m2}, F_{m3}, and F_p. Deriving any of the F_q matrices requires that

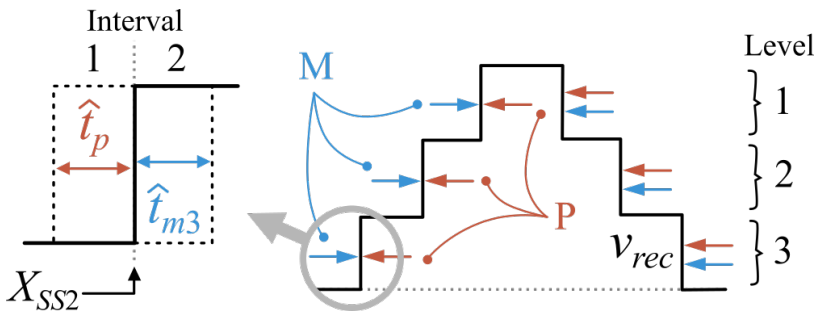


Figure 6.1: Modulation (M) and phase (P) type control actions around steady state v_{rec} resulting in time perturbations $\hat{t}_{mn}$ and $\hat{t}_p$, respectively.

the affect of each perturbation be accounted for and then propagated through the period. The change in the states is approximated by linearizing the state space equations around the steady state solution at the point of the perturbation. The linearized change in the state vector between intervals i and $i-1$ due to perturbation $\hat{t}_i$ is called Δx_{ssi}, and it is calculated by subtracting the final interval by the initial interval. The calculation is given by

$$\Delta x_{ssi} = \big(A_i X_{ssi} + B_i U\big)\hat{t}_i - \big(A_{i-1} X_{ssi} + B_{i-1} U\big)\hat{t}_i. \tag{6.3}$$

The same process is used for each perturbation within a given control action. There are a total of twelve $\hat{t}_p$ perturbations and four t_{m1}, t_{m2}, or t_{m3} perturbations within a period, depending on which control action is performed.

The change in the state vector must be propagated through the period in order to account for the affect that a single perturbation exerts on the next period ($\hat{x}[n+1]$). Δx_{ssi} must propagate through intervals $\{i, i+1, ...16\}$, and it can be represented mathematically by including the product of the relevant exponentials:

$$\Delta x_{di} = \left(\prod_{k=16}^{i} e^{A_k t_k} \right) \cdot \Delta x_{ssi}, \tag{6.4}$$

where Δx_{di} is the affect of Δx_{ssi} on the state vector at the end of the period. To find the forced response matrix, the affect of each perturbation must be included. For example, perturbations in phase and in modulation level one respectively yield

$$F_p = \sum_{k=1}^{16} \frac{\Delta x_{di}}{\hat{t}_i}, \tag{6.5}$$

$$F_{m1} = \sum_{k \in 8,16} \frac{\Delta x_{di}}{\hat{t}_i} - \sum_{k \in 2,10} \frac{\Delta x_{di}}{\hat{t}_i}. \tag{6.6}$$

Each control action returns F_p, F_{m1}, F_{m2}, and F_{m3}, each of which can be applied to

$$G_{xq} = (zI - N)^{-1} F_q, \quad [110] \tag{6.7}$$

which gives the transfer function from control-action to the states, written as the general term G_{xq}.

G_{xq} is an 11×1 matrix, each element of which is a transfer function from the control action q to the state at that index. Isolating the output voltage state, v_{Cout}, characterizes how the output is affected by a control perturbation:

$$G_{vq} = M_{iso7} \cdot (zI - N)^{-1} F_q. \tag{6.8}$$

M_{iso7} is a vector that isolates the 7^{th} index of the state vector (v_{Cout}) by zeroing all others. $M_{iso7} = [0\,0\,0\,0\,0\,0\,1\,0\,0\,0\,0]$ isolates the 7^{th} index, and in general $M_{isoN} = [0...0\,1\,0...0]$ isolates the N^{th} index. Transfer functions G_{vq} are the plant models to be used when designing the output regulation loop.

6.1.1 Example Transfer Function Derivation

As an example, the second level is modulated, and the transfer function G_{vm2} is derived. The $q = m2$ control actuation means that each edge of the second modulation level is perturbed.

For the operating point shown in Fig. 6.2, this results in actuation around steady state points X_{ss3}, X_{ss7}, X_{ss11}, and X_{ss15}. Therefore, the time perturbation $\hat{t}_{m2}$ is applied to the circuit four times during the period, and the four applications are labeled $\hat{t}_3$, $\hat{t}_7$, $\hat{t}_{11}$, $\hat{t}_{15}$ to coincide with the beginning of the steady state operating points as shown in Fig. 6.2. The linearized effects of these perturbations are calculated by applying (6.3) to each of these points. As an example, $\hat{t}_3$ is

$$\Delta x_{ss3} = \big(A_3 X_{ss3} + B_3 U\big)\hat{t}_3 - \big(A_2 X_{ss3} + B_2 U\big)\hat{t}_3. \tag{6.9}$$

Then, (6.4) is applied to each linearized state change. For example, the effect around steady state operating point X_{ss7} is

$$\Delta x_{d7} = \left(\prod_{k=16}^{7} e^{A_k t_k}\right) \cdot \Delta x_{ss7}. \tag{6.10}$$

Next, the effect of each perturbation through the end of the period is summed. The definition in (6.3) dictates that $\hat{t}_{ss3}$ and $\hat{t}_{ss11}$ occur backwards, thus they are subtracted

$$F_{m2} \quad = \quad \sum_{i\in 7,15} \frac{\Delta x_{di}}{\hat{t}_i} - \sum_{i\in 3,11} \frac{\Delta x_{di}}{\hat{t}_i} \quad = \quad \frac{\Delta x_{d7}}{\hat{t}_7} + \frac{\Delta x_{d15}}{\hat{t}_{15}} - \frac{\Delta x_{d3}}{\hat{t}_3} - \frac{\Delta x_{d11}}{\hat{t}_{11}}. \tag{6.11}$$

Finally, the transfer function describing how an increase in the conduction time of modulation level 2 affects the output voltage is

$$G_{vm2} = M_{iso7} \cdot (zI - N)^{-1} F_{m2}, \tag{6.12}$$

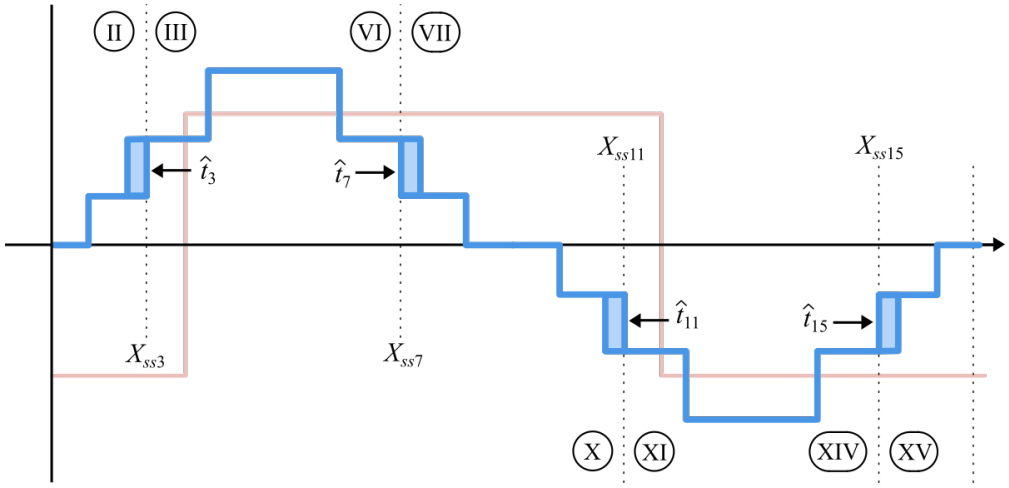


Figure 6.2: Perturbations for an increase in modulation level 2 (increase modulation level duration).

where, again, M_{iso7} isolates the index pertaining to v_{Cout}.

This process can be performed for any control action $q = \{m1, m2, m3, p\}$. Each resulting transfer function describes how a specific control action affects the output voltage (control-to-voltage), allowing a control loop to be designed that compensates for the affects of the WPT plant model. To accomplish frequency synchronization, however, the plant model must be expanded to include zero-crossing information. No state in the state vector inherently holds the information required to model the plant in terms of a control-to-phase transfer function.

6.2 Phase Transfer Functions

Frequency and phase regulation are accomplished by first sensing the power waveforms. A zero-crossing detector (ZCD) is placed across the secondary-side capacitor, C_s, and the resulting ZCD square wave is fed into the controller as a reference. The sensing strategy is discussed in detail in Section 6.5. In this section, the small signal model is designed with the experimental sensing strategy in mind, and the resulting transfer functions are derived to quantify the change in time of the zero-crossing event.

A small signal state space equation is written in a form that isolates the states at the zero crossing event, and it is

$$\hat{x}_z[n] = H\hat{x}[n] + J_q\hat{t}[n]. \tag{6.13}$$

The small signal variable $\hat{x}_z$ represents the change in the states at the steady state zero-crossing event, X_{ssz}, and this event occurs at the moment that the secondary side capacitance voltage crosses zero ($v_{Cs} = 0$). Equation (6.13) is similar to (6.1), but the result is within the current sample, $[n]$, instead of the next sample, $[n+1]$. Here, H and J_q describe the affect of $\hat{x}[n]$ and $\hat{t}[n]$ on $\hat{x}_z$, respectively.

Similar to (6.2) and (6.5), matrix H propagates the states through each interval, and matrix J_q considers the affect of each control perturbation. The difference, however, is that instead of accounting for the entire sampled period, either matrix only considers its respective mechanisms *up until* the zero-crossing event, X_{ssz}. Matrix H is given by

$$H = e^{A_z t_z} \cdot \prod_{i=i_z-1}^{1} e^{A_i t_i}, \tag{6.14}$$

where i_z is the interval within which the zero-crossing event occurs. A_z is the state matrix within interval i_z, and t_z is the time of the zero-crossing referenced to the beginning of interval i_z. The effect of each perturbation (Δx_{ssi}) is now propagated through the zero crossing event

$$\Delta x_{dzi} = e^{A_z t_z} \prod_{k=i_z-1}^{i} \left(e^{A_k t_k}\right) \cdot \Delta x_{ssi}, \tag{6.15}$$

meaning that matrix J_{m2}, for example, is

$$J_{m2} = -\Delta x_{dz3}, \tag{6.16}$$

because perturbation $\hat{t}_3$ is the only perturbation that occurs before X_{ssz} as shown in Figs. 6.2 and 6.3.

The transfer functions from control changes to the state variables at the zero-crossing event are

$$G_{xzq} = H(zI - N)^{-1}F_q - J_q, \tag{6.17}$$

the form of which is the general solution for a transfer function describing a state space output [110]. The state of interest is v_{Cs}, so the isolation vector is applied to give the relevant transfer function,

$$G_{vcszq} = M_{iso9}G_{xzp}. \tag{6.18}$$

The transfer function G_{vcszq} describes how voltage v_{Cs} changes at the steady state zero-crossing as a result of control action q. Fig. 6.3 shows this change as $\hat{v}_{Csz}$ for a change in modulation of the 2^{nd} rectifier level ($\hat{t}_{m2}$: $q = m2$).

For frequency synchronization, the goal is to define the relationship from a control action to the affected zero-crossing event, and in Fig. 6.3, the zero-crossing is changed by $\hat{t}_z[n]$. The slope of the steady state secondary capacitor voltage at the zero-crossing event ($\dot{v}_{Csz}$) is used as a linear projection to approximate $\hat{t}_z$ as a function of $\hat{v}_{Csz}$. State space equation (4.17) is used to find this slope

$$\dot{v}_{Csz} = M_{iso9}.\Big(A_z X_{ssz} + B_z U\Big), \tag{6.19}$$

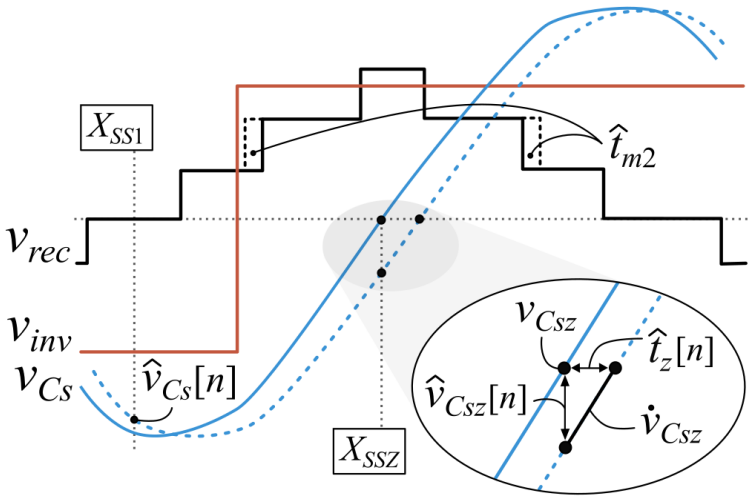


Figure 6.3: Steady state waveforms (solid) with a perturbation on level 2 ($\hat{t}_{m2}$) and the resulting change in v_{Csz}. The linear projection using the steady state slope, $\dot{v}_{Csz}$, gives the change in zero-crossing, $\hat{t}_z$.

and the final transfer function from control action q to the change in zero-crossing time $\hat{t}_z$ is

$$G_{zq} = \frac{\hat{t}_z}{\hat{q}} = \left(\frac{\hat{v}_{Csz}}{\hat{q}}\right)/\dot{v}_{Csz} = G_{vcszq}/\dot{v}_{Csz} = M_{iso9} \cdot \Big(H(zI - N)^{-1}F_q - J_q\Big)/\dot{v}_{Csz}. \quad (6.20)$$

Equations (6.13)-(6.19) culminate in (6.20) which gives a novel *time-to-time* transfer function. A more traditional transfer function example is the *time-to-voltage* transfer function in (6.8), where a control action (units of time) affects a state (units of voltage). Here, G_{zq} is useful to address the synchronization problem by characterizing how the switching actions of the plant affect the timing of the sensed control.

With four types of control actuation and two circuit characteristics being sensed, there are a total of eight transfer functions for the plant. These characterize how modulations of phase and each of the three v_{rec} levels affect both v_{Cout} and the zero-crossing of v_{Csz}. Table 6.1 summarizes the plant transfer functions that are used in designing the control loops in Section 6.4.

6.3 MATLAB Implementation

Chapter 4 explains how state space techniques are applied to the 7-level switched capacitor WPT platform. Table 6.1 summarizes the small signal plant models. For both models, there are practical implementation details that warrant explanation. First, the interval numbers between which the inverter voltage flips polarity are dependant on operating point. Instead of manually defining the interval time and orders, the code base is constructed to receive the

Table 6.1: Final Small Signal Plant Model Transfer Functions

	Sensed Circuit Characteristic	
Cntl. Action	Output Voltage, $\hat{v}_{Cout}$	v_{Cs} Zero-Crossing Time, $\hat{t}_z$
Phase, $\hat{t}_p$	$G_{vp} = M_{iso7}(zI - N)^{-1}F_p$	$G_{zp} = M_{iso9}\big(H(zI - N)^{-1}F_p - J_p\big)/\dot{v}_{Csz}$
Level 1, $\hat{t}_{m1}$	$G_{vm1} = M_{iso7}(zI - N)^{-1}F_{m1}$	$G_{zm1} = M_{iso9}\big(H(zI - N)^{-1}F_{m1} - J_{m1}\big)/\dot{v}_{Csz}$
Level 2, $\hat{t}_{m2}$	$G_{vm2} = M_{iso7}(zI - N)^{-1}F_{m2}$	$G_{zm2} = M_{iso9}\big(H(zI - N)^{-1}F_{m2} - J_{m2}\big)/\dot{v}_{Csz}$
Level 3, $\hat{t}_{m3}$	$G_{vm3} = M_{iso7}(zI - N)^{-1}F_{m3}$	$G_{zm3} = M_{iso9}\big(H(zI - N)^{-1}F_{m3} - J_{m3}\big)/\dot{v}_{Csz}$

modulation and phase times. The code base uses this information to build out the correct interval order, interval times, and correct state space matrices.

Next, steady state is calculated, and the output voltage is measured. The output voltage is determined by the modulation and phase times combined with the value of R_{load}. The former are declared by the user, so R_{load} is changed if the output voltage is wrong. In this case, the code base re-derives the state space matrices, re-solves for steady state, and checks the output voltage again. This iterative loop continues until the output voltage converges within tolerance, and the steady state operating point is located.

Now the interval order, interval durations, state space matrices, and steady state values are known by the code. Each of these elements plays a role in calculating the small signal models in Table 6.1, but the zero-crossing models must also know the interval during which the zero-crossing occurs. The code now scans the steady state operating point for the first zero-crossing of v_{Cs}, identifying both the zero-crossing interval and zero-crossing time.

The plant models defined in Table 6.1 require knowledge of the system to construct the appropriate coefficient matrices. Some matrices are simpler than others. For instance, the natural response matrix N is defined in MATLAB for all plant transfer functions as shown in Fig. 6.4a. It is simply the product of the $e^{A_i t_i}$ terms for each interval. Similarly, matrix H is defined in Fig. 6.4b, but it begins with the zero-crossing interval and propagates backward from there.

Matrices F_q and J_q are more complicated. On top of the interval order, times, state space description, steady state values, and zero-crossing information, these matrices require

```
% Natural Response Matrix.
N = 1;
for jj = fliplr(1:1:length(td))                    % From last interval to 1st.
    N = N * expm(topA(:,:,jj)*td(jj)); end         % propogate through "reverse" period.
```

(a)

```
% Output: Natural Response Matrix.
H = expm(topA(:,:,zint)*tz);                       % Zero-crossing interval eval'ed first.
for jj = fliplr(1:1:zint)
    if(jj~=zint) H = H*expm(topA(:,:,jj)*td(jj));  % Back to start of period.
    end; end
```

(b)

Figure 6.4: The (a) natural response matrix N and (b) natural response matrix for the output H as defined in MATLAB.

knowledge of each perturbation location and the direction of each perturbation. For F_q, the code iterates through each perturbation, finds the correct steady state value, calculates the linearized change in the states given the direction of the perturbation, and propagates through the rest of the period given for that specific perturbation. Finally, the effect of each perturbation is summed to return F_q. Fig. 6.5a shows this process executed in MATLAB for F_{m1}. Fig. 6.5b shows a similar process for J_{m1}, but the code only iterates over the perturbations that necessarily affect the states at the zero-crossing time, stopping any propagation after this point.

These matrices are compiled to form the eight transfer functions in Table 6.1. The high-level algorithm that drives the code base is outlined in Fig. 6.6. In summary, the modulation times, phase time, and output voltage are declared as inputs. The code builds the intervals and state space representations, combs values of R_{load} to find the desired value of V_{out}, locates the zero-crossing of v_{Cs}, and calculates each of the small signal plant models. This process is executed in under 5 seconds for a single operating point. The fast execution time for complete steady state and small signal descriptions of the 7-level WPT system is invaluable when designing.

6.4 Design of Isolated Control Loops

Looking at the output regulation and frequency synchronization control loops separately provides a good basis for understanding the entire control problem. Phase modulation is intended to control the frequency and phase synchronization, and the three level modulation

```
% Forced Response DUTY Matrix. (LVL 1)
Fd1 = zeros(size([Xss Xss]));
for ii = 1:1:length(inPair1(:,1))
    in1 = inPair1(ii,1); in2 = inPair1(ii,2);       % intervals b4+after perterbation.
    Xp = Xss_all(:,in2);                            % Xp is steady state op point.
    if(inPolD1(ii) == 1)                            % "1" is perturbation left to right.
        Ae = topA(:,:,in1); Be = topB(:,:,in1);
        As = topA(:,:,in2); Bs = topB(:,:,in2);
    else                                            % "0" is perturbation right to left.
        As = topA(:,:,in1); Bs = topB(:,:,in1);
        Ae = topA(:,:,in2); Be = topB(:,:,in2);
    end
    xd = ((eye(ns)+Ae)*Xp+Be*U) - ...                % state diff due to perterbation.
            ((eye(ns)+As)*Xp+Bs*U);
    Fdi1 = 1;                                       % initialize the multiplication.
    for jj = fliplr(in2:1:length(td))
        Fdi1 = Fdi1 * expm(topA(:,:,jj)*td(jj)); end
    Fd1(:,ii) = Fdi1*xd;                            % all propogated perturbations.
end
Fd1 = sum(Fd1,2);                                   % sum all propogated perturbations.
```

(a)

```
% Output: Forced Response DUTY Matrix. (LVL 1)
Jd1 = zeros(size([Xss Xss]));
rPIs = (inPair1(:,1)<zint); rPIs(rPIs==0) = [];     % Relevant perturbations that
rPair = [inPair1(rPIs,1) inPair1(rPIs,2)];          % ... affect tz in FC Model.
for ii = 1:1:length(rPair(:,1))
    in1 = rPair(ii,1); in2 = rPair(ii,2);           % intervals b4+after perterbation.
    Xp = Xss_all(:,in2);                            % Xp is steady state op point.
    if(inPolD1(ii) == 1)                            % "1" is perturbation left to right.
        Ae = topA(:,:,in1); Be = topB(:,:,in1);
        As = topA(:,:,in2); Bs = topB(:,:,in2);
    else                                            % "0" is perturbation right to left.
        As = topA(:,:,in1); Bs = topB(:,:,in1);
        Ae = topA(:,:,in2); Be = topB(:,:,in2);
    end
    xd = ((eye(ns)+Ae)*Xp+Be*U) - ...                % state diff due to perterbation.
            ((eye(ns)+As)*Xp+Bs*U);
    Jdi1 = expm(topA(:,:,zint)*tz);                 % initialize the multiplication.
    for jj = fliplr(in2:1:zint)                     % From pert to zero-cross interval.
        if(jj~=zint) Jdi1 = Jdi1*...
            expm(topA(:,:,jj)*td(jj));
        end; end; Jd1(:,ii) = Jdi1*xd;              % all propogated perturbations.
end
Jd1 = sum(Jd1,2);                                   % sum all propogated perturbations.
```

(b)

Figure 6.5: The (a) forced response matrix F_{m1} and (b) forced response matrix for the output J_{m1} as defined in MATLAB.

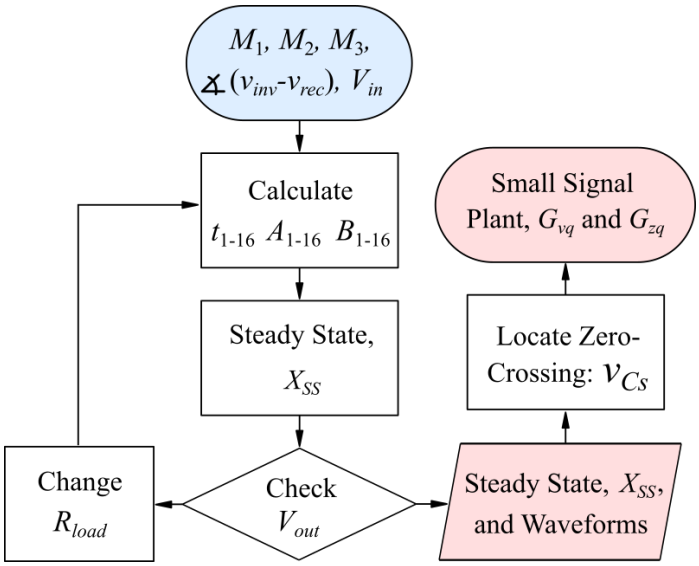


Figure 6.6: The high-level overview of how the code base calculates both the steady state power model and the small signal system model. Modulation, phase, and voltage inputs are converted into steady state values, waveforms, and small signal models.

is intended to control the output. In reality, either type of actuation will have an affect on the other control loop through the transfer functions in Table 6.1.

Here, these cross-coupling type affects are ignored and the loops are isolated as a starting point for control design. An example design is shown for each isolated control loop, and the control results are verified. The verification of each individual feedback loop validates the fundamental approach, laying the groundwork for the more complicated problem of dual-loop control in following sections.

6.4.1 Output Voltage Regulation

The 7-level rectifier is able to modulate any of its three levels during the half-period. The rectifier's modulation index is defined as $M = |v_{rec,1}|/V_{out}$, where $v_{rec,1}$ is the fundamental component of v_{rec}. The modulation index, M, represents the ratio between the output voltage and rectifier's input voltage, ranging from 0 to 3.81. As the fundamental model derivation showed, the rectifier's input impedance, Z_{rec}, is a function of M, which enables the MSC to tune the WPT circuit until the correct output voltage is established. An overview of the isolated small signal feedback loop that dictates this relationship is shown in Fig. 6.7.

Because the three rectifier levels can be individually actuated, each is individually considered via G_{vm1}, G_{vm2}, and G_{vm3} before they are all added together to represent the total change in output voltage, $\hat{v}_{out}$. Adding the affect of each level is acceptable only because the small signal system is modeled as linear, time-invariant (LTI). The small signal gain of

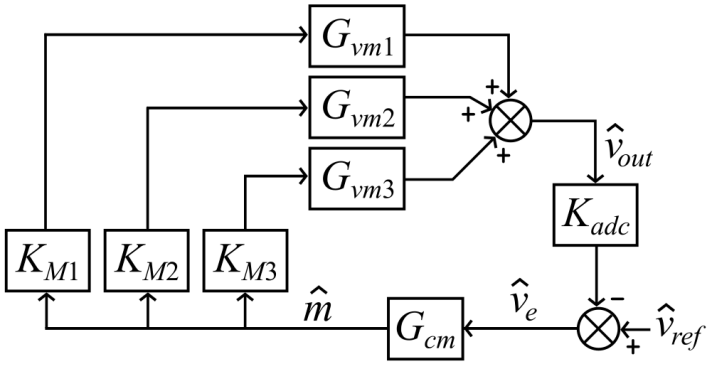


Figure 6.7: The control loop for output voltage regulation isolated from the rest of the system.

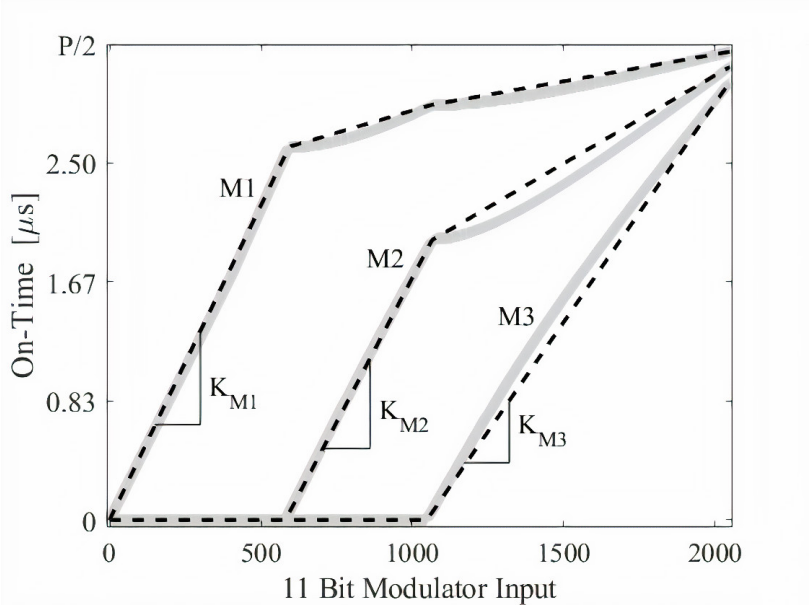


Figure 6.8: Modulation scheme of the 7-level switched capacitor rectifier. The input is 11 bit, and the output is the on-time of each level (solid lines) ranging from 0 seconds to half the period ($P/2$). The small signal gains of the modulator are approximated using the linear slopes shown by the dotted lines.

the analog-to-digital converter (ADC) includes a resistor divider as well as the 11 bit, 3.3 V referenced device: $K_{adc} = (1/2) \cdot 2048/3.3$.

The reference ($\hat{v}_{ref}$), compensator (G_{cm}), and modulators (K_{M1}, K_{M2}, and K_{M3}) are all implemented digitally. The input to the modulators is an 11 bit variable (range: 1 to 2048), and the modulators output the PWMs that control each rectifier level. The modulation scheme that maps the 11 bit input to the on-time of each level is seen in Fig. 6.8 where $M1$, $M2$, and $M3$ are the half-period on-times of each respective level. The approximated small signal gains of the three modulators are computed using the linear approximations shown by the dotted lines. Note that the values of K_{M1}, K_{M2}, and K_{M3} each change as the steady state operating point lies within one of three regions. Fig. 6.8 represents the modulation from input to output as [11 bit]-to-[on-time]. This is for visualization purposes alone, and gains K_{M1}, K_{M2}, and K_{M3} are actually mathematically defined based on the approximated slopes for the relationship [11 bit input]-to-[switching time]. Functionally, the model remains the exact same, but coherence with the plant models requires that the modulator gains be defined in terms of switching time, not modulation duration.

The total loop gain of this isolated control loop is given by

$$T_{out} = K_{adc} G_{cm} \big(K_{M1} G_{vm1} + K_{M2} G_{vm2} + K_{M3} G_{vm3} \big). \tag{6.21}$$

6.4.2 Phase and Frequency Synchronization

A PLL is used in order to stably synchronize the switching frequency of the rectification stage to the carrier frequency present by the primary side. Additionally, a discrete time model and a linear projection method describe the synchronization dynamics of the power stage. In this section, the frequency synchronization loop is analyzed and designed in isolation, demonstrating the correctness of both the discrete time plant model and the larger control loop implementation when incorporating the plant model.

The frequency synchronization control scheme is shown in Fig. 6.9, where the phase-frequency detector (PFD), compensator (comp), and digitally controlled oscillator (DCO) make up the PLL. The zero-crossing detector measures the secondary-side capacitor voltage, v_{Cs}, and reports the zero-crossings with rising and falling edges, thereby creating a square wave signal that describes the WPT carrier frequency, f_{wpt}. The PFD compares this signal to the output of the PLL (f_{pwm}) and generates a 3-level signal containing information about the two signals' phase difference. This phase difference is compared to a reference, an error is generated, and the compensator evaluates the error to drive the DCO. The output of the DCO is sent to both the power circuit to drive the PWM signals and to the input of the PLL for phase comparison. The PFD, summation, compensation, and DCO blocks are all implemented digitally inside the controller.

Fig. 6.9 is converted to a small signal model and shown in Fig. 6.10. The DCO changes its oscillation frequency by adding or subtracting clocks to change its period length. Therefore, the gain K_{dco} is the derivative at the steady state operating point: $K_{dco} = f_{clk}/N_{clks}^2$ where

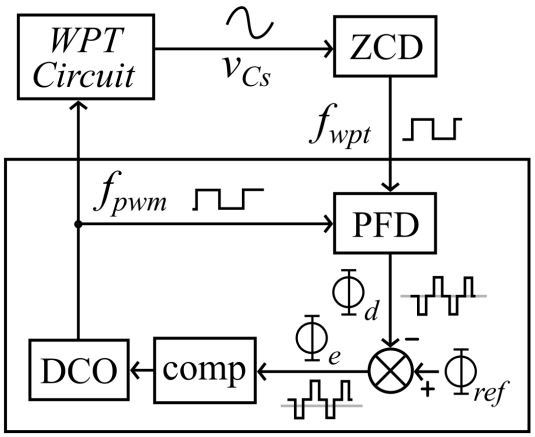


Figure 6.9: Block diagram of the control circuitry responsible for synchronizing the rectifier switching frequency, f_{pwm}, to the WPT carrier frequency, f_{wpt}.

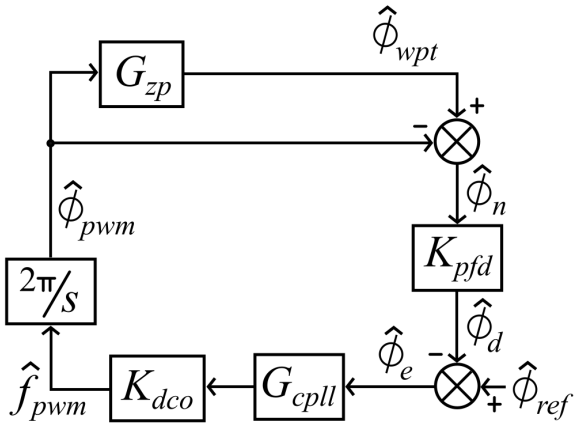


Figure 6.10: Small signal representation of the frequency synchronization control loop.

f_{clk} is the clock frequency and N_{clks} is the number of clock periods at the steady state operating point.

Understanding how the phase-frequency detector is converted into a small signal model is more complicated. First, K_{pfd} is a constant gain given by $N_{clks}/2\pi$, which just converts from units of radians to units of clock edges. Next, the $2\pi/s$ block converts the frequency content of the f_{pmw} square wave in Fig. 6.9 to phase information given by ϕ_{pwm}, for comparison with ϕ_{wpt}.

The way the discrete time plant model is derived means that both the zero-crossing detector and the conversion from f_{wpt} to ϕ_{wpt} are encompassed in G_{zp}. Furthermore, although G_{zp} is previously explained as a *time* input to *time* output transfer function (for consistency with the other plant model derivations), the exact same model of G_{zp} can be used as a *phase-to-phase* transfer function because $\hat{t}_z/\hat{t}_p = \hat{\phi}_z/\hat{\phi}_p$. Therefore, the plant model, ZCD, and PFD are all accounted for within the G_{zp}, $2\pi/s$, summation, and K_{pfd} blocks.

The total loop gain of the small signal model in Fig. 6.10 is

$$T_{freq} = K_{pfd} G_{cpll} K_{dco} \frac{2\pi}{s}\big(G_{zp} - 1\big), \tag{6.22}$$

where G_{cpll} is designed so that the control loop is stable.

6.5 Zero-Crossing Detector

The small signal representation of the frequency synchronization control loop requires the zero-crossing information of the secondary-side tuning capacitance voltage, v_{Cs}. Thus far, the assumption has been that the plant model simply has access to this information, but in reality the prototype platform requires a physical sensing circuit to retrieve the zero-crossing information in a reliable way to inform the controller.

6.5.1 Prototype Implementation

The experimental sensing circuit topology is shown in Fig. 6.11. The large capacitors labeled C_{DC} are used to block any DC that may try to flow through the WPT tank to ground. Resistors R_{DC}, R_1, and R_2 are used to step-down the voltage for the comparator circuit. A 2.5 V DC bias is placed at the comparator inputs by $R_{DC} = R_2 = 976\ \Omega$. This keeps the signals from clipping on the internal diodes connected to the rails of the comparator.

Because they are in parallel, R_{DC} and R_2 set the voltage division ratio with R_1 to be $488/(488+5110)$, or a multiplier of 0.087. The comparator is part number LTC6752HMS8-2 by Analog Devices and has an input voltage rating of 5 V. The divider ratio means that voltages up to 57 V relative to ground are safe at either end of C_s. Given that C_s is balanced in the prototype, the power capacitance being sensed is actually $2C_s = 223.5$ nF as shown in Fig. 6.11. With this capacitance value and a fundamental of 150 kHz, approximately 12 A can flow through the secondary side before the sensing circuit is overvoltaged. Finally, C_{fil}

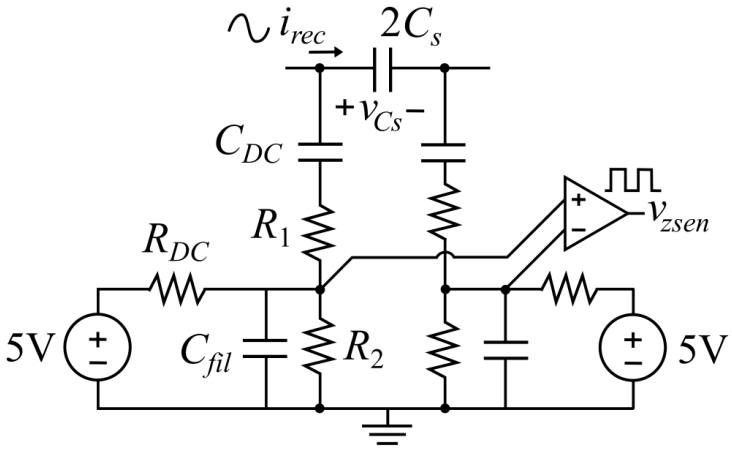


Figure 6.11: circuit diagram

Table 6.2: Values of Sensing Circuit

C_{DC}	R_1	R_2	R_{DC}	C_{fil}
10 μF	5,110 Ω	976 Ω	976 Ω	22 pF

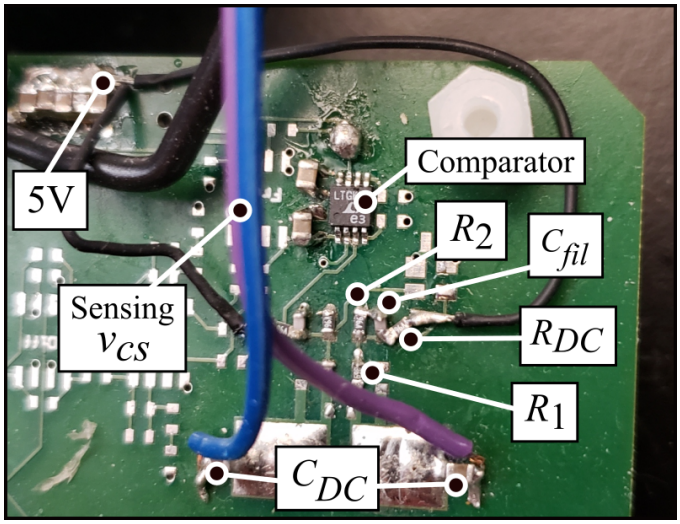


Figure 6.12: ZCD as implemented on the prototype PCB.

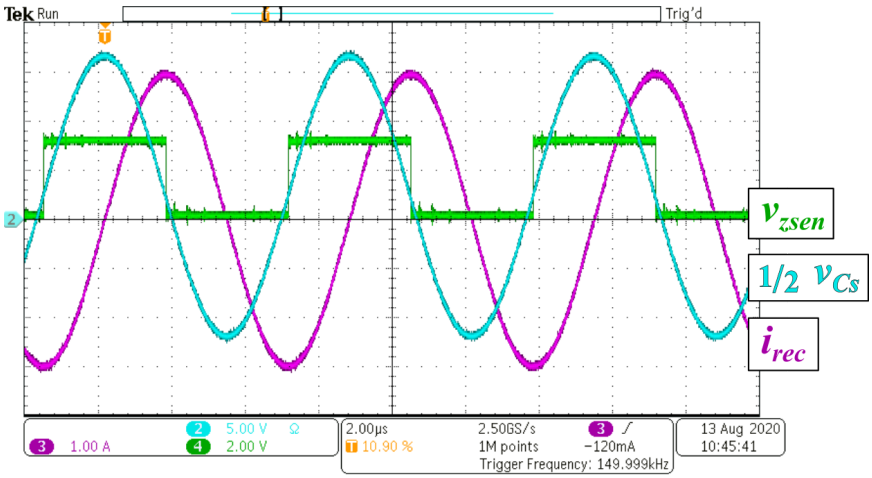


Figure 6.13: Example waveforms showing the sensing circuitry function: v_{Cs}, i_{rec}, and v_{zsen}.

is a small filter capacitor chosen to eliminate noise without causing significant phase shift between v_{Cs} and v_{zsen}. The values of the sensing components are given in Table 6.2.

Fig. 6.12 shows the sensing circuit implemented on the PCB. The capacitor $2C_s$ has jumper wires that run to the sensing circuit and connect to the two C_{DC} capacitors. The filtering circuit informs the comparator chip, and the comparator chip outputs v_{zsen} to the control FPGA via PCB traces. The secondary current (i_{rec}), sensed capacitor voltage $1/2v_{Cs}$, and the output of the comparator, v_{zsen}, are shown in Fig. 6.13. The sensor identifies the zero-crossings well without significant phase delay between v_{Cs} and v_{zsen}, and it even compensates for the small amount of DC offset shown on $1/2$ v_{Cs} in Fig. 6.13.

6.5.2 Small Signal Representation

Experimentally, the sensing circuit is implemented as a "stand-alone" unit. Basic open-loop operation is possible with or without the physical sensing circuit present. However, the feedback model does not recognize the sensor as an independent entity but sees it absorbed into the model of the power circuit. The small signal plant model outputs the change in zero-crossing time, $\hat{t}_z$. This is actually the output of the sensing circuit. A block diagram of the control loop (the PLL and modulator are implemented digitally) is shown in Fig. 6.14, and the red dotted line shows the small signal power stage model derived earlier in this chapter. A change in the rising and falling edges of v_{zsen} is equivalent to a change at $\hat{t}_z$ in the small signal domain. The figure illustrates how the plant model accounts for the zero-crossing detector.

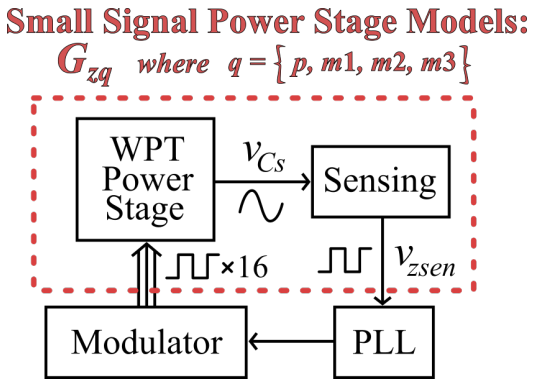


Figure 6.14: Basic frequency synchronization loop with showing the plant model absorbing the zero-crossing detection circuit.

6.6 Simulation Platform

A simulation of the feedback control loops is useful for characterizing and validating the control systems presented in this section. Given that MATLAB is used to manipulate the state space matrices and build the power waveform model, Simulink is a powerful and convenient tool for the control portions of this work. The state space model for the circuit is imported into Simulink, and non-linear items like sensing, clock functionality, and ADC quantization are incorporated. Both the output voltage regulation and frequency synchronization control loops can be simulated either in isolation or in tandem.

Fig. 6.15 shows the simulation as constructed in Simulink and describes each portion. The light red segments are the state space circuit model. The inverter and rectifier blocks read their respective inputs and set the values of the state space matrices accordingly. The circuit simulation block takes the state space information, solves $\dot{x}$, and linearly projects the state values for the small, fixed time-step. The state information is fed to both control loops.

The green control loop at the bottom of Fig. 6.15 is the output voltage regulation loop. The output voltage (state: v_{Cout}) is sent to a voltage divider and then an ADC where it is quantized and converted to a digital value. The digital value is compared to the voltage reference, and the digital error signal is sent to the compensator. The output of the compensator feeds the modulator, which is built into the red rectifier simulation block in this model. The startup handler is only active while the circuit voltage is growing because the required loop gain is inverted until a high enough power level is achieved. The startup

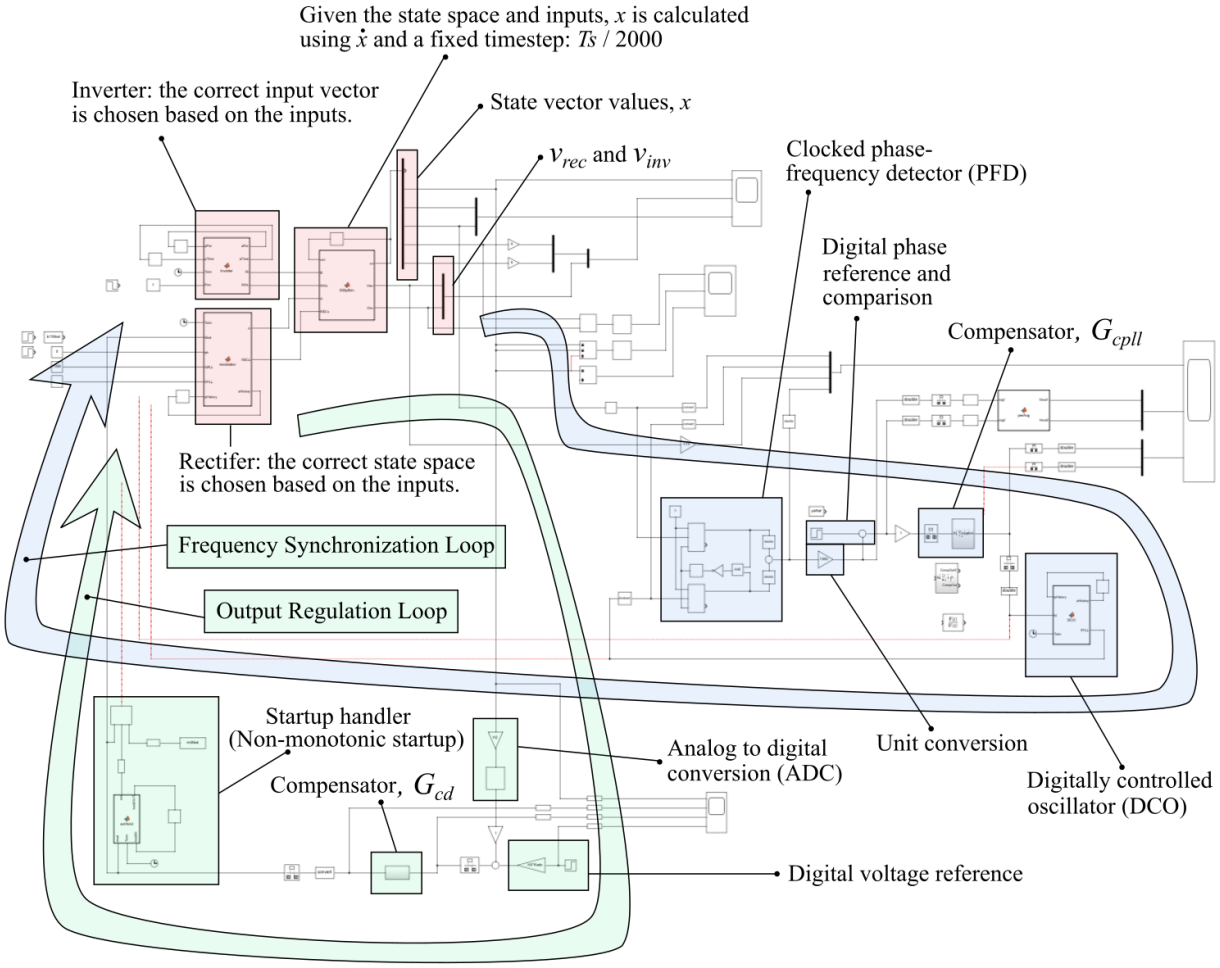


Figure 6.15: Simulink control simulation. The file can be executed with either loop working in isolation or with dual-loop functionality. The effect of non-linearities like clock-edge execution, quantization, and limited control resolution can be investigated using this model.

block clamps the modulation until the gains are correct and thereafter acts only as a short within the output regulation loop.

The blue control loop at the right of Fig. 6.15 is the frequency synchronization feedback system. The secondary capacitor voltage (state: v_{Cs}) is fed into the phase-frequency detector. The PFD uses two D-flip-flops, some logic blocks, and a delay, all clocked at the same frequency of the experimental platform. The 3-level output of the PFD (1,0,-1) is multiplied by 1000 as a unit conversion to clock edges before comparison to the digital phase reference. The output of the difference block is the error signal to be fed into the compensator, which informs the digitally controlled oscillator with the number of clock edges required. The DCO generates a square wave signal that coincides with the number of edges, and both the number and square wave are sent to the modulator. The modulator (embedded in the rectifier block) uses this information to assign PWM signals to the rectifier, closing the loop.

The Simulink model allows the control schemes to be tested prior to experimental investigation and enables no-risk consideration of non-idealities and loop-interactions. The simulation is utilized for validation of the isolated synchronization loop design, but it is used more extensively for the investigating dual-loop functionality.

6.7 Validation of Isolated Control Loops

The experimental setup from Chapter 5 is used to validate the solutions to each isolated control loop. Here, an intermediate operating point is chosen using a different WPT tank than was presented in Chapter 5. Otherwise, the same experimental platform is used to

validate the designs put forth for each isolated control loop. The tests are performed according to the system description given in Table 6.3. The prototype platform incorporating the second WPT tank is shown in Fig. 6.16 and has parameter values according to Table 6.3.

6.7.1 Isolated Output Regulation

Fig. 6.17 shows a bode plot of the uncompensated loop gain, the compensator, and the final loop gain after a compensator is designed for the output regulation loop. The loop gain has a crossover frequency of $f_{c-out} = 2.99$ kHz and a phase margin of $\phi_{m-out} = 64.4°$. The discrete time model is accurate well-past a crossover frequency of 2.99 kHz, but Fig. 6.17 shows the plant model has a phase roll-off around 10 kHz. This phase roll-off is consequent of a right-half-plane zero in the plant, and for this reason, the control bandwidth is significantly restricted. The discrete time model of the WPT system provides the insight necessary to quantify and predict this phase roll-off.

The compensator is designed in the z-domain using only powers of 2 so that the corresponding math can be easily handled by the digital controller. The discrete compensator is tested in Simulink using delay blocks, and upon successful implementation, it is exported into a VHDL code segment using a MATLAB add-on. The code segment is uploaded to the FPGA, and the designed compensator is

$$G_{cm} = \left(\frac{z^{-1}}{1-(1-2^{-5})z^{-1}}\right)\left(\frac{-2^{-15}z^{-1}}{1-z^{-1}} + \frac{2^{-9}z^{-1}}{1-(1-2^{-7})z^{-1}}\right). \tag{6.23}$$

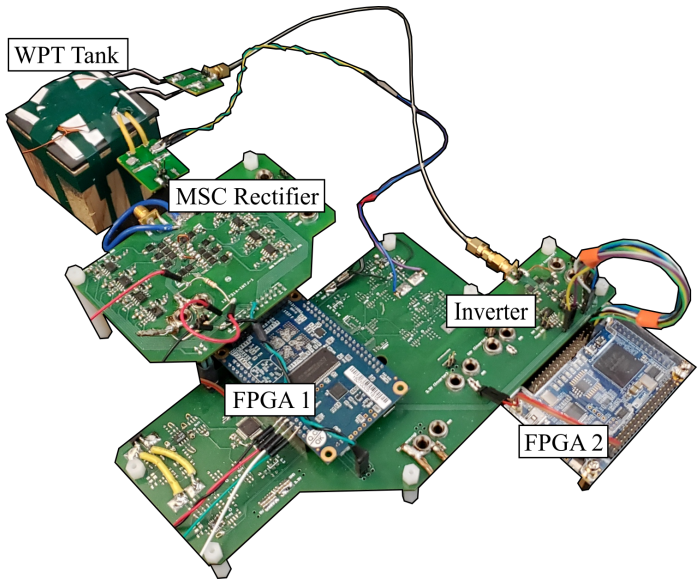


Figure 6.16: Experimental setup with a different WPT tank than is presented in Chapter 5.

Table 6.3: Operating Point Used to Validate Isolated Loop Designs

V_{in}	V_{out}	Φ_{ref}	t_1	t_2	t_3	P_{out}	η
10 V	2 V	$-67.7°$	5.25 %	16.2 %	30.0 %	4.54 W	84.12 %
R_p	C_p	L_{tx}	R_s	C_s	L_{rx}	k	
155 mΩ	221 nF	10.78 μH	390 mΩ	95 nF	12.11 μH	0.50	

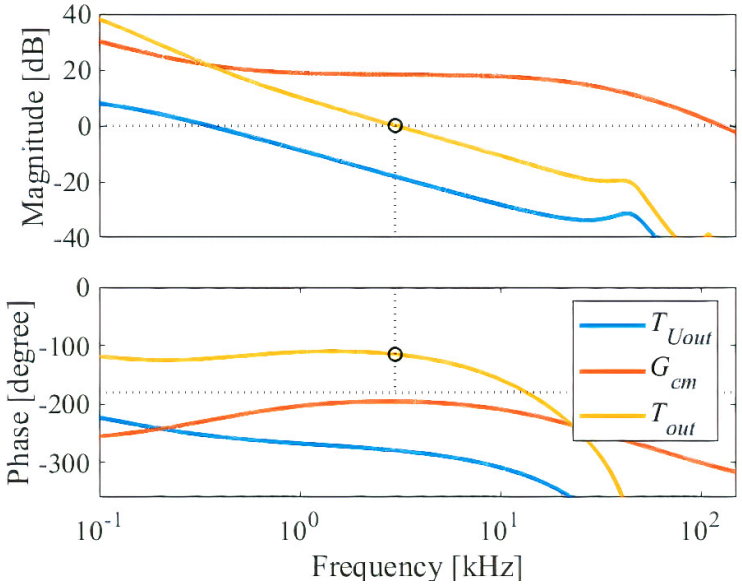


Figure 6.17: Plot of the uncompensated loop gain (T_{Uout}), compensator gain (G_{cm}), and loop gain (T_{out}).

In order to test the closed-loop design, the inverter and rectifier are both driven by the same controller so that no feedback is needed for frequency synchronization, isolating the output regulation control loop. The control scheme references two different operating clocks. The compensator is built for a 20 MHz clock, and the modulator works with a 150 MHz clock, thereby setting the modulation resolution to 1000 steps per fundamental period.

Due to the digital implementation, creating a step-change in the voltage reference is a simple clock-edge command that triggers $V_{ref} = 616$ to change to $V_{ref} = 596$. This 20 integer difference in V_{ref} is equivalent to a -0.0645 V change in the steady state operating point.

Fig. 6.18 shows the experimental result of the reference step and compares it to the small signal prediction. The experimental data is smoothed to help in visualizing the comparison. The test demonstrates good agreement with the model, showing that the methods used for the isolated voltage control loop are accurate.

6.7.2 Isolated Frequency Synchronization

The compensator is designed in the same manner as G_{cm}, relying on a known digital clock frequency and powers of 2 for easy implementation. G_{cpll} is

$$G_{cpll} = \left(\frac{2^{-21}}{1 - z^{-1}}\right)\left(\frac{2^{-11}}{1 - (1 - 2^{-8})z^{-1}}\right). \tag{6.24}$$

This gives a loop crossover frequency of $f_{c-freq} = 7.08$ kHz and a phase margin of $\phi_{m-freq} = 58.6°$. The compensator and final loop gain are shown in Fig. 6.19.

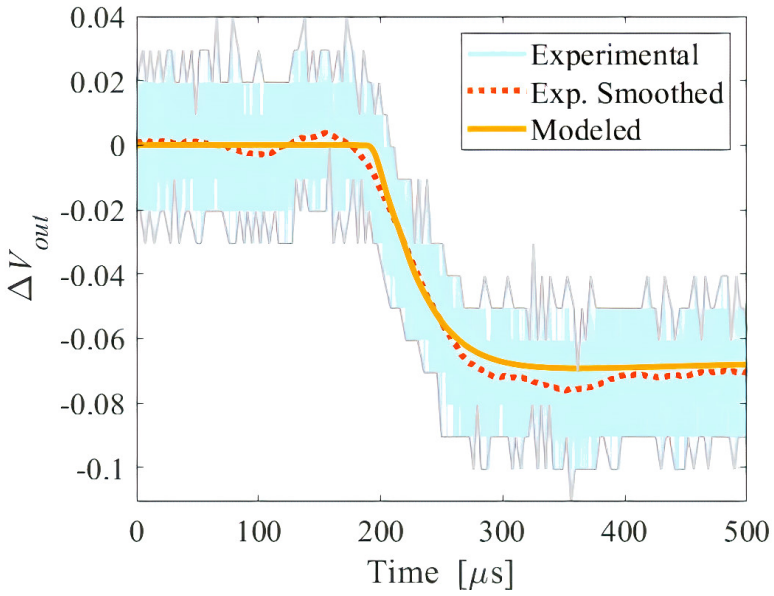


Figure 6.18: Experimental vs. modeled response to a step change in V_{ref} for the design in Fig. 6.17.

To isolate the frequency synchronization loop, the modulation index is fixed and two controllers are used. One drives the inverter, and the other drives the rectifier. The sensed ZCD signal is sent to the digitally-implemented PLL within the rectifier controller. The PFD and compensator reference the 20 MHz clock, and the DCO references the 150 MHz clock. A line of code checks for simultaneous edge triggers between the two clocks in order to avoid detrimental race conditions. The digital PLL reports both the number of clock edges in the current period (output of compensator) and the square wave (output of DCO) to the PWM-generating code block, and the rectifier switches are triggered to match the sensed frequency.

For comparison to the model, the system is set for a step-change in Φ_{ref} from -188 to -198, where these numbers denote the number of clock edges and correspond to $-67.7°$ and $-71.3°$, respectively. Experimental waveforms are extracted from the oscilloscope and imported into MATLAB. Waveform data is interpolated to increase the sampling resolution, and then the zero-crossings of v_{rec} and edges of the sensed ZCD signal are located within the program. The phase difference between these points is calculated along the length of the experimental data, and the result is reported in Fig. 6.20 with the small signal prediction overlaid.

A simulation is included in Fig. 6.20 to illustrate that the non-linearities in the experimental data are expected. If the frequency synchronization control loop is designed correctly the number of clock edges should dither around the carrier frequency. When the switching frequency is too low clock edges are subtracted to increase the frequency. Likewise, increasing the number of clocks per period will decrease the switching frequency. The average

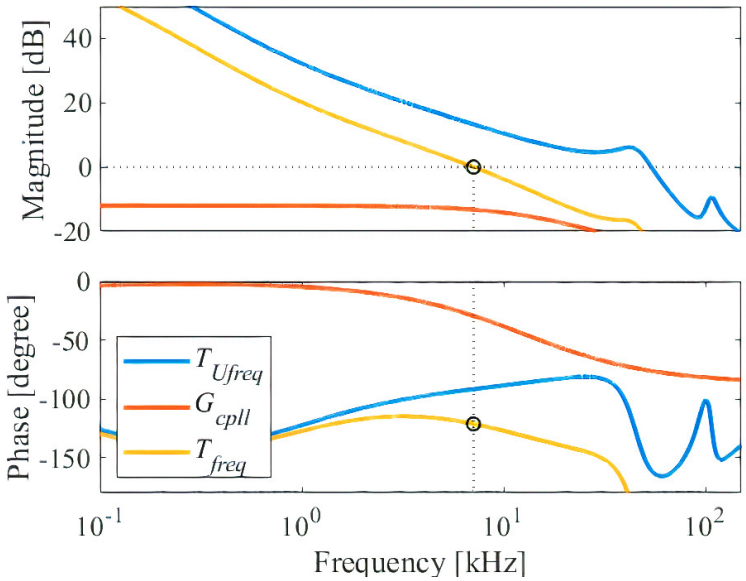


Figure 6.19: Frequency synchronization uncompensated loop gain (T_{Ufreq}), compensator (G_{cpll}), and final loop gain (T_{freq}).

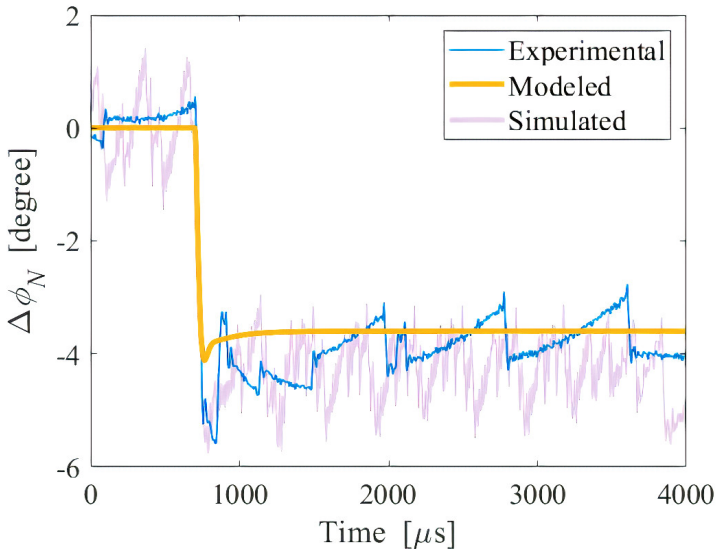


Figure 6.20: Experimental vs. modeled vs. simulated response to a step change in Φ_{ref} for the design in Fig. 6.19.

switching frequency exactly converges to the carrier frequency by means of this dithering effect.

Fig. 6.20 illustrates the dithering in both the experimental data and the simulated data. The measured phase drifts while the number of clocks per period is fixed, and the phase drifts the opposite direction after the compensator changes the number of clocks in the period. The slope of the drift characteristic is a function of the frequency difference between the f_{wpt} and the instantaneous value of f_{pwm}, and the height of the drift characteristic is a function of the clock resolution and the bandwidth. The small signal prediction does not include these non-linearities, but Fig. 6.20 proves that the model clearly predicts the dominant behavior of the system.

In conclusion, the two control loops are modeled and designed for stability. The loops are verified via a stable response to a step in reference wherein the predicted dynamics of each loop accurately reflect the observed dynamics. The next chapter introduces the issue of cross coupling behaviors that exist between the output regulation and frequency synchronization control loops, destabilizing simultaneous operation in some circumstances.

Chapter 7

Dual-Loop Control

In the real wireless power transfer system both the frequency synchronization and output regulation control loops must operate simultaneously. The two isolated control loops that are experimentally verified in Chapter 6 only consider the affects of four of the eight plant transfer functions in Table 6.1. The other four transfer functions describe how the two loops are coupled together. Fig. 7.1 takes the isolated control loops and adds the remaining plant models to reveal the full cross-coupled system from a small signal perspective.

Modulation of any of the levels influences the phase of the system. Likewise, a change in phase affects the output voltage at the rectifier load. The variable $K_{rad} = 2\pi/T_s$ is a conversion to radians, and the variable $K_{vp} = T_s/(2\pi)$ is a conversion to time. While it is useful to consider the design of each control system separately, these cross-coupling affects must be considered when implementing the real system.

Fundamentally, the two control loops must operate as one large stable system that is capable of traversing many steady state operating conditions without instability. The

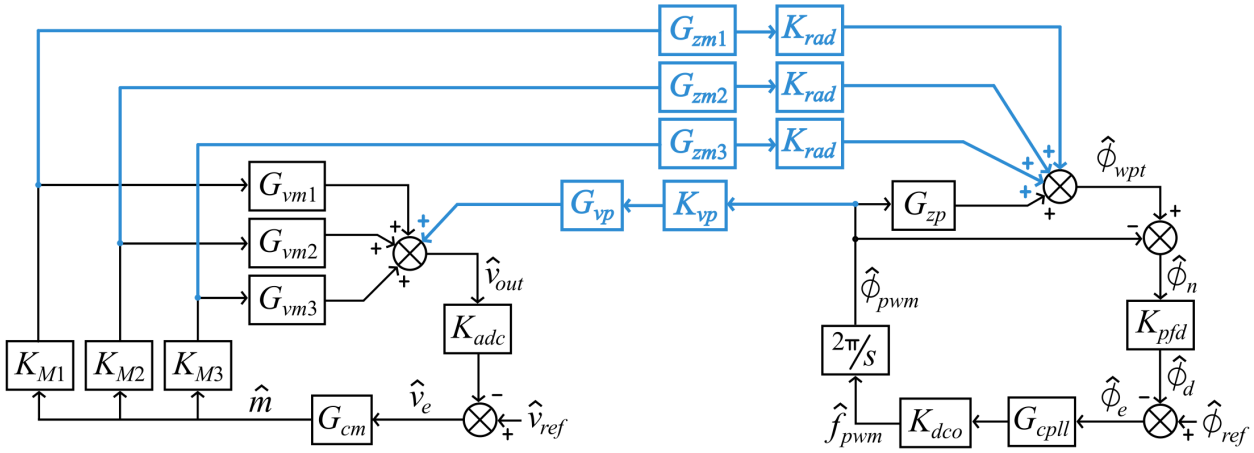


Figure 7.1: The isolated loop designs with the true cross-coupling effects of the power stage incorporated.

fundamental models used to motivate rectifier retuning warrant that a wide range of rectifier impedance (and consequent system loadings, output powers, distortion levels, etc.) must be steady-state stable. Furthermore, the advantages of dynamic system-level retuning warrant that transients between operating points remain stable as well. Therefore, this Chapter is dedicated to providing the solution strategy and experimental validation for dual-loop control design that enables a wide range of fundamental rectifier impedances and ensured stability when traversing the operating region.

7.1 Closed Form Representation

First, the closed form representation of the system is developed as a means to characterize the loop interactions. The small signal representation of the full system is re-illustrated in Fig. 7.2 to complement the analytical derivation. Blocks G_{cp} and M_p are added, and they are an additional compensator and a unit conversion, respectively. The system-level inputs and outputs are highlighted as well. The input reference values $\hat{v}_{ref}$ and Φ_{ref} are highlighted in purple, and regulated nodes $\hat{v}_{out}$ and $\hat{\phi}_n$ are highlighted in red. Because the system is treated as linear time-independent, superposition allows the effect of any single input to be mapped to any single output. The following derivation ultimately results in the four equations detailing how $\hat{v}_{ref}$ and $\hat{\phi}_{ref}$ affect $\hat{v}_{out}$ and $\hat{\phi}_n$ by means of the control circuit.

Subcircuits 1 and 2 in Fig. 7.2 are translated to the diagrams in Fig. 7.3a. The output voltage loop gain is defined in Chapter 6 as $T_{out} = K_{adc}G_{cm}\big(K_{M1}G_{vm1} + K_{M2}G_{vm2} +$

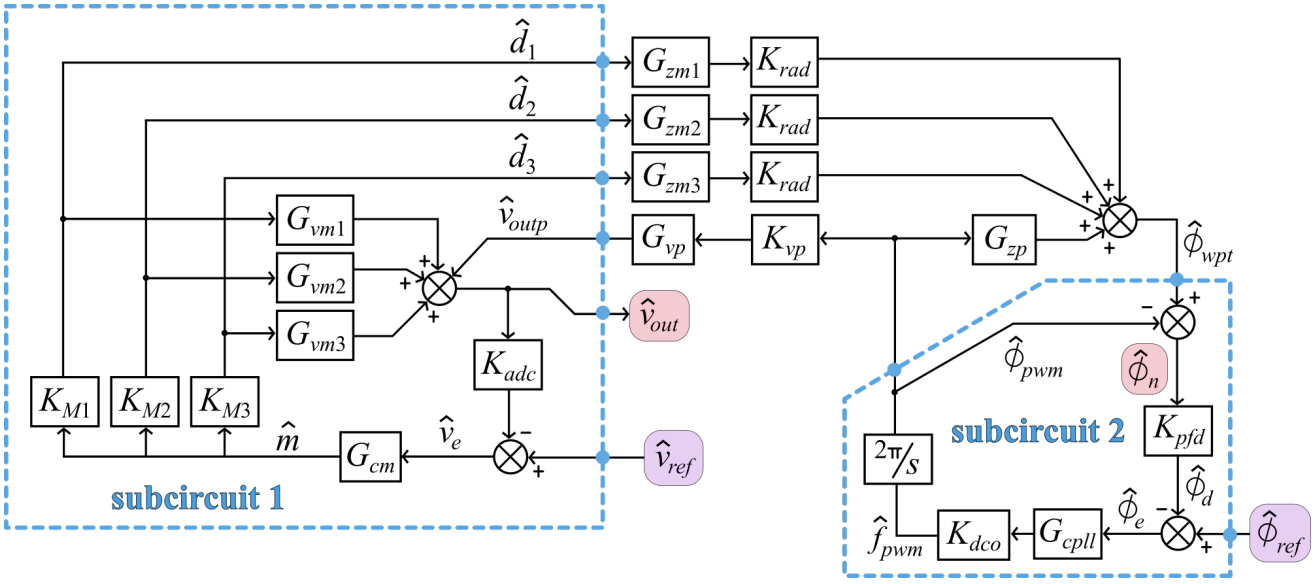


Figure 7.2: The full small signal model with blue dotted lines identifying the subcircuits used to derive the closed form equations.

$K_{M3}G_{vm3}\Big)$, and the loop gain of the PLL without the plant is

$$T_{pll} = K_{pfd}G_{cpll}K_{dco}\Big(2\pi/s\Big). \tag{7.1}$$

To simplify the small signal circuit, the each subcircuit output in Fig. 7.3a is defined in terms of the subcircuit inputs. In subcircuit 1, output $\hat{v}_{out}$ is

$$\hat{v}_{out} = \hat{v}_{outp} + \Big(K_{M1}G_{vm1} + K_{M2}G_{vm2} + K_{M3}G_{vm3}\Big)G_{cm}\Big(\hat{v}_{ref} - K_{adc}\hat{v}_{out}\Big), \tag{7.2}$$

which reduces to

$$\hat{v}_{out} = \hat{v}_{outp}\ \frac{1}{1+T_{out}} + \hat{v}_{ref}\ \frac{1}{K_{adc}}\ \frac{T_{out}}{1+T_{out}}. \tag{7.3}$$

Next, the output of subcircuit 2 is

$$\hat{\phi}_{pwm} = \frac{2\pi}{s}K_{dco}G_{cpll}\Big(\hat{\phi}_{ref} - \Big(\hat{\phi}_{wpt} - \hat{\phi}_{pwm}\Big)K_{pfd}\Big) \tag{7.4}$$

which simplifies to

$$\hat{\phi}_{pwm} = \hat{\phi}_{ref}\ \frac{1}{K_{pfd}}\ \frac{T_{pll}}{1-T_{pll}} - \hat{\phi}_{wpt}\ \frac{T_{pll}}{1-T_{pll}} \tag{7.5}$$

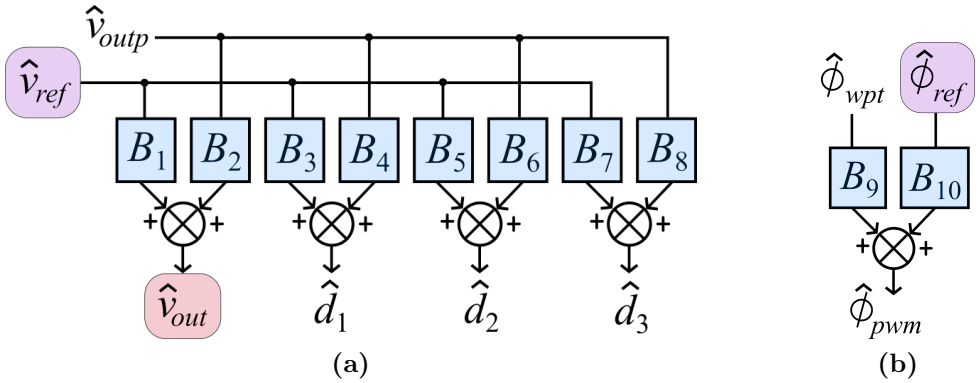


Figure 7.3: The simplified versions of (a) subcircuit 1 and (b) subcircuit 2 from Fig. 7.2.

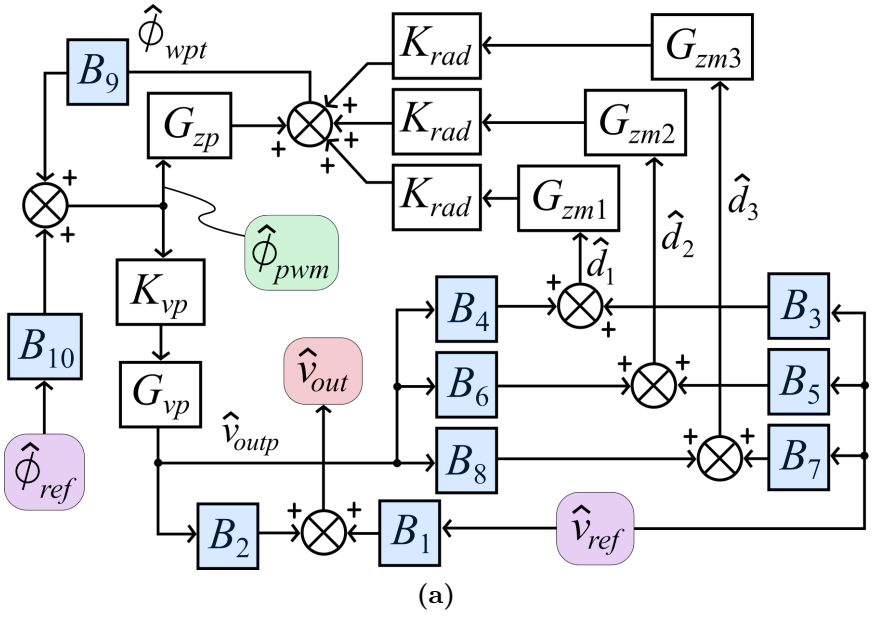


Figure 7.4: The simplified small signal model.

These expressions for $\hat{v}_{out}$ and $\hat{\phi}_{pwm}$ are defined in terms of the inputs of their respective subcircuits. The other outputs are derived in a similar manner. Table 7.1 lists the equations of the subcircuits and defines the $\{B_1, B_2, ...B_9, B_{10}\}$ blocks based on those equations. Each blue block in Fig. 7.3 describes the internal characteristics of the that subcircuit.

The expressions in Table 7.1 and Fig. 7.3 are used to simplify the small signal model into Fig. 7.4. Node $\hat{\phi}_{pwm}$ is highlighted in green in Fig. 7.4 because solving for this node enables the four closed form expressions for the LTI system. First, the loop equation for $\hat{\phi}_{pwm}$ is written:

$$\begin{aligned}\hat{\phi}_{pwm} = B_{10}\hat{\phi}_{ref} + \hat{\phi}_{pwm}B_9G_{zp}+ \\ B_9K_{rad}G_{zm1}\Big(B_3\hat{v}_{ref} + \hat{\phi}_{pwm}B_4G_{vp}K_{vp}\Big)+ \\ B_9K_{rad}G_{zm2}\Big(B_5\hat{v}_{ref} + \hat{\phi}_{pwm}B_6G_{vp}K_{vp}\Big)+ \\ B_9K_{rad}G_{zm3}\Big(B_7\hat{v}_{ref} + \hat{\phi}_{pwm}B_8G_{vp}K_{vp}\Big).\end{aligned} \tag{7.6}$$

The $\hat{\phi}_{pwm}$ terms are consolidated as well as the $\hat{v}_{ref}$ and $\hat{\phi}_{ref}$ terms. Rearranging and simplifying, the expression for $\hat{\phi}_{pwm}$ becomes

$$\hat{\phi}_{pwm}\ (\hat{v}_{ref}, \hat{\phi}_{ref}) = \frac{\begin{aligned}\hat{\phi}_{ref}B_{10} + \hat{v}_{ref}\Big(B_9B_3K_{rad}G_{zm1}+ \\ B_9B_5K_{rad}G_{zm2} + B_9B_7K_{rad}G_{zm3}\Big)\end{aligned}}{\begin{aligned}1 - \Big(B_9G_{zp} + B_9B_4K_{rad}G_{zm1}G_{vp}K_{vp} + \\ B_9B_6K_{rad}G_{zm2}K_{vp}G_{vp} + B_9B_8K_{rad}G_{zm3}K_{vp}G_{vp}\Big)\end{aligned}}. \tag{7.7}$$

Equation 7.7 is written as a function of two inputs for simplicity. $\hat{\phi}_{pwm}$ is included in the final derivations with either input zeroed, as is the property of LTI systems. For $\hat{v}_{out}$, the

Table 7.1: Subcircuit Equations and Block Diagram Coefficients

Output	Equation	Subcircuit Blocks	
$\hat{v}_{out}$	$\hat{v}_{out} = \hat{v}_{ref}\ \frac{1}{K_{adc}}\ \frac{T_{out}}{1+T_{out}} + \hat{v}_{outp}\ \frac{1}{1+T_{out}}$	$B_1 = \frac{1}{K_{adc}}\ \frac{T_{out}}{1+T_{out}}$	$B_2 = \frac{1}{1+T_{out}}$
$\hat{d}_1$	$\hat{d}_1 = \hat{v}_{ref}\ \frac{K_{M1}G_{cm}}{1+T_{out}} - \hat{v}_{outp}\ \frac{K_{M1}G_{cd}K_{adc}}{1+T_{out}}$	$B_3 = \frac{K_{M1}G_{cm}}{1+T_{out}}$	$B_4 = -\frac{K_{M1}G_{cd}K_{adc}}{1+T_{out}}$
$\hat{d}_2$	$\hat{d}_2 = \hat{v}_{ref}\ \frac{K_{M2}G_{cm}}{1+T_{out}} - \hat{v}_{outp}\ \frac{K_{M2}G_{cd}K_{adc}}{1+T_{out}}$	$B_5 = \frac{K_{M2}G_{cm}}{1+T_{out}}$	$B_6 = -\frac{K_{M2}G_{cd}K_{adc}}{1+T_{out}}$
$\hat{d}_3$	$\hat{d}_3 = \hat{v}_{ref}\ \frac{K_{M3}G_{cm}}{1+T_{out}} - \hat{v}_{outp}\ \frac{K_{M3}G_{cd}K_{adc}}{1+T_{out}}$	$B_7 = \frac{K_{M3}G_{cm}}{1+T_{out}}$	$B_8 = -\frac{K_{M3}G_{cd}K_{adc}}{1+T_{out}}$
$\hat{\phi}_{pwm}$	$\hat{\phi}_{pwm} = \hat{\phi}_{ref}\ \frac{1}{K_{pfd}}\ \frac{T_{pll}}{1-T_{pll}} - \hat{\phi}_{wpt}\ \frac{T_{pll}}{1-T_{pll}}$	$B_9 = -\frac{T_{pll}}{1-T_{pll}}$	$B_{10} = \frac{1}{K_{pfd}}\frac{T_{pll}}{1-T_{pll}}$

definition is easy to derive as a function of $\hat{\phi}_{pwm}$:

$$\hat{v}_{out} = \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_2K_{vp}G_{vp} + \hat{v}_{ref}B_1. \tag{7.8}$$

This is the final description of $\hat{v}_{out}$ in terms of inputs $\hat{v}_{ref}$ and $\hat{\phi}_{ref}$. The derivation of $\hat{\phi}_n$ requires an extra step that begins with

$$\begin{aligned}\hat{\phi}_{wpt} = {} & \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})G_{zp} + K_{rad}G_{zm1}\Big(\hat{v}_{ref}B_3 + \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_4K_{vp}G_{vp}\Big) + \\ & K_{rad}G_{zm2}\Big(\hat{v}_{ref}B_5 + \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_6K_{vp}G_{vp}\Big) + \\ & K_{rad}G_{zm3}\Big(\hat{v}_{ref}B_7 + \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_8K_{vp}G_{vp}\Big).\end{aligned} \tag{7.9}$$

This description of $\hat{\phi}_{wpt}$ is in terms of $\hat{v}_{ref}$ and $\hat{\phi}_{ref}$ via the use of $\hat{\phi}_{pwm}$. Finally, the to desired output $\hat{\phi}_n$ is defined in Fig. 7.2:

$$\hat{\phi}_n = \hat{\phi}_{wpt} - \hat{\phi}_{pwm}. \tag{7.10}$$

The LTI description of the whole small signal WPT system is summarized in Table 7.2, where the four relationships between the two system inputs and two system outputs are characterized.

Table 7.2: Complete Small Signal Model

Definitions
$\hat{\phi}_{pwm}\ (\hat{v}_{ref}, \hat{\phi}_{ref}) = \dfrac{\hat{\phi}_{ref}B_{10} + \hat{v}_{ref}\Big(B_9B_3K_{rad}G_{zm1} + B_9B_5K_{rad}G_{zm2} + B_9B_7K_{rad}G_{zm3}\Big)}{1 - \Big(B_9G_{zp} + B_9B_4K_{rad}G_{zm1}G_{vp}K_{vp} + B_9B_6K_{rad}G_{zm2}K_{vp}G_{vp} + B_9B_8K_{rad}G_{zm3}K_{vp}G_{vp}\Big)}$
$\hat{\phi}_{wpt} = \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})G_{zp} + K_{rad}G_{zm1}\Big(\hat{v}_{ref}B_3 + \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_4K_{vp}G_{vp}\ \Big) + K_{rad}G_{zm2}\Big(\hat{v}_{ref}B_5 + \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_6K_{vp}G_{vp}\ \Big) + K_{rad}G_{zm3}\Big(\hat{v}_{ref}B_7 + \hat{\phi}_{pwm}(\hat{v}_{ref}, \hat{\phi}_{ref})B_8K_{vp}G_{vp}\Big)$

Relationship	Equation
$\hat{v}_{out}\big(\hat{v}_{ref}\big)\big\vert_{\hat{\phi}_{ref}=0}$	$\hat{v}_{out} = \hat{\phi}_{pwm}(\hat{v}_{ref}, 0)B_2K_{vp}G_{vp} + \hat{v}_{ref}B_1$
$\hat{v}_{out}\big(\hat{\phi}_{ref}\big)\big\vert_{\hat{v}_{ref}=0}$	$\hat{v}_{out} = \hat{\phi}_{pwm}(0, \hat{\phi}_{ref})B_2K_{vp}G_{vp}$
$\hat{\phi}_n\big(\hat{\phi}_{ref}\big)\big\vert_{\hat{v}_{ref}=0}$	$\hat{\phi}_n = \hat{\phi}_{wpt}(0, \hat{\phi}_{ref}) - \hat{\phi}_{pwm}(0, \hat{\phi}_{ref})$
$\hat{\phi}_n\big(\hat{v}_{ref}\big)\big\vert_{\hat{\phi}_{ref}=0}$	$\hat{\phi}_n = \hat{\phi}_{wpt}(\hat{v}_{ref}, 0) - \hat{\phi}_{pwm}(\hat{v}_{ref}, 0)$

Table 7.3: Operating Point used to Examine the Closed Form Small Signal Model

V_{in}	V_{out}	P_{out}	R_{out}	η
15 V	5 V	16.88 W	1.47 Ω	93.77 %
t_1	t_2	t_3	$\lvert Z_{rec,1}\rvert$	$\angle Z_{rec,1}$
2.6 %	8.1 %	15.0 %	6.78 Ω	21.92 °

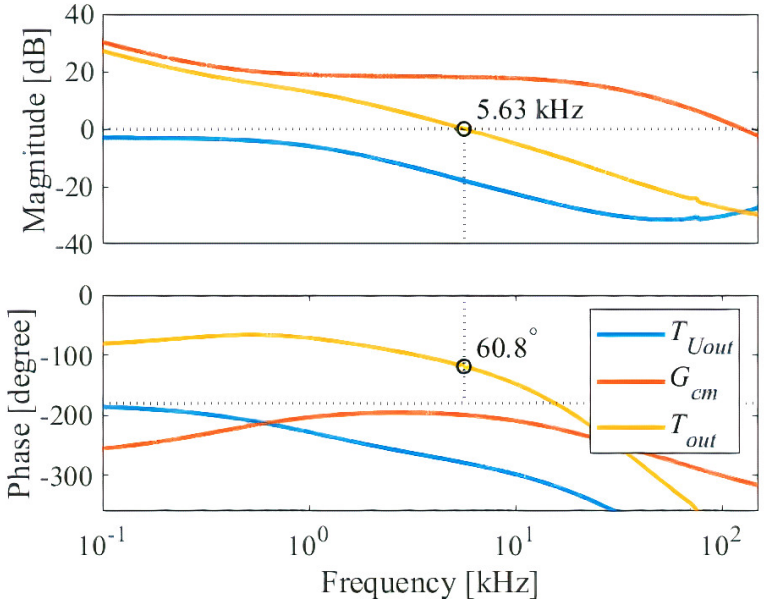
7.2 Closed Form Equations Applied

The closed form equations provide insight into the system-wide interactions. However, translation from the designs of each isolated control loop to the final closed form, system-wide loop gains requires some explanation. An example operating point is examined with two different isolated loop designs, and the resulting system-wide gains are calculated and discussed in order to establish a more intuitive understanding of the control system. First, the operating point used during this section is outlined in Table 7.3.

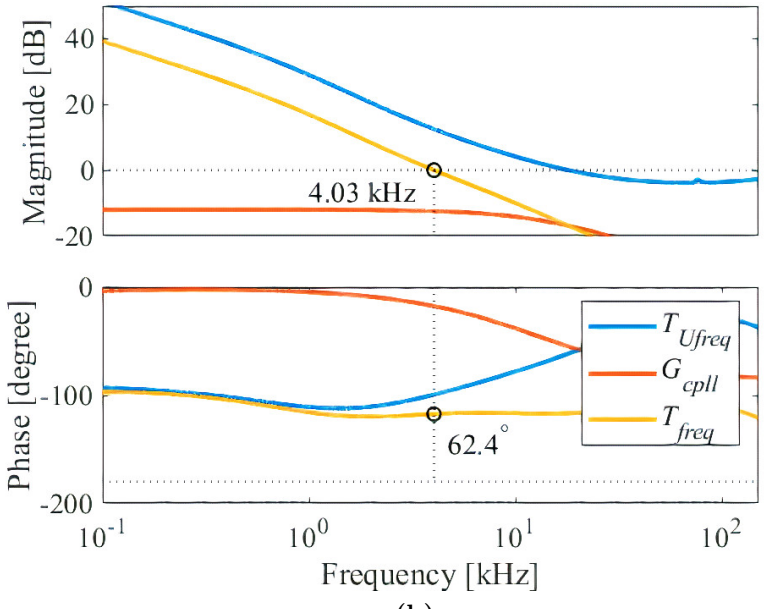
The operating point in Table 7.3 is a nearly 17 W, 94 % efficient point, with $M = 3.12$. Each rectifier level is utilized, but with $t_3 = 15.0$ % of the period, v_{rec} is far from being a square wave. This operating point is arbitrarily chosen but does incorporate most "normal" system characteristics. Using the methodology established in Chapter 6, the isolated loops are designed to be stable for this operating point. Fig. 7.5 shows the isolated loop designs for the output regulation and frequency synchronization loops.

The two loop designs in Fig. 7.5 have the very similar control bandwidths. The output regulation loop has a crossover frequency of $f_{c-out} = 5.63$ kHz and a phase margin of $\phi_{m-out} = 64.4°$. The frequency synchronization loop has $f_{c-freq} = 4.03$ kHz and $\phi_{c-freq} = 62.4°$. When the equations from Table 7.2 are applied with these isolated loop designs, the results are shown in Fig. 7.7. Note that these results are taken with $G_{cp} = 0$: this element is included in the derivation for later incorporation into the model.

Many useful observations can be made about the bode plots in Fig. 7.7. First, the cross-referenced relationships ($\hat{\phi}_{ref} \rightarrow \hat{v}_{out}$ and $\hat{v}_{ref} \rightarrow \hat{\phi}_n$) have some affect near in the



(a)



(b)

Figure 7.5: Isolated loop designs for both (a) output voltage regulation and (b) frequency synchronization.

higher frequency range in accordance with the isolated loop bandwidths, but they have no DC gain. This means that changing either reference has some initial effect on the opposite control output, but ultimately the system returns that output to the same value. Ideally, these cross-coupling effects would not exist, but given that they do, the closed-form system description quantifies them and gives design insight.

The second important observation is related to the direct-referenced relationships: $\hat{\phi}_{ref} \rightarrow \hat{\phi}_n$ and $\hat{v}_{ref} \rightarrow \hat{v}_{out}$. The isolated output and frequency control loops are written in terms of reference-to-output via

$$\frac{\hat{v}_{out}}{\hat{v}_{ref}} = \frac{1}{K_{adc}} \frac{T_{out}}{1 + T_{out}} \tag{7.11}$$

and

$$\frac{\hat{\phi}_n}{\hat{\phi}_{ref}} = \frac{1}{K_{pfd}} \frac{T_{freq}}{1 + T_{freq}}, \tag{7.12}$$

respectively. These isolated relationships are compared to the complete system model in Fig. 7.7. The comparison shows that the predictions made by isolating each loop no longer hold when every characteristic of the small signal system is included. Both bode plots show resonant behavior near the crossover frequency that is not predicted by the isolated loop designs. The implication is that the interactions of the two control loops cause significant deviation from the predicted behavior.

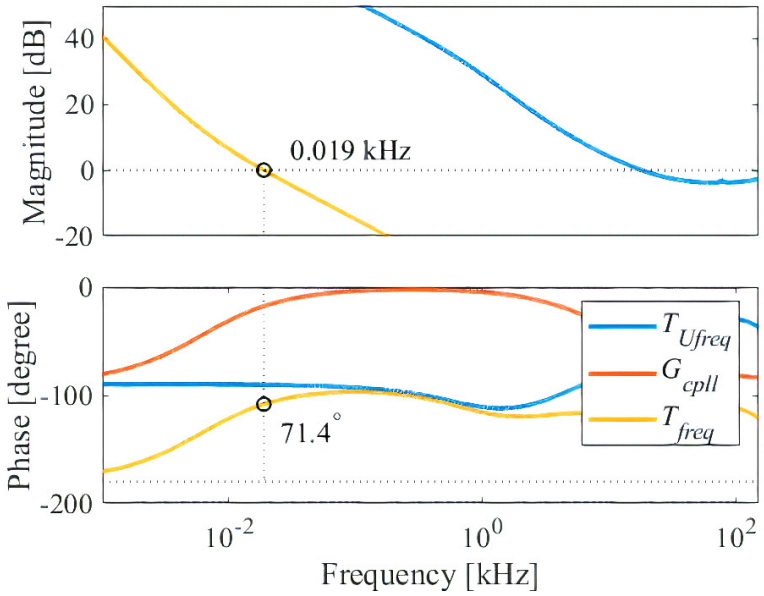


Figure 7.6: Lower bandwidth design for the isolated frequency synchronization control loop.

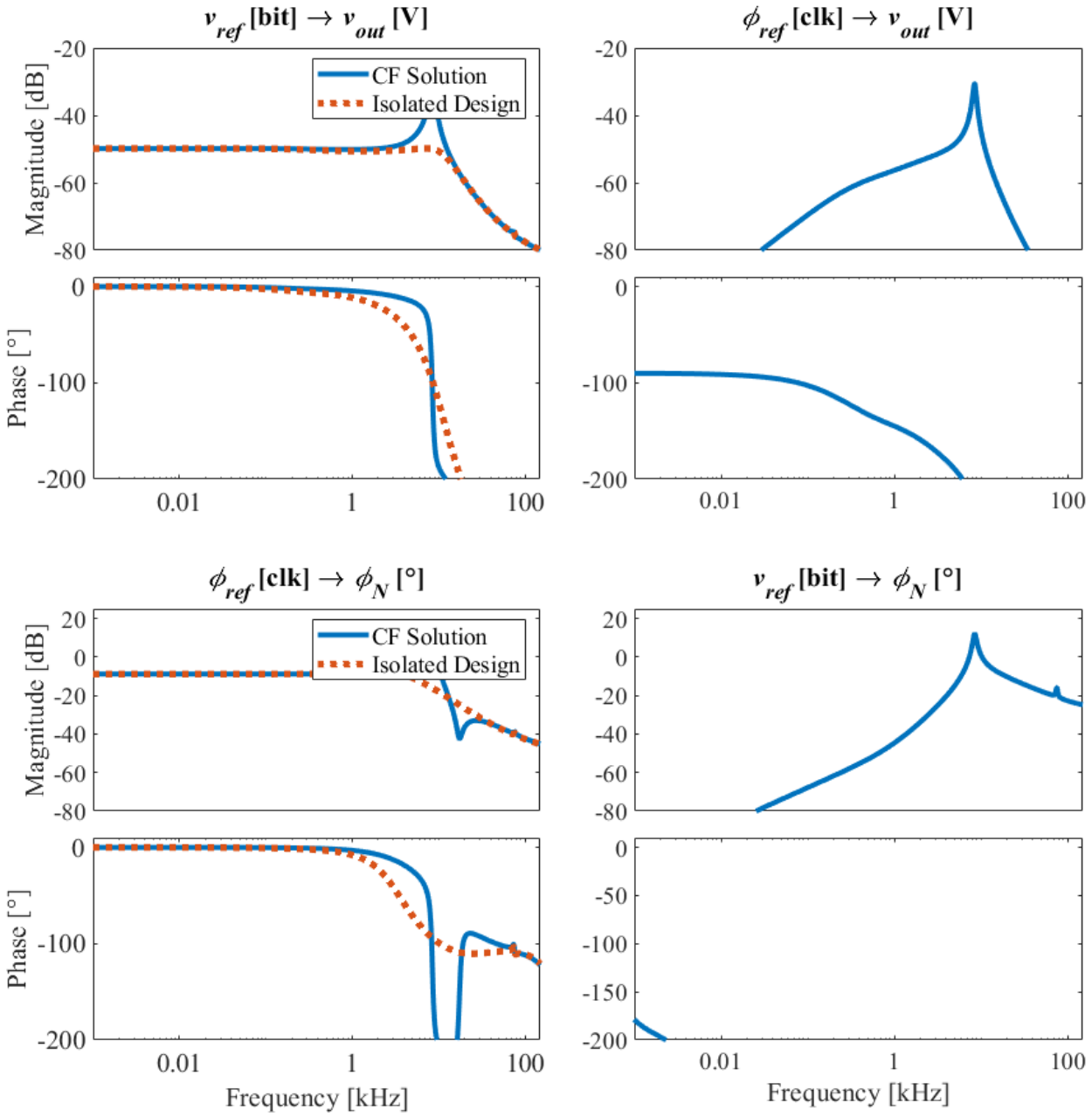


Figure 7.7: Initial input-to-output interactions given similar control bandwidths for the isolated feedback loop designs.

One approach to addressing this deviation is bandwidth decoupling. This technique sets different control bandwidths for the two individual loops, implying less cross-coupling. One approximate way of understanding this approach is to say that the faster loop always reaches steady state before the slower loop responds, thereby decoupling their interactions by disallowing each loop to be actively editing the circuit at the same time. To test this, the isolated frequency synchronization loop is redesigned for lower bandwidth: $f_{c-freq} =$ 0.019 kHz and $\phi_{m-freq} = 71.4°$.

The closed form equations are again applied to the system, and the results are printed in Fig. 7.8. Again, the cross-referenced terms showcase some effect at higher frequencies and zero effect at DC. Here, however, the difference between the isolated voltage loop and the full-system representation is effectively negligible. Decoupling the control bandwidths significantly reduces loop interaction and establishes the isolated loop approximation as a valid approach for the faster control loop. Furthermore, the relationship between the phase reference and phase output is affected by the presence of the much faster voltage feedback loop, but there is significantly less discrepancy between the simple and complete models than before the control bandwidths were decoupled. The only notable resonance occurs near the crossover of the voltage control loop, and these frequencies are almost completely attenuated due to the lower bandwidth of the frequency synchronization loop. The plotted results in Fig. 7.8 actually show increased bandwidth within the phase control loop, which is a welcome characteristic insofar as the system remains stable.

The simulation platform is used to further investigate dual-loop operation. The bandwidth decoupled design shown in Fig. 7.8 is implemented in the Simulink platform.

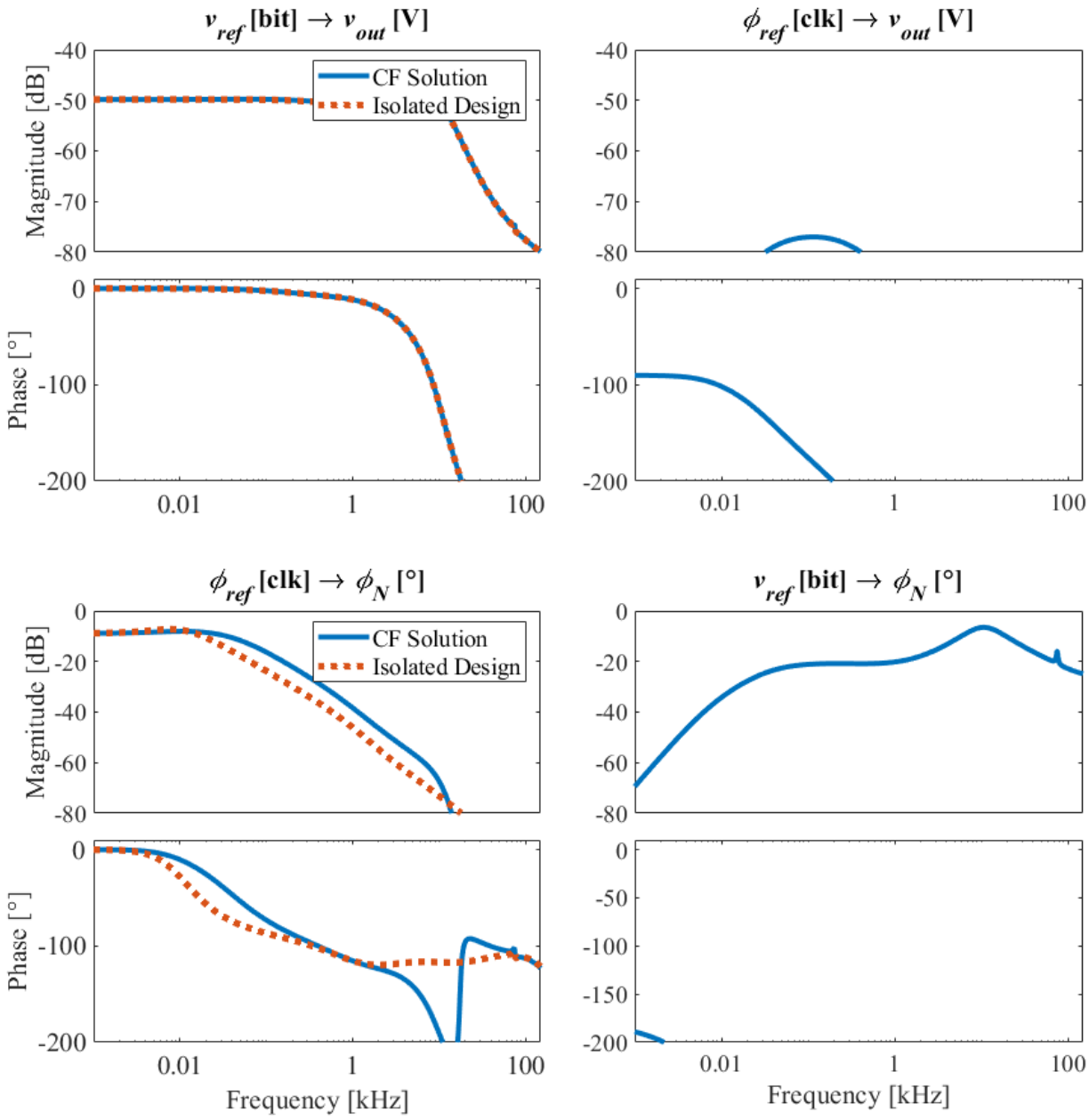


Figure 7.8: Input-to-output interactions given a much lower bandwidth design for the isolated frequency synchronization loop.

Fig. 7.9 shows the results of two voltage reference steps and one phase reference step. The output voltage tracks the voltages reference with a bandwidth that is noticeably higher the the phase response. Furthermore, there is no noticeable effect on V_{out} when Φ_{ref} is stepped. This is predicted by the small signal model in Fig. 7.8: the peak effect is smaller than -80 dB. The small signal model also predicts that stepping $\hat{v}_{ref}$ has a noticeable effect on $\hat{\phi}_n$, which is once again verified by the simulation.

The closed form equations of the entire system provide insight into the cross-coupling behaviors of the two control loops. While these equation do not provide a final solution to the dual-loop control problem, the system characterization and consequent designer intuition are both useful for investigating potential solutions. The mathematical analysis is supported by the dual-loop simulation in Fig. 7.9, where both loops appear stable and the cross-coupling behaviors are as predicted. The bandwidth decoupling method is shown to circumvent unwanted cross-coupling interactions, but the drawback is a low bandwidth frequency synchronization loop. Fundamentally, there is a lower limit to the bandwidth of the frequency synchronization loop. If the control loop responds too slowly the phase drift of the power stage will run away with catastrophic consequences. In the case that the output regulation loop is driven to low bandwidth by the plant, eventually bandwidth decoupling will warrant system failure due to this phase drift effect. Therefore, bandwidth decoupling is useful for illustrating how the closed form system equations interact with the isolated designs, but it is not the optimal design solution to ensure functionality.

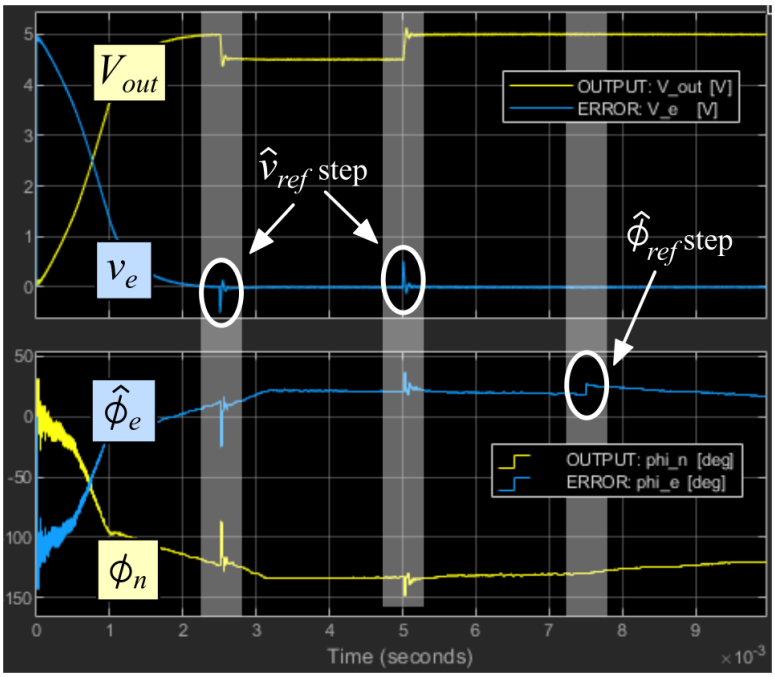


Figure 7.9: Simulated result of multiple reference steps for the bandwidth-decoupled design.

7.3 Zero-Slope Power Contours

Bandwidth decoupling demonstrates that design can influence the degree to which the two isolated control loops are cross-coupled. To extend this type of approach, the steady state power contours are plotted for the experimental tank in Fig. 7.10a. Two steady state operating points are highlighted, an orange square and a white dot. At these points, the slope of the 20 W power contour is exaggerated by straight black lines. The slope of the power contour at the white circle is parallel to the ϕ_{ref} axis, thereby decoupling power throughput from this axis. Intuitively, this is beneficial because modulation (y-axis) is used to control power: a change in modulation near this point affects output power. Inversely, a change in ϕ_{ref} around this same operating point does not affect the steady state output power. The orange square in Fig. 7.10a demonstrates a different case, and a change in either M or ϕ_{ref} around this point varies the output power.

The small signal representations of the square and dot points from Fig. 7.10a are shown in Figs. 7.10b and 7.10c, respectively. For Fig. 7.10b, the loop gains T_{out} and T_{freq} are compensated to have similar bandwidths (4.5 kHz and 5.4 kHz). The complete closed-form solution derived in Table 7.2 predicts resonant dynamics that the isolated designs miss. For Fig. 7.10c, the same compensators are used, and the two small signal derivations show good agreement. Here, designing the two control loops in isolation is a valid strategy, but the same is not true of Fig. 7.10b.

Fig. 7.10 implies that cross-coupling effects can be loosely predicted by the steady state operating points of the converter. Ideally, the trajectory that best attenuates cross-coupling

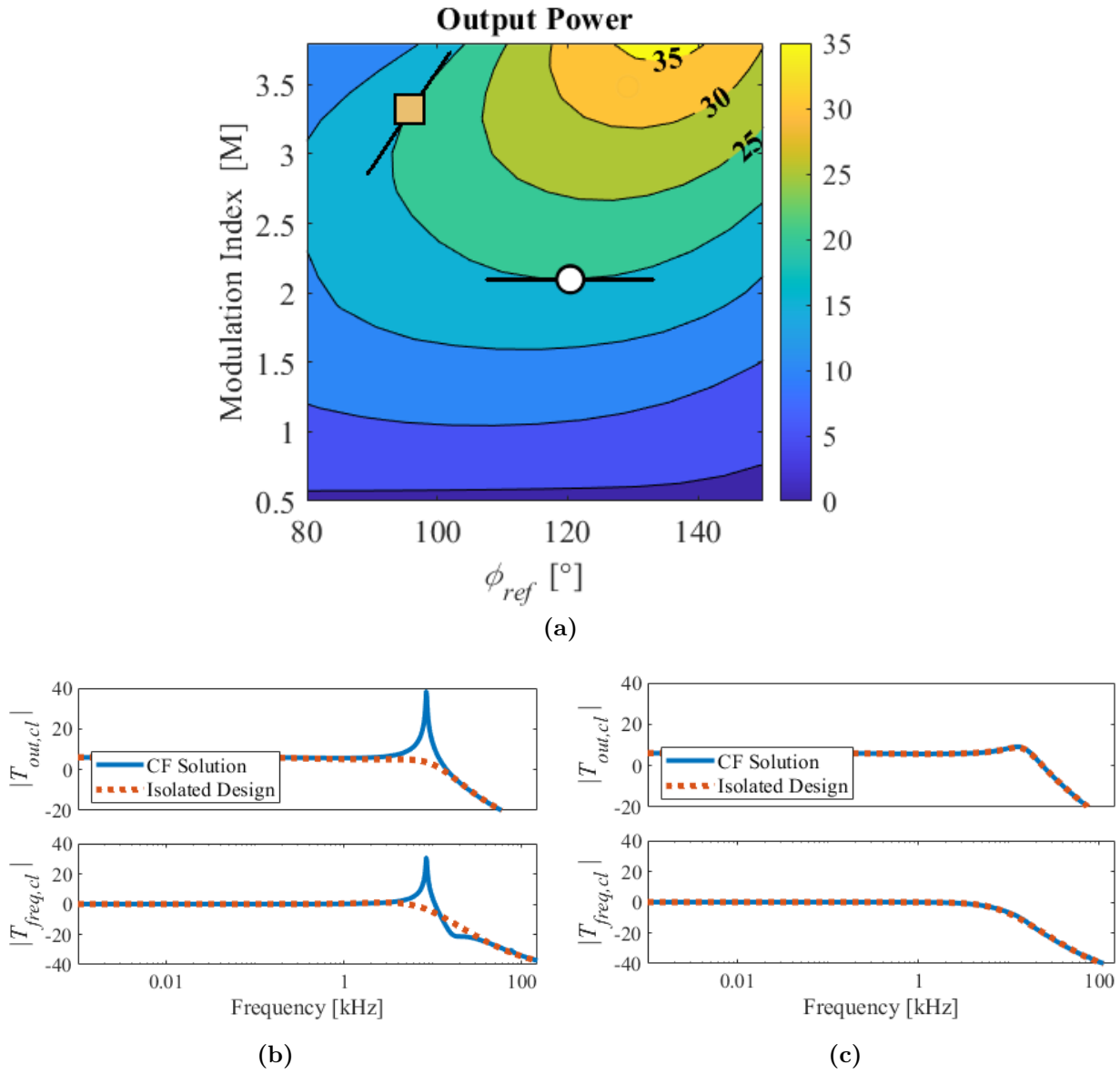


Figure 7.10: (a) Modeled output power with two labeled points. Small signal characteristics are shown for the (b) orange square and (c) white dot.

effects would be in good agreement with the trajectory for highest efficiency. Incidentally, this alignment occurs when the tank is tuned at the carrier frequency. Under the ideal tuning, the primary and secondary both resonate at the fundamental, that is: $L_{tx}|C_p = 150$ kHz and $L_{rx}|C_s = 150$ kHz (this shorthand is used to describe the resonance of the listed components). This case is shown in Fig. 7.11. Under the fundamental model, the maximum rectifier efficiency is the trajectory where the impedance presented by the rectifier is resistive (shown by the white line). This trajectory is perpendicular to the iso-power contours at all points, meaning that the highest efficiency and lowest cross-coupling trajectory are identical in the ideal tuning case. However, when the tank is detuned from the ideal case and items like harmonic content, sensing delays, and switching loss are considered, then the optimal trajectories for efficiency and cross-coupling attenuation will not precisely coincide.

While convenient, control cannot be a strict function of ideal tank tuning. Given that an engineer has control over the design of the secondary side resonance but not the primary, the system must be dual-loop stable in the cases where the primary side tuning deviates from the ideal case. To test this concept, a set of experiments is carried out wherein four different tanks are used to test dual-loop control. Each tank is tested with a constant value of ϕ_{ref} defined so that the 20 W zero-slope power contour intersects with the operating trajectory (the trajectory where cross-coupling attenuation is implied). All tests have $L_{rx}|C_s = 150$ kHz and some non-ideal value for $L_{tx}|C_p$, and the first three tests are carried out with a carrier frequency of 150 kHz. The aim of these tests is to isolate primary side $L_{tx}|C_p$ detuning. The fourth test leverages a carrier frequency of 200 kHz, another system characteristic set by the inverter. The purpose of this test is to isolate a case where both sides are detuned.

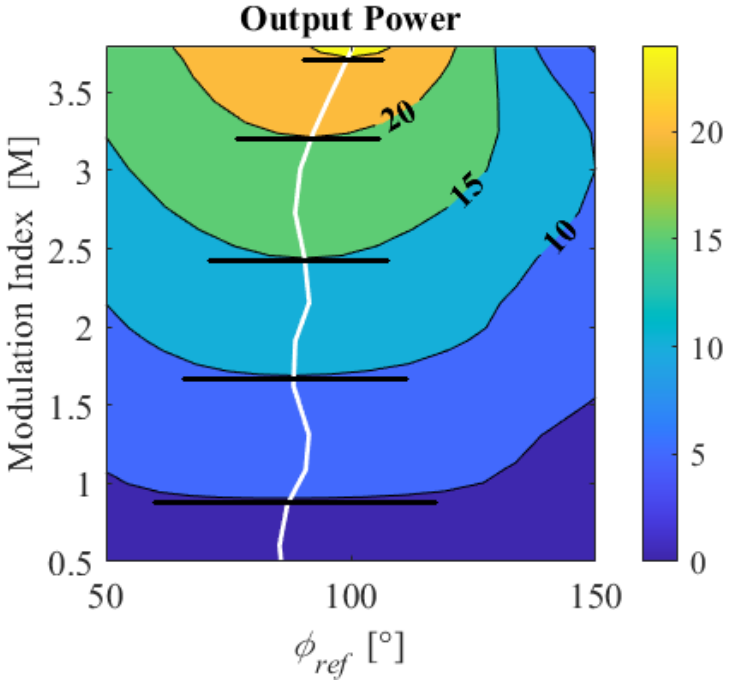


Figure 7.11: Power contours for the ideal tank tuning ($L_{tx}|C_p$ = 150 kHz and $L_{rx}|C_s$ = 150 kHz) accompanied by a white line that denotes $\angle Z_{rec,1} = 0°$.

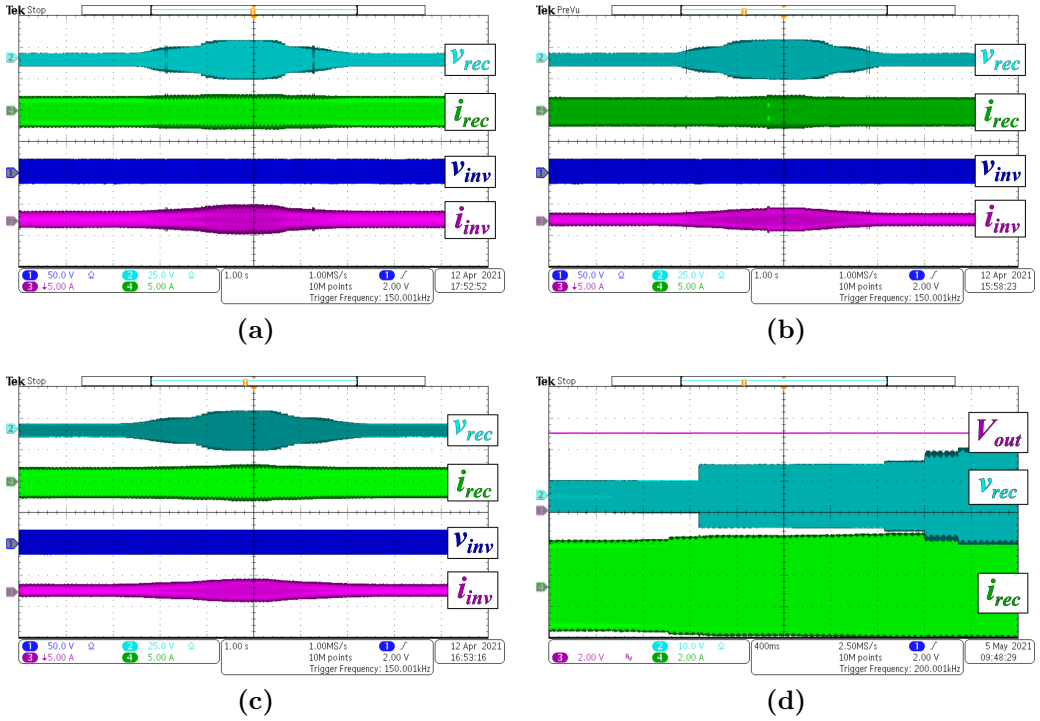


Figure 7.12: Low power (≈7 W) to 20 W sweeps under dual-loop operation with a constant value of ϕ_{ref}. Primary side tanks tuned with $L_{rx}|C_s = 150$ kHz and secondary side tanks ($L_{tx}|C_p$) tuned at (a) 180, (b) 120, and (c) 90 kHz with a fundamental operating frequency of 150 kHz. (d) Carrier frequency of 200 kHz with tuning of $L_{tx}|C_p = 131$ kHz and $L_{rx}|C_s = 150\ kHz$.

Fig. 7.12 shows the experimental results of the tests and illustrates that dual-loop control is viable under non-ideal $L_{tx}|C_p$ tuning conditions. Each test traverses from low power ($\approx$ 7 W) to 20 W at peak power. The ϕ_{ref} value for each test is set so that the 20 W operating point occurs at the zero-slope power contour. According to the detuning, the lower power operating points deviate from the zero-slope power contour trajectory. This experimentally tests the degree to which deviation from this trajectory deters stable operation.

For primary side tunings of 180, 120, and 90 kHz, the experimental results in Figs. 7.12a-7.12c demonstrate stability across a wide range of operating powers, including full power at 20 W. The four tank waveforms are shown in these images to give reference to how the tank waveforms change with operating load. Fig. 7.12d also shows stability in the case where both sides are detuned because the carrier frequency deviates from the secondary side resonance. Here, output voltage is shown as proof of output regulation, and a high frequency digital filter removes noise from the waveform. The results in Fig. 7.12 validate the zero-slope power contour concept as a viable means of cross-coupling attenuation when the WPT tank is tuned away from the fundamental frequency.

7.4 Experimental WPT Tank Retuning

According to Chapter 5, the experimental tank is not tuned at or near the ideal tuning. The primary and secondary side resonances of the experimental system are $L_{tx}|C_p = 131$ kHz and $L_{rx}|C_s = 50$ kHz. The original motivations for this tuning are two-fold. As presented in Section 5.2, tuning the tank with the ideal values leads to significant harmonic components

due to the line resonance that includes components C_p, L_p, L_s, and C_s. Next, a detuned tank is used to showcase the advantages of the MSC: even though the WPT tank is not ideal, the experimental results in Chapter 5 show the rectifier adequately traversing the operating region at high efficiencies for many different powers.

The first of these reasons is answered with low THD switching. As shown by the SHE modulated experimental results in Section 5.8, the distortion in the tank is significantly reduced by the combination of MSC staircase and inverter SHE waveforms. The second reason resolves now that the MSC topology is already motivated. Given the experimental results in Chapter 5, the focus now turns to system-wide design and optimization. Given that tuning the WPT system near the ideal case complements both the dual-loop control work and system-wide optimization (to follow in Chapter 8), the experimental system is retuned.

The caveat to the ideal tuning is that the WPT tank has no impedance at the fundamental frequency. This means that if the rectifier presents high impedance $|Z_{rec,1}| = \infty$, then the primary side experiences very large circulating current. This catastrophic case must be avoided, so the primary side is tuned near the fundamental but not perfectly at the fundamental. This prevents the need for protection circuitry by inserting impedance and reducing the maximum possible circulating current. Furthermore, it serves to validate dual-loop control insofar as stable implementation is not strictly a function of perfect tuning.

The tank is retuned and measured with the impedance analyzer using the same method as Section 5.2. The values of the new WPT tank are given in Table 7.4, and the power contour plot is shown in Fig. 7.13 with efficiency lines overlaid.

Table 7.4: New WPT Tank Values

L_{tx}	L_{rx}	C_p	C_s	R_p	R_s
13.22 μH	13.26 μH	111.01 nF	84.14 nF	70.95 mΩ	74.31 mΩ
k	R_{pp3}	R_{pp5}	R_{ss3}	R_{ss5}	
0.784	351.46 mΩ	920.85 mΩ	358.66 mΩ	933.53 mΩ	

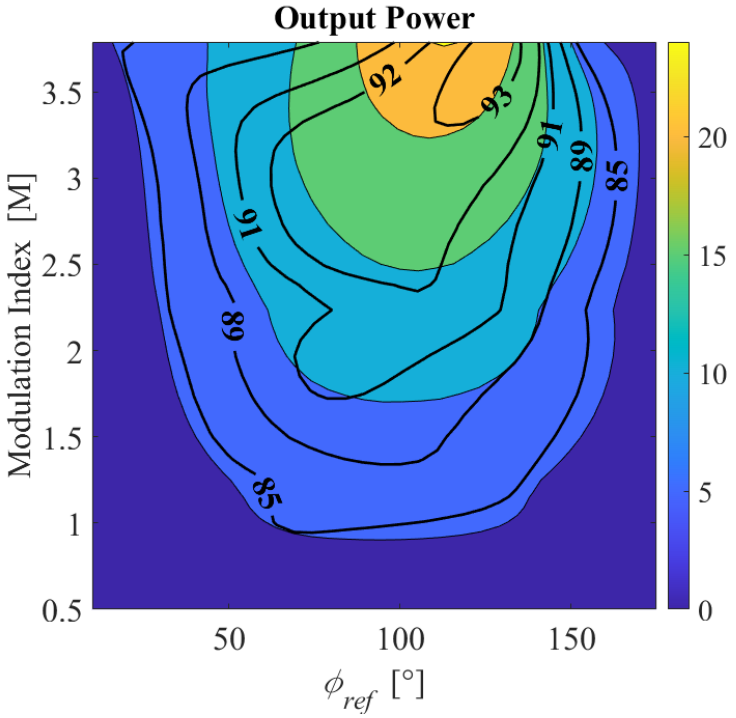


Figure 7.13: Power contours (color) for the new experimental tank tuning ($L_{tx}|C_p$ = 131.1 kHz and $L_{rx}|C_s$ = 151.0 kHz) accompanied efficiency contours (black) at V_{in} = 19 V.

7.5 Model Deviation and Instability

The difference in the small signal models in Fig. 7.10 is substantial, implying that cross-coupling dynamics (and consequent instability) are more relevant in certain operating regions than in other regions. The analysis in this section aims to quantify the differences between the complete an isolated models over the entire operating range. This information, accompanied by pole information from the complete system model, is used to predict stability and instability regions.

First, the complete and isolated small signal models are constructed for each operating points in the space. Two compensators are designed at the 20 W black X on Fig. 7.14a with the same methodology outlined in Chapter 7.4. The frequency loop has 85° of phase margin at a crossover frequency of 1.32 kHz, and the output regulation loop has 56.2° of phase margin at a crossover frequency of 7.09 kHz. Each control loop results in a range of bandwidths and phase margins according to the plant characteristics at any given steady state operating point. The loop gain information for the whole operating range is given in Fig. 7.14. The output regulation compensator is designed for 7 kHz in the zero-slope power contour region wherein the majority of the operation will take place. Similarly, the frequency synchronization loop is designed for around 2 kHz along the same trajectory.

Next, the isolated designs shown in Fig. 7.14 are compared to the complete, closed-form system model in order to highlight the regions where significant differences exist between the models. For each operating point, comparisons are made between the isolated and complete models (like the comparisons in Figs. 7.10b and 7.10c), and the maximum deviation between

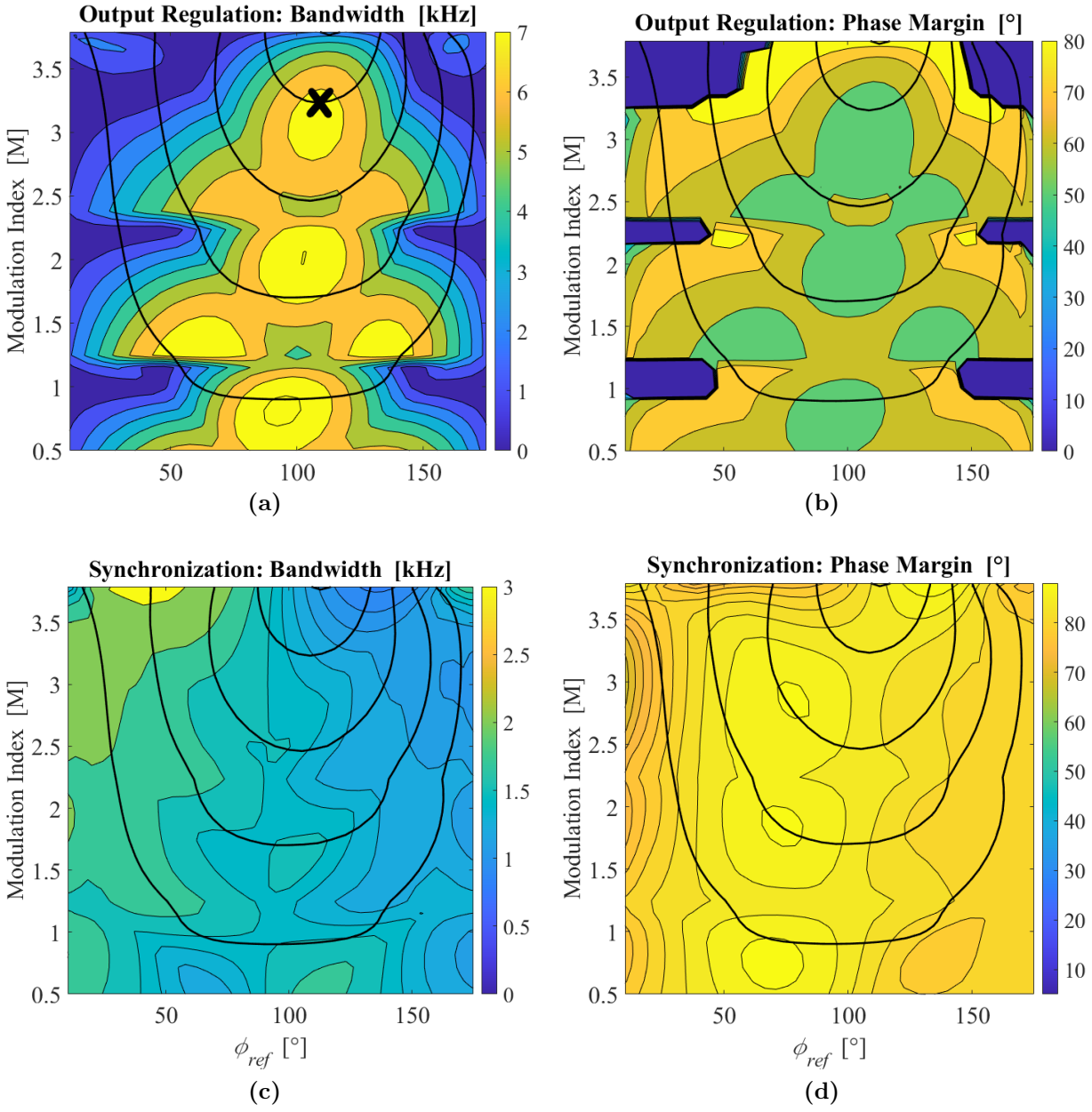


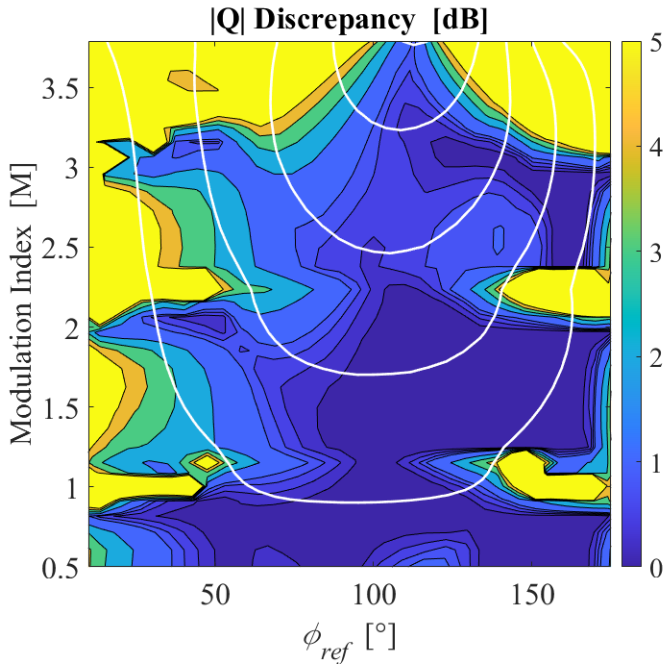
Figure 7.14: Output regulation and frequency synchronization compensators applied to the entire operating space, showing output regulation (a) bandwidth and (b) phase margin and frequency synchronization (c) bandwidth and (d) phase margin. The overlaid black lines are the power contours that match Fig. 7.13

the models is recorded in decibels. The magnitudes of these differences for the V_{out}/V_{ref} and ϕ_n/ϕ_{ref} relationships are summed, and the result of this analysis is shown in Fig. 7.15a.

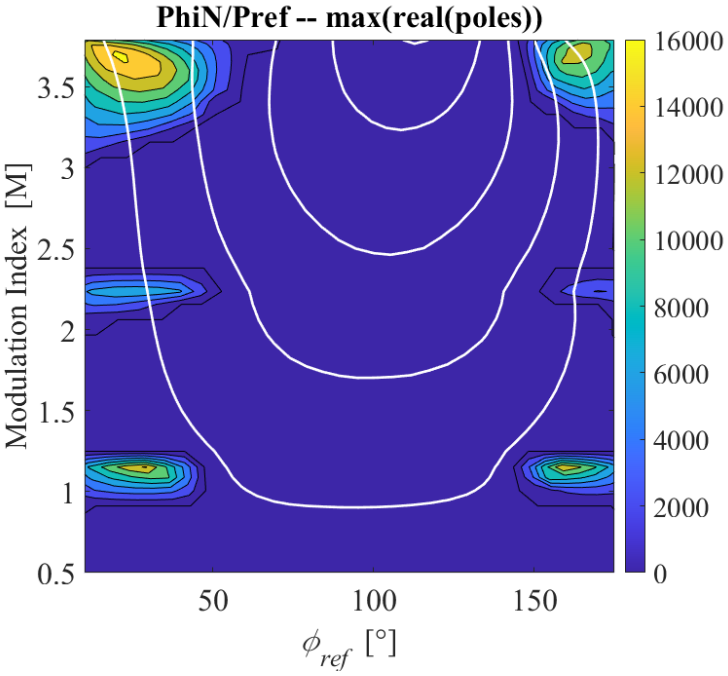
Designing via the isolated models is sufficient along the zero-slope power contour trajectory, further confirming the intuitive analysis established earlier. The models deviate moving outwardly away from the trajectory, and very significant deviation between the isolated and complete models occurs at the upper corners of Fig. 7.15a, where the power contour slopes are nearly vertical. Furthermore, the models appear to deviate when modulation levels are removed at around $M = 1.25$ and $M = 2.25$. Here, deviation between the models strongly implies unwanted control characteristics, but it does not guarantee instability.

Lastly, the poles of the closed form models are shown in Fig. 7.15b. All of the pole and zero information is extracted for each steady state operating point using the complete, closed form system model. The relationship V_{out}/V_{ref} is referenced, and each pole is evaluated based on its real portion. The plot in Fig. 7.15b shows the maximum real portion across all the poles for any given operating point. The data illustrates that the regions highlighted by Fig. 7.15a for deviation between the two models are the same regions that are inherently unstable via the full system model. These regions showcase right half plane poles, clearly predicting instability.

Two experiments are carried out to validate the stability models. First, low power (< 1 W in some cases) up to 20 W is tested with multiple values of ϕ_{ref}. The phase reference does not change during the power testing, so the 11 different testing points shown on Fig. 7.16



(a)



(b)

Figure 7.15: (a) Absolute value of the sum total difference in dB between the isolated and closed form small signal representations of the WPT system. The white power contours match Fig. 7.13 and are present for reference. (b) Complete system model closed loop gain for V_{out}/V_{ref}. The zeros and poles are extracted for each transfer function, and the plots show the maximum real portion among all the pole.

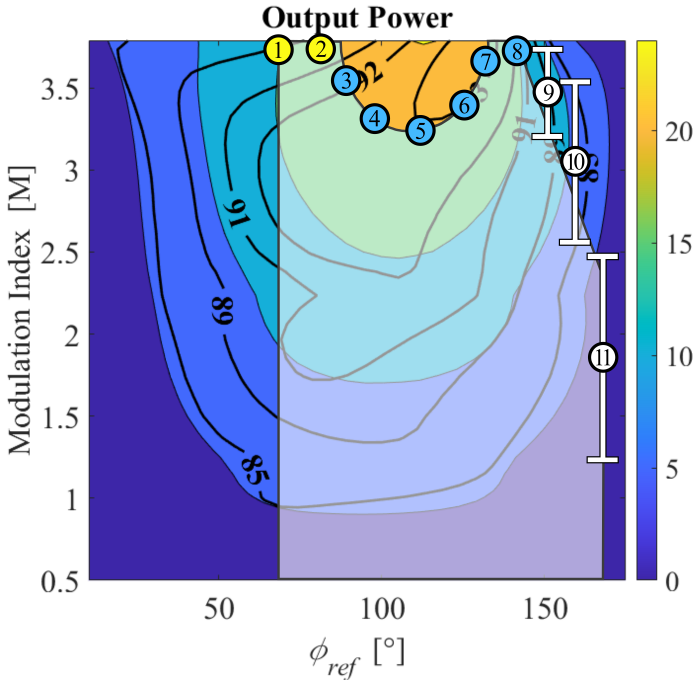
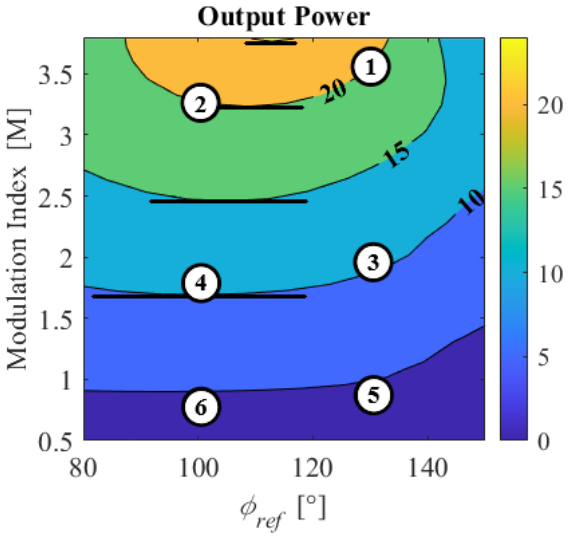


Figure 7.16: Wide range stability testing using the control loops outlined in Fig. 7.14. Each power range is tested with a constant ϕ_{ref}, and points 1-3 saturate before 20 W, points 4-8 reach 20 W, and points 9-11 go unstable before 20 W.

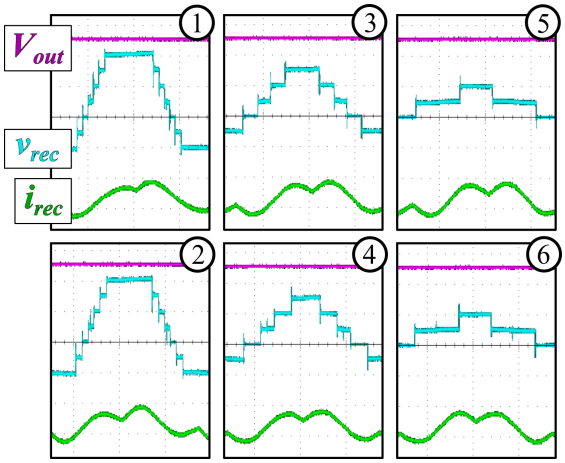
are each have code that is compiled with a different value of ϕ_{ref}. In each case, the power of either saturation or instability is recorded. Points 1-2 on Fig. 7.16 saturate the modulation index prior to hitting 20 W. Their maximum powers are 14 W and 16 W. Points 3-8 all hit 20 W without saturating or going unstable, and point 8 should not be able to reach 20 W, implying a phase shift likely caused by sensing misalignment. Lastly, points 9-11 each go unstable at 15 W, 11 W, and 4 W, respectively. Aside from the phase shift, the data is in good agreement with the stability predictions of Figs. 7.15a and7.15b as they simultaneously predict instability in the top right corner of the power contour plot and stable saturation around $\phi_{ref} = 80°$.

The second experiment is comprised of dynamically changing ϕ_{ref} and output power. Here, the code system is compiled to linearly move from one value of ϕ_{ref} to another, holding value in between moves. Simultaneously, the electric load is varied so that the output power climbs up to 20 W. Using this method, points 1-6 are tested in Fig. 7.17, where Fig. 7.17a shows where the points occur on the power contour plot, Fig. 7.17b shows the steady state rectifier waveforms for the points, and Fig. 7.17c is a oscilloscope screen grab that includes each point and the transients between them. Note that the fast oscillations are the effect of aliasing inherent to zooming the oscilloscope window out for a 20 second screen recording, and the slow oscillations are the system translating back and forth between $\phi_{ref} = 100.1°$ and $\phi_{ref} = 129.2°$.

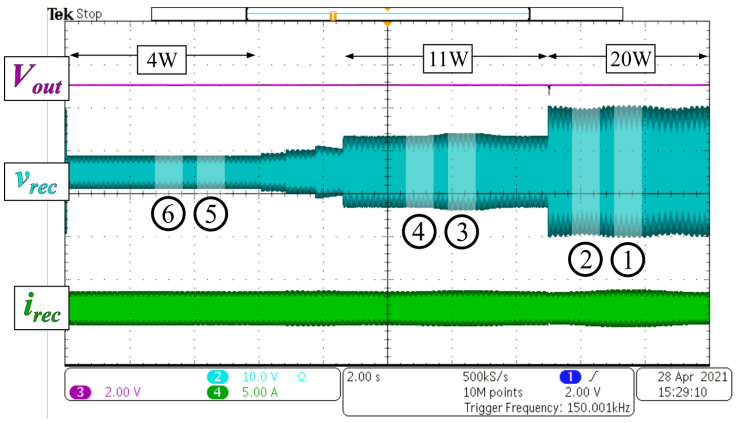
In summary, the issue of cross-coupling in the complete, dual-loop WPT system is outlined in this chapter. Bandwidth decoupling motivates the attenuation of cross-coupling relationships inherent to the system, but the strategy comes at the cost of slowing the



(a)



(b)



(c)

Figure 7.17: Wide operating range test dynamically moving between operating points.

frequency synchronization control loop. The steady state power contours provide intuitive insight into the regions of attenuated cross-coupling affects, regions that incidentally occur along the same trajectory as the high efficiency trajectory for the ideal WPT tuning case. Fig. 7.12 illustrates that designing near zero-slope power contours is a valid strategy even when the primary and secondary sides tuning deviates from the ideal.

Compensators are designed for the entire operating space in Fig. 7.14, and the differences between the isolated control loop designs and the complete, cross-coupled designs are investigated. The poles are also extracted from the complete system model, and the instability regions predicted by these poles shows good agreement with the implied instability regions put for by the model deviation data in Fig. 7.15. Finally, the operating range is tested for both wide loading range stability in Fig. 7.16 and stable, dynamic operating point translation in Fig. 7.17, each of which showcases stability where predicted. The design approach outlined in this chapter enables the dynamic impedance retuning characteristics of the MSC to be used in a real system, demonstrating that frequency synchronization and output regulation can be co-designed for dual-loop wide-range stability including transients as the operating region is traversed.

Chapter 8

WPT System Design

Chapter 3 outlines the proposed WPT system, detailing the modulation actions, loss mechanisms, impedance characteristics, and switching limits. Chapter 4 explains how the state space mathematical framework is applied to the WPT system, and Chapter 5 outlines the experimental platform, validating the earlier analysis and showing how the MSC topology is able to effectively traverse the operating space via impedance control. Designing each of these topics in detail is essential for the WPT charging system, but system-level design is also required to ensure that every topic covered in this work synergizes well upon implementation. This chapter addresses assumptions made earlier in the work and puts forth a design methodology to best choose component, voltage, and control values for optimal efficiency. Furthermore, modulation scheme is addressed in terms of distortion and loss reduction in order to complement the system-wide goals of low-distortion, high efficiency operation.

One very important aspect of system-level design is how the WPT tank is tuned. According to Chapter 5, the primary and secondary sides are tuned at $L_{tx}|C_p = 131$ kHz and $L_{rx}|C_s = 50$ kHz, respectively. This tank tuning both significantly attenuates the third harmonic (under the experimental value of coupling) and showcases the rectifier's ability to compensate for non-ideal tank tuning. The ideal tuning (both sides resonate at the fundamental) requires no reactance injection by the rectifier, an attractive characteristic in WPT systems. Tank tuning is a system-level design consideration, but the experimental WPT system is re-tuned to the near-ideal case ($L_{tx}|C_p = 131$ kHz and $L_{rx}|C_s = 150$ kHz) in Chapter 7 for the purpose of control. It should be noted that the tank retuning assigned in Chapter 7 is also relevant to this Chapter, where the entire WPT system is considered in tandem. Furthermore, unless otherwise stated, the tuning defined in Chapter 7 is used for the duration of the work.

8.1 Voltage and Control Optimization

Capacitor size, control trajectory, and input voltage are all factors that significantly affect the on the efficiency and power density of the WPT system. The tuning capacitors are updated from those presented in Chapter 5 to the values in Table 7.4, resulting in a near-ideal tuning for the WPT tank ($L_{tx}|C_p = 131$ kHz and $L_{rx}|C_s = 151$ kHz). The size of the flying capacitors, however, remains at 15.66 μF and directly influences power density, conduction loss, charge sharing loss, and component count. The control trajectory presented in Chapter 5 is not the optimal, and there is room for design improvement in terms of

modulation and phase control relative to power throughput. Given that the primary and secondary sides can communicate in modern Qi systems, the input voltage can be leveraged to regulate power throughput. Each of these items affects the others – the input voltage affects the modulation, and the modulation is a function of the flying capacitance sizes, etc. Therefore, it is pertinent to design these characteristics in tandem.

A brute force optimization technique is used with three inputs: input voltage, modulation index, and control phase. Control phase is the phase of the inverter voltage: the phase shift from rectifier switching to inverter switching dictates the operating point. The use of $\angle v_{inv}$ is convenient because it is an input to the state space system, but within the relevant operating region, any $\angle v_{inv}$ phase is easily monotonically translated to ϕ_{ref} or Z_{rec}. Because of the reduced distortion without any efficiency drop at high powers in Chapter 5, SHE modulation is used here onward in the work. The output voltage remains at a constant $V_{out} = 5$ V. Fig. 8.1 shows the plotted data, highlighting the best points. The data density is intentionally higher near the optimal region to increase the resolution of the results.

The optimal points of Fig. 8.1 are programmatically extracted and fit lines are generated in Fig. 8.2. The optimization data shows that input voltage and modulation index scale with output power, while the inverter voltage phase remains relatively constant. The modulation index scales more quickly at lower powers and tapers off above ≈10 W. The fit lines are used to generate a set of optimized test points for closer inspection. These test points are shown in Fig. 8.3.

Fig. 8.3 shows the optimized data points and resulting experimental data compared to best η trajectory of the fundamental model. The best loading trajectory of the fundamental

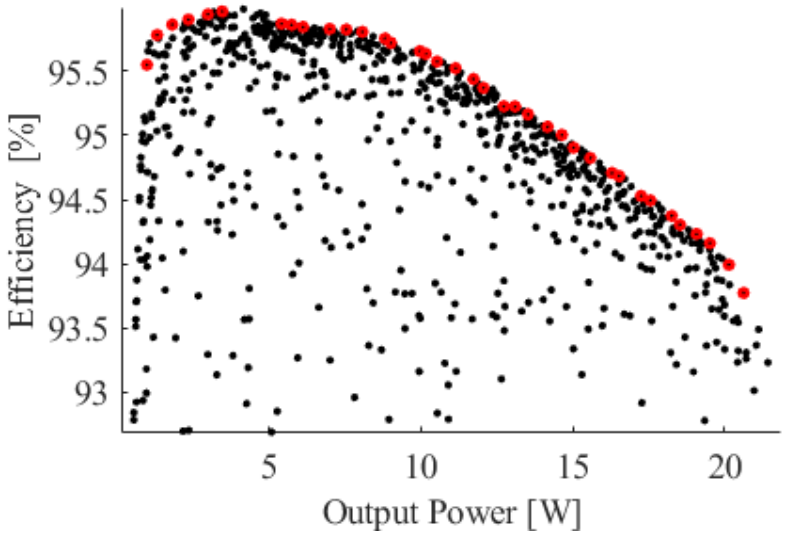


Figure 8.1: Optimization of modulation index, control phase, and input voltage for the experimental system with 15.66 μF.

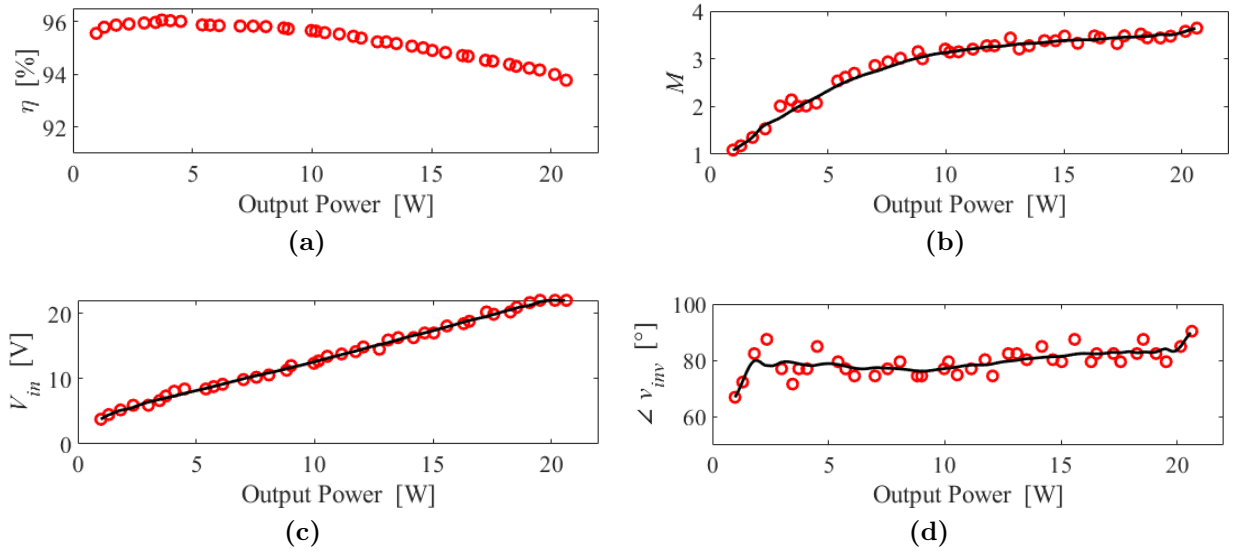


Figure 8.2: Results of the optimization. The best data is extract and fit lines are assigned for (a) system efficiency, (b) modulation index, (c) rectifier phase, and (d) input voltage.

model is found for both $V_{in} = 18.49$ V (to match the data in Chapter 5) and ΔV_{in} (to match the optimization in Fig. 8.1). Neither version of the FHA model accounts for switching losses, only fundamental tank loss. Each of these three trajectories is then plugged into the complete state space model, accounting for tank non-linear ESRs, switching loss, and harmonics.

The efficiency data in Fig. 8.3 illustrates that the optimization of the complete loss model is driven mainly by the WPT tank, as the optimal trajectory matches the FHA ΔV_{in} trajectory for the majority of the power sweep. This is reinforced by the rectifier impedances shown in Figs. 8.3b and 8.3c. The FHA $V_{in} = 18.49$ V trajectory shows significantly poorer efficiency at lower power, signifying that variable input voltage is essential for highly efficient power transfer at lower powers. However, both FHA trajectories deviate from the optimal above 15 W, where Fig. 8.3d shows that each is driven into saturation and is prevented from reaching 20 W. Neither FHA model predicts that 20 W power transfer is possible given the tank design. Notably, the $V_{in} = 18.49$ V trajectory briefly bests the ΔV_{in} model above 15 W, something that is not possible based on the fundamental circuit alone.

The optimization circumvents pushing the system into saturation, recognizing that a more efficient route to 20 W output is possible. The experimental data in Fig. 8.3a is taken to match the optimized trajectory and shows good agreement. Figs. 8.3d and 8.3f prove that the optimization is correct: the experimental system is capable of reaching 20 W without saturating the modulation index. The highest power point on Fig. 8.3a experimentally demonstrates 19.86 W at 92.94% efficiency.

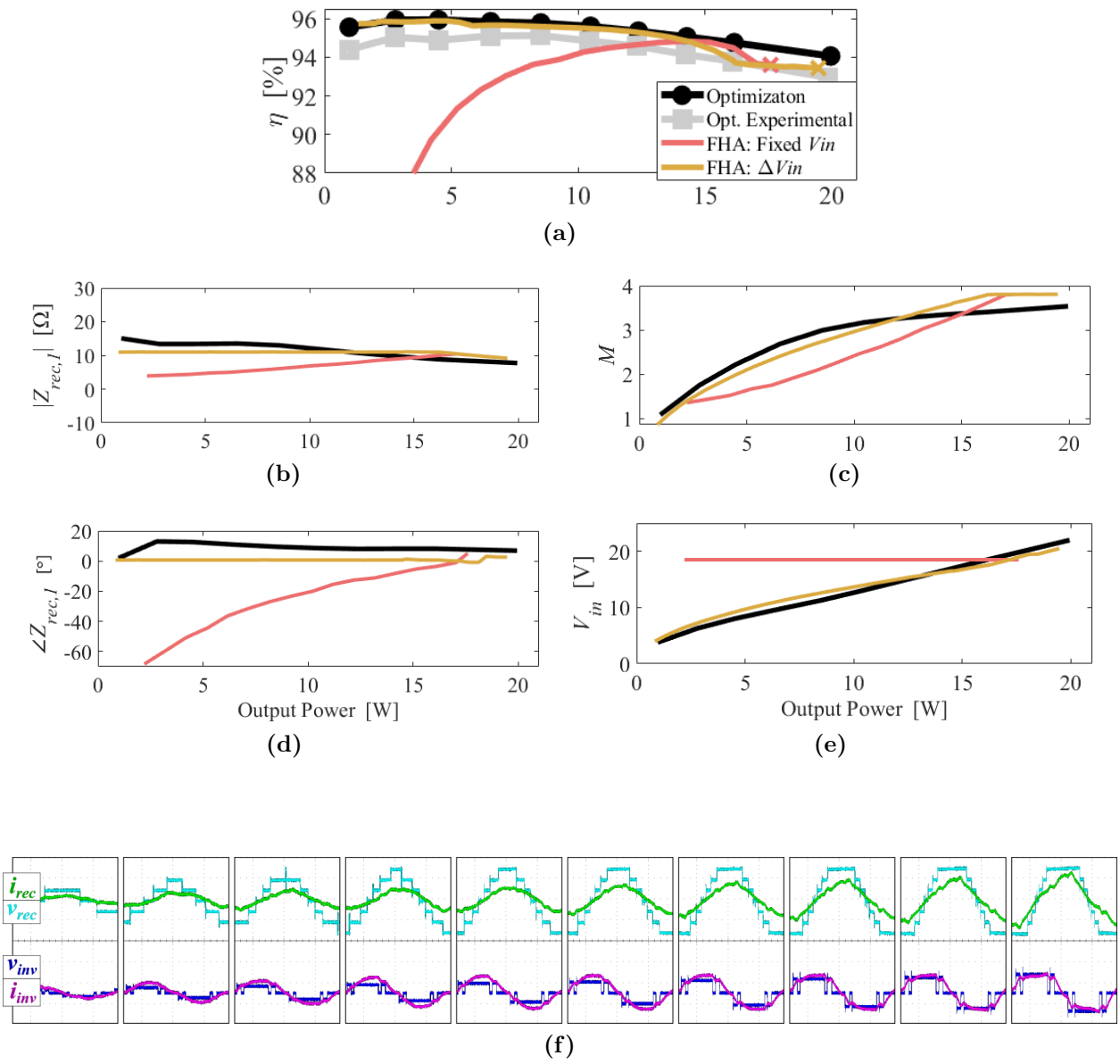


Figure 8.3: Optimized model trajectory as compared to the best η trajectory of the fundamental circuit. The (a) efficiency plot compares the optimal to the first harmonic approximation circuit with v_{inv} both fixed and varied. The rectifier impedance (b) magnitude and (c) phase are listed as well as the (c) modulation index and (e) DC inverter voltage. The (a) efficiency plot shows test results in good agreement with the model. The experimental waveforms are given in (f).

8.2 Capacitance and Footprint Area

The results in Fig. 8.3 do not consider the effect of C_{xx} sizing. For simplicity, this thesis uses only the C1608JB1A226M080AC capacitor presented in Chapter 5. The C1608JB1A226M080AC is a 0603 package, measuring 1.6 x 0.8 mm length and width with 0.8 mm height. It has a nominal capacitance value of 22 μF, but in Chapter 5 the impedance analyzer reports 15.66 μF with a 1.39 mΩ ESR value under a 5 V DC bias for a group of 4 devices in parallel. This means that each individual capacitor is 3.915 μF with a parasitic ESR value of 5.56 mΩ. This section evaluates the footprint impact of reducing the count of capacitors in the circuit. For simplicity, values 4, 8, and 16 μF are used to refer to the cases with a single device (3.915 μF), two devices (7.830 μF), and four devices (15.660 μF), respectively.

The 0603 footprint is small (1.6 x 0.8 mm, or 1.28 mm^2), but the 16 μF MSC design uses 39 of them for a total area of 49.92 mm^2. Assuming an IC chip size of 4 x 4 mm, the capacitors require more than three times the footprint area of the IC itself. Fig. 8.4 aids in visualizing the size of an IC layout and the accompanying capacitors for implementation in a consumer device. The total footprint area is significantly impacted by the size of the flying capacitance in the MSC design. Scaling the output capacitance linearly (at roughly $C_{out} = 4 \cdot C_{xx}$) and reducing the capacitance from 16 μF to 8 μF, the footprint area is reduced by almost 37 %. Further reducing C_{xx} to 4 μF results in a total footprint reduction of 56.3 %, at which point the sum total footprint of the MSC capacitors (12.8 mm^2) is less

than the IC itself (16 mm^2). Fig. 8.4d illustrates the total component areas compared to one another for each of the three designs.

8.3 Capacitance and System Efficiency

The optimization technique for $\{M, \angle v_{inv}, V_{in}\}$ is again leveraged here. The flying capacitor size is changed for each iteration of the analysis, and the parameter values of the 4, 8, and 16 μF designs are listed in Table 8.1. The modulation index and input voltage trajectories are nearly identical, showing that the optimal loading trajectory is almost exclusively a function of the tank design, driven by reducing the system-wide conduction losses. The efficiencies shown in Fig. 8.5a do not reduce linearly with C_{xx} sizing. Rather, they are heavily influenced by charge sharing loss, which is a function of the square of the voltage ripple on C_{xx}. This is evidenced in Fig. 8.5d, where the charge sharing loss increases very significantly as the capacitance size is reduced. As exemplified by Fig. 8.5a, the modeled 20 W efficiencies for the 16, 8, and 4 μF designs are 94.1, 92.7, and 89.3 % efficient, respectively.

Figs 8.5 and 8.4 considered in unison highlight the design challenge associated with choosing the size of C_{xx}. As more capacitors are added, the efficiency increases but the power density is reduced. The opposite happens as capacitors are removed. There is no clear best solution, as a quantifiable optimal does not exist. Rather, the size of C_{xx} is a function of the system specifications. Take a 2 W loss allowance for example. If a consumer device design requires 2 W or less to safely operate, then either the 4 μF design is removed, or the 4 μF design cannot be operated at full power. Thereafter, it is the choice of the

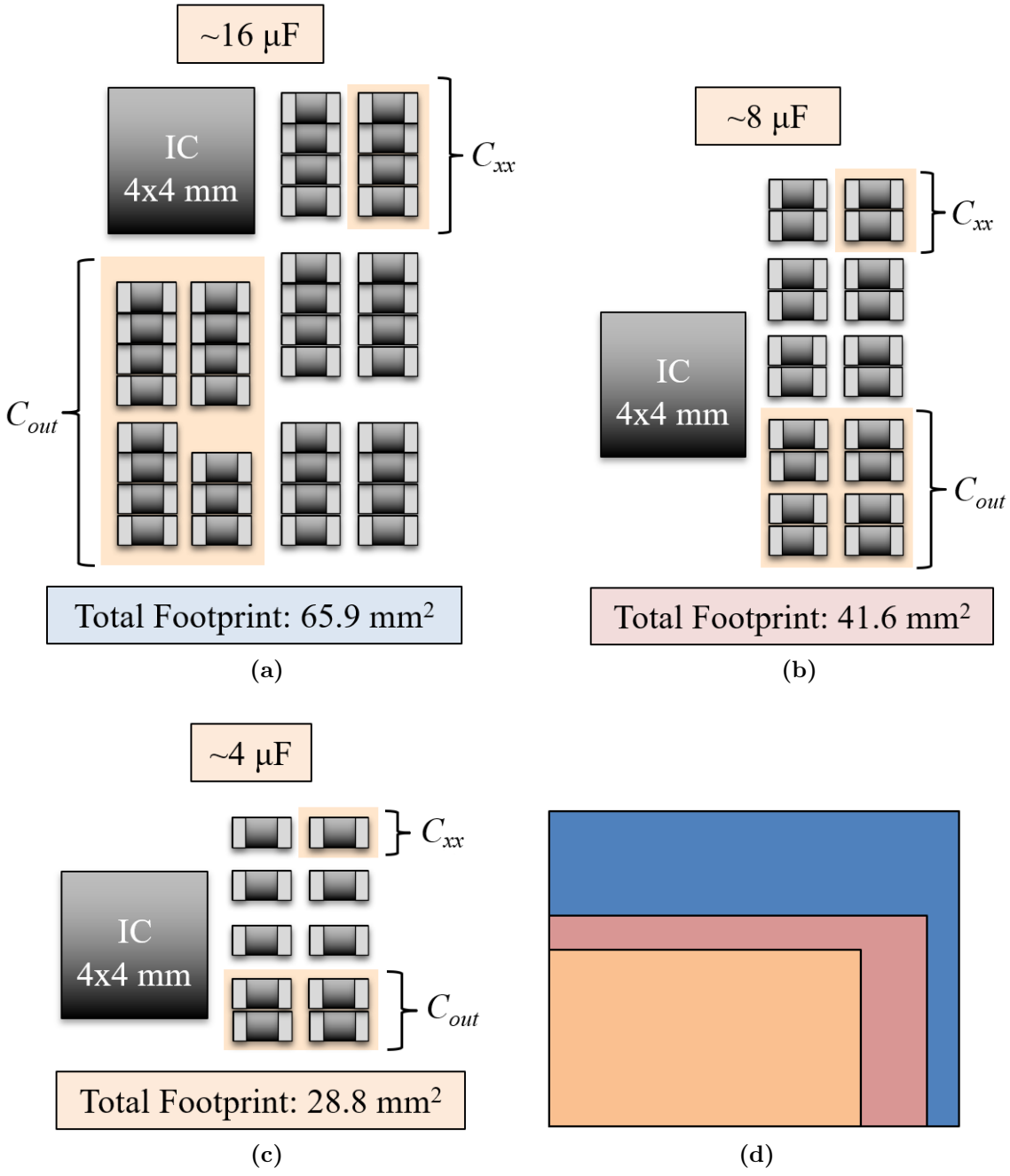


Figure 8.4: Assuming a 4 x 4 mm IC design, to scale component sizes for the (a) 16, (b) 8, and (c) 4 μF designs are shown. The sum total component areas are visualized in (d).

Table 8.1: Optimization Capacitance and ESR Values

	$4\mu F$	$8\mu F$	$16\mu F$
Actual C_{xx}	3.92 μF	7.83 μF	15.66 μF
C_{out}	15.66 μF	31.32 μF	62.64 μF
ESR C_{xx}	5.56 mΩ	2.78 mΩ	1.39 mΩ
ESR C_{out}	1.39 mΩ	0.70 mΩ	0.37 mΩ

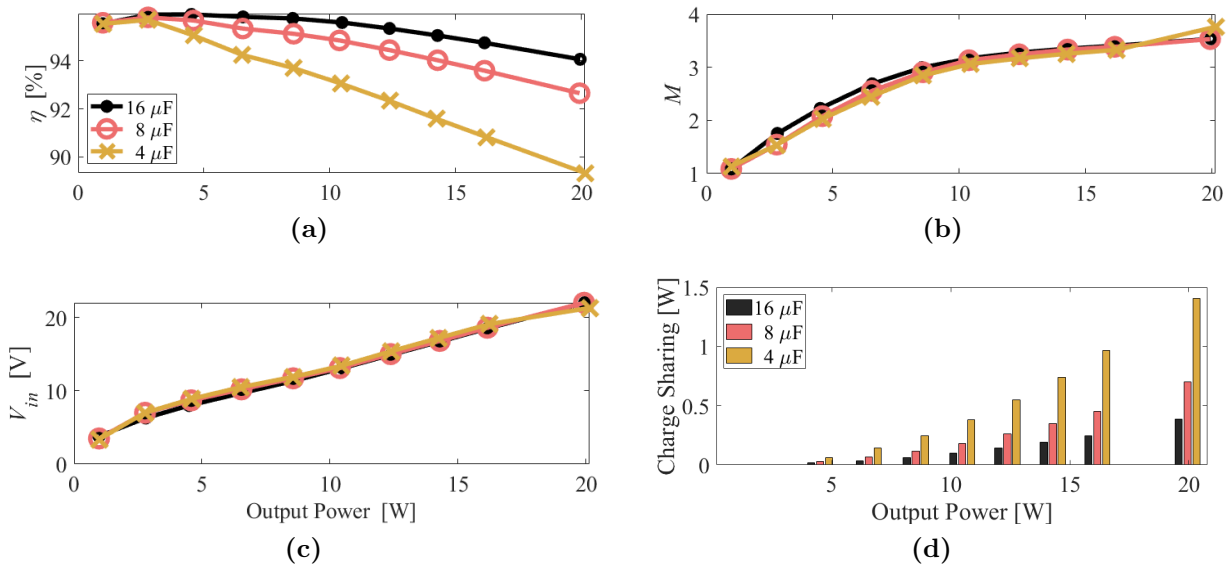


Figure 8.5: Comparison of optimized efficiency trajectories for 4, 8, and 16 μF flying capacitance designs showing (a) efficiency, (b) modulation index, (c) input voltage, and (d) charge sharing loss.

engineer to decide between the 8 and 16 μF designs depending on how important the space and loss savings are. If the only constraint is to keep the losses below 2 W, then the higher power density design is likely best, and the 8 μF case is chosen.

The system-wide efficiency optimization in Fig. 8.3 illustrates that higher efficiencies are attained relative to the initial presentation in Chapter 5. The gains especially manifest at low power where switching losses are significantly reduced with lower values of V_{in}. These gains are the effect of leveraging each controllable parameter in order to minimize loss. Furthermore, optimizing these three parameters $\{M, \angle v_{inv}, V_{in}\}$ for multiple sizes of C_{xx} showcases the significant efficiency roll off associated with flying capacitor ripple. The design of flying capacitance demonstrates sizeable impact on both efficiency and power density. There is no closed-form optimal relationship between flying capacitance and efficiency, but there is a defined relationship. In the examples put forth in this Chapter, for instance, the 4 μF design cannot reach 20 W output power and simultaneously maintain $<$ 2 W of loss. This relationship (between efficiency and size) motivates an investigation into MSC modulation control.

8.4 Modulation

The modulation index of the rectifier directly affects the distortion, loading, and efficiency of the WPT system. The modulation strategy is considered a significant aspect of system-level design. The distortion of v_{rec} is a function of how the MSC levels are inserted into the system, thereby influencing the system-wide distortion via the power currents. Furthermore,

the trade offs between rectifier size and efficiency are directly related to capacitance size via the avenue of charge sharing loss. Because charge sharing loss is a function of capacitor ripple, there is an opportunity to insert extra switching actions (and consequent extra switching loss) into the modulation scheme in order to reduce charge sharing loss and increase system-wide efficiency. Low-distortion modulation is investigated first, followed by a modulation technique to increase efficiency.

8.4.1 Low THD Modulation

The distortion associate with a given modulation index impacts the system efficiency. Multilevel converters are known to provide advantages in terms of distortion reduction and elimination of specific harmonics [115–117]. This work, however, focuses on reduction of the sum total distortion through the 7^{th}, neglecting solutions that may see specific harmonics minimized and focusing on the lowest net distortion.

In general, the seven level staircase modulation of the MSC topology is significantly lower in waveform distortion than a square waveform. However, given a certain fundamental component, a square wave has only a single design variable: amplitude. In the case of the multilevel switched capacitor rectifier, there are multiple switching schemes that result in a desired fundamental component. Because the WPT system is mainly loaded by the fundamental component, the ideal switching scheme would leverage each of the MSC levels in order to produce the lowest possible THD_7 waveform for any given fundamental component.

Then the topology can load the system with a range of fundamental components ranging from $0 < M < 3.81$ with certainty that distortion is minimized.

To determine the optimally low distortion modulation scheme, the first tool to develop is the closed form equation for calculating the harmonic components of each 7-level staircase waveform. In this model, each modulation level is considered constant, and dead times are ignored. The resulting period-long waveform is a combination of DC intervals, the effect of any one of which is calculated with

$$h_{ni} = \frac{V_{dc}}{n\pi}\left(\cos\left(\frac{n2\pi t_1}{T_s}\right) - \cos\left(\frac{n2\pi t_2}{T_s}\right)\right). \tag{8.1}$$

The notation h_{ni} is the contribution to harmonic number $n = \{1, 3, 5, 7...\}$ for the i^{th} interval with voltage value V_{dc}, meaning that the sum of all h_{1i} gives the fundamental, the sum of all h_{3i} returns the 3^{rd}, etc. A Matlab code is constructed to sweep all modulation index combinations to search for those that share a single fundamental component. A desired fundamental component is specified, and the code base leverages (8.1) to return every combination of level 1, 2, and 3 duty cycles that create the desired fundamental component. Thereafter, the 3^{rd}, 5^{th}, and 7^{th} harmonics are calculated using (8.1), and the THD_7 is calculated. Fig. 8.6 shows the result of this analysis, plotting the values of THD_7 with respect to the color bar. The triangle shape is a function of inherent limits to the modulation scheme: the level 1 duty cycle can never be higher than the level 2 duty cycle, and level 2 cannot be higher than level 3. Fig. 8.6 shows a clear best result near the middle of the data set, wherein the distortion value approaches 5%.

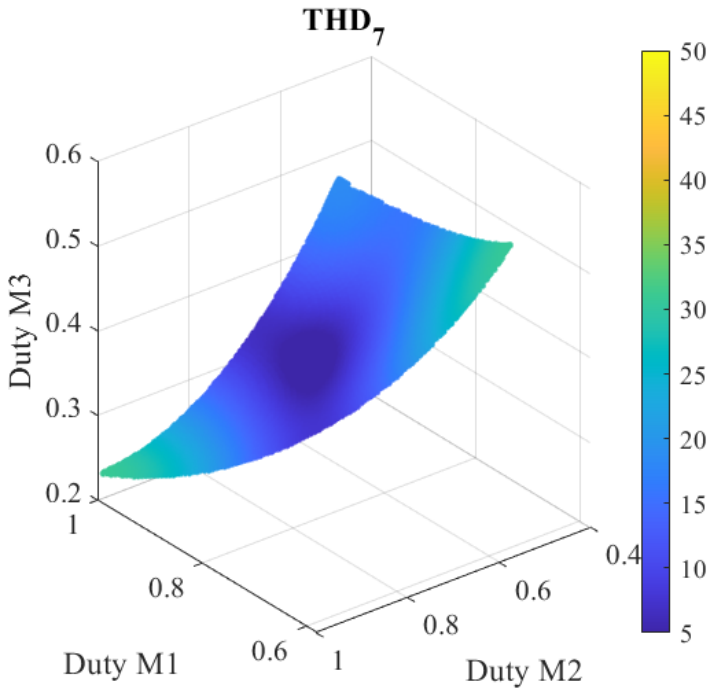


Figure 8.6: Every modulation scheme and its accompanying THD_7 that gives a specific fundamental component.

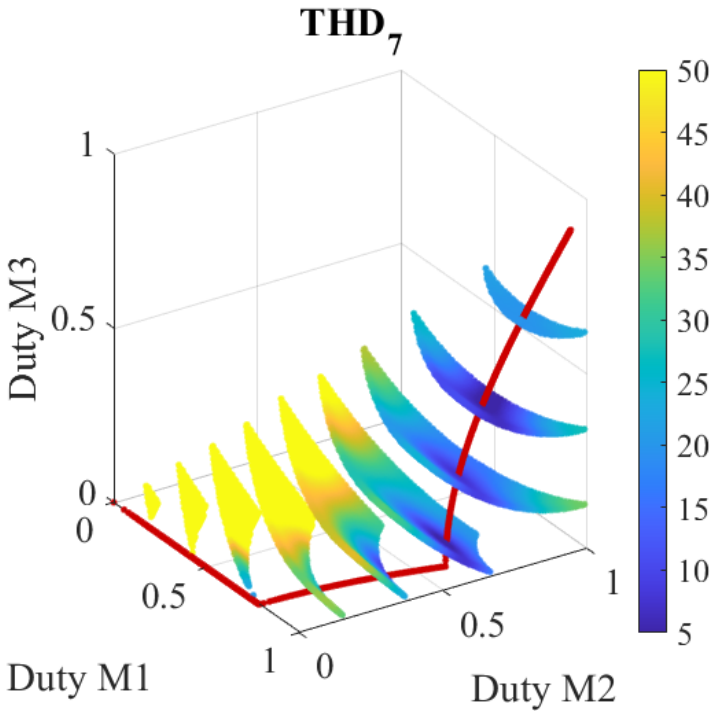


Figure 8.7: Optimal modulation scheme for harmonic reduction through the 7^{th} component: the red line is a digitized sinusoid.

This analysis is expanded to incorporate multiple fundamental values, each represented by a colored sheet in Fig. 8.7. For each sheet (single value of $v_{rec,1}$), a clear best modulation scheme is visible. The red line through the sheets in Fig. 8.7 is the digitized sinusoidal modulation trajectory outlined in Section 3.4. The design idea presented in Section 3.4 is that digitizing a sinusoid produces less harmonic distortion, and the analysis in Fig. 8.7 validates the assumption, proving the modulation trajectory to be the low-distortion optimal. Lowering distortion is valuable for both mitigating potential filtering needs near the WPT coils and for inadvertently increasing efficiency by reducing conduction loss (via either fewer lossy filter components or less I^2R loss due to non-linear coil ESRs). With the optimally low THD_7 modulation identified, the concept of reducing loss via modulation scheme is now expanded to include additional switching actions to address a dominant loss mechanism in highly power-dense designs: charge sharing loss.

8.4.2 Gap Modulation

When rectifier capacitance is reduced, the charge sharing loss quickly begins to dominate the loss profile of the system. Fig. 8.5d shows the dramatic increase in charge sharing loss as the system capacitance, C_{fly}, is decreased from 16 μF to 4 μF. The trade off of the increased loss is that the converter size is reduced (and the power density improved) by greater than 50%. Thus, the relationship between power density (size) and efficiency is a system-wide consideration. Therefore, a modulation scheme that potentially improves this relationship and offers higher efficiency for a given power density is a system-wide improvement.

There is an opportunity for these higher power density designs to see reduced charge sharing loss by leveraging additional switching actions. The charge sharing loss is large because the small capacitance results in large voltage ripple as the power current flows through each flying capacitor. The voltage ripple on each capacitor translates to charge sharing loss via $1/2C_{xx}\Delta V^2$, thus reducing the squared term (voltage ripple) is paramount to increasing efficiency.

The voltage ripple is redistributed each time the flying capacitors are connected in parallel with the output capacitance. By adding switching actions in the middle of the modulation scheme, the ripple on each flying capacitor can be split into two sections. Because of the squared voltage term, calculating $1/2C\Delta V^2$ twice using half the original value of ΔV is less lossy than one instance of charge sharing loss with the original value of ΔV.

This motivates gap modulation: an approach that sees C_{x1} and C_{x2} connected to the output during the middle of their active half period. The basic operation waveforms are shown in Fig. 8.8 where the modulation index decreases from $v_{rec} = 3$ to $v_{rec} = 1$ during the middle of the half period as the two higher level flying capacitors are shorted with the output. For this simplified example, a 2 A secondary current is assumed to be purely sinusoidal, and the ripple on second flying capacitor is shown to approach $V_{out} = 5$ V during the gap.

With this approach, the fundamental limitation of $\tau = RC$ must be considered. Ideally, the charge on the capacitors redistributes instantaneously, but in a real circuit, the redistribution current must flow through device on resistances and PCB parasitics. In Fig. 8.8 the limited rate of charge distribution is pictured. The time constant sets a minimum useful gap length, t_{gap}. Ignoring PCB parasitics, the worst case τ is derived using the circuit

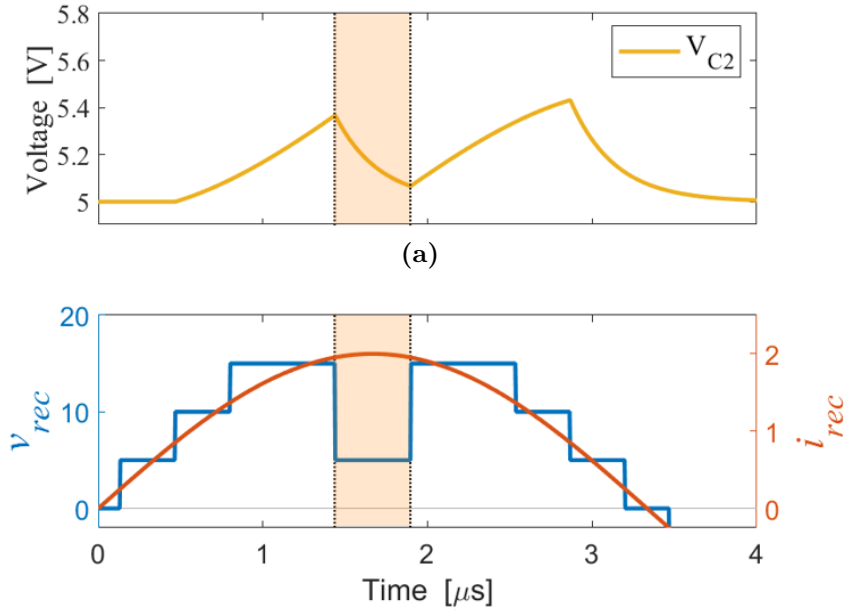


Figure 8.8: Example gap modulation showing (a) the voltage ripple on the level two capacitance and (b) the modulation index with a $v_{rec} = 1$ interval in the middle.

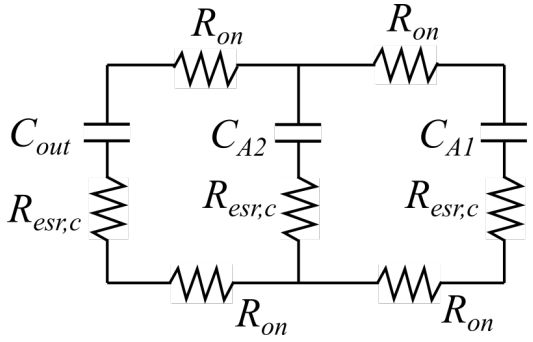


Figure 8.9: The equivalent circuit used to calculate the worst case τ through C_{x1}.

shown in Fig. 8.9:

$$\tau_{wc} = C_{x1}(4R_{on} + 2R_{esr,c}). \tag{8.2}$$

An interesting observation is ascertained here: reducing C_{fly} also reduces the minimum effective t_{gap}, implying that gap modulation compliments higher power density designs.

With the values in the 4 μF system, $\tau_{wc} = 164$ ns. This means that for about 95% charge redistribution, t_{gap} must be $\approx 3\tau_{wc} = 493$ ns, or about 14.8% of a 150 kHz half-period. This analysis helps describe a practical the lower limit of gap modulation, but other significant trade offs exist as t_{gap} is increased (implying a soft upper limit). First, the insertion of the gap reduces the fundamental component, $v_{rec,1}$. This is easily illustrated by (8.1), where the sum total of all modulation intervals is considered. Fundamentally, the insertion of a t_{gap} replaces a segment of $V_{dc} = 3$ V operation with a segment of $V_{dc} = 1$ V operation, thereby lowering the total fundamental component when all intervals are summed. This is equivalent to a reduction in the maximum value of modulation index, M. A lower fundamental component changes the steady state operating point and introduces more distortion into the system (navigating away from the optimal THD_7 trajectory identified earlier). These factors push the size of t_{gap} lower.

The byproducts of t_{gap} insertion are illustrated in Fig. 8.10, where varying gap sizes are plotted along the x-axis in terms of the 150 kHz fundamental period. The rectifier current and input phase are once again assumed constant. As the gap length is increased, Figs. 8.10a and 8.10b show the distortion getting worse as the harmonic values change and the fundamental value increases. Fig. 8.10c shows how the output power is changed under due

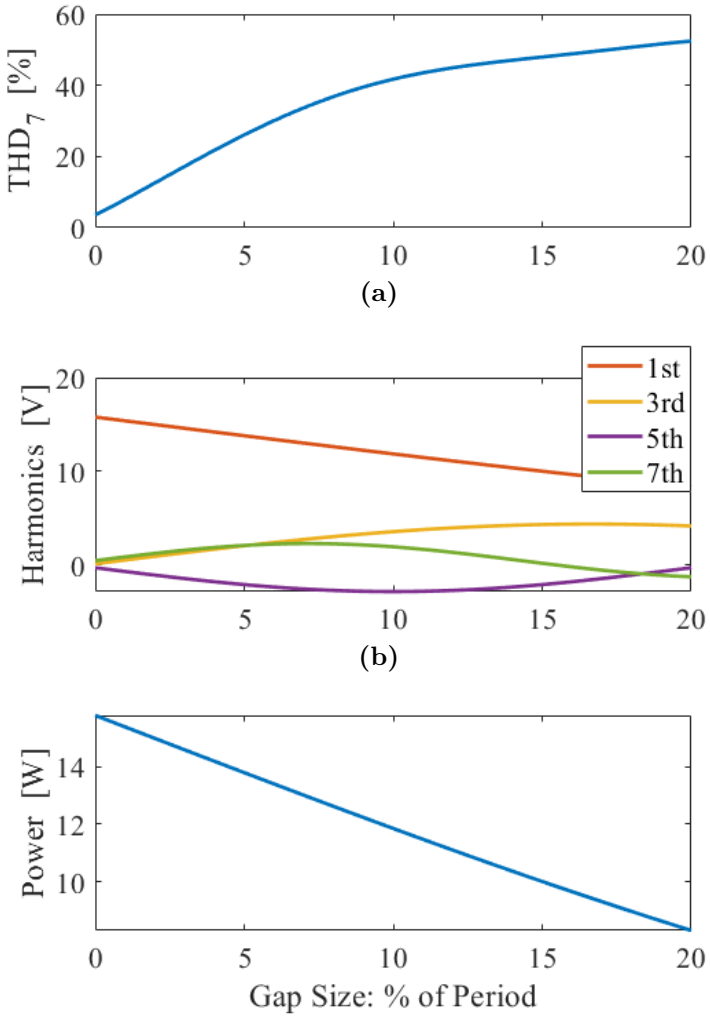


Figure 8.10: Assuming a fixed $i_{rec,1} = 2$ A and $Z_{rec} = 0$, the insertion of various sizes of t_{gap} affects both the (a) THD_7 of v_{rec} by changing (b) the components of v_{rec} and (c) the output power of the system.

to the constant current and diminishing rectifier voltage. Fig. 8.10 describes the dominant system-level trade-offs, but the illustration is far from precise. In reality, the THD, efficiency, rectifier currents impedances, charge sharing losses and steady state operating point all affect one another. They must, therefore, be considered in-tandem for precisely accurate results.

Assuming the gap modulation is small may enable sufficiently accurate sequential analysis, but this assumption is akin to reducing the value of τ. A small t_{gap} value will be limited in its effectiveness at reducing loss. This leads back to in-tandem consideration of the distortion, efficiency, loading, and output power characteristics. For this reason, t_{gap} is included as a variable in the optimization from Chapter 8. The optimization is now run with four inputs such that: $\{M, \angle v_{inv}, V_{in}, t_{gap}\}$. Not only does this enable simultaneous consideration of dominant circuit characteristics, the intrinsic upper and lower limits of τ are inherently considered when those operating points that display sub-optimal gap length are less efficient.

The analysis of τ for the 4 μF design that returns $t_{gap} \approx 14.8\%$ can be repeated for the 8 μF and 16 μF designs. Not only does each of these designs have less charge sharing loss to begin with, but for the same $\approx$95% voltage ripple convergence, the designs respectively require $t_{gap} \approx 30\%$ and $t_{gap} \approx 60\%$. Therefore, the nominal and gap modulated optimizations are compared only for the 4 μF case, where the efficiency improvement is expected to be the greatest.

Each of the efficiency predictions is tested for experimental validity using the 4 μF prototype. Fig. 8.11 sees the two modeled trajectories compared with the two experimental

trajectories, and unlike the prediction, the experiment shows the two modulation types to be essentially equal in efficiency.

8.4.3 Parasitics

Thus far the parasitic elements predicted by the Q3D analysis in Chapter 5 have not been included in the modeling process. However, insertion of those parasitic elements into the modeled data from Fig 8.11 affects the predictions. Fig. 8.12 shows the same experimental data compared to modeled trajectories that include parasitic resistance and inductance.

The parasitic resistances and inductances are inserted node-by-node into the state space model in PLECS. When the parasitics are added to the model, the value PCB ESR value of R_{rec} is removed to avoid "double counting" parasitic resistance. The output capacitance is split into 3 capacitors – each in parallel aside from parasitic resistance. The sum total number of states in the system is now 37 after the additional parasitic inductances are included. One might expect the efficiency of the gap modulation to be decreased because of how the parasitics effect charge redistribution (effectively, τ). However, Fig. 8.12 shows that the main change is an efficiency increase in the nominally modulated trajectory.

The inserted parasitic inductance serves to both slow the charge redistribution (increasing τ and making the gap less effective) and reduce the peak charge redistribution current (reducing I^2R loss). With higher voltage ripple, this charge redistribution current is highest in the nominally modulated case, meaning that a reduction in peak current disproportionately benefits the nominally modulated case. The sum total of the two effects

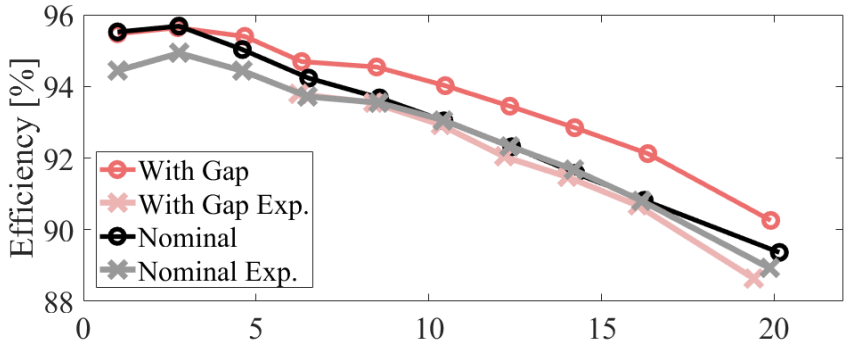


Figure 8.11: Comparison of modeled and experimental optimized trajectories for the 4 μF rectifier design.

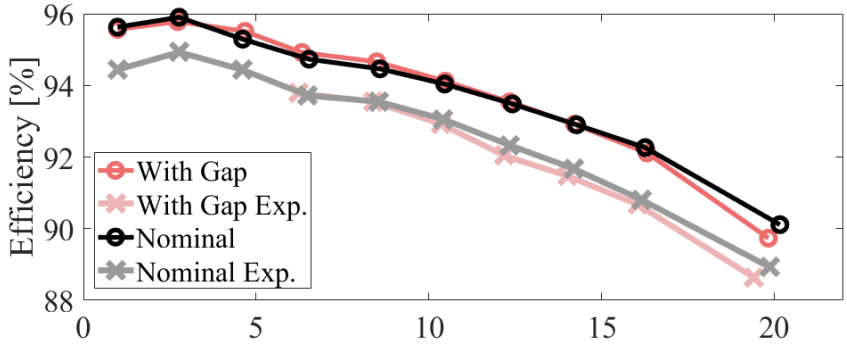


Figure 8.12: Comparison of modeled and experimental optimized trajectories for the 4 μF rectifier design. Here, the model includes individual parasitic elements in the rectifier PCB.

roughly cancels out for the gap modulated case, but the result is a net increase in efficiency for the nominal case.

While there is a small discrepancy between the modeled and measured efficiencies, they data sets now accurately showcase a negligible difference between the two control techniques. Because charge redistribution time and loss are both significantly influenced by circuit parasitics, the R and L parasitic elements cannot be neglected when predicting system efficiency differences between modulation techniques. This analysis shows the significance of including circuit parasitics when predicting efficiencies, but a separate experiment is leveraged to show the effectiveness of gap modulation.

8.4.4 100 kHz Gap Modulation

The benefit of gap modulation is highlighted when charge sharing loss dominates the loss profile and when the circuit parasitics allow produce lower peak redistribution currents while maintain fast redistribution times. Given that the circuit parasitcs cannot be changed for the experimental prototype, the benefit of gap modulation is verified by operating the experimental system at a point where charge sharing loss is higher.

The fundamental frequency of the system is reduced to 100 kHz. The main effect of this change is that, because of the longer period, each flying capacitor is exposed to the power current for longer, thereby increase capacitor ripple. This means that charge sharing loss plays a larger role in the loss profile of the rectifier, and decreasing charge sharing loss has a larger positive effect on the efficiency of the WPT system.

The WPT tank is once again re-tuned to accommodate the new fundamental frequency. The tank is tuned such that $L_{tx}|C_p = 91.5$ kHz and $L_{rx}|C_s = 99.7$ kHz. The primary side ESR_{1-7} values are $\{108, 241, 532, 990\}$ mΩ. The secondary side measures $\{91, 237, 532, 992\}$ mΩ. In order to locate the operating trajectories, two optimizations (nominal modulation and gap modulation) are performed with estimated tank ESR and tuning values assigned prior to actual tank hardware measurements. These optimized trajectories are then run with measured tank ESR values and plotted in Fig. 8.13.

For both the model and the experiment, Fig. 8.13 shows that the gap modulated data points are significantly higher efficiency than the nominally modulated data points. This result illustrates the potential benefit: a reduction in overall loss without a change in hardware. Gap modulation is validated as a viable approach to rectifier control, and it is shown to be an option for high power density (low capacitance) designs that suffer from larger values of voltage ripple and charge sharing loss.

However, Fig. 8.13 also shows general discrepancy between the experiment and the model. It is clear that the trends predicted by the model are in agreement with the experiment, but with a $\approx$3% point deviation, the discrepancy should not be ignored. Additional measurements are taken to ensure the validity of the model, namely: waveform comparison, capacitor ripple comparison, and thermal camera heat distribution. When modeled, each of these items is in good agreement with the experiments, so the conclusion is that the data set is well founded and can be used to validate the effectiveness of gap modulation.

System-level design of the wireless power transfer circuitry includes tank tuning (originally put forth in Chapter 7), optimization of the operating trajectory, and consideration

of the MSC modulation scheme. The optimization tests many data points and extracts those that give the highest efficiency trajectory through the operating space. Parameters $\{M, \angle v_{inv}, V_{in}\}$ are the original optimization inputs until an additional input, t_{gap}, is added in order to reduce charge sharing loss for highly power dense MSC designs. Gap modulation is shown to be both sensitive to parasitic components and valuable for reducing loss in designs with lower values of flying capacitance.

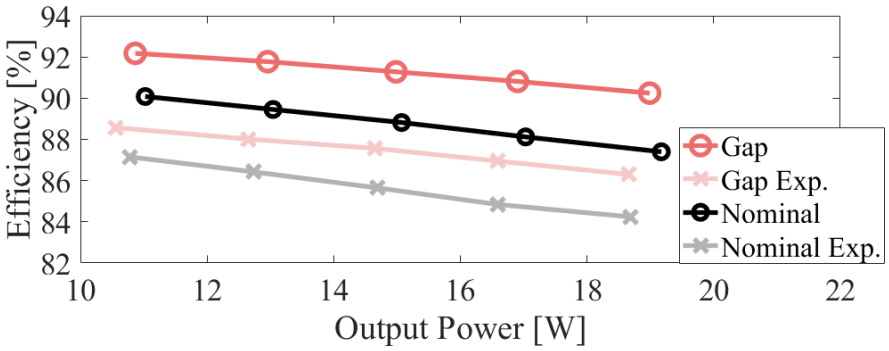


Figure 8.13: Comparison of modeled and experimental optimized trajectories for the 4 μF rectifier design at 100 kHz.

Chapter 9

Future Work: Integration

Future work for the MSC platform is integration onto a chip. Any design to be implemented in a consumer device will be integrated beforehand. IC design is complementary with gap modulation in terms of τ improvement: integration provides opportunity for parasitic elements to be both reduced and more precisely predicted. Furthermore, the discrete devices used in the experimental prototype are 30 V blocking MOSFETs. Depending on the technology employed, the integrated implementation could see lower values of R_{on} than demonstrated in the prototype, an aspect that would both improve efficiency and again improve the attractiveness of gap modulation by lowering τ. Lastly, a real implementation would be connected to a battery at the output DC bus. Contingent on the battery proximity and parasitic elements, the output capacitance of the MSC system may be reduced without significant issue. Insofar as the battery mimics an ideal voltage source across V_{out}, no output capacitance is needed, thereby increasing the power density of the integrated design.

9.1 Conclusions

This thesis motivates, models, and validates the 7-level switched capacitor rectifier as a viable candidate for WPT applications. The MSC rectifier captures the step-up and step-down effects of DC-DC post-rectification stages often implemented in WPT systems. The MSC is able to reduce distortion and tune its input impedance to optimize system-wide efficiency. This thesis contributes a both a system model and experimental platform that show good agreement.

Controlling the MSC necessarily includes the stability of both the output regulation and frequency synchronization feedback loops. This work contributes discrete time plant models for both control problems, leveraging a novel linear projection method to develop the time-to-time transfer function used in the synchronization work. Furthermore, cross coupling interactions are modeled, and a zero-slope power contour method is shown to provide insight into regions of attenuation loop interactions. This analysis is demonstrated to be sufficient for stable wide-range dual-loop operation.

Finally, the state space based modeling technique is used to construct a brute-force optimization strategy. The optimization highlights the best control trajectories for the system – which are heavily influenced by the fundamental tank loading. The charge sharing loss increases dramatically as power density (inversely related to the converter and capacitor sizes) increases, thereby motivating the technique of gap modulation. Predicting the effectiveness of gap modulation relative to the nominal modulation is shown to be

significantly influenced by parasitics, and the future work of incorporating gap modulated analysis is therefore a function of system (and parasitic) design.

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Vita

Spencer Cochran was born in Knoxville, Tennessee in 1992. He received a B.S. degree in electrical engineering in 2015 and a M.Sc. degree with a focus in power electronics in 2017, both from the University of Tennessee. This dissertation characterizes the body of his completed doctoral work at the University of Tennessee, Knoxville.

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At the conclusion of his PhD, Dr. Cochran and his wife, Blakely, relocated to San Francisco to begin a career in the heart of Silicon Valley.