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I am submitting herewith a thesis written by Randall Scott Smith entitled "Development of a Multiplicity Discriminator for High Energy Physics Experiments." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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DEVELOPMENT OF A MULTIPLICITY DISCRIMINATOR FOR HIGH ENERGY PHYSICS EXPERIMENTS

A Thesis
Presented for the
Master of Science
Degree
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Randall Scott Smith
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Dedication

This thesis is dedicated to my wife, Shana, and my parents Doris and Eddy Smith, whose continual support provided me the will to carry on in times of great strife.

Acknowledgments

I would like to thank the many people who have made this work possible. Members of my committee including Dr. E. J. Kennedy, my major professor, Dr. T. V. Blalock, Dr. J. M. Rochelle were instrumental in providing the motivation and valuable instruction to pursue this endeavor.

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Finally, I would like to thank my Lord and Savior Jesus Christ for providing me with the ability and strength to complete this venture and maintain complete sanity. He has always directed my paths and I am eternally grateful.

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Abstract

A current output multiplicity discriminator for use in the front-end electronics (FEE) of the Multiplicity Vertex Detector (MVD) for the PHENIX detector at RHIC has been developed in the Orbit Semiconductor 1.2 μ CMOS, n-well process. Requirements for the multiplicity discriminator include low-power, small area, high speed and common threshold matching. Additionally the discriminator must trigger on input signals ranging from 0.25 MIP(20 mV for the detector) to 5 MIP. Frequency response of the discriminator is such that the circuit is capable of generating an output for every detector beam crossing (105 ns). One channel of multiplicity discriminator occupies an area of 85 μ by 530 μ and consumes 515 μW. Details of the design and results from prototype device testing are presented.

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Chapter 1

Colliders and Collider Detectors

The study of elementary particle physics at high energies has been made possible over the past two decades due to the development of particle colliders. With the increased interest in exploring and explaining subatomic phenomena, the need for higher energy particle colliders has emerged in the physics community. By observing the interaction of colliding particles within selected matter, insight into the fundamental nature of the universe can be gained. There are a variety of particle colliders currently under construction around the world whose designs differ based on the specific particle and phenomena to be observed by the experiment. Each collider is instrumented with several detectors which carry out a specific set of measurements. These measurements are then used to characterize the subatomic phenomena observed. Recent work in the physics community has focused on the investigation of the origins of mass and the crucial issue of electroweak symmetry breaking as predicted by the Standard Model [1]. Evaluation of such phenomena require colliders with energies and luminosities on the order of the canceled Superconducting Super Collider (SSC) and the proposed Large Hadron Collider (LHC) at CERN [2,3]. Several colliders such as the Relativistic Heavy Ion Collider (RHIC) located at Brookhaven National Laboratory (BNL) and Tevatron at Fermilab exist to investigate

lower energy phenomena which is also critical to the further development of the Standard Model [4].

1.1 The Standard Model

The Standard Model is the most complete explanation of elementary particles and their interaction known today [5]. Developed from experimental results, the Standard Model is a quantum theory which includes the theory of strong interaction (Quantum chromodynamics, QCD) as well as a unified theory of weak and electromagnetic interactions (electroweak). To describe the interactions of the observed fundamental forces, the Standard Model defines a set of fundamental particles from which all known matter is composed. These spin-1/2 particles fall into two categories, leptons or quarks. Leptons interact through electromagnetic and weak forces. Quarks interact through electromagnetic, weak and strong forces. The Standard Model also predicts the existence of neutral spin-zero particles known as bosons which allow the transmission of the three fundamental forces.

Although the Standard Model describes many of the interactions observable today, it also raises many questions. For instance, the Standard Model provides no insight into why there are three pairs of quarks and leptons or why the universe contains much more matter than antimatter. Are quarks and leptons really fundamental or do they have substructures? To date the Standard Model provides no means by which a unification theory of strong and weak forces can be established. A truly complete model would require the unification of not only strong, weak and

electromagnetic, but also gravitation forces. Through the use of high energy particle colliders conditions equivalent to those found in the early universe can be established. This being the case, according to Einstein's famous theory of relativity, $E = mc^2$, new matter can be created by the collision of high-energy particles. It is the analysis of this new matter which will enable the questions raised by the Standard Model to be answered [6].

1.2 Particle Colliders

High energy particle colliders exist for the purpose of exploring the interactions of particles at the subatomic level. Existing colliders as well as those currently under construction basically operate on the same principles. Particles are accelerated around a ring comprised of many magnets until they reach the required velocity at which time they are collided within a detector where precise measurements can be obtained. Differences between colliders occur mainly in the maximum obtainable energy and luminosity levels as well as the type of particles to be collided. Modern colliders approach energy levels up to 14 TeV with luminosities on the order of 10^{34} per cm^2(sec) and require hundreds of megawatts of power to operate [7]. Several of these colliders shall be presented as a means of comparing and contrasting the differences among high energy particle colliders.

The desire to explore the compelling physics questions left unanswered by the Standard Model such as electroweak symmetry breaking, supersymmetric particles and top quark properties led physicists more than a decade ago to propose the building of

a super particle collider. From its conception, the Superconducting Super Collider (SSC) was to be powerful enough to guarantee energy levels necessary to characterize these phenomena. The SSC was to be a proton-proton collider capable of energies up to 20 TeV and luminosities on the order of 10^{33} per cm^2(sec) [2]. With an acceleration ring of over 87 kilometers in circumference, the SSC was projected to cost in excess of 10 billion dollars. This high price tag coupled with U.S. cutbacks in government spending led to the eventual cancellation of the project in October of 1993. Cancellation of the SSC left physicists with no available collider having the energy levels needed to guarantee appropriate addressing of electroweak symmetry breaking.

The failure of the U.S. to complete the SSC points to the need for such large scale scientific efforts to be truly international. Such an endeavor is currently underway. In conjunction with the European Community, the U.S. and other countries are participating in the construction of the Large Hadron Collider (LHC) at CERN. Like the SSC, the LHC is to be a proton-proton and heavy ion collider capable of high energies and luminosities. The LHC is comprised of a 27 kilometer acceleration ring designed to operate at 14 TeV of energy with a luminosity of 10^{34} per cm^2(sec) for a proton-proton collision and 1.25 TeV for a heavy ion collision [7]. Due to its lower energy, the LHC does not guarantee the discovery of the mechanism of symmetry breaking as the SSC did. However, the energy level provided by the LHC is 7 times that of the Tevatron, the most powerful existing collider, located at Fermilab [7]. Increased luminosity of the LHC will further aide in the colliders ability

to explore the proposed goals at the cost of increased radiation damage to front-end-electronics (FEE) and a decrease in signal-to-noise performance.

To investigate the subatomic phenomena such as electroweak symmetry and supersymmetry requires the high colliding energy offered by the SSC and the LHC. However, there is still meaningful subatomic physics to be explored at much lower energies. The Relativistic Heavy Ion Collider (RHIC) scheduled for completion in 1999 at Brookhaven National Laboratory (BNL) is one such collider. When completed RHIC will collide heavy ions at an energy of 100 GeV with a luminosity of 2×10^{26} per cm^2(sec) and protons at levels of 250 GeV with a luminosity of 10^{31} per cm^2(sec) [4]. Although the LHC has a factor of 30 times the energy for colliding ions, the increased luminosity of RHIC (for ion collisions) enables it to obtain measurements that would be impossible with the LHC. The performance of RHIC is anticipated to be high enough to create a hot, dense plasma of quarks and gluons. This plasma of quarks and gluons, termed the Quark-Gluon Plasma (QGP), is theorized to be the state the universe existed in for several microseconds after the singularity. As with the larger colliders, RHIC is instrumented with numerous collider detectors enabling precise recreation of subatomic phenomena. Such measurements offer the ability to evaluate the Standard Model to fractions of a percent.

1.3 Collider Detectors

Collider detectors provide the means by which accelerated particle collisions may be measured in a useful manner. Generally, colliders are equipped with several

detectors which attempt to evaluate the subatomic phenomena by using slightly different methods. The differing methods place emphasis on different particles such as electrons, protons, hadrons, muons etc. By utilizing different approaches to measure the particle decay after a high energy collision, a more complete and informative description of the event is obtained. The LHC is composed of two general purpose particle detectors, ATLAS and CMS, and one large heavy-ion detector, ALICE [8,9]. RHIC is instrument with four collider detectors: BRAHMS, STAR, Phobos, and PHENIX [4,10]. Each of these collider detectors contain numerous subsystems required to provide the needed timing, trigger, energy, vertex and momentum information.

The general purpose detectors, ATLAS and CMS, at the LHC are designed to allow the study of a broad range of physics at the maximum luminosities anticipated at the LHC machine [8]. The ability to achieve such high luminosities enable both detectors to provide measurements necessary to explore the pertinent physics questions to be addressed by the LHC. Although slightly different architectures are used, both detectors rely on superconducting magnets to create large magnetic field volumes needed to measure the momentum of energetic charged particles. ATLAS operates with a smaller magnetic field and requires a mixture of discrete high precision and continuous lower precision measurements to provide the required pattern recognition and momentum resolution. CMS takes advantage of the higher magnetic field present and uses a large number of discrete high precision measurements. The methods by which these measurements are made gives both detectors the powerful

vertexing capability needed to reconstruct decaying particles. ALICE, the remaining detector at the LHC, is a dedicated heavy-ion detector. Like the PHENIX experiment at RHIC, the goal of ALICE is to study interacting particles at the large energy densities needed to create the theorized QGP. ALICE will be used to study hadrons, electrons and protons produced from heavy-ion collisions. Embedded in a large magnet operating in a weak solenoidal field, the detector consists of a high resolution inner tracking system, a particle identification array and a electromagnetic calorimeter.

The four collider detectors at RHIC differ in detector size, particle emphasis and experimental goals. Both BRAHMS and Phobos are relatively small detectors. BRAHMS is designed to place emphasis on hadrons over a broad range of rapidity and momentum. Phobos seeks to measure very soft hadrons whose production may offer insights into the QGP. In comparison to BRAHMS and Phobos, STAR and PHENIX are relatively large collider detectors. STAR utilizes hadronic activity to aide in the search for signatures of the QGP. Through the correlation of data obtained on an event-by-event basis, possible signatures can be established. In the search for the QGP and the identification of its properties, PHENIX places emphasis on measuring electrons, photons and muons. Each of the collider detectors presented above consist of subsystems necessary to measure the same fundamental elements: timing, trigger, energy, vertex and momentum. Thus the description of PHENIX subsystems to be presented in Chapter II is applicable to a first order for almost all collider detectors.

1.4 Tracking Systems

Tracking systems in collider detectors provide the means by which particles are located and identified [10]. The ability to determine the position of decaying particles after a high energy collision is a necessity to recording the physics associated with the event. Consequently, tracking systems represent a vital component of every collider detector. Generally, detectors consist of several different tracking systems. Each system is designed to provide high resolution location information needed for pattern recognition. By building tracking systems for specific directions and dimensions more area may be covered, which represents improved resolution and accuracy for the detector. One method of particle tracking involves determining the vertex position of the trajectory particles after a collision. The use of customized front-end electronics (FEE) enables data to be gathered through detectors sensitive to the particles being generated. If the measured data meets certain established criteria, the event is deemed to contain interesting physics and is analyzed further to determine the vertex position.

1.5 Scope of Thesis

The size and complexity of colliders and collider detectors offer many opportunities for challenging electronics design. Integrated circuit technology offers the perfect match for the high channel count, low power and small area constraints presented by FEE of detectors. The bulk of this thesis will explore the design and characterization of a multiplicity discriminator for the FEE of PHENIX's Multiplicity Vertex Detector (MVD) [10,11]. The multiplicity discriminator is a very unique

component. While basically functioning as a comparator (discriminator either fires or has no output), each discriminator provides an discrete current output. When combined with other discriminator output currents, a total current sum proportional to the number of discriminators firing is generated. This data is then factored into the trigger information responsible for determining whether a particular event contained meaningful physics. Carrying out this function of multiplicity discriminator offered several challenging and stringent requirements such as low power, small area, high speed, programmability and radiation resistance. Aspects of the design and layout for the multiplicity discriminator fabricated in a 1.2 μ CMOS process will be presented. Due to the structure and geometry of several devices used in this design an appropriate discussion on device modeling will be given. In addition to the design of the monolithic discriminator, this thesis is also concerned with selecting an appropriate readout amplifier needed to convert the summed current outputs to a voltage suitable for analog-to-digital conversion. The discriminator will be characterized based on the measured performance of fabricated integrated circuits. After the design has been described and the performance characterized, appropriate conclusions on the acceptability of the multiplicity discriminator for use in the MVD and other PHENIX subsystems will be discussed. Due to the importance of the PHENIX detector to the developed electronics to be presented in this thesis, a complete description of the detector subsystems will be presented in Chapter II.

Chapter 2

PHENIX Collider Detector

2.1 Searching for the QGP

As briefly alluded to in Chapter I, the primary goals of the PHENIX collider detector at RHIC are to detect the QGP and measure its properties [10]. It is anticipated that the energy and luminosity of RHIC will be adequate to produce conditions necessary for the forming of the hot, dense plasma of quarks and gluons which make up the QGP. According to the Big Bang Theory, the universe existed as a QGP for several microseconds after the four fundamental forces which govern all physics were established. Figure 2-1 illustrates the relative timing of these forces; gravity, strong nuclear, weak nuclear and electromagnetic, with respect to the singularity and the creation of the QGP. Many potential signatures for the QGP have been suggested in recent years. PHENIX seeks to explore these signatures through the study of both lepton and hadron activity. To accomplish this task, the detector subsystems have been designed to measure a variety of particles at luminosities and resolutions enabling the detection of rare processes. Figure 2-2 is a cross-sectional view of the PHENIX detector illustrating the numerous subsystems required to measure various decaying particles of interest [12].

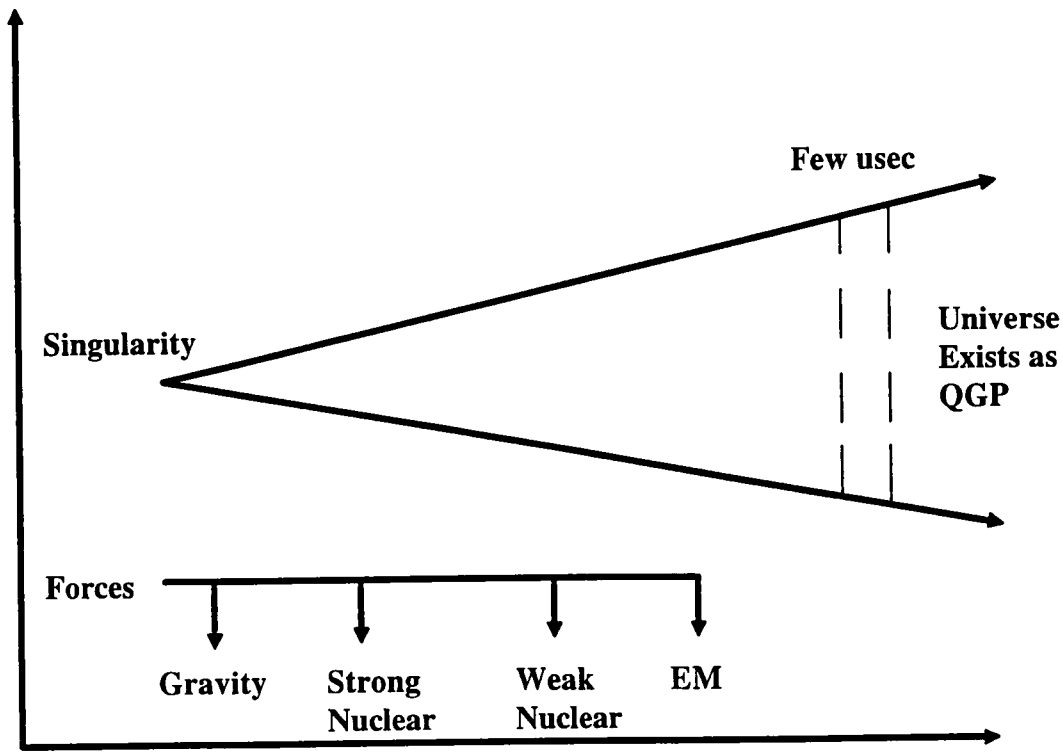


Figure 2-1. First few microseconds after the singularity and relative timing of fundamental forces.

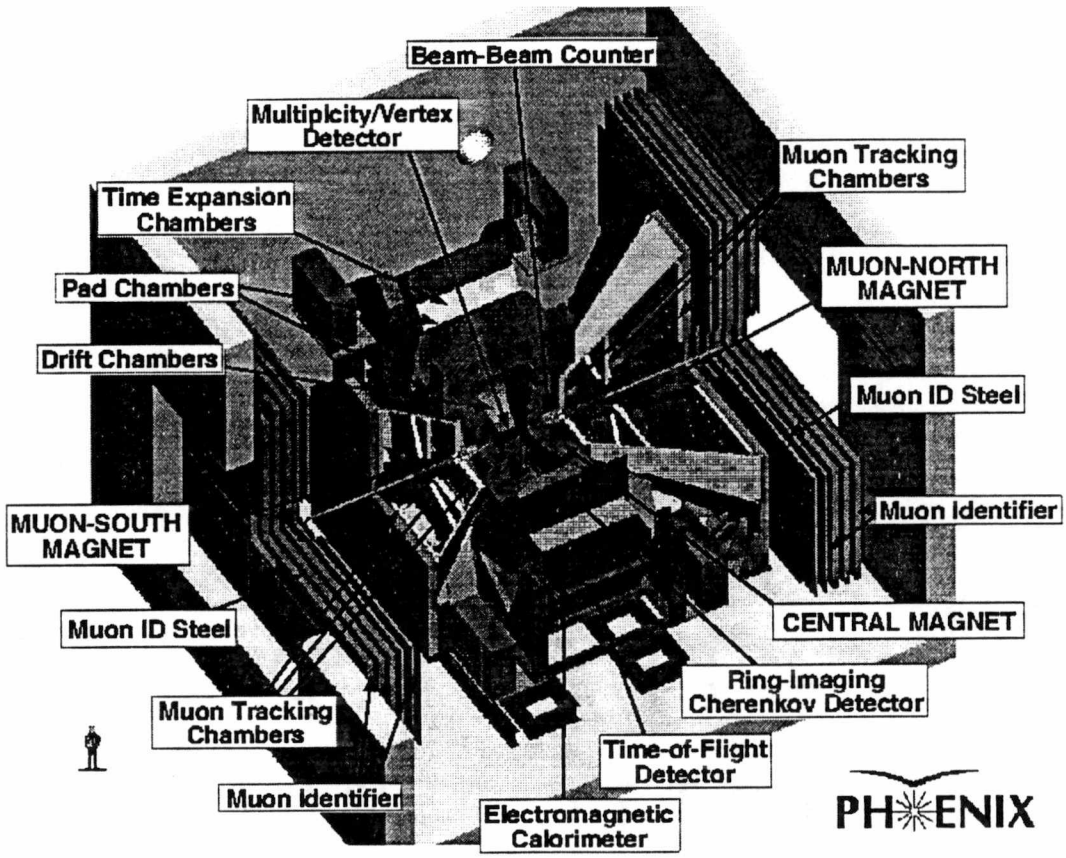


Figure 2-2. Cross-sectional view of the PHENIX collider detector illustrating the relative location of every subsystem.

2.2 PHENIX Subsystems

The PHENIX collider detector is comprised of two central spectrometers for electron, photon and hadron detection as well as a third arm needed for muon measurement. These arms provide the needed particle tracking, identification, momentum and energy measurements required to accomplish the goals established for the detector. In addition to the three arms, the detector also has inner detectors capable of providing start time and vertex location for an event as well as event multiplicity and multiplicity distribution. Figure 2-2 illustrates the relative position of each subsystem within the large superconducting magnets needed to generate the appropriate electromagnetic field strength.

2.2.1 Central Arm

Charged particle tracking and momentum measurements for the PHENIX detector are achieved through a tracking system made up of three components: drift chambers (DC), pad chambers (PC) and a time expansion chamber (TEC). Low mass DC provide accurate particle trajectories needed for pattern recognition. Additionally, the mass of pairs of particles may also be determined from the DC. There are approximately 10,200 channels of DC present in the detector. Three nonprojective PC consisting of over 48,000 channels provide a three-dimensional position measurement used for both pattern recognition and momentum determination. The final component in the PHENIX tracking system for the central arm is the TEC. The TEC consists of

29,000 channels capable of particle identification (electrons from pions) and pattern recognition [10].

Electron and photon energy measurements are carried out through the use of an integrated electromagnetic calorimeter (EMCal). A calorimeter is a device which determines a particles energy by converting its momentum into a measurable form of energy such as light. The main goals of EMCal are to identify both electrons and protons and measure their energy. Calorimetry measurements are made through the use of a medium known as a scintillator. A scintillator is a material that slows particles until their kinetic energy is converted to light energy at which time the energy can be transformed to an electrical signal by means of a photomultiplier tube (PMT). EMCal incorporates two types of scintillators into the detector design; lead-scintillator (PbSc) and lead-glass (PbGl). The roughly 18,000 channels of PbSc offer an inexpensive means to achieve good energy resolution and excellent uniformity. Both scintillators provide the necessary resolution required by the EMCal, although the 10,000 channels of PbGl offer slightly better segmentation.

The final system components for the central arm involve subsystems whose primary goals are particle identification. Although systems such as EMCal provide some particle identification, the main identification system consists of a Time-of-Flight detector (TOF), a Ring Imaging Cherenkov Counter (RICH) and a TEC. TOF is a high resolution detector made up of 1,000 channels capable of identifying charged hadrons over a large momentum range. RICH consist of 6,400 channels and

represents the primary electron identification component of the detector. The previously discussed TEC also provides valuable electron identification information.

2.2.2 Muon Arm

Like the central arms, the muon arm provides system components which allow for particle tracking and identification as well as momentum analysis. Muon arm tracking consists of a DC responsible for measuring the momenta of muons and other charged particles entering the arm. The muon tracking system is divided into three sections which total approximately 20,000 channels. Particle identification for the muon arm is achieved through the Muon ID. Being the outermost subsystem from the collision point of the PHENIX detector, the Muon ID has been designed such that hadronic particles are blocked and only muons remain for detection. The 4,600 channels comprising the Muon ID also serve as the Level-1 trigger for the muon detector.

2.2.3 Inner Detectors

The innermost detector subsystems responsible for measuring start time and vertex of an event as well as event multiplicity and multiplicity distribution consist of a beam-beam counter (BB) and a multiplicity vertex detector (MVD). The primary goal of the roughly 130 channels of BB is to provide precise timing information (50 ps resolution) on the beam-beam collision. Although both components provide a means of vertex positioning, the MVD yields a measurement having a standard deviation of

less than 2 mm while the BB counter is around 2 cm. As illustrated by Figure 2-3, vertex positioning allows the determination of the angle of particle trajectories after a heavy-ion collision. To accomplish the task of obtaining a precision vertex, the MVD utilizes roughly 34,000 channels of silicon strip detectors aligned within two concentric barrels and 6,000 channels of silicon pad detectors to form the endcaps of the barrel. Figure 2-4 is a cross sectional view of the MVD barrel. Within this barrel exists the point at which the particle collision occurs. From the figure it can be seen that the silicon strip and pad detectors provide nearly complete coverage of the beam interaction chamber. This coverage provides a means by which most particles are detected. The concentration of a particle or particles within a given area is often termed the event multiplicity. Multiplicity information is used to provide trigger data for the MVD. If the generated trigger data meets certain established criteria, the event is deemed to contain interesting physics and is analyzed further. Due to the closeness of the MVD to the beam interaction, increased levels of radiation damage are anticipated for the MVD over other PHENIX subsystems. This is especially true with the high luminosities of RHIC at which PHENIX will operate.

The preceding discussion has briefly explained the purpose for each of the subsystems associated with the PHENIX collider detector. From the point of the initial collision within the inner detectors, a position vertex (MVD) and start time (BB) are established. The position vertex provides an initial tracking measurement which is input into the Level-1 trigger. Generation of a Level-1 trigger means the event whose data is stored within the FEE analog memory unit (AMU) is digitized by

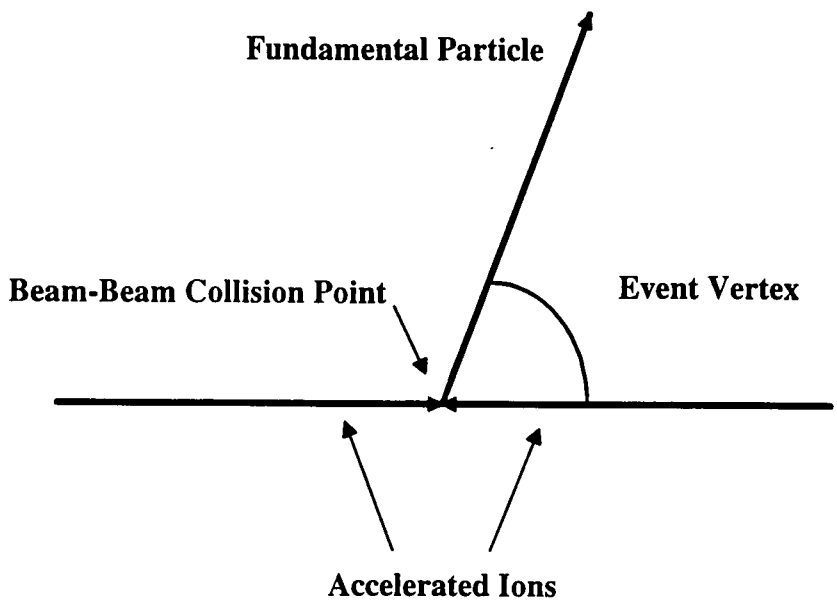


Figure 2-3. Illustration of event vertex positioning as performed by the MVD.

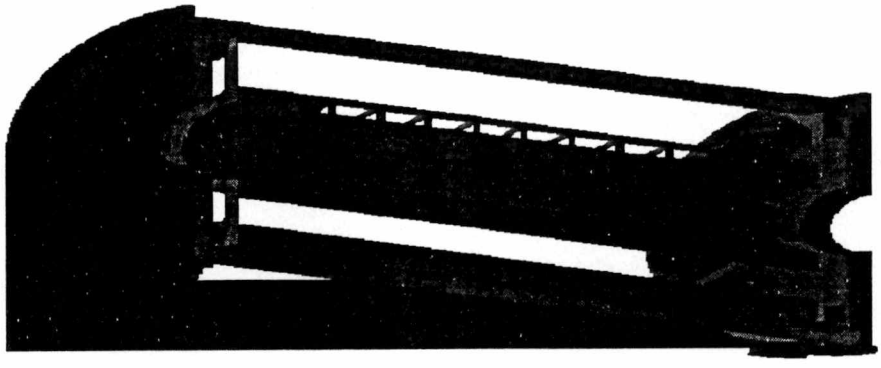


Figure 2-4. Cross-sectional view of MVD barrel where high energy particle collisions occur.

the analog-to-digital converter (ADC). Such an early evaluation of the collected data reduces the amount of processing by eliminating data which does not contain events of merit. After passing through the MVD barrel, the charged particles proceed to the central arms of the detector. Once in the central arms, DC, PC and TEC become responsible for providing the particle tracking while EMCal circuitry measure electron and photon energy. Although several systems such as EMCal provide particle identification, RICH and TOF are the components responsible for most identification. Overlapping subsystems further enhance the performance of PHENIX. Particles reaching the muon arm are tracked by muon DC and identified by the Muon ID system. System components of the PHENIX detector provide the coverage and flexibility necessary for accurate measurements needed to detect the QGP. Nearly 200,000 channels of FEE and 500 tons of magnets occupying an area of several thousand square feet are required to accomplish this task. Table 2.1 provides a summary of the PHENIX subsystems in relation to function and channel count [10].

Table 2.1. Summary of PHENIX Subsystems

PHENIX Subsystem	Channel Count	Function
Drift Chambers (DC)	10,200	Tracking, Pattern Recog., Momenta
Pad Chamber (PC)	48,000	Pattern Recognition, Tracking
TEC	29,000	Tracking, Electron Identification
EMCal	28,000	Electron and Photon Measurements
TOF	1,000	Hadron Identification
RICH	6,400	Electron Identification
Muon Tracker	20,000	Tracking, Momentum Measurement
Muon ID	4,600	Muon Identification
BB	130	Start Time, Fast Vertex
MVD	34,000	Event Multiplicity, Precise Vertex

2.3 MVD Subsystem Architecture

To perform the vertex positioning and multiplicity distribution measurements, the MVD is equipped with a highly integrated system of front-end electronics (FEE). The roughly 34,000 channels required for both silicon strip and silicon pad detectors coupled with the relatively small confined area of the barrel shown in Figure 2-4 offer many challenging design problems. High channel count, power consumption and area make traditional discrete electronics design utilizing crate type housings non-economical and impractical. The use of CMOS application specific integrated circuits (ASIC) provide an excellent low cost means of realizing the custom designed FEE of PHENIX. Radiation damage to FEE offer even greater challenges for the MVD. MVD is expected to receive a lifetime dose of roughly 60 krads. Specialized radiation hardened processes are commercially available through some silicon foundries at a much increased price over nonhardened processes. For this reason the FEE for the MVD will be implemented in a standard radiation soft CMOS process capable of withstanding the anticipated dose.

The FEE components for the 34,000 channel MVD include a charge sensitive preamplifier, an AMU with correlated sampler, a 10-bit Wilkinson type ADC, a overall system controller referred to as Heap Manager (HM) and a multiplicity discriminator [11]. Figure 2-5 is a functional diagram of the MVD FEE. Each component of the FEE is designed to operate at speeds necessary to achieve the maximum luminosity for the detector. The system beam clock for PHENIX operates on a 105 ns period, meaning every 105 ns particles are collided and a new event is

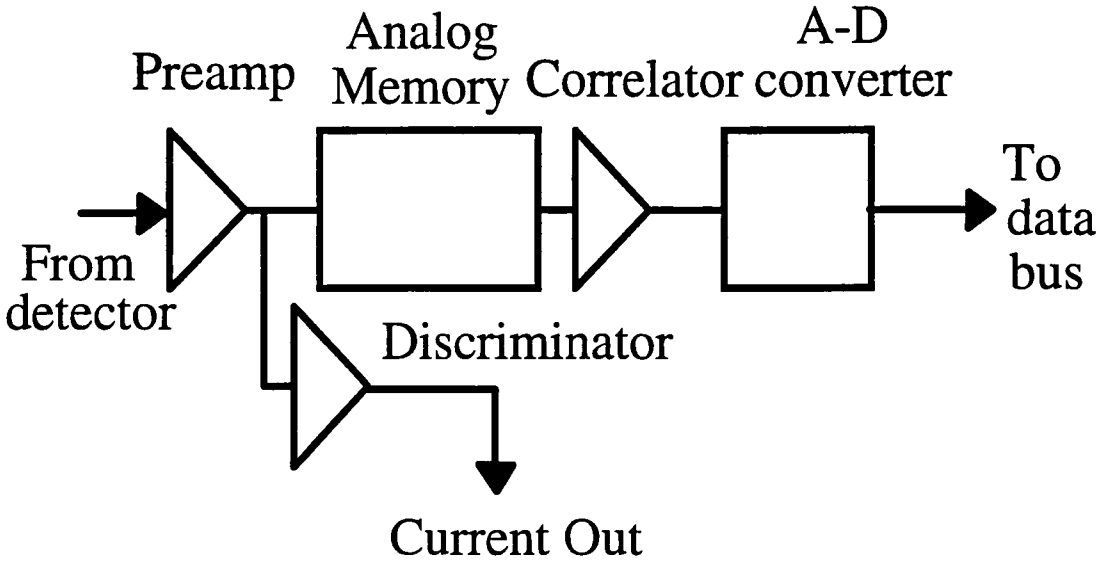


Figure 2-5. Block diagram of MVD FEE architecture.

generated. Thus individual FEE elements must function such that data is acquired at the highest possible rate of the detector. Due to the importance of the FEE to the function of the multiplicity discriminator, each element of the architecture shall be briefly described and discussed in relation to position, individual function and system performance.

2.3.1 Preamplifier

The silicon strip and silicon pad detectors to be used in the MVD have been optimized, as seen in Figure 2-6, for detection of particles equal to the Minimum Ionizing Particle (MIP). For these detectors one MIP is equal to 4 fC of charge. A minimum signal-to-noise ratio of 20:1 has been established for a single one MIP event (roughly 80 mV). This specification results in an rms noise of less than 2500 electrons. The need for such a low system noise places a special burden on the charge-sensitive preamplifier. Receiving input directly from the silicon strip detector, the preamplifier utilizes a PMOS cascode amplification stage to achieve low 1/f noise performance. Figure 2-7 is a simplified block diagram of the preamplifier. The preamplifier contains special calibration circuitry to allow controlled injection of charge in order to null unwanted offsets. As particles impact the detector, a resulting charge is placed on the amplifier's input. This input charge results in a positive ramping output having a risetime of approximately 60 ns. Charge continues to stack up with every new event (as evident by the ever ramping output) until a reset is given as shown in Figure 2-8. Resets occur to discharge the stored charge before the

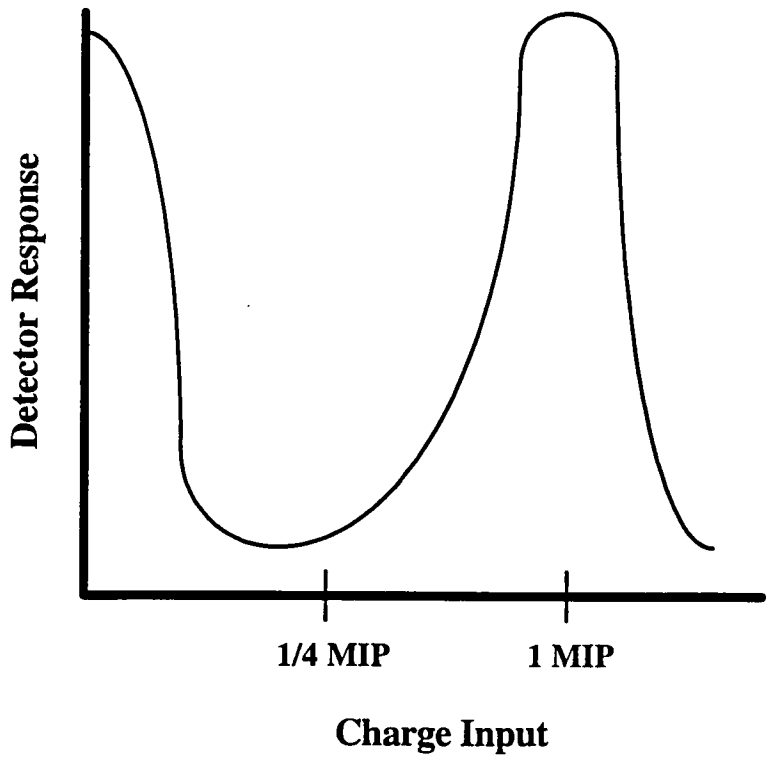


Figure 2-6. Graphical illustration of silicon strip detector response with optimal performance occurring for a 1 MIP input.

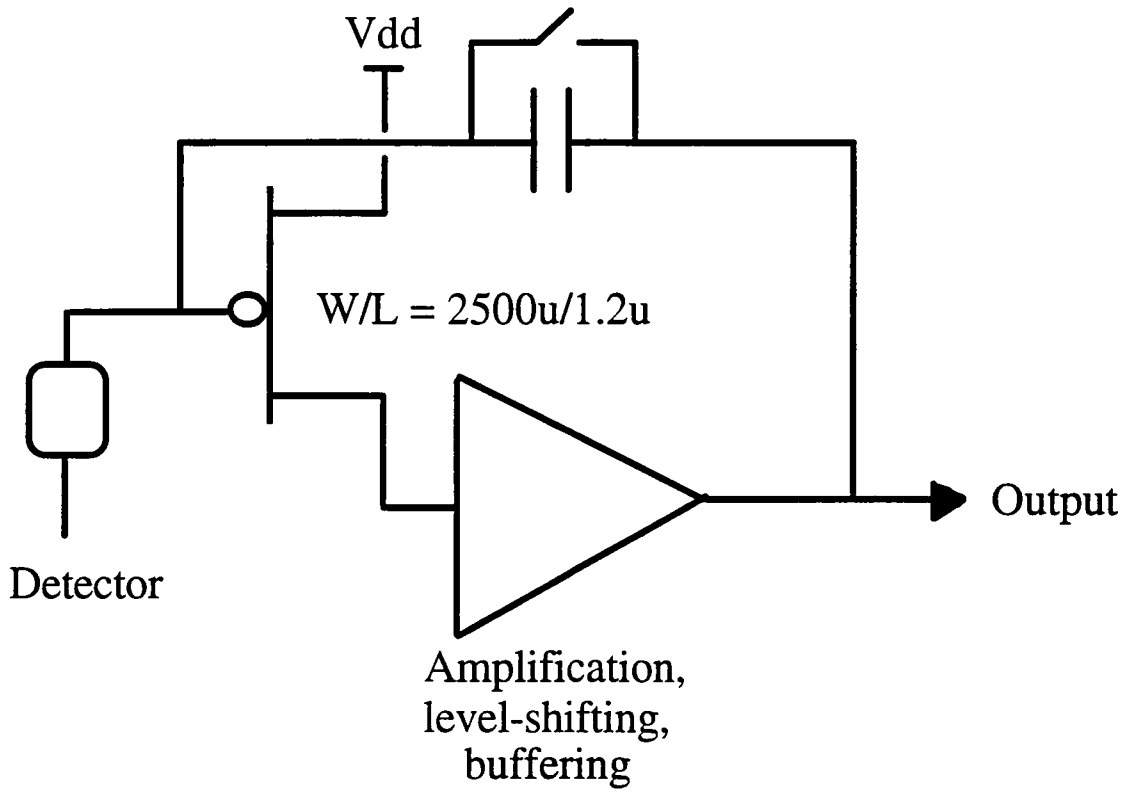


Figure 2-7. Simplified block diagram of charge-sensitive preamplifier.

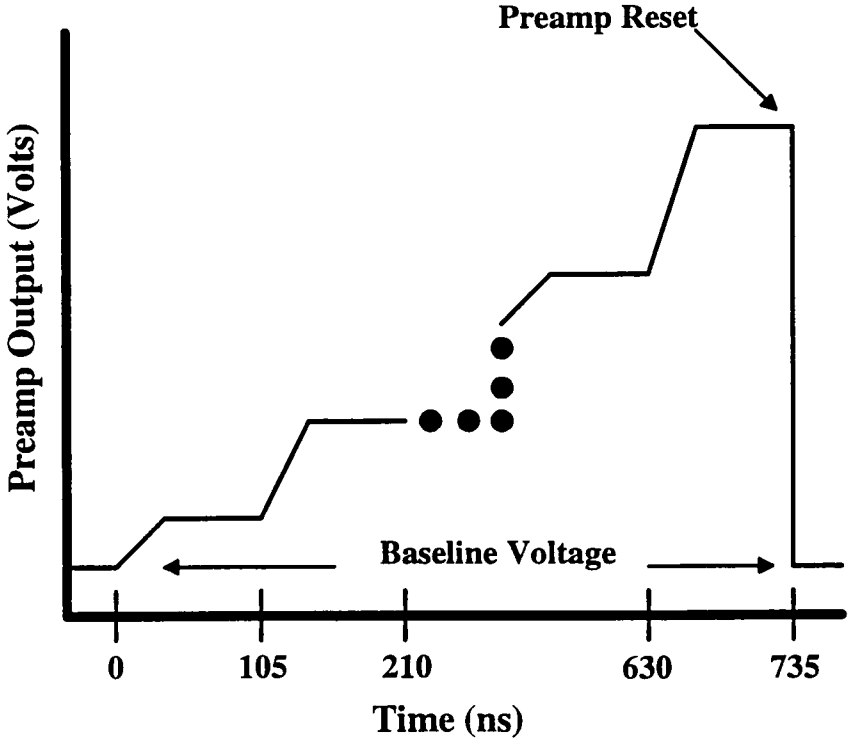


Figure 2-8. Charge-sensitive preamplifier output illustrating the accumulation of events every 105 ns until a reset occurs.

amplifier's dynamic range is exceeded. For a dynamic range of roughly 3 V, a maximum hit of 5 MIPs (400 mV) dictates a reset on the order of every 7 beam clocks or 735 ns. The use of input devices operating in weak inversion allow for a wideband preamplifier design with a measured power consumption of 1.2 mW. The preamplifier has also been measured to have a gain of 20 mV/fC, slope of 69 e/pF and 0 pF noise of 660 e. Additionally, the output stage is designed to drive capacitive loads of several picofarads.

2.3.2 Analog Memory Unit (AMU)

Connected to the output of the preamplifier is the AMU with correlated sampler. As illustrated is Figure 2-9, an AMU basically consists of an array of addressable capacitive cells which are read-out through a unity gain buffer amplifier. The AMU developed for the MVD FEE provides a deadtime-less, 64-cell deep, voltage-write-voltage-read topology. While functioning as a "dumb" memory, the AMU receives all read and write control from the system HM. The 64-cell deep memory provides pre and post event data storage necessary until a Level-1 trigger decision to accept the data is made. Latency for this decision can be several beam clocks. Immediately following the AMU output is a double-correlated sampler. Double correlated sampling enables the data rate to double by performing an internal subtraction of the pre and post values. A complete block diagram of the memory unit may be seen in Figure 2-10. Measured results for the AMU yield a power consumption of 1 mW/channel with a resolution of roughly 8 bits.

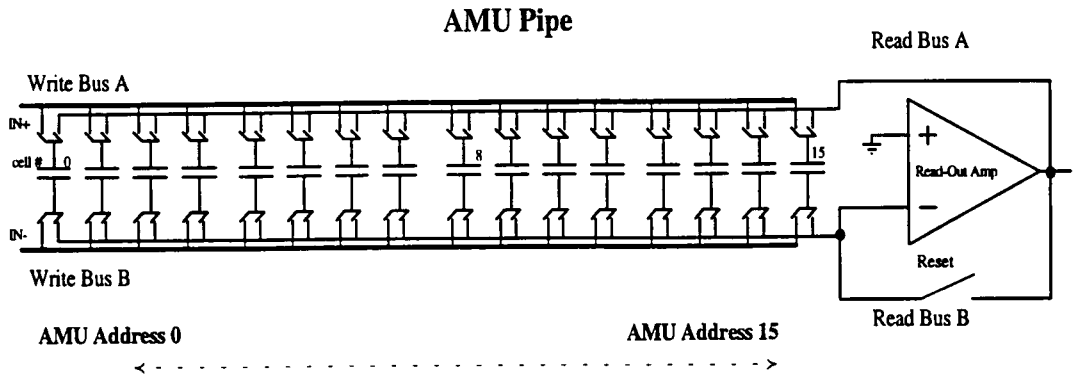


Figure 2-9. Functional diagram for the AMU implemented in the FEE of MVD.

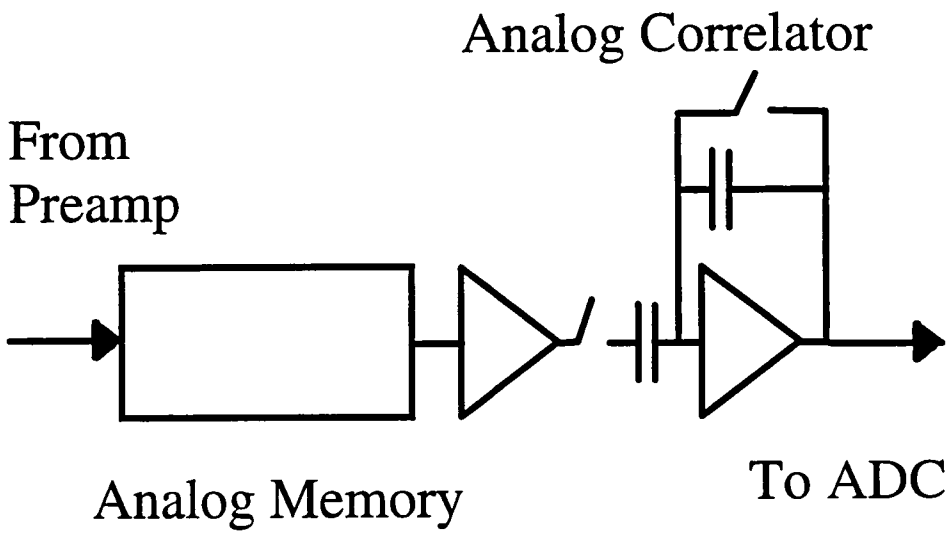


Figure 2-10. AMU / Correlator functional diagram.

2.3.3 Wilkinson ADC

If the Level-1 trigger accepts the data stored in the AMU, then the event has been determined to contain meaningful physics and is digitized by the ADC. The ADC is a switchable 10-, 11-, 12-bit Wilkinson type. For MVD the ADC operates at 10-bit resolution to achieve certain dynamic range requirements. Figure 2-11 is a functional diagram illustrating the fundamental components of the Wilkinson ADC. The ADC has been measured to provide 10-bit resolution in 5 μs with a dynamic range of 4.5 V. Power consumption for a 100 MHz clock rate was measured to be 600 μW/channel for the ADC [12].

2.3.4 Heap Manager Controller

To provide the control needed to carry out the data acquisition required by the MVD, a heap manager controller has been developed. Heap manager is responsible for all system control including preamplifier resets, AMU read and write addressing, correlator timing and ADC acquisition/conversion control. Additionally, the heap manger serves as the FEE link to the Level-1 trigger decision. Once a Level-1 decision has been made, the heap manager organizes the digitized data in a format required by the on-line processing elements of PHENIX. Commercially available Field Programmable Gate Arrays (FPGA) have been selected to implement these functions to allow in-circuit functional upgrades.

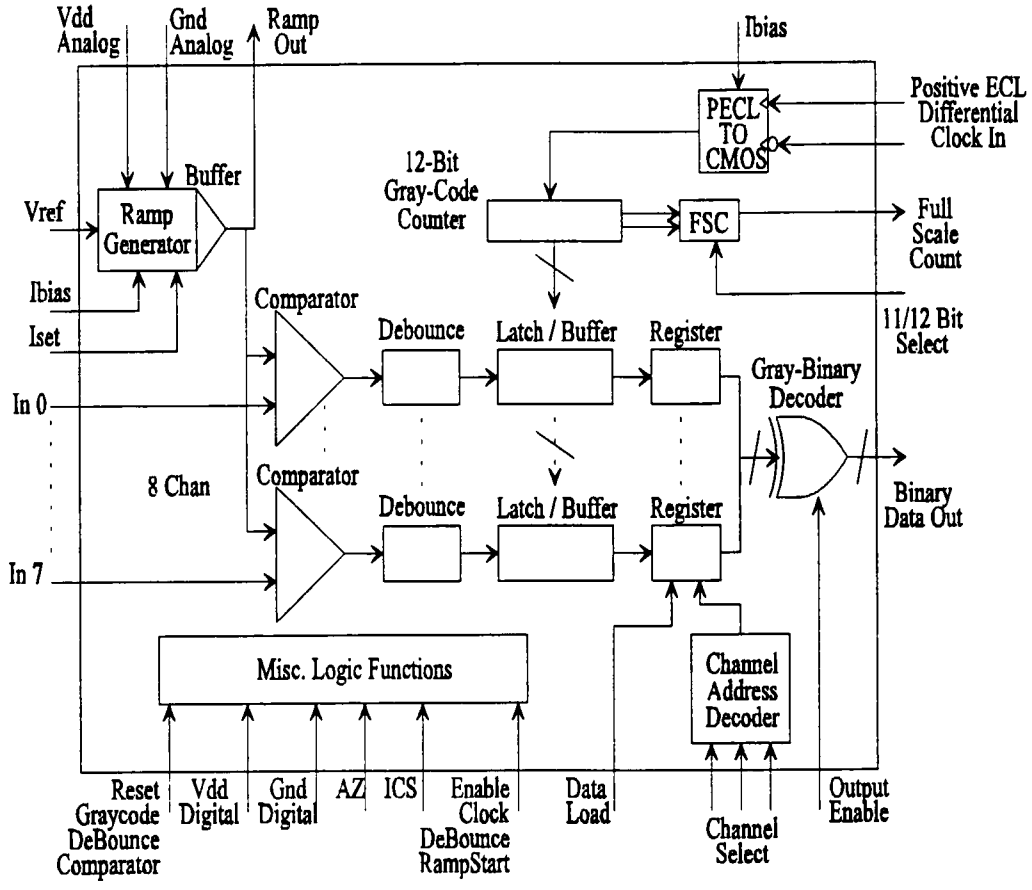


Figure 2-11. Functional diagram for the MVD FEE 10-bit Wilkinson ADC.

2.3.5 Multiplicity Discriminator

The final component of the MVD FEE is the multiplicity discriminator. While basically functioning as a comparator, the discriminator provides an discrete current output. When combined with other discriminator output currents, a total current sum proportional to the number of discriminators firing is generated. Figure 2-12 offers a high level depiction of the functionality for the multiplicity discriminator. The discriminator receives input directly from the output of the charge sensitive preamplifier. Once an input signal equal to the equivalent threshold setting of the discriminator is detected, a current source of fixed value is switched onto a summing node common to 256 discriminators. This current sum information is required by the Level-1 trigger to provided multiplicity distribution data necessary for making the trigger decision. To provide the current sum at rates needed for maximum RHIC luminosity requires a zero deadtime design. The multiplicity discriminator features a deadtime-less topology capable of firing on 0.25 MIP (20 mV) input signals while consuming only 500 μW/channel of power. A complete description of the multiplicity design and results will be presented in Chapters III and IV respectively. Table 2.2 provides a summary of MVD FEE components.

2.3.6 System Integration

System integration of the aforementioned MVD FEE will be carried out through the use of Multi-Chip Module (MCM) technology. The high packaging density obtainable by MCMs enables the 34,000 channels of MVD FEE to fit within

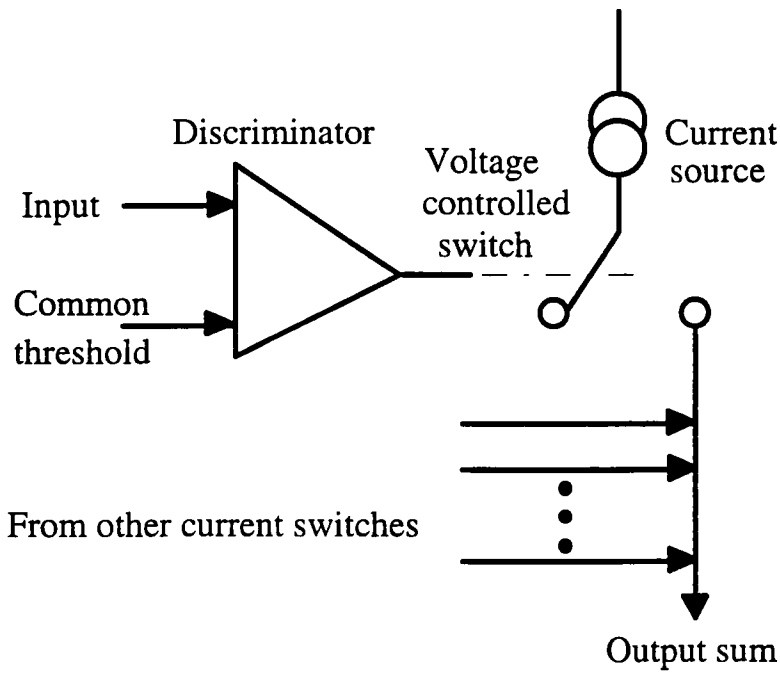


Figure 2-12. Functional diagram of multiplicity discriminator.

Table 2.2. Summary of MVD FEE Elements

MVD FEE Element	Specifications
Charge-Sensitive Preamplifier	Risetime = 60 ns, SNR = 20:1, Gain = 20 mV/fC, Dynamic Range = 3 V, Power = 1.2 mW/channel
AMU/Correlator	64-Cell Deep Memory, 8-Bit Resolution, Power = 1 mW/channel
Wilkinson ADC	10-Bit Resolution, Settling Time = 5 μs, Dynamic Range = 4.5 V, Power = 600 mW/channel
Heap Manager Controller	Two commercial FPGA's to provide complete system control
Multiplicity Discriminator	0.25 MIP Triggering, Power = 500 uW/channel

the barrel of Figure 2-4. For performance and economic reasons, the FEE have been combined into different chip sets. The first chip contains 32 channels of charge-sensitive preamplifier and multiplicity discriminator. The second chip contains 32 channels of AMU and ADC. Each MCM will contain 8 preamplifier/discriminator die and 8 AMU/ADC die for a total of 256 channels of FEE. Additionally, the MCM will also contain the heap manager FPGA die. Figure 2-13 illustrates the MCM realization of 256 channels of FEE.

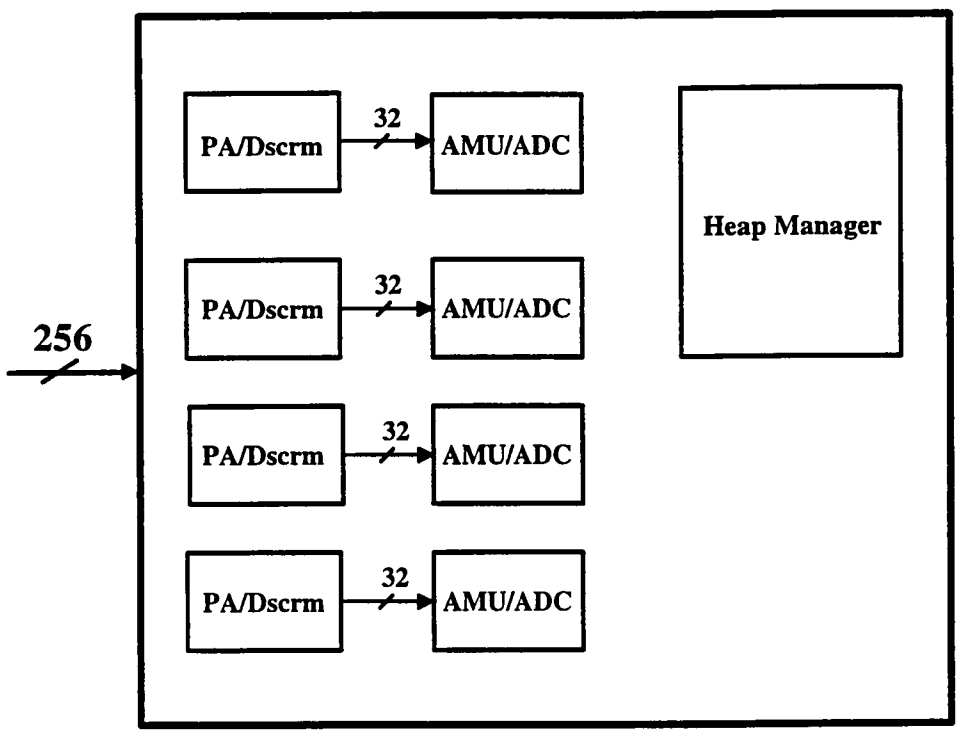


Figure 2-13. One MCM consisting of 256 channels of the MVD FEE.

Chapter 3

Multiplicity Discriminator Design

3.1 Discriminator Requirements

Implementing the function of multiplicity discrimination within the MVD FEE structure places many challenging and stringent requirements on the design. Issues such as power consumption, area, speed, adjustability and matching play a significant role in the development of an appropriate circuit topology. As illustrated in Table 2.2, power consumption requirements for the MVD FEE are very high compared to that obtainable with discrete designs. Excess power consumption within the MVD barrel produces levels of heating which can have detrimental effects on FEE. With approximately 34,000 channels of multiplicity discrimination, the need for a low power design is evident. A design goal of roughly 500 μW/channel was determined to be an acceptable limit. At this level, the multiplicity discrimination function alone requires 17 W for the entire MVD. Although the FEE will be maintained at a constant temperature, reduction in power consumption places less stringent requirements on the closed circuit cooling system. Since the FEE of MVD also consists of a charge sensitive preamplifier, AMU, ADC and heap manager within the confined area of the MVD barrel, the need for low power consumption is magnified.

There are numerous factors which contribute to the need for a design which requires minimal silicon area. The high channel count coupled with the limited physical area of the detector offer much motivation for a minimal area design. There are also several economic reasons such as prototyping costs and final IC yield which contribute to the need for a minimal area design. It has been shown that the less silicon area used, the higher the yield of the IC [25]. Since the multiplicity discriminator is only one part of the 32 channel combined preamplifier/discriminator chip, any reduction in area directly corresponds to decreased die size and increased yield. For these reasons the discriminator layout was determined to be arrayable on an 85 μ pitch (to match the pitch of all MVD FEE) with a length of less than 600 μ.

Perhaps the most challenging aspect of the multiplicity discriminator is the need to be active for every beam crossing (105 ns) with no deadtime. Since the discriminator receives input directly from the charge sensitive preamplifier with a ramping output having a risetime of roughly 60 ns, there is only 45 ns for the discriminator to fire, return to baseline and await the next crossing. This aspect of the design is complicated by the requirement that the discriminator trigger on inputs ranging from 0.25 MIP (20 mV) to 5 MIP (400 mV). From this range, worst case conditions occur when the maximum input of 5 MIP is followed by the minimal input of 0.25 MIP on the subsequent beam crossing. The desired signal differentiation response for this case in depicted in Figure 3-1.

In order to achieve a robust system, a design featuring as few external adjustments as possible is highly desirable. As with most forms of comparators there

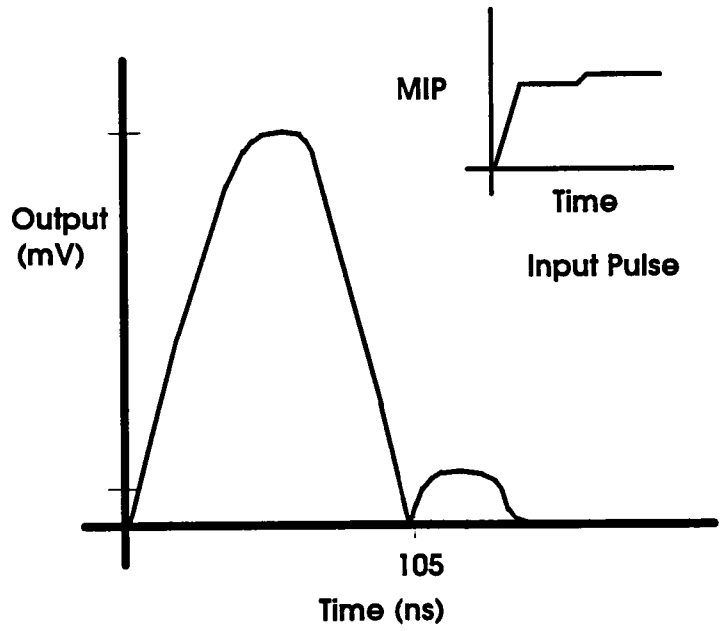


Figure 3-1. Desired differentiation response under worst case conditions.

exists the need for a threshold adjustment which for this application must be common to 32 channels of discriminator. To provide precise event multiplicity data, threshold matching must be within ± 5 mV across the die. Commercially available integrated circuits often require factory trimming where high levels of matching are desired. Often additional devices are added to a design for the sole purpose of trimming. Many times these devices may occupy a substantial amount of the chip area. Due to the desire to keep the silicon area to a minimal, the most compact topology that allows for adequate matching should be explored. Although the heap manager offers the ability to provide programming through a serial interface, a design which utilizes the minimal amount of external adjustments is highly desirable. Table 3.1 provides a summary of the established design goals for the multiplicity discriminator.

Table 3.1. Summary of Multiplicity Discriminator Design Goals

Element	Specification
Power	Maximum power must be less than 500 μW/channel
Silicon Area	Layout must be on 85 μ pitch with a length less than 600 μ
Speed	Discriminator must fire and return to baseline in ≈ 45 ns
V_T Matching	Threshold matching must be within 10 mV from channel-to-channel
Firing Range	Discriminator must fire on input signals ranging from 0.25 to 5 MIP
Adjustability	As few adjustments needed to accomplish task

3.2 Comparators

On the most basic level, the multiplicity discriminator performs the function similar to that of a comparator. Comparators are devices which allow an output state

change based on the input voltage relative to an established trip point or threshold. The simple inverter of Figure 3-2 provides an example of a type of comparator. With Vn held constant such that M1 is conducting and Vbias such that M2 is off, output of the circuit moves toward Vdd. As Vbias is increased until the point M1 begins to conduct, the output is pulled low. Depending on which device, M1 or M2, is conducting the most current the output is either high or low. If M1 conducts the most Vout is low. On the other hand, as the conduction of M2 equals the current of M1, the transition from low to high begins. Thus there exists a certain bias voltage such that this transition occurs. However, due to the finite gain of the amplifier given by

$$A_V = \frac{-gm1}{gds1 + gds2} = \frac{-(gm1)(rds1)(rds2)}{rds1 + rds2} \qquad \textbf{(3.1)}$$

this transition does not occur instantaneously once the trip voltage is reached, but more gradually over a span of several millivolts. The trip voltage may be calculated by [26]

$$V_{trip} = Vdd - \left[\frac{2I_B}{\mu C_{OX}(W/L)_2 \left[1 + \lambda(\frac{Vdd - Vss}{2}) \right]} \right]^{1/2} - |V_{T2}| \qquad \textbf{(3.2)}$$

where I_B is

$$I_B \approx (\mu C_{OX}(W/2L))_1 (V_{BIAS} - Vss - V_{T1})^2 \left[1 + \lambda(\frac{Vdd - Vss}{2}) \right] \qquad \textbf{(3.3)}$$

From this equation it can be seen that trip voltage has heavy dependence on the power supply. Designs with low power supply rejection in which slight changes in power

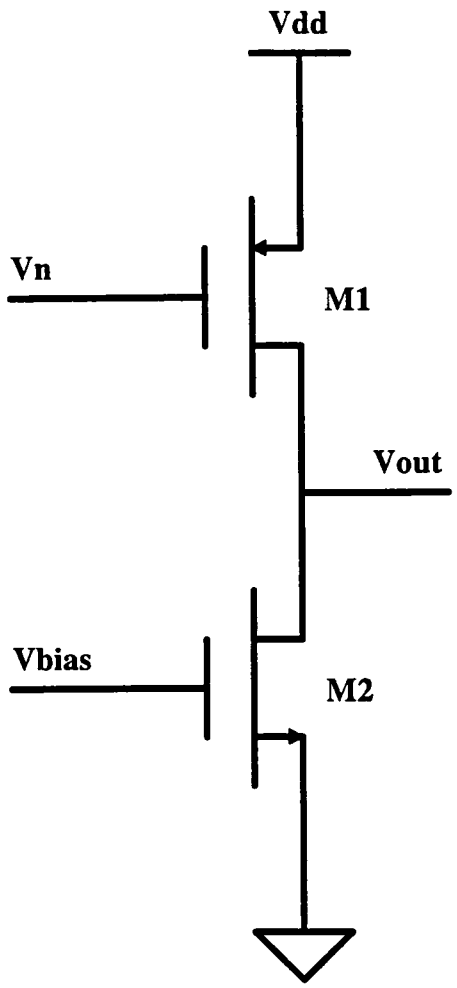


Figure 3-2. Simple inverter which can serve the function of a comparator.

serious drawbacks to implementing a high precision circuit. Although the trip voltage can be adjusted, the range of adjustment to ensure proper performance is rather small. Such sensitive designs exhibit considerable variation over unavoidable process gradients.

Many of the problems associated with the simple inverter can be eliminated through the use of the differential amplifier topology as seen in Figure 3-3 [26]. Fundamentally, the differential pair performs an amplification of the difference signal between the inverting (Vn) and noninverting (Vp) inputs while providing a gain given by [15]

$$A_V = \frac{gm2}{gds2 + gds4} \tag{3.4}$$

When the voltage applied to Vp is greater than that applied to Vn, M1 receives more current and the drain of M4 is pulled high. If on the other hand Vn is greater than Vp, more tail current from M5 is steered through M2 than M1 and the output is pulled low. The use of the differential pair amplifier eliminates the comparators dependence on power supply fluctuations at the cost of reduced output dynamic range given by

$$V_{OH} = Vdd - V_{DSAT4} \tag{3.5}$$

and

$$V_{OL} = V_P - V_{T1} - \left[\frac{I_{TAIL}}{\mu C_{OX}(W/L)_1}\right]^{1/2} \tag{3.6}$$

By removing the comparators dependence on power supply changes, the threshold voltage could theoretically be controlled perfectly. However, any process variations

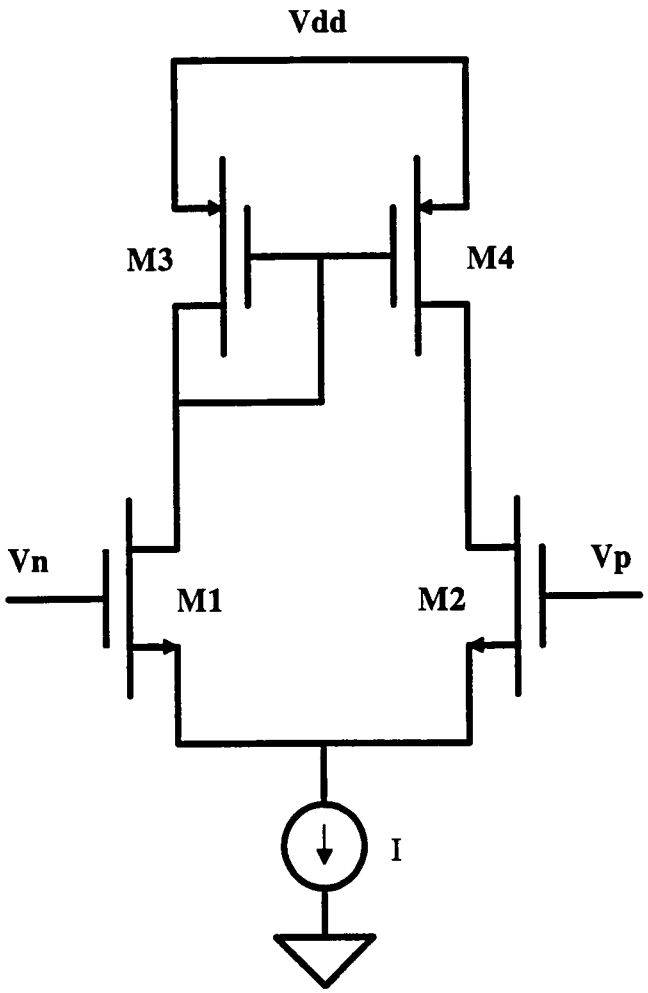


Figure 3-3. Differential amplifier topology.

causing mismatch in threshold voltages for the M1 and M2 devices produce an undesirable offset voltage. This offset voltage may be in the tens of millivolts and once again place a limit on the achievable threshold voltage control. Additionally, drain voltage mismatch between M1 and M2 produce further nonideal effects due to channel-length modulation.

A combination of the circuits illustrated in Figures 3-2 and 3-3 may be seen in Figure 3-4. The circuit of Figure 3-4 overcomes the drawbacks of each circuit individually while capitalizing on the advantages of both. While the differential amplifier offered limited output dynamic range capabilities, the addition of the inverter enables rail-to-rail operation. The gain of this configuration is given by the product Eqs. (3.2) and (3.4) or simply

$$A_V = \left(\frac{gm1}{gds2 + gds4}\right)\left(\frac{gm6}{gds6 + gds7}\right) \tag{3.7}$$

Frequency response for the circuit is limited by the amount of current available to charge parasitic capacitances. These capacitances include the depletion capacitance of M2 and M4, the gate-to-source capacitance of M6 in addition to any load capacitance associated with the output node. The more precise control of the comparator threshold voltage provided by the differential pair when coupled with the increased gain of the inverting stage, provide a relatively high performance comparator.

A prototype 8 channel version of a topology similar to the circuit described in Figure 3-4 was implemented in a 1.2 μ CMOS process. Total silicon area required for one channel of discriminator was measured to be 85 μ x 240 μ. Power consumption

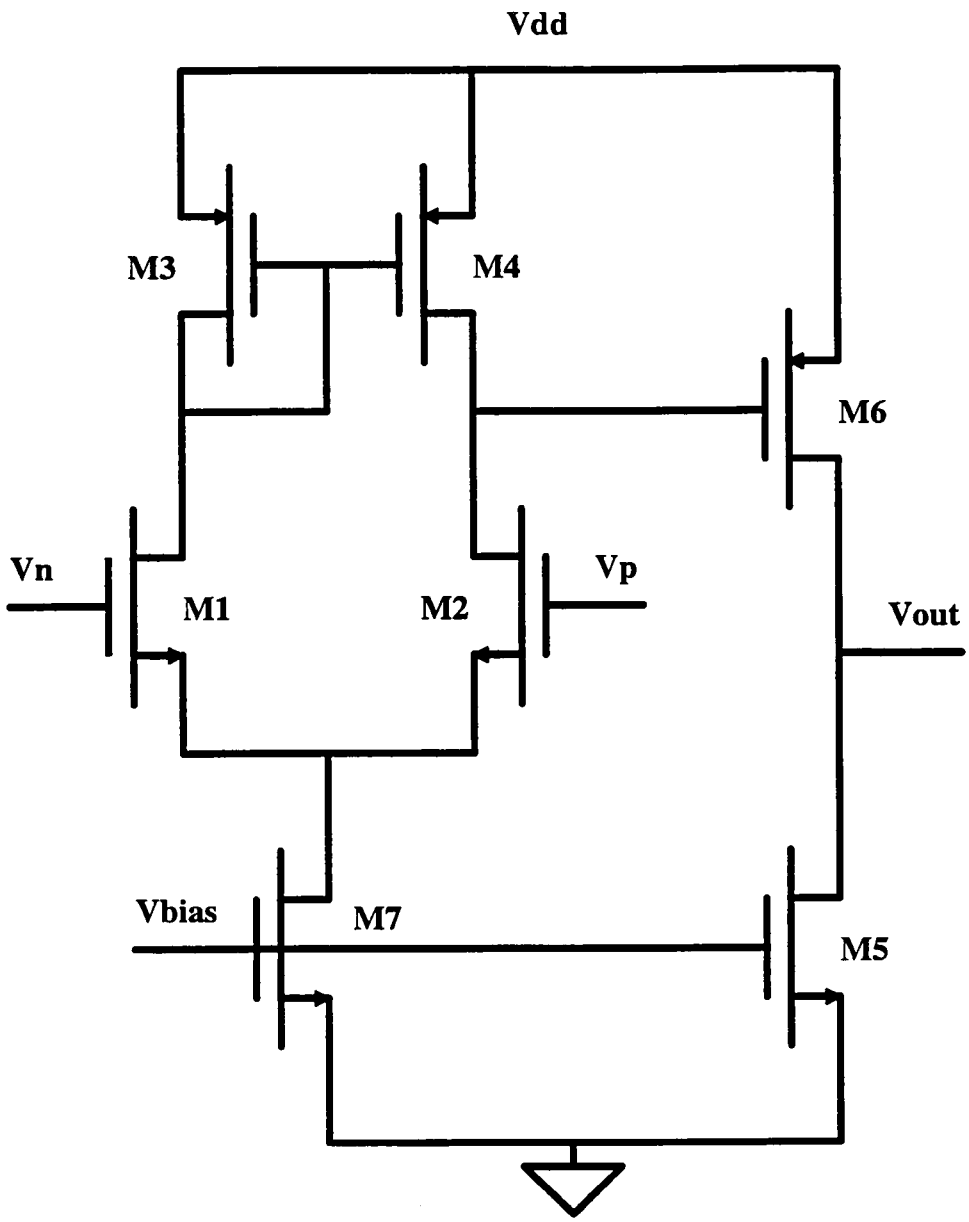


Figure 3-4. Comparator combining the advantages of the differential amplifier and the inverter.

for the discriminator was measured to be less than 1 mW per channel. Clearly from these specifications the topology appears to be adequate based on the design goals previously established. However, this design exhibits one problem which renders it unacceptable for use in the FEE of MVD. One of the main design objectives was to achieve a topology that provided common threshold matching of less than 10 mV. This is extremely important since one threshold bias voltage will be common to 32 channels of discriminator in the final MVD FEE. To set the threshold voltage for multi-channel use, the voltage is adjusted such that, for a given input signal, the most sensitive channel is on the verge of firing. A measure of the channel-to-channel matching may then be determined by increasing the input signal until all channels fire. The circuit was found to have a threshold mismatch in excess of $\pm$ 30 mV. From these results it was obvious that common threshold matching from channel-to-channel was not adequate to fulfill the needs of the MVD.

3.3 Discriminator Design

The inability to fabricate a design utilizing the previously discussed topologies such that a common threshold could be accurately matched over multiple channels required the implementation of a new topology. Any new design must incorporate a comparator stage which is insensitive to power supply fluctuations, efficient with respect to size and power, and allows precision threshold matching from channel-to-channel. The designed circuit consists of several stages including an input differentiator stage, gain stage, threshold adjustment and output current switch. Each

of these stages will now be discussed. Figure 3-5 is a block diagram illustrating the signal flow for an applied input.

3.3.1 Input Differentiator

The design and implementation of the input differentiator is of utmost importance to the acceptability of the multiplicity discriminator for use in MVD FEE. As previously discussed, the need for a differentiating input is brought about by the 60 ns risetime ramping output signal of the charge sensitive preamplifier. With a preamplifier reset occurring approximately every 7 beam crossings, the need exists to differentiate between each new event. There are several factors which must be considered when designing an appropriate differentiator circuit for use as an input for the discriminator. In keeping with the established design goals for the multiplicity discriminator, the input differentiator must be optimized for speed, area and power consumption. Another dimension to the design which is unique to the input differentiator is the attenuation/gain factor. An input differentiator which is optimized for speed, area and power may not be the most optimal design when considering the entire discriminator. Such a design would most likely attenuate the input signal drastically and require more gain stages within the remaining design. Thus by making the differentiator optimal with respect to area and power, the area and power requirements for the entire discriminator might actually increase.

The most basic implementation of a differentiator is that consisting of a passive C-R network. As illustrated by Figure 3-6, the C-R network provides a differentiation

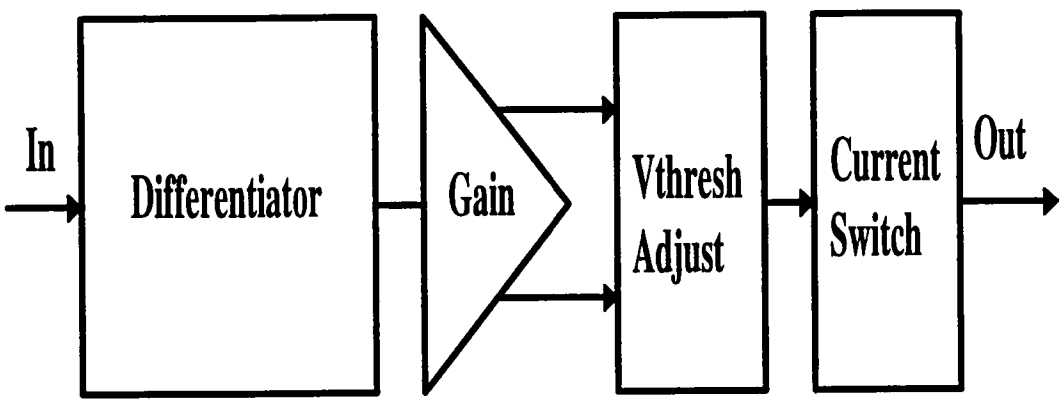


Figure 3-5. Signal flow diagram for the multiplicity discriminator.

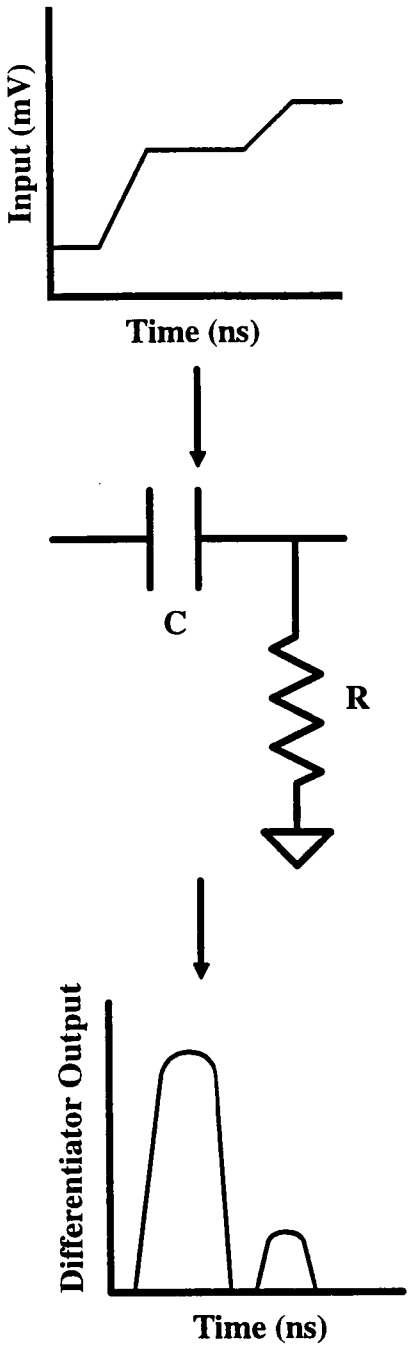


Figure 3-6. Diffferentiation of ramping input signal by a passive C-R network.

of the ramping input pulse. Once the preamplifier begins ramping upward, current begins to flow through the capacitor with a relationship given by

$$i = C\frac{dV}{dt} \tag{3.8}$$

This current can then flow through the resistor and produce the corresponding output voltage given by

$$Vout = RC\frac{dV}{dt} \tag{3.9}$$

When the preamplifier stops ramping and remains at a constant dc level, the differentiator output goes to zero. This action is fundamental to the nature of a capacitor since no current can flow through a capacitor which does not have a changing voltage across it.

From Eq. (3.9) it is evident that the differentiator output voltage is directly proportional to the rate of change of the input signal and the values of R and C. For a fixed risetime (60 ns), the rate of change (dv/dt) of the input signal varies, under worst case conditions, from 6.67 μV/sec for a 5 MIP (400 mV) event to 0.333 μV/sec for a 0.25 MIP (20 mV) event. Knowing this range of operation allows values of R and C to be selected to achieve a desired response. Due to the difficulty in achieving small, stable, high valued capacitors within monolithic processes, the value of C must be chosen to be fairly small. Conversely, relatively high valued resistors can be achieved within small areas. For example, a 5 pF poly-poly capacitor in the Orbit 1.2 μ process having a density of 0.5 fF/μ^2 would require an area of 10,000 μ^2. Placing this within the 85 μ pitch of the discriminator and allowing a modest 20 μ for routing and power

supply busses would require a capacitor having dimensions of 65 μ x 154 μ which is over a third of the desired length for the discriminator. Reducing the capacitor value an order of magnitude to 0.5 pF would require only 1,000 μ^2 and could be implemented in a 65 μ x 15 μ area. Based on these results a 0.5 pF capacitor shall be used in all future calculations.

Selection of an appropriate R for the circuit of Figure 3-6 is dominated by two contrasting effects. For speed considerations the RC time constant associated with the C-R differentiator must be as small as possible. In order for no beam crossings to be missed, the differentiator must be fast enough to satisfy the worst case conditions of a maximum event followed by a minimal event on the very next crossing. It should be noted that additional delays will be introduced into the response by the remaining discriminator circuitry. For this reason a maximum delay for the differentiator must be specified. Assuming the remaining circuitry can perform the required functions in 15 ns to 20 ns, an upper limit of roughly 90 ns can be established for a 5 MIP (400 mV) input as illustrated by Figure 3-7. By choosing a minimal value of R, the time constant is minimized for a fixed value of C. Such a response may be seen from the HSPICE simulation of Figure 3-8 for an R=1 Ω and C=0.5 pF under worst case conditions. An input differentiator response of roughly 60 ns for a 400 mV input is achieved at the cost of attenuating the signal amplitude. Attenuation of the input signal to the levels shown in Figure 3-8 places the differentiator output signal in the noise floor for the system. As the value of R is increased, the attenuation as well as the circuit speed decreases. The HSPICE plot of Figure 3-9 illustrates this point for values of R=1 KΩ,

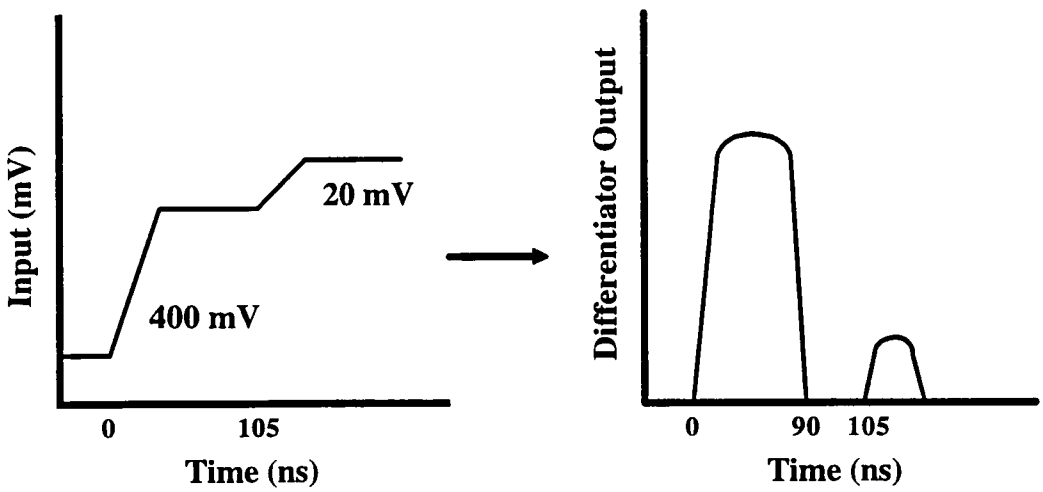


Figure 3-7. Desired response of passive differentiator.

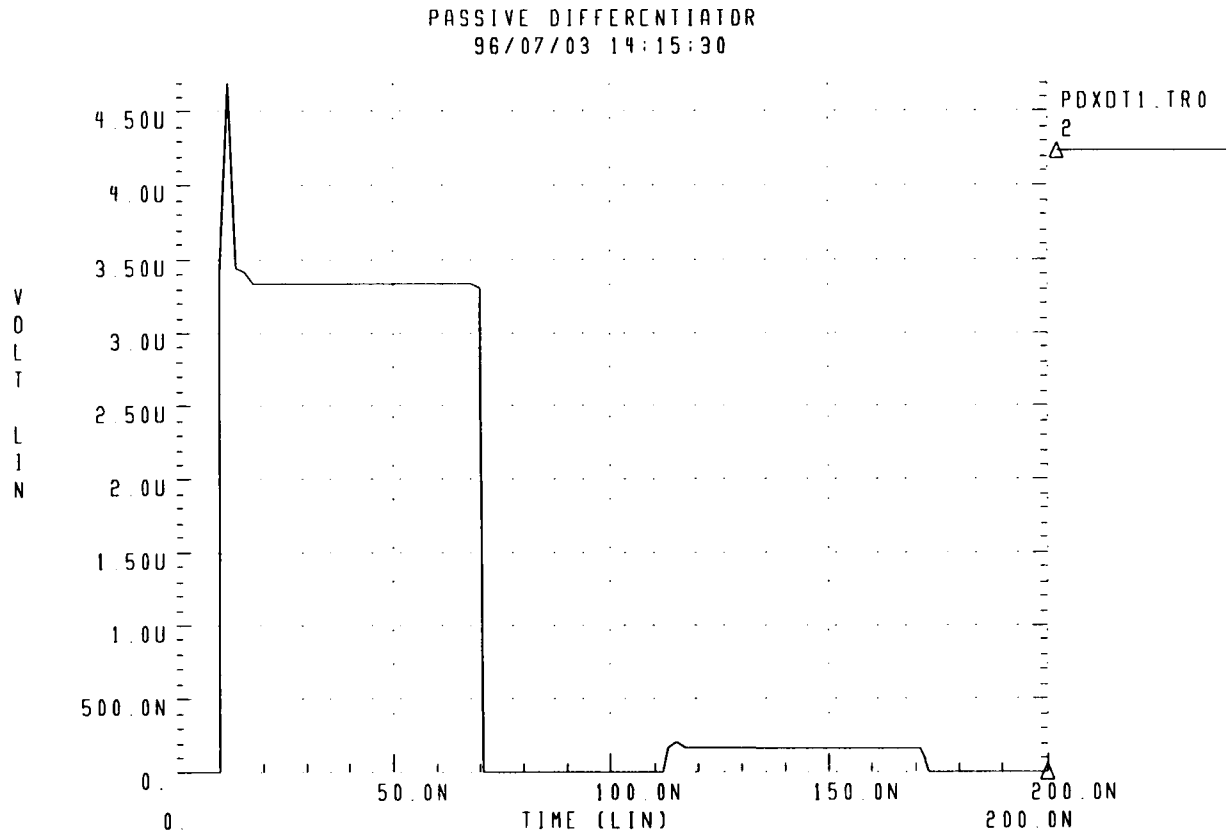


Figure 3-8. Passive differentiator response for C = 0.50 pF and R = 1 Ω.

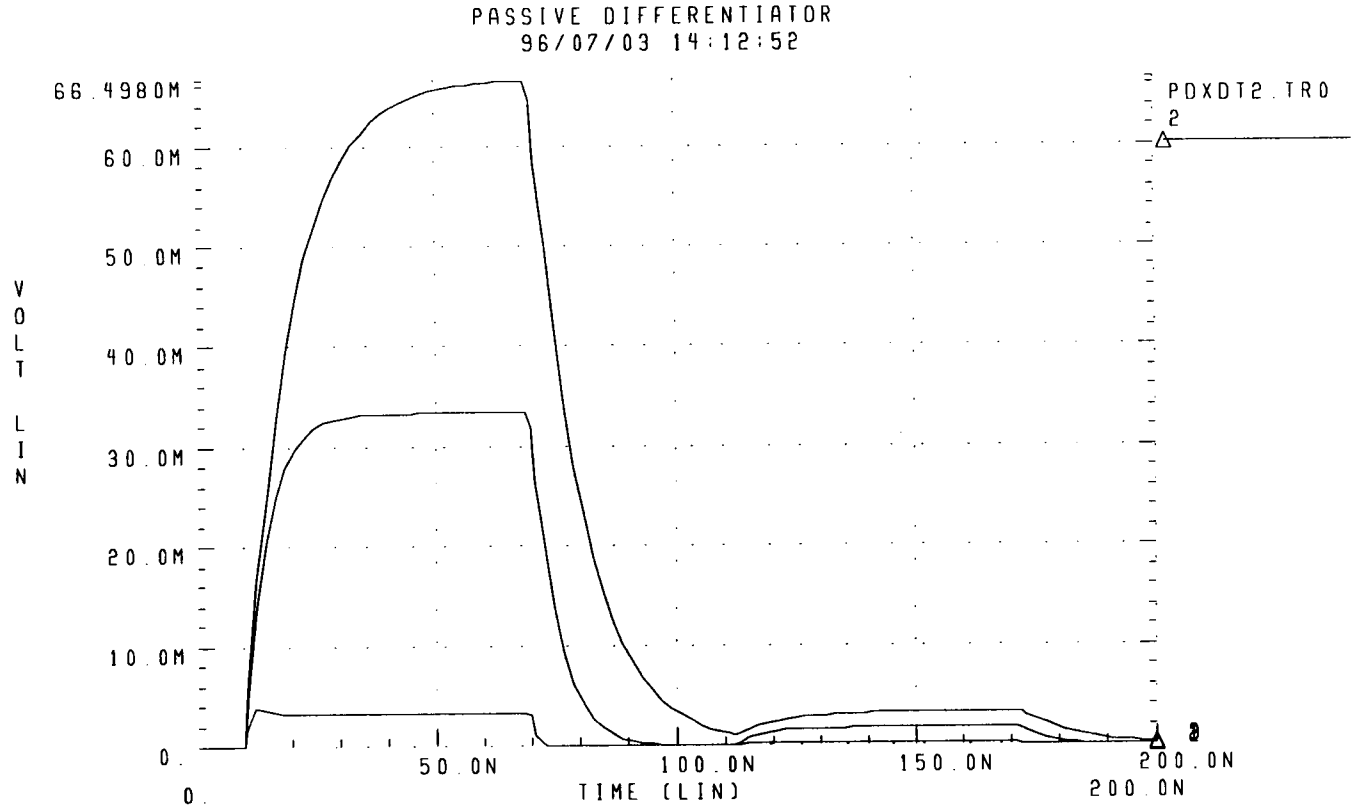


Figure 3-9. Passive differentiator response for C = 0.50 pF and R = 1 KΩ, 10 KΩ and 20 KΩ.

10 KΩ and 20 KΩ. From the plot it is evident that a resistance of 20 KΩ requires more than the acceptable 90 ns and actually never returns to baseline before the next event occurs. Somewhere in the vicinity of 10 KΩ seems to be optimal in that an 80 ns response is achieved at the cost of only a factor of 10 attenuation. Closer analysis reveals a value for R of 12 KΩ provides the desired response with an attenuation factor of exactly 10. A resistor of this value could be constructed in a monolithic process utilizing one of several structures such as a poly resistor or a diffusion resistor. For example, a 12 KΩ poly resistor having a density of roughly 50 ohms per square would require an area of 65 μ x 4 μ.

Although implementation of the simple C-R network of Figure 3-6 provides an acceptable means of performing the differentiation function, the loss of gain due to the passive nature of the topology places increasing demands on the remainder of the discriminator circuit. The need for additional gain results in a larger gain stage requiring more quiescent current. One solution to the issue of signal attenuation is the use of an active input differentiator stage which allows for an acceptable frequency response plus a gain amplification. Figure 3-10 provides the topology of one such active differentiator. As illustrated by the small-signal equivalent circuit shown in Figure 3-11, the resistance seen looking into the source of the simple common-gate stage replaces the R of Figure 3-6 and is given approximately by

$$Rin = \frac{1}{gm + gm_{body}} \qquad \textbf{(3.10)}$$

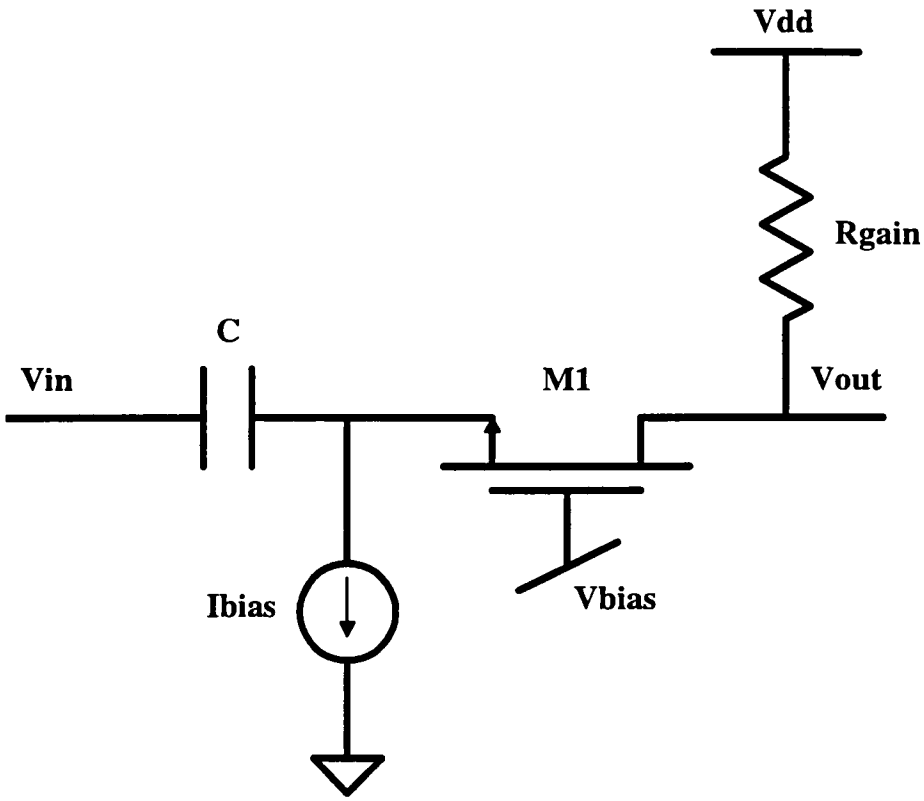


Figure 3-10. Active differentiator topology.

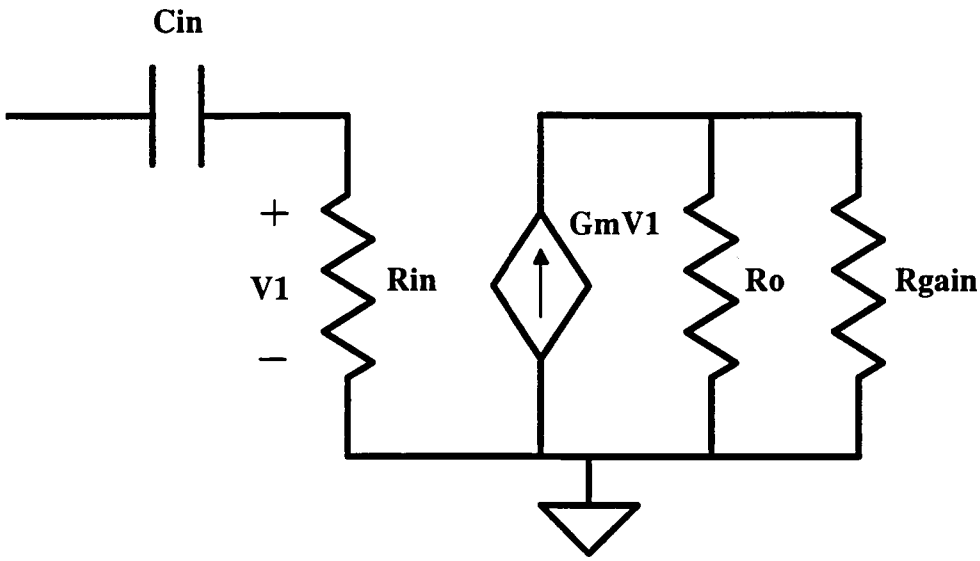


Figure 3-11. Input differentiator small-signal equivalent circuit.

From this equation it can be calculated that M1 requires a transconductance (gm) of roughly 83 μA/V to achieve the equivalent of the 12 KΩ resistor. Additionally, the amplifier may be shown to have a gain of

$$A_V = gm(R_{Gain}) \tag{3.11}$$

Differentiating the square law relationship given by

$$I_D \approx \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)(Vgs - Vt)^2 \tag{3.12}$$

with respect to Vgs provides the transconductance in the form

$$gm = \left[2 I_D \mu C_{OX} (W / L)\right]^{1/2} \tag{3.13}$$

From this equation for a fixed drain current Id, the W/L ratio needed to generate the desired Rin may be calculated. Selection of a bias current is extremely important for the input differentiator since in addition to determining the characteristics of M1 it will also set the dc output voltage by the voltage drop across the gain resistor. For power consumption concerns a bias of less than 20 μA is desired. To establish a dc output voltage between 3 V to 4 V for the needed gain and Rin, a current in the 10 μA to 20 μA is required. Using the minimum value of KP/2 = 30 $\mu A/V^2$ provided in the process parameters for the Orbit 1.2 μ process with Id = 15 μA and gm = 100 μA/V, the calculated W/L required to provide an Rin of greater than 10K is roughly 6. It can be shown by

$$f_T = 1.5\frac{\mu}{2\pi L^2}(Vgs - Vt)^2 \tag{3.14}$$

that for a MOS device frequency response is inversely proportional to the square of the length L [16]. Thus for optimal frequency performance a minimal geometry L should be selected. Utilizing a minimal length of L = 1.2 μ, the minimal width is calculated to be W = 7.2 μ.

In order to place M1 in strong inversion, a value for Vbias must be selected such that M1 has a Vgs greater than the threshold voltage of the device. Also from Eq. (3.14) the use of a larger Vbias will enhance the frequency performance of the circuit. For the Orbit 1.2 μ process, n-channel devices have a nominal threshold voltage of roughly 1 V. Thus placing Vbias at a voltage of 2.5 V fulfills the requirement while offering a relatively easily obtainable voltage. Simulating the circuit of Figure 3-10 utilizing BSIM models with $(W/L)_{M1}$ = 7.2 μ/1.2 μ, Rgain = 100 KΩ, Vbias = 2.5 V and an ideal current source of 15 μA produces a response which is slightly slower than that desired. Fundamentally, the unity gain frequency of a MOS transistor is given by the relation

$$f_T = \frac{gm}{2\pi(Cgs + Cgd + Cgb)} \tag{3.15}$$

where for small devices Cgd and Cgb are negligible. Neglecting Cgd and Cgb reduce Eq. (3.15) to the approximate result of

$$f_T \approx \frac{gm}{2\pi Cgs} \tag{3.16}$$

where Cgs is a capacitance which is intrinsic to the device and may be approximated to a first order by [25]

$$Cgs = \frac{2}{3} WLC_{ox} \tag{3.17}$$

From Eq. (3.16) it is obvious that to increase the frequency performance of the device the gm must be increased at the cost of lowering the equivalent R for the differentiator. As evident by Eq. (3.13) the gm may be increased by either increasing the W/L ratio or the drain current of M1. Since a current of roughly 20 μA has been established as the maximum bias for the input differentiator, manipulation of the W/L ratio for M1 remains the only means by which the frequency response can be adjusted. However, by Eq. (3.17) parasitic capacitance Cgs is directly proportional to the area established by the product of W and L. There exists an optimal W/L ratio such that the gm of M1 can be maximized while keeping the parasitic Cgs small enough to allow the circuit to provide adequate frequency response. For a fixed gain of 10 and fixed current of 18 μA implemented by an ideal current source, BSIM models predict an optimal W/L ratio to be roughly (12 μ/1.2 μ). It should be noted that although this provides an approximate value for the sizes of W and L, other nonideal effects dictate slight changes in this ratio. Since the current source for the circuit is not ideal and must be implemented with MOS transistors, there exists additional nonideal parasitic capacitances as illustrated by Figure 3-12 which further add to the total capacitance associated with the critical node and slow the circuit response.

Establishment of an adequate current source is crucial to the performance of the input differentiator. Nonideal effects such as a non-infinite rds and intrinsic parasitic capacitances place further constraints on the sizing of the transistors used to

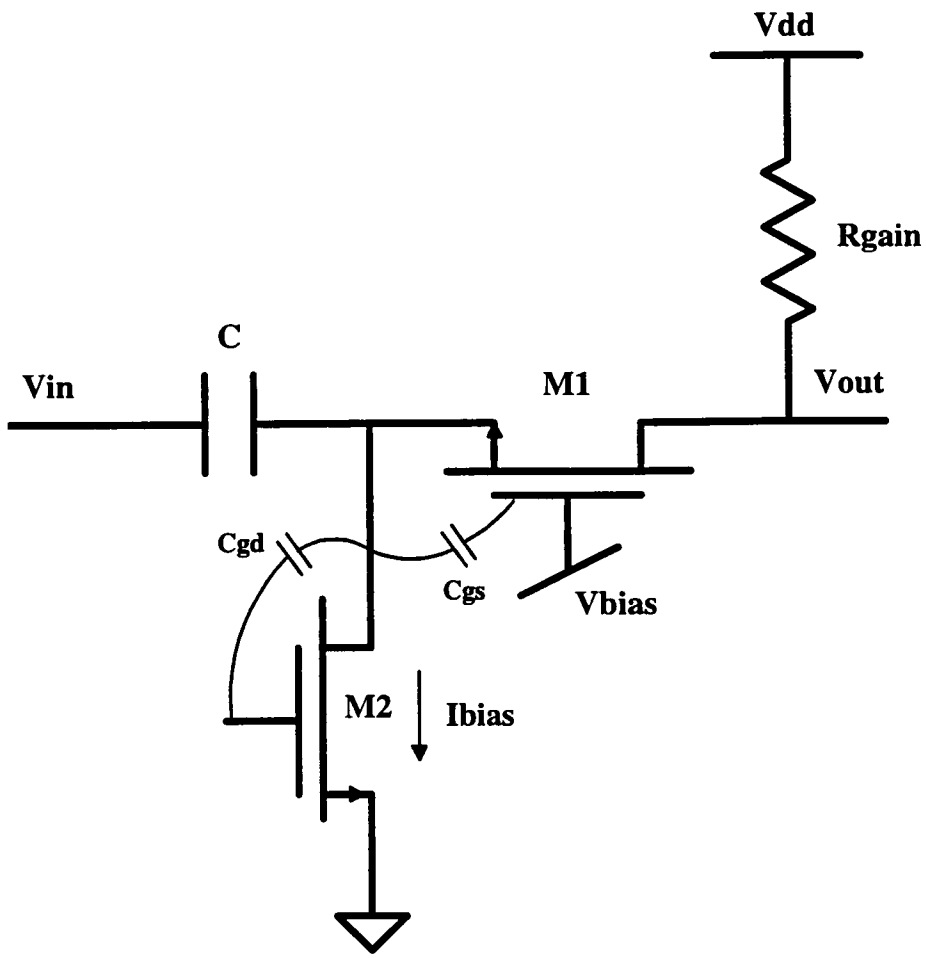


Figure 3-12. Nonideal parasitic capacitance associated with differentiator input.

make up the current source. The value of rds for the basic current mirror of Figure 3-12 is given by

$$r_{ds} = \frac{(V_A + V_{DS})}{I_D} \tag{3.18}$$

where the term

$$V_A = \frac{L_{eff}}{I_D}\left(\frac{dX_d}{dV_{DS}}\right)^{-1} \tag{3.19}$$

is often referred to as $1/\lambda$ [25]. Clearly the value for rds is inversely proportional to Id and directly proportional to the effective length, L_{eff}, of the channel. Thus by making Id small and L_{eff} large, a maximum rds can be achieved for this topology. Since matching among current mirrors is determined by rds, it is imperative that the value of L not be of minimal geometry due to the fact that minimal geometry devices are much more susceptible to process variations [17]. Other topologies such as the cascode current mirror of Figure 3-13 offer an increased rds given by

$$R_O = r_{o2}\left[1 + (gm_2 + gmb_2)r_{o1}\right] + r_{o1} \tag{3.20}$$

at the cost of a higher drop out voltage. A configuration such as this would require not only twice the area, but would also result in the need for a higher bias voltage at the source of M1. Due to the low bias current being utilized by the differentiator, achieving an acceptable value of rds should be possible with the basic current mirror connection. As a compromise between area, matching and parasitic capacitance a current mirror sizing of W = 12 μ with L = 2.4 μ was selected. Using this current mirror with a nominal bias current of 18 μA for a fixed gain of 10, the W/L ratio of

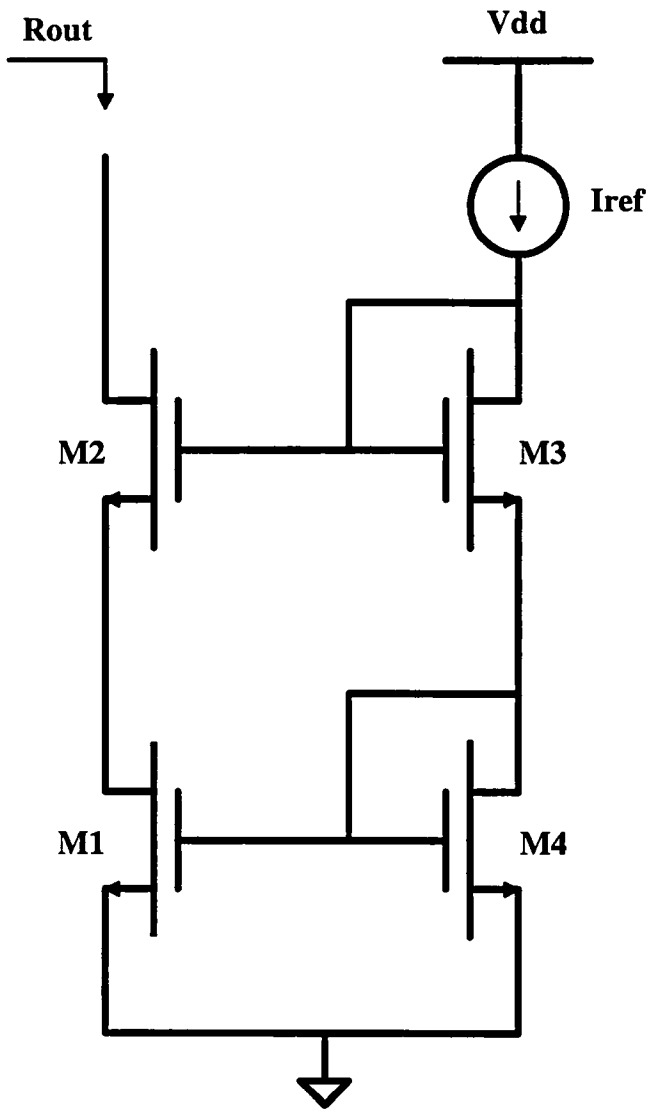


Figure 3-13. Cascode current mirror with increased Rds over the basic mirror.

M1 may be adjusted to achieve the needed frequency response while keeping in mind the fact that matching improves as the WL product increased [17]. Figure 3-14 is an HSPICE plot of the circuit response under worst case conditions using the drawn ratio of (28.8 μ/1.2 μ). Although the large signal does not return to baseline until slightly more than 90 ns, the response is fast enough to allow the remaining discriminator circuitry to provide the required output.

The final component of the input differentiator to be selected involves the method of implementing the gain resistor for the common-gate stage. There are two methods by which this resistance can be implemented: 1) process resistor or 2) MOS transistor biased in the ohmic region. Process resistors such as nwell, diffusion and poly are available within the Orbit 1.2 μ process. Table 3.2 offers some insight into the relative tolerances, density and matching characteristics of several available resistors [18]. Generally speaking, most IC resistors offer bad absolute tolerance although matching can be quite good across a die. Although nwell resistors offer high resistance in a small area, more accurate resistors such as the poly resistor would require large amounts of area to implement the roughly 100 KΩ resistor needed.

Table 3.2. Comparison between Process Resistors

Resistor Element	Range of Values	Relative Accuracy	Absolute Accuracy
Diffused Resistor	10-100 Ω/sq	2%	35%
Poly Resistor	30-200 Ω/sq	2%	30%
n-well Resistor	1-10 KΩ/sq	2%	40%
Pinch Resistor	5-20 KΩ/sq	10%	50%

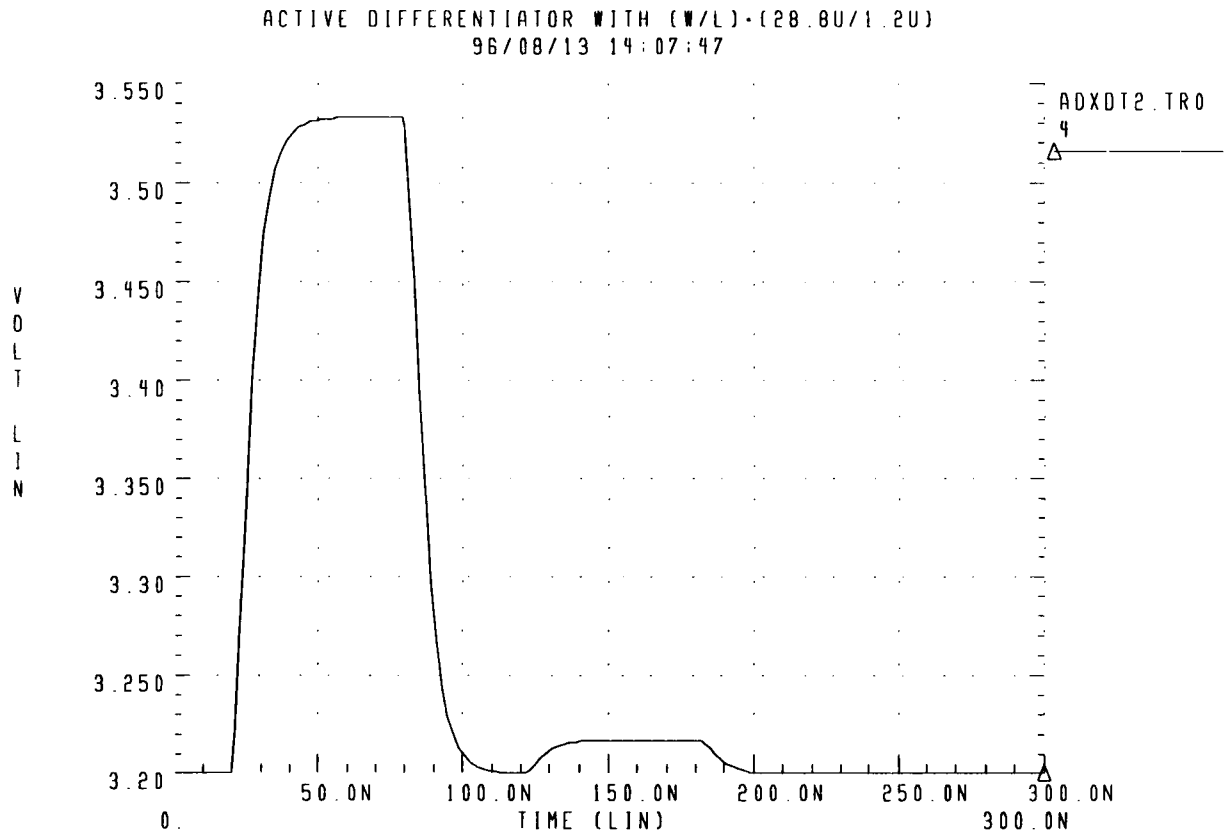


Figure 3-14. Active differentiator response for drawn (W/L).

Perhaps the most serious problem with a fabricated resistor in a topology requiring a fairly accurate value is the inability to adjust the resistor after fabrication if the circuit does not perform properly. The alternative to a process resistor is the use of a MOS transistor biased in the ohmic region as exhibited in Figure 3-15. MOS transistors biased in the ohmic region offer a high but nonlinear resistance in a relatively small area. More importantly an external means of adjustment is provided by the manipulation of the transistor's gate voltage. Based on the area efficiency and adjustability of the MOS transistor, a p-channel device of ratio (4.8 μ/14.4 μ) was selected to realize the gain resistor. The resistance of the device is a minimum for a gate voltage of 0 V and increases as the gate voltage is increased. For a voltage of 0 V the anticipated resistance is roughly 4 KΩ with a resistance of 30 KΩ possible for a gate voltage of 3.5V. Operation between a Vgate of 1 V and 1.5 V is expected to provide the needed range of adjustment for the differentiator.

Figure 3-16 provides the final schematic for the input differentiator circuit. The topology occupies an area of 85 μ x 109.2 μ and consumes less than 100 μW. A simulation of worst case conditions from the extracted layout file may be seen in Figure 3-17. Clearly the differentiator meets the discriminator timing constraints.

3.3.2 Threshold Adjustment

Key to the success of the multiplicity discriminator is the ability to have a threshold circuit which enables a high degree of matching such that a common threshold can control 32 channels of discriminator. As illustrated previously there are

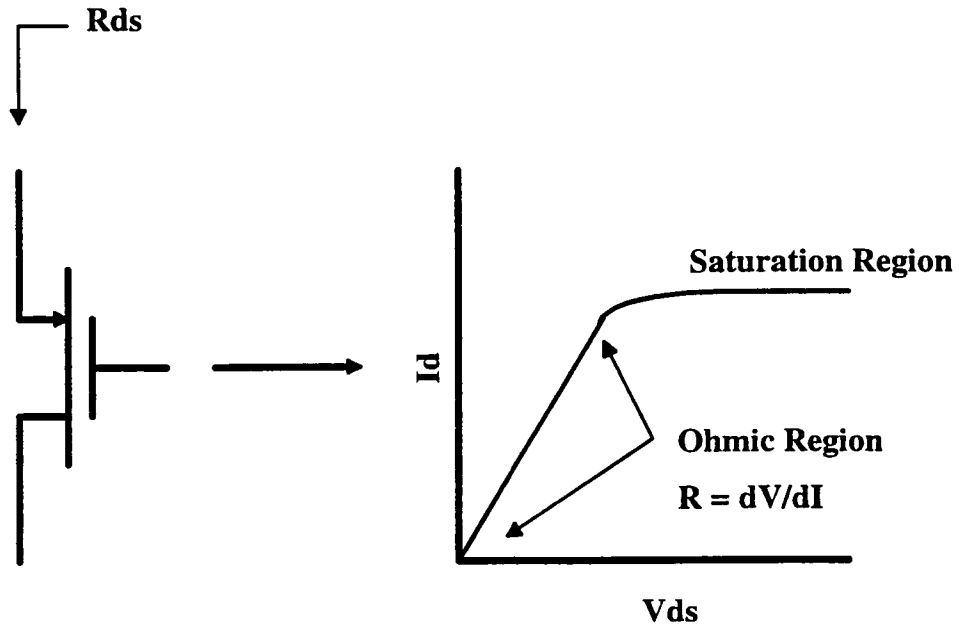


Figure 3-15. Characteristic curve of MOS transistor biased in the ohmic region.

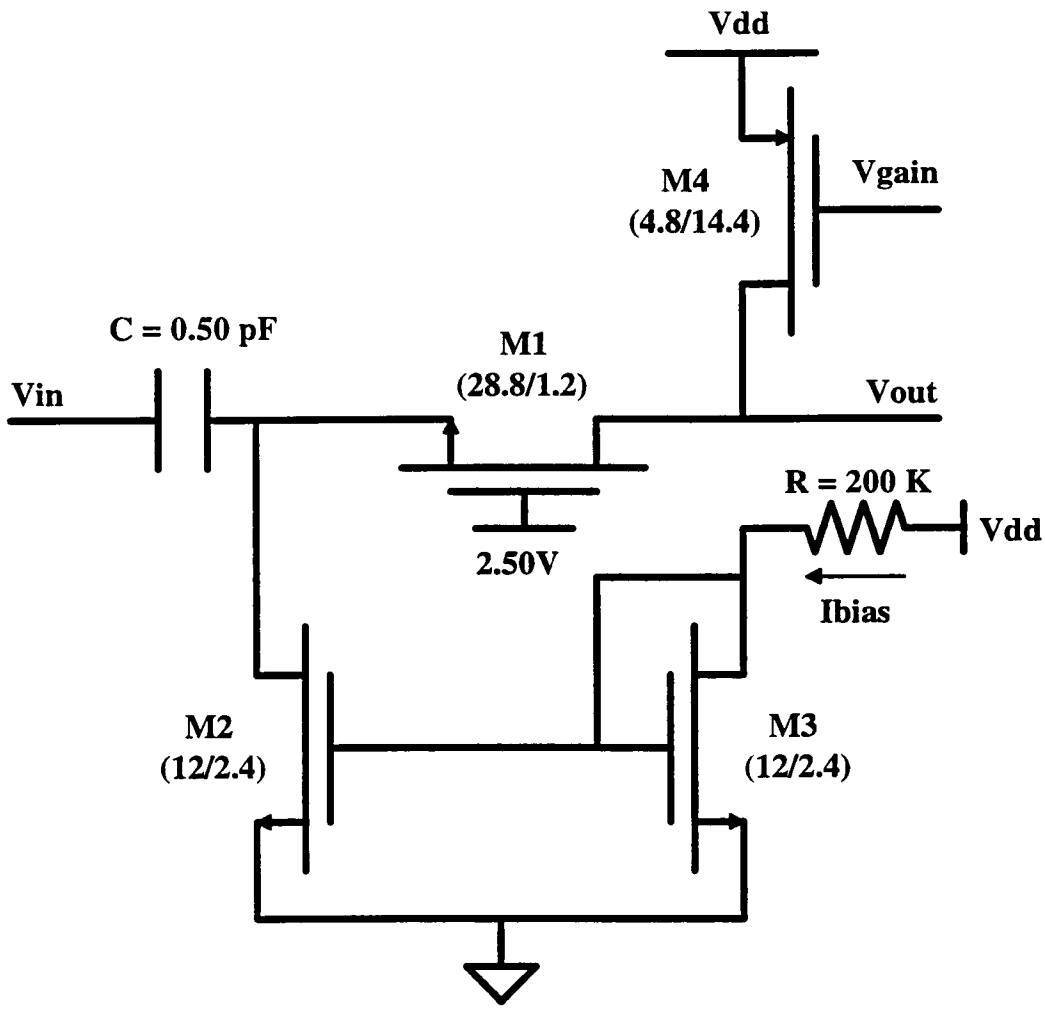


Figure 3-16. Complete schematic of finalized input differentiator circuit.

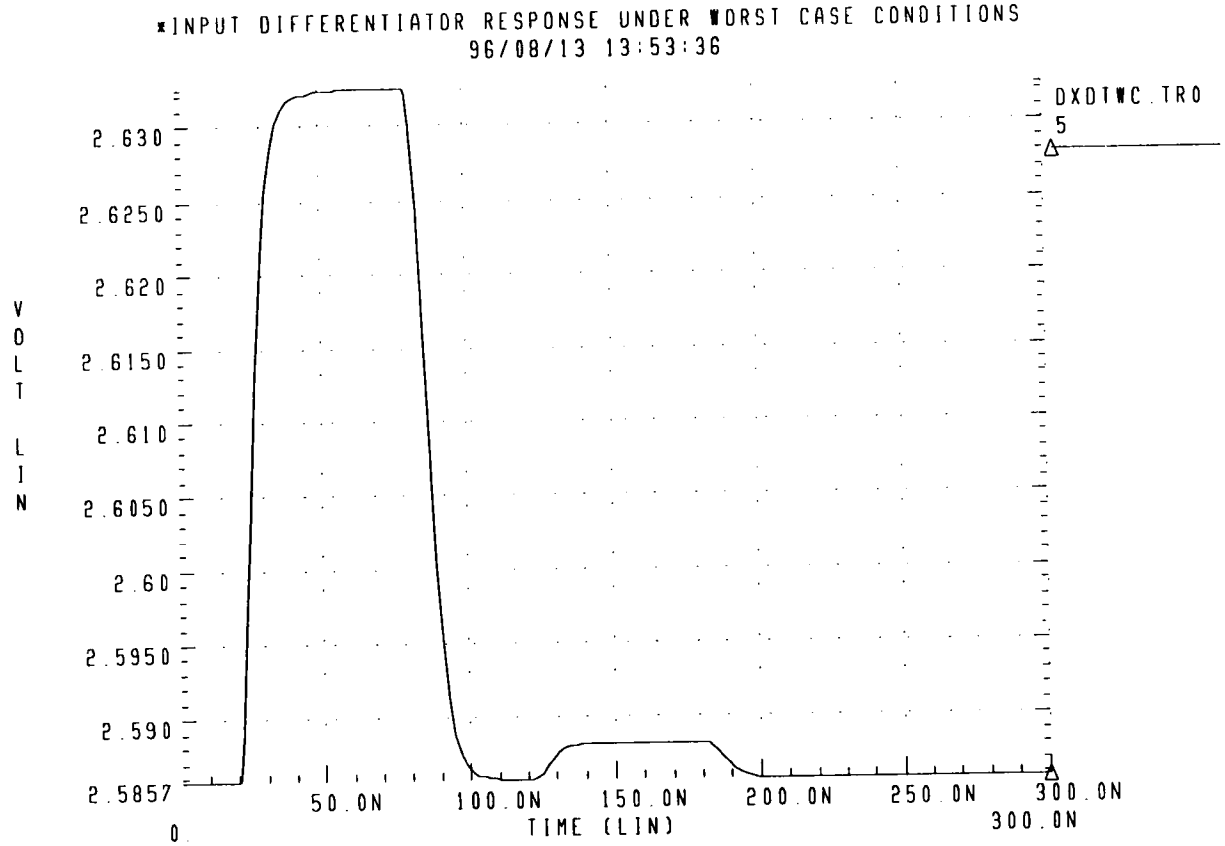


Figure 3-17. Timing response of extracted input differentiator under worst case conditions.

many available comparator topologies but few which allow precision threshold matching. The threshold circuit to be implemented in the multiplicity discriminator is identical to a threshold circuit developed at ORNL for use in a constant-fraction discriminator (CFD) needed for the EMCal and RICH systems of PHENIX. Matching for the circuit of Figure 3-18 has been measured to be on the order of ± 2 mV to ± 3 mV for an 8 channel prototype CFD circuit [19].

The design uses 5 active transistors and 1 transistor connected as a capacitor for bypass purposes to form a differential-to-single ended conversion as well as threshold adjustment capability. With a threshold setting of 0 V and no input applied, M27 and M28 are sized such that they require more current than M29 and M30 can source resulting in the output being pulled low. When a differential input of appropriate magnitude is received, M29 and M30 source more current than M27 and M28 can sink which results in the output being pulled high. It should be noted that M28 has been sized larger than M27 to further insure the output remains lower than the trip point of the following inverter for differential signals smaller than those necessary to trigger the discriminator. Transistor M26 serves the purpose of external threshold adjustment. As Vthresh is increased, M26 begins to turn on and rob current from M27 resulting in less current being mirrored into M28. Less current in M28 means less signal amplitude needed to source all the current M28 can sink. As a result, the minimal differential input required to force the output to the high state has decreased. Table 3.3 is a comparison of the differential signal required to achieve a high output for varying Vthresh values.

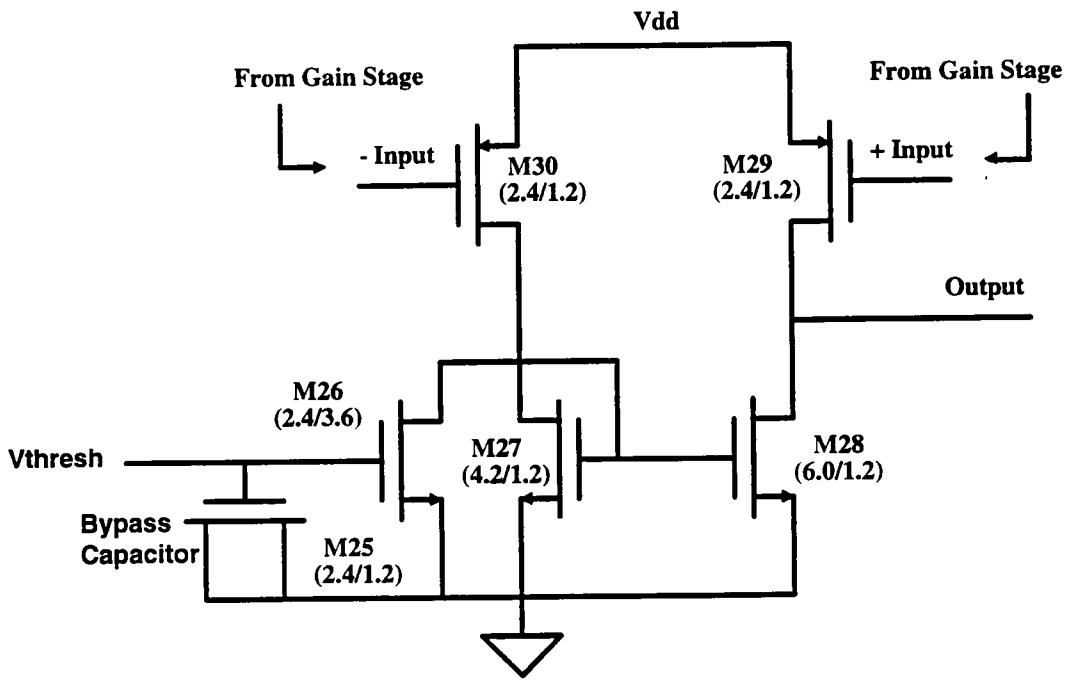


Figure 3-18. Complete schematic of threshold adjustment circuit for the multiplicity discriminator.

Table 3.3. Input Required to Trigger Discriminator as a Function of Vthresh

Threshold Voltage Setting (V)	Discriminator Input (mV)	Threshold Circuit Differential Input (mV)
0.90	75	315
1.00	70	290
1.10	60	275
1.20	55	245
1.30	40	180
1.40	20	95

From Table 3.3 it is evident that the circuit only allows for roughly 55 mV of adjustment. Additionally, the minimal differential signal capable of producing a high output for any setting of Vthresh is approximately 95 mV. Below this signal level the circuit will not fire regardless of the external threshold voltage. When the minimal differential signal is applied to the inputs of the circuit, an output similar to Figure 3-19 is produced. It should be noted that the effects of the long pulse tail decay shown in Figure 3-19 are eliminated by the addition of an inverter stage following the output. Since the high gain inverter makes a sharp transition after the trip voltage is reached, the excessive transition delay of the threshold circuit is not seen by the output current switch of the multiplicity discriminator. The circuit, including inverter, requires an area of 85 μ x 50 μ and consumes approximately 130 μW of power from a single +5 V supply. Due to the open loop nature of the threshold adjustment circuit of Figure 3-18, temperature variations which generate changes in mobility and device threshold would drastically affect the performance of the discriminator. Fortunately, the MVD

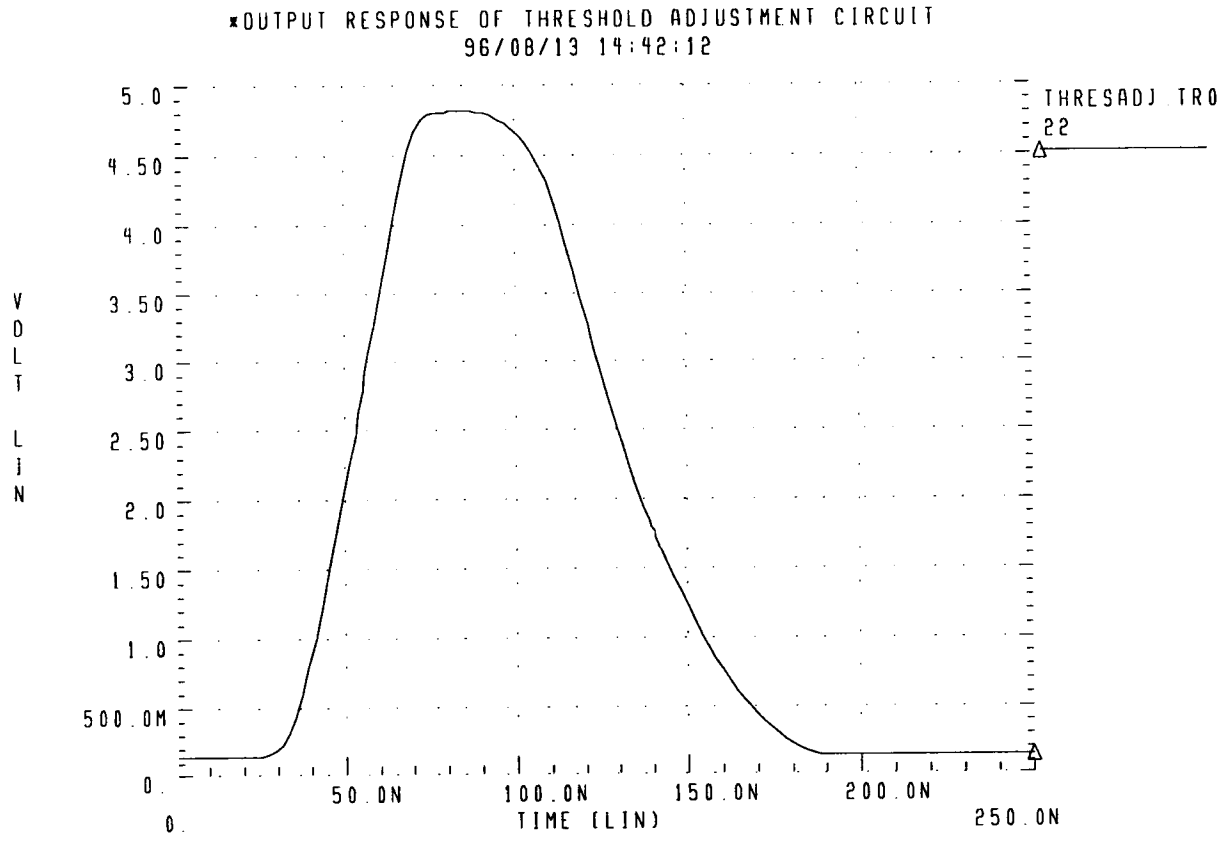


Figure 3-19. Output response of threshold adjustment circuit.

FEE operate within a constant temperature environment which eliminates these concerns.

3.3.3 Gain Stage

The need to obtain a 300 mV differential input signal to trigger the threshold circuit required the development of an additional gain stage between the input differentiator and the comparator circuit. To achieve a differential signal of this amplitude for the minimal input of 20 mV, a differential gain of roughly 15 V/V must be established. It should also be noted that any gain stage designed for use in the multiplicity discriminator must allow for a high performance, small area, low power implementation. One such topology capable of achieving adequate results is the differential amplifier of Figure 3-3 [15]. The ability of differential amplifiers of this type to amplify the input difference while maintaining a high common-mode rejection ratio (CMRR) which enables the rejection of signals common to both inputs, makes them attractive for used in analog circuits requiring these differential characteristics.

By making a slight modification to the circuit of Figure 3-3, the topology of Figure 3-20 which offers improved matching and a better gain to area ratio may be realized. The circuit provides n-channel inputs with p-channel "enhancement" load devices. Unlike the common active load connection of Figure 3-3 where only one transistor is diode connected, enhancement loads allow both devices to be diode connected. Such a configuration enables the Vgs of both devices to be equal which in turn allows for better device matching among the active loads. Since the value of

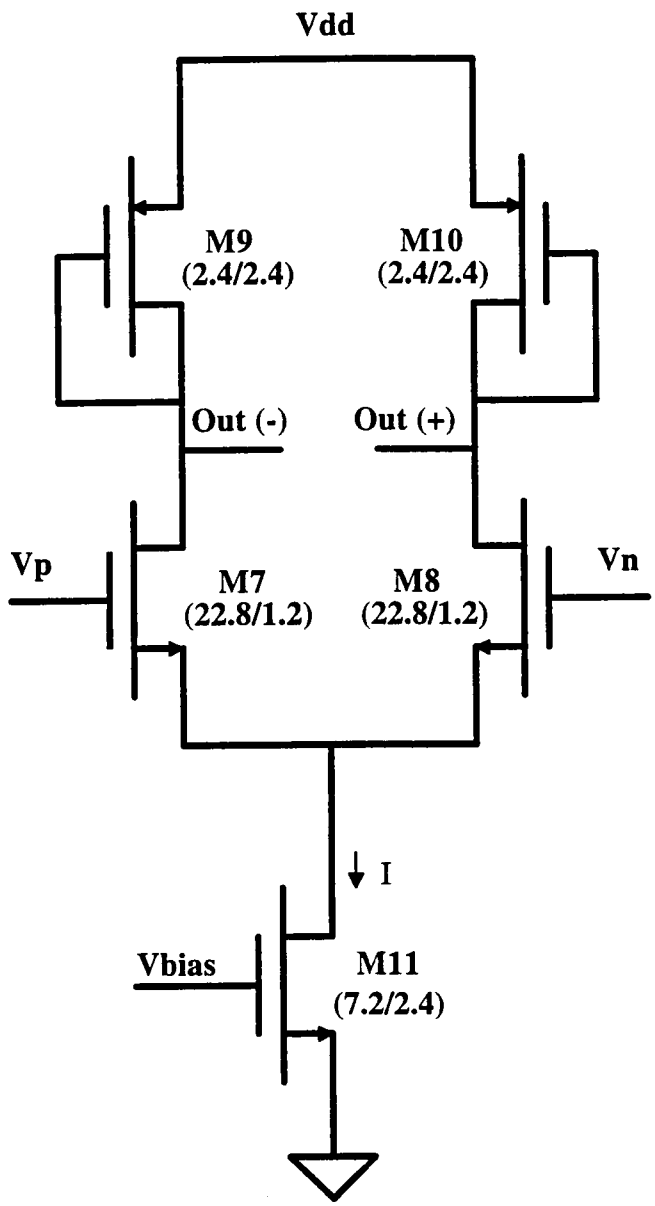


Figure 3-20. Differential amplifier with p-channel enhancement loads.

resistance seen looking into the active load is given by roughly $r_o = 1/gm$, the use of p-channel devices provide a higher gain for the same size devices than do n-channel loads. This is due to the lower gm of the p-channels caused by reduced mobility of holes (300 cm^2/V sec) over electrons (600 cm^2/V sec) [20]. The single-ended gain for this topology may be shown to be approximately

$$A_V = \left[\frac{\mu_N (W/L)_N}{\mu_P (W/L)_P}\right]^{1/2} \approx \left[\frac{2(W/L)_N}{(W/L)_P}\right]^{1/2} \quad \textbf{(3.21)}$$

From the equation it is evident that the gain for the circuit goes as the square root of the W/L ratios of input devices to load devices. Thus maximum gain should be achieved by minimizing the W/L of the load devices while maximizing the W/L of the input devices to within the allowable area constraints. One potential drawback to the use of p-channel loads with n-channel input devices is the potential variation in the mobility of holes and electrons from process run-to-run. If n-channel loads were used any change in the mobility of electrons would be exhibited equally by both the input and load thus resulting in no net change in the gain of the circuit. Whereas the use of p-channel loads allows for a gain which is dependent on both electron and hole mobility which may or may not track from run-to-run.

Power consumption for the circuit is of considerable importance as with all circuitry associated with the multiplicity discriminator. For this reason a bias current of 12 μA was established as an upper limit for the differential gain stage. Generation of the tail current for the differential pair is accomplished by mirroring from the main circuit bias included in the input differentiator. Based on this bias current, the W/L

ratios of M7-M10 may be manipulated to achieve the highest possible differential gain. Using BSIM models the maximum achievable gain was accomplished by letting the load ratio be unity while sweeping the W/L of the input devices until a maximum gain was reached. The resulting W/L for M7 and M8 was determined to be 22.8 μ/1.2 μ which for a unity load ratio produced a gain of roughly 5 V/V.

Frequency response of the gain stage is extremely critical. Due to the time delays associated with the input differentiator, the gain stage must perform the amplification function with minimal delay if the discriminator is to be live for every beam crossing . Although the impedance of the loading node of the differential pair is given by roughly 1/gm, the restriction of bias current (only 12 μA) will result in a fairly high impedance node. For this reason it is crucial that parasitic capacitances at this node be minimized. Since M9 and M10 are in saturation, the majority of the parasitic capacitance comes from the gate-to-source capacitance presented in Eq. (3.17). Minimizing the W and L for these devices will thus reduce the total nodal capacitance. For a ratio of (2.4 μ/2.4 μ) the approximate contribution of the load devices to the nodal capacitance is roughly 4 fF. Devices M7 and M8 function as common-source amplifiers and thus have a corresponding Miller capacitance associated with them which will add to the total capacitance of the loading node. For the device sizes found previously of (22.8 μ/1.2 μ), the Miller capacitance is given by [21]

$$C_{miller} = Cgs(1 - A_V) \qquad \textbf{(3.22)}$$

Adding Eqs. (3.17) and (3.22) provide a total parasitic capacitance of roughly 24 fF. Using an extracted circuit and BSIM models, HSPICE calculates a capacitance of 32.7

fF for this node. A plot of the pulse response for the amplifier may be seen in Figure 3-21.

Another important characteristic is the dynamic range capabilities of the differential amplifier. The positive common-mode range (CMR+) is given by

$$CMR+ = Vdd - \left(\frac{I_{tail}}{\mu C_{OX}(W/L)} \right)^{1/2} - |V_{TO}|_9 + V_{T7} - V_{IN} \qquad \textbf{(3.23)}$$

where Id = 12 μA and μC_{OX} = 20 $\mu A/V^2$ as given in the Orbit 1.2 μ process parameters data located in Appendix 1. Substituting into Eq. (3.23) and calculating results in a CMR+ of roughly 3.6 V. Similarly the CMR- may be expressed as

$$CMR- = \left(\frac{I_{tail}}{\mu C_{OX}(W/L)_7} \right)^{1/2} + V_{T7} + Vds_{SAT11} \qquad \textbf{(3.24)}$$

In the previous discussion of the input differentiator the dc output voltage was found to be from 3.5 V to 4 V. From the calculated values of CMR+ and CMR- it is clear that the dc voltage of the input should be lowered to achieve more optimal performance. To accomplish this task a basic source follower can be added prior to the input of the differential amplifier to provide the needed level shifting. A summary of several critical performance parameters, both hand analysis and simulated, for the differential amplifier is presented in Table 3.4.

The results of Table 3.4 point out the fact that the required minimal differential gain of 15 V/V was not achieved with the proposed circuit. Instead, the simulated gain of the circuit is just slightly over half of that desired. One attractive aspect of differential amplifiers is their ability to be directly coupled to one another without the

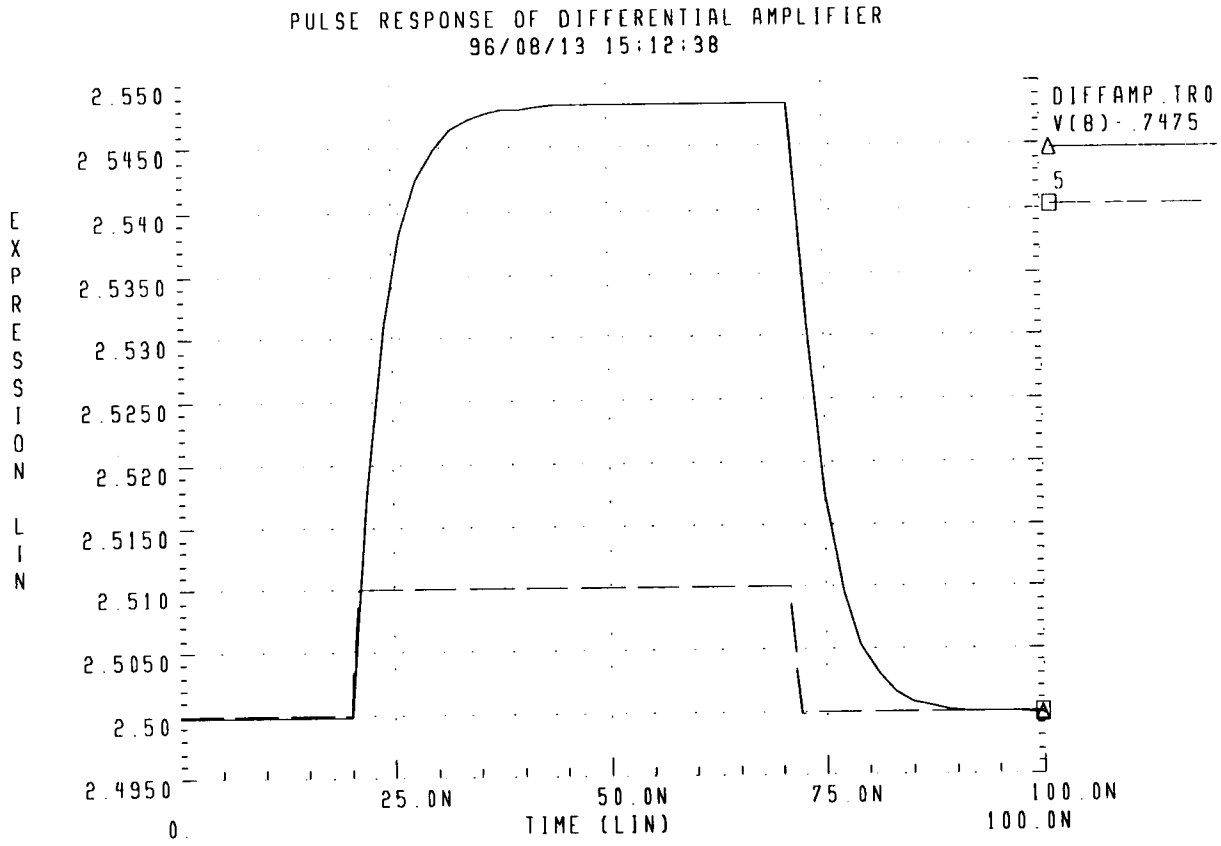


Figure 3-21. Pulse response of differential amplifier.

Table 3.4. Summary of Differential Amplifier Characteristics

Characteristic	Hand Result	Simulated Result
Gain (V/V)	≈ 6	4.9
Risetime (ns)	≈ 5	10
CMR+ (V)	3.6	3.8
CMR- (V)	2.7	2.9
Dynamic Range + (mV)	400	600
Dynamic Range - (mV)	500	300
Power (μW)	60	60

need for coupling capacitors. Due to time constraints in the development of the circuit, it was decided to implement a second identical gain stage. Since the combined gain of the two stages will be higher than that required to trigger the threshold circuit, the gain requirements for the input differentiator may be reduced to compensate. From Table 3.4 the dynamic range and gain capabilities of the differential amplifier are such that the output of the second stage just saturates for the smallest input signal. As long as a differential signal of 300 mV is provided to the threshold circuit, the discriminator will fire.

3.3.4 Elimination of Offset

Every topology containing a differential pair amplifier is restricted by a nonideal offset voltage which limits the obtainable dc precision of the circuit. Offsets consist of systematic errors created by the particular topology implemented and mismatch induced errors which result from nonideal device characteristics. As illustrated by Figure 3-22 the lumped sum offset voltage may be thought of as a

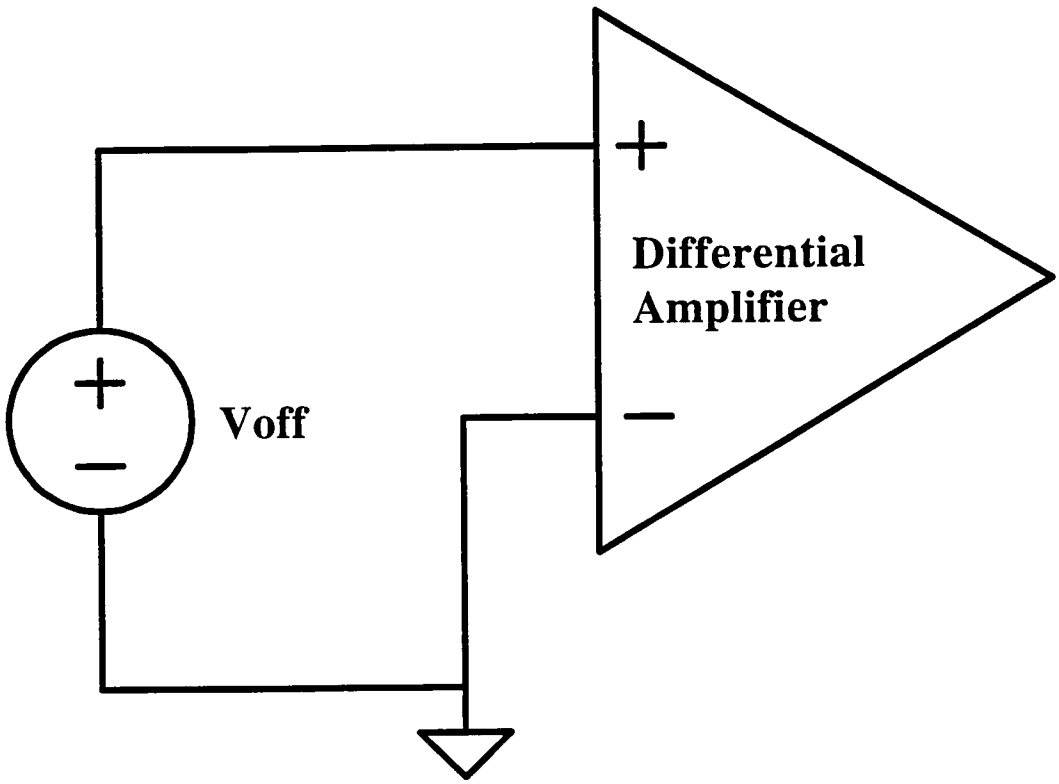


Figure 3-22. Equivalent representation of differential pair offset voltages.

voltage source connected to the input terminal of the amplifier. When multiplied by the gain of the amplifier, the offset voltage can become a major source of error.

Unlike differential amplifiers utilizing bipolar transistors, differential amplifiers using MOS devices can exhibit offsets in the 10 mV to 20 mV range. These offset results primarily from mismatches in the Vgs of the input devices or

$$V_{OS} = V_{GS1} - V_{GS2} \tag{3.25}$$

and may be shown to reduce to

$$V_{OS} = \Delta Vt + \frac{(Vgs - Vt)}{2}\left[\left(\frac{-\Delta RL}{RL}\right) - \left(\frac{\Delta(W/L)}{(W/L)}\right)\right] \tag{3.26}$$

where the R_L term incorporates the mismatch associated with the load devices into a complete expression for offset [22]. Clearly from Eq. (3.36) it may be observed that increasing the W/L ratio of the devices reduce the effects of any photolithographic errors induced in processing [17]. It should be noted that for the case of the MOS device, the threshold voltage given by

$$V_{TO} = \phi_{MS} + 2\phi_F + \frac{Q_B}{C_{OX}} - \frac{Q_{SS}}{C_{OX}} \tag{3.27}$$

can vary across a wafer among equally sized transistors due to nonideal processing effects. Errors such as these are especially troublesome since they are direct functions of the cleanliness and accuracy of the process and not dependent on the actual design.

The differential amplifier described previously contains all of these associated dc errors. Device mismatch due to photolithographic effects are especially pronounced due to the minimal length of the input devices. Increasing this dimension

and applying a common centroid type layout would improve matching performance tremendously; however, the remaining offsets might still be unacceptable for the precision required by the multiplicity discriminator. For example, if the total referred input offset voltage for two gain stages were 10 mV, when multiplied by the combined gain of the stages, a dc error of roughly 150 mV results. This error is well within the required amplitude needed to trigger the threshold circuit and fire the discriminator for certain Vthresh setting. There are several available means by which the problem of offset voltages may be addressed within the design. These methods include ac coupling the amplifiers, using switched dc feedback and continuous dc feedback. Each of these methods shall be discussed in relation to their acceptability for use in the multiplicity discriminator.

The most common means of eliminating unwanted offsets is the use of an ac coupling capacitor between stages to block the dc voltage. This method offers a straight forward approach to solving the offset problem through the use of passive components as illustrated by Figure 3-23. However, there are several disadvantages to using ac coupling as a means of offset elimination. One of the main disadvantages is the large amount of area required to implement integrated capacitors. Since the signal is taken differentially between the stages, two capacitors would be required for each stage. Additionally, with the dc bias blocked from one stage to the next, the n-channel input differential pair would need to be biased from a reference voltage or converted to p-channel inputs for proper biasing. Utilizing a resistive network to establish the appropriate dc bias (shown in Figure 3-23) creates problems similar to those seen in

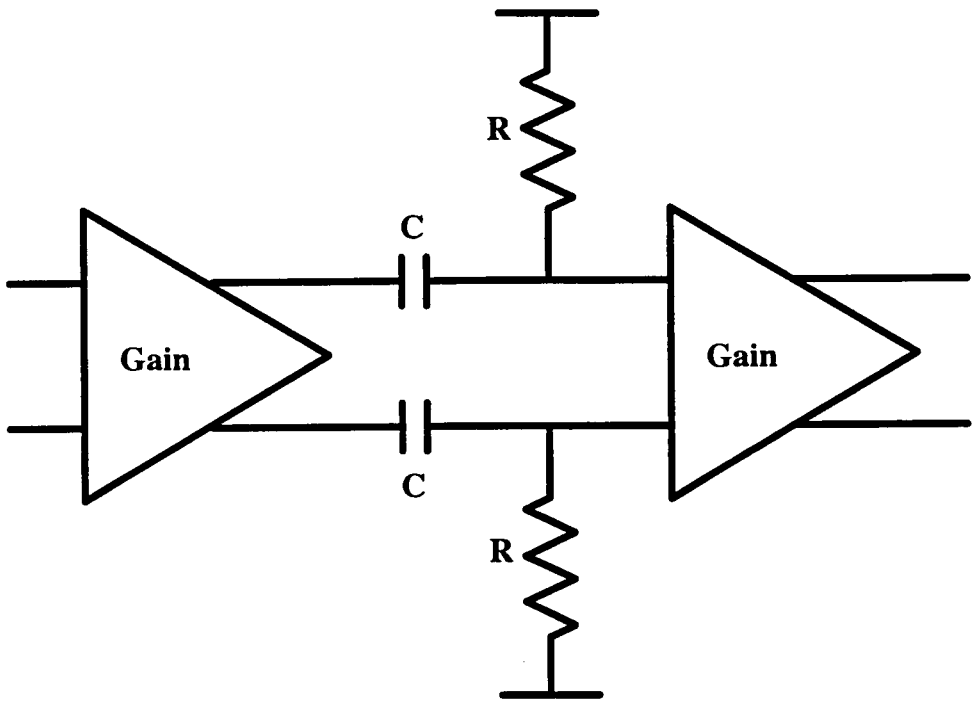


Figure 3-23. AC coupling method of offset elimination.

the passive differentiator. Setting the frequency corner high enough to meet the speed requirements of the design would greatly attenuate the corresponding signal. Such attenuation would require higher gain amplifiers which occupy a much more significant amount of area. Since one of the main requirements of the multiplicity discriminator was for a minimal area design, the use of ac coupling was eliminated as a feasible option.

Both switched and continuous feedback require the implementation of a dc feedback loop similar to the one shown in Figure 3-24 to eliminate the nonideal offset voltages. Through the use of the dc feedback limit amplifier and the low frequency pole created by the R_ZC_Z time constant, an error signal is fed back into the negative terminal of the discriminator gain stage. Although both methods utilize roughly the same circuitry and would require the same amount of silicon area, each method has distinct advantages and disadvantages when evaluated on the basis of a particular application. As implied by the name, switched feedback involves the connecting and disconnecting of the negative feedback depending on whether a signal is being applied to the circuit. By disabling the feedback while the signal is present, switched feedback minimizes rate effects which can produce feedback offsets provided the signal rate and/or amplitude is large enough [19]. To perform the auto-zeroing function a switch must be placed in series with R_Z and a guaranteed signal-free time provided to serve as the switching control signal as illustrated in Figure 3-25. The implementation of such a function would require an additional input pin to carry the signal-free time onto the chip. When the input signal is applied, the switch control would be such that the

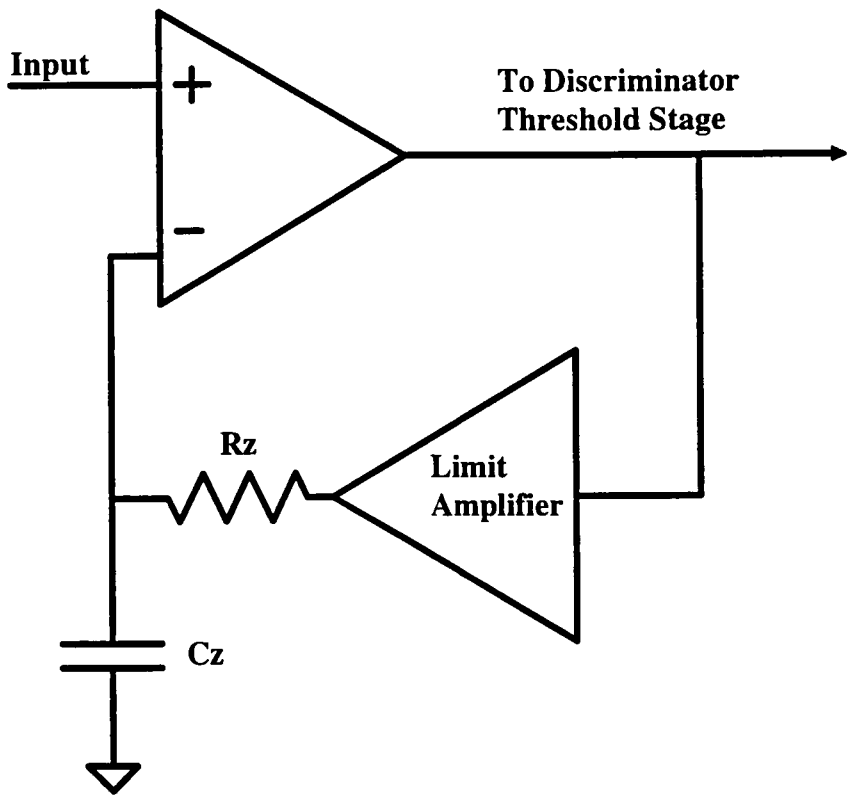


Figure 3-24. Basic feedback circuit required to implement either switched or continuous dc feedback.

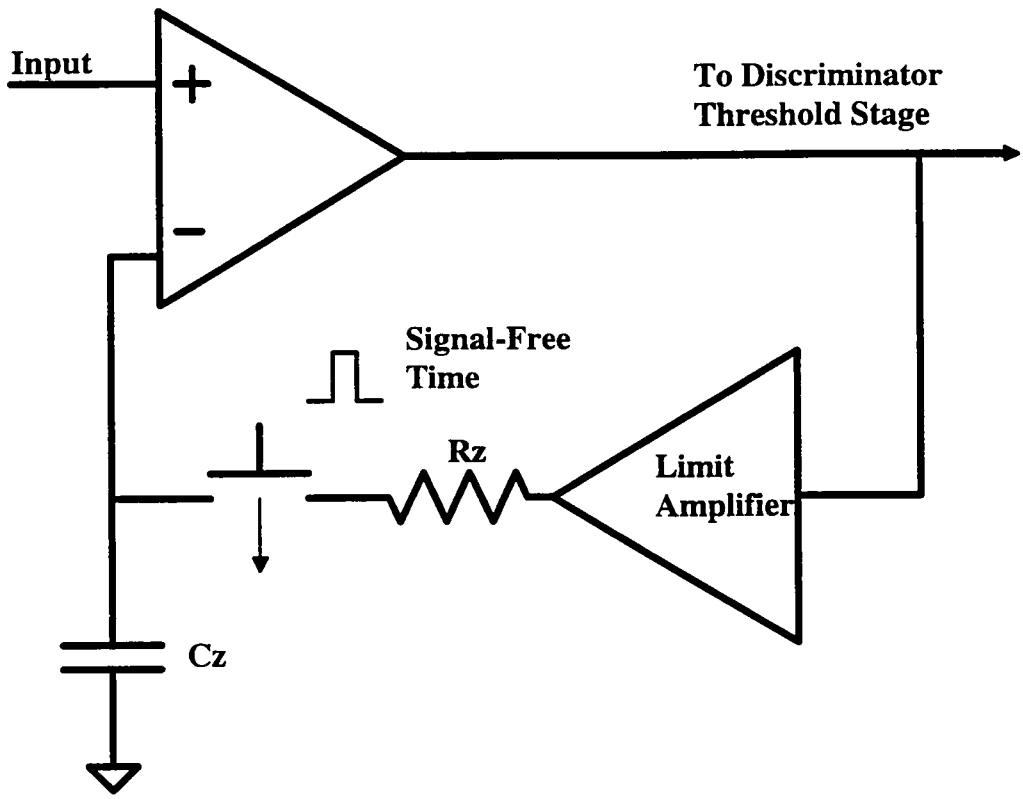


Figure 3-25. Modified dc feedback loop adequate for switched feedback.

feedback is connected and then disconnected when the applied signal is terminated. Since an ideal switch cannot be implemented with MOS devices, certain nonideal effects arise from the use of a switch. Due to the intrinsic gate-to-source and gate-to-drain parasitic capacitances, Cgs and Cgd respectively, a capacitive divider is established between the gate of the switching device and the hold capacitor C_Z [23]. For a hold capacitor of 2 pF with a switch Cgd of roughly 10 fF and a control voltage of 5 V applied to the gate of the switch, as much as 25 mV could be injected onto the hold capacitor during a switch transition. Additionally due to the nonlinear nature of Cgs and Cgd, the perturbation voltage injected onto the hold capacitor will also be nonlinear. The existence of this nonlinear charge injected voltage within the feedback compensation loop can lead to threshold mismatch problems and represents a major disadvantage of this method of offset voltage elimination.

Continuous feedback offers a solution to several of the problems associated with switched feedback. Since there is no switching taking place within the dc feedback loop, the nonideal effects of charge injection which lead to discriminator threshold variations are eliminated. Obviously the need for a signal-free time and additional input pin are also relinquished. However, because the feedback is now connected while the input signal is being applied, a small amount of charge is injected onto the hold capacitor with each new input. As in the case of the switched feedback the charge injected onto the hold capacitor constitutes an offset voltage which can lead to threshold matching problems. However, unlike the switched feedback, method

charge injected by continuous feedback is a direct function of the rate and amplitude of the input signal. The injected offset may be given by

$$V_{ERROR} = |V_{LIMIT}|(W)(R) \quad \textbf{(3.28)}$$

where V_{Limit} is the limit voltage required to correct for the expected range of offset voltage, W is the average signal width and R is the average rate of the input signal [19]. For the conditions expected in the multiplicity discriminator, a limit voltage of ± 300 mV, pulse width of 90 ns and rate of 1 KHz produce an offset error of roughly 27 μV. Thus if the amplitude-rate product is kept small enough, effects of the offset are negligible. After extensive simulations, the continuous dc feedback method of offset elimination was determined to be the most feasible for the design.

3.3.5 DC Feedback Loop

Implementation of a continuous dc feedback loop like the one of Figure 3-24 to meet the needs of the multiplicity discriminator requires the development of several key elements such as an appropriate R_ZC_Z time constant and limit amplifier. In order to maintain sufficiently low ac ripple on the input it is essential that the R_ZC_Z time constant be long. Also, if the R_ZC_Z time constant does not become the dominant pole, instabilities will occur due to interaction among other system poles. Ideally the R_Z element shown in Figure 3-24 is representative of the limit amplifier's output resistance, however if an appropriately large R_Z is not achieved it may be necessary to add some form of series resistance element.

To provide the needed offset voltage elimination obtainable by continuous dc feedback an appropriate limit amplifier must be designed. The limit amplifier functions as a linear amplifier providing an output which is proportional to the input until a limit voltage level is reached. Once the limit voltage is reached, the amplifier must hold this level until the input signal returns to the linear range of the limit amplifier. By establishing the limit voltage slightly larger than the expected offset voltage, the negative feedback can effectively eliminate the nonideal offsets of the cascaded gain stages. The topology used to implement the limit amplifier may be seen in Figure 3-26. The limit amplifier is made up of devices M17 through M22 and is surrounding the second gain stage (M12-M16) of the discriminator. Under ideal quiescent conditions where no threshold voltage mismatches exist to cause offset voltages, M20 mirrors more current to M21 and M22 than M18 and M19 can source which causes the dc output voltage to move toward zero. However, since mismatches do occur in the differential amplifiers, the dc output is forced to a non-zero potential. As the differential output signal of the gain stage increases, M20 mirrors less current to M21 while M18 begins to turn on harder due to the increased Vgs. This results in a positive linear ramping of the drain of M19 and M22 whose gain is given by

$$A_V = \frac{gm}{(gds19' + gds21')} \tag{3.29}$$

where $gds_{19'}$ and $gds_{21'}$ can be obtained by applying Eq. (3.20). When the output reaches a limit voltage of 300 mV above the quiescent baseline, the amplifier's dynamic range is reached and the output ceases to increase with increasing differential

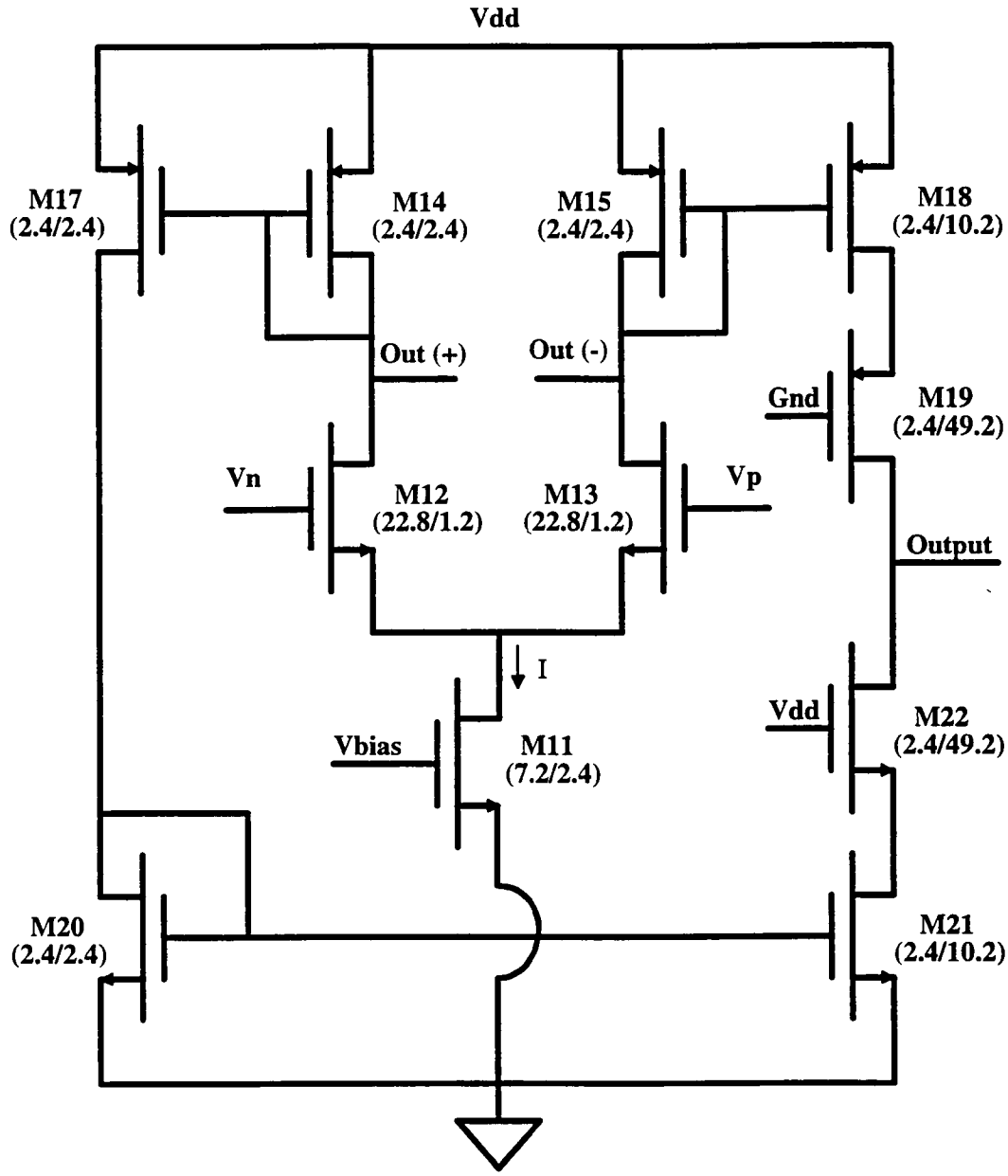


Figure 3-26. Limit amplifier surrounding the second gain stage of the multiplicity discriminator.

signal. As the differential signal decreases to within the range of the limit amplifier, the dc output tracks the input once again.

It is of utmost importance to the stability of the circuit that the pole created by the feedback circuitry dominate the closed loop response. In order for this to happen the R_ZC_Z time constant must be much longer than any other time constant associated with the circuit. Area considerations lead to the desire to minimize the size of the hold capacitor utilized while maximizing the effective R_Z of the system. The cascode configuration of the high gain amplifier allows for a much increased output resistance which may be represented by

$$R_{OUT} \approx r_{O19}[1+(g_{m19}+g_{mb19})(r_{O18})]+r_{O18}\|r_{O22}[1+(g_{m22}+g_{mb22})(r_{O21})]+r_{O21} \qquad \textbf{(3.30)}$$

Since r_o is directly proportional to channel length L, constructing devices M19 and M22 especially long further increases the output resistance of the limit amplifier. Substitution into Eq. (3.30) using calculated gm and r_o values for an Id =1.36 μA yield a resistance of roughly 50 MΩ seen looking back into the limit amplifier. For a hold capacitor of 2 pF, the R_ZC_Z time constant produces a dominant pole at 1600 Hz. However, simulations proved this frequency corner to be too high to establish a stable circuit. To improve the stability of the circuit, either the hold capacitor C_Z or the output resistance of the limit amplifier R_Z must be increased. Leaving the R_Z constant and increasing C_Z until a corner frequency of 800 Hz is obtained requires a 4 pF double poly capacitor occupying an area of 8000 μ^2. Alternatively, the same frequency corner could be achieved by increasing the effective R_Z by roughly 100 MΩ. Implementation of such a high valued process resistor would also require a rather large

area and could vary in absolute value by as much as 50% from chip-to-chip. Although absolute value of the resistance is not critical, there does exists a minimal value that must be achieved to maintain circuit stability. Thus in order to guarantee a resistance of at least 100 MΩ, a resistor of value 200 MΩ must be fabricated. Fabricated resistors of these values are completely impractical for integrated circuit design. Another means by which the resistor (up to several MΩ) can be implemented involves the use of a MOS transistor biased in the ohmic region as was done in the input differentiator design.

As previously discussed, high valued resistors can be achieved in a comparably small area when implemented by a MOS transistor biased in the ohmic region. Since resistance for such a device is directly proportional to the channel length L, higher values may be obtained by simply increasing the channel length. After extensive simulations it was determined that an n-channel device with drawn dimensions given by 1.8 μ/95.4 μ should be adequate to maintain circuit stability and allow the dc feedback to eliminate the offsets. To further increase the versatility of the prototype discriminator it was decided to use a transmission gate instead of a single n-channel device. By using a transmission gate in the feedback loop to establish the needed resistance, the concept of switched feedback could be implemented if the continuous feedback failed to provide sufficient results. Under normal continuous feedback operating conditions the control voltage applied to the gate of the switch is such that only the n-channel device is active. The resulting resistance is then given by

$$R_{ON} = r_{dsn} \| r_{dsp} \approx \frac{1}{\lambda_n I_D} \tag{3.31}$$

and may be seen from the HSPICE simulation of Figure 3-27 as function of bias voltage. However, if the continuous feedback fails to work, the switch is available for the auto-zeroing function required by switched feedback. Utilizing the transmission gate structure to realize the needed resistance results in the topology of Figure 3-28 to generate the dc feedback dominant pole.

One potential problem with the limit amplifier and transmission gate design is the area required to construct the long channel devices. Due to the 85 μ pitch requirement a horizontal layout of these devices would be required and would add roughly 100 μ to the length of the discriminator. Since the channel length for these devices can not be reduced and the dc feedback still function properly, an alternative layout must be found. Two optional layouts may be seen in Figure 3-29. Figure 3-29a illustrates a serpentine layout in which the device is sized to fit within the 85 μ pitch by zig zagging the transistor in a snake like fashion. Figure 3-29b shows a vertical "goalpost" layout in which the needed length is halved and a duplicate version is connected in series. The crossbar in the middle of the structure is poly silicon used to connect the gates of the two transistors. Although the serpentine configuration can be implemented in slightly less area (48 μ x 13 μ compared to 52 μ x 18 μ) than the goalpost configuration, both methods represent a significant reduction in discriminator length over conventional transistor layout. However, because of the nonstandard geometry of the transistors, appropriate modeling becomes a major concern. Since no

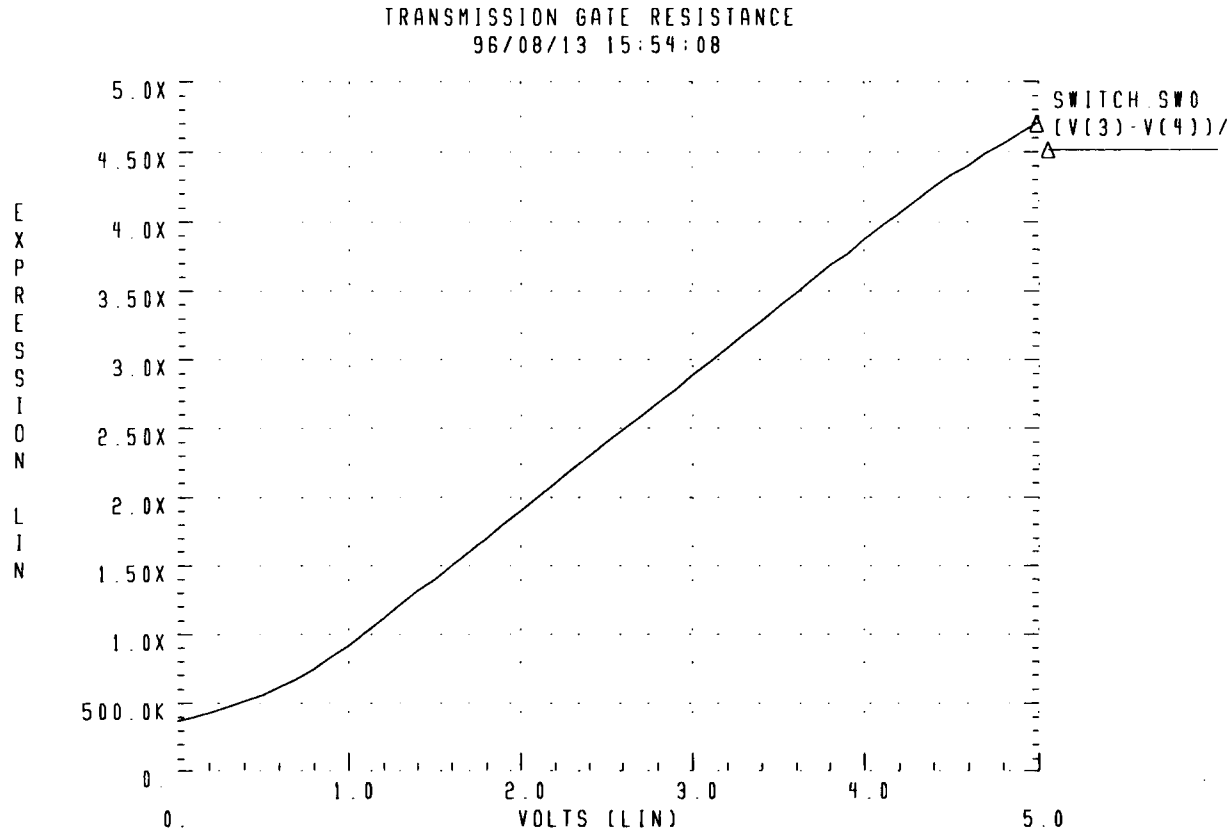


Figure 3-27. Simulated R_{ON} of transmission gate switch.

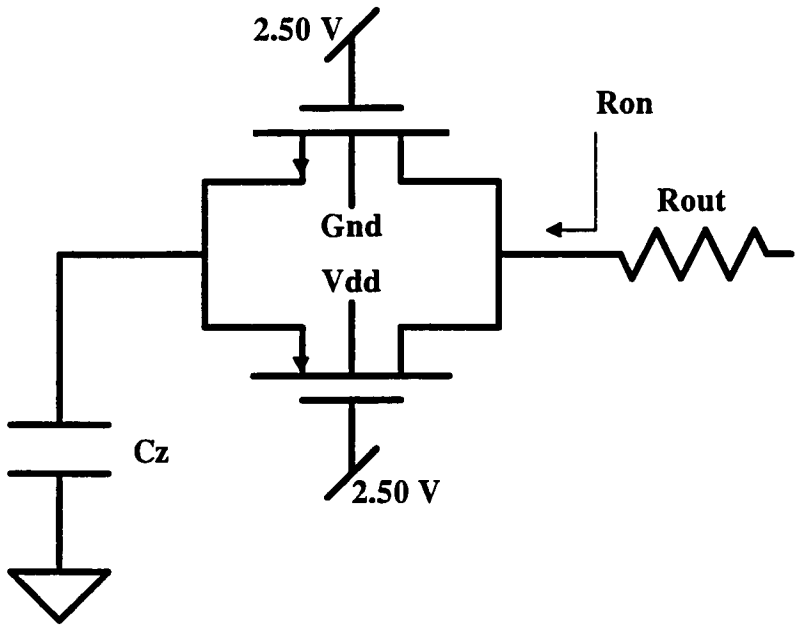
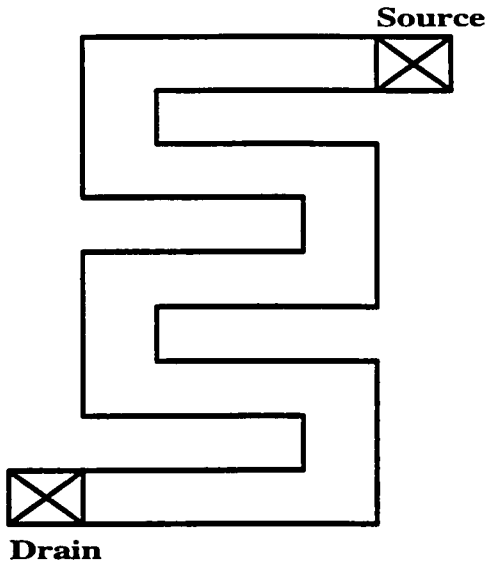
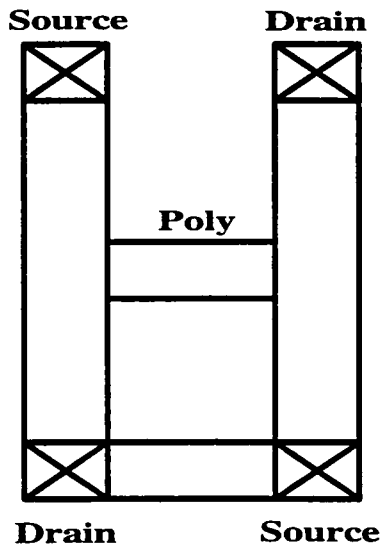


Figure 3-28. Topology utilized to generate DC pole.



(a)



(b)

Figure 3-29. Alternative layout for long-channel transistors. a) Serpentine, and b) Goalpost geometries.

test devices with similar structures existed prior to the design of the multiplicity discriminator, reliable models for these transistors could not be developed. Instead standard BSIM models were used to evaluate the entire dc feedback circuit prior to the submission of the design to the foundry. Both n- and p-channel transistors with serpentine and goalpost geometry were later fabricated and tested. The measured results and device modeling for these test devices will be presented in Chapter IV.

A complete diagram of the dc feedback loop including two gain stages, a limit amplifier, transmission gate and hold capacitor may be seen in Figure 3-30. Combining the gains of the differential and limit amplifiers as a function of frequency yields the closed loop response of the feedback network. Assuming that the dc loop gain T_O is much greater than one, the closed loop gain may be written as

$$A(f) = \frac{(A_{Diff\,1})(A_{Diff\,2})(A_{Limit})}{(1 + j\frac{f}{f_{Diff\,1}})(1 + j\frac{f}{f_{Fiff\,2}})(1 + j\frac{f}{f_{Limit}})} \qquad \textbf{(3.32)}$$

where A_{diff1} and A_{diff2} have been shown to be roughly 5 V/V for small input signals; f_{Diff1} and f_{Diff2} represent the high frequency corner (35 MHz) created by the parasitic capacitances at the output of each differential amplifier; and f_{Limit} is the dominant system pole located at 1500 Hz.

3.3.6 Current Switch

The final component of the multiplicity discriminator is the current switch output circuit. Up to this point the discriminator's output has been characterized by either a logic high (when firing) or logic low (when not firing) state. However, since

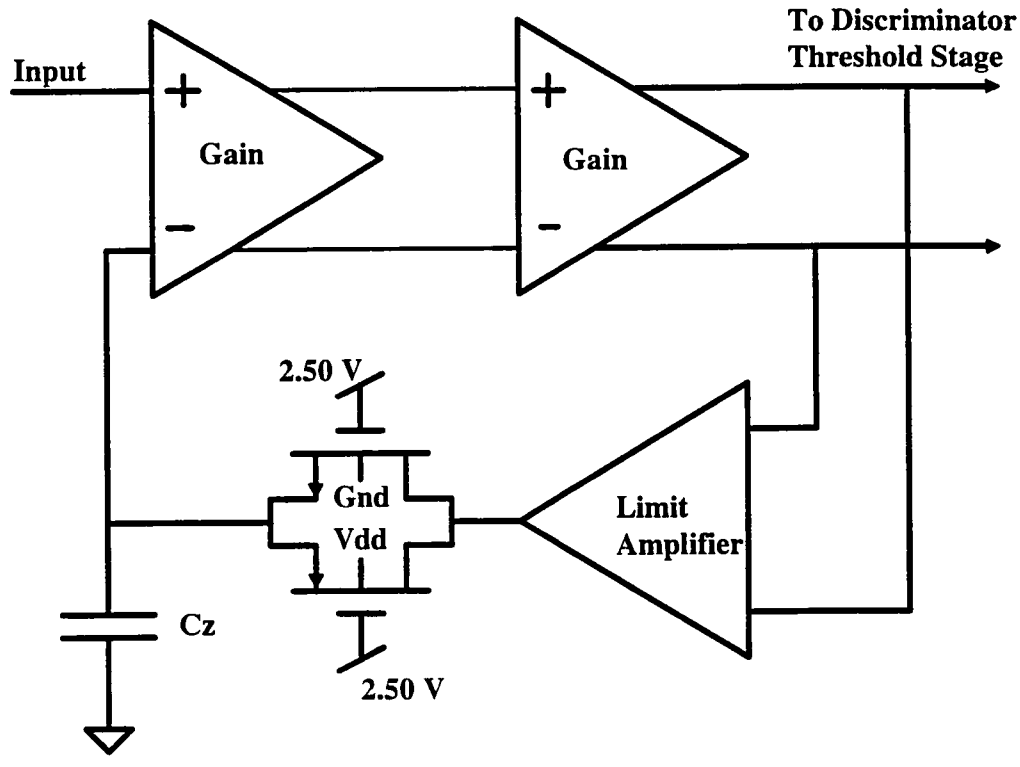


Figure 3-30. Complete block diagram of dc feedback loop.

the discriminator is required to produce a current sum to aide in the determination of event multiplicity for the MVD, a means by which the output voltage level can be converted to an output current is desired. A topology capable of such a conversion may be seen in Figure 3-31. Transistors M1-M4 comprise the bias and reference voltage common to 32 channels of discriminator. When the discriminator fires, the threshold circuit output moves toward Vdd which drives the inverter output to ground. Applying 0 V to the gate of M6 forward biases the source-to-gate junction of the p-channel device and turns the transistor on. With M6 active, current flows through M5 and onto the current summing bus. If however, the system input is such to cause the discriminator not to fire, the high state of the inverter reverse biases the source-to-gate junction of M6 and turns the device off. With M6 turned off, no current can flow through M5 thus resulting in no additional current being added to the summing bus.

3.3.7 Discriminator Topology Summary

The previously described subcircuits including an input differentiator, two gain stages with continuous dc feedback, threshold adjustment circuit and current switch comprise the elements necessary to implement the multiplicity discriminator required by the MVD. A complete diagram for one channel of multiplicity discriminator may be seen in Figure 3-32. As the ramping output of the preamplifier (60 ns risetime) is applied to the input of the discriminator, the differentiated signal results in a pulse similar to the one previously discussed in Figure 3-1. After propagating through a

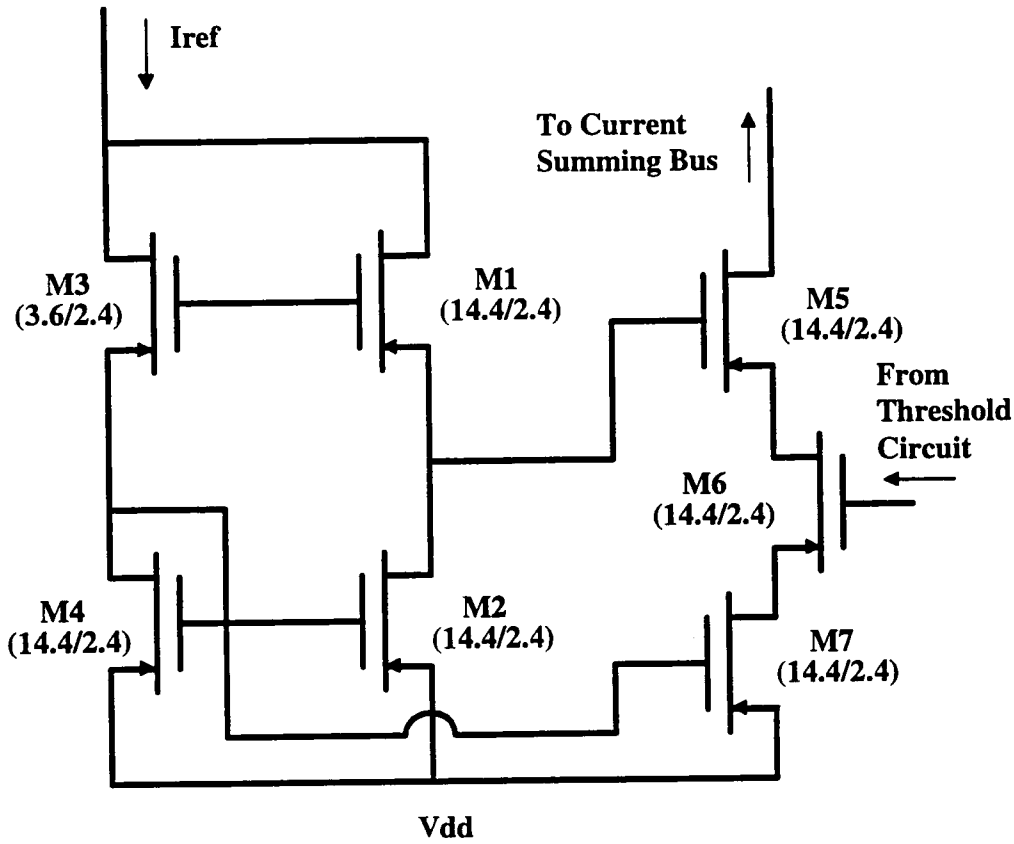


Figure 3-31. Current switch topology.

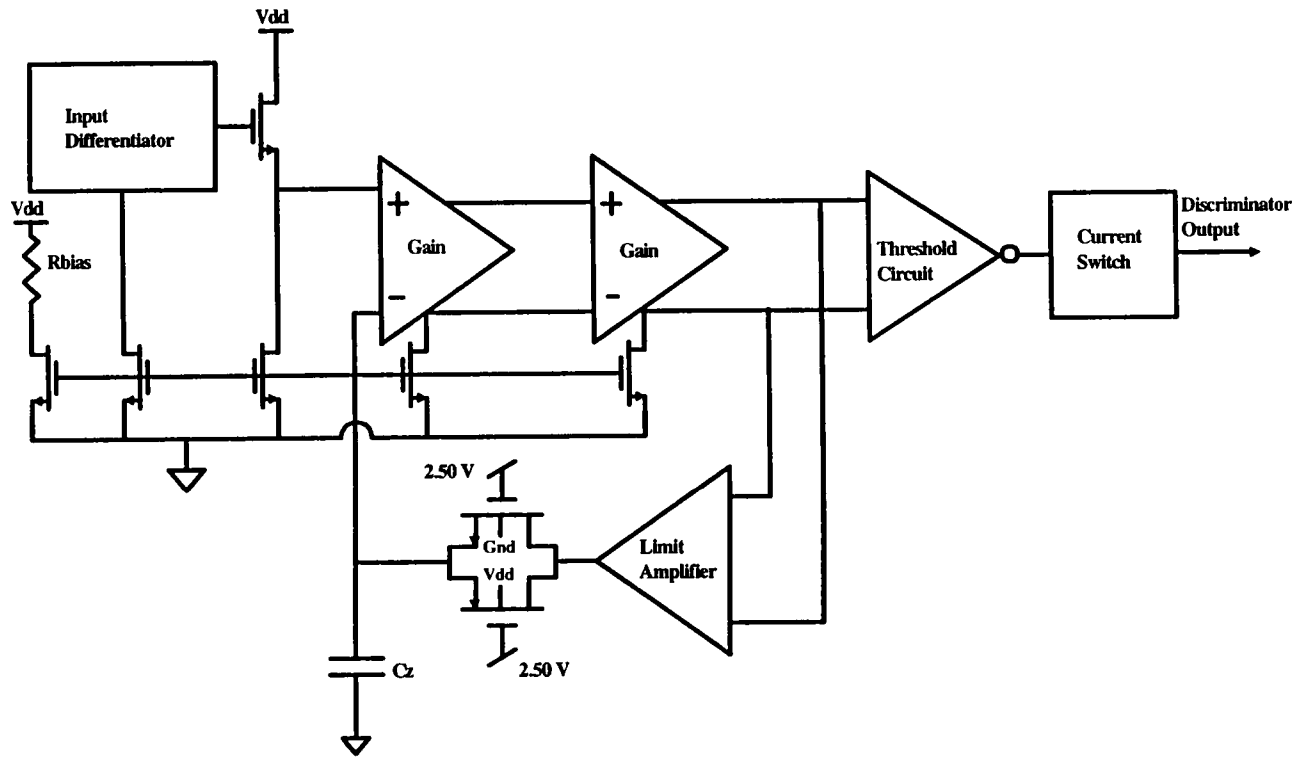


Figure 3-32. Complete diagram for 1 channel of multiplicity discriminator.

level shifting source-follower required to establish an appropriate dc bias, the differentiated pulse undergoes an amplification via two stages of differential amplifiers each having a single-ended gain of roughly 5 V/V for very small input signals. Figure 3-33 is an HSPICE plot of the resulting differential signal at the output of each stage of amplification. The gain stages are surrounded by continuous dc feedback which enables nonideal offset voltages created by mismatches within the differential amplifiers to be eliminated. Provided the differential signal reaches a peak-to-peak amplitude of approximately 300 mV, the output of the threshold adjustment circuit will move towards Vdd. When this output crosses the trip voltage of the following inverter, the resulting output is a logic low state at ground potential. The presence of zero volts applied to the input of the current switch circuit results in approximately 20 μA of current being placed onto the summing bus for a finite period of time. As the threshold circuit begins to turn off and moves back through the trip voltage of the inverter, the output is driven to Vdd and the current switch is disconnected from the bus. The process of firing or not firing on a given input signal of fixed amplitude is determined by the settings of the input differentiator gain voltage and the threshold adjustment voltage. Increasing the gate voltage of the p-channel gain resistor used in the input differentiator results in an increased system gain which enables triggering on smaller input signals. Similarly, an increase in the threshold adjustment voltage results in less current available to keep the threshold circuit output held low. Consequently, the discriminator requires less input to trigger.

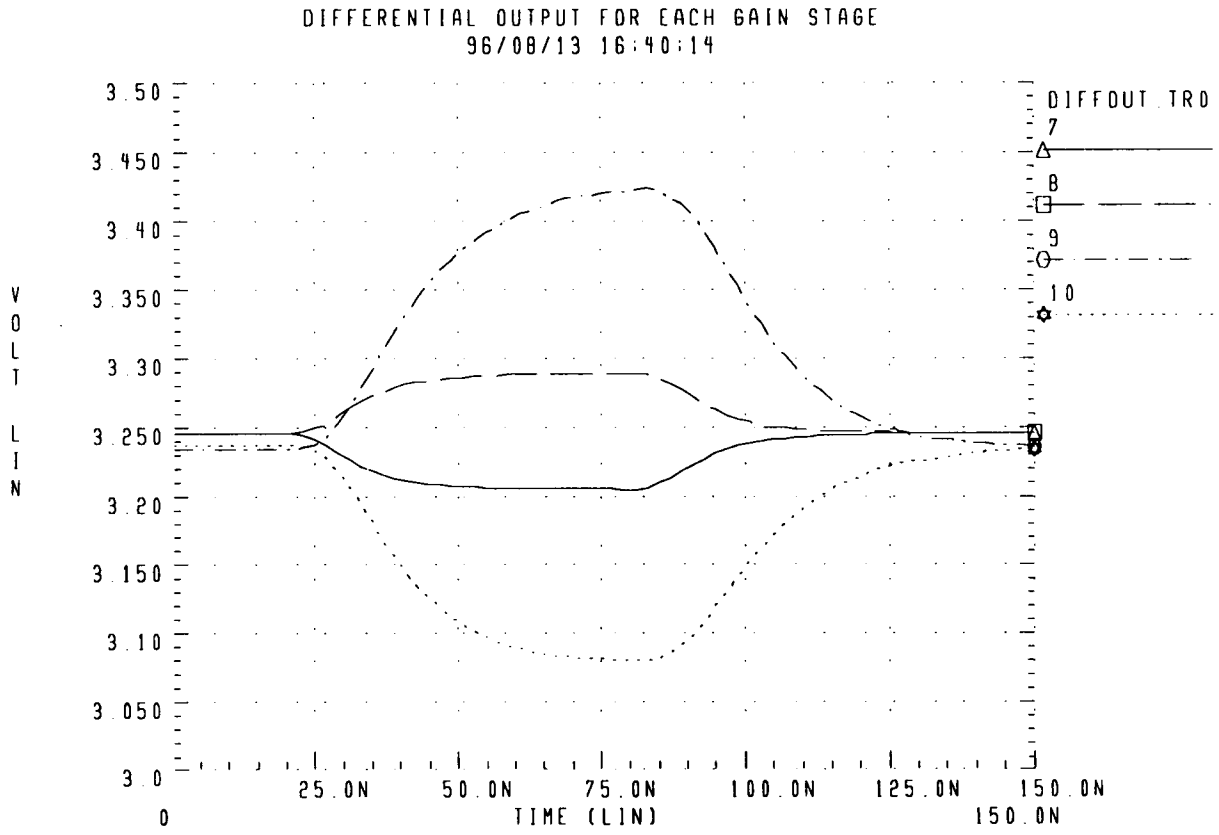


Figure 3-33. Plot of differential output for each gain stage.

3.4 Discriminator Layout

With any monolithic design, circuit layout plays a critical role in the obtainable performance of the topology. The multiplicity discriminator is no exception to this rule. To meet the stringent pitch and length requirements set forth in the design specifications requires a compact layout for the discriminator. Since each channel of discriminator must be arrayable within the 85 μ pitch, all routing including power busses and signal traces must be contained within this pitch. Routing of this nature can take nearly 20 percent of the available pitch height which places further restrictions on the remaining circuitry. An additional restriction which places further constraints on the density of the layout is the inclusion of substrate guard rings around certain devices. These guard rings become necessary due to the existence of parasitic npn and pnp transistors within CMOS circuits. If these devices become forward biased, a positive feedback loop is formed; and the circuit ceases to function properly. By placing the guard rings around transistors, the carriers which could turn on the parasitic devices are diverted to the substrate [24].

Coupling these factors in with the long channel devices required by the dc feedback loop provides many challenges in meeting the area specification. A summary of the size of each element of the multiplicity discriminator is given in Table 3.5. Summing the individual lengths given yield a total length of 527.4 μ for discriminators using serpentine devices and 558 μ for the goalpost version. Clearly both of these designs fall within the desired length of less than 600 μ. A plot of the complete multiplicity discriminator layout may be seen in Figure 3-34.

Table 3.5. Summary of Subcell Areas for the Multiplicity Discriminator

Circuit Element	Area (Pitch μ x Length μ)
Front Vertical Routing (Bias and Power)	85 x 19.8
Input Differentiator	85 x 89.4
First Gain Stage	85 x 32.4
Second Gain Stage	85 x 32.4
Limit Amplifier	85 x 50.4 (Serpentine) 85 x 62.4 (Goalpost)
Feedback Switch	85 x 49.2 (Serpentine) 85 x 67.8 (Goalpost)
Feedback Capacitor	85 x 97.2
Threshold Adjustment Circuit	85 x 51.6
End Routing	85 x 34.8
Current Switch	85 x 70.2

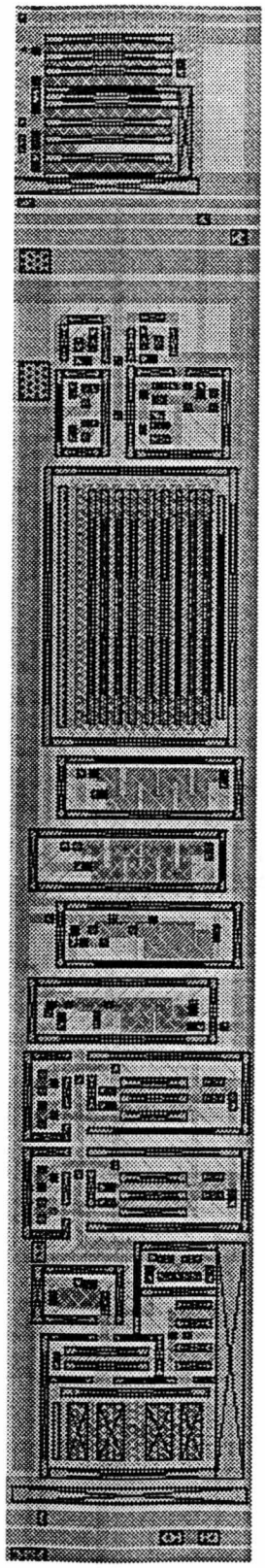


Figure 3-34. Multiplicity discriminator layout.

3.5 Summed Current Readout

In order for the output current pulse of the discriminator to be of use in the determination of event multiplicity within the MVD, a means of conversion into a representative voltage suitable for analog-to-digital conversion must be obtained. Within one MCM the sum for 256 channels of multiplicity discrimination having a nominal output of 20 μA per channel is formed. Once the summed current is converted to an appropriate voltage, conversion will be performed by a flash analog-to-digital converter (FADC) located off the MCM. Keeping the resolution demands of the FADC to a minimum requires a summing amplifier capable of a fairly high gain. For instance, to resolve 20 μV (if only unity gain existed) requires a FADC resolution of nearly 16 bits. One configuration which allows for a high gain and yields itself directly to the conversion from a current to a voltage is that of the transimpedance amplifier illustrated in Figure 3-35. By definition, a transimpedance amplifier is one which produces an output voltage which is related to an input current by the relationship

$$V_O = Z(f)(I_{IN}) \tag{3.33}$$

Several topologies, including voltage feedback and current feedback circuits, exist which will allow for the implementation of such a device. As typical with any design, certain advantages and disadvantages are associated with the implementation of a particular circuit topology. For this reason, a comparison of voltage feedback and current feedback transimpedance amplifiers as their performance relates to the discriminator summed current readout philosophy of the MVD shall now be presented.

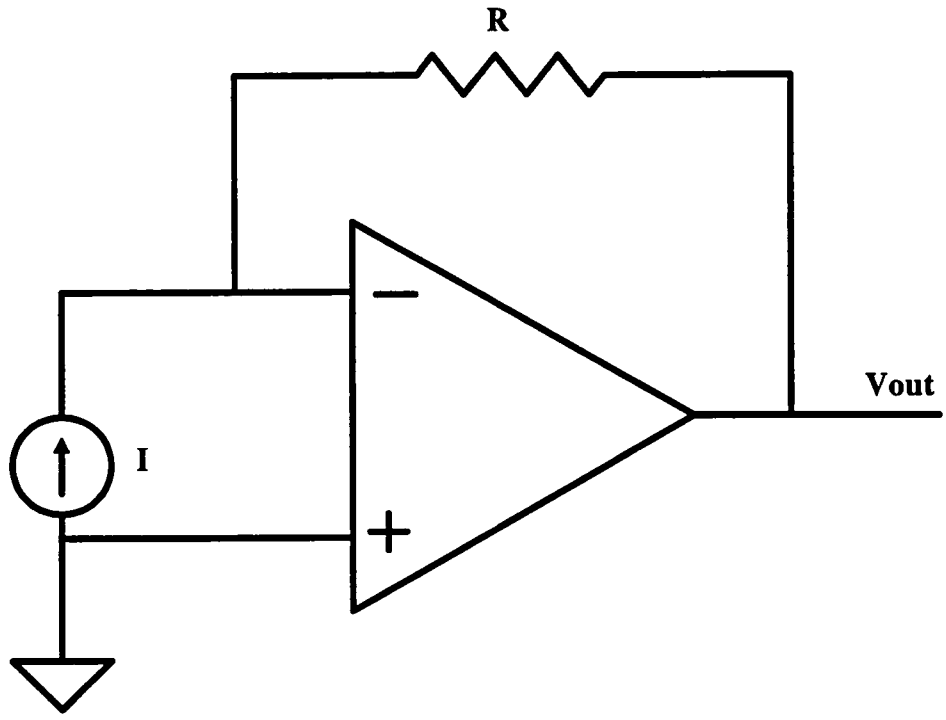


Figure 3-35. Transimpedance amplifier.

3.5.1 Voltage Feedback vs. Current Feedback

Although most conventional and commercially available operational amplifiers employ voltage feedback topologies, another topology having several advantages exists. Classically, the voltage feedback operational amplifier is represented by a voltage source whose value is determined by the potential difference between the input terminals. The ideal device shown in Figure 3-36 has infinite input impedance into either terminal and an output impedance of zero [25]. Generally voltage feedback amplifiers are compensated with a dominant pole to insure closed loop stability. As illustrated by Figure 3-37 the typical 20 dB per decade roll off from a dominant pole dictate a gain versus bandwidth tradeoff in which gain must be sacrificed to achieve a large bandwidth and vice versa. Another limiting effect of voltage feedback topologies is the slew-rate limitations brought about by the inability of internal circuitry to charge and discharge capacitive loads. This is especially true for the case of the compensation capacitor used to establish open-loop bandwidth.

Like voltage feedback operational amplifiers, current feedback amplifiers also provide a means of error signal multiplication. As seen by Figure 3-38 the current feedback amplifier includes a unity gain buffer whose noninverting and inverting input terminals approach infinity and zero respectively [26]. With the output determined once again by a voltage source, the output impedance remains at zero. While the voltage source for the voltage feedback amplifier was controlled by the potential difference of the input terminals, the current feedback circuit utilizes the error current from the inverting terminal to control the output voltage source. Unlike the

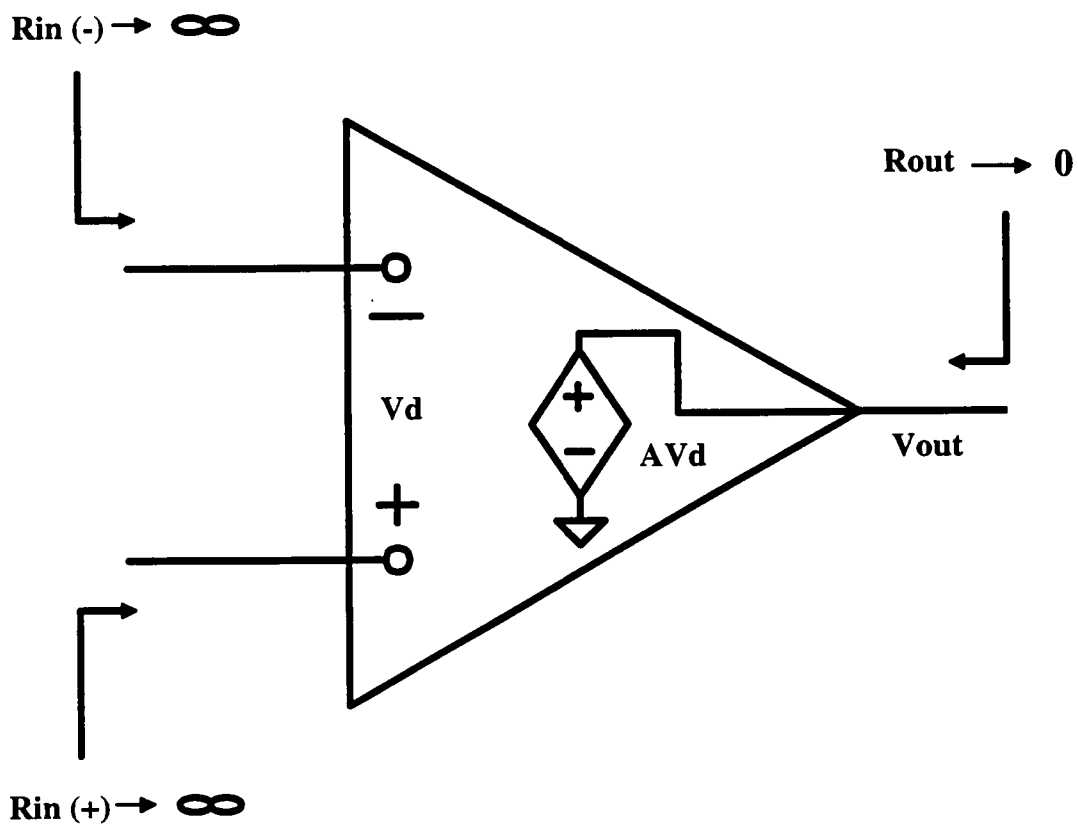


Figure 3-36. Ideal voltage feedback operational amplifier.

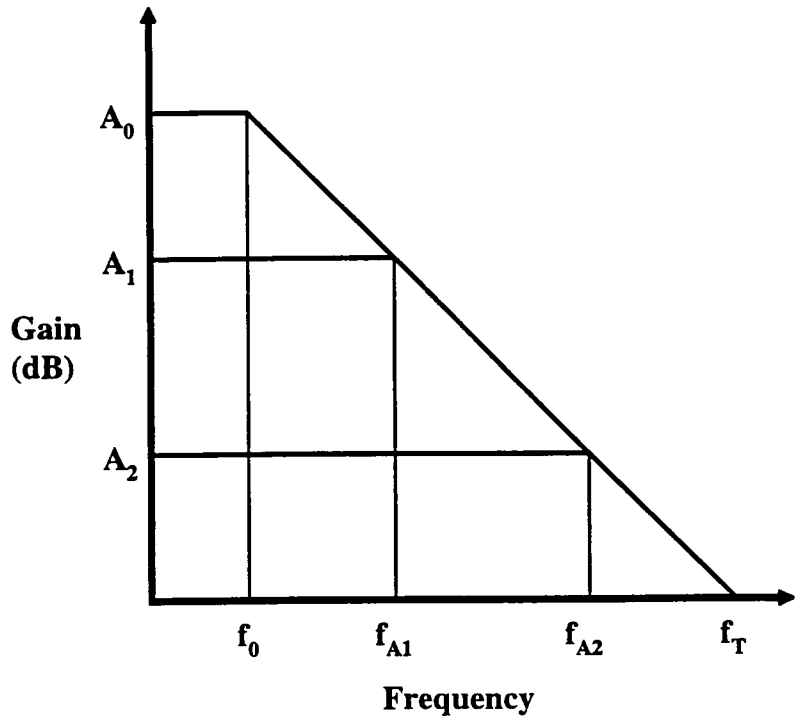


Figure 3-37. Closed loop frequency response for a voltage feedback operational amplifier illustrating the interdependence of gain and bandwidth.

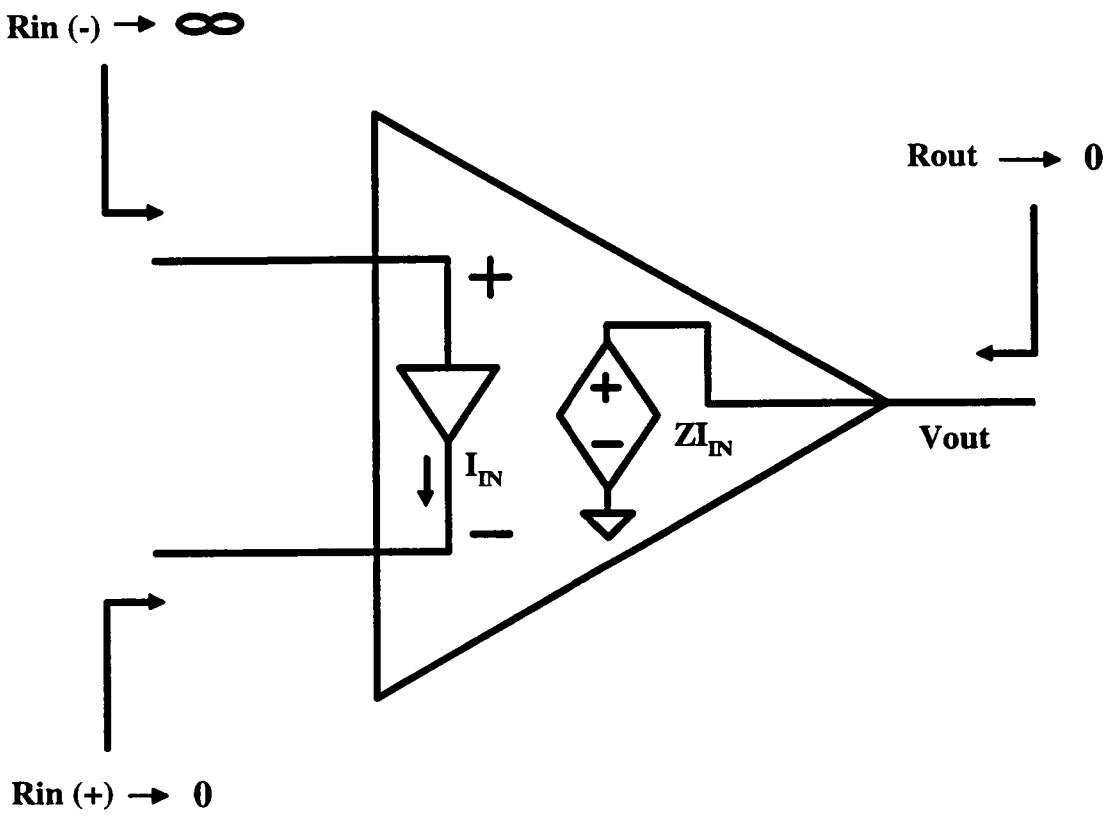


Figure 3-38. Ideal current feedback operational amplifier.

gain/bandwidth dependence seen in the voltage feedback amplifier, the current feedback device provides a bandwidth shown in Figure 3-39 which is theoretically independent of closed-loop gain. Another advantageous feature of current feedback amplifiers is the absence of slew-rate effects. Since the current available to charge internal capacitance is directly proportional to the size of the input step, slew-rate limitations never occur. However, to maintain the maximally flat closed-loop response, current feedback amplifiers are often internally compensated for a specific value feedback resistance. Deviations from the user's specified value can result in serious performance degradation. This result affects the manner in which a current feedback can be successfully compensated. For example, to compensate for added input capacitance, voltage feedback circuits promote a simple picofared valued capacitor in parallel with the feedback resistor. However, at high frequencies the capacitor has a low impedance and would cause the current feedback amplifier to oscillate.

3.5.2 Selection of Readout Amplifier

When considering an appropriate operational amplifier for performing the current summing function for 256 channels of multiplicity discrimination, advantages and disadvantages of the selected topology must be carefully weighed against system requirements. Both voltage feedback and current feedback yield acceptable topologies provided the selected device has adequate specifications. Regardless of the selected topology, Figure 3-40 illustrates the required transimpedance configuration needed to

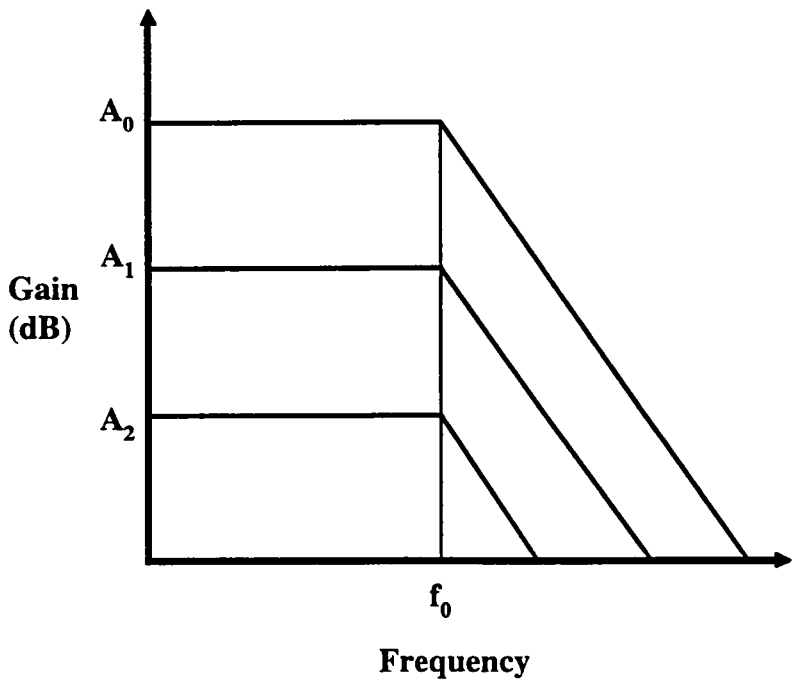


Figure 3-39. Closed loop response for an ideal current feedback operational amplifier illustrating the absence of a gain dependent bandwidth.

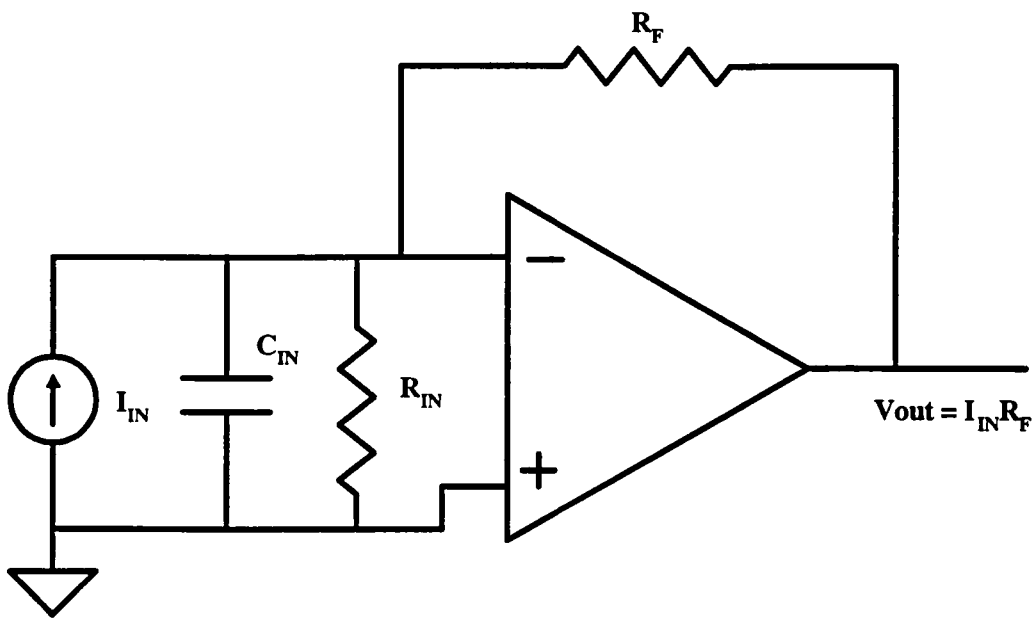


Figure 3-40. Transimpedance amplifier configuration with the appropriate input capacitance and resistance shown.

convert the discriminator output current into a voltage. It should be noted that the equivalent model for the discriminator current switch also includes capacitance and resistance in addition to the output current. Applying an ac source to the output of the discriminator and sweeping over frequency generates the impedance plot of Figure 3-41. Solving for the capacitance C and resistance R produced for a 32-channel system give values of 71 pF (2.2 pF/channel) and 1560 GΩ respectively. For the final 256-channel version the capacitance increases to over 560 pF while the equivalent resistance is roughly 200 GΩ. The extremely high value of input capacitance present will most likely require external compensation to achieve adequate stability.

Due to the need for input capacitance compensation, the use of a conventional voltage feedback topology seems the natural choice. The selected operational amplifier must have several characteristics including a bandwidth greater than 50 MHz, dynamic range greater than 3 V and very low power operation. Of the many circuits capable of meeting the given specifications two were selected for detailed evaluation. The two devices chosen were the Comlinear CLC426 and CLC440 wideband voltage feedback operational amplifiers. Both devices provide low-noise operation from a single 5 V to 12 V or duel ±2.5 to ±5 V supplies. Since the CMOS circuits comprising the MVD FEE operate from a 5 V source, single supply operation is very attractive. However, due to threshold voltage shifts caused by radiation damage effects, a small negative supply will be provided for the charge sensitive preamplifier. With the presence of the negative power supply rail, the dynamic range abilities of the opamp increase tremendously. Additionally, both the CLC426 and CLC440 have

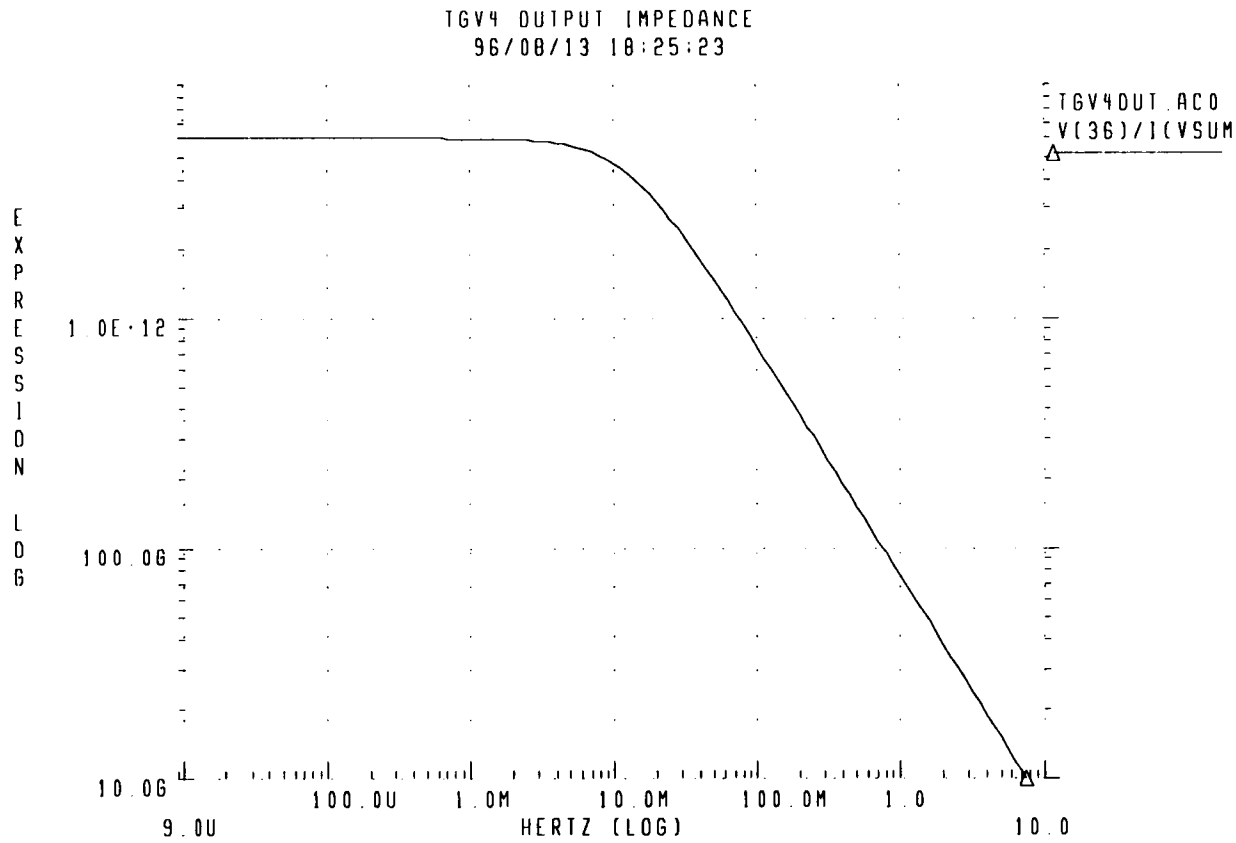


Figure 3-41. Output impedance of multiplicity discriminator.

excellent slew rates with values greater than 400 V/μs. The gain bandwidth of the CLC440 (400 MHz) is slightly higher than that of the CLC426 (230 MHz). However, the CLC426 allows for an adjustable bias current which can be used to reduce the quiescent from 11 mA to 2 mA. This feature is especially desirable when attempting to reduce the power requirements of the MVD.

For the equivalent model presented earlier, both devices were evaluated using PSPICE macromodels supplied by Comlinear. Using ±5 V power supplies (as will was utilized for the MVD beam test) .with a 2 KΩ feedback resistor, 10 pF external compensation capacitor and 10 pF feedback capacitor for input compensation excellent results were obtained for both devices. Figures 3-42 and 3-43 illustrate the inverting voltage output of the transimpedance amplifier for a single discriminator current and 32 firing channels respectively. Although the signal does not return to baseline within 105 ns, repeated simulations indicate that the output is accurate if sampled every 105 ns from some time delayed starting position. Being pin-by-pin compatible, the CLC426 and CLC440 offer much design flexibility. Due to the adjustable bias current, the CLC426 appears to be the preferred device, however if additional bandwidth is needed the CLC440 is available.

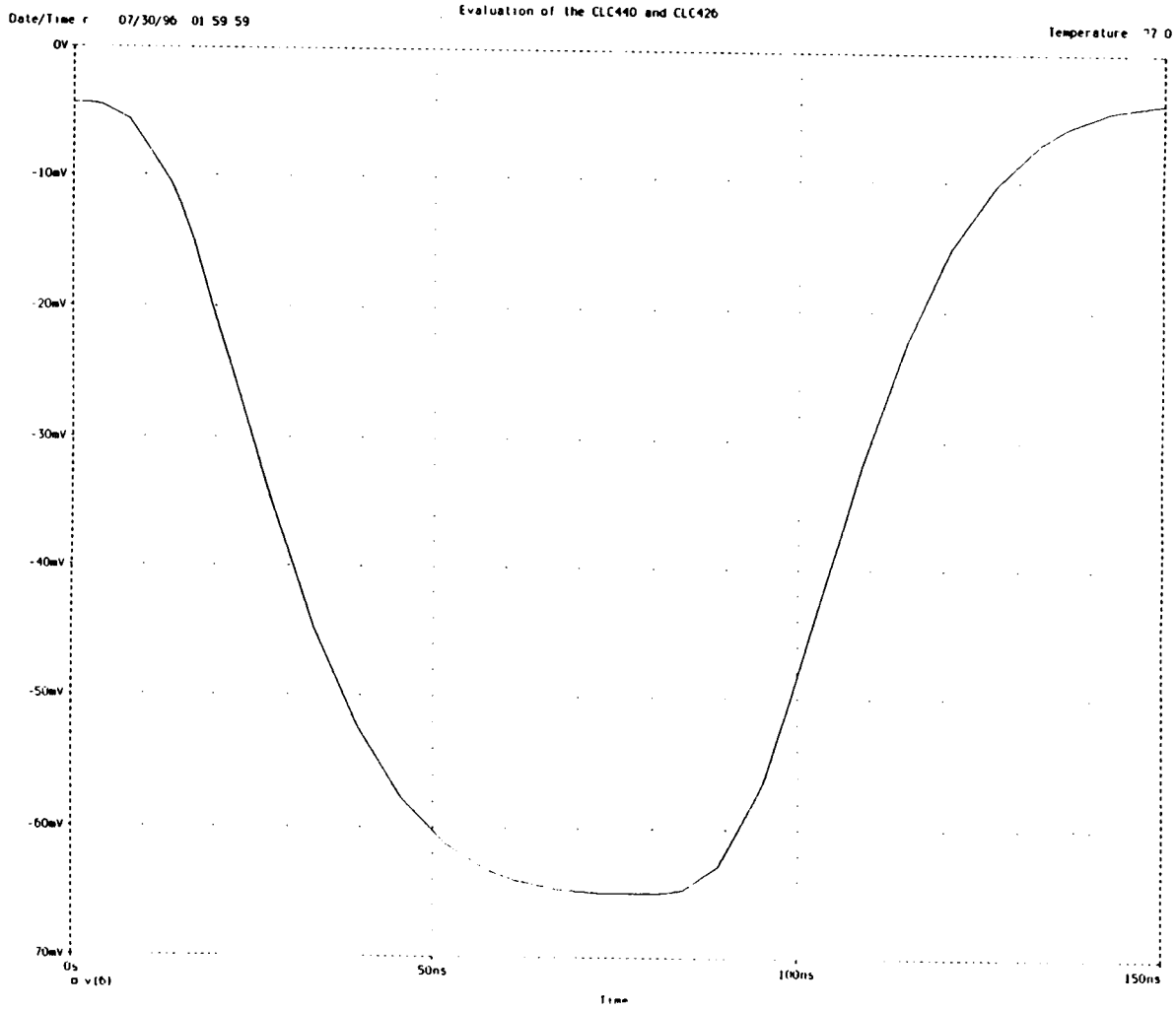


Figure 3-42. Output response of CLC426 for minimum input (1 channel firing).

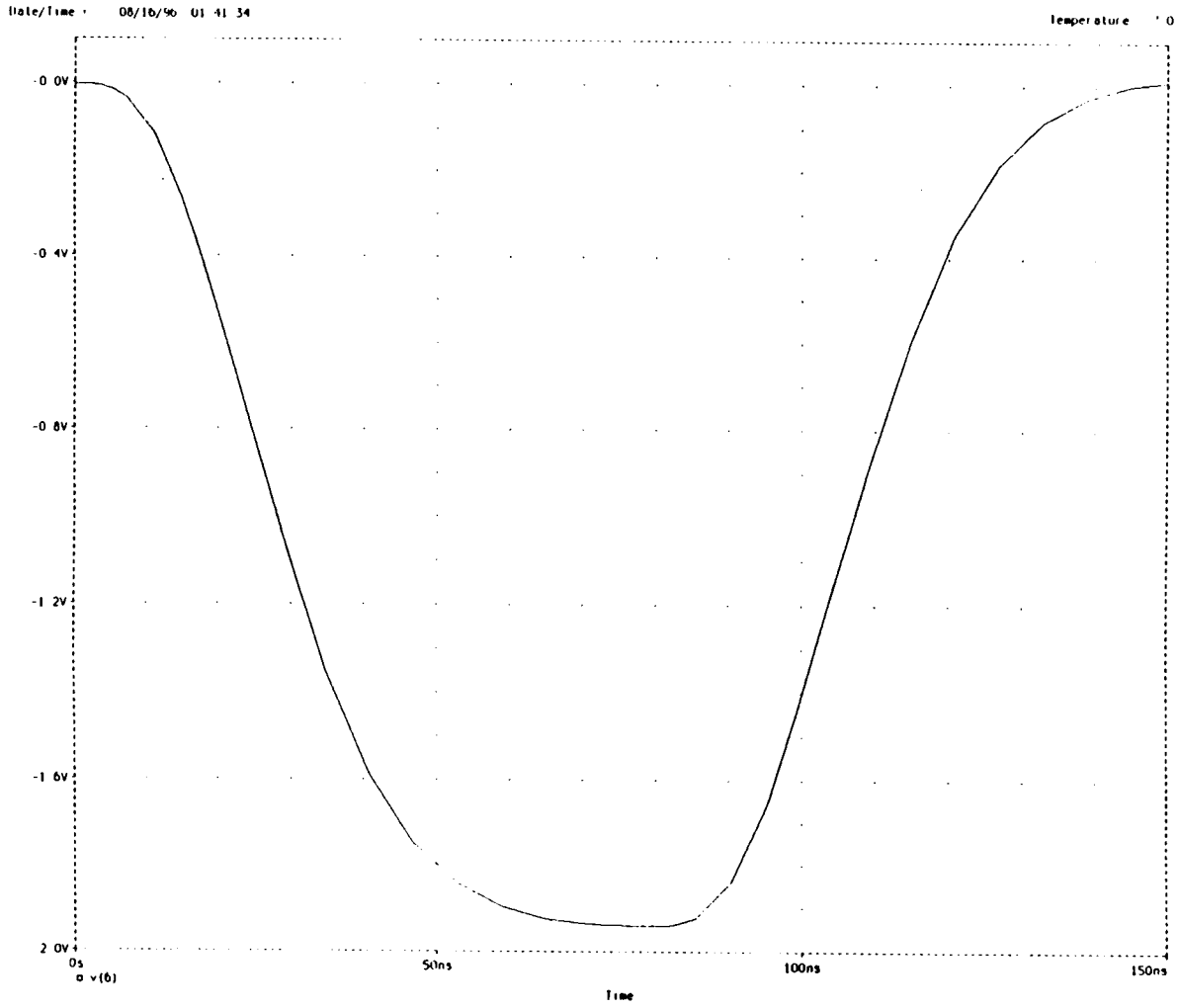


Figure 3-43. Output response of CLC426 for maximum input (32 channels firing).

Chapter 4

Experimental Results

As established in Chapter III, successful design of a multiplicity discriminator suitable for use in the MVD required a topology capable of meeting several stringent requirements. These requirements were presented in Table 3.1 to be relatively low power consumption, small area, high speed, excellent common threshold matching, large input dynamic range, external adjustability and radiation resistance. Implemented circuit area including all necessary interconnect has been shown (Section 3.4) to be 85 μ x 527.4 μ which is within the acceptable area constraints. The ability of the multiplicity discriminator to fulfill the remaining specifications will now be discussed based on the results of fabricated integrated circuits.

4.1 Circuit Characterization

Device characterization for the multiplicity discriminator was carried out based on the measured results of three different integrated circuits. All devices were fabricated with a die size of 2 mm x 2 mm in a 1.2 μ nwell CMOS process furnished by Orbit Semiconductor. The first circuit to be evaluated was the DSCRM2 chip. DSCRM2 contains a 16-channel version of the multiplicity discriminator without the output current switch. Since the current switch is not present, an additional inverter

was added to the output such that a triggered discriminator would produce a 0 to 5 V pulse. Additionally, the long channel devices set forth in the design contain a serpentine geometry for the DSCRM2 chip. Due to the 16-channel array having common bias currents and voltages, DSCRM2 offers an excellent means of evaluating common threshold matching as well as several other circuit characteristics. Based on the results of DSCRM2 testing a second prototype chip was fabricated. DSCRM_TST consists of 4 channels of discriminator with independent bias current and voltages for each channel. Two of the channels present on DSCRM_TST were identical to those of DSCRM2 while the remaining two channels utilized a slightly larger hold capacitor and a goalpost geometry for the long channel devices. Like DSCRM2, the discriminator output was in the form of a 0 to 5 V pulse. Although threshold matching information is not possible from this chip due to the independent nature of the devices, other performance characteristics such as power consumption, speed and dynamic range can be evaluated. The final chip fabricated containing the multiplicity discriminator was the TGV4 chip. TGV4 was constructed for use in the MVD preliminary beam test. The chip contained 8 channels of charge sensitive preamplification and 8 channels of multiplicity discrimination while providing critical information needed to evaluate the system performance of the MVD FEE. Since the TGV4 was a prototype version of the eventual 32-channel preamplifier/discriminator chip, the circuit contained every needed feature of the final chip including a current mode output for the discriminator. Although the chip contained multiple channels with common bias voltages, the inability to acquire a silicon-strip detector and

appropriate radiation source at ORNL rendered the chip nonusable for measuring threshold matching. However, the inclusion of the current output discriminator allows for a means of evaluating the summing amplifier described previously that is not possible with the other fabricated circuits. Additionally, TGV4 provides the ability to evaluate the preamplifier-discriminator behavior when placed on the same substrate.

4.1.1 Evaluation of DSCRM2

As briefly alluded to previously, DSCRM2 consists of 16 channels of multiplicity discrimination (voltage output) with common Vthresh, Vgain, bias and Vmid for all channels as shown in Figure 4-1. Of the six fabricated DSCRM2 die, five were fully functional while one exhibited 8 dead channels. Although the 8 remaining channels on the bad die appeared to function properly, only the 5 fully functional die will be considered in the characterization of the circuit. To evaluate the good die, a printed circuit board utilizing a separate ground plane was constructed.

Under bias conditions equal to those previously simulated with Ibias $\approx$ 20 μA (Rbias = 200 K), Vmid = 2.5 V, Vthresh = 0 to 1.6 V, Vgain = 0 to 3 V the circuit exhibited an unpredicted oscillation. The observed instability was independent of discriminator channel, input signal amplitude, threshold setting (Vthresh) and input differentiator gain established by the Vgain setting. However, the instability was seen to be sensitive to changes in the Vmid voltage as well as the bias current. By raising the Vmid from 2.5 V to roughly 4 V, the circuit stability improved drastically. Additional stability was gained by decreasing the bias current from nearly 20 μA to

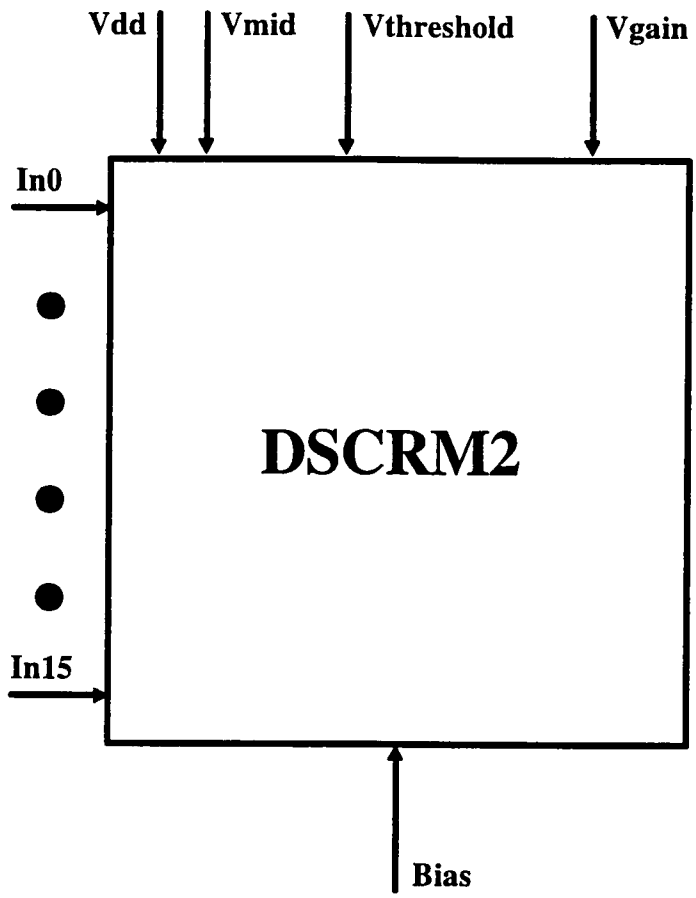


Figure 4-1. DSCRM2 chip diagram illustrating the common connections of the circuit.

just under 10 μA (Rbias = 400 K). Repeated HSPICE simulations utilizing BSIM and Level 3 models failed to predict or duplicate this undesirable result. Since the Vmid voltage was used to establish bias for the common-gate configuration of the input differentiator and control the gate voltage of the transmission gate used within the dc feedback loop, an exact determination of the problem could not be made. However, because the increased Vmid only slightly alters the dc operating point of the input differentiator and affects its performance very little, the source of the instability was believed to be within the dc feedback loop. Increasing the gate voltage on the transmission gate devices (by increasing Vmid) further increases the gate-to-source voltage of the n-channel thus placing it further into ohmic operation while making the Vgs of the p-channel more positive and further turning it off. As in the case of the input differentiator increasing the Vmid voltage appears to not make any major changes in the operating conditions of the circuit.

With the Vmid increased to 4 V, the circuit functioned properly with no oscillations or instabilities. Using the LeCroy 9210 pulse generator to generate a 60 ns risetime pulse the discriminator exhibited the ability to fire on input signals ranging from 20 mV to greater than 400 mV for a fixed Vgain and Vthresh. An oscilloscope plot of discriminator triggering on the minimal input signal may be seen in Figure 4-2. As the bias current is increased the gain of the discriminator increases and should result in a smaller detectable input signal. This proved to be true until the higher bias began to cause instability problems. At that point the minimal detectable input signal

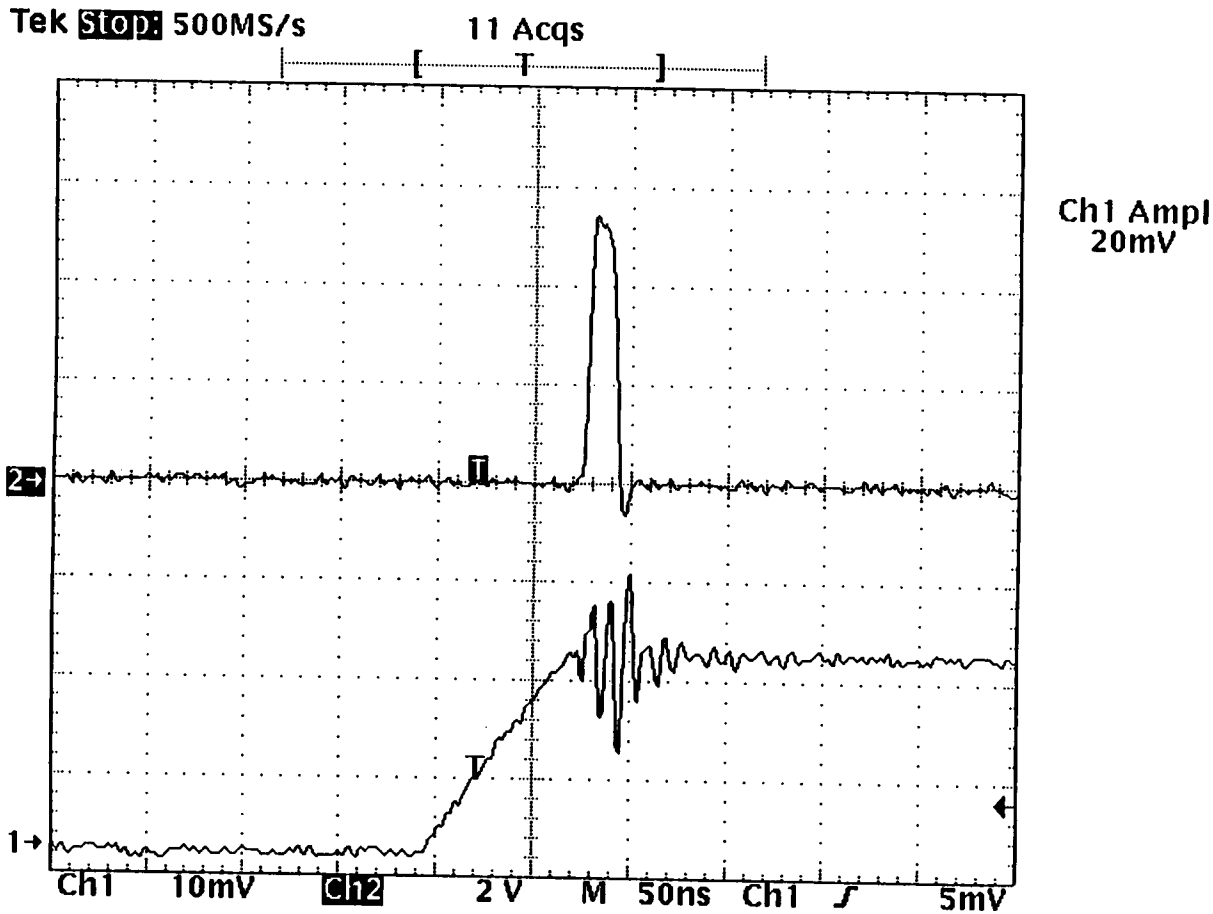


Figure 4-2. Oscilloscope plot of discriminator triggering on minimal input (20 mV).

increased due to the change required in the Vgain voltage to stabilize the circuit. This result may be seen in the graph of Figure 4-3.

Another very critical result is the measured speed of the discriminator. With the MVD system beam clock occurring every 105 ns, it is vital that the discriminator fire and return to baseline within this allotted time. Worst case timing conditions occur when a maximum input of 5 MIP (400 mV) is followed by a minimal input of 0.25 MIP (20 mV) on the subsequent beam crossing. Thus if the discriminator is to meet these requirements, the output pulse must return to baseline 105 ns from the point the preamplifier first received the input signal. Simulated results showed the discriminator had a response of roughly 108 ns under these conditions. Since the chance of this maximum hit occurring is statistically small, the speed of the discriminator was deemed acceptable. Measured results for discriminator speed as a function of bias may be seen in Table 4.1.

Table 4.1. Measured Discriminator Speed for Maximum Input

Bias Current (μA)	Speed for 400 mV Input Signal (ns)
6.5	140
7.8	135
9.7	130
12.7	120
19	110

Note as bias current is increased the speed of the discriminator also increases. This is expected since gm increases as the square root of Id (Eq. 3.13) and the frequency

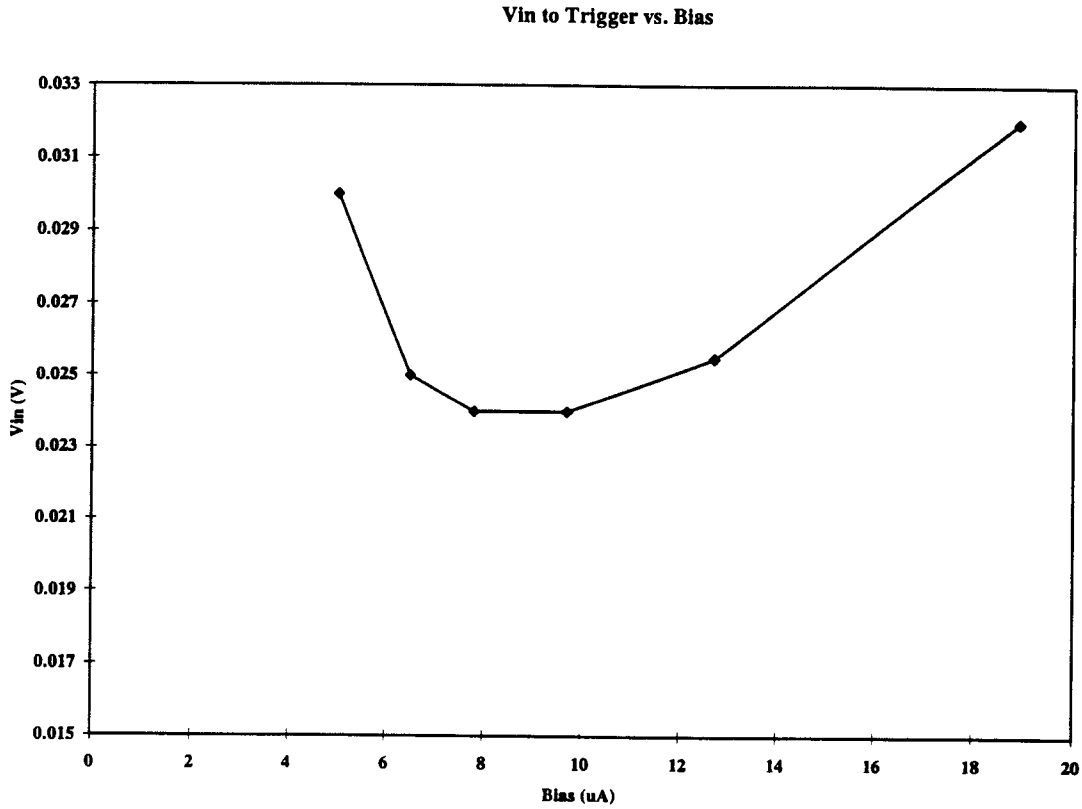


Figure 4-3. Minimal input signal capable of triggering the discriminator as a funtion of bias.

response of MOS transistors is directly proportional to the transconductance (Eq. 3.16). Both the input differentiator and the gain stages are affected by the change in bias. From the data of Table 4.1 and Figure 4-4 it is evident that for the anticipated bias of roughly 19 μA the measured response is nearly identical to that predicted by HSPICE. However, for the more stable circuit bias of 10 μA the discriminator response is approximately 20 ns too slow to meet the requirements of the MVD beam clock.

The ability to perform external adjustments on parameters such as gain and threshold allow the multiplicity discriminator to be a versatile circuit over anticipated process variations. As explained in Chapter III, increasing the Vgain voltage increases the gain resistor which increases the gain of the input differentiator circuit and allows smaller input signals to trigger the discriminator. Similarly, increasing the Vthresh voltage robs current from the differential to single ended amplifier and reduces the amount of differential signal needed by the threshold adjustment circuit to trigger the discriminator. Consequently, smaller and smaller input signals can be triggered on provided the appropriate values for Vgain and Vthresh are established. Since each of these voltages will be provided on a 32-channel chip basis, chip-to-chip matching can be precisely controlled by adequate characterization of the circuits and establishment of the necessary values. As seen by the simulated results of Table 3.3, varying the threshold voltage with the Vgain held at a constant value, allows for roughly 55 mV of variation in the input signal required to trigger the discriminator. Additionally by adjusting the Vgain setting the minimal input signal required to fire the discriminator

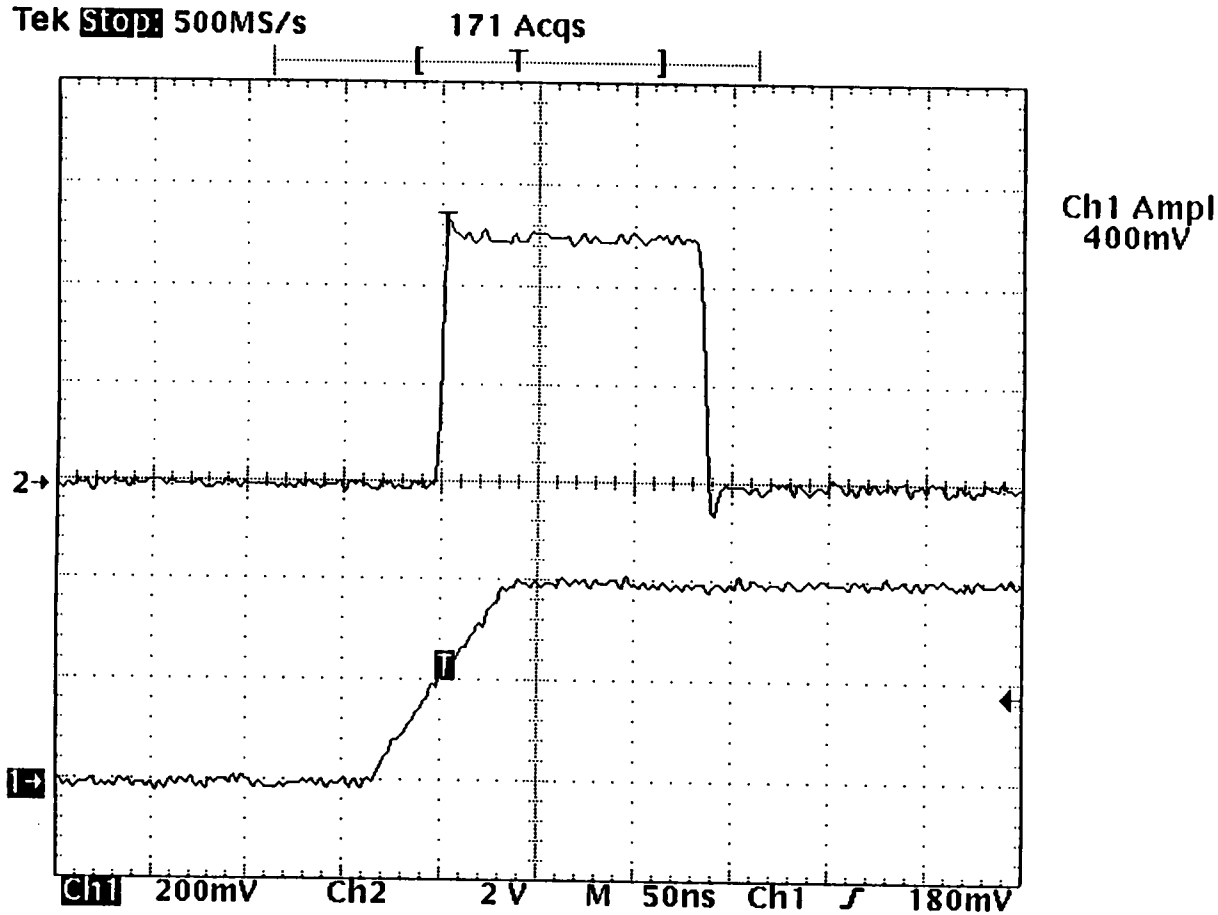


Figure 4-4. Oscilloscope plot of discriminator triggering on maximum input (400 mV).

can be altered regardless of the threshold setting. Performing an HSPICE simulation under these conditions generates the set of curves seen in Figure 4-5. From Figure 4-5 the maximum range of threshold adjustability is seen to occur for the minimal input differentiator gain setting (Vgain = 0 V). These simulated results may be verified through measured values by simply setting the needed bias voltages (Vgain and Vthresh) and recording the input signal amplitude required for firing. Figures 4-6a and 4-6b provide measured results for channel 0 of chips 3 and 6. As seen from the Figures 4-6a and 4-6b, both chips are capable of adjustment from roughly 60 mV to 20 mV. Although somewhat less than that predicted by simulations, this adjustment allows for an adequate range over which process variations can be nullified.

With one common threshold being required for 32 channels of multiplicity discriminator, channel-to-channel threshold matching across a die is extremely important to the usefulness of the circuit. In order to evaluate each 16-channel chip for threshold matching characteristics a standard test setup and procedure were utilized. Figure 4-7 illustrates the required test setup for measuring channel-to-channel threshold matching. A pulse having an amplitude of 500 mV, risetime of 60 ns and a width of several hundred ns was supplied from the LeCroy 9210 pulse generator to a 873 Kay 2 GHz attenuator. Since the LeCroy is not capable of providing signals having amplitudes less than 50 mV, the attenuator is used to produce the needed 20 mV input pulse. With a 20 mV input applied and Vgain set near maximum (to trigger on the smallest possible inputs requires maximum gain) for the chip under test,Vthresh

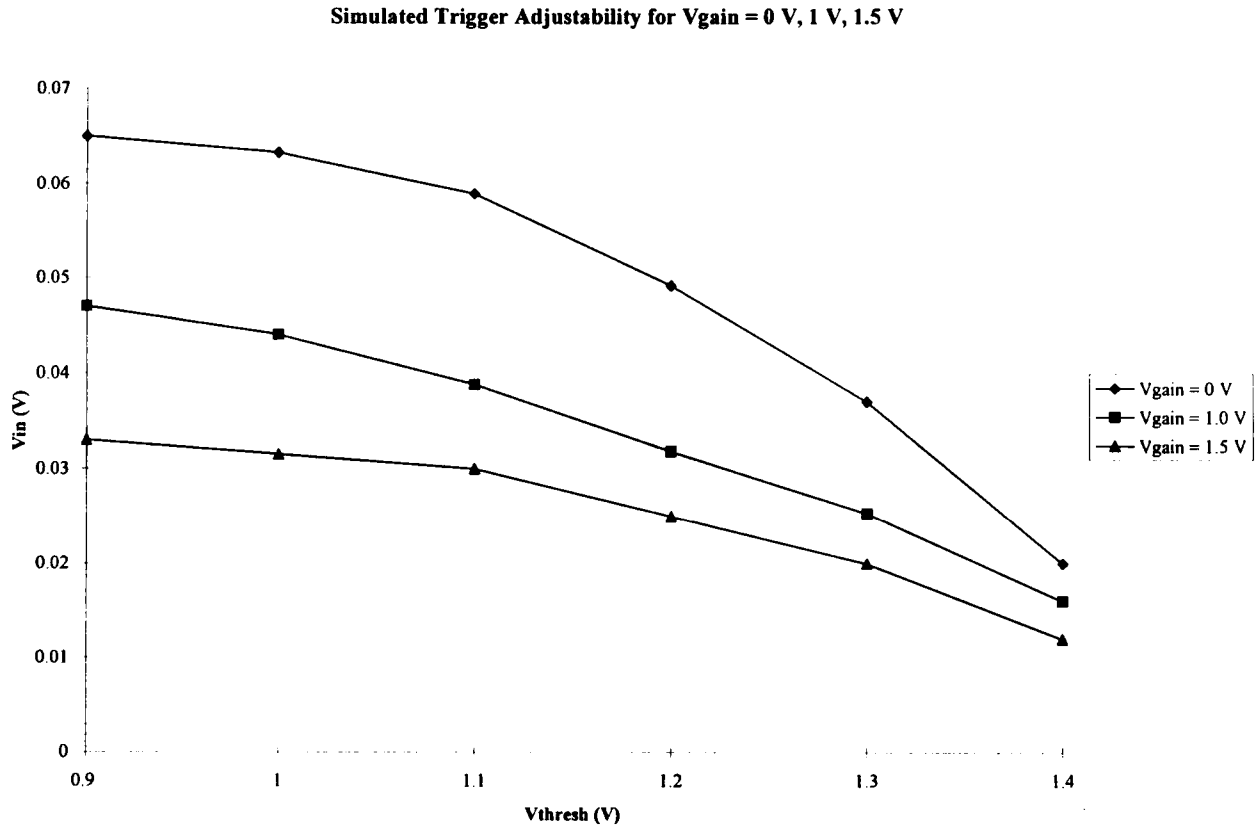
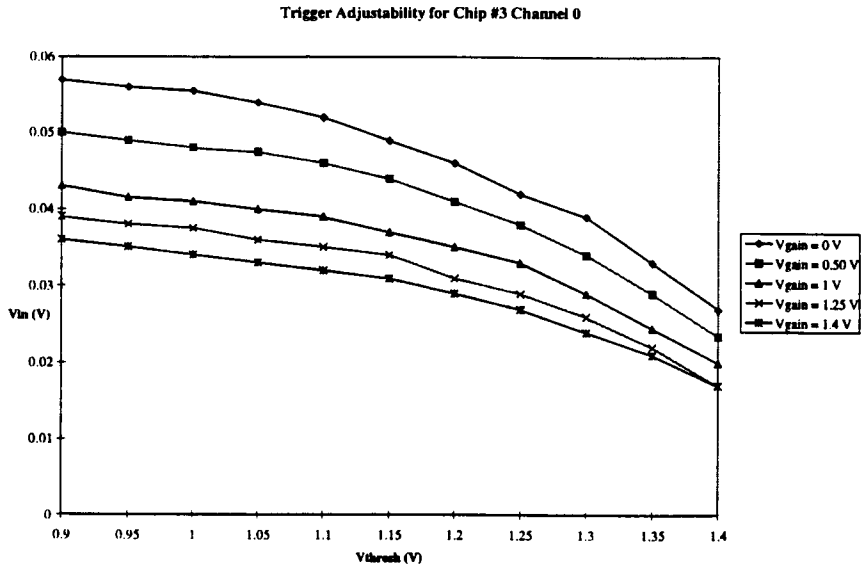
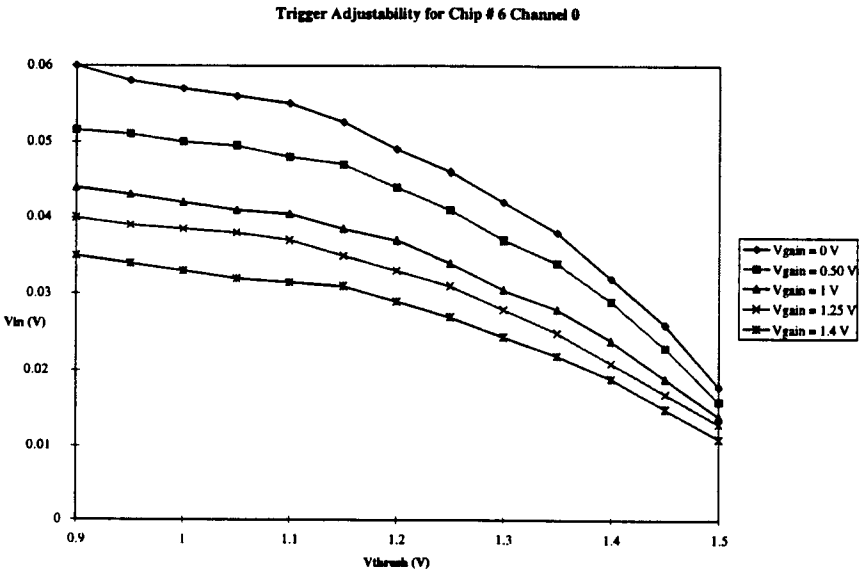


Figure 4-5. Simulated data illustrating discriminator trigger adjustability as a function of Vthresh and Vgain.



(a)



(b)

Figure 4-6. Measured data illustrating the variation in input signal as a function of Vthresh and Vgain. a) Chip # 3 channel 0, b) Chip # 6 channel 0.

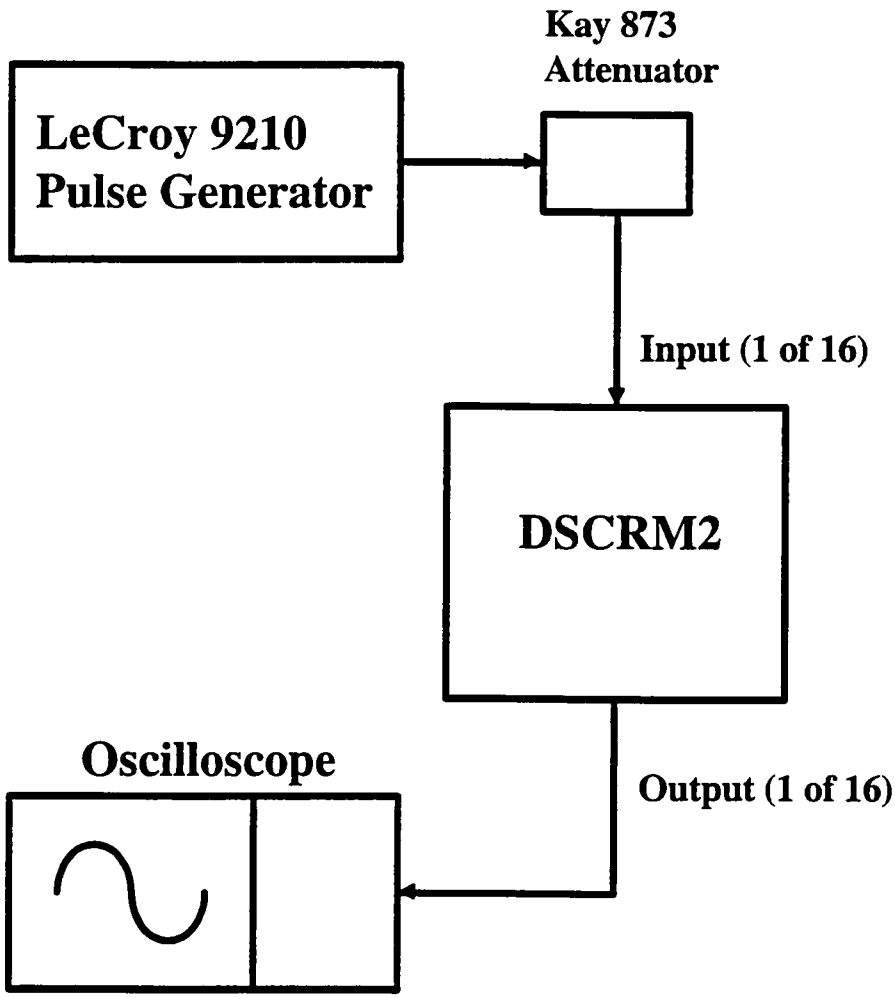


Figure 4-7. Test fixture used to measure common threshold matching.

is adjusted such that the most sensitive channel (highest gain channel) does not fire. As the amplitude of the applied input is increased, each channel begins to fire. By observing the discriminator output on a Tektronix oscilloscope, a particular channel is judged to be triggered when the output is fired roughly 50 percent of the time. Due to the crude nature of the measurement, a 1 to 2 mV error can be expected. For every evaluated chip there exists a spread of input amplitudes required to trigger the individual channels of the discriminator. Subtracting the maximum input (low gain channel) from the minimal input (high gain channel) provides a measure of common threshold matching. An ideal threshold deviation of zero would represent perfectly matched channels and allow exceptional resolution for the multiplicity measurement. Practically integrated circuit channels do exhibit mismatch that must be considered in any characterization of the circuit. A deviation of 10 mV ($\pm$ 5 mV) was established as the maximum acceptable limit for the multiplicity discriminator. Figures 4-8 through 4-12 present the measured threshold variation as a function of bias current for the five fabricated chips. Generally, it may be seen that the mismatch decreases with increasing bias current until a bias of roughly 10 μA is exceeded. At this point the threshold mismatch increases slightly. This is somewhat expected since (as previously discussed) the circuit tends to become less stable for higher bias currents than 10 μA. As illustrated by Table 4.2, at the 10 μA level chips 2, 5 and 6 exhibit variations less than $\pm$ 6 mV, while chips 1 and 3 show threshold mismatchs greater than $\pm$ 10 mV.

The measured levels of threshold variation exceed those anticipated by several millivolts. As reported by Simpson and Young [19] and described in Chapter III, the

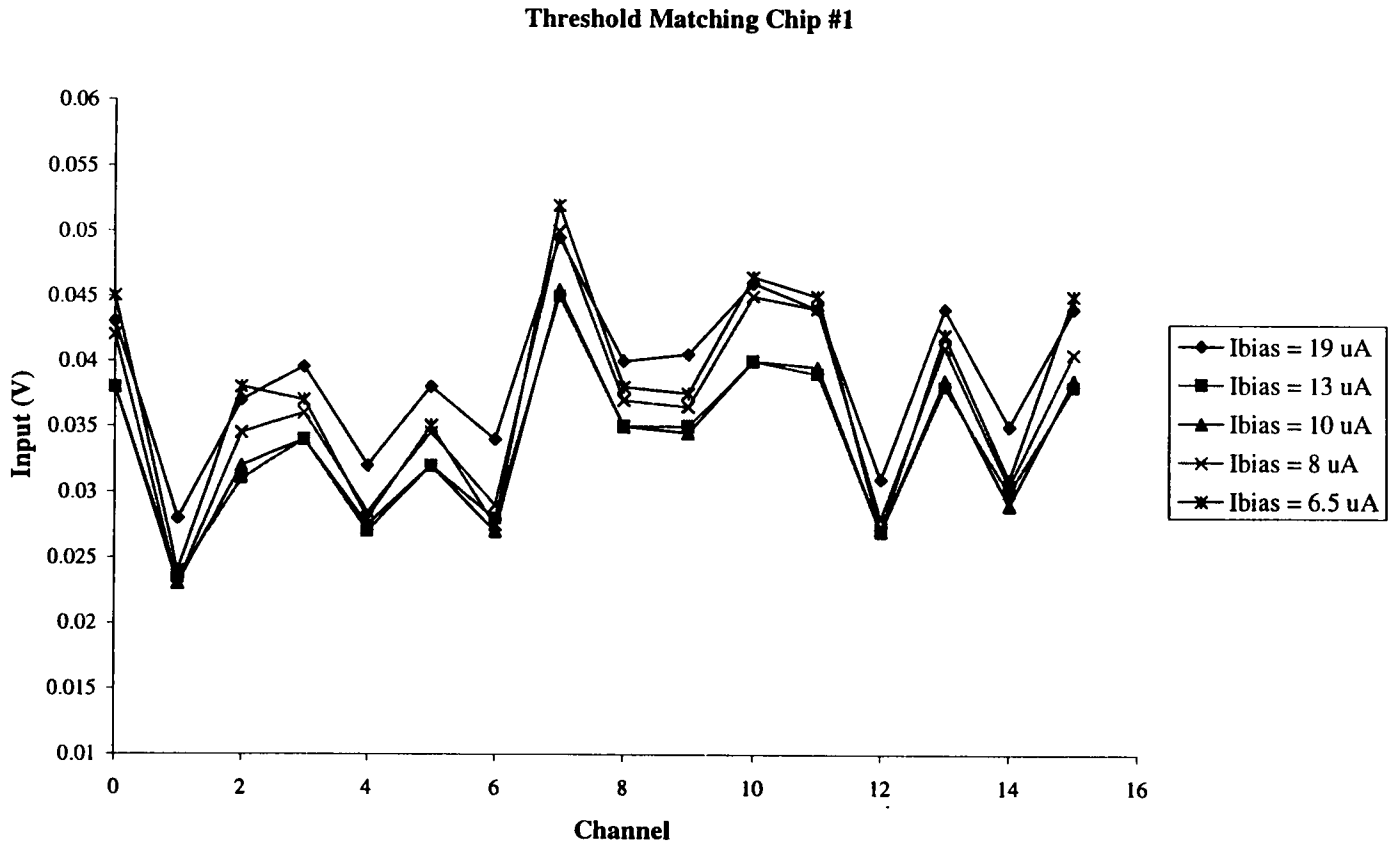


Figure 4-8. Threshold matching for chip # 1 as a function of bias.

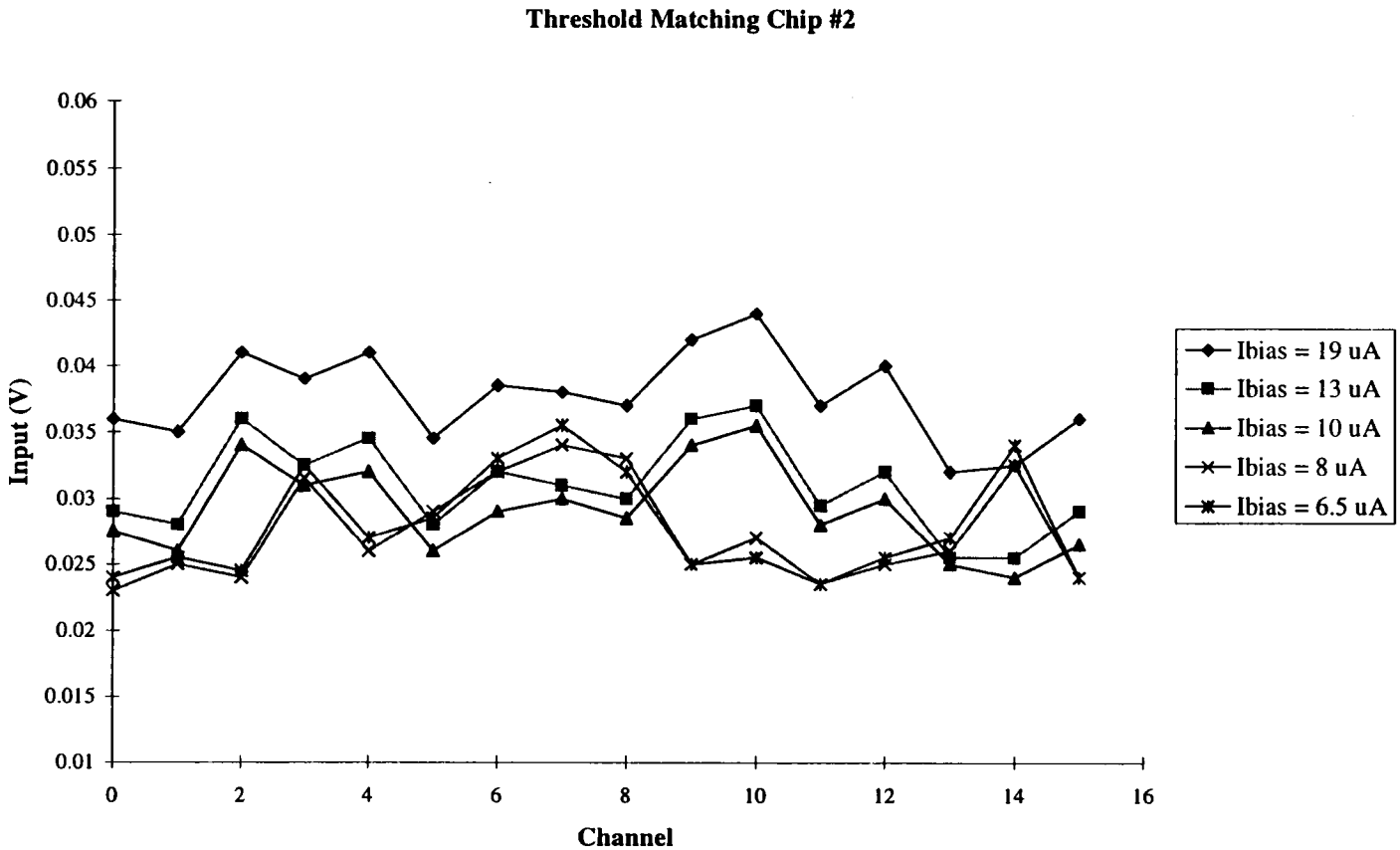


Figure 4-9. Threshold matching for chip # 2 as a function of bias.

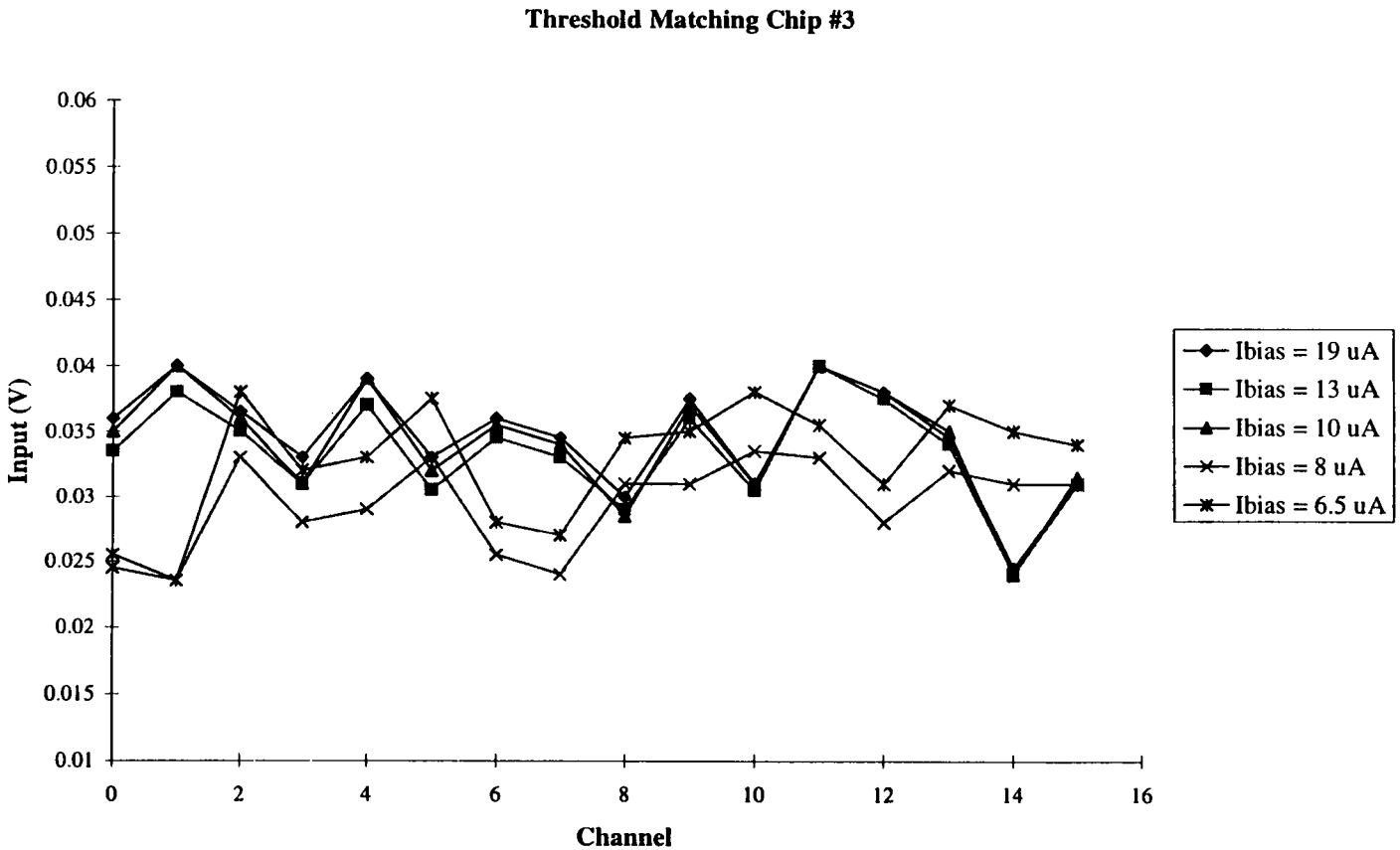


Figure 4-10. Threshold matching for chip # 3 as a function of bias.

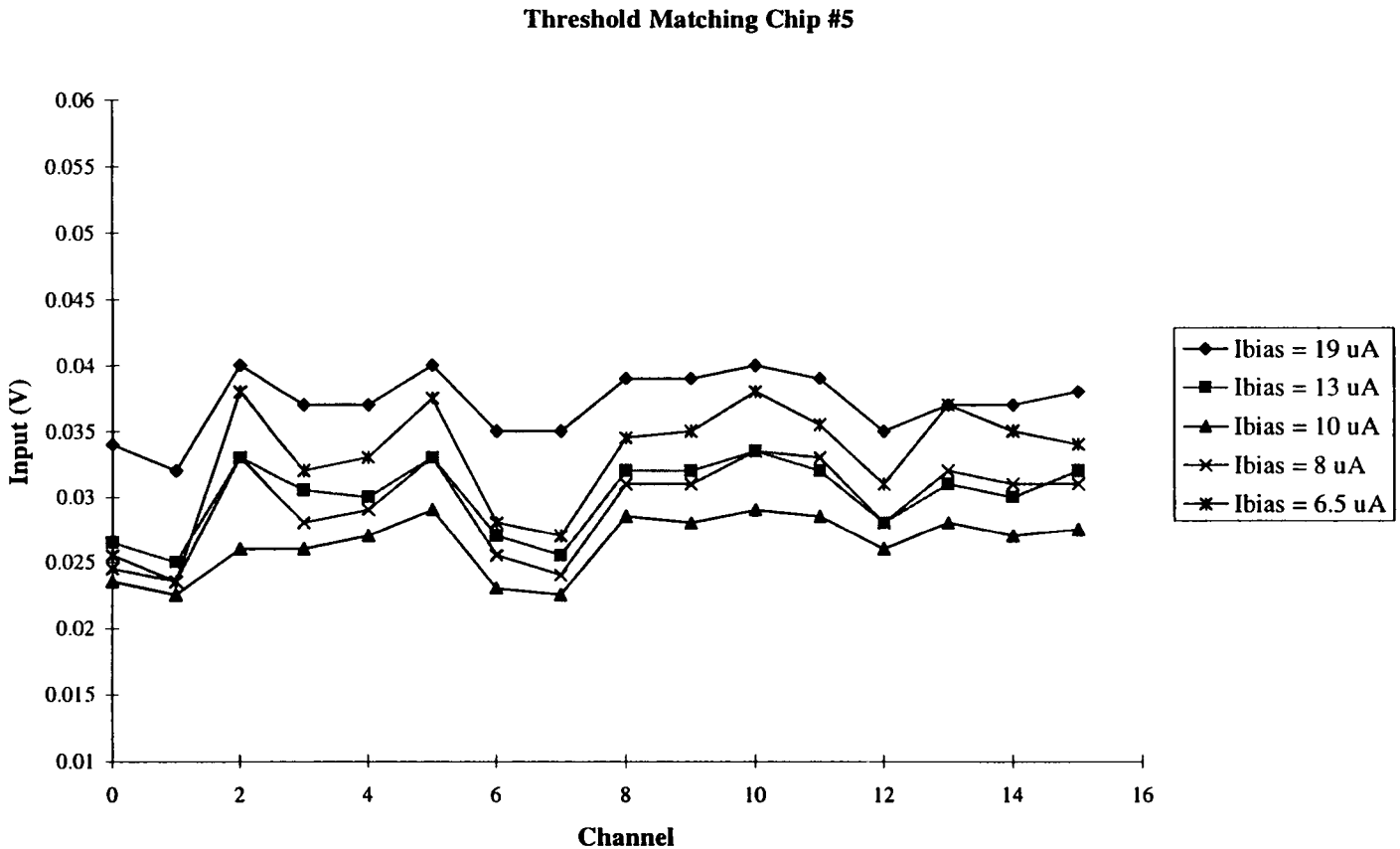


Figure 4-11. Threshold matching for chip # 5 as a function of bias.

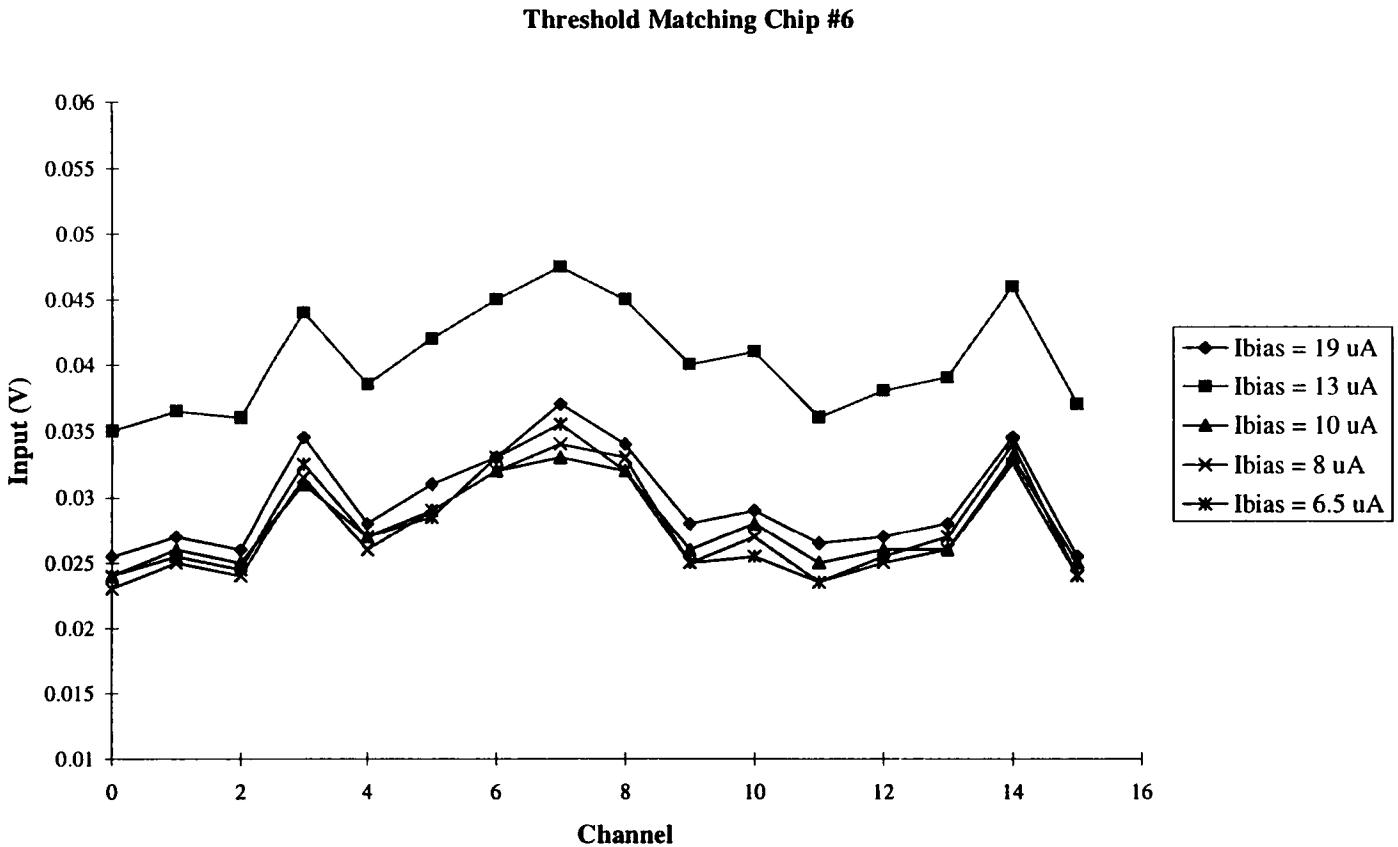


Figure 4-12. Threshold matching for chip # 6 as a function of bias.

threshold adjustment circuit is capable of threshold matching better than ± 3 mV. All of the measured chips yield mismatches greater than this with the worst case (chip 6) being nearly four times larger. With the threshold circuit known to be within ± 3 mV and the gain stages compensated by negative feedback, only the input differentiator remains as a possible source of the large threshold variations.

Table 4.2. Threshold Variation as a Function of Bias

Bias (μA)	Chip #1 (mV)	Chip #2 (mV)	Chip #3 (mV)	Chip #5 (mV)	Chip #6 (mV)
6.5	38 ± 14	33 ± 8	34 ± 10	30.25 ± 7.25	28.25 ± 5.25
8	36.5 ± 13.5	30.5 ± 6.5	33.5 ± 10	28.5 ± 5	28.5 ± 5.5
10	34.25 ± 11.25	29.75 ± 5.75	32 ± 8	25.75 ± 3.25	28.5 ± 4.5
13	34.25 ± 10.75	31.25 ± 5.75	32 ± 8	29.25 ± 4.25	41.25 ± 6.25
19	38.75 ± 10.75	38 ± 6	32 ± 8	36 ± 4	31.25 ± 5.75

Since the input differentiator is followed by two stages having a differential gain of roughly 12 V/V, a 1 mV channel-to-channel difference in the output of the differentiator could lead to a major change in the input required to trigger the threshold adjustment circuit. There are two basic mismatch errors present within the input differentiator. The first mismatch occurs due to variation in the gm of M1. For a fixed load resistance, the gain variation due to deviations in gm is simply

$$GainError = \Delta gm(Rgain) \tag{4.1}$$

However, since gm is proportional to the square root of W/L and matching to the WL product, the drawn dimensions of 28.8/1.2 should be adequate [17,27]. This points to

the second source of error being the dominant factor. The second source of error stems from mismatches in the differentiator bias from channel-to-channel. As illustrated in Figure 4-3, changes in differentiator bias current can cause vast deviations in the signal required to trigger the discriminator. To alleviate this mismatch error requires only that the area of the current sources to be increased. Thus at the cost of a modest increase in area, the multiplicity discriminator should exhibit tremendous improvement in matching.

4.1.2 Evaluation of DSCRM_TST

To investigate the instability problems of DSCRM2 a test chip containing two DSCRM2 discriminators and two new discriminators was developed. Each of these devices required individual bias and separate voltages for the gate of the input differentiator common-gate transistor and the control nodes of the transmission gate within the dc feedback loop. The new design simply replaced the long channel serpentine transistors with the goalpost geometry described in Chapter III. One of the new designs as well as one of the old discriminators has the feedback node (at the hold capacitor) brought out to a pad. Figure 4-13 further illustrates the configuration of the DSCRM_TST chip.

The ability to set Vmid1 and Vmid2 separately immediately eliminated the input differentiator as a source of the observed problem. As expected, reducing Vmid1 to 2.5V produced no instabilities in either of the four circuits regardless of bias, input or gain setting. The same could not be said for the transmission gate control

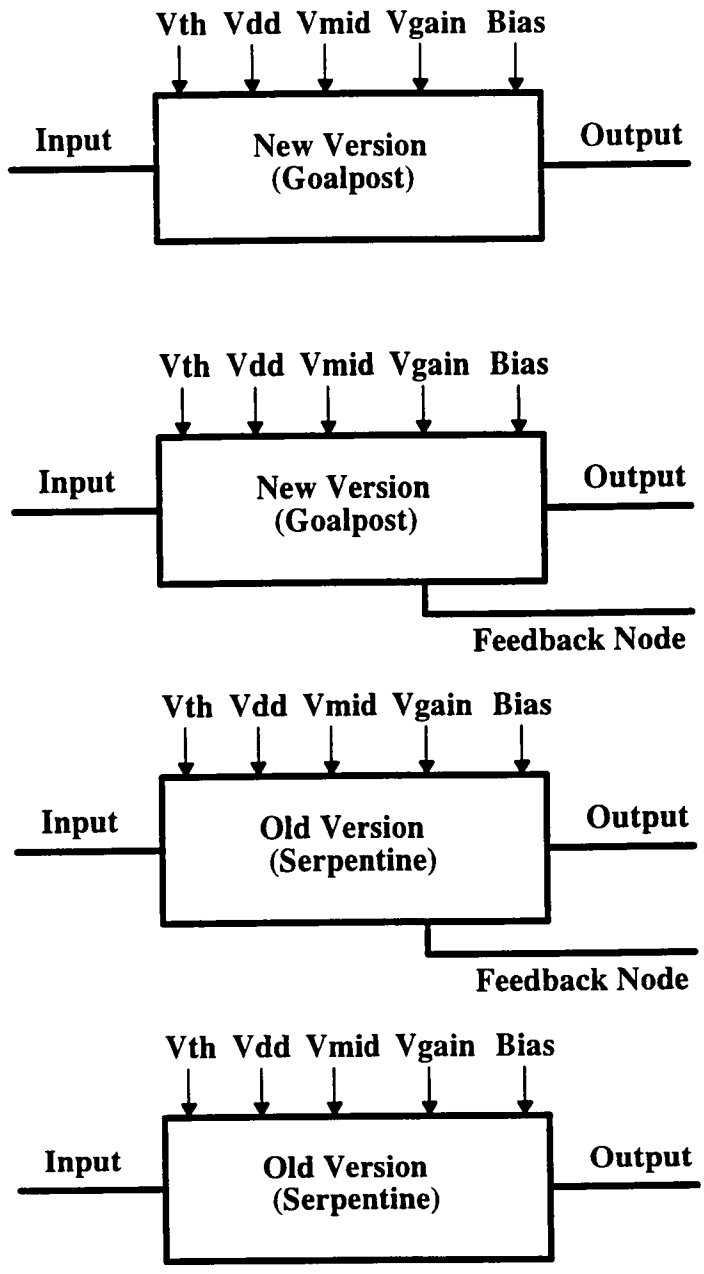


Figure 4-13. Layout of DSCRM_TST chip illustrating independent biasing and variations from one channel to the next.

nodes set by Vmid2. For Vmid2 = 2.5 V every circuit (new and old) exhibited instability problems like those seen in DSCRM2. However, both of the new discriminators as well as the old design with the feedback node brought out to a pad required a Vmid2 of only 3.5 V to stabilize the circuit compared to the 4 V needed by the old design. Decreasing the gate voltage from 4 V to 3.5 V decreases the Vgs of the n-channel device which in turn increases the effective Ron of the transmission gate (note the p-channel is still turned off). Increasing the effective R further reduces the location of the dc feedback dominant pole. However, the three circuits which exhibited the new characteristics also have a larger effective hold capacitor than does the old design. Both of the new designs have a hold capacitor which has been increased to roughly 3.5 pF compared to 2 pF in the old design. Additionally, one of the new circuits and one of the old circuits have roughly 3 pF added to the effective capacitance due to their connection to an external pad.

Obviously from these results the instability problem is definitely a consequence of the dc feedback loop and appears to improve with increasing resistance and hold capacitance. Increasing the R_ZC_Z time constant further lowers the dominant pole which was seen to be roughly 870 Hz. Other aspects of the new multiplicity discriminator compared very well with the results of DSCRM2 testing. The discriminator was capable of firing on 20 mV (0.25 MIP) signals with speeds comparable to those seen previously in Table 4.1. Additionally, power consumption for the new design was measured to be 515 μW/channel.

4.1.3 Evaluation of TGV4

The final fabricated circuit evaluated was the 8-channel preamplifier / discriminator prototype TGV4 chip designed for use in the 32-channel MVD beam test system. Integrating the preamplifier and the discriminator onto the same silicon substrate offers insight into their performance as a system compared to the stand alone characteristics. HSPICE simulations similar to the one shown in Figure 4-14 were performed on the TGV4 circuit to ensure proper functionality. As the applied input signals (from a representative model of the detector) generate preamplifier outputs of roughly 20 mV or larger, the discriminator associated with each particular channel should inject a nominal current of 20 μA onto the current summing bus. In order to view the current sum output in relation to the preamplifier output (as in Figure 4-14) the summed current was converted to a voltage value by placing a 1 KΩ resistor to ground in series with the bus. Simulation results verified the ability of the preamplifier/discriminator circuit to trigger on 0.25 MIP input signals in accordance with that seen by discriminator simulations of the DSCRM2 chip.

Generally speaking, the role of a circuit simulator is to provide an accurate low order description of the design. The ability to accomplish this task is obviously limited by the precision and completeness of the models being utilized to model both active and passive integrated components. This is especially true in the simulation of systems in which many of the higher order effects, deemed negligible for individual circuits, become dominant. As a result, actual fabricated circuits implementing a system of electronics often exhibit nonideal characteristics. Several of these undesirable

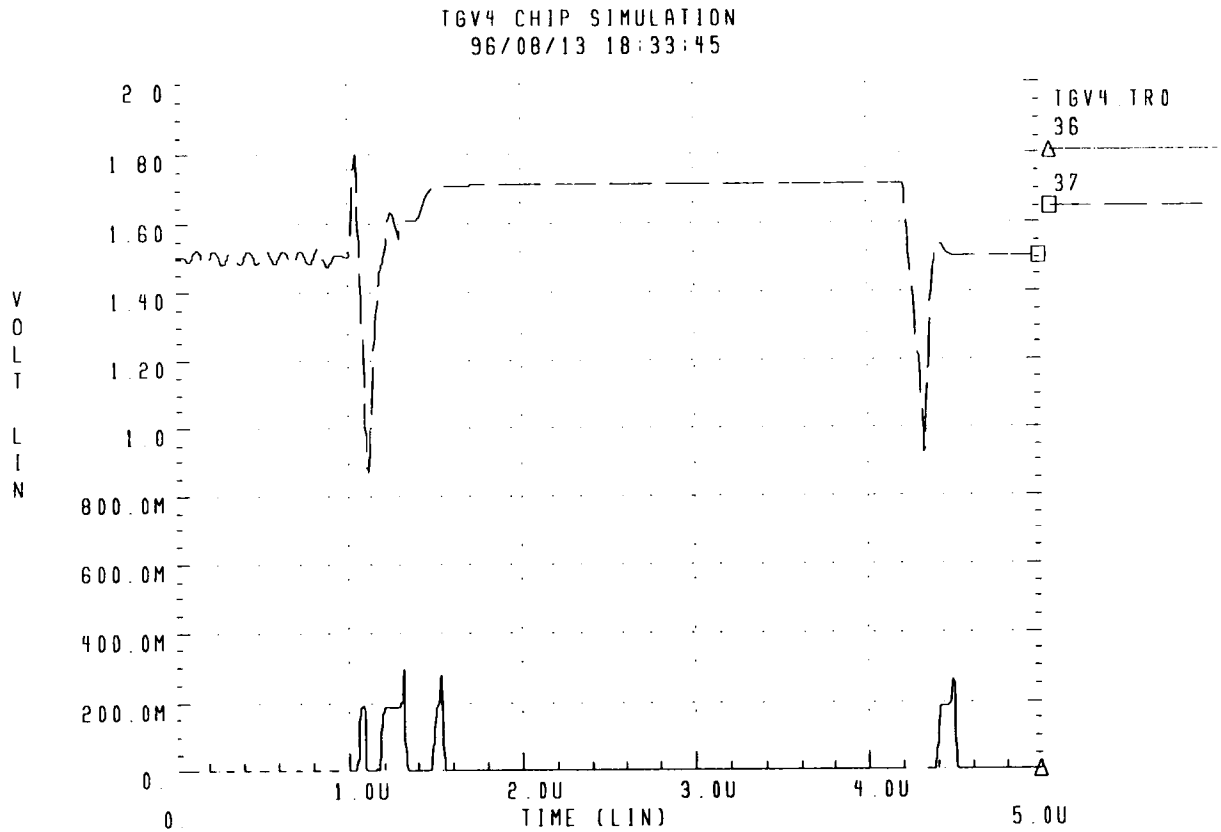
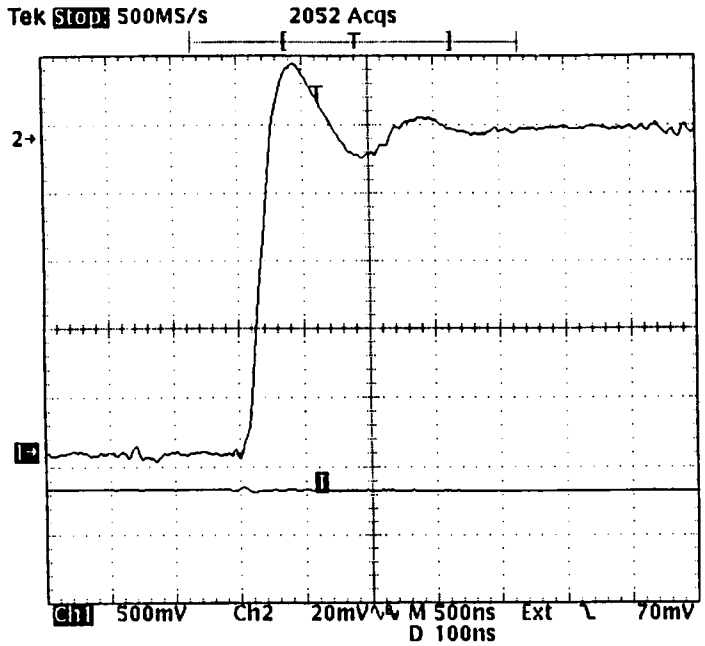


Figure 4-14. Simulation plot of TGV4 output response.

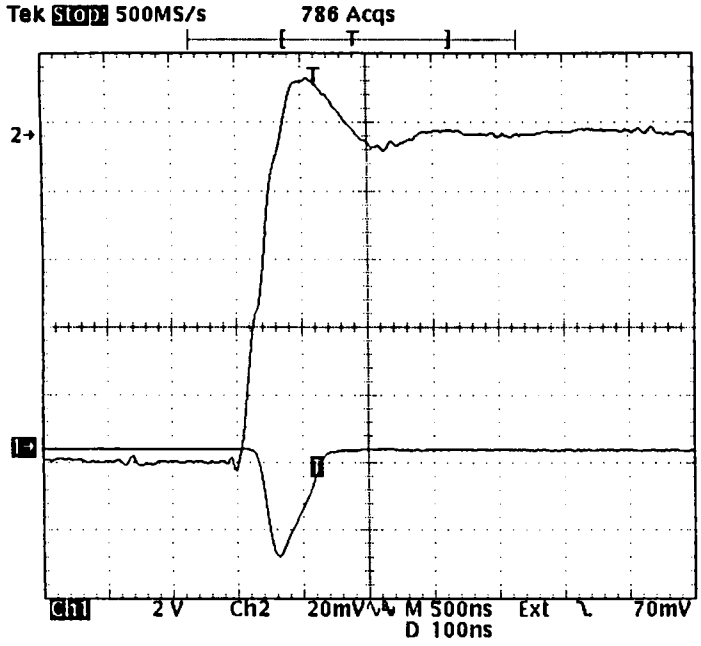
characteristics including lack of adequate adjustability and substrate coupling were discovered in the evaluation of the TGV4 chip.

The graph of Figure 4-6 illustrated the ability of the multiplicity discriminator to adjust the minimal input required for triggering from roughly 20 mV to 60 mV. This result implies that the discriminator can be adjusted such that it will not trigger on signals less than 60 mV but will always trigger (regardless of settings) for inputs greater than 60 mV. However, experimental results of the TGV4 chip yield a much different scenario. While the multiplicity discriminator is capable of firing on 20 mV inputs, the range of adjustability has been greatly reduced. Practically, this means that for the MVD beam test system which is constructed using printed circuit board and chip-on-board technologies, any spurious system noise (from switching transients etc.) could trigger the discriminator and produce a false event. Although the inability to establish a higher minimal input threshold seriously reduced the accuracy of the beam test multiplicity measurement, through extensive grounding and shielding schemes the noise level was reduced enough to overcome the lack of adjustability.

Another observed nonideal effect was the presence of coupling between the discriminator and the preamplifier. At the point the discriminator triggered, the preamplifier output signal was altered. This may be seen by the illustration of Figures 4-15a and 4-15b. Figure 4-15a represents a normal preamplifier output response without the discriminator firing. From the plot the signal may be seen to have a setting time of roughly 80 ns. However, as seen in Figure 4-15b the preamplifier output becomes somewhat distorted by the presence of a triggered discriminator. Instead of



(a)



(b)

Figure 4-15. Variation in preamplifier output response due to substrate coupling. a) no discriminator triggered, b) with discriminator firing. Note the change in waveform shape and the slightly larger settling time.

the behaved response of Figure 4-15a, the settling time has increased by 10 to 15 ns. Since the preamplifier must also supply valid data to the AMU for further processing, signal deviations of this sort can cause serious errors. The source of this problem stems from high-order nonideal substrate coupling of the fast switching discriminator output to the charge-sensitive input of the preamplifier.

Interactions of this nature have become a major problem as system integration has continued to increase. Several modeling approaches including numerical, analytic and curve fitting techniques have sought to solve this three dimensional problem [28,29]. However, most of these approaches are either too simplistic or require too much processing time to be of any real value. The physical nature of substrate coupling comes from parasitic capacitance and inductance as well as substrate resistance which provide an electrical connection between circuitry that would otherwise be isolated. This representation may be seen in the substrate model shown in Figure 4-16 where the contact nodes represent the path of the electrical connection. The simple model of Figure 4-16 provides a means of representing the resistive, capacitive and inductive elements associated with substrate coupling. Typically the direct coupling element or substrate resistance is of relatively low value in CMOS processes in order to suppress latch-up conditions. Under these low resistivity substrate conditions Gharpurey and Meyer [28] have shown that the addition of guard rings around devices proves ineffective in reducing the effects of coupling due to the presence of vertical current flow. However, if a high resistance substrate is utilized such as in some BiCMOS processes, guard rings can be effective in reducing the

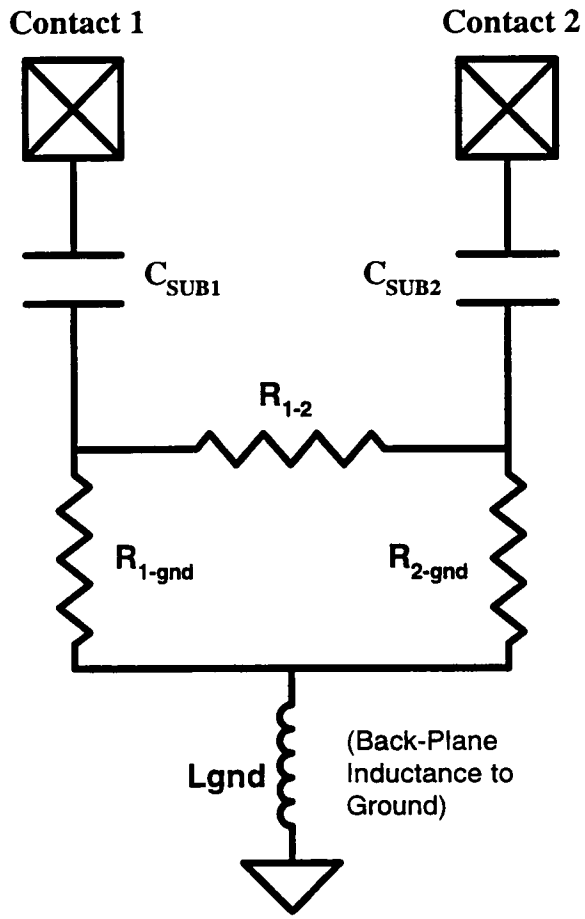


Figure 4-16. Simple model representation of the parasitic elements responsible for substrate coupling.

effects of substrate coupling. Based on these findings there appears to be very little that can be done to reduce the substrate coupling exhibited in the preamplifier / discriminator chip other than place each circuit on a separate die. One possible way of avoiding the problem is to delay writing to the AMU until the preamplifier response has settled. The feasibility and physics impact of such a solution is currently under evaluation.

Evaluation of the TGV4 chip in the frame work of the 32-channel MVD beam test system provided an excellent opportunity to evaluate the CLC426 voltage feedback operational amplifier. Connected in a transimpedance configuration, the amplifier served to convert the summed currents from each firing discriminator into a representative voltage suitable for flash analog-to-digital conversion. The simulation plots of Figures 3-42 and 3-43 pointed to the need to have an external compensation as well as an input compensation capacitor valued at 10 pF combined with a 2 KΩ feedback resistor. However, evaluation with these component values produced an undesirable oscillation. To eliminate the oscillation, the input compensation capacitor was lowered from 10 pF to 4.7 pF. This nonideal effect was most likely the result of parasitic capacitances on the critical nodes of the circuit. Nevertheless, with the compensation capacitor modified, the circuit functioned properly. A typical output is shown in Figure 4-17.

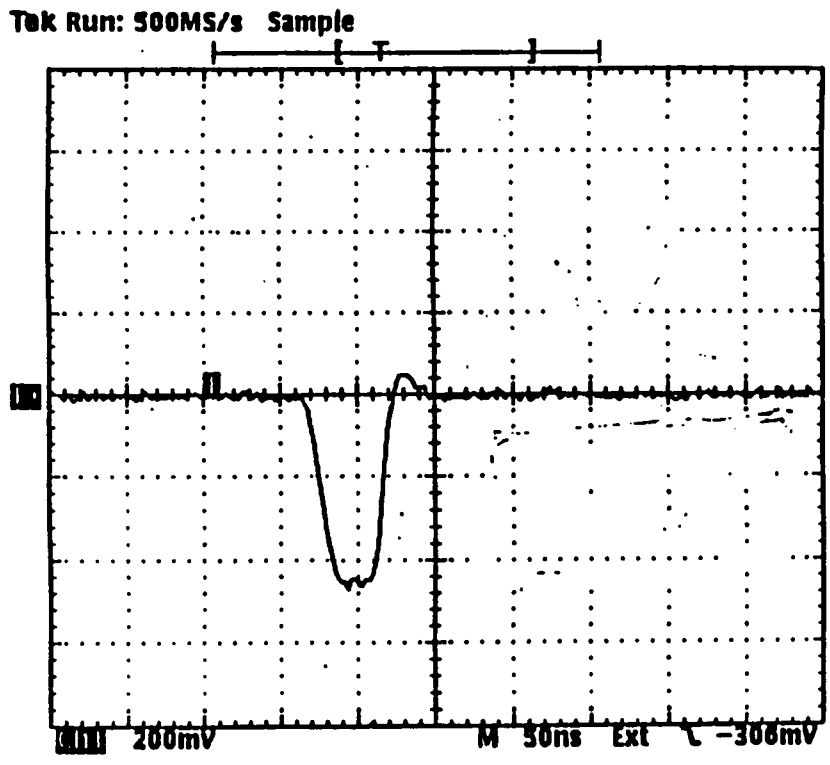


Figure 4-17. Typical output response of the transimpedance current sum readout amplifier.

4.2 Long Channel Device Modeling

As a means of verifying the performance and characteristics of the long channel transistors utilized within the dc feedback loop of the multiplicity discriminator, test structures were constructed for both n- and p-channel devices with serpentine and goalpost geometries. Based on the results of the tests performed using the HP4145B Semiconductor Parameter Analyzer an appropriate model can be generated to accurately represent the performance of the device under certain bias conditions. Specifically, since these MOS devices are used to generate a high valued resistance, characterization within the ohmic region is critical if an accurate model is to be developed. In addition to developing simple Level 1 and Level 2 HSPICE models, the performance of existing BSIM and Level 3 models furnished by Orbit and verified by ORNL will also be evaluated.

The two most important questions associated with the use of nonstandard geometry structures such as the goalpost and serpentine devices used by the multiplicity discriminator are: 1) Do these transistors behave in a normal fashion and 2) Can their characteristics be accurately modeled by either simple Level 1,2 or existing models such as BSIM, Level-3 etc. To answer the first question one only needs to examine a set of characteristic curves (Id vs. Vds for varying Vgs) for each of the proposed structures. Figures 4-18 through 4-21 provide measured results obtained via the HP4145B parameter analyzer of typical curves for Vgs from 1 to 5 V in 1 V increments. Clearly, the transistors appear to function as normal MOS devices from the ohmic region through saturation. Due to the small W/L ratio, the drain current

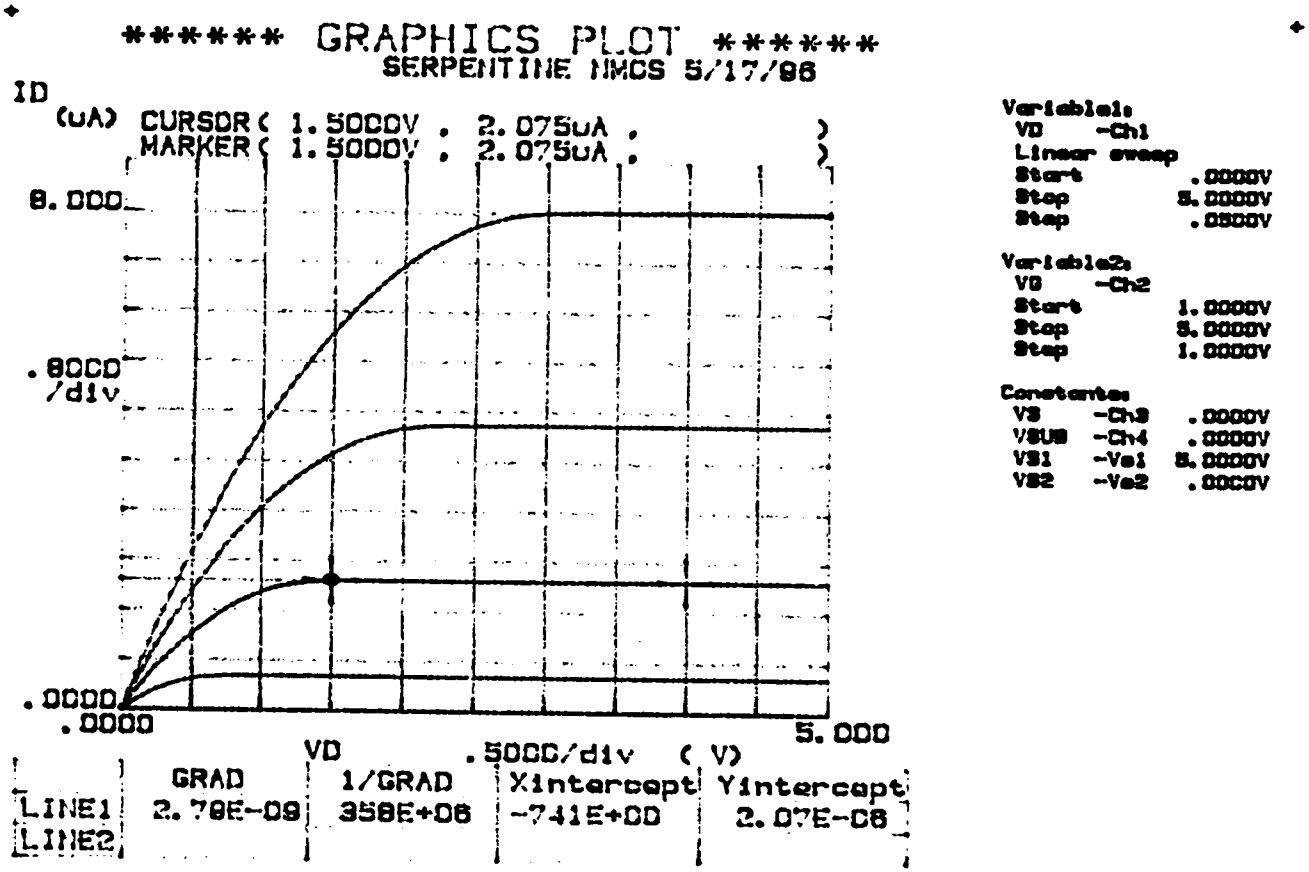


Figure 4-18. Serpentine NMOS characteristic Id vs. Vds curves.

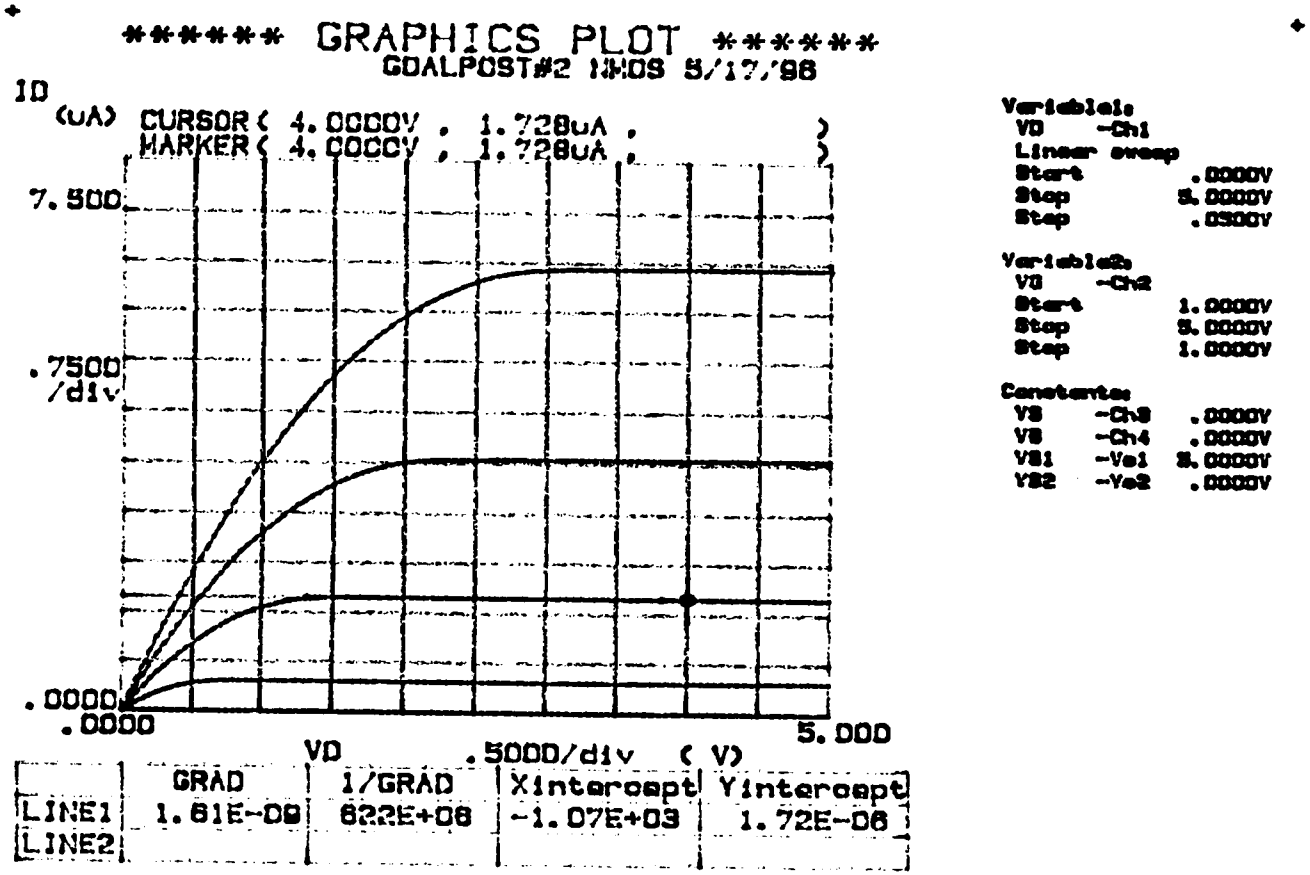


Figure 4-19. Goalpost NMOS characteristic Id vs. Vds curves.

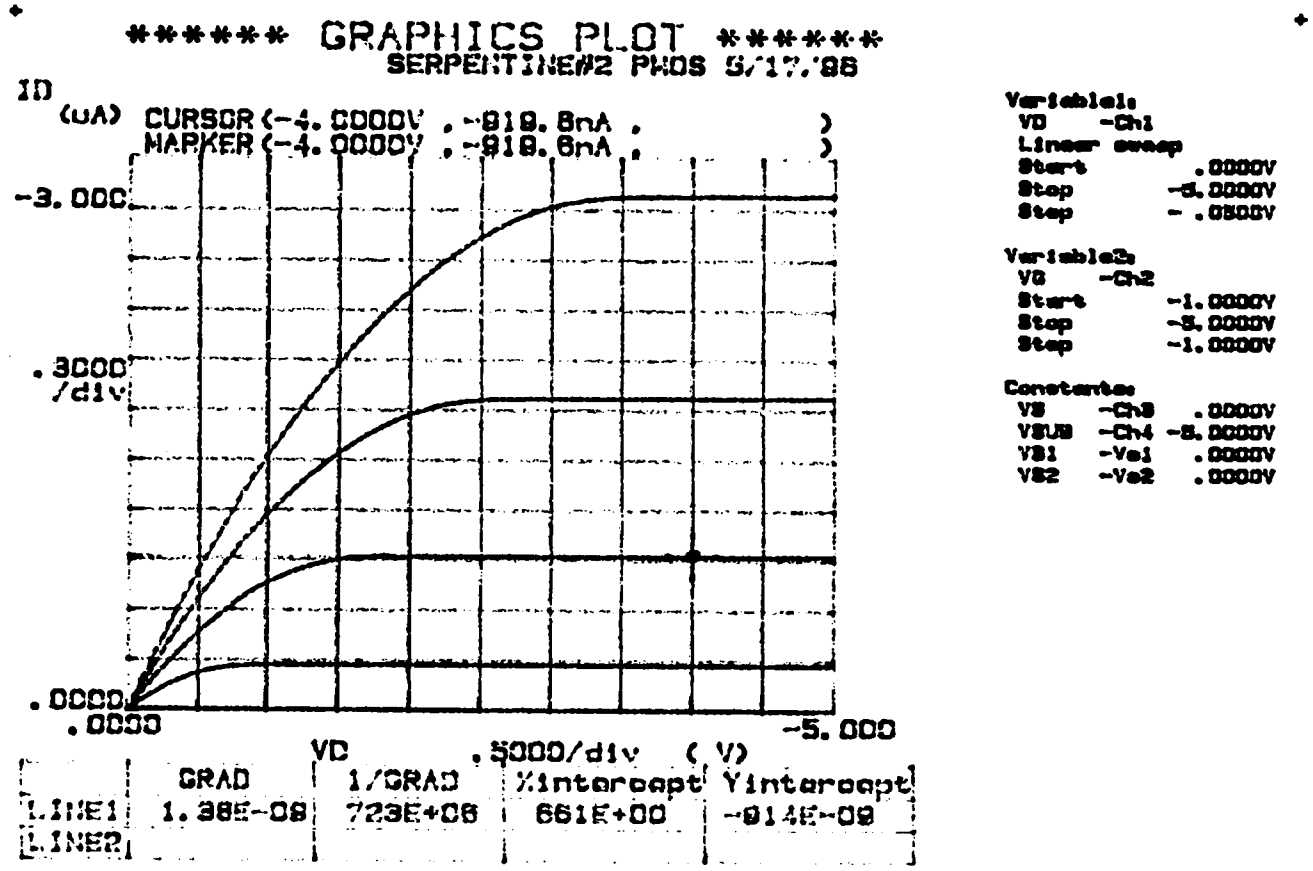


Figure 4-20. Serpentine PMOS characteristic Id vs. Vds curves.

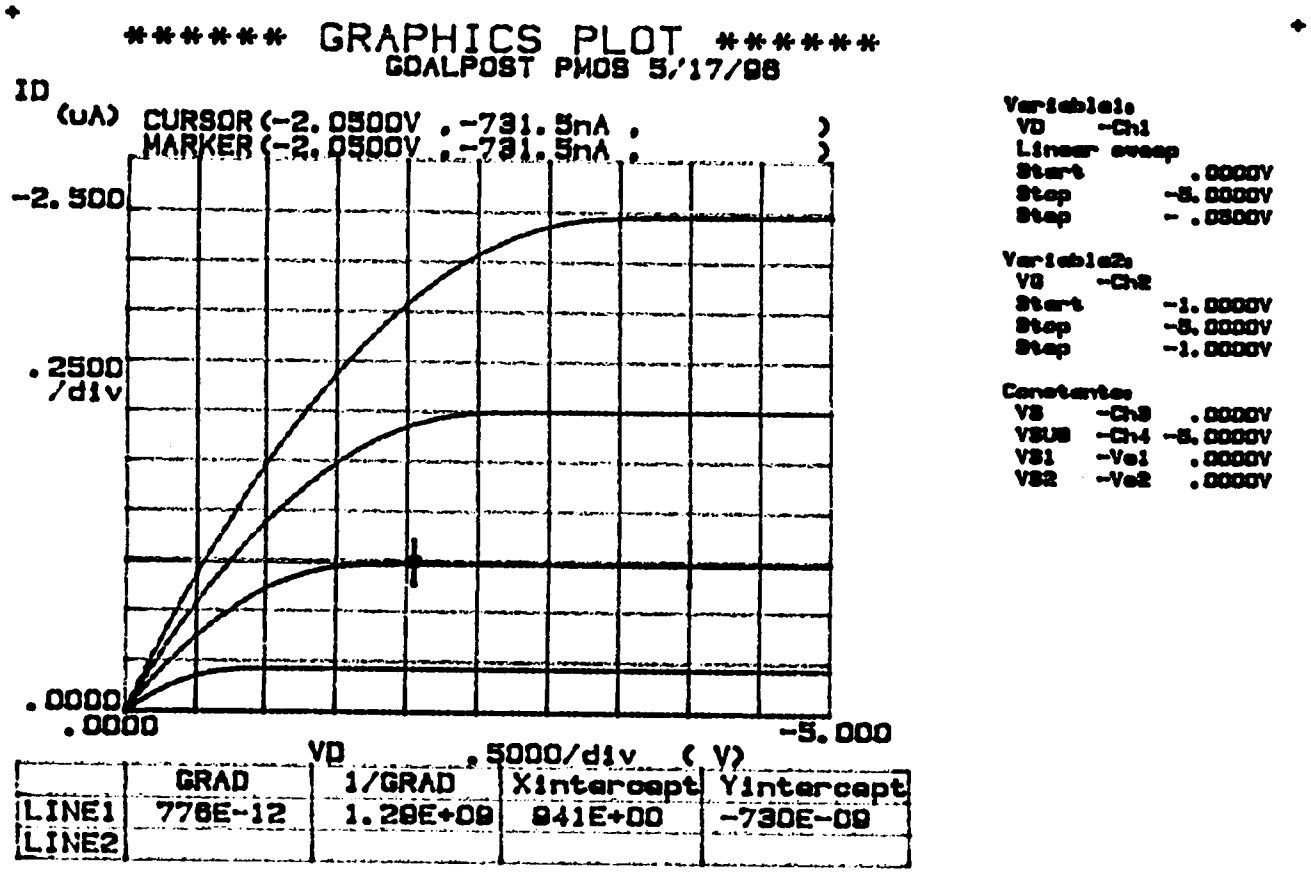


Figure 4-21. Goalpost PMOS characteristic Id vs. Vds curves.

(Id) in saturation is rather low with the n-channels having roughly 2.5 times that of p-channels due to the increased mobility of electrons over holes. One unexpected result illustrated in Figures 4-18 through 4-21 is the roughly 15 percent increase in Id for the serpentine structures over the goalpost configuration. Although both devices have similar drawn lengths, the goalpost is slightly shorter (92.4 μ) than the serpentine (95.4 μ). From the basic drain current equation

$$I_D = \frac{\mu C}{2}(\frac{W}{L})(Vgs - Vt)^2 \qquad \textbf{(4.2)}$$

the shorter length of the goalpost structure should provide a slightly larger Id than that obtainable with the serpentine device. Thus one can only conclude that the effective length of the serpentine transistor is much less than that drawn due to the edge effects inherent to the structure. Indeed a reduction in L from the drawn 95.4 μ to roughly 80 μ produces a drain current which is consistent with that observed from the goalpost structure.

Although the performance of the serpentine and goalpost transistors in the saturation region is important , due to their use within the multiplicity discriminator design, ohmic region operation is of much greater concern. As in the case of saturation, drain current in the ohmic region is given by

$$I_D = \mu C_{ox}(\frac{W}{L})[(Vgs - Vt)Vds - \frac{Vds^2}{2}] \qquad \textbf{(4.3)}$$

and is directly proportional to the (W/L) ratio. Since the obtainable resistance is determined by the slope of the Id vs. Vds characteristic curve as illustrated by

$$R_{DS} = \frac{Vds}{I_D} \tag{4.4}$$

an increase in drain current dictates a smaller Rds for a fixed Vds. Thus based on this conclusion the goalpost structures should achieve a higher Rds than their corresponding serpentine counterparts. To verify this experimentally, the ohmic region of any of the curves in Figures 4-18 through 4-21 could be used to obtain an accurate measure of the slope. However, to better match the conditions under which the device is actually being utilized an appropriate Vgs should be selected at which the needed tests can be performed. Using the stable conditions found for the DSCRM_TST chip with the control node voltage at roughly 3.5 V should place the operating Vgs of the device between 1.5 and 2.5 V. Thus performing the required Id vs. Vds sweep for a Vgs of 2 V produces values of 760 KΩ and 990 KΩ for the n-channel serpentine and goalpost devices respectively. Although the p-channel transistors are not active in the multiplicity discriminator, the same procedure was followed for a Vgs of -2 V and yielded values of 1.9 MΩ and 2.4 MΩ for the serpentine and goalpost structures. As theorized, the goalpost device has a higher Rds value due to the longer effective channel length.

To generate any SPICE model capable of representing the actual performance of the long channel devices requires the defining of several parameters. For simple Level 1 or Level 2 models these parameters include the zero-bias threshold voltage VTO, intrinsic transconductance parameter KP, body effect factor GAMMA, and channel-length modulation parameter LAMBDA [30,31]. VTO may easily be

obtained by plotting the square root of the drain current Id verses gate voltage Vg for a constant Vds. Figure 4-22 illustrates such a plot. The zero-bias threshold voltage may be observed to occur at the x-intercept of a line drawn tangent to the sloping line. For the n-channel serpentine structure, the measured VTO is roughly 0.91 V. Clearly from the plot it is evident that such long channel devices truly follow the square law model. Repeating this procedure for the goalpost structure yields a nearly identical result while the p-channel devices were found to have a VTO of -0.85 V. The curve of Figure 4-22 also serves as a means of determining the intrinsic transconductance parameter KP. Manipulation of Eq. 4.2 yields an expression for KP given by

$$KP \approx 2\left(\frac{\Delta\sqrt{I_D}}{\Delta Vgs}\right)\left(\frac{L}{W}\right) \qquad \textbf{(4.5)}$$

which may be used to compute an appropriate value. Since the devices were not wired such that the body terminal could be brought out of the chip, the GAMMA parameter was determined by adjusting its value until simulated results matched the previously discussed curves. Inclusion of the channel length modulation parameter LAMBDA was made possible by observing the slope of the drain current in saturation of Figures 4-18 through 4-21. The final parameters included in the simple Level 1 and Level 2 models was the surface inversion potential PHI which is present in the calculation of the effective threshold voltage and the substrate doping NSUB. If PHI is not specified the simulator will calculate a value based on the provided NSUB. If NSUB is not provided the simulator uses the GAMMA term to calculate a substrate doping value. By specifying these terms HSPICE is forced to use the provided values

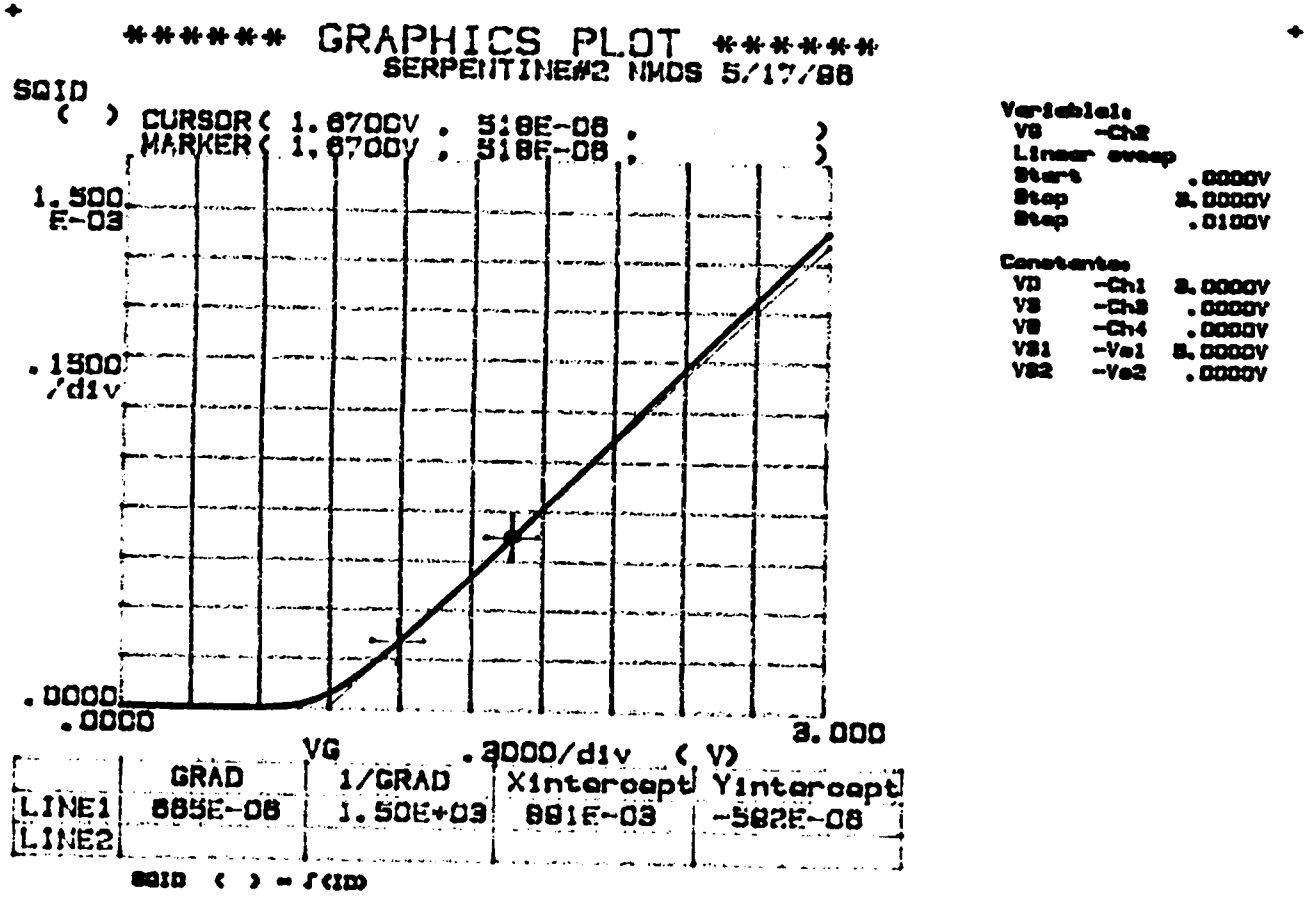


Figure 4-22. Serpentine NMOS √Id vs. Vg.

instead of calculating values based on other parameters. Table 4.3 provides a list of the terms used in the models for each of the test devices.

Table 4.3. Defined Parameters for Level 1 and Level 2 Models

Device	VTO (V)	KP (A/V^2)	GAMMA ($V^{1/2}$)	LAMBDA (1/V)	PHI (V)	NSUB (cm^{-3})
NMOS Serpentine	0.91	50E-6	0.50	1.35E-3	0.60	5.70E+16
NMOS Goalpost	0.90	40E-6	0.50	1.04E-3	0.60	5.70E+16
PMOS Serpentine	-0.85	26E-6	0.50	1.4E-3	0.60	5.70E+16
PMOS Goalpost	-0.85	20E-6	0.50	1.06E-3	0.60	5.70E+16

Using the parameters of Table 4.3 HSPICE simulations were performed for Level 1 and Level 2 modeling. Both models did an adequate job of representing the device while in saturation. However, for linear operation both models were slightly optimistic in the measured Rds. Additionally, the calculated Vdsat for the Level 1 model was excessively high. For this reason the Level 1 model was judged to be too simplistic to produce accurate results. Although the Level 2 model was optimistic with respect to Rds, the calculated Vdsat was much closer to that actually observed. As a basis for comparison Figures 4-23 and 4-24 present actual measured characteristic curves and simulated (Level 2 model) results respectively for the n-channel serpentine device. To further examine the relationship between measured and simulated results several additional models including BSIM and Level 3 (see

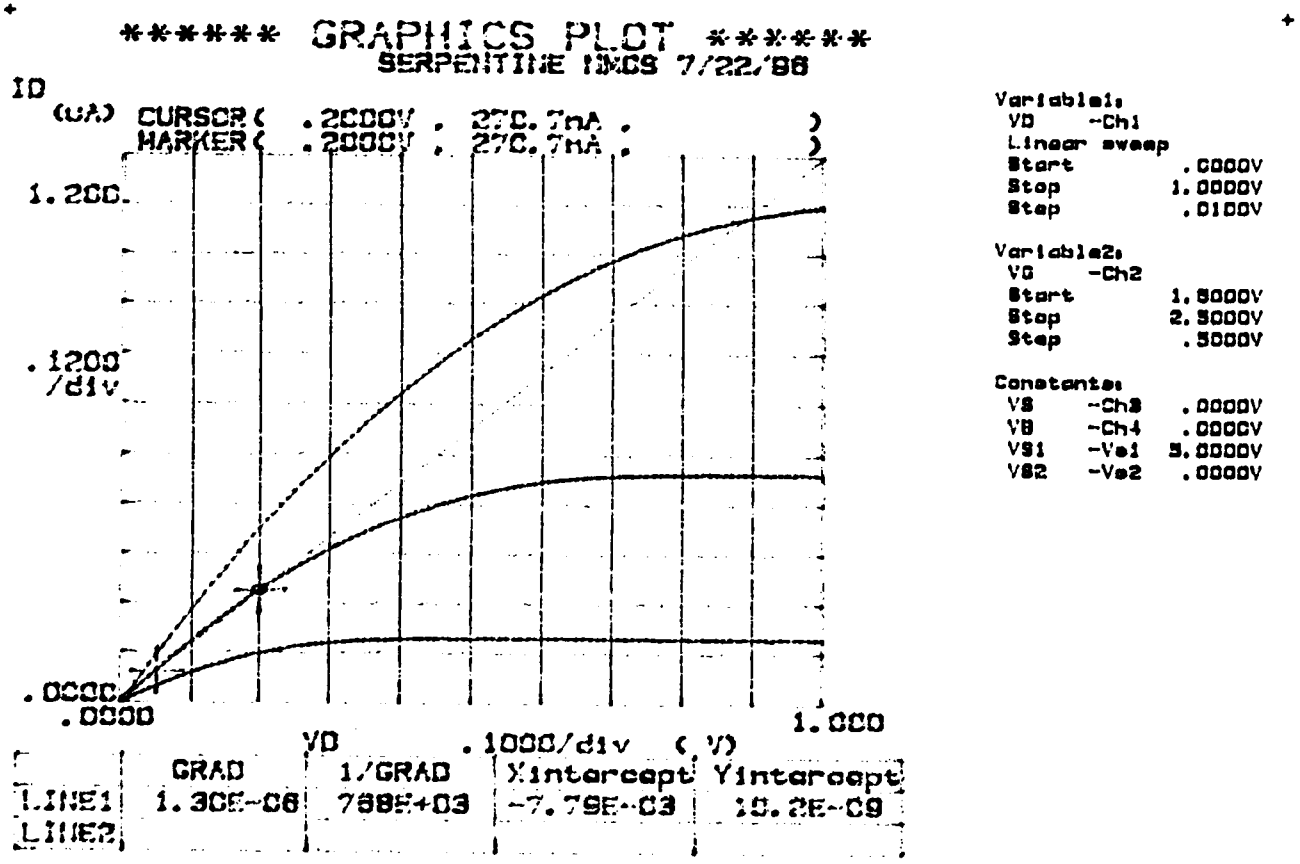


Figure 4-23. Parameter analyzer plot of serpentine NMOS for Vgs = 1.5 V, 2 V and 2.5 V.

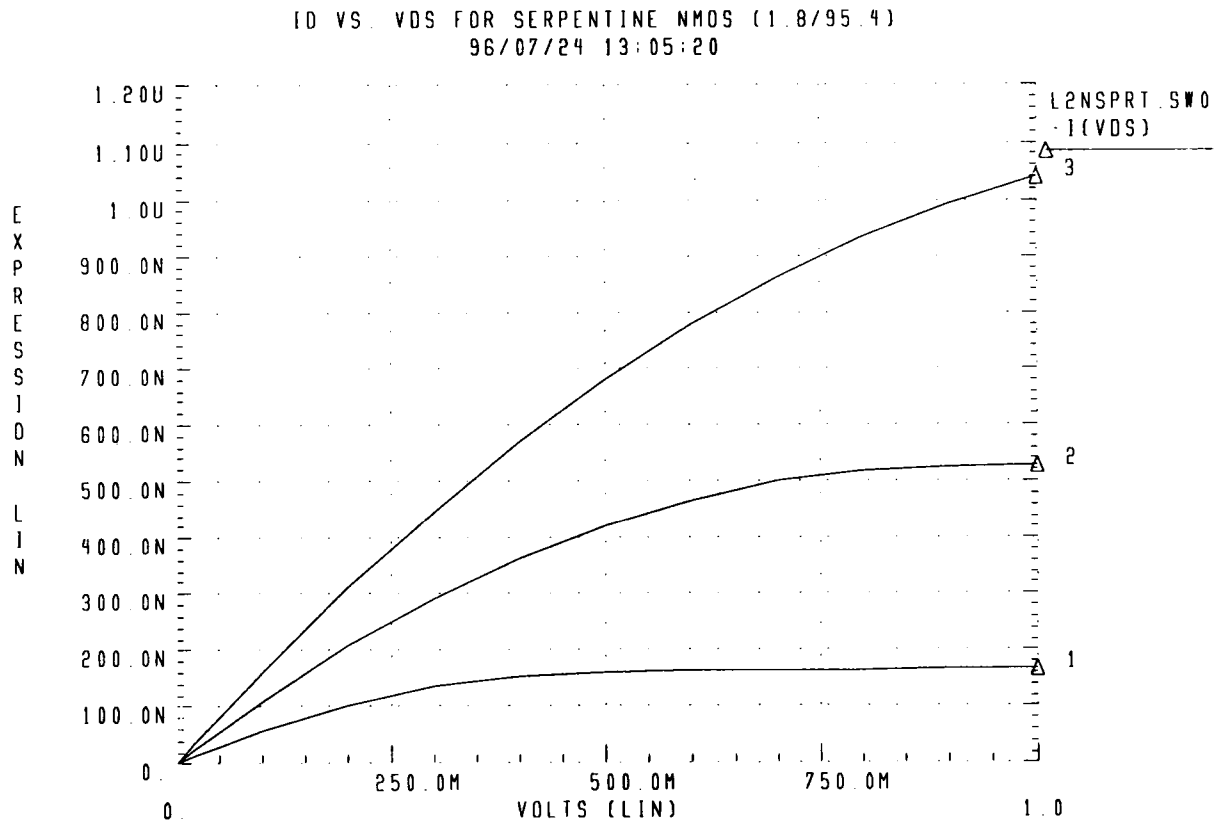


Figure 4-24. Simulated results using level 2 model for serpentine NMOS device.

Appendix 2). Figure 4-25 is an HSPICE plot of the characteristic curves over the range of interest for Level 2, BSIM and Level 3 fast models. Comparing Figure 4-23 to Figure 4-25 it is obvious that 1) Level 2 model is optimistic in the linear region with Id in saturation approximately equal to that measured; 2) BSIM calculated Rds in the linear region is pessimistic while the simulated drain current in saturation is slightly optimistic; 3) Level 3 fast model appears to be the best representation for both regions of operation. These conclusions also apply to the goalpost n-channel devices.

Repeating the above comparison for the p-channel devices yields a much different scenario. While Level 3 illustrated the best matching for the n-channel devices with Level 2 and BSIM being overly optimistic and pessimistic, modeling of the p-channel devices using these same models with the appropriate parameters produced the exact opposite results. Once again comparing the measured plot for the PMOS serpentine transistor in Figure 4-26 and the HSPICE plot of Figure 4-27 generate several conclusions. Though matching fairly well within the saturation region of operation, the Level 2 model under estimates the resistance of the linear region. Whereas the Level 3 model accurately predicts the characteristics of the NMOS device, the PMOS Level 3 simulation grossly over estimates the linear region resistance and under estimates the saturation drain current. BSIM models appear to better match the linear region while remaining somewhat conservative in the saturation region.

Although the Orbit BSIM and Level 3 models could be adjusted to better match the observed results of the long channel transistors, the main purpose of

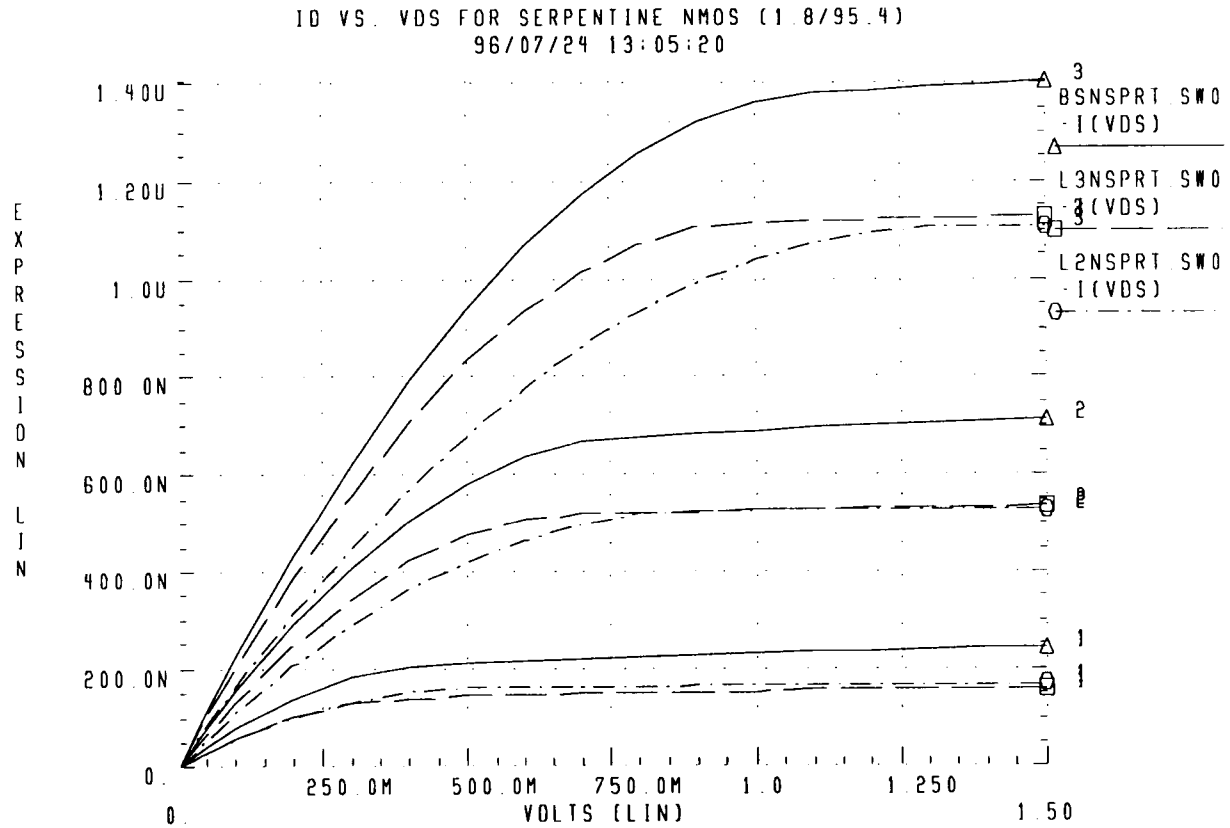


Figure 4-25. Comparison of level 2, level 3 and BSIM models for serpentine NMOS device.

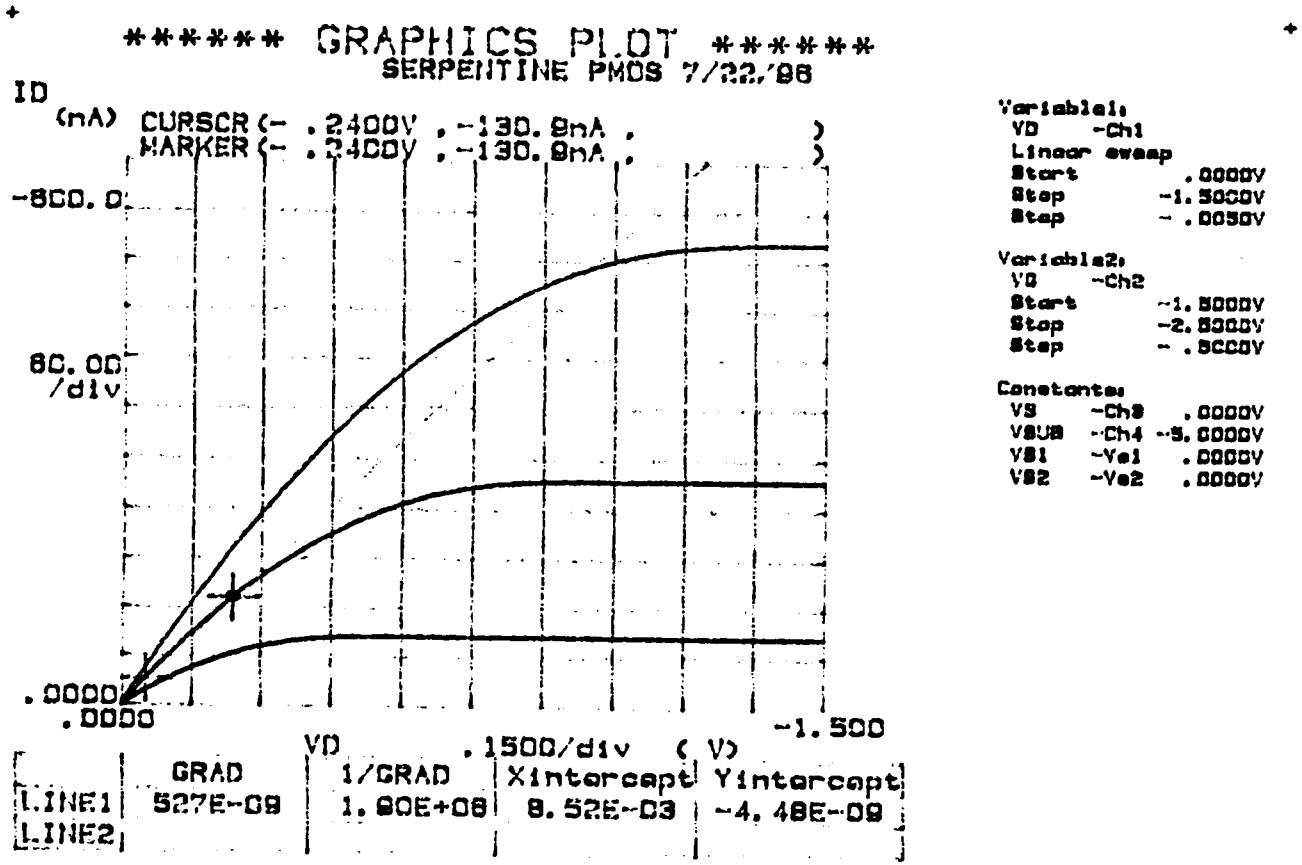


Figure 4-26. Parameter analyzer plot of serpentine PMOS for Vgs = -1.5 V, -2 V and -2.5 V.

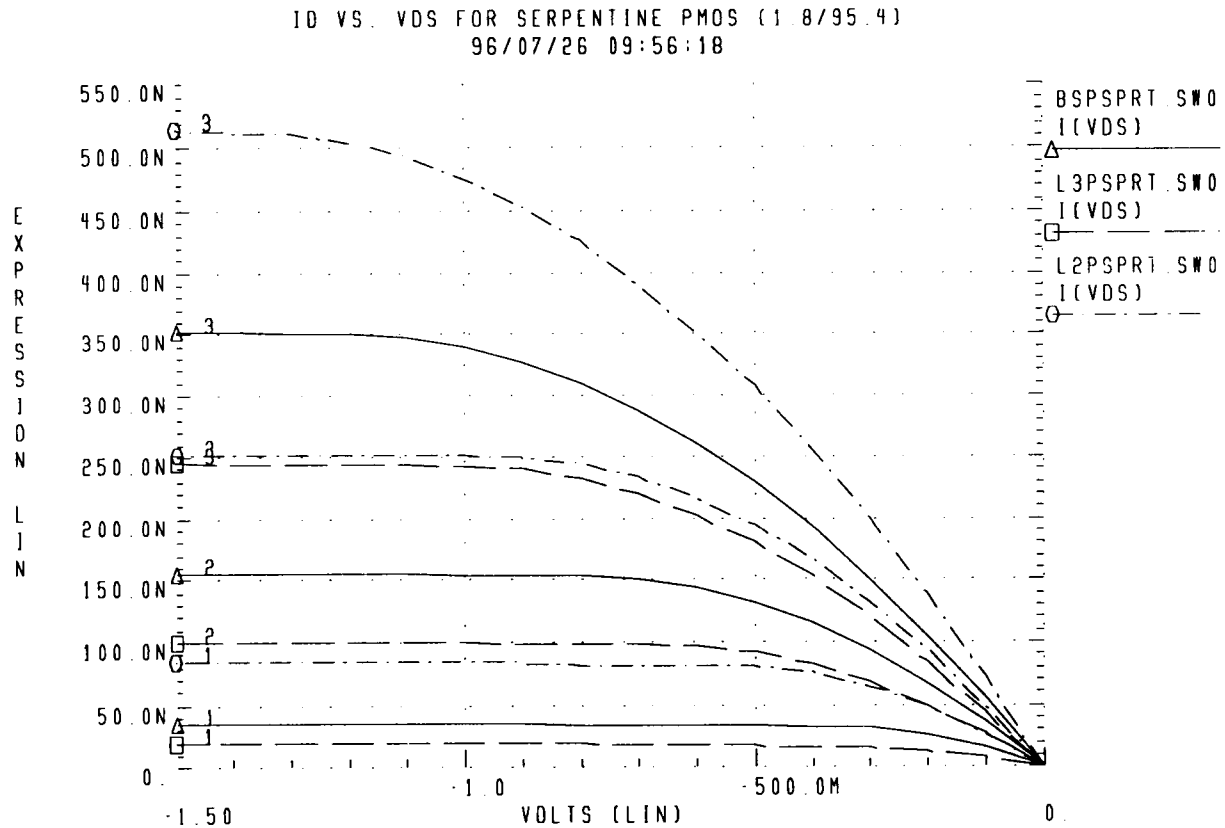


Figure 2-27. Comparison of level 2, level 3 and BSIM models for serpentine PMOS device.

presenting them is to allow a means of comparison with Level 2 simulations. On the average, the simple Level 2 models created for each of the four structures proved to provide an adequate representation of the actual device performance. Though slightly optimistic for NMOS and pessimistic for PMOS in the linear region, manipulation of the KP and LAMBDA terms allow for excellent saturation region modeling.

Chapter 5

Design Modifications

Several of the results presented in Chapter IV point to the need for slight modifications in the multiplicity discriminator design. Although the multiplicity discriminator could be utilized in its present state, resolving issues such as instability, lack of adequate adjustability and excessive threshold mismatch would only improve the usefulness and robustness of the design. Several specific changes have been proposed to alleviate these nonideal characteristics. These changes include modifications to the input differentiator designed to improve threshold matching and range of adjustability. Additionally, instability issues are addressed by the use of a higher value and higher density hold capacitor structure within the dc feedback loop. Each of these changes will now be described in detail as they relate to critical performance details of the multiplicity discriminator.

5.1 Input Differentiator Modifications

Of the changes to be made to the multiplicity discriminator most occur within the input differentiator topology. As established previously (Chapter III) the input differentiator plays a significant role in several critical specifications such as speed and

gain adjustment. The results of Chapter IV further illustrate the dependence of threshold matching on the input differentiator. Since the differentiator circuit is not contained within the dc feedback loop, any errors generated by process deviations directly affect the channel-to-channel matching characteristics of the discriminator. There are however several preventative measures which can be implemented to reduce the effects of process variation on the common threshold matching. The most simple of these is to reduce current mirror mismatch within the differentiator circuit. It has been shown that drain current mismatch is inversely proportional to the channel length [17]. Thus increased matching and reduced susceptibility to process variations requires an increase in the drawn channel length dimension. Ideally, a length of many times the minimal feature size (1.2 μ) should be implemented to minimize these random; processing effects. Practically, there exists a limit to the device sizing within the area constraints of the multiplicity discriminator. With this in mind, maintaining the same W/L ratio, an acceptable length for differentiator current mirror devices was determined to be 4.8 μ. It should be noted that it was not necessary to increase the current source channel lengths for the differential amplifiers due to the presence of the negative feedback network.

Although increasing the channel length of the input differentiator biasing devices should eliminate most of the undesirable threshold mismatch exhibited by the DSCRM2 circuit, additional measures can be taken to compensate for remaining errors. The graph of Figure 4-3 illustrated the variation in minimal detectable input signal as a function of bias current. Thus manipulation of the input differentiator bias

current represents a means by which individual channels could be adjusted over roughly 10 mV. With 34,000 channels of multiplicity discriminator required by the FEE of the MVD such calibration would require tremendous amounts of system resources and would be impractical. However, since most threshold variations across a die were found be in the 10 to 14 mV range adjusting the bias current on a chip-by-chip basis could provided an adequate solution to the problem. For example, suppose the lowest gain channel requires an input signal 10 mV larger than the highest gain channel in order to trigger the discriminator. If the lowest gain channel is to fire on a 20 mV input, the high gain channel must trigger on 10 mV signals. By increasing the bias current over an established range, this scenario could be realized at a much reduced cost of system resources.

Implementing the needed range of current adjustment was carried out by switching in varying sized devices to add to the total bias current. To reduce the number of current sources and switches needed, a range of 13 to 22 μA for a nominal bias of 19 μA (R = 200 KΩ) was selected. As seen by the simulated results of Figure 5-1, for fixed Vthresh and Vgain settings this range provides a 14 mV adjustment capability. Realization of this range may be easily achieved by establishing a main reference (reference which is always on) of 13 μA and two switchable current sources of values 3 μA and 6 μA. Control switches for the lesser current sources are realized by insertion of a simple n-channel switch. When a logic high is applied to the gate of the n-channel transistor the current source is turned on and the input differentiator bias current increases. The 2-bit control required is well within the available processing

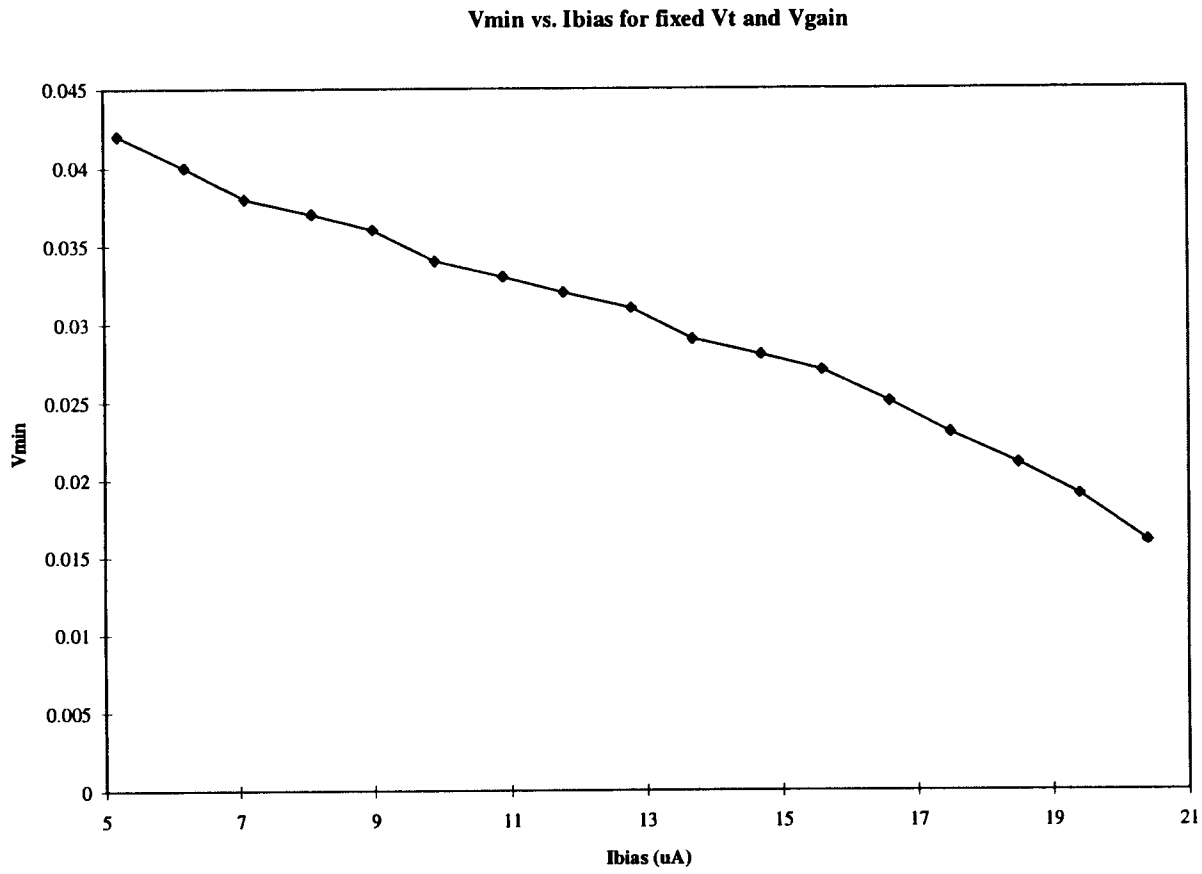


Figure 5-1. Minimum input as a function of bias current.

capabilities of the Heap Manager serial interface. A schematic of the modified input differentiator may be seen in Figure 5-2.

One very evident problem as seen by the results of TGV4 chip testing was the inability to adjust the discriminator such that input signals greater than 60 mV would not generate a trigger. To provide a more versatile circuit a new range of adjustment from 20 to 400 mV was established to replace the previous 20 to 60 mV range. The ability to move the triggering point from 20 mV to 400 mV requires the input differentiator to provide a high level of attenuation as well as gain. Since the main mechanism for controlling this characteristic is through the Vgain adjustment, appropriate sizing must be performed on the ohmicly biased transistor serving as the gain resistor. After extensive simulations a W/L ratio of (10.2/3.6) was determined to yield the needed range for the gain transistor. For Vgain voltage settings of 0 V (minimum gain) and 3.5 V (maximum setting) the resistance was observed to change from 3.5 KΩ to 23 KΩ. A plot of the simulated input required to trigger the discriminator for varying Vthresh and Vgain settings may be seen in Figure 5-3. Since no one setting of Vgain produces the complete range of 20 mV to 400 mV, a choice must be made by the user whether the discriminator will be placed in a high or low gain configuration. Setting Vgain = 3.3 V establishes a high channel gain and provides a range of roughly 20 mV to 80 mV. Decreasing Vgain to roughly 1 V allows inputs of over 400 mV to be suppressed while increasing the minimal signal to roughly 90 mV. Although these ranges do not overlap, the extended control over discriminator firing should be adequate while providing a much more versatile circuit topology.

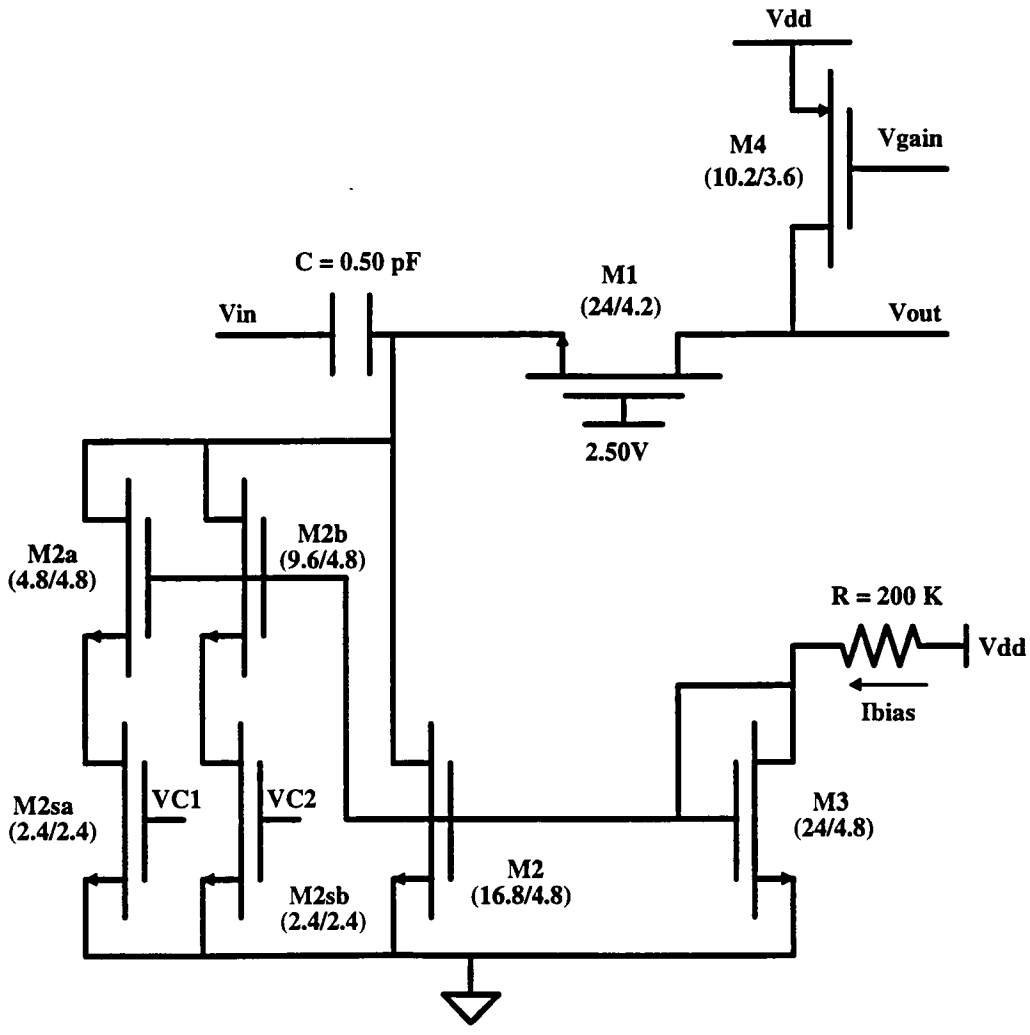


Figure 5-2. Complete schematic of modified input differentiator.

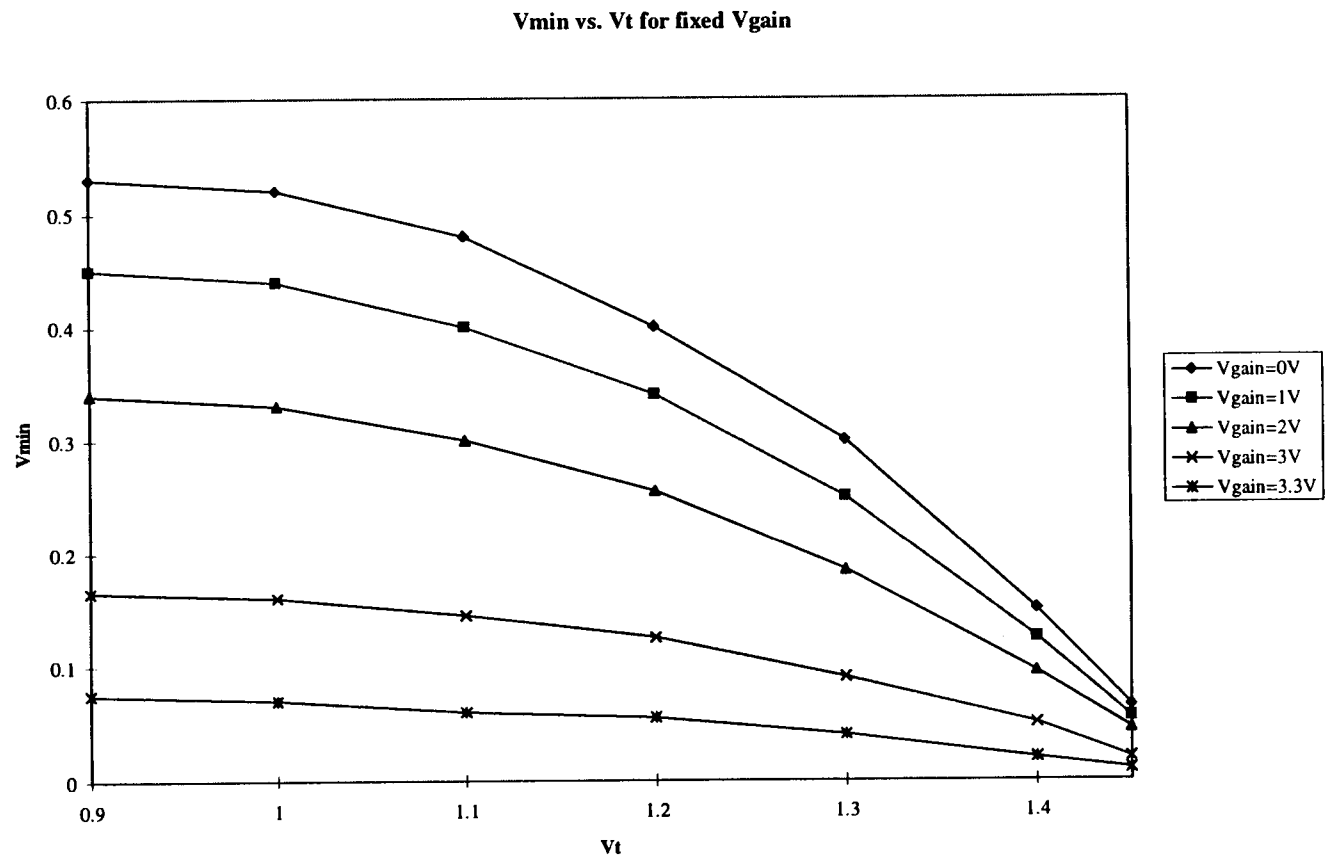


Figure 5-3. Input required to trigger for various Vt and Vgain settings.

5.2 DC Feedback Loop Modifications

The results of the DSCRM_TST chip and the individual modeling of the serpentine and goalpost long channel devices pointed to the need for a decreased dominant pole in the dc feedback loop in order to increase the stability of the circuit. Since the effective resistance R_Z is already extremely large and would require significant design changes to improve, the obvious choice is to increase the size of the capacitor by two to three times. However, the stringent area requirements of the multiplicity discriminator coupled with the large area required to fabricate high valued capacitors make it very difficult to increase the value of the capacitor. For instance, an 8 pF double poly capacitor having a density of 0.5 fF/μ^2 would require an area of roughly 16,000 μ^2. Keeping within the 85 μ pitch an area of this size would stretch the length of the discriminator by several hundred micron.

An acceptable alternative would be the use of a higher density capacitor structure which enabled large capacitors to be constructed in less area. With a density of roughly 1 fF/μ^2 the MOS capacitor offers a 50 percent reduction in area for the same value capacitor. However, even with the increased density of the MOS capacitor area requirements are still quite excessive. One final structure to consider is that of a much higher density capacitor. As seen by Figure 5-4 the high density structure combines the densities obtained by the poly-poly capacitor and the MOS capacitor into one capacitor with a theoretical density that can approach 2 fF/μ^2. Since the high density capacitor consists of a MOS device with the input signal applied to the gate, it is subject to all the surface charge conditions that are common to MOS transistors.

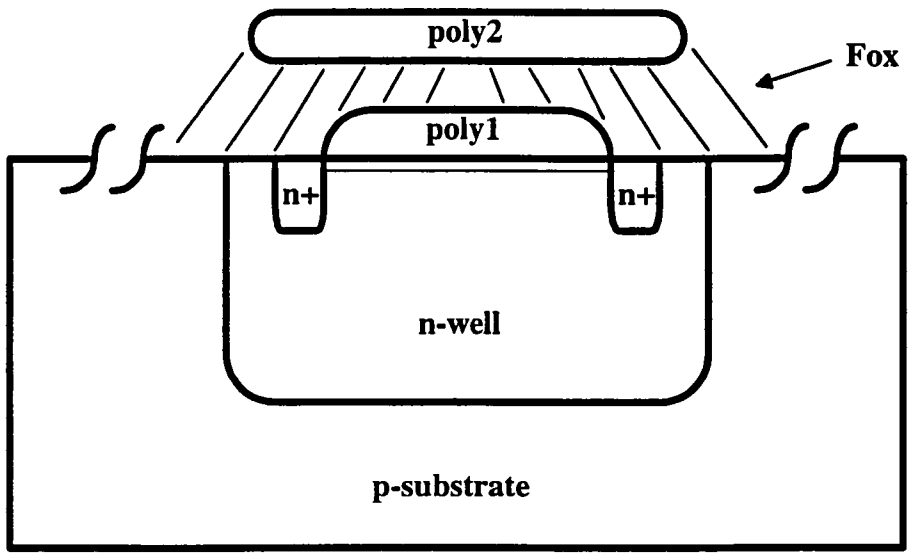


Figure 5-4. High density capacitor structure.

These conditions include accumulation, depletion and inversion and are illustrated by the graph of Figure 5-5 [32]. Assuming PMOS (which is the desired choice for an nwell process) accumulation occurs when negative charge accumulates on the gate and positive charge within the substrate. At this point the effective capacitance value is equal to that shown in Figure 5-4. As the gate voltage becomes less positive electrons become excluded from under the gate an a condition of carrier depletion occurs. While in the depletion region the effective capacitance of the structure decreases to the much lower depletion capacitance of the device. Further decreases in the applied gate voltage force the device further into depletion until a critical value equal to twice the Fermi level is reached. Once this value is obtained a thin channel of holes are created in the depletion layer under the oxide and the device enters into inversion. After entering inversion the capacitance of the MOS device returns to that observed while in the accumulation region.

Two devices whose operation is similar to the theoretical description given above were fabricated in the Orbit 1.2 μ nwell CMOS process. Each structure consisted of a 128 unit array of capacitors having a unit size of 21.6 μ x 21.6 μ. The first device to be evaluated was the PMOS1 capacitor of Figure 5-6. Notice that this device has a structure which is identical to that of Figure 5-4 with the poly2 and nwell layers internally connected. Evaluation of the capacitors performance required the use of a HP4192A LF Impedance Analyzer. To measure the capacitors characteristics under various dc bias conditions which lead to accumulation, depletion and inversion surface conditions, the analyzer applies a small ac signal to one input terminal and

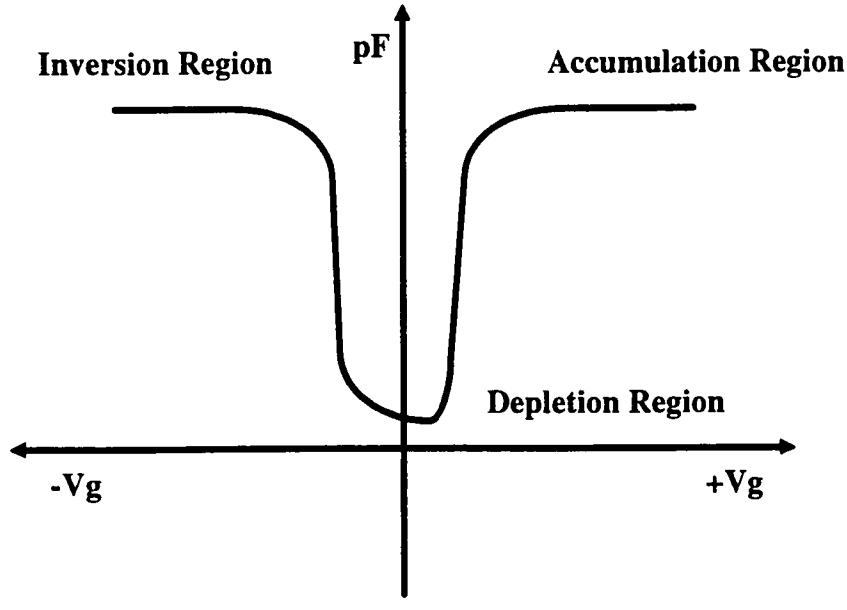


Figure 5-5. Characteristic C-V curve for PMOS capacitor.

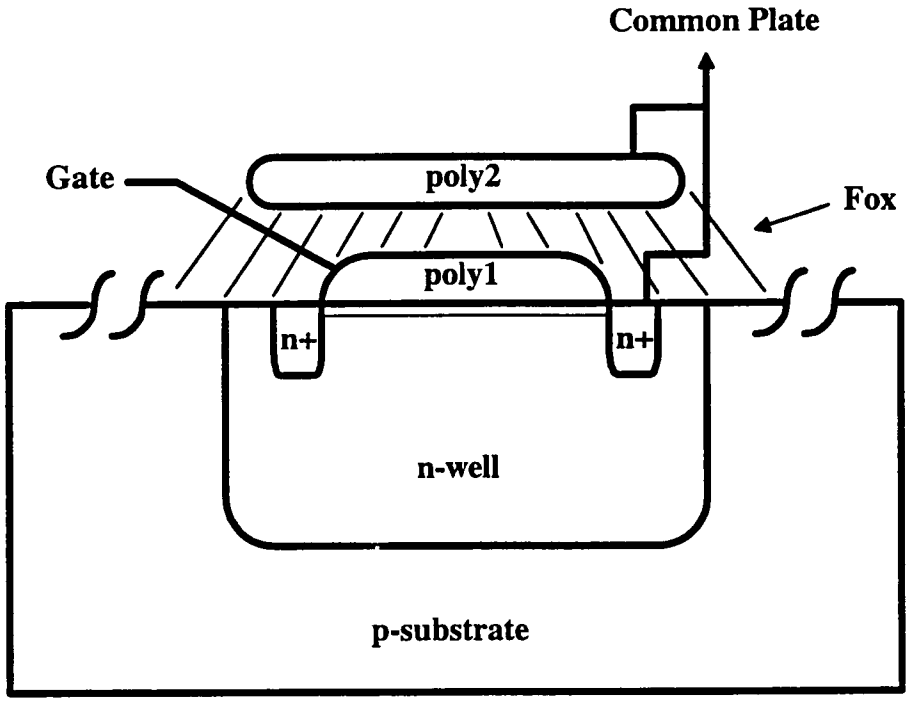


Figure 5-6. PMOS1 high density capacitor structure.

measures the voltage across and the current through the device under test (DUT) as illustrated in Figure 5-7 [33]. With a 5 V power supply providing bias to the protected input pads of the DUT the HP4192A was configured as shown in Figure 5-8. In order to assure a more precise measurement any stray capacitance associated with the 40-pin DIP package was zeroed out. Applying a 1 MHz 30 mV rms ac signal and sweeping the gate voltage of the PMOS1 capacitor from -5 V to 5 V yields the C-V relationship of Figure 5-9. From the plot it is evident that for values of Vg greater than roughly 1 V accumulation is achieved and the high capacitance (roughly 113 pF) generated by the parallel combination of the poly-poly and MOS capacitors is present. This value when divided by the total area of the structure produces a density of 1.9 fF/μ^2. As Vg decreases below 1 V, the device enters into carrier depletion and the much smaller depletion capacitance of approximately 40 pF is measured. However, unlike the theoretical curve of Figure 5-5, PMOS1 never enters inversion but remains in depletion regardless of the applied bias. This result can be explained by the absence of the low resistive path needed by minority carriers to invert the n-type material within the well.

Inclusion of an n^+ diffusion connected to the existing p^+ diffusion provides the much lower resistance path needed by minority carriers to invert the channel. The second structure to be evaluated PMOS2 is identical to PMOS1 with the exception of the additional n^+ diffusion as illustrated by Figure 5-10. Applying the same input as for the PMOS1 testing and sweeping the gate voltage from -5 V to 5 V produces the C-V curve of Figure 5-11. Unlike the PMOS1 structure, PMOS2 exhibits all three surface

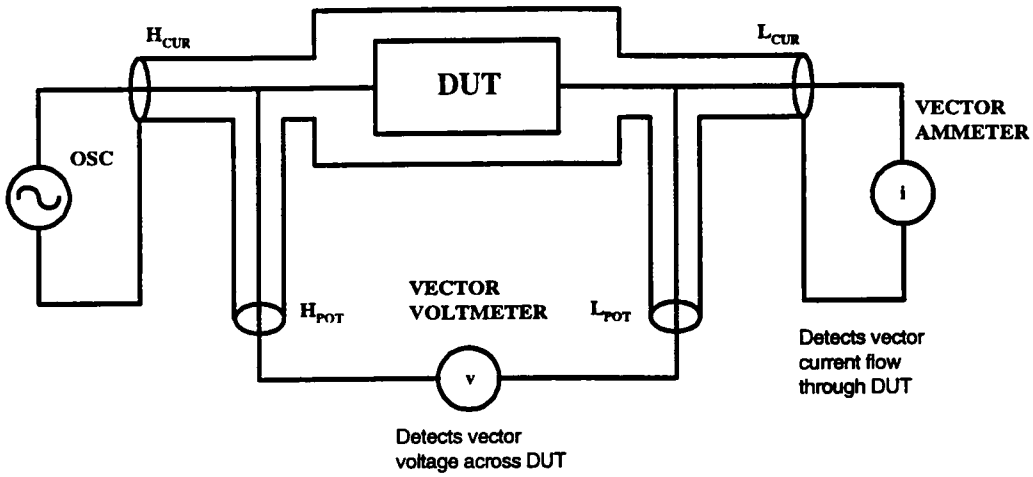


Figure 5-7. HP4192A Impedance Analyzer method of measurement.

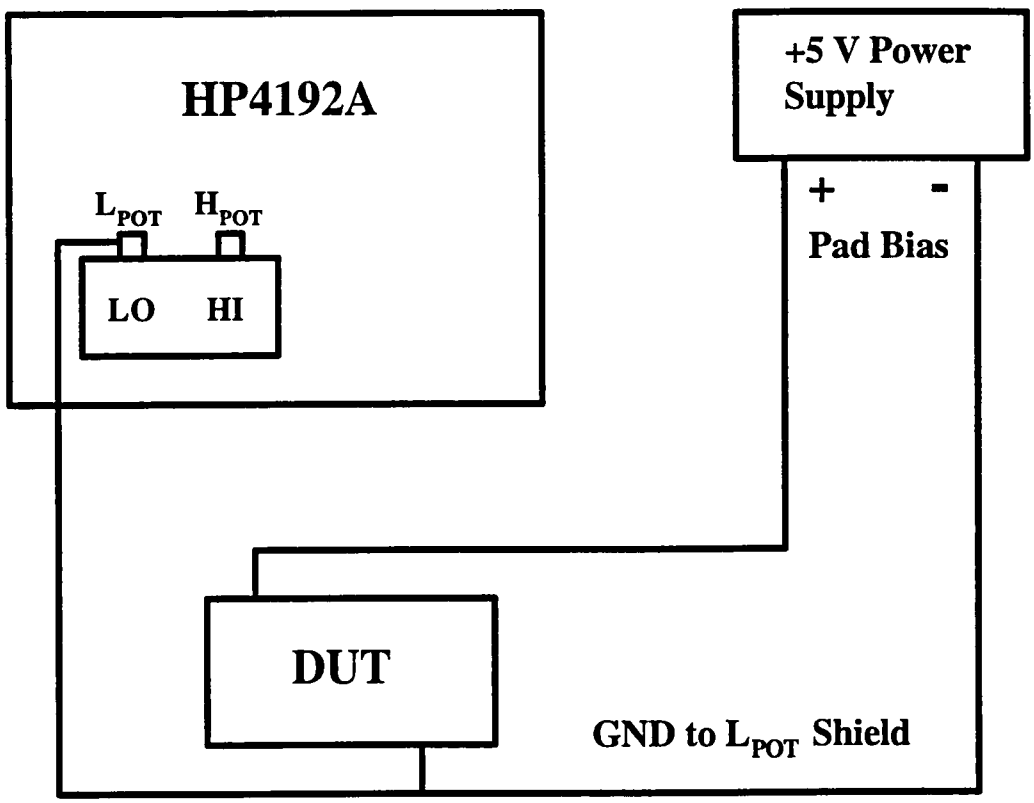


Figure 5-8. Test fixture utilized to evaluate the high density capacitor structure.

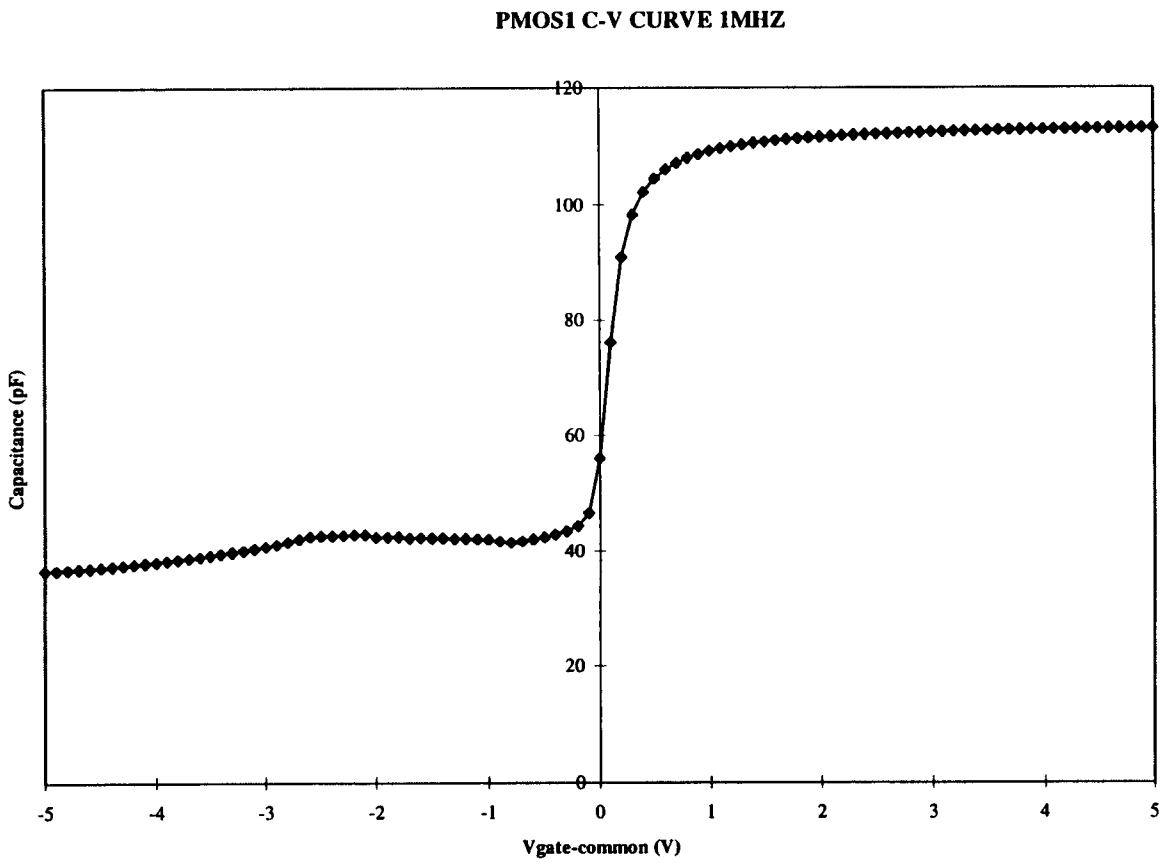


Figure 5-9. C-V characteristic curve for PMOS1 structure.

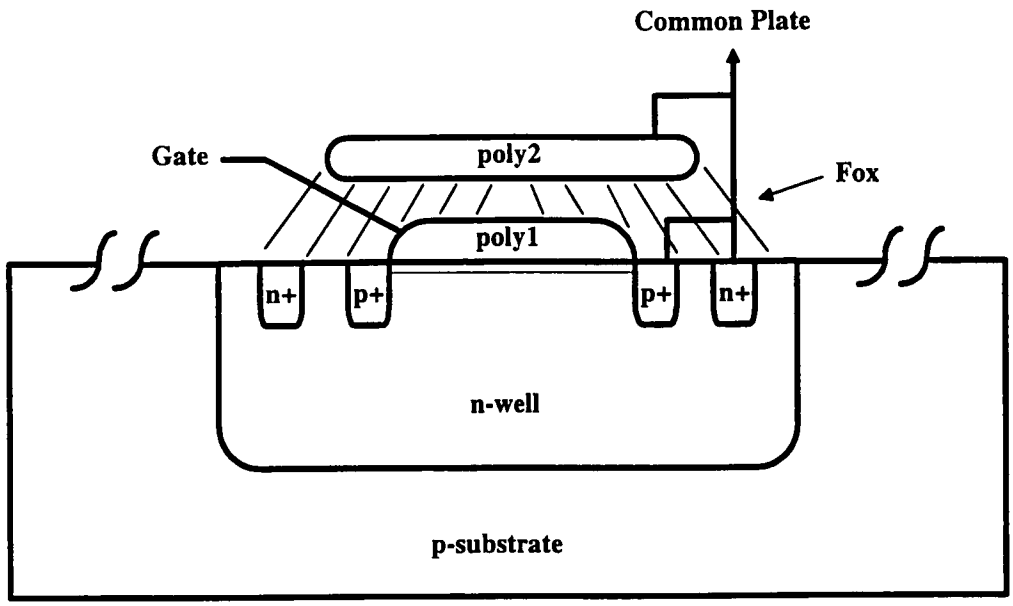


Figure 5-10. PMOS2 high density capacitor structure.

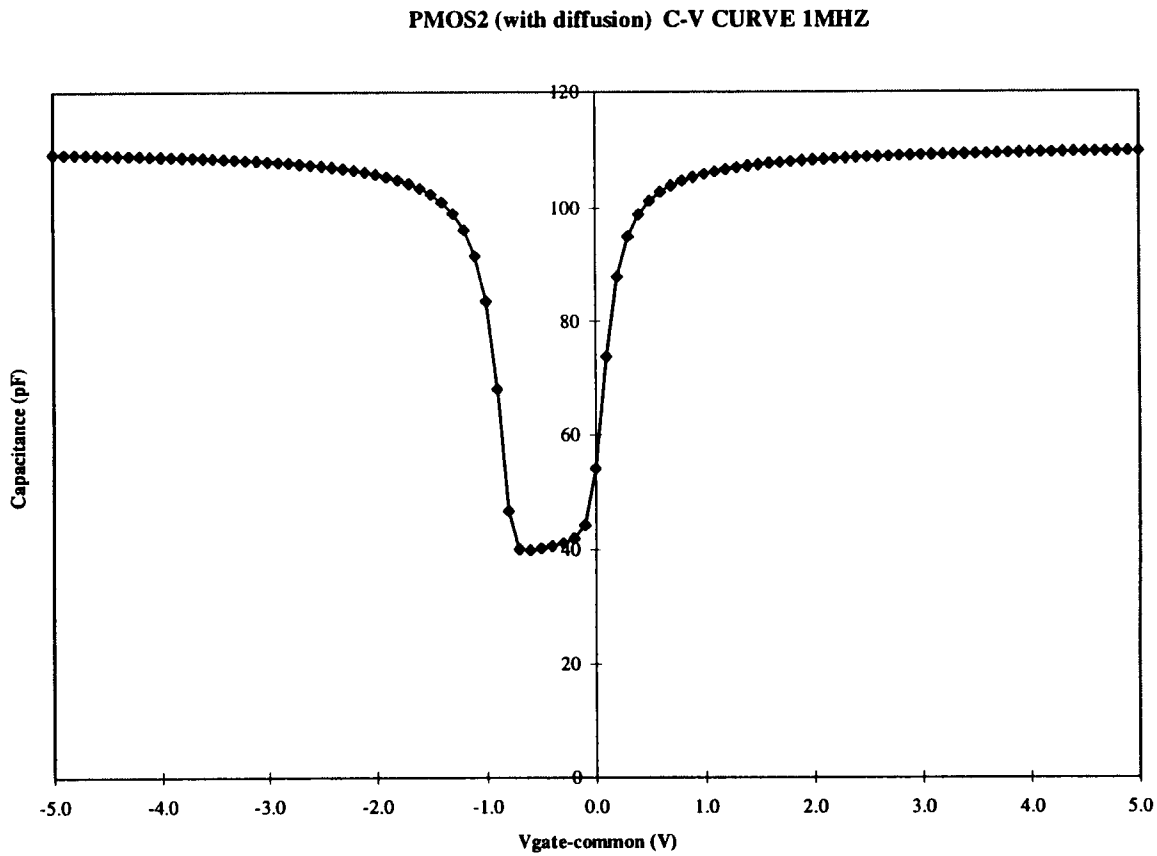


Figure 5-11. C-V characteristic curve for PMOS2 structure.

charge conditions including inversion. As theoretically predicted the capacitance values in inversion and accumulation are approximately equal and approach a peak value of 110 pF. Dividing once again by the total area of the device yields a density of 1.83 fF/μ^2 for the PMOS2 capacitor.

Although the PMOS1 and PMOS2 structures appear to be nearly identical (with respect to density) for positive gate biasing, further examination yields a much higher nonideal series resistance for the PMOS2 device. While giving measured capacitance values as a function of gate bias, the impedance analyzer also provides values for conductance G and dissipation factor D for the measurement. These values can then be converted using

$$R = \left(\frac{D^2}{1+D^2}\right)\left(\frac{1}{G}\right) \tag{5.1}$$

into a corresponding value for series resistance [33]. The graph of Figure 5-12 provide a comparison of the measured series resistance for both the PMOS1 and PMOS2 structures. While the peak series resistance of the PMOS1 is seen to be less than 30 Ω, the PMOS2 exhibits a peak value more than an order of magnitude larger. This increased series resistance exhibited by the PMOS2 device makes the PMOS1 capacitor the structure of choice if biasing within the high resistance region.

Combining the results of the capacitance measurement and the series resistance calculation provides the data necessary to arrive at a basic representative model to describe the high density capacitor. For operation in accumulation the basic model must include the poly-poly capacitance and series resistance of the polysilicon material

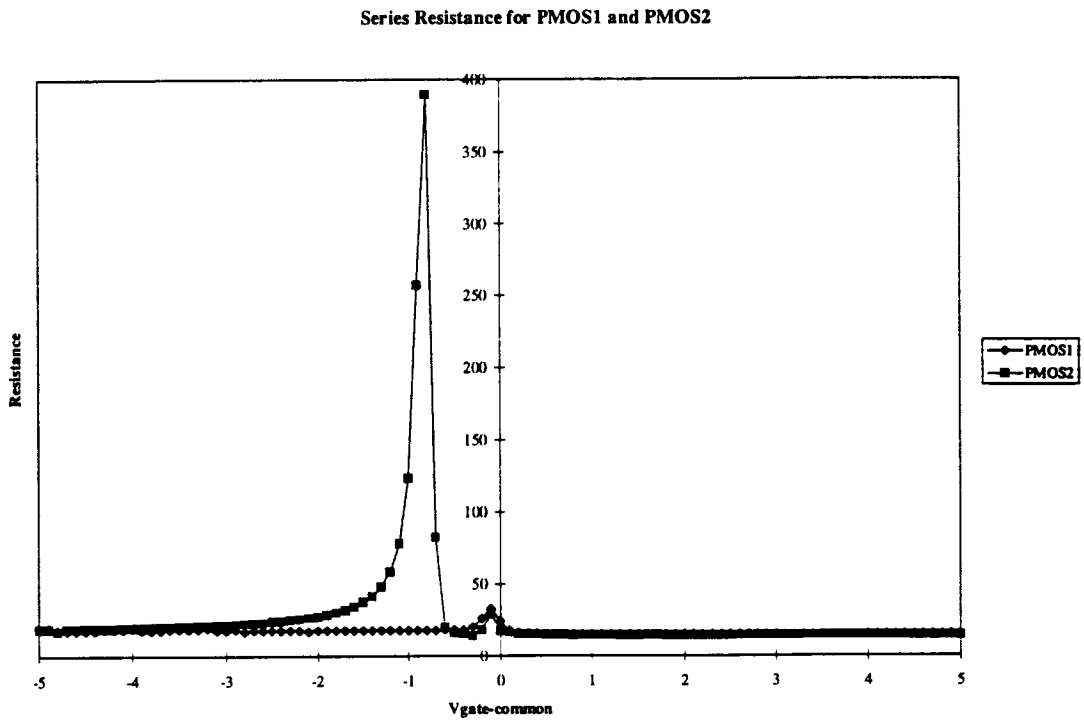


Figure 5-12. Measured series resistance for PMOS1 and PMOS2 structures.

as well as the poly-well capacitance and well series resistance. The representative model is illustrated in Figure 5-13. At a density of 0.5 fF/μ^2 the poly-poly structure contributes roughly 30 pF while the poly-well capacitor comprises the remaining 83 pF. Additionally, the series resistance associated with the poly is less than 10 Ω while the well resistance was seen to be approximately 26 Ω for PMOS1 and 390 Ω for PMOS2. As the channel becomes depleted of carriers, the much smaller depletion layer capacitance is placed in series with the network of Figure 5-13 and the resulting equivalent circuit becomes that of Figure 5-14.

Although the PMOS1 and PMOS2 devices are much larger than the needed 8 pF capacitor for the multiplicity discriminator, the measured density and series resistance results should apply for any size capacitor. Utilizing the density obtained for the PMOS1 structure, a capacitor of roughly 8 pF was created in an area of 85 μ x 166 μ. With this capacitance and an effective resistance R_Z of approximately 52 MΩ, the dominant pole becomes 380 Hz. It should be noted that every other aspect of the dc feedback loop remained unchanged from the circuit described in Chapter III.

5.3 Results

Modifications to the input differentiator coupled with the much larger hold capacitor increase the required discriminator length from 527 μ to roughly 670 μ. Although the increased circuit length is undesired, the improved stability accomplished through the implementation of an 8 pF capacitor outweighs the area constraints. Since the magnitude of the bias current has only slightly changed from that of the original

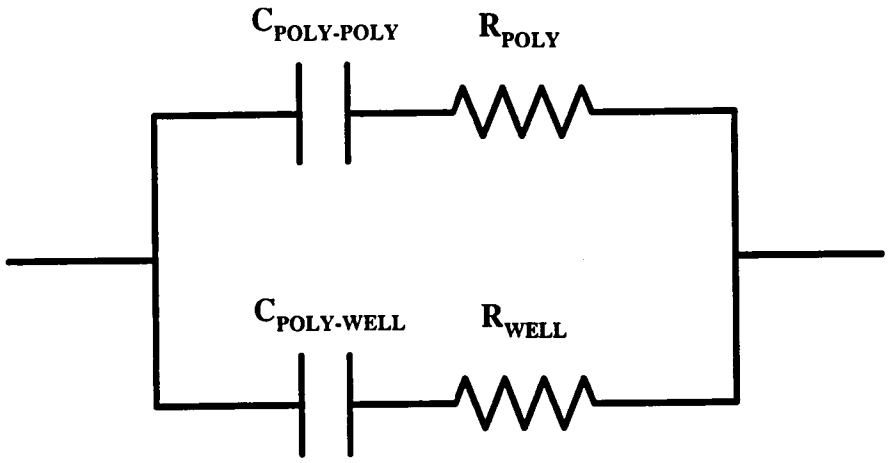


Figure 5-13. Equivalent model of given high density capacitor structure.

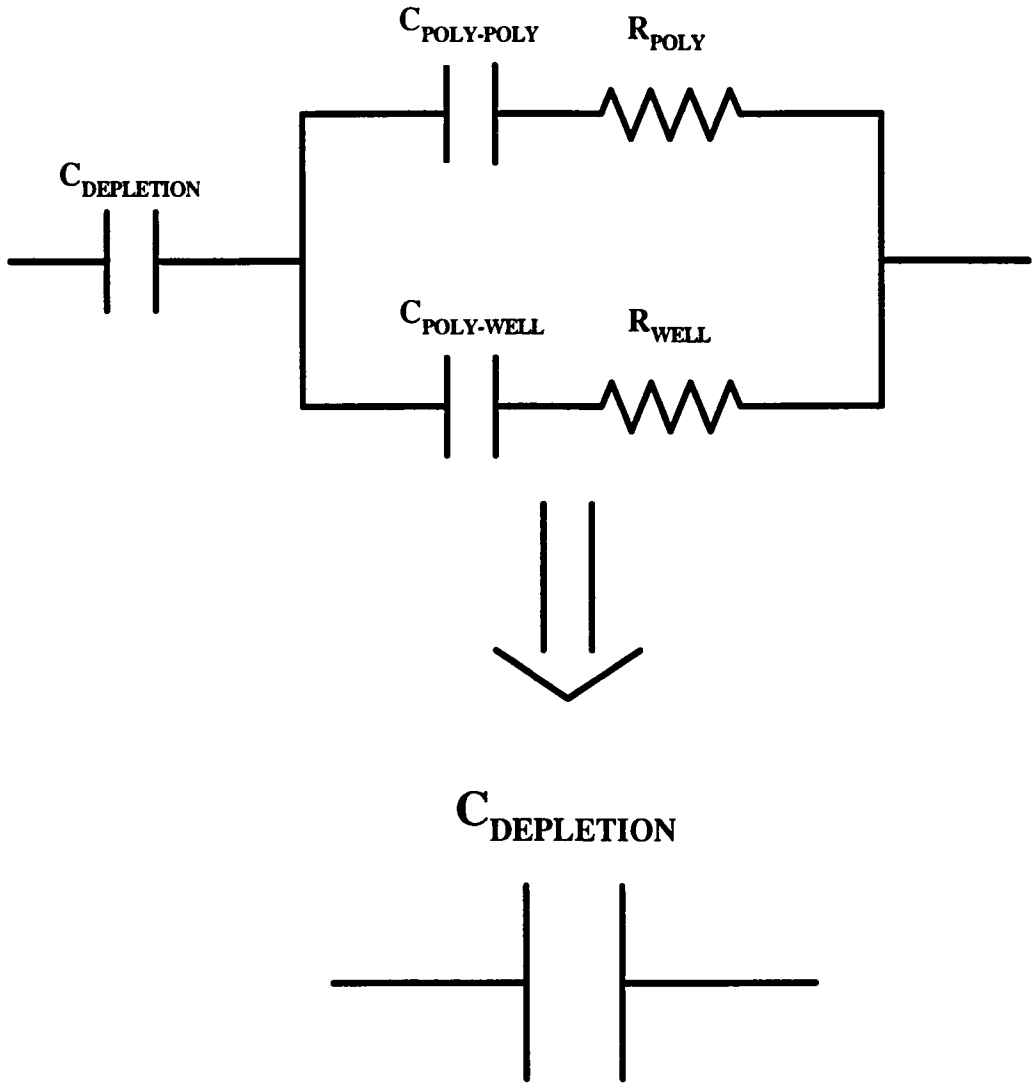


Figure 5-14. Equivalent model of high density capacitor in depletion.

design, power consumption remains roughly 500 μW/channel. While most performance characteristics of the discriminator remained approximately the same as those originally described, discriminator speed decreased considerably from 110 ns to nearly 160 ns for a 400 mV input. Such an increase in speed means that for large input signals the discriminator will not return to baseline before the next event occurs. For example, if the worst case conditions described in Chapter III of a maximum input followed by a minimum input occur, the output pulse will remain high such that the two individual pulses can not be distinguished. However, as seen by Figure 5-15 the discriminator output does return to baseline before the next event. In fact after numerous simulations of various input sequences it was determined that by introducing a fixed delay and then sampling the discriminator output every 100 ns, the correct output was always obtained. This may be seen more clearly by the timing diagram of Figure 5-16. In conclusion, the modifications discussed in this chapter should provide a discriminator with improved threshold matching, improved stability, adequate timing capabilities and increased adjustability at the cost of additional circuit length.

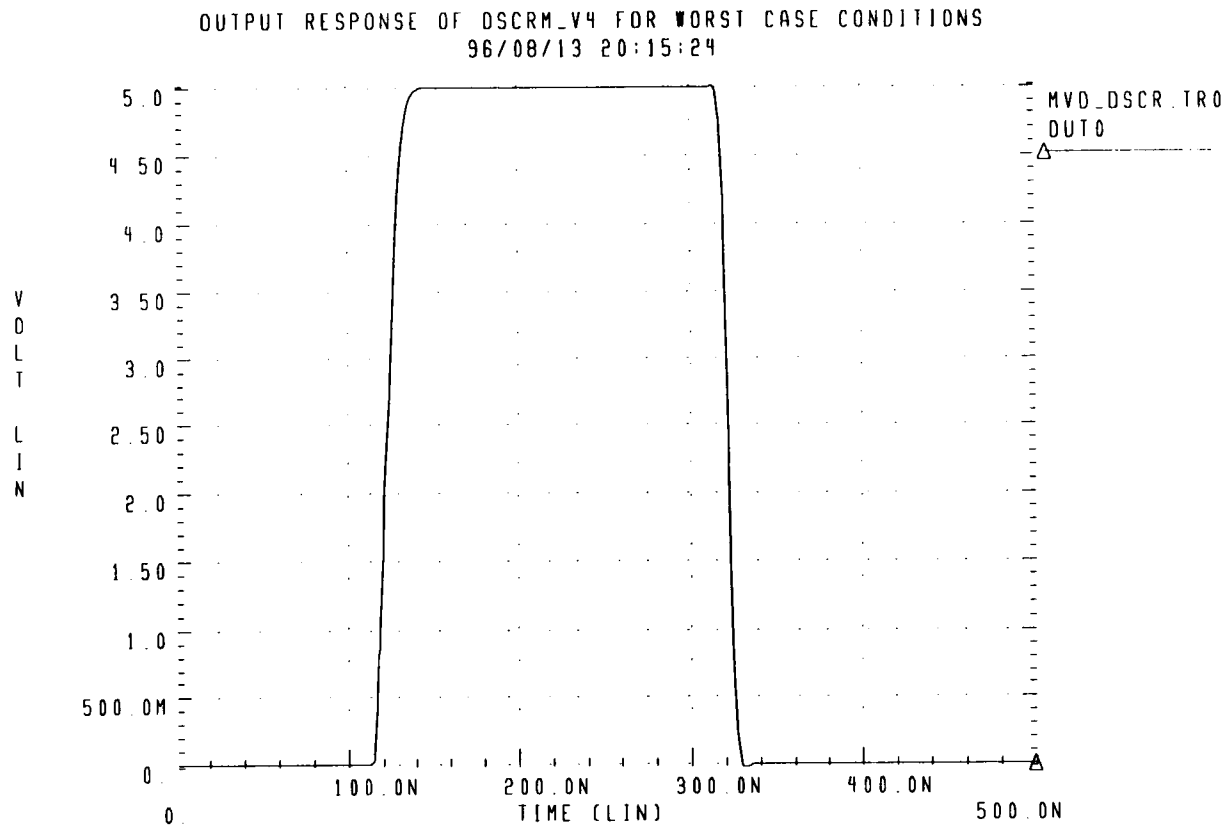


Figure 5-15. Output response of modified discriminator.

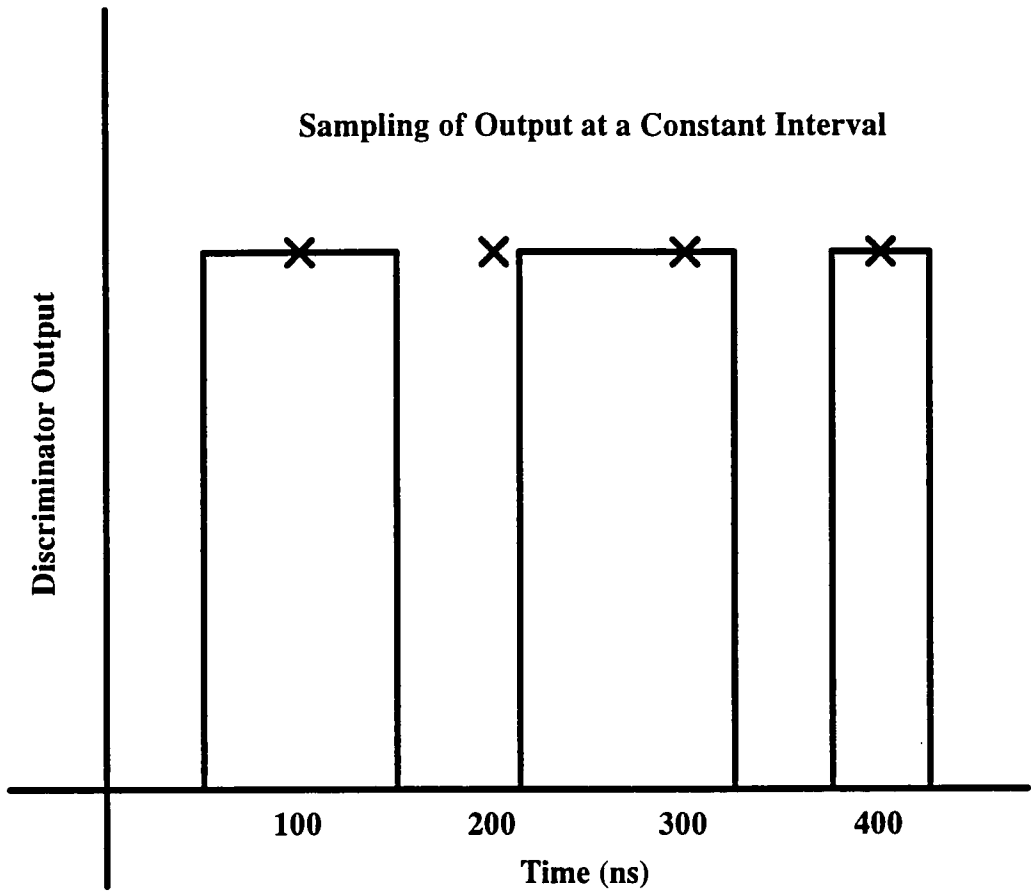


Figure 5-16. Sampling concept required to obtain an accurate number of triggered discriminators.

Chapter 6

Conclusions

A current output multiplicity discriminator for use in the FEE of the MVD has been designed and fabricated in the Orbit Semiconductor 1.2 μ CMOS nwell process. The primary goal of the discriminator is to provide event multiplicity data needed to establish a level 1 trigger which is indicative of an interesting physics event. By summing the current outputs of 256 discriminators located on one MCM the needed multiplicity information is provided. Implementing this function of multiplicity discriminatoion within the 34,000 channel MVD FEE structure placed many challenging and stringent requirements on the design. Issues such as power consumption, area, common threshold matching, small triggering threshold, speed and adjustability define the constraints of the design.

To evaluate these specifications, several variations of the same basic design topology were fabricated. Each topology contained an input differentiator, two gain stages with dc feedback, a threshold adjustment circuit and current switch. The slight differences focused on elements used to generate the dc feedback loop. To eliminate unwanted offset voltages the method of continuous dc feedback was selected over switched dc feedback and the ac coupling concept. Circuit stability relies on a low frequency dominant pole being established within the feedback loop. One version of

the discriminator (DSCRM2) utilized serpentine MOS transistors biased in the ohmic region to implement the needed resistance while another design (DSCRM_TST) used long channel devices in a "goal post" configuration to achieve the needed resistance. Independent evaluation of test devices having these geometries verified the operation of each long channel transistor. From this experimental evaluation it was determined that the serpentine long channel transistor had an effective channel length that was much less than the drawn length. This result was manifested by the higher drain current of the serpentine device over the "goal post" structure for the same drawn length. Modeling of these devices using a derived Level 2 model and existing Orbit BSIM and Level 3 models verified the high resistance value.

As implemented in 1.2 μ CMOS, one channel of multiplicity discriminator occupies an area of 85 μ by 530 μ and requires roughly 515 μW of power. Although triggering on inputs ranging from 0.25 MIP (20 mV) to 5 MIP (400 mV) is possible, worst case timing conditions of the maximum input followed by the minimal input on the subsequent beam crossing presents a problem. For the discriminator to provide multiplicity information with no deadtime, the ramping input signal from the charge sensitive preamplifier must be differentiated, amplified and triggered on with the resulting discriminator output returned to baseline within one cycle of the 105 ns system beam clock. Although this timing scenario was not met by the fabricated design, a method of sampling the output at a fixed interval proved to yield acceptable results.

Due to the extremely high channel count of the MVD, common discriminator threshold matching across a 32-channel die represents a stringent design goal. This goal implies that the 32 discriminators located on one chip be extremely well matched over all process variations. To meet this objective a scheme consisting of continuous dc feedback for offset elimination and a previously fabricated threshold adjustment differential to single ended circuit was used. The threshold adjustment circuit had exhibited mismatch of less than $\pm$ 3 mV in previous designs and was thought to be adequate for use in the multiplicity discriminator. However, measured results presented in Chapter IV showed a much higher degree of threshold mismatch. Since most of the circuit is surrounded by negative feedback designed to eliminate these types of variations, the source of the mismatch was determined to stem from bias current mismatch within the input differentiator. This being the case, slight modifications (presented in Chapter V) to the original design should drastically improve common threshold matching.

In addition to the discriminator design and experimental evaluation, prototype floating-gate capacitor structures were also fabricated and tested. The need to increase the hold capacitor within the dc feedback loop for improved circuit stability while still maintaining a minimal area design called for the use of a much higher density capacitor structure. Consisting of a double poly capacitor in parallel with a MOS capacitor, the floating-gate structure achieved a density nearly four times that of a double poly capacitor. Of the two versions evaluated the PMOS1 (without additional

diffusion) structure is highly preferred due to the much lower nonideal series resistance. A corresponding simple model of the capacitor was presented.

In conclusion, the multiplicity discriminator presented in this thesis should provide an adequate means of determining event multiplicity and distribution within the framework of the MVD FEE. Although speed and threshold matching characteristics of the tested circuits do not meet the desired goals, modifications presented in Chapter V should allow for improved performance. These changes require minimal increases with respect to area and power needs. Other nonideal effects such as the distortion created by substrate coupling between the discriminator and preamplifier appear to be acceptable provided the sampling of the preamplifier output is delayed in time. Additionally, when combined with a simplified Level 2 model for the long channel transistors, BSIM models provide an accurate representation of the actual performance of the multiplicity discriminator. It should be stressed again that the performance of the multiplicity discriminator depends on the constant temperature environment established within the MVD. Since many of the circuits are especially sensitive to temperature via mobility and threshold variations, a constant controlled temperature is required for successful results.

References

References

[1] Armstrong, Betty, "Components of the Standard Model of Fundamental Particles and Interactions", Lawrence Berkeley National Laboratory, Berkeley, CA, http://pdg.lbl.gov/cpep.html,1996.

[2] "The Superconducting Super Collider Project A Summary", Drell Panel Executive Report, http://jobs.ssc.gov/new/history/appendixa.html, 1996.

[3] "History of LHC", CERN, Geneva, Switzerland, http://delinfo.cern.ch/CERN/LHC/pgs/general/history.html, 1996.

[4] "Relativistic Heavy Ion Collider", Brookhaven National Laboratory, Long Island, NY, http:/www.rhic.bnl.gov, 1996.

[5] "Standard Model Summary", Lawrence Berkeley National Laboratory, Berkeley, CA, http://pdg.lbl.gov/cpep/mainchart, 1996.

[6] "Why Take the Next Step", Drell Panel Executive Report, Section I, http://gus.phy.vanderbilt.edu/~gabella/drell/sec1.html, 1996.

[7] "The Energy Frontier", Drell Panel Executive Report, Section IV, http://gus.phy.vanderbilt.edu/~gabella/drell/sec5.html, 1996.

[8] "United States Collaboration in the Large Hadron Collider", http://uscms.fnal.gov/uscms/announce/draft_us_lhc_doc.html, 1996.

[9] "ALICE - Purpose of the Experiment", Letter-of Intent for ALICE, htpp://www.cern.ch/ALICE/loi_abs.html, 1996.

[10] Kehoe, W. L., et al., PHENIX Conceptual Design Report. 29 Jan. 1993.

[11] Britton, C.L. et al, "Multiplicity Vertex Detector Electronics for Heavy Ion Detectors" Proceedings of the First Workshop on Electronics for LHC, Lisbon, Portugal, September 1995, pp. 288-292.

[12] Emery, M.S., et al., "A 11-bit Multi-Channel ADC for Use in the PHENIX Detector", To be Presented at the 1996 Nuclear Science Symposium, October 1996.

[13] Gray, P.R., Meyer, R.G., Analysis and Design of Analog Integrated Circuits, Third Edition, John Wiley & Sons, Inc., New York, 1993, Chapter 2.

[14] Allen, P.E., Holberg, D.R., CMOS Analog Circuit Design, Harcourt Brace Jovanovich, Fort Worth, 1987, Chapter 7.

[15] Kennedy, E.J., Semiconductor Devices and Circuits, (text in preparation), Chapter 7.

[16] Gray, P.R., Meyer, R.G., ibid., Chapter 1.

[17] Lakshmikumar, K.R., et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 6, December 1986.

[18] Allen, P.E., Holberg, D.R., ibid., Chapter 2.

[19] Simpson, M.L., et al., "A Monolithic, Constant-Fraction Discriminator Using Distributed R-C Delay Line Shaping", To be Published in IEEE Transactions on Nuclear Science, 1996.

[20] Kennedy, E.J., ibid., Chapter 5.

[21] Gray, P.R., Meyer, R.G., ibid., Chapter 7.

[22] Gray, P.R., Meyer, R.G., ibid., Chapter 3.

[23] Britton, C.L.,"Studies On High-Speed Analog Memories for Physics Experiments with Emphasis On Radiation Hardening", PhD. Dissertation, University of Tennessee, Knoxville., May 1995.

[24] Yang, E. S., Microelectronic Devices, McGraw-Hill, New York, 1988, Chapter 12.

[25] Kennedy, E.J., Operational Amplifier Circuits, Holt, Rhinehart and Winston, Inc., Fort Worth, 1988, Chapter 1.

[26] Buck, A., "Current Feedback Myths Debunked", Application Note OA-20, Comlinear Corporation, Fort Collins, Colorado, 1994.

[27] Gray, P.R., Meyer, R.G., ibid., Chapter 4.

[28] Gharpurey, R., Meyer, R.G., "Modeling and Analysis of Substrate Coupling in Integrated Circuits", IEEE Journal of Solid-State Circuits,Vol. SC-31, No. 3, March 1996.

[29] Su, D. K., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", IEEE Journal Solid State Circuits, Vol. 28, N0. 4, April 1993, pp. 420-430.

[30] Vladimirescu, A., Liu, S., "The Simulation of MOS Integrated Circuits Using Spice2", Memorandum No. UCB/ERL M80/7, University of California, Berkeley, CA.

[31] HSPICE User's Manual: Elements and Models. Meta-Software, Inc., 1992.

[32] Schroder, D. K., Advanced MOS Devices, Chapter 1, pp. 3-9, Addison-Wesley Publishing Company Inc., 1987.

[33] HP4192A Users Manual, Hewlett-Packard, Ltd., 1985.

Appendices

Appendix 1

12.1.2 DEVICE SPECS: 1.2 MICRON 2 POLY 2 METAL N-WELL AND P-WELL CMOS

	N-Channel			P-Channel			
	Min	Typ	Max	Min	Typ	Max	
VTE (VBS=0) 30x1.2u	0.6	0.8	1.1	-1.1	-0.8	-0.6	(Volts)
BVDSS (VBS=0) 30x1.2u	10	15			-14	-8	(Volts)
IDS @ VGS=5v,VDS=5v,L=1.2u	0.17	0.24	0.29	-0.14	-0.11	-0.08	(mA/micron)
K Prime (lnr) 30x30u (uCox/2) VD=0.1v VG=2.3v	30	33	36	7.5	9.5	11.5	(uA/V**2)
Leff @ Ldrawn=1.2u	0.8	0.9	1.0	1.0	1.1	1.2	(microns)
Oxide Encroachment/side	0.48	0.52	0.56	0.48	0.52	0.56	(microns)
BE (short channel) 1.2u = delta VT (VBS=0,2)	0.4	0.6	0.8	0.2	0.35	0.5	(Volts)
BE (long channel) 30u = delta VT (VBS=0,2)	0.5	0.7	0.9	0.3	0.45	0.6	(Volts)
VTF Poly	10	16			-13	-10	(Volts)
Diffusion Resistance	25	40	50	50	70	100	(ohm/sq)
Poly Resistance	15	24	30	15	25	30	(ohm/sq)
Substrate Resistance	1.5	2.0	2.5	1.4	1.6	1.8	(Kohms/sq)
Substrate Cs	1E16	1.5E16	2E16	6E15	7E15	8E15	(/cm3)
Diffusion Junction	0.25	0.3	0.35	0.25	0.3	0.45	(microns)
Well Junction	3.5	4.0	4.5	3.5	4.0	4.5	(microns)
Sidewall Spacer		0.2			0.2		(microns)
Contact Resistance(1.4x1.4u)		75			150		(ohms)
ViaResistance(1.4x1.4u)		75			75		(milliohms)
Junction Breakdown Voltage		15			15		(volts)
N-Well to P- Substrate Breakdown			45				(volts)
Metal1 Sheet Resistance	50	55	60				(mohm/sq)
Metal2 Sheet Resistance	22	28	33				(mohm/sq)
VTE poly2		1.55			-1.6		(volts)

Appendix 2

```
*********************************************************************
**$$ below is the HSPICE optimized BSIM1 PMOS model:

*.model cMOSp Pmos(LEVEL=13 TOXM=22.5m VDDM=6,LD=0.23U, WD=0.43U
.model cMOSp Pmos(LEVEL=13 capop=4 TOXM=22.5m VDDM=6,LD=0.1U, WD=0.43U
+ NSUB=1E16 PB=0.7298 MJ=0.4022 CJ=451U PJW=0.863 MJSW=0.3646
+ CJSW=445.4P JS=610N JSW=0.2N FC=0.5 CGSO=108P CGDO=108P CGBO=625P
+ TREF=25 xpart=1 RSH=370)
* KF=?. MUST specify NLEV=1, or really perhaps NLEV=3 with AF=0.8 would
* be a better fit to both linear and sat. regions?? If use NLEV=3, then
* the value of KF is different than the KF value for NLEV=1.
+ af=0.5 kf=4.2e-31 nlev=1 acm=3 hdif=1.2u
*+ muz=184.84
+ muz=300
+ vfb=-0.2192   lvfb=0.069    WVFB=.1241
+ phi0=0.7692   LPHI=0.0598   WPHI=0
+ MUS=247.7     LMUS=31.66    WMUS=-21.15
+ u00=0.1468    LU0=0.2623    WU0=-0.0585
+ k1=0.4806     LK1=2.167m    WK1=0.0336
+ k2=0.01617    LK2=0.0551    WK2=-1.282m
+ ETA0=-9.4m    Leta=0.0408   WETA=0
+ U1=0.2659     LU1=-0.138    WU1=0
+ X2E=-0.792m   LX2E=-1.545m  WX2E=-0.9233m
+ X3E=1.183m    LX3E=-2.16m   WX3E=-4.061m
+ X2MZ=8.366    LX2MZ=13.83   WX2MZ=1.822
+ X2MS=14.81    LX2MS=1.524   WX2MS=0.801
+ X3MS=1.0      LX3MS=0       WX3MS=-0.0526
+ x2u0=-0.2914m LX2U0=0.0691  WX2U0=0.5875m
+ X2U1=-0.1138m LX2U1=3.39m   WX2U1=0
+ X3U1=0.02579  LX3U1=-0.01815 WX3U1=0
+ N0=1.317      LN0=0.143     WN0=0
+ NB=63.24m     LNB=-97.29m   WNB=-0.4176
+ ND0=0         LND=0         WND=0


*********************************************************************
*$$ below is the HSPICE nmos BSIM1 model, with the values obtained from
*$$ the same optimized parameters of PSPICE above, 'BUT' results are not
*$$ necessarily the same as with PSPICE??? (1/25/95 DATA)

*.model cMOSn Nmos(LEVEL=13 TOXm=22.5E-3 VDDM=7 LD=0.235u WD=0.104u
.model cMOSn Nmos(LEVEL=13 capop=4 TOXm=22.5E-3 VDDM=7 LD=0.1u WD=0.104u
+ NSUB=1E16 PB=0.749 MJ=0.4158 CJ=554.2U PJW=0.9958 MJSW=0.4017
+ CJSW=371.9P JS=0.25U JSW=75P FC=0.5 CGSO=310P CGDO=310P
+ CGBO=340P  TREF=25 XPART=1 RSH=350 )
+ af=.5 kf=2.3e-29 nlev=1 acm=3 hdif=1.2u
*+ MUZ=550
+ MUZ=650
*+ VFB=-0.8708  LVFB=13.14m    WVFB=-0.1
+ VFB=-0.6708  LVFB=13.14m    WVFB=-0.1
+ PHI=0.7665    LPHI=28.62m    WPHI=0
+ MUS=559.9     LMUS=44.18     WMUS=-20
+ U00=99.48m    LU0=0.2747     WU0=-0.0506
```

```
+ K1=1.172    LK1=-33.63m    WK1=0.2099
+ K2=62.18m   LK2=40.96m     WK2=0.020
+ ETA0=-66.8u LETA=10.76m    WETA=0.0158
+ U1=0.06     LU1=0          WU1=0
+ X2E=-0.8775m LX2E=-4.17m   WX2E=-1.246m
+ X3E=0.957m  LX3E=-1.76m    WX3E=-4.8m
+ X2MZ=6.419  LX2MZ=17.17    WX2MZ=3
+ X2MS=-0.8378 LX2MS=22.12   WX2MS=3
+ X3MS=-0.3   LX3MS=0        WX3MS=0
+ X2U0=-7.547m LX2U0=33.22m  WX2U0=6.912m
+ X2U1=0.017m LX2U1=-0.5m    WX2U1=0
+ X3U1=0.26   LX3U1=0        WX3U1=0
+ N0=1.649    LN0=0.0251     WN0=-0.544
+ NB=74.1m    LNB=19.93m     WNB=-0.501
+ ND0=0       LND=0          WND=0


**********************************************************************
*Orbit Semi. 1.2u level3 models with WIC=3 weak-inversion corrections.
*     FAST VALUES
*     for use with HSPICE version H92b.
*     Orbit Manual section 12.1 dated July 1992.
*     C. L. Britton
*     Revisions - - - - - - - - - - - - - - - - - - - - - - >
*
.model cmosn nmos LEVEL=3 CAPOP=9 HDIF=1.2U ACM=3
+ UO=521.3 VTO=.82  NFS=.6E12 TPG=1 TOX=21E-9 NSUB=5.7E16
+ VMAX=49500 XJ=300E-9 LD=278E-9
+ DELTA=5.28  xqc=0.4 wd=98e-9
+ PB=.8 MJ=435E-3 CJ=556E-6 PJW=.9958 MJSW=.344
+ CJSW=371.9E-12 JS=10E-6 CGSO=310E-12 CGDO=310E-12 CGBO=340E-12 FC=.5
+ RSH=349.7
+ wic=3 n0=1.7
+ theta=0.005 eta=.01 kappa=.2


.model cmosp pmos LEVEL=3 CAPOP=9 HDIF=1.2U ACM=3
+ UO=167.5 VTO=-1.1 NFS=.65E12 TPG=-1 TOX=21E-9 NSUB=3.7E16
+ VMAX=200000 XJ=300E-9 LD=146E-9
+ DELTA=2.15 wd=283e-9 xqc=0.4
+ PB=.8 MJ=404E-3 CJ=448.6E-6 PJW=.8626 MJSW=.334
+ CJSW=445.4E-12 JS=10E-6 CGSO=108E-12 CGDO=108E-12 CGBO=625E-12 FC=.5
+ XPART=1 RSH=418.2
+ WIC=3 N0=1.1
+ theta=.005 eta=.03 kappa=10
```

Vita

Randall Scott Smith was born in Knoxville, Tennessee on October 30, 1971. He attended Heritage High School located in Maryville, Tennessee where he graduated with honors in June, 1989. After graduating from high school he entered the University of Tennessee, Knoxville to pursue a degree in Electrical and Computer Engineering. In December, 1994 he graduated Magna Cum Laude with a Bachelor of Science degree in Electrical Engineering. While an undergraduate Randall participated in numerous organizations and honor societies including the cooperative education program, IEEE, Tau Beta Pi and Phi Kappa Phi. In May, 1994 he began working with the Monolithic Systems Development Group in the Instrumentation and Controls Division at the Oak Ridge National Laboratory (ORNL). At the encouragement of ORNL staff members he entered graduate school at the University of Tennessee in January, 1995 under the guidelines of the joint UT-ORNL graduate program in Mixed Signal-VLSI design. He graduated with a Master of Science with a major in Electrical Engineering in December, 1996. In addition to analog circuit design, Randall enjoys nature and nearly all forms of athletics. He is currently employed by IBM in Raleigh, North Carolina were he is an analog circuit designer involved in transceiver communications development.