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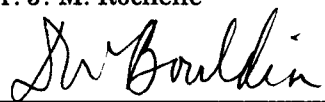
I am submitting herewith a thesis written by Charles Lanier Britton, Jr. entitled "Studies On High-Speed Analog Memories for Physics Experiments with Emphasis On Radiation Hardening". I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

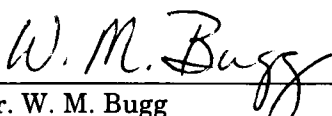

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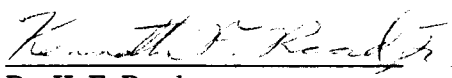
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**Studies On High-Speed Analog Memories for
Physics Experiments with Emphasis On
Radiation Hardening**

A Dissertation

Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Charles Lanier Britton, Jr.

May 1995

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DEDICATION

This dissertation is dedicated to my wife Carol, my children Lanie, Mariruth, and Katie, my parents Charles and Mary, and Carol's parents Jack and Ruth Davis without whose support the work presented here would have been most impossible.

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I would like to thank the many people that contributed to the work represented by this dissertation. Dr. E. J. Kennedy, my major professor, was the major source of guidance and sanity during the hectic period of data taking and writing. The committee, composed of Dr. J. M. Rochelle, Dr. T. V. Blalock, Dr. D. W. Bouldin, Dr. W. M. Bugg, and Dr. K. F. Read, were not only helpful, but very supportive with guidance in both academics and general advice.

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ABSTRACT

The use of analog memory units (AMUs) for fast storage in large physics experiments has grown dramatically in the last five years. As more experiments require improvements in measurement precision, the need for precise, fast, small and low-priced temporary data storage has increased to where almost every major experiment has at least one subsystem with imbedded analog memory. Along with the increased usage has come increased expectations of the performance of such memories. The newer high-energy experiments such as the now-defunct Superconducting Super Collider (SSC) and the Large Hadron Collider at CERN in Switzerland require memories that are resistant to ionizing radiation and heavy particles.

This thesis presents the development and testing of such memories. Two different memory topologies as well as two different readout amplifiers were designed, fabricated in a radiation-hard CMOS process (Harris AVLSI-RA), and tested. Combinations of these circuits were tested for linearity, pedestal variation, cell droop (leakage), and nearest neighbor interaction. The circuits were tested after exposure to 0-, 1-, and 5MRad of gamma radiation. The results indicated that the CMOS process was radiation-hard to at least 5MRad ionizing radiation. The Voltage-Write-Voltage-Read (VWVR) topology exhibited better linearity, pedestal performance, and less effect on nearest neighbors than the Voltage-Write-Charge-Read (VWCR) topology.

A method of pedestal correction used with a memory fabricated in a non-rad-hard process was also tested that indicated address-dependent pedestal noise (so called 'pattern' noise) could be reduced by employing a real-time correction.

Radiation levels of up to 75KRad in a standard process had no effect on the correction method.

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I. INTRODUCTION

A. Scope of the dissertation

This dissertation is the result of approximately two years of planning, development, design, and testing. Prior to the work outlined here, there had been no published work in the area of analog random-access memories for high data rate, high-radiation environments. Analog memories, as we shall see, had been used in physics experiments, but there had never been an experiment of the class offered by the Superconducting Super Collider (SSC).

This dissertation presents the design and measurement of the memory development program undertaken to study the possibility of memory usage in the SSC environment. Because the goal of this development was a finished test circuit and because the cost of fabrication was so high (approximately \$90,000), the development went directly to a complete circuit, not small test sub-circuits. The individual circuit components are therefore buried within the overall circuit. Most testing is thus aimed at system-level tests to infer the performance of individual sub-circuits. Consequently, much testing must be performed to adequately investigate these circuits. This dissertation primarily consists of the testing of the unique integrated circuits presented. The mathematics presented is to describe the development of the individual components of the memory, but the heart of this document is indeed the extensive testing of these circuits. The testing took two people four months to complete and generated thousands of sheets of data, a very small portion of which is presented here.

B. The use of analog memory in physics experiments

The high-energy and particle physics communities have been performing larger and larger experiments over the course of time. Early experiments utilized small accelerators and simple detection electronics [REV1]. As the need for higher and higher kinetic energies became evident, the accelerators became larger and the detectors became more complex. As the search for the more exotic particles progressed, the need for an increased number of samples arose in order to improve the statistics of the observed phenomena. The fundamental tradeoff was, for more samples, increase the time of data taking, or increase the rate at which data was taken, or both. Increased rates implied faster detector systems which began to require the fastest electronics. Because most of the data taken in a physics experiment is uninteresting, the event triggering became most important. With many events occurring, ideally one would like to wait some number of microseconds to let the various sub-detectors in a system contribute information so that a decision can be made as to whether a particular event is of interest. This implies use of a method of storing the event information for some period while the trigger system is deciding on the data validity. Ideally one would like to take data, much of which is analog in nature, convert it to digital form, keep what is interesting and throw away the rest. To do this for modern experiments would require a tremendous amount of processing power in the form of high-speed analog to digital conversion. Because power dissipation is also of major concern, this becomes impractical in many applications. One approach that has been successfully used is that of analog storage. This allows the analog information to be stored for some period of time while a trigger decision is being made. The interesting data is then converted to digital form, and the

uninteresting data is simply discarded. Power for conversion to digital form is used only on interesting data.

The analog memories have features that cause problems if not addressed [WALK1, SAK1]. In addition, for very high-energy experiments, the radiation field generated by the experiment can cause damage to the analog memories thus reducing their accuracy. This dissertation addresses some problems associated with radiation damage to these memories and the methods for overcoming the problems.

C. Brief background of the experiments

1. Gammas, Electrons, and Muons (GEM)

The GEM detector was a large particle physics detector for use at the Superconducting Super Collider (SSC). The primary purpose of the detector was central to the existence of the SSC: to study high transverse momentum phenomena resulting from the collision every 16ns of the counter-rotating beams of protons [TDR1]. It was expected that study of the phenomena would lead to possible confirmation or refinement of proposed physics theories attempting to explain the origin of mass.

A cutaway drawing of the detector in perspective is shown [TDR1] in Fig. 1-1. As in many experiments, the detector was actually a combination of several smaller, specialized subsystems, each a detector within itself. The detector consisted of a magnet to bend the path of charged particles, a central tracker to find the origin and paths of the particle-producing interactions, a calorimeter to measure the total energy of events, and muon chambers to measure muon activity. All this surrounded the beam pipe in which the interactions originated. The entire detector was to be 38m long and 24m in diameter.

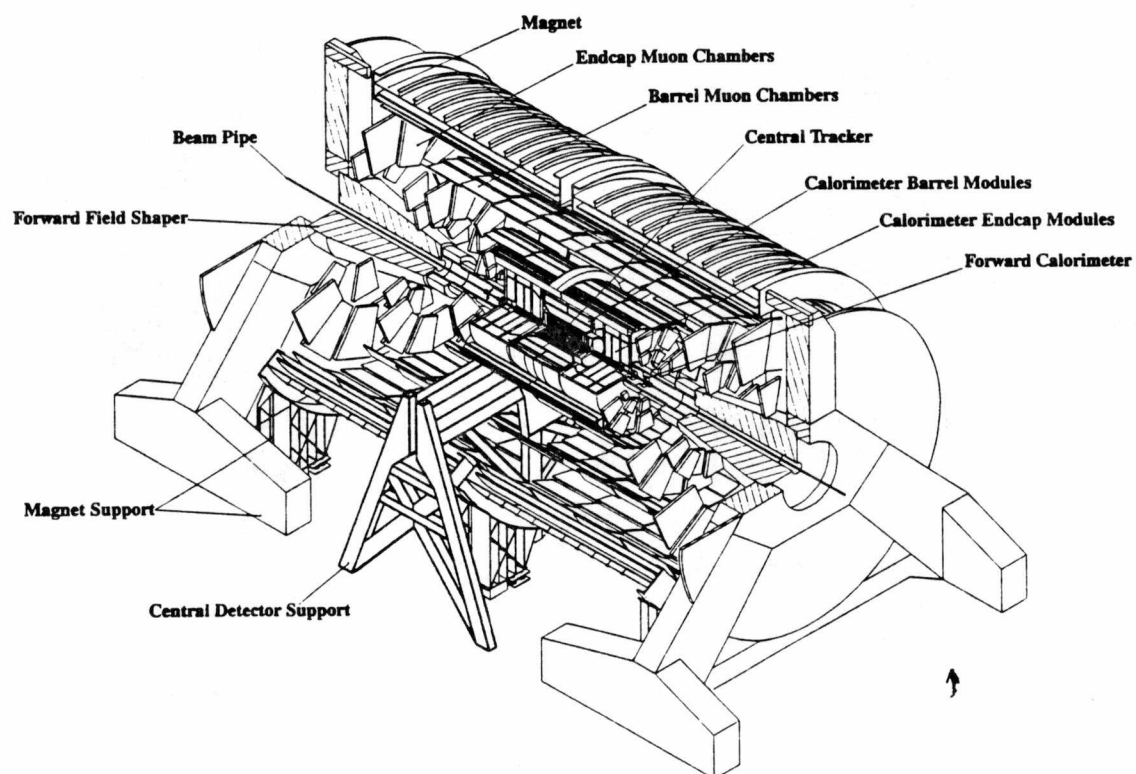


Figure 1-1. Perspective view of the GEM detector.

2. PHENIX detector

The PHENIX detector is one of two planned large experiments at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory. The purpose of the experiment is best explained by the following quote from the PHENIX 1993 Conceptual Design Report [CDR1]:

"The primary goals of the PHENIX experiment at the Relativistic Heavy Ion Collider (RHIC) are to detect a new phase of matter, the quark-gluon plasma (QGP), and to measure its properties. During the past few years, many experimental probes of the QGP have been suggested. The PHENIX experiment measures many of the best potential signatures to see if any or all of these physics variables show simultaneous anomalies due to the formation of the QGP."

In concept, the PHENIX detector looks quite similar to the GEM detector. The detector is composed of several subsystems which essentially do tracking and particle identification. The major difference is that there are more detector subsystems in PHENIX and they look for some different types of particles. The beams are also different: they are made up of heavy ions such as sulfur and gold in addition to protons. The collisions also are designed for 112ns intervals instead of 16ns. A perspective cutaway of the detector is shown in **Fig. 1-2**.

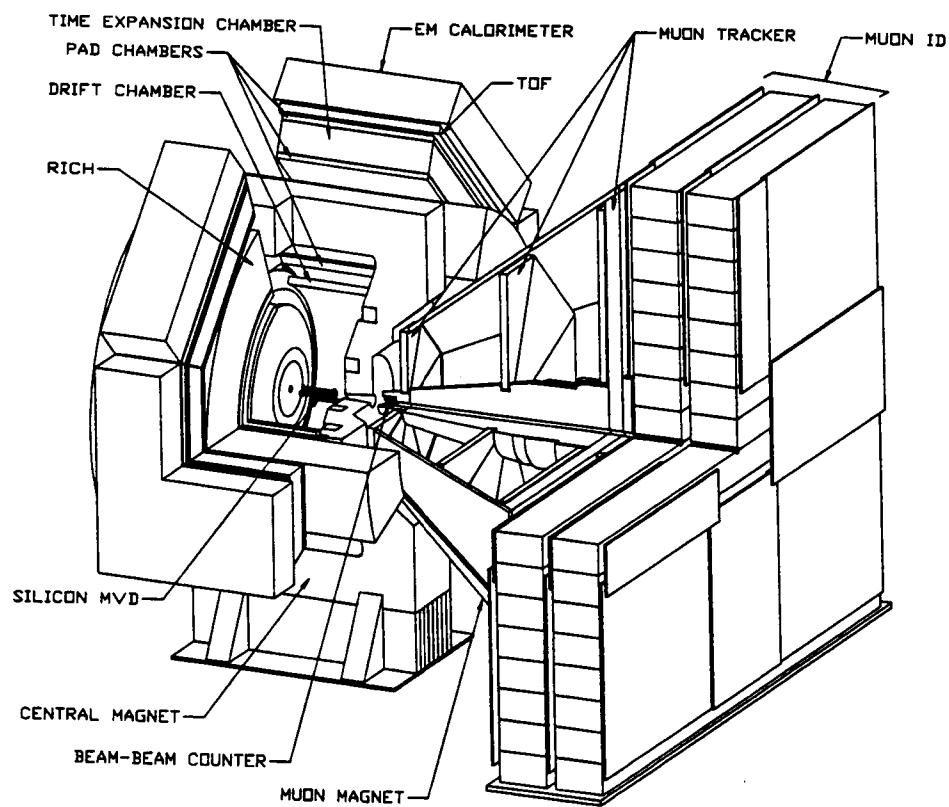


Figure 1-2. Perspective view of the PHENIX detector.

II. ANALOG MEMORY OVERVIEW

A. Reasons for using analog memory

The use of analog memories in physics experiments is a relatively recent trend [WAD1]. The earliest memories date from the mid 1970s and were made with discrete components. It was not until the mid 1980s that integrated circuit technology was seriously applied to the fabrication of these memories. The earliest applications are referenced here but will not be discussed because the focus of this thesis is on integrated circuit implementations [CENT, BROOK, FARR, BERN, SHAP].

There are two primary reasons for using an analog memory in a system. The first is for deadtime-less operation of the data acquisition system. The term deadtime-less implies that a system can continually acquire events at the actual rate the events occur, not missing any events. The rate at which the data are processed may be much lower, but, from the point of view of the detector, the data collection system does not 'go dead' and miss collection of any events. The analog memory makes this possible by storing the events as they happen and allowing the data reduction system (analog-digital converter or ADC) to convert the desired stored analog data to digital data at a slower rate thus sparsifying the data and throwing away uninteresting events. Obviously, if all data are interesting and the ADC can not convert as fast as the data is coming in, this approach does not work and some data will be lost.

The second reason for using an analog memory is to introduce delay in a system. In some fixed-target experiments, the events are occurring at the detector but the signals that form the trigger (indicating a 'good' event) can be delayed by a few hundred nanoseconds due to propagation delay through cables

and electronics. In the past 80m cables [WA80] have been employed between the detectors and the input electronics to delay the signals' arrival with respect to the trigger. For a few channels, this may be acceptable. For many thousands of channels, this becomes prohibitive in both size and expense. Analog memories have recently been used [WA98] to replace the cables in an experiment. This approach requires the memory to be continually sampling until a trigger is received. At that time, the sampling stops and the desired values stored in the memory are converted for use. This is not a deadtime-less system (it is commonly referred to as a 'stop-and-read' system) but a system in which the memory is a true time-delay element.

B. Types of analog memories

There are many analog memory implementations for various applications being used or proposed for use in the literature [NI, FR, ASP, HO, TED]. These circuits are being used throughout the world. Many of them presently have quite similar architectures, the most typical of which is presented in Fig. 2-1. Typically, the circuit will have a preamplifier which is connected to the detector element. The output of the preamplifier is then connected to the input of the memory. The preamplifier itself may have gain and filtering to improve the noise and temporal characteristics of the event. The preamplifier may also employ some form of correlated sampling [BUTTL1] to improve noise or dynamic range.

The preamplifier typically precedes the memory which can actually vary in cell length from one element [AMP1] to 256 or more elements [SAK1] per

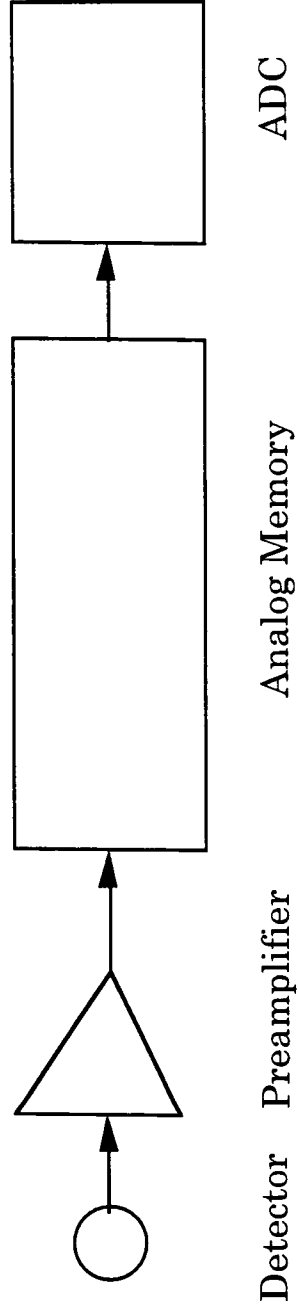


Figure 2-1. Typical system utilizing an analog memory.

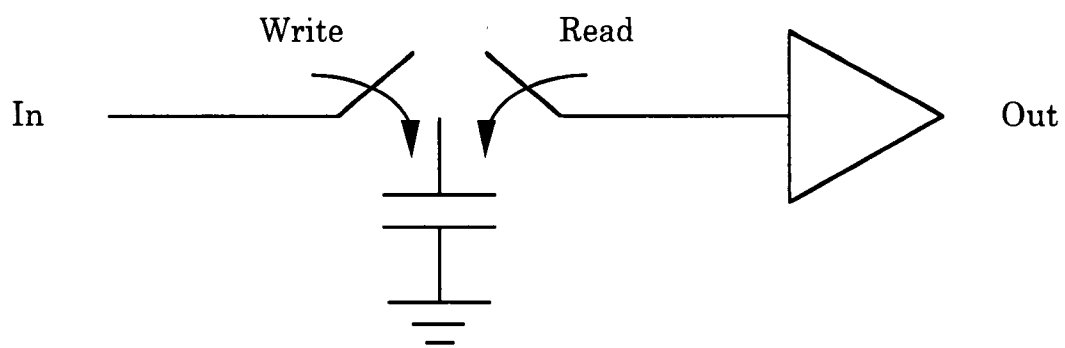
channel. There have been several different memory topologies developed, but most of them can be classified as one of three topologies: voltage-write-voltage-read (VWVR), voltage-write-charge-read (VWCR), and charge-write-voltage-read (CWVR). The basic operation of the topologies will be presented, but technical details on those of interest (VWVR, VWCR) will be presented in Chapter IV.

1. VWVR

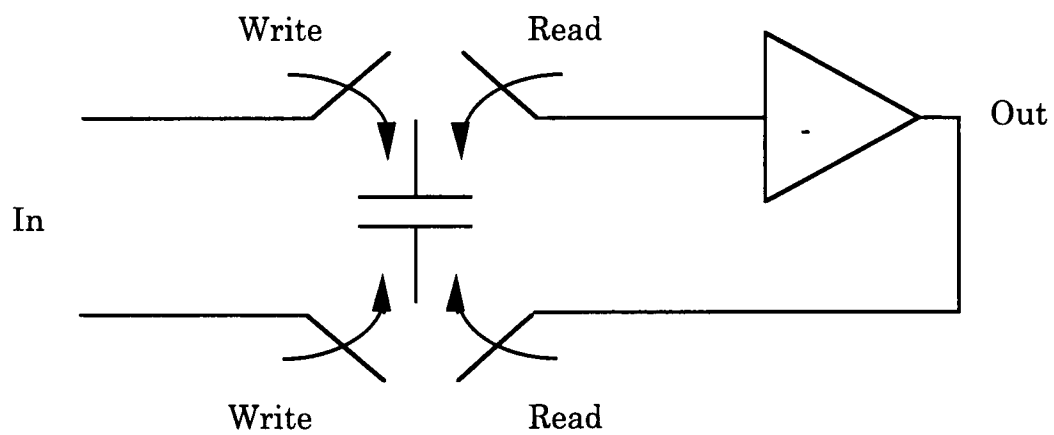
This topology is presented in **Fig. 2-2** and is widely used because of its basic transfer function. The voltage that is written is read without a conversion to or from charge. The most basic implementation is shown in **Fig. 2-2(a)**. The voltage is stored on the capacitor when switch 1 is closed and is read when switch 2 is closed. The implementation in **Fig. 2-2(b)** is preferred due to its insensitivity to stray capacitances [SAK1, SAK2, ANG1, APV1, BRIT1, GARA] but some earlier circuits did use the topology of **Fig. 2-2(a)** [WALK1]. The topology of **Fig. 2-2(c)** has been used to implement high-frequency sampling (900MHz) for signals with bandwidths of the order of 20MHz [HAL1].

2. VWCR

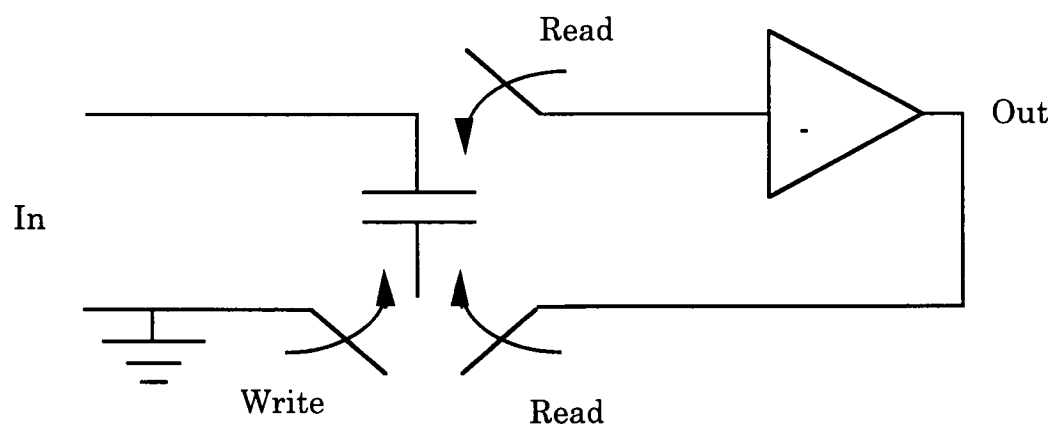
This topology, shown in **Fig. 2-3**, stores the voltage impressed across the sampling capacitor during writing. To read the memory, one connects the sampling capacitor to the inverting input of the readout amplifier. The amplifier is connected such that a capacitor is placed between the output and inverting input. The feedback action of the amplifier transfers the stored charge from the sampling capacitor to the feedback capacitor. The resultant output is given as



(a)



(b)



(c)

Figure 2-2. Various implementations of VWVR topology.

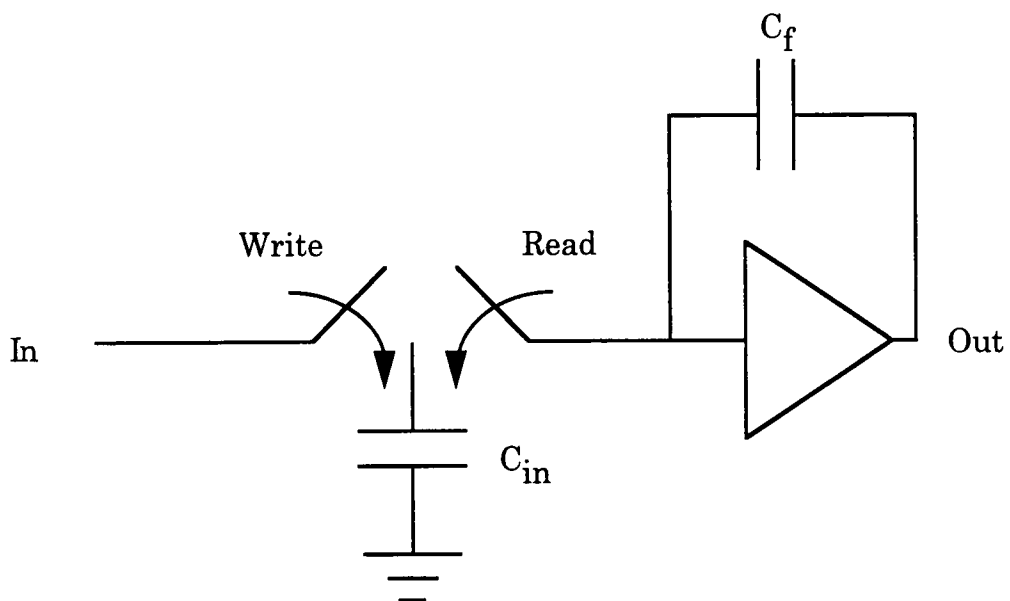


Figure 2-3. Implementation of VWCR topology.

$$V_{out} = V_{in}(C_{in}/C_f) \quad (2.1)$$

where V_{out} and V_{in} are the output and input voltages respectively. This has been used in at least two implementations [MOSCH, BRIT1].

3. CWVR

This topology has been gaining in popularity in recent years. The general topology is shown in Fig. 2-4. The input amplifier is used as an integrator for the sampling capacitors. When readout is desired, the sampling capacitor is connected across the readout amplifier as in the VWVR topology thus reading the voltage stored on the capacitor. The two applications of this approach have been to either make a preamplifier whose output is current which then feeds the memory [MUND, CAMP, BOR], or make the input amplifier itself the charge-sensitive preamplifier [ZIM1]. The gain variations of this topology are similar to that of the VWCR topology because a charge is involved instead of a voltage. In the case of the CWVR, the charge is input on the read.

C. ADC multiplicity

The memory designs employ either one ADC per channel [WA98] or multiplexer to allow a single ADC to sequentially convert data from a group of memory channels, typically 8-16 channels [TDR1, MOSCH]. The types of ADCs used are pipeline [ANG1], Wilkinson [WA98], and flash [TDR1].

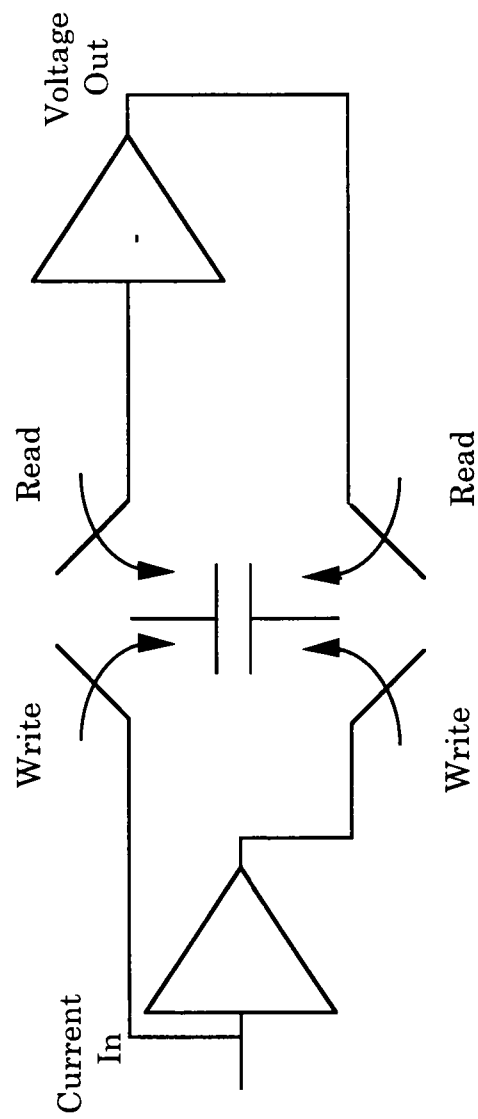


Figure 2-4. Implementation of CWVR topology.

III. EFFECTS OF RADIATION ON CMOS

When particles emitted from a radioactive source pass through a CMOS transistor, the device is inevitably left with damage of some form. If the damage is minor, the device can usually still operate with some degradation in performance. If the damage is great, the performance may be so badly degraded as to render the device useless. This chapter will discuss the mechanisms by which the actual damage occurs and the resultant effects upon the performance of the devices.

A. Radiation types and interactions

The intentional collision of known types of particles is the essence of a collider experiment. It is from these collisions that other species of particles are generated and are 'thrown into' the detector. The three types of particles that are commonly encountered in experiments can be categorized as follows: [SROUR1, MA1]

1. Photons

Photons are typically called x-rays if they have energies below 10KeV, and gamma rays if they are above 10KeV. Photons, having no rest mass and carrying no charge, interact with matter through the photoelectric effect, Compton scattering, and pair production. The result of interest is that a valence electron is freed from its atom thus creating an electron-hole pair.

2. Charged particles

Charged particles can be electrons, protons, alphas, or various species of

heavy ion. The sources can from naturally occurring radio nuclides emitting alphas to ion implanting machines emitting heavy ions. They interact with matter primarily through Rutherford scattering which can generate either an electron-hole pair as in photon interactions or through actually displacing constituent atoms from their lattice positions. Nuclear interactions can also occur for some particles such as proton capture by a nucleus followed by alpha particle emission.

3. Neutrons

Neutrons are large, heavy, uncharged particles that interact through elastic and inelastic scattering, and transmutation reactions. Elastic scattering involves a neutron with energy great enough to dislodge an atom from its lattice position and send the atom into other atoms which can be ionized or displaced. Inelastic scattering involves the atomic capture of a neutron by the nucleus of a now excited atom followed by the emission of the neutron at a lower energy. Transmutation involves atomic capture of a neutron by the nucleus followed by the emission of a proton or alpha particle thus resulting in a different atomic number for the atom.

The scope of this dissertation has been limited to irradiation of parts by photons, in particular gammas having energies of 1.17MeV and 1.33MeV (Co^{60}). The expected radiation dose is 2-3MRad of ionizing radiation (a mixture of charged particles and gammas) in the region of the detector. Testing with a charged particle source is all but impossible since the sources themselves are typically accelerators whereas a gamma source is readily available Co^{60} . The response to neutron dose is also difficult to test because the available neutron sources (reactors) have a different spectrum of neutron energies than the

colliders. The Harris AVLSI-RA process was rated to be hard to 10^{15} neutrons/cm², a factor of two greater than the expected fluence. The remaining discussion will therefore concentrate on the effects of gamma radiation, i.e., ionization.

B. Effects of ionization

The primary effect of ionization is quite simple. Valence electrons are excited and removed from the atoms around which they orbit. The end results of this effect can, on the other hand, be quite complicated. The situation is presented schematically in **Fig. 3-1 [EJK1, SROUR2, MA2]**. The biasing in the case shown is for the gate more positive than the substrate (this would be typical for an NMOS transistor). In this case the electron-hole pair is generated by an incident photon. In a very small percentage of the cases, the electron and hole will recombine immediately [YOSH1], but in the majority of the cases, the electrons are swept toward the gate and the holes are swept toward the Si/SiO₂ interface. The electrons are swept to the gate essentially instantaneously. The mobility of electrons at room temperature is approximately 20 cm²/V-sec while the mobility of holes is approximately 2×10^{-5} cm²/V-sec, a ratio of 10^6 [SROUR3]. Even at the low temperature of 4K, it has been found that the electrons are swept out of a 760nm gate oxide in less than 1μs [OTH1]. In essence, electron trapping is of no practical consequence.

The holes migrate towards the Si/SiO₂ interface and are either trapped in the bulk of the oxide or drift toward the interface. Those that are trapped in the

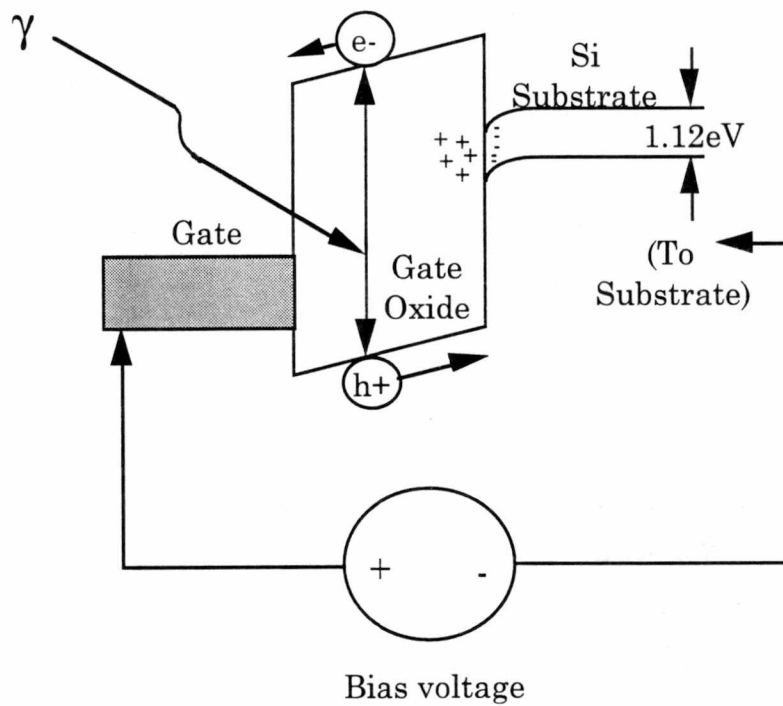
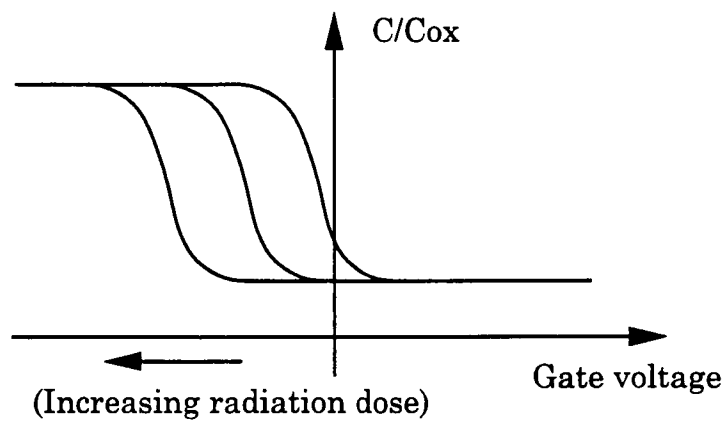


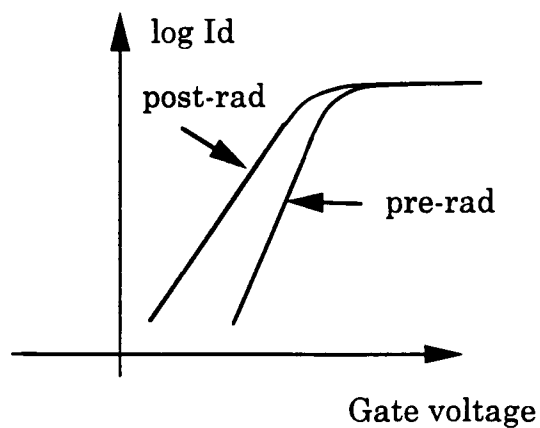
Figure 3-1. Schematic representation of electron-hole generation for positive bias due to ionizing radiation.

bulk of the oxide (away from the interface) act to simply bias the capacitance-voltage (C-V) curves in such a way as to cause a shift [SROUR5] as shown in **Fig. 3-2(a)** (C-V curves are a plot of the capacitance of a device versus some controlling voltage, in this case, the gate). This is, in effect, a threshold voltage shift due to the trapped charge. Traps that are close to the interface (in the order of 2-3nm) are termed "border traps" [FLEET1, MA3] and can exchange charge with the silicon substrate via either tunneling or thermally activated processes. The interface traps affect the C-V curves differently than those holes trapped further from the interface. The traps increase with increasing gate bias and tend to exhibit more effect closer to strong inversion and less at weak inversion [YOSH1] as shown in **Fig. 3-2(b)**. Radiation also induces bond-breaking of hydrogen-bearing impurities in the oxide. The resultant H and OH ions also act as trapping sites [YOSH1].

The overall effect of the traps is to shift the threshold voltage V_t of the devices being irradiated. The general effect is shown in **Fig. 3-3 [EJK]**. The NMOS devices (**Fig. 3-3(a)**) exhibit a negative threshold shift due primarily to holes trapped in the bulk of the oxide. At "low" dosages, low being a term relative to the process, the effect of oxide traps dominates and the V_t decreases. At some dose, the interface traps begin to compensate for the oxide traps and the V_t can actually rise and go more positive than the pre-radiation value [MA4]. Ultimately the oxide traps may again dominate and the threshold voltage would continue to drop. This scenario is bias dependent and will be different for transistors on the same substrate with different bias conditions. The PMOS device shift is shown in **Fig. 3-3(b)**. Everything said concerning the NMOS devices applies to the PMOS except that, because of the reversed electric fields,

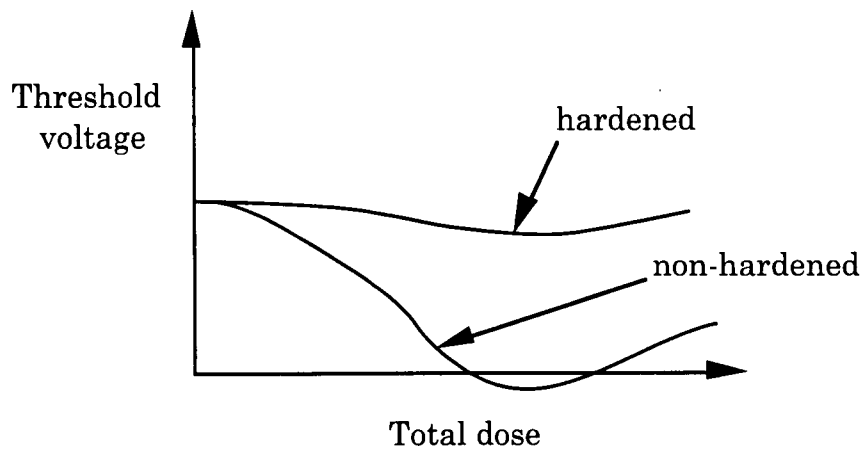


(a) Capacitance-voltage curve shift vs. dose.

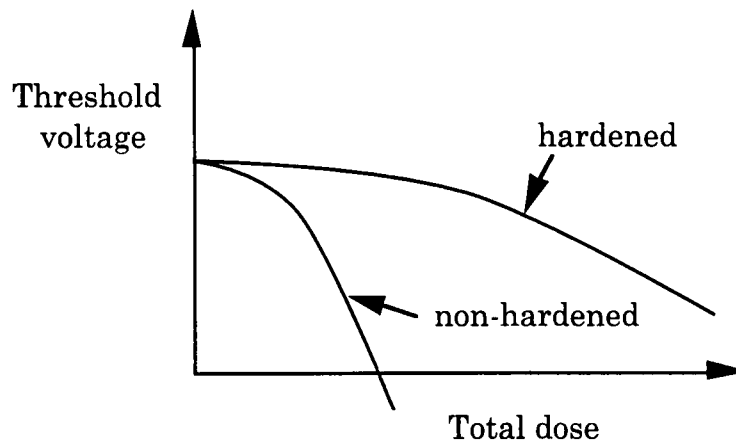


(b) Current-voltage (I-V) curves for pre- and post-radiation.

Figure 3-2. Transistor operating curves for pre- and post-radiation.



**(a) NMOS threshold voltage
vs. dose.**



**(b) PMOS threshold voltage
vs. dose.**

**Figure 3-3. Device threshold voltages
vs. dose.**

the PMOS interface traps exhibit less of an effect [YOSH1]. Electrons, with their higher mobility, do not create interface traps as readily as holes. Consequently, the V_t compensating effect seen in the NMOS devices at higher doses does not exist. The V_t shift is due almost entirely to bulk hole traps.

The bias condition has an important but not always consistent effect upon radiation damaged devices. Ma and Dressendorfer [MA5] found that devices biased OFF experience greater effects than devices biased ON. Yoshii, on the other hand, found that PMOS devices when OFF showed little if any effects of radiation while ON devices showed a great deal of oxide trap-induced shifting and little interface trap-induced shifting [YOSH1]. NMOS devices showed much worse damage effects when ON than when OFF. Obviously, exact bias conditions and processing plays a most important part in actual performance and sweeping generalizations are not possible. There have been measurements made that indicate dose rate also effects the device hardness [MA6]. The number of interface traps appears to be lower at low doses thus resulting in a smaller negative or even positive shift for NMOS devices.

Another area of performance that is degraded is the channel mobility. The mobility has a direct influence on the transistor transconductance and therefore a direct impact on the available transistor gain. The cause of the degradation appears to be the radiation-induced interface traps [MA7] and does not, at least to a first order, appear to be dependent on the oxide traps.

Thus far we have considered only the effects of radiation on the gate oxide. The number of oxide traps is proportional to T_{ox}^n where T_{ox} is the oxide thickness and n is an exponent with value between 2 and 3 [YOSH1]. The field oxides are typically much thicker (10x or greater) than the gate oxides which would make them much more susceptible to oxide traps. The n-well underneath a

metal line, for example, could become inverted due to the voltage on the metal line because of a large negative shift in the V_t of the field oxide transistor composed of the nwell, field oxide, and metal trace (gate). This could cause a loss of isolation between transistors within the nwell resulting in a large amount of leakage between devices or between the drain and source of a single device.

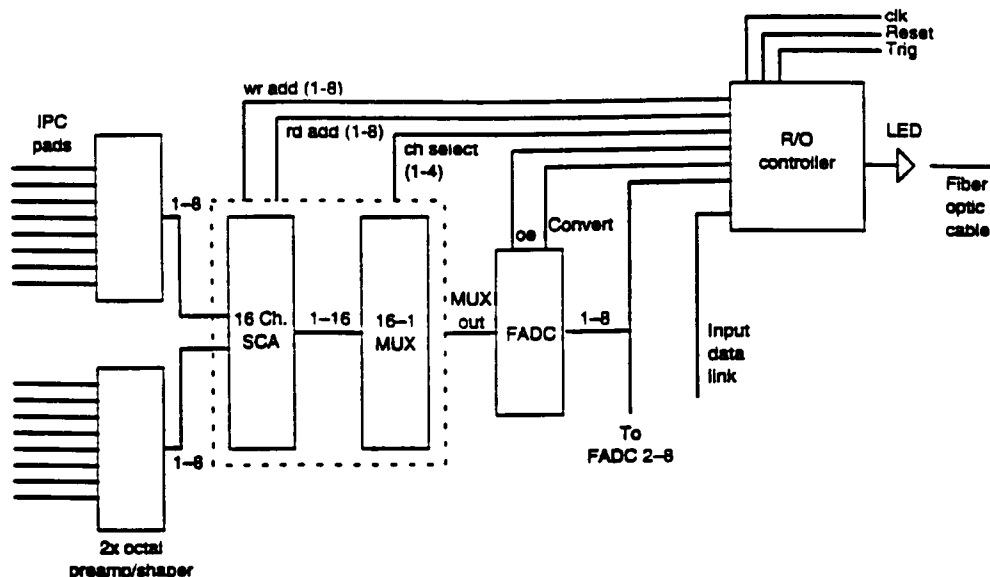
Noise is another parameter that is degraded by radiation. The channel noise is a function of transconductance (g_m) which is also a function of the channel mobility. The interface states cause a decrease in channel mobility and therefore increase the channel noise [VAND1]. Of equal or greater concern in MOS design is the effect of $1/f$ or flicker noise. There is evidence that the $1/f$ noise performance of a MOS device may be a good nondestructive indicator of radiation hardness [VAND1, FLEET1] as there is some correlation between the $1/f$ noise and the interface states. The correlation is weak, but present. This basic observation has also lead to the conclusion that process steps which impart radiation hardness also can result in lower noise devices.

IV. GEM ANALOG MEMORY DESIGN PHILOSOPHY

The design of this memory was undertaken to fulfill the requirements of the Interpolating Pad Chamber (IPC) subsystem of the GEM Central Tracker [TDR1]. It was decided early in the planning stages of the project that geometrical interpolation would be quite suitable for the operation of the IPC. Geometrical interpolation is a method by which three physically adjacent detector elements are taken for any given event and the relative signal contribution of each of the three elements are mathematically weighted in a predetermined fashion to result in a precise location of the event of interest. This required a charge-sensitive preamplifier (CSP) for collecting the charge induced on the pads from the wires due to an event. The analog memory sampled and stored the output from the CSP every 16ns and held the information until either the voltages due to a given event in the memory were read out and digitized, or written over by a subsequent event.

The candidate process was the Harris AVLSI-RA radiation-hard CMOS process. This process was chosen because of the availability of high-density two-plate capacitors. Three processes were considered, but this was the only with capacitors.

The requirements, shown in **Fig. 4-1 [TDR2]**, of a CSP, an analog memory unit (AMU), a multiplexer, and flash ADC obviously led to an early desire for a CMOS process that could implement the CSP, AMU, and multiplexer, and survive the harsh radiation environment present in the region of the IPC over the projected 10 year running life of the GEM detector. CMOS was an obvious choice since bipolar or GaAs processes were not suitable for analog memories due to the



Notes:

1. **SCA** is the Switched Capacitor Array (Analog Memory).
2. **MUX** is a 16x1 multiplexer used to route the 16 Analog memory channels into a single ADC.
3. **FADC** is a 25MHz Flash ADC that digitizes the analog memory output.
4. **R/O Controller** is a readout controller that addresses the memory, controls the MUX and the FADC. It is the "traffic cop" of the system.

Figure 4-1. Proposed Interpolating Pad Chamber (IPC) Electronics Architecture.

lack of adequate switches, the lack of choice of processes, and the generally expensive nature of the processes. It was not known, however, if a preamplifier suitable for the large detector capacitances could be built in CMOS. The main advantage of building the CSP and the AMU in the same process was primarily cost: it would be less expensive to share prototype fabrication costs between the two developments than pay for each individually if, for example, a bipolar process were chosen for the CSP and CMOS was chosen for the AMU.

There were several reasons for the chosen topology, which is shown in **Fig. 4-2**. There had been little if any work performed on rad-hard analog memories. It was unclear if any processes would work satisfactorily for the application of storing analog voltages for several tens of microseconds without significant deviation due to the effects of leakage currents. Irradiation generally produces an increase in p-n junction leakage currents which would add to or subtract from the stored voltage on the sampling capacitor. There was also a desire to minimize the chances of nonfunctional silicon due to a design flaw that replicated throughout blocks that were used in many places in the circuit, primarily because a single prototype fabrication run of five wafers was approximately \$90,000. It was for this reason that each of the two memories designed included several differences in pipeline topology and addressing schemes, i.e., no two pipes are exactly alike. Some of the features of the memories include:

- * Two different lengths of capacitor cell switches
- * Two different operational amplifier (readout) topologies
- * Interdigitated or sectional decoding

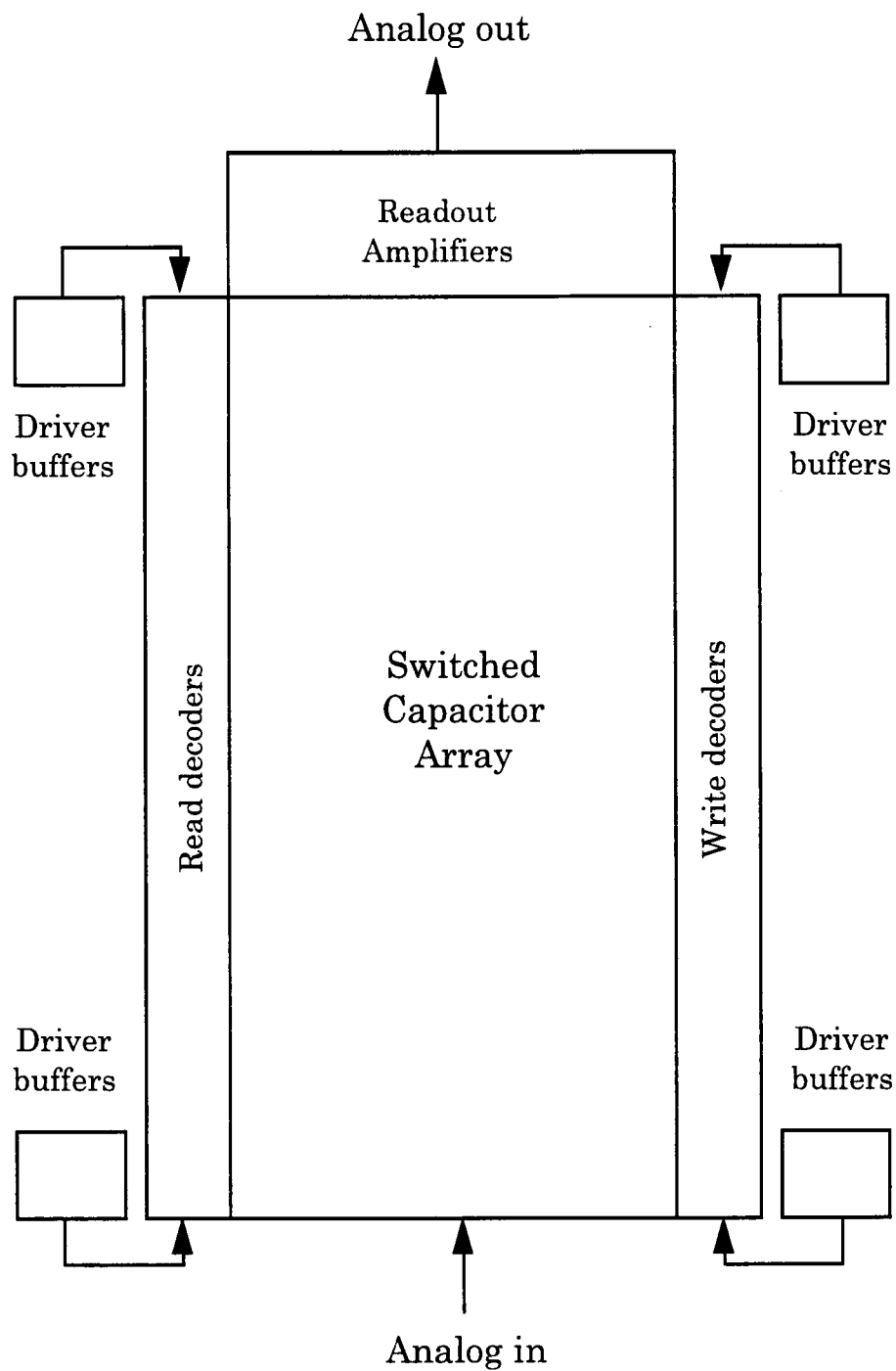


Figure 4-2. Layout topology for GEM memories.

- * Simple static address decoders
- * 8 pipes x 128 cells/pipe ($\sim 2.4\mu\text{s}$ deep pipes)
- * Approximately rail-to-rail input and output.

The design philosophy of the memories will now be explained.

A. GEM Experimental needs

1. Linearity

From the basic detector resolution requirements, it was determined that the integral non-linearity (INL) required for the analog memory be on order 0.5% or better for the semi-Gaussian pulse output from the pad preamplifier. This was due primarily to the inherent measurement accuracy of the IPC concept being approximately 1% [TDR1]. It was desired that the INL be as good as possible for the pre-radiation condition because the linearity would probably get worse as the chip received its predicted radiation dose.

The non-linearity was due to several effects. They are:

a. Switch non-linearities The basic memory cell, shown in Fig. 4-3, is actually a non-linear resistor in series with a relatively linear capacitor. The non-linearity is primarily due to the modulation of the channel on-resistance as a function of both input voltage and output voltage. The channel resistance is typically low as the input is close to the power-supply rails and peaks somewhere towards the midpoint voltage with one or two peaks, depending upon the relative sizing of the switches as shown in Fig. 4-4. This will be further discussed later in this document.

b. Pedestal variations. The voltage stored on the capacitor, because of the presence of the CMOS switches, will have some uncertainty

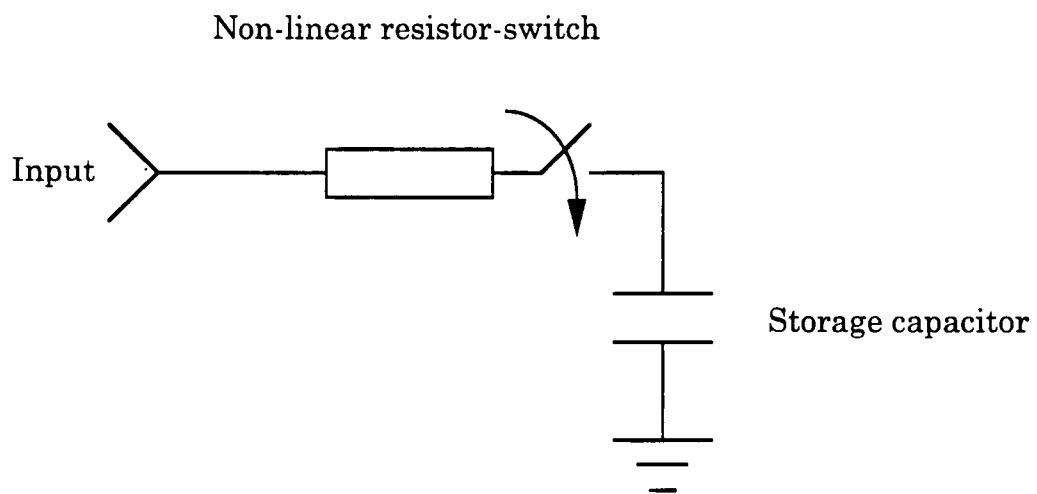
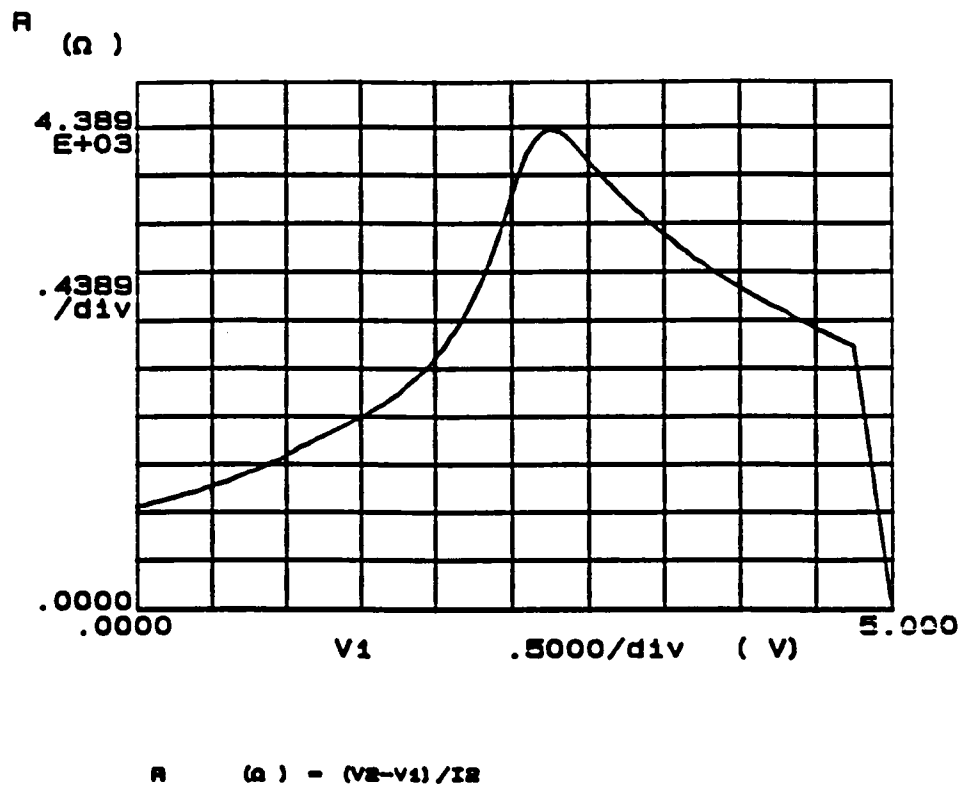


Figure 4-3. Basic memory cell.



Note: Data taken with the HP4145B Semiconductor Parameter Analyzer.

Figure 4-4. CMOS complementary switch resistance vs. input voltage.

associated with the turn-off of the devices due to injected charge. Because no two cells are identical, the injected charge will be slightly different from cell to cell. The cell to cell variations are called pedestal variation and are typically repeatable for a given input voltage. The pedestal variations in the memory were to be corrected by storing a pedestal table offline for later subtraction. If a subtraction of the pedestal from a measured channel is performed, any difference in the measured and actual pedestals will be manifested as a non-linearity. The goal was to have an rms pedestal variation of not more than 5mV. This would be approximately 0.1% rms of full scale for a 5V full scale.

c. kT/C noise During charging of a cell by an input signal, the switches are closed and thus present a low impedance between the input source and the capacitor. The switch resistance generates noise like any other resistor. For the purposes of noise calculations, the sampling system of **Fig. 4-3** can be represented [TVB1] as shown in **Fig. 4-5**. The $n\delta(t)$ term is the autocorrelation of a resistive white noise source with $n=4kT/R$ and $h(t)$ is the impulse response of the RC filter network of **Fig. 4-3**. We assume that the switch is open prior to time $t=t_0$ and after time $t=t_1$. The mean-square noise can then be calculated by

$$\overline{x^2(t_1)} = 2 \int_{t_0}^{t_1} h(v) \left[\int_{t_0}^v h(u) \delta(u-v) du \right] dv \quad (4.1)$$

The impulse response of the RC network of **Fig. 4-3** can be shown to be

$$h(t) = \frac{1}{\tau} e^{-\frac{t}{\tau}} \quad (4.2)$$

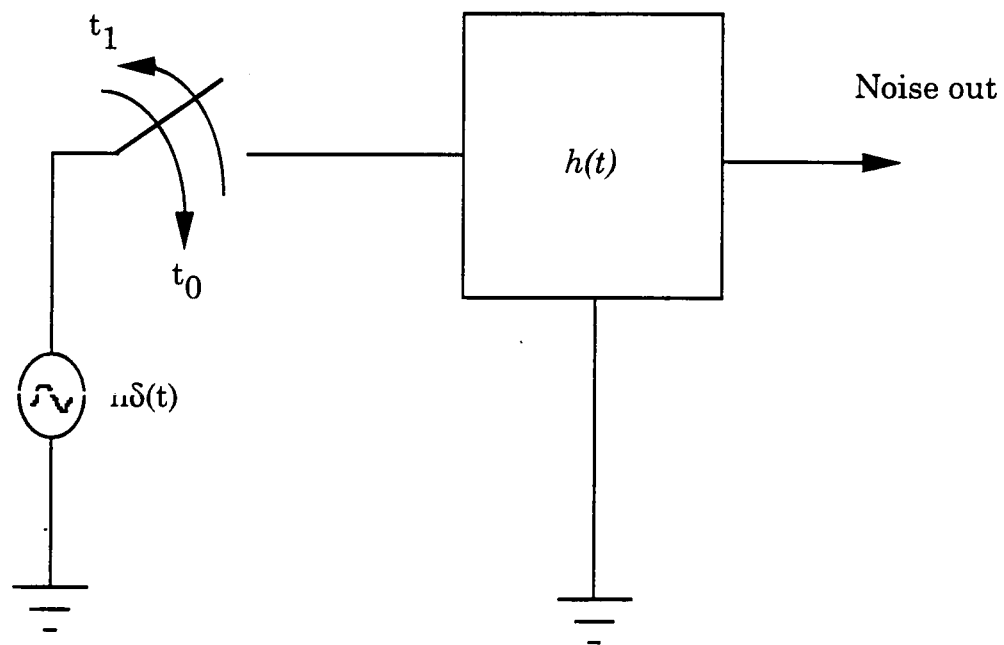


Figure 4-5. System with white noise switched at input.

where $\tau = RC$. Because the impulse function of the noise 'sifts' the right-hand side of the integral, and because we only want the noise spectrum for positive time, the integral can be reduced to

$$\overline{x^2(t_1)} = 2kT \int_{t_0}^{t_1} [h(v)]^2 dv \quad (4.3)$$

For $t_0=0$, this becomes

$$\overline{x^2(t_1)} = \frac{2kTR}{\tau^2} \int_0^{t_1} e^{-\frac{2v}{\tau}} dv \quad (4.4)$$

which can be evaluated to

$$\overline{x^2(t_1)} = \frac{kT}{C} \left(1 - e^{-\frac{2t_1}{\tau}} \right) \quad (4.5)$$

If the switch is on forever, we get

$$\overline{x^2} = \frac{kT}{C} \quad (4.6)$$

which is the noise power in units of V^2/Hz for a simple R-C circuit. The obvious feature of Eq. 4.6 is that the noise power is totally independent of the resistor value. This feature in essence sets the minimum noise achievable and limits the maximum dynamic range for processing with switched capacitor filters of any

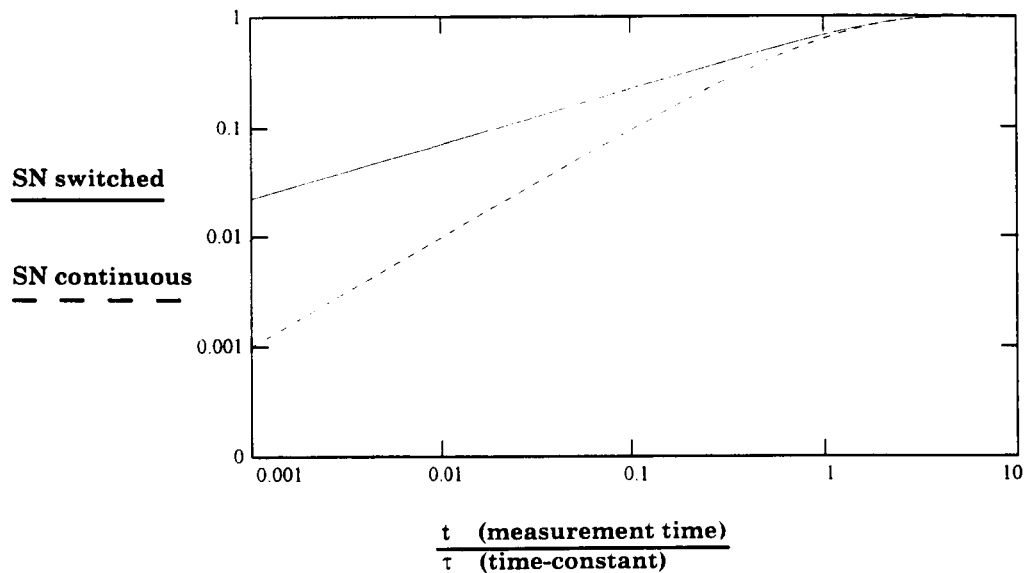
type. We may set the dynamic range equal to the signal-to-noise [TOM1] such that

$$DR = \frac{V_{ref}}{Noise} = \frac{V_{ref}}{\sqrt{kT/C}} = 2^n \quad (4.7)$$

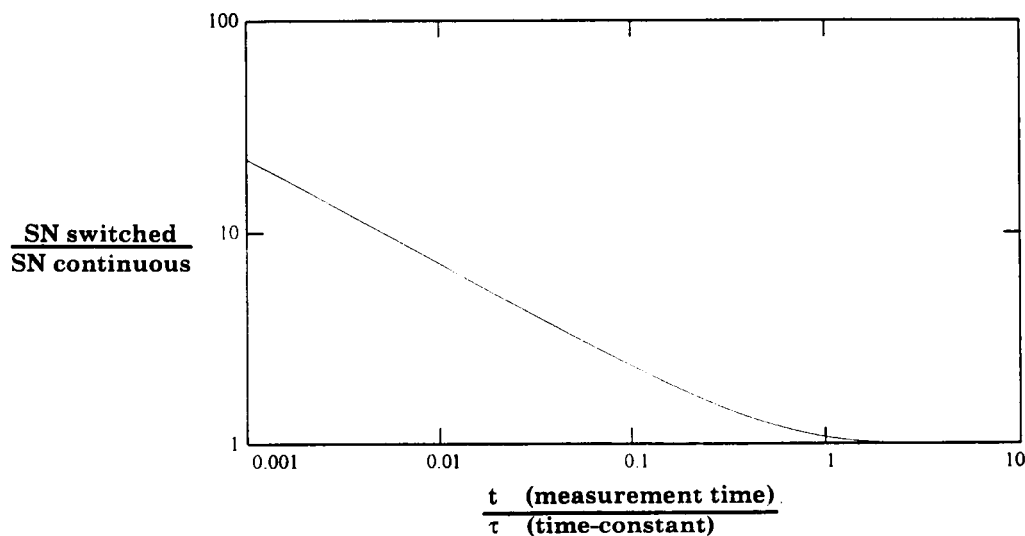
where DR is the dynamic range and V_{ref} is the maximum expected signal. Taking the logarithm of both sides and solving for n (number of effective bits of dynamic range) we obtain

$$n = \frac{0.5 \ln(C) + \ln(V_{ref}) - 0.5 \ln(kT)}{\ln(2)} \quad (4.8)$$

Obviously, the number of bits resolution is limited by the capacitor size for a given V_{ref} . For example, we will show presently that the sampling capacitor for the memory was 1pF. The noise voltage present on the sampling capacitor can be calculated from Eq. 4.6 to be 64.5μV rms. This can *only* be lowered by using a larger capacitor, *not* a smaller resistor. The noise measured at the sampling time t_I , on the other hand, is affected by the value of the resistor if the switch is closed for a finite time. As we will see in a later section, the value of R is 2K. If the sampling time is 10ns, we will find from Eq. 4.5 that the minimum noise voltage achievable is 64μV, only a 1% decrease. As we will presently see, this is a negligible contributor. Equation 4.1 holds for any white noise source at the input of the switch. The signal-noise ratio (S/N) of the switched network for a unit step input vs. the ratio of the measurement time to the filter time constant is shown in **Fig. 4-6(a)**. This figure also shows the S/N ratio for the unswitched filter.



(a) Switched filter SN and continuous filter SN.



(b) Ratio of switched filter SN to continuous filter SN.

Figure 4-6. Signal-to-noise (SN) comparisons of continuous-time RC filter vs. switched RC filter.

Figure 4-6(b) shows the ratio of the S/N of the switched divided by the S/N of the continuous. It is apparent that the measurement time must be significantly shorter than the time constant for a major improvement to be realized. This would seriously reduce the amplitude of the stored signals which would degrade performance due to other noise sources.

d. Readout amplifier noise During the time of readout, the amplifier and capacitor selected for readout form a wideband voltage amplifier as shown in **Fig. 4-7**. The equivalent input noise of the amplifier is amplified by the ratio of the capacitors such that

$$\overline{v_{out}^2(f)} = \overline{v_{amp}^2(f)} \left(\frac{C_p}{C_s} + 1 \right)^2 \quad (4.9)$$

where C_p is the stray input bus capacitance and switch diode capacitance for the voltage-read topology, and is the same for the charge-read topology with the addition of the sampling capacitor. C_s is the sampling capacitor for the voltage-read topology and the fixed feedback capacitor for the charge-read topology. This noise is present during the readout and is uncorrelated with the noise already present on the storage capacitor.

e. Pattern noise Switching noise is due to the addition or removal of charge from storage capacitors during activity of the digital control lines coming onto the chip and from nearby on-chip logic circuits that are active during some part of the storage time. This is evident to some extent in most mixed-mode integrated circuits. The modeling of this phenomenon is quite involved and is dependent upon both the process employed and the layout

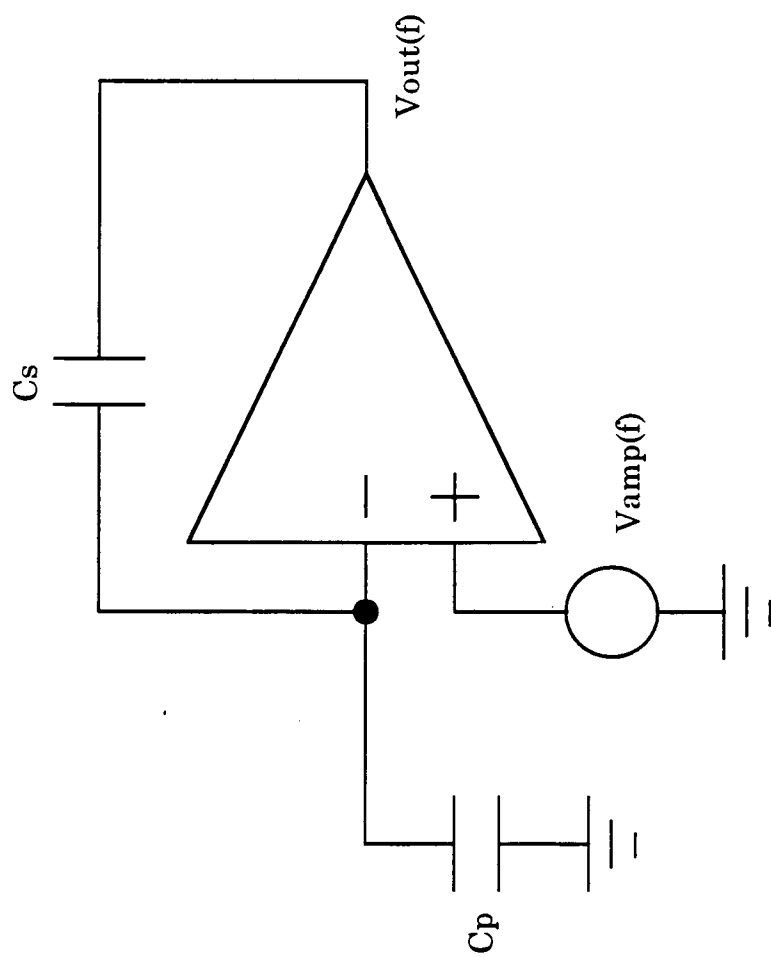


Figure 4-7. Readout configuration with lumped noise source.

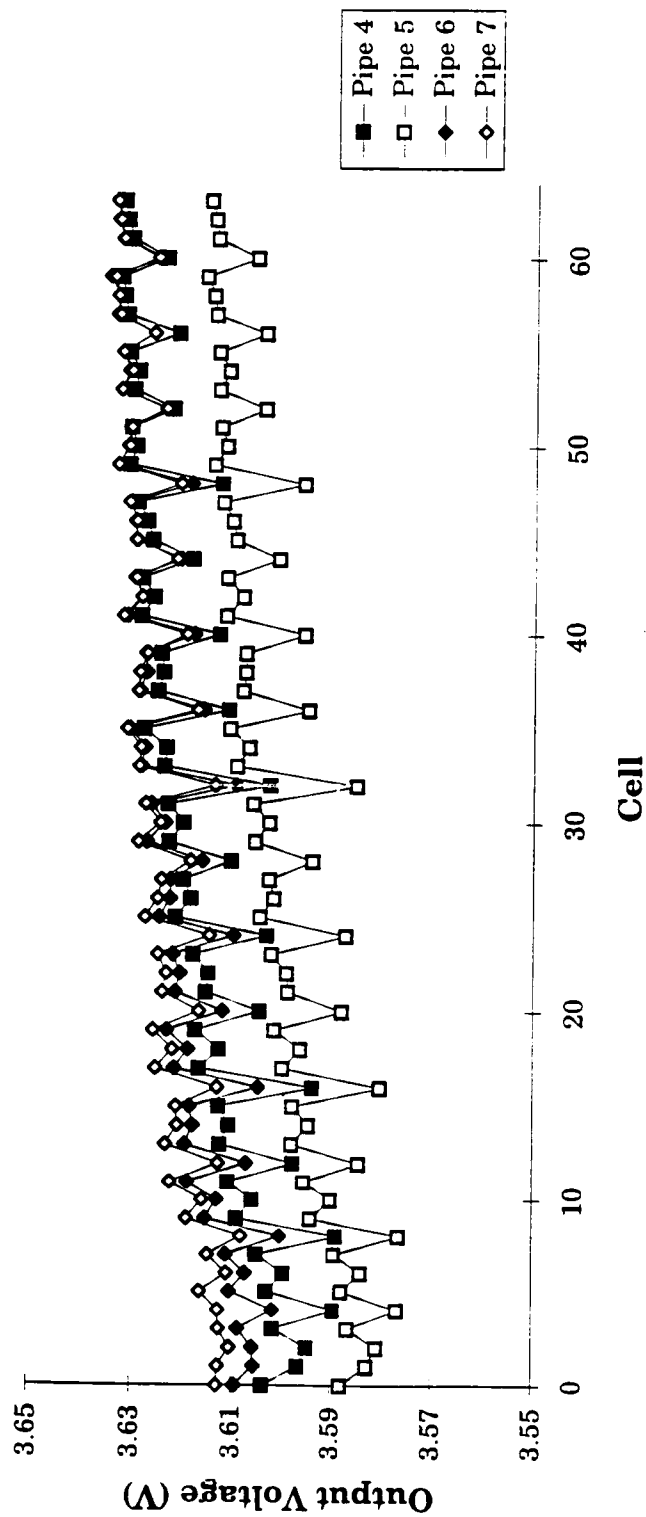
techniques[SU1] . For the specific case of analog memories that utilize parallel address buses for write-addressing and read-addressing, the cells, after a single pass write cycle of all cells in the pipelines, take on different amounts of charge due to the different times at which they are written. Upon reading the cells in the order in which they were written, a specific pattern of voltages can usually be seen, thus the name "pattern noise". If a binary pattern is used for addressing and the input is a dc voltage, one can see a distinct binary pattern upon reading, as shown in Fig. 4-8. If this pattern were the same for all possible input writing combinations, this would be relatively simple to correct. The memories of interest are simultaneous read-write, however, so the reading will take place asynchronously to the writing. This results in different patterns depending on the respective positions of the read and write pointers.

2. Readout speed

The amount of time allowed for an entire read cycle once a trigger has been received is estimated as follows: [TDR1]

<u>Operation</u>	<u>Dt</u>
Assert time slice (N_s times)	0
>Wait for AMU to settle	500ns
Assert channel (16 times)	0
>Wait for MUX to settle	20ns
Convert FADC	40ns
Assert chip (8 times)	0
>Load data / add	17ns
Increment chip	0
Increment channel	0
Increment time slice	0

The loops are represented by indentation. An equation describing this is given by



D99, Odd, 1.5 Volt Input, Average, 47.5MHz Binary Write.

Figure 4-8. Cell voltage vs. cell number.

$$\Delta t = N_S \times (500\text{ns} + 15 \times 20\text{ns} + 16 \times 40\text{ns} + 128 \times 17\text{ns}) \quad (4.10)$$

The AMU settling time is approximately 14% of the total. This time is one of the *largest* single contributors to the overall readout time. Prior to the design of this memory, the readout time of the memories available were on order of 1-2 μ s [LEVI1]. The biggest contributor to the minimum readout time is the settling time of the output readout amplifier. The design goals were to have an 8-bit settling time of $\leq 500\text{ns}$ for a 10pF load capacitance, while power dissipation should not exceed approximately 6mW. With the preamplifier design not finalized, the operating range was also not determined. Because the readout amplifiers, as shown previously, needed to function as inverters, the decision was then made to design an amplifier that would function optimally as an inverter with the input at approximately mid-scale (2.5V out of 5V) and to allow an output range very near both rails (rail-to-rail).

3. Power dissipation

The IPC detector required approximately 400,000 channels, each with its own preamplifier, AMU channel, and MUX channel. One FADC would be shared by 16 AMU channels. The entire IPC detector was given a budget of 25KW of power for all electronics. Because most of the power dissipated in an analog memory is due to the readout amplifier bias current, preliminary estimates of amplifier design indicated that we could develop a suitable amplifier with approximately 5mW dissipation (1mA total bias current and a 5V supply). We doubled this number for ample headroom and settled on a per channel dissipation of 10mW. This would result in approximately 4kW power dissipated due to the

memories for the entire detector. This allowed 21KW for all other functions, a number which was found to be suitable by designers of the other functional blocks in the detector.

4. Addressing

The 128-deep memory required a 7-bit address for both read and write. An on-chip address generator that would serve both read and write functions was a possibility, but would have required at least as much development as the rest of the memory. Because the reason for this development was first and foremost to determine the analog performance of the candidate CMOS process, a simple approach to address generation was chosen: i.e. all control would be handled by a state machine controller that was a separate chip. In addition, little was known about the Harris AVLSI process and how successful the first fab run would be. With these thoughts in mind, a decision was made to make the addressing to the AMU chip very simple. Because the pipeline was to be 128 cells deep, this would require a 7-bit decoder. In order to ease the requirements of having cell enable logic able to settle every 16 ns due to the beam crossing clock of the SSC, the decoders were configured as two separate 6-bit decoders, each controlling 64 cells in a pipe.

The major problem with this addressing approach was that since there are 12 read-address lines and 12 write-address lines, several lines will be toggling at any given time. As discussed in the section on linearity, this injects noise into the substrate and gives rise to pattern noise. An approach that is gaining popularity in Europe is to have internal skip logic. That is, in essence, a shift register that passes an 'on' signal from row to row on each beam clock [ANG1]. In this way,

only one row is on at any given time. This, in concept, should be less noisy due to injected charge but has added complexity of keeping track of addresses in some indirect fashion; i.e., keeping track of which row is on as opposed to what the address is. The simpler approach taken in the IPC memory allows one address manager chip to be used to control many memory chips, whereas for the token approach each chip must have some local address management. Otherwise, addresses would have to be piped to all chips under the control of a given manager; this would use more pins thus negating the benefits of the token scheme. Address management is one of the great areas of debate in modern large physics experiments that use simultaneous read-write memories.

5. Plans for expansion

The next step in the development of the GEM readout system would have been a 16-channel AMU, multiplexer, and ranging circuit for the memory. This was due to the decision that the cost of the electronics was lower for a 16-channel chip than for twice as many 8-channel chips. IPC also needed a greater dynamic range of approximately 10 bits. The ranging concept, shown in **Fig. 4-9**, has been implemented before [ALW1, SUM1] and has been shown to work well for the chosen applications, but it had never been put on an integrated circuit. This work was never completed due to termination of the SSC experiment.

GEM Memory Development

1. Topologies

a. Voltage-read The Harris Semiconductor AVL SI-RA process was chosen for this development for two reasons. First, the process had high-

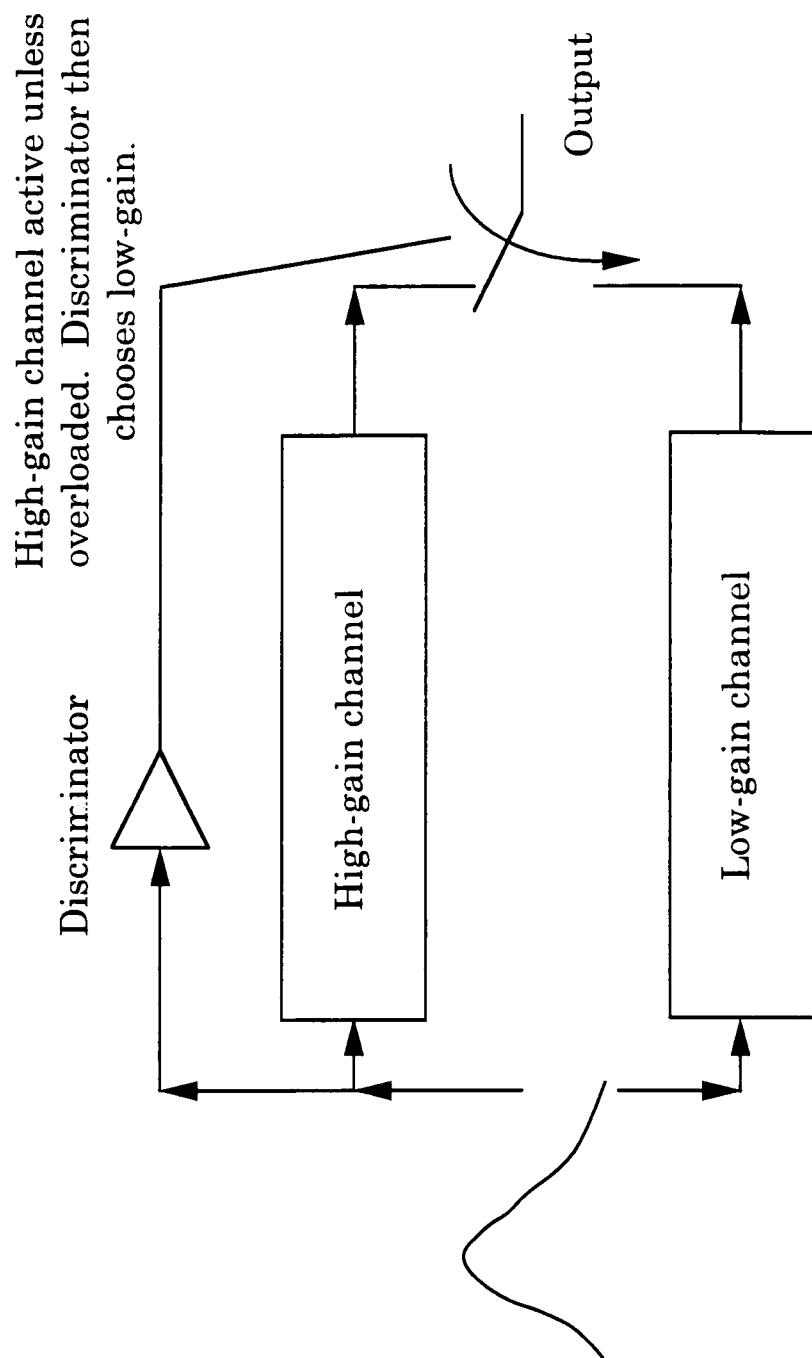


Figure 4-9. Ranging concept.

density capacitors as part of the standard processing steps. Second, ORNL had developed a good working relationship with Harris during a prior development that utilized the Harris Very-High Frequency (VHF) bipolar process [CLB1, RAT1]. With the availability of two-plate discrete capacitors, a voltage-write-voltage-read (VWVR) memory topology was developed. This topology has been widely used [SAK1, WA98] and has the advantage of reading a voltage and writing a voltage so that, to a first order, there is no component-dependent conversion-gain to introduce uncertainty in the measurement. Also, the switching action reduces common-mode noise effects. The simplified VWVR topology is shown in Fig. 4-10. The basic function is that during a write cycle, switches S1 and S2 are closed, while S3 and S4 are open. The voltage difference due to $(IN+) - (IN-)$ present at the input terminals is stored on the capacitor. At the end of the write cycle, switches S1 and S2 open leaving the voltage present at the end of the cycle stored on the capacitor C_{SAMPLE} . For a read cycle, the switches S1 and S2 remain open and S3 and S4 close connecting the capacitor across the output amplifier. The result is that the voltage present across the capacitor is then readable between the amplifier output and OUTREF. Many switches-and-capacitor cell sets just like the above can be added to the lines $IN+$ and $IN-$ resulting in a cell array as deep as one would need. The necessary decoding logic must be added for the user to choose which cell to write and which cell to read at any given time. It should be noted that because the input reference is $IN-$ and the readout reference is OUTREF, the input and output references can be equal or not equal, depending on the application. There are some practical limitations in the implementation, but separate references are possible.

Another advantage is that the readout speed is a function of the amplifier

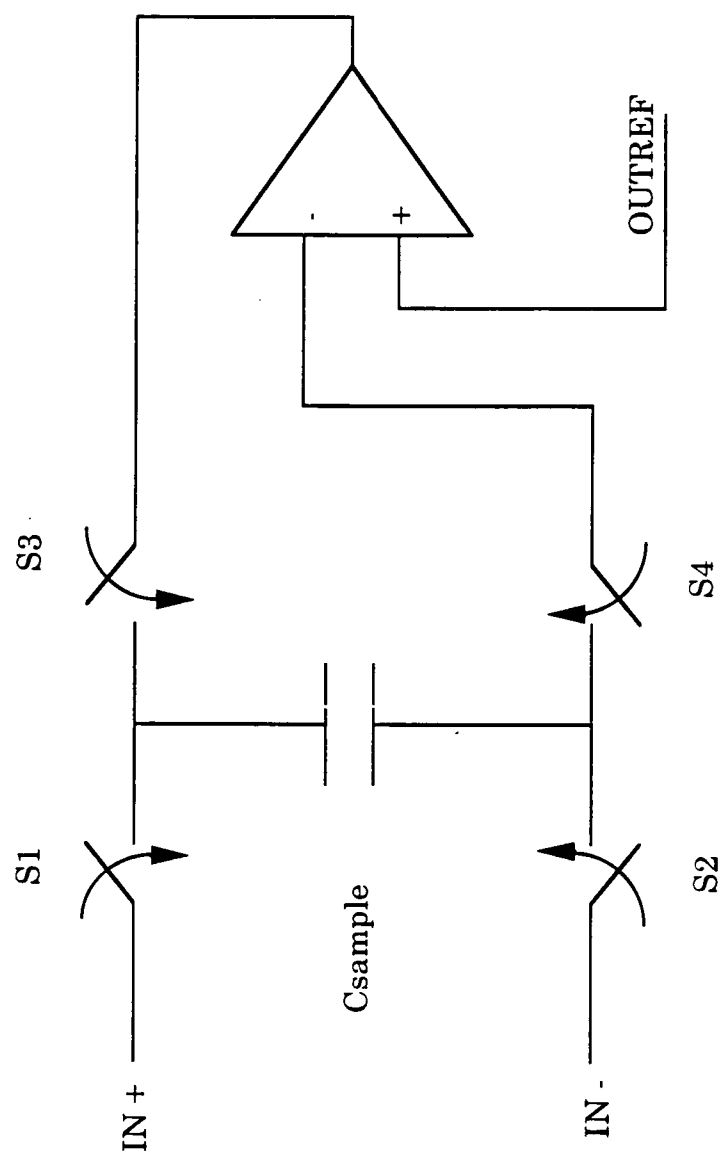


Figure 4-10. Simplified VWVR topology.

bandwidth, the sampling capacitor, and the stray capacitance on the inverting input bus as shown in **Fig. 4-11**. For a first order system, it is known that

$$t_{rise} = \frac{0.35}{f_{high}} \quad (4.11)$$

If we assume that the amplifier has a first order response, then

$$t_{rise} = \frac{0.35}{GBWP} \left(1 + \frac{C_{bus}}{C_{sample}} \right) \quad (4.12)$$

where $GBWP$ is the Gain-Bandwidth Product of the amplifier. From this it is obvious that the bus capacitance imposes a limit on the risetime of the readout and thus on the achievable readout speed (we will see in the next section that the Voltage-Write-Charge-Read (VWCR) topology has a more severe limit on the rise time). A proper compromise between amplifier speed, sampling capacitor size, and allowable bus capacitance is therefore necessary for fast readout with long (high-capacitance) busses.

The major disadvantage to the VWVR is that there are two resistors in series, each due to one set of switches, as shown in **Fig. 4-12**. We are interested in the time-constant required for the cell to settle to within some desired percentage of the final voltage. If we assume that the response of the sampling circuit is first order, the unity step response and the final value is defined by

$$h(t) = 1 - e^{-\frac{t}{RC}} \quad (4.13)$$

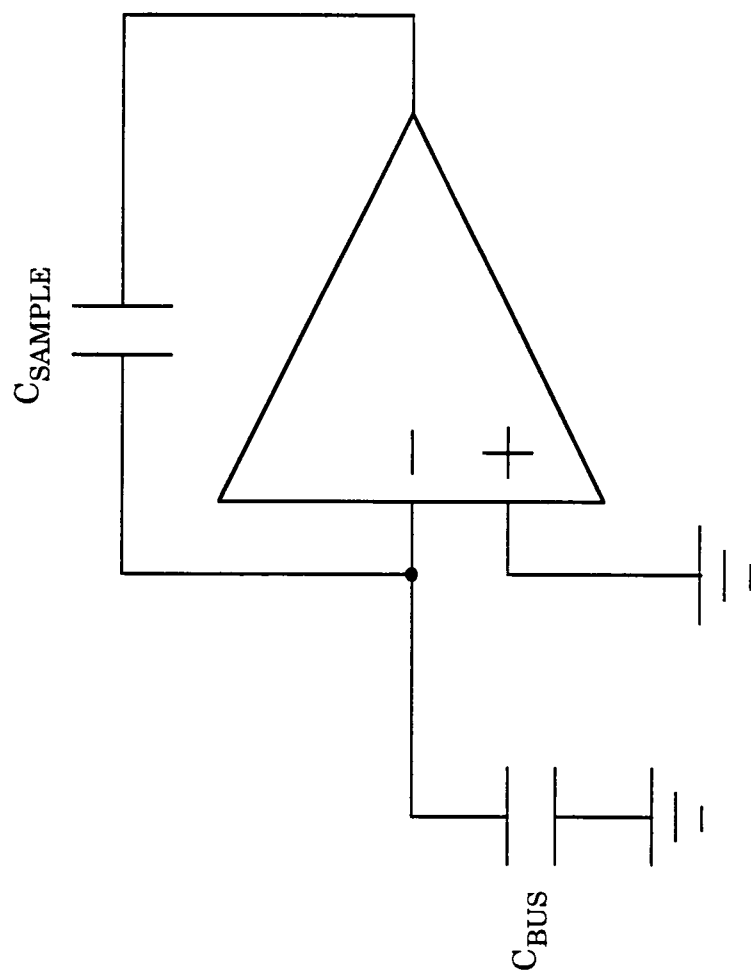


Figure 4-11. VWVR topology with simplified parasitics.

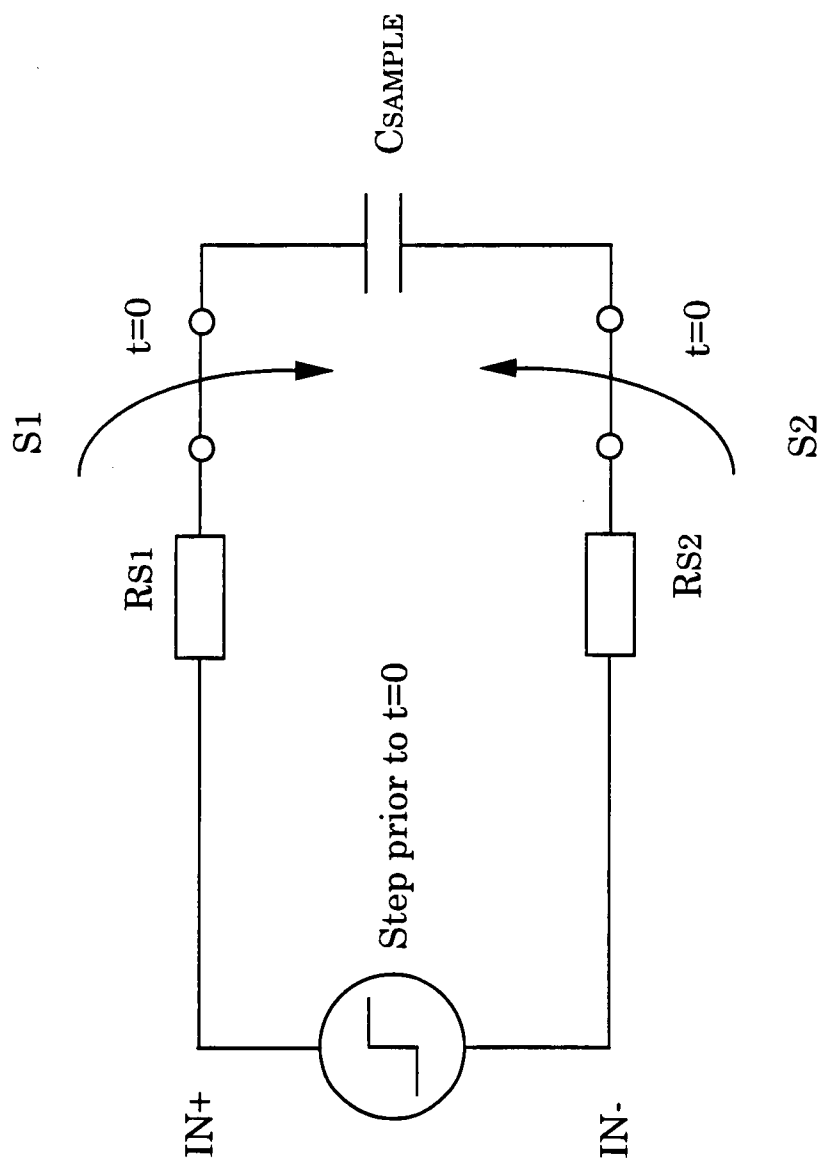


Figure 4-12. Equivalent circuit of VVR with series resistors added.

where t is the measurement time. If we want to find the voltage to which the step response of the filter has settled, we can subtract the filter response from the unity step itself and set the result equal to the inverse of the binary value to which we wish to settle obtaining

$$\frac{1}{2^n} = 1 - \left(1 - e^{-\frac{t}{RC}} \right) = e^{-\frac{t}{RC}} \quad (4.14)$$

Taking the logarithm of both sides and solving for RC we arrive at

$$\tau = RC = \frac{t_{\text{settling}}}{n \cdot \ln(2)} \quad (4.15)$$

where t_{settling} is the time desired for settling to within some desired n -bits of precision and τ is the required maximum time-constant of the RC circuit. A summary of the required time-constants normalized to a 1s settling time is presented in Table 4-1. The risetime associated with the given switch time constant is also presented. For example, if the desired precision of a given cell is 8-bits and the switch is on for 10ns, a time constant of 1.8ns is needed. This would result in a 1pF capacitor and a switch resistance of no larger than 1.8K. To implement a VWVR topology, the sum of the total switch resistance of both S1 and S2 must be no more than 1.8K. This means that, assuming equal sized switches, each switch would have to contribute no more than 0.9K.

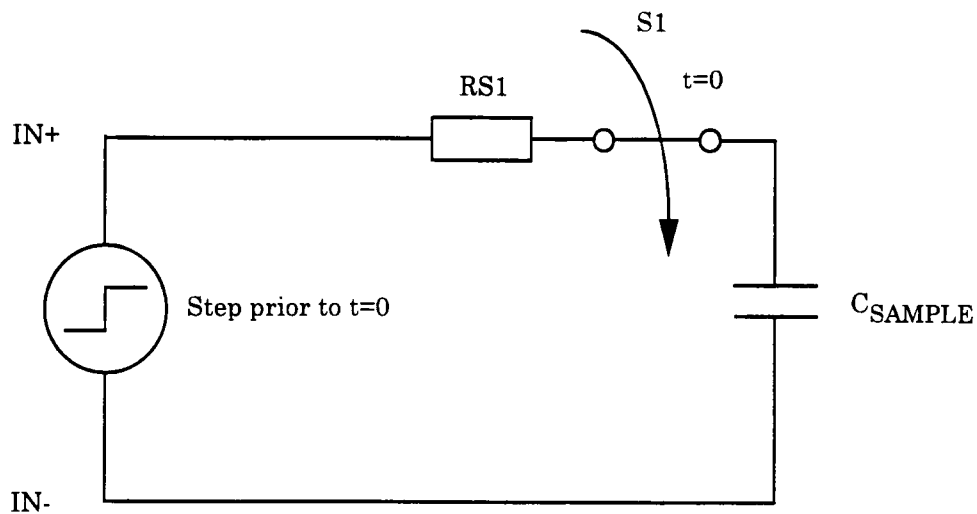
b. Charge-read Without having used the Harris AVL SI-RA process before and without having any true idea of it's hardness, there was a desire among the GEM management to have a backup plan in case the Harris option

failed. There were other processes available, but none (to our knowledge) had the high-density two plate capacitors. A decision was then made to fabricate a second

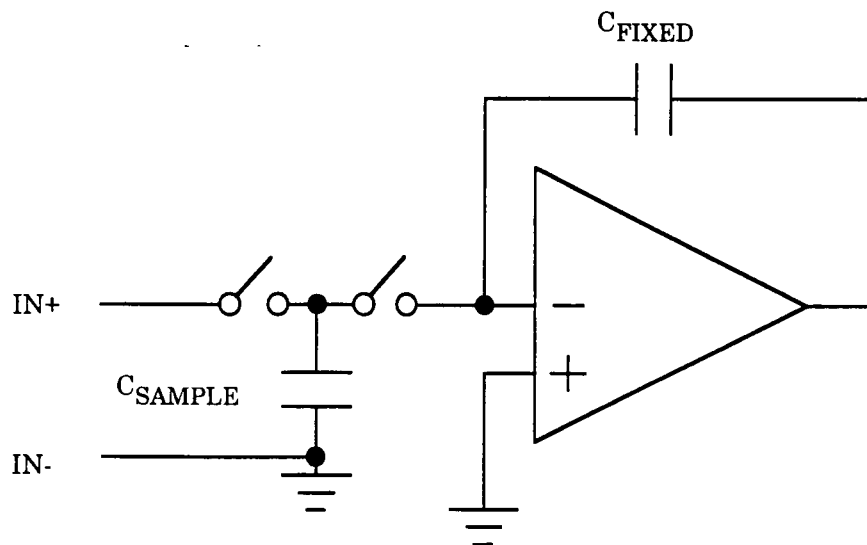
Table 4-1. Time-constant and associated risetime for a desired number of bits precision for a normalized settling time of 1 sec.

<u>BITS</u>	<u>τ</u>	<u>trise</u>
7	0.206	0.453
8	0.180	0.396
9	0.160	0.352
10	0.144	0.317
11	0.131	0.288

topology along with the VWVR that could possibly be built in a process not having precision capacitors. The topology chosen was the previously mentioned Voltage-Write-Charge-Read. The simplified VWCR topology is shown in **Figs.4-13(a)** and **(b)**. The sampling capacitor is written to in the same fashion as the VWVR. The difference is that, for the readout, the capacitor is connected to the inverting input of an amplifier that already has a fixed feedback capacitor as in **Fig. 4-13(b)**. The feedback action of the amplifier-feedback capacitor causes the charge present on the sampling capacitor to be transferred to the feedback capacitor. Because only one side of the sampling capacitor is connected to the amplifier, a capacitor with a grounded plate can be used as the sampling cap, thus eliminating the need for a floating capacitor in every cell. In concept, a MOSFET



(a) Equivalent circuit of VWCR with series resistors added.



(b) Typical VWCR amplifier connection.

Figure 4-13. Simplified VWCR topology.

gate could be used as the sampling capacitor if a digital rad-hard CMOS process had to be chosen. This, then, was the *main* reason for interest in the VWCR topology. Another advantage is the size of S1 for a given charging time constant. Because the deep-ohmic (where $|V_{DS}| \ll |V_{GS} - V_T|$) resistance of a MOSFET is described by

$$R_{ohmic} \propto \frac{L}{W} \quad (4.16)$$

where L is the length of the transistor and W is the width, the switch of **Fig. 4-13(a)**, for a given time-constant, would consume 1/4 the area compared to a VWVR topology for the same capacitor size.

The most obvious performance disadvantage of a VWCR topology is the increase in risetime of the readout amplifier and the resultant drop in readout speed. The risetime of the amplifier of **Fig. 4-13(b)** follows from the same concept as Eq. 4.12, namely

$$t_{rise} = \frac{0.35}{GBWP} \left(1 + \frac{C_{sample} + C_{bus}}{C_{fixed}} \right) \quad (4.17)$$

Unlike the VWVR topology, the VWCR topology output risetime depends not only on the values of the bus and sample capacitors, but on the ratio of the sum of these to the value of the feedback capacitor. For a unity gain inverting memory, the feedback capacitor must equal the sample capacitor. The relationship then becomes

$$t_{rise} = \frac{0.35}{GBWP} \left(2 + \frac{C_{bus}}{C_{fixed}} \right) \quad (4.18)$$

Because the switches are smaller in the VWCR memory, the bus capacitance is smaller than for the VWVR, but as we shall see in a later section, VWCR is still slower than a comparable VWVR.

c. Digitated vs. Sectioned As will be presently shown, the design requirements ultimately resulted in a sampling capacitor value of 1pF. The resultant cell size with switches is 330μ x 33μ. The overall plan was to develop two different readout amplifiers and, as already mentioned, two different types of cells. In addition, there was some concern about radiation effects on the off resistance of the switch transistors due to short-channel effects [TPM1, YANG1]. Each of the two types of memory cells therefore had two different lengths of transistors to test the effects of off resistance. The final layout was then to have 8 pipelines, each 128 cells long, with the combinations shown in Table 4-2. The decision was made to layout both VWVR and VWCR cells in the same pitch, even though the charge-read cells could be made smaller. This allowed the two amplifier designs to be used for both memory types without re-layout. The cells and control logic were designed to abut on all four sides of a cell so that any cell could be placed at any location. This greatly simplified layout.

Because the cells were 32μ long, the resultant memory length is 128x32μ or 4096μ. The decoding logic was to be designed with the same vertical pitch as the cells, i.e., 32μ tall. This would put a single logic decoder and driver on each row of the memory, all write decodes on one side and all read decodes on the other as shown in Fig. 4-14. The procedure for a simple static decoder is to address the

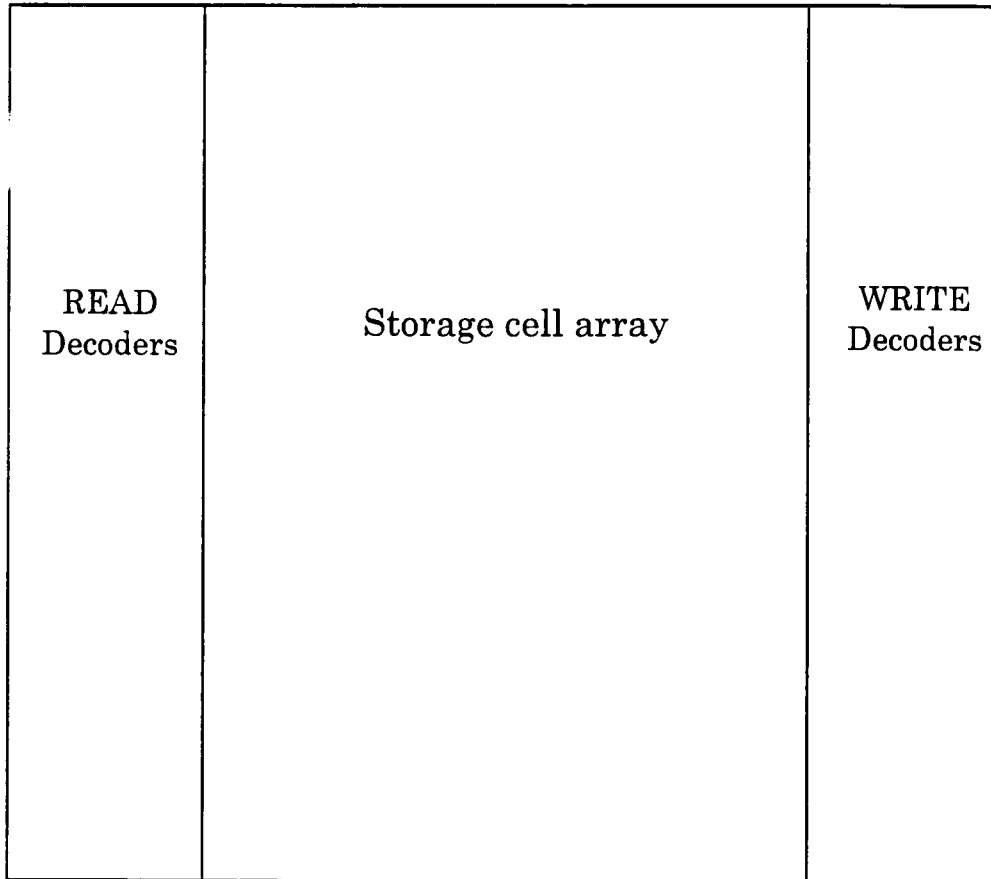


**Figure 4-14. WRITE decoder and
READ decoder locations.**

decoder with the address of the row desired for reading or writing, wait for the address to settle, and then enable the decoders. This last step actually turned on the read or write switches on an entire row of cells thus allowing the memory to be addressed. The enable line is the critical line with respect to timing and drive loading because it goes to every cell. The desired enable cycle for writing in this memory is to enable the memory cell for 8ns during a read, disable it for 4ns after read, issue a new address and wait 4ns more after which the cycle is repeated continuously.

Table 4-2. Analog memory pipeline components

<u>PIPELINE</u>	<u>MEMORY TYPE</u>	<u>AMPLIFIER</u>	<u>DEVICE LENGTH</u>
0	VWVR	IPC4B	short
1	"	"	long
2	"	IPC5C	short
3	"	"	long
4	VWCR	IPC4B	short
5	"	"	long
6	"	IPC5C	short
7	"	"	long

This problem of driving long enable lines is not new. A different approach has been implemented at CERN by utilizing shift registers that are clocked and 'bounce' the address along [SIP1, ANG1]. We chose to implement two different

chips to study this problem. The first was the Sectioned (S) chip. The S-chip employed two 6-bit decoders, called odd and even, respectively. Each decoded 64 cells with the even cells being spatially the lower 64 cells and the odd being the upper 64 as shown in **Fig. 4-15**. The Digitated (D) chip utilized the same cells and decoder circuitry, but the decoders were connected such that each decoder is connected to every other cell as shown in **Fig. 4-16**, thus the name Digitated. The expected advantage of the S-chip layout is that the write-enable lines were half as long as the same lines on the D-chip layout. This was expected to reduce the switching current through the lines and thus improve the reliability. The expected advantage of the D-chip layout was that the uniformity between pipelines should be better since the even and odd cell placement is spatially similar.

2. Capacitor cells

a. Non-ideal characteristics of CMOS switches Because MOSFETs allow the designer to implement a near ideal switch, analog memories should conceptually be straightforward in function because of the inherent simplicity. In reality, the implementation and testing of these memories expose several factors that are not ideal. Some of the more important factors will now be discussed.

1. Resistance vs. Input Voltage - A perfect switch would exhibit a series resistance of zero ohms when turned on and an infinite resistance when turned off. In a real MOSFET, this is not the case. For the "on" state, if we assume the gate voltage to be at 5V, the drain and source voltages approximately equal to each other, and the gate-source voltage to be more than the threshold

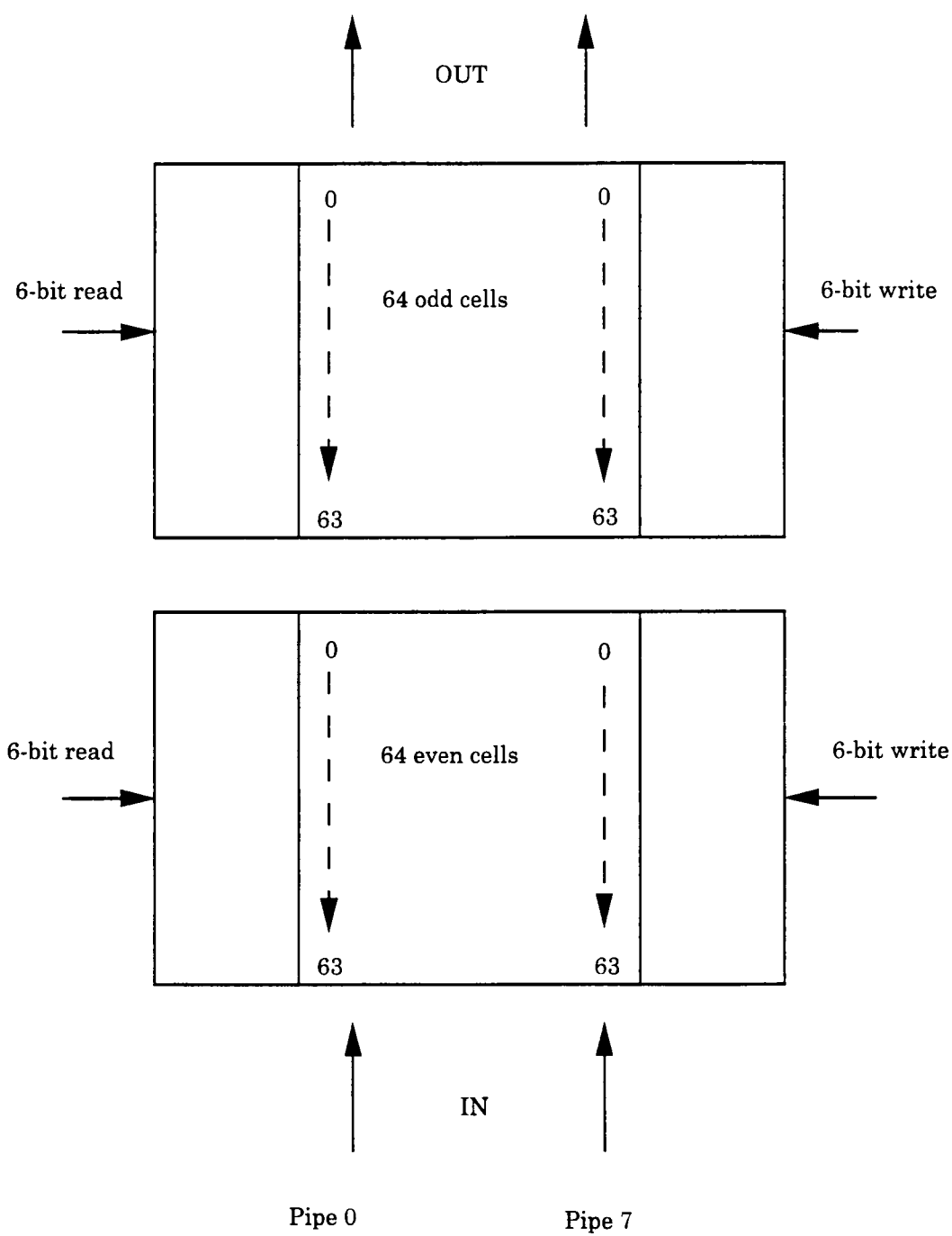


Figure 4-15. S-chip spatial layout.

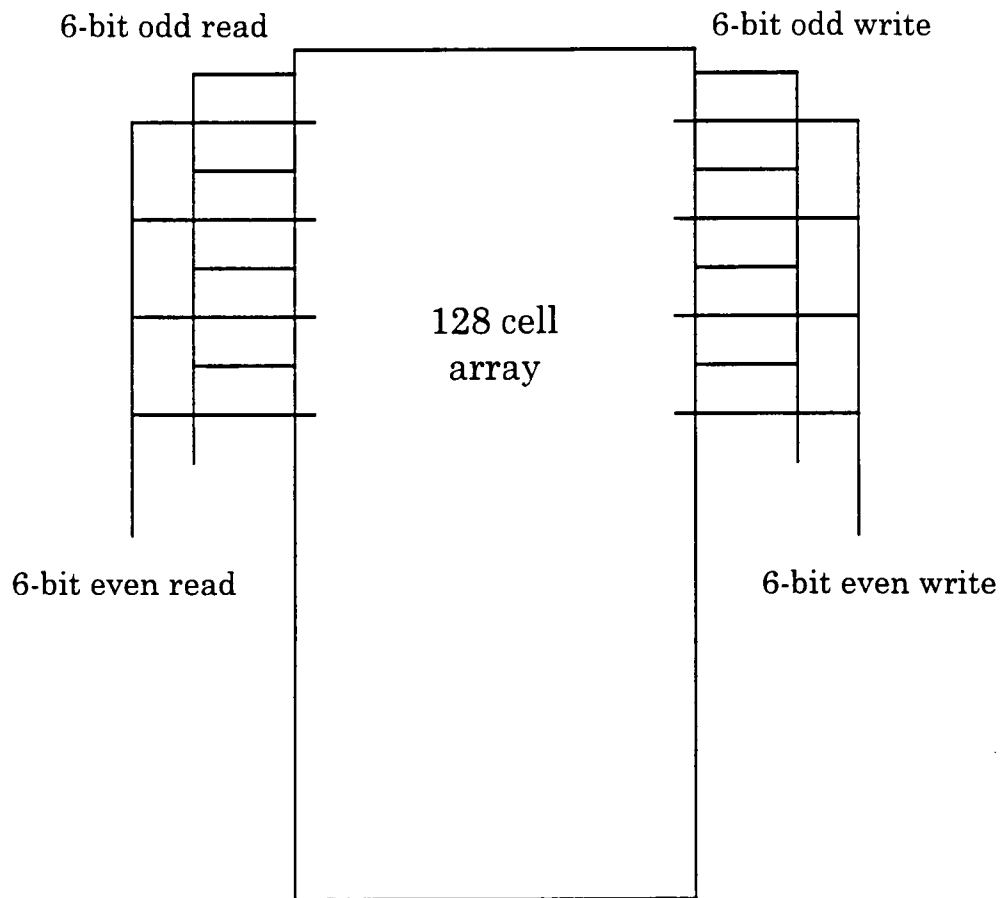


Figure 4-16. D-chip decoding and spatial layout.

voltage according to $|v_{GS} - V_T| \gg |v_{DS}|$, the current through the switch is given by [GRE1]

$$i_D = k \left[2 \left[v_{GS} - V_T(v_{GS}, v_{DS}) \right] v_{DS} - v_{DS}^2 \right] \quad (4.19)$$

where v_{GS} and v_{DS} are the gate-source and drain-source voltages respectively, V_T is the threshold voltage, and k is the transconductance factor. The approximate resistance between the drain and source terminals is

$$R_{ON} \approx \frac{1}{2k \left[v_{GS} - V_T(v_{GS}, v_{DS}) \right]} \quad (4.20)$$

The V_T term is shown as a function of gate-source and drain-source voltages because if the body voltage is tied to the negative rail (0V in this case), the threshold varies as a function of v_{SB} . When v_{GS} becomes approximately equal to V_T , the device turns off and the drain-source resistance approaches infinity as illustrated in **Fig. 4-17**. If two devices, one NMOS and one CMOS are combined in parallel, the resistance can be made to be low throughout the range from positive supply to negative supply if the NMOS gate is tied to the positive supply and the PMOS gate is tied to the negative supply. The NMOS is on and the PMOS off when the input goes toward the negative supply, and vice-versa when the input goes toward the positive supply. The problem generated by this type of response is that the charging time-constant of the capacitor is controlled by the voltage-sensitive resistance of the switch. For small signals close to the power-supply rails, the resistance and thus the charging time-constant is short and the capacitor can follow the input voltage. Close to the center of the power supply

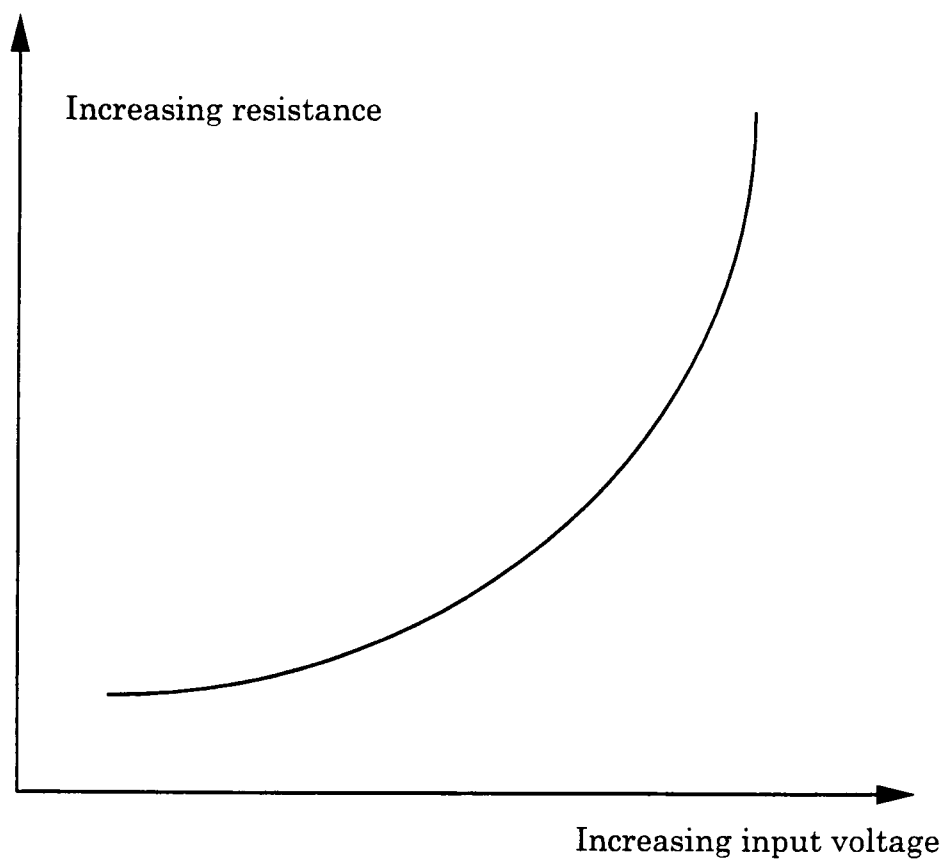


Figure 4-17. NMOS resistance vs. input voltage.

rails, the resistance is larger and thus the charging time-constant is longer which inhibits the capacitor from closely following the input and thus introduces non-linearity.

2. Charge injection - A perfect switch will simply turn on and off without disturbing the circuitry to which it is connected. A real switch implemented in MOS technology has several components that make it imperfect. A simple equivalent circuit is shown in **Fig. 4-18 [GRE1]**. The gate-source and gate-drain capacitances are the two primary contributors of charge injection into the input and output circuitry. To a first order, the values of C_{gs} and C_{gd} are constant. This results in a capacitive divider between the gate and the sampling capacitor. If the sampling capacitor is 1pF, C_{gd} is 10fF, and the gate voltage changes by 5V, as much as 50mV could be injected onto the sampling capacitor from the gate transition. A more accurate model of the stray capacitances (shown in **Fig. 4-19 [GRE3]**) confirms that reality is even worse because both C_{gs} and C_{gd} are non-linear. This will result in a non-linear perturbation voltage due to the stray charge injection.

Another source of charge injection is distribution of the charge within the MOS channel at the time of turnoff **[WEG1, SHEU1]**. This charge is generated when the transistor is turned on and the channel underneath the gate is inverted. The maximum time required for a mobile charge to reach one end of the channel is proportional to

$$T_0 \propto \frac{L^2}{\mu(V_{GON} - V_{TE})} \quad (4.21)$$

where μ is the carrier mobility, L the effective channel length, V_{GON} is the

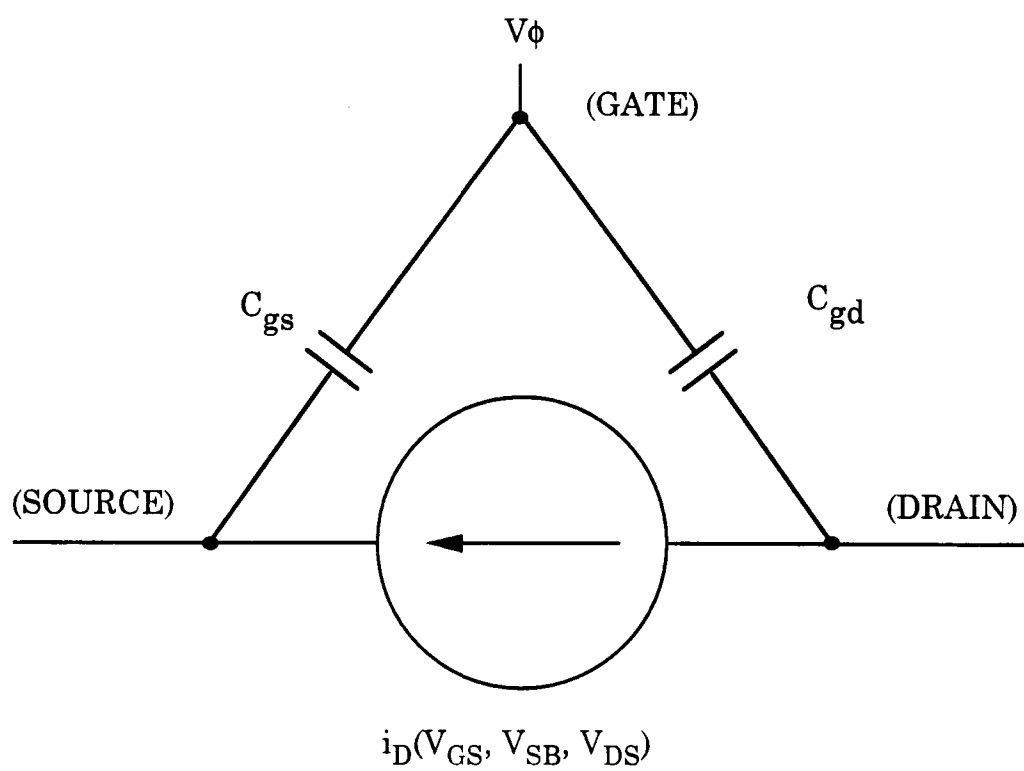


Figure 4-18. Simple MOS circuit.

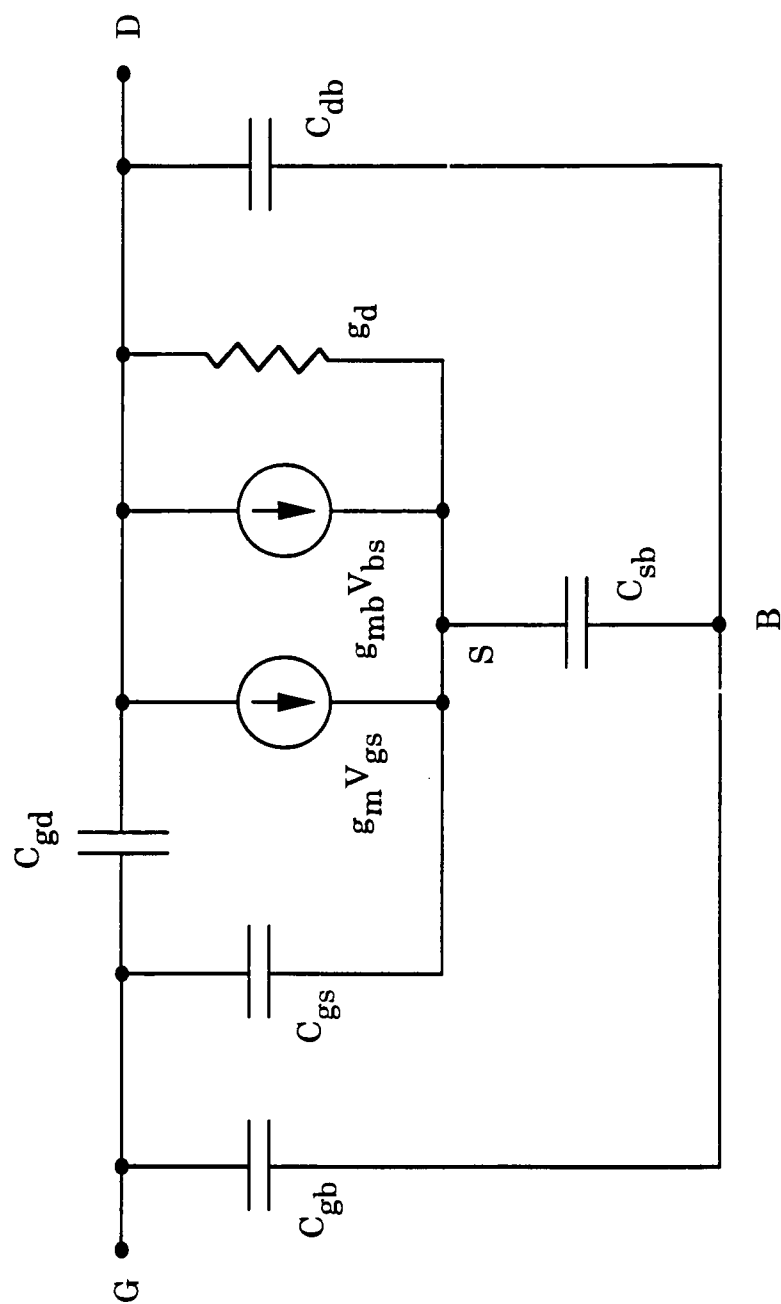


Figure 4-19. Equivalent MOS model.

voltage at which the gate is biased ON (+5V for NMOS and 0V for PMOS), and V_{TE} is the threshold voltage [WEG1]. If the transistors turn-off time is greater than T_0 the charge all flows from the channel into the drain and source circuits and essentially none into the substrate. If the turn off time is less than T_0 some charge is forced into the substrate and the charge flows approximately equally to the drain and source circuits. This is a problem because this charge will do little to affect the input of the memory bus, but the charge flowing towards the sampling capacitor will collect on the capacitor and show up as an error voltage. This is in addition to the perturbation due to the gate-source and gate-drain capacitances.

While the transistor is turning off but the gate-source voltage is still above the threshold voltage, all the sources of injection are operative. After the gate-source voltage has dropped below the threshold voltage, the charge from the channel has already been forced out through the drain and source, and the parasitic capacitances now account for most of the remaining charge injection.

3. Radiation Effects - The effects of ionizing radiation on the switches result in three basic effects. The first is the change in threshold voltage V_T . The change in threshold voltage for the AVLSI-RA process is supposed to be very small. We estimate the threshold voltage should change <10% of the power supply rail for our desired range of dose [THOM1]. Typically, the threshold voltages for both NMOS and PMOS devices shifts more negative after a moderate dose (10^5 rads) of gamma radiation. This in itself is not a major problem as the transistors will be turned on very hard during write. The areas in which the change in threshold could affect operation is in the charge injection. If the threshold voltage drops, the channel charge will have more time to distribute

during the turn-off, so the injection could change from pre-rad to post-rad.

The second effect is that the channel resistance increases after radiation. This is due to the reduction of mobility mentioned in Chapter III. The problem with this is that the time constant associated with the charging of the sampling capacitor through the switch will increase. This will adversely affect the linearity by reducing the available precision for a given write-enable time.

The third effect is the increase in leakage currents in the drain and source diodes of the transistors. The causes of this are 1) the currents generated by formation of electron-hole pairs in the drain-source diodes during irradiation and 2) an increase in generation centers due to displacement damage [SROUR4]. The thermal generation of electron-hole pairs at these centers will cause an increase in reverse-leakage current. The current from the diodes at the sampling capacitor have no where to go except onto the capacitor, which then disturbs the stored voltage. If the time allowed for this to continue is relatively short, the perturbation is small enough to be harmless. If the leakage increases however, the amount of time the charging can be allowed decreases, thus reducing the usefulness of the memory.

b. Effects of cell size on linearity As illustrated in Table 4-1, the charging time-constant, τ , of a cell determines the precision to which the sampled voltage can settle in a fixed amount of time. If the input is always a known, fixed shape, the decision of what t to use would be straightforward. A value for τ would be chosen that would allow settling to some desired final voltage at some known point on the waveform. The reality of the situation is, unfortunately, not so simple. The peaking time of the preamplifier-shaper that preceded the memory was approximately 50ns, greater than the sampling time of an individual cell.

The memory was designed to sample every 16ns for a duration of approximately 8-12ns as illustrated in **Fig. 4-20**. Also, due to the uncertainty of the position of the event with respect to the pickup wire and gas drift velocity, the position of the peak of the preamplifier signal with respect to the cell sampling time was a random variable, as illustrated in **Fig. 4-21**. Because of the uncertainty, any given cell has a very low probability of sampling exactly at the peak of the pulse. The most likely scenario was that the memory would sample within a few nanoseconds of the peak resulting in samples from the rising or falling edges of the pulse.

If a completely linear sampler was used, there would be little problem. The waveform would be sampled and some form of curve fit (assuming apriori knowledge of the wave shape) would allow the peak value to be approximated. The sampler is, however, not linear as discussed in section 2.a.1. If the pulse is some large fraction of the dynamic range, the time constant for each sample will be different, as shown in **Fig. 4-22**. This figure presents the results of a simulation in which a CMOS switch is connected to a 1pF capacitor and driven by a step voltage source which starts at 0V and steps to values of 0.1, 0.5, 1, 2.5, and 4V. A schematic of the simulation is shown in **Fig. 4-23**. The simulated resistance vs. input voltage plot of the circuit is presented in **Fig. 4-24** and shows a peak at approximately 3V. The time constants of **Fig. 4-22** are plotted vs. the input voltages in **Fig. 4-25**. This figure shows that the effective time constant for a signal whose normal baseline starts in the low-value region of the V-R curve of the switches is approximately equal to the time constant obtained by taking the instantaneous resistance value for a given peak voltage and multiplying it by the sampling capacitance. If the signal reaches the peak of the V-R curve and

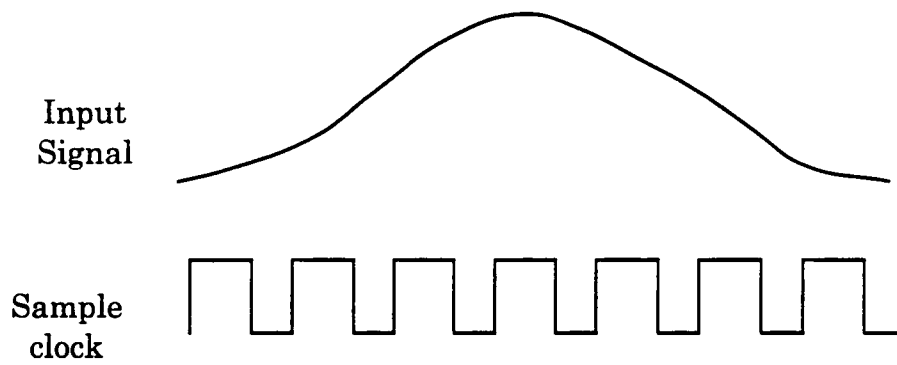


Figure 4-20. Sample clock and input signal relationship.

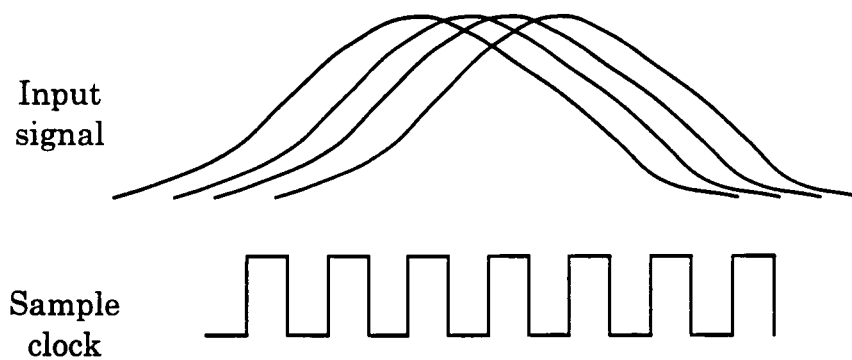


Figure 4-21. Exaggerated delay of input signal with respect to sampling signal due to gas delay.

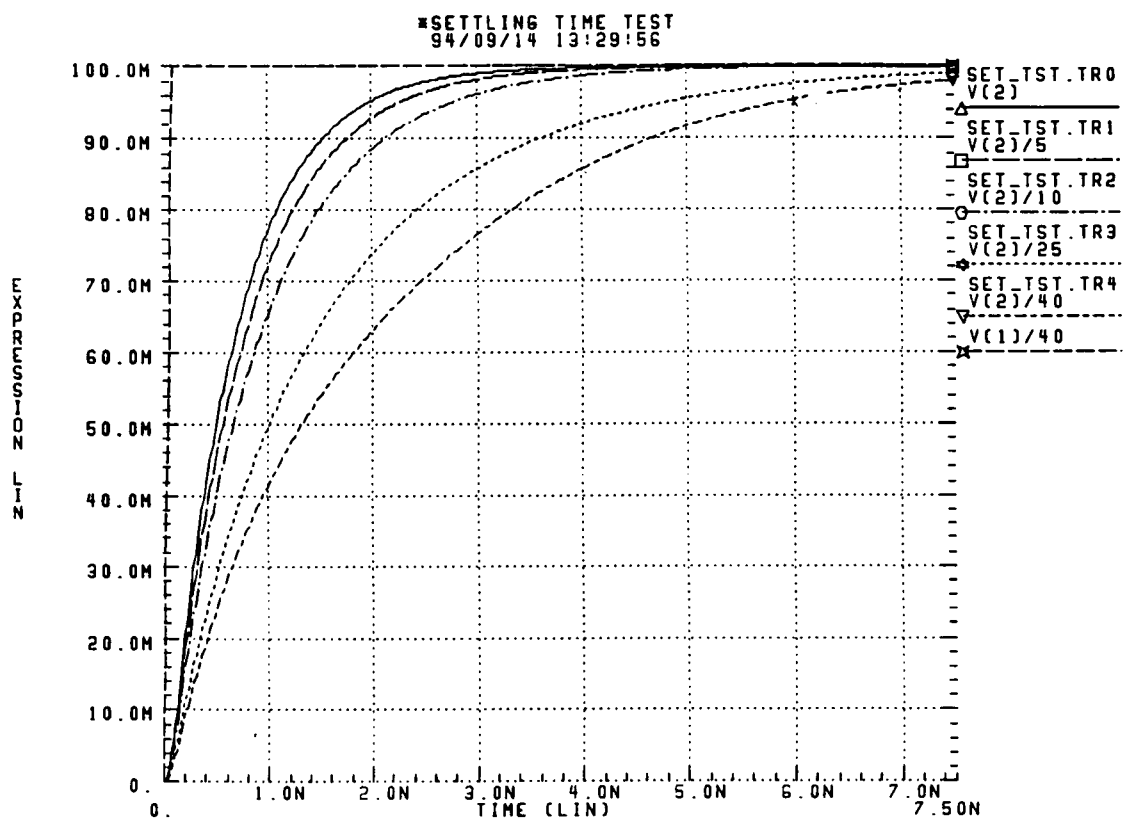


Figure 4-22. Normalized output pulse for input steps of 0V, 0.1V, 0.5V, 1V, 2.5V, and 4V.

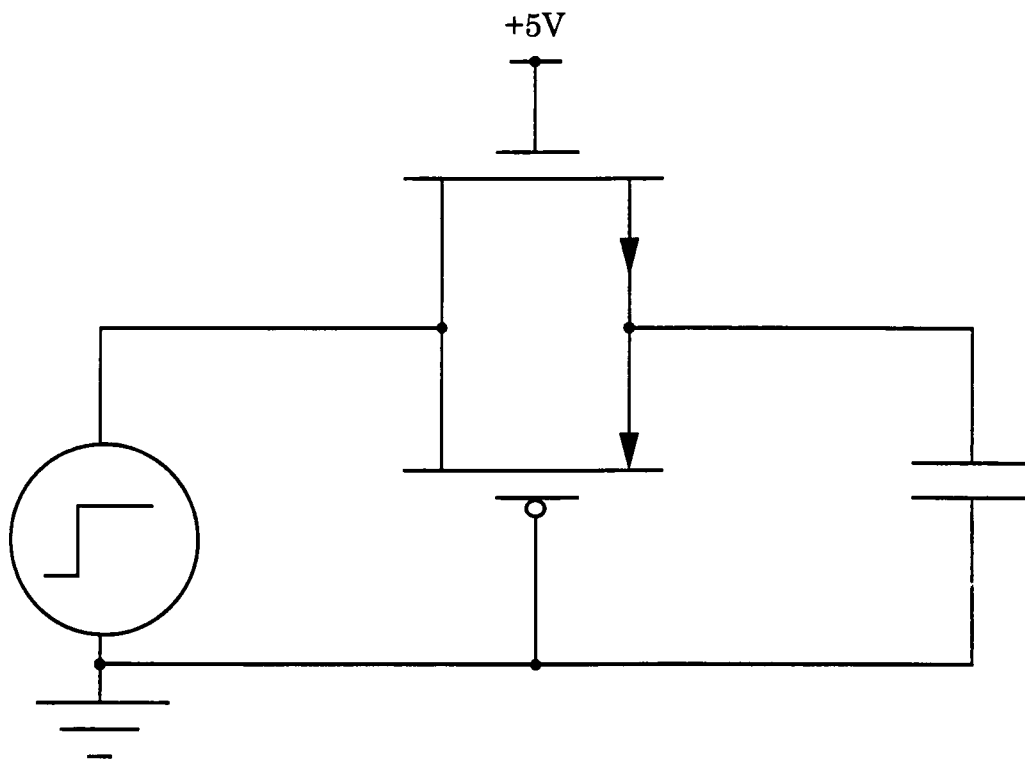


Figure 4-23. Schematic of the simulation.

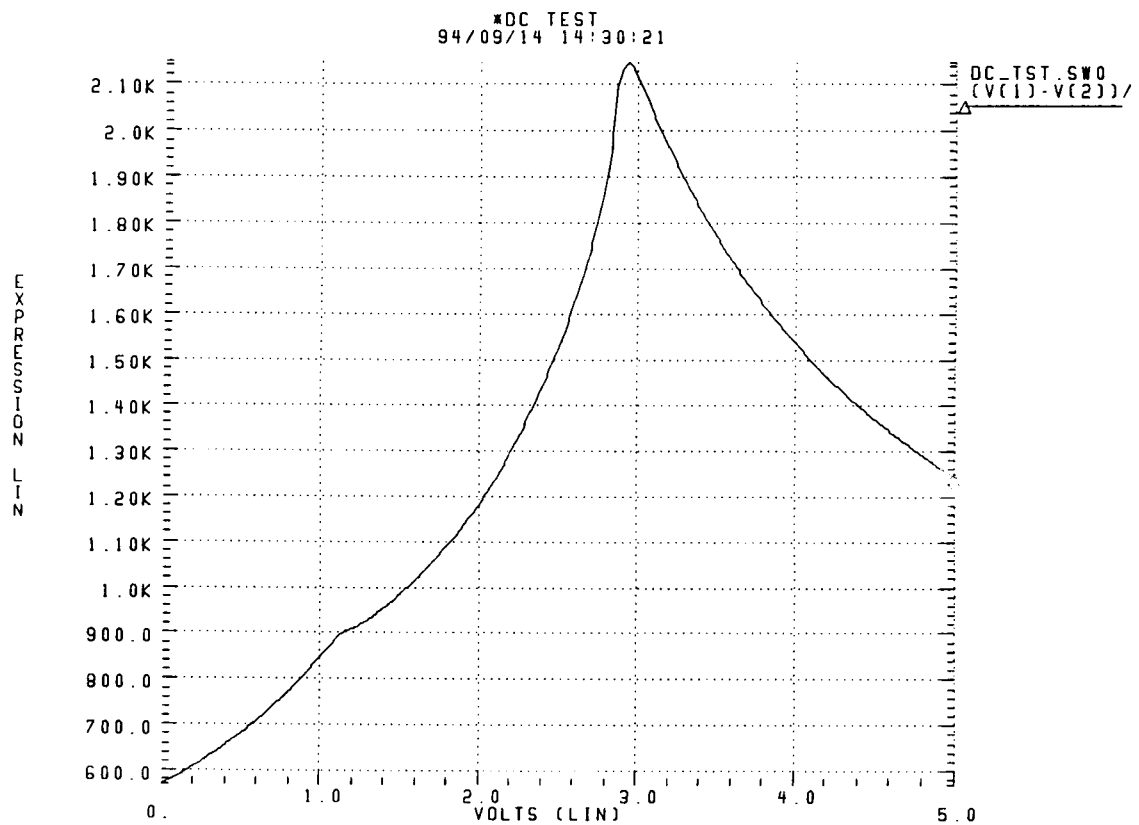


Figure 4-24. Simulated resistance vs. input voltage.

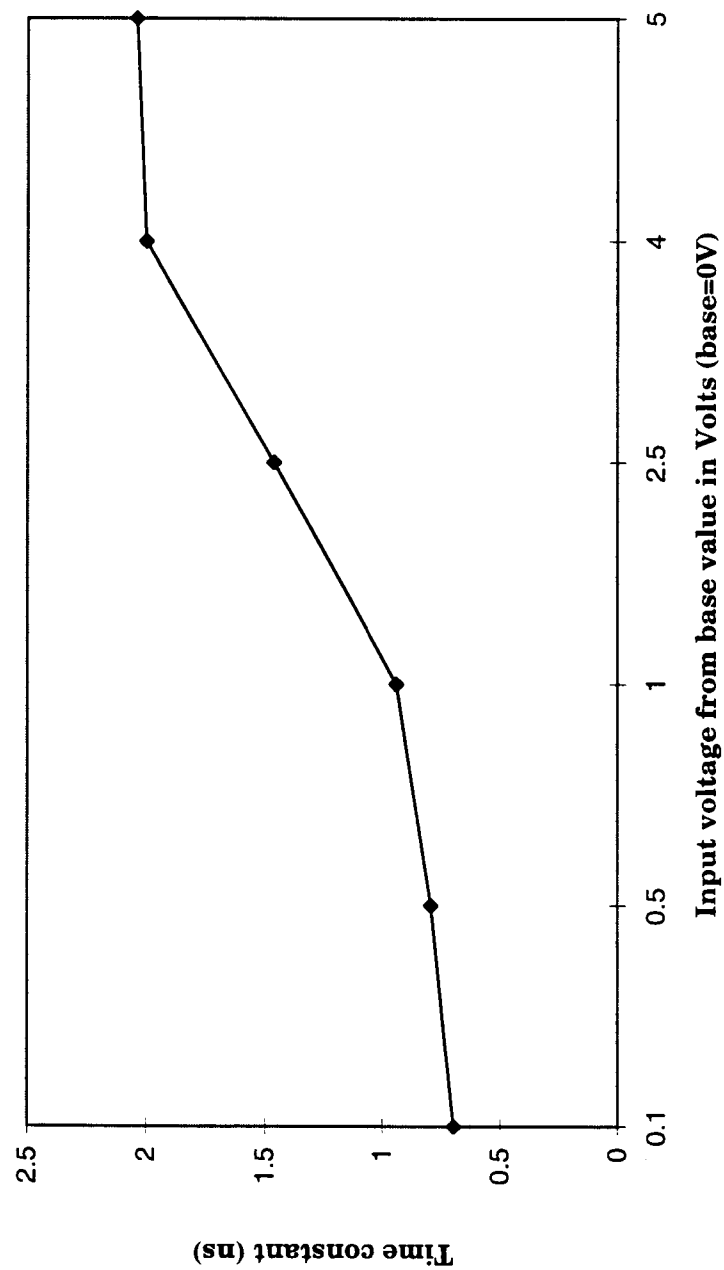


Figure 4-25. Simulated time constant vs. input voltage.

continues, the maximum value appears to hold. Mathematically, this would be written as

$$\tau_{effective} \approx \left[\max R(v_{in}) \right] \cdot C_{sample} \quad (4.22)$$

With this relationship, the transistor switch peak resistance and the capacitor size can be determined for a given sampling precision. If we assume the peak value of 2K is reasonable, the value from Table 4-1 for a 9-bit sampling precision can be used to calculate the capacitor, for a 12ns sampling time, as

$$C_{sample} = \frac{\tau_{effective}}{\max R(v_{in})} = \frac{0.160 \cdot 12ns}{2000} = 0.96pF \quad (4.23)$$

A 1pF capacitor was thus chosen.

The quiescent output voltage of the preamplifier immediately preceding the memory sets the baseline, so the memory operating point must be determined prior to designing the preamplifier if optimum performance is to be obtained. Consider the case of a preamplifier whose quiescent output is 3V and whose output goes more negative for greater signal voltages. The effective time-constant is much different for this case than the previous. The simulated $\tau_{effective}$ is shown in **Fig. 4-26**. This case places the quiescent operating point such that the increasing signal goes through the impedance maximum. **Fig. 4-27** presents a case that is only slightly different. It shows a case for a preamplifier that is just below the impedance maximum but whose output is also more negative for increasing signal. The values for $\tau_{effective}$ are quite different for the two cases.

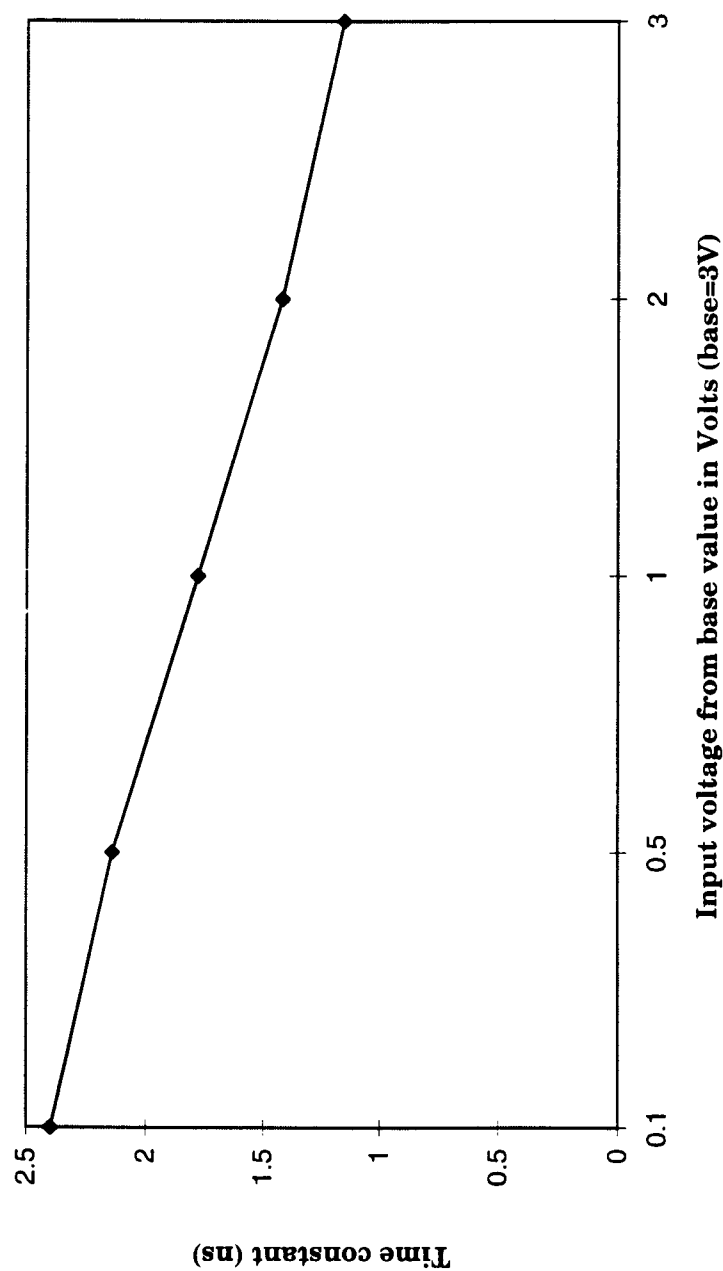


Figure 4-26. Simulated effective time-constant for input voltage of 3V to 0.1V.

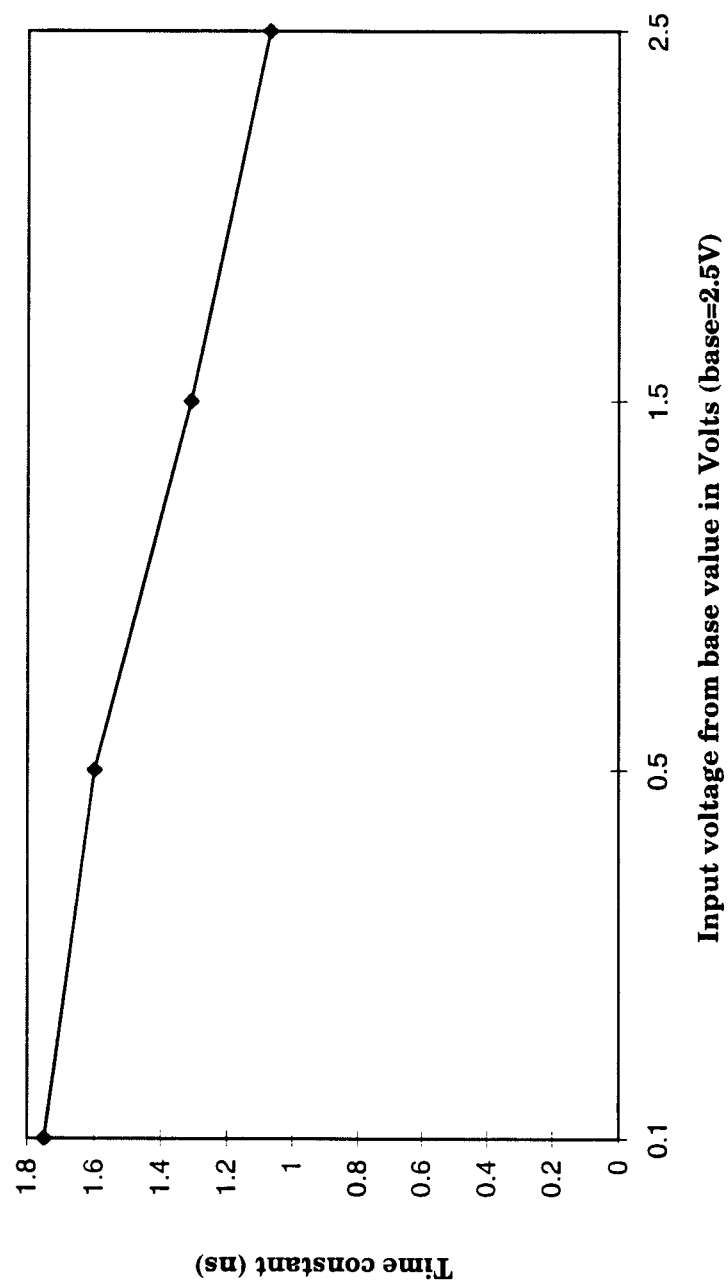


Figure 4-27. Simulated effective time-constant for input voltage of 2.5V to 0.1V.

3. Amplifier requirements

a. Bandwidth The required amplifier bandwidth is slightly different depending on whether VWVR or VWCR are being considered. Both will be discussed here. For the VWVR, if we require a settling time of 500ns for a 9-bit precision, Table 4-1 will give us a required rise time of 176ns. If we further anticipate a bus capacitance of 4pF and a sampling capacitor of 1pF and then rearrange Eq. 4.12 to solve for $GBWP$, we get

$$GBWP = \frac{0.35}{176ns} \left[1 + \frac{4pF}{1pF} \right] = 9.9MHz \quad (4.24)$$

In a similar fashion we can calculate the required $GBWP$ for the VWCR using Eq. 4.17. This gives a required $GBWP$ of 11.9MHz.

b. Slew rate With a required risetime of 176ns, we would at least want to be able to rise full scale in this time. Full scale from a midpoint reset will be 2.5V, so

$$SR = \frac{2.5V}{176ns} = 14.2V / \mu s \quad (4.25)$$

This should be considered a lower limit for the slew rate.

c. Effects of noise The noise gain of the system, as stated in Eq. 4.9, is a function of the sampling capacitor, the bus capacitance, and (for the VWCR configuration) the feedback capacitor. An estimate for the maximum input-referred noise can be calculated in the following way. Amplifier simulations showed the 100MHz bandwidth unity-gain output noise to be approximately

120 μ V rms. For a bus capacitance of 4pF and a feedback capacitor and sampling capacitor of 1pF, the noise-gain is approximately 5 (according to Eq. 4.9). This results in a 600 μ V output noise. The noise bandwidth for a single-pole lowpass system is [MACH1]

$$NBW = \frac{\pi}{2} f_{hi} \quad (4.26)$$

If the GBWP as previously calculated is 11.9MHz and the noise-gain is 5, the bandwidth will be equal to 2.4MHz. The noise bandwidth will then be equal to

$$NBW = \frac{\pi}{2} (2.4MHz) = 3.8MHz \quad (4.27)$$

The required spot-noise limit (ignoring 1/f noise) is

$$e_{noisein} = \left[\frac{(e_{noiseout})^2}{NBW} \right]^{1/2} = \left[\frac{(600\mu V)^2}{NBW} \right]^{1/2} = 308 \frac{nV}{\sqrt{Hz}} \quad (4.28)$$

This will be considered during opamp design.

d. Stability during read To a first order, the amplifier during readout is a straightforward voltage amplifier as shown in Fig. 4-11. In reality, the lines connected to the cells are distributed delay lines [NI] as shown in Fig. 4-28. The metal line has some resistance which is shown lumped as R_{line} . The stray capacitance of the metal and the depletion capacitance of the drain or source diodes are shown lumped together as C_{line} . The resistance and wiring

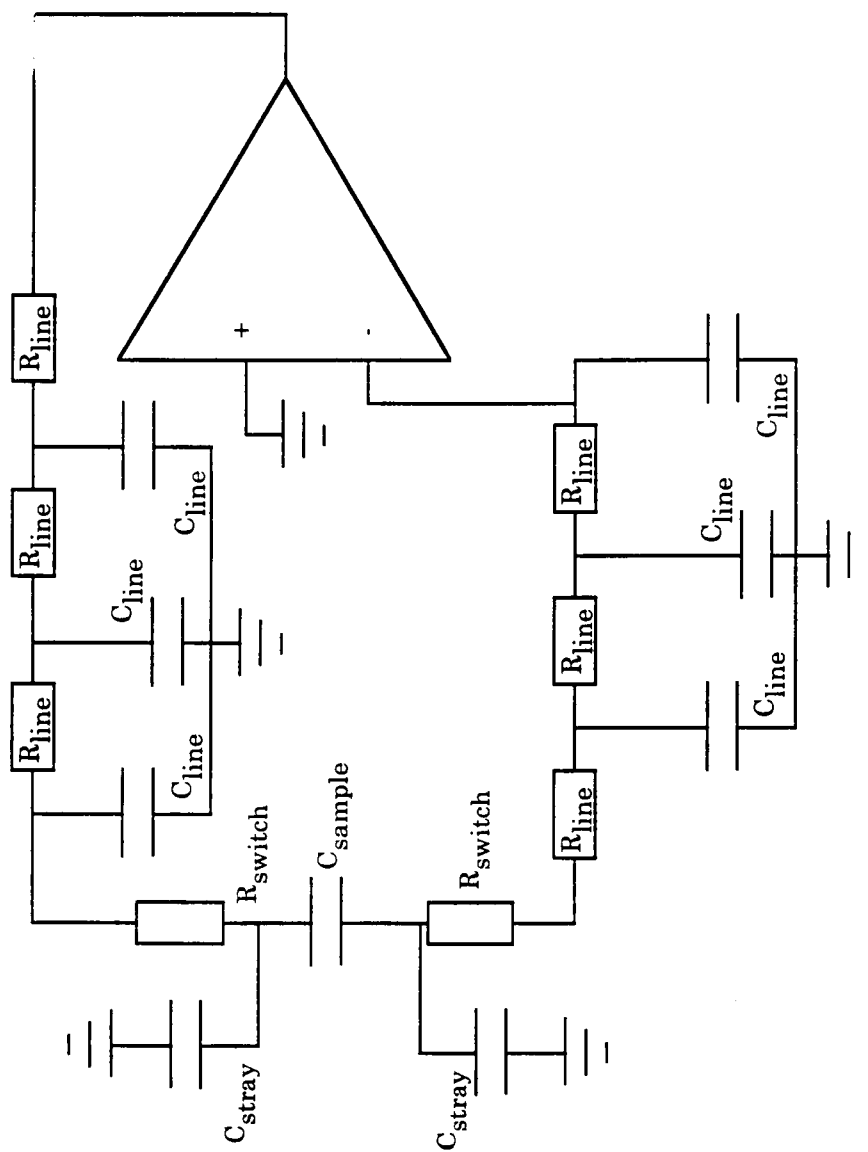


Figure 4-28. Model with lumped element delays in interconnect line.

capacitance of the switches are shown as R_{switch} and C_{stray} respectively. There are actually 128 sections of this R-C delay element in each line. Later simulations will show that the effect of this is small but present.

4. Readout amplifier design

a. Early versions The choice of a readout amplifier topology was driven by many requirements. The topology needed to be essentially a single-pole topology with high dc gain (>1000). It needed to be relatively bias independent (i.e., bias not dependent upon absolute values of components but upon matching and tracking of components). Amplifiers had been developed at ORNL for various projects [CLB2] but after simulations with Harris models, none of the topologies appeared to be sufficient. The main problem was phase margin for high gain-bandwidth products ($>10\text{MHz}$) and large output capacitances ($>10\text{pF}$). Two topologies were finally decided upon. The first was a modification of a previously published topology and the second was a modification of a standard two stage CMOS opamp. The developments will be covered separately.

The approach to development of both opamps taken in this development was a semi-empirical one. The equations with some first order approximations were derived in order to emphasize the most important effects. Components were then adjusted in simulations to achieve the desired response. The general design equations will be presented along with the resultant designs.

b. IPC4B The IPC4B amplifier was an outgrowth of major modifications on the rail-to-rail CMOS amplifier presented in an earlier publication [BAB1]. The amplifier as published employed fully differential and fully complementary input and output stages. This allowed both input and

output signals to operate close to the supply rails. Because the topology of the readout amplifiers required an inverting configuration, the input would always be at a fixed, known voltage of approximately $V_{dd}/2$. Only the output of the amplifier would need to approach the supply rail for large signals.

The essence of the output stage operation is presented in **Fig. 4-29**. The output consists of a push-pull differential to single-ended converter (M1, M2, M3, and M4). If the transistors are sized according to

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_4 \cdot \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3} \quad (4.29)$$

the effective transconductance to the output for a differential signal at the inputs of M2 and M4 is equal to the transconductance of M2. The gate capacitances of M1 and M3 generate a parasitic pole that can be controlled with sizing of the transistors. The time constant $\tau_{parasitic}$ of the pole as a function of the width of the transistors can be found by noting that the total capacitance at the gate of M1 is

$$C = C_{ox} \cdot (W_1 L_1 + W_3 L_3) \quad (4.30)$$

where W and L are the lengths and widths respectively of the subscripted transistors and C_{ox} is the oxide capacitance of M1 and M3. The resistance of M3 can be found to be [ALN1]

$$R_3 = \sqrt{\frac{2KW_3i_D}{L_3}} \quad (4.31)$$

where K is the transconductance factor and i_D is the drain current. The time constant $\tau_{parasitic}$ is found by combining Eqs. 4.30 and 4.31 to obtain

$$\tau_{parasitic} = CR_3 = \frac{L^2 C_{ox}}{\sqrt{2i_D K}} \left(\frac{W_3}{\sqrt{W_3}} + \sqrt{W_3} \right) \quad (4.32)$$

The minimum time constant is when $W_1=W_3$. In practice, that would have M1 dissipating the same amount of power as M3, clearly a wasteful situation. For this particular design, M1 was chosen to be equal to M2 and the width of M3 was chosen to be one-half of M1. The power dissipation of the amplifier was therefore dominated by the drain currents of M1-M2 with M3-M4 dissipating only 1/2 the power of M1-M2. The resultant $\tau_{parasitic}$ is only 2.1 times the theoretical minimum.

The input differential pair is important in that the rail-to-rail drive capability is derived from the balanced drive of the input pair. In order to stabilize the fully-differential input, a common-mode loop (**Fig. 4-29**) is utilized that, to a first order, allows only differential-mode signals to propagate to the output and inhibits common-mode signals. The common-mode loop is formed by M20-23, M16B and M17B. M17 acts as a voltage input that sets the operating point of the loop. M20 and M21 sense the common-mode voltage at the drains of M15 and M14. In order to keep the input devices balanced, the current in M22 must equal the sum of currents in M20 and M21.

If M20 and M21 were perfectly linear devices, any amplitude of differential signal at the gates of M20 and M21 would not disturb the voltage at the source of M22. In reality, the non-linearity and finite output impedance of M20-M22 introduce an unbalance in the common-mode response of the amplifier. The original paper presented an analysis of the common-mode loop that apparently had at least one typographical error and thus put the results into question. A simplified re-derivation is presented here.

The high dc gain of the Babanezhad opamp was not needed for the analog memory and thus the cascode interstage was removed. The gain-bandwidth product, taking information from the paper, was approximated as

$$GBWP \approx \frac{g_{m1}}{C1 + C2} \quad (4.33)$$

If we model the two capacitors as Miller capacitors and multiply each by a gain factor G to reflect the summation of the two paths at the output, the differential-mode response between the gates of M21-M22 and the output can be shown to have a pole at

$$p_1 = \frac{-g_{m21}}{2 \cdot \left(\frac{C1_{Miller} \cdot C2_{Miller}}{C1_{Miller} + C2_{Miller}} \right)} \quad (4.34)$$

and a zero at

$$z_1 = \frac{2 \cdot g_{m21}}{C1_{Miller} + C2_{Miller}} \quad (4.35)$$

assuming the gains G are equal. If the values of the Miller capacitances are equal, the pole and zero will cancel. If they are not, there is an opportunity for an un-canceled pole-zero doublet to cause settling problems [BAB1]. Miller capacitance is a capacitor whose virtual value is increased by the feedback circuit in which it is employed [PAUL1]. In fact, this approach to analysis is somewhat flawed because in reality the input impedances to each of the two paths of the output stage is resistive. In addition, the analysis ignores poles and delays inherent in the devices that definitely effect the transient response. It is for these reasons that the final transient response was adjusted in simulations.

The amplifier with final values is presented in **Fig. 4-30**. The right-half plane zero cancellation resistors M8 and M11 were sized according to the relationship [ALN2]

$$R_{M8} = \left(1 + \frac{C1}{C_{load6}} \right) \cdot \left(\frac{1}{g_{m6}} \right) \quad (4.36)$$

and

$$R_{M11} = \left(1 + \frac{C2}{C_{load25}} \right) \cdot \left(\frac{1}{g_{m25}} \right) \quad (4.37)$$

The transistors M8 and M11 are employed as resistors because, as shown in Eq. 4.20, the resistance (R_{ON}) of the transistor in the ohmic region is inversely proportional to the transconductance factor k but g_m is directly proportional to k . Because g_m is in the denominator of Eqs. 4.36 and 4.37, the values of resistance

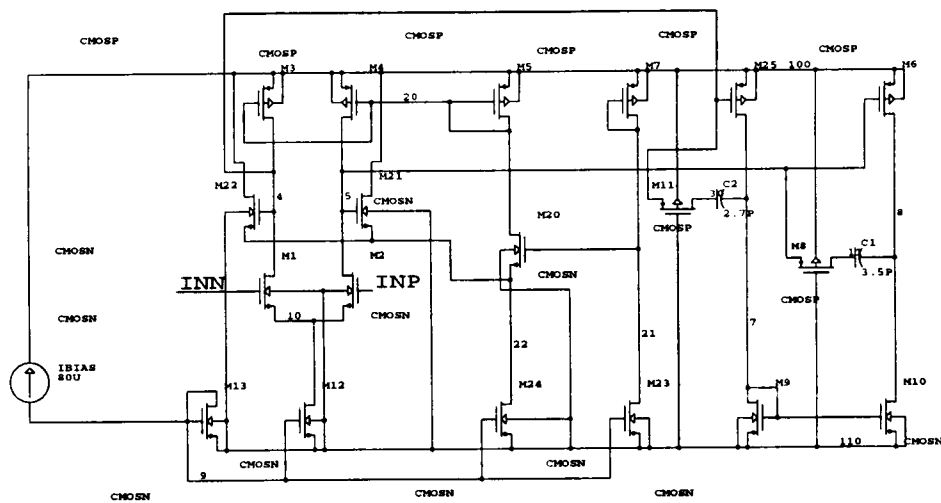


Figure 4-30. Final schematic IPC4B.

should track over process and temperature variations. From the requirements of driving the package, printed circuit board, and oscilloscope probe, C_{load6} (the output capacitance) is nominally 15pF. The simulated transient response was adjusted by varying C1. The final result is shown in **Fig. 4-31**. The expanded view of this result is shown in **Fig. 4-32**. If C2 is increased an overshoot results as shown in **Fig. 4-33**. A corresponding decrease in C2 results in an undershoot. The calculated noise of the resultant design is approximately $9\text{nV}/(\text{Hz})^{1/2}$ which is within the desired limit. The slew-rate in volts/ μs can be shown to be equal to

$$SR = \frac{I_{tail}}{C_{comp}} \quad (4.38)$$

Where I_{tail} is the total current in mA being supplied to the differential input pair and C_{comp} is the value in pF of the compensation capacitor. For this amplifier, the calculated slew-rate is approximately 23V/ μs .

c. IPC5C The IPC5C design, whose block diagram is shown in **Fig. 4-34**, is similar to the two-stage operational amplifiers found in most textbooks [ALN1] except that the output stage has a bi-directional drive capability. Transistor M6 is the primary driver that is driven from the high-impedance node of M4 and the differential input, but the complementary path of M3, M7, M9, and M10 provides an active, positive drive capability. The value of C1 sets the band width according to [ALN1]

$$GBWP \approx \frac{g_{m(input)}}{C1} \quad (4.39)$$

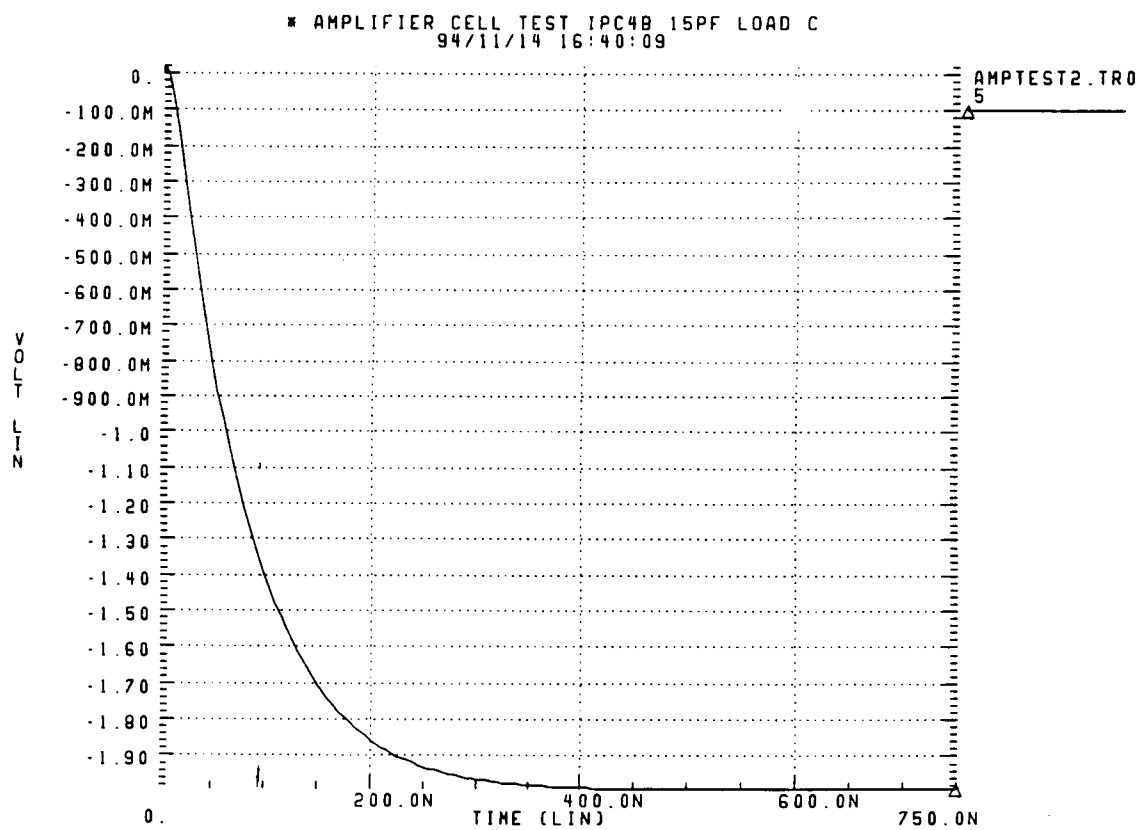


Figure 4-31. Transient response simulation.

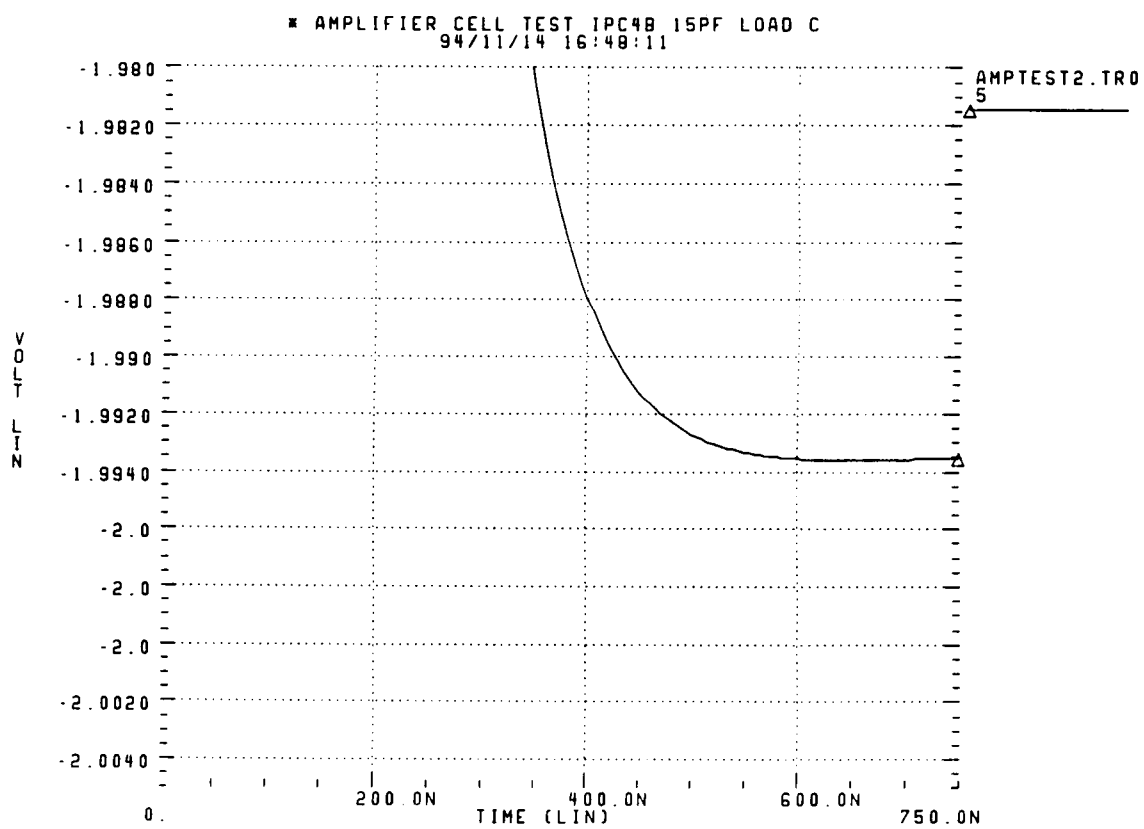


Figure 4-32. Expanded transient response simulation.

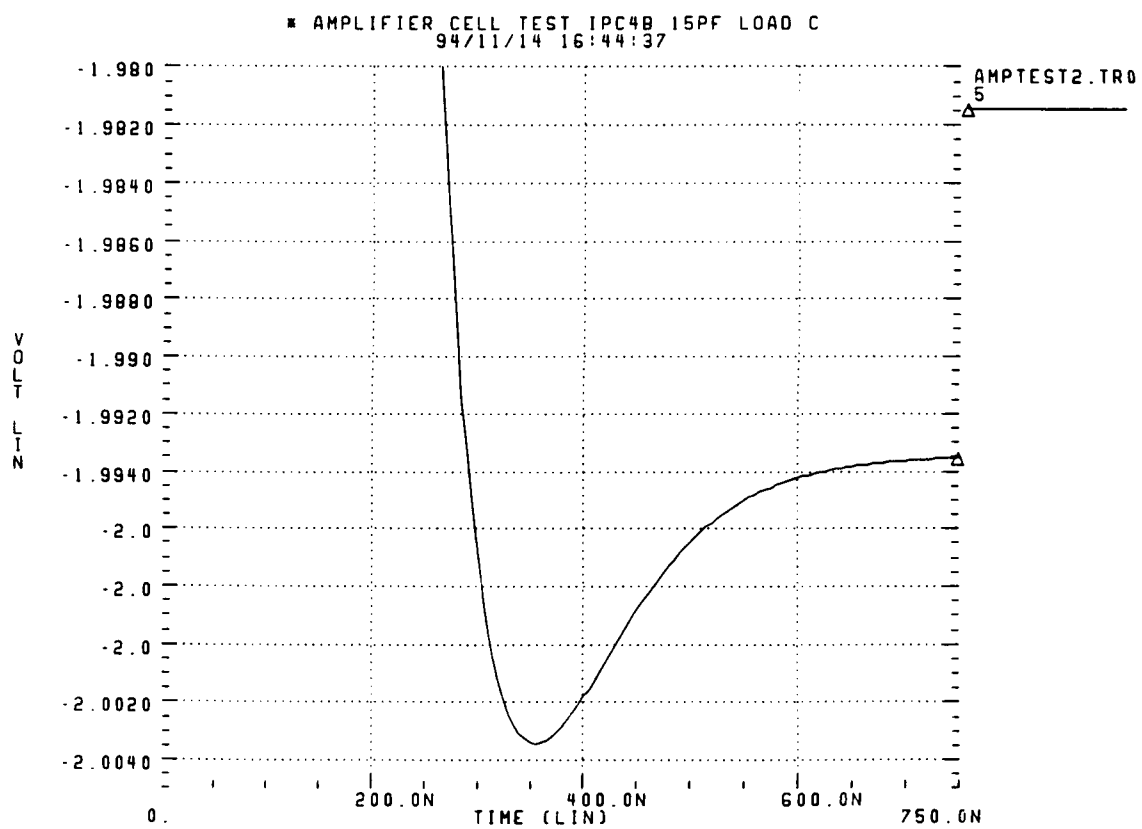


Figure 4-33. Transient response simulation for C2=5.6pF.

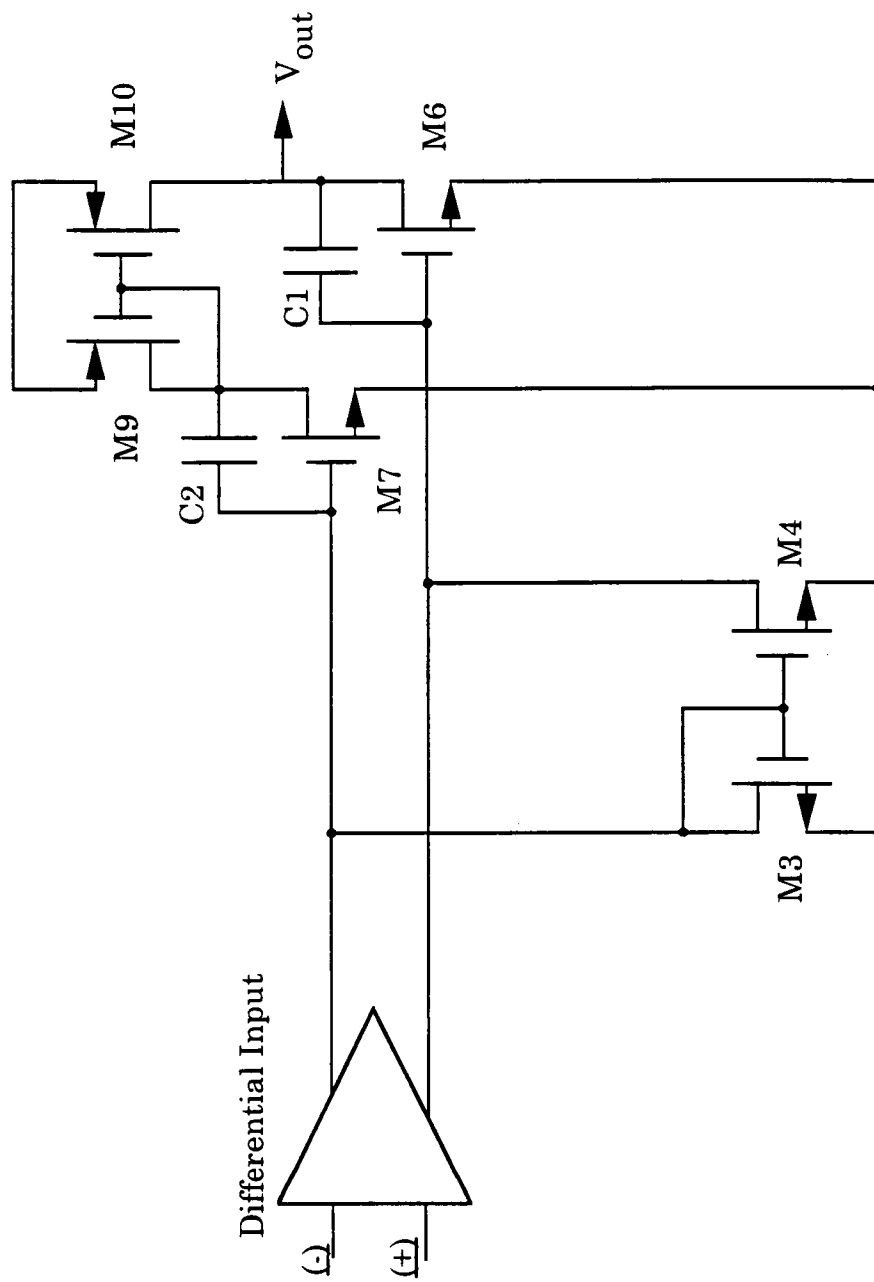


Figure 4-34. Block diagram of IPC5C opamp.

The presence of C2 reduces the gain-bandwidth of the upper path and improves the phase margin of the overall circuit. Without C2, the pole at the gate of M9 dominates the upper path response and can lead to instabilities. The addition of C2 reduces the gain of the upper path. The chosen design sets the pole at the gate of M9 at approximately 29MHz. The inclusion of C2 allows the pole location remain essentially unchanged but adds a lower frequency pole at approximately 16MHz. The value of C2 was adjusted in simulation to give the optimum unity-gain pulse response. A schematic of the final amplifier is shown in **Fig. 4-35**.

5. Logic Design

The development of the logic for the memories involved the architectural considerations and the transistor sizing considerations. The basic architecture is shown in **Fig. 4-36**. The 6-bit addresses are made present on lines A0-A5, given time to settle, and then the ENABLE line is set high. The logic architecture is identical for both read and write: only device sizes are different. A schematic of the 3-input NOR is presented in **Fig. 4-37** and the inverters in **Fig. 4-38**. In order to minimize the delay through all the drivers, the inverters were designed as tapered buffers [GAS1]. The gates employ standard CMOS topologies [WESTE1]. The static topologies were chosen over more area-conserving dynamic topologies due to the need in a dynamic topology of multiphase clocks [WESTE2].

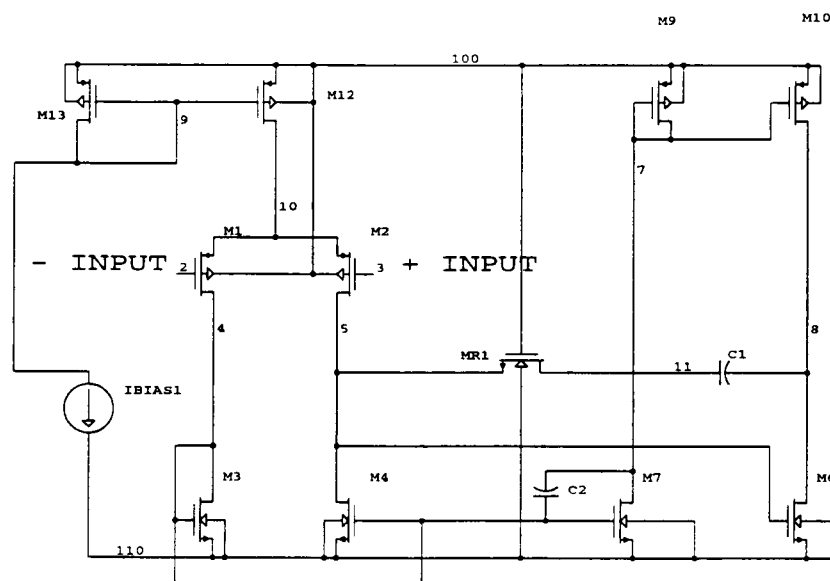


Figure 4-35. Final schematic IPC5C.

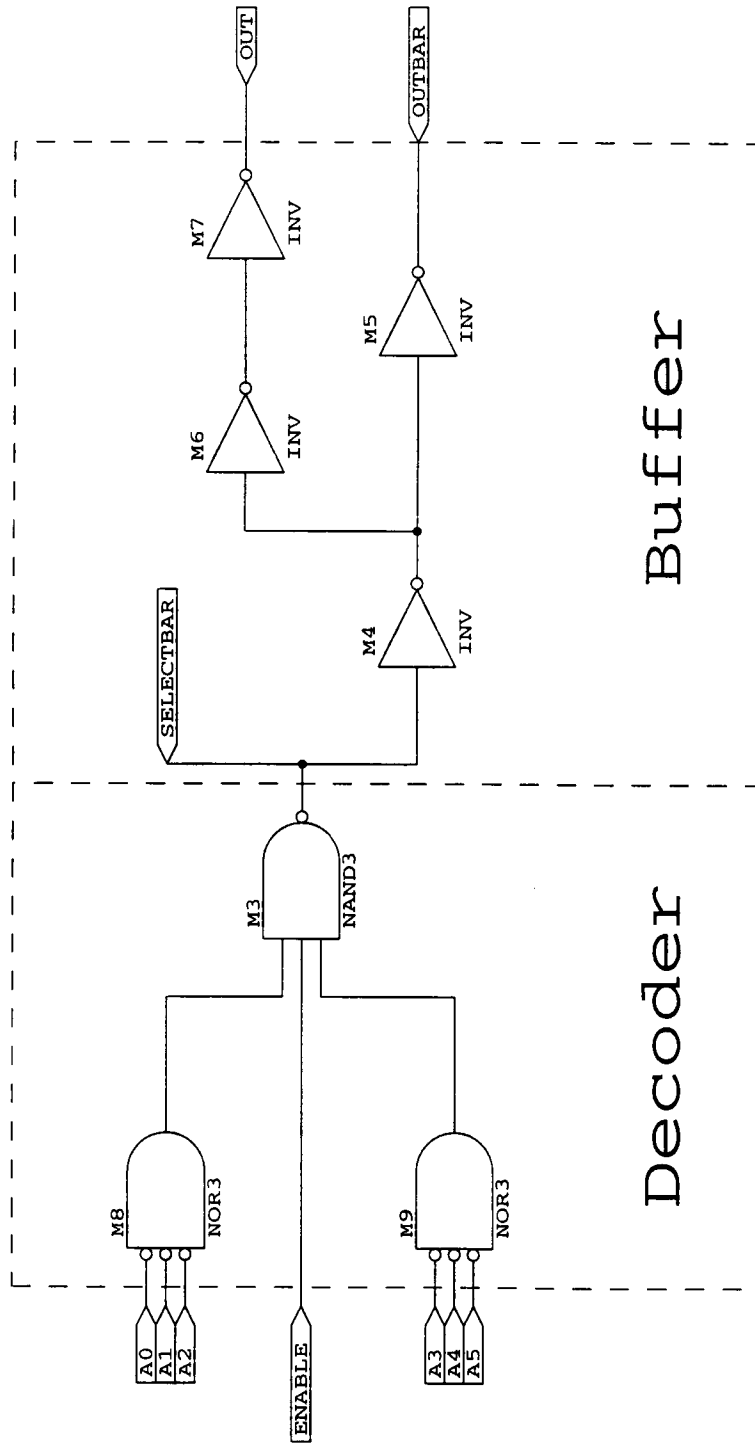


Figure 4-36. Basic logic decoder architecture.

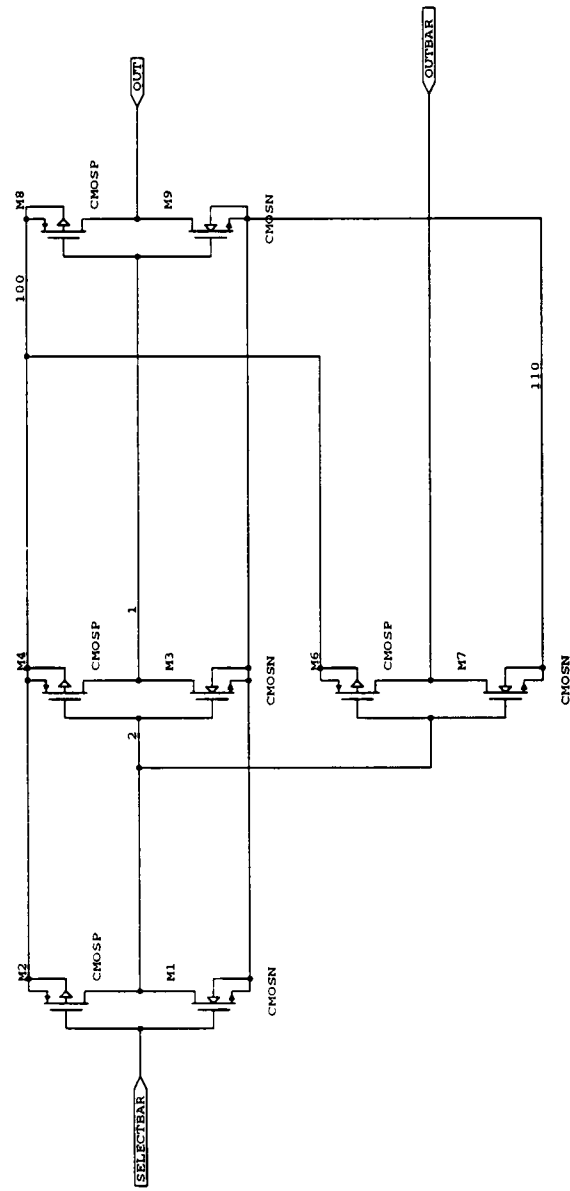


Figure 4-38. Schematic of inverter.

V. PEDESTAL CORRECTION

The actual implementation of systems utilizing analog memories are typically large detector systems having hundreds or thousands of channels. The signals being sampled by the memories come from a preamplifier of some type which is in turn connected to a detector. The detectors that are associated with a given analog memory chip typically have some spatial correlation (i.e., they are near each other). This means they share cable bundles and power supply grounds and therefore, to some extent, noise. A method of correlated noise cancellation would therefore be valuable [WALK1, FREY]. The type of noise associated with the front-end chips (in addition to inherent device noise) is normally system noise caused by the nearby digital control and conversion. This noise can be synchronized to the beam clock. The beam clock is the master clock derived from the times when the counter-rotating beams of particles are forced to collide with each other.

Some discussions have taken place concerning the best way to cancel noise in the detector chains. One approach is to use differential preamplifiers and memories for storage as shown in **Fig. 5-1** [SIP3, HAL2]. This introduces the problem of doubling the number of memory cells required for the system. An optional approach [SIP2, PAF1, HAL2], shown in **Fig. 5-2**, would be to use a single pipeline as a reference from which other pipelines would be subtracted, thus introducing a quasi-differential signal. The unknown in this approach is the amount of correlation between a single pipeline and its neighbors. A further unknown is the change in any existing correlation as a function of radiation dose.

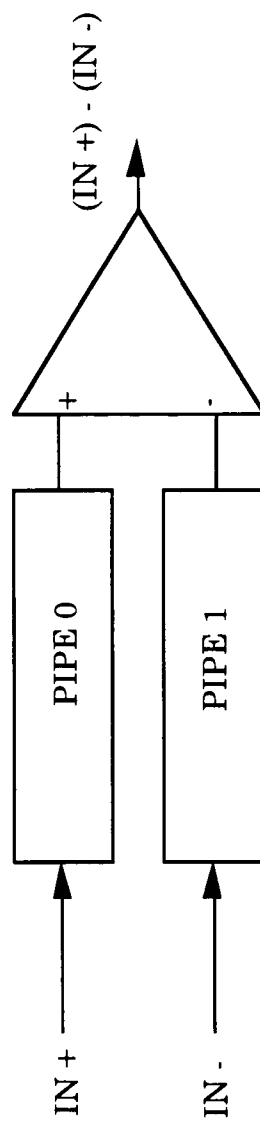


Figure 5-1. Differential readout.

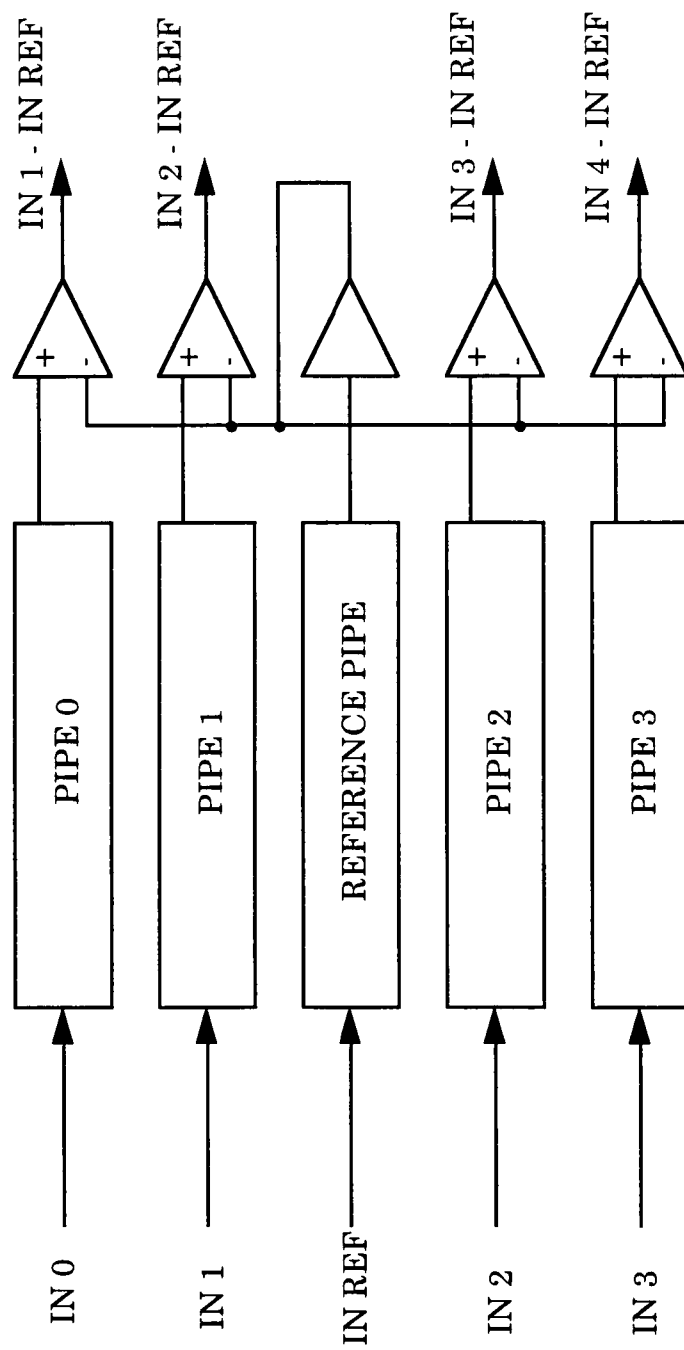


Figure 5-2. Modified differential readout.

The subtraction from a reference pipeline would reduce the effects of several sources of noise. The first would obviously be the pattern noise due to charge-injection from the local address logic. The second would be variations in the power-supply rails induced by switching logic both on and off chip. This type of noise will be especially troublesome in large systems because of the sheer number of gates switching at the same time throughout the detector. The third source would be the pickup noise from the input preamplifiers. The preamplifiers will typically be located next to the analog memories, but the detectors may be several inches away from the preamplifiers and connected by cables. The difference in location and the length of the input lines results in pickup of switching noise and ac power, especially in the case of charge-sensitive preamplifier inputs. The charge-sensitive inputs, as discussed in Chapter 2, have a gain set by the feedback capacitor. If a signal of any sort is present in the vicinity of the input, a very small amount of capacitive coupling can give rise to a significant output signal. For example, a coupling of 1fF between the input of a preamp and the output of a logic gate will inject 5fC for a 5V logic swing. This is a factor of ten larger than the smallest detectable signal for the PHENIX MVD preamplifier and a factor of 30 greater than the noise of the preamplifier. Obviously, this type of noise can seriously degrade the accuracy of the measurement.

If one channel of the preamplifier-memory system is used as shown in **Fig. 5-2**, and the noise pickup is identical in each channel, then perfect cancellation of the noise is possible. Unfortunately, there are several caveats regarding this approach. They are as follows:

1. *Unequal noise in each channel.* - If the noise pickup is different for some channels, the cancellation will be imperfect and could actually worsen the noise in channels. Channels in which there is a small amount of noise would, after subtraction from the reference channel, have whatever noise is present in the reference channel.

2. *Unequal gains in the preamplifier prior to the memory.* - This would have the same effect as 1.

3. *Uncorrelated noise between channels.* - This noise is due to the device noise present in all preamplifiers. The net effect of this noise is to increase uncertainty by the geometric addition of two uncorrelated noise sources or

$$e^2_{total} = e^2_{source1} + e^2_{source2} \quad (5.1)$$

For two well matched preamplifiers, this would increase the rms noise by approximately 40%.

4. *Unequal pedestal contributions from channel to channel.* - Obviously, if the pedestal variations between channels are different, there will be a degradation in the effectiveness of the cancellation.

To address items 1 & 2, the channels need to be tightly grouped (physically) from the standpoint of the detectors, the cabling, and the input preamplifiers. Consistency in grounding is also extremely important. In particular, item 2 can be addressed by grouping channels to be corrected on the same chip as the reference pipeline. Item 3 is addressed by ensuring preamplifier

noise is as low as possible in the design. This will limit the achievable improvement using this technique. Item 4 is addressed by assuring the grouping of the channels to be corrected is as small as reasonably possible and by ensuring that channels are corrected by a pipe on the same chip.

Within the scope of this dissertation, the intent is to study only item 4 as a function of radiation dose. The plan is to irradiate with gammas an 8-channel, 16-cell memory prototype (referred to as the Thin Glenn memory) to be used in the PHENIX MVD . The change in pedestals on the chips and the pre- and post-rad correction using one channel as a reference will be studied. The goal is to give a basic understanding of the effectiveness of radiation effects upon the technique. Further work concerning items 1, 2, 3, & 4 will be performed as the real systems are developed for PHENIX.

VI. TEST RESULTS

A. *GEM AMU*

Prior to beginning the testing on the memories, we had been warned by others who had devoted hundreds of hours testing analog memories that one could spend almost an entire career testing memories [SIPPACH, MARLOW]. With this somber warning in mind, we undertook the task of defining the appropriate tests that would yield the desired information. The GEM AMU tests were designed to evaluate the important operational aspects of the memories as a function of radiation dose. The tests are not intended to completely characterize the memory operation in a system. Testing to that extent would easily have taken four times as long or even more. The tests were intended to answer the following question: could a memory be built in a rad-hard process that could approach the desired performance characteristics. To this end, the tests were intended to address the areas of signal fidelity, address line noise, power dissipation, and yield. The measurements were performed at 0MRad, 1MRad, and 5MRad gamma dose. As stated in an earlier chapter, the detector would have seen a mixture of charged particles and gammas with a total dose of 2-3MRad. Gammas were chosen for testing because no other source was available. The 5MRad maximum was chosen because of the time required to irradiate and measure. Irradiation was performed at Argonne National Laboratory where the dose rate of approximately 82KRad/hr. was measured using Cobalt glass dosimetry.

The tests fall into two categories: static and dynamic. The static tests were performed with read and write addressing at two frequencies but with dc voltages as input signals. The purposes of these tests were to study the pattern

noise of the memory, the dc offset voltages of the readout amplifiers, the dc integral non-linearity (INL) of the capacitor cells and the readout amplifier cells, the capacitor cell droop rate, the noise, nearest neighbor interaction, and the stability of pedestal correction. The dynamic testing primarily involved the measure of INL for a real 50ns peaking-time pulse. The details of each test will be discussed as the data is presented.

A block diagram of the test setup is presented in **Fig. 6-1**. The AMUs were socketed in a test board that allowed connection to the LeCroy 9112 Arbitrary Function Generator, a National Instruments AT-MIO-16X Data Acquisition Card, and a read control board. The 9112 provided the memory writing vectors to the test board, i.e., the control signals that actually addressed the memory for writing. The 9112 ran at a 10MHz address rate and at a 47.5MHz address rate. The read control board was a module that received a signal from the 9112 that indicated writing was finished and then output read addresses to the memory. The read and write timing is illustrated in **Fig. 6-2**. The National Instruments (NI) card provided the 16-bit DAC input to the test board and the 16-bit ADC for the test board analog output.

Two personal computers were used in the testing. The first was the main computational machine that ran the actual control and acquisition programs and processed the data. The second machine controlled the 9112 through the EasyWave software package. EasyWave allowed write-vector files to be created as text files and then downloaded to the 9112. It also provided a user-settable delay marker for triggering the 50ns semi-Gaussian input pulse.

The test descriptions will be presented along with the results and interpretations. A chip photograph is presented in **Fig. 6-3**.

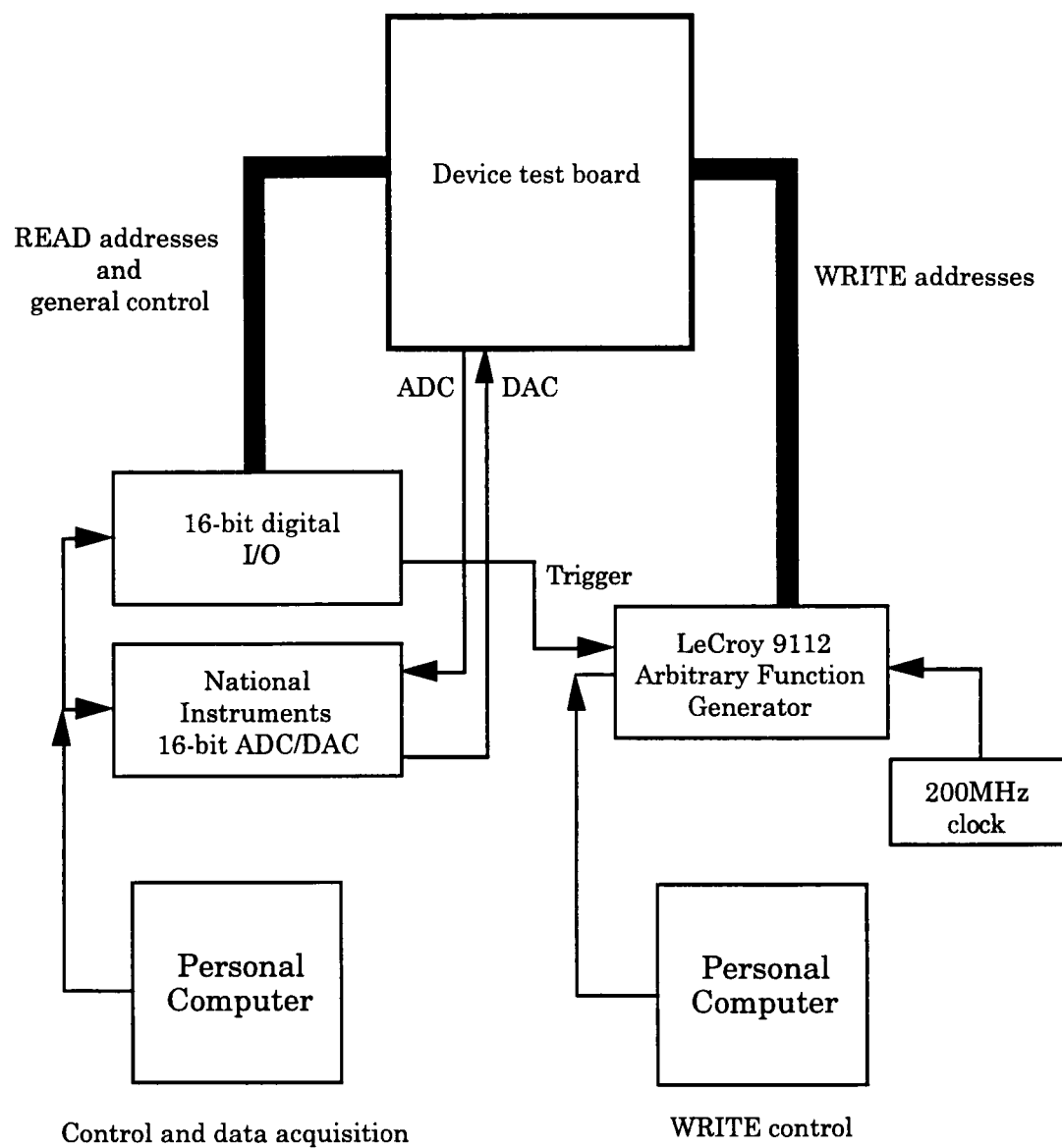


Figure 6-1. Block diagram of test system.

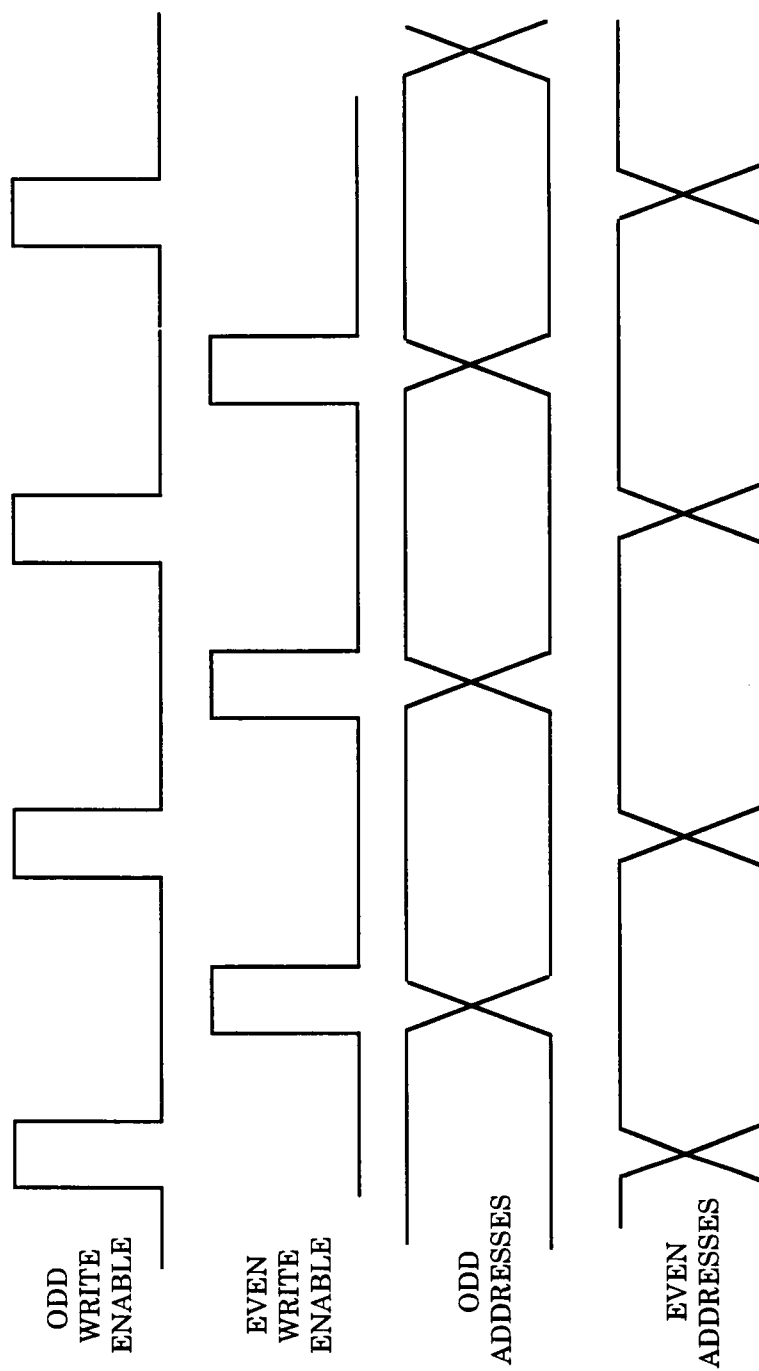


Figure 6-2. Relative READ and WRITE Timing.

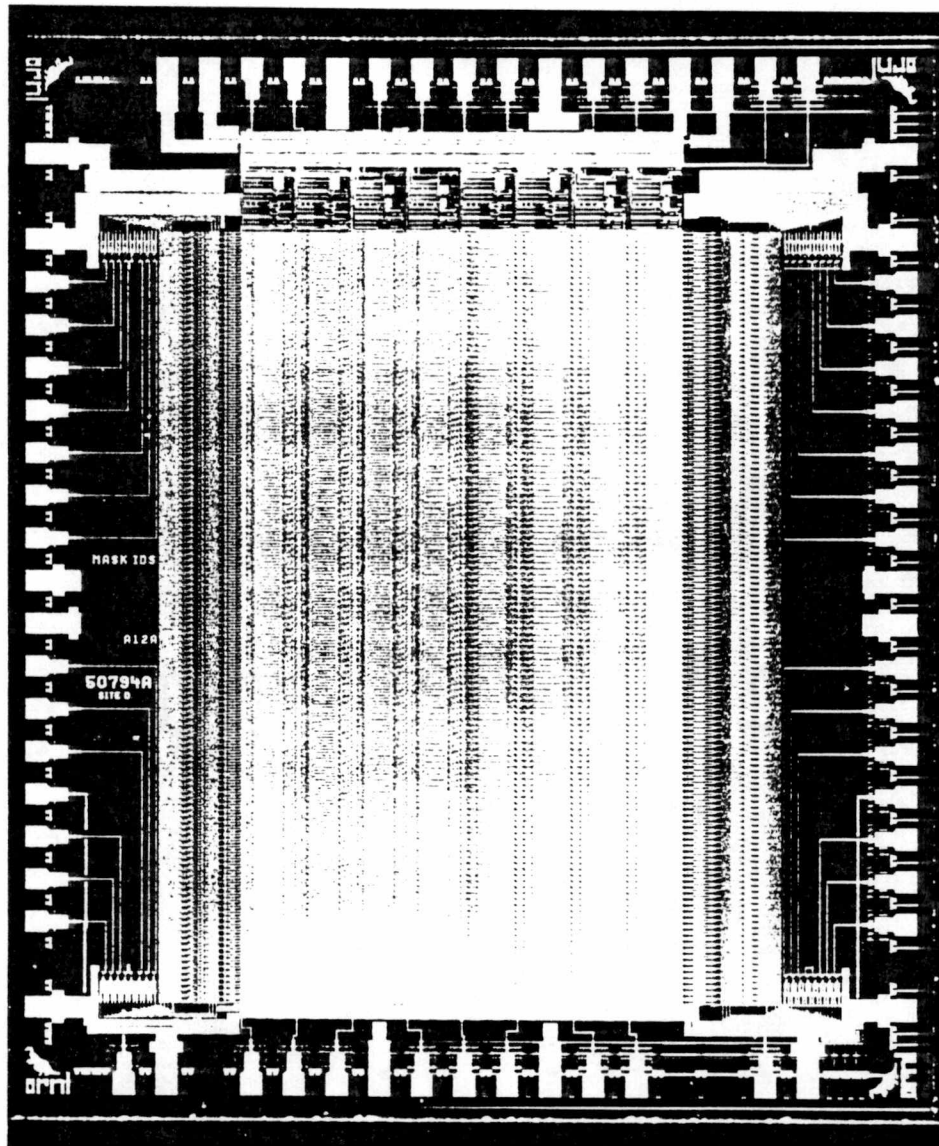


Figure 6-3. Chip photograph.

1. Static testing

a. Input offset voltages, risetime, slew-rate The purpose of the input offset test was to determine the static input offset voltage of the readout amplifiers. The device under test (DUT) was set up to have the amplifier resets active and the read and write clocks turned off. The non-inverting inputs of all the readout amplifiers were internally connected together at design time and for this test (and for normal operation) the non-inverting input was set to approximately +2.5V. This voltage was chosen to allow a single voltage at which the input stages of both output amplifiers would operate. For a perfect amplifier, the output should be at the same voltage as the non-inverting input if the reset switches are turned on. The reset condition with the input offset voltage modeled as a voltage source is shown in **Fig. 6-4**. The setup of the test was to first run the board with the differential inputs of the National Instruments (NI) board both tied to the +2.5V supply. This was to measure the systematic level-dependent offset of the NI board. The offset of the NI board was found to vary 1-2mV each time a new measurement was made. Because the measured amplifier offsets were on the order of one millivolt, the systematic NI offset value was then subtracted from each amplifier measurement.

Two sets of data are presented. The first, presented in **Figure 6-5**, are the actual pre-rad offsets for each channel of chip D99. Pipes 0,1,4, and 5 are the IPC4B amplifiers, and pipes 2, 3, 6, and 7 are the IPC5C amplifiers. The only consistent grouping of offsets were pipes 0 and 1 (IPC4B). The peak difference for all chips was approximately $\pm 4\text{mV}$. The IPC4B mean was -1.4mV with a σ of 1.76mV while the IPC5C mean was $+0.23\text{mV}$ with a σ of 2.1mV .

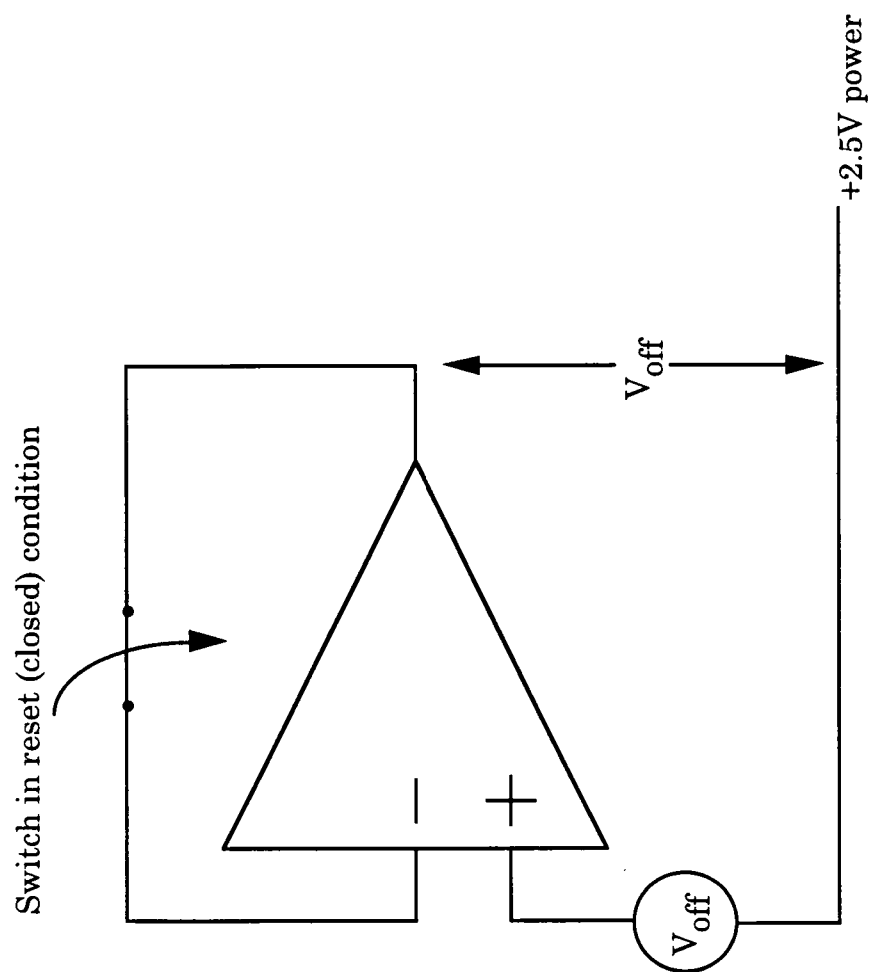


Figure 6-4. Readout amplifier with lumped input offset voltage.

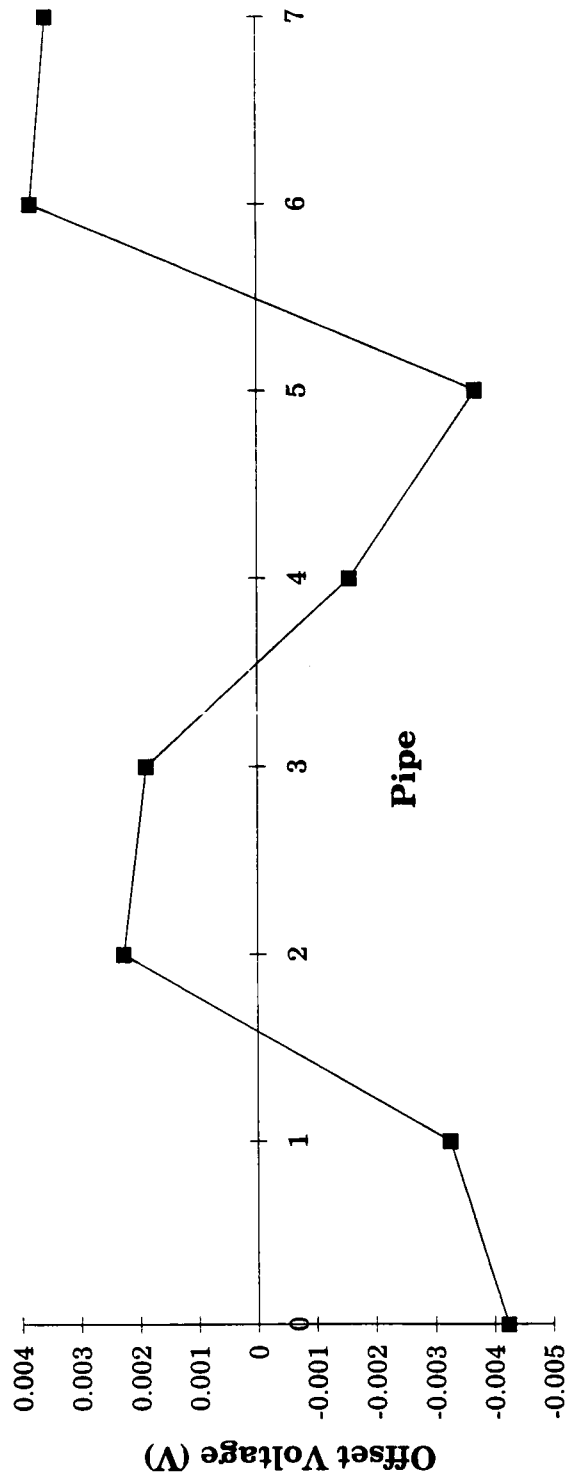


Figure 6-5. D99, prerad absolute offset.

The change in offsets relative to the 0MRad initial offsets are presented in **Figure 6-6**. The worst variation appears to have been 5mV which would indicate the amplifier designs are very stable in this process with respect to radiation damage. Because the variation is small, systematic, and would appear equal for every cell in a channel, the absolute value is unimportant to the operation of the memory. The value is important in the sense that even though the threshold voltages are changing several hundred millivolts as the radiation dose increases [THOM1], the tracking between the differential input devices is within 5mV. This indicates that indicates that, because of apparently good device tracking in at least a local area, some degree of radiation resistance can be designed in to the circuit.

The large-signal (2.25V) risetimes and slew-rates are presented in **Table 6-1**. These were taken by reading a 2.25V input signal with an output '0V' level of 2.5V thus resulting in an output of between 0.25V and 4.75V. The most interesting feature of this is that the IPC5C appears to be the most radiation tolerant of the two amplifiers. Because the major change seen is in the risetime, it would appear that the IPC5C is more resistant because the PMOS input device exhibits less change during irradiation and therefore the gain-bandwidth product exhibits less change than the IPC4B which has an NMOS input device. The PMOS devices were indeed found to have less change in g_m than the NMOS devices [EJK2].

b. Integral non-linearity Integral non-linearity (INL) is a measure of the deviation of the actual output from the expected output as a function of amplitude and is expressed as a percent of full-scale range. A perfect

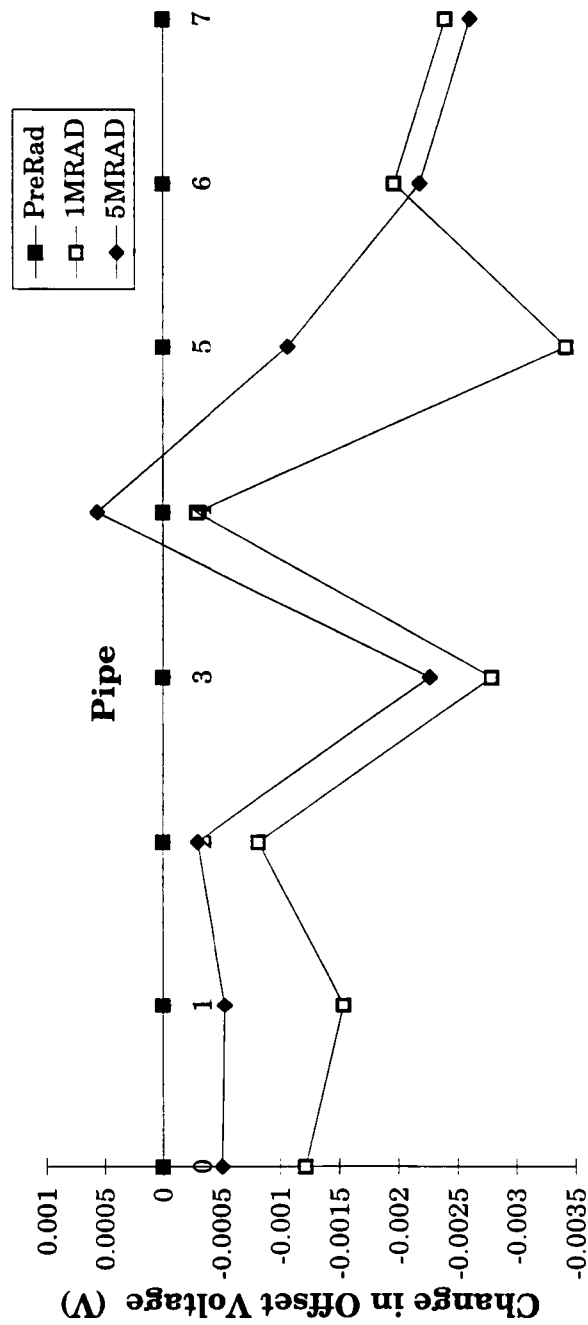


Figure 6-6. D99 offsets for 0,1, and 5MRAD.

**Table 6-1. Measured slew-rates and risetimes for the IPC4B
and IPC5C amplifiers.**

	'4B 0MRad	'4B 1MRad	'4B 5MRad	'5C 0MRad	'5C 1MRad	'5C 5MRad
+Slew (V/μs)	15.3	15.3	15.7	17.3	17	16.9
-Slew (V/μs)	15.6	15.7	16.7	16.8	17	16
VWVR + t_r (ns)	157	166	185	132	134	134
VWVR - t_r (ns)	183	188	205	145	142	145
VWCR + t_r (ns)	192	209	225	187	187	184
VWCR - t_r (ns)	193	218	242	186	190	187

amplifier would have an INL of 0%. The procedure used to measure INL for our tests is as follows:

1. Input a known voltage in 0.25V steps starting at 0V and ending at 5V.
2. Measure the output voltage at each step.
3. Perform a least-squares fit (LSF) to the output data.
4. Take the slope and intercept from the fit and use them, along with the input data, to find the expected data.
5. Subtract the actual output data from the expected output data.
6. Multiply the above result by 100 and divide by the full scale voltage.

The above can be expressed as

$$\%INL = \left[V_{ideal} - V_{actual} \right] \cdot \frac{100}{V_{peak}} \quad (6.1)$$

where

$$V_{ideal} = (m \cdot V_{in}) + b \quad (6.2)$$

m and b are slope and intercept respectively of the fitted output data, V_{actual} are the output values at each input voltage, and V_{peak} is the difference between the maximum and minimum output voltages.

The value of the static INL measurement is primarily to test basic dc properties of the memory such as capacitor matching, charge injection in switches, stray layout capacitance, and readout amplifier dynamic range without having to correct for errors due to charging effects between the sampling capacitor and the input switches. Because the least-squares fitting weights all points

equally in the calculation, points at the extremes of the input voltage range (points $< 0.5\text{V}$ or $> 4.5\text{V}$) can "skew" the fit for the middle points resulting in apparently high non-linearity for intermediate points. The data will be presented for LSF of three different ranges; 0-5V (5V scale), 0.5-4.5V (4V scale), and 1-4V (3V scale). Because the data for each chip is so similar, chip S99 even address will be presented.

Plate 1 (all plates are found in the Appendix) shows the pre-rad lower four pipes (pipes 0-3, VWVR) for 5V, 4V, and 3V scale respectively. The plots illustrate that the output amplifiers all begin to run out of dynamic range at approximately 0.25V from the respective power-supply rails. The IPC5C amplifier has consistently better performance at the positive rail than the IPC4B. For the negative rail, they are both about the same. This is believed to be due to the method by which the output drive is accomplished. For the '4B, both output drivers are heavily driven while in the '5C, the NMOS output (negative drive) is more heavily driven than the PMOS output (positive drive). When a transistor is turning on to drive, the saturation voltage V_{DSAT} increases due to the increase in V_{GS} . This reduces the allowable linear range of the transistor thus potentially reducing the linear range of the amplifier.

The linearity of the upper four pipes shown in **Plate 2** (pipes 4-7, VWCR) appears to be worse than the lower four. The slope of the gain, however, shows that the VWCR pipes have a gain of approximately 1.17 associated with them so that the input range is reduced by approximately the same amount. If this is considered, the VWCR linearity is seen to be quite comparable and even somewhat better at the end approaching 0V for the input.

The 5MRad data is shown in **Plate 3** for the VWVR pipes and the VWCR. Comparing to the 0MRad data, the lower voltage linearity has improved somewhat indicating there may have been some systematic measurement error associated with pipes 0 and 3. The 1MRad data, although not presented here, indicates that the linearity had also improved, thus further strengthening the hypothesis of systematic error. There does appear to be a slight worsening of the linearity near 5V at 5MRad, but it is not a major problem because it remains less than 0.5%.

The slope of the LSF is presented in **Table 6-2** for 0, 1, and 5MRad exposures. It is obvious that there is little change in the gain up to 5MRad. The gain of the lower four pipes (VWVR) would be expected to show little if any change because the output voltage is actually the input voltage stored on the capacitor plus any injected charge. The upper four pipes (VWCR) are more sensitive to component variation because the gain depends upon the ratio of the input capacitor to the feedback capacitor.

Table 6-2. Linear least-squares-fit slope for 0, 1, and 5MRad data of chip S99 even addresses.

<u>DOSE</u>	<u>P0</u>	<u>P1</u>	<u>P2</u>	<u>P3</u>	<u>P4</u>	<u>P5</u>	<u>P6</u>	<u>P7</u>
0MRad	.998	1.00	1.00	1.00	-1.20	-1.20	-1.21	-1.20
1MRad	1.00	1.00	1.00	1.00	-1.20	-1.20	-1.21	-1.21
5MRad	.999	1.00	1.00	.998	-1.19	-1.19	-1.20	-1.20

c. Droop Droop is the disturbance of the stored voltage on the sampling capacitor by either leakage due to the drain-source diodes of the switches or leakage through the switches themselves. Both sources of leakage were discussed in Chapters III and IV. The droop performance was one of the less obvious factors in the specification of the design. With a system that might require samples to be held for as long as 40 μ s, droop became a major concern. For an 8-bit system, 12mV is one bit for a 3V full scale (12mV in 40 μ s is a 300V/s leakage rate). After receiving some preliminary leakage data from Harris, the concern was raised that junction-diode leakage of the switches might degrade the stored charge after irradiation.

The measurement procedure was to write a dc voltage to a cell, wait some fixed time, and then measure the stored voltage. This was done for two input voltages, 0.75V and 4.25V. These voltages were chosen because they are just inside the linear range of the VWCR cells. The measurement times were 0s, 0.5s, and 1s. Cell 5 and cell 50 in each pipe were measured with the results being similar.

The results were quite impressive. The amount of data taken was large so that only a small fraction of it will be presented here. The data for chip D4A, cell 50 are typical and are shown in the following **Plate 4**. In summary, the worst case droop at 5MRad total dose was less than 2V/s while most were less than 0.5V/s. This gives less than 40mV/40ms period which is droop acceptable for a 15-bit system. This data was taken for VDS $\sim$ 0V. The circuits were retested approximately 5mos. later after being kept in a freezer to minimize annealing and periodically cycled to room temperature. The retest was done for VDS = $\pm$ 1.75V. The results were essentially the same.

d. Pedestals The pedestal testing generated data that showed the differences in pattern noise for various addressing modes. The memories were addressed at 10MHz and at 47.5MHz. For each of these rates, the addresses were input as binary and as Gray code [FLO1]. The Gray code is an unweighted code that has a single bit change from one code value to the next. The term "unweighted" means that the binary value of any code is not numerically proportional to the number it represents. The number of edge transitions made by a binary address ranging in value from 0 to 2^n and back to 0 can be seen by inspection to be $2^{n+1}-2$. In contrast, a Gray code will produce 2^n transitions for the same conditions. The ratio of the number of transitions is then

$$\frac{\#binary}{\#Gray} = \frac{2^{n+1}-2}{2^n} = 2 \cdot (1 - 2^{-n}) \quad (6.3)$$

If $n=6$, the ratio is 1.97. The average current through a capacitor [GRE4] is given by

$$i_{cap} = C \cdot v \cdot f \quad (6.4)$$

where C is the capacitance, v is the difference between the power supply rails, and f is the frequency at which the capacitor is charging and discharging between the rails. If f is reduced by a factor of two, the amount of current being pumped into the substrate should be reduced and this should result in less disturbance in the storage capacitors.

The first data presented is chip D99, 10MHz and 47.5MHz binary write, even addresses, readings averaged and single shot. The "averaged" means that

the cell was written to and then read 100 times, the results of which were averaged. The purpose of this was to remove the random uncorrelated noise. The single shot is simply write all cells, read even and odd cells n , write all cells, read even and odd cells $n+1$, etc. This would include all noise. The inputs were dc at three voltages; 1.5V, 2.5V, and 4.5V. The first set of data is shown in **Plate 5** (even and odd upper and lower pipes for 1.5V input).

The data has several important features which must be discussed. The first is the systematic pedestal or "tilt". For 10MHz, the tilt is lowest at the end containing cell 0 and gradually increases from there. For the 47.5MHz data, the tilt is just the opposite. The tilt can reasonably be explained as the result of two different mechanisms. The first is processing variation of the oxide thickness. This will have a greater effect upon the upper pipes than the lower pipes because the upper pipe gain of each cell is the ratio of that cell capacitance to the fixed feedback capacitor in the readout amplifier. If there is a gradient to the dielectric thickness, the gain will vary accordingly for the upper pipes. To a first order, the lower pipes should be immune to this effect because the gain of the pipes is independent of the capacitor value. The second mechanism is a heating effect due to increased writing rate. This is further supported by noting that there is a difference between the single shot mean and the averaged mean.

The even data exhibits "spikes" at addresses corresponding to 2^n-1 . This can be explained to be due to the changing of the odd write addresses at that time. The odd write address changes from n to $n+1$ when the even address value is n and is being written to. Because the maximum number of bit transitions occur when addresses change from 2^n-1 to 2^n , it is not surprising that the even data would be disturbed when the odd has it's maximum number of transitions. The

odd addresses, on the other hand, exhibit the same kind of disturbance except at addresses of 2^n . This is when the even address is changing from 2^n-1 to 2^n . The basic data thus appears to be consistent with the environment of the memory.

The even and odd upper pipes illustrate somewhat anomalous behavior. The tilt for the even data is going in the opposite direction from the odd data for the 10MHz writing rate. Because the cells at a given even and odd address are physically next to each other, any processing differences should affect each almost identically. There is clearly some other effect which affects the response. The most probable effect is the location of the drive circuitry for the decoders. **Fig. 4-2** shows the spatial layout of the drive buffers on the chip. The current flow is opposite for the even with respect to the odd because of the location. This can cause voltage drops through the supply lines and thus disturb the drive voltage to the capacitors. The power connections to the chip were varied in an effort to see if supply flow to the pins had an effect. The major effect was to change the amount of spiking seen, but there was little if any variation in the tilt. The exact cause of this is very difficult to isolate without another fabrication run, so that a definitive cause can not really be stated. The consistent data would seem to indicate that the capacitors near the 0 address end of the D-chip (the inputs) have a greater value (thinner oxide). This would explain the greater value of output for a given input at the lower addresses. The same effect is seen on the S-chip.

Single shot data was taken by writing to the memory, reading cell 0 odd, writing, reading cell 0 even, writing, reading cell 1 odd, etc. (no averaging took place). As can be seen, the results are somewhat worse. The main features seen in the averaged data remain the same, but the extremes are worse. Close

inspection reveals that the upper pipes appear to retain more similarity between averaged and single shot than do the lower pipes.

The 2.5V input data (averaged) are presented in **Plate 6**. Whereas the 1.5V data should be dominated by the NMOS response (the PMOS is almost off) and the 3.5V data by the PMOS response (the NMOS is almost off), the 2.5V data should be an "average" because both of the transistor types in the switches are on by approximately the same amount. In general, the data looks as expected. The tilt of the channels showed little change except that the amount present in the upper channels appeared to have reduced somewhat. Some spiking in the single shot data is apparent and appears to be due to some form of system noise because it is not always present.

The 3.5V data is presented in **Plate 7**. This data shows what is believed to be some socket contact problems. Some of the averaged data exhibits what appears to be a "step" around cell 55-56. We had experienced some socket contact problems at other times using the 68-pin ceramic leaded chip carriers. This was not apparent on any of the single shot data. The trends in the data remain apparent as there appears to be significant increase in the tilt of the upper pipes. This would lead to a preliminary conclusion that some of this tilt is due to operating point-dependent charge injection.

The data for chip S99 is presented next. **Plate 8** are the data for the odd and even pipes at 10MHz and 47.5MHz. With the exception of odd cell 36 apparently being bad, the structure looks quite similar to D99 odd lower. The even lower also looks similar to D99 even lower. There appears to be little difference from a perspective of spatial correlation. As stated earlier, cell 0 of S-chips odd corresponds to the same location as cell 63 of the even and odd cells in

D-chips while odd cell 63 and even cell 0 of S-chips corresponds to approximately cell 32 of odd and even for D-chips. The respective regions appear to be relatively flat (little tilt). The odd uppers appear to have a slight tilt upwards while the even uppers appear to have much more (almost twice) tilt. This, when compared with the D99 data, is consistent with some amount of systematic tilt being due to processing and some being due to even-odd drive. The major problem appears to be with even pipe 7 on both types of chip. This pipe has consistently more tilt than any other and is also in the same spatial direction on both chips. This is probably due to processing variations next to the decoding logic.

The 2.5V data is presented in **Plate 9**. The odd data is similar to the D99 data, but the even data appears to be definitely better. The lack of tilt would indicate that the tilt seen at 1.5V is input voltage dependent and thus has some cause associated with the transistors. The difference between the upper pipe offsets at 10MHz and 47.5MHz is similar to that for the D99 chip. Because the lower pipes are grouped together as are the upper pipes, the probable reason is that there is some voltage drop along the power lines going to the even decoders. The even decoders are farthest from the power pins.

The 3.5V data are presented in **Plate 10**. The most obvious differences between the D99 and S99 in this set is the 10MHz upper odd. The S99 has much less tilt than the D99 which would correspond to the top half of the D99 odd addresses which is relatively flat. The S99 even uppers have tilt that corresponds spatially to the lower part of the D99 odd uppers. This would indicate some systematic processing-induced pedestal. Besides the increase in pattern noise at the 47.5MHz sampling rate, the data are similar.

There is a lot of similarity in the Gray code data, so only a small portion of it is presented. **Plate 11** show the data for 1.5V input. There are two major features of the data. The first is that much of the fine structure shown in the binary write data is absent from the Gray code data. This is an indication that the number of edges changing for any given code do indeed affect the stored voltage in the cells. There are still "jumps" in the Gray code data, but the regular nature of the location of the jumps is greatly reduced. The result of this in a real system would be manifested as a variation in pedestal level depending upon the amount of writing and the pattern of writing occurring after the event of interest.

The second feature is that the tilt is essentially unchanged. There is no improvement or degradation in the amount of tilt despite the order of writing the bits. The net result of both of these features is that for a real system that subtracts pedestals from data, the order of writing will have a minimal influence on the data due to pedestal tilt, but will definitely have an effect arising from the variation in writing history. This will be shown in later data.

A very small portion of the 5MRad data is shown in **Plate 12**. There appeared to be very little change in the memories after irradiation to 5MRad. The conclusion from this observation is that the basic process is stable enough from the standpoint of pedestal variation to allow standard techniques of pedestal correction to be employed in the IPC subsystem.

The next set of data are the pedestal subtraction results. This particular test is important because it tests the memory in a way that is very similar to the actual function of the devices. In this series of tests, the averaged pedestals for 1.5V, 2.5V, and 3.5V inputs are stored in an array. The memory is then run once (single shot) for all addresses for a 1.5V input, and the 0 address even and odd

cells are read and stored. The memory is run again and the 1 address even and odd are read. This continues until all cells are read. The single shot sequence is repeated for 2.5V and 3.5V. The single shot data is subtracted cell by cell from the averaged pedestal data and an rms is calculated for the even addresses and the odd addresses. **Plate 13** present chips D4A and S4A 47.5MHz Gray and binary typical raw 1.5V single shot data at a given input voltage for each pipe and the rms subtracted values for the single shot minus the 3 averaged pedestals. The data shows that even though the Gray code tends to show a reduced single shot pedestal rms, the subtracted pedestal is typically no better than the binary. The data also indicates that, in general, the VWVR cells exhibit less change as a function of input voltage than do the VWCR cells.

The 5MRad D4A 47.5MHz 1.5V binary data is presented in **Plate 14**. There is very little difference between this data and the pre-rad data. This indicates that the changes induced by the radiation damage are not drastically affecting the process characteristics that determine the systematic offsets. This is a very important finding because the major purpose of these chip designs was to determine if this process would support a memory that could be calibrated and used after radiation damage. If the changes did not make the memory unusable, the device would still be acceptable because the calibration cycles would likely occur several times each day and slowly changing systematic offsets would be subtracted from real data.

e. Nearest-neighbor interaction With pipelines having as close a proximity to each other as those in this memory, there was concern about readout interaction between the pipes. A test was performed that would expose any bias or operation-dependent crosstalk. Seven of the eight pipes were tied to 2.5V input

and the eighth had an input equal to 1.5V, 2.5V and 3.5V. The average pedestals were then calculated and compared at each of the 3 input voltages. This was done for each of the eight pipelines being varied. The output data for chip D99, even address, pipe 3 varied is shown in **Plate 15**. Series 1 data show output voltage for an input of 1.5V, series 2 an input of 2.5V, and series 3 an input of 3.5V. Ideally, one would like for all other pipes to remain unchanged despite changes in any given pipe. The detailed prerad data for pipe 3 and pipe 5 are shown in **Plate 16**. The scale is expanded about the mean values so that the extremes of the pipe being exercised are off scale. The tests of pipe 3 show a very slight (1-2mV negative) correlation of the VR pipes with increase in pipe 3 input voltage, but there is essentially no change in the CR pipes as pipe 3 increases. Exercise of CR pipes (pipe 5) shows a marked change (negative 4-5mV) in the CR pipes and a slight change in the VR pipes. It is interesting to note that the change in output voltage for neighboring pipes is opposite in sign to that of similar types (VR and CR) and the same sign for different types. In other words, VR increasing voltage results in a slight voltage decrease in other VR pipes and no change in CR pipes, and CR increasing voltage results in a greater decrease in other CR pipes, but a slight increase in voltage for VR pipes. At first, it was thought that this might be an artifact of the test fixture (dielectric absorption of the external input capacitor), but it was then realized that the input capacitor is connected to only one channel at a time and thus would not explain the results. The layouts of the capacitor cells give no clues because all cells in a pipe are isolated from each other by substrate and well plugs. The only explanation that appears to be consistent with the data is that when the cells are to be readout, all cells in a row are connected to the readout amplifier at the same instant. The VR cells are placed

across the readout amplifier but the CR cells are placed between the inverting amplifier input and ground. The output ground circuits are all tied together so that any disturbance on ground will affect all cells. The CR circuit functions by transferring charge from the sampling capacitor to the feedback capacitor of the readout amplifier. This transient is probably responsible for much of the disturbance seen by the CR circuits. This transient is absent from the VR cells because no charge is transferred upon reading the sampling capacitor. The 5MRad data is presented in **Plate 17**. There was essentially no change seen between the prerad and the 5MRad data. Pipe 0 appears to have some change but this is because it is inoperable after the irradiation.

2. Dynamic testing

The dynamic testing consisted of integral non-linearity measurements using a 50ns input pulse similar to that expected in actual use. The calculations used are identical to those presented for static INL. The input for the tests came from a BNC BH-1 Tail Pulser fed through a KAY 50W switchable attenuator. The attenuator was attached to an AD844 current-mode amplifier which served as an input to the analog memory. An AD844 was present on each input of the memory and served two purposes. The first was as a buffer-driver from the pulse generator-attenuator to the memory. The second was to allow a DC offset for the pulse so that an initial (no signal) quiescent operating point could be set. For the tests presented here, the operating point was set for 1V. This allowed the signal to range from 0V to 3.5V and still be within the operating range of the memory.

Obtaining a signal with 50ns peaking time with a high degree of linearity (>8bits) is a difficult task. In order to generate a system that would be useful in a

reasonable amount of time, we chose to go with the AD844 as a buffer for speed and characterize the linearity of the result.

The prerad data for chip S4A, even cell 6 is shown in **Plate 18**. The lower 4 pipes (VWVR) appear to have a slightly better INL than do the upper 4 (VWCR). The lower pipes do not appear to exhibit the same INL shape as does the pulser curve. This is probably due to both noise and charge injection of the cells. In contrast, the upper pipes appear to have more of the shape of the pulser. The effect is exaggerated when compared to the actual pulser curve. This is probably due to the worse INL of the CR memories. The data for 5MRad is presented in **Plate 19**. As can be seen, there is some change in the memories (in particular the VR cells), but the numbers appear to be similar to prerad.

B. Pedestal correction

The pedestal correction tests were run on the Thin Glenn memory which was designed as a prototype memory for the Multiplicity-Vertex Detector (MVD) in PHENIX. The memory is similar in architecture to the GEM memory except that it has 8 channels (or pipes) each 16 cells deep. The addressing is accomplished in the same manner as the GEM memory: an address is presented and the write enable is set true after the address has settled. The addresses are only 4-bits wide because of the 16 cell depth of the pipes.

The testing was implemented in the same test fixture shown in **Fig. 6-1**. The pedestal data was taken for input voltages of 0.5V, 1.5V, and 2.5V. The reason for the voltages being skewed towards the bottom end of the range is that this memory was designed for inputs from 0.5V up to 3.2V. A single pass was made for each cell and the result stored. A separate program then took the

resulting data files and ran subtraction of each cell from all other cells in a row, i.e., cells at the same address. In order to limit the amount of raw data, the testing as implemented assumed the random noise in the output stages of the readout amplifiers to be very small and pipe-pipe matching not be a function of readout amplifier variations. As seen in the real-time subtracted data, this assumption proved to be correct. This allowed the array to be exercised with all inputs at the same voltage thus generating the pedestal array data. While not exactly implementing real-time subtraction, it nevertheless resulted in a manageable volume of data adequate to study the pipe-pipe correlation vs. radiation dose. It should be noted that the data subtracting process for same value inputs (i.e., 0.5V-0.5V) does indeed implement the real-time subtraction and exhibited excellent correlation. Some data was taken in the real-time mode.

The data ultimately available included raw pedestal data at 0.5V, 1.5V, and 2.5V in, and subtracted data of 0.5V-0.5V, 1.5V-1.5V, 2.5V-2.5V, 0.5V-1.5V, 0.5V-2.5V, and 1.5V-2.5V. In addition, the tests were performed after the chips had received radiation doses of 0-, 25-, 50-, and 75KRad. There were three chips that were irradiated with gammas for approximately 70min. in a field of 22KRad/hr. The circuits were unpowered during irradiation with the leads electrically shorted together. The reasoning behind the choice of gammas was the same for this memory as it was for the GEM AMU. The availability of gammas made test facilities available. The radiation dose in the PHENIX detector had not yet been well characterized by the physicists, but 10-50KRad of ionizing radiation consisting of a mixture of charged particles and gammas had been predicted.

The results of the GEM AMU tests indicated that even different cell sizes across a chip would exhibit some matching and that cells identical by design

should exhibit very good matching. Further, the low pedestal change seen after radiation gave rise to the hope that even a non-radiation-hardened process might maintain reasonably good matching at low doses. That indeed appears to be the case. **Figure 6-7** shows the raw pedestal variance for 0KRad as a function of input voltage for chip #1. The variation is the calculation of the σ of the cells in a given pipe. The first and last cells are not included in order to remove variations due to location. Also, the LeCroy pulse generator had an anomaly that, in gated mode (one set of 16 write addresses per gating pulse), the first cell might not be addressed properly. The 1.5V input range exhibits the worst variation vs. pipe which is approximately 0.9mV between pipe1 and pipe 6. **Figure 6-8** shows the raw pedestals for 25KRad total dose. Notice that the pedestals had shifted down in value. This is the only one of the three chips in which this occurred. This is probably due to the global threshold shifting to values that injected either less charge or injected more equal amounts of complementary charge that canceled. It is obvious that the variation in threshold is indeed global and relatively uniform across the chip because of the 0.5mV maximum variation from pipe to pipe. **Figures 6-9** and **6-10** present the pedestals at 50KRad and 75KRad. There is obviously some variation between 50KRad and 75KRad. The pedestals are more tightly grouped than the 50KRad data. This leads to the observation that, even at a 75KRad dose, the circuits will track to some extent on a given die.

The subtracted pedestals for 0.5V-0.5V using pipe 1 are presented in **Fig. 6-11**. This figure illustrates a remarkable correlation between pipes. The difference in tracking between pipe 1 and any other pipe for a dose between 0KRad and 75KRad is approximately 0.5mV. **Figures 6-12** and **6-13** present the same conditions except pipes 4 and 8 respectively have been used as the

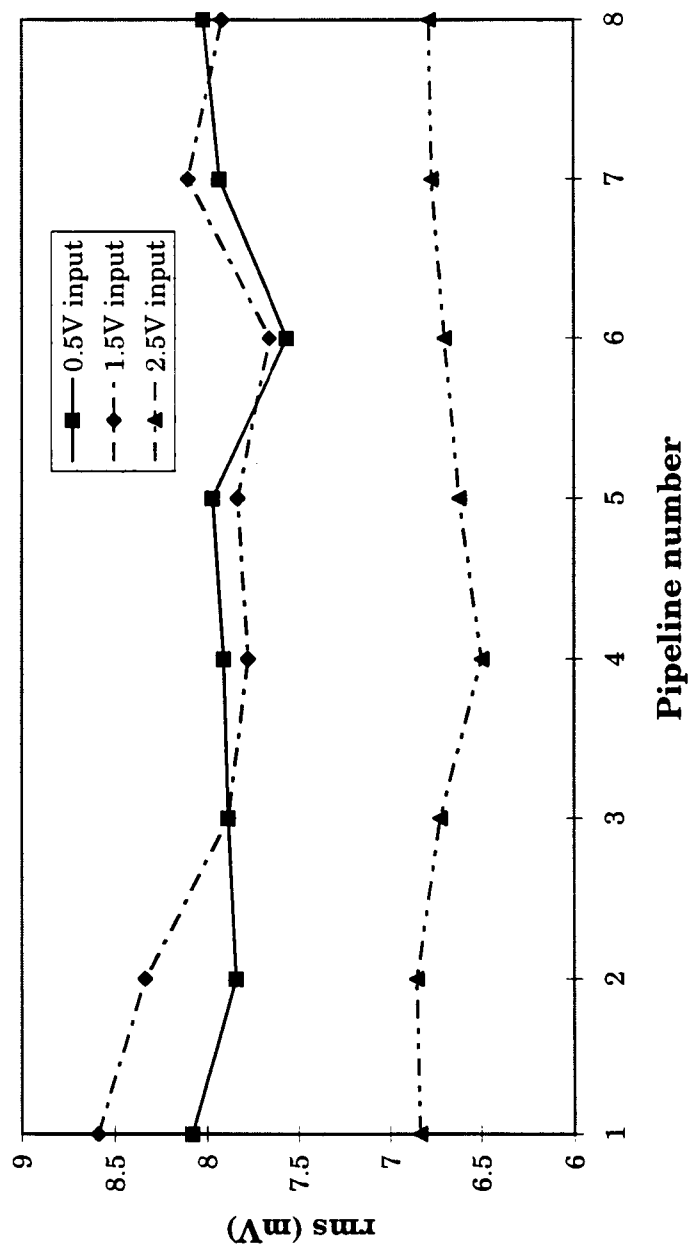


Figure 6-7. Thin Glenn chip 1, raw pedestals for 0 KRad.

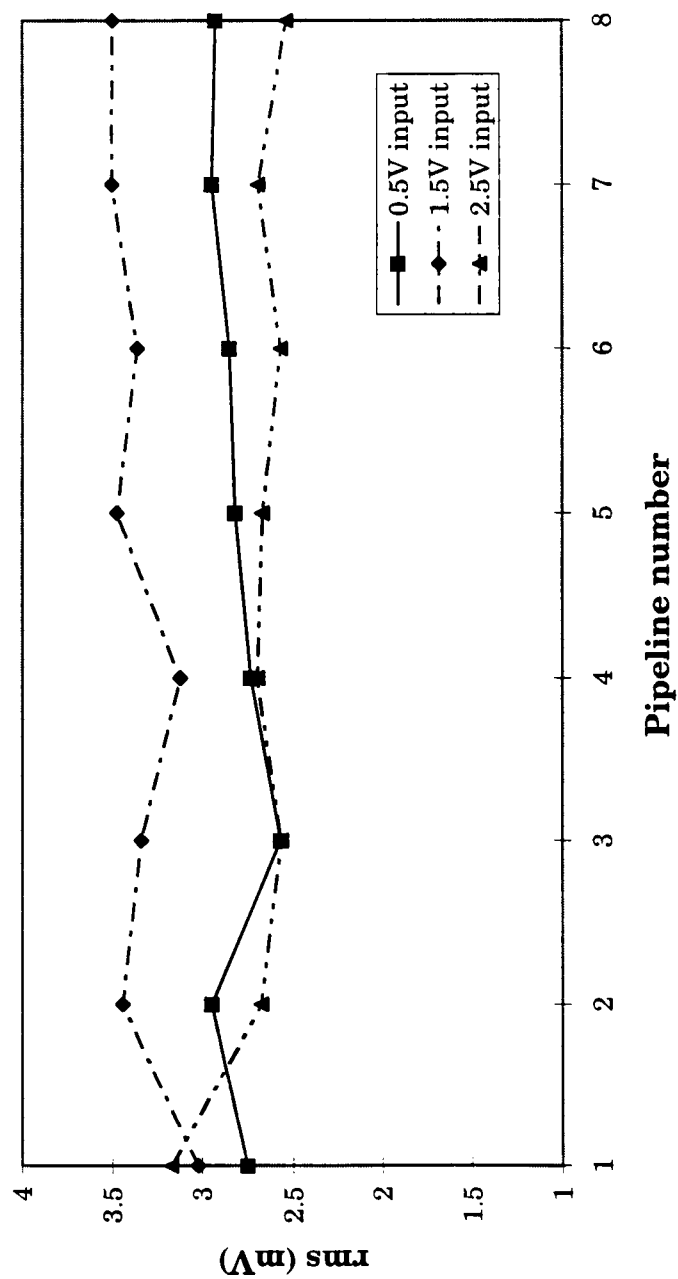


Figure 6-8. Thin Glenn chip 1, raw pedestals for 25 KRad.

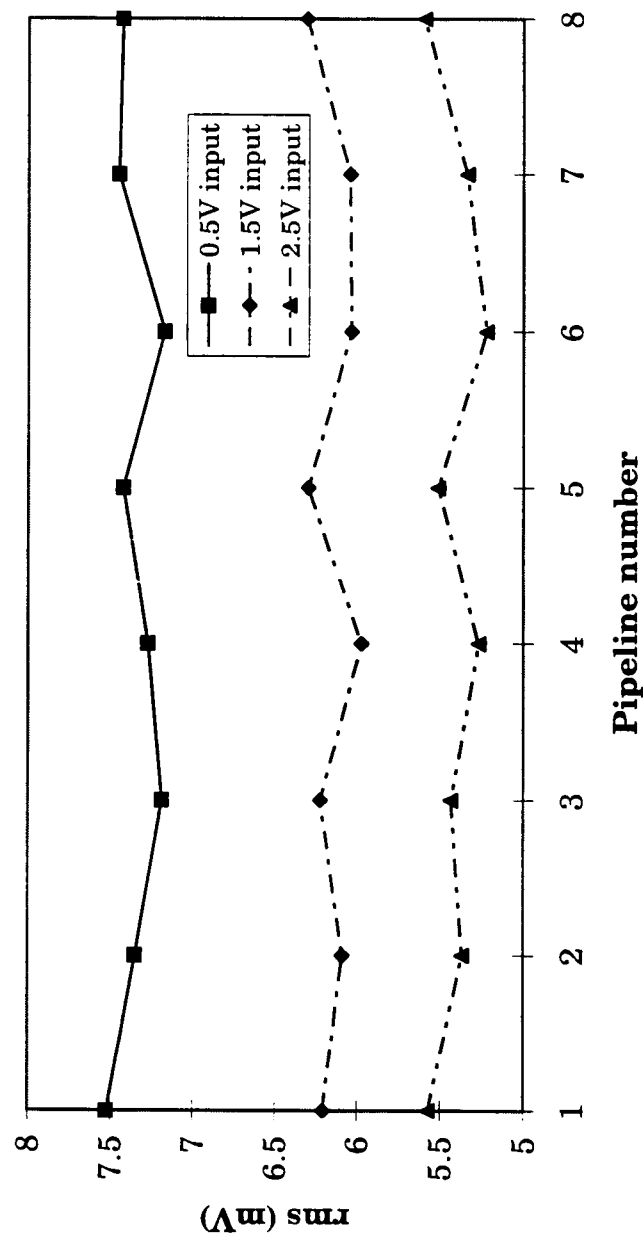


Figure 6-9. Thin Glenn chip 1, raw pedestals for 50 KRad.

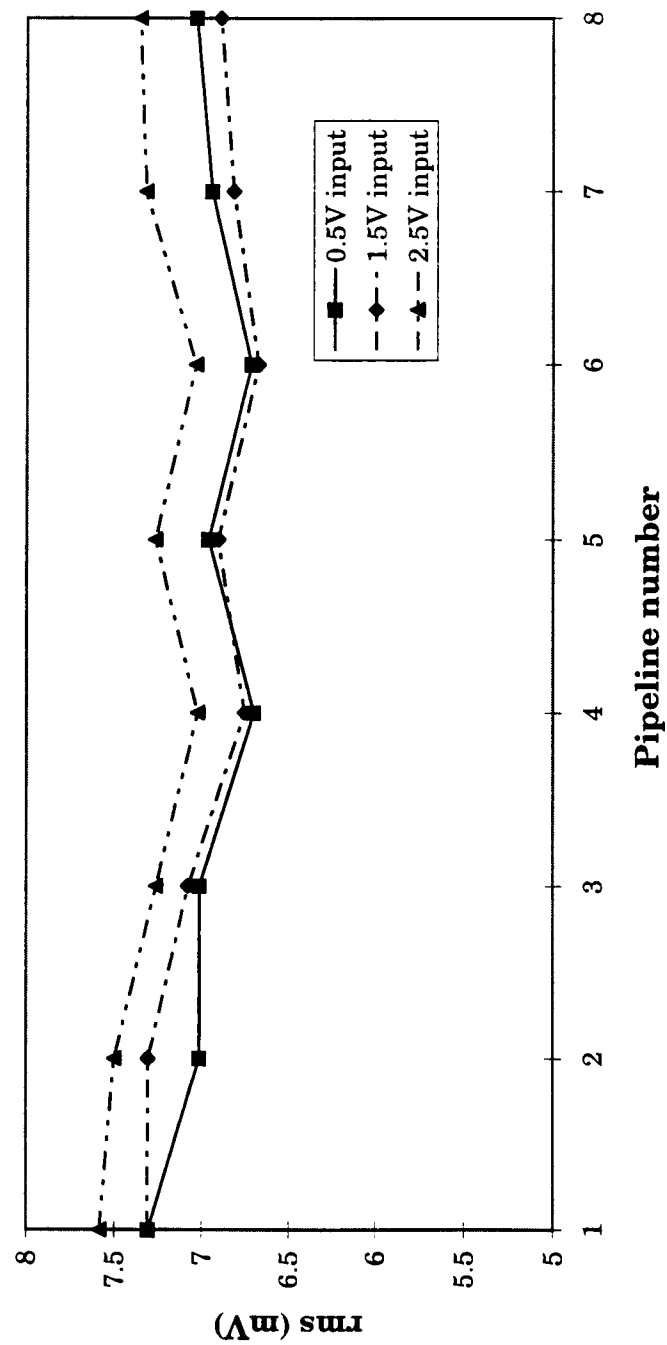


Figure 6-10. Thin Glenn chip 1, raw pedestals for 75 KRad.

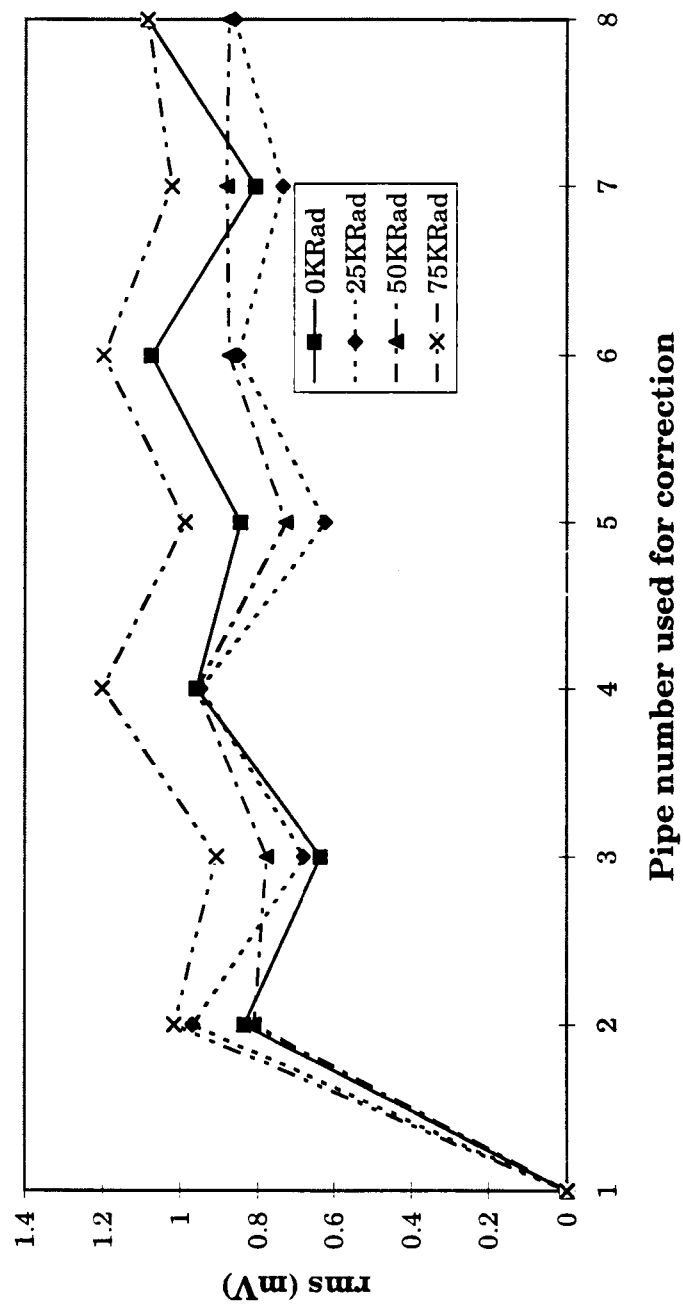


Figure 6-11. Thin Glenn chip 1, pipe 1 values, 0.5V-0.5V.

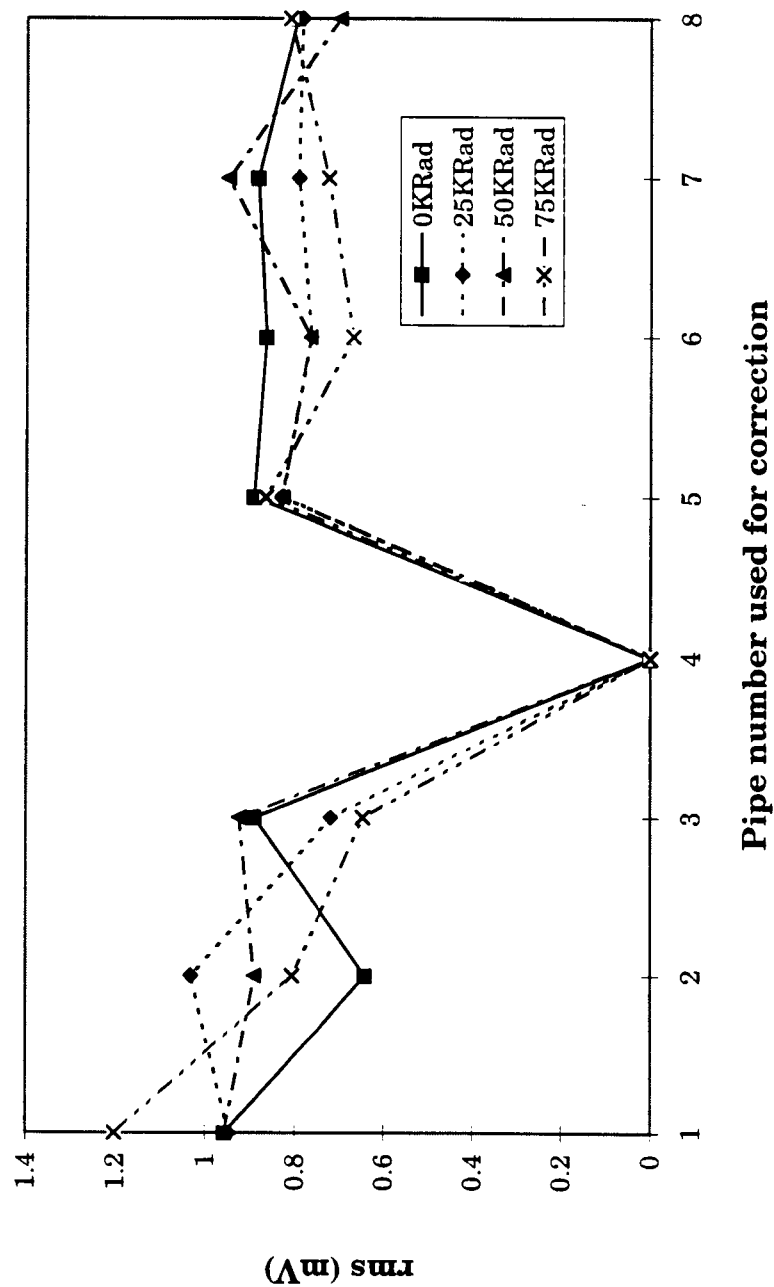


Figure 6-12. Thin Glenn chip 1, pipe 4 values, 0.5V-0.5V.

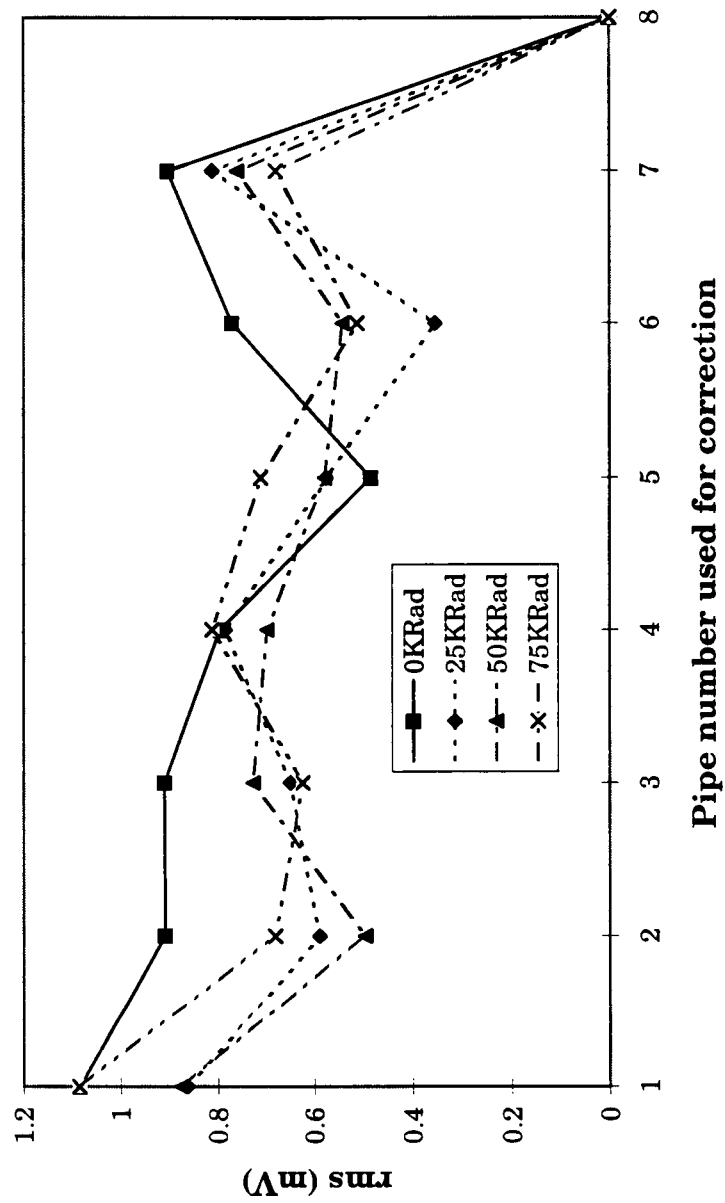


Figure 6-13. Thin Glenn chip 1, pipe 8 values, 0.5V-0.5V.

reference. The results are similar to that shown by pipe 1. This indicates that the spatial matching for the pipes appears to be very good for at least the 8 pipes on this chip. Such a large drop from raw pedestal values to subtracted values indicates that the pedestal variation is primarily due to systematic noise probably injected from the addressing as seen in the GEM AMU testing. Had there been a large amount of random noise between channels, there would be much more variation in the subtracted values.

Figure 6-14 presents the actual real-time subtracted data (prerad) for chip 8 with channel 4 used as subtraction reference. Each channel is then subtracted from channel 4. The input to channel 4 is held at a constant 0.5V while the other channels are run with 0.5V, 1.5V, and 2.5V inputs. The variation of channel 4 raw data is due to the finite output impedance of the opamp driving the channel while the other channels had a driving impedance of essentially 0 ohms. The results show that the pedestals are improved and exhibit less variation from channel to channel. **Figures 6-15 and 6-16** presents the results of chip 1 at 75kRad for channels 4 and 8 as references. This shows that a portion of the variance appears to be pattern related and that for a memory of this size, the channel location used for correction appears to be unimportant. One feature in all this data that needs to be noted is that the raw data variation exhibits more spread than the corrected data and that the radiation appears to have little effect on the ability of this technique to correct the basic pedestal variations.

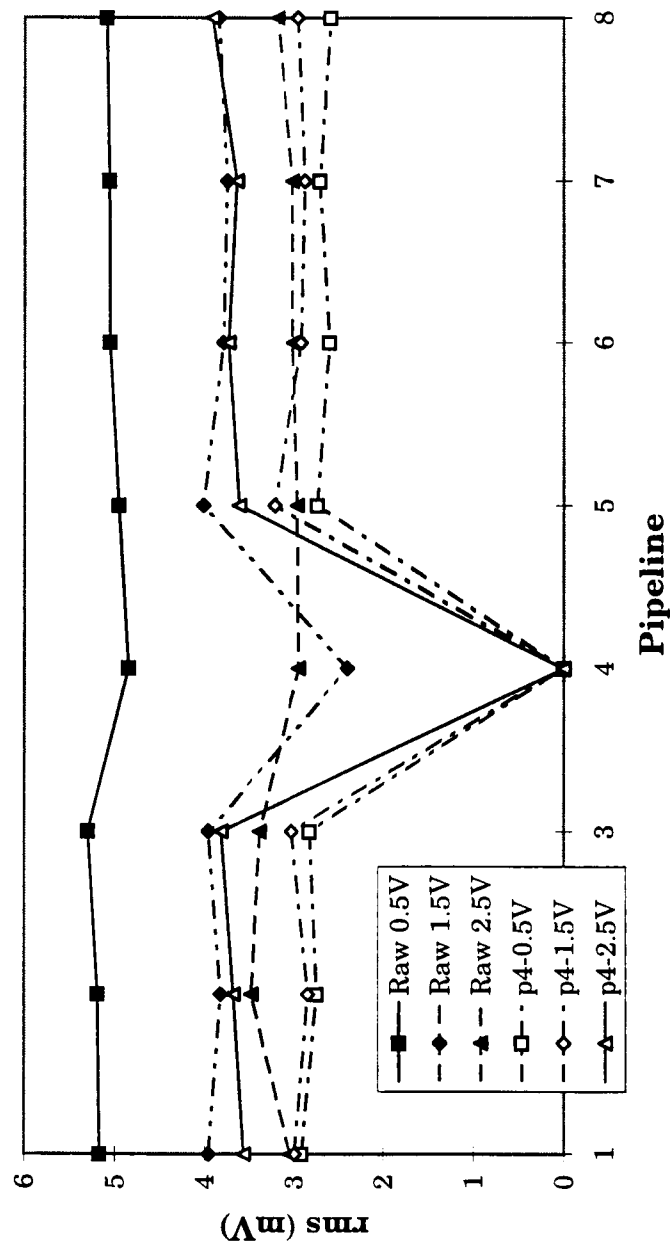


**Figure 6-14. Chip 8, 0KRad, channel 4 as reference
with 0.5V input.**

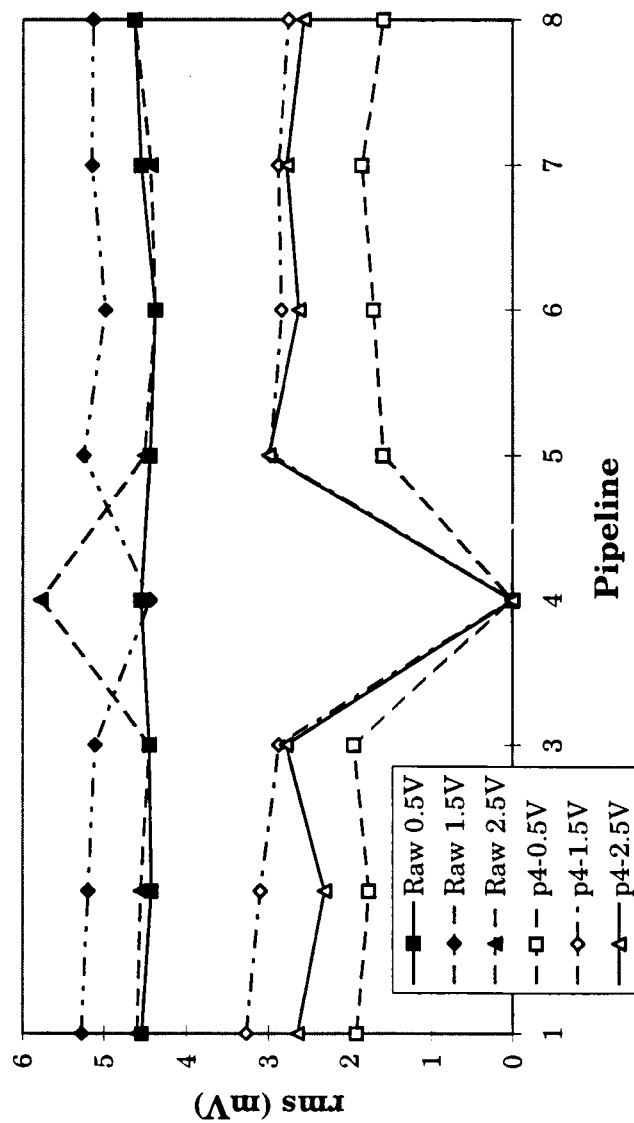


Figure 6-15. Chip 1, 75KRad, channel 4 as reference with 0.5V input.

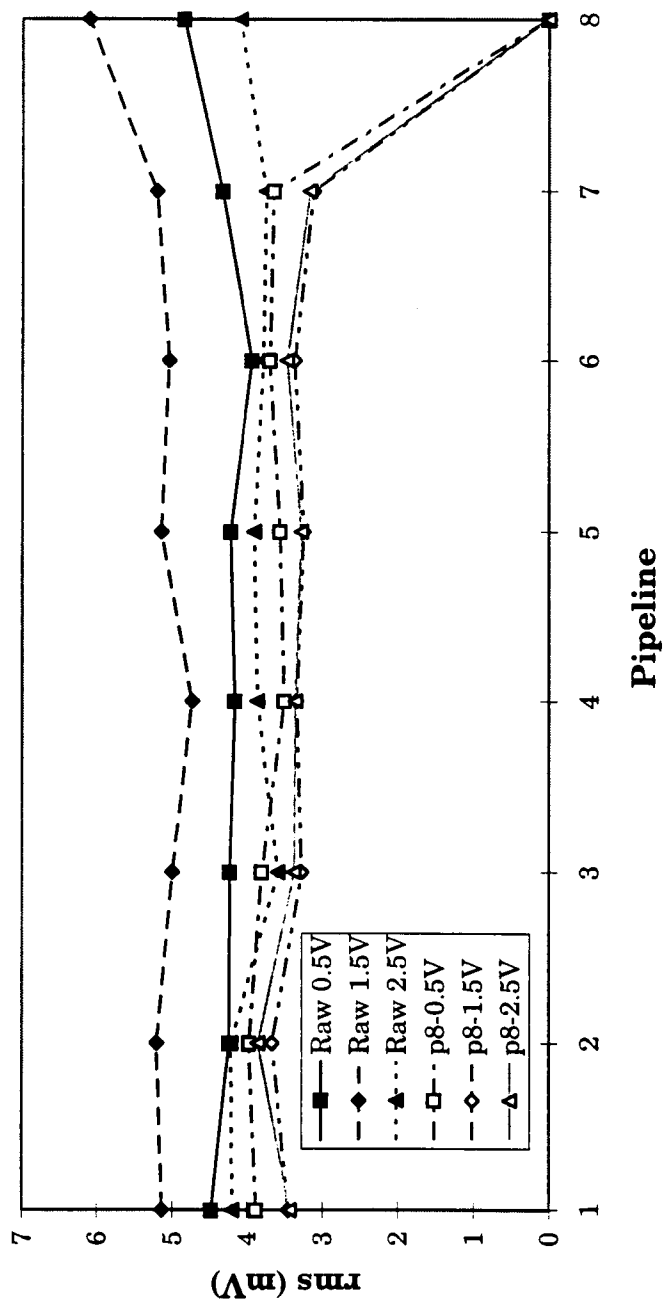


Figure 6-16. Chip 1, 75KRad, channel 8 as reference with 0.5V input.

VII. SUMMARY AND CONCLUSIONS

A. GEM Analog Memory design philosophy

The design of this analog memory unit (AMU) was undertaken to fulfill the requirements of the Interpolating Pad Chamber (IPC) subsystem of the GEM Central Tracker. Geometrical interpolation was employed for the operation of the IPC. This required a charge-sensitive preamplifier (CSP) for collecting the charge induced on the pads from the wires due to an event.

The analog memory sampled and stored the output from the CSP every 16ns and held the information until either the voltages due to a given event in the memory were read out and digitized, or written over by a subsequent event. The requirements of a CSP, an AMU, a multiplexer, and flash analog-digital converter (FADC) led to an early desire for a CMOS process that could implement the CSP, AMU, and multiplexer, and survive the harsh radiation environment present in the region of the IPC over the projected 10 year running life of the GEM detector. CMOS was an obvious choice since bipolar or GaAs processes were not suitable for analog memories due to the lack of adequate switches, the lack of choice of processes, and the generally expensive nature of the processes. It was not known, however, if a preamplifier suitable for the large detector capacitances could be built in CMOS. The main advantage of building the CSP and the AMU in the same process was primarily cost: it would be less expensive to share prototype fabrication costs between the two developments than pay for each individually if, for example, a bipolar process were chosen for the CSP and CMOS was chosen for the AMU.

There were several reasons for the chosen topologies. There had been

little if any work performed on rad-hard analog memories. It was unclear if any processes would work satisfactorily for the application of storing analog voltages for several tens of microseconds without significant deviation due to the effects of leakage currents. Irradiation generally produces an increase in p-n junction leakage currents which would add to or subtract from the stored voltage on the sampling capacitor.

B. GEM experimental needs

1. Linearity

From the basic detector resolution requirements, it was determined that the integral non-linearity (INL) required for the analog memory be on order 0.5% or better for the semi-Gaussian pulse output from the pad preamplifier. This was due primarily to the inherent measurement accuracy of the IPC concept being approximately 1%.

2. Readout Speed

The biggest contributor to the minimum readout time is the settling time of the output readout amplifier. The design goals were to have an 8-bit settling time of approximately $< 500\text{ns}$ for a 10pF load capacitance, while power dissipation should not exceed approximately 10mW . With the preamplifier design not finalized, the operating range was also not determined. The design of an amplifier was undertaken that would work as an inverter with the input at approximately mid-scale (2.5V out of 5V) and would allow an output range very near both rails (rail-to-rail).

3. Power Dissipation

The IPC detector required approximately 400,000 channels, each with its own preamplifier, AMU channel, and MUX channel. One FADC would be shared by 16 AMU channels. With the required linearity, it was decided that the power budget for the AMU would be 10mW/channel, maximum. This would result in approximately 4kW power dissipated due to the memories for the entire detector.

4. Addressing

For the reasons of simple interfacing, the preamplifier and the memory were made 'dumb': i.e., all control would be handled by a state machine controller that was a separate chip. Because the pipeline was to be 128 cells deep, this would require a 7-bit decoder. In order to ease the requirements of having cell enable logic able to settle every 16 ns due to the beam crossing clock of the SSC, it was decided to configure the decoders as two separate 6-bit decoders, each controlling 64 cells in a pipe.

C. GEM memory development

1. Topologies

a. Voltage-read The Harris Semiconductor AVLSI-RA process was chosen for this development for two reasons. First, the process had high-density capacitors as part of the standard processing steps. Second, ORNL had developed a good working relationship with Harris during a prior development that utilized the VHF bipolar process. With the availability of two-plate discrete capacitors, the decision was made to pursue some level of development in voltage-write-voltage-read (VWVR) memory. This topology has been widely used and has the

advantage of reading a voltage and writing a voltage so that, to a first order, there is no component-dependent conversion-gain to introduce uncertainty in the measurement. Also, the switching action reduces common-mode noise effects.

b. Charge-read Unlike the VWVR topology, the voltage-write-charge-read (VWCR) topology output risetime depends not only on the values of the bus and sample capacitors, but also on the ratio of the sum of these to the value of the feedback capacitor. For a unity gain inverting memory, the feedback capacitor must equal the sample capacitor.

c. Digitated vs. Sectioned The design requirements ultimately resulted in a sampling capacitor value of 1pF. The overall plan was to develop two different readout amplifiers and, as already mentioned, two different types of cells. In addition, there was some concern about radiation effects on the off resistance of the switch transistors. Each of the two types of memory cells therefore had two different lengths of transistors to test the effects of off resistance. The final layout was then to have 8 pipelines, each 128 cells long.

2. Capacitor size

Because the resistance of the sampling switch is non-linear, it can be shown that

$$\tau_{effective} = \left[\max R(v_{in}) \right] \cdot C_{sample} \quad (7.1)$$

where $\tau_{effective}$ is the effective time constant of the switch-capacitor combination, $R(V_{in})$ is the peak resistance of the switch within the operating

range, and C_{sample} is the sample capacitor value. With this relationship, the transistor switch peak resistance and the capacitor size can be determined for a given sampling precision. The chosen capacitor size was 1pF.

3. Readout Amplifiers

The readout amplifier topologies were chosen for stability, and drive capability. In general, single pole amplifiers give the best settling time. Unfortunately, the expected load capacitances of 5-15pF did not allow for a single-pole design that was relatively independent of load capacitance. Two topologies were fabricated in the memory. The first, IPC5C, was a modification of the standard two-stage CMOS amplifier. It is similar to that found in many textbooks except that the drive was extended to be push-pull. The other topology, IPC4B, was similar to one previously published except that it was optimized for improved settling at faster risetimes. Both of these designs work within approximately 0.2V of the supply rails.

D. Experimental results

A set of tests was designed to evaluate the suitability of both the process and candidate topologies for use in the central tracker. The tests were by no means exhaustive, but even so generated over 100Mb of data. Six parts from three wafers were irradiated at approximately 82KRad/hr. to 1MRad and 5MRad gamma dose. Measurements were taken at 0-, 1-, and 5MRad intervals. The chips were powered but not operating during radiation exposure. A summary of some of the test results are as follows:

1. Readout amplifier measurements

The input offset voltages of the amplifiers were measured with the reset lines active. The prerad IPC4B mean offset voltage was -1.4mV with a σ of 1.8mV and the IPC5C mean was 0.2mV with a σ of +2.1mV. The worst case change at 5MRad was 5mV with the average change being approximately 3mV. The 0MRad measured dc gain of the IPC4B was approximately 10K and the IPC5C was approximately 12.5K. The gain-bandwidth and slew-rate for the IPC4B were 11MHz and 18V/ms respectively and for the IPC5C 12MHz and 20V/ms respectively. The gain-bandwidths showed a degradation of approximately 10% after 5MRad.

2. DC Integral non-linearity (INL)

The INL was measured for a set of fixed dc voltages and showed a result of approximately $\pm 0.5\%$. The linearity showed little change between 0- and 5MRad.

3. AC INL

The 5MRad INL for a 50ns pulse similar to that from a real preamplifier was tested and showed performance similar to the DC INL. There was little change between 0- and 5MRad.

4. Droop rate

The change in cell voltages after 0.5s and 1s at 5MRad were measured. The cells exhibited a droop of much less than 1V/s at 0MRad and after 5MRad which is much better than needed. This had been a major concern during

design.

5. Pre- and post-correction pedestals

The pre- and post-correction pedestals were measured for 47.5MHz clock rate. The voltage-read channels in general had much better correlation than the charge-read channels and pedestals were approximately 4-6mV rms.

6. Nearest-neighbor channel interaction

The purpose of this test was to look for a channel disturbing it's neighbors. Each channel was written 1.5V, 2.5V, and 3.5V while all others were at 2.5V. The voltage-read channels showed no systematic effect. The charge-read neighboring channels did exhibit a deviation of approximately 4mV for a charge-read 2V span. This was thought to be due to the large error signal at the input of the readout amplifier when the sampling capacitor is connected for readout. This causes the input reference line to be disturbed in adjacent channels. Individual amplifier reference lines might solve this but would represent a cumbersome layout.

E. Questions to be answered

In the planning stages of the memory development, it was found that although memories were being utilized in experiments, no one had looked experimentally at the topics for which we needed information. These included

1. Can one build *any type* of memory to successfully survive the radiation environment of the GEM detector?

2. Can any optimization of memory cell area be obtained for the readout times necessary for the detector?
3. How good does a wide dynamic range output amplifier have to be in order to be useful for this memory?
4. How well can a pedestal correction table correct the data for both pre- and post-radiation measurement?
5. Does a non-weighted addressing code such as a Gray code result in improved data acquisition?
6. For a given process, what results will a head-to-head comparison of different memory topologies and different amplifier topologies show?
7. Does pattern noise even exist?
8. What level of accuracy does a real-time pedestal subtraction allow?
9. Does the pedestal subtraction require only some limited nearby pipes to work or can any number of pipes be used on a given chip?
10. Does ionizing radiation effect the ability of pedestal correction to function correctly?

F. Conclusions

An error-budget analysis [EBUD] was undertaken to determine the peak error expected due to the various contributions. The results are presented in

Table 7-1. A full-scale input of 3V was assumed.

Table 7-1. Error-budget analysis.

<u>Parameter</u>	<u>VWVR</u>	<u>VWCR</u>
<u>Pedestals</u>	10mV	12mV
<u>Dynam. INL</u>	$\pm 0.25\%$ (8mV)	$\pm 0.6\%$ (18mV)
<u>Noise (est.)</u>	5mV	5mV
<u>TOTAL (3σ)</u>	23mV (0.77%)	35mV (1.17%)

The results of this indicate the VWVR memory is approximately 7-8 bits and the VWCR memory is approximately 6-7 bits.

Both the Sectioned and Digitated memories worked on first silicon. The memories were able to function at a sample rate of 47.5MHz, the limit of our test equipment. The pedestal variations of between 5-10mV rms were acceptable for the intended experiment. It was demonstrated that these could be reduced by pedestal subtraction. The readout amplifiers worked as designed with one of the topologies exhibiting performance superior to the other. The memories had acceptable droop performance and were resistant to radiation-induced degradation to at least 5MRad total dose.

The pedestal correction method tested indicated that some improvement in memory performance can be obtained in a radiation environment even with a non-radiation hard process. The correction method showed that for eight channel pipelines, the correlation between pipes is good enough for 8-10 bit performance which is the goal for use of this method.

The major questions posed by this dissertation can be summarized by the following: 1) Could an analog memory be designed and fabricated that would even approach the performance required for the Interpolating Pad Chamber? and 2) Could a non-radiation-hard process be used for a corrective approach to measurement in a radiation environment? According to the measurements, the answers would have to be 'yes'. The conclusions will be addressed topically.

1. Topology

The voltage-write-voltage-read topology appears to be the most desirable of the two topologies tested when considering the readout settling time, linearity, nearest neighbor effects, and pedestal correctability. In all cases, the VWVR topology equaled or surpassed the performance of the VWCR topology. The major drawback of this topology is, of course, the size of the capacitor-switch cells. Had the SSC continued, the next round of design on this circuit would have been to increase the length of the pipelines to at least 144 cells and the number of pipes per chip to 16. The first change would have been to reduce the capacitor size to approximately 0.75pF and the switches to one half the present width. This would have increased the input charging time by approximately 50%, but it appears from the dynamic linearity measurements that this would be acceptable. In general these results would preclude any major size optimizations. This was as expected.

2. Pedestals

The questions concerning the amount of pedestal variation vs. radiation dose appear to have been answered with the results presented in Chapter VI.

The pedestals exhibit little change in the AVLSI-RA process as the ionizing dose is increased. The process appears to track pedestal correction better for the voltage-read than for the charge-read topology. The only concern is that the pedestal tilt appeared to be systematic from chip to chip to some degree but not entirely. An unexpected result of the testing is that the tilt would need to be a pass-fail parameter during chip testing and would therefore affect the yield. Some form of pedestal subtraction would definitely be needed. Another memory would have to be built in the AVLSI-RA process, this time with entirely uniform cells, in order to test the real-time pedestal correction, but pedestal table subtraction appears to work well. Smaller switches for the cells would be incorporated into the next designs since, as seen in **Table 7-1**, the pedestals appear to be one of the major contributors to the available memory resolution. It is apparent that pedestal noise does indeed exist and that although Gray code addressing seemed like a good idea, the only way it would improve readout is if no correction were to be applied, and then only marginally.

3. Readout amplifier

As is often the case in engineering, simpler things work better and that definitely appears to be the case in the readout amplifier designs. The IPC5C standard topology appears to have better speed and available phase margin than the rail-to-rail IPC4B. The '5C takes up less space and uses less power than the '4B. The input offset variations vs. radiation dose, which would indicate degradation of device matching, was approximately the same for both. The slight edge in phase margin would have been needed for further development because the pipelines would have been longer and the sampling capacitors would have

been smaller. To maintain the settling time performance, further work would have been necessary on this amplifier. Without a doubt, the PMOS input device is desirable for this application. It appears to exhibit less change with radiation dose than the NMOS, so future amplifier developments would have been based on the PMOS input.

4. Digitated vs. Sectioned layout

The Digitated layout appeared to have the best spatial characteristics of the two. For the next design, the major problem would have been how to lengthen the pipes and maintain minimum ENABLE delay. The best solution appeared to be a distributed set of buffers up and down the pipeline instead of a single buffer to drive all the enables. If a buffer for each eight or sixteen cells were implemented, the current density and propagation delay in the drive lines would drop almost proportionally.

5. Pedestal correction

The pedestal correction appears to work well at eight- or nine-bit resolution. The radiation effects appear to be global with regard to the changes in pedestal variations. This is fortuitous because not only can the correction be applied on a large scale to all memory cells, the correction method actually depends on the changes being global, not local. Further work on larger memories will be undertaken at a later date, but the work presented here has been instrumental in determining that the approach is indeed valid.

G. Future Work

Work for the next versions of PHENIX circuitry is already underway. The testing for the new memories will build upon the lessons learned from the GEM AMU testing. Although the memories for PHENIX are, except for MVD, not subject to much radiation, the testing will be an extension of that already performed. Simultaneous read-write testing will be the focus of the new program. This is not only because of the intended usage, but also because of the results of the binary code and Gray code results from the GEM AMU. The results have raised serious concerns about the effects of the pattern noise and how different patterns affect the readout.

The pedestal correction work will be applied to larger memories (16 channels x 64 cells deep). The correction will be further tested with the new memory which itself is planned to be the basis for a 10-12 bit resolution system. The MVD will ultimately become a 10-bit system with 32 channels per chip. The actual corrector will likely be built in to the ADC. Tests will be run to determine if the 32-channel version functions as well as the eight-channel version.

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APPENDIX

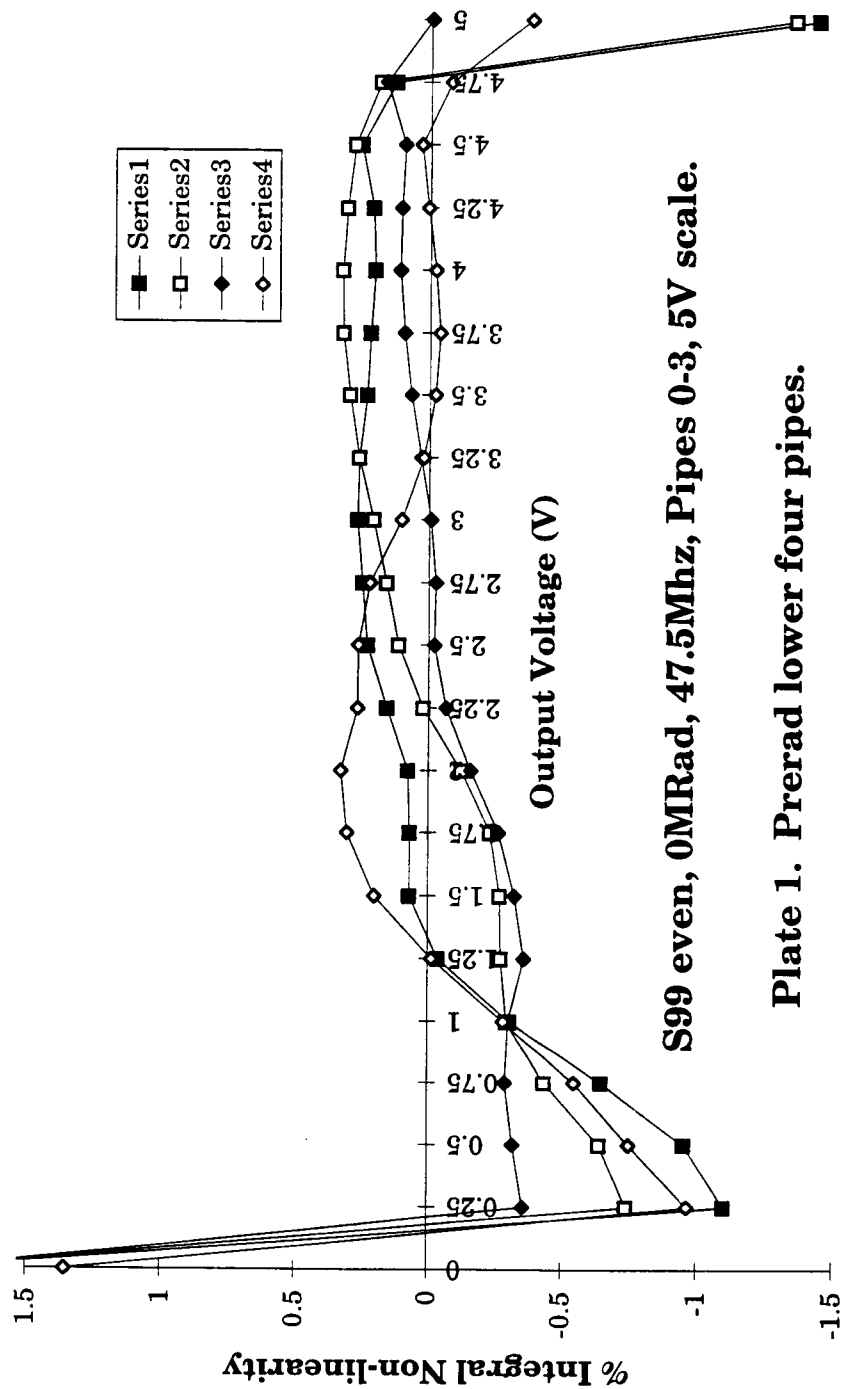
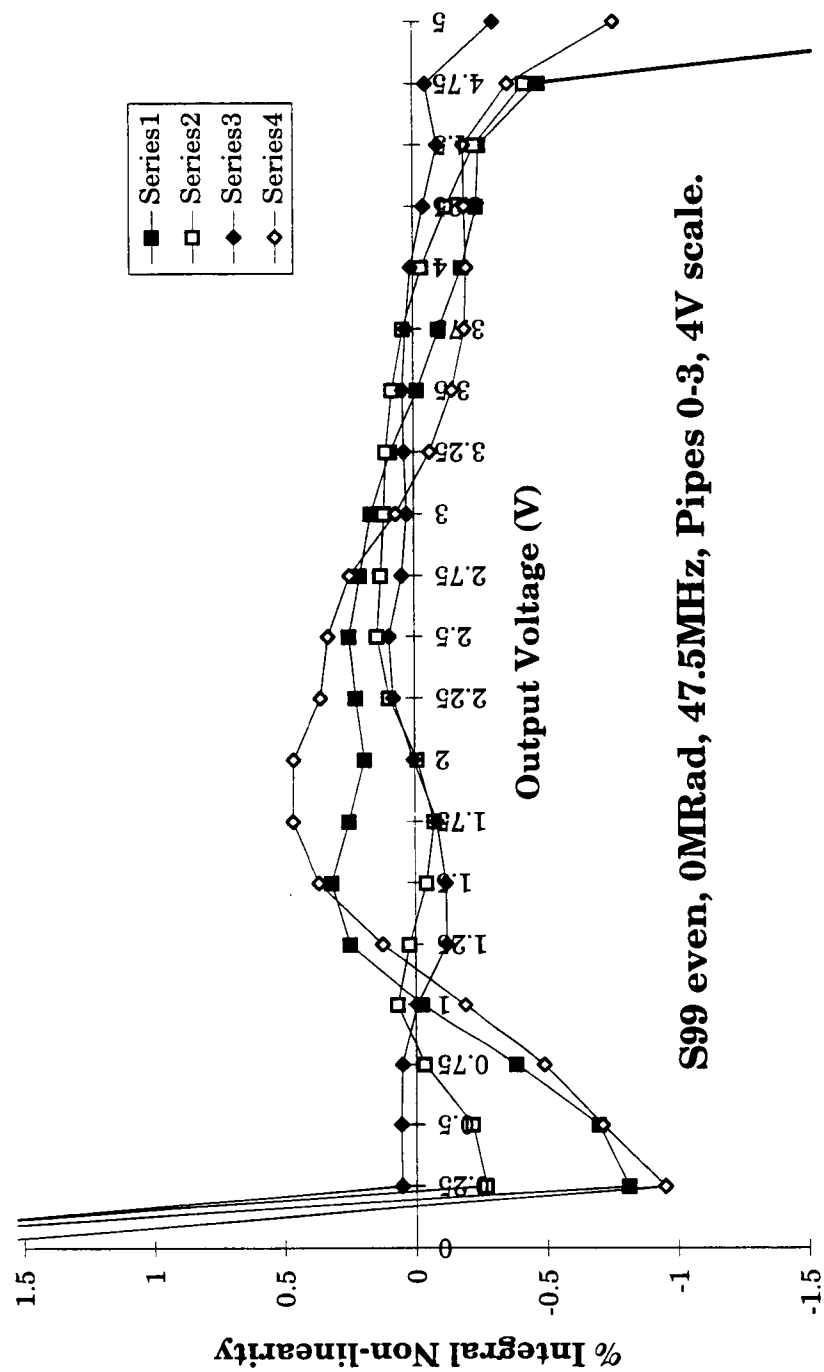
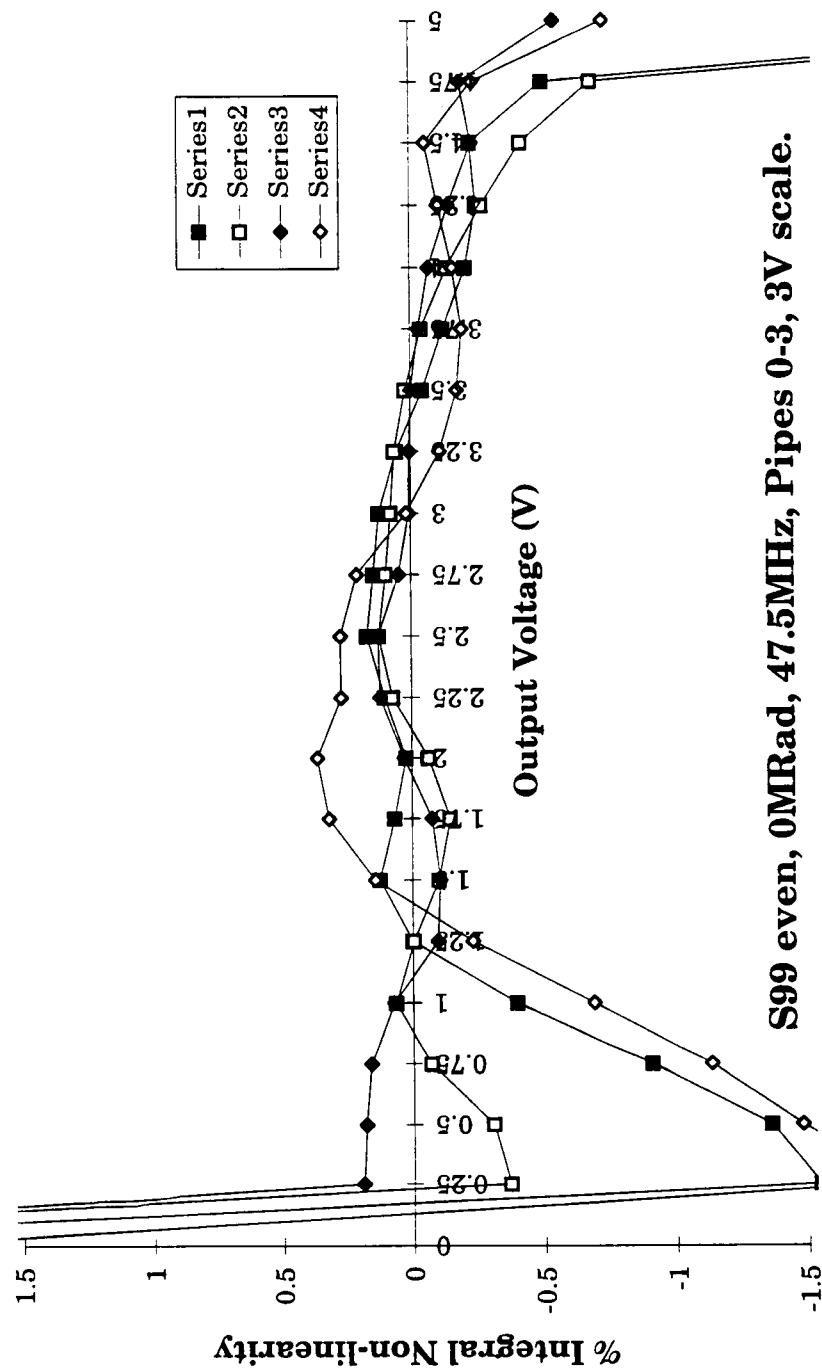


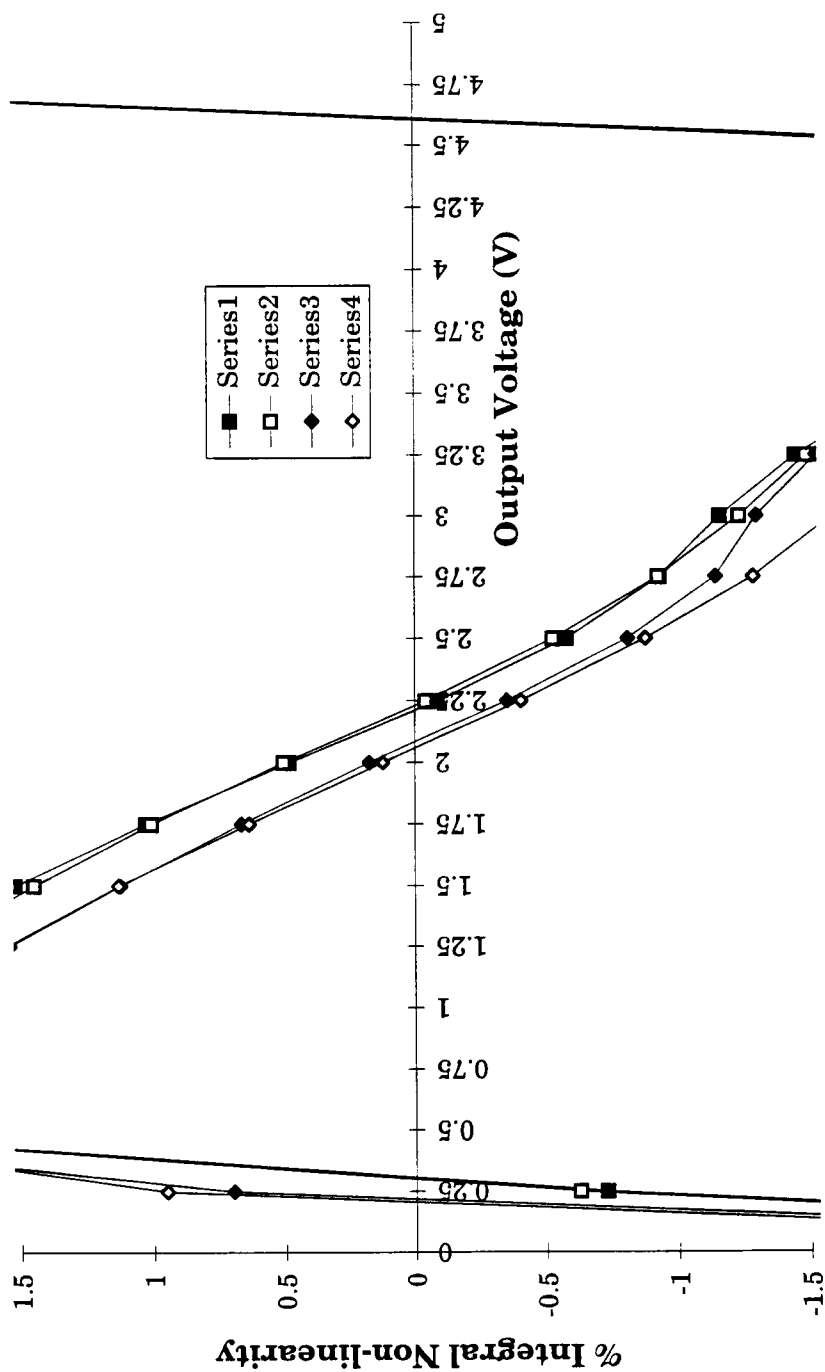
Plate 1. Prerad lower four pipes.



S99 even, 0MRad, 47.5MHz, Pipes 0-3, 4V scale.

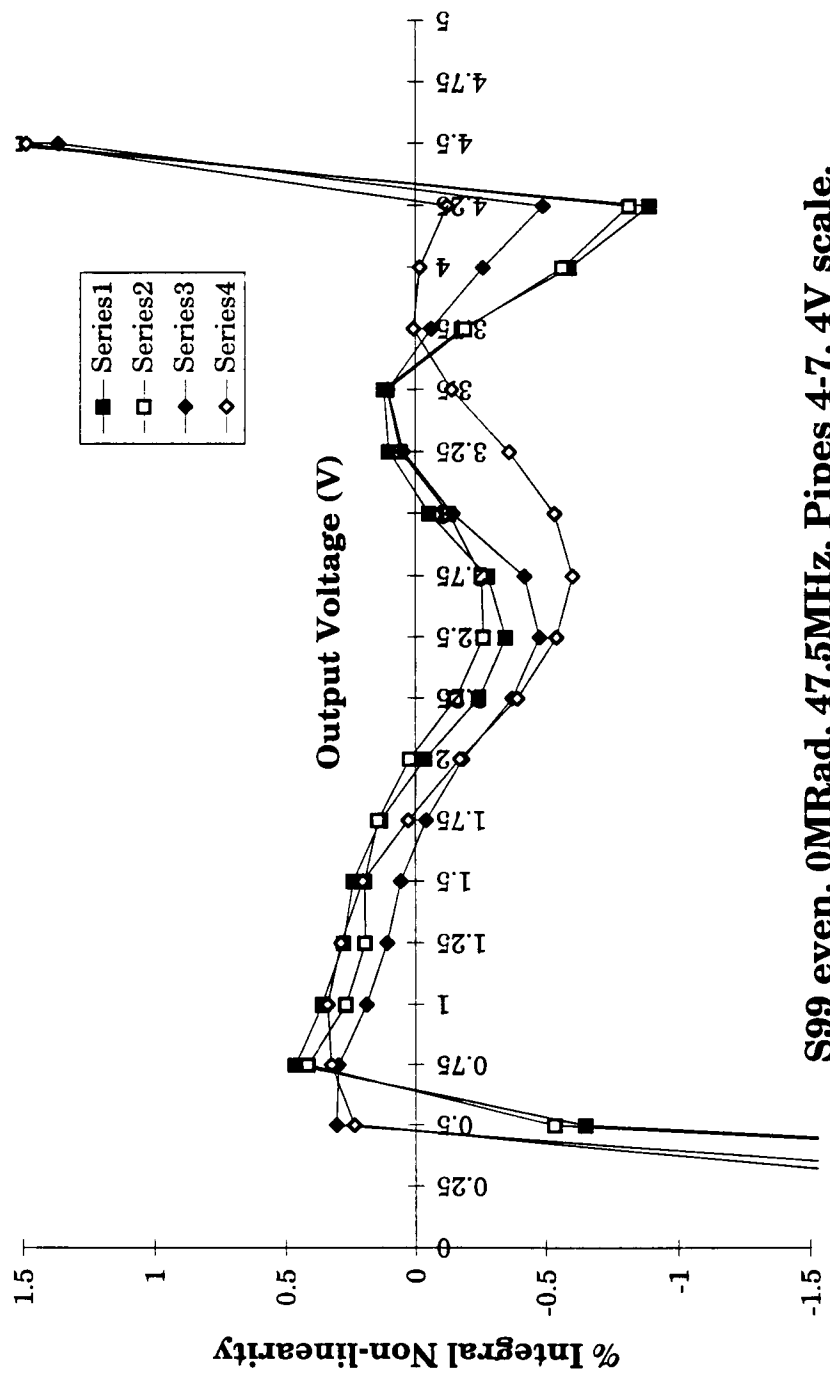


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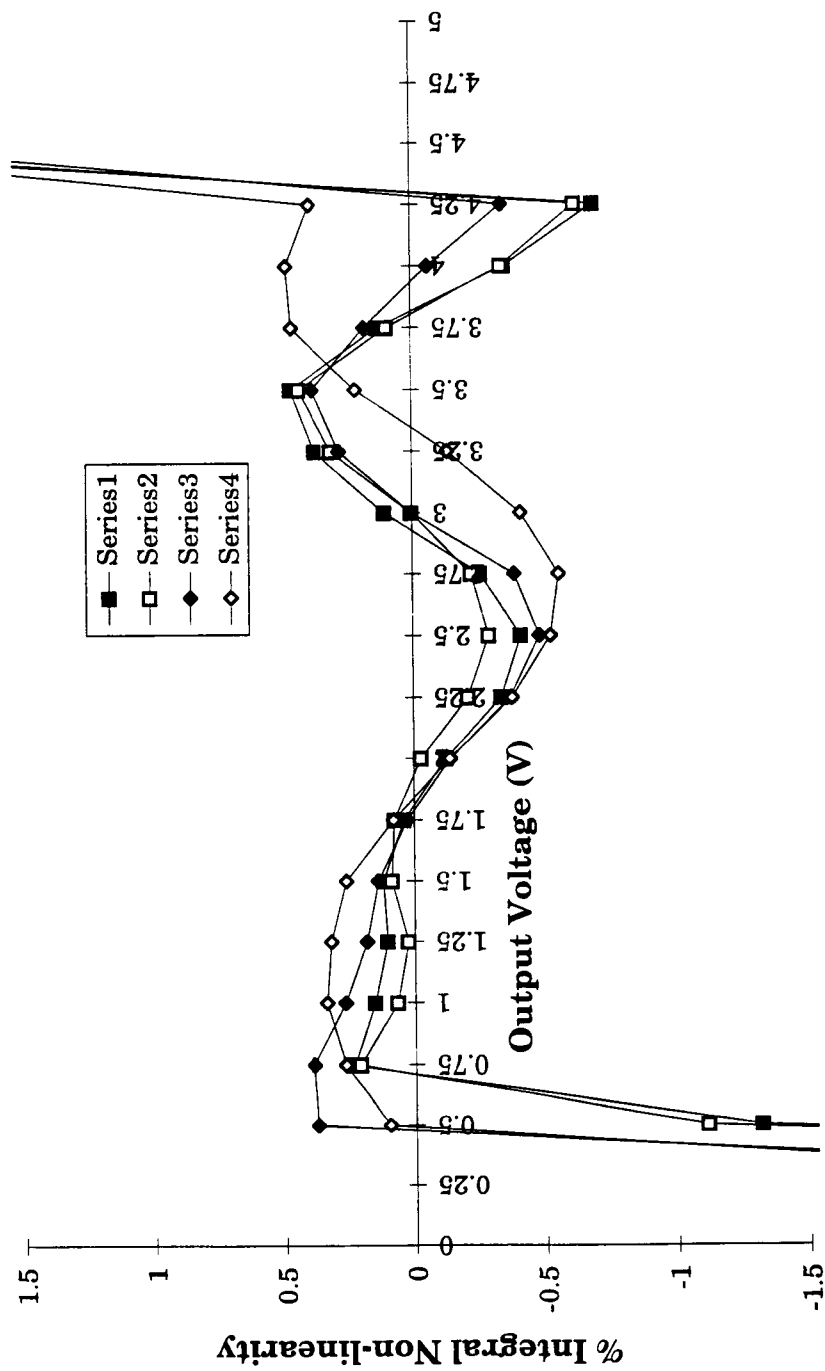


S99 even, 0MRad, 47.5MHz, Pipes 4-7, 5V scale.

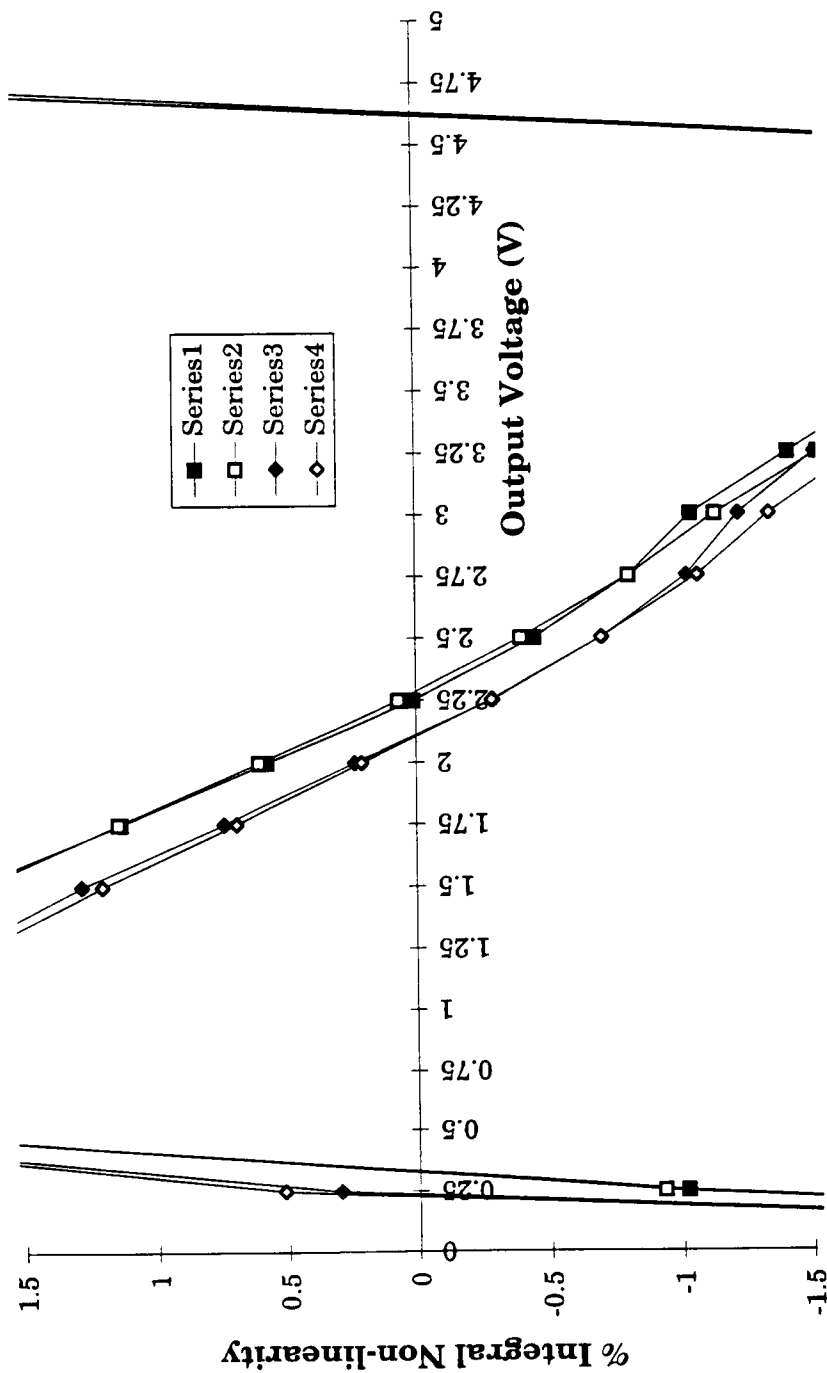
Plate 2. Prerad upper four pipes.



S99 even, 0MRad, 47.5MHz, Pipes 4-7, 4V scale.

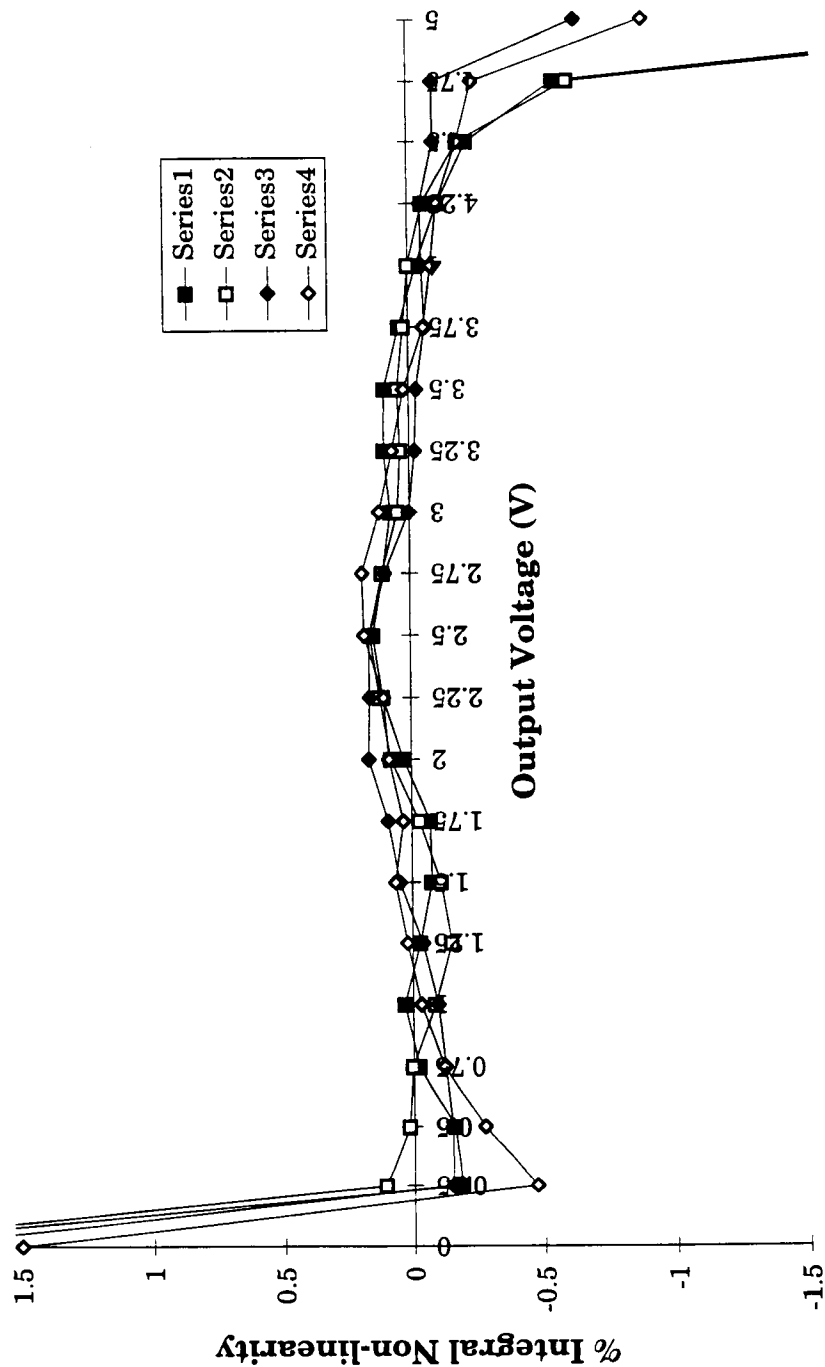


S99 even, 0MRad, 47.5MHz, Pipes 4-7, 3V scale.

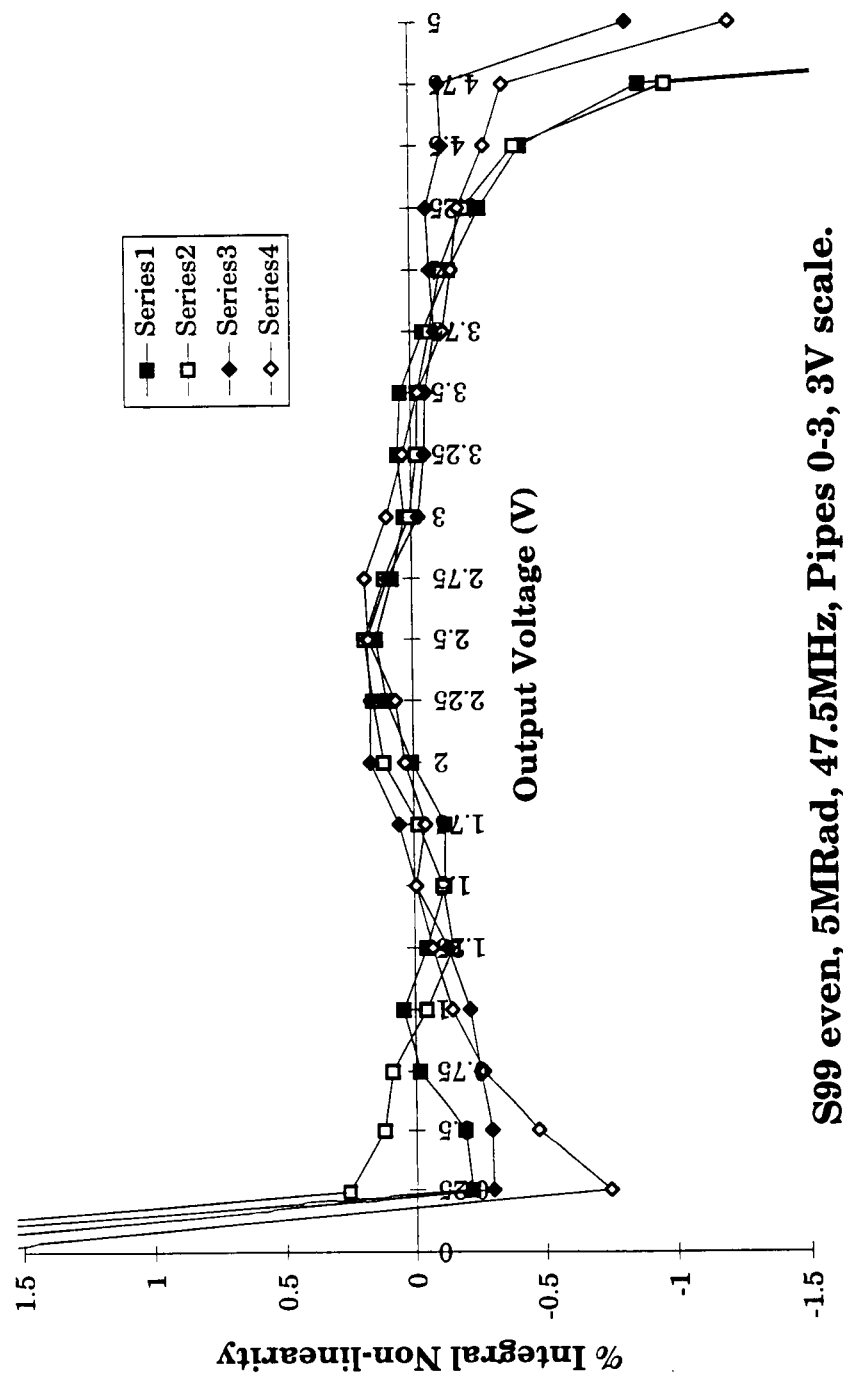


S99 even, 5MRad, 47.5MHz, Pipes 4-7, 5V scale.

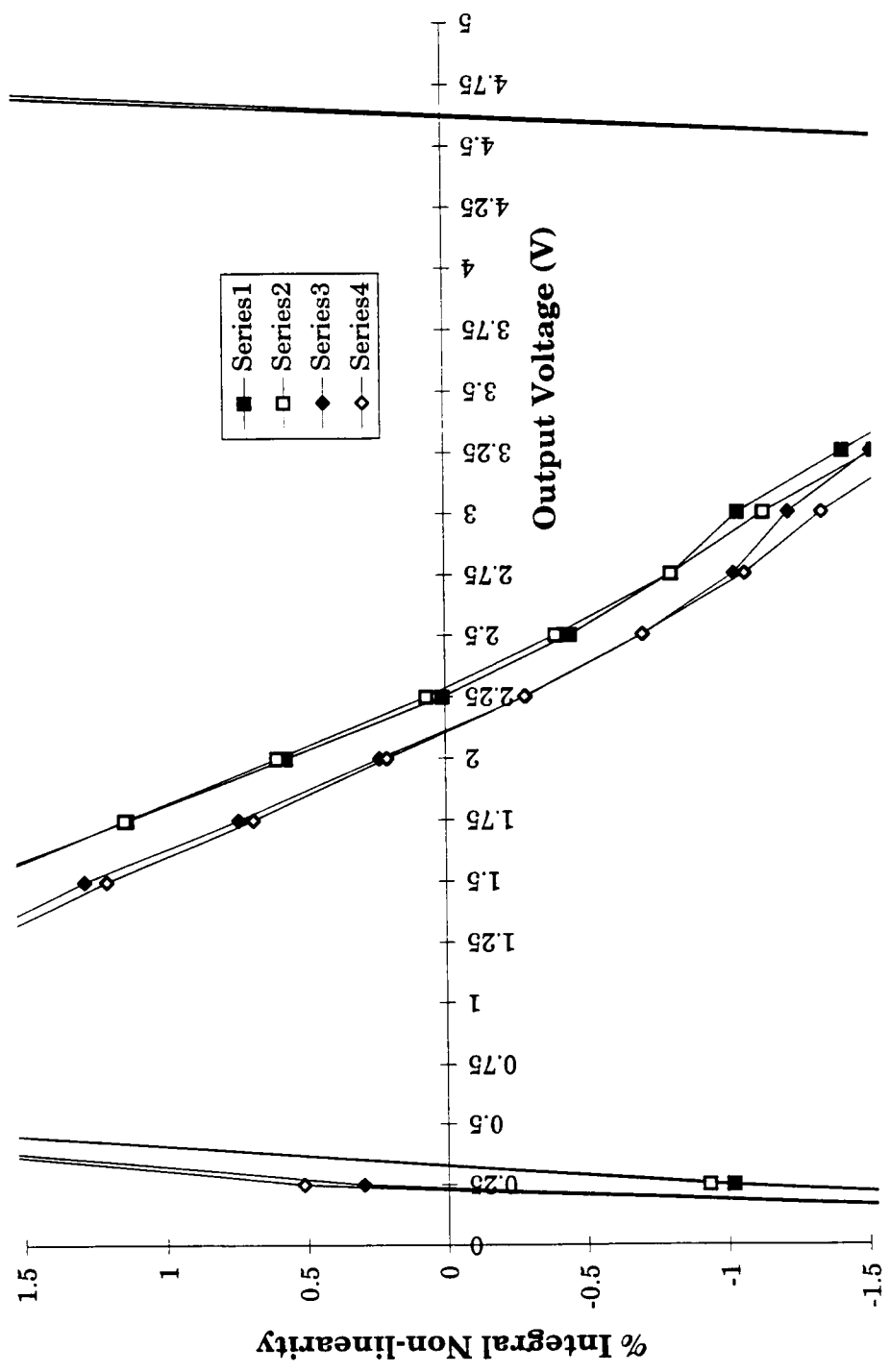
Plate 3. 5MRad INL.



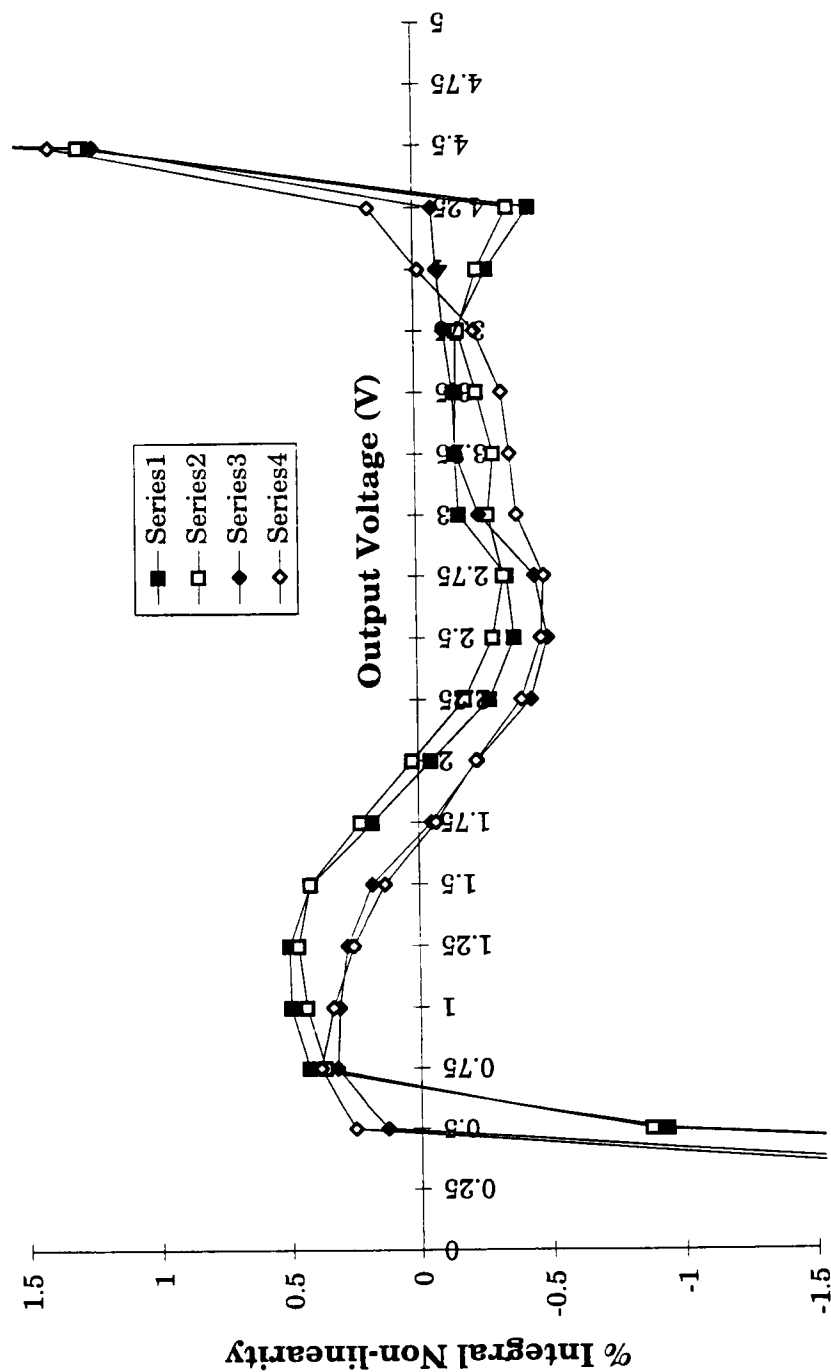
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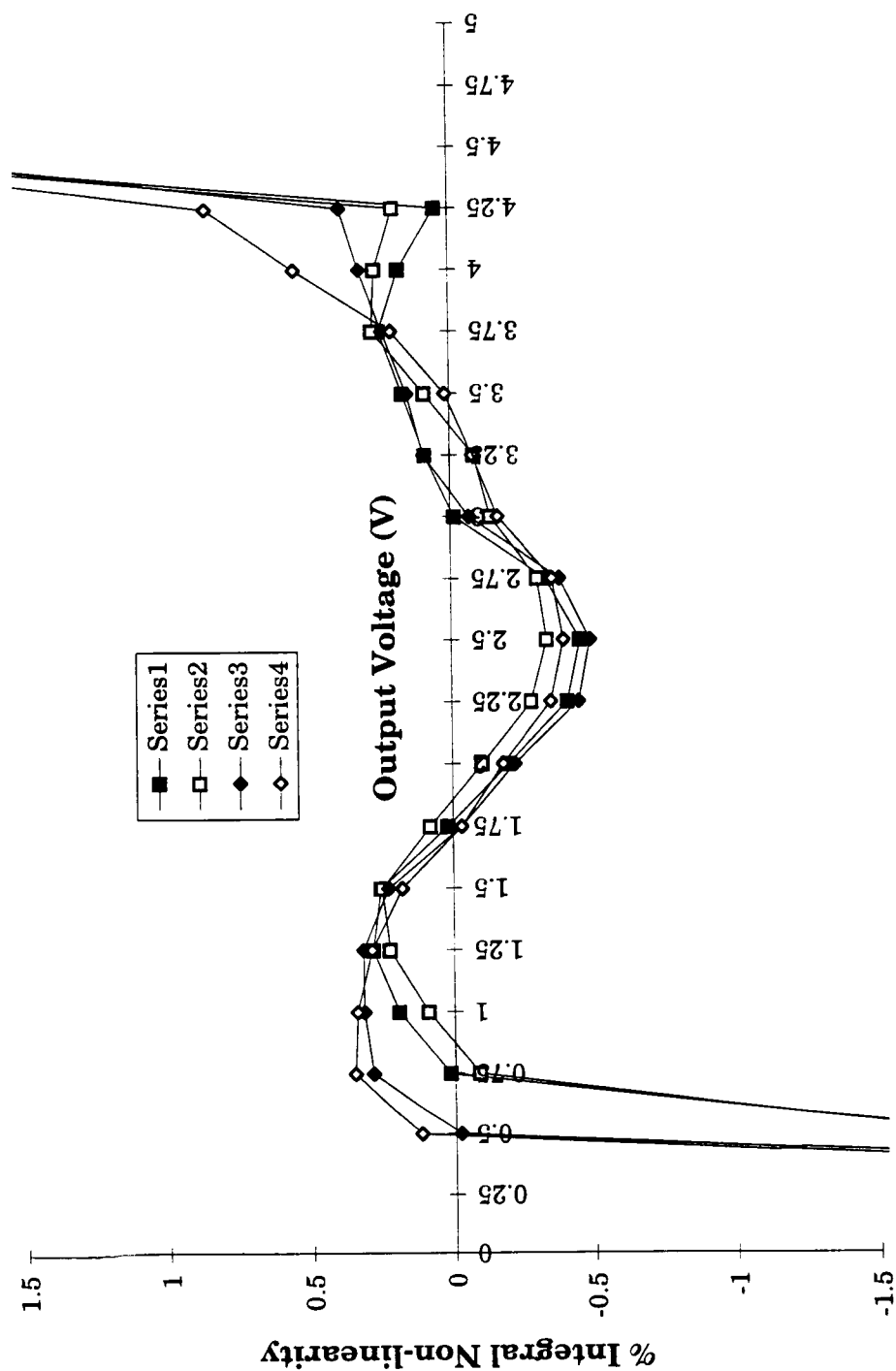
S99 even, 5MRad, 47.5MHz, Pipes 0-3, 3V scale.



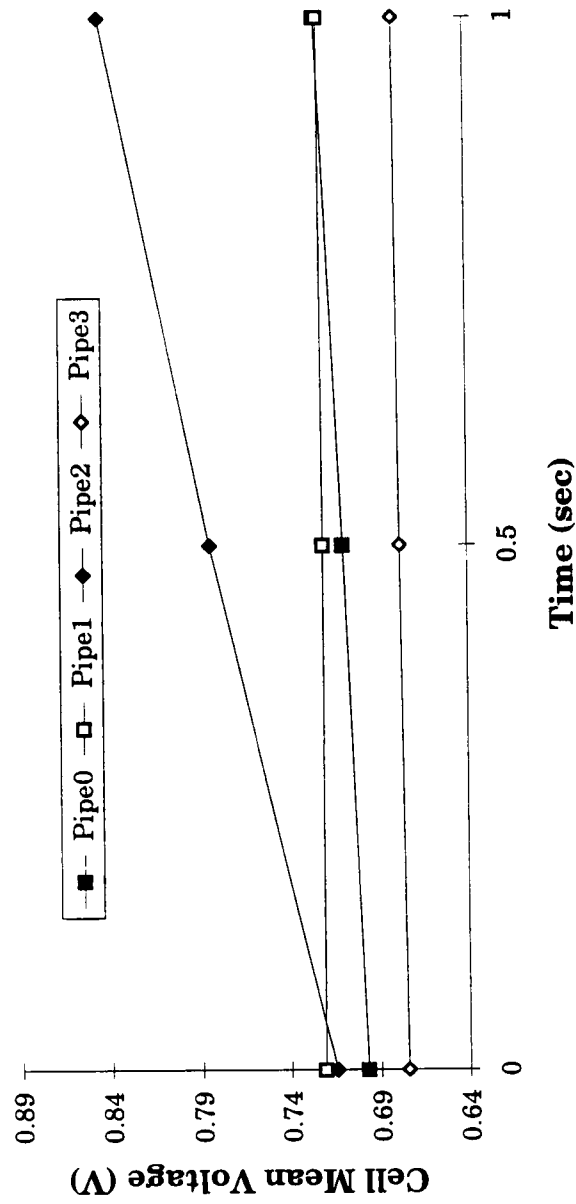
S99 even, 5MRad, 47.5MHz, Pipes 4-7, 5V scale.



S99 even, 5MRad, 47.5MHz, Pipes 4-7, 4V scale.

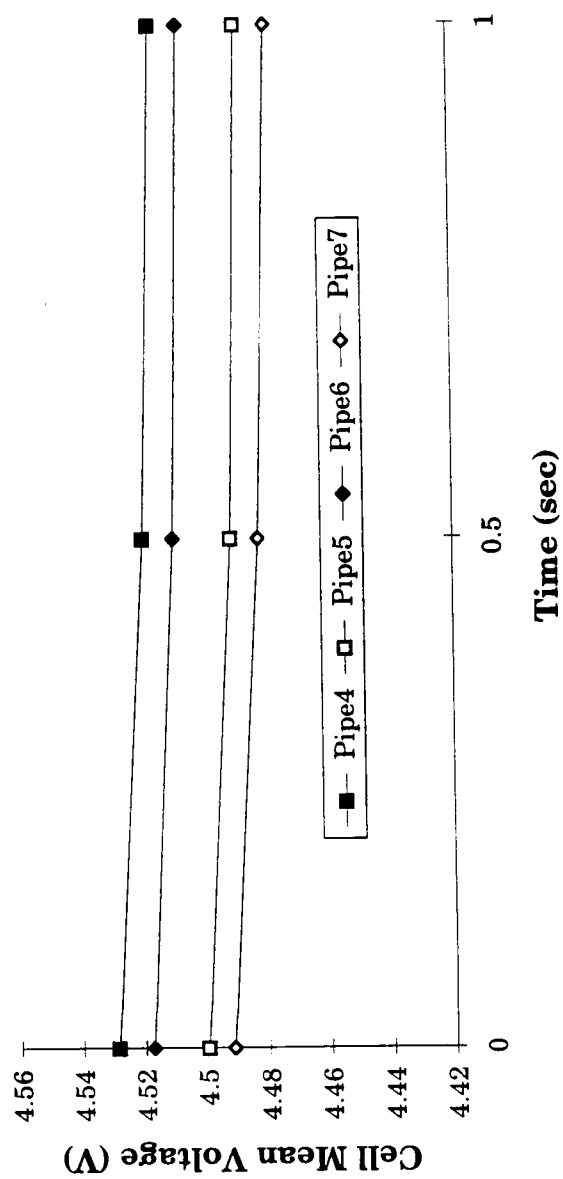


S99 even, 5MRad, 47.5MHz, Pipes 4-7, 3V scale.

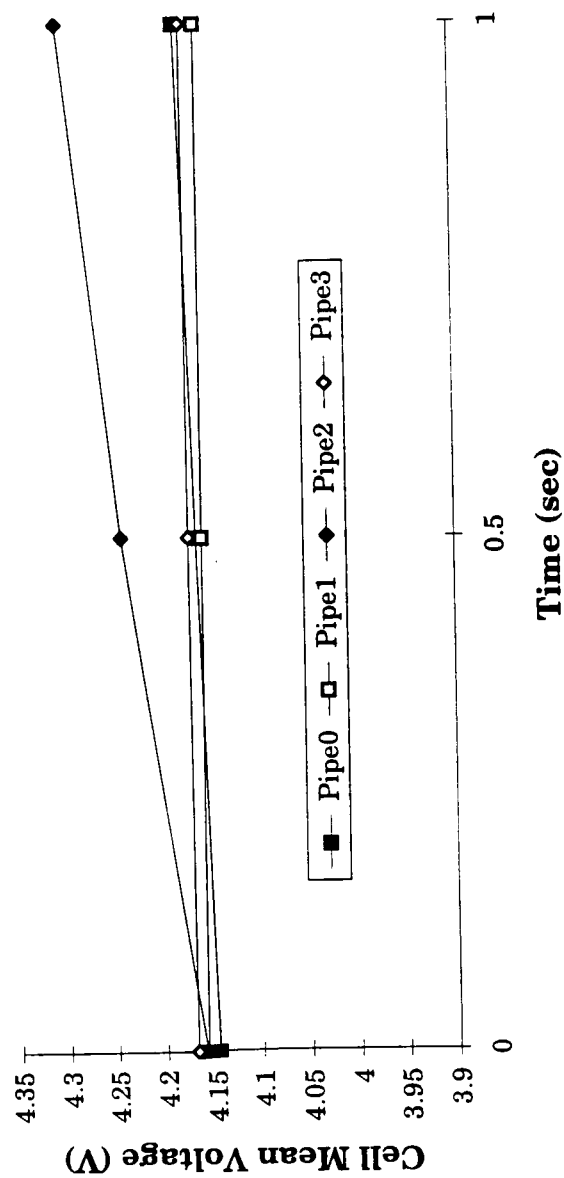


Pre Rad Droop for Cell 50, D4A, Even, .75 DC Input.

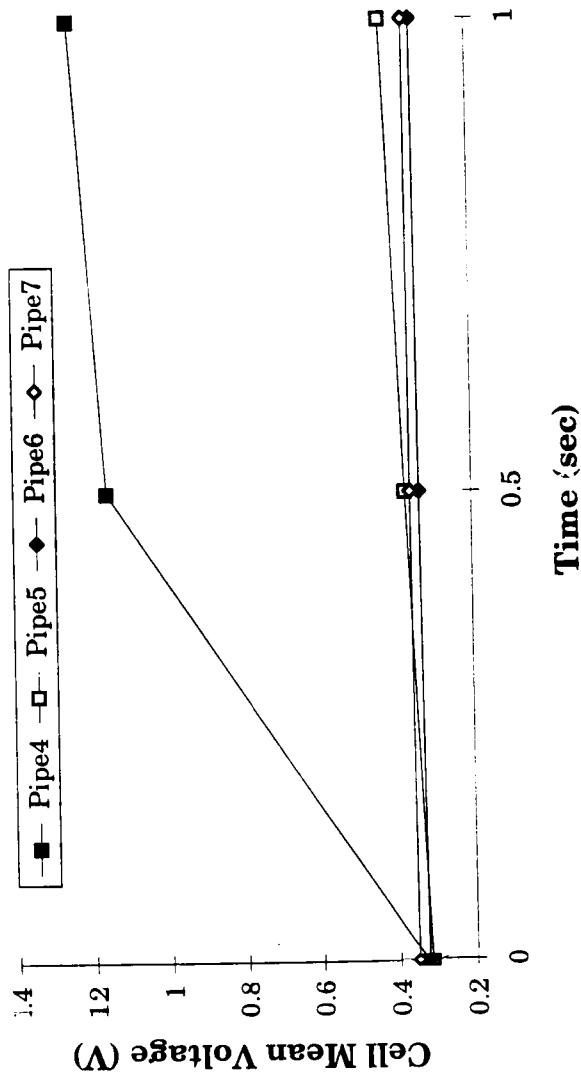
Plate 4. Droop measurements.



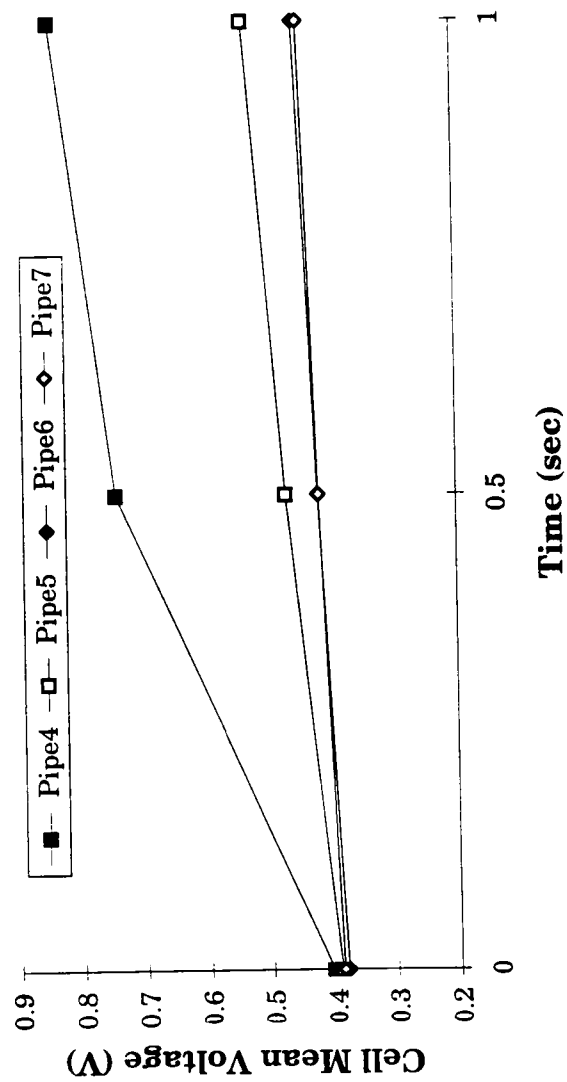
Pre Rad Droop for Cell 50, D4A, Even, .75 DC Input.



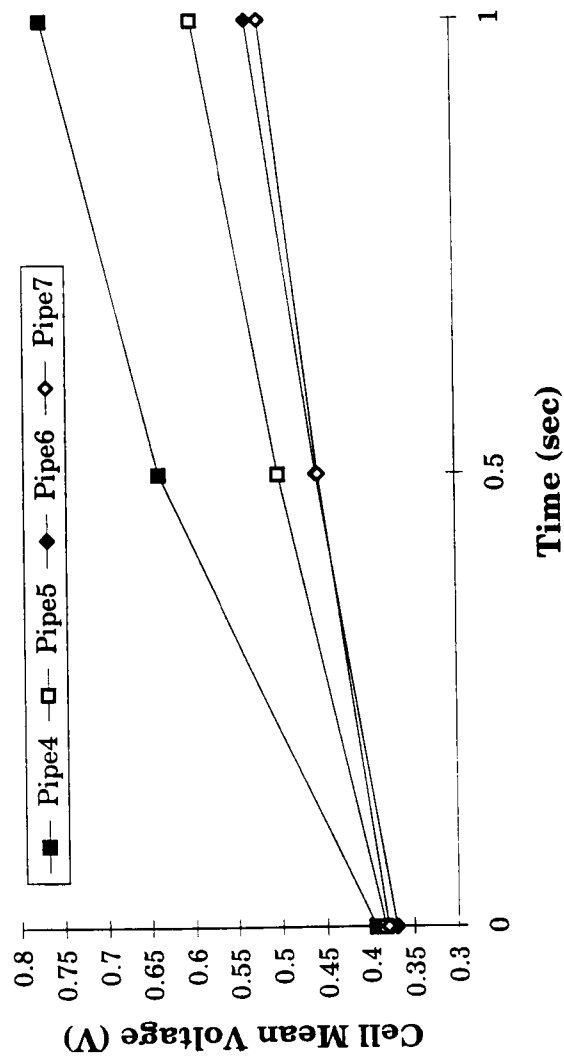
Pre Rad Droop for Cell 50, D4A, Even, 4.25 DC Input.



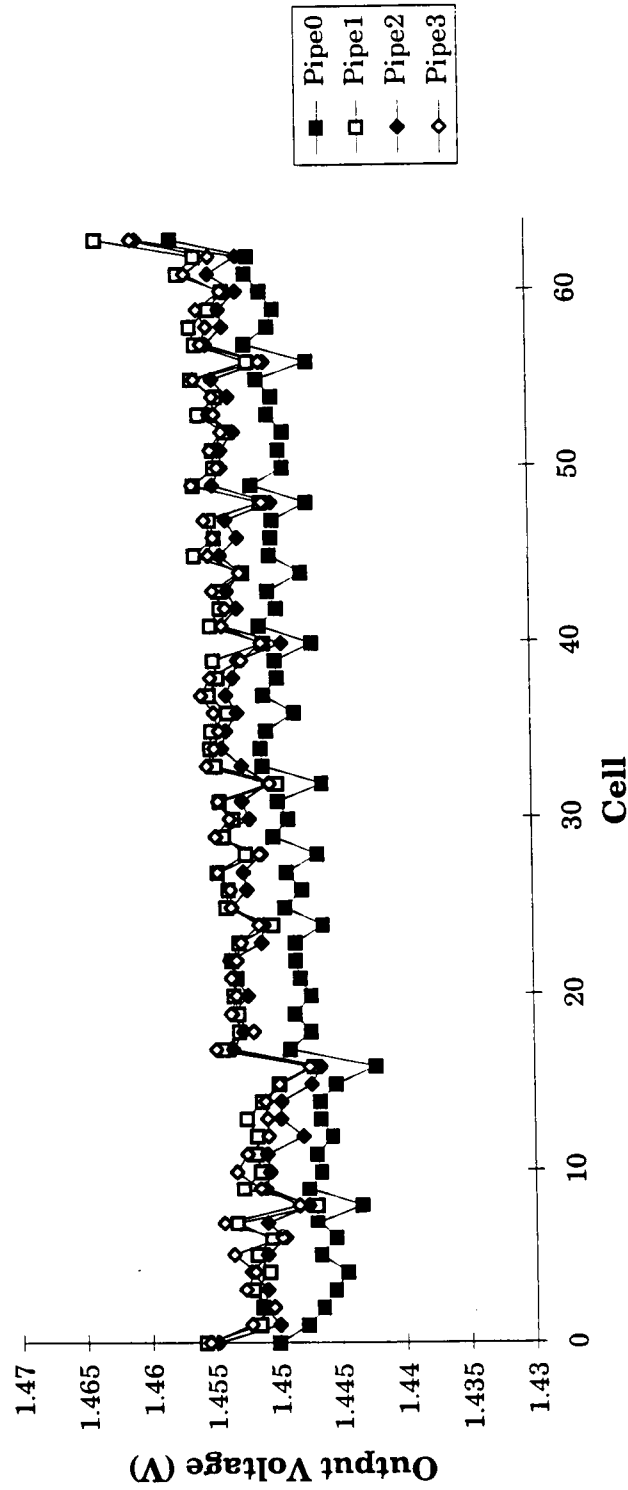
Pre Rad Droop for Cell 50, D4A, Even, 4.25 DC Input.



1MRad Droop for Cell 50, D4A, Even, 4.25V DC Input.

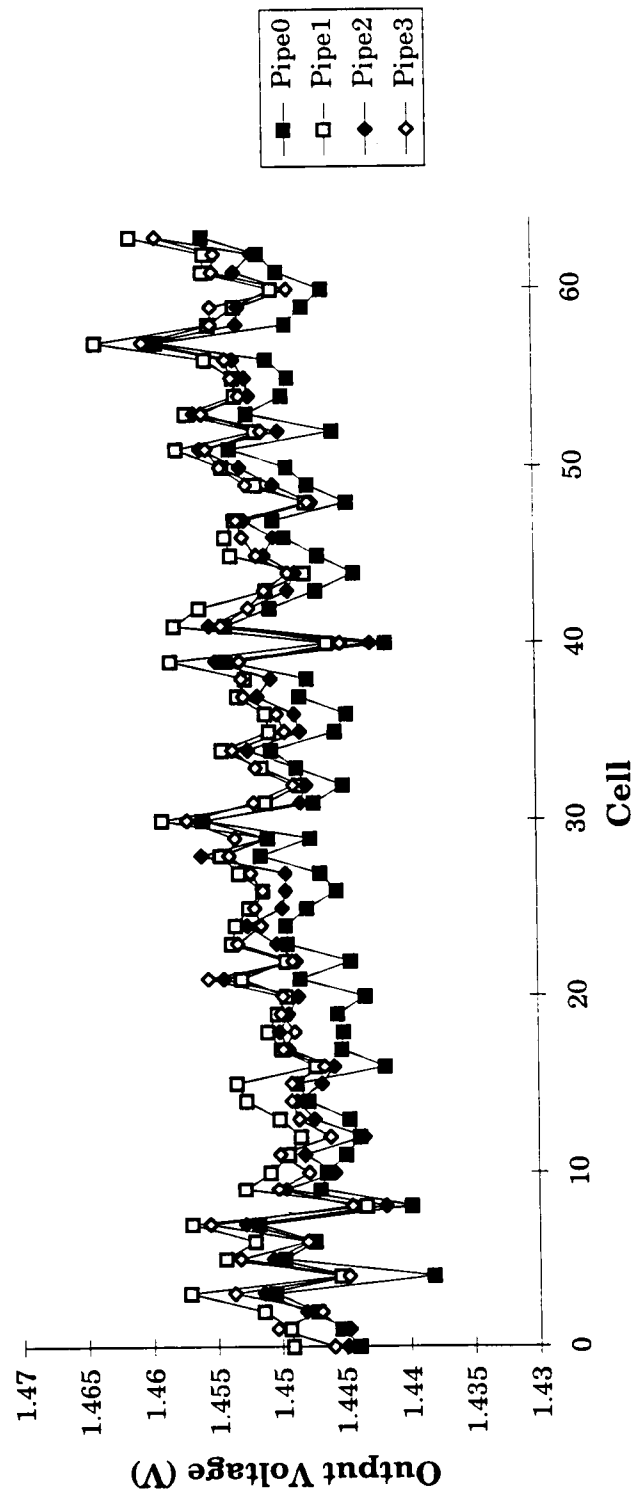


5MRad Droop for Cell 50, D4A, Even, 4.25V DC Input.

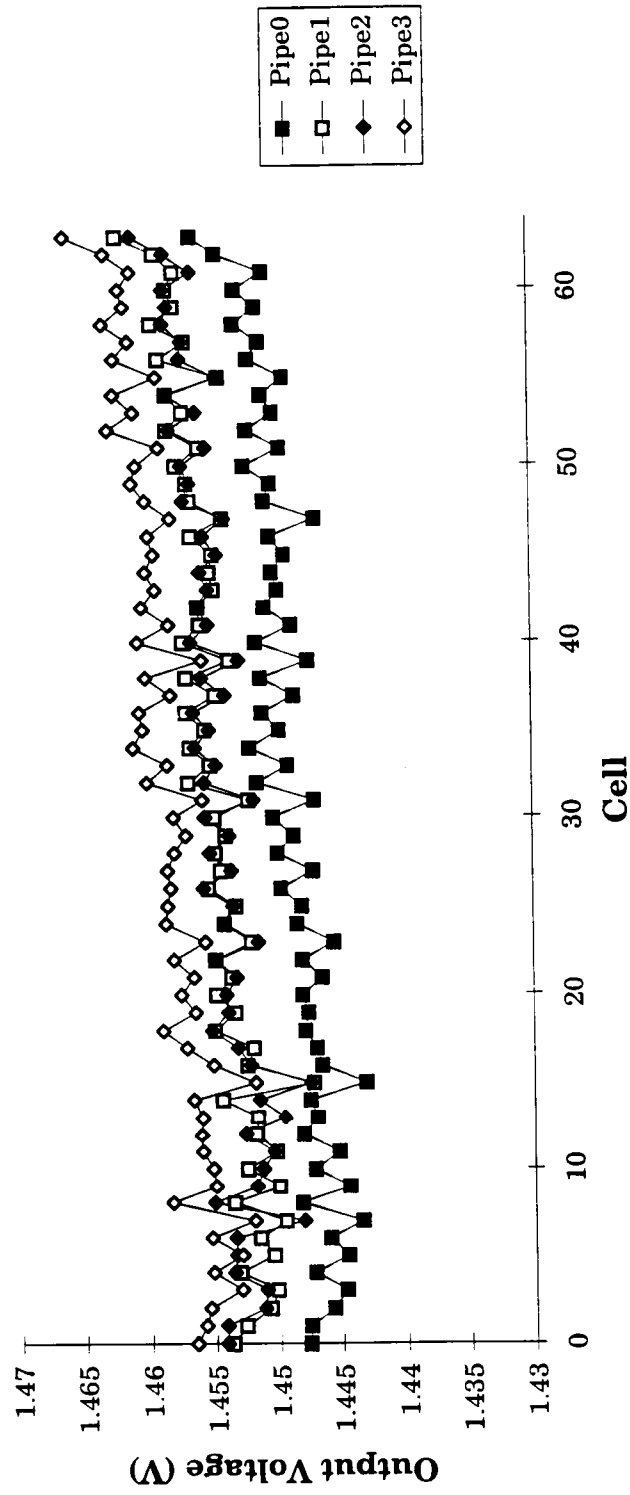


D99, Odd, 1.5 Volt Input, Average, 10MHz Binary Write.

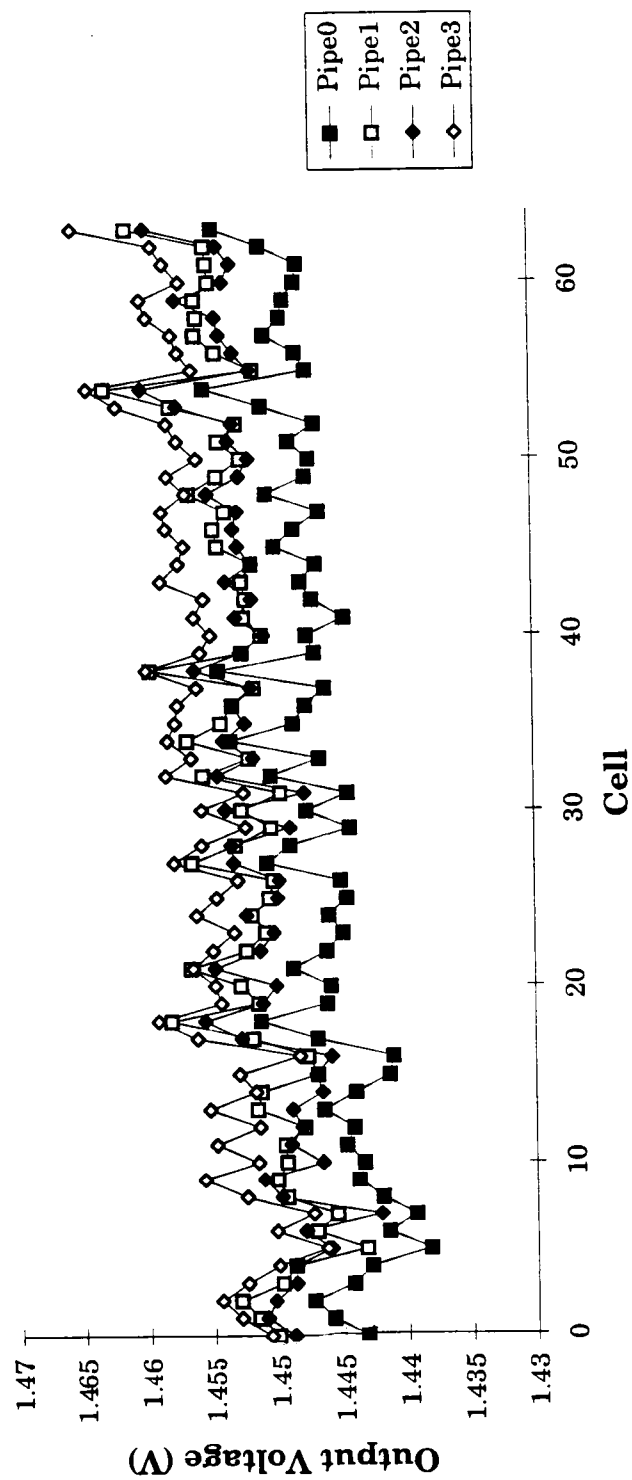
Plate 5. Chip D99, 1.5V input.



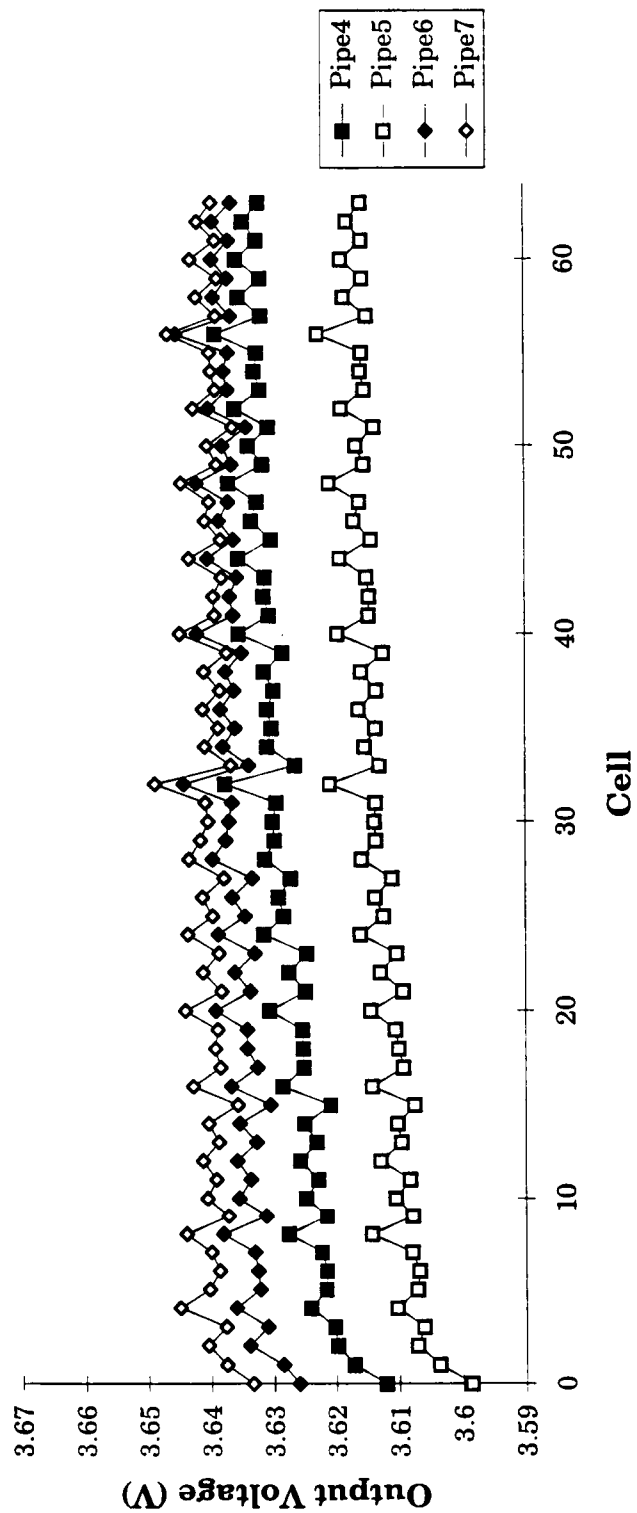
D99, Odd, 1.5 Volt Input, Single Shot, 10MHz Binary Write.



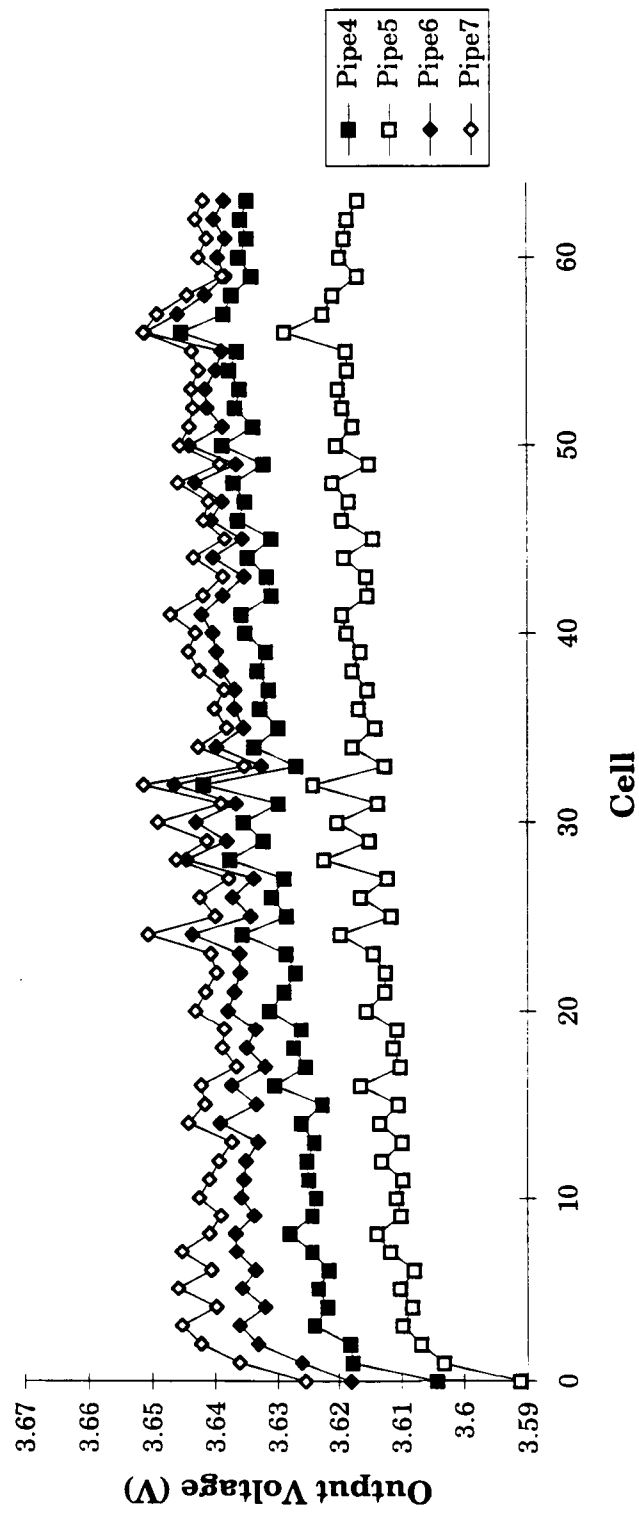
D99, Even, 1.5 Volt Input, Average, 10MHz Binary Write.



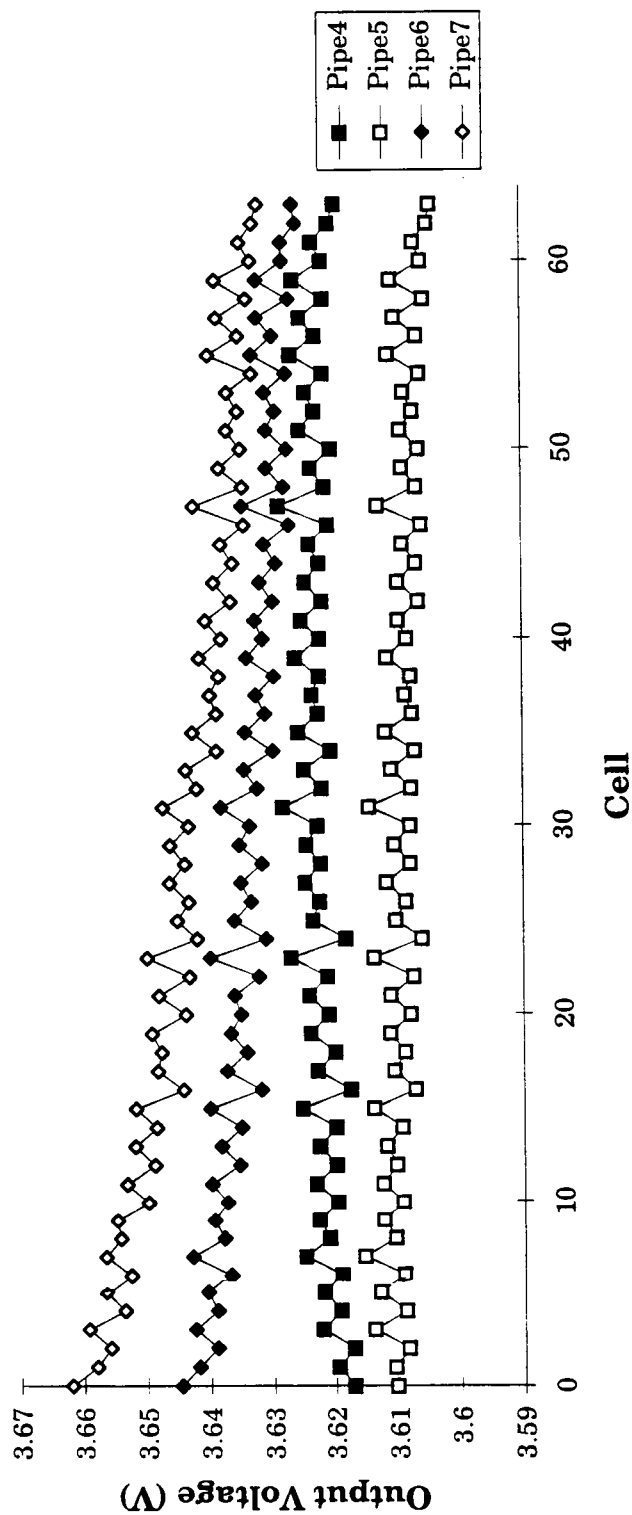
D99, Even, 1.5 Volt Input, Single Shot, 10MHz Binary Write.



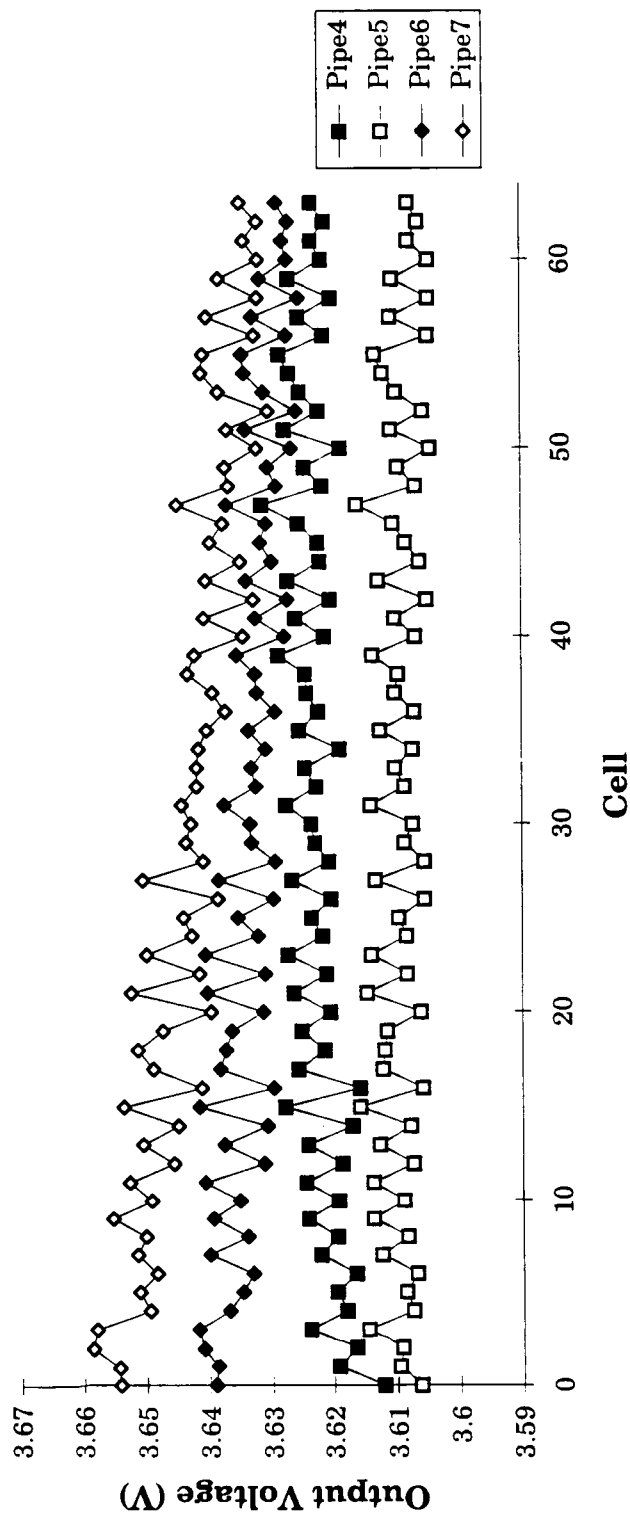
D99, Odd, 1.5 Volt Input, Average, 10MHz Binary Write.



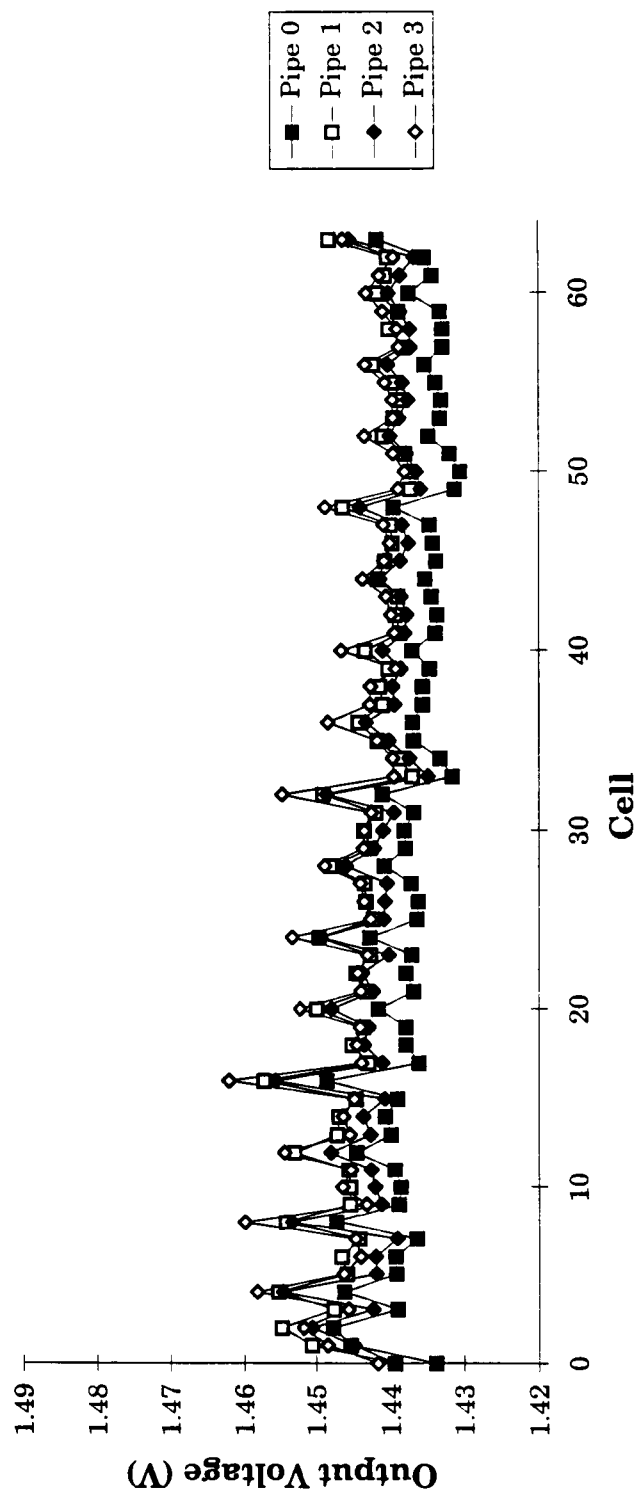
D99, Odd, 1.5 Volt Input, Single Shot, 10MHz Binary Write.



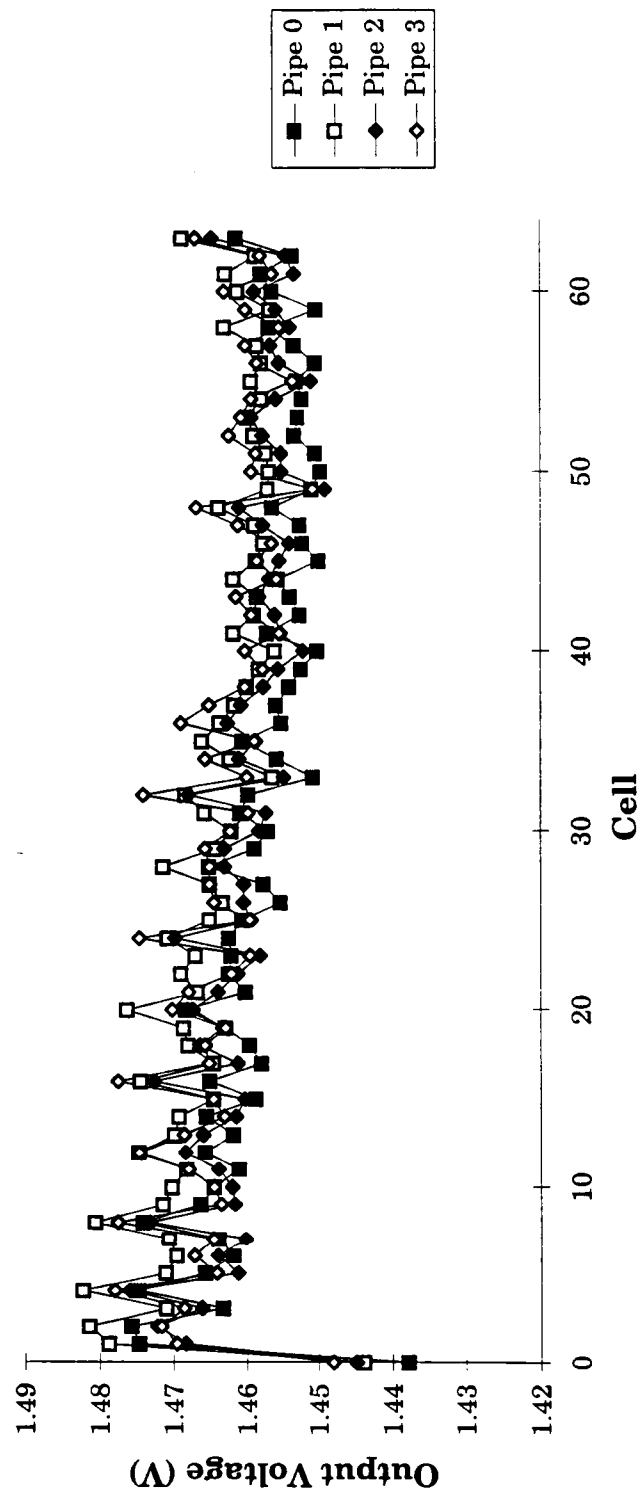
D99, Even, 1.5 Volt Input, Average, 10MHz Binary Write.



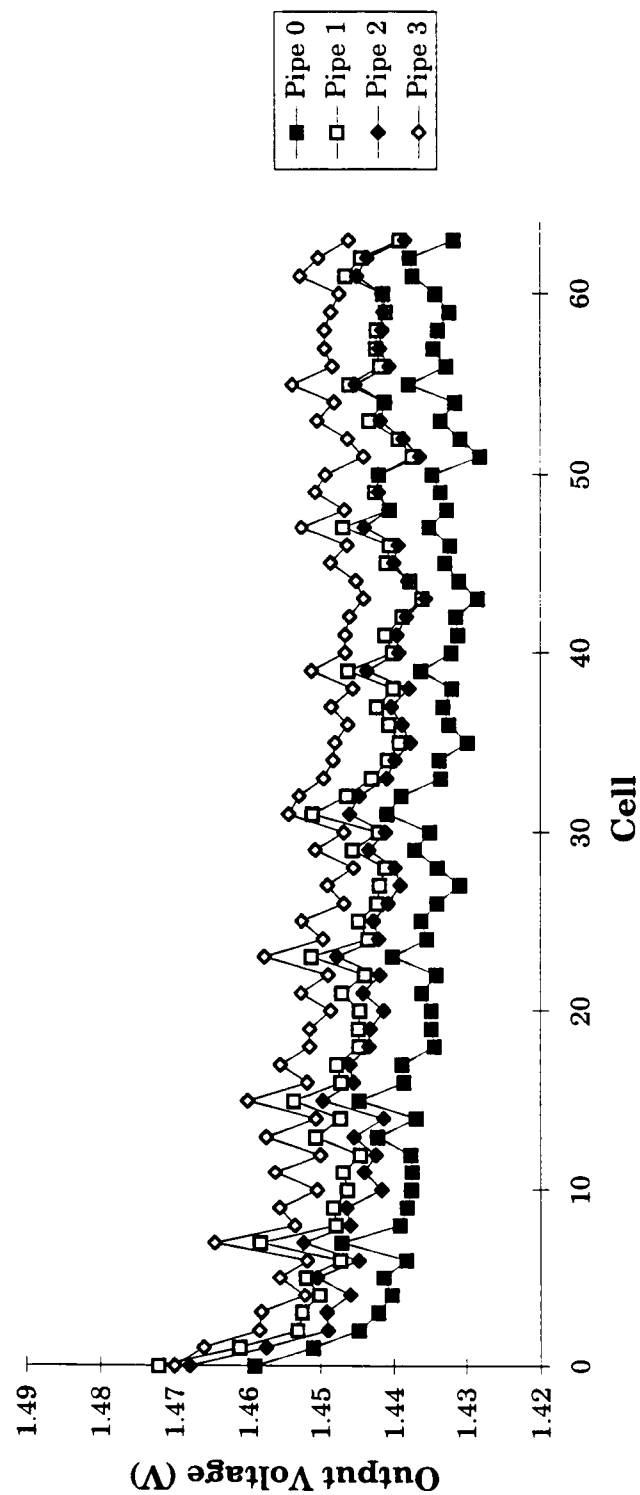
D99, Even, 1.5 Volt Input, Single Shot, 10MHz Binary Write.



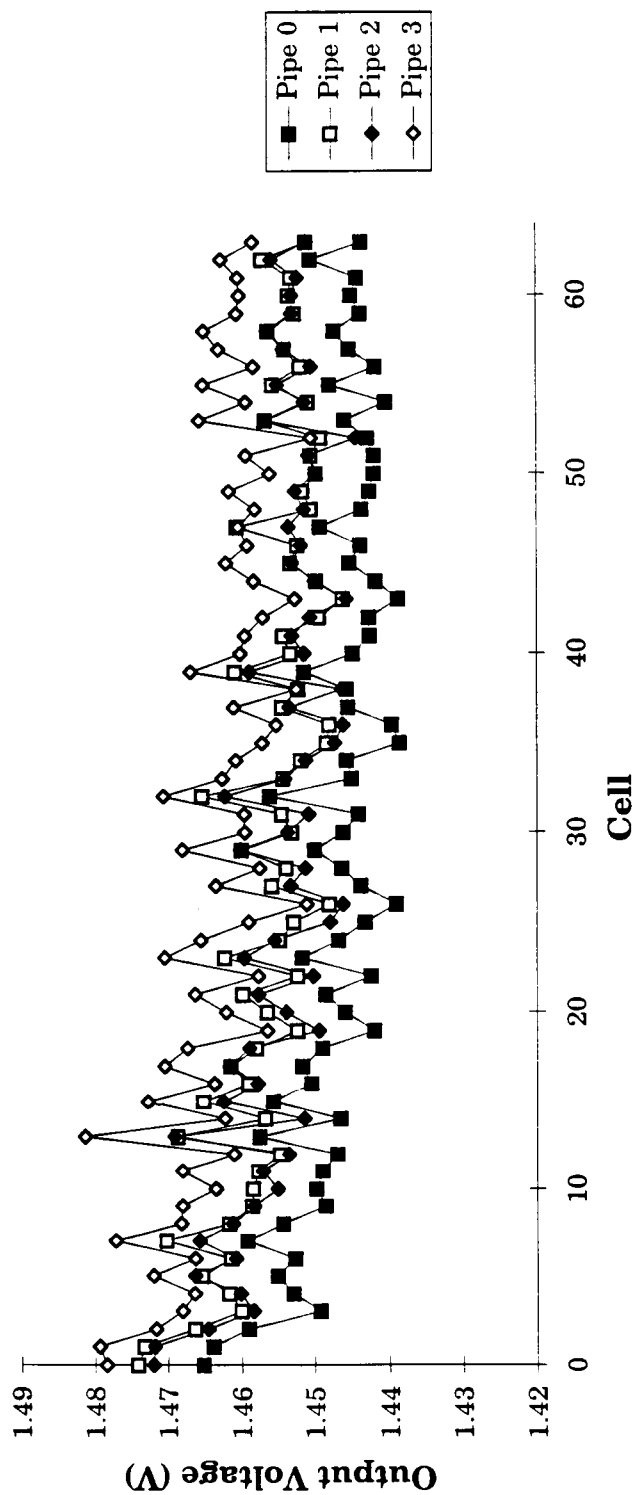
D99, Odd, 1.5 Volt Input, Average, 47.5MHz Binary Write.



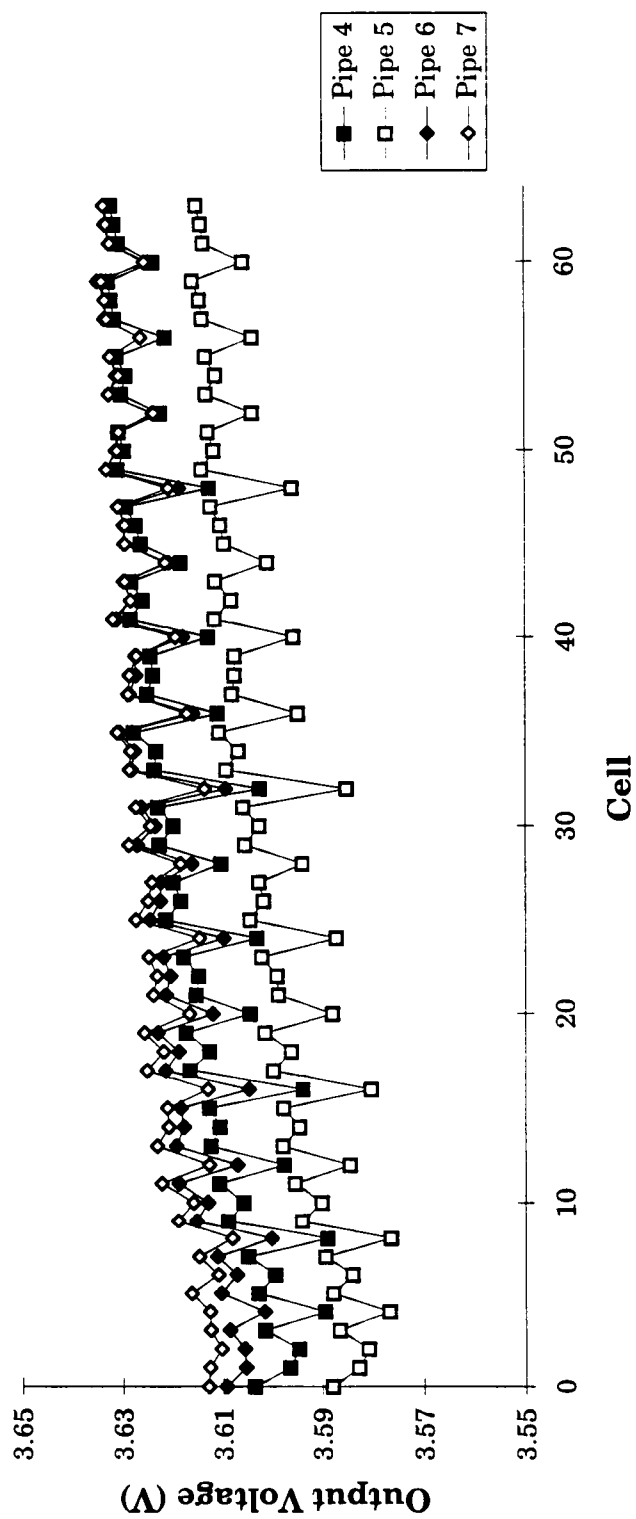
D99, Odd, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.



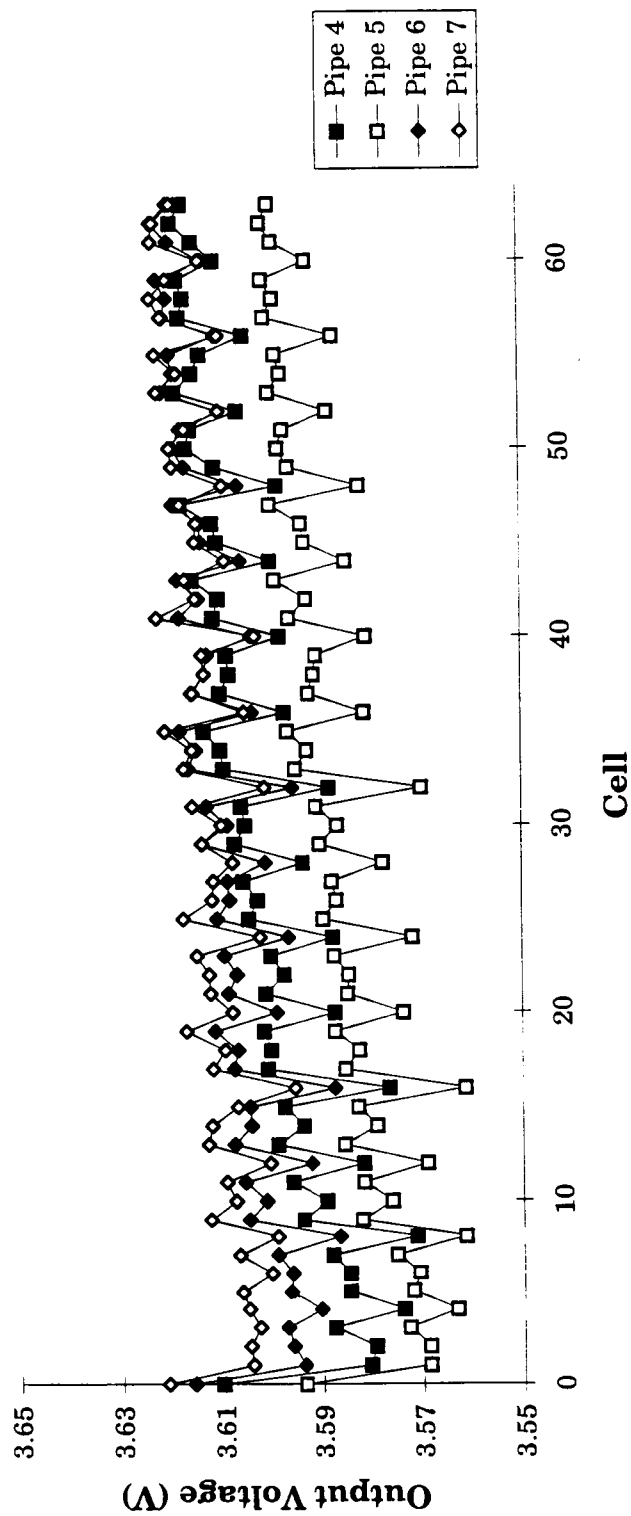
D99, Even, 1.5 Volt Input, Average, 47.5MHz Binary Write.



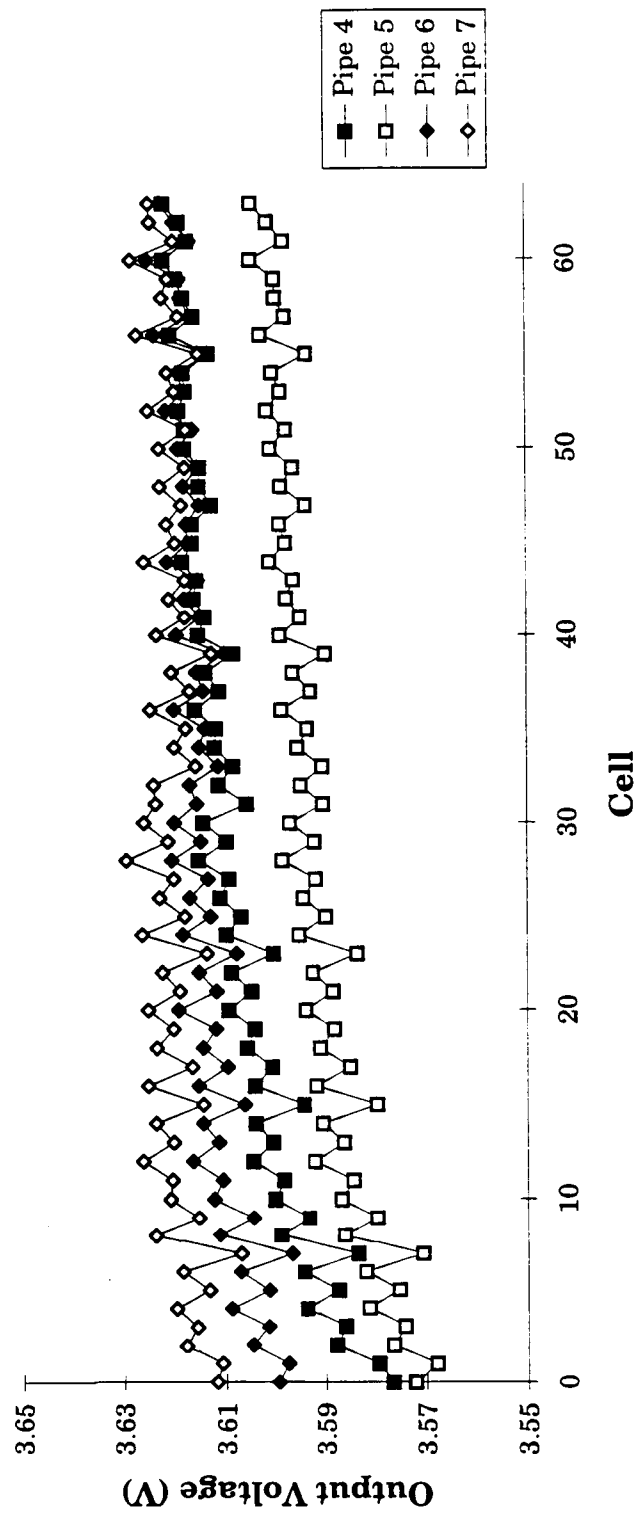
D99, Even, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.



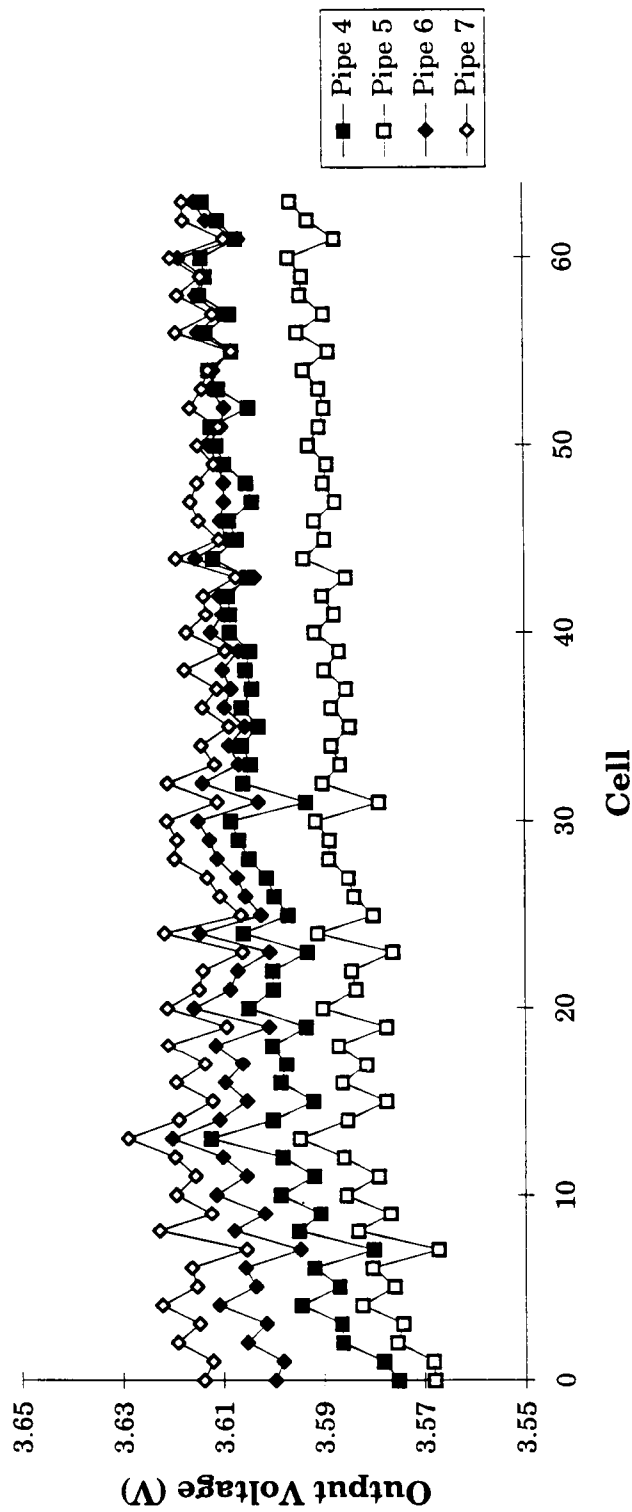
D99, Odd, 1.5 Volt Input, Average, 47.5MHz Binary Write.



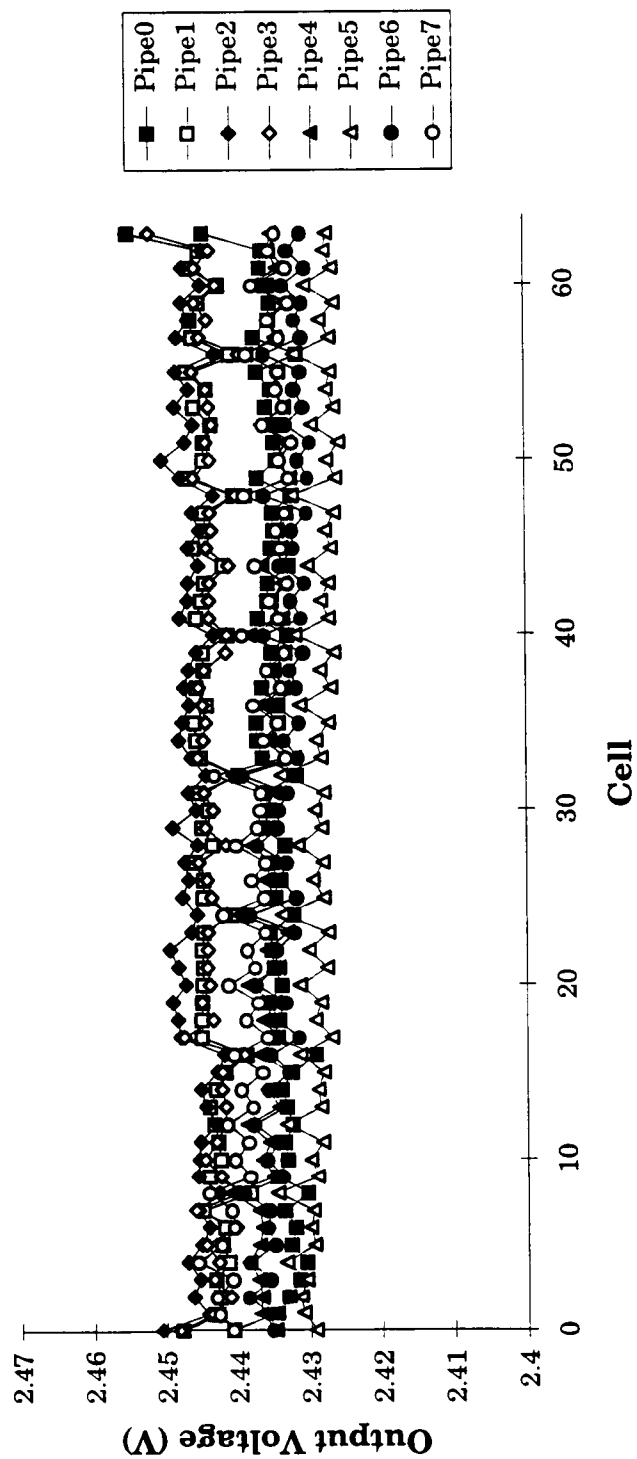
D99, Odd, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write



D99, Even, 1.5 Volt Input, Average, 47.5MHz Binary Write.

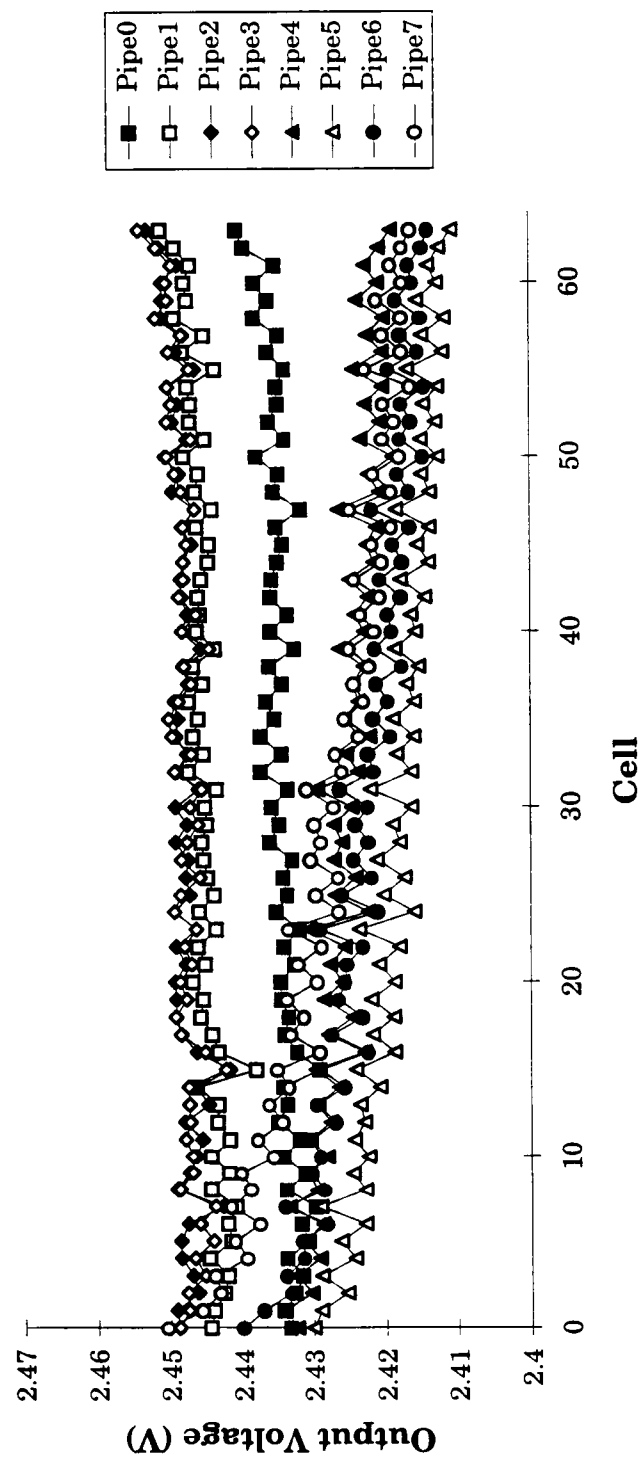


D99, Even, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.

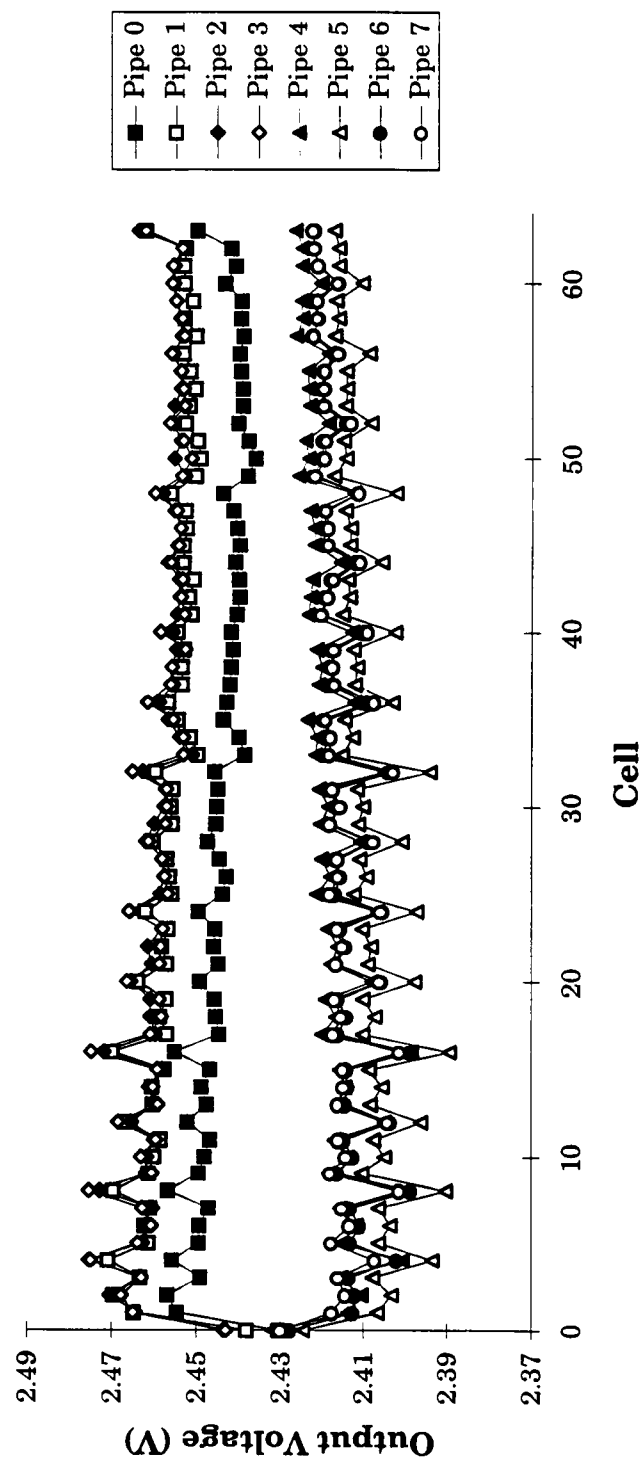


D99, Odd, 2.5 Volt Input, Average, 10MHz Binary Write

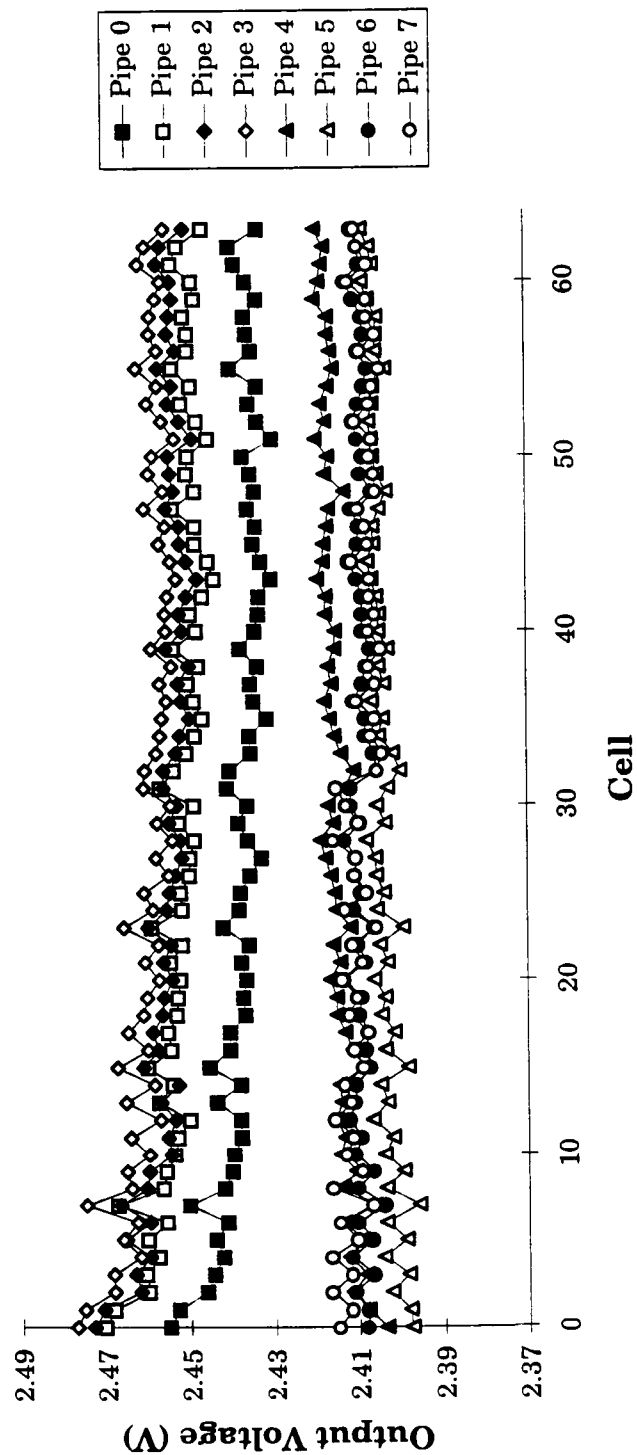
Plate 6. Chip D99, 2.5V input.



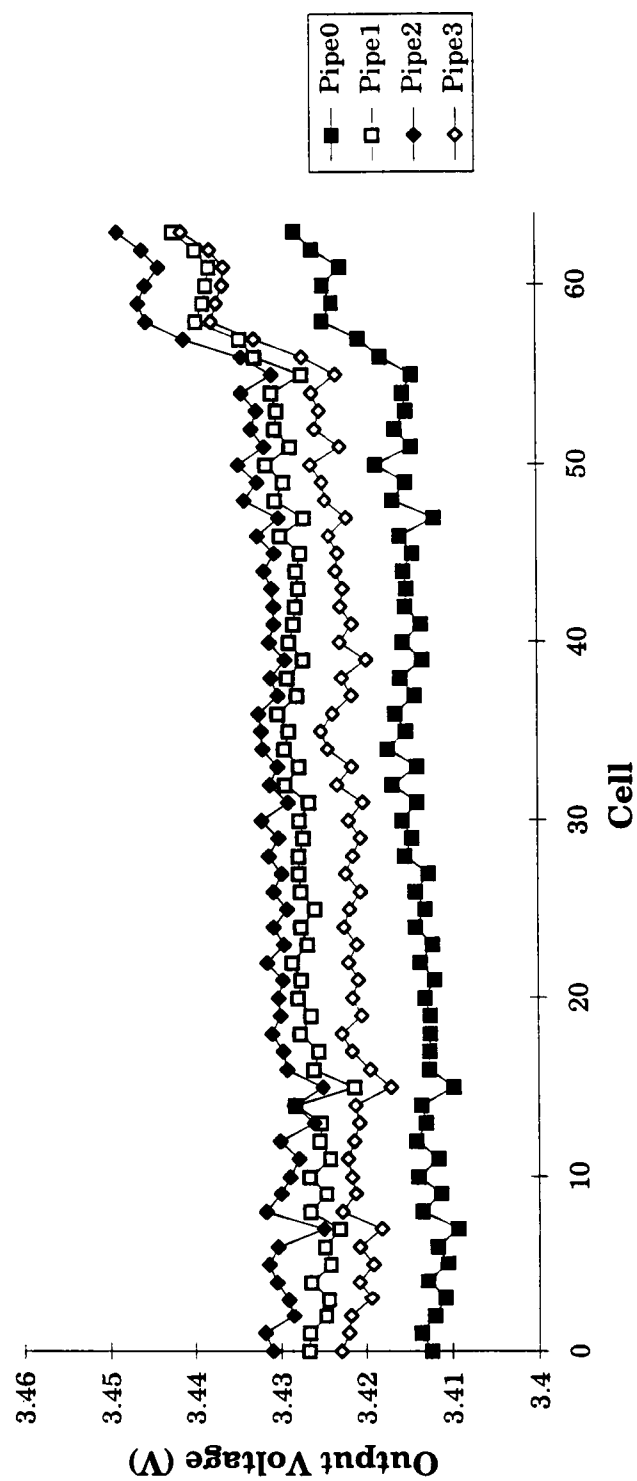
D99, Even, 2.5 Volt Input, Average, 10MHz Binary Write



D99, Odd, 2.5 Volt Input, Average, 47.5MHz Binary Write.

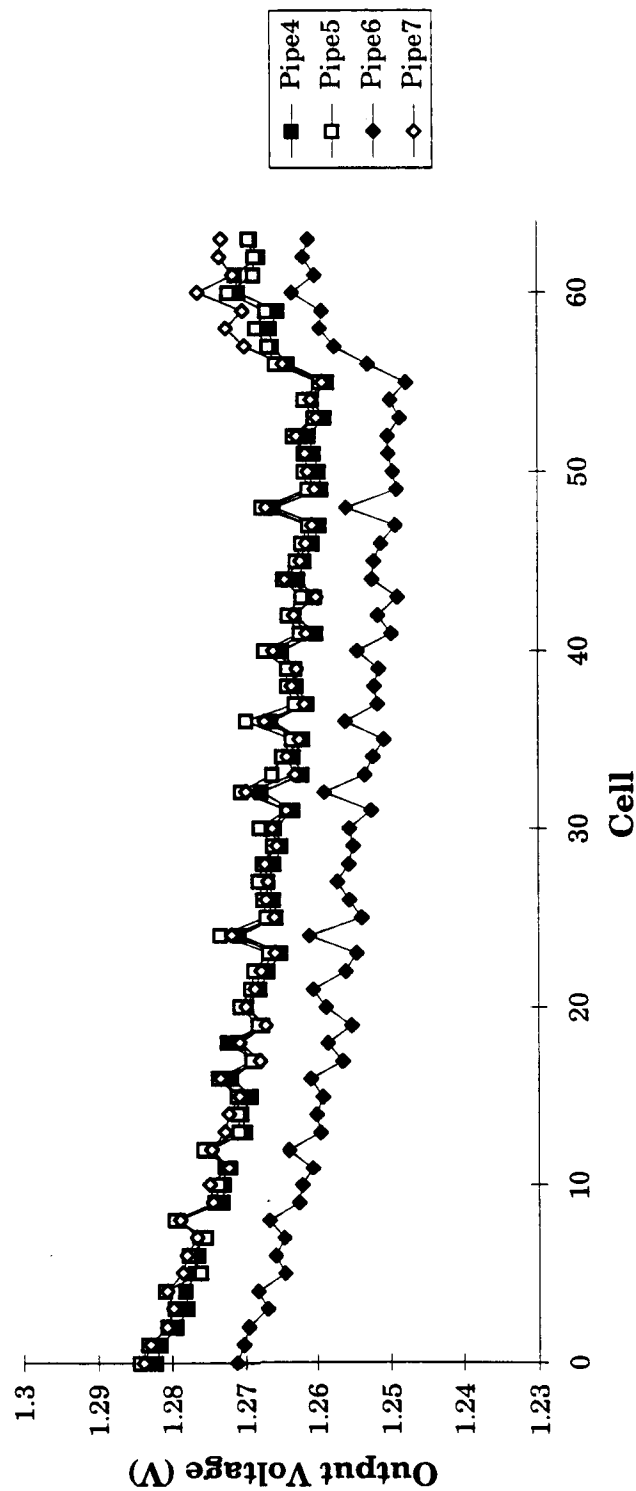


D99, Even, 2.5 Volt Input, Average, 47.5MHz Binary Write.

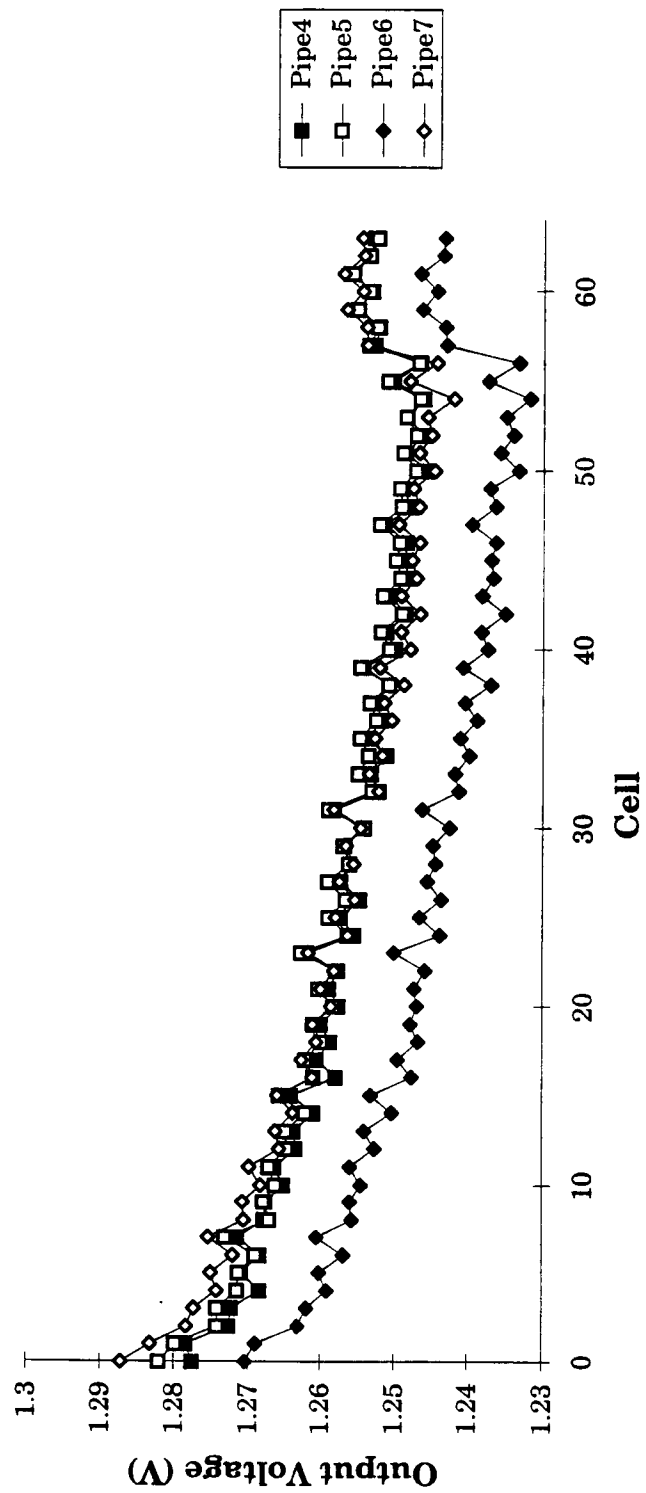


D99, Even, 3.5 Volt Input, Average, 10MHz Binary Write.

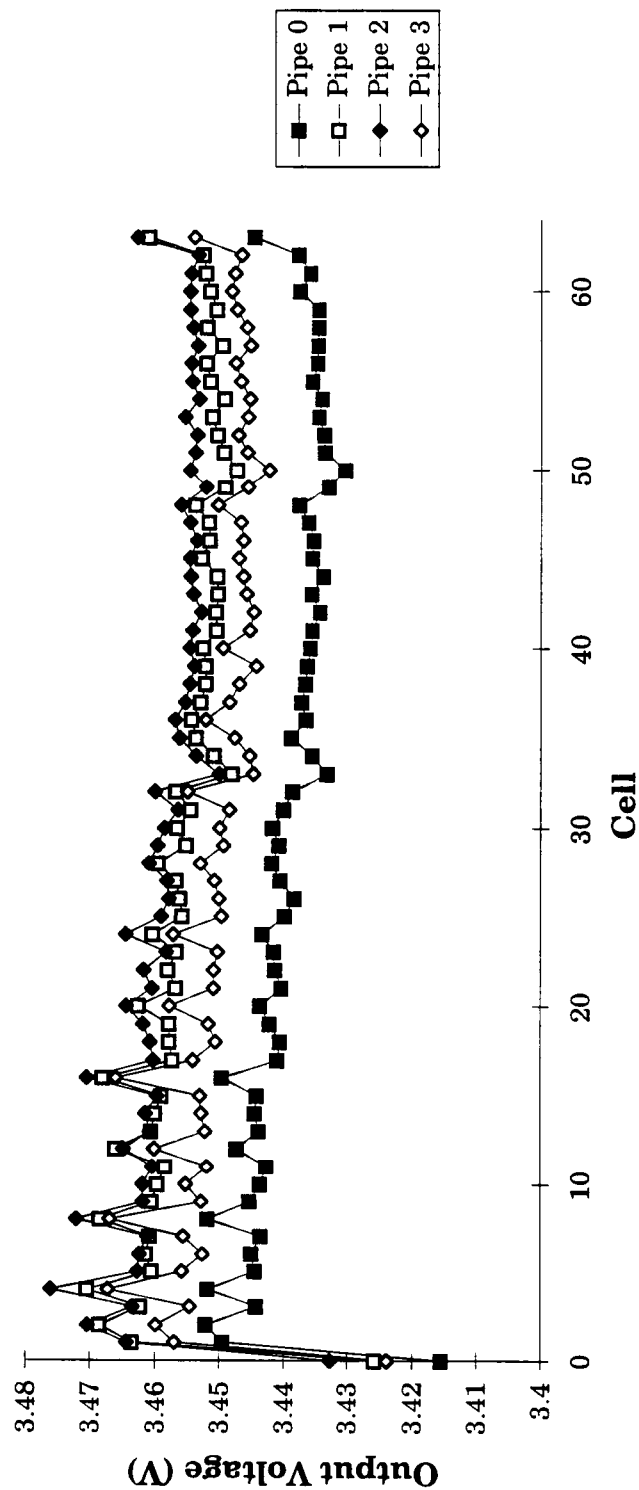
Plate 7. Chip D99, 3.5V input.



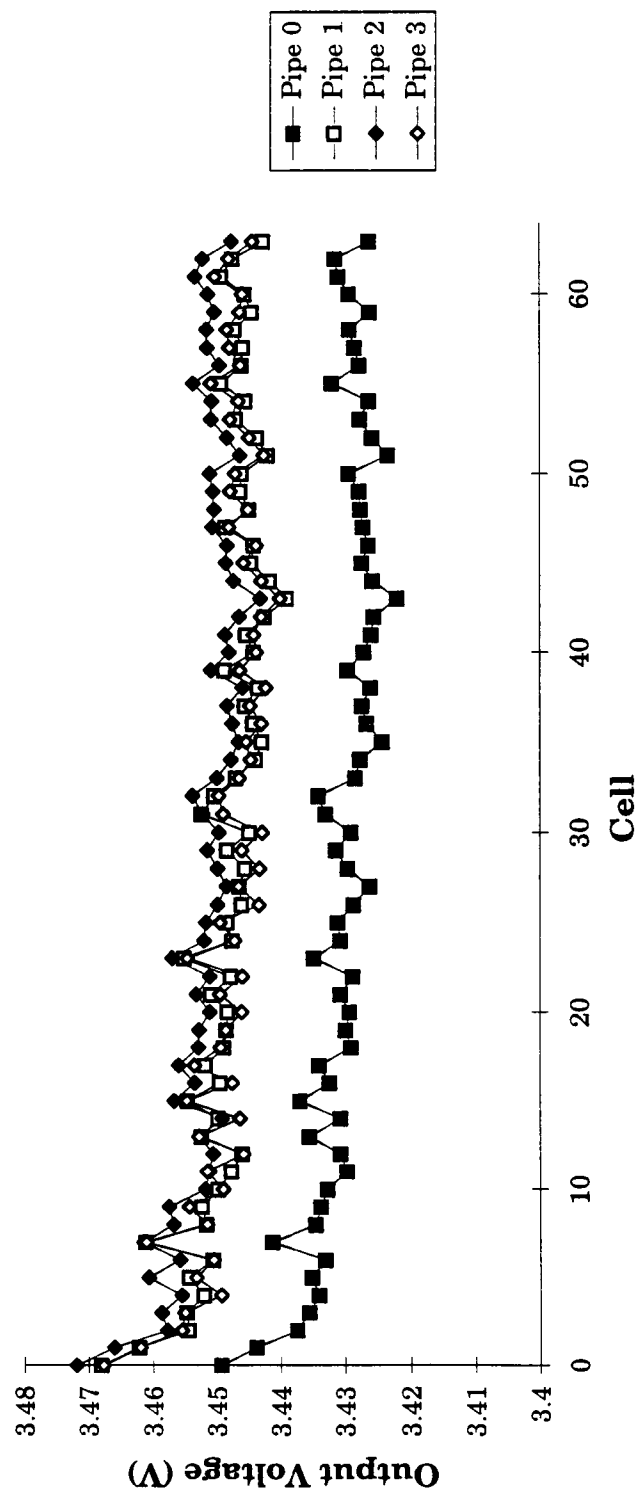
D99, Odd, 3.5 Volt Input, Average, 10MHz Binary Write.



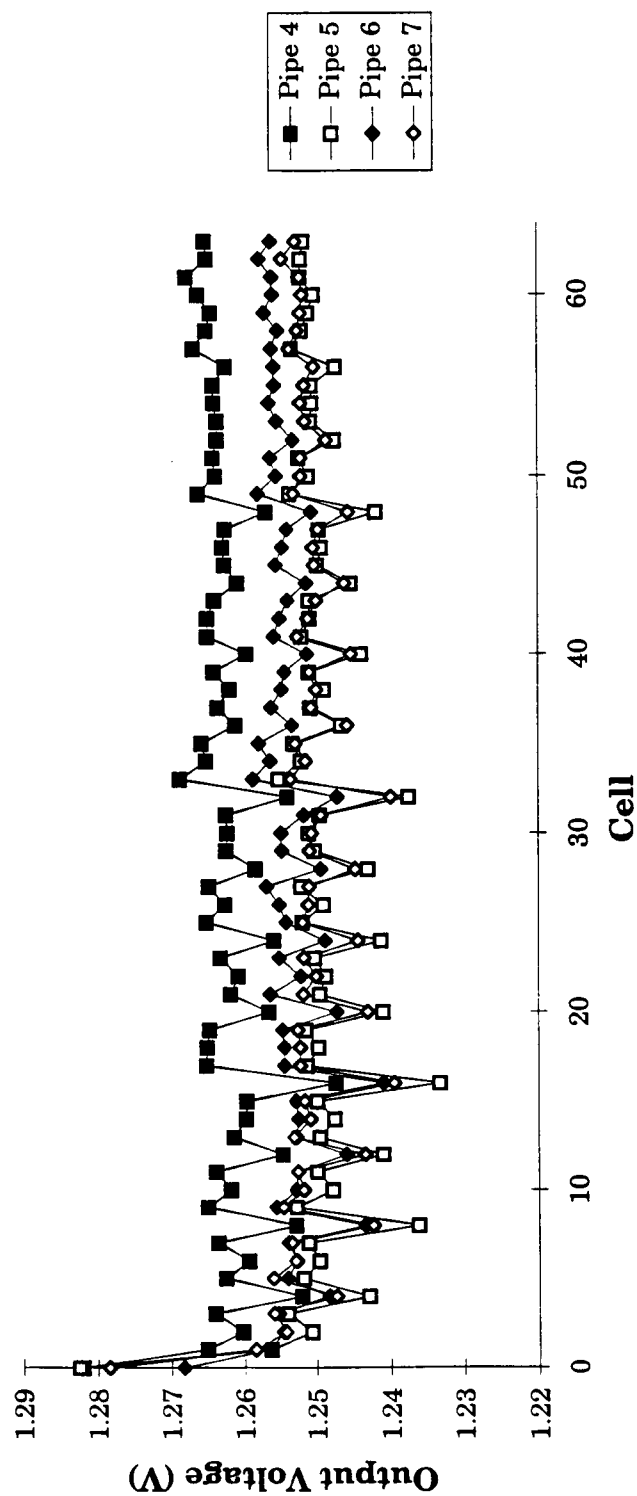
D99, Even, 3.5 Volt Input, Average, 10MHz Binary Write.



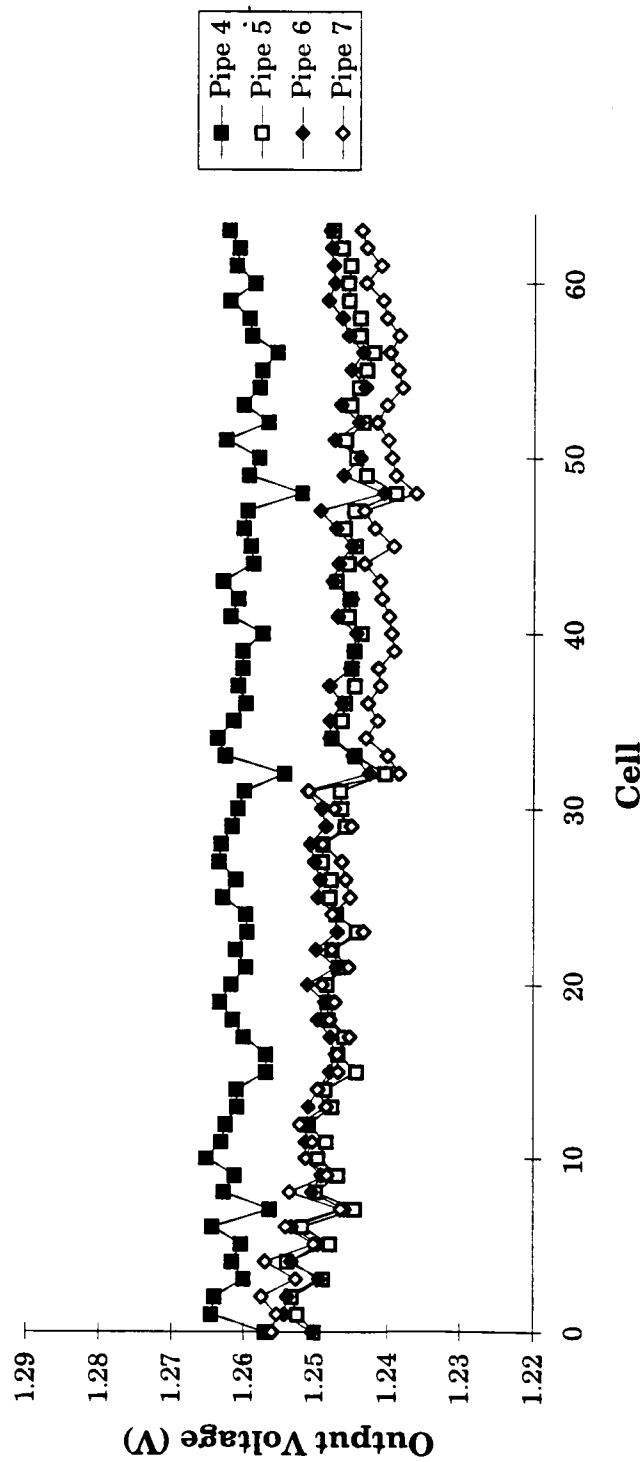
D99, Odd, 3.5 Volt Input, Average, 47.5MHz Binary Write.



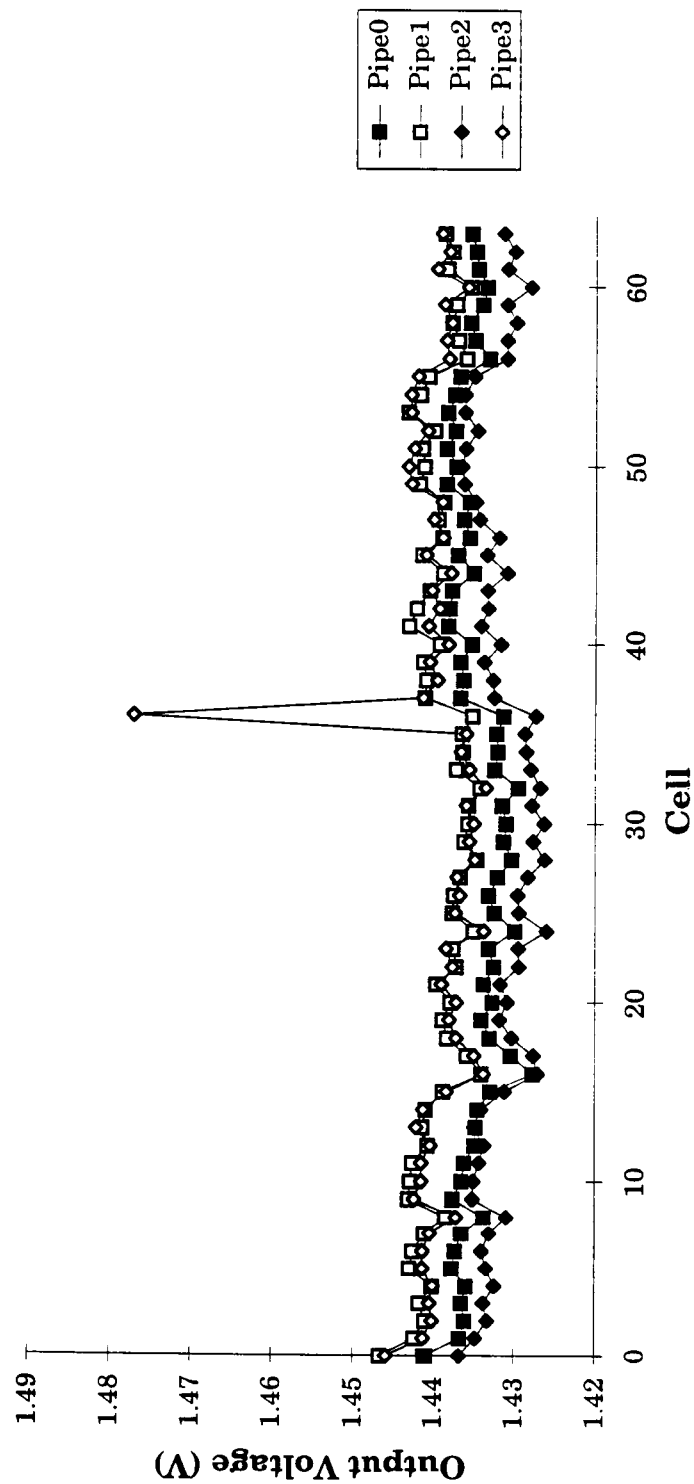
D99, Even, 3.5 Volt Input, Average, 47.5MHz Binary Write.



D99, Even, 3.5 Volt Input, Average, 47.5MHz Binary Write.

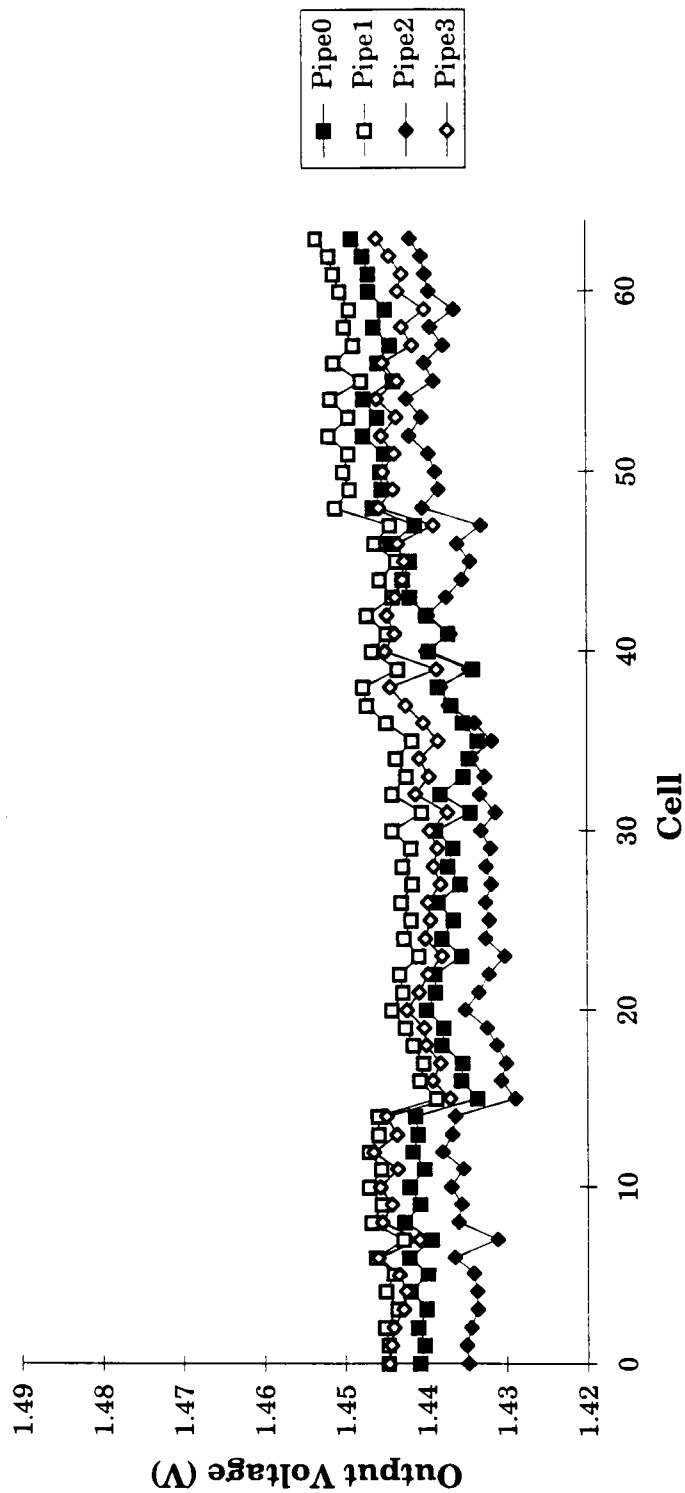


D99, Even, 3.5 Volt Input, Average, 47.5MHz Binary Write.

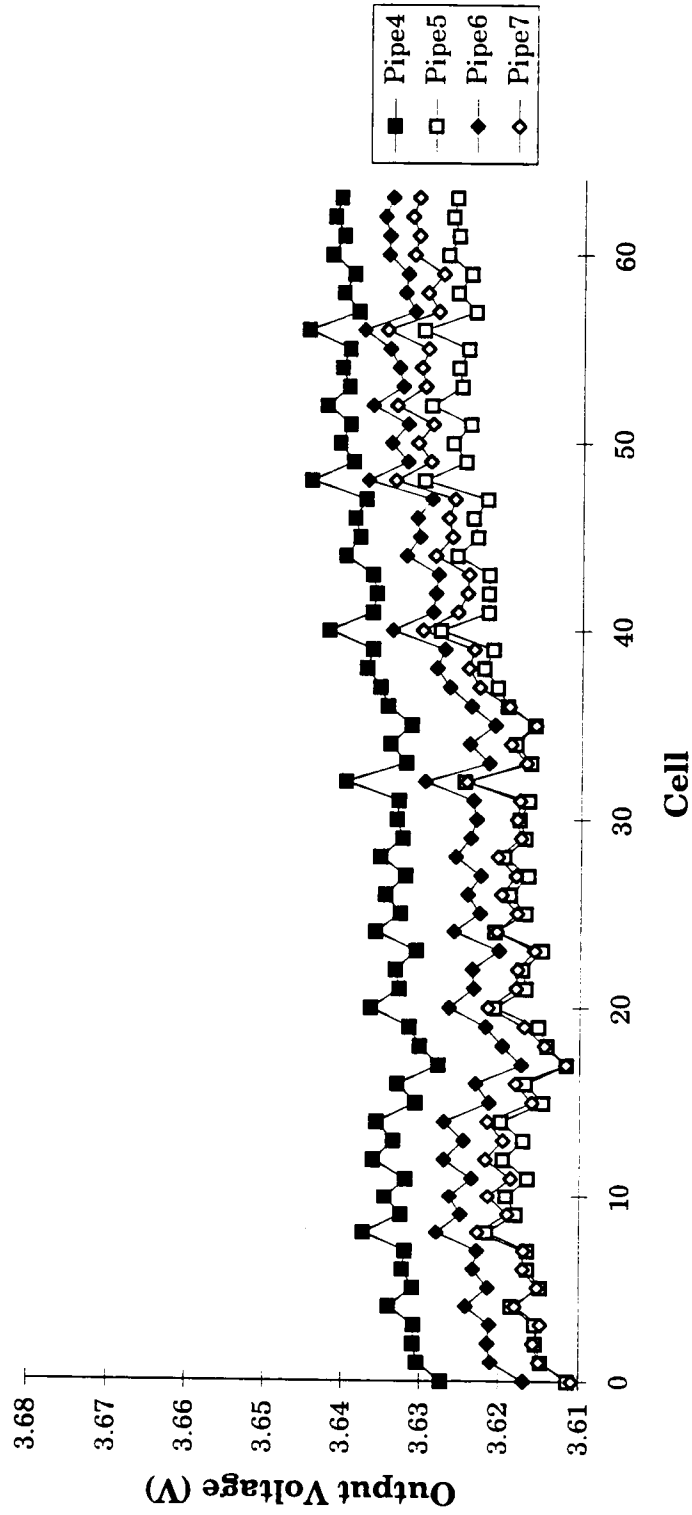


S99, Odd, 1.5 Volt Input, Average, 10MHz Binary Write.

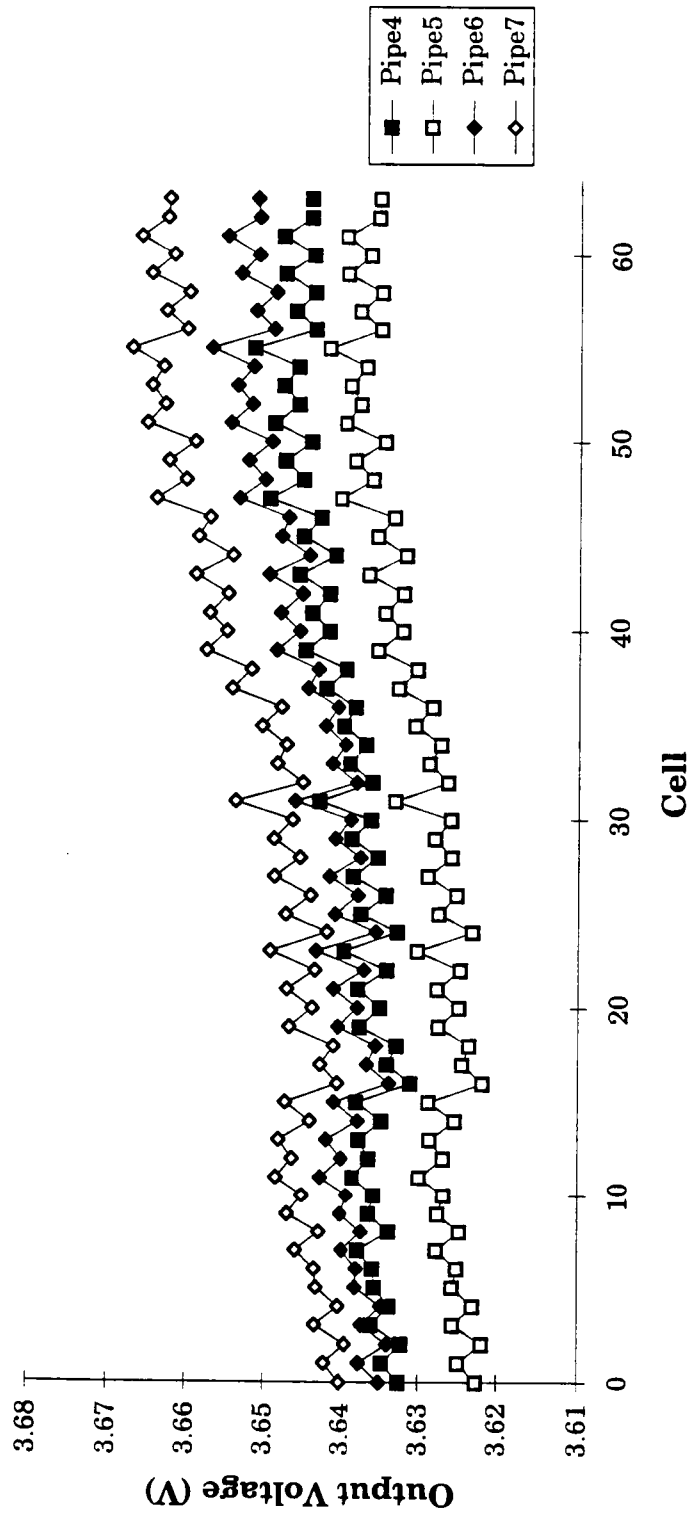
Plate 8. Chip S99, 1.5V input.



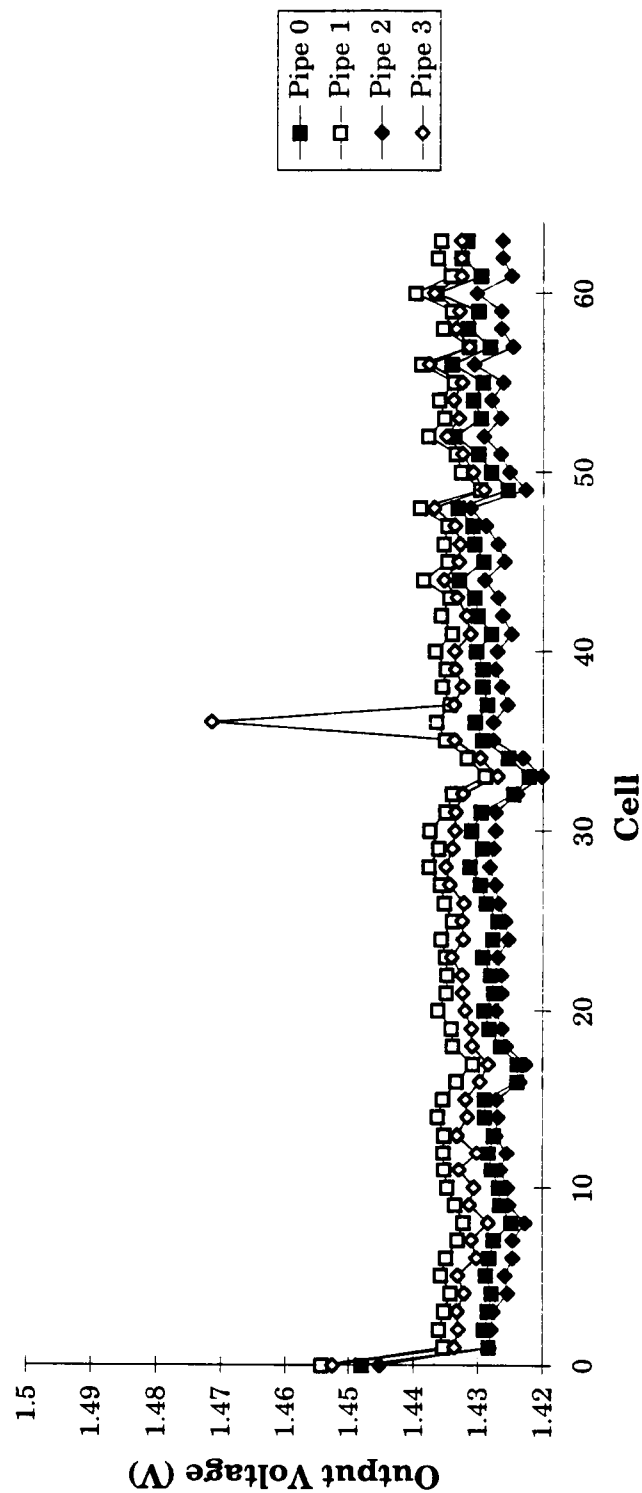
S99, Even, 1.5 Volt Input, Average, 10MHz Binary Write.



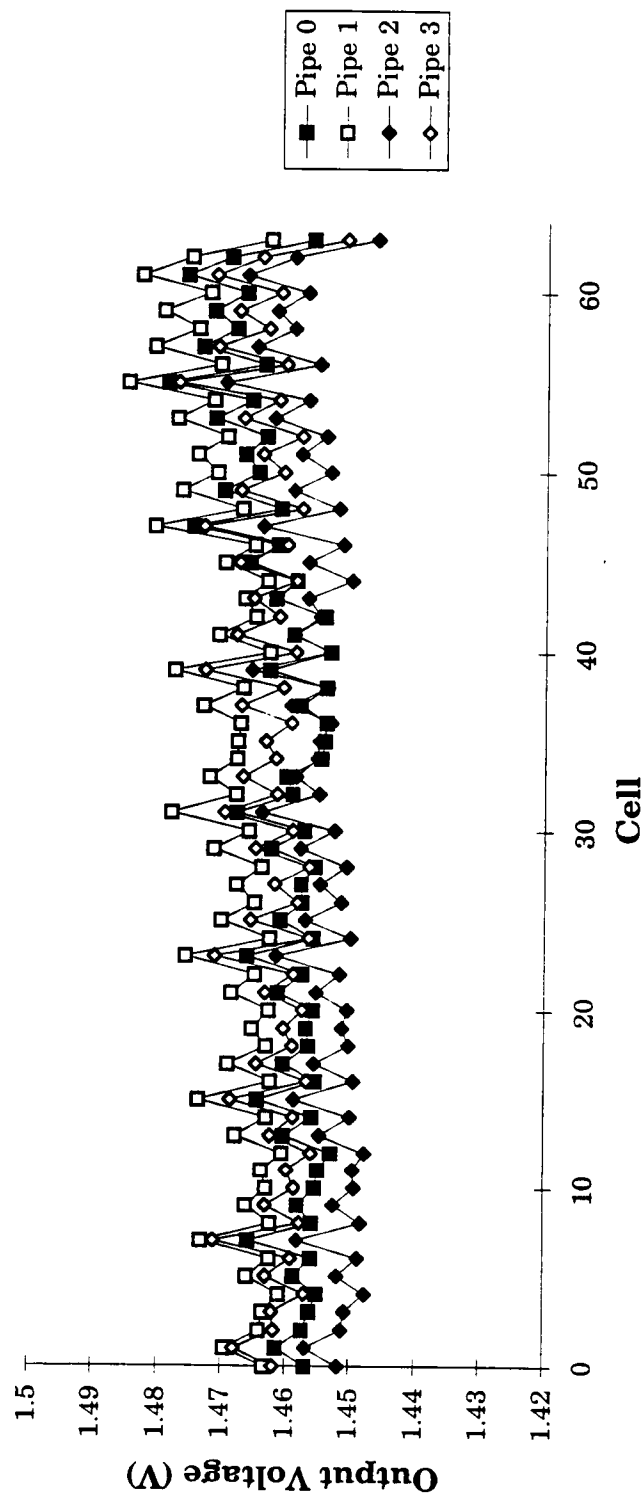
S99, Odd, 1.5 Volt Input, Average, 10MHz Binary Write.



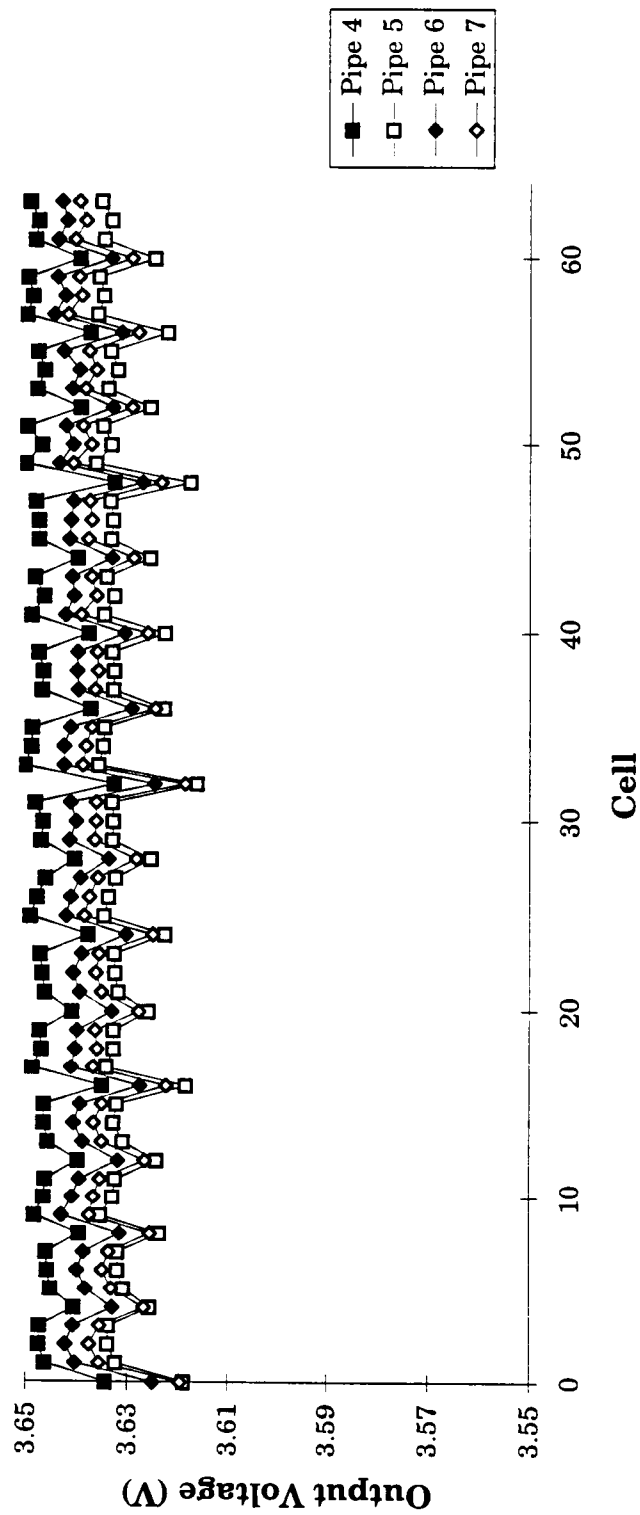
S99, Even, 1.5 Volt Input, Average, 10MHz Binary Write.



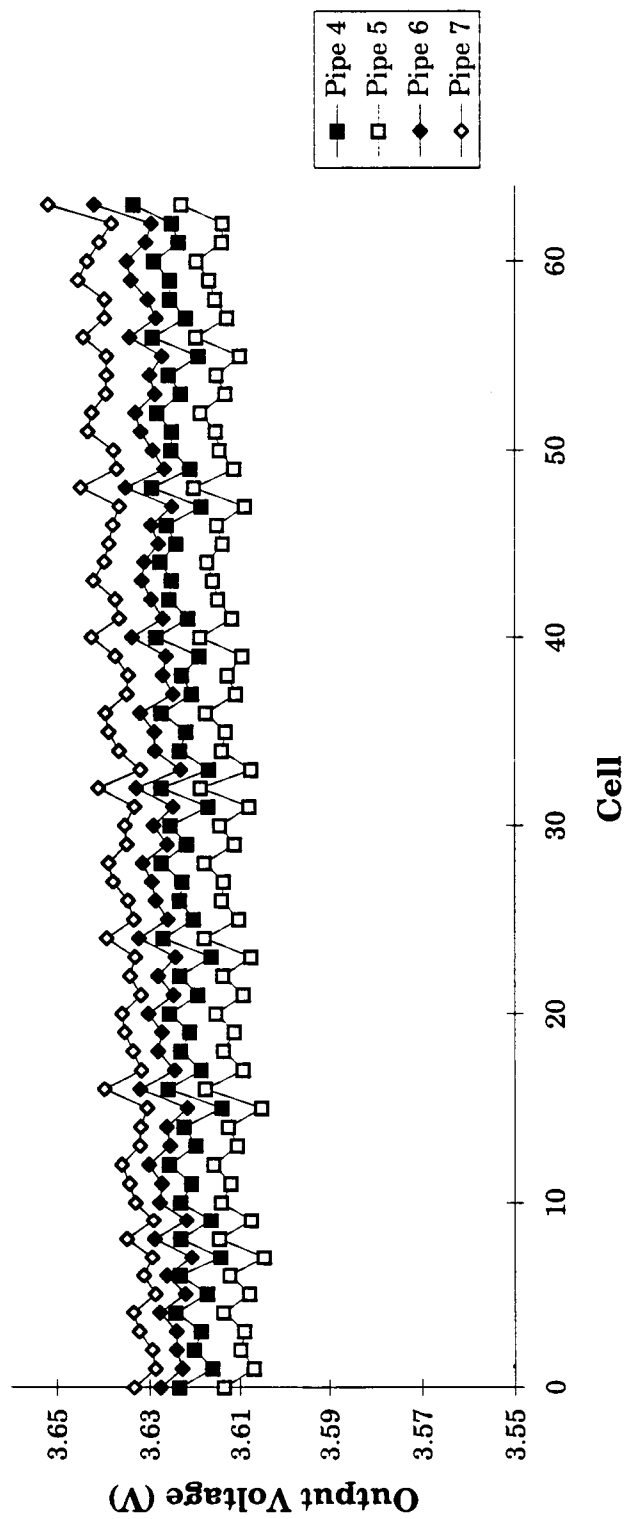
S99, Odd, 1.5 Volt Input, Average, 47.5MHz Binary Write



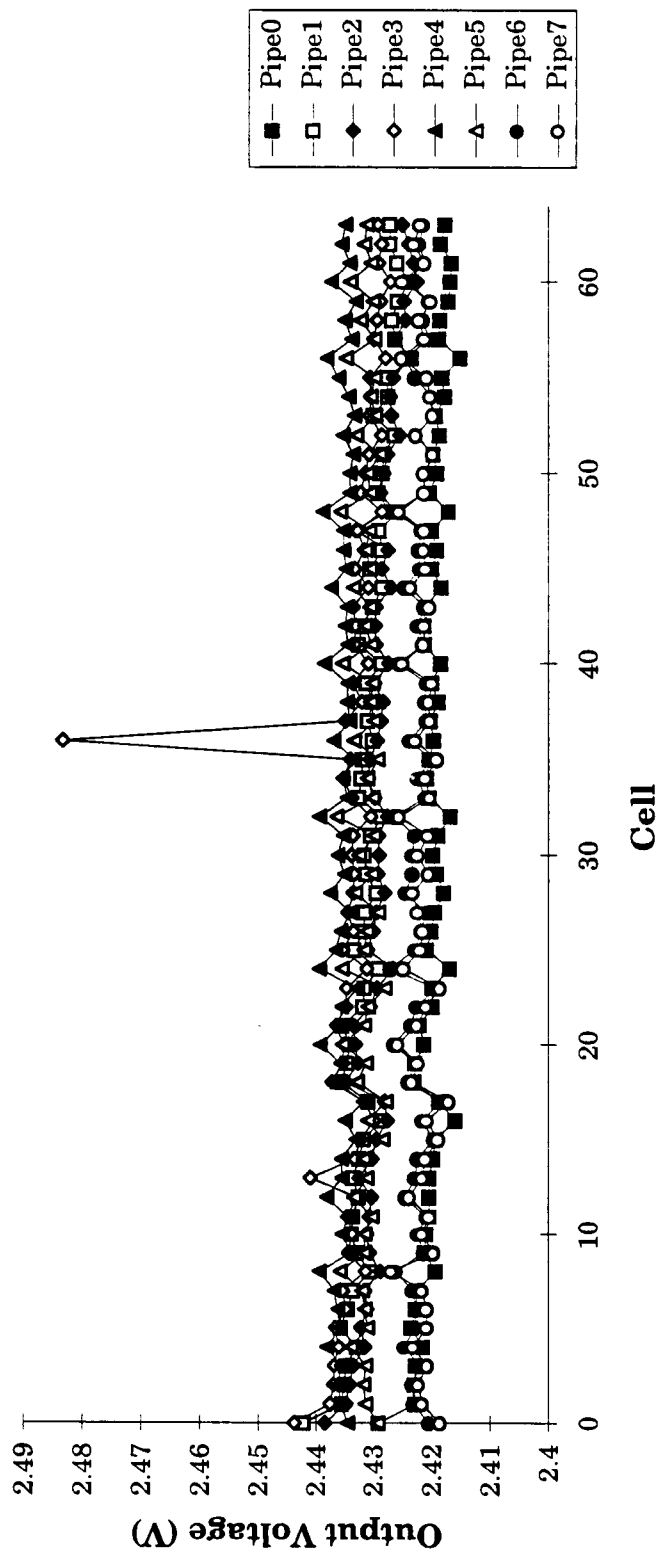
S99, Even, 1.5 Volt Input, Average, 47.5MHz Binary Write



S99, Odd, 1.5 Volt Input, Average, 47.5MHz Binary Write

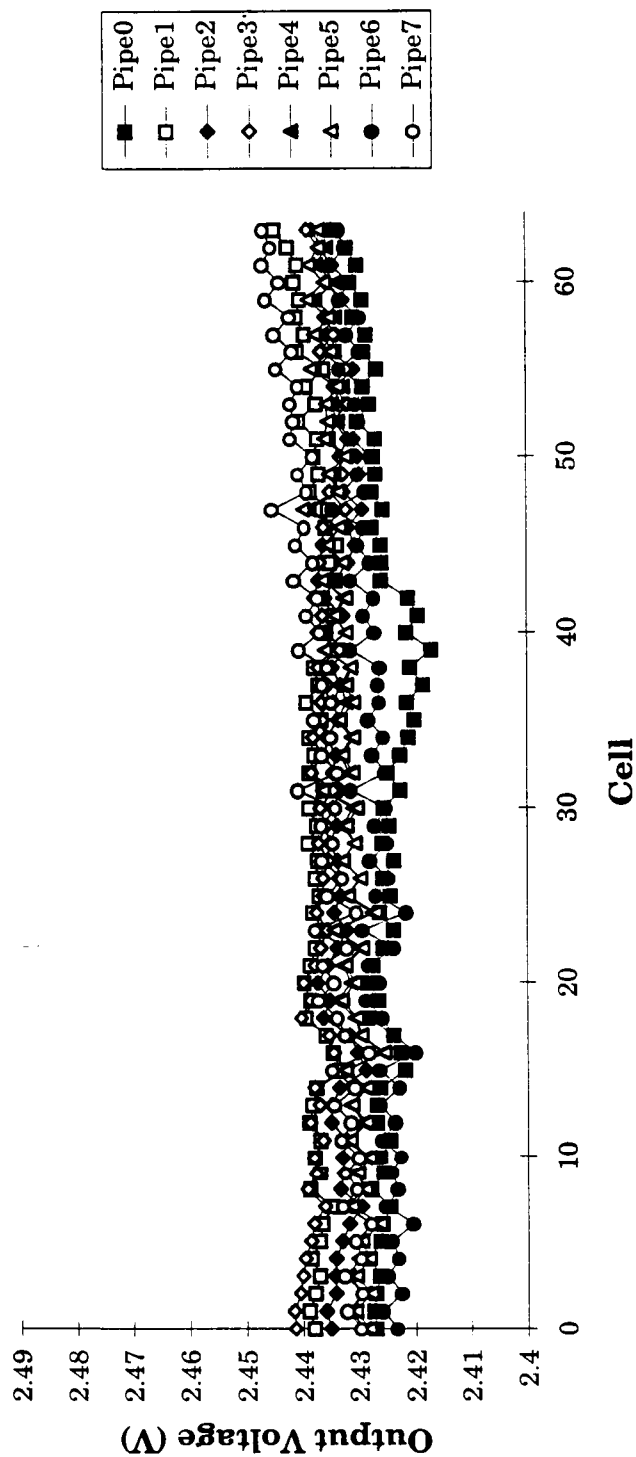


S99, Even, 1.5 Volt Input, Average, 47.5MHz Binary Write.

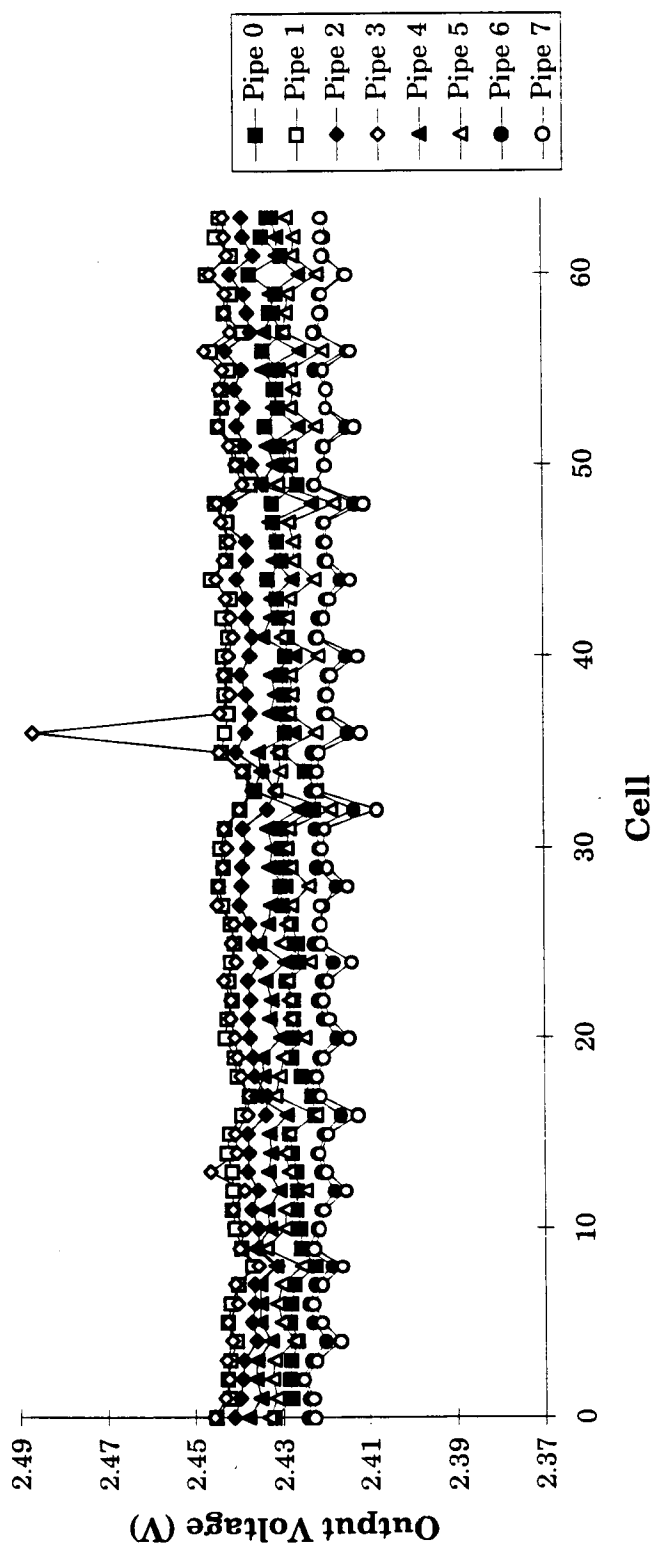


S99, Odd, 2.5 Volt Input, Average, 10MHz Binary Write.

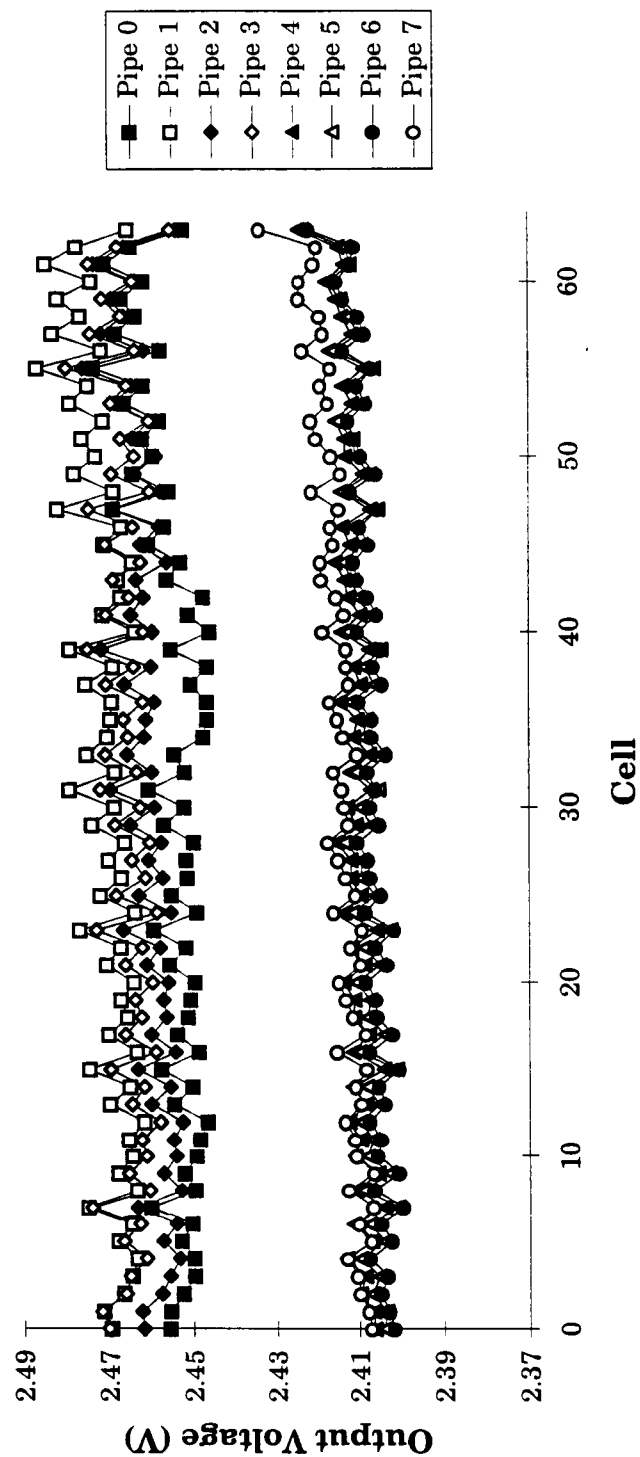
Plate 9. Chip S99, 2.5V input.



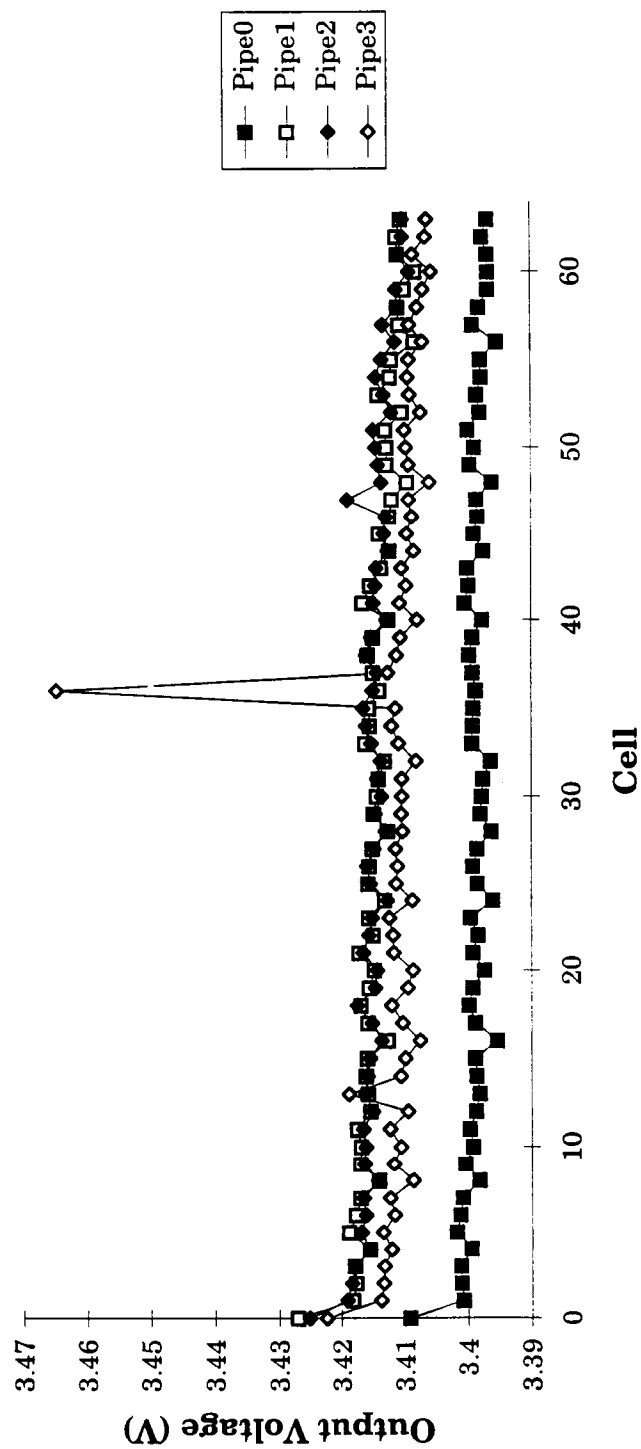
S99, Even, 2.5 Volt Input, Average, 10MHz Binary Write.



S99, Odd, 2.5 Volt Input, Average, 47.5MHz Binary Write.

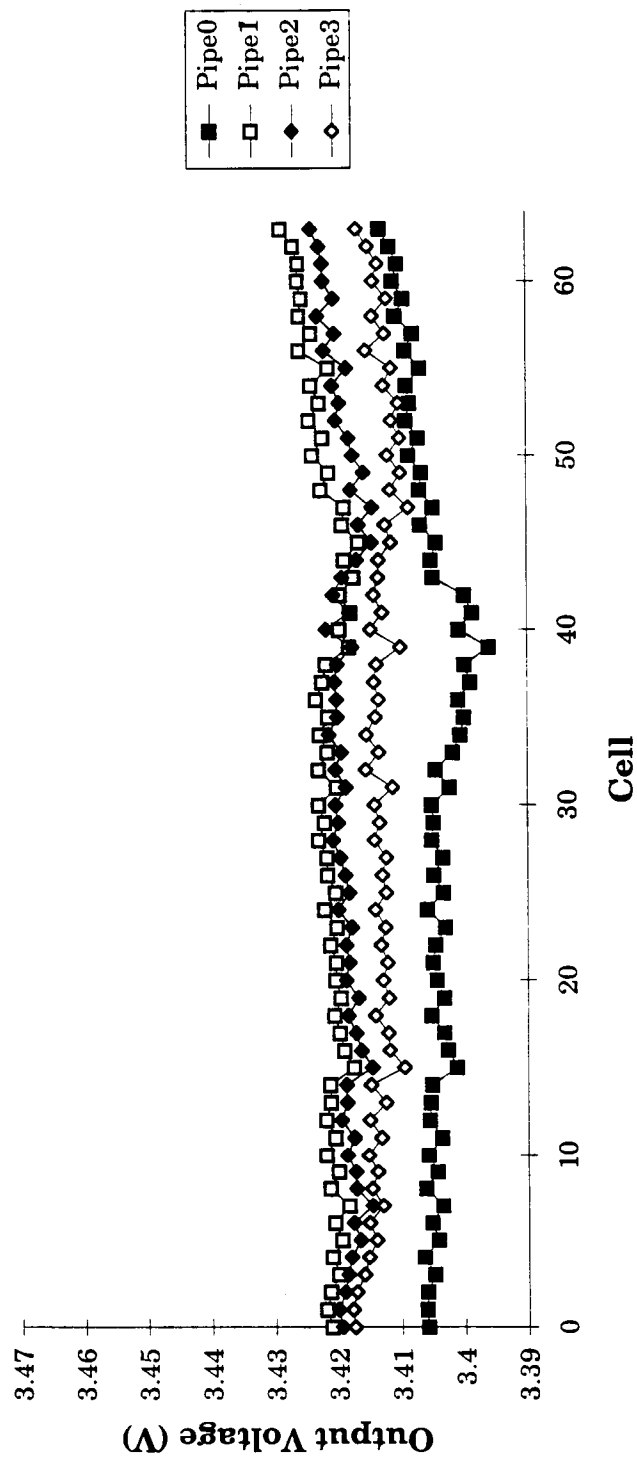


S99, Even, 2.5 Volt Input, Average, 47.5MHz Binary Write.

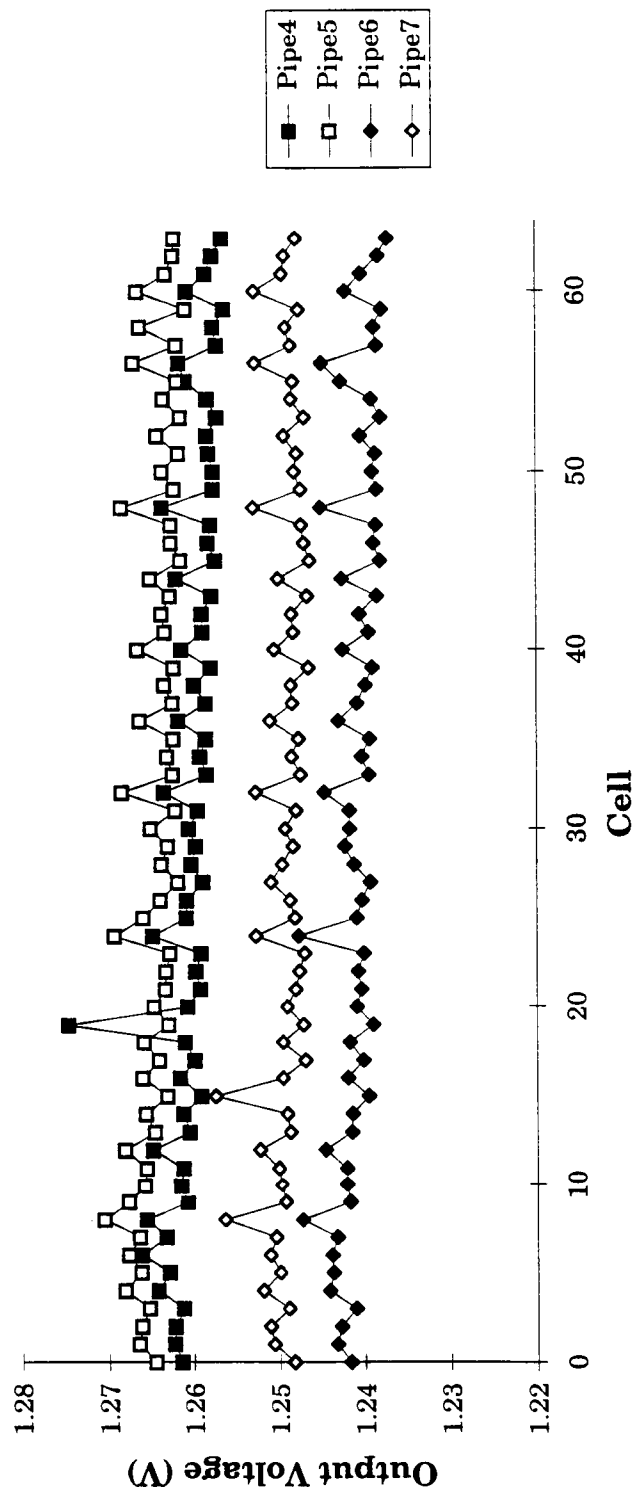


S99, Odd, 3.5 Volt Input, Average, 10MHz Binary Write.

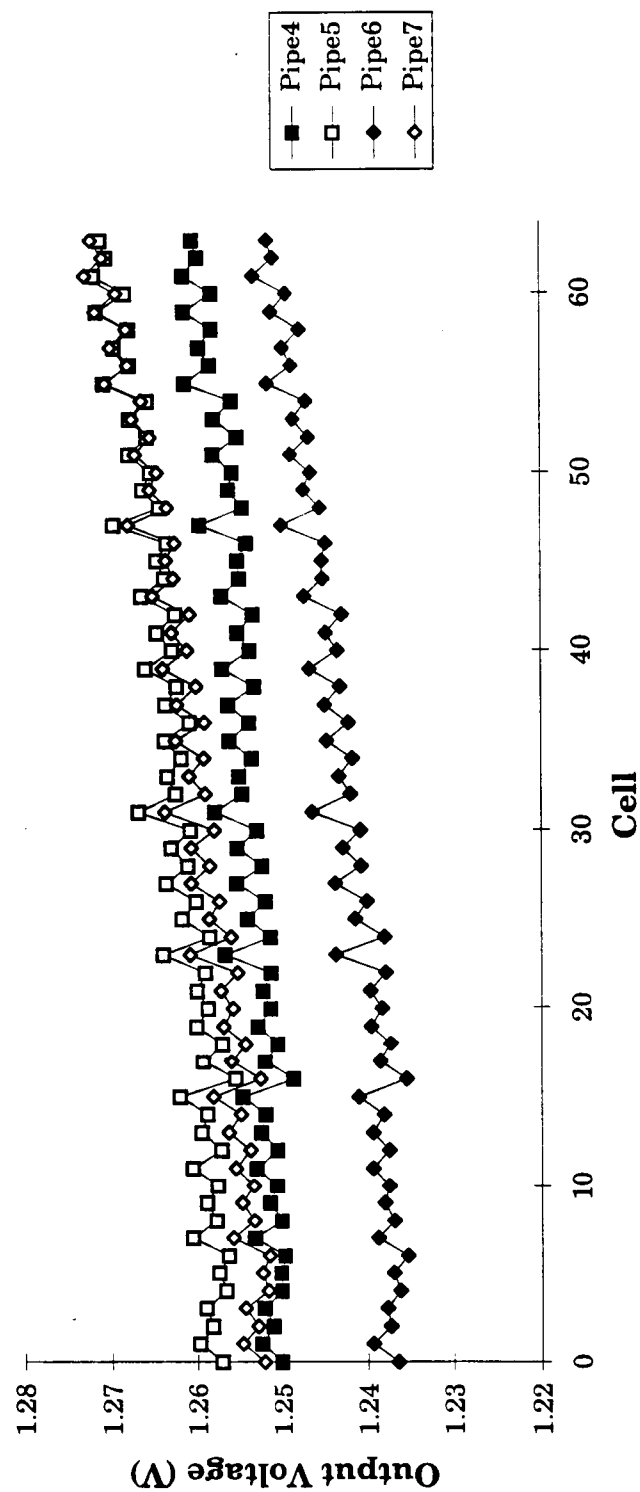
Plate 10. Chip S99, 3.5V input.



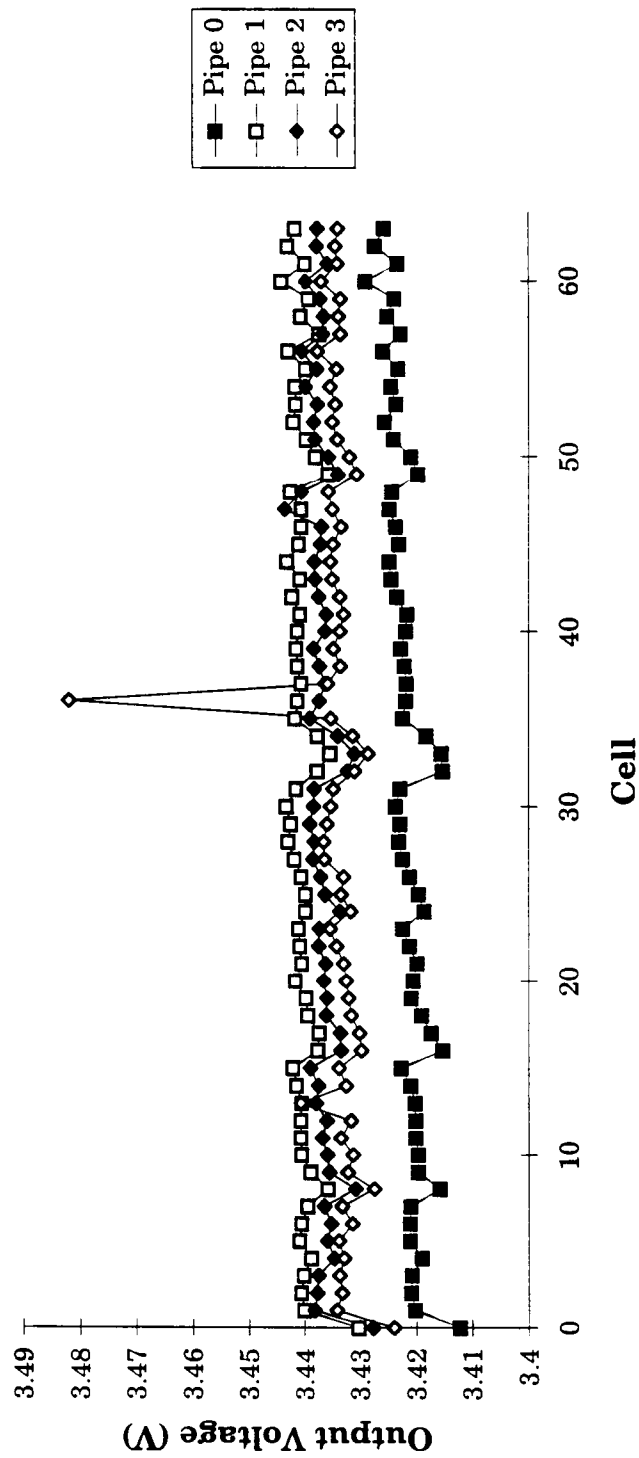
S99, Even, 3.5 Volt Input, Average, 10MHz Binary Write.



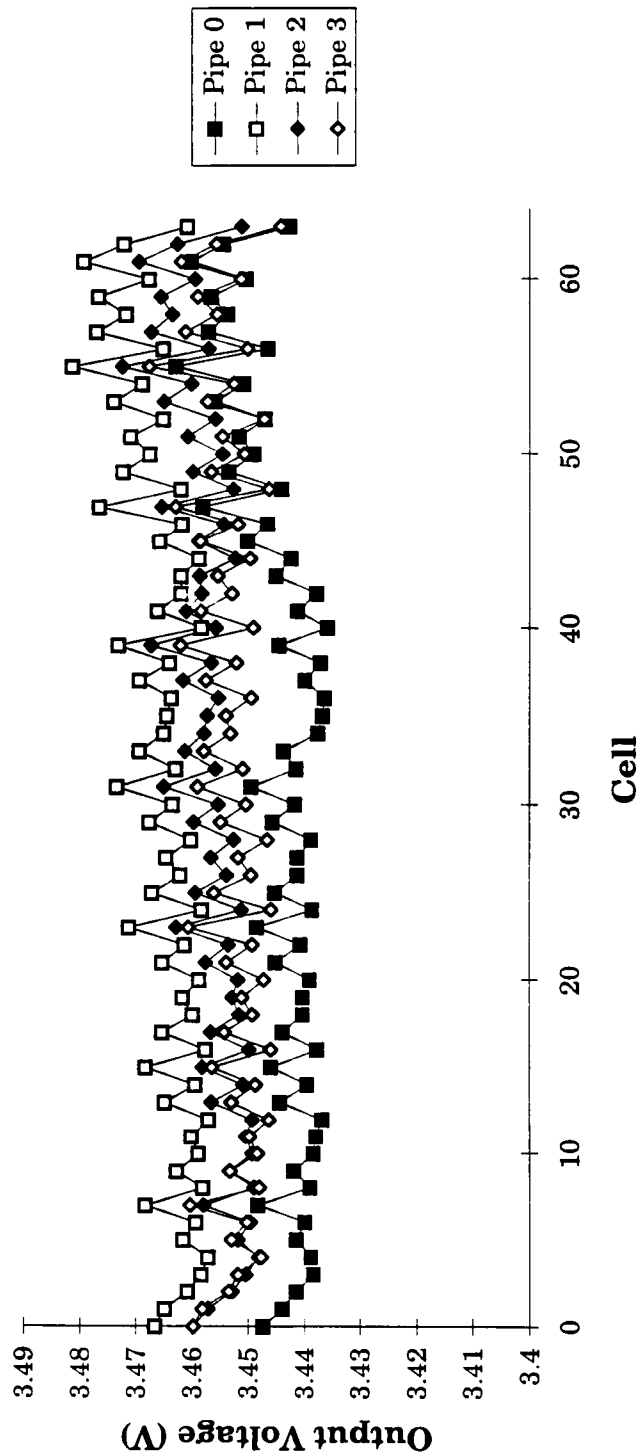
S99, Odd, 3.5 Volt Input, Average, 10MHz Binary Write.



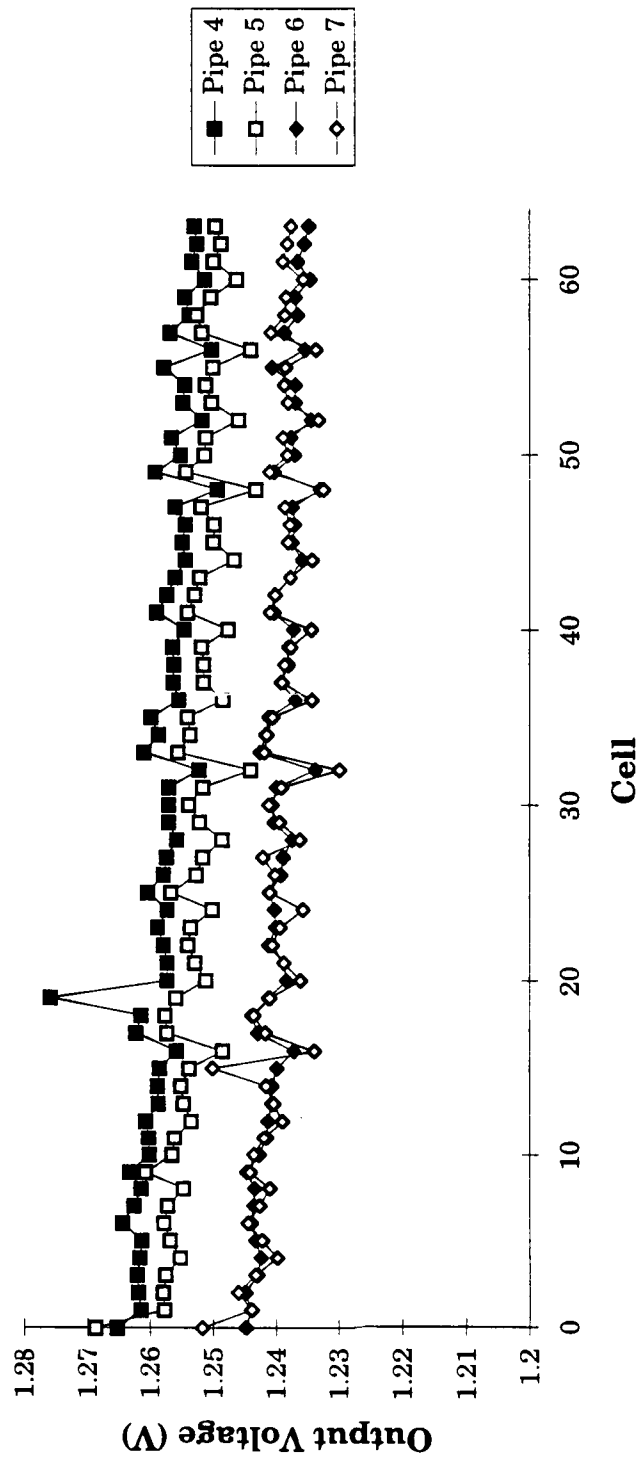
S99, Even, 3.5 Volt Input, Average, 10MHz Binary Write.



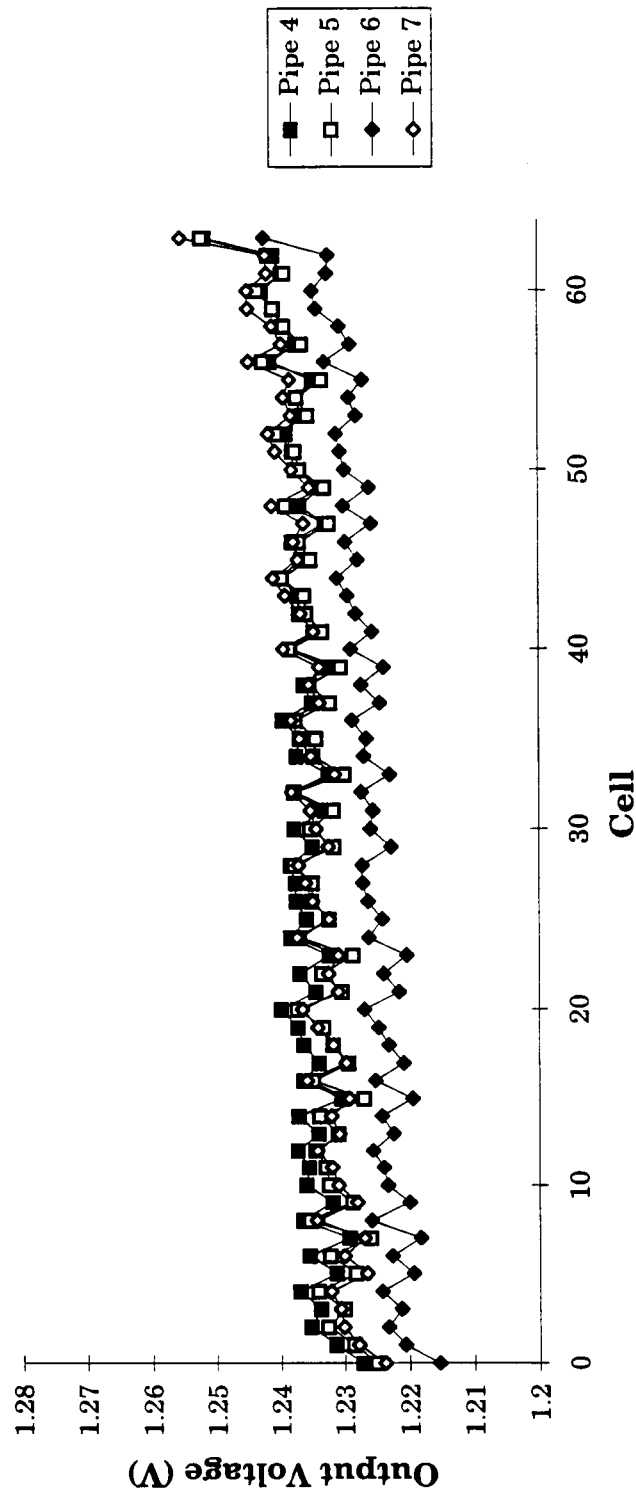
S99, Odd, 3.5 Volt Input, Average, 47.5MHz Binary Write



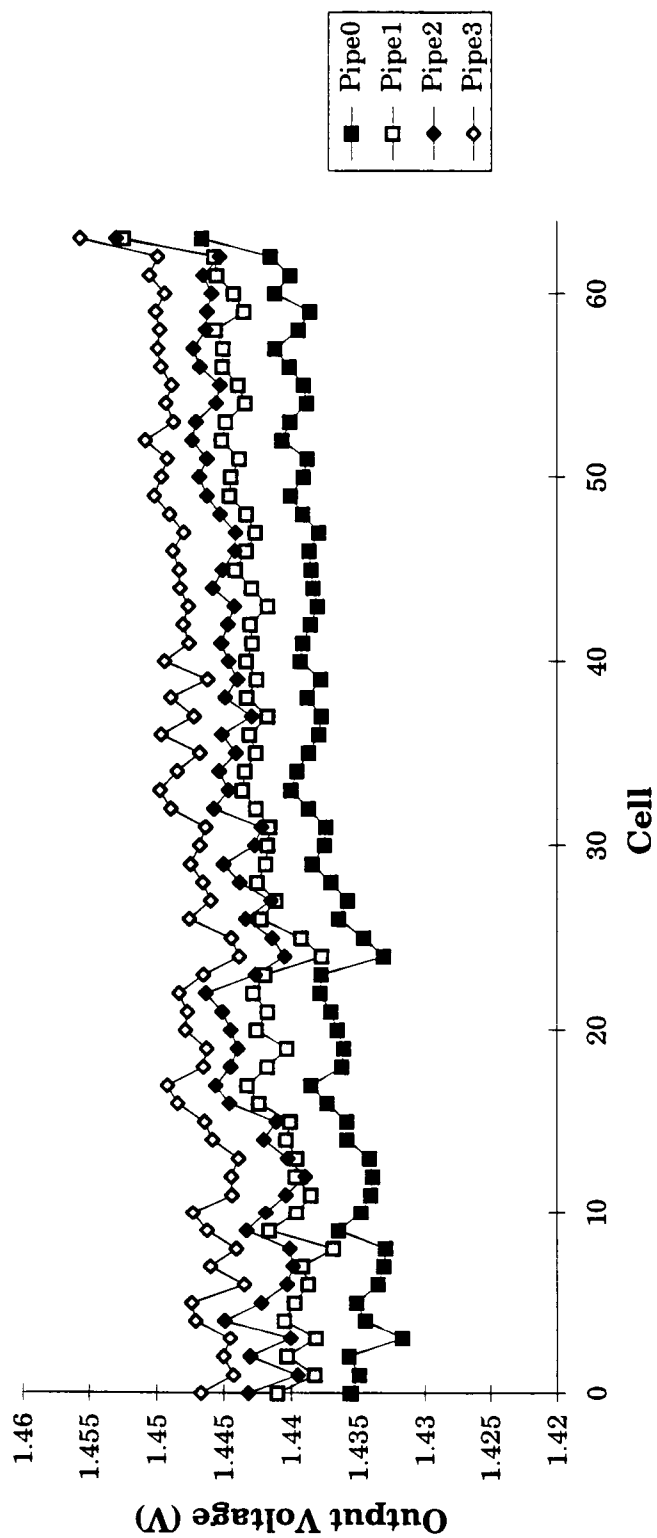
S99, Even, 3.5 Volt Input, Average, 47.5MHz Binary Write.



S99, Odd, 3.5 Volt Input, Average, 47.5MHz Binary Write.

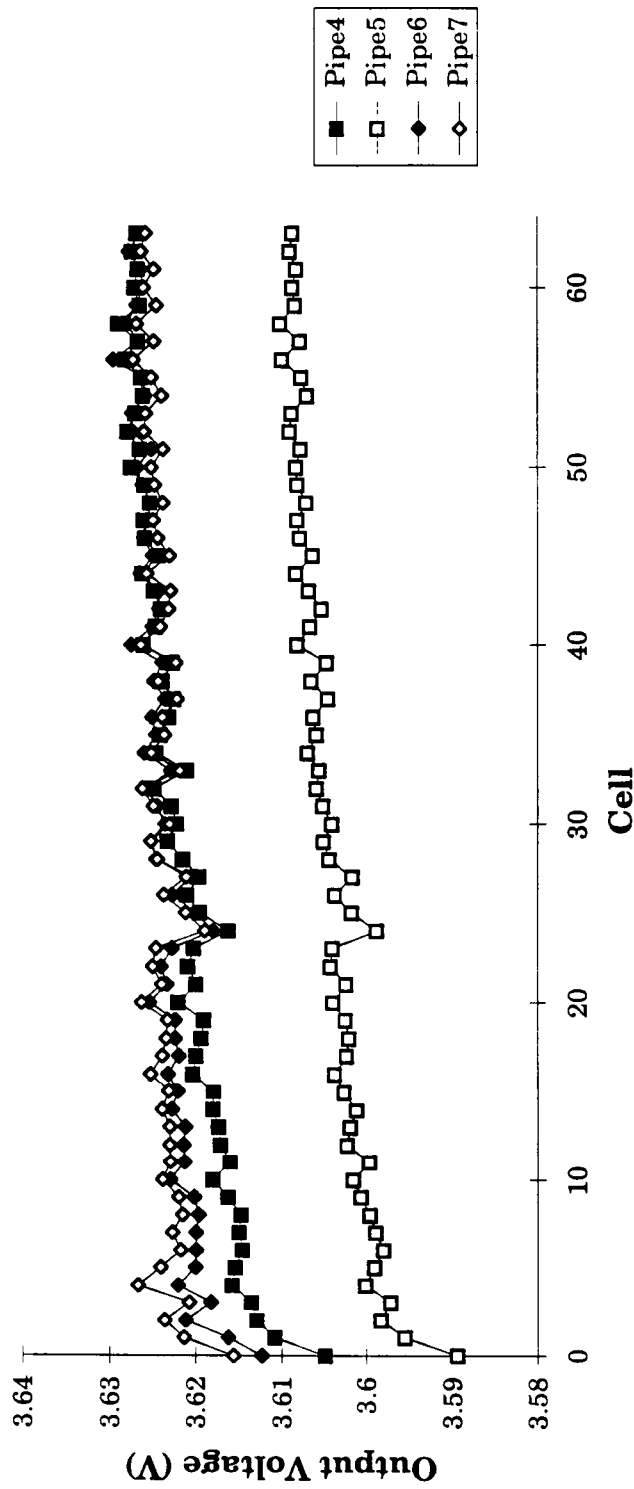


S99, Even, 3.5 Volt Input, Average, 47.5MHz Binary Write.

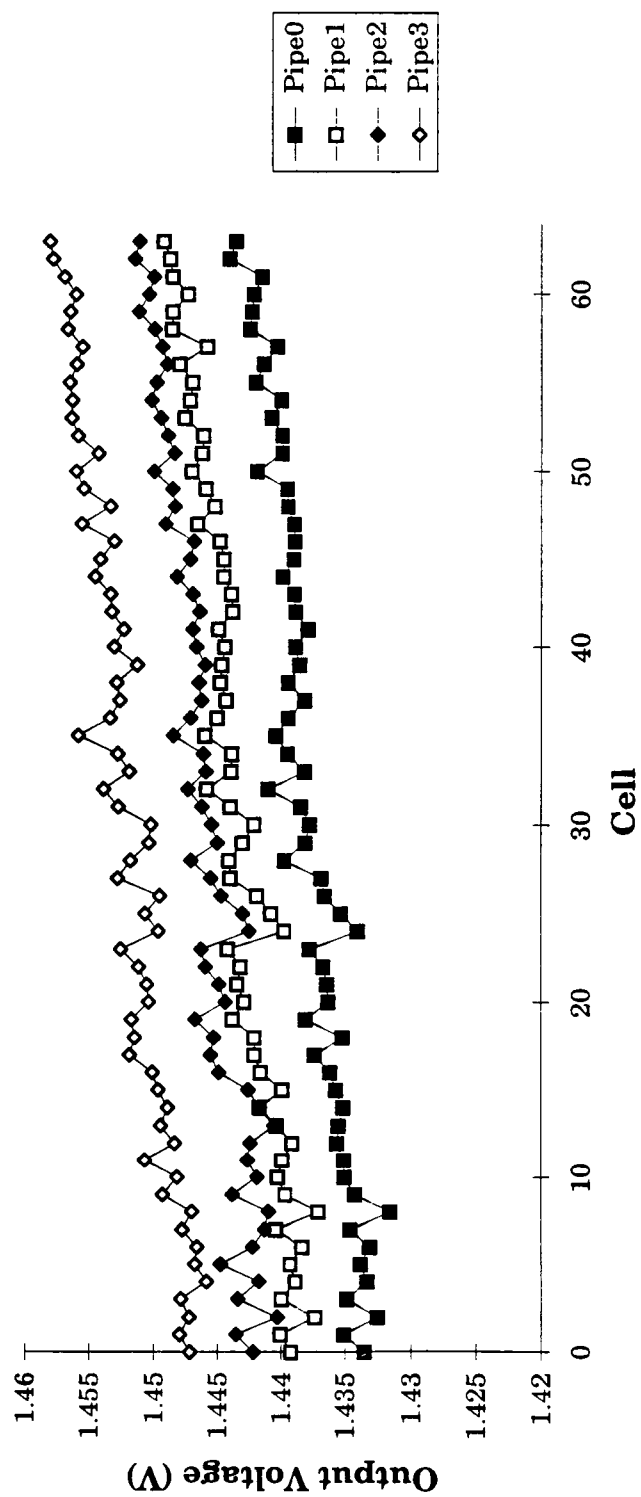


D99, Odd, 1.5 Volt Input, Average, 10MHz Gray Code Write

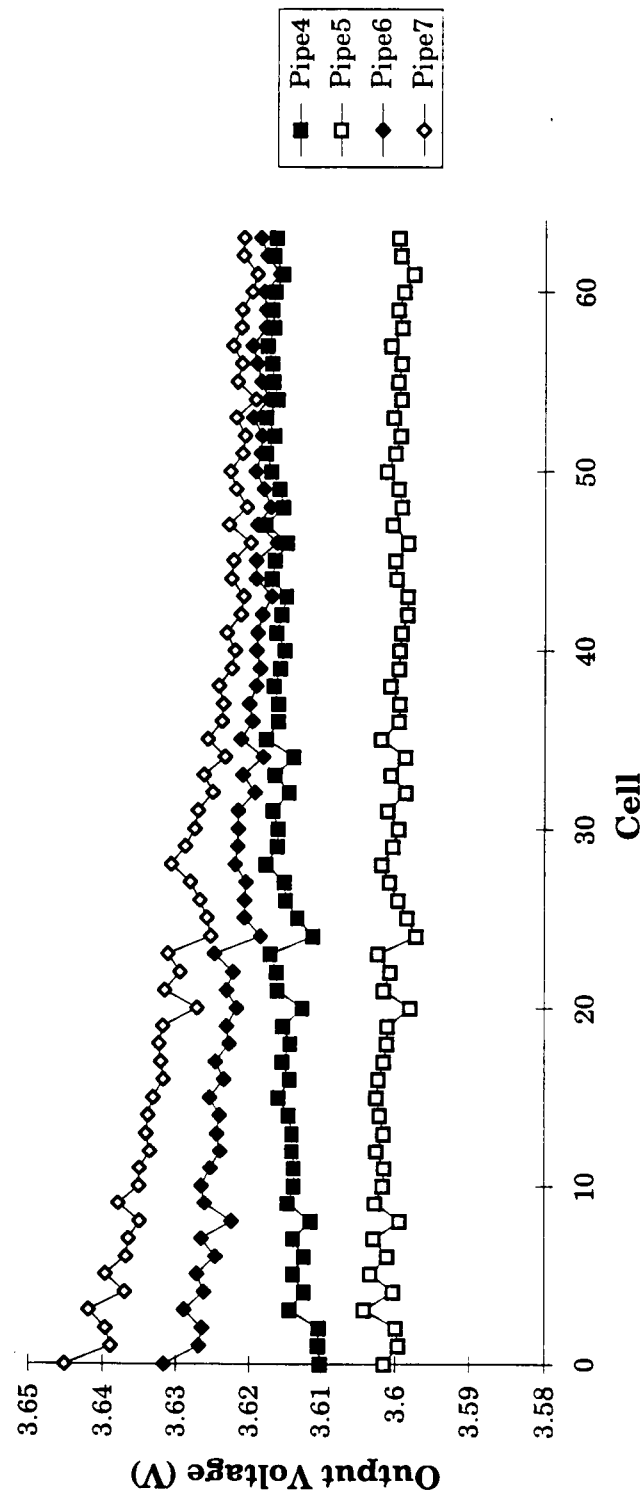
Plate 11. Chip D99, 1.5V input, Gray code.



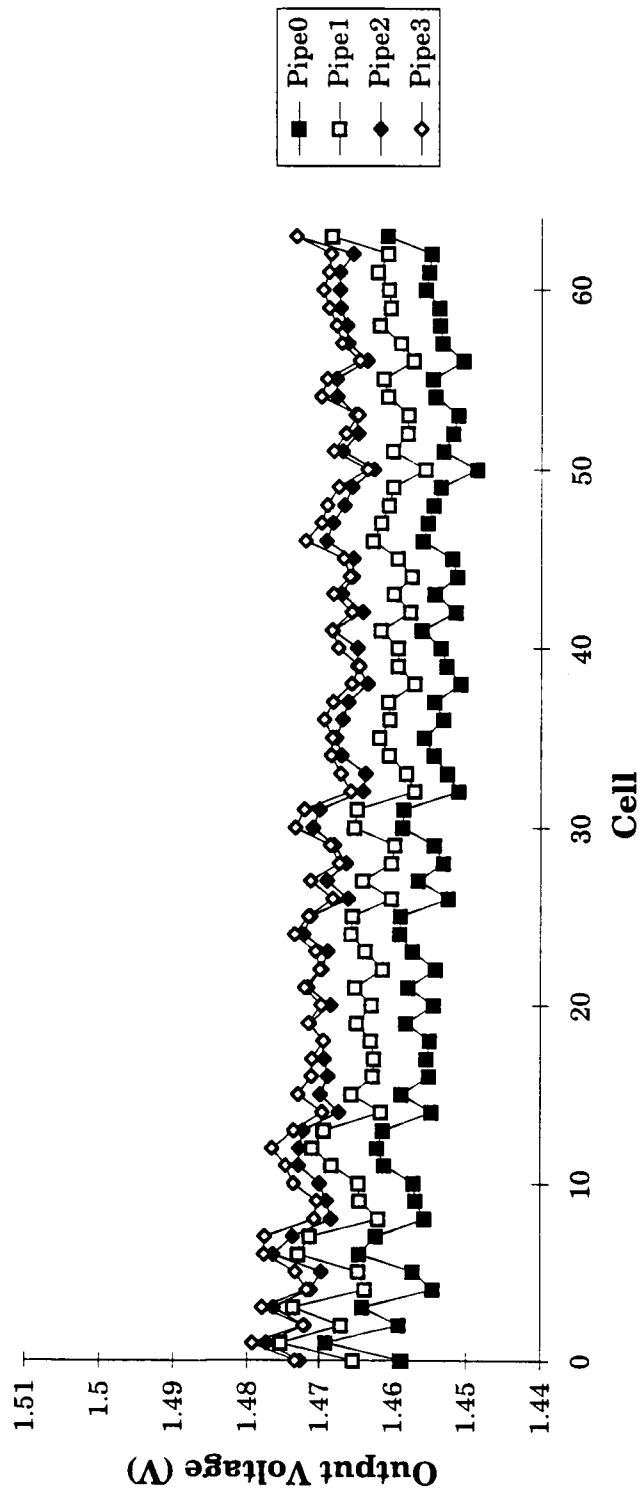
D99, Odd, 1.5 Volt Input, Average, 10MHz Gray Code Write.



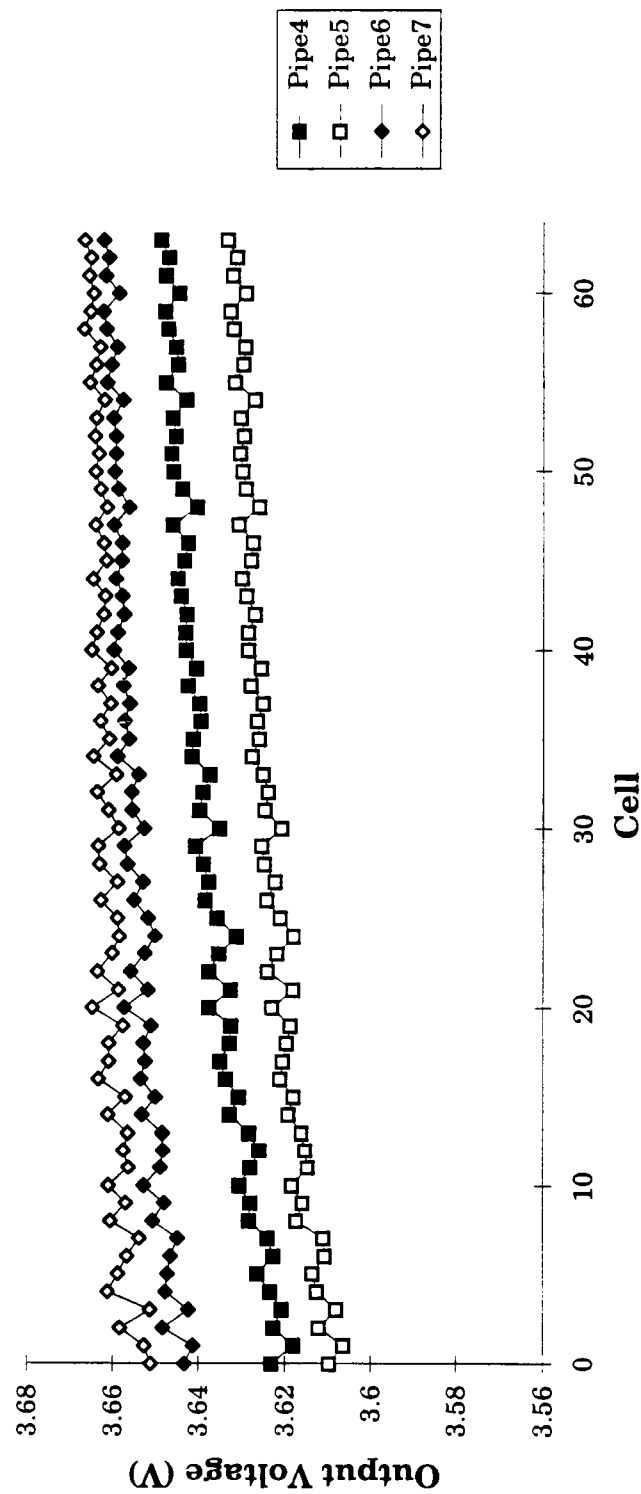
D99, Even, 1.5 Volt Input, Average, 10MHz Gray Code Write.



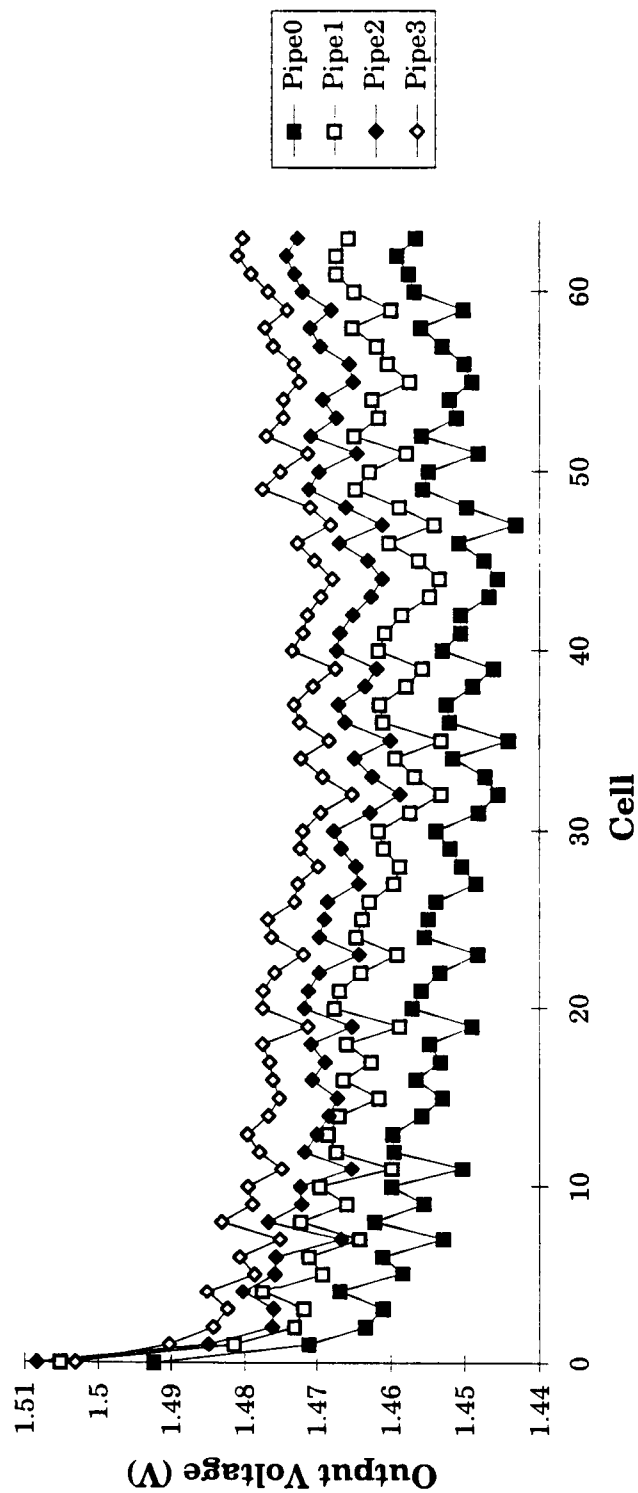
D99, Even, 1.5 Volt Input, Average, 10MHz Gray Code Write.



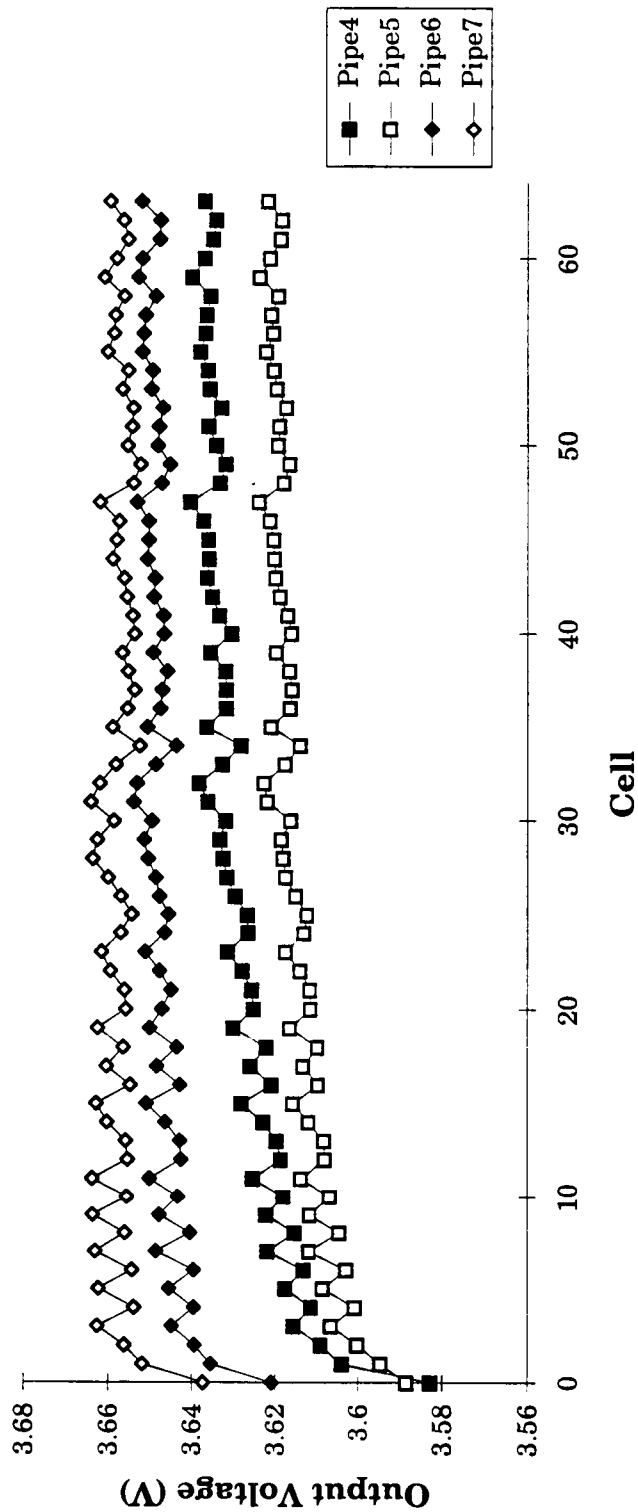
D99, Odd, 1.5 Volt Input, Average, 47.5MHz Gray Code Write.



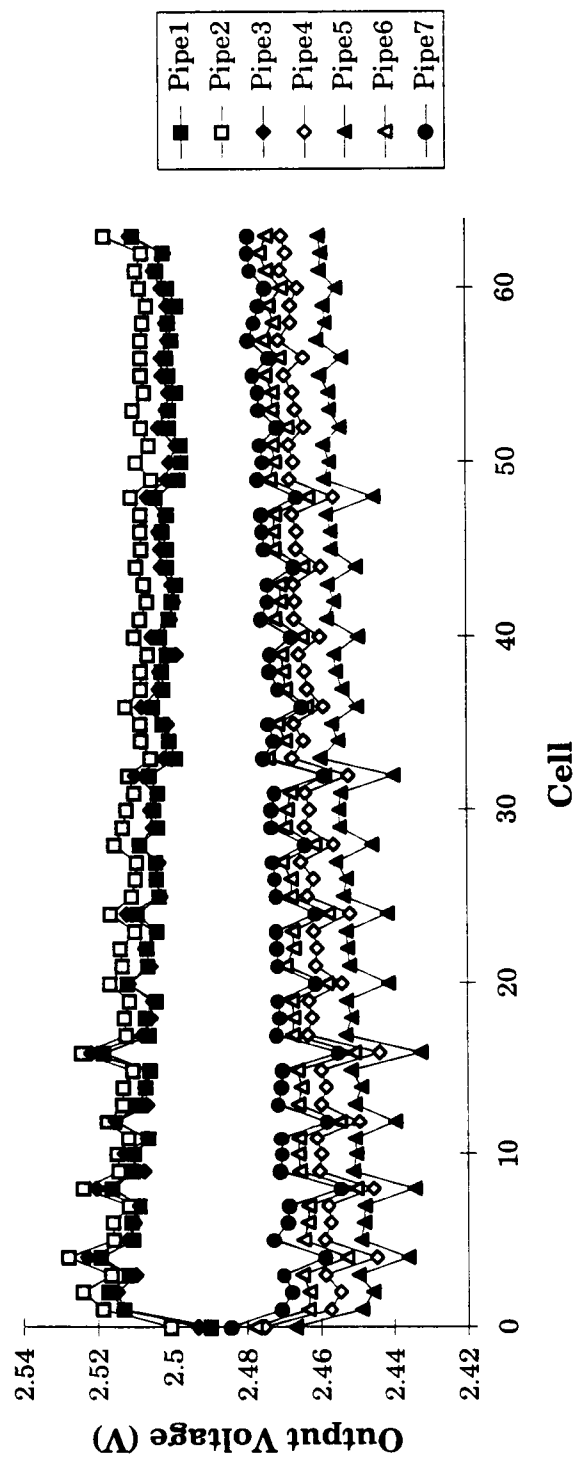
D99, Odd, 1.5 Volt Input, Average, 47.5MHz Gray Code Write.



D99, Even, 1.5 Volt Input, Average, 47.5MHz Gray Code Write.

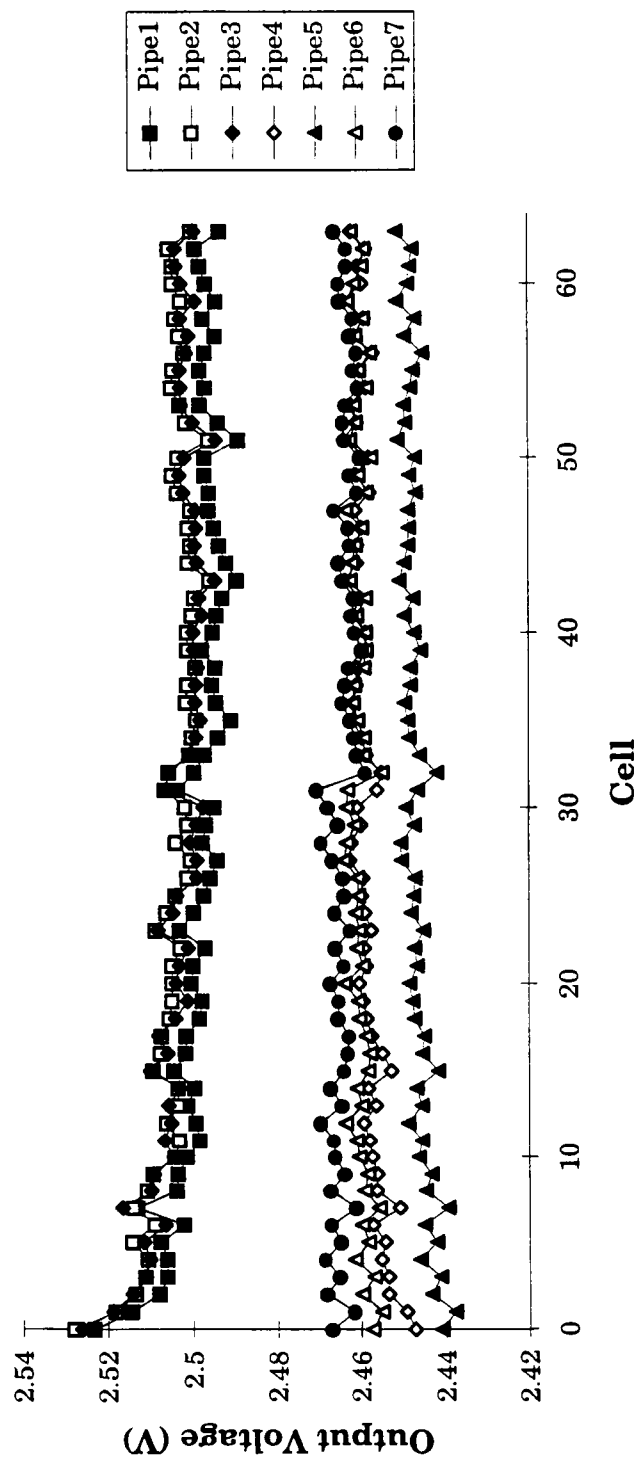


D99, Even, 1.5 Volt Input, Average, 50MHz Gray Code Write.

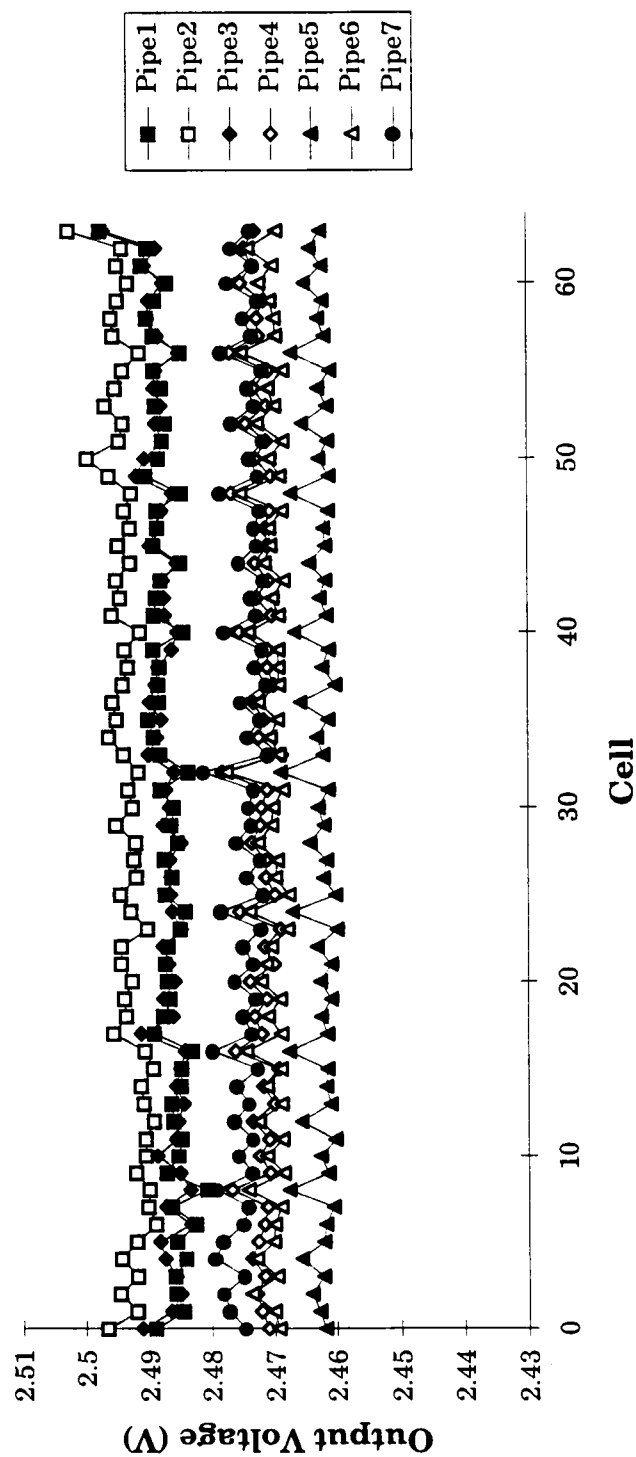


5MRad, D99, Odd, 2.5 Volt Input, Average,
47.5MHz Binary Write.

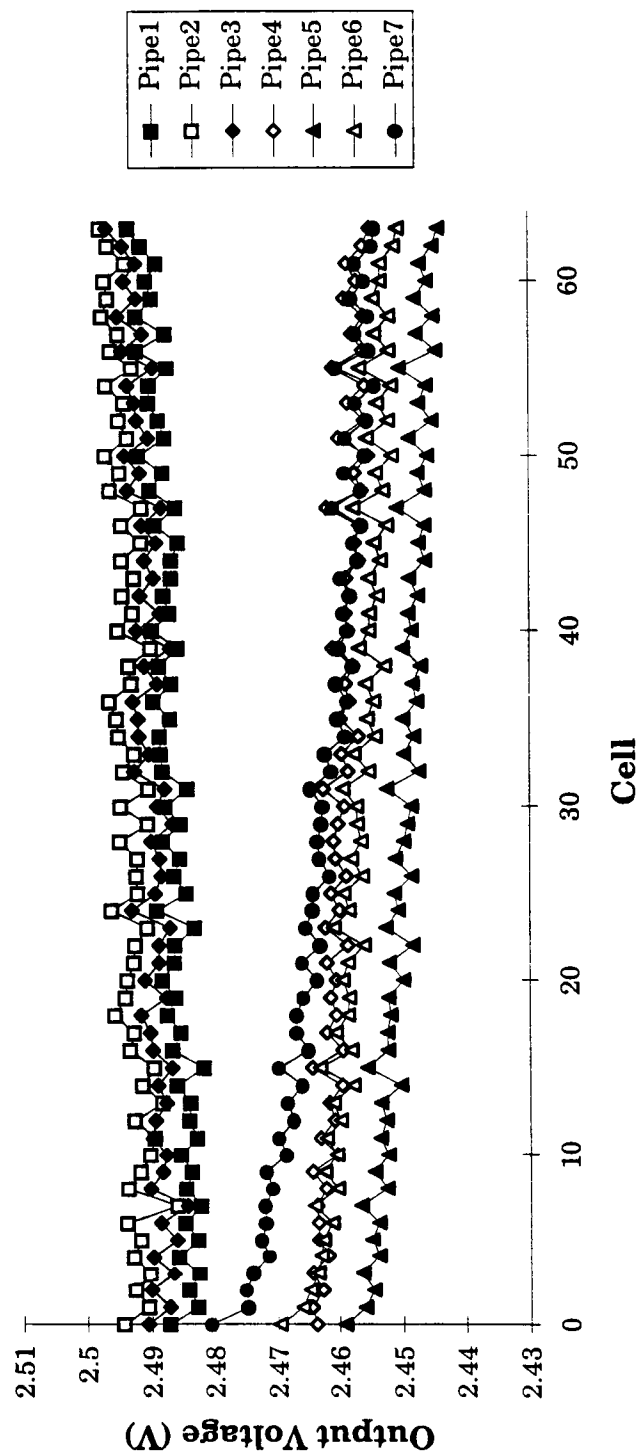
Plate 12. Chip D99, 2.5V input, 5MRad.



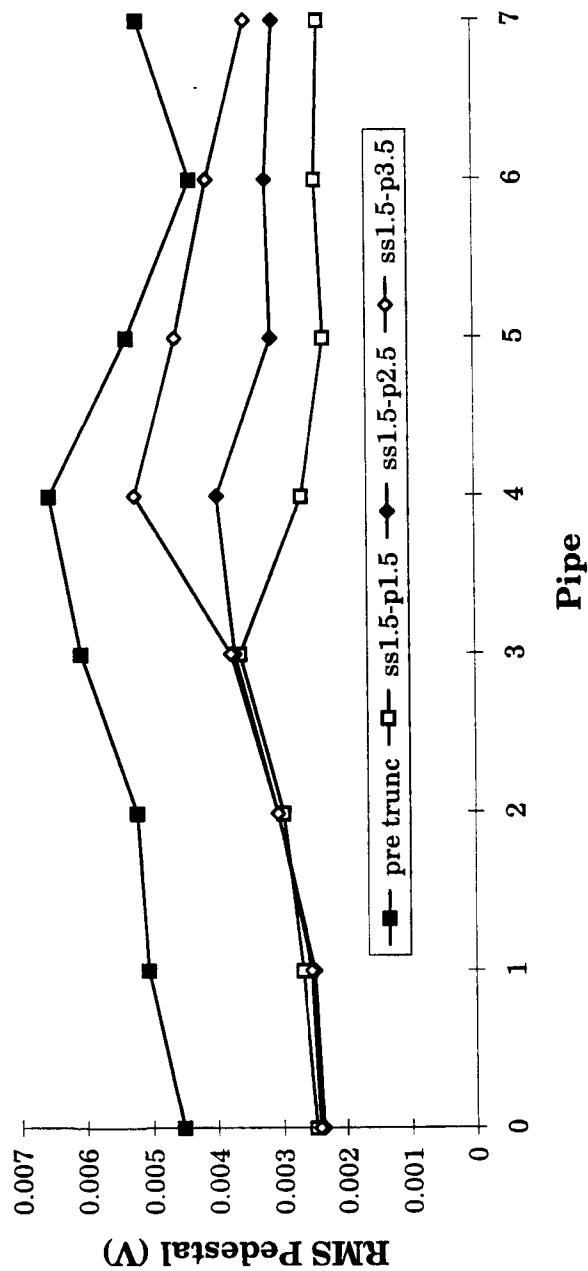
5MRad, D99, Even, 2.5 Volt Input, Average,
47.5MHz Binary Write.



**5MRad, D99, Odd, 2.5 Volt Input, Average,
10MHz Binary Write.**

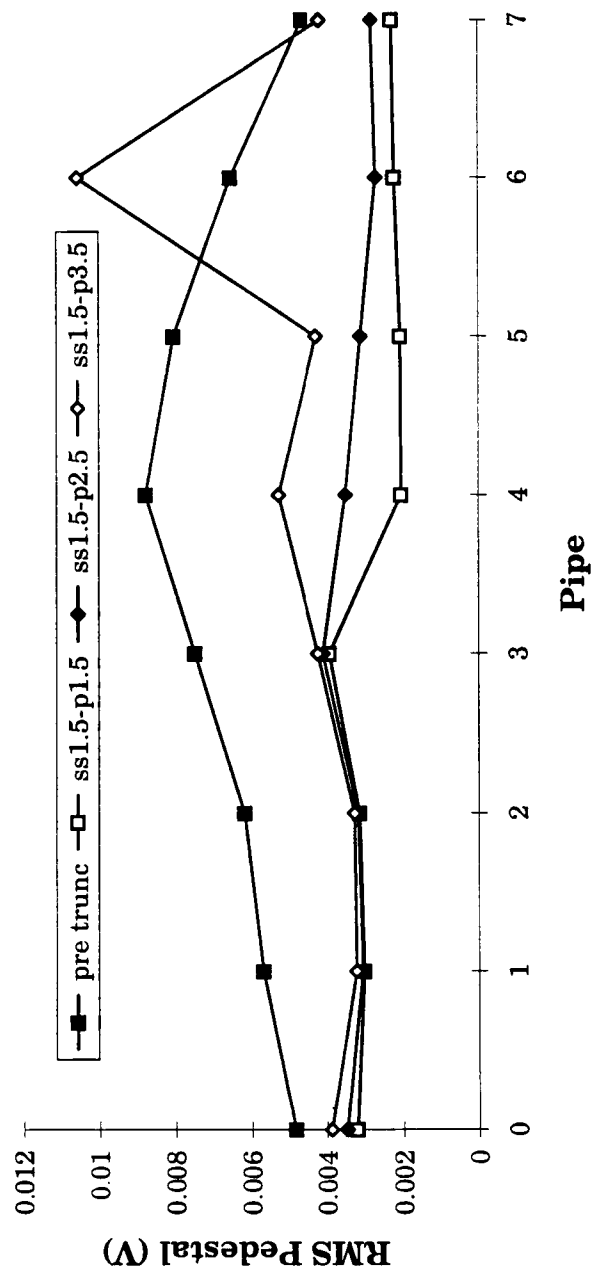


5MRad, D99, Even, 2.5 Volt Input, Average,
10MHz Binary Write.

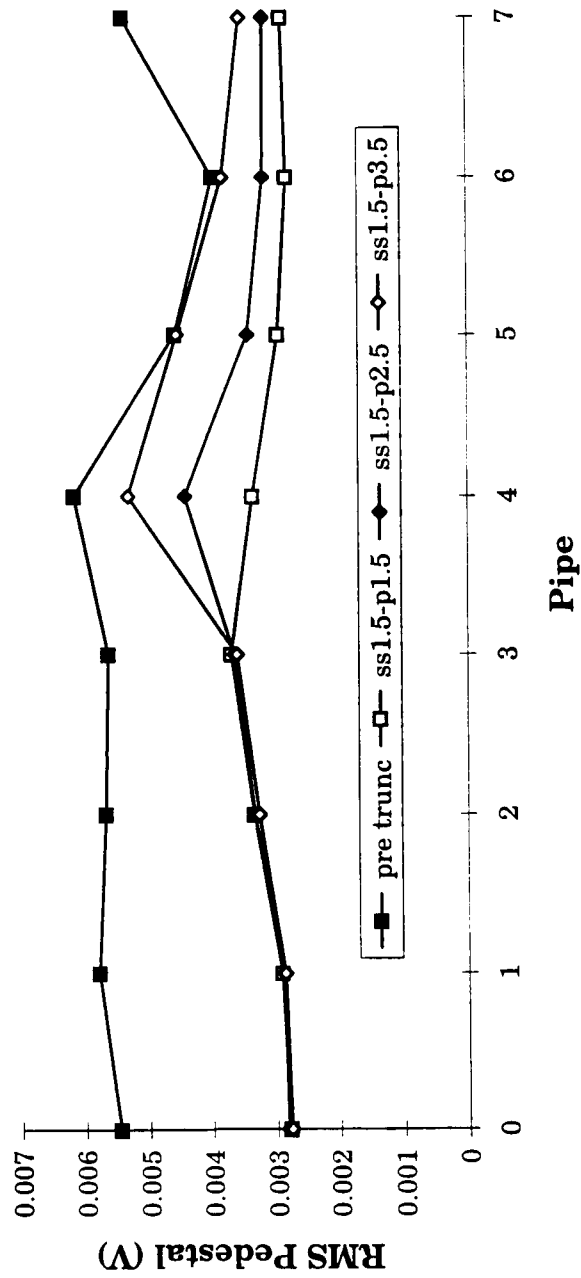


D4A, Even, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.

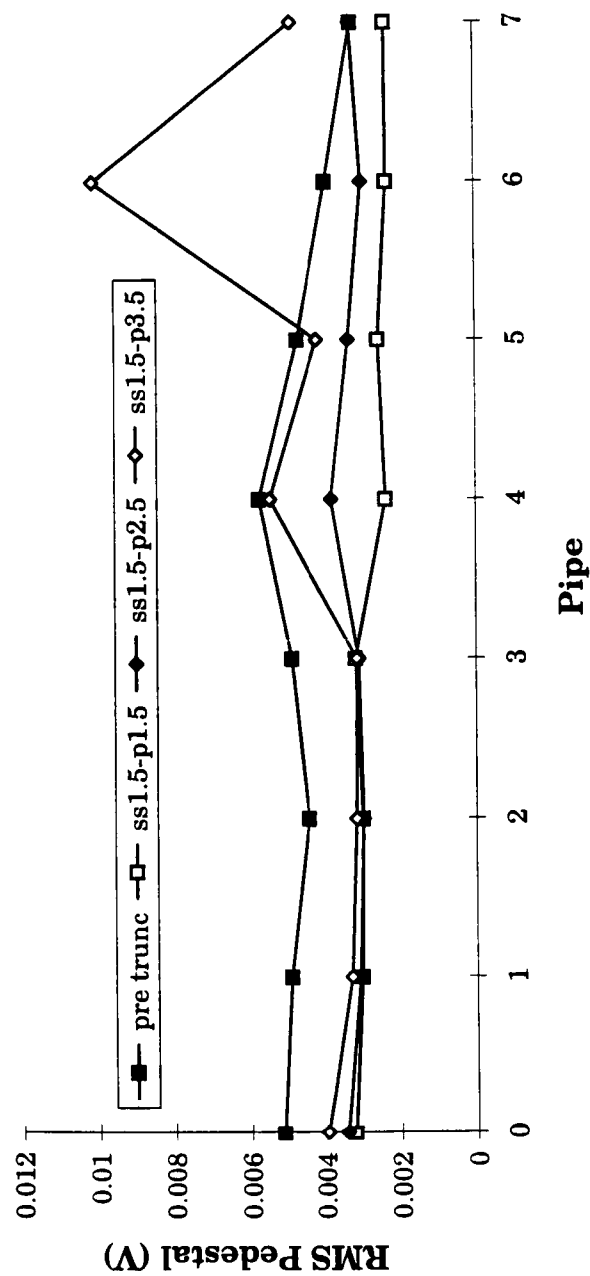
Plate 13. Pedestal subtraction results.



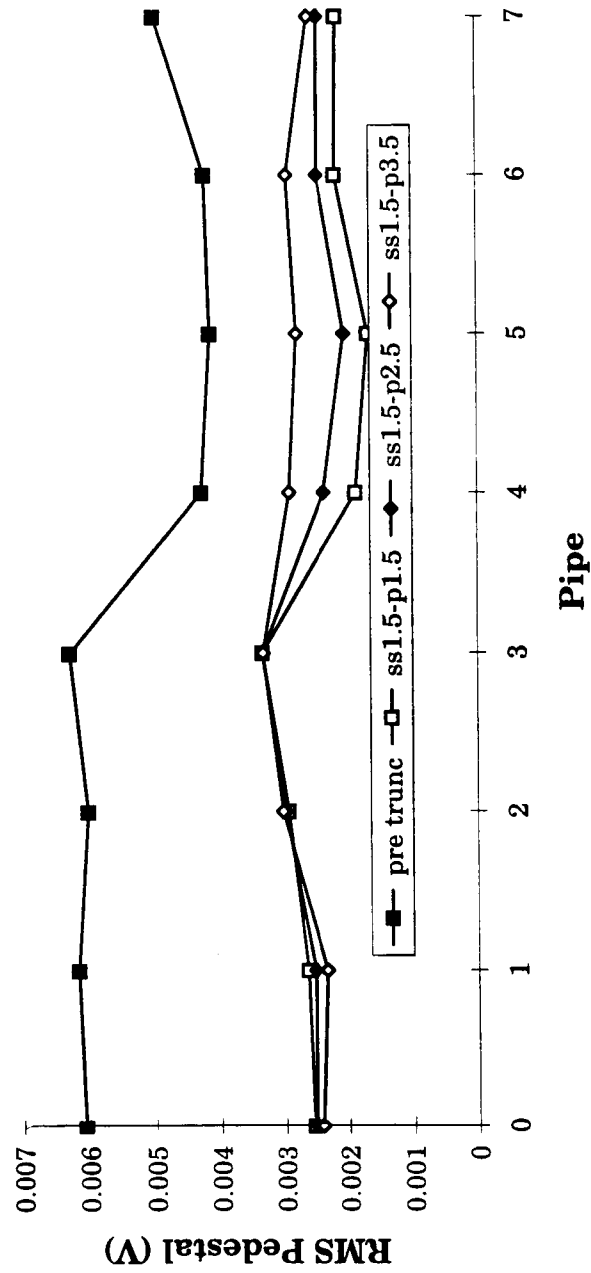
D4A, Odd, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.



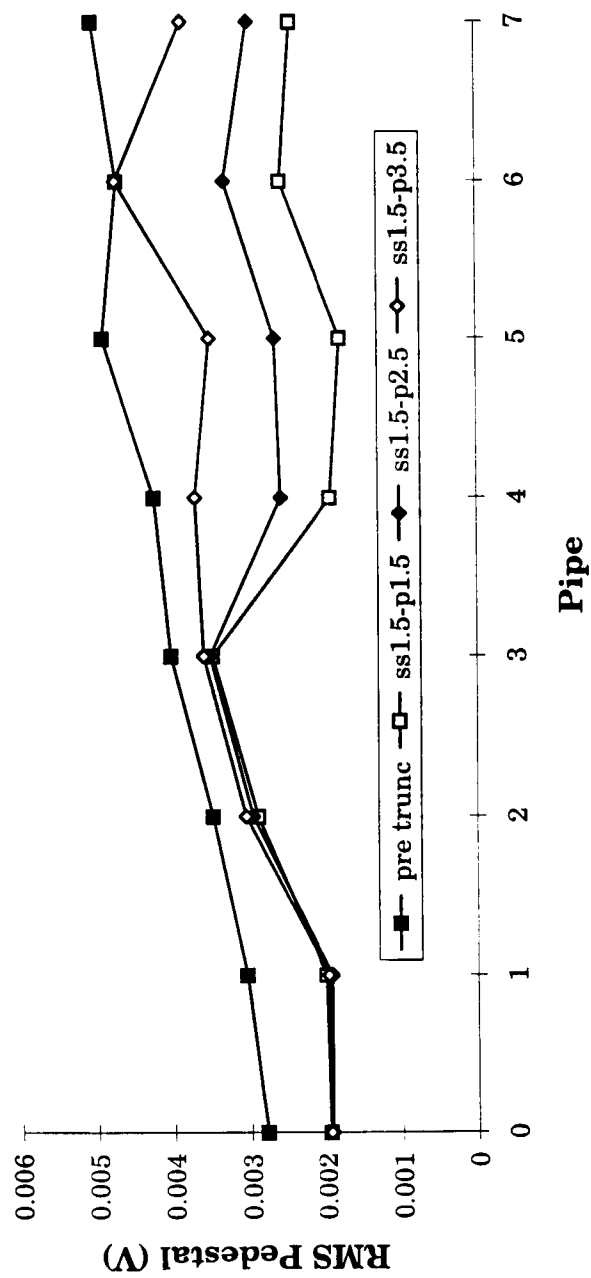
D4A, Even, 1.5 Volt Input, Single Shot, 50MHz Gray Code Write.



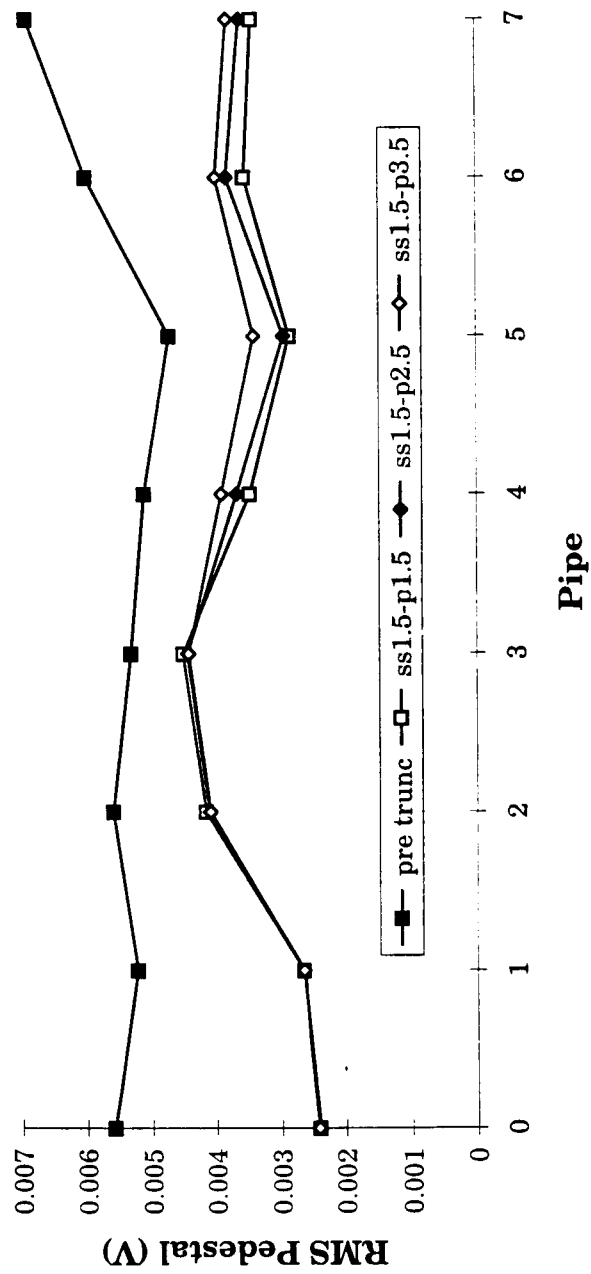
D4A, Odd, 1.5 Volt Input, Single Shot, 47.5MHz Gray Code Write.



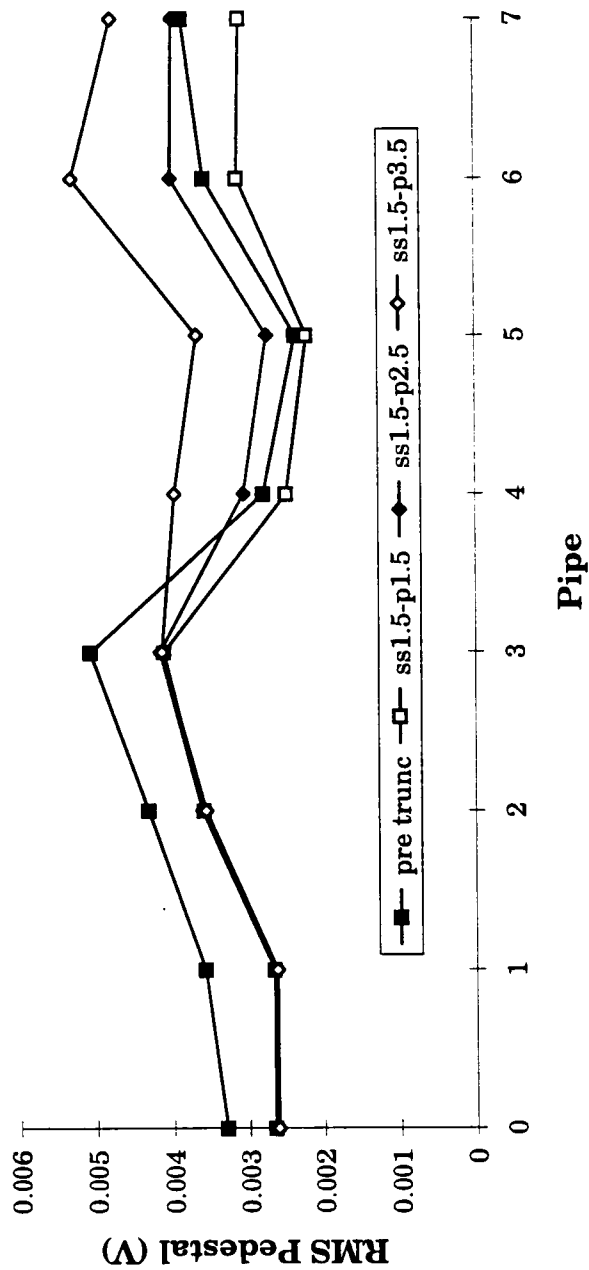
S4A, Even, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.



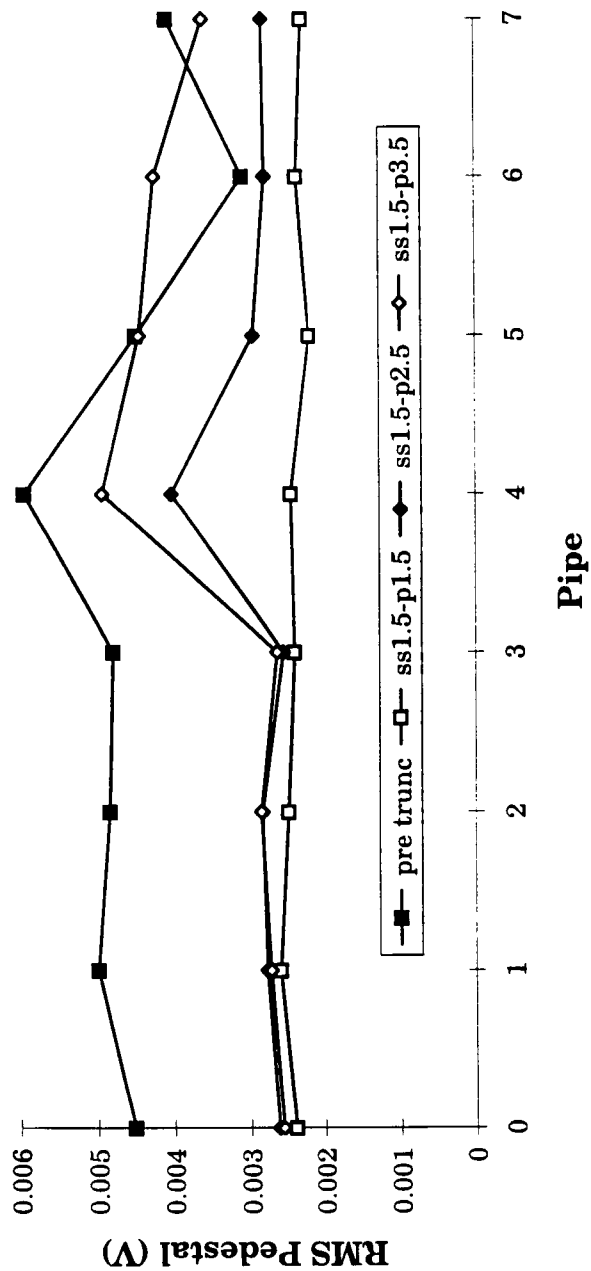
S4A, Odd, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.



**S4A, Even, 1.5 Volt Input, Single Shot, 47.5MHz
Gray Code Write.**

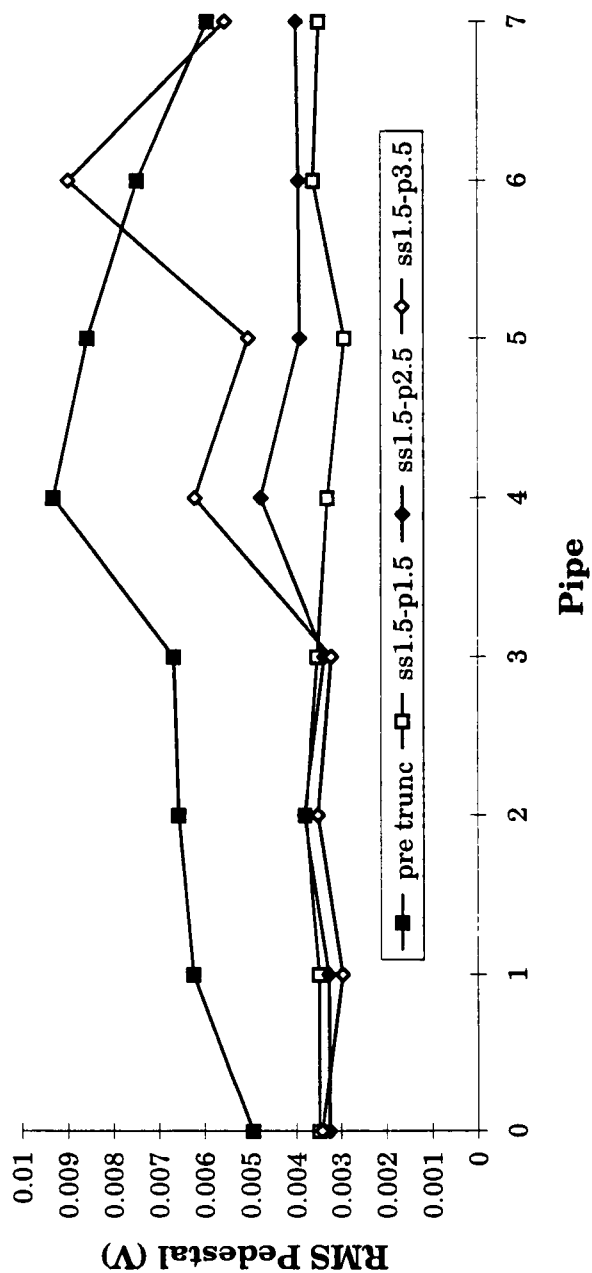


S4A, Odd, 1.5 Volt Input, Single Shot, 47.5MHz
Gray Code Write.



D4A, 5MRad, Even, 1.5 Volt Input, Single Shot, 47.5MHz Binary Write.

Plate 14. 5MRad pedestal subtraction results.



**D4A, 5MRad, Odd, 1.5 Volt Input, Single Shot, 47.5MHz
Binary Write.**

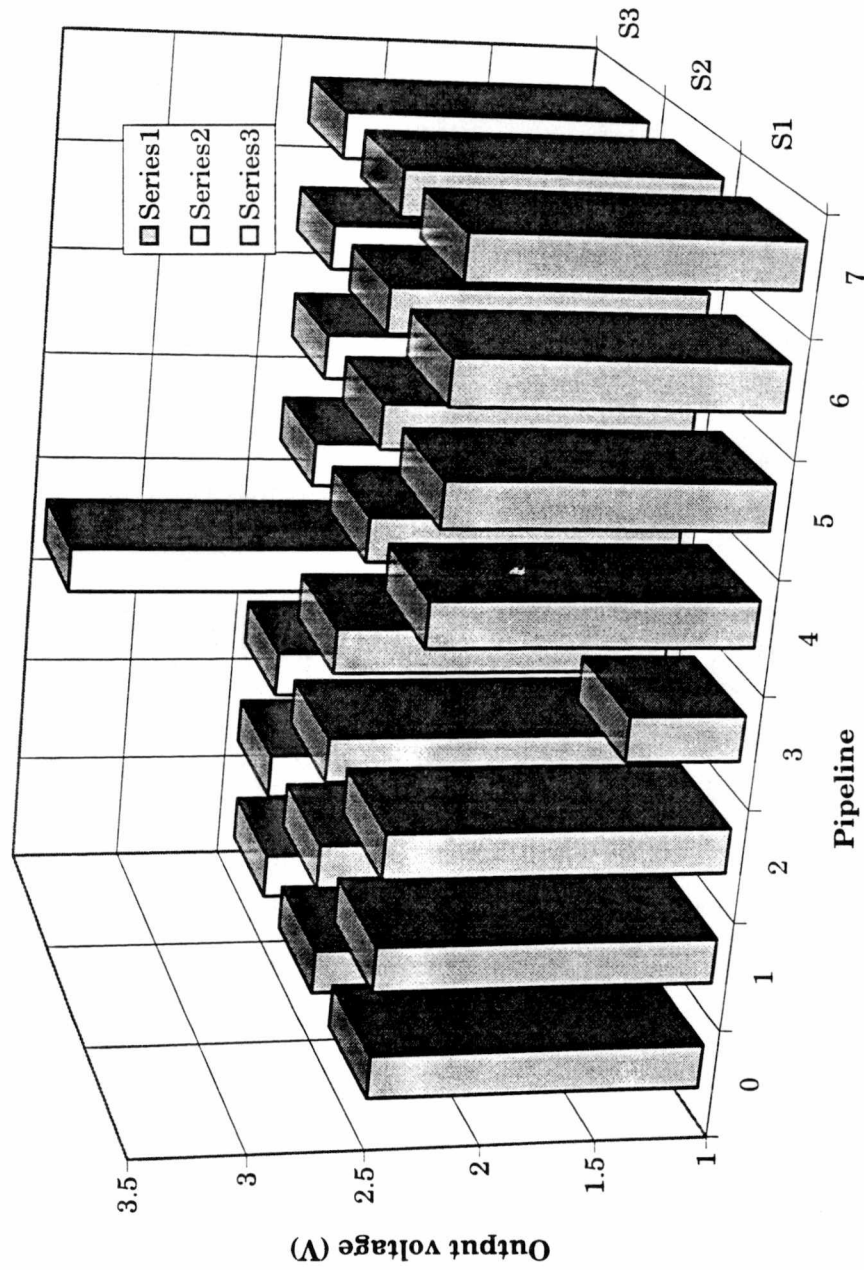
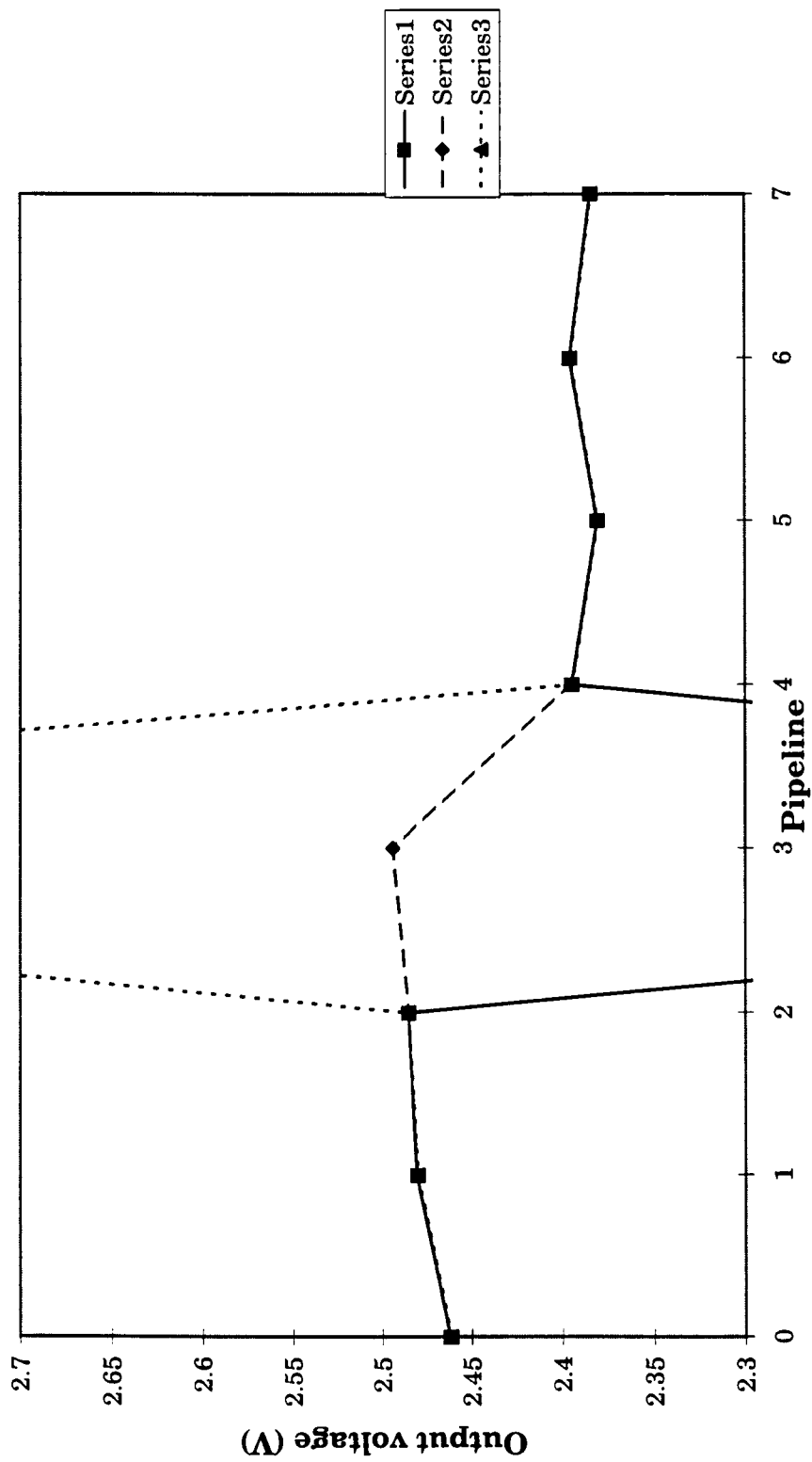
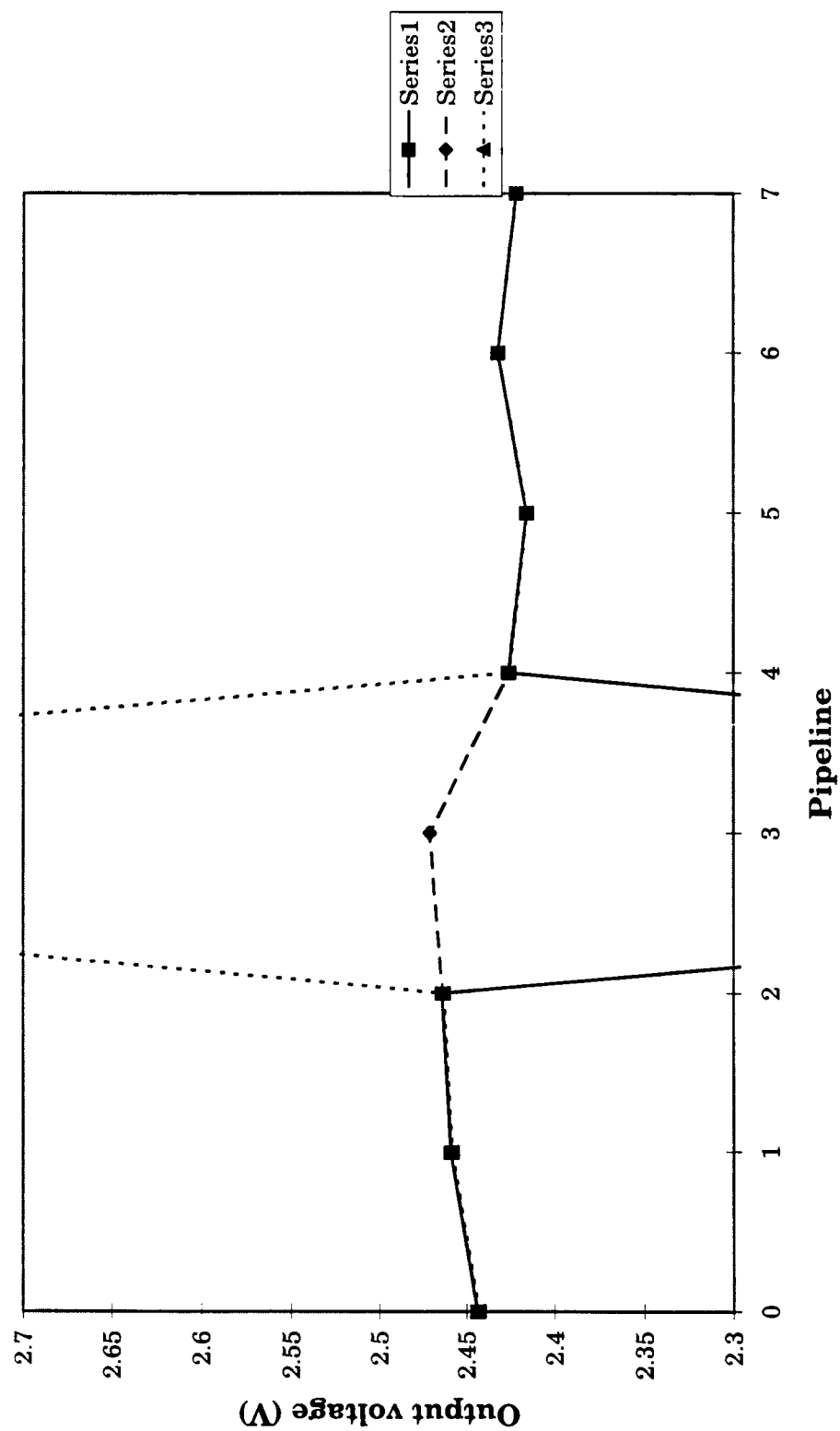


**Plate 15. Chip D99 prerad, even, pipe 3 variation
(3-dimensional).**

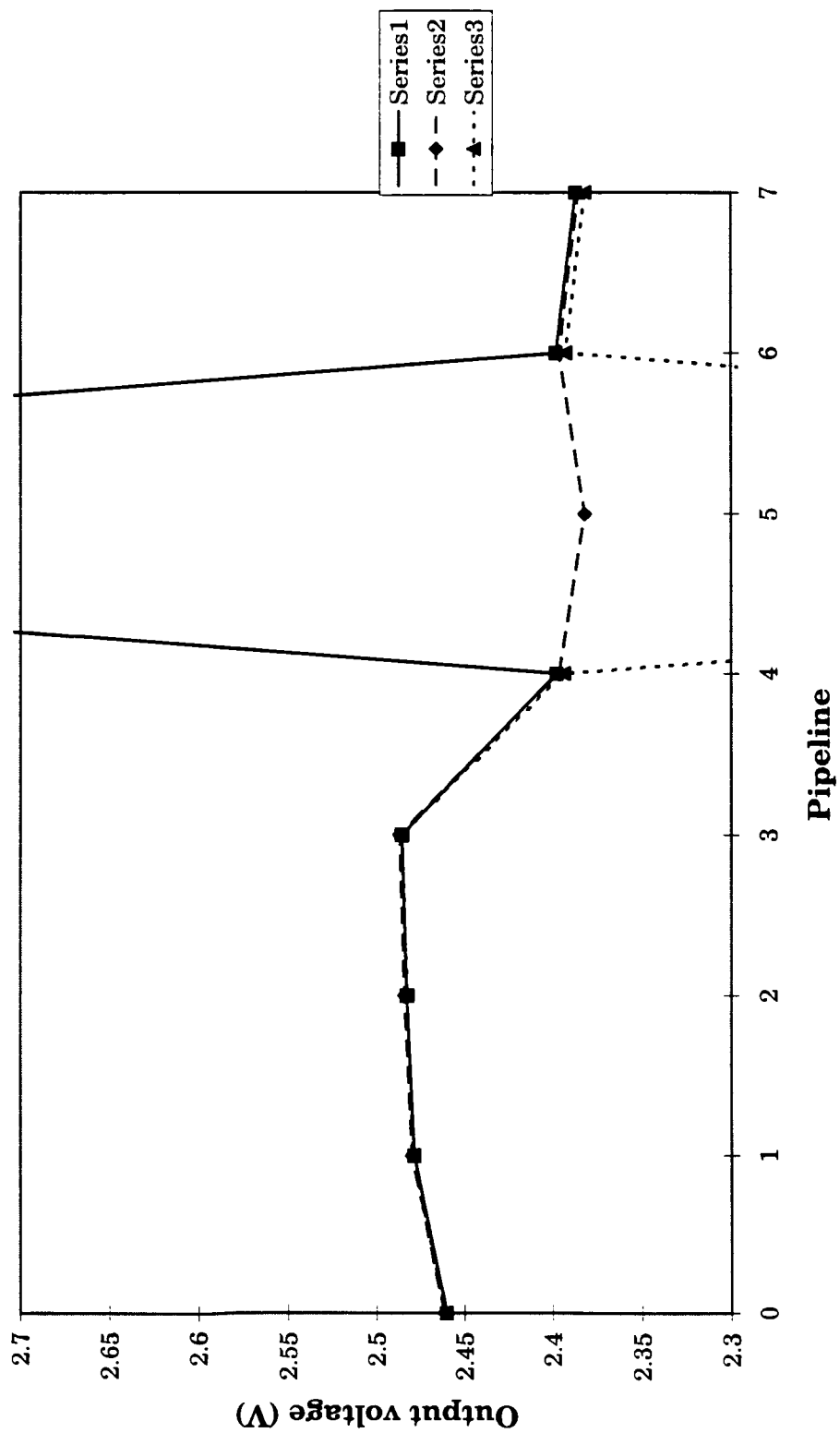


Even, pipe 3 variation.

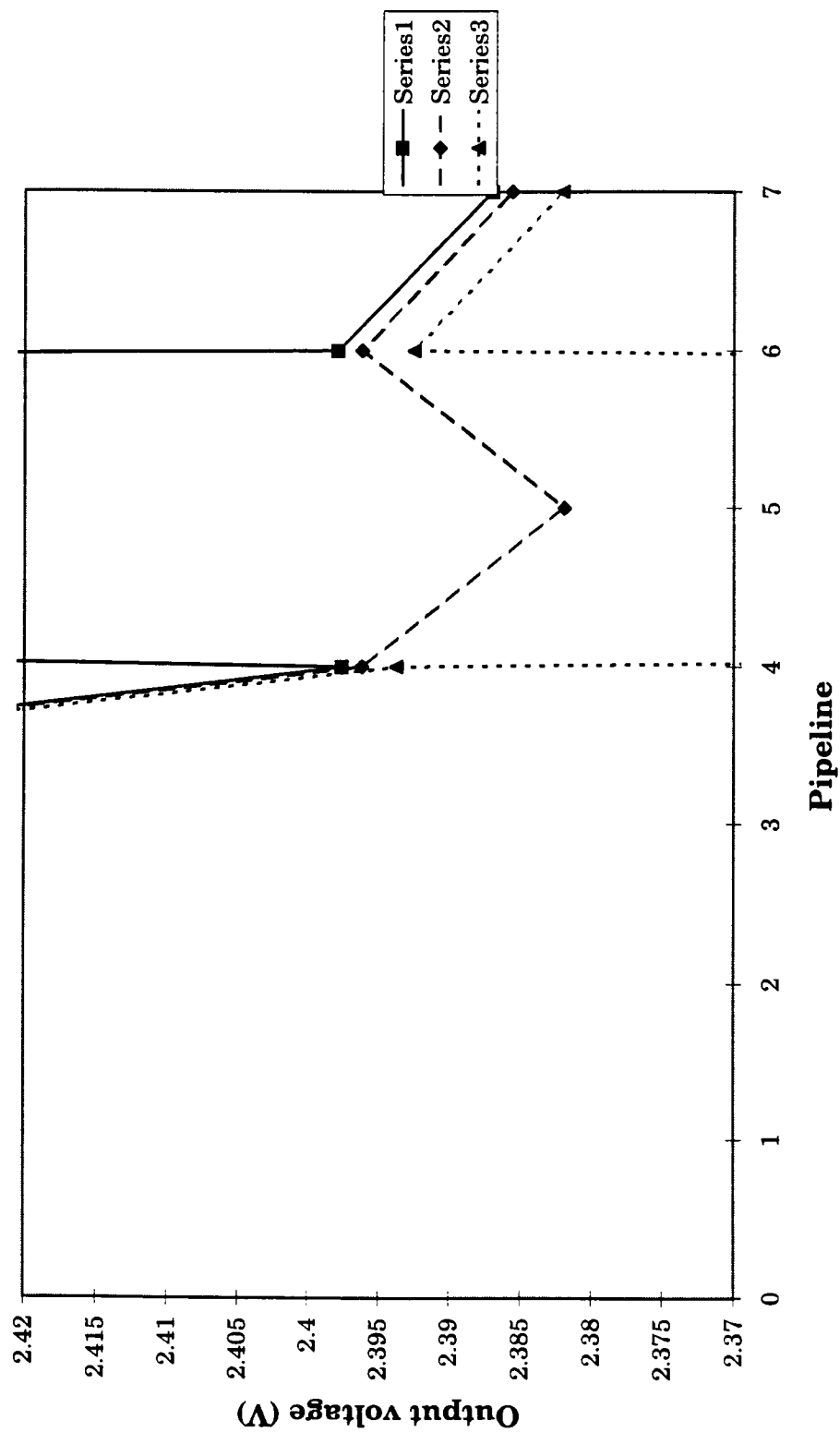
Plate 16. Chip D99, prerad.



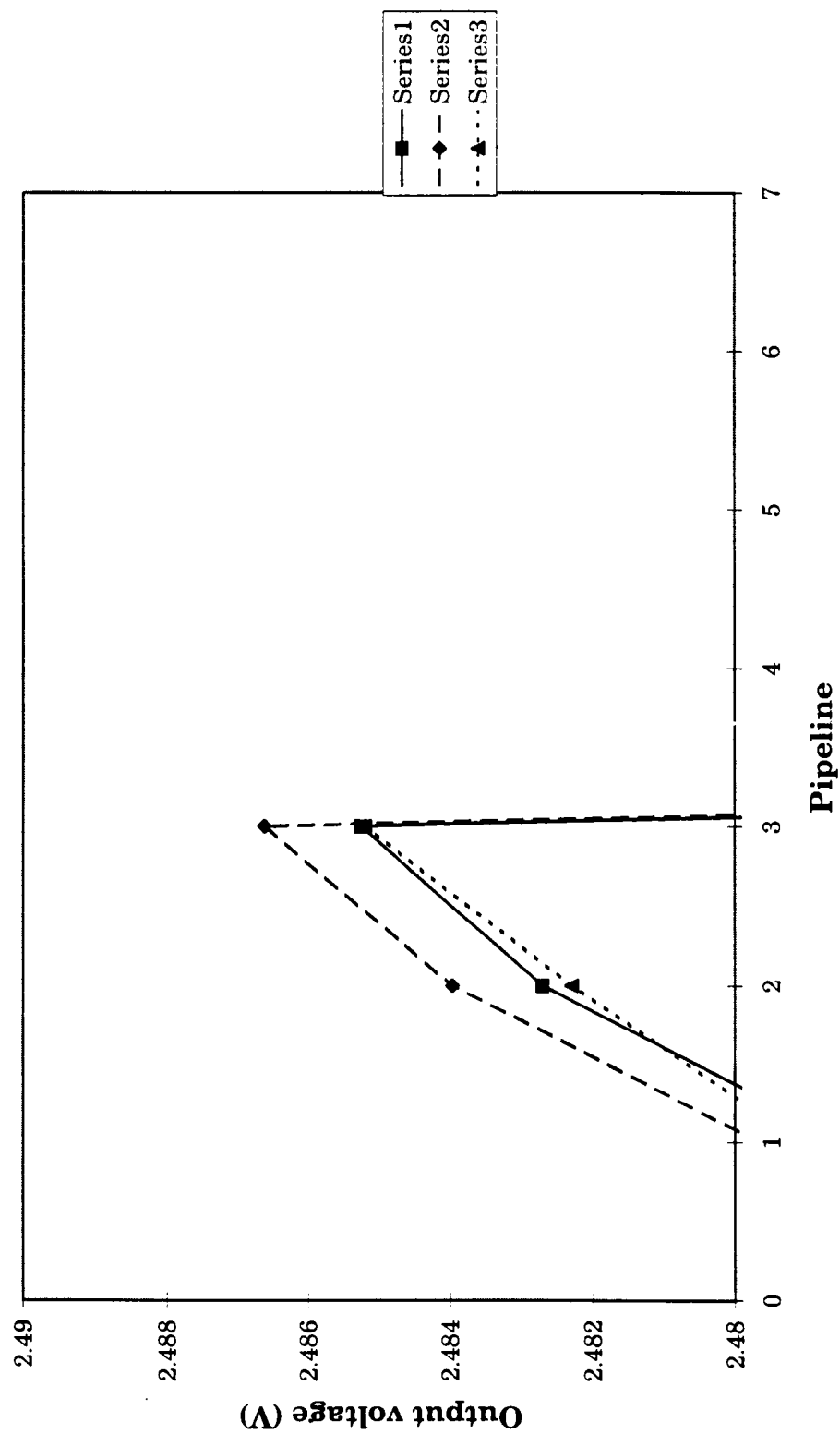
D99 prerad, odd, pipe 3 variation.



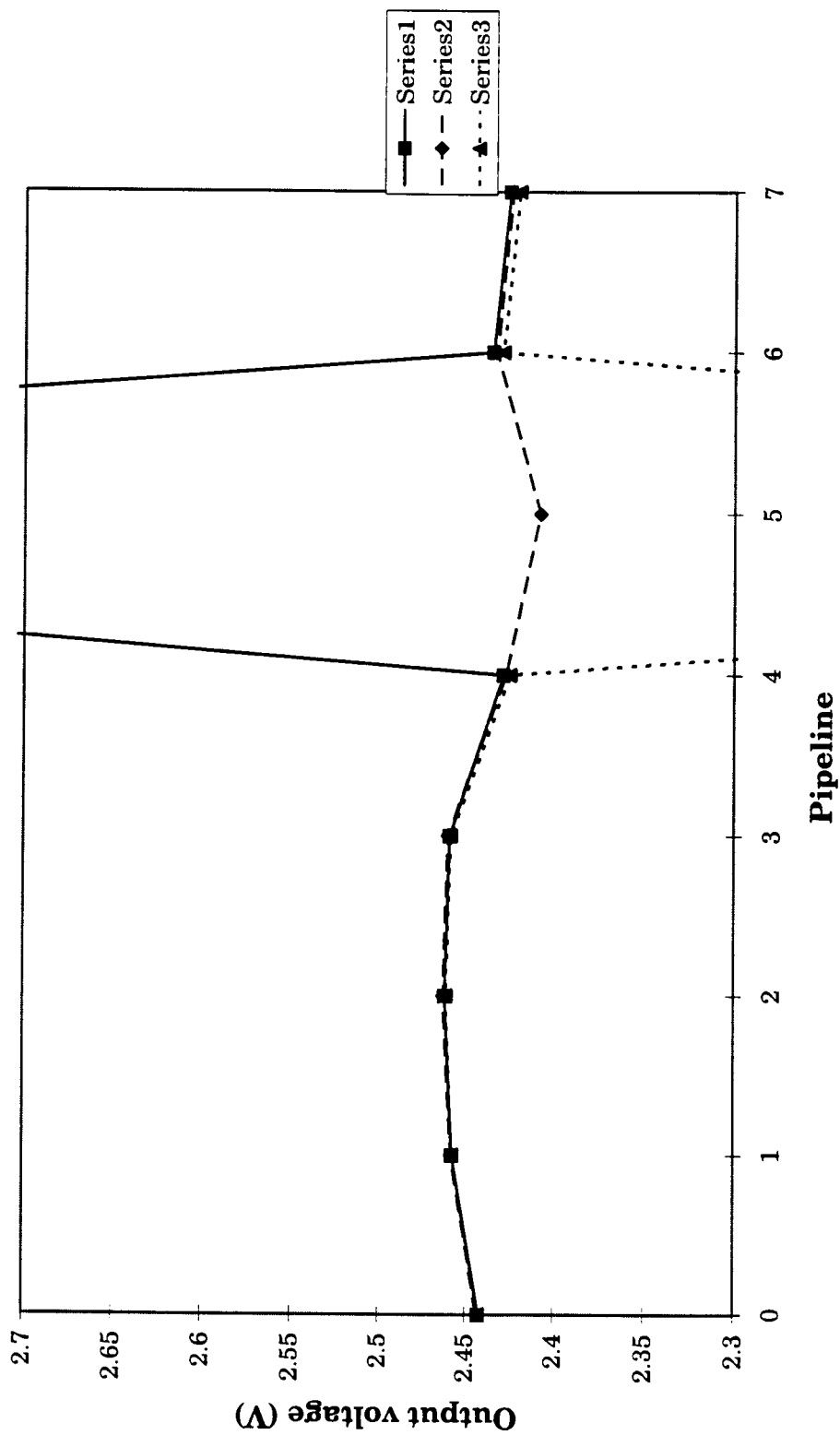
D99 prerad, even, pipe 5 variation.



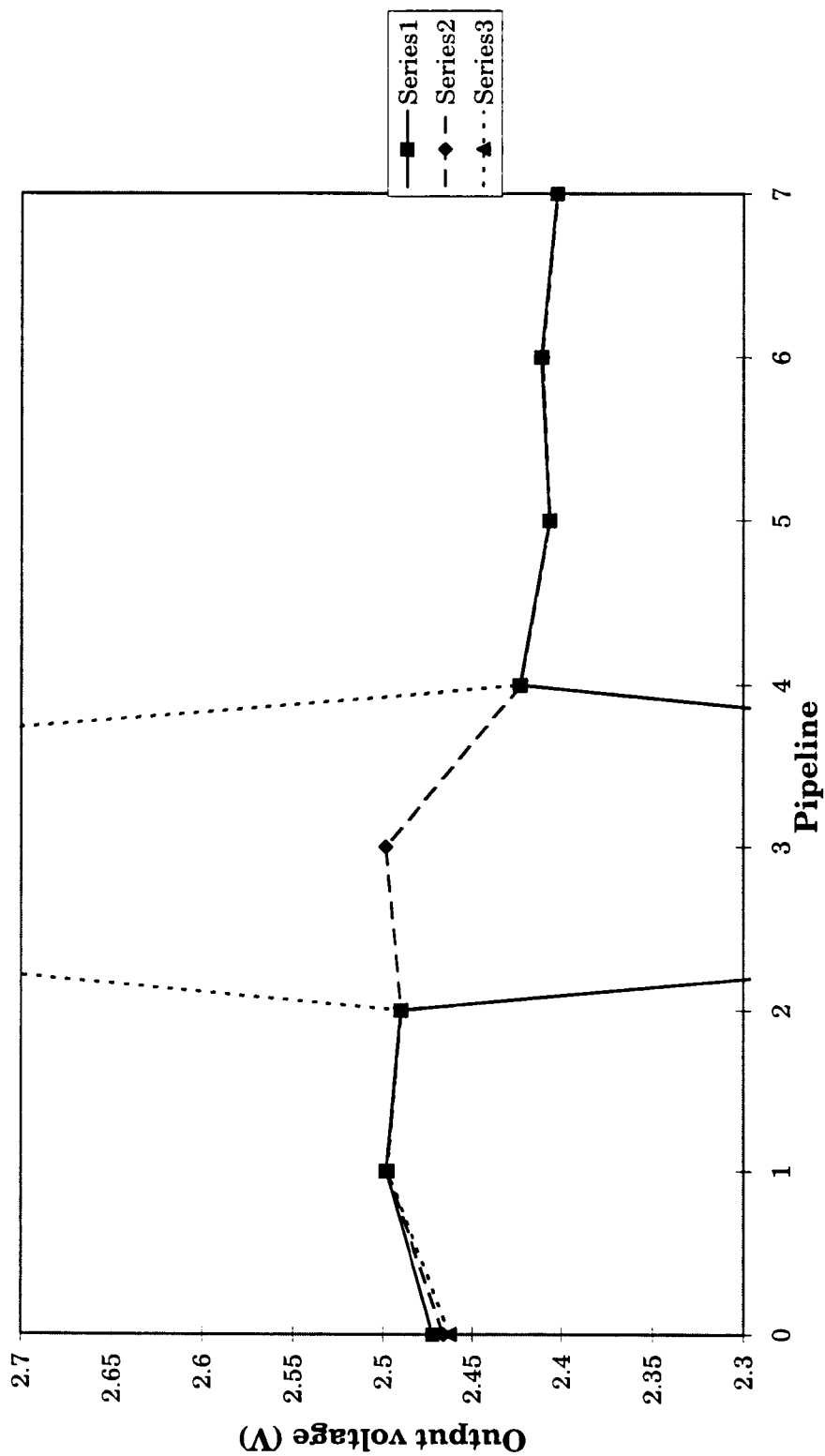
D99 prerad, even, pipe 5 variation.



D99 prerad, even, pipe 5 variation.

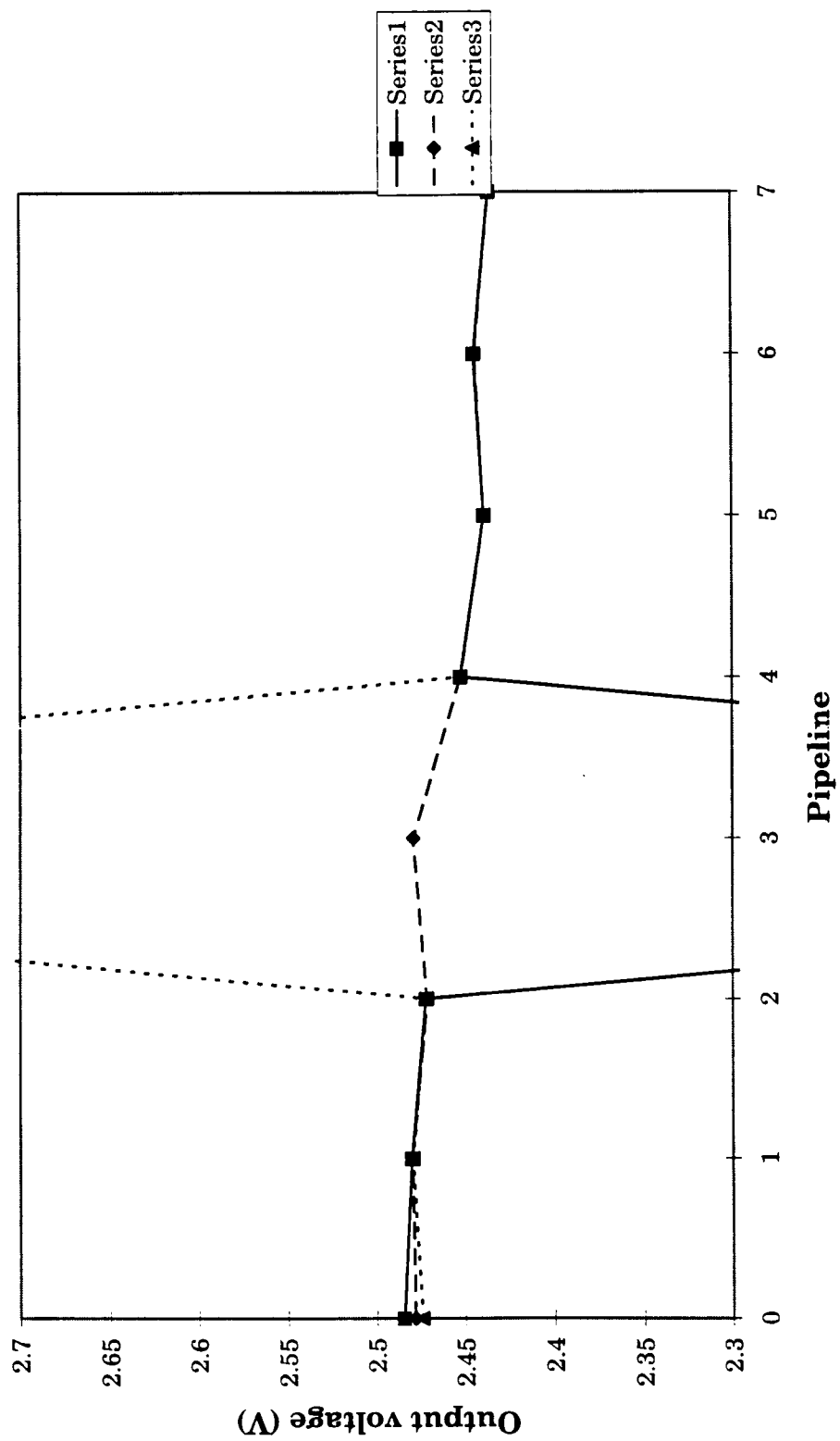


D99 prerad, odd, pipe 5 variation.

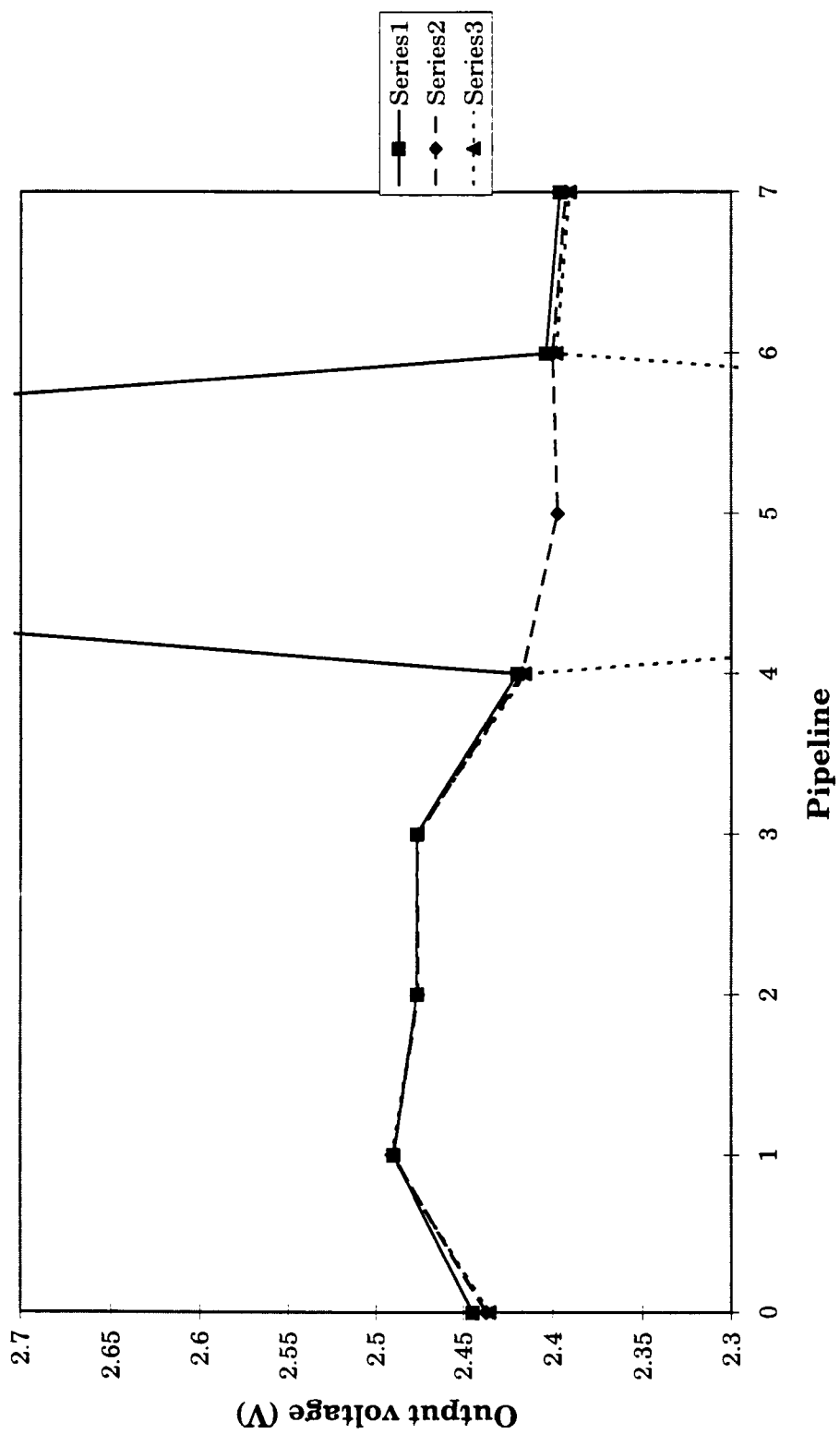


5MRad, even, pipe 3 variation.

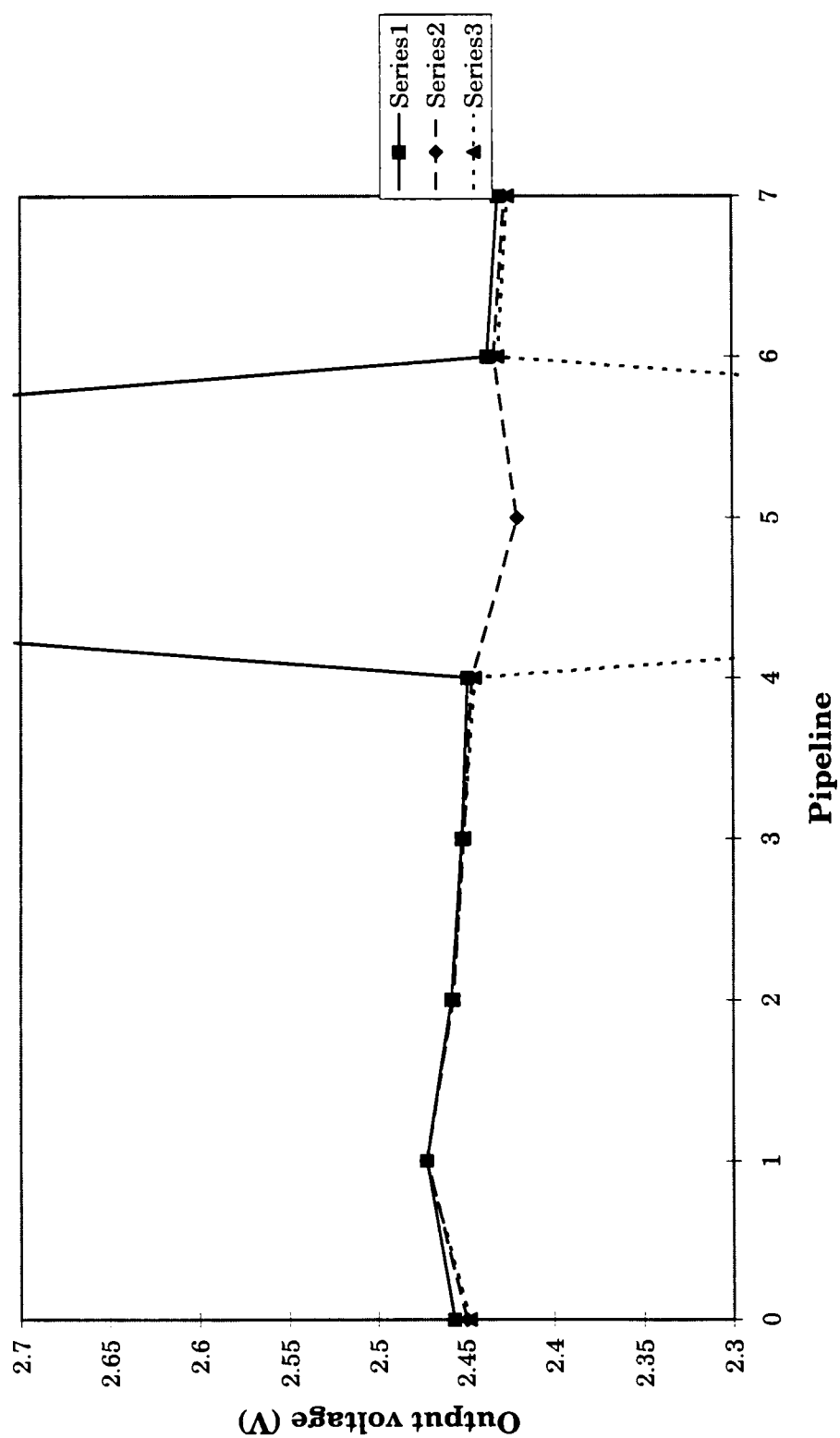
Plate 17. Chip D99, 5MRad.



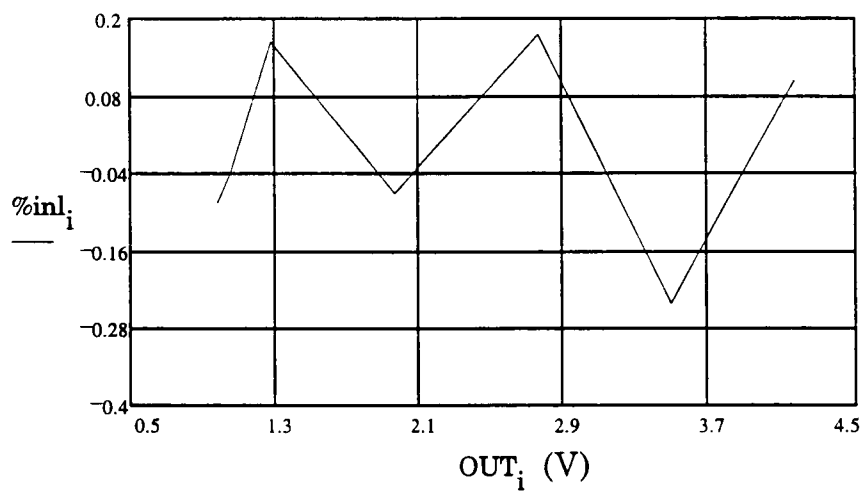
D99 5MRad, odd, pipe 3 variation.



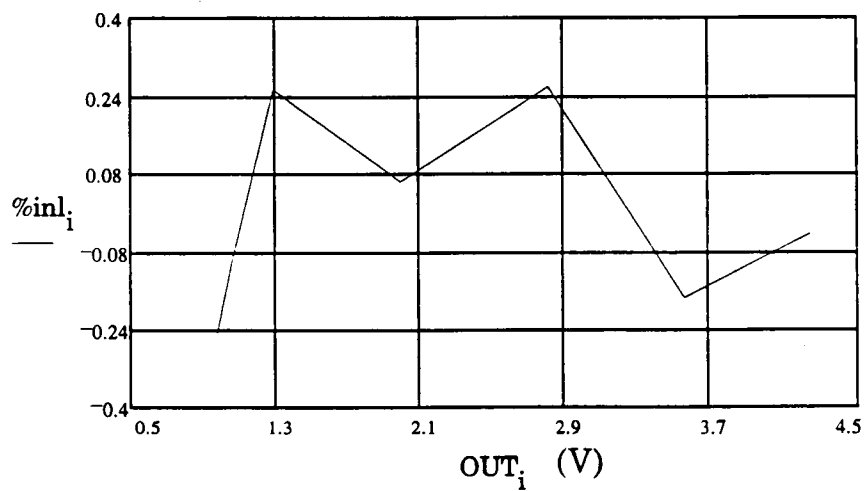
D99 5MRad, even, pipe 5 variation.



D99 5MRad, odd, pipe 5 variation.

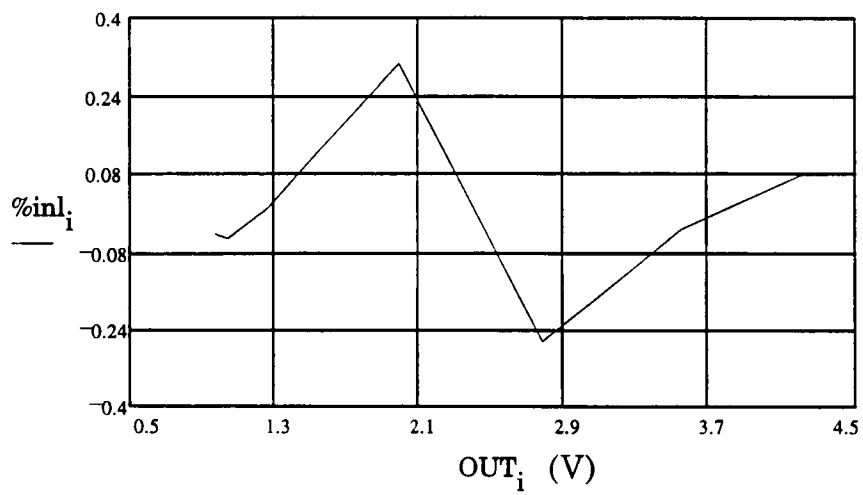


Pipe 0

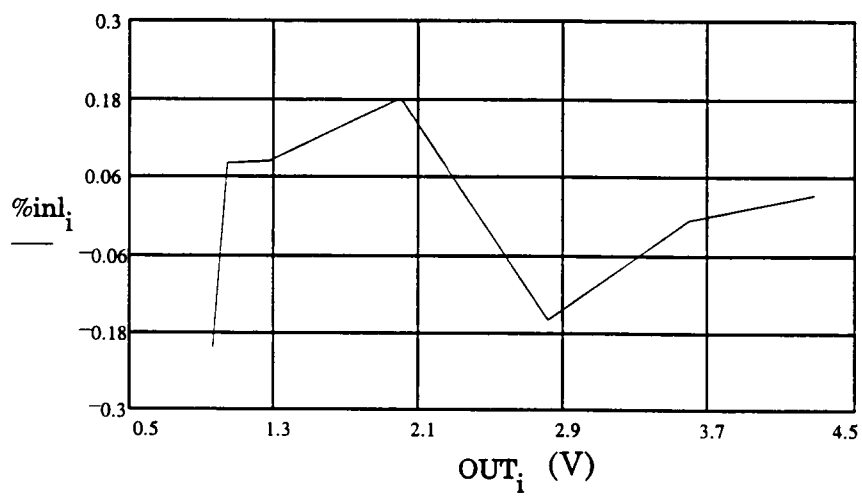


Pipe 1

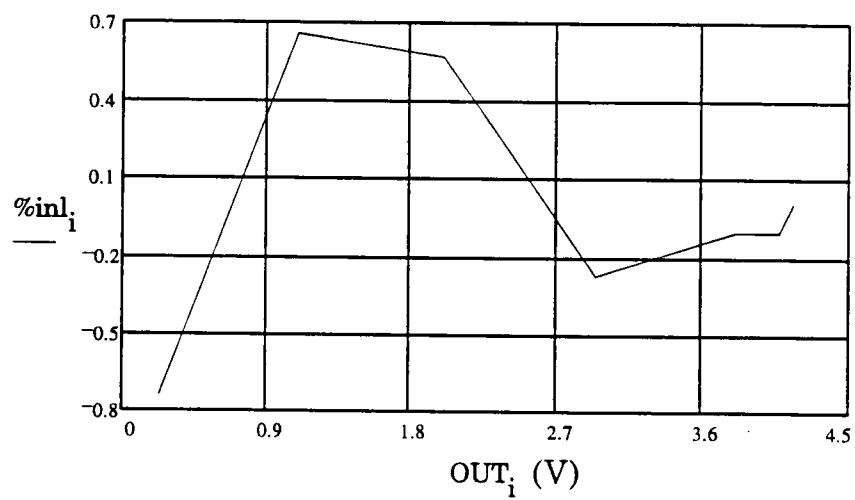
Plate 18. Chip S4A dynamic INL, even cell 6, prerad.



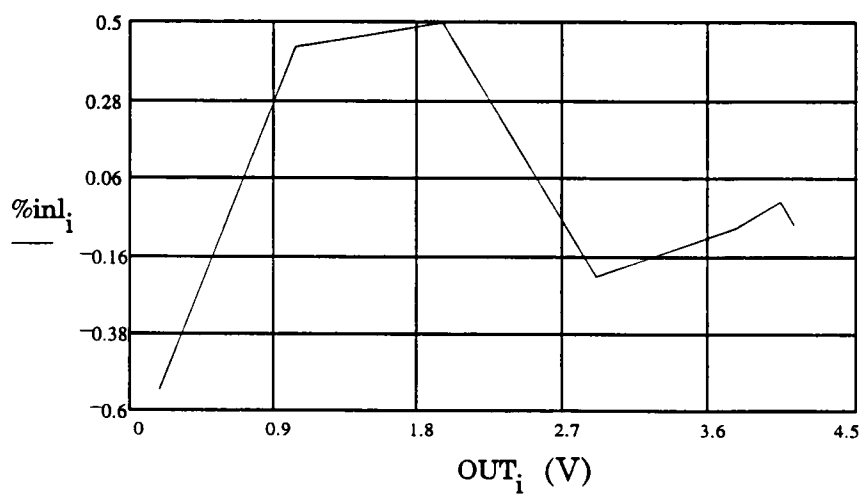
Pipe 2



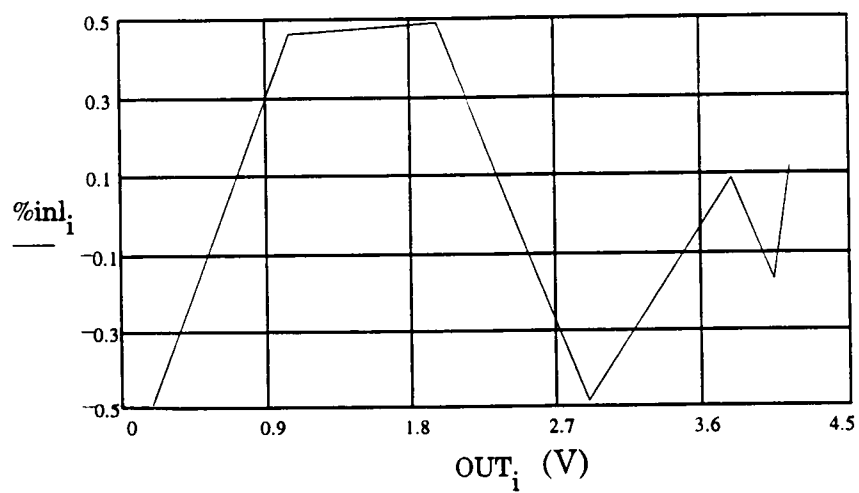
Pipe 3



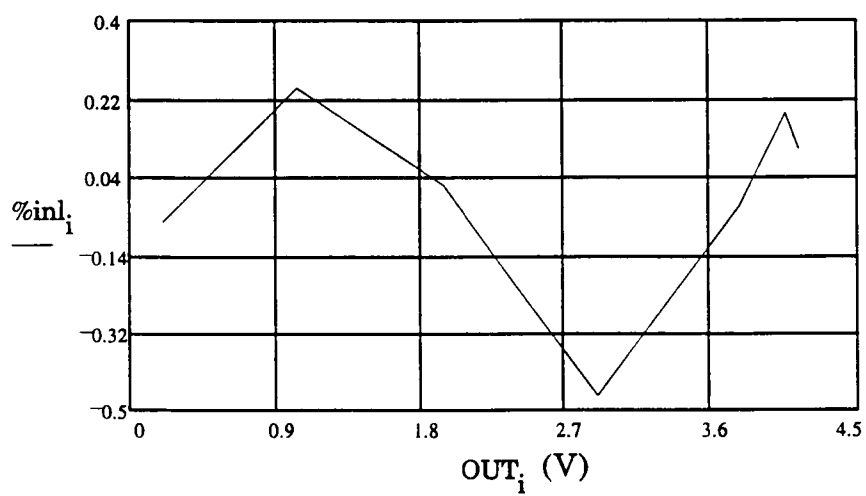
Pipe 4



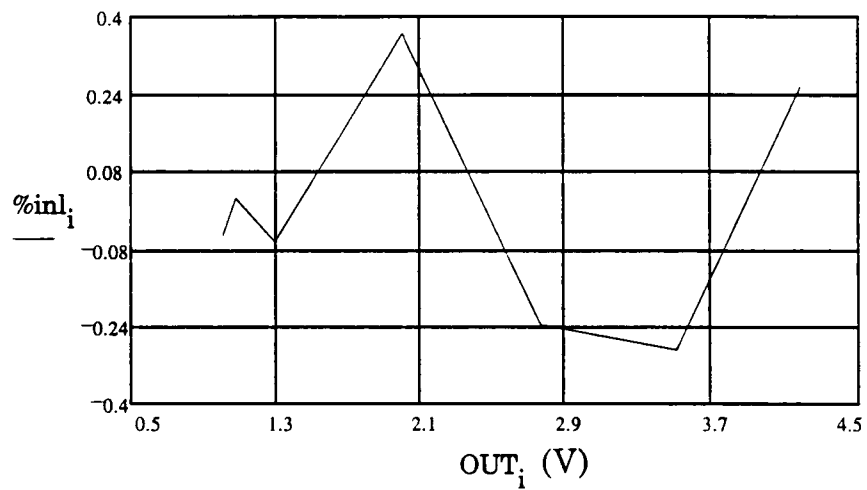
Pipe 5



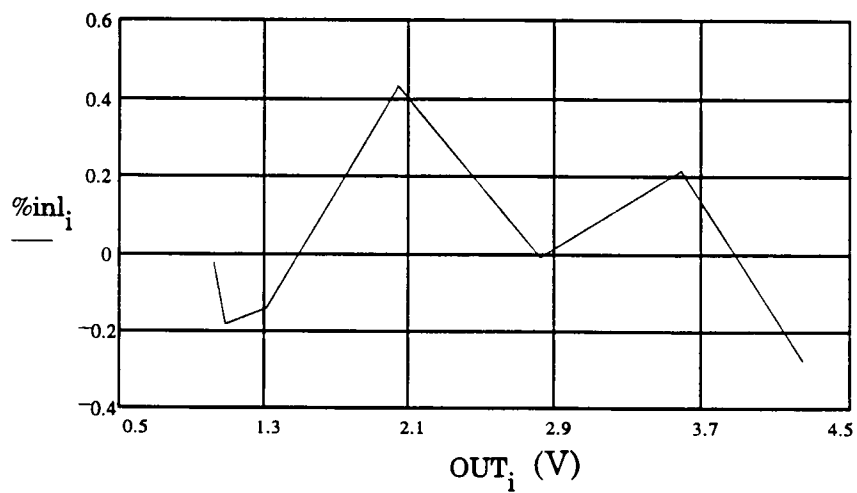
Pipe 6



Pipe 7

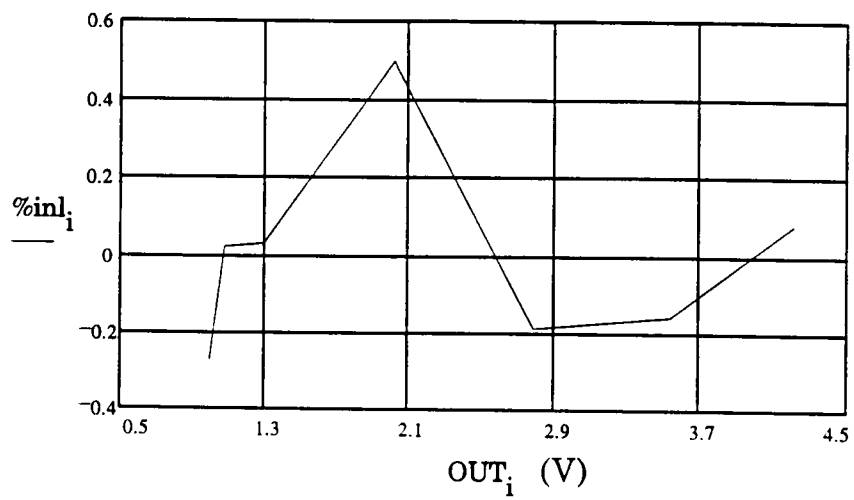


Pipe 0

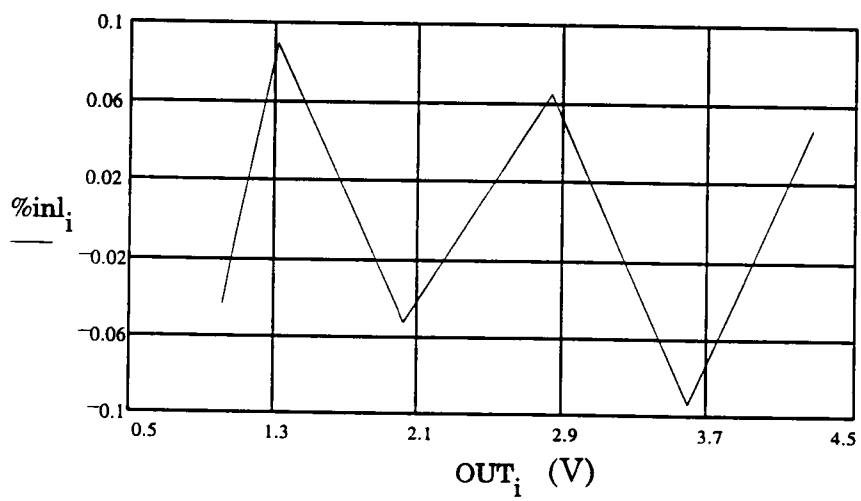


Pipe 1

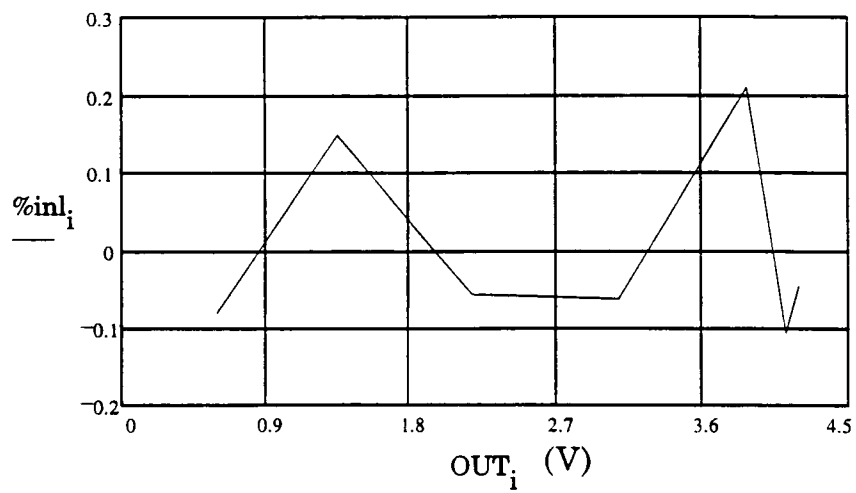
Plate 19. Chip S4A dynamic INL, even cell 6, 5MRad.



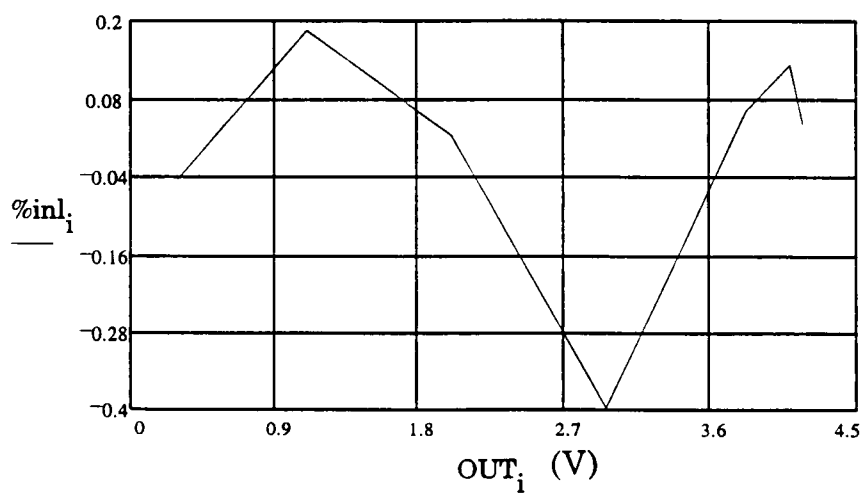
Pipe 2



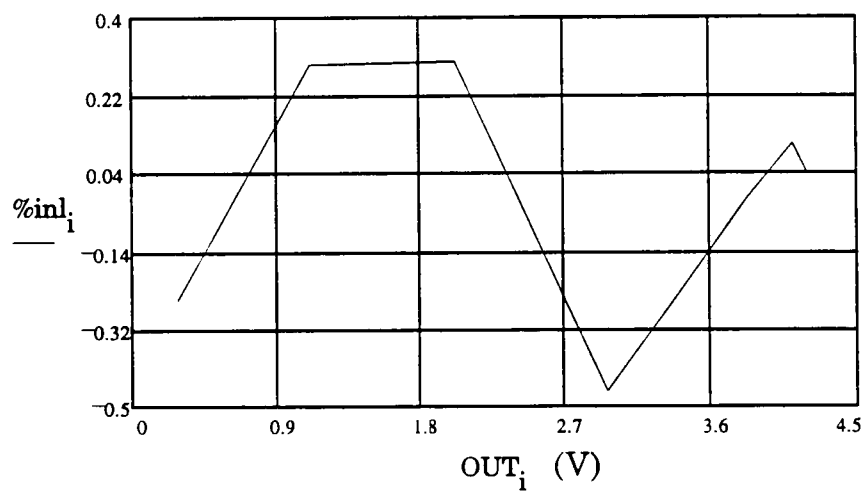
Pipe 3



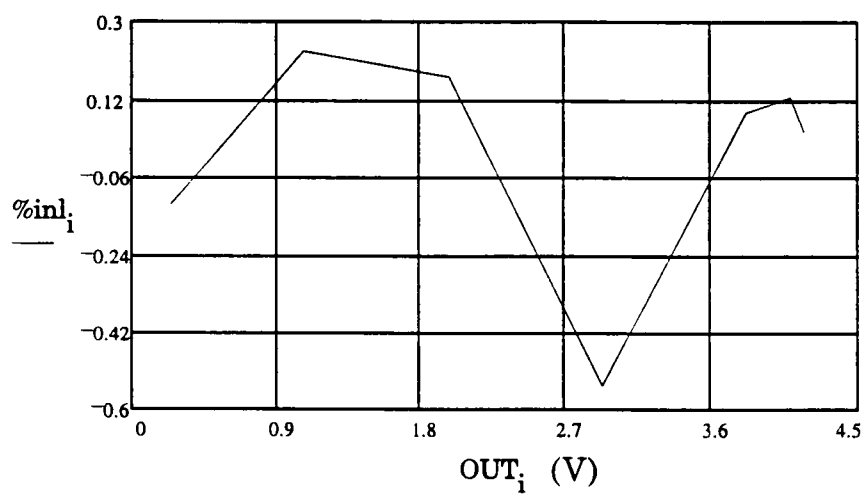
Pipe 4



Pipe 5



Pipe 6



Pipe 7

VITA

Charles Lanier Britton, Jr. was born in Covington, Kentucky on November 17, 1952. He attended secondary schools there, in Louisville, Kentucky, Kansas City, Missouri, Memphis, Tennessee, and Alcoa, Tennessee. He graduated from Alcoa High School in May, 1970 and entered The University of Tennessee the following September. He received the Bachelor of Science degree in Electrical Engineering in June, 1975 and the Master of Science degree with a major in Electrical Engineering in 1978. He worked for Hewlett Packard Company in Colorado Springs, Colorado from 1976 through 1978. He worked for E.G. & G. in Oak Ridge, Tennessee from 1979 through 1985 and for North American Philips from 1985 through 1986. He began work at the Oak Ridge National Laboratory in December 1986 and remains employed there, working in the area of full-custom integrated circuit design. He began to work towards the Ph. D. degree with a major in Electrical Engineering in 1987 and graduated in June, 1995.

Mr. Britton is a member of IEEE, Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi. He has been involved with the IEEE Nuclear Science Symposium as an instructor of short courses on integrated circuit design, and with the technical program committee. He holds two U. S. patents in the area of circuit design.

Mr. Britton lives in Alcoa, has three children and is married to the former Carol Ann Davis of Philadelphia, Pennsylvania.