Characterization and Realization of High Switching-speed Capability of SiC Power Devices in Voltage Source Converter

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Abstract

The emerging wide band-gap, silicon carbide (SiC) power devices greatly improve the switching performance due to their inherent fast switching capability. However, the high switching-speed performance makes their switching behavior become more susceptible to parasitics of the application circuit. In the end, unlike the excellent switching performance of SiC devices tested in manufacturer' datasheets, the observed switching performance in actual power converters is almost always worse. This dissertation aims at characterization and realization of high switching-speed capability of SiC devices in one of the most widely used converter types, the voltage source converter (VSC).

To evaluate the fast dynamic characteristics of SiC devices with high fidelity, a methodology of switching performance characterization is summarized. The assessed switching loss is highly sensitive to V−I timing alignment and cross-talk. A practical method is proposed to cope with these issues for accurate switching loss evaluation.

Based on the methodology of switching performance characterization, limitations and impact factors of switching performance of SiC devices in VSC are explored. Cross-talk, turn-on overvoltage, and parasitics of inductive loads are identified as the "killer" impact factors.

To suppress cross-talk, intelligent gate drivers are designed to be capable of tuning the gate voltage and gate resistance during different switching transients for both devices in a phase-leg. The spurious gate voltage induced by cross-talk can be limited, leading to the improved switching performance with fast switching speed and low switching losses.

To mitigate the turn-on over-voltage and parasitic ringing, the placement of gate drivers, devices and power stage and layout design for SiC devices with TO package are proposed and implemented, enabling 30% power loop and common source inductance reduction.

To decouple the interaction between devices and inductive load, a dedicated auxiliary filter is introduced to reshape the inductive load's high frequency impedance, allowing the switching behavior to become as excellent as that tested by the optimally-designed inductor.

In the end, a SiC based three-phase VSC fed motor drives are built by using the knowledge and techniques developed above. It shows that switching behaviors in VSC have nearly identical performance as that characterized in the optimally-designed switching test circuit.

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1 Introduction

This chapter starts with an introduction of voltage source based power electronics converter in traditional and emerging applications. Then the significance of the switching performance of power devices in voltage source converter is illustrated. After examining the excellent characteristics of silicon carbide (SiC) semiconductor power devices, especially the high switching-speed capability, the benefits and challenges of utilizing fast switching SiC devices in voltage source converter to achieve the optimal switching behavior and overall performance of power conversions are described afterwards. Finally, the organization of this research dissertation is presented.

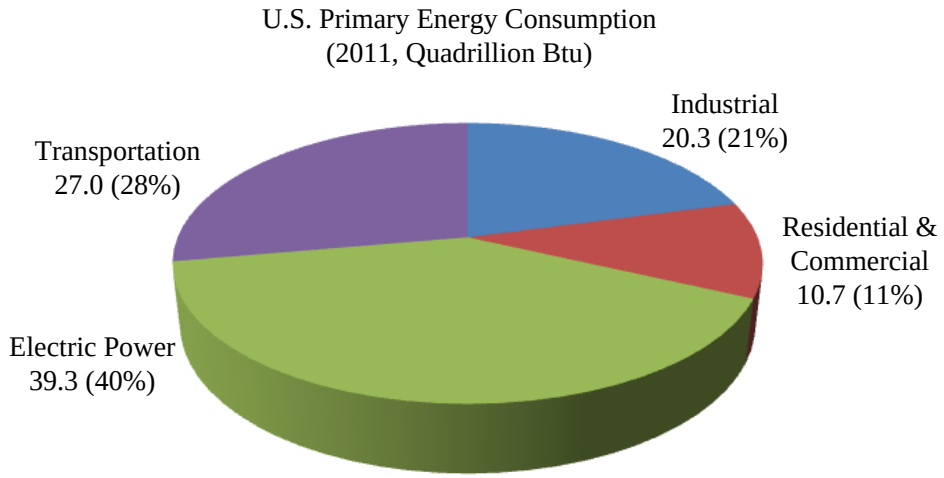


Fig. 1-1. U.S primary energy consumption [1].

1.1 Application Background

40% of the energy in U.S. is consumed by electric energy in 2011, which was more than 13 times greater than the electricity use in 1950 [2, 3]. As the issues of natural resource depletion,

booming of population, and environment conservation have gained greater visibility, the usage of electricity will be growing continuously, and to efficiently converter, control and use electrical energy is critical [4]. As a result, power electronics, as an enabling technique to achieve high efficiency power conversion, becomes more and more popular [5]. In 2005, 30% of the electricity is flowed through power electronics based converters. Furthermore, as expected based on the report of Annual Energy Review DOE/EIA in 2012, 80% of electricity could flow through power converters in 2030 [1].

In power electronics converter, considering simple configuration and high efficiency, voltage source converter is the most popular topology in both traditional and emerging applications. For example, it has been estimated that roughly 65% of electrical energy from the grids of U.S. nowadays is consumed in electrical machine drives, and voltage source pulse width modulation (PWM) converter occupies 99% of the market shares [6-8]. In addition, voltage source converter is dominant in industry power supply systems, such as Uninterruptible Power Supply (UPS), Power Supply Unit (PSU), for information and computing technology, of which the electricity consumption is between 10-15 % of the total U.S. electricity [8]. Furthermore, the voltage source converter is also popular in many emerging applications, such as renewables (e.g., wind, photovoltaic (PV), etc.), utility (e.g., High-Voltage Direct Current electric power transmission system (HVDC), Flexible AC Transmission system (FACTs)), and transportation (e.g., Electric Vehicles (EVs), Locomotives, Airplane) [9-16]. It is found that these emerging applications cover the generation, transmission, and consumption of electricity, which in the future will occupy increased portion of the electrical energy. In the end, voltage source converter is important to power electronics and electrical energy nowadays and in the future.

1.2 Impact of Switching Performance of Devices on Voltage Source Converter

The key design objectives of power conversions across all applications include high power density (i.e., low volume and weight), high efficiency, high reliability, and low cost [1]. The function of power conversion is achieved via controlling the states of power semiconductor devices. Therefore, thousands switching events occur per second to chop the voltage/current to achieve the power conversion, in the meantime, to affect the power conversion.

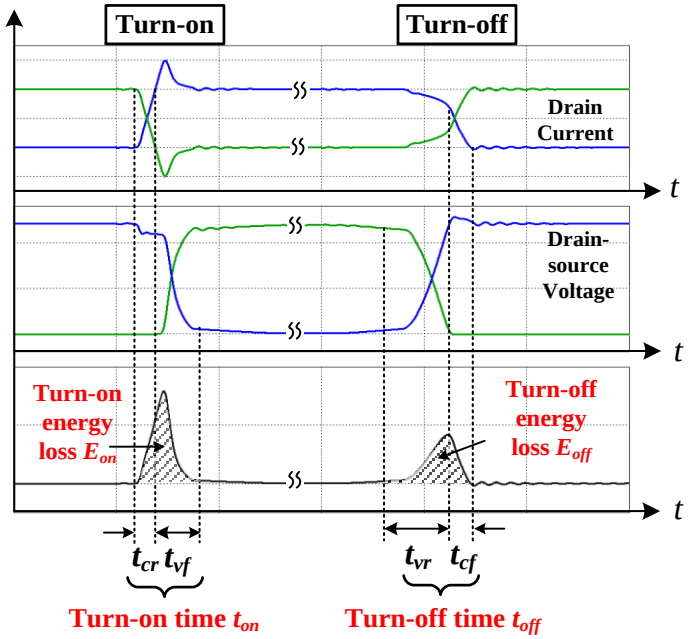


Fig. 1-2. Switching waveform of power devices indicating switching time and switching loss.

As shown in Fig. 1-2, each switching event (turn-on or turn-off) of power devices takes a certain amount of time (i.e., switching time t_{on}, t_{off}) with certain energy dissipation (i.e., switching loss E_{on}, E_{off}), which is the underlying reason causing the non-ideal power conversion [17, 18]. Specifically, according to the aforementioned objectives of power conversions, the

impacts of the switching performance on the efficiency, density, EMI and reliability are illustrated as follows.

1.2.1 Loss and Efficiency

The loss dissipated by power converters primarily comes from three parts: active power loss consumed by power devices, passive components induced loss, and auxiliary circuits related loss. Among them, the devices related active power loss occupies great proportion. For certain applications without magnetic components in the power stage, such as motor drives, electric traction drives, power devices dissipate majority of the total loss of power converter.

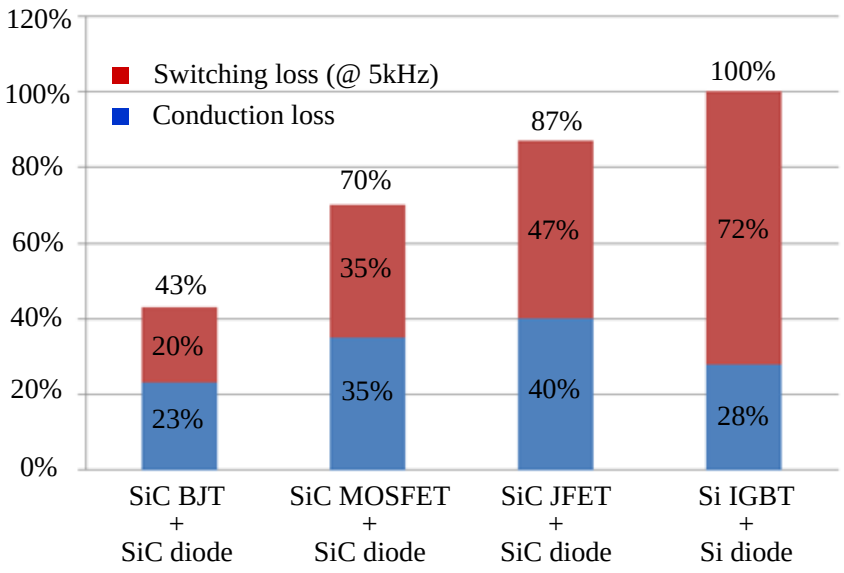


Fig. 1-3. Ratio between switching loss and conduction loss for different power devices [16].

Active power loss consists of conduction loss and switching loss [17, 18]. For the voltage source converter, switching loss is the main contributor to the active power loss as compared to the corresponding conduction loss. Fig. 1-3 displays the ratio between switching loss and

conduction loss with different combination of power devices for a 40 kW traction system [16]. Although the different static and dynamic characteristics of power devices would affect the results, the switching loss is almost always greater than 50% of the total active loss. Also note that the switching frequency is merely 5 kHz in this comparison case. Thus, switching loss plays greater role on voltage source converter with higher switching frequency, which is the trend of the development of power converters. More data in FACTs and EVs also demonstrate the significance of switching loss on the total power loss [13, 14]. In the end, the switching loss of power devices greatly impacts the efficiency of voltage source converter.

1.2.2 Size and Weight

Power devices, cooling systems, passive components, and auxiliary circuits primarily contribute to the size and weight of voltage source converters. Among them, cooling systems (e.g., heat sink and fan) and passive components (e.g., bulky dc bus capacitor and ac inductor, as well as harmonics and EMI filter) are often dominating [9].

As one of the important parameters of designing the required cooling systems, thermal resistance is closely related to the active power loss of devices. Based on the aforementioned analysis, the switching loss would apparently affect cooling requirement, and then impact the weight and size of cooling systems. For example, in hybrid electric vehicles (HEVs), as compared to the traditional power devices, using emerging wide band-gap power devices decreases the size and weight of the heat sink to one third [15].

In addition, the passive components will also be affected due to the switching performance by means of switching frequency. For example, in a 5 kW boost converter, which is an essential part in most PV inverters and EVs, in comparison with the smoothing inductor with 20 kHz

switching frequency, 100 kHz related inductor reduces the size by 70% with less than one fifth weight, as shown in Fig. 1-4 [19]. Also, it is noted that the upper limit of the switching frequency is determined by the switching time and switching loss. First, the switching period (i.e., reciprocal of the switching frequency) should be longer than the switching time. Second, proportional to switching frequency, the switching loss cannot exceed the capability of existing cooling systems in practical applications.

In total, the switching performance of power devices affects the design of cooling systems via switching loss and passive components by switching frequency, and finally influences the size and weight of power converters.

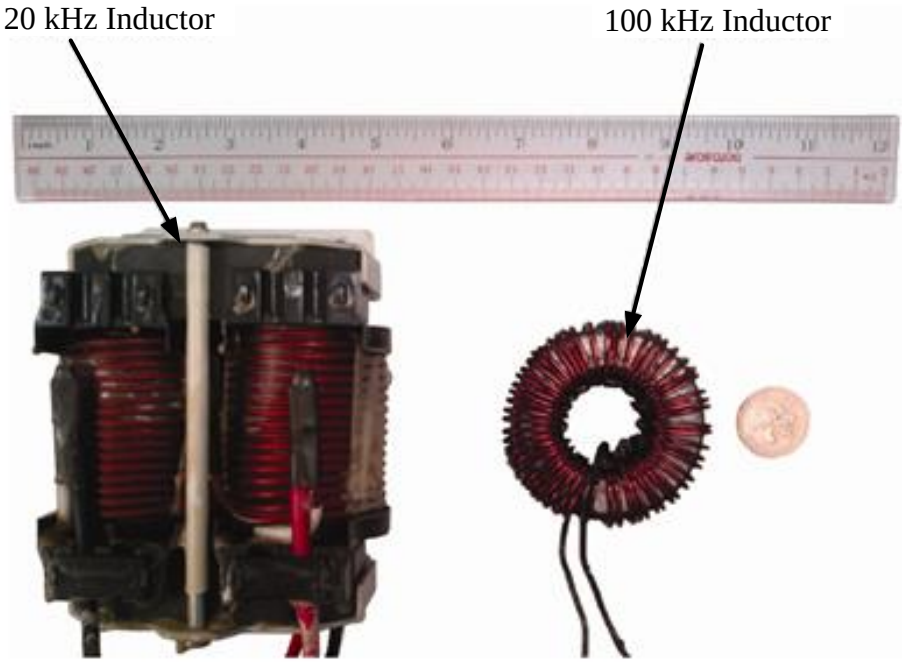


Fig. 1-4. Size comparison of boost inductor between 20 kHz and 100 kHz switching frequency [19].

1.2.3 EMI and Reliability

Electromagnetic interference (EMI) is another critical concern when developing power converters to achieve design objectives. First, EMI will affect the operation reliability of neighboring equipment as well as the power converter itself. Second, to suppress the generated EMI to comply with the standards (e.g., IEC61800-3 Qp for motor drives, DO-160E for airborne equipment), EMI filter has to be used, which will then increase the size and weight of the whole system [9, 19-24].

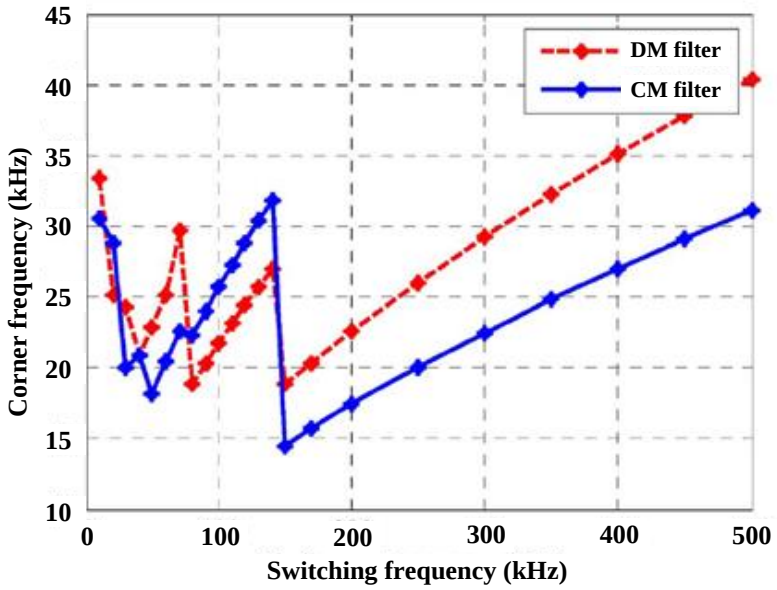


Fig. 1-5. Corner frequency of EMI filters versus switching frequency of power converter [9].

Switching frequency impacts the common mode (CM) and differential mode (DM) bare noise, and then influences the selection of corner frequency of CM and DM filter. Fig. 1-5 shows the corner frequency of EMI filters dependence on the switching frequency for a back-to-back voltage source converter based on the DO-160E standard [9]. It can be observed that switching

frequency affects the corner frequency of EMI filters with a nonmonotonous relationship unless the switching frequencies are beyond 300-500 kHz.

Additionally, *dv/dt* and *di/dt* (i.e., switching speed) is the noise source of EMI, especially at high-frequency range [20]. Faster the switching speed, higher the *dv/dt* and *di/dt* as well as voltage/current overshoot during switching transients. Also, the circuit parasitics induced ringing plays an increasing role in EMI production. As shown in Fig. 1-6, the measured EMI spectra of motor drive systems with fast switching devices are always higher than the spectra of the motor drive systems with slow switching devices in both CM and DM noises, which means that EMI filter with higher attenuation capability should be applied for fast switching device based system to satisfy the same standard [23].

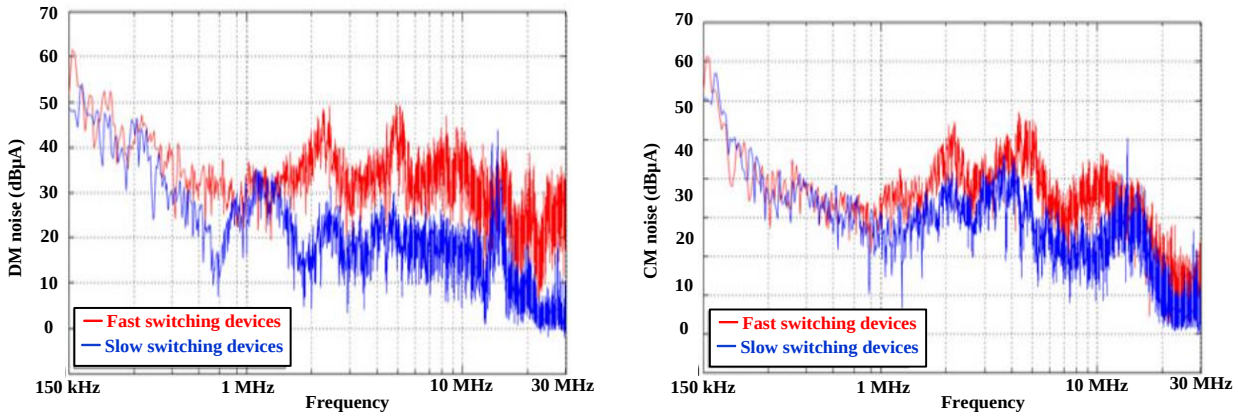


Fig. 1-6. Comparison of measured EMI spectra between fast switching-speed device based motor drives and low switching-speed device based motor drives [23].

In total, either the switching frequency or the switching speed, according aforementioned analysis, is related to the switching performance. Therefore, switching performance significantly affects EMI.

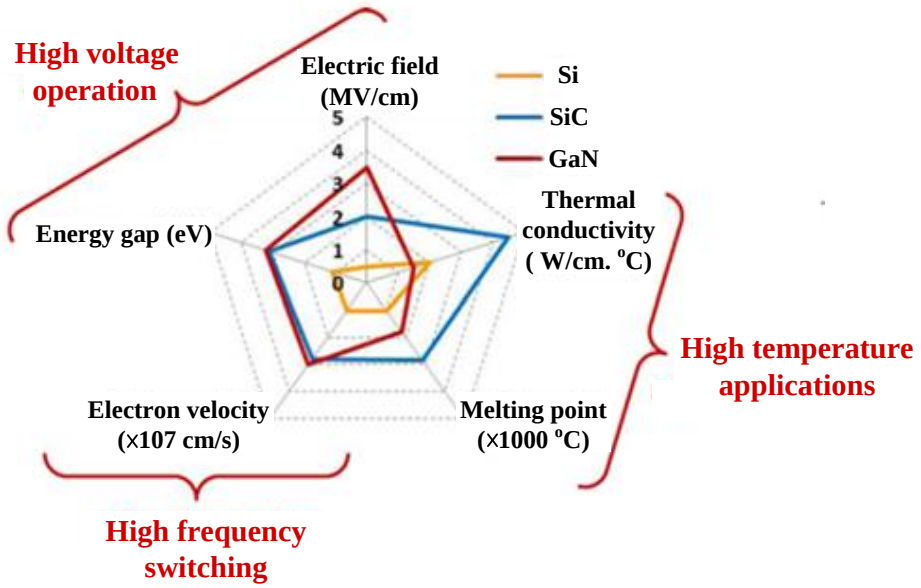


Fig. 1-7. Summary of Si, SiC, and GaN relevant material properties [25].

1.3 Silicon Carbide Devices Applied in Voltage Source Converter

Characteristics of power semiconductor devices, including the switching performance, significantly affect overall performance of power conversion. Currently, these power devices are based on the mature and very well established silicon (Si) technology although Si exhibits some important limitations regarding blocking voltage capability, operation temperature, and switching frequency [25, 26]. Fortunately, a new generation of power devices based on wide band-gap (WBG) semiconductor materials is under development. Among the possible semiconductor materials candidates, silicon carbide (SiC) and gallium nitride (GaN) show the best tradeoff among theoretical characteristics (e.g., high block voltage capability, high temperature operation, and high switching frequency), real commercial availability of the starting material (e.g., wafers and epitaxial layers), and maturity of their technological processes. Some key material properties of WBG semiconductor candidates as compared to traditional Si

are highlighted in Fig. 1-7. In today's market, SiC process technologies are the most mature among WBG semiconductor materials, even as compared to GaN.

1.3.1 Benefits

Table 1-1 lists the main characteristics comparison between Si and 4H-SiC at 300K, where 4H-SiC is generally preferred in practical power device manufacturing currently for its higher carrier mobility and lower dopant ionization energy [27-29]. As can be observed in Table 1-1, since the breakdown field of SiC is higher than that of Si by a factor of 10, a thinner drift layer with higher doping concentration can be utilized for SiC to manufacture the device with the same blocking voltage of their Si counterparts. Thus, a smaller chip size can be achieved. The reduced chip size of SiC devices enables the junction capacitance become small, which means the fast switching speed of SiC devices. Moreover, the velocity of minor carriers swept out of the depletion region is determined by saturation drift velocity. Hence, a higher saturated drift velocity of SiC will also increase the switching speed [28, 30]. In the end, in terms of material's properties, SiC based power devices inherently have high switching-speed capability.

Table 1-1. Comparison of Electrical Properties of Si and 4H-SiC

Material Property	Si	4H-SiC
Energy Bandgap E_G (eV)	1.12	3.26
Breakdown Field E_B (V/cm)	2.5×10^5	2.2×10^6
Thermal Conductivity (W/cm^{o}C)	1.5	4.9
Saturation Drift Velocity v_s (cm/s)	1.0×10^7	2.1×10^7

The parameters in power device's level also demonstrate the high switching-speed capability of SiC devices [27, 31]. For example, as an indicator of how much charge should the gate driver source or sink to turn on and turn off power devices, the gate charge is the smallest for SiC devices as compared to their Si counterparts, including trench/field stop (TFS) Si IGBT, non-punch though (NPT) Si IGBT, Si supper junction MOSFET (SJMOSFET), and Si MOSFET (Si MOS8) in Fig. 1-8. Also note that, as the representative of fast switching Si devices, Si SJMOSFET is rated at only 900 V while SiC devices applied in this comparison is a 1.2 kV part. Therefore, triggered by the gate driver with the same driving capability, SiC devices definitely have the fastest switching speed. Thanks to the fast switching speed and low junction capacitance, the switching loss of SiC devices is the lowest as well. Fig. 1-9 displays the switching loss comparison under different operation temperatures [31].

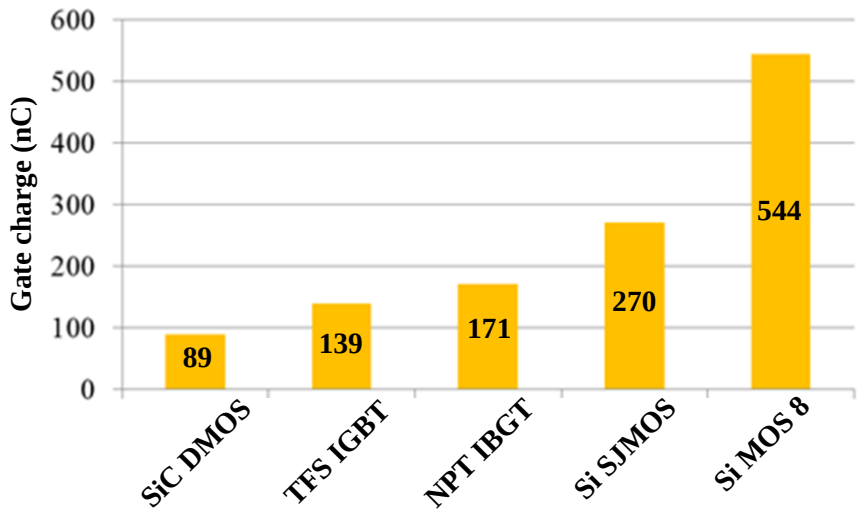


Fig. 1-8. Gate charge comparison between SiC and Si devices [31].

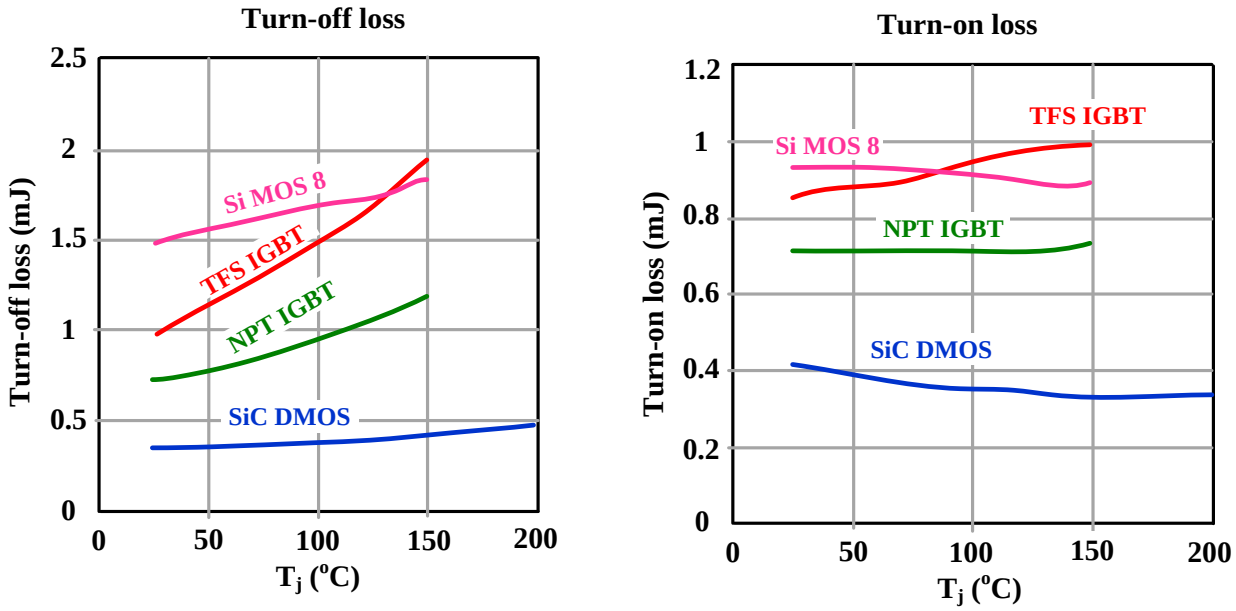


Fig. 1-9. Switching loss versus temperature comparison between SiC and Si devices [31].

1.3.2 Challenges

As described previously, due to the fast switching-speed capability, SiC devices offer a promising opportunity to significantly improve the overall performance of power conversion, such as increased power efficiency and density, as compared to their Si counterparts. However, it is the high switching-speed performance of SiC devices that makes their switching behavior become more susceptible to the parasitics and noise of the application circuit. In the end, unlike the excellent switching performance of SiC devices tested in manufacturer' datasheets, the observed switching performance of SiC devices in actual power converters is almost always worse. Previously reported works observed that in a SiC based current source rectifier, the turn-off energy was increased by a factor of 5, with 3 times longer current fall time compared with the test result of DPT under the same operating condition [32]. Similarly, in a SiC based voltage source inverter, due to the increased overshoot current and slower turn-off time, the total

switching energies were increased by a factor of 1.5 to 1.8 [33]. Therefore, to fully utilize the high switching-speed performance of SiC devices in the voltage source converter, which is the focusing topology in this dissertation, we have to overcome the following challenges:

(1) Characterization of high switching-speed performance of SiC devices in voltage source converter, including measurement of fast switching waveform with high fidelity and processing of obtaining data with high accuracy.

(2) Interpretation of the limitations and impact factors of switching performance of SiC devices in voltage source converter, including all the critical components from both converter and source/load sides.

(3) Development of approaches for suppression of previously identified impact factors in (2) and verification of their effectiveness by means of the proposed methodology for switching characterization of SiC devices in (1).

Once the high switching-speed performance of SiC devices has been realized, efficiency and power density can be improved; in the meanwhile, the EMI and reliability may become worse. It is therefore natural for researchers to question the motivation of maximizing the switching speed of SiC devices in voltage source converter. In author's perspective, high switching frequency with fast switching speed is no doubt the trend of the development of power electronic converters in the future. Thus, it is unwise to sacrifice the high switching-speed capability of the advanced SiC devices to compromise the EMI issue. We should investigate the mechanisms causing EMI issue and novel EMI filter strategies to best serve SiC based power converters. Many researchers have taken the initiatives of exploring EMI noise and filter design for SiC based power converters [9, 20-24]. And it is out of the scope of this dissertation.

1.4 Dissertation Layout

This dissertation is organized as follows:

Chapter 2 reviews the research activities in three areas according to the previously identified challenges of utilization of the high switching-speed performance of SiC devices in voltage source converter, including 1) the widely-accepted methodology of switching performance characterization, 2) the investigated limitations and impact factors of switching performance, and 3) the state-of-art approaches for switching performance improvement of power devices. Since SiC devices are emerging and fundamentals of their switching characteristics are similar to the traditional Si devices, literature review in this chapter focuses on but not limits to the SiC based research. Several works concentrating on the fast switching Si devices are also included.

Chapter 3 illustrates a methodology of switching performance characterization capable of assessing the fast dynamic characteristics of SiC devices with high fidelity. First, a layout design criteria of the switching characterization board is introduced. Second, high-speed measurement issues are discussed, including switching voltage/current detection and voltage-current (V-I) alignment. Among them, a special attention is given on the V-I timing alignment since the assessed switching losses are significantly sensitive to the V-I timing alignment. Also, the latest techniques for high-speed voltage and current measurement and the corresponding models of probes are summarized. Third, the impact of grounding effects induced by probes on the measurement of switching waveforms is illustrated. Fourth, the impact of parasitic ringing on switching loss is analyzed as a fundamental knowledge for the following data processing. Finally, a practical method is introduced to accurately evaluate the switching loss of SiC devices with the consideration of parasitic ringing, cross-talk in a phase-leg, as well as V-I alignment.

Chapter 4 studies the limitations and impact factors of switching performance of SiC devices in voltage source converter. According to inherent properties of SiC devices, six factors are identified and investigated: 1) reverse recovery characteristics of the SiC MOSFETs' body diode, 2) over-voltage of the opposite device during the turn-on transient of the operating one, 3) interference of the lower and upper devices in a phase-leg configuration (i.e., cross-talk), 4) parasitics of the inductive loads, 5) the interaction of phase-legs in a three-phase system, and 6) heat sink. For each factor, the theoretical analysis and experimental verification are presented.

Chapter 5 presents intelligent gate drivers designed to best serve SiC devices in voltage source converter. First, two gate assist circuits are introduced to suppress cross-talk for high switching-speed performance enhancement and devices' reliability improvement, since cross-talk is one of the identified critical limiting factors. And then, to further increase the switching speed as well as to achieve anti-cross-talk functionality, another intelligent gate driver is developed, enabling the overall switching performance of SiC devices to be continuously improved. The basic ideas, gate driver circuits and operating principles of all three gate driver schemes are discussed with the experimental verification for the effectiveness evaluation.

Chapter 6 presents the optimization of interconnection design to achieve the high switching-speed performance of SiC devices in voltage source converter. First, the placement of gate drivers, devices and power stage and PCB layout design are investigated to minimize the critical parasitics in switching loop for the mitigation of over-voltage and parasitic ringing, especially during the turn-on transient. Second, a dedicated auxiliary filter is introduced to decouple the interaction bewteen devices and parasitics of inductive loads during the switching transient. The design criteria and experimental verification are given, respectively.

Chapter 7 presents experimental demonstration of the high switching-speed performance of SiC devices in voltage source converter. A SiC based three-phase voltage source inverter fed motor drives are built by using the knowledge and techniques developed above. The switching behavior of SiC devices in the actual power converter is measured and compared with that tested in the optimal-designed switching characterization circuit.

Chapter 8 presents the conclusion and future work.

2 Literature Review

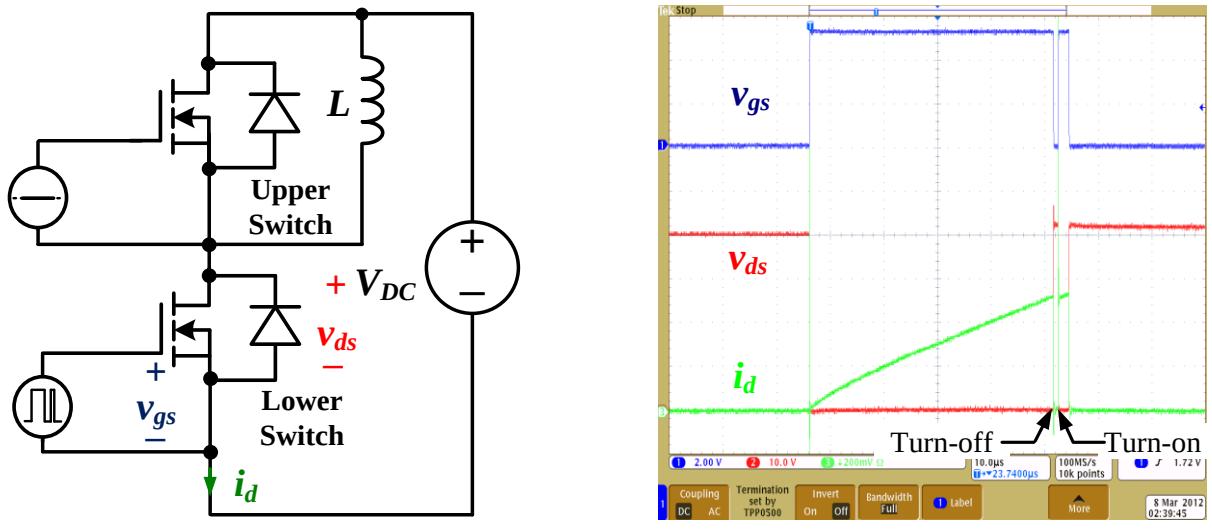
Switching behavior of power devices is important to the performance of power converters for both traditional Si and emerging SiC devices. There are extensive studies on switching performance characterization, analysis, and improvement. In this chapter, the research activities are reviewed in three areas according to the previously identified challenges of utilization of high switching-speed performance of SiC devices in voltage source converter, including first the widely-accepted methodology of switching performance characterization, second the investigated limitations and impact factors of switching performance, and third the state-of-art approaches for switching performance improvement. Since SiC devices are emerging; also the fundamentals of their switching characteristics are similar to the traditional Si devices, literature review in this chapter focuses on but not limits to the SiC based research. Several works concentrating on the fast switching Si devices are also included. In addition, some GaN related studies are reviewed and summarized as well to make the literature review completed.

2.1 Switching Performance Characterization of Power Devices

Nowadays, the widely accepted method to assess the switching performance of power devices is double pulse test (DPT). Two pulses are launched to the device under test (DUT) in a clamped inductive load circuit, as shown in Fig. 2-1. By regulating the dc bus voltage and first pulse duration, the DUT's switching transients can be captured under any desired voltage and current stresses at the end of the first pulse and beginning of the second pulse. Since DUT is switching only twice each trigger, the device junction temperature rise due to the switching loss is reduced to minimum. Based on the DPT, test results quantify the switching performance of power devices, and also provide a basis for the power converters' design, such as switching

frequency selection, dead time setting, thermal management, and efficiency estimation [31, 33-40].

The DPT setup is illustrated in Fig. 2-2. For the control stage, double-pulse signals with adjustable pulse widths are sent from the microcontroller, which is controlled by a PC. The switching waveforms are measured by a oscilloscope, and then the data are transferred back to PC. PC is responsible for programming the double-pulse signals, collecting switching waveforms, and post-processing the raw data. For the power stage, the optimal-layout DPT board is designed with gate driver circuits, power devices, and peripheral interfaces to connect with dc voltage source, load inductor and auxiliary power supply. Considering the SiC devices with high switching-speed capability, the challenges and instructions of DPT are highlighted according to literature review, including high-speed measurement, attachment of probes induced grounding effects, and data processing.



(a) Schematics of DPT. (b) Typical waveforms of DPT.

Fig. 2-1. Double pulse tester circuit.

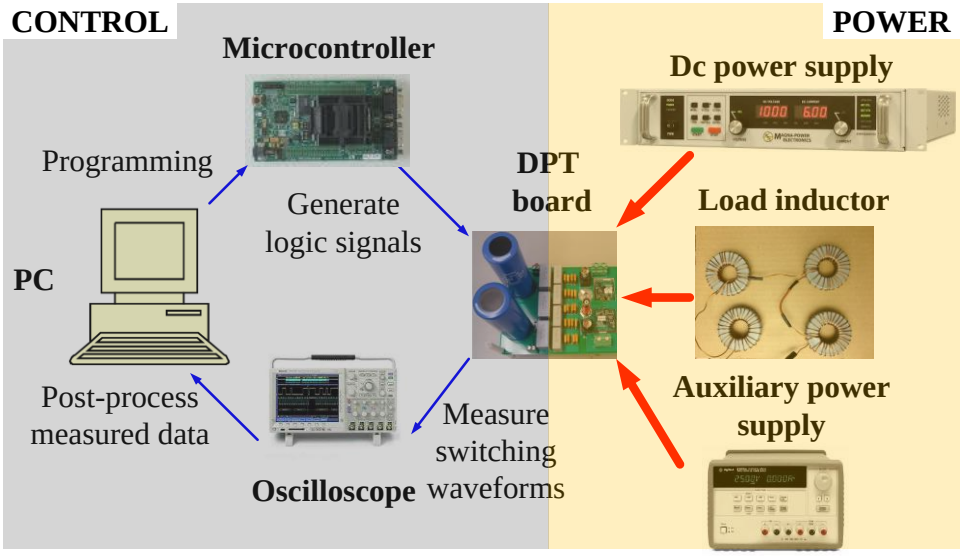


Fig. 2-2. Double pulse tester setup.

2.1.1 High-Speed Measurement

The high-speed switching transients of the SiC device require that the probes should have sufficient bandwidth in order to capture the fast rise and fall edges of the switching waveforms with high fidelity. According to signal theory, the effective bandwidth of a slope signal with a rise time t_r or a fall time t_f can be expressed as [35, 40]

$$f_{SW} = \frac{0.35}{\min(t_r, t_f)} \tag{2-1}$$

Therefore, based on (2-1), the measurement system bandwidth is determined by the fastest switching transient of SiC devices to be captured.

Typically, the switching characterization of power devices basically includes three waveforms, i.e., gate-source voltage v_{gs}, drain-source voltage v_{ds}, and drain current i_d, as displayed in Fig. 2-1 [35, 40]. Therefore, high-speed voltage and current measurement are necessary.

Table 2-1. Pros and cons of different types of high-speed voltage measurement [41-43].

Types	Pros	Cons
Differential probes	Galvanic isolation	Limited bandwidth, long connection leads to device under test
Voltage divider	Ultra-high bandwidth	High resistive loading requirement, not suitable for v_{ds} measurement
Passive probes	High bandwidth, short connection leads to device under test	Non-galvanic isolation

Table 2-2. Pros and cons of different high-speed current measurement techniques [44-48].

Types	Pros	Cons
Coaxial shunt	High bandwidth, high accuracy	Non-galvanic isolation, non-continuous operation
Current transformer	High bandwidth, galvanic isolation	Saturation for large current, non-continuous operation for dc
Split core current probe	Galvanic isolation, continuous operation	Low accuracy, limited bandwidth
Rogowski Coil	Galvanic isolation	Low bandwidth and accuracy

For voltage measurement, high bandwidth and high dynamic range are the two requirements of the voltage probes, especially for v_{ds} measurement. There are three types of voltage probes satisfying the requirements: differential probes, voltage divider probes and passive probes [41]. Table 2-1 summarizes the characteristics of different types of high-speed voltage measurement.

For current measurement, high bandwidth and high accuracy are two requirements. Several current measurement techniques exist for i_d measurement, including coaxial shunt, current transformer, split core current probe, and Rogowski coil. Note that Hall-effect sensors are not considered for the current measurement due to the limited bandwidth which is far less than the necessary bandwidth needed. Table 2-2 summarizes the advantages and disadvantages of different high-speed current measurement techniques.

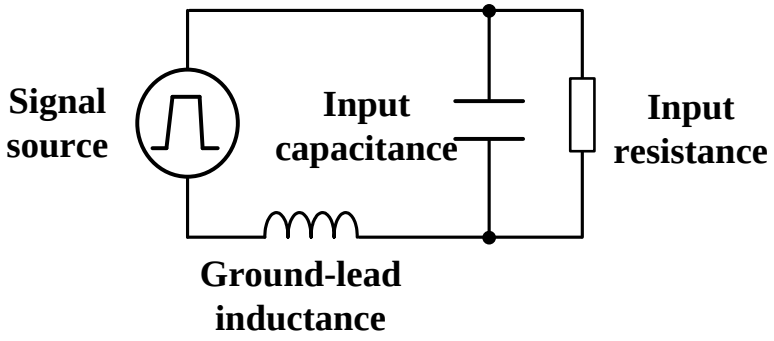
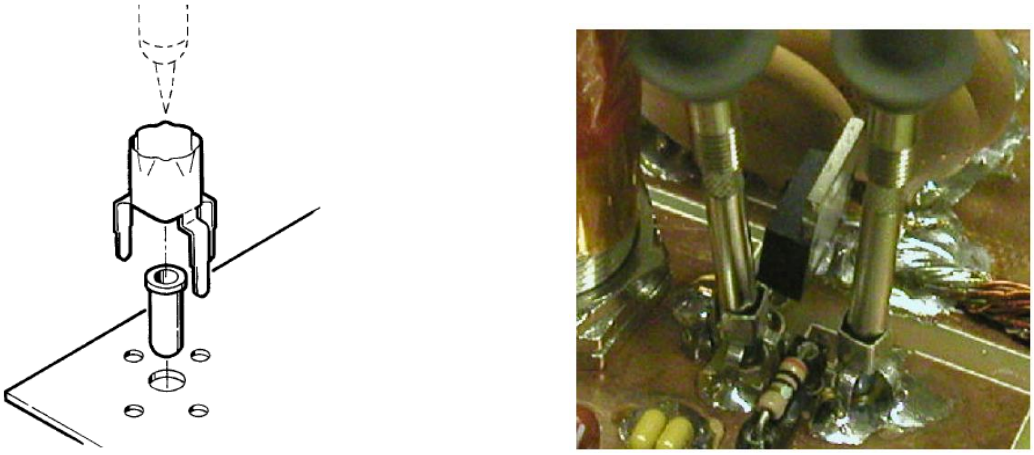


Fig. 2-3. Equivalent circuit of a typical passive probe considering grounding-lead [41].



(a) Schematic diagram [41]. (b) Hardware photo [40].

Fig. 2-4. Probe-tip adaptor.

2.1.2 Attachment of Probes with Test Board

Considering the bandwidth, dynamic range, and measurement accuracy, high voltage passive probe and coaxial shunt have better performance for switching voltage and current measurement. However, measurement accuracy of switching waveforms will be negatively affected by improper attachment of probes with test board. Practically, a short grounding lead is used in the passive probe to clip the grounding point in the circuit under test. However, there is an inductance associated with the grounding lead, as shown in the equivalent circuit of a passive probe in Fig. 2-3. Notice that the grounding-lead inductance with the input capacitance of the probe forms a series resonant network. Once this series resonant circuit is hit with a pulse, ringing is induced. In addition, this excessive grounding-lead inductance will suppress the charging current to the input capacitance and, thus, will limit the rise time of the pulse signal [41, 49, 50]. To reduce the grounding-lead inductance, a probe-tip adaptor is recommended, as shown in Fig. 2-4 [40, 41].

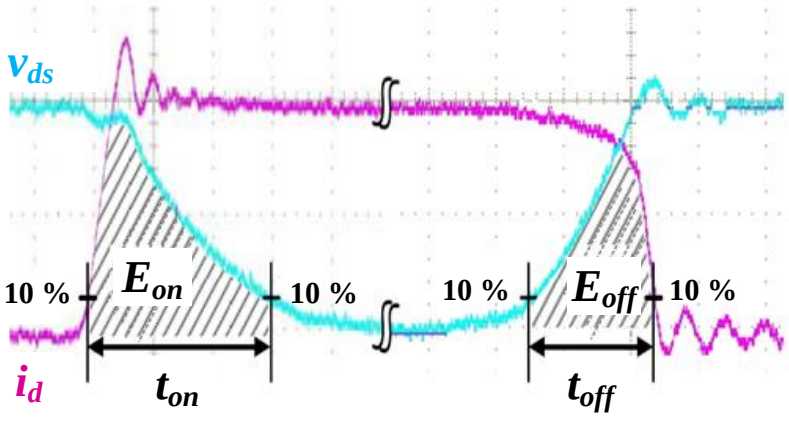


Fig. 2-5. Practical method of calculating switching times and energies [35].

2.1.3 Data Processing

After switching waveforms are captured by oscilloscope, the switching data are imported to PC for the post-processing. Usually, Matlab is used to analyze the raw data and calculate the switching time and energy loss [35, 49]. Fig. 2-5 indicates a commonly applied method to obtain switching times and energies. Specifically, turn-on time is defined as the duration between the moment when the drain current rises to 10% of the inductive load current and the moment at which the drain-source voltage falls to 10% of the dc bus voltage. Similarly, turn-off time is the interval that starts to the drain-source voltage approaching 10% of the dc bus voltage and ends to the drain current reaches 10% of the inductive load current. The switching energy are the integral of drain-source voltage and drain current during the switching time [35].

2.2 Impact Factors of Switching Performance in Voltage Source Converter

Phase-leg configuration is the basic cell of voltage source converter, and commonly selected as the representative of voltage source converter for the switching performance assessment. Fig. 2-6 display the schematics of phase-leg configuration with main components that would impact the switching performance, including power devices, gate drivers, parasitics, and operating conditions. As a user of power devices, the impact factors of switching performance reviewed below only focus on gate drivers, parasitics, and operating conditions.

2.2.1 Gate Driver

As can be observed in Fig. 2-6, generally, gate driver primarily consists of gate driver integrated circuit (IC), signal isolator, and isolated power supply. Among them, gate driver IC directly hooks up with the gate terminals of power devices and is one of the dominant components to determine the switching performance of power devices [51, 52]. Additionally,

signal isolator and isolated power supply, as the auxiliary components to transmit PWM signals and power gate driver IC, would also limit the switching speed if they cannot operate properly during the fast switching transient [53].

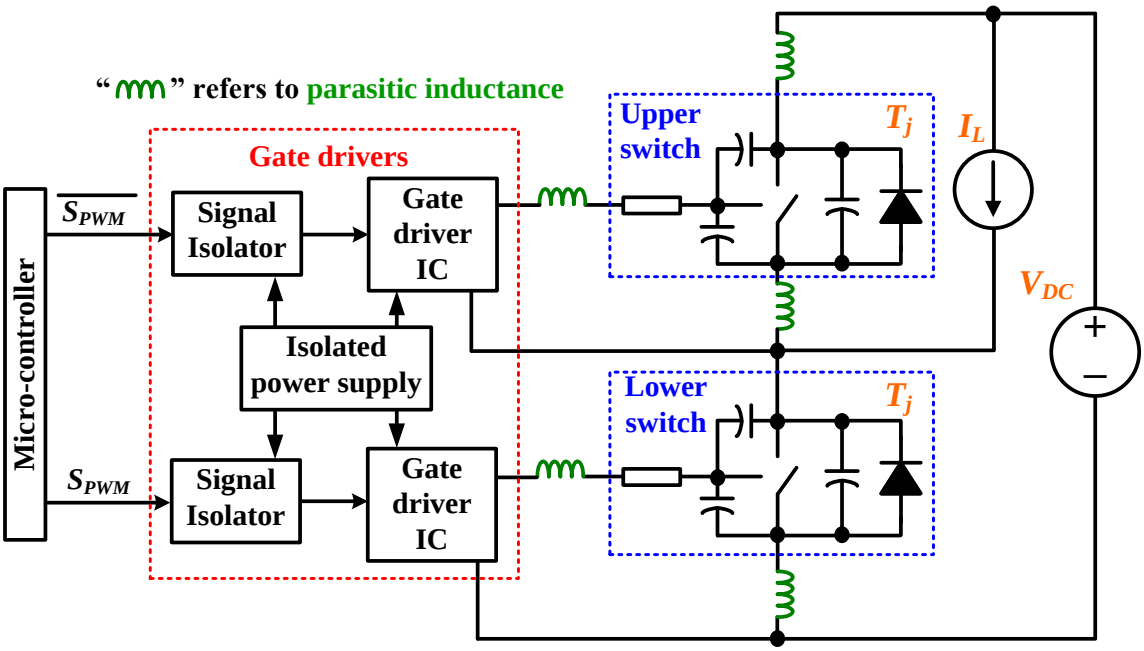


Fig. 2-6. Schematics of phase-leg configuration with gate drivers and parasitics.

First, the influence of gate driver IC on the switching performance is discussed. Fig. 2-7 depicts schematics of phase-leg configuration with gate driver IC. According to its functionality, the gate driver IC can be simplified as a PWM voltage source in series with internal resistance, where the voltage source can be analytically expressed by rise (fall) time and amplitude of gate driver output voltage (t_r, t_f and V_p in Fig. 2-7), the internal resistance represents the pull-up (-down) resistance of gate driver induced by transistors S_1 and S_2 [51, 54]. Assume the lower switch in a phase-leg to be the device under operation, the typical switching waveform during the switching transient of the lower switch is shown in Fig. 2-8.

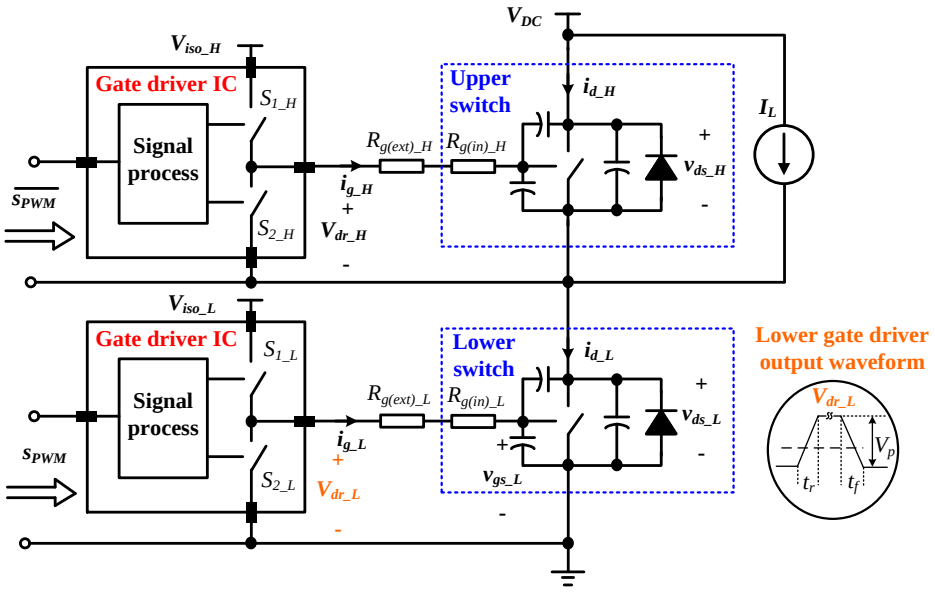


Fig. 2-7. Impact of gate driver IC on switching performance of power devices.

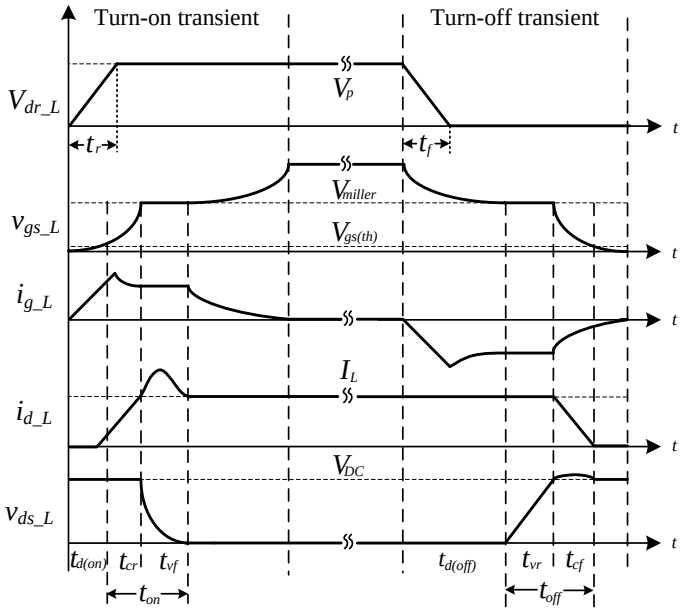


Fig. 2-8. Typical waveforms during switching transient.

Turn on time t_{on} is determined by the current rise interval t_{cr} together with the voltage fall interval t_{vf}. Furthermore, t_{cr} depends on the slew rate of gate voltage v_{gs_L}, and t_{vf} is proportionally

related to gate current i_{g_L} [18, 54]. v_{gs_L} and i_{g_L} in terms of gate driver related parameters are shown as follows.

During the turn on transient, the output of the lower gate driver V_{dr_L} is given by

$$V_{dr\_L}(t) = \begin{cases} \frac{V_p}{t_r} \times t, 0 < t < t_r \\ V_p, \ t > t_r \end{cases} \tag{2-2}$$

where V_p and t_r refer to the amplitude and rise time of lower gate driver output voltage, as shown in Fig. 2-7.

The gate voltage v_{gs_L} during current rise interval t_{cr} is shown as

$$v_{gs\_L}(t) = \begin{cases} \frac{V_p}{t_r} R_{g\_L} C_{iss\_L} \times e^{-\frac{t}{R_{g\_L} C_{iss\_L}}} + \frac{V_p}{t_r} \times (t - R_{g\_L} C_{iss\_L}), t < t_r \\ V_p + \frac{V_p}{t_r} R_{g\_L} C_{iss\_L} (e^{-\frac{t_r}{R_{g\_L} C_{iss\_L}}} - 1) \times e^{-\frac{t - t_r}{R_{g\_L} C_{iss\_L}}}, \ t > t_r \end{cases} \tag{2-3}$$

where C_{iss_L} and R_{g_L} refer to the input capacitance and gate loop resistance associated with the lower switch.

The gate current i_{g_L} charging the Miller capacitor during the voltage fall interval t_{vf} is

$$i_{g\_L}(t) = \frac{V_{dr}(t) - V_{Miller}}{R_{g\_L}} \tag{2-4}$$

where $V_{dr}(t)$ is the output voltage of the gate driver, V_{Miller} refers to the Miller plateau.

According to (2-2) - (2-4), the switching speed during the turn-on transient is determined by t_r, V_p, and R_{g_L}. Note that R_{g_L} consists of three parts: the pull-up resistance of the gate driver, external gate loop resistance $R_{g(ext)\_L}$, and inner gate resistance of the power devices $R_{g(in)\_L}$. Resistances within the gate driver IC and power devices are inevitable. Once the device is selected, the minimum value of R_{g_L} is based on the pull-up resistance of gate driver.

The analysis of the turn-off transient is similar. Remarkably, the impact of these parameters on the switching speed under different operating conditions is different. When t_r or t_f is longer than the delay time $t_{d(on)}$ or $t_{d(off)}$, gate voltage v_{gs_L} during the current rise interval t_{cr} and gate current i_{g_L} during the voltage fall interval t_{vf} will be primarily limited by t_r or t_f, rather than V_p and R_{g_L}. Consequently, t_r or t_f becomes the dominant limit factor of the switching speed. Otherwise, the switching speed largely depends on V_p and R_{g_L}.

Fig. 2-9 shows the influence of t_r on gate driver capability. Based on the aforementioned analysis, v_{gs_L} during the current rise subinterval together with i_{g_L} during the voltage fall subinterval determine the turn-on time t_{on}. In Fig. 2-9, the orange curve shows v_{gs_L} and i_{g_L} with t_r of 2 ns, which is approximately equal to $t_{d(on)}$. It is straightforward to observe that v_{gs_L} and i_{g_L} with t_r of 10 ns (pink curve) are lower than that with t_r of 2 ns (orange cure). However, the differences of v_{gs_L} and i_{g_L} between t_r of 2 ns and that of 1ns (blue curve) are slight. Therefore, if t_r is larger than $t_{d(on)}$, then t_r tremendously affects gate driver capability. Otherwise, t_r no longer impacts the device switching speed, as shown in Fig. 2-10. Table 2-3 summarizes dominant factors of gate driver IC that limits the switching speed under different operating conditions.

Table 2-3. Dominant factors of gate driver IC that limits switching speed under different operation conditions

Turn-on transient	Operating conditions	$t_r < t_{d\ (on)}$	$t_{d\ (on)} < t_r$
	Dominant factors	V_p, R_{g_L}	t_r
Turn-off transient	Operating conditions	$t_f < t_{d\ (off)}$	$t_{d\ (off)} < t_f$
	Dominant factors	V_p, R_{g_L}	t_f

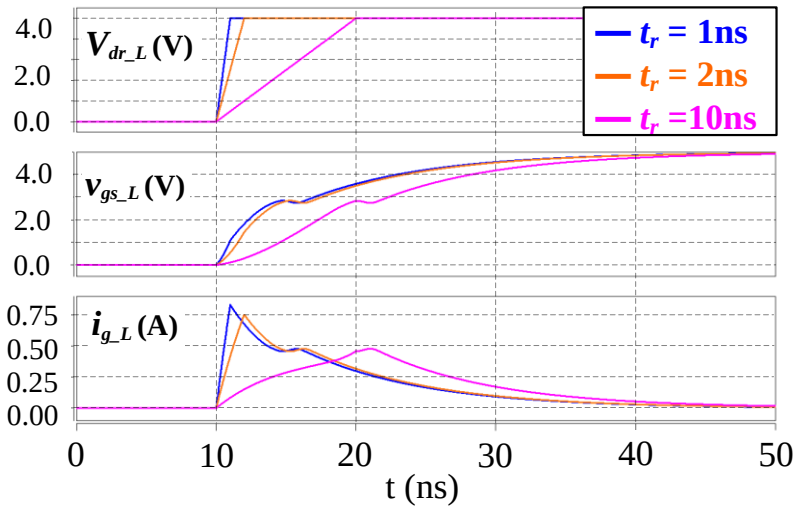


Fig. 2-9. Impact of t_r on v_{gs_L} and $_{ig\_L}$.

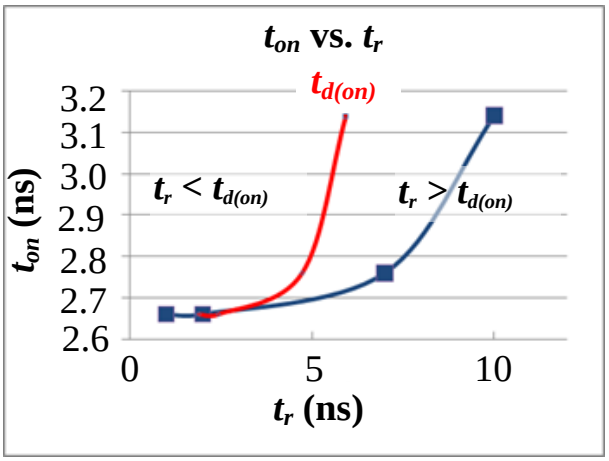


Fig. 2-10. t_r vs. t_{on} based on $t_{d(on)}$.

In addition to the gate driver IC, signal isolator and isolated power supply will also limit the switching speed if the fast switching transient makes them abnormally operate. As shown in Fig. 2-6, the ground of the secondary side of signal isolator and isolated power supply for the upper switch associated gate driver circuit swings from dc bus voltage to 0 when the states of power devices are changing. Therefore, the primary and secondary sides of isolation components suffer

high *dv/dt* during the switching transient. Meanwhile, the input-to-output parasitic capacitance (i.e., C_{IO} in Fig. 2-11) offers a path to conduct common source (CM) noise induced by *dv/dt* [53, 55, 56]. In the end, PWM signals from micro-controller will be interfered; and the output voltage quality of the isolated power supply will be affected. Thus, the input-to-output parasitic capacitance of signal isolator and isolated power supply results in limited CM noise immunity capability, and eventually negatively affect the switching speed of power devices, especially for fast switching SiC or GaN devices. For example, the maximal *dv/dt* immunity capability of the commercial available signal isolator is around 35 kV/μs to 50 kV/μs [57, 58]. However, the *dv/dt* of SiC devices has already approached up to 80 kV/μs. Even worse, for GaN transistor, *dv/dt* of 150 kV/μs has been reported [53].

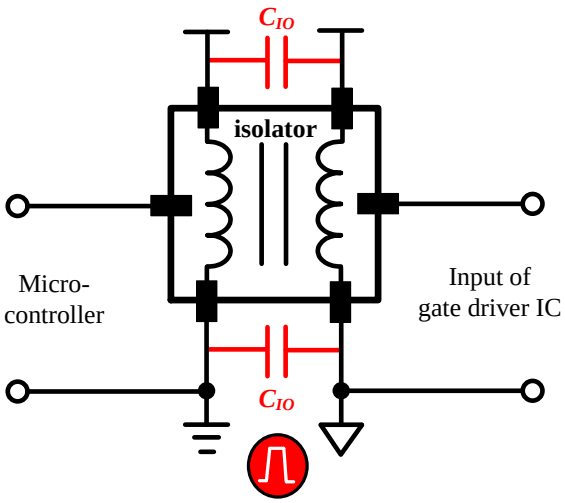


Fig. 2-11. Effect of common mode noise on high side signal isolator.

2.2.2 Parasitics

Parasitics is another critical impact factor to limit the switching speed [59-64]. Fig. 2-12 shows the primary parasitics involved in switching transitions, including three parasitic

inductances, three parasitic capacitances, and one internal gate resistance of power devices. All the parasitics are divided into three groups according to their positions in switching commutation loop, namely parasitics in the gate loop (i.e., gate loop inductance L_{gs}, gate-source capacitance C_{gs}, and internal gate resistance $R_{g(in)}$), parasitics in the power loop (i.e., power loop inductance L_{ds} and drain-source capacitance C_{ds}), and mutual parasitics shared in both gate and power loops (i.e., common source inductance L_{cm} and Miller capacitance C_{gd}).

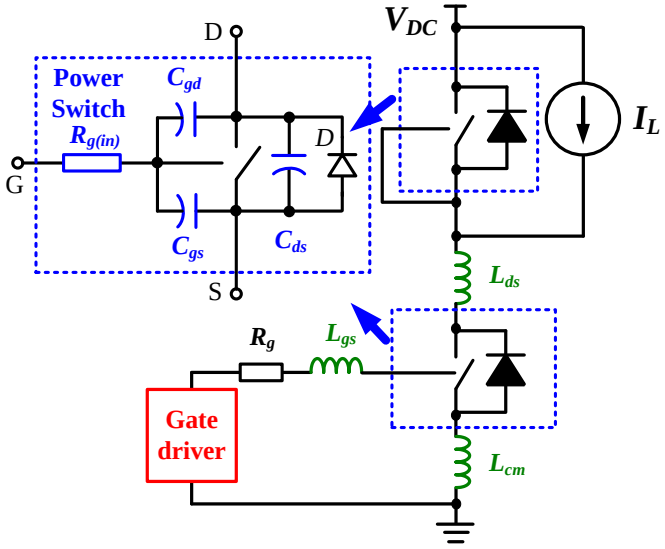


Fig. 2-12. Parasitics involving in the switching commutation loop.

First, parasitics in the gate loop are discussed. As can be observed in Fig. 2-13, parasitic inductance, junction capacitance and gate resistance associated in the gate loop, including gate loop inductance L_{gs}, gate-source capacitance C_{gs}, and internal gate resistance of power devices $R_{g(in)}$, forms a *LRC* series resonant network and causes the oscillation in the gate-source voltage [35]. For GaN devices with low gate voltage rating, such as EPC GaN transistors, this gate loop ringing easily allows the voltage overshoot at gate-source terminals to exceed the maximum

allowable gate voltage required by devices, and then overstress devices [65]. In this case, a large external gate resistance $R_{g(ext)}$ has to be selected to suppress the gate loop resonance with the penalty of switching speed reduction. Also, the phenomenon of the self-sustained oscillation during the turn-off transient due to relatively large gate loop inductance L_{gs} was investigated for fast switching SiC JFET in [66]. Fortunately, parasitics in the gate loop has limited impact on the switching waveform in the power loop. Also, due to the small chip size of SiC devices as compared to their Si counterparts, the internal gate resistance $R_{g(in)}$ of SiC devices becomes large, which to certain extend suppresses the ringing induced by *LRC* resonance network in the gate loop [27]. In the end, gate loop parasitics may influence the switching performance, but with limited contribution.

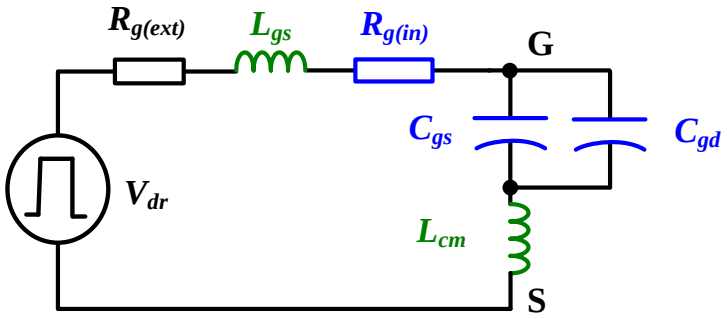
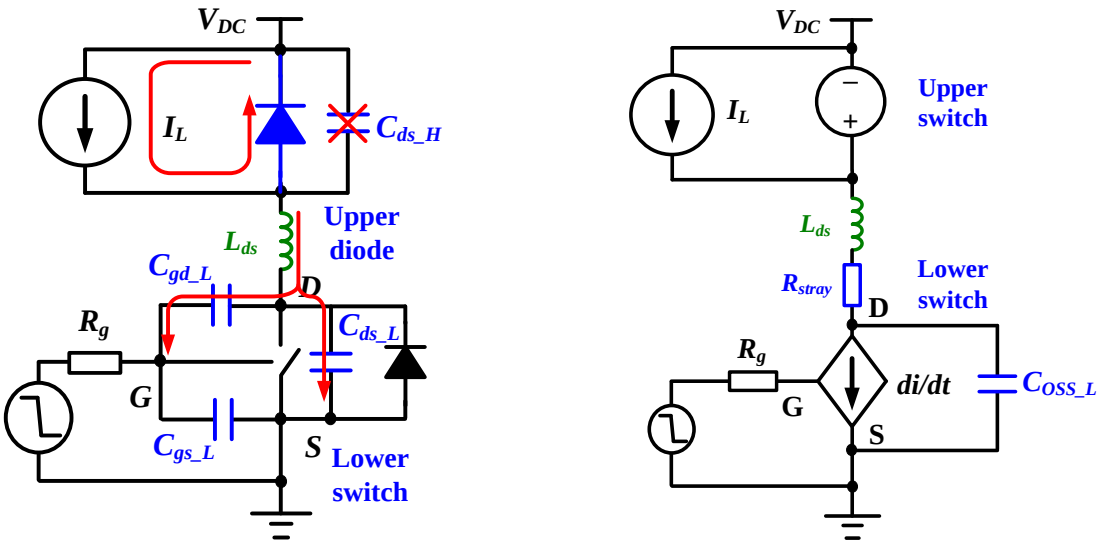


Fig. 2-13. Equivalent circuit of gate loop with parasitics.

As compared to parasitics in the gate loop, power loop parasitics play a greater role on the switching performance of power devices [35, 63]. It is the power loop inductance L_{ds} resonance with drain-source capacitance C_{ds} that causes parasitic ringing in drain current and drain-source voltage. Taking turn-off transient of the lower switch as an example, as shown in Fig. 2-14, the upper switch stays off and can be represented as a freewheeling diode. Considering the high *di/dt*

drain current of the lower switch flows into a paralleled *LRC* resonance network formed by L_{ds}, output capacitance of the lower switch C_{oss_L} and stray resistance R_{stray} in the power loop, an over-voltage is induced across the drain-source terminals of the lower switch. Unlike the gate loop, the damping factor in power loop is smaller ($R_{stray} << R_g$), and the slew rate of drain current is much higher than that of the gate current ($di_{d\_L}/dt >> di_{g\_L}/d_t$). Thus, the parasitic ringing in power loop is more serious with higher drain-source voltage overshoot. To guarantee drain-source voltage of power devices below their breakdown voltage, the slew rate of drain current has to be controlled within certain boundary. In other words, the switching speed is limited.



(a) Schematics. (b) Equivalent circuit.

Fig. 2-14. Mechanisms causing resonance during turn-off ringing transient.

The last and the most important impact factor of switching speed is the mutual parasitics shared in both gate and power loops, i.e., common source inductance L_{cm} and Miller capacitance C_{gd}. During *di/dt* transient (i.e., t_{cr} during turn-on and t_{cf} during turn-off in Fig. 1-2), the voltage

across common source inductance L_{cm} reduces the effective gate driver output voltage, and then decreases the gate current that is used to charge/discharge gate-source capacitance C_{gs}. In the end, the switching speed is reduced [35, 62]. Similarly, during *dv/dt* transient (i.e., t_{vf} during turn-on and t_{vr} during turn-off in Fig. 1-2), the displacement current induced by Miller capacitance C_{gd} distributes the gate current that originally flows to gate-source capacitance C_{gs} [17, 18, 51]. Therefore, the speed of the switch state transition becomes slow. In addition to the aforementioned qualitative analysis, the following explanation with analytical expression is more easily understandable.

During *di/dt* transient, the voltage across common source inductance v_{Lcm} is expressed as

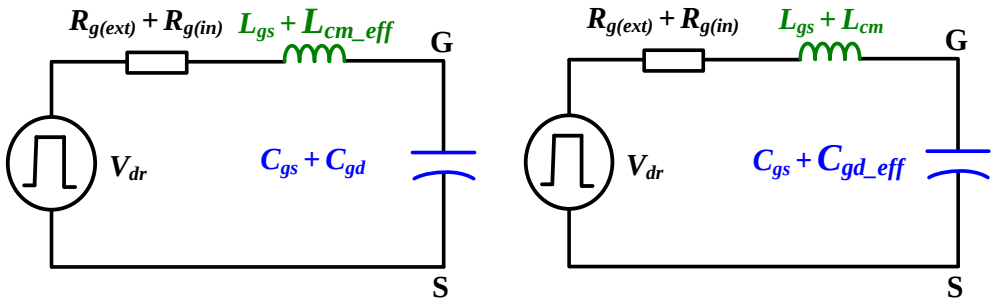
$$v_{Lcm} = L_{cm}\frac{d}{dt}\left(i_d - i_g\right) = L_{cm}\left(\frac{di_d}{di_g} - 1\right) \times \frac{di_g}{dt} = L_{cm\_eff}\frac{di_g}{dt} \tag{2-5}$$

where L_{cm_eff} is the effective common source inductance in the gate loop during *di/dt* transient. As di_d/di_g >>1, L_{cm_eff} is much larger than L_{cm}, which means the equivalent gate loop impedance increases, especially at high frequency. Therefore, the switching speed during *di/dt* decreases.

During *dv/dt* transient, the current flows into Miller capacitance i_{Cgd} is given by

$$i_{Cgd} = C_{gd}\frac{d}{dt}\left(v_{ds} - v_{gs}\right) = C_{gd}\left(\frac{dv_{ds}}{dv_{gs}} - 1\right) \times \frac{dv_{gs}}{dt} = C_{gd\_eff}\frac{dv_{gs}}{dt} \tag{2-6}$$

where C_{gd_eff} is the effective Miller capacitance in the gate loop during *dv/dt* transient. As dv_{ds}/dv_{gs} >>1, C_{gd_eff} is much larger than C_{gd}, which is the mechanism causing Miller effect [51]. Therefore, the fast switching speed during *dv/dt* is limited. Fig. 2-15 shows the equivalent circuit of the gate loop considering the effect of common source inductance and Miller capacitance.



(a) During *di/dt* transient. (b) During *dv/dt* transient.

Fig. 2-15. Equivalent circuit of gate loop considering the effect of common source inductance and Miller capacitance.

In addition to the traditional parasitics discussed above, recently, few studies start to focus on parasitics induced by other components of SiC based power converters, such as heat sink and inductive load [19, 33]. For example, in a three-phase PWM inverter, SiC devices are attached to a heat sink for thermal management. Usually, a thin layer of insulating material is used to separate the SiC devices from the electrically conductive heat sink. Thus, as shown in Fig. 2-16, a parasitic capacitance C_{dh} is formed between the drain base plate of the SiC devices and the common heat sink plate. These parasitics capacitances induced by lower and upper devices are connected in series via electrically conductive heat sink. In the end, a lumped coupling capacitance is formed and paralleled with drain-source terminals of devices, which equivalently increases their effective output capacitance. It was investigated in [33] that for SiC JFETs with anti-paralleled diodes, due to the capacitive coupling effect, the switching performance is significantly deteriorated, causing the current spike to increase by a factor of 1.75 and turn-off switching time reduced up to 60%. Also, the parasitics of inductive load worsen the switching performance. Taking adjustable speed drive application as an example, the test results indicate

that the efficiency of the Si PWM inverter decreases due to the use of long power cables and its resultant higher switching losses [67].

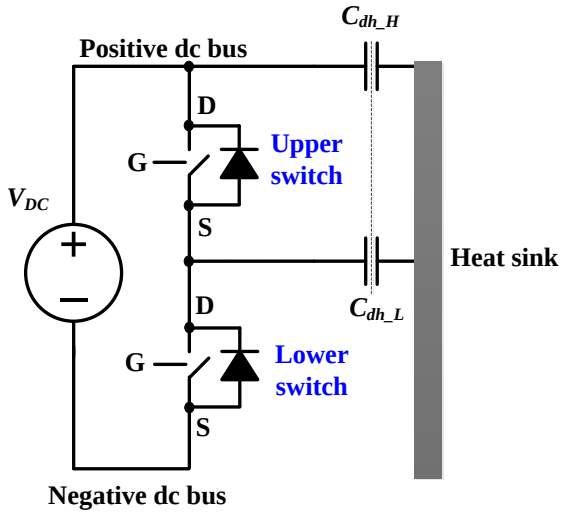


Fig. 2-16. Capacitive coupling between drain terminal of SiC devices and heat sink plate in the phase-leg configuration.

2.2.3 Operating Conditions

Switching performance is also affected by operating conditions, such as dc bus voltage, inductive load current, and junction temperature. For SiC devices, the influence of operating voltage and current on the switching behavior is similar to that of their Si counterparts, which will not be repeated in the section.

However, as compared to Si devices, the switching performance of SiC devices dependence on junction temperatures is different. As junction temperature increases, the threshold voltage of SiC devices reduces, and their transconductance increases. Therefore, during the turn-on transient, turn-on delay time becomes shorter due to the lower threshold voltage. *di/dt* turns to be

higher because of the larger transconductance. Also the lower Miller plateau makes the charging gate current during the *dv/dt* transient larger, leading to higher *dv/dt*. In the end, the turn-on switching speed is accelerated as the junction temperature increases. And then, the resultant turn-on switching loss is lower. On the other hand, during the turn-off transient, the lower Miller plateau at higher operating temperature prolongs the turn-off delay time. Also the discharging gate current becomes lower, causing longer switching voltage commutation time and turn-off time. In the end, the turn-off switching loss turns to be higher. In general, the total switching loss dependence on junction temperature stays nearly constant.

Additionally, two aspects need to be taken into account when the turn-on switching performance of SiC devices is analyzed at high operating temperature: one is the reverse recovery characteristics of device's body diode; the other is the interference between lower and upper switches in a phase-leg (i.e., cross-talk). First, SiC has shorter lifetime of minority carriers so that not a large reverse recovery current is estimated, which enables the body diode of the SiC MOSFET to be a brilliant body diode with almost no reverse recovery charge [68]. However, due to the lateral-vertical channel design, the body diode of normally-on SiC-JFETs and SiC MOSFETs is a P-N junction diode. Although its reverse recovery characteristics are substantially lower when compared to the state-of-art Si counterparts, and equivalent to that of a discrete SiC SBD [31, 69], the performance at high operating temperature will become worse. It is reported that the body diode of normally-on SiC JFETs gave rise to severe reverse recovery as junction temperature increases, leading to significant increase of switching losses[70]. Second, due to higher *dv/dt* and lower threshold voltage of SiC devices at increased junction temperature, cross-talk becomes severe, which enables the potential hazard of shoot-through failure during the turn-on transient to be worse. In the end, without Schottky barrier diodes antiparalleled with main

switches and cross-talk suppression, the tested turn-on switching loss may become larger as the junction temperature increases.

2.3 Approaches for Switching Performance Improvement of Power Devices

Generally, there are two approaches for switching performance improvement, one is the gate driver, including active gate driver which depends on the online detection of the switching behavior to actively tune gate driving capability and intelligent gate driver which bases on the understanding of inherent characteristics of power devices to offline preset different gate drive output under different switching states; the other is the passive solution, including layout design and packaging optimization for parasitics minimization.

2.3.1 Gate Driver

Originally for high voltage Si IGBTs, the active gate driver was designed to deal with the conflicting requirements of the optimal switching performance, such as to achieve fast switching speed, minimized switching losses, as well as electromagnetic interference noise suppression and the switch stress limitation. This optimal switching performance cannot be realized simultaneously by conventional gate driver circuits with fixed gate voltage and resistor [71]. Generally, to actively control gate voltage or regulate gate loop impedance under different switching subintervals (e.g., *di/dt* transient, *dv/dt* transient) are the main strategies for active gate driver. Either the gate voltage control or gate loop impedance regulation, as a matter of fact, is to tune the gate current in real time to achieve the function of active gate drivers. Thus, gate current injection is also a popular terminology in related studies [71-79].

For high voltage Si IGBTs, in order to separately control the gate current during different switching subintervals, a feedback control with a sensor is usually employed. This sensor is used

to identify different switching subintervals. For example, in [75-77], Miller plateau is detected by a phase-locked loop to distinguish the *dv/dt* transient. Moreover, the voltage across the Kelvin emitter inductance is monitored to identify *di/dt* transient (Fig. 2-17) [71]. The feedback control is implemented by high bandwidth analog circuits with small signal transistors. Also, digital approach is another option. Recently, there have been several research efforts on using FPGA with high-speed high-resolution D/A and A/D conversion [80, 81].

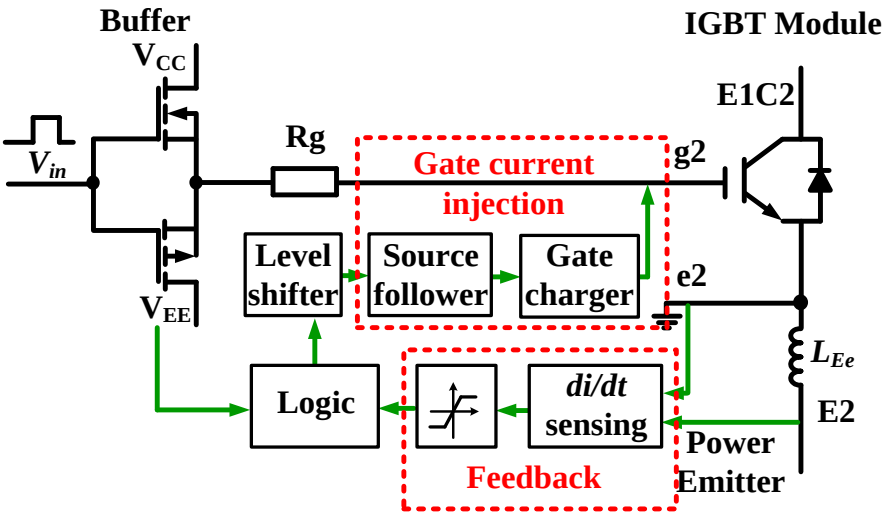


Fig. 2-17. Typical active gate driver diagram for IGBT module [71].

As compared to traditional Si IGBTs with slow switching speed, the fast switching SiC devices make the implementation of active gate driver more difficult for the following reasons, although the concept of conventional active gate driving scheme is still applicable. First, considering the switching time for SiC devices is as short as tens of nanoseconds, the feedback control becomes not feasible since the propagation delay induced by analog circuits or digital micro-controller may be comparable, even longer than the switching time. Second, the fast switching is always along with serious parasitic ringing so that any sensor that attempts to

identify different switching subintervals based on certain electric parameters are easily interfered, resulting in improper operation. In the end, based on today's technology, the traditional active gate driver with feedback control, which can best serve Si IGBTs, is not suitable for SiC devices. Currently for fast switching WBG devices, the proposed gate driver circuits bases on the intelligent gate driving shcemes with feedforward control and focuses on addressing unique challenges due to the inherent properties of these emerging power devices [39, 82-89].

For example, for normally-off SiC JFETs, the gate is not insulated from the channel by an oxide as MOSFETs, but forms a pn-junction with drain and source terminals, it is therefore required to inject hundreds of milli-amperes gate-source current during the on-state. On the other hand, during the switching transient, the gate driver should sink/source several amperes peak gate current to achieve fast switching [86]. To meet the different requirements for turn-on and turn-off switching transients on one hand and the steady on-state on the other hand, a special consideration should be taken into the design of gate drivers. [39] introduce a two-stage gate driver scheme: one stage supplies a short pulse with high gate voltage during the switching transient and a second stage delivers the dc current from the same supply voltage rail via a relatively large resistor during on-state. In addition, an ac-coupled gate driver is proposed to reduce the complexity of the two-stage gate drivers, where the supply voltage is fed through a capacitor to the gate during the turn-on and turn-off transient and through a resistor during the on-state to address different driving requirements [89].

For enhance mode GaN power transistors, as compared to their Si counterparts, they have similar V-I curve in the 1^{st} quadrant. However, in the 3^{rd} quadrant, they are totally different, which leads to significant power loss during dead-time. To cope with this issue and improve the efficiency of power conversion, some researchers develop a three-level driving method which is

capable of outputting three different gate voltages under off-state, on-state and dead-time interval [85, 87]. In addition, considering a limited gate voltage ratings of enhance mode GaN power transistors (e.g., 0 V – 6 V for EPC GaN), a dedicated gate driver IC LM5113 released by Texas Instrument integrates an auxiliary circuit to clamp the output voltage within a safe boundary [90].

Additionally, as the switching speed of power devices continuously increases, especially for WBG power devices, *dv/dt* induced spurious turn-on in a phase-leg configuration becomes common and more attention is given on this phenomenon. Several gate assist circuits are designed to address this issue for different types of power devices, including Si MOSFETs, SiC JFETs, and MOSFETs [83, 88, 91].

2.3.2 Layout Optimization and Packaging Techniques

As discussed in 2.2.2, parasitics more or less limit the switching speed of power device. Thus, parasitics minimization is another important aspect for switching performance improvement. In this section, the parasitics are categorized into two types: one is power device related parasitics, including gate-source capacitance, drain-source capacitance, Miller capacitance, and internal gate resistance; the other is interconnection related parasitics, primarily including three parasitic inductances, such as gate loop inductance, power loop inductance, and common source inductance. As a user of power devices, we have to accept power device related parasitics, and try our best to avoid adding additional equivalent parasitics externally, especially for Miller capacitance due to its high sensitivity on the switching performance. Furthermore, interconnection related parasitics should be minimized as small as possible.

Fig. 2-18 shows the distribution of interconnection related parasitics in the phase-leg configuration, including bonding wire and lead related parasitics inductance from package, PCB

trace induced inductance and equivalent series inductance (ESL) of capacitors [92, 93]. As can be observed, common source inductance is mainly contributed by the device package; gate loop inductance comes from the package together with the PCB trace; and power loop inductance involves all the parts of interconnection, consisting of package, PCB trace and ESL of capacitors.

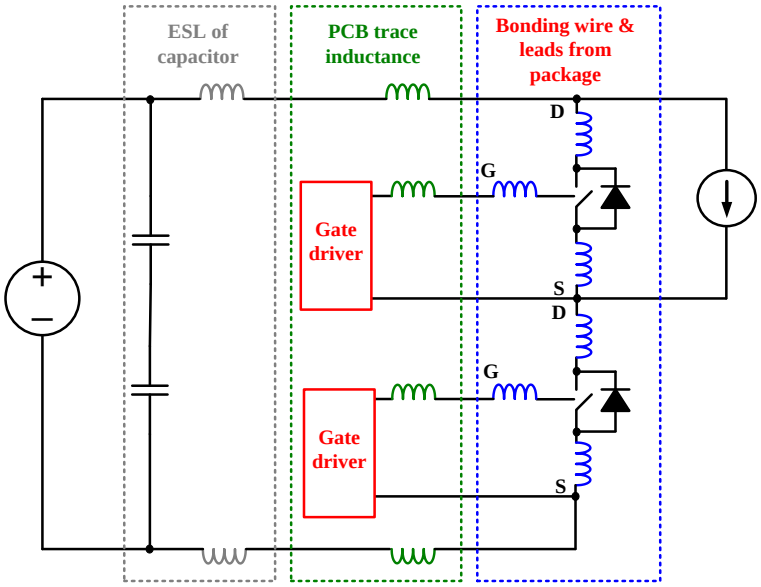
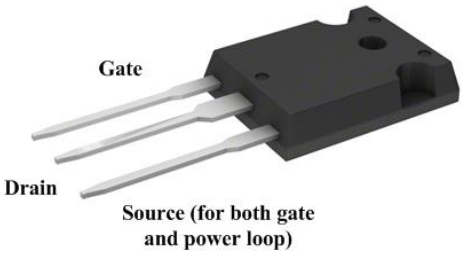


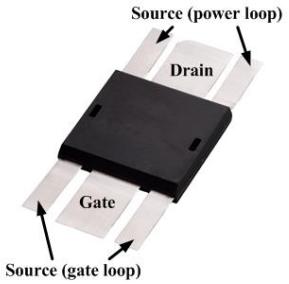
Fig. 2-18. Distribution of interconnection parasitics.

To minimize common source inductance, the improvement of packaging technique is critical. The SiC devices are mainly used in the voltage range up to 900 V; and GaN transistors with 600 V breakdown voltage become popular. In these voltage ratings, clearance and Creepage distance requirements must be considered. For this reason, the most popular packages are industry standard TO-series, such as TO-220, TO-247, TO-3P and TO-263 [94]. These packages with three leads make the lead associated with source terminal of devices involve in both gate and power loops, resulting in an inevitable common source inductance, as shown in Fig. 2-19(a). To cope with this issue, several advanced packaging techniques are developed, such as DE-series

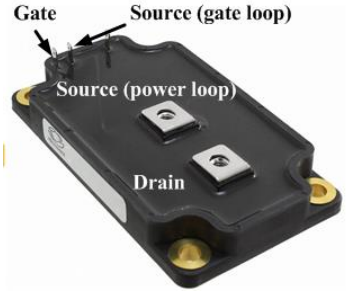
package and power module [95]. These packages introduce two source terminals, one for the gate loop and the other for power loop. Therefore, the coupling between gate and power loop induced by bonding wire and lead is significantly minimized.



(a) TO-series package.



(b) DE-series package.



(c) Power module.

Fig. 2-19. Power devices with different package.

To minimize gate loop inductance, gate driver and gate resistance must be placed as close as possible to the gate pin of power devices. Also, a ferrite bead is suggested to add in the gate loop to increase the gate loop resistance at high frequency (tens of MHz to hundreds of MHz) for the gate loop oscillation mitigation due to the gate loop inductance, but with little influence on the low frequency gate loop impedance, since the impedance characteristics of ferrite bead are frequency dependent [94].

To minimize power loop inductance, in addition to packages, PCB layout design, dc capacitor selection and placement are also important. First, for the packaging technology, TO-series package is replaced by Power Quad Flat No-Lead (PQFN) package to eliminate the lead induced parasitic inductance [96]. Even better, the stack-die package reduces some internal critical bonding wires, which is beneficial for multi-chip based package, such as cascade GaN device [97]. Also, to employ P-cell and N-cell concept for the layout design of Direct Bonded Copper (DBC) substrate can further decrease the power loop inductance inside the module [98]. In addition, the planar power module, featuring a symmetric sandwiched substrate-switches-substrate structure, is able to significant minimize the parasitic inductance induced by package [99, 100]. Second, for the PCB layout, the magnetic field cancellation can be used as a concept to minimize PCB trace induced parasitic inductance. This layout design is not limited in lateral plane or vertical plane. The internal layer can be utilized to create a more flexible option of layout design [101]. Moreover, for the discrete power device based PCB layout, the aforementioned P-cell and N-cell concept is also applicable [102]. Third, for dc capacitors, it is recommended to place amount of ceramic capacitors as close as possible to the phase-legs. These ceramic capacitors with small ESL would greatly suppress the parasitic ringing and reduce over-voltage [103]. Also, the idea of magnetic field cancellation can be used as a guideline for the placement of dc capacitors [92, 93].

2.4 Summary

This chapter reviews three areas that are closely related to switching performance of power devices.

First, a widely-accepted methodology of switching performance characterization is reviewed from three aspects: high-speed measurement, probes attachment induced issue, and data process.

For high-speed measurement, the selection criteria of measurement system bandwidth for switching waveform, pros and cons of different types of switching voltage and current measurement techniques are summarized. Also, the probes induced grounding-lead issue is discussed and the probe-tip adapter is considered as the recommended solution. Finally, the practical method of data processing is presented.

Second, the limitations and impact factors of switching performance in voltage source converter are discussed from three aspects: gate driver circuit, parasitics, and operating conditions. For gate driver circuit, the gate driver IC is the dominant factor to impact the switching behavior. Specifically, the pull-up (-down) resistance of gate driver, rise (fall) time, and amplitude of gate driver output voltage determine the gate driver capability, and then affect the power device switching speed. Meanwhile, under different operating conditions, the roles of these parameters on switching speed are different. Additionally, the common mode noise immunity capability of signal isolator and isolated power supply is identified as a limit factor of the switching speed, especially for the fast switching WBG devices. For parasitics, the mutual parasitics, including common source inductance and Miller capacitance, serve as negative feedbacks from the power loop to the gate loop due to *di/dt* and *dv/dt*, leading to slower switching speed. Also, parasitics in power loop are the crucial contributor to parasitic ringing and overshoot voltage, causing EMI and reliability issues. For operating conditions, higher junction temperature accelerates the turn-on switching speed of SiC devices but slow down their turn-off transition. In the end, the total switching loss stays nearly the same under different temperatures. Also, the reverse recovery characteristics of the SiC devices' body diode and cross-talk become worse as the junction temperature increases.

Third, the state-of-art approaches for switching performance improvement of power devices are introduced, including gate driver and interconnection optimization. For active/intelligent gate driver, gate voltage control and gate loop impedance regulation are the two primary methods to adjust gate driving capability for switching performance optimization. Currently proposed gate driving schemes for WBG devices mainly focus on addressing unique challenges due to the inherent properties of these emerging power devices. Considering their fast switching speed, the feedforward control is suitable as compared to feedback control for traditional Si devices. For the interconnection optimization, several packaging techniques and their characteristics are summarized, such as TO-series, DE-series, QPFN, and stack-die. Also, the concepts of P-cell and N-cell, as well as magnetic field cancellation are introduced for the optimization of PCB layout design.

3 Methodology for Switching Performance Characterization of SiC Devices

Double pulse tester (DPT) is a widely accepted method to evaluate the switching behavior of power devices, including SiC devices. This chapter summarizes the key issues of DPT so that it is capable of assessing the fast dynamic characteristics of SiC devices with high fidelity. First, the design criteria of double pulse tester's main components, including load inductor, dc capacitor bank, gate driver circuits are introduced. Also, the guidelines for physical layout of a DPT board are described. Second, high-speed measurement issues are discussed, including switching voltage/current detection and voltage-current alignment. Among them, special attention is given on the voltage-current alignment since the tested switching loss is greatly sensitive on the voltage-current alignment. Also, the latest techniques for high-speed voltage and current measurement and the corresponding models of probes are summarized. Third, the impact of probes induced grounding effects on the measurement of switching waveforms is illustrated. Fourth, the impact of parasitic ringing on switching loss is analyzed as a fundamental knowledge for the switching data processing. Finally, a practical method is introduced to accurately evaluate the switching loss of SiC devices with the consideration of parasitic ringing, cross-talk in a phase-leg, as well as voltage-current alignment.

3.1 Design Criteria of Components and Layout for Double Pulse Tester

As shown in Fig. 2-1(a), in addition to device under test (DUT), the double pulse tester primarily consists of load inductor, dc capacitor, and gate driver circuits. The design of these components and their physical interconnection significantly affect the switching behavior of DUT.

3.1.1 Components Design Criteria

Load inductor is to establish the desired inductive current during the first pulse and enable this inductive current stays nearly constant during the upcoming turn–off/–on transients. Therefore, the selected load inductance L should be large enough so as to limit the inductive current variation ΔI_L during the switching transient, yielding

$$L \geq \frac{V_{DC}}{\Delta I_L} t_{sw} = \frac{V_{DC}}{k_{\Delta I_L} \times I_L} t_{sw} \tag{3-1}$$

where t_{sw} is the switching time, of which the preliminary data can be obtained from device's datasheet, $k_{\Delta IL}$ indicates the current ripple coefficient, which practically is selected to be 1% ~ 5%, V_{DC} and I_L refer to the operating voltage and current. Usually, the switching performance of DUT is characterized under several different operating points. According to (3-1), the worst condition for the load inductance selection is under the maximum operating voltage and minimum current. In addition, it is preferred to construct the load inductor by connecting several equivalent small inductors in series. Each inductor has only one layer of windings to minimize its equivalent parallel capacitance (EPC). For WBG devices with fast switching-speed and high sensitivity on parasitics, load inductor's EPC minimization is critical.

Dc capacitor is employed to support a stable dc bus voltage in the DPT board. One group of capacitors with large capacitance supplies energy during the 1st pulse interval to establish the inductive current; while the other group of decoupling capacitors with high current capability and minimum equivalent series resistance is responsible for the transient current during the switching transition.

The capacitance of the bulky capacitors C_{bulky} is selected to limit the dc bus voltage variation ΔV_{DC} when the energy transfers from C_{bulky} to L during the 1st pulse, that is

$$C_{bulky} \geq \frac{LI_L{}^2}{(2V_{DC}-\Delta V_{DC})\Delta V_{DC}} = \frac{LI_L{}^2}{(2-k_{\Delta VDC})k_{\Delta VDC}V_{DC}{}^2} \approx \frac{LI_L{}^2}{2k_{\Delta VDC}V_{DC}{}^2} \quad (3\text{-}2)$$

where $k_{\Delta VDC}$ indicates the voltage ripple coefficient, which practically is selected to be 1% ~ 5%. Unlike the load inductance, the worst condition for bulk capacitance selection is under the minimum operating voltage and maximum current. Generally, electrolytic or film capacitors are preferred for the bulky capacitors bank.

The capacitance of the decoupling capacitors C_{dec} is selected to provide transient current and mitigate over-voltage during the switching transient. According to [103, 104], practically, C_{dec} is designed by

$$C_{dec} > 250 \times C_{oss} \quad (3\text{-}3)$$

where C_{oss} is the output capacitance of the DUT. Usually, ceramic capacitors are recommended for decoupling capacitors.

Gate driver circuits are another crucial component to double pulse tester and have been extensively investigated [52, 105]. Their detailed design criteria will not be repeated in this section.

3.1.2 Layout Design Considerations

The purpose of DPT is to grasp the experimental data of power devices in a simplified DPT board to evaluate their switching behaviors in the actual power converter. Therefore, the prior guideline of the layout design is the universality of the physical layout from the DPT to the future converters. And then, the parasitics minimization is considered.

To easily leverage the layout design of the DPT to future converters, it is preferred to separate the power stage and gate driver and modularize the gate driver with power devices. One

power stage mother board and two gate driver daughter boards integrated with power devices can be designed for DPT. In this way, we can utilize a uniform gate driver layout design for the future converters regardless of the specific topologies.

Parasitics minimization is the other critical consideration for the layout design. As shown in Fig. 3-1, there are mainly six parasitics in the DPT, including parasitics in the gate loop, L_{gs} and C_{gs}, parasitics in the power loop L_{ds} and C_{ds}, as well as mutual parasitics shared in both gate and power loop, L_{cm} and C_{gd} [35, 59-63]. Among them, power loop inductance L_{ds}, common source inductance L_{cm} and Miller capacitance C_{gd} significantly impact the switching performance of power devices, especially for the fast switching SiC devices.

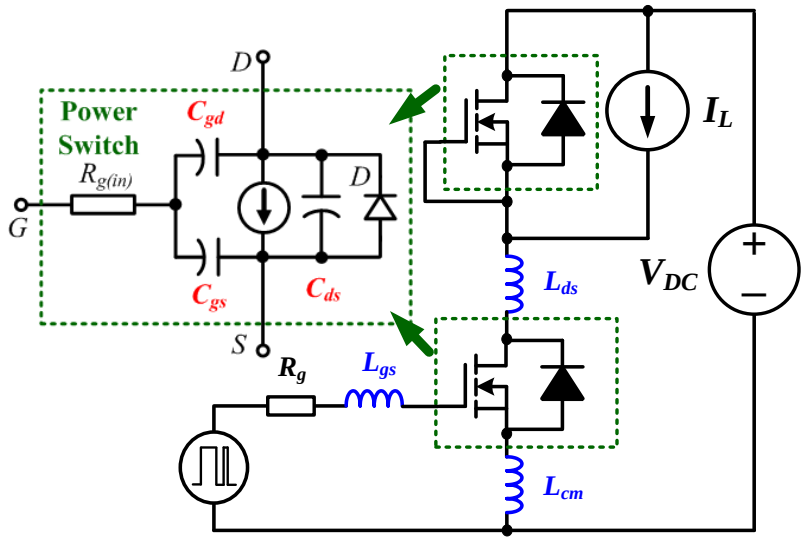


Fig. 3-1. Six parasitics in DPT board.

Power loop inductance L_{ds} is the crucial contributor to the parasitic ringing and overshoot voltage, causing EMI and reliability issues [35]. Magnetic field cancellation technique and P-cell N-Cell concept can effectively mitigate the parasitic inductance for the PCB layout design [92,

93, 101]. In addition, the mutual parasitics L_{cm} and C_{gd} serve as negative feedbacks from the power loop to the gate loop due to *di/dt* and *dv/dt*, leading to slower switching speed and more switching losses [5].

Modularized design of gate driver with power devices is recommended for L_{cm} and C_{gd} minimization. Taking one SiC MOSFET with TO−247 package as an example, a practical example of the layout design is shown in Fig. 3-2. Separated from the power loop on the mother board, a standalone gate drive daughter board is designed for a discrete power device. Kelvin gate connection with separate source return path is achieved to minimize L_{cm}. Meanwhile, integrated with the gate drive board, the power device has only source and drain terminals connected with the mother board, so that the parasitics between drain and gate terminals can be eliminated to avoid additional impact on C_{gd}. Overall, this modularized design effectively suppresses the impact of layout-induced parasitics, and can be simply leveraged to the actual power converter.

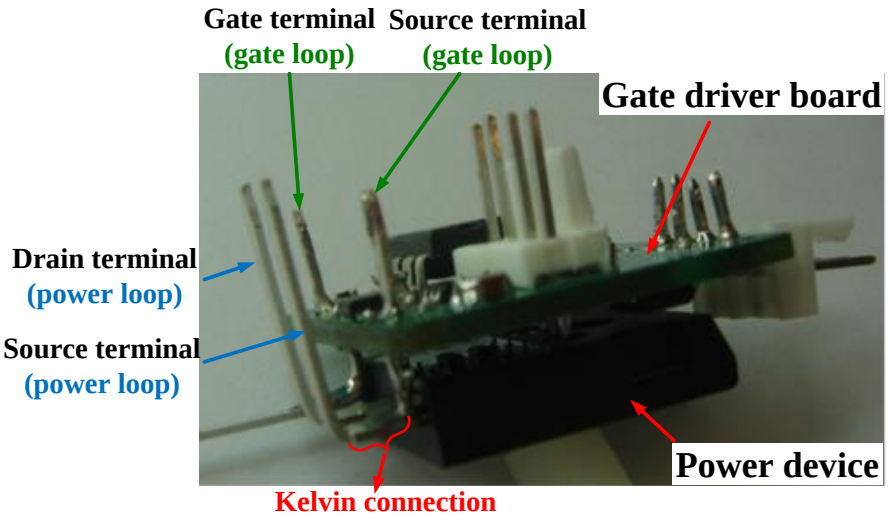


Fig. 3-2. Modularized design for DPT layout.

3.2 High-speed Measurement Issues

The fundamentals of high-speed measurement have been reviewed in Section 2.1.1. This section summarizes the latest techniques for high-speed voltage and current measurement and the corresponding models of probes. Also, the voltage-current alignment is highlighted.

Traditionally, the switching characterization of power devices basically includes three waveforms, i.e., gate-source voltage v_{gs}, drain-source voltage v_{ds}, and drain current i_d, as displayed in Fig. 2-1(b) [35, 40]. Among them, v_{ds} and i_d are two key waveforms, which indicate switching characterization, such as switching time, *di/dt*, *dv/dt* and switching losses.

3.2.1 Voltage Measurement

Table 3-1 summarizes the latest voltage probes for 600/1200 V SiC devices, including their models, specifications and characteristics. The passive probes are preferred due to their higher bandwidth and dynamic range.

Table 3-1. Latest Voltage Probes for V_{DS} Measurement [42, 43]

Types	Models	Maximum voltage	Bandwidth	Rise time	Pros	Cons
Differ-ential probes	THDP0200	± 1600 V	200 MHz	8.75 ns	Galvanic isolation	Limited bandwidth, longer connection leads to device
	TMDP0200	± 750 V	200 MHz	8.75 ns		
Passive probes	P5150	2,500 V	500 MHz	3.50 ns	High bandwidth	Non-galvanic isolation
	TPP0850	2,500 V	800 MHz	2.19 ns		

3.2.2 Current Measurement

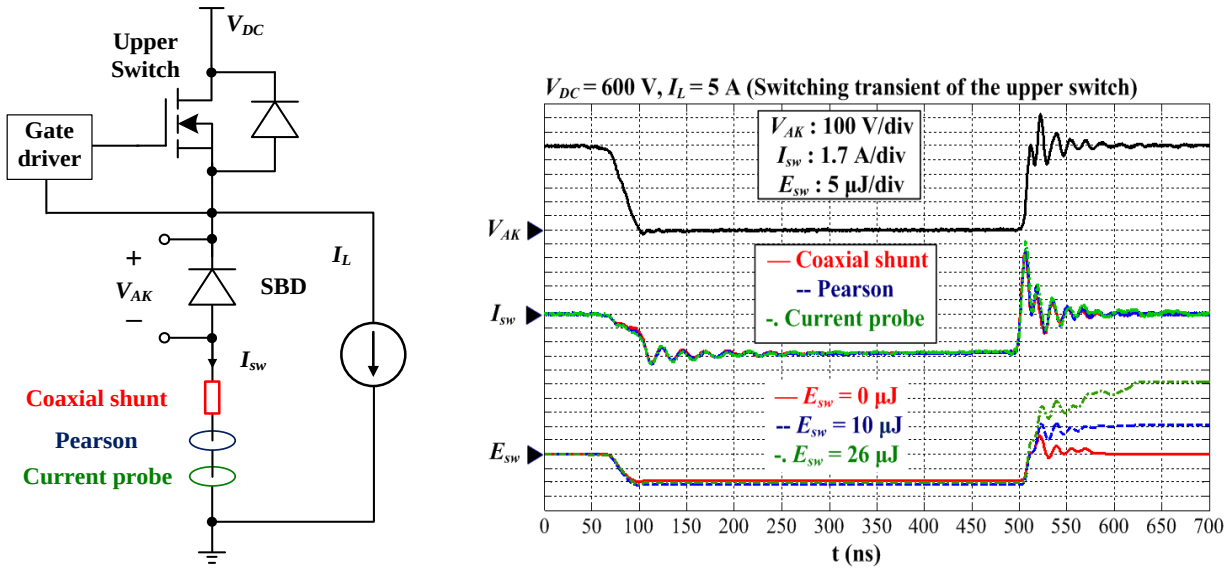
Table 3-2 summarizes the characteristics and state-of-art models of four current measurement techniques for i_d measurement, including coaxial shunt, current transformer, split core current probe, and Rogowski coil. Due to the limited bandwidth, Rogowski coil is not a suitable current sensor for switching current measurement.

Table 3-2. Four Current Measurement Techniques [45-48]

Types/Models	Current type	Bandwidth	Rise time	Pros	Cons
Coaxial shunt SSDN-10	dc/ac	2,000 MHz	0.88 ns	High bandwidth, high accuracy	Non-galvanic isolation, non-continuous operation
Current transformer Pearson 2877	ac	200 MHz	8.75 ns	High bandwidth, galvanic isolation	Saturation for large current, non-continuous operation
Split core current probe TCP0030A	dc/ac	120 MHz	14.58 ns	Galvanic isolation, continuous operation	Low accuracy, limited bandwidth
Rogowski Coil CWT Mini	ac	17 MHz	102.9 ns	Galvanic isolation	Low bandwidth and accuracy

In addition to the bandwidth, high accuracy is another criterion for the transient current measurement. A comparison test with Cree CMF20120D SiC MOSFETs and C2D10120D SiC Schottky barrier diode (SBD) is conducted to assess the measurement accuracy of coaxial shunt, current transformer, and split core current probe, as shown in Fig. 3-3(a). During the switching

transient of the upper switch, the switching waveforms of the lower side SBD are monitored. The switching current through SBD is measured by coaxial shunt, Pearson current transformer, and split core current probe listed in Table 3-2. Due to the excellent reverse recovery characteristics of SBD, theoretically, the switching losses of SBD should be zero. Fig. 3-3(b) displays the switching waveforms and losses of SBD during the switching transient of the upper MOSFET. It shows that the switching current I_{sw} measured by different current measurement techniques seems to be identical, but their corresponding switching losses are different. The accuracy of the switching current measured by coaxial shunt is the highest since its switching losses approach zero, while the error of the switching losses measured by the split core current probe is largest. Thus, the split core current probe has the lowest accuracy.



(a) Test circuit. (b) Switching waveforms of SBD.

Fig. 3-3. Accuracy evaluation of different current measurement techniques.

Also, to measure the switching current, every current measurement techniques will induce additional parasitic inductance in the power loop, which worsens the switching behaviors of the DUT. This negative effect is more serious for the fast WBG power devices with small PCB footprints, such as EPC GaN transistors, since the excessive parasitic inductance induced by inserting switching current sensors occupies large portion of the total power loop inductance. Therefore, the test results from DPT cannot accurately represent the switching performance of the DUT in the actual converter. To mitigate this issue, a customized current shunt was developed with tens of 1 Ω resistors with 0201 package in parallel to minimize the dimensions of the shunt and its induced parasitic inductance [36, 106].

3.2.3 Voltage-Current (V-I) Alignment

Each of the voltage and current probes has its own characteristic propagation delay. The difference in these two delays, known as skew, will cause serious timing misalignment, eventually leading to the inaccurate switching loss evaluation, especially for the fast switching SiC devices.

Fig. 3-4 shows the sensitivity of V−I timing misalignment on switching losses of both the lower and upper switches (i.e., E_{sw_L} and E_{sw_H}) in a phase-leg under the operating condition of 600-V/10-A with 2-Ω gate resistance. It shows that 1 ns V−I timing misalignment causes 272 μJ error for E_{sw_H} and -75μJ error for E_{sw_L}, which is comparable to the real switching losses (see Fig. 3-4). More experimental data under different gate resistance are summarized in Table 3-3. Thus, V−I alignment significantly affects the accuracy of the switching losses evaluation for SiC devices.

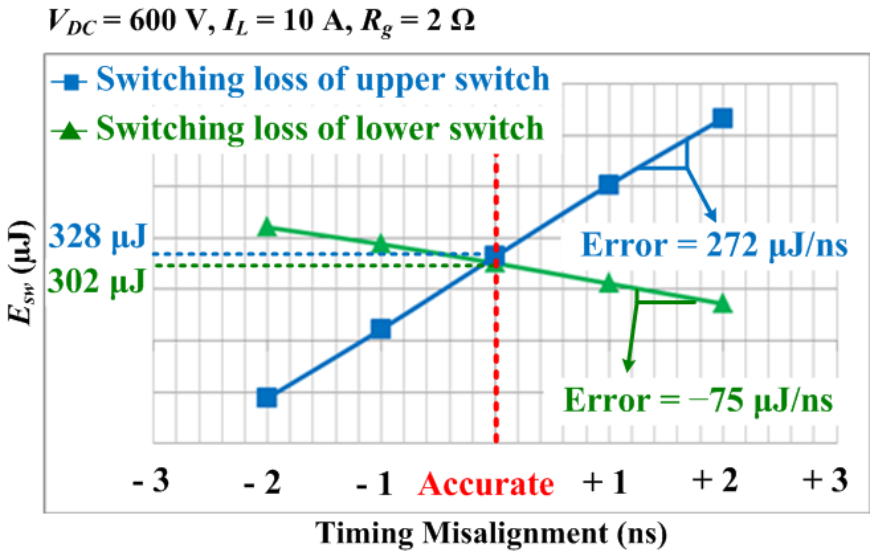


Fig. 3-4. Sensitivity of V−I alignment.

Table 3-3. Sensitivity of V-I Alignment on Switching Losses

R_g (Ω)	10	5	2
E_{sw_L} (µJ/ns)	26	132	272
E_{sw_H} (µJ/ns)	-16	-47	-75

Based on more test results, there are several tips:

1) For the active probes, such as differential voltage probe and current probe, the propagation delay under different measurement range is different. Taking THDP0200 differential voltage probe as an example, the difference of delay between 150 V dynamic range and 1500 V dynamic range is around 1 ns. Therefore, instead of low dynamic range, the active probes should be deskewed under the high dynamic range.

2) For the coaxial shunt, in addition to the delay induced by coaxial cable, shunt itself will incur delay. For instance, with the same coaxial cable, the delay of SSDN-10 shunt is around 1.4 ns shorter than that of SSDN-015.

3) For probes of the same model, the propagation delays still have slight difference. Hence, every probe needs to be calibrated before measurement.

There are three methods for the V−I alignment:

1) Adopt the power measurement deskew and calibration fixture [107]. This method is convenient, but less compatible due to the connector constraints. Only current probes from Tektronix can be deskewed with this fixture. Also, its maximum allowable voltage is 8 V RMS, which is not suitable for the calibration of the active probes because the low input voltage can be hardly measured by probes under the high dynamic range.

2) Use the probe compensation output of the scope as a standard square waveform signal source for V−I alignment [35]. In addition to the low input voltage (~ 2.5 V), another issue of this method is that only a coaxial cable rather than the combination of coaxial cable and shunt is deskewed, which will induce timing misalignment in the switching current measurement.

3) Remove the inductor in DPT and replace one device with a low inductance 100 Ω resistor [38]. Based on this resistive DPT, the voltage across a pure resistor is just 100x of the current through it with negligible phase shift induced by the extremely small ratio between series inductance and resistance (~ 50 ps in practical). The maximum input voltage is determined by the resistor, usually several hundred volts. This method for V−I alignment is preferred.

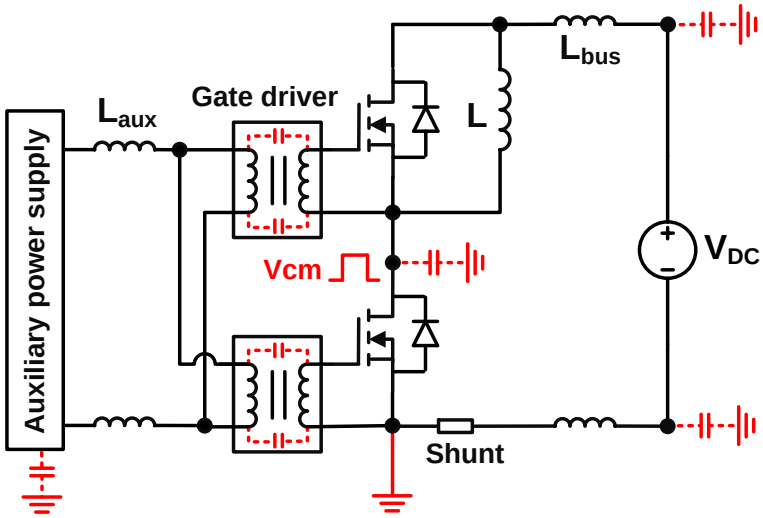
3.3 Probes Induced Grounding Effects

Considering the bandwidth, dynamic range, and measurement accuracy, high voltage passive probe and coaxial shunt have better performance for switching voltage and current measurement. However, the negative terminals of both probes input to the oscilloscope are common and tied to the earth ground. This grounding effects induced by probes will impact the measurement of switching waveforms.

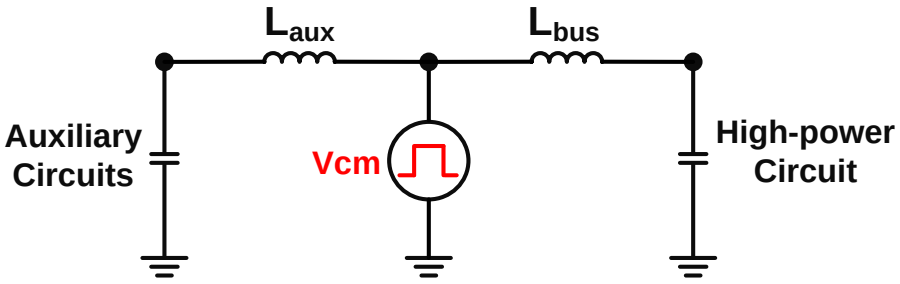
Fig. 3-5 illustrates DPT setup considering the earth ground. The negative terminal of probes enables the source terminal of the lower switch to share the same potential of the earth ground. Also, dc power supplies, including main dc bus voltage source and auxiliary power supply are connected to the test-bed by long wires, leading to non-ignorable parasitic inductance (L_{aux} and L_{bus}). Their output terminals create a significant capacitive coupling to the earth ground due to the copper foil for windings of the isolation transformer, which is used in many power supplies. Therefore, during the switching transient, high *dv/dt* (i.e., the slew rate of drain-source voltage) causes common-mode noise via the parasitic inductance and capacitance in the capacitively coupled ground loop. This common-mode current flows into the earth ground of oscilloscope, resulting in a common-mode current ringing in the measured switching current i_d, as shown in Fig. 3-6.

To alleviate this issue, common-mode chokes with high impedance at the common-mode ringing frequency can be employed at both main dc voltage source and auxiliary power supply, as shown in Fig. 3-7. In this way, very small common-mode current will flow through the capacitance to the ground due to the high impedance induced by chokes [40]. In addition, a more convenient solution is to float the ground of oscilloscope, although it is not recommended considering the potential hazard to equipment and operator. With floated ground, the capacitively

coupled ground loop does not exist, and the corresponding common-mode current will be suppressed. Fig. 3-6 illustrates the comparison of the measured drain current during switching transient between different DPT setup. It shows that the low frequency ringing of drain current induced by grounding loop effects is suppressed by the means of floating scope ground and employing common-mode chokes.



(a) Capacitive coupled ground loop induced by passive probes.



(b) Simplified equivalent circuit.

Fig. 3-5. Capacitive coupled ground loop induced by DPT setup.

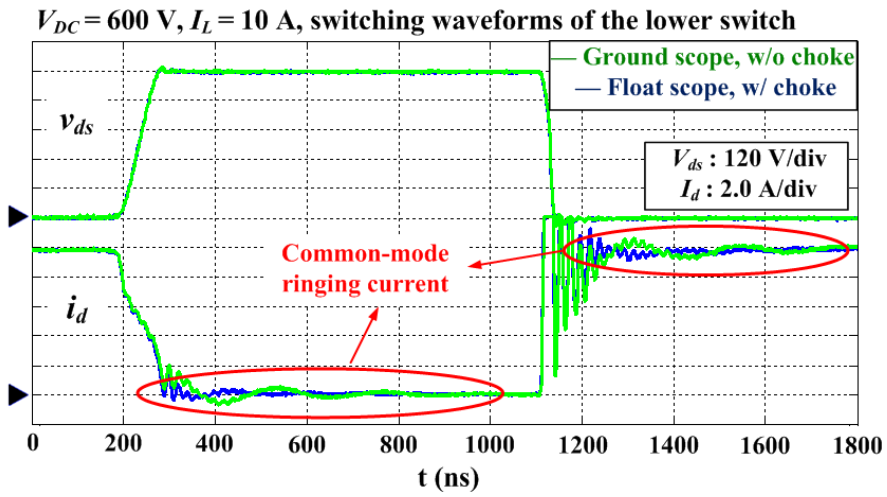


Fig. 3-6. Impact of capacitive coupled ground loop on drain current measurement.

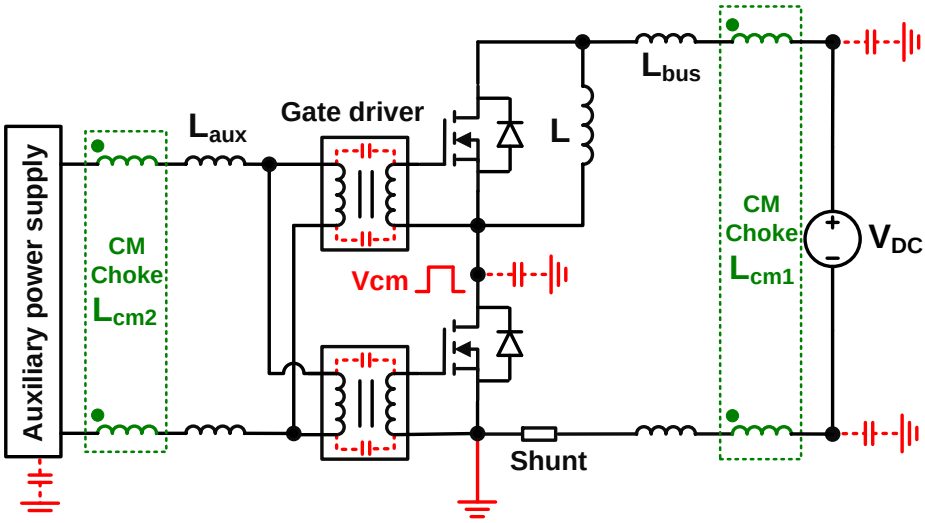


Fig. 3-7. DPT setup with common-mode (CM) chokes.

Also note that the grounding point in the double pulse circuit cannot be the middle point in a phase-leg since the voltage fluctuation is very large on this point and will cause large grounding current ringing. It is recommended to connect the negative terminal of the probes to the dc bus.

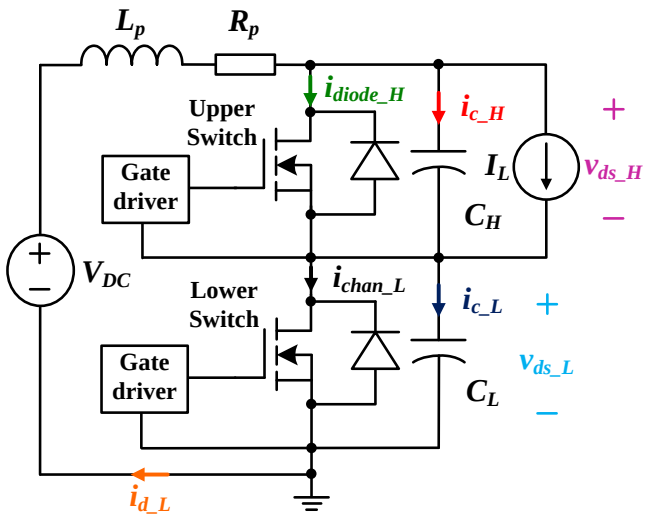


Fig. 3-8. Double pulse test circuit with consideration of stray resistance in the power loop.

3.4 Parasitic Ringing

During the much faster switching transient, the impact of parasitics on switching behavior becomes significantly intensified, leading to serious ringing, which can be commonly observed in the switching waveform. This parasitic ringing may contribute additional loss when it is damped. Thus, how to evaluate the parasitic ringing induced power dissipation becomes critical for the switching loss assessment of fast switching SiC devices. Therefore, the impact of parasitic ringing on switching losses is worth investigating.

A double pulse circuit is redrawn with the consideration of stray resistance in the switching loop, as shown in Fig. 3-8. According to the energy conservation, the total energy dissipated in the circuit during the switching transient can be assessed by calculating the difference among the input energy supplied by a dc source, the output energy stored in a load inductor, and the energy transferred among parasitics, yielding

$$E_{sw} = \int \left(V_{DC} i_{d\_L} - v_{ds\_H} I_L\right) dt \mp \frac{1}{2} L_p \Delta {I_{Lp}}^2 \mp \frac{1}{2} C_H \Delta {V_{c\_H}}^2 \pm \frac{1}{2} C_L \Delta {V_{c\_L}}^2 \qquad (3\text{-}4)$$

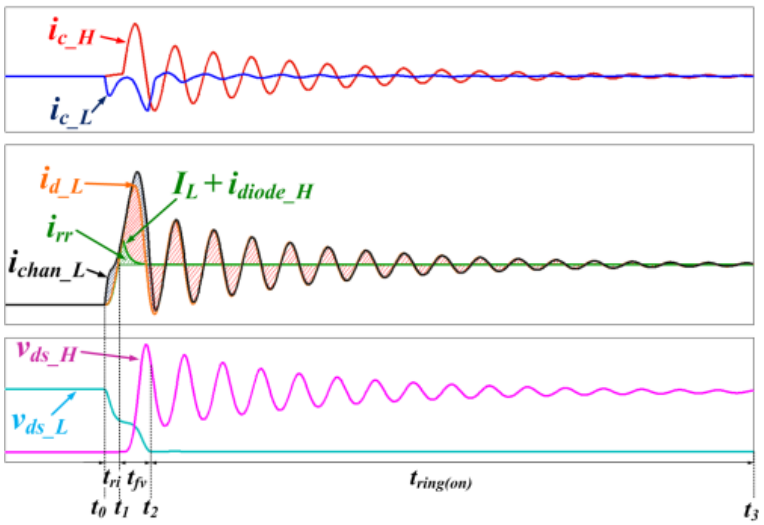
where E_{sw} refers to the total energy dissipated in the circuit, V_{DC}, v_{ds_H}, i_{d_L}, and I_L indicate the dc source output voltage, drain-source voltage of the upper switch (i.e., voltage across the load inductor), drain current of the lower switch (i.e, current through dc source) and inductive load current, respectively. L_p is the lumped parasitic inductance, of which the current difference between the initial and final values is expressed as ΔI_{Lp}. C_H and C_L are the equivalent output capacitances of the upper and lower switches, ΔV_{c_H} and ΔV_{c_L} represent their voltage variations during the switching transient. The signs of the latter three terms in (3-4) depend on the direction of energy transfer. Based on (3-4), in addition to the switching losses of power devices, the energy dissipated by stray resistance R_p is also covered to evaluate the ringing related switching losses more accurately. The lower switch in the phase-leg configuration is selected as the device under test.

3.4.1 Analytical Switching Loss Model for Ringing Loss Identification

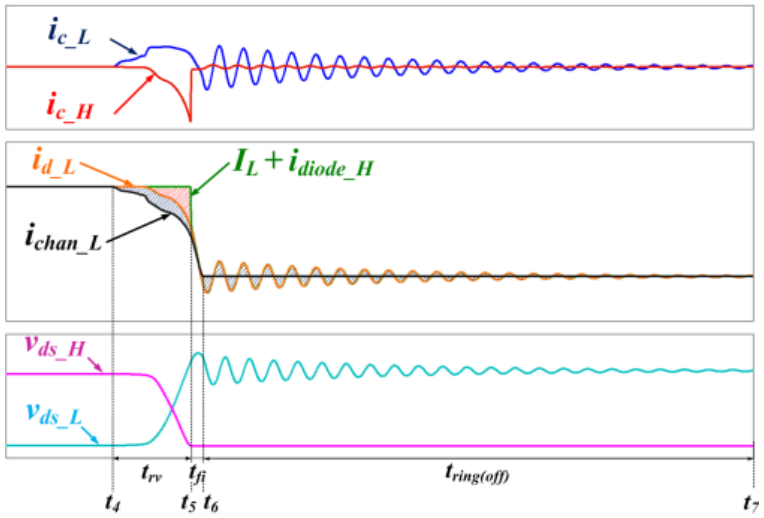
Fig. 3-9 displays the typical switching waveforms of SiC devices. The turn-on transient in Fig. 3-9(a) consists of three subintervals: 1) current rise subinterval t_{ri} from t_0 to t_1. At t_1, i_{d_L} increases to I_L; 2) voltage fall subinterval t_{fv} from t_1 to t_2. At t_2, v_{ds_L} drops to 0, the lower switch is in the ohmic region; 3) Ringing subinterval $t_{ring(on)}$ from t_2 to t_3. At t_3, ringing is damped, turn-on commutation process is completed.

Based on the aforementioned method, the input energy supplied by dc source $E_{dc(on)}$, the output energy stored in load inductor $E_{load(on)}$, and the energy transferred among parasitics $E_{p(on)}$ during the turn-on transient are given by (3-5) – (3-7) respectively, listed in Fig. 3-10, respectively. i_{chan_L} is the channel current of the lower switch, i_{rr} refers to the reverse recovery current, i_{c_L} and i_{c_H} indicate the displacement current from C_L and C_H. Q_{rr} is the reverse

recovery charge due to the upper freewheeling diode. V_{diode} is the forward voltage drop of the upper freewheeling diode, and $R_{ds(on)}$ refers to the on-resistance of the lower switch.



(a) Turn-on transient.



(b) Turn-off transient.

Fig. 3-9. Typical switching waveforms of SiC devices in a phase-leg.

$$E_{dc(on)} = \int_{t_0}^{t_3} V_{DC} i_{d\_L} dt = V_{DC} \int_{t_0}^{t_1} \left(i_{chan\_L} + i_{c\_L}\right) dt + V_{DC} \int_{t_1}^{t_3} \left(I_L + i_{rr} + i_{c\_H}\right) dt$$

$$= V_{DC} \int_{t_0}^{t_1} i_{chan\_L} dt - C_L V_{DC} \left(V_{DC} - v_{ds\_L}(t_1)\right) + V_{DC} I_L \left(t_{fv} + t_{ring(on)}\right) + V_{DC} Q_{rr} + C_H {V_{DC}}^2$$

(3-5)

$$E_{load(on)} = \int_{t_0}^{t_3} v_{ds\_H} I_L dt = I_L \int_{t_0}^{t_1} -V_{diode} dt + I_L \int_{t_1}^{t_3} \left(V_{DC} - L_p \frac{di_{ds\_L}}{dt} - R_p i_{ds\_L} - v_{ds\_L}\right) dt$$

$$= -I_L V_{diode} t_{ri} + I_L V_{DC} \left(t_{fv} + t_{ring(on)}\right) - R_p I_L \left(I_L t_{fv} + Q_{rr} + C_H V_{DC}\right)$$

$$-I_L \int_{t_1}^{t_2} v_{ds\_L} dt - C_H R_{ds(on)} I_L \left(V_{DC} - v_{ds\_H}(t_2)\right) - \left(R_{ds(on)} + R_p\right) {I_L}^2 t_{ring(on)}$$

(3-6)

$$E_{p(on)} = -\frac{1}{2} L_p {I_L}^2 - \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 \quad (3\text{-}7)$$

$$E_{tot(on)} = V_{DC} \int_{t_0}^{t_1} i_{chan\_L} dt + I_L \int_{t_1}^{t_2} v_{ds\_L} dt - C_L V_{DC} \left(V_{DC} - v_{ds\_L}(t_1)\right) + I_L V_{diode} t_{ri}$$

$$+ R_p {I_L}^2 t_{fv} + V_{DC} Q_{rr} - \frac{1}{2} L_p {I_L}^2 + \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 + R_p I_L (Q_{rr} + C_H V_{DC})$$

$$+ C_H R_{ds(on)} I_L \left(V_{DC} - v_{ds\_H}(t_2)\right) + \left(R_{ds(on)} + R_p\right) {I_L}^2 t_{ring(on)}$$

(3-8)

Fig. 3-10. Summary of turn-on switching loss calculations under normal operating conditions.

Thus, according to (3-4), the total energy loss during the turn-on transient is expressed as (3-8). The last term $\left(R_{ds(on)} + R_p\right) {I_L}^2 t_{ring(on)}$ in (3-8) is the conduction loss during the ringing subinterval, which should be removed for the switching loss assessment.

In addition, as shown in Fig. 3-9(b), the turn-off transient also contains three subintervals: 4) voltage rise subinterval t_{rv} from t_4 to t_5. At t_5, v_{ds_H} drops to 0; 5) current fall subinterval t_{fi} from t_5 to t_6. At t_6, i_{chan_L} drops to 0, the lower switch is in the cutoff region; 6) Ringing subinterval $t_{ring(off)}$ from t_6 to t_7. At t_7, ringing is damped, turn-off commutation is finished.

Similarly, the input energy supplied by dc source $E_{dc(off)}$, the output energy stored in load inductor $E_{load(off)}$, and the energy transferred among parasitics during the turn-off transient are given by (3-9) – (3-11) respectively, listed in Fig. 3-11.

Thus, the total energy loss during the turn-off transient is expressed as (3-12). The last term $I_L V_{diode} t_{ring(off)}$ in (3-12) indicates the conduction loss during the ringing subinterval, which should be removed from the switching loss calculation.

Consequently, the total energy loss $E_{sw(tot)}$ dissipated in the circuit is given by

$$E_{sw(tot)} = E_{sw(on)} + E_{rr} + E_{sw(off)} + E_{sw(ringing)} \tag{3-13}$$

where $E_{sw(on)}$ is the turn-on switching loss from t_0 to t_2 (shown in Fig. 3-9(a)), as in (3-14). E_{rr} refers to the reverse recovery induced switching energy dissipation, as in (3-15). $E_{sw(off)}$ indicates the turn-off switching losses from t_4 to t_6 (shown in Fig. 3-9(b)), as in (3-16). $E_{sw(ringing)}$ represents the switching losses during turn-on and turn-off ringing subintervals, which are considered as the energy dissipation contributed by damping parasitic ringing, as in (3-17). Rewritten (3-17), $E_{sw(ringing)}$ is expressed as

$$E_{sw(ringing)} = \frac{2R_{ds(on)}I_L}{V_{DC}}\left(1 - \frac{v_{ds\_H}(t_2)}{V_{DC}}\right)E_{c\_H} + 2\left(1 - \frac{v_{ds\_L}(t_5)}{V_{DC}}\right)E_{c\_L} \tag{3-18}$$

where $v_{ds\_H}(t_2)$ is the amplitude of v_{ds_H} when v_{ds_L} approaches 0 during the turn-on transient, $v_{ds\_L}(t_5)$ is the amplitude of v_{ds_L} when v_{ds_H} is equal to 0 during the turn-off transient, $E_{c\_H} =$

$C_H {V_{DC}}^2/2$, $E_{c\_L} = C_L {V_{DC}}^2/2$, corresponding to the energy stored in the output capacitance of upper and lower switches, respectively. Generally, E_{c_H} and E_{c_L} are small compared with $E_{sw(tot)}$. Considering $R_{ds(on)} I_L \ll V_{DC}$, the first term of (3-18) can be ignored. Also, due to the negative slew rate of i_{d_L} at t_5 during the turn-off transient, in Fig. 3-9(b), $v_{ds\_L}(t_5) = V_{DC} - L_p \, di_{d\_L}(t_5)/dt > V_{DC}$, so that the second term in (3-18) is always negative. Therefore, the impact of ringing on switching losses is not significant under normal operating conditions.

$$E_{dc(off)} = \int_{t_4}^{t_7} V_{DC} i_{d\_L} dt = V_{DC} \int_{t_4}^{t_5} \left(I_L - i_{c\_H}\right) dt + V_{DC} \int_{t_5}^{t_6} \left(i_{chan\_L} + i_{c\_L}\right) dt + V_{DC} \int_{t_6}^{t_7} i_{c\_L} dt$$

$$= V_{DC} I_L t_{rv} - C_H {V_{DC}}^2 + V_{DC} \int_{t_5}^{t_6} i_{chan\_L} dt + C_L V_{DC} \left(V_{DC} - v_{ds\_L}(t_5)\right) \quad (3\text{-}9)$$

$$E_{load(off)} = \int_{t_4}^{t_7} v_{ds\_H} I_L dt = I_L \int_{t_4}^{t_5} \left(V_{DC} - L_p \frac{di_{ds\_L}}{dt} - R_p i_{ds\_L} - v_{ds\_L}\right) dt + I_L \int_{t_5}^{t_7} -V_{diode} dt$$

$$= V_{DC} I_L t_{rv} + L_p I_L \left(I_L - i_{d\_L}(t_5)\right) - R_p I_L (I_L t_{rv} - C_H V_{DC}) - I_L \int_{t_4}^{t_5} v_{ds\_L} dt - I_L V_{diode} (t_{fi} + t_{ring(off)}) \quad (3\text{-}10)$$

$$E_{p(off)} = \frac{1}{2} L_p {I_L}^2 + \frac{1}{2} C_H {V_{DC}}^2 - \frac{1}{2} C_L {V_{DC}}^2 \quad (3\text{-}11)$$

$$E_{tot(off)} = I_L \int_{t_4}^{t_5} v_{ds\_L} dt + V_{DC} \int_{t_5}^{t_6} i_{chan\_L} dt - L_p I_L \left(I_L - i_{d\_L}(t_5)\right) + R_p {I_L}^2 t_{rv} + I_L V_{diode} t_{fi} + \frac{1}{2} L_p {I_L}^2 - \frac{1}{2} C_H {V_{DC}}^2 - \frac{1}{2} C_L {V_{DC}}^2 - R_p I_L C_H V_{DC} + C_L V_{DC} \left(V_{DC} - v_{ds\_L}(t_5)\right) + I_L V_{diode} t_{ring(off)} \quad (3\text{-}12)$$

Fig. 3-11. Summary of turn-off switching loss calculations under normal operating conditions.

$$E_{sw(on)} = V_{DC}\int_{t_0}^{t_1} i_{chan\_L}dt + I_L\int_{t_1}^{t_2} v_{ds\_L}dt + I_L V_{diode}t_{ri} + R_p {I_L}^2 t_{fv} - C_L V_{DC}\left(V_{DC} - v_{ds\_L}(t_1)\right) \quad (3\text{-}14)$$

$$E_{rr} = (V_{DC} + R_p I_L)Q_{rr} \quad (3\text{-}15)$$

$$E_{sw(off)} = I_L\int_{t_4}^{t_5} v_{ds\_L}dt + V_{DC}\int_{t_5}^{t_6} i_{chan\_L}dt + R_p {I_L}^2 t_{rv} + I_L V_{diode}t_{fi} - L_p I_L\left(I_L - i_{d\_L}(t_5)\right) \quad (3\text{-}16)$$

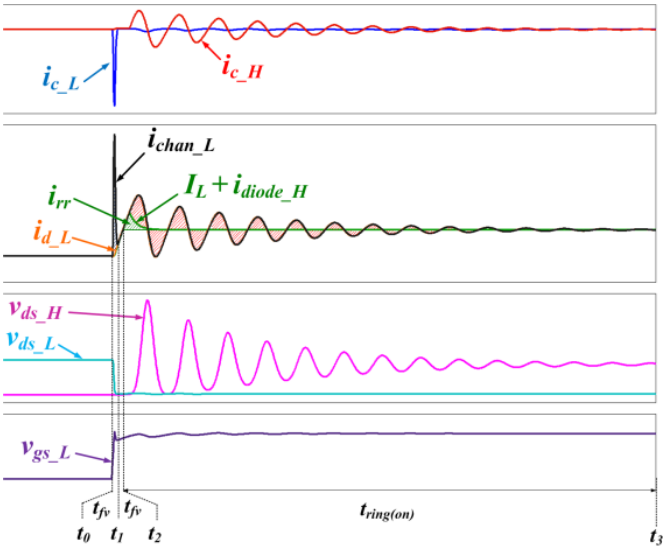
$$E_{sw(ringing)} = C_H R_{ds(on)} I_L\left(V_{DC} - v_{ds\_H}(t_2)\right) + C_L V_{DC}\left(V_{DC} - v_{ds\_L}(t_5)\right) \quad (3\text{-}17)$$

Fig. 3-12. Summary of total switching loss calculations under normal operating conditions.

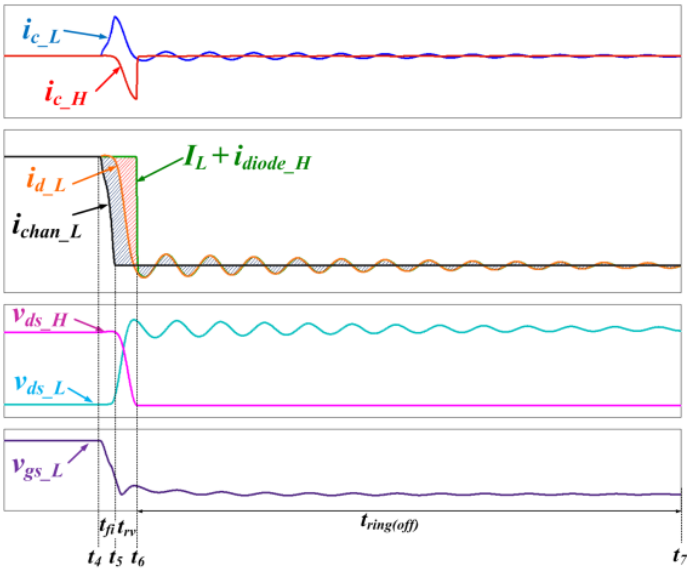
3.4.2 Ringing Losses under Extreme Operating Conditions

The aforementioned analysis is based on the typical switching waveforms displayed in Fig. 3-9. However, for the fast switching SiC devices, the switching behavior will be greatly changed under certain extreme operating conditions. For instance, under low dc voltage and large load current, during the turn-on transient, v_{ds_L} will drop to 0 at t_1 before i_{d_L} approaches I_L at t_2, as shown in Fig. 3-13(a). Also, under the high dc voltage and small load current case, i_{chan_L} will first become 0 at t_5 during the turn-off transient, and then, v_{ds_L} rises to V_{DC} at t_6, like the waveform shown in Fig. 3-13(b). Consequently, the switch state transitions under these operating conditions are much faster than the drain current and drain-source voltage commutation process. Taking the turn-on transient as an example, instead of t_2 in Fig. 3-9(a), the lower switch is in the ohmic region at t_1 under the operating condition shown in Fig. 3-13(a), such that the impact of

ringing on turn-on switching behavior becomes longer and more serious. So does the impact of ringing on turn-off switching behavior. It is therefore necessary to investigate the effect of ringing on switching losses under these extreme operating conditions.



(a) Turn-on transient.



(b) Turn-off transient.

Fig. 3-13. The switching waveforms of SiC devices under extreme operating conditions.

During the turn-on transient, the input energy supplied by dc source $E_{dc(on)}$, the output energy stored in load inductor $E_{load(on)}$, and the energy transferred among parasitics $E_{p(on)}$ under extreme operating conditions are given by (3-19) – (3-21), listed in Fig. 3-14, respectively.

$$E_{dc(on)\_extreme} = \int_{t_0}^{t_3} V_{DC} i_{d\_L} dt = V_{DC} \int_{t_0}^{t_2} i_{d\_L} dt + V_{DC} \int_{t_2}^{t_3} \left(I_L + i_{rr} + i_{c\_H}\right) dt =$$

$$V_{DC} \int_{t_0}^{t_2} i_{d\_L} dt + V_{DC} I_L t_{ring(on)} + V_{DC} Q_{rr} + C_H {V_{DC}}^2 \quad (3\text{-}19)$$

$$E_{load(on)\_extreme} = \int_{t_0}^{t_3} v_{ds\_H} I_L dt$$

$$= I_L \int_{t_0}^{t_2} -V_{diode} dt + I_L \int_{t_2}^{t_3} \left(V_{DC} - L_p \frac{di_{ds\_L}}{dt} - \left(R_p + R_{ds(on)}\right) i_{ds\_L}\right) dt$$

$$= -I_L V_{diode}(t_{fv} + t_{ri}) + I_L V_{DC} t_{ring(on)} - (R_p + R_{ds(on)}) I_L (Q_{rr} + C_H V_{DC}) - \left(R_p + R_{ds(on)}\right) {I_L}^2 t_{ring(on)} \quad (3\text{-}20)$$

$$E_{p(on)\_extreme} = -\frac{1}{2} L_p {I_L}^2 - \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 \quad (3\text{-}21)$$

$$E_{tot(on)\_extreme} =$$

$$V_{DC} \int_{t_0}^{t_2} i_{d\_L} dt - \frac{1}{2} L_p {I_L}^2 + \left(1 + \frac{\left(R_p + R_{ds(on)}\right) I_L}{V_{DC}}\right) V_{DC} Q_{rr} + \left(1 + \frac{2\left(R_p + R_{ds(on)}\right) I_L}{V_{DC}}\right) \frac{1}{2} C_H {V_{DC}}^2 +$$

$$\frac{1}{2} C_L {V_{DC}}^2 + I_L V_{diode}(t_{fv} + t_{ri}) + \left(R_{ds(on)} + R_p\right) {I_L}^2 t_{ring(on)} \quad (3\text{-}22)$$

Fig. 3-14. Summary of turn-on switching loss calculations under extreme operating conditions.

Thus, according to (3-4), the total energy loss during the turn-on transient under the extreme operating condition in Fig. 3-13(a) is given by (3-22). Considering the extreme case where v_{ds_L} during the turn-on transient drops to 0 instantaneously (i.e., t_{fv} approaches 0), the first term in (3-22) can be rewritten as (consider $\left(R_p + R_{ds(on)}\right) i_{d\_L} \ll V_{DC}$)

$$V_{DC} \int_{t_0}^{t_2} i_{d\_L} dt = V_{DC} \int_0^{I_L} \frac{L_p i_{d\_L}}{V_{DC} - \left(R_p + R_{ds(on)}\right) i_{d\_L}} di_{d\_L} \approx \frac{1}{2} L_p {I_L}^2 \tag{3-23}$$

Substitute (3-23) into (3-22) and remove the conduction loss term $\left(R_{ds(on)} + R_p\right) {I_L}^2 t_{ring(on)}$, yielding

$$E_{sw(on)\_extreme} \approx \left(1 + \frac{\left(R_p + R_{ds(on)}\right) I_L}{V_{DC}}\right) V_{DC} Q_{rr} + \left(1 + \frac{2\left(R_p + R_{ds(on)}\right) I_L}{V_{DC}}\right) \frac{1}{2} C_H {V_{DC}}^2$$

$$+ \frac{1}{2} C_L {V_{DC}}^2 + \frac{2V_{diode}}{V_{DC}} \frac{1}{2} L_p {I_L}^2 \approx V_{DC} Q_{rr} + \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 \tag{3-24}$$

Similarly, during the turn-off transient, the input energy supplied by dc source $E_{dc(off)}$, the output energy stored in load inductor $E_{load(off)}$, and the energy transferred among parasitics $E_{p(off)}$ are given by (3-25) – (3-27) respectively, listed in Fig. 3-15.

Thus, the total energy loss during the turn-off transient under the extreme operating condition in Fig. 3-13(b) is given by (3-28). Considering the most extreme case during the turn-off transient, where i_{chan_L} drops rapidly to 0 with the slightly increase of v_{ds_L},

$$V_{DC} \int_{t_4}^{t_5} i_{chan\_L} dt \approx 0 \tag{3-29}$$

$$I_L \int_{t_4}^{t_6} v_{ds\_H} dt \approx I_L \int_{V_{DC}}^{-V_{diode}} \frac{C_L + C_H}{I_L} v_{ds\_H} dv_{ds\_H} \approx -\frac{1}{2} C_H {V_{DC}}^2 - \frac{1}{2} C_L {V_{DC}}^2 \tag{3-30}$$

Thus, removing the conduction loss term $I_L V_{diode} t_{ring(off)}$ in (3-28), the switching loss during turn-off transient under the most extreme case is simplified as

$$E_{sw(off)\_extreme} \approx \frac{1}{2} L_p {I_L}^2 \tag{3-31}$$

Combining (3-24) with (3-31), the total energy loss dissipated in the circuit under the most extreme operating condition is shown as

$$E_{sw\_extreme} = V_{DC} Q_{rr} + \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 + \frac{1}{2} L_p {I_L}^2 \tag{3-32}$$

It is found that the power loss contributed by ringing under the extreme operating condition is the energy consumption due to the reverse recovery and the energy stored in parasitics, which always exist under the normal operating conditions [17]. Note that all the aforementioned analysis depends on a generalized device model, and can be applied for Si MOSFETs as well.

$$E_{dc(off)\_extreme} = \int_{t_4}^{t_7} V_{DC} i_{d\_L} dt = V_{DC} \int_{t_4}^{t_5} \left(i_{chan\_L} + i_{c\_L}\right) + V_{DC} \int_{t_5}^{t_7} i_{c\_L} dt =$$

$$V_{DC} \int_{t_4}^{t_5} i_{chan\_L} dt + C_L {V_{DC}}^2 \tag{3-25}$$

$$E_{load(off)\_extreme} = \int_{t_4}^{t_7} v_{ds\_H} I_L dt = I_L \int_{t_4}^{t_6} v_{ds\_H} dt + I_L \int_{t_6}^{t_7} -V_{diode} dt = I_L \int_{t_4}^{t_6} v_{ds\_H} dt -$$

$$I_L V_{diode} t_{ring(off)} \tag{3-26}$$

$$E_{p(off)\_extreme} = \frac{1}{2} L_p {I_L}^2 + \frac{1}{2} C_H {V_{DC}}^2 - \frac{1}{2} C_L {V_{DC}}^2 \tag{3-27}$$

$$E_{sw(off)\_extreme} = V_{DC} \int_{t_4}^{t_5} i_{chan\_L} dt + I_L \int_{t_4}^{t_6} v_{ds\_H} dt + \frac{1}{2} L_p {I_L}^2 + \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 +$$

$$I_L V_{diode} t_{ring(off)} \tag{3-28}$$

Fig. 3-15. Summary of turn-off switching loss calculations under extreme operating conditions.

3.4.3 Discussion

As a matter of fact, each switching commutation contains two processes: switch state transition (i.e., from cutoff region to ohmic region for turn-on and from ohmic region to cutoff region for turn-off) and switch's voltage/current change (i.e., v_{ds} from V_{DC} to 0, i_d from 0 to I_L for turn-on and v_{ds} from 0 to V_{DC}, i_d from I_L to 0 for turn-off). Ideally, these two processes are completed simultaneously. However, considering the inevitable parasitics in practical application, the voltage and current of switches do not arrive at the steady state when the switch state transition is finished. Therefore, after the switch state transition completion, the energy stored in output capacitances of switches and power loop inductance will continuously transfer back and forth until the voltage and current of switches approach to their steady state value. Thus, the parasitic ringing originates from the energy transfer among parasitics after the switch state transition completion. Also, according to the energy conservation, the energy dissipation induced by damping parasitic ringing should theoretically be equal to the energy variation of every parasitic. In total, the parasitic ringing contributed switching energy loss do exist, but is at most the energy stored in the parasitics as in (3-32), regardless of the reverse recovery, which is a reasonable assumption for SiC devices with excellent reverse recovery characteristics. Compared with the total switching energy which is primarily induced by the overlap between the drain-source voltage and drain current, the switching energy loss induced by damping ringing is a small portion, and can be ignored.

3.5 Data Processing

Traditionally, v_{ds} and i_d of the operating device are detected. However, considering the impact of cross-talk on the switching behavior (detailed description can be found in section

4.1.3), the aforementioned two parameters seem to be insufficient in the high-speed switching test.

3.5.1 Impact of Cross-Talk on Data Processing

In a phase-leg configuration, high *dv/dt* during fast turn-on transient of one device will generate a displacement current from the Miller capacitance of its complementary device. This displacement current flows into the gate loop, leading to a positive spurious gate voltage, as shown in Fig. 3-16. This positive spurious gate voltage may generate a shoot-through current, flowing from the affected device to the operating one. Therefore, it is possible that during the switching transient of one device, the switching losses of its complementary device become comparable to that of the operating one. So v_{ds} and i_d of both the upper and lower devices should be detected.

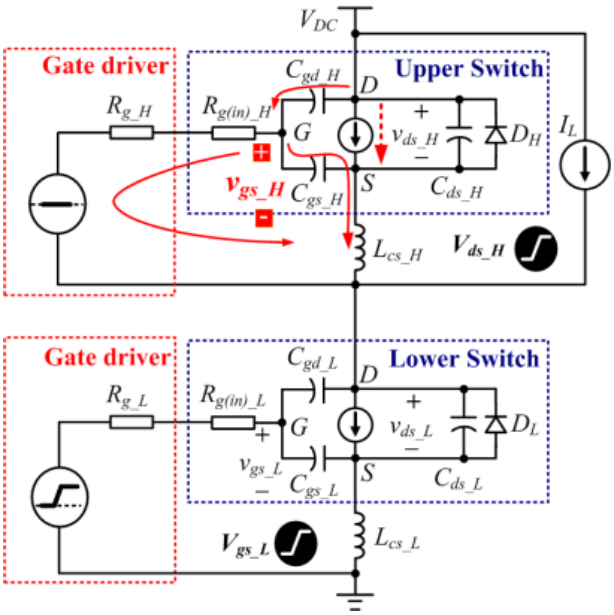


Fig. 3-16. Mechanism causing cross-talk during the turn-on transient.

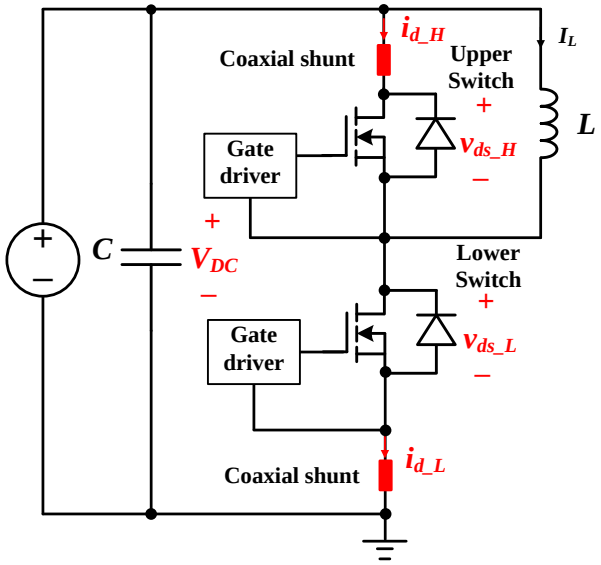


Fig. 3-17. Measurement parameters in DPT for switching loss evaluation.

3.5.2 A Practical Method for Switching Loss Evaluation

To obtain the total switching losses during the switching transient of the DUT, v_{ds} and i_d of both the upper and lower switch in a phase-leg should be measured. Thus, as shown in Fig. 3-17, two coaxial shunts are required to insert into the drain terminal of the upper switch and source terminal of the lower switch, which will induce more parasitic inductance in the power loop.

A more practical method is proposed for switching loss evaluation in a phase-leg. According to energy conservation, the losses dissipated during the switching transient of DUT are equal to the difference between the energy supplied by the dc capacitor and the energy stored in the load inductor. Hence, based on i_d of the operating device (i.e., current through dc source), v_{ds} of its complementary device (i.e., voltage across load inductor), together with the dc bus voltage V_{DC} and inductive load current I_L, the switching losses are given by (assuming the lower device as the device under operation)

$$E_{io} = \int (V_{DC} i_{d\_L} - I_L v_{ds\_H}) dt \tag{3-33}$$

This method only requires one coaxial shunt, but can still measure the switching losses of both upper and lower devices. Another advantage of this method is its insensitivity on V−I alignment, because, as in (3-33), each term incudes one switching waveform (i_{d_L} or v_{ds_H}) and a relatively constant variable (V_{DC} or I_L).

3.5.3 Experimental Verification

Fig. 3-18 shows a phase-leg power module built with Cree CPM2-1200-0025B SiC MOSFETs and CPW5-1200-Z050B SiC Schottky diode bare dies. A double pulse tester with this phase-leg power module is established for the switching characterization, as shown in Fig. 3-19.

Based on the aforementioned method, Fig. 3-20 displays the V_{DC}, v_{ds_H}, I_L and i_{d_L} during the switching transient of the lower switch under the operating condition of 600-V/30-A with 10 Ω gate resistance. According to (3-33), the total switching loss E_{io} is 574 μJ. Based on the traditional method, E_{sw_L} and E_{sw_H} under the same operating condition are 499 μJ and 73 μJ, respectively. Hence, E_{io} is approximately equal to the sum of E_{sw_L} and E_{sw_H}.

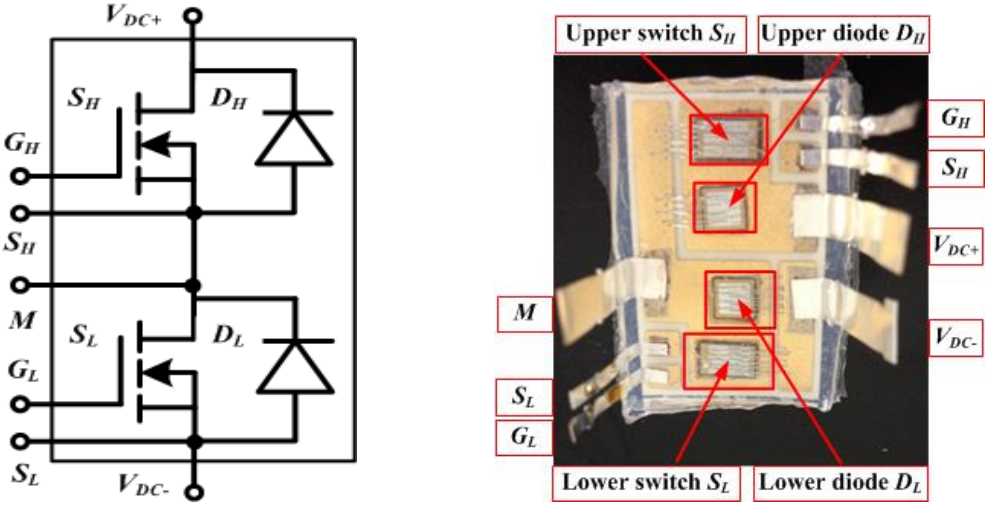


Fig. 3-18. 1200 V SiC based phase-leg power module.

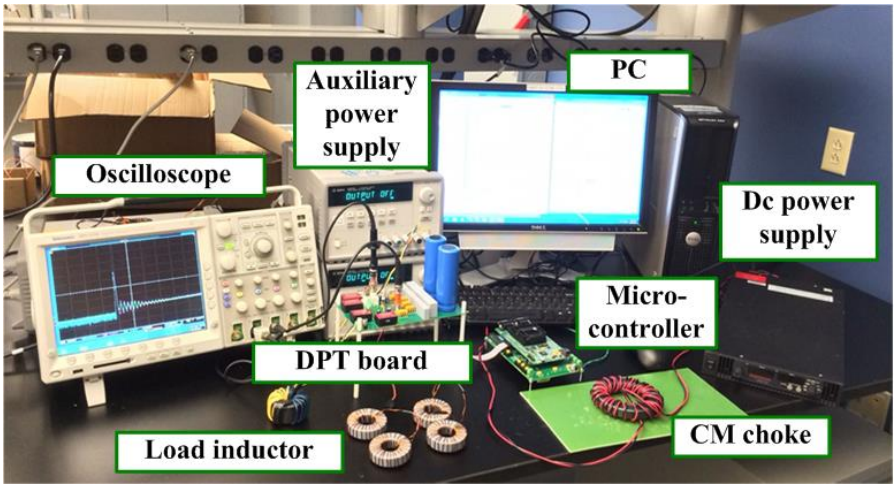


Fig. 3-19. Double pulse tester hardware setup.

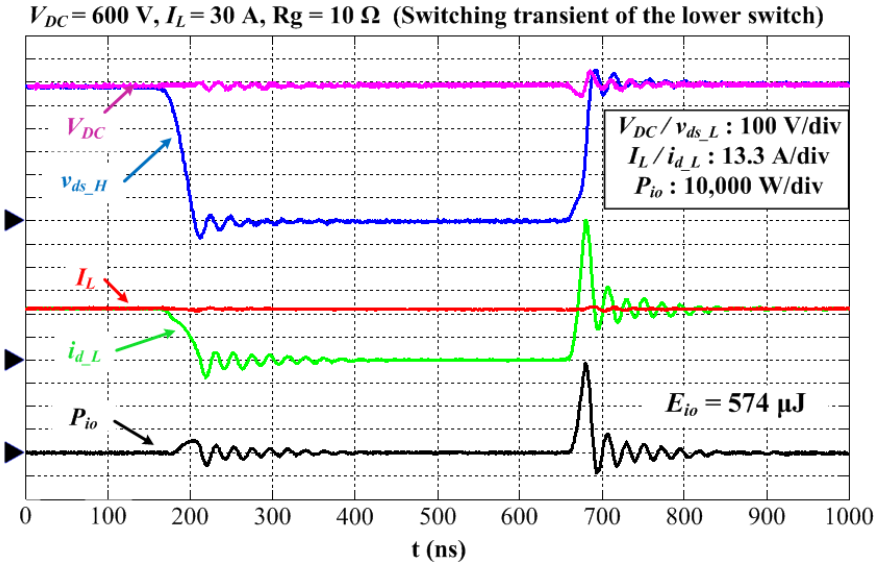
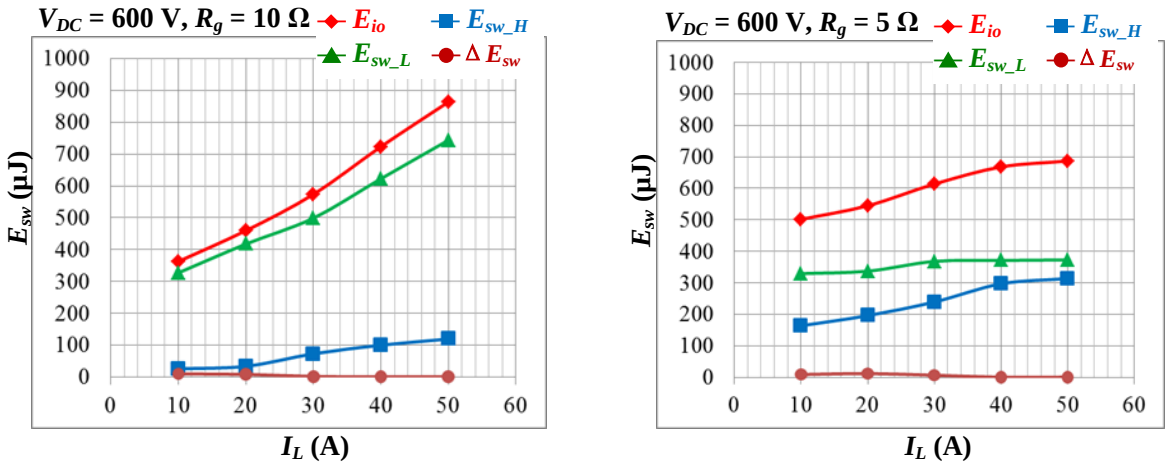


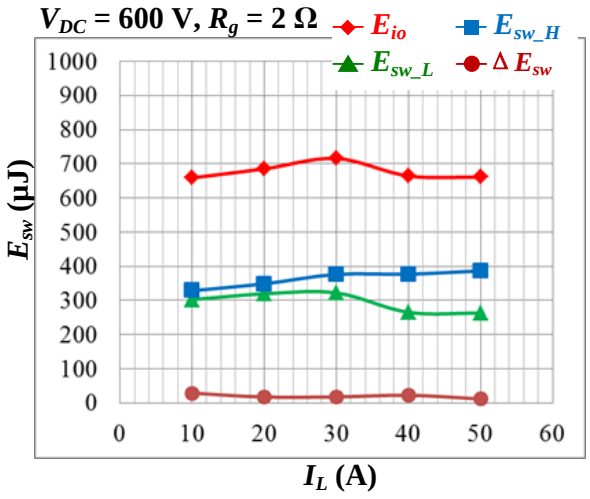
Fig. 3-20. Switching waveforms for the proposed method.

More cases with gate resistances of 10/5/2 Ω, operating voltages of 600 V, and operating currents of 10/20/30/40/50 A are tested, as shown in Fig. 3-21. Note that ΔE_{sw} indicates the difference between E_{io} and the sum of E_{sw_L} and E_{sw_H}. It shows that E_{sw_H} is comparable to E_{sw_L} during the switching transient of the lower switch, especially under the operating conditions with

small gate resistance. When gate resistance becomes 2 Ω, E_{sw_H} is even larger than E_{sw_L}. In addition, ΔE_{sw} always approaches zero under different operating conditions, which means that E_{io} can accurately evaluate the total switching losses.



(a) R_g = 10 Ω. (b) R_g = 5 Ω.



(c) R_g = 2 Ω.

Fig. 3-21. $E_{sw(tot)}$, E_{sw_L}, E_{sw_H}, and ΔE_{sw} dependence on load currents.

Fig. 3-22 shows the test of sensitivity of E_{io} on the V−I timing alignment. Under the operating condition of 600-V/10-A with 2-Ω gate resistance, instead of steep slew rates for E_{sw_L} and E_{sw_H}, E_{io} remains constant when the timing alignment changes. Consequently, the proposed method is a practical and accurate solution for switching losses evaluation of SiC devices in a phase-leg configuration.

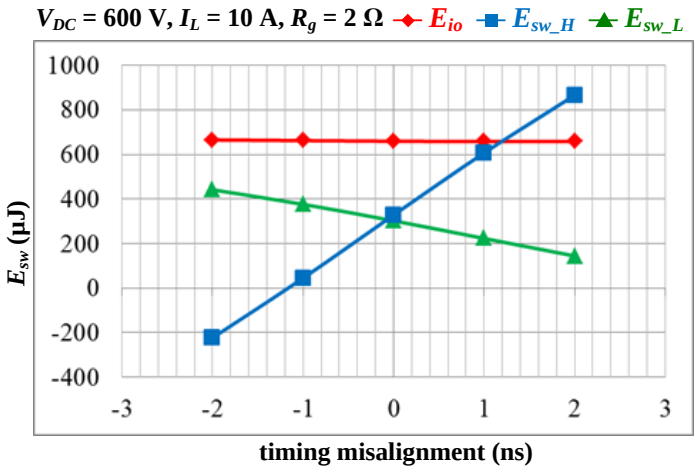


Fig. 3-22. Comparison of V−I alignment sensitivity among E_{io}, E_{sw_L} and E_{sw_H}.

3.6 Conclusion

Five factors need to be taken into account for the switching characterization of SiC devices in a phase-leg configuration. First, layout of the DPT board should be universal for the actual converters and optimized for the sensitive parasitics (e.g., power loop inductance, common source inductance and Miller capacitance). Second, probes for switching waveforms should satisfy bandwidth, dynamic range, and accuracy requirements. Based on the comparison of the latest probes, high voltage passive probe and coaxial shunt are preferred. Third, V−I timing alignment must be carefully deskewed due to its high sensitivity on switching losses (tested up to

272 μJ/ns). Three methods of V−I alignment and tips are summarized. Fourth, probes induced grounding effects should be suppressed for the measurement accuracy of high-speed switching waveforms. Common-mode choke is recommended. Fifth, in a phase-leg, the switching losses of the non-operating devices cannot be ignored, especially for the fast switching SiC devices. To cope with the sensitivity issue of V−I timing alignment and the complexity of testing two devices for the switching losses evaluation, a practical method by calculating the difference between the input energy supplied by a dc capacitor and the output energy stored in a load inductor is proposed. Based on Cree 1200 V SiC MOSFETs, the experimental results show that this method can accurately obtain the switching loss of both devices by using only one coaxial shunt. Also, its test results are insensitive to the V−I alignment.

Additionally, the commonly observed parasitic ringing in the switching waveforms does not need to take into account for the switching loss assessment. This is because that the switching energy contributed by damping parasitic ringing is at most the energy dissipation induced by reverse recovery and the energy stored in parasitics, which is a small portion of the total switching losses.

4 Characterization of Limitations and Impact Factors of High Switching-Speed Capability of SiC Devices

This chapter studies the limitations and impact factors of switching performance of SiC devices in voltage source converter. As compared to previous research efforts, in this chapter, we not only focus on the interaction between gate driver and power device in a phase-leg, but also consider the impacts of all the possible factors in a voltage source converter. A three-phase voltage source inverter fed motor drives are selected as the representative of voltage source converter since it is a widely applied voltage source topology in a popular application. Also, the three-phase voltage source inverter in motor drives covers almost all the components in a voltage source converter. Thus, the generality of the following analysis is not lost.

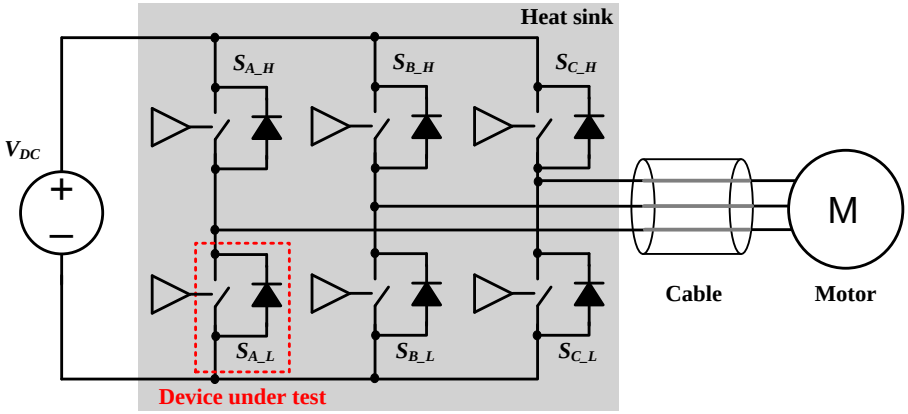


Fig. 4-1. Three-phase voltage source inverter fed motor drives.

Fig. 4-1 displays a three-phase voltage source inverter fed motor drives, where the lower switch of phase A is selected as the device under test (DUT). As can be observed, the switching performance of DUT will be affected by the interaction between gate driver and device, and the

interference between upper and lower switches in a phase-leg. Also, in a three-phase voltage source inverter, the other phase-legs (i.e., phase B and C) and heat sink may become the possible impact factors. Moreover, motor/cable load will impact the switching performance as well. Consequently, except the impact factors studied previously and mentioned in literature review, six factors are investigated in this chapter according to the inherent properties of SiC devices, including 1) reverse recovery characteristics of the SiC devices' body diode, 2) the over-voltage of the opposite device during the turn-on transient of the operating one in a phase-leg, 3) interference of the lower and upper devices in a phase-leg (i.e., cross-talk), 4) parasitics of the inductive loads, 5) the interaction of other phase-legs in a three-phase system, and 6) heat sink. These identified impact factors cover the interaction of gate driver and power device, upper and lower devices in a phase-leg, phase-legs of three-phase voltage source converter, as well as voltage source converter and load, which form a comprehensive understanding of the limitations and impact factors of switching performance for SiC devices in voltage source converter. In this chapter, six factors are divided into two groups in the following discussion: the first three factors in the phase-leg configuration form one group; the other group contains the last three factors with respect to the three-phase motor drive system. For each factor, the theoretical analysis and experimental verification are presented.

4.1 Impact Factors in the Phase-leg Configuration

4.1.1 Body Diode of SiC MOSFETs

Switching commutation occurs between the channel of the operating device and the freewheeling diode of the non-operating one in a phase-leg. Originally, instead of utilizing the body diode of silicon (Si) device considering its poor reverse recovery characteristics, an external Schottky barrier diode (SBD) is added for switching performance optimization [108,

109]. However, the extra SBD will increase the number of the devices employed in the power converter, and then worsen the power density.

Unlike traditional Si devices, SiC has shorter lifetime of minority carriers so that not a large reverse recovery current is estimated, which enables the body diode of the SiC MOSFET to be a brilliant body diode with almost no reverse recovery charge [68]. Therefore, a few researchers and semiconductor manufacturers claim that it is unnecessary to antiparallel external SBD for a SiC based power conversion system [31, 69].

However, due to the lateral-vertical channel design, the body diode of normally-on SiC-JFETs and SiC MOSFETs is a P-N junction diode. Although its reverse recovery characteristics are substantially lower when compared to the state-of-art Si counterparts, and equivalent to that of a discrete SiC SBD [31, 69], the performance at high *di/dt* transient with high operating temperature may become worse [109]. It is reported that the body diode of normally-on SiC JFETs gave rise to severe reverse recovery as junction temperature increases, leading to significant increase of switching losses[70].

In total, there is no evident conclusion on the usage of the body diode of SiC MOSFETs in the voltage source converter. Therefore, it is important to evaluate the reverse recovery performance of the body diode of SiC MOSFETs, especially during the fast switching transient under high operating temperature. A double pulse tester board with Cree 2nd generation 1200-V/20-A SiC MOSFETs is constructed, as shown in Fig. 4-2. Additionally, Cree 1200-V/20-A SiC Schottky diodes are prepared to reassemble the phase-leg configuration from switch-switch pair to switch-diode pair (see Fig. 4-3) for the evaluation of body diode's impact on the switching behavior.

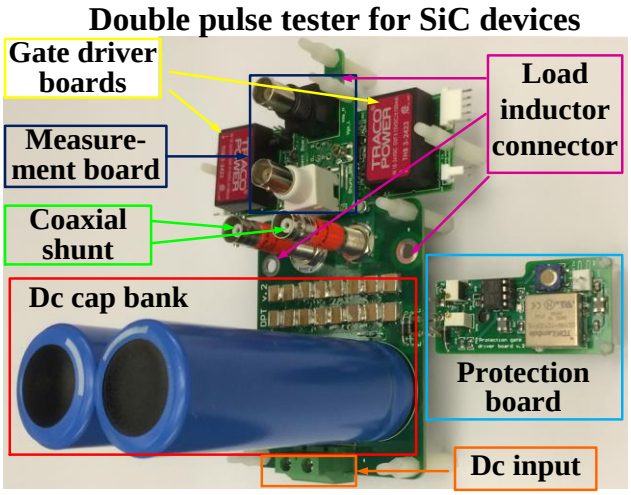
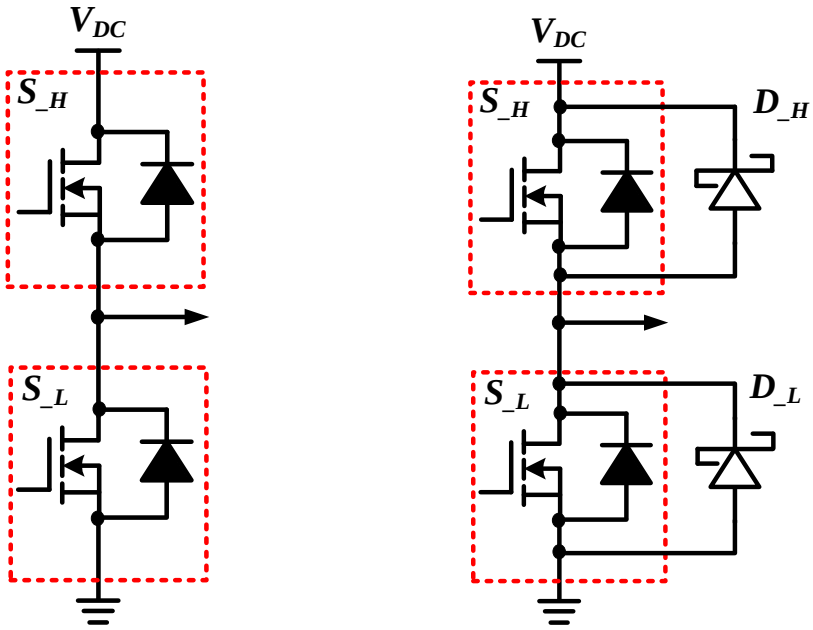


Fig. 4-2. Double pulse tester setup.



(a) switch-switch pair. (b) switch-diode pair.

Fig. 4-3. Typical phase-leg configuration.

As can be observed in Fig. 4-4, the switching performance in the switch-switch pair based phase-leg configuration is highly sensitive to the junction temperature. There is an apparent

higher over-current at 100 ^{o}C as compared to that at room temperature, leading to increased turn-on switching loss up to 25.2%. Generally, the over-current during the turn-on transient comes from three sources: 1) reverse recovery current, 2) displacement current induced by junction capacitance, 3) cross-talk induced shoot-through current. Considering the roughly same *dv/dt* under different junction temperature, the *Cdv/dt* induced displacement current should stray nearly constant. Also, the cross-talk induced shoot-through current can be effectively eliminated since the gate drivers are integrated with the anti-cross-talk function (detailed description will be given in chapter 5). Thus, the extra over-current at high junction temperature is originated from the reverse recovery current of the device's body diode.

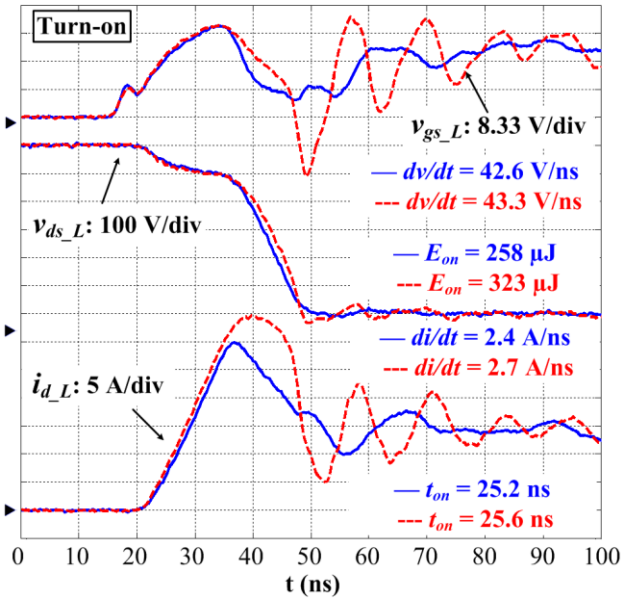


Fig. 4-4. Switching waveform comparison under different junction temperatures for switch-switch pair configuration: solid blue line refers to switching waveform at room temperature; dashed red line indicates switching waveform at 100 ^{o}C.

To further verify the reverse recovery characteristics of the body diode, another comparison experiment is carried out. Under the same junction temperature (e.g., 100 ^{o}C), the switching waveform with different phase-leg configurations is monitored, as shown in Fig. 4-5. It is straightforward to observe that the Schottky diode in the switch-diode pair based phase-leg configuration significantly mitigates the over-current, resulting in less switching losses. Hence, the excessive over-current in the switch-switch pair configuration in Fig. 4-4 is due to the reverse recovery current of the device's body diode.

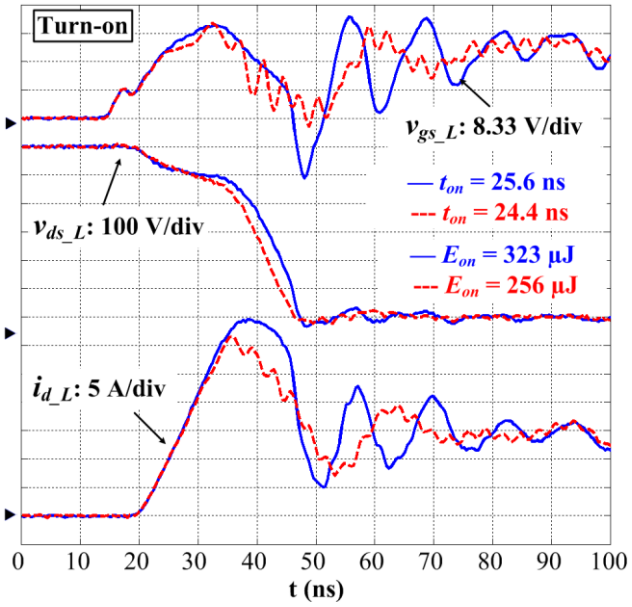


Fig. 4-5. Switching waveform comparison under different phase-leg configurations @ 100^{o}C: solid blue line refers to switch-switch pair; dashed red line indicates switch-diode pair.

Also, the switching waveform comparison in Fig. 4-6 shows that the switching behavior in switch-switch configuration is almost identical to that in switch-diode configuration at room temperature, which means that reverse recovery characteristics of the device's body diode at

room temperature is acceptable. In the meantime, the switching behavior in the switch-diode configuration is nearly regardless of the junction temperature. In total, the reverse recovery performance of the body diode of SiC MOSFETs becomes worse as the junction temperature increases. It is recommended to have antiparallel Schottky diode to guarantee the stable switching performance under different operating temperatures, which is especially critical for the SiC based converter for high temperature applications.

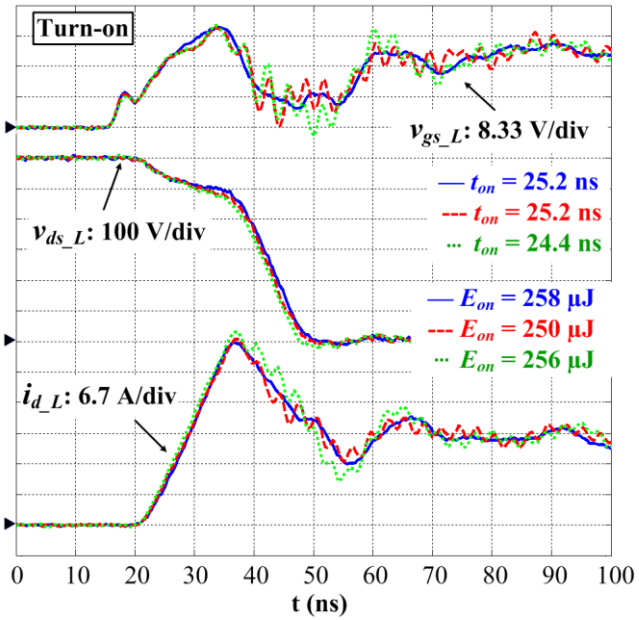


Fig. 4-6. Switching waveform comparison under different phase-leg configurations and different junction temperatures: solid blue line refers to switch-switch pair @ 25 ^{o}C; dashed red line indicates switch-diode pair @ 25 ^{o}C; dotted green line represents switch-diode pair @ 100 ^{o}C.

There is a tradeoff on the selection of antiparallel Schottky diode: first, junction capacitance of the selected Schottky diode should be as small as possible since it increases the equivalent output capacitance of the main switch and negatively affects the switching speed. Therefore, the

lower current rating Schottky diode is preferred. On the other hand, the lower current rating means higher forward voltage drop, causing certain amount of inductive load current flowing through the body diode of the main switch instead of the antiparallel Schottky diode. Accordingly, the turn-on switching performance will still be suffered by the relatively poor reverse recovery characteristics of the main switch, especially at high operating temperature. In practice, anti-parallel Schottky diode should be selected to have larger current rating than that of the main switch.

4.1.2 Fast Turn-on Transition Induced Over-Voltage

Voltage spike during the switching transient is a well-known issue to limit the switching speed. Since the over-voltage becomes higher as the switching speed increases; once the voltage overshoot approaches the breakdown voltage of power devices, the switching speed cannot further increase. Prior reported works primarily focus on the over-voltage of the operating device during the turn-off transient, limited studies investigate the over-voltage of the opposite device during the turn-on transient [103, 104]. However, as can be observed in Fig. 4-7, which shows the test results based on Cree 2nd generation 1200-V/50-A SiC MOSFETs, the voltage spikes during the turn-on transient are always higher than the voltage overshoot during the turn-off transient under different operating currents with varied gate resistors. Even worse, using a gate driver with anti-cross-talk gate assist circuit (detailed description will be given in chapter 5), the turn-on over-voltage with 2-Ω gate resistance has reached the breakdown voltage of the device under test (i.e., 1200 V), then the upper switch is observed to be damaged. Therefore, the over-voltage during turn-on should be concerned for the fast switching SiC devices.

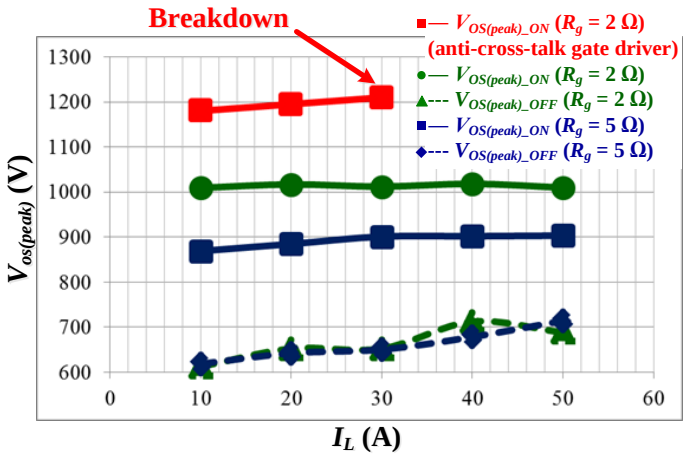


Fig. 4-7. Over-voltage comparison between turn-on and turn-off transients.

4.1.2.1 Mechanisms Causing Over-voltage during Turn-on

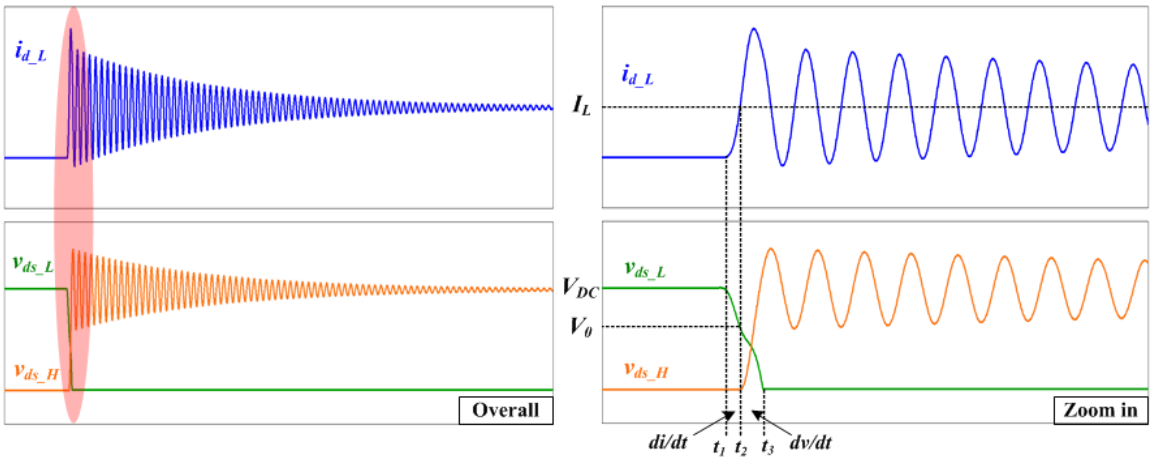
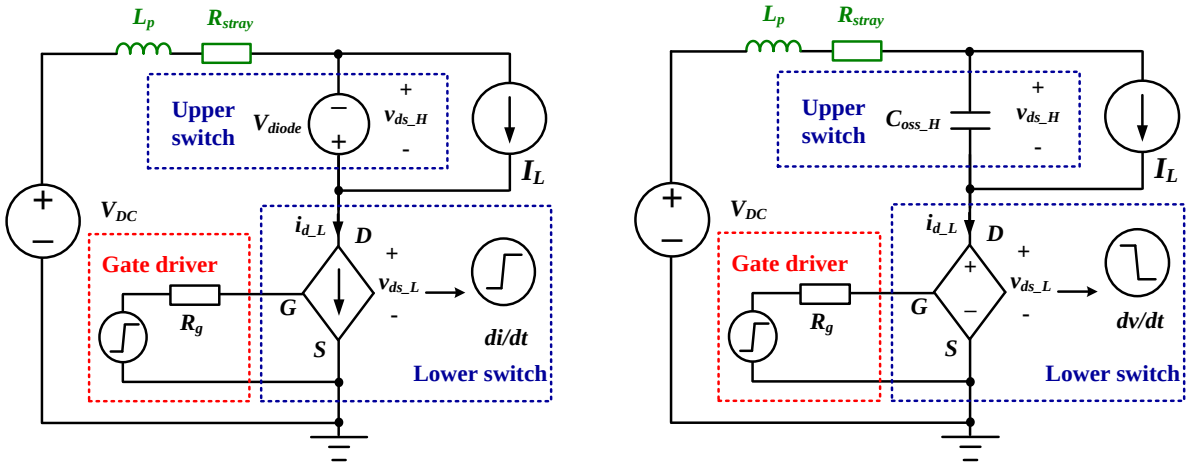


Fig. 4-8. Switching waveforms during turn-on transient.

Fig. 4-8 shows switching waveform during the turn-on transient of the lower switch, including drain current of the lower switch i_{d_L}, drain-source voltage of the lower and upper switches v_{ds_L}, v_{ds_H}. During *di/dt* subinterval, the upper switch can be regarded as a freewheeling diode in conduction mode with a forward voltage drop of V_{diode}; once i_{d_L} approaches inductive

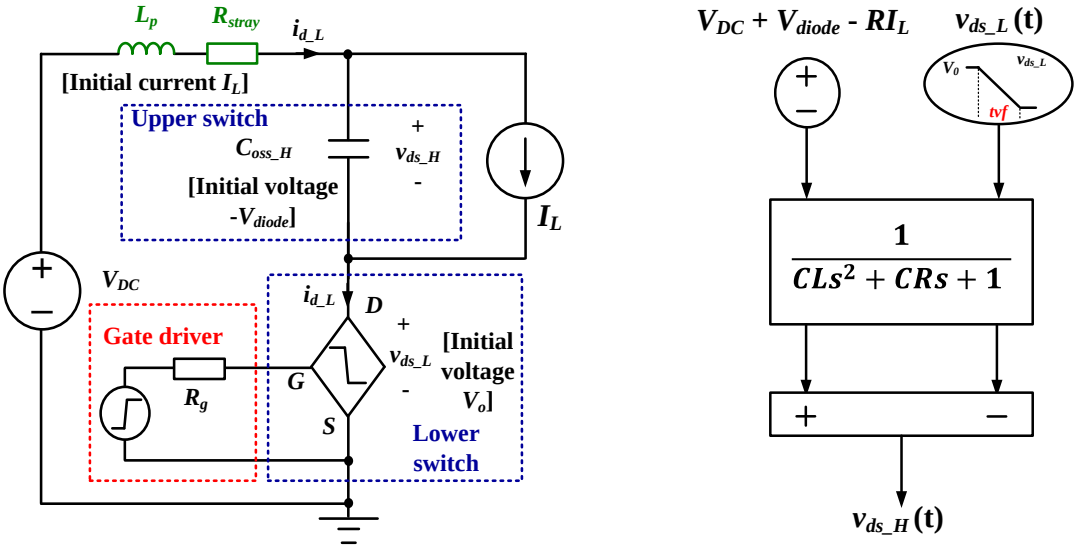
load current I_L, upper switch starts to block voltage, and is considered as an output capacitance C_{oss_H} during *dv/dt* subinterval, as shown in Fig. 4-9. An assumption is made for the above analysis, that is the freewheeling diode of the upper switch has excellent reverse recovery characteristics so that the upper switch shows capacitive characteristics instantaneously when all the inductive current flows into the lower switch. This assumption makes sense due to a SiC Schottky diode is commonly paralleled with the main switch as the freewheeling diode. Therefore, the analysis of the over-voltage of the upper switch can be simplified to solve the peak value of voltage across C_{oss_H} during *dv/dt* subinterval in Fig. 4-10(a). Via Laplace transform, the expression of v_{ds_H} is given in Fig. 4-10(b) and (4-1), where for the simplification, *L*, *R*, *C* represent the power loop inductance L_p, stray resistance R_{stray}, and output capacitance of power device C_{oss}, respectively.

$$v_{ds\_H}(s) = \frac{V_{DC}+V_{diode}-RI_L}{s(CLs^2+CRs+1)} - \frac{v_{ds\_L}(s)}{CLs^2+CRs+1} \tag{4-1}$$



(a) *di/dt* transient. (b) *dv/dt* transient.

Fig. 4-9. Equivalent circuit of phase-leg configuration during turn-on transient.



(a) Equivalent circuit with initial value. (b) Expression after Laplace transform.

Fig. 4-10. Equivalent circuit and expression for turn-on over-voltage analysis.

It is found that two excitations involve in the expression of v_{ds_H}: one is V_{DC} + V_{diode} –RI_L, which is a dc component indicating the voltage difference of the upper switch between off-state and on-state; the other is v_{ds_L}, which is a transient component, and can be modeled as a controllable voltage source with a ramp change. The switching speed determines the slew rate of this voltage source. Thereby, the mechanism causing over-voltage of the upper switch is due to a voltage source with high *dv/dt* hits a *LRC* series resonant network. Considering the SiC devices with high switching-speed capability and small on-state resistance, the overshoot voltage is higher and parasitic ringing duration becomes longer compared with their Si counterparts.

For the analytical modeling, v_{ds_L} during *dv/dt* subinterval can be simplified as

$$v_{ds\_L}(t) = \begin{cases} V_o\left(1 - \frac{t}{t_{vf}}\right), \ if \ t < t_{vf} \\ 0, \ otherwise \end{cases} \tag{4-2}$$

where t_{vf} is the voltage fall time during the turn-on transient; V_0 is the initial voltage across the drain-source terminals of the lower switch, which is lower than V_{DC} due to the snubber effect induced by L_p during *di/dt* subinterval, but usually greater than 0. Under certain extreme operating conditions, such as low dc bus voltage or large load current, v_{ds_L} will drop to 0 before i_{d_L} approaches I_L, which means that V_0 equals to zero [110]. Thus, two cases according to different V_0 are discussed for the analytical model of v_{ds_H} afterwards.

First, assume V_0 equals to 0. In this case, only one dc component affects v_{ds_H}, the corresponding expression of v_{ds_H} is given by

$$v_{ds\_H}(t) = V_{DC} - RI_L + (V_{DC} + V_{diode} - RI_L)sin(2\pi f \times t) \cdot e^{-\frac{t}{\tau}} \qquad (4\text{-}3)$$

where $f = \frac{1}{2\pi\times\sqrt{CL}}$ is the parasitic ringing frequency; $\tau = \frac{2L}{R}$ is damping time constant. Considering the ringing period T (i.e., $1/f$) is always shorter than τ, the peak value of v_{ds_H} is approximately equal to

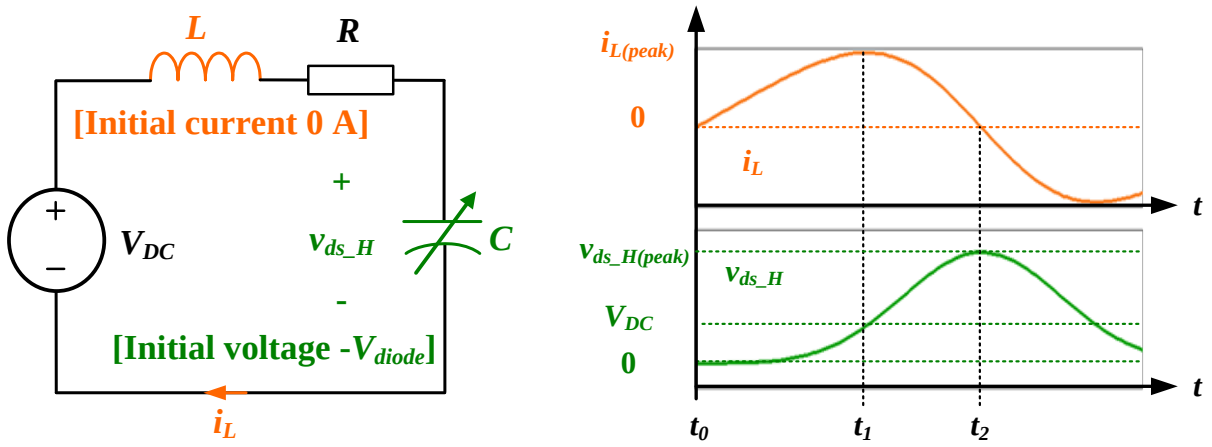
$$v_{ds\_H(peak)} \approx 2V_{DC} + V_{diode} - 2RI_L \approx 2V_{DC} \qquad (4\text{-}4)$$

Since in this case, v_{ds_L} is 0. Also, according to (4-1), v_{ds_L} negatively affects v_{ds_H}. Thus, $v_{ds\_H(peak)}$ obtained in this case is the highest. However, (4-4) illustrates that $v_{ds\_H(peak)}$ in the worst case will never exceed two times of dc bus voltage, which conflicts with the test results in Fig. 4-7. This contradiction makes us take the non-linear characteristics of the device's output capacitance into account.

In the worst case (V_0 = 0), the equivalent circuit in Fig. 4-10(a) can be redrawn as in Fig. 4-11(a), which is a typical *LRC* series resonance circuit. According to circuit theory with the initial value of *LC* in Fig. 4-11(a), the resonance waveform is shown in Fig. 4-11(b). During the first quarter of the resonant period from t_0 to t_1, dc voltage source charges output capacitance of the

upper switch, enabling v_{ds_H} to increase from -V_{diode} to V_{DC} with certain amount of energy storage, In the meantime, the same amount of energy is stored in power loop inductance L. During the next quarter of the resonant period from t_1 to t_2, all the energy stored in L transfers to C, resulting in the over-voltage $v_{ds\_H(peak)}$. Hence, the energy stored in C from t_0 to t_1 should be identical to the increased energy of C from t_1 to t_2, yielding

$$\int_{-V_{diode}}^{V_{DC}} C \times v_{ds\_H} \times dv_{ds\_H} \approx \int_{0}^{V_{DC}} C \times v_{ds\_H} \times dv_{ds\_H} = \int_{V_{DC}}^{v_{ds\_H(peak)}} C \times v_{ds\_H} \times dv_{ds\_H} \tag{4-5}$$



(a) Equivalent circuit. (b) Resonance waveform.

Fig. 4-11. Over-voltage during turn-on in the worst case (V_0 = 0).

Additionally, output capacitance of the power device C is voltage dependent, the lower the drain-source voltage, the higher the C, as shown in Fig. 4-12. For the sake of simplicity in the analysis, a common way of expressing non-linear C as two discrete values is adopted, as

$$C = \begin{cases} C_1, \ if \ v_{ds\_H} < V_1 \\ C_2, \ otherwise \end{cases} \tag{4-6}$$

where C_1 >> C_2, V_1 is determined by the boundary of devices between ohmic and saturation region [111, 112]. Substituting (4-6) into (4-5), a new expression of $v_{ds\_H(peak)}$ considering non-linear characteristics of C is given as

$$v_{ds\_H(peak)} = V_{DC}\left(1 + \sqrt{1 + 2\frac{C_1}{C_2}\frac{V_1}{V_{DC}}}\right) > 2V_{DC} \tag{4-7}$$

Thus, the test results in Fig. 4-7 can be explained.

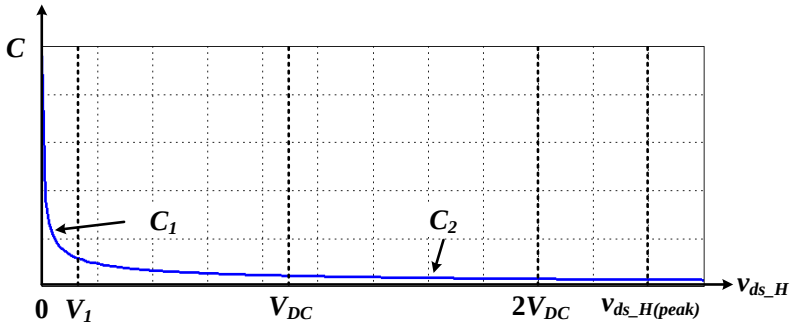


Fig. 4-12. Non-linear characteristics of device's output capacitance.

For the normal operating condition (V_0 ϵ (0, V_{DC}]), v_{ds_L} is expressed as in (4-2), $v_{ds\_H(peak)}$ is given by

$$v_{ds\_H}(t) = \begin{cases} V_{DC}(1 - cos\omega t \times e^{-\frac{t}{\tau}}) - V_0(1 - cos\omega t \times e^{-\frac{t}{\tau}} - \frac{t}{t_{vf}} + \frac{sin\omega t}{\omega t_{vf}} \times e^{-\frac{t}{\tau}}),\ if\ t < t_{vf} \\ V_{DC}\left(1 - cos\omega t \times e^{-\frac{t}{\tau}}\right) + V_0(cos\omega t + \frac{sin(\omega t - \omega t_{vf}) - sin\omega t}{\omega t_{vf}}) \times e^{-\frac{t}{\tau}},\ otherwise \end{cases} \tag{4-8}$$

where $\omega = 2\pi f = \frac{1}{\sqrt{CL}}$ is the parasitic ringing angular frequency.

4.1.2.2 Impact of Turn-on Over-voltage on Switching Speed

It is straightforward to conclude that the over-voltage, especially turn-on over-voltage, limits the switching speed of SiC devices. The following effort is to quantify this limitation via establishing a *di/dt* and *dv/dt* safe operating area in terms of $v_{ds\_H(peak)}$. To keep the generality for different models of power devices with different operating conditions, $v_{ds\_H(peak)}$ in (4-8) is normalized

$$\frac{v_{ds\_H}(t)}{V_{dc}} =$$

$$\begin{cases} (1-cos(2\pi k_t \times \frac{t}{t_{vf}})) - k_v(1-cos(2\pi k_t \times \frac{t}{t_{vf}}) - \frac{t}{t_{vf}} + \frac{sin(2\pi k_t \times \frac{t}{t_{vf}})}{2\pi k_t}),\ if\ t < t_{vf} \\ \left(1-cos(2\pi k_t \times \frac{t}{t_{vf}})\right) + k_v(cos(2\pi k_t \times \frac{t}{tv_f}) + \frac{sin(2\pi k_t \times (\frac{t}{t_{vf}}-1)) - sin(2\pi k_t \times \frac{t}{t_{vf}})}{2\pi k_t}),\ otherwise \end{cases}$$

(4-9)

where $k_v = \frac{V_0}{V_{DC}}$ is the coefficient related to the snubber effect induced by power loop parasitic inductance *L* during *di/dt* transient, $k_t = \frac{t_{vf}\omega}{2\pi} = \frac{t_{vf}}{T}$ is the coefficient to indicate voltage fall time. Fig. 4-13 shows the impact of k_v and k_t on the normalized over-voltage. It is observed that the over-voltage increases as the decrease of k_v. In other words, higher the *di/dt*, more serious the *L* related snubber effect is, and lower the V_0 would be, causing the higher over-voltage. In addition, k_t shows an uncertain relation with over-voltage: if k_t <1 (i.e., $t_{vf} < T$), the smaller k_t or the shorter t_{vf} leads to the higher over-voltage; otherwise, their relation is nonmonotonous. In summary, *di/dt* affects k_v, while *dv/dt* impacts k_t, and both of them determines the turn-on over-voltage. Two new coefficients, k_{di_dt} and k_{dv_dt}, are applied to establish the relation between over-voltage and *di/dt*, *dv/dt* in a normalized system.

$$k_{di\_dt} = k_v = \frac{di}{dt} \times \frac{L}{V_{DC}} \tag{4-10}$$

$$k_{dv\_dt} = \frac{1}{k_t} = \frac{dv}{dt} \times \frac{T}{V_{DC}} \tag{4-11}$$

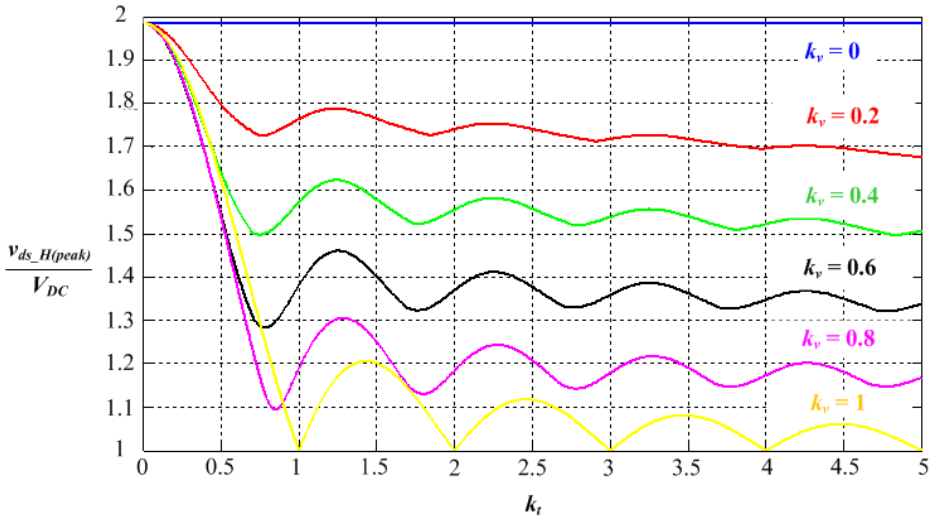


Fig. 4-13. Normalized turn-on over-voltage dependence on k_v and k_t.

Fig. 4-14 displays a 3-D plot, indicating the normalized turn-on over-voltage dependence on k_{dv_dt} and k_{di_dt}. Assume the safe margin of the voltage overshoot is 1.5 times of V_{DC}, we can obtain a *dv/dt*, *di/dt* related safe operating area (SOA), as shown in Fig. 4-15. According to this SOA, $k_{dv\_dt} < 1$ together with $k_{di\_dt} < 0.4$ can guarantee the over-voltage below 150% V_{DC}. The absolute value of *di/dt* and *dv/dt* depends on the parasitic inductance associated in power loop, device's output capacitance, as well as the specific operating point. Taking Cree 1200-V/50-A SiC MOSFETs operating at 800 V V_{DC} with 50 nH power loop inductance as an example, to satisfy the over-voltage requirement, *dv/dt* should be less than 38.4 V/ns with *di/dt* below 6.4 A/ns. Also note that the above analysis does not take non-linear characteristics of device's output capacitance into account. Thus, the maximum over-voltage is always lower than 2 times of V_{DC}.

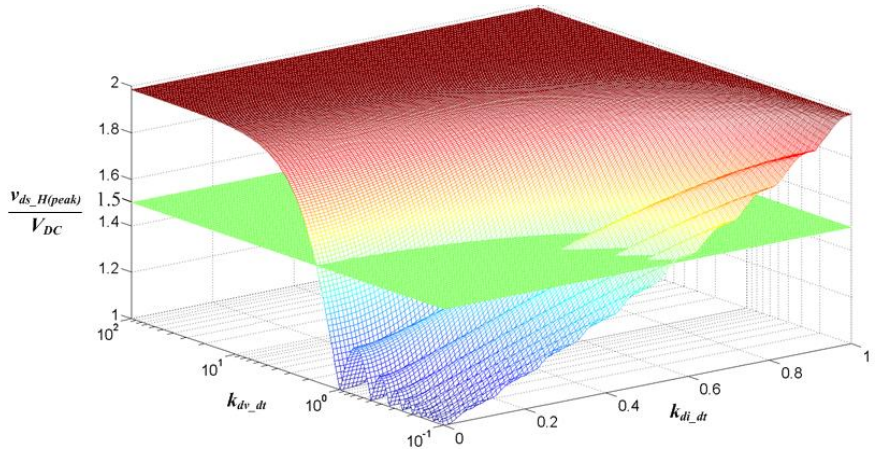


Fig. 4-14. Normalized turn-on over-voltage dependence on k_{dv_dt} and k_{di_dt}.

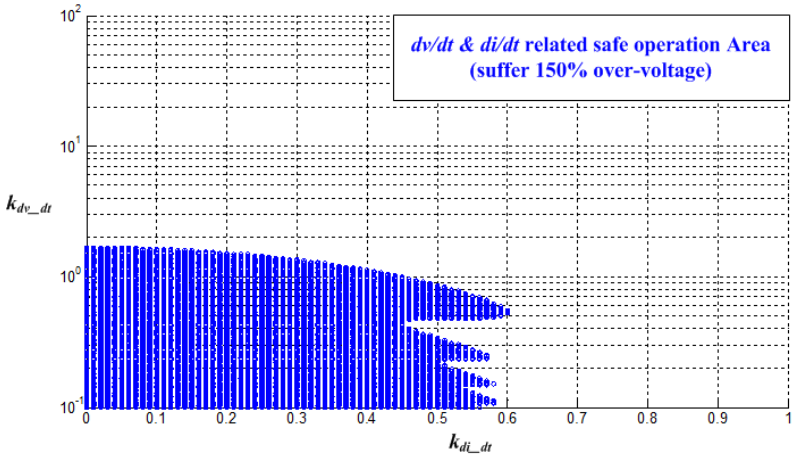


Fig. 4-15. *dv/dt* and *di/dt* related safe operating area (150% over-voltage case).

Non-linear characteristics of the device's output capacitance worsens the turn-on over-voltage. Fig. 4-16 shows the absolute value of turn-on over-voltage dependence on k_{dv_dt} and k_{di_dt} when Cree 1200-V/50-A SiC MOSFET operates at 800 V V_{DC}. The maximum overvoltage approaches to 1950 V, which is 2.4 times of V_{DC}. To limit the over-voltage below breakdown voltage, the *dv/dt*, *di/dt* should locate within the safe operating area in Fig. 4-17. Also, it shows

that the large power loop inductance shrinks the *dv/dt*, *di/dt* related safe operating area. Therefore, the switching speed is limited.

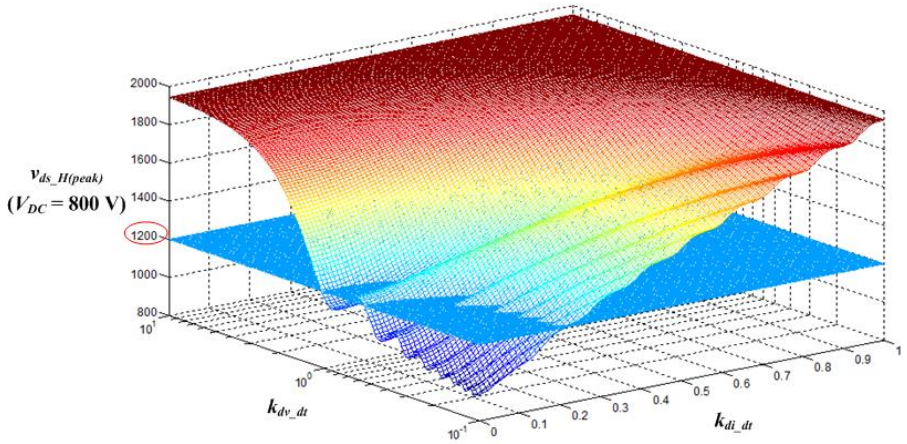


Fig. 4-16. Turn-on over-voltage dependence on k_{dv_dt} and k_{di_dt} (1200-V/50-A Cree SiC MOSFET)

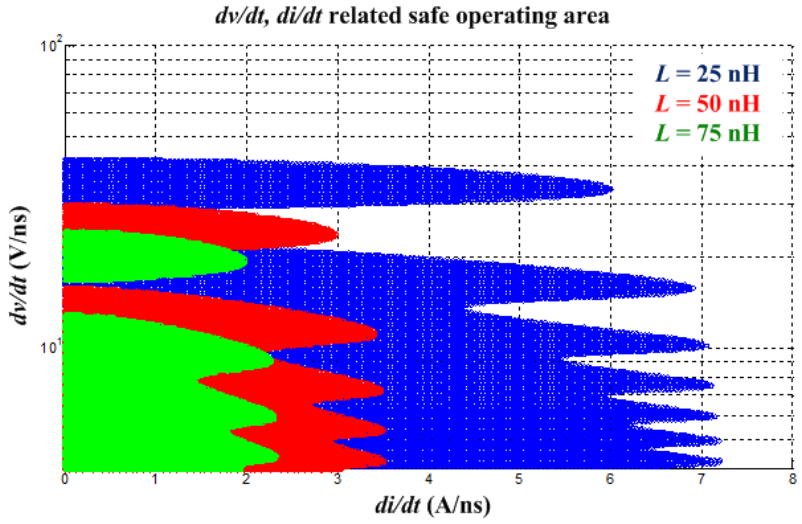
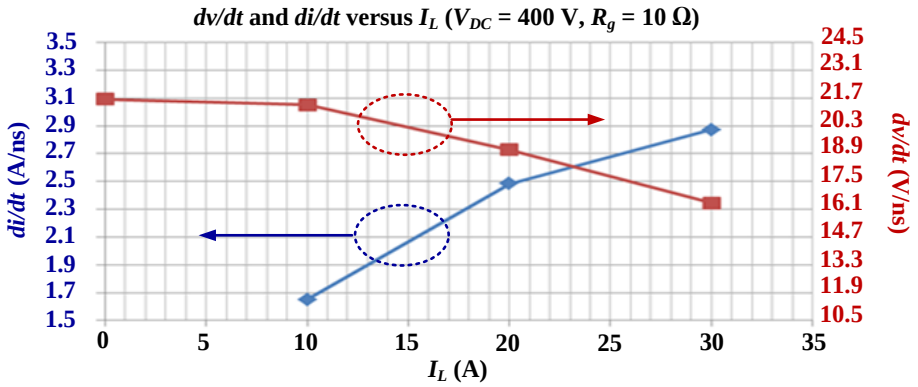
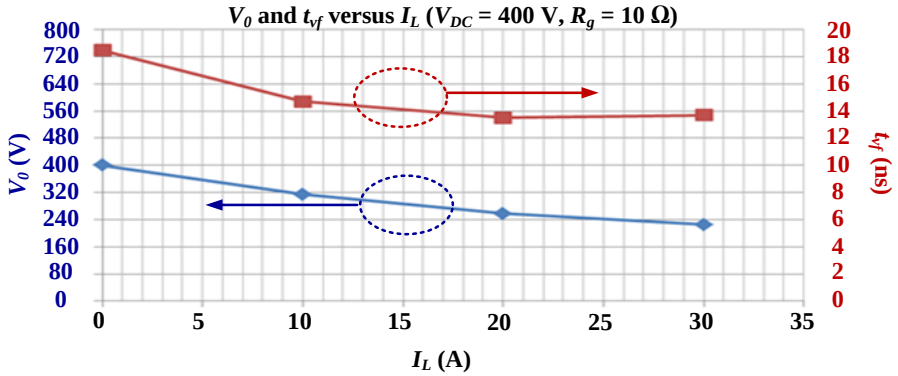


Fig. 4-17. Impact of power loop inductance on *dv/dt*, *di/dt* safe operating area for 1200-V/50-A Cree SiC MOSFET.

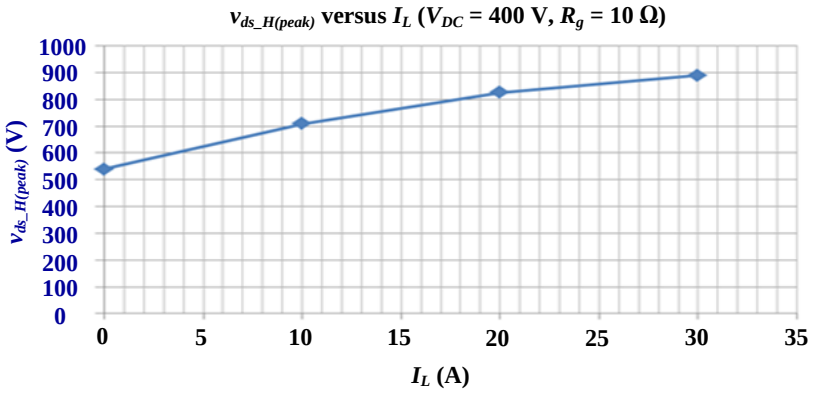
4.1.2.3 Experimental Verification



(a) *dv/dt* and *di/dt* dependence on I_L.



(b) V_0 and t_{vf} dependence on I_L.



(c) $v_{ds\_H(peak)}$ dependence on I_L.

Fig. 4-18. $v_{ds\_H(peak)}$ dependence on *dv/dt* and *di/dt* under different operating currents.

Based on Cree 1200-V/50-A SiC MOSFETs, Fig. 4-18 shows the test results of $v_{ds\_H(peak)}$ dependence on *dv/dt* and *di/dt* under different operating current. As I_L increases, *di/dt* becomes higher, leading to lower V_0. In the meantime, t_{vf} turns to be shorter. According to aforementioned theoretical analysis, both the lower V_0 and shorter t_{vf} cause the higher $v_{ds\_H(peak)}$, which can be verified by the test data in Fig. 4-18(c).

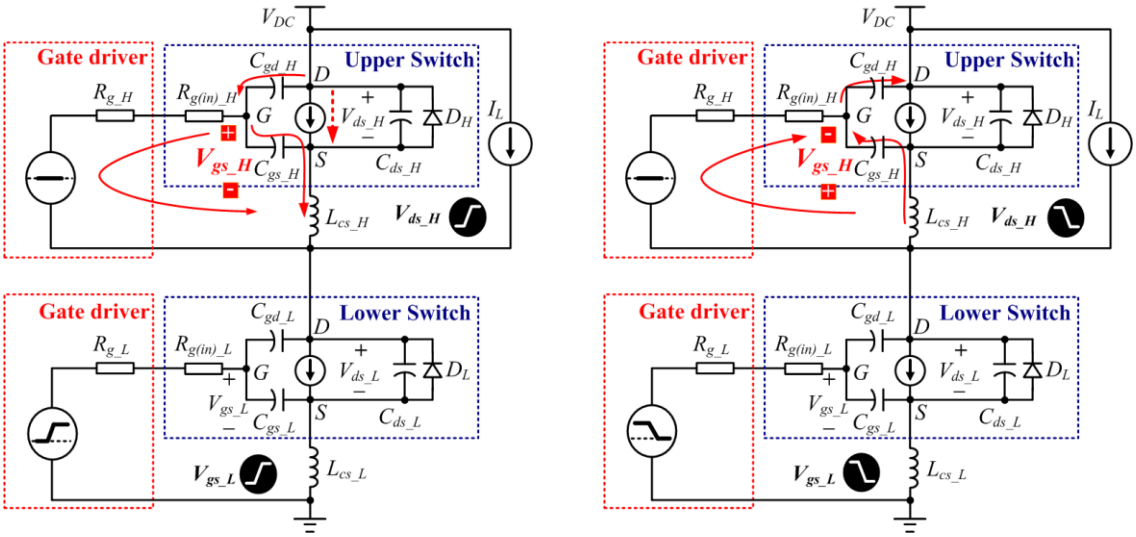
4.1.3 Cross-Talk

4.1.3.1 Mechanisms Causing Cross-Talk

In the phase-leg configuration, the switching process of the lower switch will affect the operation condition of the upper one, which in turn might worsen the switching performance of the lower switch and the reliability of upper switch. This interaction between the two switches is called cross-talk and illustrated in Fig. 4-19 [54].

During the turn-on transient of the lower switch, the drain-to-source voltage rise on the upper switch induces a current that is coupled through its Miller capacitance C_{gd_H}. This induced current generates a voltage drop across the gate resistance R_{g_H}. If this positive spurious gate voltage exceeds the threshold voltage of the upper switch, the upper switch will partially turn on. As a result, a shoot-through current will flow from the upper switch to the lower one, leading to excessive switching losses in both switches. Meanwhile, based on the transfer characteristics of power devices, this additional shoot-through current will increase the channel current of the lower switch, affecting the gate voltage. The increased gate voltage of the lower switch will reduce the gate current, resulting in the decrease of *dv/dt*. Thus, the turn-on switching speed of the lower switch would be limited by this self-regulating mechanism.

During the turn-off transient of the lower switch, similarly, a negative spurious gate voltage would be induced. This negative spurious gate voltage will not generate a shoot-through problem, but it may degrade the upper switch's reliability if its magnitude exceeds the maximum allowable negative biased gate voltage acceptable to the semiconductor device itself.



(a) Turn-on transient of lower switch. (b) Turn-off transient of lower switch.

Fig. 4-19. Mechanism causing cross-talk interference.

Consequently, in order to mitigate cross-talk, the fast switching speed capability of power devices in the phase-leg has to be sacrificed. Based on the aforementioned analysis, the core element of cross-talk is the spurious gate voltage of the upper switch. The peak value of this spurious gate voltage is shown as [113-115],

$$v_{gs\_H(\max)} = \frac{dv}{dt} \times R_{g\_H} C_{gd\_H} \times \left(1 - e^{-\frac{V_{DC}}{\frac{dv}{dt} \times C_{iss\_H} R_{g\_H}}}\right) \tag{4-12}$$

where *dv/dt* is the slew rate of drain-to-source voltage of the lower switch, partially representing the switching speed. R_{g_H}, C_{gd_H} and C_{iss_H} refer to the gate resistance, Miller capacitance and

input capacitance of the upper switch. Thus, *dv/dt*, R_{g_H}, C_{gd_H}, C_{iss_H} and V_{DC} determine the peak value of spurious gate voltage of upper switch.

Table 4-1. Characteristics of Several Comparable Si/SiC Power Devices [116-120]

Type	Manufac-turer	Model	V_{DS} / I_D (100 °C)	$V_{gs(th)}$ (25 °C)	$V_{gs\_\max(-)}$	$R_{g(in)}$
TFS Si IGBT	Fairchild	FGA20N120FTD	1200-V / 20-A	5.9 V	−25 V	N/A
NPT Si IGBT	IR	IRG4PH505	1200-V / 33-A	4.5 V	−20 V	1.6 Ω
Si MOSFET	Micro-semi	APT34M120J	1200-V / 22-A	4.0 V	−30 V	N/A
SiC MOSFET	CREE	CMF20120D	1200-V / 24-A	2.5 V	−5 V	5 Ω
SiC JFET	Semisouth	SJEP120R100	1200-V / 17-A	1.0 V	−15 V	6 Ω

According to the inherent properties, SiC devices in a phase-leg configuration are easily affected by cross-talk due to the following reasons: 1) fast switching-speed, which results in high *dv/dt*; 2) relatively large internal gate resistance $R_{g(in)}$, which increases resistance associated in the gate loop ; 3) lower threshold voltage $V_{gs(th)}$, enabling the positive spurious gate voltage easily incurs shoot-though failure during turn-on; 4) lower maximum allowable negative gate voltage $V_{gs\_\max(-)}$, allowing the negative spurious gate voltage easily overstress the gate-source terminals of power devices during turn-off. Table 4-1 lists the comparison of $R_{g(in)}$, $V_{gs(th)}$, and $V_{gs\_\max(-)}$ between SiC devices and their Si counterparts.

4.1.3.2 Experimental Verification

Based on the EPC2001 GaN transistor, Fig. 4-20 to Fig. 4-23 show the impact of C_{gd_H}, dv/dt, R_{g_H} and V_{DC} on spurious v_{gs_H} induced by cross-talk, respectively. Among them, Fig. 4-20 is the simulation result that shows the impact of Miller capacitance of power devices C_{gd_H} on switching behavior, since it hard to regulate in the experiment. Experimental results focusing on the influence of dv/dt, R_{g_H}, and operating conditions on cross-talk and switching speed are shown in Fig. 4-21 to Fig. 4-23.

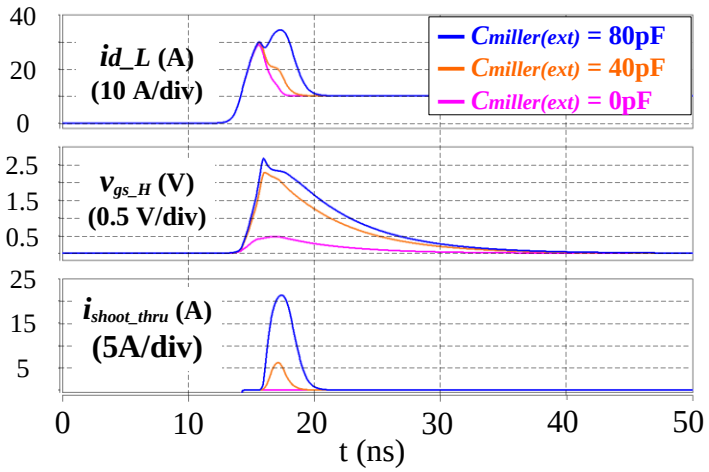
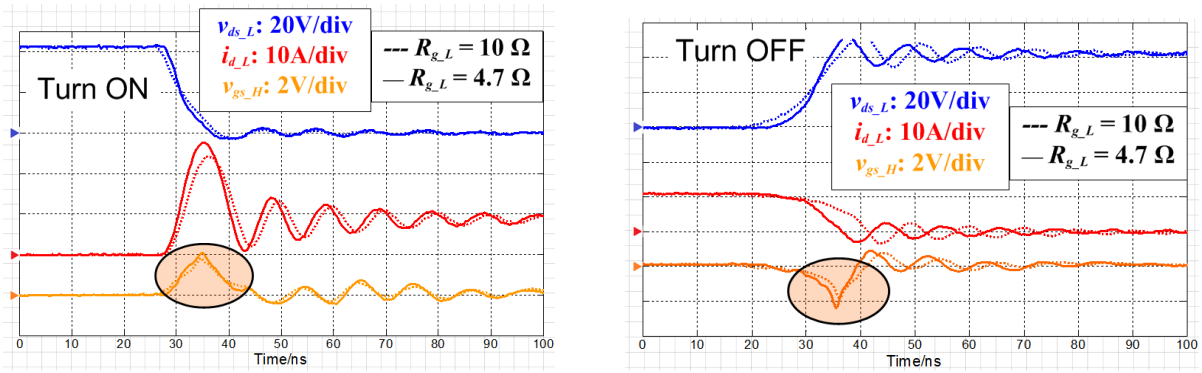


Fig. 4-20. V_{gs_H} dependence on C_{gd_H}.

In Fig. 4-20, large C_{gd_H}, determined by the external capacitor placed in parallel with the Miller capacitor of the upper switch, increases the peak value of v_{gs_H}, leading to large shoot-through current flowing into the lower switch.



(a) Turn-on transient. (b) Turn-off transient.

Fig. 4-21. v_{gs_H} dependence on switching speed (controlled by R_{g_L}).

In Fig. 4-21, *dv/dt* is controlled by changing the value of R_{g_L}, and R_{g_H} remains constant. It shows that higher *dv/dt* induces higher positive v_{gs_H} during the turn-on transient and lower negative v_{gs_H} during the turn-off transient under the operating condition of 40-V/10-A. Fig. 4-22 presents the impact of R_{g_H} on cross-talk, and corresponding experimental data are listed in Table 4-2. It shows that with the same R_{g_L}, larger R_{g_H} induces more serious cross-talk, resulting in larger i_{d_L}, longer t_{on} and more E_{on}. In this case, R_{g_L} is 10 Ω. Generally, R_{g_H} should also set to be 10 Ω. However, in comparison with R_{g_H} of 0 Ω, the cross-talk with R_{g_H} of 10 Ω would increase t_{on} from 10.4 ns to 12.4 ns, and E_{on} from 6.23 µJ to 6.96 µJ. Therefore, cross-talk limits the switching speed and worsens the switching performance of power devices in the phase-leg configuration. Fig. 4-23 presents v_{g_H} and i_{d_L} under different operating voltage in the unified coordinates. Higher V_{DC} induces higher v_{g_H} (orange curve), resulting in large shoot-through current (red curve). Meanwhile, the impact of R_{g_H} on cross-talk is verified as well.

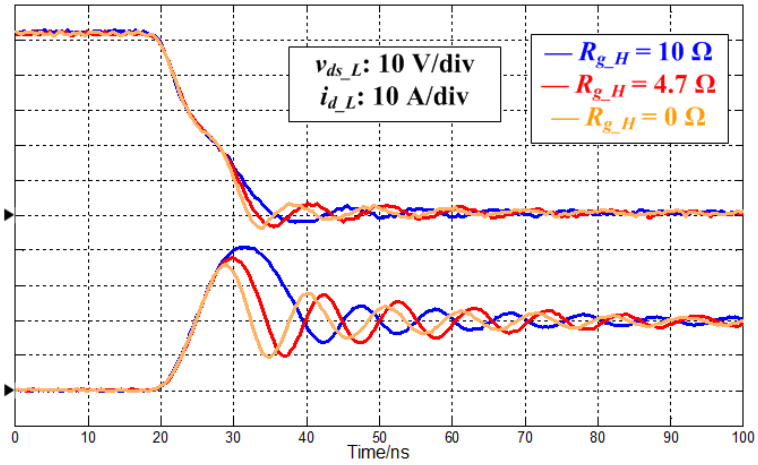


Fig. 4-22. v_{gs_H} dependence on R_{g_H}.

Table 4-2. Impact of R_{g_H} on Turn-on Switching Behavior

R_{g_H} (Ω)	t_{on} (ns)	E_{on} (μJ)	dv/dt (V/ns)	di/dt (A/ns)
10	12.4	6.96	3.32	4.05
4.8	11.2	6.30	3.68	4.15
0	10.4	6.23	3.88	4.00

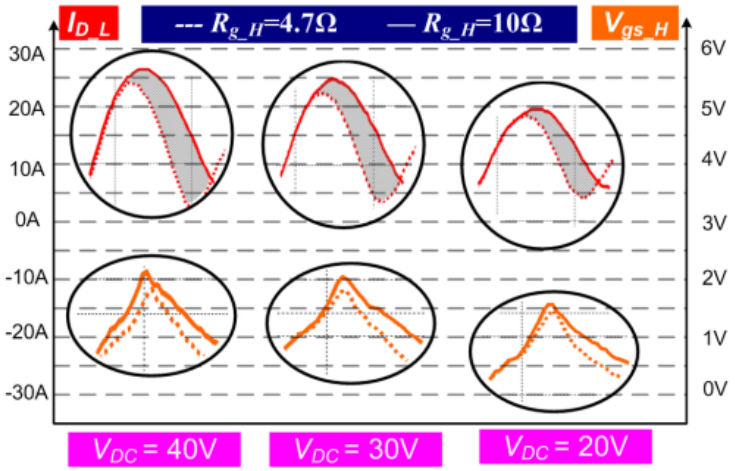


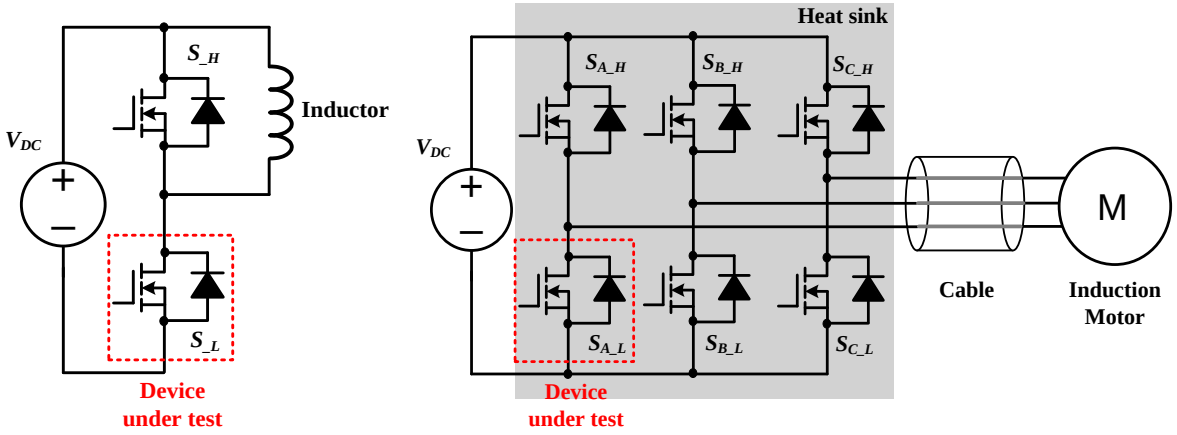
Fig. 4-23. v_{gs_H} dependence on R_{g_H}, V_{DC} and induced shoot through current (shadow area).

4.2 Impact Factors in Three-phase Voltage Source Converter

The aforementioned impact factors focus on the phase-leg configuration. In the meanwhile, as the widely accepted method to assess the switching performance of power devices, the double pulse test (DPT) circuit is a phase-leg as well. It seems that the switching performance of power devices can be accurately evaluated via DPT in a phase-leg. Maybe this is true to the slow Si devices, but not anymore for fast switching SiC devices. Due to intrinsic characteristics of SiC devices, such as small junction capacitance, small specific on-resistance, and high *di/dt* and *dv/dt* during fast switching transients, their switching behavior becomes more susceptible to parasitics and noise of the application circuit, compared with slower Si devices. Thus, the simple and layout-optimized double pulse tester with an optimally-designed load inductor in the phase-leg configuration may not sufficiently represent a more complex configuration of actual converters and loads.

Therefore, the switching performance of a SiC based three-phase voltage source inverter for motor drives need to be systematically evaluated as compared to the switching behavior in DPT. As shown in Fig. 4-24, there are three primary differences between the configuration of a three-phase voltage source inverter and a double pulse tester: different inductive loads, two more phase-legs for inverter, and cooling systems (e.g., heat sink). Accordingly, first, the high frequency impedances of an induction motor and the optimally-designed inductor employed in double pulse tester is compared. The resulting switching behavior differences are analyzed. Second, the impact of the other two phase-legs on the switching performance of the phase-leg under test is described for the three-phase voltage source inverter. Third, the parasitic capacitive coupling effect between power devices and heat sink, and its influence on the switching performance, is discussed for motor drives. Finally, for experimental verification, the switching performance of

Cree 1200-V/24-A SiC MOSFETs is evaluated under pulse test and continuous operating condition in a three-phase voltage source inverter connected to an induction motor.



(a) DPT circuit. (b) Three-phase voltage source inverter fed motor drives.

Fig. 4-24. Configuration comparison between double pulse tester and three-phase voltage source converter.

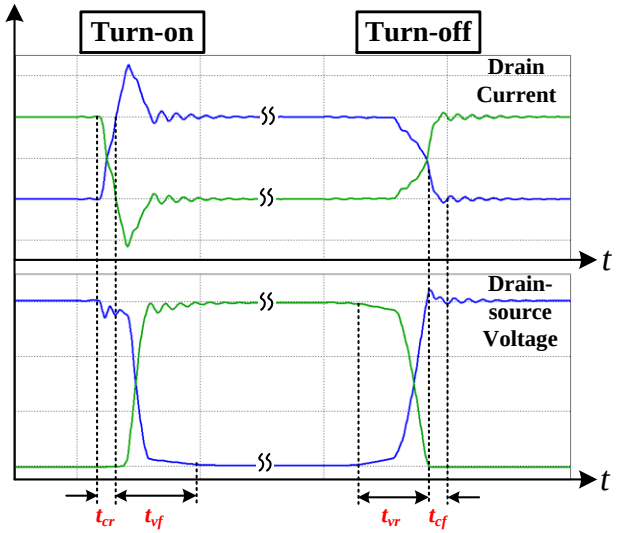


Fig. 4-25. Typical switching current /voltage waveforms.

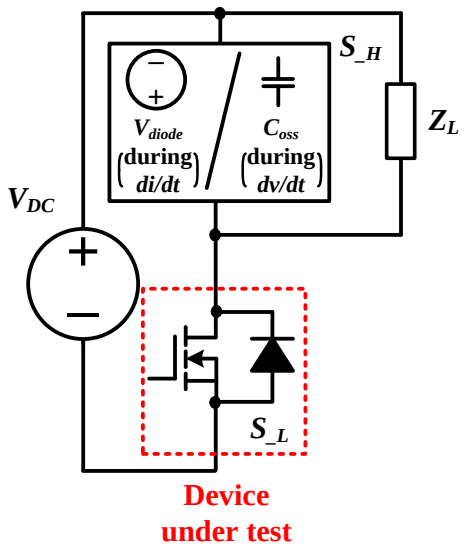


Fig. 4-26. Simplified DPT circuit.

4.2.1 Parasitics of Inductive Load

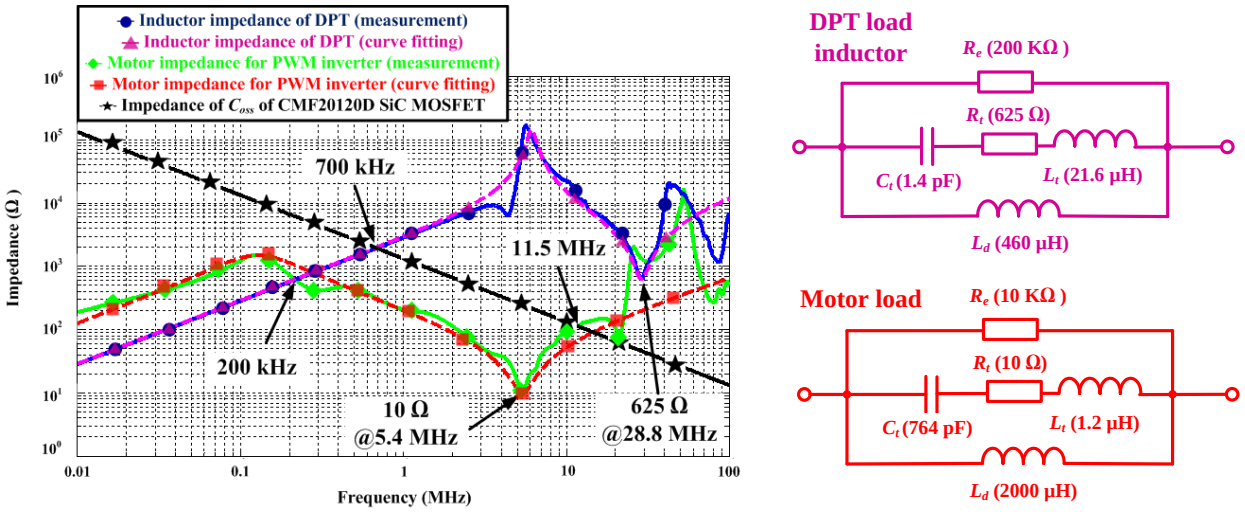
As can be observed in Fig. 4-24(a), the load inductor of the DPT circuit is paralleled with the upper switch, assuming the lower switch is selected as the device under test (DUT). During the switching transient, the upper switch stays off, and can be modeled as a conducting diode when the switching current is commutating (i.e., current rise subinterval t_{cr} during the turn-on transient and current fall subinterval t_{cf} during the turn-off transient in Fig. 4-25) or an output capacitance while the switching voltage is changing (i.e., voltage fall subinterval t_{vf} during the turn-on transient and voltage rise subinterval t_{vr} during the turn-off transient in Fig. 4-25). Thus, the DPT circuit can be redrawn as Fig. 4-26, where Z_L represents the inductive load impedance. If Z_L is much greater than the equivalent impedance of the upper switch during the switching transient, then the impact of inductive load on the switching performance can be neglected; otherwise, Z_L must be taken into consideration. For the specific analysis of the comparisons between DPT load inductor and induction motor load, four 115 μH inductors in series are

employed to form a DPT load inductor, which is a typical way of designing DPT load inductor with small parasitic capacitance; a 7.5 kW induction motor and 2-meter power cable are selected as the representative of the motor load since it is a proper load in terms of power rating for the SiC devices under evaluation (Cree CMF20120D 1200-V/24-A SiC MOSFETs). In addition, for the higher power rating induction motor with longer power cable in many practical applications, the associated impedance Z_L at high frequency becomes lower [121]. Thus, the motor load selected in this case study indicates a conservative impact of induction motor on the switching performance. Then the generality of the following analysis is not lost.

4.2.1.1 Impact of Induction Motor on Switching Performance

As illustrated in Fig. 4-26, during the switching current commutation subinterval, the impedance of the upper switch is extremely small since it can be considered as a voltage source. During the switching voltage change subinterval, the impedance of the upper switch depends on the output capacitance of the device. Normally, the equivalent impedance of the upper switch is also small in the switching-related frequency range that is determined by the switching speed [122]. Typically, the frequency range is several MHz to tens of MHz for SiC devices considering switching intervals of tens of nanoseconds.

In the typical DPT, the load inductor during a switching transient can be approximated as a current source. Ideally, due to the infinite impedance of the current source during this dynamic process, the load inductor has no impact on the switching behavior of the DUT. Practically, the load inductor of the DPT is optimally-designed so that its parasitics, such as equivalent parallel capacitance (EPC), are very small [35], making the load inductor impedance much larger than the upper switch equivalent impedance at frequencies of interest with respect to the switching transition. Therefore, the load inductor has little effect on the switching performance in the DPT.

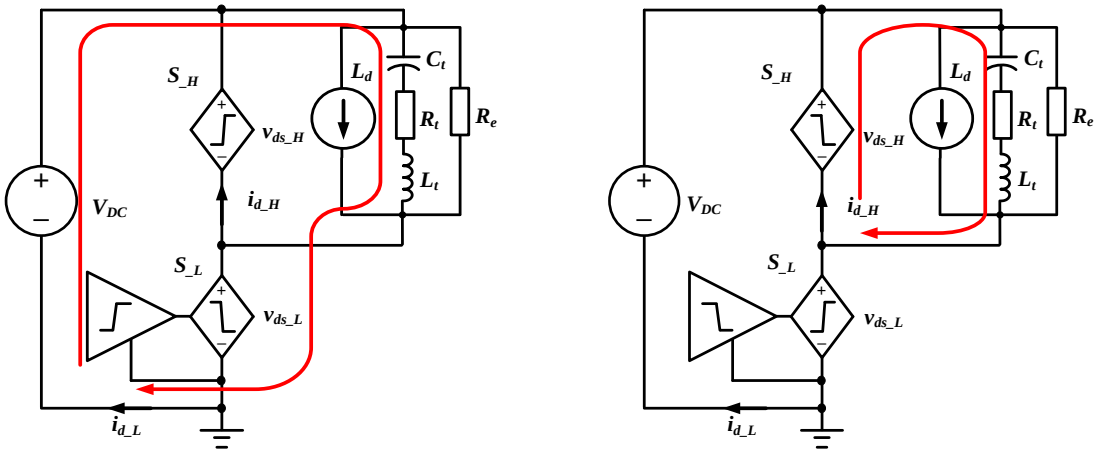


(a) Impedance of inductive loads vs. C_{oss} of SiC device. (b) Circuit model of inductive loads.

Fig. 4-27. Impedance and circuit model of inductive loads.

However, in adjustable speed drive systems, the parasitics of the induction motor cause its high frequency impedance to be significantly decreased, as shown in Fig. 4-27(a). Measured using the Agilent 4294A impedance analyzer, the impedance of the DPT load inductor is greater than the induction motor equivalent impedance above 200 kHz, although the DPT load inductance is smaller than the induction motor inductance. In addition, the measured induction motor impedance in our example system is even smaller than the equivalent impedance of the SiC device used in this case (Cree CMF20120D SiC MOSFET) below 11.5 MHz. Note the device equivalent impedance is mainly determined by its output capacitance and the Cree device has an output capacitance of 120 pF [119]. On the contrary, above 700 kHz, the DPT load impedance is greater than the device's impedance due to its output capacitance. Consequently, the induction motor will play a significant role in the switching behavior of the DUT due to the small motor impedance at high frequencies. Also, it is important to note that, SiC has smaller

output capacitance than its Si counterpart, resulting in higher equivalent impedance and making the SiC switching behavior more susceptible to the parasitics of the induction motor.



(a) Turn-on transient. (b) Turn-off transient.

Fig. 4-28. Impact of parasitics of induction motor on switching current.

Based on the measured impedance, circuit models of the DPT load inductor and motor load are built, as shown in Fig. 4-27(b) following the methods in [121, 123-125]. Each parameter in the circuit model has physical meaning and significance. L_d refers to the stator winding leakage inductance; R_e represents the high-frequency iron loss of the stator winding; L_t C_t and R_t are introduced to capture the second resonance in the motor impedance characteristics, according to [125], that may be caused by the skin effect and turn-to-turn capacitance of the stator windings. As can be observed in Fig. 4-27(a), the fitted curves of the inductive load impedance based on the circuit models can represent the critical characteristics of the motor and DPT impedances. During the switching transient, the large inductance L_d can be modeled as a current source, as shown in Fig. 4-28. It is the series resonant network formed by L_t, C_t and R_t that affects the switching performance. Compared with the DPT load inductor with extremely small parasitic

capacitance C_t (1.2% C_{oss} of SiC MOSFET under evaluation) and large damping resistance R_t (625 Ω), the parasitic capacitance C_t of the induction motor is 6 times that of C_{oss} of the SiC MOSFETs, and its corresponding damping resistance R_t (10 Ω) is relatively small. Therefore, in the time domain, considering the high *dv/dt* drain-source voltage of the upper switch V_{ds_H} across the *LRC* series resonant network, the induction motor with large C_t and small R_t causes more serious parasitic ringing with longer duration. This parasitic ringing causes additional resonant current to flow in the switching commutation loop. Thus, the switching performance of the lower switch is affected. Unlike the typical high frequency parasitic ringing (typically tens of MHz) due to the resonance between the power loop inductance and C_{oss} of power devices, the ringing caused by parasitics of the induction motor has relatively low frequency with 5.4 MHz in this case study (see Fig. 4-27(a)). Also, this lower frequency ringing will be observed in the drain current of the lower switch during the turn-on transient and drain current of the upper switch during the turn-off transient, as illustrated in Fig. 4-28.

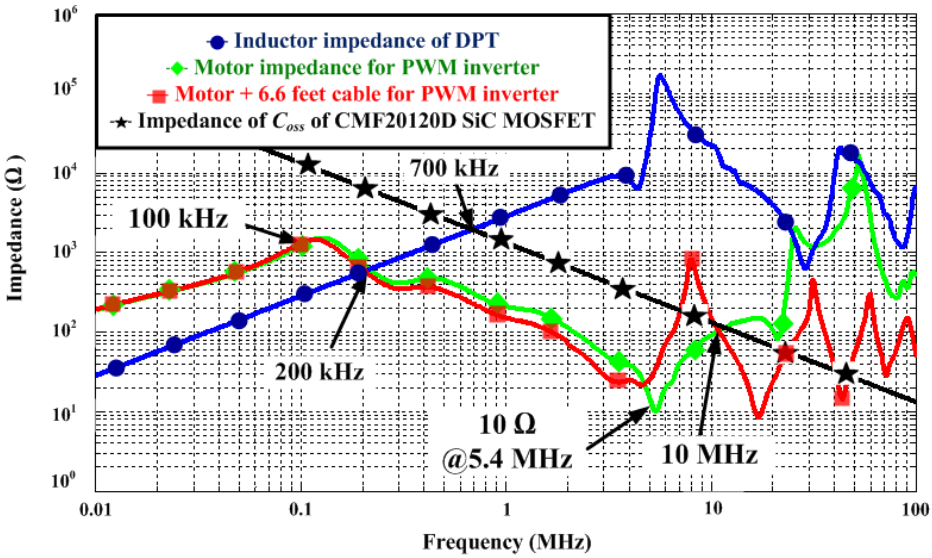


Fig. 4-29. Impedance of induction motor with 2 meters cable vs. induction motor.

4.2.1.2 Impact of Induction Motor with Power Cable on Switching Performance

Induction motor drive systems fed with a power cable are widely used in many industrial applications. It is therefore necessary to evaluate the impact of an induction motor with a power cable on the switching performance. Fig. 4-29 displays the impedance comparison between the induction motor and the induction motor with 2-meter power cable. The impedances of the induction motor and the induction motor plus power cable are identical below 100 kHz, but significant differences occur at high frequency. Especially above 10 MHz, the impedance of the induction motor with power cable is smaller than that of the induction motor, and is even comparable to the impedance of the SiC MOSFET's C_{oss}. Based on the aforementioned analysis in the frequency domain, more serious impact on switching performance can be expected of the induction motor with power cable. Also, since the cable length in practical applications is generally much longer than the 2 meters length used in this case study, more attention must be paid to the power cable's impact. In the time domain, due to the complicated model of power cable with distributed *LC* networks, it is difficult to illustrate the precise relationship between the power cable and the switching behavior based on a high-order circuit model. Generally, the capacitive coupling among the conductors of the power cable extends the charging/discharging subinterval during switching transients, leading to lower *dv/dt*, longer switching time, and larger switching losses.

4.2.2 Interaction of Phase-legs

As can be observed in Fig. 4-24, as compared to double pulse tester consisting of only one phase-leg, a three-phase PWM inverter has two additional phase-legs. Thus, additional device and interconnection parasitics will be involved in the circuit. Assuming the upper switches of phase B and C are in on-state while their lower switches in off-state during the switching

transients of the phase A devices, Fig. 4-30 displays the equivalent circuit of a three-phase PWM inverter considering the parasitics, where the upper switches of phase B and C are represented by their on-state resistance $R_{ds(on)}$, and the junction capacitance C_{oss} represents the lower switches of phase B and C. Also, $L_{p(in)}$ is the power loop parasitic inductance within each phase-leg, while $L_{p(ext)}$ is the parasitic inductance distributed in the dc bus. Z_{LA}, Z_{LB} and Z_{LC} are the impedances of the inductive load of each phase.

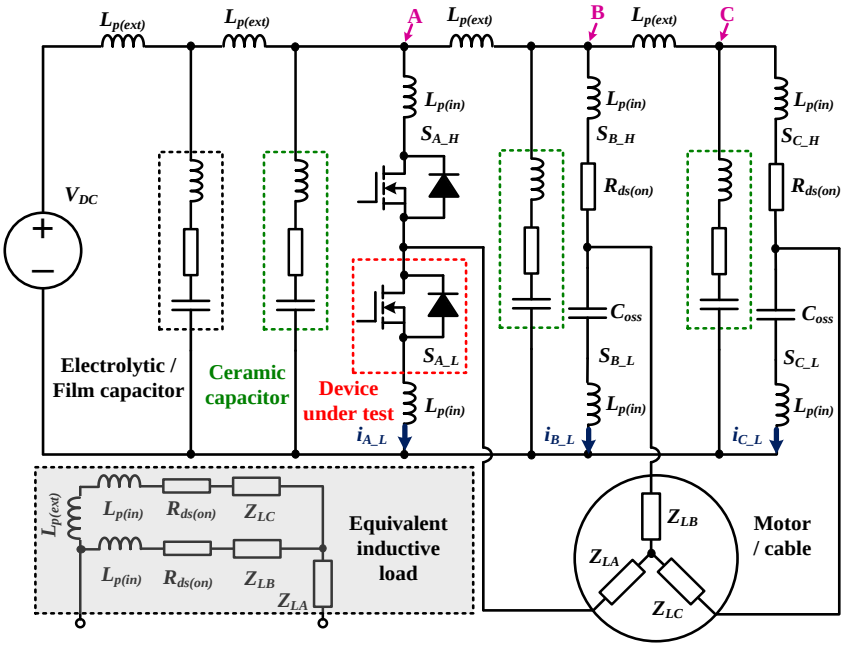


Fig. 4-30. Equivalent circuit of three-phase PWM inverter considering the parasitics.

As can be observed in Fig. 4-30, the equivalent inductive load consists of parasitic inductance, on-state resistance, and three-phase inductive loads. Considering the relatively small parasitic inductance (i.e., $L_{p(in)}$,$L_{p(ext)}$) and the small $R_{ds(on)}$ of SiC devices in comparison with the impedance of inductive loads (Z_{LB}, Z_{LC}), the impact of parasitics induced by the upper switches of phase B and C on the inductive loads can be negligible. In addition, the potentials at node B

and C will almost stay constant during the switching transient of the phase-A DUT due to the existence of ceramic capacitors with small equivalent series inductance (ESL) utilized as decoupling capacitors mounted close to each phase-leg in practical applications. Therefore, for the lower switches of phase B and C, the voltages across C_{oss} have little variation so that the switching performance of the DUT is hardly affected by the lower switches of phase B and C.

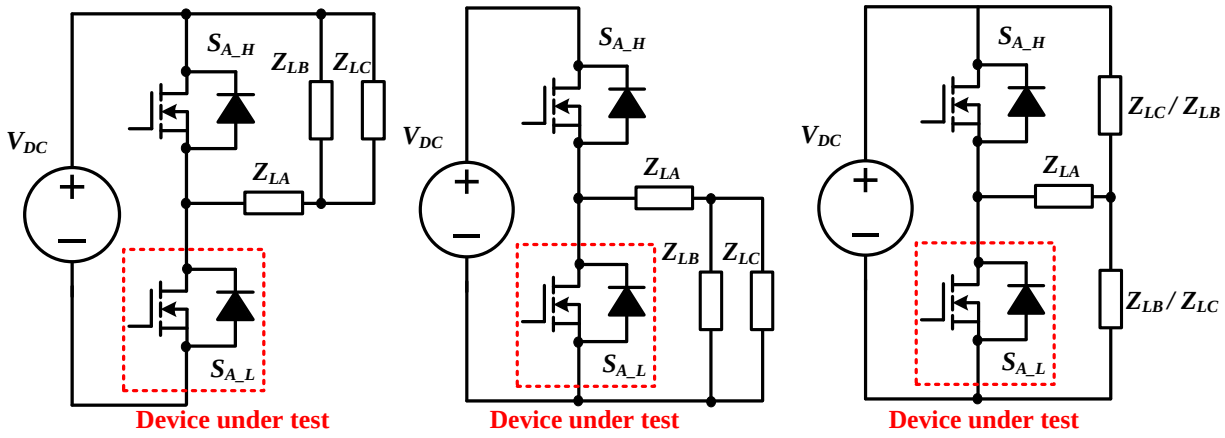


Fig. 4-31. Connection structures of inductive loads according to different sections of space vector modulation.

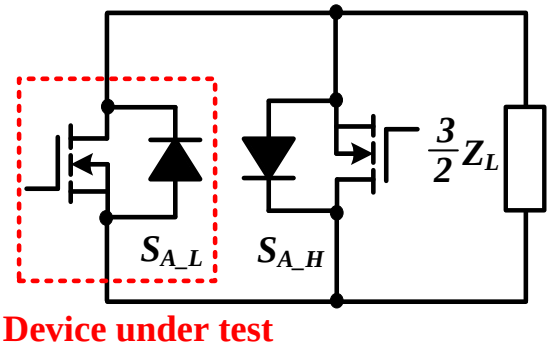


Fig. 4-32. Uniform equivalent circuit considering constant dc bus voltage thanks to decoupling capacitors.

In addition to the parasitics induced by phase B and C, the on/off states of switches in the other phase-leg alter the connection structure of inductive loads with respect to the phase-leg under test. Therefore, different from a fixed inductive load position within the DPT, the tested device in a three-phase voltage source inverter during the commutation interval will see different combinations of the inductive loads. According to the on/off states of the phase B and C switches, based on the space vector modulation scheme, there are three connection structures of inductive loads with respect to phase A during a switching transient, as shown in Fig. 4-31. Fortunately, as previously mentioned, the dc bus voltage during the switching transient stays nearly constant thanks to the decoupling capacitors close to each phase-leg. Hence, according to circuit theory, the dc bus voltage source is shorted during the dynamic process analysis. Assuming the impedances of inductive loads for all phases are identical and denoted by Z_L, three different circuits in Fig. 4-31 can be simplified as a uniform equivalent circuit, as shown in Fig. 4-32. Consequently, different connection structures due to the switching states of phase B and C have little effect on the switching performance of phase A devices in practical applications.

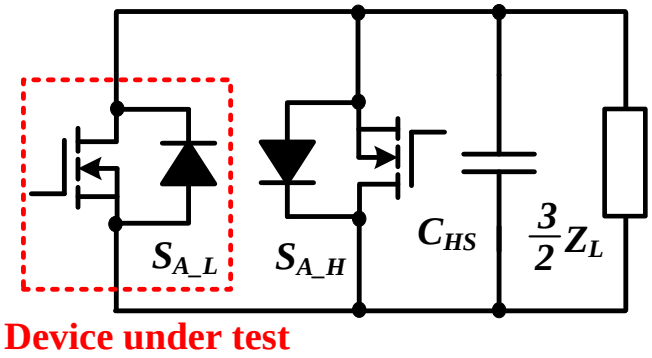


Fig. 4-33. Uniform equivalent circuit considering capacitive coupling effect induced by heat sink.

4.2.3 Coupling Effect by Heat Sink

In a three-phase PWM inverter, SiC devices are attached to a heat sink for thermal management. Usually, a thin layer of insulating material is used to separate the SiC devices from the electrically conductive heat sink. Thus, a parasitic capacitance is formed between the drain base plate of the SiC devices and the common heat sink plate [33]. In the end, this capacitance C_{HS} is paralleled with devices, which equivalently increases their effective C_{oss}. However, in a motor drives in this study, in addition to the coupling capacitance between devices and heat sink, the parasitics of the induction motor is paralleled with devices as well, as shown in Fig. 4-33. Compared with the motor parasitic capacitance C_t (764 pF in Fig. 4-27(b)), the coupling capacitance (39.75 pF based on our test setup) is only 5.2% of C_t. Therefore, the capacitive coupling effect is insignificant when evaluating the switching performance of SiC MOSFETs in an motor drive system with relatively large capacitive parasitics.

4.2.4 Experimental Verification

4.2.4.1 Hardware Setup

To evaluate the influence of the aforementioned impact factors in Section 4.2.1- 4.2.3, a three-phase voltage source inverter test circuit was designed to satisfy the following requirements: 1) sufficient flexibility such that the three-phase voltage source inverter can be evolved from a layout-optimized double pulse tester; 2) during this design evolution, the layout associated with the DUT must remain consistent; and 3) a common heat sink is used for all power devices. Fig. 4-34 displays a three-phase voltage source inverter with Cree 1200 V CMF20120D SiC MOSFETs, including one uniform mother board, six gate drive daughter boards integrated with devices, and one common heat sink. Hence, a DPT configuration can be

achieved by means of merely connecting the gate drive boards of phase A with the mother board. In addition, a three-phase PWM inverter can be assembled with all six gate drive boards of three phase-legs mounted to the mother board. Also, using the lower switch of phase A as the DUT, it can be observed that the layouts of both the power and gate loop for the DUT under either DPT configuration or inverter circuit are nearly the same.

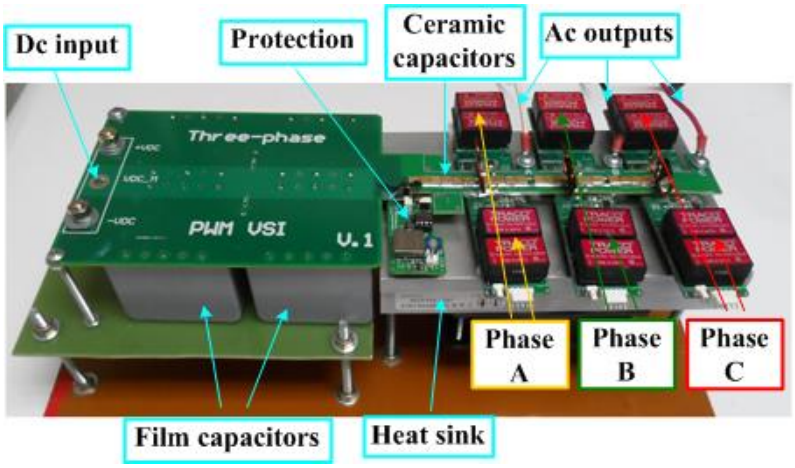
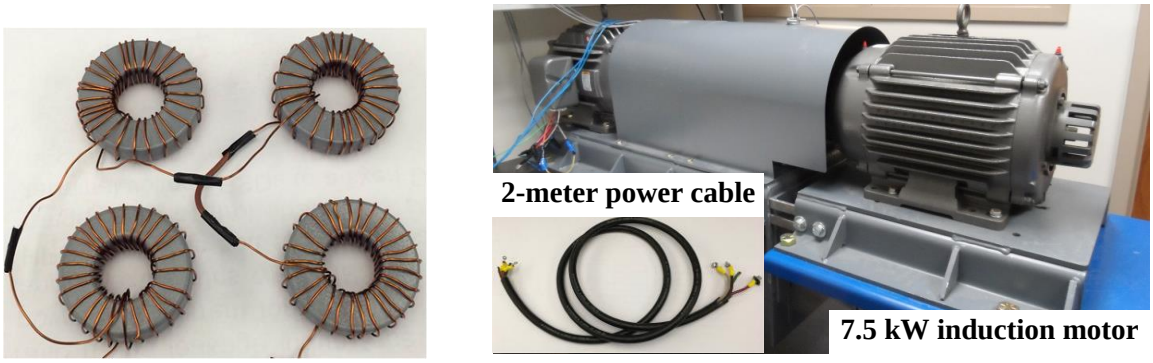


Fig. 4-34. SiC based three-phase voltage source inverter.



(a) DPT load inductor. (b) 7.5 kW induction motor with 2-meter power cable.

Fig. 4-35. Different inductive loads.

Fig. 4-35 displays two types of inductive loads: DPT load inductor and a 7.5 kW induction motor with a 2-meter power cable for evaluation of the difference in switching performance for double pulse tester and motor drive conditions. Note that the DPT load inductor consists of four small inductors in series to minimize parasitics. For the fast transient measurement, the following equipment is used to detect the switching waveforms: a digital oscilloscope (Tektronix DPO 401) with frequency bandwidth of 1 GHz and maximum sampling rate of 5 GS/s, two THDP0200 high voltage differential probes with frequency bandwidth of 200 MHz for drain-source voltage measurement of the upper and lower switches in a phase-leg, and two TCP0030A current probes with frequency bandwidth of 120 MHz for drain current measurement of the upper and lower switches in a phase-leg.

4.2.4.2 Methodology for Experimental Verification

A four-step verification procedure has been devised, that starts with the double pulse tester and ends with the three-phase PWM inverter fed induction motor drive. Each step will now be described.

1) Evaluation of the impact of different inductive loads on the switching performance. Here the gate drive boards of phase A are connected with the mother board to form a DPT circuit, and the switching performance of the phase A lower switch is tested with the optimally-designed load inductor, 7.5 kW induction motor, and 7.5 kW induction motor plus 2-meter power cable. As shown in Fig. 4-36, the switching performance differences in this step are only attributed to the inductive loads. For simplicity, PL-DPT, PL-IM, and PL-IM-PC refer to the test circuits with DPT load inductor, induction motor, and induction motor plus power cable, respectively.

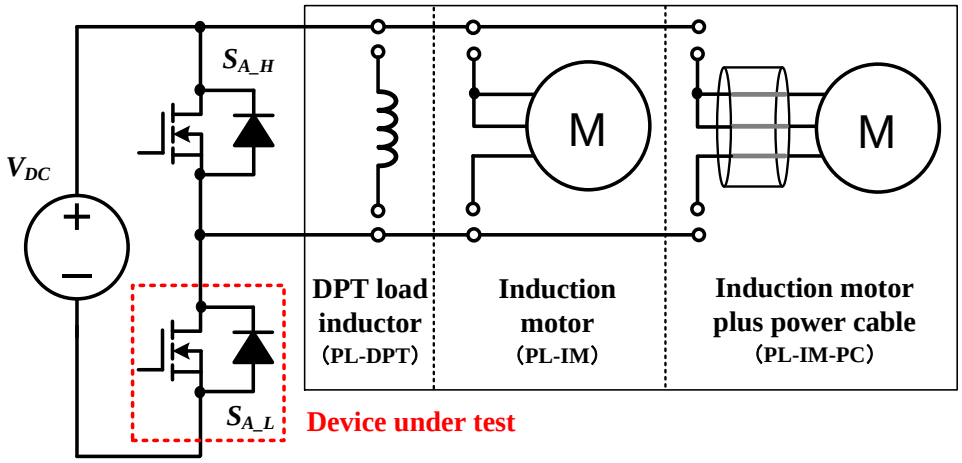
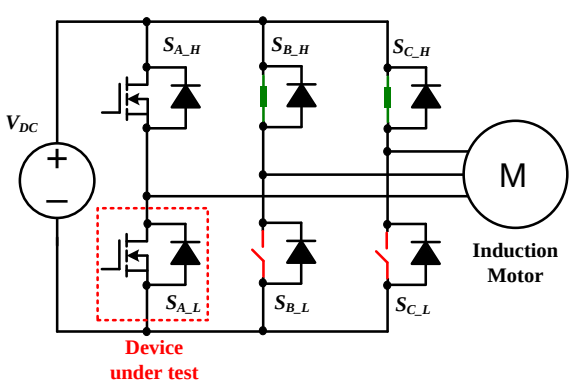
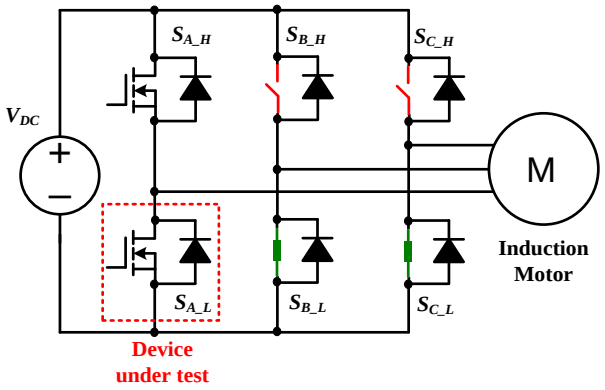


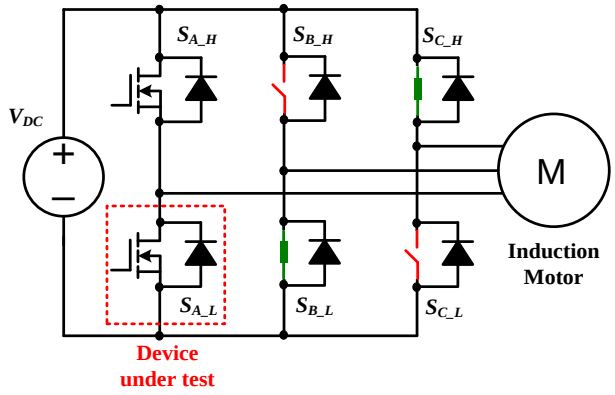
Fig. 4-36. Test circuits for evaluation of switching performance with different inductive loads.



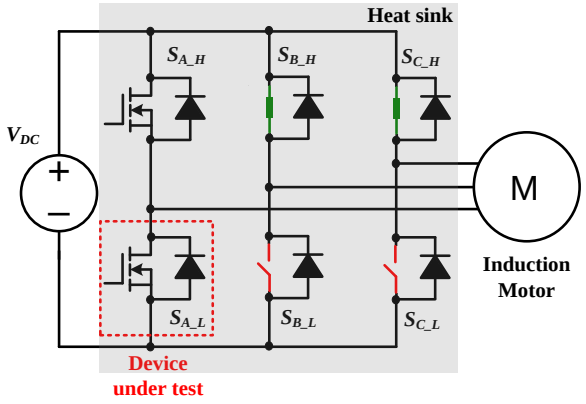
(a) 3Φ-IM-1.



(b) 3Φ-IM-2.



(c) 3Φ-IM-3.



(d) 3Φ-IM-HS-1.

Fig. 4-37. Test circuits for evaluation of the impact of phase-legs and heat sink on the switching performance.

2) Evaluation of the interaction of phase-legs on switching performance. The gate drive boards of phase B and C are added to the mother board to establish a three-phase inverter, and the switching performance of the DUT is tested by turning on the upper switches of phase B and C, as shown in Fig. 4-37(a). Hence, compared with the switching behavior of the DUT with the induction motor in step 1 (i.e., PL-IM), the impact of parasitics induced by phase B and C can be identified. Then, according to the modulation scheme, the switches of phase B and C are controlled in different on/off states during the switching transient of the DUT, as shown in Fig. 4-37(b) and (c), to evaluate the impact of different inductive load connection structures on switching performance. For simplicity, 3Φ-IM-1, 3Φ-IM-2, and 3Φ-IM-3 indicate the test circuits as shown in Fig. 4-37(a), (b), and (c), respectively.

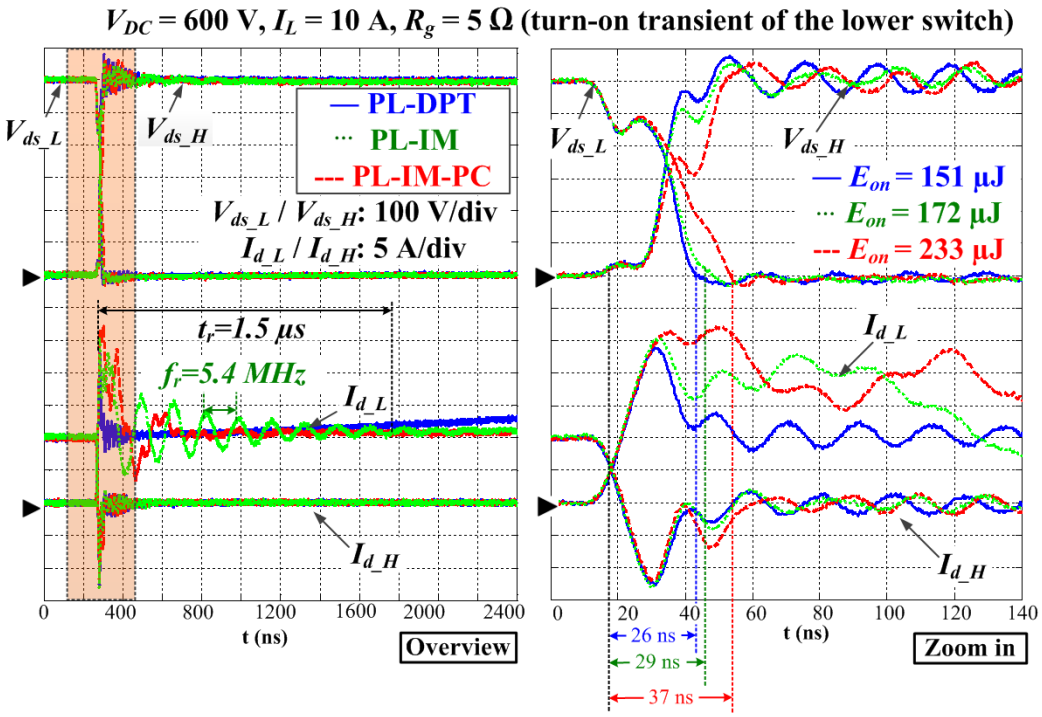
3) Evaluation of the impact of the heat sink on switching performance. A common heat sink is attached with all the power devices in the three-phase inverter, and the switching behavior of the DUT is tested by controlling the upper switches of phase B and C to be on, as shown in Fig. 4-37(d). Thus, in comparison with the switching performance of the DUT with the same on/off states of the switches of phase B and C in step 2 (i.e., 3Φ-IM-1), the capacitive coupling effect induced by the heat sink can be identified. For simplicity, 3Φ-IM-HS-1 represents the test circuits in Fig. 4-37(d).

4) Evaluation of the impact of the induction motor rotation on the switching performance. The switching behaviors in the previous three steps are evaluated based on pulse test, which means that the motor is not rotating, although certain pulse currents flow through the stator windings. In step 4, the switching performance of the DUT is tested when the induction motor is rotating. Based on the same hardware setup as in step 3, the difference of the switching performance under the motor running test and pulse test can be evaluated. Also note that the

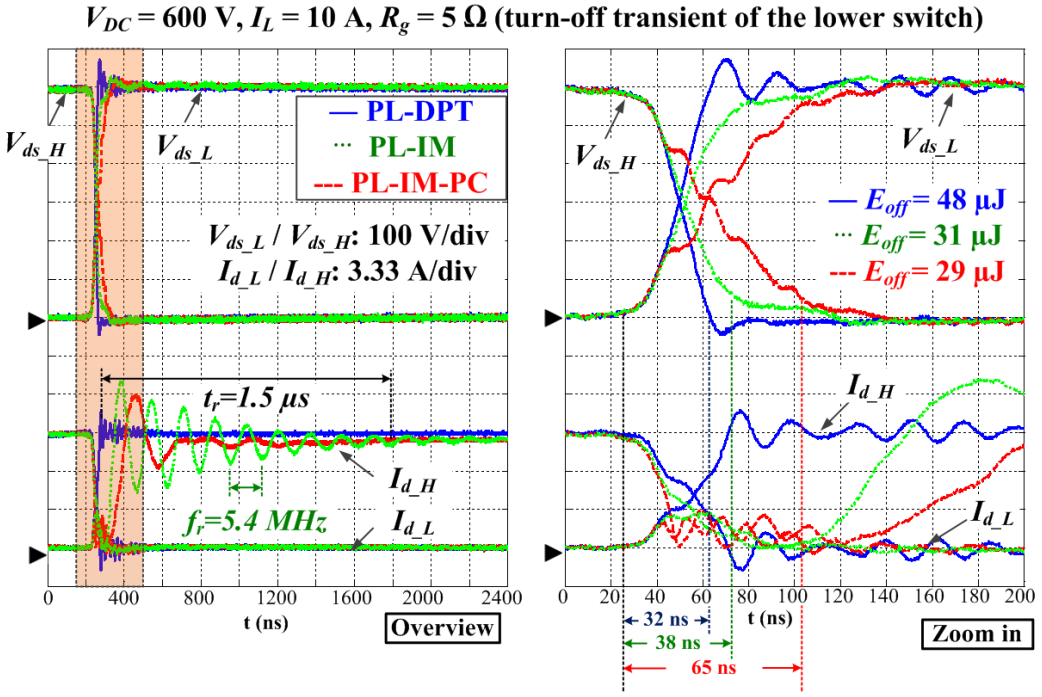
junction temperature variation of the DUT under the continuous operating condition will become another factor that impacts the switching behavior. In this test, the low switching frequency of 5 kHz and small ac RMS current of 11 A are selected to minimize active power loss. Also, the heat sink with forced air cooling is utilized for thermal management. Thus, the junction temperature rise of the DUT under no load operating condition for 1 to 2 minutes is insignificant.

4.2.4.3 Experimental Results

Fig. 4-38 shows the comparison waveforms with three different inductive loads under the operating condition of 600-V/10-A with 5-Ω gate resistance. As can be observed from the overall switching waveforms during both turn-on and turn-off transients, there is a 5.4 MHz frequency ringing in the switching current with the induction motor, which corresponds to the resonance frequency created by the parasitics of the induction motor (see Fig. 4-27). In addition, as predicted, during a turn-on transient, this low frequency ringing current is found from the drain current of the lower switch; while during a turn-off transient, it flows through the upper one. Also note that the ringing duration is up to 1.5 μs, which is much longer than the tens-of-nanoseconds' switching time, as shown in the zoomed-in switching waveforms. Furthermore, as compared to the switching behavior with the DPT load inductor, the parasitics of the induction motor cause the turn-on and turn-off switching time to increase from 26 ns to 29ns and 32 ns to 38 ns, respectively. The total energy loss slightly increases as well. After inserting a 2-meter power cable between the inverter and motor, the switching performance becomes worse: switching time increases up to 42% during turn-on, and doubles during turn-off; an additional 32% of energy loss is dissipated during the switching transient.

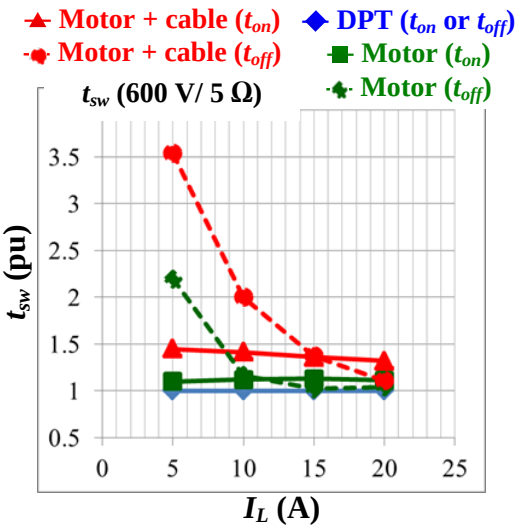


(a) Turn-on transient.

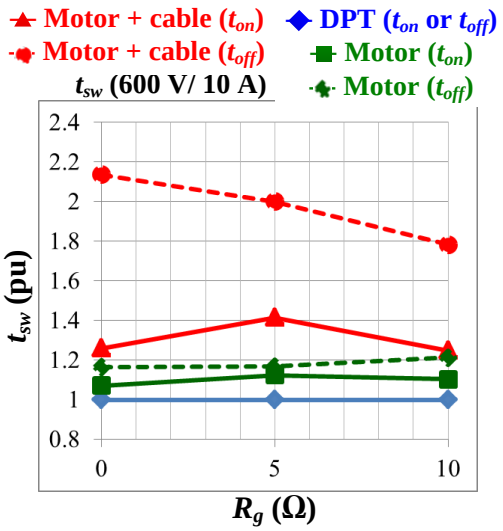


(b) Turn-off transient.

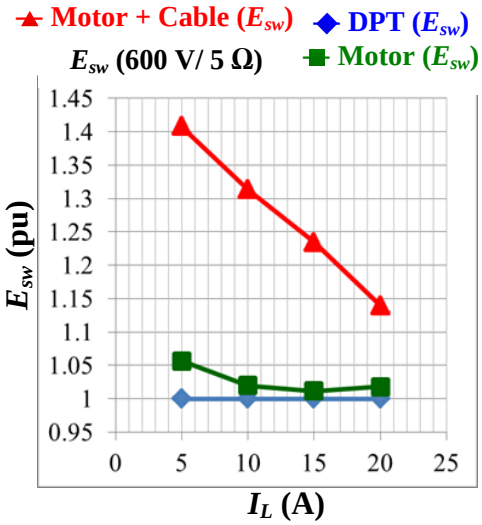
Fig. 4-38. Impact of different inductive loads on switching performance.



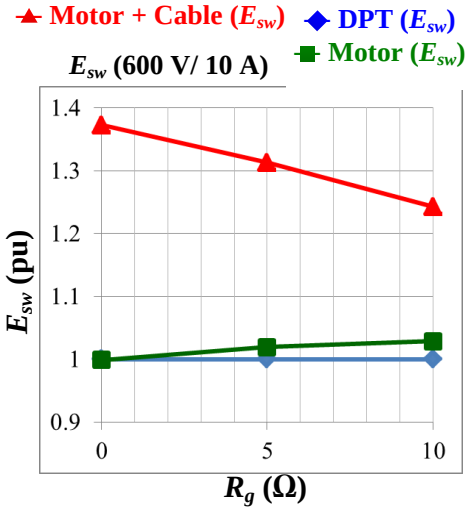
(a) t_{sw} dependence on I_L.



(b) t_{sw} dependence on R_g.



(c) E_{sw} dependence on I_L.



(d) E_{sw} dependence on R_g.

Fig. 4-39. Comparison of t_{sw} and E_{sw} among different inductive loads under different I_L and R_g.

More test results with different load currents and gate resistances are shown in Fig. 4-39. In order to clearly demonstrate the impact of different inductive loads on the switching performance, the switching time t_{sw} and energy loss E_{sw} with induction motor and motor plus power cable are

normalized based on results with DPT load inductor, which are listed in Table 4-3 and. These results show that under different load currents with varying gate resistances, t_{sw} and E_{sw} with either induction motor or induction motor plus power cable are increased compared to the test data with DPT load inductor. In addition, the impact of the induction motor plus power cable on the switching performance is more serious. All of the experimental data agree with the theoretical analysis in Section 4.2.1.

Table 4-3. t_{sw} & E_{sw} vs. I_L Under DPT with V_{DC} of 600 V & R_g of 5 Ω

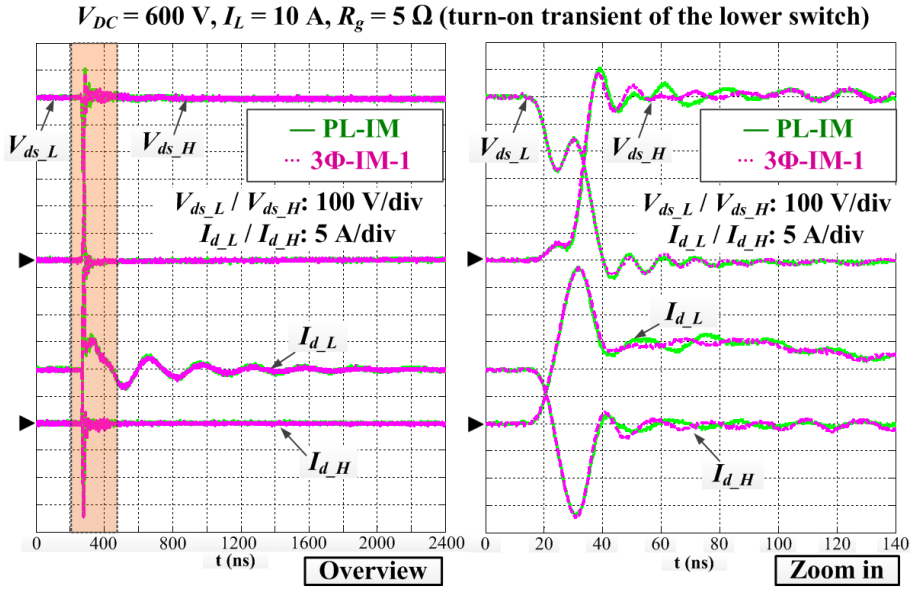
I_L (A)	5	10	15	20
t_{ON} (ns)	16	17	18	20
t_{OFF} (ns)	51	29	24	23
E_{sw} (μJ)	104	141	195	265

Table 4-4. t_{sw} & E_{sw} vs. R_G Under DPT with V_{DC} of 600 V & I_L of 10 A

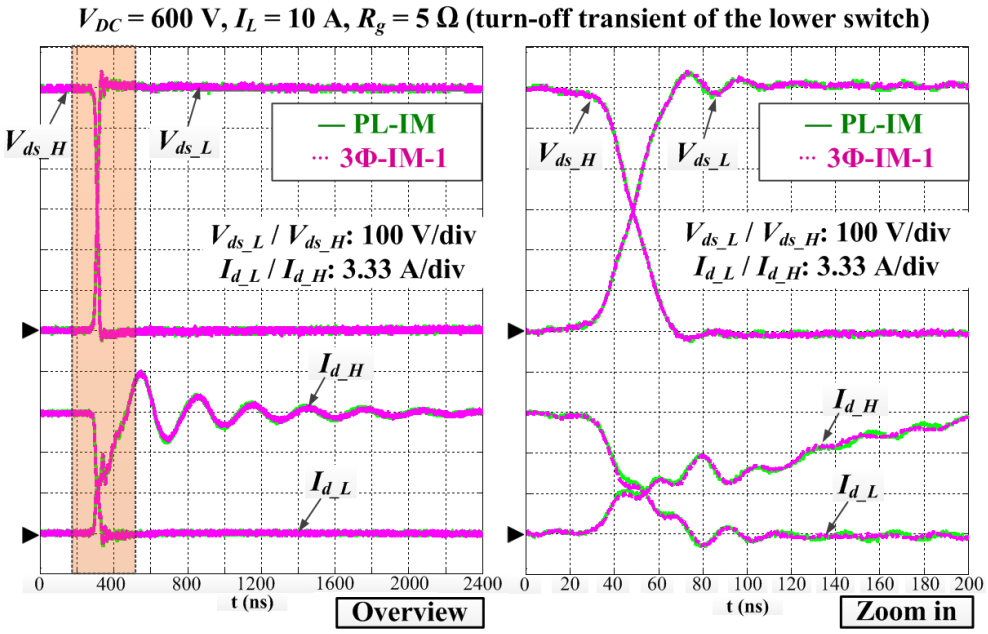
R_G (Ω)	0	5	10
t_{ON} (ns)	17	26	41
t_{OFF} (ns)	29	32	38
E_{sw} (μJ)	132	176	240

Switching waveforms in Fig. 4-40 and Fig. 4-41 illustrate the impact of phase B and C on the switching performance of the lower switch in phase A. Neither the parasitics induced by phase B and C nor the different inductive load connection structures due to the switches' on-off states have significant effect on the switching performance since the switching current and voltage

under different test configurations are almost identical. Similarly, as can be observed in Fig. 4-42, the impact of the heat sink on the switching performance is insignificant.

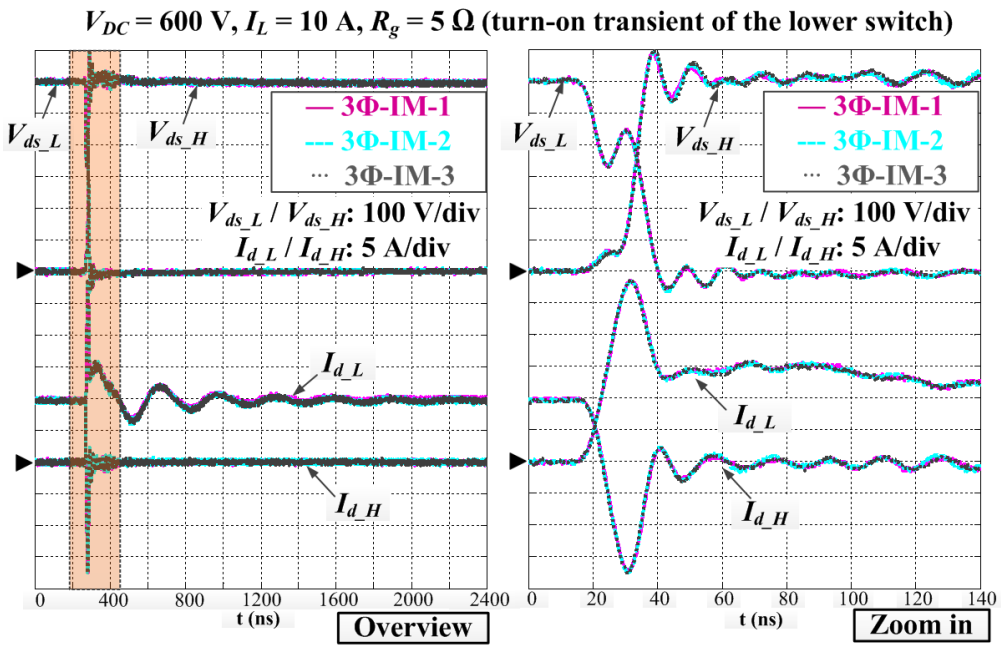


(a) Turn-on transient.

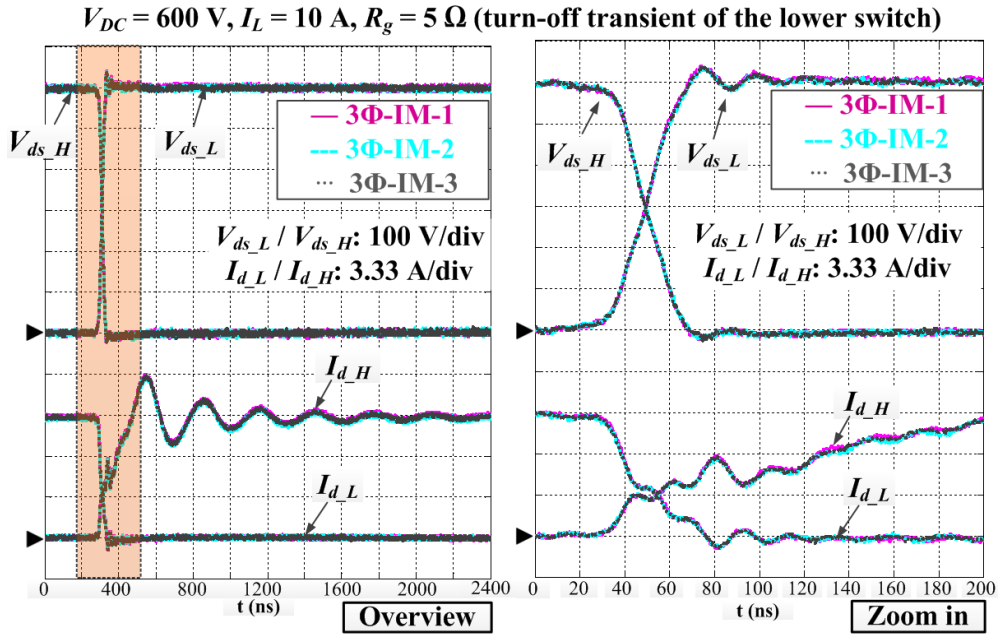


(b) Turn-off transient.

Fig. 4-40. Impact of parasitics induced by phase B and C on switching performance.

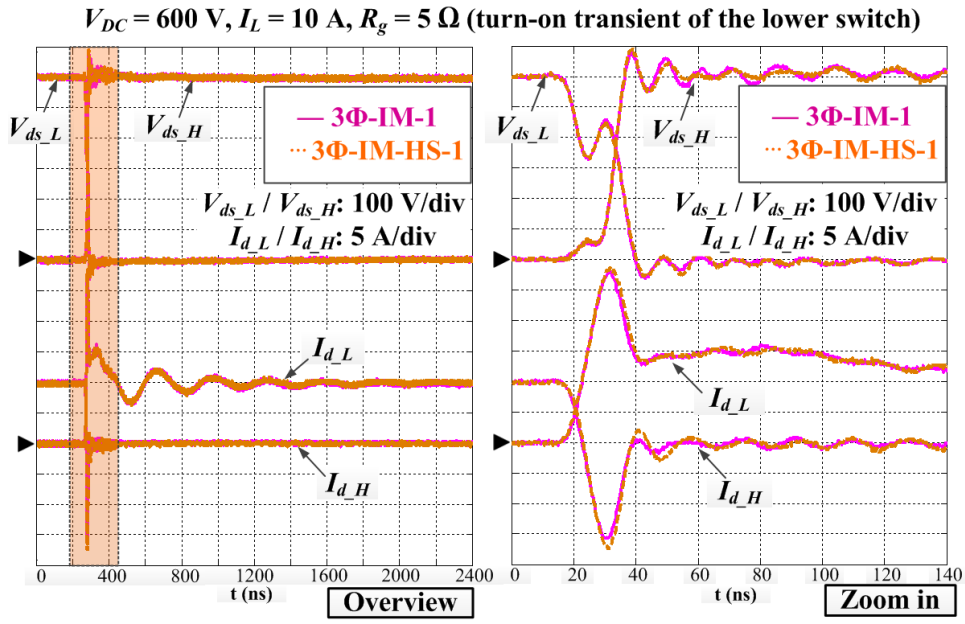


(a) Turn-on transient.

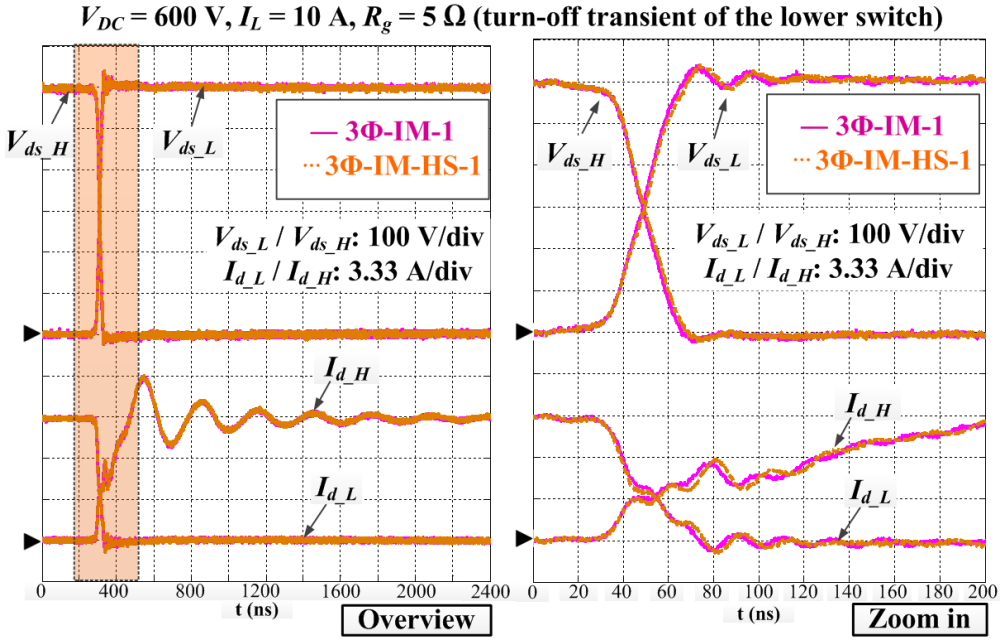


(b) Turn-off transient.

Fig. 4-41. Impact of different connection structures of inductive loads on switching performance.



(a) Turn-on transient.



(b) Turn-off transient.

Fig. 4-42. Impact of capacitive coupling effect on switching performance.

Since the aforementioned test results are based on the pulse test, we cannot necessarily draw a conclusion for a rotating induction motor until additional tests are done. Fig. 4-43 shows the gate signal, line-to-line voltage and phase current of the three-phase inverter when driving the induction motor with no load. According to the modulation scheme, we picked one switching cycle when the circuit configuration during a switching transient is the same as that in 3Φ-IM-HS-1 (see Fig. 4-37(d)), and compared the switching waveforms between the running test and previous pulse test. The switching waveforms in Fig. 4-44 verify that the induction motor rotation has no appreciable influence on the switching performance. The reason is that the flux penetrating into the rotor magnetic circuit at high frequency is very small such that the high frequency impedance of induction motor is almost independent of the rotor speed [125].

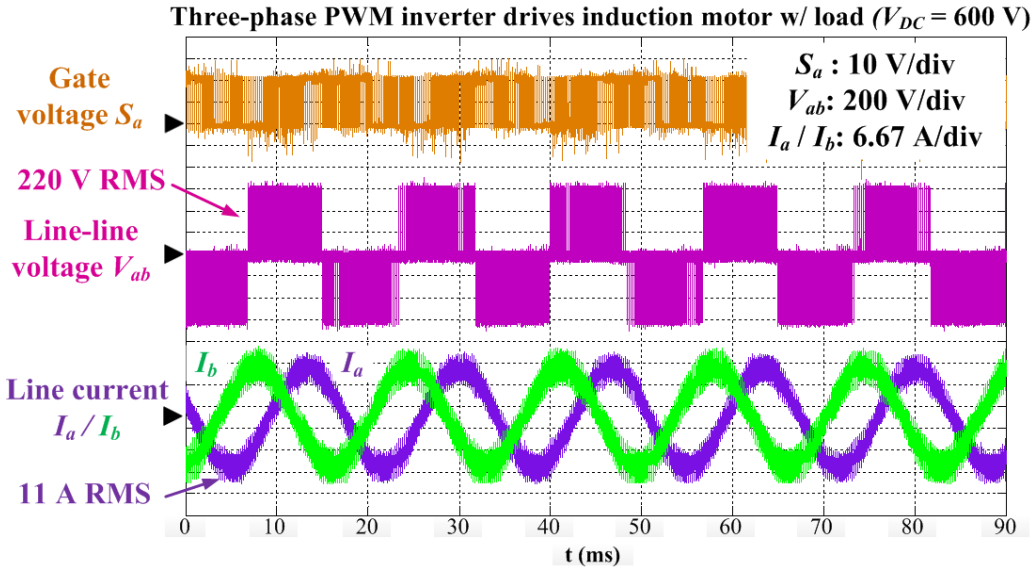
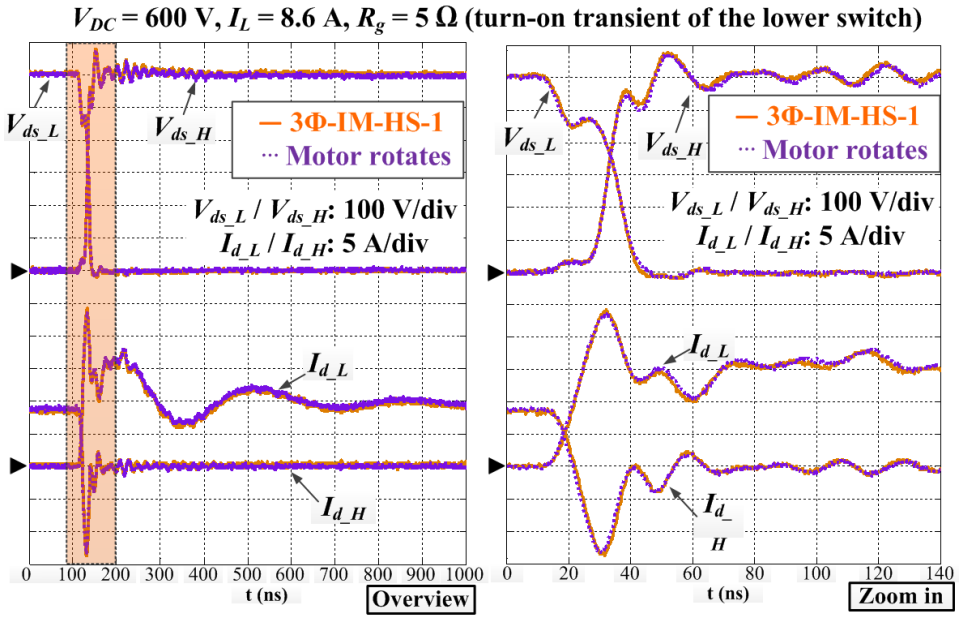
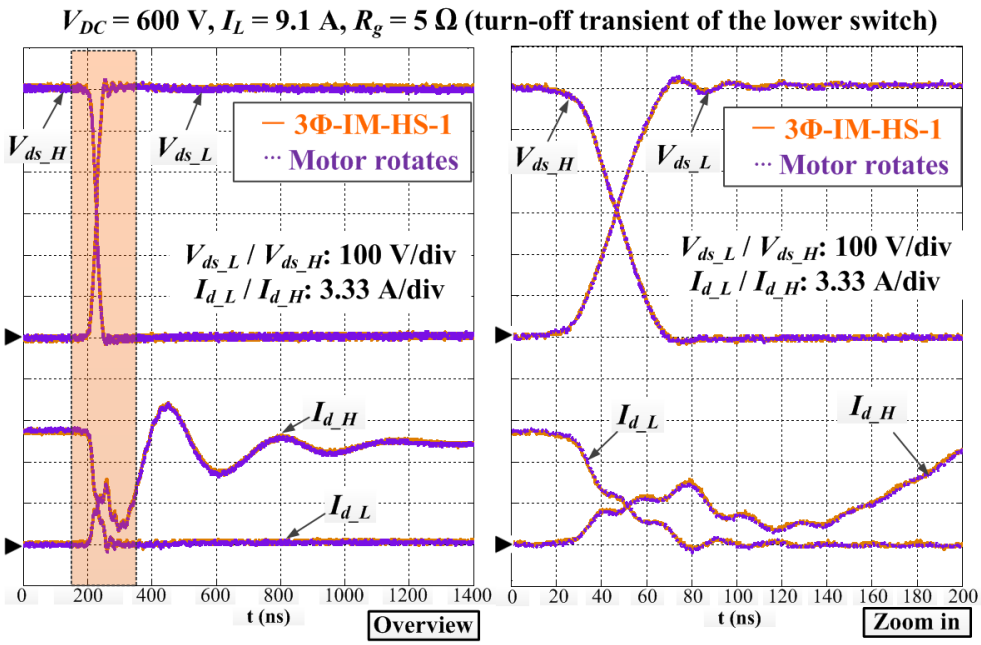


Fig. 4-43. Typical waveforms of three-phase inverter under continuous operating condition.



(a) Turn-on transient.



(b) Turn-off transient.

Fig. 4-44. Impact of mechanical state of induction motor on switching performance.

4.3 Conclusion

Six potential impact factors of switching performance of fast SiC devices are investigated in the phase-leg configuration and three-phase motor drive system.

In the phase-leg configuration, reverse recovery characteristics of the body diode, over-voltage during turn-on and cross-talk are analyzed. First, the test results show that at room temperature, the reverse recovery performance of the SiC MOSFETs' body diode is satisfying, but it becomes significantly poor at high operating temperature. It is recommended to have the antiparallel Schottky diode to guarantee the stable switching performance among wide operating temperature range. Second, the simulation and experimental results show that for fast switching SiC devices, the turn-on over-voltage is worse than the voltage overshoot during turn-off. Also, to avoid the voltage spike during turn-on exceeds the device's breakdown voltage, the switching speed is limited within a *dv/dt*, *di/dt* related safe operating area. Third, the cross-talk induces a spurious gate voltage on its complementary device, which may generate shoot-through current and degrade the device. Thus, to avoid this failure, the switching speed has to be limited as well. According to the inherent properties, SiC devices in a phase-leg configuration are easily affected by cross-talk due to: 1) fast switching-speed; 2) relatively large internal gate resistance; 3) lower threshold voltage; 4) lower maximum allowable negative gate voltage.

In the three-phase voltage source converter, three potentially impact factors of switching performance were investigated, including motor loads, phase-legs, and heat sink. Based on the three-phase PWM inverter with Cree 1200-V/24-A SiC MOSFETs, the test results show that the induction motor, especially with a relatively long power cable, will significantly impact the switching performance, leading to a switching time increase by a factor of 2, switching loss increase up to 30% in comparison with that yielded from DPT, and serious parasitic ringing with

1.5 μs duration, which is more than 50 times of the corresponding switching time. In addition, the interactions among three phase-legs cannot be ignored unless decoupling capacitors are mounted close to each phase-leg to support the dc bus voltage during the switching transient. Also, the coupling capacitance due to the heat sink equivalently increases the junction capacitance of power devices; however, its influence on the switching behavior in motor drives is small considering the relatively large capacitive parasitics of the motor load.

5 Intelligent Gate Driver for Switching Performance Improvement of SiC Devices

This chapter presents intelligent gate drivers designed to best serve SiC devices in voltage source converter. First, two gate assist circuits are introduced to suppress cross-talk for high switching-speed performance enhancement and devices' reliability improvement, since cross-talk is one of the identified critical limit factors. Then the suitable way of implementing each gate assist circuit is compared. Furthermore, another intelligent gate driver is developed to achieve anti-cross-talk functionality as well as further increase the switching speed so that the overall switching performance of SiC devices is continuously improved. The basic ideas, gate driver circuits and operating principles of all three gate driving schemes are discussed with the experimental verification for the effectiveness evaluation.

5.1 Gate Assist Circuits for Cross-Talk Suppression

According to the inherent properties, SiC devices in a phase-leg configuration are easily affected by cross-talk due to the following reasons: 1) fast switching-speed; 2) relatively large internal gate resistance; 3) lower threshold voltage; 4) lower maximum allowable negative gate voltage. Therefore, to fully utilize the potential advantages of fast SiC devices and guarantee the reliability of the power converter, cross-talk should be suppressed. Prior reported work has proposed several methods for cross-talk mitigation [31, 39, 88, 102, 126, 127]. They can be divided into three categories:

1) Add additional capacitance between gate-source terminals to shunt the Miller current [31, 39, 126, 127]. This external gate-source capacitor is to take up additional charge originating from the Miller capacitance, resulting in spurious gate voltage reduction, and cross-talk mitigation for

the affected power device. While the device is under operation, this capacitor will worsen the switching performance with slower switching speed and higher switching losses.

2) Apply a negative biased turn-off gate voltage [31, 39, 126, 127]. This method suppresses the impact of cross-talk during the turn-on transient, but worsens the overstress of power devices' gate terminal due to the higher negative spurious gate voltage induced during the turn-off transient, especially for the SiC device when considering its lower maximum allowable negative gate voltage compared with the silicon-based power device (see Table 4-1).

3) Use active Miller clamping [102, 127]. The operation principle of this method is to activate an additional transistor between the gate-source terminals to short the gate-source region after detecting the gate voltage of the affected power device above the clamp threshold [127]. Thus, it is the measured gate voltage that is used to identify the existence of cross-talk. However, due to the relatively large internal gate resistance of SiC devices, as shown in Table 4-1, the measured spurious gate voltage is less than that across the internal gate-source terminals. Moreover, during the fast switching transient, the measured gate voltage will be greatly interfered due to the coupling of the common source inductance (i.e., L_{cs_L} and L_{cs_H} as shown in Fig. 4-19) between the gate loop and power loop, which is inevitable in practical situations [128, 129]. Thus, active Miller clamping is not suitable for SiC power devices.

Additionally, previous studies of cross-talk suppression merely focus on the *Cdv/dt* induced shoot-through, with little attention on the harm of the negative spurious gate voltage [31, 39, 88, 102, 126, 127]. Moreover, because of the relatively low maximum allowable negative gate voltage of SiC power devices, the negative spurious gate voltage would easily exceed its range, and overstress power devices.

In summary, because of the intrinsic characteristics of SiC power devices, such as low threshold gate voltage, low maximum allowable negative gate voltage, and large internal gate resistance, cross-talk is a serious issue for these devices and a suitable solution for cross-talk suppression is essential. Two gate assist circuits are proposed to actively suppress cross-talk. For the sake of clear description, the first gate assist circuit that uses one auxiliary transistor in series with a capacitor is designated as the gate impedance regulation (GIR) circuit; and the second gate assist circuit consists of two auxiliary transistors with a diode and is called gate voltage control (GVC) circuit, corresponding to their operation principle. The basic idea, structure, detailed operation description, and the design of each gate assist circuit are presented. Based on Cree 1200-V/24-A SiC MOSFETs, a double pulse tester with different gate drive circuits is established to demonstrate the validity and effectiveness of the new gate assist methodology.

5.1.1 Gate Impedance Regulation Based Gate Assist Circuit

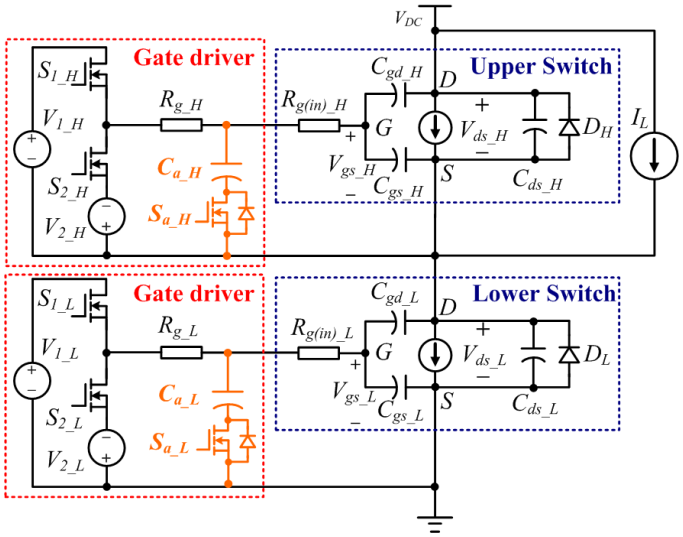
5.1.1.1 Basic Idea for Cross-talk Mitigation

As displayed in Fig. 4-19, the core element of cross-talk is the spurious gate voltage of the upper switch, and its amplitude is determined by the portion of displacement current from the Miller capacitance that is used to charge/discharge the gate-source capacitance of the affected device. Once its gate impedance becomes small during the switching transient, most displacement current will be bypassed by the gate loop, resulting in less current that would induce spurious gate voltage, and thus cross-talk is mitigated.

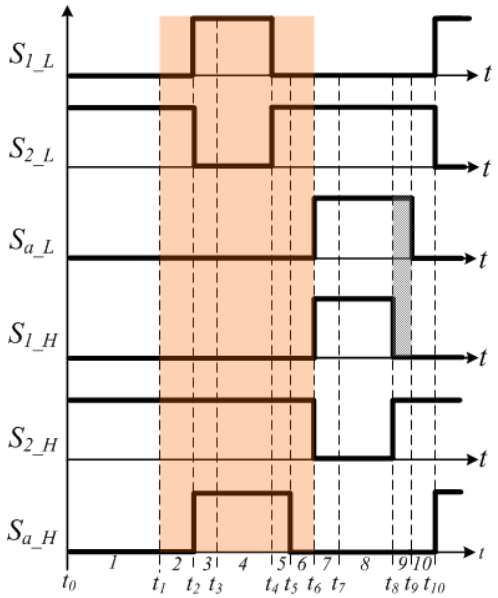
5.1.1.2 Structure and Operation Principle

The proposed gate assist circuit for gate impedance regulation and the logic signals of its corresponding transistors are shown in Fig. 5-1. Compared with the conventional gate drive

circuit (S_{1_H}, S_{2_H} or S_{1_L}, S_{2_L}), only one auxiliary transistor (S_{a_H} or S_{a_L}) in series with one capacitor (C_{a_H} or C_{a_L}) is added between the gate-source terminals of each device. The operation principle of the proposed gate assist circuit is described below, as shown in Fig. 5-2.



(a) GIR based gate assist circuit (S_{a_H}, C_{a_H} or S_{a_L}, C_{a_L}).



(b) Corresponding logic signals of main device (S_{1_H}, S_{2_H} or S_{1_L}, S_{2_L}) and auxiliary transistor (S_{a_H} or S_{a_L}).

Fig. 5-1. Gate assist circuit for gate impedance regulation.

Subinterval 1 [$t_0 - t_1$]: Auxiliary capacitor pre-charge. Before the main power devices start to operate, the auxiliary capacitors C_{a_L} and C_{a_H} need to be pre-charged. Via the body diode of auxiliary transistors S_{a_L}, S_{a_H} and gate resistor R_{g_L}, R_{g_H}, the voltage across C_{a_L} and C_{a_H} is established at the negative gate voltage V_2 at the end of t_1. The duration of this subinterval is determined by the time constant R_gC.

Subinterval 2 [$t_1 - t_2$]: Initialization completion. Auxiliary transistors S_{a_H}, S_{a_L} remain off to wait for the operation of the main power devices. At the end of t_2, the lower switch starts to turn on.

Subinterval 3 [$t_2 - t_3$]: Turn-on transient of the lower switch. S_{1_L} turns on, and both S_{2_L} and auxiliary transistor S_{a_L} turn off. At this moment, the gate-source terminals of the lower switch are connected with the output capacitance of S_{a_L} in series with C_{a_L}. Since the output capacitance of the auxiliary transistor is usually an order of magnitude smaller than the input capacitance of the main power device, this auxiliary circuit has negligible impact on the turn-on switching behavior of the lower switch. Meanwhile, auxiliary transistor S_{a_H} turns on. C_{a_H} directly connects with the gate-source terminals of the upper switch. This large external capacitance offers a low impedance loop to *Cdv/dt* induced current during the turn-on transient of the lower switch, i.e., the gate loop impedance of the upper switch is largely decreased. Therefore, the positive spurious gate voltage will be minimized, and then the cross-talk during the turn-on transient is suppressed. At the end of t_3, the turn-on transient of the lower switch is completed.

Subinterval 4 [$t_3 - t_4$]: Fully turn-on the lower switch. The switching status of all transistors remains the same as that during subinterval 3. The negative power supply V_{2_H} starts to discharge

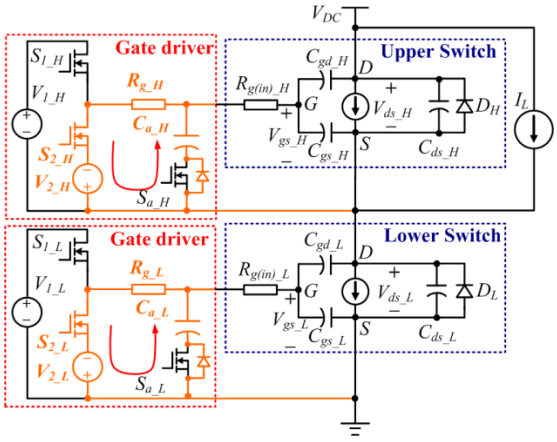
C_{a_H} and C_{gs_H} through R_{g_H} until voltages across C_{a_H} and C_{gs_H} return to V_{2_H}. At the end of t_4, the lower switch starts to turn off.

Subinterval 5 [$t_4 - t_5$]: Turn-off transient of the lower switch. S_{1_L} turns off, S_{2_L} turns on, and auxiliary transistor S_{a_L} remains off. Just as in subinterval 3, the auxiliary circuit does not affect the turn-off switching performance of the lower switch. Meanwhile, auxiliary transistor S_{a_H} remains on. The gate loop impedance of the lower switch is decreased due to the low impedance C_{a_H}. Also, the negative spurious gate voltage is minimized. At the end of t_5, the turn-off transient of the lower switch is completed.

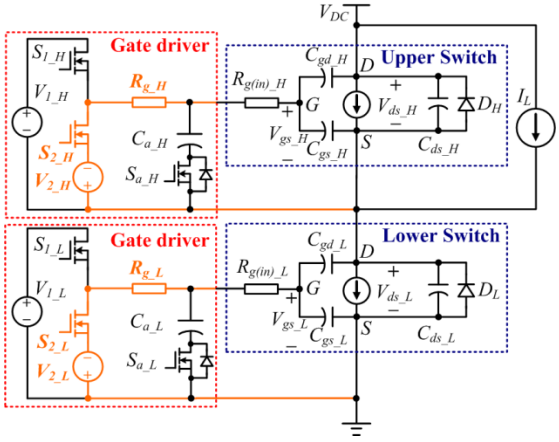
Subinterval 6 [$t_5 - t_6$]: Fully turn-off the lower switch. Auxiliary transistor S_{a_H} turns off. C_{a_H} is disconnected from the gate-source terminals of the upper switch for the upcoming switching transient of the upper switch. The negative power supply V_{2_H} starts to charge C_{gs_H} through R_{g_H} until V_{gs_H} returns to V_{2_H}. At the end of t_6, the upper switch starts to turn on.

Based on the circuit symmetry, the operation principle during a switching transient of the upper switch, i.e., subintervals 7-10, as shown in Fig. 5-1(b), are similar to that during subintervals 3-6. Specifically, subintervals 7-10 represent turn-on transient of the upper switch, fully turn-on the upper switch, turn-off transient of the upper switch, and fully turn-off the upper switch, respectively.

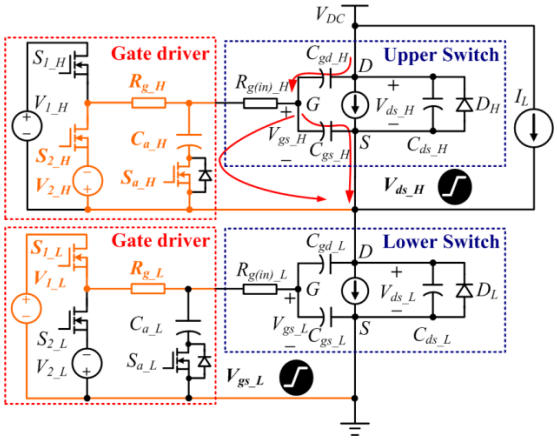
According to the operation principle, the logic signals of auxiliary transistors are almost the same as that of their complementary main power devices, except that the auxiliary transistors will remain on until the end of the turn-off transient of the complementary main power devices, as shown in Fig. 5-1 (shaded area). Consequently, logic signals of auxiliary transistors can be easily synthesized based on the logic signals of the main power devices, and this feedforward control scheme is suitable for the SiC power devices with fast switching capability.



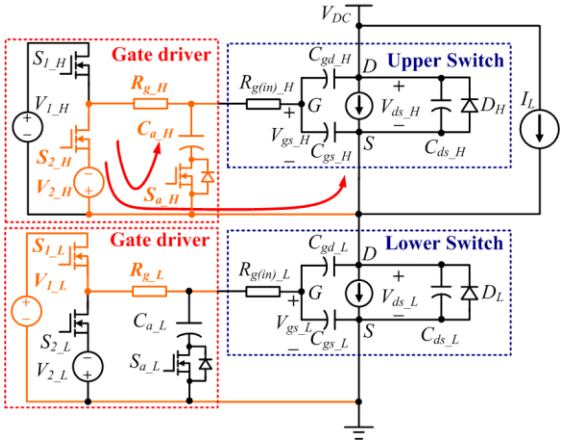
(a) Subinterval 1 [t_0 - t_1].



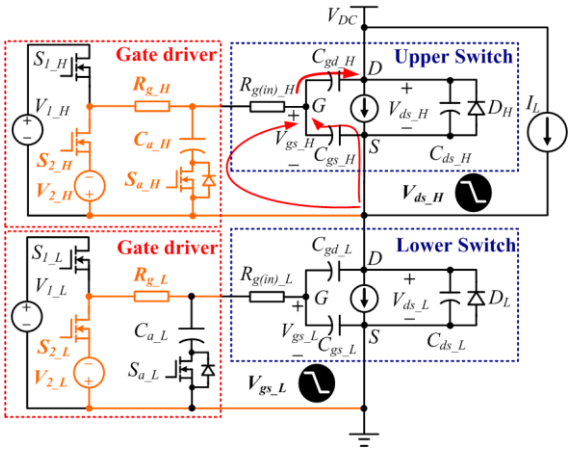
(b) Subinterval 2 [t_1 - t_2].



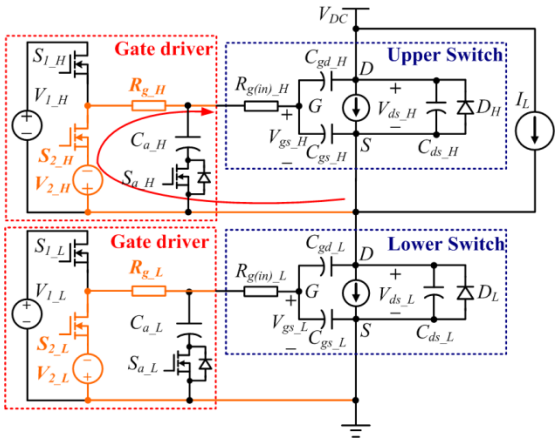
(c) Subinterval 3 [t_2 - t_3].



(d) Subinterval 4 [t_3 - t_4].



(e) Subinterval 5 [$t_4 - t_5$].



(f) Subinterval 6 [$t_5 - t_6$].

Fig. 5-2. Operation principle of the gate impedance regulation (GIR) circuit.

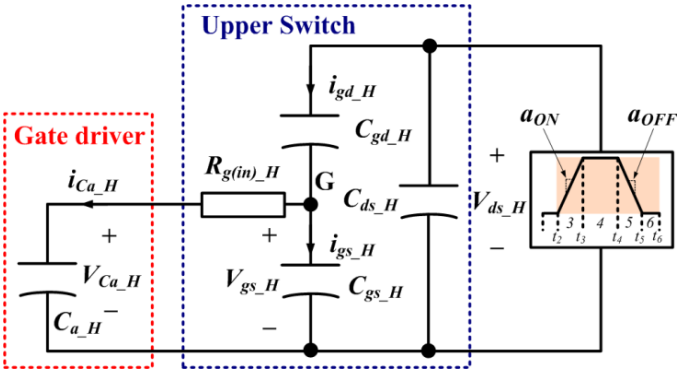


Fig. 5-3. Simplified equivalent circuit of the lower switch during the switching transient of the upper switch.

5.1.1.3 Primary Parameters Design

To avoid cross-talk during both turn-on and turn-off transient, the spurious gate voltage must be limited within the range from the maximum allowable negative gate voltage $V_{gs\_max(-)}$, to the threshold voltage V_{th}. Thus, a key issue for cross-talk suppression is to obtain and control the positive and negative peak value of spurious gate voltage with the gate assist circuit during turn-on and turn-off switching transients.

Assume the upper switch is the device under interference, Fig. 5-3 shows the simplified equivalent circuit of the upper switch during the switching transient of the lower switch. Applying KCL at nodal G and KVL into the gate loop, yielding

$$C_{gd\_H}\frac{d(V_{ds\_H}-V_{gs\_H})}{dt} = C_{gs\_H}\frac{dV_{gs\_H}}{dt} + C_{a\_H}\frac{dV_{Ca\_H}}{dt} \tag{5-1}$$

$$V_{gs\_H} = V_{Ca\_H} + R_{g(in)\_H} \times C_{a\_H}\frac{dV_{Ca\_H}}{dt} \tag{5-2}$$

where C_{gd_H} and C_{gs_H} refer to the Miller capacitance and gate-source capacitance. $R_{g(in)\_H}$ is the internal gate resistance of the upper switch.

Assuming a constant slew rate of drain-source voltage of the upper switch V_{ds_H} during switching transient, referred to as a, the spurious gate voltage variation ΔV induced by dV_{ds_H}/dt can be express as

$$\Delta V = \frac{C_{gd\_H} V_{DC}}{A} + \frac{C_{a\_H}^2 R_{g(in)\_H} C_{gd\_H} a}{A^2} \left(1 - e^{\frac{-AV_{DC}}{a \times C_{a\_H} R_{g(in)\_H} C_{iss\_H}}}\right) \tag{5-3}$$

where C_{iss_H} refers to the input capacitance of the upper switch, the sum of C_{gd_H} and C_{gs_H}. A is the sum of C_{a_H} and C_{iss_H}. V_{DC} is the DC bus voltage.

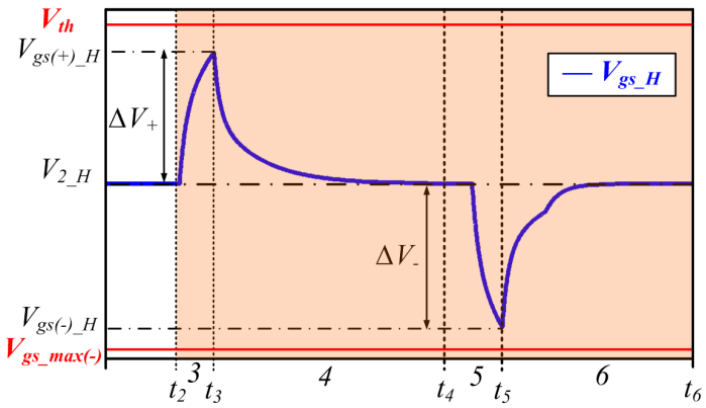


Fig. 5-4. Spurious gate voltage (blue curve) during the switching transient.

During the turn-on transient of the lower switch (i.e., subinterval 3 in Fig. 5-2(c)), this spurious gate voltage increases, as shown in Fig. 5-4. Its positive peak value $V_{gs(+)\_H}$ is expressed as

$$V_{gs(+)\_H} = V_{2\_H} + \Delta V_+ = V_{2\_H} + \frac{C_{gd\_H} V_{DC}}{A} + \frac{C_{a\_H}^2 R_{g(in)\_H} C_{gd\_H} a_{ON}}{A^2} \left(1 - e^{\frac{-AV_{DC}}{a_{ON} C_{a\_H} R_{g(in)\_H} C_{iss\_H}}}\right) \tag{5-4}$$

where V_{2_H} is the turn-off gate voltage of the upper switch, ΔV_+ represents the positive spurious gate voltage variation during the turn-on transient of the lower switch, and a_{ON} is the slew rate of V_{ds_H}, as shown in Fig. 5-3.

During the turn-off transient of the lower switch (i.e., subinterval 5 in Fig. 5-2(e)), the spurious gate voltage decreases, as can be observed in Fig. 5-4. Its negative peak value $V_{gs(-)\_H}$ is given by

$$V_{gs(-)\_H} = V_{2\_H} - \Delta V_- = V_{2\_H} - \frac{C_{gd\_H} V_{DC}}{A} - \frac{C_{a\_H}^2 R_{g(in)\_H} C_{gd\_H} a_{OFF}}{A^2} \left(1 - e^{\frac{-AV_{DC}}{a_{OFF} C_{a\_H} R_{g(in)\_H} C_{iss\_H}}}\right) \tag{5-5}$$

where ΔV_- is the negative spurious gate voltage variation, and a_{OFF} is the slew rate of V_{ds_H}, as shown in Fig. 5-3.

According to the aforementioned analysis, to avoid cross-talk, $V_{gs(+)\_H}$ should be smaller than V_{th}. Also, $V_{gs(-)\_H}$ should be greater than $V_{gs\_max(-)}$. Thus, the following requirements must be satisfied

$$\Delta V_+ + \Delta V_- \leq V_{th} - V_{gs\_\max(-)} \tag{5-6}$$

$$V_2 \leq V_{th} - \Delta V_+ \tag{5-7}$$

$$V_2 \geq V_{gs\_max(-)} + \Delta V_- \tag{5-8}$$

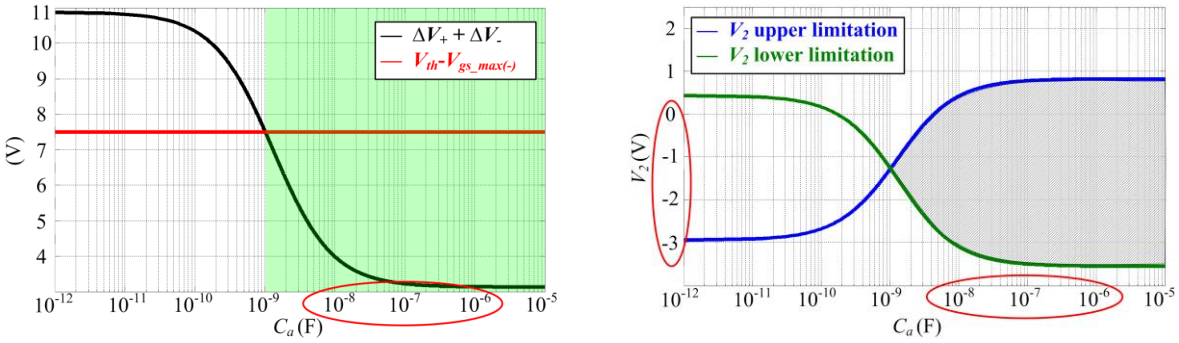
Substituting (5-4) and (5-5) into (5-6), the range of the auxiliary capacitance C_a is determined. The negative biased turn-off gate voltage V_2 can be selected based on (5-7) and (5-8). Taking the Cree CMF20120D 1200-V/24-A SiC MOSFET as an example, based on the parameters and specifications listed in Table 5-1, the selection ranges of C_a and V_2 are shown in Fig. 5-5. The proper auxiliary capacitance is around 10 nF to 1 μF, and the proper negative

biased turn-off voltage is around −3 V to 0 V. In the test, a 100 nF ceramic capacitor with 0 V turn-off voltage are selected.

Table 5-1. Parameters of CMF20120D and Specifications

C_{gd}	13 pF	C_{gs}	1900 pF
V_{th}	2.5 V	$V_{gs\_max(-)}$	−5 V
V_{DC}	800 V	a_{ON}*	27 V/ns
$R_{g(in)}$	5 Ω	a_{OFF}*	23 V/ns

* determined according to test results.



(a) Selection ranges of C_a. (b) Selection ranges of V_2.

Fig. 5-5. Primary parameters design.

5.1.2 Gate Voltage Control Based Gate Assist Circuit

5.1.2.1 Basic Idea for Cross-talk Elimination

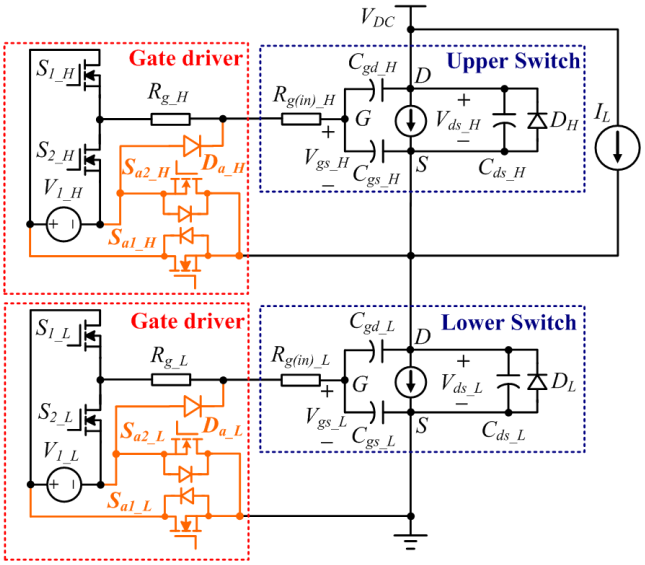
In addition to regulating gate loop impedance for cross-talk mitigation, a more direct solution to avoid cross-talk is to actively control the gate voltage of the affected device during

the switching transient of the opposite switch in a phase-leg. Specifically, we can negatively pre-charge the gate-source capacitance of the upper switch before the turn-on transient of the lower switch so that *Cdv/dt* induced positive spurious gate charge will be cancelled by this pre-stored negative gate charge. Once the pre-stored gate-source charge of the upper switch is sufficient, cross-talk during the turn-on transient of the lower switch can be eliminated. Also, during the turn-off transient of the lower switch, considering the potential hazard of shoot-through, instead of pre-charging gate-source capacitance of the upper switch with positive charge, the gate loop impedance is reduced to minimize the negative spurious gate voltage.

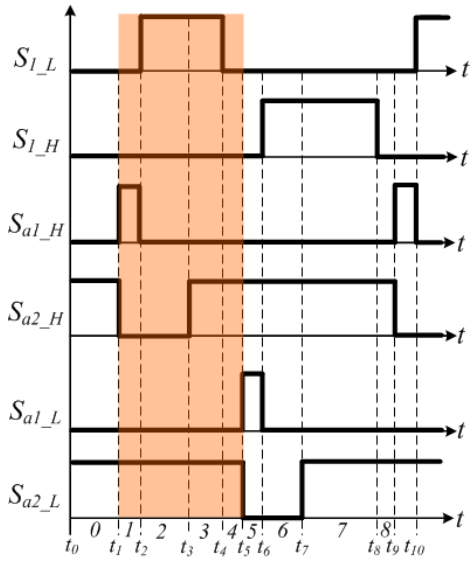
5.1.2.2 Structure and Operation Principle

Based on the aforementioned concept, a gate assist circuit for gate voltage control and its corresponding logic signals for control of the transistors are proposed, as shown in Fig. 5-6. Compared with the conventional gate drive circuit (S_{1_H}, S_{2_H} or S_{1_L}, S_{2_L}), two auxiliary transistors (S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L}) together with one diode (D_{a_H} or D_{a_L}) are added between the gate-source terminals of each device, while the commonly used negative isolated power supply (V_{2_H} or V_{2_L}) is not needed (see Fig. 5-1). Fig. 5-7 displays the operating procedure of the proposed gate assist circuit, described as follows.

Subinterval 1 [$t_1 - t_2$]: Gate-source capacitance pre-charge of the upper switch. Before the lower switch starts to turn on, S_{1_H} and auxiliary transistor S_{a2_H} turn off; S_{2_H} and auxiliary transistor S_{a1_H} turn on. Via the loop formed by S_{2_H}, S_{a1_H} and R_{g_H}, the positive turn-on gate voltage V_{1_H} is used to pre-charge the gate-source capacitance of the upper switch C_{gs_H} to the required negative voltage for the cross-talk elimination at the end of t_2. The duration of this subinterval is determined by the required pre-charge negative voltage, which will be discussed in detail in the next section. At the end of t_2, the lower switch starts to turn on.



(a) GVC based gate assist circuit (S_{a1_H}, S_{a2_H}, D_{a_H} or S_{a1_L}, S_{a2_L}, D_{a_L}).



(b) Corresponding logic signals of main device (S_{1_H} or S_{1_L}) and auxiliary transistors (S_{a1_H}, S_{a2_H} or S_{a1_L}, S_{a2_L}).

Fig. 5-6. Gate assist circuit for gate voltage control.

Subinterval 2 [$t_2 - t_3$]: Turn-on transient of the lower switch. S_{1_L} turns on, S_{2_L} turns off, auxiliary transistor S_{a2_L} remains on, and S_{a1_L} remains off. Since the junction capacitance of the

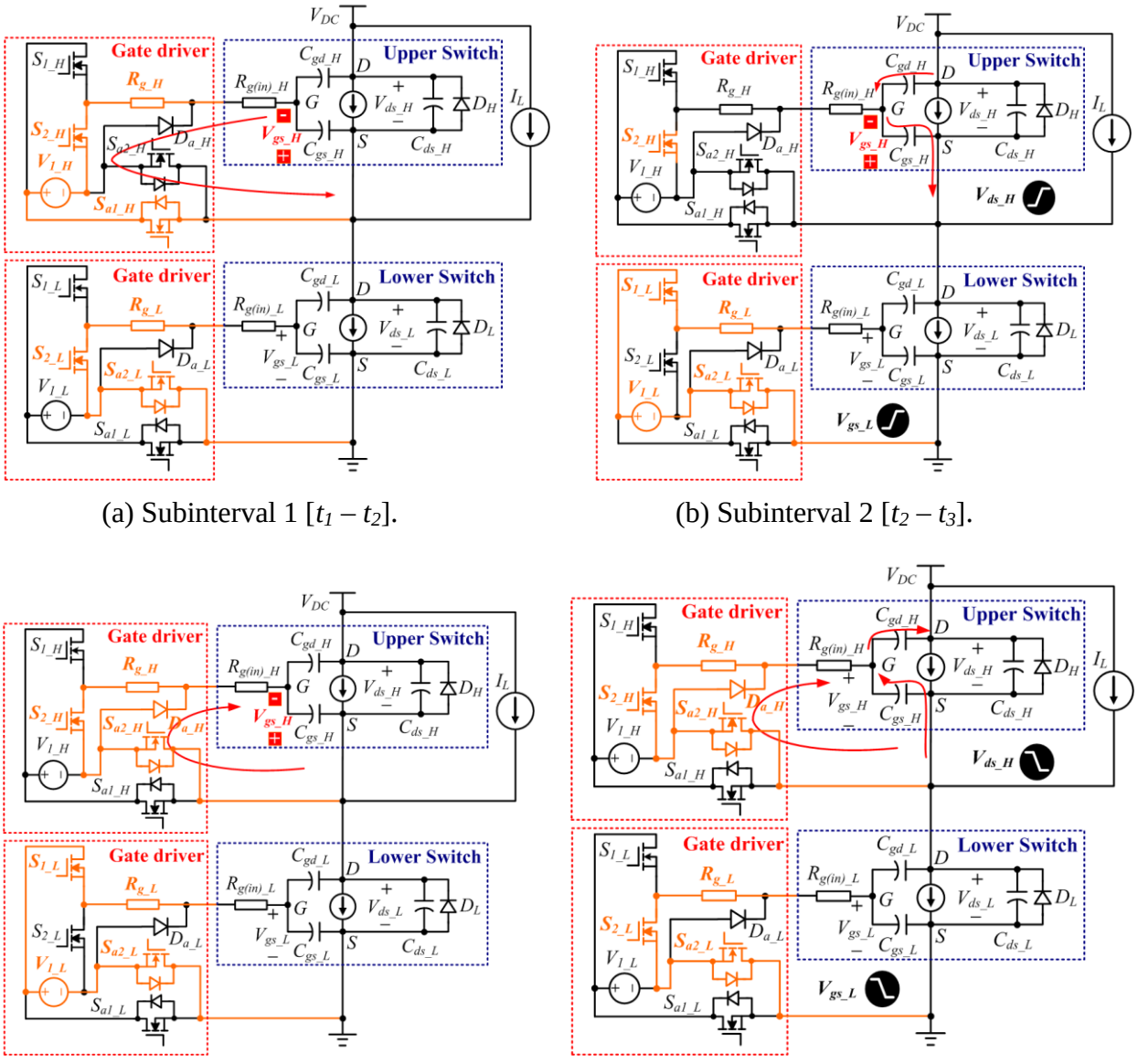
auxiliary diode D_{a_L} is usually an order of magnitude smaller than the input capacitance of the main power device, this auxiliary circuit has negligible impact on the turn-on switching behavior of the lower switch. Meanwhile, auxiliary transistor S_{a1_H} turns off and S_{a2_H} remains off. Due to the body diode of S_{a2_H} and auxiliary diode D_{a_H}, instead of bypassing through the external gate loop, the negative charge pre-stored in C_{gs_H} is fully utilized to cancel the positive charge transferred from the Miller capacitance of the upper switch C_{gd_H}. Once this pre-stored negative gate-source charge (i.e., negative gate voltage) is sufficient, cross-talk during the turn-on transient of the lower switch can be eliminated. At the end of t_3, the turn-on transient of the lower switch is completed.

Subinterval 3 [$t_3 - t_4$]: Fully turn-on the lower switch. Auxiliary transistor S_{a2_H} turns on. The residual negative voltage across C_{gs_H} at subinterval 2 returns to 0 for the preparation of cross-talk mitigation during the upcoming turn-off transient of the lower switch. At the end of t_4, the lower switch starts to turn off.

Subinterval 4 [$t_4 - t_5$]: Turn-off transient of the lower switch. S_{1_L} turns off and S_{2_L} turns on. Switching status of all auxiliary transistors are the same as that during subinterval 3. This auxiliary circuit does not affect the turn-off switching performance of the lower switch, just as in subinterval 2. Meanwhile, auxiliary transistor S_{a2_H} and diode D_{a_H} offer a low impedance loop to *Cdv/dt* induced current during the turn-off transient of the lower switch, that is, the gate loop impedance of the upper switch is largely decreased. Therefore, the negative spurious gate voltage is minimized. At the end of t_5, the turn-off transient of the lower switch is finished.

Based on the circuit symmetry, the operation principle during switching transient of the upper switch, i.e., subintervals 5-8, as shown in Fig. 5-6(b), are similar to that during subintervals 1-4. Specifically, subintervals 5-8 correspond to gate-source capacitance pre-charge

of the lower switch, turn-on transient of the upper switch, fully turn-on the upper switch, and turn-off transient of the upper switch, respectively.



(a) Subinterval 1 [$t_1 - t_2$]. (b) Subinterval 2 [$t_2 - t_3$].

(c) Subinterval 3 [$t_3 - t_4$]. (d) Subinterval 4 [$t_4 - t_5$].

Fig. 5-7. Operation principle of the gate voltage control (GVC) circuit.

According to the operation principle, the logic signals for the control of auxiliary transistors can be synthesized merely based on the logic signals of the main power devices using several logic gates. Thus, through feedforward control, the gate voltage control (GVC) assist circuit is well suited for SiC power devices with fast switching capability.

5.1.2.3 Primary Parameters Design

For cross-talk suppression, the pre-stored gate-source charge must be capable of cancelling the charge stored in the Miller capacitance. I.e., the gate voltage variation due to the gate-drain charge during the switching transient has to be lower than that pre-charged across the gate-source capacitance, as in (5-9)

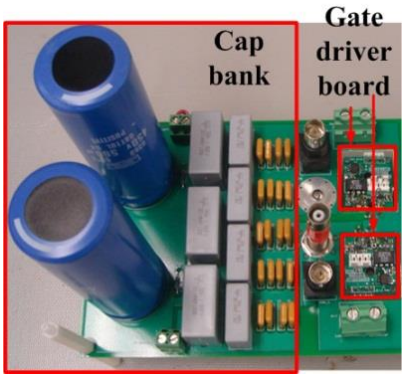
$$Q_{gs(pre)} \geq Q_{Miller} \text{ or } V_{gs(pre)} \geq \Delta V_{gs} = \frac{C_{gd} V_{DC}}{C_{gs}} \tag{5-9}$$

where $Q_{gs(pre)}$ and Q_{Miller} refer to the pre-stored gate-source charge and gate-drain charge, respectively. $V_{gs(pre)}$ and ΔV_{gs} are the pre-charged gate voltage and the gate voltage variation during switching transient. C_{gd} and C_{gs} indicate the Miller capacitance and gate-source capacitance of the power device. Based on $V_{gs(pre)}$, the pre-charge duration at subinterval 1 and 5 should satisfy

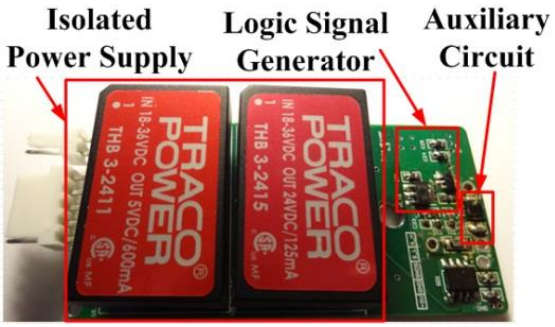
$$t_{pre} \geq -(R_g + R_{g(in)}) \times C_{iss} \times \ln(1 - \frac{\Delta V_{gs}}{V_1}) \tag{5-10}$$

where t_{pre} represents the pre-charge duration. R_g, $R_{g(in)}$, and C_{iss} refer to the external gate resistance, internal gate resistance, and input capacitance of the power devices, respectively. V_1 is the positive output voltage of the gate driver. Note that t_{pre} is only related to the operating voltage, no matter how large the variation of load current and gate resistance. Once t_{pre} is selected under the maximum operating voltage, this gate assist circuit can eliminate *Cdv/dt*

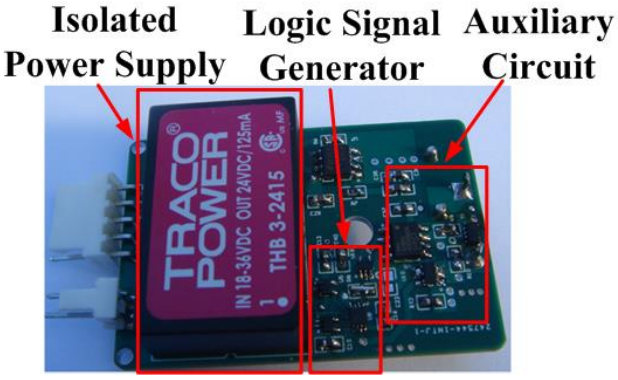
induced shoot-through under different operating conditions. Practically, t_{pre} is tens of nanoseconds.



(a) Double pulse test motherboard with two gate driver daughter boards.



(b) Proposed gate driver board with gate impedance regulation (GIR) circuit.



(c) Proposed gate driver board with gate voltage control (GVC) circuit.

Fig. 5-8. Hardware setup.

5.1.3 Experimental Verification

A double pulse test with Cree CMF20120D 1200-V/24-A SiC MOSFETs in a phase-leg configuration is established for experimental verification, as shown in Fig. 5-8. Sharing one motherboard, two active gate drive daughter boards integrating different gate assist circuits are designed to guarantee that the switching performance improvement of the SiC devices merely comes from the gate driver rather than different layouts and their induced parasitics in the power loop. The auxiliary components of each gate assist circuit are listed in Table 5-2. To evaluate the effectiveness of the gate assist circuits for cross-talk suppression, comparison experiments under four different groups are conducted according to different gate assist circuits and varying negative biased turn-off gate voltage, as listed in Table 5-3. For simplicity, GIR refers to gate impedance regulation circuit, while GVC represents gate voltage control circuit. For each group, 12 cases with gate resistances of 10/4.7 Ω, operating voltages of 800/600 V, and operating currents of 5/10/20 A are tested.

Table 5-2. Auxiliary Components of Gate Assist Circuits

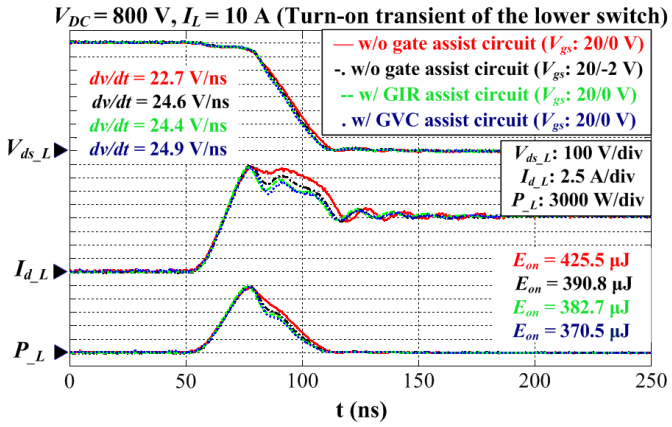
Gate impedance regulation (GIR) circuit (1^{st} gate assist circuit)	Auxiliary transistor	Si7308DN N-Channel Si MOSFET
	Auxiliary capacitor	100 nF/ 35 V ceramic capacitor
Gate voltage control (GVC) circuit (2^{nd} gate assist circuit)	Auxiliary transistors	Si5902BDC Dual N-Channel Si MOSFETs
	Auxiliary diode	MSS1P3 Schottky Barrier diode

Table 5-3. Four Comparison Groups

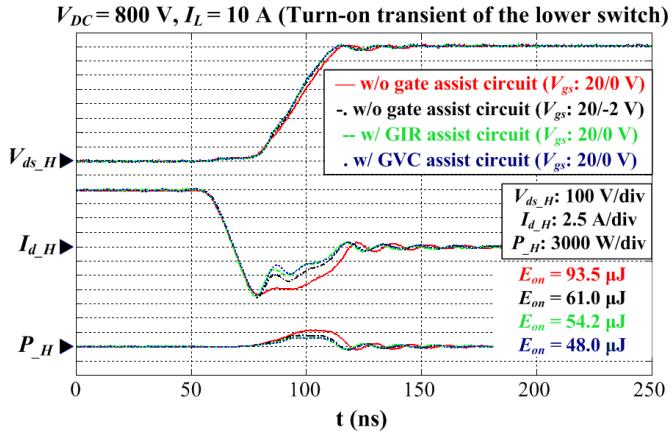
1st Group	w/o gate assist circuit with V_{gs} of 20/0 V
2nd Group	w/o gate assist circuit with V_{gs} of 20/-2 V
3rd Group	w/ GIR assist circuit with V_{gs} of 20/0 V
4th Group	w/ GVR assist circuit with V_{gs} of 20/0 V

Fig. 5-9 displays the comparison waveforms under four different groups with the operating condition of 800-V/10-A with 10-Ω gate resistance. During turn-on transient of the lower switch, as shown in Fig. 5-9(a), the turn-on energy losses of the lower switch with either gate assist circuit are less than that without gate assist circuit, even if −2 V turn off gate voltage is applied. Meanwhile, without further reducing the switching speed, both gate assist circuits improve the slew rate of the drain-source voltage. Also, as can be observed Fig. 5-9(b), the switching losses of the upper switch generated by *Cdv/dt* induced shoot-through current are decreased due to the gate assist circuits. Moreover, during the turn-off transient of the upper switch, both gate assist circuits enable the spurious negative gate voltages of the lower switch to be largely suppressed, as shown in Fig. 5-9(c).

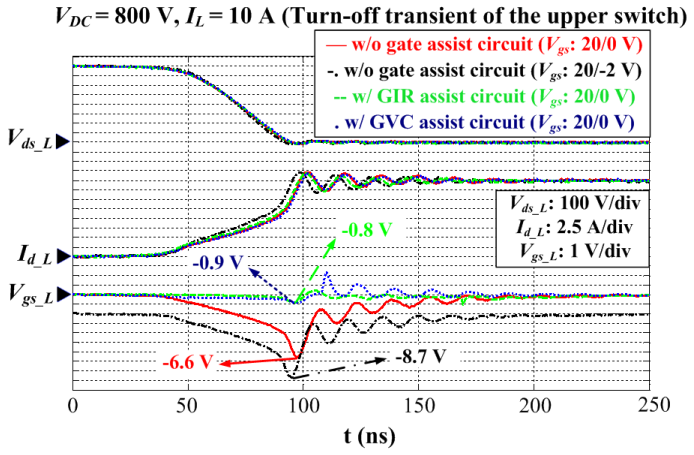
For example, under V_{gs} of 20/0 V, with GIR based assist circuit, the turn-on energy loss of the lower switch and shoot-through energy loss of the upper switch are reduced by 42.8 μJ and 39.3 μJ, respectively, enabling total turn-on energy loss savings of approximately 17.1%. In addition, *dv/dt* increases from 22.7 V/ns to 24.4 V/ns. Also, the negative peak value of the spurious gate voltage is minimized from −6.6 V (which exceeds −5 V, the maximum rating of negative gate voltage of the CMF20120D) to −0.8 V.



(a) Lower switch waveforms during the turn-on transient of the lower switch.



(b) Upper switch waveforms during the turn-on transient of the lower switch.



(c) Lower switch waveforms during the turn-off transient of the upper switch.

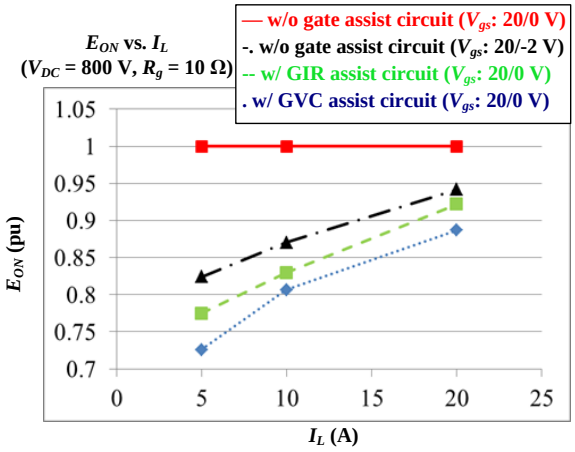
Fig. 5-9. Switching waveforms comparison: conventional gate driver versus proposed gate driver with anti-cross-talk assist circuit.

Furthermore, the GVC based assist circuit is more effective for the switching performance enhancement: total turn-on energy loss reduction up to 19.4%, *dv/dt* improvement from 22.7 V/ns to 24.9 V/ns, and spurious negative gate voltage suppression below −1.0 V. The reason why GVC based assist circuit has better performance than the GIR based assist circuit for cross-talk elimination during turn-on transient is due to the large internal gate resistance of SiC devices, which limits the total gate impedance minimization; obviously the GIR based assist circuit can only eliminate the impact of the external gate impedance.

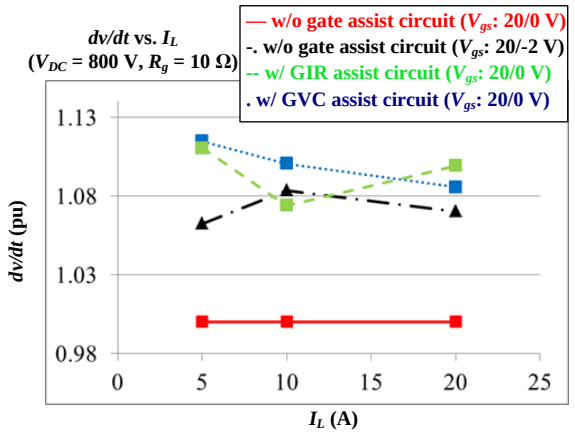
Fig. 5-10 presents the comparison test results dependence on the load current under the dc bus voltage of 800 V with 10-Ω gate resistance. In order to clearly demonstrate the effectiveness of the gate assist circuits, the turn-on energy loss and *dv/dt* under the 2nd, 3rd, and 4th group are normalized based on that under the 1st group, which are listed in Table 5-4. It shows that under different load currents, the turn-on energy losses with gate assist circuits of 0 V turn-off gate voltage are always less than that with conventional gate driver, and *dv/dt* is higher, even for the case of when −2 V turn-off gate voltage is applied in the conventional gate driver. Note also that both gate assist circuits have the capability of limiting the peak value of negative spurious gate voltages within its required range. Furthermore, better switching behavior during the turn-on transient by using the GVC assist circuit verifies again that the large internal gate resistance of SiC devices limits the performance of GIR assist circuit for cross-talk suppression.

Table 5-4. E_{on} and *dv/dt* vs. I_L Under 1st Group with V_{DC} of 800 V and R_g of 10 Ω

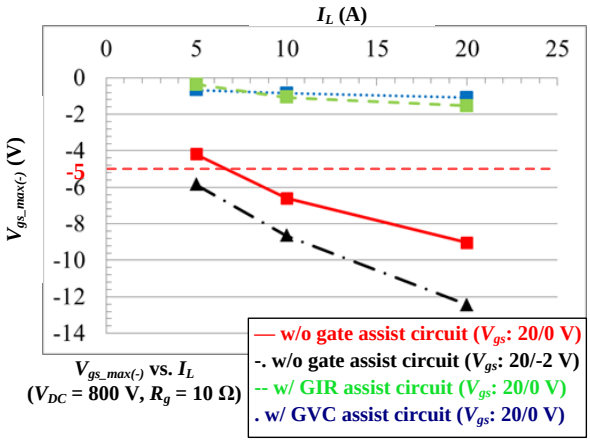
I_L (A)	5	10	20
E_{ON} (μJ)	381.3	519.0	852.6
dv/dt (V/ns)	23.5	22.7	21.1



(a) Normalized turn-on energy losses during the turn-on transient of the lower switch.



(b) Normalized *dv/dt* during the turn-on transient of the lower switch.



(c) Negative peak value of spurious gate voltage during the turn-off transient of the upper switch.

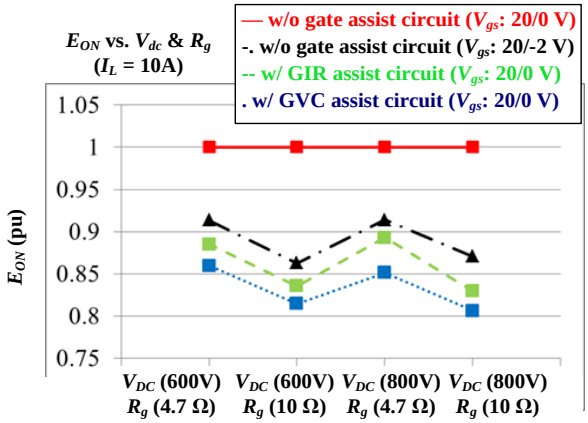
Fig. 5-10. Comparison test results dependence on load current.

Fig. 5-11 illustrates the comparison test results dependence on dc bus voltage and gate resistance under the load current of 10 A. According to the conditions under the 1st group listed in Table 5-5, turn-on energy loss and *dv/dt* under the 2nd , 3rd, and 4th group are managed the same as that in Fig. 5-10. The experimental results show that under different dc bus voltage with varying gate resistances, the gate assist circuits have the capability to improve the switching behavior of power devices in a phase-leg configuration in comparison to the conventional gate circuit, even with −2 V turn-off gate voltage. Moreover, compared with GIR assist circuit, the GVR assist circuit is still more effective for cross-talk suppression.

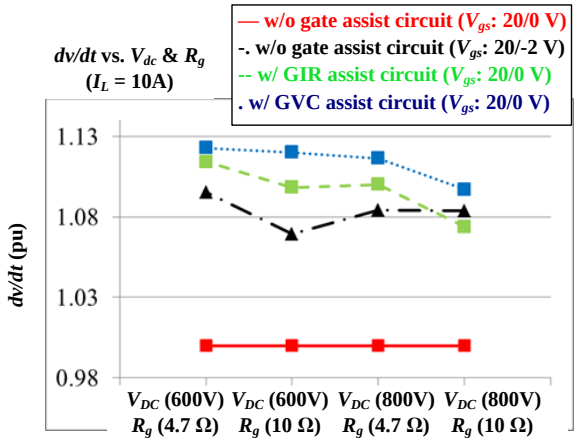
In summary, both gate assist circuits have the capability for cross-talk suppression. Considering the characteristics of auxiliary components and generation of logic signals for control, each gate assist circuit has its own application. Thanks to its fewer auxiliary components and easier logic signal synthesis, the gate impedance regulation (GIR) based assist circuit is convenient to integrate with a conventional gate driver on a printed circuit board. But the implementation issue of embedding a large capacitor on chip impedes its chip-level integration when considering gate driver integrated circuit design. On the contrary, the all-transistors based gate voltage control (GVC) circuit is a suitable gate assist methodology for gate driver chip-level integration, which largely simplifies the implementation of relatively complicated logic signal synthesis.

Table 5-5. E_{on} and *dv/dt* vs. V_{DC} and R_g Under 1st Group with I_L of 10 A

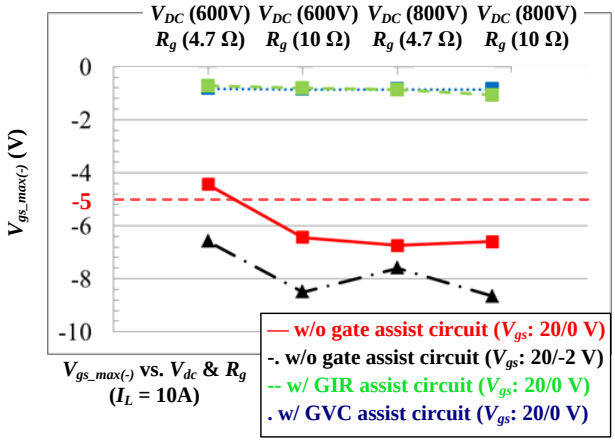
V_{dc}/R_g (V/ Ω)	600/4.7	600/10	800/4.7	800/10
E_{ON} (μJ)	263.8	332.0	416.3	519.0
dv/dt (V/ns)	29.7	19.7	33.1	22.7



(a) Normalized turn-on energy losses during the turn-on transient of the lower switch.



(b) Normalized *dv/dt* during the turn-on transient of the lower switch.



(c) Negative peak value of spurious gate voltage during the turn-off transient of the upper switch.

Fig. 5-11. Comparison test results dependence on dc bus voltage and gate resistance.

5.2 Intelligent Gate Driver for Overall Switching Performance Improvement

In addition to suppress cross-talk by means of the gate assist circuit, gate driver can further improve the switching performance via enhancing the driving capability. However, this gate driver design must depend on the fully understanding of switching characteristics of SiC devices under each switching subinterval; otherwise, more issues will be incurred, such as serious parasitic ringing, extremely high voltage spike. The unique properties of SiC device during switching transients are summarized as follows.

SiC switching behavior during turn-on and turn-off transients can be divided into four subintervals: switching delay subinterval, current commutation subinterval (i.e., *di/dt* transient), voltage commutation subinterval (i.e., *dv/dt* transient), and finally ensuing ringing subinterval [110]. Specifically, during the turn-on transient, the antiparallel Schottky diode enables the reverse recovery charge to be negligible, even at high *di/dt* and high operating temperature [27, 31]. Also, the modest transconductance and large internal gate resistance due to small chip size of SiC devices as compared to their silicon counterparts limit the *di/dt* as well [27, 31, 64]. Thus, unlike the design criterion of active gate driver for Si power devices, SiC based fast gate driver no longer need to limit the *di/dt* during the turn-on transient [71, 73]. However, high *dv/dt* induced cross-talk is critical for SiC devices on account of the low threshold voltage and large internal gate resistance [54, 130-132]. Therefore, the gate driver of SiC devices should have the capability of cross-talk suppression; otherwise, SiC switching speed has to be sacrificed to avoid the potential hazard of shoot-through failure induced by cross-talk [54]. During the turn-off transient, due to the low negative allowable maximum gate voltage, the spurious gate voltage triggered by cross-talk can easily exceed the gate voltage rating of SiC devices. Hence, similar to the turn-on transient, cross-talk mitigation during the turn-off transient is necessary for the gate

driver design [132]. In addition to the switching time and losses, the switch stress, especially the over-voltages during switching transients is another critical factor that must be taken into account for fast switching SiC devices. Fig. 5-12 shows the measured switching waveform of Cree 1200-V/20-A SiC MOSFETs operating at 600-V/10-A with 0-Ω gate resistance. Obviously, the over-voltage and ringing during the turn-on transient is more severe as compared to that during the turn-off transient. Therefore, it is better for SiC gate driver to be capable of adjusting the driving capability during turn-on and turn-off transients separately.

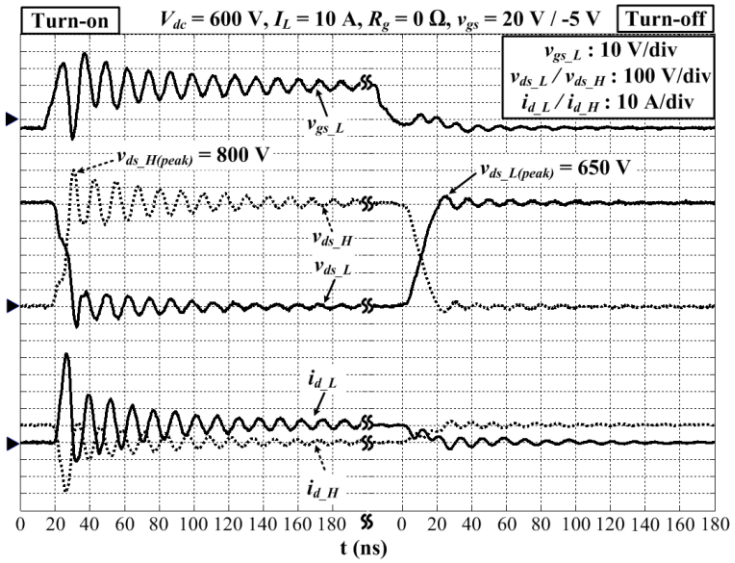


Fig. 5-12. Measured switching waveform of SiC devices.

According to the aforementioned discussion, an intelligent gate driver is proposed for fast switching and cross-talk suppression with less penalty of overstressing SiC devices. First, on the basis of the intrinsic properties of SiC device, the design criteria of gate drivers for both lower and upper switches in a phase-leg during turn-on and turn-off transients are investigated. Second, according to this driving strategy, an intelligent gate driver circuit is introduced; its structure and

operation principle are presented. Third, a double pulse tester with Cree 2nd generation 1200-V/20-A SiC MOSFETs is established to demonstrate the validity and effectiveness of this proposed approach.

5.2.1 Design Criteria

Assume the lower switch in a phase-leg as the device under operation, and the upper one to be the device under interference by cross-talk, the ideal gate voltages and gate loop impedances of each device during turn-on and turn-off transients are summarized as follows:

1) For the lower switch (i.e., the operating device) during the turn-on transient, the gate voltage is preferred to be the maximum allowable positive gate voltage $V_{gs\_max(+)}$ for the fast turn-on; after the turn-on transient, the gate voltage should be controlled as the normal on-state gate voltage V_{gs_on} to not overstress the gate-source terminals of power devices during the steady state. In addition, a relatively large gate resistor R_{g_on} during the turn-on transient should be selected to mitigate the serious ringing in both the gate loop and power loop (see Fig. 5-12). The gate resistor is used to tune the driving capability since it is the gate resistance that directly determines the damping factor and suppresses the ringing in the gate loop. During the turn-off transient, the gate voltage should be the maximum allowable negative gate voltage $V_{gs\_max(-)}$ for the fast turn-off; after the turn-off transient, the gate voltage should be 0 V to reduce the gate voltage stress as well as improve the response of the upcoming turn-on command. Also, the preferred gate resistor is 0 Ω during this transient since the related parasitic ringing and overvoltage during the turn-off transient with 0 Ω gate resistance are acceptable (see Fig. 5-12).

2) For the upper switch (i.e., the non-operating device) during the turn-on transient of the lower switch, the gate voltage should be the maximum allowable negative gate voltage $V_{gs\_max(-)}$

with the gate resistor of 0 Ω to reduce the positive spurious gate voltage induced by cross-talk, and decrease the possibility of shoot-through. During the turn-off transient of the lower switch, 0 V gate voltage together with 0 Ω gate resistor are preferred to minimize the peak value of negative spurious gate voltage within the required range [132].

The ideal gate voltages and resistors to best serve SiC devices in the phase-leg configuration during different switch states are summarized in Table 5-6.

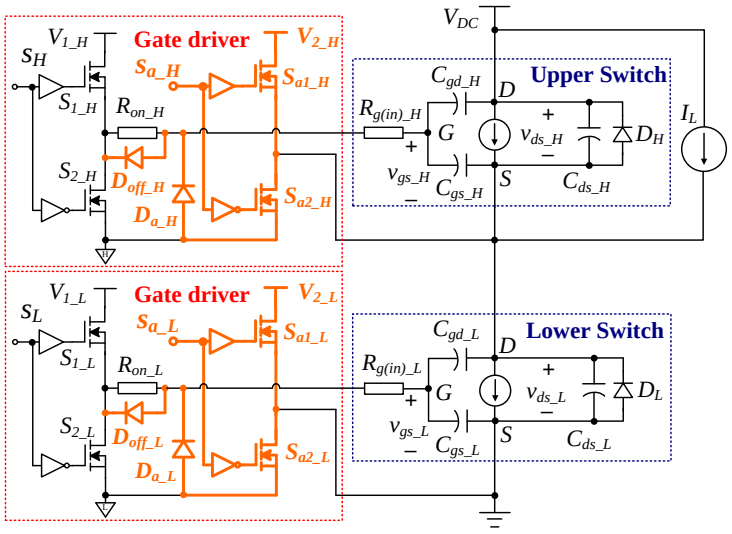
Table 5-6. Ideal Gate Voltages and Resistors When the Lower Switch Operates

Switch states	V_{g_L}	R_{g_L}	V_{g_H}	R_{g_H}
Turn-on transient	$V_{gs\_max(+)}$	R_{g_on}	$V_{gs\_max(-)}$	0 Ω
Turn-off transient	$V_{gs\_max(-)}$	0 Ω	0 V	0 Ω
On-state	V_{gs_on}	N/A	0 V	N/A
Off-state	0 V	N/A	0 V	N/A

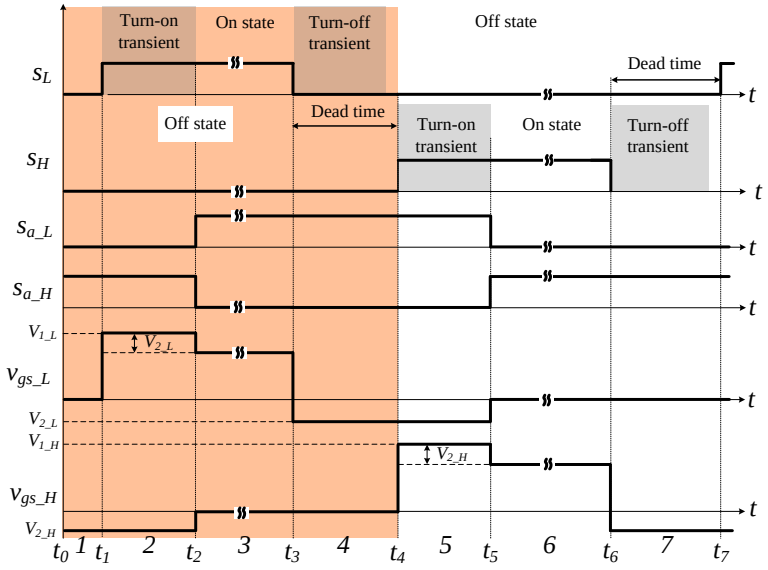
where V_{g_L} / V_{g_H} and R_{g_L} / R_{g_H} refer to gate voltages and resistors of lower and upper switches.

5.2.2 Structure and Operation Principle

Based on the aforementioned design criteria, an intelligent gate driver for fast switching and cross-talk suppression is proposed, as shown in Fig. 5-13. Compared with the conventional gate drive circuit (S_{1_H} and S_{2_H} orS_{1_L} and S_{2_L}), two auxiliary transistors (S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L}) together with two diodes (D_{a_H} and D_{off_H} or D_{a_L} and D_{off_L}) are added. Fig. 5-14 displays the operating procedure of the proposed gate assist circuit, described as follows.



(a) Gate assist circuit (S_{a1_H}, S_{a2_H}, D_{a_H}, D_{off_H} or S_{a1_L}, S_{a2_L}, D_{a_L}, D_{off_L}).

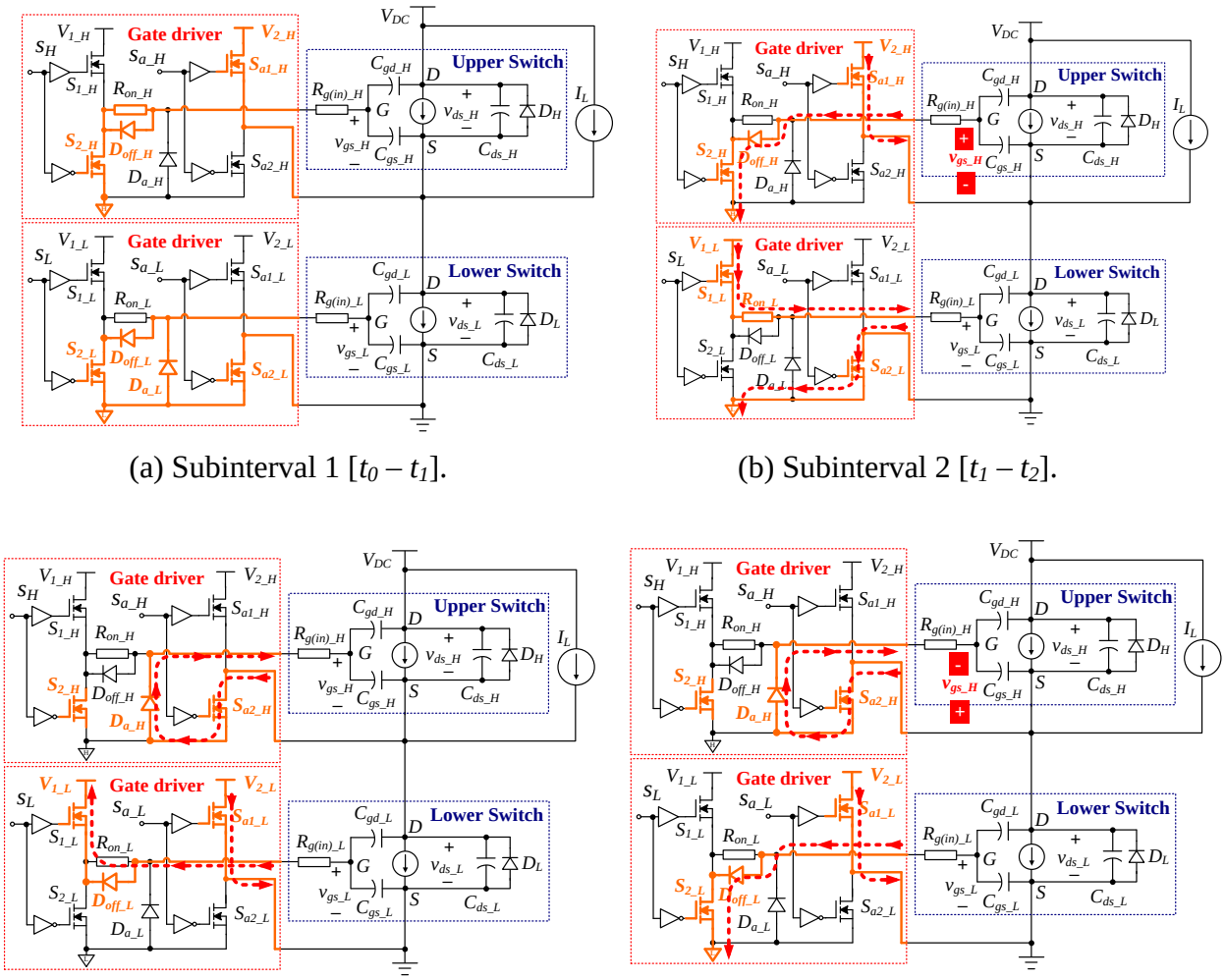


(b) Logic signals of main device (S_H or S_L) and auxiliary transistors (S_{a_H} or S_{a_L}).

Fig. 5-13. Intelligent gate driver for fast switching and cross-talk suppression.

Subinterval 1 [t_0 – t_1]: Off-state of the lower switch. For the lower gate driver, S_{2_L} and auxiliary transistor S_{a2_L} turn on, and the gate voltage of the lower switch is regulated to 0 V for gate voltage stress reduction as well as the fast response of the upcoming turn-on command. For

the upper gate driver, S_{2_H} and auxiliary transistor S_{a1_H} turn on, and the gate voltage of the upper switch is controlled to be $-V_{2\_H}$ to mitigate the cross-talk during the following turn-on transient.



(a) Subinterval 1 [$t_0 - t_1$].

(b) Subinterval 2 [$t_1 - t_2$].

(c) Subinterval 3 [$t_2 - t_3$].

(d) Subinterval 4 [$t_3 - t_4$].

Fig. 5-14. Operation principle of the intelligent gate driver from t_0 to t_4.

Subinterval 2 [$t_1 - t_2$]: Turn-on transient of the lower switch. For the lower gate driver, S_{1_L} turns on and auxiliary transistor S_{a2_L} stays on. Gate voltage of the lower switch is V_{1_H} which is

designed to be higher than the normal on-state gate voltage for the fast turn-on. And a relatively large gate resistor of R_{on_L} is to limit the parasitic ringing and device's voltage stress. For the upper gate driver, the states of the transistors remain the same, and the gate voltage of the upper switch stays $-V_{2\_H}$ with the gate resistor of 0 Ω. Both the negative gate voltage and small gate loop impedance are beneficial for mitigating the positive spurious gate voltage induced by cross-talk.

Subinterval 3 [$t_2 - t_3$]: On-state of the lower switch. For the lower gate driver, S_{1_L} stays on and auxiliary transistor S_{a1_L} turns on. Gate voltage of the lower switch is regulated to be the normal on-state gate voltage $V_{1\_H} - V_{2\_H}$ for the gate voltage stress reduction. For the upper gate driver, S_{2_H} stays on and auxiliary transistor S_{a2_H} turns on. Gate voltage of the upper switch becomes 0 V for the cross-talk mitigation during the upcoming turn-off transient.

Subinterval 4 [$t_3 - t_4$]: Turn-off transient of the lower switch. For the lower gate driver, S_{2_L} turns on and auxiliary transistor S_{a1_L} stays on. Gate voltage of the lower switch turns to be $-V_{2\_H}$ with the gate resistor of 0 Ω for the fast turn-off. For the upper gate driver, the states of the transistors remain the same, 0 V gate voltage of the upper switch with 0 Ω gate resistor are the most effective combination to minimize the negative spurious gate voltage induced by cross-talk.

Based on the circuit symmetry, the operation principle during switching transient of the upper switch, i.e., subintervals 4-7, as shown in Fig. 5-13(b), are similar to that during subintervals 1-4. Specifically, subintervals 4-7 correspond to turn-on transient of the upper switch, on-state of the upper switch, and turn-off transient of the upper switch, respectively. According to the operation principle, the logic signals for the control of auxiliary transistors can be synthesized merely based on the logic signals of the main devices using several logic gates.

Thus, through the feed-forward control, this gate assist circuit is well suited for SiC devices with fast switching capability.

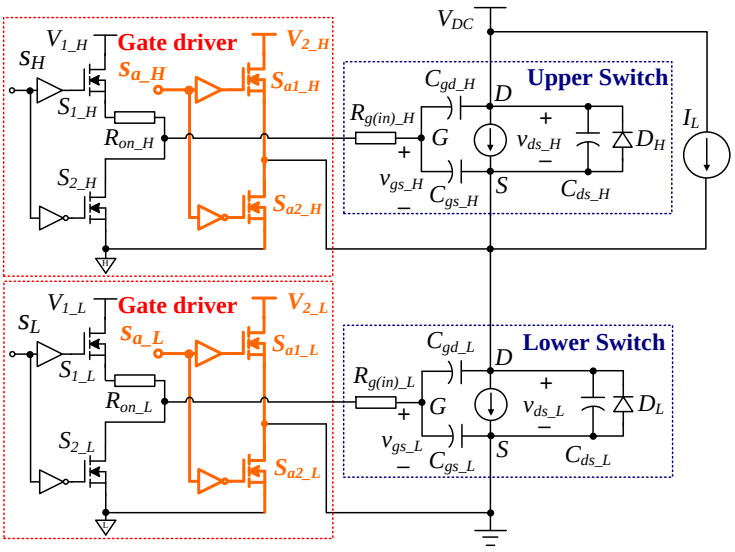


Fig. 5-15. Simplified intelligent gate driver with conventional gate driver having independent source/sink outputs.

Additionally, originated from the intelligent gate driver in Fig. 5-13(a), a simplified version consisting of only two auxiliary transistors (S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L}) with a simple modification of the conventional gate drive circuit (S_{1_H} and S_{2_H} or S_{1_L} and S_{2_L}) is proposed, as shown in Fig. 5-15. To achieve the same function of the aforementioned intelligent gate driver, this simplified alternative requires the conventional gate driver with independent source/sink outputs. Its logic signals for the control of auxiliary transistors and corresponding operation principles are the same.

5.2.3 Experimental Verification

A double pulse tester board with Cree 2nd generation 1200-V/20-A SiC MOSFETs is constructed as shown in Fig. 5-16. Fig. 5-17 displays the prototype gate driver board with the proposed driving strategy. According to the datasheet of the device under test, V_{1_H} and V_{1_L} are set to be 25 V, and V_{2_H} and V_{2_L} of 5 V are selected for the following experiment. The 5 V supplies for V_{2_H} and V_{2_L} are obtained from 25 V V_{1_H} and V_{1_L} by means of the voltage regulator. Table 5-7 lists gate voltages and gate resistors of each switch in a phase-leg when the lower switch is operating. As compared to data displayed in Table 5-6, the proposed intelligent gate driver almost achieves the optimal gate voltages and resistors under different switch states.

Also, via controlling the logic signals of the auxiliary transistors (i.e., S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L} in Fig. 5-13(a)), this gate driver board is able to achieve the same functionality as the conventional gate driver with 0 V turn-off gate voltage (i.e., turn on S_{a2_H} and S_{a2_L} in Fig. 5-13(a) during the switching interval) and with negative turn-off gate voltage (i.e., turn on S_{a1_H} and S_{a1_L} in Fig. 5-13(a) during the switching interval). Thus, by setting the mode selection jumper of gate driver board in Fig. 5-17, comparison experiments are carried out under four different groups (see Table 5-8) to evaluate the effectiveness of the proposed intelligent gate driver. Among them, the 3rd comparison group has the same gate voltage of the 2nd group, but with asymmetrical R_g for turn-on and turn-off transients, which is identical to the gate resistances of intelligent gate driver in the 4th group (i.e., R_{g_on} for turn-on and 0 Ω for turn-off). Each comparison group is tested with the gate resistances of 10/5/0 Ω, operating voltages of 400/600 V, operating currents of 5/10/15/20/25 /30/35 A, and junction temperatures of 25/68/107/150 ^{o}C.

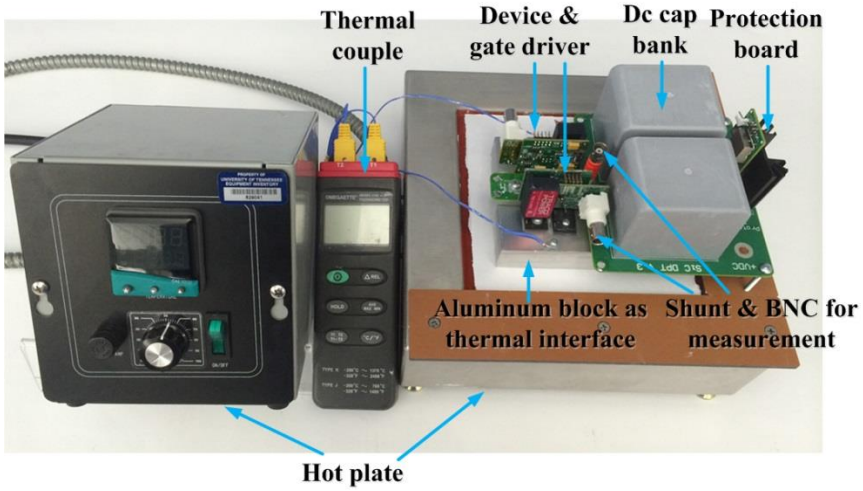
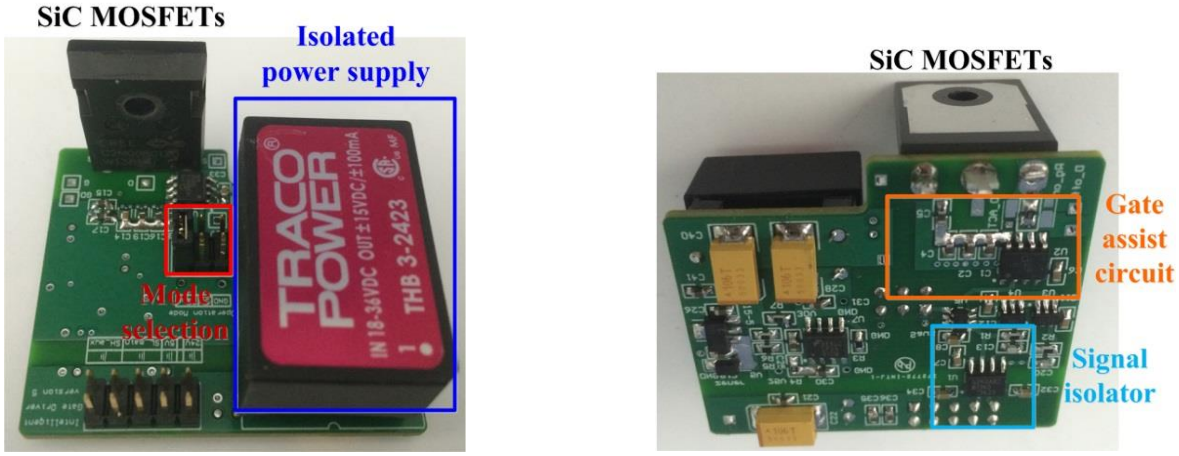


Fig. 5-16. Double pulse tester setup.



(a) Top view. (b) Bottom view.

Fig. 5-17. Intelligent gate driver board.

As can be observed in Fig. 5-18, in comparison with the two-level gate voltages of the conventional gate driver (i.e., 20/0 V of 1st group and 20/-5 V of 2nd group and 3rd group), the intelligent gate driver can output four-level gate voltages (i.e., 25/20/0/– 5 V) which are designed to best serve SiC devices under different switch states.

Table 5-7. Gate Voltages and Resistors Dependence on Different Switch States (Lower Switch Operates)

Switch states	V_{g_L}	R_{g_L}	V_{g_H}	R_{g_H}
Turn-on transient	25 V	R_{g_on}	– 5 V	0 Ω
Turn-off transient	– 5 V	0 Ω	0 V	0 Ω
On-state	20 V	N/A	0 V	N/A
Off-state	0 V	N/A	0 V	N/A

where V_{g_L} / V_{g_H} and R_{g_L} / R_{g_H} refer to gate voltages and resistors of lower and upper switches.

Table 5-8. Four Comparison Groups

1st Group	Conventional gate driver (CGD) with V_{gs} of 20/0 V
2nd Group	Conventional gate driver (CGD) with V_{gs} of 20/-5 V
3rd Group	Conventional gate driver (CGD) of 20/-5 V with asymmetrical R_g
4th Group	Proposed intelligent gate driver (IGD)

Fig. 5-19 shows the comparison waveforms of four different groups under the operating condition of 600-V/20-A with 5-Ω gate resistance at room temperature. The switching waveforms in Fig. 5-19(a) show that during the turn-on transient of the lower switch, the turn-on time by using intelligent gate driver reduces from 33.6 ns of the 1st gate driver and 32.8 ns of the 2nd gate driver to 27.2 ns, i.e., decreases by up to 24% and 21% as compared to the 1st and 2nd gate drivers, respectively. The *di/dt* and *dv/dt* during the turn-on transient increase as well. It is noted that the 2nd and 3rd groups have the same gate voltage and resistance during turn-on. Thus, their switching performances are almost identical, which are worse than the switching behavior by using the intelligent gate driver in the 4th group.

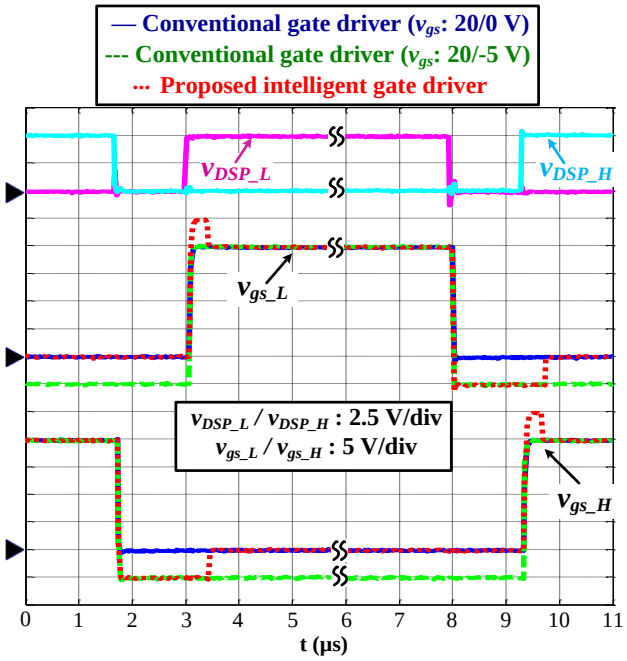
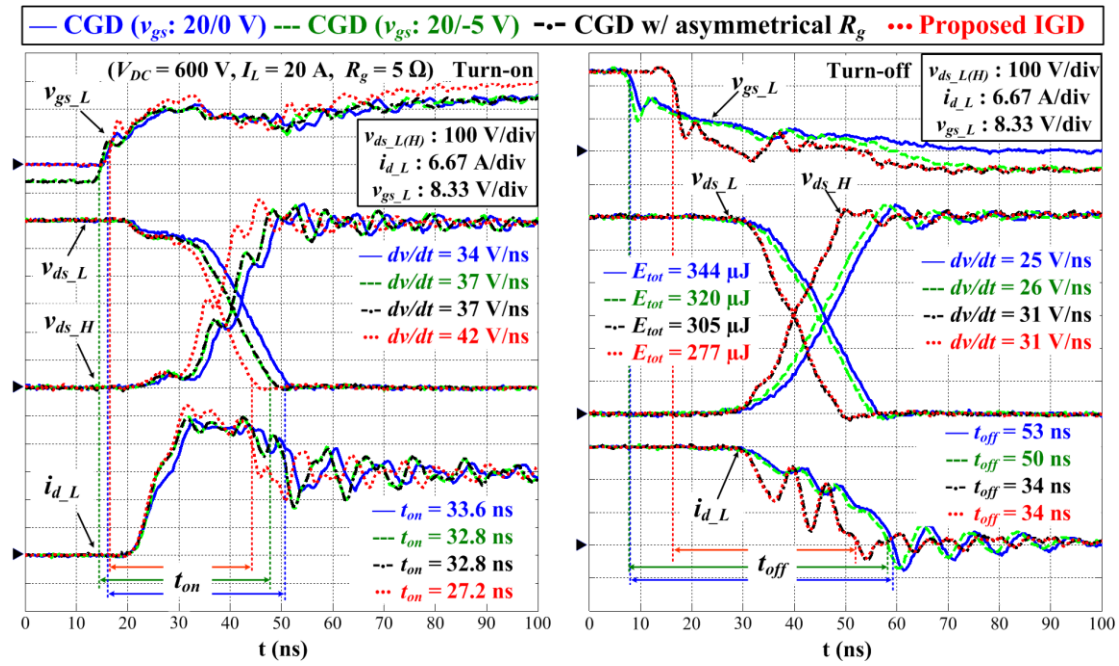
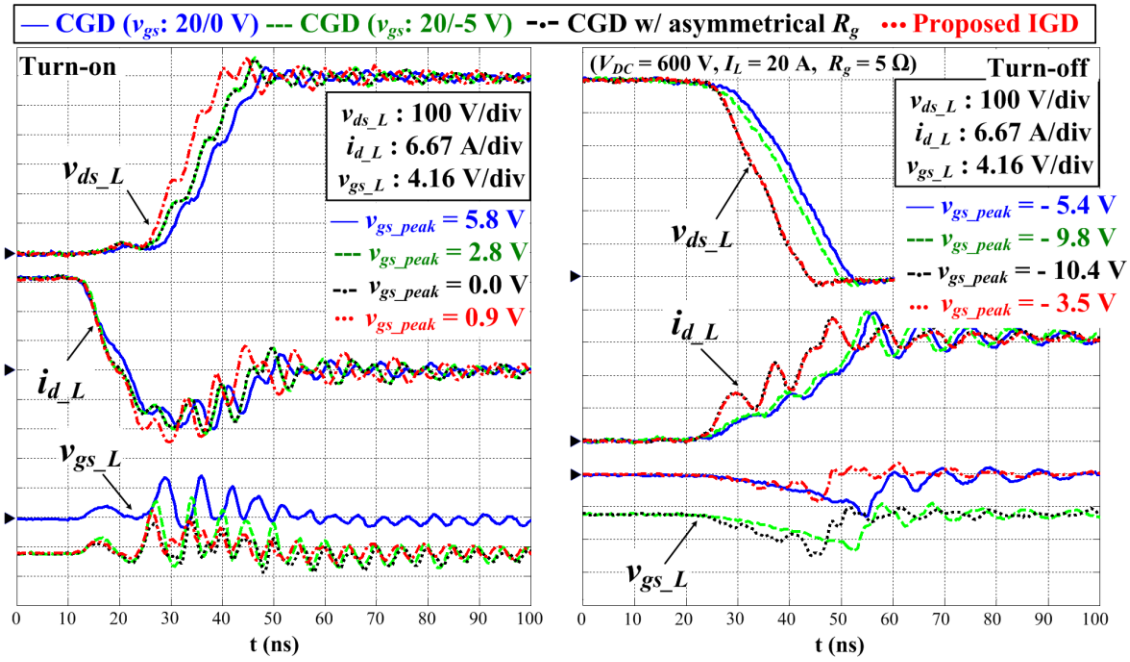


Fig. 5-18. Gate voltages for different gate drivers.

During the turn-off transient of the lower switch, as shown in Fig. 5-19(a), due to – 5 V gate voltage and 0 Ω gate resistance, the intelligent gate driver results in decreases of turn-off time from 53 ns (1st gate driver) and 50 ns (2nd gate driver) to 34 ns, namely the turn-off time by using intelligent gate driver reduces up to 56% (1st gate driver) and 47% (2nd gate driver). The *dv/dt* during the turn-off transient increases as well. Since the gate voltage and resistance of the 3rd group are the same as that of the intelligent gate driver in the 4th group, the turn-off waveforms by using the conventional gate driver with asymmetrical R_g is almost identical to that of the 4th group with intelligent gate driver. The total switching loss by using intelligent gate driver decreases by 24%, 16%, and 10% as compared to that of the 1st, 2nd, and 3rd gate drivers, respectively. Also note that the over-voltages during both turn-on and turn-off transients by means of intelligent gate driver are still within the acceptable ranges, although the switching speed increases significantly.



(a) Switching waveform comparison in terms of the switching speed.



(b) Switching waveform comparisons in terms of cross-talk performance.

Fig. 5-19. Switching waveforms comparison under 600-V/20-A with 5-Ω gate resistance: conventional gate drivers versus intelligent gate driver.

To identify the impact of cross-talk on the gate voltage of the non-operating switch by using different gate drivers, the waveforms of the lower switch are monitored during the switching transient of the upper one under the operating condition of 600-V/20-A with 5-Ω gate resistance at room temperature, as displayed in Fig. 5-19(b). It shows that during the turn-on transient of the upper switch, the positive spurious gate voltage of the lower switch by using the intelligent gate driver is minimized to be 0.9 V thanks to – 5 V gate voltage with 0 Ω gate resistance as compared to 5.8 V of the 1st gate driver, 2.8 V of the 2nd gate driver. Since the gate voltage and resistance for the 3rd gate driver are identical to the intelligent gate driver, but with slower switching speed, its spurious gate voltage is lower during the turn-on transient.

During the turn-off transient of the upper switch, the negative spurious gate voltage of the intelligent gate driver is minimized to be – 3.5 V thanks to 0 V gate voltage with 0 Ω gate resistance as compared to – 5.4 V of the 1st gate driver, – 9.8 V of the 2nd gate driver, and – 10.4 V for the 3rd gate driver. Also note that the measured gate voltage is the voltage across external gate-source terminals of the device. Considering the relatively large internal gate resistance, the internal gate voltage will be worse than the observation. For the tested SiC devices, – 10 V is the maximum allowable negative gate voltage.

Fig. 5-20 presents the comparison test results dependence on the load current under the dc bus voltage of 600-V with 5-Ω gate resistance. In order to clearly demonstrate the effectiveness of the intelligent gate driver, the switching loss and switching time under 1st, 2nd, and 3rd groups are normalized based on that under the 4th group, which are listed in Table 5-9. It shows that under different load currents, as compared to the conventional gate driver in 1st, 2nd, and 3rd groups, the intelligent gate driver is able to reduce the switching loss (see Fig. (b)), minimize the peak value of negative spurious gate voltages within its required range (see Fig. (c)), decrease

delay time and switching time during turn-on and turn-off transients (see Fig. (d-g)). Also, the over-voltages by means of the intelligent gate driver during both turn-on and turn-off transients are acceptable (see Fig. (h) and (i)).

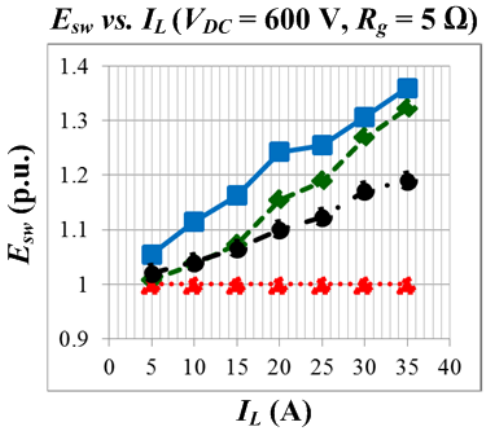
Similarly, Fig. 5-21and Fig. 5-22 illustrate the comparison test results dependence on dc bus voltage, gate resistance and junction temperature. The switching loss and time under the 1st, 2nd, and 3rd groups are managed the same as that in Fig. 5-20 according to the conditions under the 4th group listed in Table 5-10 and Table 5-11respectively. The experimental results show that with different dc bus voltages and gate resistances at varying junction temperatures, the intelligent gate driver in the 4th group has the capability to improve the switching behavior of power devices in a phase-leg in comparison with the conventional gate driver, such as reduced switching loss and switching time during both turn-on and turn-off transients, minimized peak value of negative spurious gate voltage due to the suppression of cross-talk. Moreover, the voltage spikes during both turn-on and turn-off transients by means of the intelligent gate driver slightly increases, but far beyond the breakdown voltage of the tested device.

Table 5-9. E_{sw} and Switching Time vs. I_L under 4th Group with 600-V / 5-Ω @ Room Temperature

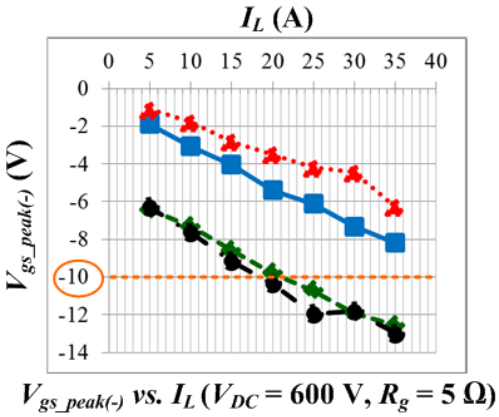
I_L	E_{sw}	$t_{d(on)}$	t_{on}	$t_{d(off)}$	t_{off}
5 A	169 μJ	4.0 ns	18.4 ns	25.6 ns	71.0 ns
10 A	197 μJ	4.8 ns	19.2 ns	20.4 ns	35.2 ns
15 A	237 μJ	4.8 ns	20.8 ns	16.8 ns	24.8 ns
20 A	277 μJ	5.2 ns	22.0 ns	15.6 ns	18.8 ns
25 A	344 μJ	4.8 ns	24.0 ns	14.8 ns	16.4 ns
30 A	408 μJ	4.8 ns	25.2 ns	14.4 ns	14.8 ns
35 A	480 μJ	4.8 ns	26.8 ns	13.6 ns	13.6 ns

Fig. 5-20. Comparison test results dependence on load current.

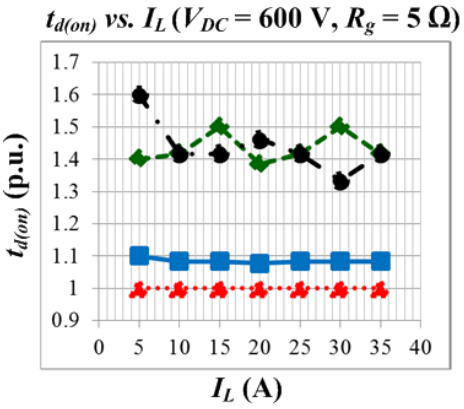
(a) Labels of comparison groups.



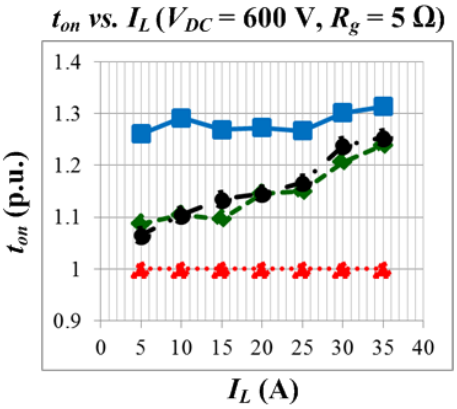
(b) E_{sw} dependence on I_L.



(c) $V_{gs\_peak(-)}$ dependence on I_L.

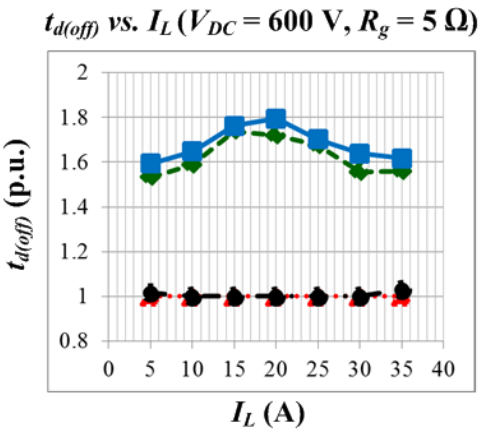


(d) $t_{d(on)}$ dependence on I_L.

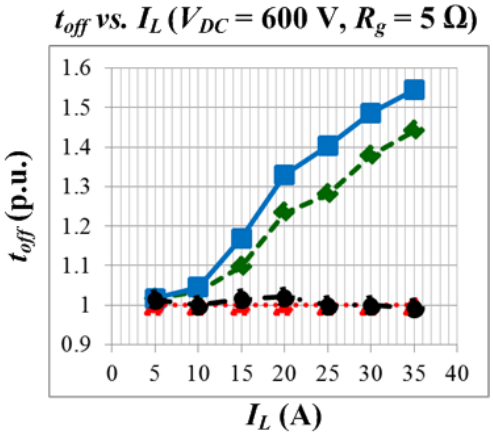


(e) t_{on} dependence on I_L.

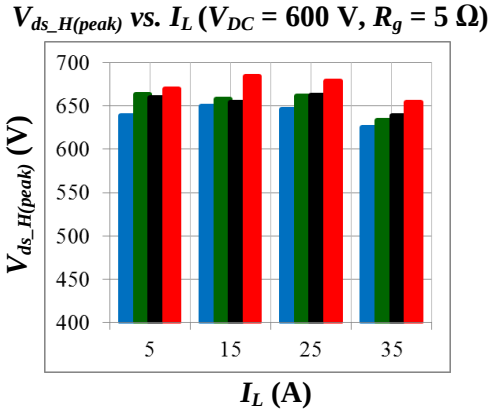
Fig. 5-20. Continued.



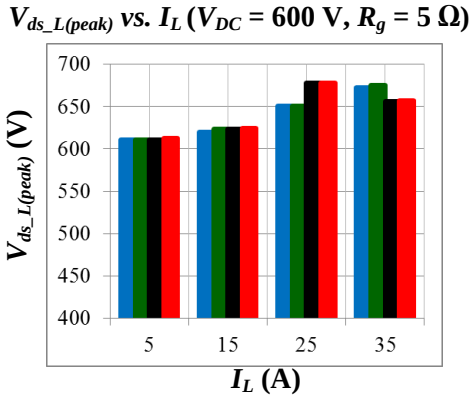
(f) $t_{d(off)}$ dependence on I_L.



(g) t_{off} dependence on I_L.



(h) $V_{ds\_H(peak)}$ dependence on I_L.

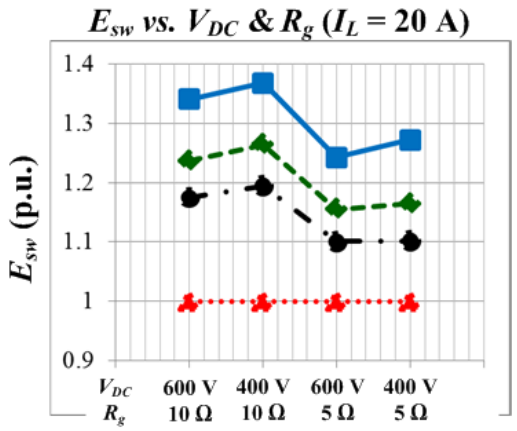


(i) $V_{ds\_L(peak)}$ dependence on I_L.

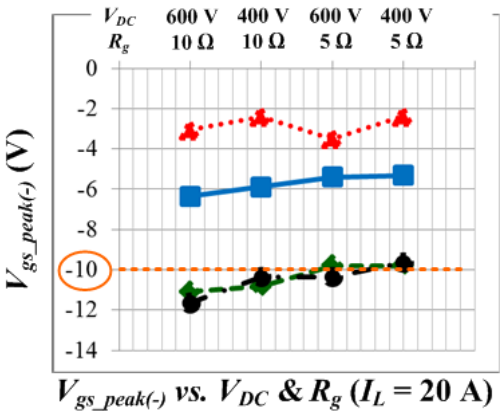
Fig. 5-20. Continued.

Fig. 5-21. Comparison test results dependence on dc bus voltage and gate resistance.

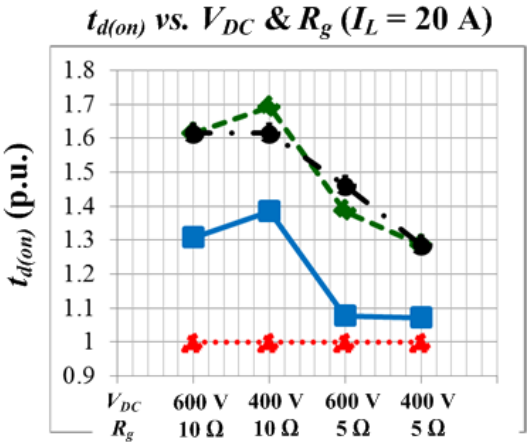
(a) Labels of comparison groups.



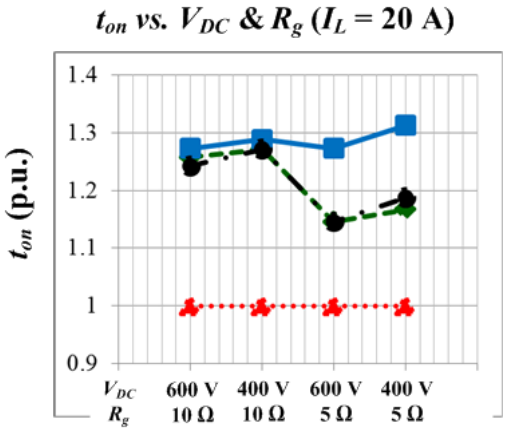
(b) E_{sw} dependence on V_{DC} and R_g.



(c) $V_{gs\_peak(-)}$ dependence on V_{DC} and R_g.

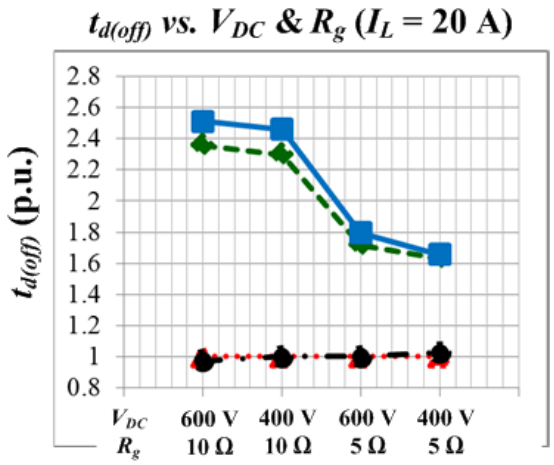


(d) $t_{d(on)}$ dependence on V_{DC} and R_g.

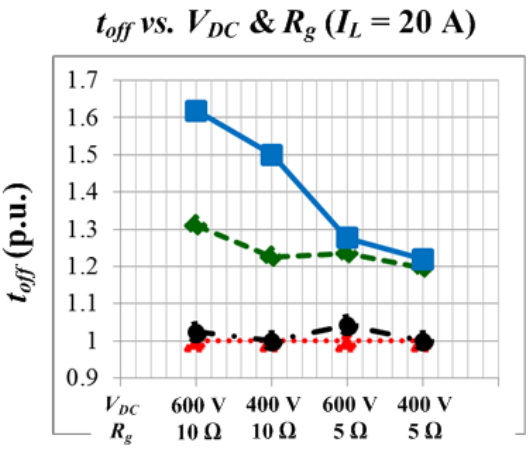


(e) t_{on} dependence on V_{DC} and R_g.

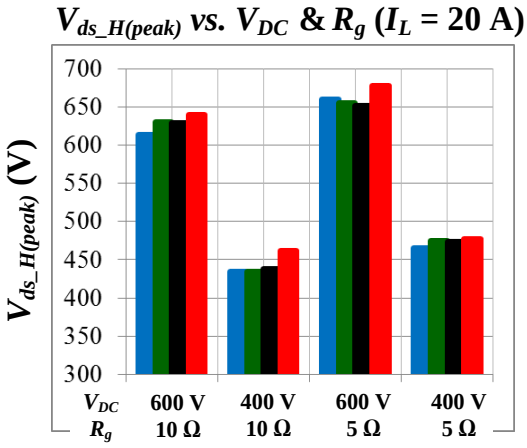
Fig. 5-21. Continued.



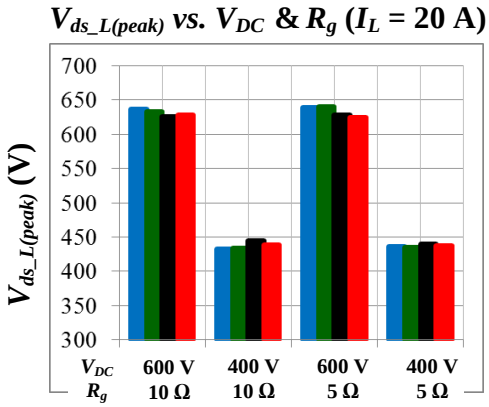
(f) $t_{d(off)}$ dependence on V_{DC} and R_g.



(g) t_{off} dependence on V_{DC} and R_g.



(h) $V_{ds\_H(peak)}$ dependence on V_{DC} and R_g.

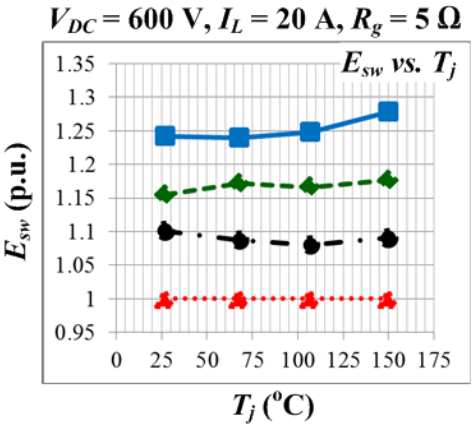


(i) $V_{ds\_L(peak)}$ dependence on V_{DC} and R_g.

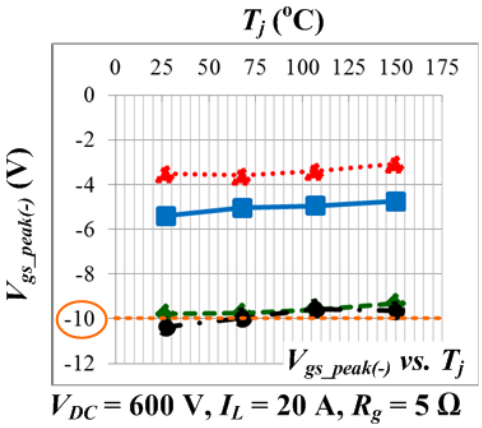
Fig. 5-21. Continued.

Fig. 5-22. Comparison test results dependence on junction temperature.

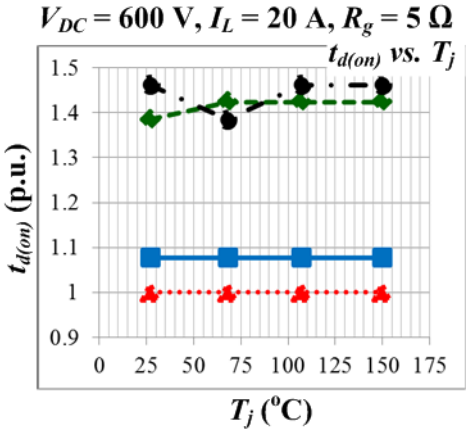
(a) Labels of comparison groups.



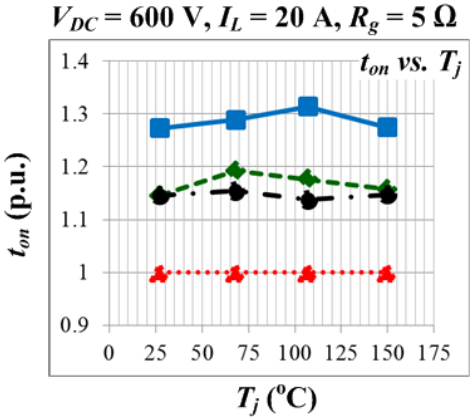
(b) E_{sw} dependence on T_j.



(c) $V_{gs\_peak(-)}$ dependence on T_j.

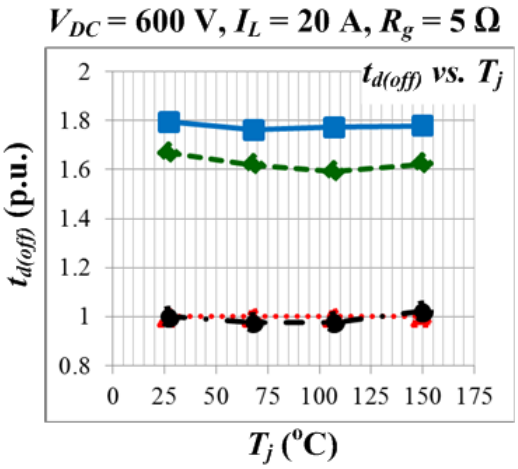


(d) $t_{d(on)}$ dependence on T_j.

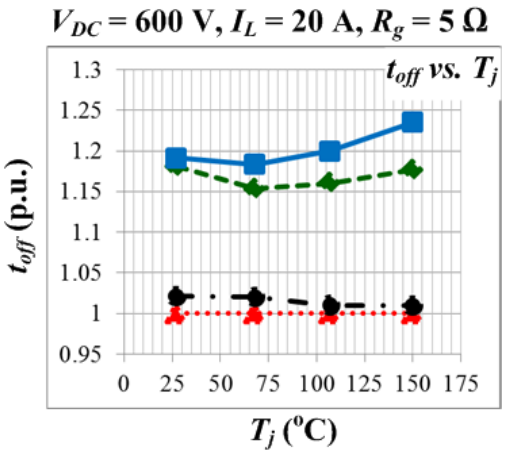


(e) t_{on} dependence on T_j.

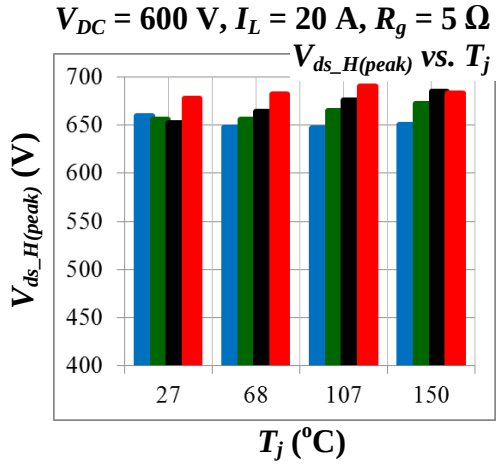
Fig. 5-22. Continued.



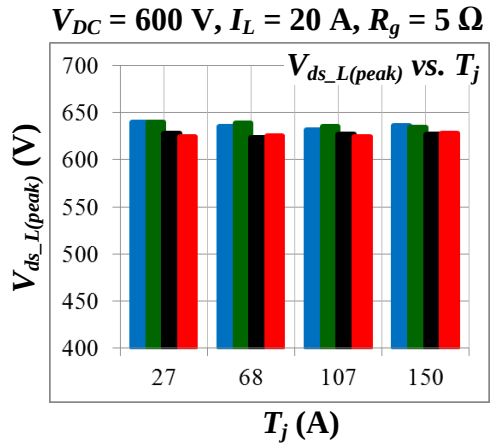
(f) $t_{d(off)}$ dependence on T_j.



(g) t_{off} dependence on T_j.



(h) $V_{ds\_H(peak)}$ dependence on T_j.



(i) $V_{ds\_L(peak)}$ dependence on T_j.

Fig. 5-22. Continued.

Table 5-10. E_{sw} and Switching Time vs. V_{DC} and R_g Under 4th Group with I_L of 20 A

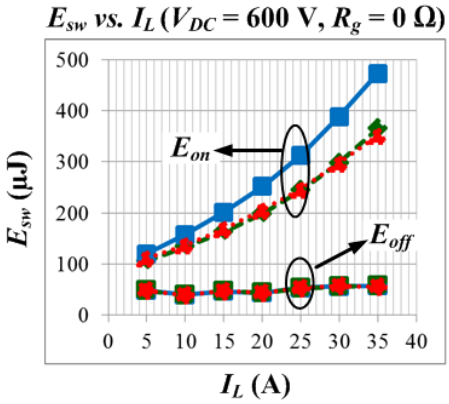
V_{DC}	R_g	E_{sw}	$t_{d(on)}$	t_{on}	$t_{d(off)}$	t_{off}
600 V	10 Ω	304 μJ	5.2 ns	26.4 ns	15.6 ns	16.8 ns
400 V	10 Ω	169 μJ	5.2 ns	23.6 ns	14.8 ns	16.0 ns
600 V	5 Ω	277 μJ	5.2 ns	22.0 ns	15.6 ns	18.8 ns
400 V	5 Ω	152 μJ	5.6 ns	19.2 ns	15.2 ns	16.4 ns

Table 5-11. E_{sw} and Switching Time vs. T_j Under 4th Group with 600-V/ 20-A / 5-Ω

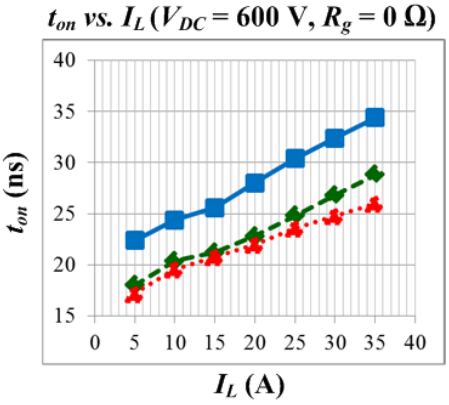
T_j	E_{sw}	$t_{d(on)}$	t_{on}	$t_{d(off)}$	t_{off}
27 °C	277 μJ	5.2 ns	22.0 ns	15.6 ns	18.8 ns
68 °C	275 μJ	5.2 ns	20.8 ns	16.8 ns	19.6 ns
107 °C	275 μJ	5.2 ns	20.4 ns	17.6 ns	20.0 ns
150 °C	273 μJ	5.2 ns	20.4 ns	18 ns	20.4 ns

Since the designed double pulse tester board leverages the optimal interconnection techniques investigated in chapter 6, it is pleased to note that the voltage spike and parasitic ringing during the turn-on transient with the gate resistance of 5 Ω is not severe. To further accelerate the switching speed of the tested device, 0 Ω gate resistance is used for the experimental comparison among different gate driving schemes. Since the gate resistance is set to be 0 Ω, the gate driver circuits in 2nd and 3rd comparison groups become identical. Hence, only three comparison groups are conducted, as shown in Fig. 5-23(a).

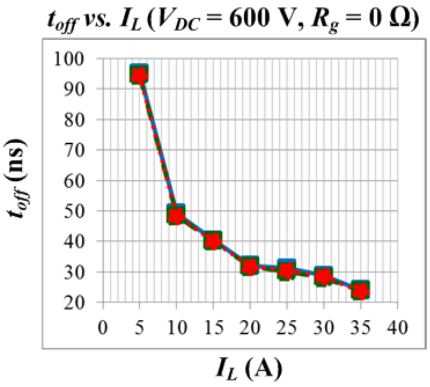
(a) Labels of comparison groups.



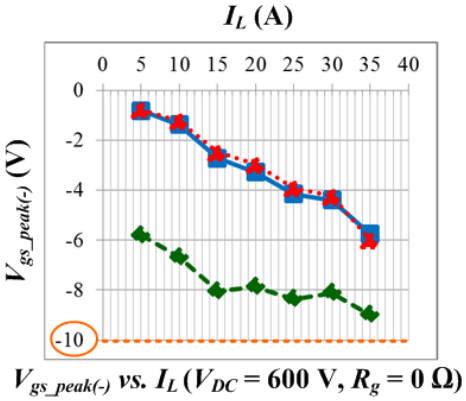
(b) E_{sw} dependence on I_L.



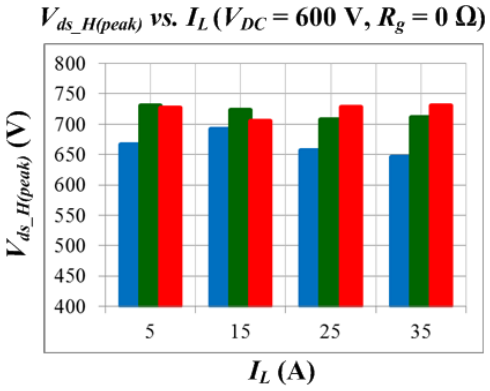
(c) t_{on} dependence on I_L.



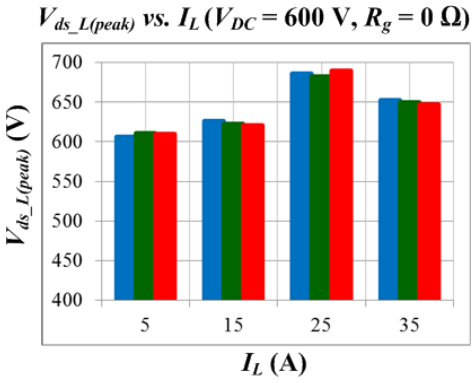
(d) t_{off} dependence on I_L.



(e) $V_{gs\_peak(-)}$ dependence on I_L.



(f) $V_{ds\_H(peak)}$ dependence on I_L.



(g) $V_{ds\_L(peak)}$ dependence on I_L.

Fig. 5-23. Comparison test results dependence on load current.

Under different operating conditions, Fig. 5-23(b-d) illustrate that the intelligent gate driver is able to reduce the switching loss with shorter switching time during the turn-on transient, but with nearly identical turn-off switching losses and turn-off time among different gate driver circuits. The reason why the turn-off switching losses are regardless of gate driver schemes is because of the strong gate driving capability makes the turn-off transition dominated by power loop parameters. I.e., the gate driver no longer determines the turn-off behavior [133]. In the end, the total switching loss by using the intelligent gate driver reduces by 35% and 6% as compared to the switching loss in 1^{st} and 2^{nd} groups, respectively, under the operating condition of 600-V/35-A. Additionally, the peak value of negative spurious gate voltages by using the intelligent gate driver are within the required range and almost always lower than the other conventional gate driver circuits, as shown in Fig. 5-23(e). Fig. 5-23(f-g) display that voltage spikes during both turn-on and turn-off transients are far beyond the breakdown voltage of the tested device. Accordingly, the proposed intelligent gate driver with 0 Ω gate resistance is capable of improving the turn-on switching performance with less penalty of overstressing the device under test.

In total, Fig. 5-24 summarizes the switching performance by using different gate drivers, the proposed intelligent gate driver has the capability of improving the overall switching performance of SiC devices.

5.3 Conclusion

Three intelligent gate drivers are developed for cross-talk suppression and overall switching performance improvement.

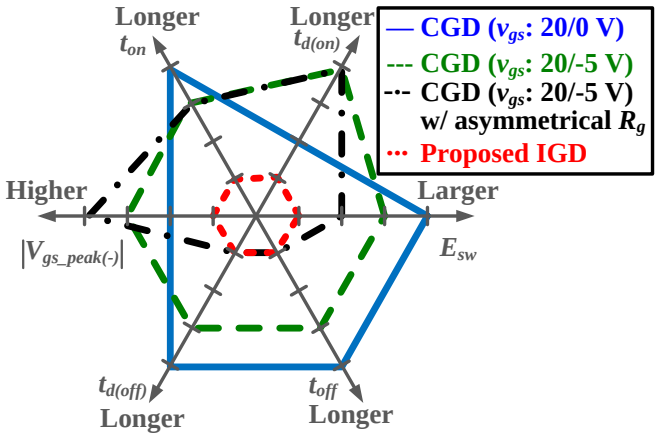


Fig. 5-24. Summary of switching performance by different gate drivers.

First, considering SiC devices with low threshold voltage, low maximum allowable negative gate voltage, and large internal gate resistance, two gate assist circuits are investigated for cross-talk suppression. The test results using Cree 1200-V/24-A SiC MOSFETs show that both gate assist circuits improve the switching performance under different operating conditions in comparison with the conventional gate drive, even with −2 V turn-off gate voltage: turn-on transient becomes fast, turn-on switching losses are reduced up to 17%, and spurious negative gate voltage is minimized within its maximum required range. In addition, compared with the gate voltage control (GVC) assist circuit with two transistors and one diode, the gate impedance regulation (GIR) circuit with one transistor and one capacitor is simpler, but less effective for cross-talk suppression due to the large internal gate resistance of SiC devices. Furthermore, the gate impedance regulation (GIR) circuit is a suitable gate assist methodology for board-level integration, while the all transistor based gate voltage control (GVC) assist circuit is a more promising option for cross-talk suppression for gate driver chip-level integration.

Second, based on the intrinsic characteristics of SiC power devices, such as modest transconductance, relatively large internal gate resistance, and high susceptibility of cross-talk,

an intelligent gate driver employing two auxiliary transistors together with two diodes is proposed for fast switching and cross-talk suppression. The test results with Cree 2nd generation 1200-V/20-A SiC MOSFETs verify that this approach has the capability of tuning gate voltage and gate loop resistance during different switching transients so that the lower and upper switches in a phase-leg can be best served. As compared to the conventional gate drivers, the overall switching performance has been improved by means of the proposed intelligent gate driver: switching time decreases by up to 24% during turn-on and 56% during turn-off at the tested operating point with the switching energy loss reduction by 24%. The spurious gate voltages induced by cross-talk are always maintained within the required range during both turn-on and turn-off transients. This gate driver strategy offers a simple, efficient, and cost-effective solution to increase the utilization of the high switching-speed capabilities of SiC devices. Also, it is a promising option for gate driver chip-level integration.

Table 5-12 summarizes the feature comparison of three intelligent gate drivers.

Table 5-12. Summary of Different Intelligent Gate Drivers

	GIR gate assist circuit	GVC gate assist circuit	3rd intelligent gate driver
Operating principle & effectiveness	Gate impedance regulation for cross-talk mitigation	Gate voltage control for cross-talk elimination (more effective than GIR gate assist circuit)	Gate impedance & voltage control for cross-talk suppression and switching speed acceleration (most effective approach)
Auxiliary components	Two auxiliary components (one transistor + one cap)	Three auxiliary components (all transistors based)	Four auxiliary components (all transistors based)
Logic signal synthesis circuit	Simple circuitry for logic signal generation	A fewer gates for logic signal synthesis	Simple circuitry for logic signal generation
Implementation method	Convenient for board level integration	Suitable for gate driver chip assembly	Suitable for gate driver chip assembly

6 Interconnection Design Optimization for Switching Performance Improvement of SiC Devices

This chapter presents the optimization of interconnection design to mitigate the adverse effect of parasitics on switching performance. According to the critical impact factors of high switching-speed capability of SiC devices identified in chapter 4, in addition to the cross-talk, which has been suppressed by the intelligent gate driver proposed in chapter 5, parasitic inductance associated in the switching loop significantly worsens the parasitic ringing and voltage spikes, especially during the turn-on transient. Also, the switching performance is greatly affected by the interaction between power device and inductive load. To cope with these issues, first, the placement of gate drivers, power devices and power stage as well as layout design are investigated to minimize the critical parasitics in the switching loop. Second, a dedicated auxiliary filter is designed and inserted between the converter and inductive load so that the inductive load's parasitics will not be "seen" from the converter side during the switching transient. The discrete Cree SiC MOSFETs with TO-247 package and the motor load are selected as the power device and inductive load under investigation in this chapter.

6.1 Switching Loop Parasitic Minimization for Power Devices with TO Package

In an actual voltage source converter, as shown in Fig. 6-1, the switching loop associated parasitic inductance are contributed by the interconnection among power devices' bare dies, gate driver and dc decoupling capacitor bank, specifically including bonding wires and leads related parasitics inductance from package, PCB trace induced inductance and equivalent series inductance (ESL) of decoupling capacitors.

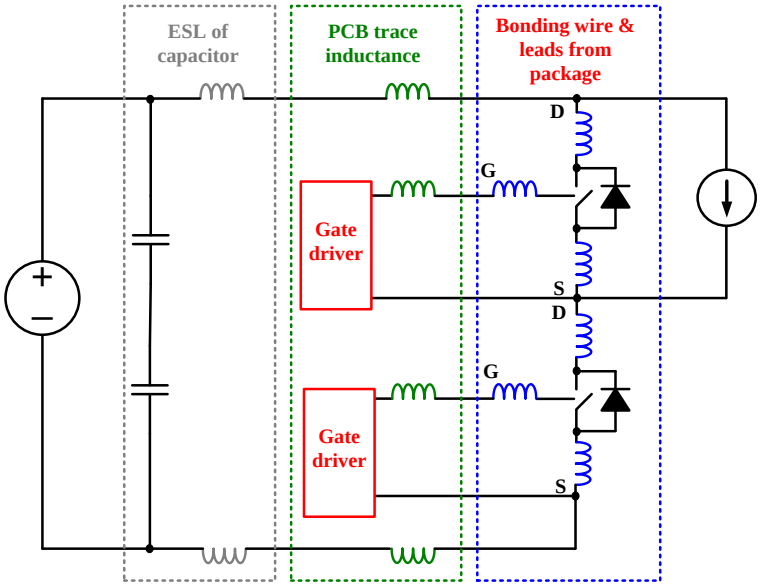


Fig. 6-1. Distribution of interconnection parasitics.

Among them, bonding wires are embedded in the devices' package. As device users, we have to accept their induced parasitic inductances. The leads of power devices act as a connector to assemble power device, gate driver, and power stage board. To minimize the effective length of the lead in the switching loop, the placement of power device, gate driver, and power stage board need to be investigated. The PCB trace induced inductance greatly depends on the PCB layout design. Hence, the optimal PCB layout design of gate driver and power stage should be studied, especial attention is paid on the power stage board since the impact of the power loop parasitic inductance on the switching behavior is more severe than that due to gate loop parasitics. For dc decoupling capacitors, surface mount ceramic capacitors are popular. Their ESL is determined by chip size, given by [134]

$$ESL = 394.727 \times 1.052^{L} \times 1.317^{L/W} \tag{6-1}$$

where L and W refer to the length and width of ceramic capacitor's package. As listed in Table 6-1, ESL of commonly-used chip styles of 100 nF ceramic capacitors for high voltage application

is around 1 nH to 1.5 nH, which is much smaller than 30 nH, the package induced parasitic inductance of the state-of-art SiC power module [135]. Moreover, the decoupling capacitor bank per phase-leg usually consists of several ceramic capacitors in parallel, which results in a smaller equivalent ESL. Therefore, the parasitic inductance due to ESL of decoupling capacitor bank can be ignored.

Table 6-1. ESL of 100 nF Surface Mount Ceramic Capacitors for 1000 V Voltage Rating

Chip Style	L/W	L	ESL
2225	22/25	22	1534 pH
2220	22/20	22	1680 pH
1825	18/25	18	1175 pH
1812	18/12	18	1425 pH

In total, the effort of parasitic minimization in this section focuses on the placement of power device, gate driver, and power stage board to reduce the effective length of device's leads in the switching loop and PCB layout design for the power stage board.

6.1.1 Placement of Gate Driver, Power Device and Power Stage

Fig. 6-2 displays an industry standard TO-series package, which is the most popular package for discrete SiC devices in today's market. Based on power devices of TO-series package, the conventional placement of power devices, gate drivers and power stage board in the phase-leg configuration is displayed in Fig. 6-3. In this design, the lead associated with the source terminal of devices involves in both gate loop and power loop, resulting in an inevitable common source

inductance. To minimize this lead induced common source inductance, a Kelvin connection with separate source return path is recommended by power device manufacturers [31]. I.e., a new source terminal is manually created by soldering a pin at the root of the device's source lead for the gate loop, as shown in Fig. 6-4. Thereby, the source paths for the gate loop and power loop are separated externally, and then the common source inductance is reduced.

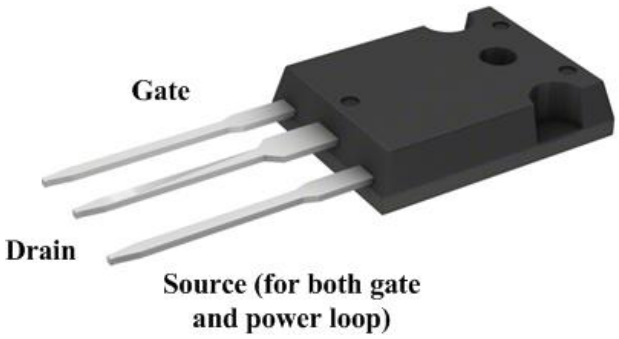


Fig. 6-2. Standard TO-series package.

However, for the aforementioned two placements, the leads of the device are first bended, and then soldered into the PCB. No matter how close the PCB is placed on the top of power devices, at least 5 mm lead is necessary considering the height of the device, thickness of the PCB as well as the size of components mounted on the bottom of the PCB. Practically, the lead associated parasitics per mm is around 1 nH [35]. Hence, there will be around 10 nH additional parasitic inductance induced by leads of lower and upper switches in a phase-leg, which will greatly impact the parasitic ringing and over-voltage during the fast switching transient.

To further minimize the effective length of leads involved in the switching loop, a new placement of power devices, gate drivers and power stage board is proposed, as shown in Fig. 6-5. Separated from the power stage board, a gate driver daughter board is placed perpendicular to

the power device and soldered at the root of device's gate and source leads, and then drain and source leads of the device directly attach the surface of the power stage board. Therefore, the effective lead lengths in both gate and power loop are greatly reduced. Also note that this new placement remains the Kelvin connection, namely, there is no extra common source inductance induced by the source lead of power devices. In total, the minimum common source and power loop parasitic inductances can be achieved.

Based on Q3D Extractor, the gate loop, power loop and common source inductances for different placement styles are simulated, and listed in Table 6-2. As compared to the conventional and Kelvin connection based placements, the proposed placement enables the power loop inductance to decrease by up to 28.6%. Also, its common source inductance reduces by 29.4% when compared with that of the conventional placement and is almost identical to the optimal common source inductance achieved by the Kelvin connection based placement.

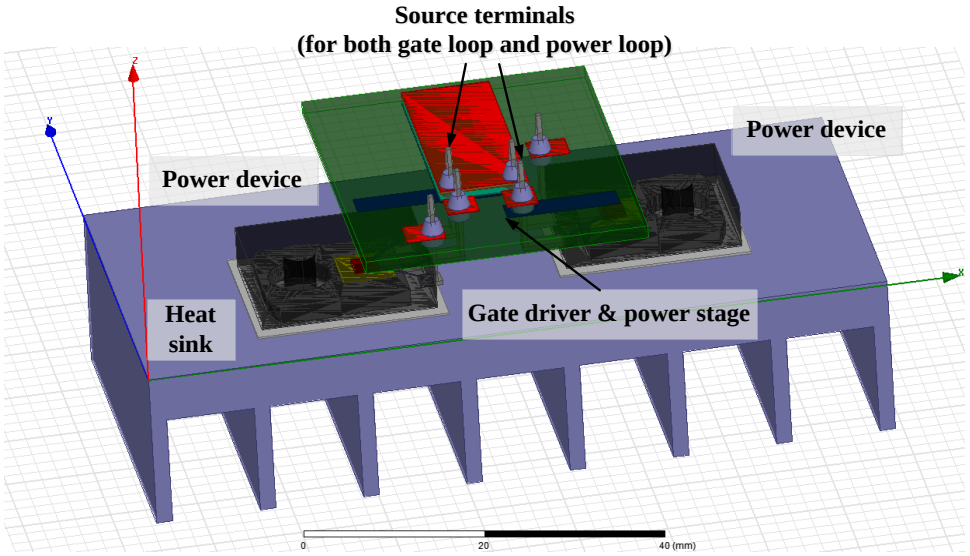


Fig. 6-3. Conventional placement of power devices, gate drivers and power stage board in the phase-leg configuration.

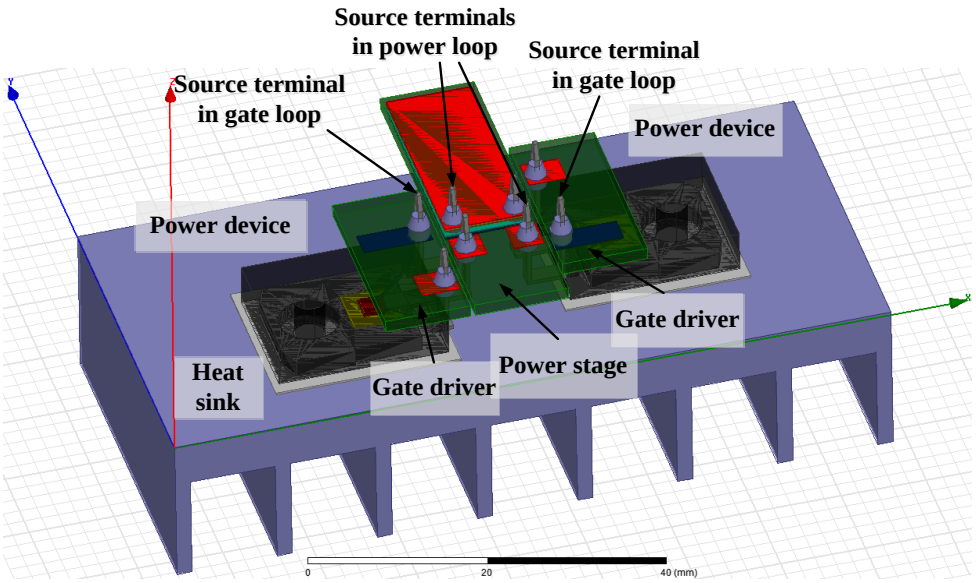


Fig. 6-4. Placement of power devices, gate drivers and power stage board in the phase-leg configuration with Kelvin connection.

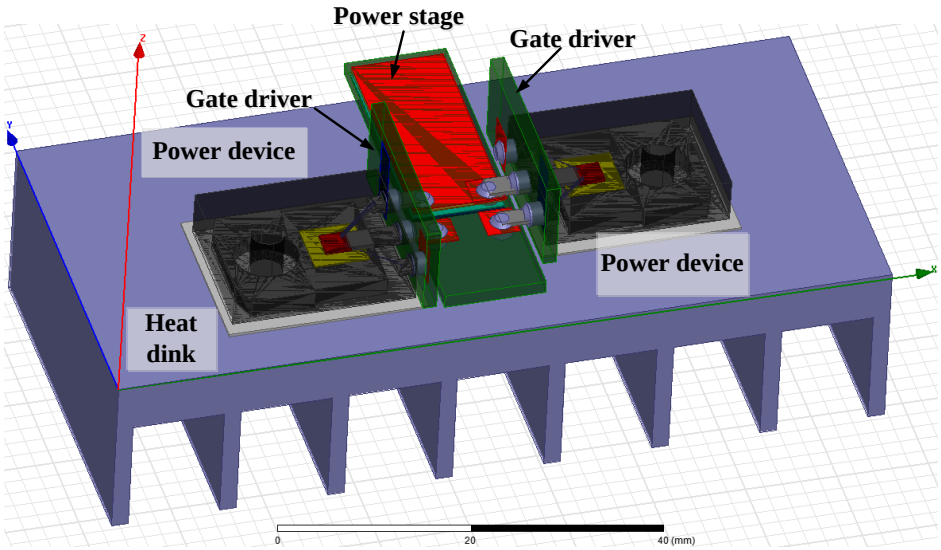


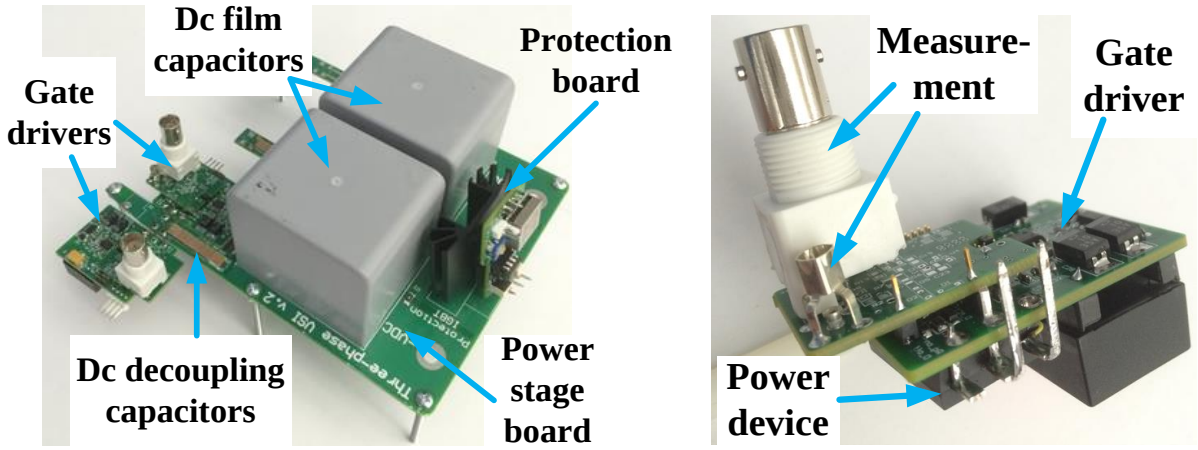
Fig. 6-5. Proposed placement of power devices, gate drivers and power stage board in the phase-leg configuration.

To further verify the effectiveness of the proposed placement on the switching performance, based on Cree 2nd generation 1200-V/36-A SiC MOSFETs, a voltage source converter is built with power stage board and gate driver daughter boards, as shown in Fig. 6-6. Sharing with the same power devices, gate drivers and power stage board, Fig. 6-7 - Fig. 6-9 display the voltage source converters with different assemblies according to three placement styles discussed above. Therefore, switching behavior differences measured afterwards merely come from different placements. Also note that the gate driver board is designed based on the intelligent gate driving scheme proposed in chapter 5.

Fig. 6-10 shows the comparison waveforms of three different placements under the operating condition of 600-V/25-A with 0-Ω gate resistance. The switching waveforms in Fig. 6-10(a) show that during the turn-on transient of the lower switch, as compared to the conventional placement, the switching time by using the proposed placement decreases from 28.0 ns to 23.6 ns. Although the drain current cannot be directly measured in this hardware setup, the shorter interval from the moment when the drain-source voltage starts to drop to the moment at which the drain-source voltage falls rapidly (i.e., t_{di_dt} in Fig. 6-10(a)) by using the proposed approach clearly indicates that the current rise time with respect to the conventional placement is longer. This means that the primary contributor of the increased turn-on speed for the proposed approach is because of less common source inductance, which agrees with the Q3D simulation results in Table 6-2. Additionally, as compared to the Kelvin connection based placement, it is observed that the voltage spike by using the proposed placement is significantly suppressed from 820 V to 697 V with less severe parasitic ringing. This is due to the smaller power loop inductance achieved by shorter effective lead length involved in the switching loop.

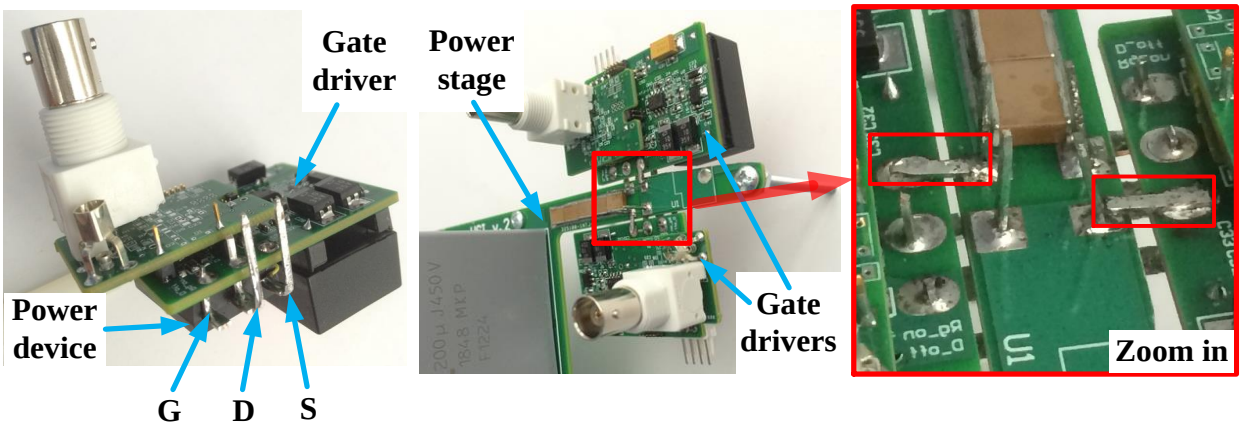
Table 6-2. Parasitic Inductance Dependence on Different Placements Based on Q3D

Placement style	Gate loop inductance	Power loop inductance	Common source inductance
Conventional placement	20.4 nH	23.9 nH	6.8 nH
Kelvin connection based placement	17.7 nH	23.8 nH	4.5 nH
Proposed placement	15.2 nH	17.0 nH	4.8 nH



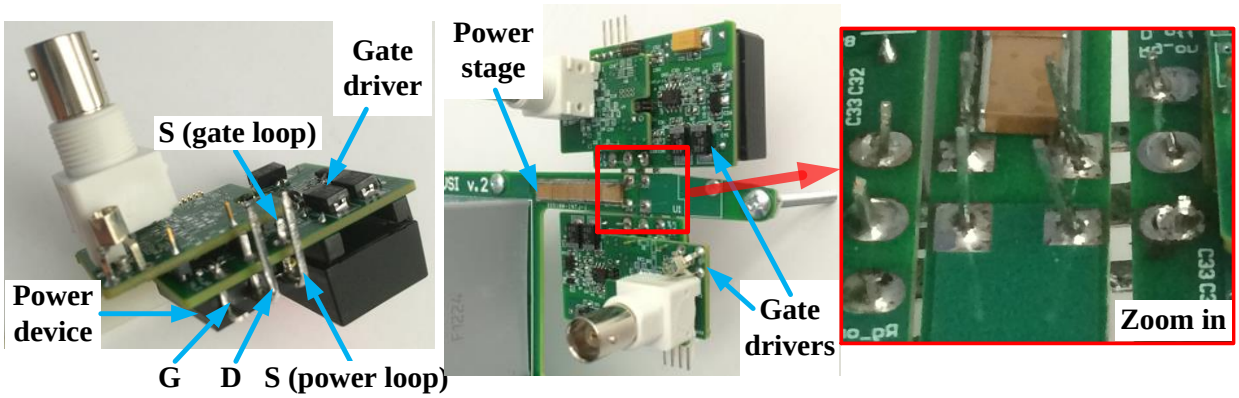
(a) Power stage with gate driver daughter boards. (b) Gate driver daughter board.

Fig. 6-6. Hardware setup for different placements comparison.



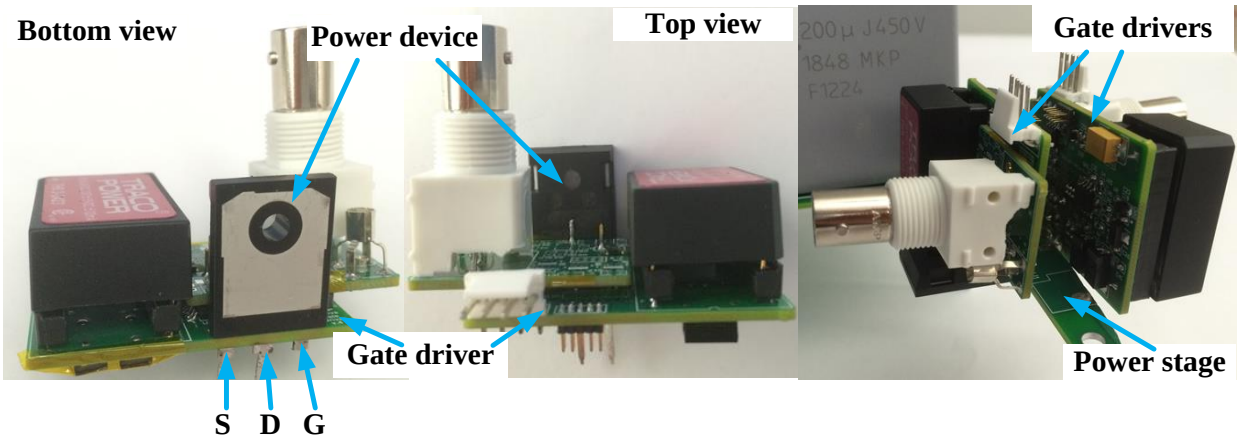
(a) Gate driver versus power device. (b) Power stage versus gate drivers.

Fig. 6-7. Phase-leg configuration built with the conventional placement.



(a) Gate driver versus power device. (b) Power stage versus gate drivers.

Fig. 6-8. Phase-leg configuration built with the Kelvin connection based placement.



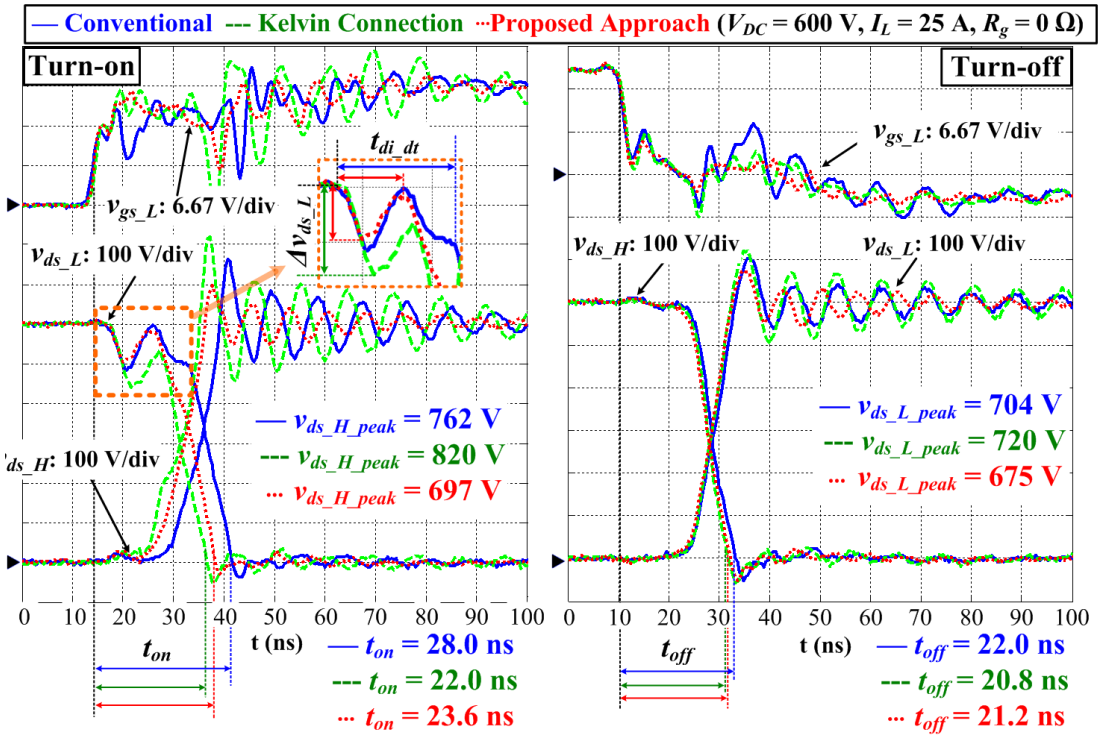
(a) Gate driver versus power device. (b) Power stage versus gate drivers.

Fig. 6-9. Phase-leg configuration built with the proposed placement.

Another interesting phenomenon observed in Fig. 6-10(a) is that the turn-on time of Kelvin connection based placement is shorter than that when the proposed approach is adopted. The reason is because the snubber effect induced by power loop inductance during the fast *di/dt* transient makes a voltage dip (i.e., $L_p\, di/dt$) across the drain-source terminals of the power device. Larger power loop inductance causes deeper voltage dip (see Δv_{ds_L} in Fig. 6-10(a)), which

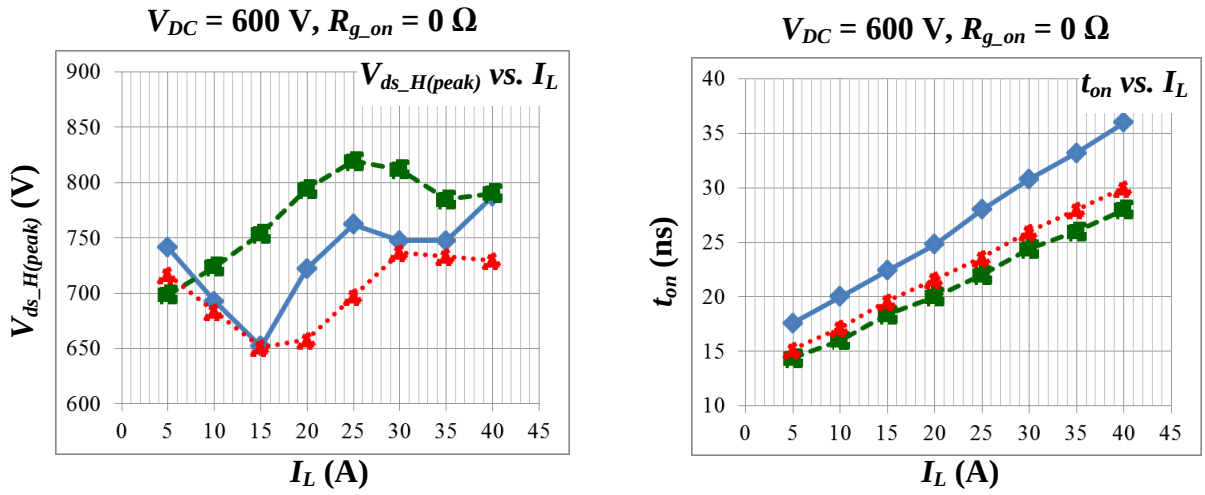
means that it would be faster to let the drain-source voltage drop to zero during the following *dv/dt* transient. In the end, the turn-on time by using the Kelvin connection based placement becomes shorter.

Similar switching behaviors can be observed during the turn-off transient in Fig. 6-10: the turn-off time with respect to the proposed placement is shorter than that by using the conventional approach; also among three placements, the proposed approach enables the lowest over-voltage with the least parasitic ringing.



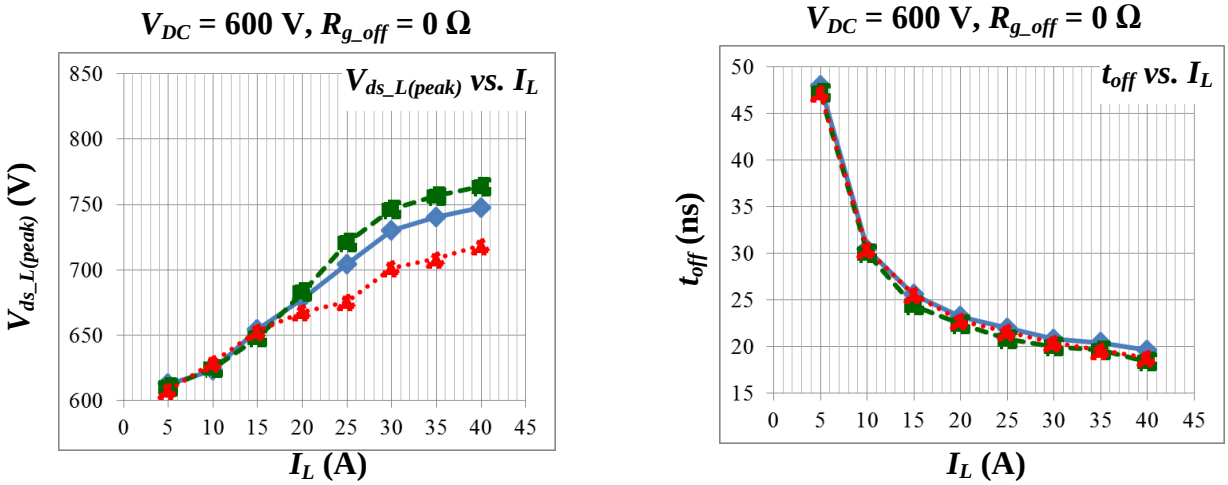
(a) Turn-on transient. (b) Turn-off transient.

Fig. 6-10. Switching waveform comparison under 600-V/25-A with 0-Ω gate resistance: conventional and Kelvin connection based placements versus proposed placement.



(a) $V_{ds\_H(peak)}$ depedence on I_L. (b) t_{on} depedence on I_L.

Fig. 6-11. Comparison of voltage spike and switching time dependence on load current during the turn-on transient.



(a) $V_{ds\_L(peak)}$ depedence on I_L. (b) t_{off} depedence on I_L.

Fig. 6-12. Comparison of voltage spike and switching time dependence on load current during the turn-off transient.

Table 6-3. Summary of Highest Over-Voltage Under the Worst Operating Condition

Over-voltage	Conventional	Kelvin Connection	Proposed Approach
Turn-on	764 V @ 600-V/ 5-A	821 V @ 600-V/ 25-A	731 V @ 600-V/ 5-A
Turn-off	743 V @ 40 A	768 V @ 600-V/ 40-A	718 V @ 600-V/ 40-A

More data in terms of voltage spike and switching time under different load currents during both turn-on and turn-off transients are shown in Fig. 6-11 and Fig. 6-12. Additionally, Table 6-3 summarizes the highest over-voltages under the worst operating condition for three placements. It shows that the proposed approach offers the best tradeoff between the switching speed and the voltage stress among a wide operating range.

In addition, according to the parasitic ringing frequency f_{ring} obtained from the switching waveforms in Fig. 6-10, the power loop inductance L_p can be experimentally quantified by the following equation

$$f_{ring} = \frac{1}{2\pi\sqrt{L_p C_{oss,eq}}} \tag{6-2}$$

where $C_{oss,eq}$ refers to the equivalent capacitance across the device's drain-source terminals, primarily consisting of the output capacitance of the tested device, PCB trace induced equivalent capacitance and the equivalent parallel capacitance (EPC) of the inductive load. Thanks to the optimal design of PCB layout and load inductor, $C_{oss,eq}$ in this case study is dominated by the output capacitance of the tested device, which can be found in the datasheet. Table 6-4 lists the power loop inductances for different placements calculated by (6-2) according to the tested switching waveforms. The data are almost identical to the corresponding simulation results based

on Q3D Extractor. Therefore, the proposed placement is capable of reducing the power loop inductance by 30% as compared to the conventional design in this study.

Table 6-4. Power Loop Inductance Comparison between Simulation and Test

Placement Style	Switching test result	Q3D Extractor
Conventional	24.2 nH	23.9 nH
Kelvin connection	25.4 nH	23.8 nH
Proposed approach	17.4 nH	17.0 nH

6.1.2 Design Consideration of Power Stage Layout

In addition to the parasitic inductance induced by the lead of device, PCB layout design is also critical. Since the impact of parasitic inductance in the power loop on the switching performance is more severe than that in the gate loop, in this section, the PCB layout design focuses on the power stage board. As discussed in section 4.1.1, the phase-leg configuration with switch-diode pair is preferred in an actual voltage source converter. Hence, the following discussion is based on this configuration.

There are two basic rules to follow when designing the power stage board for the parasitic minimization: one is P-cell and N-cell concept, the other is magnetic field cancellation. By leveraging these two PCB layout design principles together with the placement proposed above, the interconnection design for the phase-leg configuration consisting of discrete SiC MOSFETs and Schottky diodes is developed, as shown in Fig. 6-13. Fig. 6-14 and Fig. 6-15 illustrate how

the P-cell and N-cell concept and magnetic field cancellation are practically implemented in the PCB layout design.

First, as can be observed in Fig. 6-14, the main power device and its complementary freewheeling diode are placed next to each other (i.e., P-cell and N-cell concept), so that the physical distance of PCB trace in the actual switching commutation loop is naturally minimized.

Second, as displayed in Fig. 6-15, the PCB layout design utilizes the first inner layer as a power loop return path (Fig. 6-15(b)). This return path is located directly underneath the top layer's power loop (Fig. 6-15(a)), allowing for the smallest physical loop size combined with field self-cancellation. The lateral view ((see Fig. 6-15(c)) illustrates the switching current flowing path of creating a low profile self-cancelling loop for the power loop inductance minimization.

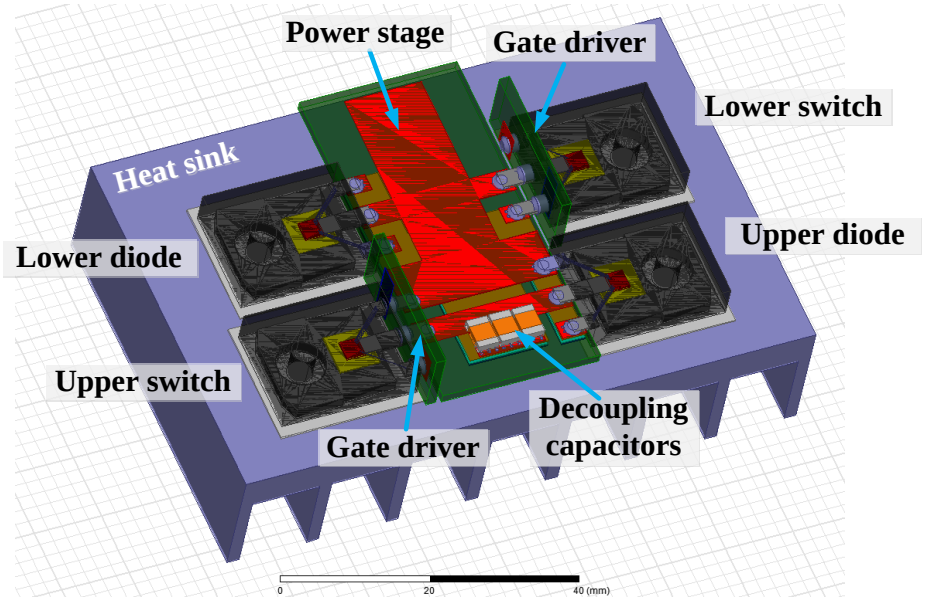


Fig. 6-13. Proposed placement and layout design in switch-diode pair based phase-leg configuration.

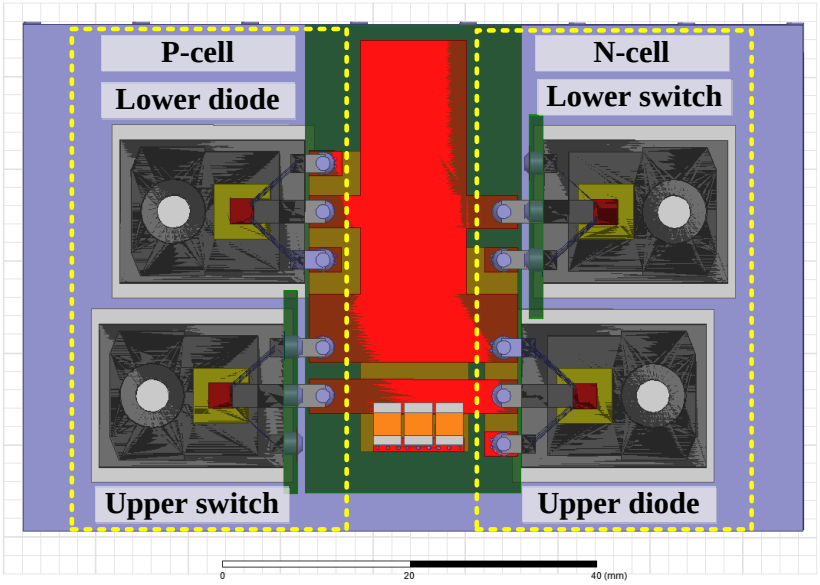
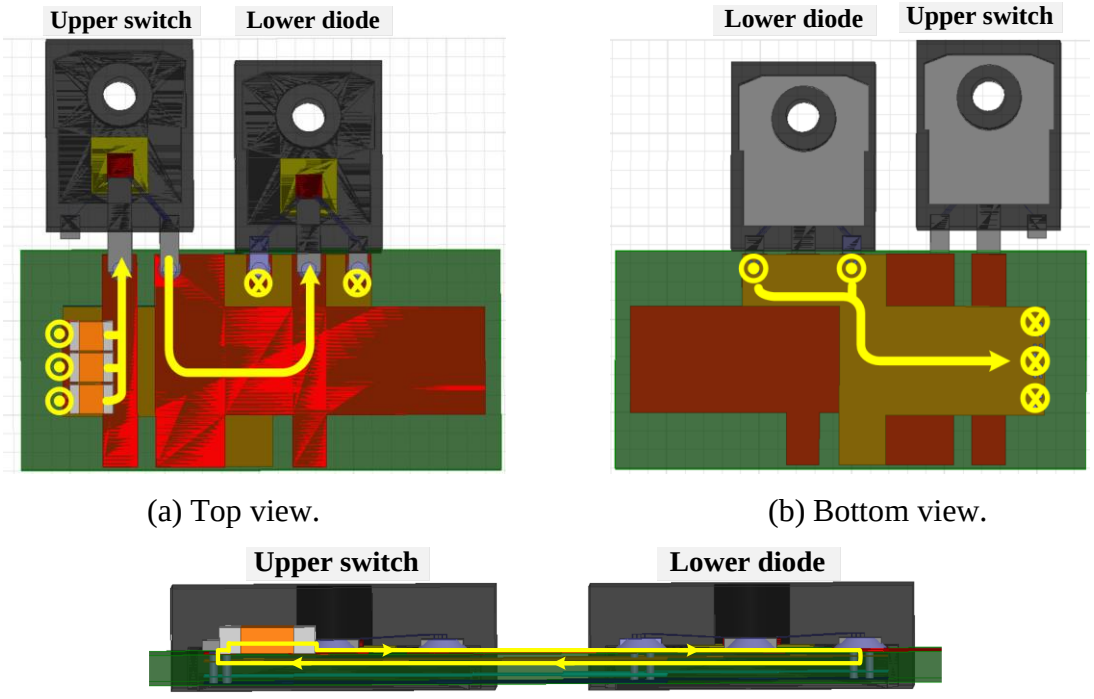


Fig. 6-14. Power stage PCB layout design based on P-cell and N-cell concept.



(a) Top view.

(b) Bottom view.

(c) Lateral view.

Fig. 6-15. Power stage PCB layout design based on magnetic field cancellation (taking P-cell as an example).

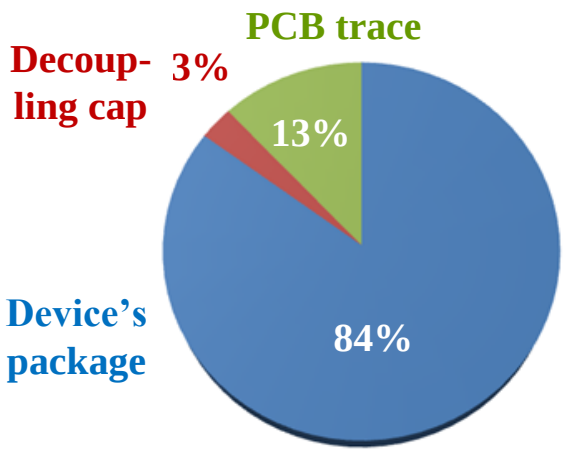


Fig. 6-16. Power loop inductance breakdown.

In total, based on Q3D Extractor, the power loop inductance induced by PCB is 2.2 nH. As compared to 14.8 nH power loop inductance due to the device's package, the power stage PCB layout design is acceptable. Fig. 6-16 illustrates the power loop inductance breakdown. It is observed that instead of the placement and layout design, the TO-247 package itself becomes the hurdle to further reduce the power loop inductance. In other words, the proposed placement and layout design are good enough for the switching loop parasitic minimization.

To enable the similar switching behavior between the double pulse tester and the actual voltage source converter, based on design criteria discussed in section 3.1.2, the same placement and layout design proposed above for the voltage source converter are leveraged in the design of the double pulse tester, as shown in Fig. 6-17. However, the power loop inductance of the double pulse tester would inevitably increase due to the insertion of the current sensor for the switching current measurement (coaxial shunt is used in this study). By adopting the idea of magnetic field cancellation in the PCB layout design, only 0.7 nH power loop inductance increase is observed according to the simulation by Q3D Extractor, which is negligible as compared to the total power

loop inductance. Therefore, the switching performance difference due to the different layout design between double pulse tester and actual voltage source converter becomes slight. The experimental verification will be given in chapter 7.

Note that the aforementioned design and effectiveness verification are carried out with TO-247 SiC MOSFETs, but the proposed placement and layout design can be directly leveraged to other power devices with TO-series package. Furthermore, the basic idea and concept discussed above are applicable to the interconnection design of the switching loop for power devices with different packages.

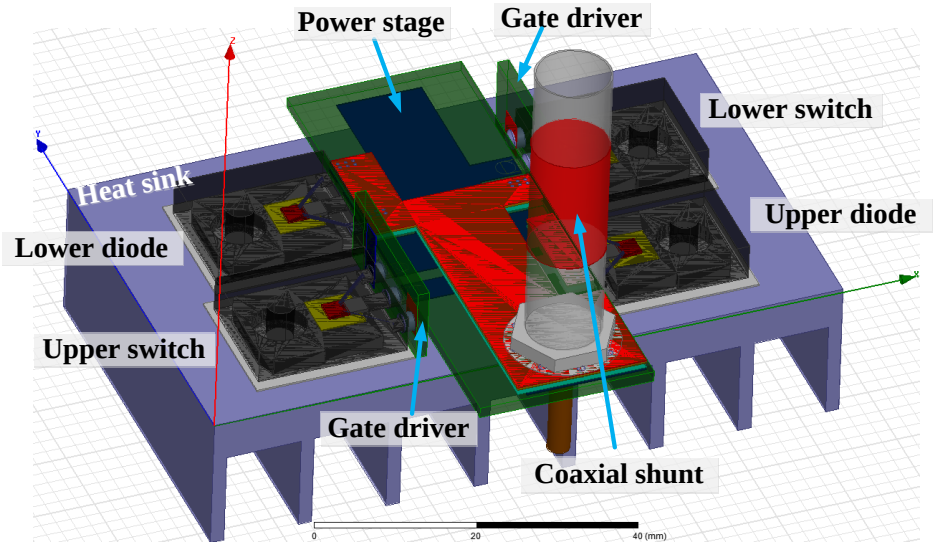


Fig. 6-17. Switching loop interconnection design of double pulse tester.

6.2 Decoupling of Interaction between Power Device and Inductive Load

The impact of inductive load on the switching performance mainly comes from the relatively low impedance at the switching transient related frequency range. As discussed in section 4.2.1, the experimental results show that the inductive load consisting of the motor and power cable significantly worsen the switching speed and losses. Consequently, this section

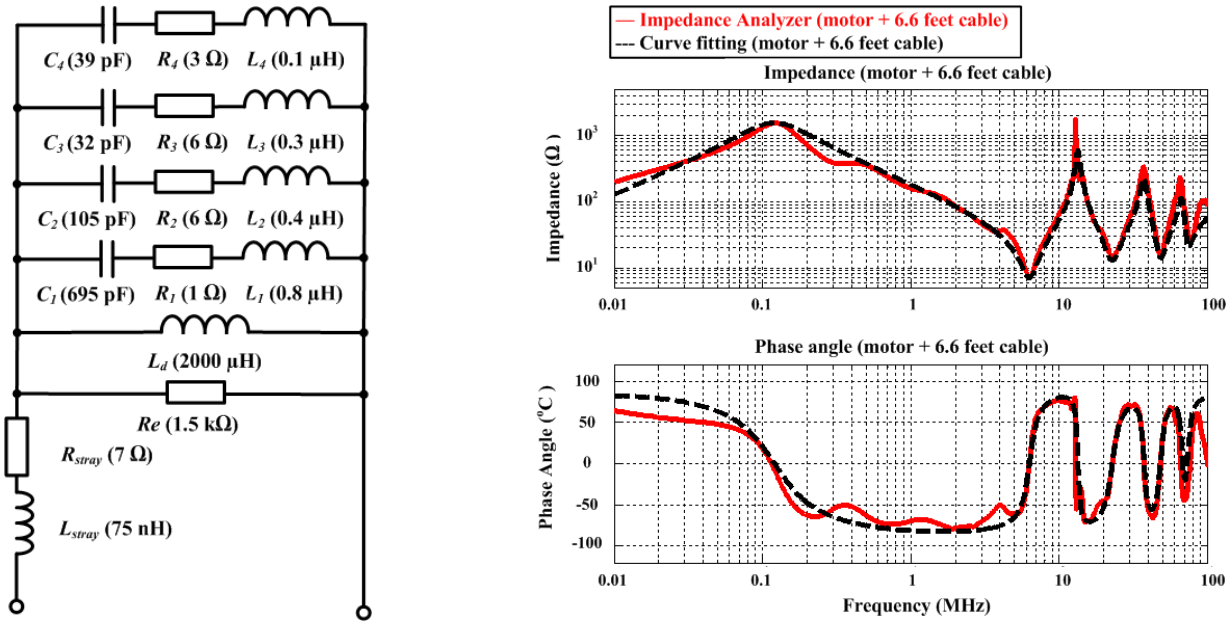
focuses on the motor plus power cable based inductive load, and aims at mitigating its negative influence during the switching transient. First, the high frequency inductive load modeling is presented, as the fundamental knowledge for the following solution development. Second, a basic idea of decoupling the interaction between the inductive load and power device in the voltage source converter during the switching transient is discussed. Based on this idea, an auxiliary filter is designed and inserted between the converter and inductive load so that the parasitics of the load will not be "seen" from the converter side during the switching transient. Finally, a double pulse tester with Cree 2nd generation 1200-V/20-A SiC MOSFETs is established to demonstrate the validity and effectiveness of this proposed approach.

6.2.1 High Frequency Modeling of Inductive Load

According to the high frequency impedance of the inductive load consisting of motor plus cable measured by impedance analyzer, a circuit model is derived, as shown in Fig. 6-18(a). Several *LRC* series resonant networks are employed in a paralleled structure to simulate the high frequency behavior of the inductive load under investigation. As can be observed in Fig. 6-18(b), the fitted curves of the inductive load impedance based on the circuit model can represent the critical characteristics of the motor plus cable impedances in frequency domain.

Based on the behavior model proposed above, a simulation circuit is built by Matlab/Simulink to verify the accuracy of this high frequency model in time domain. In Fig. 6-19(a), the voltage across the inductive load (i.e., drain-source voltage of the upper switch v_{ds_H}) measured by double pulse test is added at terminals of the inductive load's circuit model. And then the current flowing through the inductive load in the simulation is monitored and compared with the tested inductive current. The switching waveform comparison in Fig. 6-19(b) shows that the simulated inductive current I_L is almost identical to that based on test results during both

turn-on and turn-off trainsets. In total, the derived high frequency circuit model is accurate in both frequency and time domains and can be used for the following investigation.



(a) High frequency behavior model. (b) Impedance comparison.

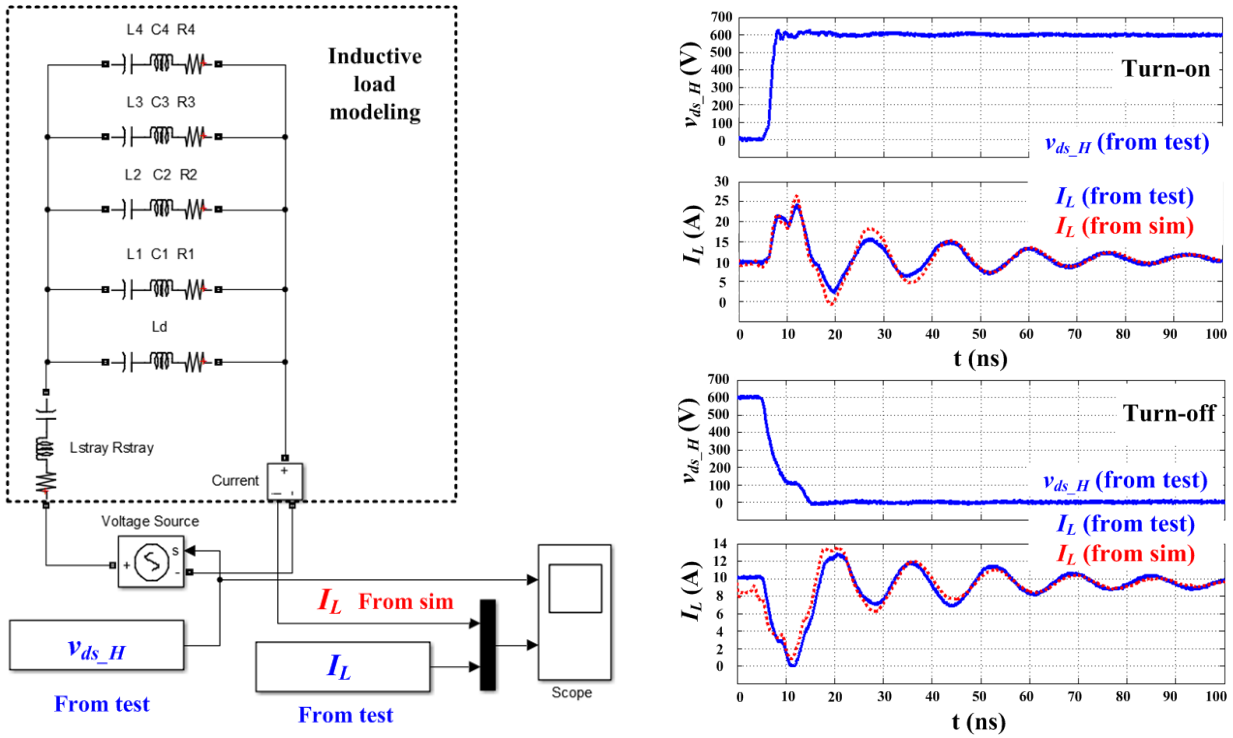
Fig. 6-18. High frequency impedance and circuit model of motor plus cable based inductive load.

6.2.2 Basic Idea for Mitigation of Adverse Effect from Inductive Load

According to the circuit model in Fig. 6-20(a), the large inductance L_d can be considered as a current source during the switching transient. It is the *LRC* series resonant networks that affect the switching behavior. Taking turn-on transient as an example, as can be observed in Fig. 6-20(b), during *dv/dt* transient, there will be resonant current excited per each *LRC* series resonant branch (i.e., I_1 to I_4). This additional current flows into the device and increases the channel current, resulting in the slower turn-on speed with larger switching losses. On the other hand, during the turn-off transient in Fig. 6-20(c), the resonant current induced by *LRC* series resonant

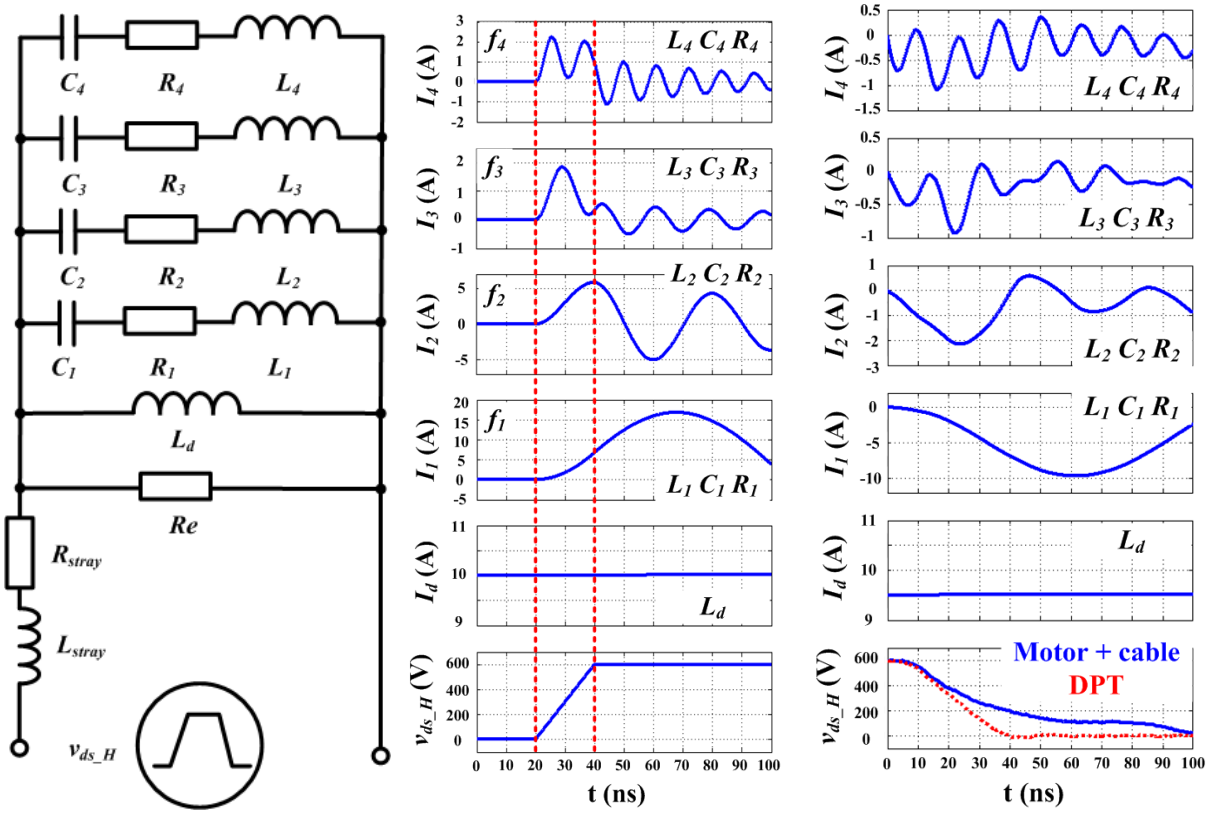
branch decreases the equivalent inductive current, leading to a longer turn-off time for charging/discharging of the device' output capacitance. Hence, the turn-off speed decreases as well.

To mitigate the impact of the inductive load's parasitics on the switching performance, resonant current suppression during the switching transient is critical. There are two basic ideas: 1) minimization of the resonant currents for the *LRC* branches with respect to the high resonant frequency (e.g., f_2 to f_4 in Fig. 6-21(a)), 2) regulation of the resonant period of the low resonant frequency based *LRC* branch (e.g., f_1 Fig. 6-21(a)) to be much longer than the switching commutation time so that there is almost no response for this series resonant network to the switching voltage excitation during the switching transient.



(a) Evaluation platform by Matlab/Simulink. (b) Test versus model based simulation.

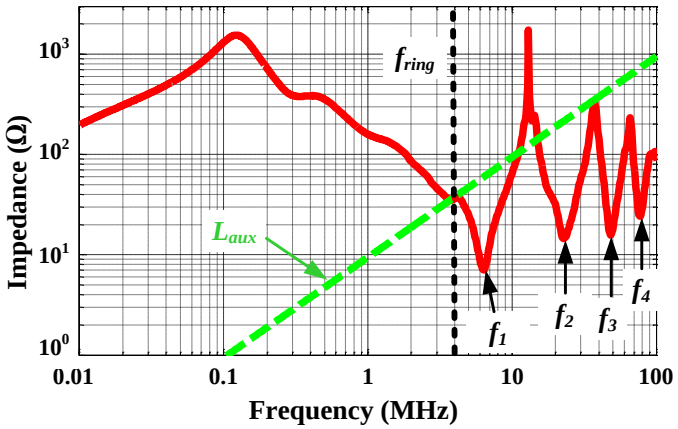
Fig. 6-19. Accuracy verification of the high frequency modeling.



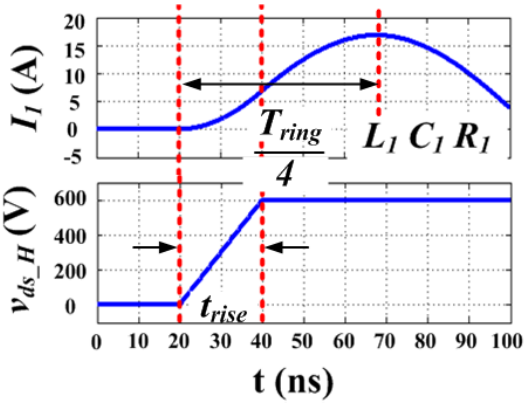
(a) Circuit model. (b) During turn-on transient. (c) During turn-off transient.

Fig. 6-20. Impact of parasitics of inductive load on the switching behavior.

To achieve these two ideas, an auxiliary inductor with small EPC is introduced in series with the existing inductive load to modify the high frequency impedance of the inductive load. As can be found in Fig. 6-21(a), first, this inductor has an excellent inductive characteristic at high frequency. Hence, the *LRC* branches with respect to the resonant frequency of f_2 to f_4 will disappear. Second, this inductor is capable of tuning the resonant frequency of the $L_1R_1C_1$ branch from f_1 to f_{ring}, enabling its corresponding resonant period T_{ring} to be much longer than the switching commutation time. And then the resonant current I_1 remains small during the switching transient (see Fig. 6-21(b)).



(a) High frequency impedance comparsion: inductive load versus auxilliary inductor.



(b) Resonant current I_l during the switching voltage commutation time.

Fig. 6-21. Basic idea for mitigation of the adverse effect from inductive load.

6.2.3 Design Criteria of the Auxiliary Filter

According to the basic idea discussed above, the inductance for the auxiliary inductor L_{aux} is determined by f_{ring}, which is directly related to the switching voltage commutation time. However, the switching voltage commutation time changes as the operating condition varies. Therefore, it is critical to select a switching voltage commutation time that enables the switching performance not to be affected by the inductive load under most of operating conditions. As can

be observed in Fig. 6-22, the switching voltage commutation time tested by the double pulse tester is greatly depends on the operating current, and the longest switching voltage commutation time occurs during the turn-off transient under the light inductive load. If f_{ring} is determined based on the turn-off switching voltage commutation time at the extremely light load, the required L_{aux} will be fairly large, but the benefit we can obtained is limited since the turn-off switching loss at the light load is always almost zero. Thus, it is wise to select a switching voltage commutation time which is longer than all of the turn-on commutation time and part of the turn-off commutation time so that except the turn-off time at the light load, the switching time under the rest of the operating conditions together with the switching losses under all of the operating points will not be affected by the parasitics of the inductive load. In the following case study, f_{ring} is determined by the switching voltage commutation time of 34 ns during turn-off transient under the operating condition of 600-V/10-A (see Fig. 6-22).

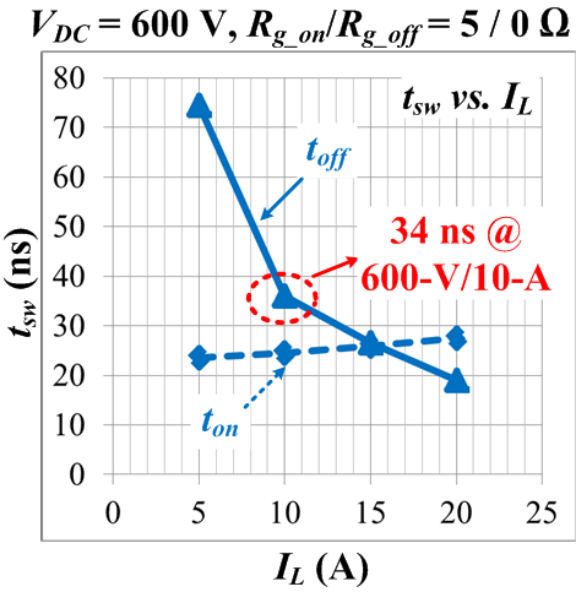


Fig. 6-22. Voltage commutation time dependence on load current measured by double pulse test.

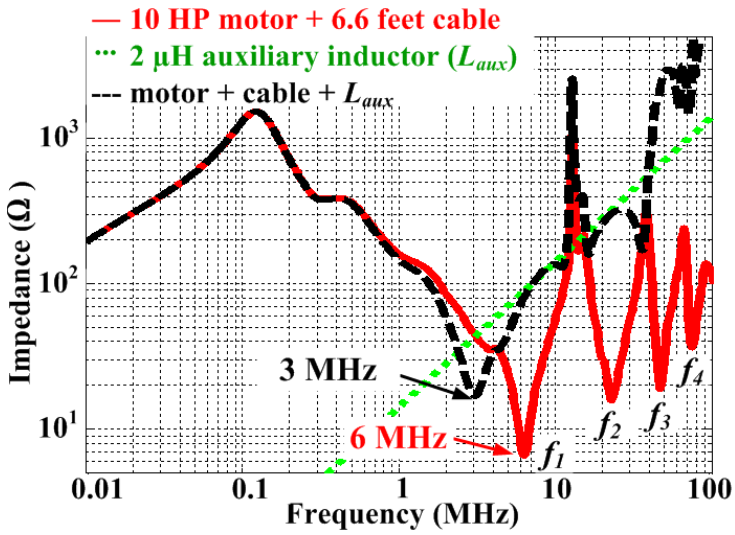


Fig. 6-23. High frequency impedance comparison: inductive load versus auxilliary inductor versus inductive load in series with the auxilliary inductor.

Based on the aforementioned design idea, f_{ring} should satisfy,

$$\frac{1}{f_{ring}} \gg t_{v,worst} \tag{6-3}$$

where $t_{v,worst}$ refers to the switching voltage commutation time at the selected worst operating conditions (e.g., 34 ns at 600-V/10-V in this case study). f_{ring} of 3 MHz is selected so that its corresponding resonant period T_{ring} is 10 time longer than $t_{v,worst}$. Combining with the high frequency impedance of the inductive load, a 2 µH auxiliary inductor is needed. Fig. 6-23 illustrates that after insertion of a 2 µH auxiliary inductor, high resonant frequencies, such as f_2, f_3 and f_4 existing in the original motor plus cable load is suppressed. Moreover, the resonant frequency of f_1 is shifted from 6 MHz to 3 MHz. In total, a 2 µH auxiliary inductor achieves all the design requirements described above. Considering the three-phase conversion system, the auxiliary inductor per phase is 1.4 µH.

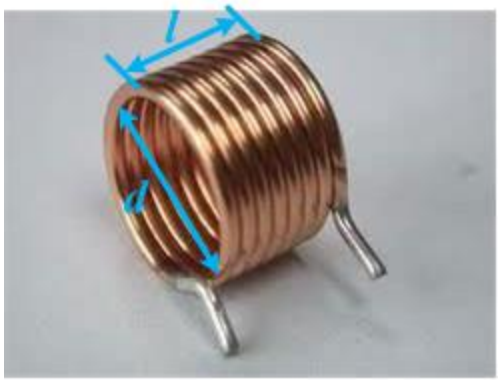
In addition to the inductance selection, physical design of the auxiliary inductor is important, because it affects the loss dissipated by this auxiliary inductor. The design objective is to minimize this extra loss so that combining with the switching loss reduction due to the proposed auxiliary inductor, the total power loss of the converter can decrease. In this case study, considering the relatively small inductance, an air core inductor is employed. The design methodology is described as follows.

First, AWG of the magnet wire is selected based on the maximum operating current. In this case study, based on 11 A RMS current per each phase in the three-phase voltage source inverter together with 4 A/mm^2 maximum current density for copper wires, 12 AWG magnet wire is selected.

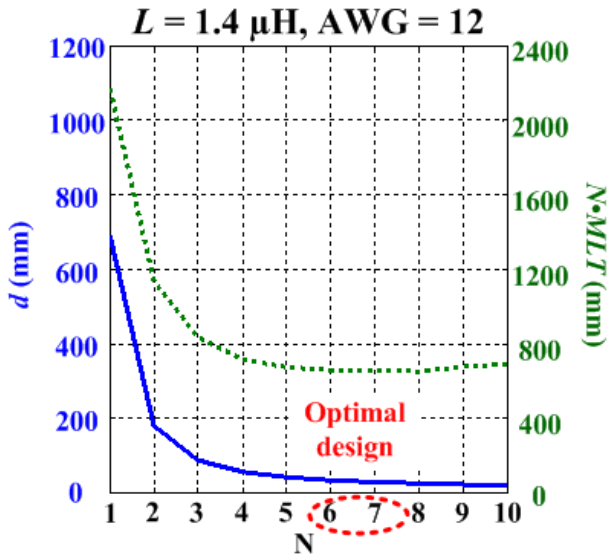
Second, diameter d and number of turns N of the air core inductor are designed to achieve the required inductance with the shortest length of the copper wire (i.e., smallest $N \times MLT$ (mean-length-per turn)) for the minimization of power loss dissipated by this auxiliary inductor. Fig. 6-24(a) shows a typical air core inductor, and its inductance is given by

$$L = (d^2 + N^2)/(18d + 40l) \tag{6-4}$$

where L is inductance in μH, d is the coil diameter in inches, N is number of turns, l is coil length in inches, which can be determined by N and diameter of the copper wire (i.e., AWG). According to (6-4), the relationship between N and d to achieve a 1.4 μH air core inductor is illustrated in Fig. 6-24(b). To minimize the length of the copper wire (i.e., $N \times MLT$), there will be the optimal design in terms of N and d. In this case study with 12 AWG copper wire, the smallest $N \times MLT$ is achieved when N of 6 or 7 is selected. In the end, based on the parameters listed in Table 6-5, three air core inductors are designed and fabricated, as shown in Fig. 6-24(c).



(a) Typical air core inductor.



(b) Design optimization of air core inductor: *d* dependence on *N* and corresponding N×*MLT*.

(c) Three air core inductors designed as auxiliary inductors.

Fig. 6-24. Design of auxiliary inductors.

Table 6-5. Parameters of the Designed Air Core Inductor.

Max. current density	RMS current per phase	AWG	*N*	*d*
4.0 A/mm^2	11 A	12	7	30 mm

6.2.4 Experimental Verification

Leveraging the same double pulse test setup with the proposed gate driver circuit from chapter 5, as shown in Fig. 5-16 and 5-17, the comparison experiments are carried out under three different groups (see Table 6-6) to evaluate the effectiveness of the proposed auxiliary inductor on the switching performance improvement.

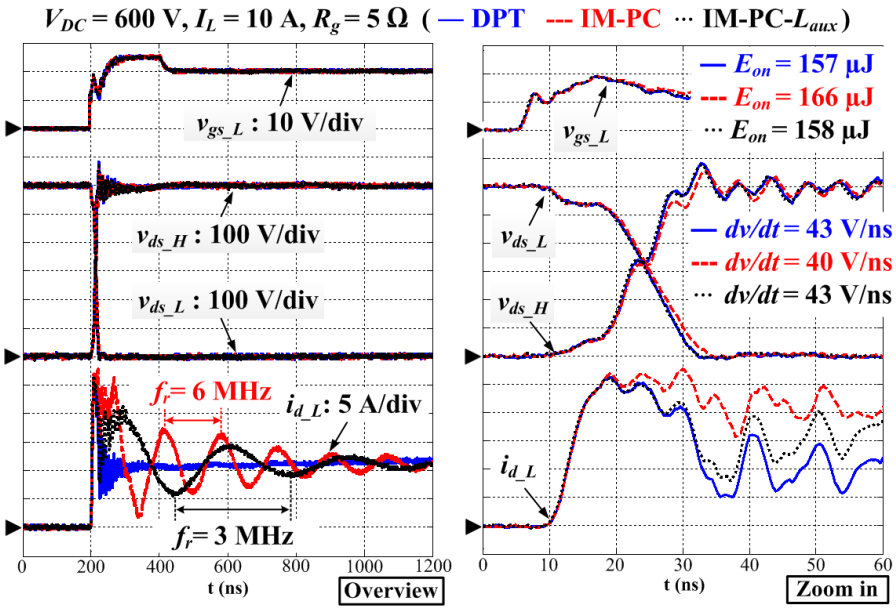
Table 6-6. Three Comparison Groups with Different Inductive Loads

1st Group	Double pulse test based inductor (DPT)
2nd Group	10 HP induction motor plus 6.6 feet power cable (IM-PC)
3rd Group	Induction motor plus power cable with auxiliary inductor (IM-PC-L_{aux})

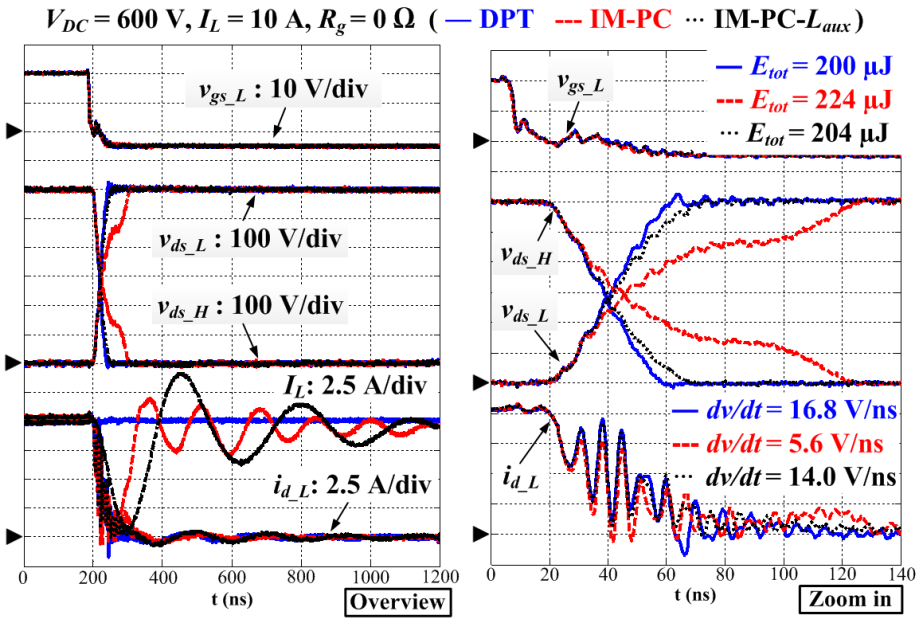
Fig. 6-25 shows the comparison switching waveforms with three different inductive loads under the operating condition of 600-V/10-A with 5-Ω gate resistance during the turn-on transient and 0-Ω gate resistance during the turn-off transient. As can be observed from the overall switching waveforms during both turn-on and turn-off transients, there is a 6.0 MHz frequency ringing in the switching current with the motor plus cable based inductive load (see dashed red waveforms in Fig. 6-25). After inserting 1.4 µH air core inductor per each phase, the ringing frequency is varied from 6.0 MHz to 3.0 MHz (see dotted black waveforms in Fig. 6-25), which agrees with the aforementioned design.

Also, as predicted, during the turn-on transient, auxiliary inductor let switching performance become better as compared to that with motor plus cable (IM-PC) based inductive load: *dv/dt* increases from 40 V/ns to 43 V/ns, and the turn-on switching loss reduces from 166 µJ to 158 µJ.

Additionally, thanks to the auxiliary inductor, its corresponding switching behavior is almost identical to that by using the optimally-designed DPT based inductor load.



(a) Turn-on transient.



(b) Turn-off transient.

Fig. 6-25. Switching waveform comparisons among different inductive load.

Similarly, during the turn-off transient, auxiliary inductor allows *dv/dt* with motor plus cable based inductive load increases from 5.6 V/ns to 14.0 V/ns, which almost approaches to the *dv/dt* of 16.8 V/ns by using the DPT inductor. Furthermore, the total switching losses of motor plus cable inductive load with the auxiliary inductor decreases from 224 μJ to 204 μJ, which is nearly the same as 200 μJ, the total switching losses achieved by DPT inductor.

In summary, during the switching transient, the proposed auxiliary inductor successfully decouples the interaction between the inductive load and power device, enabling the switching performance with the practical inductive load (e.g., motor plus cable based inductive load in this case study) to mostly achieve the excellent behavior when the optimally-designed DPT inductor is employed.

Additionally, based on the design consideration of the auxiliary inductor, to minimize the required inductance, there will be penalty for the turn-off time at the light load (e.g., < 10 A in this case study). As can be observed in Fig. 6-26, under the operating current of 5-A, the turn-off time with the motor plus cable based inductive load becomes even longer when the auxiliary inductor is applied. This is because that the relatively long turn-off time at the light operating current cannot avoid the impact of the resonant current induced by the parasitics of the inductive load. Also, the proposed auxiliary inductor let the resonant frequency decrease from 6.0 MHz to 3.0 MHz, which means that the duration of the resonant current with lower resonant frequency becomes longer, and then the turn-off time by using the auxiliary inductor turns to be longer as well. However, the tested turn-off switching loss at the light load current stays nearly constant, and theoretically equals to the energy stored in the junction capacitance of the power device and its antiparallel diode. Fig. 6-26 illustrates that although the turn-off time difference with different inductive loads are significant; their turn-off switching losses are almost identical.

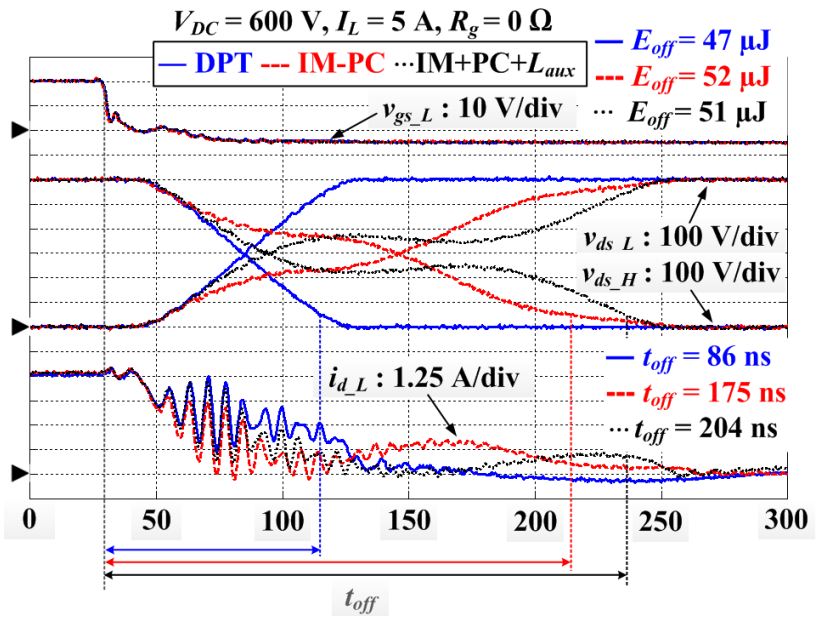
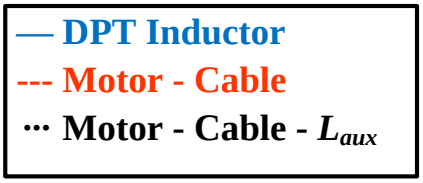


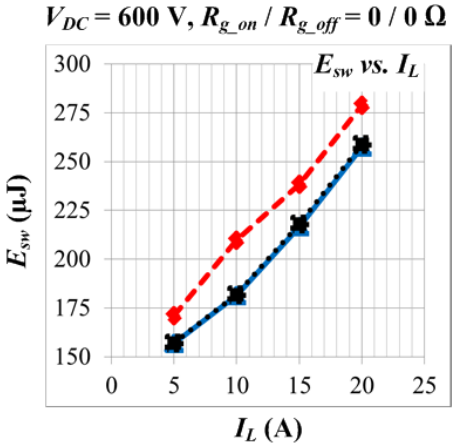
Fig. 6-26. Comparison of turn-on switching performance among different inductive load.

Fig. 6-27 gives more switching data comparison among different inductive loads under different operating currents. Fig. 6-27(b) shows that, thanks to the auxiliary inductor, the total switching loss with motor plus cable becomes lower, and is almost identical to the switching losses tested by using DPT inductor. Similar behavior can be found in terms of turn-on switching time in Fig. 6-27(c). In Fig. 6-27(d), except the light load (i.e., < 10 A in this case study), the turn-off time with motor plus cable based inductive load after the insertion of the auxiliary inductor decreases, and becomes identical to that when the DPT inductor is employed.

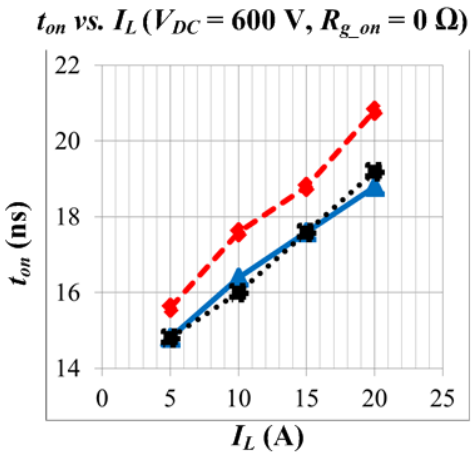
Fig. 6-28 illustrates the comparison test results dependence on the junction temperature. As predicted, the experimental data demonstrate the effectiveness of the proposed auxiliary inductor on the switching performance improvement.



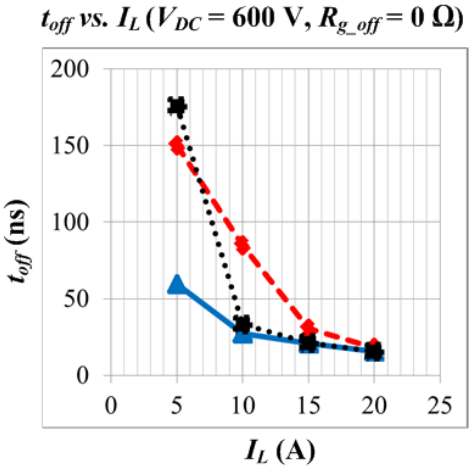
(a) Labels of comparison groups.



(b) E_{sw} dependence on I_L.

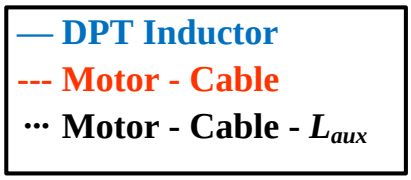


(c) t_{on} dependence on I_L.

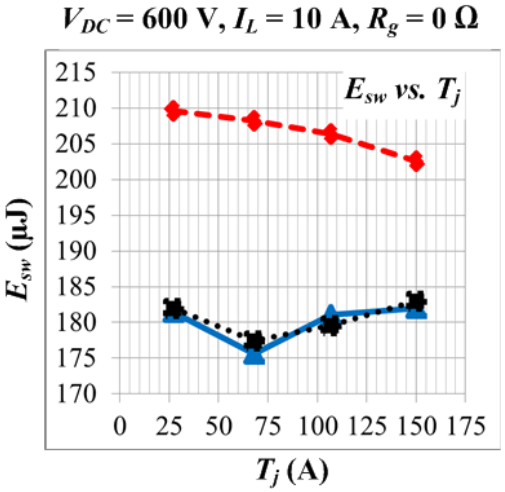


(d) t_{off} dependence on I_L.

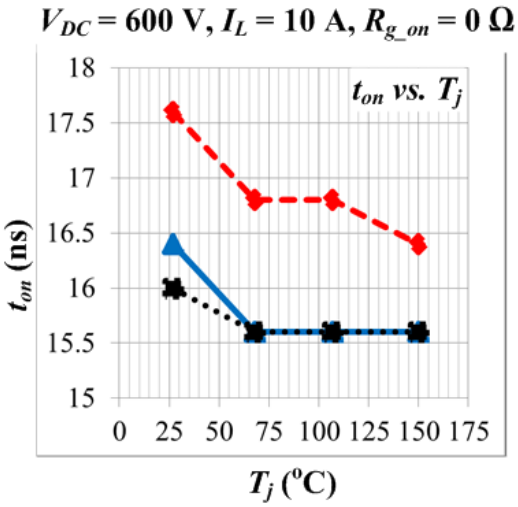
Fig. 6-27. Comparison test results dependence on load inductor with 600-V dc bus voltage and 0-Ω gate resistance.



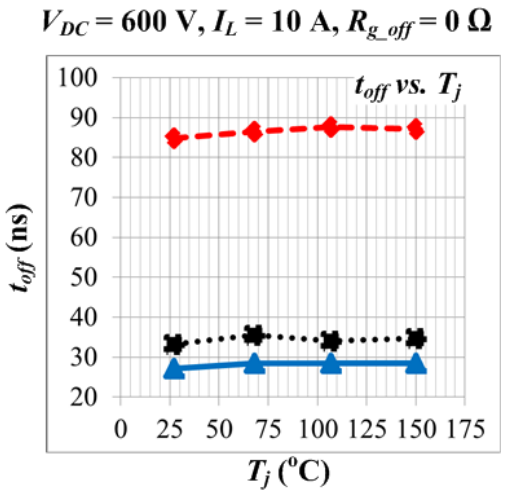
(a) Labels of comparison groups.



(b) E_{sw} dependence on T_j.



(c) t_{on} dependence on T_j.



(c) t_{off} dependence on T_j.

Fig. 6-28. Comparison test results dependence on junction temperatures under 600-V/ 10-A with 0-Ω gate resistance.

In total, the proposed auxiliary inductor is capable of mitigating the interaction between the inductive load and power device among a wide operating range: except the turn-off time at the light load, the switching time under the rest of the operating conditions together with the switching losses under all of the operating points will not be affected by the parasitics of the inductive load.

In addition to suppress the adverse impact of inductive load on the switching behavior, the auxiliary inductor is able to mitigate the *dv/dt* and over-voltage across the motor terminals. Fig. 6-29 illustrates that under the operating condition of 600-V/10-A, the auxiliary inductor let the motor terminal over-voltage decrease from 1049 V to 1018 V together with the *dv/dt* reduction up to 44%. The reason causing the mitigation of over-voltage and its *dv/dt* is because the ringing frequency of the voltage across motor terminals becomes lower when the auxiliary inductor is employed (see Fig. 6-29). More test data under different operating currents are shown in Fig. 6-30. In the end, the proposed auxiliary inductor is beneficial to the insulation of induction motor.

To make a fair judgement of the benefits gained from the auxiliary inductor, the additional power loss dissipated by this auxiliary inductor should be taken into account. As shown in Fig. 6-31, considering the skin effect, the extra power loss induced by L_{aux} is lower than the switching loss reduction when the switching frequency is above 50 kHz. Therefore, for the high switching frequency applications, the proposed approach is able to improve the overall efficiency of the power conversion system.

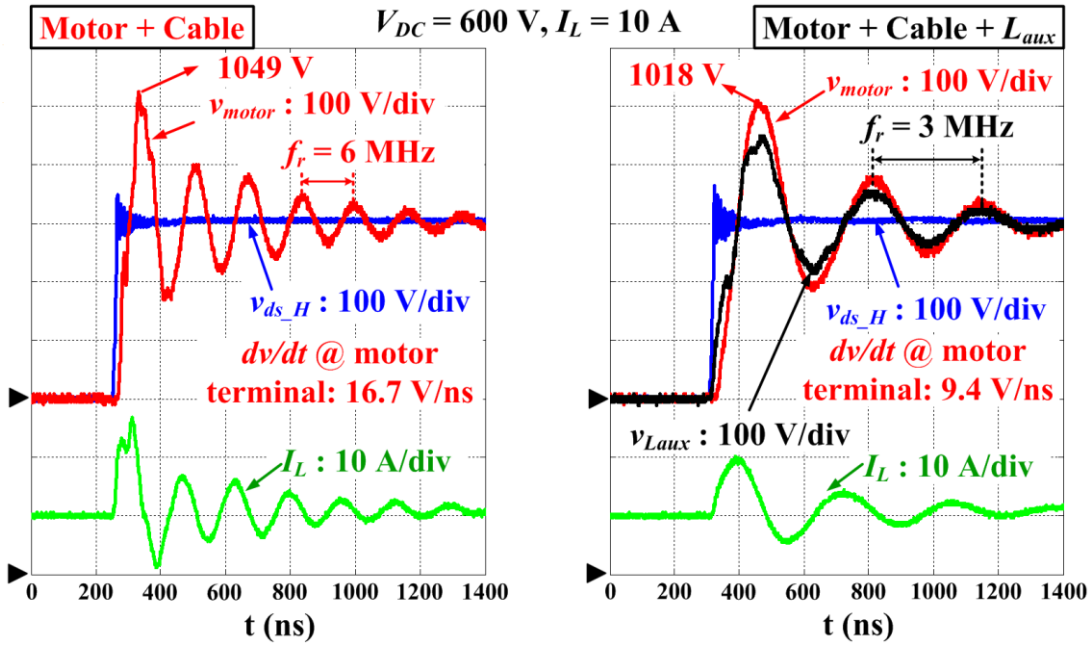


Fig. 6-29. Impact of auxiliary inductor on motor terminal voltage: v_{ds_H} is drain-source voltage of the upper switch; v_{motor} is motor terminal voltage; v_{Laux} is converter terminal voltage (after L_{aux}).

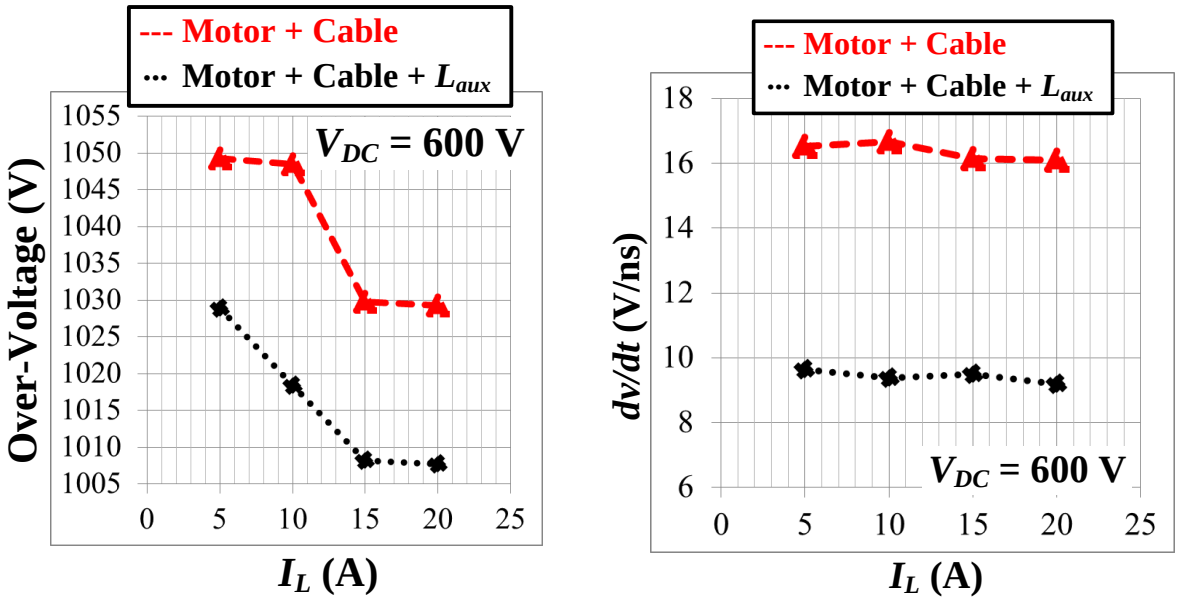


Fig. 6-30. Motor terminal over-voltage and its *dv/dt* comparison dependence on load currents.

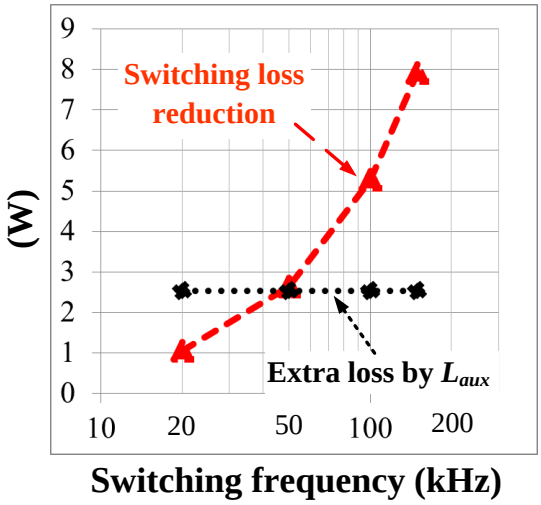


Fig. 6-31. Power loss comparison: switching loss reduction versus extra loss by L_{aux}.

6.3 Conclusion

Optimization of the interconnection design is explored for SiC switching performance improvement in the voltage source converter.

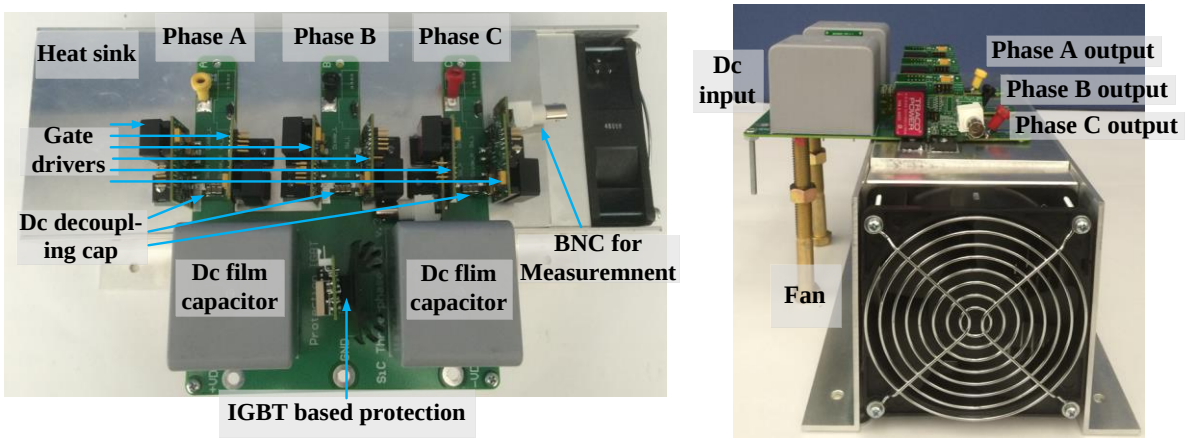
First, the placement of gate drivers, devices and power stage are investigated to minimize the effective length of power devices' leads in the switching loop. The proposed placement enables the common source inductance to decrease by up to 29.4% as compared to that when the conventional placement is employed, together with the power loop inductance reduction up to 28.6%. The test results based on Cree 2nd generation 1200-V/36-A SiC MOSFETs show that the proposed placement offers the best tradeoff between the switching speed and the voltage stress among a wide operating range. Furthermore, PCB layout design of the power stage board is optimized on the basis of P-cell and N-cell concept and magnetic field cancellation. In total, parasitic inductance associated in the power loop is minimized to be 17 nH, which is smaller than 30 nH, the package induced parasitic inductance of the state-of-art SiC power module built with the similar bare dies in this study [135]. Additionally, according to the inductance

breakdown, 84% of the total power loop inductance is induced by TO-247 package, which means that package itself becomes the hurdle to further reduce the power loop inductance. In other words, the proposed placement and layout design are good enough for the switching loop parasitic minimization.

Second, a dedicated auxiliary inductor is designed and inserted between the converter and inductive load so that the parasitics of the load will not be "seen" from the converter side during the switching transient. The test results with Cree 2nd generation 1200-V/20-A SiC MOSFETs verify that the proposed auxiliary inductor is capable of mitigating the interaction between the inductive load and power device under different operating conditions: except the turn-off time at the light load, the switching time under the rest of the operating conditions together with the switching losses under all of the operating points will not be affected by the parasitics of the inductive load. Also, it is noted that the extra loss dissipated by the auxiliary inductor is lower than the switching loss reduction for the high switching frequency applications (> 50 kHz in this case study), leading to an overall efficiency improvement in the power conversion system.

7 Experimental Demonstration of High Switching-Speed Performance of SiC Devices in Voltage Source Converter

This chapter aims at evaluating the high switching-speed performance of SiC devices in the voltage source converter after comprehensively utilizing all the developed knowledge and techniques from chapter 3 to chapter 6. The ultimate objective is to verify that when the voltage source converter is operating, the tested switching performance of SiC devices can repeat the excellent switching behavior obtained by using the optimally-designed double pulse test. A three-phase voltage source inverter fed motor drives is selected as the representative of the voltage source converter under assessment.



(a) Top view. (b) Lateral view.

Fig. 7-1. SiC based three-phase voltage source converter.

First, a three-phase voltage source inverter with Cree 2nd generation 1200-V/20-A SiC MOSFETs is built based on the intelligent gate driver proposed in chapter 5 and optimal interconnection design developed in chapter 6, as shown in Fig. 7-1.

Second, based on this three-phase voltage source inverter, a set of experiments has been devised to make a comprehensive comparison of switching performance. The methodology for experimental verification is described as follows.

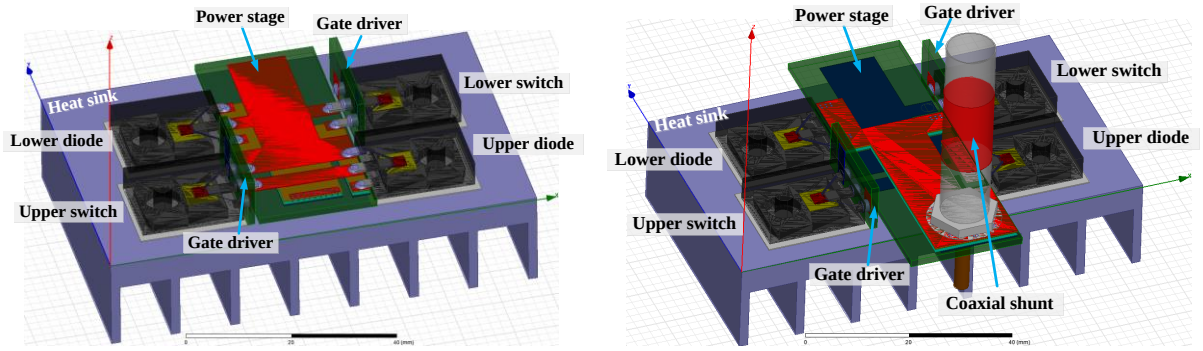
1) Evaluation of switching performance difference between the double pulse test (DPT) board and three-phase voltage source converter (VSC). Since in previous chapters, all the experimental verification for each technique, such as intelligent gate driver, optimal interconnection design, is conducted based on the DPT board, it is important to demonstrate that power devices in three-phase VSC have the similar switching behavior to that by using DPT board.

2) Evaluation of the interaction of phase-legs and impact of heat sink on the switching performance. DPT circuit merely depends on a phase-leg configuration, but in an actual three-phase VSC, there will be two more phase-legs as well as a heat sink. Based on the investigation and experimental verification in section 4.2, it shows that the influence of the other two phase-legs and heat sink on the switching performance is slight, but previous conclusion is drawn based on Cree 1st generation SiC MOSFETs without intelligent gate driver and optimal interconnection design. Therefore, it is worthwhile to re-evaluate the influence of phase-legs and heat sink on the switching behavior according to the latest version of three-phase VSC.

3) Evaluation of ultimate switching performance of SiC devices in the three-phase VSC when the motor is rotating. This switching behavior will be monitored and directly compared with the switching performance tested by the optimally-designed DPT with intelligent gate driver and optimal interconnection design. Once they have the similar switching characterization, we can conclude that the high switching-speed performance of SiC devices can be realized in the actual VSC.

7.1 Switching Performance Comparison between DPT Board and Three-phase VSC

Fig. 7-2 shows the comparison of switching loop interconnection design between one phase-leg of three-phase VSC and DPT board. Even if the same placement and PCB layout design together with the gate driver board are applied for both the DPT board and VSC, the power loop inductance of the DPT board would be inevitably larger due to the insertion of the coaxial shunt for the switching current measurement. Therefore, switching performance tested in DPT board and three-phase SVC will always be different. However, as discussed in section 6.1.2, thanks to the optimal PCB layout design of the DPT board, the extra power loop inductance induced by coaxial shunt is fairly small, enabling the switching behavior difference in three-phase VSC and DPT board to be slight.



(a) Phase-leg cell of three-phase VSC. (b) Phase-leg configuration of DPT.

Fig. 7-2. Switching loop interconnection design comparison: one phase-leg of three-phase VSC versus DPT board.

Fig. 7-3 illustrates the switching waveform comparison between DPT board and three-phase VSC when the DPT based load inductor is employed under the operating condition of 600-V/10-A with 0-Ω gate resistance. Although, the switching current cannot be monitored in the three-

phase VSC, the comparison of gate voltage and drain-source voltages indicates that the switching performance in the three-phase VSC is almost identical to that tested by the DPT board. Also, based on different voltage dips due to the snubber effect of power loop inductance during turn-on *di/dt* transient together with voltage spikes, we can identify that the power loop inductance in the three-phase VSC is smaller than that in the DPT board.

Considering the practical inductive load consisting of a 10 HP induction motor plus 6.6 feet power cable with 2 μH auxiliary inductor (MCL), the switching waveform comparison between DPT board and three-phase VSC are displayed in Fig. 7-4. Similar to the observation in Fig. 7-3, the difference of the switching waveform between DPT board and three-phase VSC is slight.

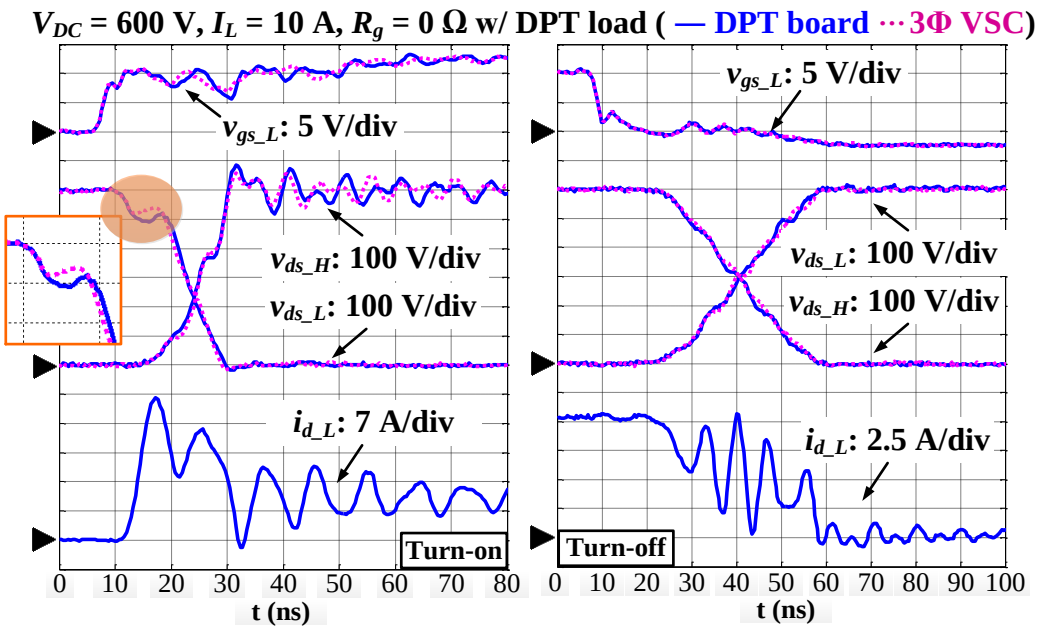


Fig. 7-3. Switching waveform comparison with DPT load inductor between DPT board and three-phase VSC.

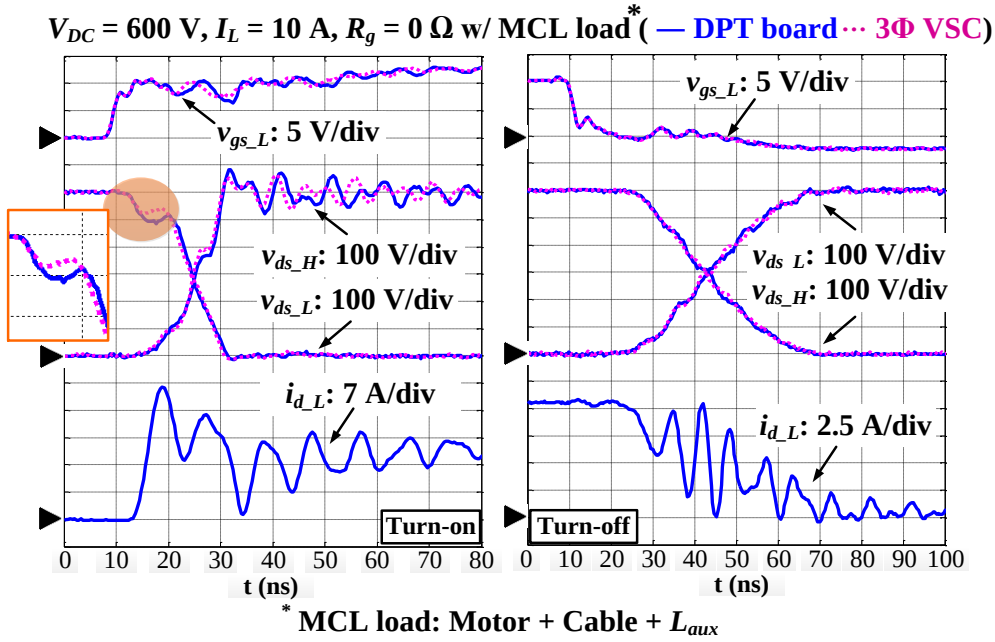


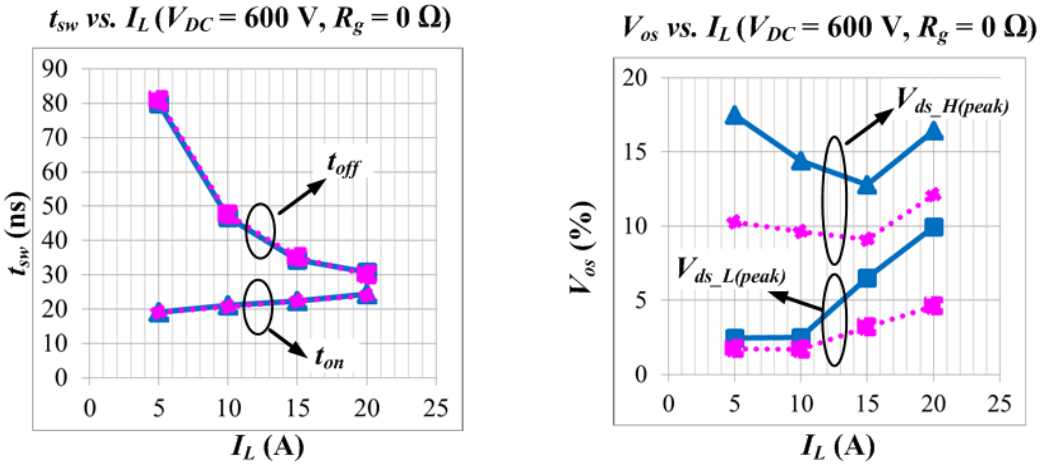
Fig. 7-4. Switching waveform comparison with MCL load inductor between DPT board and three-phase VSC.

More comparison test results dependence on load currents for both the DPT load and MCL load are shown in Fig. 7-5 and Fig. 7-6. It demonstrates that the switching time during both turn-on and turn-off transients with different test boards are almost the same. Even better, due to the smaller power loop parasitic inductance for the three-phase VSC, its corresponding over-voltages are always lower than that tested by the DPT board. The definition of $V_{os}(\%)$ in Fig. 7-5(c) and Fig. 7-6(c) is given by

$$V_{os}(\%) = \frac{(V_{os} - V_{DC})}{V_{DC}} \times 100\% \tag{7-1}$$

where V_{os} is the peak value of the drain-source voltage; V_{DC} refers to the dc bus voltage.

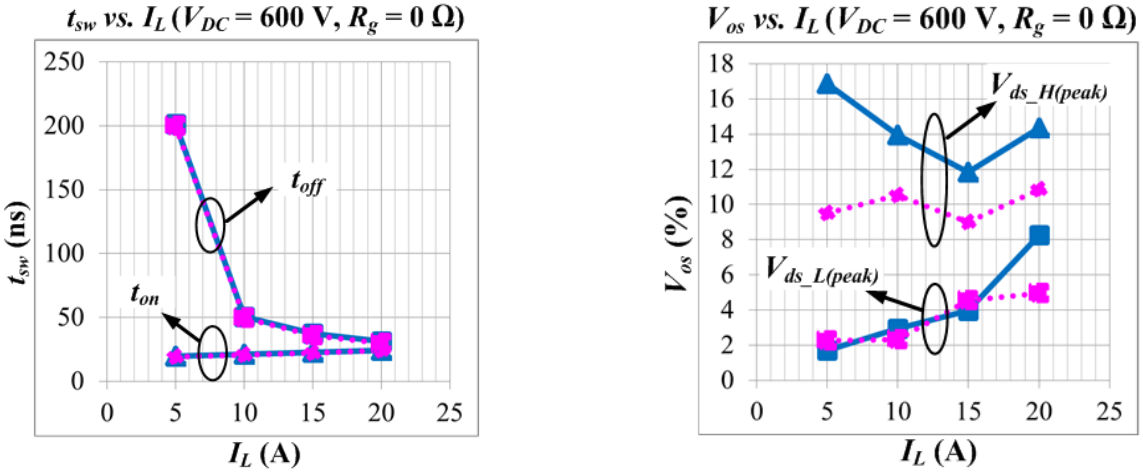
(a) Labels of comparison groups.



(b) Switching time dependence on load currents. (c) Voltage spike dependence on load currents.

Fig. 7-5. Comparison test results dependence on load currents with DPT load inductor.

(a) Labels of comparison groups.



(b) Switching time dependence on load currents. (c) Voltage spike dependence on load currents.

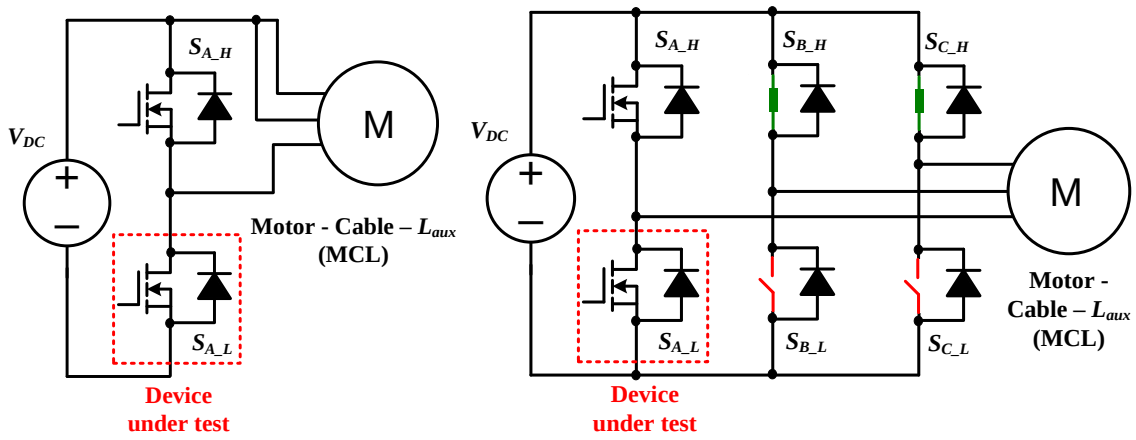
Fig. 7-6. Comparison test results dependence on load currents with MCL load.

In total, the excellent switching waveforms based on DPT board can be achieved in the phase-leg of three-phase VSC. Accordingly, the switching waveform improvement verified by DPT board in previous chapters is still valid in the three-phase VSC.

7.2 Interaction of Phase-legs and Impact of Heat Sink on the Switching Performance

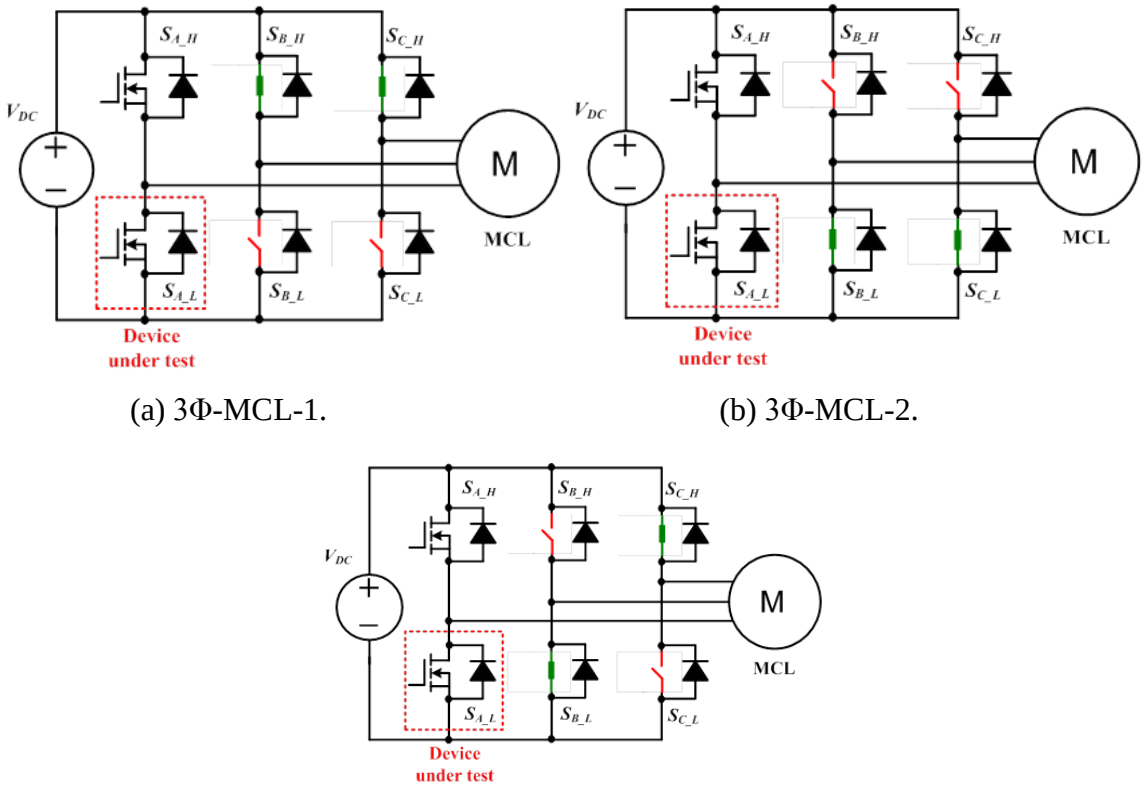
The DPT circuit merely depends on a phase-leg configuration, but in actual three-phase VSC, there will be two more phase-legs as well as a heat sink. The impact of phase-legs and heat sink on the switching performance is experimentally investigated based on the latest version of three-phase VSC.

According to test circuits for evaluation of the impact of two more phase-legs on the switching behavior, as shown in Fig. 7-7 and Fig. 7-8, the switching waveforms in Fig. 7-9 and Fig. 7-10 illustrate that neither the parasitics induced by phase B and C nor the different inductive load connection structures due to the switches' on-off states have significant effect on the switching performance since the gate voltage and drain-source voltage under different test configurations are almost identical. Similarly, based on test circuits in Fig. 7-11, the switching waveform comparison in Fig. 7-12 shows that the capacitive coupling effect induced by heat sink on the switching performance is insignificant. More comparison test results in Fig. 7-13 indicate that under different operating conditions, the influence of two more phase-legs and heat sink on the switching time of SiC devices in the three-phase VSC is negligible, which agrees with the conclusion drawn in section 4.2.



(a) PL-MCL. (b) 3Φ-MCL.

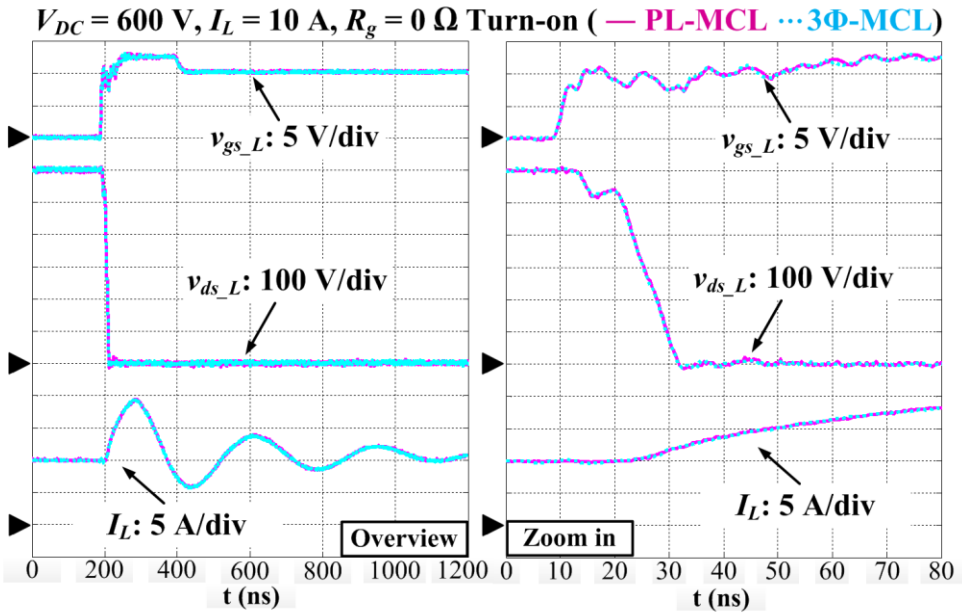
Fig. 7-7. Test circuits for evaluation of the impact of two more phase-legs' parasitics on the switching behavior.



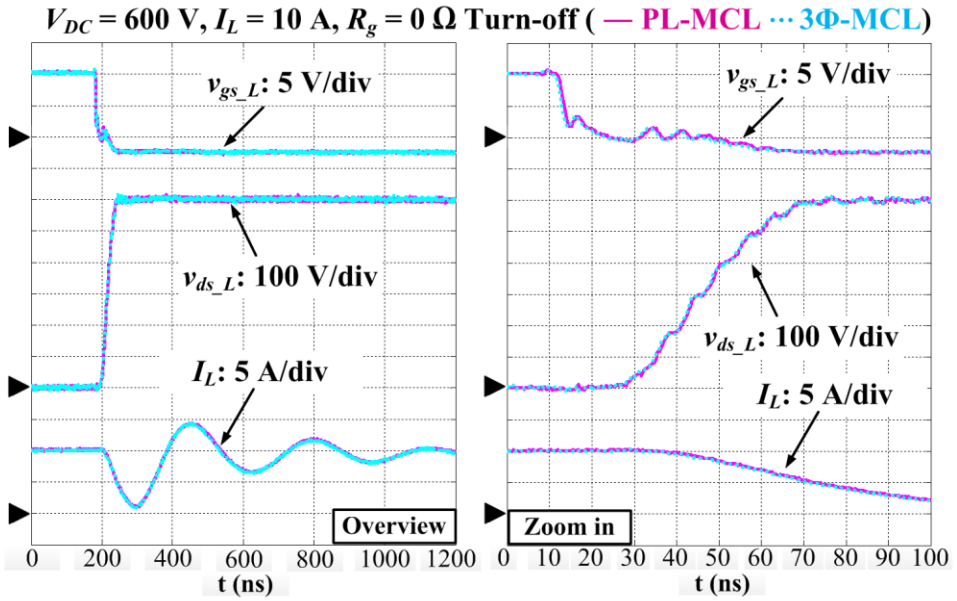
(a) 3Φ-MCL-1. (b) 3Φ-MCL-2.

(c) 3Φ-MCL-3.

Fig. 7-8. Test circuits for evaluation of the impact of switch states of two more phase-legs on the switching behavior.



(a) Turn-on transient.



(b) Turn-off transient.

Fig. 7-9. Impact of parasitics induced by two more phase-legs on the switching performance.

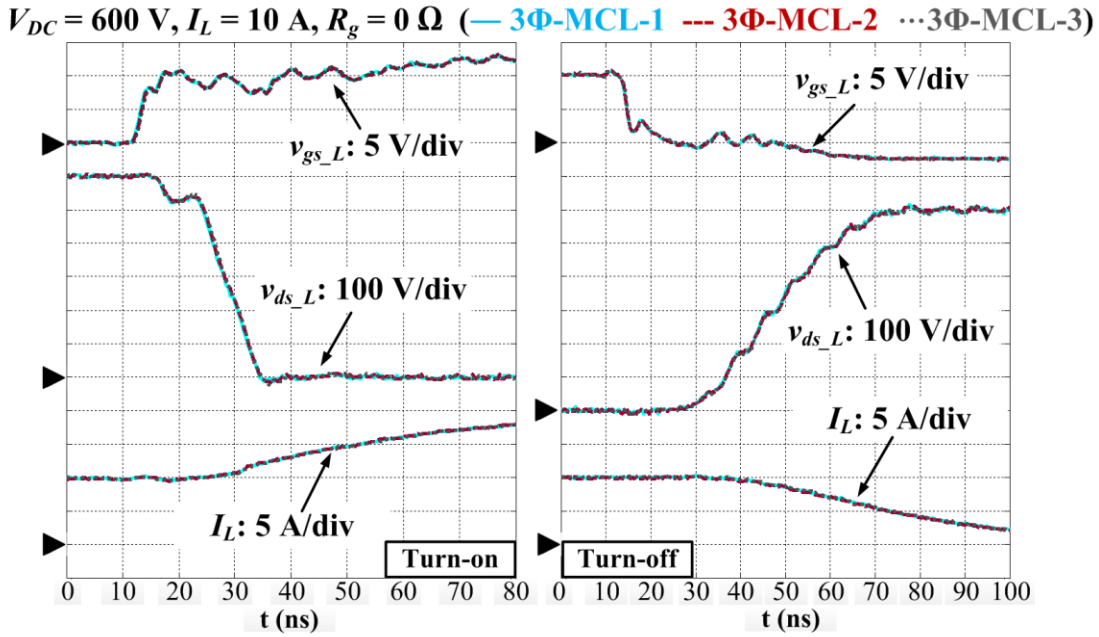
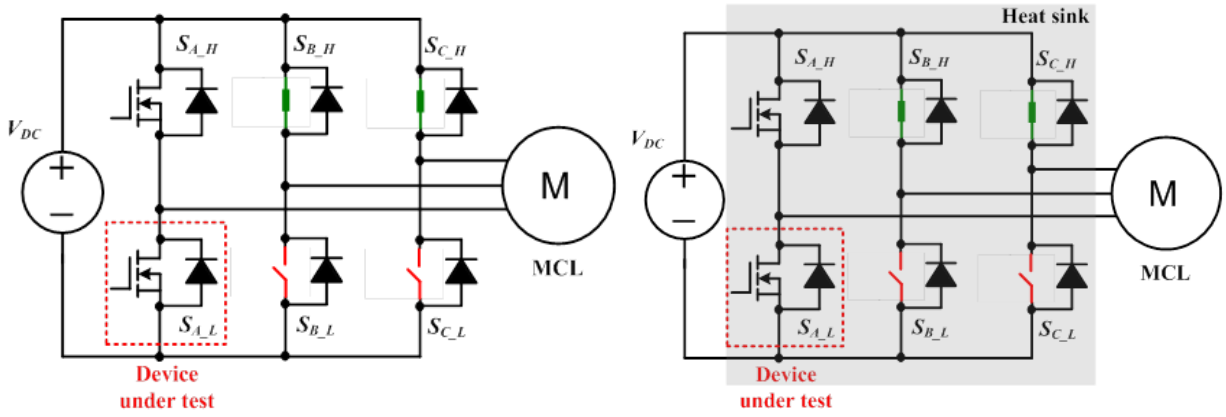


Fig. 7-10. Impact of switch states of two more phase-legs on the switching behavior.



(a) 3Φ-MCL-1. (b) 3Φ-MCL-HS-1.

Fig. 7-11. Test circuits for evaluation of the impact of heat sink on the switching behavior.

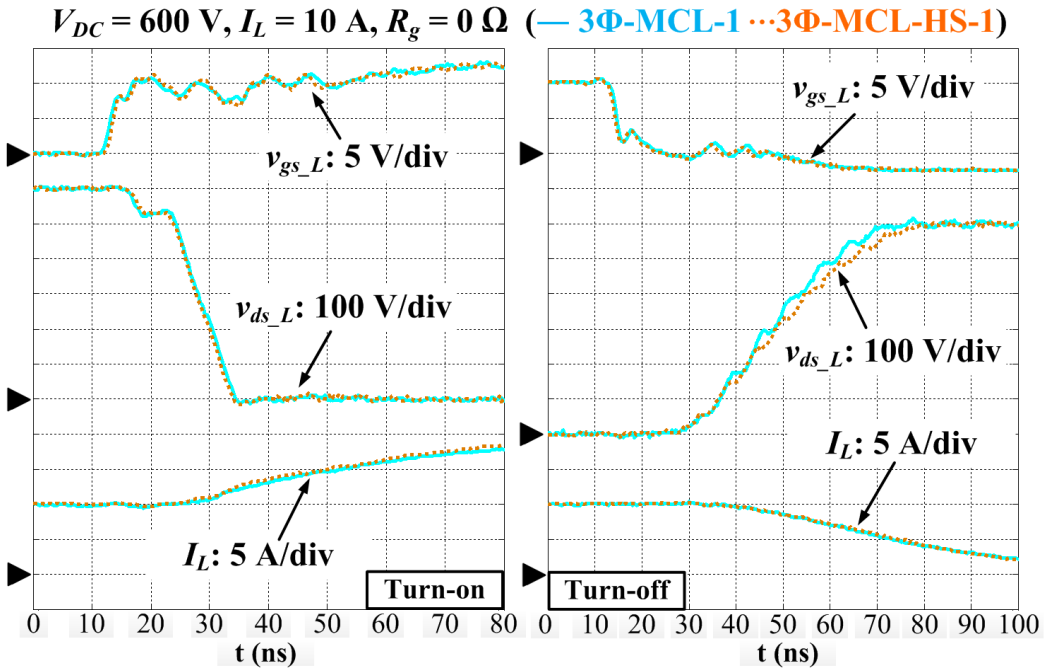
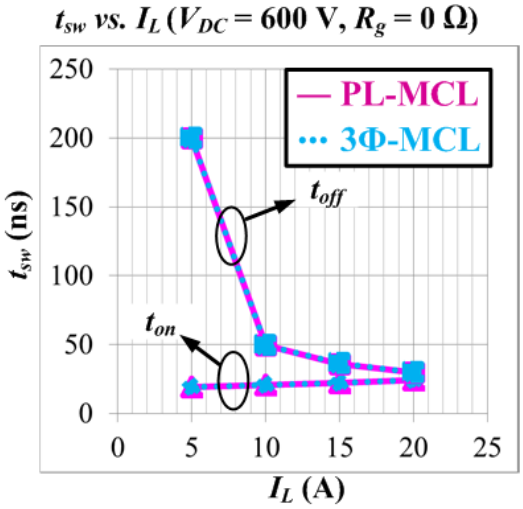


Fig. 7-12. Impact of heat sink on the switching behavior.

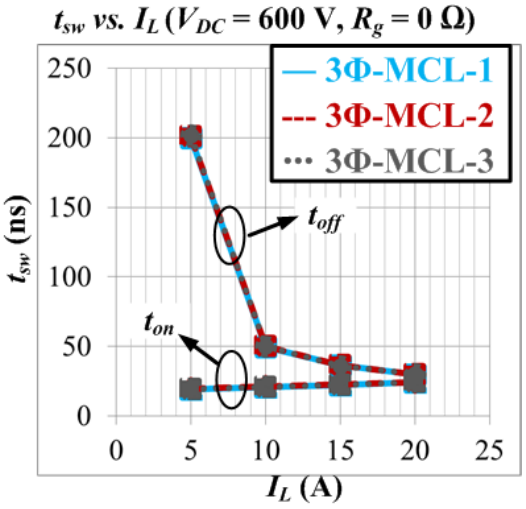
7.3 Realization of High Switching-Speed Performance of SiC Devices in Voltage Source Converter

Since the aforementioned test results are based on the pulse test, we cannot necessarily draw a conclusion for a voltage source converter when it operates until additional tests are done. Fig. 7-14 shows the gate signal, line-to-line voltage and phase current of the three-phase inverter when driving the induction motor. And then, we pick one switching cycle when the current direction enables the device under test to be the operating switch, and compare the switching waveforms between the running test and previous double pulse test. The switching waveforms in Fig. 7-15 shows that under the operating condition of 600-V/10-A with 0-Ω gate resistance, when the induction motor rotates, the switching performance is almost identical to that tested with MCL load by using the DPT board (DPT-MCL) during both turn-on and turn-off transients.

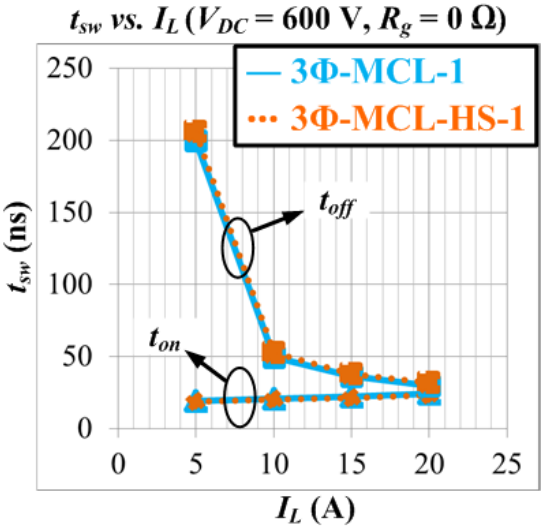
Additionally, the switching performance of SiC devices in the actual three-phase VSC can mostly repeat the excellent switching behavior measured by the DPT board with the optimally-designed DPT load (DPT-DPT).



(a) Impact of phase-legs's parasitics.



(b) Impact of phase-legs' switch states.



(c) Impact of heat sink.

Fig. 7-13. Comparison test results dependence on load currents with MCL load for the evaluation of the impact of two more phase-legs and heat sink on the switching performance.

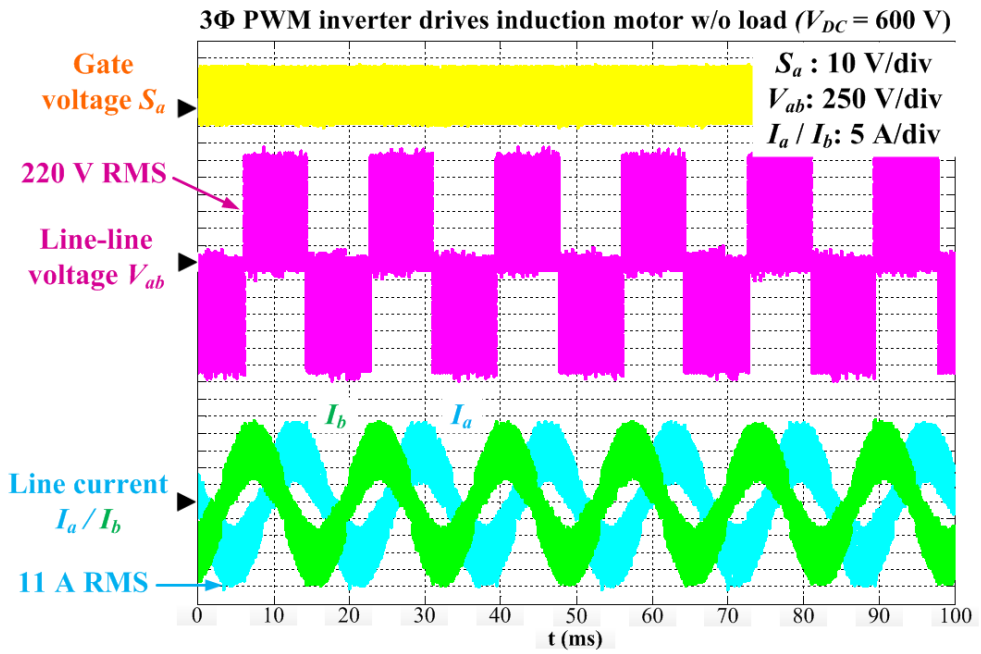


Fig. 7-14. Typical waveforms of three-phase voltage source inverter fed motor drives under continuous operating condition.

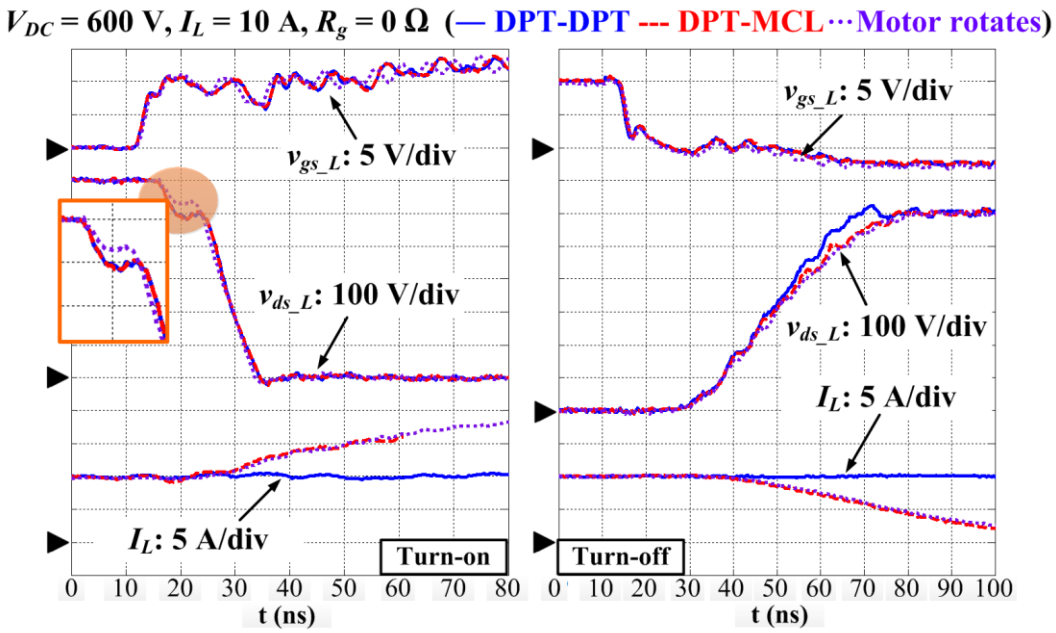
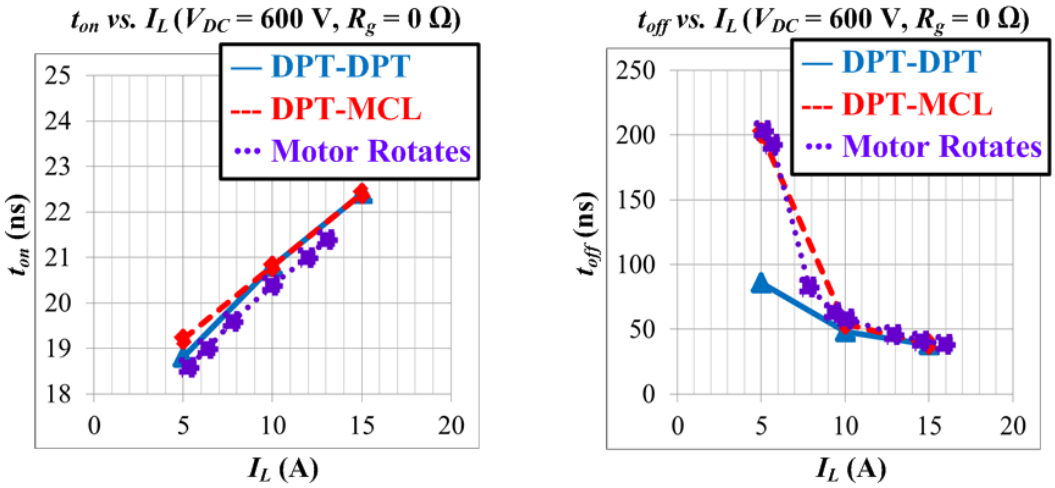
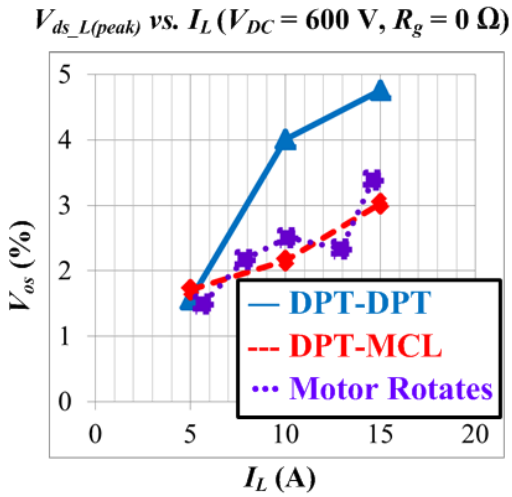


Fig. 7-15. Ultimate switching waveform comparisons: three-phase voltage source inverter fed motor drives versus double pulse tester.

More comparison test results in Fig. 7-16 further verify that as compared to the switching performance tested by the DPT board, the similar high switching-speed performance of SiC devices can be realized in the voltage source converter.



(a) Turn-on time dependence on load current. (b) Turn-off time dependence on load current.



(c) Voltage spike dependence on load current.

Fig. 7-16. Ultimate comparison test results dependence on load currents: three-phase voltage source converter versus double pulse tester.

7.4 Conclusion

By comprehensively utilizing all the developed knowledge and techniques in previous chapters, a three-phase VSC with Cree 2nd generation 1200-V/20-A SiC MOSFETs is built based on the intelligent gate driver and optimal interconnection design. Test results show that the switching behavior of SiC devices in the actual three-phase VSC fed motor drives can mostly repeat the excellent switching performance tested by the optimally-designed DPT board with DPT inductor. In the end, the high switching-speed capability of SiC devices has been realized in VSC.

8 Conclusion and Future Work

8.1 Conclusion

This dissertation systematically investigates the characterization and realization of high switching-speed capability of SiC devices in voltage source converter. The conclusion can be draw as follows.

- Five factors need to be taken into account for the switching characterization of SiC devices in the phase-leg configuration. First, layout of the DPT board should be universal for the actual converters and optimized for the sensitive parasitics (e.g., power loop inductance, common source inductance and Miller capacitance). Second, probes for switching waveforms should satisfy bandwidth, dynamic range, and accuracy requirements. Based on the comparison of the latest probes, high voltage passive probe and coaxial shunt are preferred. Third, voltage−current (V−I) timing alignment must be carefully deskewed due to its high sensitivity on switching losses (tested up to 272 μJ/ns). Fourth, probes induced grounding effects should be suppressed for the measurement accuracy of high-speed switching waveforms. Common-mode choke and probe-tip adaptor are recommended. Fifth, in a phase-leg, the switching losses of the non-operating devices cannot be ignored, especially for the fast switching SiC devices. To cope with the sensitivity issue of V−I timing alignment and the complexity of testing two devices for the switching loss evaluation, a practical method by calculating the difference between the input energy supplied by a dc capacitor and the output energy stored in a load inductor is proposed. The experimental results show that this method can accurately obtain the switching losses of both devices by merely monitoring one

switching current and voltage. Also, its test results are insensitive to the V−I alignment. Additionally, the commonly observed parasitic ringing in the switching waveforms does not need to be taken into account for the switching loss assessment. This is because the switching energy contributed by damping parasitic ringing is at most the energy dissipation induced by reverse recovery and the energy stored in parasitics, which is a small portion of the total switching losses.

- Six potentially impact factors of high switching-speed performance of SiC devices are investigated. First, the reverse recovery performance of the SiC MOSFETs' body diode at room temperature is satisfying, but it becomes poor at high operating temperature. It is recommended to have the antiparallel Schottky diode to guarantee the stable switching performance among wide operating temperature range. Second, the turn-on over-voltage is worse than the traditionally-focused turn-off voltage overshoot. To avoid voltage spike during turn-on beyond the device's breakdown voltage, the switching speed is limited within a *dv/dt*, *di/dt* related safe operating area. Third, the cross-talk induces a spurious gate voltage on its complementary device, which may generate shoot-through current and degrade the device. Thus, to avoid this failure, the switching speed has to be limited. Forth, the parasitics of the inductive load, such as the induction motor, especially with a relatively long power cable, will significantly impact the switching performance, leading to longer switching time, increased switching loss and serious parasitic ringing as compared to that yielded from double pulse test. Fifth, the interactions among three phase-legs cannot be ignored unless the decoupling capacitors are mounted close to each phase-leg to support the dc bus voltage during the switching transients. Sixth, the coupling capacitance due to the heat sink equivalently

increases the junction capacitance of power devices; however, its influence on the switching behavior in motor drives is small considering the relatively large capacitive parasitics of the motor load.

- Three intelligent gate drivers are developed for cross-talk suppression and overall switching performance improvement. First, two gate assist circuits are investigated for cross-talk suppression. The test results show that both gate assist circuits improve the switching performance under different operating conditions in comparison to the conventional gate driver: turn-on transient becomes fast, turn-on switching losses are reduced, and spurious negative gate voltage is minimized within its maximum required range. In addition, compared with the gate voltage control (GVC) assist circuit with two transistors and one diode, the gate impedance regulation (GIR) circuit with one transistor and one capacitor is simpler, but less effective for cross-talk suppression due to the large internal gate resistance of SiC devices. Furthermore, the gate impedance regulation (GIR) circuit is a suitable gate assist methodology for board-level integration, while the all transistor based gate voltage control (GVC) assist circuit is a more promising option for cross-talk suppression for gate driver chip-level integration. Second, to further improve the gate driving capability, an intelligent gate driver employing two auxiliary transistors together with two diodes is proposed. The test results verify that this approach has the capability of tuning the gate voltage and gate loop resistance during different switching transients so that both lower and upper switches in a phase-leg can be best served. As compared to the conventional gate drivers, the overall switching performance has been improved by means of the proposed intelligent gate driver with increased switching speed, reduced switching energy loss,

and minimized spurious gate voltages induced by cross-talk during both turn-on and turn-off transients. This gate driver strategy offers a simple, efficient, and cost-effective solution to increase the utilization of the high switching-speed capabilities of SiC devices. Also, it is a promising option for the gate driver chip-level integration.

- Interconnection design optimization is explored for the switching performance improvement of SiC devices in voltage source converter. First, the placement of gate drivers, devices and power stage are investigated to minimize the effective length of power devices' leads in the switching loop. The proposed placement minimizes the common source inductance and power loop inductance by up to 28.6% as compared to that when the conventional placement is employed, offering a best tradeoff between the switching speed and the voltage stress under different operating conditions. Furthermore, the PCB layout design of the power stage board is optimized on the basis of P-cell and N-cell concept and magnetic field cancellation. In the end, parasitic inductance associated in the power loop is minimized to be 17 nH, of which 84% is induced by TO-247 package. It means that instead of the placement and layout design, package itself becomes the hurdle to further reduce the power loop inductance. Second, a dedicated auxiliary inductor is designed and inserted between the converter and inductive load so that the parasitics of the load will not be "seen" from the converter side during the switching transient. The test results verify that the proposed auxiliary inductor is capable of mitigating the interaction between the inductive load and power device among a wide operating range: except the turn-off time at the light load, the switching time under the rest of the operating conditions together with the switching losses under all of the operating points will not be affected by the parasitics of the inductive load.

Also, it is noted that the extra loss dissipated by the auxiliary inductor is lower than the switching loss reduction for the high switching frequency applications (> 50 kHz in this case study), leading to an overall efficiency improvement in the power conversion system.

- A three-phase voltage source converter with Cree 2nd generation 1200-V/20-A SiC MOSFETs is built by leveraging the intelligent gate driver and optimal interconnection design developed above. Test results show that the switching behavior of SiC devices in this three-phase voltage source converter fed motor drives can mostly repeat the excellent switching performance tested by the optimally-designed DPT board with DPT load inductor. In the end, the high switching-speed capability of SiC devices has been realized in voltage source converter.

8.2 Future Work

- Reconsideration of the design and operation for SiC based voltage source converter (VSC)

  Switching behavior of SiC power semiconductor devices highly depends on operating conditions and significantly affects the final performance of VSC. To achieve higher performance power conversion among a wide operating range, the design and operation of SiC based VSC should be intelligently regulated based on the switch status (e.g., switching time, switching loss, voltage spike, junction temperature) to fully utilize the potential benefits of SiC devices.

  For example, the dead-time in traditional IGBT based VSC is fixed and determined by turn-off time at the worst operating condition (maximum dc bus voltage, largest load

current, highest operating temperature) with sufficient safe margin. However, for SiC devices, considering the high sensitivity of turn-off time on operating conditions and relatively large reverse conduction loss, it is preferred to adaptively tune the dead-time under different operating conditions on the basis of the insight on the turn-off behavior of SiC devices. Therefore, the optimal tradeoff between reliability and efficiency can be achieved. [133] demonstrates that by using the adaptive dead-time regulation, the power loss decreases by 12% at full load and 18.2% at light load in SiC based VSC.

In addition to the dead-time setting, there are many degrees of freedom we can intelligently design and adaptively regulate based on the deep understanding of switch status in SiC based VSC, such as gate driver circuits, switching frequency, modulation scheme, etc. In the end, SiC devices are able to achieve a performance approaching their inherent capabilities, reducing unnecessary overdesign, and bypassing performance limitations.

- Reliability diagnosis, prediction, and improvement for SiC based voltage source converter

Although the emerging SiC devices demonstrate excellent performance in terms of efficiency and power density for power conversion system, currently fewer SiC transistors are utilized in industrial products, mainly due to the high cost and reliability concerns. Therefore, it is an important and promising research topic on reliability diagnosis, prediction, and improvement for SiC based voltage source converter.

Recently, several related work is carried out for IGBT in high power applications, such as thermal modeling and lifetime estimation [136, 137], online junction temperature monitoring [138-140], reliability oriented design of power electronics

converter [141-146]. However, for SiC devices, the fast switching speed, limited short circuit capability, high temperature capability, and advanced packaging technologies bring new challenges in terms of reliability.

- Suppression of high *dv/dt* induced adverse impact on motor drive applications

  High switching-speed capability of SiC devices is beneficial to the switching loss and switching time. But for motor drive applications, high *dv/dt* worsens the over-voltage at the motor terminal as well as its insulation with significantly increased CM noise and EMI [147]. Therefore, sometimes, the high switching-speed capability of SiC devices has to be sacrificed to compromise the adverse impact induced by high *dv/dt*.

  To cope with this issue, the development of a motor "friendly" converter with SiC devices to suppress the high *dv/dt* induced adverse impact is critical.

- Switching performance evaluation and improvement of GaN transistor and high voltage SiC devices

  Generally, the device under investigation in this dissertation focuses on Cree 1200-V, 20-A to 50-A SiC MOSFETs. It would be interesting to leverage the knowledge accumulated and approached proposed in this study for the investigation of GaN transistors and high voltage SiC devices.

- Development of gate driver IC integrated with more functionality

  To efficiently utilize the proposed gate driving schemes in SiC based power converters, it is important to integrate the intelligent assist circuits into the gate driver IC.

8.3 Publication List

Journal Papers

- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, "Evaluation of switching performance of SiC devices in PWM inverter fed induction motor drives", in *Proc. IEEE Trans. Power Electronics*, accepted.
- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, "Active gate driver for cross talk suppression of SiC power devices in a phase-leg configuration", in *Proc. IEEE Trans. Power Electronics*, vol. 29, no. 4, April. 2014, pp. 1986-1997.

Conference Papers

- **Z. Zhang**, Z. Wang, F. Wang, L. M. Tolbert, B. J. Blalock, "Reliability-oriented design of gate driver for SiC devices in voltage source converter", in *Proc. IEEE Integrated Power Packaging,* May. 2015, accepted.
- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, "Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration", *in Proc. IEEE Applied Power Electronics Conference and Exposition,* March. 2015, pp. 774-781.
- **Z. Zhang**, D. J. Costinett, H. Lu, F. Wang, L. M. Tolbert, B. J. Blalock, "Dead-time optimization of SiC devices for voltage source converter", *in Proc. IEEE Applied Power Electronics Conference and Exposition,* March. 2015, pp. 1145-1152.
- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, "Understanding the limitations and impact factors of wide bandgap devices' high switching-speed capability in a voltage source converter", in *Proc. IEEE Wide Bandgap Power Devices and Applications,* Oct. 2014, pp. 7-12.
- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, "Evaluation of switching performance of SiC devices in PWM inverter fed induction motor drives", in *Proc. IEEE Energy Conversion Congress and Exposition,* Sept. 2014, pp. 1597-1604.

- **Z. Zhang**, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, "Impact of ringing on switching losses of Wide Band-Gap devices in a phase-leg configuration", in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March. 2014, pp. 2542-2549.
- **Z. Zhang**, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, P. Ning "Methodology for switching characterization evaluation of Wide Band-Gap devices in a phase-leg configuration", in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March. 2014, pp. 2534- 2541.
- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, "A gate assist circuit for cross talk suppression of SiC power devices in a phase-leg configuration", in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2013, pp. 2536-2543.
- **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, "A novel gate assist circuit for cross talk mitigation of SiC power devices in a phase-leg configuration", in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March. 2013, pp. 1259-1265.
- **Z. Zhang**, W. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2012, pp. 3950-3955.
- W. Zhang, Z. Xu, **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, "Evaluation of 600 V cascode GaN HEMT in device characterization and all-GaN-based LLC resonant converter", in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2013, pp. 3571-3578.
- B. Guo, F. Xu, **Z. Zhang**, Z. Xu, F. Wang, L. M. Tolbert, B. J. Blalock, "Compensation of input current distortion in three-phase buck rectifier", in *Proc. IEEE Applied Power Electronics Conference and Exposition*, March. 2013, pp. 930-938.
- W. Zhang, Y. Long, **Z. Zhang**, F. Wang, L. M. Tolbert, B. J. Blalock, S. Henning, C. Wilson, R. Dean, "Evaluation and comparison of silicon and gallium nitride power transistors in LLC resonant converter", in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2012, pp. 1362-1366.

Reference

[1] T. Heidel, "Achieving high efficiency, high power density, high reliability, & low cost," in *ARPA-E initiatives in power electronics*, ed. Ft. Worth: Adacanced research projects agency, U.A. Department of Energy, 2014.

[2] EIA, "Annual energy review DOE/EIA-0394 (2011)," 2012.

[3] http://www.eia.gov/energyexplained/index.cfm?page=electricity_use.

[4] http://apps1.eere.energy.gov/news/news_detail.cfm/news_id=15650.

[5] http://www.abb.us/cawp.

[6] Two major uses of power electronics [Online]. Available: www.engr.colostate.edu/ECE562/

[7] B. K. Bose, "Recent advances and applications of power electronics and motor drives - introduction and perspective," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE* 2008, pp. 25-27.

[8] Changing the way electricity is used [Online]. Available: www.ece.vt.edu/news/ar09/cpes.php

[9] L. Rixin, W. Fei, R. Burgos, P. Yunqing, D. Boroyevich, W. Bingsen, T. A. Lipo, V. D. Immanuel, and K. J. Karimi, "A Systematic Topology Evaluation Methodology for High-Density Three-Phase PWM AC-AC Converters," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 2665-2680, 2008.

[10] M. P. Bahrman, J. G. Johansson, and B. A. Nilsson, "Voltage source converter transmission technologies - the right fit for the application," ABB Inc.

[11] S. Cole and R. Belmans, "Transmission of bulk power," *Industrial Electronics Magazine, IEEE,* vol. 3, pp. 19-24, 2009.

[12] H. Xie, "Voltage source converters with energy storage capability," KTH Electrical Engineering, Stockholm2006.

[13] J. H. Chow, "Voltage-sourced converter based FACTs controller seminar," presented at the NSF US-Africa research and education collaboration workshop, 2004.

[14] Z. Hui, L. M. Tolbert, and B. Ozpineci, "Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles," *Industry Applications, IEEE Transactions on*, vol. 47, pp. 912-921, 2011.

[15] B. Ozpineci, L. M. Tolbert, and S. K. Islam, "Silicon carbide power device characterization for HEVs," in *Power Electronics in Transportation, 2002*, 2002, pp. 93-97.

[16] F. Shang, A. P. Arribas, and M. Krishnamurthy, "A comprehensive evaluation of SiC devices in traction applications," in *Transportation Electrification Conference and Expo (ITEC), 2014 IEEE*, 2014, pp. 1-5.

[17] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, 2001.

[18] D. Grant, "Power MOSFETs: theory and applications," 1989.

[19] J. Liu, K. L. Wong, S. Allen, and M. John, "Performance evaluations of hard-switching interleaved DC/DC boost converter with new generation silicon carbide MOSFETs," Cree Inc.

[20] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2393-2407, 2014.

[21] P. Bogonez-Franco and J. B. Sendra, "EMI comparison between Si and SiC technology in a boost converter," in *Electromagnetic Compatibility (EMC EUROPE), 2012 International Symposium on*, 2012, pp. 1-4.

[22] E. Rondon, F. Morel, C. Vollaire, and J. L. Schanen, "Impact of SiC components on the EMC behaviour of a power electronics converter," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 4411-4417.

[23] G. Xun and J. A. Ferreira, "Comparison and Reduction of Conducted EMI in SiC JFET and Si IGBT-Based Motor Drives," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1757-1767, 2014.

[24] G. Xun, Josifovic, x, I., and J. A. Ferreira, "Modeling and Reduction of Conducted EMI of Inverters With SiC JFETs on Insulated Metal Substrate," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 3138-3146, 2013.

[25] P. Roussel, "SiC market and industruy update," presented at the Int. SiC Power Electron. Appl. Workshop, Kista, Sweden, 2011.

[26] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2155-2163, 2014.

[27] Rohm, SiC Application Note: SiC power devices and modules [Online]. Available: www.rohm.com/documents/11303/2861707/sic_app-note.pdf

[28] J. Wang, "Design, Characterization, Modeling and Analysis of High Voltage Silicon Carbide Power Devices," Ph.D., North Carolina State Univ., 2010.

[29] S. Xu, A. Q. Huang, and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," *Emerging and Selected Topics in Power Electronics, IEEE Journal of,* vol. 1, pp. 186-198, 2013.

[30] A. Hefner, R. Sei-Hyung, B. Hull, D. Berning, C. Hood, J. M. Ortiz-Rodriguez, A. Rivera-Lopez, D. Tam, A. Adwoa, and M. Hernandez-Mora, "Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Devices," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE*, 2006, pp. 330-337.

[31] B. Callanan. CREE CPWR AN-08. Application considerations for silicon carbide MOSFETs [Online]. Available: http://www.cree.com

[32] C. J. Cass, W. Yi, R. Burgos, T. P. Chow, F. Wang, and D. Boroyevich, "Evaluation of SiC JFETs for a Three-Phase Current-Source Rectifier with High Switching Frequency,"

in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 345-351.

[33] I. Josifovic, J. Popovic-Gerber, and J. A. Ferreira, "Improving SiC JFET Switching Behavior Under Influence of Circuit Parasitics," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 3843-3854, 2012.

[34] R. Burgos, C. Zheng, D. Boroyevich, and F. Wang, "Design considerations of a fast 0-Ω gate-drive circuit for 1.2 kV SiC JFET devices in phase-leg configuration," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 2293-2300.

[35] Z. Chen, "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices," Master of Science, Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, 2009.

[36] M. Danilovic, C. Zheng, W. Ruxi, L. Fang, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2681-2688.

[37] Z. Weimin, X. Zhuxian, Z. Zheyu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Evaluation of 600 V cascode GaN HEMT in device characterization and all-GaN-based LLC resonant converter," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 3571-3578.

[38] B. Callanan. SiC MOSFET double pulse fixture [Online]. Available: http://www.cree.com

[39] Semisouth AN-SS1. Silicon carbide enhancement-mode junction field effect transistor and recommendations for use. [Online]. Available: http://www.semisouth.com

[40] J. B. Witcher, "Methodology for Switching Characterization of Power Devices and Modules," Master of Science, Electrical Engineering, Virginia Polytechnic Institute and State University.

[41] Tektronix, Primer: ABCs of Probes [Online]. Available: www.tek.com

[42] Tektronix, high-voltage differential probes [Online]. Available: http://www.tek.com

[43] Tektronix, passive high voltage probes [Online]. Available: http://www.tek.com

[44] D. A. Ward and J. L. T. Exon, "Using Rogowski coils for transient current measurements," *Engineering Science and Education Journal*, vol. 2, pp. 105-113, 1993.

[45] PEARSON Current monitor 2877 Datasheet [Online]. Available: http://www.pearsonelectronics.com/pdf/2877.pdf

[46] PEM CWT mini specification [Online]. Available: http://www.pemuk.com/Userfiles/CWTmini/cwt_mini_1110.pdf

[47] T & M research products, SSDN series coaxial shunt [Online]. Available: http://www.tandmresearch.com/

[48] Tektronix, TCP0030A datasheet [Online]. Available: http://www.tek.com

[49] Tektronix, Power supply measurement and analysis [Online]. Available: http://www.tektronix.com.

[50] Tektronix, Improve measurement accuracy and reduce cost with passive probes from Tektronix [Online]. Available: http://www.tektronix.com

[51] L. Balogh, "Design and application guide for high speed MOSFET gate drive circuits," in *Power Supply Design Seminar*, 2001.

[52] P. J. Grbovic, "Advanced power semiconductors: art of control, from theory to practice," presented at the Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, Denver, 2013.

[53] Z. Wei, H. Xiucheng, F. C. Lee, and L. Qiang, "Gate drive design considerations for high voltage cascode GaN HEMT," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 1484-1489.

[54] Z. Zheyu, Z. Weimin, F. Wang, L. M. Tolbert, and B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 3950-3955.

[55] C. M. Zhen, "Keep Hybrid Powertrain Drives Noise Free by Rejecting dV/dt Noise With Isolated-Gate Drivers," Avago Technologies2008.

[56] C. L. Fandrich, "An on-chip transformer-based digital isolator system," Master of Science, Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, 2013.

[57] Avago Technologies, ACPL_4800 high CMR intelligent power module and gate drive interface opticoupler datasheet [Online]. Available: http://www.avagotech.com/docs/AV01-0193EN

[58] Analog Devices, Dual-channel Isolator ADuM5240 datasheet [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADUM5240_5241_5242.pdf

[59] Z. Huibin, A. R. Hefner, and L. Jih-Sheng, "Characterization of power electronics system interconnect parasitics using time domain reflectometry," *Power Electronics, IEEE Transactions on,* vol. 14, pp. 622-628, 1999.

[60] F. Merienne, J. Roudet, and J. L. Schanen, "Switching disturbance due to source inductance for a power MOSFET: analysis and solutions," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 1743-1747 vol.2.

[61] W. Teulings, J. L. Schanen, and J. Roudet, "MOSFET switching behaviour under influence of PCB stray inductance," in *Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE*, 1996, pp. 1449-1453 vol.3.

[62] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, 2004, pp. 516-521 Vol.1.

[63] C. Zheng, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 164-169.

[64] Z. Chen, D. Boroyevich, and J. Li, "Behavioral comparison of Si and SiC power MOSFETs for high-frequency applications," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 2453-2460.

[65] http://epc-co.com/epc/.

[66] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability Considerations for Silicon Carbide Field-Effect Transistors," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 4453-4459, 2013.

[67] E. Matheson, A. von Jouanne, and A. Wallace, "Evaluation of inverter and cable losses in adjustable speed drive applications with long motor leads," in *Electric Machines and Drives, 1999. International Conference IEMD '99*, 1999, pp. 159-161.

[68] T. Appel, "Reverse recovery behavior of the body diode of the SiC MOSFET," in *PCIM*.

[69] ROHM. SiC Power Devices and Modules [Online]. Available: http://rohmfs.rohm.com/

[70] J. Dong, R. Burgos, W. Fei, and D. Boroyevich, "Temperature-Dependent Characteristics of SiC Devices: Performance Evaluation and Loss Calculation," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 1013-1024, 2012.

[71] W. Zhiqiang, S. Xiaojie, L. M. Tolbert, W. Fei, and B. J. Blalock, "A di/dt Feedback-Based Active Gate Driver for Smart Switching and Fast Overcurrent Protection of IGBT Modules," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 3720-3732, 2014.

[72] P. J. Grbovic, "An IGBT Gate Driver for Feed-Forward Control of Turn-on Losses and Reverse Recovery Current," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 643-652, 2008.

[73] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 849-855, 2006.

[74] V. John, S. Bum-Seok, and T. A. Lipo, "High-performance active gate drive for high-power IGBT's," *Industry Applications, IEEE Transactions on*, vol. 35, pp. 1108-1117, 1999.

[75] C. Licitra, S. Musumeci, A. Raciti, A. U. Galluzzo, R. Letor, and M. Melito, "A new driving circuit for IGBT devices," *Power Electronics, IEEE Transactions on*, vol. 10, pp. 373-378, 1995.

[76] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "A new adaptive driving technique for high current gate controlled devices," in *Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings 1994., Ninth Annual*, 1994, pp. 480-486 vol.1.

[77] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "Switching-behavior improvement of insulated gate-controlled devices," *Power Electronics, IEEE Transactions on*, vol. 12, pp. 645-653, 1997.

[78] T. Shimizu and K. Wada, "A gate drive circuit of power MOSFETs and IGBTs for low switching losses," in *Power Electronics, 2007. ICPE '07. 7th Internatonal Conference on*, 2007, pp. 857-860.

[79] S. Yaxiu, S. Li, A. Esmaeli, and Z. Ke, "A Novel Three Stage Drive Circuit for IGBT," in *Industrial Electronics and Applications, 2006 1ST IEEE Conference on*, 2006, pp. 1-6.

[80] D. Lan, H. Kuhn, and A. Mertens, "Digital Adaptive Driving Strategies for High-Voltage IGBTs," *Industry Applications, IEEE Transactions on,* vol. 49, pp. 1628-1636, 2013.

[81] L. Michel, X. Boucher, A. Cheriti, P. Sicard, and F. Sirois, "FPGA Implementation of an Optimal IGBT Gate Driver Based on Posicast Control," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2569-2575, 2013.

[82] J. Colmenares, D. Peftitsis, J. Rabkowski, D. P. Sadik, and H. P. Nee, "Dual-Function Gate Driver for a Power Module With SiC Junction Field-Effect Transistors," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2367-2379, 2014.

[83] W. Jianjing and H. S. h. Chung, "A passive level-shifter for elimination of spurious turn-on in the bridge-leg configuration," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 1920-1925.

[84] R. Kelley, A. Ritenour, D. Sheridan, and J. Casady, "Improved two-stage DC-coupled gate driver for enhancement-mode SiC JFET," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 1838-1841.

[85] S. Tong, R. Xiaoyong, D. Hao, Z. Zhiliang, and R. Xinbo, "Three-level driving method for GaN transistor with improved efficiency and reliability within whole load range," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 2569-2573.

[86] B. Wrzecionko, D. Bortis, J. Biela, and J. W. Kolar, "Novel AC-Coupled Gate Driver for Ultrafast Switching of Normally Off SiC JFETs," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 3452-3463, 2012.

[87] R. Xiaoyong, D. Reusch, J. Shu, Z. Zhiliang, M. Mingkai, and F. C. Lee, "Three-level driving method for GaN power transistor in synchronous buck converter," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 2949-2953.

[88] Y. Zushi, S. Sato, K. Matsui, Y. Murakami, and S. Tanimoto, "A novel gate assist circuit for quick and stable driving of SiC-JFETs in a 3-phase inverter," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 1734-1739.

[89] M. S. Mazzola and R. Kelley, "Application of a Normally OFF Silicon Carbide Power JFET in a Photovoltaic Inverter," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 649-652.

[90] Texas Instruments, LM5113 Datasheet [Online]. Available: www.ti.com

[91] W. Ruxi, M. Danilovic, D. Boroyevich, C. Zheng, and R. Kaushik, "Transformer-isolated gate drive design for SiC JFET phase-leg module," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 1728-1733.

[92] Cree, Design considerations for designing with CREE SiC Modules: Part 2. techniques for minimizing parasitic inductance [Online]. Available: http://www.cree.com

[93] Cree, Design Considerations for Designing with Cree SiC Modules Part 1. Understanding the Effects of Parasitic Inductance [Online]. Available: www.cree.com

[94] Fairchild, AN-9005: Driving and layout design for fast switching super-junction MOSFETs [Online]. Available: www.fairchildsemi.com

[95] G. J. Krausse. Direct Energy, Inc.: DE-series fast power MOSFET™: an introduction [Online]. Available: www.ixyscolorado.com/

[96] "Freescale Semiconductor, Application Note: Power Quad Flat No-lead (PQFN) Package."

[97] L. Zhengyang, H. Xiucheng, Z. Wenli, F. C. Lee, and L. Qiang, "Evaluation of high-voltage cascode GaN HEMT in different packages," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 168-173.

[98] S. Li, "Packaging design of IGBT power module using novel switching cells," PhD diss., University of Tennessee, 2011.

[99] P. Ning, Z. Liang, and F. Wang, "Double-sided cooling design for novel planar module," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 616-621.

[100] L. Zhenxian, N. Puqi, F. Wang, and L. Marlino, "Planar bond all: A new packaging technology for advanced automotive power modules," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 438-443.

[101] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high frequency gallium nitride based point of load converter," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 649-655.

[102] C. Zheng, M. Danilovic, D. Boroyevich, and S. Zhiyu, "Modularized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-10.

[103] C. Zheng, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 1886-1893.

[104] L. Qian, W. Shuo, A. C. Baisden, W. Fei, and D. Boroyevich, "EMI Suppression in Voltage Source Converters by Utilizing dc-link Decoupling Capacitors," *Power Electronics, IEEE Transactions on*, vol. 22, pp. 1417-1428, 2007.

[105] Z. Zheyu and Wang, "Driving and Characterization of wide bandgap semiconductors for voltage source converter applications," in *Wide Bandgap Power Devices and Applications (WiPDA), 2014 IEEE Workshop on*, 2014, pp. 1-84.

[106] J. A. Ferreira, W. A. Cronje, and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE,* 1992, pp. 1284-1290 vol.2.

[107] Tektronix, power measurement deskew & calibration fixture instructions [Online]. Available: http://www.tek.com

[108] L. Huawu, W. Hongfei, L. Yangjun, X. Yan, and S. Kai, "A high efficiency inverter based on SiC MOSFET without externally antiparalleled diodes," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 163-167.

[109] C. Cai, W. Zhou, and K. Sheng, "Characteristics and Application of Normally-Off SiC-JFETs in Converters Without Antiparallel Diodes," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 4850-4860, 2013.

[110] Z. Zheyu, G. Ben, F. Wang, L. M. Tolbert, B. J. Blalock, L. Zhenxian, and N. Puqi, "Impact of ringing on switching losses of wide band-gap devices in a phase-leg configuration," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 2542-2549.

[111] W. Jianjing, R. T. H. Li, and H. S. H. Chung, "An Investigation Into the Effects of the Gate Drive Resistance on the Losses of the MOSFET-Snubber-Diode Configuration," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 2657-2672, 2012.

[112] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics - Converters, Appliations and Design*. New York: Wiley, 1995.

[113] T. Wu. International Rectifier, Cdv/dt induced turn-on in synchronous buck regulations [Online]. Available: http://www.irf.com/

[114] A. Elbanhawy, "MOSFET susceptibility to cross conduction," in *Power Electron. Technol.*, 2005, pp. 26-33.

[115] Fairchild Semiconductor AN-7019, Limiting Cross-Conduction Current in Synchronous Buck Converter Designs [Online]. Available: http://www.fairchildsemi.com/an/AN/AN-7019.pdf#page=1

[116] Fairchild FGA20N120FTD Datasheet, Rev A, Dec. 2007 [Online]. Available: http://www.fairchildsemi.com/ds/FG/FGA20N120FTD.pdf

[117] International Rectifier IRG4PH505 Datasheet, PD-96225, 02/09/09 [Online]. Available: http://www.irf.com/product-info/datasheets/data/irg4ph50s.pdf

[118] Microsemi APT34M120J Datasheet, 050-8088 Rev C, 7-2011 [Online]. Available: http://www.microsemi.com/en/sites/default/files/datasheets/APT3 4M120J_C.pdf

[119] Cree CMF20120D Datasheet, Rev A. [Online]. Available: http://www.cree.com/~/media/Files/Cree/Power/Data%20Sheets/CMF20120D.pdf

[120] Semisouth SJEP120R100 Datasheet, Rev 3.0 [Online]. Available: http://semisouth.com/wp-content/uploads/2011/05/SJEP120R100.pdf

[121] B. Mirafzal, G. L. Skibinski, R. M. Tallam, D. W. Schlegel, and R. A. Lukaszewski, "Universal Induction Motor Model With Low-to-High Frequency-Response

Characteristics," *Industry Applications, IEEE Transactions on,* vol. 43, pp. 1233-1246, 2007.

[122] Z. Zheyu, G. Ben, F. Wang, L. M. Tolbert, B. J. Blalock, L. Zhenxian, and N. Puqi, "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 2534-2541.

[123] A. Boglietti and E. Carpaneto, "Induction motor high frequency model," in *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*, 1999, pp. 1551-1558 vol.3.

[124] M. Schinkel, S. Weber, S. Guttowski, W. John, and H. Reichl, "Efficient HF modeling and model parameterization of induction machines for time and frequency domain simulations," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, 2006, p. 6 pp.

[125] W. Liwei, C. N. m. Ho, F. Canales, and J. Jatskevich, "High-Frequency Modeling of the Long-Cable-Fed Induction Motor Drive System Using TLM Approach for Predicting Overvoltage Transients," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 2653-2664, 2010.

[126] R. Kelley, F. Rees, and D. Schwob, "Optimized gate driver for enhancement-mode SiC JFET," in *PCIM*, 2009.

[127] Avago Technologies AN-5314. Active Miller clamp [Online]. Available: http://www.avagotech.com

[128] A. G. Black, "Impact of Source Inductance on Synchronous Buck Regulator FET Shoot Through Performance," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 981-986.

[129] B. Yang and J. Zhang, "Effect and utilization of common source inductance in synchronous rectification," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, 2005, pp. 1407-1411 Vol. 3.

[130] Z. Zheyu, F. Wang, L. M. Tolbert, and B. J. Blalock, "A novel gate assist circuit for cross talk mitigation of SiC power devices in a phase-leg configuration," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 1259-1265.

[131] Z. Zheyu, F. Wang, L. M. Tolbert, and B. J. Blalock, "A gate assist circuit for cross talk suppression of SiC devices in a phase-leg configuration," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 2536-2543.

[132] Z. Zheyu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1986-1997, 2014.

[133] Z. Zhang, D. J. Costinett, H. Lu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Dead-time optimization of SiC devices for voltage source converter," in *Applied Power Electronics Conference and Exposition*, 2015, pp. 1145-1152.

[134] J. Cain. Parasitic inductance of multilayer ceramic capacitors [Online]. Available: http://www.avx.com/

[135] Datasheet: CCS020M12CM2 [Online]. Available: http://www.cree.com/

[136] M. Ke, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 590-602, 2015.

[137] W. Rui, W. Huai, M. Ke, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 2901-2908.

[138] N. He and R. D. Lorenz, "Sensing power MOSFET junction temperature using gate drive turn-on current transient properties," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 2909-2916.

[139] H. Niu and R. D. Lorenz, "Sensing Power MOSFET Junction Temperature Using Circuit Output Current Ringing Decay," *Industry Applications, IEEE Transactions on,* vol. 51, pp. 1763-1773, 2015.

[140] N. Baker, S. Munk-Nielsen, M. Liserre, and F. Iannuzzo, "Online junction temperature measurement via internal gate resistance during turn-on," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[141] W. Huai, M. Ke, and F. Blaabjerg, "Design for reliability of power electronic systems," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 33-44.

[142] S. Yantao and W. Bingsen, "Survey on Reliability of Power Electronic Systems," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 591-604, 2013.

[143] W. Huai, Z. Dao, and F. Blaabjerg, "A reliability-oriented design method for power electronic converters," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 2921-2928.

[144] R. Burgos, C. Gang, F. Wang, D. Boroyevich, W. G. Odendaal, and J. D. van Wyk, "Reliability-Oriented Design of Three-Phase Power Converters for Aircraft Applications," *Aerospace and Electronic Systems, IEEE Transactions on,* vol. 48, pp. 1249-1263, 2012.

[145] Y. Shaoyong, X. Dawei, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 2734-2752, 2010.

[146] J. Morroni, A. Dolgov, M. Shirazi, R. Zane, and D. Maksimovic, "Online Health Monitoring in Digitally Controlled Power Converters," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 112-118.

[147] M. J. Scott, J. Brockman, H. Boxue, F. Lixing, X. Longya, W. Jin, and R. Darbali Zamora, "Reflected wave phenomenon in motor drive systems using wide bandgap devices," in *Wide Bandgap Power Devices and Applications (WiPDA), 2014 IEEE Workshop on*, 2014, pp. 164-168.

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