

**The Design of a CMOS Peak Detect and Hold Circuit for a
Portable Gamma Ray Spectroscopy System**

A Thesis

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Dedication

This thesis is dedicated to my beautiful wife, Rachel.

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Abstract

A new CMOS peak detect and hold (PDH) circuit based on the two stage, CMOS op amp topology has been developed for a portable gamma ray spectroscopy system under development at the Oak Ridge National Laboratory. The PDH circuit detects and holds a semi-Gaussian voltage pulse until it can be processed by the digital electronics. The PDH circuit operates over a dynamic range of greater than 150:1 with a maximum INL of 0.12 %. The PDH circuit has a wide bandwidth of 8.1 MHz, a minimum slew rate of 2 V/ μ s, a droop rate of only 4.5 μ V/ μ s, and a power consumption of less than 100 μ W. The control circuits required by the PDH circuit to function within the gamma ray spectroscopy system have also been developed and are presented. A review of gamma ray spectroscopy systems is included to set the context for the PDH circuit design. Then the design, analysis, and experimental results for the PDH prototype are presented. The prototype was fabricated in the 1.2 μ m AMI process through MOSIS.

Table of Contents

Chapter 1 – Introduction to the HotSpotter Project	1
1.1 Portable Radiation Detectors	1
1.1.1 Overview	1
1.1.2 Analog Signal Processing for Particle Detection	1
1.2 B-10 Detector Development	4
1.2.1 B-10 Version 1 Prototype	4
1.2.2 Analog Signal Processing for Particle Detection	5
1.3 Introduction to the HotSpotter	6
1.3.1 HotSpotter Overview	6
1.3.2 Pulse Height Analysis	7
1.4 Scope of Thesis	9
Chapter 2 – Gamma Ray Spectroscopy Systems	12
2.1 Introduction to Nuclear Spectroscopy	12
2.2 Building Blocks of a Gamma Ray Spectroscopy System	12
2.2.1 Scintillator	13
2.2.2 Photomultiplier Tubes	15
2.2.2.1 Function of Photomultiplier Tube	15
2.2.2.2 Photocathode	17
2.2.2.3 Dynodes	17
2.2.2.4 Circuit Model of the Photomultiplier Tube	18
2.2.2.5 Noise in Photomultiplier Tubes	21
2.2.3 Analog Electronics	22
2.2.4 Digital Signal Processing Electronics	24
2.3 Limitations of Pulse Height Analysis	26
Chapter 3 – CMOS Peak Detect and Hold Circuit Design	29
3.1 Peak Detect and Hold Circuit Operation	29
3.2 PDH Topology Selection	29
3.2.1 Candidate Topologies	29
3.2.2 Core PDH Circuit Used in the HotSpotter	35
3.3 PDH System Operation	36
3.4 PDH Ancillary Circuits	38
3.4.1 Linear Gate	38
3.4.2 PDH Enable Design	40
3.4.3 Peak Ready Design	42
3.4.3.1 First Implementation of Peak Ready Block	42
3.4.3.2 Second Implementation of Peak Ready Block	43
3.5 Design and Analysis of the PDH Circuit	45
3.5.1 Stability Analysis	46
3.5.2 Offset Analysis	51
3.5.3 Charge Injection	54

3.5.4 Slew Rate	57
3.5.5 Droop Rate	59
3.6 PDH Test Circuit	61
3.7 Summary of PDH Circuit Analysis	62
Chapter 4 – Layout and Simulation	63
4.1 Tools and Technology	63
4.2 Layout	63
4.2.1 PMT Channel	63
4.2.2 PDH System Layout	65
4.2.3 Peak Ready Comparator	66
4.2.4 PDH Circuit	67
4.3 System Simulation	69
Chapter 5 – Experimental Results	71
5.1 Test Setup	71
5.2 PDH Operation	74
5.3 Small Signal Results	76
5.4 Slew Rate Results	77
5.5 Offset Voltage and Charge Injection	79
5.6 Hold Capacitor Voltage Droop	81
5.7 Linearity	83
5.8 Pedestal Measurement and Dynamic Range	86
5.9 Analog Channel Test	87
5.10 Summary of Experimental Results	88
Chapter 6 – Conclusion	90
6.1 Summary	90
6.2 Future Work	91
6.2.1 PDH Circuit	91
6.2.2 Analog Channel	92
6.2.3 System	92
References	94
Appendices	98
Appendix A. MOSIS Process Parameters Used in Pre-fabrication Design	99
Appendix B. MOSIS Process Parameters from Prototype Chip Run (N97N)	103
Appendix C. SPICE Source Code and PDH Magic Extraction Files Used in HotSpotter Simulations	109
Vita	120

List of Figures

Figure 1.1. Analog signal processing chain of a radiation detection instrument.....	2
Figure 1.2. NIM rack and NIM modules with an HP calculator as a reference.....	3
Figure 1.3. B-10 signal processing block diagram.....	4
Figure 1.4. B-10 Thermal Neutron Detector: (a) end view and (b) internal view with an HP calculator as a reference.....	6
Figure 1.5. Pulse Height Spectroscopy signal processing channel. The box outlines the blocks included on the ASIC fabricated for the HotSpotter's PMT channel.....	7
Figure 2.1. Gamma-Ray Spectroscopy Channel with the sub-blocks that make up the analog electronics highlighted.	13
Figure 2.2. Decay scheme for a common gamma reference source showing major energy transitions [2].	14
Figure 2.3. Illustration of the gamma ray and scintillator interaction.....	14
Figure 2.4. Diagram of a linearly focussed photomultiplier tube [19].....	16
Figure 2.5. Illustration of the dynode amplification scheme. A PMT is typically composed of ten or more of these dynode stages with high voltage between each stage.	18
Figure 2.6. PMT biasing circuit with the Anode at ground potential and the Cathode at negative High Voltage. Note that the Cathode could be placed at ground potential and the Anode at positive High Voltage.....	19
Figure 2.7. (a) Scintillator light output. Anode output with (b) large R_a (c) small R_a	20
Figure 2.8. PMT spectra for a ^{22}Na source obtained with NIM test equipment and a PC based MCA. The Compton effect and the Noise floor are also illustrated.	25
Figure 2.9. Illustration of (a) the histogram resulting from (b) pulses riding on top of noise [3].	27

Figure 3.1. Classical discrete implementation of a PDH circuit [10].	30
Figure 3.2. CMOS implementation of classic PDH topology [8].	31
Figure 3.3. PDH implementation using a switched capacitor approach [8].	32
Figure 3.4. PDH implemented with a rectifying current mirror [12].	33
Figure 3.5. PDH topology using a modified CMOS two stage operational amplifier [14].	34
Figure 3.6. Schematic of PDH circuit used in HotSpotter pulse spectroscopy channel.	35
Figure 3.7. HotSpotter Peak Detect and Hold System Block Diagram.	37
Figure 3.8. PDH system timing diagram [26].	37
Figure 3.9. Linear Gate schematic.	38
Figure 3.10. Hand calculated series resistance of Linear Gate.	40
Figure 3.11. PDH Enable comparator Schematic.	41
Figure 3.12. Version 1 schematic of the Peak Ready block.	42
Figure 3.13. Second implementation of the Peak Ready block.	44
Figure 3.14. Hand calculated loop transmission for (a) $I_{d5} = 8 \mu\text{A}$ and (b) $I_{d5} = 0.1 \mu\text{A}$.	48
Figure 3.15. HSPICE simulation of loop transmission with (a) $I_{d5} = 8 \mu\text{A}$ and (b) $I_{d5} = 0.1 \mu\text{A}$.	49
Figure 3.16. Circuit model of the PDH circuit under balanced condition where balanced means that the output voltage is exactly equal to the input voltage.	52
Figure 3.17. Illustration of critical nodes of the PDH circuit during a switching transient when a peak voltage is reached.	55
Figure 3.18. HSPICE simulation showing the switching characteristics of node 2 and 3 of the PDH circuit when a peak is detected.	56

Figure 3.19. Comparison of hand calculated offset voltage with HSPICE results.	58
Figure 3.20. Illustration of offset and charge injection errors that occur when a peak is detected.	58
Figure 3.21. HSPICE simulation of SR versus input voltage magnitude.	59
Figure 3.22. Illustration of the reverse biased p-n junctions at the output node during the hold operation of the PDH circuit.	60
Figure 3.23. PDH test circuit with source follower output stage included for driving off chip.	61
Figure 4.1. Magic layout of the PMT channel prototype chip.	64
Figure 4.2. Photograph of PMT channel prototype chip.	64
Figure 4.3. Magic layout of the PDH block.	65
Figure 4.4. Magic layout of the Peak Ready circuit.	66
Figure 4.5. Magic layout of the PDH circuit.	68
Figure 4.6. Magic layout of PDH test circuit.	68
Figure 4.7. Simulation of PDH test circuit operation.	68
Figure 4.8. Post Layout simulation of PDH system illustrating the operation of the shaper and PDH of the PMT channel.	70
Figure 5.1. ASIC prototype test board.	72
Figure 5.2. Test circuit schematic.	72
Figure 5.3. Automated test setup used to characterize the PDH test circuit and the PMT channel.	73
Figure 5.4. PDH test circuit response to the analog channel shaper output.	75
Figure 5.5. PDH circuit response (channel 1) and Pk_Ready (channel 2) illustrating that the PDH system is functioning properly.	75

Figure 5.6. PDH test circuit response (channel 2) to a 160 mV step input (channel 1).	76
Figure 5.7. Plot of SR versus input voltage magnitude for the PDH test circuit.	78
Figure 5.8. Slew rate measurement of the PDH test circuit for a large input signal.	78
Figure 5.9. Plot of offset voltage versus PDH bias current comparing the hand calculated offset, HSPICE simulated offset, and experimentally measured offset voltages.	80
Figure 5.10. Comparison of the response of the PDH test circuit (channel 1) and the PDH circuit within the PMT channel (channel 2) to the same shaper output pulse.	81
Figure 5.11. PDH test circuit output illustrating the hold voltage droop for a 600 mV output signal.	82
Figure 5.12. Plot of experimentally measured voltage droop versus output signal amplitude.	82
Figure 5.13. PDH test circuit's output voltage versus input voltage with a straight-line reference.	85
Figure 5.14. INL measurement of PDH test circuit with and without the cascode transistor.	86
Figure 5.15. PMT spectra for a ^{22}Na source obtained with the prototype analog channel and the test setup.	88

List of Tables

Table 1.1. Summary of PDH design specifications.....	11
Table 3.1. Summary of components in PDH circuit loop transmission.....	47
Table 3.2. Comparison of hand calculated and simulated loop transmission.	49
Table 5.1. Summary and comparison of hand calculations, HSPICE simulations, and experimental measurements to the PDH circuit's design specifications.....	89

CHAPTER 1

Introduction to the HotSpotter Project

1.1 Portable Radiation Detectors

1.1.1 Overview

Inexpensive, portable radiation detection devices are under development at the Oak Ridge National Laboratory (ORNL). For portability, the critical constraints placed on the instruments are package size, power consumption, cost, and functionality. The package size must be small, similar to a pocket calculator or cellular telephone. The power consumption must be minimized to extend the operating life of the batteries, and, because the instrument may be mass produced, cost must be minimized. Finally, the instrument must satisfy the functionality prescribed by the customer under laboratory or field conditions.

1.1.2 Analog Signal Processing for Particle Detection

At ORNL, the portable detector development focuses on the signal processing electronics, and this thesis will focus primarily on the analog signal processing channel while providing a brief discussion of the detector and digital signal processing (DSP) in order to set the context for the analog electronics design considerations. For a typical radiation detection system, the analog electronics channel will resemble the block diagram shown in Figure 1.1 [1-3]. The detector performs the function of a transducer in that it takes the particle or energy of interest and converts it into a pulse of current that can be electronically processed. In some applications, the detector output can be very

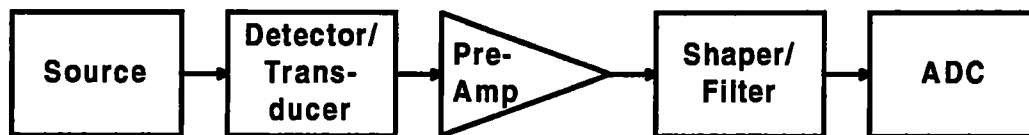


Figure 1.1. Analog signal processing chain of a radiation detection instrument.

small, about tens of thousands of electrons. Thus, a low noise, high gain preamplifier is required to amplify the signal with a minimal reduction in the signal-to-noise ratio (SNR). The shaper block then filters and amplifies the preamplifier output further while shaping the signal into a form that maximizes the SNR. Typically, the output of the shaper will be either a bipolar or a semi-Gaussian voltage pulse [1]. Finally, the analog-to-digital converter (ADC) interfaces the analog electronics to the DSP electronics. The ADC block could be as simple as a threshold comparator in counting applications or it could be a twelve bit ADC in energy measurement applications. Other circuits such as a baseline restorer or pulse pile-up rejector may be present in the analog chain, but they are not required for all applications and will not be investigated further in this thesis [1].

In the past, the electronics making up the blocks of Figure 1.1 were implemented in discrete designs that required significant power consumption and space. One example of popular discrete designs is NIM modules used in laboratories for experimental study. NIM amplifiers provide very good performance and versatility, but they are bulky and consume a significant amount of power [2]. In the laboratory where only one or two channels of electronics are required, power consumption and size are not critical. Figure 1.2 shows a photograph of a NIM bin containing several NIM modules. Each module

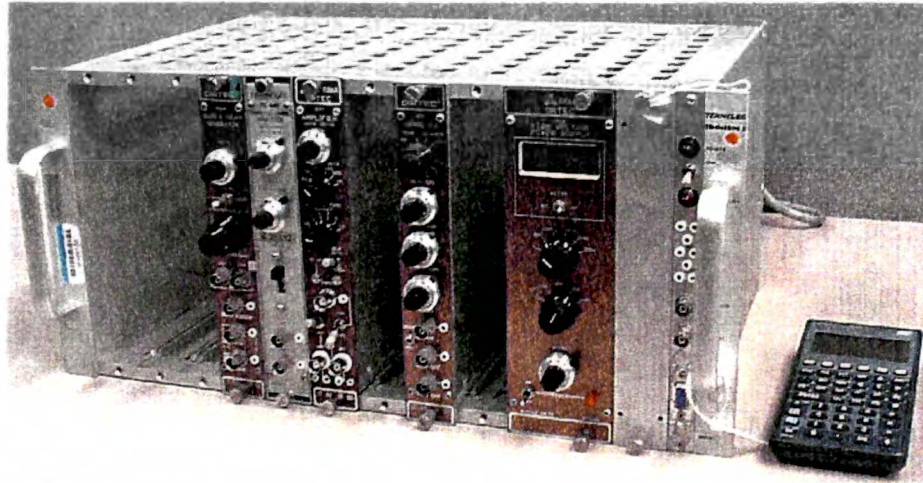


Figure 1.2. NIM rack and NIM modules with an HP calculator as a reference.

performs a single function such as a shaper amplifier. The NIM modules plug into slots contained in the bin and are interchangeable, and the large bin supplies regulated power to each module. An HP pocket calculator has been included to serve as a reference to illustrate that NIM modules are not practical for low power, portable solutions, solutions that require multiple channels of electronics, or solutions that may require both portability and multiple channels. One solution for providing multiple channels of electronics that are power and size efficient is the use of an application specific integrated circuit (ASIC) [4]. For example, the circuits shown in Figure 1.1, from the preamplifier to the ADC, can be integrated multiple times onto a single substrate as small as 2 mm^2 . Thus, ASICs allow radiation detection instruments containing multiple signal processing channels to be realized in pocket sized packages.

1.2 B-10 Detector Development

1.2.1 B-10 Version 1 prototype

Presently, a pocket-sized instrument known as the “B-10” detector that detects and counts thermal neutrons has been developed at ORNL [5]. The B-10 detector detects and counts thermal neutrons and stores the counts in non-volatile memory for later retrieval by a personal computer (PC). Since thermal neutrons are a signature of fissile material, the B-10 detector can be used to find radioactive material, or it can be used as a radiation monitor to find leaks in containers where fissile materials are stored. The B-10 detector employs a novel ^{10}B (Boron isotope) coated PIN photodiode developed at ORNL [6]. The ^{10}B -neutron reaction is well known, and, since both products of the ^{10}B -neutron reaction are visible by a PIN photodiode, combining the ^{10}B with a PIN photodiode made a portable instrument possible [6]. The first B-10 prototype contained a single photodiode detector and thus only a single channel of electronics. Figure 1.3 shows a block diagram of the B-10 signal processing channel. When struck by a neutron, the ^{10}B coated PIN photodiode produces a tiny charge proportional to the energy of the incident neutron. The charge is then amplified by the low-noise charge sensitive preamplifier into

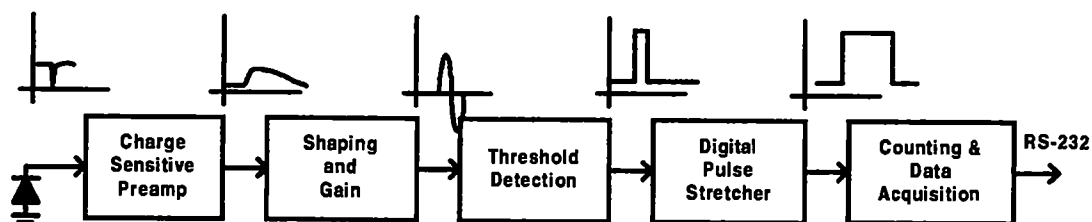


Figure 1.3. B-10 signal processing block diagram.

a voltage pulse resembling a positive step function with a slow decay. The shaper then converts the voltage step into a bipolar shape while adding additional voltage gain. A comparator with an adjustable threshold follows the shaper and produces a time over threshold square pulse that is then stretched to the required width for the μ -controller by a digital pulse stretcher. The μ -controller then processes and stores the counts in non-volatile memory where they can be accessed by a PC via an RS-232 port located on the B-10 instrument.

1.2.2 B-10 Detector Version 2 Prototype

Because the detection efficiency of the B-10 is proportional to the PIN photodiode area, a second version of the B-10 detector was developed that contains four PIN photodiodes. While a single discrete analog channel was used for the first B-10 prototype, the analog electronics for the second prototype were implemented as a multi-channel, CMOS ASIC with four detection channels. The CMOS ASIC allowed circuit board space and power to be conserved, and it also provided the digital logic needed to produce two desired outputs for the digital signal processing to be included on the same substrate.

The CMOS ASIC provides a rugged and inexpensive solution for integrating multiple channels of electronics onto a single, tiny substrate. However, a performance trade-off is made when the analog electronics are implemented in a CMOS process. One trade-off is noise performance compared to discrete designs using low noise JFETs where power consumption is less important [7]. In addition, CMOS amplifiers are slower than amplifiers realized in a similar bipolar technology [8, 9]. However, these trade-offs are

warranted for portability. A picture of the latest prototype is shown in Figure 1.4 (a), and Figure 1.4 (b) shows the B-10 with the same pocket sized HP calculator that was used as a reference in Figure 1.2. Figure 1.4 illustrates that the functionality provided by the bulky NIM modules has been shrunk into a low power, multi-channel, pocket sized instrument.

1.3 Introduction to the HotSpotter

1.3.1 HotSpotter Overview

Successful “Proof of Principle” delivered by the B-10 instrument has led to a project to develop a more advanced portable radiation detection instrument. The new instrument is to combine the neutron counting capabilities of the B-10 Detector with the additional functionality of gamma ray spectroscopy for identifying gamma ray emitting isotopes. Like the B-10 Detector, the new instrument will contain multiple detectors, with at least one detector used for neutron sensitivity and one detector used for gamma



(a)



(b)

Figure 1.4. B-10 Thermal Neutron Detector: (a) end view and (b) internal view with an HP calculator as a reference.

ray sensitivity. Since each detector requires its own analog electronics channel, the analog electronics will again be implemented as a CMOS ASIC to conserve space and power consumption.

1.3.2 Pulse Height Analysis

The addition of the gamma ray spectroscopy channel adds complexity to the analog channel shown in Figure 1.3. Now, instead of doing threshold detection, pulse height analysis must be performed. This means that instead of producing a one bit signal needed simply to count the pulses, a digital word of at least ten bits is needed to represent the precise height of each pulse detected. Figure 1.5 shows the signal processing chain required to do pulse height analysis and the waveform output for each block in the signal chain. Those blocks implemented as an ASIC for the HotSpotter's PMT channel are enclosed within the box indicating the ASIC perimeter.

Because a wide range of energies will be studied by the gamma ray spectroscopy channel, a different detector than that used in the B-10 instrument must be used. Instead of using a PIN photodiode which has no internal gain making detection of energies less than 25 keV difficult, a photomultiplier tube (PMT) which has large internal gain will be

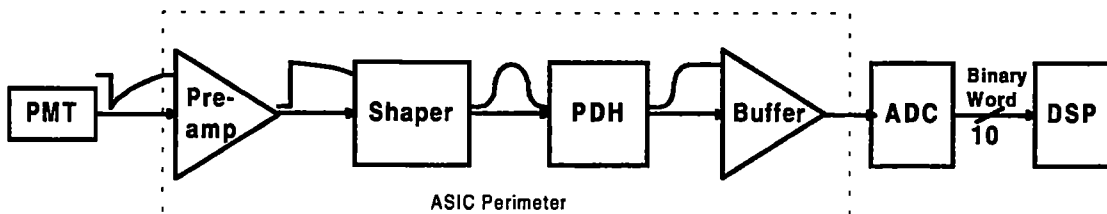


Figure 1.5. Pulse Height Spectroscopy signal processing channel. The box outlines the blocks included on the ASIC fabricated for the HotSpotter's PMT channel.

used. Changing detectors requires a re-design of the preamplifier and shaper blocks from those used in the PIN photodiode channel. In fact, because the PMT provides large amplification, it simplifies the design of the preamplifier, and reduces the amount of voltage gain that the shaper must provide. However, the PMT complicates the system design because it requires a high voltage supply and consumes more power than the PIN photodiode, but a trade-off must be made to meet the performance requirements.

Another change is that the shaper now produces a semi-Gaussian shaped pulse rather than a bipolar shaped pulse. The bipolar pulse is centered around zero and does not cause a baseline shift at high count rates when the blocks shown in Figure 1.5 are capacitively coupled, but the semi-Gaussian shaped pulse provides better SNR performance than a bipolar shaped pulse [1]. If a semi-Gaussian pulse is passed through a capacitor, then the baseline will shift, and a baseline restore circuit is required in the system shown in Figure 1.5. To avoid the need for the baseline restorer and the resulting signal degradation, the analog blocks were *dc* coupled [1].

The spectroscopy channel also requires the addition of the Peak Detect and Hold (PDH) circuit and the ADC to the blocks shown in Figure 1.3. The PDH circuit samples the peak of the semi-Gaussian pulse and holds it until the ADC finishes its conversion. The PDH is a special case of a sample-and-hold circuit that is necessary because the occurrence of the pulses is asynchronous and accurate sampling of the peak is crucial for spectroscopy because the peak height of the pulse is proportional to the incident gamma ray energy. The ADC then converts the voltage peak held by the PDH into a digital word that can be processed by the DSP electronics. The DSP block histograms the outputs of

the ADC for a specified increment of time and then uses the results to determine the gamma ray emitting isotope.

1.4 Scope of Thesis

This thesis will focus in on the design and development of the CMOS PDH circuit that will sample and hold the shaper output at an accuracy that is sufficient to perform gamma ray spectroscopy for a hand held instrument. PDH circuits are an integral block in many gamma ray spectroscopy systems, and a detailed overview of the PDH circuit development will be presented in Chapter 3. However, a discussion of the PDH function within nuclear systems can be found in [1] while further discussion of candidate PDH circuit designs can be found in [10-14].

In order to achieve an adequate design, several specifications must be satisfied by the analog signal processing channel which includes the PDH. First, an energy range of 10 keV to 1.1 MeV must be detected. This means that the PDH must perform over a range of at least 100 to 1. For example, if the minimum input energy of 10 keV corresponds to a 20 mV shaper output then the maximum input energy of 1.1 MeV will correspond to a 2 V shaper output. Thus, the PDH will need to detect a signal as small as 20 mV and a signal as large as 2 V.

The second specification that must be met is speed. The PDH must have sufficient bandwidth and slew rate to follow the output of the shaper over the full voltage range. For this application, the time constant of the shaper is set at 2 μ s. Thus, the PDH must have a slew rate greater than 1 V/ μ s. The third specification is the PDH hold time,

and it is dependent upon the ADC conversion time and on the μ -processor speed. The hold time is defined as the length of time that the PDH can hold the peak voltage without droop due to leakage currents. For this application, the PDH must hold the signal for at least 10 μ s at an accuracy of at least 10 bits. The final, and most important, specification is that the PDH output must be linear over the entire voltage range with maximum deviation of 0.1% at each point along an ideal straight line output in order to achieve a minimum of ten bits of accuracy.

Several issues can cause non-linearity in the PDH [8]. Errors due to droop and slewing have already been discussed above. Another major source of error arises due to pedestals. A pedestal is a small error voltage upon which the real signal rides, and it causes the sampled peak of the PDH to be greater than or less than the actual peak [8]. Two design considerations arise when dealing with the pedestal. First, the pedestal must be minimized because it defines the smallest voltage that can be detected by the PDH. Secondly, if the pedestal remains constant over the entire dynamic range, then it will not affect the linearity of the PDH, and it can be subtracted by the DSP. Because a feedback configuration will be used to implement the PDH, other issues such as stability against oscillations and overshoot must also be addressed. Table 1.1 summarizes the design specifications that must be met by the PDH circuit.

Along with an in-depth analysis of the PDH mentioned above, this document contains an overview of nuclear pulse spectroscopy systems with emphasis on the specific blocks used in the HotSpotter's signal processing channel in Chapter 2. Chapter 3 gives a detailed analysis of the PDH circuit design while Chapter 4 contains the Magic

Table 1.1. Summary of PDH design specifications.

Parameter	Specification
Dynamic Range	100:1
Bandwidth	1.1 MHz
Phase Margin	65°
Slew Rate	1 V/ μ s
Pedestal	1.2 mV
Droop	10 μ V/ μ s
INL	0.10%
Power Consumpti	200 μ W

layout and HSPICE system simulation results. The experimental test results of the PDH circuit are presented and compared with the hand calculations and HSPICE simulations in Chapter 5. Finally, Chapter 6 contains the conclusion and suggestions for further investigation.

CHAPTER 2

Gamma Ray Spectroscopy Systems

2.1 Introduction to Nuclear Spectroscopy

Nuclear spectroscopy systems detect and measure the energy of atomic particles in order to identify the source of the radiation [1, 2]. When a radioisotope decays, it produces alpha particles, beta particles, neutrons, x-rays, and gamma rays. Here, gamma rays are of particular interest because they can provide a characteristic signature which may be used to identify a given radioisotope.

Gamma ray spectroscopy systems detect multiple gamma rays, measure their energy, and then build a histogram of the detected energies. Various methods have been developed to perform gamma ray spectroscopy [15-17]. The instrumentation ranges from large PC sized products [16] to bulky, bench-top equipment such as NIM modules [2] to hand held detectors [18]. The building blocks of most classical gamma ray spectroscopy systems are similar to those shown in Figure 2.1. This chapter reviews the fundamental components used to implement each block in order to realize a spectroscopy system similar to that used in the HotSpotter.

2.2 Building Blocks of a Gamma Ray Spectroscopy System

A gamma ray is a high energy photon that is emitted when a nucleus decays from a higher energy state to a lower energy state. The emitted photon's energy is approximately proportional to the difference between the two energy states [2]. Figure

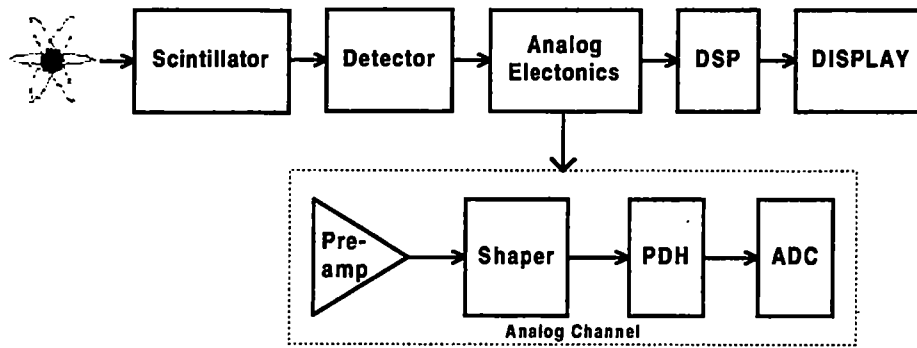


Figure 2.1. Gamma-Ray Spectroscopy Channel with the sub-blocks that make up the analog electronics highlighted.

2.2 shows an energy diagram of ^{22}Na , a common gamma ray reference source [2]. This diagram illustrates the emission of a 1.274 MeV gamma ray as it decays.

2.2.1 Scintillator

Since gamma rays are a form of electromagnetic energy, they must be converted into an energy form that can be processed by the analog electronics. One common method for converting energy is to couple a scintillator to a semiconductor detector or to a photo-multiplier tube (PMT). Numerous materials can be used as scintillators. Typically, the application dictates which type of scintillator will be most effective based on properties such as atomic number or stopping power, light output, wavelength, decay time, efficiency, and linearity [2].

Figure 2.3 illustrates the gamma ray and scintillator interaction. Light is produced when the incident gamma enters the scintillator and collides with a valence electron. There are actually three ways in which gammas lose energy: the photoelectric effect, the Compton effect, and pair production, but the two modes of importance here are the photoelectric effect and the Compton effect [2]. Photoelectric absorption occurs when

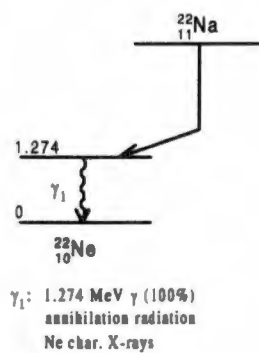


Figure 2.2. Decay scheme for a common gamma reference source showing major energy transitions [2].

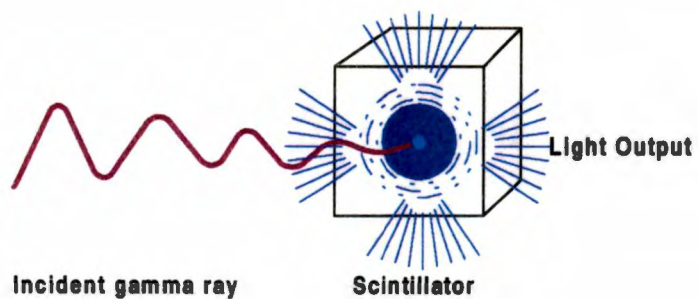


Figure 2.3. Illustration of the gamma ray and scintillator interaction.

the energy of the gamma is high enough to cause a state change by the electron. Thus, upon collision the electron will absorb the incident gamma's energy and jump to the conduction band resulting in the creation of an electron-hole pair. As the excited electron loses energy and eventually recombines, a photon is produced.

While the photoelectric effect produces photons at a specific energy, the Compton effect produces photons at over a range of energies extending from nearly zero up to a maximum possible energy. The Compton effect results from gamma ray / electron interactions where only a portion of the gamma's energy is absorbed by the electron while the photon is scattered to collide with another electron. The partial absorption causes the energy spread of the emitted photons. In both effects, however, photons in the visible range usually around the blue region and sometime in the ultraviolet region are produced. It is also of interest to note that different scintillators have different decay times and different speeds. The decay time refers to the amount of time it takes for all of the visible light to dissipate after being struck by a gamma, and speed refers to the amount of delay between a gamma ray interaction and the production of visible light. Both of these properties play a part in signal processing chain.

2.2.2 Photomultiplier Tubes

2.2.2.1 Function of the Photomultiplier Tube

Once gamma ray energy has been converted to visible light, a detector is required to convert the light input into a signal output that can be processed by the analog electronics. The light intensity from the scintillator can be very weak at lower energies; thus, a very sensitive detector is required. The most commonly used detector in scintillation counters is the photomultiplier tube (PMT) [2].

PMT's are popular detectors for gamma-ray spectroscopy, but have portability drawbacks due to their high voltage power supply, power consumption, fragility, and cost [18]. Semiconductor detectors offer a good alternative for portability and cost but lack in noise performance due to the increased detection area for adequate sensitivity [2, 18]. Semiconductor detectors also have poorer performance at lower energy measurements. Although PMT's consume more space and power than semiconductor detectors, they simplify the analog electronics by providing significant gain for the signal.

Figure 2.4 shows that a PMT is composed of a photocathode followed by several dynodes or amplification stages followed by a collector or anode, and all the components are enclosed in a vacuum. The dynodes can be arranged in several different geometries. The arrangement shown in Figure 2.4 is called the linear focussed type, and this is the arrangement upon which the following discussion will focus.

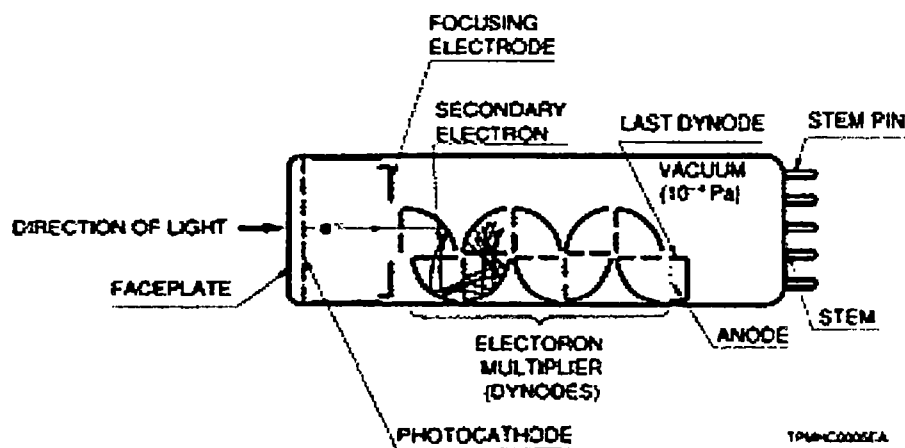


Figure 2.4. Diagram of a linearly focussed photomultiplier tube [19].

2.2.2.2 *Photocathode*

A commonly used photocathode is composed of 'bialkali' (K_2CsSb) [3], which is a semi-transparent material that converts the visible light into a proportional number of electrons. Because the visible light has a relatively low energy, special processing steps must be taken to lower the work function of the cathode to a level that will allow a high number of electrons to escape into free space. The energy difference between free space and the conduction band is called the work function. Quantum Efficiency (QE) defines the number of electrons produced by the incident photons and is expressed as

$$QE = \frac{\# \text{ of Photoelectrons}}{\# \text{ of Photons}} \times 100(\%) \quad (2.1)$$

where a QE of 30% is typical [3]. The transparent material used at the cathode end of the PMT also plays a significant role in the QE , and it usually sets the limit on the smallest wavelength that can be detected. This lower limit results from the fact that the energy of the gamma ray is inversely proportional to its wavelength. Thus, the photon energy increases with decreasing wavelength, and as the energy increases, the distance the photon travels in a particular medium before being absorbed typically decreases [3]. Often, a plot of the QE for cathode will be included with the PMT's datasheets [19].

2.2.2.3 *Dynodes*

The focusing electrodes shown in Figure 2.4 guide the photoelectrons toward the first dynode. The photoelectrons strike the first dynode causing secondary electrons to be released. The dynodes are typically made from the same material as the photocathode [3]. Because the dynodes are biased at successively higher voltages, an electric field exists between each stage. Figure 2.5 shows the orientation of the field between two

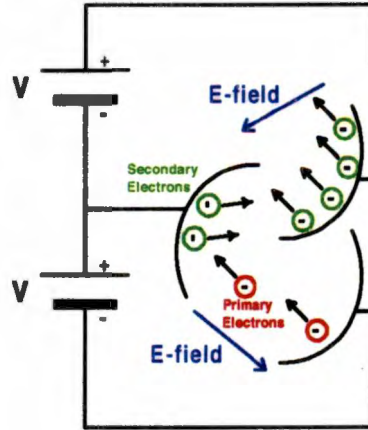


Figure 2.5. Illustration of the dynode amplification scheme. A PMT is typically composed of ten or more of these dynode stages with high voltage between each stage.

successive dynodes. Due to the large voltage bias (V), the electrons are accelerated toward the next dynode in the chain. The primary electrons then collide with the next dynode, and a higher number of secondary electrons are released. Thus, the gain of each dynode (δ) is defined as the number of secondary electrons produced for each primary electron. Typically, δ is between three and four [2]. Thus, if there are n dynode stages, then the gain of the PMT (M) can be expressed as

$$M = C\delta^n \quad (2.2)$$

where C is the fraction of all photoelectrons collected by the multiplier source [2]. Typically, there are nine or more dynode stages resulting in a PMT gain of 10^6 or greater.

2.2.2.4 *Circuit Model of the Photomultiplier Tube*

Figure 2.6 shows the circuit model for the PMT where D denotes a dynode and C_i is the total capacitance at the anode including parasitics. The resistor divider network sets the bias for the cathode and each dynode. Typically, the resistors between each

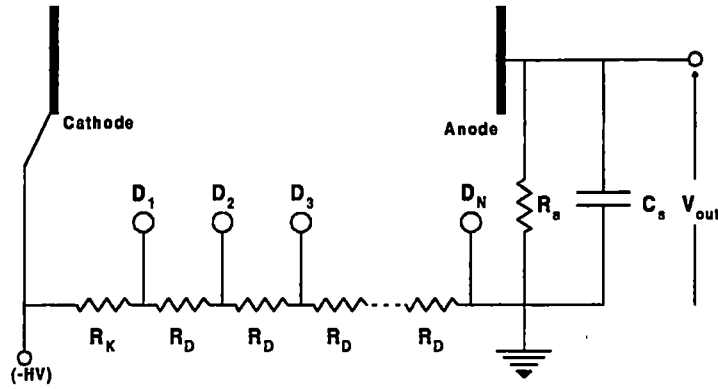


Figure 2.6. PMT biasing circuit with the Anode at ground potential and the Cathode at negative High Voltage. Note that the Cathode could be placed at ground potential and the Anode at positive High Voltage.

dynode (R_D) are equal while the resistor between $D1$ and the Cathode (R_K) is larger to increase the voltage drop between $D1$ and the cathode and, therefore, improve the collection efficiency of the photoelectrons. The cathode can be placed either at the negative voltage with the anode at ground potential, or the cathode can be placed at ground potential with the anode at positive high voltage.

The gain of the PMT also varies significantly with changes in High Voltage (HV) because increasing or decreasing the HV will increase or decrease the electric field between each dynode [2]. Therefore, a stable and very low ripple voltage supply is required for good PMT performance because any voltage ripple that occurs early in the dynode chain will be multiplied by the gain of the remaining dynode stages and could result in large noise signals at the anode.

The PMT output voltage ($v_a(t)$) is dependent upon the $R_a C_s$ time constant of the circuit in Figure 2.6. If C_s is assumed to be constant, then two cases for $v_a(t)$ emerge: one due to large R_a and one due to small R_a [2]. Figure 2.7 (a) illustrates that the light output of the scintillator decays exponentially with the time constant τ_s that can range

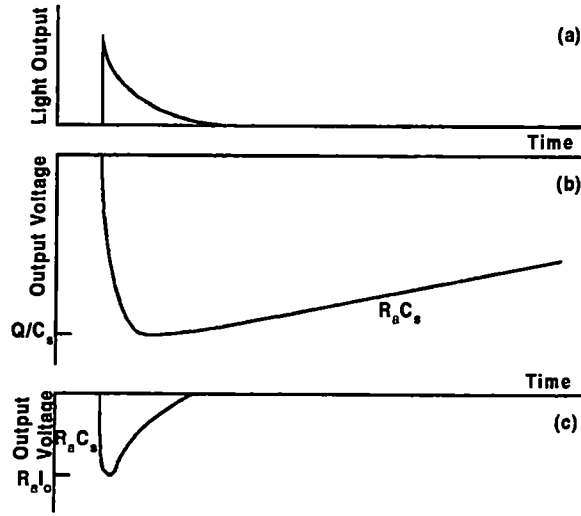


Figure 2.7. (a) Scintillator light output. Anode output with (b) large R_a (c) small R_a .

from a few nanoseconds to a few microseconds for different materials. If the transit time through the PMT is small compared to τ_s , then the resulting current flow induced in the anode ($i_a(t)$) of the PMT is expressed as

$$i_a(t) = I_o \exp(-t/\tau_s), \quad (2.3)$$

where I_o is the initial PMT current. If the value of R_a is large, the anode voltage ($V_a(t)$) equals

$$V_a(t) = \frac{Q_a}{C_s} e^{-t/R_a C_s}, \quad (2.4)$$

where Q_a is the total charge at the anode found by integrating equation 2.3. Figure 2.7 (b) shows that the resulting anode voltage waveform for this mode. It has a negative magnitude because the current flows from anode to cathode, and the fall time is set by τ_s while the rise time is set by the $R_a C_s$ time constant. The voltage only reaches its

maximum amplitude (Q_a/C_s) if the $R_a C_s$ time constant is much larger than τ_s so that all of the charge gets integrated onto C_s .

The second case is where R_a is small so that $R_a C_s \ll \tau_s$, and Figure 2.7 (c) shows the resulting anode output. Since R_a is small, and the current $i_a(t)$ now flows through R_a , and the maximum anode voltage will be small ($\sim R_a I_o$). In both cases, the anode voltage will be proportional to the incident light's intensity, but the second case will be more sensitive to noise because the output voltage is smaller [2]. However, the second case is valuable in applications where high count rates are expected.

2.2.2.5 *Noise in Photomultiplier Tubes*

The PMT does present some non-idealities to the signal processing chain that degrade the SNR. The non-idealities are unwanted, random fluctuations in the PMT signal that are commonly referred to as noise. The noise sources of the PMT are classified as: dark current, Johnson noise, and shot noise. Dark current is defined as the current that flows when the PMT is in complete darkness, and it is a figure typically quoted in datasheets because the dark current sets the minimum detectable signal. The Dark current results from thermionic emissions and is therefore temperature dependent. The dark current (i_d) can be expressed as

$$i_d = aA_{cath}T^2 \exp\left(-\frac{e\phi}{kT}\right), \quad (2.5)$$

where A_{cath} is the cathode area, T is temperature, e is the electron charge, ϕ is the work function, k is Boltzman's constant, and a is a constant for pure metals [20]. Equation 2.5 shows that the dark current can be reduced by reducing the Temperature, and this is done in applications where extremely small signals must be detected. Shot noise results from

the random emission of each electron between dynode stages. Johnson or thermal noise appears across the load resistor at the anode, and it is typically smaller than the dark current shot noise [20].

The noise source that typically dominates peak broadening in the system output energy spectrum is due to Poisson statistics of primary photoelectron production that occurs at the first stage of the PMT [2]. This means that the number of photoelectrons produced (N) will have a standard deviation of $\sigma = \sqrt{N}$. The resolution of the spectroscopy system is defined as E_{FWHM}/E_{peak} . Since the average pulse height (E_{peak}) is proportional to the gamma ray photon's energy, then the maximum resolution (R) can be defined as

$$R = \frac{E_{FWHM}}{E_{peak}} = \frac{\sqrt{N}}{N} = \frac{K\sqrt{E}}{E} = \frac{K}{\sqrt{E}}, \quad (2.6)$$

where K is a constant of proportionality relating the energy to the number of photoelectrons [2].

Although it is not considered a noise signal, PMTs are susceptible to magnetic fields. Magnetic fields can alter the flight trajectories of the electrons between dynodes resulting in gain fluctuations. Therefore, the PMT must be equipped with proper shielding if it is to be used in an area containing high magnetic fields. Despite these non-idealities, the PMT serves as an excellent detector for gamma ray spectroscopy systems.

2.2.3 Analog Electronics

Figure 2.1 shows that the output of the PMT is then processed by the analog electronics. In many radiation detectors, the output is a tiny charge pulse that requires amplification with minimal distortion by the preamplifier before it can be further

processed and analyzed [21,22]. The preamplifier presents a high impedance to the detector and a low impedance to the pulse-processing electronics. The charge sensitive preamplifier typically has a fast rise time and a slow decay time to ensure that all of the charge from the detector is collected [2, 22]. Since the PMT provides large internal gain, a large amplification stage is not always required. Instead, the preamplifier topology is dependent upon the output voltage characteristic of the PMT. If the PMT does not develop a voltage at the anode internally, then a transimpedance preamplifier is required to convert the PMT current into a voltage.

The shaper provides additional amplification while improving the signal-to-noise ratio (SNR) of the system. The shaper output voltage pulse typically approaches a semi-Gaussian shape because that shape offers the best practical SNR performance. The semi-Gaussian shape is typically realized by cascading several stages of integration with the same time constant [2]. The shaper's time constant affects several aspects of the spectroscopy system. The first is the SNR. Often, the optimum time constant for a detector is found experimentally by measuring the detector's resolution over a range of time constants. An optimum time constant will then emerge where the SNR is at a maximum [2]. The time constant also sets the rate at which the shaper output returns to the baseline. Thus, a short time constant results in a fast return to baseline and a reduction in pulse pile-up. However, the optimum return to baseline rate for a particular system often conflicts with optimum noise performance introducing a trade-off that must be made [22].

The shaper's pulse height must also be proportional to the gamma ray's energy in spectroscopy systems. To ensure this, the time constant must be long enough to collect

all charge produced by the preamplifier [22]. Again, this time constant may conflict with that giving optimum SNR. Finally, the semi-Gaussian shape gives a relatively flat peak that can be more accurately sampled by the PDH.

The PDH then samples the peak voltage produced by the shaper and holds it until the ADC can convert the signal. The PDH must sample the pulse peak with greater accuracy than the ADC to ensure that the desired resolution can be achieved. A detailed analysis of the PDH will be presented in the next chapter.

The ADC interfaces the analog electronics to the digital electronics by taking an input voltage that can occur at any point within the dynamic range and converting it to a specific digital code. The digital code length is determined by the precision of the ADC, or the number of bits (b) the ADC produces. The number of bits determines the number of bins into which the voltage range of interest will be divided, and the number of bins is equal to 2^b . The resolution of the ADC is important in gamma ray spectroscopy because it determines the accuracy in which the energy can be measured.

2.2.4 Digital Signal Processing Electronics

The digital electronics take the ADC output and perform the required analysis for spectroscopy, or more specifically, the digital electronics are used to implement a multi-channel analyzer (MCA). Therefore, the digital signal processing (DSP) contains a microprocessor to perform the analysis and memory to store the results. For laboratory experiments and testing, the digital signal processing can be done with a commercial MCA that plugs into a PC [24]. However, for a portable instrument, the DSP electronics must be implemented with an onboard micro-controller, memory, and a readout such as a liquid crystal display.

An MCA detects the peak of the semi-Gaussian pulse produced by the shaping amplifier and held by the peak stretcher and converts it into a digital word [2]. The digital word corresponds to a single bin in a histogram, and when the digital word is detected, the corresponding bin count is incremented by one. Thus, as several pulses of equal height occur, the same bin or channel in the MCA is incremented. Figure 2.8 shows an example spectra for a PMT coupled to an ORTEC 471 shaping amplifier obtained by a PC based MCA (PCA3) manufactured by Oxford Instruments [24]. The x -axis of Figure 2.8 corresponds to the energy range of interest while the y -axis represents the number of counts in each channel. The spectrum also illustrates the Compton effect defined above and the system's noise floor.

Ideally, each bin width is equal so that the probability of a detection occurring for each bin is equal. The total number of bins and the dynamic range of the pulse energies

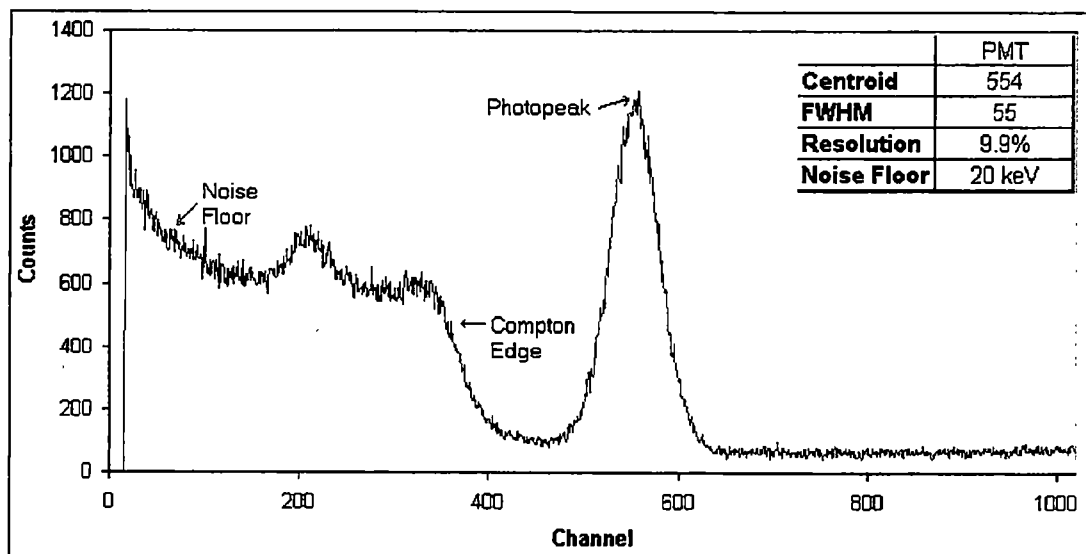


Figure 2.8. PMT spectra for a ^{22}Na source obtained with NIM test equipment and a PC based MCA. The Compton effect and the Noise floor are also illustrated.

affect the maximum resolution of the MCA. For example, if the pulse height can range from 2.5 V to 5.0 V and a 10 bit ADC is used, then each bin width will be $2.5 \text{ V} / 1,024$ giving a quantization uncertainty of 2.5 mV, and a pulse height measurement error of no less than a 0.1 %. This illustration reveals two principles about the spectroscopy system design. The first is that the ADC resolution sets a minimum achievable accuracy of the system so that increasing the accuracy requires more bits of precision. The second is that the system error introduced by the analog electronics should be less than the quantization uncertainty of the ADC.

Another important consideration in pulse height analysis systems is the count rate. The count rate refers to how fast the MCA can sample the peak, process the data, and then sample the next peak. The finite amount of time needed to process each peak, called dead time, will limit the system's throughput [2]. Thus, for spectroscopy systems where the average pulse spacing is less than the dead time, valid events will be lost and statistical corrections must be made to obtain proper spectra [2].

2.3 Limitations of Pulse Height Analysis

Each stage of the gamma ray spectroscopy system shown in Figure 2.1 contributes noise to the signal that results in distortion of the peak and loss of resolution. Ideally, the gamma rays of a particular energy from a particular radioisotope would produce counts in a single channel of the MCA and result in a sharp peak. However, Figure 2.9 (b) illustrates how the noise of the spectroscopy system causes the peak to vary randomly. Since the noise of the spectroscopy system can be modeled as a Gaussian distribution, the pulse height has a Gaussian distribution [1]. Figure 2.9 (a) illustrates

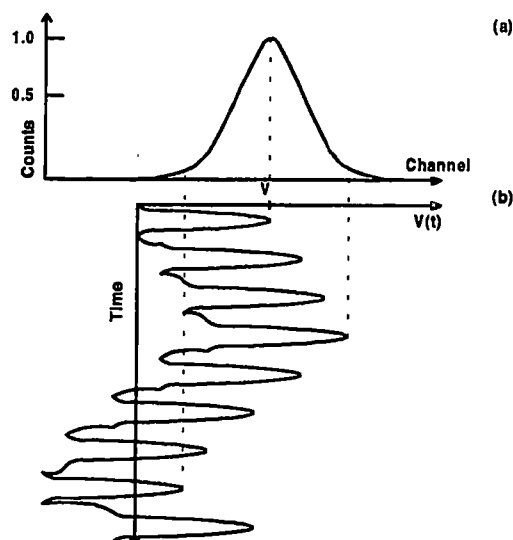


Figure 2.9. Illustration of (a) the histogram resulting from (b) pulses riding on top of noise [3].

that the resulting histogram compiled by the MCA will also have a Gaussian distribution due to the randomness of the pulse peaks [1]. The full width at half max (*FWHM*) of the histogram can be related to the root mean square (r.m.s.) noise of the system by the following relationship

$$\sigma_E = \frac{E_{FWHM}}{2.36} , \quad (2.7)$$

where E_{FWHM} is the FWHM of the energy and σ_E is the r.m.s. noise of the system [1].

Equation 2.6 showed that the PMT noise often dominates the system so σ_E is proportional to $\sqrt{E}$. Thus, Equations 2.6 and 2.7 show that the resolution decreases by the square root of increasing energy.

As the noise of the system increases, the spread around the energy peak widens. This spread is significant because it reduces the resolution of the spectroscopy system

since two closely spaced peaks must be separated by at least their E_{FWHM} in order for their peaks to be resolved.

A description of the blocks used in gamma ray spectroscopy systems has been presented along with an explanation of some system design considerations. Next, Chapter 3 will focus on the design of a PDH circuit, a critical block in the analog electronics.

CHAPTER 3

CMOS Peak Detect and Hold Circuit Design

3.1 Peak Detect and Hold Circuit Operation

Chapter 2 showed that the PDH, or peak stretcher, samples and holds the peak of the semi-Gaussian shaped pulse produced by the shaper until the ADC can convert the signal. Because the peak voltage of the semi-Gaussian shaped pulse is proportional to the incident gamma ray's energy, measuring the peak accurately is critical to perform gamma ray spectroscopy. This makes the PDH circuit a critical block in the analog signal processing channel, and it places stringent requirements on the circuit design. Table 1.1 listed the specifications that the PDH circuit must meet to function within the HotSpotter system, and this chapter presents the analysis of the PDH circuit designed to meet those requirements.

3.2 PDH Topology Selection

3.2.1 Candidate Topologies

The PDH circuit is a specialized form of a sample-and-hold circuit that samples asynchronously rather than at a certain clock frequency. The circuit samples asynchronously because gamma rays are randomly emitted and detected by the spectroscopy system. Thus, the ability to both detect and hold the peak voltage accurately places requirements on the PDH circuit that do not exist for sample-and hold circuits.

The first stage of the PDH circuit design consisted of choosing a topology that would yield the best performance in a CMOS technology. The classical topology used in discrete implementations is shown in Figure 3.1, and this topology gives insight into the principle operation of most PDH circuits [10]. The circuit is configured as a positive rectifying voltage follower where the operational amplifier adjusts its output so that the PDH output voltage is equal to the input. As the input increases, the output voltage follows and charges up the hold capacitor (C_h) until its voltage equals the input voltage. When the input voltage reaches its maximum value and begins to decrease, the output will try to decrease, but it cannot because there is no current path available to discharge C_h . At the point where the input voltage drops below the output voltage, the op amp output voltage will decrease at its slew rate limit and reverse bias D_1 . This negative voltage step causes a charge injection error on C_h , and different techniques used to minimize this and other errors of this circuit have been implemented but are beyond the scope of thesis [10].

Since diodes are not readily available and modeled in a standard CMOS process,

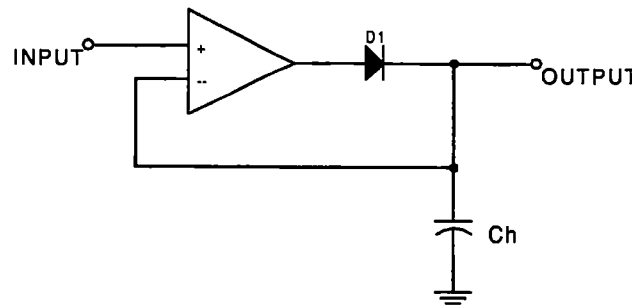


Figure 3.1. Classical discrete implementation of a PDH circuit [10].

the topology presented in Figure 3.1 must be modified to realize a CMOS PDH. By replacing D_I in Figure 3.1 with an NMOS transistor configured as a source follower as shown in Figure 3.2, a CMOS PDH can be realized [8]. This topology was considered for the HotSpotter; however, a couple of non-idealities made it unacceptable. The major problem again is the signal dependent charge injection through C_{gs} that occurs when the circuit goes open loop and the operational amplifier output goes to the lower rail. Another problem with this topology is that its dynamic range is limited to $V_{DD} - V_{GS}$, an undesirable effect in spectroscopy systems.

An alternate implementation that is compatible with CMOS technology is the switched capacitor approach shown in Figure 3.3 [8]. The NMOS transistor acts as a switch controlling the input to C_h and the comparator has a built in latch. This approach offers a high speed solution, but accuracy is sacrificed due to the signal dependent charge injection of the transistor. The latched comparator monitors the voltage difference across the finite channel impedance of the transistor. While the input is increasing, the input

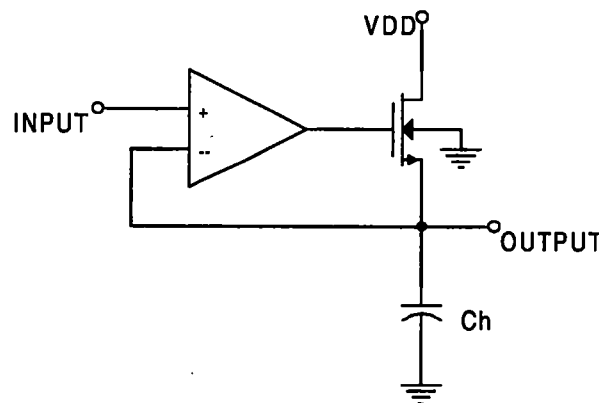


Figure 3.2. CMOS implementation of classic PDH topology [8].

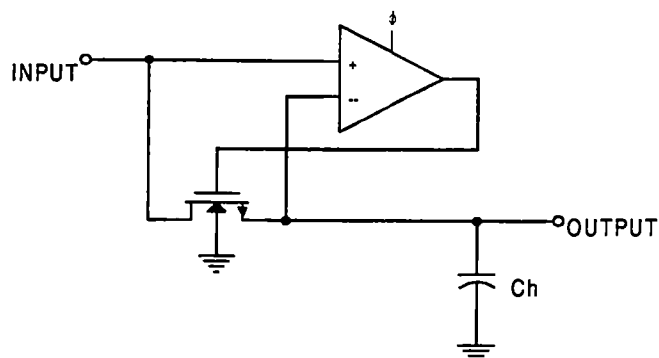


Figure 3.3. PDH implementation using a switched capacitor approach [8].

voltage is slightly greater than the output voltage, and the switch remains closed. When the input decreases and falls slightly below the output voltage, the latched comparator opens the switch and holds the peak voltage on C_h . Thus, this circuit requires a high performance comparator. Even with a good comparator, the signal dependent charge injection of the transistor makes this topology unsuitable for the HotSpotter application.

A fourth topology considered, shown in Figure 3.4, was developed for a CMOS nuclear spectroscopy system [12, 13]. It uses a current mirror to perform the signal rectification, and it can be implemented as either a positive or negative peak stretcher by complementing the transistors. The circuit shown in Figure 3.4 is a negative peak stretcher. When the input decreases, the current output of the differential amplifier increases. This output current is then mirrored to the output by the rectifying current mirror and discharges C_h until the output voltage equals the input voltage. When the input voltage increases, the differential amplifier output decreases and turns the current mirror off. Thus, the peak voltage is held on C_h . Notice that the circuit will again go open loop when the input becomes greater than the output causing the differential amplifier output to switch to ground. Since the output is already near ground,

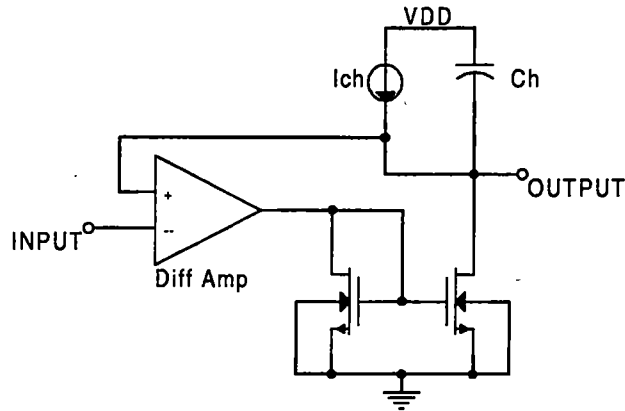


Figure 3.4. PDH implemented with a rectifying current mirror [12].

approximately one V_{GS} above it, then the charge injection inherent in previous topologies is nearly eliminated [12]. Another desirable characteristic of this topology is that the output can be driven all the way to the positive or negative supply rail.

One disadvantage with this topology is that under quiescent conditions, a tiny current must flow through the current mirror to ensure stability [25]. This current is provided by the I_{ch} current source. When a peak is detected, this current source must be disabled or it will cause a droop error [13]. Another possible problem with this topology is speed. For large signals, the maximum current available to charge or discharge C_h is equal to the tail current of the input differential amplifier. When a large negative signal appears at the input of Figure 3.4, then all of the tail current is going to flow into the branch connected to the current mirror. Therefore, only a current equal to or less than the tail current can be mirrored to the output (assuming the mirror devices are of equal size). A final disadvantage is the low loop gain of the circuit which limits the accuracy of detection. However, An integral non-linearity (INL) of 0.16% and a pedestal of 5 mV have been reported for the negative peak stretcher [13].

The final topology investigated is similar to the rectifying current mirror and is shown in Figure 3.5 [14]. It was designed for use as a peak detector in a hard disk drive servo loop. The circuit resembles a two stage operational amplifier connected as a voltage follower except the active load on the common source output stage has been replaced with C_h . This approach offers several advantages over the design shown in Figure 3.4. First, the loop gain has been greatly increased by replacing the current mirror with a common source stage. Secondly, the speed is improved because the output current is no longer limited by the tail current of the input stage. Instead, the current is dynamically controlled by the V_{GS} of M_3 , similar to a Class AB stage. Thus, the output charging current can be quite high under large signal conditions. Charge injection is still minimized because the gate voltage of the output stage is close to the positive supply rail, approximately one V_{GS} down, when the circuit goes open loop. A final advantage is that a bias current is not required to bypass C_h under quiescent conditions.

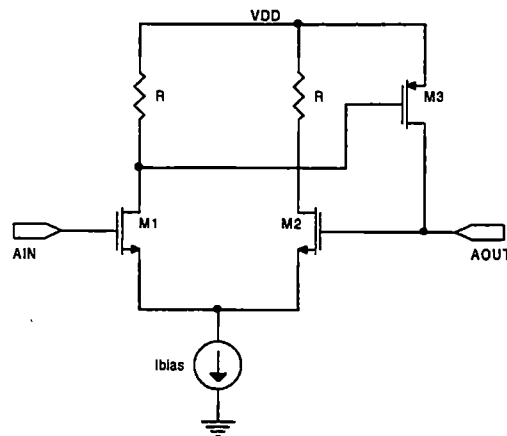


Figure 3.5. PDH topology using a modified CMOS two stage operational amplifier [14].

3.2.2 Core PDH Circuit Used in HotSpotter

The topology presented in Figure 3.5 offered optimum potential performance for the pulse spectroscopy system. It functions at high speeds, it can drive its output to the upper rail in order to maximize dynamic range, it has a large loop gain for high accuracy, and it minimizes charge injection when the circuit goes open loop. Thus, this topology was modified to function as the PDH circuit in the HotSpotter system. Figure 3.6 shows the schematic of the PDH circuit.

The first modification to the circuit shown in Figure 3.5 was replacement of the resistors with an active load. Second, the cascode transistor M_6 was included to boost the loop gain. The third change was the addition of C_h and the reset transistor because the circuit shown in Figure 3.5 was designed to only to detect peaks, not hold them [14]. The large hold capacitance improves the accuracy by reducing droop and charge injection

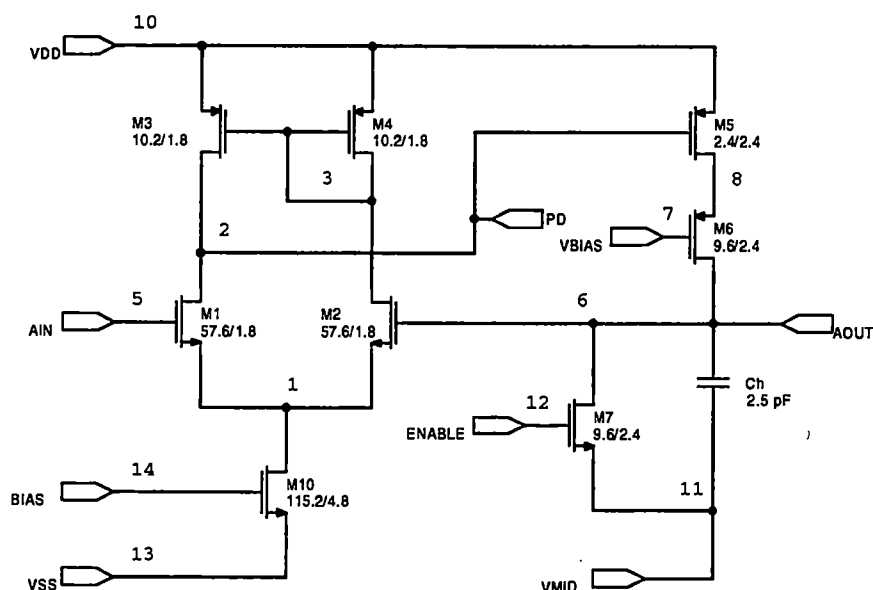


Figure 3.6. Schematic of PDH circuit used in HotSpotter pulse spectroscopy channel.

errors, and the reset switch enables C_h to be reset immediately rather than be discharged by a constant current.

3.3 PDH System Operation

In order for the PDH circuit shown in Figure 3.6 to operate correctly within the HotSpotter system, additional circuit blocks that perform control and logic functions had to be added [25]. The block diagram of the HotSpotter PDH system is shown in Figure 3.7, and the system timing diagram is shown in Figure 3.8 [26]. The timing diagram illustrates the sequence of events that occur when a pulse is detected.

When a gamma ray is detected, the shaper produces the semi-Gaussian shaped pulse labeled *Pulse_In* in Figure 3.8. When the pulse height exceeds the *PDH_En* threshold, then the *PDH_En* signal goes low and enables the PDH to track the input. The *PDH_En* threshold is a DC voltage set externally at a value above the noise floor of the system to ensure that no false peaks are incorrectly detected. The PDH output (*Peak_Out*) follows the pulse to the peak, but as *Pulse_In* decreases, *Peak_Out* remains at the peak value. When a peak has been sampled, the DSP section must be notified that the peak is ready to be processed. A digital pulse called *PK_Ready* is used to perform this task by going high when the ramp voltage *PD_Ramp* exceeds a threshold voltage monitored by a comparator in the Peak Ready block of Figure 3.7.

The *PK_Ready* line also controls the state of the Linear Gate by closing it when a peak is detected so that no additional pulses can be processed. The PDH then waits until

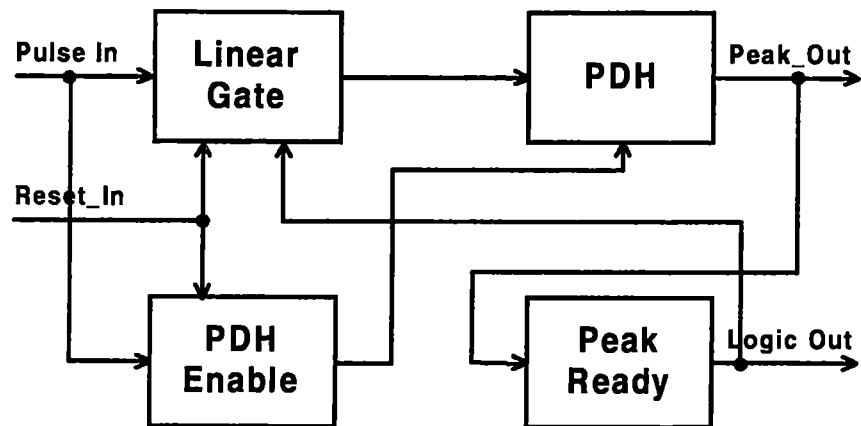


Figure 3.7. HotSpotter Peak Detect and Hold System Block Diagram.

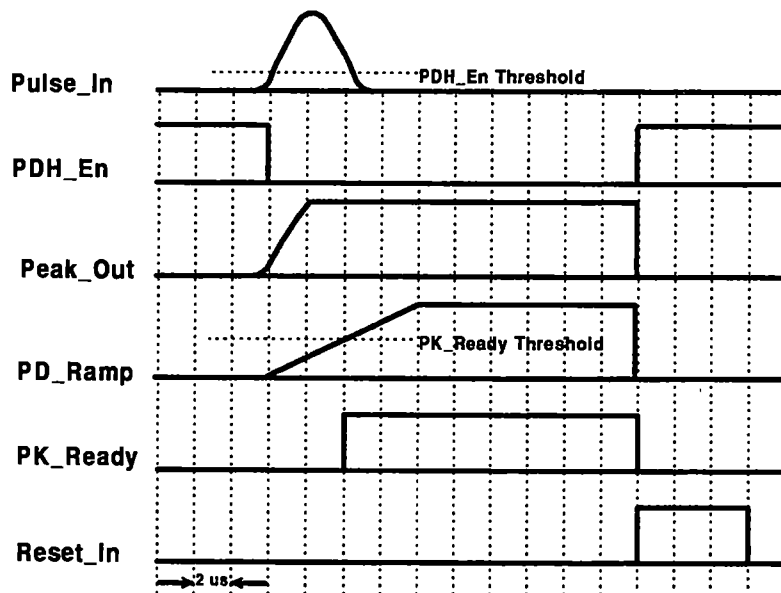


Figure 3.8. PDH system timing diagram [26].

a reset pulse (*Reset_IN*) is given by the DSP. The *Reset_In* pulse resets the signal levels back to their initial states, and the PDH is now ready to process the next pulse.

3.4 PDH Ancillary Circuits

3.4.1 Linear Gate

The Linear Gate is a switched transmission gate that controls the input to the PDH by blocking the PDH input from receiving additional inputs while a sampled pulse is being processed. The schematic of the Linear Gate, shown in Figure 3.9, shows that it is composed of a transmission gate and some digital logic to control the state of the gate. For prototyping purposes, a linear gate enable line (*LGENABLE*) was added to allow the Linear Gate to be enabled or disabled with an external voltage level.

The operation of the Linear Gate is as follows: after a reset, the Linear Gate is open, and *AOUT* is equal to *AIN*. When a pulse peak is detected, the Peak Ready block

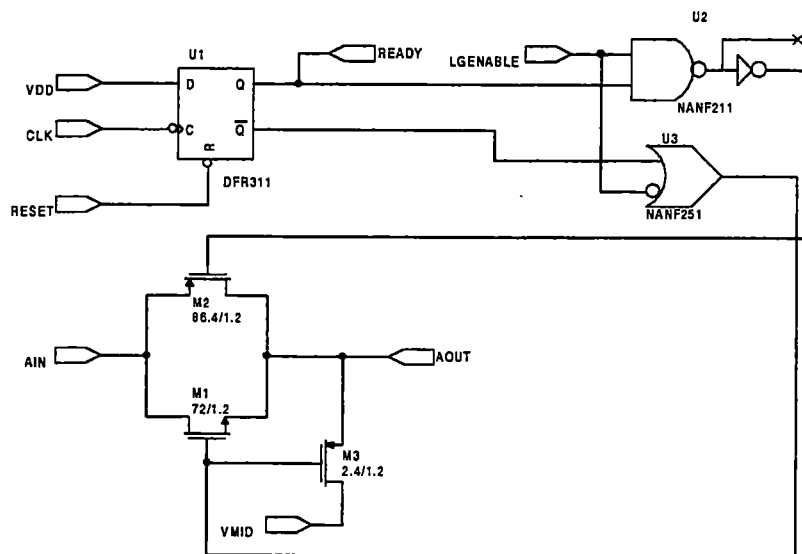


Figure 3.9. Linear Gate schematic.

(Figure 3.7) will clock the Flip Flop causing the transmission gate to be closed, if *LGENABLE* is high. Now *AOUT* is no longer equal to *AIN*. Instead, transistor M_3 has been included to hold *AOUT* at V_{mid} so that the input to the core PDH will not be floating. Since disabling the Linear Gate means that a peak has been detected, the output of the Flip Flop designated as *READY* in Figure 3.9 is also used as a logic signal to notify the DSP section that the peak is ready to be processed by the ADC. The Flip Flop is reset when *Reset_In* is pulsed by the DSP and the Linear Gate is again enabled to process the next pulse.

Two primary issues were considered when designing the Linear Gate: the series resistance of the switch and charge injection. The charge injection issue was eliminated by timing the switching of the Linear Gate after the pulse amplitude has dropped significantly, and the PDH circuit is open loop. Also, transistor M_3 is a PMOS device so that its charge injection will be negative when it is turned on to short the input to V_{mid} . Finally, when the Linear Gate is re-opened, the charge injection is not an issue because the PDH circuit output is being held at V_{mid} .

Second, a large switch resistance coupled with parasitic capacitance can introduce a large time constant in the signal channel that could degrade the rise time of the pulse. Thus, the switch was designed to have a small resistance. The finite channel resistance (r_{ds}) of the transistors is given as

$$r_{ds} = \frac{1}{\mu C_{ox} (W / L) (V_{GS} - V_t)} , \quad (3.1)$$

where μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, W is the channel width, L is the channel length, V_{GS} is the gate-source voltage, and V_t is the transistor threshold

voltage [8]. Equation 3.1 shows that r_{ds} can be reduced by increasing the W/L ratio or by increasing V_{GS} .

The bias dependence of r_{ds} illustrated in Equation 3.1 shows that the series resistance is large at low values of V_{GS} . This means that when the input voltage approaches VDD, r_{ds1} approaches infinity. Conversely, when the input voltage approaches VSS, r_{ds2} approaches infinity. Therefore, using a CMOS switch forms a parallel combination of r_{ds2} with r_{ds1} to give an approximately linear resistance over the full signal range. Figure 3.10 illustrates the Linear Gate resistance (r_{ds}) over the full dynamic range. The slight increase in r_{ds} could be minimized by increasing the W/L ratio of $M2$, but a maximum channel resistance of $120\ \Omega$ was sufficient.

3.4.2 PDH Enable Design

The PDH Enable block determines when a pulse has exceeded the noise floor and enables the core PDH to begin processing. As mentioned in the system description

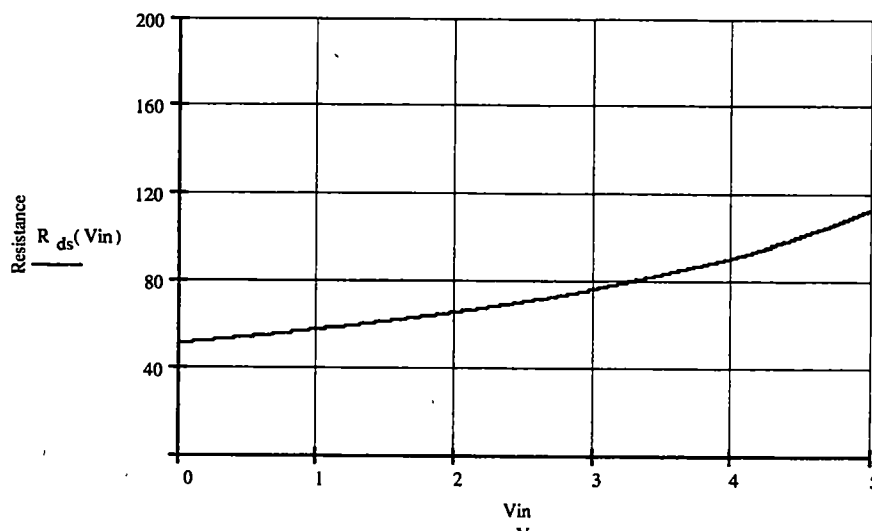


Figure 3.10. Hand calculated series resistance of Linear Gate.

above, the *PDH_EN* threshold is used by PDH Enable as a reference for incoming signals. Therefore, PDH Enable is simply composed of a threshold comparator that clocks a *D* Flip-Flop to hold the *PDH_EN* state. The PDH Enable comparator schematic is shown in Figure 3.11 without the Flip Flop included. A two stage CMOS operational amplifier operated open loop was used with a inverter placed on the output to give a fast rail-to-rail output swing [8].

The *PDH_EN* threshold is to be set off chip for prototyping purposes. Relatively small devices were used to minimize space and parasitics and improve speed. However, care was taken to minimize systematic offset voltage by sizing the *W/L*'s of *M*₇ and *M*₈ so that the current densities of *M*₃, *M*₄, and *M*₇ would be equal. The inverter was designed to have a threshold voltage of 2.5 V by making the *W/L* ratio of *M*₁₁ to *M*₁₂ equal to k_p/k_n where $k_n = \mu_n C_{ox}$ and $k_p = \mu_p C_{ox}$ [27]. The final *W/L* ratios were then tweaked with HSPICE. Simulation results showed that the comparator had a gain of 50 dB, a

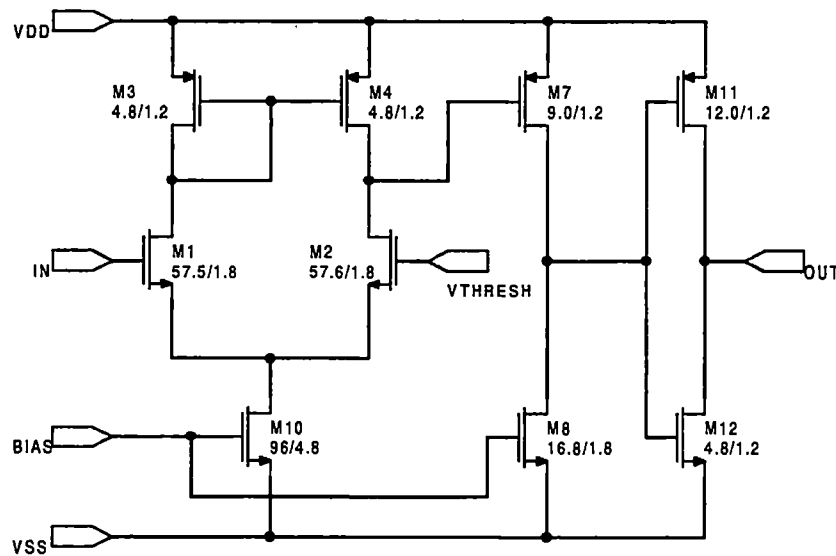


Figure 3.11. PDH Enable comparator Schematic.

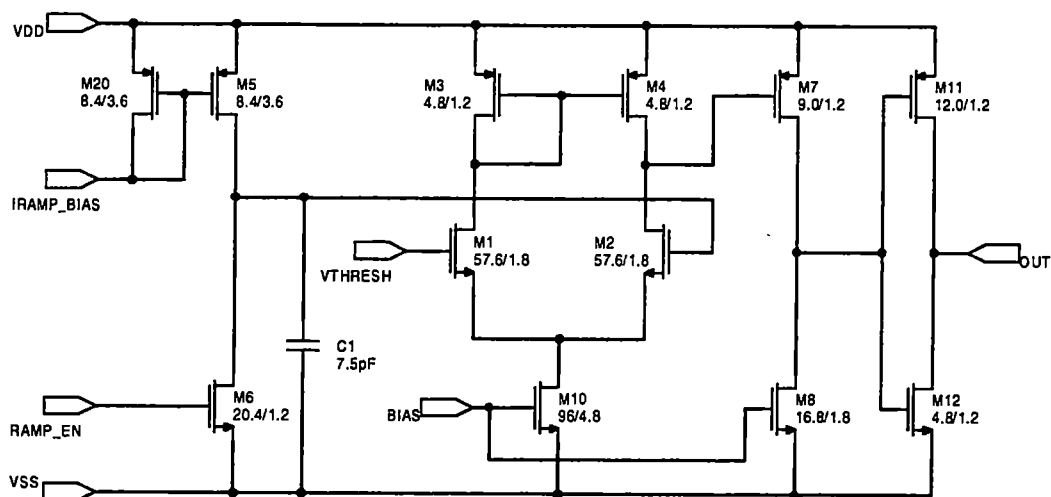
M_6 discharges capacitor C_1 at a constant rate set by the constant bias current of M_6 and the size of C_1 . The ramp output is then connected to a threshold comparator similar to the PDH Enable comparator. For prototyping purposes, the threshold voltage of this comparator, labeled *PK_Ready* Threshold in Figure 3.8, is set off chip.

When the ramp voltage drops below the *PK_Ready* threshold, the output of the comparator will go low and clock the Flip Flop in the Linear Gate. When the DSP section is done with the conversion and generates the reset pulse for the PDH, then the input to the ramp generator will drop back to its quiescent point, and M_5 will quickly charge C_1 to a voltage near V_{DD} .

This implementation of the Peak Ready block does have one potential problem. Undershoot on the input to the core PDH can cause the input to M_5 to go high and start the ramp prematurely. If the undershoot is significant, then the ramp could fall below the *PK_Ready* threshold before the peak of the pulse was reached causing the Linear Gate to be disabled and a false peak to be latched by the PDH.

3.4.3.2 Second Implementation of the Peak Ready Block

In order to ensure that no errors would occur in the Peak Ready block, a second implementation based strictly on the pulse timing was fabricated [26]. Since the shaper produces a pulse with a $\sim 2 \mu\text{s}$ rise time independent of magnitude, then the peak will always occur after the same amount of delay from the time the pulse exceeds the *PDH_En* threshold. Therefore, the second implementation shown in Figure 3.13 uses the *PDH_En* signal to start the voltage ramp by setting *RAMP_En* low only after a valid pulse has occurred. When *Ramp_En* goes low, then M_5 begins to charge C_1 at a constant rate set by its constant bias current I_{RAMP} and magnitude of C_1 . The ramp speed can be



found quantitatively by solving the fundamental relationship of $I = Cdv_c/dt$ for v_c by rearranging terms and integrating. The result is

where Δt is the difference between the start and stop time of the ramp and C_I is the capacitance in Figure 3.13. Thus, Equation 3.2 shows that increasing C_I decreases the slope of the ramp while increasing the bias current increases the slope.

3.5 Design and Analysis of the PDH Circuit

Figure 3.6 shows that the PDH circuit topology is similar to the classic two stage operational amplifier connected in a unity gain, voltage follower configuration [8]. However, the design is complicated by the non-linear operation of the circuit since current flows in the output stage only under transient conditions. The nonlinear operation presents some design trade-offs for this circuit that will be presented throughout the analysis. The nonlinear operation also makes analyses such as stability against oscillations and slew rate difficult with hand calculations alone. Therefore, approximate hand calculations will be used along with HSPICE simulations to characterize the circuit operation.

The operation of the circuit within the PDH system can be understood by referring to Figures 3.7 and 3.8. While the PDH is waiting for a pulse to occur, the *ENABLE* line in Figure 3.6 is held high and the output is then shorted to V_{MID} . The output is held at V_{MID} to keep input glitches from being integrated onto C_h . When a pulse is detected, the output of PDH Enable goes low, clocks the *D* Flip Flop that sets *ENABLE* low, and disconnects the output from V_{MID} . Now the PDH circuit is configured to follow the input pulse. The PDH circuit is actually enabled an instant before the shaper output is available by monitoring a node within the shaper circuit rather than at the shaper output.

As the input voltage increases, the circuit charges up C_h until it equals the input. Then when the input decreases, C_h cannot be discharged. When the input falls below the output, then the node labeled *PD* will instantly jump to V_{DD} and turn M_5 off. This operation occurs because the circuit goes open loop, and starts the voltage ramp in the first version of the Peak Ready block discussed above. Because *PD* changes at different

rates for different signal levels, the first version was susceptible to false peak ready indications. When the DSP section issues a reset, the D Flip Flop controlling $ENABLE$ resets and turns on M_7 , and C_h is discharged. The PDH circuit is then ready to process the next pulse.

Before presenting the PDH circuit analysis, it is of interest to note that the models used for hand calculations and HSPICE simulations were obtained from previous $1.2\ \mu\text{m}$ AMI ABN fabrication runs. The models used for the hand calculations and simulations presented below are in Appendix A at the end of this thesis.

3.5.1 Stability Analysis

The PDH circuit was designed to have enough bandwidth to process pulses with $2\ \mu\text{s}$ rise times. This corresponds to a minimum required bandwidth of only 400 kHz. The PDH circuit can easily achieve this bandwidth, but since the circuit uses negative feedback to improve its accuracy, it must be stable against oscillations. In fact, it must be over-damped because any overshoot in the circuits time response would translate to errors in peak detection.

The PDH circuit's stability against oscillations was analyzed by opening the connection between the output node (*node 6*) and the gate of M_2 (Figure 3.6). The equivalent impedance seen at *node 6* with the feedback connected was preserved by adding $C_{gs2}/2$ and $C_{gd2} (1+g_{m2}/2g_{m4})$ to C_h . C_{gs2} is decreased due to bootstrapping, and C_{gd2} is increased due to the Miller Effect. Using small signal analysis, the loop transmission ($T(f)$) was then derived by finding the mid-band loop gain (T_{mid}) and by finding the poles each node and the zero at *node 3* [28]. T_{mid} was calculated as the approximate small signal gain from the gate of M_2 to the output (*node 6*) while using the

relationship of $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$ to simplify the final expression. The pole frequencies, the zero frequency, and T_{mid} were then plugged into the following general form to get the complete loop transmission expression:

$$T(f) = \frac{T_{mid} \left(1 + \frac{jf}{f_{z2}} \right)}{\left(1 + \frac{jf}{f_2} \right) \left(1 + \frac{jf}{f_3} \right) \left(1 + \frac{jf}{f_6} \right) \left(1 + \frac{jf}{f_8} \right)} \quad (3.3)$$

The frequency subscripts in Equation 3.3 correspond to the node numbers in Figure 3.6.

Table 3.1 lists the expressions for each component in Equation 3.3.

Because no current flows in the output stage under quiescent conditions, the loop transmission changes under transient conditions. To account for this change, the loop transmission was evaluated for a worst case and best case condition.

Simulations show that the output current flow through M_5 (I_{d5}) is greatest at the beginning of the semi-Gaussian pulse, where the slope is the greatest. The current then decreases until the peak is reached and M_5 shuts off completely. Therefore, the loop

Table 3.1. Summary of components in PDH circuit loop transmission.

PARAMETER	VALUE
T_{mid}	$\frac{g_{m2}}{g_{ds1} + g_{ds3}} * \frac{g_{m5}g_{m6}}{g_{ds5} * g_{ds6}}$
f_{z2}	$-\frac{g_{m5}}{2\pi * c_{gd5}}$
f_2	$\frac{1}{2\pi * \left[c_{gs5} + c_{gd5} \left(1 + \frac{g_{m5}}{g_{m6}} \right) + c_{gd1} + c_{db1} + c_{gd3} + c_{db3} \right] * r_{ds1} r_{ds3}}$
f_3	$\frac{g_{m3}}{2\pi * (c_{gd4} + c_{db4} + c_{gs4} + c_{gs3} + c_{db2} + c_{gd2})}$
f_6	$\frac{1}{2\pi * (C_h + c_{gd} (1 + g_{m2}/2g_{m4}) + c_{gd}/2) + c_{gd} + c_{db6} + c_{db} + c_{gd} + c_{db2} + c_{gd2}) * g_{m6}/ds/ds}$
f_8	$\frac{g_{m6}}{2\pi * (c_{gd5} + c_{db5} + c_{gs6} + c_{sb6})}$

transmission was calculated for two cases: first when I_{d5} is maximum and a second when I_{d5} is approaching shutoff. Figure 3.14 (a) shows the loop transmission when $I_{d5} = 8 \mu\text{A}$ and Figure 3.14 (b) shows the result when $I_{d5} = 0.1 \mu\text{A}$. The results show that the circuit becomes more stable and the bandwidth decreases as the signal nears its peak. The results also show that the PDH circuit has a nearly single pole response with *node 6* dominating due to the relatively large C_h . The pole at *node 2* is the second critical pole because it occurs near the unity gain frequency (f_c) of the loop transmission. Therefore, its time constant was minimized by making M_3 and M_4 small to minimize parasitic capacitance. The cascode transistor M_6 helped keep the time constant at *node 2* small by reducing the Miller Effect across M_5 [9]. The other poles and zeros in Equation 3.3 occur well beyond f_c and do not significantly affect the circuit's stability. The offset analysis later shows that the constraint placed on the time constant at *node 2* introduces a trade-off that must be made between the circuit's phase margin and offset.

Figure 3.15 shows the HSPICE simulation results for the PDH circuit under the same bias conditions used in Figure 3.14. The simulation results are similar to those obtained by hand calculation. Table 3.2 summarizes the results for bandwidth, phase

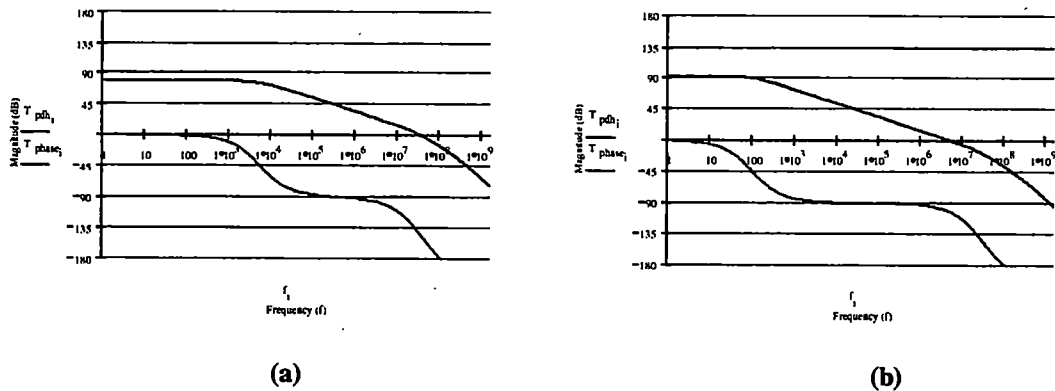
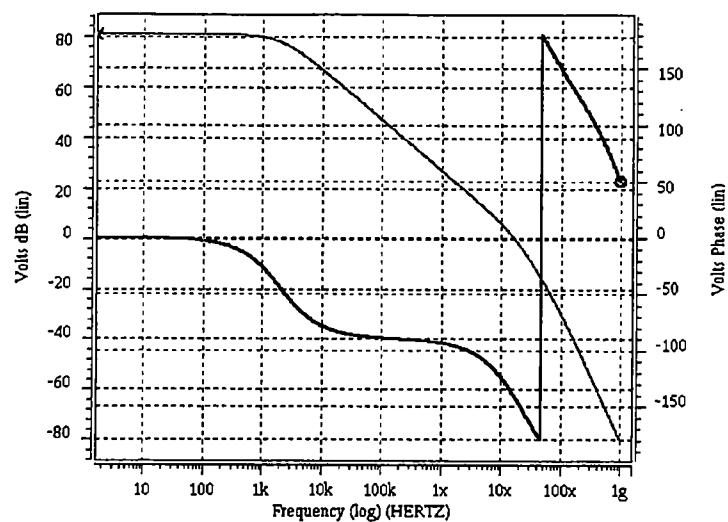
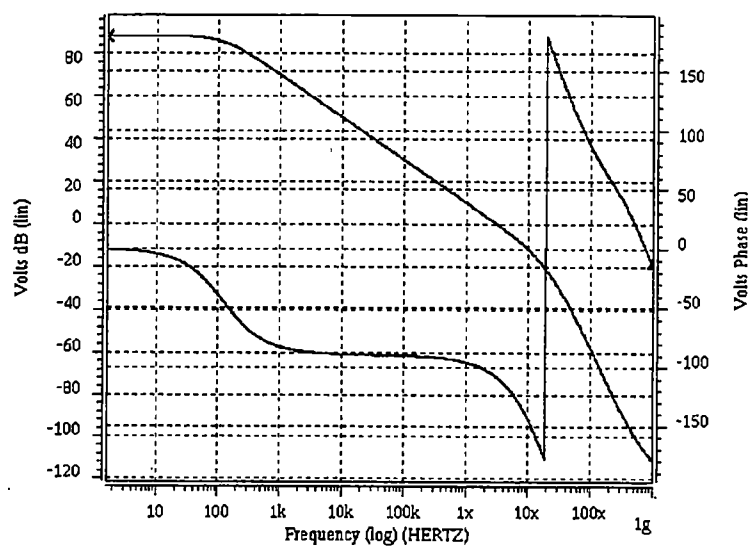


Figure 3.14. Hand calculated loop transmission for (a) $I_{d5} = 8 \mu\text{A}$ and (b) $I_{d5} = 0.1 \mu\text{A}$.



(a)



(b)

Figure 3.15. HSPICE simulation of loop transmission with (a) $I_{d5} = 8 \mu\text{A}$ and (b) $I_{d5} = 0.1 \mu\text{A}$.

Table 3.2. Comparison of hand calculated and simulated loop transmission.

Design Parameter	Hand Calculated		HSPICE Simulation	
	$I_{d5}=0.1 \mu\text{A}$	$I_{d5}=8 \mu\text{A}$	$I_{d5}=0.1 \mu\text{A}$	$I_{d5}=8 \mu\text{A}$
DC Gain (dB)	92	78	88	82
Bandwidth (MHz)	4	25	3.2	16
Phase Margin (deg.)	76	35	70	40
Gain Margin (dB)	40	15	20	15

margin, and gain margin found with simulation and by hand calculation. Notice that the phase margin shrinks as I_{d5} increases. The reduction in phase margin occurs because the gain-bandwidth product of the second stage, which is equal to g_{m5}/C_h , increases while the second critical pole is virtually in the same location. Although the phase margin is small, the circuit does not oscillate because the increased speed of the circuit allows the output voltage to quickly charge to the input voltage, and as the output nears voltage approaches the input voltage, I_{d5} is reduced significantly making the circuit more stable. An error may occur with a pulse whose rise time approaches the maximum rise time of the PDH circuit. Here, the PDH circuit may not recover fast enough, and the reduced phase margin would result in overshoot at the output. However, the small signal analysis shows that the PDH circuit can achieve wide bandwidth, and overshoot is not a problem for pulses with $\sim 2 \mu\text{s}$ rise time.

The loop transmission results show that the circuit has sufficient bandwidth to process a pulse with a $2 \mu\text{s}$ rise time. The large DC loop gain also indicates that accuracy will be high when the loop is closed. The addition of the cascode transistor M_6 did not greatly improve the PDH circuit's phase margin by reducing the Miller effect at node 2. The Miller effect was not significantly reduced because of two reasons. The first is that g_{m6} is proportional to I_{d5} so that when I_{d5} is small, the impedance at node 8 is high. Therefore, there is still significant gain across C_{gd5} . The second reason is because at frequencies near f_c , C_h dominates and the output impedance and the gain across C_{gd5} is low. It does improve the DC gain by $\sim 25 \text{ dB}$, and the experimental testing will be used to determine if this improves the accuracy of the PDH circuit.

3.5.2 Offset Analysis

Recall that under ideal conditions, when no input to the PDH circuit is present, no current will flow in the output stage. If any current does flow, then it will be integrated onto C_h and appear as an offset voltage. Therefore, under quiescent conditions, transistor M_5 must be completely off to eliminate current flow in the output stage. This could only be achieved if magnitude of $V_{GS,on5}$ were greater than $V_{GS,on3}$. However, M_3 , M_4 , and M_5 can not be sized to achieve zero quiescent current flow in the output stage, but the negative feedback will adjust the voltage at *node 3* to ensure that $I_{d5} = 0$ under quiescent conditions. The required voltage adjustment at *node 3* leads to an undesirable offset voltage (V_{off}) at the output. The expression for V_{off} in the following analysis shows that M_3 , M_4 , and M_5 can be sized in a way that minimizes the error.

The source of the offset voltage can be explained as follows: before a pulse arrives at the input of the PDH circuit, the input is at V_{mid} and the output is held at V_{mid} by M_7 . Thus, the voltage at *node 2* is equal to the voltage at *node 3*, and the differential amplifier of the PDH circuit is balanced. Figure 3.16 models the condition when the differential amplifier is balanced. The circuit is similar to a current mirror, and it shows that I_{d5} will flow and is going to be proportional to $I_{tail}/2$. Now, if *ENABLE* (Figure 3.6) was taken low while the input to the PDH circuit remained at V_{mid} , current would continue to flow through M_5 and charge C_h . However, referring back to the PDH circuit (Figure 3.6) shows that as the output voltage rises, current is switched from M_3 to M_4 due to the negative feedback. This forces the drain voltage of *node 2* to rise until M_5 is completely off and $I_{d5} = 0$. This voltage change required at *node 2* (ΔV_2) to turn M_5 off can be expressed as

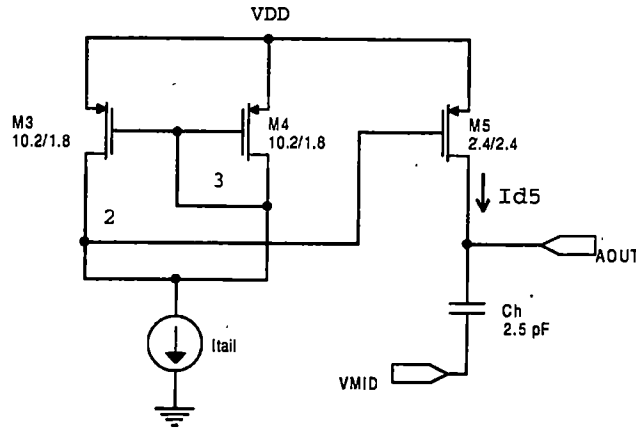


Figure 3.16. Circuit model of the PDH circuit under balanced condition where balanced means that the output voltage is exactly equal to the input voltage. The circuit operates like a current mirror.

$$\Delta V_2 = V_{on3} - V_{on5} \quad (3.4)$$

where $V_{on} = -V_{GS} + V_{ip}$ for a PMOS transistor. Substituting this expression for V_{on3} and V_{on5} into Equation 3.4 gives

$$\Delta V_2 = \sqrt{\left(\frac{2I_{D3}}{\mu_p C_{ox} (W/L)_3} \right)} - \sqrt{\left(\frac{2I_{D5}}{\mu_p C_{ox} (W/L)_5} \right)}. \quad (3.5)$$

Since V_2 must change enough to cause no current to flow in the output stage, then $I_{D5} = 0$.

Plugging $I_{D5} = 0$ into Equation 3.5 gives

$$\Delta V_2 = \sqrt{\left(\frac{2I_{D3}}{\mu_p C_{ox} (W/L)_3} \right)}. \quad (3.6)$$

Equation 3.6 is valid if the transistor is assumed to turn completely off when its gate voltage drops below the threshold voltage. This neglects subthreshold operation, but gives a good first order approximation.

This ΔV_2 is actually caused by a change in output voltage. Now, ignoring M_5 and M_6 , it has been shown that changing the output voltage, which is the voltage at the gate of M_2 , results in a voltage change at *node 2*. The resulting voltage change at *node 2* is simply the voltage change at *node 6* multiplied by the voltage gain of the differential amplifier (A_{vdiff}). Conversely, the positive voltage change at *node 2* expressed in Equation 3.6 can be referred to a positive offset voltage at the output by dividing by A_{vdiff} to give

$$V_{off} = \frac{\sqrt{\left(\frac{2I_{D3}}{\mu_p C_{ox} (W/L)_3} \right)}}{A_{vdiff}} \quad (3.7)$$

Equation 3.7 shows that ΔV_2 is reflected to the output by dividing by the gain of the differential pair. The gain of an actively loaded differential pair can be expressed as

$$A_{vdiff} = \frac{g_{m1}}{2\lambda I_D} \quad (3.8)$$

where λ is channel length modulation. Substituting the expression for A_{vdiff} and $g_m = \sqrt{\mu C_{ox} W / L 2I_D}$ into Equation 3.7 and simplifying give the following expression:

$$V_{off} = \frac{2\lambda I_{D3}}{\sqrt{\mu_p C_{ox} (W/L)_3} \sqrt{\mu_p C_{ox} (W/L)_1}} \quad (3.9)$$

Equation 3.9 gives insight into the major factors that contribute to systematic offset voltage: I_{D3} , $(W/L)_3$ and $(W/L)_1$. Increasing $(W/L)_3$ decreases ΔV_2 in Equation 3.6 by reducing V_{eff3} and decreasing I_{D3} or increasing $(W/L)_1$ increases A_{vdiff} in Equation 3.8. It is important to note that neither the size of M_5 nor I_{D5} affect V_{off} .

This offset analysis has led to an important trade-off in the PDH circuit design. The stability analysis showed that the pole at *node 2* must be minimized by making M_3 and M_4 small to minimize the time constant and achieve adequate phase margin. However, the offset analysis has shown that large $(W/L)_1$ and $(W/L)_3$ reduce the offset voltage. Thus, a trade-off must be made between bandwidth and voltage offset.

3.5.3 Charge Injection

Charge injection occurs when the PDH circuit detects a peak and goes open loop. Figure 3.17 highlights the two PDH circuit nodes that contribute to the charge injection. The first is due to *node 2* switching from $V_{DD} + V_{GS3}$ to V_{DD} to turn M_5 off when a peak has been reached. When M_5 shuts off, the channel charge (Q_{ch}) of M_5 and M_6 must flow out. It is assumed that most of M_5 's channel charge flows out of the source and can be neglected. There is also clock feed-through due to C_{gd5} , but it can also be neglected because $C_{gd5} \ll C_h$. However, all of the channel charge of M_6 will flow onto C_h . Neglecting the body effect, the channel charge of M_6 is can be expressed as

$$Q_{ch6} = \frac{2}{3} * (W * L)_6 * C_{ox} * (V_{eff6}) . \quad (3.10)$$

This Equation holds while M_6 is saturated [9]. When M_6 drops out of saturation, the 2/3 in Equation 3.10 becomes 1. The charge flow will cause a voltage change at the output (ΔV_{out}) expressed as

$$\Delta V_{out} \Big|_{Q_{ch6}} = \frac{Q_{ch6}}{C_h} , \quad (3.11)$$

and the change is positive because the charge is positive. For $V_{eff6} = 1.5$ V,

$\Delta V_{out}|_{Q_{ch6}} = 6.4$ mV while in saturation and 9.5 mV while in the ohmic region. Both of these values are dependent only on the cascode transistor biasing.

Figure 3.17 also shows another source of charge injection: clock feed-through at *node 3* due to C_{gd2} . Although the voltage change at *node 3* is small, the HSPICE simulation in Figure 3.18 shows it does decrease to accept the full tail current (I_{tail}) of the differential pair after a peak has been detected. The change at *node 3* can be expressed as

$$\Delta V_3 = V_{SG3}|_{I_{D3}=I_{tail}/2} - V_{SG3}|_{I_{D3}=I_{tail}} \quad (3.12)$$

Equation 3.12 is valid because at the peak, the input and output voltages are equal so that the differential pair is balanced (Figure 3.18). Then as the input decreases, all of the current switches to the right side of the differential pair.

Substituting the expression for V_{GS} into Equation 3.16 and reducing gives

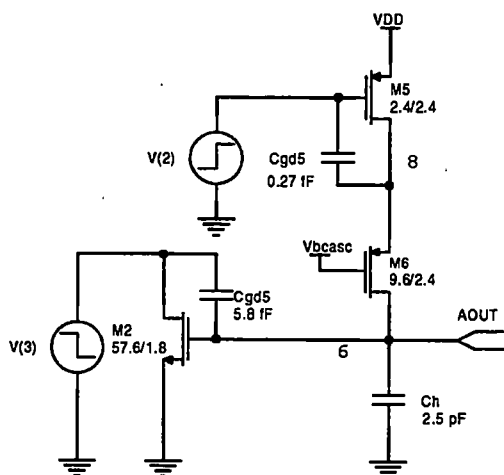


Figure 3.17. Illustration of critical nodes of the PDH circuit during a switching transient when a peak voltage is reached.

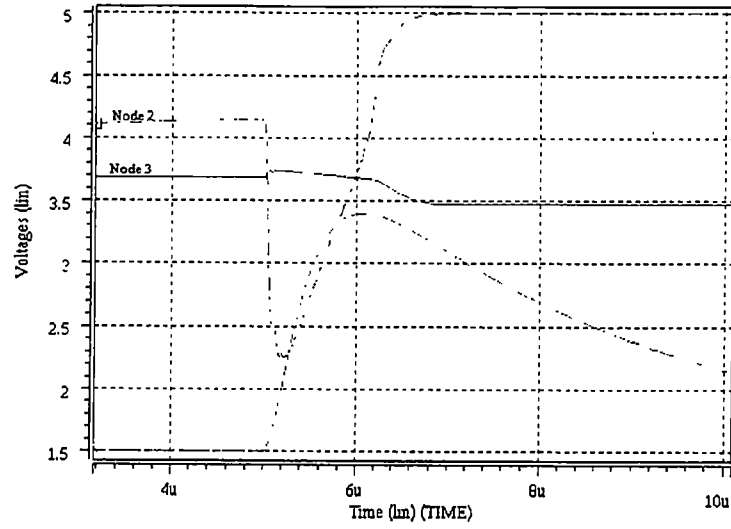


Figure 3.18. HSPICE simulation showing the switching characteristics of node 2 and 3 of the PDH circuit when a peak is detected.

$$\Delta V_3 = \sqrt{\frac{I_{tail}}{\mu_p C_{ox} (W/L)_3}} * [1 - \sqrt{2}] \quad (3.13)$$

which shows that ΔV_3 is negative. This voltage change is then referred to the output by the capacitor divider formula [8]

$$\Delta V_{out}|_{node3} = \Delta V_3 \frac{C_{gd2}}{C_h + C_{gd2}} \quad (3.14)$$

Using the values in Figure 3.16 and for $I_{tail} = 25 \mu A$, $\Delta V_3 = -0.18V$ and

$\Delta V_{out}|_{node3} = -1.1mV$. This value is approximately independent of signal amplitude

but dependent on biasing. Finally, the total error due to charge injection is the sum of Equation 3.11 and Equation 3.14 or approximately $5.3 mV$ while M_6 is in saturation.

The total output error voltage can now be expressed as

$$V_{off,tot} = \Delta V_{out}|_{node3} + \Delta V_{out}|_{Q_{ch6}} + V_{off} \quad (3.15)$$

Figure 3.19 compares a plot of Equation 3.15 versus bias current with HSPICE simulated offset voltage. The results show good agreement, but the hand calculated result has a slightly steeper slope. This variation may be due to the dependence of Equation 3.9 on the output impedance of M_1 and M_3 , which is not modeled well. However, the hand equations do give good insight into the major sources of error.

Figure 3.20 shows an HSPICE simulation that illustrates all three errors that occur when a peak is detected. The negative change in the output corresponds to the negative voltage step at *node 3* illustrated in Figure 3.18 above. The negative change predicted by SPICE is about twice the value predicted by hand calculation. It is impossible to determine what amount of the positive voltage error is due to offset and what amount is due to charge injection.

Although these errors reduce the circuit's ability to sample and hold the exact peak value, they do not degrade the linearity of the circuit if they are constant over the entire dynamic range. The results shown in Figure 3.19 and Figure 3.20 are calculated for a single input amplitude, but the PDH circuit will be tested over the full range of amplitudes.

3.5.4 Slew Rate

The slew rate (SR) of the circuit is dependent upon the amount of current that can be delivered to the relatively large C_h , and it can be expressed as

$$SR = \frac{dv_{out}}{dt} = \frac{I_{D5}}{C_h}. \quad (3.16)$$

Since I_{D5} is related to V_{GS5} by the square law relationship, and V_{GS5} changes with signal amplitude, the SR is time varying. The derivation of an analytical expression for the slew

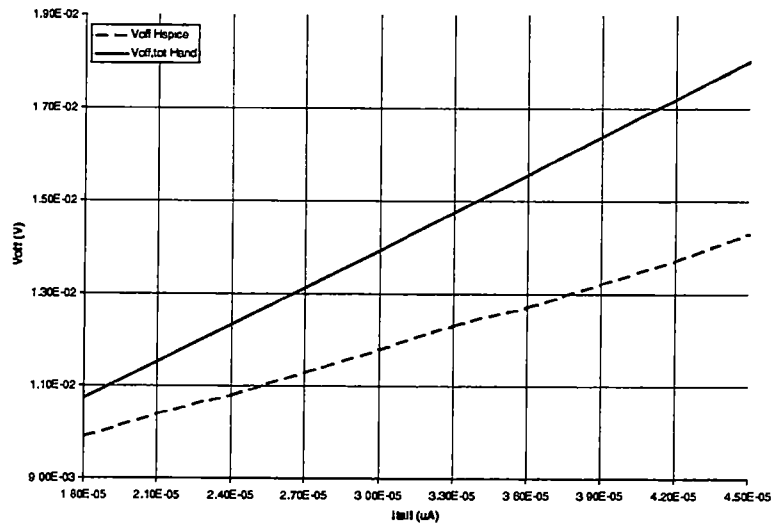


Figure 3.19. Comparison of hand calculated offset voltage with HSPICE results.

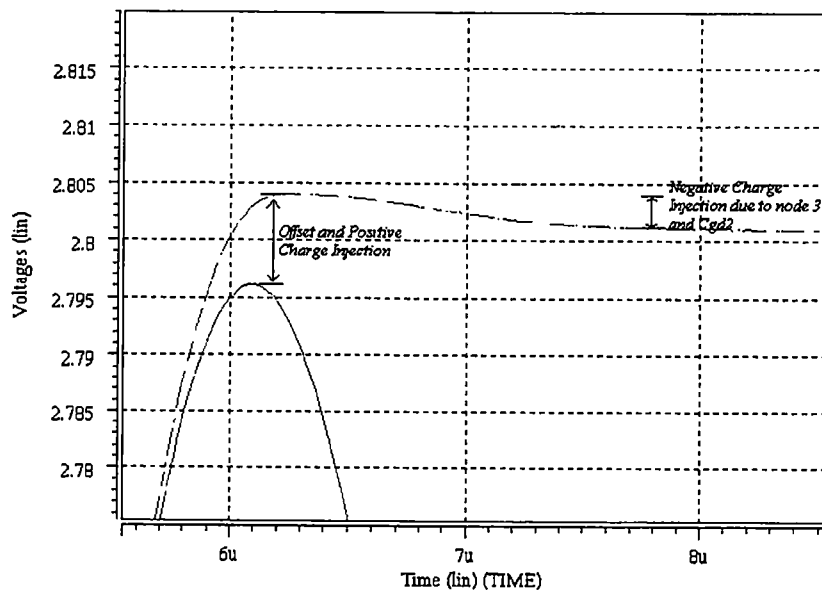


Figure 3.20. Illustration of offset and charge injection errors that occur when a peak is detected.

rate is complicated because the value of V_{GS5} cannot be found analytically. However, this dynamic operation does allow the PDH circuit to achieve good SR performance by adjusting the $(W/L)_5$ ratio. Figure 3.21 shows the SR versus input voltage amplitude obtained with HSPICE. Figure 3.21 shows that the SR decreases as the input voltage increases. This is due to the square law relationship between output current V_{GS5} . As the output voltage approaches the input voltage, V_{GS5} decreases causing I_{D5} to decrease. Thus, the SR decreases as the output voltage nears the input voltage. The SR drops significantly at amplitudes above 2.25 V. This is because M_5 is dropping out of saturation and the output current is no longer controlled by the square law relationship. Instead, it just operates as a voltage controlled resistor making the SR dependent upon the $r_{ds5}C_h$ time constant, which is also time varying.

3.5.5 Droop Rate

Once the peak has been sampled onto C_h , leakage currents (I_{leak}) at the output node $AOUT$ will cause the voltage to droop. The magnitude of the voltage droop rate

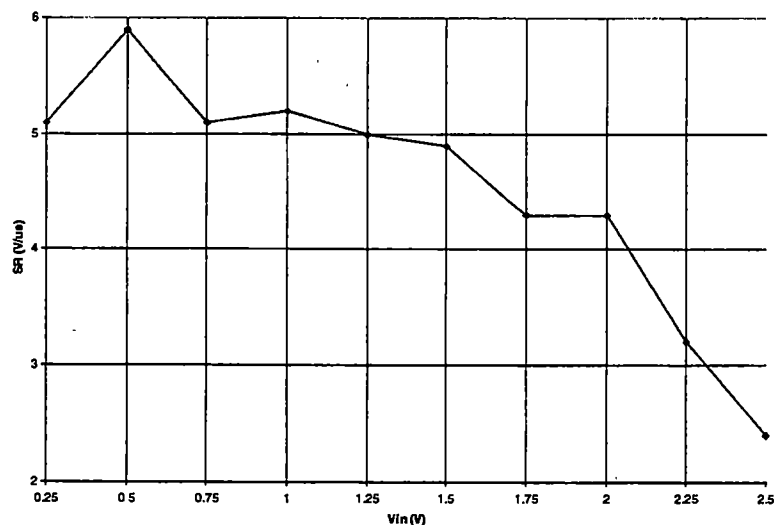


Figure 3.21. HSPICE simulation of SR versus input voltage magnitude.

(ΔV_{droop}) can be expressed as

$$\frac{\Delta V_{droop}}{\Delta t} = \frac{I_{leak}}{C_h} \quad (3.17)$$

Voltage droop (V_{droop}) results from leakage currents at the output node due to MOS gates, reverse biased $p-n$ junctions, and finite insulation resistance of the polysilicon capacitor. The voltage droop is typically dominated by the leakage currents of the reverse biased diodes connected to the output (Figure 3.22) [9, 26]. The reverse current of the diodes has a voltage dependence [9]. Therefore the droop rate will vary with output signal amplitude.

The leakage current was measured with HSPICE by sweeping a voltage source connected to the output node and measuring the current of the source. At an output of 5 V, the worst case $I_{leak} = 8.6$ pA. This gives a droop rate of $3.25 \mu\text{V}/\mu\text{s}$. Since the DSP section is expected to take less than $10 \mu\text{s}$ to complete a conversion, this droop rate will not be a significant source of error.

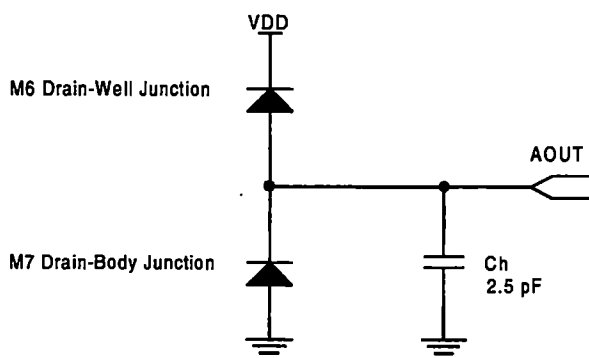


Figure 3.22. Illustration of the reverse biased $p-n$ junctions at the output node during the hold operation of the PDH circuit.

3.6 PDH Test Circuit

The PDH circuit used in the HotSpotter analog channel does not have the capability to drive large capacitive loads. Therefore Figure 1.5 shows that a buffer amplifier was placed after the PDH circuit to drive off chip. Because the PDH circuit was included in the complete PMT channel, stand alone testing would be difficult. Thus, a test PDH circuit was fabricated without the external control blocks shown in Figure 3.7 included so that the circuit could be thoroughly analyzed. Figure 3.23 shows the schematic of the test PDH circuit. Notice that a source follower stage has been included inside the feedback loop to drive the pad capacitance when going off chip. Since the output stage gain was less than one, the size of M_5 and C_h were modified slightly to

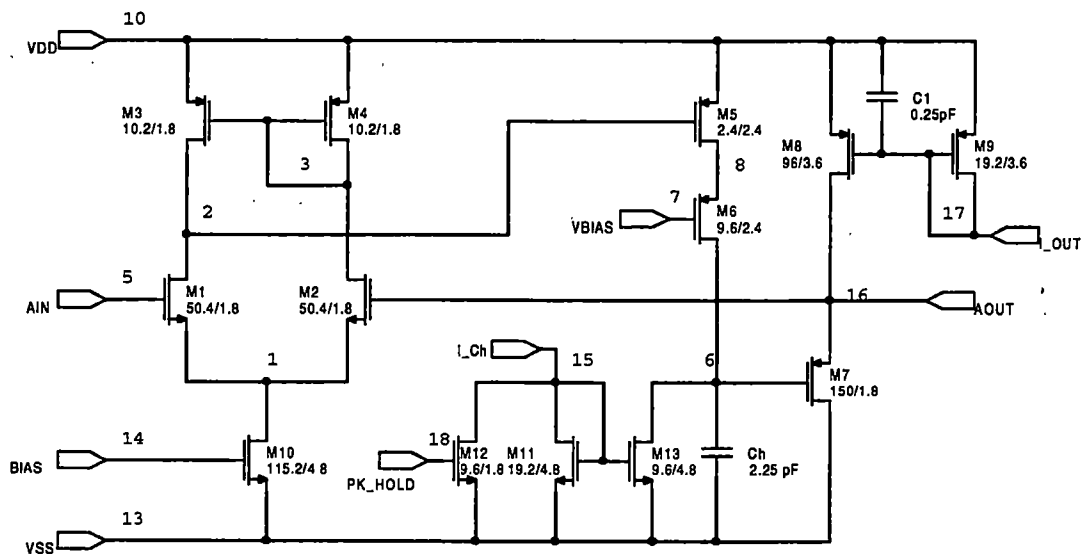


Figure 3.23. PDH test circuit with source follower output stage included for driving off chip. Additional biasing circuitry has also been added to provide at *node 6* for biasing purposes.

maintain the same bandwidth as the PDH circuit. Another difference is that the C_h is no longer referenced to V_{mid} . A current mirror was included for biasing, and it is turned off by setting PK_HOLD high when detecting a peak.

3.7 Summary of PDH Circuit Analysis

The hand analysis and HSPICE simulation has highlighted the critical design constraints of the PDH circuit. The major trade-offs are the size of the hold capacitor, size of the active load transistors, and the size of the output drive transistor (M_5). The offset and droop analysis show that a large C_h improves the accuracy of the circuit, but the SR and small signal analysis show that it reduces the bandwidth and speed of the circuit. The offset analysis showed that increasing the W/L ratios of the load transistors reduces the offset voltage, but the small signal analysis showed that this would reduce the phase margin. Finally, increasing the W/L of M_5 increases the speed and loop gain of the circuit, but decreases the stability and offset voltage. These are the critical issues that must be addressed when designing the PDH circuit shown in Figure 3.6, and each one has been optimized through analysis and with simulation to provide the best performance for the HotSpotter system.

CHAPTER 4

Layout and Simulation

4.1 Tools and Technology

The PMT channel prototype for the HotSpotter was fabricated in the 1.2 μm AMI ABN process through MOSIS. The process is an n-well process with two polysilicon layers and two metal layers. The process parameters provided by MOSIS for the PMT channel prototype run (N97N) are shown in Appendix B. Models from previous runs are also provided by MOSIS, and the set used for pre-fabrication simulations and for the hand calculations (N88Z) done in Chapter 3 is also shown in Appendix A.

The layout was done with the public domain CAD tool Magic version 6.3 running on a Sun workstation [29]. The SPICE netlist extractions were obtained by using a modified version of Magic's netlist utility. HSPICE version 96.3.1 by Meta-Software, Inc. was then used to perform the circuit simulations with the BSIM v3.1 models provided by MOSIS.

4.2 Layout

4.2.1 PMT Channel

A single PMT channel was fabricated for prototyping purposes on a tiny chip measuring 2.1 x 2.1 mm. Figure 4.1 shows the Magic layout of the chip, and Figure 4.2 shows a photograph of the die. The tiny chip has forty pads and the channel consumed thirty-five of those. The five remaining pins and available die area allowed the PDH test circuit to be included at the lower left corner.

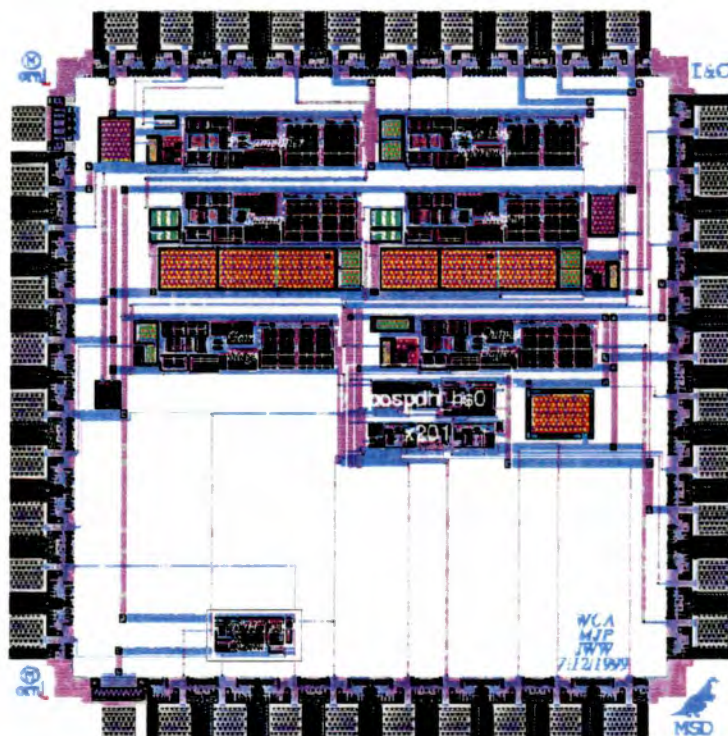


Figure 4.1. Magic layout of the PMT channel prototype chip.

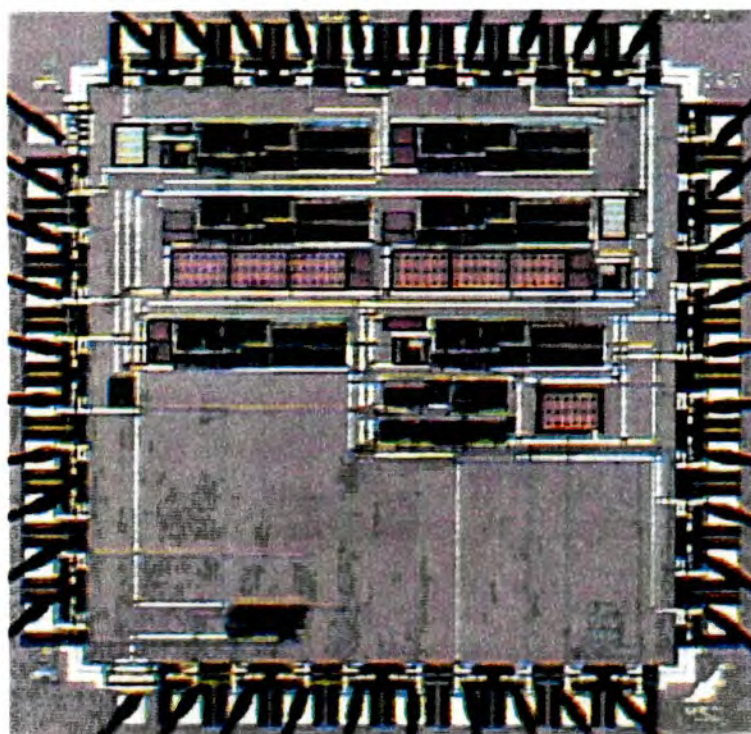


Figure 4.2. Photograph of PMT channel prototype chip.

Each block of the analog channel was given separate power and ground pins to prevent noise from coupling from one section of the channel to the next, and bypass caps were included where space permitted. Separating the power and ground nets also aided in experimental testing by allowing each block to be powered independently. The preamplifier is located at the top left corner of the chip. The baseline reference circuit is located next to the preamplifier, and the shaper is located below these two blocks and stretches across the full width of the die. Below the shaper and on the left side is an additional gain stage. The final block of the analog channel is the PDH, labeled `pospdh_hs0` in Figure 4.1. For testing purposes, the output of each block was brought out to a pad.

4.2.2 PDH System Layout

Figure 4.3 shows the Magic layout of the PDH block. The arrangement of the four PDH cells within the layout corresponds to the block diagram shown in Figure 3.7.

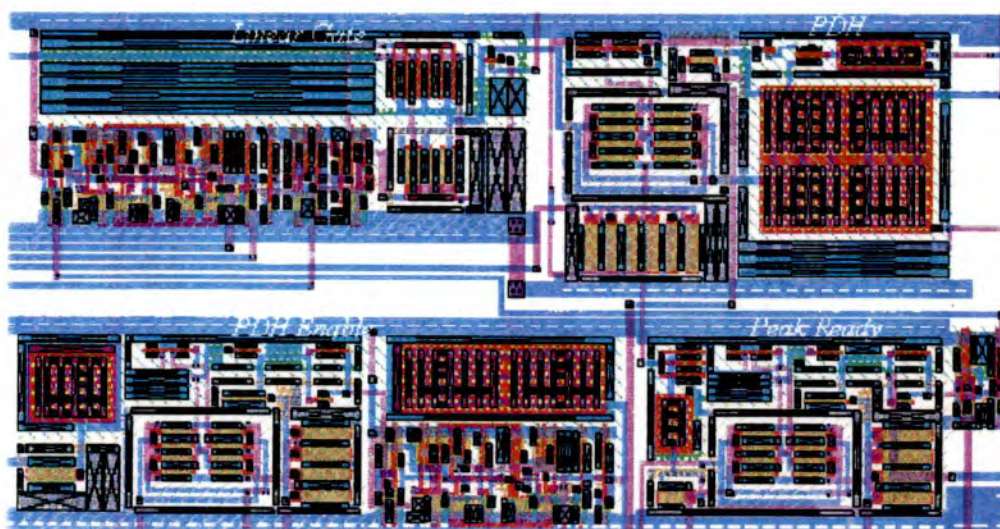


Figure 4.3. Magic layout of the PDH block.

The wide power rails that border the top and bottom of each cell were slotted to offer strain relief and to prevent the silicon nitride layer from peeling [22]. Because the PDH block contains both digital and analog signals, attention was paid when routing critical analog traces to isolate them from transients during switching. The input to the Linear Gate is routed near the upper supply rail and guard rings isolate it from the standard cell *D* Flip-Flop and logic gates at the bottom of the cell. The two transistors that form the CMOS transmission gate are located at the right side of the cell, and are inter-digitated to reduce parasitics [8]. The tiny transistor at the upper right hand corner of the cell holds the PDH input at V_{mid} when the Gate is closed. Guard rings were also used between transistors and between cells to minimize substrate coupling between devices. The PDH block measures $317.2\ \mu\text{m} \times 501\ \mu\text{m}$.

4.2.3 *Peak Ready Comparator*

The layout of the Peak Ready circuit is shown in Figure 4.4. The ramp generator is located to the left of the comparator. The PMOS current mirror located in the upper

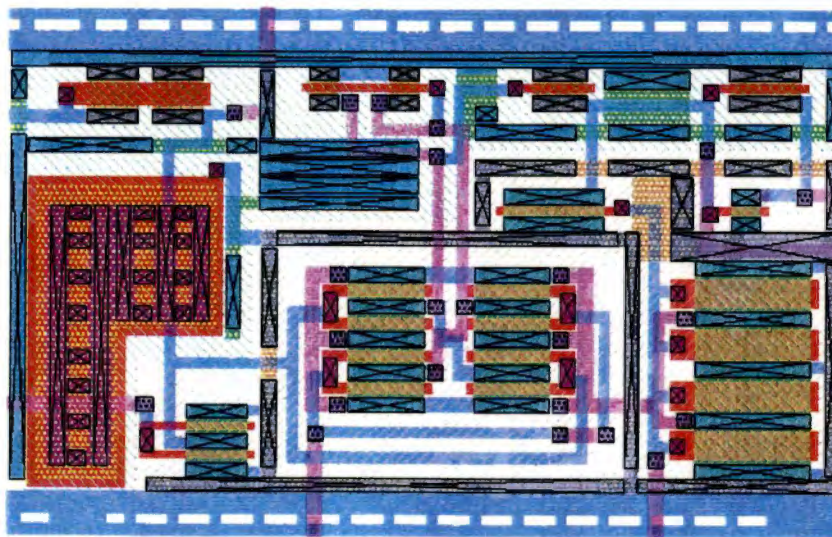


Figure 4.4. Magic layout of the Peak Ready circuit.

left corner provides the constant current to charge the capacitor, and the NMOS transistor at the bottom left corner resets and starts the ramp. The actual capacitor value was not critical, so it was laid out using extra space within the cell. The Peak Ready block measures $87.6 \mu\text{m} \times 129.6 \mu\text{m}$.

The PDH Enable cell is similar to the Peak Ready cell with the difference being the omission of the ramp generator. The PDH Enable block measures $87.6 \mu\text{m} \times 107.4 \mu\text{m}$.

4.2.4 PDH Circuit

Figure 4.5 shows the PDH circuit layout, Figure 4.6 shows the PDH test circuit layout, and Figure 4.7 shows a simulation of the PDH test circuit. The differential pair is located on the left side of the cell. The load transistors are at the top, the tail current source is at the bottom, and the input transistors are in the middle. Input transistor matching is important to minimize offsets due to gradient effects across the die, so they were laid out in a common-centroid geometry [8]. The large transistors were also inter-digitated to minimize die area and parasitics. The reset transistor, M_7 , is located beside differential pair load transistors. M_5 and M_6 are the tiny transistors located above the large capacitor. The small capacitor at the top of the cell fills unused area and serves as a bypass for the cascode transistor's gate bias line. The hold capacitor was made with two polysilicon layers separated by SiO_2 . The process parameters found in Appendix B show that the capacitive density of the double polysilicon capacitor is $\sim 0.6 \text{ fF}/\mu\text{m}^2$. The hold capacitor measures $66.6 \mu\text{m} \times 66.6 \mu\text{m}$ to give an extracted capacitance of $\sim 2.65 \text{ pF}$. The actual capacitance value has a tolerance of $\pm 20 \%$, and this was accounted for when

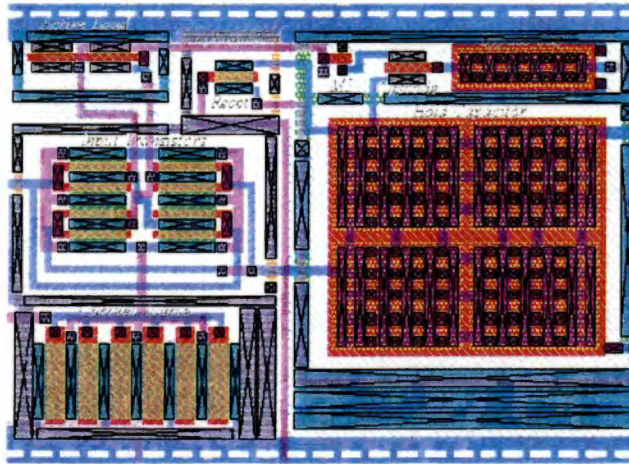


Figure 4.5. Magic layout of the PDH circuit.

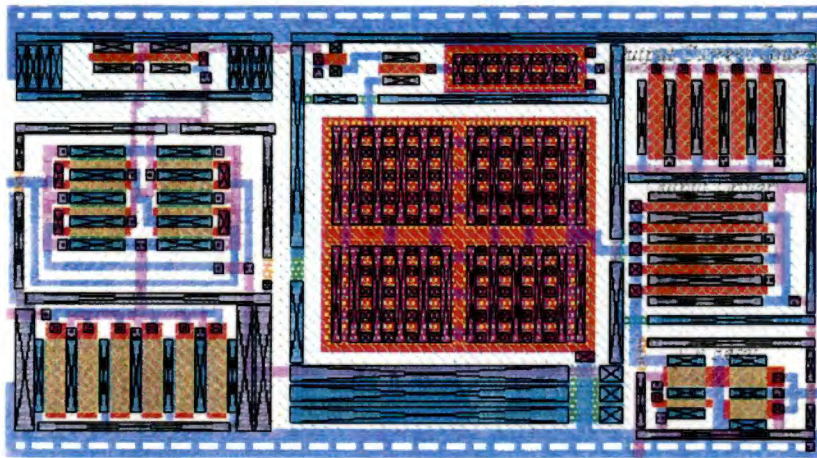


Figure 4.6. Magic layout of PDH test circuit.

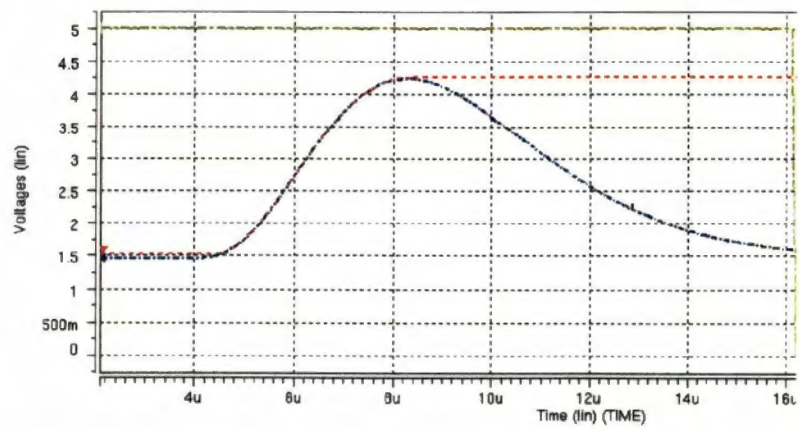


Figure 4.7. Simulation of PDH test circuit operation.

choosing the value of C_h . C_h was isolated from the transistors with guard rings and placed over an n-well to minimize substrate noise during switching. The n-well increases the parasitic capacitance of the bottom plate [8], but the effect was eliminated by connecting the bottom plate to the low impedance power rail while connecting the top plate to the drain of M_6 . Finally, the contact pattern on the top of the capacitor was used to provide strain relief. The HSPICE simulations of the PDH circuit were covered in Chapter 3. The PDH circuit measures $117.6\ \mu\text{m} \times 182.4\ \mu\text{m}$.

The PDH test circuit contains the source follower output stage. These transistors are relatively large due to the large current they must deliver to the output. It also contains the C_h bypass current source and reset switch located at the bottom right corner the cell. The PDH test circuit measures $117.6\ \mu\text{m} \times 246\ \mu\text{m}$.

4.3 System Simulation

Prior to submission, the complete chip was simulated from input pad to output pad to verify operation. Appendix C shows the SPICE source file used for the system simulation and the Magic extraction files for PDH circuits. The SPICE file generated the preamplifier input by passing a negative voltage step through a charge terminator along with a voltage controlled current source to simulate the PMT output. The results of one system simulation is shown in Figure 4.8 and verifies that the design was working before submission. Figure 4.8 shows the PDH circuit detecting the peak of the semi-Gaussian pulse produced by the shaper. It also shows the voltage ramp operation of the Peak Ready comparator and the *Pk_Ready* line going high when the ramp crosses the threshold set at 2.5 V. Finally, a *Reset_In* is issued to simulate the DSP operation and all signals

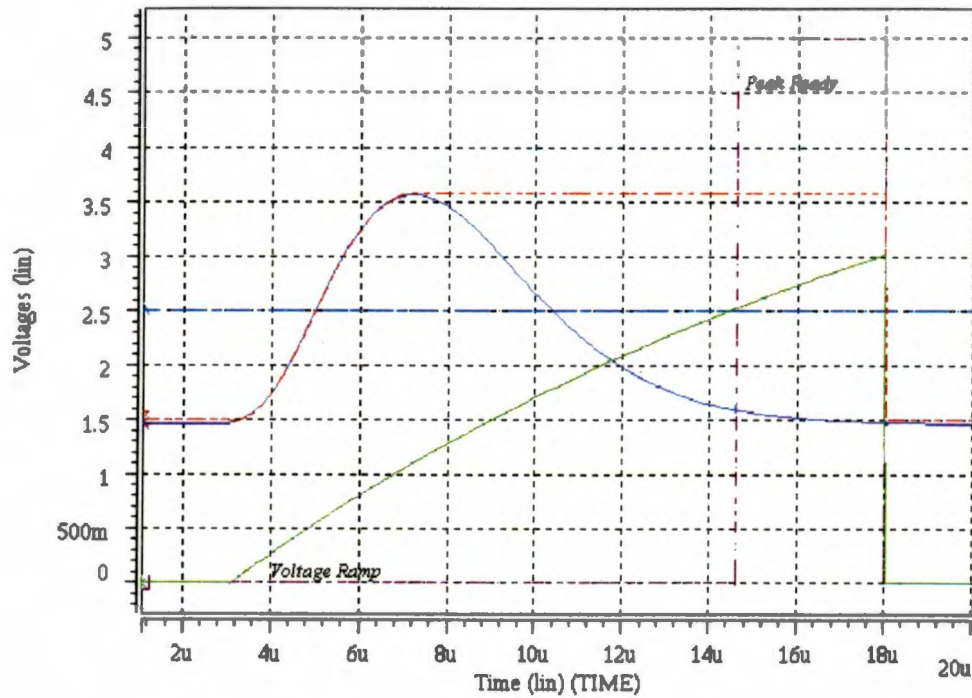


Figure 4.8. Post Layout simulation of PDH system illustrating the operation of the shaper and PDH of the PMT channel.

return to their initial states illustrating that the PDH is ready to process the next pulse.

The PDH test circuit was also tested by connecting its input to the output of the shaper in the SPICE source file.

CHAPTER 5

Experimental Results

5.1 Test Setup

The test board shown in Figure 5.1 was constructed to evaluate the prototype chip. The test circuit shown in Figure 5.2 consisted of the biasing circuitry required for the current sources and for the threshold voltages. Each block was given its own current source and all the threshold voltages were adjustable for maximum freedom when testing. Each V_{DD} pin was jumpered so that blocks could be powered independently and tested independently. Each V_{mid} was also jumpered between a 2.5 V reference generated on the test board and to the B_{LINE} reference voltage generated on the chip. The B_{LINE} reference generator allows V_{mid} to be adjusted so that the dynamic range of the spectroscopy channel could be maximized. The LEMO connectors on the left side are for the input signals and control lines, and the LEMO connectors on the right side are for the output signals. The test board also contains a header to allow easy access to PDH control lines and circuit inputs and outputs for automated testing purposes.

An automated test setup shown in Figure 5.3 was constructed to characterize the linearity of the PDH test circuit and of the complete analog channel. The automated test setup consisted of software written with LabView version 5.1, a National Instruments 6025E data acquisition (DAQ) card, and a passive shaping network. The DAQ card is equipped with two analog output channels, sixteen analog input channels, and digital control lines that are software configurable. To test the linearity, the LabView program

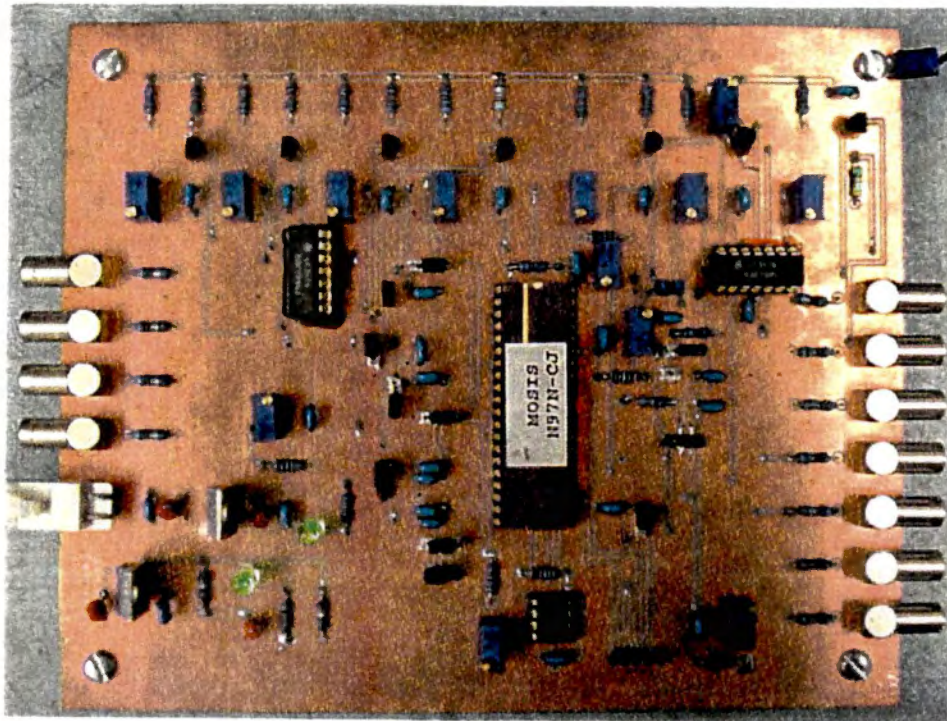


Figure 5.1. ASIC prototype test board.

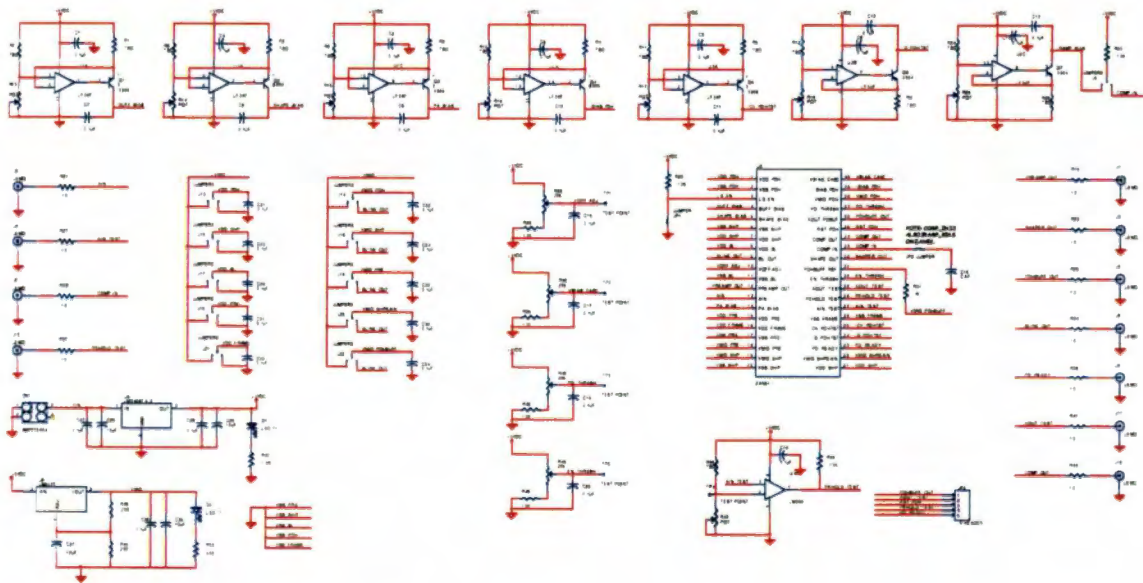


Figure 5.2. Test circuit schematic.

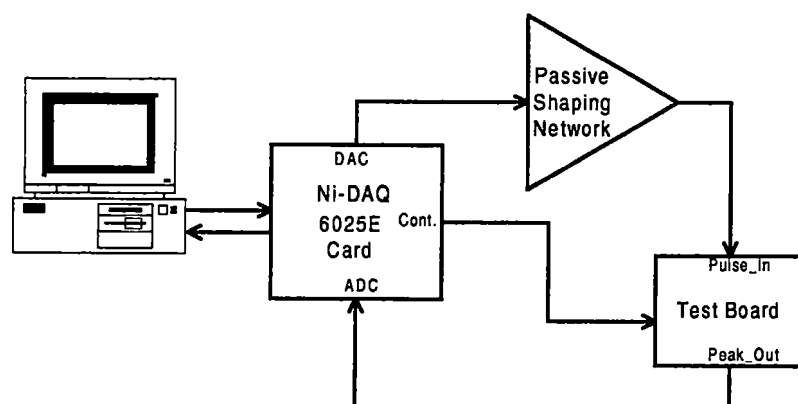


Figure 5.3. Automated test setup used to characterize the PDH test circuit and the PMT channel.

generates the analog input voltage to the test board with the digital-to-analog converter (DAC) and then reads the PDH circuit output voltage with the ADC. This function can be done in a loop to test the PDH circuit over a voltage range at a desired voltage increment.

The analog output voltage produced by the DAC is a step function that is then shaped by a passive filter into a semi-Gaussian pulse. The data is plotted on the graphical user interface (GUI), and it can be stored to a text file. The test program also controls the *Reset_In* signal to the PDH circuit and the *PKHOLD* (Figure 3.22) signal on the PDH test circuit.

The test program is also equipped with a histogram function so that the test setup can be configured to operate as an MCA. In this mode, the program writes the same voltage level out and measures the PDH output. The resulting data is histogrammed so that the peak spread can be measured. Tying the *Pk_Ready* line to the available external trigger allows the test program to function with the test source and the PMT connected to the analog channel.

The automated test setup was used to test the linearity and noise performance of the PDH test circuit and of the analog channel. The PDH test circuit was also evaluated for bandwidth, slew rate, offset voltage, charge injection, and droop using an HP 8013B Pulse Generator, a Tektronix TDS 360 Digital Oscilloscope, and an HP 34401A Digital Multimeter.

5.2 PDH Operation

The PDH test circuit operation was verified in two ways. The first, used with the test setup, was done by injecting a voltage step into a passive shaping network to produce a semi-Gaussian pulse input for the circuit. The second was by connecting the output of the shaper in the analog channel to the PDH test circuit's input. Before injecting the pulse, the I_{ch} current generator was disabled by taking Pk_Hold high, and the test setup had a digital control line to toggle this line. Once the pulse was sample by the PDH test circuit, it was held until the Pk_Hold line went low and enabled the I_{ch} current to discharge C_h at a constant rate. Figure 5.4 shows the PDH test circuit's response to the shaper in the analog channel. The figure shows that the PDH test circuit has a slight offset voltage that causes the output peak to be slightly higher than the input. The linearity analysis to follow will show that this does not significantly affect the linearity.

Figure 5.5 shows the response of the PDH circuit in the analog channel. It also shows the Pk_Ready line going high to notify the DSP section that a peak has been sampled and is ready to be processed. The delay between the peak and the switching of Pk_Ready is controlled by the threshold voltage and by the voltage ramp bias current. The response verified that the PMT channel was functioning properly.

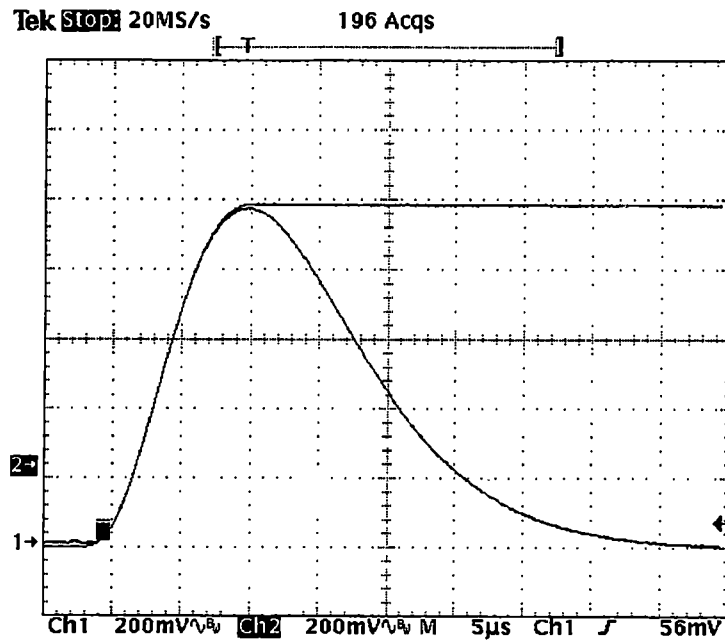


Figure 5.4. PDH test circuit response to the analog channel shaper output.

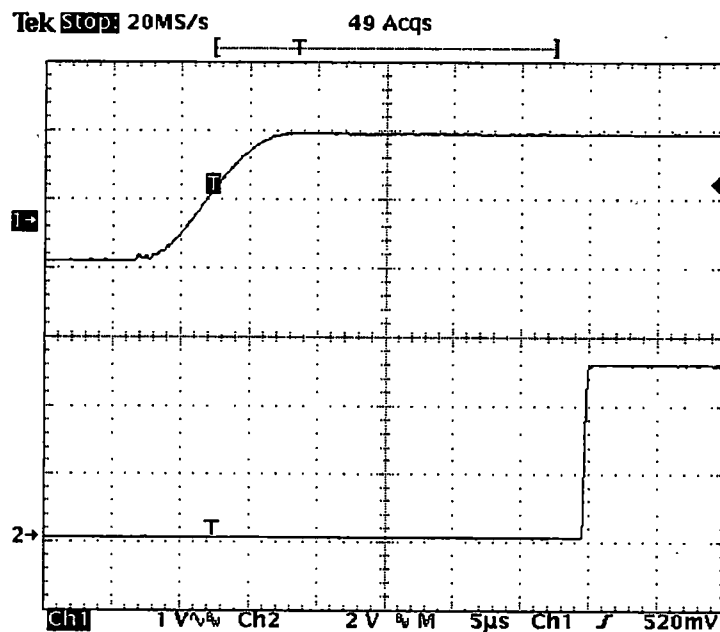


Figure 5.5. PDH circuit response (channel 1) and Pk_Ready (channel 2) illustrating that the PDH system is functioning properly. Pk_Ready is the digital output that notifies the DSP that a peak has been detected.

5.3 Small Signal Results

Figure 5.6 shows the PDH test circuit's response to a 165 mV voltage step. The small signal step response was used to experimentally (for $I_{D10} = 25 \mu\text{A}$) determine the bandwidth and phase margin of the circuit. The circuit rise time (τ_r) was then related to f_c by

$$f_c = \frac{0.35}{\tau_r}, \quad [5.1]$$

where the PDH circuit is assumed to be first order [9]. Figure 5.6 shows that $\tau_r = 43 \text{ ns}$, and Equation 5.1 gives an $f_c = 8.1 \text{ MHz}$. A comparison of the experimental step response with an HSPICE simulation shows that the bandwidth may actually be limited by the large capacitive load at the output of the PDH test circuit rather than by the time constant at node 6 (Figure 3.23).

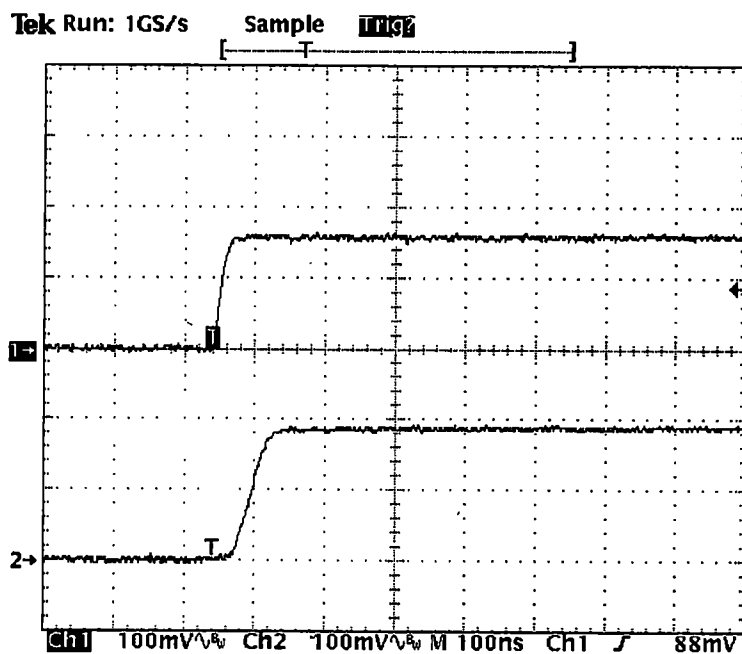


Figure 5.6. PDH test circuit response (channel 2) to a 160 mV step input (channel 1).

The percent overshoot is difficult to measure because the output of the PDH circuit can only increase. There is no settling time involved. Therefore the amount of overshoot was estimated by taking into account the positive offset voltage of the circuit (~ 14 mV) and subtracting it from the difference between the input step voltage and the PDH output voltage. The resulting percent overshoot was measured to be 8 %. This corresponds to a PM of $\sim 65^\circ$ [8, 28], and verifies that the first order approximation is valid. It is also important that the circuit be over-damped because overshoot results in an unwanted signal dependent error when sampling.

5.4 Slew Rate Results

The *SR* was measure by injecting voltage step into the PDH test circuit and measuring the output rise time (10 – 90 %) with the digital oscilloscope. Chapter 3 showed that the *SR* varied over input voltage amplitude, so it was experimentally measured for multiple amplitudes.

The experimental results are shown in Figure 5.7 along with the HSPICE results shown in Chapter 3. The results show good agreement between simulation and experimental measurement. The scope trace shown in Figure 5.8 helps illustrate the cause of the *SR* degradation as the input signal increases. Notice that the output does not increase linearly while the circuit is slewing. Instead, as the output slope decreases as its magnitude increases due to the square law relationship between V_{GS} and I_{DS} of the PDH circuit. The result is a lower *SR* for larger signals.

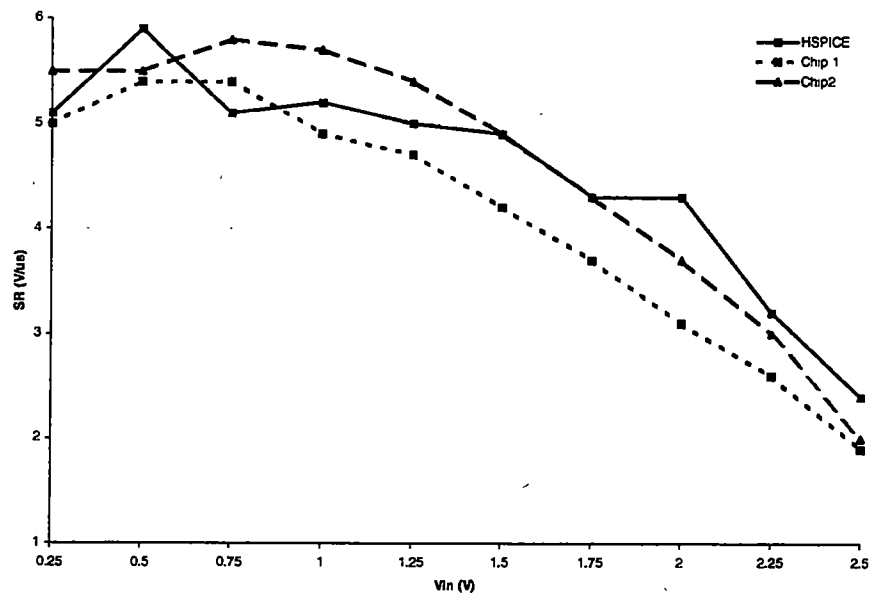


Figure 5.7. Plot of SR versus input voltage magnitude for the PDH test circuit. Experimental results measured on two different chips plotted along with the HSPICE simulation results.

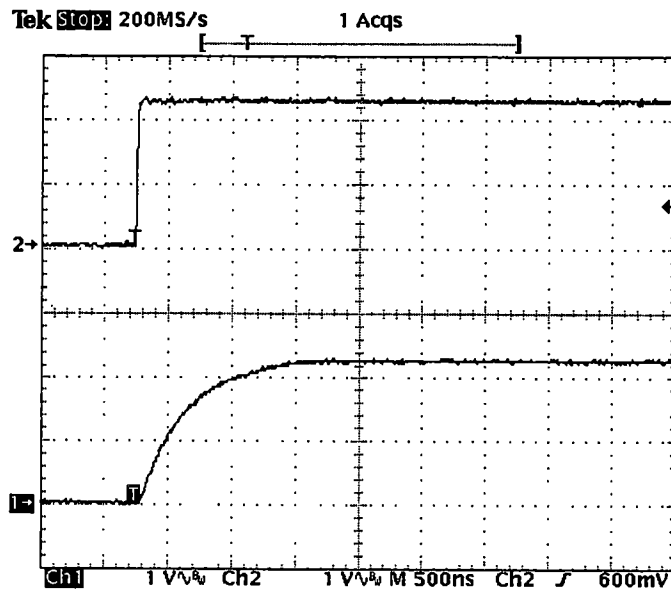


Figure 5.8. Slew rate measurement of the PDH test circuit for a large input signal.

The scope trace shown in Figure 5.8 helps illustrate the cause of the SR degradation as the input signal increases. Notice that the output does not increase linearly while the circuit is slewing. Instead, the output slope decreases as the input voltage amplitude increases due to the square law relationship between V_{GS} and I_{D5} of the PDH circuit. The result is a lower SR for larger signals.

The significant SR decrease at $V_{in} = 2.25$ V is due to a second reason. The SR decreases significantly because M_5 drops out of saturation and no longer functions as a square law device able to deliver a large current to C_h . Instead, it functions as a voltage controlled resistor and the SR response resembles the charging of a large $R_{ds}C_h$ time constant.

The small signal and SR results obtained above are significant because they determine the maximum speed of a signal which the PDH circuit can track. The results show that PDH circuit's SR and bandwidth performance are very good and they do meet the specified requirement over the entire dynamic range.

5.5 Offset Voltage and Charge Injection

The offset voltage was measured versus input bias current using an HP digital voltage meter. As discussed in Chapter 3, the measurement includes the offset voltage error along with the charge injection errors. The experimental results are shown in Figure 5.9 along with the hand calculated and simulation results for comparison. The experimental offset values are slightly higher, but the trend follows that predicted by hand calculation and by simulation. The difference in the experimental results may be due to voltage offset due to device mismatches not taken into account with simulation or hand analysis.

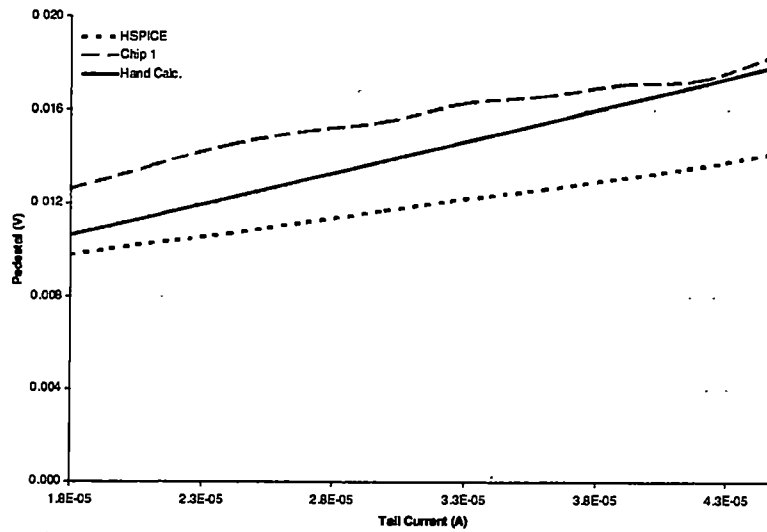


Figure 5.9. Plot of offset voltage versus PDH bias current comparing the hand calculated offset, HSPICE simulated offset, and experimentally measured offset voltages.

Another source of error may be the dependence on the poorly modeled small signal output impedance of the transistors.

The offset analysis in Chapter 3 showed that the PDH circuit has a negative charge injection that was visually illustrated in the HSPICE plot of Figure 3.19. Experimental analysis confirmed that the negative charge injection occurs and is approximately constant (~ 3 mV as HSPICE predicted) over the full dynamic range. However, Figure 5.10 shows the response of the PDH test circuit on channel 1 and the PDH circuit in the PMT channel on channel 2 to the same shaper output pulse. A look at the output shows that the peak of the test circuit does not have the slightly negative voltage change that is inherent in the PDH circuit. This is because M_2 's gate is not connected to C_h in the test circuit, so the negative voltage change at node 3 can not couple to the output through C_{gd2} [30]. Since the negative charge injection is

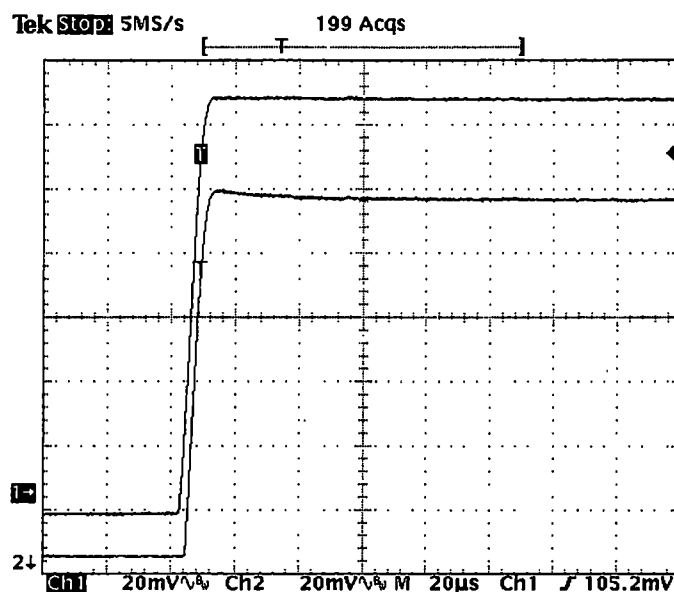


Figure 5.10. Comparison of the response of the PDH test circuit (channel 1) and the PDH circuit within the PMT channel (channel 2) to the same shaper output pulse. The negative charge injection that occurs in the PDH circuit only is illustrated.

approximately constant, it does not affect the linearity of the system. However, the test circuit shows that the error can be eliminated by adding the output stage to the PDH circuit.

5.6 Hold Capacitor Voltage Droop

The voltage droop rate was experimentally measured with the automated test setup discussed above. The pulse amplitude was incremented from 0.25 V to 2.5 V in 0.25 V increments. The ΔV_{out} of the PHD test circuit's output over an 8 ms time period was measured on the oscilloscope at each increment. Figure 5.11 illustrates the droop rate of the PDH circuit at one step. The resulting droop rate measurements are plotted in Figure 5.12. The results show that the droop rate increases with output voltage magnitude. This is expected because of the voltage dependence of the reversed biased

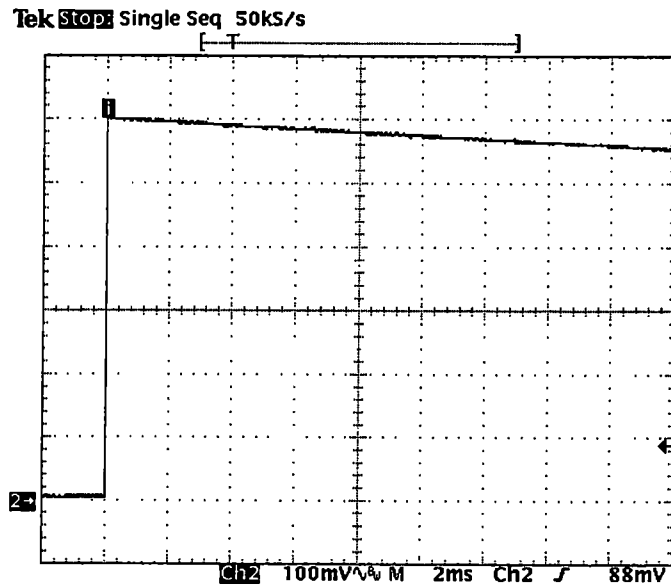


Figure 5.11. PDH test circuit output illustrating the hold voltage droop for a 600 mV output signal.

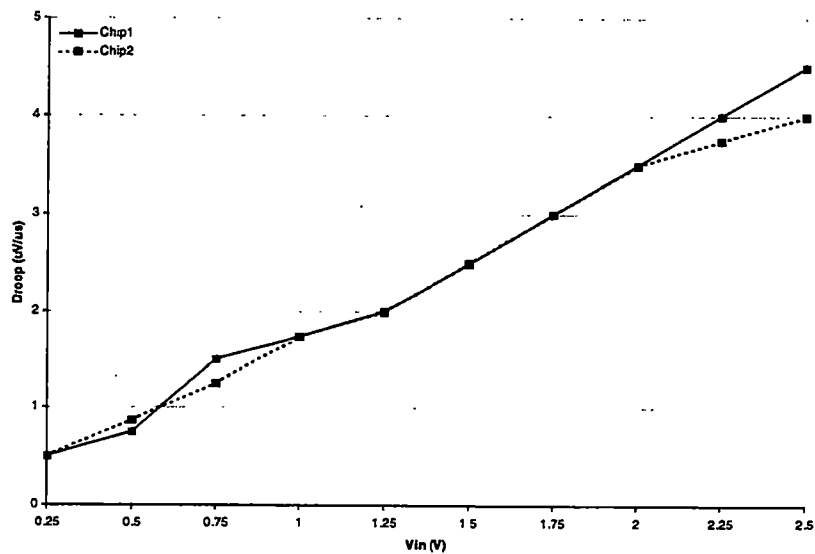


Figure 5.12. Plot of experimentally measured voltage droop versus output signal amplitude.

p - n junctions at the output node discussed in Chapter 3. The leakage current at each point can easily be determined by multiplying the droop rate by C_h . Thus, the worst case leakage current is approximately 11 pA. The results show that the PDH circuit's worst case droop rate is low as expected in MOS sample-and-hold designs, and this error is not a significant factor in the system performance [8].

5.7 Linearity

The linearity of the PDH circuit defines how accurately the PDH circuit can measure a voltage peak over the specified voltage range. The linearity was measured by sweeping the input voltage over a specified dynamic range and measuring the corresponding output voltage ($V_{out,exp}$) with the test system shown in Figure 5.3. The integral non-linearity (INL) of the circuit was then computed by measuring the test circuit output's deviation from an ideal straight line [8,31]. The INL is often quoted as a percentage of the full scale range voltage (V_{FSR}) and is expressed as

$$INL(\%) = \frac{V_{out,exp} - V_{out,ideal}}{V_{FSR}} * 100. \quad (5.3)$$

Typically, the INL is calculated after the offset and gain errors have been removed, but the INL of the PDH test circuit was calculated from the actual measured outputs.

The PDH circuit needs to have 10 bits of accuracy to satisfy the spectroscopy systems requirements. This results in less than a 2.5 mV of deviation from a straight line or $\leq 0.1\%$ INL for the circuit operating over 2.5 V. Since the 6025E DAQ card contains only a 12 bit ADC and a 12 bit DAC operating over a 10 V range, the error of the test setup alone could significantly degrade the INL measurement. Therefore, an error

correction was done to remove the test setups error from the PDH circuits data to ensure that *INL* of the circuit only was measured.

The error of the test setup was measured by removing the PDH circuit from the test loop shown in Figure 5.3, and then running the test program. The error was averaged over several runs. A correction (α_n) factor was then calculated at each point using the following formula

$$\alpha_n = \frac{n * V_{FSR}}{N} - V_{test}(n), \quad (5.4)$$

where N is the number of steps and V_{test} is the specific measurement of the test system at point n . The array of correction factors was then subtracted from the PDH circuit data ($V_{meas,PDH}$) to give a the corrected voltage (V_{cor}) found by

$$V_{cor}(n) = V_{meas,PDH}(n) + \alpha_n. \quad (5.5)$$

The result was substituted into Equation 5.3 for $V_{out,exp}$ to find the *INL*.

The PDH test circuit was used to measure the *INL*. The input voltage was swept from 2 V to 5 V in ~2.9 mV increments. This corresponds to $2^{10} = 1024$ steps. The *INL* was then calculated using the method described above. The *INL* was actually measured for two cases: with and without the cascode transistor operational in the circuit. This enabled the *INL* of both cases to be compared to determine if the addition of the cascode transistor improves the PDH circuit's accuracy.

Figure 5.13 shows a plot of the input voltage versus the measured output voltage (V_{cor}) of the PDH test circuit. The best-fit straight line has been included for a reference. Visibly, the measured output does not deviate from the straight line until the input voltage reaches the upper end of the scale. The slight deviation here is due to the

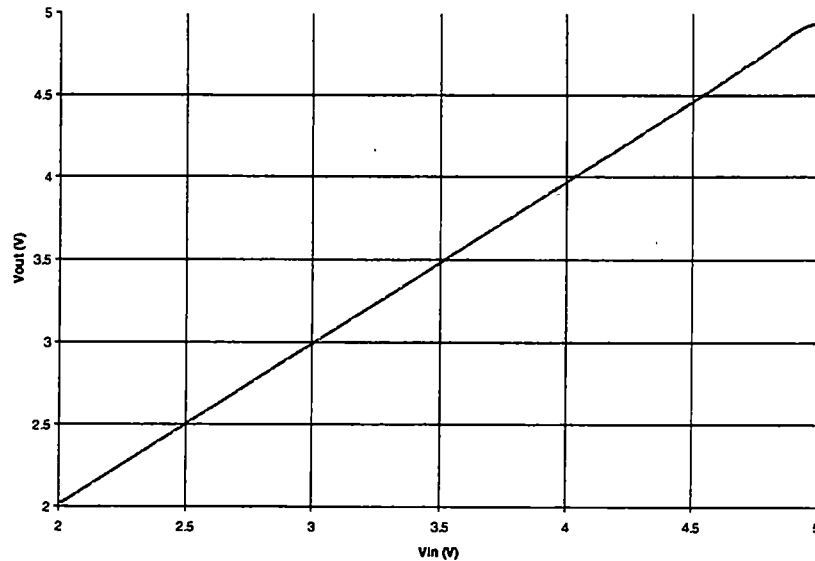


Figure 5.13. PDH test circuit's output voltage versus input voltage with a straight-line reference.

significant decrease in loop gain when M_8 , the load in the output stage (Figure 3.22), drops out of saturation. This sets the upper limit on the dynamic range of the circuit. For the PDH circuit without the output stage, the error is due to M_5 dropping out of saturation.

Figure 5.14 shows the *INL* for both cases, with and without the cascode transistor. The plot shows that the error increases significantly at the end points. The error is greatest at upper end of the voltage range due to the error illustrated in Figure 5.13. The worst case *INL* is typically used to characterize the circuit. Near 5 V, the *INL* is as high as 0.8%. However, over the range of 2.006 V to 4.7 V, the *INL* is <0.12 %. A comparison of the *INL* for the two cases shows that there is no improvement in accuracy due to the addition of the cascode device; actually, the accuracy is slightly worse.

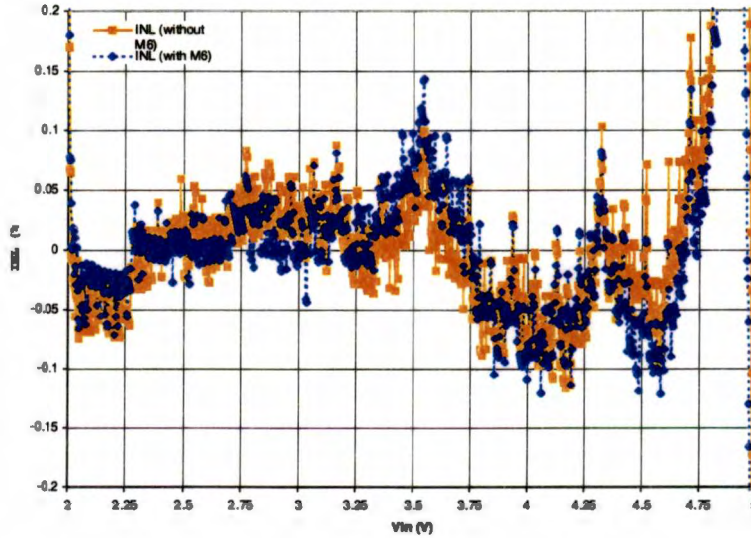


Figure 5.14. INL measurement of PDH test circuit with and without the cascode transistor.

5.8 Pedestal Measurement and Dynamic Range

The *INL* measurement also gives the pedestal values for the circuit. The pedestal is any error that causes the PDH output to deviate from the input when the circuit changes from sample mode to hold mode [8]. Ideally, this error would be signal independent so that the PDH output would not vary from an ideal straight line, but this is not true here. Thus, the pedestals are the source of *INL* as it has been defined here, and the pedestals are primarily due to the charge injection error discussed in Chapter 3. The pedestal voltages (V_{ped}) were found at each point by using the following formula

$$V_{ped} = INL * V_{FSR} . \quad (5.6)$$

For the *INL* of $\pm 0.12\%$, $V_{ped} = \pm 3.2$ mV. This is an error of approximately 1.23 least significant bits (LSB). Again, the large error near the maximum input voltage is not due to pedestal errors but instead the error is due to non-linearity in the circuit gain.

The dynamic range is defined as the range of voltage pulse amplitudes that can be processed by the PDH circuit. The minimum voltage pulse amplitude (V_{min}) is determined by the systematic offset voltage and charge injection discussed in chapter 3. The maximum voltage pulse amplitude (V_{max}) is set by the V_{DD} supply rail for the PDH circuit. If $V_{mid} = 2.5$ V and $I_{D10} = 20$ μ A, then the dynamic range is $V_{max} / V_{min} = 2.5$ V / 13 mV = 190. If the PDH circuit output voltage is limited to 4.7 V to maintain accuracy, then the dynamic range is reduced to 170. However, the dynamic range exceeds the specification.

5.9 Analog Channel Test

The final experiment was the analysis of the PDH system performance with the complete analog channel, a PMT, and a test source. The analog channel, shown in Figure 1.5, was tested with the same source (^{22}Na) and scintillator as that used to obtain the spectra shown in Figure 2.8. The test setup (Figure 5.3) was used to perform the function of the MCA by sampling the output of the PDH and issuing the Reset_In pulse. The LabView software then used a built-in function to build a histogram of the sampled data. Figure 5.15 shows the resulting histogram. The horizontal axis corresponds to the input voltage magnitude rather than the channel number. However, the histogram function divided the input voltage range into 1024 bins (or channels) to correspond to a 10 bit ADC. The large photopeak corresponds to 511 keV gamma rays, and the small photopeak near 5 V is due to 1.2 MeV gamma rays. The noise floor of the system, listed in Figure 5.15, was converted to eV to give an indication of the sensitivity of the analog

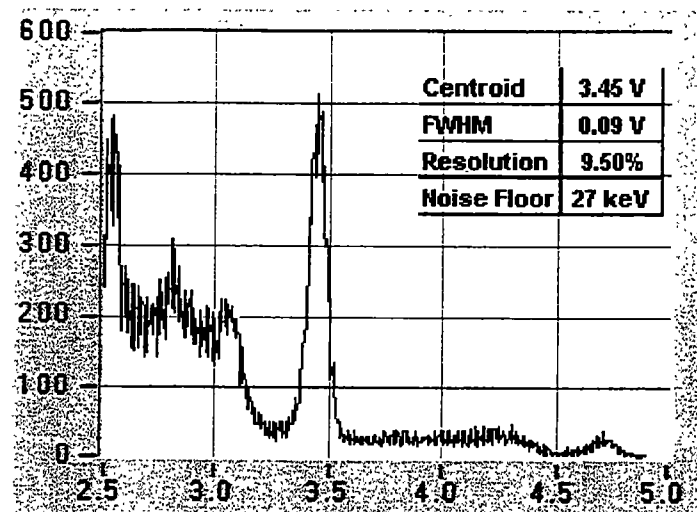


Figure 5.15. PMT spectra for a ^{22}Na source obtained with the prototype analog channel and the test setup.

channel. The noise floor is a bit high, but additional testing with better shielding of the test board and shorter cables for the test setup may result in a lower noise floor.

5.10 Summary of Experimental Results

Table 5.1 summarizes the experimental results presented above, it includes the design specifications presented in Chapter 1, the hand-calculated results, and the HSPICE simulation results where they apply for comparison. The power consumption was experimentally determined by lowering the PDH circuit's bias current until it could no longer track the shaper output accurately, and the quoted value is for the PDH circuit only. If the output stage is included, the power consumption will increase. The offset voltage and dynamic range are quoted for a single bias current, and the worst case *SR* is quoted.

Table 5.1. Summary and comparison of hand calculations, HSPICE simulations, and experimental measurements to the PDH circuit's design specifications.

Parameter	Specification	Hand Calc.	HSPICE	Experimental
Dynamic Range	100:1	-----	-----	170:1
Bandwidth	1.1 MHz	4.0 MHz	3.2 MHz	8.1 MHz
Phase Margin	65°	76°	70°	65°
Slew Rate	1 V/ μ s	-----	2.5 V/ μ s	2 V/ μ s
Pedestal	1.2 mV	-----	-----	3.6 mV
Droop	10 μ V/ μ s	-----	3.3 μ V/ μ s	4.5 μ V/ μ s
Offset Voltage	-----	13 mV	11 mV	15 mV
INL	0.10%	-----	-----	0.12%
Power Cons.	200 μ W	125 μ W	125 μ W	< 100 μ W

The table shows that the hand calculations, HSPICE simulations, and experimental results all show good agreement. The summary also shows that the PDH circuit meets all of the design specifications except the *INL*. The measured *INL* is slightly higher than the specified value.

CHAPTER 6

Conclusion

6.1 Summary

A new CMOS PDH circuit based on the two-stage CMOS op amp topology has been designed and fabricated in the AMI 1.2 μm process. The PDH circuit was designed to operate within the analog channel of a gamma ray spectroscopy system. The experimental results listed in Table 5.1 shows that the PDH circuit exhibited wide bandwidth, good *SR* performance, high dynamic range, and only 0.12 % error while consuming less than 100 μW of power. A PDH test circuit was also designed and fabricated for testing purposes. The PDH test circuit showed that an output stage can be included in the circuit to drive large capacitive loads without degrading the circuit's performance. In addition, Table 5.1 reveals that the experimental evaluation of the PDH circuit showed good agreement with hand calculations and with HSPICE simulations and verifies that the PDH test circuit met the design specifications for operating within the spectroscopy channel.

The PDH system that contained the PDH circuit and the ancillary circuits required to function within the gamma ray spectroscopy system was designed and fabricated. The ancillary circuits designed include a new Linear Gate implemented with a CMOS transmission gate and standard cell logic, two CMOS comparators, and a voltage ramp generator. The PDH system using a new method for determining the occurrence of a peak detection based on pulse rise time only was developed. The new system ensures that no false peaks are detected.

Finally, the new PDH system was fabricated within the PMT analog channel. The experimental testing shows that the analog channel functions properly with a PMT and with the external DSP control signals.

6.2 Future Work

6.2.1 PDH Circuit

Current results indicate that the PDH circuit design is adequate, but there are parts of the design that could be improved. The first area needing further work is the systematic offset voltage. Experimental results showed that the addition of the cascode transistor did not improve the performance of the PDH circuit. The stability requirements on the amplifier can be relaxed so that additional gain could be added to the input stage to reduce the offset voltage.

The second area needing additional attention is the output stage design. The inclusion of the output stage reduces negative charge injection and allows the circuit to drive large capacitive loads. Additional attention needs to be paid to the changes caused by the inclusion of the stage in the feedback loop. The addition of an output stage also requires additional biasing for C_h , and a more elegant method needs to be developed to make the PDH test circuit topology more robust. Care must also be taken to ensure that the output stage does not degrade the frequency response and SR of the PDH circuit.

Another area of investigation is the linearity performance for large signals. This may be tied to the output stage design, but additional work needs to be done to improve the accuracy of the circuit when the output voltage nears V_{DD} .

The design of the control blocks included with the PDH circuit also needs further attention to achieve a more elegant solution. First, a high speed, low offset comparator would improve the PDH Enable function. Second, the comparator in the PK Ready block could be eliminated leaving only a ramp generator and a *D* Flip-Flop, and the threshold of the *D* Flip-Flop would then control the switching in the PK Ready block.

Finally, additional work needs to be done with the PDH block to improve its robustness for use in a portable instrument. For prototyping, all bias currents and threshold voltages were generated independently on the test board. This gave flexibility in experimental testing, but the external components are undesirable for a portable solution because they increase circuit board area. Therefore, a supply independent biasing scheme needs to be added to the next revision to provide stable bias currents and bias voltages on chip.

6.2.2 Analog Channel

The analog channel needs additional work and improvement in a few areas. The first area is testing. The analog channel has been tested with a PMT and a test source, but additional work needs to be done to fully characterize the analog channel's performance. Second, the current prototype chip contains only one analog channel, but the final ASIC will contain at least two analog channels. Thus, the layout of the analog channel needs to be more compact. Finally, a current biasing scheme for the preamplifier and shaper needs to be developed.

6.2.3 System

The DSP section of the spectroscopy system is currently under development. Additional work needs to be done to ensure that the interface between the analog channel

and digital electronics is properly defined. Once the DSP section has been designed, it must be tested with the analog channel. Then the entire system can then be tested with a PMT and gamma ray source. When the complete system is working, a system board, a battery operated power supply, and portable case must be designed and assembled to realize a portable gamma ray spectroscopy system.

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Appendices

Appendix A

MOSIS Process Parameters Used in Pre-fabrication Design

MOSIS PARAMETRIC TEST RESULTS

RUN: N88Z

VENDOR: AMI

TECHNOLOGY: SCN12

FEATURE SIZE: 1.2 microns

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.69	-1.03	Volts
SHORT	10.8/1.2			
Idss		193	-86	uA/um
Vth		0.57	-0.89	Volts
Vpt		10.0	-14.8	Volts
WIDE	30/1.2			
Ids0		0.8	-0.5	pA/um
LARGE	10.8/10.8			
Vth		0.61	-0.87	Volts
Vjbkd		16.9	-15.7	Volts
Ijlk		-26.7	3.8	pA
Gamma		0.64	0.83	V^0.5
Delta length		0.31	-0.03	microns
(drawn - electrical)				
Delta width		1.46	1.53	microns
(drawn - electrical)				
K' (Uo*Cox/2)		35.4	-12.0	uA/V^2

N88Z SPICE LEVEL3 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.0400E-08 XJ=0.200000U TPG=1
+ VTO=0.6081 DELTA=1.3700E+00 LD=9.0910E-10 KP=7.4209E-05
+ UO=653.3 THETA=9.5780E-02 RSH=5.1480E+01 GAMMA=0.6166
+ NSUB=1.4780E+16 NFS=5.9090E+11 VMAX=1.8150E+05 ETA=7.7500E-02
+ KAPPA=2.4680E-01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.4138E-10 CJ=2.8065E-04 MJ=5.3057E-01 CJSW=1.4649E-10
+ MJSW=1.0000E-01 PB=9.7858E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 8.9440E-07
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.0400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8311 DELTA=3.1900E+00 LD=9.0910E-10 KP=1.9344E-05
+ UO=170.3 THETA=1.0050E-01 RSH=3.3060E+01 GAMMA=0.3046
+ NSUB=3.6060E+15 NFS=5.9090E+11 VMAX=1.6930E+05 ETA=8.5870E-02
+ KAPPA=9.9940E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.2737E-10 CJ=2.9597E-04 MJ=4.4146E-01 CJSW=1.4645E-10
+ MJSW=1.0000E-01 PB=7.4913E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 8.2900E-07
```

N88Z SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

* DATE: Oct 19/98

* LOT: n88z WAF: 03

* Temperature_parameters=Default

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 3E-7         NCH     = 7.5E16       TOX      = 3.04E-8
+K1      = 0.9340278    K2      = -0.0670013    VTH0     = 0.5815607
+K3B     = -2.149369    W0      = 2.544414E-7    K3       = 4.2645743
+DVT0W   = 0           DVT1W   = 5.3E6         NLX      = 1.146796E-7
+DVT0    = 1.8024609    DVT1    = 0.4371369    DVT2W    = -0.032
+U0      = 640.0382895  UA      = 1.134603E-9    DVT2     = -0.1548912
+UC      = 6.425777E-11 VSAT   = 1.025002E5    UB       = 4.305021E-18
+AGS     = 0.1089496    B0      = 9.758203E-7    A0       = 0.6075572
+KETA    = -0.0121885   A1      = 0           B1       = 9.451406E-7
+RDSW    = 2.163377E3   PRWG    = -1E-3       A2       = 1
+WR       = 1          WINT     = 6.756618E-7    PRWB     = 6.127803E-3
+DWG      = -1.937825E-8 DWB     = 2.628633E-8    LINT     = 1.125536E-7
+NFACTOR  = 0.4949859   CIT      = 0          VOFF     = -0.0836217
+CDSCD    = 0          CDSCB    = 0          CDSC     = 2.4E-4
+ETAB     = -0.042698   DSUB     = 0.5907438    ETA0     = 0.1365138
+PDIBLC1  = 5.419543E-3 PDIBLC2  = 1.208657E-3    PCLM     = 1.1870837
+DROUT    = 0.0281681   PSCBE1   = 1.072772E9    PDIBLCB  = 0
+PVAG     = 0.0523589   DELTA    = 0.01         PSCBE2   = 5.002526E-9
+PRT      = 0          UTE      = -1.5       MOBMOD   = 1
+KT1L     = 0          KT2      = 0.022      KT1      = -0.11
+UB1      = -7.61E-18   UC1      = -5.6E-11    UA1      = 4.31E-9
+WL       = 0          WLN      = 1          AT       = 3.3E4
+WWN      = 1          WWL      = 0          WW       = 0
+LLN      = 1          LW       = 0          LL      = 0
+LWL      = 0          CAPMOD   = 2         LWN      = 1
+CGSO     = 2.7E-10     CGBO     = 0          CGDO     = 2.7E-10
+PB       = 0.9785784   MJ       = 0.5305733    CJ       = 2.806451E-4
+PSW      = 0.99        MJSW      = 0.1       CJSW     = 1.464911E-10
+PRDSW    = -989.097    PK2      = -5.38285E-3    PVTH0    = -0.0614433
+LKETA    = -9.8354E-4  PAGS     = 0.482296    WKETA    = 4.117011E-3
*)
```

```
.MODEL CMOSP PMOS (
+VERSION = 3.1          TNOM    = 27          LEVEL    = 49
+XJ      = 3E-7         NCH     = 2.4E16       TOX      = 3.04E-8
+K1      = 0.4627141    K2      = -3.916965E-3    VTH0     = -0.8058627
+K3B     = -2.5656586   W0      = 2.209688E-7    K3       = 13.4883082
+DVT0W   = 0           DVT1W   = 5.3E6         NLX      = 6.936779E-7
+DVT0    = 2.431363     DVT1    = 0.5455412    DVT2W    = -0.032
+U0      = 268.4532224  UA      = 4.801783E-9    DVT2     = -0.0725453
+UC      = -1E-10       VSAT   = 1.09645E5     UB       = 4.238494E-18
+AGS     = 0.155562     B0      = 4.547478E-6    A0       = 0.2531802
+KETA    = -0.0135114   A1      = 0           B1       = 1.951094E-6
+RDSW    = 1.45858E3    PRWG    = -1E-3       A2       = 1
+WR       = 1          WINT     = 6.473685E-7    PRWB     = -1E-3
+DWG      = -1.555331E-8 DWB     = 3.228232E-8    LINT     = 9.093131E-9
+NFACTOR  = 0.9890363   CIT      = 0          VOFF     = -0.0672947
+CDSCD    = 0          CDSCB    = 0          CDSC     = 4.036955E-4
+ETAB     = 0          DSUB     = 0.5907438    ETA0     = 0.0188953
```

+ETAB	= 0	DSUB	= 0.0223077	PCLM	= 15
+PDIBLC1	= 0	PDIBLC2	= 1E-5	PDIBLCB	= 0
+DROUT	= 3.896422E-3	PSCBE1	= 1.83251E10	PSCBE2	= 5.004583E-9
+PVAG	= 0	DELTA	= 0.01	MOBMOD	= 1
+PRT	= 0	UTE	= -1.5	KT1	= -0.11
+KT1L	= 0	KT2	= 0.022	UA1	= 4.31E-9
+UB1	= -7.61E-18	UC1	= -5.6E-11	AT	= 3.3E4
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	CGDO	= 2.7E-10
+CGSO	= 2.7E-10	CGBO	= 0	CJ	= 2.959698E-4
+PB	= 0.7491338	MJ	= 0.4414592	CJSW	= 1.464496E-10
+PBSW	= 0.9434007	MJSW	= 0.1	PVTH0	= 0.188273
+PRDSW	= -990	PK2	= -0.0146098	WKETA	= 0.0149993
+LKETA	= 0.0152763	PAGS	= 2.85026	)	
*					

Appendix B

MOSIS Process Parameters from Prototype Chip Run (N97N)

MOSIS PARAMETRIC TEST RESULTS

RUN: N97N
TECHNOLOGY: SCN12

VENDOR: AMI
FEATURE SIZE: 1.2 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.63	-1.06	Volts
SHORT	10.8/1.2			
Idss		222	-91	uA/um
Vth		0.51	-0.98	Volts
Vpt		9.8	-9.4	Volts
WIDE	30/1.2			
Ids0		6.7	-15.5	pA/um
LARGE	10.8/10.8			
Vth		0.59	-0.94	Volts
Vjbkd		17.7	-15.1	Volts
Ijlk		-32.3	-6.8	pA
Gamma		0.66	0.72	V^0.5
K' (Uo*Cox/2)		36.7	-11.6	uA/V^2

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL
-----	-----
SCN (lambda=0.6)	0.00
AMI_ABN	0.00

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.6/2.4			
Vth		0.92	-1.26	Volts
SHORT	7.2/2.4			
Vth		0.90	-1.18	Volts
LARGE	21.6/21.			
Vth		0.90	-1.16	Volts
K' (Uo*Cox/2)		22.5	-7.0	uA/V^2

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta		153	
V_early		36.2	Volts
Vce,sat		0.1	Volts
2X2	2X2		
Beta		155	
V_early		35.5	Volts
Vce,sat		0.1	Volts
2X4	2X4		
Beta		157	
V_early		34.8	Volts
Vce,sat		0.1	Volts
2X8	2X8		
Beta		157	
V_early		34.2	Volts
Vce,sat		0.1	Volts
BVceo		6.8	Volts
BVcbo		28.3	Volts
BVebo		7.8	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Sheet Resistance	53.0	75.6	28.4	26.7	0.06	0.03	1484	ohms/sq
Width Variation (measured - drawn)	-0.64	-0.87	-0.16	0.41	0.50	0.54		microns
Contact Resistance	47.1	35.4	25.3	17.3		0.05		ohms
Gate Oxide Thickness	305							angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	MTL1	POLY	POLY2	MTL2	N_WELL	UNITS
Area (substrate)	290	314	20	38		12	51	aF/um^2
Area (N+active)			51	1132	718	26		aF/um^2
Area (P+active)				1113	708			aF/um^2
Area (poly)			46		603	22		aF/um^2
Area (poly2)			46					aF/um^2
Area (metall)						41		aF/um^2
Fringe (substrate)	73	173	57			49		aF/um

Fringe (poly)	55	43	aF/um
Fringe (metall)		56	aF/um
Overlap (N+active)	168		aF/um
Overlap (P+active)	194		aF/um

CIRCUIT PARAMETERS

	K		UNITS
Inverters			
Vinv	1.0	1.77	Volts
Vinv	1.5	2.10	Volts
Vol (100 uA)	2.0	0.51	Volts
Voh (100 uA)	2.0	4.36	Volts
Vinv	2.0	2.30	Volts
Gain	2.0	-9.71	

Ring Oscillator Freq.

MOSIS (31-stage,5V)	65.60	MHz
DIV64 (31-stage,5V)	65.22	MHz
NON_FEATU (31-stage,5V)	42.28	MHz

Ring Oscillator Power

MOSIS (31-stage,5V)	47.54	uW/MHz/g
DIV64 (31-stage,5V)	0.45	uW/MHz/g
NON_FEATU (31-stage,5V)	0.60	uW/MHz/g

N97N SPICE LEVEL3 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U TPG=1
+ VTO=0.6063 DELTA=4.7620E-01 LD=1.2100E-07 KP=7.6456E-05
+ UO=675.3 THETA=7.9020E-02 RSH=6.8720E+01 GAMMA=0.6693
+ NSUB=1.7300E+16 NFS=5.9080E+11 VMAX=2.0890E+05 ETA=1.2620E-01
+ KAPPA=3.8640E-01 CGDO=2.0549E-10 CGSO=2.0549E-10
+ CGBO=4.4943E-10 CJ=2.8197E-04 MJ=5.3962E-01 CJSW=1.3603E-10
+ MJSW=1.0000E-01 PB=9.9000E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.4000E-06
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9084 DELTA=2.1300E+00 LD=9.0910E-10 KP=2.0436E-05
+ UO=180.5 THETA=7.9360E-02 RSH=2.3050E+01 GAMMA=0.3597
+ NSUB=4.9960E+15 NFS=5.9090E+11 VMAX=1.2600E+05 ETA=1.1130E-01
+ KAPPA=5.6030E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=4.2631E-10 CJ=3.1189E-04 MJ=4.4543E-01 CJSW=1.7631E-10
+ MJSW=1.0000E-01 PB=7.6608E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.2920E-06
```

N97N SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Sep 13/99

* LOT: n97n WAF: 04

* Temperature_parameters=Default

.MODEL CMOSN NMOS (

+VERSION = 3.1	TNOM = 27	LEVEL = 49
+XJ = 3E-7	NCH = 7.5E16	TOX = 3.05E-8
+K1 = 0.9618187	K2 = -0.0803239	VTH0 = 0.54738
+K3B = -1.3828111	W0 = 1E-7	K3 = 3.1303795
+DVT0W = 0	DVT1W = 0	NLX = 1E-8
+DVT0 = 0.5079419	DVT1 = 0.1953651	DVT2W = 0
+U0 = 673.3626374	UA = 2.183409E-9	DVT2 = -0.2188993
+UC = 4.359709E-11	VSAT = 1.106465E5	UB = 5.873701E-21
+AGS = 0.1327497	B0 = 1.268894E-6	A0 = 0.6427102
+KETA = -6.750616E-3	A1 = 0	B1 = 5E-6
+RDSW = 2.797196E3	PRWG = -0.0424904	A2 = 1
+WR = 1	WINT = 7.28535E-7	PRWB = -0.0387081
+XL = 0	XW = 0	LINT = 2.396434E-7
+DWB = 2.495366E-8	VOFF = 0	DWG = -2.052354E-8
+CIT = 0	CDSC = 3.464997E-6	NFACTOR = 0.8346224
+CDSCB = 1.529759E-5	ETA0 = 0.212761	CDSCD = 3.511988E-6
+DSUB = 0.8988941	PCLM = 0.7889076	ETAB = -0.1249183
+PDIBLC2 = 8.897537E-3	PDIBLCB = -9.980199E-4	PDIBLC1 = 0.0212061
+PSCBE1 = 6.432568E8	PSCBE2 = 2.830966E-9	DROUT = 0.1712202
+DELTA = 0.01	MOBMOD = 1	PVAG = 3.384001E-4
+UTE = -1.5	KT1 = -0.11	PRT = 0
+KT2 = 0.022	UA1 = 4.31E-9	KT1L = 0
+UC1 = -5.6E-11	AT = 3.3E4	UB1 = -7.61E-18
+WLN = 1	WW = 0	WL = 0
+WWL = 0	LL = 0	WWN = 1
+LW = 0	LWN = 1	LLN = 1
+CAPMOD = 2	XPART = 0.4	LWL = 0
+CGSO = 1.68E-10	CGBO = 0	CGDO = 1.68E-10
+PB = 0.99	MJ = 0.5396162	CJ = 2.819749E-4
+PBSW = 0.99	MJSW = 0.1	CJSW = 1.360299E-10
+PRDSW = -416.757313	PK2 = -0.010719	PVTH0 = -4.939483E-3
+LKETA = -0.0218162	)	WKETA = 3.974836E-3

*

.MODEL CMOSP PMOS (

+VERSION = 3.1	TNOM = 27	LEVEL = 49
+XJ = 3E-7	NCH = 2.4E16	TOX = 3.05E-8
+K1 = 0.4585903	K2 = -8.926194E-7	VTH0 = -0.8933041
+K3B = -2.1270144	W0 = 7.084747E-7	K3 = 12.5244457
+DVT0W = 0	DVT1W = 0	NLX = 4.803547E-7
+DVT0 = 0.6649312	DVT1 = 0.33158	DVT2W = 0
+U0 = 271.9184429	UA = 5.115542E-9	DVT2 = -0.1723688
+UC = -8.77062E-11	VSAT = 1.281286E5	UB = 1.020281E-20
+AGS = 0.1586454	B0 = 4.735384E-6	A0 = 0.3903969
+KETA = 3.31383E-3	A1 = 0	B1 = 5E-6
+RDSW = 1.86657E3	PRWG = -0.0188598	A2 = 1
+WR = 1	WINT = 7.974775E-7	PRWB = -0.2300469
		LINT = 5.406906E-8

+XL	= 0	XW	= 0	DWG	= -2.981815E-8
+DWB	= 2.893739E-8	VOFF	= -0.0514077	NFACTOR	= 0
+CIT	= 0	CDSC	= 3.625129E-7	CDSCD	= 0
+CDSCB	= 1.439167E-4	ETA0	= 0.0171533	ETAB	= 1.11372E-5
+DSUB	= 0.0212199	PCLM	= 14.78107	PDIBLC1	= 0.0316428
+PDIBLC2	= 1E-3	PDIBLCB	= 1.182067E-3	DROUT	= 0.1821216
+PSCBE1	= 2.804114E10	PSCBE2	= 7.658032E-9	PVAG	= 1.6449348
+DELTA	= 0.01	MOBMOD	= 1	PRT	= 0
+UTE	= -1.5	KT1	= -0.11	KT1L	= 0
+KT2	= 0.022	UA1	= 4.31E-9	UB1	= -7.61E-18
+UC1	= -5.6E-11	AT	= 3.3E4	WL	= 0
+WLN	= 1	WW	= 0	WWN	= 1
+WWL	= 0	LL	= 0	LLN	= 1
+LW	= 0	LWN	= 1	LWL	= 0
+CAPMOD	= 2	XPART.	= 0.4	CGDO	= 1.94E-10
+CGSO	= 1.94E-10	CGBO	= 0	CJ	= 3.118892E-4
+PB	= 0.7660773	MJ	= 0.4454303	CJSW	= 1.763116E-10
+PBSW	= 0.99	MJSW	= 0.1	PVTH0	= 0.0859903
+PRDSW	= -445.1478541	PK2	= 2.096572E-3	WKETA	= 8.056278E-4
+LKETA	= 1.72854E-3	)			
*					

Appendix C

SPICE Source Code and PDH Magic Extraction Files Used in HotSpotter Simulations

Circuit Analysis File

Filename: top_hs1.sp

HotSpotter Top Level Simulation

* POWER SUPPLY CIRCUITRY

VDD1 1011 0 DC 5

VMID1 1031 0 DC 2.5

VSS1 1021 0 DC 0

VDD2 1012 0 DC 5

VMID2 1032 0 DC 2.5

VSS2 1022 0 DC 0

VDD3 1013 0 DC 5

VMID3 1033 0 DC 2.5

VSS3 1023 0 DC 0

RMIDG 134 115 1

VDD4 1014 0 DC 5

*VMID4 1034 0 DC 1.4

RMID4 1034 115 1

VSS4 1024 0 DC 0

VDD5 1015 0 DC 5

VSS5 1025 0 DC 0

VDD6 1016 0 DC 5

VSS6 1026 0 DC 0

* THRESHOLD AND BIAS VOLTAGE CIRCUITRY

Vb_casc 127 0 DC 2.3

Voff_adj 117 0 DC 3.5

Vin+_pa 113 0 DC 2.5

VEN_thr 123 0 DC 2.52

VPD_thr 124 0 DC 2.5

VLG_EN 122 0 DC 5

* BIAS CURRENT CIRCUITRY

Ipa_bias 1011 111 DC 25u

Ishp_bias 1013 118 DC 15u

Ibuf_bias 1014 120 DC 15u

Ipdh_bias 1014 126 DC 4.1u

Ich_bias 1015 153 DC 2u

Iout_bias 154 0 DC 10u

Iinv 133 0 DC 1u

* Load Capacitance

Cpre 112 0 3pF

Cshp 119 0 3pF

Cout 129 0 8pF

Como 132 0 3pF

Comi 133 0 2pF

Cf 110 112 5pF

* INPUT PULSE GENERATOR

Vi+ 200 0 pulse(0 140e-5 2us 1ns 1us 30us 20us)

Cin 200 201 1u

Rin 201 0 1

Gin 110 1031 201 0 1

* RESET_IN PULSE GENERATOR

V_rst 125 0 pulse(5 0 1us .01us .01us .5us 17us)

```

*****
*   PHD TEST CIRCUIT CONTROL
*****
*   Output of Shaper is connected to PDH
*   Test circuit input through Rtestin.
*****

Rtestin 116 150 1
Vhold 156 0 pulse(0 5 .1us .1us .1us 15us 18us)

*****
*   INCLUDE FILES
*****

.include "N88Z.149"
.include top_hs1.spice

*****
*   ANALYSIS CARDS
*****

.OPTIONS LIST NODE POST
.option accurate=1
.OP
*.AC DEC 100 1 1e9
*.DC VB1 .5 1.5 0.1
.tran 100ns 20us
.ic V(2) = 1.5 *V(151) = 2.5
*.print Vdb(2) Vdb(6)

.END

```

Magic Extraction Files

Filename: lingate_hs0.spice

Note: This is the Linear Gate block.

```
** subcircuit definition for lingate_hs0
** extraction file is
** /msd23/allenwc/hotspotter/lingate_hs0.ext
.subckt lingate_hs0 1 3 6 7 8 10 11 13 16
** instance-id:          nanf251_0
x1 2 9 10 4 16 13 12 nanf251
** instance-id:          nanf211_0
x2 14 8 10 16 5 13 nanf211
** instance-id:          dfrf311_0
x3 15 6 10 17 10 7 13 18 8 9 dfrf311
m1 1 4 3 13 cmosn m=5 w=14.40u l=1.20u geo=0
m2 1 5 3 10 cmosp m=6 w=14.40u l=1.20u geo=0
m3 11 4 3 10 cmosp w=2.40u l=1.20u geo=0
c1 5 10 1.2f
c2 16 13 1.0f
c3 7 13 1.6f
c4 10 3 4.6f
c5 10 1 15.8f
c6 13 3 2.4f
c7 6 0 2.1f
c8 10 0 79.3f
c9 11 0 1.6f
c10 13 0 73.2f
c11 16 0 6.0f
c12 1 0 31.7f
c13 3 0 17.3f
c14 4 0 23.2f
c15 5 0 19.4f
c16 7 0 2.2f
c17 8 0 2.8f
c18 9 0 4.3f
*** node listing for subckt: lingate_hs0
** n0                      == idealgnd
** n1                      [u=3] == n1
** n2                      [u=1] == nanf251_0/21
** n3                      [u=4] == n3
** n4                      [u=3] == n4
** n5                      [u=2] == n5
** n6                      [u=2] == n6
```

```

** n7                [u=2]      ==  n7
** n8                [u=3]      ==  n8
** n9                [u=2]      ==  n9
** n10               [u=7]      ==  n10
** n11               [u=2]      ==  n11
** n12               [u=1]      ==  nanf251_0/150
** n13               [u=5]      ==  n13
** n14               [u=1]      ==  nanf211_0/o1
** n15               [u=1]      ==  dfrf311_0/21
** n16               [u=3]      ==  n16
** n17               [u=1]      ==  dfrf311_0/25
** n18               [u=1]      ==  dfrf311_0/28
.ends

```

Filename: pcomp2.spice

Note: This is the Peak Ready block.

```

** subcircuit definition for pcomp2
** extraction file is /msd23/allenwc/hotspotter/pcomp2.ext
.subckt pcomp2 2 3 4 6 9 10 11 12 13 14
** instance-id:      cap3r5_3
x1 13 6 cap3r5
** instance-id:      cap3r5_0
x2 13 6 cap3r5
** instance-id:      cap3r5_4
x3 13 6 cap3r5
** instance-id:      cap3r5_1
x4 13 6 cap3r5
** instance-id:      cap3r5_5
x5 13 6 cap3r5
** instance-id:      cap3r5_2
x6 13 6 cap3r5
c1 6 13 capamilr2 scale=1067.76
c1p 13 0 capamilr2p scale=1067.8
* c1=640.66ff c1p=13.88ff
m1 7 4 5 13 cmosn m=4 w=12.60u l=1.80u geo=0
m2 8 6 5 13 cmosn m=4 w=12.60u l=1.80u geo=0
m3 7 7 10 10 cmosp w=4.80u l=1.20u geo=0
m4 8 7 10 10 cmosp w=4.80u l=1.20u geo=0
m5 6 2 10 10 cmosp w=8.40u l=3.60u geo=0
m7 9 8 10 10 cmosp w=9.00u l=1.20u geo=0
m8 9 3 13 13 cmosn w=16.80u l=1.20u geo=0
m10 5 3 13 13 cmosn m=4 w=19.20u l=4.80u geo=0
m11 12 9 10 10 cmosp w=12.00u l=1.20u geo=0

```

```

m12 12 9 13 13 cmosn w=4.80u l=1.20u geo=0
m20  2 2 10 10 cmosp w=8.40u l=3.60u geo=0
m21 6 11 13 13 cmosn m=2 w=10.20u l=1.20u geo=0
c2  6 13 1.4f
c3  6 13 2.9f
c4  6 13 2.8f
c5 10 8 1.3f
c6 13 3 1.6f
c7 10 9 1.6f
c8 10 6 1.4f
c9  2 0 16.4f
c10 11 0 6.2f
c11 10 0 44.9f
c12 12 0 8.2f
c13 13 0 262.2f
c14 6 0 79.3f
c15 3 0 16.9f
c16 4 0 20.7f
c17 5 0 17.6f
c18 7 0 10.6f
c19 8 0 12.2f
c20 9 0 8.1f

```

*** node listing for subckt: pcomp2

```

** n0 == idealgnd
** n2 [u=4] == 8_153_228#
** n3 [u=3] == n3
** n4 [u=2] == n4
** n5 [u=3] == n5
** n6 [u=11] == n6
** n7 [u=4] == n7
** n8 [u=3] == n8
** n9 [u=5] == n9
** n10 [u=13] == n10
** n11 [u=2] == 8_107_32#
** n12 [u=3] == n12
** n13 [u=18] == n13
** n14 [u=1] == 9_442_25#
.ends

```

Filename: comp_hs0.spice

Note: This is the PDH Enable block.

```
** subcircuit definition for comp_hs0
** extraction file is /msd23/allenwc/hotspotter/comp_hs0.ext
.subckt comp_hs0 3 4 6 10 12 13
m1 7 4 5 13 cmosn m=4 w=12.60u l=1.80u geo=0
m2 8 6 5 13 cmosn m=4 w=12.60u l=1.80u geo=0
m3 7 7 10 10 cmosp w=4.80u l=1.20u geo=0
m4 8 7 10 10 cmosp w=4.80u l=1.20u geo=0
m7 9 8 10 10 cmosp w=9.00u l=1.20u geo=0
m8 9 3 13 13 cmosn w=16.80u l=1.20u geo=0
m10 5 3 13 13 cmosn m=4 w=19.20u l=4.80u geo=0
m11 12 9 10 10 cmosp w=12.00u l=1.20u geo=0
m12 12 9 13 13 cmosn w=4.80u l=1.20u geo=0
c1 13 3 1.3f
c2 10 9 1.6f
c3 10 8 1.2f
c4 10 0 33.8f
c5 12 0 4.1f
c6 13 0 36.0f
c7 3 0 15.1f
c8 4 0 17.8f
c9 5 0 17.6f
c10 6 0 18.2f
c11 7 0 10.6f
c12 8 0 12.2f
c13 9 0 8.1f
*** node listing for subckt: comp_hs0
** n0 == idealgnd
** n3 [u=3] == n3
** n4 [u=2] == n4
** n5 [u=3] == n5
** n6 [u=2] == n6
** n7 [u=4] == n7
** n8 [u=3] == n8
** n9 [u=4] == n9
** n10 [u=9] == n10
** n12 [u=3] == n12
** n13 [u=9] == n13
.ends
```

Filename: ppdh2_hs0.spice

Note: This is the PDH circuit.

```
** subcircuit definition for ppdh2_hs0
** extraction file is
/msd23/allenwc/hotspotter/ppdh2_hs0.ext
.subckt ppdh2_hs0 5 6 7 10 11 12 13 14
c1 7 10 capamilr2 scale=334.08
c1p 10 0 capamilr2p scale=334.1
* c1=200.45ff c1p=4.34ff
c2 6 11 capamilr2 scale=3709.44
c2p 11 0 capamilr2p scale=927.4
* c2=2225.66ff c2p=12.06ff
m1 2 5 1 13 cmosn m=4 w=14.40u l=1.80u geo=0
m2 3 6 1 13 cmosn m=4 w=14.40u l=1.80u geo=0
m3 2 3 10 10 cmosp w=10.20u l=1.80u geo=0
m4 3 3 10 10 cmosp w=10.20u l=1.80u geo=0
m5 8 2 10 10 cmosp w=2.40u l=2.40u geo=0
m6 6 7 8 10 cmosp w=9.60u l=2.40u geo=0
m7 6 12 11 13 cmosn w=9.60u l=2.40u geo=0
m10 1 14 13 13 cmosn m=6 w=19.20u l=4.80u geo=0
c3 14 1 1.8f
c4 10 6 2.4f
c5 6 11 3.6f
c6 13 10 2.8f
c7 10 0 68.3f
c8 11 0 42.8f
c9 12 0 12.9f
c10 13 0 56.9f
c11 14 0 18.4f
c12 1 0 21.4f
c13 2 0 16.3f
c14 3 0 8.5f
c15 5 0 19.2f
c16 6 0 76.7f
c17 7 0 7.7f
c18 8 0 1.9f
*** node listing for subckt: ppdh2_hs0
** n0 == idealgnd
** n1 [u=3] == n1
** n2 [u=3] == n2
** n3 [u=4] == n3
** n5 [u=2] == n5
** n6 [u=5] == n4
** n7 [u=3] == n7
```

```

** n8                [u=2]      ==  n8
** n10               [u=9]      ==  n10
** n11               [u=3]      ==  n11
** n12               [u=2]      ==  n12
** n13               [u=6]      ==  n13
** n14               [u=2]      ==  n14
.ends

```

Filename: ppdhout_hs0.spice

Note: This is the PDH test circuit.

```

** subcircuit definition for ppdhout_hs0
** extraction file is
** /msd23/allenwc/hotspotter/ppdhout_hs0.ext
.subckt ppdhout_hs0 4 5 7 14 15 17 18 101 102
c1 7 101 capamilr2 scale=334.08
c1p 101 0 capamilr2p scale=334.1
* c1=200.45ff c1p=4.34ff
c2 6 102 capamilr2 scale=3709.44
c2p 102 0 capamilr2p scale=927.4
* c2=2225.66ff c2p=12.06ff
m1 2 5 1 102 cmosn m=4 w=14.40u l=1.80u geo=0
m2 3 4 1 102 cmosn m=4 w=14.40u l=1.80u geo=0
m3 2 3 101 101 cmosp w=10.20u l=1.80u geo=0
m4 3 3 101 101 cmosp w=10.20u l=1.80u geo=0
m5 8 2 101 101 cmosp w=3.00u l=2.40u geo=0
m6 6 7 8 101 cmosp w=9.60u l=2.40u geo=0
m7 4 6 102 101 cmosp m=5 w=30.00u l=1.80u geo=0
m8 4 17 101 101 cmosp m=5 w=19.20u l=3.60u geo=0
m10 1 14 102 102 cmosn m=6 w=19.20u l=4.80u geo=0
m11 15 15 102 102 cmosn m=2 w=9.60u l=4.80u geo=0
m12 15 18 102 102 cmosn w=9.60u l=1.80u geo=0
m13 6 15 102 102 cmosn w=9.60u l=4.80u geo=0
c3 102 4 1.1f
c4 17 7 2.4f
c5 1 14 1.8f
c6 102 6 4.3f
c7 102 101 2.6f
c8 101 0 89.0f
c9 102 0 113.3f
c10 14 0 18.4f
c11 15 0 17.8f
c12 4 0 51.0f
c13 17 0 14.3f
c14 18 0 5.0f

```

```

c15 1 0 21.4f
c16 2 0 13.6f
c17 3 0 9.8f
c18 5 0 19.2f
c19 6 0 62.7f
c20 7 0 13.6f
c21 8 0 1.9f
*** node listing for subckt:  ppdhout_hs0
** n0                      ==  idealgnd
** n1                      [u=3]    ==  n1
** n2                      [u=3]    ==  n2
** n3                      [u=4]    ==  n3
** n4                      [u=4]    ==  n4
** n5                      [u=2]    ==  n5
** n6                      [u=4]    ==  n6
** n7                      [u=3]    ==  n7
** n8                      [u=2]    ==  n8
** n14                    [u=2]    ==  n14
** n15                    [u=5]    ==  n15
** n17                    [u=2]    ==  n17
** n18                    [u=2]    ==  n18
** n101                   [u=12]   ==  n101
** n102                   [u=13]   ==  n102
.ends

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Vita

Wade Christopher Allen was born on February 22, 1974 in Connersville, Indiana. He grew up in nearby Cambridge City, Indiana and attended Temple Christian School, where he graduated in May 1992. He entered Asbury College in Wilmore, Kentucky in August 1992 and began study in a 3-2 joint program with the University of Kentucky's College of Engineering. After three years at Asbury College, he entered the University of Kentucky's College of Engineering in August 1995. While at the University of Kentucky, he participated in the cooperative education program by spending three semesters working in the Monolithic System Group at the Oak Ridge National Laboratory in Oak Ridge, Tennessee. He received a B.A. in Physical Science from Asbury College in August 1996, and then he received a B.S. in Electrical Engineering from the University of Kentucky in May 1998. He then entered the University of Tennessee at Knoxville and participated in the UT/ORNL Joint Program in Mixed Signal VLSI and Monolithic Sensor Design where he received his Master of Science in Electrical Engineering in December 1999.