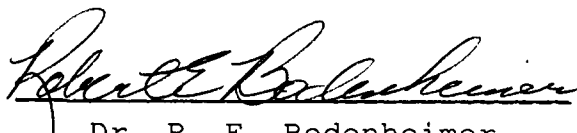


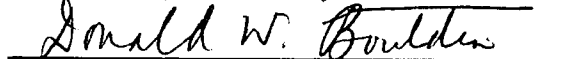
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DESIGN VERIFICATION TEST METHODS
FOR ANALOG INPUT DEVICES

A Thesis
Presented for the
Master of Engineering
Degree
The University of Tennessee, Knoxville

Mack A. Marshall

June 1988

ABSTRACT

Successful manufacturers need to introduce reliable products to the marketplace in a timely manner. This need is met through efficient design-assurance testing. Design-assurance test methods for analog input devices were developed in a design-assurance environment from Winter 1984 through Autumn 1987. Industry test standards and analog input design techniques were researched. Test cycles were monitored and analyzed for efficiency. Test methods were refined to increase test coverage and decrease test cycle time. The resulting test methods comprise an efficient approach to design-assurance testing of analog input devices. Although these methods are tailored specifically for analog input devices, the fundamental methodology can be extended to other product types.

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CHAPTER 1

INTRODUCTION

Realizing sales are driven by customer beliefs, many leading high-technology manufacturers are striving to improve their quality image. Extensive advertising campaigns have been undertaken by Ford Motor Company and others to promote company commitment to quality. Sales tools, particularly in industrial markets, have been expanded to include system reliability predictions. Warranty periods, perceived by customers as direct reflections of reliability, have been extended to unprecedented lengths. Claims of customer satisfaction, low customer-down times, and on-time deliveries are prevalent. Quality-image improvement has become a major goal of many manufacturers.

A successful company not only claims high levels of quality, reliability, and customer satisfaction, but also meets these claims by providing safe, reliable products which satisfy customer requirements. To aid in the reliability effort, many companies recently implemented formal quality training programs such as Juran training and Taguchi methodology. Structured analysis and design techniques, such as

Yourdon methodology, were introduced to improve software maintainability and reliability. Quality and Reliability Assurance groups were strengthened to ensure product specifications are met. Successful companies regard product reliability as necessary for continued business success. (1)

Manufacturers desiring high reliability generally perform a thorough evaluation of a new product and minimize all known reliability risks before releasing the product for customer use. This evaluation is typically performed by a design-assurance team, and may involve several iterations as the product undergoes corrective design changes. Although methods vary between companies, the common goal of design-assurance teams is to ensure products meet or exceed all relevant published specifications, and function in a safe, predictable manner. However, since most new products are needed in the marketplace as soon as possible, lengthy evaluation periods are not desirable. Thus, a design-assurance engineer is faced with the challenge to maximize evaluation coverage and minimize evaluation time.

This thesis presents several key test methods for efficiently evaluating analog input devices, products which measure analog signals and convert them to digital data. General test preparations are discussed

in Chapter 2, while functional test methods are presented in Chapter 3. Chapter 4 focuses entirely on accuracy and repeatability measurements and includes a discussion of an automated test procedure. Environmental and electrical noise tests methods are given in Chapter 5 followed by a brief conclusion presented in Chapter 6. These test methods are intended to provide thorough test coverage with reasonable test length.

CHAPTER 2

PREPARATION

Careful preparation is essential for efficient design-assurance testing. Planning should begin as early as possible in the design cycle. Even as the product is being conceived, long before hardware becomes available, the design-assurance engineer should be an active team member working with design and marketing personnel to ensure the product addresses the desired market. Customer surveys, if done correctly, and competitive product literature indicate current market needs and expectations. Further useful information can often be obtained from manufacturers of transducers. For example, a list of top selling thermocouple types from a major supplier would be welcomed by a team faced with the task of providing an input device capable of only one thermocouple type. Defining correct product requirements is crucial, because if a market need is not satisfied, the product will surely fail.

As soon as all specifications are agreed upon, they should be documented along with related market analysis, cost goals, and other pertinent information. This document should be signed by all personnel

responsible for the project, and should contain all the necessary information for designing and testing the product. Specifications should be presented from a customer viewpoint so they can be adapted easily into a user manual. Additionally, specifications should conform to those of previous similar products or to industry standards if they exist. Proper documentation of the product requirements facilitates design, design-assurance testing, and user-manual generation, and minimizes changes during product development due to misunderstandings.

After the product requirements are understood and documented, a test plan and a test procedure should be generated. The test plan should include a high-level description of the tests required and a summary of who will perform each test. The test plan should be published to the team as soon as possible so that any scheduling conflicts can be addressed. A sample test plan is shown in Figure 2-1.

The test procedure should contain a detailed, step-by-step description of the tests to be performed, a list of equipment required for each test, data sheets for logging test results, and pass/fail criteria. The test procedure should be a published document approved by the design-assurance engineer. Care must be taken to provide adequate test coverage

Test	Responsibility	Estimated Test Time (days)

FUNCTIONAL:		
Accuracy	Design Assurance	5
Repeatability	Design Assurance	2
Calibration	Systems	1
Error Words	Systems	1
Channel Interference	Systems	3
Power Variation	Systems	2
Manual Verification	Systems	10
ENVIRONMENTAL:		
Storage	Design Assurance	8
Moisture	Design Assurance	10
Thermal Shock	Design Assurance	3
Vibration	Design Assurance	1
Temperature Cycle	Design Assurance	3
Humidity	Design Assurance	7
NOISE:		
Conducted	Design	10
Radiated	Design	3
ESD	Design	1

Figure 2-1. Sample Test Plan for an Analog Input Device.

with minimal test effort. Automated test methods should be attempted only if a considerable savings is anticipated. In addition to the initial verification, the test procedure will be useful for evaluating design changes throughout the life of the product.

As soon as the test plan and procedure are complete, manpower and test equipment requirements should be estimated and published. Assignment of personnel to a project generally depends upon availability, project priority, business conditions,

and business strategy. The method of obtaining equipment will depend on the circumstances. Most often, a manufacturer of analog input devices will own the general-purpose test equipment, such as temperature chambers, power supplies, and oscilloscopes, but will lack the specialized test equipment for certain applications. Special test equipment, such as resistance-temperature-detector (RTD) simulators and thermocouple simulators, can be very expensive, especially when high degrees of accuracy are required. Test equipment acquisition should be carefully planned.

Options for obtaining test equipment include securing on-site equipment, leasing, purchasing, and securing off-site equipment. A search should be conducted throughout the site for the necessary test equipment, and if found, the availability of this equipment should be determined. If on-site equipment is unavailable, leasing or purchasing might be desirable. Leasing offers the advantage of no capital expense, but becomes unattractive when schedule slips occur. Purchasing may result in a substantial outlay of cash, but offers the advantage of availability if a retest is required. Furthermore, specialized equipment can usually be passed on to production personnel as a test/troubleshoot aid or kept for testing future

similar projects. If none of the above approaches are satisfactory, off-site testing should be considered. Many private facilities exist for performing custom as well as standard tests. In fact, some regulatory agencies, such as Underwriters Laboratories (UL) and Canadian Standards Association (CSA), may require products to be sent to their labs for evaluation before granting approval. Off-site testing is most attractive to small companies with low capital investments or to companies featuring a small number of product types.

Other actions can be taken by design and design-assurance engineers prior to hardware availability. These actions include stress analysis, reliability prediction, worst-case circuit analysis, review of single- and sole-sourced parts, and plan for problem documentation. Stress analysis can be performed on paper by verifying each component remains well below its recommended maximum power consumption during worst-case conditions. Stress calculations can be further applied in reliability-prediction techniques such as Military Standard MIL-HDBK-217D, Reliability Prediction of Electronic Equipment. A worst-case circuit analysis should always be performed on paper. Test units are unlikely to reflect worst-case conditions. Therefore, calculation of

accuracy errors and timing margins is often the sole indicator of a potential problem, especially when dealing with analog circuitry. Single-source parts (those having multiple sources, yet only one approved for use) and sole-source parts (those having only one source) are undesirable from a maintainability standpoint, and their use should be avoided if possible. To avoid confusion during the test cycle, the method of reporting and dispositioning problems should be understood by team members before any testing begins. (2)

Often, design-assurance testing can begin on engineering prototypes. This approach allows the tester to become familiar with the product. Also, problems can be found early in the design cycle where they are most easily corrected. However, the tester should be cautioned against performing final verification tests using engineering prototypes. Final version assemblies should be verified, since etch and component placement are often critical to proper circuit operation. Furthermore, the final verification devices should be manufactured by the same process intended for production. A unit assembled in an engineering environment does not, in general, reflect a unit assembled by a manufacturing line. In effect, a

manufacturing-process audit and a product design verification are conducted simultaneously.

Efficient design-assurance testing can only be accomplished through careful preparation. Planning should start as early as possible in the design cycle. All aspects of the test effort should be addressed and understood prior to actually beginning the tests. Preparation is key to a successful design-assurance test phase.

CHAPTER 3

FUNCTIONAL VERIFICATION

In functional verification, all the product features are exercised, and the product's performance is evaluated. Unlike environmental and electrical noise tests, which are essentially unchanged for a variety of products, functional testing requires thorough product knowledge and varies as the product features vary. The purpose of this chapter is to discuss functional verification as applied to analog input devices and to present functional test methods. Features typically controlled by software are discussed first followed by effects of power source variation and user misapplications. Finally, accuracy and repeatability are briefly discussed while a more thorough discussion is presented in Chapter 4.

Generally, functions which depend solely on software (firmware) can be evaluated at any convenient, benign environment within the specified operating range. Of course, the hardware running the software must be verified to operate properly throughout the specified environment as explained in Chapter 5. Additionally, some software functions might require testing in a special environment. For example,

communication error detection should be evaluated in an electrically noisy environment.

Functions typically found under software control for analog input devices include user programming, error reporting, and control of channel update times. Often devices must be programmed by the user to select appropriate options for the application at hand. An example of available options for a thermocouple input device is shown in Table 3-1. Programming information

Table 3-1. Configuration Options for a Thermocouple Input Device.

Thermocouple Type	!	Range	!	Configuration Code
J	!	Full	!	0
J	!	Half	!	1
K	!	Full	!	2
K	!	Half	!	3
T	!	Full	!	4
T	!	Half	!	5
S	!	Full	!	6
S	!	Half	!	7

can be retained by the device in several ways ranging from simple jumper placement to more complicated storage in electrically-eraseable-programmable-read-only-memory (EEPROM). The device should be tested by selecting all option types and verifying the correct responses are made and the correct mode is invoked.

User friendliness and user documentation should be considered. Although the specification might be met, a more efficient method for programming the device might exist.

Some devices are capable of reporting errors. Problems external to the device, within the device, or both can be reported. Internal error detection is a result of self diagnostics. A device may perform thorough diagnostics upon power application or reset, and may continue to perform limited diagnostics in a background mode during operation. If an error is detected, the device notifies the user or host device by providing visible indication, sending an error code, or both. In some devices, the error code is reported in the same location normally reserved for data, but is distinguishable from valid data in some way. Figure 3-1 illustrates one such arrangement in which the sign bit of a 16-bit word is used to distinguish data from error codes. This enforces the

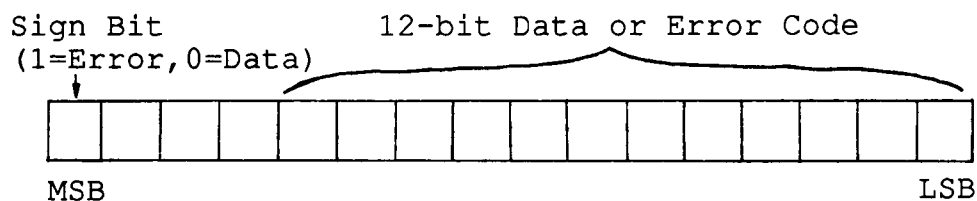


Figure 3-1. Common Location for Data and Error Information.

understanding that the data cannot be trusted if an error occurs. A sample list of error codes for a resistance temperature detector (RTD) input device is given in Table 3-2. Each of the error codes should be

Table 3-2. Error-code List for RTD Input Device.

Error Code	!	Error
-1	!	RTD Probe Shorted
-2	!	RTD Probe Open
-3	!	Input Under Range
-4	!	Input Over Range
-5	!	External Supply Out of Range
-6	!	Communications Error with Host
-7	!	EEPROM Data Altered
-8	!	RAM Failure
-9	!	ROM Failure

artificially induced. If a correct response does not occur, the device has failed. After verification, the list of error codes should be included with the user documentation.

The update time for a channel is the time between any two consecutive readings for that channel. Figure 3-2 illustrates the concept of update time for a single channel device, a multi-channel device with parallel processing, and a multi-channel device with serial processing. One method of measuring update times is to connect an oscilloscope probe to the

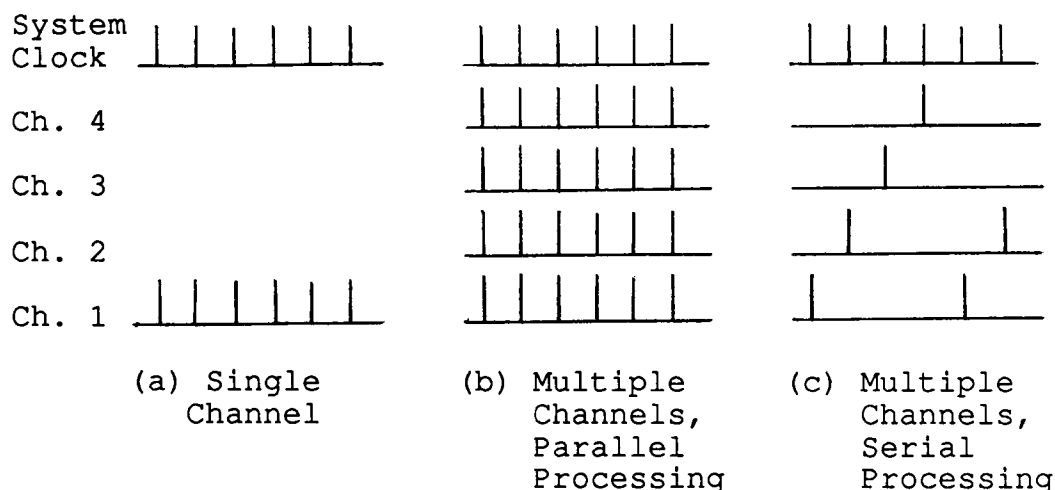


Figure 3-2. Update Times.

signal which triggers the start of a new sample period and measure the time between pulses. A simpler method which requires no knowledge of internal signals is to monitor the host device for a given channel while varying the input to that channel in a continuous and monotonic fashion as shown in Figure 3-3. The time between changes in the readings is the update time. Each channel should be tested to ensure the update time agrees with specified performance.

Many multi-channel devices, particularly those employing serial processing, utilize common circuitry for reporting data from multiple channels. Therefore, the data from each channel must be verified to reach the proper location. A sample test setup is shown in Figure 3-4 for performing this channel logic

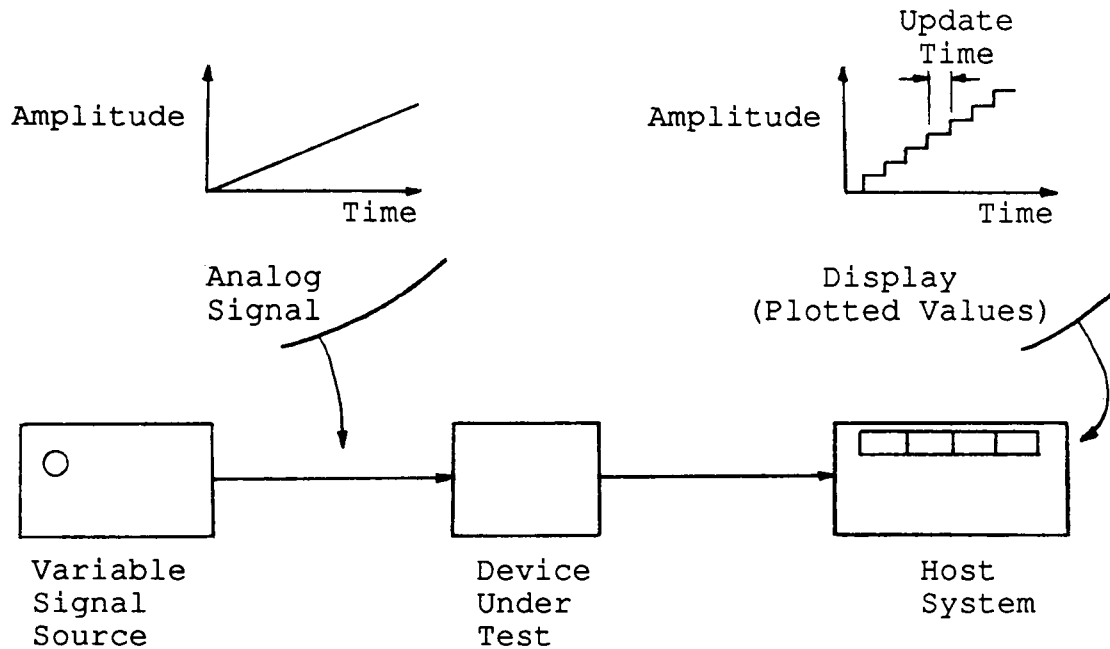


Figure 3-3. Update Time Test Configuration.

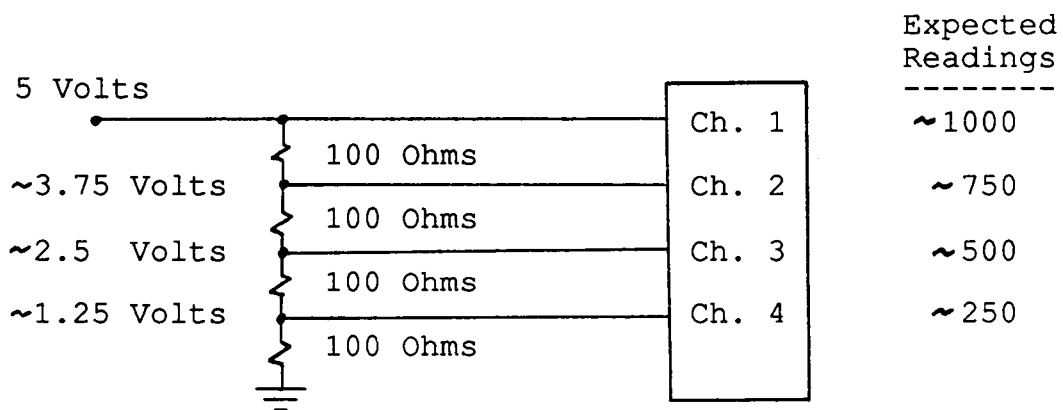
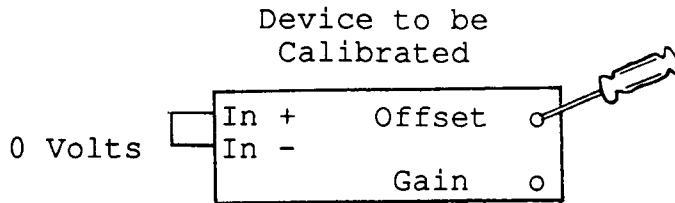


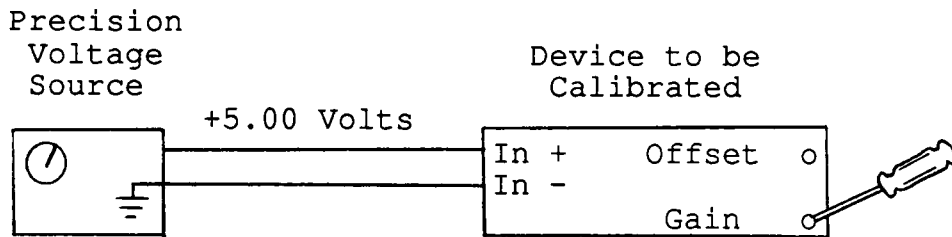
Figure 3-4. Channel Logic Verification for a Four-channel 0- to 5-volt Analog Input Device.

verification for a four-channel, 0- to 5-volt analog input device. In this case, the digital readings produced are linearly scaled integers ranging from 0 to 1000 corresponding to inputs from 0 to 5 volts respectively. For each channel, the actual reading should be compared with the expected value to ensure the results are properly placed. This approach can be adapted to other types of analog input devices.

Some analog input devices are self-calibrating in which case the accuracy is based upon some precise reference which remains essentially constant throughout the desired operating environment. Others may be calibrated with an external signal using potentiometers, variable capacitors, or removable (clip-out) discrete components. Calibration on others might be accomplished through software and an external source by storing parameters within the device to adjust internal references. Figure 3-5 illustrates a typical calibration setup requiring an external precision voltage source and a non-metallic screwdriver. In this example, the offset is adjusted first while the input is 0 volts (shorted). The gain is adjusted next while applying 5.00 volts to the input.



(a). Offset Adjust.



(b). Gain Adjust.

Figure 3-5. Typical Calibration Setup.

Although many calibration methods exist, one procedure for verifying all methods is to perform the specified calibration and ensure accuracy is retained throughout the specified operating conditions. Parameters stored in EEPROM or non-volatile random access memory (NOVRAM) are most likely to exhibit problems during power cycles or power glitches. Calibration methods based on variable components are more likely to have trouble during thermal shock where varying temperature gradients can cause unprovoked adjustment changes. For example, the wiper of a wire-

wound potentiometer might alternate between two adjacent windings due to induced temperature gradients and thermal expansion properties of the component. If field calibration is allowed, the calibration procedure should be checked for user friendliness and user manual correctness. Calibration verification consists of properly calibrating the device under test and checking the calibration following the performance of other tests.

For multi-channel devices, or multiple single channel devices sharing the same bus, the effects of one channel upon another should be determined. These effects should be evaluated for common failure modes as well as normal operating conditions. As an example of an undesirable effect, consider a capacitor used in an integrating circuit shared by several inputs. After converting one channel, the charge in this capacitor must be depleted prior to converting the next channel. Suppose the normal operating input range for each input is from 0 to +5 volts, and suppose each input is driven by a 0- to 5-volt transmitter powered by +30 volts DC. Under normal conditions, all input signals are 5 volts or less, and the charge in the integrating capacitor is depleted easily between channel conversions. However, if one transmitter fails such that its output is shorted to the supply, 30 volts

will be present at the corresponding channel input. Sufficient time may not exist for the device to deplete the charge associated with a 30-volt input before processing the next channel. This extra charge may cause the next channel to read artificially high.

Other undesirable effects exist, such as induced noise from one channel to another due to improper etch placement. All these undesirable effects can be considered channel-to-channel interference. Testing for this interference consists of assessing the ability of each channel to operate properly regardless of the signal applied to other channels, within reason. In keeping with the above example, Figures 3-6, 3-7, and 3-8 present a test setup, a test procedure, and a data sheet for performing channel-to-channel interference testing.

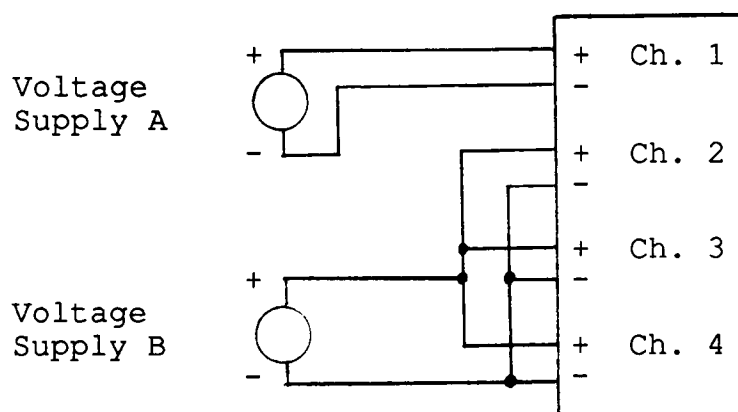


Figure 3-6. Initial Setup for Channel-to-channel Interference Test.

- (1). Obtain the test setup described in Figure 3-6.
- (2). Set supply B to 0.00 volts. This corresponds to a minimum operating voltage.
- (3). Set supply A to 0.00 volts.
- (4). Read and record each channel.
- (5). Change supply A to maximum operating voltage of 5.00 volts.
- (6). Read and record each channel.
- (7). Change supply A to absolute maximum voltage of 30 volts.
- (8). Read and record each channel.
- (9). Change supply B to 5 volts and repeat steps 3 through 8.
- (10). Move supply A to next channel, and supply B to three other channels only.
- (11). Repeat steps 2 through 10 until each channel has been driven by supply A.

Note: Perform at 0, 25, and 50 degrees Celsius

Figure 3-7. Channel-to-channel Interference
Test Procedure.

Channel-to-channel Interference Test Results

Device # _____

Tested By _____

Temp. ____0C ____25C ____50C

Date _____

Supply Settings (volts)			Channel Readings (Integer)		
Supply A	Supply B		Supply A	Supply B	
Ch. ____	Chs. ____		Ch. ____	Ch. ____	Ch. ____
0	0	!	_____	_____	_____
5	0	!	_____	_____	_____
30	0	!	_____	_____	_____
0	5	!	_____	_____	_____
5	5	!	_____	_____	_____
30	5	!	_____	_____	_____

Note: This table must be used four times per device
(once per each channel connected to supply A)

Pass / Fail Criteria: All readings in normal operating range of 0 to 5 volts must meet accuracy specification. All readings for absolute maximum voltage of 30 volts must be error code for over-range.

Figure 3-8. Data Sheet for Channel-to-channel Interference Test.

A device should continue to function correctly whenever the power supplied to the device remains within the specified interval. Whether power is supplied by an external supply, an internal supply (possibly host), or both, tests should be conducted to ensure proper operation under worst case power arrangements. To perform these tests, all device power supplies must be capable of being adjusted to the minimum and maximum specified levels. External supplies generally present little difficulty with regard to adjustment since adjustable supplies are very common. However, internal supplies are usually not easily adjusted. Under these circumstances, the internal supply should be bypassed and replaced with a separate, external, adjustable supply for these tests. This replacement entails breaking or cutting the power lead or etch from the internal supply, connecting the power lead from the replacement supply to the device, and joining the reference voltages (grounds) from the internal and replacement supplies. This arrangement should be used for this test only.

These tests are conducted by applying combinations of worst-case power arrangements and verifying correct device operation. All possible combinations should be tested as indicated in Table 3-3 for a device requiring +5 and +12 volts DC. Supply

Table 3-3. Power Supply Variation Test Points.

Test Point	!	Supply	
		+5v +/- 5%	+12v +/- 5%
1	!	4.75v	11.4v
2	!	5.25v	11.4v
3	!	4.75v	12.6v
4	!	5.25v	12.6v

current should be measured for each supply and test point, and power consumption should be calculated to ensure the device is within acceptable power budget limits. If a voltage ripple requirement is specified, the tests should be repeated while inducing the appropriate AC ripple voltage onto the DC supply lines. These tests should be performed at minimum, midpoint, and maximum operating temperatures for the device.

One very important area of testing from a reliability standpoint deals with product misuse and abuse. A product must function correctly if applied correctly, but should also exhibit robustness when applied incorrectly. Obviously, the product cannot be expected to function correctly if misapplied. However, the product should not be damaged by common misapplications. All potential misapplications cannot

be predicted or designed around. Thus, precautions should be taken to ensure that the product fails in a safe manner if it must fail. Safety is a substantial topic, and a discussion of safety is not the intent of this thesis. Discussion is limited to methods for evaluating the ability of a typical analog input device to survive common misapplications.

Steps can be taken early in the design phase to reduce the chances of user misapplication. For example, all devices in a set of similar devices should follow the same wiring convention. Power connections should be clearly distinguished from signal connections. Connector keying can be used to safeguard against improper connections. Where possible, protection circuitry should be provided to protect signal and power inputs from the highest potential expected in the area. Protection circuitry should be in place to protect inputs in the event of a probe failure which could present high voltages to the inputs. Also, if possible, the design should allow the device to be repeatedly connected and disconnected from all signal and power sources with power applied without experiencing permanent damage or configuration alterations. This should be a design goal, even if the customer is warned to remove power before modifying an installation.

Specifications for allowable levels of abuse may or may not be published externally. In either case, these levels should be internally specified and tested. Testing for effects of miswiring can be accomplished by applying the absolute maximum potential expected in the area to the input under test for several minutes, removing this condition, and verifying proper device operation. Effects of probe failure can be determined by applying the maximum potential expected to the signal input for an extended length of time, removing this potential, and verifying proper operation. This test should be performed concurrently with channel-to-channel interference testing described earlier, if applicable. The two areas of concern are interference on other channels and permanent damage to the channel under stress. Evaluation of connection and disconnection of power and signal sources with power applied can be accomplished by repeatedly making and breaking connections in various sequences, each time verifying proper device operation and configuration retention.

Accuracy and repeatability tests should be performed at minimum, midpoint, and maximum operating temperatures for the device under test. All probe types intended for use with the device should be considered. Accuracy should be evaluated in intervals

no larger than 10% of the full-scale range for each probe type, and repeatability should be measured at least in the lower, middle, and upper portions of the range for each probe type. Certain circumstances might allow the evaluation to be split into two or more segments, such as a hardware examination of the unaltered conversion data bits followed by a software analysis of linearization tables and interpolation routines. However, caution should be exercised when examining accuracy in multiple segments since the final verification should utilize the device in the same manner to be used by the customer. Due to the level of detail required to discuss accuracy and repeatability, Chapter 4 has been devoted entirely to this subject.

CHAPTER 4

ACCURACY AND REPEATABILITY

Generally, specifications receiving the most attention for analog input devices are those dealing with accuracy and repeatability. This chapter is devoted entirely to accuracy and repeatability. A specification method is defined, customer perception is discussed, and an automated test method for performance evaluation is presented.

Many methods of describing the accuracy and repeatability of an analog input device are used in industry today. Care must be taken when selecting an analog input instrument to be sure the accuracy and repeatability specifications are acceptable for the intended application. Different manufacturers specifying the same numbers might mean different things. Thus, the procurer must clearly understand how the manufacturers arrived at their specifications.

For the purpose of discussing design verification testing, a specification method based on statistical properties is presented. Noise effects which occur in the analog input circuitry, signal, and signal wiring tend to result in a variety of readings for a fixed signal input. This variation or fluctuation in

readings is a characteristic of all analog input instruments. By far, for a fixed input, most analog input devices produce discrete readings which approximate a normal (Gaussian) probability distribution. The normal distribution is a continuous probability distribution, and the approximation improves as the number of samples increases.

Consider the histogram shown in Figure 4-1. Note

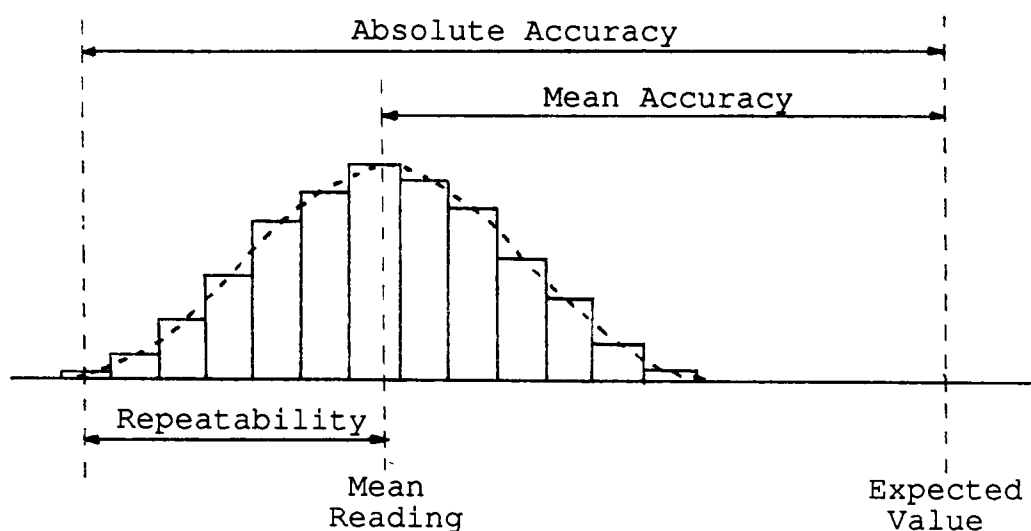


Figure 4-1. Sample Histogram with Specification Definitions.

the Gaussian shape of the dashed line which connects the discrete distribution points. The expected value corresponds to the ideal reading and can be calculated by applying the conversion equations to the present analog input signal. The mean reading is an average of

all the readings taken. In an ideal device, the mean would equal the expected value. The difference between the mean and the expected value is defined to be the mean accuracy.

Using statistical properties of the normal distribution, a definition for repeatability can be obtained. Repeatability, simply stated, is a measure of the variability of readings about the mean. The variance associated with a distribution is computed by taking the second moment about the mean. Sigma, the positive square root of the variance, is known as the standard deviation. The probability that a measurement will lie between two points is computed by determining the area under the distribution function between these two points. Table 4-1 lists three intervals for a normal distribution and the probability that a reading lies within the corresponding interval. Table 4-1 indicates that 99.7 % of the readings for a normal

Table 4-1. Probability a Reading Lies within an Interval for Normal Distribution.

Interval Endpoints	!	Probability Reading Lies between Endpoints
mean +/- sigma	!	0.683
mean +/- 2 sigma	!	0.954
mean +/- 3 sigma	!	0.997

distribution lie within three standard deviations of the mean. Extending these concepts to discrete terminology, 997 of 1000 readings would be expected to lie within a fixed distance of the mean. Three sigma provides a good cut-off point by providing a high percentage of readings within some specified distance of the mean while leaving some room for a few readings further from the mean. Thus, repeatability, or three-sigma repeatability, is defined as the distance from the mean within which 99.7 % of the readings lie.

Absolute accuracy is the sum of the mean accuracy and the repeatability. Given any two, the third specification can be determined. These specifications are usually presented as a percentage of some full-scale input parameter. A further discussion of the concepts used to define these terms can be found in an engineering probability and statistics book. (3)

Customer confusion sometimes arises regarding resolution. Resolution is the smallest change that can be reported, and is usually expressed as a number of bits. A device might exhibit 12 bits of resolution yet only 10 bits of accuracy. Unlike a digital-to-analog conversion device, an analog-to-digital instrument cannot have accuracy better than its resolution. Thus, the resolution sets an upper bound on the accuracy. However, nothing can be said about the lower bound on

accuracy based on the resolution. Consider two analog input systems, each offering 12 bits of resolution. One system might exhibit 10 bits of accuracy while the other exhibits only 6 bits of accuracy. When procuring an analog input device, the misconception that high degrees of resolution imply high degrees of accuracy should be avoided.

To gain a true characterization of accuracy and repeatability performance, many readings must be taken. Automated testing can save valuable time. Figure 4-2 shows a block diagram for fully automated testing. A programmable, precision source, at least an

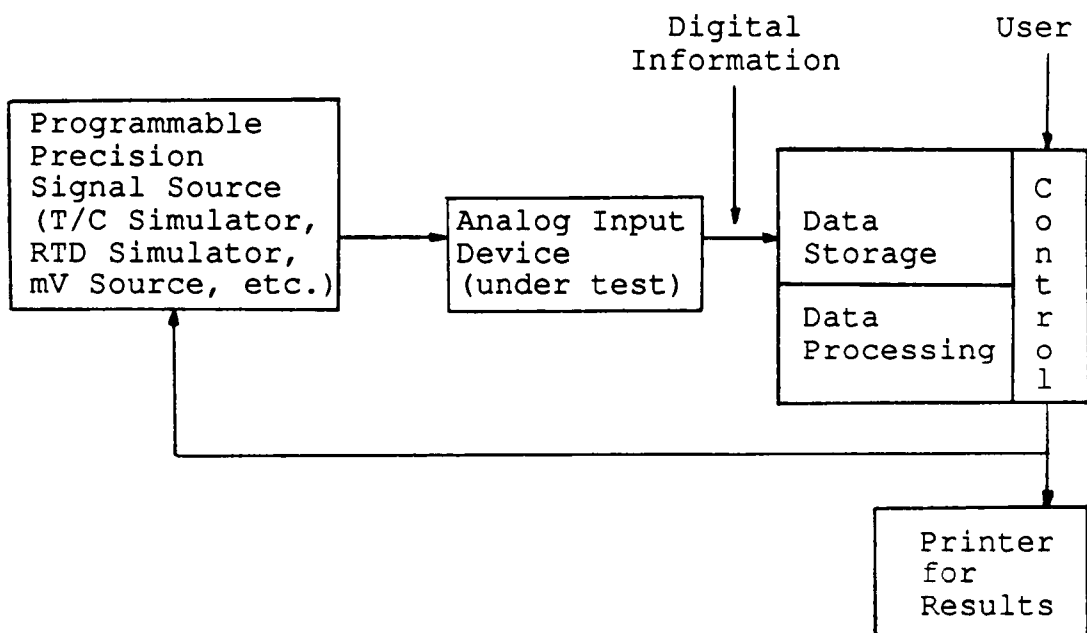


Figure 4-2. Fully Automated Accuracy and Repeatability Testing.

order of magnitude more accurate than the device under test, must be used to drive the analog input device. Very short lengths of shielded signal wire is desirable to minimize the effects of external noise. The digital output of the device under test is supplied to a data-storage / data-processing unit. A control section interfaces with the test operator, synchronizes the programmable source, supervises data retrieval and data processing, and directs output to the printer. The time between samples must be greater than or equal the update time of the device under test to avoid multiple readings of the same information. A sample flowchart for an automated test cycle is given in Figure 4-3.

Valuable time can also be saved using a semi-automated setup. For example, if the precision source is not programmable, the data points can be set manually while still allowing the remainder of the system to function as described above. Similarly, a programmable source might be available, but more effort might be required to interface the source to the control section than to simply adjust the source manually for each new point.

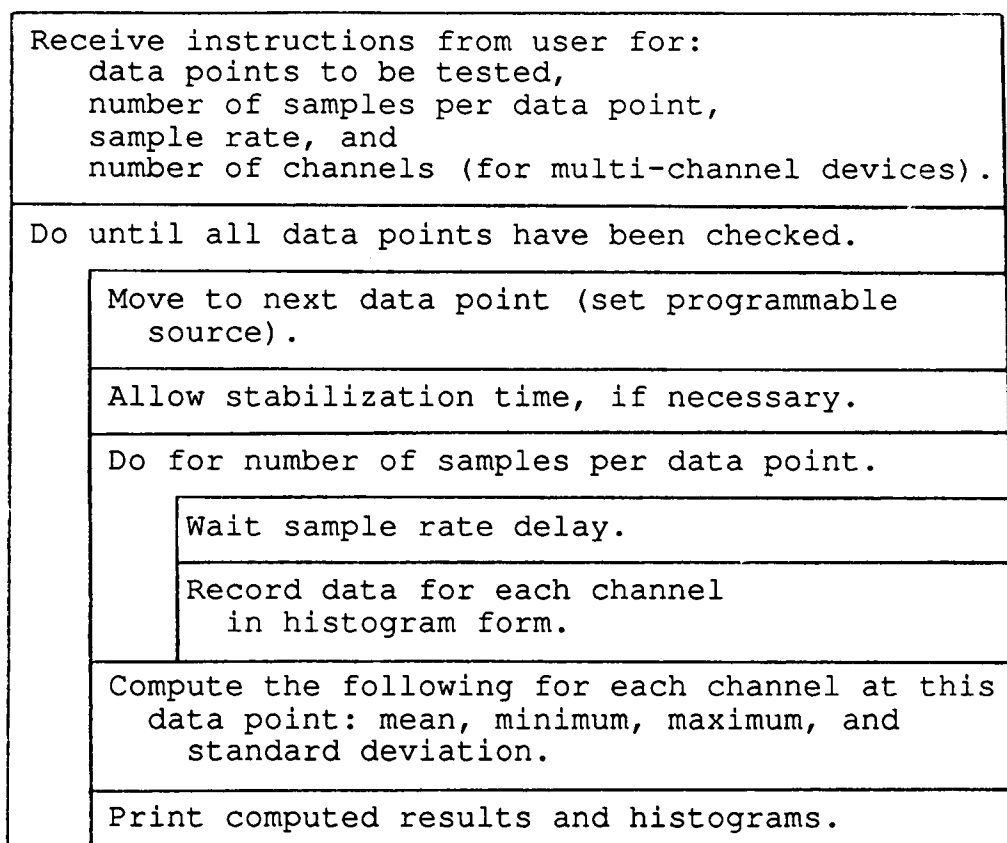


Figure 4-3. Structured Flowchart Describing a Fully Automated Accuracy and Repeatability Test.

Appendix A contains a ladder logic program used in a Texas Instruments Model 530 programmable controller to test 500-series analog input modules. Instructions for use and a sample output are included. Although this is not fully automated in the sense that no control is provided to adjust the signal source, an advantage is gained due to ease of data retrieval since the controller and modules are designed to work together. (4)

CHAPTER 5

ENVIRONMENTAL AND ELECTRICAL NOISE VERIFICATION

A device capable of proper operation only in a very limited range of environmental conditions is of no use in an application where the environment cannot be precisely controlled or predicted. The goal of most manufacturers is to provide products that will reliably satisfy customer needs throughout an extended environmental range. Environmental specifications are often used by industry as a measure of robustness. Much engineering effort has been expended to define and ensure acceptable levels of environmental robustness. As a result, many military and industry standards have been developed for performing environmental and electrical noise testing. Since general environmental and noise test procedures are well defined, this chapter focuses on the application of these tests to analog input devices. Non-operating tests, such as shipping and storage, are considered first followed by operating tests, such as temperature cycling and humidity. Electrical noise testing is discussed last. (5), (6), (7), (8)

The first environment which must be survived by a product is the trip from the manufacturer to the

customer. This trip typically involves package handling, one or more shipping methods, and storage arrangements. Furthermore, customers may elect to store the product before or between use. Generally, no special precautions are taken to control temperature and humidity for electronic products during shipment and storage. Handling and storage tests have been developed to assess the ability of a product to withstand the shipping and storage environment.

Handling tests, such as drop and non-operating vibration, are generally not dependent on product type. Thus, no special arrangements apply when testing analog input devices. The procedure for performing handling tests for all product types is to verify proper product operation, package the product in the appropriate pack material, subject the product to the desired conditions, unpack the product, check for cosmetic damage, and verify proper operation. An internal inspection should also be performed to check for internal damage not obvious through functional testing, such as loose components, loose screws, printed circuit board misalignment, or a loose chassis ground wire. A check should always be made to verify chassis ground continues to provide a good connection to all exposed metal. Table 5-1 shows a sample of drop heights and drop positions which might be used by a

Table 5-1. Drop Test Requirements for
Packaged Products.

Weight of Packaged Product (pounds)	Drop Height (inches)	Number of Drops / Drop Positions
< 10	48	10 / 6 sides, 3 contiguous edges, corresponding corner
10 to 50	36	10 / 6 sides, 3 contiguous edges, corresponding corner
> 50	12	1 / bottom (assumes pallet and forklift handling)

company to verify adequate product protection. This chart is based solely on the weight of the packaged product. Other charts might rely on package size as well as weight. Failures occurring during packaged drop testing are usually attributed to insufficient pack material. Consequently, the pack material, not the product, is normally redesigned in the event of a failure. Drop testing on unpackaged products is often performed on devices which are considered portable or require hand-held operation, such as calculators and telephones. However, these unpackaged tests are usually not applicable for analog input devices which are not handled during normal operation and are seldom moved after initial installation.

Non-operating vibration is intended to simulate shipping conditions when performed on packaged products. Testing methods range from strapping the package to a vibration platter and applying a certain acceleration for a certain time to placing the package unconfined on a cyclic bounce tray and adjusting the tray to cause the package to rise above the tray a certain height each cycle. Test methods are performed similar to drop testing, and failures are similarly attributed to insufficient pack material. Table 5-2 gives an example of packaged vibration test parameters.

Table 5-2. Packaged Vibration Test Parameters
(Non-operating).

Type Test	!	Parameters	!	Duration
Confined (strapped to platter)	!	.01 g ² /Hz random vibration, 200 to 600 Hz	!	10 minutes per axis, 3 axes
Unconfined (bounce tray)	!	2 Hz cycle time, must leave tray .125 inch each cycle	!	15 minutes per axis, 3 axes

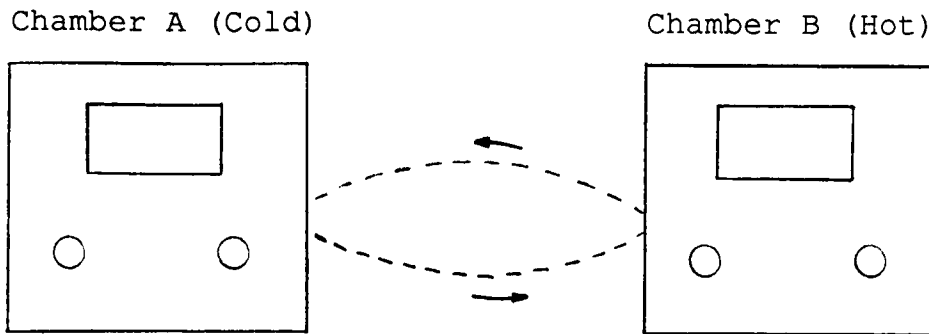
Storage tests are designed to reflect warehouse conditions. Temperature extremes, thermal shock, and moisture tests all fall into the storage category.

Again, analog input devices are not treated differently from other product types during these non-operating tests, since most other electronic products are shipped and stored by similar methods. The test procedures consist of verifying proper product operation, applying the adverse conditions, again verifying proper product operation, and performing a visual inspection for internal and cosmetic damage. Products may be stored with or without pack material, so tests should be conducted both ways. If the same pack material was previously proven acceptable on a similar product, the tests may be performed on the unpackaged product only.

Temperature storage tests are typically performed by subjecting the device under test to the minimum specified storage temperature for one to four days followed by the same length of time at the maximum specified storage temperature. Device operation can be checked between the cold and hot storage tests or after both tests have been completed. In either case, the product must be allowed to stabilize until the operating temperature has been reached. Some manufacturers specify a maximum rate of temperature change for operation of analog input devices, so this should be appropriately factored into the stabilization time.

If temperature storage tests are successfully passed, thermal shock tests can be conducted. Thermal shock generally consists of cycling the product several times between the minimum and maximum storage temperatures. The purpose of this test is to uncover problems caused by different materials expanding or contracting at different rates. The device under test is typically held at one extreme until stable. Stabilization is largely a function of materials comprising the product and the mass of the product. After stabilization has been reached at one extreme, the product should be removed and placed into a separate chamber which is already adjusted to the other temperature extreme. Some procedures allow the product to reside near 25 degrees Celsius for three or five minutes between chamber transfers while others require immediate transfer. Unlike temperature storage tests discussed earlier, shock testing requires two separate environmental chambers. A typical thermal shock test setup is shown in Figure 5-1.

Following a successful thermal shock test, the product should be subjected to a moisture test. Typical moisture tests involve condensing moisture for six to ten days and temperature cycling above and below the freezing point of water. A one day drying period is usually allowed before verifying proper



NOTES:

- (1) Perform 10 complete cycles (cycle indicated by dashed line)
- (2) Allow a 3 minute dwell time between chambers
- (3) Allow a 3 hour stabilization time in each chamber

Figure 5-1. Thermal Shock Test Setup.

operation. Hairline cracks may be induced in components during thermal shock, but the product may continue to function correctly until the moisture test is performed. Moisture can condense in these hairline cracks, and freezing could cause further cracking and permanent component failure. Test sequence is important since the increased cracking condition will not occur if thermal shock is performed after moisture.

Operating tests are those which reflect environmental conditions expected for an installed, functioning product. Temperature, humidity, and vibration are the most common operating tests. Operating tests generally require more ingenuity than

non-operating tests since the product hardware must be fully exercised and monitored during the test. Operating tests may last as long as seven days or more, and some method must exist to monitor product status throughout the test. Ideally, the monitor method is automated, thoroughly evaluates the hardware through a sequence of diagnostics, continuously repeats the diagnostic sequence, reports number of failures and passes, reports failure codes upon failure, and retains data through a power cycle. Although the monitoring method must exercise and diagnose the hardware, no effort should be applied to exercise functions solely dependent upon software since software errors exist regardless of the environment.

One method of exercising an analog input device is to use a complimentary analog output device driven by a common host as illustrated in Figure 5-2. In this arrangement, automated testing can be achieved by writing a known digital word to the analog output device and then comparing the resulting digital word produced by the analog input device with the expected value. Several values throughout the valid range can be tested before repeating the sequence. This concept is further illustrated by the structured flowchart of Figure 5-3.

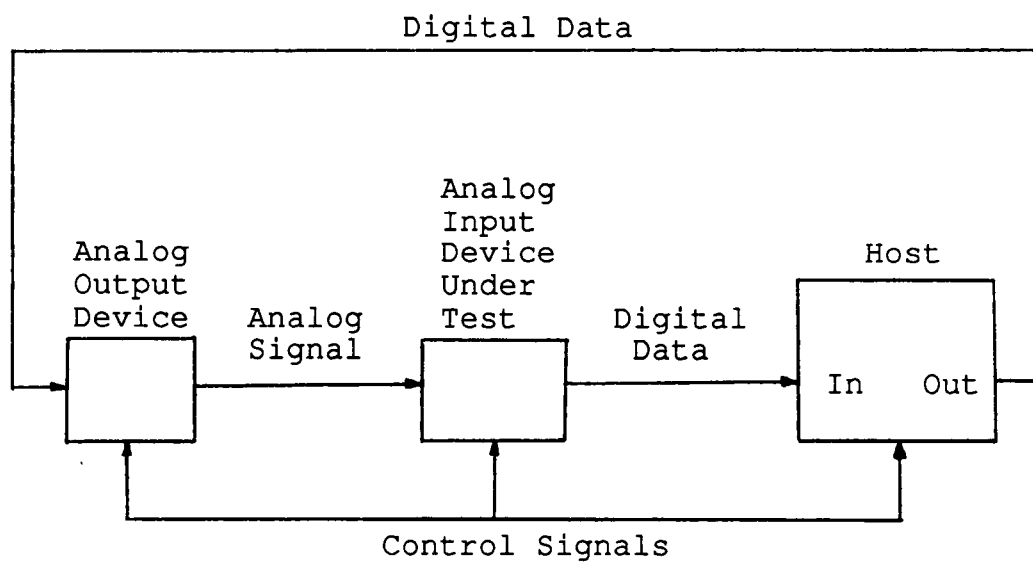


Figure 5-2. Setup for Monitoring Analog Input Device.

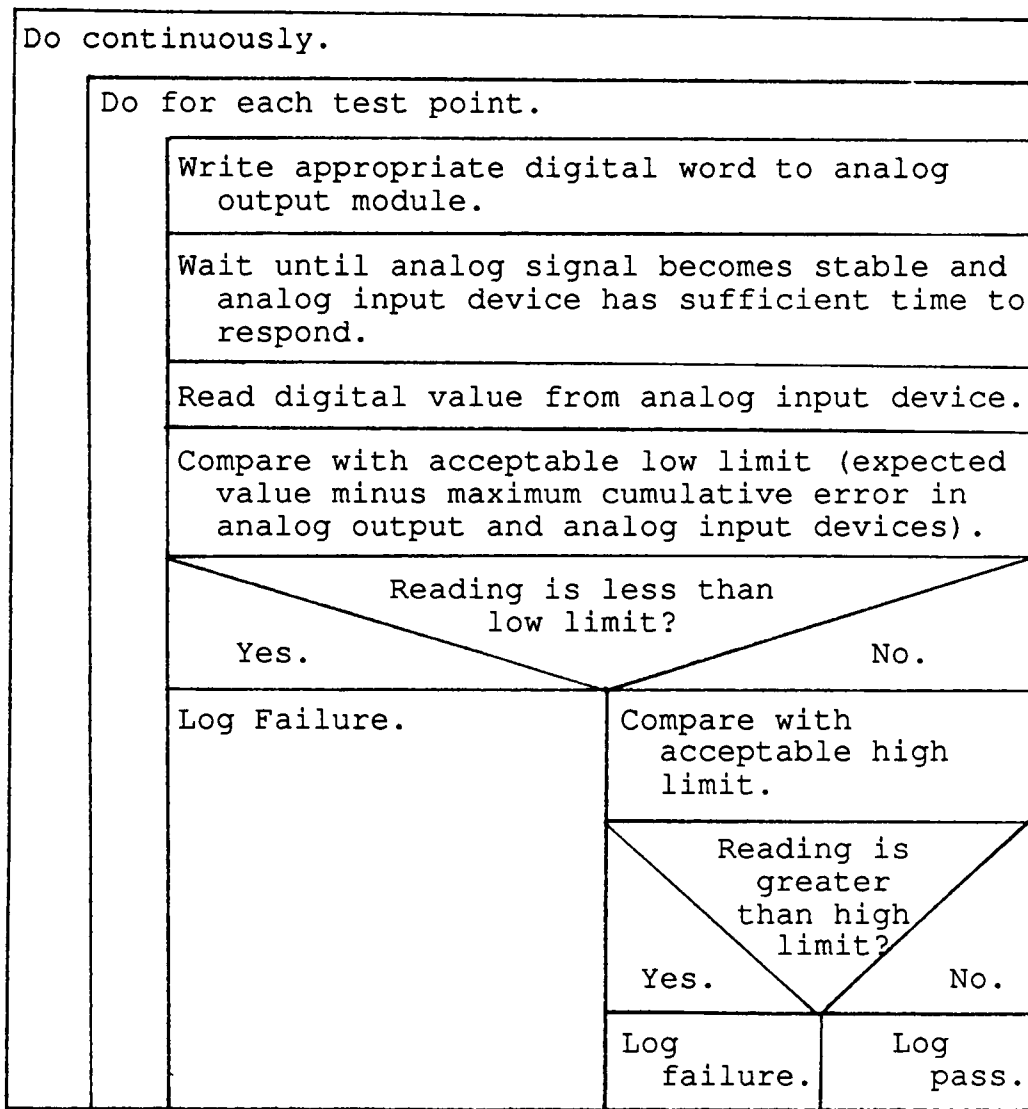


Figure 5-3. Structured Flowchart for Automated Monitoring of an Analog Input Device.

A complimentary analog output device may not always be available. In such cases, the test can be conducted by supplying a single fixed analog signal to the analog input device under test and comparing the resulting digital word with appropriate upper and lower limits. An example of this monitoring technique is given in Figure 5-4 for an RTD input device. This

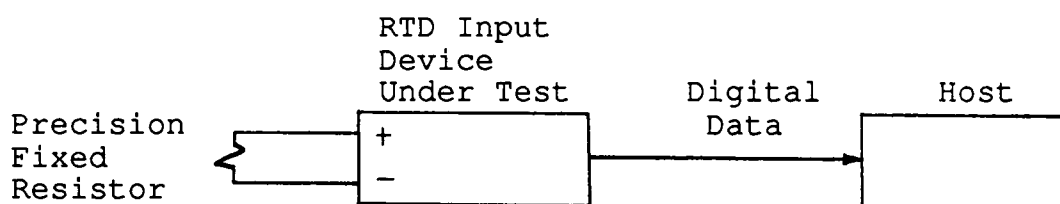


Figure 5-4. Monitoring Technique using a Precision, Fixed Resistor.

configuration is not as thorough as that of Figure 5-2, but meaningful results can still be obtained.

Operating temperature testing can be performed by subjecting the device to the minimum required operating temperature followed by a controlled ramp, if specified, to the maximum operating temperature. If an automated chamber capable of performing a smooth temperature ramp is unavailable, an approximation can usually be made by changing the oven setting a few degrees and waiting the corresponding amount of time

before proceeding. Thus, the maximum temperature will be reached through a series of discrete settings rather than a linear ramp. A temperature stress test should be performed by subjecting the device to temperatures slightly above and below the operating temperature range. The purpose of this stress test is to determine the amount of margin associated with the specification for operating temperature range. For analog input devices, the operating temperature cycle should be repeated several times to verify calibration retention. The device should also be power cycled at each temperature extreme.

Humidity testing can be performed by exposing the device to the maximum specified relative humidity at the maximum allowable wet-bulb temperature. Generally, for analog input devices, the relative humidity is specified in percent and the maximum wet-bulb temperature is not specified. In this case, the environmental chamber should be set to a dry-bulb temperature equal to the maximum specified operating temperature. Relative humidity tests are normally steady state, last for several days, and may include occasional power cycling.

Operating vibration is intended to simulate the movement to be encountered in the intended environment. This test is generally performed using a

vibration table as described previously for non-operating vibration.

Two types of electrical noise testing exist. One type involves the quantification of electrical noise generated by the device which is expelled into the surroundings. For example, Federal Communications Commission (FCC) testing involves determining the amount of noise radiated from the product under test. This radiated noise level must remain below certain defined levels to ensure this product will not interfere with other nearby electronic products. Tests for this type noise may be required by law, and often must be performed under the supervision of a regulatory agency.

The second type of electrical noise testing deals with immunity, or the ability of the device under test to function correctly while under the influence of externally produced noise. The external noise can be conducted through power or signal lines, radiated into the device, or produced through electrostatic discharge. Conducted noise tests are usually performed by inducing spikes of various amplitude and pulse-width onto the signal and power lines. Radiated noise tests are performed using an antenna which produces an electric field, and may require a shielded screen room to protect personnel and nearby electronic equipment.

ESD tests are intended to simulate transfer of charge between the product and a finger or tool, and are typically performed using an ESD test gun calibrated in terms of energy level and output capacitance and resistance.

In general, analog input devices should be noise tested using the monitored setup described earlier. However, an analog input device is designed to respond to the signal present at its input terminals. If noise is radiated onto the signal lines, the device will process this noise along with the true signal and produce a corresponding noisy digital output. Thus, the product cannot be expected to remain accurate with respect to true signal under these circumstances. Consequently, tests should be conducted using the recommended signal wire, and then repeated using the shortest signal wire possible. For example, a voltage-input device should be tested while connected through the maximum amount of recommended cable to a voltage-output device, and then retested with the inputs shorted. The results should be compared to determine the effect due to the signal wires versus the product itself. ESD testing should be performed by producing an electric arc to all parts accessible to the user. Sufficient time should be allowed between arcs to allow the charge to dissipate. Again, arcs to

the signal wires should be expected to produce momentary fluctuations in readings. If performed correctly, and with the intended environment in mind, environmental and electrical noise tests can be used to predict product performance in the field.

CHAPTER 6

CONCLUSION

This thesis presents test methods for performing efficient, thorough design-assurance testing of analog input devices. Many of the topics discussed apply to other types of products as well. If these methods are performed correctly and completely, most reliability risks can be identified and minimized before the product is released for production. However, the design-assurance effort continues long after product release. Field returns and customer feedback should be monitored continuously for signs of reliability and quality problems. Changes to the product for producibility improvements, cost reductions, or other reasons must be monitored and documented carefully. Occasionally, a mini design-assurance test cycle might be required to ensure a change does not adversely affect product performance. Adequate coverage of all aspects of design assurance will lead to safe, reliable products which satisfy customer requirements.

LIST OF REFERENCES

LIST OF REFERENCES

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- (5) MIL-STD-810C, Environmental Test Methods, 1981
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APPENDIX

HISTOGRAM PROGRAM EXPLANATION

Program Description

1. Purpose - This program provides a frequency distribution of the number of samples of a given analog input voltage which occur within +/- 7 counts of an expected decimal value.
2. Number of Samples - The number of samples taken by the program is set to 100 by counter 1 but can be modified by the user.
3. Sampling Frequency - The sampling frequency is set to 250 ms by timer 2.
4. Program Execution - The 530 sequencer must be in the RUN mode to execute this program. The program is started by forcing X1 off and back on. When all the samples are taken, program execution halts. The expected values for the samples must be entered before the program is executed. The program tests eight channels of a voltage input module logged into the second slot of the 530 system.

Memory Allocation: Minimum, Maximum, Expected Values

Channel	Location	Minimum Value Seen	Maximum Value Seen	Expected Value
1	WX09	V1	V9	V17
2	WX10	V2	V10	V18
3	WX11	V3	V11	V19
4	WX12	V4	V12	V20
5	WX13	V5	V13	V21
6	WX14	V6	V14	V22
7	WX15	V7	V15	V23
8	WX16	V8	V16	V24

Note: The expected value (locations V17 through V24) must be placed into V memory using the AUX25 function of the VPU.

Memory Allocation: Histogram Results

Histogram Distribution of Samples	Ch 1 (WX09)	Ch 2 (WX10)	Ch 3 (WX11)	Ch 4 (WX12)
-7	V100	V200	V300	V400
-6	V101	V201	V301	V401
-5	V102	V202	V302	V402
-4	V103	V203	V303	V403
-3	V104	V204	V304	V404
-2	V105	V205	V305	V405
-1	V106	V206	V306	V406
EXPECTED	V107	V207	V307	V407
+1	V108	V208	V308	V408
+2	V109	V209	V309	V409
+3	V110	V210	V310	V410
+4	V111	V211	V311	V411
+5	V112	V212	V312	V412
+6	V113	V213	V313	V413
+7	V114	V214	V314	V414

Histogram Distribution of Samples	Ch 5 (WX13)	Ch 6 (WX14)	Ch 7 (WX15)	Ch 8 (WX16)
-7	V500	V600	V700	V800
-6	V501	V601	V701	V801
-5	V502	V602	V702	V802
-4	V503	V603	V703	V803
-3	V504	V604	V704	V804
-2	V505	V605	V705	V805
-1	V506	V606	V706	V806
EXPECTED	V507	V607	V707	V807
+1	V508	V608	V708	V808
+2	V509	V609	V709	V809
+3	V510	V610	V710	V810
+4	V511	V611	V711	V811
+5	V512	V612	V712	V812
+6	V513	V613	V713	V813
+7	V514	V614	V714	V814

VPU Status Chart Configuration

STATUS CHART

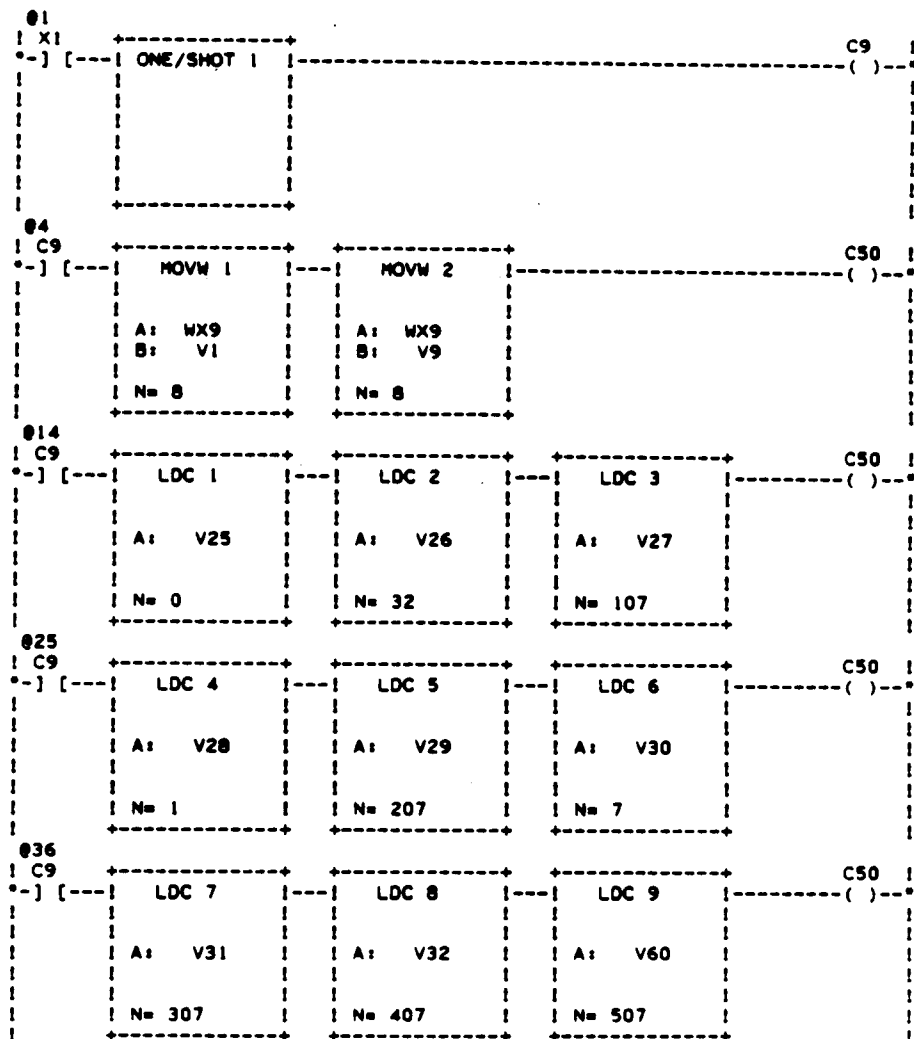
V105 = SIGNED	V405 = SIGNED	V705 = SIGNED
V106 = SIGNED	V406 = SIGNED	V706 = SIGNED
V107 = SIGNED	V407 = SIGNED	V707 = SIGNED
V108 = SIGNED	V408 = SIGNED	V708 = SIGNED
V109 = SIGNED	V409 = SIGNED	V709 = SIGNED
V205 = SIGNED	V505 = SIGNED	V805 = SIGNED
V206 = SIGNED	V506 = SIGNED	V806 = SIGNED
V207 = SIGNED	V507 = SIGNED	V807 = SIGNED
V208 = SIGNED	V508 = SIGNED	V808 = SIGNED
V209 = SIGNED	V509 = SIGNED	V809 = SIGNED
V305 = SIGNED	V605 = SIGNED	WX09 = SIGNED
V306 = SIGNED	V606 = SIGNED	WX10 = SIGNED
V307 = SIGNED	V607 = SIGNED	WX11 = SIGNED
V308 = SIGNED	V608 = SIGNED	WX12 = SIGNED
V309 = SIGNED	V609 = SIGNED	WX13 = SIGNED
		WX14 = SIGNED
		WX15 = SIGNED
		WX16 = SIGNED
TCC1 = TMR/CTR		

Note: This status chart only includes expected value +/- 2 (example: V105, V106, V107, V108, and V109) for each channel. The VPU screen is too small to display all locations.

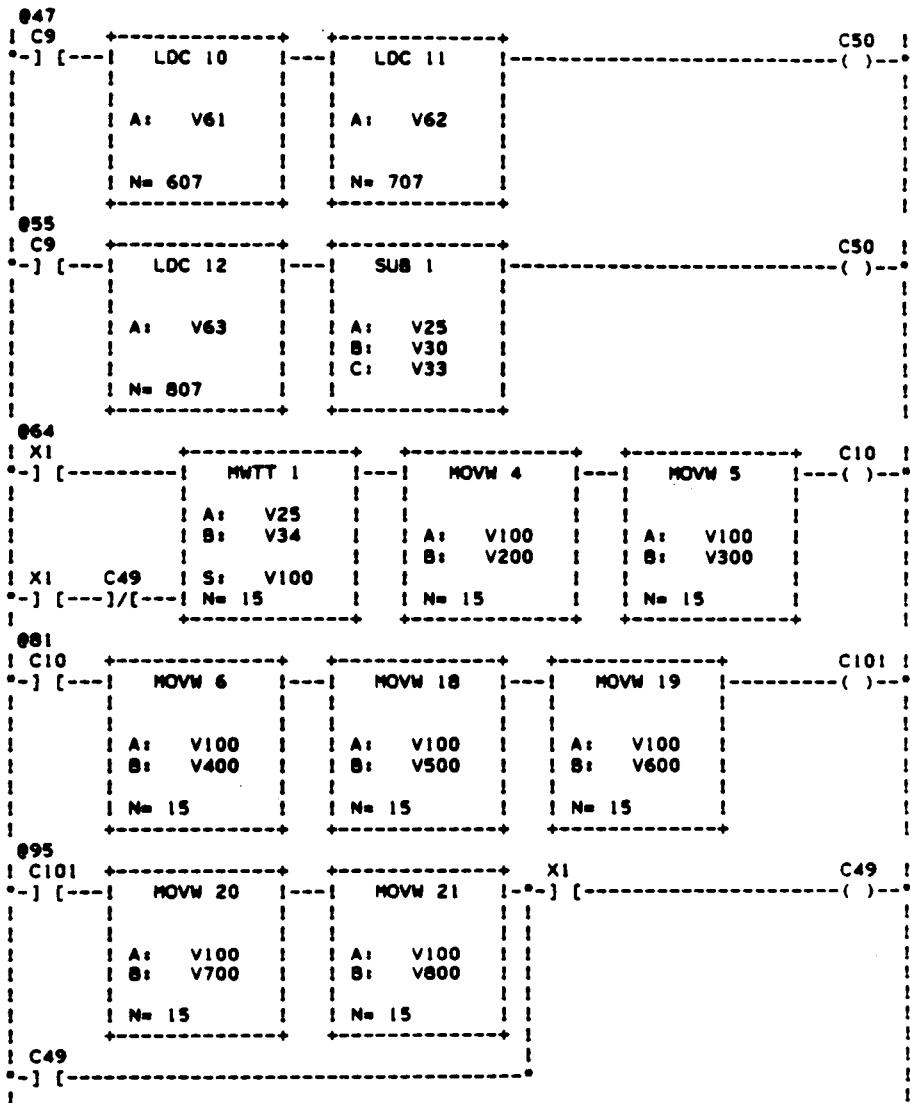
Program Listing

The next twenty pages contain a ladder logic listing of the Histogram Program.

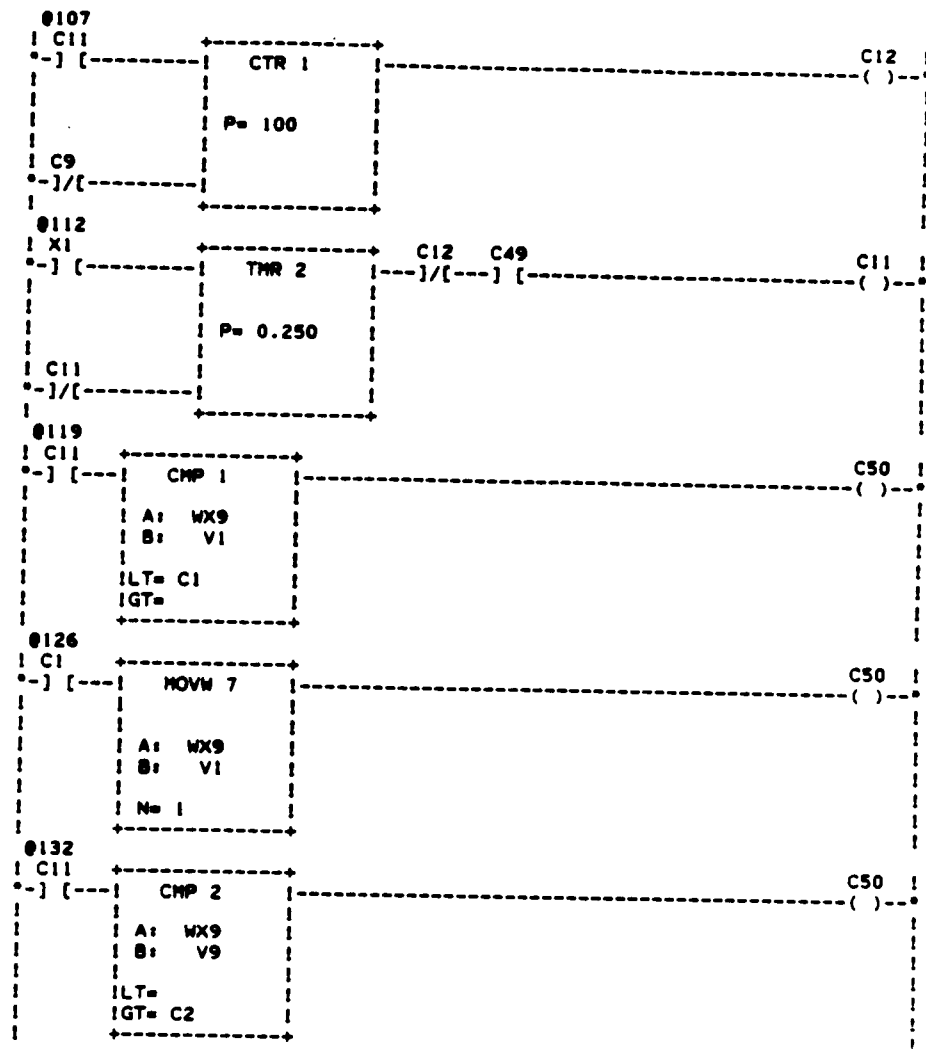
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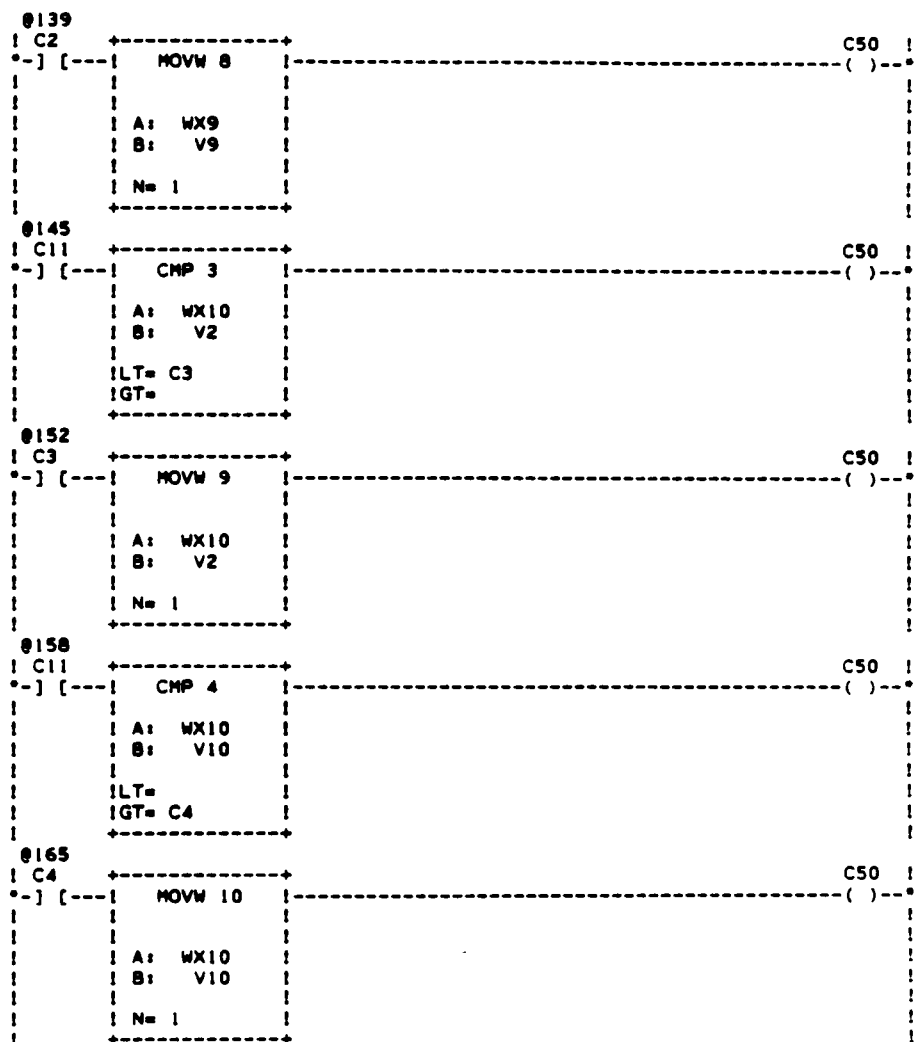
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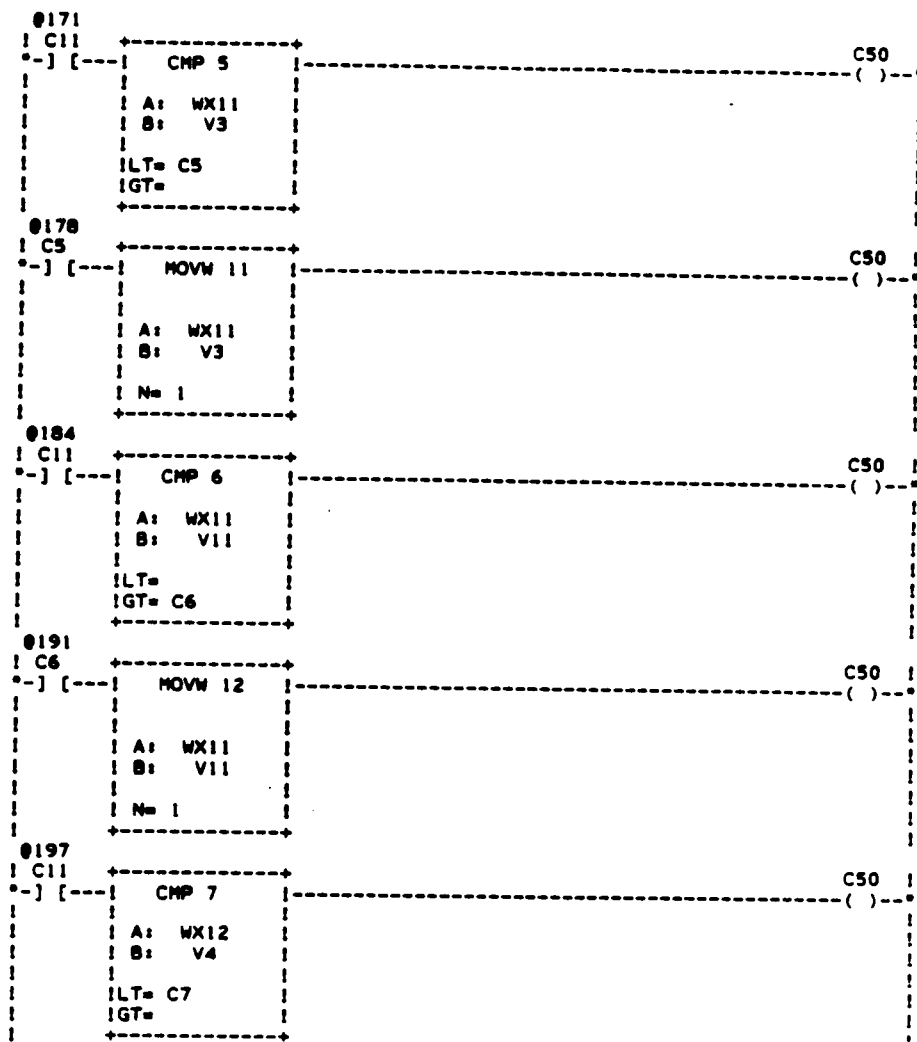
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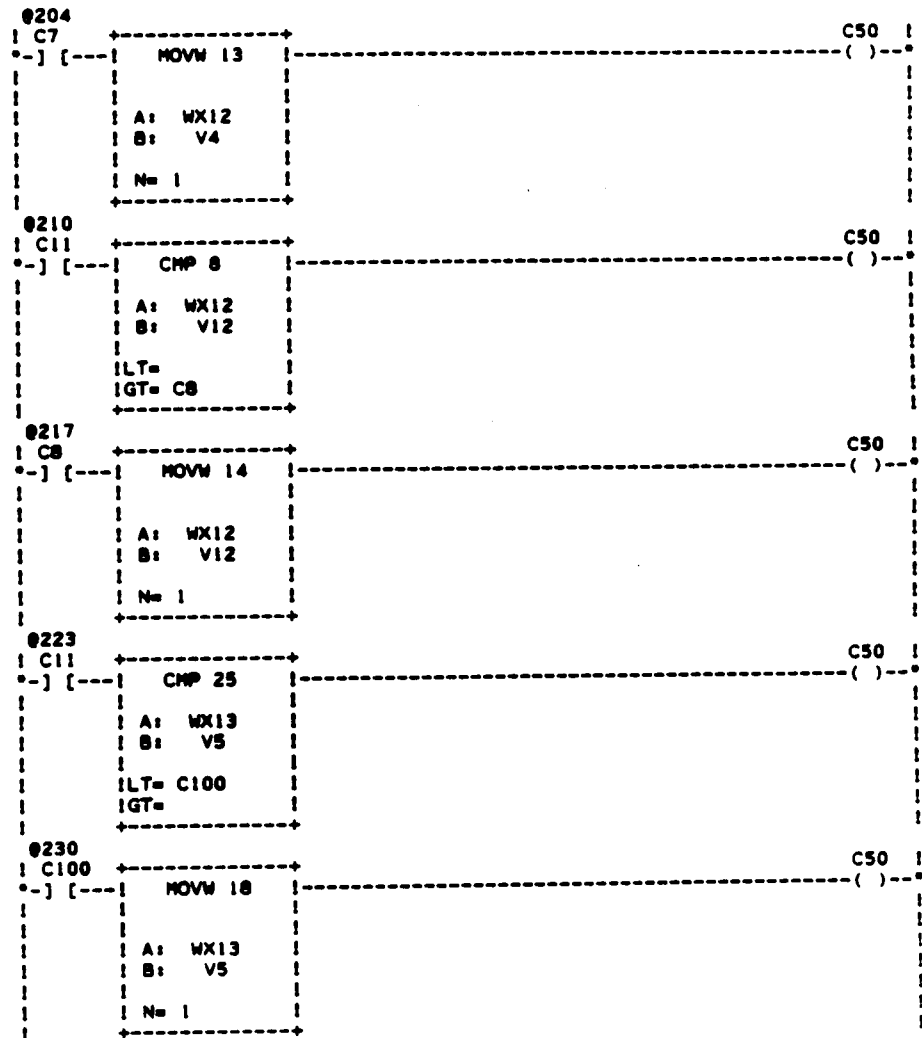
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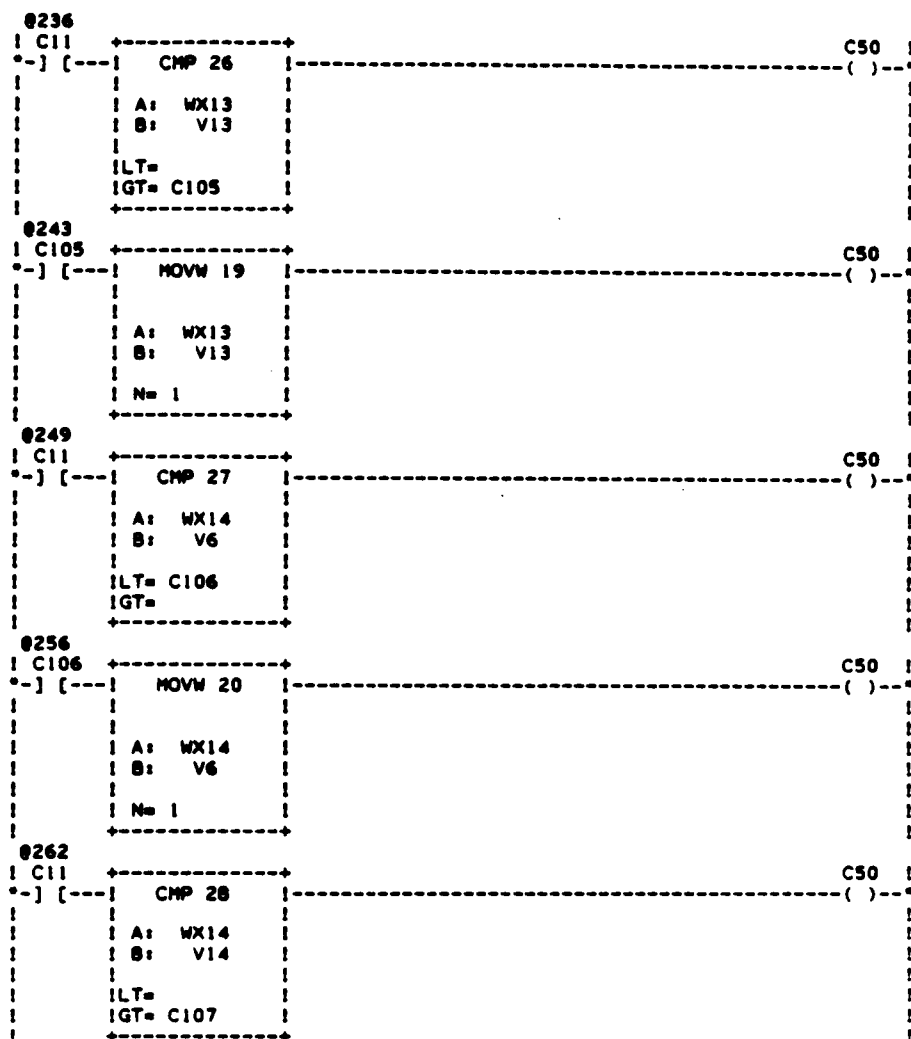


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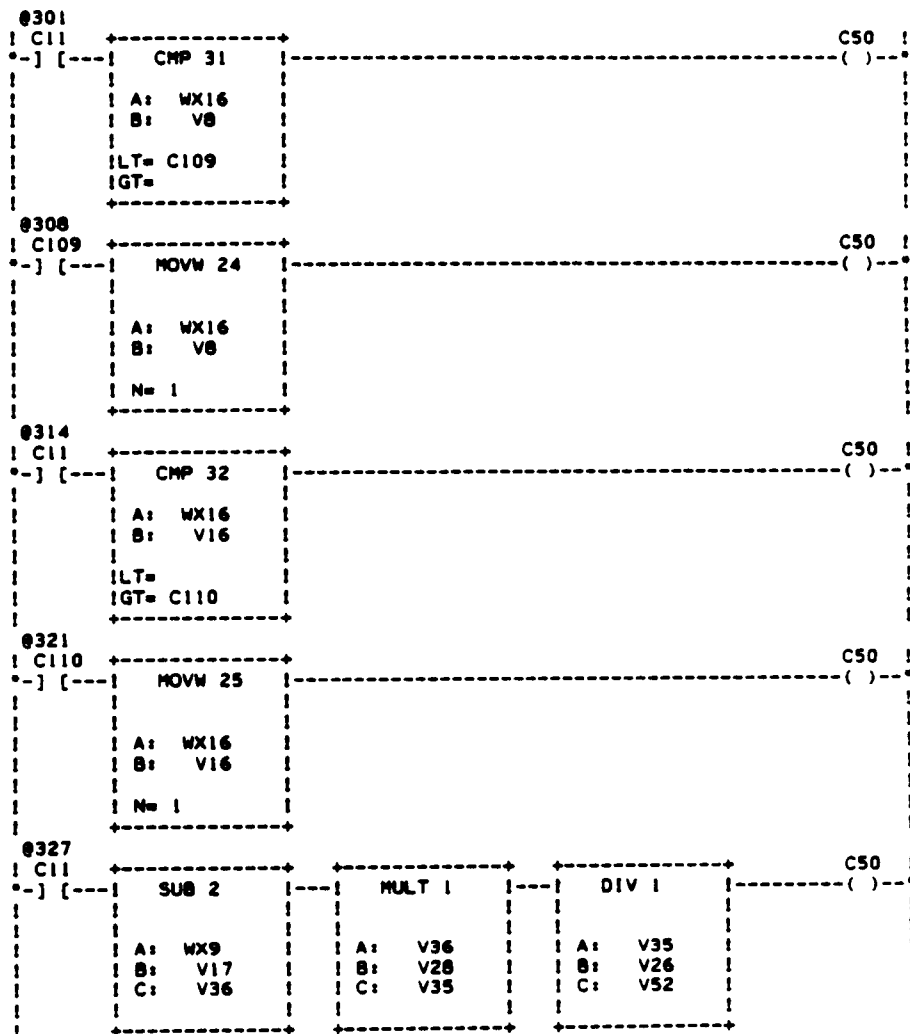
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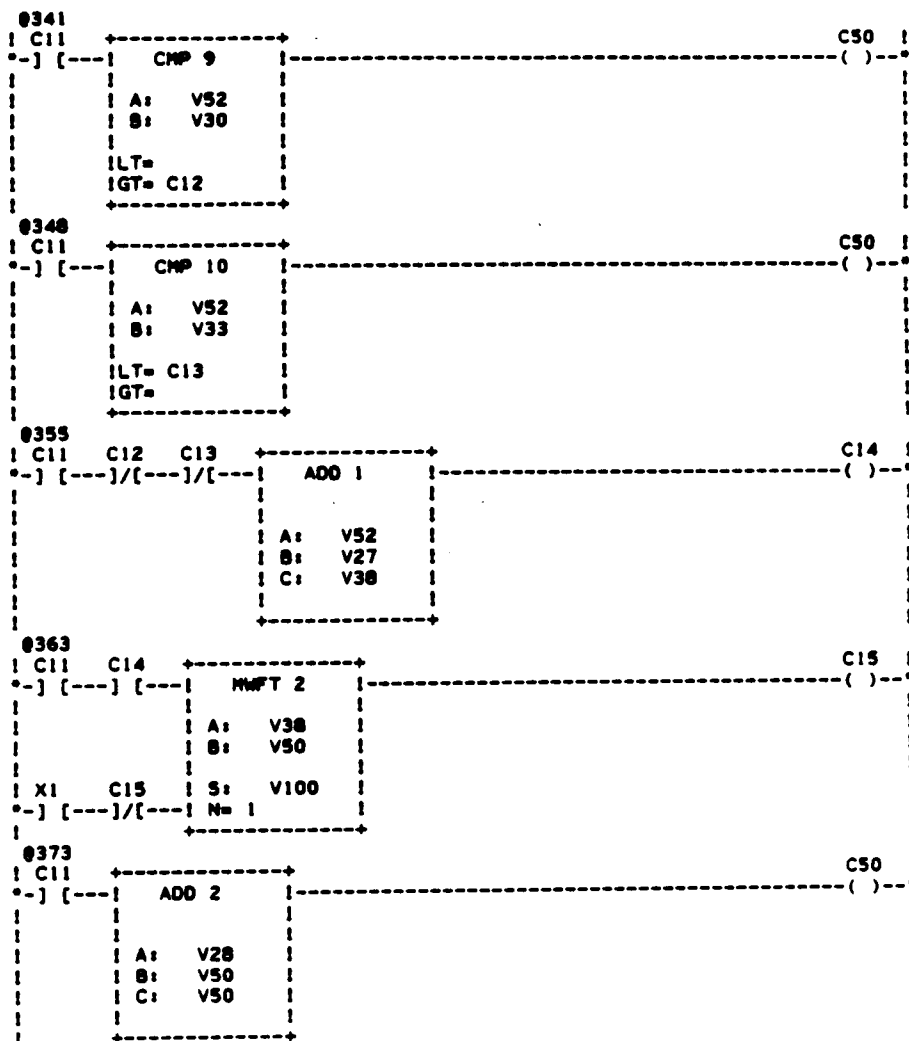
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0269
| C107 |-----| C50 | |
| -] [---| MOVW 21 |-----| ( ) |
|      |         |
|      | A: WX14  |
|      | B: V14   |
|      | N= 1     |
|-----|
0275
| C11  |-----| C50 | |
| -] [---| CMP 29  |-----| ( ) |
|      |         |
|      | A: WX15  |
|      | B: V7    |
|      | LT= C108 |
|      | GT=      |
|-----|
0282
| C108 |-----| C50 | |
| -] [---| MOVW 22 |-----| ( ) |
|      |         |
|      | A: WX15  |
|      | B: V7    |
|      | N= 1     |
|-----|
0288
| C11  |-----| C50 | |
| -] [---| CMP 30  |-----| ( ) |
|      |         |
|      | A: WX15  |
|      | B: V15   |
|      | LT=      |
|      | GT= C109 |
|-----|
0295
| C109 |-----| C50 | |
| -] [---| MOVW 23 |-----| ( ) |
|      |         |
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|      | B: V15   |
|      | N= 1     |
|-----|
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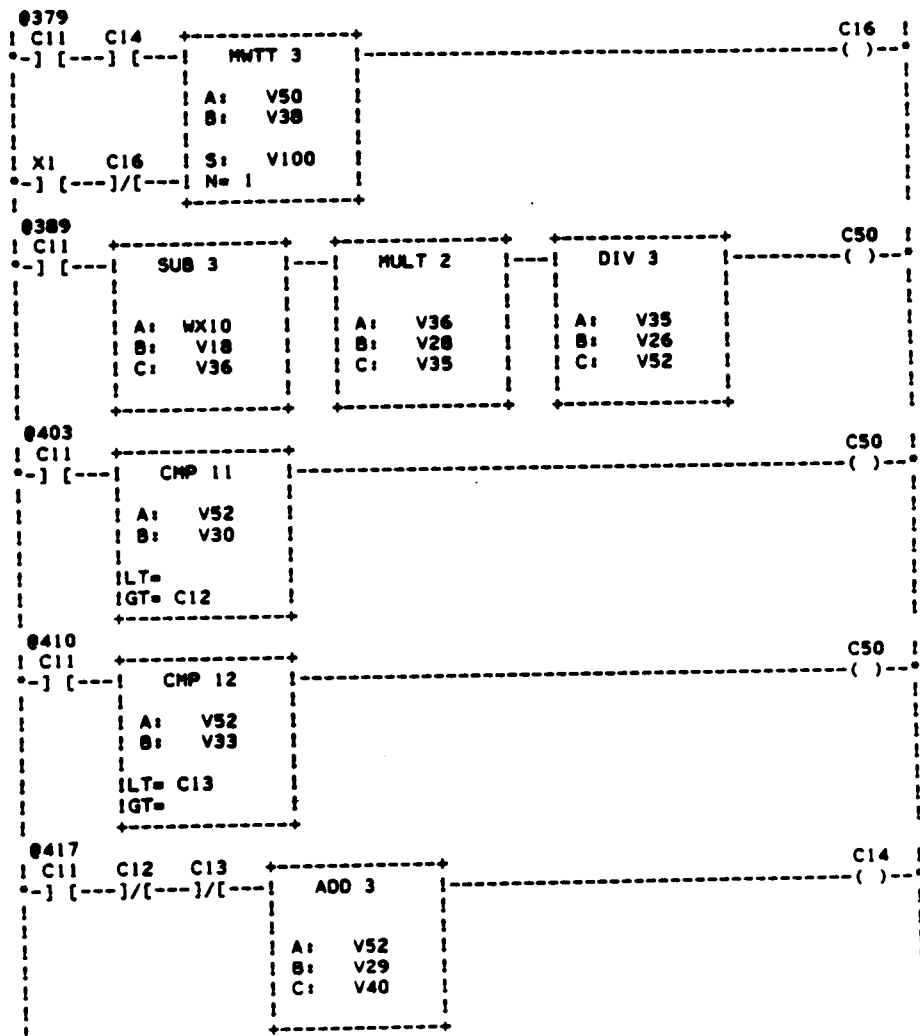
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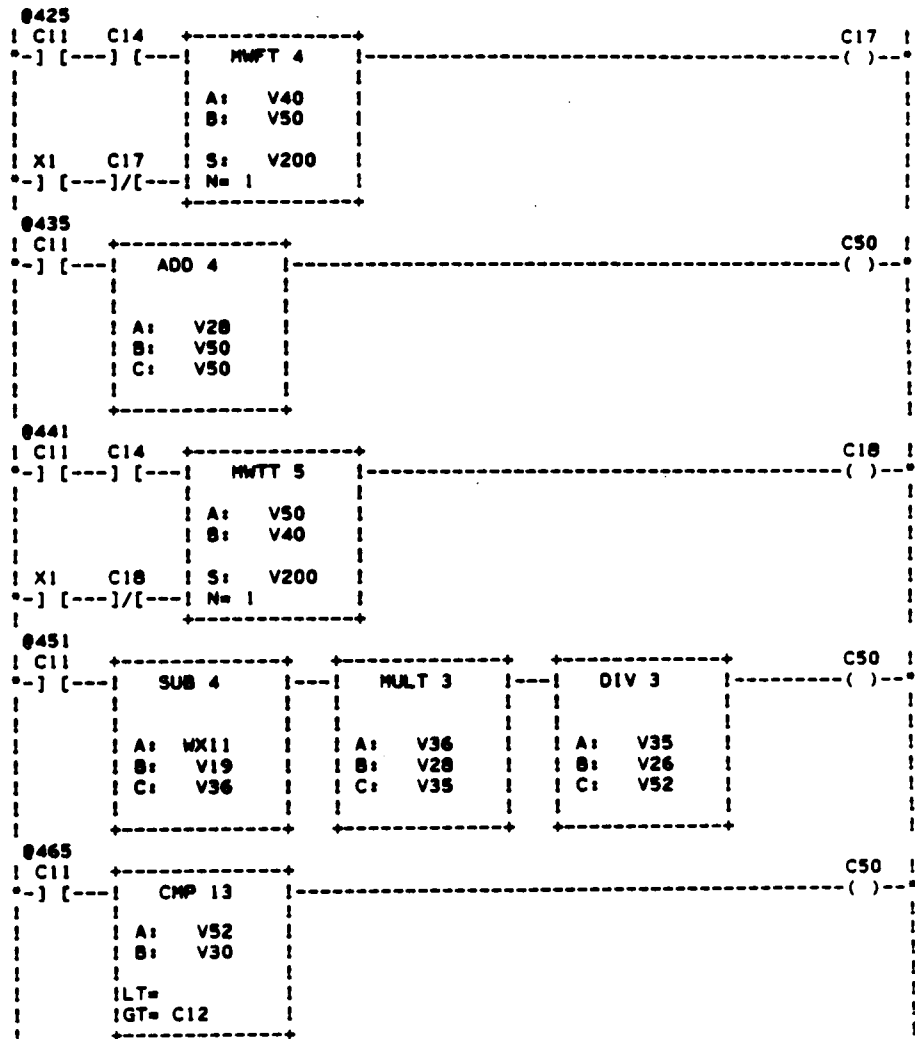
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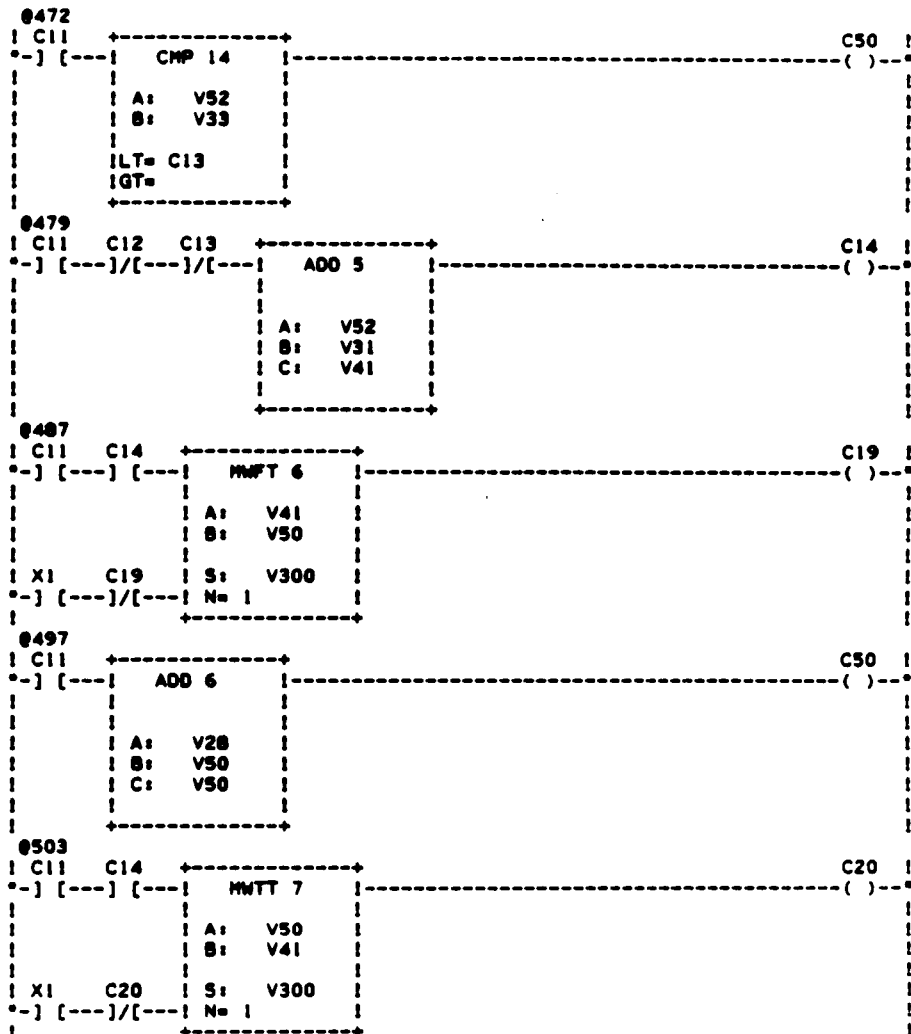
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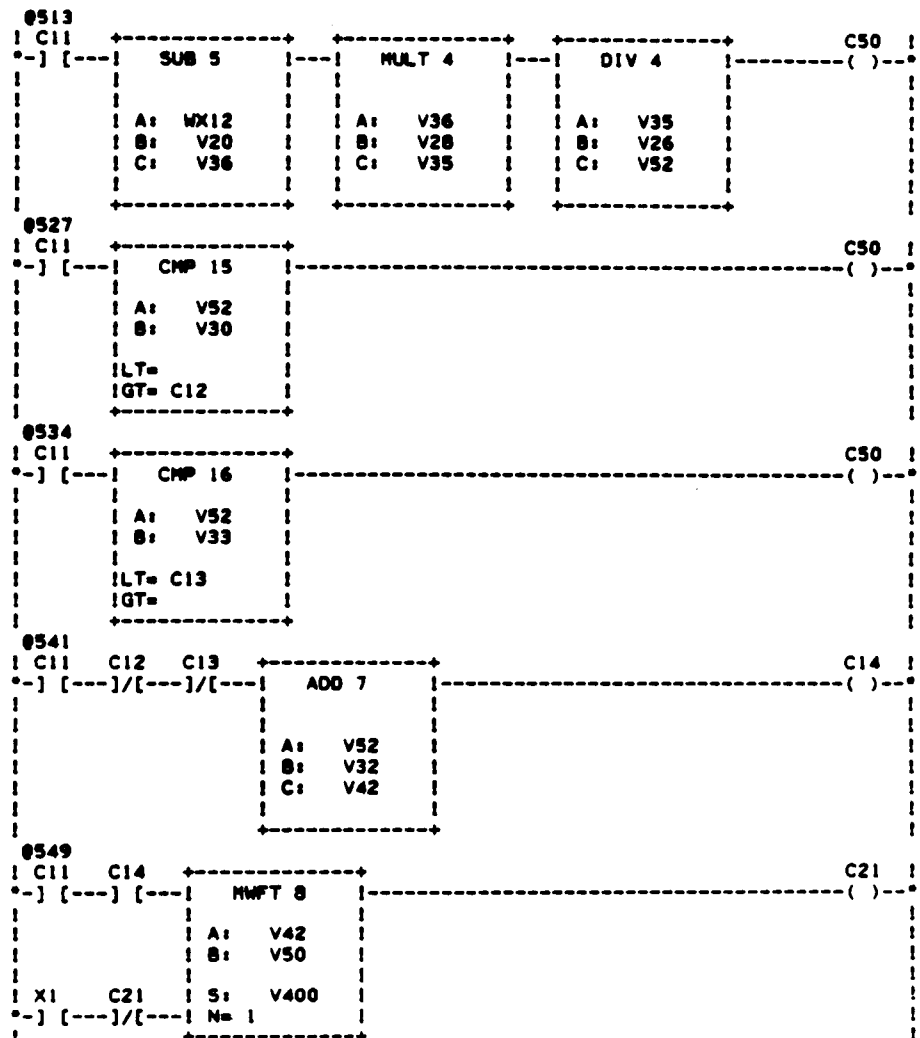
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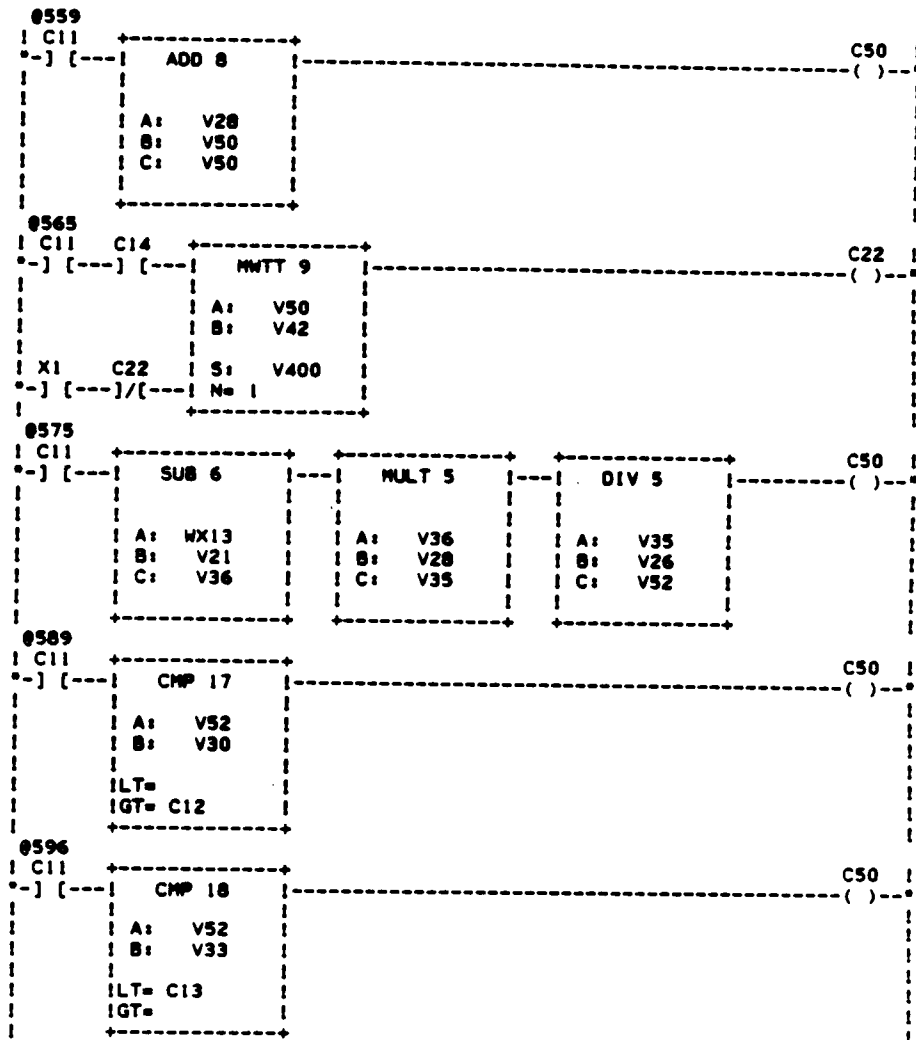
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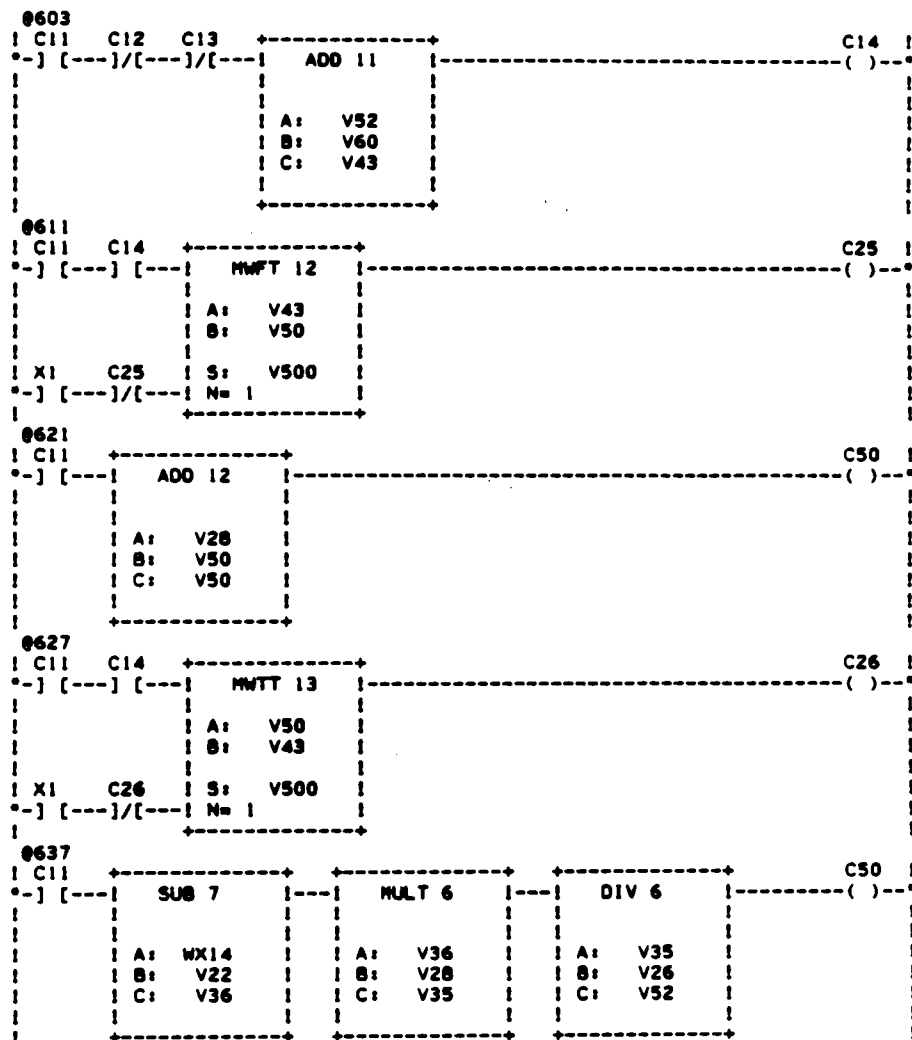
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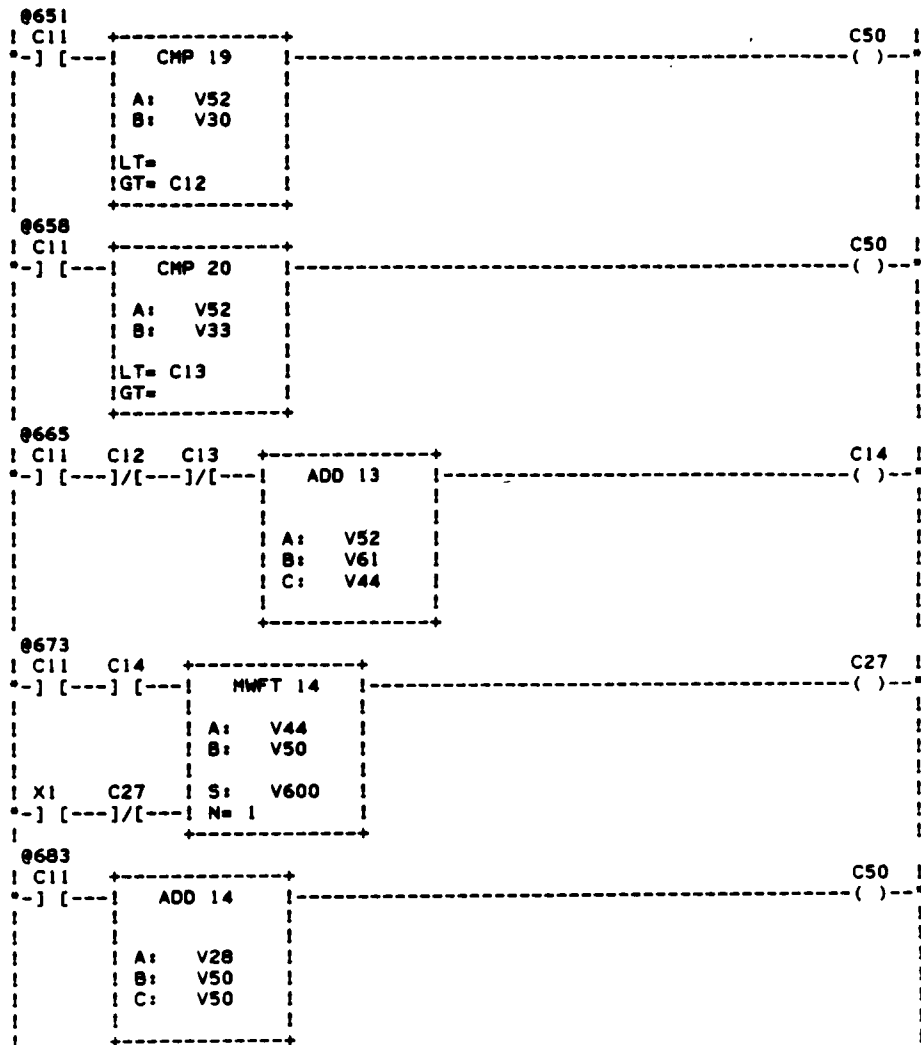
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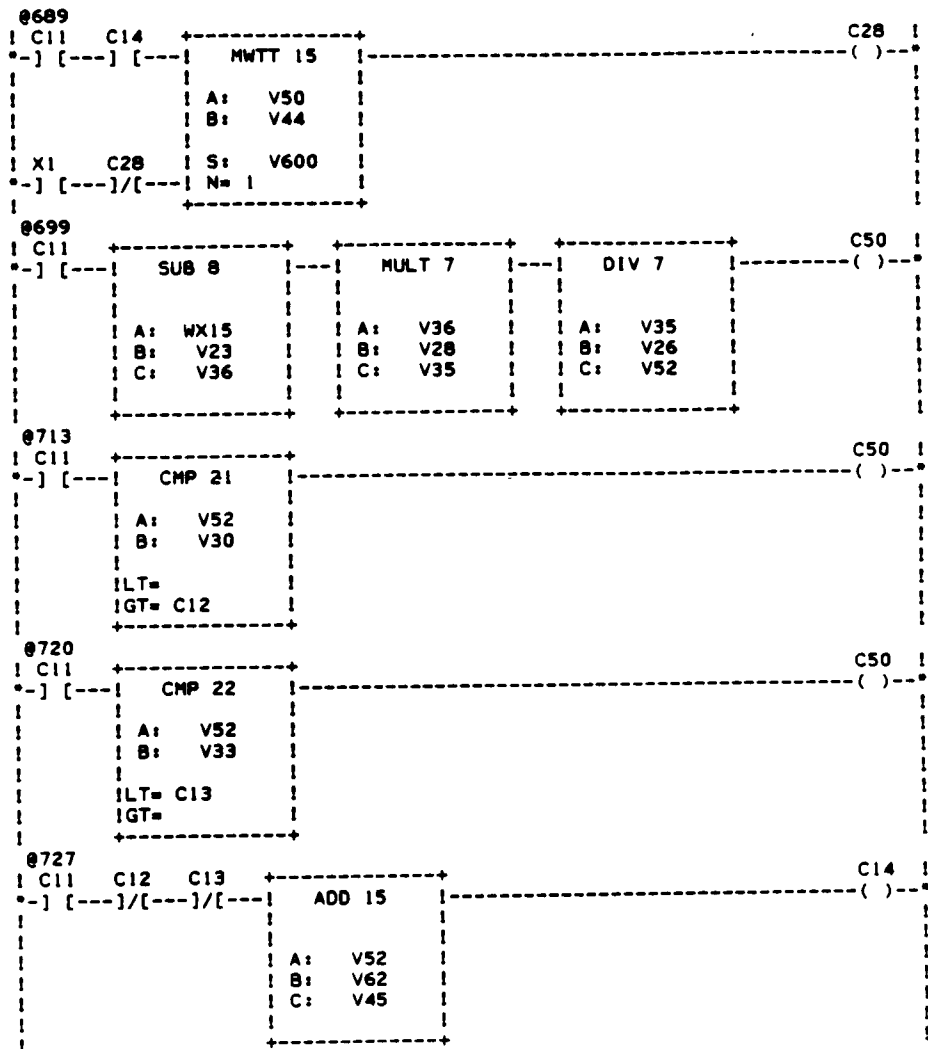
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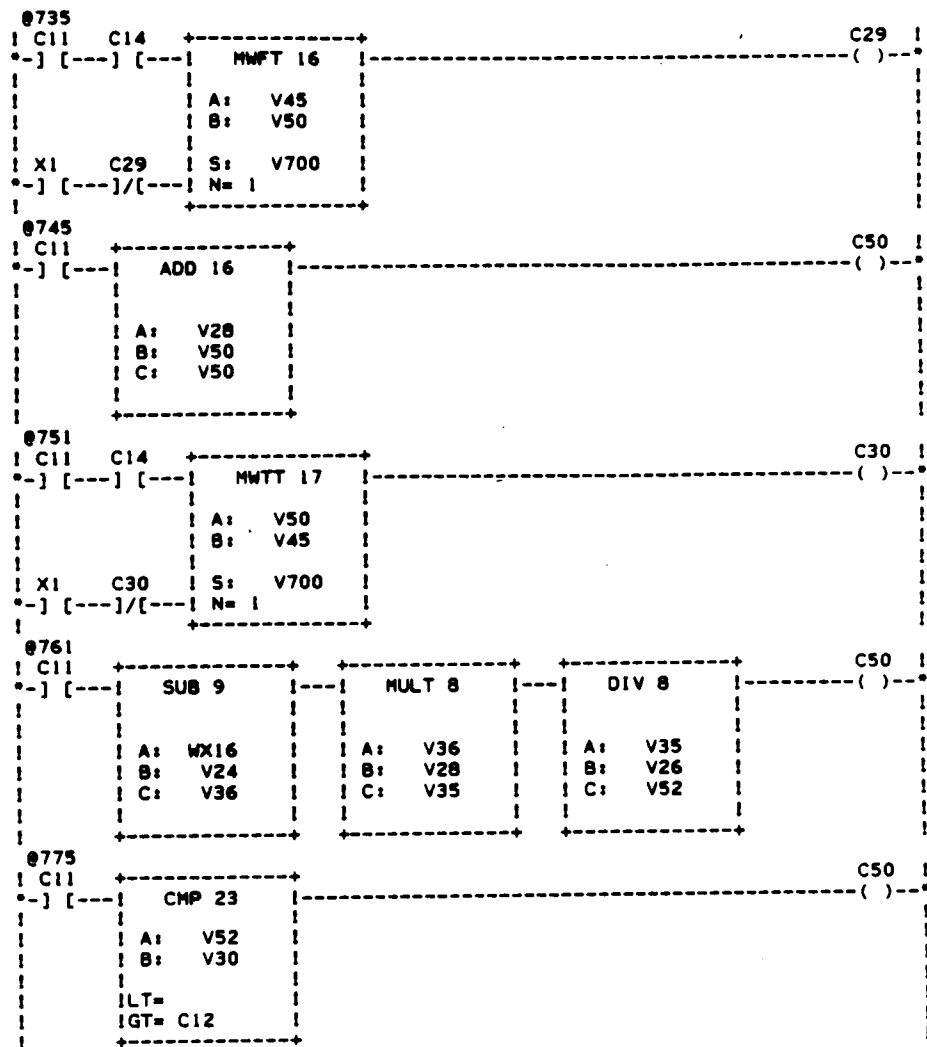
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0782
! C11 +-----+-----+ C50 !
!-] [---] [---] CMP 24 [---] ( )--*
!      | A: V52 |
!      | B: V33 |
!      |LT= C13 |
!      |GT=     |
! +-----+-----+
0789
! C11 C12 C13 +-----+ C14 !
!-] [---]/[---]/[---] ADD 7 [---] ( )--*
!      | A: V52 |
!      | B: V63 |
!      | C: V46 |
! +-----+-----+
0797
! C11 C14 +-----+ C31 !
!-] [---] [---] MWFT 18 [---] ( )--*
!      | A: V46 |
!      | B: V50 |
! X1 C31 | S: V800 |
!-] [---]/[---] N= 1 [---] ( )--*
! +-----+-----+
0807
! C11 +-----+ C50 !
!-] [---] ADD 18 [---] ( )--*
!      | A: V28 |
!      | B: V50 |
!      | C: V50 |
! +-----+-----+
0813
! C11 C14 +-----+ C32 !
!-] [---] [---] MWTT 19 [---] ( )--*
!      | A: V50 |
!      | B: V46 |
! X1 C32 | S: V800 |
!-] [---]/[---] N= 1 [---] ( )--*
! +-----+-----+
0823
! END !
!-] [---] ( )--*

```

VITA

Mack A. Marshall was born in Gatlinburg, Tennessee on February 6, 1959. He attended the elementary school in that city and was graduated from Sevier County High School in June, 1977. The following September he entered The University of Tennessee, Knoxville. Mack was employed as a co-op student by International Business Machines and as a summer development student by Texas Instruments before receiving a Bachelor of Science degree in Electrical Engineering in June, 1982.

Upon graduation, Mack accepted a permanent position with Texas Instruments. Continuing as a full-time employee, Mack began study toward a Master's degree from The University of Tennessee, Knoxville in September, 1982. He received the Master of Engineering degree with a major in Electrical Engineering in June, 1988. Mack was able to apply his experience as a design-assurance engineer to help complete the thesis requirements.