To the Graduate Council:

I am submitting herewith a thesis written by John W. York entitled "Testing a Multi-Chip Module Containing Untested Components." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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and Dean of The Graduate School

TESTING A MULTI-CHIP MODULE CONTAINING UNTESTED COMPONENTS

A Thesis

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ABSTRACT

This thesis research involved the testing of two Digital Signal Processor based Multi-Chip Modules which contained untested dies. Testing was performed using a custom-design printed circuit board. The design and development of the PCB were performed using tools produced by Mentor Graphics. Resources on the PCB provided an environment in which to test the MCMs. Results of the testing for both modules indicated that both MCMs were defective. One module's (module A) Vcc and GND terminals were directly shorted, and the other module (module B) had an unexpectedly high power dissipation. The suspected cause of the fault for module A was a defective substrate, while the problem with module B was suspected to be a faulty FPGA die, embedded on the substrate. Discussion of the potential enhancement of testability by using an embedded FPGA is also given.

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CHAPTER 1

Introduction

A MCM (Multi-Chip Module) is basically the integration of a PCB (Printed Circuit Board) system onto a silicon or some other type of substrate. Bare die IC (Integrated Circuit) components are used instead of packaged components. The use of bare dies along with MCM technology allows the component spacing to be much smaller compared to an equivalent PCB. There are several benefits in using MCM technology over the standard PCB technology for an IC system design.

First, there can be a significant increase in system operation speed since inter-chip routing on an MCM substrate has orders of magnitude less capacitance than a comparable PCB. Second, there is the benefit of smaller packaging of a system of ICs, which, in turn, can lead to reduced production cost and an advantage in market share. However, a major concern limiting MCM technology is testability.

1.1 Difficulties Testing MCMs

One of the major obstacles inhibiting MCMs to be a widely accepted and mass-produced technology is testability. In most cases, MCM testing involves the verification of substrate interconnects, logical connections and IC interaction functionality. Testing methods for ICs are difficult to apply to MCMs since they

often contain a heterogeneous mix of components. Even though the MCM module may have the physical appearance of a large IC, it would be impractical to test the MCM as a single IC on a standard IC tester.

The MCM cannot be considered as a single IC, but as a group of interconnecting ICs (an integrated SYSTEM). Custom testers have to be developed to test MCMs as a system. Unfortunately, MCM testers are usually unique to the specific design in that, unlike IC testers, they cannot be easily reconfigured to test other MCMs. The testing of MCMs can involve the use of capacitive or resistive probing with flying probes, high-density probe cards or electron-beam probe testing, all of which can be expensive and time consuming. It is possible for the cost of testing and validation to exceed the design and fabrication cost of the MCMs themselves [1-2, 5-11].

1.2 Boundary Scan

One method of reducing testing cost and time, thereby reducing overall MCM cost, is the utilization of boundary scan features found on some IC devices. If all devices on the MCM have boundary scan features, a complete substrate test is possible. Unfortunately, many IC devices, including custom designed ICs, do not incorporate boundary scan circuits; therefore, other methods of testing are needed [6].

1.3 Known Good Die

Known good die (KGD) is an issue for MCM testability, since untested dies may be assembled in an MCM system. A KGD is an unpackaged IC that has been tested to some degree or level of confidence. The level of confidence or testing can range from a simple DC test (while the die is still on the wafer) to more complicated and complete at-speed, functional validation tests.

With the advent of different levels of KGD, the functionality of ICs in an MCM can be assured *at some level* depending on cost. However, the IC interconnects and system functionality must still be validated as a complete module. There are two drawbacks with relying on KGD for an MCM design.

First, fully tested KGD of the highest level can be relatively expensive compared to their IC packaged equivalents. This can substantially raise the cost of an MCM, thereby overwhelming the benefits of using thoroughly tested MCMs over an equivalent printed circuit board. Second, not all ICs on the market today are available as KGD at any level.

Unfortunately, a standard by which to set KGD levels has yet to be established among vendors. For instance, a level 2 KGD from one vendor may only be equivalent to a level 1 KGD from another. As an example, the following are descriptions of the different available levels of KGD from Motorola's MPG96002DIE data sheet for their DSP 96002 series IC.

Level 1 and 3: DC Tested - *Die processed to levels 1 and 3 are of the same quality level as that used for assembly of Motorola commercial and military*

packaged products. Probe parameters have been selected which allow for high yield within the performance spectrum of the packaged product offerings. Packaged good yield data based on sample sizes typically much larger than that used for element evaluations is available. NO guarantees are made regarding die performance or data sheet parameters.

Level 2, 4, 5 and 6: AC/DC Tested - *Die processed to levels 2, 4, 5, and 6 provide known performance. High performance probe hardware allows utilization of the comprehensive testing associated with packaged die. In addition, die are stress tested at a voltage level appropriate to the particular processing technology. Test conditions are contained in the attached data sheet and apply to the junction temperature which is applicable to the specific processing level.*

Level 7: Burned-In Fully Tested - *Die processed to level 7 utilize die carrier technology which allows for testing at multiple temperatures and burn-in. Test conditions are contained in the Electrical Performance Characteristics of this specification and apply to junction temperatures from -55 degrees C to 125 degrees C. (Future Offering)*

1.4 Smart Substrates

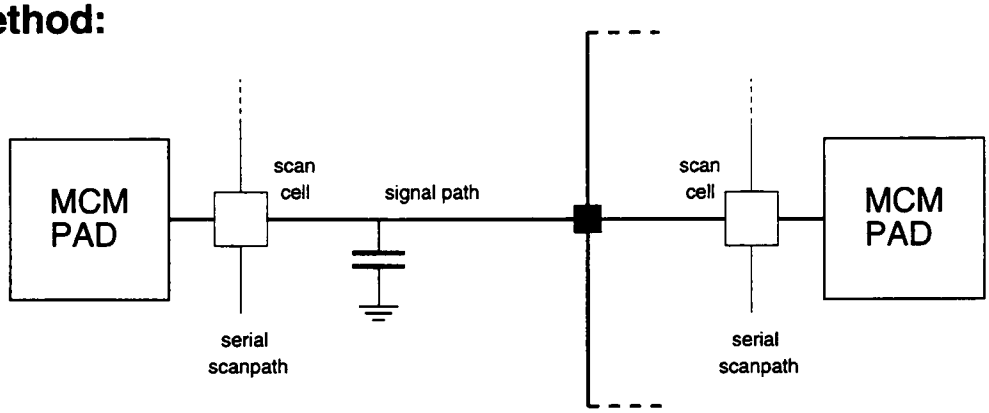
One method of testing MCMs is the use of Smart Substrates [1]. The main concept of Smart Substrates is the application of active silicon substrates. KGD is not necessarily a factor as Smart Substrates have the potential to tolerate incompletely tested dies and provide the needed testing capabilities. For example,

Smart Substrates can provide the means to control and monitor individual MCM dies from the module's pins. This allows the identification of faulty ICs after or during module assembly. If rework facilities are available, defective die(s) can be replaced which can effectively increase MCM yield. Examples of testing features, controllability and observability, that Smart Substrates can provide are boundary scan or Built-in Self Test [5].

There are two methodologies for Smart Substrate testing: (1) Standard boundary scan devices, scan cells, are placed in the signal path to be tested (ISP method), and (2) scan cells are placed beside the signal path (BSP method). Figure 1.1 shows the two methods. The ISP method has the advantage of testing the MCM at all stages of assembly, from bare substrates via partially mounted MCMs to fully assembled modules. This method can be fully compatible with current boundary scan methods and test systems (IEEE 1149.1).

The BSP method reduces test capabilities compared to the ISP method due to its organization. Like the ISP method, the BSP can provide the features of standard IEEE 1149.1 boundary scan, and can allow for bare substrate tests. Since the BSP method places scan cells in 'parallel' to the MCM pads, only a small capacitive load is seen during regular operation when the scan cells are disabled. Unlike, ISP cells, BSP cells cannot interrupt the signal flow between connected die, therefore, they are unable to control IC inputs which are already connected to other IC/MCM outputs. This restriction inhibits the testing of a partially assembled module. However, an IC under test on a partially or fully

ISP Method:



BSP Method:

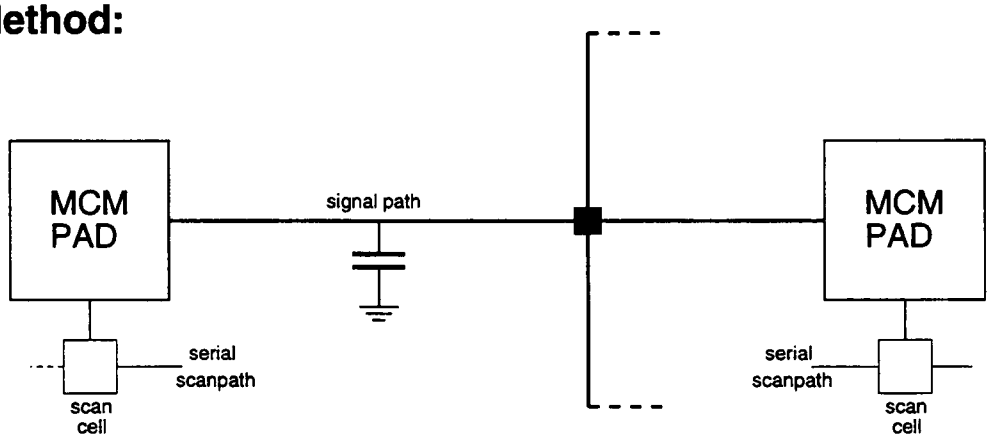


Figure 1.1: *Placement of Scan Cells for ISP and BSP Methods [6].*

assembled module can be tested completely by the BSP cells under certain conditions. Maximum benefit can be obtained from BSP scan cells by careful planning of the order of assembly and an appropriate test strategy.

System test of a fully assembled MCM is possible with BSP cells by stimulating and monitoring the external MCM I/O before and after mounting the MCM in its final package. By observing internal nodes via the BSP circuits, this test can be enhanced. However, testing of the MCM in its working environment is limited [5].

1.5 Embedded FPGA

An embedded FPGA (Field Programmable Gate Array) can have some of the testing benefits of Smart Substrates of either the BSP or ISP method. However, unlike Smart Substrates, testing of an MCM system can occur within its working environment during operation. Using the concept of Reconfigurable Computing, an FPGA can be reconfigured from its 'glue logic' use to become testing and monitoring logic device. Moreover, the testing with the FPGA can be self contained as with a BIST (Built-In Self Test) configuration.

1.6 Purpose of Thesis Research

The purpose of this research is to test DSP (Digital Signal Processor) based MCMs which contain untested dies. Each module is planned for a gradual test-

ing scenario, starting from the simple continuity check between Vcc and GND (ground) to more complicate functional validation. If an MCM is to be rated as a functional unit, then each die within the module is required to be functional, not only on individual bases, but also interactively with other dies within the MCM system.

A proper environment is needed to test the DSP MCMs. A testing environment can be provided in several ways; however, a significant part of this thesis research involves the development and fabrication of a test/demo PCB, designed specifically for the DSP MCMs. The PCB provides wire routing (external to the MCM) and device resources to allow for the testing of the modules. The external wiring and resources are needed not only for testing, but are also needed for basic functional operation of the MCM. Vital resources such as system clock, power and configuration circuitry are provided by the PCB for the modules. Moreover, those same resources can also be used to demonstrate the DSP MCMs' technology capability. Specifics of the PCB are discussed later in the report.

The DSP MCMs available for this thesis research have an embedded FPGA on the substrate, one die per module. If the FPGA component can be established as a functional unit, then it can, in turn, be used to test the rest of the devices within the MCM. This concept was briefly described in the previous section and is discussed in further detail later in the report.

1.7 Report Overview

An overview of the prototype DSP MCM used for this thesis research is presented in the Background section, Chapter 2. Chapter 3 conceptually discusses the testing possibilities with an embedded FPGA and discusses some considerations for designing a microprocessor based MCM for testability. A brief discussion of the design and development of the PCB, the PCB testing environment and functional testing methods for the MCM (using the embedded FPGA) is presented in Chapter 4. Testing results are presented in Chapter 5. A Summary, Conclusions and Future Work section is contained in Chapter 6.

CHAPTER 2

Background

2.1 Prototype MCM

Figure 2.1 shows a flow diagram of the DSP MCM designed at the University of Tennessee [4]. Placement and routing were done by Tim Powell, a previous graduate research student, using tools from the Mentor Graphics Design Manager. There are a total of six ICs on the MCM including a Motorola 32-bit digital signal processor. Figure 2.2 shows a photograph of the MCM that was fabricated by Micro Module Systems via the MIDAS Service [4]. The other ICs within the module include two Micron 64K x 16 SRAM (Static Random Access Memory), an Atmel 128K x 8 EEPROM (Electrically Erasable Programmable Read Only Memory), a Xilinx XC4010 series FPGA and a 12-bit Analog-to-Digital Converter (ADC) from the Oak Ridge National Laboratory. Note that a full data bus (Port A) is interconnected to the Xilinx 4010 FPGA die within the module. Since this was an experimental prototype and none of the dies were KGD, most of the I/O (Input/Output) of the FPGA (and other ICs) were brought out as external I/O for the module. This helps isolate ICs for testing and for fault isolation.

To allow for testing and demonstrations, many of the MCM's I/Os from the FPGA will need to be 'wrapped' back into the MCM. These 'wrapped' back

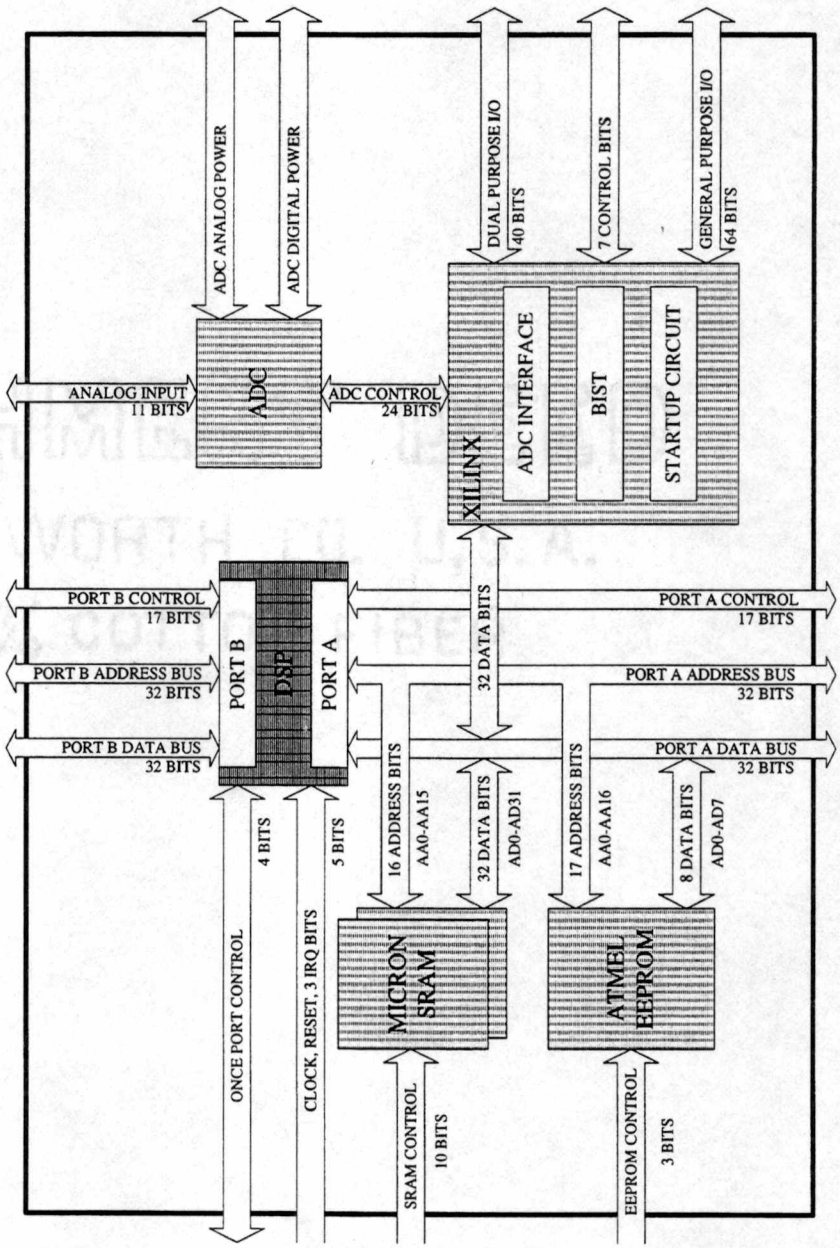


Figure 2.1: *Flow Diagram of DSP MCM.*

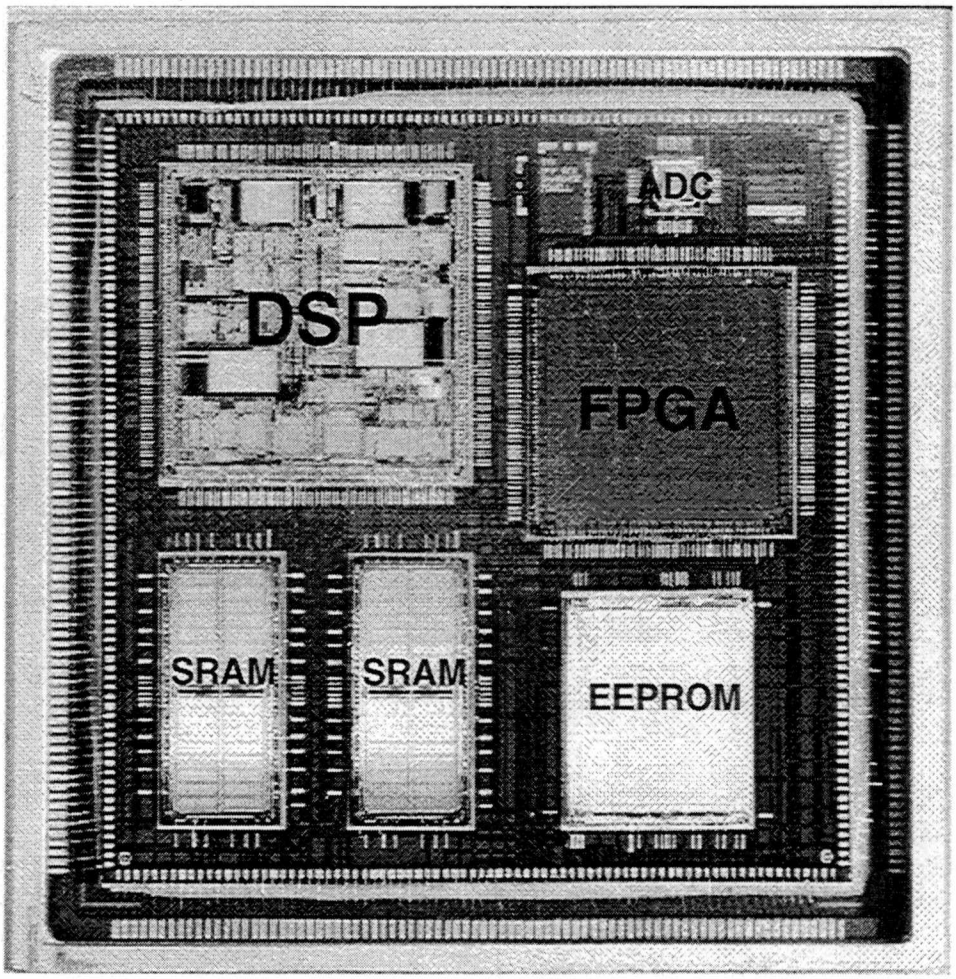


Figure 2.2: *Photograph of the DSP MCM.*

connections should allow the FPGA to connect to the address bus (Port A) and control bus of the DSP and other ICs in the module. Some of the FPGA-MCM I/O will be used to communicate with the MCM's environment. A custom designed PCB was developed to allow for these 'wrapped' back connections, to provide resources for FPGA configuration and to allow communication between the MCM and its environment. Figure 2.3 shows a block diagram of the PCB that will be used to provide this environment. The PCB is described in more detail in Chapter 4.

It is important to note that the FPGA in the MCM was not originally designed into the module just for testability. The FPGA was deemed as necessary glue logic to provide operational resources for the MCM system. For example, the FPGA can provide logic for an address decoder, an interactive user I/O interface and the means for reconfigurable computing with the DSP processor. During the development process, concern for testing of the MCM became an issue. It was decided that the FPGA could be utilized to validate and test the DSP MCM, with the flexibility of the MCM I/O and the proper environment. To implement this concept, the FPGA, with the resources of the test/demo PCB, would need to be tested first.

2.2 Concerns

Some areas for concern are: (1) none of the ICs on the any of the DSP MCMs are KGD; (2) proper placement and connection of the wire bonds should be

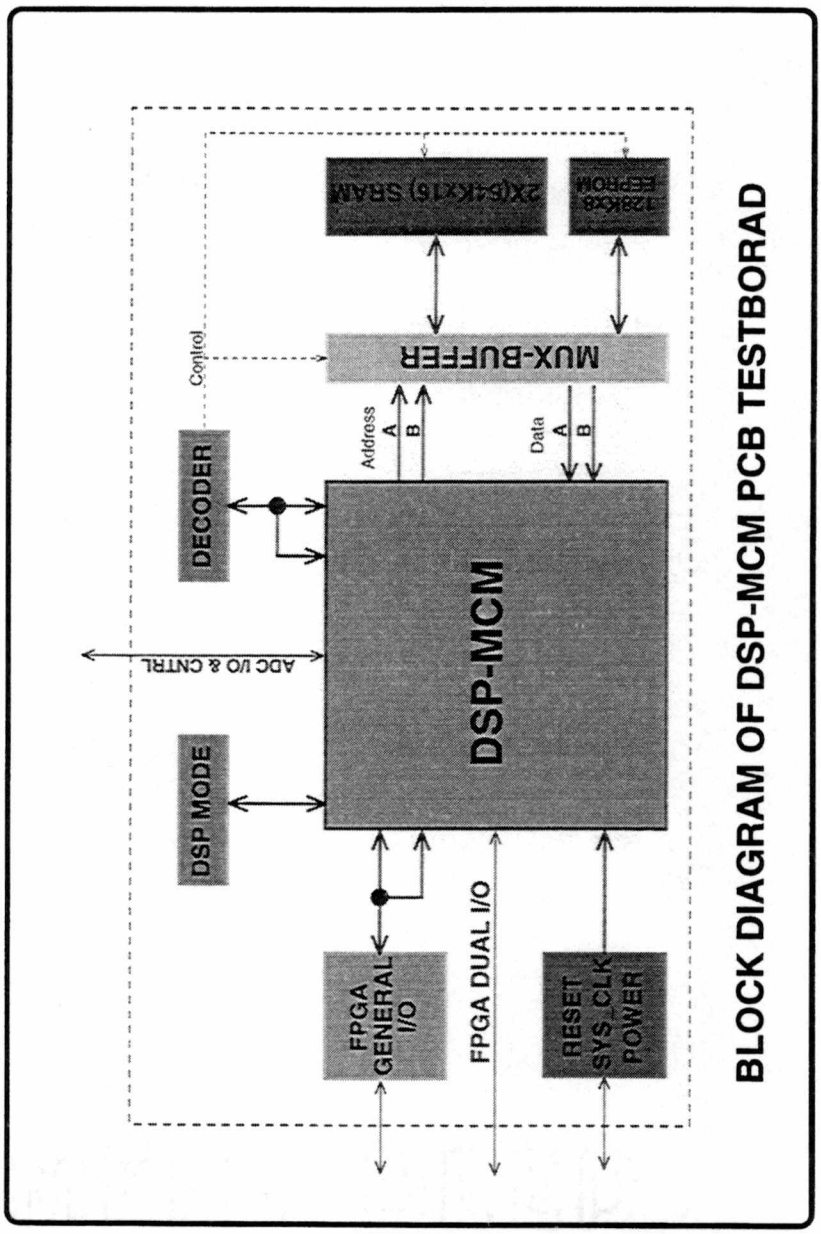


Figure 2.3: *Flow Diagram of the Test Environment PCB.*

verified visually; and (3) proper interconnections of ICs for desired functionality need to be checked against design specifications. The test/demo PCB developed for the DSP MCM needed to isolate most faults that occur in one or more of these areas.

CHAPTER 3

Testing with an Embedded FPGA - Designing for Testability

MCMs with an embedded reconfigurable FPGA in the design can enhance its testability. As with some IC designs, the MCM system must be designed and planned for testability to maximize the effectiveness of the testing. As shown in Figure 3.1, the MCM design should not only consider functionality but also testability. The figure also shows that the design for testability can benefit from the design for functionality. If functionality dictates that data and control buses be connected from the microprocessor to the FPGA, those same buses can also be utilized by the function of testability.

3.1 Possible Methods

Critical signal paths can be connected to the FPGA I/O, and some of the FPGA logic can be configured as scan cells for boundary scan. This setup is similar to that of the BSP method for Smart Substrates. However, BSP testing using an embedded FPGA would be possible only after final assembly of the dies onto the substrate so bare substrate tests would be impractical.

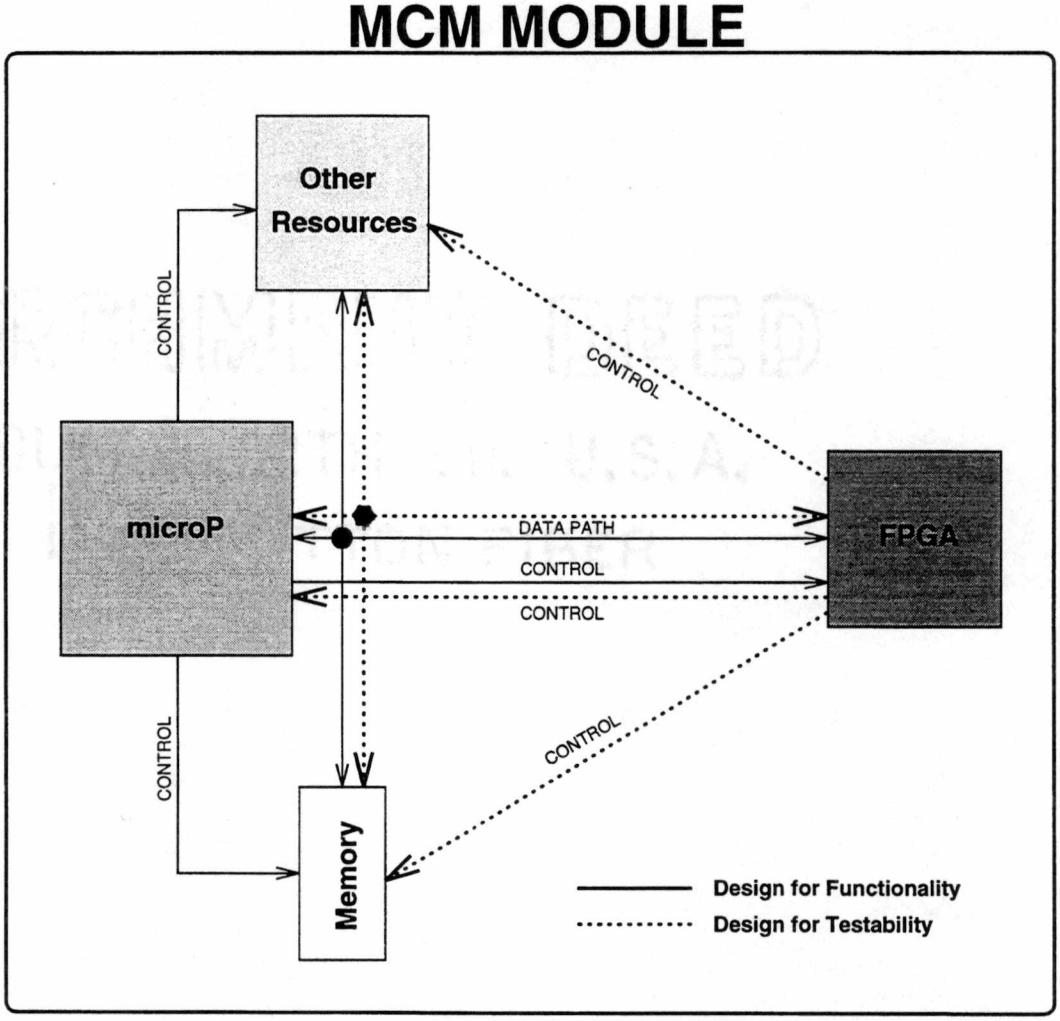


Figure 3.1: *Designing for Testability for a Typical MCM.*

Careful planning for testability, proper connectivity and configuration of the FPGA not only can allow for an emulated BSP methodology, but can also allow thorough testing of the MCM in its environment. The FPGA can be configured as a pseudo built-in logic analyzer that can monitor core dies within the MCM in real time. This allows testing of not only the hardware aspect, but also allows monitoring of software execution in a limited manner.

Moreover, an FPGA can be configured as a self-tester for the module by creating stimuli and monitoring results. If the FPGA has access to the external I/O of the module itself, testing results can be sent as output and observed as they become available. With the proper reconfigurable resources and connectivity, the FPGA can provide all of the above forms of testing in a virtually self-contained unit.

3.2 FPGA Size for Testability

It has been stated above that the testability of an MCM can be enhanced with an embedded FPGA with the proper connectivity and configuration. The question arises as to what size (number of logic gates/cell blocks) FPGA to use, and what connections must be made between the FPGA and other ICs on the MCM and between the FPGA and the module's I/O. The optimum size is dependent on the particular design. The questions are important since an FPGA can occupy a significant amount of routing and substrate area. The size of the FPGA can depend on the complexity of the MCM and the desired complexity

of testing required. Figure 3.2 gives a qualitative illustration of the spectrum of possibilities.

3.3 Design Considerations

It can be assumed that there is no one setup that will work for all MCMs, as applications of MCMs vary. However, for processor-based MCMs, some common bases can be set. In a processor-based MCM, the critical signal paths will likely be the address and data buses. Therefore, the FPGA I/O should be allowed to tap into those signal lines.

In order for the FPGA to isolate chips for testing or fault identification, the FPGA would need access to the control lines of the other ICs. This allows the FPGA to 'turn off' other devices for isolated testing and enables an algorithm to identify a functionally faulty IC in the system. As with the BSP Smart Substrate method, the necessity of using KGD can be avoided, excluding the FPGA itself. With proper rework facilities, faulty components could be replaced on the MCM to increase yield.

In general, it would not be a wise decision to include an FPGA in an MCM design just for testing purposes. A FPGA can take up a significant amount of area on the MCM substrate. It is recommended that an embedded FPGA be used for testing purposes if an MCM core design already incorporates a reconfigurable FPGA in the module. Unfortunately, design constraints may not allow an embedded FPGA to be used for testing. For instance, designing for testabili-

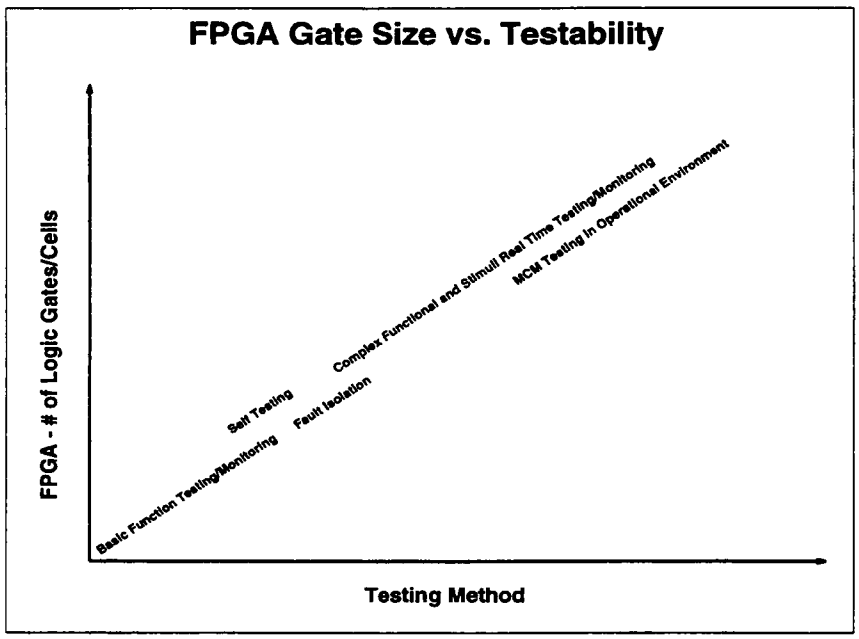


Figure 3.2: *FPGA Gate Size vs Complexity of Testing.*

ty may require additional routing and/or increases in FPGA gate count and/or increases in the number FPGA I/O. The gate size of the FPGA can be increased without significantly increasing the overall size of the IC. However, even with the additional gates, using the FPGA for module testing and validation may still be impractical, if additional routing is required and routing within the substrate is saturated. If an FPGA is included in an MCM for resource or glue logic, the overall design of the MCM needs to be adequately flexible to allow for design expansions and additions. Moreover, if the FPGA is not an KGD, design considerations in external I/O routing must be made to help established it as a KGD. It is essential that the FPGA be an KGD before it is used to test the remainder of the MCM system. If the FPGA is not established as a high level KGD, it could

be difficult to determine sources of random occurring faults.

The ideal case would be to construct MCMs will all KGD, and to allow testing to concentrate on functional validation. Unfortunately, using all KGD can be costly and still would not solve the problem of system testing. However, if the FPGA is to be the center for testing and module's functional validity, it may be prudent to use, at least, a KGD FPGA in the MCM design.

CHAPTER 4

The PCB and Functional Testing the DSP MCM

4.1 Purpose for PCB

The primary reason for developing a test/demo PCB for the DSP MCM is to provide an environment in which the MCM can be operated by a user for testing and demonstrations. The PCB provides necessary resources for proper mode operation and functionality of the MCM (i.e., SYS CLK and Address Decoder). Resources such as LEDs (Light Emitting Diode) and data ports are provided on the PCB to allow the MCM to communicate with the user. Bypass and backup circuitry and resources are also provided to isolate faults and allow continued testing in the event of faults. The board also provides redundant memory resources that will allow the continual testing of the MCM in case of memory device failures or faults. These external memory resources are the same as those within the MCM.

The PCB environment will help establish the FPGA as a KGD before it is used for testing. This environment will also allow testing of the MCM to be continued regardless of certain faults that may occur within the module. There are 'wrapped around' connections on the PCB for the MCM. The 'wrapped around' routing, as described before, allows connections between the FPGA and the main address

bus and the control lines of the other ICs, including the DSP unit. The PCB is designed to allow the FPGA to be the main interface between the MCM and its environment.

Configuration and reconfiguration of the FPGA will also be performed via resources provided by the PCB. The circuitry necessary for configuration was designed exactly like that of the Xilinx XC40xx-PC84 demonstration board, since its design is a proven one [16]. Most of the MCM I/O tasks will be given to the MCM FPGA, since it can be easily configured for I/O. Therefore, it is imperative that the FPGA be thoroughly tested and established as a KGD. The I/O configurations of the external LEDs, DIP switches and push-button switches on the PCB were also designed exactly like that of the Xilinx XC40xx-PC84 board. By using already proven circuitry, the design time for the whole PCB was reduced, significantly.

4.2 Development of MCM Test/Demo PCB

As with the DSP MCM itself, tools from Mentor Graphics were used to design and develop the test/demo PCB. Figure 4.1 shows a schematic of the PCB design that was created using Design Architect Tools in Mentor Graphics. Notice from the schematic that there are several lines from the MCM routed back to the MCM itself. This particular design of the board will allow the MCM to operate in a virtual 'stand alone' configuration, with the FPGA providing resources necessary for operation. Of course, the 'stand alone' configuration is only possible provided

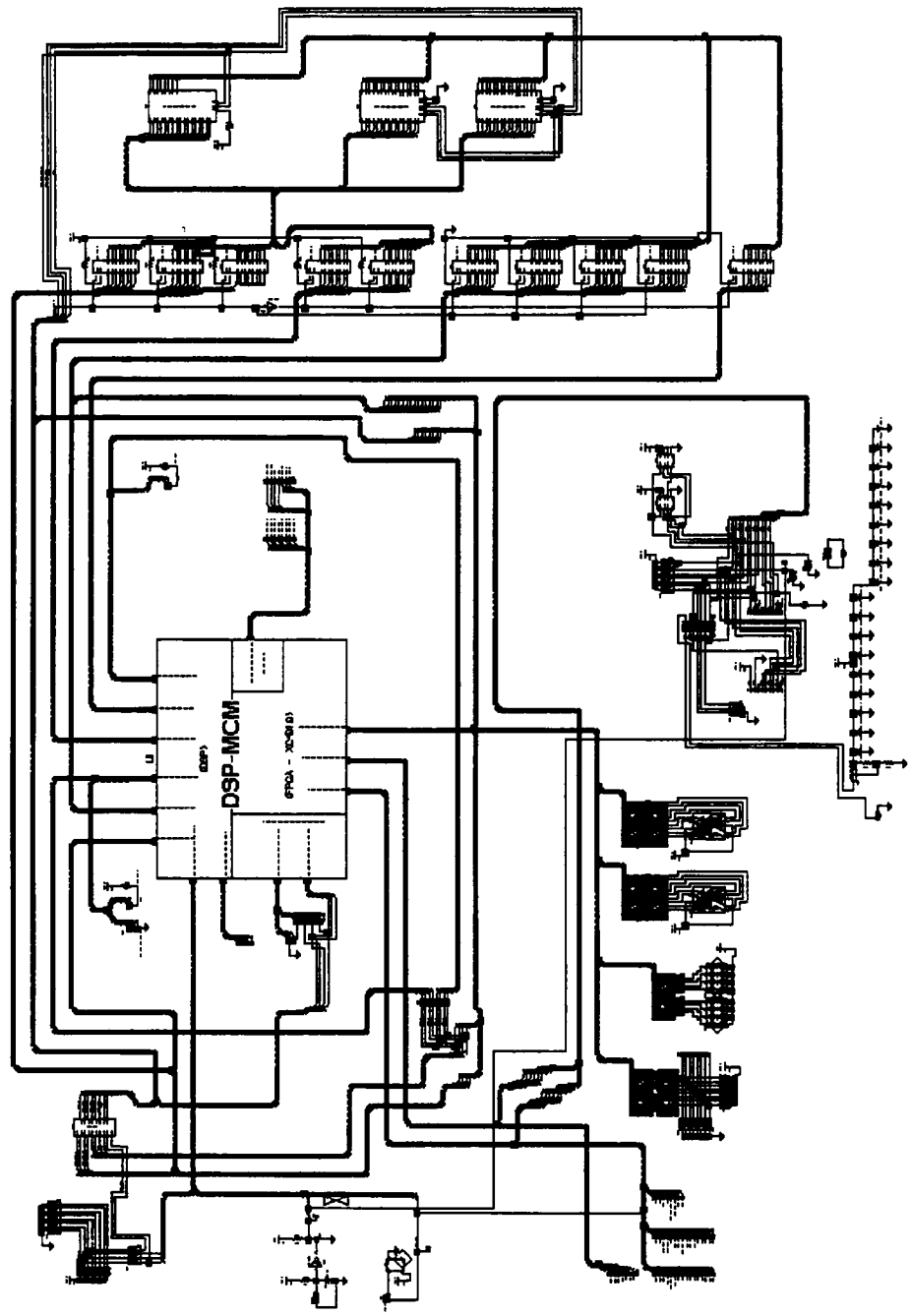


Figure 4.1: *Schematic of the Test/Demo PCB from Design Architect.*

that all the ICs on the MCM are functioning properly.

The MCM itself is not be placed on the PCB, but instead a custom designed socket from Nepenthe was used to interface the MCM to the PCB. The pin size and configuration of the MCM socket are non-standard; therefore, the Librarian Tools in Mentor Graphics had to be used to design a custom geometry configuration of the MCM socket. A geometry defines the physical parameters (i.e., size, shape, pin spacing, etc.) of an object used in the design. The geometry was then used in the Librarian and Layout Tools to establish a 'footprint' of the MCM socket on the PCB. Other geometries of devices on the PCB, including the PCB itself, had to be created in Librarian as well.

Two major difficulties were encountered during the development of the PCB. First, there was the tedious task of learning the various tools of Mentor Graphics, and determining which of the many tools were actually needed to develop the test/demo PCB. Second, technical terms and nuances of PCB technology had to be learned in order to begin layout of the design. Figure 4.2 show a flow diagram of the design process used to design the PCB in Mentor Graphics. Of the many available tool packages from Mentor Graphics, only five were used to go from the conceptual stage to the final product.

Using the Automatic Router in the Layout Tool in Mentor Graphics, 100 percent completed routing was achieved with no apparent routing or component placement errors or violations. Using an Ultra Sparc Sun workstation, complete routing of the PCB took approximately 3 hours, cycling through 30 iterations for

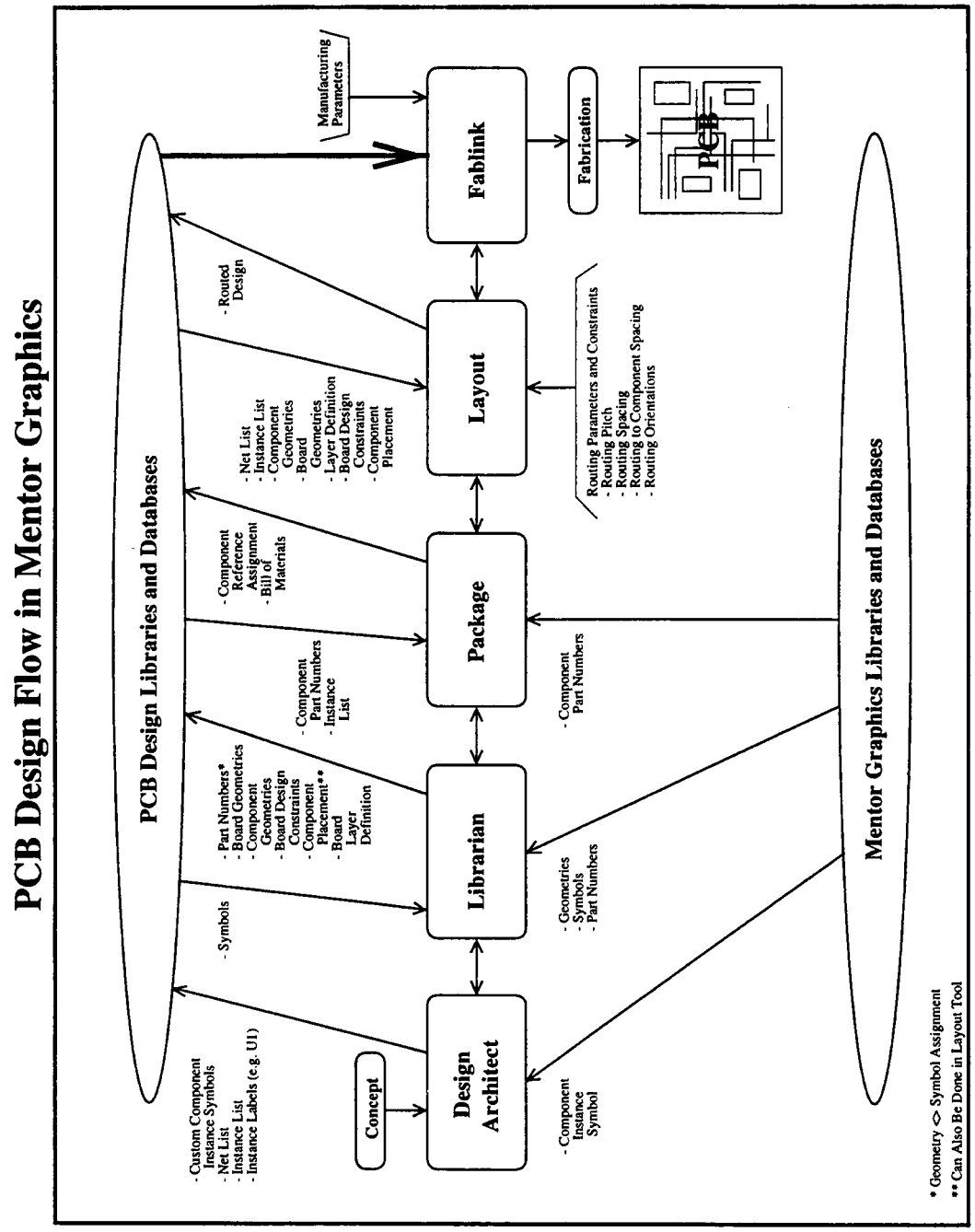


Figure 4.2: *Flow Diagram of the PCB Design Process in Mentor Graphics.*

design and 20 iterations for manufacturing. Component placement was performed manually in Librarian using a 0.01 inch snap-to-grid placement. Then the Fablink tool was utilized to generate the gerber file for each layer along with the drill table. Figure 4.3 shows the layout of the PCB in Fablink tool with all signal and power layers. The PCB was manufactured by Multek via MIDAS. Note the many intervias between the MCM and PCB resources. The board is comprised of four signal layers and two (VCC and GND) power layers. This level of complexity is needed to provide the MCM a testing and functional environment.

If the MCM were to be manufactured as a stand alone application unit, many of the 'wrapped around' connections (MCM to glue logic resources to MCM) would be fabricated within the substrate of the MCM. For example, on the PCB, address lines from the prototype MCM are traced to a PAL (Programmable Array Logic) device, and then traced back to the MCM. This was necessary since an address decoder was not incorporated into the MCM design. The PAL would be configured as a custom address decoder. For an application, the address lines would be routed internally to the embedded FPGA, which would be configured as an address decoder, along with other necessary logic. However, since this MCM was a prototype, most I/O ports of the ICs within the MCM were routed to external pins to aid in testing of the MCM. Having most all of the I/Os available should help establish ICs within the MCM as functional, partially functional or nonfunctional units.

Table 4.1 shows some of the electrical characteristics of the components on the

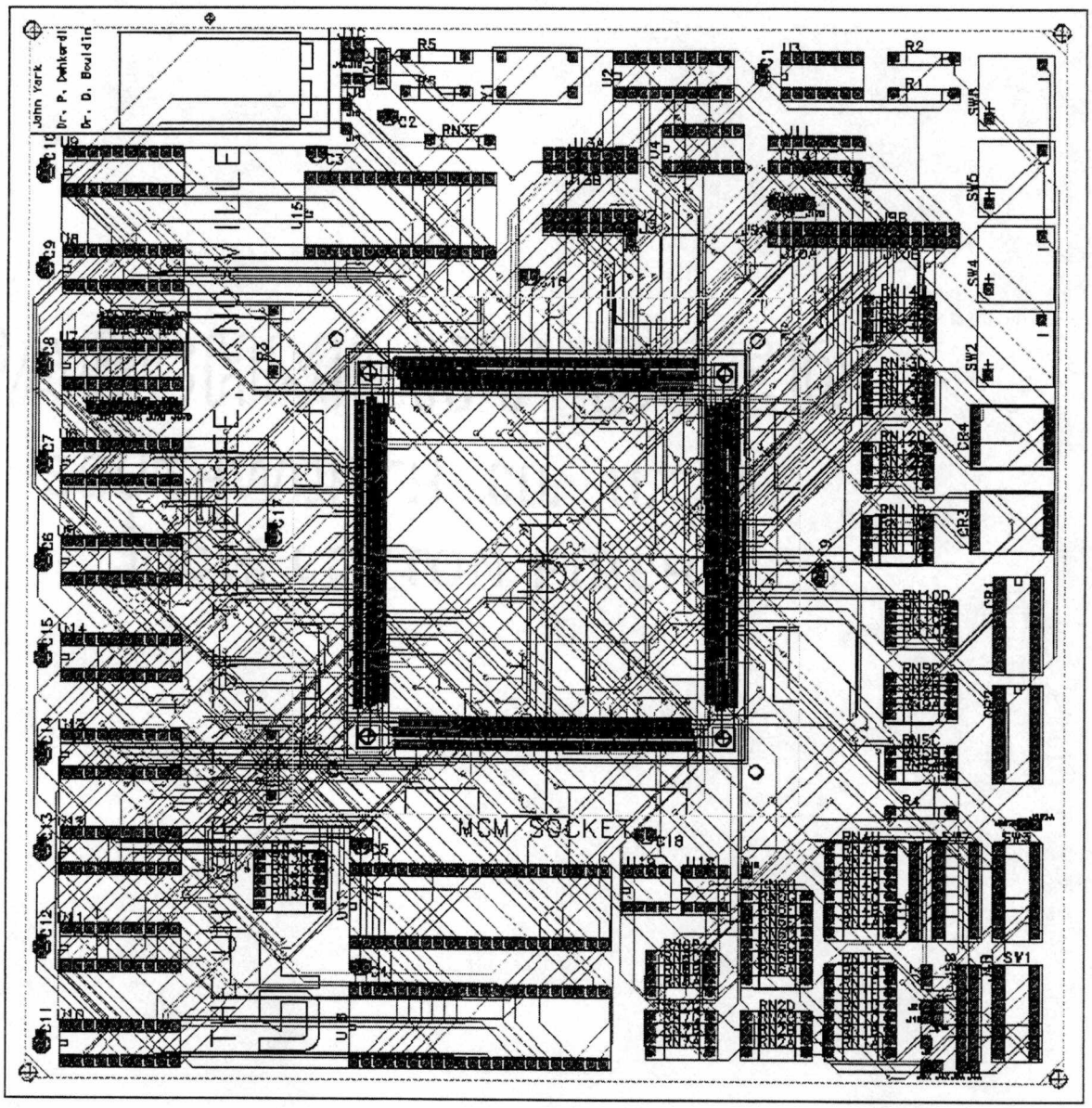


Figure 4.3: *Actual Layout of the PCB (From the Layout Tool).*

Table 4.1: *Electrical Characteristics of Devices on the PCB.*

Electrical Device Charateristics

Device	Vih	Vih	Voh	Vol	Icc	CL	tpd(freq)
DSP 96002	2.00	0.80	**	0.40	30mA	10pF	40MHz typical
Xilinx 4010	2.00	0.80	**	0.40	30mA	15pF	25ns(40MHz)
Atmel EEPROM	2.00	0.80	4.20	0.45	300uA	10pF	120ns(8MHz)
Micron SRAM	2.20	0.80	**	0.40	45mA	5pF	25ns(40MHz)
AMD 16L8 PAL	2.00	0.80	2.40	0.50	80mA	6pF	(18MHz)
74HC14N	3.15	0.90	4.40	0.33	20uA	10pF	31ns(32MHz)
74HC245AN	3.15	0.90	4.40	0.33	80uA	10pF	58ns(17MHz)
74UC4066AN	3.15	0.90	n/a	n/a	40uA	15pF	n/a

* All values are worst case. All V values are in volts. All tpd values are with a 50 pF load unless otherwise stated.

** Per available data sheets: Voh = 2.4V @ Ioh = -4.0mAand Voh = Vcc-1 @ Ioh = -10uA.

PCB and within the MCM. Using the values in Table 4.1, the theoretical power dissipation in static or wait mode should be approximately 0.83 watts. Worst case noise margin is 200 mV, between the I/Os of the 16L8 PAL and Micron SRAMs device. However, one concern is the Voh output voltage values of the DSP 96002, Xilinx 4010 and Micron SRAM ICs when Ioh = -4.0mA and when Ioh = -10uA. On the PCB, the address and data buses from the DSP 96002 are routed externally (of the MCM) to several 74HC245 buffer ICs. According to the table, the buffers require a minimal value of 3.15 volts for a valid logic high with an absolute input current value of 5uA. Therefore, care must be taken during operation of the PCB/MCM system not to drive the output of the address and data lines of the DSP 96002 more than -10uA. It is uncertain what the output voltage of the DSP 96002 would be at output currents just below -10uA and just

above -4.0mA. This concern also applies to the SRAM memory chips located on the PCB, since those devices are interfaced with 74HC245 buffer ICs.

4.3 Functional Test Algorithms

Using the resources on the test/demo PCB, the Xilinx XC4010 FPGA would be isolated on the DSP MCM, and VHDL (VHSIC (Very High Speed Integrated Circuits) Hardware Description Language) configuration using PowerView or Synopsys can be created to perform a simple functional test of the FPGA. The test/demo PCB allows the used of XCHECKER or serial EPROMs (Erasable Programmable Read Only Memory) to configure the MCM FPGA [16]. Unlike the DSP and other components within the MCM, testing of the FPGA can be interactive with output to the LEDs and input from the DIP/push-button switches. Since the FPGA is linked to the module's SRAMs via a 32-bit data bus, the FPGA can also be used to test these memory ICs. Once confidence is established as to the total functionality of the FPGA, it can be configured as a pseudo logic analyzer. Using the connections provided by the PCB, the FPGA can monitor data and address lines on the MCM during operation or in stepping mode. Moreover, it may be possible to use the module's ADC as a type of voltage meter, since the control of the ADC is directly linked to the FPGA within the MCM.

After the FPGA is established as a functional unit (KGD), testing of the MCM and its components can begin. One of the simplest testing that can be done is data monitoring (pseudo logic analyzer) with fault isolation. For example,

the FPGA can be configured to 'turn off' all of the ICs except for the internal EEPROM and DSP processor. The Motorola DSP processor has a built-in boot algorithm that allows the loading of an 4K instruction set from a byte-wide memory source. Simple instruction codes can be loaded into the EEPROM. With the DSP initiated in the proper mode, transfer of address code and data (instruction code) can be monitored by the FPGA. Since the address bus has to go through the FPGA first for decoding, it can determine if the DSP processor is sending the proper addresses. This should be simple since the addressing will be sequential and an initial address value will be known.

Monitoring of the address bus will validate or invalidate not only the DSP's address capability, but also the routing lines from the DSP's address bus. If the instruction set within the EEPROM is kept to an alternating, repeating code, the FPGA can monitor the data bus for errors from the EEPROM. Since this particular FPGA has an internal system clock, it can stop operations once an error or fault is detected and notify its environment (PCB - LEDs) the probable cause of the error/fault. If the FPGA receives an incorrect address midway through the boot cycle, it can flag the DSP as the fault cause. Then, if an incorrect instruction code is seen, it can flag the EEPROM as the cause of the error. Figure 4.4 illustrates the basic algorithm for the pseudo logic analyzer. However, if incorrect address values and/or incorrect instruction codes are seen by the FPGA continuously from the start, it will be difficult to determine whether the device or the routing is at fault. In this case, a more complex algorithm will

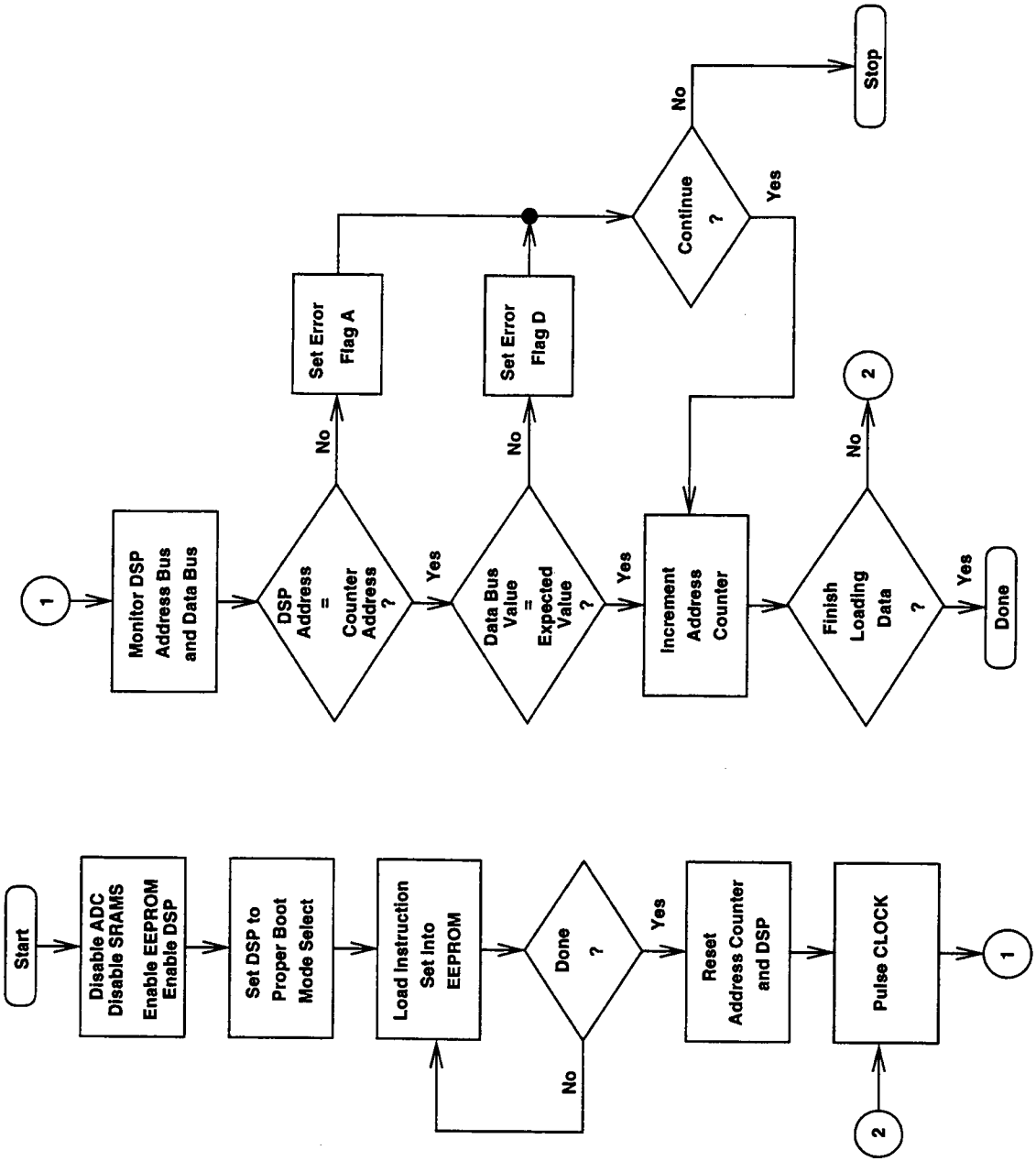


Figure 4.4: *Flow Diagram of Pseudo Logic Analyzer.*

be needed for the FPGA to determine the difference between routing faults and device faults.

Testing of the MCM and its components can also be done without the FPGA. This may be necessary if the FPGA cannot be established as an KGD. Using the PCB, a test routine can be isolated to the DSP and memory units. First, the operation of the processor would be isolated from the other ICs. The processor would be set to boot from an 8-bit external memory after reset. A simple functional algorithm, created using a DSP 96002 based C-compiler, can be booted up from the external on-board EEPROM. The algorithm could be as simple as have the processor address and send data to the external on-board SRAMs, which can be monitored by the user. The same method could be used to perform simple check tests on the internal SRAMs and EEPROM.

The test routine would be kept as simple as possible, so that any faults that occurred, whether it be something in the MCM or the algorithm source code, can be easily identified. Also, successful execution of the simple test routines can be a confidence enhancer to the functionality and validity of the MCM design. Once functional verification is performed on every IC within the MCM, the test/demo PCB can then be used as an environment or resource (i.e., LEDs and extra SRAM memory) to demonstrate executions of DSP algorithms in the DSP MCM system. Algorithms can vary from computations as simple as FFT/IFFT (Fast Fourier Transform/Inverse Fast Fourier Transform) to more complex operations involving sounds or images.

CHAPTER 5

Testing Results

5.1 Visual Inspection of Wire Bonds within the DSP-MCM

Before the DSP MCM modules were manufactured, a premanufacturing prototype was constructed to verify the assembly process. This MCM was visually inspected to verify the physical construction of the module. A low power microscope was used to inspect visually all wire bonds and pads between each IC and its respective I/O ring. The wire bonds and pads around the MCM substrate and module I/O pin pads were also inspected for physical flaws.

The results of this visual inspection allowed for the manufacturing of the final modules. No significant flaws were found in the wire bonds or pads within the MCM module. There were, however, a few 'near misses' between wire bonds and respective pads in various places within the module. Since this module was a prototype, it was determined that the actual modules would be assembled with higher quality. Due to limited resources in equipment, the actual MCM modules were not visually inspected for flaws. It was assumed that the actual modules would be manufactured with at least the same quality as the premanufacturing prototype module.

5.2 Validating the PCB (Before Assembly)

Before the PCB was used to test the DSP MCM, the board itself was put through a series of tests to verify its design. The first and most important test checked the continuity and resistance between the Vcc (+5 volts) and GND planes. The PCB(s) passed this test with no continuity and infinite resistance between the Vcc and GND planes.

A test to check continuity and resistance of the many signal lines was also performed to ensure that all signals were available for testing. Moreover, those signal lines which default to logic high or logic low were also checked to validate their proper connection to Vcc or GND. All of the signal lines of the PCB were validated and deemed to have proper connectivity according to the design schematic.

However, one flaw was found in one of the signal lines that connected to an MCM socket pad from a select DIP switch pad. The current limiting resistor on this particular signal line appeared to be directly bypassed or shorted. A continuity check on this signal line, from the DIP switch pad to the MCM socket pad, indicated a zero resistance. An attempt was made to repair this flaw physically, but due to the complexity of the PCB, inherent damage to other nearby signal lines may have occurred from the repair. Fortunately, this flaw did not inhibit the full assembly of the PCB, nor did it prevent the testing and validation of the MCM itself.

5.3 Validating the PCB (After Assembly)

After all of the resource components were assembled on the PCB, the same series of tests mentioned in the previous section was performed on the PCB to ensure proper assembly. All tests went through with no apparent flaws. Then with all of the components assembled on the PCB, except the MCM module itself, power was applied to the PCB with digital multimeters monitoring voltage at Vcc and current draw.

Using a standard 9 volt battery through a regulator as the power source, the voltage at Vcc was measured at a steady 5.15 volts. The current draw was less than 100 milliamps. Power was applied constantly over a 5 minute interval, and all values remained constant, with none of the devices on the PCB exhibiting increased thermal activity.

5.4 Validating the PCB with DSP-MCM Module

Testing of the MCM modules began with the determination of pin 1 on the module. This was vital since the known location of pin 1 on the module would ensure proper orientation when placed in the MCM socket on the PCB. At the time of testing, only two MCM modules were available for validation. One module was still in the original packaging from the vendor, while the other had been handled and examined. The module that had been handled was tested first, since it had already been exposed to the environment. For some reason, if the

PCB inadvertently damaged or destroyed the module, a new, undisturbed module would still be available. The module that had been opened was labeled 'module A,' and the module still in its packaging was labeled 'module B.'

From available notes and data sheets, pin 1 was determined for the MCMs. Module A was placed in the MCM socket. Then continuity and resistance were measured between Vcc and GND using a multimeter. The result was a short circuit between Vcc and GND. Pin 1 may have been incorrectly determined, so the module was rotated 90 degrees clockwise. The same results appeared: short between Vcc and GND. Module A was rotated 90 degrees clockwise another two times and each time a short between Vcc and GND appeared on the multimeter. Once module A was removed from the PCB, there was no short between Vcc and GND.

Since module A appeared to be defective, it was used to verify the exact location of pin 1 for module B with respect to the module's external pinouts. Each module can be opened and the substrate with bonded ICs exposed for testing and/or inspection. From available notes, data sheets and IC I/O maps, it was known that pin 1 of the MCM was given to the signal, Port A Data Bus 17 (AD17), which was from the DSP IC at pin/pad 155. Module A was opened and using the smallest probes available, pin 1 was physically verified. Referring to the photograph of the MCM in chapter 2, pin 1 is located at the top right hand corner of the MCM's I/O pad ring.

With pin 1 of the MCM physically verified, module B was placed on the PCB.

Continuity and resistance were checked between Vcc and GND. A short circuit did not appear between Vcc and GND, but several thousand ohms were measured between the two power planes. With a multimeter set to monitor voltage at Vcc and with the proper mode selects for the DSP and FPGA ICs (static or wait) via DIP switches, power was applied to the PCB. The voltage measure at Vcc upon power up was approximately 3.0 volts. The power was quickly turned off, and the MCM removed from its socket. Power was then reapplied to the PCB. Voltage at Vcc measured close to 5.0 volts.

To verify the previous results, module B was placed back into the socket. A multimeter was set to measure voltage at Vcc, and another was set to measure current from the 9 volt battery. Power was applied and again the voltage Vcc was measured to be approximately 3.0 volts. The current drawn from the 9 volt source was measured to be close to 200 milliamps, well beyond the normal operating conditions for a standard 9 volt battery. Moreover, observation of the PCB during the application of power revealed that segments of both 7-segment LEDs were illuminated, as if receiving a low signal from the FPGA. (The circuit design for the LEDs enable them to come on when the signal source is in a logic low state.) The partial illumination of the 7-segment LEDs was unexpected since all I/Os of the FPGA should have been tristated with no configuration.

To be able to continue testing, a more powerful battery was needed to supply the PCB. Two 6 volt flashlight, lantern batteries were obtained and connected in series to supply the PCB's voltage regulator with approximately 12 volts (since

the regulator needs at least 8 volts on its primary side to operate). The larger batteries were able to supply higher currents than the single 9 volt battery without a significant voltage drop.

With the new power source, the PCB with module B was powered up with multimeters measuring voltage at Vcc and current from the batteries. The results were unexpected as approximately 5.0 volts appeared on Vcc with nearly 700 milliamps being drawn from the power source. This meant that the PCB, supposedly in static mode, was dissipating nearly 3.5 watts compared to the theoretical value of 0.83 watts. As before, the same segments of the 7-segment LEDs were illuminated, although brighter this time due to a more substantial power source. Even though a thermal probe was not available, the 'finger touch' method was used to determine if any of the devices, including the MCM, had unusually high thermal activity. The MCM itself did not exhibit any extraordinary thermal activity; its temperature can be best described as 'luke warm.' Thermal activity seemed to be nonexistent for the rest of the components on the PCB except for one, the voltage regulator. The regulator was, to the touch, extremely warm, and its thermal activity had increased its case temperature significantly above room temperature. Power was turned off, and a TO-52 case heatsink was mounted on the voltage regulator along with some thermal grease. This was done to help the regulator maintain thermal stability which would help prolong its operational longevity.

The next step was to ensure that all logic inputs for each component on the

PCB were connected to either a signal path or terminated to Vcc or GND. Most all of the IC components on the PCB, including the MCM, belong to the CMOS (Complementary Metal Oxide Silicon) family of logic. One concern in using CMOS logic is that care must be taken not to allow floating inputs in the circuit design. Allowing the voltage to 'float' at the gate of a CMOS circuit can have indeterminate and/or undesirable results at the corresponding output(s). The PCB was checked for floating inputs against the design schematic, and none were found to be physically unconnected or floating.

It was difficult to ascertain the cause of the relative high power drain of the PCB with the MCM. One theory was that the mode selects for the DSP and FPGA components within the module were not set properly for static mode upon power up. The mode selects for both devices were checked against data sheets and notes, and were found to be properly set.

In case of errors or discrepancies in the data sheets and notes, a test routine was performed in which every possible combination of the DIP switches were set to every possible mode select for both the DSP and FPGA components. In the first part of the test routine, the PCB was be powered up with a new mode select, and the PCB was observed for changes. This was done until all possible mode selects were exhausted for both the DSP and the FPGA. The last part of the test routine involved the same basic steps as the first part, except mode selects were changed while the PCB was continuously on.

Both parts of the test routine brought about no change to the response of

the PCB and MCM. For each mode select, whether during or after power up, the PCB would still draw approximately 700 milliamps, and the same segments of the 7-segment LEDs would be illuminated. In other words, this test routine yielded nothing as for determining the cause of the relatively high power drain of the PCB with the MCM.

One last theory to explain the cause of the high current draw was that perhaps pin 1 on the MCM was not actually pin 1. Because of this it may have been possible that some of the pins of the module were getting crossed between signal, Vcc and GND. However, this being the case, the MCM may have already been damaged from all the previous testing. To verify that pin 1 of the MCM was indeed, pin 1, a test was performed similar to that performed on module A. Module B was rotated in the socket in 90 degree steps, and at each step, continuity and resistance was measured across Vcc and GND. The results of the measurements showed a short circuit between Vcc and GND, until the module was rotated back to its original position. Pin 1 was indeed pin 1, assuming the module was not damaged during previous tests.

5.5 Other Possible Contingencies

The PCB has a few design flaws that may inhibit or adversely affect testing and validation of the MCM module. Unfortunately, these flaws were not discovered or realized until after the fabrication and assembly of the PCB and during initial testing of the MCM module. Three major flaws of the PCB are clock signal

termination issues, power supply and power consumption and thermal effects.

Figure 5.1 shows the proper connectivity of the primary clock signal to various units on a PCB. Routing from the clock source to other units must be equal length and minimize the use of vias and crossovers. Each clock signal trace should be 55 ohms impedance, with a 47.5 ohm series terminating resistor as close as possible to the clock source.

The PCB for the DSP-MCM module was expected to operate around 40MHz. While this clock speed is no longer considered fast by current standards, the frequency is significantly high enough to consider termination issues which include capacitive trace loads, trace resistance and signal reflections. This would not have affected initial testing of the MCM module, as vectoring and monitoring tests would be operated well below 40MHz. However, full scale, at speed (40MHz) functional tests or demonstrations would be affected in terms of high frequency performance.

The available power supply on the PCB will probably need to be increased, in terms of wattage, for actual full run tests of the MCM. Currently, the voltage regulator on the PCB is rated for a maximum sustained power delivery of 5 watts. The regulator will probably need to be able to supply at least 10 watts with 5.00 volts at Vcc. This assumes that the MCM and all the resources on the PCB are at full operation, at a speed near 40MHz.

In relation to the power supply of the PCB, thermal analysis may be required to prevent the MCM and PCB from unpredictable operation and even self

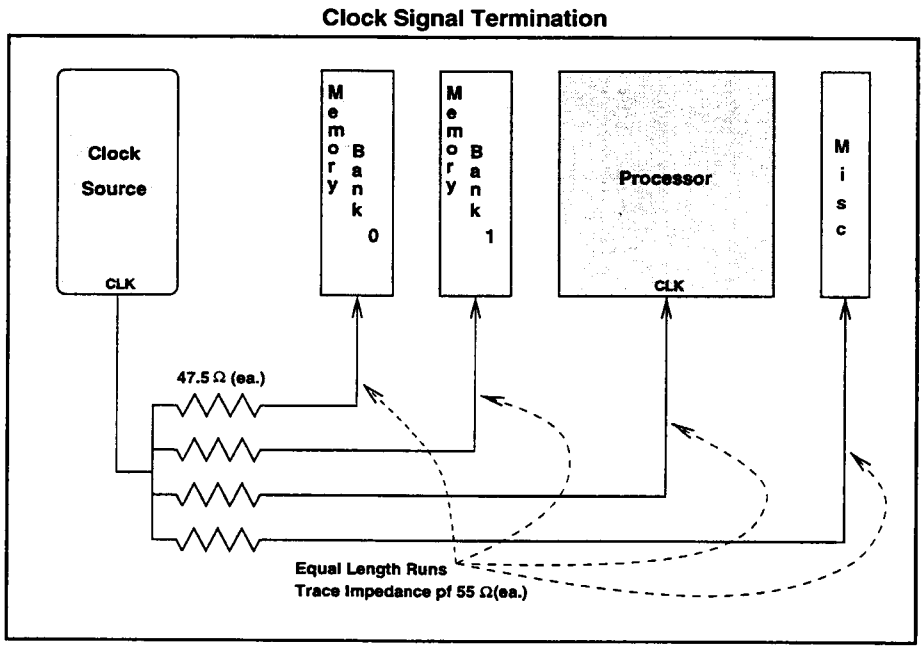


Figure 5.1: *Proper Termination of Clock Signal Lines.*

destruction due to high thermal activity. Because of time constraints, thermal analysis of the PCB with the MCM module was not performed before the manufacturing and assembling of the PCB. The AutoTherm Tool in Mentor Graphics can be used to perform the thermal analysis with little effort. Since the DSP-MCM module and test/demo PCB were designed using the Mentor Graphics tools set, all that is needed to perform thermal analysis are thermal parameters of the PCB, MCM and all devices on the PCB.

CHAPTER 6

Conclusions, Summary and Future Work

The purpose of this thesis research was to test the DSP MCMs which contain untested dies. Unfortunately, results of the testing indicated that both modules, A and B, had critical flaws. While it is not immediately clear the defects of the MCMs, some educated speculation can be derived from the testing results. If it is assumed that the construction quality for module A was at least good as the premanufacture prototype module, the short circuit could be attributed to a faulty substrate or a faulty IC within the MCM. However, it would be more likely a fault with the substrate, since a preliminary DC test would have been performed on each IC at the foundry before wafer separation.

If the same can be said for module B as for module A, in terms of construction quality, then its undesired response, upon power up, could be attributed to the same causes as module A. However, because of the unexpected illumination of segments of the 7-segment LEDs, which are directly connected (via series resistors) to the FPGA I/Os, the fault seems to lead inherently to the FPGA IC within the MCM. Moreover, since the FPGA's power dissipation rating is second only to that of the DSP, some fault associated with the FPGA could have contributed to the high current draw of the PCB with MCM.

There is another factor which could have contributed to the unexpected high power dissipation of the PCB with the module. The DSP IC within the MCM could have caused the unusual power consumption. The DSP 96002 has two main ports, A and B, both of which contain a 32-bit address and data bus. The logic design of the MCM allowed the whole 32-bit address and data bus of port A to be accessed externally. However, for port B, only 16-bits of the address bus and 8-bits of the data bus were allowed to be I/O for the MCM. It cannot be assured that the other 16-bits and 24-bits of the address and data bus, respectively, were properly terminated to Vcc or GND. Otherwise, the unused I/O would be left 'floating' which could have undesired effects on the operation of the device.

Desired test results and continued testing were not possible with the MCMs available at time of testing. This was due to limited equipment resources and time constraints. Therefore, possible future work could include the further investigation of the problems described in the previous chapter. A microprobe station and logic analyzer, in conjunction with the PCB, could determine and isolate the cause(s) of the problems with both MCMs.

Other possible future work could include the redesign of the test/demo PCB. The redesign should address the possible contingencies stated in chapter 5. If the MCM ever does reach a point to demonstrate its technology, these issues would become critical to proper, fully functional operation. At the very least, the ability for the embedded FPGA to enhance functional testing for an MCM system would be proven.

MCM designs that include a reprogrammable FPGA for glue logic can have the benefits of enhanced testability. Even though additional design costs may be needed to consider using the FPGA for testing purposes, the benefits of testability can far outweigh those costs, depending on the interconnections and size of the FPGA in the design. Again, it is not recommended that an FPGA be incorporated into an MCM solely for testing. Design for testability utilizing an embedded FPGA is recommended only when an FPGA is necessary as a resource for the MCM system.

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