September 4, 1973

To the Graduate Council:

I am submitting herewith a thesis written by Vernon Gene Fendley entitled "Development of a CMOS Control Logic for a Width-Modulated Binary Rebalance-Loop of a Strapdown Gyroscope." I recommend that it be accepted for nine quarter hours of credit in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

L. Vaughn Eldredge
Major Professor

We have read this thesis
and recommend its acceptance:

E. D. Kennedy

G. C. Bishop, Jr.

Accepted for the Council:

Hilton A. Smith
Vice Chancellor for
Graduate Studies and Research

DEVELOPMENT OF A CMOS CONTROL LOGIC FOR A WIDTH-MODULATED BINARY REBALANCE-LOOP OF A STRAPDOWN GYROSCOPE

A Thesis

Presented to

the Graduate Council of

The University of Tennessee

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Vernon Gene Fendley

December 1973

ACKNOWLEDGEMENTS

The author is indebted to his Major Professor, Dr. T.V. Blalock, for his valuable suggestions and continued assistance throughout the preparation and writing of this thesis.

Appreciation is also expressed to Dr. E.J. Kennedy and Dr. A.O. Bishop for providing data and helpful discussions.

The author's sincere appreciation is extended to Mr. R.D. McKnight, who supplied necessary electronic techniques, and Mr. Mike Galyon, who constructed the logic circuits.

A particular acknowledgment is due Mrs. Carole F. Byrd for an expertly typed manuscript.

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ABSTRACT

The primary objective of this study was to analyze, design, breadboard, and experimentally evaluate a new control logic section of a width-modulated binary rebalance loop for strapdown gyroscopes using CMOS (Complementary-Symmetry/Metal Oxide Semiconductor) logic blocks. An auxiliary objective of this study was to design a new control logic section which would perform scale factor selection by examination of the data train.

A comprehensive examination was performed on a previous TTL (Transistor-Transistor Logic) design of a logic system for strapdown gyroscopes, developed by HS (Hamilton Standard) with particular emphasis placed on the proper operational functions instead of on the logic organization. A new design of the control logic incorporating CMOS devices and the HS logic organization was implemented and experimentally evaluated by feeding the logic with a variable-width limit-cycle generator which used the 0-16 blanking signal for synchronization. The limit-cycle used was constructed using TTL logic.

This study has established that the control logic of a width-modulated binary rebalance electronics loop using the HS organization can be implemented using CMOS low power devices with the addition of a few logic pieces. After implementation and evaluation of the CMOS logic design, it was found to function as reliably as the HS TTL logic design. Typical 10-90% rise and fall times of the CMOS logic were found to be approximately 10-30 nanoseconds. The total power consumption for the CMOS design was measured at 207 mW in the low mode versus 10.35 W for the TTL design and 212 mW in the high mode versus 10.6 W for the TTL design.

An attempt was made to design another type of control logic based on the examination of the data train for mode selection. The design goal was to implement a control logic requiring fewer logic pieces than the HS logic. No way was found to accomplish this goal with the available CMOS devices.

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CHAPTER I

INTRODUCTION

As a result of the study on the Hamilton Standard (HS) TTL (Transistor-Transistor Logic) control logic[1] of a width-modulated binary rebalance electronics loop for strapdown gyroscopes done at The University of Tennessee last year and presented in Scientific Report S-23,[2] a decision was made to develop the control logic of a width-modulated binary loop using CMOS (Complementary-Symmetry/Metal Oxide Semiconductor) integrated circuits. The CMOS devices were chosen because of their low power consumption and excellent noise immunity compared to the HS TTL logic now in use.

An analysis was performed on the existing HS control logic of a width-modulated binary rebalance electronics loop. Included in this analysis are equations which were derived for proper operation of the control logic.

The development of a new CMOS control logic for a width-modulated binary loop is presented in this thesis. Contained in the presentation are the necessary changes required to achieve the loop parameters of the new rebalance loop developed at The University of Tennessee in 1972-73.[3]

Another type of logic organization different from the Hamilton Standard System was proposed that would make scale factor selections by examination of the data train. The basic design goals of this new control logic were (1) to reduce the number of logic pieces required to implement the control logic for increased reliability and (2) to generate scale factor requirements by counting the number of data pulses present during an interrogation period.

A detailed analysis of the HS control logic is given in Chapter II. Chapter III presents design analysis and experimental evaluation of the new CMOS version of the HS control logic. Chapter IV contains information and experimental results on the attempts to develop another type of control logic section. Although no simpler design was achieved, some important results were obtained. These results and suggestions for further study are given in Chapter V.

CHAPTER II

GENERAL DESCRIPTION AND ANALYSIS OF THE CONTROL LOGIC FOR A WIDTH-MODULATED BINARY REBALANCE LOOP

A general description of the HS control logic for a width-modulated binary loop is presented in this chapter. General functions of the HS control logic in the rebalance loop will be described. The general design equations for the synthesis of a control logic for the rebalance loop will be derived. Finally, a complete analysis of the control logic function generator and the control logic scale factor selector of the HS realization for a width-modulated binary rebalance loop will be given.

I. General Functions of the HS Control Logic in the Rebalance Loop

A block diagram of the HS control logic section of the width-modulated binary rebalance electronics loop of a strapdown gyroscope is shown in Figure 1. The control logic can be divided into two sections: (1) the digital function generator (DFG), and (2) the scale factor selector (SFS).

A block diagram of the rebalance electronics is shown in Figure 2. The rebalance electronics senses the movement of the gyro float from its null position and then generates a duty-cycle controlled square wave of torque-current to restore the float to its null position. The control logic determines the error signal sampling frequency, level of torque-

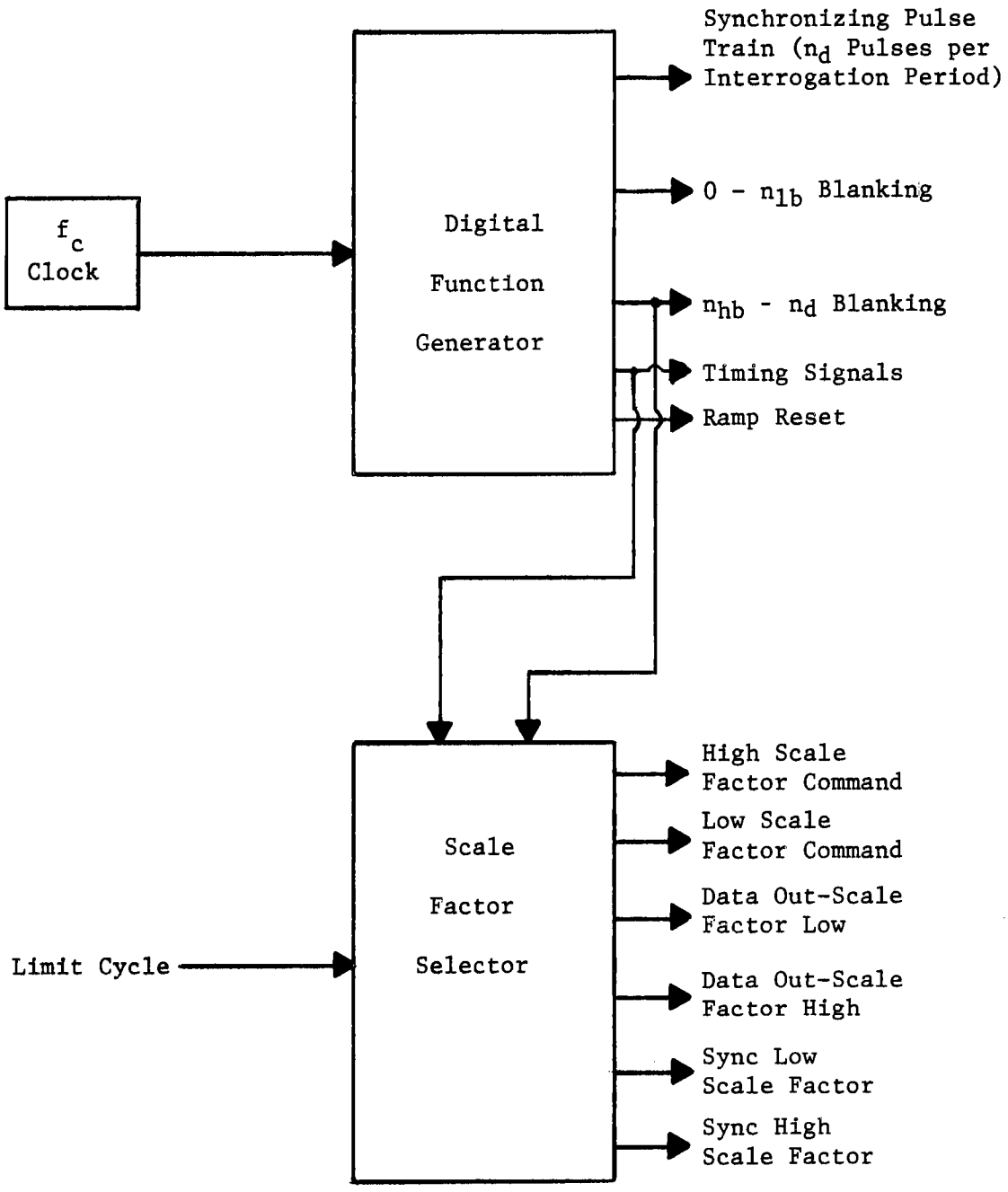


Figure 1. Hamilton Standard control logic for a width-modulated binary rebalance electronics loop.

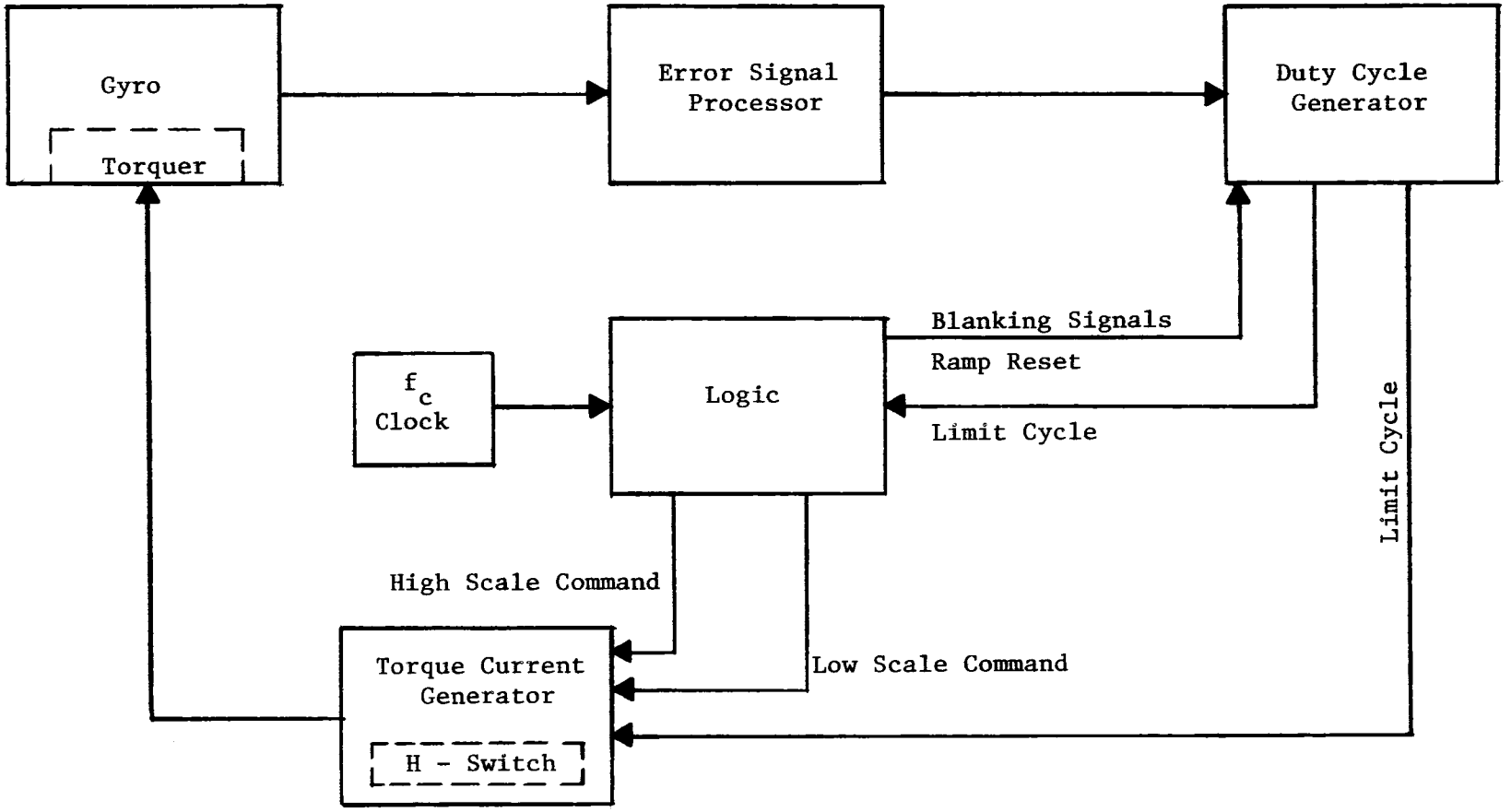


Figure 2. Rebalance electronics - block diagram.

current (torquing mode), and switches scale factor (changes torque-current level) when necessary. The control logic also generates a data pulse train which gives the amount of torque-current area (ampere-seconds) fed to the torquer (see Reference 2).

The signal, which comes from the error signal processor is mixed with a ramp signal in the duty cycle generator. The zero voltage crossing point of this composite signal determines how the total torque-current applied to the torquer will be apportioned between positive and negative values. The zero crossing is detected by a group of logic gates in the duty cycle generator. Detection of the zero crossing is indicated by a transition in a J-K flip-flop which feeds a forced limit-cycle signal to the control logic for torque mode determination and to the torque-current generator for torque-current determination.

An H-switch in the torque-current generator routes a precisely controlled current I to the torquer. Because of the bilateral nature of the H-switch, it allows current to be driven in both directions through the torquer so that the net movement of the gyro float axis for each torquing interval is proportional to the differences between the positive torque-current area and the negative torque-current area. Thus, a zero net torque requirement is fulfilled by equal positive and negative torque-current areas (see Reference 2).

The system scale factor is determined by the current level feeding the H-switch; therefore, by switching the current level with a scale-factor change command from the control logic to the torque-current regulator a scale factor change is executed. The design requirements for the current I were 150 mA in the high mode and 30 mA in the low mode. For a complete

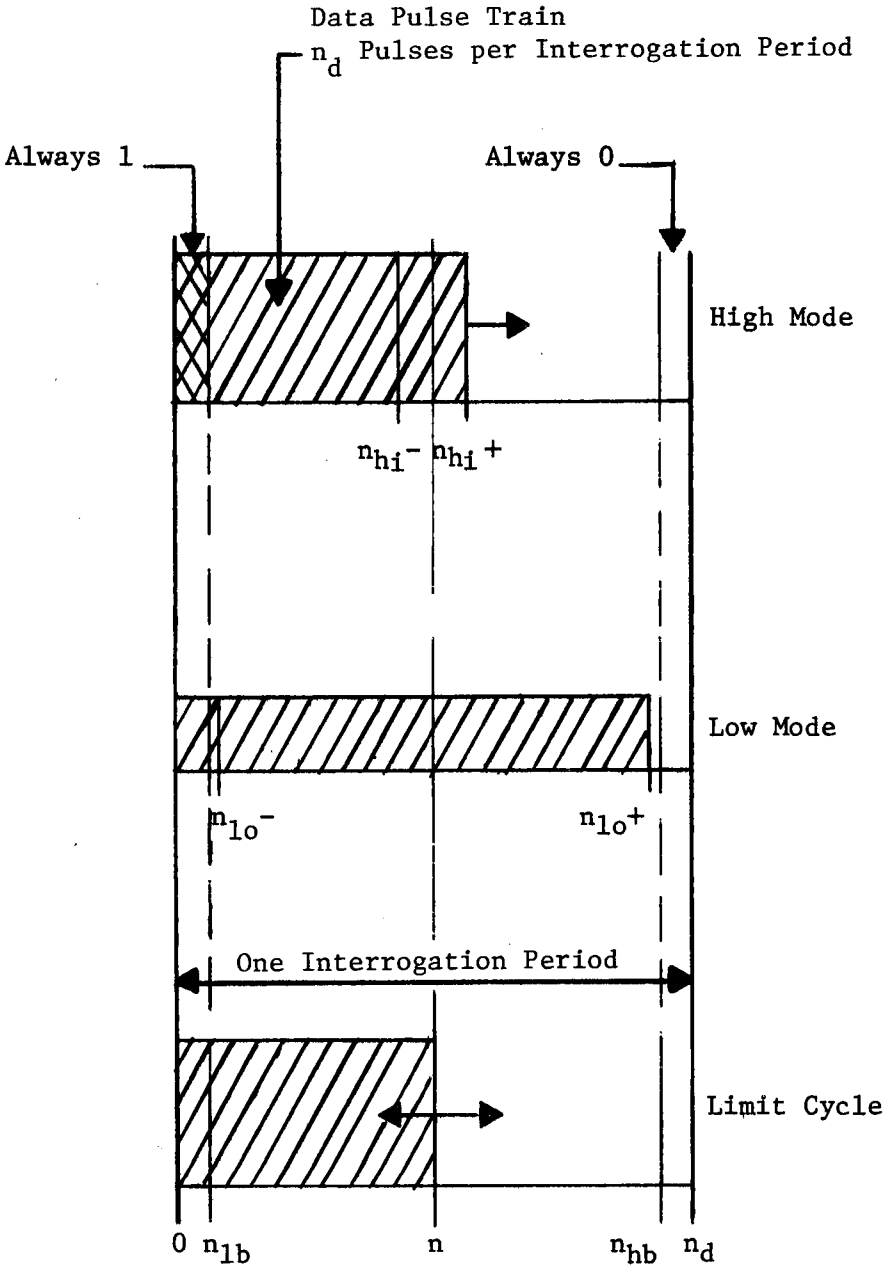


Figure 3. Timing diagram.

analysis of the rebalance electronics see the July 13, 1973, Scientific Report S-25.[3]

The DFG is fed by a clock of frequency f_c. The DFG generates (1) a $0\text{-}n_{lb}$ blanking signal, (2) a $n_{hb} - n_d$ blanking signal, (3) a data pulse train of frequency f_{c1}, (4) a ramp reset signal, which is the inversion of the $n_{hb} - n_d$ blanking signal, and (5) timing signals. The blanking signals assure that for any torquing condition both positive and negative torque will be applied for at least one blanking period (n_b/n_d) per interrogation period.

The SFS is fed by the limit-cycle from the duty-cycle generator, which contains n_d data pulses per interrogation period t_i. The SFS generates (1) a high scale factor command, (2) a low scale factor command, (3) a data out-scale factor low, (4) a data out-scale factor high, and (5) high and low mode sync pulses are transmitted out on two other lines to indicate the initiation of a data pulse train (a data train is produced for each t_i period).

In the SFS section, the limit-cycle is examined during each t_i period to ascertain in which torque mode (high or low) the rebalance loop should be operating. If the low mode is needed, the SFS will generate a low-scale factor command after sufficient delay T_{dhi}; the high-scale factor command should be generated after another delay T_{dlo}. Usually $T_{dlo} << T_{dhi}$.

The control logic of the system must be governed by the timing requirements indicated in Figure 3. The modes of operation are as follows: (1) If the system is in the high mode and n is greater than $n_{hi}-$, but less than $n_{hi}+$, then the system will go to the low mode after some

delay; (2) if the system is in the high mode and n is less than n_{hi}^- or greater than n_{hi}^+, then the system should stay in the high mode; (3) if the system is in the low mode and n is less than n_{lo}^- or greater than n_{lo}^+, the scale factor switches to high mode after some delay; and (4) if the system is in the low mode and n is between n_{lo}^- and n_{lo}^+, then the system should stay in the low mode.

II. Design Equations for Scale Factor Selection

To find the timing points n_{lo}^-, n_{hi}^-, n_{hi}^+, and n_{lo}^+ the following equations were derived by the use of Figure 3. The total number of synchronizing pulses (or data pulses) per interrogation period is defined as n_d. If the system is in the high mode and should go to the low mode, then choose

$$[(n_d/2) - (n_{hi}^-)] = [(n_d/2) + (n_{hi}^+)] ,$$

and

$$[(n_d/2) - (n_{lo}^-)] = [(n_d/2) + (n_{lo}^+)] .$$

Solving these two equations yields

$$n_{hi}^- = n_d - n_{hi}^+ , \tag{1}$$

and

$$n_{lo}^- = n_d - n_{lo}^+ . \tag{2}$$

Since the system scale factor is determined by the current level feeding the H-switch, a scale factor change is executed by switching the current level with a scale-factor change command from the control logic to the torque current regulator. To change scale factor from high to low, the area of the high torque-current anywhere in the range $n_{hi}^- < n < n_{hi}^+$

must be less than the maximum area of the low torque-current. If this were not the case, then for some gyro rates, the system could reach an unstable condition characterized by a continuous switching between high and low torque modes. For a complete analysis of the current level requirements of the H-switch see Reference 3.

From the conditions stated above and the use of Figure 3, page 8, the following equation can be written:

$$\alpha(n_{hi}+ - n_{hi}-) < (n_{lo}+ - n_{lo}-) \ , \tag{3}$$

where α = high current level/low current level. Substituting Equation 1 and Equation 2 into Equation 3 and solving yields

$$\alpha[n_{hi}+ - (-n_{hi}+ + n_d)] < [n_{lo}+ - (-n_{lo}+ + n_d)] \ ,$$

$$\alpha[2n_{hi}+ - n_d] < [2n_{lo}+ - n_d] \ ,$$

$$(n_{hi}+) < [(n_{lo}+ - n_d/2)/\alpha] + n_d/2 \ . \tag{4}$$

Solving Equation 4 for $n_{lo}+$ yields

$$[n_{hi}+ - n_d/2]\alpha < [n_{lo}+ - n_d/2] \ ,$$

$$(n_{lo}+) > \alpha[n_{hi}+ - n_d/2] + n_d/2 \ . \tag{5}$$

These equations will be used in Chapter III to find the timing marks.

III. Analysis of HS Control Logic Function Generator

Figure 4 shows the organization of the HS control logic function generator. The DFG generates the synchronizing signal of frequency f_{c1} by

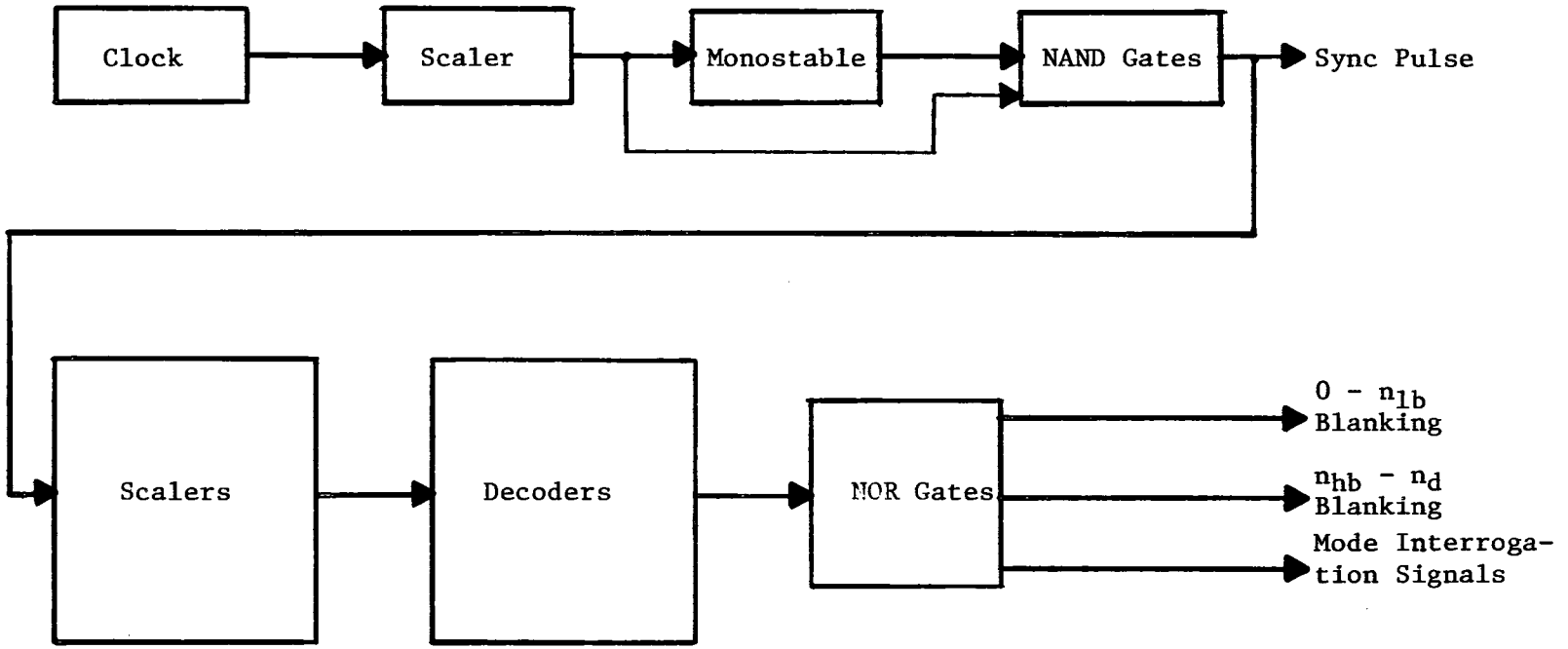


Figure 4. Organization of digital function generator.

feeding the system clock of frequency f_c into a scaler. By pulling off the correct output of the scaler, the synchronizing pulse train at frequency f_{c1} is obtained. This signal is used as the trigger on the monostable. Now by using the output pulse of the monostable, and the correct signals from the scaler as inputs to NAND gates, the sync pulse is obtained. The sync pulse train is fed to another group of scalers which will set up the inputs to the binary-to-decimal decoders which provide the o - n_{lb} blank, n_{hb} - n_d blank, and a set of gating signals. The gating signals, and the output signals from the first counter are fed into a set of positive NAND gates where the gating signals select certain of the first counter signals. These output signals are the mode interrogation signals $n_{lo}-$, $n_{lo}+$, $n_{hi}-$, and $n_{hi}+$. In the HS control logic the DFG also generates (1) a CRS signal, which either counts down the delay counter or resets the counter to zero, and (2) a PRS signal which sets the counter input gates to either count or not count. The mode-interrogation signals are shown in Figure 5 (see Reference 2, Figure 5-3), where PRS occurs at time t_1, $n_{lo}-$ occurs at time t_2, $n_{hi}-$ occurs at time t_3, $n_{hi}+$ occurs at time t_4, $n_{lo}+$ occurs at time t_5, and CRS occurs at time t_6.

IV. Analysis of HS Control Logic Scale Factor Selector

Figure 6 (see Reference 2, Figure 5-4) shows the organization of the HS control logic scale factor selector. The SFS can be divided into four basic sections. They are (1) the scale factor-set J-K flip-flop which is in the "one" state for low scale factor and the "zero" state for high scale factor, (2) a NAND gate group and J-K flip-flop that makes

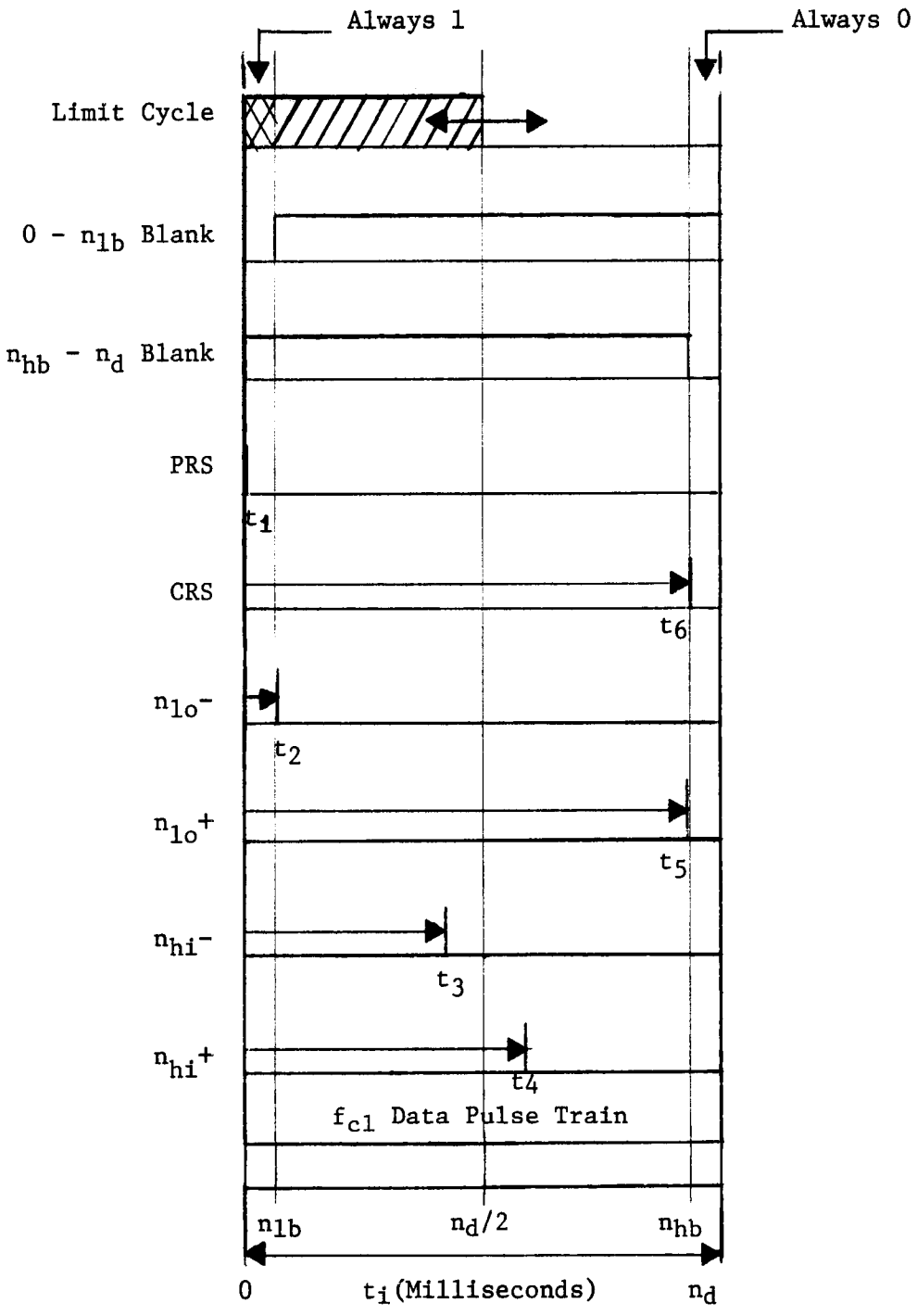


Figure 5. Signals generated by the digital function generator.

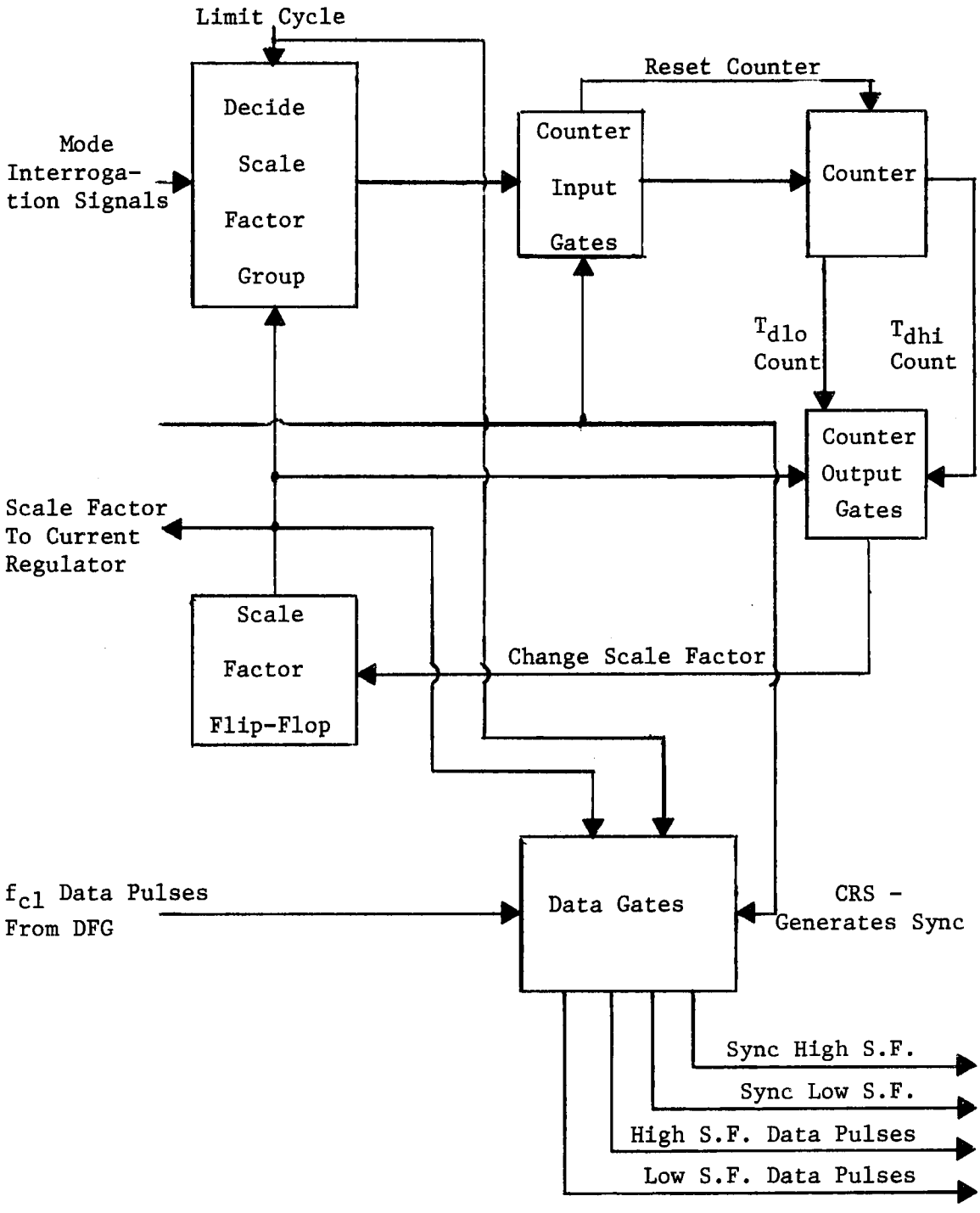


Figure 6. Organization of scale factor selector.

scale factor decisions, (3) a cascade of three 4-bit binary counters and associated NAND gates for providing delays T_{dhi} and T_{dlo} before a scale factor change command is transmitted, and (4) a NAND gate group for gating the data pulses and sync signals into the appropriate output lines.

Scale factor change requirements are decided in the following manner: The scale factor set signal (which tells the SFS which mode the system is in), the limit cycle, and the mode-interrogation signals are fed into the decide scale factor group. The signal from the decide scale factor group and the CRS signal is fed to the delay counter where the counters will either count down or not count according to the mode the system is in, and at what range the limit-cycle is at. This is decided in the following manner: (1) If the system is in the low mode and $n < t_3$ or $n > t_5$ the counter will be set to count. After T_{dlo} counts the scale factor set flip-flop will go to zero and high-scale factor will be demanded; (2) if the system is in the low mode and $t_2 < n < t_5$ the counter will only be reset by signal CRS during each interrogation period; (3) if the system is in the high mode and $n < t_3$ or $n > t_4$ the counter will be reset by signal CRS and no scale factor change will be demanded; and (4) if the system is in the high mode and $t_3 < n < t_4$ the counter will be counted down, after T_{dhi} counts the scale factor set flip-flop will go to the "one" state and low-scale factor will be demanded.

The sync high and sync low signals are generated by gating the correct output from the scale factor flip-flop, the CRS signal, and the sync pulse. The data low and high signals are generated by gating the correct output from the scale factor flip-flop, the sync pulse, and the limit-cycle.

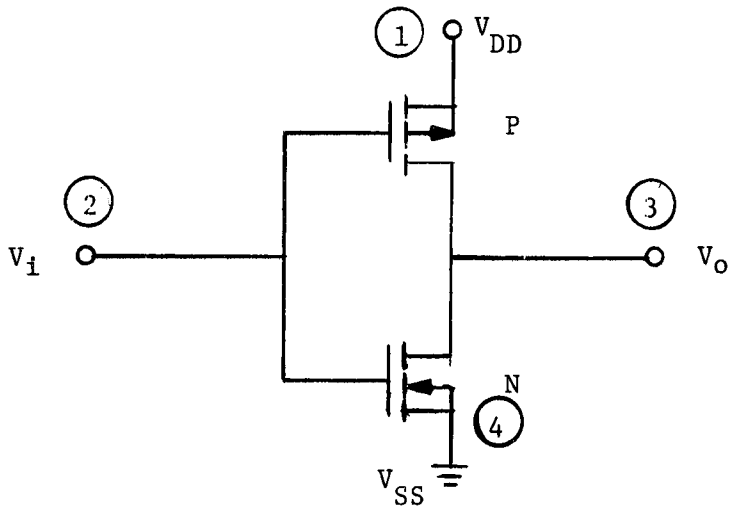
CHAPTER III

DEVELOPMENT OF THE NEW CMOS CONTROL LOGIC

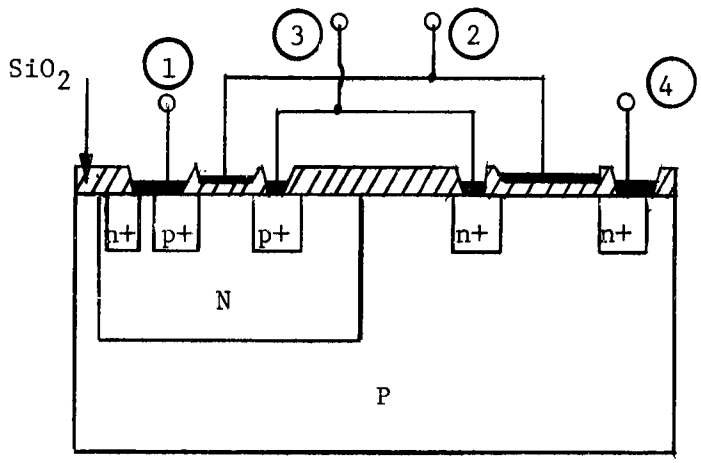
The CMOS devices were chosen for the development of the control logic because of their micro-power quiescent operation and their excellent noise immunity. In this chapter a brief discussion of the operation of CMOS devices is given. Calculations for the timing marks, that are used with the new CMOS logic, will be obtained by application of Equation 1 through Equation 5 which are derived in Chapter II. The selection of specific values for system parameters, together with the development of a new control logic section using RCA CMOS CD4000 series logic components and using the HS control logic organization will be presented in detail. Finally, experimental results of this new logic are presented.

I. Theory of Operation of CMOS Devices

Complementary metal oxide semiconductor technology employs both p-channel and n-channel devices on the same silicon substrate. Both types are enhancement-mode devices; that is, gate voltage must be increased in the direction that inverts the surface in order for the device to conduct. An enhancement-mode device is normally turned off. Figure 7A shows the basic complementary-pair inverter, and Figure 7B illustrates the basic construction of CMOS. It is seen that the n-channel and p-channel devices are connected in series. Only one device is turned on at a time, resulting in extremely low power dissipation. Dissipation



(A) Basic CMOS Inverter Circuit



(B) Cross Section of Inverter Circuit Chip

Figure 7. Basic CMOS construction.

is primarily from the switching of devices through the active region and the charging and discharging of capacitances. Due to the symmetry of the devices and MOS construction, either a positive or negative supply may be used. CMOS design allows operation from +3 volts to +15 volts on V_{DD}, with +10 volts nominal.[3] A complete analysis of the basic complementary-pair inverter is given in Appendix A.

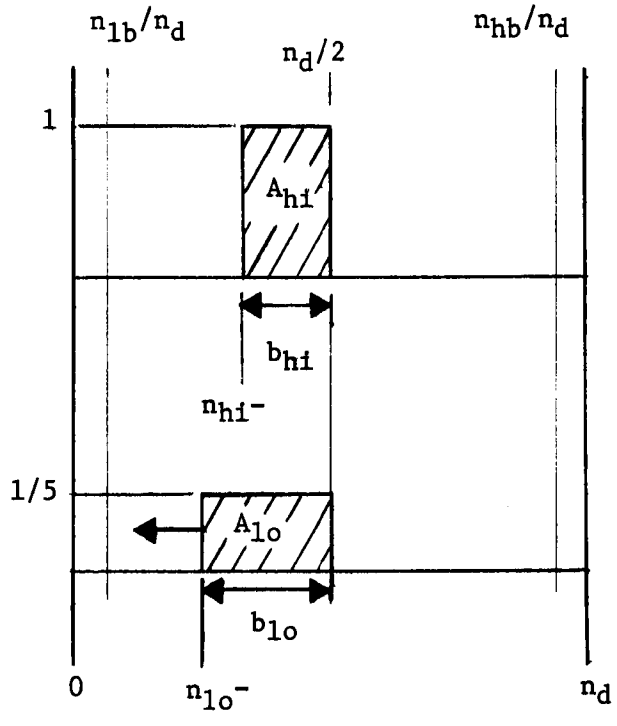
II. Calculations of Timing Marks

By applying the equations that are derived in Chapter II, the values for $n_{lo}-$, $n_{lo}+$, $n_{hi}-$, and $n_{hi}+$ are now derived for a torque-current ratio of 5 to 1. The high mode current is five times as large as the low mode current. Using this ratio, the previously derived equations and Figure 8, the following values are obtained for the maximum allowable range of operation. Figure 8 shows the condition that exists in obtaining the timing marks. Equation 3 states the condition for stable operation. This condition is that the area of the high torque-current (A_{hi}) must be less than the area of the low torque-current (A_{lo}). If this was not the case, then the system could become unstable for some gyro rates.

From Equation 3 and Figure 8:

$$A_{lo} > A_{hi} \text{ for stable operation}$$

If the system is in the high mode and should go to the low mode, then for the case of n_d = 256 data pulses per interrogation period and blanking periods of 16 data pulses as presented in Scientific Report S-23,[2]



Where: $A_{hi} \equiv$ Area Of High Torque Current

$A_{lo} \equiv$ Area Of Low Torque Current

Figure 8. Condition existing for deriving timing marks.

$$A_{lo} \text{ max} = (1/5)\ (128-16) = 22.4\ ,$$

$$A_{hi} \text{ max} = (1)\ (b_{hi})\ ,$$

and

$$b_{hi} < 22.4\ ,$$

where b_{hi} is the maximum base length of the high mode current area. Since

$$A_{hi} = (b_{hi})\ (1)\ ,$$

then

$$A_{hi} \leq 22.4\ .$$

Because only whole numbers are obtainable, 22 is chosen for A_{hi}. This value is permissible since any value less than 22.4 will satisfy the condition $A_{lo} > A_{hi}$.

Using 22 for A_{hi} will then yield

$$b_{hi} = 22\ ;$$

therefore,

$$n_{hi}- = 106 \text{ data pulses.}$$

$n_{hi}+$ can now be found from Equation 1,

$$n_{hi}+ = -n_{hi}- + 256$$

solving

$$n_{hi}+ = 150 \text{ pulses}\ .$$

From Equation 5:

$$n_{lo}+ > 128 + \alpha[n_{hi}+ - 128]$$

where

$$\alpha = 5$$

$$n_{lo}+ > 238.$$

From Equation 2:

$$n_{lo}- = 256 - n_{lo}+$$

$$n_{lo}- = 17 \text{ pulses} ,$$

where $n_{lo}+$ was chosen to be 239 pulses.

As a check to prove the validity of the timing points derived above, use the condition:

$$A_{lo} > A_{hi}$$

where

$$A_{lo} \text{ max} = (1/5)\ (128 - 17)$$

$$A_{lo} \text{ max} = 22.2 .$$

Since this value is greater than 22, it is valid to use a value of 112 for b_{lo} in deriving the timing points, where b_{lo} is the maximum base length of the low mode current area.

III. System Parameters

The system clock (f_c) was set to be 2.466 MHz and scaled down to a 616 kHz (f_{cl}) pulse train to be used for both data generation and synchronization of logic functions. These values were selected for proper operation of the rebalance electronics loop. A design goal for the University of Tennessee rebalance electronics loop was to double the sample

rate of 1 kHz (halve the interrogation period) of the width-modulated binary loop available at the initiation of the development work. A rate of 2.4 kHz was chosen to agree as an even multiple of 2.466 MHz. Each interrogation period t_i was divided into 256 increments.[3]

As stated earlier, the maximum torque-current was to be approximately 150 mA and the minimum torque-current was to be 30 mA, which gave a scale factor ratio of 5 to 1 which means α is equal to 5.

Because the blanking signal inputs to the duty cycle generator come from the logic, which sets lower bounds to the duration of positive and negative torque currents, the blanking signals were chosen to be 0-16 and 241-256 to assure that for any torquing condition, both positive and negative torque will be applied for at least 16/256 t_i msec. Since the blanking signals are sent to the duty cycle generator, they limit the range of the limit-cycle. The time to the edge of the limit-cycle is always at least 1/16 t_i msec, but never more than 15/16 t_i msec. This assures that the leading and falling edges of the torque pulses are never disturbed by the limit-cycle.

It was desired to have the delay associated with the high mode to occur very quickly; however, low mode was not to be set until after considerable delay. For this reason, if the high mode is needed, the SFS will generate a high scale factor command after 4 high torque-current pulses. The low scale factor command will be generated after 2048 low torque-current pulses.

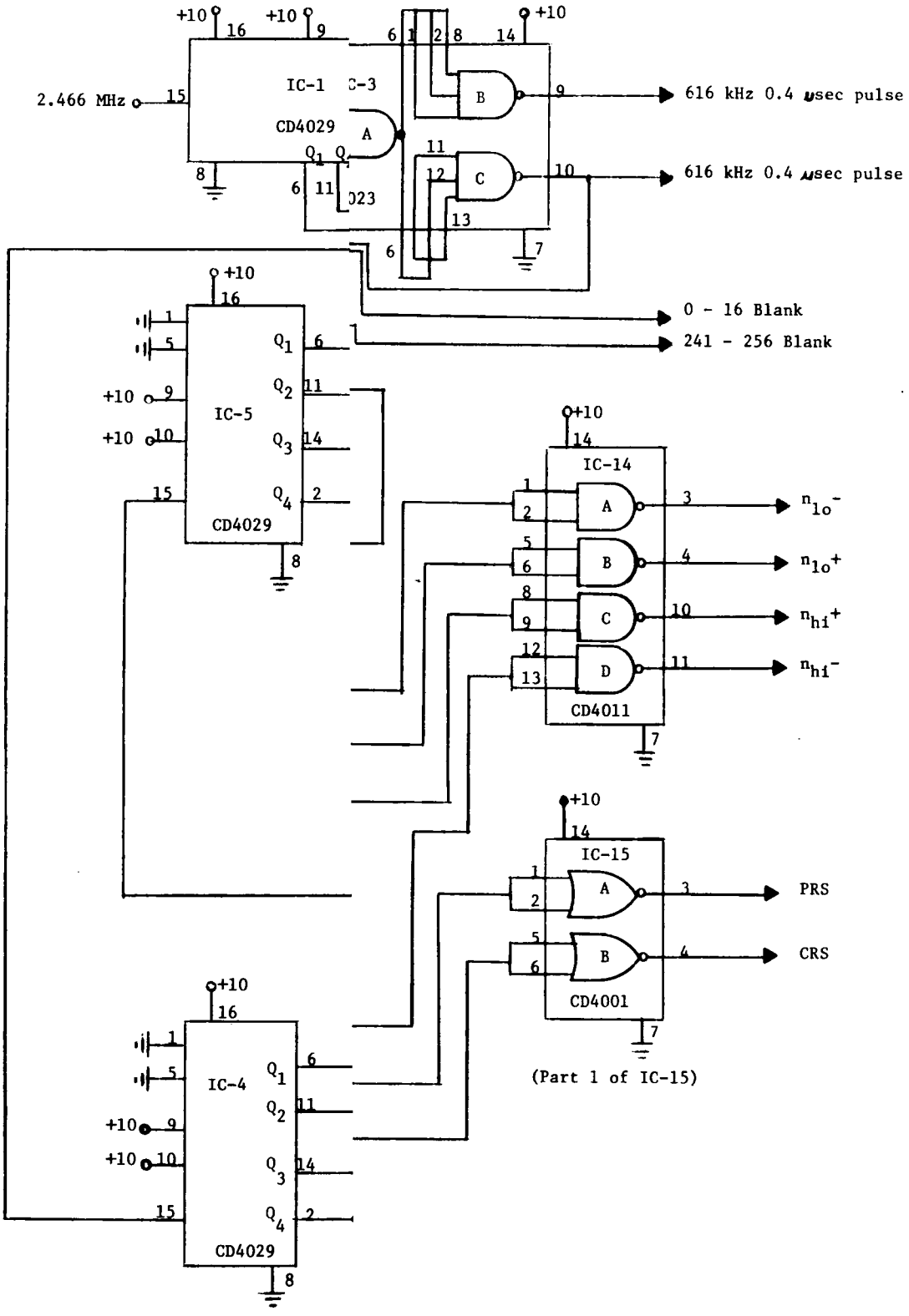
A complete analysis of these parameters is given in the Scientific Report S-23 (see Reference 2) and the July 13, 1973 Scientific Report S-25 (see Reference 3).

IV. Development of Logic Implementation

A detail design of the DFG using CMOS logic components is given in Figure 9. RCA CD4000 series CMOS logic components were used for the implementation. The function of the DFG is to produce the following signals: (1) a 616 kHz, 0.4 μsec wide pulse; (2) the 0-16 blanking pulse; (3) the 241-256 blanking pulse; (4) the ramp reset pulse; and (5) the six mode-interrogation signals.

The DFG operates in the following manner: To satisfy the requirement of generating a 616 kHz 0.4 μsec wide pulse, the 2.466 MHz clock signal is fed to the clock input of a 4-bit binary counter (CD4029 A). This counter is used because the 616 kHz pulse can easily be obtained from the output pin Q_2, which is the scale down of the frequency by a scale factor of four. The output Q_1 of the counter scales down the 2.466 MHz clock signal to 1.233 MHz. To obtain the 616 kHz 0.4 μsec wide pulse, it is necessary to use the Q_1 and Q_2 outputs of the counter as inputs to a NAND gate. Because a NAND gate produces a "high" output when any input is "low," the 616 kHz 0.4 μsec wide pulse is obtained in inverted form. It is necessary to invert this pulse and the inversion was accomplished by tying the inputs of a NAND gate together and using the inverted 616 kHz 0.4 μsec wide pulse as the input.

The HS logic includes a monostable with its output also used as an input to the NAND gate along with the Q_1 and Q_2 outputs of the counter. Because it is not necessary to use a monostable to produce the required sync pulse, it was not included in the new CMOS design. The purpose of this monostable is to change the width of the 616 kHz 0.4 μsec wide pulse. An analysis of a CMOS monostable is presented in Appendix B.


+10
+10
16
9
6
1
2
8
14
+10
2.466 MHz
15
IC-1
C-3
CD4029
A
B
C
616 kHz 0.4 μsec pulse
616 kHz 0.4 μsec pulse
11
12
10
13
6
11
023
8
7
0 - 16 Blank
241 - 256 Blank
IC-5
CD4029
IC-14
CD4011
A
B
C
D
n_{lo}^-
n_{lo}^+
n_{hi}^+
n_{hi}^-
IC-15
CD4001
PRS
CRS
IC-4
(Part 1 of IC-15)

This analysis is presented for completeness so that the pulse width could be adjusted if necessary. Figure 10A shows the waveforms of the 616 kHz 0.4 μsec wide pulse and Figure 10B shows the effect of adjusting the output of the monostable on this pulse.

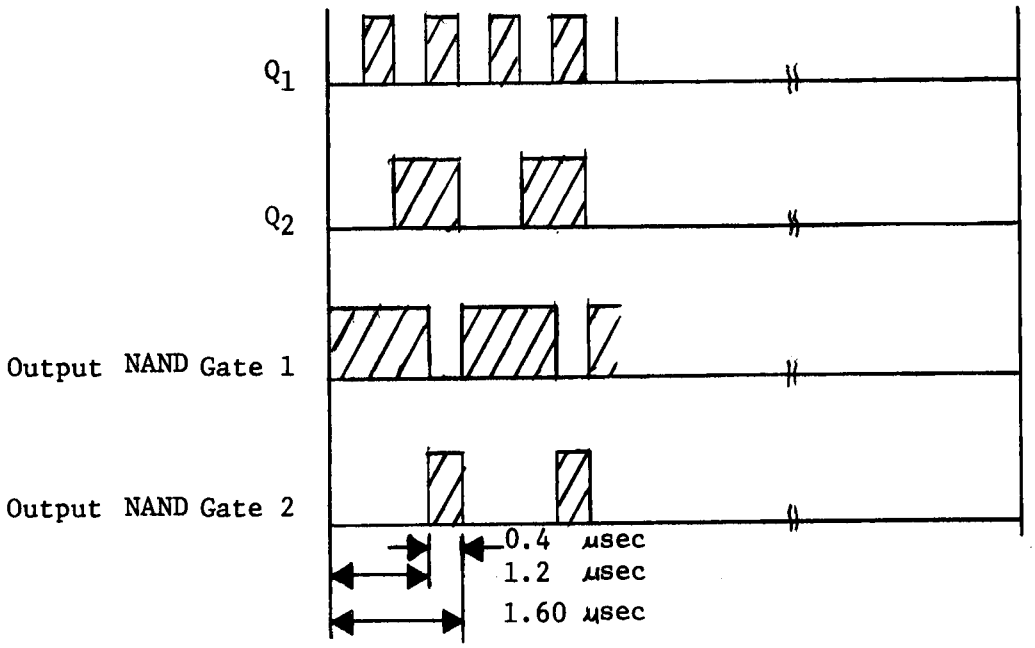
The 616 kHz 0.4 μsec wide pulse is used as the clock input to a two stage 4-bit binary counter. This is necessary to produce the correct input to the decoders. The output signals of the first stage are: (1) Q_1, 308 kHz; (2) Q_2, 154 kHz; (3) Q_3, 77 kHz; and (4) Q_4, 38.5 kHz.

The output signals obtained from the second stage are: (1) Q_1, 19.25 kHz; (2) Q_2, 9.625 kHz; (3) Q_3, 4.813 kHz; and (4) Q_4, 2.401 kHz.

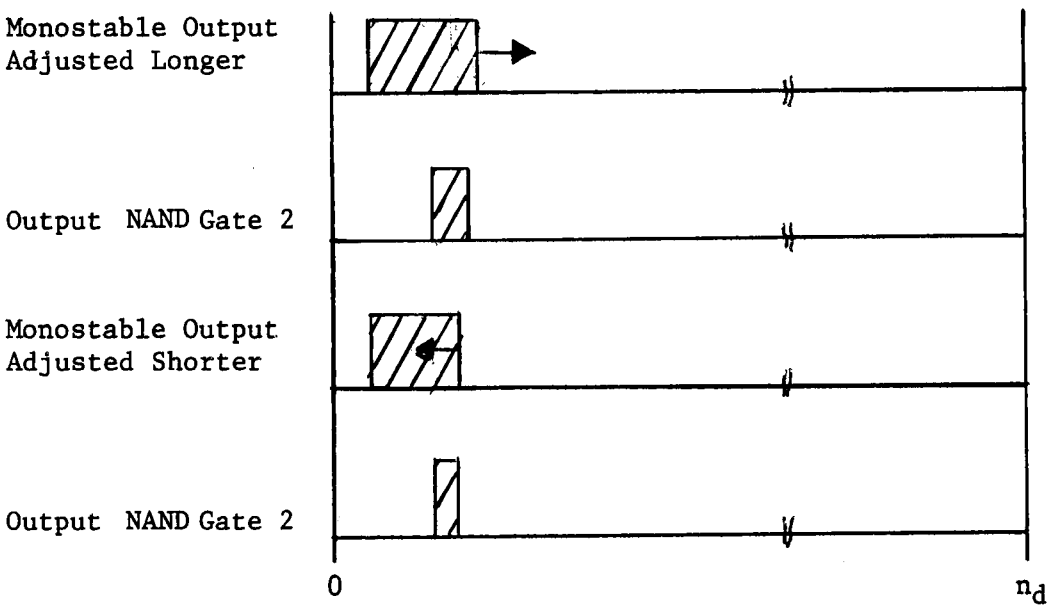
The outputs of the two stage counter along with the inversion of Q_4 from both stages are used as the inputs to a set of four 4-line-to-10-line BCD-to-Decimal Decoders (CD4028 A). When a BCD code is applied to the four inputs of a decoder, a "high" level appears at the selected one of the 10 decimal decoded outputs.

Two decoders are fed by the outputs of the first stage of the two stage counter. The outputs of these decoders produce a pulse that is at a "high" level for one-sixteenth of every sixteen pulse period. Two more decoders are then fed by the outputs of the second stage of the two stage counter. The outputs of these decoders produce a pulse that is at a "high" level for an entire sixteen pulse period.

To obtain the six mode-interrogation signals it is necessary to apply the AND operation to the proper outputs of the decoders. Since no AND gates are available in the RCA CD4000 series, the AND operation is completed here by performing the NAND operation followed by an inversion. The 241-256 and 0-16 blanking pulses are generated by the inversion of



(A) Waveforms Generating the 616 kHz 0.4 μsec Pulse



(B) Waveforms of the 616 kHz 0.4 μsec Wide Pulse with the Effect of Adjusting the Monostable

Figure 10. 616 kHz 0.4 μsec wide pulse waveforms.

the proper decoded outputs. The six mode-interrogation signals, the 241-256 blanking signal, and the 0-16 blanking signal are shown in Figure 11.

The SFS logic developed using RCA CD4000 series CMOS logic components is shown in Figure 12. A NAND gate group examines the signals $n_{lo}-$, $n_{lo}+$, $n_{hi}-$, $n_{hi}+$, PRS, the limit-cycle, and the mode of operation the system is in (high or low) during each interrogation period. Scale factor change requirements were presented in Chapter II, but will be repeated here for the convenience of the reader. The interrogation signals $n_{lo}-$ and $n_{lo}+$ determine the low mode range, the signals $n_{hi}-$ and $n_{hi}+$ determine the high mode range, the signal PRS sets the counter input gates to either count or not count, and the signal CRS either counts down the counter or resets the counter to zero. If the system is in the low mode and the limit-cycle n is less than $n_{lo}-$ or greater than $n_{lo}+$, the delay counter will be set to count. After four counts the scale factor set flip-flop will go to zero and high-scale factor will be demanded. If the system is in the low mode and $n_{lo}- < n < n_{lo}+$, the counter will only be reset by the CRS signal during each interrogation period. If the system is in the high mode, and $n < n_{hi}-$ or $n > n_{hi}+$, the counter will be reset by signal CRS and no scale factor change will be demanded. If the system is in the high mode, and $n_{hi}- < n < n_{hi}+$, the delay counters will be counted down. After 2048 counts the scale factor set flip-flop will go to the "one" state and low-scale factor will be demanded.

A complete analysis with waveforms will be given for when $n < n_{lo}-$ and the system is operating in the low mode. The following assignments

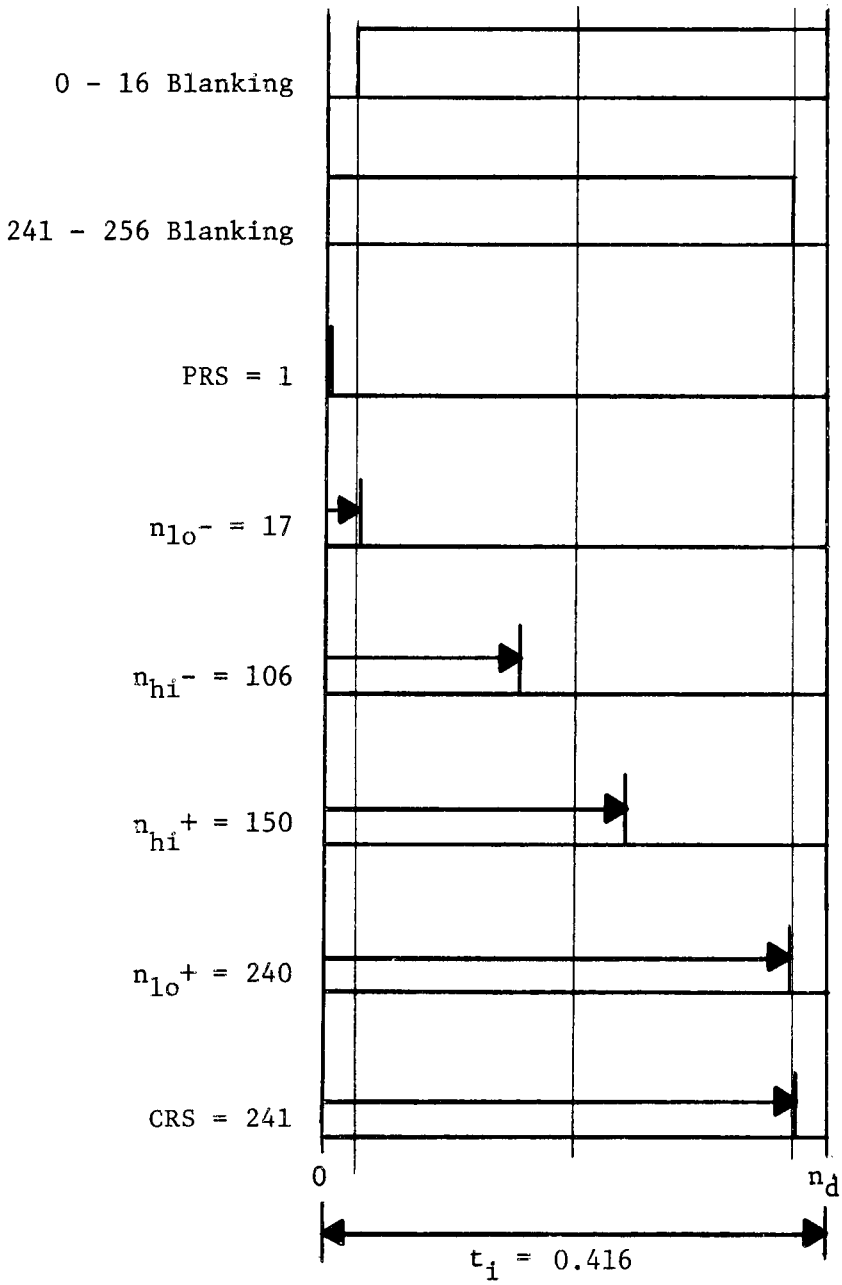
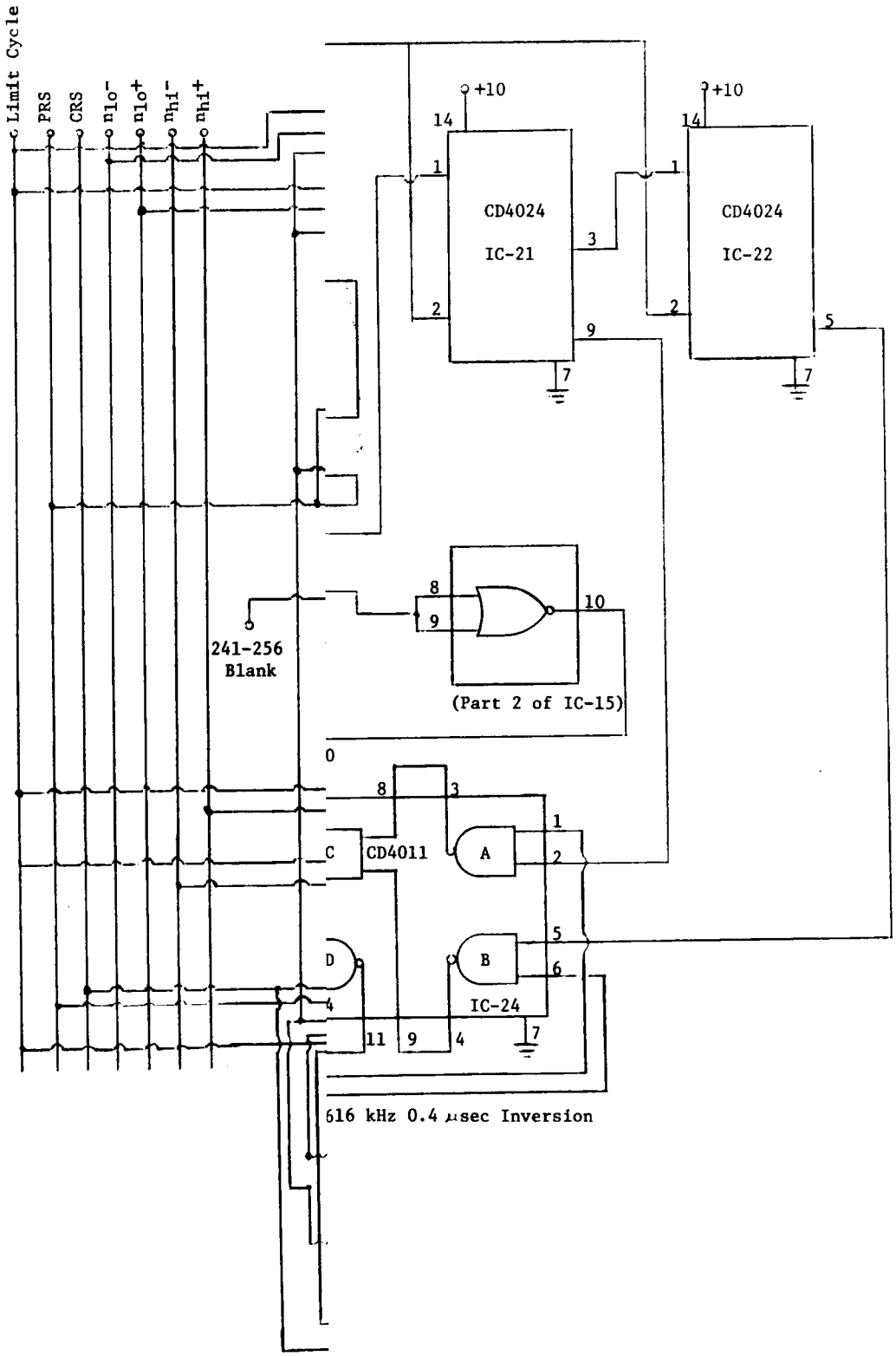


Figure 11. Signals generated by the digital function generator using CMOS logic.


Limit Cycle
PRS
CRS
n_{lo}^-
n_{lo}^+
n_{hi}^-
n_{hi}^+
+10
14
1
2
3
9
7
CD4024
IC-21
CD4024
IC-22
5
8
9
10
241-256
Blank
(Part 2 of IC-15)
0
C
CD4011
A
D
B
IC-24
4
11
616 kHz 0.4 μsec Inversion

are made to reduce confusion during the analysis: (1) the PRS signal is defined as time t_1, (2) the n_{lo}- signal is defined as time t_2, (3) the n_{hi}- signal is defined as time t_3, (4) the n_{hi}+ signal is defined as time t_4, (5) the n_{lo}+ signal is defined as time t_5, and (6) the CRS signal is defined as the time t_6.

Referring to Figure 12, the signals n_{lo}-, Q of the scale factor flip-flop, and the limit-cycle are fed to the input of NAND gate A of IC-16. Since the signal n_{lo}- is "low" for the complete interrogation period, the output of this NAND gate is "high." The signals n_{lo}+, Q of the scale factor flip-flop, and the limit-cycle are fed to the input of NAND gate B of IC-16 which produces a "high" output. The PRS signal and $\overline{Q}$ output of the scale factor flip-flop are used as the inputs to NAND gate A of IC-17 which produces a "high" output for this mode of operation. NAND gate B of IC-17 is fed by the PRS signal and Q of the scale factor flip-flop to obtain a "low" output at time t_2. Similar analysis of IC-18 will show that a "high" at time t_1 is present at the output of NAND gate C. NAND gate C of IC-16 produces a "low" output. The output of IC-16 and IC-18 are used as the K and J inputs respectively to a J-K flip-flop.

The Q output of the flip-flop is fed to an AND gate with the CRS signal which produces an output that is "high" at t_6. Since for this mode of operation it is required for the system to command a scale factor change, the delay counters must be fed a count command signal. The "high" signal at time t_6 serves this purpose and is used as the clock input to the two stage 7-bit binary counter (CD4024 A). The $\overline{Q}_1$ flip-flop output of IC-19 is fed together with the CRS signal to an AND operation, which produces a "low" output. This "low" signal is used as the reset signal to

both stages of the 7-bit binary counters. Since the clock signal to the first counter is not zero and the reset signal is zero, the counters will begin to count. After four counts, output Q_3 of the first 7-stage counter will go "high." This output is fed to the input of a NAND gate along with the Q_2 output of IC-19. Until the counter reaches a count of four, the output of this NAND gate will be "low." The Q_5 output of the second delay counter will be "low" until a count of 2048 is reached. The 2048 count output is fed to an input with the $\overline{Q}_2$ of IC-19 to a NAND gate. This NAND gate will produce a "low" output until a count of 2048 is reached.

The outputs of these two NAND gates serve as inputs to another NAND gate, which produces a "high" output until the count of four is reached. At that time it goes "low." This "low" signal serves two purposes: (1) It is used as the J-K inputs to flip-flop two of IC-19, and (2) it is fed to the input of a NAND gate with the CRS signal. The output of this gate, because the flip-flop resets Q to a zero when reset goes "high," is inverted and is used as the reset signal on flip-flop one of IC-19. Until the delay counters reach the count of four the clock signal will remain present at the input of the delay counter for this mode of operation. Once the count of four is reached the reset on flip-flop one of IC-19 is reset to zero which will produce a "low" at the input to the delay counters and a "high" on the reset of the delay counters. This reset signal now resets the delay counters to zero. The output of gate C of IC-24 will go "high" when the count of four appears at the input to gate A. This high output causes flip-flop two of IC-19 to switch states; thus putting a zero at the J input and a one at the K input to the set scale factor flip-flop. This input to the scale factor flip-flop causes the output Q to go "low" and a scale factor change has been

commanded. Waveforms of this analysis are given in Figure 13. A similar analysis for the other mode of operations can be made and are summarized in Table 1.

The mode control low command was obtained by the inversion of the Q output of the scale factor flip-flop. Mode control high command was generated by the inversion of the $\overline{Q}$ output of the scale factor flip-flop. These signals could be obtained directly from the scale factor flip-flop, but the HS logic uses the gating technique, so it is assumed that these gates are needed for proper operation of the total rebalance loop. The data low output is obtained by performing the NAND operation of the limit cycle, the 616 kHz 0.4 μsec wide pulse, and the Q_2 output of IC-19. The data high output pulse is obtained by feeding the limit cycle, the 616 kHz 0.4 μsec wide pulse, and the $\overline{Q}_2$ output of IC-19 to a NAND gate. The high and low mode sync pulses are transmitted by performing the NAND operation of the CRS signal, the 616 kHz 0.4 μsec wide pulse, and the proper output of flip-flop two of IC-19. The sync pulses are generated to indicate the initiation of a data pulse train. The ramp reset signal is generated by the inversion of the 241-256 blanking signal. These output signals are given in Figure 14 for the low mode of operation and $n < n_{lo}$-. For other modes of operation the waveforms are similar.

V. Laboratory Testing

The circuit was constructed using RCA CD4000 14 and 16 pin lead dual-in-line plastic CMOS integrated circuits. The results that will be presented in this section have been experimentally verified on the breadboard constructed in the laboratory. The scale factor switching was

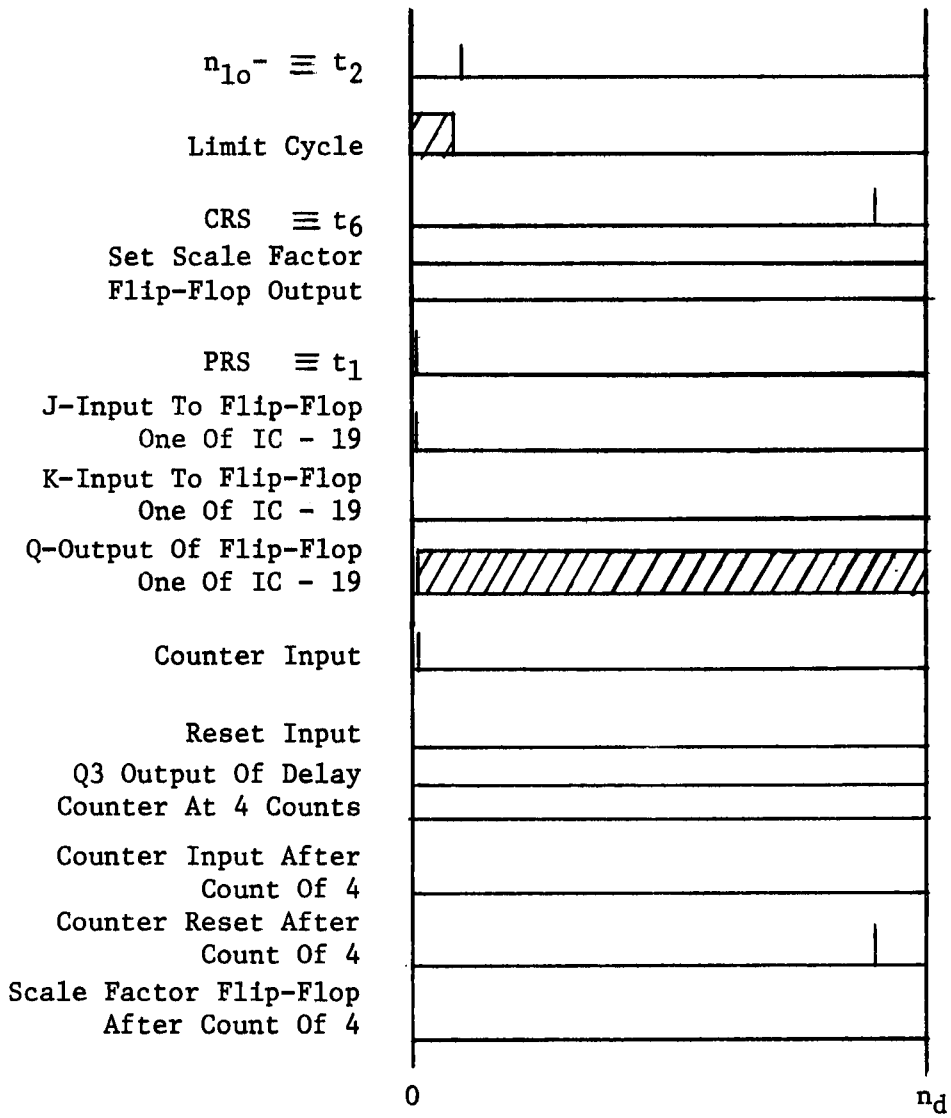


Figure 13. Waveforms for SFS logic when system is in low mode and $n < n_{lo}^-$.

Table 1. Summary of Modes of Operation

Mode	Limit Cycle	n_{lo}^-	n_{lo}^+	n_{hi}^-	n_{hi}^+	Flip-Flop One of IC-19 Inputs J	Flip-Flop One of IC-19 Inputs K	Flip-Flop One of IC-19 Outputs Q	Flip-Flop One of IC-19 Outputs $\overline{Q}$	Delay Scaler Input	Delay Scaler Reset	Scale Factor Flip-Flop at End of Period (t_i) Q	Scale Factor Flip-Flop at End of Period (t_i) $\overline{Q}$
Low	$n<n_{lo}^-$	0	0	0	0	$1@t_1$	0	$1@t_1$-t_6	$1@t_0$-t_1	$1@t_6$	0	0	1
	$n>n_{lo}^+$	1	1	1	1	$1@t_1$,t_5	$1@t_2$	$1@t_1$,t_5,t_6	$1@t_0$-t_1, t_2-t_4	$1@t_6$	0	0	1
	$n_{lo}^-<n<n_{lo}^+$	1	0	X	X	$1@t_1$	$1@t_2$	$1@t_1$	$1@t_0$-t_1, t_2-t_6	0	$1@t_6$	1	0
High	$n<n_{hi}^-$	X	0	0	0	0	$1@t_1$	0	$1@t_0$-t_6	0	$1@t_6$	0	1
	$n>n_{hi}^+$	1	X	1	1	$1@t_3$	$1@t_1$,t_4	$1@t_3$	$1@t_0$-t_3, t_4-t_6	0	$1@t_6$	0	1
	$n_{hi}^-<n<n_{hi}^+$	1	0	1	0	$1@t_3$	$1@t_1$	$1@t_0$-t_1, t_3-t_6	$1@t_1$-t_2	$1@t_6$	0	1	0

where: 1 represents a "high"
0 represents a "low"
X represents either a "low" or "high"

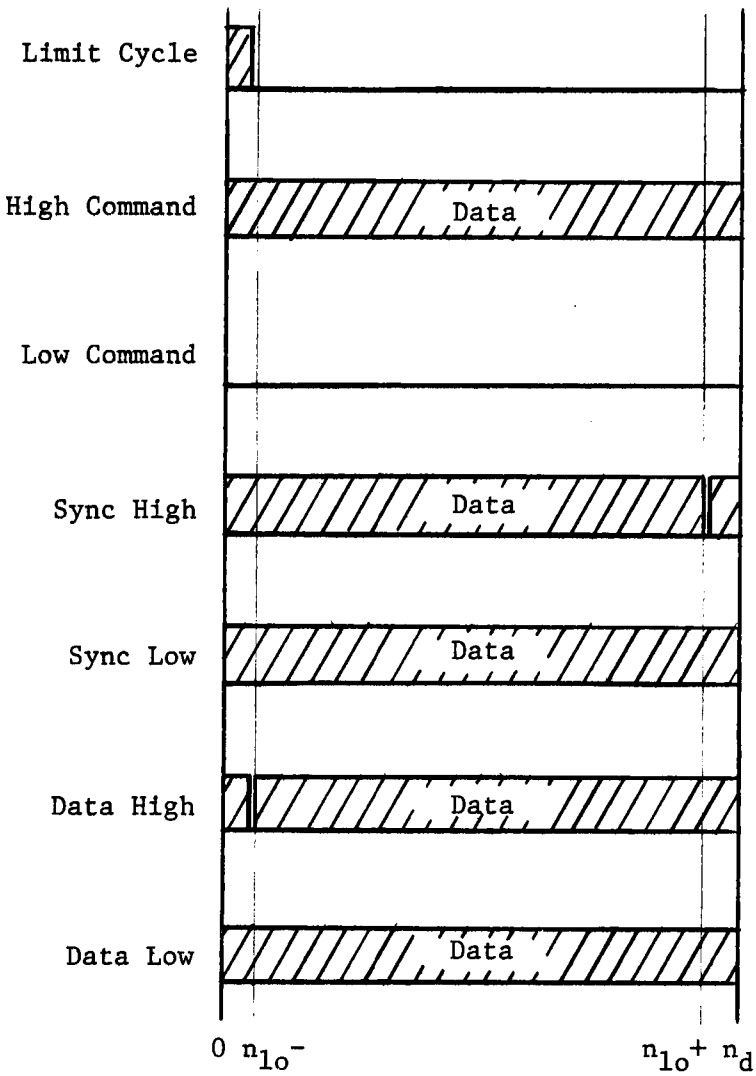


Figure 14. Signals generated by the SFS logic.

experimentally checked by feeding the logic with a variable-width limit-cycle generator which used the 0-16 blanking signal for synchronization. The limit-cycle used was constructed using TTL logic, therefore, a voltage divider was used to scale the 0-16 blanking signal down to +5 volts, and an interfaced circuit was required to bring the voltage level of the limit-cycle back up to +10 volts. All unused inputs were connected to either V_{SS} or V_{DD}, whichever was appropriate for the logic circuit involved.

A supply voltage of +10 volts was used. When the supply voltage was varied from +10 volts by an amount of ±1 volt, the only effect introduced on the waveforms was a change in the voltage level by an amount of ±1 volt.

The system clock frequency was operated at 2.466 MHz. The measured value of the sync frequency was 616.688 kHz. For proper operation, the maximum values of rise and fall times given under the Dynamic Electrical Characteristics in the data sheets were not exceeded. The 10-90% rise and fall times of the clock were measured at 30 nanoseconds. The 10-90% rise and fall times for the mode-interrogation signals were measured to be 20 and 10 nanoseconds respectively.

The current requirement of the new CMOS logic system was measured to be 20.7 mA in the low mode and 21.2 mA in the high mode. Thus, the power dissipation is 207 mw in the low mode and 212 mw in the high mode.

CHAPTER IV

SCALE FACTOR SELECTION BY EXAMINATION OF THE DATA TRAIN

In this chapter a control logic design philosophy different from that of the HS logic will be discussed. The design goals were (1) to satisfy the function of the control logic as set forth in Chapter II, and (2) to use fewer logic components to obtain a reliability greater than that of the HS system. In the technique presented here, a basic problem existed. This was the problem of generating the timing marks without using 16 more logic pieces than the HS organization. Attempts to implement this new control logic failed for reasons delineated in this chapter.

The basic difference between the design presented here and the HS design is that the HS design produced the pulse timing marks and compared these marks with the limit-cycle to determine mode requirements, while the design presented in this chapter processed the data train to obtain mode needs.

The function of the DFG is reduced, due to the fact that the timing marks are going to be determined by counting the data pulses and therefore need not be generated in the DFG. The function of the DFG is now to produce the 616 kHz 0.4 μsec sync and data signal, the 0-16 blanking signal, and the 241-256 blanking signal.

Figure 15 shows the block diagram of the new DFG. The DFG operates in the following manner: The 2.466 MHz clock is fed to a 4-bit binary counter and by selection of the divide by four output, the 616 kHz sync and data pulse is obtained. The 616 kHz output, along with

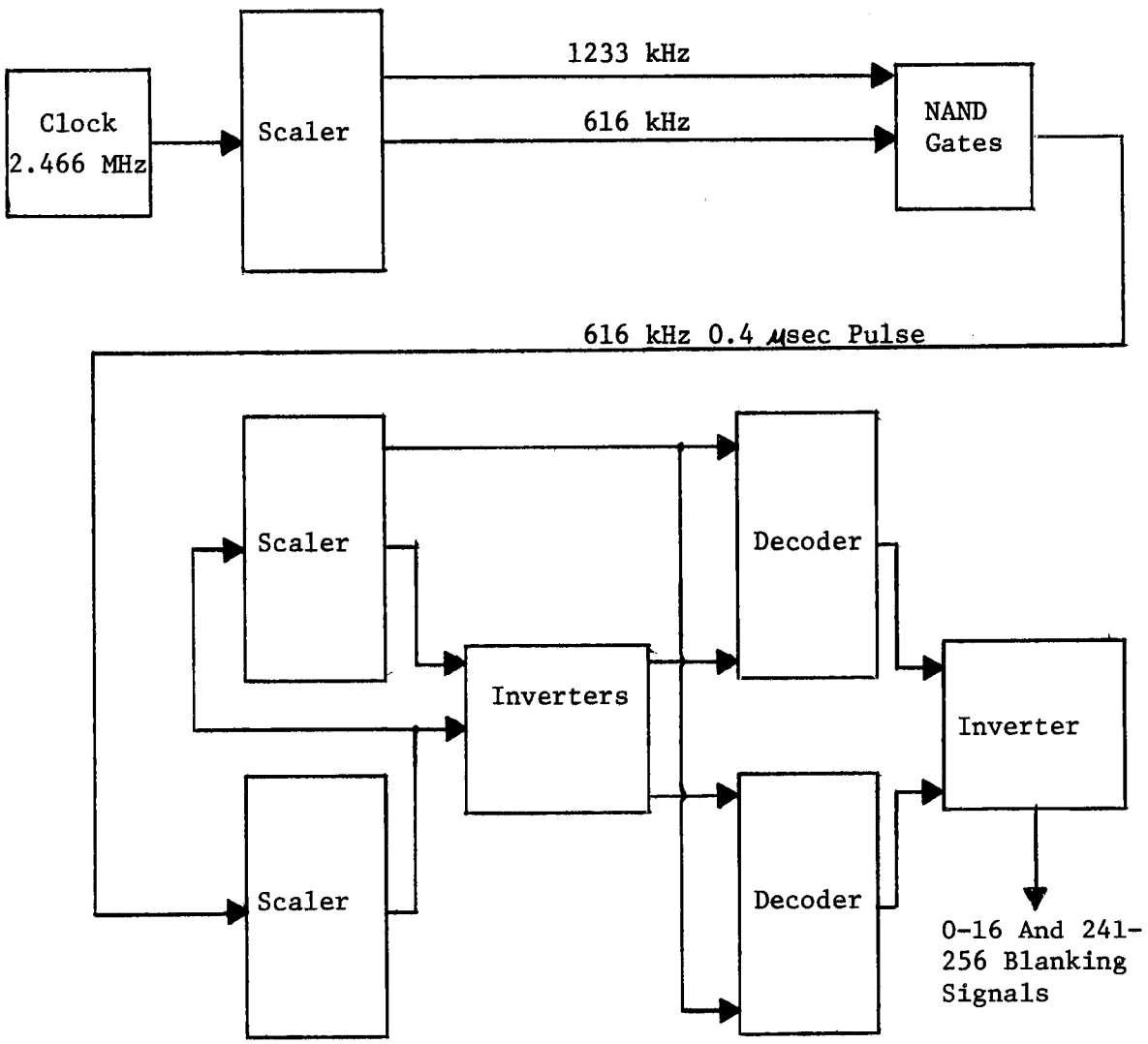


Figure 15. Proposed functional block diagram of new DFG.

the 1.233 MHz output of the counter, are used as inputs to a NAND gate. The NAND gate is followed by an inversion, which produces the 616 kHz 0.4 μsec wide pulse. The 616 kHz 0.4 μsec wide pulse is fed as the clock input to a two-stage 4-bit binary counter. The output of these counters are then connected as the inputs to 4-line-to-10-line BCD-to-Decimal Decoders. The outputs of the decoders produce a high output for a sixteen pulse period. The inversion of the proper output of the decoders produces the 0-16 and 241-256 blanking signals.

Keeping in mind the system must satisfy the requirements presented in Chapter II, the SFS logic section must be capable of generating the timing marks that are necessary for the system to control scale factor properly. The SFS logic for the new design performs the function of counting the data pulses. The basic technique proposed is shown in Figure 16 for a 5 to 1 scale factor range. The limit-cycle and the 616 kHz 0.4 μsec wide pulse are fed to an AND gate, which will produce an output with a designated number of data pulses according to the width of the limit-cycle. This is shown in Figure 17. The output of the AND gate is used as the input to a two-stage binary counter. Two stages are required in order to reach the maximum number represented by $n_{lo}+ = 240$. The timing pulses $n_{lo}-$, $n_{hi}-$, $n_{hi}+$, and $n_{lo}+$ are obtained by feeding the correct counter outputs to an AND gate. The counter output for a particular case is shown in Figure 17. To obtain a count in this manner is a trivial problem. Table 2 shows the procedure used to obtain the count of seventeen. From the truth table it can be seen that the function necessary to produce the count of seventeen is

$$F = 17 = Q_{2A}\,\overline{Q}_{1D}\,\overline{Q}_{1C}\,\overline{Q}_{1B}\,Q_{1A}\ ,$$

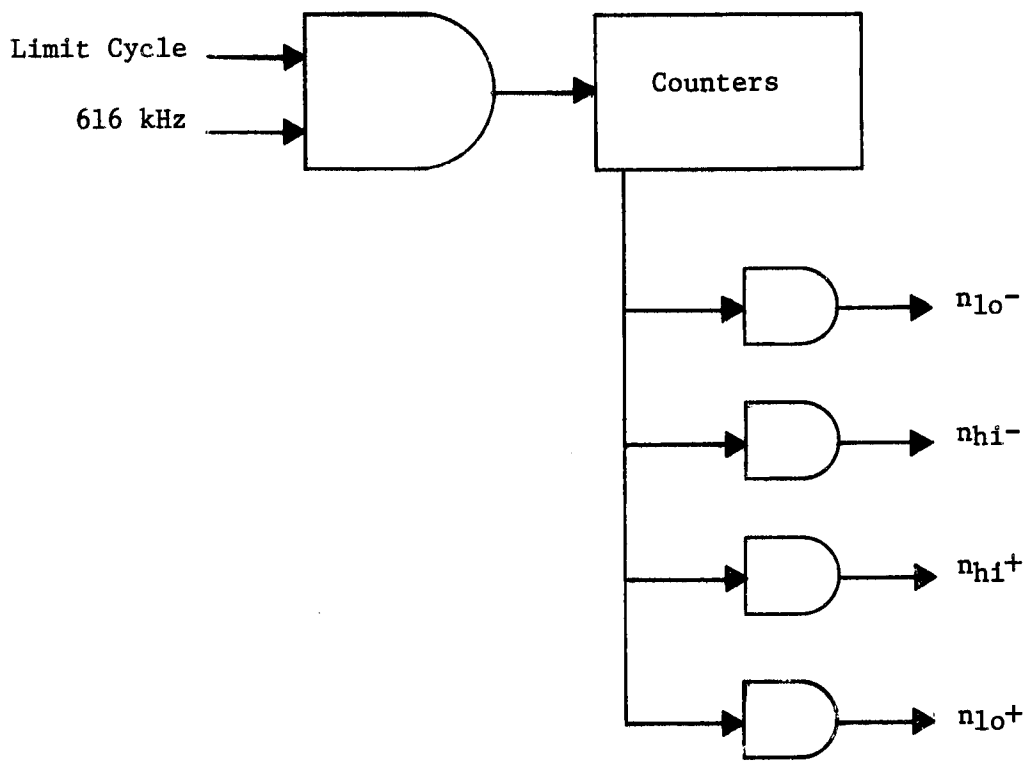


Figure 16. Proposed design for counting data pulses.

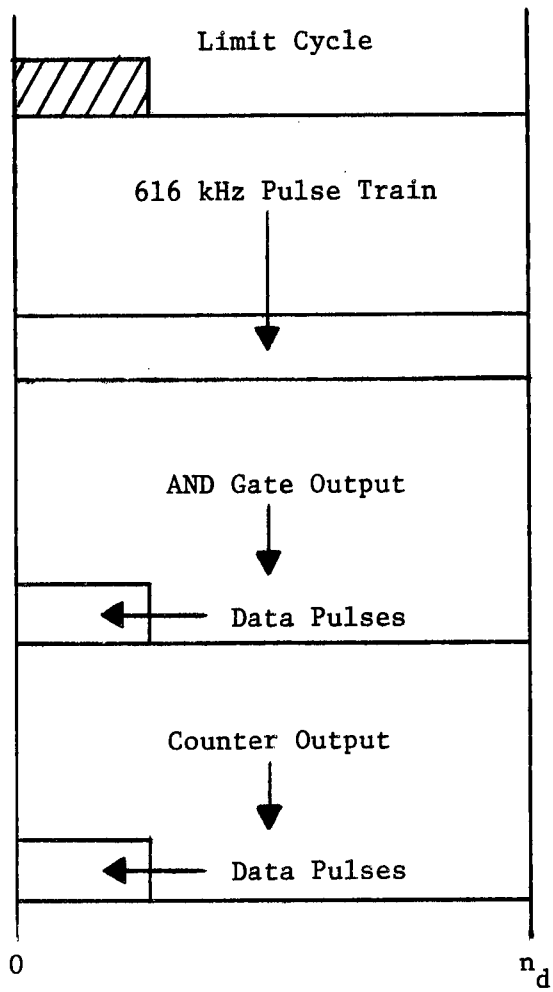


Figure 17. Output waveforms of new SFS section.

Table 2. Derivation for Count of Seventeen

Counter Outputs					
Q_2A	Q_1D	Q_1C	Q_1B	Q_1A	Count
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17

$$17 = Q_2A\ \overline{Q}_1D\ \overline{Q}_1C\ \overline{Q}_1B\ Q_1A$$

where

Q_{2A} is the count of sixteen counter output,

Q_{1D} is the count of eight counter output,

Q_{1C} is the count of four counter output,

Q_{1B} is the count of two counter output,

Q_{1A} is the count of one counter output.

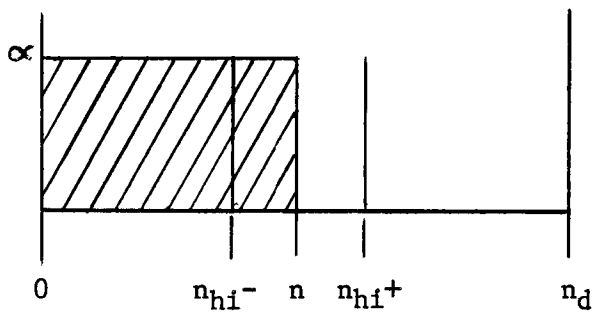
To implement this function would require inverting the Q_{1D}, Q_{1C}, and Q_{1B} outputs of the first counter and then feeding the inputs to an AND gate. Since no AND gates are available in the CMOS logic family, and four inputs are the largest number of inputs available to a gate, it would require six NAND gates plus three inverters to implement this function. Already it can be seen that this procedure would require many more logic pieces to generate the timing marks than the procedure employed by the HS logic. There are several procedures that can reduce the number of logic pieces required to implement the technique of counting data and these are discussed in the following chapter.

The basic reason for counting data pulses can be seen by a study of Figure 18. From this figure the following logic can be derived:

1. If the system is in the high mode and $n > n_{hi}-$ and $n < n_{hi}+$, then the system should switch modes.

2. If the system is in the low mode and $n < n_{lo}-$ or $n > n_{lo}+$, then the system should switch modes.

To satisfy these conditions, it was proposed to use a limit-cycle Q that performs the AND operation with the 0-16 blanking pulse, and a limit-cycle $\overline{Q}$ that performs the AND operation with the 241-256 blanking pulse. This was done to assure that no clock pulse would be applied to the



(A) High Mode



(B) Low Mode

Figure 18. Conditions existing for switching modes of operation.

respective counter when the duty cycle generator output was in either the maximum positive or the maximum negative torque range. This procedure would also require the use of a set of counters for the limit-cycle Q and a set of counters for the limit-cycle $\overline{Q}$. The conditions that this would produce for maximum positive torque, maximum negative torque, and low torque are shown in Figure 19. The outputs shown in Figure 19 are the inputs to the respective set of counters. The logic to implement the new design is shown in Figure 20. When testing this implementation against the summary of operations shown in Table 3, it was concluded that this logic would not work for all cases. As can be seen from Table 3, the logic will not work when the system is in the low mode and $n_{lo}- < n < n_{lo}+$ or when the system is in the high mode and $n_{hi}- < n < n_{hi}+$, because an output should appear at the output of gate 5 when $n < n_{lo}-$, $n > n_{lo}+$, and $n_{hi}- < n < n_{hi}+$. The reason for this is that the coincidence which must occur for an AND gate to produce an output will not occur since it is being fed by two different pulses occurring at different times. A condition will be presented in the next chapter where this idea would be of benefit. Many logic techniques were applied to the technique shown in Figure 20, but no correct logic could be derived. The idea of this logic concept was presented because the technique would require fewer logic pieces than the HS logic, but the main problem of creating the timing marks for comparing the number of data pulses present to that of when the system should switch modes still exists.

The new design was abandoned because no design could be derived in which fewer logic pieces were required than the number required for the HS control logic. The following chapter gives some further possibilities for realizing a system that counts data pulses for scale factor selection.

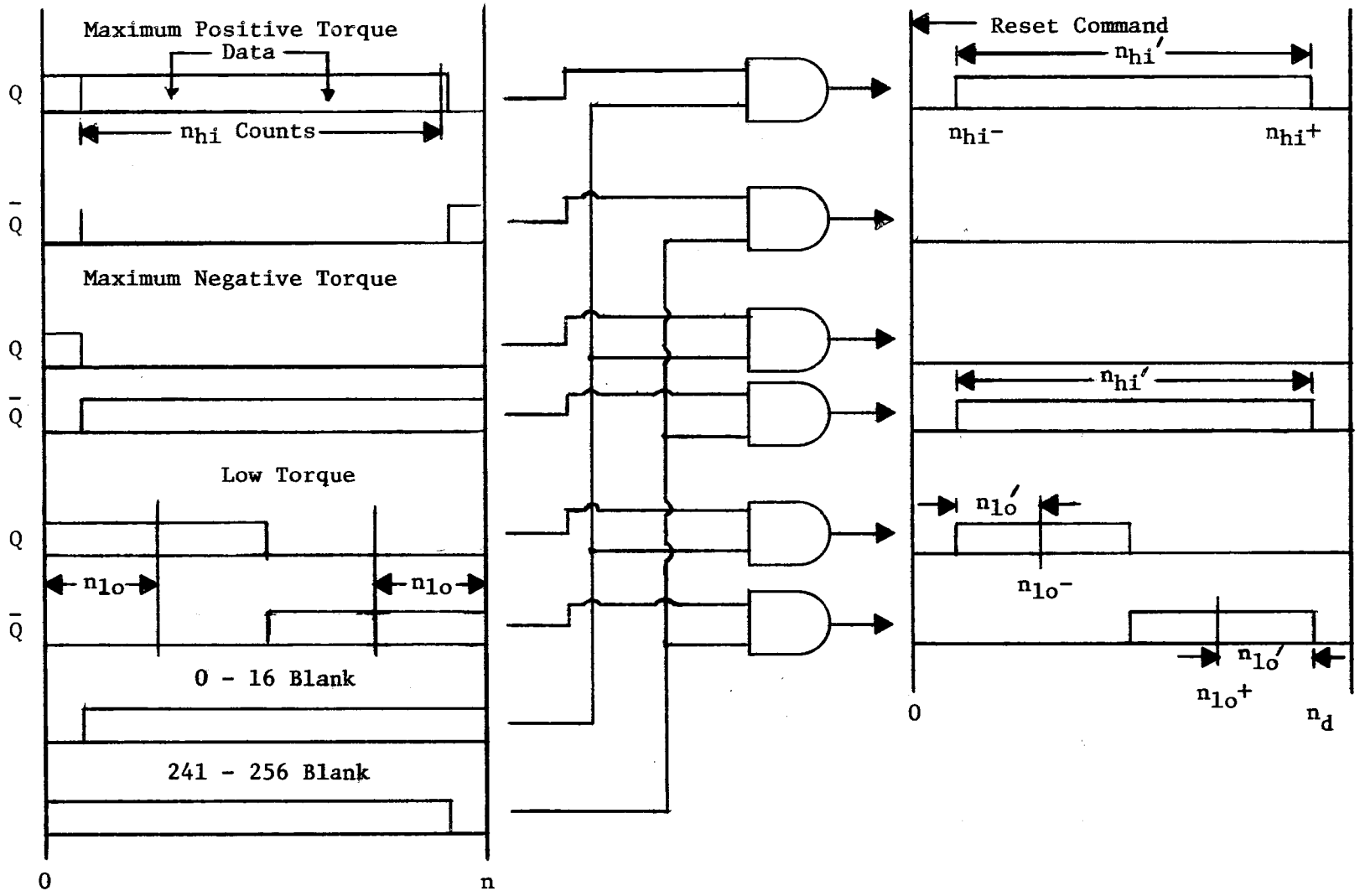


Figure 19. Outputs when employing a limit cycle Q and $\bar{Q}$.

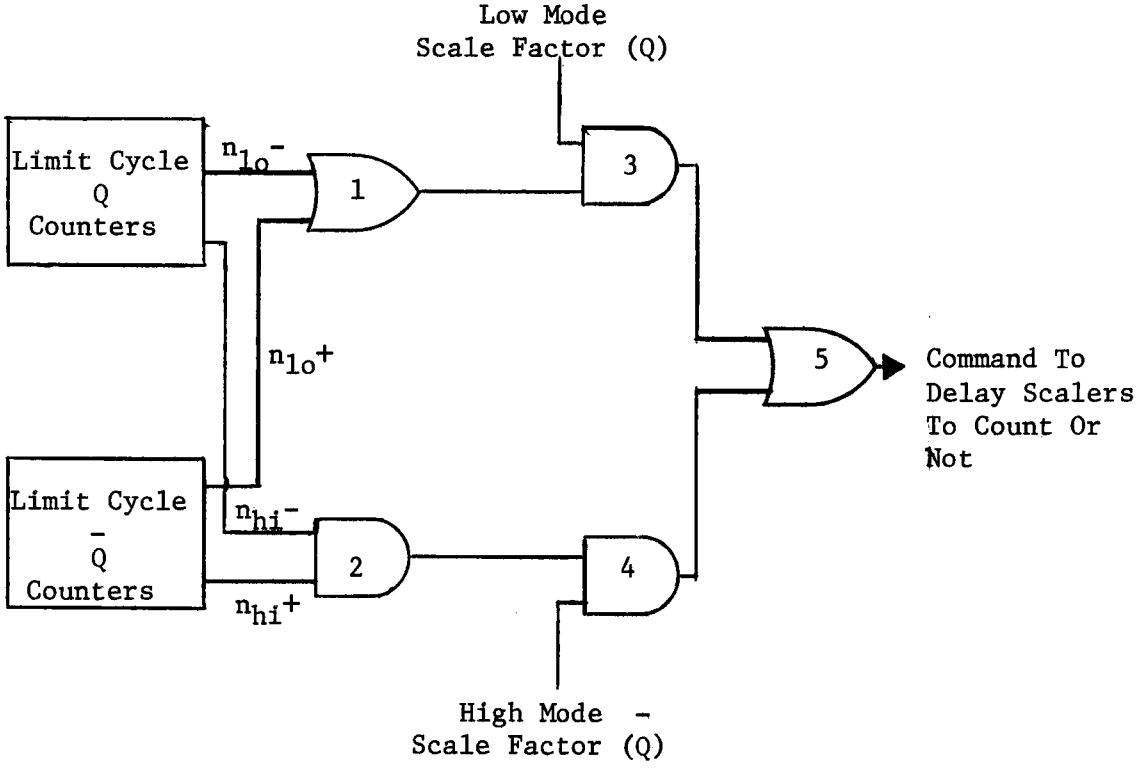


Figure 20. Proposed implementation of logic to generate count command of new design.

Table 3. Summary of Outputs for Proposed Implementation of Logic to Generate Count Command of New Design

Count (n)	Scale Factor Flip Flop Output Q	Scale Factor Flip Flop Output $\overline{Q}$	Gate 1 Input $n_{lo}-$	Gate 1 Input $n_{lo}+$	Gate 2 Input $n_{hi}-$	Gate 2 Input $n_{hi}+$	Gate 1 Output	Gate 2 Output	Gate 3 Output	Gate 4 Output	Gate 5 Output
$n<n_{lo}-$	1	0	0	1	0	1	$1@n_{lo}+$	0	$1@n_{lo}+$	0	$1@n_{lo}+$
$n>n_{lo}+$	1	0	1	0	1	0	$1@n_{lo}-$	0	$1@n_{lo}-$	0	$1@n_{lo}-$
$n_{lo}-<n<n_{lo}+$	1	0	1	1	X	X	$1@n_{lo}-$, $n_{lo}+$	0	$1@n_{lo}-$, $n_{lo}+$	0	$1@n_{lo}-$, $n_{lo}+$
$n<n_{hi}-$	0	1	X	1	0	1	$1@n_{lo}+$	0	0	0	0
$n>n_{hi}+$	0	1	1	X	1	0	$1@n_{lo}-$	0	0	0	0
$n_{hi}-<n<n_{hi}+$	0	1	1	1	1	1	$1@n_{lo}-$, $n_{lo}+$	0	0	0	0

where: 1 represents a "high"
0 represents a "low"
X represents either a "low" or "high"

CHAPTER V

CONCLUSIONS

I. Summary of the Thesis

Several objectives of this thesis as presented in the Introduction were completed, while one objective was not. The HS system was analyzed and the findings have been reported in Chapter II. A new control logic was then developed using CMOS logic components. The new CMOS system was constructed and tested in the laboratory and found to function properly. Although the system could not be designed to use fewer logic pieces, important facts were found.

In analyzing the HS logic, there were certain techniques employed that seem to have no logic value. The first of these was the use of a monostable in establishing the 616 kHz 0.4 μsec wide pulse. The advantages and disadvantages of this have been discussed in this thesis, but it was found that the logic design meets the requirements without the use of the monostable. The second technique employed in the HS that did not prove to be necessary for CMOS logic was that the timing marks were fed into a set of 4-bit RIGHT-SHIFT LEFT-SHIFT REGISTERS. It appears that the purpose of these registers was to store the information that was present on the inputs. When developing the system using CMOS logic components the registers were included, but served no positive function and therefore were removed. The system operated properly without the registers. The third technique employed in the HS that appears to be unnecessary for proper operation of the logic section was that the scale

factor flip-flop outputs were inverted to produce the low and high mode scale factor commands. These same signals could have been attained by proper selection of the outputs of the scale factor flip-flop. In developing the system these inversions were included and it was assumed that they were necessary for the total rebalance electronics loop system to operate properly.

In developing the HS logic using CMOS logic components as compared to the TTL logic that is presently used, several additional pieces were required to perform certain functions while other functions required fewer logic pieces. The first of these differences can be noted in the BCD-to-Decimal Decoders. The TTL logic decoders produced a zero blanking period on their output, while the CMOS decoders produced a high output for the same period on their output pins. This fact required the use of the AND operation to generate the timing marks using CMOS logic as compared to the NOR operation using the TTL logic. Since no AND gates are available in the CMOS logic family, the AND operation had to be performed by a NAND operation followed by an inversion. Thus the need for more logic pieces was required here when using CMOS logic.

The second difference between the two logic families that produce a change in the number of logic pieces required was that the TTL family only has 4-bit counters available. Due to this fact it was necessary to use three stages in order to implement the count of 2048 for the delay counters. In contrast, the CMOS logic family offers a 7-bit binary counter. In using the 7-bit counters the count of 2048 could be obtained in two stages, thus the CMOS logic family offers a savings of one logic piece.

The third difference between the logic families is noted in the fact that the TTL flip-flops reset the Q output to zero when a "low" is applied to the reset. The CMOS flip-flops reset to zero when a "high" is applied to the reset input. Thus, the need to invert the flip-flop reset signal was required. All other logic pieces were compatible between the two logic families.

New logic functions are now available in the TTL and CMOS logic families that were not available at the initiation of this study. All three stages of the scalers in the CMOS DFG can now be obtained by using one 12 stage binary instead of three 4-bit binaries. A 12-bit counter is available which would allow the use of one counter for the delay scalers instead of the two as required in this thesis. In the TTL logic family higher orders of bit counters are available in TTL MSI (Medium Scale Integrated) circuitry, thus reducing the required number of logic pieces in this system.

To the author, it first seemed that the best logical way to obtain the timing marks was to use counters and then perform the AND operation on the appropriate counter outputs. As proven in this thesis, this technique would require the use of more logic pieces than the number used in the HS logic. An attempt was also made to use fewer logic pieces in generating the count signal to the delay scalers. As shown in Chapter IV no solution to this problem was reached. Although no better design was derived, some important facts were disclosed that should be considered at a future time. These facts are presented in the next section.

II. Suggestions for Further Study

Due to the simplicity of the logic required to generate the count signal to the delay scalers as presented in Chapter IV, further study is

needed in order to reduce the total number of pieces required to implement the new control logic. The logic presented in Chapter IV, Figure 20, page 47, along with the idea of using a limit-cycle Q and a limit-cycle $\overline{Q}$, will pass the correct output if the n count is used as the inputs to the gating sequence instead of the timing marks. An area of further study would be to produce these outputs by considering the position of the count (n), and then comparing this output with the mode of operation the system is in and the timing marks. This solution to the problem still does not solve the question of how to generate the timing marks.

Since CMOS circuits are still relatively new, there is no doubt that some of the needs will be met by future MSI designs. Further, many manufacturers are interested in custom CMOS design, and if sufficient volume were needed, many of these required digital control functions could be implemented in a custom design.

An area of study that could be given some attention is the following: If the timing marks are derived by pulling only the counts needed to attain a certain count from the counter outputs, and then these outputs were passed through an AND operation, this would produce an output that contains higher multiples of the count which has been derived. For example, to get the count of seventeen, only the output of the counters containing the count of sixteen and one are used. Due to the symmetry of the timing marks, and the fact that the first pulse of the count will appear at the count of the timing mark required, possibly a don't care[8] situation could be set up for the higher multiples of the count.

Another area of further study is the generation of timing marks. To reduce the number of pieces required, the following technique is proposed and is outlined in Figure 21. The basic principle used here is that the counters are constructed of flip-flop integrated circuit chips instead of using the 4-bit counter integrated circuit chips. The purpose for using the flip-flops is that both Q and $\overline{Q}$ outputs are available, whereas with the counter only the Q output is available. Since the correct logic for the count is obtained by performing the AND operation, the following logic was derived

$$A \cdot B = \overline{\overline{A} + \overline{B}} \ .$$

This logic can be implemented by using the $\overline{Q}$ output of the flip-flops fed to a NOR gate as shown in Figure 21. This alone will reduce the number of logic pieces because now no inverters or NAND gates are required. By feeding the outputs of the NOR gates to the second stage of flip-flops will cause the flip-flops to ge "high" at the designated count. A method of attaining the appropriate timing mark would be to load the second stages of flip-flops with the next highest count of the timing marks, and then perform the AND operation of the $\overline{Q}$ output, and the count obtained by performing the AND operation off the first flip-flop stages. This would help reduce the number of logic pieces required but still would require more than that used in the HS logic.

The technique presented in Figure 21 would also offer the benefit of generating the limit cycle Q and $\overline{Q}$ without two different stages of counters as presented in Chapter IV. Thus, an investigation into the minimum number of pieces required in combining these methods is suggested for future study.

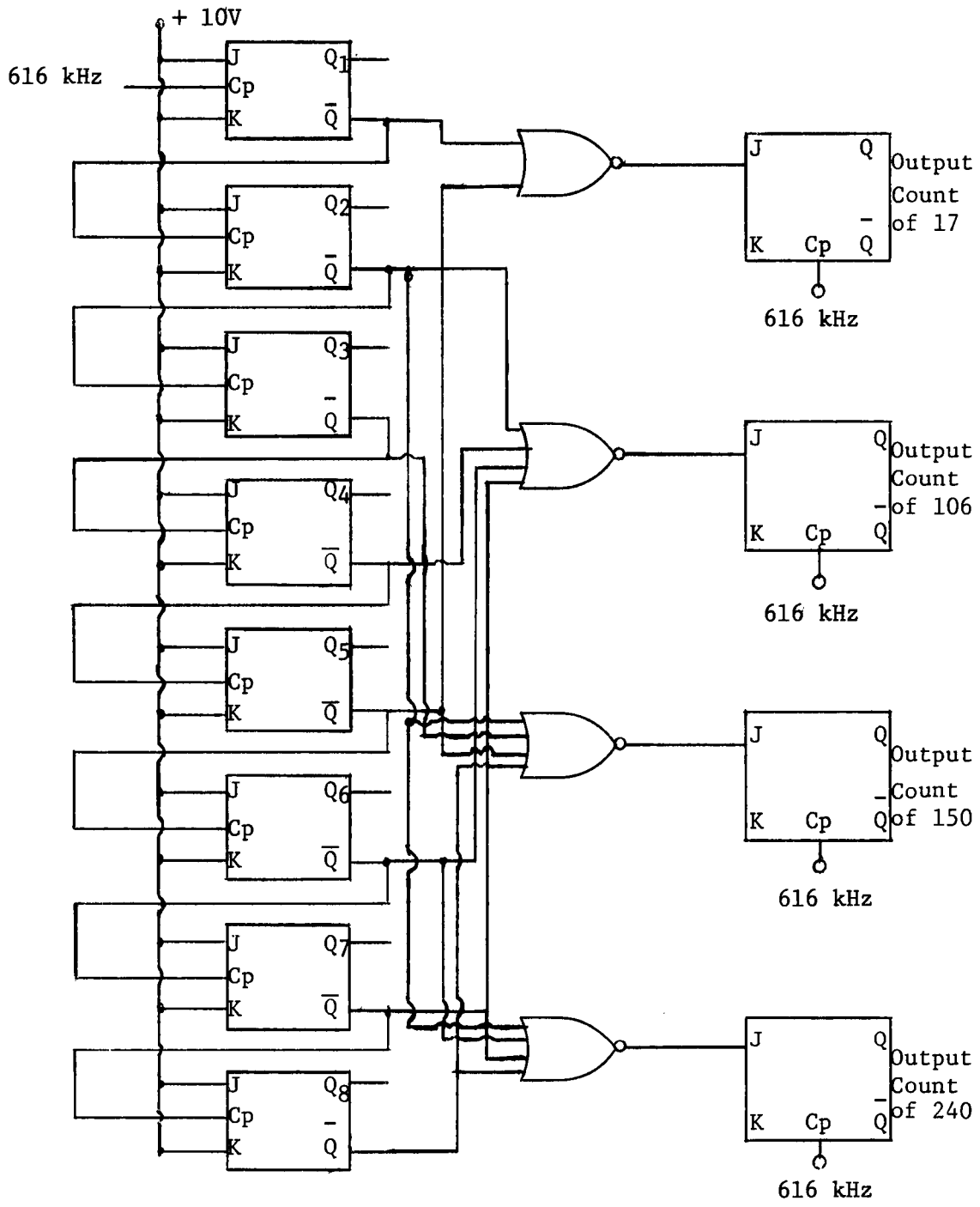


Figure 21. Derivation of timing marks using flip-flops.

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APPENDIXES

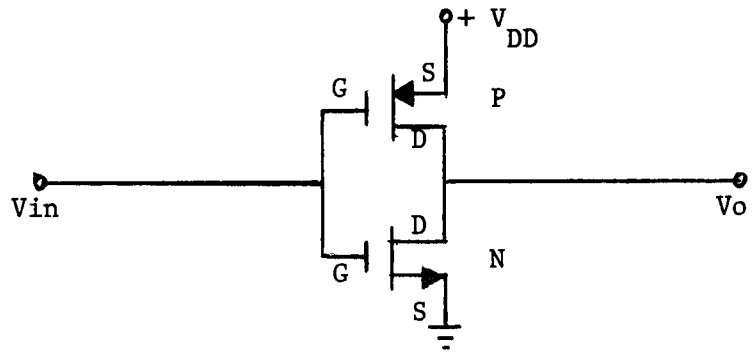
APPENDIX A

CHARACTERISTICS OF A BASIC CMOS LOGIC INVERTER

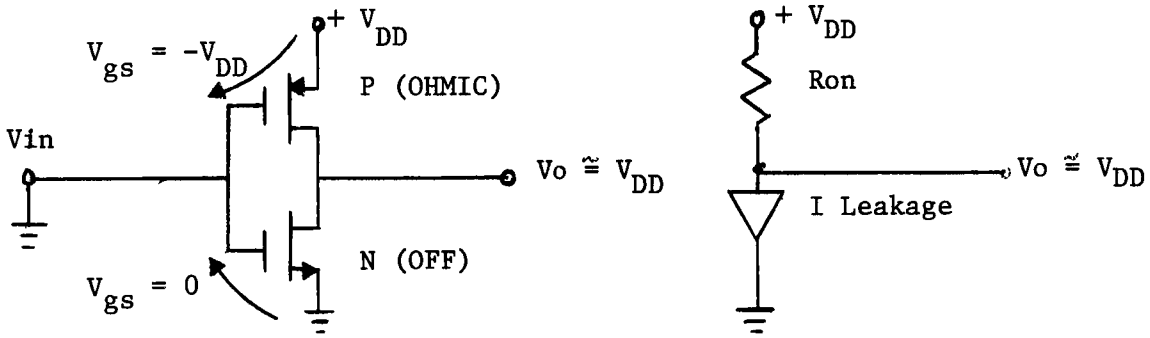
The basic logic inverter (or gate) formed by use of only a p- and an n-type device in series is shown schematically in Figure 22A. When the input lead is grounded (logical "0"), the n-device is cut-off, and the p-device is biased on. As a result, there is a low-impedance path from the output to V_{DD}, and an open circuit to ground. The resultant output voltage is essentially V_{DD}, or a logic "1." Figure 22B depicts this situation.

Similarly, when the input voltage is a logic "1," or V_{DD}, then the n-channel device becomes a low impedance, while the p-channel device becomes essentially zero volts (logic "0"). Figure 22C depicts this situation.

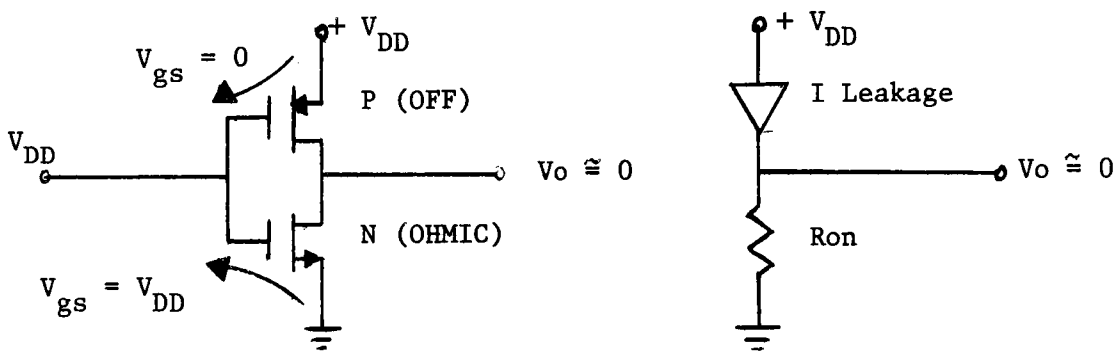
Note that one of the devices is always cut-off at either logic extreme, and that no current flows into the insulating gates. As a result, the inverter quiescent power dissipation is negligible (equal to the product of V_{DD} times the leakage current). Figure 23 shows typical characteristics of the RCA CMOS logic devices for transfer characteristics and power dissipation.[5]



(A) Basic Complementary - Pair Inverter

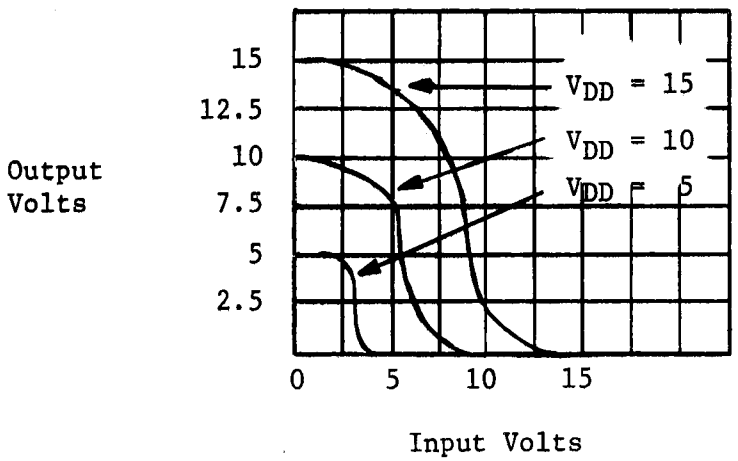


(B) Reduced Model Under Logical - 0 Excitation

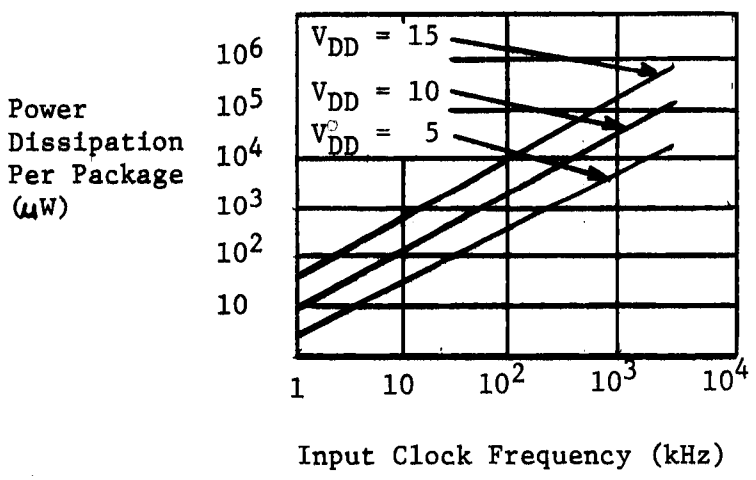


(C) Reduced Model Under Logical - 1 Excitation

Figure 22. Complementary-symmetry logic.



(A) Transfer Characteristics



(B) Power Dissipation Characteristics

Figure 23. Typical characteristics of RCA CMOS devices.

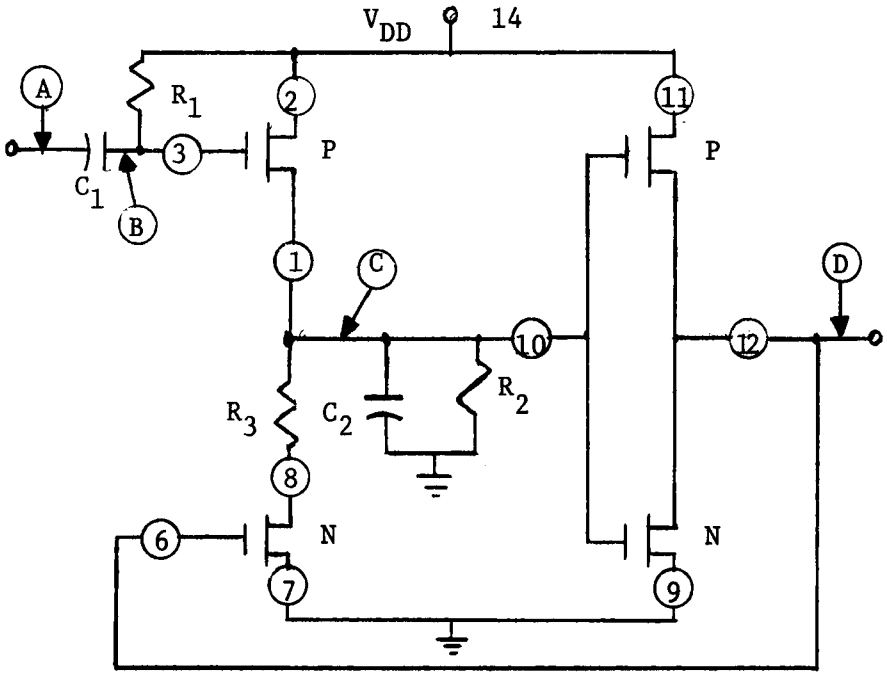
APPENDIX B

DESIGN OF A MONOSTABLE USING RCA CMOS CD4007A INVERTER

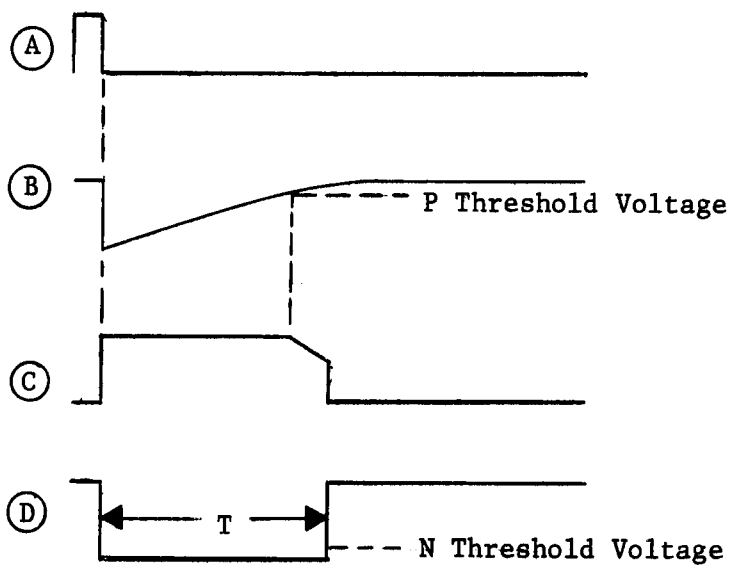
Figure 24A shows a circuit using the RCA CD4007A integrated circuit as a monostable. Figure 24B shows the waveforms of this circuit. In the quiescent state, the p-channel transistor of the first inverter is off, while the n-channel transistor is biased on. Therefore, the output at C is low, and that at D is high. When a negative-going pulse is introduced into the circuit through C_1, the capacitor C_1 becomes negatively charged, and the p-channel device is turned on. C_2 then charges to V_{DD}, the output of D becomes low, and the n-channel device of the first inverter is turned off. C_1 immediately begins to charge to V_{DD} through R_1. The p-channel transistor remains on, keeping C_2 charged to V_{DD}, until the waveform generated passes through its threshold voltage level and turns it off. The n-channel transistor of the first inverter is still off because the output of the second inverter is still low. When the p-channel device of the first inverter turns off, C_2 begins to discharge through R_2 to ground. As it discharges, it passes through the threshold voltage of the second p-channel transistor so that it begins to turn on. The voltage waveform at D then begins to rise, and the n-channel device of the first inverter turns on and provides a second discharge path for capacitor C_2. As a result, the output waveform changes state from low to high quite rapidly to complete the cycle.[5] From the experimental evaluation of this circuit the input used was the 616 kHz frequency.

Using

$$v(t) = FV + (IV - FV)\ e^{-t/\tau}$$



(A) Circuit



(B) Waveforms

Figure 24. Monostable using a RCA CMOS CD4007A inverter.

and a threshold voltage of 1.5 volts for both p- and n-channel devices, the following two equations can be written

$$v_1(t) = 10 + (0-10)\, e^{-t/R_1C_1} = 10 - 10\, e^{-t_1/R_1C_1} ,$$

$$v_2(t) = 0 + (10-0)\, e^{-t/R_2C_2} = 10\, e^{-t_2/R_2C_2} .$$

Solving these equations yields

$$t_1 = 1.9\, R_1C_1 ,$$

$$t_2 = 0.36\, R_2C_2 ,$$

since

$$T = t_1 + t_2 = 1.6\ \mu\text{sec} ,$$

the following assignments were made to obtain the 616 kHz 0.4 μsec wide pulse

$$t_1 = 1.2\ \mu\text{sec} = 1.9\, R_1C_1 ,$$

$$t_2 = 0.4\ \mu\text{sec} = 0.36\, R_2C_2 .$$

By using these equations, the values used for R_1, R_2, C_1, and C_2 were

$$R_1 = 4.27\ \text{k}\Omega ,$$

$$C_1 = 101\ \text{pf} ,$$

$$R_2 = 6.81\ \text{k}\Omega ,$$

$$C_2 = 159\ \text{pf} .$$

These values have been experimentally verified.

VITA

The author was born in Fairfax County, Virginia, on May 18, 1944. He graduated from Fairfax High School in 1963. He attended Northern Virginia Community College and received an Associate in Applied Science degree in Electronic Technology in June, 1968. He received a Bachelor of Science degree in Electrical Engineering from Virginia Polytechnic Institute and State University in December, 1971. At that time, he began study toward a Master's degree at the University of Tennessee.

He is married to the former Susan Crowley of Garden City, New York.