To the Graduate Council:

I am submitting herewith a thesis written by Thomas Chris Layne entitled "Real Time Signal Validation Circuitry for Burst-Type Laser Velocimeters." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Ronald A. Belz, Major Professor

We have read this thesis
and recommend its acceptance:

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Accepted for the Council:

The Graduate School

REAL TIME SIGNAL VALIDATION CIRCUITRY FOR BURST-TYPE LASER VELOCIMETERS

A Thesis

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ABSTRACT

The laser velocimeter (LV) is often used to measure the velocity of fluid flows. Burst-type signal processing is one of the more popular methods of extracting velocity information from randomly occurring LV signals. A major assumption in burst-type signal processing is that each LV signal processed is the result of an individual particle which is following the flow. Before accepting a measurement, burst-type LV processors perform various signal validation tests which determine if an LV signal satisfies the above assumption. These signal validation tests are either performed during data acquisition (at the expense of a minimal data acquisition cycle time) or after data acquisition has ended (at the expense of efficient data acquisition memory use). Circuitry was designed which performs a signal validation test in real time, thereby making efficient use of data acquisition memory at no cost in time to the data acquisition cycle. A system was designed to simulate LV signals so that the signal validation circuitry could be compared to another method of hardware signal validation under controlled and repeatable conditions. Results are presented from tests made by processing these simulated LV signals. Results are also presented from tests made by processing real LV signals. These results show that the signal validation circuitry consistently improves the quality of the data acquired by the LV processor. The most substantial improvement in the data quality is observed when processing signals with a low signal-to-noise ratio.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER I

INTRODUCTION

Considerable effort has been expended in the development of laser velocimetry techniques for fluid flow measurements since their initial development some nineteen years ago [1].* In recent years much attention has focused on the burst-type laser velocimeter (LV). The interest in burst-type LV systems can be understood by examining the mechanism by which LV signals are generated. Two mutually coherent and polarization-alligned laser beams are crossed to establish equally spaced, planar regions of maximum and minimum illuminating intensity, called interference fringes. The crossover region defines a volume in space called the sample volume. As a particle following the flow passes through the sample volume, it experiences illumination that sinusoidally alternates from some maximum value to a minimum value. If the light scattered out of the sample volume is focused onto a photosensitive detector, such as a photomultiplier tube, the detector will output an amplitude-fluctuating signal whose rate of amplitude fluctuation (frequency) is proportional to the rate at which the particle intercepts the interference fringes. Thus, the velocity of the particle can be determined by dividing the distance between adjacent maxima (interference fringes) by the measured period of the photodetector's output. Unlike burst processors, most other LV signal processing methods (including classical spectral analysis and

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*Numbers in brackets refer to similarly numbered references in the List of References.

frequency tracking) require a quasi-continuous LV signal (i.e., a high concentration of light-scattering particles within the flow). In many applications the concentration of scattering centers is too low to generate a quasi-continuous signal; under such conditions burst-type processors are most applicable.

Burst-type processors were designed to process a composite signal consisting of high-frequency sinusoidal oscillations (the periodic component) that are superimposed on a Gaussian-shaped lower frequency bias signal (the pedestal component). The number of cycles in the periodic component and the time between adjacent signal bursts are variables correlated with such parameters as the number of interference fringes in the sample volume, the size of the sample volume, the flow seeding, and the flow velocity. The basic operation performed by a burst-type processor is the measurement of the average period of the periodic component of the LV signal. This period measurement is made by filtering out the pedestal component of the signal and then counting the number of cycles of a high-frequency clock (with known period, τ_{CLK}) during a preselected number of cycles of the signal burst. In other words, if the processor is set up to average the input over N_L cycles then the average period of the periodic component, τ_{PER}, is given by

$$\tau_{PER} = \frac{N_{CLK}\,\tau_{CLK}}{N_L} \tag{1}$$

where N_{CLK} is the number of cyles of the high frequency reference clock contained in the N_L cycles of the input signal burst. The primary assumptions here are that all N_L cycles of the input were

generated by a single particle passing through the sample volume and that the particle was not undergoing acceleration or deceleration; otherwise, the measurement will be in error. As each individual measurement is made, it is stored so that the flow can later be described statistically.

Virtually all burst processors employ some form of signal validation to detect and delete erroneous data. These error detection methods are usually based on the assumption that there is no significant change in the period of the signal burst within a period on the order of the time of flight through the measuring volume [2]. Thus, if one can detect measurable changes in frequency or period of the signal burst occurring during a measurement, then the data is assumed to be in error and the measurement is excluded from the flow statistics.

Some common signal validation techniques will be discussed in the next chapter. However, it should be noted that these techniques cause either an increase in the processor's dead time between successive measurements (important in short-lived flows such as rocket engine exhausts) or the storage of erroneous data that must be rejected after data acquisition is over (important in systems with limited memory such as microcomputer-based processors). Present signal validation techniques require that minimal system dead time be sacrificed for efficient memory use or vice versa. This thesis will describe signal validation circuitry that was designed to efficiently use data acquisition memory at no cost to system dead time.

The design was carried out with the goal of integrating the resulting circuitry into an existing microcomputer-based LV processor [3]. The design philosophy and hardware will be detailed in Chapters II and III. In order to confirm the operation of the signal validation circuitry under controlled and repeatable conditions, an additional circuit was designed to simulate LV signals (the design of this circuit is detailed in the Appendix). Chapter IV contains a comparison of a common signal validation method and the signal validation circuitry described in this thesis when processing simulated signals. Data resulting from the processing of real signals is also presented in Chapter IV. A summary of the work along with conclusions and recommendations is presented in Chapter V.

CHAPTER II

REVIEW OF BURST-TYPE SIGNAL PROCESSING

The operation of a burst-type signal processor can be best understood by examining the block diagram and timing diagram shown in Figure 1. The amplified output of the photomultiplier tube (PMT) is high-pass filtered so that the low-frequency pedestal component of the signal burst is removed, leaving only the high-frequency periodic component [4]. The zero crossing detector (ZCD) converts the periodic component to a digital pulse train with pulse widths determined by the length of time the signal exceeds the ZCD's threshold level. The threshold level is generally set just high enough so that noise on the ZCD's input (in the absence of signal) does not generate output pulses. The period of the ZCD's output, τ_{PER}, is related to the flow velocity, V, by

$$V = \delta/\tau_{PER} \tag{2}$$

where δ is the distance between adjacent interference fringes.

The ZCD's output serves as the clock signal for the fringe counter. The fringe counter generates the gating pulse, LONG, whose width is equal to N_L periods of the ZCD output, the time required by the particle to cross N_L interference fringes. The value of N_L preset into the fringe counter may be set either by hardware (fixed) [5] or by software (programmable) [3]. The gating pulse (LONG) is used to gate the high-frequency reference clock into the clock counter. When LONG goes low, the clock counter output, N_{LCC}, is stored (or printed in some cases) and the processor is reset, enabling it to process the

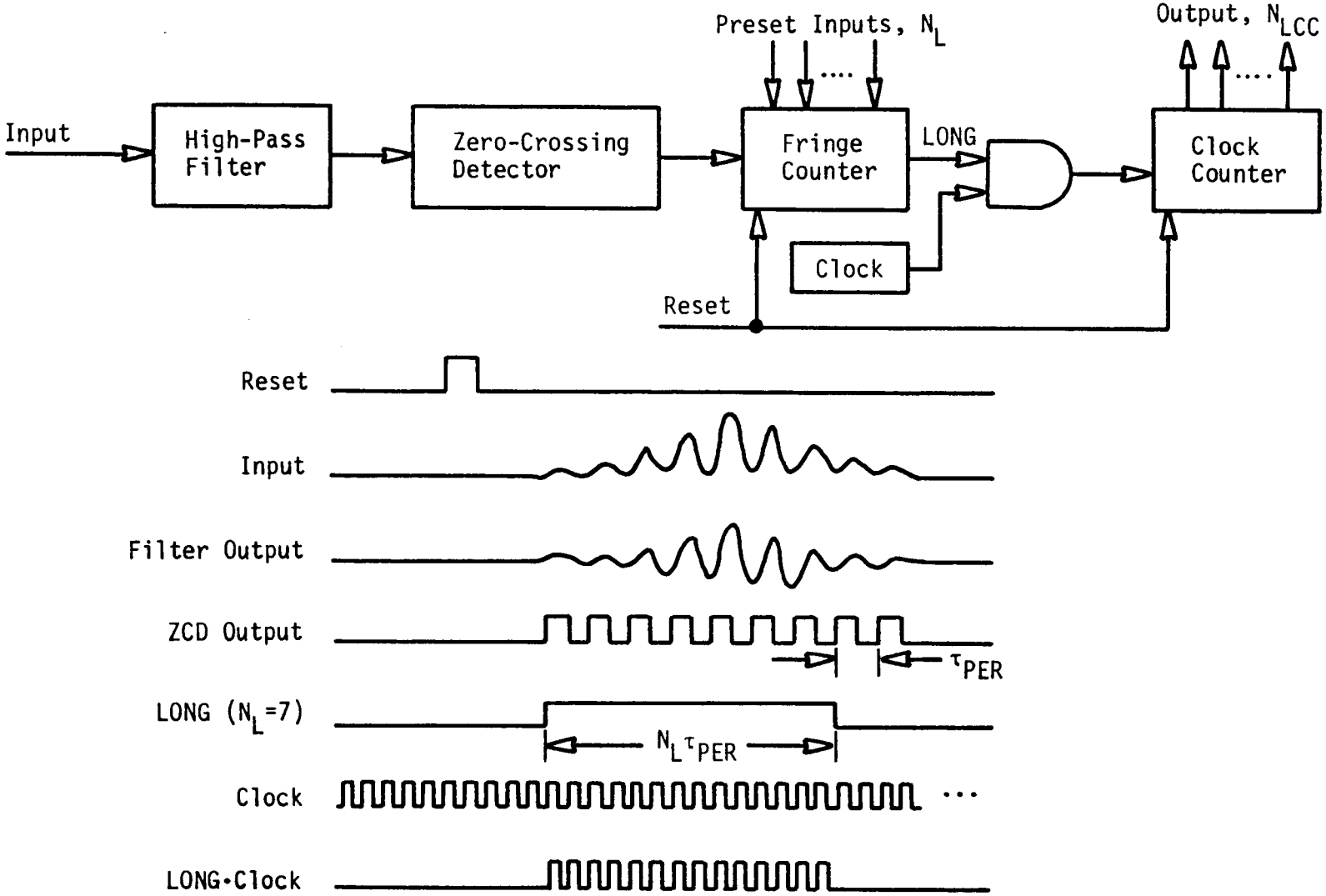


Figure 1. Basic LV burst processor and timing diagram.

next burst that occurs. After data acquisition has ended, individual clock counter readings are transformed to velocity data by combining Equations 1 and 2 yielding

$$V_i = \frac{\delta N_{L_i}}{N_{LCC_i} \tau_{CLK}} \tag{3}$$

where V_i is the ith velocity measurement.

Theoretically, the burst processor of Figure 1 is acceptable; however, in practice it does not perform well because the ZCD's input is often a noisy random signal [10,11]. Consider the ZCD output shown in Figure 2. A ZCD output such as this would be caused by one particle leaving the probe volume (signal dropout) shortly followed by another particle entering it. Note that the final count accumulated by the clock counter is erroneously high; this causes a measured τ_{PER} of 2.5 τ_{CLK} when the actual value is 2.0 τ_{CLK}. This result of making a measurement on such a signal would be a measured velocity lower than the true value.

Errors like this can be eliminated by testing the ZCD output for periodicity. A popular way to test a signal's periodicity involves a second set of fringe and clock counters as shown in Figure 3. The LONG fringe counter is preset to count N_S cycles, where N_L is greater than N_S. At the end of a measurement, the LONG and SHORT clock counters hold counts of N_{LCC} and N_{SCC}, respectively. The aperiodicity error, ε, is given by [8]

$$\varepsilon = \left| 1 - \frac{N_L N_{SCC}}{N_S N_{LCC}} \right| \tag{4}$$

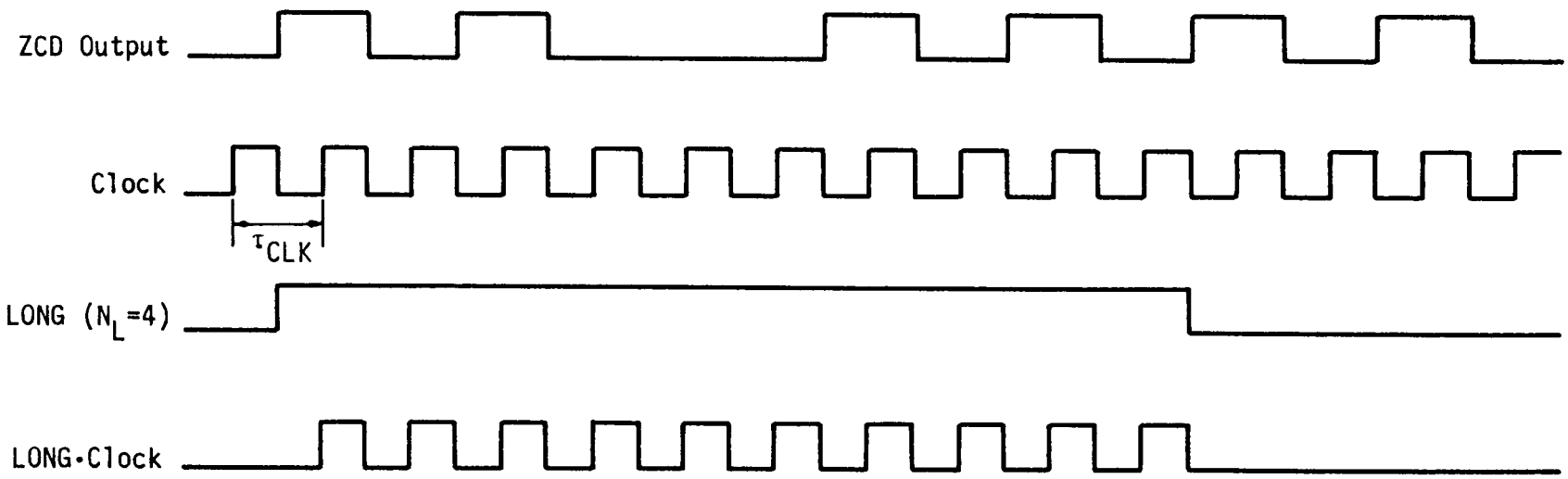


Figure 2. LV burst processor timing diagram with ZCD dropout.

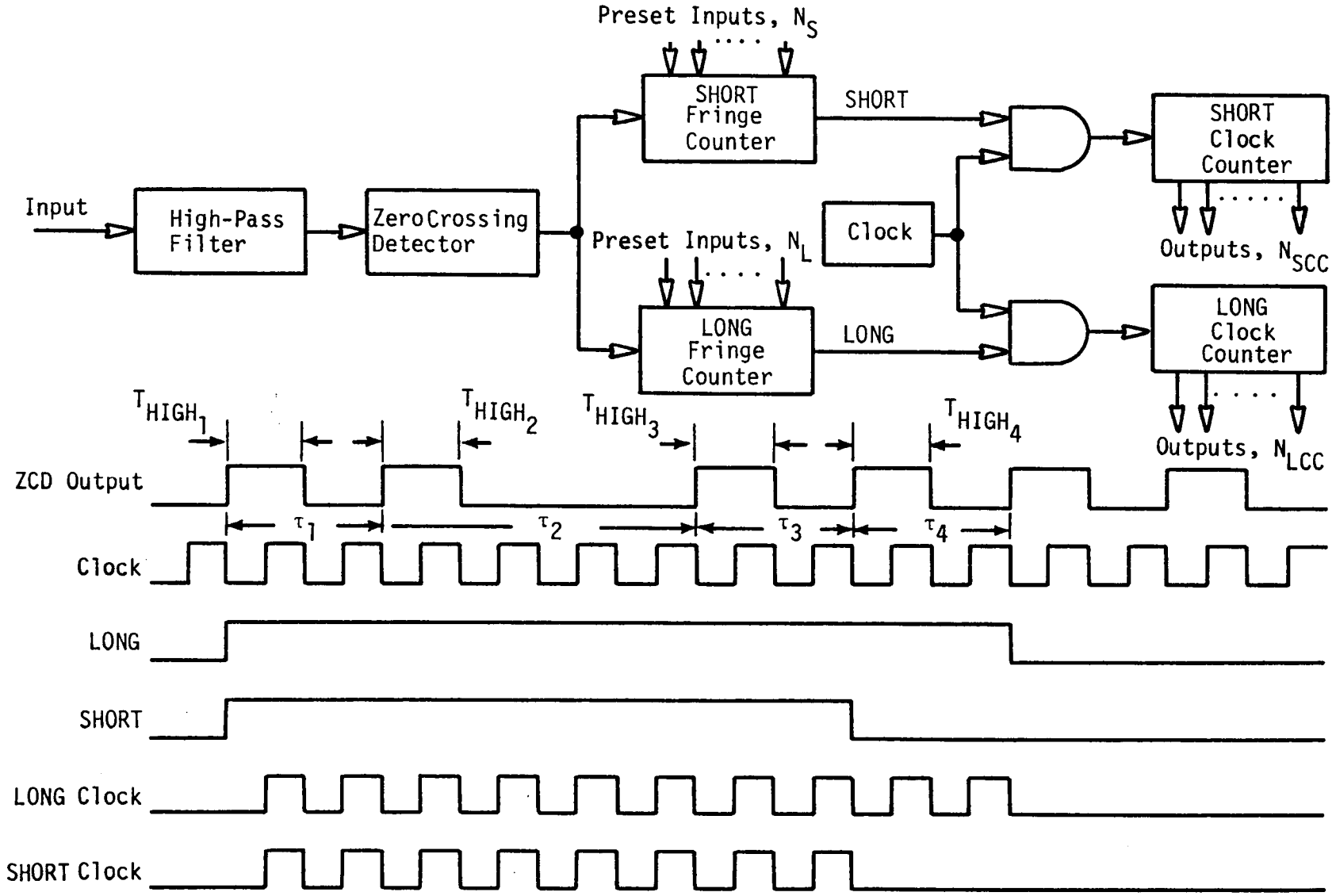


Figure 3. Dual counter burst processor and timing diagram.

In the case of a periodic ZCD signal, the ratio N_L/N_S would equal the ratio N_{LCC}/N_{SCC}; therefore, a periodic signal would have an aperiodicity error of zero. When the aperiodicity error exceeds a preset limit for a given measurement, the measurement is rejected. The timing diagram of Figure 3 demonstrates how an aperiodic ZCD signal would be processed. The LONG and SHORT fringe counts are 4 and 3, respectively; the resultant LONG and SHORT clock counts are 10 and 8, respectively. Thus, the aperiodicity error given by Equation 4 is 6.7 percent.

Since the aperiodicity error is the criterion on which data is accepted or rejected, it should be computed before data is stored if memory is to be economically used. Even though some processors employ such sophisticated schemes as specialized hardware [5] and microcomputers programmed in machine language [6], the evaluation of the aperiodicity error cannot be done in real time. The processor is unable to acquire new data during signal validation; therefore, the processor's dead time is increased for the sake of efficient use of the data storage medium.

A primary cause of high aperiodicity error is signal dropout occurring during a measurement. The burst processor designed by Morris [3] includes a dropout detector to reset the processor when signal dropout occurs. Operation of the dropout detector can be understood by examining the block diagram shown in Figure 4. A binary counter, called the high counter, accumulates a count, K_H, proportional to the length of time that the ZCD output is high; another counter, called the low counter, contains a count, K_L, proportional to

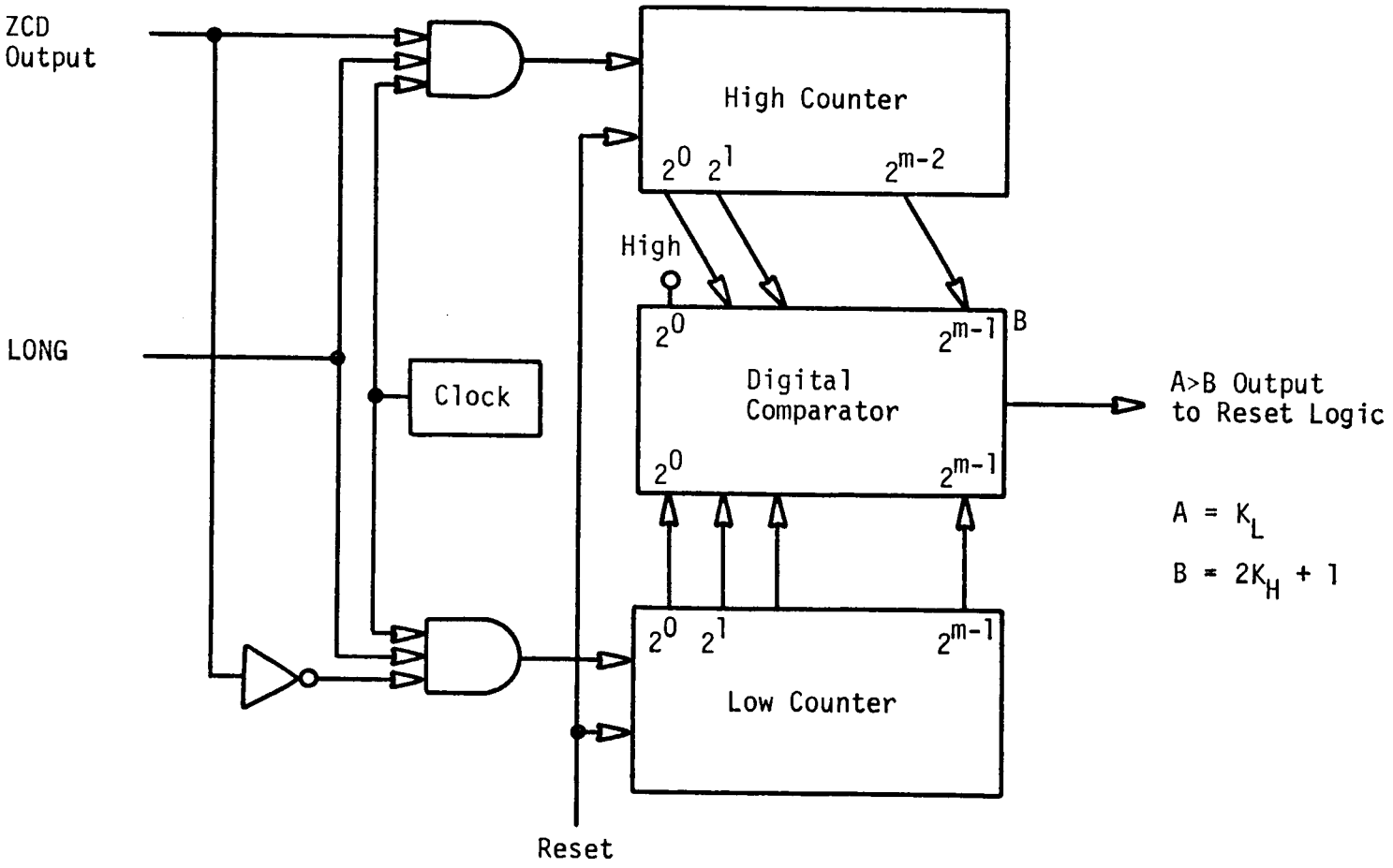


Figure 4. Block diagram of signal dropout detector.

the length of time the ZCD output is low. The high count is multiplied by two (by shifting right one bit) and compared to the low count. if the signal drops out and ZCD stays low twice as long as it was high ($K_L > 2K_H + 1$), then the comparator generates a reset pulse to the processor. Since the dropout detector has the ability to detect aperiodic signals during data acquisition, the aperiodicity error is evaluated through software after data acquisition has ended, keeping system dead time to a minimum.

Basically, the dropout detector performs a crude aperidicity test in real time; however, it should be noted that the sensitivity of the dropout detector to an aperiodic signal is not only a function of the signal's aperiodicity but also a function of when the aperiodicity occurs and the ZCD threshold level. For example, when a signal drops out near the beginning of a measurement, the low counter will double the high counter sooner than if dropout had occurred later in the measurement; thus, the dropout detector is more likely to reject an aperiodic signal if dropout occurs early in the signal. Also, the higher the ZCD's threshold level is set, the sooner dropout will be detected. The dropout detector is not able to detect every aperiodic signal (the aperiodic signal of Figure 3 would be undetected by the dropout detector); therefore, measurements based on aperiodic signals will be stored only to be rejected later by the software aperiodicity test. In this way, efficient use of memory is traded for minimal system dead time.

The signal validation circuitry (SVC) to be described is similar to the dropout detector in that binary counters and comparators are

used to determine if the ZCD output becomes aperiodic in the course of a measurement. The SVC, however, determines on a period-by-period basis if the ZCD output is periodic. Basically, the SVC measures the period of each cycle of the ZCD output and resets the LV processor if the period of a cycle does not fall within a preset percentage of the previous cycle's period. In other words, the period of the second cycle must equal the period of the first cycle within some percentage of the first cycle. The third cycle is similarly compared to the second cycle and so on until the fringe count is completed. Since the SVC eliminates the need for a dropout detector, it was designed to be interchangable with the dropout detector in the LV processor described in [3].

A complete block diagram of the LV processor designed by Morris is shown in Figure 5. This is the same basic processor as shown in Figure 3 except for the addition of a precounter, a digital high-pass filter, and microcomputer control. In order to avoid starting measurements at the beginning of a burst when the signal-to-noise (S/N) ratio is low, the precounter requires that a preset number of ZCD pulses be counted before the ZCD is gated to the fringe counters. The digital high-pass filter compares the LONG clock count to a preset limit; if the LONG clock count exceeds the high-pass filter limit, the processor is reset. This prevents the storage of erroneously low velocity measurements possibly resulting from relatively large particles that tend to lag behind the flow. The operation of the dropout detector was detailed earlier in this chapter and will not be explained here. The processor is controlled via data, address, and control busses by a Z-80 based microcomputer.

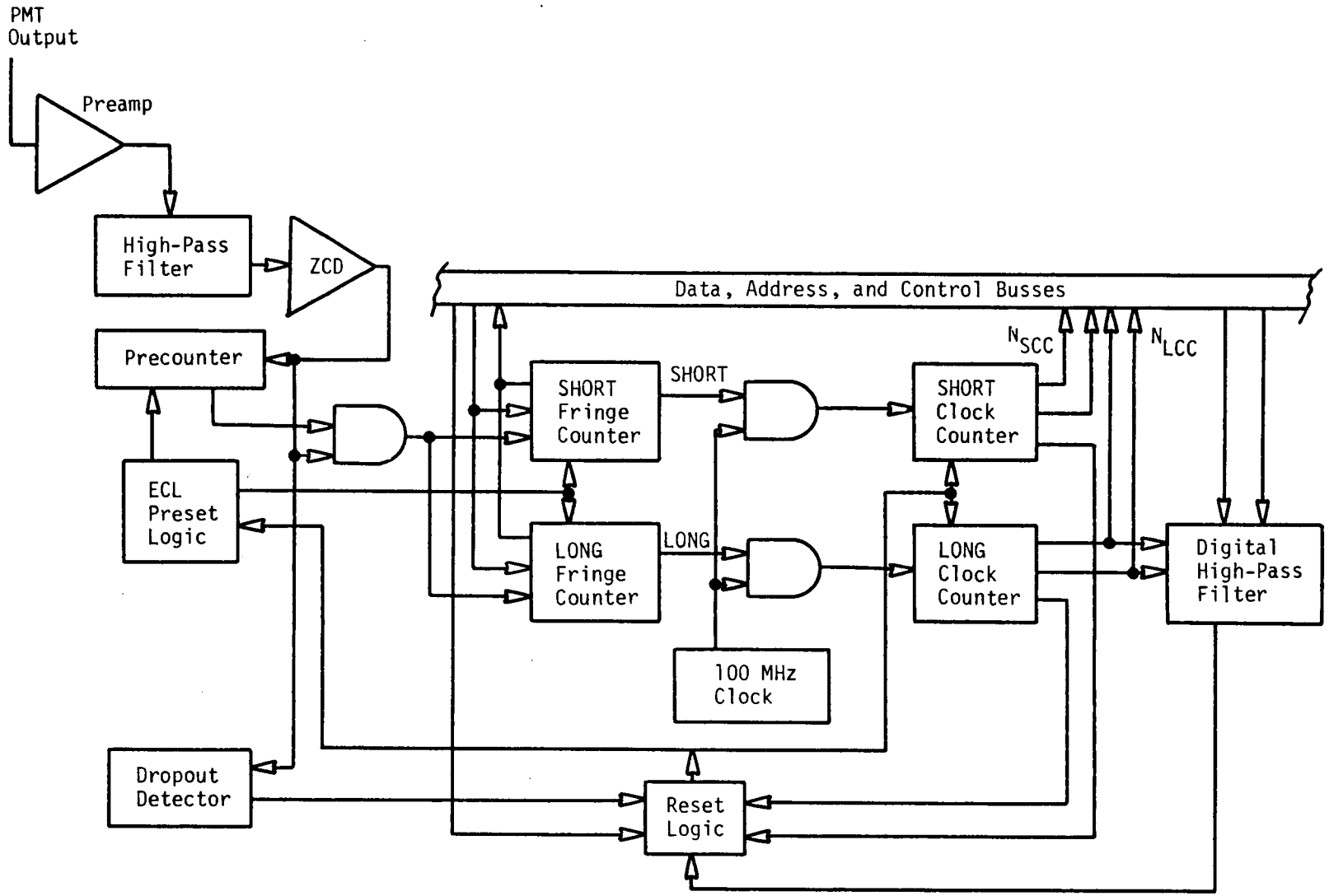


Figure 5. Complete block diagram of LV processor.

CHAPTER III

SIGNAL VALIDATION CIRCUITRY DESIGN

It can be shown that during each velocity measurement, the dropout detector requires the ZCD output to fulfill the condition given by

$$\tau_N - 3T_{HIGH_N} < \sum_{i=1}^{N-1} (3T_{HIGH_i} - \tau_i) \qquad (5)$$

where T_{HIGH_i} is the pulse width of the ith ZCD pulse, τ_i is the period (pulse width plus time to next pulse) of the ith cycle of the ZCD output, and τ_N and T_{HIGH_N} correspond to the ZCD output pulse presently being processed (see Figure 3, page 9). Should the Nth cycle of the ZCD output fail to satisfy the condition set forth in Equation 5, the dropout detector would reset the LV processor. Careful examination of Equation 5 reveals two major reasons why it is not a good measure of a signal's aperiodicity. The criterion on which the signal is tested ($\sum_{i=1}^{N-1} (3T_{HIGH_i} - \tau_i)$) becomes decreasingly selective as N increases. Also, the severity of the test is a function of the ZCD output pulse width, T_{HIGH} (which is a function of the ZCD threshold setting). As T_{HIGH} gets larger, the test becomes less stringent.

A better approach is to compare the cycle of the ZCD output presently being processed (the cycle with index N) to the cycle of the ZCD output that directly preceded it (the cycle with index (N-1)). The SVC performs such a test. As a velocity measurement is being made, the SVC tests the ZCD output to ensure that it satisfies the following relation:

$$\frac{\tau_{N-1}}{\alpha} \leq \tau_N < \alpha\tau_{N-1} \qquad (6)$$

where τ_N is the period of the cycle of the ZCD output presently being processed, τ_{N-1} is the period of the previous cycle of the ZCD output, and α is a real constant greater than unity. The aperiodicity test given by Equation 6 was implemented through the block diagram shown in Figure 6. Period timers A and B measure the period of alternate cycles of the ZCD output by counting a high-frequency clock. Multiplication by α is done in hardware for maximum speed. The comparators were also designed for minimum delay from input to output. Output generating logic decodes the comparator's outputs along with certain LV processor control signals and sends a restart pulse to the LV processor if the ZCD output fails to satisfy Equation 6 at any point during a measurement. The SVC is interconnected to the LV processor via the processor's 50-pin bus and the microcomputer's S-100 bus.

Operation of the SVC is outlined by the flowchart shown in Figure 7. The SVC is activated at the point in the LV processor's data acquisition cycle when the precount has just been completed; the velocity measurement is started on the next rising edge of the ZCD's output. When the ZCD generates this rising edge, SHORT goes true, indicating that the LV processor is attempting a measurement. The rising edge of SHORT arms the output generating logic, enabling it to reset the processor. Timers A and B alternately accumulate and hold counts proportional to the period of the cycle of the ZCD output presently being processed. Each cycle of ZCD is timed and tested until either the measurement is completed or the processor is reset.

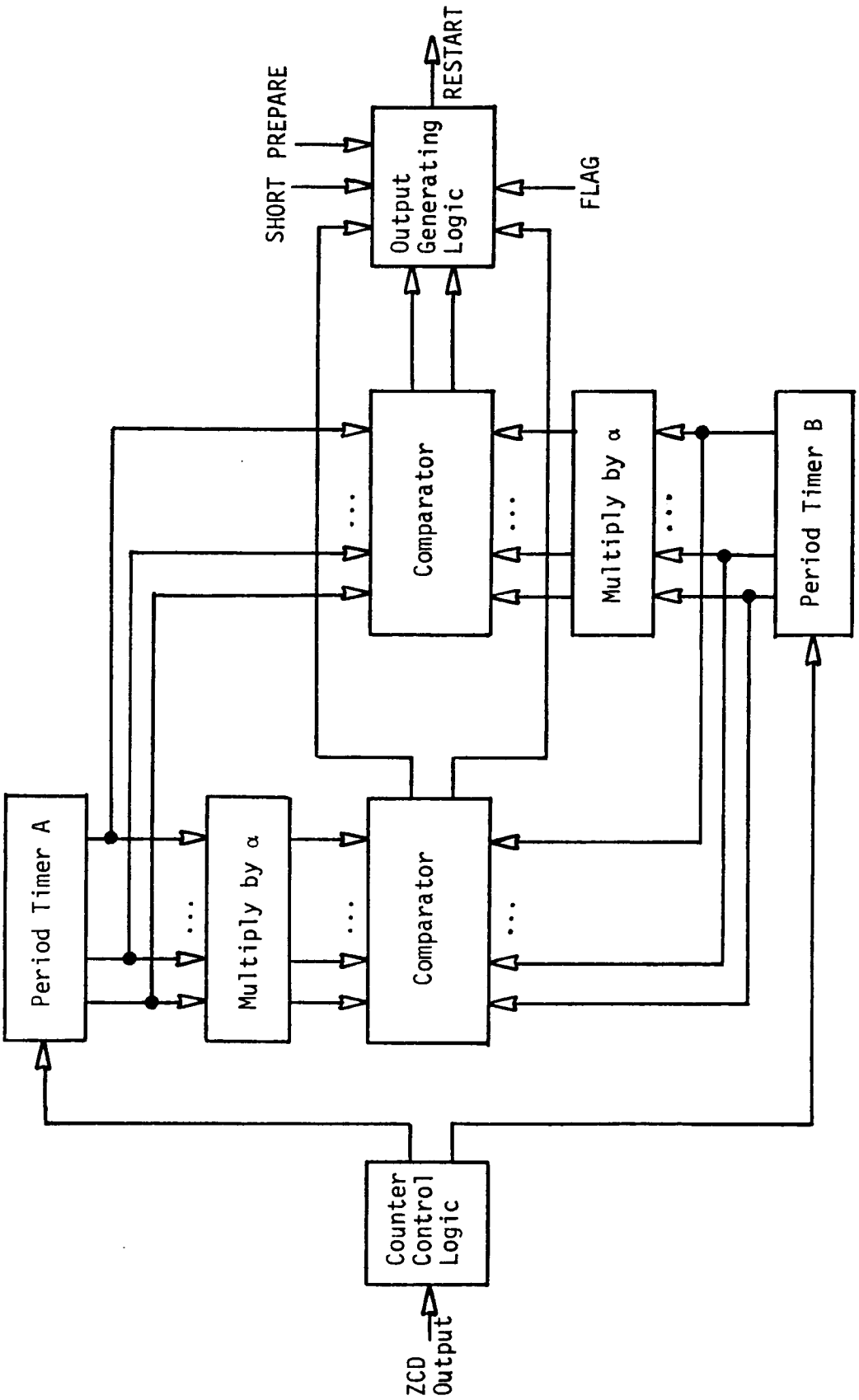


Figure 6. SVC block diagram.

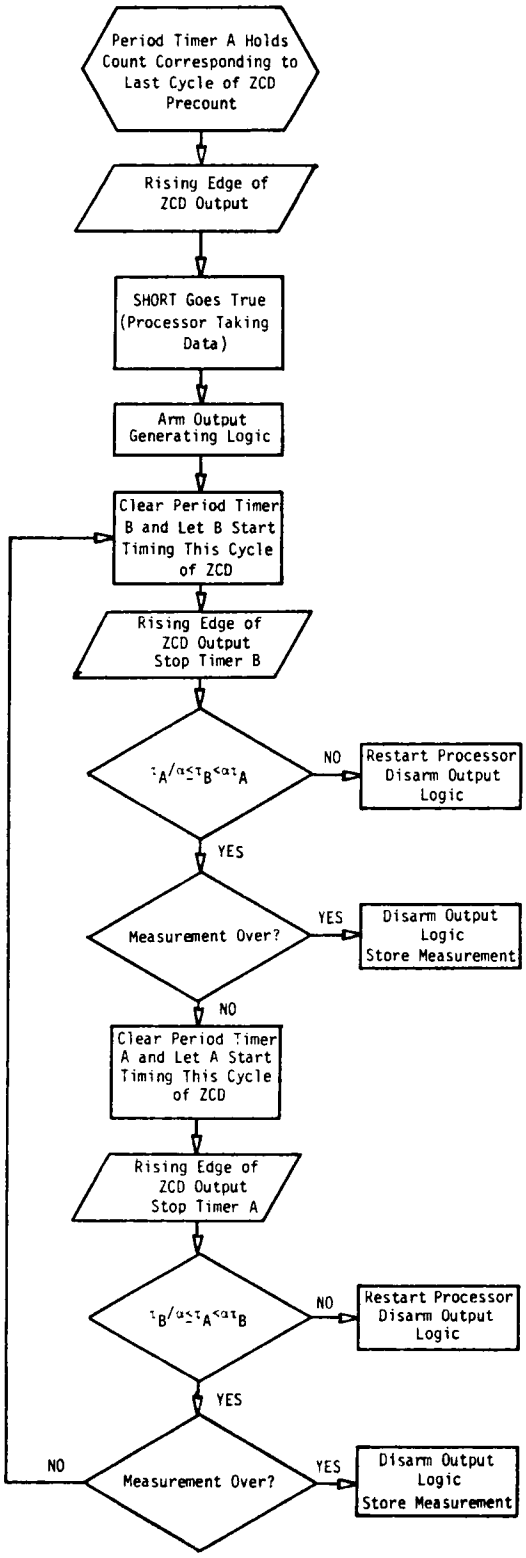


Figure 7. SVC flow diagram.

ZCD Period Timer

The period of each cycle of the ZCD's output is timed by binary counters which count a high-frequency clock during each cycle of the ZCD's output. The operation of the period timer is similar to that of the clock counters discussed in Chapter II, except that the period timer only counts for one cycle of the ZCD output instead of N_L cycles. The ZCD period timer can be divided into four major blocks as shown in Figure 8: the ZCD synchronizer circuit, the counter control log, and two binary counter circuits (period timers A and B). The counter control logic resets a period timer and then gates the high-frequency clock to the timer during each period of the ZCD output. Since the counter control logic generates control signals based on the ZCD output, the ZCD synchronizer circuit is required to synchronize the ZCD output with the clock to prevent uncertainty in period timing caused by simultaneous transitions in the ZCD output and the clock. Further considerations in the design of each of these blocks will be discussed later in this section.

The complete schematic diagram of the ZCD period timer is shown in Figure 9. IC 1 receives the ZCD's differential, ECL-level output, and IC 2 converts it to a single-ended, TTL-level signal. The period timer's high-frequency clock signal is generated by the crystal controlled oscillator circuit containing IC 25. Depending on the frequency of its input, the ZCD synchronizer circuit (composed of IC 3 through IC 5) functions in one of two modes as shown in Figure 10. When the frequency of the ZCD output is less tha 10 MHz (the clock

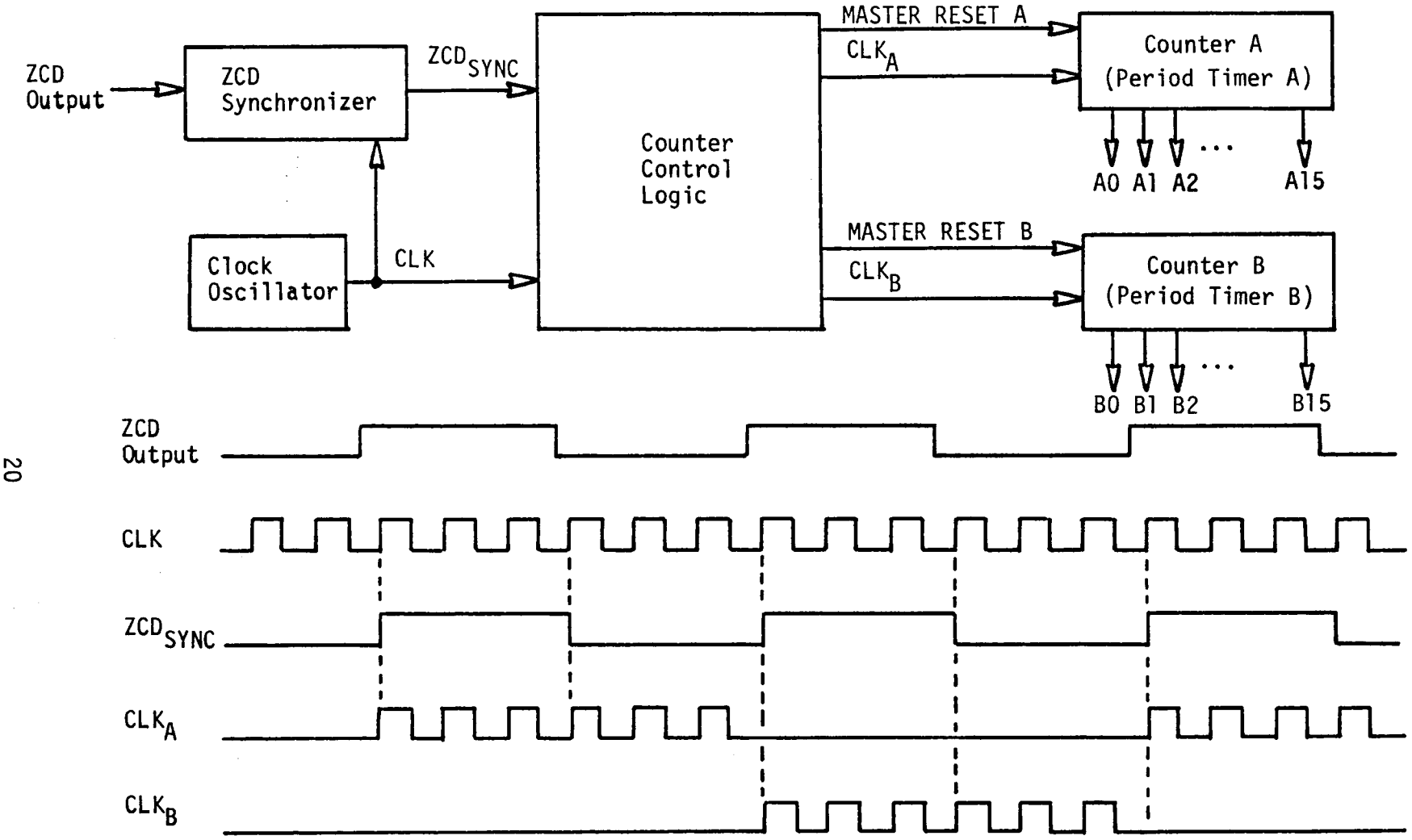


Figure 8. Period timer block diagram.

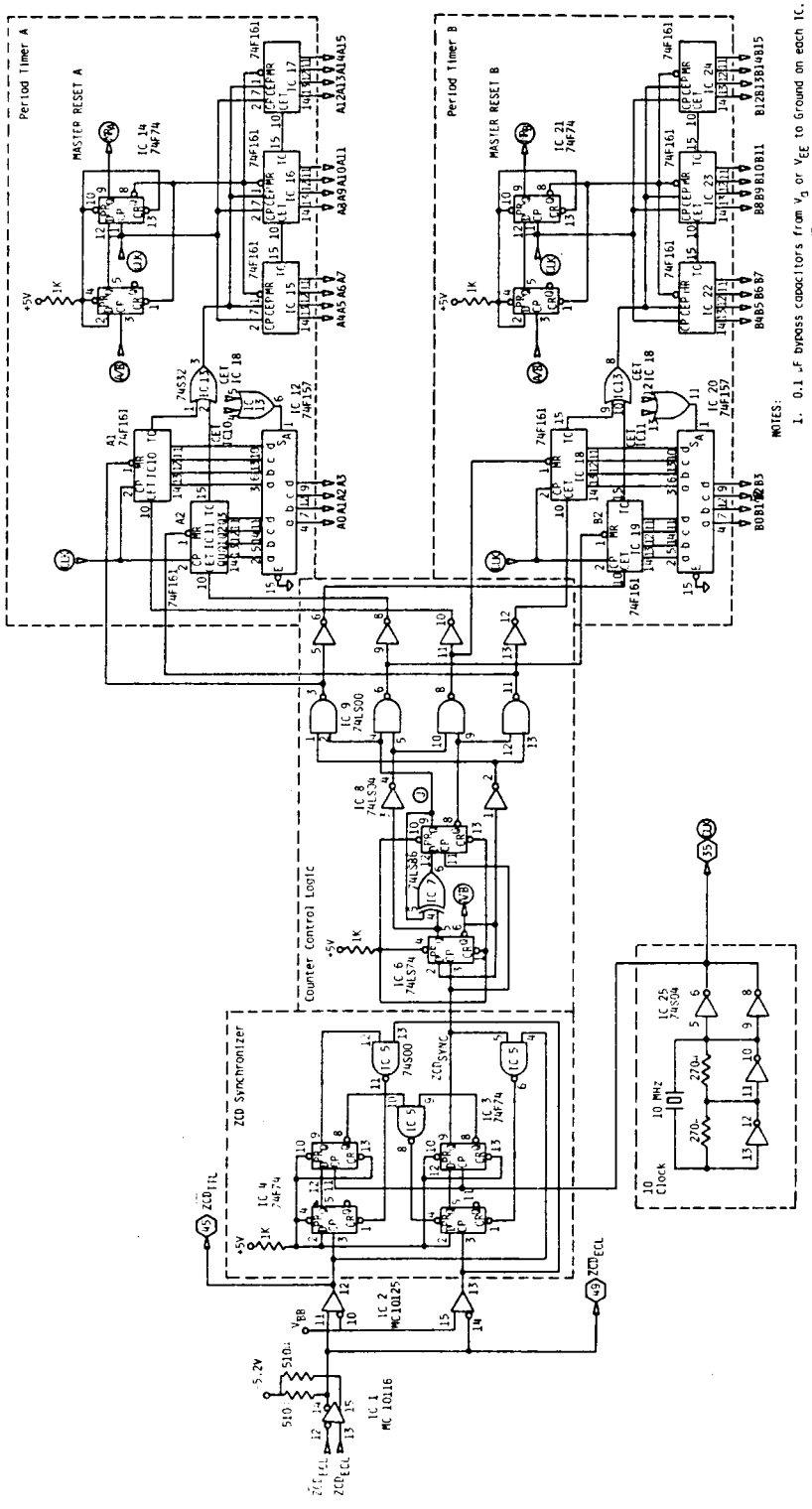
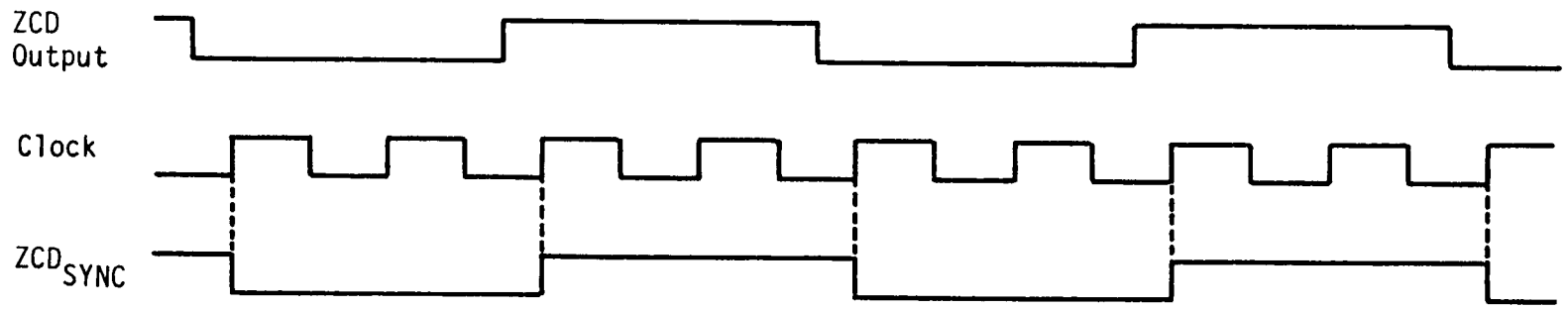
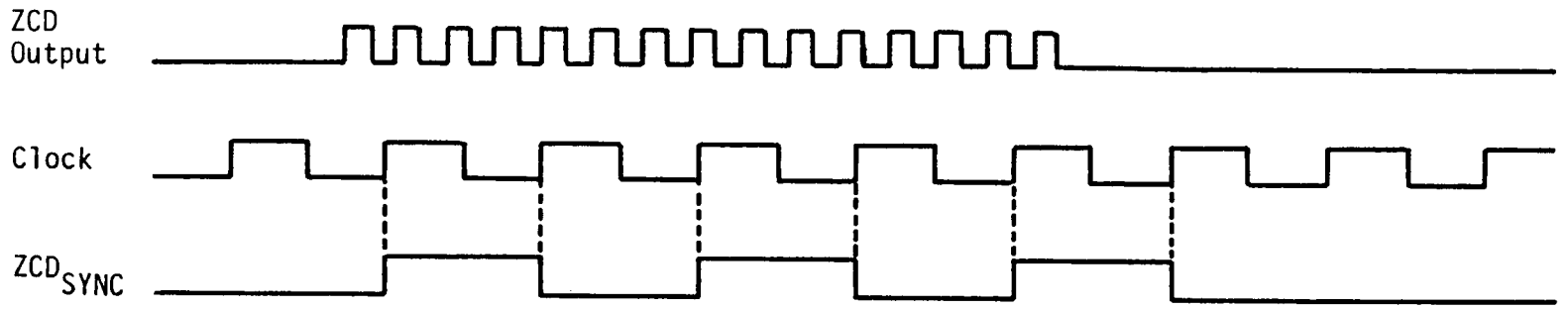


Figure 9. ZCD period timer schematic diagram.



(a) ZCD output frequency less than clock frequency.



(b) ZCD output frequency greater than clock frequency.

Figure 10. ZCD synchronizer timing diagram.

frequency), the ZCD synchronizer synchronizes both the rising and falling edges of the ZCD output with the rising edges of the 10 MHz clock signal (as shown in Figure 10a). In this case, the SVC is in the mode of operation shown in Figure 7. Since the resolution of the period measurement is limited by the clock frequency, the period timer is unable to supply enough information to support the test of Equation 6 when the frequency of the ZCD output exceeds 10 MHz. In order to prevent erroneous operation of the period timer caused by a ZCD output frequency greater than 10 MHz, the ZCD synchronizer detects multiple state changes in the ZCD output that occur less than one clock period apart. These multiple state changes are saved in the ZCD synchronizer and determine the state of ZCD_{SYNC} on successive rising edges of the clock signal as shown in Figure 10b. Therefore, any ZCD output frequency greater than the 10 MHz clock frequency results in a 5 MHz ZCD_{SYNC} signal which corresponds to two clock counts per cycle in the ZCD period timers. If the period timer does not contain more than two counts, then the frequency of the ZCD output was too high for the SVC to process; consequently, the SVC's output is disarmed.

The period timer outputs, A0 through A15 and B0 through B15, appear to the rest of the SVC as the outputs of a pair of binary counters that can be cleared and count enabled instantaneously. The operation of the period timers (shown in Figure 8) is illustrated by the timing diagram of Figure 11. Each counter counts up from zero for one period of ZCD_{SYNC} and holds that count for the next period of ZCD_{SYNC}. It is then cleared and counts up again. Thus, the period timers count and hold on alternate periods of ZCD_{SYNC} so that Equation 6 can be implemented.

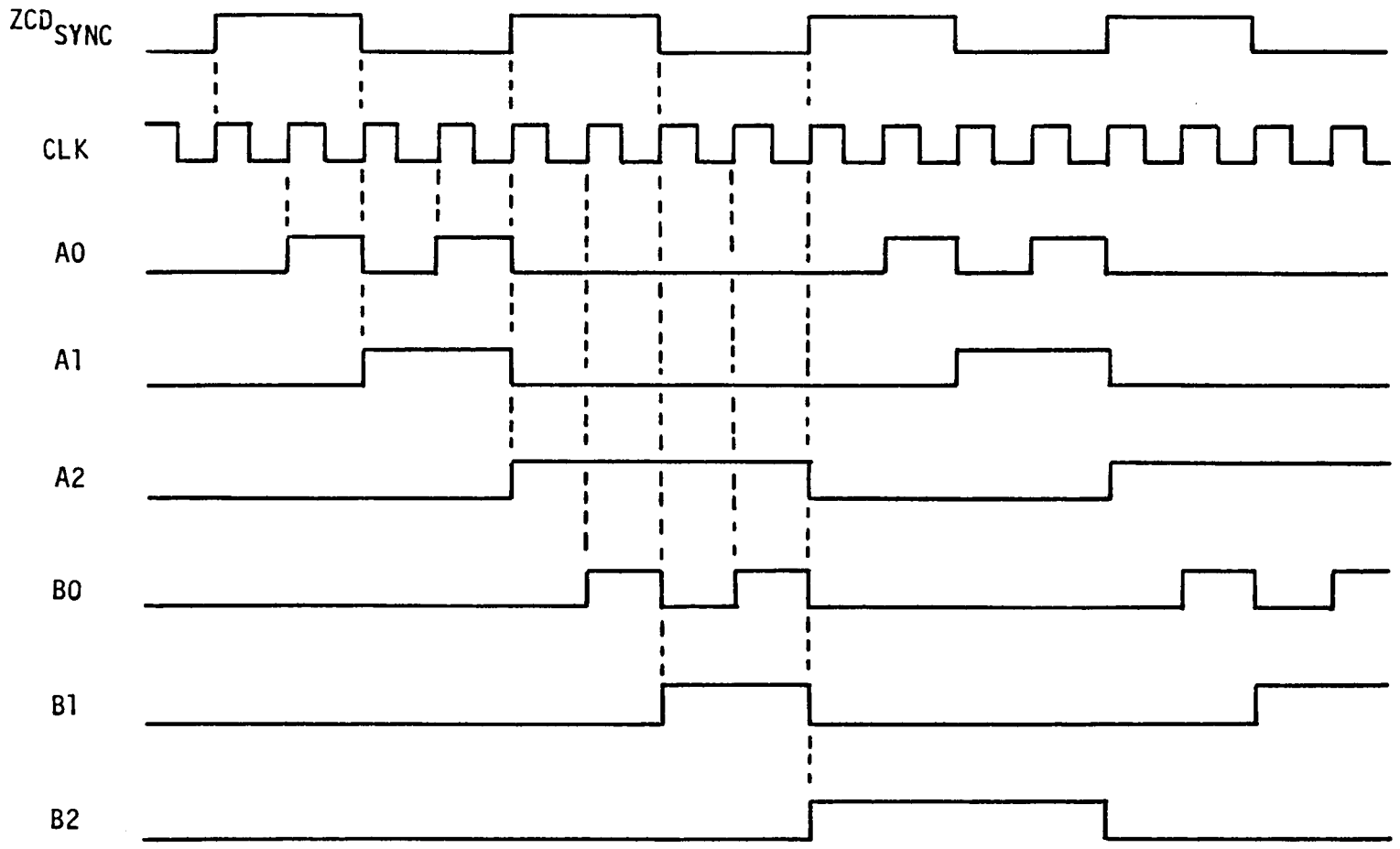


Figure 11. Timing diagram for period timers shown in Figure 8. Counter outputs A3 through A15 and B3 through B15 are always low for this example.

The primary concern in the design of the period timer blocks shown in Figure 8 was that the amount of time required to clear the counters would cause the counters to miss clock cycles at the beginning of a cycle of ZCD_{SYNC}. Should the counters not recover from being cleared quickly enough, the final count they contain will be erroneously low. This problem was alleviated by using two counters (IC 10 and IC 11) to generate the lower four bits of a period timer. Each of these counters is capable of generating the lower four bits for the period timer and a multiplexer (IC 12) is used to select the appropriate counter's outputs. In this manner, one counter is always cleared and ready to count so that the only delay from resetting to restarting a period timer is the 10 ns required by the multiplexer (IC 12) to select the correct counter [7]. Since the upper bits of a period timer are not active until after the lower four bits have overflowed, the upper bits are cleared by $\overline{\text{Master Reset A}}$ or $\overline{\text{Master Reset B}}$ on the first clock pulse counted by the first stage.

The counter control logic generates the control signals that enable and clear the period timing counters. The timing diagram shown in Figure 12 depicts typical operation of the counter control logic. Period timers A and B are alternately selected by signal $A/\overline{B}$ to time the period of ZCD_{SYNC}. Signals $A/\overline{B}$ and J (labeled on Figure 9) are decoded to yield the CET (count enable) and $\overline{MR}$ (master reset) control signals for counters A1, A2, B1, and B2. Counters A1 (IC 10) and A2 (IC 11) generate the lower four bits of period timer A, while counters B1 (IC 18) and B2 (IC 19) generate the lower four bits of period timer B. When the CET signal is high, the counter is enabled to count; if

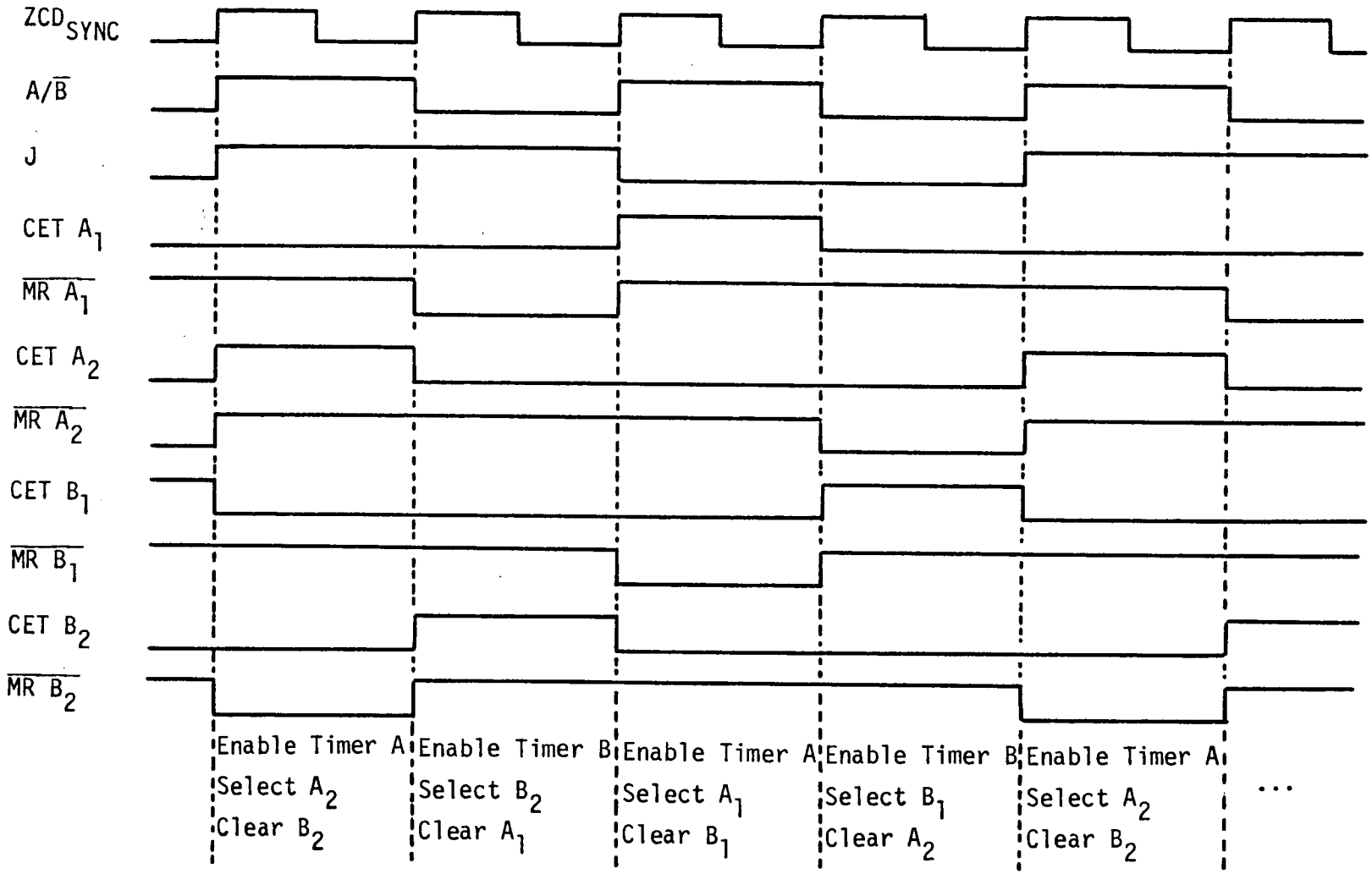


Figure 12. Counter control logic timing diagram.

it is low, the counter holds. Whenever the $\overline{MR}$ signal goes low, it resets the counter to zero.

Period Multiplication and Comparison

Once the period timers have measured the period of a cycle of the ZCD output, multiplication by α and magnitude comparison are performed. Obtaining a minimum propagation delay was the major concern in the design of the circuits that perform the multiplications and comparisons shown in the block diagram of Figure 6, page 17. The propagation delay had to be minimized so that the SVC's maximum input frequency would be maximized.

The flowchart of Figure 7, page 18, indicates that each cycle of ZCD_{SYNC} is tested according to Equation 6 on the rising edge of the following cycle of ZCD_{SYNC}. The rising edges of ZCD_{SYNC} are synchronized with the rising edges of the clock. Since the period timers change state on the rising edge of the clock, the outputs of the multipliers and comparators must settle to their final values before the next rising edge of the clock. Therefore, the multiplication by α and the comparison shown in Figure 6, page 17, must be performed in a length of time less than the period of the clock so that the comparators' outputs are not read while they are in a transient state. Thus, the minimum allowable clock period is equal to the sum of the settling times of the counters, multiplexers, and comparators. This minimum allowable clock period determines the maximum ZCD_{SYNC} frequency that can be measured by the ZCD period timers (i.e., the upper limit of the SVC's frequency response).

Since available 16-bit binary adder circuits are faster than available 16-bit binary multiplier circuits, the multiplication by α was performed by left-shifting the number to be multiplied by α and then adding the left-shifted number and the original number to give the product. This algorithm greatly increases the speed of the multiplication; however, the values of α are now limited to 1.5, 1.25, 1.125, 1.0625, and so on. The inherent quantitization error of the period timing counters (plus or minus one count) coupled with the round off error in the multiplication require that a minimum count, equal to $2/(\alpha - 1)$, be reached for error-free operation. The SVC's output is, therefore, disabled unless the minimum count is reached. The highest input frequency the SVC can test, F_{MAX}, can be written as

$$F_{MAX} = \frac{(\alpha - 1)F_{CLK}}{2} \tag{7}$$

where F_{CLK} is the frequency of the SVC's clock. For example, an α of 1.5 and a clock frequency of 10 MHz correspond to an F_{MAX} of 2.5 MHz.

Figure 13 is the schematic diagram of the circuitry that performs the period multiplication and comparison. IC 27 through IC 30 and IC 36 through IC 39 are the binary adders that perform the multiplication by α. The inputs labeled MA0 through MA15 and MB0 through MB15 are the left-shifted versions of A0 through A15 and B0 through B15, respectively. The comparison is performed by IC 31 through IC 35 and IC 40 through IC 44. Through the use of 4:1 multiplexers and a dip switch, α is selectable to 1.5, 1.25, 1.125, or 1.0625. The schematic diagram of the α select circuitry is shown in Figure 14.

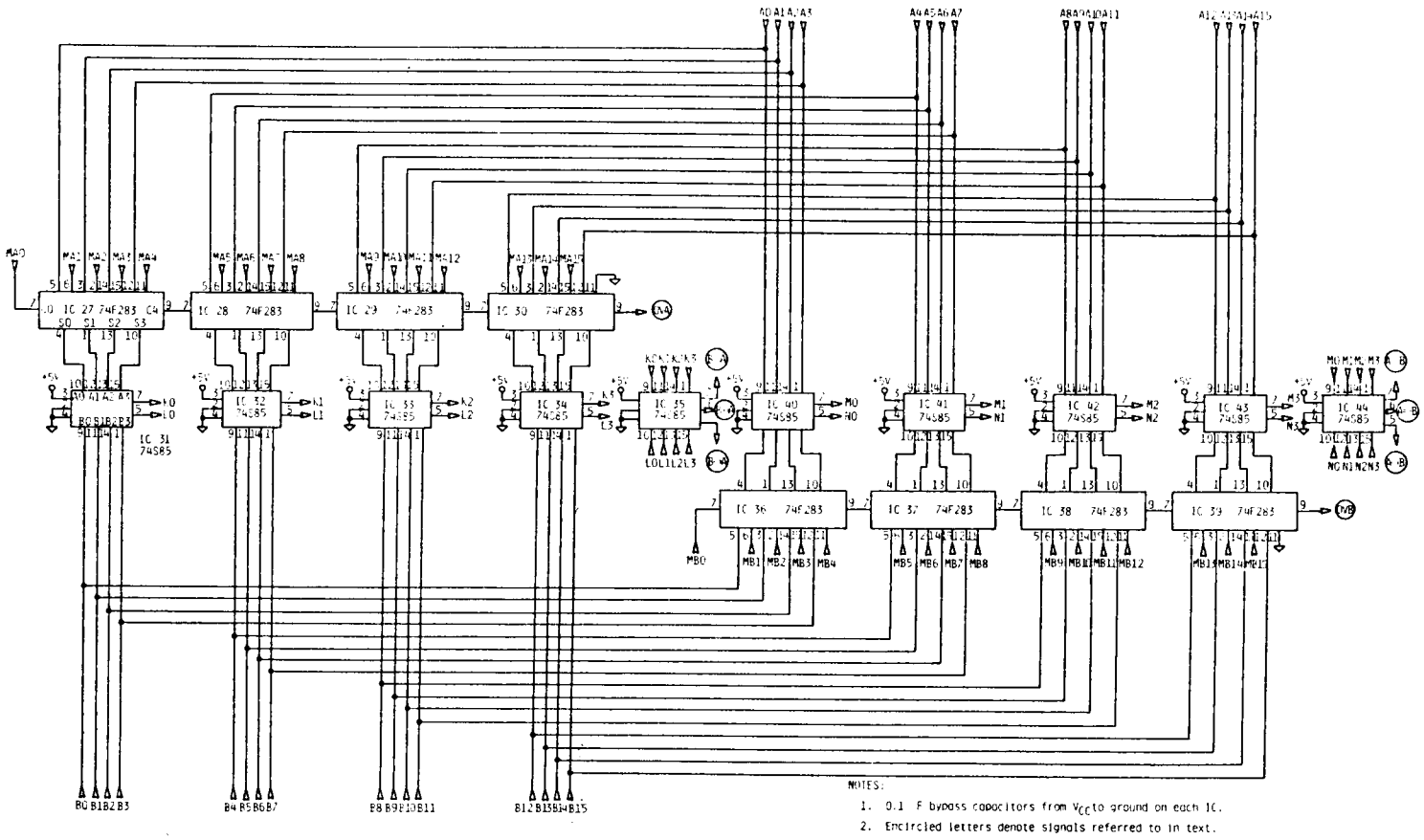
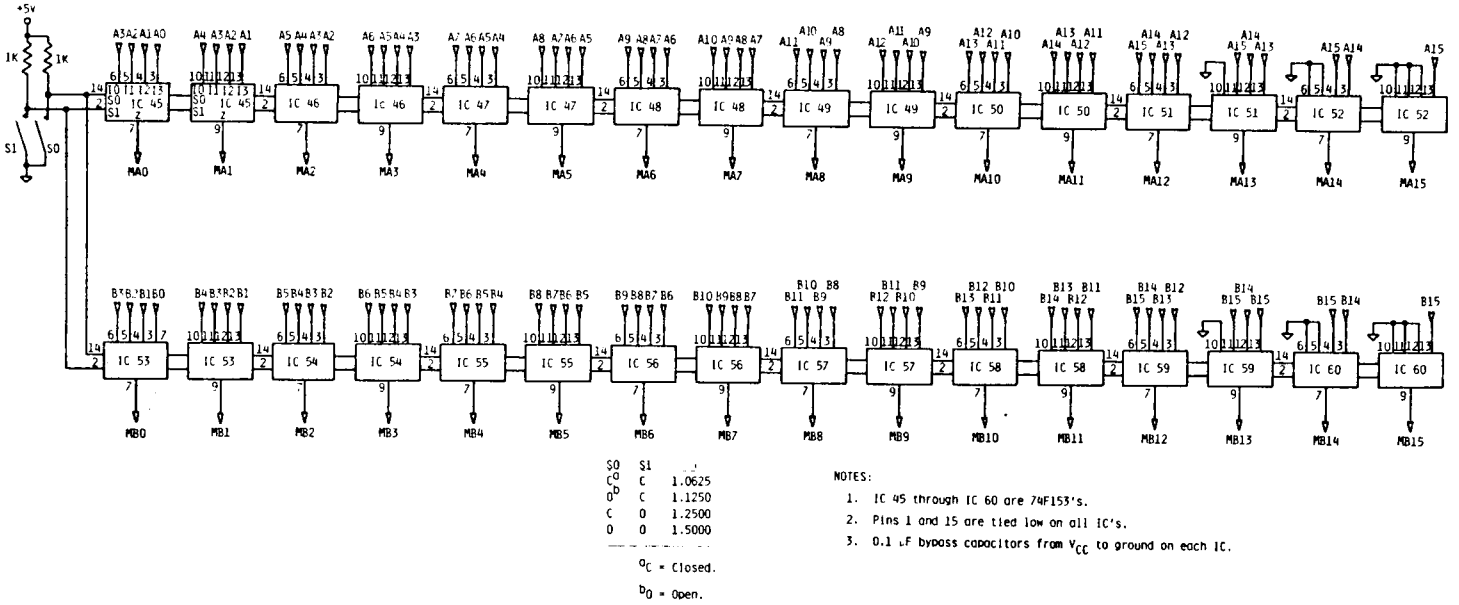


Figure 13. ZCD period comparator schematic diagram.



S0	S1	
C[a]	C	1.0625
C[a]	C	1.1250
C	0	1.2500
0	0	1.5000

[a]C = Closed.

[b]0 = Open.

NOTES:

1. IC 45 through IC 60 are 74F153's.
2. Pins 1 and 15 are tied low on all IC's.
3. 0.1 µF bypass capacitors from V_{CC} to ground on each IC.

Figure 14. Range select logic schematic diagram.

Output Generating Logic

The output generating logic shown in Figure 15 decodes the comparators' outputs as well as the LV processors' control lines to determine if the ZCD's output fails to satisfy Equation 6 in the course of a velocity measurement. If the minimum count was reached by the period timers, the result of applying Equation 6 (signal $\overline{\text{AFAIL}}$) is latched into IC 65 on the rising edge of ZCD_{SYNC}. If $\overline{\text{AFAIL}}$ makes a one to zero transition while the output is enabled (TST is high), then IC 68 fires a 150 ns wide $\overline{\text{RESTART}}$ pulse to the LV processor. The output is enabled when SHORT goes high (indicating that a measurement is in progress) and is disabled when FLAG goes high (indicating the end of a measurement) or when $\overline{\text{PREPARE}}$ goes low (indicating that the LV processor has been reset).

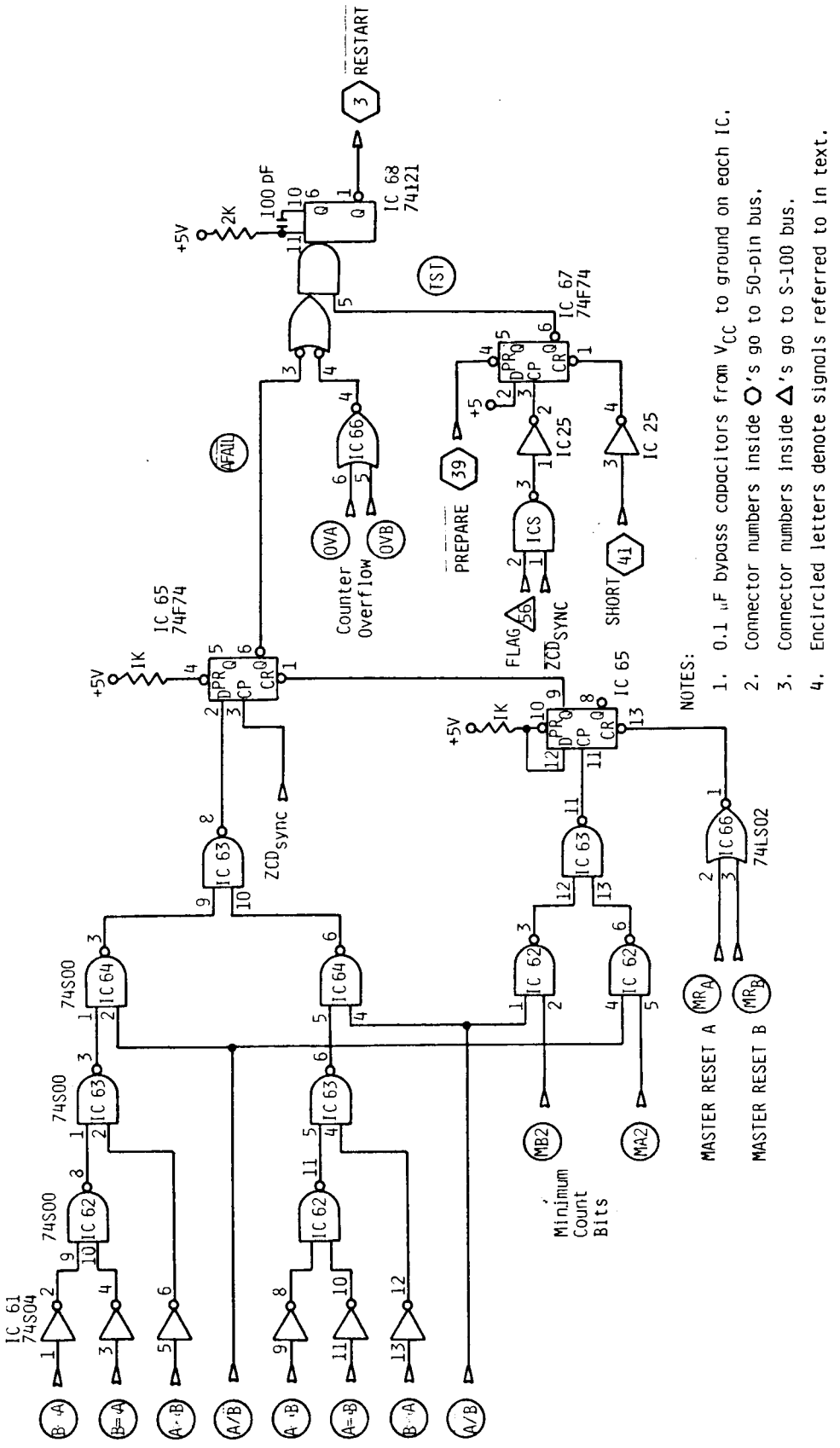


Figure 15. Output generating logic schematic diagram.

CHAPTER IV

PROCESSING OF LV SIGNALS

A comparison of the performances of the LV processor with and without the SVC installed was made to verify the SVC's operation. In order to make such a comparison, a controlled and repeatable source of LV signals was required. Since flow conditions (velocity, turbulence, and seeding) are difficult to control, a method to electronically simulate the high-pass filtered PMT output was devised. The circuit which generates the simulated LV signals is described in the Appendix. To generate a more realistic signal, various amounts of white noise (bandlimited to 5 MHz) were added to the simulated LV signal by means of a resistive adder network.

Processing of Simulated Signals

The simulated noisy LV signal was processed by the LV processor with and without the SVC installed. Measurements consisting of 5000 points each were taken for various signal-to-noise ratios and turbulence intensities. The turbulence intensity (TI) of a measurement is defined as:

$$TI = \sigma/\overline{V} \tag{8}$$

where $\overline{V}$ is the mean velocity of the distribution and σ is the standard deviation [9]. The mean signal frequency (velocity) was constant at 100 kHz for all measurements. The LV processor was set up for a LONG count of 8, a SHORT count of 5, and a PRECOUNT of 1. This fringe count was chosen so that the processor would only be able to complete

a single velocity measurement on a burst. α was set equal to 1.0625 to provide the most stringent test possible without exceeding the upper limit of the SVC's frequency response. The digital high-pass filter was disabled so that the only data rejected during acquisition was rejected by either the SVC or the dropout detector depending on which was in place. During data reduction, the maximum allowed aperiodicity error was 2 percent. The percentages of data points passing the aperiodicity test (percentage accepted) for each method of hardware signal validation (dropout detector and SVC) are plotted in Figure 16.

From Figure 16 it can be seen that there is very little difference in percentage accepted for data points processed with S/N above 20 dB. However, when S/N falls below 20 dB, the percentage of data points accepted is consistently higher when the SVC was in use. Based on processing artificial signals, it is concluded that the SVC improves the LV processor's acceptance ratio in low S/N environments.

Processing of Real LV Signals

The previous data illustrates the SVC's ability to enhance data acquisition by a pronounced improvement in acceptance ratio for low S/N signals. Since the test was made by processing artificial signals and white noise, conclusions concerning the processor's performance when processing real signals must be carefully drawn based on those results. In order to determine if the SVC causes any significant gain in the percentage of data points accepted when processing real signals, another experiment was required. In this experiment the

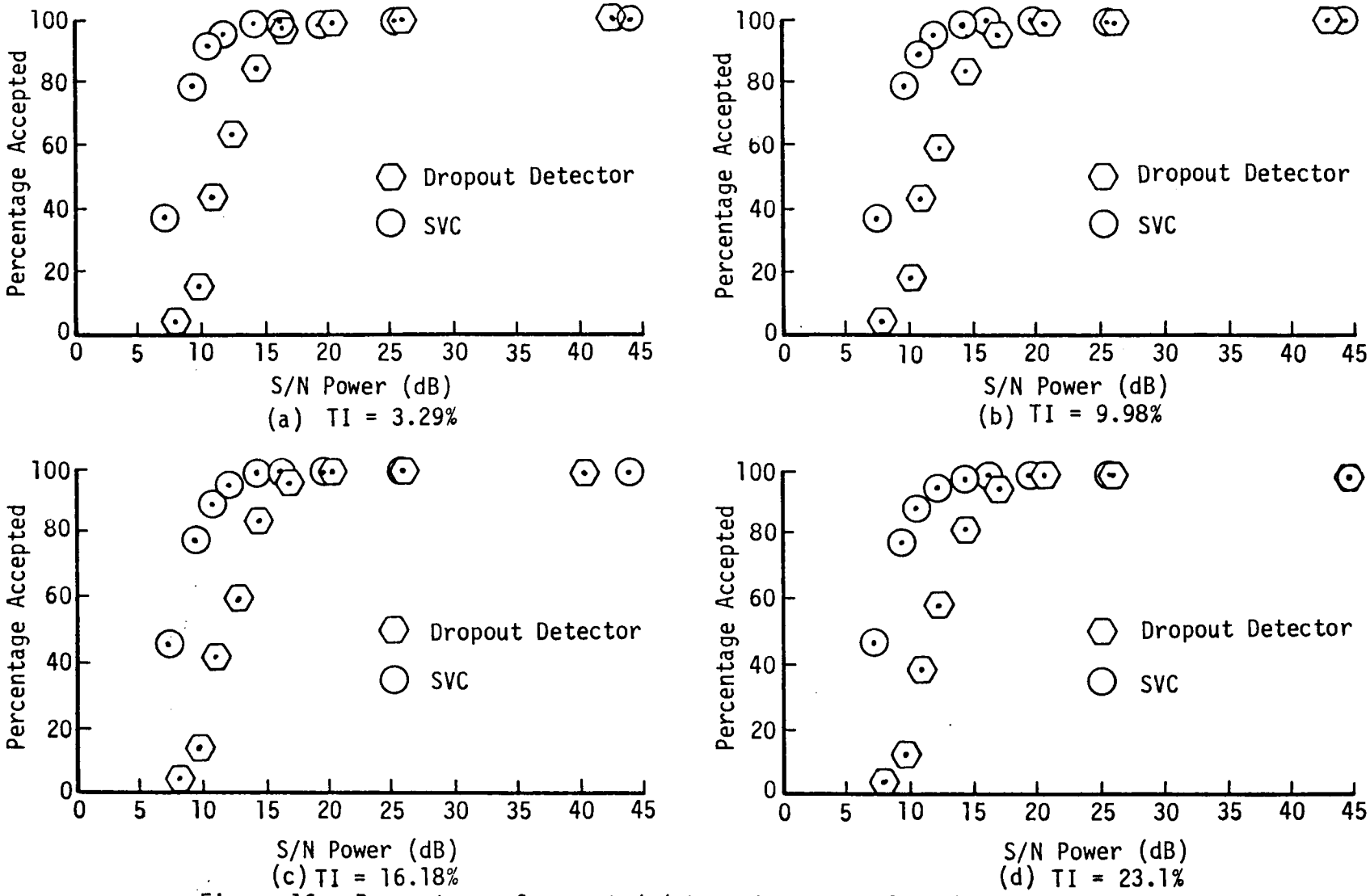


Figure 16. Percentage of accepted data points as a function of S/N.

signals were generated by an LV using a Bragg-diffracted, dual-beam optical system with an argon ion laser. A photomultiplier tube collected the backscattered light approximately 15° off axis.

A small fan was placed in a laminar flow as a turbulence generator, and a series of velocity measurements were made at three test points in the flow. Four measurements of 5000 points each were made at each test point. In two of the measurements the dropout detector was in place, while in the other two, the SVC was used. For each configuration of the LV processor, one measurement was made with the laser operating at 500 mW (giving high S/N), while the other measurement was made with 50 mW of laser power (corresponding to a lower S/N). Since equipment necessary to determine the signal-to-noise ratio of a real LV signal was not available, the actual S/N's of the signals processed in this experiment were not known. The processor's operating parameters (LONG count, SHORT count, etc.) were the same as in the experiment with artificial signals.

Data resulting from the experiment are presented in Table 1. As in the experiment with artificial signals, the percentage accepted is consistently higher for the SVC. At the high S/N value, the SVC acquired 9.95 percent more data points (on the average) that passed the 2 percent periodicity test than did the dropout detector. At low S/N, an average of 62.17 percent more points passed the aperiodicity test when acquired by the SVC. As in the earlier experiment, the SVC gives the greatest gain in earlier experiment, the SVC gives the greatest gain in percentage accepted in low S/N conditions. It is also interesting to note that the measured values of mean frequency and TI at low

Table 1. Comparison of SVC and Dropout Detector When Processing Real Signals with Reduced S/N.

Test Point	Hardware	Mean Frequency (kHz)		TI (%)		Percentage Accepted	
		High S/N	Low S/N	High S/N	Low S/N	High S/N	Low S/N
1	DOD	102.171	106.142	1.094	12.258	87.02	28.46
	SVC	101.625	100.943	0.905	1.072	93.18	82.30
2	DOD	113.204	117.402	6.817	14.505	84.52	34.38
	SVC	111.945	112.166	6.805	7.347	94.84	92.12
3	DOD	73.437	89.780	11.677	27.346	80.64	15.30
	SVC	75.053	76.943	11.641	13.215	94.36	90.24

S/N tend to be closer to the true (high S/N) values when measured with the SVC.

CHAPTER V

SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

A signal validation criterion was established and hardware was developed to implement it in real time. This hardware was integrated into an existing LV processor and two experiments were performed to verify operation and to compare it to another method of hardware signal validation. The first experiment consisted of processing simulated LV signals at various signal-to-noise ratios and comparing the resulting data. In the second experiment, similar measurements were made on real LV signals.

In both experiments the data acquired by the SVC consistently had a higher percentage acceptance than the data acquired by the dropout detector. A pronounced improvement in data acceptance was shown by the SVC when processing low S/N inputs. In addition, the data generated by the SVC appear to be closer to the correct values.

The SVC's greatest limitation is its high-frequency response. With a system clock of 10 MHz, the SVC's high-frequency cutoff (F_{MAX}) ranges from 312.5 kHz for α = 1.0625 to 2.5 MHz for α = 1.5. Since F is directly proportional to the SVC's system clock, the SVC's frequency response could be improved by using a higher clock frequency. However, in order to make any significant improvement in the frequency response, the clock frequency would have to be raised so high as to necessitate a redesign of the SVC using a faster logic family (possibly ECL).

LIST OF REFERENCES

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1. Durrani, T. S., and C. A. Greated. Laser Systems in Flow Measurement. New York: Plenum Press, 1977.

2. Buchhave, P. "The Measurement of Turbulence with the Burst-Type Laser Doppler Anemometer--Errors and Correction Methods." Ph.D. Dissertation, State University of New York at Buffalo, 1979.

3. Morris, R. D. "Design of a High-Frequency, Programmable, Laser Velocimeter Signal Processor." M.S. Thesis, University of Tennessee at Knoxville, 1978.

4. Durst, F., A. Melling, and J. H. Whitelaw. Principles and Practice of Laser-Doppler Anemometry. New York: Academic Press, 1976.

5. Kalb, H. T., D. B. Brayton, and J. A. McClure. "Laser Velocimetry Data Processing," AEDC-TR-78-116, Arnold Air Force Station, Tullahoma, Tennessee, September 1973.

6. Hornkohl, J. O. Unpublished notes, January 1984.

7. Fairchild Camera and Instruments Corporation. FAST Data Book. South Portland, Maine: Fairchild Camera and Instruments Corporation, 1982.

8. Pfeifer, H. J. "Advances in Digital Signal Processing," Laser Velocimetry and Particle Sizing (H. D. Thompson and W. H. Stevenson, eds.), pp. 67-78. New York: Hemisphere Publishing Corporation, 1979.

9. Cline, V. A., and H. T. Bentley, II. "Application of a Dual Beam Laser Velocimeter to Turbulent Flow Measurements," AEDC-TR-74-56, Arnold Air Force Station, Tullahoma, Tennessee, September 1974.

10. Durst, F. "Electronic Processing of Optical Anemometer Signals," The Accuracy of Flow Measurements by Laser Doppler Methods (Proceedings of the LDA-Symposium, Copenhagen, Denmark, 1975), pp. 208-250, 1976.

11. Hösel, W., and W. Rodi. "Errors Occurring in LDA--Measurements with Counter Signal Processing," The Accuracy of Flow Measurements by Laser Doppler Methods (Proceedings of the LDA-Symposium, Copenhagen, Denmark, 1975), pp. 251-257, 1976.

12. Peebles, P. Z. Probability, Random Variables, and Random Signal Processing. New York: McGraw-Hill Book Company, 1980.

APPENDIX

APPENDIX

GENERATION OF SIMULATED LV SIGNALS

In order to make fair comparisons between different methods of processing LV signals, a controlled and repeatable input to the LV processors is required. By electronically simulating the output of the PMT, the methods to be compared can process exactly the same signal, thereby eliminating uncertainties caused by nonrepeatable flows. Since the output of the PMT is high-pass filtered (to remove the pedestal) before it is input to the ZCD, the simulated LV signal must approximate only the periodic component of the LV signal. The signal used to model the periodic component consisted of constant-amplitude, sinusoidal bursts with a dead time, T_D, between bursts. Figure 17 illustrates a typical simulated LV signal train. The frequency of a burst, F_B, is fixed for the duration of the burst but varies from burst to burst. The duration of a burst is also variable and is always an integer number of cycles, N_C. T_D, F_B, and N_C are random variables whose probability density functions approximate those of real LV signals [1,12].

The probability density functions that characterize the simulated signal are shown in Figure 18. The probability density function of T_D is Gaussian with a mean of 200 μs and a standard deviation of 50 μs. The distribution of burst frequencies, F_B, is also Gaussian and has a mean of 100 kHz. The standard deviation of F_B was not fixed at a single value so that more than one turbulence intensity could be simulated. The probability density function of N_C consists of discrete

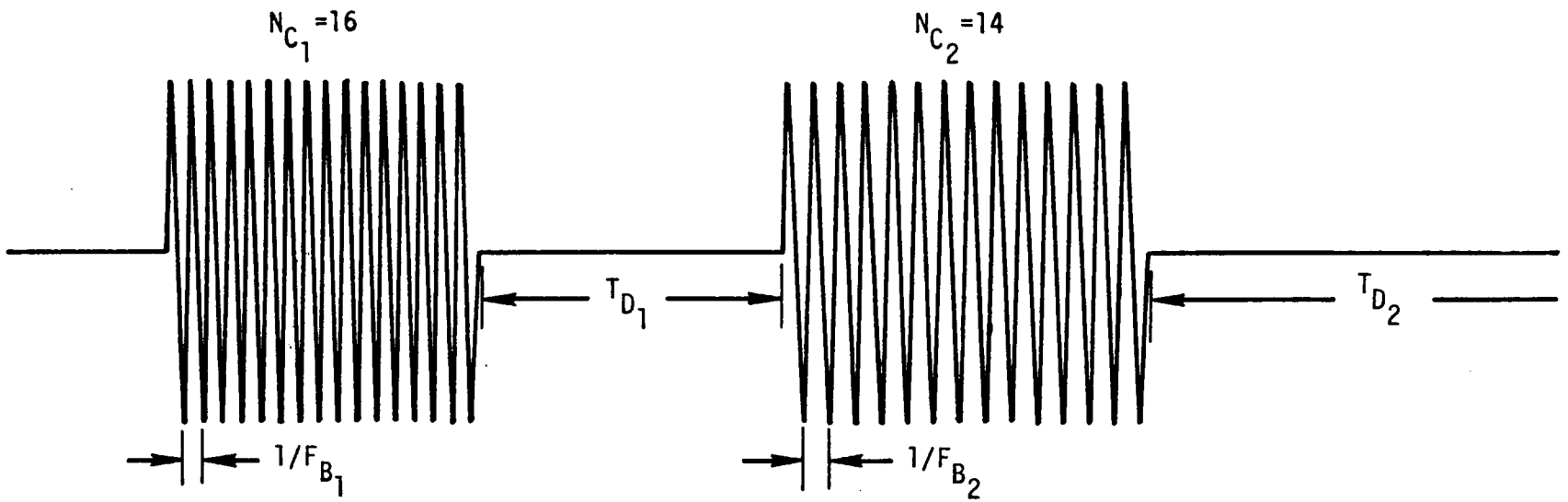
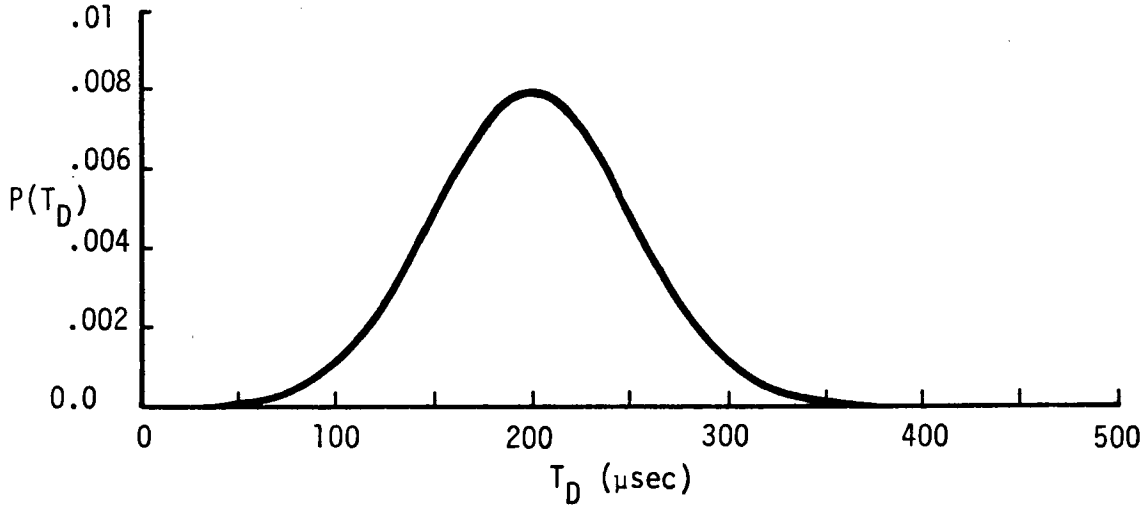
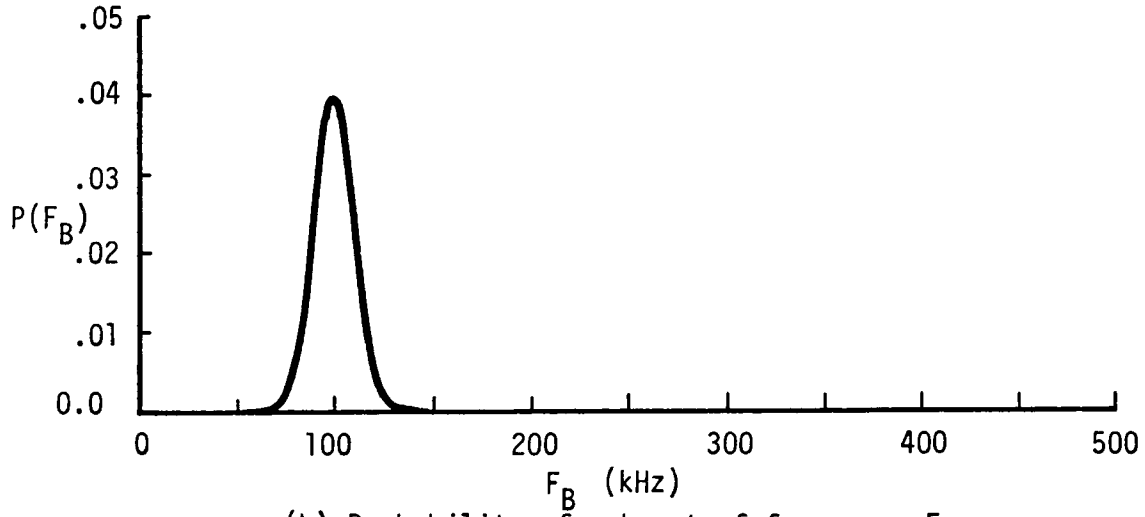


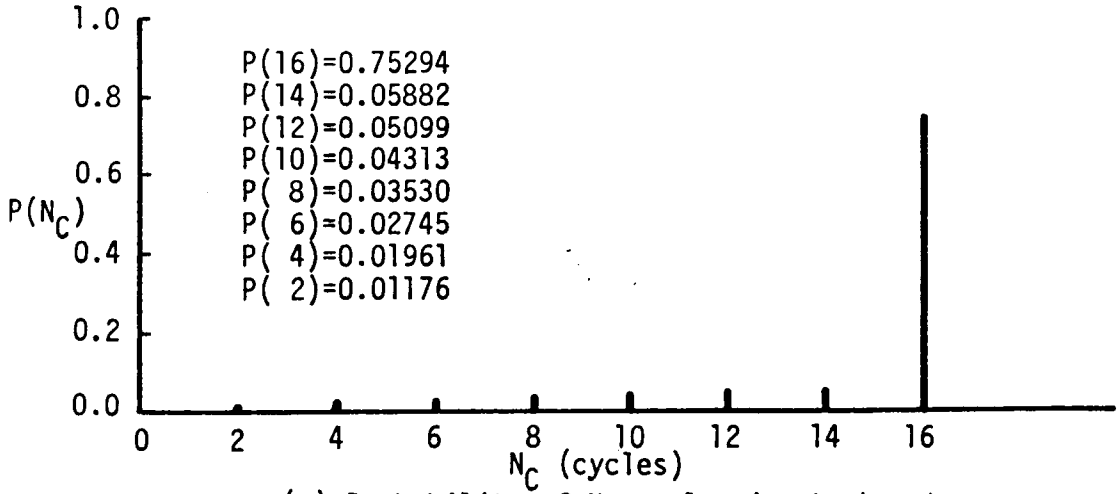
Figure 17. Typical simulated LV signal.



(a) Probability of T_D μsec between bursts.



(b) Probability of a burst of frequency F_B.



(c) Probability of N_C cycles in the burst.

Figure 18. Characteristic probability density functions of simulated LV signals.

integer values for N_C as shown in Figure 18c. Approximately 75 percent of the simulated signals consisted of 16 cycles, while the remaining 25 percent had less than 16 cycles. The distribution of Figure 18c was developed based on an ellipsoidal sample volume with a major axis of 800 μm, a minor axis of 200 μm, and 16 equally spaced interference fringes that are 12.5 μm apart. This distribution also implies that all particles will have trajectories normal to the fringe plane.

The LV signal was generated by a sweep generator that was controlled by external circuitry. This control circuitry gates and frequently modulates the sweep generator's output via its GATE and VCG inputs. The generator's output was turned on for a predetermined number of cycles, N_C, and then turned off for a predetermined dead time, T_D. The frequency of the generator's output during any given burst, F_B, was governed by a dc programming voltage applied to the generator's VCG input.

The signal control circuitry was programmed to generate the probability distributions illustrated in Figure 18. This was accomplished by making each characteristic of the signal (T_D,T_B, and N_C) presettable from a binary control word and then programming programmable read-only memories (proms) with tables of control words distributed according to Figure 18. For each burst output by the sweep generator, the following sequence of events takes place in the signal simulation circuitry. First, a control word is input to a digital-to-analog converter (DAC) which outputs a control voltage to the generator's VCG input to set the frequency of the burst to be generated, F_B.

At the same time, a presettable binary counter, the cycle counter, is preset to the one's complement of the number of cycles that are to appear in the next burst, N_C. Next, the generator is gated on with the cycle counter counting the number of cycles that are output by the generator. When the cycle counter reaches its terminal count (all ones), the generator is gated off and a programmable one-shot (presettable binary counter that counts a timing clock) determines how long the generator is to be gated off, T_D. After the one-shot "times out," a new control word is input to the DAC, the fringe counter and one-shot are preset to new values, and the sequence starts over again. The DAC, cycle counter, and the programmable one-shot receive their inputs from proms containing tables of binary numbers which correspond to the probability density functions of T_D, F_B, and N_C.

The complete schematic diagram of the signal simulation circuitry is shown in Figure 19. The VCG input to the sweep generator is output by a multiplying DAC, IC 122. IC 122 is a prom containing a table of control words which correspond to the distribution of frequencies shown in Figure 18b. Each time a burst is completed (the cycle counter reaches terminal count) the address counter, IC 118 through IC 120, is incremented and a new control word, corresponding to the frequency of the next burst, is output. The standard deviation of the frequency distribution is a function of V_{ref} on the DAC; for the particular sweep generator used in this work, the standard deviation was equal to 3.29 V_{ref}. The cycle counter, composed of IC 106 and IC 107, can be preset to count from 1 to 225 cycles of the sweep generator's output before gating the sweep generator off. The cycle counter

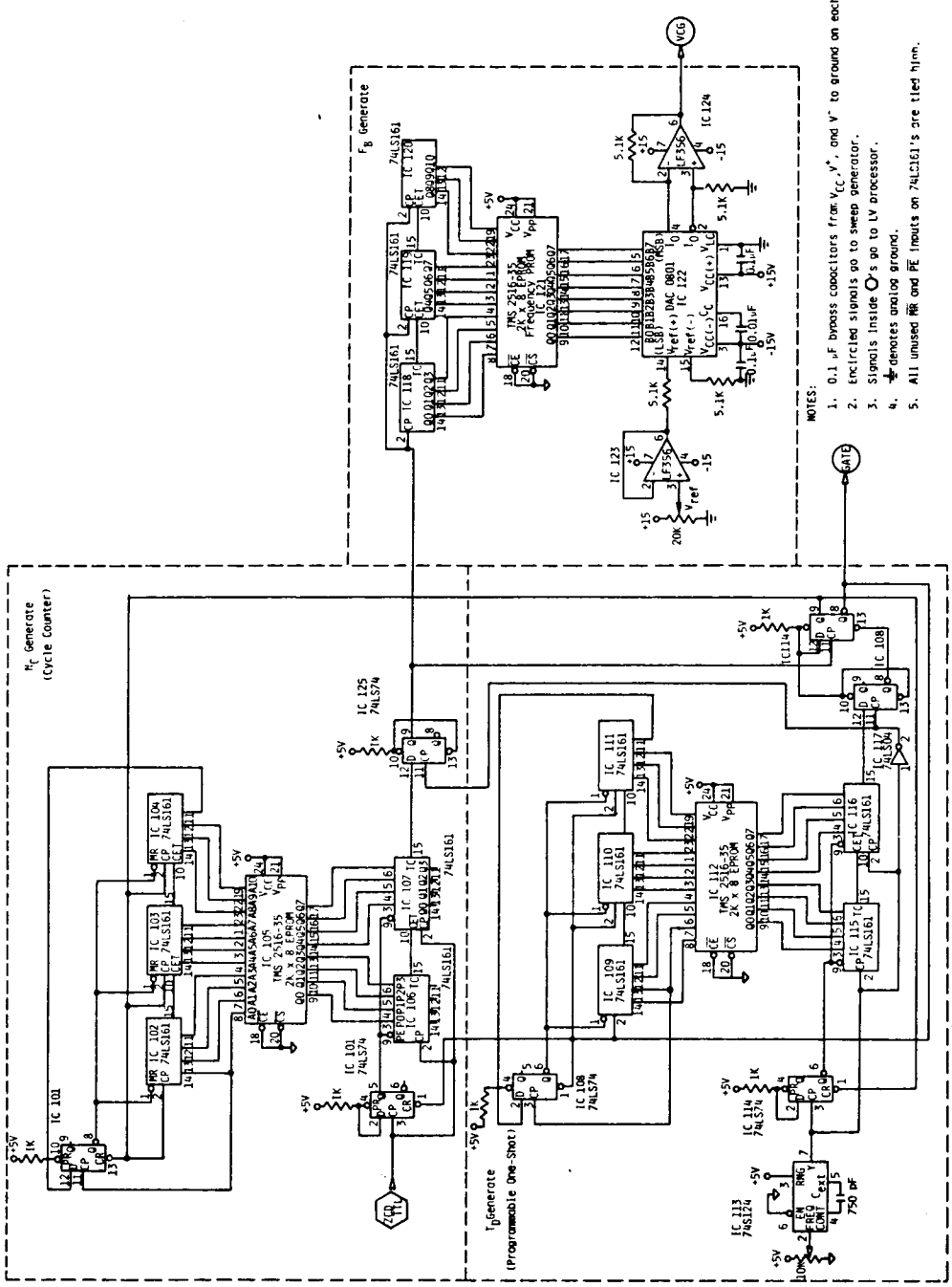


Figure 19. Signal control circuitry schematic diagram.

is preset from a prom, IC 105, whose address is incremented before each burst. The programmable one-shot operates in the same fashion as the cycle counter with one exception; the one-shot counts a timing clock (IC 113) instead of ZCD pulses.

It should be noted that the control words are stored in the proms in a random order so there should be no correlation between a prom's address and the value of the control word residing at that address. Since all three proms' address counters are incremented once per burst, they are synchronized with one another. Therefore, once a particular combination of control words is accessed (selected by the address counters), that same combination will be accessed each time the address counters recycle. This unacceptable condition was overcome by generating every possible combination of control words with three address counters. The address counters count from 0 to 2047. One of the three counters loses one count each time it recycles, while another counter loses two counts each time it recycles. Therefore, there are $(2048)^3$ combinations of control words addressed before a combination is repeated.

VITA

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