Growth, Structure, Electronic and Transport Properties of Yttrium Disilicide Nanowires

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Saban Mustafa Hus

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To my Father

Haydar Hus

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Abstract

The electronic properties of low-dimensional materials deviate significantly from their bulk counterparts. Especially in quasi one-dimensional (1D) materials, a small number of structural defects can lead to strong electron localization. Electrons may also display unusual collective behavior in 1D. As integrated circuits continue to shrink in size, there is an increasing need for understanding and possibly manipulating electronic transport in quasi 1D materials. Here, we focus on electrical transport in self-assembled YSi_2 [yttrium disilicide] nanowires on Si(001). Being just a few atoms wide, these nanowires are one of the closest experimental realizations of a 1D conductor. YSi_2 nanowires are particularly attractive because they can be integrated into silicon based electronic circuits. Little is known about their electrical transport properties, however, because it is extremely difficult to connect these atomically thin wires to macroscopic measurement contacts. This technical obstacle was overcome by developing an in-situ method for contacting these atomically thin nanowires in ultrahigh vacuum. Here, one wire end is contacted to a macroscopic contact pad via shadow mask deposition, while the other end is contacted with the tip of a scanning tunneling microscope. The nanowires turn out to be very resistive and the relation between the measured resistance and wire length is highly non-linear. From the resistance measurements, we infer a localization length that is comparable to the atomic defect spacing in the wire, thus confirming the 1D nature of the transport and highlighting the importance of charge trapping by defects. Whereas the nanowires on Si(001) grow into orthogonal directions, nanowires on Si(110) all grow in the same

direction. They exhibit a clear preference of nucleating at step edges when these edges are aligned along the [1-10] growth direction. This suggests a promising avenue for the fabrication of regular nanowire arrays with controlled wire separation, by varying the miscut angle of the Si wafer. We have demonstrated the feasibility of controlling nanowire growth, including their orientation, and related the nanowire resistance with the atomic dimensions and atomic-scale features of the wires. These insights will be increasingly relevant as nanoscale interconnects will ultimately approach the atomic limit.

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Chapter 1

Introduction and Overview

One dimensional (1D) nanostructures or nanowires are interesting realizations of strongly correlated electron systems [7]. These structures possess exotic properties, ranging from disorder induced localization effects and metal-insulator transitions [8] to dynamical separation of the spin and charge degrees of freedom [9, 10]. The bright future of nanowires in technology draws even more attention than their exotic beauty. With the current speed of transistor shrinkage, it is inevitable that nanowires will be employed as interconnects and active components of microelectronic devices in the very near future.

Any structure that will be used as an interconnect in ever-shrinking integrated circuits must be a good conductor. However, a real 1D system such as a chain of hydrogen atoms cannot be metallic [11, 12]. Furthermore, there cannot be any long range order in 1D, not even at zero Kelvin, due to large thermal and quantum mechanical fluctuations [13]. Luckily, a genuine 1D system like an atomic chain is not essential for confining electronic motion to 1D. Electrons will still be forced to move in one direction if they are confined to channels with width comparable to (ideally smaller than) their Fermi wavelength. Recent developments in nano fabrication methods [14] and synthesis techniques [15] have provided many of these quasi-1D

systems where we can still observe and utilize the behavior of electrons propogating in 1D.

Two different approaches can be followed to create 1D electron systems. In the first approach, electrons in a 2D or 3D crystal are confined to 1D by means of electric fields [16]. The electric fields are created by electrodes fabricated with "top-down" techniques. "Top-down" techniques such as ultraviolet lithography, electron beam lithography (EBL) are already being utilized by the micro-electronics industry. However, the resolution limits of these fabrication techniques are of the order of tens of nanometers [14]. Therefore, they may not present us with some of the unique transport properties we expect to observe in 1D electron systems. The second approach employs quasi-1D crystals or nano-structures as 1D electron systems. These structures are usually fabricated with self-assembly methods or "bottom-up" techniques. The features created via self assembly of atoms or molecules can reach much smaller scales since in principle they are only limited by the size of the atoms. In the last two decades many new nano-structures such as carbon nanotubes, semiconductor nanowires, atomic point contacts, atomic chains and silicide nanowires have been experimentally realized and used to investigate the complex nature of 1D electron systems [14].

Among many different types of 1D electron systems, self-assembled rare-earth metal silicide nanowires on silicon substrates [17, 18, 1] have attracted great interest due to possible integration into existing micro electronic circuit technologies. Furthermore, in their thinnest form, these nanowires are one of the closest realization of a 1D material both structurally and electronically [5], showing the capabilities of self-assembly and signaling an abundance of interesting physics [5]. Although the structure of these nanowires is fairly well understood [19, 20], our knowledge about their formation mechanism and transport properties is still very limited [21, 22].

Our lack of knowledge about the formation of rare-earth silicide nanowires arises from the time scale of the formation process which prohibits the use of relatively slow scanning microscopy techniques. On the other hand, the difficulty in bridging

different length scales between the nanowire and measurement contacts restricts the number of possible methods for transport measurements. This thesis focuses on these important but poorly understood properties of rare earth silicide nanowires. Among the many different rare-earth silicides, yttrium disilicide (YSi_2) nanowires was chosen as a model system because of their extraordinarily high aspect ratio and structural uniformity [5].

We begin in Chapter 2 by reviewing previous studies on rare-earth silicide nanowires. The majority of these studies focuses on the final structure of the nanowires as seen from Scanning Tunneling Microscopy (STM) images, while few of them also examine their formation, again only with STM. Discussion of a limited number of available transport studies on these nanowires will be left to the final chapter. In Chapter 3 we will familiarize ourselves with the experimental techniques used in this study and then in Chapter 4, we will detail our experimental studies of the formation and structure of YSi_2 nanowires on Si(100) and Si(110) substrates. In this chapter we will see how the formation process is controlled by a very delicate competition between kinetic and thermodynamic driving forces. We will also explain the advantages brought by two-fold symmetric Si(110) surface and discuss the possibility of growing parallel nanowire arrays with a controlled separation [6].

In Chapter 5 we will discuss electron transport models. Starting from the classical models developed for 3D materials we will see how the transport properties are expected to change with reduced dimensionality. We will discuss the limits of these models and try to examine their applicability to atomically thin nanowires.

Studying transport in nanowires requires a solution to the challenging task of connecting atomic scale wires with mesoscopic scale electrodes as a first step. In Chapter 6 we will explain our experimental approach to this problem and discuss its feasibility for the in-situ transport measurements on ultrathin nanowires. After we examine the behavior of electrical contacts connecting the nanowires to the macroscopic outside world, we will study the wetting layer surrounding them. Here we will discuss the possibility of leakage currents through this reconstructed surface

and look at the evaluation of its conductivity over the time. Finally we will discuss our results, which indicate a highly resistive nature for the ultrathin nanowires. We will try to understand the reasons behind the observed high resistivity and unusual relationship between the resistance of the nanowire and its length. In this chapter we will also compare our findings with previous studies on thicker rare-earth nanowires and nanowire bundles to show the big contrast in the electron transport properties of a material as it transitions from quasi-1D to an almost purely 1D structure.

Chapter 2

Rare Earth Silicides and Si substrates

Today many different types of quasi 1D structures can be synthesized, but only a handful of them can be easily integrated into silicon based microelectronics. Metallic behavior and self-assembly on a Si substrate, preferably Si(100), are two most essential characteristics to look for in a good candidate. Once they satisfy these conditions, nanowires can in principle be used as interconnects in nano-electronic devices or as gate electrodes in non-planar transistors. Some of the most promising materials for epitaxial nanowire growth on silicon are the rare earth (RE) silicide compounds. In addition to their well appreciated properties like good conductivity in bulk form and low Schottky barrier height [23] with n-type silicon, RE silicides also self-assemble into atomically thin nanowires on Si (100)[17]. The variety of possible RE silicide compounds, and the rich phase diagram for each of them, provides a large selection of nanostructures to examine and utilize in practical applications. In this chapter we will summarize a large number of studies published within the last 16 years and highlight some key findings. We will also investigate the silicon substrates the wires grow on to better understand their formation and structure.

2.1 One Dimensional Phases of Rare Earth Silicides

Formation of RE silicide nanowires was first reported by Preinesberger et al. using Dy [17]. This study was followed by many other studies on, e.g., Er [18], Ho [24], and Gd [25]. Similar nanowires have also been reported to form with Sc [25] and Y [26]. Strictly speaking, Sc and Y are not rare earth metals, but except for their lack of f-electrons, they have the same electronic configuration and form similar silicide nanowires. We therefore include these elements in the RE silicides family.

The driving force behind RE silicide nanowire formation on Si (100) is thought to be the anisotropic strain between the aluminum diboride (AlB_2) crystal structure of RE silicides and the silicon (100) substrate (see Fig.2.1). This mismatch results in a very fast growth along the less strained $[0\bar{1}1]$ direction of the Si(100) surface, and a very limited growth along the more strained [011] direction [27].

The ratio of strain in the two directions $\gamma = \epsilon_{yy}/\epsilon_{xx}$ determines the final aspect ratio of the nanowire [28, 29]. Therefore, materials with higher lattice mismatch anisotropy are more likely to display strong 1D characteristics. Table 2.1 gives the lattice mismatches between the hexagonal AlB_2 structure of various RE silicides and Si(100) surface.

Among the RE silicide structures, the lattice constant a of YSi_2 has the best lattice match with Si(100) while the lattice constant c of YSi_2 has one of the highest mismatches (see Table 2.1). Having an almost perfect lattice match in one direction makes YSi_2 the best starting point in the search of nanowires that are thin enough to display 1D transport and long enough for practical interconnects. Furthermore, the lack of strongly localized 4f electrons makes YSi_2 a suitable starting point for theoretical calculations [20], which will ultimately help us understand the transport mechanisms in these nanowires.

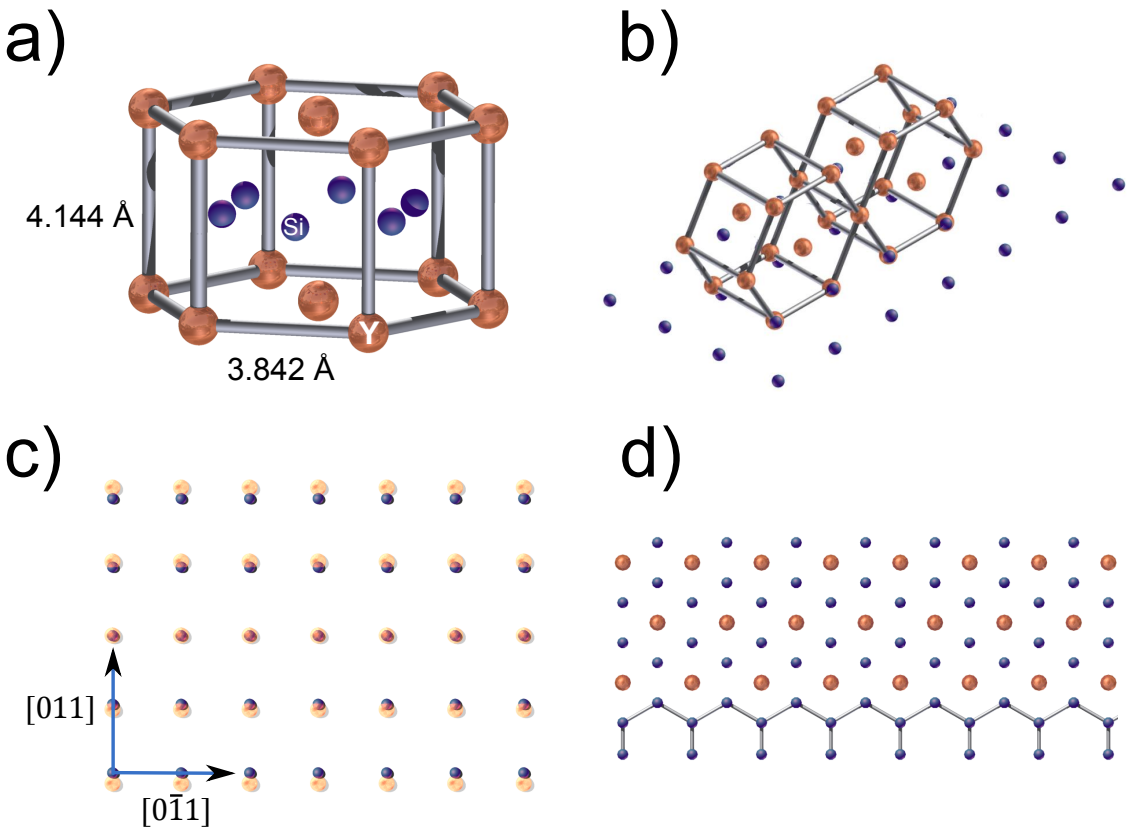


Figure 2.1: Illustration of anisotropic growth on the Si(100) surface. (a) Hexagonal AlB_2 type structure of YSi_2. (b) Alignment of YSi_2 unit cells on the Si(100) surface. (c) Top view of the YSi_2 lattice on Si(100) surface, showing one-dimensional lattice matching between the YSi_2 ($1\bar{1}00$) plane and Si(100) surface (d). Side view of epitaxial YSi_2 on Si(100)

Table 2.1: Bulk lattice constants of the hexagonal phases of various RE silicides and their % mismatch with the lattice constant of the unreconstructed Si(100)(1×1) surface [1].

Rare Earth Silicide	a(Å)	(%)	c(Å)	(%)
$ScSi_{1.7}$	3.66	(4.69)	3.87	(+0.78)
YSi_2	3.842	(+0.05)	4.144	(+7.92)
Sm_3Si_5	3.9	(+1.64)	4.21	(+9.64)
$GdSi_2$	3.877	(+0.96)	4.172	(+8.65)
$DySi_2$	3.831	(0.23)	4.121	(+7.32)
$HoSi_2$	3.816	(0.63)	4.107	(+6.95)
$ErSi_{2-x}$	3.79	(1.30)	4.09	(+6.51)
$YbSi_2$	3.784	(1.46)	4.098	(+6.71)

2.2 Si Substrates for Epitaxial Nanowire Growth

RE silicide nanowires grow epitaxially on different substrate orientations. In its bulk form silicon crystallizes in the diamond crystal structure with a lattice spacing of 0.543 nm. In this form each silicon atom makes four strongly covalent bonds with its four neighbor atoms. Different surfaces of silicon can be prepared by cutting a 3D Si crystal along a specified orientation. However, during this process at least one bond per surface atom has to be cut in half, thus creating a dangling bond. Dangling bonds increase the surface free energy, therefore the surface atoms rearrange in order to minimize the number of dangling bonds. This new arrangement of the surface atoms is referred to as a surface reconstruction.

The unreconstructed (i.e. (1×1)) structure of these surfaces determines the lattice mismatch between the substrate and the silicide and is responsible for the anisotropic growth discussed in the previous section. On the other hand, silicon substrate surfaces are always reconstructed, even at the relatively high temperatures employed during nanowire growth. The structure of the surface has a significant role on the formation

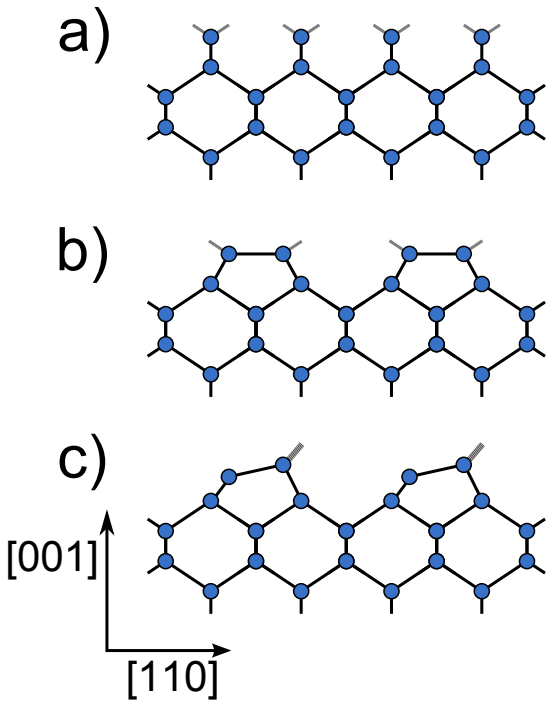


Figure 2.2: Side view of the Si(100) surface reconstruction. (a) The unstable bulk truncated (1×1) structure, (b) the p(2×1) structure with symmetric Si-Si dimers, and (c) the p(2×1) structure with asymmetric dimers.

kinetics of the nanowires. In the following sections we will examine the low index surfaces of silicon, used for nanowire growth.

2.2.1 The Si(100) Surface

Among the different low-index surfaces of the silicon crystal, Si(100) has the simplest surface reconstruction. Furthermore, most of the silicon wafers used in the semiconductor industry have the {100} orientation. Therefore, the structural and electronic properties of the Si(100) surface have been studied in great detail [2]. The bulk truncated {100} surface has two dangling bonds per surface atom, as illustrated in Fig.2.2(a). Energetically such a configuration is very unfavorable. The surface therefore reconstructs by forming Si-Si dimers on the surface, which reduces the number of dangling bonds by one half, see Fig.2.2(b),(c).

At room temperature, the Si(100) surface exhibits a 2×1 reconstruction [30, 31]. The 2×1 periodicity of the Si(100) surface can be visualized by moving a pair of surface atoms slightly towards each other to form a Si-Si dimer(see Fig.2.2b and Fig. 2.3). The formation of a symmetric dimer removes one of the two dangling bonds per atom and lowers the surface free energy by 2 eV per 2x1 unit cell [2]. The surface energy can be further decreased by tilting these dimers [32]. This out of plane buckling lowers the surface free energy with an extra 0.1 eV per dimer (Fig.2.2c). The existence of tilted dimers on the Si(100) surface has been supported by several diffraction methods [33, 34]. However, in a typical STM image taken at room temperature, dimer rows appear to be symmetric due to the slow time scale of the experimental method. Molecular dynamics calculations [35] predicts that a tilted dimer oscillates up-down with a period of approximately 200 fs which is much faster than the typical recording time per pixel in the STM. Tilted dimers can still be detected near defects and at low temperature where they are frozen in the asymmetric orientation. Dimerization does not only affects the surface atoms but also creates a strain field which can penetrate 4-5 layer into the bulk [36, 37].

Below 120 K, p(2×2) and c(4×2) surface reconstructions have been observed on Si(100) [38]. The p(2×2) surface (see Fig. 2.3), where the asymmetric dimers are arranged in an alternating fashion, has a total energy that is 0.03 eV/dimer lower than that of the asymmetric p(2×1) structure. The c(4×2) surface illustrated in Fig. 2.3 represents an energy gain of only $\sim$ 1 meV per dimer compared to the p(2×2) structure [2]. Hence, both surfaces usually coexist at temperatures below 120 K [38].

On nominally flat Si(100) wafers, there are two 2×1 domains, which are rotated 90° with respect to one another. These domains are separated by a single layer height step and are present on the surface in equal amounts [39]. However the area ratio of the two domains can be altered by applying external strain [39, 40]. Compressive strain favors the formation of large domains where the dimer bonds are parallel to the direction of the applied strain field. Small minority domains in between the majority domains remain separated by single layer height steps [41].

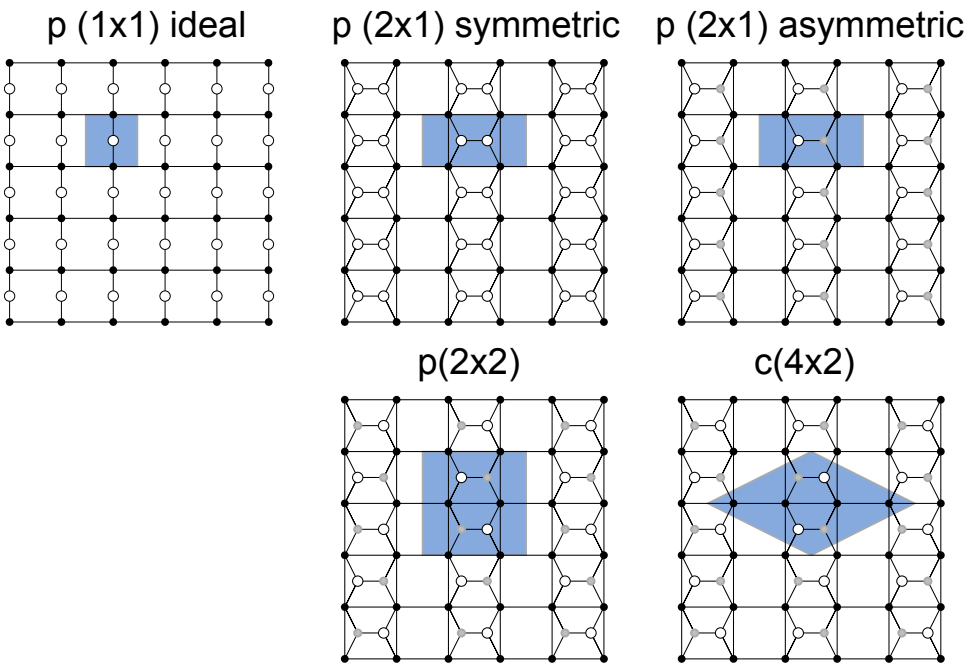


Figure 2.3: Top view of Si(100) surface reconstructions. Solid black circles represent the second layer atoms, whereas the white and gray ones are the surface atoms. For the buckled dimers, white circles protrude further out whereas the gray ones are depressed. Unit cells are represented by blue areas. Adopted from [2]

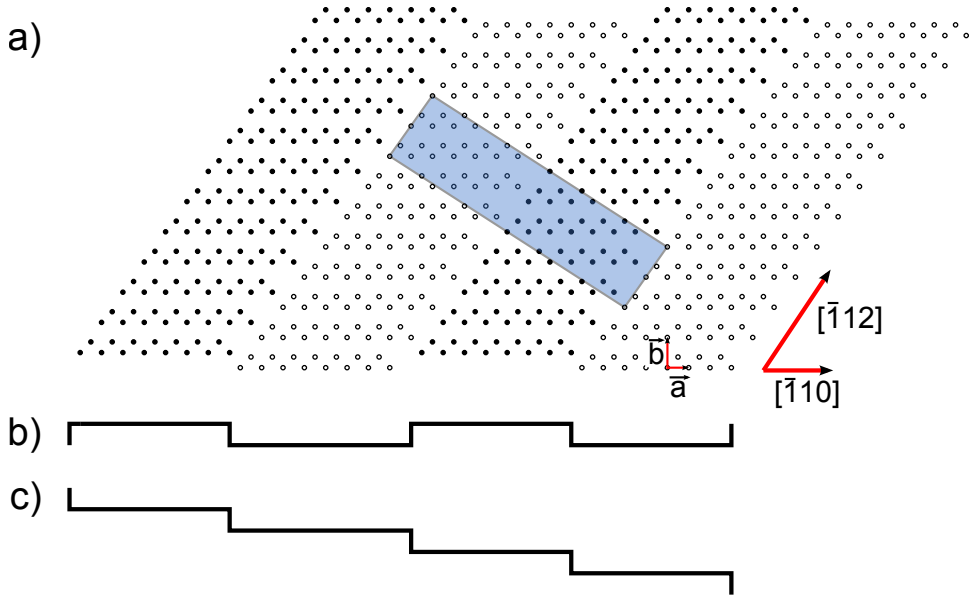


Figure 2.4: (a) Top view of the Si(110) 16×2 surface reconstruction. The solid and open circles represent the Si atoms in up and down terraces, respectively. The blue rectangle represents the 16×2 unit cell. (b) Illustration of the up-down terraces on the flat Si(110) 16×2 surface. (c) Stepped structure of the Si(17,15,1) 2×1 surface. Adopted from[3]

2.2.2 The Si(110) Surface

The {110} surface of silicon exhibits a much more complicated surface reconstruction. Various reconstructions, such as the 2×1, 5×1, 7×1, 9×1, 4×5, and 16×2 have been reported [42]. However, it was shown later that all reconstructions other than the 16×2 reconstruction are induced by minuscule amounts of nickel contaminants [43, 44].

In fact, the 16×2 reconstruction of Si(110) does not exhibit a genuine 16×2 periodicity in terms of the primitive transition vectors $\overrightarrow{a}$ and $\overrightarrow{b}$ of the unreconstructed Si(110) surface, as shown in Fig.2.4. The naming comes from the observed 16 times periodicity in RHEED patterns. The 16×2 structure is written as the $\sqrt{171} \times \sqrt{6}R(32.7°,\ 35.3°)$ reconstruction in Wood notation [45].

STM images of the Si(110) 16×2 surface are composed of a periodic arrangement of light and dark stripes along the [$\bar{1}$12] or [1$\bar{1}$2] directions. When stripes in different

directions meet, they form a chevron structure with a 70.5° angle [46]. On a flat surface, the bright stripes are one atomic layer (1.92 Å) higher than the darker ones. On a vicinal Si(110) surface, the periodic structure of up-down terraces is broken by Si(17,15,1) 2×1 facets. The structure of the Si(17,15,1) 2×1 terraces is very similar to the upper or lower terraces of Si(110)(16×2) [3]. However, Si(17,15,1) 2×1 terraces have a step structure as illustrated in Fig.2.4. The 16×2 structure forms when flash annealed Si(110) surfaces are cooled to ∼700° C. It will serve as the template for an yttrium induced surface reconstruction on top of which YSi_2 nanowires will be grown.

Chapter 3

Experimental Methods

In this chapter, the experimental methods employed in this thesis will be described. After a short description of the Ultra High Vacuum (UHV) system, two major experimental techniques, namely Scanning Tunneling Microscopy (STM), and Reflection High Energy Electron Diffraction (RHEED), will be introduced.

In this study, STM was used for two purposes: first as a surface characterization technique and second as a probe for the transport measurements. While this chapter focuses on traditional use of STM for imaging surfaces and nanostructures, its nanofabrication capabilities will also be mentioned. STM's use in transport measurements will be detailed in Chapter 6. Finally, the use of RHEED as a complementary tool to STM imaging and its unique capability to observe nanowire formation in real time will be explained.

3.1 Nanowire Growth in Ultra High Vacuum

YSi_2 nanowire growth starts with the preparation of an atomically clean Si surface. The cleanliness of a surface depends on three parameters: first the reactivity of the surface, second the type of contaminants found in the immediate environment, and third the number of such contaminants. Reactivity is a property of the surface under investigation and cannot be controlled without modifying the surface itself. However,

the other two parameters can be controlled. For a carefully prepared and protected sample, the only contaminants come from the sample holder or from the residual gas molecules surrounding the sample. The number of these molecules can be controlled by keeping the sample in a vacuum environment. Due to the reactive nature of both clean Si surfaces and the rare earth metals, the samples have to be prepared and kept at extremely low residual gas pressures of 10^{-10} Torr or better. This special environment is known as Ultra High Vacuum (UHV) and requires advanced techniques to be produced and maintained [47].

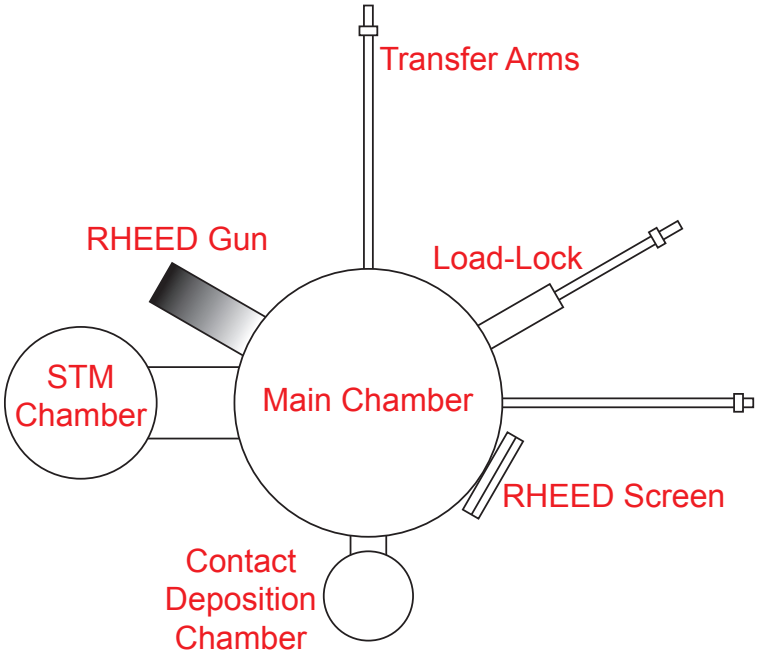


Figure 3.1: Schematic top view of the UHV chamber used in our experiments

The UHV system used in this study is composed of several sections as illustrated in Fig. 3.1. The main chamber is a home built stainless steel chamber and is used for sample preparation and RHEED experiments. It contains a sample manipulator capable of heating samples with a resistive heater to 500° C and cooling them with liquid nitrogen to about 120 K. Samples can be further heated by passing a electrical current through them. The STM chamber contains an Omicron variable temperature STM (VT-STM) and a sample storage platform. The contact deposition chamber is

a small chamber designed and built solely for depositing in-situ metal contacts on the nanowires. Finally, the system has a load-lock separated from the main chamber with a gate valve. The load-lock allows samples to be introduced to the system without breaking the vacuum in the main chamber. The UHV chamber has a base pressure of around 3x10^{-11} Torr which is maintained by an ion pump and a titanium sublimation pump (TSP).

3.2 Scanning Tunneling Microscopy

Studying materials at the nanoscale and utilizing their novel properties requires microscopy methods with spatial resolutions high enough to visualize individual atoms or molecules. Even though the field ion microscope provided such an opportunity during the mid 20^{th} century, it had not received widespread use due to its complexity. Major breakthroughs in the field of nanoscience and nanotechnology only materialized after the invention of the STM in early 1980s [48, 49].

The STM is based on the concept of quantum tunneling which will be explained in detail in the next few pages. When the metal tip of an STM is brought into very close proximity to the sample surface, the wave functions of the tip and the sample begin to overlap. Therefore, electrons can tunnel between the two [50]. The application of a potential difference between the tip and the sample generates a net tunneling current, which strongly depends on the wave function overlap. This overlap is determined by the distance between the tip and sample. The current also depends on the local density of states (DOS)[51]. If the height of the tip is fixed, protrusions and depressions on the surface result in higher or lower tunneling currents, respectively.

STM images can be created by measuring the current as the tip is moved across the sample in the x-y plane [50]. This method is referred to as constant height topography (Fig. 3.2(a)). Another way to obtain the surface topography is by using a feedback system, which keeps the tunneling current constant while scanning by

moving the tip up and down along the z-direction. This mode is called constant current topography (Fig. 3.2.(b)). Each mode has its own advantages. The constant height topology provides faster scans since the tip height is not regulated. However, it is only suitable for relatively smooth surfaces. In constant current topography, the tip height is controlled (or measured) with a piezoelectric scanner, which has a 0.01 nm or better spatial resolution. Regulation of current by adjusting the tip height provides a slow but more accurate reading of surface topology. Therefore, in this mode, the surface topography can be mapped with greater precision than with the constant height mode, as the tip scans the surface in the x-y plane [50]. In both modes, the resolution in x-y plane is usually limited by the finite radius of curvature of the STM tip.

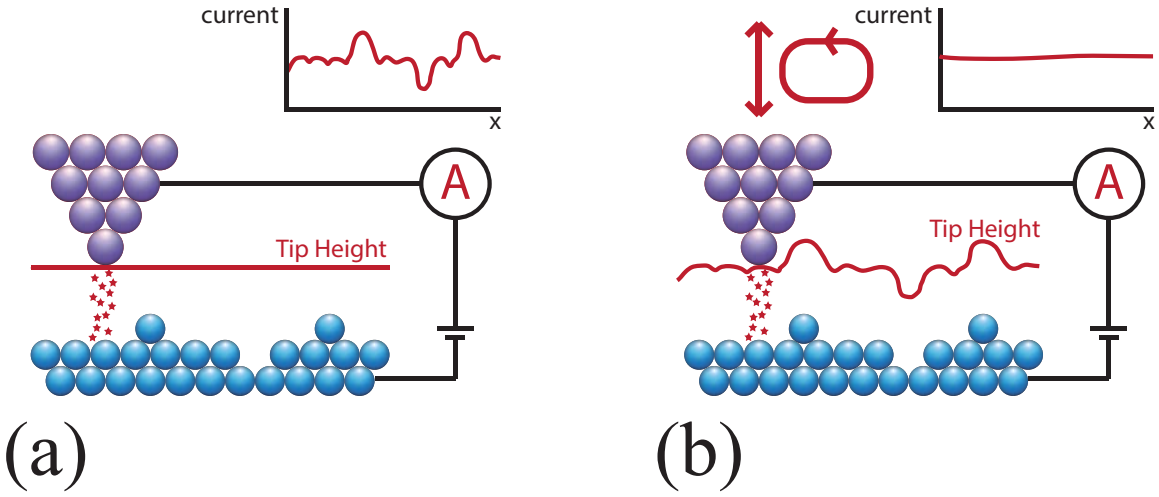


Figure 3.2: STM Modes. (a) In constant height topography, the tip height is kept constant while the tunneling current is being recorded; (b) In the constant current mode, the tip height is controlled via a current feedback loop so as to maintain a fixed tunneling current (b).

In the simplest 1-D elastic tunneling case, the probability of tunneling can be derived from the decay of the electron wave function inside the potential barrier between the tip and the sample, i.e.

$$\Psi_e(z) = \Psi_e(0)e^{-\kappa z} \tag{3.1}$$

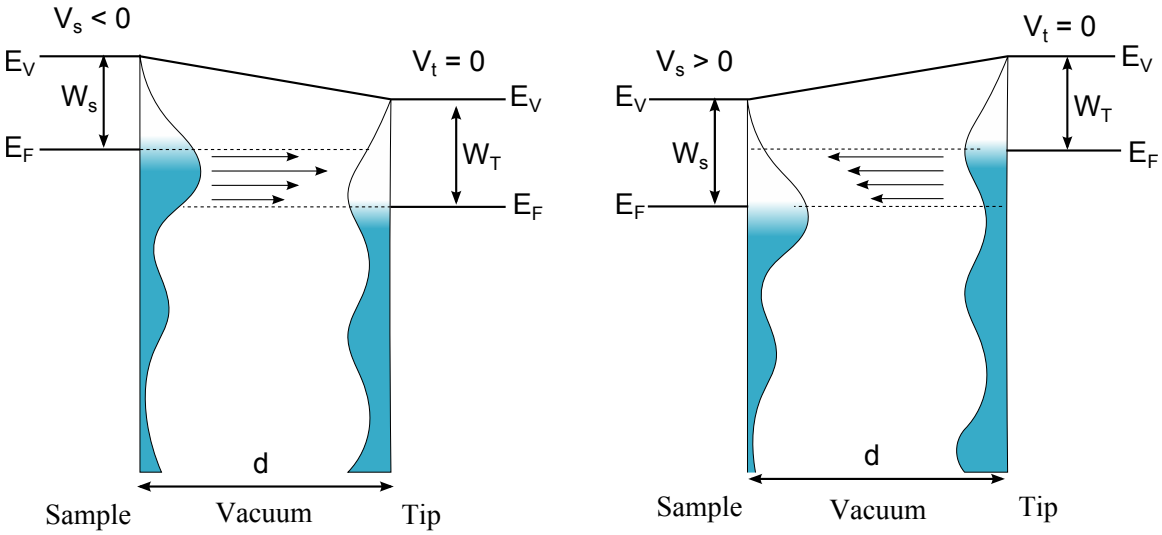


Figure 3.3: Energy level diagram of the tunnel junction between a metal tip and metal surface. The left hand side of the figure represents a negatively biased sample, whereas the right hand side represents a positively biased sample. Electrons occupying the states within the energy window between the Fermi levels of sample and tip contribute to the net tunneling current.

Where $\Psi_e(0)$ is the wave function of the electron inside the tip (or sample) and

$$\kappa = \frac{\sqrt{2m(U-E)}}{\hbar} \tag{3.2}$$

where U is the barrier height, m the mass of the electron, E its initial energy and $\hbar$ the reduced Planck constant. Therefore the probability of tunneling through a barrier of width d can be given as

$$P(d) = |\Psi_e(d)|^2 = |\Psi_e(0)|^2 e^{-2\kappa d} \tag{3.3}$$

The tunneling current is given by integrating these tunneling probabilities over all possible initial and final energies as illustrated in Fig. 3.3 [52].

$$I = \frac{4\pi e}{\hbar} \int_{-\infty}^{\infty} [f(E_f - eV) - f(E_f + \epsilon)]\rho_s[E_f - eV + \epsilon]\rho_t[E_f + \epsilon]|M|^2 d\epsilon \tag{3.4}$$

where f is the Fermi function. ρ_s and ρ_t are the density of states of the sample and tip, respectively. Finally M is the tunneling matrix between the wave functions of the tip and the sample surface [51].

By using a step like Fermi distribution function for low temperatures and constant matrix elements in equation 3.4 the tunneling current reduces to:

$$I \propto \int_0^{eV} \rho_s[E_f - eV + \epsilon]\rho_t[E_f + \epsilon]d\epsilon \tag{3.5}$$

which is simply the convolution of the DOS of the tip and sample. If the DOS of the tip is known, then the DOS of the sample can be deconvolved. Assumption that the tip DOS is constant, it can be easily shown that

$$\frac{dI}{dV} \propto \rho_s[E_f - eV] \tag{3.6}$$

The relationship between the tunneling current and LDOS provides highly valuable information about the electronic properties of the sample surface. By fixing the other variables like the spatial position of tip and the sample tip separation one obtains information about the LDOS of the sample by simply varying the tip-sample bias. This method is called (scanning) tunneling spectroscopy (STS) and frequently accompanies topographic STM images [50].

3.2.1 STM for Contact Fabrication

In addition to its imaging and spectroscopic capabilities, STM is also a very powerful tool for controlled manipulation of atoms on surfaces with atomic precision [53]. The fabrication capability of the STM can also be employed for creating electrical contacts to nanostructures for transport studies. This can be done both by depositing metal clusters on top of the nanostructures [54, 22] or by desorbing metal films to reveal the underlying nanostructures [55].

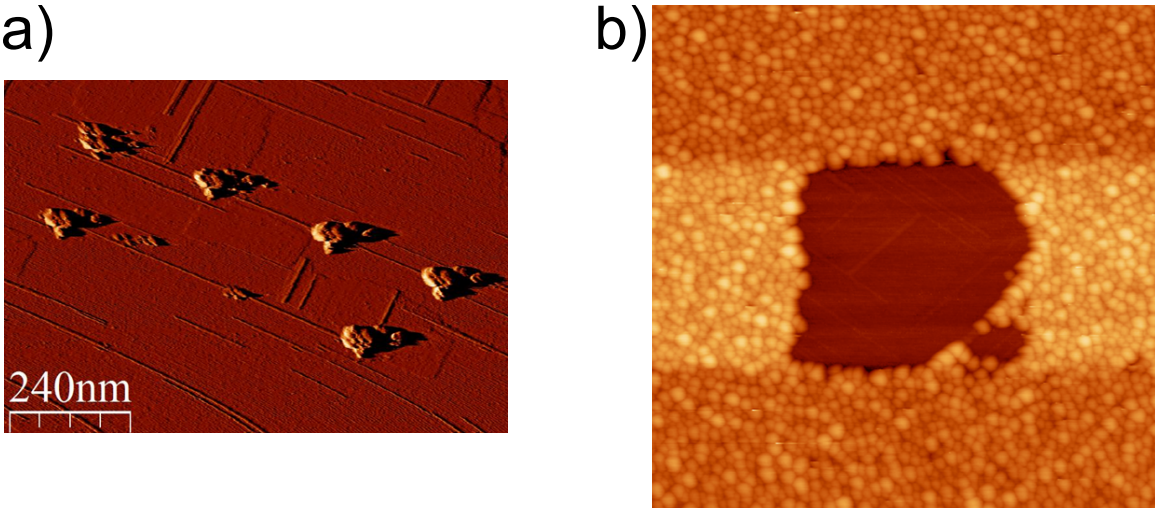


Figure 3.4: Examples of nanofabrication capabilities of STM for transport measurements. (a) The STM tip can be used to deposit nanoclusters with atomic precision. (b) It can also be employed as an electron gun to lift-off the metal clusters. STM Image size: 500 × 500 nm.

In this study, the feasibility of both approaches for metal contact deposition on a nanowire has been tested. In the first approach [22], silver (or gold) clusters were deposited on the sample surface by applying voltage pulses to the silver STM tip when it was positioned within tunneling distance. With this approach we successfully deposited metal contacts over the nanowires with a very high precision of position and repeatability as shown in Fig.3.4(a). These clusters usually had sizes between 10-100 nm. In this process metal deposition may occur either by field-induced emission of silver atoms [54] or by an initial contact between the tip and the sample [56, 57]. Contact deposition via STM tip was used during our transport measurements to check for the contribution of the tip-wire contact resistance to the total measured resistance.

Another method for fabricating microscopic contact pads for transport measurements is to use the STM tip as a nano-lithographic tool [58]. The STM tip can be viewed as a very small, highly localized electron gun, which can be used to trigger surface reactions similar to the ones used in electron beam lithography (EBL) or electron beam-induced deposition (EBID) [59, 60, 61]. The most successful

implementation of this method is the use of an STM tip to create sub-10 nm wide conductive Si:P wires on a H terminated Si surface [62, 63].

We have used a similar technique to access the nanowires buried under a thin metallic film. In this method, a thin silver (or lead) film was deposited on a Si sample with YSi_2 nanowires. The STM tip was then used to locally desorb the silver clusters from the surface, opening a window to the buried Si surface with epitaxial nanowires (see 3.4(b)). In this method, thin silver films were swept from the surface by quickly scanning the selected area at low tip voltages. Even though we did not use it in our transport measurements, this method can still be employed to draw complex contact patterns or markers with STM.

3.3 RHEED

YSi_2 nanowires studied in this work are all grown epitaxially, meaning that the substrate, wetting layer, and nanowires all have periodic structures and that there is a well-defined registry between them. Such periodic structures invite the use of diffraction techniques to investigate the surface structure. Among the many diffraction techniques, RHEED is the most commonly used method in MBE because of its surface sensitivity and its scattering geometry, which allows for real time monitoring of the surface structure during growth [64].

In this work the main purpose of the RHEED experiments was to complement the STM studies in determining the surface structure. In contrast to STM, RHEED has the capability for real time monitoring of the surface structure over a macroscopic area. Such a survey would be very time consuming with STM because of its slow scan speed for atomic-resolution imaging. In addition, with RHEED we can follow the evolution of the surface structure during growth. The chamber geometry and fast time scale of the nanowire growth make it impossible to observe this process with STM.

In RHEED, a high energy electron beam produced and focused by an electron gun is reflected from the surface at grazing angle. The reflected electrons hit a phosphorous screen and reveal a diffraction pattern as illustrated in Fig. 3.5. Bright spots in this pattern result from constructive interference of the scattered electron beams, which occurs when the Bragg condition is satisfied. For a one dimensional chain of atoms, the Bragg condition can be written as,

$$a\cos(\theta_i) - a\cos(\theta_f) = n\lambda \tag{3.7}$$

where a is the periodic spacing between two atoms, θ_i (θ_f) is the angle between the incident (final) beam and the atom chain, λ is the wavelength of the electrons and n is an integer. Before starting a more complete discussion of electron diffraction in terms of the Laue-Ewald construction, one should look at figure 3.5 and equation 3.7 to appreciate the strong points of RHEED in MBE. Grazing angles (small θ) have many advantages for the experimental set-up. First it provides an ideal set-up where the electron gun, sample, and phosphorus screen are well separated from one another allowing a large number of deposition sources to be placed in the system without blocking the electron beam. Grazing incidence also limits the penetration of the electrons deep into the substrate, and therefore enhances the surface sensitivity. Finally λ has to be much smaller than a to satisfy the Bragg condition meaning that high energy electrons have to be employed. This significantly simplifies the electron gun design and provides a well focused electron beam[64].

Diffraction patterns in RHEED can be better understood with the Laue-Ewald construction. Using $k = 2\pi/\lambda$ and $b = 2\pi/a$ equation 3.7 can be written as,

$$k\cos(\theta_i) - k\cos(\theta_f) = nb \tag{3.8}$$

Because b is the fundamental translation vector of the one-dimensional reciprocal lattice, Eq. 3.8 indicates that constructive interference will be observed when the difference between the momentum vectors of the incoming and outgoing electrons

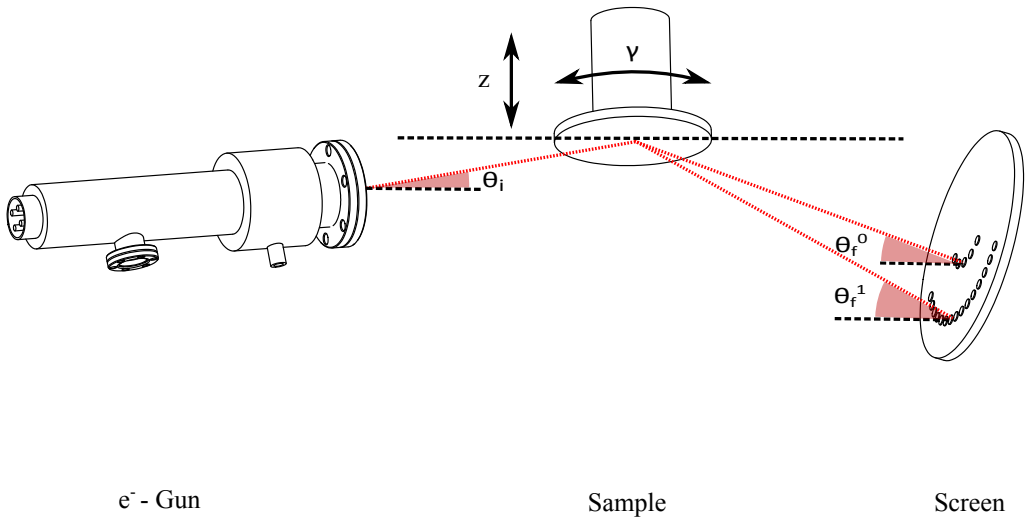


Figure 3.5: Set-up of the RHEED experiments. A high energy electron beam, produced and focused by an electron gun, is reflected from a surface at a grazing angle θ_i . The reflected electrons hit a phosphorous screen, revealing a diffraction pattern. While the electron gun and screen locations are fixed, the sample can be rotated to observe diffraction patterns along different crystal azimuths.

equals a reciprocal lattice vector. For a 1D chain of atoms, the reciprocal lattice consists of a periodic array of diffuse planes, spaced by a distance $|b|$, that are perpendicular to the atom chains in real space. For elastic scattering, $|k|$ is constant and Eq. 3.8 is satisfied if the momentum vectors of the outgoing electrons form a cone with half angle θ_f. The base of the cones can be interpreted as the intersection of the n^{th} order reciprocal lattice plane with the Ewald sphere of radius $|k|$.

The Laue-Ewald construction for a 1D chain of atoms is illustrated in Fig .3.6. In this construction the RHEED screen acts as a view port, showing only a small part of the Ewald sphere. The latter typically has a radius much larger than reciprocal lattice distances. The illustration shows the diffraction patterns observed on the RHEED screen as it is rotated around the Ewald sphere. In reality, the RHEED screen and

electron gun have fixed position and the sample (therefore, the reciprocal lattice) is rotated instead.

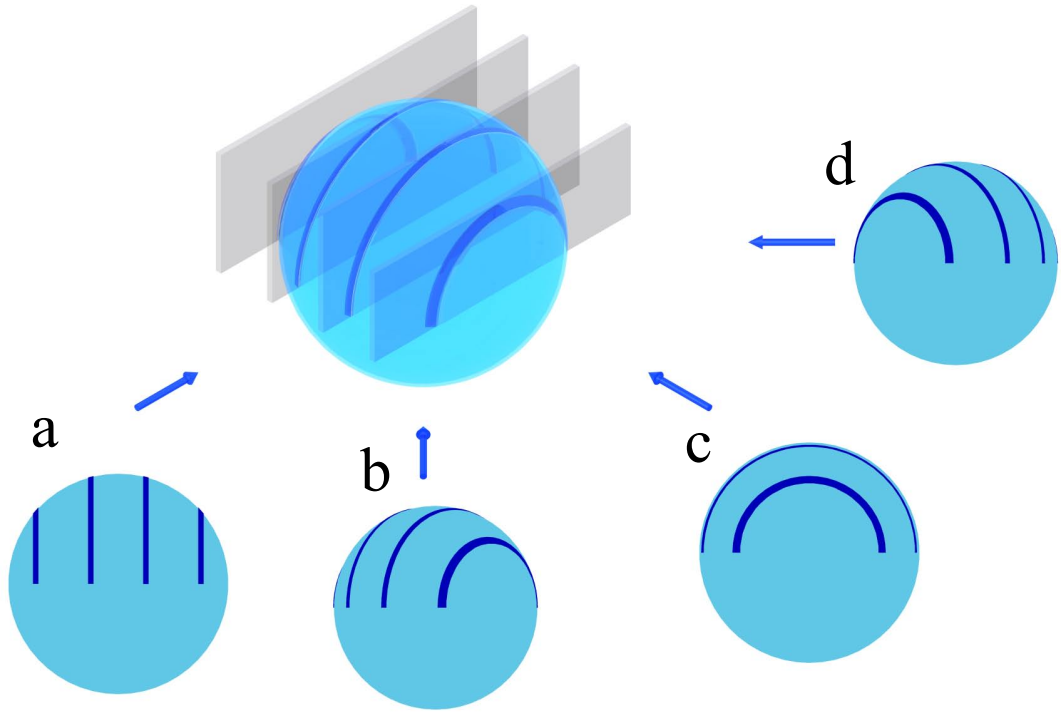


Figure 3.6: Illustration of Laue-Ewald construction for an atomic chain and the corresponding RHEED pattens. The phosphorous screen acts like a view port to observe the Ewald sphere along directions indicated by the arrows. The angle between the atomic chain direction and the screen normal is (a) 90°), (b) 45°, (c) 0°, and (d) -45°.

As seen in Fig.3.6 if the atom chains are perpendicular to the screen, one observes half circles on the RHEED screen. As the sample is rotated, the half circles transform into curvy lines. Finally, when the atom chain and RHEED screen are parallel to one another, the RHEED pattern consists of vertical lines. Such transformations were used the determine the orientation of the nanowires on the different substrates.

Eq. 3.8 can be expanded to 2D surfaces and 3D crystals and can be expressed as:

$$|k_f| = |k_i| \tag{3.9}$$

$$k_f - ki = G_m \tag{3.10}$$

where k_i and k_f are the incident and scattered wave vectors and G_m is a vector of 2D or 3D reciprocal lattice.

A crystal surface has no translational symmetry perpendicular to the surface. Therefore, its reciprocal lattice is composed of ordered rods perpendicular to its surface. When these rods intersect the Ewald sphere, the diffraction condition expressed in Eq. 3.10 is satisfied and bright spots are observed in RHEED screen. This construction can easily be visualized by replacing the reciprocal lattice planes (gray rectangles) of Fig. 3.6 with rods which lie on the gray planes and perpendicular to its long edge.

RHEED patterns are very useful for surface characterization. However, RHEED has one more advantage that distinguishes it from other diffraction methods. The intensity of the diffraction spots depends on the surface roughness and this roughness oscillates periodically during layer by layer MBE growth. This period is equal to the time required to deposit one monolayer of material [65, 66]. Due to its grazing angle geometry, RHEED allows observation of these oscillations during MBE growth and is commonly used to count the number of deposited layers [64].

The nanowires examined in this study all grow at sub-monolayer coverage. Therefore, RHEED oscillations cannot be observed. However, the intensity of a particular spot still depends on the surface area covered with the corresponding surface reconstruction. We qualitatively studied the evaluation of spot intensities during nanowire growth to better understand the formation sequence of the different surface phases.

Chapter 4

Growth and Characterization of YSi_2 Nanowires on Various Si Substrate Orientations

In this chapter we will investigate the growth and structure of YSi_2 nanowires on various silicon surfaces. First we will discuss the formation and structure of nanowires on Si(100) which has been studied in great detail . Next, we will examine nanowires on the Si(110) surface where they show unidirectional growth.

4.1 YSi_2 Nanowires on Si(100)

As we discussed in section 2.1 the rare earth silicide nanowires were first fabricated on the Si(100) surface [17]. Despite the large number of studies following the work of Preinesberger *et al.*, the formation and structure of the thinnest nanowires are still surrounded with questions.

As a product of anisotropic strain, YSi_2 nanowires are meta-stable [1, 4]. Therefore, small variations in substrate temperature and deposition time have a significant effect on the final shape of the nanowires. In this section we will investigate

the various stages of YSi_2 nanowire formation with STM. Starting with the formation of the wetting layer and ultra-thin nanowires, we will describe the evaluation of the nanowires as a function of yttrium coverage. Then we will look at the influence of substrate temperature on the nanowire growth. At the end of the section we will present RHEED studies, which complement and confirm the STM experiments and answer more questions about the formation of nanowires.

4.1.1 Sample Preparation and Nanowire Growth

The silicon substrates used in this study were sliced from commercial wafers. They were first cleaned with acetone and isopropyl alcohol in an ultrasonic cleaner for 10 minutes and rinsed with deionized (DI) water before being inserted in the load-lock compartment of the UHV system. Once they were transferred to the MBE chamber, samples and sample holders were thoroughly degassed with a resistive heater mounted on the sample stage. This process has two benefits. First, it minimizes the sudden pressure increase when flashing the sample for surface cleaning purposes. Second, it decreases the resistance of the sample which enables us to pass a current through the sample which would otherwise be highly resistive. Once the sample holder was outgassed and sample resistance dropped below 1 KΩ, a potential difference was applied between the two ends of the sample to further heat it by passing a direct current through the sample. The sample temperature was observed with a pyrometer and set to $\sim$600 °C by adjusting the sample current. The samples were subsequently outgassed at this temperature for several hours. The native SiO_2 layer was subsequently removed by flash heating the sample to 1200 °C several times. Care was taken to ensure that chamber pressure stayed below 1×10^{-9} mbar during the flash heating. The duration of the flash anneal was increased with each cycle and samples were considered to be clean once they could be kept at 1200°C for more than 20 seconds while satisfying the chamber pressure condition. After the flash anneal, samples were rapidly cooled to $\sim$900°C and held at this temperature for five more

minutes. Next, the sample was slowly cooled to a temperature between 600°C and 650°C where the nanowires were grown.

YSi_2 nanowires were grown via e-beam evaporation of 99.99 % pure yttrium metal onto the heated Si(100) substrate. The thinnest nanowires form at an yttrium coverage (θ) between 0.4 and 0.5 ML, where 1 ML corresponds to 6.78 x 10^{14} atoms/cm^2, which is the surface atomic density of Si(100). Samples were quenched immediately after deposition or after a short post annealing. The post annealing was typically less than 30 seconds. The substrate temperature and/or yttrium coverage were used as variable parameters to investigate the formation of the various yttrium silicide structures on Si(100).

4.1.2 Self Assembly on Si(100)

Wetting Layer

Nanowire growth is controlled by a very delicate competition between kinetic and thermodynamic driving forces and is still not fully understood [1]. Our STM studies show that nanowire growth starts with the formation of Y adatom chains similar to the results from earlier studies on other rare-earth silicide nanowires [67]. These adatoms create a 2D yttrium induced surface reconstruction or wetting layer. Two different types of wetting layers are observed in the Y/Si(100) system, namely the (2×4) and (2×7) surface reconstructions [4]. The (2×4) reconstruction starts to form in the very early stages of yttrium deposition and is gradually replaced by the (2×7) reconstruction, which finally covers the whole surface.

Fig. 4.1 presents an STM image of the sample surface at low yttrium coverage (θ) of 0.25 ML. In this image both the clean Si surface and the wetting layer reconstruction can be resolved, showing that the wetting layer rows grow perpendicular to the surrounding silicon dimer rows. As we discussed in section 2.1, there are two types of terraces on a pristine flat Si(100) surface, the Type-A terrace (T_A) where the Si dimer rows are running parallel to the down-step edge, and the Type-B terraces

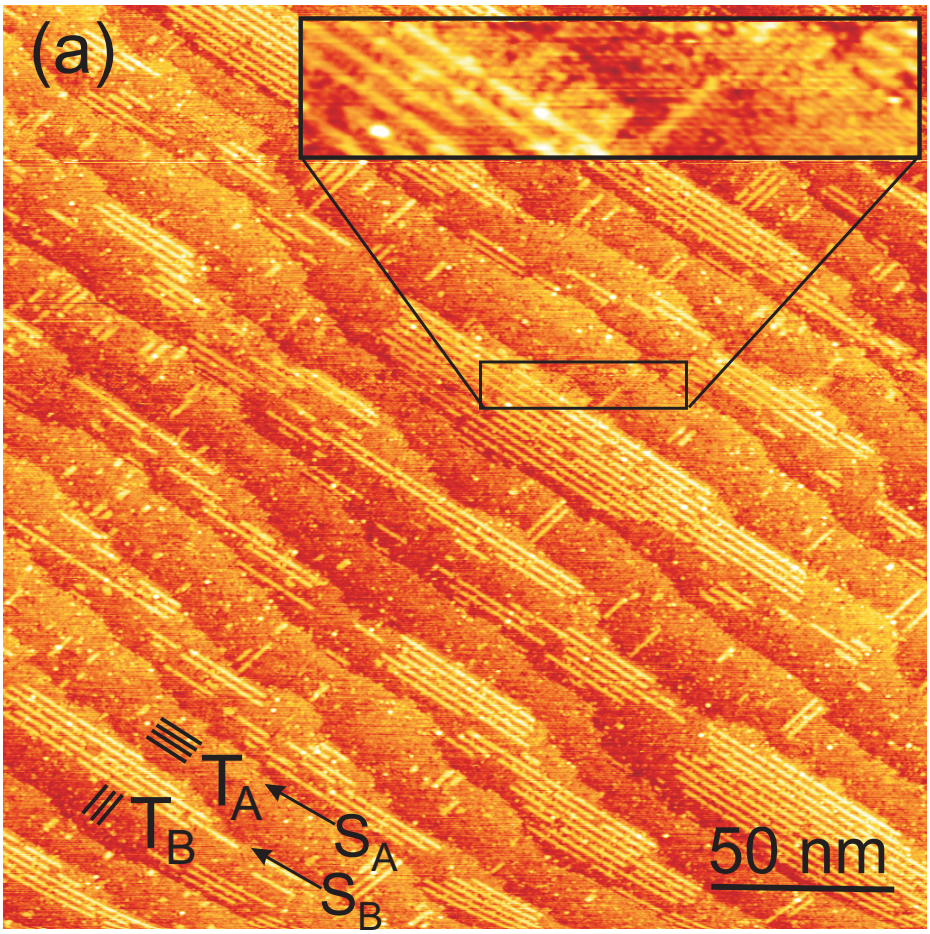


Figure 4.1: STM image showing an incomplete (2×7) wetting layer. The two types of steps, S_A and S_B, and the respective terraces, T_A and T_B, are indicated.The inset shows an enlarged area for a better visualization of the reconstruction. Notice the Si dimer rows in the background. The image was recorded at 1.5 V, 0.1 nA. Adopted from [4].

(T_B) where the dimer rows are perpendicular to the down-step edge. These terraces were indicated in the figure together with the respective steps edges (S_A) and (S_B). Due to the intrinsic four-fold symmetry of the Si(100) surface, one always finds two orthogonal domains with equal probability unless special preparation procedures are followed [50]. Fig. 4.1 does not show any preference between alternating Type-A or Type B terraces. However at this low coverage, the (2×7) wetting layer is predominantly formed on the Type-B terraces, suggesting that the terrace edges play an important role in wetting layer nucleation. Yttrium atoms on Type-A terraces can travel over very long distances parallel to the terrace edges [68]. However, on the Type-B terraces they travel much shorter distances before reaching a terrace edge, where they nucleate or merge with existing (2×7) patches. Interestingly, unlike the yttrium rows of the (2×7) reconstruction, the YSi_2 nanowires do not show any preference for the terrace type, nor is there a clear preference for nucleation at the terrace edges. As θ increases both the clean Si(100)(2×1) and yttrium induced (2×4) reconstructions start to disappear in favor of the (2×7) reconstruction. When $\theta =$ 0.4 ML, the (2×7) wetting layer formation is completed on both type of terraces.

The STM images in Fig. 4.2 show the details of the (2×7) wetting layer. It is composed of dimer rows separated by the areas of lower apparent height depending on the tunneling bias and polarity. In addition to the dimer rows, slightly thicker and brighter lines parallel to the dimer rows are also visible at this coverage as highlighted by the arrows in Fig. 4.2. The brighter lines grow on top of the dimer rows and appear to be 0.1 nm higher than those at -1 V bias [4] . These bright lines may be immature nanowires and precursors of the ultrathin nanowires. Similar lines have also been observed for Dy on Si(100) [69] where they have been referred to as 'dark wires'. For yttrium, these dark wires are found to be between 1.1 nm and 1.5 nm wide and their formation seems to be associated with occasional phase shifts in the (2×7)reconstruction. Cui *et al.* [69] studied these phase shifts in detail for Dy on Si(100) and claimed that they are responsible for the formation of the nanowires.

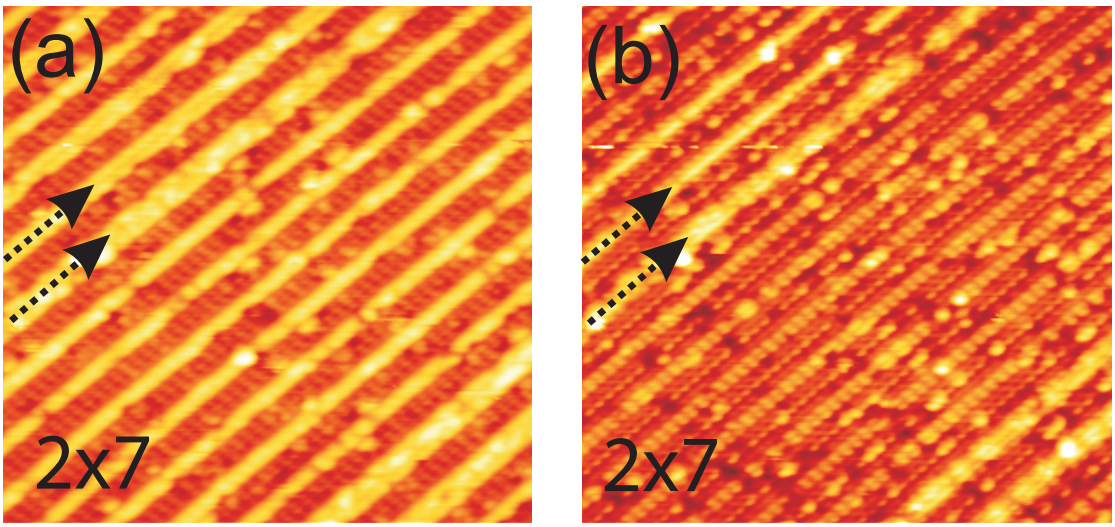


Figure 4.2: (a) and (b) Filled-state (-1.3 V) and empty-state (+1.3 V) STM images of a complete wetting layer. Arrows point to extra rows on top of the (2×7) atom rows. The image size is 27 nm×27 nm. Adopted from [4]

Four-probe transport measurements [21] and STS studies [4] indicate that the wetting layer is not metallic. However our STS measurements show that the wetting layer is initially metallic but quickly passivates even at very low chamber pressures. Details of these measurements will be discussed in section 6.4.

Formation of Ultrathin Nanowires

The ultrathin nanowires nucleate after an almost complete (2×7) wetting layer is formed and can only be observed in a very narrow coverage range $(0.4 \leq \theta \leq 0.5)$. These nanowires grow parallel to the atom rows of the wetting layer, suggesting that the adatom diffusion barriers are lowest along the atom rows. They are isolated from each other and have widths ranging from 1.3 to $\sim$ 4 nm. Furthermore, the in-plane widths of these nanowires are quantized in integer multiples of the Si(100) lattice constant ($a_0 = a_{Si} = 0.384$ nm). For simplicity the wires will be named according to their width such as $3a_0$, $4a_0$, etc. The $3a_0$ and $5a_0$ nanowires are most common [5]. Even multiples ($4a_0$, $6a_0$) are also visible [70] but they are less common. The structure of these nanowires will be discussed in section 4.1.4.

If they are grown on substrates with low miscut angle ($\leq 0.1°$), the nanowires can grow as long as 1000 nm depending on the local availability of yttrium. By optimizing the growth parameters we were able to grow nanowires with lengths up to 2000 nm. This was done by high temperature annealing (950°C for 30 min) of the clean Si(100) substrate right before the final cooling process described in section 4.1.1. This process results in very wide flat terraces separated by a series of narrow terraces. One of the reasons behind this behavior may be the mechanical stress on the substrate, which is clamped between molybdenum plates at both ends[39]. Once the wide terraces were obtained, the deposition rate also had to be modified. The longest nanowires were obtained with the combination of fast deposition rates (0.5 ML /min) and one minute post annealing. Post annealing allows immature nanowires to merge into longer ultra-thin nanowires. However, this recipe may also lead to the formation of nanowire bundles, as will be discussed later. Formation of these bundles can be minimized by keeping the total growth time (deposition + post annealing) below 3 minutes.

Formation of Nanowire Bundles

Deposition rate, substrate temperature, and the yttrium content of the wetting layer are all expected to influence the growth and morphology of the nanowires. Our studies [4] show that a small change in any one of these parameters can have a strong influence on the growth process. Particularly, the balance between the formation of isolated wires versus nanowire bundles is very delicate. Keeping all the other parameters fixed (deposition rate = 0.2ML/min, T_s=630°C) a slight increase in yttrium coverage ($\Delta\theta$ = 0.1 ML) initiates bundle formation. Bundles contain several nanowires with an interwire distance of $1a_0$. Most of the wires assembled in bundles have widths of $3a_0$ to $7a_0$, however, thicker wires can be occasionally observed particularly on vacancy rich wetting layers. DFT calculations indicate that these nanowire bundles are energetically preferred over spatially separated nanowires [4].

Besides the yttrium coverage, the substrate temperature also has a significant effect on the formation of the various YSi_2 phases. To study the effect of substrate temperature in more detail, we have created a 75 °C temperature gradient over the sample and placed it far away from the deposition source to ensure a homogeneous deposition rate across the sample. The coverage ($\theta = 0.35$ ML) is selected so as to observe the surface close to the completion of wetting layer growth. On the cold side of the sample(≈600 °C), the (2×7) wetting layer covers both the A and B type terraces while the nanowires are absent (Fig. 4.3(a)). However, at the center of the sample, where the substrate temperature reached 630 °C, thin nanowires appear (see Fig. 4.3(b)). Note that vacancies and phase shifts in the (2×7) row structures are uniformly distributed, showing no indication of yttrium or silicon depletion in the immediate vicinity of the nanowires. At 650 °C, on the hot side of the sample, wire-bundles start forming and the single isolated nanowires and (2×7) wetting layer have disappeared (Fig. 4.3(c)). Hence, at a fixed global yttrium coverage, increased temperature and surface diffusion reduces the (2×7) wetting layer coverage, as more yttrium (and silicon) is incorporated into the nanowires. When the influence of high coverage and high temperature are combined very long nanowire bundles can be grown [4]. With the help of the high substrate temperatures these bundles can easily modify the terraces of Si surface by both eroding the steps and forming their own terrace as they grow longer. At high coverage the growth of a bundle stops only when it runs into another bundle creating a so called nanowire bundle junction. Despite being on different terraces these junctions make electrical contact [21] and form a wire network on a macroscopic area. At this stage of YSi_2 deposition one can start to see the nucleation of a second layer of silicide on top of the bundles as a precursor to the upcoming 3D structures.

Formation of 3D Islands

Neither the wetting layer nor the nanowires can be grown at substrate temperatures greater than 650°C. Instead very thick (possibly 3D) wires and wide bundles dominate

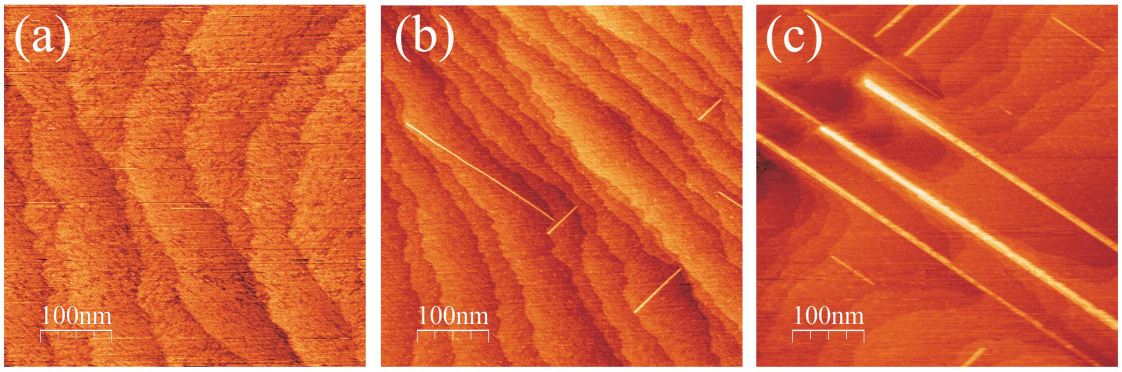


Figure 4.3: STM images illustrating the different sample morphologies at fixed coverage ($\theta = 0.35$ ML) but different growth temperatures. (a) At 600 °C the surface is almost completely covered with the (2×7) surface reconstruction and nanowires are still absent. (b) At slightly higher temperature, thin nanowires form and structural deformations in the wetting layer can be observed. (c) At 650 °C increased surface diffusion leads to wider and extremely long bundles and the (2×7) reconstruction has almost disappeared. The tunneling parameters are 0.07 nA, 1.4 V in (a), -1.8 V in (b) and 1.4 V in (c). Adopted from [4]

the surface of samples grown a this temperature. These structures can also be formed by post-growth annealing of the samples with ultrathin nanowires, showing the metastable nature of thin nanowires. As the substrate or the post-growth annealing temperature is increased to 670°C rectangular, quasi-2D islands can be observed. These islands exhibit a hexagonal AlB_2 structure, as inferred from the Moire patterns [4].

Samples annealed at 700°C or higher for 10 minutes exhibit only 3D silicide islands. Fig. 4.4 shows such islands which burrow through the silicon. These islands locally inhibit Si surface diffusion and one often observes step bunches near the islands. These 3D islands have a very low aspect ratio and a volume estimate from STM is difficult because they are partially buried under the Si surface. Both quasi-2D and 3D islands exhibit the c(2×2) reconstruction, as shown in the inset of Fig. 4.4 for a 3D island. A high density of vacancies is easily observable . Close inspection of the surface reveals the presence of ripples separated by 2.1 nm that may appear as a stress release effect. Similar observations were made for other rare earth silicides

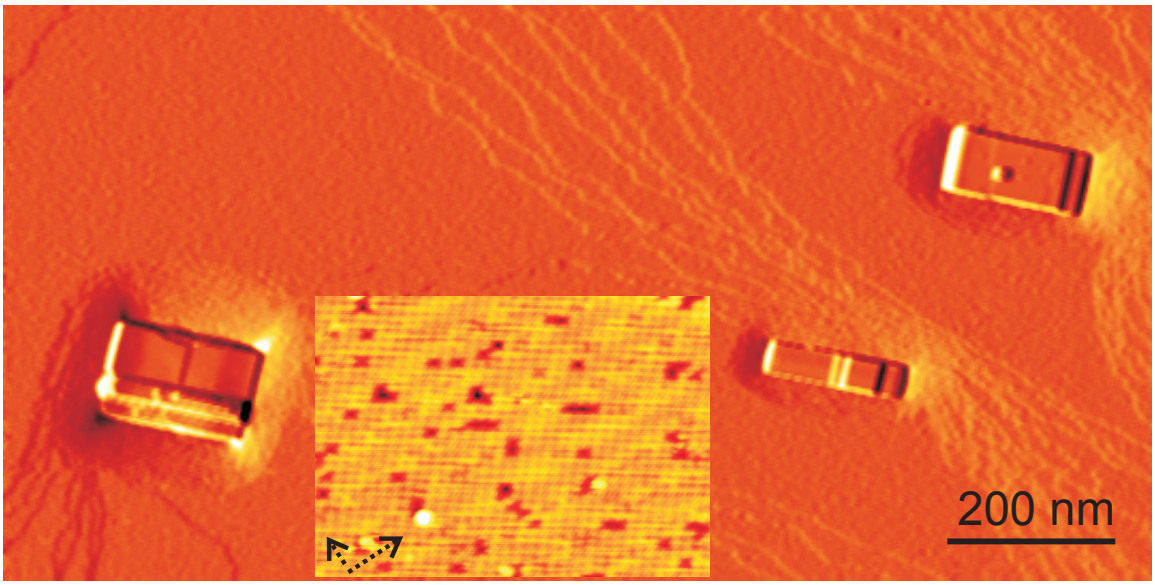


Figure 4.4: YSi_2 STM image showing several Type II YSi_2 islands. The inset shows an atomic resolution image (20 nm x 14 nm) of the type II island displaying a $c(2x2)$ surface reconstruction. Arrows indicate the orientation of the island's edges. Tunneling parameters are V_S=-1.2V, I_t=0.1 nA adopted from [4]

islands [71, 72]. TEM studies of similar $GdSi_2$ islands indicated that their structure is orthorhombic or tetragonal [71]. Based on the close resemblance of YSi_2 with $GdSi_2$, it is very likely that the 3D YSi_2 islands are orthorhombic [4]. Once they are formed the 3D islands are stable even at very high temperatures exceeding 1000°C.

4.1.3 RHEED Studies for Formation of Nanowires

As we discussed in the previous section, the formation of nanowires is strongly influenced by deposition time. During our studies we observed that the deposition and post annealing processes have to be completed within a few minutes to prevent bundle formation. It is very difficult, if not impossible, to observe such a fast process in real time with the STM. Such an observation requires specialized instruments [1]. Also, the high substrate temperatures required for the formation of nanowires further prohibits the use of our STM system, even if the growth process could be slowed down. Therefore, the STM studies employed for understanding the formation

of nanowires are limited to samples that were cooled down to room temperature. Even though they provide a detailed picture of the final product, STM images do not give any information about the growth dynamics. Questions such as " Do the (2×4) and (2×7) surface reconstructions form during growth at 625°C?" or "do they form as the result of a surface phase transition as the sample is cooled down?" cannot be answered with STM alone. On the other hand, RHEED provides a very good picture of the surface evolution during the growth (see section 3.3). The formation and evolution of different YSi_2 phases can be monitored with time resolution better than 100 ms at any substrate temperature.

Before discussing the details of nanowire formation as observed from the RHEED patterns, we will first look at the RHEED experiments performed at room temperature. Fig. 4.5 displays a series of RHEED patterns obtained from such samples, together with the simulated RHEED patterns of corresponding surface reconstruction. One should note that these RHEED images are high dynamic range (HDR) composite images formed by combining many images with different exposure times. While providing a clear picture of the faintest interference spot together with the brightest one, these images do not present the relative intensities of these spots and should not be used for quantitative statements. Such information can be obtained from the individual RHEED patterns shown in the appendix. Also the reader should note that the flat Si(100) surface and yttrium induced reconstruction always have two equivalent domains that are orthogonal to each other (i.e (2×1), (1×2) ;(4×2),(2×4); (2×7), (7×2)). For clarity, our discussion focusses on a single domain.

Fig.4.5(a) shows a RHEED pattern for clean the Si(100) surface with (1×2) and (2×1) reconstructed domains. Very sharp spots belonging to these reconstructions are clearly visible. Additional spots seen at $(\frac{1}{2} \pm \frac{1}{2})$ have a relative intensity of less than one percent, thus showing the capabilities of the RHEED technique. Fig. 4.5(c) shows the RHEED pattern of the yttrium induced Si(100)(2×4)-Y surface reconstruction, obtained from a sample with an yttrium coverage of $\theta = 0.15$ ML. At this coverage, the (2×7) reconstruction is not yet visible. On the other hand, the (2×4) spots completely

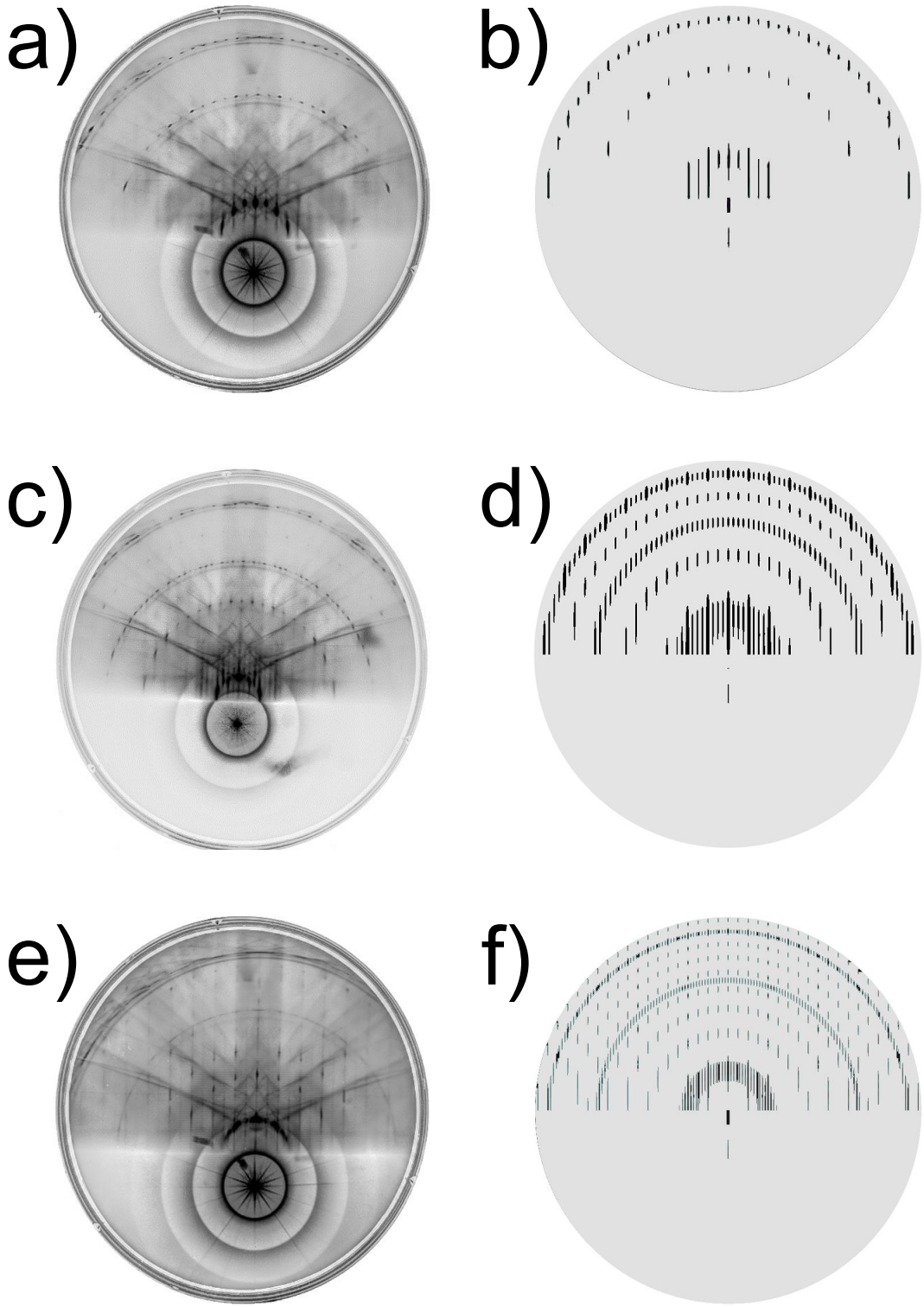


Figure 4.5: Experimental (a) and Simulated (b) RHEED patterns for the clean Si(100)(2×1) surface; the yttrium induced Si(100)(4×2) surface (c,d); and the yttrium induced Si(100)(7×2) surface (e,f). The beam voltage is 15 kV and the incident beam direction is along [011].

disappear at (θ =0.35) and only the (2×7) diffraction spots are visible. At this stage streaks produced by the nanowires are not clearly distinguishable (see Fig.4.5(e)). The STM and RHEED data recorded at room temperature are in excellent agreement.

In order to study the formation of nanowires in real time, we recorded consecutive RHEED images during yttrium deposition at 625°C. Since the RHEED intensities decrease significantly at elevated substrate temperatures, we focused on the 0^{th} Laue zone where the diffraction spots are brightest. To see the effects of post deposition annealing, the samples were annealed for 15 more seconds after the deposition was stopped, and subsequently quenched to room temperature. Fig.4.6 shows a series of selected RHEED patterns obtained during this process and Fig.4.7 shows the intensity of selected spots as a function of yttrium coverage. A complete set of images obtained during growth and used for calculating the spot intensities can be found in the appendix.

RHEED patterns and spot intensities presented in Fig 4.6 and Fig. 4.7 give a clear picture of the surface evolution during deposition. The intensity of the sharp (1/2,0) spots of the clean Si(100) (2×1) surface decreases immediately when opening the effusion-cell shutter. This behavior can be explained with the disorder introduced by the yttrium adatoms. Spots belonging to the (4×2) reconstruction appear just after 0.10 ML of yttrium is deposited and their intensity rises quickly between 0.1 and 0.15 ML of yttrium coverage. However, the intensity of the (4×2) spots start to decrease with the onset of the (7×2) spots, thus revealing a transition from the (4×2) to (7×2) reconstruction with additional yttrium. Starting from 0.15 ML, the intensity of the (7×2) spots rises very quickly and reaches maximum intensity at ($0.28 \leq \theta \leq 0.35$) where the intensity of (6/7,0) peaks saturate the camera. As diffuse streaks originating from the nanowires appear, the intensity of the other (7×2) spots (not shown) begin to decrease indicating that the (7×2) surface covers the entire surface and cannot extend anymore. The decrease in the spot intensity can be explained with the disorder introduced by the nanowires, dividing the wetting layer

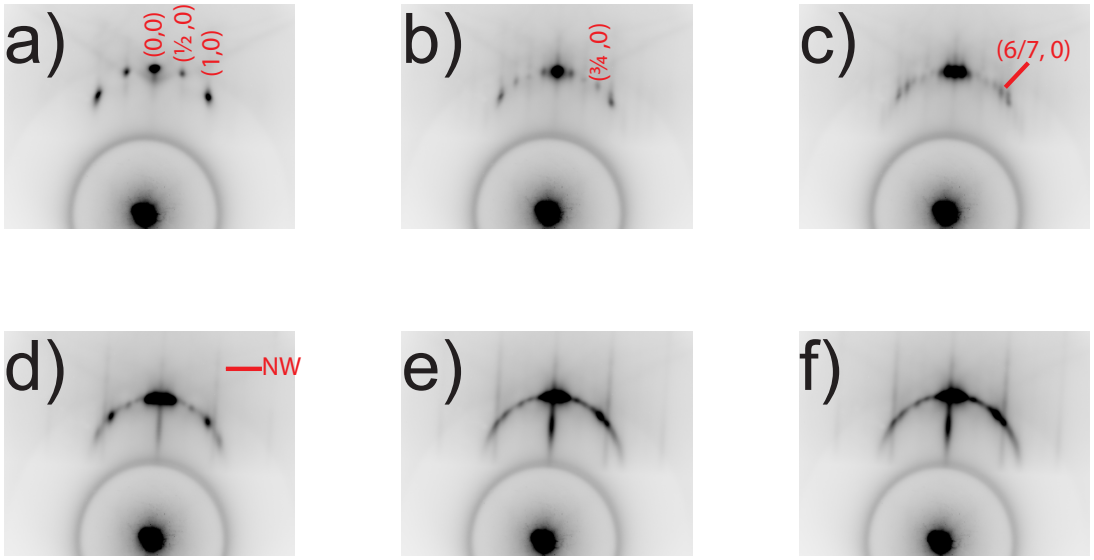


Figure 4.6: Selected RHEED patterns recorded at different yttrium coverages (θ) during growth. (a) Clean Si(100)(2×1) surface θ=0; (b) θ=0.14 ML; (c) θ=0.21 ML; (d) θ=0.40 ML; (e) θ=0.57 ML + 5 second post annealing; and (f) θ=0.57 ML, quenched sample. Spots used for intensity monitoring are marked. The beam voltage is 15 kV and the incident beam direction is along the Si [011] direction.

into smaller segments. This observation supports our STM findings and our claim that the nanowires only form after completion of the (7×2) wetting layer.

Once the deposition is stopped but the sample is still held at 625°C for post deposition annealing, we observe a faster pace of decrease in the intensity of the (7×2) spots.The intensity of the nanowire streaks also starts to decrease. All of the spot intensities increase very sharply as soon as the sample is quenched.

The observations summarized above show that the wetting layer and nanowires are formed during deposition, not during cool down. They also reveal the complex dynamics of nanowire growth and contribute to our understanding of the growth process.

Our discussion concerning the formation of nanowires can be summarized with a schematic diagram given in Fig. 4.8, which illustrates the various stages of YSi_2 nanostructure formation for different coverages and growth temperatures [4]. The illustration should not be taken as a true phase diagram, since the exact compositions

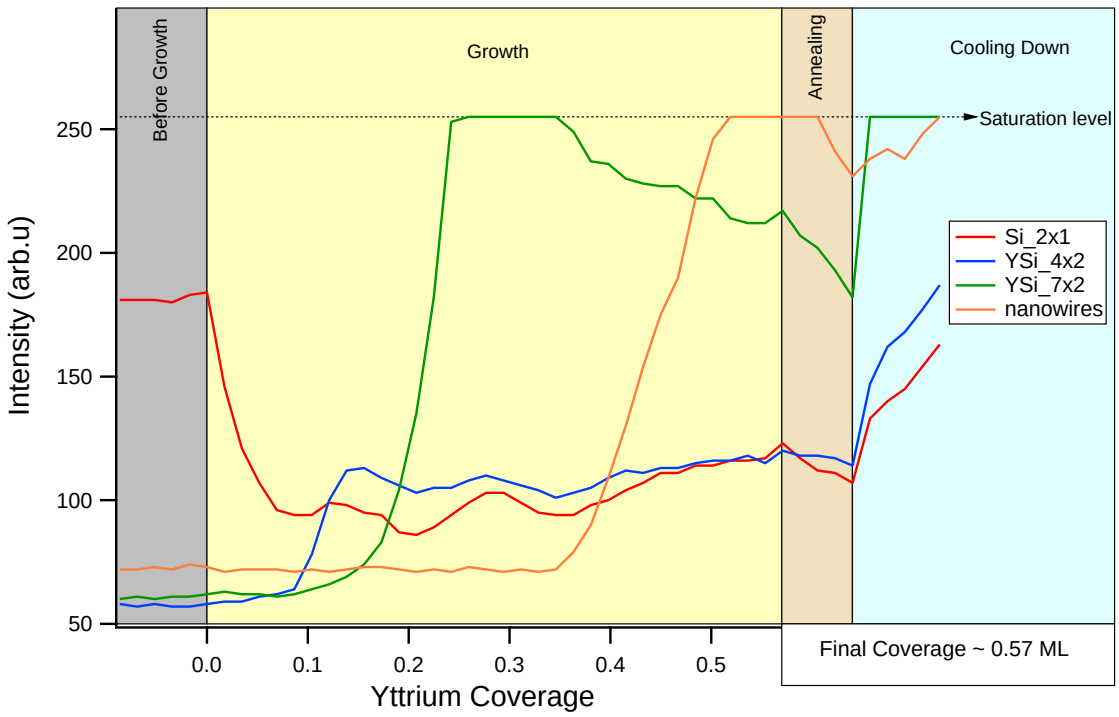


Figure 4.7: Intensity of selected RHEED spot during yttrium deposition. The beam voltage is 15 kV.

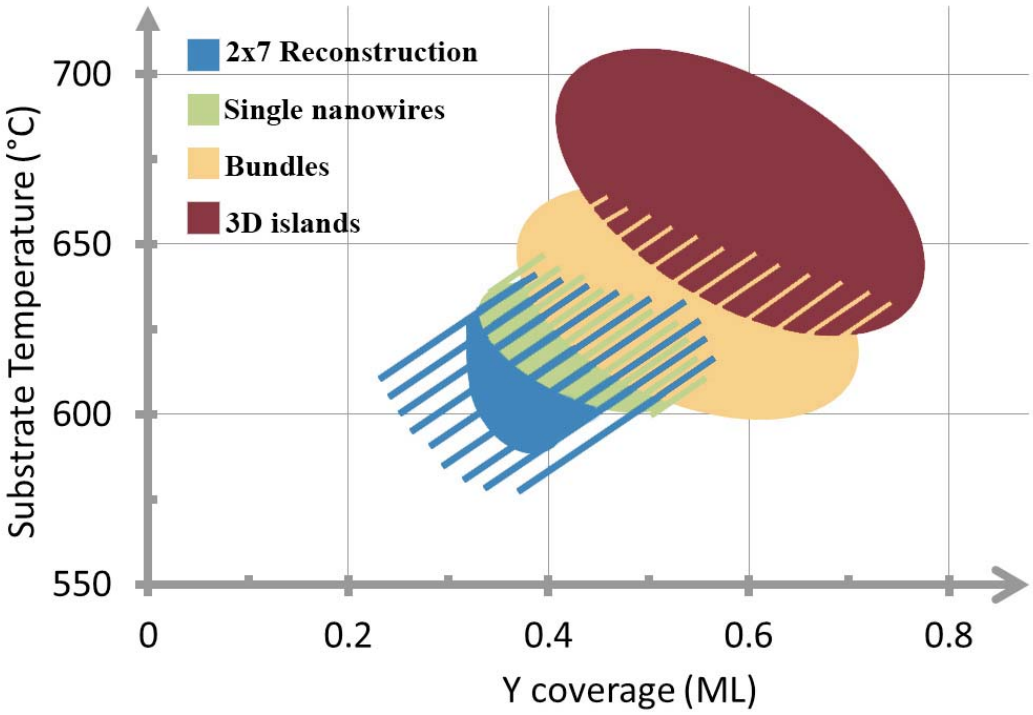


Figure 4.8: YSi_2 structures observed at different yttrium coverages and substrate temperatures. Solid colors indicate the dominant structures while stripes indicate mixed phases. [4]

and homogeneity ranges of the various nanostructures are unknown. Furthermore, most structures are non-equilibrium structures. The occasionally observed (2×4) wetting layer patches and the clean Si(100)(2×1) reconstruction have been omitted for clarity, so as to better highlight the main features.

4.1.4 Structure and Electronic Properties of Ultrathin YSi_2 Nanowires on Si(100)

As we discussed in section 4.1.2, ultrathin nanowires are formed at low yttrium coverage ($0.4 \leq \theta \leq 0.5$), when the total length of the deposition and post annealing time is kept below 3 minutes [5, 4] . An STM image showing such wires is presented in Fig.4.9. The single nanowires in Fig.4.9 have discrete widths that vary between

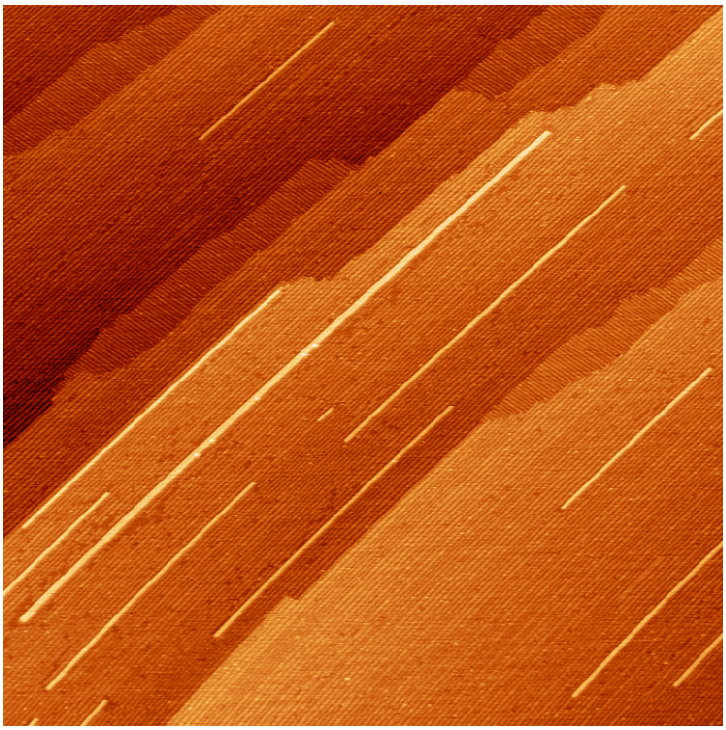


Figure 4.9: STM image of ultrathin YSi_2 nanowires. Nanowires of various thicknesses starting form $3a_0$ can be observed. Image size: 500 × 500 nm

$3a_0$ and $7a_0$ where a_0 is the in-plane Si lattice constant (0.384 nm) [5]. Due to their extremely small size these nanowires can not be studied by transmission electron microscopy (TEM). Fortunately, combined with the anisotropic growth model discussed in Section 2.1 high resolution STM images can provide a starting point to determine the structure of these nanowires. However, the STM images contain both topological and electronic structure information which are not easy to decouple [73]. Therefore, the structure of the nanowires has to be determined by comparing the experimental STM images and STS data with simulated topographic images and dI/dV spectra obtained from first principles density functional theory (DFT) calculations. The structure and electronic properties of thinnest nanowires have been well studied with this method and were shown to represent a very close realization of a 1D electronic system.[5, 4, 70]

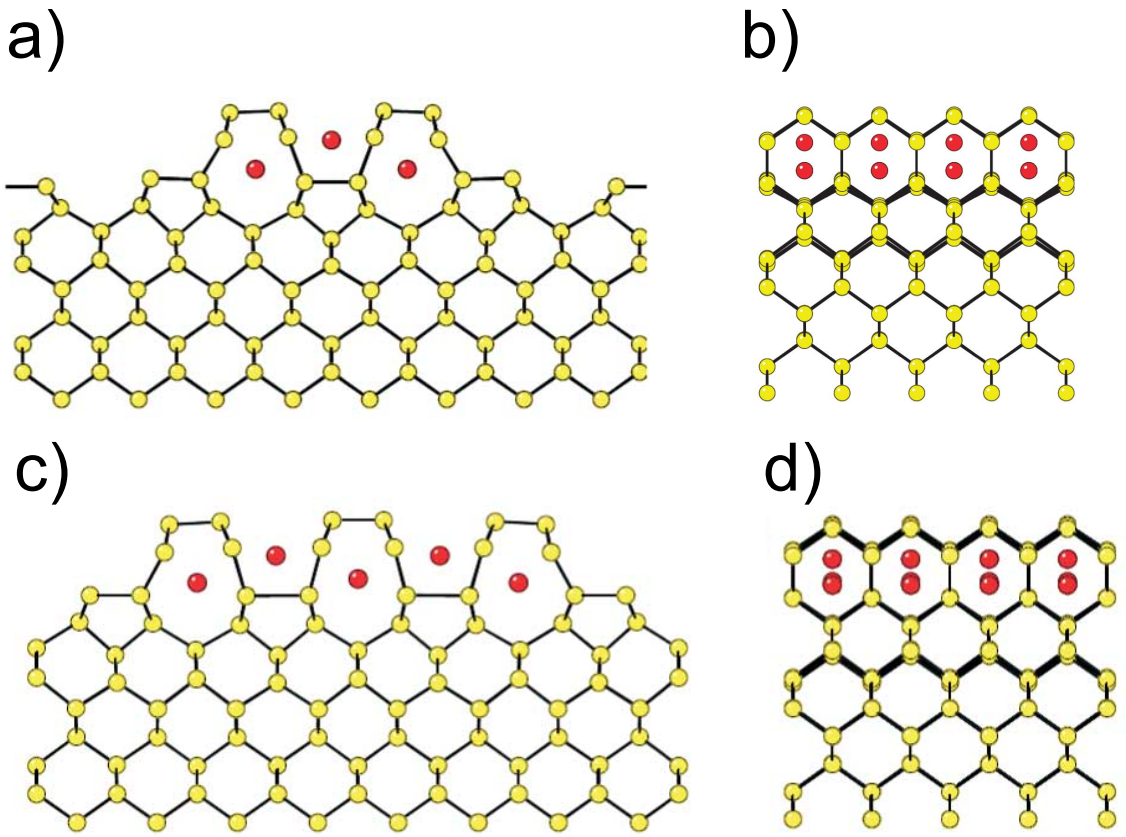


Figure 4.10: Structure models of ultrathin YSi_2 nanowires. (a) Cross sectional and (b) side view of total energy minimized structure of a $3a_0$ nanowire. A similar structure can be derived for the $5a_0$ nanowires. Adopted from [5, 4]

The thinnest nanowires in Fig.4.9 have a cross section of 0.4×1.15 nm^2. Hence they are named as $3a_0$ nanowires [5]. These nanowires exhibit van Hove type singularities in the one-dimensional density of states and charge-order fluctuations below 150 K[5]. STS measurements on these nanowires indicate that they have a metallic density of states at room temperature. A detailed examination of the calculated electronic structure shows that the STS peaks derive from tunneling through near-band-edge hybridized YSi *sp* states that are localized along the wire while decaying into the bulk substrate, as shown in Fig. 4.11 [5].

Wires with odd-multiple wire widths ($3a_0$, $5a_0$) exhibit mirror plane symmetry [5, 4, 70]. Here, the mirror plane is defined by the [1120] direction of the hexagonal silicide and the surface normal. On the other hand, the even-multiple wires ($4a_0$,

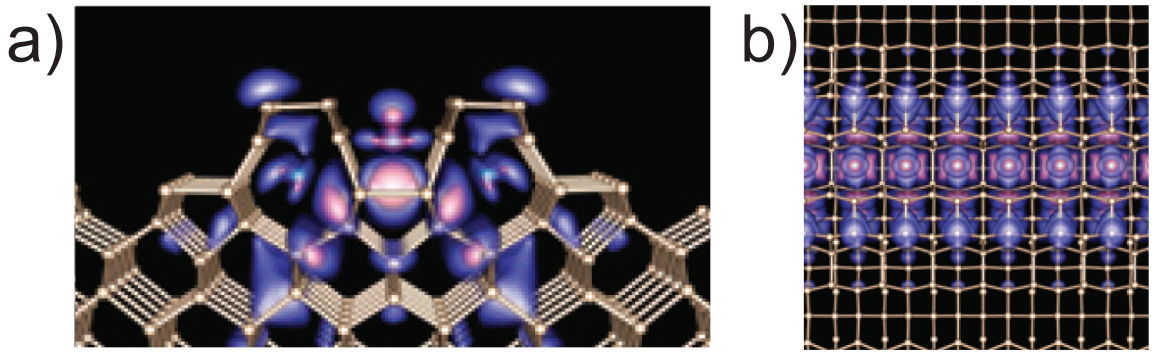


Figure 4.11: Top view and cross-sectional view of the calculated wavefunction densities on the $3a_0$-wide YSi_2 nanowire. Blue and magenta represent 30% and 70% wavefunction density isosurfaces respectively. adapted from [5]

$6a_0$) do not have mirror plane symmetry [5, 70]. The absence of mirror plane greatly increases the number of possible candidates for the structural model. However, a careful analysis of STS data and calculated density of states produced a strongly preferred candidate model for the $4a_0$ wire [70]. Like the odd-multiple wires, the even-multiple nanowires show a metallic density of states at room temperature.[70]

$5a_0$ nanowires are also commonly observed. Thermodynamic analysis of their relative stability shows that $5a_0$ nanowires are the most stable among the thinest nanowires. Their formation energy is 0.11 and 0.32 eV less than that of the $3a_0$ and $4a_0$ wires, respectively [70]. They exhibit a $\times 2$ periodicity along the wire direction which has not be seen in thinner wires [5, 4]. Furthermore, the $5a_0$ nanowires exhibit several surface reconstructions, making the structure determination much more complicated. The structure model (Fig. 4.10) derived from the previously introduced model of the $3a_0$ wires fails to reproduce the observed period doubling along the wire [4]. On the other hand, structure models with ordered yttrium vacancies can capture the $\times 2$ periodicity and produce simulated STM images that are in quite good agreement with the experimental ones.

In addition to the existence of periodic yttrium vacancies, $5a_0$ nanowires also exhibit a high density of adatom and other vacancy defects [4, 21]. A detailed analysis of these defects with STM gives a density of one defect per 6 nm [21]. These

defects may also introduce other local surface reconstructions on the nanowires [4] and possibly create phase shifts in the ytrrium vacancy ordering. The lack of a long range $\times 2$ ordering is also visible in the RHEED images, which show very clear streaks passing through the Si(0,1) spots while the ones passing though the $(0,\pm\frac{1}{2})$ position are missing. The existence and abundance of these defects has a significant influence on the transport properties of these wires, as will be discussed in Chapter 6.

4.2 YSi_2 Nanowires on Si(110)

In the previous chapter we have seen that silicide nanowires with extreme aspect ratios can be grown on Si(100) where the highly anisotropic lattice-match between the Si(100) substrate and silicide layer favors 1D growth [5, 28, 24, 19, 25, 4]. However, because the Si(100) surface is four-fold symmetric, nanowires on cascading single-step terraces are always perpendicular to one another, which could be a significant drawback for practical applications. On the other hand, the Si(110) surface is two-fold symmetric and should therefore be a better candidate for growing nanowires that are always parallel to each other. Indeed, uni-directional growth of silicide nanowires on Si(110) has already been demonstrated with several metals including Co,[74] Dy,[75] Ag,[76] and Gd [77]. However, these nanowires were either thick endoxial nanowires, [74, 75, 78] or they coalesced into a two-dimensional array of nanowires with very small, non-tunable wire spacing [76, 77].

In this Section, we will show that metallic YSi_2 nanowires with cross sections as small as 1.5 nm^2 can be grown in a single orientation on Si(110). After a short description of sample preparation we will discuss the structure of the nanowires together with the reconstructed Si(110)-$(2\sqrt{3}\times\sqrt{3})R54.7°$-Y semiconductor surface layer accompanying them. Finally, we will show the possibility of tuning the interwire distance by varying the miscut angle of the substrate wafer.

4.2.1 Sample Preparation and Nanowire Growth on Si(110)

A sample preparation procedure similar to the Si(100) substrates was followed for the Si(110) substrates. n-type Si(110) substrates ($\sim 2\Omega$ cm) were outgassed at 550°C for several hours, then flashed at 1250°C for about 30 seconds, while maintaining the system pressure below 1×10^{-9} mbar. The samples were post annealed at 750°C for 10 minutes and slowly cooled to room temperature.[79, 80] The formation of an atomically clean Si(110)16×2 surface was confirmed with STM and RHEED. The thinnest nanowires discussed in this section were formed by depositing 0.20 to 0.25 monolayer (ML) of yttrium onto the atomically clean substrate at 550°C (1 ML$\approx4.8\times10^{14}$ atoms/cm^2). The deposition rate of 0.4 ML min^{-1} was calibrated from the exposure needed to complete the well-known 2×7 yttrium-induced reconstruction on Si(100).[4] The nanowire samples were quenched to room temperature so as to prevent the formation of thicker nanowires.

4.2.2 Structure of Ultrathin YSi_2 Nanowires on Si(110)

The uni-directional growth of the YSi_2 nanowires over macroscopic areas of the Si(110) surface was confirmed with RHEED, as will be discussed later. A large area STM image of the nanowires (Fig. 4.12(a)) also reveals that all nanowires are elongated along the $[1\bar{1}0]$ direction of the Si substrate. Higher magnification STM images show that the widths of individual nanowires range from 3.0 to 7.0 nm. Occasionally, one observes nanowire bundles on the surface. Fig. 4.12(b) shows a STM image of the thinnest YSi_2 nanowires observed. These nanowires have a cross-sectional area of $\sim (30\times5)$Å^2 and may grow up to several hundred nanometers in length. They have straight edges and atomically flat surfaces along their entire length. However, we have not been able to acquire atomic resolution images from these wires, presumably because of their small metallic corrugation.

Similar to the case of rare-earth silicide nanowires on Si(100), the quasi one-dimensional growth of YSi_2 nanowires on Si(110) is attributed to the anisotropic

lattice mismatch between the hexagonal AlB_2-type structure of the bulk silicide and the Si(110) surface. In the case of YSi_2, the silicide lattice constant along the $[11\bar{2}0]$ direction matches almost perfectly (∼0.05% mismatch) to the Si lattice constant along its $[1\bar{1}0]$ direction, while the mismatch along the orthogonal direction is ∼31%. It is interesting to note that the latter mismatch creates a beating period of 1.63 nm ($3\times a_{Si} \approx 4\times c_{YSi_2}$) which is very close to the half-width of the thinnest nanowires.

High-resolution STM images shown in Fig. 4.13 indicate that the nanowires are surrounded by a $(2\sqrt{3}\times\sqrt{3})$ $R54.7°$ surface reconstruction. A second surface domain, which is the mirror image of the first one about the $[1\bar{1}0]$ axis (namely $(\sqrt{6}\times\sqrt{6})R35.3°$) was also observed. The surface of neighboring terraces are randomly decorated with one of these reconstructions. While filled-state STM images show a clear periodicity (with defects), empty states images (Fig.4.13(b)) do not show a clear periodic structure.

The RHEED patterns in Fig.4.14 clearly show all of the super-lattice spots related to $(2\sqrt{3}\times\sqrt{3})R54.7°$ and $(\sqrt{6}\times\sqrt{6})R35.3°$ domains. There are no additional spots. The other notable features in the RHEED patterns are the curved parallel streaks [81]. They are associated with the strictly one-dimensional periodicity of the nanowires. These streaks pass through the Si 1×1 spots indicating that the nanowires are crystalline and that the silicide lattice constant along the growth direction exactly matches that of the Si(110) substrate, consistent with the proposed hexagonal AlB_2-type structure of the nanowires. When the incident electron beam is perpendicular to the nanowires (i.e [001]) the curved lines completely disappear (Fig. 4.14(b)). The RHEED observations thus clearly confirm that the nanowires all grow in the same direction over macroscopic areas and that the nanowires are crystalline and epitaxial.

Once the Si(110)-$(2\sqrt{3}\times\sqrt{3})R54.7°$ surface is formed, the surface cannot be reverted back to its pristine (16 × 2) structure by flashing the sample at 1250° C. Mesoscopic scale STM images of the flashed surface do not reveal any nanowires or island formations. Higher resolution images show that the yttrium-induced surface reconstruction between the nanowires remains preserved. RHEED patterns of the

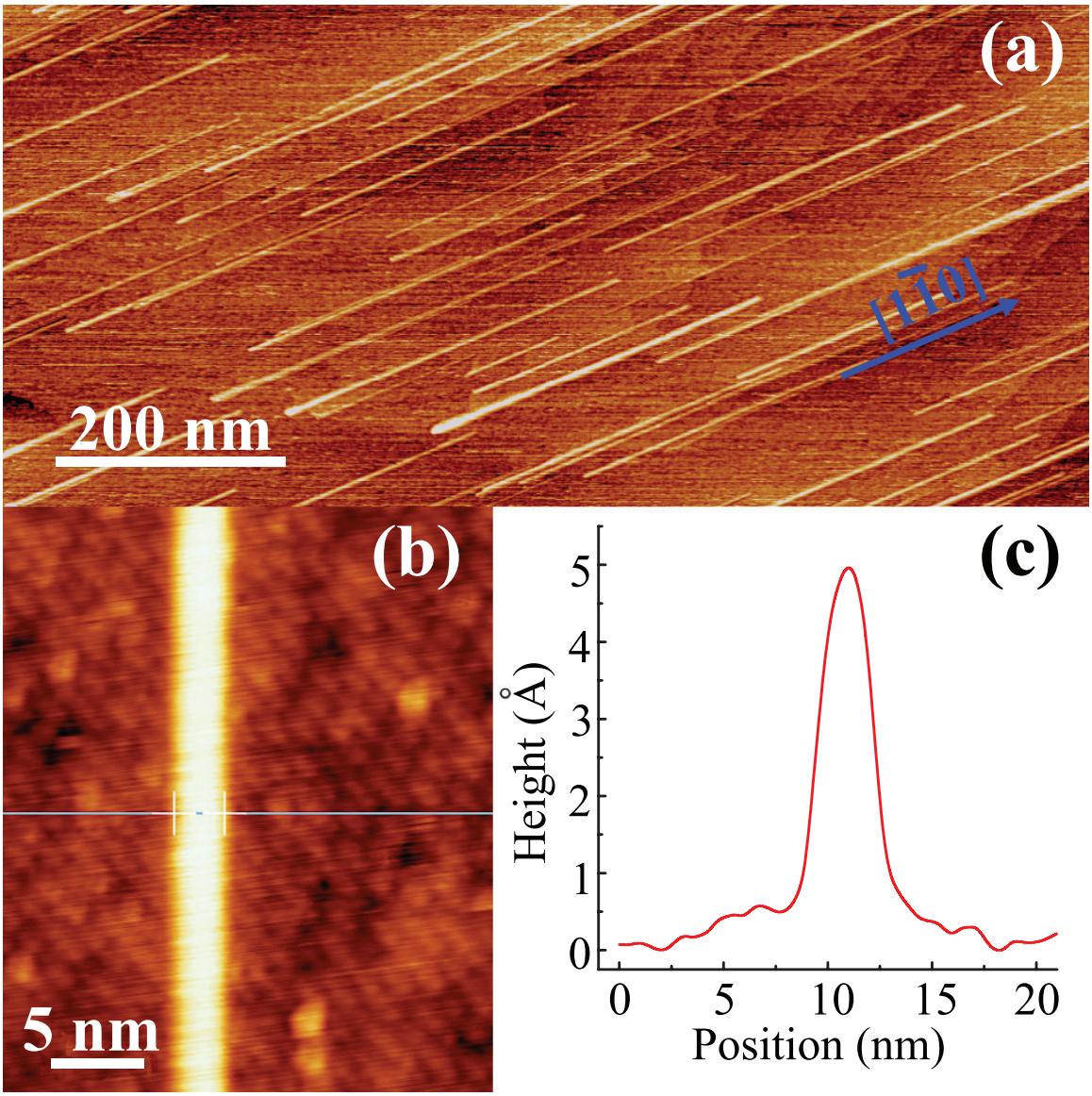


Figure 4.12: (a) STM image of individual YSi_2 nanowires on Si(110) after depositing 0.2 ML of yttrium (V_S =1.5V I_t= 0.05nA). Nanowires grow unidirectionally along the Si [1$\bar{1}$0] direction. (b) STM image of the thinnest nanowires (V_S =-1.5V I_t= 0.1nA). (c) Averaged cross-sectional line profile on the thinnest YSi_2 nanowire.[6]

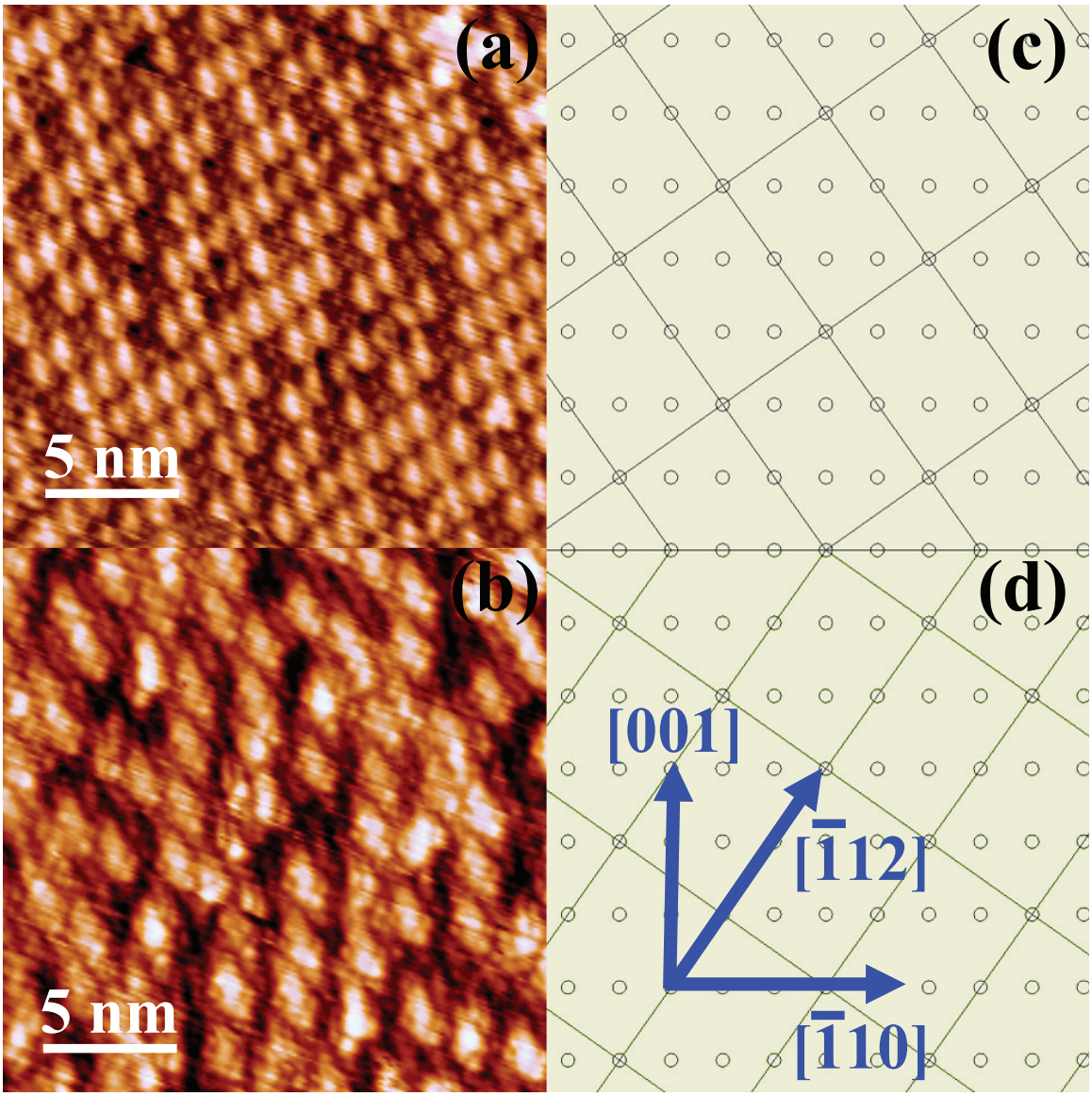


Figure 4.13: Dual-polarity STM images of the surface in between the YSi_2 nanowires: (a) Filled state (V_S =-2V I_t= 0.1nA) and (b) empty state (V_S =2V I_t= 0.1nA) image of the same region. (c,d) Illustration of the observed Si(110)-$(\sqrt{6}\times\sqrt{6})R35.3°$ and $(2\sqrt{3}\ \times\sqrt{3})R54.7°$ surface reconstructions. Open circles represent the Si(110)1×1 lattice.

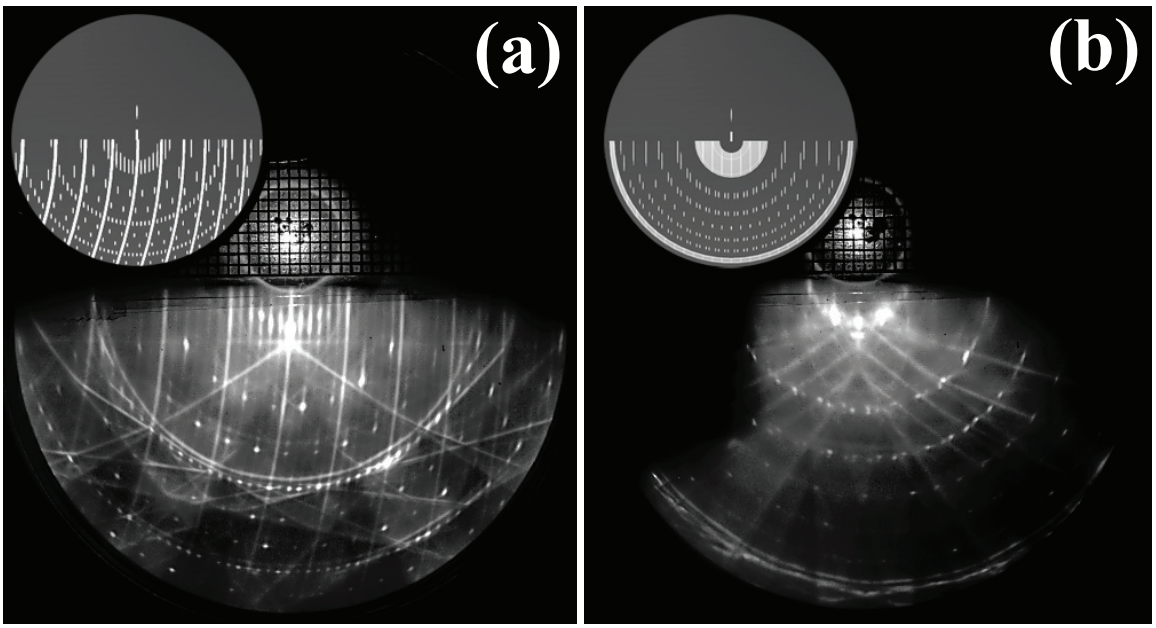


Figure 4.14: RHEED pattern of the nanowire-covered surface along the (a) $[1\bar{1}1]$ and (b) $[1\bar{1}0]$ direction, together with the calculated RHEED patterns for Si(110)-$(2\sqrt{3}\times\sqrt{3})R54.7°$-Y surface reconstruction with epitaxial nanowires (insets). The beam voltage is 15 kV.

flashed surface are identical to those of Fig. 4.14, except for the absence of the curved streaks. Similar observations were made for submonolayer amounts of Ni,[3] Ag,[76] and other metals on Si(110). In those cases, minute metal amounts or metal 'contaminants' produce 5×1 and several other n×1 surface reconstructions. However, the $(2\sqrt{3}\times\sqrt{3})R54.7°$ reconstruction observed here has not been reported before.

STS measurements taken on top of the YSi_2 nanowires and surrounding surface reconstruction are presented in Fig. 4.15. The experimental I-V spectra and the corresponding differential conductance ($\mathrm{d}I/\mathrm{d}V$) spectra indicate that the nanowires are metallic at room temperature, while the surface in between the nanowires is semiconducting with a band gap of ~ 0.8 eV. The band gap of the flashed surface is similar.

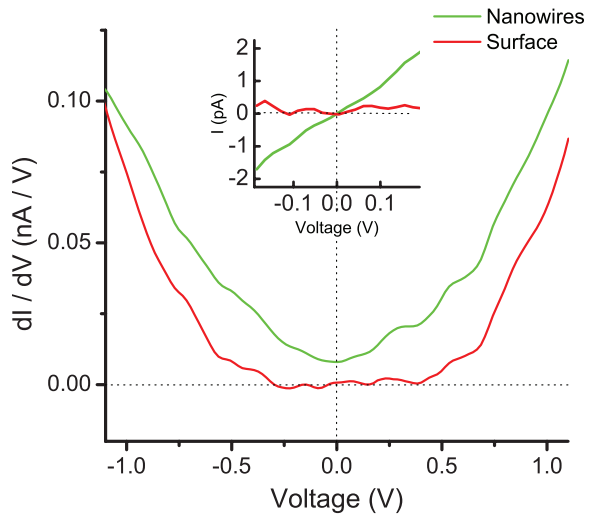


Figure 4.15: Averaged $\mathrm{d}I/\mathrm{d}V$ curves of the YSi_2 nanowires (green curves) and adjacent substrate area (red curves). The inset shows the I-V curve near zero bias. Tunnelling set point: (V_S =1.5V I_t= 0.1nA)

4.2.3 Preferential Growth of YSi_2 Nanowires on Terrace Edges

On the Si (110) surface, the nanowires are always oriented along the $[1\bar{1}0]$ direction of silicon, regardless of the surface domain or terrace-edge orientation. However, we observed that the nanowires show a clear preference of growing near surface defects, such as domain boundaries or terrace edges, particularly when these edges are also oriented along the $[1\bar{1}0]$ growth direction. Fig. 4.16 illustrates such a case, in which the YSi_2 nanowires grow along step edges that are almost parallel to the $[1\bar{1}0]$ direction. Such a behavior is welcome since it may provide an avenue to control the wire separation by using vicinal silicon surfaces. Alternatively, it should be possible to control the wire position via creation of artificial defects on the surface.

To further illustrate the unidirectional growth on vicinal Si(110) surfaces we have grown YSi_2 nanowires on the Si(331) surface. Ideally a miscut Si wafer with terrace edges oriented along the $[1\bar{1}0]$ should have a Si(xx1) surface where arctan(1/x) is the miscut angle. Therefore, the Si(331) surface can be considered as an extreme case of miscut Si(110) with an miscut angle of 18.4 °. Fig.4.17 shows YSi_2 nanowires grown

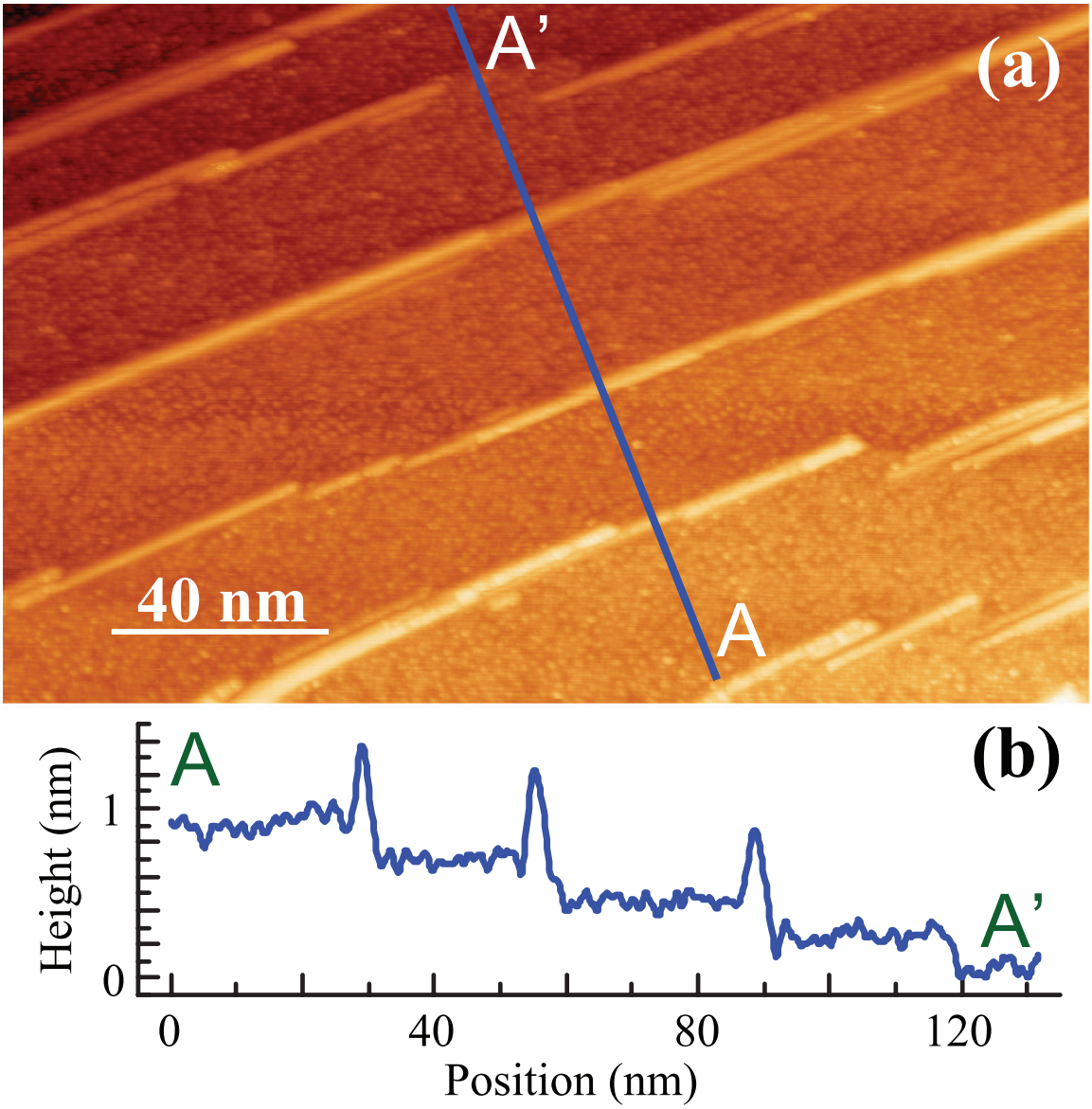


Figure 4.16: YSi_2 nanowires on a Si (110) surface with terrace edges almost parallel to the $[1\bar{1}0]$ direction. (V_S =1.5V I_t= 0.1nA) (b) Cross-sectional height profile perpendicular to nanowires. The nanowires exhibit a clear preference of growing at the terrace edges.

Si(331) surface and illustrates that the unidirectional growth is persistent even at very high miscut angles. The nanowires shown in this STM image are relatively thick wires with cross sections of 5.0 ± 2.0 nm. It is very likely that thinner nanowires can be obtained by fine tuning the growth parameters as we did for Si(110) surface.

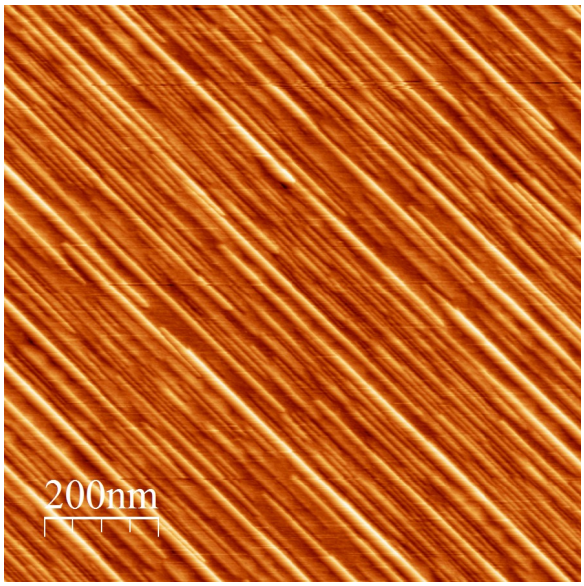


Figure 4.17: YSi_2 nanowires on a Si(331) surface shows a unidirectional growth (V_S =1.5V I_t= 0.1nA)

In conclusion, ultrathin metallic YSi_2 nanowires can be grown in a single orientation on Si(110). The nanowires are crystalline and epitaxial and their formation is driven by anisotropic lattice mismatch between the silicide and silicon lattices. The wires are embedded in a non-metallic yttrium-induced Si(110)-$(2\sqrt{3}\times\sqrt{3})R54.7°$-Y reconstruction. They may have great potential for practical applications because of their preference to be seeded at surface defects, such as point defects and step edges, and because of the possibility of controlling the interwire spacing using intentionally-miscut silicon substrates.

Chapter 5

Electron Transport in Low Dimensions

In this chapter we will discuss various electronic transport models, starting with the classical Drude model for a 3D metal and ultimately addressing quantum mechanical transport in 1D.

5.1 Electron Transport in 3D Materials

In order to understand the basics of electron transport in reduced dimension, we should first look at the classical transport model for electrons moving in three dimensions. The first microscopic theory to explain Ohm's empirical law was proposed by Paul Drude in 1900, just a few years after the discovery of the electron. Drude assumed that a metal is composed of fixed, positively charged ions and of free electrons [82]. The only interaction considered for these free electrons is their instantaneous collision with the stationary ions. Therefore, in the absence of an external electric field, an electron moves with a constant velocity v_o in between these collisions. After each collision v_o has a random magnitude and direction. Hence, no net current is generated. The average time τ between consecutive collisions is called the relaxation

time. On the other hand, in the presence of an external electric field E, electrons are accelerated after each collision. Their velocity in between collisions can be given as

$$v = v_0 + v_d \tag{5.1}$$

$$v(t) = v_0 + \frac{eE(t - t_0)}{m} \tag{5.2}$$

where e and m are the charge and mass of the electron, respectively, and t_o is the time of the last collision. While v_o has a random direction v_d always has a direction opposite to the external electric field. If there are n electrons per unit volume, then the current density can be written as

$$J = nev_d = ne^2\tau E/m \tag{5.3}$$

the above equation predicts that the current density is proportional to the applied voltage as is well known from Ohm's law (i.e. $J = \sigma E$). Hence we identify

$$\sigma = ne^2\tau/m \tag{5.4}$$

where σ is the conductivity.

The classical Drude model partially explains the microscopic origin of Ohms law. However it falls short of explaining a large number of physical properties including the specific heat of a metal. The main weakness of the Drude model is that it treats electrons as a classical particle obeying Maxwell-Boltzmann statistics. A correction was offered by Sommerfeld, who introduced the Pauli exclusion principle and Fermi Dirac statistics to the problem, and established a relation between the electron density and Fermi wavevector. The density of the electrons in a macroscopic metal cube was found to be

$$n = \frac{k_F^3}{3\pi^2} \tag{5.5}$$

The new model, known as the Drude Sommerfeld model, successfully explained many other experimental observations [83]. The quantum mechanical treatment of free electrons also implies that their kinetic energy is quantized when they are confined to a finite size metal object [84, 85]. For instance, for a metal cubic with side L, the level spacing between the ground state and first excited state is

$$\Delta E = \frac{3h^2}{2mL^2} \tag{5.6}$$

Even though energy spacing is small for macroscopic sized objects (i.e. 4.5×10^{-12} eV for L =1mm), it will be significant for nano sized objects (179 meV for L =5 nm) [85]. Since the thermal energy of the electron k_BT is around 25 meV at room temperature, quantization effects cannot be ignored for transport at the nanoscale.

5.1.1 Limits of 3D Transport Models

Electronic conductivity is one of the most important properties when evaluating candidate materials for technological applications. However, these properties may be dramatically different for the bulk, thin film, or nanowire modification of a given material [14, 7]. Some of these property variations can be captured with classical transport models.

In our discussion of electronic transport in 3D, we assumed that electrons travel a mean free path l in between collisions with, e.g., phonos or random lattice defects. However, this approximation is no longer valid for electrons moving within close proximity of the metal surface. If an electron travels within a distance d from the surface and d is comparable to, or smaller than l, then it can also be scattered by the surface [86]. Hence, these electrons will have a smaller mean free path. For a macroscopic conductor the ratio of electrons satisfying the condition $d \lesssim l$ is negligible. However, as the thickness of the conductor approaches l its resistance may increase sharply due to surface scattering.

Initial studies of diffusive scattering at thin film boundaries were conducted by Fuchs and Sondheimer (F-S) [86, 87], who attempted to explain the relationship between the resistance and thickness of a thin film. The F-S model was also successfully used to calculate the resistance of wires for a variety of cross-sectional geometries [88, 89]. For instance, when surface scattering is considered the resistivity of a circular wire can be approximated as [87, 90]:

$$\frac{\rho_{FS}}{\rho_0} = 1 + \frac{3l}{4r}(1-p) \tag{5.7}$$

Where ρ_0 is the bulk resistivity with negligible surface effects, p is the fraction of electrons that are specularly reflected at the film surfaces, and r is the diameter of the wire.

Even though the F-S model showed very good agreement with measurements on micron sized films and wires, significant departures from this model were found once the wire diameters decreased below 1μm [91]. Mayadas-Shatzkes (M-S) [92] partially resolved this discrepancy by attributing the enhanced resistivity to grain boundary scattering. In metal films with thickness below 1μm the mean grain size is approximately equal to the film thickness. Hence, as the film thickness or wire diameter decreases, grain boundary scattering may dominate the resistance [92]. The M-S model has two important parameters, the average grain size D and the electron reflection coefficient R. D can be measured with electron microscopy and R can be calculated from the transport data [85].

According to the M-S model, the grain boundary contribution to the resistivity can be written as [92, 90]

$$\frac{\rho_{MS}}{\rho_0} = [1 - \frac{3\alpha}{2}(1 - 2\alpha + 2\alpha^2 ln(1 + \frac{1}{\alpha}))]^{-1} \tag{5.8}$$

where

$$\alpha = \frac{l}{D}(\frac{R}{1-R}) \tag{5.9}$$

Because surface and grain boundary scattering are statistically independent events their contributions to the resistivity can simply be added together using Mathiesens rule[93, 90]:

$$\rho = \rho_{FS} + \rho_{MS} \tag{5.10}$$

However, combining the surface and grain scattering contributions to the resistivity with other intrinsic contributions such as electron-phonon and electron-electron scattering requires a much more sophisticated analysis [85].

The F-S and M-S models successfully described the scaling of the resistivity with decreasing wire radius down to several tens of nanometers. However, they too fail as wire diameters continue to shrink towards the one dimensional limit. Because the overall behavior of electrons changes when they are confined to wires with diameters close to their Fermi wavelength. For instance, in the case of ultrathin YSi_2 nanowires, which are only few atoms wide, the thickness d $\ll l$ for every single electron and the electron wavevector in the radial direction of nanowire is quantized with large spacings.

On the other hand, defects play a much more important role in 1D systems. For these extremely small dimensions, every single defect can act as a grain boundary. The grains themselves are also very small ,therefore, the discrete nature of energy levels of the grains or defect centers should be considered when considering the transmission of electrons from one grain to the next. Finally, electron-electron interactions may give rise to exotic ground states in 1D, which also has profound implications for the transport mechanism.

5.2 Electron Transport in 1D Systems

5.2.1 1D Transport Models

As we mentioned in the previous section, classical models of electron transport can capture an essence of the relationship between the dimensionality of the system and its conductivity. However, they fail as the material approaches the 1D limit. In this section we will look at the electron transport models applicable to quasi-1D and 1D systems, where the transport can be examined in four different regimes [94] (a) ballistic, (b) diffusive, (c) Luttinger-liquid, (d) Anderson Localization. After summarizing the first two, we will have a closer look at Anderson localization since it is particularly important to understand the transport properties of the YSi_2 nanowires. The Luttinger-liquid regime will not be included because our transport studies were performed at room temperature while the Luttinger liquid signatures are usually observed at very low temperature. The YSi_2 nanowires are too resistive in this regime.

Electrical transport in 1D largely depends on three length parameters: The length of the nanowire (L), the localization length (L_0), and the coherence length (L_φ). L_0 is associated with the impurities in the system while L_φ is the dephasing length, which is determined by inelastic scattering processes. [94]

Ballistic Regime (Quantum Conductance)

Ballistic transport refers to a regime where the electrons are transported through a 1D channel without scattering. This happens when the length (L) of the 1D system is smaller than L_φ and L_0 [94]. The conductance of the channel can be derived from the Drude model. According to this classical model, the conductivity of a simple metal is given by Eq. 5.4. In the free electron model, the electron density of a one dimensional conductor is $2k_F/\pi$, where k_F is the Fermi wavevector. Therefore, for a one dimensional conductor of length L the conductance is given as

$$G = \frac{\sigma}{L} = \frac{2e^2}{h}(\frac{2v_F\tau}{L}) = \frac{2e^2}{h}T \tag{5.11}$$

Here, T is the transmission coefficient and v_F is the Fermi velocity. In the ideal case, where the electron collides with nothing but both ends of the conductor, $T = 1$, and the conductance becomes:

$$G = G_0 = \frac{2e^2}{h} \approx \frac{1}{12900}\Omega^{-1} \tag{5.12}$$

which is known as the quantum of conductance [95].

The quantum conductance only describes the ideal case of ballistic transport through a single channel. When plotting the conductance as a function of wire diameter, one often observes step like increases of the conductance (in units of G_0), as seen for instance in gold break junctions [96, 97] or in GaAs-AlGaAs heterostructures [98]. Each step corresponds to the opening of a new conduction channel. More generally, there are several channels and the transmission coefficient of each channel is often less than one. The electrical conductance in these systems can be given as a summation of the individual channel conductances, i.e.,

$$G = G_0 \sum_n T_n \tag{5.13}$$

where T_n is the transmission probability for the n^{th} channel [95, 15].

Diffusive Regime

1D electron transport in diffusive regime resembles the bulk conductance, where inelastic electron-phonon interaction dominates the conductivity and a linear relationship between the length of the quasi 1-D system and its resistance is expected. In this case L_φ is smaller than L and L_0.

Diffusive transport has been observed in long and almost defect free carbon nanotubes [99]. This study showed that at low bias voltages only the acoustic phonons

can be excited and the electron mean free path for acoustic phonon scattering is 650 nm. However, at higher bias voltages ($\geq$ 0.3V) optical phonons are also excited. Hence, a shorter mean free path and higher resistance is observed [99].

Anderson Localization Regime

Even though the defect free nanotubes exhibit ballistic or diffusive transport depending on their length, introduction of a small number of defects can qualitatively alter the transport mechanism by pushing the wires into the Anderson localization regime. It is well known that Anderson localization is inevitable in a disordered 1D system [100]. On the other hand, a crystalline quasi-1D system, such as a carbon nanotube or epitaxial nanowire, have very little disorder. In this case the density of defects on these wires determines the degree of localization and the so called the localization length L_0. If the defect density is high enough L_0 will be much smaller than L and L_φ and the system will be in strong Anderson localization regime. In this case, electrons will be localized by the random potential generated by defects and their wavefunctions will only extend over distances of the order of L_0. Electrons can be transported between the two ends of the nanowire only by a tunneling process. Hence, an exponential dependence of the nanowire resistance versus the length of the nanowire is expected [94]. i.e.

$$R = R_0 e^{(L/L_0)} \tag{5.14}$$

Strong Anderson localization has been observed and well-studied in carbon nanotubes [101, 102]. These studies showed that as grown carbon nanotubes usually exhibit a L_0 of the order of several hundred nanometers, which can be significantly reduced by creating defects on the nanotubes. Defects have been introduced by irradiating nanotubes with an Ar^+ ion beam. This method provided good control over the defect density of the nanotubes and enabled a systematic study of the defect density versus localization length in a quasi 1D system [101]. Theoretical calculations in this study,

which are in good agreement with the experimental data, predicted that L_0 should saturate around 23 nm if the average distance between the defects is less than 14 nm.

Anderson localization also predicts that at zero temperature conductance of 1D system will fluctuate [100]. However these fluctuations are washed out at room temperature [94].

Chapter 6

Electron Transport in YSi_2 Nanowires

The electronic transport properties of a given material often change in reduced dimensionality. However, the most dramatic change is expected to occur when it goes from being quasi one dimensional to being strictly one dimensional. Due to their large variety of cross sections, starting from just a few atoms wide, the rare-earth silicide nanowires are one of the very few platforms where this transition might be observed. Despite the technological and scientific importance of this transition, only few studies attempted to address this issue. Qin et al. [22] showed that interwire coupling in $GdSi_2$ nanowires stabilizes metallic conductance while isolated wires go through a metal insulator transition at low temperature. On the other hand, Iancu et al. [21] showed that the conductance in the YSi_2 nanowire bundles are thermally activated despite the metallic density of states observed in STS measurements. Furthermore, this study showed that transport through the nanowires is strongly influenced by trapped charges at local defect sites.

Even though the previous studies on YSi_2 nanowires [21] successfully revealed a correlation between the defect density and transport properties of nanowire bundles, Iancu *et al*. were unable to study the thinnest nanowires. They pursued an ex-situ

approach using EBID to define metallic contact pads for the transport measurements. This required a protective capping layer to be deposited on top of the nanowires before they were removed from UHV for contact fabrication in a different system. Albeit being very thin, this capping layer obstructs the view of the nanowires. Therefore, one never knows the precise structure and diameter of the wires that are in contact with the metal pads. The capping layer also prevented the observation of individual defects on the nanowire. Hence, a one-to-one matching between a particular defect and its influence on the electron transport is not possible.

Studying the transport in ultrathin nanowires and correlating it with individual defects requires an all in-situ approach. Moreover, performing transport measurements on ultra thin nanowires presents a great challenge, both technically and scientifically. Ideally one should seek to perform four-probe transport measurements to eliminate contact resistances. However, such a measurement is not an easy one for nanowires. Conventional probe stations, which are commonly used to measure the transport in thin films or mesoscopic structures, use optical microscopes with lateral resolutions several orders of magnitude smaller than the nanowire width. Therefore, a much more sophisticated probe station such as a 4-Probe STM [103] is required. Even with such a system the minimum distance between probes cannot be less then several hundred nanometers due to finite radius of curvature of the STM tips. Several attempts to overcome this problem utilized STM tips with carbon nanotubes or other metal nanostructures attached to their end [104]. These studies successfully measured the resistance of CoSi nanowires with a 4 probe configuration. However, these measurements were limited to thick and long endoxial nanowires. Transport measurements on ultra thin nanowires, on the other hand, have been only performed by using a 4-probe STM in a 2-probe configuration [22, 105].

A different approach for measuring the wire resistance employs only two probes with variable probe spacing. In this approach both the contact and wire resistance can be extrapolated from the resistance versus probe spacing measurements. Such a measurement can be performed with a single probe STM by fabricating a fixed contact

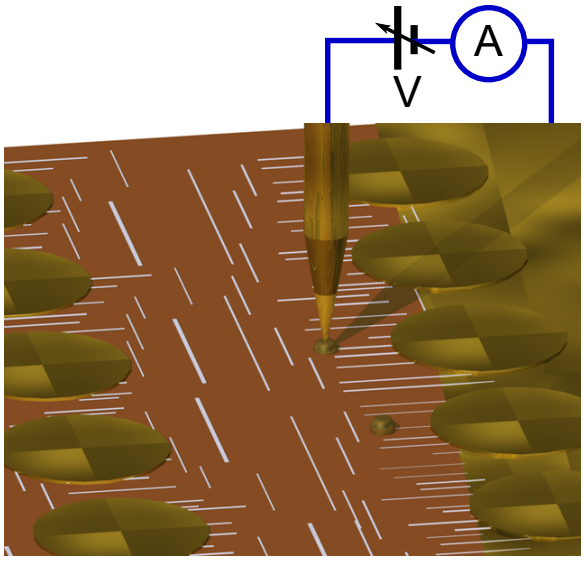


Figure 6.1: Illustration of transport measurements with a single probe STM. First a fixed macroscopic contact is deposited on one end of the nanowire. Then the STM tip is used as a second contact to study the electron transport as a function of distance from the first contact.

on one end of the nanowire, while using the STM tip as a second probe at various positions on the nanowire. This method is illustrated in Fig. 6.1. In addition to being compatible with our single probe STM, this method also offers the opportunity to study very short nanowire segments. Our studies showed that this capability is crucial because the wires have very high resistivity.

6.1 Sample Preparation for In-situ Transport Measurements

In order to fabricate the fixed contact on one end of the nanowire, we developed an in-situ contact deposition method compatible with our Omicron VT STM system. Two different approaches were used for this purpose. In the first one, summarized in Fig. 6.2, growth of the nanowires was followed by fabrication of metallic contacts with a two step shadow mask method. First, a rough shadow mask was employed for depositing a macroscopic contact between the nanowires and sample plate which

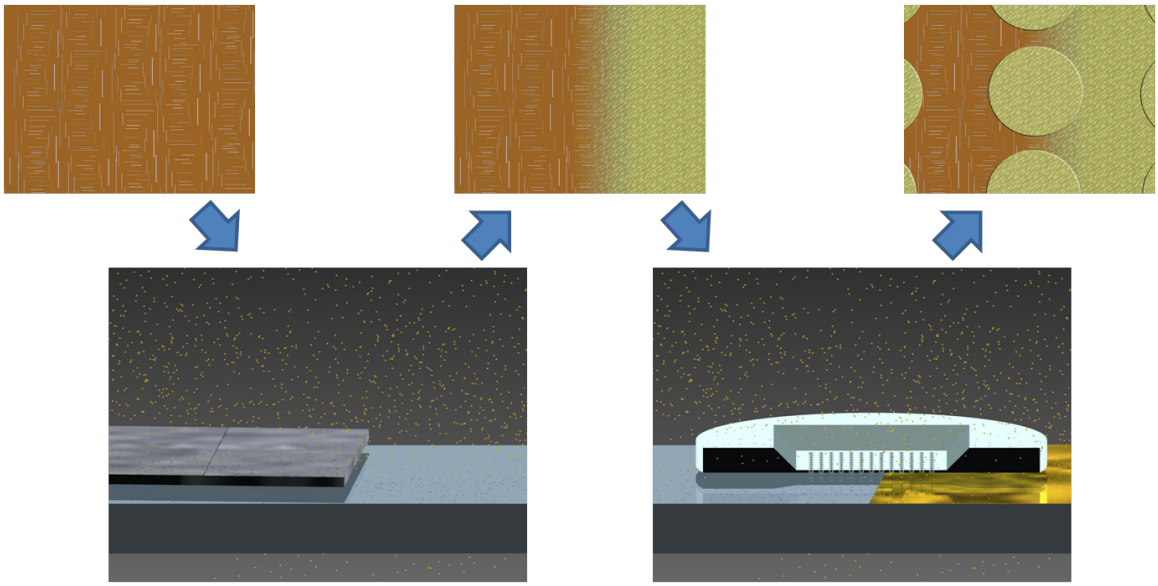


Figure 6.2: Illustration of contact deposition steps. After the YSi_2 nanowires are grown on the surface the first shadow mask is employed to deposit large electrical contacts between the wires and the sample plate. Then a stencil mask is used to create a sharp lateral boundary between the metal contacts and nanowires.

share the electrical ground with the STM. Such macroscopic contacts, when deposited with traditional shadow masks, do not have sharp boundaries. The sharpness of the boundary is determined by the thickness of the shadow mask and the distance between the mask and the sample surface. The high temperature process used during the cleaning of the silicon substrate limits the minimum value of these parameters. By optimizing the mask geometry shown in Fig. 6.3, we were able to decrease the width of the lateral boundary region between the metallic film and semiconductor surface below 1 μm. A very small Pt foil (1mm $\times$ 1mm $\times$ 25 μm) was placed between the sample and the molybdenum sample clamps to provide an ohmic contact between them. This foil formed a silicide on the Si (100) surface while alloying with the molybdenum clamp during the initial outgassing of sample and acts as a solder between the sample and clamp. Once the metal film is deposited, it also covers this Pt contact providing a ohmic contact between metal film and the sample clamps.

To further improve the sharpness of the metal film boundary, a shadow masking method known as stencil lithography [106] was employed. This method uses very

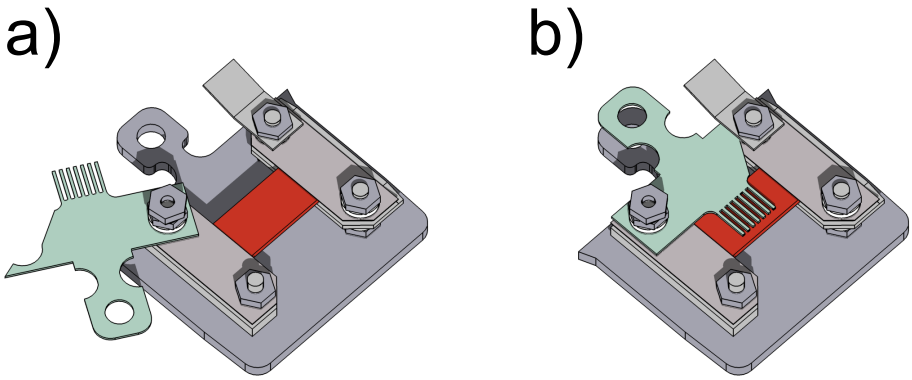


Figure 6.3: Optimized geometry of the first shadow mask (called a comb mask because of its shape). The mask is initially open (a) to allow sample cleaning and nanowire growth, closed (b) during metal contact deposition, and then opened again for the second step of the contact deposition and subsequent STM and transport experiments

thin ($\leq$ 200 nm) shadow masks to minimize the blurring caused by the finite thickness of the masks. Stencils are usually made of SiN membranes and the desired mask geometry can patterned with focused ion beam (FIB) milling. Our experiments did not require special contact geometries. Therefore, commercially available SiN membranes were used as stencils. We designed and built a small UHV chamber in which the stencil masks can be placed on the samples without damaging the nanowires. A metal evaporation source was placed at the bottom of this chamber to grow the desired patters through the stencil masks. The new chamber was attached to the existing MBE-STM system for in-situ contact deposition and transport measurements. Fig.6.4 shows the details of this chamber.

99.999 % purity silver was used for metal contact deposition. Silver was particularly attractive because it produces continuous flat films on Si(100) [107]. Atomically smooth Ag films are formed, even at low coverages, if the substrate is kept at low temperatures during growth and annealed to room temperature afterwards. Once the stencil mask is placed on the sample, both sample and mask were cooled with liquid nitrogen. After the sample stage temperature reached its minimum value

of ∼90K we waited 60 more minutes to ensure the thermal equilibrium between the sample and stencil mask. This step is required to prevent thermal drift of the mask during metal deposition. In order to release possible mechanical stress accumulated during the cooling process, the stencil masks were removed from the sample for a few seconds and placed back on top of the samples.

Fig.6.5 shows an SEM image of grounded silver contacts fabricated with this technique. Both the SEM and the STM images show a very sharp transition between the silicon surface and the silver film grown through the stencil mask. Height profiles measured by the STM indicate that the transition region is less than 50 nm wide, which has also been confirmed by the sharp increase in the resistivity measured as a function of distance from the planar metal-semiconductor border.

Even though the method described above produces sharp metallic contacts on one end of the nanowire, it requires many consecutive steps. In order to reduce the number of steps performed in UHV, we also used samples with prefabricated metal contacts as a second approach. In this case, samples with prefabricated, 25 nm thick, W or Nb contacts were used. The samples were cleaned in UHV with the following high temperature cleaning procedure [108]: After thorough degassing at 600°C, the samples were heated to 750°C where a silicide begin to form between the metal and the substrate. To prevent silicon carbide formation we avoided higher temperatures before the samples were flashed annealed.

After 10 hours annealing at 750°C samples were flash annealed to 1200°C for 3 seconds. The flash heating process was repeated several times to remove the SiO_2 layer and other contaminants from the surface. STM investigation of the sample revealed a clean Si(100) 2x1 surface with no visible trace of W or Nb contamination. Once the surface is clean, the YSi_2 nanowires were grown. One should note that the prefabricated contacts do not make direct electrical contact to the nanowires. Because silicide formation under the Nb and W contacts consumes a lot of Si from the surrounds, the step density near the contacts is very high and, consequently, the nanowires cannot grow all the way up to the metal contact. Therefore, a UHV

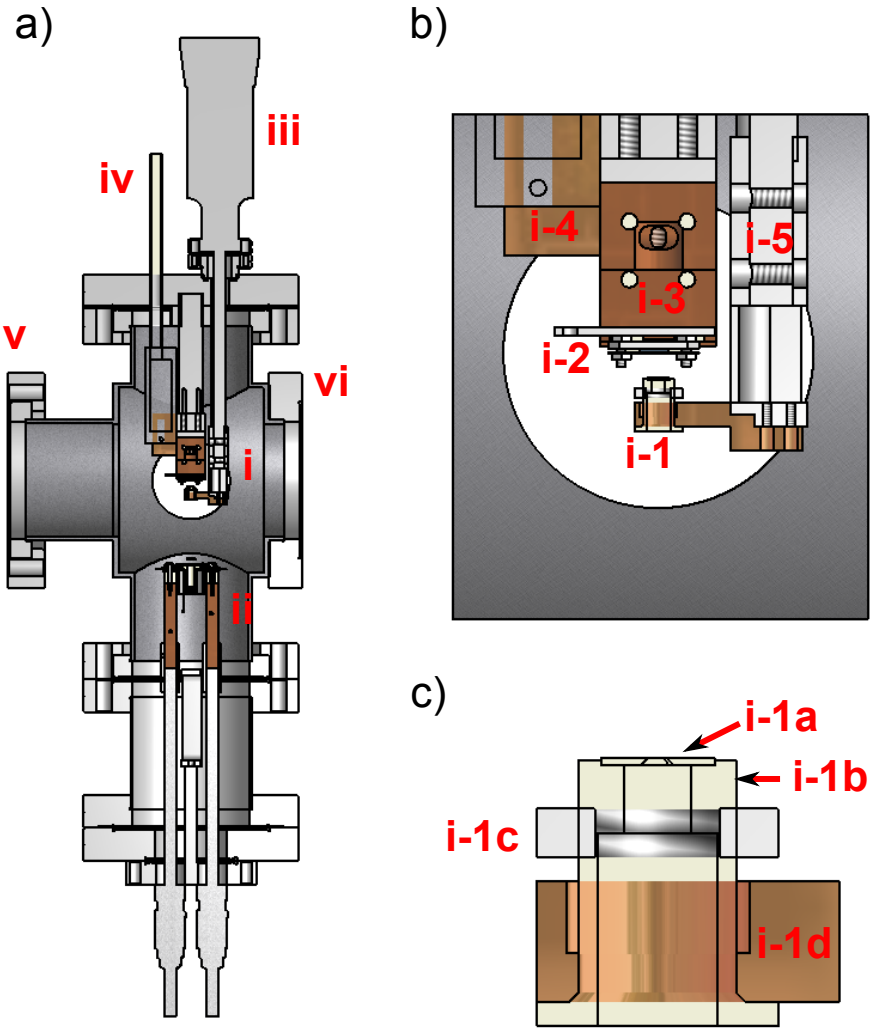


Figure 6.4: Drawing of a the new stencil mask chamber build for precise placements of stencils and contact deposition. Overview of the chamber (a). i: Contact deposition stage, ii: metal deposition source, iii: linear motion feedthrough for mask holder, iv: liquid N_2 input, v: connection to main chamber, vi: viewport. Details of contact deposition stage (b). i-1: stencil mask stage, i-2: sample, 1-3: sample stage, i-4: liquid N_2 reservoir, i-5: linear motion rod for stencil mask stage . Details of stencil mask stage (c). i-1a: stencil mask, i-1b: stencil mask holder, i-1c: springs, 1-1d:stencil mask stage.

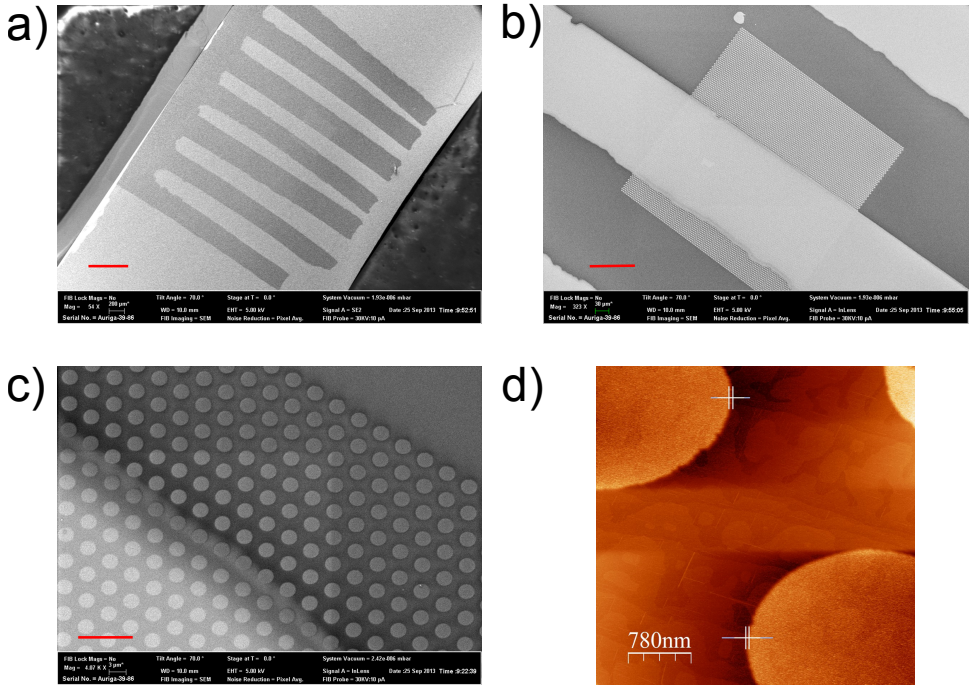


Figure 6.5: SEM images of samples fabricated with the first approach. (a) This image shows large grounded Ag contacts. The red scale bar is 500 μm; (b,c) Contacts deposited through the stencil mask at different magnifications. The scale bars in (b) and (c) are 100 μm and 10 μm, respectively; (d) STM image of the same sample showing sharp lateral borders between the Ag contacts and the nanowires

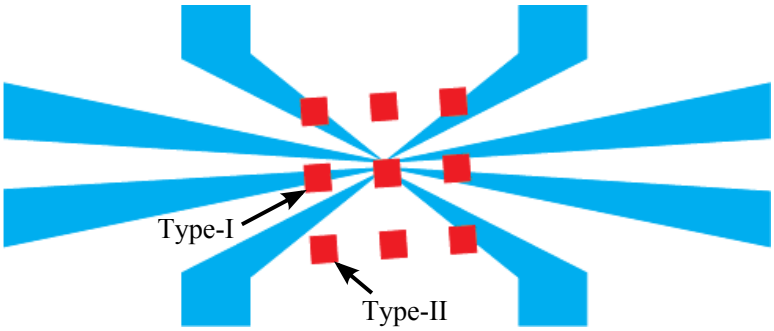


Figure 6.6: Contact geometry for the samples with prefabricated contacts. Prefabricated contacts (blue) provide a low resistivity connection to the system ground while the in-situ metal contacts (red) create a connection between the nanowires and the prefabricated contacts. Type-I contacts have a direct metal to metal contact between red and blue while type-II contacts do not. Nanowires around both type-I and type-II contacts can be studied after careful examination of the contact behavior (see text)

contact deposition step is still needed after completing the nanowire growth. In this approach, a stencil mask with larger holes (100 μm x100 μm) was used to reach the nanowires far away from the prefabricated contacts. Fig.6.6 illustrates the final contact geometry of those samples.

STM images of the border region between the silver film and silicon surface (Fig. 6.7) shows the sharp edge of the silver film. In this case, silver was deposited on a cold substrate (<150K) so as to form a flat film above the critical thickness [107]. As one moves closer to the lateral Ag/Si border on the right, the flat Ag film becomes grannular, which is possibly the result of a strain relaxation in the film. Finally, a sharp lateral border between the silver film and Si surface is observed. The border region is less than 50 nm wide and is composed of small silver clusters forming a continuous film along the border. The electrical connectivity of the silver film, together with the sharpness of the film edge, was confirmed by measururing a constant electrical resistance along the film and a four orders of magnitude increased resistance to ground when measured 50 nm away from the physical border. Details of these measurements will be presented in section 6.6.

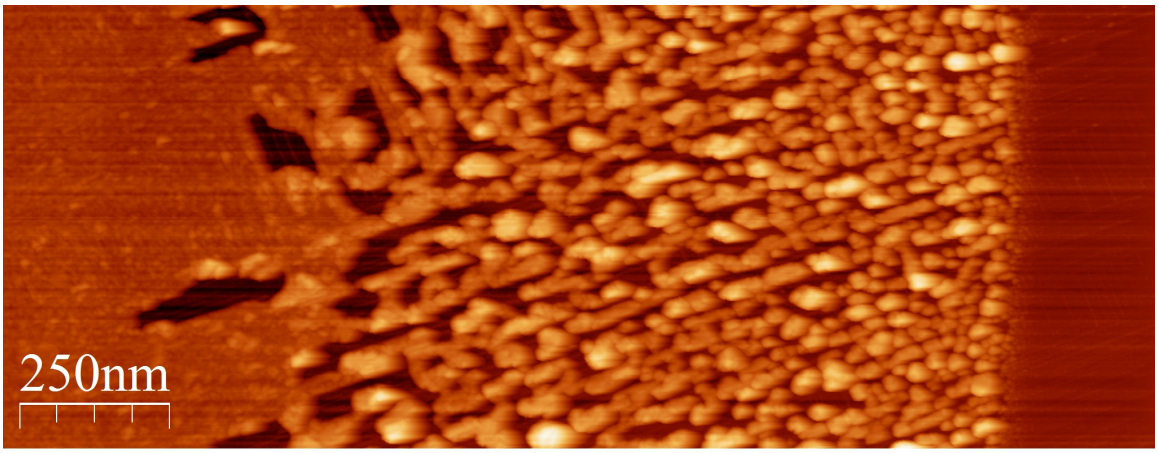


Figure 6.7: STM image of the lateral boundary between in-situ deposited silver contacts and the substrate surface. The lateral border between the Ag contact and Si sunbstrate is located on the right. When going from left to right, the flat silver film evolves into a grannular film and ultimately a very fine grain silver film right before making a sharp transition to the silicon substrate covered with YSi_2 nanowires. Electrical connectivity between the Ag grains will be demonstrated in section 6.6. Small silver clusters deposited by the STM tip during I-V measurements can be seen in upper right corner.

6.2 Metal Contact Behavior

Understanding the behavior of electrical contacts is essential for all transport measurements. As the size of the system under investigation decreases, the electrical contacts to this system become increasingly important and can easily dominate the overall transport behavior. The electrical contacts employed in this study can be divided into two classes, designated as type-I and type-II contacts. A type-I contact is simply a cascade of metal films connecting the YSi_2 nanowire to ground. This type of contact is found on samples produced by the two step metal deposition process (Fig. 6.5) and on samples with prefabricated W or Nb contacts (Fig. 6.6). The overall circuit diagram of an I-V measurement performed on a nanowire with type-I contact is shown in Fig.6.8(a). Type-II contacts, illustrated in Fig.6.6 and Fig. 6.8(b), will also be employed in our transport measurements, as will be explained below.

The type-II contact represents a metal/semiconductor junction with current rectifying behavior. The latter is due to the formation of a Schottky barrier at the

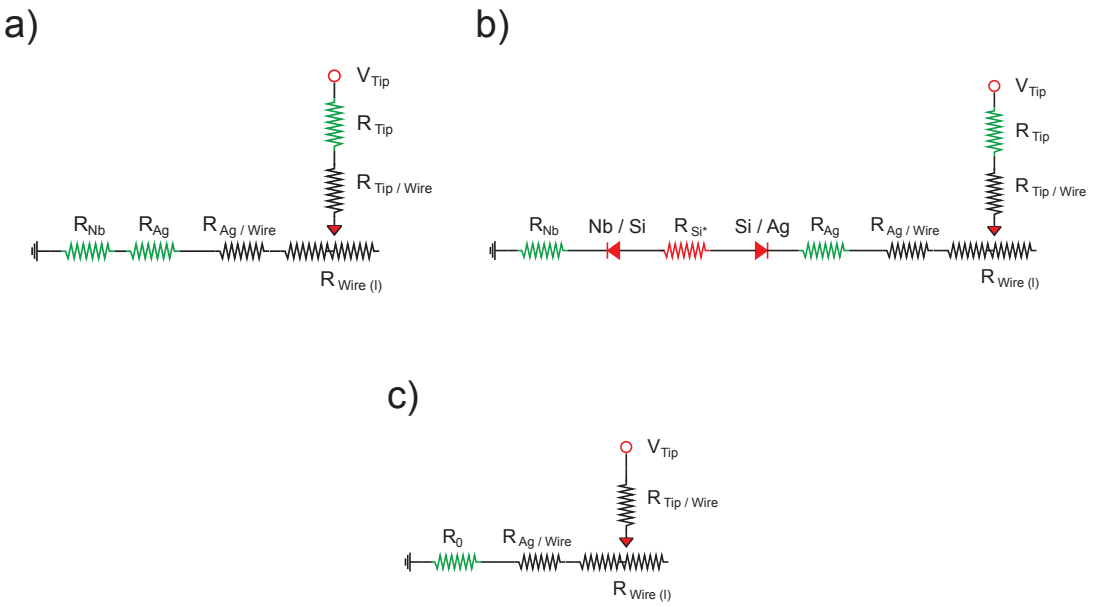


Figure 6.8: Circuit diagrams for the (a) Type-I and (b) Type-II contacts. Both circuits can be simplified to (c) for small bias voltages.

interface[109]. The formation of a Schottky barrier can be explained from the principle that in thermodynamic equilibrium, the Fermi levels on both sides of the contact need to be aligned [110, 109]. Since the metal and semiconductor have different work functions, such an alignment requires charge transfer between the metal and semiconductor, which usually results in the formation of a wide charge-depletion region on the semiconductor side. According to the simple Mott-Schottky model, the Schottky barrier height (ϕ) is given by $\phi = \Phi - \chi$ where Φ is the work function of the metal and χ the electron affinity of the semiconductor. However, this simple relation rarely works for Si where metal induced gap states at the interface make the Schottky barrier almost independent of the metal work function [110].

Without going into further details, the electrical behavior of the metal/semiconductor contacts in this study the can be understood by using the diode equation as a starting point [109]. In a metal semiconductor junction the current versus voltage (I-V) relationship can be given as

$$I = AJ_s e^{(\frac{qV}{nkT})}\,(1 - e^{\frac{qV}{kT}}) \tag{6.1}$$

where A is the area of the contact, q the unit charge, V the voltage across the junction, k the Boltzmann constant, T the absolute temperature, n the ideality factor, and

$$J_s = A^* T^2 e^{\frac{q\phi}{kT}} \tag{6.2}$$

is the saturation current density. A^* is the Richardson constant (260 for n-Si and 80 $A/cm^2/T^2$ for p-Si) and ϕ is the Schottky barrier height [111].

Fig. 6.9 shows the calculated I-V characteristics for a 100 $\times$ 100 μm sized Ag contact on the p-type Si(100) sample employed in this study. In this calculation, ϕ was assumed to be 0.35 eV as given in the literature [112]. Even though the I-V curves show a non linear behavior at higher voltage, the I-V curves are almost linear at small bias ($\pm$1 mV) This is illustrated in Fig. 6.9(b) and can easily be derived from Eq. 6.1 for $V \ll kT/q$. Furthermore, the slope of these lines does not depend on the ideality factor n. Given that the transport measurements on the nanowires are limited to a $\pm$50 nA range, it is very safe to assume a linear I-V behavior for these macroscopic contacts.

The slope of these lines can also be calculated from the diode equation. For $V \ll kT/q$, Eq. 6.1 can be simplified to

$$I = \frac{AJ_s q}{kT}\,V \tag{6.3}$$

Hence,

$$R_{ZB} = kT/AJ_s q \tag{6.4}$$

Where R_{ZB} is called the zero bias resistance. One can see that R_{ZB} increases exponentially with ϕ. Therefore, a small barrier height is crucial for low contact resistance. Fig. 6.10 shows the calculated R_{ZB} for 100 μm x 100μm silver and 1 mm

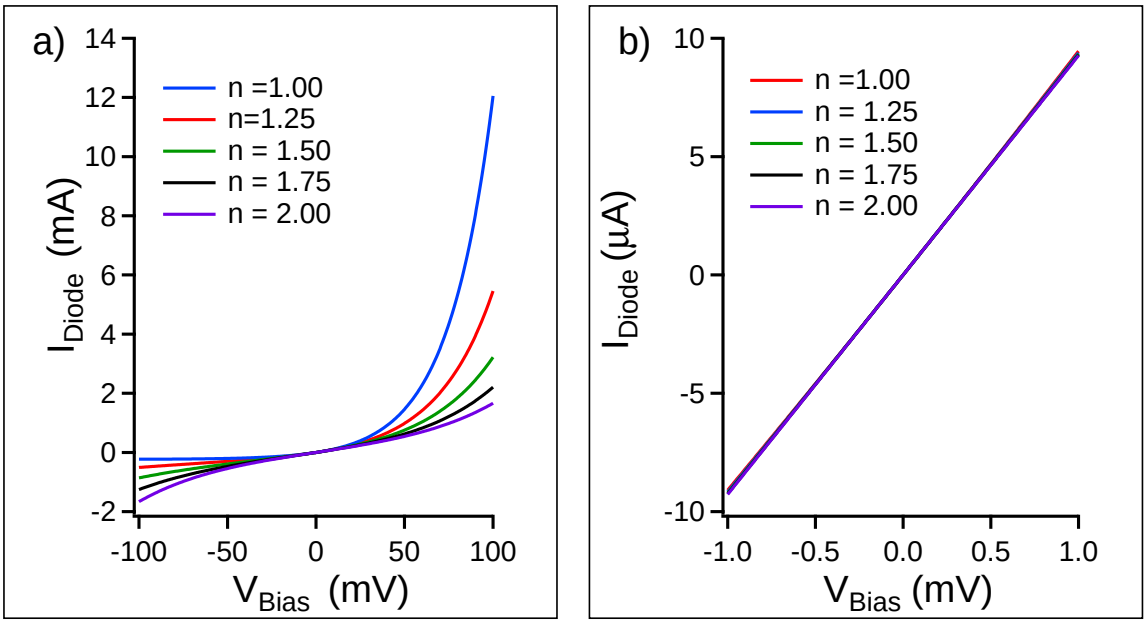


Figure 6.9: (a) I-V curve for Ag-Si junctions used in this study (b) I-V characteristic around zero bias. Note that transport measurement is limited to ± 50 nA which is a small range at the center of these plots

x1 mm niobium contacts as a function of ϕ. Gray rectangles represent the ϕ values measured for macroscopic Ag/p-Si(100) and Nb /p-Si(100) contacts [112, 113].

As shown in Fig. 6.10, the calculated R_{ZB} values for Ag/Si and Nb/Si contacts are in the range of KΩ or less. This is orders of magnitude smaller than the resistances of YSi_2 or $GdSi_2$ nanowire bundles, which were measured to be of the order of MΩ [21, 22]. Furthermore, macroscopic metal-semiconductor contacts exhibit local variations in Schottky barrier height [112], and the barrier height of each patch depends on the local details of the interface. If the overall current density is very low (as in our case), the current flows primarily through the patches with lowest ϕ. Therefore the effective ϕ may be significantly smaller than the one extracted from the extrapolation of the diode equation.

Further reduction of the barrier heights of Ag/p-Si(100) contacts may come from the yttrium interlayer between the silver contact and silicon substrate. Since yttrium has a smaller electronegativity than silicon (1.22 eV vs 1.90 eV), yttrium is expected

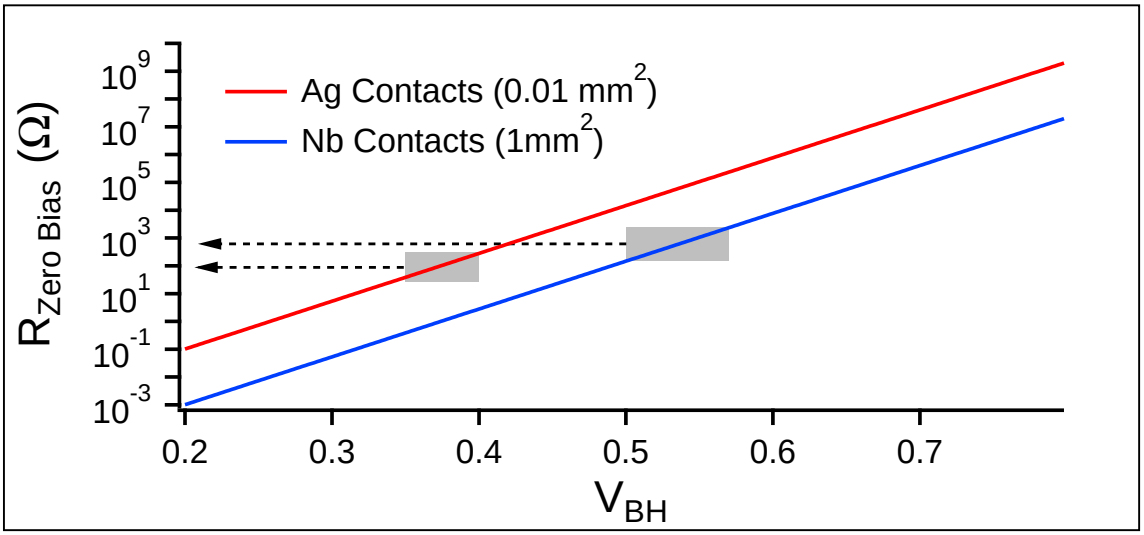


Figure 6.10: Calculated zero bias resistances for the Ag and Nb contacts. The gray areas represent the range of possible ϕ values for each contact

to transfer charge to the silicon [114], producing a positive surface dipole (surface positive, bulk negative). Such a dipole reduces the surface energy by about 0.1 eV [114] and is expected to reduce ϕ on p-type substrates. There are no Schottky barrier measurements available forAg on Si(100)(7x2)-Y but there are some general trends that do relate the shift of the Schottky barrier with the electronegativity of the interlayer atom [115]. For instance, an interlayer formed with group I-III elements decreases the Schottky barrier of Ag on p-type Si(100) while an interlayer consisting of group V-VII elements increases the barrier[115].

Since the sum of the barrier heights of Ag on p-type and n-type Si should be equal to the Si bandgap, a low barrier between silver and yttrium terminated p-type Si(100) indicates a high barrier and a high R_{ZB} between silver and n-type Si. However such a behavior has not been observed. The low barrier between the n-type samples and silver contacts in our experiments may be attributed to the presences of 3D YSi_2 crystallites on the surface, which has been observed in the SEM images. Since bulk YSi_2 has a small barrier with n-type Si (0.4 eV [23]), the R_{ZB} will be dominated by these crystallites.

6.3 I-V Measurements on Contacts

As we discussed above, the macroscopic metal-semiconductor contacts employed in this study are expected to provide an Ohmic behavior near zero bias. Fortunately this hypothesis can easily be checked by performing I-V measurements directly on the metal contacts. Transport measurements on the metal contacts were performed by placing the STM tip on top of the silver film at a tunneling distance of ∼0.5 nm and then driving the STM tip into the sample surface by 1.5 nm. Once electrical contact between the STM tip and silver film is established, we perform an I-V measurement by varying the STM tip voltage typically between ± 50 mV. Currents passing through the STM tip were recorded as a function of applied voltage. Before removing the tip, I-V sweeps were repeated several times in both directions to check for a possible hysteresis effect. An example of the software macros used for the I-V measurements can be found in the Appendix. Once conducted, these measurements can be used as simple series resistance correction when measuring the resistance of the nanowires. One should note that this assumption is valid only if the resistance between the fixed contacts and the sample ground is small compared to the nanowire resistance. Our measurements indeed show that these series resistances are several orders of magnitude smaller than the resistance of the nanowires. Fig.6.11 shows the results from such a measurement on both type of contacts. These measurements are extremely repeatable and do not show any hysteresis. During the transport measurements only silver STM tips were used. In contrast to tungsten tips which are commonly used in STM, silver tips can keep their ability to provide atomic resolution imaging even after touching the surface thousands of times.

R_{ZB} between the silver contacts and ground can be easily calculated from the slope of the I-V curves. Measured values depend on whether the contact is type-I or type-II. Type-I contacts always produce resistance values of the order of 10K-200 KΩ, which is the sum of the tip resistance, the tip-Ag contact resistance, the sheet resistance of Ag, Nb (or W) thin films, and possible voltage or current offsets created

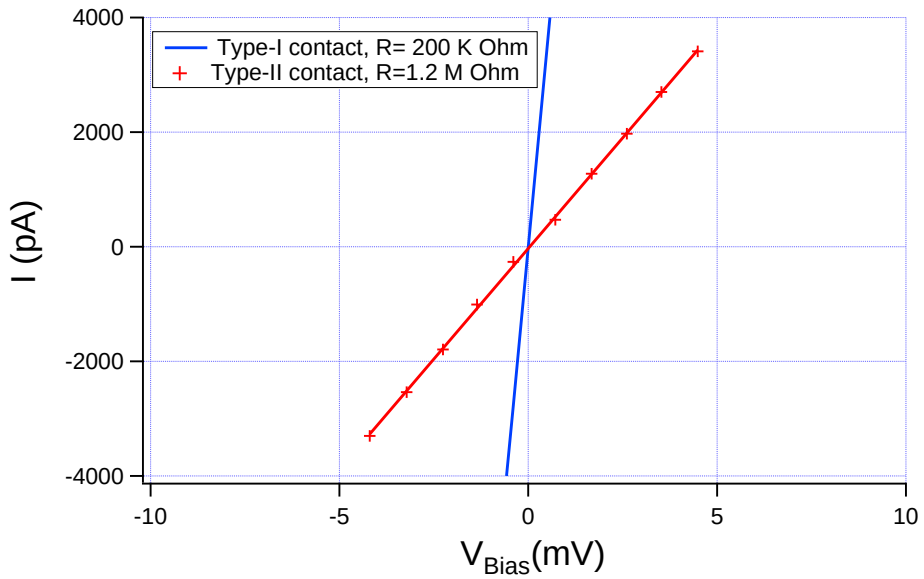


Figure 6.11: Examples of I-V measurements performed on type-I and type-II contacts

by the STM electronics. On the other hand, the resistance of type-II contacts depends on the bulk resistance of the substrate showing that the spreading resistance in silicon also plays an important role.

In light of the above discussion, at zero bias, type-I and type-II contacts can be simplified to a single equivalent resistance as illustrated in Fig.6.8. Even though the approximate resistance of each element can be estimated, they have not been measured individually for each sample. However, the equivalent resistance R_c, which is the resistance between the edge of the silver contacts and ground, has been measured for each individual nanowire and was used as a series resistance correction.

6.4 Leakage Current Through the Wetting Layer

As discussed in Chapter 4, the ultrathin YSi_2 nanowires always co-exist with a (2x7) wetting layer. Such a wetting layer may provide a significant leakage because of its 2D nature. In addition, a leakage current through the bulk is also possible. Therefore,

possible leakage currents through the bulk and the wetting layer must be understood in order to extract the transport properties of the nanowires.

The leakage through the wetting layer can occur in two ways as illustrated in Fig 6.12. In the first scenario, electrons are first injected from the STM tip into the nanowire and then hop onto the wetting layer. Due to the long length of the nanowire, the contact area between the nanowire and wetting layer is much larger than the cross section of the nanowire. Hence, the leakage current may be significant unless the wetting layer has a resistivity that is orders of magnitude larger than that of the nanowire. This scenario, however, neglects the possibility of an energy barrier between the wire and the wetting layer. In the second case, electrons are injected directly from the STM tip (or the fixed contact) into the wetting layer. Since the surface area of the electrical contacts on the nanowires (both the deposited fixed contacts and STM tip) are larger than the width of the nanowire, such a metal to wetting layer contact is inevitable.

In order to better understand the conductance through the wetting layer, we studied current injection from the STM tip to the silicon bulk by measuring the zero bias resistance. Previous STS measurements on the wetting layer had shown that the wetting layer has a non-metallic density of states at room temperature [4]. Therefore, in the simplest model, the contact between the STM tip and the bulk can viewed as a metal (Ag)-semiconductor (Si) contact with an extremely thin yttrium layer in between.

The zero bias resistance of this contact can be calculated with Eq.6.4. Assuming a tip contact area of 10 nm^2 this resistance should be of the order of 10^{12} Ω. However, this simple assumption is far from accurate. First, for such a small contact the electric field between the metal and semiconductor will have a radial shape rather than the planar electric fields in macroscopic contacts. Hence, the depletion layer in the semiconductor will also be non-planar and narrower than its macroscopic counterpart. This phenomenon is known as the edge effect since it is also observed at the sharp edges of macroscopic metal semiconductor contacts [109]. Second, the semiconductor

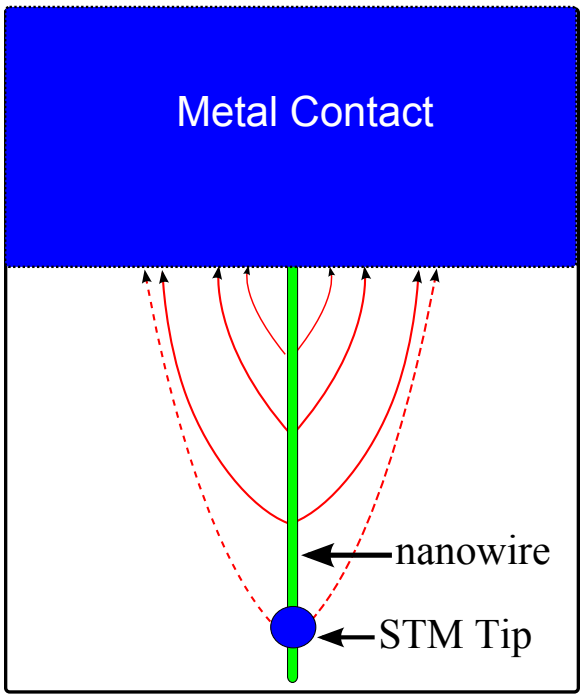


Figure 6.12: Illustration of possible leakage currents. Charge carriers can leak from the nanowire to the wetting layer due to the high aspect ratio of the nanowires (solid curves). A direct injection from the STM tip into the wetting layer is also possible (dashed curves)

surface may have surface states with a low albeit finite conductivity. The sheet resistance of such a surface state was measured to be 4x10^5 Ω for the Si(100) surface [116]. Charge carriers injected from the STM tip can spread across the surface before flowing in to the bulk, thus creating an effective contact area that is much larger than an STM point contact.

A more accurate contact resistance between the STM tip and silicon bulk is then composed of two parallel resistances. A zero bias resistance with a larger effective contact area(A_{Eff}) and a parallel resistance R_E representing the edge effects. Once the charge carriers are injected into to the bulk, the biggest component of the resistance in the bulk is the spreading resistance which can be written as

$$R_S = \frac{\rho}{A} \tag{6.5}$$

Where ρ is the bulk resistivity and A is the contact area. Therefore the modified zero bias resistance R^*_{ZB} between the STM tip and Si bulk is

$$R^*_{ZB} = \left(\frac{A_{Eff} J_s q}{kT} + \frac{1}{R_E}\right)^{-1} + \frac{\rho}{A_{Eff}} \tag{6.6}$$

Edge effects will create a finite resistance even for a truly zero dimensional contact. For a very thin contact with large surface area, R_E is inversely proportional to circumference of the contact area. Hence, $R_E \propto 1/\sqrt{A_{Eff}}$

Therefore, the resistance between an extremely small contact such as our STM tip and the bulk silicon is controlled by the effective contact area, which is determined by the spreading of charge carriers on the surface.

To determine the current spreading, therefore the possibility of leakage current through the YSi_2 wetting layer, we made a comparison with the Si(100) surface whose surface conductance is known [116]. Highly doped p-type substrates ($\rho = 0.02\Omega cm$) were used to minimize the bulk resistance. I-V measurements on a clean yttrium induced Si(100) (7x2) wetting layer returned a zero bias resistance of $\sim 10M\Omega$. This value was very close to the zero bias resistance ($\sim 6M\Omega$) measured on the clean

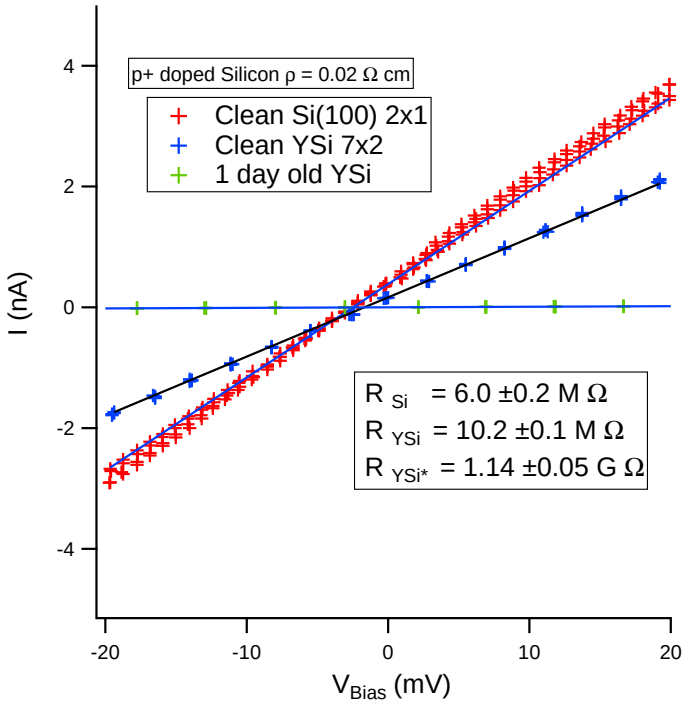


Figure 6.13: I-V curves measured on a clean Si(100)(2x1) surface, on a freshly prepared Si(100)(2x7)-Y surface, and on a one day old Si(100)(2x7)-Y surface

Si(100)(2x1) surface of the same sample before yttrium growth. These results indicate that both surfaces have a comparable sheet resistance. Furthermore, neglecting the edge effects, the effective surface area is found to be $\sim 10^5$ nm^2 giving us a spreading radius of the order of several hundred nanometers. Determination of the real spreading radius requires a very careful modeling of the electron transport. However, these measurements clearly tell us that leakage current through the clean wetting layer is not negligible.

Once we repeated the measurements on the same sample but one day after the yttrium deposition was made, we noticed that the zero bias resistance of the sample had increased by more than two orders of magnitude, as shown in Figure 6.13. The huge increase in the zero bias resistance can be attributed to the passivation of the surface states by the adsorption of residual gas molecules in the UHV chamber. Even though the chamber pressure was below 3×10^{-11} Torr during and in between these

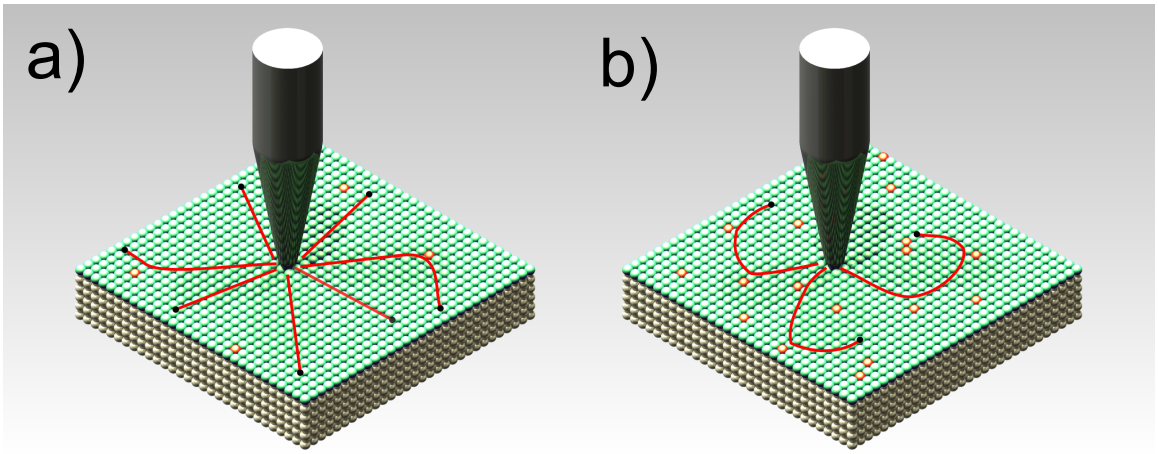


Figure 6.14: Illustration of the influence of surface contamination on the effective contact area. a) On a clean surface charge carriers injected from STM tip can spread large distances creating a large effective contact area. b) However, on a contaminated surface they are scattered by the defects and can not spread on the surface

measurements, such behavior is not unexpected for reactive surfaces. Adsorbed atoms or molecules such as hydrogen or carbon monoxide create defects and passivate the surface states. These defects scatter the electrons injected from the STM tip as illustrated in Fig.6.14. Scattering by the defects hinders the spreading of the charge carriers and thereby reduces the effective surface area and increases the resistance of the contact.

The time evolution of the conductance through the wetting layer explains the insulating behavior of the wetting layer observed with ex-situ transport measurements. However, this also raises doubts about the robustness of the surface states on the nanowires. STM and SEM studies of samples that were intentionally exposed to air showed that the nanowires are structurally stable in air. However, STS measurements on these samples were not conclusive due to the continuous absorption/desorption of contaminants during STM imaging.

In order to check the discrepancy between the previous STS and transport measurements on Si(100)(2x7)-Y, which showed a non-metallic behavior [21], and the high surface conductivity observed for a freshly prepared wetting layer, we repeated our STS measurements on a freshly prepared wetting layer. Indeed, the wetting

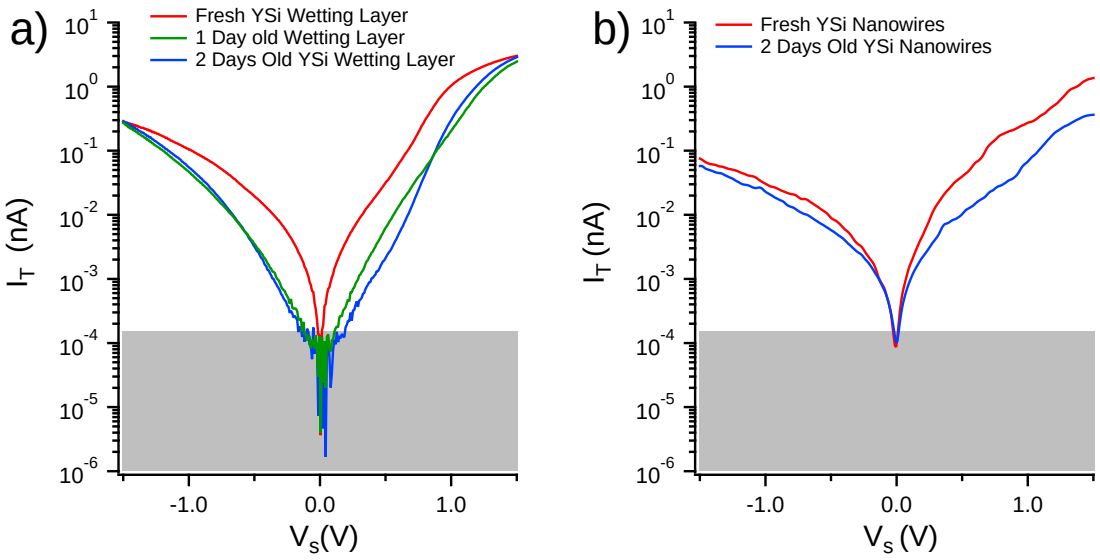


Figure 6.15: STS spectra obtained from (a) the wetting layer and (b) the nanowires recorded right after growth and on the following days. The gray areas represent the noise level for these measurements. Tunneling parameters; V_s=1.5V, I_t=0.3 nA

layer exhibits a metallic density of states. However, this metallic behavior disappears quickly and a band gap appears in the STS spectra, as shown in Fig 6.15(a). On the other hand, STS measurements on the nanowires do not reveal such a time dependence. This is shown in Fig 6.15(b). Furthermore, the peak positions in the normalized dI/dV curves do not change with time (see Fig.6.16) showing that the electronic states of the nanowires are much more resistant to surface contamination compared to the wetting layer.

The above observations are of great importance in fundamental studies and practical applications of nanowires. They indicate the possibility of eliminating the leakage current via controlled adsorption of hydrogen or other gases while preserving the electronic states of nanowires. However, they also caution that great care should be taken when measuring electronic transport through the nanowires. If the wetting layer is not completely passivated, a significant amount of current will leak through it, making it increasingly difficult to extract the transport behavior of the nanowires. During the experiments, control measurements on the wetting layer should be done

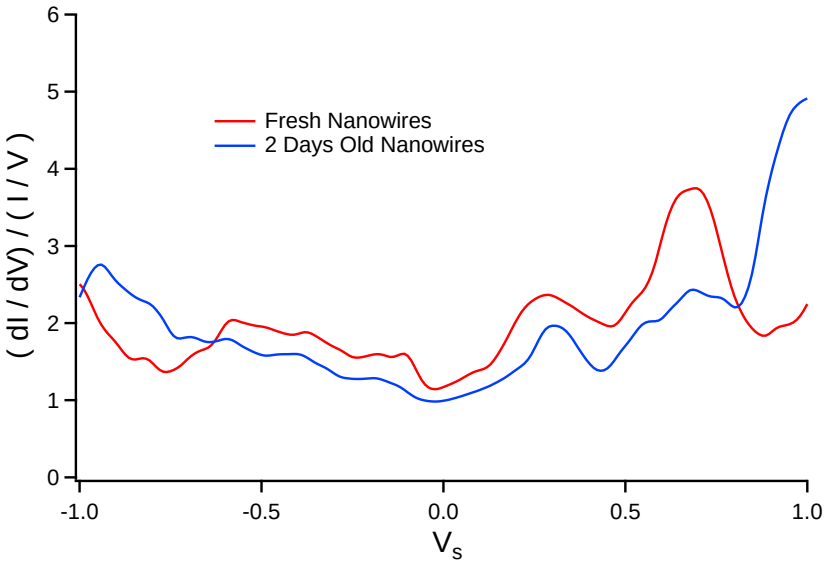


Figure 6.16: Normalized dI/dV spectra of freshly prepared (red) and two-days old (blue) nanowires. Notice that the peak positions do not change. Tunneling parameters; V_s=1.5V, I_t=0.3 nA

in parallel with the transport measurements on the nanowires with minimal delay. In our studies, the time spent for metal contact deposition following nanowire growth prevented us from conducting lateral transport measurement of a freshly prepared wetting layer using our two-probe method. However, this time also ensured the passivation of the wetting layer as required for transport measurements on the nanowires.

6.5 IV Measurements on Nanowires

Our primarly objective is to measure electronic transport in the ultrathin YSi_2 nanowires and to find possible correlations between the location and density of defects on the nanowire and its resistance. To achieve this goal we need to separate the current flowing through the wire from the leakage current, and understand the influence of the electrical contacts on the measured resistance. In this section we will describe our findings from I-V measurements performed on both grounded and

floating nanowires, and on the wetting layer. A grounded nanowire is in direct physical contact with the deposited silver film. On the other hand, nanowires that are in close proximity of a metal contact but do not make a physical connection are called floating nanowires. The transport measurements described below were performed exclusively on Si(100) substrates with bulk resistivities greater than 50 Ω cm and up to 20,000 Ω cm.

Once the sample and metal contacts were prepared, we looked for the edges of the metal contacts to find grounded nanowires that are partially buried under the metal contact. One of them was selected and examined for possible defects before starting the transport measurements. Similar to the I-V measurements on the silver contacts, transport measurements on the nanowires were performed by placing the STM tip right above the nanowire at a tunneling distance of typically 0.5 nm. Next, we moved the STM tip toward the sample surface for 1.5 nm. Once electrical contact between the STM tip and nanowire was established we performed an I-V measurement by varying the STM tip voltage typically between ± 50 mV. The current passing through the STM tip was recorded as a function of applied voltage. Before removing the tip, I-V sweeps were repeated several times in both directions to check for a hysteresis effect. Similar measurements were performed on the metal contacts, the wetting layer and the floating wires.

As we described in section 6.3, I-V measurements on the metal contacts gave us a variety of contact resistances which can be used as series resistance corrections. On the other hand, I-V measurements performed on the wetting layer always returned extremely high resistances, independent of the distance from the contact and contact resistance. In fact, the currents measured during the I-V measurements on the wetting layer were below the accepted noise levels of the tunneling measurements. Therefore, the reported values should be considered as a lower limit of the wetting layer resistance.

Fig. 6.17 presents the I-V characteristics of the wetting layer averaged over several measurements in the same area. Individual measurements given in the inset cannot

be distinguished from one another. The slope of the averaged curve gives a resistance value of $\sim$ 100 GΩ for the wetting layer. One should note that the time required for depositing the metal contacts prohibits the study of a freshly-prepared wetting layer, which has a much higher conductance as discussed in section 6.4. The I-V measurements on the wetting layer and nanowires were consecutively performed at the same time. Therefore, they can be considered as a safe baseline for estimating the leakage current.

One can claim that charge carrier injection from the tip to the wetting layer is prohibited because of a high Schottky barrier, while current leakage from the wire to the wetting layer is still possible. To test this possibility we also performed I-V measurements on the floating nanowires. These measurements also returned very high resistance values, similar to those of the wetting layer, as shown in Fig 6.17. These results unambiguously show that the nanowires are electronically disconnected from their surrounds and the leakage scenario mentioned above does not take place.

Finally, I-V measurements performed on the nanowires are presented in figure 6.18. These measurements show that the short, ultrathin nanowires have linear I-V characteristics but with resistances larger than 100 MΩ. The measured resistances are orders of magnitude larger than the values measured on nanowire bundles or thick nanowires [21, 22]. Transport measurement performed on the far end of the long nanowires produced results that are indistinguishable from the ones obtained from the wetting layer. These very high resistances were persistent, even after extensive efforts to minimize possible contact resistances between wires and ground and also between the STM tip and the wire. The reasons for this high resistance are not known, but a possible explanation will be offered in the next section, based on the observed exponential dependence of the resistance on the wire length

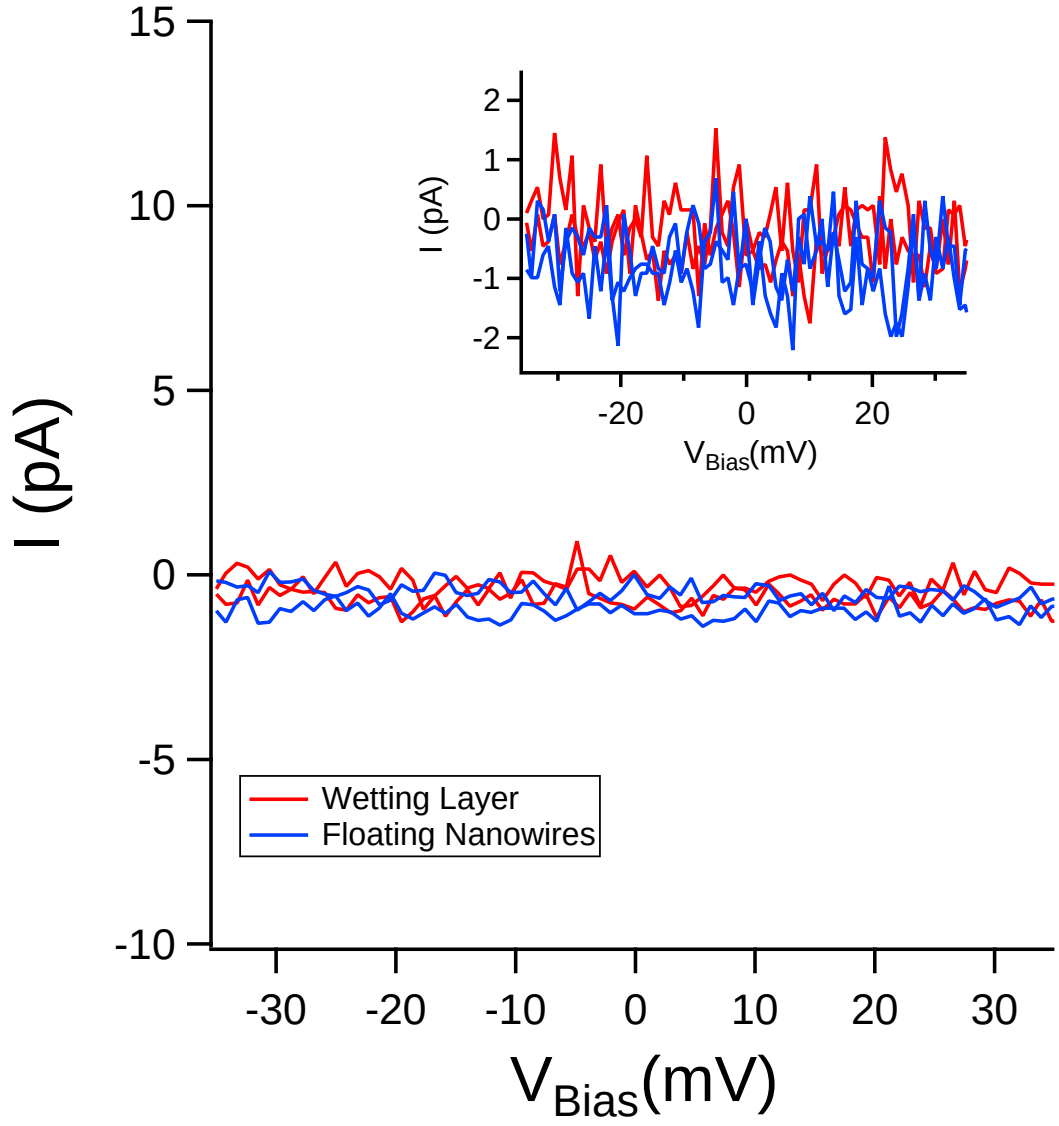


Figure 6.17: I-V characteristics of the wetting layer (red) and floating nanowires (blue), each one averaged over five measurements. I-V curves for individual measurements are provided in the inset

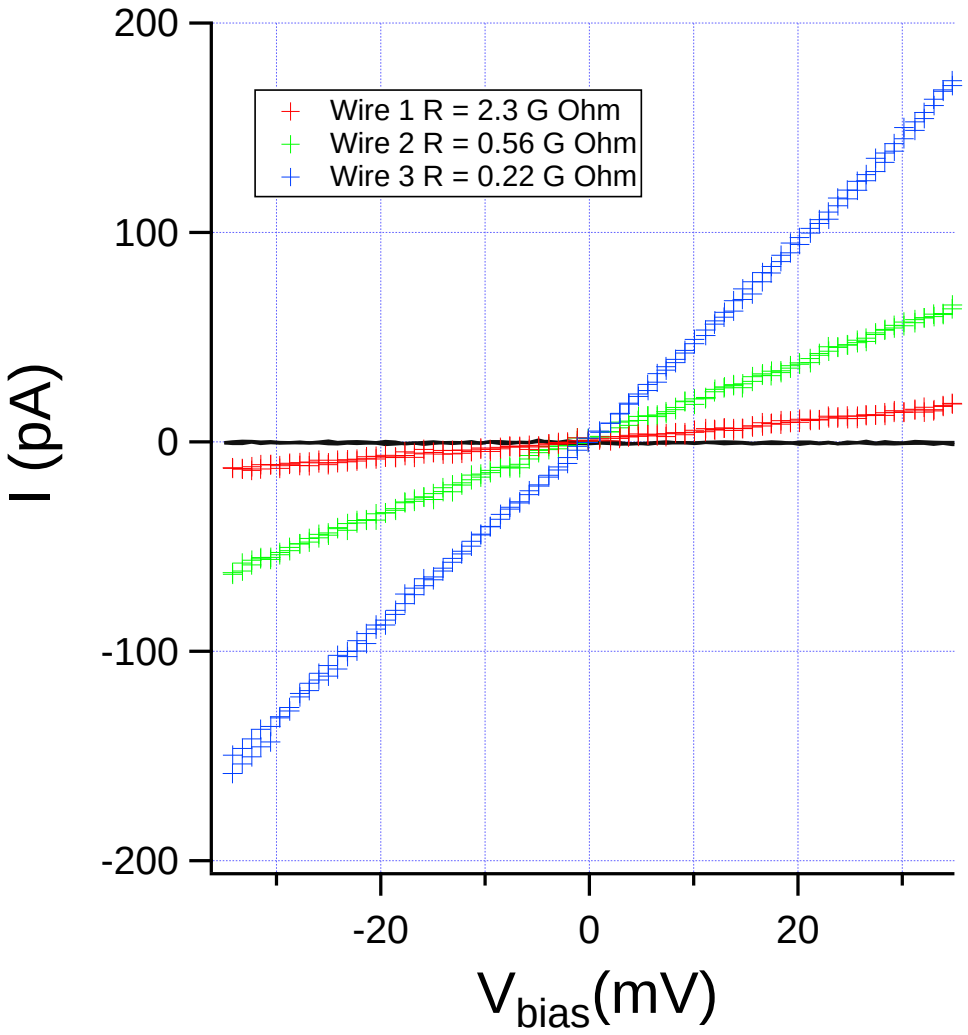


Figure 6.18: Representative I-V curves obtained from different nanowires. Nanowires exhibit linear I-V characteristics without hysteresis. They have high resistances but their I-V curves can easily be distinguished from those of the wetting layer(black solid line)

6.6 Resistance Measurements with Variable Probe Spacing

Our transport measurements on the ultrathin nanowires show that every single one of them is highly resistive at room temperature. To better understand the reason behind this high resistance we performed I-V measurements on the same nanowire as a function of distance l from the metal contacts, together with control measurements on the wetting layer.

In order to have a long well-defined border between the metal contacts and the Si(100) surface, we used stencil masks with square shaped holes and aligned these masks in such a way that nanowires are perpendicular (and parallel) to these square shaped metal contacts. To exclude the influence of tip induced wire damage on the measurement results, we started the I-V measurements from the open end of the nanowire and conducted I-V measurements as we approached the metal contact. Measurements were not taken at equidistant locations. Instead we waited until the STM tip compensates for the small drift after each I-V measurement so that the precise position on the nanowire can be determined again. We continued performing I-V measurements on the approximate position of the nanowire after it disappeared under the metal contacts. Finally the nanowire was quickly scanned again to see if any large cluster was deposited on the wire during the IV measurements.

I-V measurements on the metal contacts show that on the metal side, the contact resistance does not change as a function of distance from the contact edge. The island like structures observed at the edge of the metal contacts are therefore connected and represent a percolated network up to the flat region of the Ag film. This observation is consistent with Jiang *et al.* [107] who prepared Ag films on Si(100) under the same conditions as we did. Furthermore, the border itself is composed of small silver clusters producing a fine grain but continuous film parallel to the border. A large number of I-V measurements were performed at the border region to ensure electrical continuity of the silver film, see Fig. 6.19.

On the other hand, the resistance values measured on the wetting layer were four orders of magnitude larger than the ones measured on the metal contact. Even though the location of measurements on wetting layer was only 30 nm away from the metal contacts. At the border region I-V measurements were not very consistent, probably because the tip displaced the small silver clusters in this region. Beyond this ∼30 nm wide region, the measured current values were indistinguishable from each other and from the ones given in the inset of Fig 6.17. Hence a distance dependent I-V measurement could not be reliably performed on the wetting layer. The resistance values of the wetting layer displayed in Fig.6.19 were calculated from simple linear fits to the individual I-V curves and therefore should be taken as an approximate value. However the slope of the I-V curves averaged over many measurements performed within a distance of 40±10 nm from the border gave a similar resistance of ∼100 GΩ.

As we mentioned before the nanowires are also very resistive but they produce I-V curves that are easily distinguishable form those of the wetting layer, particularly for the short wire segments close to the metal contacts. On the other hand, the I-V curves for long wires were similar to those of the wetting layer. Distance dependent I-V measurements on single nanowires produced results that are consistent with these observations. The resistance $R(l)$ of a single grounded nanowire was consistently larger than 100 GΩ until the tip was positioned within a distance of ∼250 nm from the metal contact. At shorter distances, the resistance values decreased monotonically, except for some occasional outliers that most likely should be attributed to small drifts of the STM tip away from the wire. Finally, a nanowire to metal contact resistance ($R_{cw\Rightarrow m}$) of the order of 10 MΩ was measured for l=0. $R_{cw\Rightarrow m}$ did not depend on the resistance between the metal contacts and the ground (R_c), which is much smaller.

Even though $R(l)$ decreased monotonically with decreasing l, none of our measurements resembled a linear dependence on l. This indicating that transport through the YSi_2 nanowires is not diffusive. Some of the nanowires showed an

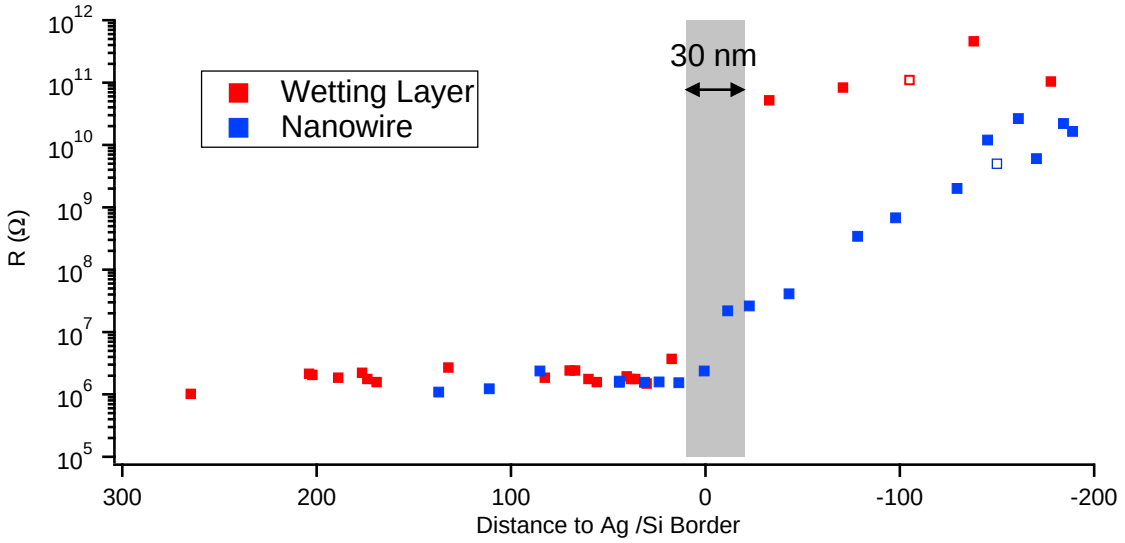


Figure 6.19: Resistance of a $5a_0$ nanowire as a function of distance l from the fixed metal contact. The resistance of the contacts does not change on the metal (left) side of the contacts while a sudden increase is observed on the right side of the contact when the tip is positioned on the wetting layer. The resistance of the YSi_2 nanowire increases monotonically with l showing an exponential dependence. Blue and red empty squares represent measurements performed on connected and disconnected islands respectively (see text)

exponential dependence between $R(l)$ and l (see 6.19) such that

$$R(l) = R_c^* + R_0 e^{(l/\xi)} \tag{6.7}$$

where $R_c^* = R_c + R_{cw \Rightarrow m}$ and ξ is $\sim$ 20 nm.

This behavior is strongly suggestive of Anderson localization, discussed in the previous chapter.

One might blame the contact resistance between the STM tip and the nanowires for the high resistance values. This possibility has been checked with two different methods. First, silver clusters were deposited on the nanowires using the STM tip, as described in Section 3.2.1. Next, we measured the I-V curves by placing the STM tip on top of the deposited silver clusters. In the second method, samples were annealed at 100°C for 10 min. After the annealing process, the initially connected silver islands at the edges of the contacts transformed into larger disconnected islands. Meanwhile, the flat silver film remained in tact. Some of the silver islands were still connected to the flat grounded silver contacts via a nanowire, as shown in Fig. 6.20. I-V measurements were performed by placing the STM tip on top of the connected or disconnected islands. These measurements returned similar resistance values with the ones where the STM tip is placed directly on top of the nanowire (see Fig 6.19). These results strongly suggest that the tip-wire contact cannot be the reason behind the measured high-resistance values.

6.7 Discussion of Results

The goal of the studies presented in this chapter was to design and develop a transport measurement method which can investigate even the shortest segments of atomically thin nanowires, and to use this method to study electron transport through individual YSi_2 nanowires. Our results clearly demonstrate the capabilities of the method we developed, both with regard to the fabrication of in-situ electrical contacts with

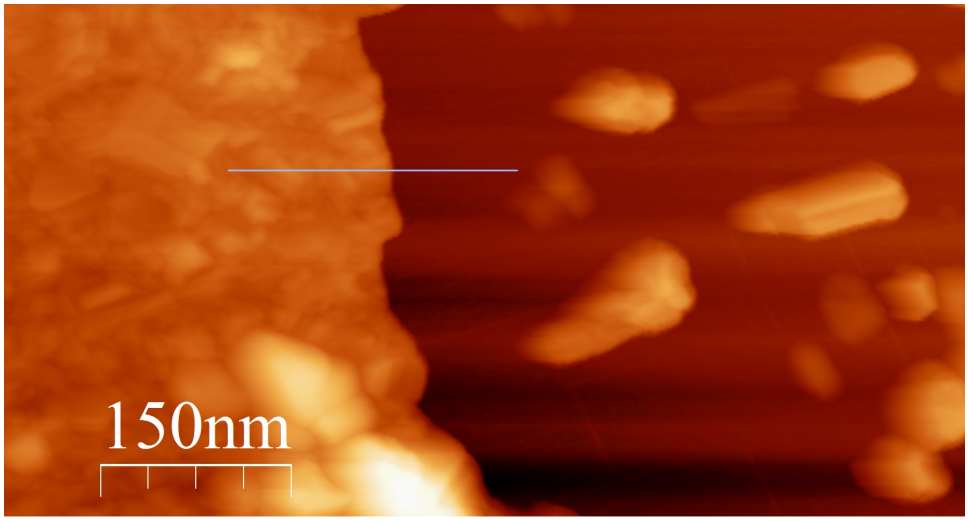


Figure 6.20: . Silver islands are formed after annealing the sample at 100°C. Some of the islands are connected to the metal contacts via a nanowire while the remaining ones are not. Transport measurements were performed on these islands to check if the contact resistance between the STM tip and the nanowire is responsible from the high resistances measured on the wires

very sharp planar boundaries, and to the in-situ transport measurements on nano structures as small as $1 \times 0.5 \times 30$ nm.

The transport studies on YSi_2 nanowires produced several interesting results. First, they show that the wetting layer, which was always considered to be insulating, has a significant conductivity right after deposition. However, it becomes insulating over time, presumably due to the adsorption of residual gas molecules present in the UHV chamber. Interestingly, the nanowires did not show this behavior and produced repeatable resistance values. Secondly, the ultrathin YSi_2 nanowires were shown to be much more resistive than their thicker counterparts. Their resistances differ by several orders of magnitude, indicating that the electronic transport in ultrathin YSi_2 nanowires approaches the 1D limit where electron transport is limited due to repeated back scattering from defects in the system.[117, 118, 95]

We also observe that the resistances of some nanowires vary exponentially with their length. The exponential fit produces a localization length of ∼20 nm. This localization length is fairly close to the average distance between defects on the

nanowire (∼5nm [21]). Hence, our observations are consistent with the prediction that the localization length should be comparable to the mean free path for backscattering in a real 1D system [95, 119]. Furthermore, the calculated value of ξ is in a good agreement with Thoulesss prediction [120] for thin wires, where ξ is calculated to be 19 nm and 32 nm for the $3a_0$ and $5a_0$ nanowires, respectively. This study also mentions the possibility of an exponential length dependence at extremely low temperatures, but predicted that this behavior should disappear at higher temperature due to phonon-assisted carrier hopping. However, due to the extremely small size and, consequently, large energy-level spacings of the wires, the exponential behavior may still hold at room temperature. As we discussed in Chapter 5, Anderson localization has already been observed and well studied in carbon nanotubes, which have similar cross sections. A similar behavior has also been predicted for silicon nanowires [121] but this remains to be confirmed experimentally.

Electron transport in nanowires can be better understood with temperature-dependent transport measurements. However, the resistance of these ultrathin nanowires is already very high at room temperature. I-V measurements at low temperatures, where the resistances will even be higher, will be very challenging because localization effects can only be observed at low bias voltages. High bias voltages can excite more phonon modes and drive the system to diffusive regime [99] as we discussed in Chapter 5. Measurements above room temperature are possible but one should be careful with the silver contacts. Silver films tend to create 3D islands when annealed at high temperatures. Therefore the connectivity of the film may be compromised. Using a different metal for contact deposition may solve this problem. On the other hand, at elevated temperatures, leakage though the bulk should also be considered.

The question remains whether the nanowires are highly resistive to begin with or whether they become resistive over time, as is the case for the (2x7) wetting layer reconstruction. It is well known that the nanowires easily form adatom and vacancy defects. However, some of these defects may not back scatter electrons once they are

passivated by absorbate molecules. This question can only be answered via systematic and controlled exposure to a variety of gas molecules, in conjunction with transport measurements.

This study provides an important insight into electron transport in ultrathin epitaxial YSi_2 nanowires on Si(100) and provides a glimpse of what to expect for real 1D systems. More experimental and theoretical studies are need to fully determine the transport mechanism and the influence of the varies types of defects, the formation of which is a most inevitable consequence of the fragility of the ordered state in one dimension.

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Appendix

Appendix A

RHEED Patterns During Yttrium Growth on Si(100) Surface

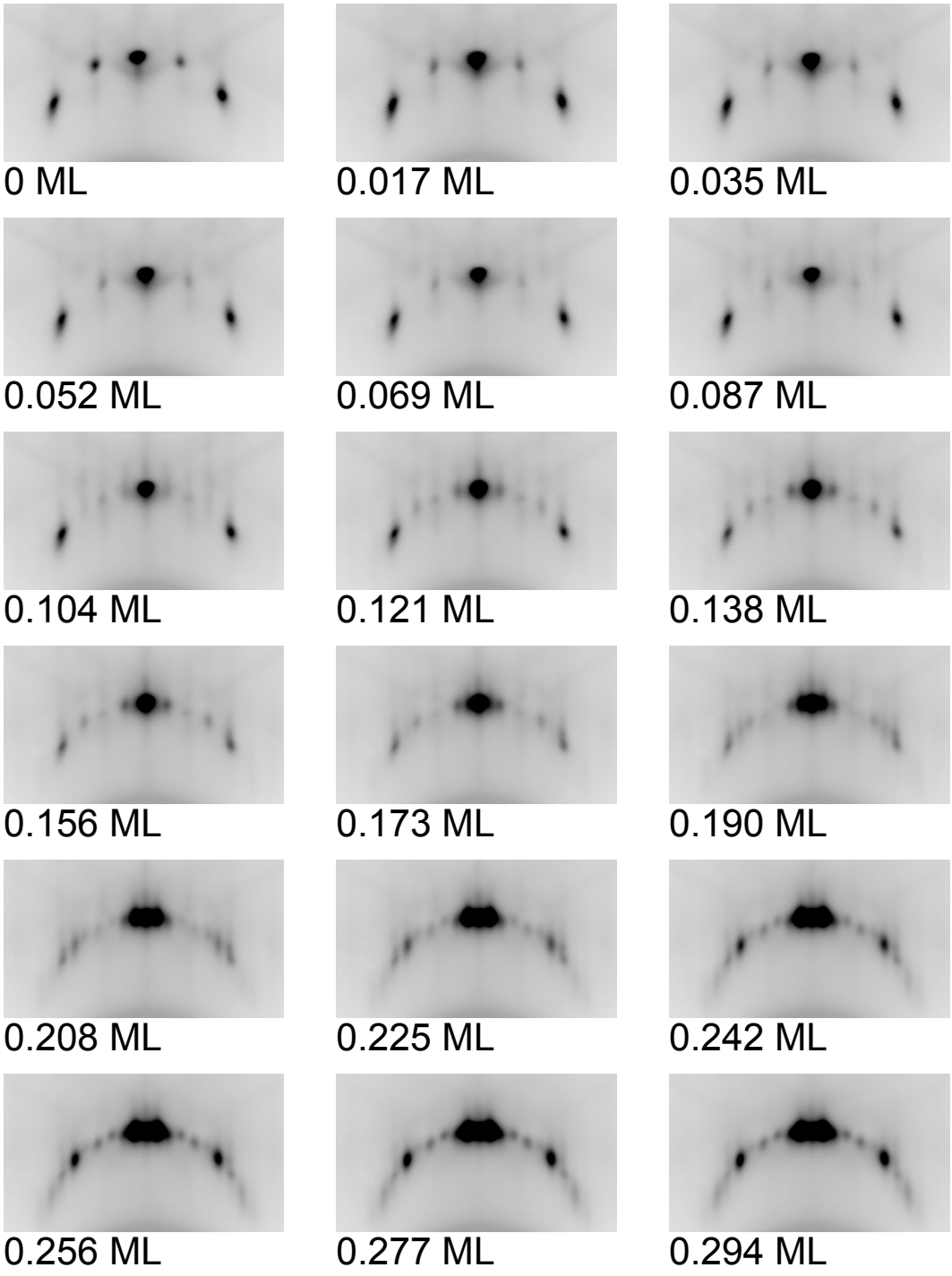


Figure A.1: RHEED patterns recorded at different yttrium coverages (θ) during nanowire growth on Si(100) surface. ($\Delta\theta = \pm 0.005$ML)

.

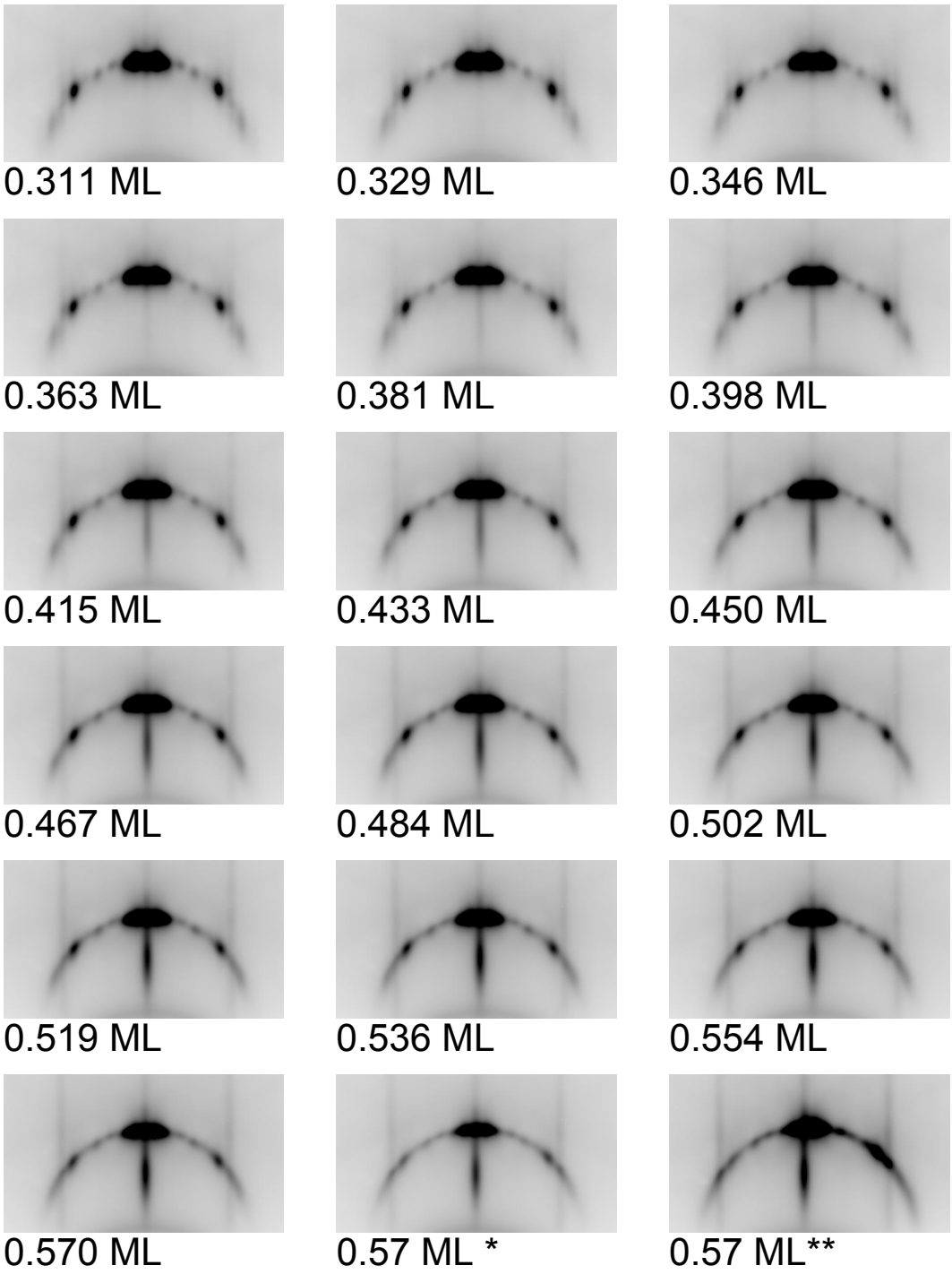


Figure A.2: RHEED patterns recorded at different yttrium coverages (θ) during nanowire growth on Si(100) surface. * After 15 seconds of post annealing, ** After quenching the sample. ($\Delta\theta = \pm 0.005$ML)

Appendix B

Macro Sample for IV Measurements

```
; When used with 'Parameter: Macro',
; the macro code below performs a transport IV measurement after
; lowering the tip to the sample.
;
; Spectroscopy Preset:
;
;   Parameter:     V
;   From:          -50 mV
;   To:            50 mV
;   Delay:         200  microseconds
;   Acquisition:   1280  microseconds
;   Feedback:      off
;   No.Data Points: 950
;
; Extra Settings:
;
```

```
;   T1:  200  microsec
;   T2:   2500  microsec
;   T3:  100  microsec
;   T4:   50  microsec

acq_time,  1280 ;define acquisition time for subsequent 'measure'
                ;commands (must be 2^n times 10 microsec)
delay,     200  ;delay before loop off (corresponds to T1)
feedback,    0  ;feedback loop off
set_v,    1.00  ;start from 1.00 V bias voltage
delay,    2500  ;delay after loop off (corresponds to T2)

loop_times, 195  ;repeat next commands 195 times | In order to prevent
  delay,     80  ;delay within voltage ramp      | charging of the
  measure        ;read the current value         | surface, the tip
  add_v,  -0.005 ;decrease voltage               | bias is slowly
loop_end                                         | reduced before
delay,     80   ;last delay within ramp          | lowering the tip
measure         ;read the last value             |

set_z,    -1.6  ;1.6 Nanometer into sample       |Tip is lowered
delay,    2000  ;2ms delay                       |

set_v,    0.050 ;start from  50 mV
delay,     2500 ;delay after loop off (corresponds to T2)

loop_times, 100  ;repeat next commands 100 times | +50 mV to -50 mV
  delay,     80  ;delay within voltage ramp      |
  measure        ;read the current value
```

```
  add_v, -0.001  ;decrease voltage
loop_end
delay,     80   ;last delay within ramp
measure         ;read the last value

loop_times, 100  ;repeat next commands 100 times | -50 mV to +50 mV
  delay,     80  ;delay within voltage ramp
  measure         ;read the current value
  add_v,  0.001  ;increase voltage
loop_end
delay,     80   ;last delay within ramp
measure         ;read the last value

loop_times, 100  ;repeat next commands 100 times | +50 mV to -50 mV
  delay,     80  ;delay within voltage ramp
  measure         ;read the current value
  add_v, -0.001  ;decrease voltage
loop_end
delay,     80   ;last delay within ramp
measure         ;read the last value

loop_times, 100  ;repeat next commands 100 times | -50 mV to +50 mV
  delay,     80  ;delay within voltage ramp
  measure         ;read the current value
  add_v,  0.001  ;increase voltage
loop_end
delay,     80   ;last delay within ramp
measure         ;read the last value
```

```
reset_z          ;Back to original Z
reset_v          ;reset gap volts to scan value
delay,     100   ;delay before loop on (corresponds to T3)
reset_feedback   ;reset feedback to previous state
delay,      50   ;delay after loop on (corresponds to T4)
```

Vita

Saban Mustafa Hus was born in Aegean region of Turkey. After graduating from Izmir Fen Lisesi, a high school specialized in science, he attended the Middle East Technical University (METU) in Ankara, Turkey. He received his bachelors degree in Electrical and Electronic Engineering in 2003, and in Physics in 2004. He earned a masters degree in experimental Condensed Matter Physics in 2006 from METU. In 2007 he started the graduate school of the University of Tennessee, Knoxville.