Design and Analysis of a Fully-Integrated Resonant Gate Driver

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Yu Long
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Abstract

Several decades ago the resonant gate driving technique was proposed. Given the recent rapid growth in GaN HEMT power device applications for high-frequency power applications, research has been conducted in the power electronics field using resonant gate driving for GaN power devices. Previous research for resonant gate drivers for GaN HEMT devices mostly focused on implementing the gate driving function itself, and mostly for normally-on HEMT devices.

The normally-off (enhancement mode) GaN power device was introduced to the commercial market in 2009. A new resonate gate driver is proposed in this work to implement resonant gate driving for commercial high-speed normally-off GaN power devices. The desired resonant condition is configured by different turn-on and turn-off driving pulses with specific driving time and pulse width. Using synchronous timing control within the driver integrated circuit, the power device gate voltage is securely clamped within the expected gate voltage at switching frequencies beyond 10 MHz. In this research, a customized resonant gate driver IC was designed and developed on a commercially-available silicon CMOS process. Compared with current commercial gate driver ICs, our test results demonstrate the effectiveness, advantages and limitations of the proposed gate driver IC for the enhancement-mode GaN power device using alternative resonant gate driving techniques for the first time.

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List of Abbreviations

MOS	metal oxide semiconductor
FET	field effect transistor
MOSFET	metal oxide semiconductor field effect transistor
BJT	bipolar junction transistor
HEMT	High-electron-mobility transistor
2DEG	two dimensional electron gas
GaN	Gallium Nitride
SEM	scanning electron microscope
FET	field effect transistor
SOI	Silicon on isolator
ZVS	zero voltage switching
ZCS	zero current switching
VDMOS	vertical diffused metal oxide semiconductor
LDEMOSFET	lateral-drain-extension MOSFET
LDMOS	laterally diffused metal oxide semiconductor
RGD	resonant gate driver
UVLO	under-voltage lock-out
BMR	beta multiplier reference
PCB	printed circuit board
ESR	equivalent series resistance
ESL	equivalent series inductance
DRC	design rule check
LVS	layout versus schematic
PEX	Calibre layout parasitic extraction
QRC	Assura layout parasitic extraction
DPT	double pulse testing
SMD	surface mount device

Chapter 1

Introduction

1.1 Background and Motivations

Recently GaN HEMT transistors, which were previously used only in RF and microwave regions since its invention decades ago, have been studied extensively. GaN-based power converters have appeared in power electronics, especially in low power high frequency DC-DC converters in recent years. In the past almost all GaN HEMT power transistors are deletion mode devices, which means normally-on when no voltage is applied at its gate (i.e., $V_{GS} = 0$ V). This greatly hindered the applications of this type of device in power electronics where a normally-off switch is greatly desired in power electronics. Usually a depletion-mode power device is potentially less reliable than a normally-off one from an applications perspective. It also needs a more specifically designed gate driver and control function since most gate drivers are designed to drive an enhancement mode device.

A breakthrough in processing GaN materials on a silicon substrate commercially made enhancement-mode GaN FETs finally a realistic alternative to conventional Si power devices. In 2009 Efficient Power Conversion Co. (EPC) announced eGaN ® series [1] enhancement-mode, a normally-off GaN HEMT power device. A power converter using GaN HEMT power switches could be as simple as using conventional Si MOSFET switches. Compared with their Si MOSFET counterparts, GaN HEMT power devices have much lower channel resistance due to higher electron mobility, significantly faster switching behavior due to much smaller gate charge and zero reverse recovery charge. However, unlike their Si counterpart, only several GaN gate drivers based on conventional totem-pole driving topologies are available on the market [2]. The gate driver provided on EPC websites for their eGaN ® series power devices are low-side driver LM5114 and half-bridge driver LM5113 from Texas Instruments. These gate drivers are specially designed for EPC devices. However, these gate drivers are still based on the conventional totem-pole structure working as a push-pull stage that in essence is a RC charging or discharging process. For a complete

RC gate charging and discharging process, all power will be finally dissipated through resistance. All gate charge accumulated on device gate during turning-on period will be finally dissipated to ground during the turning-off interval. If the switching speed of the gate driver continues increasing, the loss of the gate driver will increase as well. For GaN power devices expecting to be able to work at several MHz or even higher, the loss of the gate driver itself will be a limiting factor for their high-frequency applications.

To fully explore the advantages of GaN HEMT power devices, resonant gate driving techniques are a potential solution. However, currently there is no GaN gate driver IC designed for resonant gate driving conditions. The previously reported resonant gate driver for GaN devices using off-chip clamping diodes to implement resonant gate driving is not realistic for EPC eGaN devices and existing GaN gate drivers. Adding clamping diodes at the gate of EPC devices will significantly alter the working conditions of the GaN HEMT devices. Resonant gate drivers for customized depletion mode GaN devices have been reported but there is no resonant gate driver IC reported for enhancement mode GaN devices, such as commercial EPC eGaN series devices.

1.2 Objectives

As the maturity of GaN HEMT power devices continues growing, we can expect more and more gate drivers designed for this new type of power devices. This document is one of the efforts to design a new type of gate driver IC for EPC eGaN power device. The objective of the proposed work is to realize a resonant gate driving topology for eGaN devices (EPC2001 as an example), design a gate driver IC to support this topology and implement the proposed gate driving technique and compare the customized gate driver IC with the existing commercial gate driver ICs for EPC eGaN devices. By varying the resonant inductor and changing the driving sequences, the proposed resonant gate driver can work in different resonant driving conditions, or even the same way as the conventional gate driver. A more power efficient and more flexible gate driving technique is the purpose of this research work.

1.3 Contributions

The proposed research work is to make contributions in the following aspects.

- Propose a new resonant gate driving topology for enhancement mode GaN HEMT power devices (EPC2001 selected as an exmaple), meeting different resonant conditions by adjusting driving control signals without hardware re-design or re-programming.
- Design a new low-side resonant gate diver IC for EPC eGaN HEMT power devices in a standard CMOS process.
- Experimentally compare the switching frequency, power consumption and driving waveforms between the commercial gate driver LM5114 and customized resonant gate driver.
- Based on the experimental results and analysis on the proposed resonant gate driver design, provide guidance for future design.

1.4 Organization

This dissertation includes five parts. The first part is the introduction. It introduces the research background, motivations, objectives and contributions. Chapter 2 describes the GaN HEMT power devices and two associated gate driver topologies – conventional and existing resonant gate drivers. The limitations of these driver techniques are presented at the end of the chapter. The proposed work is in Chapter 3. First, a low-side resonant gate driving scheme using the proposed resonant structure is described. Then a half-bridge gate driver IC design using the same structure is proposed. Design blocks revealed and simulation results verified the proposed structures. Chapter 4 gives the experimental results. Finally, Chapter 5 is for conclusion and future work. After the conclusions in Chapter 5 the Appendix section includes some supplement materials such as customized IC and PCB layouts. The literature citations are listed in the References section.

Chapter 2

High-frequency Resonant Gate Drivers for Power Devices

2.1 Introduction to GaN HEMT Devices

To describe a Si MOSFET conduction, we have to consider a mechanism called "channel inversion" in a lightly doped Si substrate. Likewise, for a GaN HEMT (High-electron-mobility transistor) device, we must know the mechanisms of so called "two-dimensional electron gas", or 2DEG in short. The phase 2DEG refers to the condition where the electrons have quantized energy levels in only one spatial direction, often perpendicular to the interface, but often have extremely high mobility to move free in the other two dimensions, often parallel to the interface. Generally speaking, bringing an n-type wide band gap semiconductor layer in touch with a narrow band gap semiconductor layer will lead to a band bending in the conduction band of the narrow band gap semiconductor. In this way, a triangular well is formed, in which the transferred electrons are confined and form a two dimensional conductive channel, or 2DEG [3].

The phenomena of confining electrons along a surface may be tracked back to as early as the 1950's [4]. In 1964 Dr. W. T. Sommer demonstrated a layer of charge on the surface of liquid helium [4]. In the experimental chamber the electron discharged by an ion source with dc voltage applied was confined in an energy barrier of liquid helium. No later than 1987, the 2DEG electron layer in solid semiconductor materials was realized by a heterojunction supperlatice between n-type AlGsAs and intrinsic GaAs by Dr. Dingle and his team at Bell Laboratories [5]. The invention of the HEMT based on an AlGaAs and GaAs heterojunction structure was contributed to Dr. T. Mimura at Fujitsu Laboratories in 1979 [6]. He realized the control of electrons in that superlattice by a Schottky gate contact over a single AlGaAs/GaAs heterojuntion. In 1981 Dr. T. Mimura and his teams successfully fabricated and tested the first HEMT IC [7]. In the next few years, the AlGaAs/GaAs HEMT was successfully commercialized and first used in a LNA (Low Noise Amplifier) for radio

telescope detection [8].

Similar to the AlGaAs/GaAs heterojunction structure made from III-V compounds, the AlGaN/GaN heterojunction has its unique advantages. Firstly, as shown in Figure 2.1 [9] the bandgap energy versus lattice constant for numerous III-V compound materials, the bandgap energy for GaN is 3.4 eV, while GaAs is only 1.42 eVas shown in Table 2.1. Considering 1.12 eV for popular Si and 3.2 eV for SiC, 3.4 eV of GaN is a wide bandgap material. This results in much higher breakdown voltage and higher operational temperature, which is attractive for power electronics. Second, large lattice and large conduction band mismatch between AlN and GaN leads to a spontaneous polarization at the interface and a piezoelectric field in AlN [6]. A deeper quantum well formed in GaN at the edge leads to a very high sheet electron charge density in GaN interface, this formed structure creates a better 2DEG characteristics than conventional GaAs heterojunction. To the device perspective, this means a smaller size, less parasitic effects and higher operating frequency. A power device based AlGaN/GaN HEMT structure could be very attractive for today's high-frequency switching power applications.

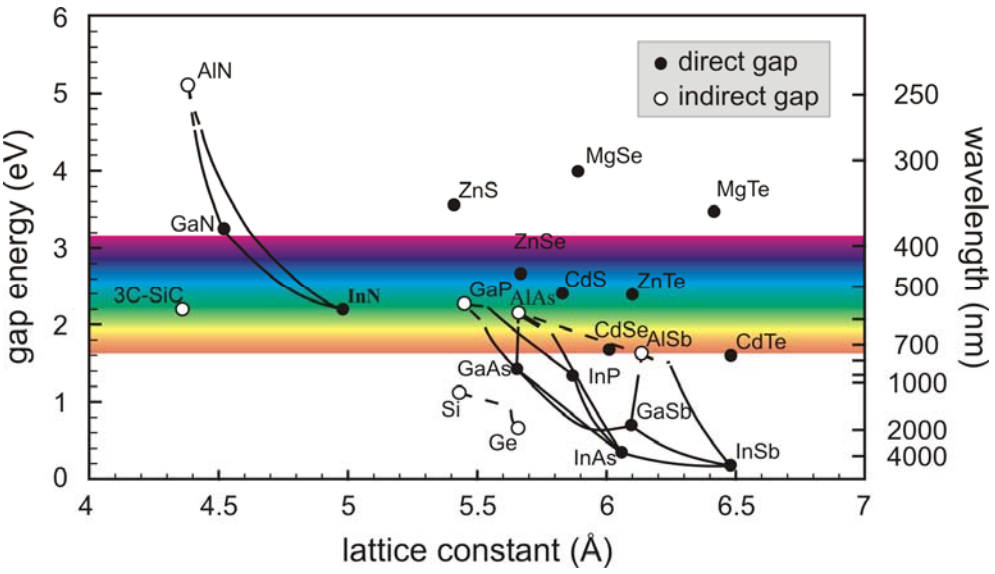


Figure 2.1. Bandgaps of the most important elemental and binary cubic semiconductors versus their lattice constant at 300°K [6].

The first AlGaN/GaN HEMT demonstrated by Dr. Asif Khan and his group in 1994 [10] was fabricated on sapphire substrate [11]. Then years later AlGaN/GaN HEMT grown on SiC substrate was reported [12] [13] and currently SiC is the substrate of choice for the epitaxial growth of high-

performance GaN HEMT devices with a thermal conductivity an order of magnitude greater than that of sapphire [14]. In the last decade or two, there has been a trend shift from the AlGaAs/GaAs HEMT to AlGaN/GaN HEMT. Currently the HEMT devices since its invention has been mostly used in microwave, high frequency low power applications. There are three potential substrate material for AlGaN/GaN structure, sapphire, SiC and Si. The sapphire substrate has poor thermal conductivity and large lattice mismatch to GaN. Expensive SiC has lower lattice mismatch and high thermal conductivity. Si substrate offers the the best trade-off considering the cost. Growing AlGaN/GaN heterojunction on Si substrate is one of the reasons hindering further expansion of this new device. Another obstacle for the application of AlGaN/GaN HEMT in power electronics is the difficulty of making a good enhancement mode device, which is especially preferred in power electronics.

Table 2.1: Material properties of Si, GaAs, SiC and GaN at 300°K [15] [16].

Properties	Unit	Si	GaAs	SiC-4H	GaN
Bandgap energy	E_G (eV)	1.12	1.42	3.2	3.44
Breakdown voltage	E_{BR} (MV/cm)	0.3	0.4	3.5	3.3
Electron saturation velocity	V_S (10^7 cm/s)	1.0	1.8	2.2	2.5
Electron mobility	μ (cm^2/Vs)	1450	8000	950	400 → 2000 [1]
Thermal conductivity	k (W/cmK)	1.5	0.55	5	1.3

There are mainly two solutions to realize an enhancement-mode power GaN FET device without losing the outstanding characteristics of the inherent depletion mode GaN 2DEG channel. One method is directly fabricating a depleted channel from the 2DEG layer. This method is adopted by EPC [1] and Panasonic [17]. Another way is to cascode an enhancement-mode Si MOSFET to the depletion-mode GaN HEMT. Transphorm [18] and International Rectifier (IR) [19] have this cascaded type high voltage GaN power transistor. Due to the processing limits, the most reliable direct enhancement-mode device is targeted to 100 V or below applications while a cascaded version can easily work at 400 – 600 V conditions. In 2013, Panasonic announced its 600 V GaN power transistor using its Gate Injection Transistors (GIT) techniques with 15 A drain

[1] The 2DEG increases the electron mobility of GaN from 400 to above 2000 cm^2/Vs.

current and 1.2 V threshold voltage [20].

In June 2009 EPC, announced the first enhancement mode wide bandgap AlGaN/GaN HEMT grown on Si substrate and fabricated with standard Si manufacturing technology and facilities [21]. The eGaN ® FET named by EPC is targeted in the open market as a replacement for the traditionally Si power MOSFET widely used in low voltage applications. Figure 2.2 shows the GaN FET cross-section structure [2]. The GaN materials are grown on a seed layer of AlN that is grown on a Si substrate. The 2DEG charge layer is formed between the thin AlGaN and GaN layer at the AlGaN side, but the region below the gate is depleted of free electrons. So the whole channel is partially depleted to have the enhancement mode gate threshold voltage without sacrificing the benefit of high mobility of 2DEG.

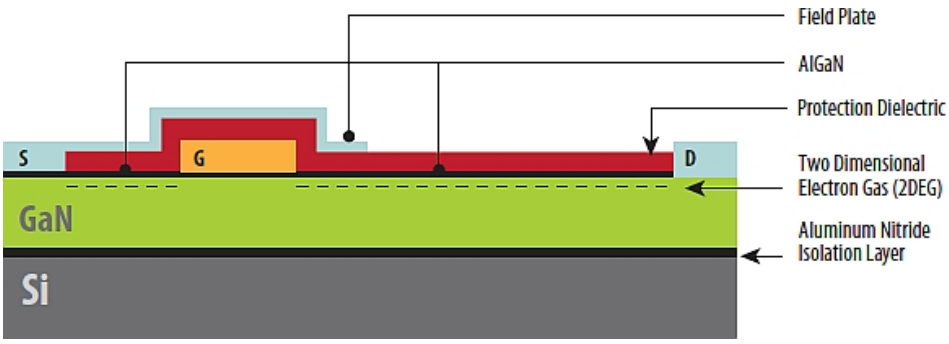


Figure 2.2. EPC eGaN ® FET structure [2].

There are several techniques to shift the negative threshold voltage associated with conventional depletion mode AlGaN/GaN HEMT devices to a positive threshold voltage. One of the methods called “gate injection transistor” is to use a p-type AlGaN named crapping layer beneath the gate electrode [22]. The p-type material injects holes into the AlGaN/GaN interface, lifts up the potential of the channel and depletes the 2DEG. Figure 2.3 shows a p-type to intrinsic AlGaN layers grown in a GaN layer to deplete 2DEG on the GaN side. However, one drawbacks of this structure is the gate to channel isolation is depends on thin layers of p-AlGaN and i-AlGaN. The p-type material and n-type conduction channel forms a diode-like structure. This means the enhancement mode GaN HEMT is very sensitive to gate voltage. A small overvoltage on V_{GS} could forward the gate-channel diode and destroy the device under high power conditions. Even though EPC did not disclose their techniques to manufacture an enhancement mode GaN device, the characteristics provided on the EPC datasheet illustrate the p-type hole injection or similar behavior.

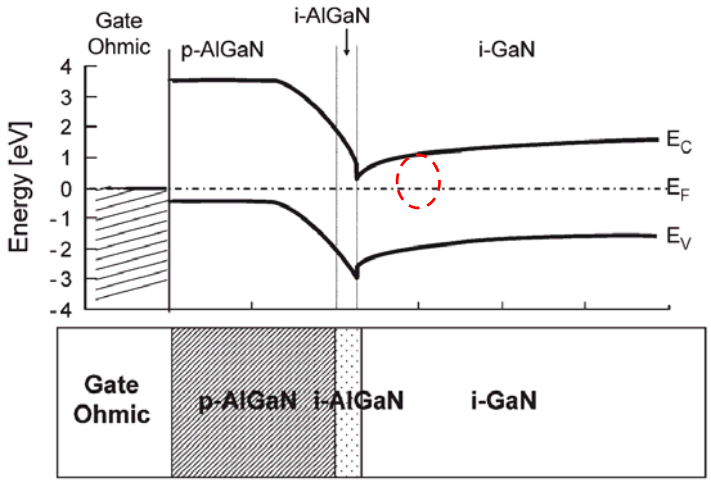


Figure 2.3. A p-AlGaN and i-AlGaN heterojuction implemented by gate injection transistor (GIT) displayed a depleted 2DEG for enhancement-mode operation [21].

The cross-section of an EPC eGaN FET is shown in Figure 2.4 [2]. Each lateral FET cell is laid on the GaN bulk material with inter-digitated layout pattern as "… G S G D G S G D …". The source nodes from each cell are routed to Metal 2 as in the graph. All these terminals are finally routed to top metal layers to the pads on the package. The characteristics associated with the electronic properties of the device will be described later in the gate driver design section.

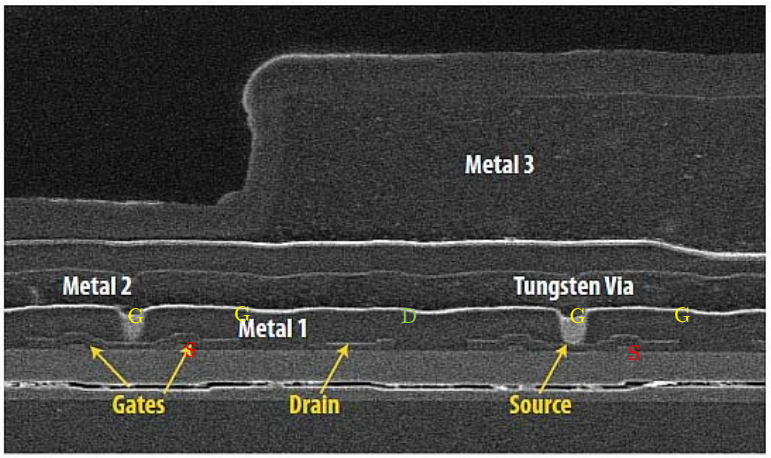


Figure 2.4. SEM micrograph of an EPC eGaN FET [15].

2.2 Conventional Gate Drivers for Power MOSFET's

Normally in power electronics applications the control signals are provided by a DSP, FPGA or other microcontroller IC's with voltages of 5 V, 3.3 V or even lower. Very few power devices can be directly driven by these digital signal outputs. An intermediate circuit is needed to convert the low power signals to drive the power switches. The gate driver IC is this circuit used to generate the voltage or current necessary to turn a power MOSFET, IGBT, or other semiconductor power switch on and off. For GaN HEMT FET, the gate driver IC is also needed.

The basic functions of a gate driver IC mainly include three aspects.

- Provide sufficient current/voltage control signals for power switching devices.
- Provide isolation or protection for control IC's from the large signal swings of the power switching devices.
- Provide protection for power switching devices under certain conditions.

There are possibly thousands of gate driver IC's for power devices on the market. Since the normally-off GaN HEMT is very similar to the conventional power MOSFET, which is also a voltage controlled threshold and capacitive induced channel device, we also call the GaN HEMT simply a GaN FET. Usually commercial FET gate drivers are based on the same topology called "totem-pole" structure for minimum transition time [23] [24] [25]. Figure 2.5 shows the simplified conventional "totem-pole" output stage driving a power MOSFET. The inverter-like M_P and M_N is the PMOS and NMOS transistors of the "totem-pole" respectively. The gate of the PMOS and NMOS are tied together to achieve fastest transient response. The drain nodes of the two transistors are connected together to form a push-pull output. Turning on the PMOS in the "totem-pole" will charge the output node and pull up the output potential to turn on the power device. Turning on the lower NMOS, the output node will be discharged below the threshold voltage of the FET device.

Among those thousands of various gate driver IC's, only three gate drivers from Texas Instruments — LM5113 [26], LM5114 [27] and UCC27611 [28] are listed on EPC website for the GaN FET's. Some other MOSFET gate drivers such as the ISL2110 [29] series from Intersil can also be used, but they are not specifically designed for EPC eGaN ® FET's. All of them have a "totem-pole" output structure with split pull-up and pull-down output pins. Figure 2.6

shows the block diagram of the LM5113 in which both high side and low side have the same "totem-pole" output [27].

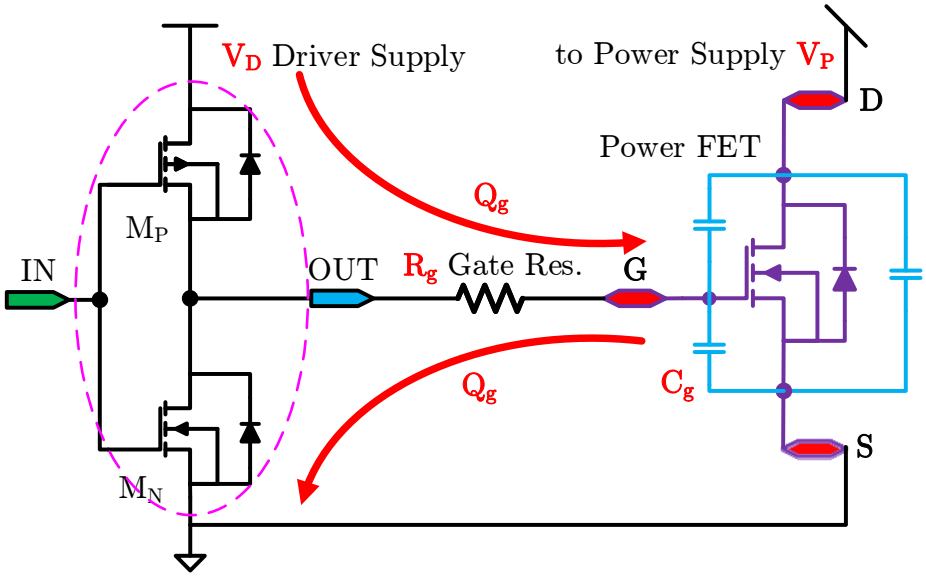


Figure 2.5. A simplified "totem-pole" output stage for a conventional power MOSFET driver.

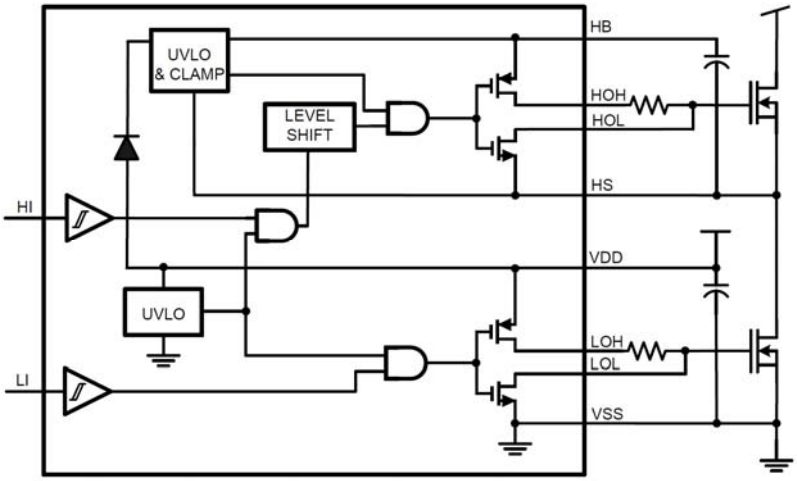


Figure 2.6. Block diagram of LM5113 [19].

To design a gate driver, we need to understand the power loss mechanisms for a "totem-pole" gate driving topology. Some literature defines the switching loss of output transistors and gate resistor loss separately [30], but they are all

essentially due to capacitive loss. In this work we define three types of power losses associated with the gate driver push-pull process.

- Static power loss P_S
- Dynamic capacitive power loss P_C
- Dynamic short-circuit power loss P_{SC}

The total gate driver power loss P_{GD} is the sum of the three types.

$$P_{GD} = P_S + P_C + P_{SC} \tag{2.1}$$

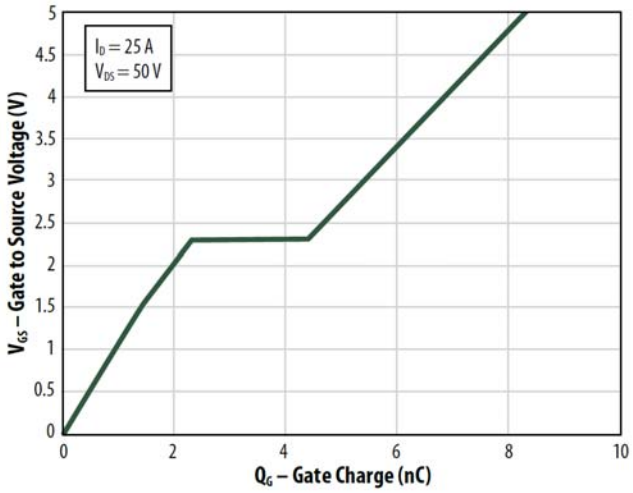


Figure 2.7. Gate charge versus Gate-source voltage for EPC2001 [30].

Static power loss is essentially due to transistor leakage current at its quiescent condition. There are two main sources of leakage, gate-channel leakage during turn on and drain-source leakage during transistor turn off. Other leakage like substrate leakage is common to all non-SOI (Silicon on Isolator) technologies [3]. Leakage loss usually is very small and can be neglected [3]. However, as temperature increases, leakage loss will increase dramatically [31].

Dynamic capacitive loss happens during the process of charging and discharging of load or any node capacitance on the drive signal path. Usually the load capacitance, which is the power device's effective gate capacitance, is much larger than other node capacitance. The Miller effect and other junction parasitics contribute to the nonlinearity of the device gate capacitance during operation. Figure 2.7 shows the gate charge versus gate voltage diagram for EPC2001 [32] as an example. Based on gate charge curve, the detailed loss analysis can be approximated by assuming a piecewise linear waveform and adding up three sections of loss during gate charging and discharging cycles [30].

However, a more systematic view can greatly simplify this analysis. Assuming the charging and discharging time is long enough such that the gate of the power device can be charged to the driver supply voltage and discharged to the ground potential, no matter what kind of resistance or nonlinear channel resistance there is, all the energy provided by the power supply will be dissipated during a complete switching cycle. Supposing the charge provided by driver supply without any leakage to the gate is Q_g, and the driver supply voltage is V_D, then the energy provided by the gate driver supply during a complete switching cycle is

$$E_{CG} = Q_g V_D \tag{2.2}$$

The energy supplied to the gate in each switching cycle is E_G. The power loss is simply the energy times the switching frequency, where C_G is the equivalent gate capacitance during the switching, normally larger than the static input capacitance given as C_{ISS} in the datasheet. Even though during the charging and discharging process there is a switching loss of the driving transistors themselves, while the transistor is in a saturation mode with resistance value significant larger $R_{DS(on)}$, the equation (2.3) has already includes this portion of loss. Some report this switching loss separately [30], but from the view of the overall loss of the gate driver, the loss due to the driving transistors is not necessary to be accounted repeatedly.

$$P_{CG} = Q_g V_D f_{sw} = C_G V_D^2 f_{sw} \tag{2.3}$$

The above equation shows that as switching frequency (f_{sw}) increases, dynamic capacitive power loss will certainly increase. Normally the output stage consists of several stages of ratioed "totem-pole" structure. If we assume an optimal stage effort of four [33], then the total capacitive loss including a chain of stages before the final output stage can be approximately expressed as

$$P_{CG}' \simeq \left(1 + \frac{1}{4} + \frac{1}{16} + \ldots\right) Q_g V_D f_{sw} = \frac{4}{4-1} Q_g V_D f_{sw} \simeq 1.34 C_G V_D^2 f_{sw} \tag{2.4}$$

Another portion of capacitive power loss for the gate driver is associated with the output parasitic capacitance of PMOS and NMOS FET's in the "totem-

pole" the gate driver. Since each PMOS and NMOS FET in an inverter has to charge the output capacitance to V_D during the turn-on stage and short it to ground during the turn-on stage, this portion of charge is completely dissipated during each switching cycle. The output parasitic capacitances associated with gate driver output stage are C_{Poss} and C_{Noss}, then gate driver dynamic output capacitive power loss is

$$P_{COSS} = (C_{Poss} + C_{Noss}) V_D^{\,2} f_{sw} \tag{2.5}$$

Considering the inverter chain as a whole, the gate driver dynamic output capacitive power loss is

$$P_{COSS}{}' \simeq 1.34 (C_{Poss} + C_{Noss}) V_D^{\,2} f_{sw} \tag{2.6}$$

Short-circuit power loss, or shoot-through power loss, happens during the transition of the upper PMOS FET and lower NMOS FET of the "totem-pole" structure. This is the same as a CMOS inverter behaves like a linear amplifier when both transistors are in the linear or saturated region [34]. This dynamic loss is unavoidable since we cannot have an ideal infinitely sharp transition region for the output stage. A portion of charge provided by the gate driver power supply has to be bypassed directly to ground without being routed to the gate of the power device. Even though short-circuit power loss is relatively much smaller than the capacitive loss, as switching frequency increases, this portion of loss also increases.

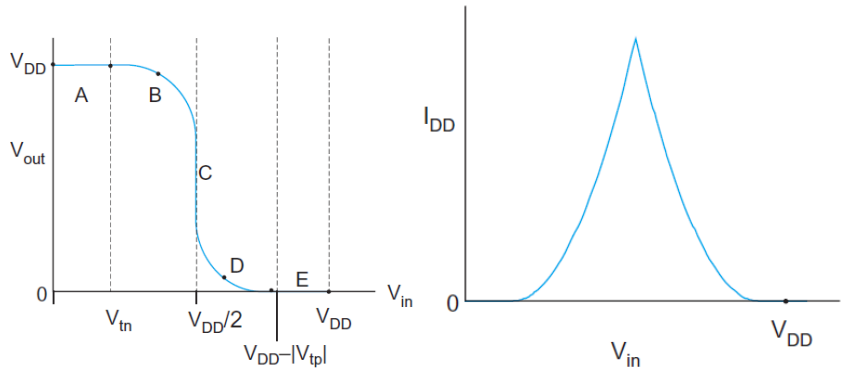


Figure 2.8. A CMOS inverter DC characteristics showing the dynamic short-circuit power loss. On the left is the output voltage vs. input voltage, on the right is the output current versus input voltage. "*B*", "*C*" and "*D*" means

the region where PMOS or NMOS is in linear or saturated region [26].

The short-circuit power loss can be estimated by a piecewise linear triangle approximation of the current waveform shown in Figure 2.8. Assuming the inverter-like "totem-pole" has a piecewise linear input slope, the short-through current is also a triangle waveform [35]. If the inverter equivalent transition time for pull-up or pull-down is t_{sc}, the peak short-circuit current is I_p, then short-circuit energy dissipated directly to ground is approximately [35]

$$E_{SC} = \frac{1}{2} V_D I_p t_{up} + \frac{1}{2} V_D I_p t_{down} = V_D I_p t_{sc} \tag{2.7}$$

Then the short-circuit power loss is

$$P_{SC} = V_D I_p t_{sc} f_{sw} \tag{2.8}$$

Similarly, consider an inverter chain of stage effort of four, the total short-circuit loss is estimated as

$$P_{SC}' \approx 1.34 V_D I_p t_{sc} f_{sw} \tag{2.9}$$

The dynamic short-circuit power loss is related to peak short-circuit current and transition time. There is a trade-off between the two parameters. Increasing the inverter PMOS and NMOS transistor sizes will increase the peak current and reduce the transition time. Increasing the inverter load capacitance will reduce the peak current but increase the transition time. The least short-circuit power loss depends on the sizes of the "totem-pole" output transistors and the gate capacitance of the power devices. A conventional gate driver will have least short-circuit power loss while driving for a specific power device loading condition. Changing the loading condition will increase short-circuit power loss and lower the gate driver power efficiency.

Based on the analysis above, the gate driver power loss for a conventional gate driver with four stages output and stage effort ratio of four can be expressed as

$$P_{GD} \approx 1.34 \left[\left(C_G + C_{Poss} + C_{Noss} \right) V_D^{\,2} + V_D I_p t_{sc} \right] f_{sw} \tag{2.10}$$

2.3 Resonant Power MOSFET Gate Drivers

A resonant gate driver has been proposed decades ago. One of the mostly cited pioneering literature on the resonant gate driver was written by Dr. Maksimovic during the early 90's [36]. Since that paper, the most important characteristics of resonant gate drivers has not changed. Unlike the conventional "totem-pole" driving scheme, the gate driving energy is completely dissipated in the resistance during the process of charging and discharging the gate of a power MOSFET device. Given that this is an equivalent RC network, the only way to apply and remove the capacitive charge during a signal transition cycle is to dissipate the charge completely via a resistive element to ground. Resonant gate driving implements the charging and discharging process by a LC resonant network. For an ideal lossless network, the capacitive energy will resonate with the inductive energy, which means no loss occurs during a complete cycle. A resonant gate driver implements a quasi-square-wave voltage applied at the gate of a power device by employing a resonant process during the conventional charging and discharging process.

The driving forces of proposing a relatively new resonant gate driving topology rather than conventional "totem-pole" output driving stage can be contributed to two main aspects. Firstly, as switching frequency keeps increasing for power converters, gate driving loss is also proportionally increasing. In the past, this portion of power loss was often times negligible compared with the switching loss and conduction loss of the power devices. Today, for low power DC-DC converters, several MHz switching frequency is normal, and gate driving loss is by no means negligible. Second, soft switching techniques, such as zero-voltage-switching (ZVS) [31] and zero-current switching (ZCS) [31], are getting more and more popular. The switching loss of the power switches in the power loop has been reduced. However, soft switching can result in more circulating current, which leads to higher conduction loss. To reduce the conduction loss, devices with lower $R_{ds(on)}$ are preferred. Normally there is a trade-off between the Q_g and $R_{ds(on)}$. The power MOSFET Figure-of-Merit (FOM, $FOM = Q_g R_{ds(on)}$) [2] suggests this. A lower $R_{ds(on)}$ normally means a higher Q_g for a given device technology at a given voltage rating. A higher Q_g will need a larger gate driver capability, such that a higher gate driving loss will be consumed if a conventional gate driver is still in use. So resonant gate driving techniques are developed to reduce the gate drive loss while allowing the increase of switching frequency or the device gate input capacitance.

Here we listed several candidate resonant gate drivers developed so far for detailed review. All of them are designed to drive a single power device as load. Other types of resonant gate drivers, especially those driving two MOSFET's with transformer coupled techniques, which is not suitable for low power applications and IC integration, will not be discussed in detail. Also, for low power applications, for power MOSFET or GaN HEMT, both of them can be treated as a non-linear gate capacitance to the gate driver. So the gate drivers discussed here are all capacitance loaded gate drivers.

2.3.1 Resonant Gate Driver – Topology A

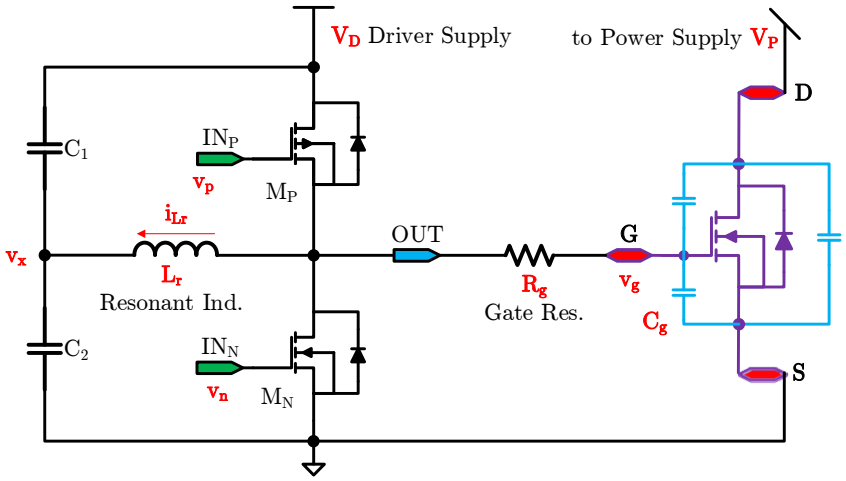


Figure 2.9. A resonant gate driver using extra resonant inductor and capacitors [34].

Figure 2.9 shows a resonant gate driver proposed by Dr. Maksimovic in the early 90's [34]. The operation principle of the above resonant gate driver can be explained with the waveform diagram in Figure 2.10. The equivalent capacitance connected to net "v_x" is much larger than the power device input capacitance C_G, such that the resonant conductor current can be approximated as triangle wave. Furthermore, if we assume an ideal lossless resonance and ideal timing condition, the resonant current will flow back and forth with the same amplitude. When p-channel FET M_P is turned on, the current i_{Lr} increases linearly, from the negative peak current -I_{Lr} to the positive peak current +I_{Lr}. Then M_P is turned off, the positive peak current will discharge the gate input

capacitance C_G. The gate charge energy will be ideally transferred to energy stored in the equivalent capacitance of C_1 and C_2. As the gate capacitance is discharged to ground potential, the n-channel FET M_N is turned on, the inductor current i_{Lr} decreases linearly, from the positive peak current $+I_{Lr}$ to the negative peak current $-I_{Lr}$. Then M_N is turned off, the negative peak current will charge the gate input capacitance C_G to the desired turn-on voltage, the gate driver supply voltage V_D. Then repeatedly, M_P is turned on again and i_{Lr} increases linearly.

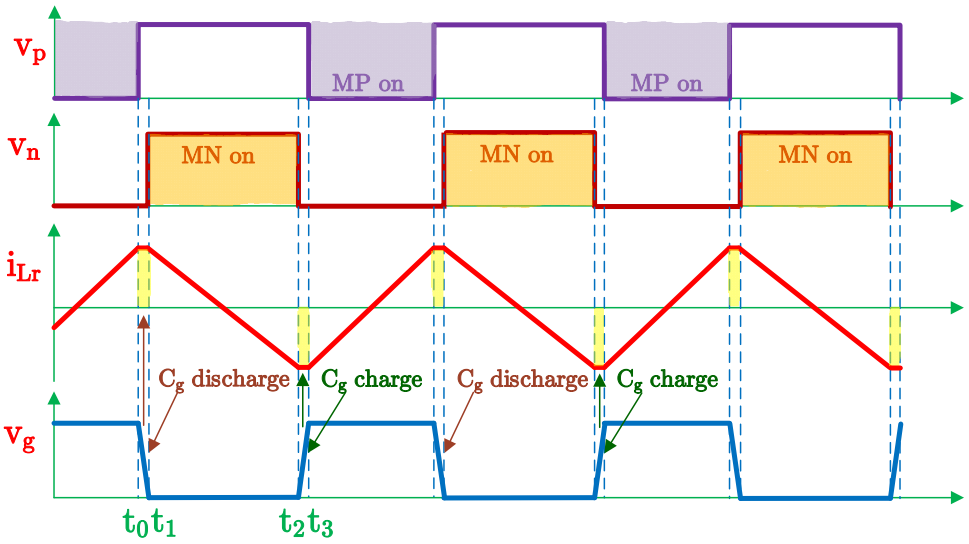


Figure 2.10. Simplified steady state waveforms of the gate driver in Figure 2.9, from top: driver output PMOS M_P gate voltage v_p, driver output NMOS M_N gate voltage v_n, resonant inductor L_r current i_{Lr} and power device gate G voltage v_g.

The resonant gate driver showed in Figure 2.9 is essentially adding an extra resonant inductor and load capacitor to the "totem-pole" gate drive output to form an unloaded ZVS quasi-square-wave buck converter [37]. The most significant advantage of this resonant gate driver is the realization of the ZVS switching of the gate driver output transistors. However, it suffers other problems. Firstly, a significant larger resonant capacitance than the power device gate capacitance is necessary to maintain a triangle wave like inductor current. This could be costly to integrate on chip. Secondly, a separate inductor is needed to form the gate resonant loop. The inherent parasitic gate inductance cannot be incorporated into this inductor. Thirdly, a large continuous current flows through the LC resonant loop. The parasitic loop resistance, especially the

equivalent series resistance (ESR) of the inductor, will give rise to conduction loss.

2.3.2 Resonant Gate Driver – Topology B

Figure 2.11 shows another resonant gate driver published in 2002 [38]. This topology utilizes the gate inductance to form the charging or discharging by LC resonance. The simplified steady-state waveforms of control logics, inductor current and device gate voltage are shown in Figure 2.12. Assume the gate capacitance of power device C_G has been discharged to the lowest negative potential V_{p-}, while M_N is on and M_P is off. The diode blocks the reverse flowing current with voltage of - V_{p-}. Then a rising edge of control signal drives M_P to turn on and M_N to turn off. A positive gate driver voltage V_D is applied across the series resonant tank composed of inductor L_r and device capacitance C_G. The C_G will be charged to its positive maximum potential V_{p+} through M_P and D_1, given the resonance is longer than a half period. The charging current will be a positive half sinusoidal waveform. The negative discharging current of a normal resonant cycle is automatically blocked by the series diode, D_1. The device C_G potential will be maintained at V_{p+} until a falling edge of control input signal occurs. At this moment, the device gate potential will be discharged through inductor L_r, D_2 and M_N. The inductor current will go through the negative half sinusoidal cycle to discharge the gate capacitance to the minimum potential of V_{p-} and maintain this gate voltage level by the reversely blocking of D_2.

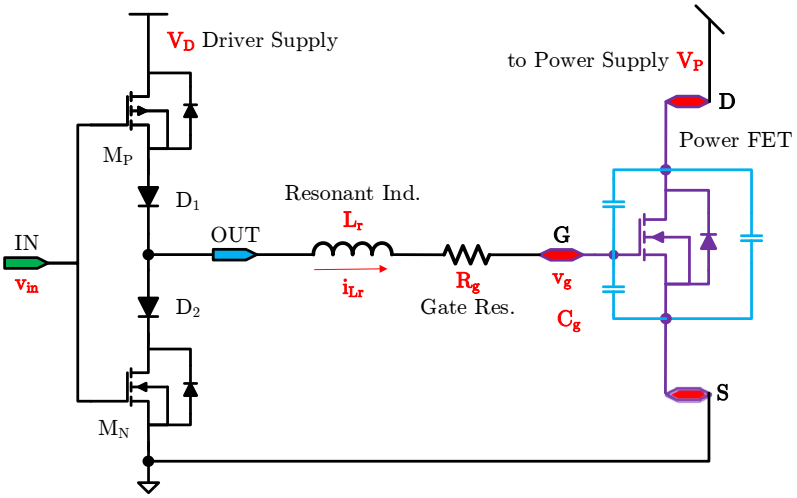


Figure 2.11. A resonant gate driver using gate inductor and reverse blocking diodes in series [36].

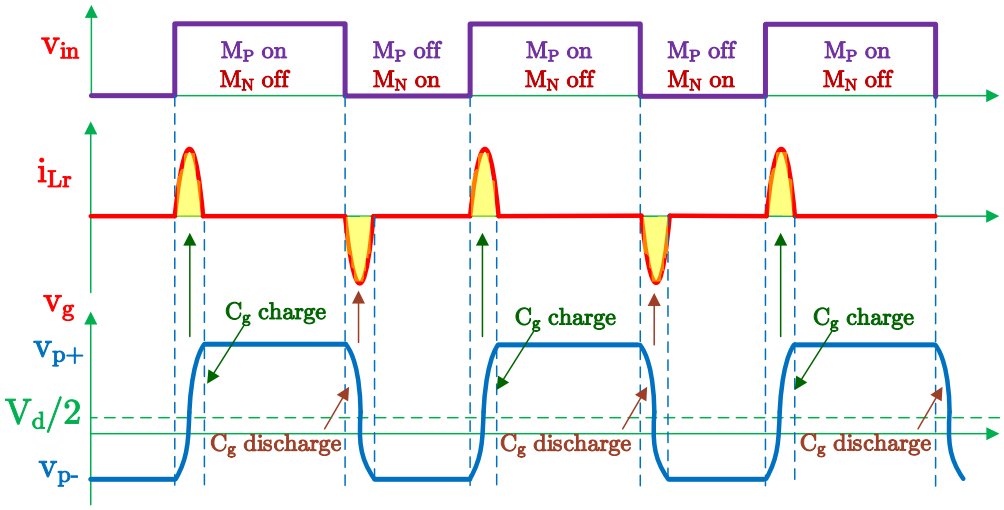


Figure 2.12. Simplified steady state waveforms of the gate driver in Figure 2.11, [from top:] driver control input *IN* voltage, resonant inductor L_r current and power device gate *G* voltage [36].

Compared to the gate driver with resonant transition [39], this resonant gate driver does not require a separate capacitance to assist gate resonance. The resonant inductor can be implemented by the parasitic inductance between the gate driver output and device gate input, or even possibly integrated on chip. Another advantage of this gate driver is the lower gate driver supply voltage. A resonant condition can make the positive charged gate voltage much higher than the gate driver voltage supply. This could be attractive for high gate voltage devices. However, for the current enhancement mode power GaN HEMT's, the optimum gate turn-on voltage is around 5 V or even less, further lowing the gate driver supply beyond that level will only create complexity by requiring an extra supply. Since the gate voltage completely relies on the exact values of resonant components, the desired gate turn-on and turn-off levels need carefully turned to these values. For example, if the minimum negative swing needs to be 0 V, the author recommended to increase the resonant capacitance by series capacitor, and a clamped Zener diode in parallel with the device gate input. To control the desired maximum positive gate voltage independently, the resonant inductor has to be split separately for the charging and discharging path, such that their resonant process can be controlled separately. All these problems make this solution not applicable to the desired gate driving for high-frequency switching with GaN HEMT's.

2.3.3 Resonant Gate Driver – Topology C

Even though the research on the resonant gate driver can be traced back to 1980's, the widespread interests on this topic started early this century. Among these papers published during that period, one of the most typical resonant gate driver papers proposed by Dr. Chen brought up the implementation of resonant gate driver "energy recovery" [40] [41] rather than the previous ideal "lossless" approach [34] [36]. Figure 2.13 shows the proposed resonant gate driver topology [38] [39]. We need to assume the Q factor of the resonant circuit is large enough such that an ideal resonance can be approximated.

The approximated waveforms are shown in Figure 2.14. The shaded area is the turn-on period of PMOS and NMOS driver switches. The highlighted portion of current is the actual charging and discharging gate current.

Before time t_0 the gate capacitance of power device C_G has been discharged completely to ground, and both M_N and M_P are off. The turn-on and turn-off process can be divided into the following four intervals.

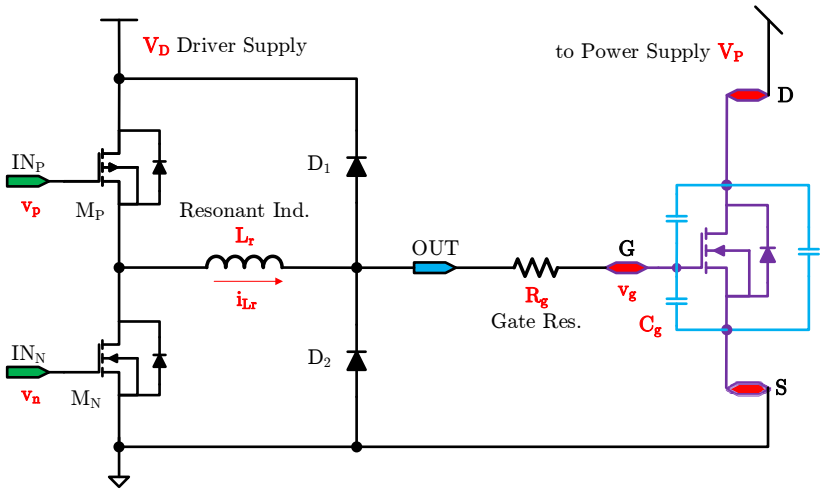


Figure 2.13. A resonant gate driver using gate inductor and gate clamping diodes in parallel [38] [39].

1) L_r resonant charge interval t_0 - t_1:

At time of t_0 a negative pulse on IN_P turns on the switch M_P, a positive current i_{Lr} will flow from the driver supply V_D through the resonant inductor L_r to charge the gate capacitance C_G. If the turn-on period of M_P is long enough, the gate capacitance C_G will be charged beyond gate driver voltage V_D. Due to

the paralleling diode D_1, the gate voltage will be clamped at V_D starting from t_1.

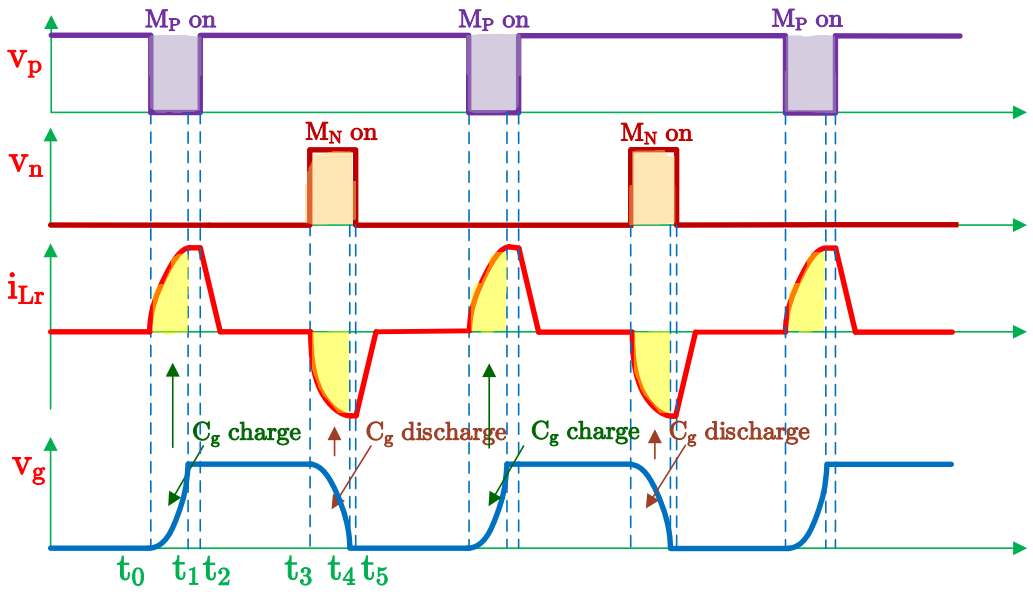


Figure 2.14. Simplified steady state waveforms of the gate driver in Figure 2.13, [from top:] gate driver PMOS M_P gate control voltage v_p, NMOS M_N gate control voltage v_n, resonant inductor L_r current i_{Lr} and power device gate G voltage v_g [38] [39].

2) D_1 clamping and recovery interval t_1 - t_2:

During the interval t_1 - t_2 the gate voltage clamping the inductor current will keep constant or clamped at its peak value via the freewheeling loop of M_P, L_r and D_1. At time t_2 the M_P will be turned off, inductor current cannot change promptly, it will continues flowing through the body diode of M_N and D_1 back to the driver supply. The constant negative voltage applied across the inductor will discharge the inductor current linearly until it vanishes completely. During this charging recovery period, all the gate charge has been returned to the driver supply.

3) L_r resonant discharge interval t_2 - t_3:

At time t_3 the n-channel driving transistor M_N is turned on, previously clamped gate voltage V_D at C_G will be discharged through the resonance with L_r. Again the gate voltage will be discharged during t_2 - t_3 and clamped by D_2 to 0 while the inductor current will reach its negative peak value and keeps freewheeling in the loop of M_N, L_r and D_2.

4) D_2 clamping and recovery interval t_3 - t_4:

At time t_4 turning off M_N will force the existing negative inductor current to be discharged through the body diode of M_P and D_2 back to the driver supply. This is the discharging recovery period. If there is no resistive loss involved during the process, then during the charge period, half of the energy provided by gate driver supply will be stored at the gate capacitance C_G voltage and the other half will be stored at inductor L_r current. During the discharge period the capacitive energy will be exhausted to 0 and transferred into inductor current. In either case the inductor current will be completely discharged to the driver supply during the recovery period.

2.3.4 Resonant Gate Driver – Topology D

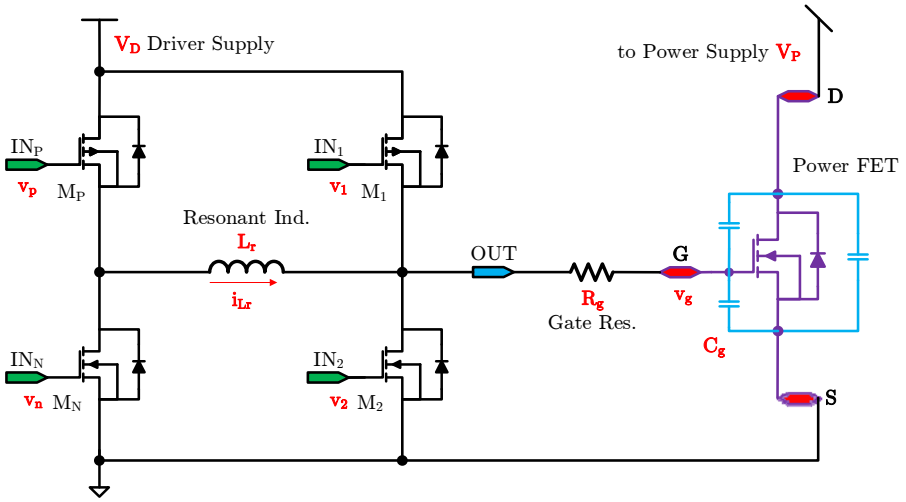


Figure 2.15. A resonant gate driver using gate inductor and gate clamping diodes in parallel [40] - [43].

Figure 2.15 shows another resonant gate driver topology also implemented with a series inductor in the gate driving loop to recover a portion of the driving energy [42] [43] [44] [45]. It utilizes extra two driving transistors in replace of the two clamping diodes proposed in Figure 2.13. The extra two transistors are not simply to reduce the forward conduction loss of a diode with a MOSFET being turned on. Before the charging and discharging process, a direct path connecting the resonant inductor to the driver supply can be built by turning on diagonal transistors, including one of these extra transistors, such that an initial non-zero charging or discharging current can be used to turn on or turn

off the power switch. Traditionally the gate driver applies the driver voltages to the gate of a power device, such that a driving current always starts from zero. An ideal current pulse leads to a faster gate charging and discharging process and shorter transition time for both gate driving loop and power loop to reduce switching loss. The resonant inductor plays an important role to apply this non-zero charging and discharging current. It is also called "current source gate driver" since the inductor behaves like a constant current source while charging and discharging the power FET gate capacitance [46] [47].

Again assuming a sufficiently large Q factor, the idealized signal waveforms of the four-transistor driver are shown in Figure 2.16. The two switches on the left leg are named as M_P and M_N (Figure 2.15) since they are the main switches providing charging and discharging current, respectively. The two on the right leg are mostly for clamping, freewheeling and recovery purposes, so they are labelled as M_1 and M_2 as C stands for "clamping". Before time t_0 both M_N and M_2 are turned on, the gate capacitance C_G is completely discharged to ground, the power device is turned off. The turn-on process can be divided into three intervals and discussed in detail.

1) L_r pre-charge interval t_0 - t_1:

The M_N is turned off and then M_P is turned on following a dead time interval. The resonant inductor L_r is connected to driver supply with the loop M_P - L_r - M_2. Due to the inductor current can must starts with 0, the M_P is turned on with ZCS. The inductor current is then ramped up linearly to a non-zero pre-charge inductor current.

2) C_G charge interval t_1 - t_2:

With the turning off of the clamping NMOS M_2 at ZVS, the non-zero pre-charge current is now steered into the gate of the power device. A resonant loop is formed with M_P - L_r - C_G. With the non-zero inductor current, the turn-on transition has been accelerated by providing C_G more charge within a given charging time. The gate voltage is clamped by the body diode of M_1 and the positive peak inductor current will freewheel in the loop of M_P - L_r - BDM_1.

3) L_r recovery interval t_2 - t_3:

With the turning off of the charging PMOS M_P at ZVS, the inductor current is immediately steered through the body diode of M_N. The conduction loop is BDM_N - L_r - BDM_1. After a short dead time, M_N is turned on with ZVS after the body diode conduction occurred during the dead time. The PMOS clamping M_1 is also turned on with ZVS due to its body diode condition. The conduction loop is now M_N - L_r - M_1. The inductor is now reversely connected

to the driver supply. The inductor current is ramped down linearly and returned to the driver supply V_D.

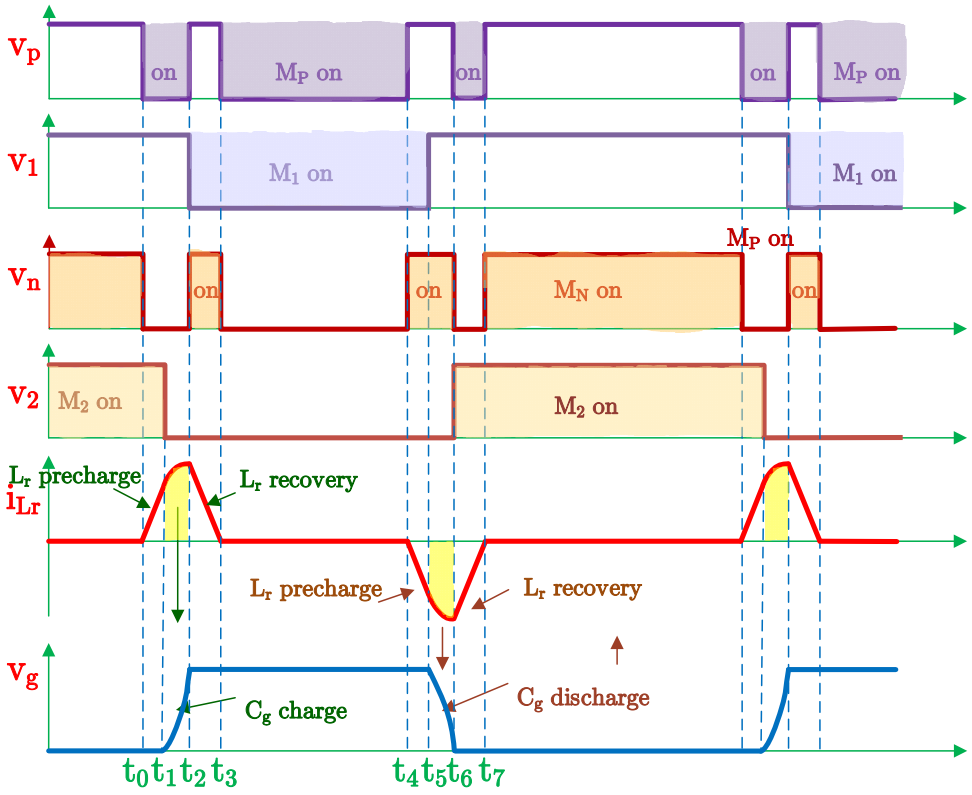


Figure 2.16. Simplified steady state waveforms of the gate driver in Figure 2.15, [from top:] gate driver PMOS M_P gate control voltage v_p, clamping PMOS M_1 gate control voltage v_1, driver NMOS M_N gate control voltage v_n, clamping NMOS M_2 gate control voltage v_2, resonant inductor L_r current i_{Lr} and power device gate G voltage v_g [40] - [43].

If the M_N is turned off before the recovery current is reduced to zero, the residual current will flow through the body diode of M_P again. Then turning on M_P will freewheel the any rest current through the M_P - L_r - M_1 loop. If the M_N is turned off after the recovery current reduced to zero. The negative current will start to build up through the inductor, turning on M_P will still freewheel any initial negative inductor current through the M_P - L - M_1 loop. In either case, the PMOS clamping transistor M_1 is always on, so the gate voltage is always clamped to V_D. At the same time, turning on M_P is always close to ZCS condition.

The discharging process is a reverse procedure of the charging process. A negative non-zero inductor current required by gate discharging is initiated by

turning off M_P and turning on M_N through the loop M_1 - L_r - M_N. Turning off PMOS clamping M_1 will quickly start the discharge of gate capacitance via loop C_G - L_r - M_N. The gate capacitance is finally discharged and clamped at ground, a freewheeling peak discharging current is now applied to the loop of BDM_2 - L_r - M_N. Turning off M_N and then turning on M_P with ZVS will form the loop of M_2 - L_r - M_P to recovery the negative inductor current to the driver supply. Finally, after turning off M_P and turning on M_N, the negative clamping condition is maintained until the next turn-on cycle.

The most distinct characteristics of this proposed resonant gate driver is the specific controlling sequence of the four driver switches to conduct the conventional resonant process. A pre-charge inductor current can be built up before charging or discharging the power device gate capacitance. The diodes of the recovery process in Figure 2.13 are replaced by controlled clamping switches M_1 and M_2 to further reduce the driving loss. However, these improvements may not be beneficial for GaN HEMT devices. For example, the driving switches M_1 and M_2 are switching three times as much as the power MOSFET does. If we want to have a 10 MHz converter switching frequency, these two driving transistors in the gate driver will need to switch at 30 MHz no matter if there is a pre-charge period for inductor current or not. Even though these switches are working at quasi ZVS or ZCS conditions, switching at this high frequency with enough accuracy is still very challenging.

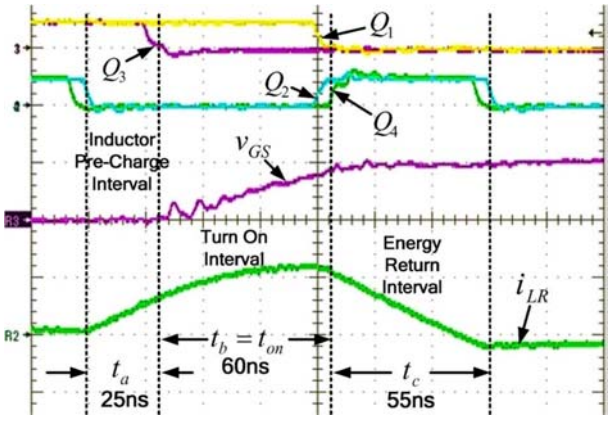


Figure 2.17. Measured waveforms of the turn-on process of a rectifier working at 1.5-MHz switching frequency. [From top:] M_1 (Q1) and M_2 (Q3) gating signals (10 V/div and 20 ns/div), M_P (Q2) and M_N (Q4) gating signals (10 V/div), power-MOSFET gate voltage V_g (5 V/div) and inductor current i_{Lr} (1 A/div). [43].

The reported resonant gate driver was tested on a full-bridge rectifier with two pairs of synchronous rectifier power switches providing 35 A maximum load at 1 V output [43]. Two IRF6691 [48] MOSFET's in parallel forms each power switch. The tested waveforms in Figure 2.17 shows the turn on process [43]. The gate charging time is about 60 ns and the whole turn on process is about 140 ns. The peak charging current is about 1.2 A. A higher switching frequency and the larger peak current required by GaN HEMT's makes the design of a gate driver based on this topology difficult.

2.3.5 Resonant Gate Driver – Topology E

Figure 2.18 shows an H-bridge resonant gate driver [49] [50] [51] with similar topology to Figure 2.15. However, this resonant gate driver implements the resonance process without connecting to the driver supply. The gate voltage can be charged to a positive level and discharged to a negative level with the same amplitude. This negative applied gate voltage is often used for high voltage and high power conversions. For the low power case, normally discharging the gate to 0 V is sufficient. The operation principle can be explained using the waveforms in Figure 2.19. Again we assume a sufficiently large Q-factor in the resonant loop such that an approximately ideal waveform can be achieved. Before time t_0 the M_{P2} and M_{N1} are turned on, and a negative V_D is applied at the gate G. At t_0 M_{P2} is turned off and M_{N2} turned on, a resonant loop M_{N1} - L_r - C_G - M_{N2} is formed. After a half resonant period, the initial capacitive voltage energy transferred to inductive current energy is returned to capacitive the gate voltage on resonant capacitance C_G with inverted polarity. The gate of the power switch is now positively charged. Then M_{N1} is turned off and M_{P1} is turned on. The driver supply will charge the gate voltage drop due to the loss during the half-cycle resonance. The gate discharging process is similar. Turning off M_{P1} and turning on M_{N1} at t_2 will again start the resonance as the same loop M_{N1} - L_r - C_G - M_{N2}. Since the gate voltage is initial positive, after half-cycle, the gate voltage will be inverted. Then turning off M_{N2} and M_{P2} turned on at t_3 will refresh the negative gate voltage.

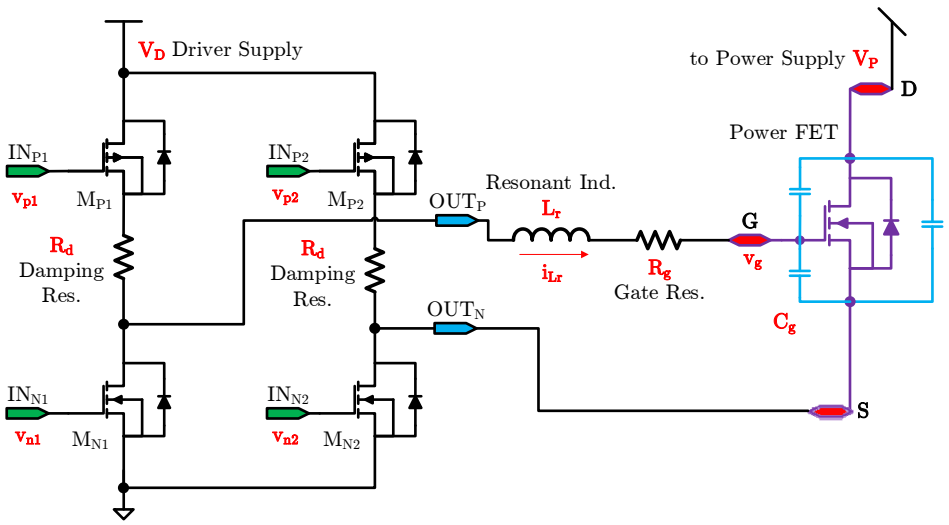


Figure 2.18. An H-bridge resonant gate driver using gate inductor in series [47] [48] [49].

This resonant gate driver has the advantage of simple gate control signals. The gating signals for M_{P1} and M_{N1}, or M_{P2} and M_{N2}, are essentially the same except with dead time in between. However, especially for applications of low power conversions, very few power switches need a symmetric positive and negative gating signals, otherwise the transition speed will be unnecessarily reduced. During one cycle, the four driving switches each has to dissipate its output capacitance charges with driver supply voltage across it. For the resonant loop M_{N1} - L_r - C - M_{N2}, the resistance should be as small as possible. When the M_{P1} or M_{P2} is connected, resonance should be depressed quickly such that an R-C like charging from the driver supply will compensate the gate voltage loss in the resonance. A damping resistor R_d has to be placed in series with M_{P1} and M_{P2} to stop the resonance. This resonant gate driver was tested in a 1 kW, 350 kHz, 230 VDC input inverter with resonant load [49]. The driven power switches are APT50M50 [52] power MOSFETs with more than 16 nF input capacitance at typical conditions. Based on these characteristics, this H-bridge resonant gate driver is not suitable for applications of the very high speed GaN HEMT with low Q_g.

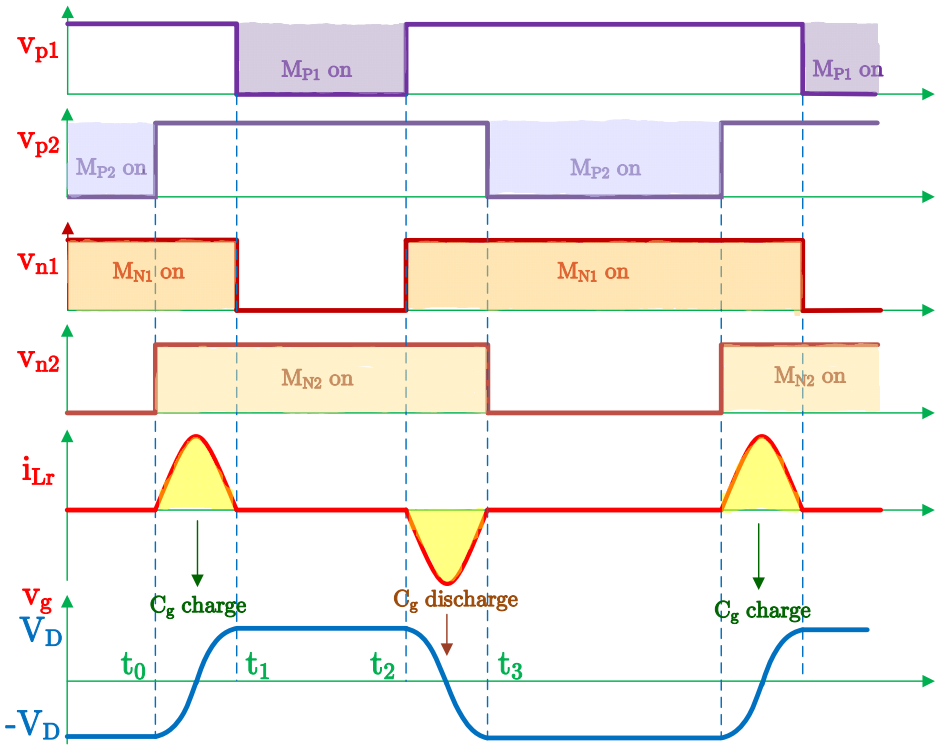


Figure 2.19. Simplified steady state waveforms of the H-bridge resonant gate [47] [48] [49].

2.3.6 Resonant Gate Driver – Topology F

Figure 2.20 shows an H-bridge resonant gate driver with extra diodes and capacitors to enhance the separate charging and discharging process [53]. This topology is an updated version of topology D [40] - [43]. Two resonant inductors (L_{ron} and L_{roff}) are each in series with two diodes (D_{on} and D_{off}), respectively, with different polarity connections implemented to direct current flow into the different inductors. The capacitors (C_{POS} and C_{NEG}) are connected in such a way that charging and discharging current flows into one of them. The charging resonant loop is M_P - L_{ron} - D_{on} - C_G - C_{POS}. The discharging resonant loop is M_N – L_{roff} - D_{off} - C_G - C_{NEG}. It is claimed as having "a programmable magnitude of the discharge current" and "a tunable turn-on current" [51]. Both the turn-on and turn-off current can be modified by the values of their resonant inductor and capacitor to match the desired transition performance. The detailed analysis is not included here, but the working principle behind it has been previously discussed.

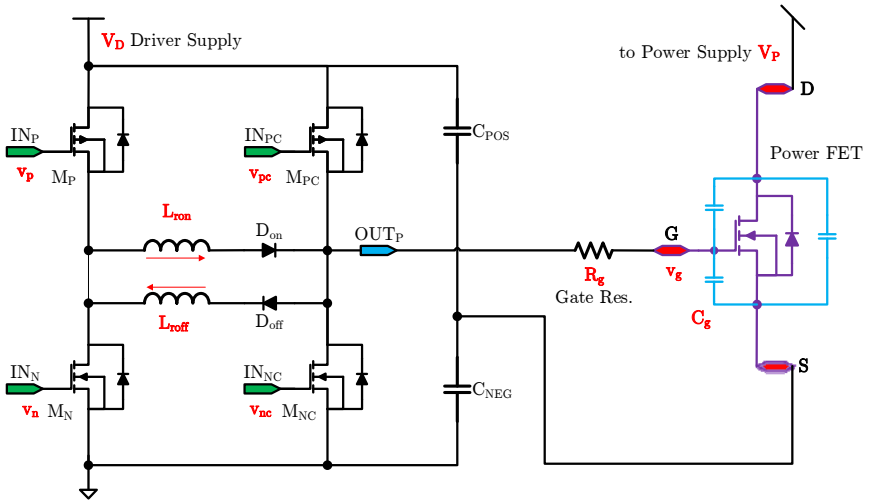


Figure 2.20. Another H-bridge resonant gate driver using gate inductor in series and capacitor voltage divider [51]

2.4 Resonant Gate Driver Design Considerations for Power GaN HEMT's

Several resonant gate drivers have been analyzed in the last section. From the early 90's to the most recent patent in 2013. All of them are implemented at the PCB define level using conventional gate driver IC's and discrete resonant inductors. We have noticed the trend that the resonant gate driver is adding more and more complex output stages and more resonant components. The power loss reduction could be up to 90% [47] compared with a conventional gate driver. But all of them suffers difficulties if we need to further improve the frequency as more detailed resonant control means more complex control signals. The resonant gate driver in [40] is an example of two driving switches having be switched three times as often as the power conversion switching frequency. The resonant gate driver in [51] is an example using more passive components to have a desired resonant control. The trend developed for conventional power MOSFET is adding more and more extra components and more control mechanisms than the conventional structure to implement the gate resonance. For current commercial enhancement mode power GaN HEMT, the gate capacitance is much smaller than the conventional power MOSFET. For example, EPC2001 [30] has only 950 pF maximum input capacitance while the peak gate driving current could be as large as 4 or 5 A when driven by

conventional gate driver IC's [25] [26] [27]. At such peak current condition with low gate capacitance, the extra components, either diodes or driving switches, will create unexpected parasitic effects leading to degraded resonant gate driving.

This work tries another direction. Without complex modifications to the gate driver output stage, change in the driver IC topology may enable the driver to control the output stage to work with parasitic gate inductance in realizing resonant gate driving. Parasitic gate inductance should always be minimized using a conventional gate driver. Resonant gate inductance is often added for high power, low frequency gate driving conditions.

In this work, the development of a novel GaN resonant gate driver seeks to reach a balance between them. The conventional design principle from PCB level to converter level should still be followed such that gate parasitic inductance should be minimized. For the unavoidable last portion of the gate inductance, without significant changes at the driver output topology, by updating the driver IC design, this portion of gate inductance, from the IC pads, bond wires to the PCB traces, can be incorporated into the resonance input capacitance of the commercial fast-switching GaN HEMT devices. Without such improvement, the conventional gate driver will finally suffer ringing due to the parasitic capacitance as switching frequency gets higher and higher.

Chapter 3

A Fully-Integrated Resonant Gate Driver for Power GaN Devices

3.1 Introduction to the eGaN FET

The GaN HEMT's power device has many different electrical characteristics from the conventional Si power MOSFET's. Implementing a resonant gate drive for such a device should have the benefits of energy saving without sacrificing the inherent superior performance of GaN device. Even though many different Si power MOSFET's technologies are available on market, most Si power MOSFET's technologies are derived from Vertical Diffused MOS (VDMOS) structure to maximize the power density for an increasing breakdown voltage rating requirements. However, all GaN power devices from EPC are lateral structure.

To better understand the differences between these two types of devices, a comparison in Table 3.1 is made for a GaN and other selected Si power FET's with similar blocking voltage V_{DSS}, current rating I_{DS}, and on-channel resistance $R_{DS(ON)}$. The BSZ035N03MS [54] is from Infineon with its innovated OptiMOS™ 3 technology. The model IRLH7134PbF [55] is provided by International Rectifier with the well-known HEXFET® Power MOSFET technology. EPC2015 [56] is the one of the eGaN ® series power devices provided from EPC. Both MOSFET's with OptiMOS™ and HEXFET® technologies are vertical structure. We will focus on the differences between gate voltage, gate charges, input/output capacitance and body diode in the following.

- Gate voltage

The gate voltage rating for eGaN FET is much smaller than Si MOSFET. This is similar voltage and current capability and channel resistance.

Table 3.1: Device characteristics for three typical power transistors with

	V_{DSS}	I_{DS}	$R_{DS(ON)}$	V_{GS}	V_{TH}	Q_G	Q_{GD}	C_{ISS}	C_{OSS}	Q_{rr}	V_{SD}
	V	A	mΩ	V	V	nC	nC	pF	pF	nC	V
BSZ035N03MS	30	40	4.3 [1]	±20	1-2	27	5.9	4300	1200	⩽20	0.81
IRLH7134PbF	40	50	3.9 [2]	±16	1.0-2.5	39	16	3720	610	25	⩽1.3
EPC2015	40	33	3.2 [3]	-5, 6	1.4	10.5	2.2	1100	575	0	1.75

mainly due to the lack of excellent isolation performance provided by gate oxide layer in the GaN structure. However, the threshold voltage is about the same. But eGaN FET have only 1 to 2 V VGS headroom from full turn-on to maximum allowable rating. This brings a challenge to the gate driver design, very careful PCB layout to minimize gate inductance is crucial to avoid damages caused by parasitic gate overshoot voltage. A secure high voltage clamp function should be provided to clamp the floating boot-strap power supply for high-side switch in a half-bridge driver configuration as in LM5113. However, due to the large charge or discharge current, using conventional voltage regulation method is not realistic, the methodology of voltage clamping at 5.5 V in LM5113 is not accessible to the commercial IP protection.

- Gate charges

All gate associated charges for eGaN FET's are significantly smaller than its comparable Si versions. So a current source gate driver may not be so applausive for GaN device considering extra time and losses for building up a non-zero current in a inductor.

- Input/output capacitance

The input capacitance is also much smaller, less than one third of similar Si MOSFET. From the design of a resonant gate driver viewpoint, this means we can have a much smaller resonant inductor for a large enough characteristic impedance. Most likely a PCB trace inductor is preferred, rather than a bulky and lossy discrete surface mounted inductor.

- Body diode

All vertical power MOSFET's has inherent source to drain body diode in parallel to the device channel. So both Si power MOSFET's in Table 3.1 have reverse recovery charges Q_{rr} during switching operations. However, for GaN

[1] BSZ035N03MS, V_{GS} = 4.5 V, I_D = 20 A.
[2] IRLH7134PbF, V_{GS} = 4.5 V, I_D = 40 A.
[3] EPX2015, V_{GS} = 5.0 V, I_D = 33 A

device there is no PN junction between source and drain, so the Q_{rr} is essentially zero. However, eGaN FET's has a much larger diode-like forward voltage drop from the source to the drain. This is mainly because the drain voltage is below the gate and source voltage such that the device is reversely conducted. Just because of the asymmetric gate-source and gate-drain structure, a higher "reverse threshold voltage" leads to a higher body diode forward voltage. This is important especially for high-side boot-strap powering in a half-bridge gate driver design, since the boot-strap capacitor might be over charged above the gate driver power supply voltage.

3.2 Operation Principles of the Proposed Resonant Gate Driver

The customized gate driver IC designed for resonant gate drive has been reported. Two typical resonant gate drivers are described here. A research team at microelectronics laboratory of University of South Carolina proposed a resonant gate driver IC designed for a depletion-mode GaN device fabricated at its own facility [57] [58] [59]. The gate driving topology is the "Resonate Gate Driver - Topology C" in section 2.3.3. The design process is 0.35 μm, 50 V high voltage H35B4 CMOS process [60] of Austriamicrosystems (AMS AG). The driver has maximum 50 mA output. The 1 mm width GaN HFET's built on sapphire has total input capacitance about 25 pF with 1 A current level and 100 V voltage rating. The PCB trace resonant inductor is about 20 nH. A switching frequency of 10 MHz was demonstrated for a load of a single GaN device test circuit. Another customized resonant gate driver using a 0.25 μm BiCMOS process is developed by Ampere laboratory at University of Lyon, France [61] [62] [63]. This gate driver is designed for an on-chip 3.6 – 2.2 V buck converter working at 200 MHz. The driver uses the topology described in "Resonate Gate Driver - Topology D" in section 2.3.4. The resonant inductor is a 400 × 400 μm^2 on-chip inductor with 8 nH inductance. The power transistors for the gate driver are the lateral-drain-extension MOSFET (LDEMOSFET) provided by the process working at 2.5 V V_{GS} and 3.6 V V_{DS} with size of 7 mm/0.25 μm. The estimated input capacitance is about 17 pF.

The gate driving requirements for the EPC GaN devices are quite different from the above published works. The input capacitance for the GaN device is

significantly larger. For example, the C_{ISS} for EPC2015 alone is almost 1000 pF, much larger than any of the applications above. The output peak current of LM 5113 is 1.2A/5 A source/sink current and almost 1.3/7.6 A for LM5114, which are the conventional gate drivers for EPC eGaN devices. For most conventional HV CMOS process, there is no such a large current rating on-chip inductors available. The solution proposed in [59] [60] [61] where area for the output transistors is almost doubled will not be favorable for EPC GaN devices. Additional large transistors in parallel turned on and off will at the gate significantly disturbs the gate capacitance and distort the gate signals.

3.2.1 Operation of Non-clamping Resonant Gate Driver

A simpler resonant gate driver is proposed without adding extra clamping or recovery diodes or transistors [64]. If the turning on and off timing could be precisely controlled, gate resonance will still be implemented and partial energy recovery can be realized. This resonant gate driver utilizes the parasitic gate inductance for resonant gate driving. The physical configuration from the load devices is the same as the conventional gate driver. The resonant gate driving is completely controlled by the sequence and pulse width of the control signals based on different resonant inductance and load capacitance values. It can be configured as resonant gate driver or conventional gate driver as practical operation conditions allowed.

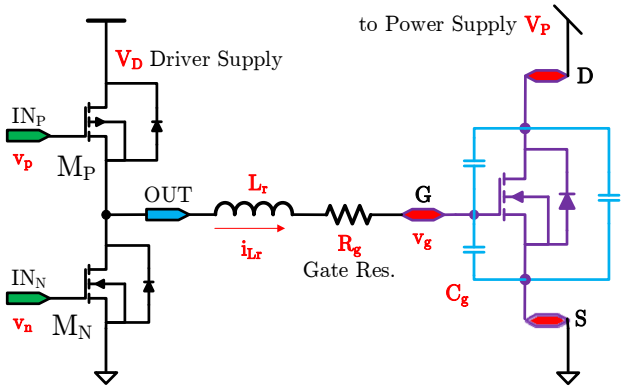


Figure 3.1. Proposed non-clamping resonant gate driver shared the same output structure as a conventional gate driver [62].

The proposed non-clamping resonant gate driver is shown in Figure 3.1. Figure 3.2 shows the simplified operating waveforms of four intervals for the charging and discharging process. The interval A - driver charging and interval B – body-diode charging completes a charging cycle. The interval C - gate discharging and interval D – body-diode recovery are for a discharging cycle.

Figure 3.3 shows the steady state waveforms of the proposed non-clamping resonant gate driver under resonant gate driving conditions. The four intervals are marked as A, B, C and D.

1) Interval A $(t_0 - t_1)$: V_D driver charging:

P-channel transistor M_P is turned on, the gate driver supply charges the power device's gate through the resonant loop $M_P - L_r - C_G$. The M_P is turned off the moment while the gate is charged almost half of the final value V_D. The energy provided by the driver supply is now split between the resonant inductor L_r and the gate capacitance C_G.

2) Interval B $(t_1 - t_2)$: M_N body diode charging:

Since the inductor current is still continuous, the rest of the current i_{Lr} will flow through the body diode of n-channel transistor M_N to finish the resonance, charging the gate voltage at the desired value of V_D. Since the transistor M_N is off, the gate capacitance voltage cannot resonate back to resonant inductor current since the reverse path is blocked.

3) Interval C $(t_3 - t_4)$: C_G gate discharging:

Similarly, as interval A, M_N being turned on for this interval, the gate potential is discharged to the half way where partial of the potential energy is transferred to inductor flux energy.

4) Interval D $(t_5 - t_6)$: M_P body diode recovery:

The current continues flowing back to the driver supply V_D. The resonance finishes when the gate capacitance C_G is completely discharged.

The timing between interval A and B, or C and D is adjusted based the actually loss of the circuit. For example, if the interval A is too short, the energy provided will not be able to charge the C_G to a desired value. If it is too long, the resonance will charge the C_G above the V_D, which might damage the device, or increases loss due to unnecessary ringing.

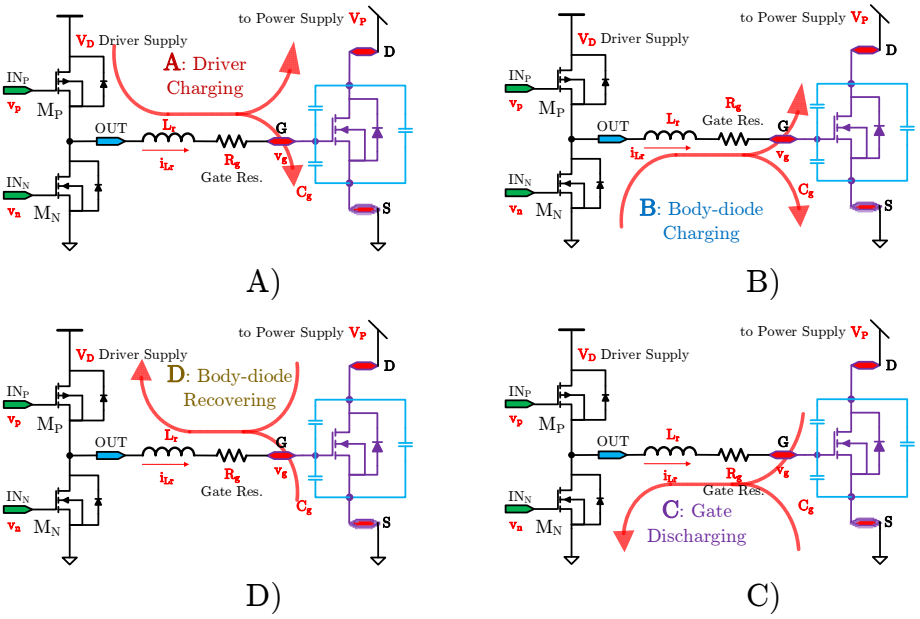


Figure 3.2. Four operation intervals for the proposed resonant gate driver, [from top-left clockwise:] A) driver charging, B) body-diode charging, C) gate discharging, D) body-diode recovery [62].

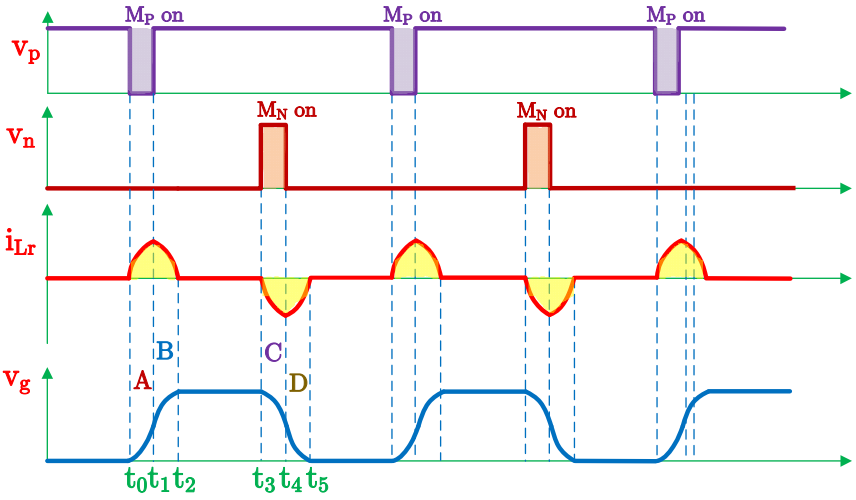


Figure 3.3. Simplified steady state waveforms of the proposed non-clamping resonant gate driver, the A, B, C and D shows the four operating intervals in Figure 3.2 [62].

3.2.2 Operation of MOSFET-clamped Resonant Gate Driver

Even though the proposed non-clamping resonant gate driver has the advantages of simple structures and controls, it has serious practical problems during application. The non-clamping (floating) gate voltages in the duration of on and off status could be distorted by any noise coupled from any components on switching converter board. Normally the noise caused by any parasitic effects on a PCB is hard to simulate and predict accurately even with any PCB level simulation softwares with 3D electro-magnetic (EM) field solvers. Comparing with other silicon power MOSFET's, the current GaN enhancement-mode HEMT's power devices are much more sensitive to gate noise. Table 3.1 shows that the GaN HEMT is especially sensitive to the positive gate voltage. To ensure a proper operation of the GaN devices under resonant gate driving condition, a MOSFET-clamped resonant gate driver is designed to eliminate the possible false turn-on or turn-off due to the coupled gate noise on board. Figure 3.4 shows the schematic diagram of the proposed MOSFET-clamped resonant gate driver.

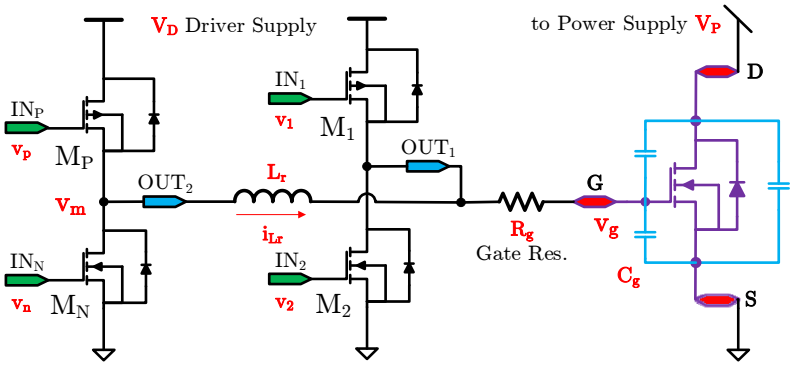


Figure 3.4. Proposed MOSFET-clamped resonant gate driver.

The hardware implementation is the same as the resonant gate driver – topology D in section 2.3.4. However, the control signal scheme is different. There is no pre-charge or pre-discharge interval where the inductor current is built up. The control sequences in topology D of section 2.3.4 are too complex for high frequency switching application. The current source gate driver is less favorable for GaN HEMT's used in low power conversions since the gate input capacitance and gate threshold voltage is smaller than other types of Si power

MOSFET's devices. Figure 3.6 shows the steady state waveforms of the proposed MOSFET-clamped resonant gate driver. The four intervals are marked as A, B, C and D in the figure.

1) Interval A $(t_0 - t_1)$: V_D driver charging:

P-channel transistor M_P is turned on, the gate driver supply charges the power device's gate through the resonant loop $M_P - L_r - C_G$. Unlike the non-clamping version, the gate voltage is completely charged to the final value during this interval. If the turn-on time of the MP is a little bit larger than the quarter resonant period, there will be s small period of free-wheeling conducting through the loop of $M_P - L_r - BDM_1$.

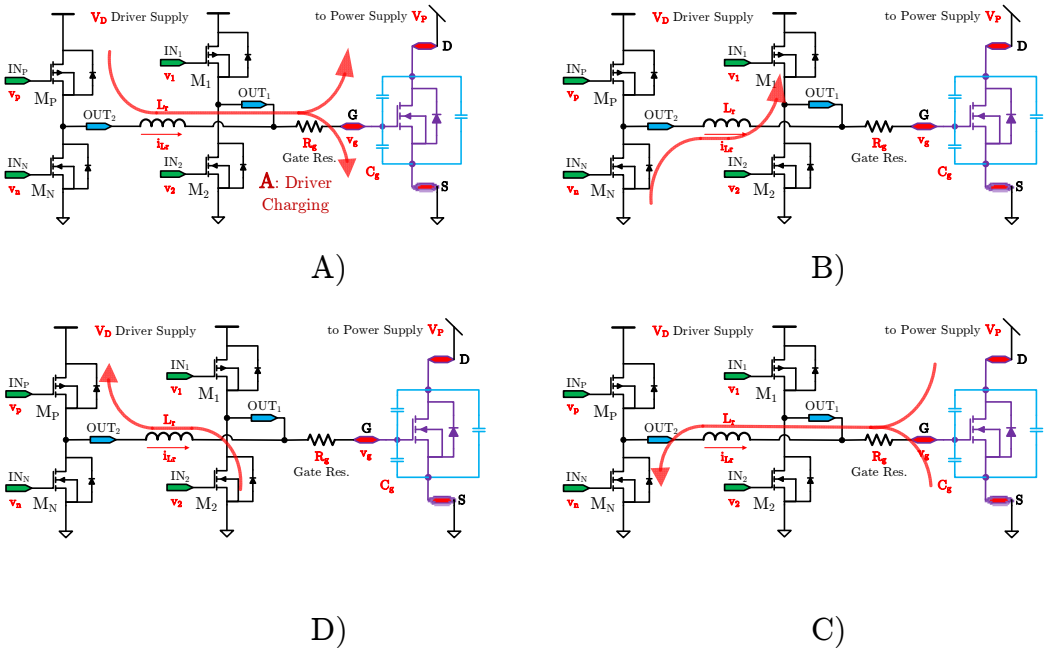


Figure 3.5. Four operation intervals for the proposed MOSFET-clamped resonant gate driver, [from top-left clockwise:] A) driver charging, B) charging recovery, C) gate discharging, D) discharging recovery.

2) Interval B $(t_1 - t_2)$: M_1 charging recovery:

The M_1 is turned on right after the M_P turned off. The rest inductor current will feed back to the driver supply via the path of $BDM_N - L_r - M_1$.

3) Interval C $(t_3 - t_4)$: C_G gate discharging:

Similarly, as interval A, M_N being turned on for this interval, the gate potential is discharged completely to ground. There can be a short period of free-wheeling conduction via the loop of $BDM_2 - L_r - M_N$.

4) Interval $D\,(t_5 - t_6)$: M_2 discharging recovery:

The M_2 is turned on right after the M_N turned off. The rest inductor current will feed back to the driver supply via the path of $BDM_P - L_r - M_2$.

3.3 Loss Analysis of the Proposed Resonant Gate Driver

A complete analytical expression on the gate driver loss is almost impossible. To simplify the loss analysis, we need to make the following assumptions.

1) A steady-state waveform is the same as the ideal lossless state waveform.
2) The only loss is the charging/discharging loss.
3) All loss can be expressed from the ideal current flow through an equivalent lumped resistance R_G, the characteristic impedance $Z_0 >> R_G$.
4) The charging or the discharging process is completely symmetrical.

In Figure 3.7 shows the inductor current i_{Lr} and gate-source voltage v_{GS} of the resonant gate driver topology C [38] [55], D [40] and the proposed non-clamping gate driving topology [62] and MOSFET-clamped resonant topology during the charging period.

3.3.1 Loss Analysis of Diode-clamped Resonant Gate Drive

In Figure 3.7 (A), the diode-clamped version of resonant gate driver, the current waveform can be split into a quarter sine waveform from t_0 - t_1 for resonant charging segment and linear inductor current feeding segment from t_1 - t_2. For the resonant charging period, we have the following equation.

$$v_{GS}(t) = \frac{1}{C_G}\int_{t0}^{t1} i_{Lr}(t)dt = V_D - R_G i_{Lr}(t) - L_r \frac{di_{Lr}(t)}{dt} \tag{3.1}$$

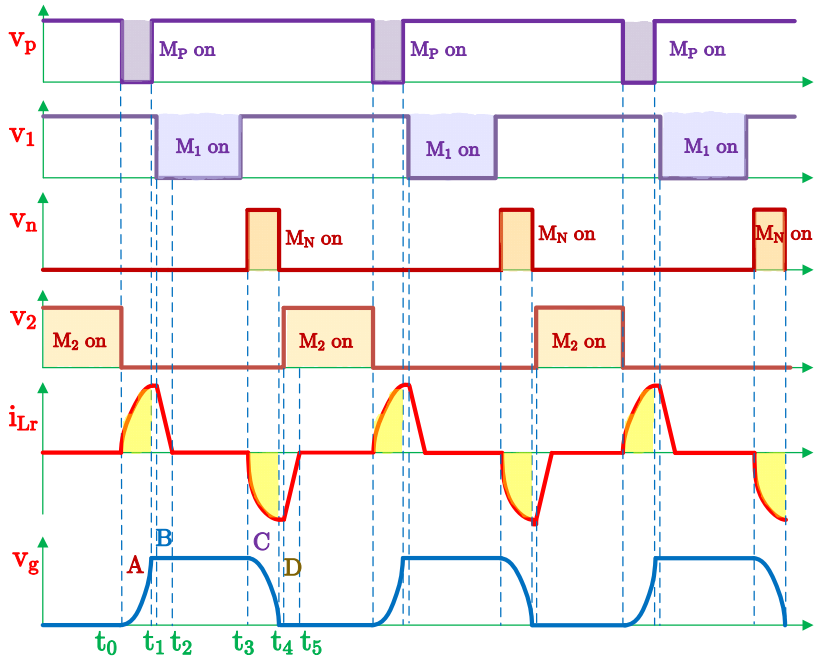


Figure 3.6. Simplified steady state waveforms of the proposed MOSFET-clamped resonant gate driver, the A, B, C and D shows the four operating intervals in Figure 3.5.

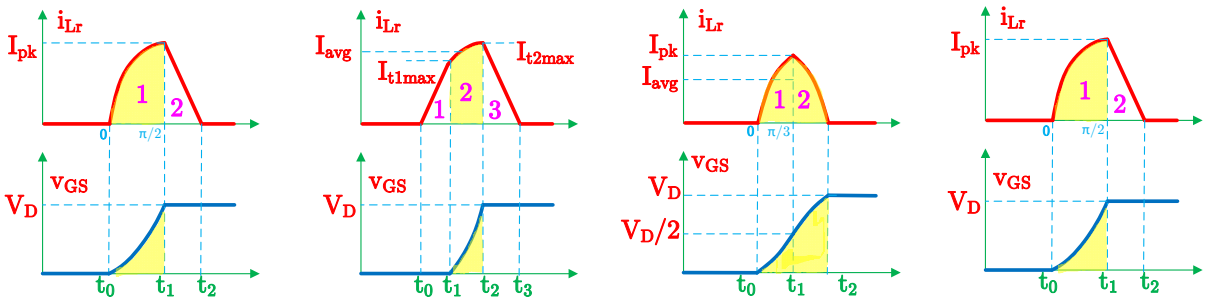


Figure 3.7. Simplified charging steady state inductor current and gate voltage waveforms of three resonant gate drivers, [from left:] (A) topology C [38] [55], (B) topology D [40], (C) proposed non-clamping topology [62] and (D) proposed MOSFET-clamped topology.

Differentiate over time, we can have a standard second-order differential equation. Solve equation based on the assumption 3), we have result in (3.2) and (3.3) [58].

$$i_{Lr}(t) = e^{-\frac{R_G}{2L_r}t}\left[A \cdot cos\theta t + B \cdot sin\theta t\right] \tag{3.2}$$

$$\theta = \frac{\sqrt{\frac{4L_r}{C_G} - {R_G}^2}}{2L_r} \tag{3.3}$$

Based on initial condition, coefficient A is zero. Coefficient B can be quickly expressed as the resonant current magnitude of a lossless series LC network.

$$I_{pk} = \frac{V_D}{Z_0} = \frac{V_D}{\sqrt{\frac{L_r}{C_G}}} \tag{3.4}$$

The inductor current for the resonant segment can be expressed as [58]

$$i_{Lr}(t) \approx \frac{V_D}{\sqrt{\frac{L_r}{C_g}}} e^{-\frac{R_G}{2L_r}t} sin \frac{\sqrt{\frac{4L_r}{C_g} - {R_G}^2}}{2L_r} t \tag{3.5}$$

Furthermore, simplify the sine term with the assumption the characteristic impedance is much larger than the gate resistance and neglecting the exponential decay

$$i_{Lr}(t) \approx \frac{V_D}{\sqrt{\frac{L_r}{C_G}}} sin\sqrt{\frac{1}{L_r C_G}} t \tag{3.6}$$

The energy loss during the charging segment can be expressed as an integral of a quarter sine wave ($0 - \pi/2$ radian angel), which leads to

$$E_{t0\text{-}t1} = \int_{t0}^{t1} {i_{Lr}}^2(t) R_G dt = \frac{\pi {V_D}^2 R_G C_G}{4Z_0} \tag{3.5}$$

For the linear current recovery segment, the time period is

$$\Delta t = t_2 - t_1 = L_r \frac{I_{pk}}{V_D} = \frac{L_r}{Z_0} \tag{3.6}$$

Since the current during recovery is linear, the current waveform in this segment can be treated as a triangle. The energy loss in this segment can be shown as

$$E_{t1\text{-}t2} = \frac{1}{3}\left(I_{pk}\right)^2 R_G \Delta t = \frac{1}{3}\left(\frac{V_D}{Z_0}\right)^2 R_G \frac{L_r}{Z_0} = \frac{{V_D}^2 R_G L_r}{3{Z_0}^3} \tag{3.7}$$

The total energy loss from $t_0 - t_1$ can be expressed as the sum of (3.5) and (3.6) [58]

$$E_{t0\text{-}t2} = \frac{\pi {V_D}^2 R_G C_g}{4Z_0} + \frac{{V_D}^2 R_G L_r}{3{Z_0}^3} = \frac{{V_D}^2 R_G C_G}{Z_0}\left(\frac{\pi}{4} + \frac{1}{3}\right) \tag{3.8}$$

The total energy loss is the sum of the charging and discharging process, with reverse current waveforms but the same amplitude. The result times the switching frequency f_{sw} is the total power loss for the resonant gate driver topology C in Figure 3.4 (A).

$$P_{total} = \frac{2{V_D}^2 R_G C_g f_{sw}}{Z_0}\left(\frac{\pi}{4} + \frac{1}{3}\right) \approx 2.24 \frac{{V_D}^2 R_G C_g f_{sw}}{Z_0} \tag{3.9}$$

3.3.2 Loss Analysis of MOSFET-clamped Current Source Resonant Gate Drive

In Figure 3.7 (B), the transistors' clamped version of resonant gate driver, from $t_1 - t_2$ segment the current waveform is a resonant segment with non-zero initial current and voltage. It will be very complicated to write down a differential equation to solve this problem. A simple way is to approximate the current of this segment as a linear current growth. So the whole charging period can be divided into three segments: pre-charging segment t_0 - t_1, charging segment t_1 - t_2 and recovery segment t_2 - t_3.

If the average current and current ripple in the segment t_1 - t_2 can be

determined, the exact current values at t_1 and t_2 will be available. The average current can be approximated as the gate charges over charge time t_{12}.

$$I_{avg} = \frac{Q_G}{t_{12}} = \frac{C_G V_D}{t_{12}} \tag{3.10}$$

The current ripple can be obtained if we assume the equivalent voltage across the inductor is the middle point of the voltage swing, which is the $V_D/2$.

$$\Delta i_{12} = \frac{V_D t_{12}}{2L_r} \tag{3.11}$$

Then the current at t_1 and t_2 can be expressed as

$$i_{t1} = I_{avg} - \frac{\Delta i_{12}}{2} = \frac{C_G V_D}{t_{12}} - \frac{V_D t_{12}}{4L_r} \tag{3.12}$$

$$i_{t2} = I_{avg} + \frac{\Delta i_{12}}{2} = \frac{C_G V_D}{t_{12}} + \frac{V_D t_{12}}{4L_r} \tag{3.13}$$

The time intervals of t_0 - t_1 and t_2 - t_3 can be approximated in the same way as in equation (3.6).

$$\Delta t_{01} = t_1 - t_0 = L_r \frac{i_{t1}}{V_D} = \frac{L_r}{V_D}\left(\frac{C_G V_D}{t_{12}} - \frac{V_D t_{12}}{4L_r}\right) \tag{3.14}$$

$$\Delta t_{23} = t_3 - t_2 = L_r \frac{i_{t2}}{V_D} = \frac{L_r}{V_D}\left(\frac{C_G V_D}{t_{12}} + \frac{V_D t_{12}}{4L_r}\right) \tag{3.15}$$

Then energy dissipated during time intervals of t_0 - t_1 and t_2 - t_3 segments can be expressed as below.

$$E_{t0\text{-}t1} = \frac{1}{3}(i_{t1})^2 R_G \Delta t_{01} = \frac{1}{3} R_G \frac{L_r}{V_D}\left(\frac{C_G V_D}{t_{12}} - \frac{V_D t_{12}}{4L_r}\right)^3 \tag{3.16}$$

$$E_{t2\text{-}t3} = \frac{1}{3}\left(i_{t2}\right)^2 R_G \Delta t_{23} = \frac{1}{3} R_G \frac{L_r}{V_D}\left(\frac{C_G V_D}{t_{12}} + \frac{V_D t_{12}}{4L_r}\right)^3 \tag{3.17}$$

For the interval of t_1 - t_2, the wave form can be treated as a superposition of an average DC value with a triangle wave. The average DC value I_{avg} is orthogonal to the triangle wave with 0 average, then total mean-square value can be obtained by simply adding mean-square value of each component.

$$E_{t1\text{-}t2} = \left[{I_{avg}}^2 + \frac{1}{3}\left(\Delta i_{12}\right)^2 \right] R_G t_{12} = \left[\left(\frac{C_G V_D}{t_{12}}\right)^2 + \frac{1}{3}\left(\frac{V_D t_{12}}{2L_r}\right)^2 \right] R_G t_{12} \tag{3.18}$$

The total energy loss is the two times of the sum of (3.16) (3.17) and (3.18) process.

$$E_{total} = 2\left(E_{t0\text{-}t1} + E_{t1\text{-}t2} + E_{t2\text{-}t3}\right) \tag{3.19}$$

The power energy loss is the product of the switching frequency f_{sw} and equation (3.19).

$$\begin{aligned} P_{total} &= E_{total} f_{sw} \\ &= 2R_G {V_D}^2 f_{sw} \left\{ \frac{1}{3} L_r \left[\left(\frac{C_G}{t_{12}} - \frac{t_{12}}{4L_r}\right)^3 + \left(\frac{C_G}{t_{12}} + \frac{t_{12}}{4L_r}\right)^3 \right] + t_{12} \left[\left(\frac{C_G}{t_{12}}\right)^2 + \frac{1}{12}\left(\frac{t_{12}}{L_r}\right)^2 \right] \right\} \end{aligned} \tag{3.20}$$

3.3.3 Loss Analysis of Non-clamping Resonant Gate Drive

The proposed resonant gate driver without clamping devices is shown in Figure 3.7 (C). The whole charging process can be divided in two segments. In the time interval t_0 - t_1 the LC resonant tank consisted of L_r and C_G is charged through M_P by V_D. During interval t_0 - t_1 the same LC tank resonates without voltage source connected. Since the time constant of the circuit is the same, for simplicity we assume between these two intervals the gate of the power device is charged to $V_D/2$, the half way to the final value V_D.

Since the resonant condition is the same as in Figure 3.4 (A), the current expression is essentially the same. The energy loss during the driver charging segment t_0 - t_1 can be expressed as an integral of a quarter sine wave ($0 - \pi/3$ radian angel),

$$E_{t0\text{-}t1} = \int_{t0}^{t1} i_{Lr}{}^2(t) R_G dt = \left(\frac{\pi}{6} - \frac{\sqrt{3}}{8} \right) \frac{V_D{}^2 R_G C_G}{Z_0} \tag{3.21}$$

The current waveform for the body-diode charging during the interval $t_1 - t_2$ is symmetric to the interval t_0 - t_1. So the total energy loss during the charging period is

$$E_{t0\text{-}t2} = 2E_{t0\text{-}t1} = \left(\frac{\pi}{3} - \frac{\sqrt{3}}{4} \right) \frac{V_D{}^2 R_G C_G}{Z_0} \tag{3.22}$$

Similarly, the discharging process is also symmetric, so the total power loss for the proposed resonant gate driver in Figure 3.4 (C) is

$$P_{total} = \left(\frac{2\pi}{3} - \frac{\sqrt{3}}{2} \right) \frac{V_D{}^2 R_G C_g f_{sw}}{Z_0} \approx 1.23 \frac{V_D{}^2 R_G C_g f_{sw}}{Z_0} \tag{3.23}$$

Comparing to the loss in (3.9), the power loss in (3.23) only has a smaller coefficient. This is due to a smaller charging current in a partial quarter sine inductor waveform in Figure 3.7 (C) compared to a full quarter current sine inductor waveform Figure 3.7 (B). However, since in the proposed resonant gate driver, half of the gate driving is conducted by body-diode, we can expect the effective R_G in Figure 3.7 (C) is larger than in Figure 3.7 (A). But both cases should have a similar gate driver power saving profile.

3.3.4 Loss Analysis of MOSFET-clamped Resonant Gate Drive

The current waveform of Figure 3.7 (A) and (D) are essentially the same. The only difference is the charge recovery process which in case (A) the inductor feeding current is via clamping diodes but in case (D) is through the clamping MOSFET's. The power loss equation is the same as in equation (3.9) since the

power loss is calculated based on the equivalent rms current value multiplied by the equivalent gate resistance R_G.

$$P_{total} = \frac{2V_D{}^2 R_G C_G f_{sw}}{Z_0}\left(\frac{\pi}{4}+\frac{1}{3}\right) \approx 2.24\frac{V_D{}^2 R_G C_G f_{sw}}{Z_0} \tag{3.24}$$

Even though the operating principle is the same, there is an important benefit of charge recovery using MOSFET's over diodes or body diodes charge recovery. Since all diodes have a reverse recovery current after forwarding current drops off, the charging or discharge voltage must somewhat have an overshoot or undershoot to provides charges for reverse current. This overshoot or undershoot is observed in the simulations of type (A) and (C) in Figure 3.7.

3.4 Design of the Low-Side Resonant Gate Driver

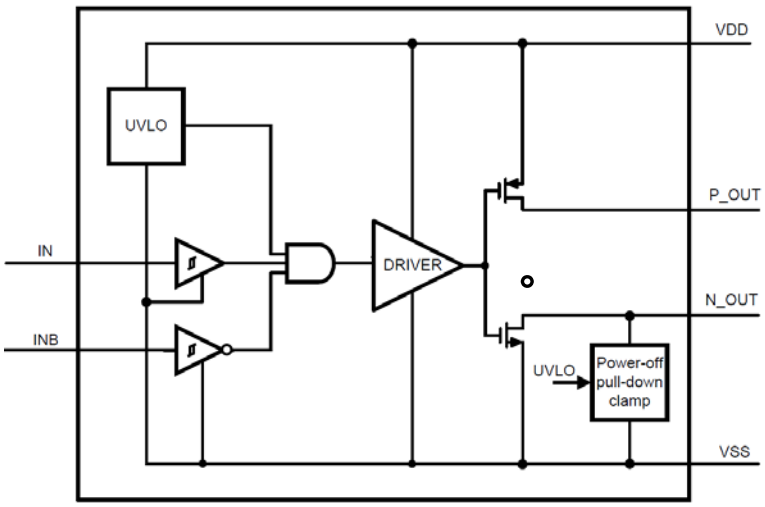


Figure 3.8. Block diagram of the low-side conventional gate driver LM5114 [26].

LM5114 is a low-side gate driver formally designed by National Semiconductor and recommended by EPC. It is specifically designed for EPC eGaN ® devices. Figure 3.8 is the block diagram of LM5114 [26]. One obvious character is that the LM5114 N_{OUT} has a pull-down clamp in parallel. This

circuit is actually a NPN BJT transistor which can turn on at less than 1 V to pull down the power device. LM5114 provides an option of non-inverting or inverting signal input, which also behaves as an enable pin while not used as PWM signal input. However, since this is essentially a conventional gate driver with totem-pole structure output, only one input is necessary to drive to circuit. This is also the reason why the LM5114 cannot be used for resonant gate driving. If we want to implement resonant gate driving for GaN HEMT's devices, a new gate driver must be designed.

3.4.1 Design of the Low-Side Non-Clamping Gate Driver

Based on the signal diagram in Figure 3.3, where the turn-on or turn-off control of the power switch is independent of each other, the proposed resonant gate driver should have two paths of completely separated control signals. The truth table of the proposed resonant gate driver is shown in Table 3.2. Unlike a conventional gate driver, both inputs have no signal, the output should be at floating status. At this moment, the resonance is implemented at the gate with the power device input capacitance and added resonant inductor.

Table 3.2: Truth table of the proposed non-clamping resonant gate driver.

IN_{ON}	IN_{OFF}	P_{OUT}	N_{OUT}
L	L	OPEN	OPEN
L	H	OPEN	L
H	L	H	OPEN
H	H	OPEN	L

Figure 3.9 shows the block diagram of the proposed low-side resonant gate driver to realize the driving logic functions in Table 3.2. The conventional one PWM signal should be split into two signals, IN_{ON} and IN_{OFF}, for the proposed resonant gate driver, each signal can control the turn-on or turn-off timing and width. As mentioned above, the output is pulled down when both IN_{ON} and IN_{OFF} inputs are high. This design is to ensure the power device is turned off when the control signals conflict with each other. Another case happens when both IN_{ON} and IN_{OFF} inputs are low. Due to the requirements of the proposed resonant gate driver, both output pins are floating at this moment. The input

IN_{ON} and IN_{OFF} first pass through a Schmitt trigger with designed hysteresis to overcome the noises at the inputs. Then a two-input NAND gate following the Schmitt trigger outputs is added in a case of abnormal input conditions where two inputs are both high. Each turn-on or turn-off signal is finally controlled by an output of the under-voltage lock-out circuit (UVLO). When the voltage supply of the gate driver drops to a designed low level, the output of UVLO will shut down the gate driver output by turning on N_{OUT} and turning off P_{OUT}, pulling of the power switch gate. The output PMOS and NMOS driving transistors are connected to the driver supply VDD. The output has separate P_{OUT} for pulling up and N_{OUT} for pulling down. The enable pin ENA is defined such that when it is low, the output will be P_{OUT} for open and N_{OUT} pulled down to shut off the power switches.

The proposed resonant gate driver is designed with a commercially available high voltage (HV) CMOS process. This process provides variety of 1.8 V, 5 V, 20 V and 50 V FET's and other active and passive devices. In this design the driver circuit core is designed with 5.5 V oxide FET's to meet the requirement of maximum 5.5 V gate-source voltage of GaN HEMT's. For the high-side circuit in the proposed half-bridge gate driver, high voltage isolated devices are used. Some other devices such as isolated Schottky diodes, resistors and capacitors are also used. However, this HV CMOS process does not have an on-chip inductor suitable for power applications. The inductor diameter is limited to the range of 100 to 400 μm. The supported metal line is limited up to 25 μm. The current limit and inductor values cannot meet the required resonant inductor. The resonant inductor must be provided off chip either with a discrete surface mount inductor or the parasitic stray inductance of a PCB wire.

Schmitt trigger is the first block on the signal path. It will filter out the noises and reconstruct the signal. The noise filtering is implemented with the hysteresis design of the Schmitt trigger. Figure 3.10 shows the schematic of the designed Schmitt trigger, where the sizing of M_{N1} and M_{N2} determines the lower triggering voltage and the sizing of M_{P1} and M_{P2} determines the upper triggering point. Figure 3.11 shows the simulation
of the Schmitt trigger in Figure 3.10. The post-layout simulation is also carried with the Caliber 3D extracted "xACT 3D" suing complete L and C options [65]. The simulation confirms the desired switching points of 3.7 V and 1.4 V matches the design specifications. It also shows the layout style is in consistent with the schematic plan.

An under-voltage lockout circuit (UVLO) is present in most gate driver circuit especially in battery powered applications to ensure proper working

conditions for the power switches. As long as the power supply is not sufficient to make the device work properly, the gate driver will turn of the switching signals. Figure 3.12 shows the schematic diagram of the proposed UVLO. From the left to the right, the UVLO is composed of a start-up circuit, a beta multiplier reference circuit (BMR) [66], a differential amplifier with one input feeding with a resistive divider, a comparator with positive feedback and an output differential amplifier. The start-up circuit will quickly push the circuit into the desired quiescent conditions whenever the power supply is added. A BMR circuit is used to create a stable reference voltage for the current mirrors needed for a voltage reference, amplifier and comparator. A resistive voltage divider is to provide a ratioed power supply voltage for one of the input of the following differential amplifier. The differential output of the differential amplifier is feeding into a positive feed-back comparator with hysteresis applied. This hysteresis control is different from the conventional feedback based hysteresis control in UVLO. The purpose of choosing this design is to minimize the transition delay. The output of the comparator is two-path rail-to-rail differential signal. This signal is feeding into the output differential amplifier with its single-ended output driving an output inverter. The final output will either following the power supply or being pulled down to ground.

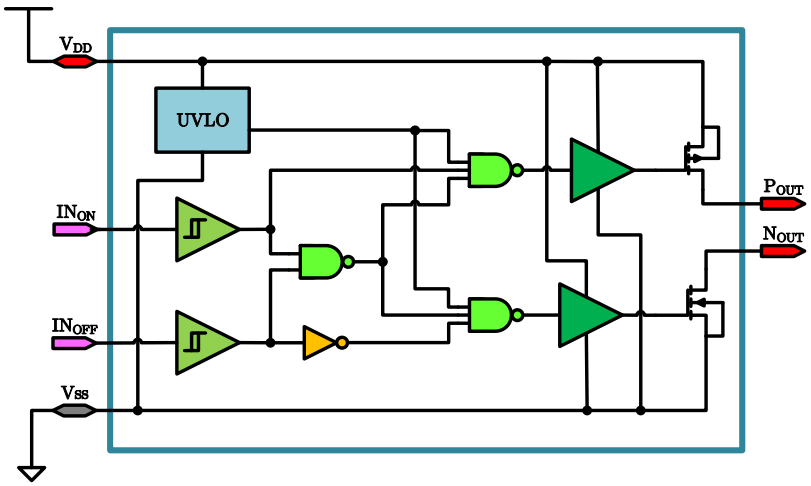


Figure 3.9. Block diagram of the proposed non-clamping low-side resonant gate driver.

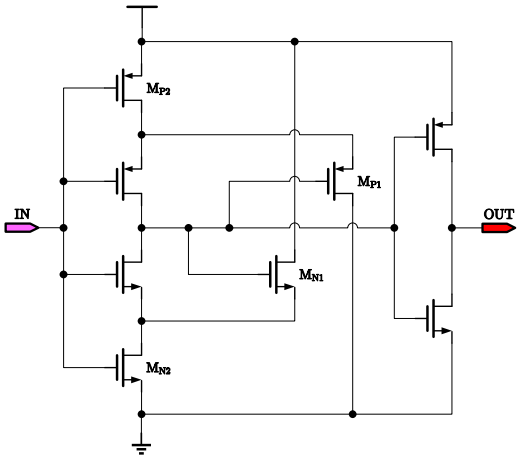


Figure 3.10. Schematic diagram of the input Schmitt trigger.

As for EPC GaN devices, the R_{DSON} will increase significantly if the gate driving voltage continuously dropping below 4 V. So the UVLO was designed with hysteresis of V_{LH} = 4.5 V and V_{HL} = 3.7 V. The hysteresis is realized by the comparator mentioned above with specified transistor sizing. Figure 3.13 shows the UVLO simulation results. The power supply V_{DD} changes from 0 V to 5.5 V and drops back to 0 V. UVLO output follows the V_{DD} when it rises to the level at V_{LH} = 4.41 V and pull down to ground again when the V_{DD} drops to the level at $V_{H}L$ = 3.60 V when V_{DD} drops. The output transition time is less than 30 ns, which is less than one period of 100 ns for 10 MHz switching. So the UVLO will take effects in one switching cycle, avoiding possible damages working with an under-voltage supply. This UVLO should meet the requirement of the proposed resonant gate driver working at high speed conditions.

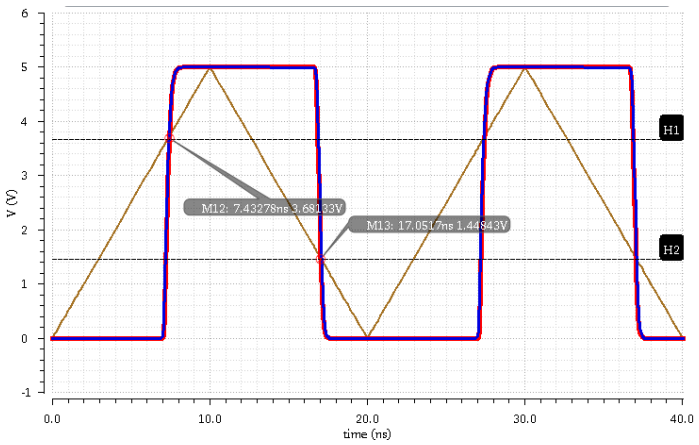


Figure 3.11. Cadence Spectre simulation of the Virtuosos schematic (in blue) and the Calibre xACT 3D extracted layout (in red).

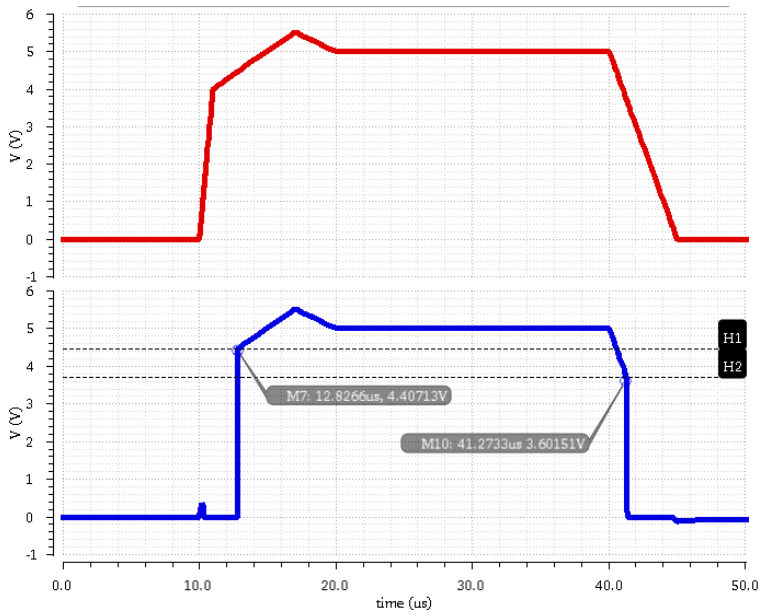


Figure 3.13. Cadence Spectre simulation of the proposed UVLO in Figure 3.7, [from top:] the V_{DD} input voltage; the UVLO output voltage.

3.4.2 Design of the Low-Side MOSFET-clamped Gate Driver

Referring to the schematic and operational diagram in Figure 3.14 and Figure 3.15, the gate driver truth table is shown in Table 3.3. For the MOSFET-clamped resonant gate driver, since it has two set of output, we need to define two truth tables for each set of output and inputs. Only the pin OUT_2 is split into P_{OUT} and N_{OUT} since this node is on the main charging or discharging path. The first truth table is similar to the non-clamping one, with the exception for C_{OUT}. When both IN_{ON} and IN_{OFF} are at the H level, the C_{OUT} is set to L, such as clamp the output to the device gate terminal to ground.

The second truth table is to determine the functions of the second output pin C_{OUT} (OUT_1 in Figure 3.4) during transitions. This output is triggered by the rising and falling edges of the control signals. When IN_{ON} changes from H to L while IN_{OFF} is L, this is the start of charging recovery as shown in Figure 3.5 (B). When IN_{OFF} changes from H to L while IN_{ON} is L, this is the start of discharging recovery as shown in Figure 3.5 (D). The driver charging process as shown in Figure 3.5 (A) startes as IN_{ON} changes from L to H when IN_{OFF} is L, while the discharging process starts as IN_{OFF} changes from L to H when IN_{ON} keeps at L. The timing for these three output pins should be carefully observed

to obtain the desired clamping without impact on the resonant process.

Figure 3.14 shows the block diagram of the MOSFET-clamped low-side gate driver. The logic function of the IN_{ON}/IN_{OFF} to P_{OUT}/N_{OUT} and C_{OUT} is designed to implement the truth table in Table 3.3. Unlike the non-clamping resonant gate driver, where the gate of the power switch will be floating after the desired resonant process finished, the clamping node output, C_{OUT}, is either shorted to ground or power supply based on the different control sequences.

The control block diagram for the IN_{ON}/IN_{OFF} to C_{OUT} can be explained with the steady state waveforms in Figure 3.6. A negative edge IN_{ON} and a low level of IN_{OFF} is to provide a turn-on duration of M_1 in Figure 3.4. A negative edge IN_{OFF} and a low level of IN_{ON} is to provides a turn-on duration of M_2. If both turn-on and turn-off signals happens due to some malfunctions of the input signals or circuitry, the output will turn off the power device to protect it. The enable pin ENA and internal UVLO control the output in the same way as the non-clamping version in Figure 3.9.

As shown in Figure 3.4, the middle point of transistors M_P and M_N is supposed to experience a large voltage swing (even higher than rail-to-rail swing) during the transition from the charging/discharging to the recovery intervals.

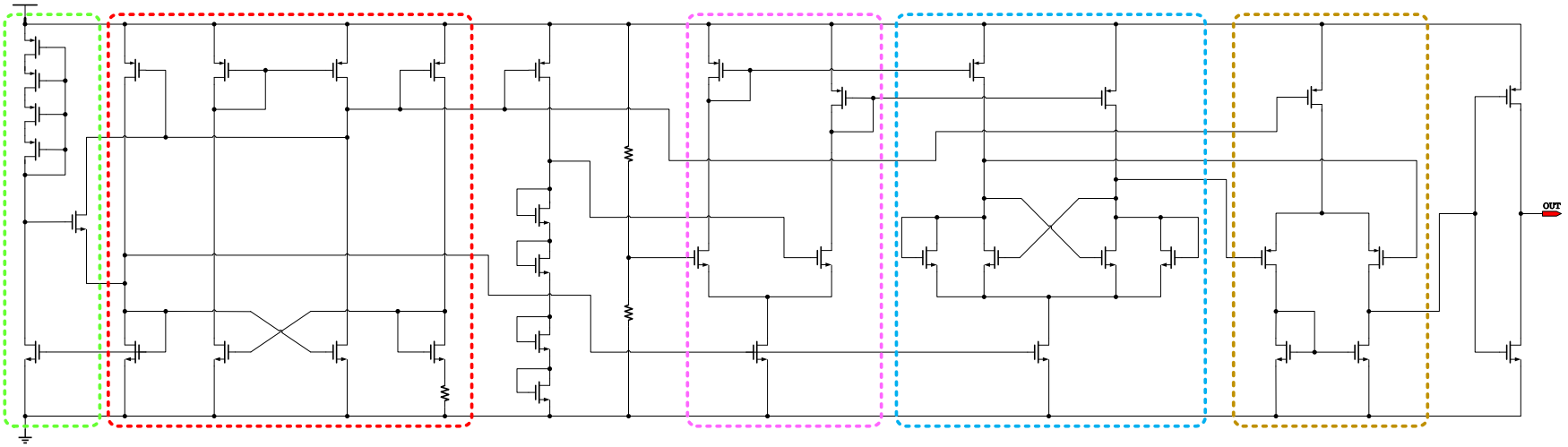


Figure 3.12. Schematic diagram of the proposed UVLO circuit, [circled area from left:] start-up circuit, BMR, differential-ended differential amplifier, comparator, single-ended differential amplifier.

To minimize the potential coupling to the gates of M_P and M_N, two methods can be employed. The first is to have a parallel diode across drain and source of M_P and M_N such that the recovery current will not flows through the body diodes. The second method is to increase the sizing of M_P and M_N to have a larger parasitic body diode. Figure 3.14 shows the drivers chain in orange for M_P and M_N and in yellow for M_1 and M_2. The former chain is a six-stage inverters and the latter four stages.

Table 3.3: Truth tables of the proposed MOSFET-clamped resonant gate driver.

IN_P	IN_N	P_{OUT}	N_{OUT}	C_{OUT}
L	L	OPEN	OPEN	TBD
L	H	OPEN	L	OPEN
H	L	H	OPEN	OPEN
H	H	OPEN	L	L

IN_P	IN_N	C_{OUT}
H → L	L	H
L	H → L	L
L → H	L	OPEN
L	L → H	OPEN

Cadence Ultrasim simulator [67] rather than conventional Spectre simulator is used to simulate the large signal power switching. The simulation mode is "Spice (S)" and speed mode is "Extreme Accuracy (1)". Under this configuration, the Ultrasim avoids converge problems occurred during most switching simulations with only 2 or 3% errors. Figure 3.15 shows the Cadence Ultrasim simulation results for the control outputs of the proposed MOSFET-clamped resonant gate driver switching at 10 MHz with 50% duty cycle. The circuit configuration is the same as in the topology (g) in Table 3.4. The resonant inductor is chosen as 20 nH. The signal inputs in the same as the non-clamping gate driver. The outputs are four strictly timing correlated channels to drive transistors M_N, M_P, M_1 and M_2 in Figure 3.4. For example, when M_N is turned on by a rising gate signal V_N, the M_1 must be quickly turned off by ramping the V_1 to 5 V. When the gate voltage of M_P, V_P, dropped to 0 V, the V_2 must be

turned off as soon as possible. The simulation at room temperature with typical process corner models shows a transition delay of these two cases of only 0.1 ns.

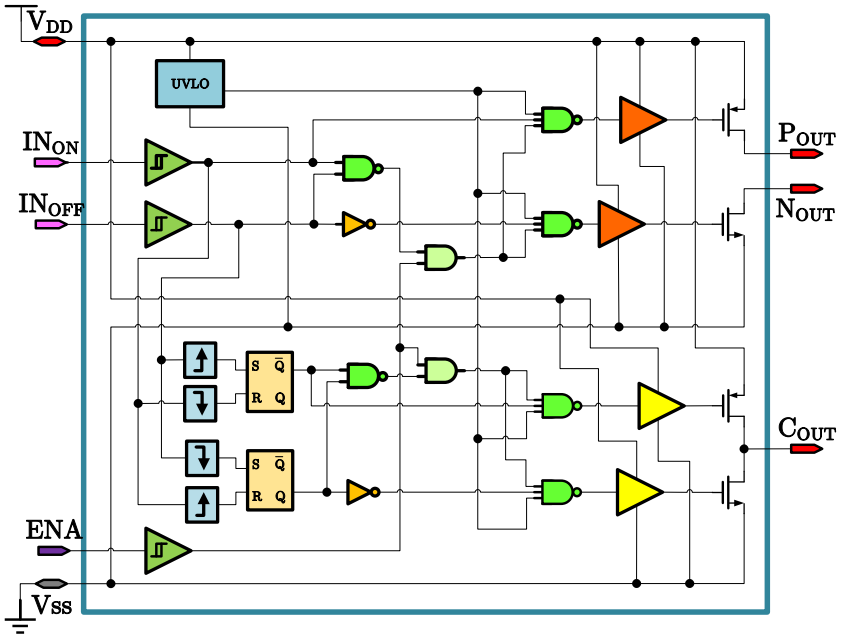


Figure 3.14. Block diagram of the proposed MOSFET-clamped low-side resonant gate driver.

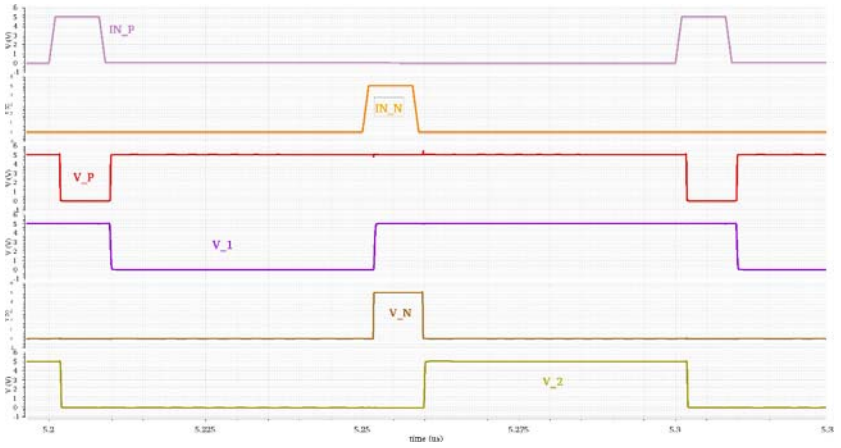


Figure 3.15. Cadence Ultrasim simulation results for the voltage control outputs of the proposed MOSFET-clamped resonant gate driver (in Figure 3.4) working a4 10 MHz with 20 nH resonant inductor (type (g) in Table 3.4), [from top:] *IN_P* and *IN_N*, control inputs; *V_P*, gate voltage of M_P; *V_1*, gate voltage of M_1; *V_N*, gate voltage of M_N; *V_2*, gate voltage of M_2.

Simulations at different temperatures and process corners also prove the effectiveness of the proposed design. Figure 3.16 shows the transition of V_N rising edge to V_1 rising edge and V_P falling edge to V_2 falling edge at 25 ° C and 125 ° C. At 125 ° C, the maximum transition delay is still less than 0.16 ns. Figure 3.17 is the same simulation result at 50 ° C using two extreme conditions: the fast NMOS slow PMOS model (fs) and the slow NMOS and fast PMOS (sf). The delay increase caused by the process corner is about 0.14 ns, even smaller than the one due to the temperature increases.

3.5 Simulation Results

To verify the effectiveness of driving power saving for the proposed resonant gate drivers compared with other existing topologies, a simple test circuit is used for the simulations. Figure 3.18 shows the simplified test circuit schematic diagram. For resonant gate drivers, a modified version with main charging PMOS and discharging NMOS FET's having a PN diodes in parallel to bypass their source–drain body diodes are also included for comparison. The green-line enclosed amplifier symbol represents each gate drivers for the following:

(a) conventional gate driver (Figure 2.5),
(b) diode-clamped resonant gate driver (Figure 2.13),
(c) diode-clamped resonant gate driver (Figure 2.13) with body diodes bypassing,
(d) non-clamping resonant gate driver (Figure 3.1),
(e) non-clamping resonant gate driver (Figure 3.1) with body diodes bypassing,
(f) MOSFET-clamped resonant gate driver (Figure 3.4),
(g) MOSFET-clamped resonant gate driver (Figure 3.4) with body diodes bypassing.

Figure 3.19 shows the schematic diagram of the resonant gate driver type (c) and (g) mentioned above. Other types of gate drivers have less components as in these two topologies. The resonant inductor has equivalent series resistance (ESR) of 10 mΩ. Table 3.4 lists the component values used for simulations. The control signal is from an ideal voltage pulse source with 5 mΩ ESR, 5 V amplitude and 1 ns rising/falling edges. The driving pulse width for signal IN_N

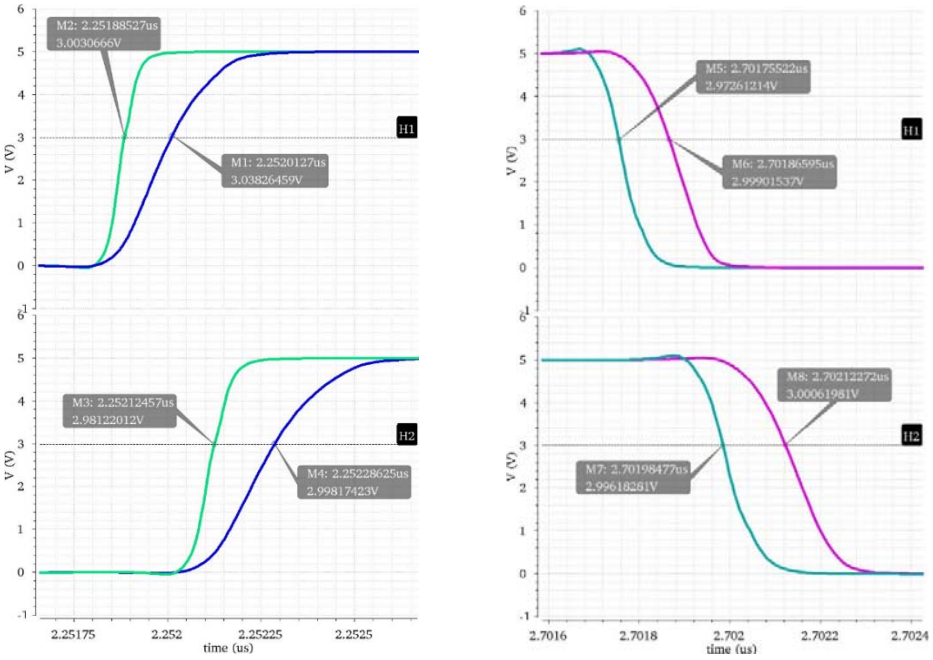


Figure 3.16. Cadence Ultrasim simulation results for the transition delay at 25 ° C (top) and 125 ° C (bottom), [from left:] V_N rising edge to V_1 rising edge; V_P falling edge to V_2 falling edge.

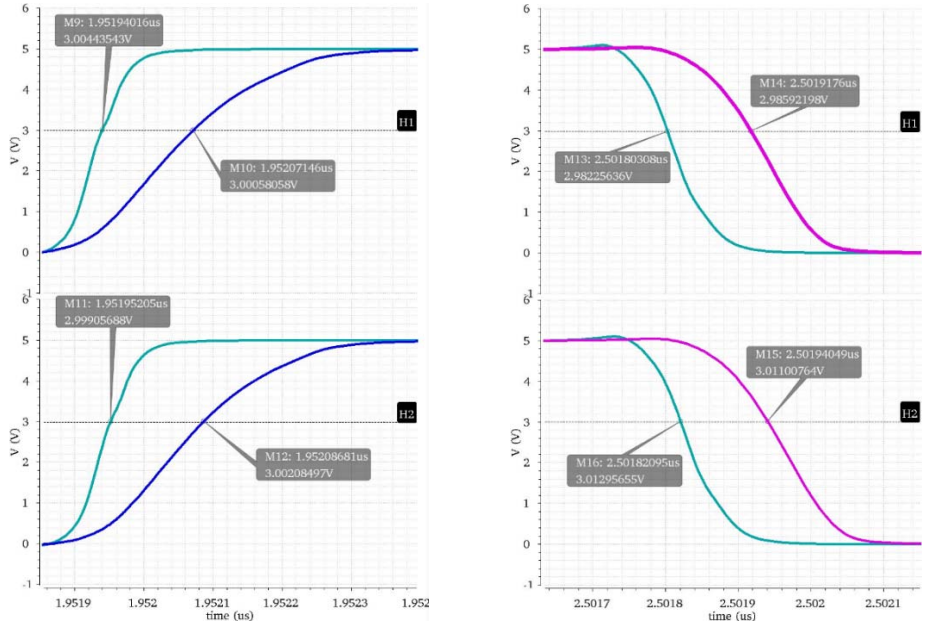


Figure 3.17. Cadence Ultrasim simulation results for the transition delay at 50 ° C (top) with different process corner models, [from left:] fast NMOS slow PMOS (fs) models; slow NMOS fast PMOS (sf) models.

and IN_P is 7 ns. The driving pulses for IN_1 and IN_2 are set respectively to IN_N and IN_P for the whole duty cycle.

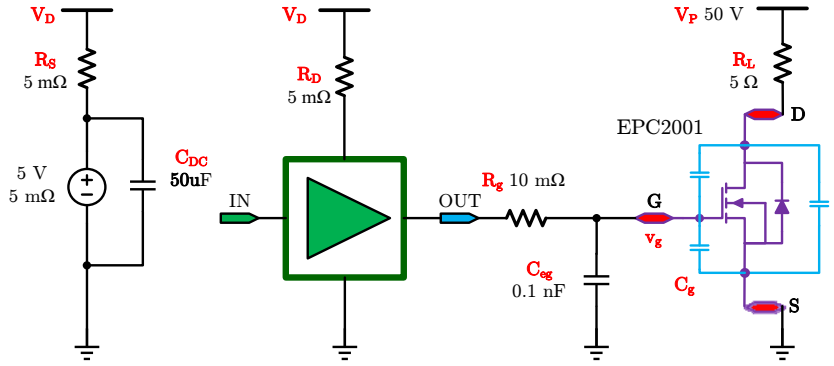


Figure 3.18. Test circuit schematic diagram for several gate drivers' simulations.

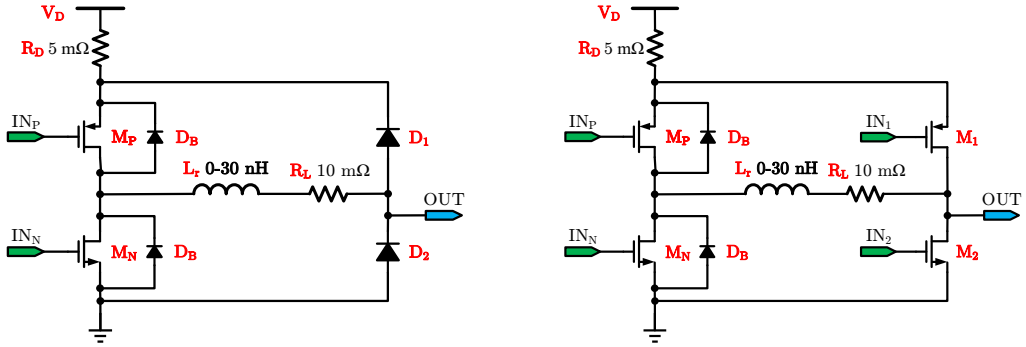


Figure 3.19. Schematic diagram for the gate drivers, [from left:] type (c) and type (g).

Figure 3.20 shows the Cadence Spectre simulation for conventional gate driver of type (a) while the gate inductance was set to 0, 2, 4, 6 nH. Even with this simple simulation at 2 nH gate inductor, the peak V_{GS} value has already exceeded 6 V, which is the maximum allowable gate-source voltage for eGaN® devices. This shows that the conventional gate driver not only suffers the inherent driving loss, any parasitic gate inductance will likely degrade the gate voltage and result in the device failure.

Figure 3.21 shows Cadence Ultrasim simulations for the average gate

driving losses and power device switching losses[1] of the gate drivers from type (a) to type (g) listed in Table 3.4. To achieve the best accuracy and avoid the convergence problems of Spectre for switching simulation, the Ultrasim simulator is chosen with simulation mode of "Spice (S)" and speed mode of "Extreme Accuracy (1)". The switching frequency is 10 MHz with 50% duty cycle. The resonant inductor values is chosen from 0 nH to 30 nH with the step size of 2 nH. The inductor series resistance is fixed at 10 mΩ. The type (a) conventional gate driver also includes the resonant inductance as its gate inductor. For resonant gate drivers, different control signals are required for different resonant conditions. As the gate resonant inductor changes, the pulse width of the driving signals will also need to be adjusted with a resolution of 0.5 ns in every 30 us run of transient simulation of each topology to obtain the desired 5 V turn-on and 0 V turn-off gate-source voltage.

Table 3.4: Components' values used in Cadence Ultrasim simulations for conventional gate driver types (a), resonant gate drivers type (b), (c), (d), (e), (f) and (g).

Type	M_P	M_N	M_1 (D_1)	M_2 (D_2)	D_B
(a)	pfetm, wt=2m, l=0.7m, nf=200 m=12	nfetm, wt=1m, l=0.7m, nf=200 m=12			
(b)	SAA (Same As Above)	SAA	sbdi, w=2u, l=30u, nf=2, m=500	sbdi, w=2u, l=30u, nf=2, m=500	
(c)	SAA	SAA	SAA	SAA	dipdnw, w=5u, l=2u, nf=2, m=100
(d)	SAA	SAA			
(e)	SAA	SAA			SAA
(f)	SAA	SAA	pfetm, wt=2m, l=0.7m, nf=200 m=6	nfetm, wt=1m, l=0.7m, nf=200 m=6	
(g)	SAA	SAA	SAA	SAA	SAA

The control signals for diode-clamped resonant gate driver was reported to be not sensitive to the variations of the exact values of resonant inductance

[1] The device switching loss is computed as the averaged product of V_{DS} and I_{DS}. It is larger than the real device switching dissipation observed during test.

[39] [57]. However, due to the reverse recovery charges at the moment of turning off a diode, it is difficult to have an ideal turn-on or turn-off gate-source voltage. Figure 3.22 shows the turn-on and turn-off waveforms of V_{GS} for the EPC2001 in the resonant gate driver type (b). The resonant inductor is 16 nH. The control signal pulse width is swept from 3 ns to 12 ns with step of 1 ns. It shows that the final turn-off V_{GS} level is approaching 0 V as the turn-off pulse width keeps increasing. However, the width cannot be too large since it will finally approach the driving loss of a conventional gate driver. It also increases the minimum switching duty cycle. This is due to the reverse recovery charges when the NMOS FET M_N is turned off, the inductor current recovery through the body diode of PMOS FET M_P is finished. The reverse recovery charges must flow through the body diode M_N. Since this recovery path is not directly connected to ground, a small oscillation at middle point of the M_P-M_N leg will finally settles and leads to a non-zero V_{GS} voltage. This also happens to the turn-on process such that different turn-on control signal will lead to different V_{GS} "on" potential. Considering with the sensitive gate-source voltage rating of GaN HEMT power devices, the previously acknowledged "insensitive" controlling for diode clamped resonant gate driver proves to be control dependent for GaN devices. The advantages of the type (b) or (c) resonant gate driver is not obvious.

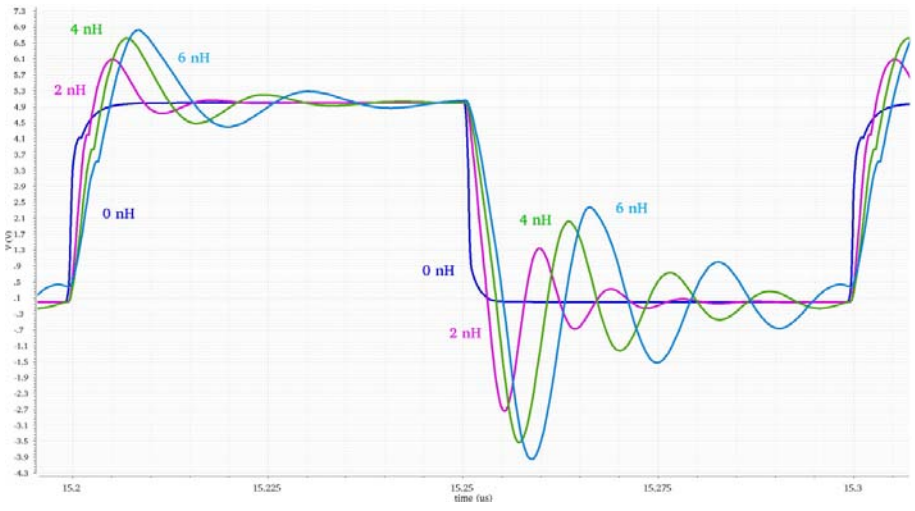


Figure 3.20. Cadence Spectre schematic simulation of V_{GS} voltage waveforms of EPC2001 for conventional gate driver type (a) with gate inductor values at 0, 2, 4, 6 nH.

Figure 3.23 shows the voltage waveforms (V_{GS}) of the GaN FET device for the three representative resonant gate driver configurations type (b): diode-

clamped, type (d): non-clamped and type (f): MOSFET-clamped. Both type (b) and (d) suffers the reverse current of the diodes, especially during the discharge process. Because the reverse current is also resonating with gate inductor, the discharging undershoot of type (d) is more obvious. The gate driver type (f) provides the best gate voltage performance. There is no obvious charging overshoot or discharging undershoot in type (f).

Figure 3.24 also shows the current waveforms (I_{GD}) of the gate driver power supply V_D for the gate driver configurations type (b), (d) and (f). The positive voltage shows the current flowing out of the supply, while the negative current recovered to the supply. It shows all these resonant gate drivers save the driving power by partial recovery of the supply charges. Both type (b) and (d) have a "negative bump" after their positive dissipating current. This is due to the reverse current mentioned above.

The device switching power loss in Figure 3.21 is explained in previous footnote. The plotted values are computed averaged values of the product of the GaN device V_{DS} and I_{DS}. Figure 3.25 shows the waveforms for the proposed resonant gate driver with MOSFET-clamping, the driver type (f) with 16 nH gate inductance. When gate voltage V_{GS} charges about 2 V, the GaN switch finishes the whole turn-on process within 2 ns. The turn-off process starts when the V_{GS} drops to 1 V. The power supply current cannot follow the speed of the turn-off of the device. It charges the device drain node through a typical RC curve while the device has already turned off. Even the switching power loss in Figure 3.21 is an over-estimated value, it still can be used as an indication of the switching performance of the device.

The proposed low-side resonant gate driver was simulated with a single EPC2001 power device switch connected to a resistive load with 50 V power supply. The switching frequency is 10 MHz and duty cycle is 50%. The gate driving signal can be created by an FPGA in a real testing setup. The inductor will be off-chip since the on-chip spiral inductor with the value around 10 to 20 nH provided by the process shows large parasitic effects which loses the benefit of resonant driving. Simulation shows the waveforms with the resonant inductor value sweeping from 6 nH to 20 nH with appropriate driving control. Increasing the resonant inductor will recover part of the charging energy back to source with little effect on the switching loss of GaN devices. This result is also due to the excellent switching characteristics of GaN devices. Simulation results are also compared to the conventional gate driver and the resonant gate driver topology C with clamping diodes (on-chip Schottky barrier diodes SBDI) [38]. The same trend of power saving profile between the proposed resonant gate

driver and the topology C with clamping diodes confirms the loss analysis in section 3.3. The resonant gate driver topology D with clamping MOSFET's [40] does not work well for this application since the switching's of the transistors at the gate significantly distort the gate voltage of the driven power devices.

Figure 3.26 shows the simulation comparison of gate driver loss results for between three types of the gate drivers working at the above configurations. Assuming 0 gate inductance, the conventional gate driver loss is about 407 mW. Assuming optimal control timing, the non-clamping resonant gate driver (type (d) in Table 3.4) and resonant gate driver with MOSFET-clamping (type (f) in Table 3.4) shows similar simulation results. It means the MOSFET-clamping resonant gate driver will achieve best power saving capability during gate transition period while provides low-impedance path to the load device gate capacitance during the steady state.

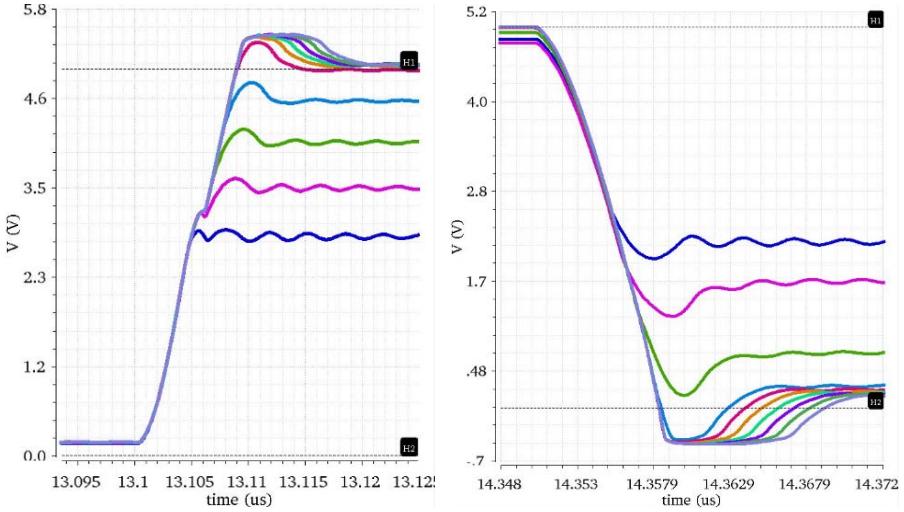


Figure 3.22. Cadence Spectre schematic simulation of V_{GS} voltage waveforms of EPC2001 for resonant gate driver type (b), [from top:] V_{GS} voltages, M_N gate control signals with pulse width of 3 to 12 ns.

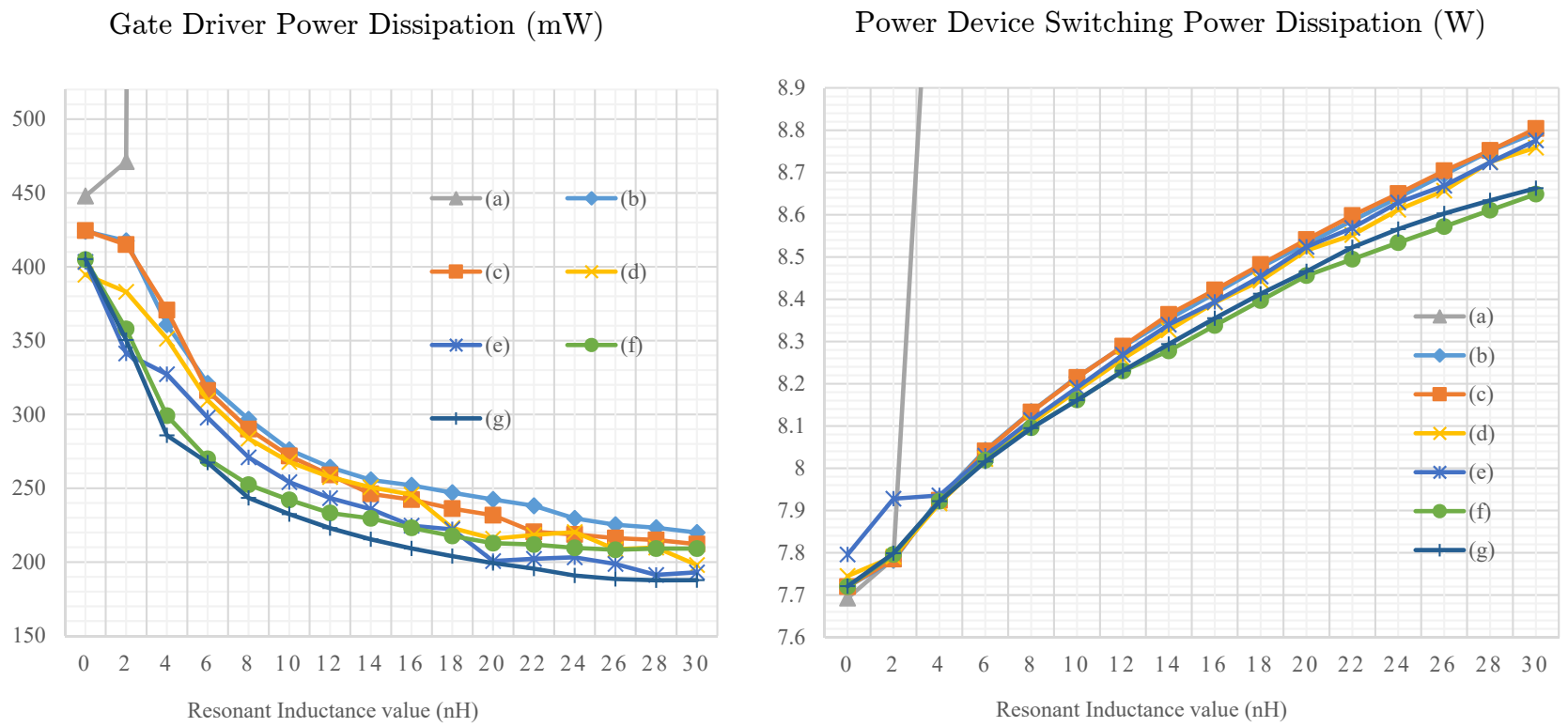


Figure 3.21. Cadence Ultrasim schematic simulation of gate driving losses and power device switching losses at 10 MHz for the gate drivers type (a), (b), (c), (d), (e), (f) and (g) in Table 3.4 with gate (resonant) inductance varies from 0 to 30 nH with the step of 2 nH.

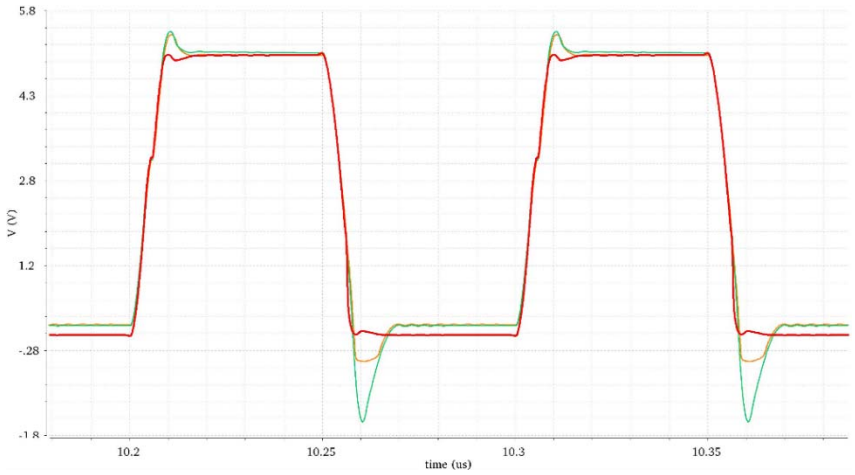


Figure 3.23. Cadence Ultrasim schematic simulation of gate-source voltage waveforms (V_{GS}) of EPC2001 for resonant gate drivers [orange] type (b), [green] type (d) and [red] type (f) in Table 3.4 with gate inductance of 16 nH.

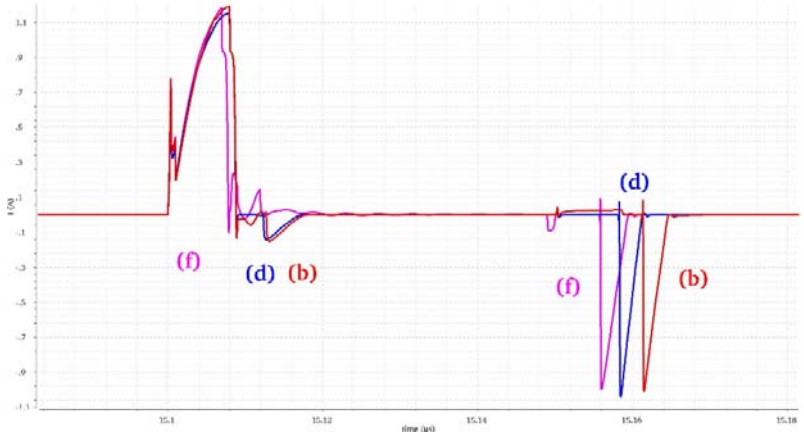


Figure 3.24. Cadence Ultrasim schematic simulation of gate driver power supply current waveforms (I_{GD}) of EPC2001 for resonant gate drivers [red] type (b), [blue] type (d) and [pink] type (f) in Table 3.3 with gate inductance of 16 nH.

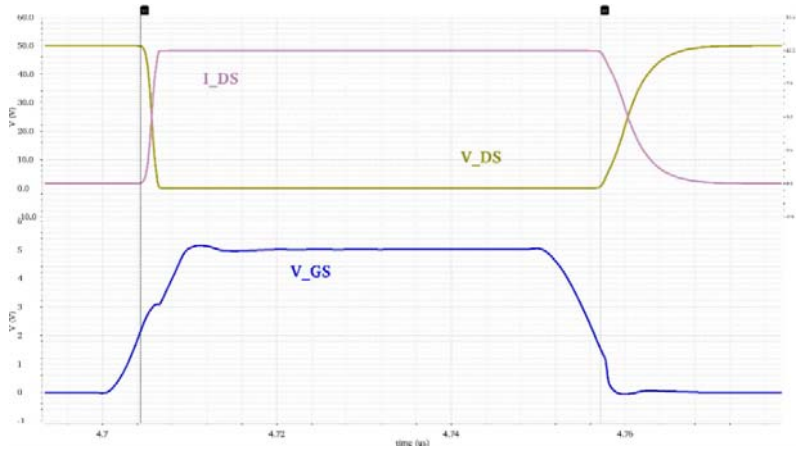


Figure 3.25. Cadence Ultrasim schematic simulation of GaN device voltage and current for the resonant gate driver with MOSFET clamp type (f) in Table 3.3 with gate inductance of 16 nH.

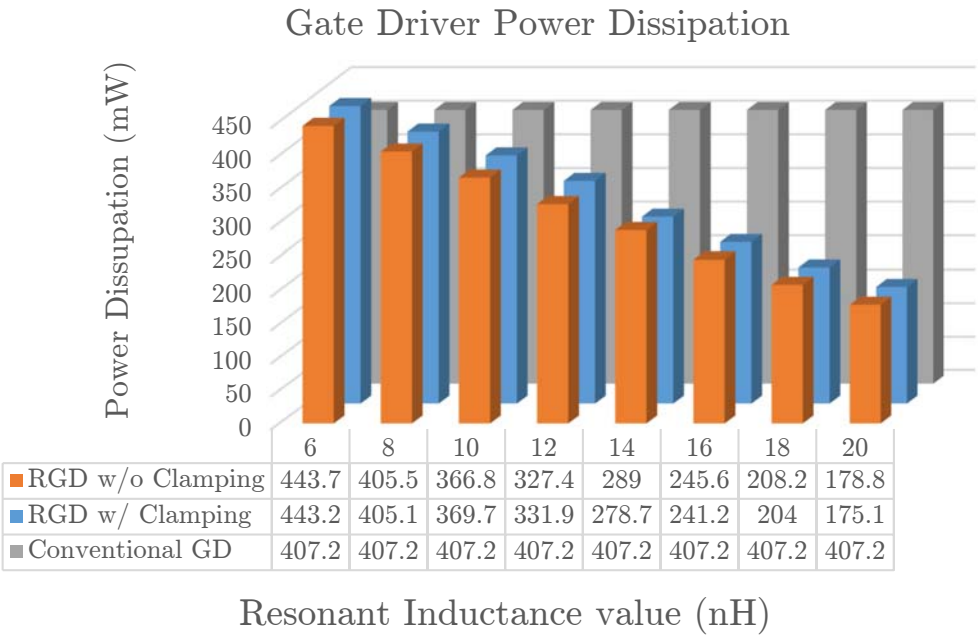


Figure 3.26. Cadence Spectre simulation of a gate driver with a single EPC2001 power load switching at 10 MHz with a resistive load connected to 50 V power supply, [from inside to outside:] conventional gate driver without resonant inductance, resonant gate driver with clamping diodes [38] and resonant gate driver without clamping devices [62].

Chapter 4

Design Implementation, Experimental Results and Analysis

4.1 Implementation of the MOSFET-Clamped Resonant Gate Driver

The final proposed MOSFET-clamped resonant gate driver for eGaN devices is designed, submitted and fabricated using a commercially available CMOS process. The basic structure follows with the design described in Chapter 3 with modifications based on simulation results. So the similar schematics are not shown in this chapter.

4.1.1 Circuit Block Design of the MOSFET-clamped RGD

Figure 4.1 shows the layout of the UVLO circuit block of the proposed resonant gate driver. The schematic is shown in Figure 2.12. All circuit components, including comparator, current mirror, resistive divider and ratioed transistors pairs are designed with strict common centroid [65] layout with dummy devices on the outer edges. From the simulation results, the turn-on voltage is about 4.0 V and turn-off voltage is about 3.4 V, with the built-in hysteresis of about 0.3 V. Figure 4.2 shows the extracted simulation results. As the power supply increases, the output starts to follow the power supply when $V_{DD} \approx 4.0$ V, and short to ground when the power supply falls from the desired 5 V to $V_{DD} \approx 3.4$ V to protect against unexpected working conditions of a converter using the switching devices when the gate driver power supply is too low such that the full switching condition is diminished. The testing results show the expected function of the UVLO.

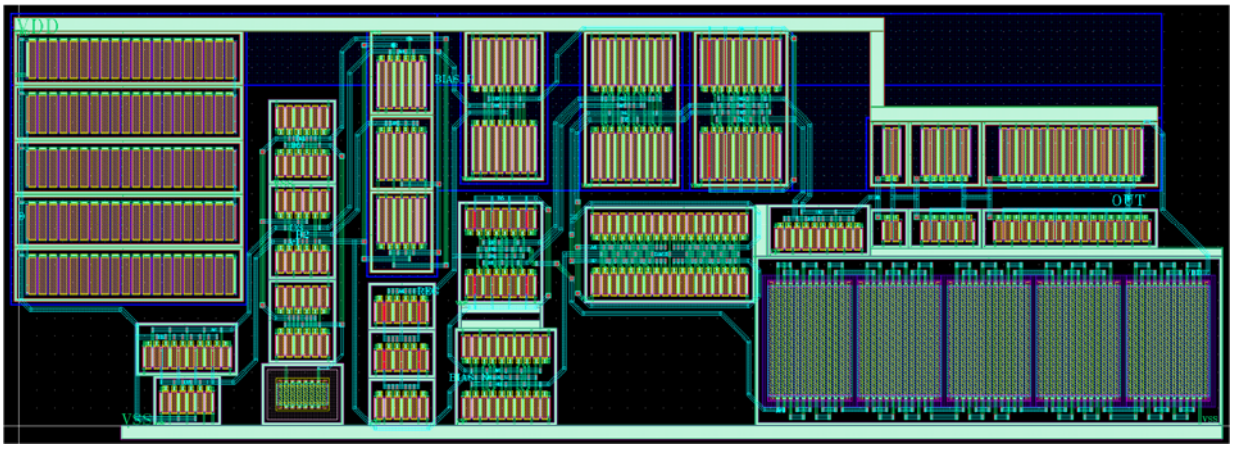


Figure 4.1. Layout of Under Voltage Lock Out (UVLO) circuit (340 µm × 120 µm).

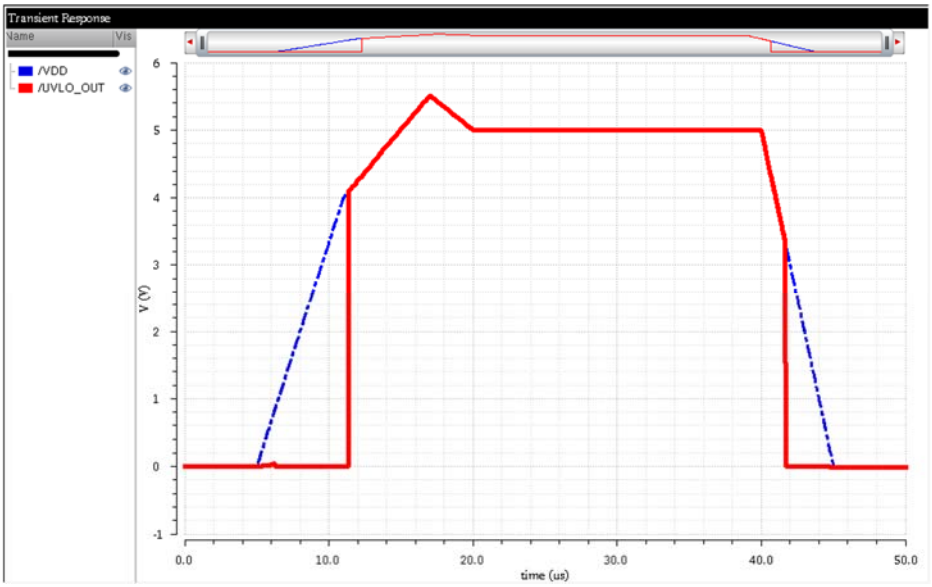


Figure 4.2. Extracted simulation of the UVLO in Figure 4.1.

The control circuit of the proposed driver is to implements the driving sequences shown in Figure 3.5. Figure 3.14 shows the schematic diagram and Figure 4.3 shows the layout of the control circuit. The devices of the control block are all 5 V devices for fast response. Figure 4.4 is a duplicate of the Figure 3.14 with corresponding node names used in the simulation results in Figure 4.5 and Figure 4.6.

Figure 4.5 and Figure 4.6 show the extracted simulation of the control block to implement the driving sequences in Figure 3.5. Figure 4.5 is for the input of the buffer chain while Figure 4.6 is for the output of the buffer. The *IN_ON* and

IN_OFF are input pulses with 10 ns pulse width and 1 ns rising/falling edges. The *P_OUT* and *N_OUT* terminals drive the main output charging (M_P in Figure 3.4) and discharging device (M_N in Figure 3.4) respectively of the resonant gate driver. The *P_C_OUT* and *N_C_OUT* nodes drive the charge clamping device (M_1 in Figure 3.4) and discharge clamping device (M_2 in Figure 3.4), respectively. Simulation shows the maximum skew or delay of those driving sequences is well below 1 ns.

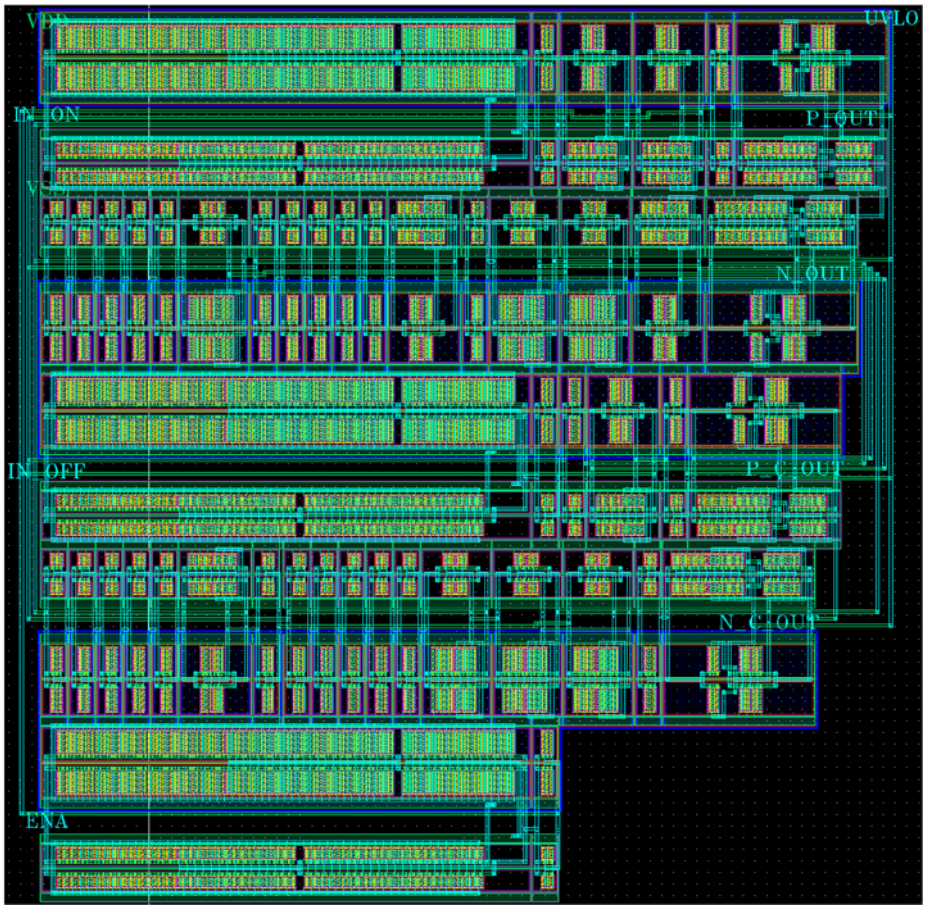


Figure 4.3. Layout of the control circuit (360 μm × 380 μm) with schematic diagram shown in Figure 3.14.

The output driving devices should be large enough to reduce the on-resistance while maintaining fast enough transitions for the resonant driving sequences. In this work the main charging PMOS (M_P in Figure 3.4) and discharging NMOS (M_N in Figure 3.4) FET's are sized as 128 × 48 (13/1.3) and 128 × 48(8/1.6) respectively, and the charge clamping PMOS (M_1 in Figure 3.4) and discharge clamping NMOS (M_2 in Figure 3.4) FET's are sized with half of

the respective charging/discharging devices. Figure 4.7 shows the layout block for 64×24(13/1.3) PMOS and 64×24(8/1.6) NMOS. For each set of 24 gates fingers devices, it has individual guard ring. This is support the body-diode conducting during the charging and discharging recovery stages as shown in Figure 3.5 (B) and (D).

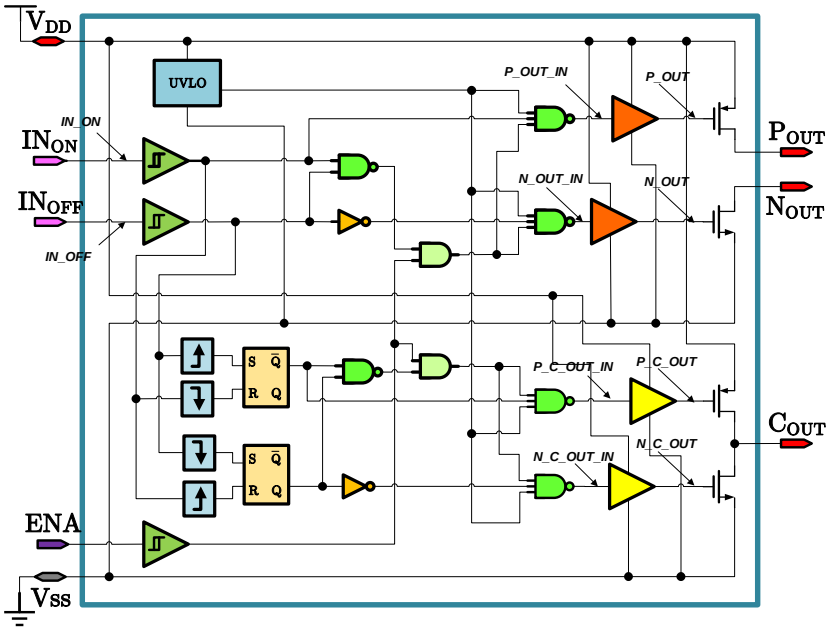


Figure 4.4. Schematic block diagram of Figure 4.3, 4.5 and 4.6.

4.1.2 Simulation Verification of the Design

To avoid the convergence problem of the fast switching conditions for Spectre simulation, a pseudo "body diode" *NW_PW* with minimum size is added in parallel with the main output charging /discharging devices, as shown in Figure 4.8 with green halo rings. The load is a 6 nF capacitance and the resonant inductance is 11 nH with 20 mΩ parasitic resistance. Two 200 mΩ resistors are also added in series to the power (*VDD*) and ground (*VSS*) of the gate driver supply path. The switching frequency is 1 MHz. Figure 4.9 shows the gate driver power supply current flow. The "dissipating current" is the current that flows out of the supply during the driver charging and charging recovery mentioned in stage (A) and (B) in Figure 3.5. The "recovery current" is the current that flows into the power supply during the driver discharging and discharging recovery mentioned in stage (C) and (D) in Figure 3.5. Simulation shows the

dissipated power due to the "dissipating current" is 114.5 mW, while the recovered power due to the "recovered current" is 40.79 mW. If we assumed the power loss of a conventional driver is the dissipated power without recovery process, the theoretical driver power dissipation ratio of the conventional to the proposed MOSFET-clamped driver working at this condition is about 65%. It means the resonant gate driver may reduce up to 35% gate driver power dissipation.

$$\frac{\text{RGD}}{\text{Conventional}} = \frac{\text{Dissipated} - \text{Recovered}}{\text{Dissipated}} = \frac{114.5\,\text{mW} - 40.79\,\text{mW}}{114.5\,\text{mW}} \approx 65\% \tag{4.1}$$

During the design, the original resonant driving topology is altered to accommodate the tradeoff between the speed and power. Figure 4.10 shows the the driver charging and charging recovery shown in stage (A) and (B) in Figure 3.5. One obvious difference is no expected charging recovery current feeding into the power supply during the state (B) of Figure 3.5. The M_1 clamping device actually assistants the load charging process by providing another charging path. The total charging current is the sum of existing the resonant inductor current from the charging device M_P and the new charging current from the clamping device M_1. Figure 4.11 shows the simulation current waveforms described. The blue curve "*MP1 Drain Current Out*" is the driver current that flows from the drain to the source of M_P, while the red curve "*MN1 Drain Current Out*" is the driver current that flows from the drain to the source of M_N. The green trace shows the negative current flowing out of the power supply. The current for the later portion of the charging process (B) includes the red body-diode current through the M_N device and the current from the clamping device M_1 that is the decaying portion of the green power supply current.

Similarly, Figure 4.12 and Figure 4.13 show the modified discharging process from stage (C) and (D) in Figure 3.5. Since no current feeding into the power supply during the modified charging process, the total driver power recovery process depends on the discharging process in Figure 4.12. The M_2 clamping device also assistants the load discharging process by providing another discharging path. The total discharging current is then the sum of the existing resonant inductor current from the body-diode of the discharging device M_P and the new charging current from the clamping device M_2. Figure 4.13 shows the simulation current waveforms described. The pink curve "*MN1 Drain Current In*" is the driver current flows from the drain to the source of M_N, while the blue

one "*MP1 Drain Current In*" is the driver current that flows from the drain to the source of M_P via its parasitic body diode. The green trace shows the positive current flowing into the power supply, which is the portion of charge recovered by the proposed resonant gate driver.

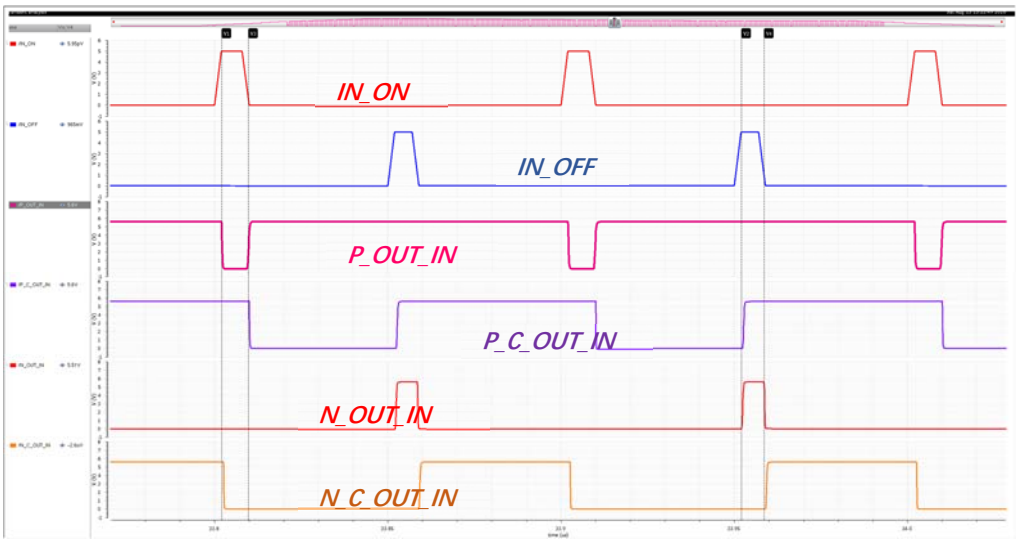


Figure 4.5. Extracted simulation of the control circuit in Figure 4.4.

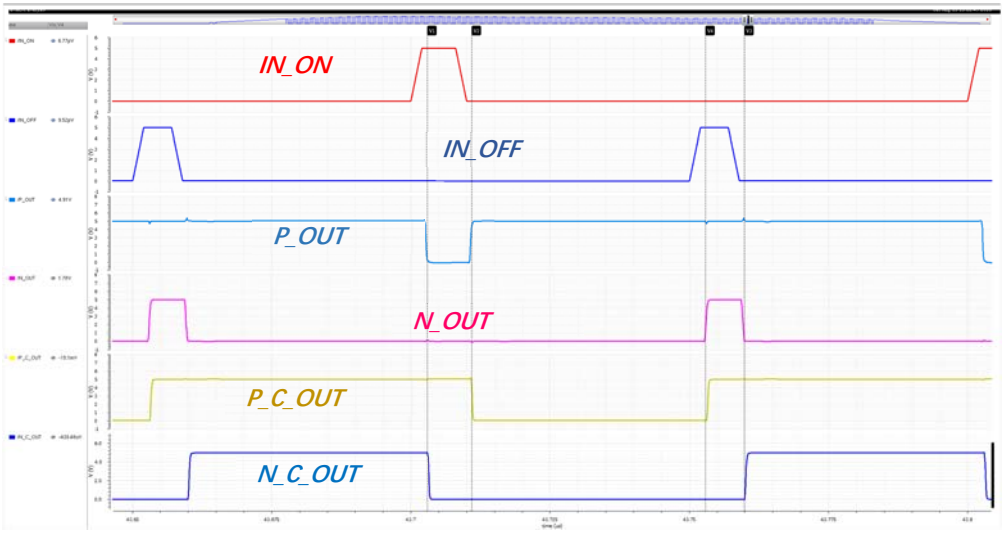


Figure 4.6. Extracted simulation of the control circuit in Figure 4.4.

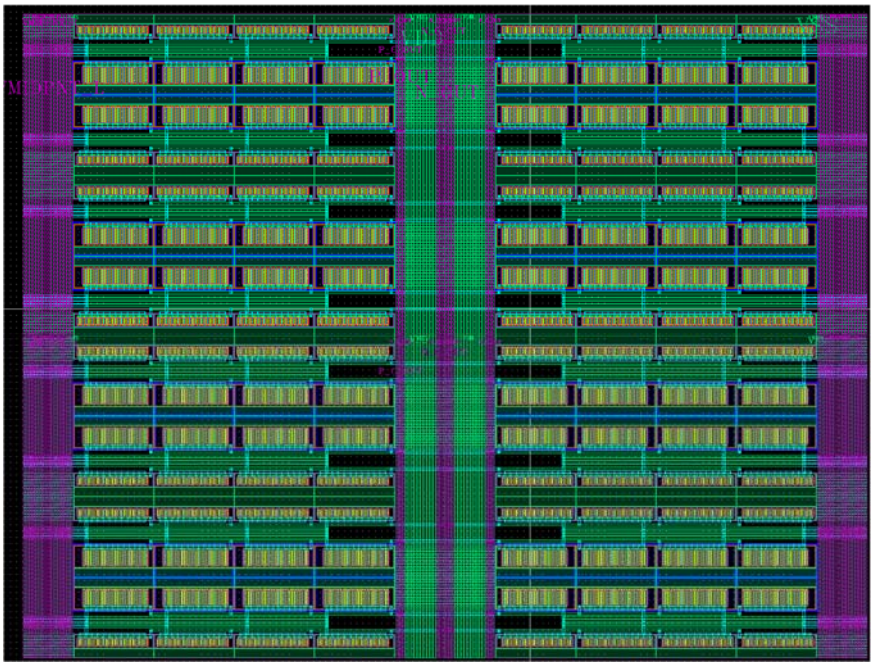


Figure 4.7. Layout of 64×24(13/1.3) PMOS and 64×24(8/1.6) NMOS FET's output buffer block (680 μm × 520 μm).

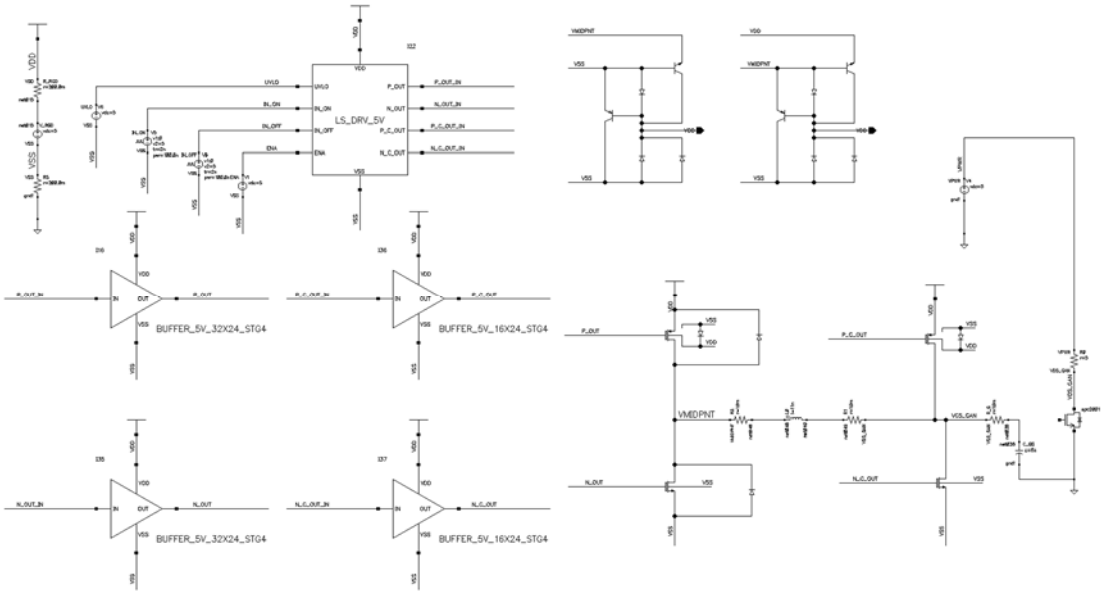


Figure 4.8. Top-level RGD schematic simulation including the control, buffer, driver and output stage with the capacitive load.

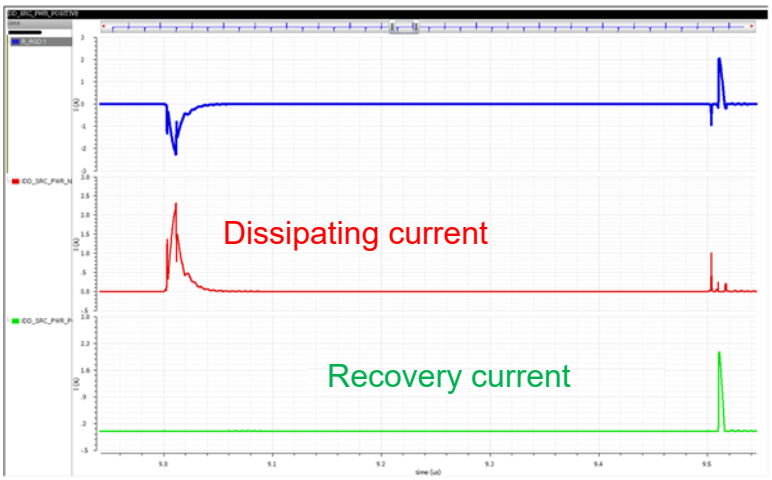


Figure 4.9. Simulation results of the gate driver power supply current flow in Figure 4.8.

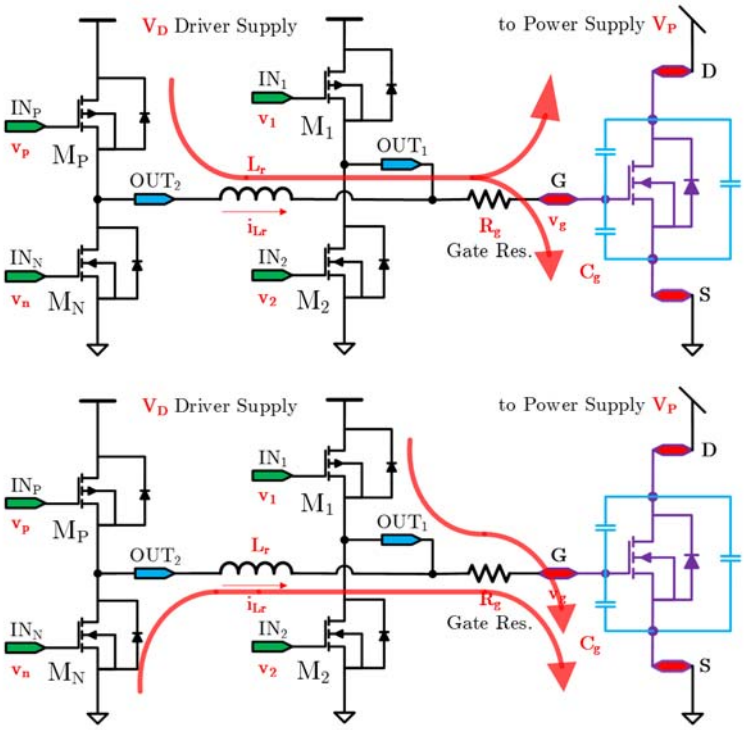


Figure 4.10. Modified charging process from the stage (A) and (B) shown in Figure 3.5.

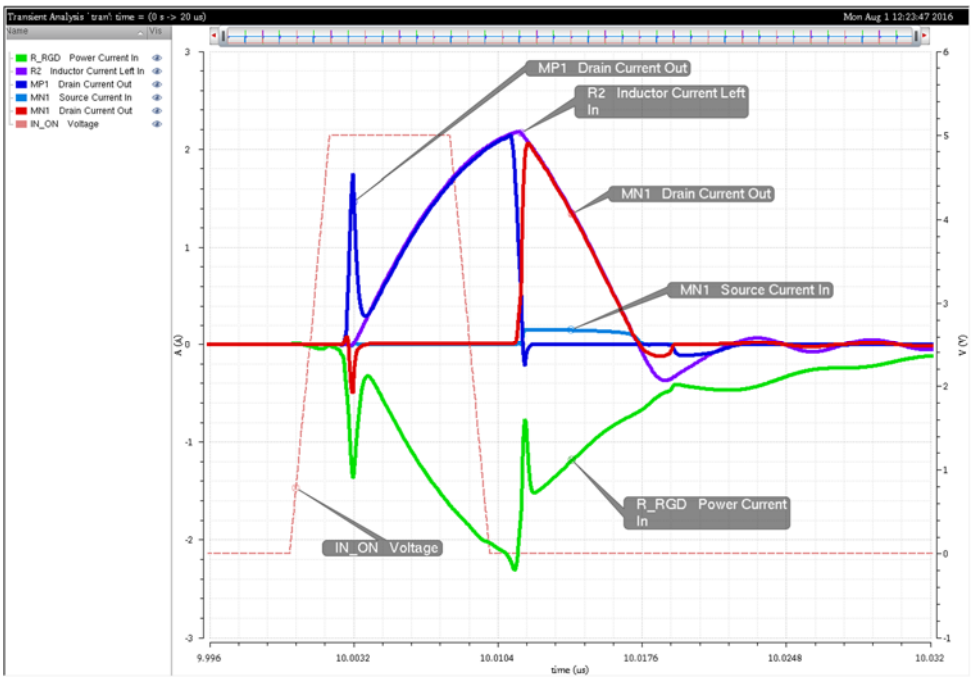


Figure 4.11. Simulation current flows for the charging process in Figure 4.10.

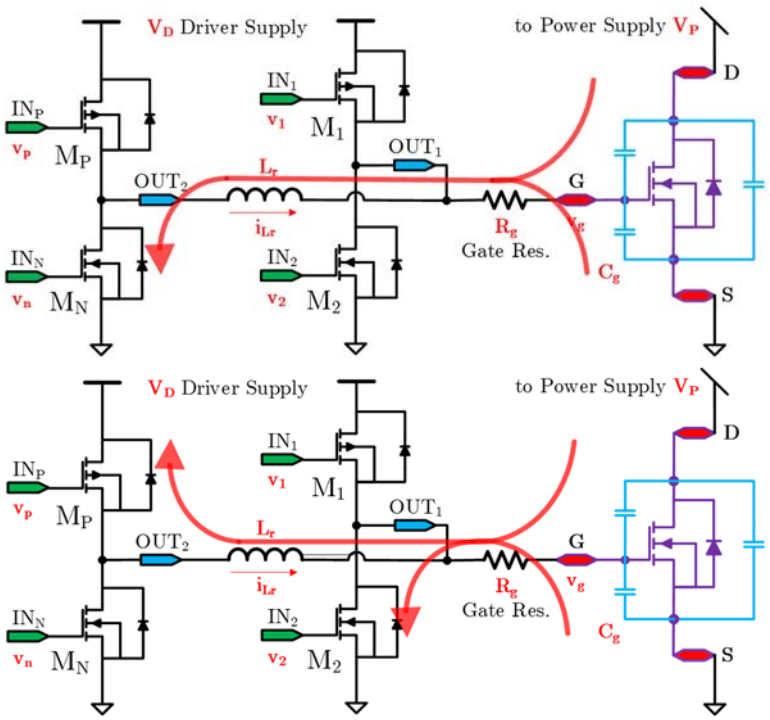


Figure 4.12. Modified charging process from the stage (C) and (D) shown in Figure 3.5.

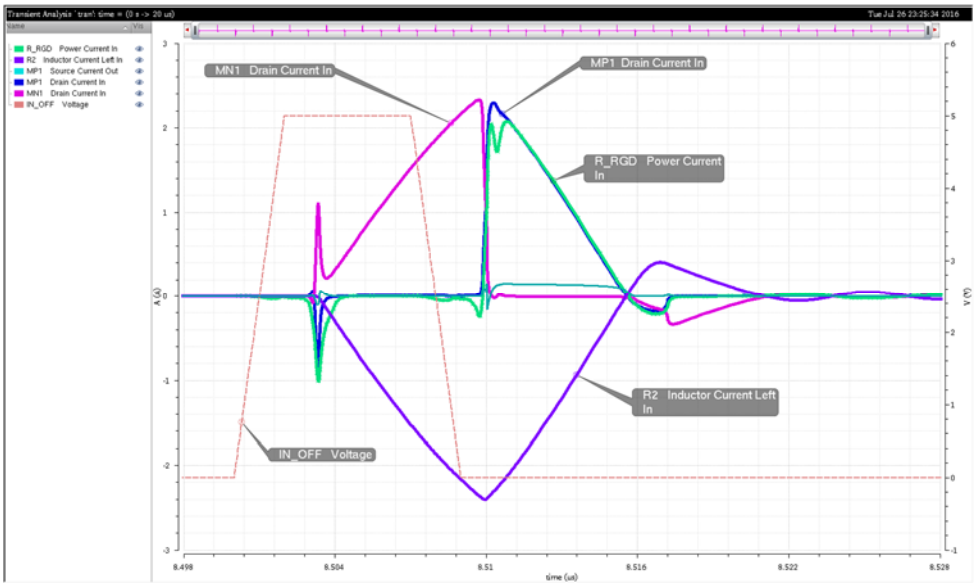


Figure 4.13. Simulation current flows for the discharging process in Figure 4.12.

4.2 Testing Results for Capacitive Load

The testing circuit is three separate circuits, each with one gate driver controlling a EPC2001 eGaN device with a SMD (surface mount device) capacitor with capacitance in the range from 1 nF to 10 nF. The gate driver IC's are the customized resonant gate drivers from this research and commercial eGaN driver LM5114. The turn-on and turn-off gate resistors for the LM5114 were chosen to be 1.5 Ω and 2.7 Ω according to the User's Guide of LM5114 and EPC2001 evaluation board [68]. By varying the load capacitance and switching frequency, the gate driver power loss is monitored by recording the current consumption of the driver power supply.

Figure 4.14 shows the test bench setup diagram. The two input signals are generated using the Agilent 33522A two channel waveform generator. The gate driver current is monitored by the Keithley DMM7510 high-precision digital multimeter.

Figure 4.15, 4.16, 4.17 and 4.18 shows the measurement results with 11 nH resonant SMD inductor (0602 footprint) and 10 MHz switching frequency for different capacitive loads, the corresponding measured output voltage waveforms for the resonant gate driver and LM5114 are side by side. The pink trace is the output waveform, the blue and green traces are the input controls.

Figure 4.19 shows the measured gate driver power dissipation ratio of RGD

to the corresponding LM5114 working at the same conditions. It shows that at low frequency the proposed resonant gate driver consumes much lower power. This is mainly due to the lower buffer driver power dissipation of the resonant gate driver. However, at higher switching frequency, the power saving reduced to less than 10%. This means the power recovery process is not significant.

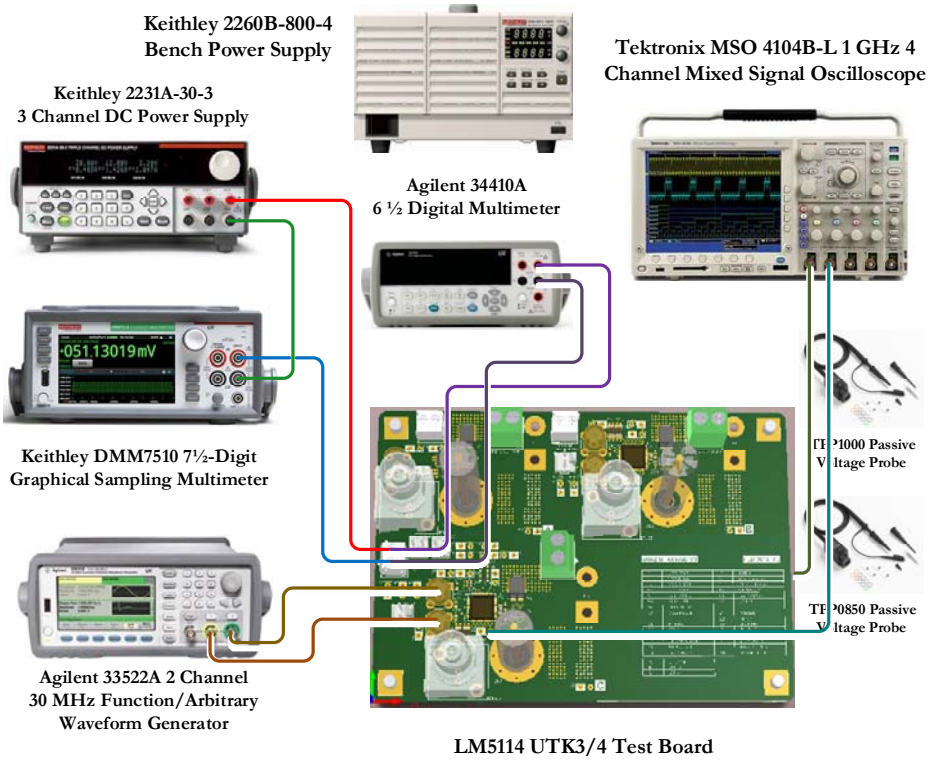


Figure 4.14. Test bench setup diagram.

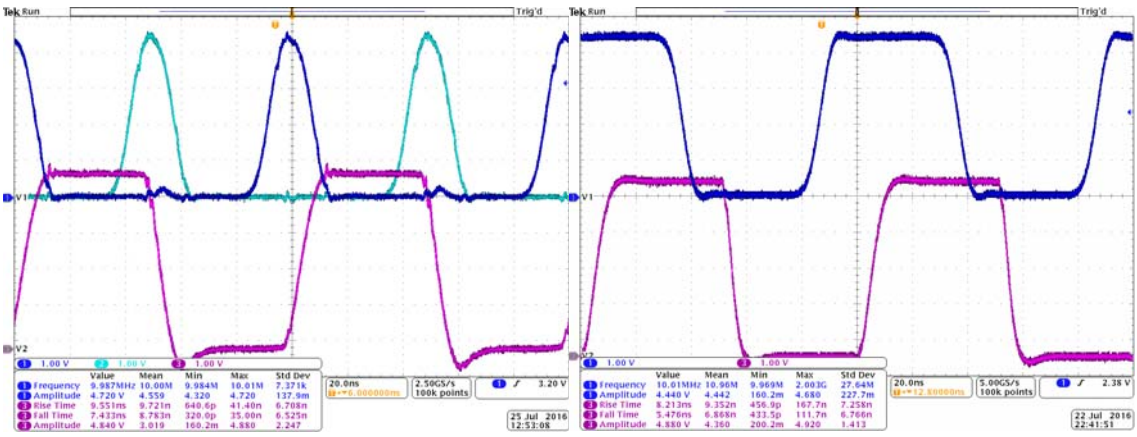


Figure 4.15. Measured waveforms for RGD (left) with 11 nH and LM5114 (right) at 1 nF load.

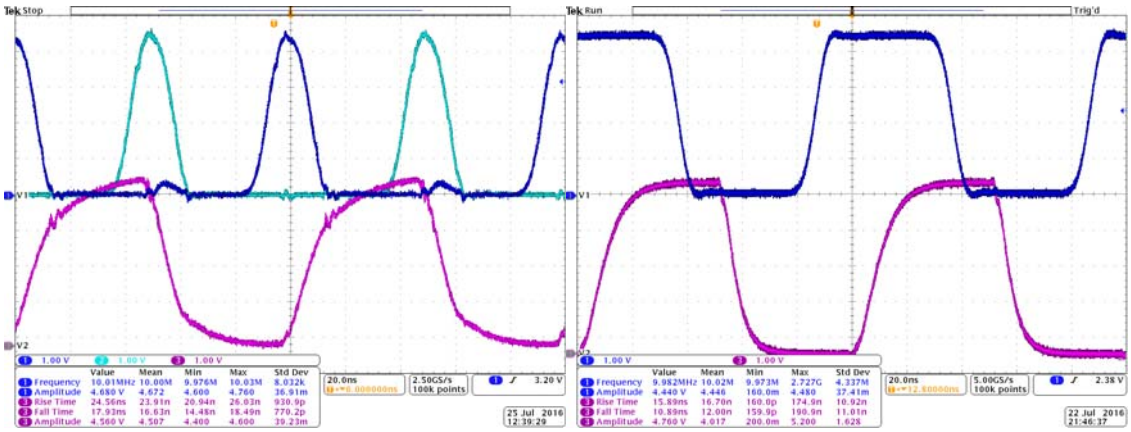


Figure 4.16. Measured waveforms for RGD (left) with 11 nH and LM5114 (right) at 2 nF load.

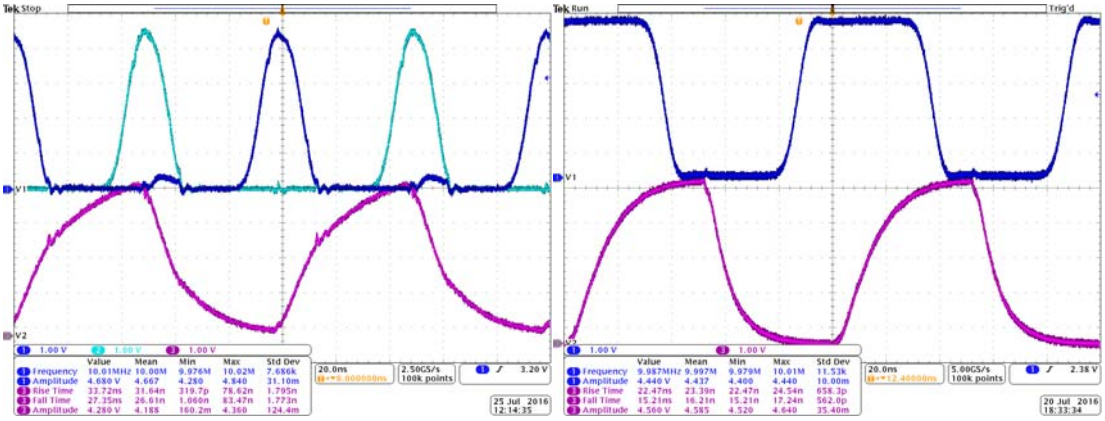


Figure 4.17. Measured waveforms for RGD (left) with 11 nH and LM5114 (right) at 3 nF load.

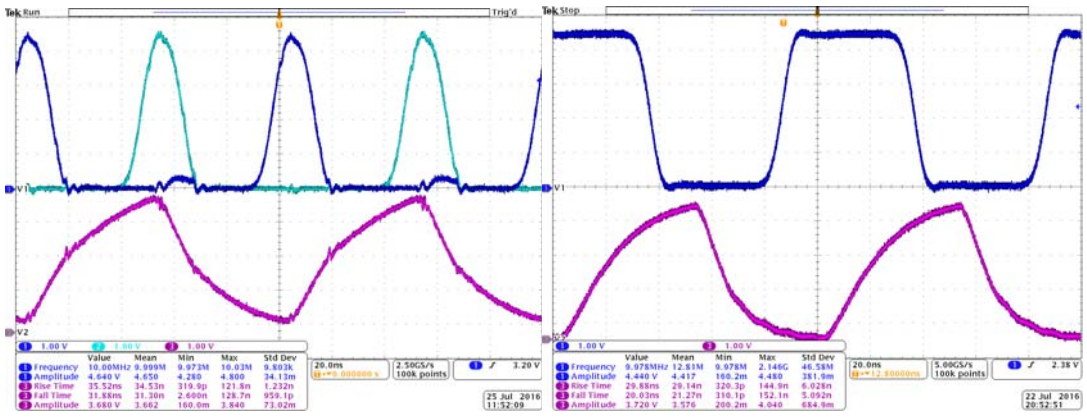


Figure 4.18. Measured waveforms for RGD (left) with 11 nH and LM5114 (right) at 4 nF load.

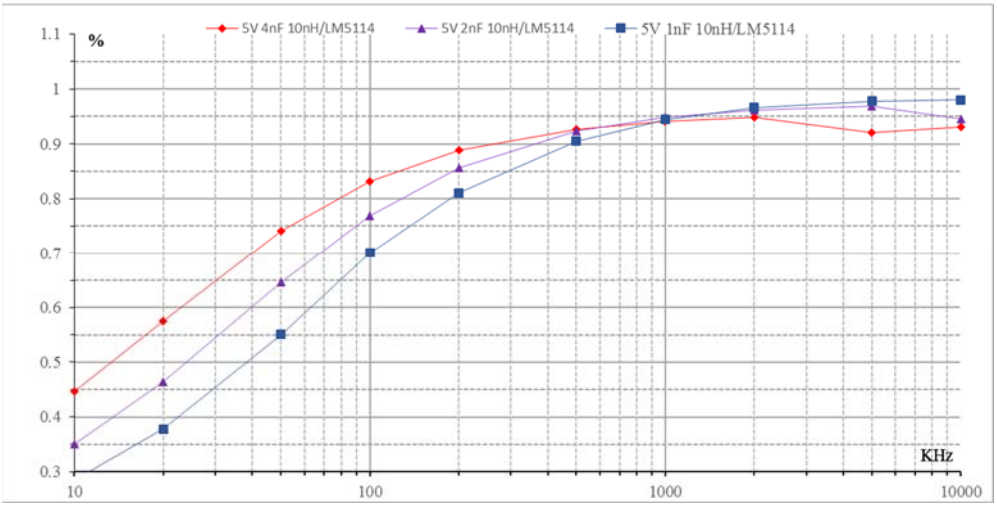


Figure 4.19. Measured gate driver power ratio of the RGD with 10 nH to LM5114 with switching frequency from 10 kHz to 10 MHz for capacitive loads of 1 nF, 2 nF and 4 nF.

4.3 Testing Results for Resistive and Inductive Load

Figure 4.20 shows the 2 rows of total six captured oscilloscope windows for the EPC2001 with resistive load. The loading resistor is 20 Ω and the supply voltage is 30 V. The top row is the waveforms of the RGD and the bottom row is the results of the LM5114. For each captured window, from the top to the bottom are the control input, V_{GS}, V_{DS} and I_{DS} of the EPC2001 GaN device. The measured gate driver power consumption ratio is similar to the results of a capacitive load in the range between 1 to 2 nF. Considering the input capacitance of EPC2001 of nearly 1 nF, with extra Miller capacitance induced by C_{DS} of the EPC during the turn-on process, this result is reasonable.

Figure 4.21 show measured double pulse waveforms for the resonant gate driver. The loading inductor is about 400 uH. Input driving signal is created using the arbitrary waveform editor of the Agilent 33522A two channel waveform generator. From the top to the bottom is the one of the two input signals, V_{GS}, I_{DS} and V_{DS} of the driving switch, EPC2001. The above measurement shows the fast driving capability and expected clamping protection during fast switching applications.

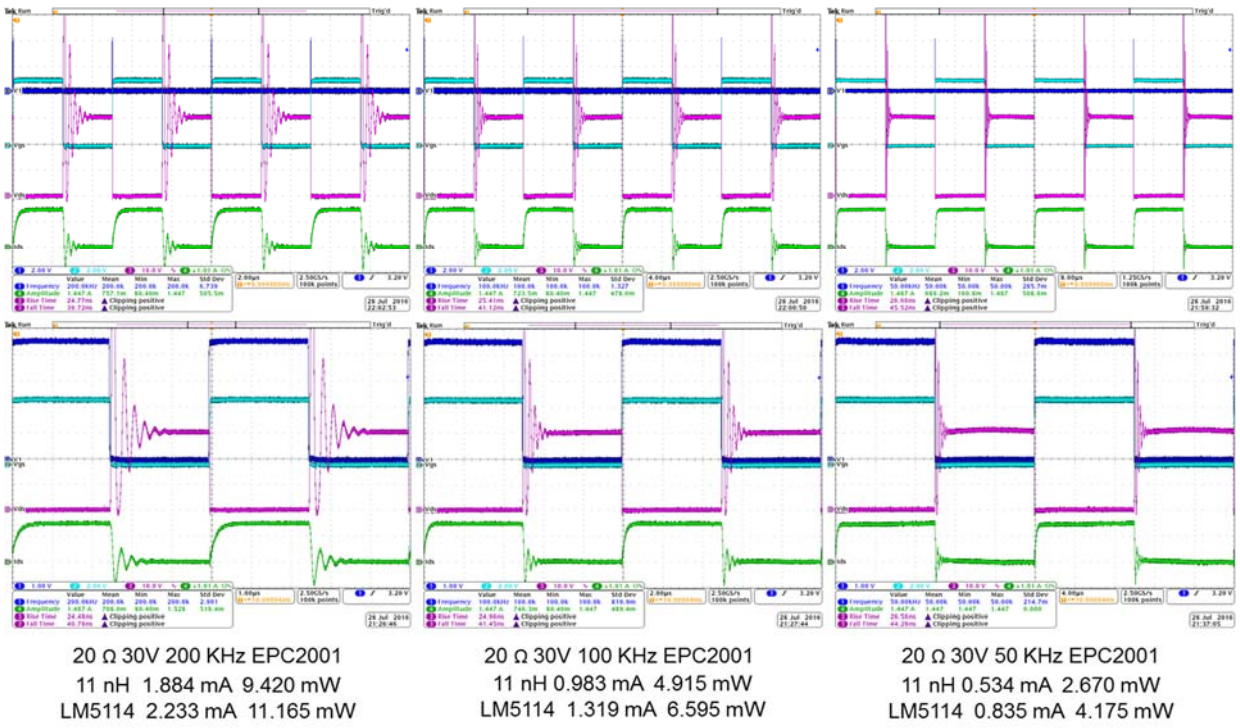


Figure 4.20. Captured oscilloscope window of resistive loading for RGD and LM5114 at 200 kHz, 100 kHz and 50 kHz.

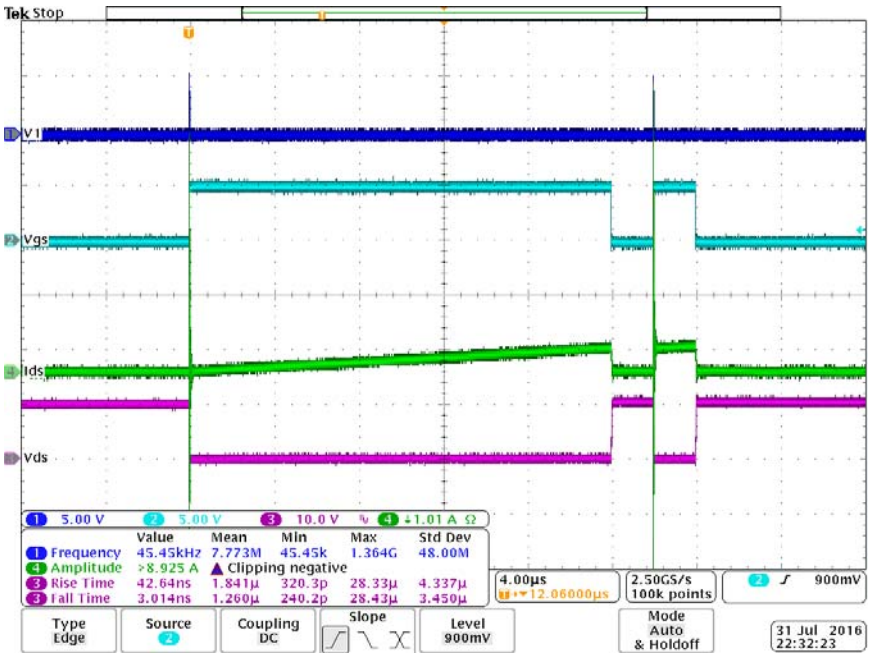


Figure 4.21. Measured waveforms of the double pulse test (DPT) of the proposed RGD.

4.4 Experimental Results Analysis

The experimental shows much less power saving capability (less than 10%) compared to simulation. Considering extra parasitic loss, it is reasonable to expect a maximum power reduction in the range of 20% to 30% from a working resonant gate driver compared to conventional driver LM5114. Even though the simulation is based on a simpler schematic due to the difficulty of convergence during Spectre simulation, the simulation results are still very helpful to diagnose the potential design, layout or process limitations.

Figure 4.22 and 4.23 show the measured waveform versus the simulated waveform of the RGD with 11 nH SMD resonant inductor and 4 nF loading capacitor. The green voltage waveform is the middle point between the PMOS charging and NMOS discharging device, which is also the OUT_1 node in Figure 3.4. The purple waveform is the driver output, which is also OUT_2 in Figure 3.4. In Figure 4.22 the green halo ring shows the charging transition waveforms, while in Figure 4.23 the discharging transition waveforms.

From the difference between the measured and simulated results shown in Figure 4.22 and 4.23, the design problems could stem from the following issues.

1) The driving force of the output devices is too low. This can be observed in the turn-on transition that the mid-point green waveform (V_M of Figure 3.4) is not pulled up sufficiently high to 5 V. During turn-off transition, this green waveform is pulled down to 3 to 4 V, far above the desired ground level.

2) The body-diode conduction voltage during the turn-off transition behaves like a capacitive ringing spike rather than a diode conduction. This also can be explained by the limited equivalent diode size with too large of a parallel parasitic resistance. Figure 4.24 shows a cross-section diagram of the NMOS and PMOS of the design process. The NMOS body-diode conduction happens during the turn-on charging recovery stage as (B) in Figure 3.4. The PMOS body-diode conduction happens during the turn-off discharging recovery stage as (D) in Figure 3.4. The larger red arrow shows most of the current should flow through the parasitic body-diode.

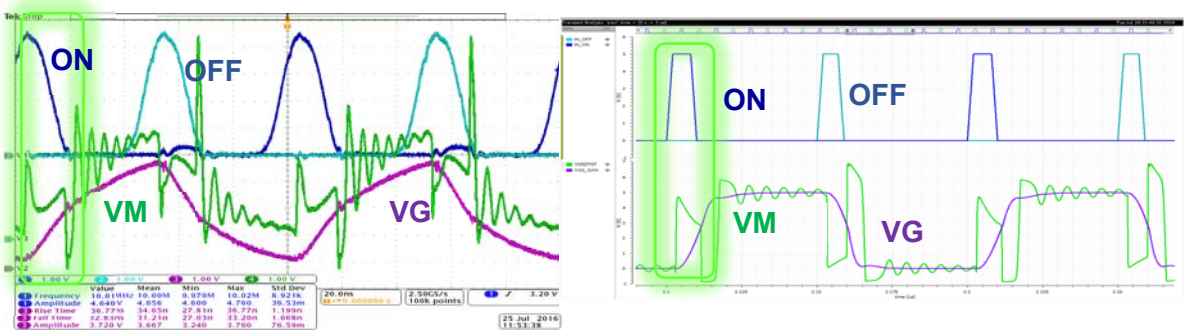


Figure 4.22. Measured vs. Simulated waveforms of RGD for 11 nH inductance and 4 nF load capacitance highlighted with turn-on transition.

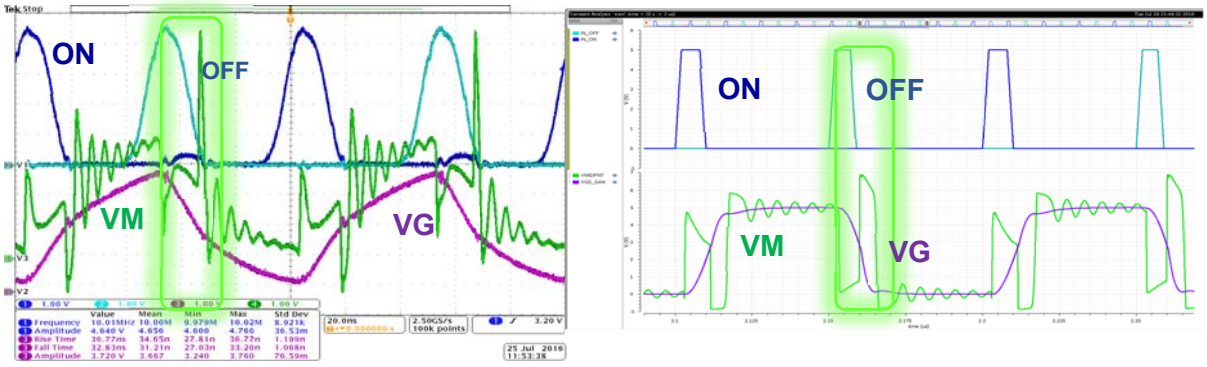


Figure 4.23. Measured vs. Simulated waveforms of RGD for 11 nH inductance and 4 nF load capacitance highlighted with turn-off transition.

3) The desired control pulse width should be large enough to initialize the charging and discharging process but short enough to start the recovery stages. The minimum pulse duty cycle for the Agilent 33522A waveform generator at 10 MHz switching frequency is 16%, which is 16 ns. Previous design simulation is based on 6 ns or even less. Figure 4.25 shows the simulation results with the control pulse width of 16 ns, 11 nH resonant inductor and 4 nF load capacitor. By reducing the schematic output device, the main charging PMOS (M_P in Figure 3.4) and discharging NMOS (M_N in Figure 3.4) FET's from the original 128 × 48(13/1.3) and 128 × 48(8/1.6) defined in Figure 4.8 to 128 × 24(13/1.3) and 128 × 24(8/1.6) respectively, and increasing the input control signal width from 6 ns in Figure 4.8 to 16 ns, the simulated middle point

waveforms in Figure 4.25 are similar to the measured waveforms shown in Figure 4.26. In Figure 4.26 the switching frequency of the driver is 10 MHz, while duty cycle the control signal pulses is 16 %, which is 16 ns, the lower limit of the arbitrary waveform generator. The green trace VM is the middle point voltage described above, and the purple VG curve is the output capacitor voltage.

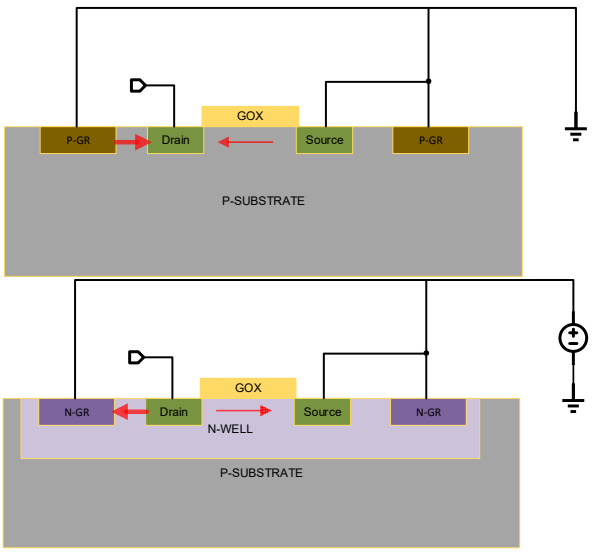


Figure 4.24. Cross-section of the body-diode conduction for NMOS M_N (left) and PMOS M_P (right) during the stage (B) and (D) in Figure 3.4 respectively.

Figure 4.27 and Figure 4.28 shows the mid-point voltage (V_M node of Figure 3.4) during turn-on and turn-off transition. The red curves shows main charging PMOS (M_P in Figure 3.4) and discharging NMOS (M_N in Figure 3.4) FET's up to 128×126(13/1.3) and 128×126(8/1.6) with 6 ns control signal width. The green waveform is for the size of 128×24(13/1.3) and 128×24(8/1.6) driving with 16 ns control pulse. Note the resemblance of the simulated waveforms at the fast switching middle point of the phase leg composed of the PMOS charging and the NMOS discharging devices in Figure 4.27 and 4.28 to the measured waveforms in Figure 4.22 and 4.23 further confirmed the reasons of unsatisfactory experimental results, indicated the guidance for the reversion of the future work.

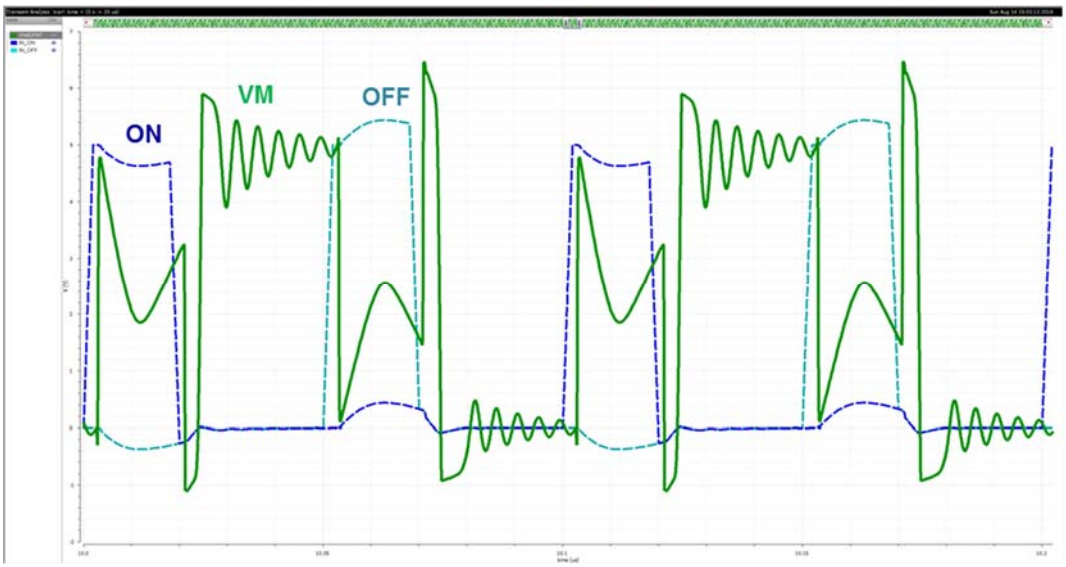


Figure 4.25. Simulation results for 10 MHz switching frequency, 16 ns control signals and reduced size of the output devices of the RGD with 11 nH inductor and 4 nF load capacitor.

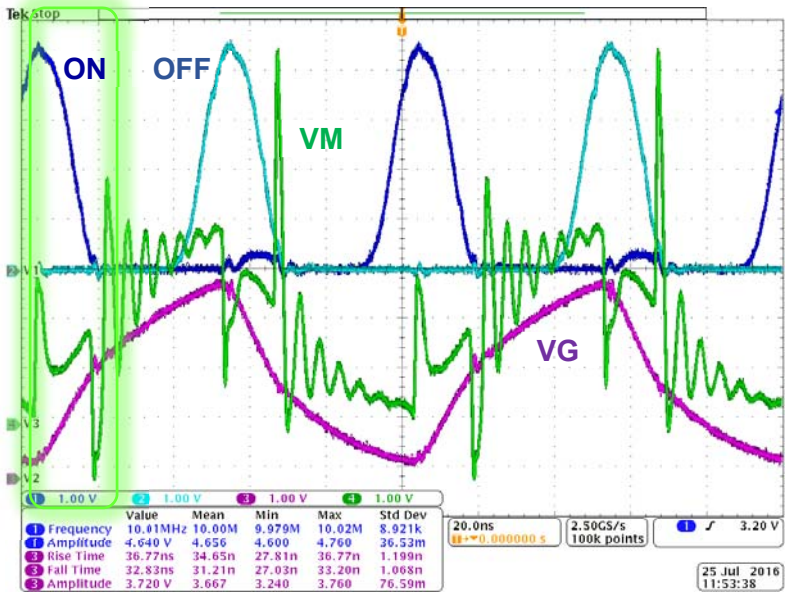


Figure 4.26. Measured waveforms for 10 MHz switching frequency, 16 ns control signals and reduced size of the output devices of the RGD with 11 nH inductor and 4 nF load capacitor.

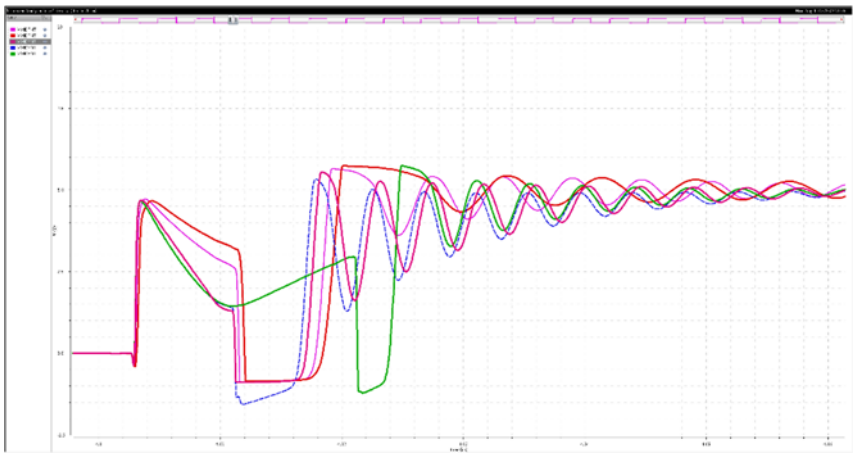


Figure 4.27. Simulation of turn-on transition mid-point voltage (V_M node of Figure 3.4) with control pulse width of 6 ns and 16 ns for different sizes of output devices.

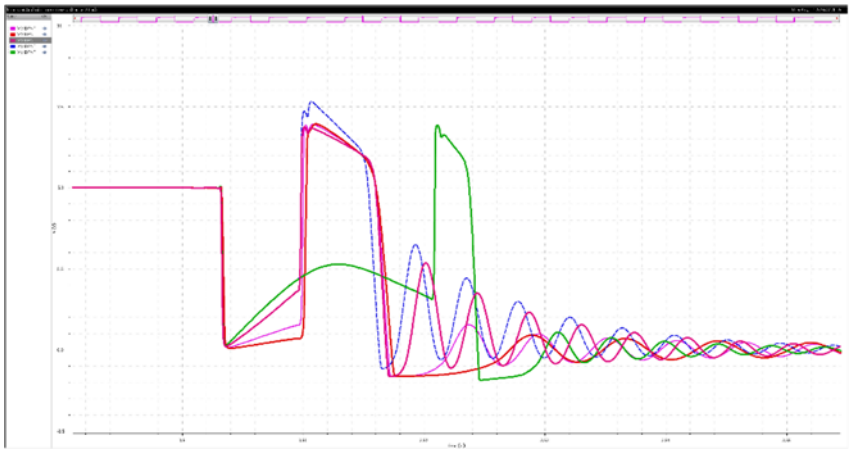


Figure 4.28. Simulation of turn-off transition mid-point voltage (V_M node of Figure 3.4) with control pulse width of 6 ns and 16 ns for different sizes of output devices.

Chapter 5

Conclusion and Future Work

A new resonant gate driver for enhancement mode GaN device (EPC2001 as an example) is proposed and implemented with a standard 5 V and 7 V CMOS process. Experimental results show the lack of power saving capability especially at high frequency. Further analysis on the testing and simulation results reveals the direction for future design. Recommendation for the future work includes the following design issues.

1) Increasing the output driving strength of the PMOS and NMOS devices aspect ratio to significantly larger than $128 \times 48(13/1.3)$ and $128 \times 48(8/1.6)$.
2) Using a FPGA or other programmable devices to generate less than 10 ns control pulse width. The ultimate solution on-chip is to include a coded pulse-width generator block to allow manual adjustment of the input control pulse width according to different driving conditions.
3) Increase body-diode conduction capability by dividing output devices in smaller sections using larger gate finger multiplier, with each section closed in a substrate or N-well guarding ring.
4) Provide more power and ground pads on-chip for the gate driver, reducing the parasitic resistance along the charging or discharging path.

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Appendix

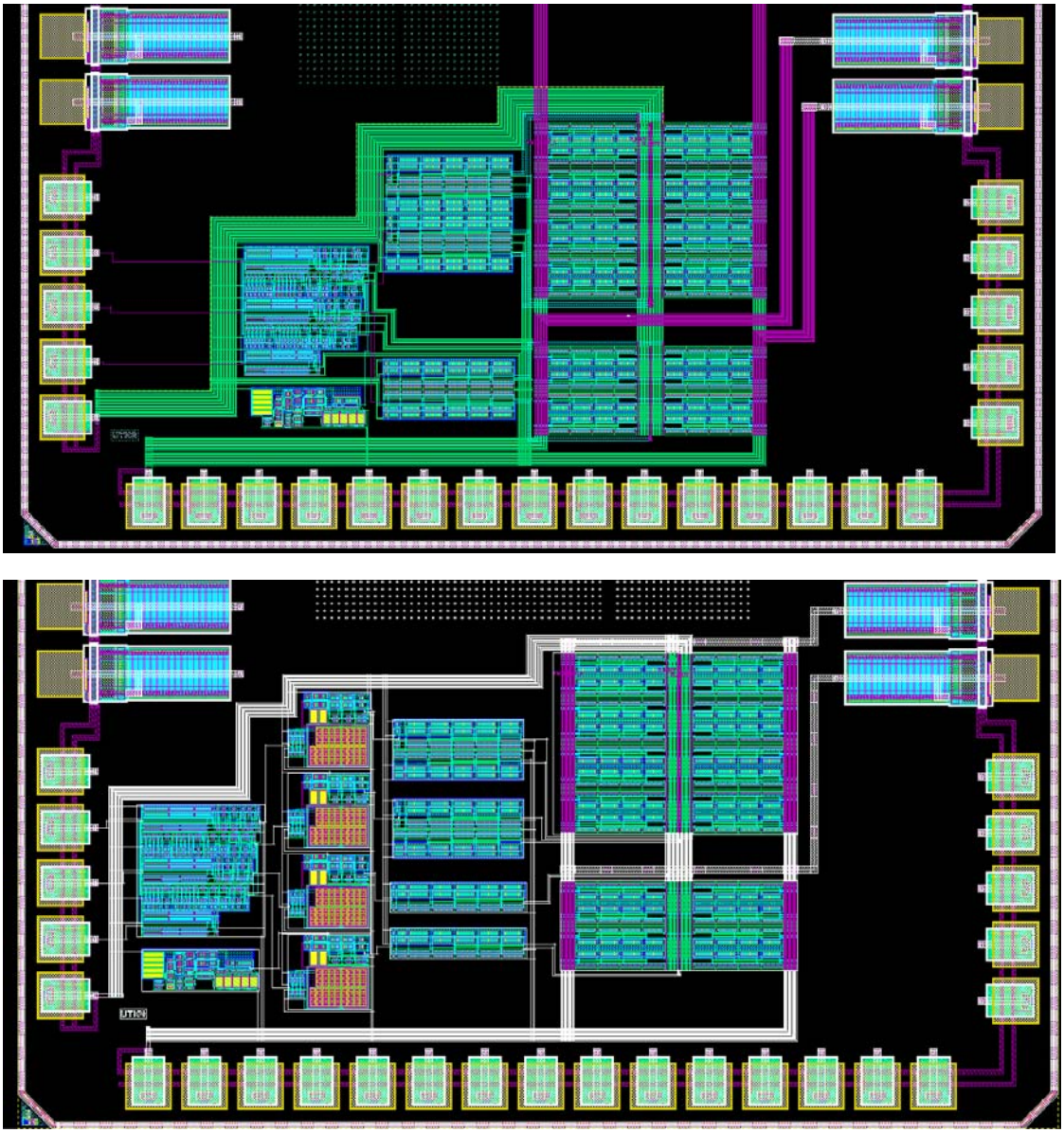
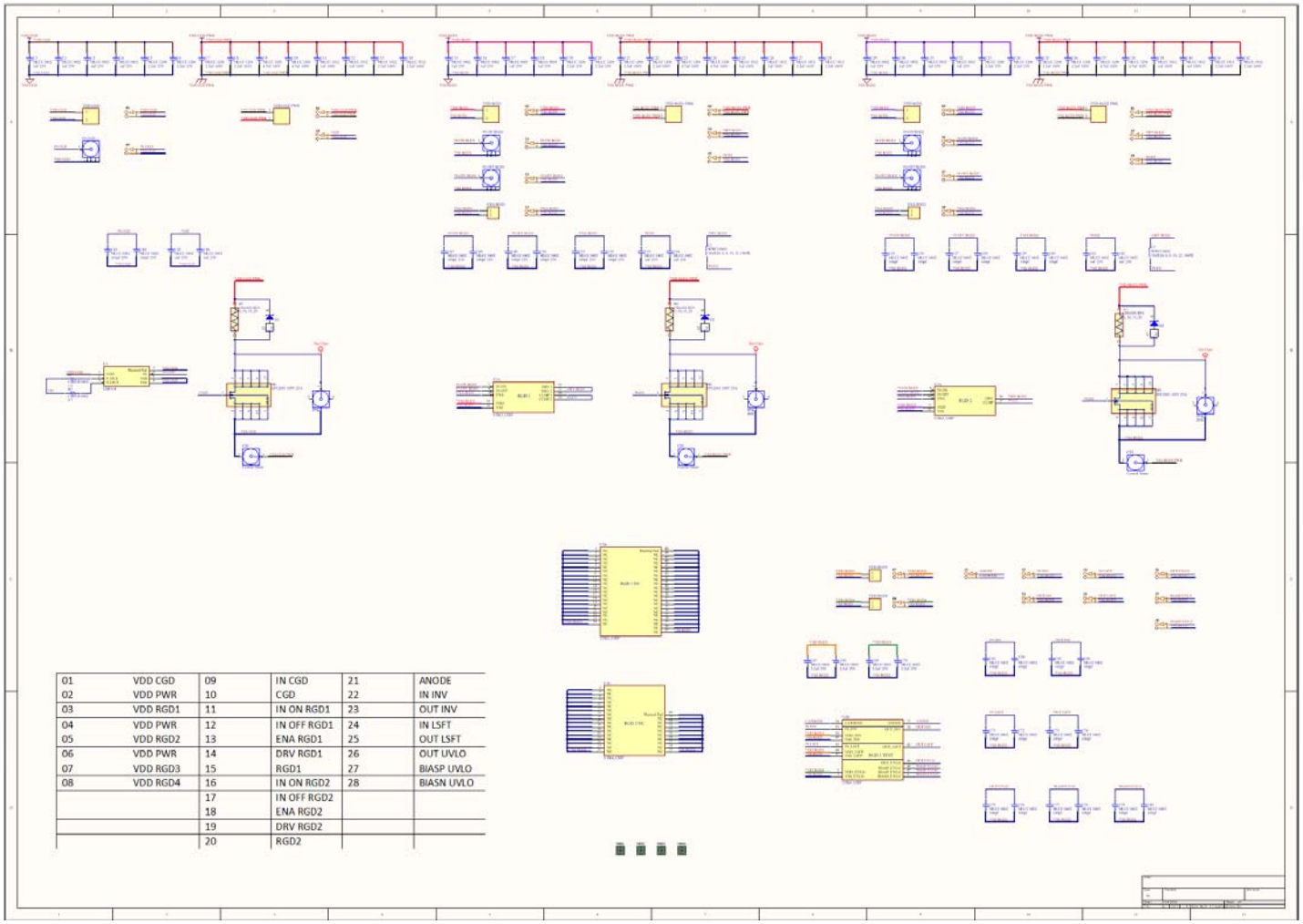


Figure A.1. Layout of the resonant gate driver, without level shifter (1600 µm × 1100 µm) (top) with level shifter (2000 µm × 1100 µm) (bottom).



01	VDD CGD	09	IN CGD	21	ANODE
02	VDD PWR	10	CGD	22	IN INV
03	VDD RGD1	11	IN ON RGD1	23	OUT INV
04	VDD PWR	12	IN OFF RGD1	24	IN LSFT
05	VDD RGD2	13	ENA RGD1	25	OUT LSFT
06	VDD PWR	14	DRV RGD1	26	OUT UVLO
07	VDD RGD3	15	RGD1	27	BIASP UVLO
08	VDD RGD4	16	IN ON RGD2	28	BIASN UVLO
		17	IN OFF RGD2		
		18	ENA RGD2		
		19	DRV RGD2		
		20	RGD2		

Figure A.2. Schematic of the testing PCB.

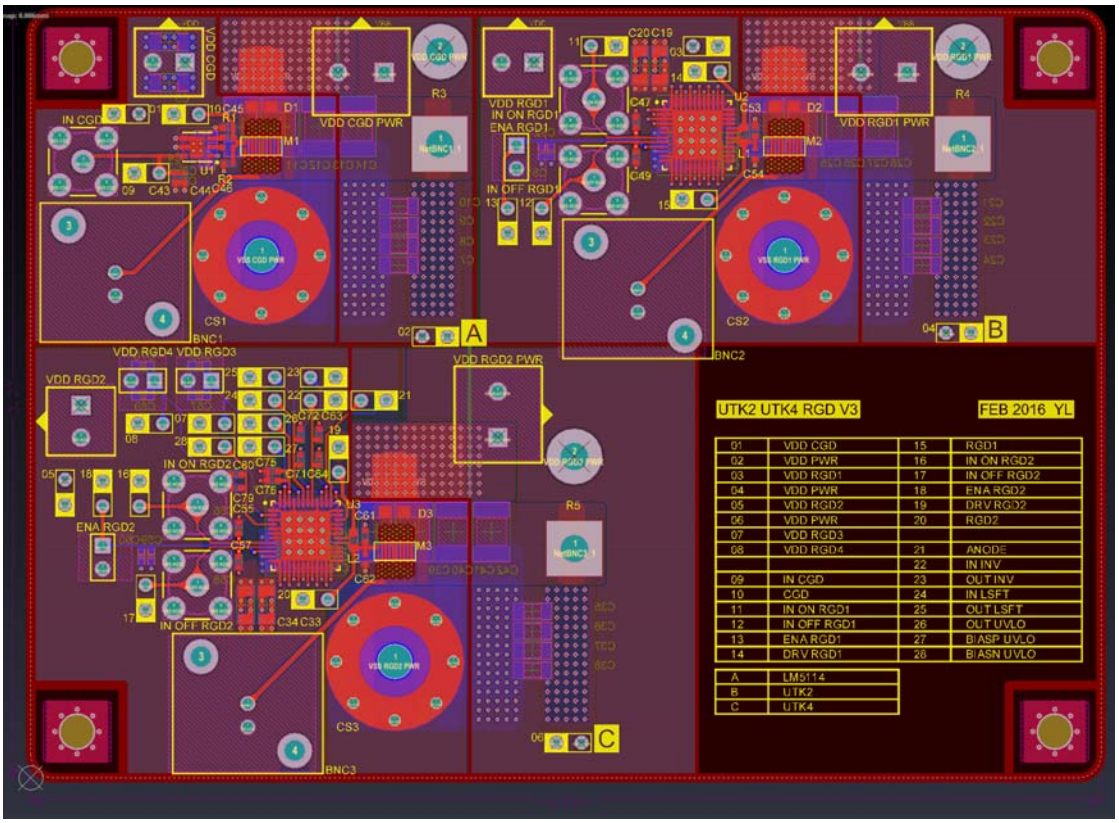


Figure A.3. Layout of the testing PCB (4.56” × 3.27”).

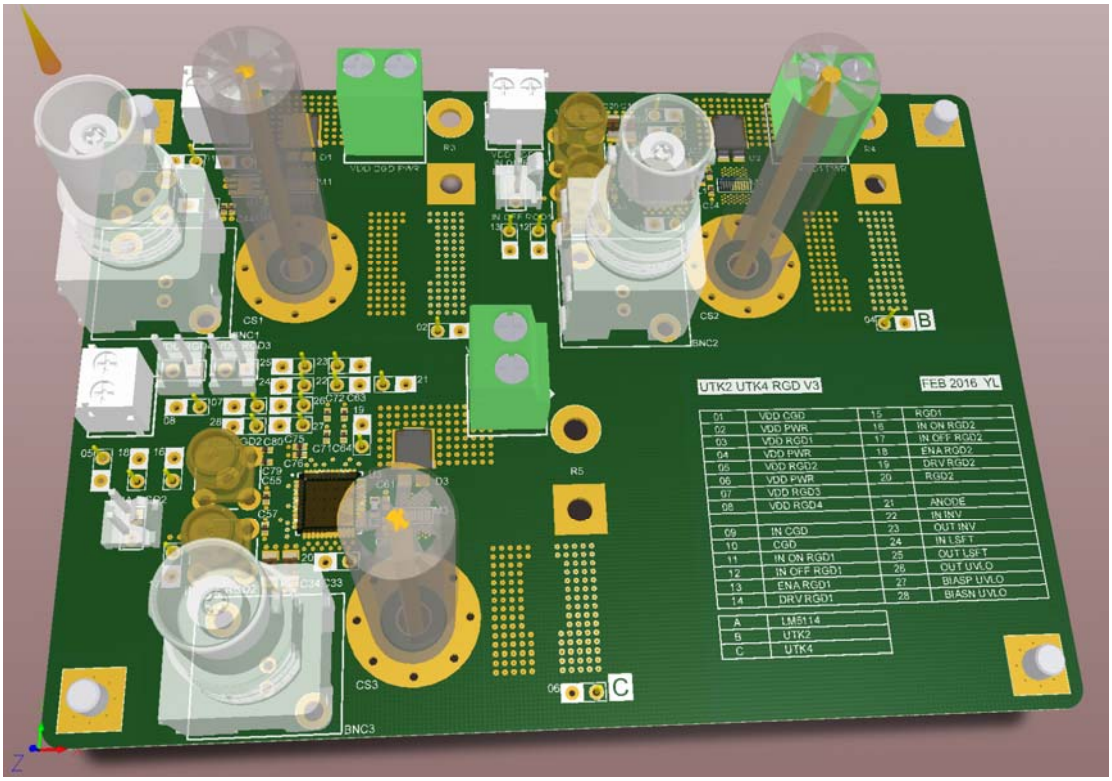


Figure A.4. 3D view of the testing PCB.

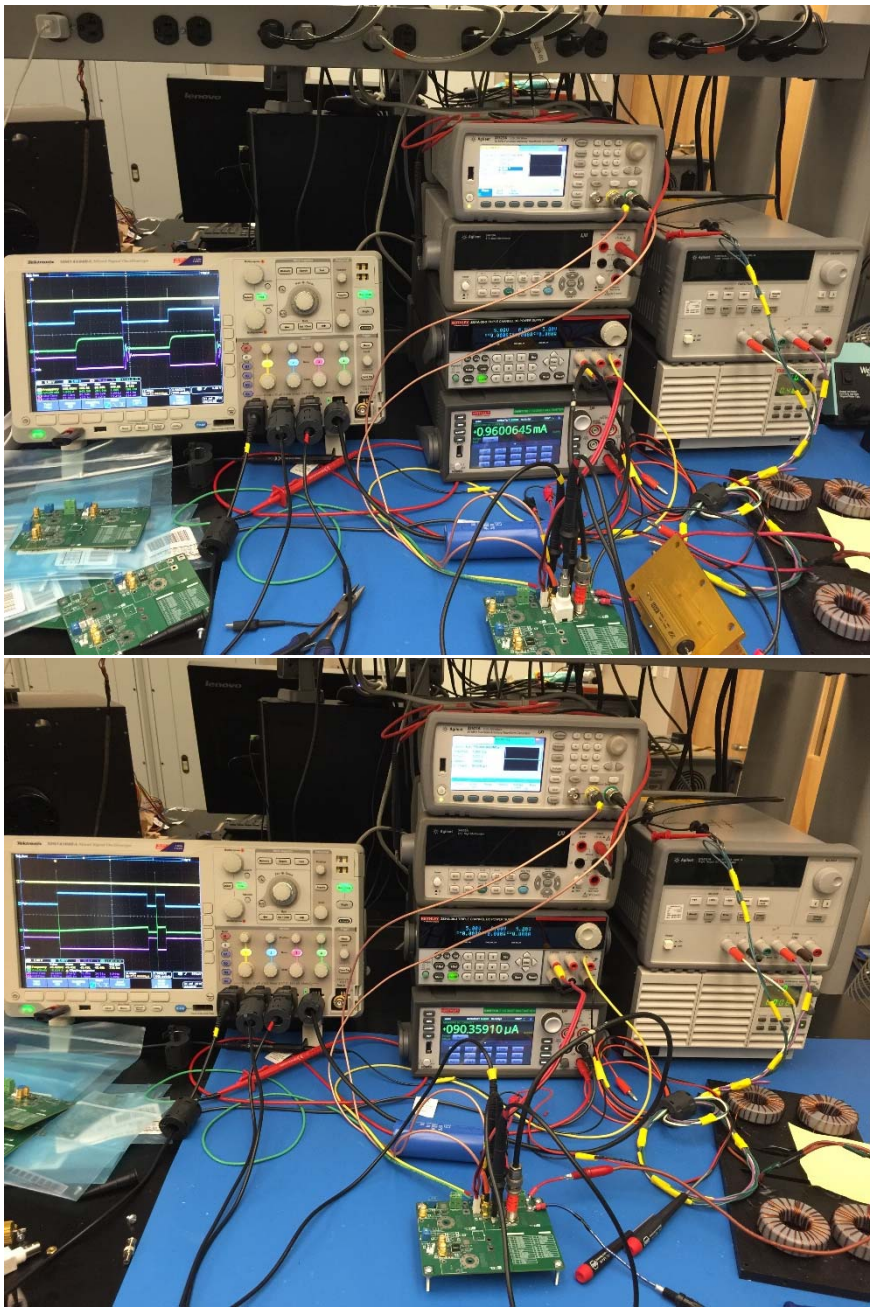


Figure A.5. Test bench setup for resistive load (top) and inductive load (bottom).

EPC Spectre model files used in design

```
// (C) Copyright Efficient Power Conversion Corporation. All rights reserved.
// ***************************************************************************
// Version History:
//              1.02: Added Copyright Statement
// Corrected by Yu Long December 2014

simulator lang=spectre

subckt epc2001 (gatein drainin sourcein)



parameters aWg=1077 A1=41.7998 k2=2.259866e+000 k3=1.2e-001 rpara=4.463059e-003
+       aITc=5.486028e-003 arTc=-4.699671e-003 ax0Tc=0.75E-4 x0_0=-0.75 x0_1=1.10
+       dgs1=4.3e-7 dgs2=2.6e-13 dgs3=.8 dgs4=.23
+       ags1=8.6952e-010 ags2=5.3168e-010 ags3=1.9975e+000 ags4=2.8377e-001
+       ags5=-1.4751e-010 ags6=-7.5163e+000 ags7=7.2121e+000
+       agd1=1.4182e-011 agd2=2.1475e-010 agd3=-3.8030e+000 agd4=5.9551e+000
+       asd1=3.3621e-010 asd2=6.3080e-010 asd3=-1.2803e+001 asd4=2.2690e+000
+       asd5=2.5818e-010 asd6=-4.0599e+001 asd7=2.0638e+001



rd (drainin drain) resistor r=(0.75*rpara*(1-arTc*(temp-25)))
rs (sourcein source) resistor r=(0.25*rpara*(1-arTc*(temp-25)))
rg (gatein gate) resistor r=(.6)

rcsdconv (drain source) resistor r=(1E9/aWg)
rcgsconv (gate source) resistor r=(1E9/aWg)
rcgdconv (gate drain) resistor r=(1E9/aWg)

gswitch drain source bsource i=( (v(drain,source)>0) ?
+       (A1*(1-aITc*(temp-25))*log(1.0+exp((v(gate,source)-k2)/k3))*
+       v(drain,source)/(1 + max((x0_0+x0_1*v(gate,source))/(1+ax0Tc*(temp-25)*(temp-25)),0.5)*v(drain,source)) ) :
+       (-A1*(1-aITc*(temp-25))*log(1.0+exp((v(gate,drain)-k2)/k3))*
+       v(source,drain)/(1 + max((x0_0+x0_1*v(gate,drain))/(1+ax0Tc*(temp-25)*(temp-25)),0.5)*v(source,drain)) ) )

ggsdiode gate source bsource i=( (v(gate,source)>10) ?
+       (0.5*aWg/1077*(dgs1*(exp((10.0)/dgs3)-1)+dgs2*(exp((10.0)/dgs4)-1))) :
+       (0.5*aWg/1077*(dgs1*(exp((v(gate,source))/dgs3)-1)+dgs2*(exp((v(gate,source))/dgs4)-1)))    )

ggddiode gate drain bsource i=( (v(gate,drain)>10) ?
+       (0.5*aWg/1077*(dgs1*(exp((10.0)/dgs3)-1)+dgs2*(exp((10.0)/dgs4)-1))) :
```

```
+       (0.5*aWg/1077*(dgs1*(exp((v(gate,drain))/dgs3)-1)+dgs2*(exp((v(gate,drain))/dgs4)-1))) )


C_GS    (gate source) bsource c=(ags1)
G_CGS1 (gate source) bsource q=(0.5*ags2*ags4*log(1+exp((v(gate,source)-ags3)/ags4))+
+       ags5*ags7*log(1+exp((v(source,drain)-ags6)/ags7)) )

C_GD    (gate drain) bsource c=(agd1)
G_CGD1 (gate drain) bsource q=(0.5*ags2*ags4*log(1+exp((v(gate,drain)-ags3)/ags4))+
+       agd2*agd4*log(1+exp((v(gate,drain)-agd3)/agd4)) )

C_SD    (source drain) bsource c=(asd1)
G_CSD1 (source drain) bsource q=(asd2*asd4*log(1+exp((v(source,drain)-asd3)/asd4))+
+       asd5*asd7*log(1+exp((v(source,drain)-asd6)/asd7)) )


ends epc2001
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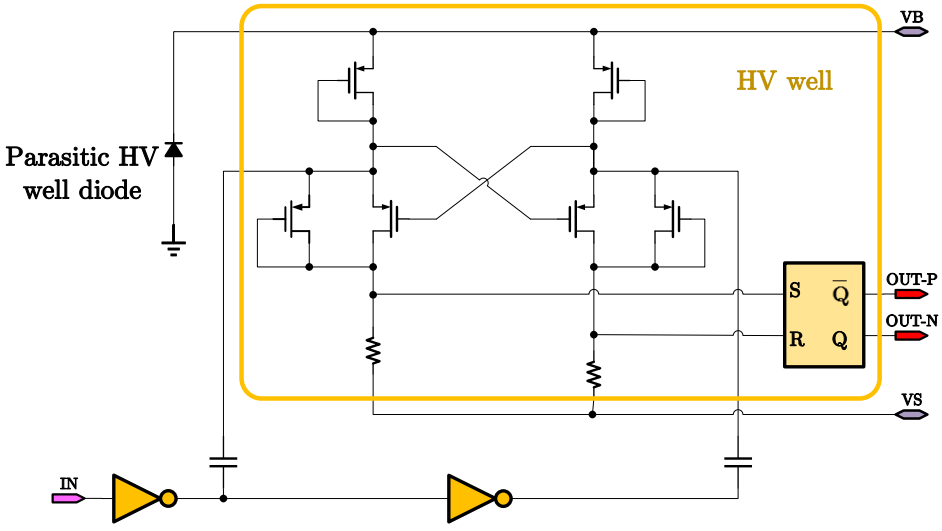


Figure A.6. Schematic diagram of the proposed capacitor coupled level shifter circuit.

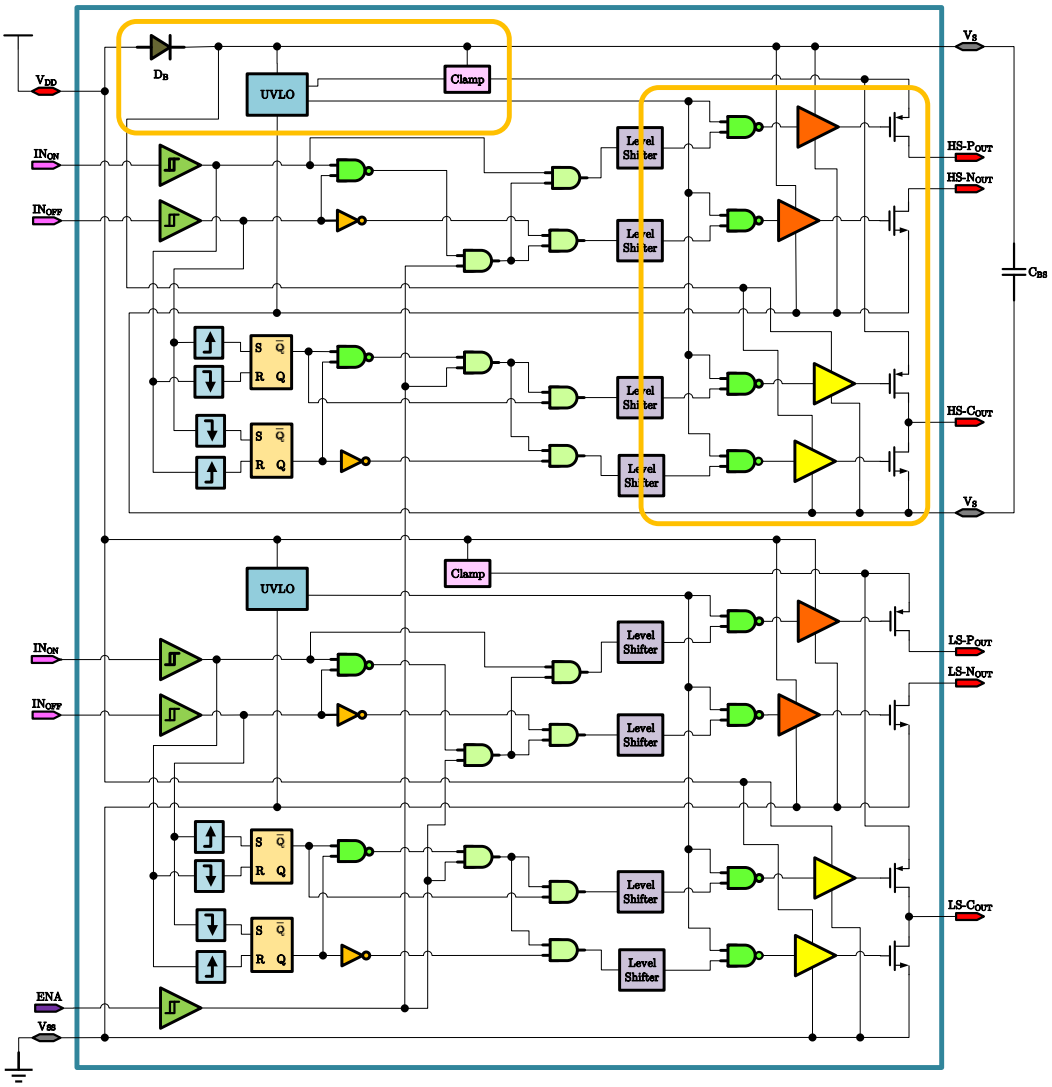


Figure A.7. Schematic block diagram of the proposed half bridge resonant gate driver, yellow ring represents high-voltage isolation well (high-side supply clamping D_B under investigation).

Vita

Yu Long received the B.E. degree in Electro-Mechanics from Chongqing Institute of Technology and the M.S. degree in applied physics from University of Science and Technology of China and then worked as a Communication engineer in China. He received the M.S. degree in electrical engineering from Virginia Tech in 2005. He is currently working toward the Ph.D. degree at the University of Tennessee in the Integrated Circuit and System Laboratory (ICASL), supervised by Dr. Benjamin Blalock. His research currently focuses on resonant gate driver IC design, on-chip isolated power supply and power management integrated circuit design for wide-bandgap power applications.