Low-Noise Micro-Power Amplifiers for Biosignal Acquisition

A Dissertation Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

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August 2016

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Acknowledgements

It has been almost six years since I came to UT for Ph.D. studies. Without insightful guidance and generous help from a great many people, I could never confidently reach the finish line. I owe my gratitude to all those people who have made this happen.

My deepest gratitude is to my advisor, Prof. Jeremy Holleman, who offered me the opportunity to work with him on interesting topics in low-power analog/mixed-signal integrated circuits design. I greatly appreciate him for being patient and considerate. Before came to United States, I was a microwave engineer, working on board-level microwave circuits design. I was initially lost in the transistor sea of integrated circuits design. However, Jeremy was very patient to share his exceptional knowledge in this field and helped me to gradually gain confidence. Jeremy also taught me how to question thoughts and express ideas. Without his encouragements and guidance, I could never make this dissertation possible.

I am also very grateful to Prof. Syed Islam, Prof. Benjamin J. Blalock and Prof. Jim Hall for serving as my Ph.D. committee members. Their helpful feedback and valuable suggestions helped to improve the readability and organization of this dissertation.

It has been a privilege and an extraordinary pleasure to work with a group of talented individuals at Integrated Silicon Systems Lab (ISS): Junjie Lu, M. Shahriar Jahan, Mohsen Judy, Kelly Griffin, Jeremy Langford, Arnab Baruah, David Basford, Nicholas Poore, Brian Coghlan, Trevor Watson, Peixing Liu, Md Munir Hasan, and Maxx Robinson. We've been through tough tapeouts together and I wish you all the best. In particular, I

would like to thank Junjie Lu for valuable technical discussions. I would also like to thank members of AVDL, ICASL and MLab groups: Kai Zhu, Song Yuan, Liang Zuo, Jinlong Gu, Terence Randall, Khandaker Mamun, Hanfeng Wang, Yu Long, Ifana Mahbub, Farhan Quaiyum, Kyle Harris, Habib Hem, Jeff Dix, Madeline Threatt and Chris Crowder. I truly hope our paths will cross sometime in the future.

I am also grateful to dear staff members of EECS department for their various forms of support during my Ph.D. studies: Dana Bryson, Kimberly Cox, Melanie Kelly, Christine Murrell, Linda Robinson, Sonja Hill, William Rhodes, Markus Iturriaga Woelfel, and Bryan Burke.

Last but certainly not least, I am deeply indebted to my entire family for their unconditional love and enduring support. I would not be where I am today if it were not for the love and support of my parents, Zhaoli Yang and Lixian He, and my wife, Yating Dong. Special thanks go to my brothers, Nan Yang and Shan Yang, for all their unconditional love and encouragement.

Abstract

There are many different types of biopotential signals, such as action potentials (APs), local field potentials (LFPs), electromyography (EMG), electrocardiogram (ECG), electroencephalogram (EEG), etc. Nerve action potentials play an important role for the analysis of human cognition, such as perception, memory, language, emotions, and motor control. EMGs provide vital information about the patients which allow clinicians to diagnose and treat many neuromuscular diseases, which could result in muscle paralysis, motor problems, etc. EEGs is critical in diagnosing epilepsy, sleep disorders, as well as brain tumors.

Biopotential signals are very weak, which requires the biopotential amplifier to exhibit low input-referred noise. For example, EEGs have amplitudes from 1 μV [microvolt] to 100 μV [microvolt] with much of the energy in the sub-Hz [hertz] to 100 Hz [hertz] band. APs have amplitudes up to 500 μV [microvolt] with much of the energy in the 100 Hz [hertz] to 7 kHz [hertz] band. In wearable/implantable systems, the low-power operation of the biopotential amplifier is critical to avoid thermal damage to surrounding tissues, preserve long battery life, and enable wirelessly-delivered or harvested energy supply. For an ideal thermal-noise-limited amplifier, the amplifier power is inversely proportional to the input-referred noise of the amplifier. Therefore, there is a noise-power trade-off which must be well-balanced by the designers.

In this work I propose novel amplifier topologies, which are able to significantly improve the noise-power efficiency by increasing the effective transconductance at a given

current. In order to reject the DC offsets generated at the tissue-electrode interface, energy-efficient techniques are employed to create a low-frequency high-pass cutoff. The noise contribution of the high-pass cutoff circuitry is minimized by using power-efficient configurations, and optimizing the biasing and dimension of the devices. Sufficient common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) are achieved to suppress common-mode interferences and power supply noises. The design are fabricated in standard CMOS processes. The amplifiers' performance are measured on the bench, and also demonstrated with biopotential recordings.

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Chapter 1

Introduction and Background

1.1 Introduction to Biomedical Signals

Generally speaking, biomedical signals can be classified into two types: endogenous signals and exogenous ones [1]. Endogenous signals such as electrocardiograms (ECG), (electroencephalograms) EEG, which arise from natural physiological processes, are obtained within or on living creatures through electrodes. Exogenous signals such as X-rays, monochromatic light, optical coherence tomography (OCT) are applied externally to detect internal structures and parameters of the objects. Almost all endogenous bioelectric signals are caused by the transient changes of transmembrane potential in living cells, particularly in nerve cells, and in muscle cells, including the heart. The endogenous biomedical signals have bandwidths generally from sub-hertz up to 10 kHz at the high end. All bioelectric signals have background noise, because they are recorded in the company of broadband noise arising from nearby physiological sources.

1.1.1 Nerve Action Potentials

Neurons are the basic information processing units in central nervous system (CNS) [2]. A neuron receives “input information” from other neurons, processes that information, and then sends that processed information as “output” to other neurons. Therefore, neurons

process all kinds of information through which we are able to move, to see, to hear, to taste, to smell, to think, and to remember. In the nerve cell membrane, the transient changes of specific ionic conductances and permeabilities generate nerve action potentials (spikes) [1]. In order to achieve long-distance and rapid communication, neurons send action potentials along axons, which is called conduction mechanism. In neurons, the action potentials play a primary role in cell-to-cell communication [3]. With extracellular metal microelectrodes, the nerve action potentials could be recorded over long periods of time. However, the extracellular recording techniques suffer from the problem that the nerve spikes from adjacent neurons are picked up by the electrodes. Unfortunately, this resulted background noise has the same bandwidth as the desired spikes, and is added to the interesting unit's signal. In order to significantly improve the recording signal-to-noise ratio (SNR), it might be possible to isolate single axons with hook or suction electrodes in dissected peripheral nerve fibers. By using fine platinum-iridium extracellular microelectrodes, it might be possible to make recording from single units in insect optic lobes, with major spike amplitudes ranging from 50 to 500 μV [1].

1.1.2 Muscle Action Potentials

The muscle action potentials arise from the depolarization of the muscle cell membrane [3]. In normal skeletal muscle cells, the action potentials are similar to the ones in nerve cells. Muscle action potentials such as electromyogram (EMG) could be recorded on the skin surface with electrodes. By using needle electrodes which pierce into a superficial muscle, it is possible to make recording from single motor units (SMUs) or individual muscle fibers. These EMGs are very important in diagnosing many

neuromuscular diseases, which could result in muscle weakness or paralysis, motor problems, and motor nerve damage.

1.1.3 Other Bioelectric Signals

Electrocardiogram (ECG or EKG) results from the polarization and depolarization of cardiac tissue [4]. The amplitude and wave-shape of the ECG is dependent on the electrodes' location on the skin surface. The recording of ECGs is very important in medical diagnosis and patient care. It can give information regarding the rhythm of the heart, the presence of any damage to the heart, as well as the effects of devices used to regulate the heart. The ECG testing is critical when a heart attack is suspected. The amplitudes of ECG QRS spikes are dependent on the recording site and the patient's body type, which can range from a 400 μV to 2.5 mV at peak [1].

Electroencephalogram (EEG) arises from ionic current flows within the neurons of the brain [5], [6]. The EEGs reflect the summation of the synchronous activity of a large number of neurons which have similar spatial orientation, because it is far too small to pick up the bioelectric potential generated by an individual neuron. The EEGs are frequently used in diagnosing epilepsy, sleep disorders, coma, brain death, as well as brain tumors and stroke [7]. The typical EEG potentials recorded on the scalp are no more than 150 μV at peak [1]. In order to localize sites of EEG activities on the brain's surface, the multi-electrode recording technique is used. Traditionally, EEGs have been classified into four frequency band [1]:

- Delta waves, which occur in adults in deep sleep, have the largest amplitudes and lowest frequencies (<4 Hz).
- Theta waves, which are seen in young children and in drowsiness in adults, have

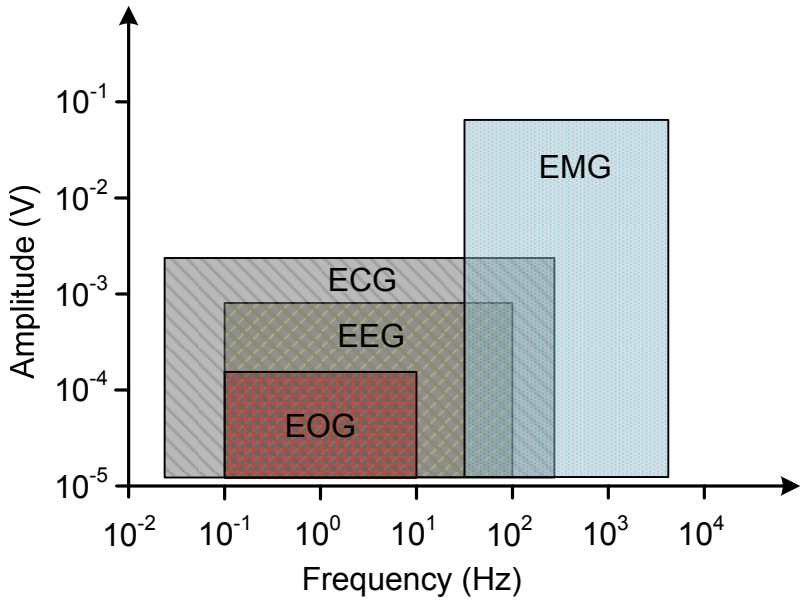


Fig. 1.1. Approximate extreme ranges of peak-signal amplitudes and approximate frequency bands of four class bioelectric signals [1].

large amplitudes and low frequencies (4 to 7 Hz).

- Alpha waves, which are recorded from adults who are conscious but relaxed with the eyes closed, lie in the frequencies of 8 to 13 Hz and amplitudes of 20 to 200 μV.
- Beta waves, having the frequency band from 13 to 50 Hz, are most easily found in the parietal and frontal regions of the scalp.

The other bioelectric signals like electroretinogram (ERG), electrooculogram (EOG), and electrocochleogram (ECoG) have low amplitude (hundreds of microvolts at peak) and contain primarily low frequencies (0.01 to 100 Hz) [1]. The recordings of these bio-potentials are for diagnostic and research purposes, and are usually accompanied by undesired noise from EMGs and the electrodes. Fig. 1.1 shows the approximate extreme

Table I. Popular Recording Techniques for Bioelectric Signals.

Recording Techniques	Description
Patch clamp technique	Recording current flow from single ion channel of an individual neuron.
Intra-cellular recording	Recording from the inside of an individual neuron.
Extra-cellular recording	Recording from the outside of an individual or a few neuron(s).
Mass unit recording	Recording from the outside of a group of neurons.

ranges of peak-signal amplitudes and approximate frequency range of EOGs, EEGs, ECGs, and EMGs signals.

1.2 Introduction to Bioelectrodes

In order to record bio-potentials, bioelectrodes are needed between bio-potential amplifiers and the "wet" environment of living creatures. The size of bioelectrodes range from microscopic intra-cellular research electrodes to large defibrillation paddles [8]. Most bioelectrodes are made of metal, but the microscopic intra-cellular research electrodes are glass capillary tubes filled with a conductive saline solution. Table I lists some popular recording techniques for bioelectric signals.

When designing a biopotential acquisition system, it is important to know the equivalent circuit that exists between the electrode terminals. Without such an equivalent model, it is difficult to specify the input impedance of the bio-potential amplifiers [9]. Each electrode can be modeled by a parallel RC circuit in series with a resistor. In general, since both resistors in the electrode model contribute thermal noise, it is desirable that the

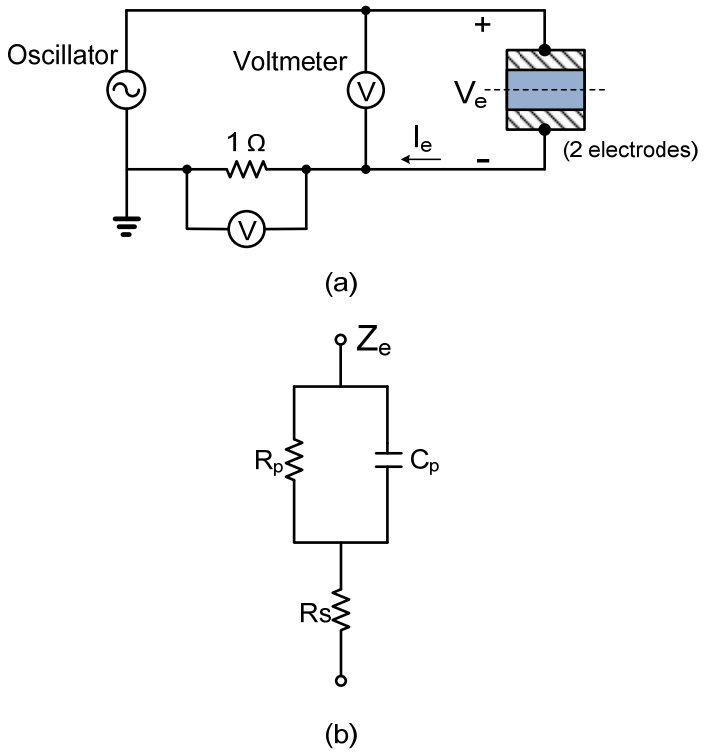


Fig. 1.2. (a) Impedance magnitude measurement circuit for the bioelectrodes. (b) Linear equivalent circuit for one electrode [1].

impedance of the electrode should be made as small as possible. Fig. 1.2 (a) shows the impedance magnitude measurement circuit for the bioelectrodes. The linear equivalent circuit for one electrode is shown in Fig. 1.2 (b). In the measurement of a bioelectric event, the biopotential amplifier must have an input impedance much larger than the impedance of the bioelectrodes. Otherwise, it may not only result in obtaining an attenuated amplitude for a bioelectric event but also may lead to serious waveform distortion [9]. Clinically, the distortion in waveform of bioelectric event may cause misguided diagnosis.

1.3 Research Motivation

There is a rapid development of multi-channel implantable integrated biopotential recording systems, which allow simultaneous recording and stimulation at multiple sites in

the brain and the body [10]. Implanted deep in the brain, the electrodes convey both high-frequency nerve action potentials (spikes), and low-frequency local field potentials (LFPs).

Placed noninvasively on the scalp or on the cortical surface, the electrodes convey brain signals known as EEG and ECoG, respectively. Fig. 1.3 shows the typical block diagram of the integrated implantable biopotential recording system. In the recording systems, the biopotential amplifier (BPA) is one of the key elements. It senses and amplifies the bioelectric signals such as action potentials, EEGs, ECGs etc., through electrode-tissue interfaces. The biopotential from the desired channel is selected by MUX, and is converted to digital waveform by ADC. The digitized signal is further processed by DSP block, and then transmitted wirelessly through the telemetry block (Tx and Rx in Fig.

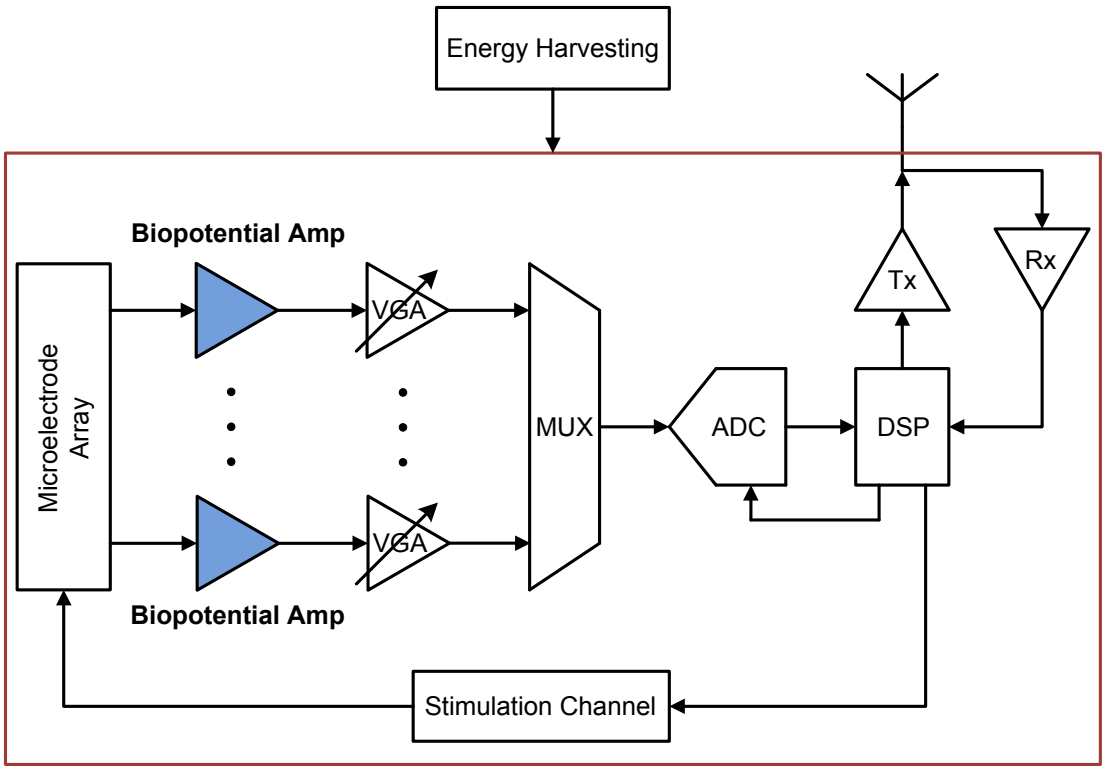


Fig. 1.3. Block diagram of the integrated implantable biopotential recording system.

1.3). The wireless telemetry block can also receive stimulation waveform data for the stimulation channel.

Monolithic amplifiers have been used for biopotential recording for decades [11], [12]. However, the large time constants inherent in the amplifier dynamics typically preclude timesharing of a single amplifier among multiple electrodes [13]. For multi-channel recording applications, a large number of BPAs (on the order of 100-1000, one per active electrode), are incorporated in the recording systems, which puts power constraints on BPA design. Firstly, the power consumption per BPA should be minimized to avoid excessive heat dissipation which may cause cell damage or death in the surrounding tissues [14], [15]. The precise limits to power dissipation can be difficult to establish. Typically, the maximum temperature increase due to the operation of the cortical implant in any surrounding tissue should be kept at less than 1°C [16]. Therefore, the power limits are determined by the dimension and shape of the implantable recording systems. For example, preliminary experiments have shown that an implanted cortical 100-electrode array with integrated electronics (rough dimension of 6mm by 6mm by 2mm) can dissipate approximately 10 mW of power in safe usage [17], [18]. With modern MEMS arrays having approximately 100 electrodes and a 10 mW power dissipation limit on the recording systems, a rough estimation shows that each channel must consume power less than 100 μW. Considering the power budget for the shared blocks on a chip such as ADC, power supply regulation, DSP, and wireless telemetry circuitry, the power limit on each BPA should be even less. For implantable recording systems with battery operation, low-power consumption could prolong the time between recharges, thus expanding the battery's life

to avoid frequent surgeries for battery replacement. If the recording systems are sufficiently ultra-low power, it might be possible for the battery to be partially or completely replaced by a radio-frequency identification (RFID) power extraction system [19] or by other forms of energy harvesting, such as body vibration [20] or body heat [21].

Since the bioelectric signals can be very weak, the input-referred noise of the BPAs has to be minimized to achieve a large dynamic range. For example, depending on distance between the active neuron and the recording electrode, typical extracellular action potentials have amplitudes up to 500 μV with much of the signal energy in the 100 Hz-7 kHz band. LFPs have amplitudes as high as 1 mV and contain signal energy from sub-Hz up to 200 Hz [22]-[24]. The input-referred noise of the BPA should be lower than the typical extracellular neural background noise of 5-10 μV_{rms} to get clean neural signal recordings [25]. For an ideal thermal-noise-limited BPA with a constant bandwidth and supply voltage, assuming that the BPA is CMOS based and all the transistors are biased in weak inversion region, power consumption of the BPA is inversely proportional to v_{ni}^2 where v_{ni} is the input-referred noise of the BPA. Therefore, there exists a trade-off between low-noise and low-power which must be well-balanced by the designers.

The BPAs should be able to adequately reject the large dc offsets present at the electrode-tissue interface. Placement of a metallic electrode in the tissue results in charge distribution, and creating a capacitive double-layer which can cause significant polarization voltages [26]. Since the BPAs are designed to be high gain (40 - 80 dB) to provide sufficient amplification for the weak biopotentials and are powered by low supply voltage to achieve low-power operation, the input offsets that can reach hundreds of millivolts would easily

saturate the BPAs. Therefore, the BPAs need to be able to reject large dc offsets without compromising the information-bearing low-frequency components of the biopotentials. Moreover, another key requirement for the BPAs design is to avoid corrosion of the electrodes that may cause cytotoxicity. This puts a leakage current constraint at the BPAs inputs.

High common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR) is important in BPAs design. Since the signal input occurs at high impedance nodes, they often pick up a considerable amount of an interfering common-mode 60 Hz noise, which lies in the bandwidth of our interest. In order to reduce pickup of 60 Hz noise, and other capacitively- and inductively-coupled interference, the signal path between the electrodes and the BPAs should be minimized. Other non-idealities that affect the performance of the biopotential recordings are common-mode noise and interference from on-chip digital circuitry, and the supply noise from the power regulation circuitry. Fully differential configurations usually provide better CMRR and PSRR than single-ended one. However, the common-mode feedback circuits (CMFB) that required in fully differential configurations increase the power consumption and design complexity.

It is desired that the BPAs should have high input impedance. Firstly, the source impedance of the electrode interface may interact with the input impedance of the BPAs, resulting in voltage dividers or parasitic frequency corners, which may attenuate or filter out the interesting biopotentials. Besides, if the BPAs don't have an input impedance much larger than the impedance of the bioelectrodes, it may lead to serious waveform distortion of the bio-potentials [9]. Clinically, the distortion in waveform of bioelectric event may

cause misguided diagnosis. Moreover, the electrode impedance imbalance may result in degradation of CMRR and PSRR. The BPAs with high input impedance are less sensitive to electrode impedance imbalance.

The area consumed per BPA must be small such that the multi-channel recording system can be designed with a small form factor. High-density integration not only reduces fabrication cost but also minimizes surgical damage in implantation.

In summary, there are several main specifications for the BPAs design:

- Have sufficiently low input-referred noise (< 5 μV_{rms}).
- Have minimal power consumption to avoid thermal damage to surrounding tissues, preserve long-battery life, and enable wirelessly-delivered or harvested energy supply (< 100 μW).
- Have much higher input impedance than the electrode-tissue interface to avoid biopotential attenuation and distortion (typically a few MΩs at 1 kHz).
- Have negligible dc input current.
- Block dc offsets present at the electrode-tissue interface to prevent saturation of the BPAs.
- Amplify bioelectric signals in the frequency bands of interest (typically from as low as sub-Hz up to 10 kHz).
- Have sufficient dynamic range convey biopotentials (spikes or LFPs).
- Have sufficient CMRR to reject 60 Hz common-mode interference and other undesired common-mode noise, and sufficient PSRR to reject noise from power supply.

- Small silicon area to allow the integration of high-channel-count recording systems.

1.4 Original Contributions

In this work, an ultra-low-power low-noise amplifier for neural recordings and a configurable low-power analog-front end for the recordings of a variety of biopotential signals is proposed. The original contribution of this work is summarized below:

- Proposed a novel amplifier array topology with ultra-low-power low-noise operation that is suitable for large-scale integration. The topology combines a highly efficient but supply-sensitive single-ended first stage with a shared reference channel and a differential second stage to effect feed-forward supply noise cancellation, combining the low power of single-ended amplifiers with improved supply rejection. A two-channel amplifier was fabricated in a 90 nm standard CMOS process. The performance was measured on the bench, and was demonstrated with neural recordings.
- Proposed a novel chopper-stabilized telescopic-cascode amplifier with complementary-input current-reuse technique which achieves excellent noise-power efficiency.
- Proposed a tunable input impedance boost loop to maximize the impedance boost factor by compensating for process variation and parasitic capacitance.
- Proposed a pseudo-resistor based large-time constant integrator to create sub-Hz high-pass corner, which is area- and power-efficient.

- Proposed a power-efficient configurable analog front-end (AFE) for the recordings of a variety of biopotential signals. The AFE was fabricated in a 130 nm standard CMOS process. The performance was measured on the bench, and was demonstrated with biopotential recordings.

1.5 Dissertation Overview

Chapter 2 provides an overview of previous research on the design of biopotential amplifiers.

Chapter 3 describes the implementation of the amplifier array topology with ultra-low-power low-noise operation. The analysis of PSRR, CMRR, noise optimization, and noise efficiency factor (NEF) calculation is presented. The experimental results and biological recordings are presented.

Chapter 4 describes the design of a power-efficient configurable analog-front-end for the recordings of a variety of biopotential signals. The experimental results and biological recordings are presented.

Chapter 5 concludes the dissertation and proposes potential future works.

Chapter 2

Literature Review

2.1 Low-Noise Low-Power Amplifiers with Capacitive Feedback

Recently there has been a great interest in designing low-power low-noise amplifiers for bio-potential recordings [11], [27]-[38]. The oft-cited amplifier [27] presents many useful techniques for designing BPAs. The schematic of the BPA is [27] shown in Fig. 2.1, which is based around on an operational transconductance amplifier (OTA). A capacitive feedback network (C_1 and C_2) is employed to set the midband gain (C_1/C_2) of

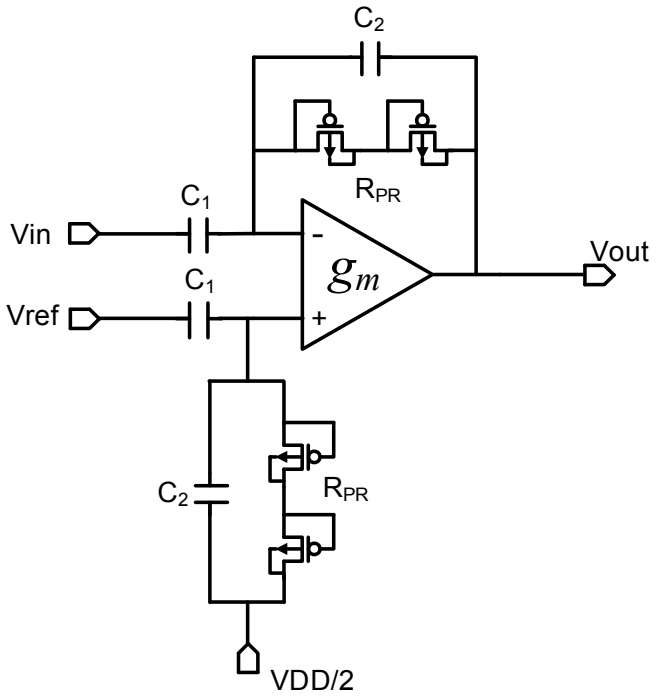


Fig. 2.1 Schematic of the BPA presented in [27]

the BPA, which offers good matching and consume no extra power. The input is AC coupled, so any dc offset generated at the electrode-tissue interface is rejected. MOS-bipolar elements [39] called pseudo-resistors are used to set the DC feedback and the low-frequency amplifier cutoff, which provides an area-efficient means of creating a huge small-signal resistance (>10^{12} Ω) for low-frequency operation. The low-frequency cutoff is given by $1/(2r_{inc}C_2)$, where r_{inc} is the small-signal resistance of the pseudo-resistors. The BPA reported in [27] employs the current-mirror OTA, which achieves high output swing at the cost of having additional current branches. The schematic of the current-mirror OTA is shown in Fig. 2.2. It is not noise-power efficient, because it has more noise contributions from the active MOS loads and more current branches. The BPA [27] consumes 80 μW to achieve low input-referred noise in the bandwidth of 7.2 kHz. In implantable multi-electrode systems, the power of 80 μW required by each neural amplifier can be a limiting factor. A two-stage OTA-based BPA [33] achieves both large gain and wide output swing with an NEF of 19.4. However, in order to ensure stability, the second stage consumes considerable current which is not power efficient. In order to reduce the output quiescent current, push-pull operation [34] has been added to a two-stage OTA to improve the NEF to 3.26.

The BPA [35] introduces a partial OTA sharing architecture, which improves the noise-power efficiency and reduces silicon area. The BPA achieves 3.5 μV_{rms} input-referred noise over 10 Hz to 7.2 kHz with a corresponding NEF of 3.35, while consuming 4.4 μA from 1.8 V supply. However, a systematic mismatch existing from one channel to another degrades the channel crosstalk performance. Moreover, in order to avoid the

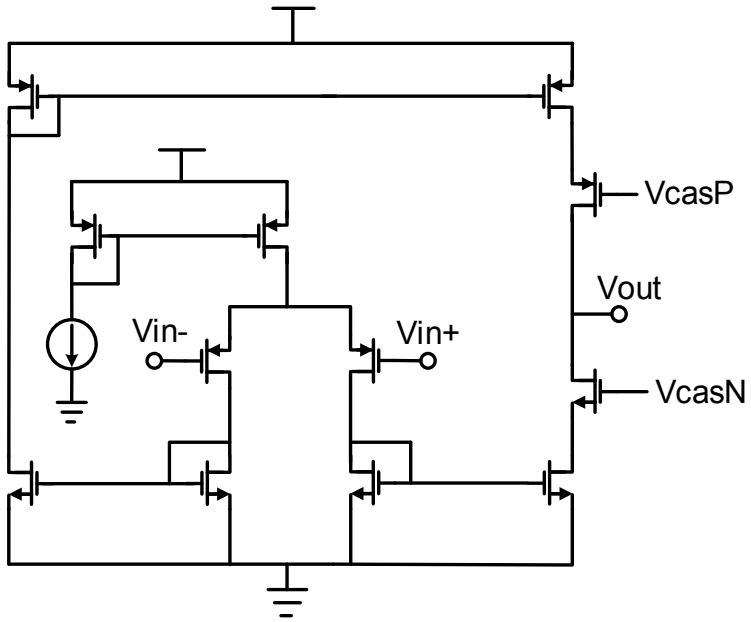


Fig. 2.2 Schematic of the OTA used in [27].

excessive degradation of the common-mode rejection ratio (CMRR) and channel crosstalk, the complexity of the circuit layout significantly increases as the number of channels increases. Thus, this sharing technique is not suitable for large-channel-count integration.

Fully-differential BPAs [36], [37] employ the folded-cascode OTA instead of current-mirror one [27]. Compared with current-mirror OTA, the folded-cascode OTA is more noise-power efficient, because it has less noise sources. However, folded-cascode OTA provides less output swing than current-mirror OTA. Since the input bio-potentials are very week (up to a few mV), the large output swing feature is not necessary. While the BPA [37] achieving 3.6 μV_{rms} input-referred noise over 20 Hz to 10 kHz, the current consumption is 8 μA at ±1.7 V. To further improve the noise-power efficiency, the modified folded-cascode topologies have been reported in [28], [29], [38].

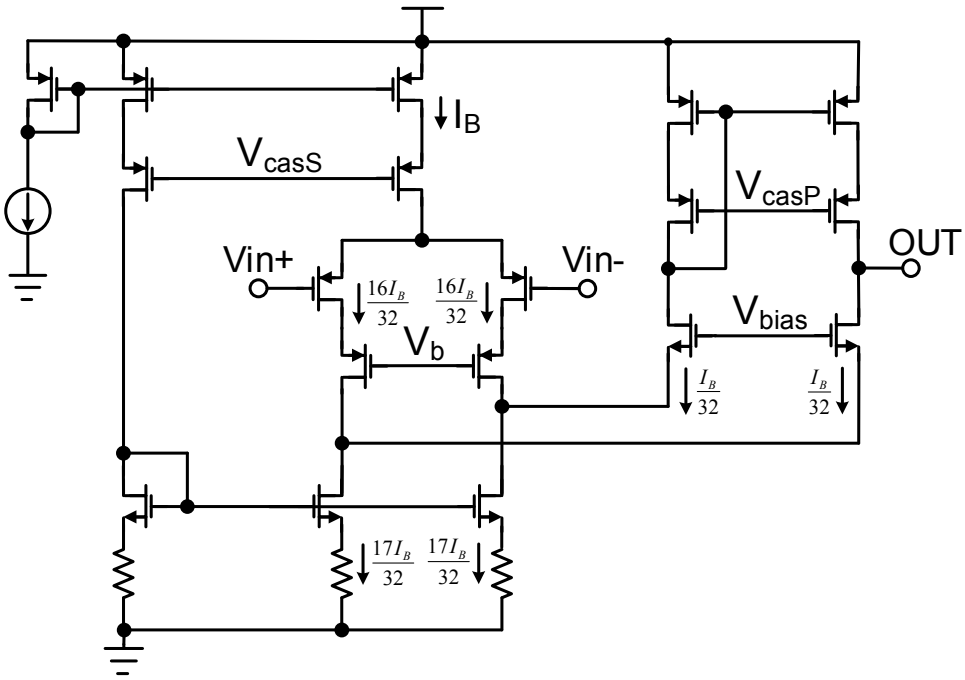


Fig. 2.3. Schematic of the folded-cascode OTA in [28].

The BPAs presented in [28], [38] employ current scaling technique to reduce the current consumption from the folded branches. The schematic of the current-scaling OTA is shown in Fig. 2.3. Although current scaling technique significantly increases the noise-power efficiency, such severe current scaling increases the impedance looking into the source of the output transistors which could significantly degrade the effective transconductance of the OTA. In order to avoid the problem, cascode transistors are added to boost the output impedance of the input pair, which requires more headroom. In addition, large source degeneration resistors are used to minimize the noise contribution and increase the output impedance of the MOS active loads at the cost of large headroom and silicon area. The BPA [28] achieves 3.06 μV_{rms} input-referred noise with a corresponding NEF of 2.67 over 45 Hz to 5.32 kHz, while consuming 2.7 μA from a 2.8V supply.

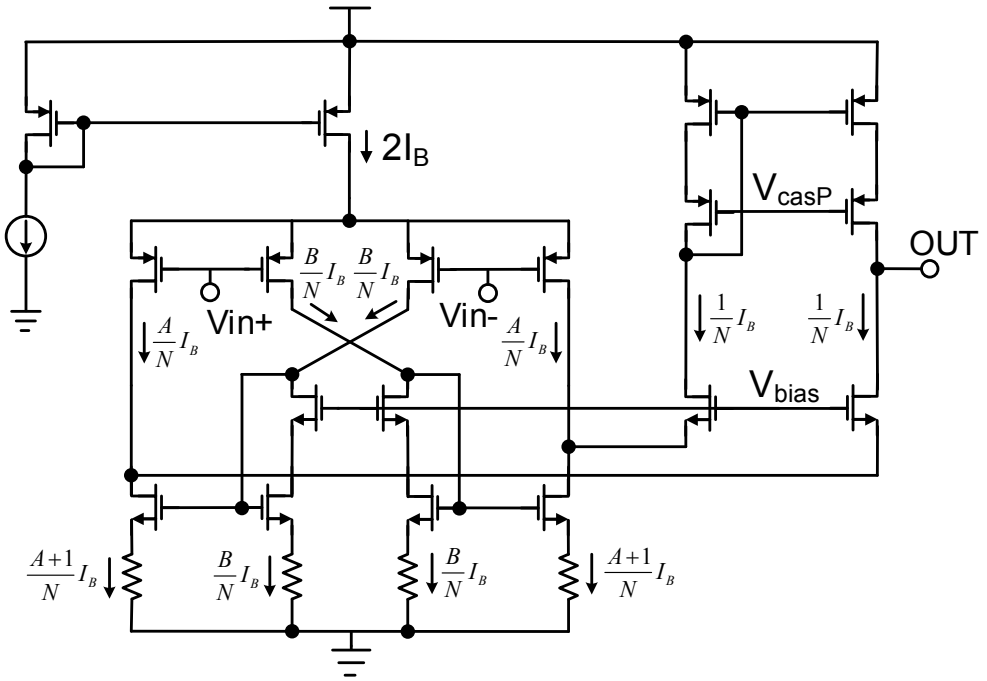


Fig. 2.4. Schematic of the folded-cascode OTA in [29].

The BPA [29] employs the current scaling technique [28] to minimize the current consumption and a current splitting technique [40] to increase the drain resistances of both input transistors and current-sinking transistors. The schematic of the OTA is shown in Fig. 2.4. The BPA [29] achieves 3.07 μV_{rms} input-referred noise with a corresponding NEF of 3.09 over 0.36 Hz to 1.3 kHz, while consuming 0.872 μA from a 2.8V supply. However, for both BPAs [28] and [29], the current errors caused by large-scale mirroring must be well-controlled. Otherwise, the severe current scaling scheme between the input differential pairs and the folded-branches will not work. Besides, the large source degeneration resistors which are used to minimize the noise contribution from the active loads increase the chip area and the voltage head-room, which makes the BPAs not suitable for low supply operation.

An open-loop single-ended amplifier with complementary–input current-reuse [30] was introduced. The schematic of the amplifier is shown in Fig. 2.5. The complementary-input current-reuse technique drives the gates of both complementary-input transistors, which doubles the effective transconductance of the amplifier. Due to the employment of complementary-input current-reuse technique and the single current branch, the BPA [30] is extremely power-efficient for a given noise and bandwidth. However, the single-ended topology features poor power supply rejection ratio (PSRR) and open-loop configuration leads to imprecise gain control. The BPA reported in [30] exhibits 3.5 μV_{rms} input-referred noise with an excellent NEF of 1.8 over 0.3 Hz to 4.7 kHz while consuming only 805 nA current from a 1V supply, at the expense of poor PSRR of 5.5 dB and total harmonic distortion (THD) of 7.1% at $1mV_{pp}$ input. Because of the poor PSRR, ultra-low noise voltage regulation circuitry is needed, which consumes additional power and potentially increase the design complexity. Besides, for neural recording applications, sufficient

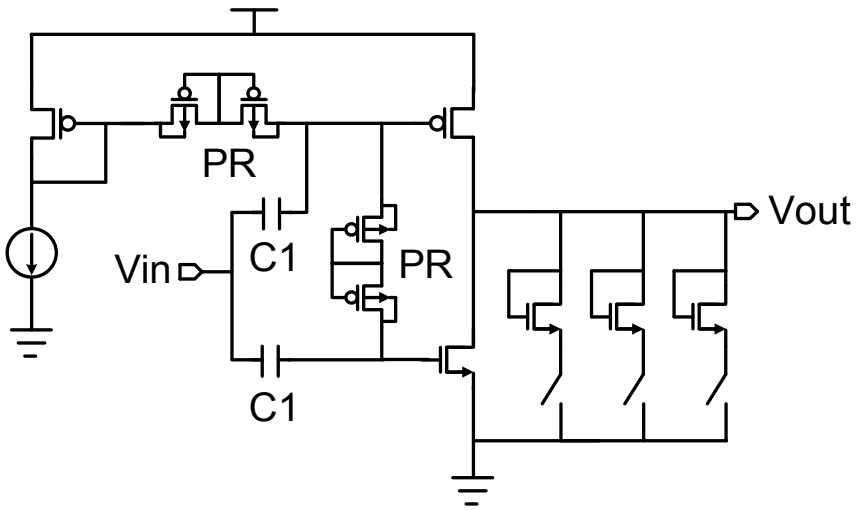


Fig. 2.5. Schematic of the open-loop single-ended amplifier in [30].

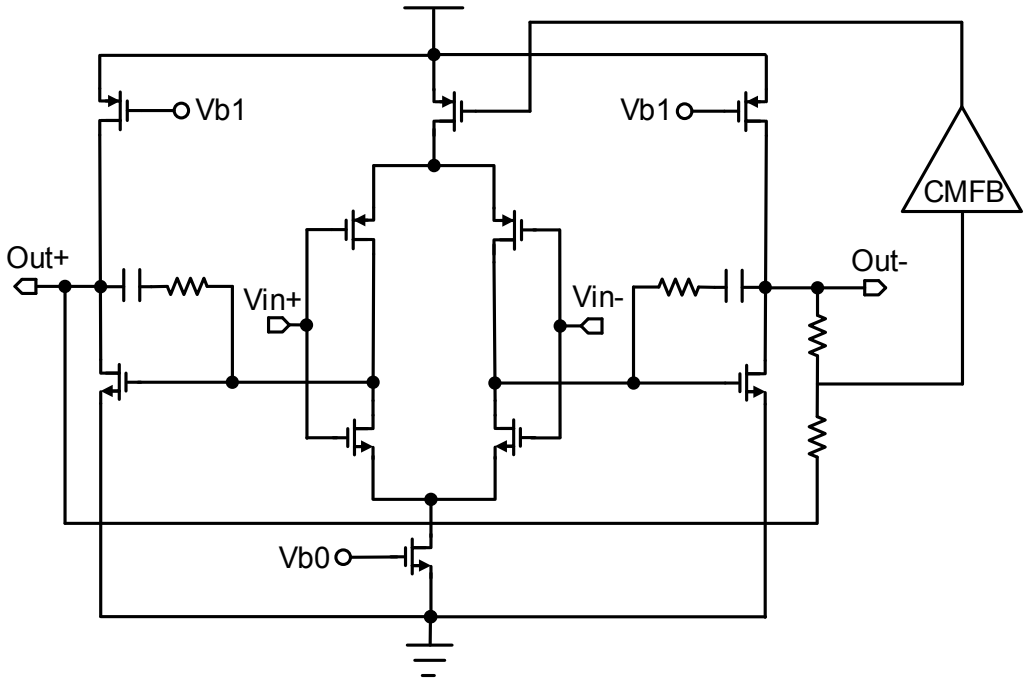


Fig. 2.6. Schematic of the closed-loop two-stage fully-differential amplifier in [31].

CMRR is also required to suppress the common-mode noise and interference from on-chip digital circuitry or other noise sources.

Recently, a closed-loop two-stage fully-differential complementary-input current-reuse amplifier has been presented in [31], in which the PSRR is greatly improved by using the differential-input configuration. The schematic of the amplifier is shown in Fig. 2.6. However, at a given power budget, the input-referred thermal noise power of the differential-input configuration is twice that of the single-ended amplifier [30] because the output noise was doubled by the differential branches, which significantly degraded the noise-power efficiency. In addition, the second stage needs to consume considerable power to ensure the stability. The BPA in [31] achieves the input-referred noise of 2.2 μVrms

with a corresponding NEF of 2.9 over 0.05 Hz to 10.5 kHz, while consuming 12.1 μA current from a 1V supply.

2.2 Chopper-Stabilized Low-Noise Amplifiers

The previous section discussed the design of energy-efficient BPAs based on capacitive feedback configuration [27]. Because bio-potentials have a bandwidth up to a few kHz, a few strategies are used to minimize the flicker noise of the CMOS transistors. Firstly, because flicker noise in PMOS transistors is typically one to two orders of magnitude lower than flicker noise in NMOS transistors, PMOS transistors are used as the input pair [41]. Secondly, the flicker noise is minimized by sizing the transistors with large gate area [42]. Lastly, the input-pair transistors are biased in the subthreshold regime to minimize the noise contribution from the active loads [27]. Some low-frequency bio-potentials like EEG are very weak (1~100 μV, sub-Hz to 100 Hz), so the BPAs needs to have excellent noise performance at low frequencies. However, since the total input-referred noise of the capacitive-feedback amplifier increases as the parasitic capacitance of the input transistors increases [27], it's not very efficient to suppress the low-frequency noise by simply sizing the transistors with large gate area. Besides, large-size transistors are not area-efficient.

To effectively minimize the low frequency noise like flicker noise (*1/f* noise) and popcorn noise, the auto-zero (AZ) and chopper stabilization (CHS) techniques can be used [43]. The basic principle of the auto-zero is sampling the undesired quantity (noise and offset) and then subtracting it from the contaminated signal either at the input or the output

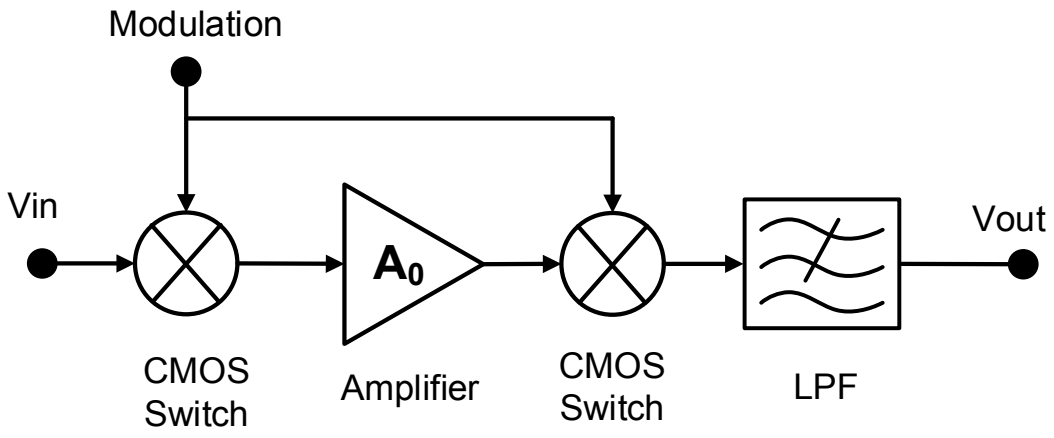


Fig. 2.7. Configuration of the typical chopper stabilized technique.

of the op-amp. Since auto-zero is a sampling process, the wideband is aliased down to the baseband, increasing the noise floor.

Unlike the auto-zero process, the chopper stabilized technique employs modulation to transpose the signal to a higher frequency where there is little *1/f* noise, and then demodulates it back to the baseband after amplification, and thus achieves superior low-frequency noise performance. The typical chopping principle is shown in Fig. 2.7. At the input, a CMOS-based switch modulator shifts the input signal to a higher frequency. The choice of the modulation frequency is set by the amplifier's excess noise. Usually, the modulation frequency should be higher than the *1/f* noise corner [43]. After the amplification, the modulated signal is translated back to baseband by a second demodulator, and the low-frequency noise (*1/f* noise, offset) is shifted up to modulation frequency. The following low-pass filter suppresses the up-modulated offsets and *1/f* noise from the amplifier output. Chopper stabilized technique is usually preferred over the auto-zero, because it is efficient in suppressing low frequency noise with minimal signal or noise

aliasing. However, this is at the cost of significant ripple at the amplifier output, due to the up-modulated offset and *1/f* noise [43].

To suppress the chopping ripple, filters with kHz cut-off frequencies are needed. However, the filters with low cut-off frequencies usually require significant chip area. In many applications, this is undesirable and so a variety of area-efficient on-chip techniques have been reported. One on-chip technique utilize auto-zeroing technique to reduce the amplifier's initial offset [44]. However, due to the increased low-frequency noise caused by the noise folding of the auto-zeroing technique, extra power dissipation is needed to meet a given noise specification. In precision temperature measurement systems, this is a serious drawback, because in these systems self-heating needs to be minimized. By reducing the amplifier's bandwidth to a fraction of the auto-zeroing frequency, the noise folding problem caused by auto-zeroing can be mitigated [45]. However, for quasi-continuous-time operation, two auto-zeroed input stages with a ping-pong operation must be used, which doubles the power consumption. Sample-and-hold filters [46], [47] can be alternatively used to reduce the chopping ripple. However, because of the involvement of sampling, a certain noise folding problem still exists. Moreover, the extra delay caused by the sample-and-hold filter significantly increases the design complexity of the frequency compensation network. Recently, a continuous-time ripple reduction loop (RRL) [48] has been proposed to minimize the chopping ripple. The loop synchronously demodulates the amplifier's output ripple, and then drives it to zero by canceling the offset of the input stage. Due to the continuous time feature of the loop, this technique doesn't suffer from noise folding problem. However, the use of a RRL creates a notch at the chopping

frequency. This notch could be inside the signal band when the chopping frequency is low (a few kHz) to ensure high input impedance and low input bias current. In order to solve this problem, a chopped current-feedback amplifier with a low frequency path and high frequency path is proposed in [49] to bury the notch while still maintaining high precision and power efficiency.

Chopper-stabilized amplifier has residual offset mainly due to the non-idealities of the chopping modulators. For simple MOS switches, the non-idealities include clock feedthrough and charge injection. Any spikes due to the input modulator non-idealities will be amplified and demodulated back to dc by the output modulator, giving rise to a residual dc component. Since the magnitude of the chopping spikes is proportional to the chopping frequency, the residual offset can be minimized by set the chopping frequency rather low (typically in the order of a few tens of kHz). In addition, charge injections can be reduced by employing complementary switches or MOS switches with half-sized dummy transistors in the modulator [43].

Instrumentation amplifiers based on chopper-stabilization technique have been reported in [45]-[63]. Current feedback instrumentation amplifiers (CFIAs) [45], [48]-[52] feature high input impedance. However, the mismatch between their input and feedback transconductances limits the gain accuracy. Moreover, CFIAs can achieve rail sensing by employing either an NMOS or PMOS-based input differential pairs. However, it is quite challenging to achieve rail-to-rail input as well as high gain accuracy, as the mismatch between the input and feedback transconductors is usually a function of the input common-

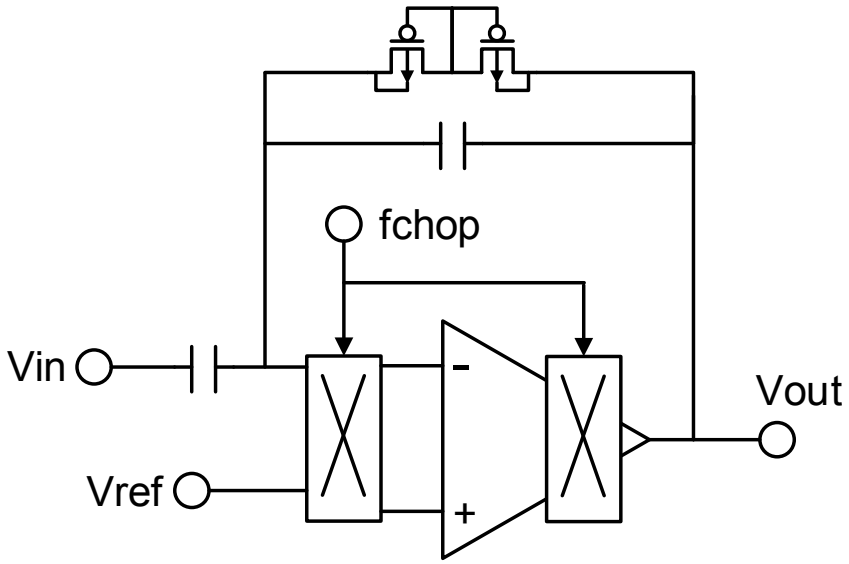


Fig. 2.8. Configuration of the CCIA in [53].

mode voltage [48]. Besides, the power efficiency of CFIAs is also limited by the need for the two input and feedback transconductances.

Capacitively-coupled chopper instrumentation amplifiers (CCIAs) have been reported in [53]-[63]. The configuration of CCIA in [53] is shown Fig. 2.8. The chopping frequency is higher than the flicker noise corner to ensure low-noise operation. Capacitive feedback is used instead of resistive feedback to avoid extra power dissipation and adding additional noise. Besides, a resistive feedback network may degrade the closed-loop gain by loading the output stage. Increasing the resistance of the feedback network leads to larger chip area and worse noise performance. The mid-band gain is defined by C_{in}/C_{fb}. Compared with CFIAs, CCIAs have several advantages. Firstly, CCIAs have a rail-to-rail DC common-mode input range if the input modulator employs complementary switches. Secondly, because the noise of CCIAs is dominated by the OTA, CCIAs are more power efficient than CFIAs. Thirdly, because good matching of capacitive feedback network can

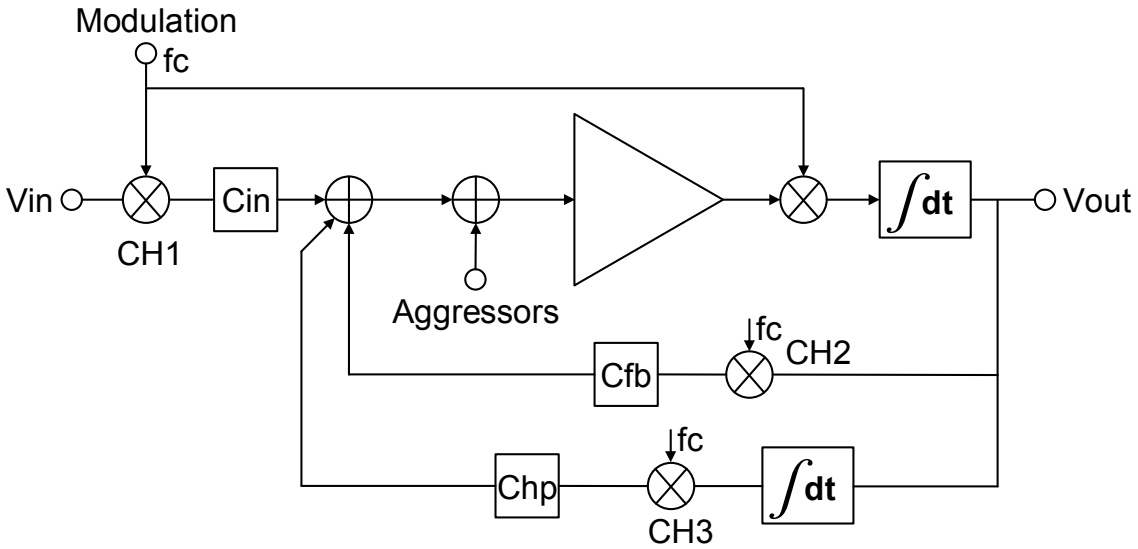


Fig. 2.9. Configuration of the CCIA in [55].

be achieved in deep submicron technology, CCIAs offers high gain accuracy. CCIAs proposed in [53], [54] feature large input impedance by placing the input chopper to the virtual ground, which is inside the feedback loop. However, CMRR is reduced, because the CMRR is limited by components mismatch [64]. More importantly, since the amplifier's virtual ground is a high-impedance node, the chopper current noise is converted into significant amounts of excess voltage noise, which dominates the amplifier's noise performance at low frequencies [65].

In order to solve this problem, the input chopper is placed before the input capacitor [55]-[63]. The configuration is illustrated in Fig. 2.9. The input signal is up-modulated to the chopping frequency before applying it to the input capacitors and so attenuate *1/f* noise and increase CMRR. In the reported architecture [55], fast modulation is performed by steering currents within the transconductance stage prior to integration, which allows a higher chopping frequency. The configuration proposed in [55] has two feedback loops.

The first feedback loop, which is composed of chopper $CH1$&$CH2$, C_{in}, and C_{fb}, sets the mid-band gain of the amplifier. The second feedback loop, which is composed of $CH1$&$CH3$, C_{in}, and C_{hp}, defines the high-pass cutoff characterization to reject DC offsets generated at the tissue-electrode interface. DC offsets are up-modulated to chopping frequency and amplified by the OTA, and then are demodulated back to DC at the output. The output DC signals are amplified by the integrator in the high-pass loop, and are up-modulated to chopping frequency and fed to the CCIA's virtual ground. In order to generate a low-frequency high-pass cutoff, the integrator needs to have a very large time constant [55]. The CCIA reported in [60] uses a two-stage fully-differential complementary-input current-reuse amplifier to achieve sufficient open-loop gain. However, the second stage needs to consume considerable power to ensure the stability. The CCIA [60] achieves the input-referred noise of 6.52 μVrms with a corresponding NEF of 2.64 over 1 to 250 Hz, while consuming 28 nA current from a 0.6 V supply. The multi-chopper CCIA [61] achieves excellent noise-power efficiency by using multiple-input/multiple-output current reuse technique [66]. However, as the number of channels increases, the stacked configuration requires more voltage headroom. Besides, the proximity and the interconnection between the channels, which is an intrinsic feature of the configuration, increases the risk of channel crosstalk [66]. The CCIA [61] achieves the input-referred noise of 1.54 μVrms with a corresponding NEF of 1.38 over 1 to 500 Hz, while consuming 266 nA current from a 1 V supply. The CCIA [62] employs duty-cycled resistors [67] to achieve high-linearity. It exhibits the input-referred noise of 7 μVrms with a corresponding NEF of 4.9 over 200 Hz to 5 kHz, while consuming 2 μW from a 1.2 V supply.

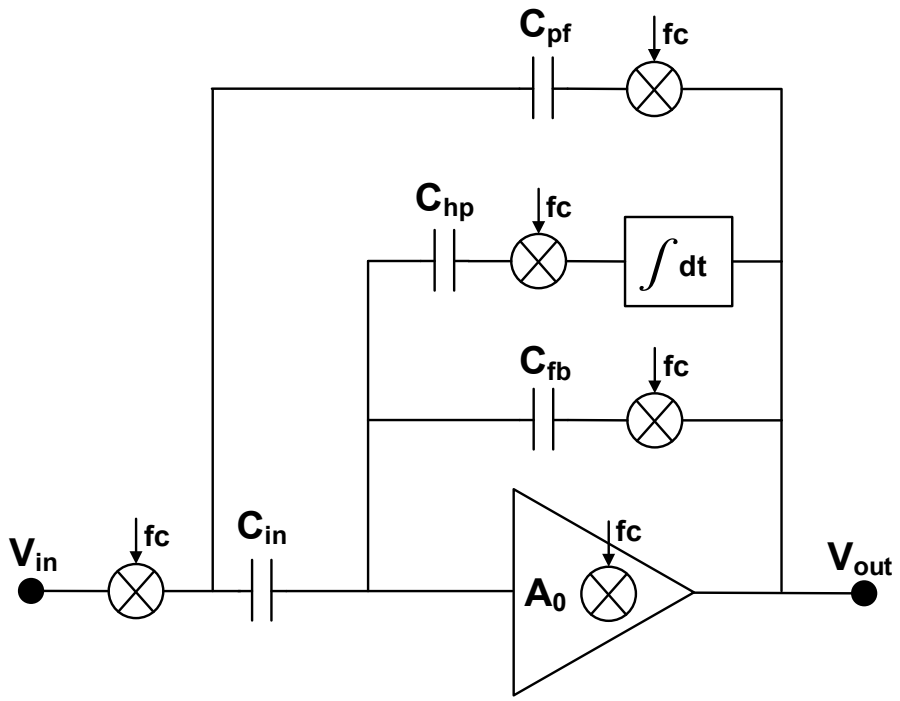


Fig. 2.10. Configuration of the CCIA with positive feedback loop in [56].

The drawback of the CCIA [55] is that its input impedance is defined by a switched-capacitor (SC) resistance formed by input chopper and input capacitor, which is limited to a few MΩ at typical chopping frequencies. The input impedance of a few MΩ is not sufficient for some of bio-potential recordings. For example, EEG recordings with dry electrodes usually require the BPAs having an input impedance higher than 100 MΩ.

In order to boost the impedance, a positive feedback loop has been reported in [56]. The configuration of the CCIA with the positive feedback loop is shown in Fig. 2.10. This loop comprises a chopper and feedback capacitor C_{pf}, which provides positive feedback to the CCIA's input. In ideal case, the positive feedback loop generates current that is equal to the current that flows through the input capacitor to achieve infinite input impedance. However, by simply choosing C_{pf}=C_{fb}, the design in [56] can't compensate for the process

variation and the parasitic capacitance associated with the bottom plate of the input capacitor, which significantly limits the input impedance boosting factor.

Chapter 3

An Ultralow-Power Low-Noise CMOS Biopotential Amplifier for Neural Recording

3.1 Introduction

Rapid advances in implantable integrated neural recording systems have allowed neuroscientists and clinicians to treat neurological disorders, such as epilepsy, Parkinson's disease, and spinal cord injuries. Large multi-channel recording systems (e.g. [12]) are capable of observing many neurons simultaneously. However, because thermal dissipation and wireless power delivery limitations constrain the total allowable power dissipation, large arrays must limit the power consumption of each channel. The small amplitude of extracellular action potentials requires input-referred amplifier noise of no more than 5-10 μV_{rms} to avoid degraded signal quality [25]. Because amplifier power is inversely related to the squared input-referred noise voltage v_{ni}^2, the simultaneous constraints on noise and power impose a challenging design tradeoff.

As discussed in chapter 2, the capacitive feedback approach proposed in [27] that uses capacitors to set the gain and to achieve DC offset rejection has become the most popular topology to build bio-potential amplifiers. Noise-power efficiency has been further improved by employing current scaling [28] and current splitting [29] techniques in folded-cascode operational transconductance amplifiers (OTA). However, the severe current scaling scheme between the input differential pairs and the folded branches requires that

current errors caused by mirroring be well-controlled. Additionally, the voltage head-room required by the large source degeneration increases the minimum supply voltage.

An open-loop single-ended CRCI amplifier [30] demonstrated very high power efficiency but suffered from poor linearity and supply rejection. Because of the poor PSRR, low-noise voltage regulation circuitry may be required, which consumes additional power and potentially increases the design complexity. Recently, a closed-loop fully-differential CRCI amplifier was presented in [31], in which the PSRR was greatly improved. However, at a given power budget, the input-referred thermal noise power was twice that of the single-ended amplifier [30] because the output noise was doubled by the differential branches, which significantly degraded the noise-power efficiency.

This chapter presents a two-stage amplifier configuration combined with CRCI technique and sharing architecture, which achieves a very good power-noise tradeoff and adequate PSRR. The AC-coupled input rejects large DC offsets generated at the electrode-tissue interface.

3.2 Neural Amplifier Design

3.2.1 Overall System Design

Fig. 3.1 shows the configuration of the proposed bio-potential amplifier. The first-stage amplifier is a single-ended CRCI amplifier [30] with capacitive feedback, which achieves a very high power-noise efficiency but poor PSRR. In order to improve the PSRR, I employ a reference amplifier (shared by N channels) which is identical to the first stage. The second stage is a fully differential OTA with capacitive feedback. The supply noise, which is equally coupled to the outputs of the first stage and the reference, is suppressed

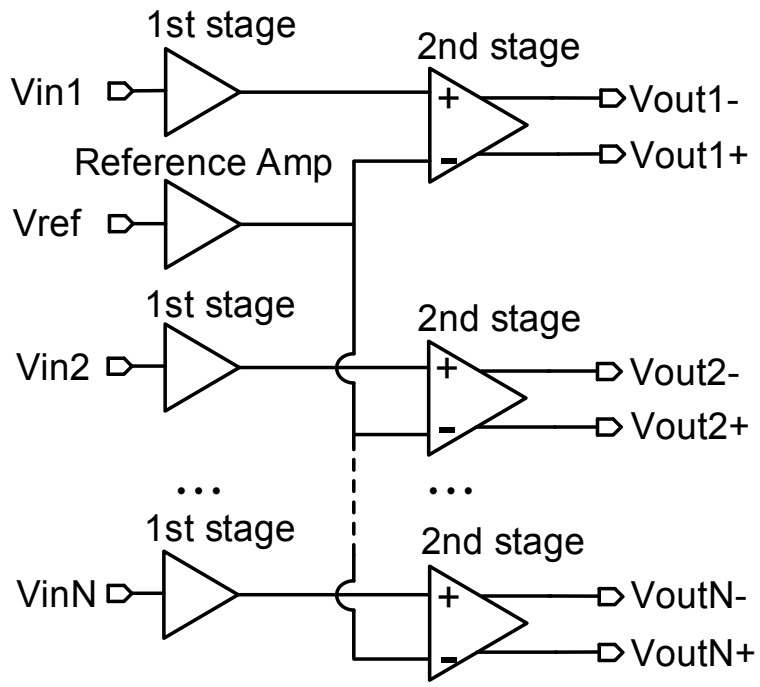


Fig. 3.1. Configuration of the proposed biopotential amplifier.

as a common-mode signal by the second stage. The sharing architecture of the reference amplifier results in a significant reduction of power dissipation. By using this approach, the whole amplifier achieves good PSRR while keeping superior noise-power efficiency.

Assuming the first stage and the reference amplifier are perfectly matched, the ideal PSRR of the whole amplifier can be expressed as

$$PSRR_{ideal} = \frac{A_{v1} \cdot A_{v2}}{A_{s1} \cdot A_{cm2}} = PSRR_1 \cdot CMRR_2 \tag{1}$$

where A_{v1} is signal gain of the first stage, A_{s1} is the supply-noise gain of the first stage, A_{v2} is the differential-mode gain of the second stage, A_{cm2} is the common-mode gain of the second stage, $PSRR_1$ is the power supply rejection ratio of the first stage, and $CMRR_2$ is the common-mode rejection ratio of the second stage.

Taking the mismatch between the first stage and the reference amplifier into consideration, (1) can be modified as

$$PSRR = \frac{A_{v1} \cdot A_{v2}}{\Delta A_{s1} \cdot A_{v2} + A_{s1} \cdot A_{cm2}} \tag{2}$$

where ΔA_s represents the supply-noise gain mismatch between the first stage and the reference. If the supply-noise gain mismatch (ΔA_s) is sufficiently small, (2) can be reduced to (1).

Using a similar approach, the CMRR of the whole amplifier can be expressed as

$$CMRR = \frac{A_{v1} \cdot A_{v2}}{\Delta A_{v1} \cdot A_{v2} + A_{v1} \cdot A_{cm2}} \tag{3}$$

where ΔA_{v1} represents the signal gain mismatch between the first stage and the reference.

The total current consumption per channel can be expressed as

$$I_{tot} = I_1 + \frac{I_{REF}}{N} + I_2 \tag{4}$$

where I_1, I_{REF}, I_2 represent the current consumption of the first stage, reference amplifier, and the second stage, respectively, while N is the number of the channels. Since the first stage and the reference amplifier are identical (I_1=I_{REF}), we get

$$I_{tot} = \frac{N+1}{N} I_1 + I_2 \tag{5}$$

If the number of channels N is large, the power consumed by the reference amplifier for each channel can be neglected.

The input-referred noise power of each amplifier can be calculated as

$$v_{ni}^2 = v_{ni1}^2 + v_{niREF}^2 + \frac{v_{ni2}^2}{A_{v1}^2} \tag{6}$$

where v_{ni1}^2, v_{niREF}^2, v_{ni2}^2 represents the input-referred noise power of the first stage, the reference amplifier, and the second stage, respectively, while A_{v1} is the gain of the first

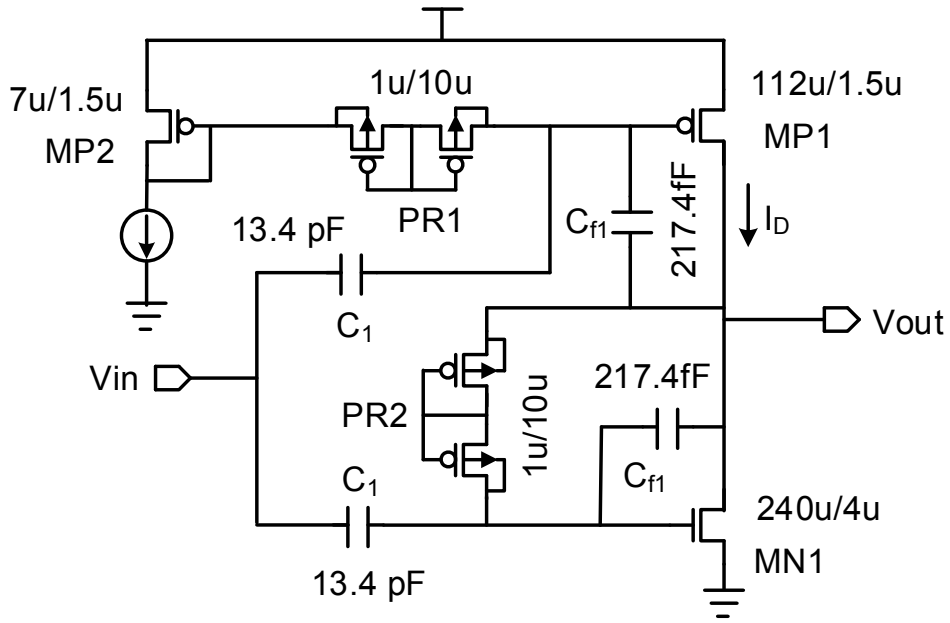


Fig. 3.2. Schematic of the first-stage amplifier.

stage. Since the first stage and the reference amplifier are identical ($v_{ni1}^2 = v_{niREF}^2$), and the gain of the first stage A_{v1} is set to be sufficiently large, (6) can be simplified as

$$v_{ni}^2 \approx 2v_{ni1}^2 \tag{7}$$

Typical extracellular action potentials have frequency content ranging from 100 Hz to 7 kHz [36]. In order to accurately capture spiking activity, this amplifier was designed to have bandwidth extending up to 10 kHz.

3.2.2 First-Stage Design

The schematic of the first-stage amplifier is shown in Fig. 3.2. In order to reject the large dc offsets generated at the electrode-tissue interface, MOS-bipolar pseudo-resistors [27] with high resistances and on-chip capacitors are employed. The incremental resistance of the pseudo-resistors is extremely high (>10 GΩ) [27] when the voltage across it is small

($|\Delta V| < 0.2$ V). The open-loop single-ended CRCI amplifier [30] can give superior noise performance for a given power budget at the expense of reduced linearity and imprecise gain control. According to (2) and (3), the gain mismatch between the first stage and the reference amplifier needs to be minimized to achieve good PSRR and CMRR. In order to obtain precise gain control and improve linearity, capacitive feedback [27] is used in the first stage and reference amplifier. The mid-band gain of the first-stage amplifier is written as

$$A_{v1} = \frac{C_1}{C_{f1}} \tag{8}$$

In order to achieve sufficient matching for the required PSRR and CMRR, the capacitors (C_1 and C_{f1}) are large and carefully laid out, occupying 45% of the chip area in this design.

By driving the gates of both PMOS and NMOS input transistors, the CRCI technique fully reuses the current and doubles the effective transconductance, which leads to a significant reduction in input-referred noise. Several other strategies are utilized to minimize the input-referred noise. Firstly, since the flicker noise is inversely proportional to gate area, the transistors *MN*1 and *MP*1 are sized large enough to reduce the flicker noise to an acceptable level. Secondly, in order to maximize g_m/I_D, the *W/L* ratios of *MN*1 and *MP*1 are chosen for weak inversion operation. Lastly, the *RC* network formed by the pseudo-resistor element and the ac-coupling capacitor at the gate of *MP*1 presents a low-pass feature to filter out most of the noise from the current reference *MP*2 and the pseudo-resistor *PR*1.

Assuming thermal noise contribution is dominant and according to the design guidelines presented in [68], analysis of this circuit reveals the input-referred noise power

of the first-stage amplifier can be expressed as

$$\frac{v_{ni1}^2}{\Delta f}=\left(\frac{C_1+C_{f1}}{C_1}\right)^2\bullet\left[\frac{2kT}{\kappa(g_{mn1}+g_{mp1})}\right]+\left(\frac{C_{f1}}{C_1}\right)^2\bullet\frac{4kTR_{PR}}{\left(1+sC_{f1}R_{PR}-\frac{sC_1R_{PR}}{g_{mn1}(r_{on1}\|r_{op1})}\right)^2}$$
$$+\left(\frac{C_1+C_{f1}}{C_1}\right)^2\bullet\left(\frac{g_{mp1}}{g_{mp1}+g_{mn1}}\right)^2\bullet\left(\frac{1}{1+sC_1R_{PR}}\right)^2\bullet\left(4kTR_{PR}+\frac{2kT}{\kappa g_{mp2}}\right) \quad (9)$$

where g_{mn1}, $g_{mp1,2}$ are the transconductances of the transistors $MN1$, $MP1$, and $MP2$, respectively, r_{on1} and r_{op1} are the output resistances of the transistors $MN1$ and $MP1$, respectively, R_{PR} represents the equivalent resistance of the pseudo-resistors, and κ is the reciprocal of the sub-threshold slope factor n_p. The last two items in (9) represent the noise contribution from pseudo-resistors and the current reference $MP2$. In order to minimize the noise contribution from pseudo-resistors and the current reference $MP2$, long-channel (L=10 μm) pseudo-resistors are used to increase their equivalent resistance. Assuming $g_{mn1}=g_{mp1}=g_m$, (9) then reduces to

$$\frac{v_{ni1}^2}{\Delta f}\approx\left(\frac{C_1+C_{f1}}{C_1}\right)^2\bullet\left(\frac{kT}{\kappa g_m}\right) \quad (10)$$

By observing (6), (8), and (10), in the design, the ratio of C_1/C_{f1} needs to be large enough to minimize the input-referred noise of the first stage and the noise contribution from the second stage.

3.2.3 Second-Stage Design

The schematic of the second-stage fully-differential amplifier is shown in Fig. 3.3. The topology of the amplifier is similar to that in [27]. The circuit employs capacitive feedback other than resistive feedback to achieve low-noise operation. The mid-band gain

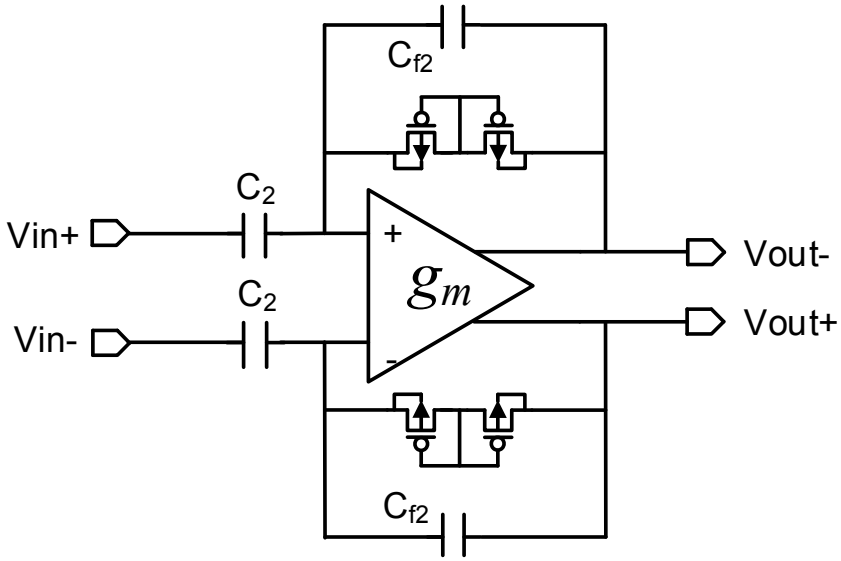


Fig. 3.3. Schematic of the second-stage amplifier.

A_{v2} is set by the ratio of C_2/C_{f2}. The MOS-bipolar pseudoresistors combined with the feedback capacitors C_{f2} creates a low-frequency high-pass cutoff.

The schematic of the OTA is shown in Fig. 3.4. The noise contribution from the second stage is v_{ni2}^2/A_{v1}^2, where v_{ni2}^2 represents the input-referred noise power of the second stage, and A_{v1} represents the gain of the first stage. Since the noise contribution of the second stage is reduced by a factor of A_{v1}, noise performance of the second stage can be sacrificed for ultra-low power operation. In order to reduce the flicker noise and achieve better matching, the transistors are large. The input-referred thermal noise power of the second stage can be expressed as

$$\frac{v_{ni2}^2}{\Delta f} = \left(\frac{4kT}{\kappa} \frac{1}{g_{mp1}} + 16kT\gamma \frac{g_{mn1}}{g_{mp1}^2} + 8kT\gamma \frac{g_{mp6}}{g_{mp1}^2} \right) \bullet \left(\frac{C_2 + C_{f2}}{C_2} \right)^2 \tag{11}$$

where κ is the reciprocal of the sub-threshold slope factor n_p, and γ is the excess noise factor of the transistor in the strong inversion regime (γ=2/3). Based on (11), the input-pair

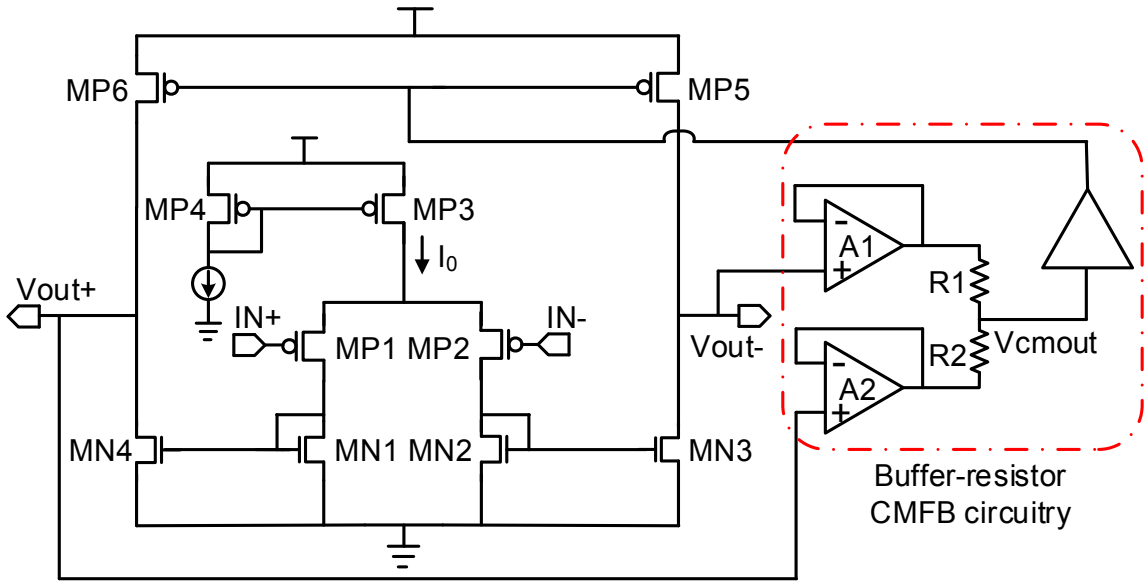


Fig. 3.4. Schematic of the OTA used in the second-stage amplifier.

transistors *MP*1 and *MP*2 are biased in weak inversion to maximize g_m/I_D, while *MN*1-*MN*4, *MP*5, and *MP*6 are biased in strong inversion regime to minimize g_m/I_D.

In the fully-differential amplifier, conventional resistor-averaged CMFB circuitry [69] is usually used, where two large resistors are employed to sense and average the output common-mode voltages. The value of the resistors needs to be much larger than the output resistances $r_{op6}||r_{on4}$, where r_{op6} and r_{on4} are the output resistances of the transistors *MP*6 and *MN*4, respectively. Otherwise, the open-loop gain of the OTA would be significantly degraded. As the tail current I_0 decreases, the output resistances of the transistors *MP*6 and *MN*4 increases. Thus, larger CMFB-averaging resistors are required. In the design, the tail current I_0=190 nA, and a total value of 100 MΩ of the CMFB-averaging resistors is needed. This large resistance is normally implemented by connecting several smaller resistors in series and occupies a large chip area of 75000 μm^2 even if the high-resistive poly-silicon resistors with minimum design rule in the process are used. Moreover, the parasitic

capacitances introduced by the large resistors are too big (>5 pF), which will greatly degrade the phase margin of the CMFB loop and make frequency compensation difficult. In order to solve these problems, I propose a buffer-resistor averaged CMFB circuitry, which is shown in Fig. 3.4. The input resistance of the buffer is large enough to ensure that the open-loop gain of the OTA will not degrade. The dimension of the differential-pair transistors are chosen to be small (5μm/0.8μm) so that the input capacitance of the buffer will not affect the stability of the CMFB loop. By using the buffers to sense the output common-mode voltage, the value of the averaging resistors can be greatly reduced. In this design, the total value of the averaging-resistors is only 240 KΩ. In the layout implementation, the total area of the buffers and the averaging-resistors is only 3000 μm^2, which is 4% of that of the conventional resistor-averaged structure. The drawback of the buffer-resistor averaged CMFB is that the current consumption of the CMFB circuitry is increased because the buffers consume additional current. In this design, the total current consumption of the buffers is 100 nA. Considering the advantages it brings, this small current-consumption increase is worthwhile.

3.2.4 Crosstalk, Nonlinearity, and NEF

Crosstalk is an issue in a multi-channel system. Firstly, there is crosstalk from the coupling between the signal output and the input of the non-corresponding second stage. These sources of coupling can be minimized through careful layout. Secondly, there is crosstalk due to supply coupling. Sufficient PSRR ensures adequate rejection of the noise coupled in the supply.

The incremental resistance of the pseudo-resistors is extremely high when the

voltage across it is small ($|\Delta V| < 0.2$ V) [27]. However, the incremental resistance is dramatically reduced as $|\Delta V|$ increases, degrading the amplifier's linearity. Although the input transistors and the active load transistors also contribute to nonlinearity, the analysis in [35] shows this contribution can be ignored if the amplifier has large loop gain. Therefore, the pseudo-resistors are the major cause of nonlinearity in the topology proposed in [27]. The proposed amplifier can be expected to exhibit more nonlinearity than single-stage amplifiers (e.g. [27]-[29]), because of the larger amplitude of the second-stage inputs signals, but the use of two series transistors in the pseudo-resistor provides sufficient linearity for the signal amplitudes expected in extracellular recording. For applications requiring greater linearity, the first-stage gain could be reduced, albeit with an increased noise contribution from the second stage. A feedback transconductor might be used in place of the pseudo-resistor [31] with a modest increase in noise. If a lower high-pass corner frequency is acceptable, additional series devices can also be added to the pseudo-resistor to increase the linear range.

Assuming thermal noise is dominant, and the noise of the second stage are negligible, from (7) and (10), the input-referred noise power of the amplifier is expressed as

$$\frac{v_{ni}^2}{\Delta f} = \left(\frac{C_1 + C_{f1}}{C_1}\right)^2 \bullet \left[\frac{4kT}{\kappa(g_{mn1} + g_{mp1})}\right] \tag{12}$$

Since $C_1 \gg C_{f1}$, and $g_{mn1} = g_{mp1} = g_m$,

$$\frac{v_{ni}^2}{\Delta f} \approx \frac{2kT}{\kappa g_m} \tag{13}$$

To compare the power-noise tradeoff among amplifiers, the noise efficiency factor (NEF) reported in [70] is adopted:

$$NEF = v_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{14}$$

where k is boltzmann constant, U_T is the thermal voltage, $v_{ni,rms}$ is the total input-referred noise, BW is the -3 dB bandwidth of the amplifier, and I_{tot} is the total current consumption.

Assuming the current consumed by the second stage is negligible ($I_{tot} \approx [(N+1)/N]\cdot I_D$), the theoretical NEF limit of the proposed architecture is derived as

$$NEF = \frac{1}{2\kappa}\bullet\sqrt{\frac{2(N+1)}{N}} \tag{15}$$

where $1/(2\kappa)$ is the theoretical limit of the NEF for a single-ended CRCI amplifier. By using this approach, the design can achieve a theoretical limit of NEF lower than that of a differential pair ($\sqrt{2}/\kappa$) [28]. Assuming a typical value of κ=0.7, the NEF is equal to 1.24 for a two-channel (N=2) amplifier, falling to 1.13 for N=8. As the number of channels N increases, NEF gets improved due to the reduction of current consumption. Excluding the current consumption of the second stage, the proposed reference-sharing architecture allows a current reduction of $[(N-1)/2N]\times 100\%$ compared to a non-sharing configuration (N=1). However, for large values of N, the complexity of a layout with good matching significantly increases, which may result in degradation of the PSRR and CMRR. In the proposed design, N=2 has been selected for a reasonable tradeoff among the critical parameters, including power, NEF, PSRR.

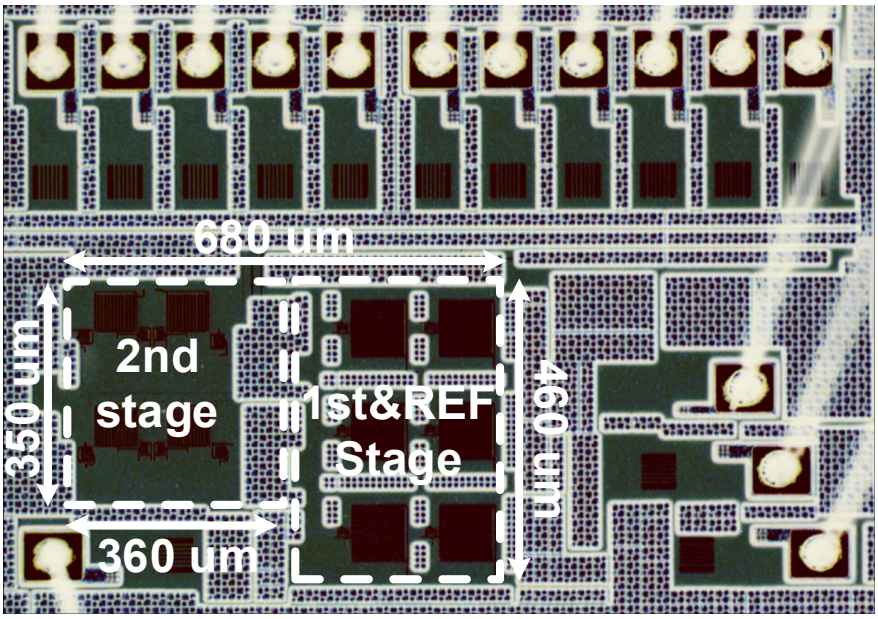


Fig. 3.5. Die photograph of the two-channel biopotential amplifier.

3.3 Experiment Results

3.3.1 Bench Measurement Results

A two-channel amplifier (*N*=2) was fabricated in a 90-nm CMOS process. A die photo is shown in Fig. 3.5. The total occupied silicon area is 0.274 mm^2, which results in a silicon area of 0.137 mm^2 for each channel. Each channel draws a current of 2.85 μA from a 1 V supply. It can be broken down as follows: 1.48 μA for the first stage, (1.48μA)/2 for the reference (shared by two), and 0.63 μA for the second stage.

The measured transfer function of the amplifier is shown in Fig. 3.6. The mid-band gain of the amplifier is 58.7 dB (34.1 dB for the first stage, 24.6 dB for the second stage). The -3-dB bandwidth is from 490 mHz to 10.5 kHz.

The input-referred noise spectrum of the amplifier is shown in Fig. 3.7. The input-

referred noise spectrum is obtained by dividing the output noise spectrum by the mid-band gain of the amplifier. The total input-referred RMS noise is 3.04 μV_{rms} integrated from 100 mHz to 100 kHz.

By using (14) and including noise and power contributions from the second stage and the reference amplifier, the calculated NEF is 1.93. NEF can be further improved when the reference amplifier is shared by more channels. Because the conventional NEF does not consider the supply voltage, a modified metric $NEF^2 \cdot VDD$ proposed in [71] is also calculated. $NEF^2 \cdot VDD$ of this design is 3.72.

Fig. 3.8 shows the measured PSRR of the amplifier, which is better than 50 dB in the pass-band. The amplifier is compared with a few other state-of-art neural amplifiers in Table II. The proposed amplifier exhibits better NEF than all other amplifiers except [30]. However, the proposed amplifier's PSRR is much better than that of [30].

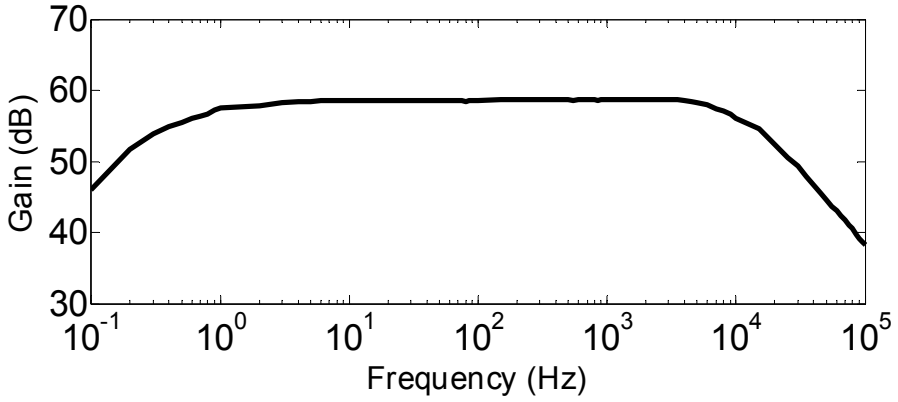


Fig. 3.6. Measured transfer function of the proposed amplifier.

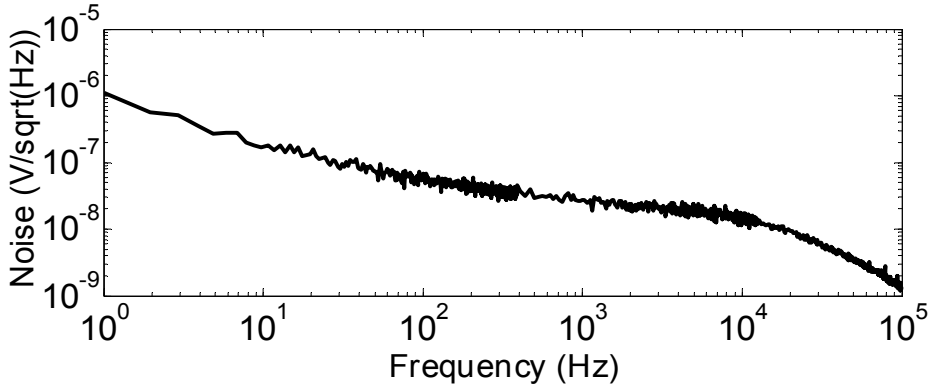


Fig. 3.7. Measured input-referred noise of the proposed amplifier.

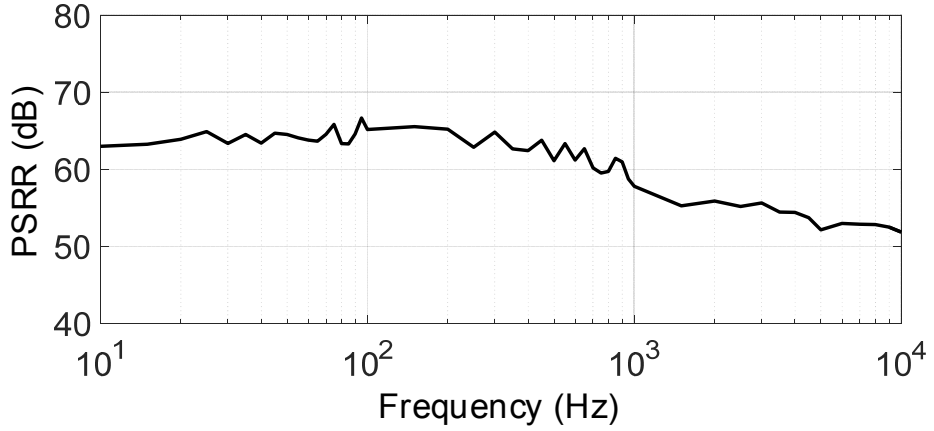


Fig. 3.8. Measured power supply rejection ratio (PSRR).

Table II Neural Amplifier Performance Comparison.

	TBioCAS 2007 [28]	JSSC 2011 [29]	EMBC 2007 [30]	TBioCAS 2012 [31]	TCASI 2013 [38]	This Work
Supply voltage (V)	2.8	2.8	1	1	1.8	1
Total current (μA)	2.7	.872	.805	12.1	6.1	2.85
Power (μW)	40.85	39.4	36.1	40	48/60	58.7
Gain (dB)	45-5.32k	.36-1.3k	.3-4.7k	.05-10.5k	1-9k	.49-10.5k
BW (Hz)	3.06	3.07	3.6	2.2	5	3.04
$V_{ni,rms}$ (μV_{rms})	2.67	3.09	1.8	2.9	4.6	1.93
NEF	20	26.7	3.24	8.4	38.1	3.72
NEF^2Vdd	< 1%	<1%	7.1%	1%	1.2%	1.6%
THD (1 mV_{pp}@1kHz)	75	>80	5.5	≥ 80	55	> 50
PSRR (dB)	66	>66	/	80	48	> 45*
Area (mm^2)	.16	.13	.046	.072	0.065	.137
Process (μm)	.5	.6	.5	.13	.18	.09

*CMRR in Monte-Carlo simulation (100 runs).

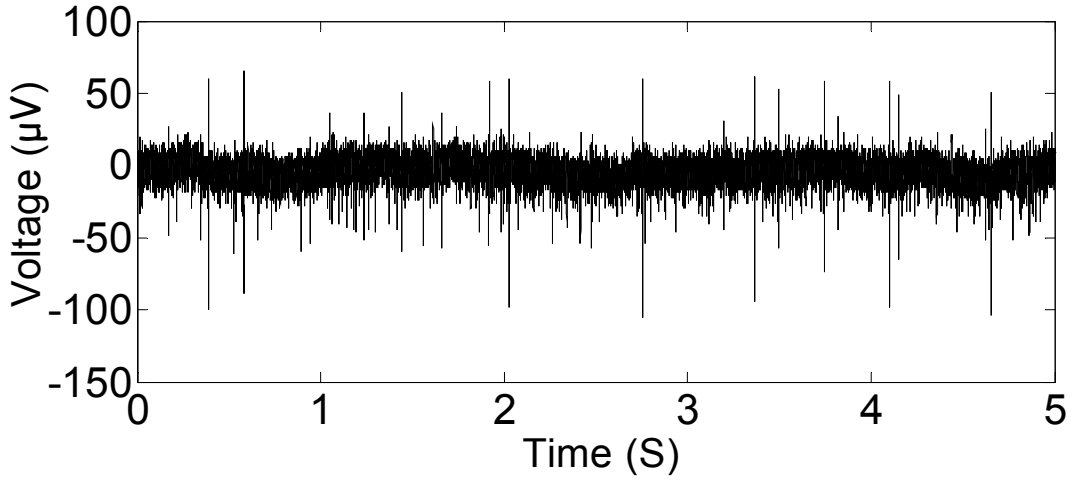
Typically, low-noise regulators [72], [73] have an output RMS noise around 20 μVrms integrated from 10 Hz to 100 kHz. The output noise of the regulator should satisfy the condition

$$v_{no,reg} \ll v_{ni,amp} \cdot PSRR \tag{16}$$

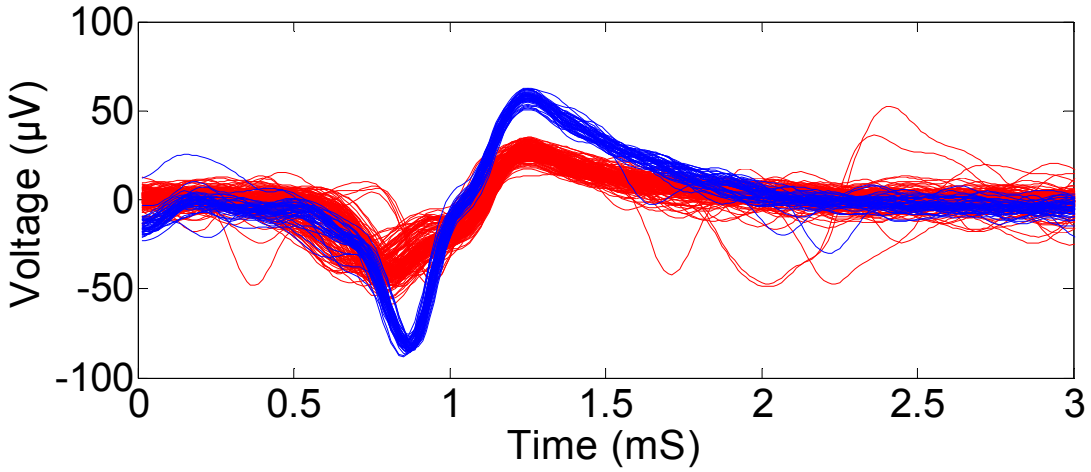
$v_{no,reg}$ is the output RMS noise of the regulator, $v_{ni,amp}$ is the input-referred RMS noise of the amplifier, PSRR is the power supply rejection ratio of the amplifier. Assuming the regulator noise referred to the amplifier input should be at least ten times smaller than the amplifier's own input-referred noise, an amplifier should have a PSRR better than 35 dB for typical values of $v_{no,reg}$ = 20 μVrms and $v_{ni,amp}$= 3.5 μVrms. The PSRR (5.5 dB) of a simple single-ended amplifier [30] is not sufficient for most applications, while the improvements described in this paper yield adequate PSRR for typical application scenarios.

3.3.2 Biological Measurement Results

The neural amplifier's performance was verified by using it to record action potentials from sensory neurons in the leg of the Orange-headed cockroach *Eublaberus posticus*. A long-duration recoding were made from the amplifier. Fig. 3.9 (a) shows the long-duration trace which is scaled by the amplifier gain. Fig. 3.9 (b) shows two classes of spikes recorded through the proposed amplifier, which are sorted using automated spike-sorting software [74].



(a)



(b)

Fig. 3.9. Biological recordings from sensory neurons in the leg of the Orange-headed cockroach *Eublaberus posticus*. (a) Long-duration trace. (b) Two classes of spikes sorted by post-processing programs.

Chapter 4

A Configurable Analog Front-End for Biosignal Acquisition

4.1 Introduction

Biopotential signals (EEG, ECG, EMG, AP, etc.) provide vital information about the patients which allow clinicians to diagnose and treat diseases like muscle paralysis, cardiovascular diseases, brain injuries, epilepsy, etc. Biopotential signals have different frequency and amplitude characteristics. For example, EEG signals have amplitudes from 1 to 100 μV with much of the energy in the sub-Hz to 100 Hz band. AP signals have amplitudes up to 500 μV with much of the energy in the 100 Hz to 7 kHz band. In order to improve the quality of healthcare, it is desirable to have a biosignal acquisition system suitable for a variety of biopotential signals. In such a system, a configurable low-noise AFE is required. Besides, in wearable/implantable systems, low-power operation is essential to extend battery life and avoid thermal damage to surrounding tissues.

Several recent efforts have advanced the state-of-the-art of low-power low-noise biopotential amplifiers [51], [55], [59], [71], [75]. Amplifiers in [55], [59] achieved good low-frequency noise (<1 μV_{rms}) by using capacitively coupled chopper topology, but focused only on NFP/EEG (sub-Hz to 100 Hz) acquisition. Dual-band AFEs in [51], [71], [75] were designed for local field potentials (LFPs, <200 Hz) and AP acquisition. However, the designs in [71], [75] exhibited inferior low-frequency noise (4.3 μV_{rms} and 14 μV_{rms},

respectively). The design reported in [51] employed a DC-coupled source-degenerated topology to achieve high input impedance, while sacrificing power efficiency which resulted in an inferior NEF of 7.6.

This chapter presents a power-efficient AFE with configurable bandwidth and gain. The AFE employs a chopper-stabilized current-reuse complementary input (CRCI) telescopic-cascode amplifier to achieve high noise-power efficiency and suppress the low-frequency noise. A tunable input impedance-boosting loop (IBL) compensates for process variation and parasitic capacitance, and maximizes the input impedance-boosting factor. The AFE's performance is demonstrated with biological measurements.

4.2 Analog Front-End Design

4.2.1 Top-Level Design

Fig. 4.1 shows the configuration of the configurable analog front-end. The bio-potentials detected by the electrode are amplified by the front-end and digitized by the following analog-digital-converter (ADC). The AFE comprises a first-stage chopper-stabilized low-noise amplifier (LNA), a second-stage variable-gain amplifier (VGA), a tunable high-linearity 2nd-order low-pass filter (LPF), and two single-ended third-stage amplifiers. The gain of the AFE ranges from 46 to 72 dB. The first-stage LNA is chopper-stabilized to minimize the low frequency noise such as 1/f noise and popcorn noise. Fully differential topology is employed to improve CMRR and PSRR. The gain of the first stage is set to be 40 dB. The second-stage VGA provides gain from 0 to 26 dB. The adjustable gain of the VGA ensures the output of the second-stage keeps half rail-to-rail. The LPF is used to tune the low-pass cut-off. More importantly, LPF is required to filter out the up-

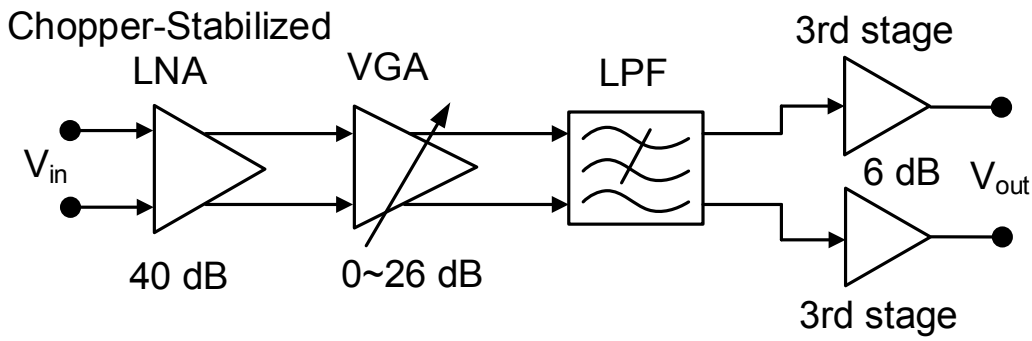


Fig. 4.1 Configuration of the proposed AFE.

modulated low-frequency noise as well as the offset. Two single-ended third-stage amplifier with a fixed gain of 6 dB is added to achieve large output swing, which can relax the resolution requirement of the ADC, and thus reduces the power consumption of the ADC as well as decreasing ADC design complexity.

There is a trade-off of placing the LPF in the front-end. The LPF is not placed after the third-stage, because high-linearity LPF with rail-to-rail input would increase the design complexity that would result in more power consumption, worse noise performance and larger chip area. By putting LPF before third-stage, the dynamic range requirement of the LPF is relaxed, and thus simplifies the filter design. By putting LPF after second-stage, the noise contribution from the LPF would be significantly attenuated, and thus reduces the power consumption.

The input-referred noise of the AFE can be expressed as

$$v_{ni}^2 = v_{ni,1\mathrm{st}}^2 + \frac{v_{ni,2\mathrm{nd}}^2}{A_{v,1\mathrm{st}}^2} + \frac{v_{ni,\mathrm{LPF}}^2}{A_{v,1\mathrm{st}}^2 \cdot A_{v,2nd}^2} + \frac{v_{ni,3\mathrm{rd}}^2}{A_{v,1\mathrm{st}}^2 \cdot A_{v,2nd}^2} \tag{17}$$

where $v_{ni,1st}^2$, $v_{ni,2\text{nd}}^2$, $v_{ni,\text{LPF}}^2$ and $v_{ni,3\text{rd}}^2$ represents the input-referred noise power of the first stage, the second stage, the LPF and the third-stage, respectively, while $A_{v,1st}$, $A_{v,2\text{nd}}$ represents the mid-band gain of the first stage and second stage, respectively. In the design, the mid-band gain of the first-stage $A_{v,1st}$ is large enough, so the noise contribution from the following blocks can be ignored. (17) can be simplified as

$$v_{ni}^2 \approx v_{ni,1\text{st}}^2 \tag{18}$$

4.2.2 First-Stage LNA Design

4.2.2.1 Top-Level Design

Fig. 4.2 shows the configuration of the chopper-stabilized first-stage amplifier. This capacitively-coupled chopper stabilization topology is composed of a chopper stabilized amplifier (OTA G_m, $CH1$, and $CH2$), a DC feedback (R_{P1} and $CH3$) biasing the OTA input, a capacitive feedback network (C_{in1}, C_{fb1}, and $CH3$), and a DC servo loop (an integrator, PMOS-buffer, C_{hp}, and $CH4$), and an input impedance boost loop (C_{ib} and $CH5$). Fully differential architecture is employed to provide high common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR).

The mid-band gain of the amplifier is set by capacitor ratio C_{in1}/C_{fb1}, which provides excellent noise and linearity properties. Note that the polarities of these feedback loops are always constant. When the polarity around the amplifier shifts, the internal chopper modulation within the OTA also changes to maintain loop stability. With $CH1$ employing complementary switches, a rail-to-rail input common mode range is achieved

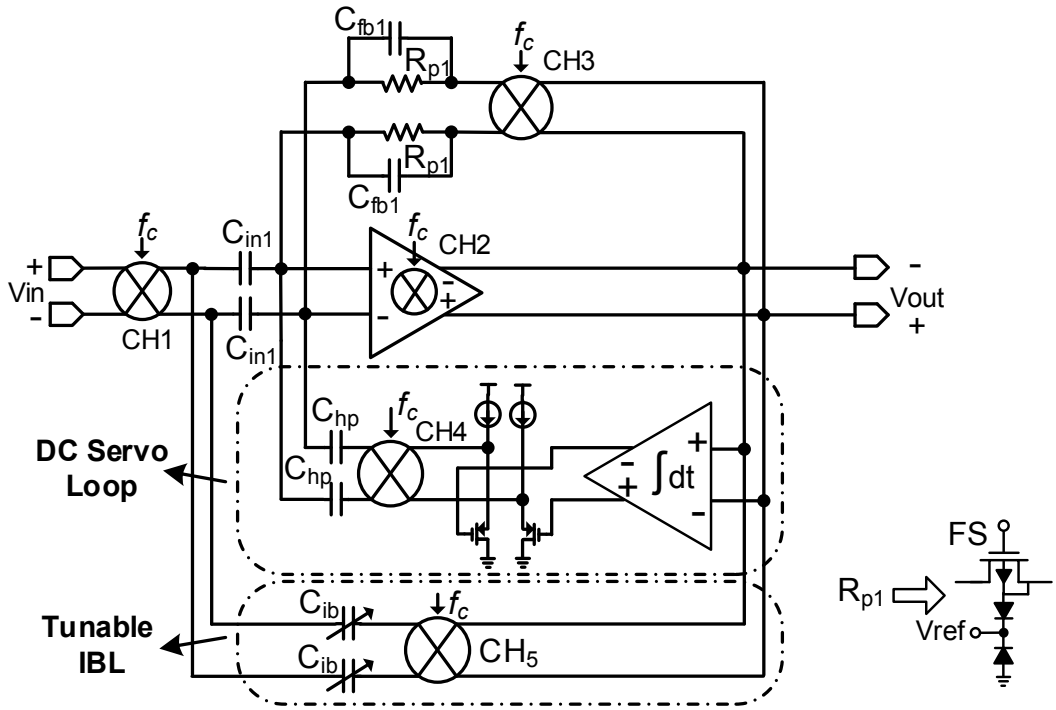


Fig. 4.2 Configuration of the first-stage chopper-stabilized LNA.

due to the input capacitor (C_{in1}). The amplifier noise is dominated by that of the OTA, which is more power efficient than CFIAs. The capacitively-coupled chopper stabilized topology modulates the input signal before applying it to the input capacitors and so attenuate flick noise and increase CMRR.

The input impedance is defined by a switched-capacitor (SC) resistance formed by input chopper and input capacitor, which can be expressed as $1/(2f_cC_{in1})$, where f_c is the chopping frequency. In this design, the gain of the first stage is set to be 100 with choosing C_{in1}=4 pF, C_{fb1}=40 fF. The chopping frequency f_c is chosen to be 25 kHz. Without input impedance boost loop, the simulated input impedance is 4.3 MΩ. A capacitive input impedance boosting loop (IBL) [56] exploits partial positive feedback to increase the input impedance without extra current consumption. In order to compensate for the process

variation and capacitance associated with C_{in1}'s bottom plate and achieve maximum impedance boosting factor, tunable capacitors (C_{ib}) are used in the design. The DC servo loop defines the high-pass cutoff characteristics of the amplifier to reject large DC electrode offsets. PMOS source-followers act as buffers for the integrator to drive the switched-capacitor load. The triple-well NMOS transistors (R_{P1}) are normally biased in subthreshold region to set DC bias, and they can also act as reset switches.

The input-referred noise of the first-stage can be expressed as

$$v_{ni,1st}^2 = \left(\frac{C_{in1}+C_{fb1}+C_{hp}+C_{ib}}{C_{in1}} \right)^2 v_{ni,OTA}^2 \tag{19}$$

4.2.2.2 First-Stage OTA Design

Folded-cascode topology are widely used to build the OTAs in instrumentation amplifiers [53], [55], [56], [59], because it achieves high gain in single stage, and features wide output swing as well as good power efficiency. Compared with the folded-cascode topology, the telescopic-cascode topology has less current branches and noise contributors while keeps high gain feature, and so is more power-efficient. Although telescopic-cascode amplifier has less common-mode input range and output swing, the small signal levels of neural signals relax those requirements. A single-ended amplifier based on current-reuse complementary-input (CRCI) technique was firstly reported in [30], which has a poor PSRR of 5.5 dB. By driving the gates of both PMOS and NMOS input transistors, the CRCI approach fully reuses the current and thus doubles the effective transconductance, which leads to a significant reduction in input-referred noise. To improve the PSRR, a fully-differential Miller two-stage amplifier based on CRCI was presented in [31].

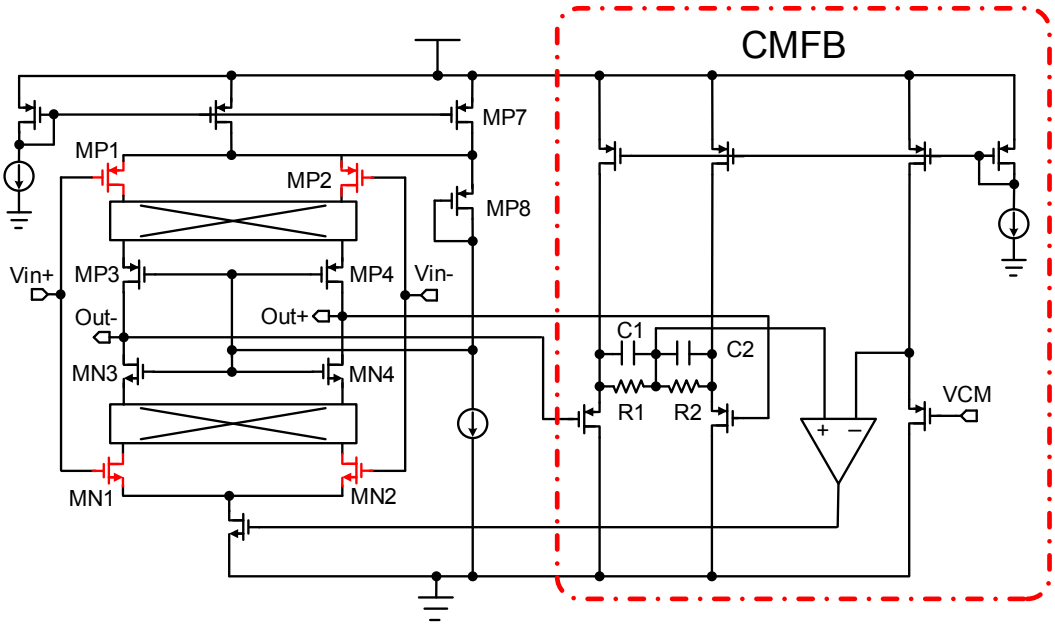


Fig. 4.3 Schematic of the current-reuse complementary input (CRCI) telescopic-cascode OTA.

Although the power consumption of the second-stage can be minimized to achieve low power, large capacitors are needed to maintain loop stability. Moreover, due to the use of the large capacitor, the limited bandwidth put constraints on the chopping frequency.

In the design, a CRCI telescopic-cascode OTA is employed. Fig. 4.3 shows the schematic of the proposed current-reuse complementary-input (CRCI) telescopic-cascode OTA. Instead of providing separate bias for the gate of the complementary-input transistors [31], the gates of the complementary-input pairs are tied together (*MP*1-*MN*1, and *MP*2-*MN*2), respectively, which saves one bias reference and simplifies the design. In the design, Cascode PMOS (*MP*3 and *MP*4) and NMOS (*MN*3 and *MN*4) pairs are utilized to increase the open-loop gain. A diode-connected transistor (*MP*8) and current source (*MP*7) are employed to bias the gates of the cascode transistors. Complementary switches are placed

at the low impedance node in between the drains of input transistors and the sources of the cascode transistors, which allows chopping the amplifier at higher frequencies. Voltage-buffer CM-sense circuitry is used to avoid the loading effect from *R*1 and *R*2. Capacitors *C*1 and *C*2 are added in parallel with each sense resistor to compensate the CMFB loop by introducing a left-half-zero. Thick-oxide MOS transistors are used at the complementary-input to reduce gate leakage currents that could result in significant DC-offsets, and to offer higher intrinsic gain. The complementary-input transistors are biased in sub-threshold region to improve the noise-power efficiency [27].

For the CRCI telescopic-cascode OTA, the primary noise sources are the complementary-input pairs (*MP*1,2 and *MN*1,2). It should be mentioned the *1/f* noise of the cascode transistors (*MP*3,4 and *MN*3,4) is not up-modulated, since the switches are placed at the sources of cascode transistors (low impedance node) instead of the output node (high impedance node). Thus, although the noise contribution of cascode transistors is significantly attenuated, the relatively large gate area is required to minimize their *1/f* noise.

The input-referred thermal noise of the CRCI telescopic-cascode OTA can be approximated as

$$v_{ni,OTA}^2 = \frac{4kT}{\kappa(g_{mn1} + g_{mp1})} \cdot \Delta f \tag{20}$$

where g_{mp1} and g_{mn1} represent the transconductance of input PMOS (*MP*1,2) and NMOS (*MN*1,2), respectively.

If $g_{mp1} = g_{mn1} = g_m$, then the equation (20) is simplified as

$$v_{ni,OTA}^2 = \frac{2kT}{\kappa g_m} \cdot \Delta f \tag{21}$$

The input-referred thermal noise of a basic differential-pair operational amplifier can be expressed as

$$v_{ni,OTA}^2 = \frac{4kT}{\kappa g_{mn}} \cdot \Delta f \tag{22}$$

Comparing the equations (21) and (22), the amplifier transconductance is doubled by the CRCI strategy at the same bias current.

4.2.2.3 DC Servo Loop

The DC servo loop proposed in [55] defines the high-pass cutoff characteristics of the amplifier to reject large DC electrode offset. The DC signal at the output of the chopper amplifier is amplified by the integrator, and up-modulated to chopping frequency by *CH*4. Then, this up-modulated signal is fed back to the input of the chopper amplifier through capacitor C_{hp} to cancel out the up-modulated DC electrode offset by negative feedback. The combination of *CH*4 and C_{hp} can be seen as an equivalent impedance of $1/(2f_cC_{hp})$ that loads the integrator's output, which may lead to a large drop of the integrator's DC gain. Two PMOS source-follower buffers are employed to isolate the integrator's output and the switch capacitor load, instead of using a fully-differential opamp buffer. PMOS source-follower exhibits the properties of better noise performance, less power consumption, and smaller area. The more important reason is the source-follower introduces less parasitic poles, which would not degrade the loop stability.

Several design constraints must be considered in the integrator design. The first constraint is a large time-constant integrator is needed to generate a sub-Hz high-pass cutoff. Switched-capacitor integrator was employed in [55] to achieve higher accuracy and tunability. However, this sampled-data filter is subject to aliasing and *kT/C* noise.

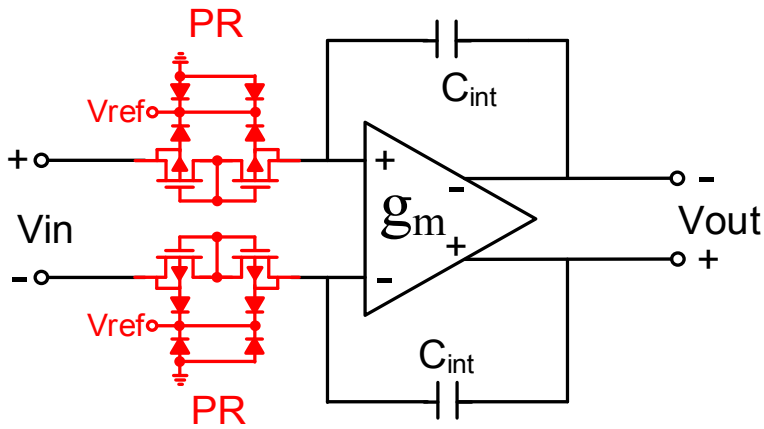


Fig. 4.4 Schematic of pseudo-resistor based large-time constant integrator.

Moreover, the capacitor used in the SC-integrator was as high as 100 pF to generate a 2.5 Hz cut-off corner. Pseudo-resistors feature extremely high incremental resistance (>10^{11} Ω) with small voltages (< 0.2 V) across them, which are good candidate for building large time-constant continuous-time integrator. Fig. 4.4 shows the configuration of the pseudo-resistor based integrator. In the design, pseudo-resistors are used to generate a sub-Hz high-pass cutoff instead of the SC resistors, which significantly saves the chip area. The high-pass cutoff is given by [55]

$$f_{hp} = \frac{C_{hp}}{C_{fb}} \cdot \frac{1}{2\pi R_{\text{int}} C_{\text{int}}} \tag{23}$$

where R_{int} is the equivalent resistance of the pseudo-resistors.

The second constraint is the trade-off between the available headroom and the noise contribution from the integrator. The available headroom with a fully differential feedback can be expressed as

$$V_{out\,\max} = \frac{C_{in}}{C_{hp}} \cdot V_{offset} \tag{24}$$

where V_{offset} is the maximum expected electrode offset and V_{outmax} represents the maximum differential output swing of the integrator. For wet electrodes, a maximum offset of ±50 mV can be expected [55], [76].

The noise contribution from the integrator referred to the amplifier input can be expressed as

$$v_{\text{int},RTI} = \frac{C_{hp}}{C_{in}} \cdot v_{\text{int}} \tag{25}$$

where $v_{int,RTI}$ is the input-referred noise contribution from the integrator, and v_{int} is the input-referred noise of the integrator. From equations (24) and (25), the noise contribution from the integrator can be reduced by decreasing C_{hp}. However, it would increase the output swing requirement of the integrator.

The electrode offset rejection (EOR) of the DC servo loop can be expressed as

$$EOR = \frac{C_{hp}}{C_{fb}} \cdot A_{\text{int}} \tag{26}$$

where A_{int} is the DC gain of the integrator. Current-mirror OTA could achieve wide output swing. However, it has four current branches and more noise contributors, and thus not noise-power efficient. Moreover, regular current-mirror OTA doesn't have high DC gain. The DC gain can be boosted by using cascoded output [27], which is at the expense of reduced output swing. In the design, a modified folded-cascode OTA is employed to achieve high DC gain while keeps desired output swing. Scaled-current technique [28] with a current scale of 3:1 is utilized to improve the power-efficient. The schematic of the OTA is shown in Fig. 4.5. The input transistors, as well as the PMOS, NMOS load transistors are sized relatively large to reduce their flicker noise. Since NMOS transistor has an order

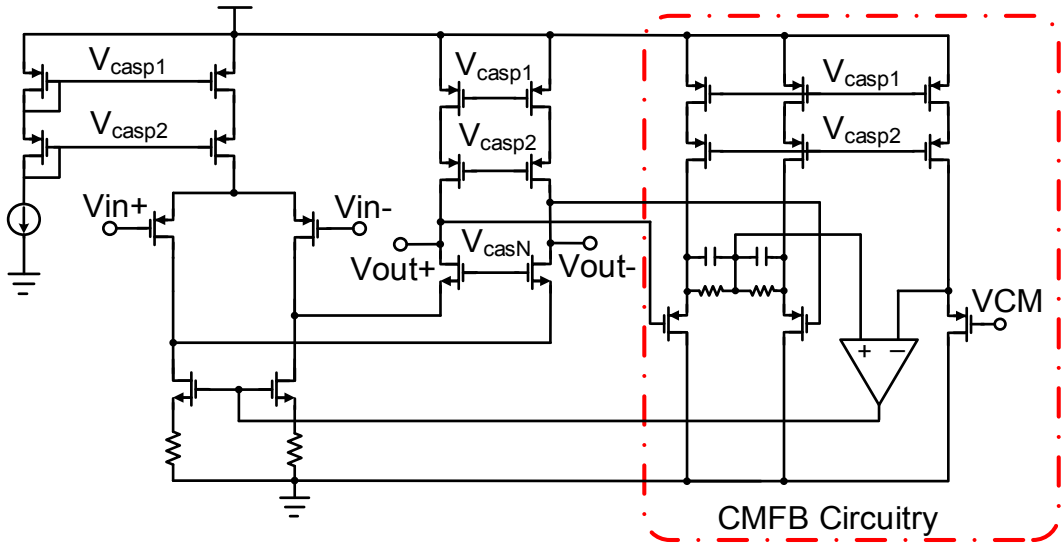


Fig. 4.5 Schematic of the OTA used in the large-time constant integrator.

magnitude higher flicker noise than PMOS [77], a source degeneration resistor of 300 kΩ is added to further reduce the flicker noise from the NMOS. The modified folded-cascode OTA in the design achieves a maximum differential output swing of 1.8 V (75% supply voltage). C_{hp} is chosen to be 235 fF to obtain a headroom of ±50 mV.

4.2.2.4 Input Impedance Boost Loop

Without the input impedance boost loop (IBL), the CCIA has limited input impedance defined by switched-capacitor equivalent impedance. The input impedance without IBL can be express as $1/(2f_cC_{in1})$. In the design, the simulated input impedance without IBL is around 4.3 MΩ, which could degrade the CMRR when there is mismatch between electrode source impedances [78]. To boost the input impedance, an impedance boost loop with positive feedback is employed [56]. This loop is composed of a chopper ($CH5$) and an adjustable capacitor bank (C_{ib}). The output voltage is up-modulated by the chopper and converted into a current by the sensing capacitor C_{ib} which is injected back

into th0e signal source. This current compensated for the current drawn from the signal source by the switched capacitor resistor, thus increasing the input impedance. In the ideal situation, this IBL generates feedback current exactly equal to the current draw from the signal source by the SC-resistor. Therefore, there is no input current drawn from the signal source, and the input impedance is infinite. In [56], to achieve infinite input impedance, the value of C_{ib} can be expressed as

$$C_{ib} = \frac{A_{CL,fir}}{A_{CL,fir} - 1} \cdot C_{fb} = \frac{C_{in}}{A_{CL,fir} - 1} \tag{27}$$

In the design, the closed-loop gain of the first-stage is set to be 100. With C_{fb}=41 fF, the ideal value of C_{ib} should be 41.52 fF to achieve infinite input impedance. However, in practice, the parasitic capacitances also need to be taken into consideration. The parasitic capacitance between the bottom plate of C_{in1} and ground forms a switched capacitor resistance with the input chopper, which would draw current from the input signals source. In a standard CMOS process, this parasitic capacitance can range from 10% to 40% of C_{in1}, thus needs to be compensated by C_{ib}. There is a threshold condition for the value of C_{ib} to maintain loop stability. If C_{ib} is made too large which leads to positive feedback of the whole loop, the input impedance is translated into negative impedance and the loop is unstable. The maximum value of C_{ib} for maintain loop stability can be expressed as

$$C_{ib} = \frac{C_{in} + C_P}{A_{CL,fir} - 1} \tag{28}$$

where C_p is the parasitic capacitance between the bottom plate of C_{in1} and ground.

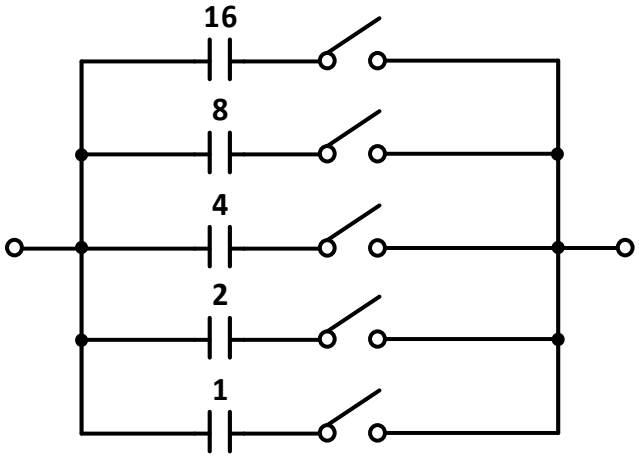
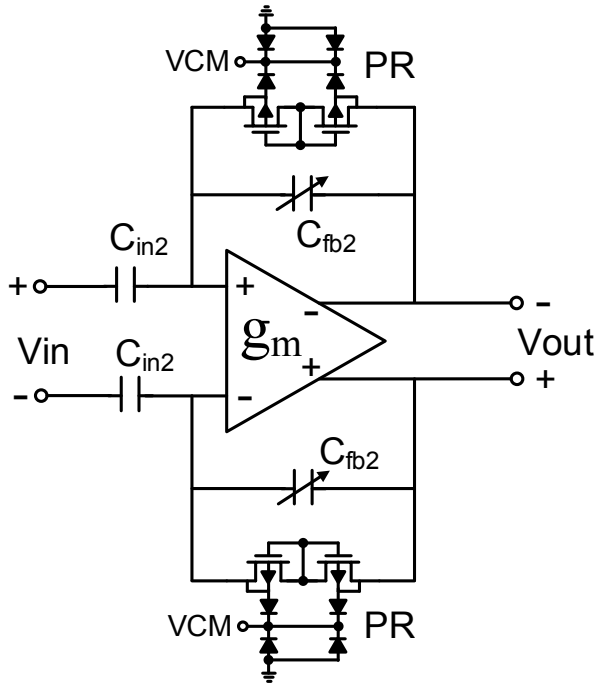


Fig. 4.6 Configuration of C_{ib} implemented by a binary capacitor array.

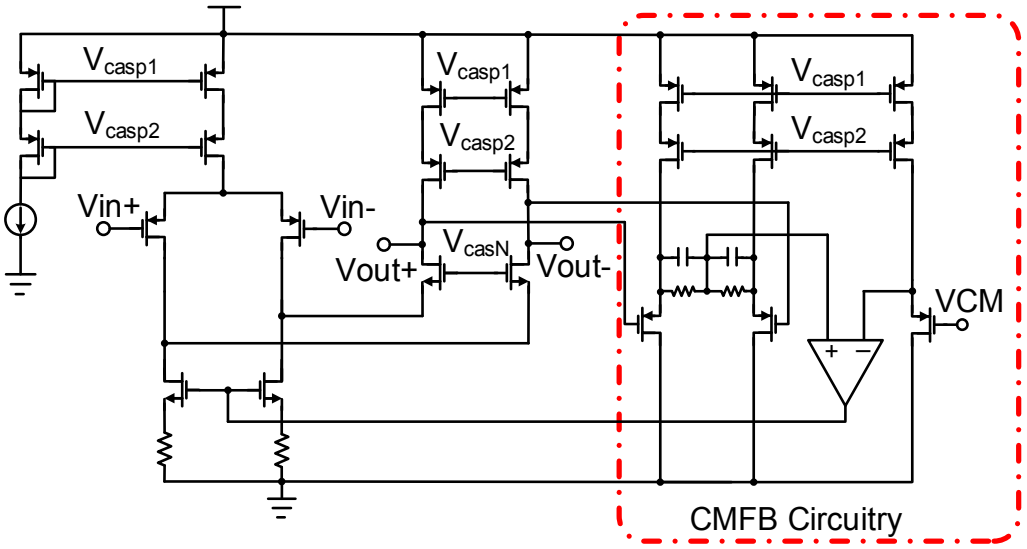
The variation of the parasitic capacitance of C_p and the wiring parasitic capacitance can not only reduce the effective input impedance boosting factor, but also may lead to potential instability. Therefore, C_{ib} is implemented as a binary capacitor array, as shown in Fig. 4.6, which allows to trim the amount of positive feedback to compensate the process variation and parasitic capacitance. The unit capacitance provided by the process is 1.86 fF, which is constructed from fingers of metal wires and vias.

4.2.3 Second-Stage VGA Design

Fig. 4.7 (a) shows the configuration of the second-stage variable gain amplifier (VGA). The second-stage is AC-coupled. Pseudo-resistors are employed to obtain a sub-Hz low-frequency high-pass corner. The pseudo-resistors also act like a reset switch. The closed-loop gain can be adjusted from 0~26 dB by using binary capacitor arrays. Fig. 4.7 (b) shows the schematic of the OTA for the VGA. Scaled-current technique [28] is employed to lower the current consumption from the load branches. The input branches consumes major current to provide sufficient bandwidth.



(a)



(b)

Fig. 4.7 (a) Configuration of the second-stage VGA. (b) Schematic of the folded-cascode OTA of the VGA.

Although the first-stage has mid-band gain of 40 dB, the low-frequency noise of the second-stage still needs to be minimized. The input as well as PMOS and NMOS load transistors are sized relatively large to reduce the flicker noise. Besides, source degeneration technique is utilized to further minimize the low-frequency noise from NMOS loads.

4.2.4 2nd-Order LPF Design

I would like to thank my previous colleague, Junjie Lu, for helping me with the design of a second-order Gm-C filter which is used to filter out the up-modulated low-frequency noise and offset, and also to tune the cut-off corner. The filter incorporates linear tunable pseudo-differential transconductors, which are based on transistors biased in triode region. A common-mode feedback (CMFB) circuit is designed to maintain suppression of CM component across the entire range of output swing. Both the architecture and circuit design are optimized specifically for bio-signal acquisition application with wide tuning range, high dynamic range and low power consumption.

4.2.4.1 Transconductor Cell Design

In a Gm-C filter, the transconductors are required to have good linearity with large differential signal input, and tunable transconductance. Common linearization techniques include source degeneration [79], bias offset [80] and source coupling [81]. The tunability can be achieved by tunable active resistor [82], or current division [83]. Apart from these techniques, transconductors based on transistors biased in triode region are good candidates as they show good linearity and wide tuning range with low circuit complexity.

For a transistor biased in triode region, its drain current is given by

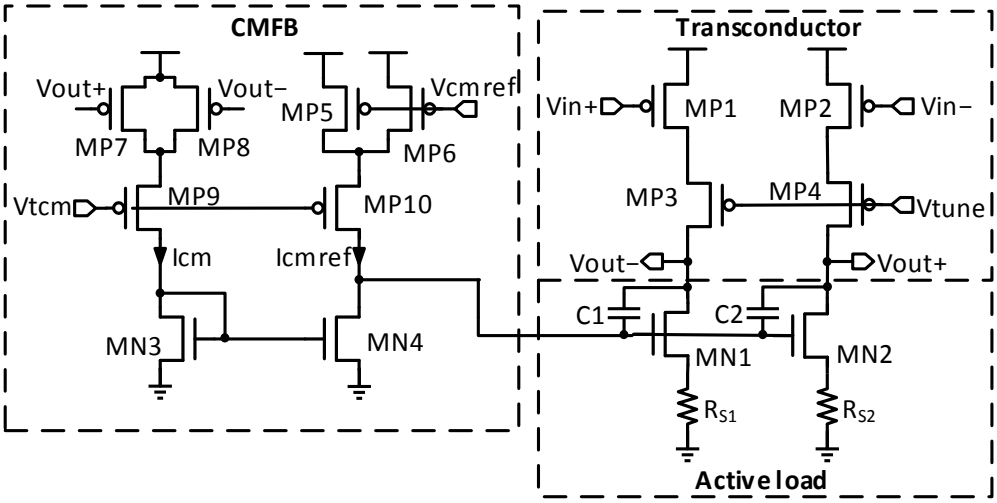


Fig. 4.8 Simplified schematic of the transconductor cell.

$$I_D = \mu C_{OX} \frac{W}{L} V_{DS} (V_{GS} - V_T - \frac{V_{DS}}{2}) \tag{29}$$

where μ is the mobility, C_{OX} is the unit gate capacitance and V_T is the threshold voltage.

The transconductance is then obtained by taking derivative of I_D to V_{GS}

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{OX} \frac{W}{L} V_{DS} \tag{30}$$

indicating that g_m is independent of V_{GS}, and tunable by V_{DS}.

The simplified schematic of the transconductor is shown in Fig. 4.8. *MP*1/*MP*2 is the input transistor biased in triode region by the cascode transistor *MP*3/*MP*4. V_{tune} determines the V_{DS} of input transistors therefore the g_m of the transconductor. Transistor *MN*1/*MN*2 and its degeneration resistors $R_{S1,2}$ acts as active load, whose current is controlled by the CMFB circuit.

The design of CMFB circuit in a linear transconductor is not trivial, as the CM path needs to be as linear as the differential mode (DM) one to maintain good suppression of

CM component and interference. The commonly used CMFB circuit using differential pairs [84] is not adequate in this application because the large differential swing at the output can completely turn off one input transistor and cause non-linearity. The proposed CMFB circuit uses similar structure as the DM path and therefore offers comparable linearity. Triode transistors *MP*7/*MP*8 convert the output voltages to CM currents I_{cm}. I_{cm} is then mirrored by *MN*3/*MN*4 and compared to I_{cmref}, which is a current generated from the CM reference voltage V_{cmref} by *MP*5/*MP*6. *MP*5-8 have the same aspect ratio the negative feedback loop stabilizes the CM output to V_{cmref}. Capacitor C_1/C_2 provides frequency compensation to ensure the stability of the loop.

In the frequency band of interest, the dominant noise source is the flicker noise in MOSFETs. Therefore, in order to eliminate this noise, the transistors are sized relatively large and source degeneration technique is employed. For the input devices, PMOSs are used because it shows much lower flicker noise than NMOSs in this process. Proper design ensures that the noise in the active load is dominated by the resistor R_S, and the input referred noise power is given by

$$v_{n,in}^2(f) = v_{n,p}^2 + \left(\frac{1}{g_{m,p}}\right)^2 \left(v_{n,\mathrm{cas}}^2 g_{ds,p}^2 + \frac{4kT}{R_S}\right) \tag{31}$$

where $v_{n,p}^2$, $g_{m,p}$ and $g_{ds,p}$ are the input referred noise power, transconductance (given by (30)) and drain conductance of the input device *MP*1/*MP*2, respectively, $v_{n,cas}^2$ is the input referred noise power of the cascode device *MP*3/*MP*4, k is the Bolzsmann constant and T is the temperature in Kelvin. Assuming that V_{DS} is small enough that the channel is homogeneous, $v_{n,p}^2$ can be expressed as

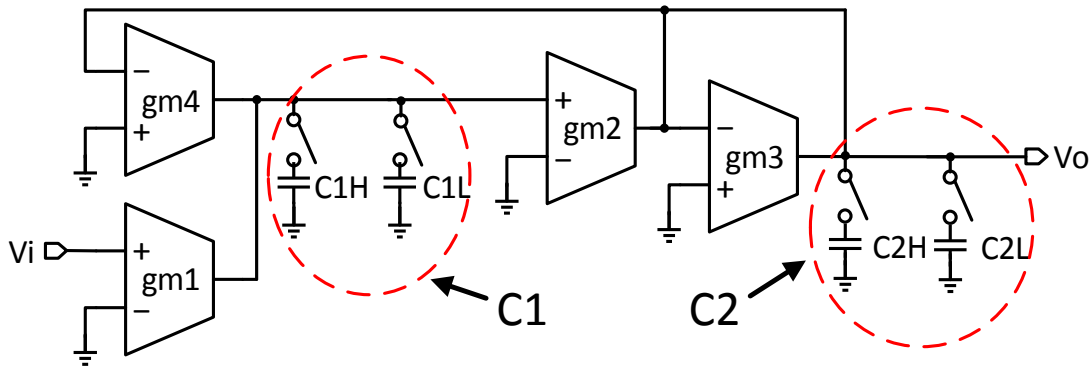


Fig. 4.9 2nd-order low-pass filter structure.

$$v_{n,p}^2 = \frac{4kT}{g_{m,p}}\left(\frac{V_{GS}-V_T}{V_{DS}}\right)+\frac{K_f}{C_{OX}WLf} \tag{32}$$

where K_f is the flicker noise coefficient. It can be seen from equations (31) and (32) that there are direct trade-offs between noise and power/area: as we increase $g_{m,p}$ to reduce noise, power consumption increases and the capacitance in the filter also needs to increase to maintain the same corner frequency. Therefore, optimization was performed to meet the system dynamic range and SNR requirement, while keeping the power and area to their minimum.

4.2.4.2 Overall Design

The proposed transconductor cell is used to implement a second-order low-pass filter. The filter design adopts the Biquad structure and its schematic is shown in Fig. 4.9. It can be shown that the filter has a transfer function of

$$H(s) = \frac{Vo(s)}{Vi(s)} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m3}}{C_2} + \frac{g_{m2}g_{m4}}{C_1C_2}} \tag{33}$$

$g_{m1\text{-}4} = g_m$ was chosen to facilitate matching. The filter's cut-off frequency (f_c) and quality factor (Q) are given by

$$f_c = \frac{g_m}{2\pi\sqrt{C_1 C_2}} \tag{34}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{35}$$

Note that Q is determined by the capacitor ratio therefore can be very accurate. To get a maximal flatness in the passband, Butterworth type is chosen and Q = 0.707. f_c is tunable by tuning g_m, while Q is unaffected by this tuning. C_1 and C_2 could be either C_{1H}, C_{2H} or C_{1L}, C_{2L} so that the cut-off frequency can be tuned from 1.2 to 7 kHz and from 70 to 400 Hz by combining with tuning the transconductance.

As shown in Fig. 4.9, g_{m1} and g_{m4} share the same output nodes, so does g_{m2} and g_{m3}. Therefore, each pair can share their cascode transistors, active loads and CMFB circuits, significantly reducing the area and power consumption of the filter system. Fig. 4.10 shows how two transconductors can be combined to a single transconductor with two inputs.

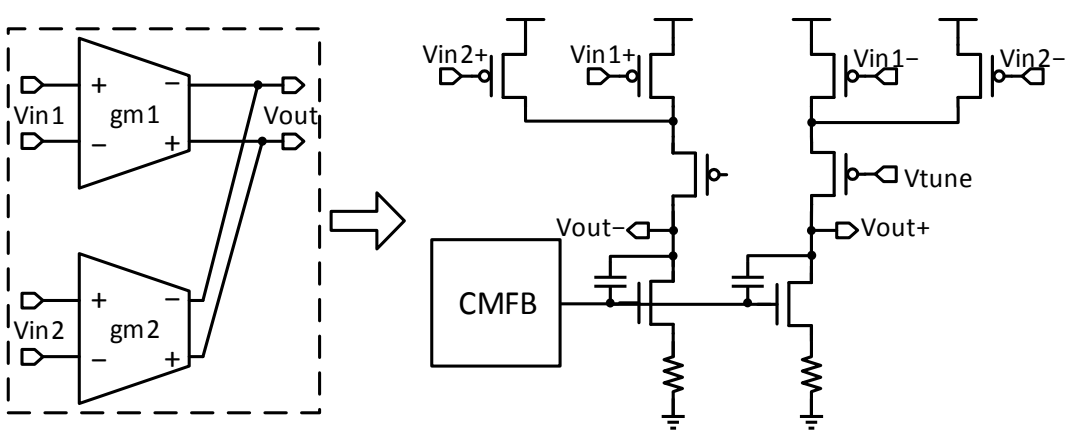
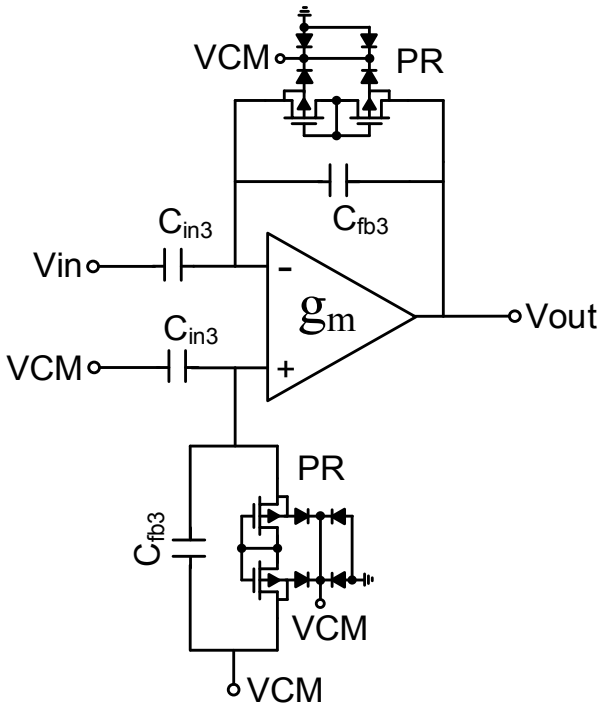
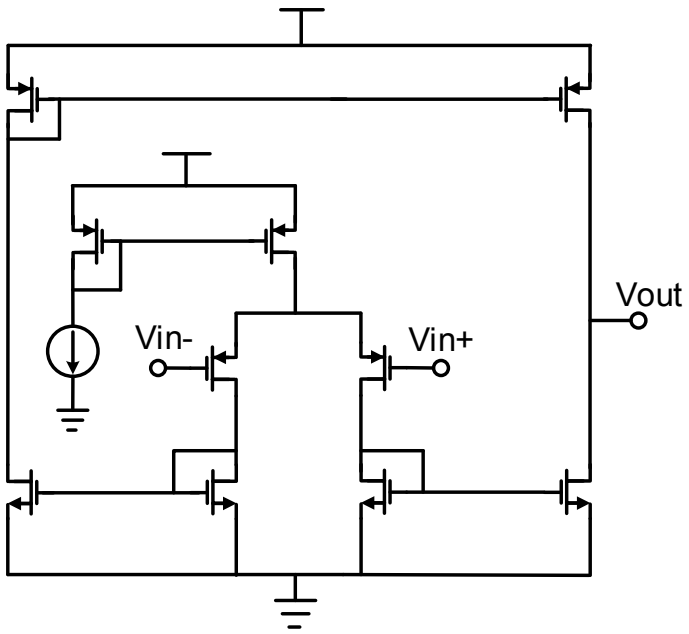


Fig. 4.10 Combination of two transconductors to share the load and CMFB.



(a)



(b)

Fig. 4.11 (a) Configuration of the third-stage amplifier. (b) Schematic of the OTA used in third-stage.

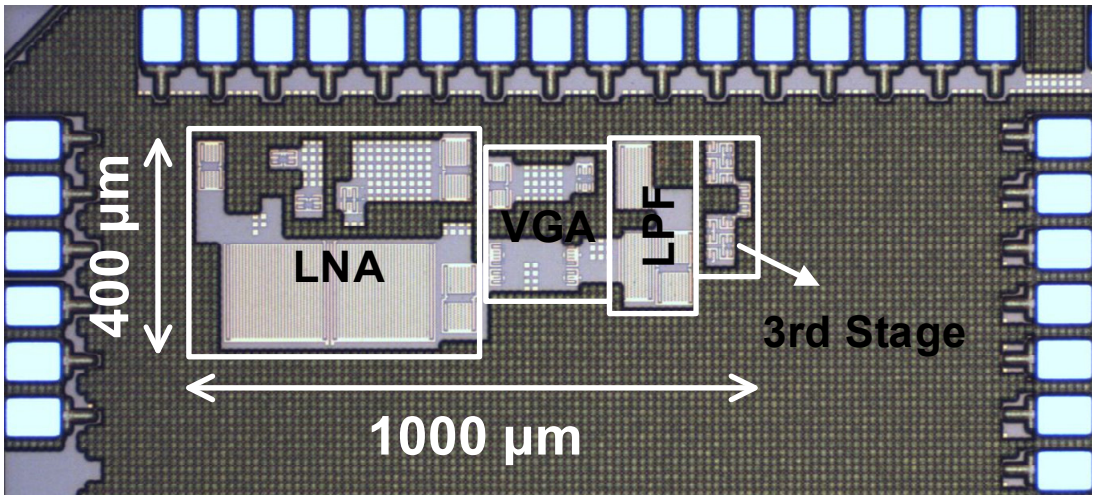


Fig. 4.12 Die microphotograph of the proposed AFE.

4.2.5 Third-Stage Amplifier Design

Fig. 4.11 (a) shows the configuration of the third-stage amplifier. The third-stage is AC-coupled. Pseudo-resistors are employed to obtain a sub-Hz low-frequency high-pass corner. The pseudo-resistors also act like a reset switch. The closed-loop gain is fixed of 6 dB by using capacitive feedback. Fig. 4.11 (b) shows the schematic of the OTA for the third-stage. Current-mirror OTA is employed to achieve wide output swing. The details are not critical to the operation of the design and will not be presented here.

4.3 Bench Measurement Results

The AFE is fabricated in a 0.13 µm CMOS process. The die microphotograph is shown in Fig. 4.12. The active area is 400 µm × 1000 µm. The AFE draws 4.4-4.9 µA from a 1.2 V supply. Table III shows the current consumption of each block.

Table III Current Consumption of Each Block in AFE.

	1st-stage LNA	2nd-stage VGA	LPF	3rd-stage Amp	Total
Current (μA)	3.0	0.9	0.3-0.8	0.2	4.4-4.9

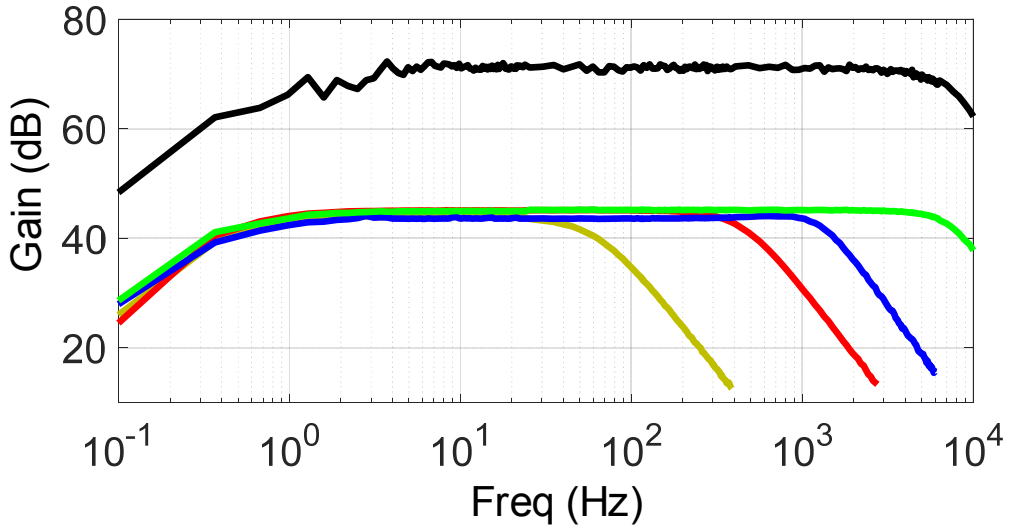


Fig. 4.13 Measured transfer function.

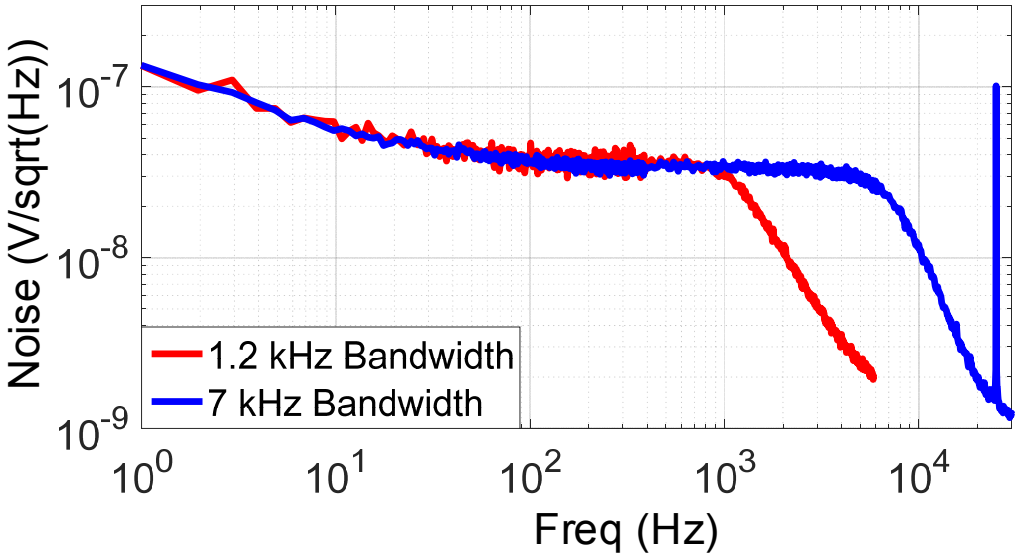


Fig. 4.14 Measured input-referred noise at the gain of 66 dB.

Table IV Performance Comparison

	[55] JSSC 2007	[59] JSSC 2013	[71] JSSC 2012	[75] JSSC 2012	[51] JSSC 2012	This work
Supply (V)	1.8	1.8	0.5	1.2	3.3	**1.2**
Power (μW)	1.8*	8.25*	5.05	35	73.9*	**5.3-5.9**
Gain (dB)	41, 50.5	52-80	32	40, 56	46, 66	**45.2-71**
Noise (μV_{rms})	0.98 (.05-100 Hz)	0.91 (.5-100 Hz)	4.3 (300 Hz) 4.9 (10 kHz)	14 (1-100 Hz) 2.2 (280-10 kHz)	0.9 (1-200 Hz) 3.3 (200-10 kHz)	**0.45 (1-100 Hz) 2.93 (1 Hz-7 kHz)**
NEF	4.6	5.1	6.0	4.5 (280-10 kHz)	7.6	**3.7 (1-100 Hz) 3.0 (1 Hz-7 kHz)**
PEF ($NEF^2 \cdot VDD$)	38*	47 *	18	24* (280-10 kHz)	190*	**16.4 (1-100 Hz) 10.8 (1 Hz-7 kHz)**
Bandwidth (Hz)	0.05-100	0.5-100	300, 10k	sub-Hz to100, 280-10k	0.1-200, 200-10k	**f_H <1, f_L=70-400, 1.2k-7k**
Z_{in} (MΩ)	8	>500	$1000 \| C_{in}$	—	100 (1-200 Hz) 320@1 kHz	**>100**
THD @1mV_{pp}	< 0.1%	—	>2%	—	< 0.1%	**<1%**
CMRR (dB)	>100	—	75	—	>110	**>95**
Area (mm^2)	1.7	—	0.013	0.26	0.15	**0.4**
Process (μm)	0.8	0.18	0.065	0.13	0.35	**0.13**

*The value is calculated based on the reported performance.

Fig. 4.13 shows the measured transfer function of the AFE. The high-pass cutoff is around 0.7 Hz. The low-pass cutoff is tunable in the range of 70-400 Hz and 1.2-7 kHz.

The input-referred noise the proposed AFE is shown in Fig. 4.14. The thermal noise density is 34 nV/sqrt(Hz). The flicker noise corner is down to 25 Hz by using chopper technique. When the AFE is configured for AP recordings (0.7 Hz-7 kHz), the input-referred noise is 2.93 μVrms integrated from 1 Hz to 50 kHz, corresponding to a NEF of 3.0. When configured for EEG recordings (0.7-100 Hz), the input-referred noise is 0.45 μVrms, corresponding to a NEF of 3.7.

The proposed AFE is compared with previous work in Table IV. To facilitate comparison, the noise efficiency factor (NEF) [70] and the power efficiency factor (PEF) [71] are adopted, which are widely utilized as the figure-of-merit to evaluate biopotential AFEs. Compared with other benchmarks, the proposed AFE exhibits the lowest noise in

EEG band (1-100 Hz). It achieves the best NEF and PEF in EEG band compared with other benchmarks, which indicates the highest noise-power efficiency in EEG band. The linearity of the proposed AFE is worse than the AFEs in [55] and [51]. This is partly due to the lower supply voltage we use.

4.4 Biological Measurement Results

To demonstrate the performance, the AFE is used to obtain the recordings of several biopotential signals.

Fig. 4.15 shows recorded human EMG signals during repeated arm extensions.

Fig. 4.16 shows recorded human ECG signals.

Fig. 4.17 shows the normalized spectrum of the measured EEG during eyes open and eyes closed. The dry electrodes are placed in positions of O1 and Cz of the head using the international 10-20 electrode placement system. Alpha waves (8-12 Hz) are clearly visible when the subject's eyes are closed and mentally relaxed, and are suppressed when eyes are open.

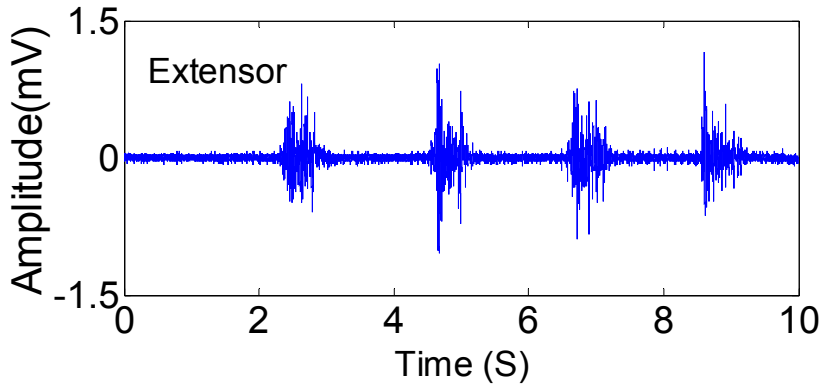


Fig. 4.15 Human EMG recordings.

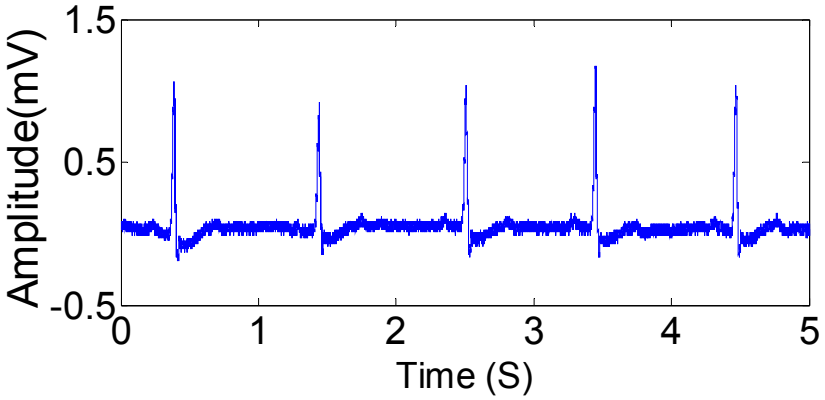


Fig. 4.16 Human ECG recordings.

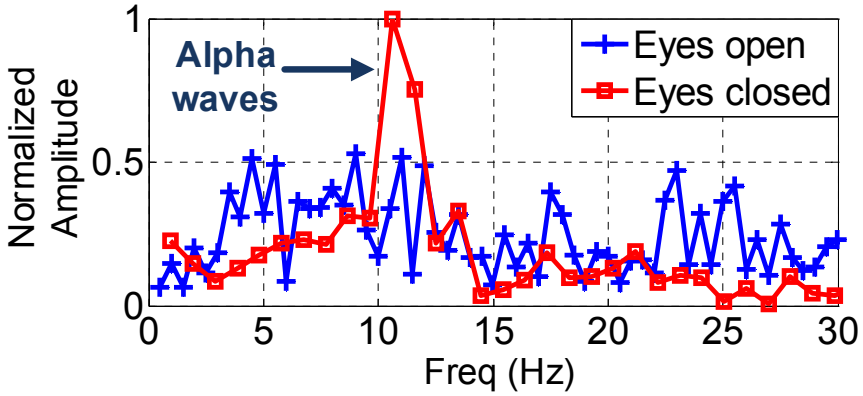


Fig. 4.17 Human EEG recordings during eyes open and eyes close.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

This dissertation presents the design of low-power low-noise amplifiers for biopotential applications. The main conclusions are summarized below.

First, I proposed a design strategy for a neural recording amplifier array with ultra-low-power low-noise operation that is suitable for large-scale integration. The topology combines a highly efficient but supply-sensitive single-ended first stage with a shared reference channel and a differential second stage to effect feed-forward supply noise cancellation, combining the low power of single-ended amplifiers with improved supply rejection. The amplifier is fabricated in a 90 nm CMOS process and occupies 0.137 mm^2 of chip area. For a two-channel amplifier, the measurements show a mid-band gain of 58.7 dB and a pass-band from 490 mHz to 10.5 kHz. The amplifier consumes 2.85 μA per channel from a 1-V supply and exhibits an input-referred noise of 3.04 μV_{rms} from 0.1 Hz to 100 kHz, corresponding to a noise efficiency factor (NEF) of 1.93. The PSRR of at least 50 dB is sufficient for typical recording scenarios. The NEF can be further improved when the reference amplifier is shared by more channels. Additionally, the 1 V supply is well suited for integration with low-power digital circuitry in complex systems-on-chip.

Second, I proposed a configurable analog front-end (AFE) for the recordings of a variety of biopotential signals, including electromyography (EMG), electrocardiogram

(ECG), electroencephalogram (EEG), action potential (AP) signals, etc. The first stage of the AFE employs a chopper-stabilized current-reuse complementary input (CRCI) telescopic-cascode amplifier to achieve high noise-power efficiency and suppress 1/*f* noise. A tunable impedance-boosting loop (IBL) is utilized, which is robust to process variation and parasitic capacitance and increases the input impedance from 4.3 to 102 MΩ. The proposed AFE is fabricated in a 0.13 μm CMOS process. The AFE has a mid-band gain from 45.2-71 dB. The low-pass corner is tunable in the range of 70-400 Hz and 1.2-7 kHz. When configured for EEG recordings (0.7-100 Hz), the AFE draws 5.4 μW from a 1.2 V supply while exhibiting input-referred noise of 0.45 μVrms, corresponding to a noise efficiency factor (NEF) of 3.7. When configured for AP recordings (0.7 Hz-7 kHz), the AFE consumes 5.9 μW with input referred noise of 2.93 μVrms and a NEF of 3.0.

5.2 Future Works

Future works that can make improvements are summarized below.

First, the two-stage amplifier array can be implemented with more channel-count. This will further improve the noise-power efficiency and reduce the silicon area per channel. A large scale amplifier array can be used with multi-electrode array for neural recordings.

Second, the area of the configurable AFE can be reduced. Significant area of the AFE is occupied by the passive devices like resistors and capacitors. In the OTAs in large-time constant integrator and the second-stage VGA, large resistors are used in CMFB circuitry to provide sufficient output swing. Switched-capacitor CMFB can be used to implement large output swing without using large resistors, which could save the area.

Third, the configurable AFE can be designed to have different power mode for corresponding biopotential recordings. Current DAC can be used to tune the bias current of the AFE. In low-power mode, AFE can be used for the recordings of high-amplitude level of biopotentials, such as EMG, ECG, etc. In high-power mode, AFE can be used for the recordings of low-amplitude level of biopotentials, such as EEG, AP, etc.

Finally, the AFE can be implemented in multi-channel configuration and integrated with an ADC and a wireless transmitter as a system-on-chip. This will provide an area- and power-efficient system solution for wearable/implantable biomedical devices.

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