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Date 3-17-94

THE DESIGN OF A CONSTANT CURRENT MUSCLE STIMULATOR

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Barry Edward Martin

May 1994

DEDICATION

I would like to dedicate this thesis
to my wife Diane and my daughter Candace.
Without their love, support, and encouragement,
this work would not have been possible.

ACKNOWLEDGEMENTS

I would like to thank Dr. James M. Rochelle, who served as my major professor, for his guidance and assistance throughout this project, and the other members of my committee, Dr. T. V. Blalock and Dr. Igor Alexeff, for their advice and suggestions. I would also like to thank my Mother and Father: David and Fay Martin for their assistance with and support of this work. I would also like to express my thanks to my wife and daughter, Diane and Candace: Diane for her support and encouragement during this work and for her assistance in writing the dedication, and Candace, a five year old wise beyond her years for understanding why "Daddy" had to work instead of play.

ABSTRACT

An instrument that produces two constant current sinusoidal signals for use in the treatment of muscular disorders in human patients was designed, developed, and evaluated. The instrument will produce 50mA rms per channel into a patient load at user selectable carrier frequencies of 2.5KHz or 5.0KHz. The instrument provides a beating effect by allowing the frequency of one channel to track the frequency of the other within a range of 1Hz to 200Hz, with the exact point in this range controlled by the user.

The instrument uses analog signal processing circuits to generate and shape the output signals, remove unwanted components, and produce high spectral purity outputs. The instrument provides isolated, constant current output signals on each channel and a maximum treatment time of sixty minutes. The instrument provides a modulated treatment mode which produces an amplitude modulated current signal on each channel to allow treatment of separate locations simultaneously. Circuitry that resets the instrument in the event of a treatment mode change or power failure is included to insure patient safety. Although every effort has been made to insure patient safety, not all possible safety issues have been addressed.

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CHAPTER 1

INTRODUCTION

1.1 Physiological Background

The use of electrical stimulation to treat various disorders of the human body is well known. In order to understand the mechanism by which an electrical current speeds recovery of damaged tissues, it is necessary to have an understanding of the electrical nature of living tissues on the cellular level. Therefore, it is the purpose of this section to describe the types of electrical potentials that exist at the cellular level.

A typical nerve or muscle cell is composed of a membrane that separates the intracellular contents from the cells environment. There exists an electrical potential across the cell boundary that is produced by differing concentrations of sodium (Na) and potassium (K) ions. Measurements of this potential record values of 60 to 90 millivolts [1], the outside of the cell being positive with respect to the inside, with the cell in an undisturbed state. In an undisturbed cell, the concentration of K is higher inside the cell and the concentration of Na is higher outside the cell. This concentration difference is a result of the fact that the cell boundary presents a greater permeability to K than to Na. Given this concentration difference, Na and K ions will try to passively diffuse across the cell boundary in an attempt to equalize the charge distribution. This diffusion process is more successful for K because of its higher permeability, and a steady state condition is eventually reached at a potential of 60 to 90 millivolts. This type of potential is known as a resting membrane potential [2] due to the fact that the cell is at rest when this

potential is present.

Most cells spend little time in a rest condition because they are continuously subjected to neural transmitters and sensory stimuli that cause the cells permeability to Na and K to increase. This increase in permeability is different in magnitude and rate for Na and K respectively. Normal stimuli will initially cause an increase in the cells permeability to Na which increases the number of Na ions moving into the cell. As the number of Na ions in the interior of the cell increases, the cell potential will be reduced. This process is known as depolarization [3]. If the cell potential reaches a certain threshold level, a level which is highly dependent on the type of cell in question, permeability to Na will increase rapidly and Na ions will rush into the cell. This causes a rapid reversal of potential across the cell membrane to approximately 30 millivolts [4], the outside of the cell negative with respect to the inside. The initial change in permeability to Na is accompanied by a smaller and delayed increase in permeability to K. These increases in permeability last for only a very brief time (milliseconds, depending on the type of cell) before cell metabolic processes restore the concentrations to their equilibrium value, and the cell to its resting potential. This quick reversal of cell potential magnitude and polarity is known as an action potential [5]. Any type of cell capable of discharging an action potential is defined as an excitable cell or membrane. Any type of cell that is not capable of discharging an action potential is known as a non-excitable cell or membrane. Cells or tissues can be classified according to their excitability as shown in Table 1.1 [6].

Table 1.1

Tissue Excitability Classification

Excitable Tissues	Non-Excitable Tissues
Nerve cells	Bone
Nerve axons	Cartilage
Voluntary motor fibers	Collagen tissues
Cardiac muscle fibers	Ligamentous tissue
Abdominal organ cells	Tendon tissue
Cells which produce a glandular secretion	

1.2 Interferential Currents

An immediate conflict arises when designing an electrical stimulator to artificially induce action potentials in excitable tissue; (1) Human skin presents a high impedance to the flow of dc or low frequency currents, and (2) action potential frequencies span this low frequency range. One solution to these conflicting design requirements was proposed by Dr. Hans Nemec [7] in the mid 1950's. Dr. Nemec proposed using two medium frequency sinusoidal current waveforms differing in frequency by a few hundred hertz. This allows use of carrier frequencies that make skin impedance negligible while providing stimulus in the action potential frequency range.

Interferential currents are generated by applying two sinusoidal currents in the configuration shown in Figure 1.1. It should be noted that this is the current distribution and areas of maximum stimulation (points labeled A) for a homogeneous medium. These current frequencies are typically in the 1KHz to 10KHz range. One is a fixed frequency f_1 , the other a variable frequency f_2 , where $f_2 = f_1 - [1\text{Hz} \leftrightarrow 200\text{ Hz}]$. As an example, one channel could be 5KHz fixed, while the other would be variable from 4.800KHz to 4.999KHz. The two signals are modulated within the tissues to produce an amplitude modulated current with an envelope or beat frequency of 1Hz to 200Hz. The two applied sinusoids and the resultant amplitude modulated waveform are shown in Figure 1.2. Note that the peak amplitude of the envelope is twice as large as the amplitude of the individual currents.

The area of maximum stimulation is static and can only be changed by moving

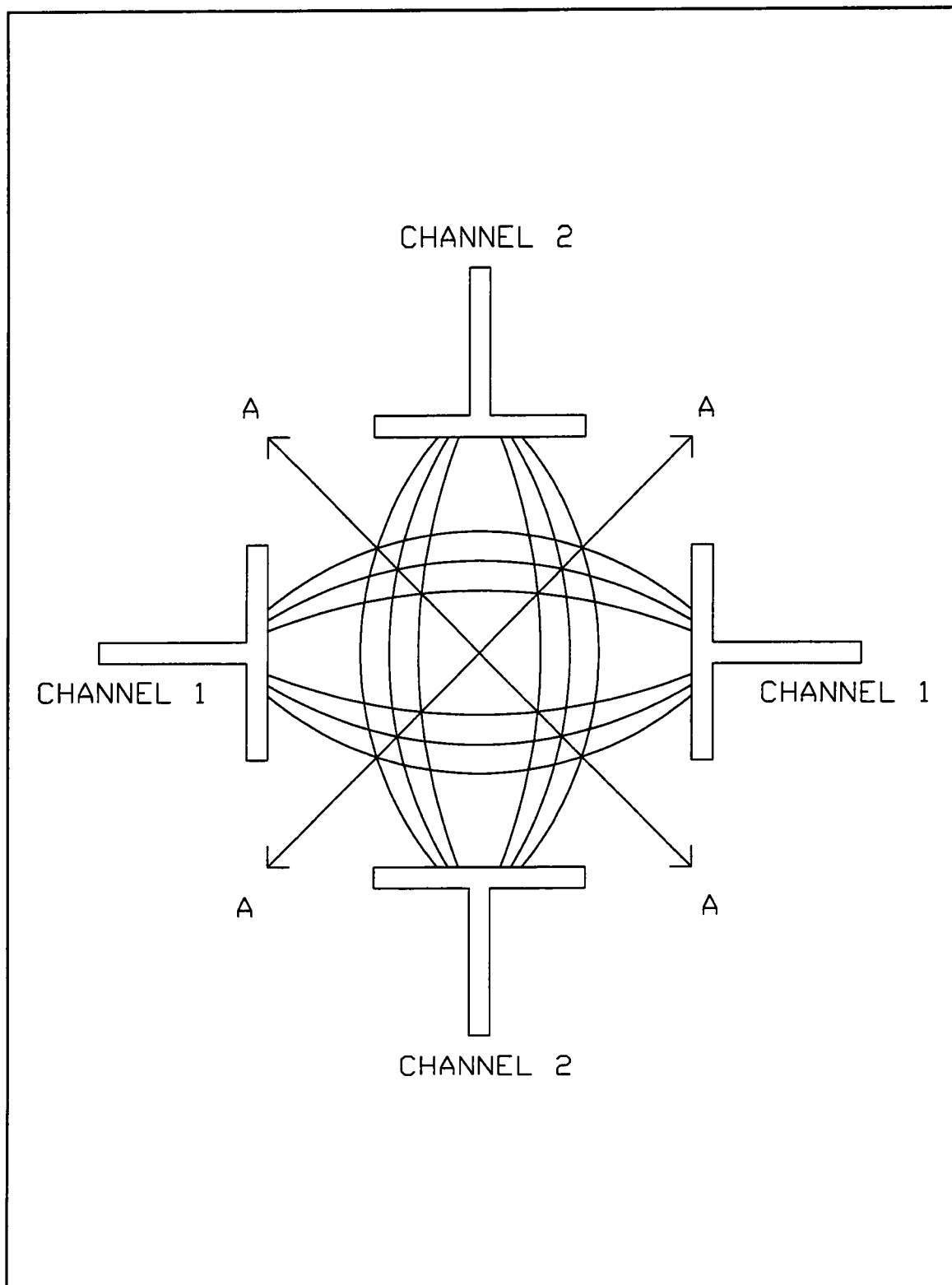
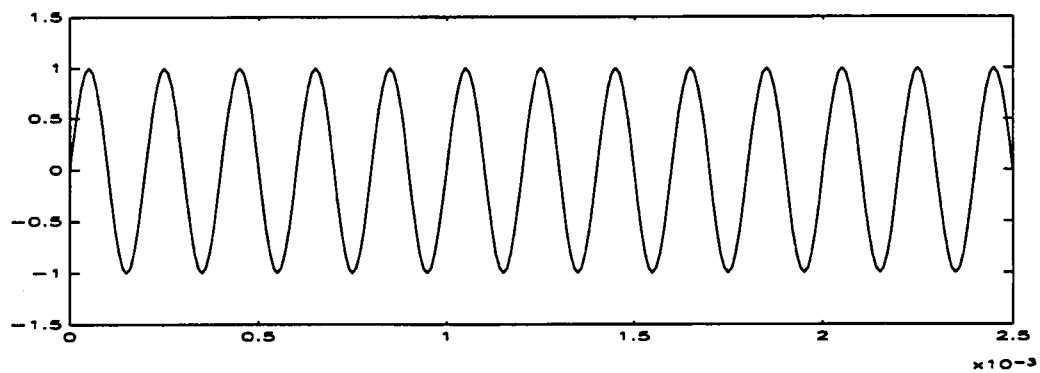
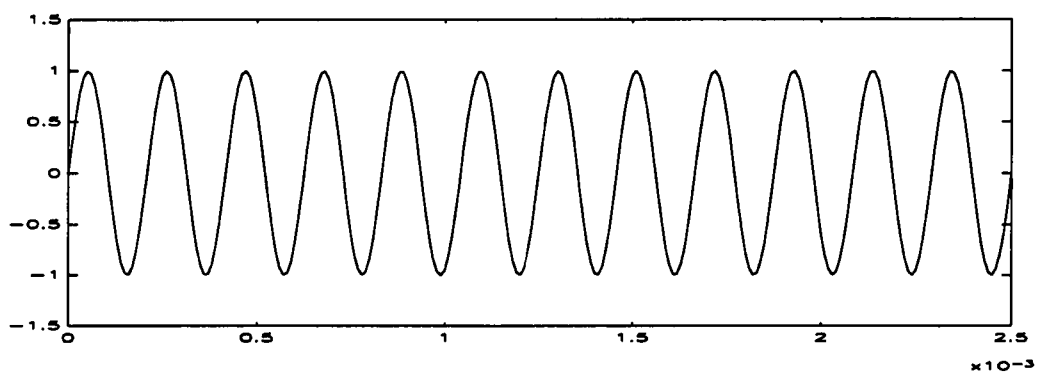


Figure 1.1. Electrode placement for the generation of interferential currents.



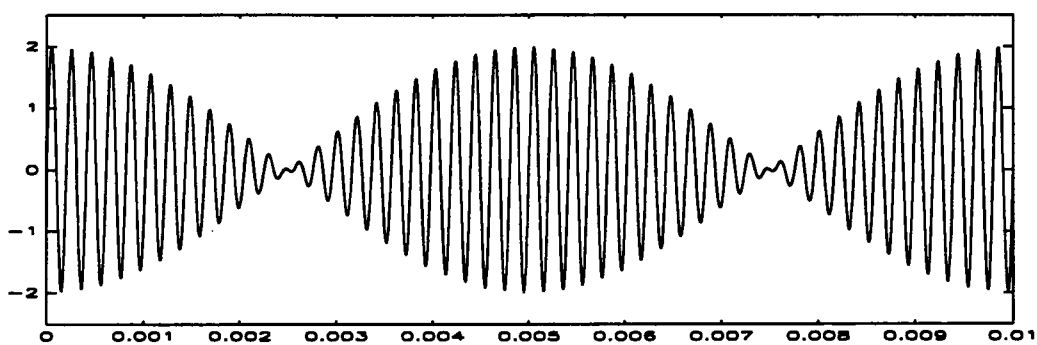
5KHz (CHANNEL 1)

(A)



4.8KHz (CHANNEL 2)

(B)



RESULTANT

(C)

Figure 1.2. Interferential waveforms.

the electrodes. An alternative to this is to change the percent modulation of the resultant waveform by increasing the amplitude of one channel and at the same time decreasing the amplitude of the other. Depending on which one is increased/decreased, the area of maximum stimulation can be rotated through an angle that depends on the percent modulation. For example, (refer to Figure 1.1) if the amplitude of channel 1 is increased to 1.5 (normalized) and the amplitude of channel 2 is decreased to 0.5, the area of maximum stimulation will be rotated 45° counterclockwise. This is equivalent to decreasing the percent modulation from 100% (equal amplitude currents) to 50%. The resultant waveform in this case is shown in Figure 1.3. There is no clinical evidence that this type of waveform provides an improvement over a static waveform and will not be discussed further.

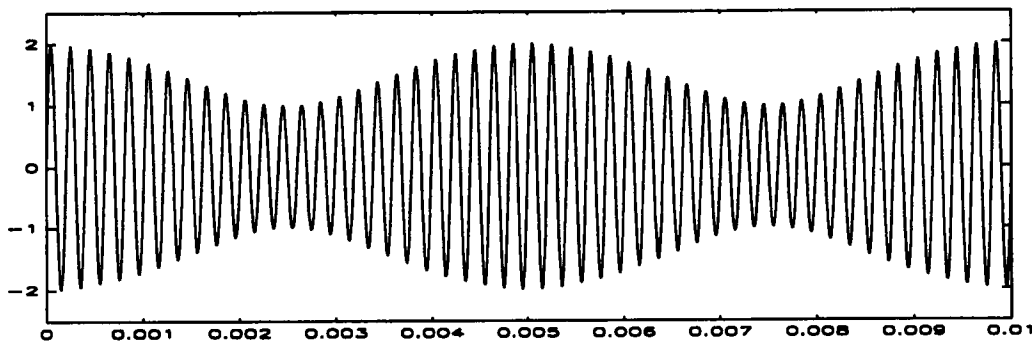


Figure 1.3. Dynamic interferential waveform.

1.3 Thesis Overview

The instrument outlined in Figure 1.4 was developed and tested. This instrument produces two, isolated, constant current sinusoids to be applied to the patient as shown in Figure 1.1. Channel 1 has a user selectable carrier frequency of either 2.5KHz or 5KHz. Channel 2's frequency tracks channel 1 in the following manner: if the carrier frequency is set to 5KHz, channel 2 will be in the range of 4.8KHz to 4.999KHz; if the carrier frequency is set to 2.5KHz, channel 2 will be in the range of 2.3KHz to 2.499KHz. The location of channel 2 within either of these ranges is set by the user with a front panel control (beat frequency potentiometer). Switching between carrier frequencies does not alter the beat frequency setting. For example, if the carrier frequency is set to 5KHz and the beat frequency is set to 100Hz (channel 2's frequency is 4.9KHz), and the user selects the 2.5KHz carrier frequency, channel 2's frequency will be 2.4KHz, resulting in a beat frequency of 100Hz.

An alternative is provided to the standard four electrode setup, namely the ability to amplitude modulate both channel's individually. This results in the waveform shown in Figure 1.2 (C) appearing at both channel 1 and 2, and allows use of only one channel (two electrodes as opposed to four) or the simultaneous treatment of two different locations.

Irrespective of the treatment mode or carrier frequency selected, the user always has control of the following parameters; (1) output amplitude, (2) output carrier frequency, (3) modulated or unmodulated, (4) beat frequency, (5) output current display

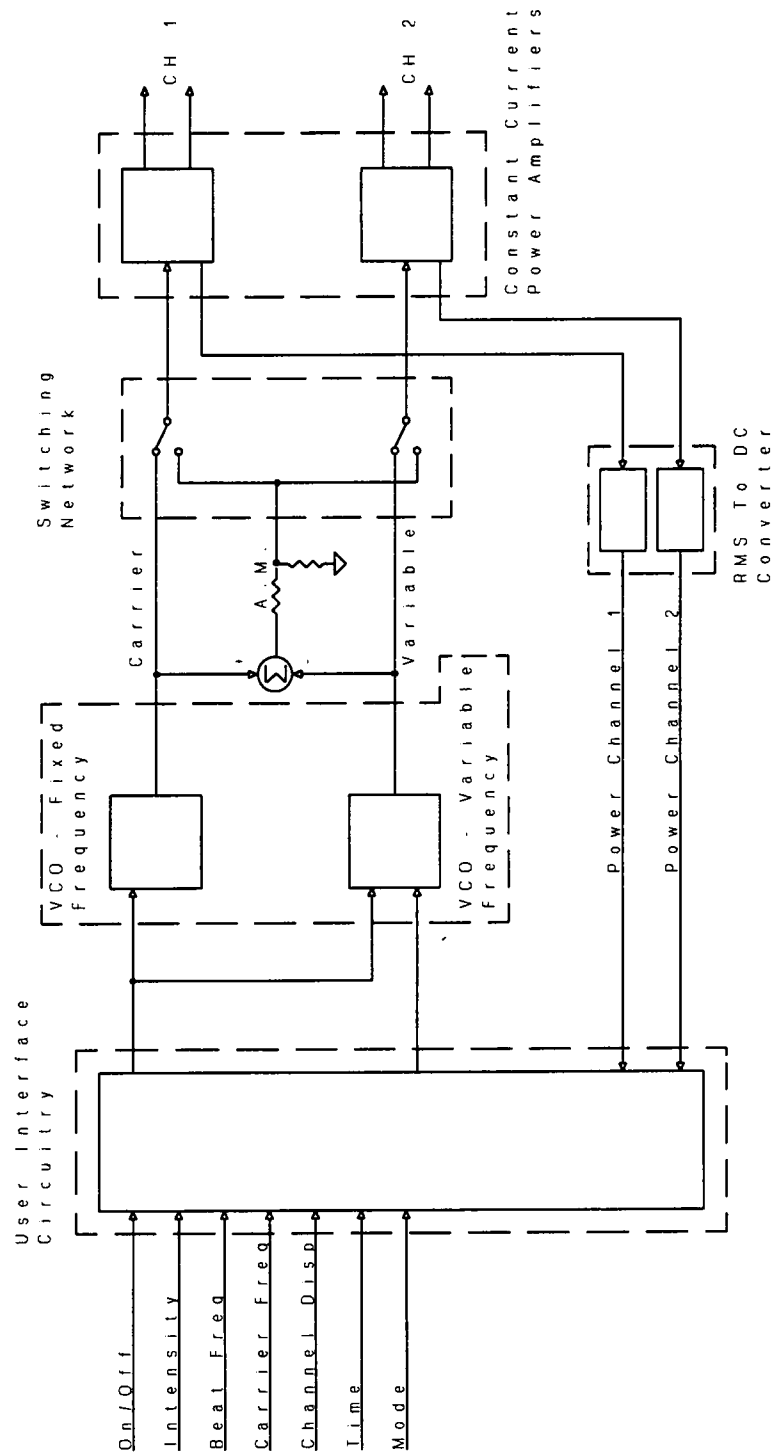


Figure 1.4. Instrument overview.

(channel 1 or channel 2, measured in rms), treatment time (up to sixty minutes), and start/stop treatment.

Given the numerous treatment modes available in this instrument, and the fact that the same patient may respond differently to different treatment modes, safety is a prime consideration. Safety circuitry is included so that any time a treatment mode is changed, the output current is reduced to zero. In order to restore the output, the output amplitude control (intensity control) must be set to zero before the instrument will respond to new inputs. For example, a typical treatment mode could be the following parameters: carrier frequency = 5KHz, output amplitude = 20mA rms, beat frequency = 50 Hz, modulation = unmodulated (four electrode setup); if the user now decides to use a carrier frequency of 2.5KHz and selects this parameter, the instrument will respond to this new setting but will reset the output to zero before doing so. This forces the user to rotate the intensity control to zero before the instrument will respond to a new intensity setting. Any change in the following modes while the instrument is active, will result in instrument reset: (1) carrier frequency, (2) modulation, (3) stop treatment, and (4) instrument power on/off.

Power to the instrument during treatment can be disrupted because of a power outage or the instrument being switched off. This results in unpredictable output signals from the constant current output stage. Since this stage is coupled directly to the patient, it is necessary to detect this event and disconnect the patient before unwanted signals appear at the output. A detector circuit was included to verify the presence of ac line voltage.

In the event of power failure, the patient is mechanically disconnected, via relays, before the dc power supplies decay. This prevents unpredictable signals from being applied to the patient thus insuring patient safety.

CHAPTER 2

DESIGN AND OPERATION OF THE INTERFERENTIAL MUSCLE STIMULATOR

This chapter discusses the design of the interferential stimulator circuits. The function of each section is explained and followed by a description of the circuitry implementing that function. Design alternatives are considered and unusual aspects are discussed in detail. Finally, the operation of the instrument is explained.

The design makes considerable use of switched capacitor filters for signal processing and analog multipliers for manual and automatic gain control. These will be discussed in detail.

2.1 Design Philosophy

The major design objective of any medical device should be the safety of the patient. This requires knowledge of how the device will be used in actual practice, and knowledge of possible failures that can cause harm to the patient. With this in mind, the highest priority was given to patient safety. Considerable time was spent determining possible failure modes (including operating mode changes) that could result in harm to the patient. With these modes determined, circuitry was included in the design to reduce the probability of harming the patient.

In addition to patient safety, the instrument was designed with the following

attributes: reliability, simplicity, ease of use, ease of manufacture, and ease of maintenance. When one of these design attributes conflicted with patient safety, the highest priority was given to patient safety.

2.2 Oscillator Overview

The heart of the instrument is a two channel oscillator that provides two sinusoidal waveforms at the desired frequencies. Channel one is a selectable frequency of either 2.5KHz or 5KHz. The frequency of channel 2 tracks channel one frequency according to the following equation

$$f_2 = f_1 - \Delta f \quad \text{Eq. 2.1}$$

where f_1 is the frequency of channel 1, f_2 is the frequency of channel two, and Δf is the beat frequency which is set by a front panel control and is in the range $1\text{Hz} \leq \Delta f \leq 200\text{Hz}$. Figure 2.1 shows how this is accomplished. Each section of the oscillator and the circuitry that implements that section will be discussed in detail in the following sections.

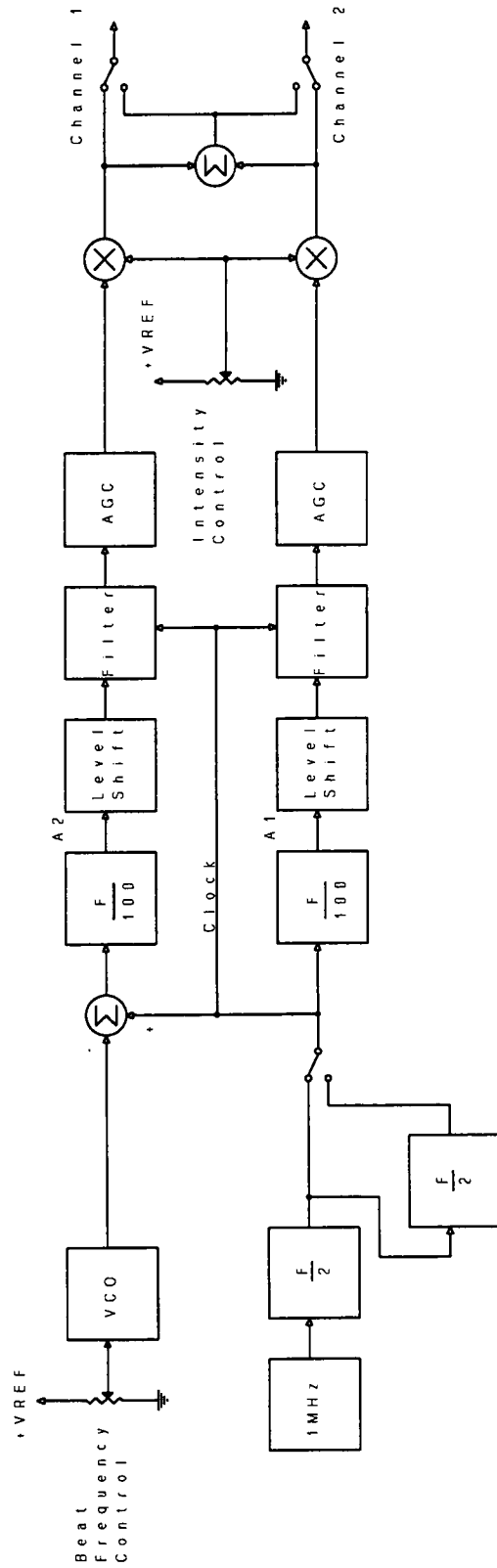


Figure 2.1. Oscillator overview.

2.2.1 Fixed Frequency Oscillator

The master frequency reference for the system is a 1MHz Pierce type crystal controlled gate oscillator. Its output is a 1MHz square wave swinging from -5 volts (logic 0) to +5 volts (logic 1)¹. It serves as a frequency reference for both channels. Figure 2.2 shows the circuit for the oscillator. The CMOS inverter A is biased in its linear region by R_1 , and the R_2 , C_2 combination provides phase shift around the loop. C_1 is added to equalize the capacitance at each node of the crystal. Gate B functions to isolate the oscillator output from the remaining circuitry. A more detailed explanation of this circuit can be found in National Semiconductor's Logic Databook, Volume 1.

The 1MHz output of the master oscillator is passed through two divide-by-two circuits in order to provide either a 500KHz signal or a 250KHz signal that will clock the switched capacitor filters used in the filtering sections. The divide-by-2 functions shown in Figure 2.1 are implemented using D flip-flops as shown in Figure 2.3. These two signals are then applied to a multiplexer circuit, shown as a single pole double throw switch in Figure 2.1, whose output frequency is 500KHz or 250KHz depending on the selection of the carrier frequency. The multiplexer is implemented using the circuit shown in Figure 2.4. The frequency select signal is set to -5V at power up to put the instrument in 5KHz carrier frequency mode. This can be subsequently changed by the user to the 2.5KHz carrier frequency mode using a selector switch on the front panel of the

¹ All logic used in the system, except where noted, use ± 5 volt power supplies.

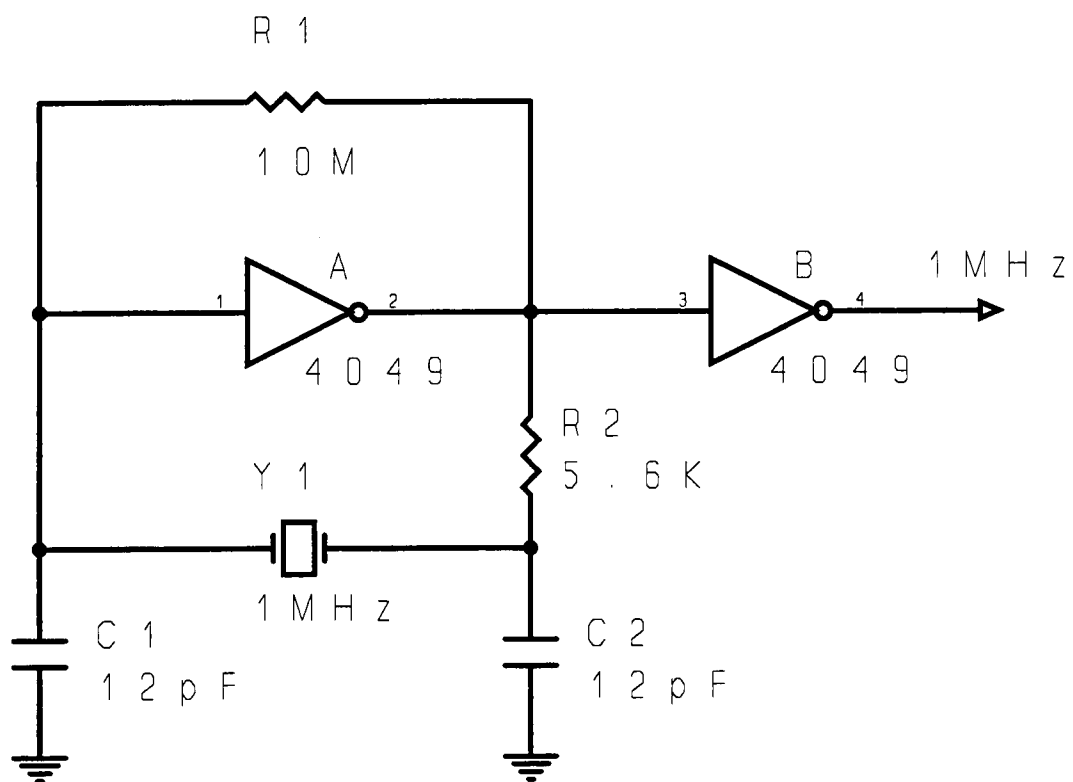


Figure 2.2. Master oscillator.

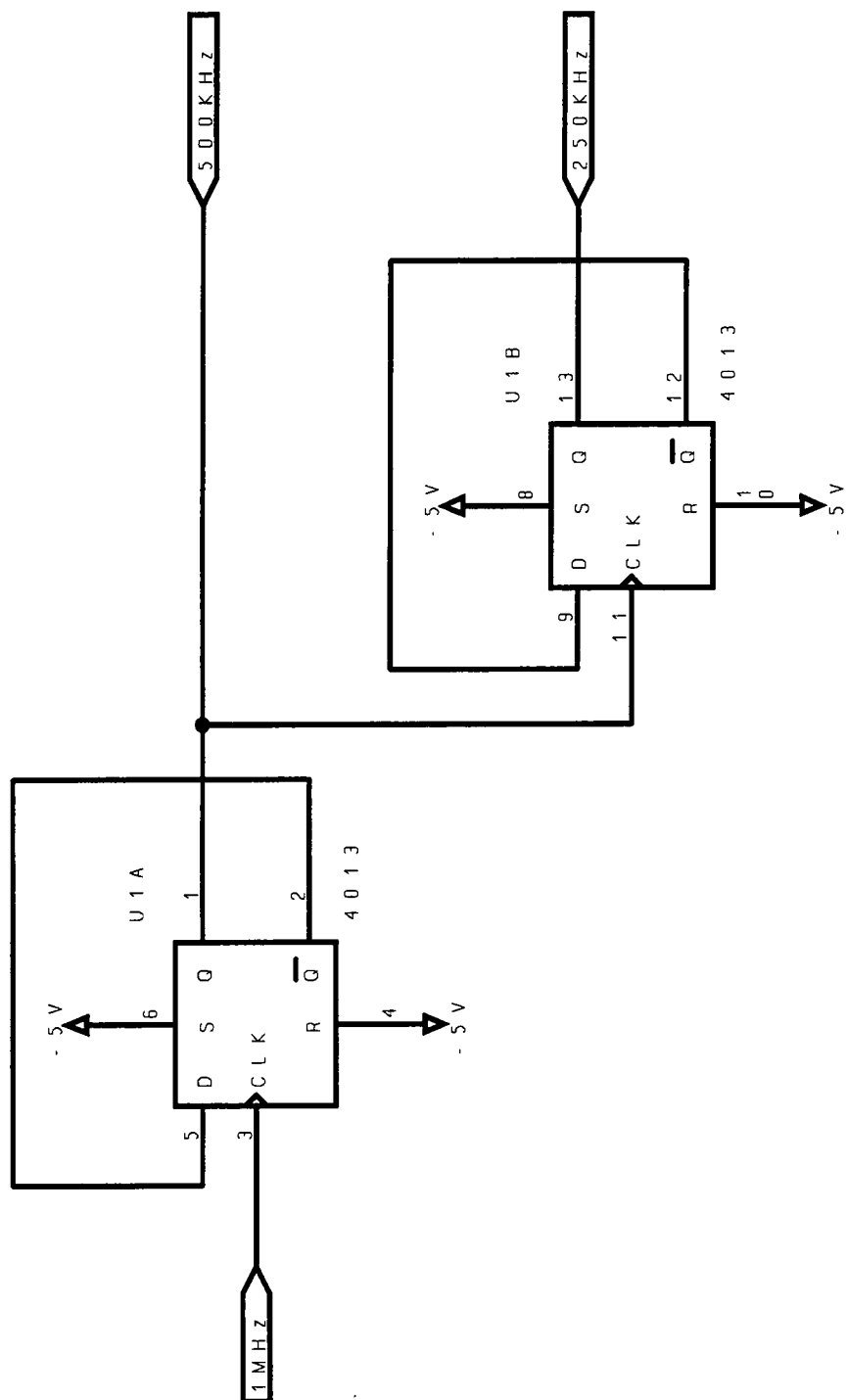


Figure 2.3. Divide-by-two.

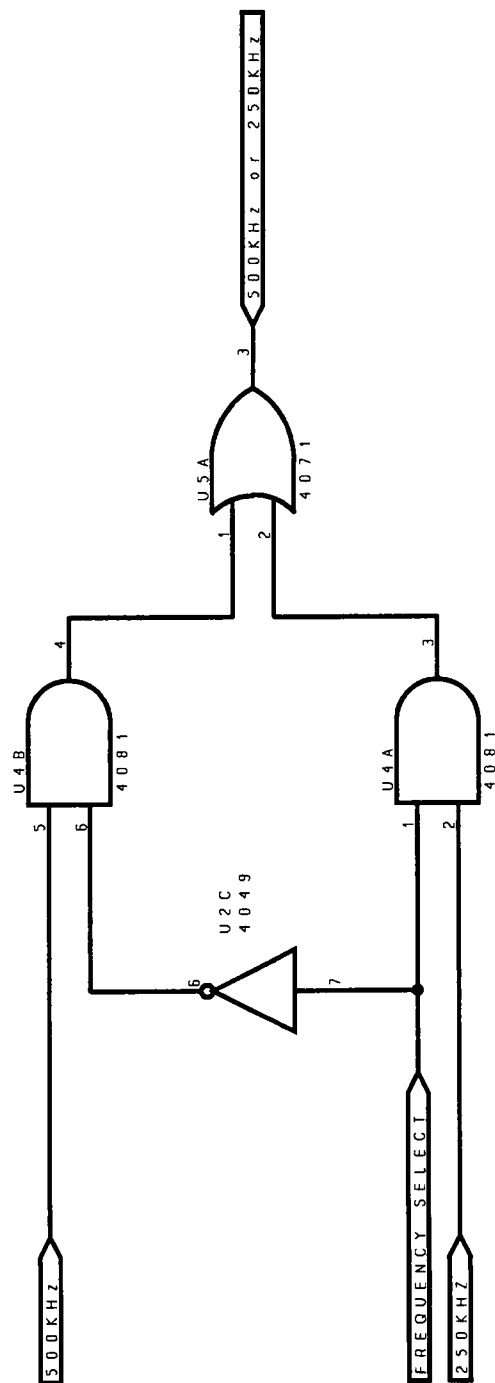


Figure 2.4. Multiplexer circuit.

instrument. The logic that generates this signal will be discussed in a later section.

In order to provide a fundamental frequency signal to be processed by the switched capacitor filters, it was necessary to divide the output of the multiplexer circuit by 100 to obtain a square wave of either 5KHz or 2.5KHz. The method used to accomplish this was to connect two divide-by-ten circuits in series. The implementation of the divide-by-100 function is shown in Figure 2.5. The output of the multiplexer is applied to the clock input of the first 4017. The carry-out bit is used as the input of the second 4017. The carry-out bit of the second 4017 provides either 5KHz or 2.5KHz.

2.2.2 Variable Frequency Oscillator

The variable frequency oscillator (f_2) consists of a front panel control to set Δf (beat frequency), a voltage controlled oscillator, a precision voltage reference, a linear digital subtractor, and a divide-by-100, to produce a square wave that tracks f_1 according to equation 2.1.

An AD654 voltage controlled oscillator (VCO) was used to provide a 100Hz to 20KHz square wave. The circuit shown in Figure 2.6 produces this signal. A voltage divider composed of R_{106} and R_{100} (front panel beat frequency control) provide a reference signal. In order to prevent loading of the divider and provide the AD654 with a low impedance drive, an AD707 precision operational amplifier was used as a buffer between the divider and the VCO. The AD707 was chosen due to its low input offset voltage drift of $0.1\mu\text{V}/^\circ\text{C}$ and its low input offset current drift of $1\text{pA}/^\circ\text{C}$. Any drift associated with this

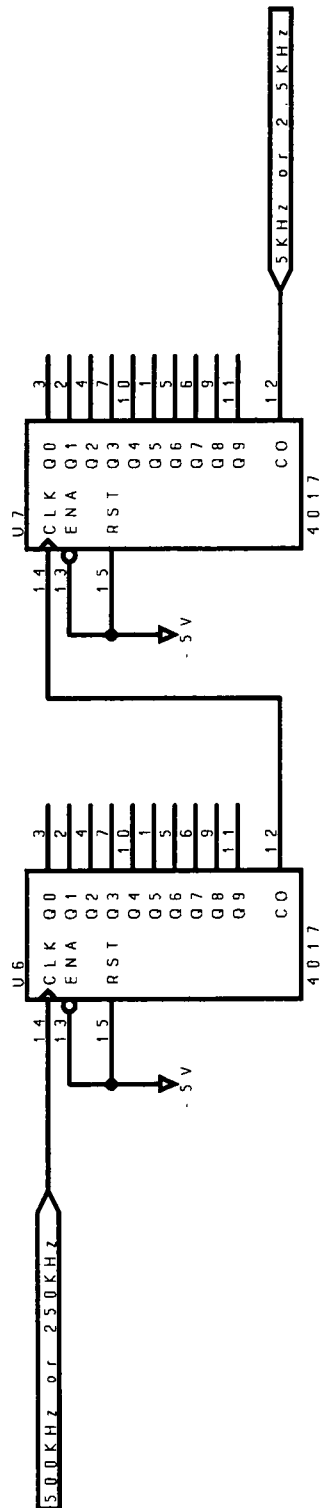


Figure 2.5. Divide-by-100.

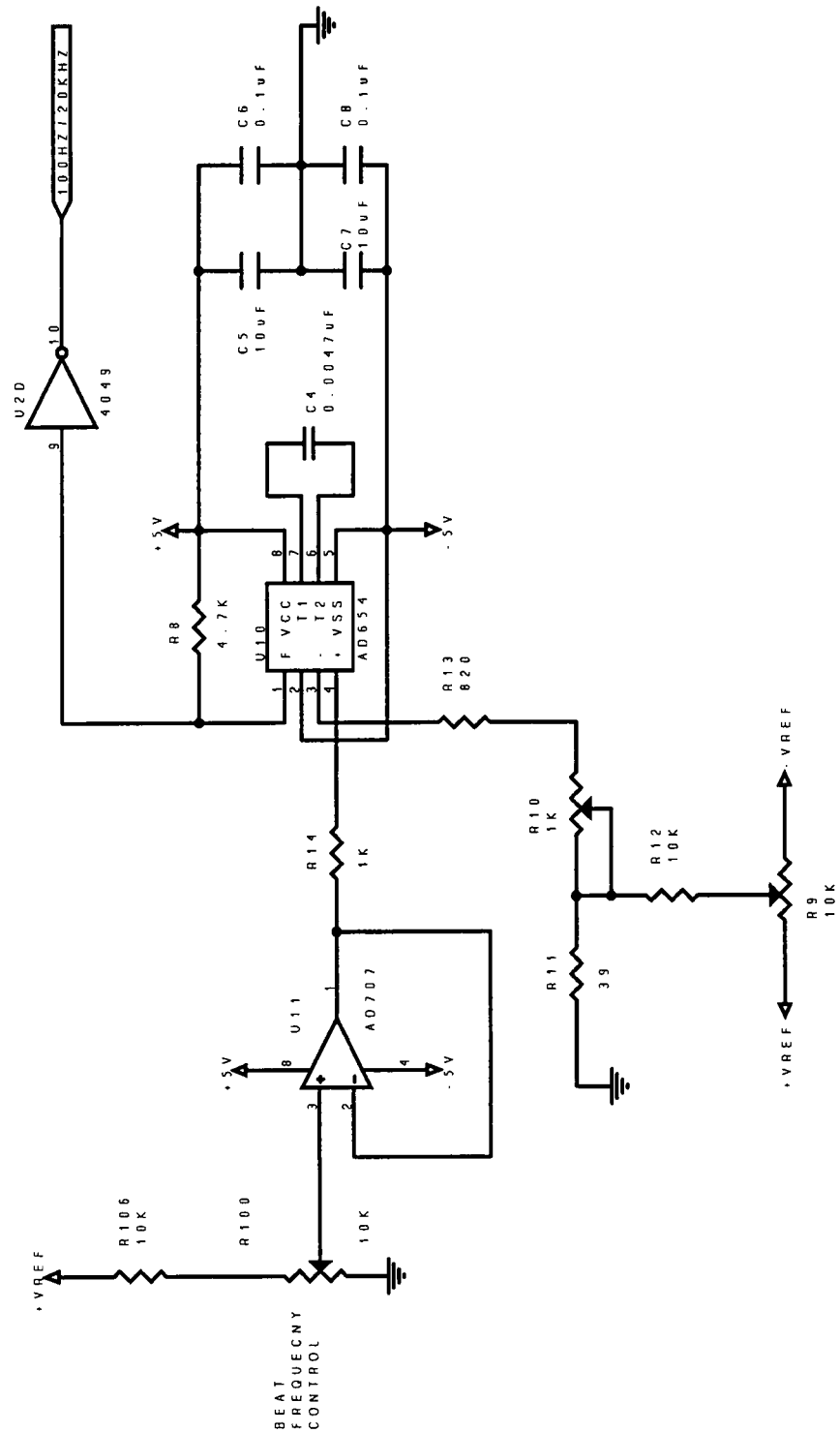


Figure 2.6. Voltage controlled oscillator.

op-amp buffer is applied to the VCO which results in drift in the VCO output. This VCO frequency drift results in drift in the final beat frequency setting and it is important at this point in the signal chain to minimize these errors as much as possible.

The output signal of the AD707 is applied to the AD654 VCO through a $1K\Omega$ resistor. The internal details of the AD654 are shown in Figure 2.7. The input voltage is converted to a scaled current in the NPN follower. The best performance is achieved when this current is 1mA [8]. The purpose of R_{comp} is to compensate for the input amplifier bias currents which will generate an offset due to the difference in dc source resistance between the inverting and noninverting input terminals. In this application minimum offset and offset drift are very important and the $1K\Omega$ was added in Figure 2.6 to balance the dc source resistance between the terminals of the input amp.

The reference voltage $+V_{REF}$ in Figure 2.6 is +2.5V so the input voltage to the AD654 is

$$V_{input} = V_{REF} \left(\frac{10K}{10K+10K} \right) = \frac{V_{REF}}{2} \quad \text{Eq. 2.2}$$

or V_{input} is in the range $0V \leq V_{input} \leq 1.25V$. Given this input voltage range, the resistive network from pin 3 to ground of the AD654 in Figure 2.6 was designed to allow an output frequency range of $100Hz \leq F_{out} \leq 20KHz$, with the provision for maximum and minimum frequency calibration over the range $0V \leq V_{input} \leq 1.25V$.

The output frequency to input voltage relationship for the AD654 is given by the following equation [8]

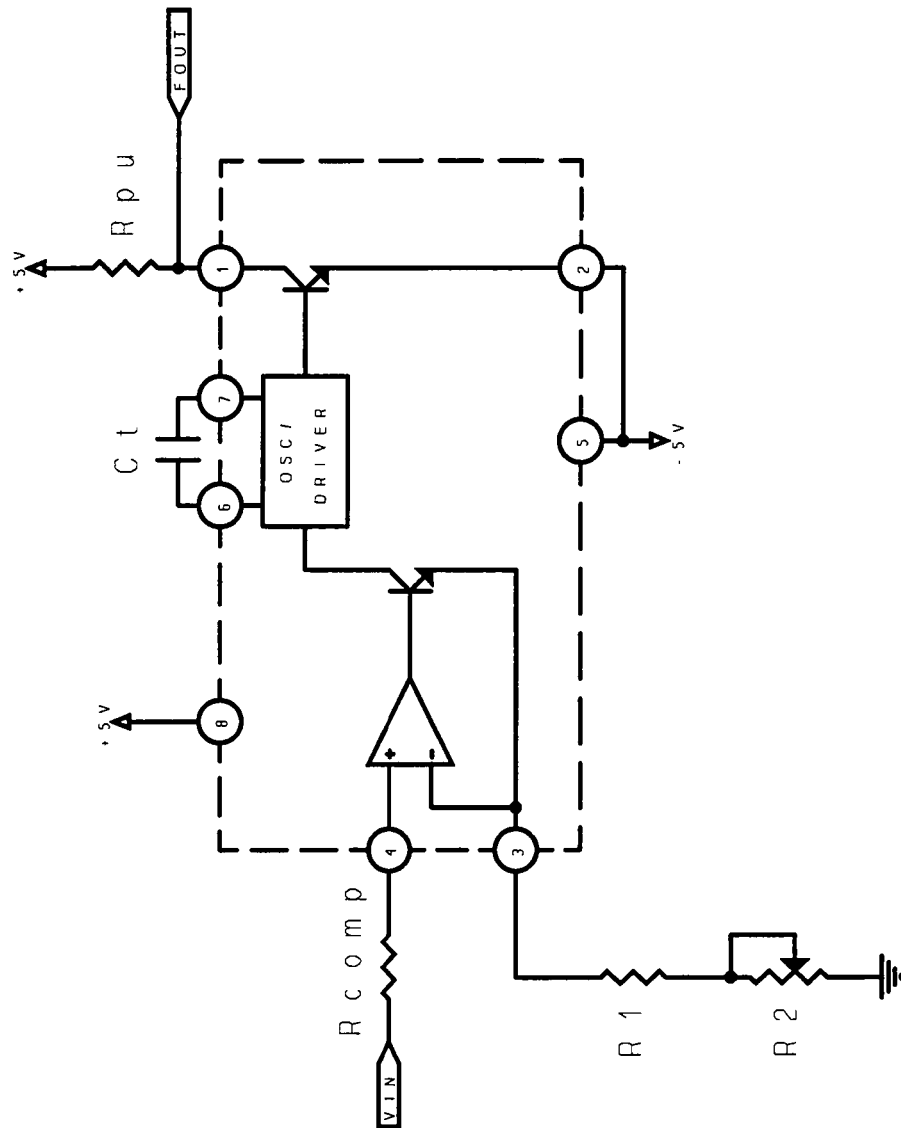


Figure 2.7. AD654 internal details.

$$F_{out} = \frac{V_{input}}{(10V) (R_1 + R_2) C_t} , \quad \text{Eq. 2.3}$$

where the quantity $(R_1 + R_2)$ is the equivalent resistance from pin 3 to ground, and C_t is the timing capacitor connected between pins 6 and 7. A polystyrene $0.0047\mu\text{F}$ capacitor was used for C_t for its low temperature coefficient.

The nominal resistance (pin 3 to ground, omitting for the moment the effect of the offset network composed of R_9 , R_{12} , and R_{11}) covers the range $820\Omega \leq R_{3\text{-ground}} \leq 1820\Omega$. Substituting $R_{3\text{-ground}}$ into equation 2.3 for the quantity $(R_1 + R_2)$, with $C_t = 0.0047\mu\text{F}$, and $V_{input} = 1.25\text{V}$, we have

$$F_{out} = \frac{1.25V}{(10V) (R_{3\text{-ground}}) (4.7\eta\text{F})} . \quad \text{Eq. 2.4}$$

Substituting 1820Ω and 820Ω into equation 2.4 for $R_{3\text{-ground}}$ we obtain the full scale calibration range for F_{out} as $14,613\text{Hz} \leq F_{out} \leq 32,433\text{Hz}$. This calculation does not include the effect of the bias network composed of $\pm V_{REF}$, R_9 , R_{12} , and R_{11} in Figure 2.6. The purpose of this network is to provide an offset calibration which sets the output frequency of the AD654 when R_{100} is at its minimum setting, i.e. $V_{input} = 0\text{V}$. This offset adjustment provides a frequency span of $20\text{Hz} \leq F_{out} \leq 160\text{Hz}$ when $V_{input} = 0\text{V}$.

To calibrate the VCO circuit, R_{100} in Figure 2.6 is set to its maximum setting (rotated fully clockwise, $V_{input} = 1.25\text{V}$) and R_{10} (full scale trim) is adjusted for an output frequency at pin 10 of U2D of 20.00KHz . It should be noted that the purpose of U2D is

to isolate pin 1 of the AD654 from the remaining circuitry to be driven. V_{input} is then set to 0V and R_9 adjusted for an output frequency at pin 10 of U2D of 100.00Hz.

As can be seen in Figure 2.6, the reference voltages $\pm V_{REF}$ have a direct impact on the stability of the VCO and hence the beat frequency. In order to minimize beat frequency drift due to these reference voltages, a precision voltage reference and two precision operational amplifiers were used to generate $\pm V_{REF}$. The circuit is shown in Figure 2.8.

To provide tracking between channels, the VCO output frequency is subtracted from the multiplexer (Figure 2.4) output frequency. This process is represented as the summer in Figure 2.1. This results in a frequency span of $480\text{KHz} \leq f \leq 499.9\text{KHz}$ (or $230\text{KHz} \leq f \leq 249.9\text{KHz}$) at the output of the summer. This subtraction process is linear in that a change in carrier frequency does not require a readjustment of the beat frequency. The circuit that performs this subtraction process is shown in Figure 2.9. The rising edge of the VCO output (trailing edge of U2D in Figure 2.6) clocks a one to the output of U12A. This one is clocked through to the Q output of U12B at the first rising edge of the multiplexer output, which immediately resets U12A's Q output to zero. No changes occur until the next rising edge of the VCO output. The Q-not output of U12B is then NAND'ed with the inverse of the multiplexer output to form the difference between the VCO output frequency and the multiplexer output frequency. This circuit essentially removes one low-high-low pulse from the multiplexer output at each rising edge of the VCO output. Since the rising edge of the VCO output is not synchronized with the rising edge of the multiplexer output, the output of this circuit contains a leading

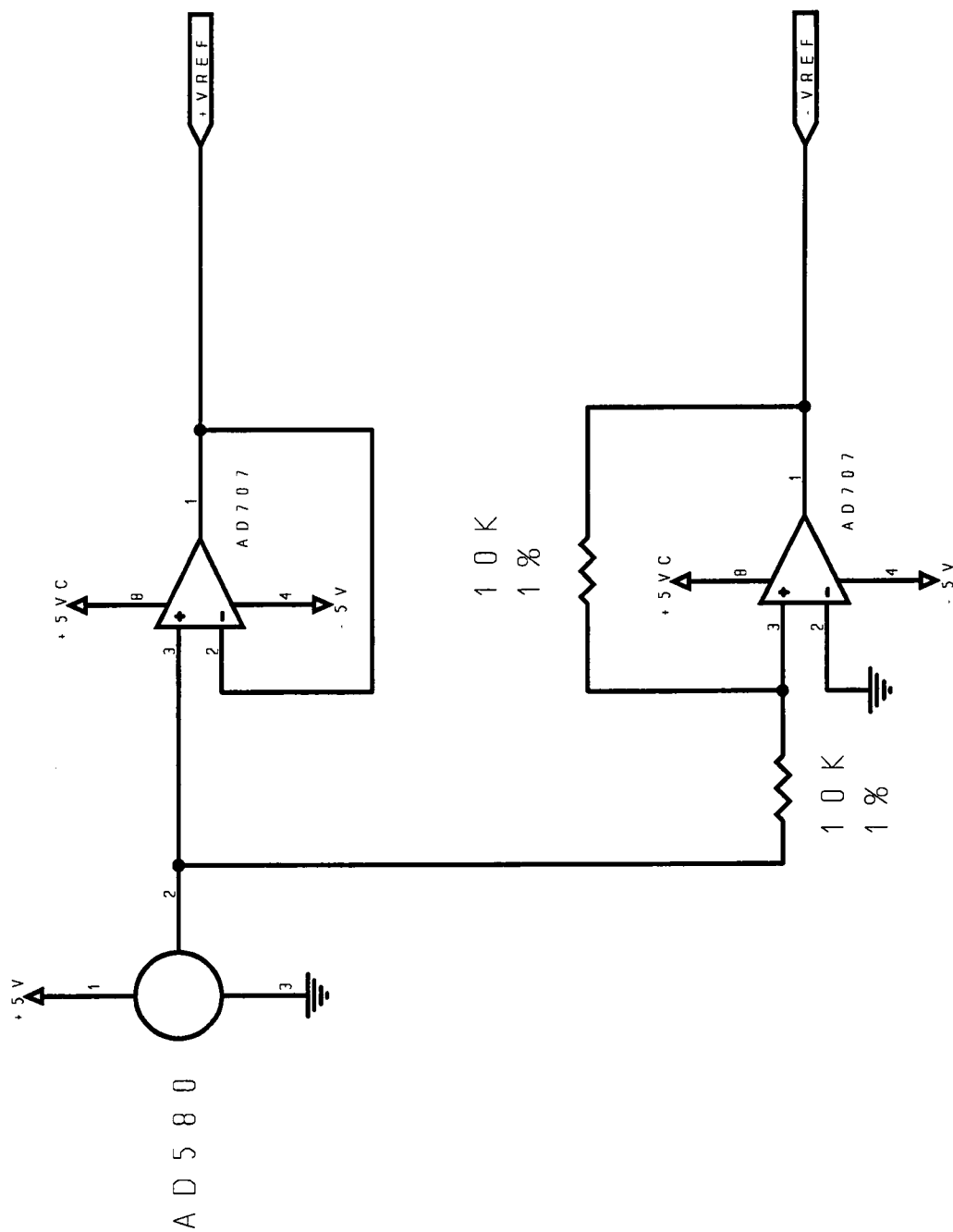


Figure 2.8. Precision reference.

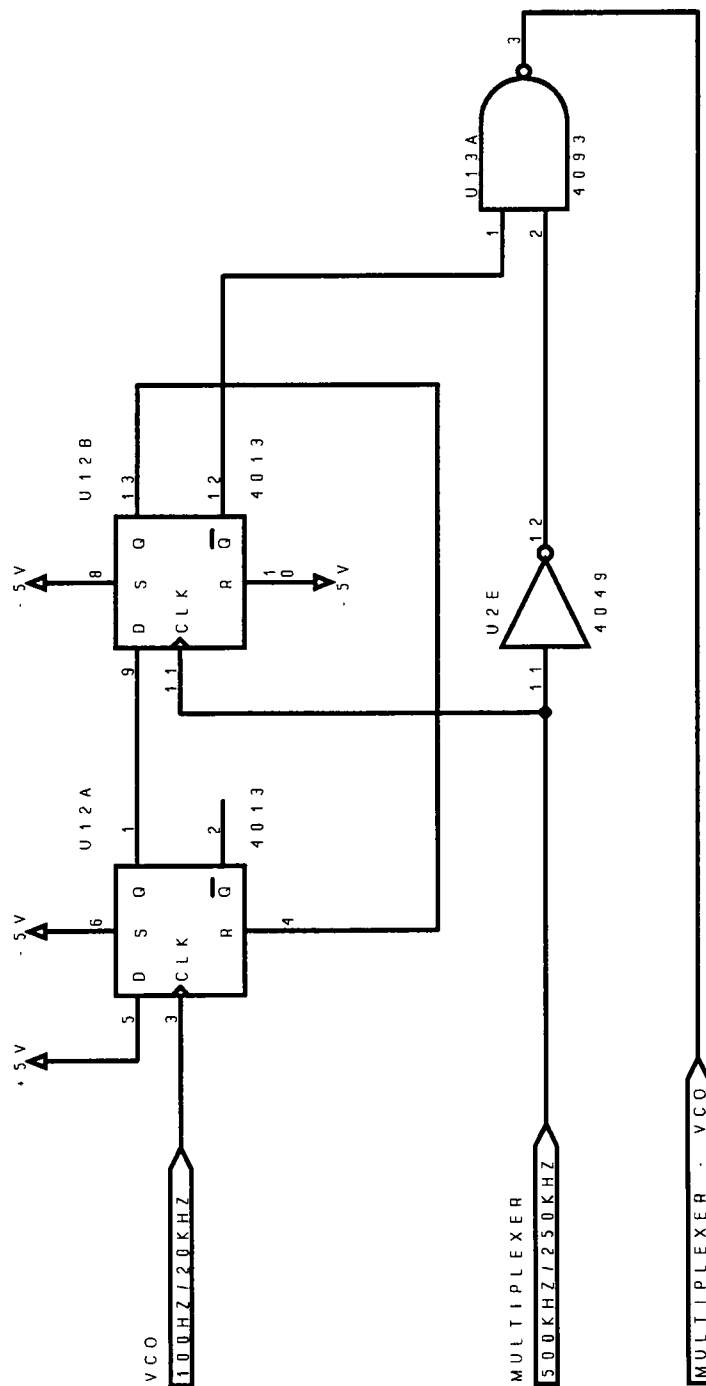


Figure 2.9. Digital subtractor.

and trailing edge uncertainty (frequency jitter) that will not exceed one multiplexer period. The worst case frequency jitter therefore occurs when the multiplexer frequency is 250KHz (longer period).

Table 2.1 shows the signal/node relationship between Figure 2.9 and the signals for the digital subtractor which are shown in Figures 2.10 through 2.12.

The output of the subtractor circuit is divided by 100 to provide a fundamental frequency to be filtered by the switched capacitor filters. The division is performed by a circuit equivalent to the one shown in Figure 2.5. This signal is then in a frequency range of $4.800\text{KHz} \leq f \leq 4.999\text{KHz}$ or $2.300\text{KHz} \leq f \leq 2.499\text{KHz}$ depending on the multiplexer frequency and the beat frequency setting. These output signals, with measurements of jitter at both multiplexer frequencies are shown in Figures 2.13 and 2.14.

From Figure 2.13 the rise/fall time of the signal is approximately (note low resolution) $1.7\mu\text{s}$. Subtracting this value from the measured trailing edge time variation, since this is approximately constant during the measurement process, the result is a trailing edge jitter of approximately $4.3\mu\text{s}$. This is approximately equal to the multiplexer period of $4.0\mu\text{s}$ (Figure 2.13 measurement was performed with a multiplexer output frequency of 250KHz). The error is due to the low resolution time scale on the rise and fall time measurements and errors in placement of the vertical measurement bars when the measurement was performed. The same analysis can be carried out for Figure 2.14 with a trailing edge jitter of approximately $2.4\mu\text{s}$. This is approximately equal to the multiplexer period of $2.0\mu\text{s}$ (Figure 2.14 measurement was performed with a multiplexer output frequency of 500KHz). The cause of the error is as stated before.

Table 2.1**Subtractor Waveform Guide**

Figure	Signal	Oscilloscope Channel	VCO Frequency	Multiplexer Frequency
2.10	pin 1, U12A	1	20KHz	250KHz
2.10	pin 13, U12B	2	20KHz	250KHz
2.10	pin 12, U12B	3	20KHz	250KHz
2.11	pin 9, U2D	1	20KHz	250KHz
2.11	pin 11, U2E	2	20KHz	250KHz
2.11	pin 3, U13A	3	20KHz	250KHz
2.12	pin 9, U2D	1	20KHz	500KHz
2.12	pin 11, U2E	2	20KHz	500KHz
2.12	pin 3, U13A	3	20KHz	500KHz

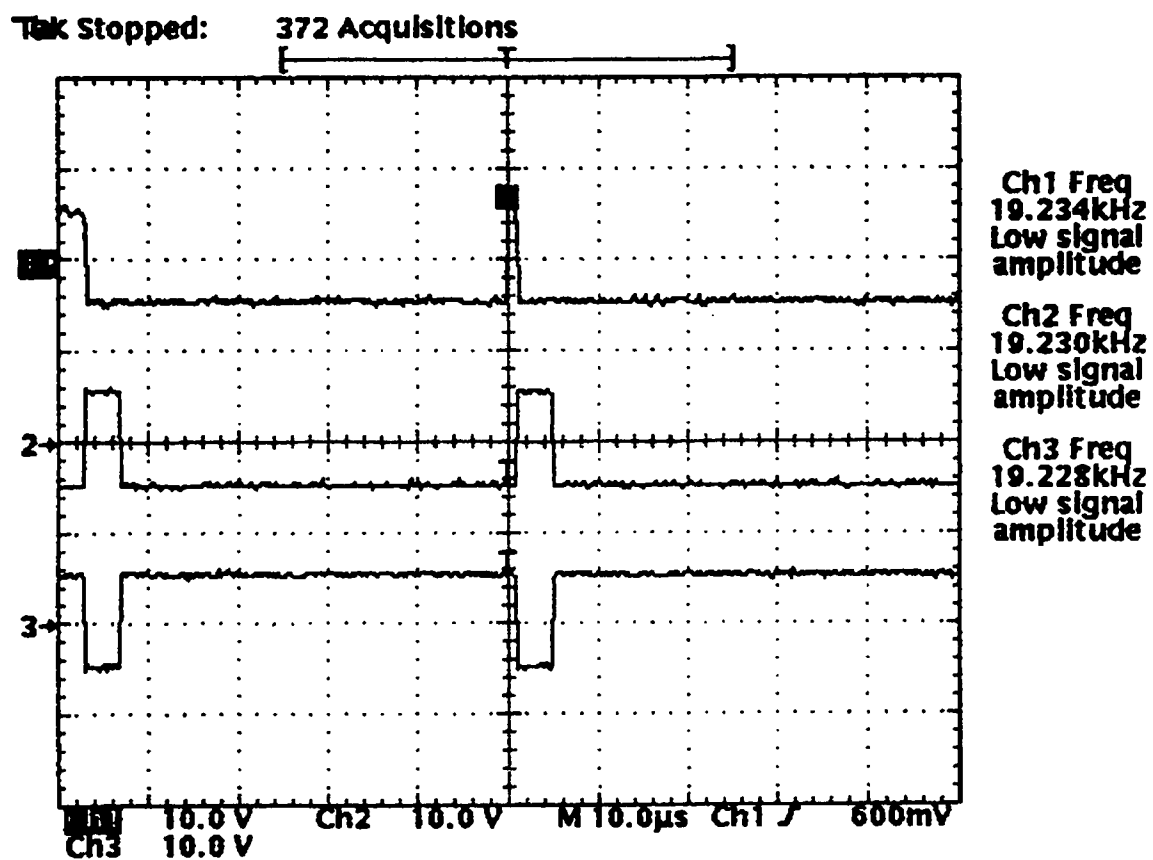


Figure 2.10. Digital subtractor internal waveforms.

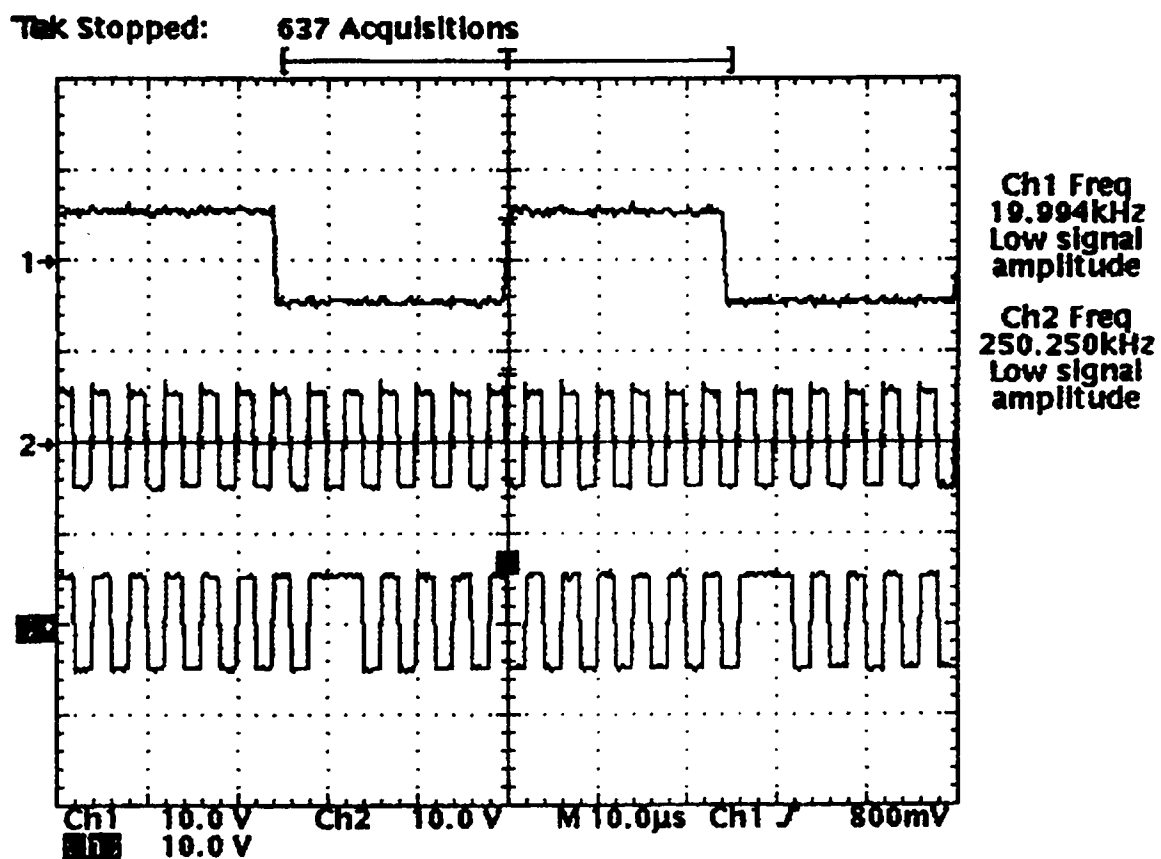


Figure 2.11. Subtractor input/output waveforms, 250KHz.

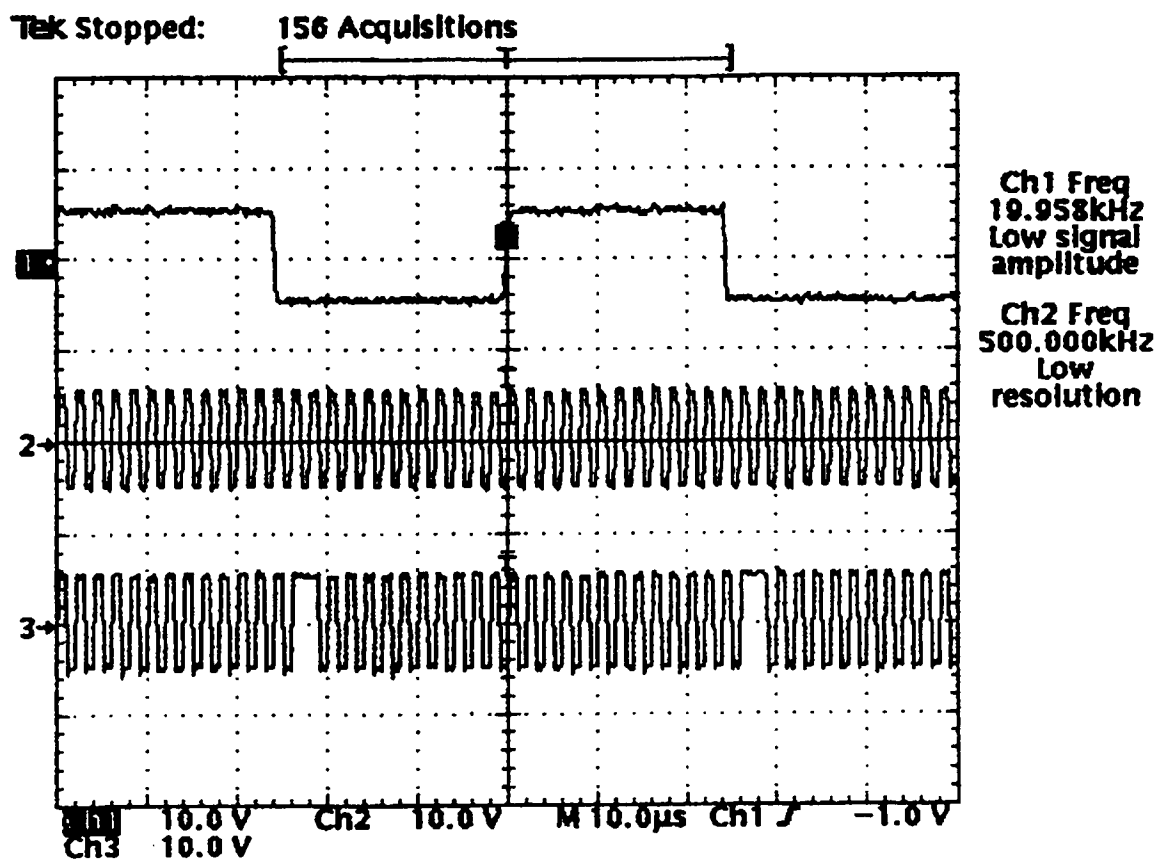


Figure 2.12. Subtractor input/output waveforms, 500KHz.

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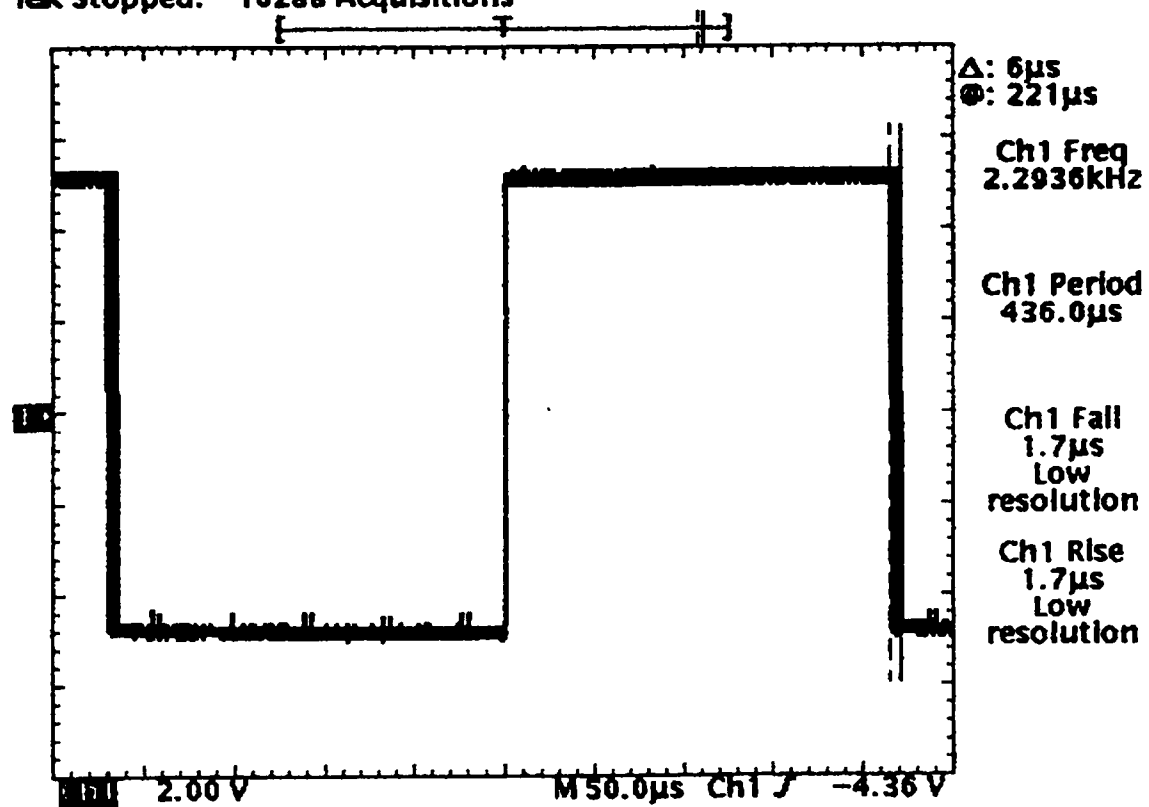


Figure 2.13. Divide-by-100 waveform, 250KHz.

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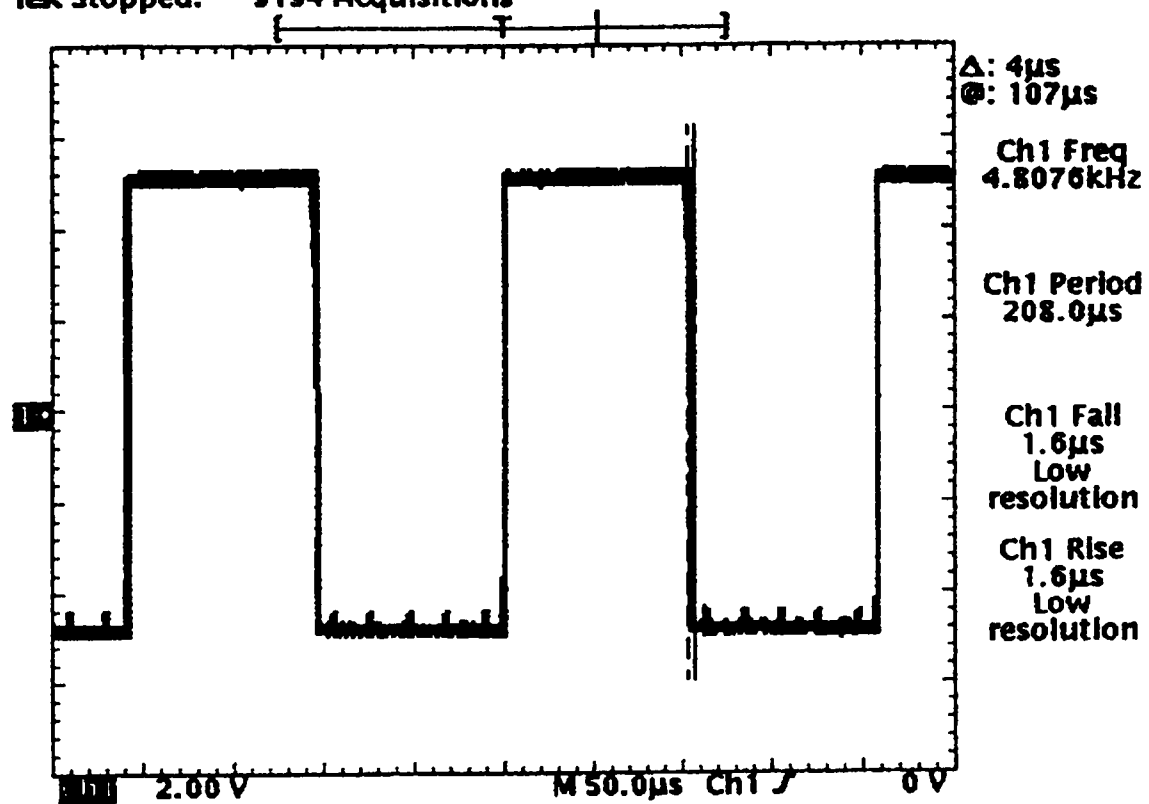


Figure 2.14. Divide-by-100 waveform, 500KHz.

Before these signals (points A1 and A2 in Figure 2.1) can be filtered, it is necessary to scale (level shift) them to an appropriate level. This is accomplished by a voltage divider and op-amp buffer. The circuit that performs this function is shown in Figure 2.15. Note that the output of each channel's divide-by-100 is followed by a circuit like the one shown in Figure 2.15. The output of this circuit is a $\pm 2V_{p-p}$ square wave. The LF347 was chosen for the buffer amp due to its 13 V/ μ s slew rate, and high input resistance of $10^{12} \Omega$.

2.2.3 Oscillator Signal Processing

The purpose of the signal processing circuitry is to shape the square wave outputs of the fixed frequency oscillator (5KHz or 2.5KHz) and the variable frequency oscillator ($4.800\text{KHz} \leq f \leq 4.999\text{KHz}$ or $2.300\text{KHz} \leq f \leq 2.499\text{KHz}$) into sinusoidal waveforms. The original idea was to take the output of the summer and multiplexer and use these signals as clock inputs to two separate switched capacitor filters. The output of the respective divide-by-100 circuits, after level shifting, would then be processed by the filters. This would take advantage of the 100:1 clock-to-center frequency ratio of the switched capacitor filters, and require no automatic gain control when either the carrier or beat frequency was changed. This scheme was prototyped and after filtering, the variable frequency channel contained significant distortion that was traced to the leading/trailing edge jitter discussed previously. It was then necessary to change the filtering scheme used for the variable frequency channel. This new design required more

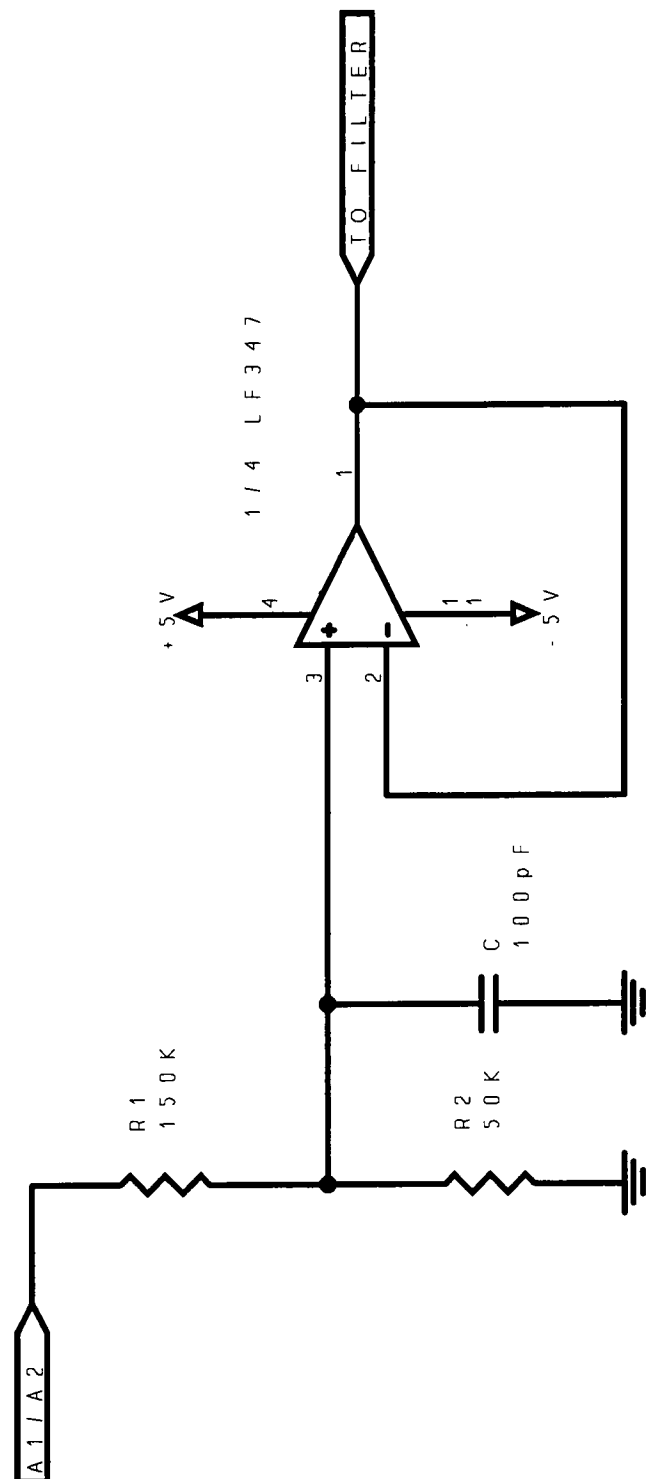


Figure 2.15. Level shifter.

elaborate filtering and will be discussed after the fixed frequency channel.

The signal for channel 1 (fixed frequency channel) is either 2.5KHz or 5KHz. Shaping square waves of these two frequencies by active op-amp methods would require two separate stages, one for each frequency. A simpler approach, using monolithic switched capacitor filters was found to be the best alternative. Using this method, one filter can be used for both frequencies by changing only the input clock frequency.

In order to define the filter parameters required, a Fourier analysis of the signal to be filtered was required. The output of the level shifter circuit shown in Figure 2.15 is the signal to be processed by the filter. A typical signal of 2.5KHz, $\pm 2V_{p-p}$, was analyzed and these results were extended for each individual case.

A 2.5KHz, $\pm 2V_{p-p}$ square wave can be represented mathematically by a Fourier series as

$$f(t) = \frac{4}{\pi} \left(\frac{\sin(\omega t)}{1} + \frac{\sin(3\omega t)}{3} + \dots + \frac{\sin(n\omega t)}{n} \right) \quad \text{Eq. 2.5}$$

or more compactly as

$$f(t) = \frac{4}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{\sin(n\omega t)}{n} \quad \text{Eq. 2.6}$$

where the summation requires an infinite number of terms to exactly represent the waveform. Using equation 2.6 to generate a 2.5KHz square wave of amplitude $\pm 2V_{p-p}$

where $n=1,3,5,\dots,31$ results in the waveform shown in Figure 2.16. If the amplitude of all harmonics greater than the fundamental ($n > 1$) are attenuated by 20db, the resulting waveform is a reasonably pure sinusoid. This filtered waveform is shown in Figure 2.17.

The amplitude of the harmonics in equation 2.6 decreases according to

$$db = 20 \log \left(\frac{1}{2^{n-1}} \right) \quad \text{Eq. 2.7}$$

where $n=1,2,3,\dots,\infty$. A plot of this function will show the gain roll-off and can be used to determine the filter gain attenuation rate or gain slope. The filter gain should be 0db at the fundamental frequency and have a gain slope 20db per decade greater than predicted by equation 2.5. It has already been shown that if the harmonics are attenuated by 20db the resulting sinusoid will be adequate. Figure 2.18 shows a plot of the actual harmonic gain slope along with the required filter gain slope. Note that the curves exhibit a slight bow in their characteristic around $n=2$. To assure that all harmonic frequencies ($n > 1$) were attenuated by at least 20db, the gain slope for the filter was chosen to be 40db per decade. This required a fourth order filter and was implemented with one LTC1060 (Linear Technology) switched capacitor filter. This device is a dual, second order filter, so two second order filters were connected in cascade to obtain a fourth order response.

The LTC1060 is a clock tunable filter that varies the center frequency of the filter function in response to a change in clock frequency. When clocked by the output of the multiplexer circuit in Figure 2.4, the center frequency of the filter tracks the output frequency of the level shifter in Figure 2.15 when the device is configured for a clock-to-

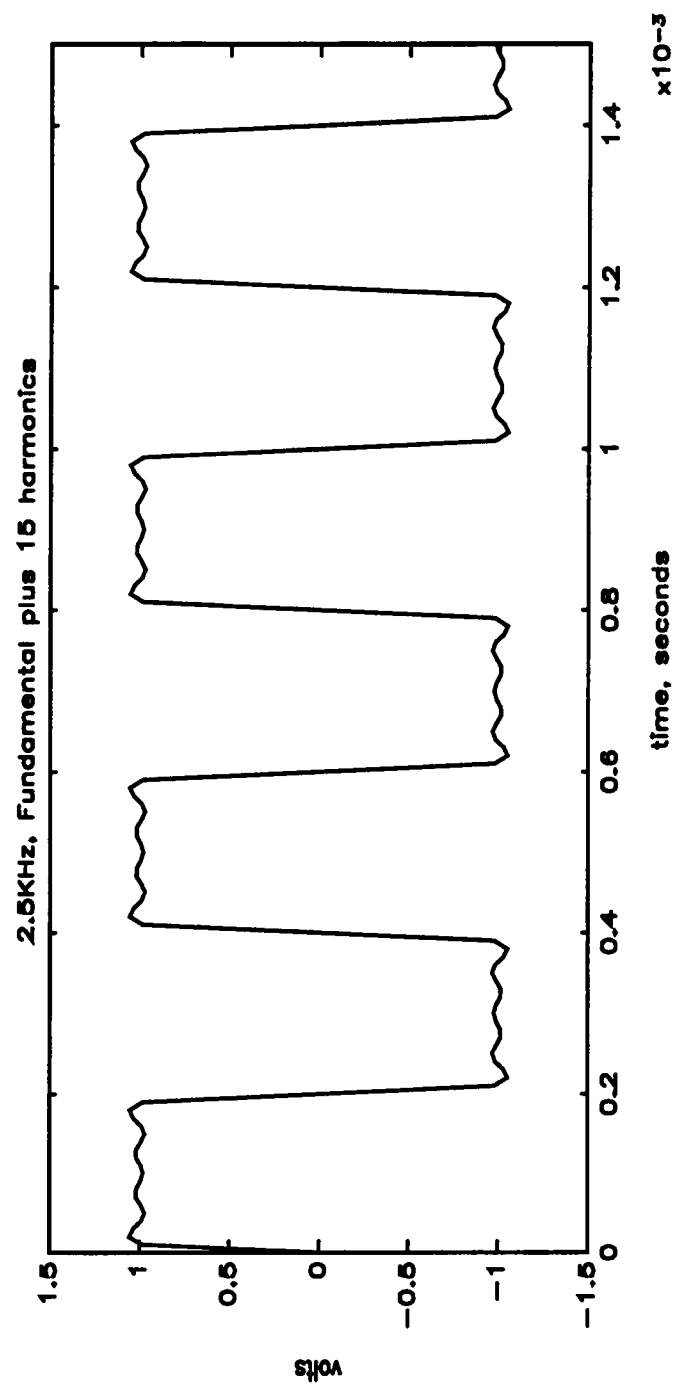


Figure 2.16. Square wave generated by equation 2.6.

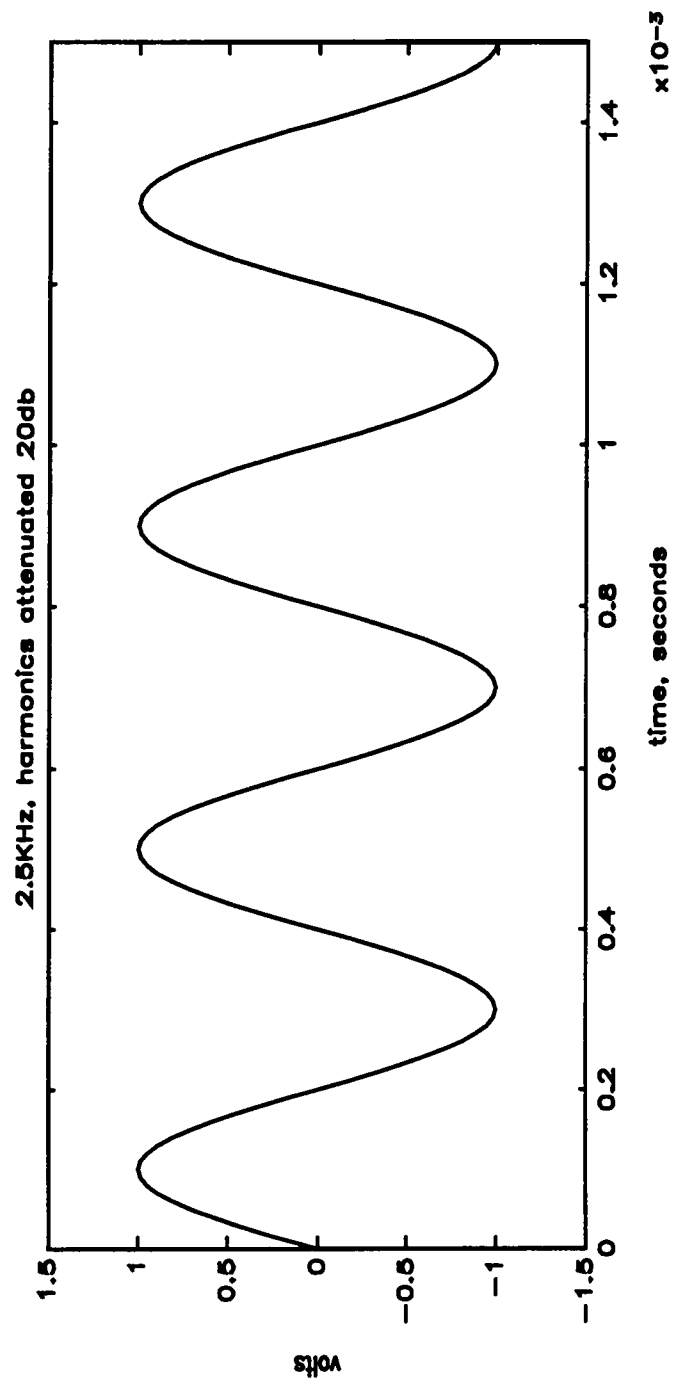


Figure 2.17. Filtered waveform.

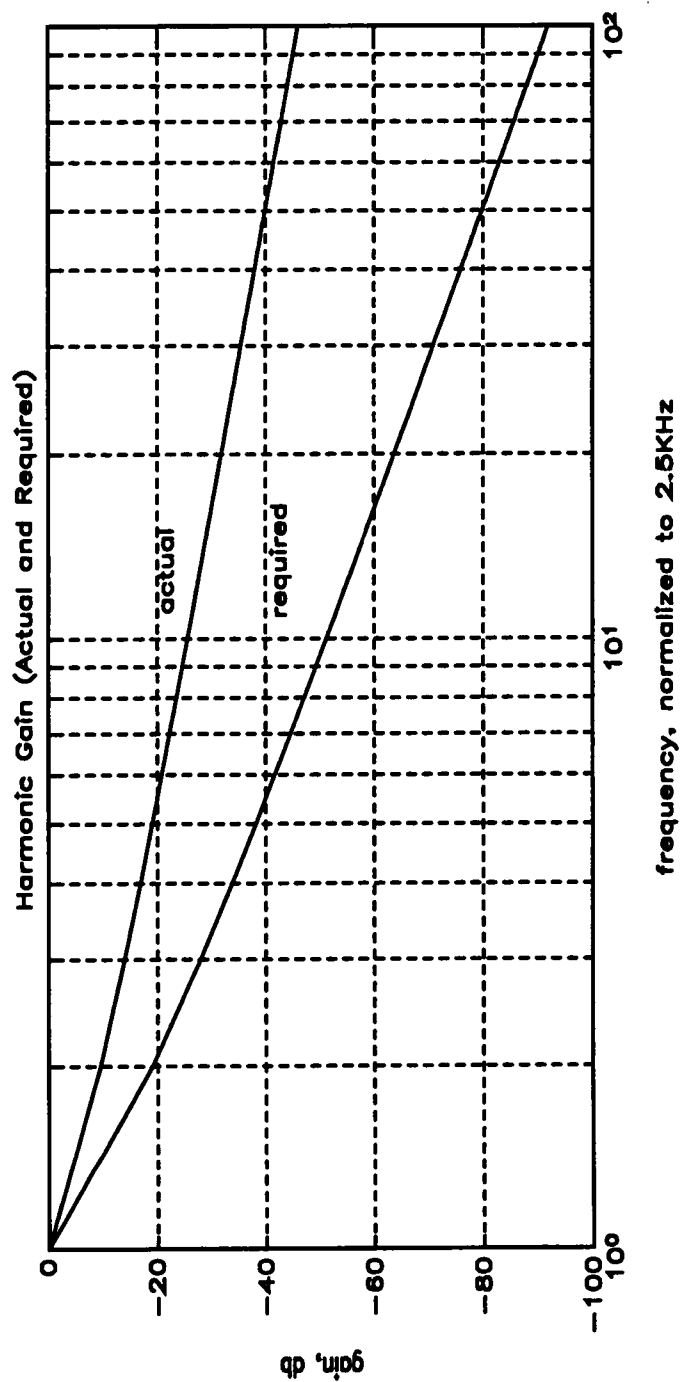


Figure 2.18. Harmonic/filter gain characteristics.

center frequency ratio of 100:1. This results in a relatively constant amplitude sinusoidal output of the filter when the multiplexer frequency is changed between 250KHz and 500KHz.

The LTC1060 consists of two second order filters with lowpass, highpass, and bandpass outputs. The center frequency of each output is determined by the respective resistor ratios and input clock frequency. Figure 2.19 shows the internal details of one filter section. Mode 3 was chosen because it allows independent tuning of the filter parameters and requires minimum external components.

To minimize dc and low frequency effects, a Butterworth bandpass response was chosen to filter all frequencies and pass only the fundamental. The general second order bandpass filter is represented by the transfer function

$$G(s) = K \frac{s \frac{\omega}{Q}}{s^2 + s \frac{\omega}{Q} + \omega^2} \quad \text{Eq. 2.8}$$

where K is the gain of the filter at the center frequency $\omega = 2\pi f_o$ (f_o is the center frequency of the complex pole pair), Q is a measure of the selectivity of the filter, and s is the Laplace operator. This can be implemented with the LTC1060 where

$$K = -\frac{R_3}{R_1}, \quad \text{Eq. 2.9}$$

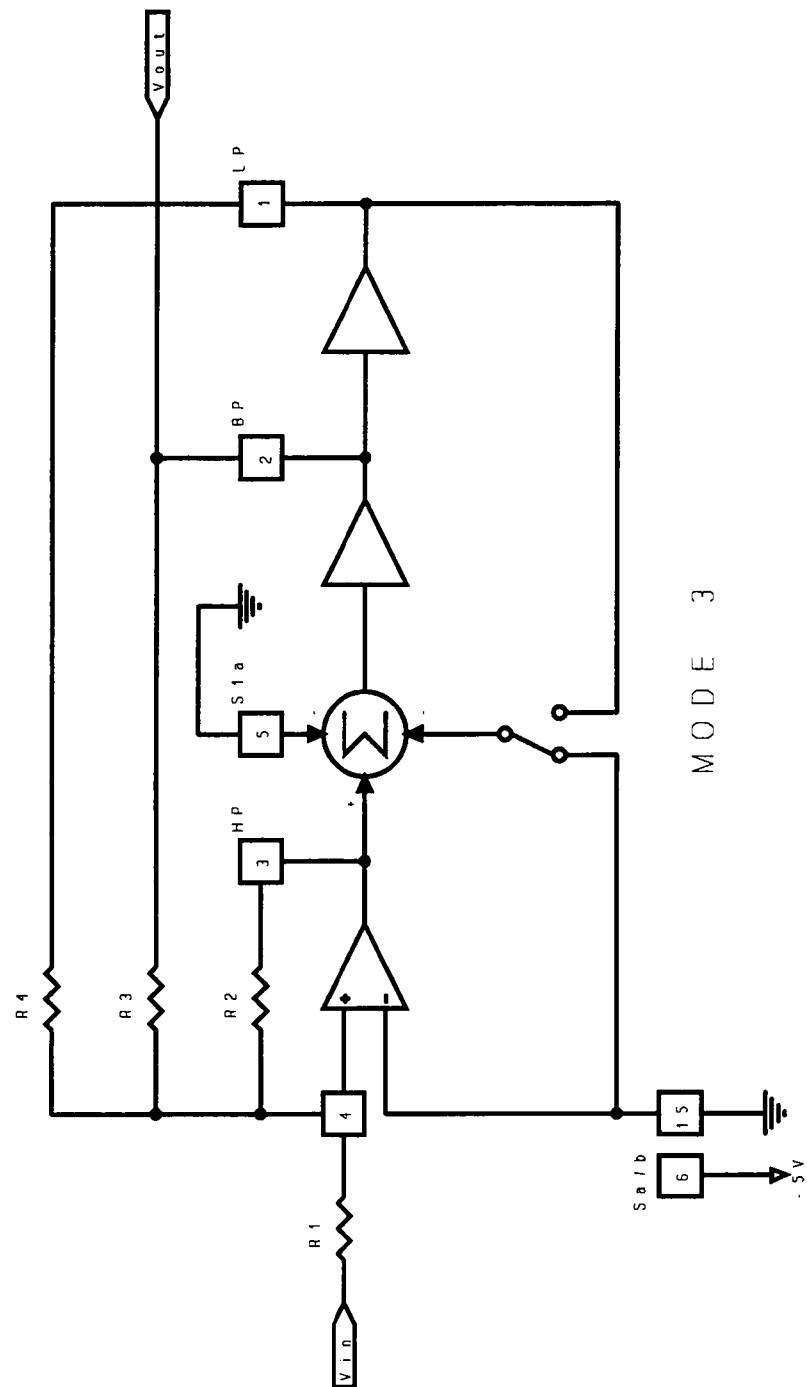


Figure 2.19. LTC1060 internal details.

$$f_o = \frac{f_{clk}}{100} \sqrt{\frac{R_2}{R_4}} , \quad \text{Eq. 2.10}$$

$$Q = \frac{R_3}{R_2} \sqrt{\frac{R_2}{R_4}} , \quad \text{Eq. 2.11}$$

are the equations that govern the operation of one second order filter section.

The design of the filter consists of cascading two second order bandpass filters with different center frequencies which produces the required fourth order response. The actual design was carried out using FilterCAD, a program supplied by Linear Technology Corporation, for use with their switched capacitor products. Experimentation with this program and subsequent breadboard evaluation resulted in the circuit shown in Figure 2.20. Resistors for stage 1 are numbered R_1 , R_2 , R_3 , and R_4 , while those for stage 2 are numbered $R_{1,2}$, $R_{2,2}$, $R_{3,2}$, and $R_{4,2}$ respectively.

Using the resistor values shown in Figure 2.20, the transfer function for the first stage can be determined as

$$G(s) = -1 \frac{2045s}{s^2 + 2045s + 2.14 \times 10^8} \quad \text{Eq. 2.12}$$

where $K = -1$ represents a 180° phase shift from input to output. The poles of this function are $p_1, p_2 = -1023 \pm j14612$ so equation 2.12 can be written as

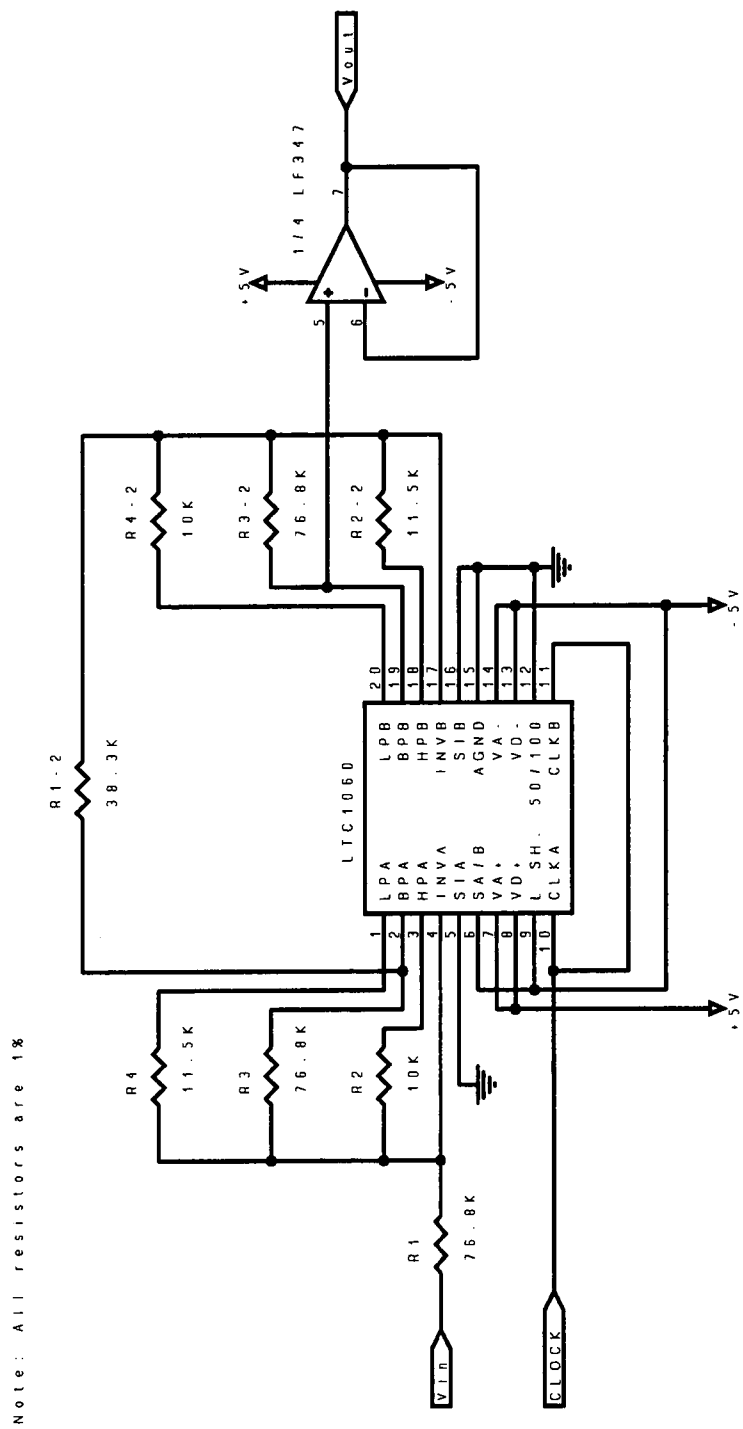


Figure 2.20. Fourth order bandpass implementation.

$$G(s) = \frac{2045s}{(s+(-1023+j14612))(s+(-1023-j14612))} \quad \text{Eq. 2.13}$$

In the same manner the transfer function for the second stage can be found as

$$H(s) = -2 \frac{2352s}{s^2+2352s+2.83 \times 10^8} \quad \text{Eq. 2.14}$$

where $K = -2$ is the gain (with a 180° phase shift) from input to output. The poles of this function are $p_1, p_2 = -1176 \pm j16804$ so equation 2.14 can be written as

$$H(s) = 2 \frac{2352s}{(s+(-1176+j16804))(s+(-1176-j16804))} \quad \text{Eq. 2.15}$$

Figures 2.21 and 2.22 are the Bode plots for $G(s)$ and $H(s)$ (magnitude and phase) with the frequency axis in hertz.

The overall filter response is $F(s)=G(s)H(s)$. Using equations 2.12 and 2.14 the transfer function of the fourth order response is found to be

$$F(s) = 2 \frac{4.8 \times 10^6 s^2}{s^4 + 4.4 \times 10^3 s^3 + 5.03 \times 10^8 s^2 + 1.08 \times 10^{12} s + 6.09 \times 10^{16}} \quad \text{Eq. 2.16}$$

where $K=+2$ implies a 360° phase shift from input to output. Figures 2.23 and 2.24 are the Bode plots for $F(s)$ (magnitude and phase) with the frequency axis in hertz. With an

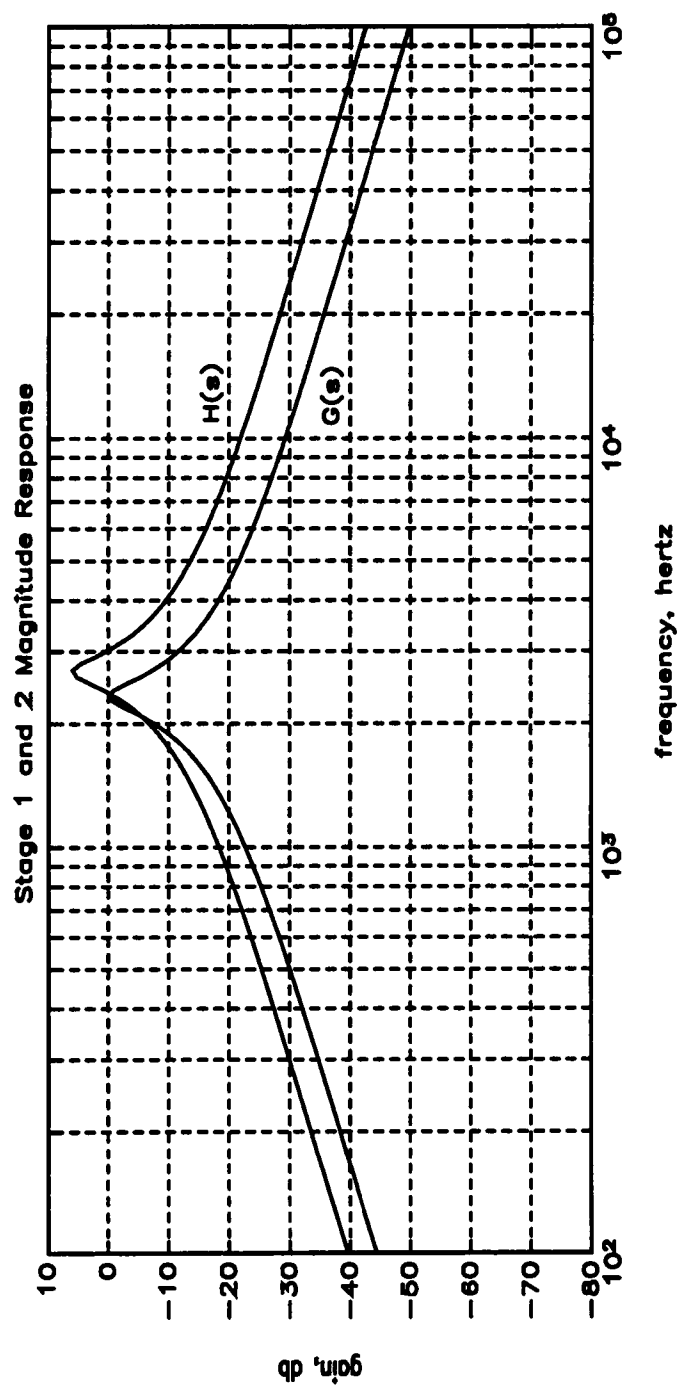


Figure 2.21. Filter stage 1 and 2 magnitude response.

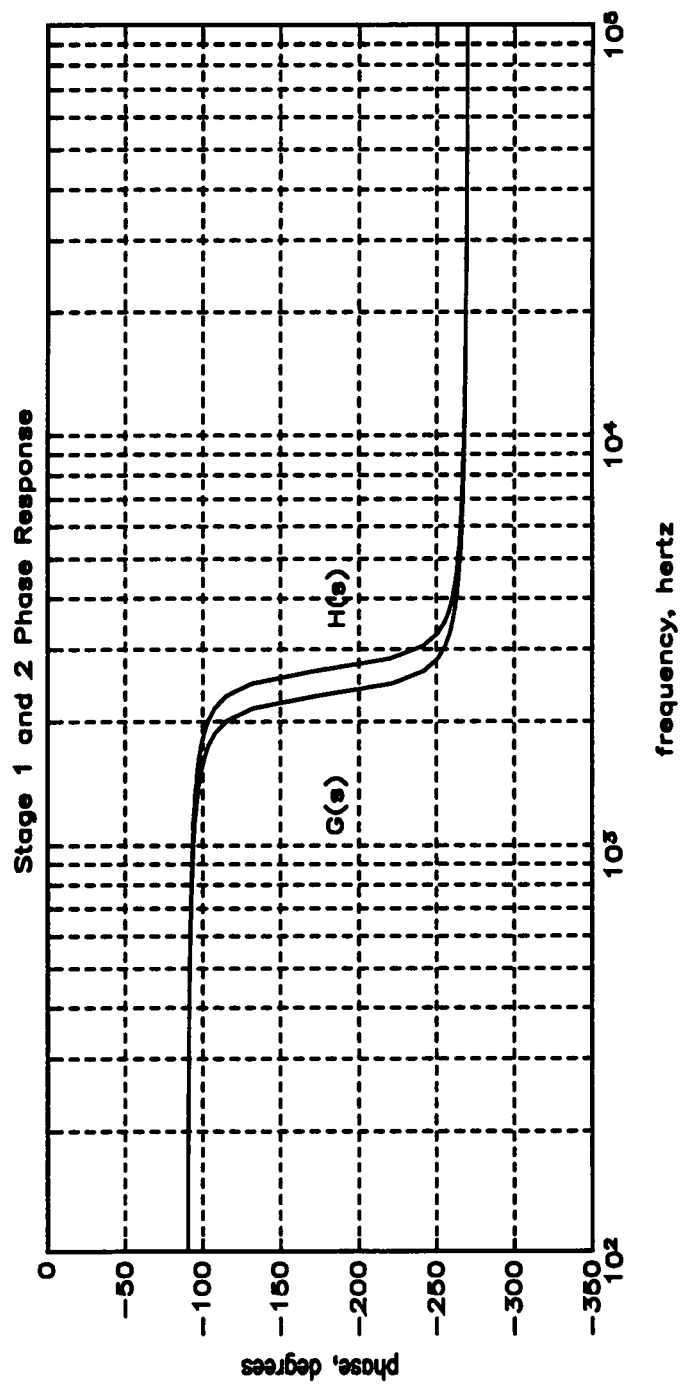


Figure 2.22. Filter stage 1 and 2 phase response.

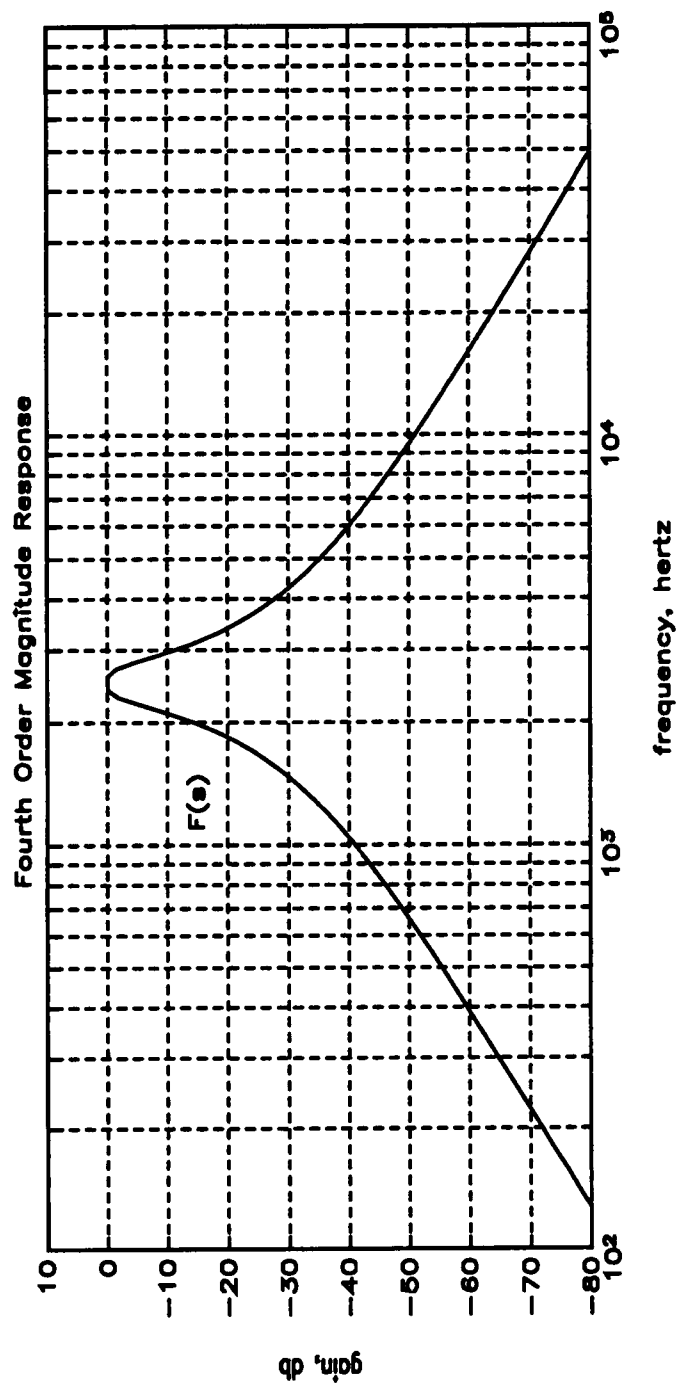


Figure 2.23. Fourth order magnitude response.

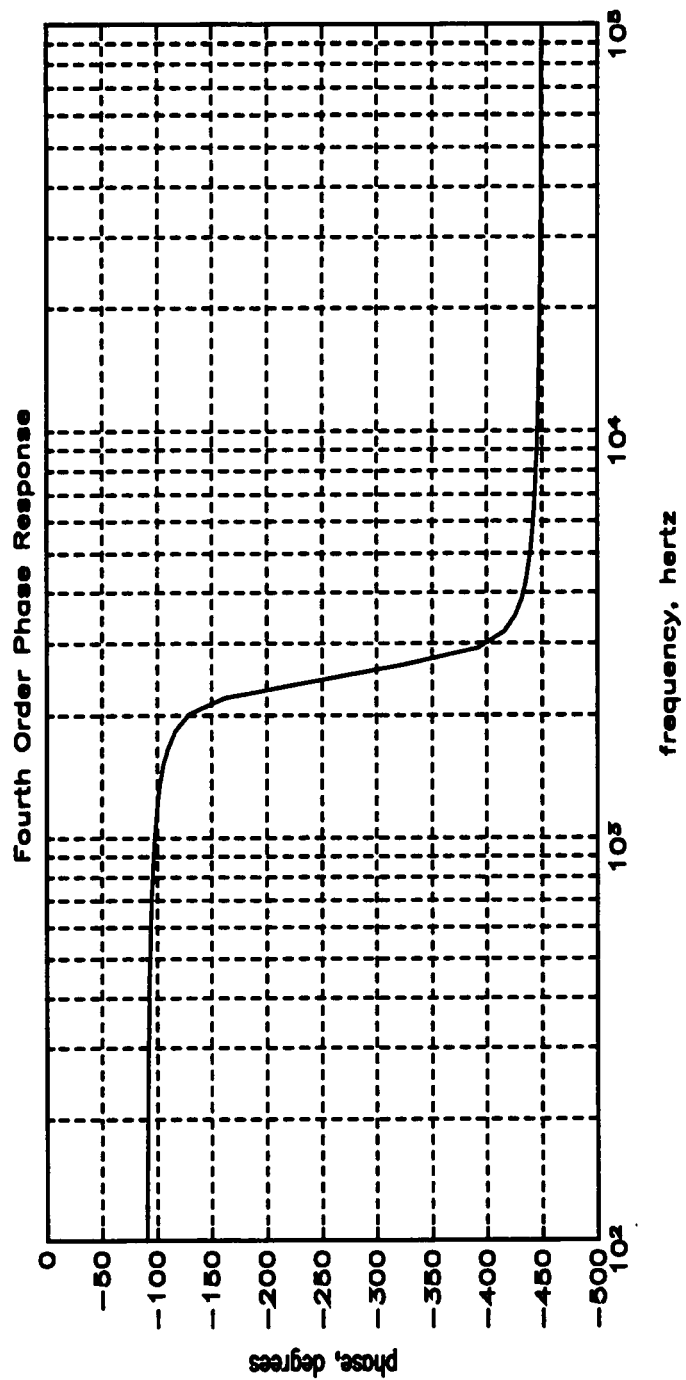


Figure 2.24. Fourth order phase response.

input clock frequency of 250KHz, the passband in Figure 2.23 is 500Hz. From equation 2.8 it can be seen that the Q of the filter is constant and that changing the clock frequency does not change the shape of the response. In fact, when the multiplexer frequency is changed from 250KHz to 500KHz (this also changes the input signal to the filter from 2.5KHz to 5.0KHz, as mentioned previously), the shape of the resulting gain and phase curves are identical to the ones shown in Figures 2.23 and 2.24. This is equivalent to shifting these curves one octave to the right, which means that the passband is 1000Hz with an input clock frequency of 500KHz.

The input and output waveforms for this filter are shown in Figures 2.25 through 2.28. Figures 2.25 and 2.26 are the input and output respectively, for a frequency of 2.5KHz (clock frequency of 250KHz). Figures 2.27 and 2.28 are the input and output respectively, for a frequency of 5.0KHz (clock frequency of 500KHz).

The output of the level shifter circuit for channel 2 is a 2Vp-p square wave in the frequency range $4.800\text{KHz} \leq f_2 \leq 4.999\text{KHz}$ or $2.300\text{KHz} \leq f_2 \leq 2.499\text{KHz}$, depending on the carrier frequency selected for channel 1 (5.000KHz or 2.500KHz). In order to shape this square wave into an acceptable sinusoid and prevent the need for a post switch-capacitor-filter automatic gain control circuit, the output of the digital subtractor in Figure 2.9 is used as the clock input to a filter identical to the one shown in Figure 2.20. The output of the level shifter for channel 2 is used as the input signal to the filter. The resulting sinusoidal output contains distortion in the 1Hz to 200Hz frequency range. This distortion increased with beat frequency and is caused by the leading/trailing edge jitter present at the output of the digital subtractor. Since the output of the digital subtractor,

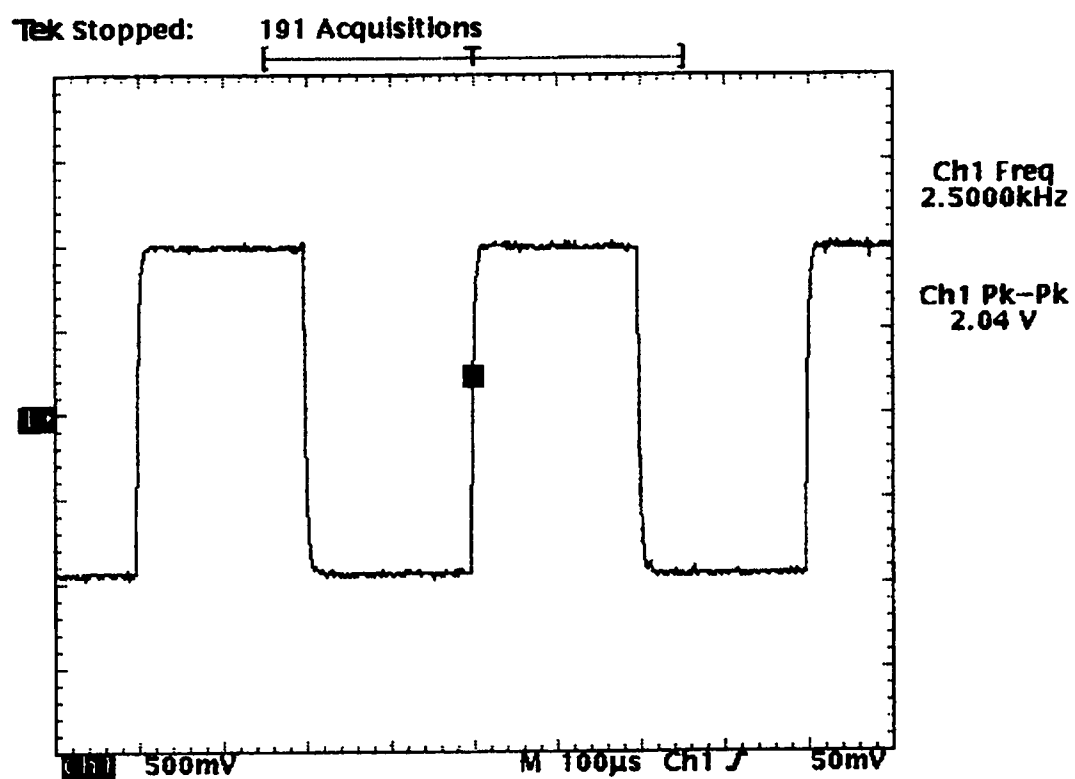


Figure 2.25. Bandpass input, 2.5KHz.

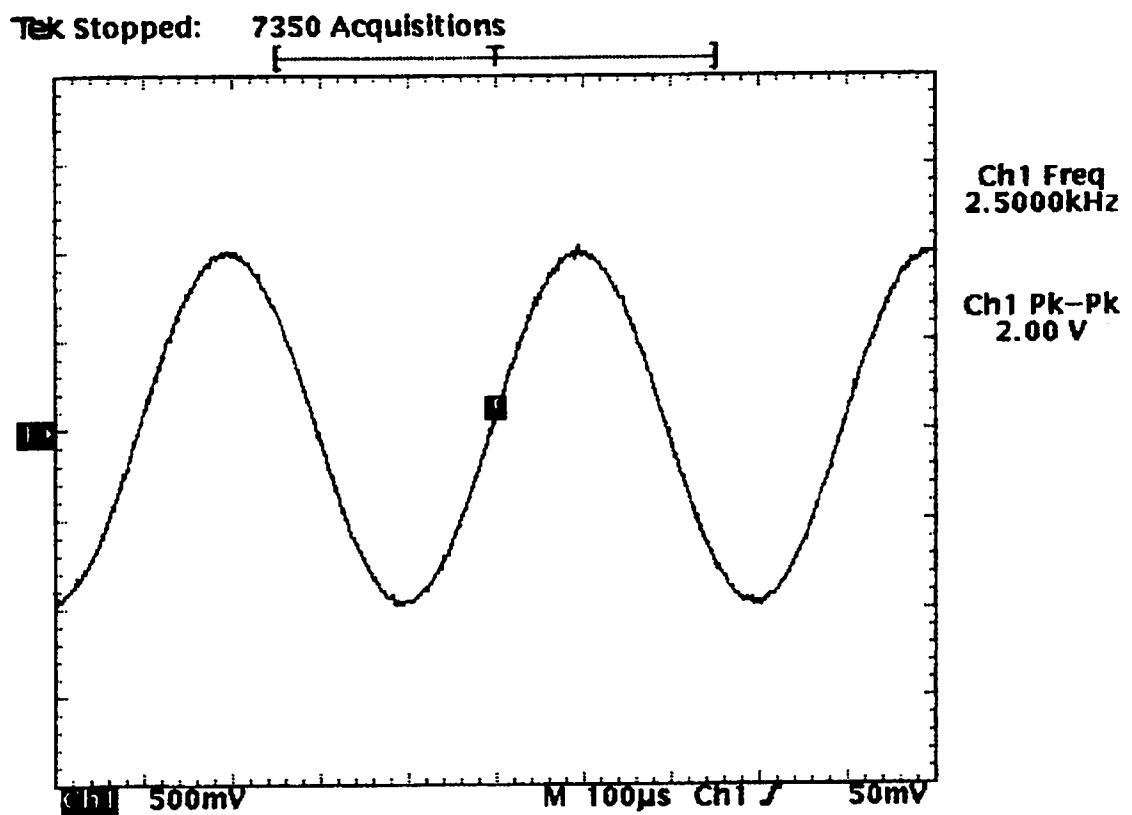


Figure 2.26. Bandpass output, 2.5KHz.

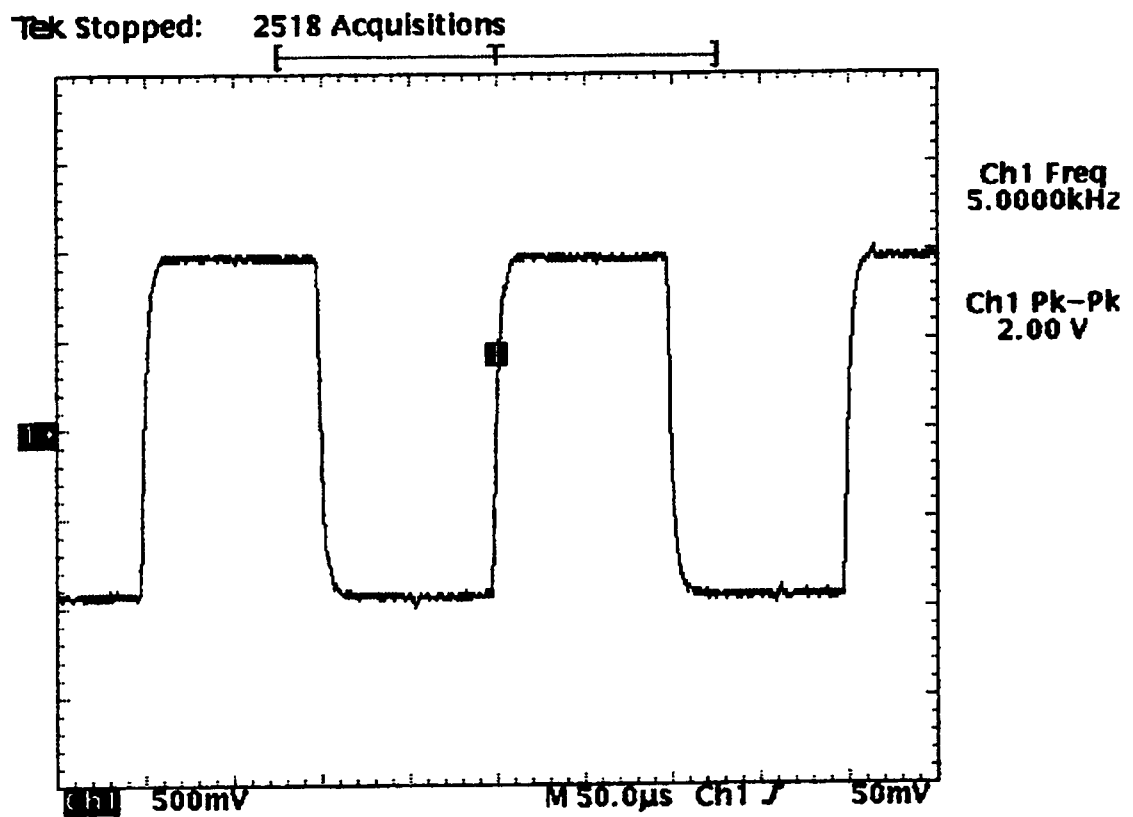


Figure 2.27. Bandpass input, 5.0KHz.

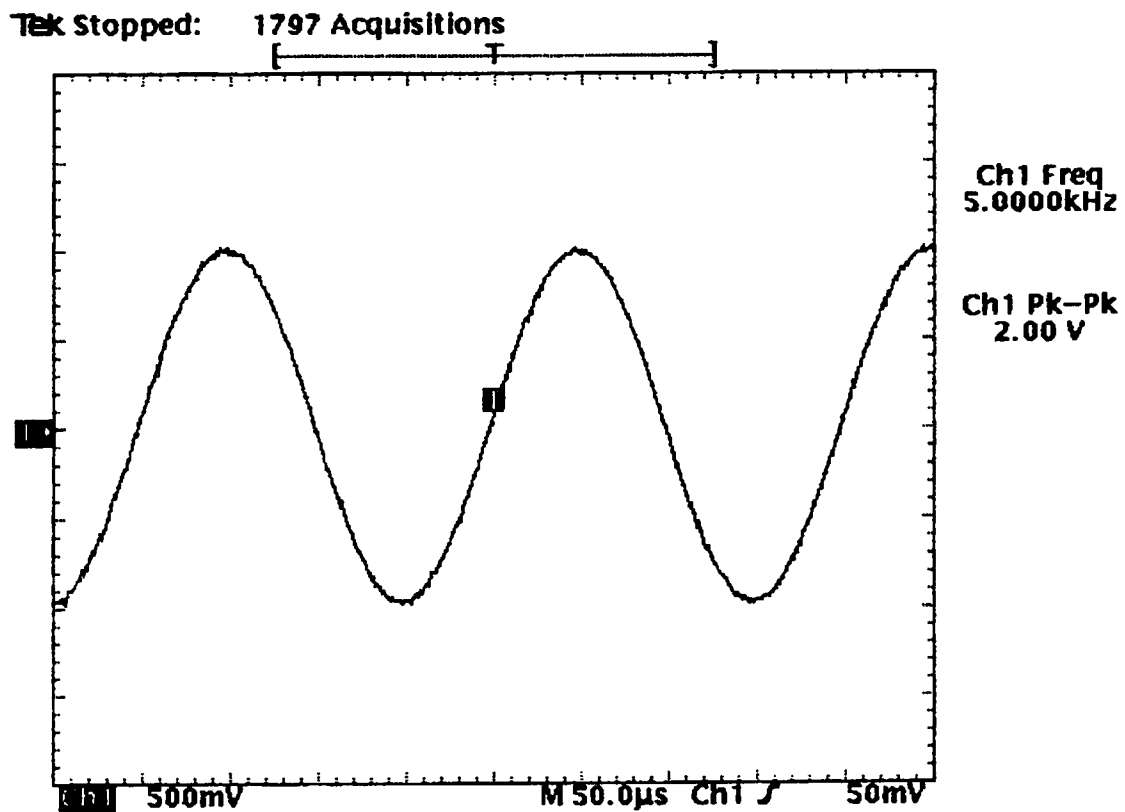


Figure 2.28. Bandpass output, 5.0KHz.

after being divided by 100 and level shifted, is used as the input to the filter, it also contains this same edge jitter. This combination of a jittery clock and input signal results in distortion in the output waveform. In order to minimize this distortion, the multiplexer output signal is used as the clock input to the filter. This is a frequency stable signal that contains no jitter. This results in a large reduction in the filter output distortion but an unacceptable amount still remains. This remaining distortion is due to the leading/trailing edge jitter that is present at the output of the level shifter circuit for channel 2. A side effect of this clock change is now the amplitude of the sinusoidal output of the filter varies as the beat frequency varies. This can be seen from Figure 2.23. If the multiplexer output frequency is 250KHz and the beat frequency is 1Hz, the output of the filter is 2.499KHz with an amplitude of 2Vp-p. As the beat frequency is increased to 200Hz, the filter output frequency decreases to 2.300KHz, resulting in an unacceptably large amplitude change. Another factor contributing to this amplitude change is the inaccuracy in the f_{clk}/f_o ratio versus f_{clk} and Q of the LTC1060 device itself. From the data sheet for the LTC1060, the f_{clk}/f_o and Q deviations are a function of f_{clk} and temperature which result in slight amplitude changes. The f_{clk}/f_o deviation from 100:1 is less than 0.4% for a Q of 5. These changes are small compared to the designed magnitude response of the filter but are still present. It should be noted that the amplitude of the output of channel 1 changes when the clock frequency is changed from 250KHz to 500KHz due to these same inaccuracies. A post switch-capacitor filter automatic gain control circuit is therefore necessary for both channels.

In order to remove the low frequency distortion still present in the filter output of

channel 2, which is due to the frequency jitter present at the output of the digital subtractor (input to channel 2 bandpass after level shifting), it is necessary to highpass filter this signal. An LTC1060, operating in mode 3, is used to implement a fourth order highpass response. The general second order highpass filter is represented by the transfer function

$$X(s) = K \frac{s^2}{s^2 + s \left(\frac{\omega}{Q} \right) + \omega^2} \quad \text{Eq. 2.17}$$

where K is the gain of the filter in the passband, $\omega = 2\pi f_0$ (f_0 is the center frequency of the complex pole pair), Q is a measure of the selectivity of the filter, and s is the Laplace operator. This can be implemented with the LTC1060 where f_0 is given by equation 2.7, Q is given by equation 2.8, and

$$K = -\frac{R_2}{R_1} \quad \text{Eq. 2.18}$$

The design of the fourth order highpass response consists of cascading two second order highpass filters with identical 3db corner frequencies but different Q's. As before, the design was carried out using FilterCAD where the corner frequency was chosen to be 2.5KHz and the passband gain is set to one. The resulting circuit is shown in Figure 2.29. Resistors for stage 1 are numbered R_1 , R_2 , R_3 , and R_4 , while those for stage 2 are numbered R_{1-2} , R_{2-2} , R_{3-2} , and R_{4-2} respectively.

Using the resistor values shown in Figure 2.29, the transfer function for the first

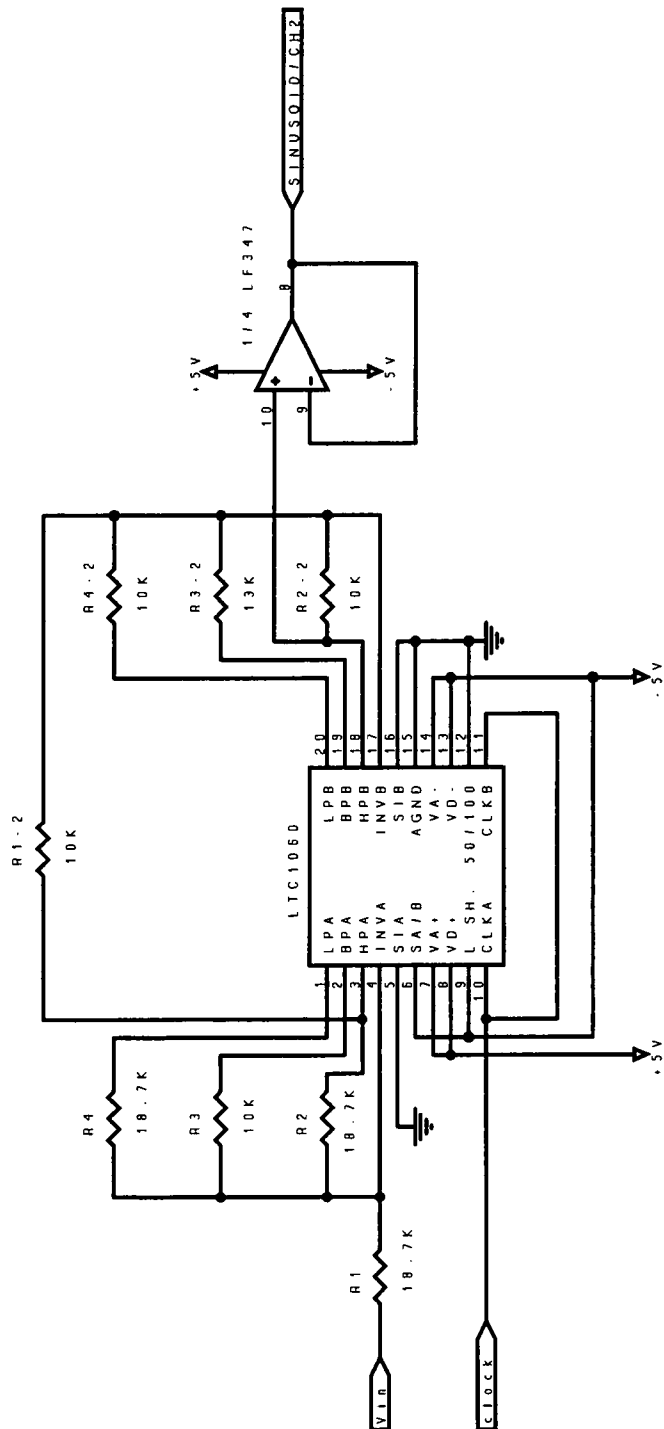


Figure 2.29. Fourth order highpass implementation.

stage can be written as ($f_0=250\text{KHz}$)

$$X(s) = (-1) \frac{s^2}{s^2 + 29373s + 2.467 \times 10^8} \quad \text{Eq. 2.19}$$

where $K = -1$ represents a 180° phase shift from input to output. The poles of this function are $p_1, p_2 = -14687 \pm j5568$ so equation 2.19 can be written as

$$X(s) = (-1) \frac{s^2}{(s + (-14687 + j5568))(s + (-14687 - j5568))} \quad \text{Eq. 2.20}$$

In the same manner the transfer function for the second stage can be found as

$$Y(s) = (-1) \frac{s^2}{s^2 + 12083s + 2.467 \times 10^8} \quad \text{Eq. 2.21}$$

where $K = -1$ represents a 180° phase shift from input to output. The poles of this function are $p_1, p_2 = -6042 \pm j14498$ so equation 2.21 can be written as

$$Y(s) = (-1) \frac{s^2}{(s + (-6042 + j14498))(s + (-6042 - j14498))} \quad \text{Eq. 2.22}$$

Figures 2.30 and 2.31 show the Bode plots for $X(s)$ and $Y(s)$ (magnitude and phase) with the frequency axis in hertz.

The overall filter response is $Z(s)=X(s)Y(s)$. Using equations 2.19 and 2.21 the

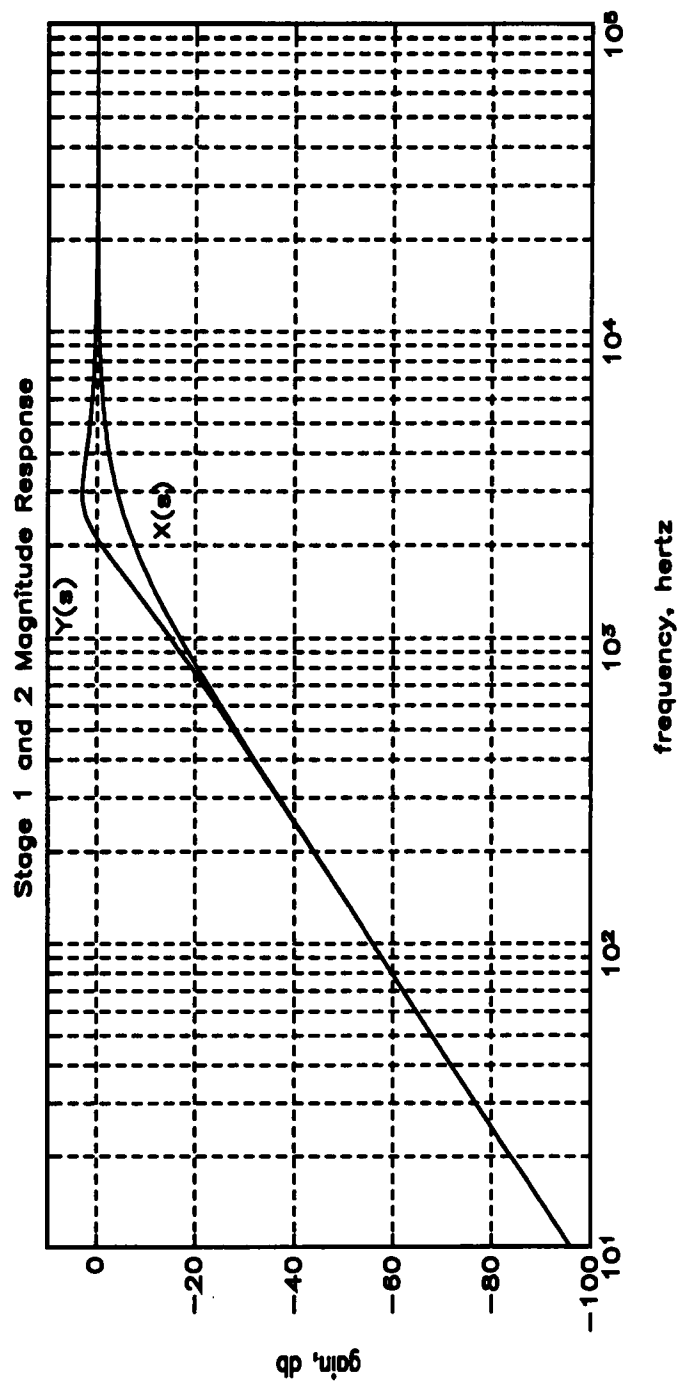


Figure 2.30. Stage 1 and 2 highpass magnitude response.

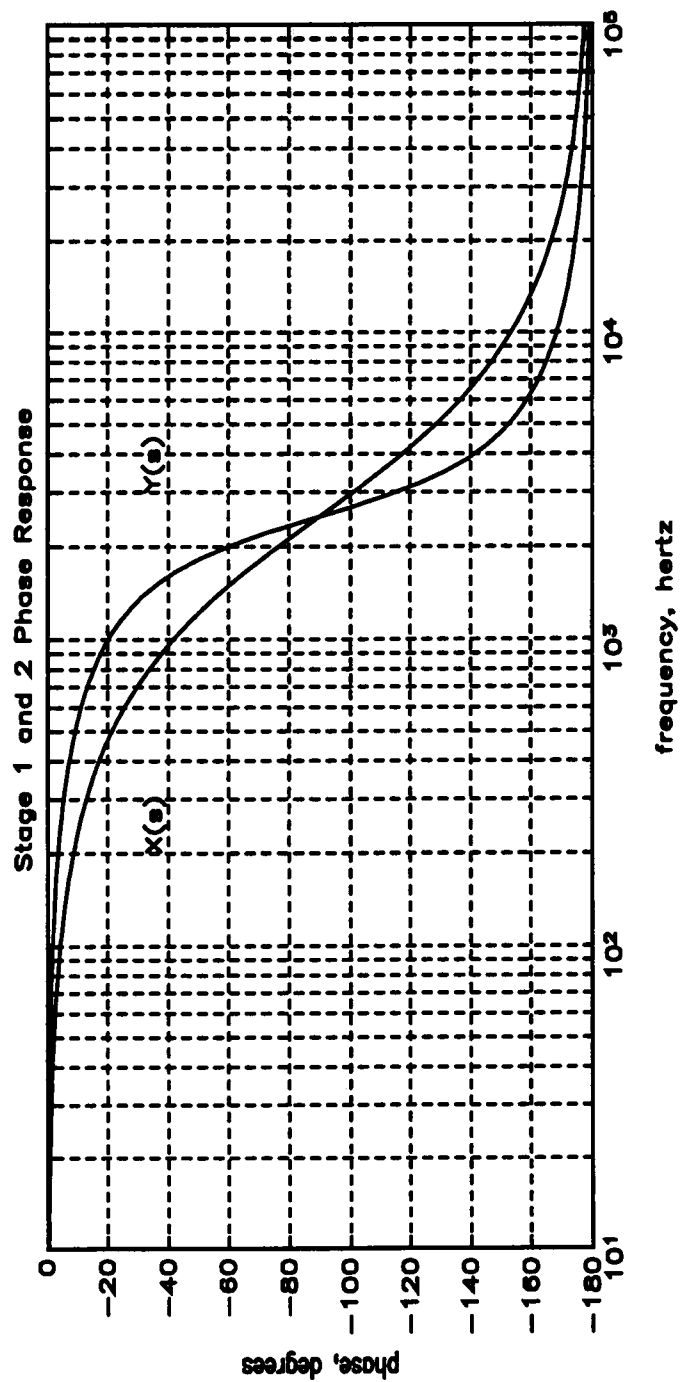


Figure 2.31. Stage 1 and 2 highpass phase response.

transfer function of the fourth order response is found to be

$$Z(s) = +1 \frac{s^4}{s^4 + 41456s^3 + 8.483 \times 10^8 s^2 + 1.023 \times 10^{13} s + 6.086 \times 10^{16}} \quad \text{Eq. 2.23}$$

where $K = +1$ implies a 360° phase shift from input to output. Figures 2.32 and 2.33 are the Bode plots for $Z(s)$ (magnitude and phase) with the frequency axis in hertz. With an input clock frequency of 250KHz, the 3db frequency is 2.5KHz. As stated previously, the Q of the filter is independent of clock frequency so changing the clock frequency to 500KHz just shifts the response curves in Figures 2.32 and 2.33 one octave to the right.

The addition of this highpass filter to the variable frequency channel resulted in unobservable low frequency distortion and an output sinusoid of acceptable spectral purity. One side effect of this additional filtering stage is the increased attenuation due to the location of the cutoff frequency of this highpass filter. These cutoff frequencies (2.5KHz or 5.0KHz) were chosen to maximize the attenuation in the 1Hz to 200Hz frequency range and minimize gain variations in the 2.3KHz to 2.499KHz or 4.8KHz to 4.999KHz frequency ranges.

To summarize the oscillator signal processing circuitry to this point, refer to Figures 2.34 through 2.36. The signal for each channel is level shifted to 2.0Vp-p, then applied to a fourth order bandpass filter. The bandpass output of channel 2 is then processed by the fourth order highpass filter in Figure 2.35 to remove low frequency distortion contributed by the jitter in the input signal. The output of the bandpass filter for channel 1, which is shown in Figure 2.36, is acceptable and requires no further active

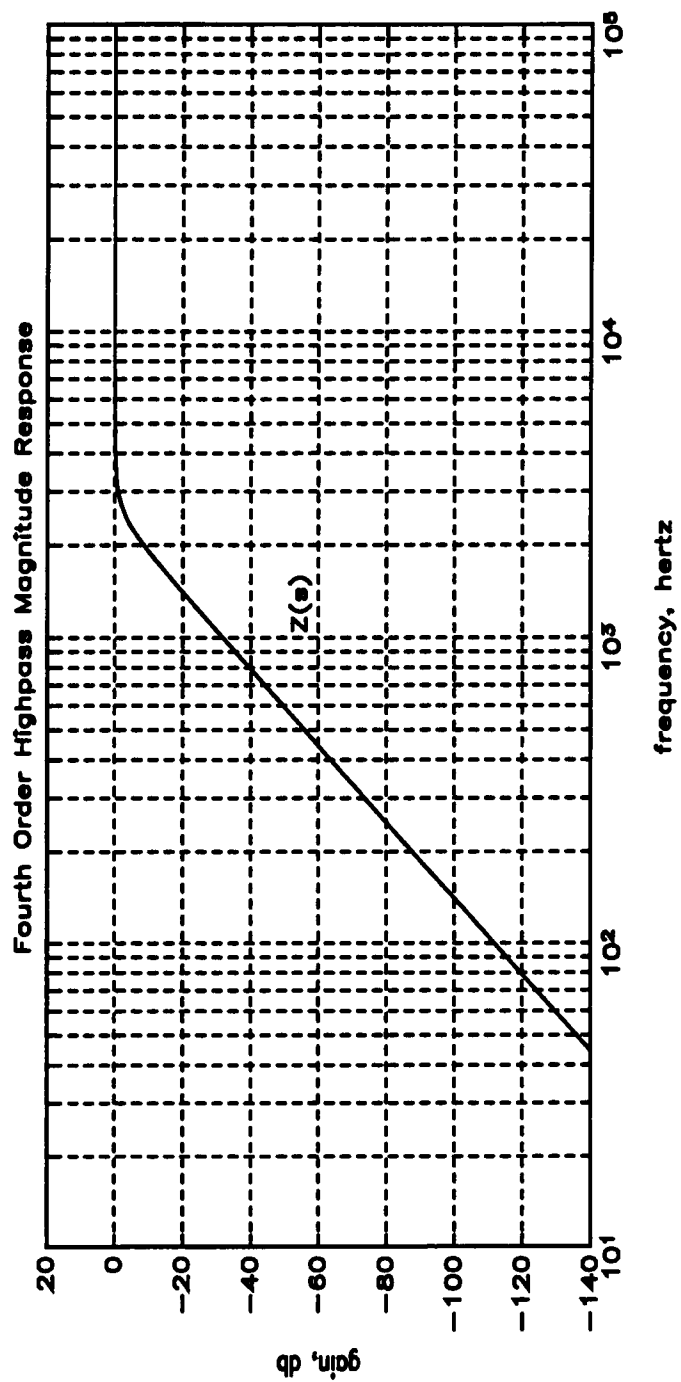


Figure 2.32. Fourth order highpass magnitude response.

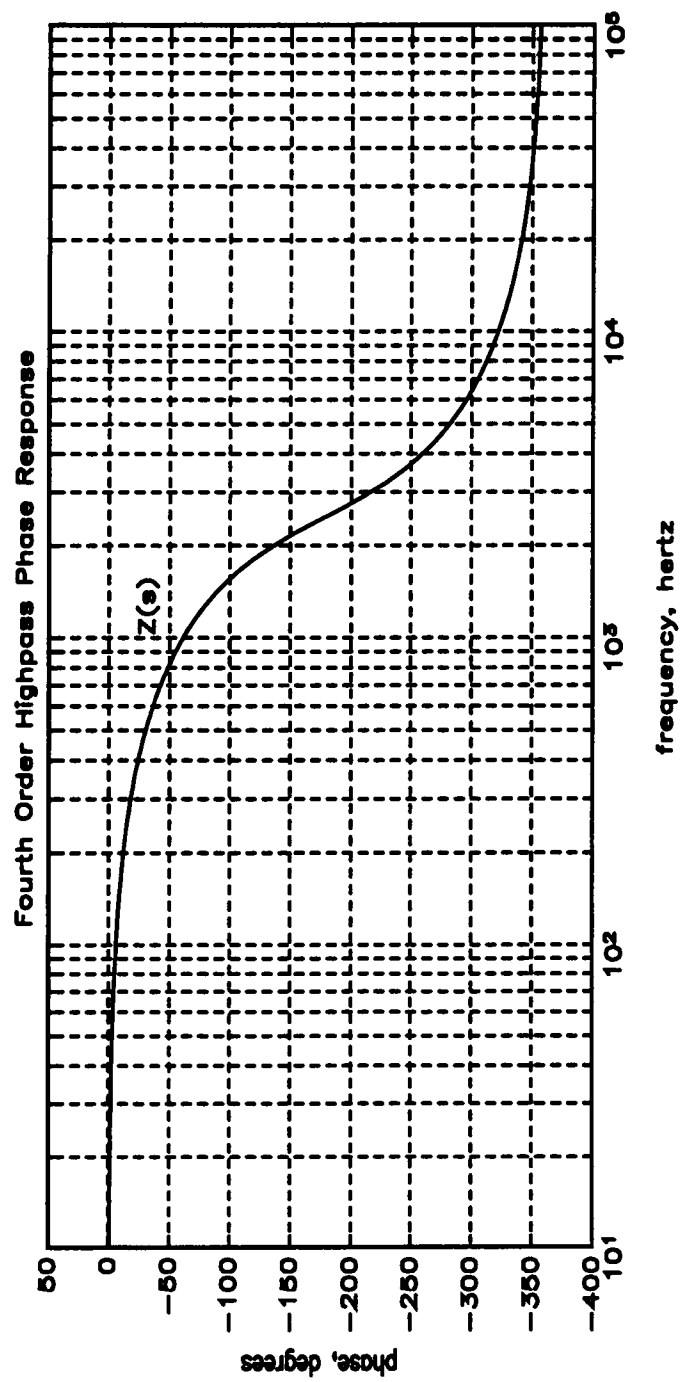


Figure 2.33. Fourth order highpass phase response.

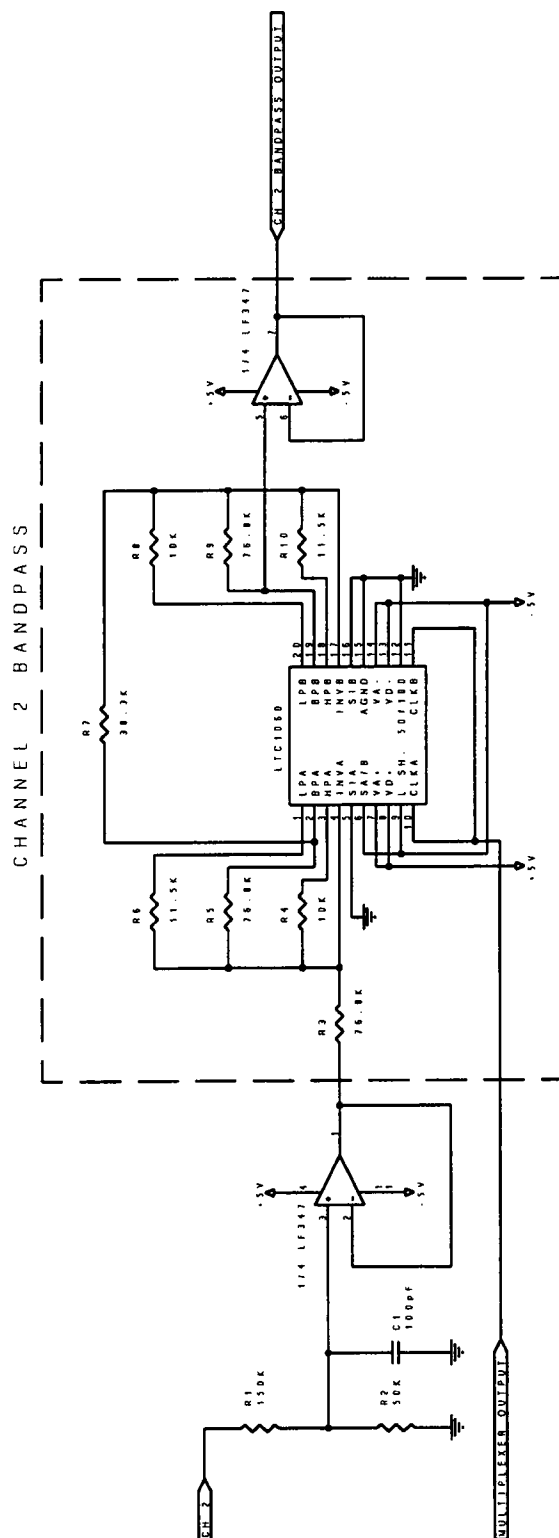
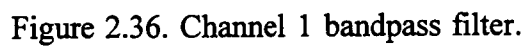


Figure 2.34. Channel 2 bandpass filter.





filtering. All switched-capacitor-filters are clocked by the output of the multiplexer circuit in Figure 2.4.

Now available at the output of the respective switched-capacitor-filters are sinusoids that track each other according to equation 2.1 and whose distortion levels are acceptable. Before the respective bandpass outputs can be processed further, it is necessary to passively filter each output to reduce the discrete steps present which are caused by the switched-capacitor filters. The switched-capacitor-filters are sampled data devices whose output signals contain significant energy at the clock frequency. When viewed with an analog oscilloscope, the output signals contain discrete steps of width τ where τ is the period of the clock input. A passive bandpass topology was chosen to eliminate the dc output offset voltage of the LTC1060 and provide smoothing of the discrete steps. Figure 2.37 shows the passive bandpass filter implementation. The Bode plot for the filter in Figure 2.37 is shown in Figures 2.38 and 2.39.

The sinusoidal signals at the output of each switched-capacitor filter can be mathematically described as $v(t) = \sin(\omega t)$ since the peak amplitude is 1Vp. The maximum voltage step size at a clock frequency of f_{clk} is $V_{step} = (dv(t)/dt) / f_{clk}$ where $dv(t)/dt = \omega \cos(\omega t)$. The maximum rate of change of a sine wave occurs at the zero crossings or $t=0$ so the maximum voltage step size present in the output of the switched-capacitor filters is $V_{step} = (\omega \cos(0)) / f_{clk} = (2\pi f_{max})/f_{clk}$. When $f_{clk} = 500\text{KHz}$, $f_{max} = 5\text{KHz}$, and when $f_{clk} = 250\text{KHz}$, $f_{max} = 2.5\text{KHz}$ so the ratio $f_{max} / f_{clk} = 0.01$ at both carrier frequencies which gives a maximum voltage step size of $V_{step} = 2\pi (0.01) = 62.8\text{mV}$.

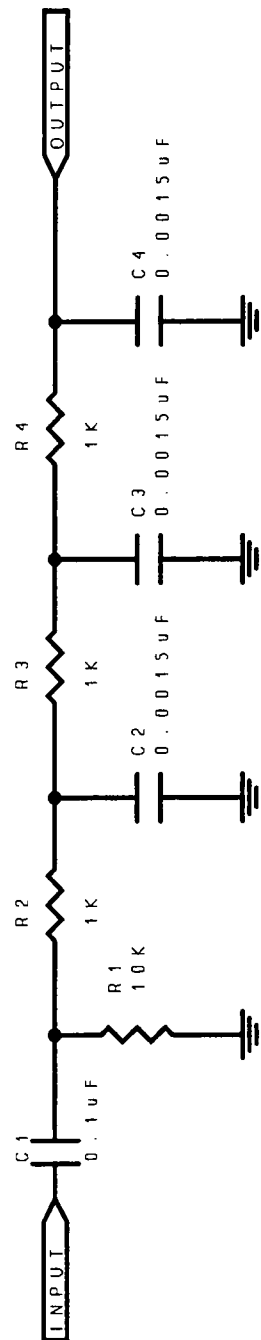


Figure 2.37. Post LTC1060 smoothing filter.

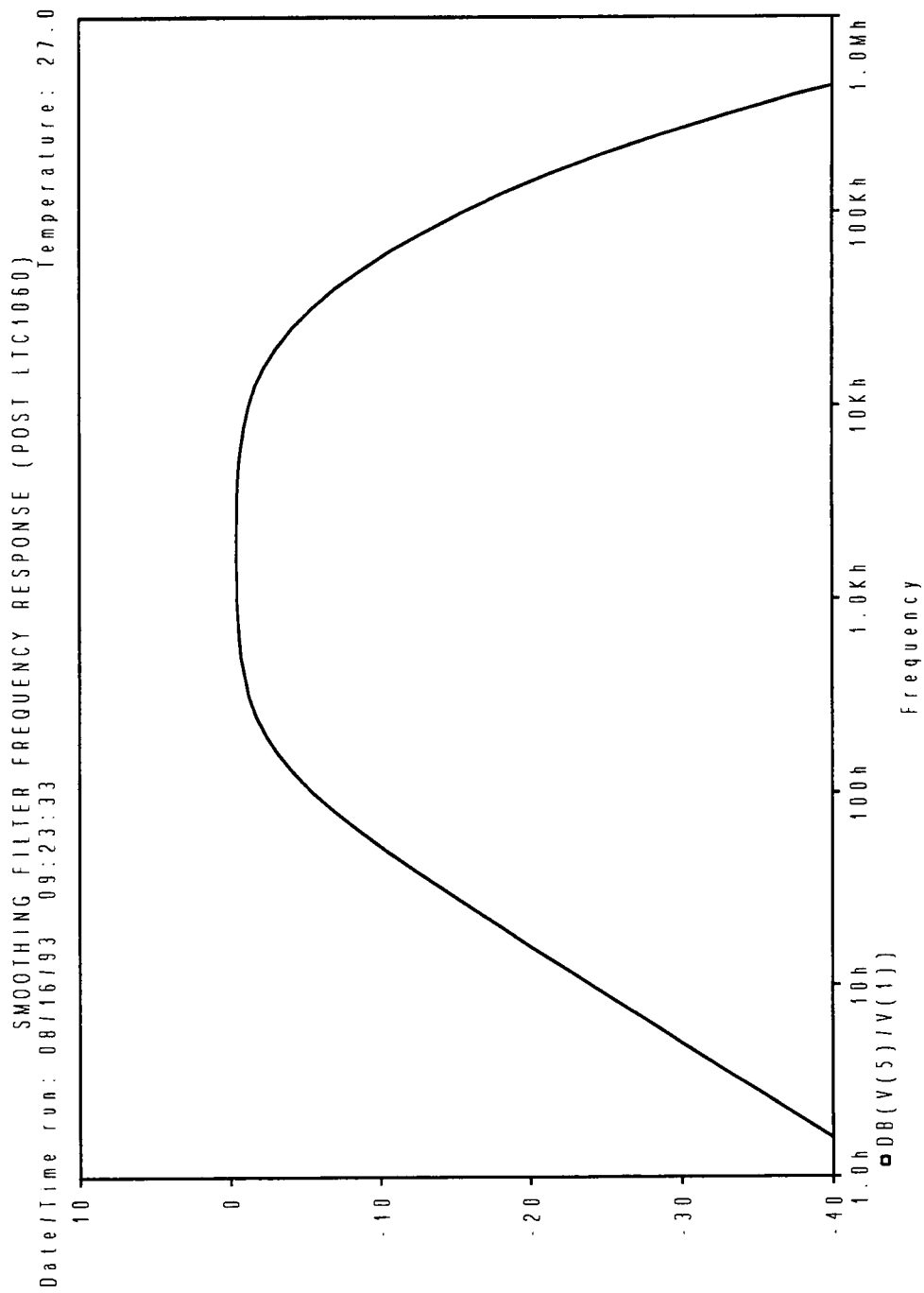


Figure 2.38. Smoothing filter magnitude response.

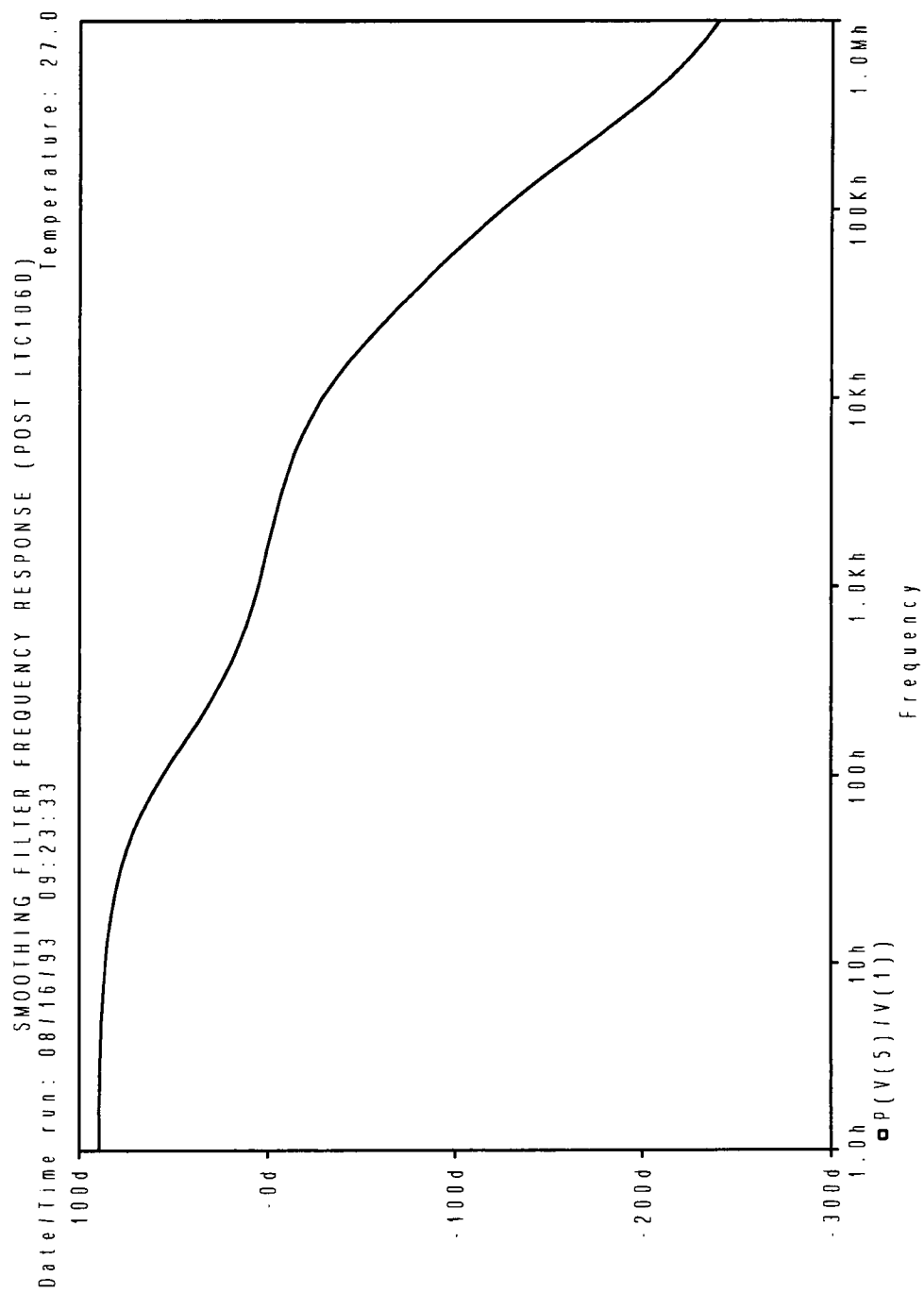


Figure 2.39. Smoothing filter phase response.

Using the PROBE feature of PSPICE² [9], the gain of the filter at 250KHz is measured to be $G_{250\text{KHz}} = -28.5\text{db}$ or $G_{250\text{KHz}} = 0.0375$, and the gain at 500KHz is $G_{500\text{KHz}} = -42.5\text{db}$ or $G_{500\text{KHz}} = 0.0075$. These values can be verified by referring to Figure 2.38. At a carrier frequency of 2.5KHz the maximum voltage step size is $(62.8\text{mV})(0.0375) = 2.35\text{mV}$ and at a carrier frequency of 5KHz the maximum voltage step size is $(62.8\text{mV})(0.0075) = 0.471\text{mV}$.

In addition to providing attenuation to the discrete voltage steps present in the sinusoidal outputs of the respective switched capacitor filters, the passive bandpass filter removes the output offset of the LTC1060 switched capacitor filters. A detrimental side effect of the passive bandpass topology is that slight gain changes occur as the input signal frequency changes from a minimum frequency of 2.300KHz to a maximum of 4.999KHz. The gain of the filter changes from a maximum of $G_{2.3\text{KHz}} = 0.949$ at 2.3KHz to $G_{5.0\text{KHz}} = 0.930$ at 5.0KHz (measured during simulation). For a 2Vp-p input signal this results in an output amplitude of 1.898Vp-p at 2.3KHz decreasing to 1.860Vp-p at 5.0KHz. This amplitude variation, although slight, is too large to allow the outputs of the respective filters to be used as reference signals for the final output amplifiers. Each signal must therefore be amplitude stabilized independent of frequency which is the subject of the next section.

² PSPICE is a registered trademark of Microsim Corporation.

2.2.4 Automatic Gain Control

The gain variations in the respective oscillator signal processing chains discussed in section 2.2.3 are too large to allow the output signals of the respective switched-capacitor-filters to be used as reference signals for the remaining circuitry. Therefore, the output of the signal processing chain for each channel is processed by an automatic gain control (AGC) circuit to provide constant amplitude signals. This AGC circuit is built around an AD734 4-quadrant multiplier/divider. Before discussing the complete AGC circuit, an explanation of the AD734 itself is necessary.

The AD734 is an accurate, wideband (10MHz full power bandwidth) 4-quadrant analog multiplier that implements the transfer function [10]

$$W = A \left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{U} - (Z_1 - Z_2) \right) \quad \text{Eq. 2.24}$$

where the quantities in equation 2.24 are defined in Figure 2.40. The AD734 provides user control of the denominator voltage U , unlike older multipliers where the denominator voltage is a constant. The internal details of the denominator control circuitry are shown in Figure 2.41. Referring to Figure 2.41 and noting that the external voltages X_1 - X_2 , Y_1 - Y_2 , Z_1 - Z_2 , and U are converted internally to proportional currents, connecting pin 13 (denominator disable) to pin 14 (positive supply) opens the bypass around Q_d . This also disables the internal current source of I_u and the collector current of Q_u must provide the denominator current. This is accomplished by applying an external control voltage across

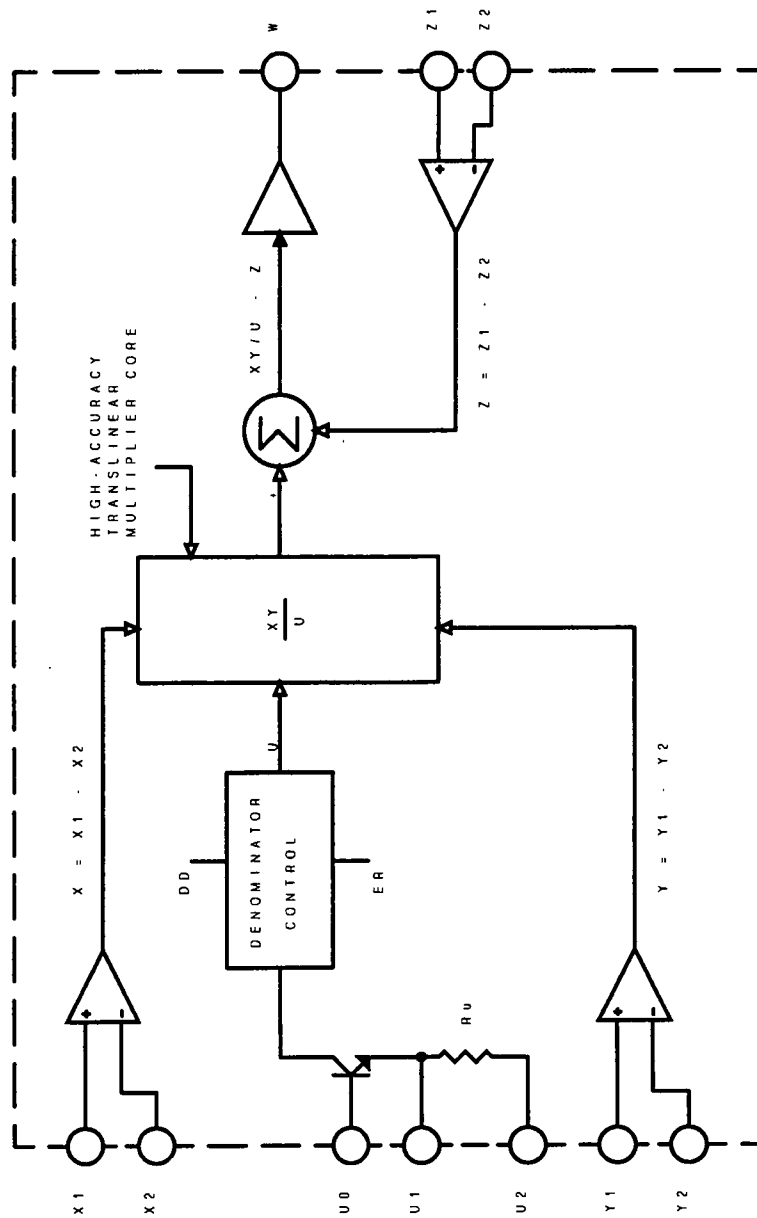


Figure 2.40. AD734 internal details.

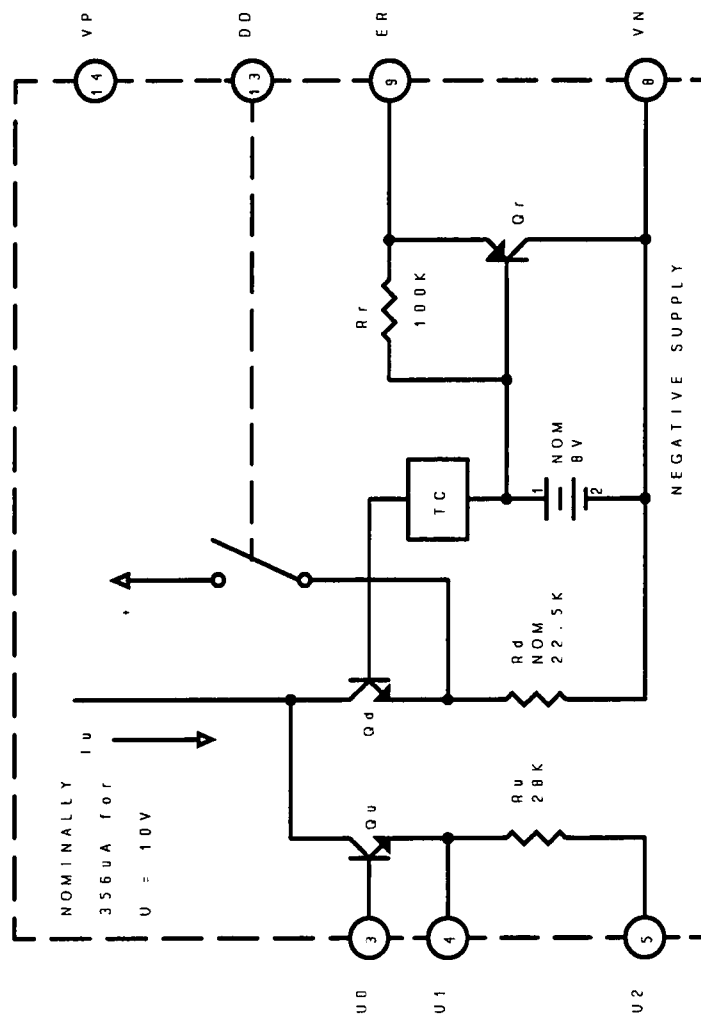


Figure 2.41. AD734 denominator control internal details.

U_0 and U_2 . The denominator current I_u is now proportional to $U=U_0-U_2$ minus the V_{be} drop of Q_u . This V_{be} error is placed inside a feedback loop in the AGC circuit and is not important in this application. The X, Y, and Z input amplifiers in Figure 2.40 respond to difference signals between their respective inputs and each has a nominal full scale differential input range of $\pm 10V$. The major difference between these input amplifiers and an ordinary op-amp is their differential input resistance of $50K\Omega \pm 20\%$. This differential input resistance is formed by real resistors and is not a small-signal approximation so this resistance must be taken into account when designing external circuitry to interface to these amps. The output of amps X and Y are converted to proportional currents and applied, along with I_u , to a translinear multiplier core which produces the ratio XY/U . This ratio, summed with Z, and amplified by the output amplifier produces the multiplier output W.

To provide the required AGC function, the circuit shown in Figure 2.42 was developed [11]. The input signal (output of the passive bandpass circuit in Figure 2.37) is applied to the X_1 input. An adjustable voltage is applied to the Y_1 input. The Z_1 input is connected to the W output and Z_2 is connected to analog ground. This forces a negative feedback path around the AD734 output amplifier (refer to Figure 2.40). Op-amp B and capacitor C_1 form an integrator with a current summing node at its inverting input. The output of the multiplier is negative peak detected by D_3 and C_2 , buffered by op-amp 2B, and applied to the integrator summing junction through R_4 . The Y_1 reference voltage, buffered by op-amp 2A is applied through the D_1 - R_3 combination to the integrator summing junction. D_1 is included to prevent interaction between the reference voltage at

Y_1 and the integrator. When the voltage at the cathode of D_1 is equal to the voltage at the output of op-amp 2B, the currents in R_3 and R_4 will be equal and the output voltage of op-amp B will remain at a constant level to maintain the required loop gain. If the input signal X_1 is zero, the current through D_1 and R_3 will cause the integrator output to ramp negative until clamped by D_2 . D_2 is present to prevent op-amp B from saturating thereby reducing the loop recovery time. With the integrator output clamped at approximately -0.6V, the denominator input (U_0 to U_2) is zero (the denominator current I_u in Figure 2.41 is cutoff). Rewriting equation 2.22 where $Z_1=W$ and $Z_2=Y_2=U_2=0$, we have

$$W = \left(\frac{X_1 - X_2}{U_0} \right) Y_1 . \quad \text{Eq. 2.25}$$

By inspection of equation 2.25, if U_0 is -0.6V (effectively 0V as far as the AD734 is concerned) then the gain under these circumstances is limited to the gain of the AD734 output amplifier which is typically 72db. A consequence of the high gain with no signal present at the X_1 , X_2 input is that the input offset voltage of the X_1 , X_2 input is amplified by the gain also. The maximum input offset voltage of the X input, over temperature, is 25mV. This offset, multiplied by the open loop gain of 72db would saturate the output amp. To prevent this from occurring, dc feedback from the output to the X_2 input is used. This dc feedback network is composed of R_5 , C_5 , and op-amp A. A buffered version of the output offset at W is applied to the inverting input X_2 . This reduces the output offset of the AD734 to the input offset voltage of the AD712 which is 4mV maximum over 0°C to 70°C. The AD712 op-amp is a dual, precision, high-speed BiFET amp and was chosen

due to its low input bias current (100pA max), low initial offset voltage (0.3 μ V typical), and low input offset voltage drift (20 μ V/ $^{\circ}$ C). Amplifiers A and B are contained in one IC as are 2A and 2B so good tracking over temperature is maintained.

Since the input at X is the output of the passive bandpass filter of channel 2, the rate of amplitude variation of this signal is directly dependent on the rate at which the front panel beat frequency control is changed (R_{100} in Figure 2.6). Assuming this control cannot be rotated from min to max in less than 20msec, the loop response of the AGC is set to 5msec. The time constant of R_4 and C_1 is set to 1msec to set the loop response to 5msec. This means the loop will stabilize within 5msec of an amplitude change on the X input.

Results of breadboard evaluation of the AGC circuit reveal that the peak output at W will track the reference voltage at Y_1 over the range $1V \leq Y_1 \leq 10V$ as long as the peak amplitude of the input signal at X_1 does not fall below approximately 100mV peak. Figures 2.43 through 2.46 show the static or steady state response of the circuit for a variety of input amplitudes and frequencies which cover the intended range of application. A dynamic test of the AGC circuit, performed by rapidly sweeping the beat frequency while observing the amplitude of the output signal revealed no observable amplitude changes.

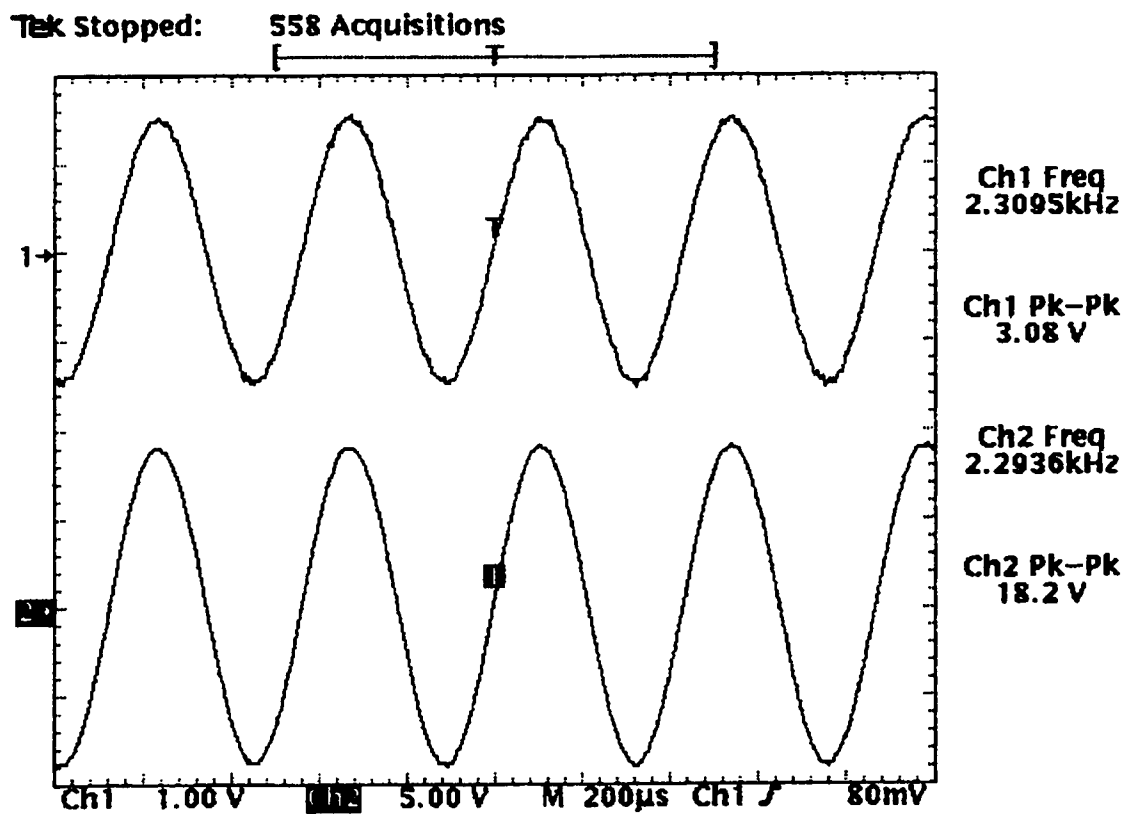


Figure 2.43. AGC response, 2.3KHz, midrange.

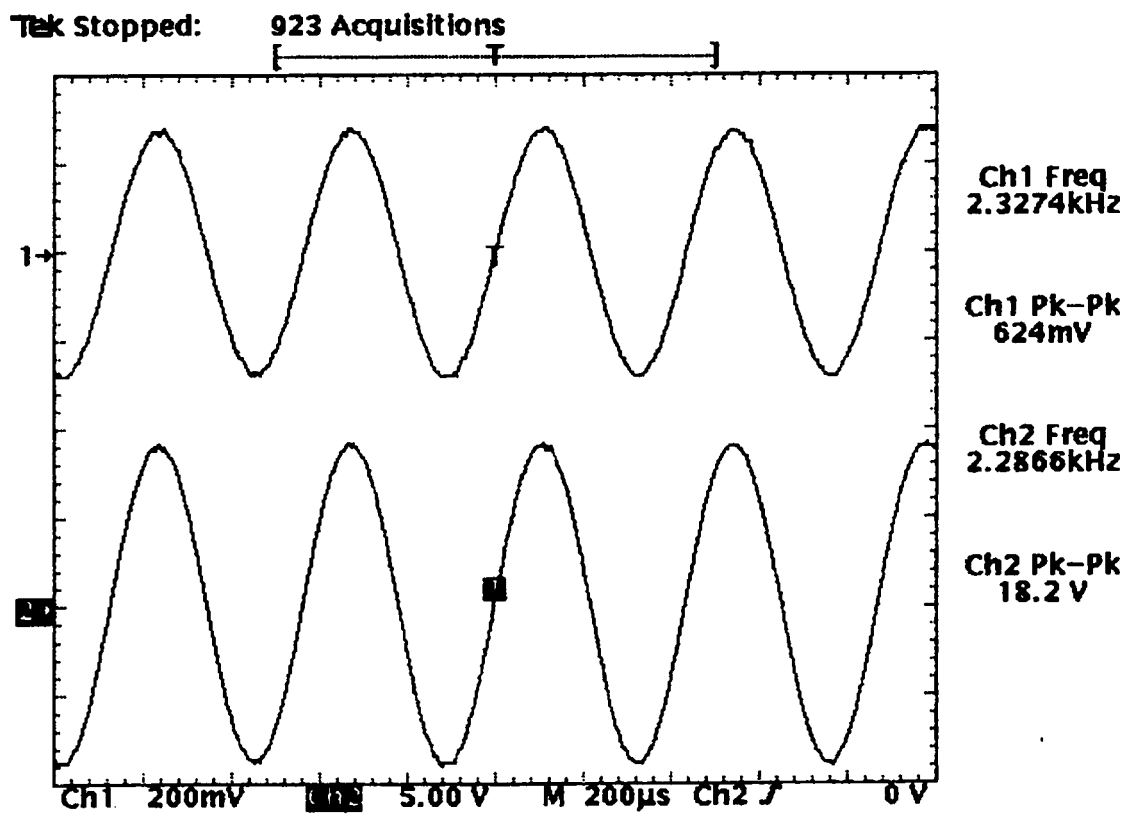


Figure 2.44. AGC response, 2.3KHz, low range.

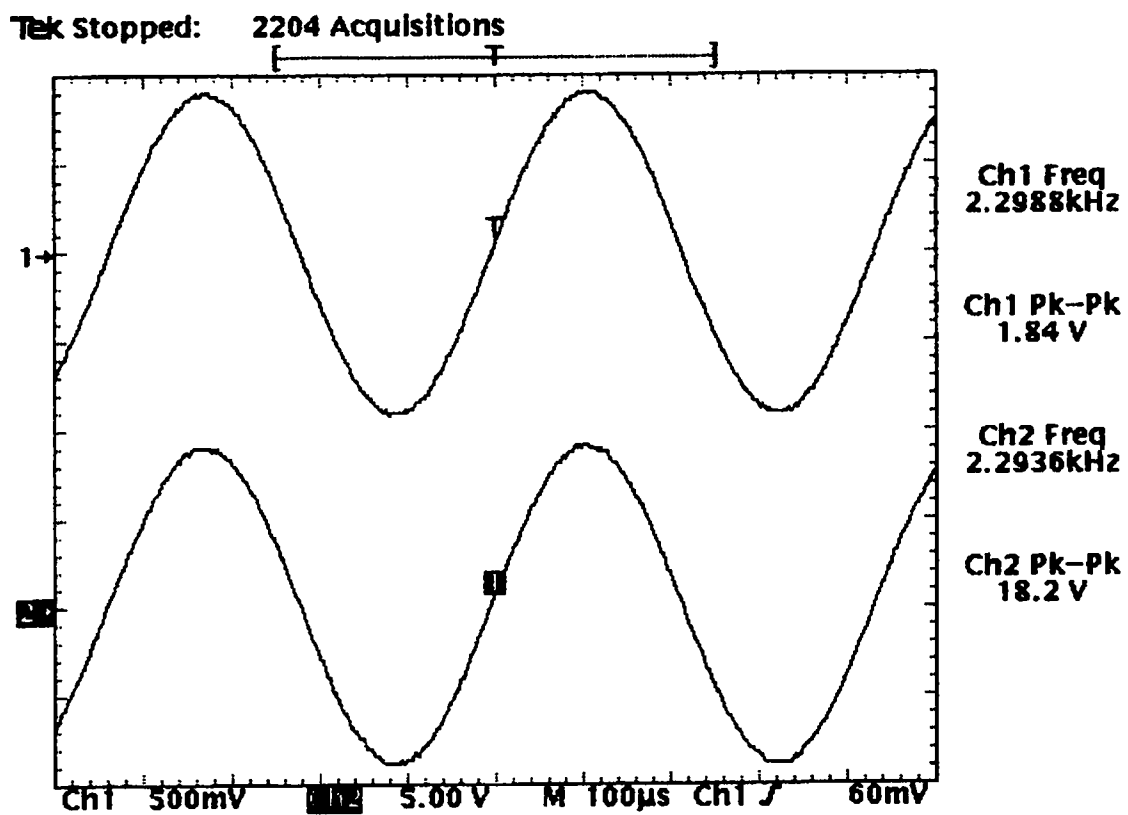


Figure 2.45. AGC response, 2.3KHz, target range.

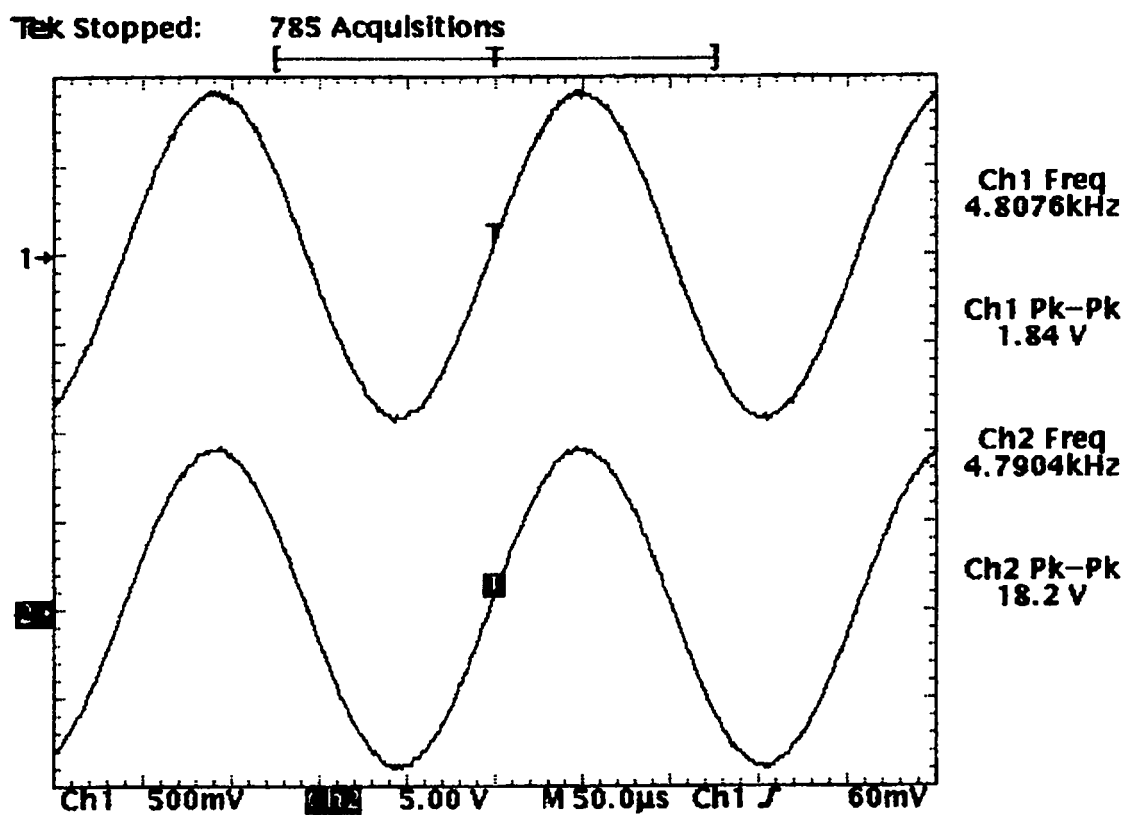


Figure 2.46. AGC response, 5.0KHz, target range.

2.3 Intensity and Modulation Control

In order to provide amplitude control for each channel, the AGC outputs are multiplied by a dc reference signal derived from a front panel potentiometer (intensity setting pot). The same dc reference signal is used for both channels so only one intensity control is required. Two AD632, 4-quadrant precision multipliers are used to implement this function as shown in Figure 2.47. The AD632 is functionally equivalent to the AD734 with the exception that no provision is made for user control of the denominator voltage, which is fixed at 10V, and the small signal bandwidth is substantially lower, having a typical value of 1MHz.

The dc reference signal is passed through a CD4053 double-pole single-throw analog switch and connected to the Y_1 input on both multipliers. The output of the respective AGC circuits are applied to the X_1 inputs. The transfer function realized by this circuit connection is

$$V_p = \frac{(X_1)(Y_1)}{10V} \quad \text{Eq. 2.26}$$

where V_p is the peak amplitude of the output signal at pin 2 of the multiplier. The circuit that generates the dc reference signal is shown in Figure 2.48. R_2 is a potentiometer located on the front panel of the instrument and is used to control the intensity (amplitude). An LM358 op-amp is used to buffer this reference and this signal is passed to one pole of the CD4053 analog switch. Since this reference signal is always positive

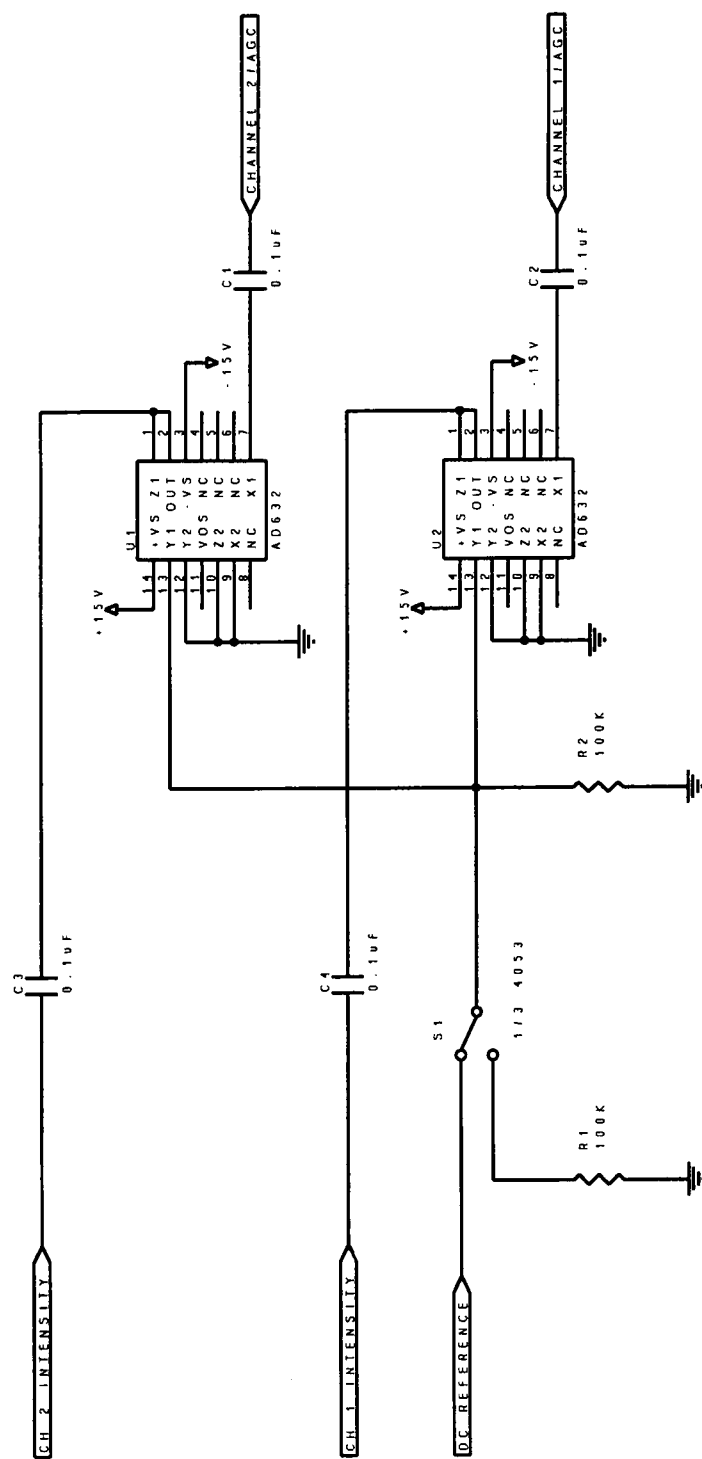


Figure 2.47. Manual intensity control.

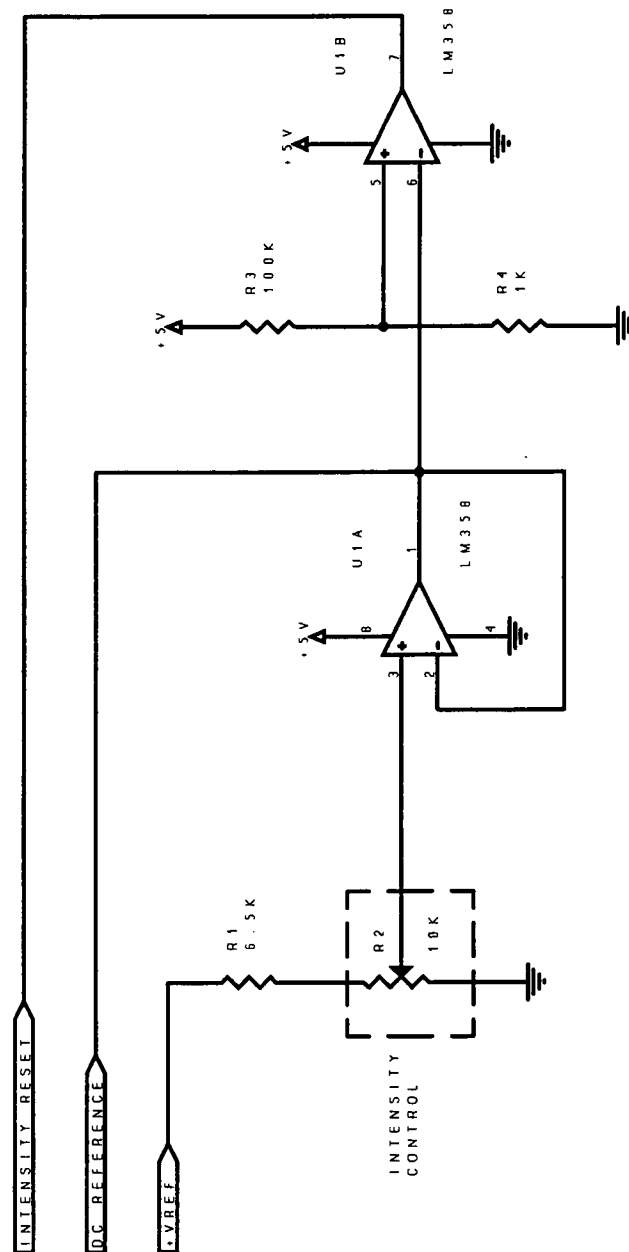


Figure 2.48. DC reference circuit.

($0V \leq \text{DC REFERENCE} \leq 1V$), the LM358 was chosen because it is designed to operate from a single supply and because of its large dc voltage gain of 100db. Op-amp U1B (U1A and U1B are contained in the same IC package) is configured as a comparator. The voltage at pin 5 of U1B is approximately 50mV. If the instrument resets for any reason (mode change, power failure, carrier frequency change), the intensity control must be rotated to the minimum position and then set to the desired level. This produces a pulse out of U1B to reset all the safety circuitry to normal operation. During the time the instrument is in a reset condition, the logic control of S1 in Figure 2.47 keeps the switch connected between R_1 and common, where R_1 pulls the input signal to the multipliers to 0V. R_2 is provided so the output of S1 does not rise during switching. Capacitors C_1 through C_4 provide ac coupling of the circuit to eliminate the dc offsets associated with the multipliers.

To generate the amplitude modulated output signal shown in Figure 1.2, the output of each manual gain control multiplier in Figure 2.47 is summed in an op-amp summing circuit. This circuit is shown in Figure 2.49. Each channel has a gain of 0.5 in order to prevent an amplitude that is larger than the individual channel amplitudes. R_3 provides an adjustment so the output signal peak voltage can be set to 1V. The CD4053 consists of three double-pole single-throw switches along with some level shifting circuitry. In Figure 2.49 pin 8 of the CD4053 is 0V and pin 7 is -5V. This configures the device to switch analog signals between $\pm 5V$ with a 0V to 5V logic control signal. The MOD/UNMOD signal is 0V to 5V hence this configuration. In Figure 2.49, when MOD/UNMOD is high, the amplitude modulated signal in Figure 1.2 is present on the

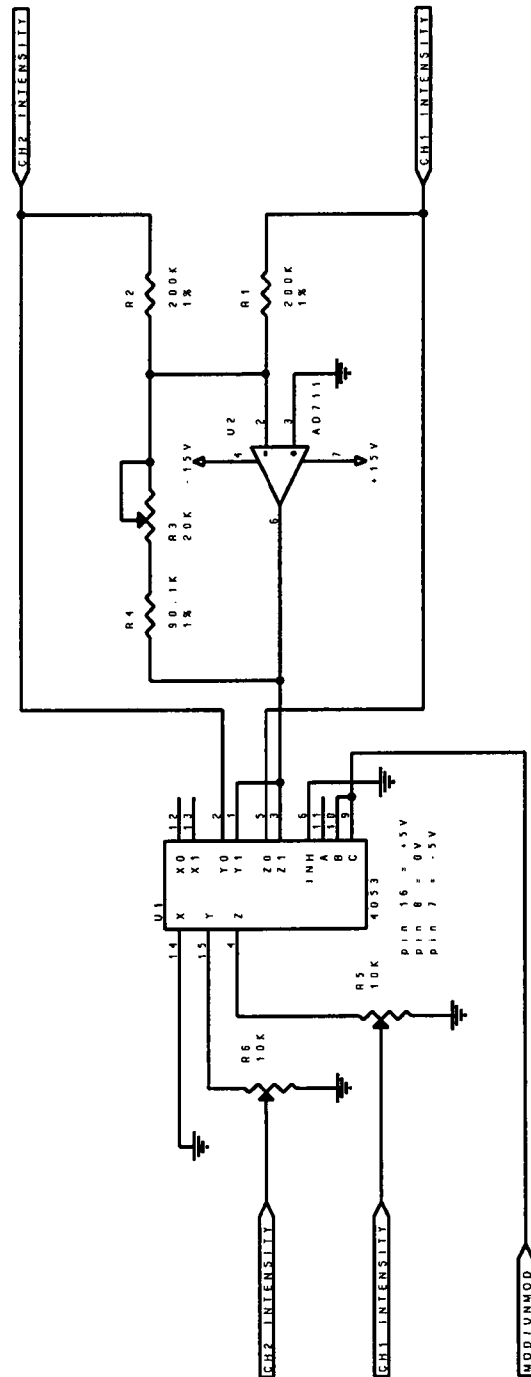


Figure 2.49. Summing/switching circuit.

Y and Z outputs. This allows the user to treat two separate locations, albeit with the same amplitude signal. Resistors R_5 and R_6 provide individual adjustment of the full scale output current for each constant current output amplifier which is necessary due to gain mismatches between the output stages.

To summarize the design to this point, we now have two sinusoidal signals that track each other according to equation 2.1 where f_1 is either 2.500KHz or 5.000KHz, f_2 is 2.300KHz to 2.499KHz or 4.800KHz to 4.999KHz (exactly where in these ranges being controlled by the user via the beat frequency control) with amplitude controlled by the intensity setting on the front panel of the instrument. The next step is to amplify these signals and apply them to the patient in the appropriate manner. This topic is covered in the next section.

2.4 Constant Current Output Stage Overview

The signals present at the output of the manual gain control circuitry are voltage mode signals so a transformation to current mode signals is required before application to the patient. The amplifier topology that implements this transformation for each signal is a transconductance amplifier which delivers a constant current despite load impedance changes.

The basic transconductance topology used is shown in block diagram form in Figure 2.50. This topology uses two feedback loops to set the voltage and current gain of the basic amplifier. The load (patient) is transformer coupled to provide impedance

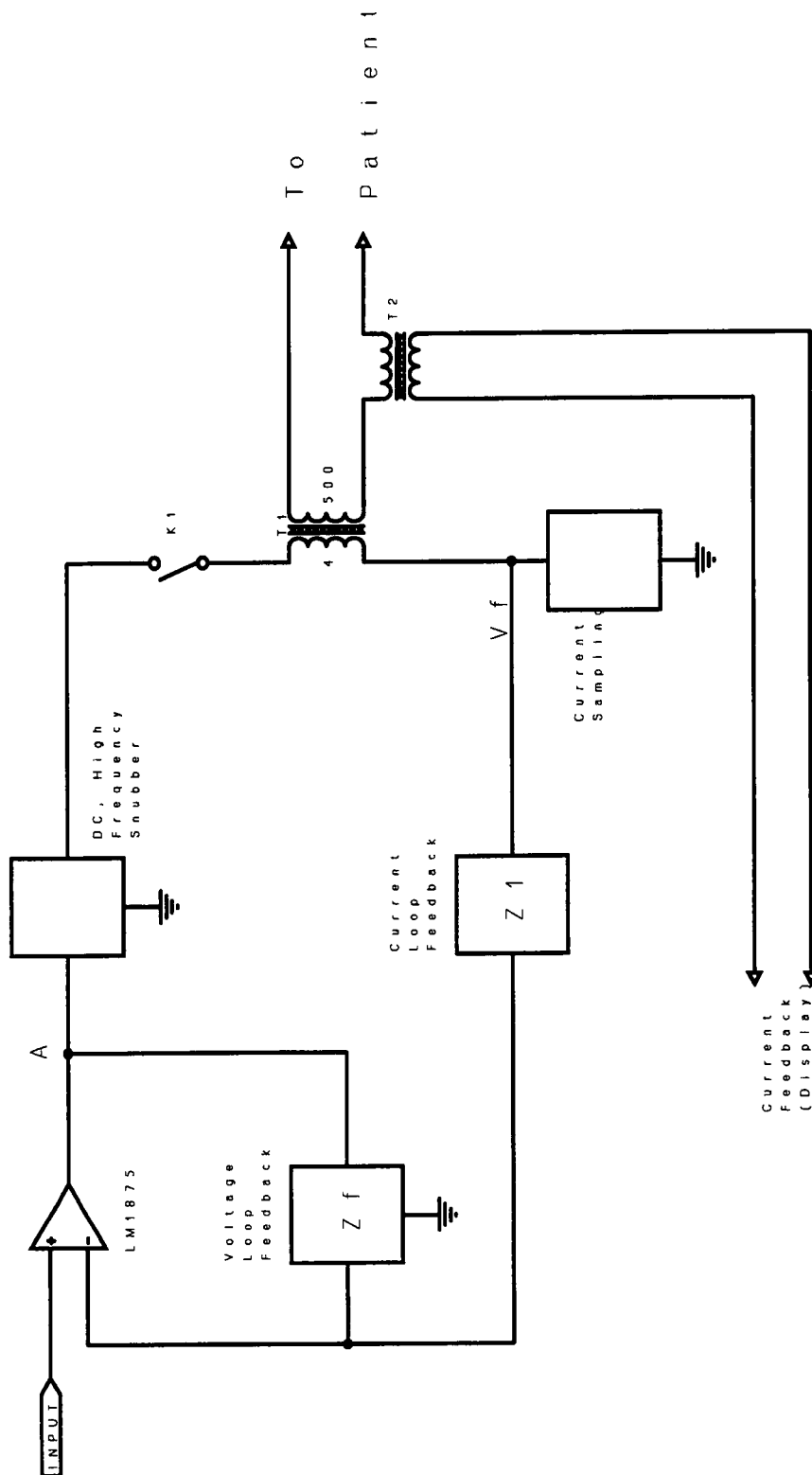


Figure 2.50. Output stage block diagram.

matching and isolation. The basic amplifier has a noninverting gain from the noninverting input of the LM1875 power amplifier to the output at point A which is set by the two-port network Z_f and the current loop network Z_1 . The current feedback signal V_f , which is proportional to the transformer primary current, is multiplied by an inverting gain which is set by Z_f and Z_1 .

To understand the operation of the circuit, assume that a constant amplitude (voltage) input signal is present and a current is flowing in a load which is connected to the transformer secondary. If the load impedance were to increase for some reason, the secondary current would decrease, causing a proportional decrease in the primary current. This reduction in the primary current would cause V_f to be reduced proportionately, which effectively increases the error signal at the input of the amplifier. This would increase the amplifier output at point A causing the transformer primary current (and also the secondary current) to be restored toward its original value. It should be mentioned that the current sampling network in Figure 2.50 is simply a 0.18Ω resistor connected between the lower tap of T1's primary and ground. This means an increase or decrease of T1's primary current will be detected as an increase or decrease of V_f respectively. If the load impedance were to decrease, the secondary current (and primary current) would increase, causing an increase in V_f . This increase in V_f reduces the error signal and the amplifier output at point A. This also restores the primary and secondary currents toward their original values.

The block labeled DC, High Frequency Snubber in Figure 2.50 is a passive two-port network that capacitively couples the output of the basic amplifier to the transformer

and provides a high impedance network for high frequency signals that might appear at the amplifier output. It also contains a lowpass passive RC filter to shunt high frequency signals to ground. Transformer T2, connected in series with the secondary of T1, is used to measure the output current and is fed back to the display board for further processing.

2.4.1 Impedance Matching and Isolation

The equivalent load impedance that an average patient presents to an electrical stimulus is modeled [12] as shown in Figure 2.51. The $100\text{K}\Omega$ resistor models the equivalent skin resistance to the flow of direct current and the R_i , C network accounts for the increased current flow with increasing frequency. R_i covers the range $100\Omega \leq R_i \leq 500\Omega$ depending on the particular location of the human body under consideration. This wide range of R_i , which is a measure of the internal or subcutaneous impedance, is due to differing internal structural details from point to point in human tissues. The power amplifier in Figure 2.50 is an audio power amplifier designed to drive a 4Ω load. To match this output impedance with R_i in Figure 2.51, an audio transformer (T1 in Figure 2.50) is connected with its 4Ω winding to the power amplifier and its 500Ω winding is coupled to the patient. This provides an "average" impedance match (average because R_i varies as a function of treatment location) with the patient and thus maximum power transfer from amplifier to patient.

In addition to impedance matching, T1, in conjunction with relay contacts K1, serve as an isolation barrier. The Food and Drug Administration (FDA) requirements for

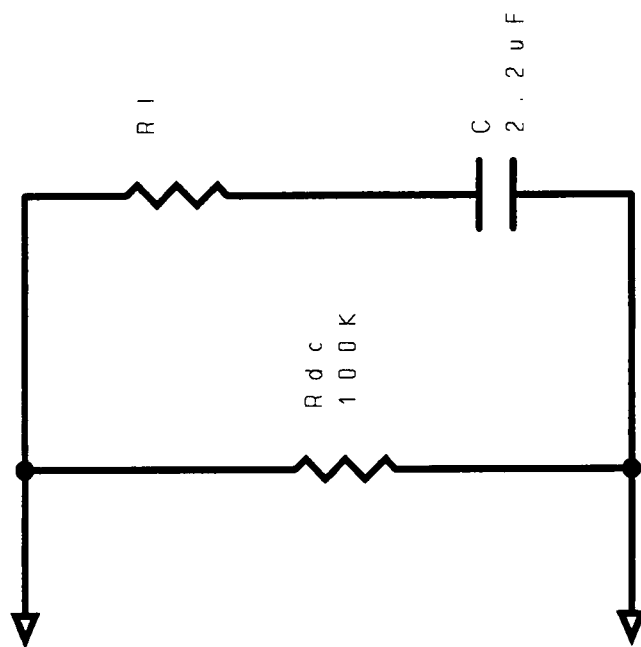


Figure 2.51. Equivalent patient load.

electrical apparatus [13] stipulate that the instrument must be capable of withstanding 4000V (dc or ac rms, 60Hz) between the patient connections and chassis ground for at least one minute with the instrument in an unpowered state. The setup for this test is shown in Figure 2.52. Note that the instrument power supply isolation transformers primary taps must be shorted during this test. From Figure 2.50, with the instrument in an unpowered state, relay contacts K1 will be open, which means the primary of T1 will be floating with respect to chassis ground. Transformer T2 is a current transformer whose action depends on the secondary current in T1. With the patient connections shorted as in Figure 2.52, no current will flow in the secondary of T1 (primary of T2) and the output voltage of T2 will be zero volts. This configuration should pass this particular test but without access to the necessary test equipment (hi-pot tester), there was no way to verify this assumption.

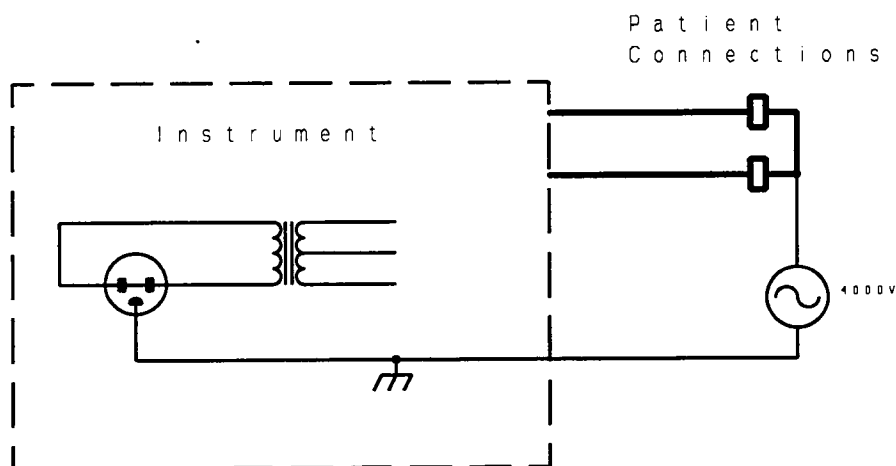


Figure 2.52. Isolation test setup.

2.4.2 Power Amplifier Frequency Response

The detailed schematic of the output transconductance amplifier is shown in Figure 2.53. The required transfer function is $I_{\text{secondary}}/V_{\text{input}}$. Since the secondary current of the output transformer T1 in Figure 2.53 is theoretically related to the primary current by the turns ratio, the transfer function I_p/V_{input} will be developed instead of $I_{\text{secondary}}/V_{\text{input}}$. To gain an understanding of how the various resistors affect the midband gain, the transfer function for the midband gain will be developed first. Referring to Figure 2.53, the development of this gain equation is based on the following assumptions; (1) the LM1875 power op-amp will be modeled as an ideal op-amp having an infinite gain, input resistance, and bandwidth, and (2) $C_2 = C_4 = 0$, $C_3 = C_p = C_1 = \infty$, and $L_1 = 0$. With these assumptions, neglecting higher order terms gives the midband gain as

$$\frac{I_p}{V_{\text{input}}} = \frac{\left[1 + \frac{R_2}{R_1} + \frac{R_3}{R_1} + \frac{R_3}{R_4} + \frac{R_3 R_2}{R_1 R_4}\right]}{\left[\frac{R_{\text{load}}}{N^2} + \frac{R_2 + R_3}{\left(\frac{R_1}{R_s} + 1\right)} + \frac{R_3 R_2}{R_4 \left(\frac{R_1}{R_s} + 1\right)}\right]} \quad \text{Eq. 2.27}$$

where R_{load} is the patient resistance and N is the turns ratio of the output transformer. The turns ratio of the transformer is given by

$$N = \sqrt{\frac{R_{\text{secondary}}}{R_{\text{primary}}}} = \sqrt{\frac{500}{4}} = 11.18 \quad \text{Eq. 2.28}$$

so equation 2.27 can be simplified as

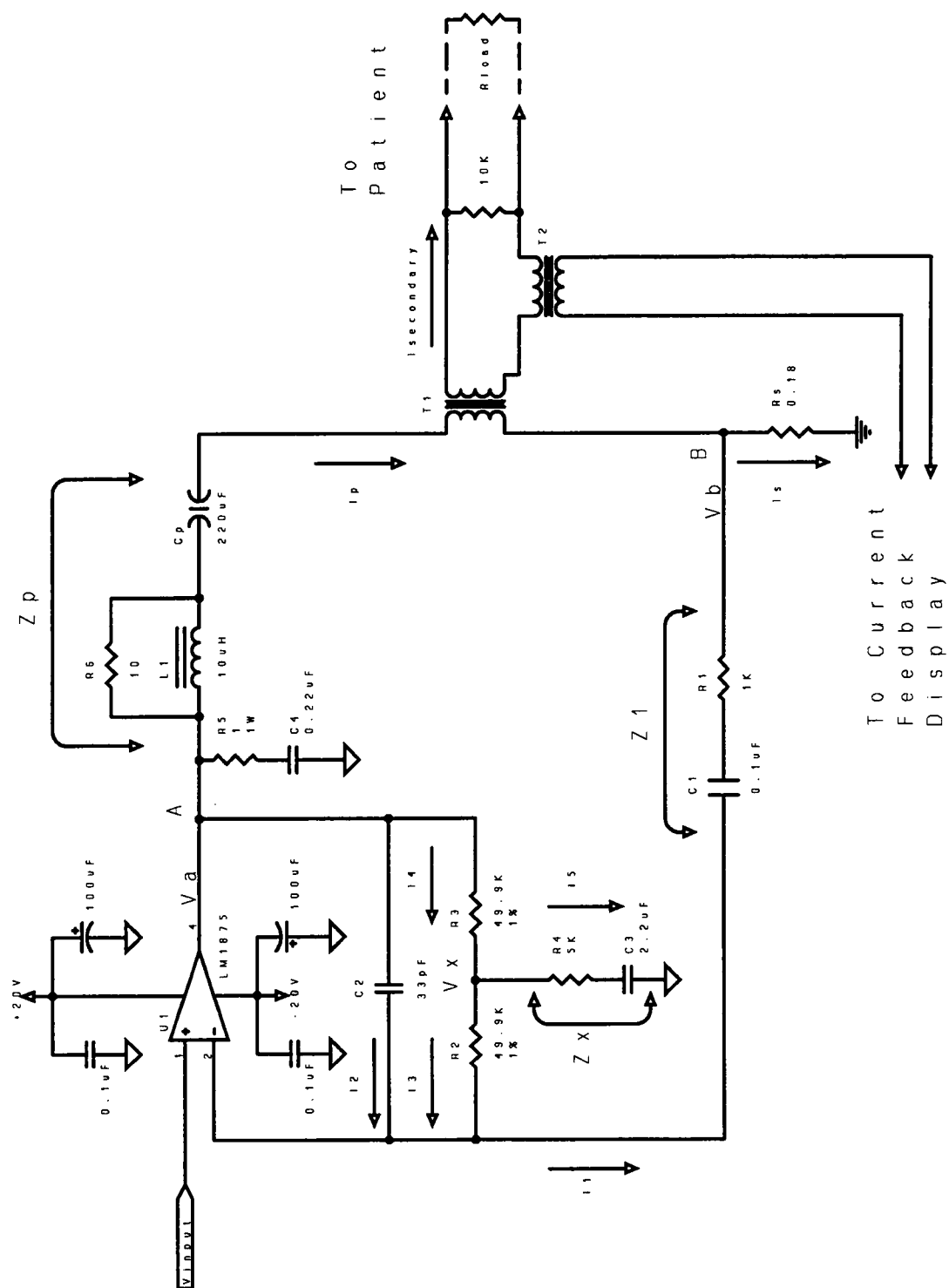


Figure 2.53. Constant current output power amplifier.

$$\frac{I_p}{V_{input}} = \frac{76375}{13500 + R_{load}} \quad \text{Eq. 2.29}$$

Using a value of 250Ω for R_{load} in equation 2.29, the midband transconductance gain is found to be

$$\left(\frac{I_p}{V_{input}} \right)_{midband} = 5.555 \frac{\text{amps}}{\text{volt}} \quad \text{Eq. 2.30}$$

The error in equation 2.27 due to the omission of the higher order terms results in an error in the derived midband gain of approximately 2%, with a calculated midband gain of 5.44 amps/volt when these terms are included.

With the midband transfer function developed, the transfer function including the effect of the reactive components in Figure 2.53 will be derived. Before developing this transfer function, some simplifying assumptions are made. The first is that the pole produced by the R_5, C_4 (723KHz) network (this network is recommended by National Semiconductor for the LM1875 amplifier) is well beyond the intended frequency range of the amplifier response and will be neglected. Second, as assumed in the development of the midband transfer function, the secondary current $I_{secondary}$ in T1 is theoretically related to the primary current I_p by the turns ratio, so if the primary current is known the secondary current can easily be found, so the transfer function I_p/V_{input} will be developed instead of $I_{secondary}/V_{input}$. The third assumption is the primary winding of T1 will be modeled as a 4Ω resistive load. Obviously this assumption will introduce errors between

the theoretical/computer analysis and the actual circuit response at very low and very high frequencies but the cause of these differences will be shown. The fourth assumption is the LM1875 power amplifier will be modeled as an ideal power op-amp with infinite gain, input resistance, and bandwidth. This assumption, like the previous, will also have to be modified to obtain agreement between experimental and computer results.

For the analytical derivation of the transfer function, refer to Figure 2.53. Since the LM1875 is assumed to be an ideal power op-amp, the voltage at its inverting input will be V_{input} . With this information I_1 is found to be

$$I_1 = \frac{V_{input} - V_b}{Z_1} \quad \text{Eq. 2.31}$$

and

$$I_2 = (V_a - V_{input}) sC_2 . \quad \text{Eq. 2.32}$$

A node equation at the LM1875 inverting input gives I_3 as

$$I_3 = I_1 - I_2 \quad \text{Eq. 2.33}$$

where substitution of equations 2.31 and 2.32 into equation 2.33 gives

$$I_3 = \frac{(V_{input} - V_b)}{Z_1} - (V_a - V_{input}) sC_2 . \quad \text{Eq. 2.34}$$

With I_3 determined the voltage V_x is given by

$$V_x = V_{input} + I_3 R_2 \quad \text{Eq. 2.35}$$

where I_3 is given by equation 2.34 so V_x can be written as

$$V_x = V_{input} + [(\frac{V_{input} - V_b}{Z_1}) - (V_a - V_{input}) sC_2] R_2 . \quad \text{Eq. 2.36}$$

To determine V_a , I_4 is required. A node equation at X gives

$$I_4 = I_3 + I_5 \quad \text{Eq. 2.37}$$

where substitution of $I_5 = V_x / Z_x$ and equation 2.34 into equation 2.35 gives

$$I_4 = [\frac{(V_{input} - V_b)}{Z_1} - (V_a - V_{input}) sC_2] + \frac{V_x}{Z_x} . \quad \text{Eq. 2.38}$$

With I_4 determined, V_a is found as

$$V_a = V_x + I_4 R_3 \quad \text{Eq. 2.39}$$

where V_x is given by equation 2.36 and I_4 is given by equation 2.38. Due to the rapidly expanding nature of the equations to this point, it was necessary to solve the remaining equations on a computer. The program Mathematica [14] was used to solve, by substitution of the numerical values shown in Figure 2.53, equation 2.39. Inspection of equations 2.36 and 2.38 show that V_a is a function of V_{input} , V_b , and V_a . This can be expressed mathematically as

$$V_a = f(V_{input}, V_b, V_a) \quad \text{Eq. 2.40}$$

V_b in Figure 2.53 is given by

$$V_b = I_s R_s \quad \text{Eq. 2.41}$$

where I_s is found from a node equation at B as

$$I_s = I_1 + I_p \quad \text{Eq. 2.42}$$

with I_1 given by equation 2.31. Substitution of equation 2.31 into equation 2.42, then equation 2.42 into 2.41 and simplifying gives V_b as

$$V_b = \frac{V_{input} \frac{R_s}{Z_1} + I_p R_s}{1 + R_s Z_1} . \quad \text{Eq. 2.43}$$

Substituting this expression for V_b into equation 2.40 allows equation 2.40 to now be written as

$$V_a = f(V_{input}, I_p, V_a) . \quad \text{Eq. 2.44}$$

Equation 2.44 can now be solved for V_a and written as

$$V_a = f(V_{input}, I_p) . \quad \text{Eq. 2.45}$$

Equation 2.45 gives the voltage at node A (LM1875 output) as a function of the input voltage V_{input} and the primary current I_p . In order to eliminate V_a , another equation for V_a must be found where V_a is also a function of V_{input} and I_p . From Figure 2.53, V_a is also equal to

$$V_a = V_b + I_p Z_p \quad \text{Eq. 2.46}$$

where Z_p is the impedance of the series network shown in Figure 2.53 and V_b is given by equation 2.43. Substituting V_b in equation 2.43 into equation 2.46 gives V_a as

$$V_a = \frac{V_{input} \frac{R_s}{Z_1} + I_p R_s}{1 + \frac{R_s}{Z_1}} + I_p Z_p \quad \text{Eq. 2.47}$$

which can be written mathematically as

$$V_a = f(V_{input}, I_p) . \quad \text{Eq. 2.48}$$

The right hand side of equation 2.48 is equal to the right hand side of equation 2.45 so equating the two terms gives

$$f(V_{input}, I_p) = f(V_{input}, I_p) \quad \text{Eq. 2.49}$$

where the left and right sides of equation 2.49 are different expressions. Referring to Figure 2.53, Z_1 , Z_x , and Z_p are given by

$$Z_1 = R_1 + \frac{1}{sC_1} , \quad \text{Eq. 2.50}$$

$$Z_x = R_4 + \frac{1}{sC_3} , \quad \text{Eq. 2.51}$$

and

$$Z_p = \frac{sL_1R_6}{sL_1+R_6} + \frac{1}{sC_p} + R_p , \quad \text{Eq. 2.52}$$

where $R_p = 4\Omega$ in equation 2.52 is used as the model for T1's primary winding impedance. Substituting the values given by equations 2.50 through 2.52 into equation 2.49 and solving for I_p/V_{input} gives the required transfer function as a function of the laplace variable s . This transfer function is written as a ratio of two polynomials in s as

$$\frac{I_p}{V_{\text{input}}}(s) = \frac{N(s)}{D(s)} \quad \text{Eq. 2.53}$$

where

$$N(s) = a_7s^7 + a_6s^6 + a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0 \quad \text{Eq. 2.54}$$

and

$$D(s) = b_7s^7 + b_6s^6 + b_5s^5 + b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0 . \quad \text{Eq. 2.55}$$

The coefficients a_i and b_i of the numerator and denominator polynomials respectively are given in Table 2.2. The Bode plot of equation 2.53 as a function of frequency (hertz) is shown in figures 2.54 and 2.55.

Table 2.2
Transfer Function Coefficients

i	a_i	b_i
0	0	1.47125x10²⁷
1	3.236567x10²³	1.79845x10²⁵
2	4.24999x10²²	2.1186x10²²
3	2.26147x10²⁰	4.40122x10¹⁹
4	4.41842x10¹⁶	8.31479x10¹⁵
5	2.22189x10¹²	4.18194x10¹¹
6	2.24844x10⁶	760212
7	0.0705092	1

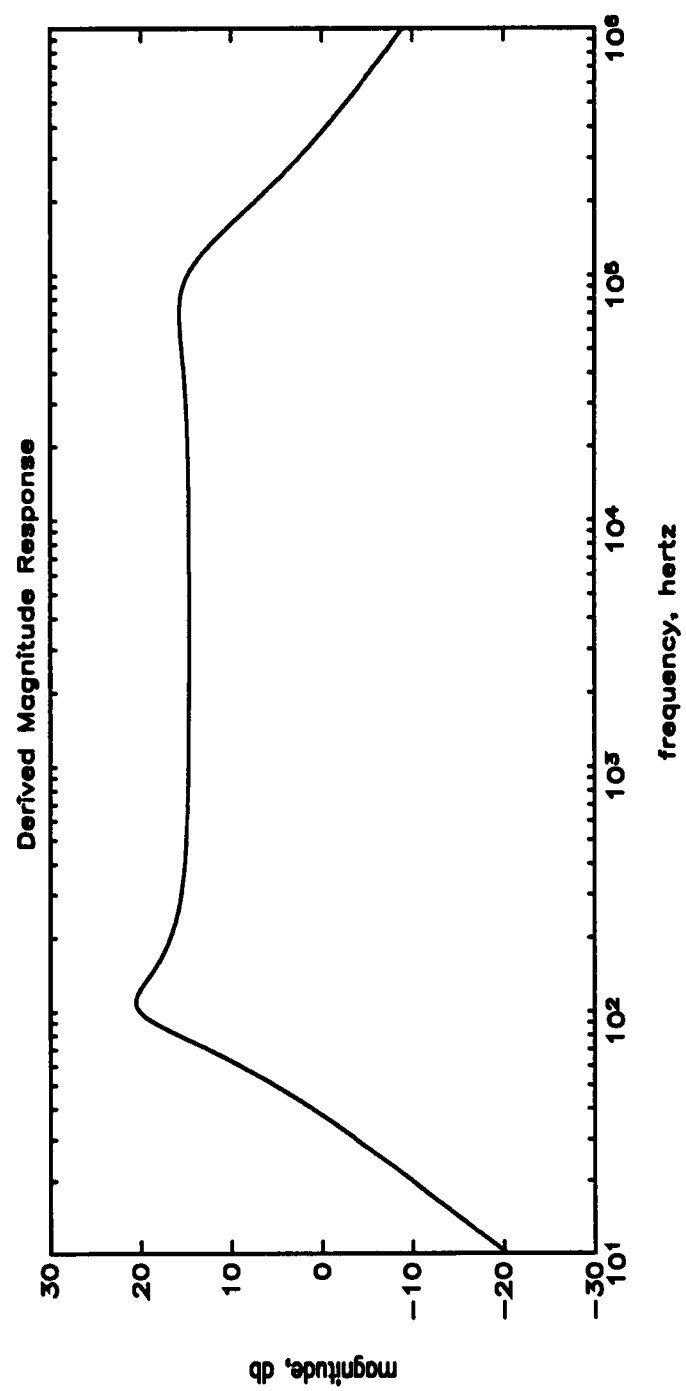


Figure 2.54. Derived magnitude response.

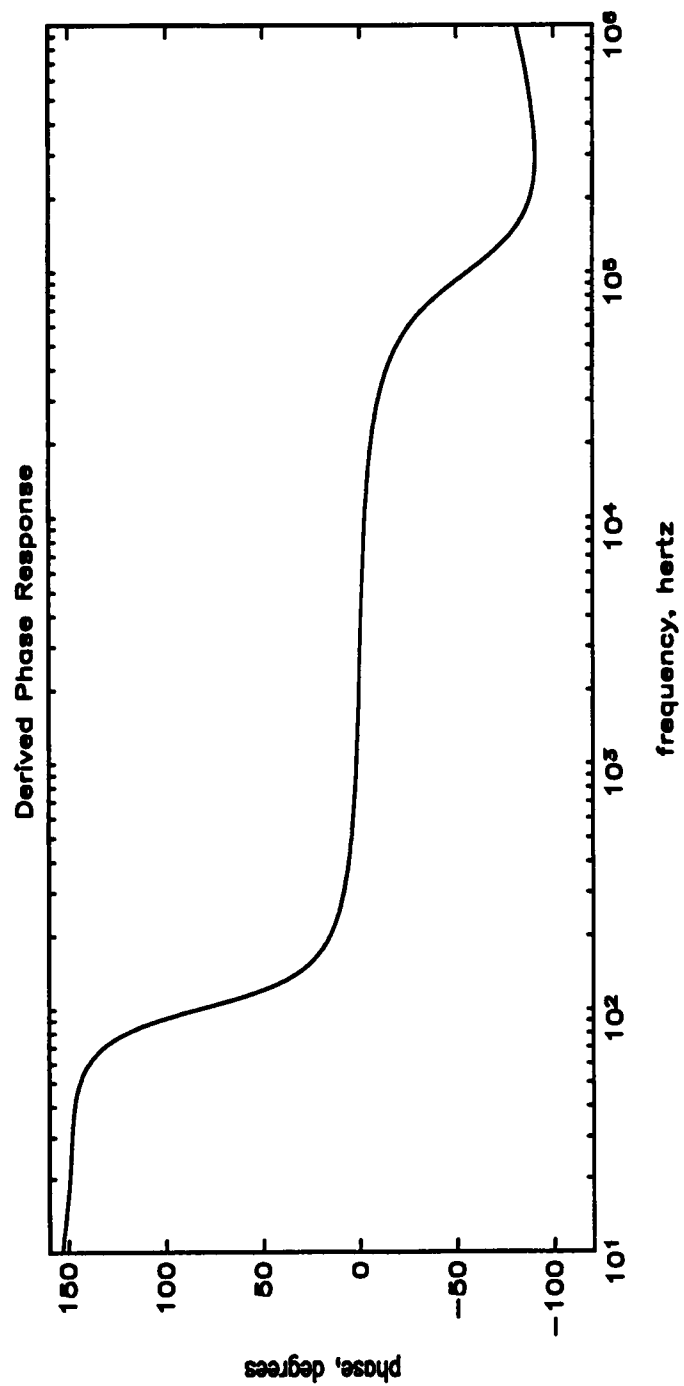


Figure 2.55. Derived phase response.

The midband gain in Figure 2.54 was measured as 14.71db during simulation which corresponds to a gain of 5.44 amps/volt. This is in good agreement with equation 2.27 which implies an accurate derivation of equation 2.27.

In order to verify the accuracy of this analysis, the circuit shown in Figure 2.56 was simulated using PSPICE. This is the same circuit as Figure 2.53 with the amplifier modeled as a voltage-controlled voltage-source and the primary impedance of the transformer modeled as a 4Ω resistance. The PSPICE source file used to simulate the circuit shown in Figure 2.56 is given in Appendix A. The 0A current sources I1 and I2 in Figure 2.56 are included to prevent the inverting and noninverting inputs of the amplifier model from floating with respect to ground because PSPICE requires that all nodes in a circuit have a dc path to ground. These sources provide this path through the infinite output resistance of the respective current source.

The resulting Bode plot for this simulation is shown in Figures 2.57 and 2.58. Comparing figures 2.57 and 2.58 with figures 2.54 and 2.55 it can be seen that the magnitude and phase curves are identical which implies an accurate derivation of the transfer function.

Although the derived and simulated bode plots show good agreement, actual circuit performance had to be verified by constructing and testing a prototype. The circuit shown in Figure 2.53 was built on a single-sided printed circuit board (a suggested pcb layout is given in Appendix B) and the frequency response determined experimentally. A test voltage was applied to the amplifier noninverting input and the current in T1's primary was measured with a current probe. The secondary of T1 was connected to a

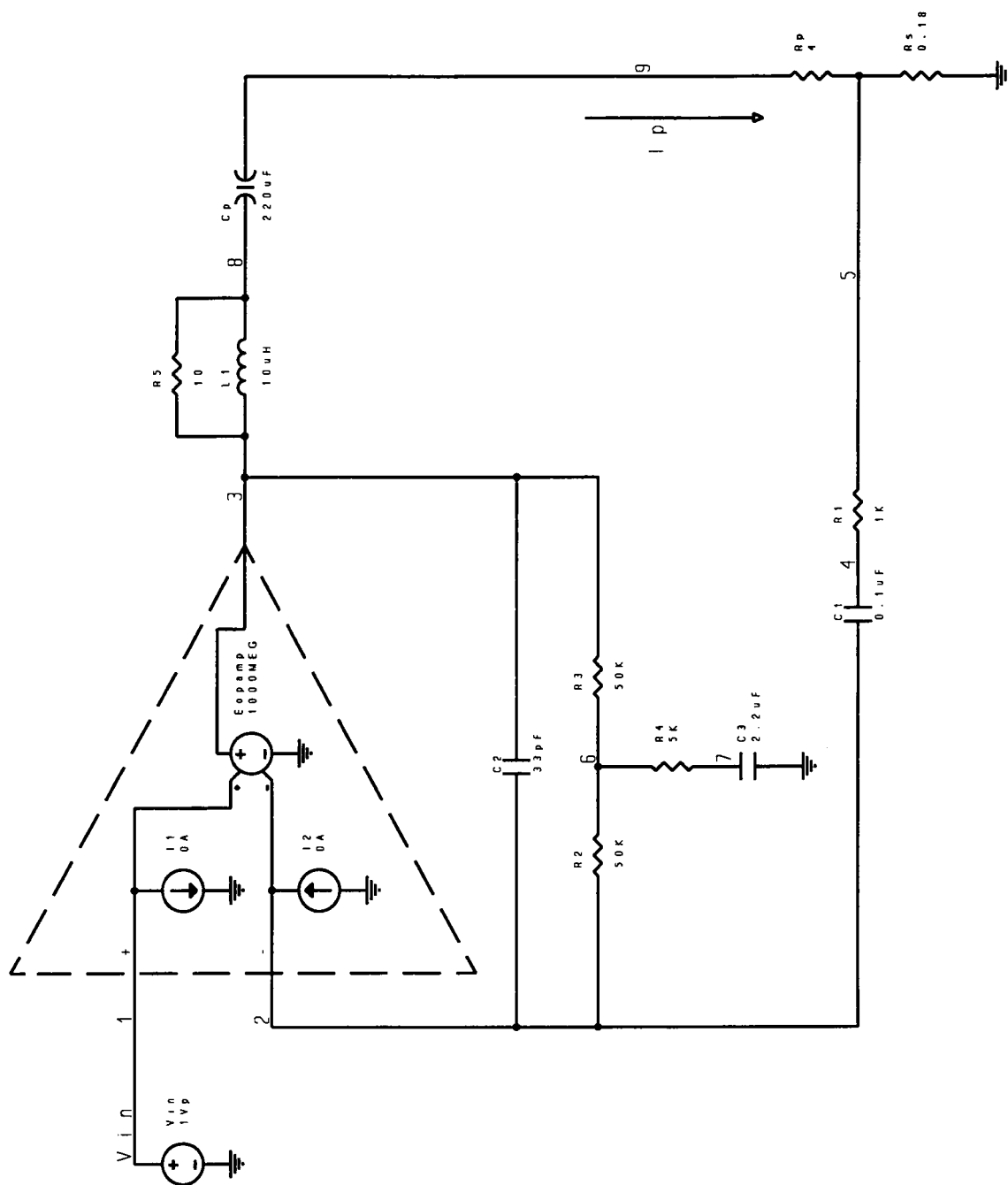


Figure 2.56. PSPICE circuit used to simulate Figure 2.53.

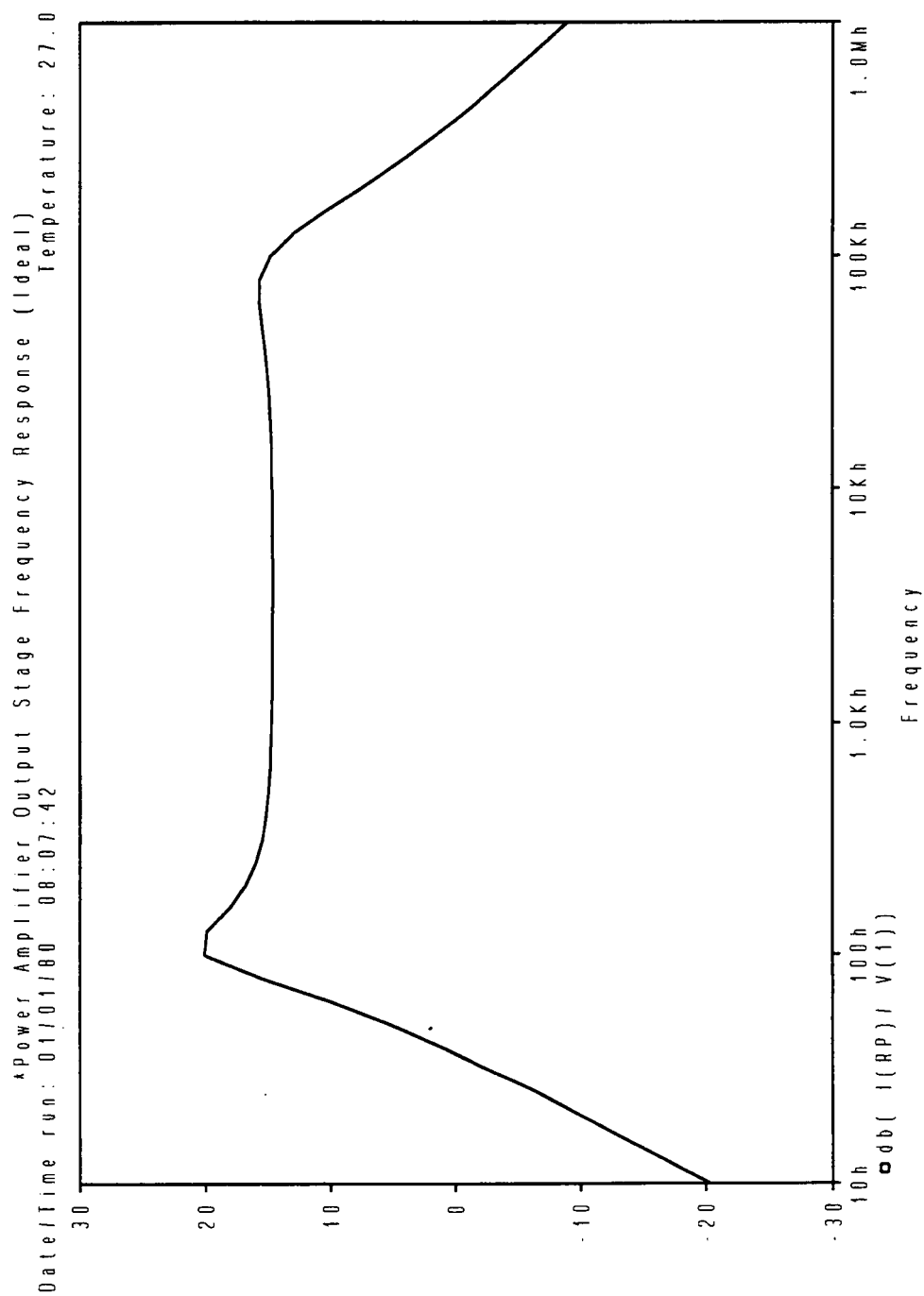


Figure 2.57. PSPICE simulated magnitude response.

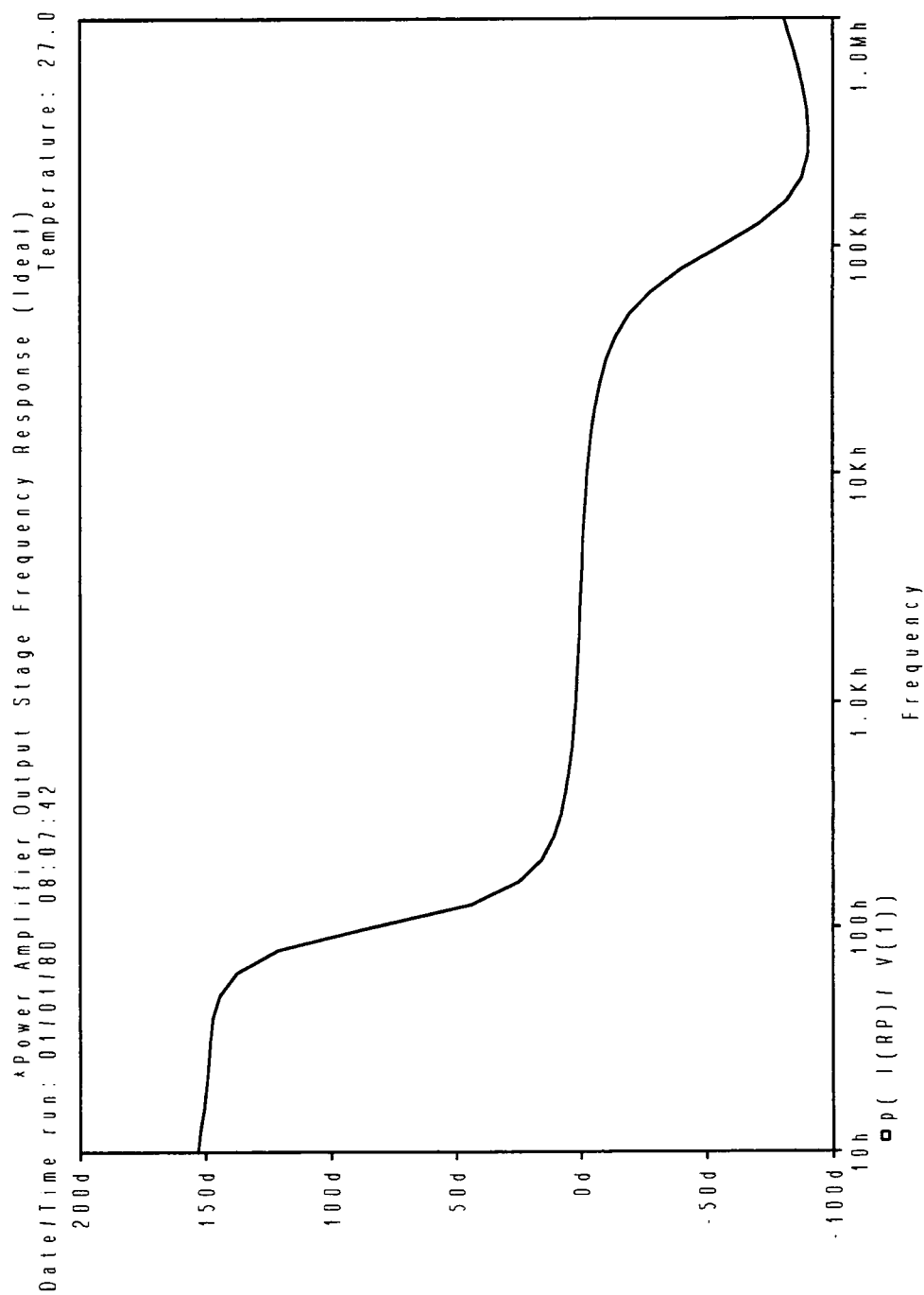


Figure 2.58. PSPICE simulated phase response.

250 Ω resistive load during this test to simulate an actual patient load. Table C.1 in Appendix C shows the data acquired from this experiment. It should be noted that the phase of T1's primary current I_p was measured relative to the positive slope zero crossing of the input test voltage. A bode plot of the data given in Table C.1 is shown in Figures 2.59 and 2.60. The magnitude response shown in Figure 2.59 was derived using $db = 20 \log_{10}(I_p/V_{input})$ where $V_{input} = 0.1V_{peak}$.

Comparing figures 2.59 and 2.60 with figures 2.57 and 2.58 shows reasonably close agreement with the exception of the peaking at approximately 53KHz in Figure 2.59 and the slope of the high frequency roll off. This discrepancy between experimental and simulated response curves is caused by two of the four simplifying assumptions made when the PSPICE model was formulated. The first error was the assumption of an infinite gain bandwidth product for the LM1875 power amplifier and the second was the assumption that the primary of the transformer (T1 in Figure 2.53) was purely resistive.

To correct the error in the model of the transformer, a bode plot for the transformer was required. To accurately model the effect of parasitics contributed by the interconnecting wiring harness, the transformer bode plot was determined with the interconnecting wiring connected as it would be in the finished instrument. With the secondary loaded with a 250 Ω resistor, a voltage was applied to the primary and the voltage and current (plus phase between the voltage and current) was measured. The curves generated by this experiment are shown in Figures 2.61 and 2.62. Figure 2.61 reveals that the transformer primary impedance is approximately 4.9 Ω below 10KHz and becomes inductive above 10KHz. Figure 2.62 reveals the phase angle of this impedance

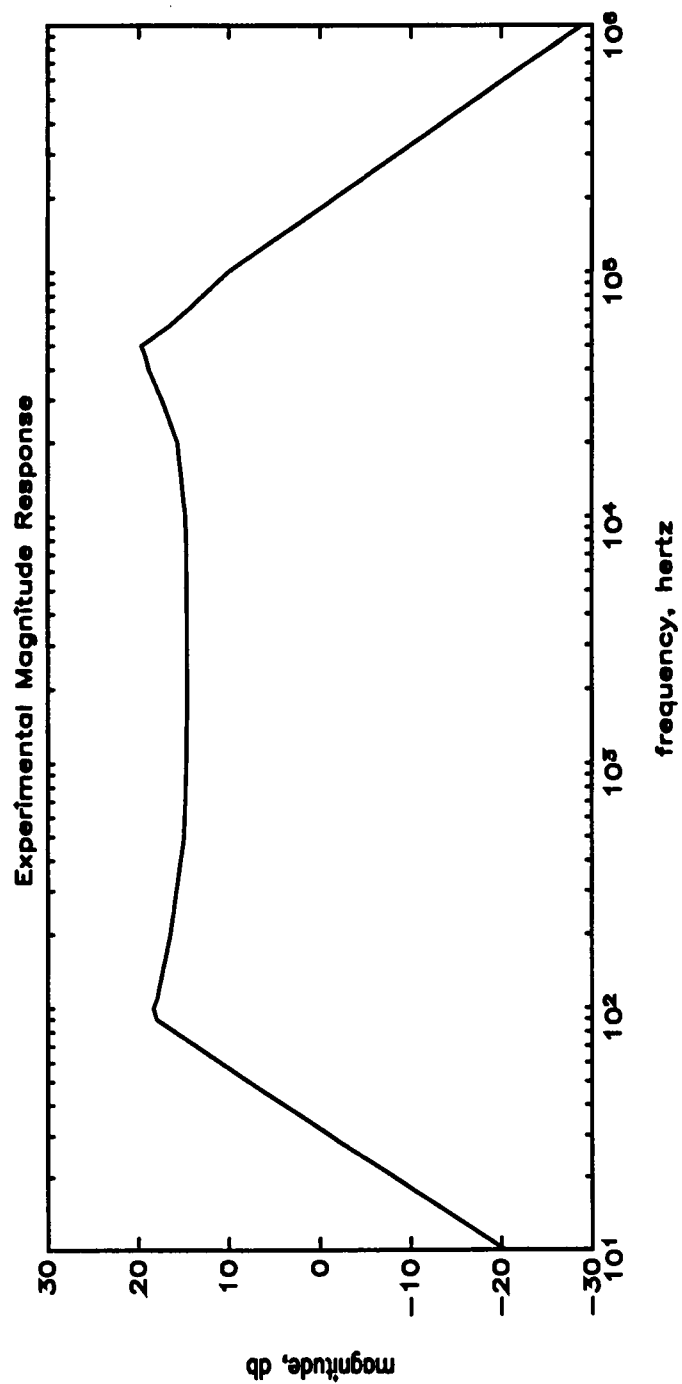


Figure 2.59. Experimental magnitude response.

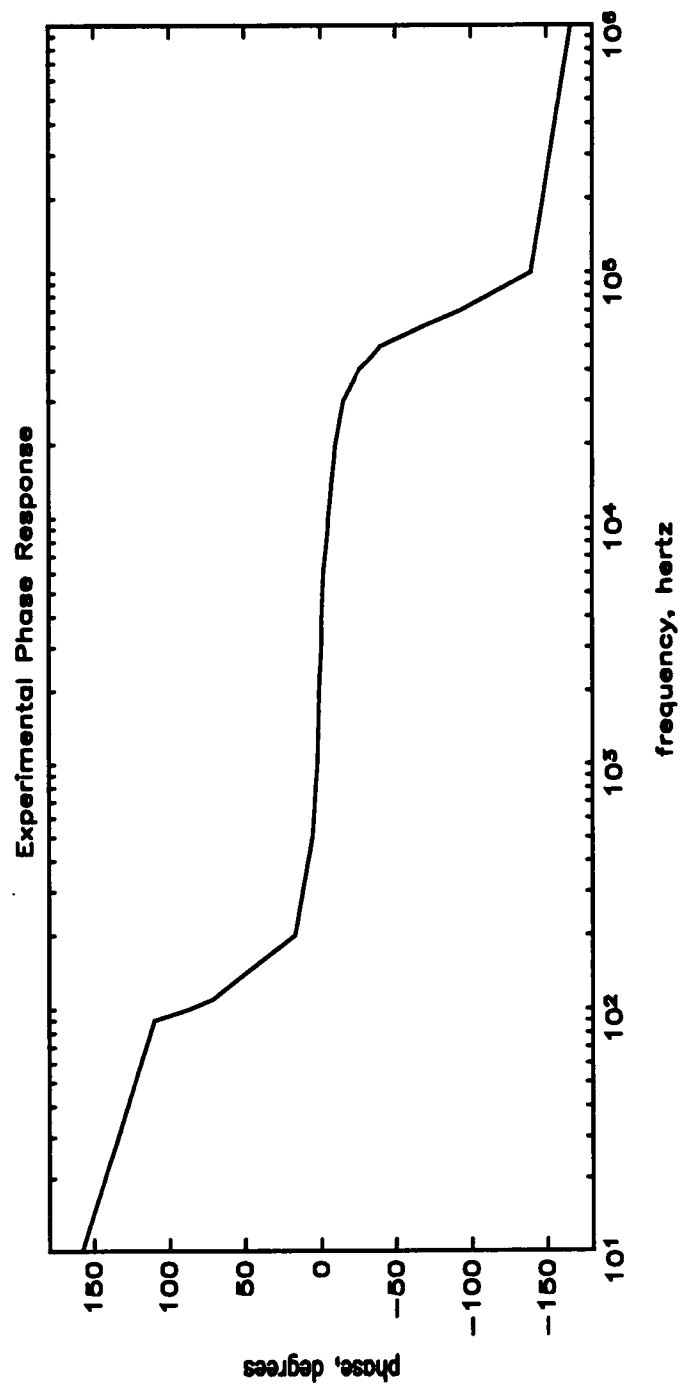


Figure 2.60. Experimental phase response.

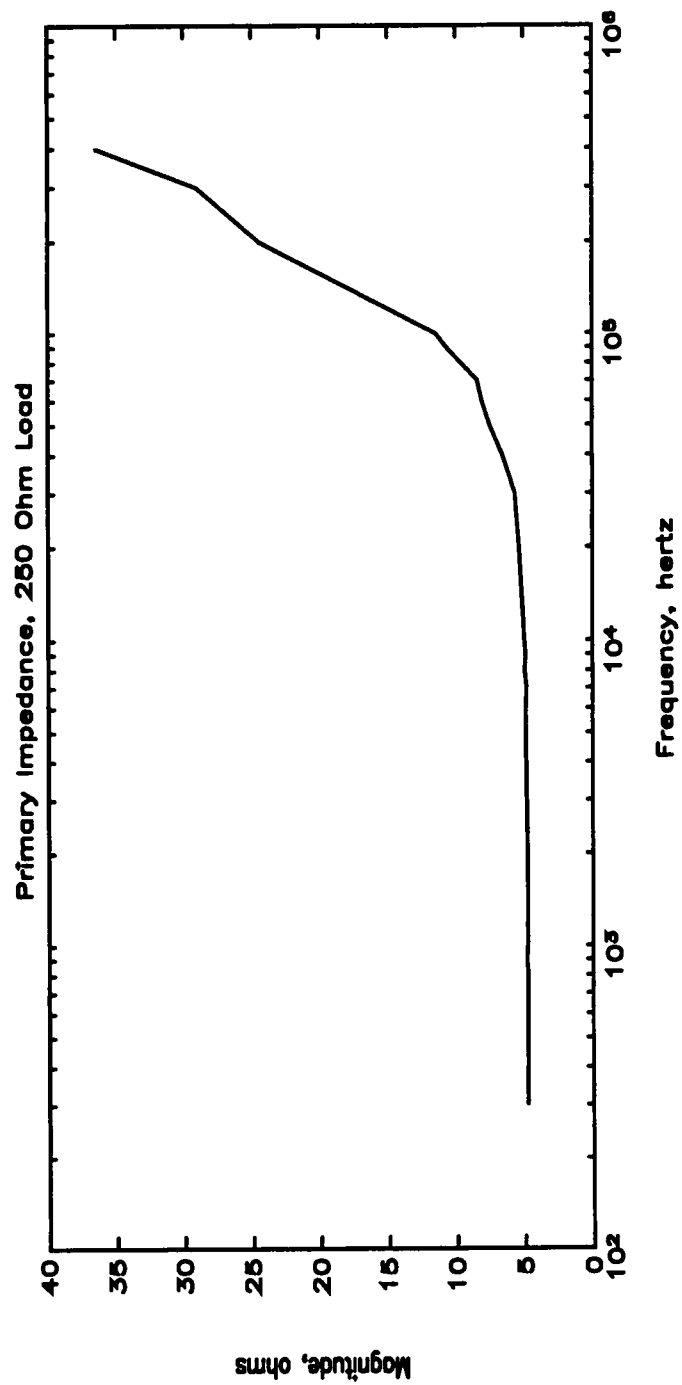


Figure 2.61. Transformer primary impedance.

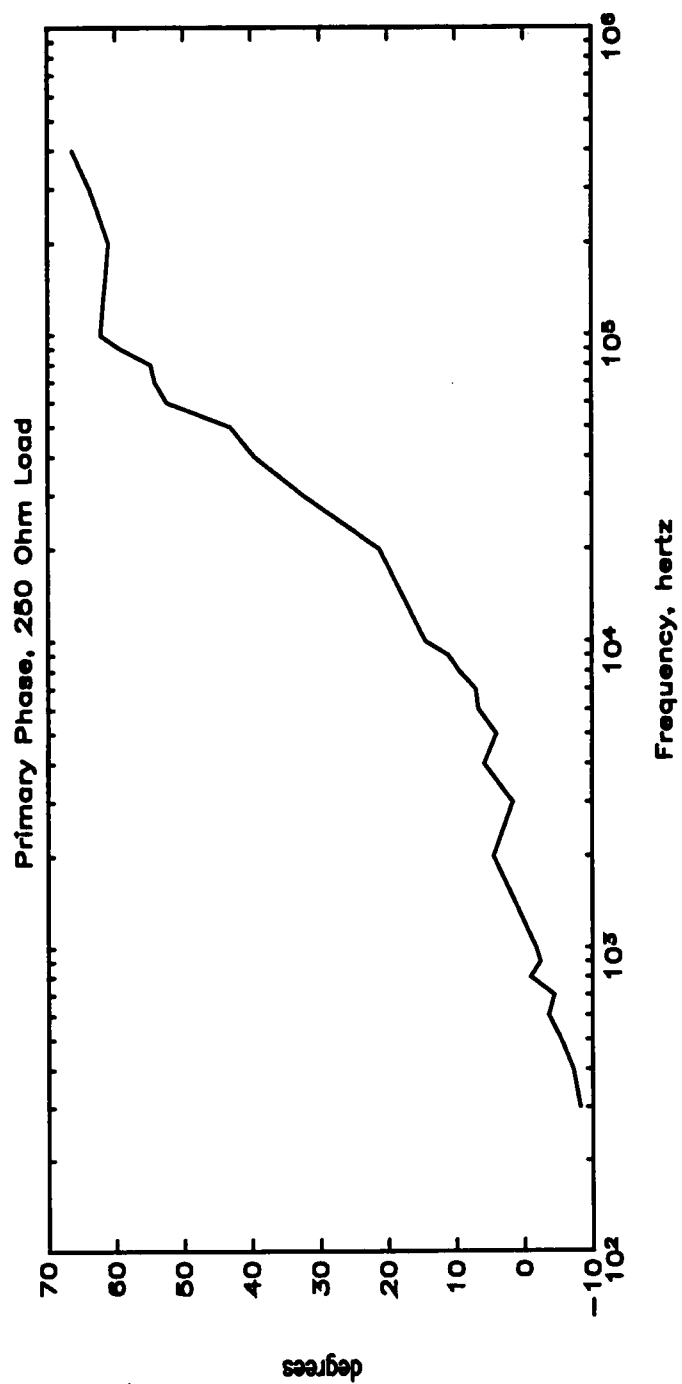


Figure 2.62. Transformer primary phase.

starts at a value close to zero and approaches 90° at high frequencies. This suggests that the primary should be modeled as a single-pole series RL circuit whose impedance increases as the frequency increases and whose phase angle approaches 90° . The value of this inductor can be determined from Figure 2.61 to be approximately $17.34\mu\text{H}$. The 4Ω resistor in Figure 2.56 can now be replaced with a 4.9Ω resistor in series with an $17.34\mu\text{H}$ inductor.

Comparing figures 2.57 and 2.59 it can be seen that the actual circuit response rolls off at 40db per decade in the high frequency region whereas the simulated response rolls off at 20db per decade. This means the prototype has an additional pole that is not accounted for in Figure 2.56. This additional pole is due to the pole in the LM1875 open loop gain response and was not included in the model of Figure 2.56. To include this pole, the gain bandwidth product of the LM1875 is required. The data sheet [15] for the LM1875 gives the gain bandwidth as 5.5MHz and a typical dc open loop gain of 90db. 90db corresponds to a gain of 31623 so the open loop pole is found as

$$f_0 = \frac{5.5 \times 10^6 \text{Hz}}{31623} = 174 \text{Hz} . \quad \text{Eq. 2.56}$$

The open loop gain of the LM1875 amplifier can now be modeled as shown in Figure 2.63 where the open loop pole is modeled by an RC network. Assuming $R = 10\text{K}\Omega$, the capacitance required is $C = 91.5\text{nF}$ which places the open loop pole at 174Hz. The typical input resistance of $50\text{K}\Omega$ has also been included between the inverting and noninverting inputs to more accurately model the actual characteristics of the LM1875.

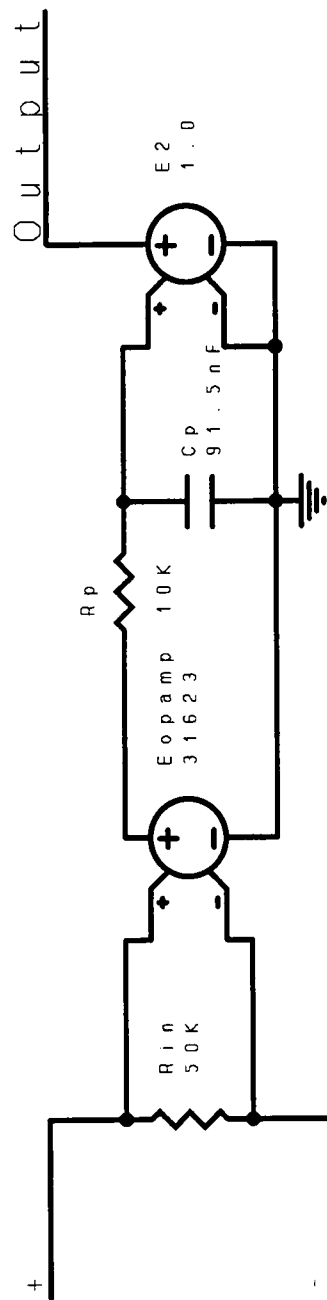


Figure 2.63. Single-pole LM1875 open loop model.

Substituting the amplifier model in Figure 2.63 into Figure 2.56 and replacing the 4Ω resistor in Figure 2.56 with a 4.9Ω resistor in series with an $17.34\mu\text{H}$ inductor and resimulating gives the bode plot shown in figures 2.64 and 2.65. Comparing figures 2.59 and 2.60 with figures 2.64 and 2.65 shows good agreement which implies the 2nd order model is a reasonably accurate representation of the actual circuit. The response of the amplifier over the frequency range the circuit will operate (2.3KHz to 5.0KHz) is flat which is required to maintain a constant amplitude current signal.

In order to understand the effect on the frequency response due to each reactive element present in the second order model, multiple PSPICE simulations were ran starting with all reactive elements removed ($C1 = C3 = C_p = \infty$, $C2 = 0$, $L1 = \infty$, and $L_p = 0$ in Figure 2.66) and inserting each component in turn to observe its contribution to the overall response. The model used for this simulation is the second order model used to generate Figures 2.64 and 2.65 and is shown in Figure 2.66. As can be seen from Figure 2.66, the model includes the single pole response of the LM1875 amplifier and the primary inductance of the output transformer.

Figures 2.67 through 2.77 show the magnitude response (upper trace is voltage response, lower trace is current response in each figure) of the circuit in Figure 2.66 starting with all reactive components removed as shown in Figure 2.67 then successively inserting the various capacitors and inductors until the complete response is obtained as shown in Figure 2.77. The single pole amplifier model is used in all these figures and it should also be noted that the range of the frequency axis has been modified to show the low frequency behavior of the circuit.

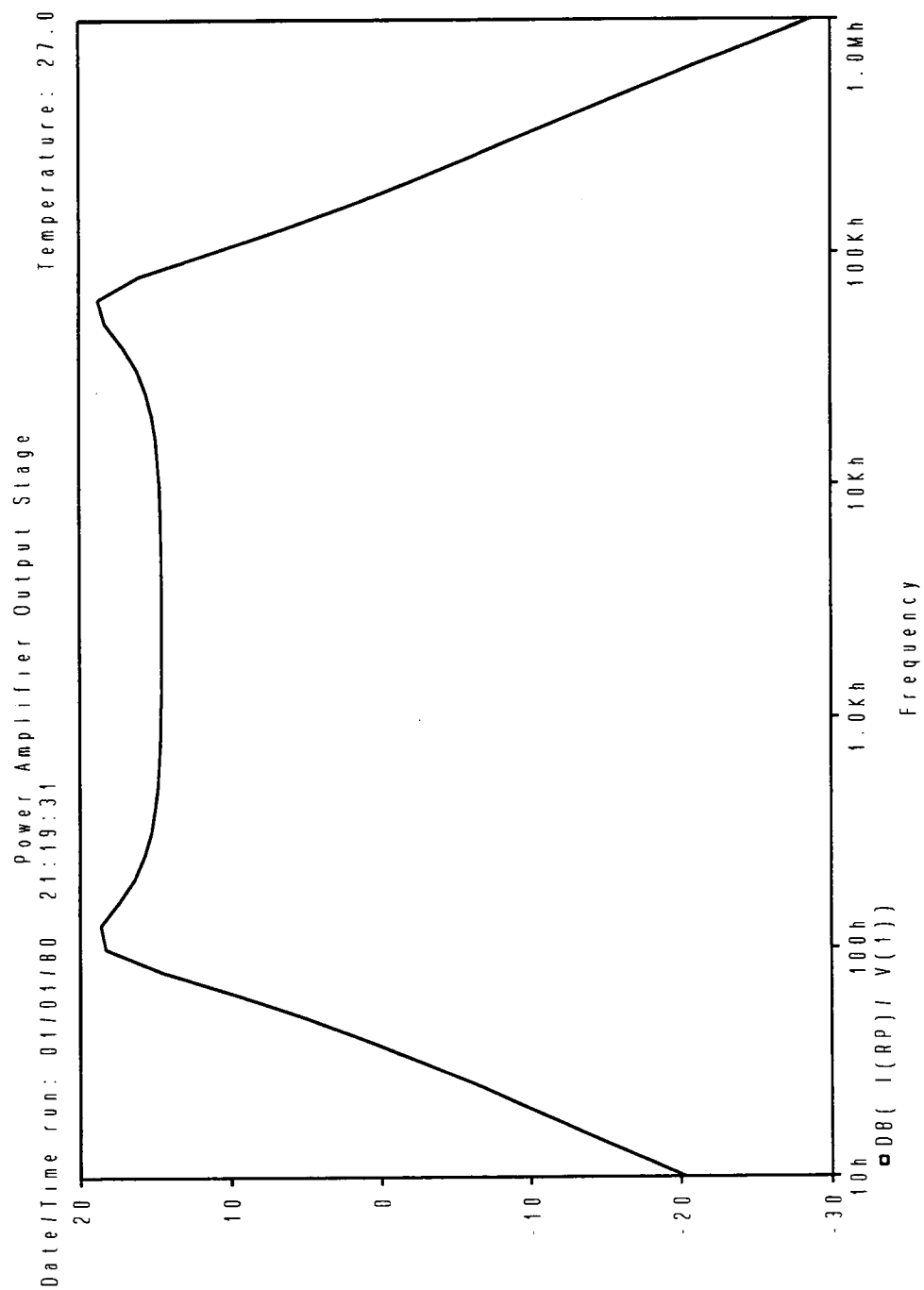


Figure 2.64. Magnitude response, 2nd order.

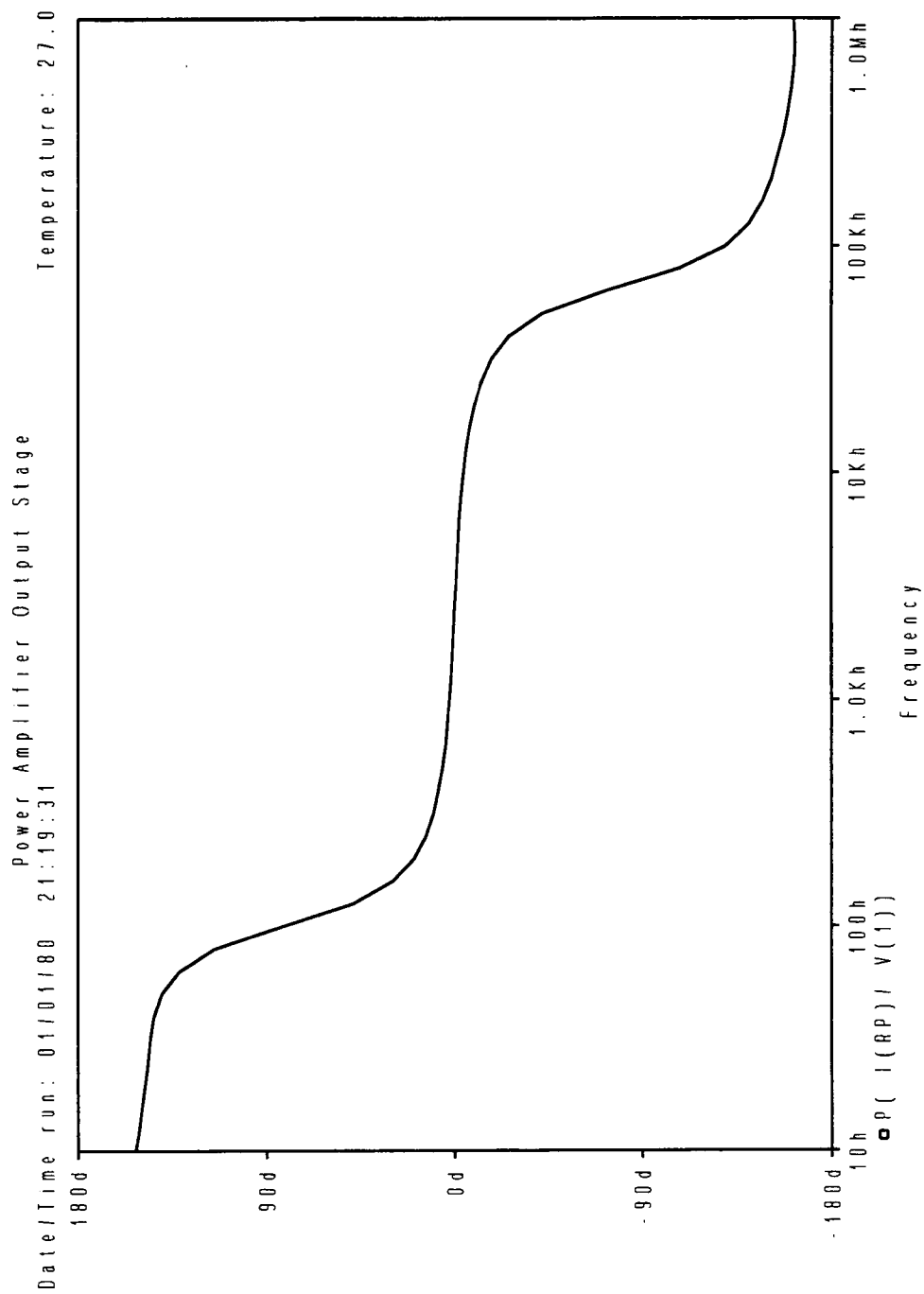


Figure 2.65. Phase response, 2nd order.

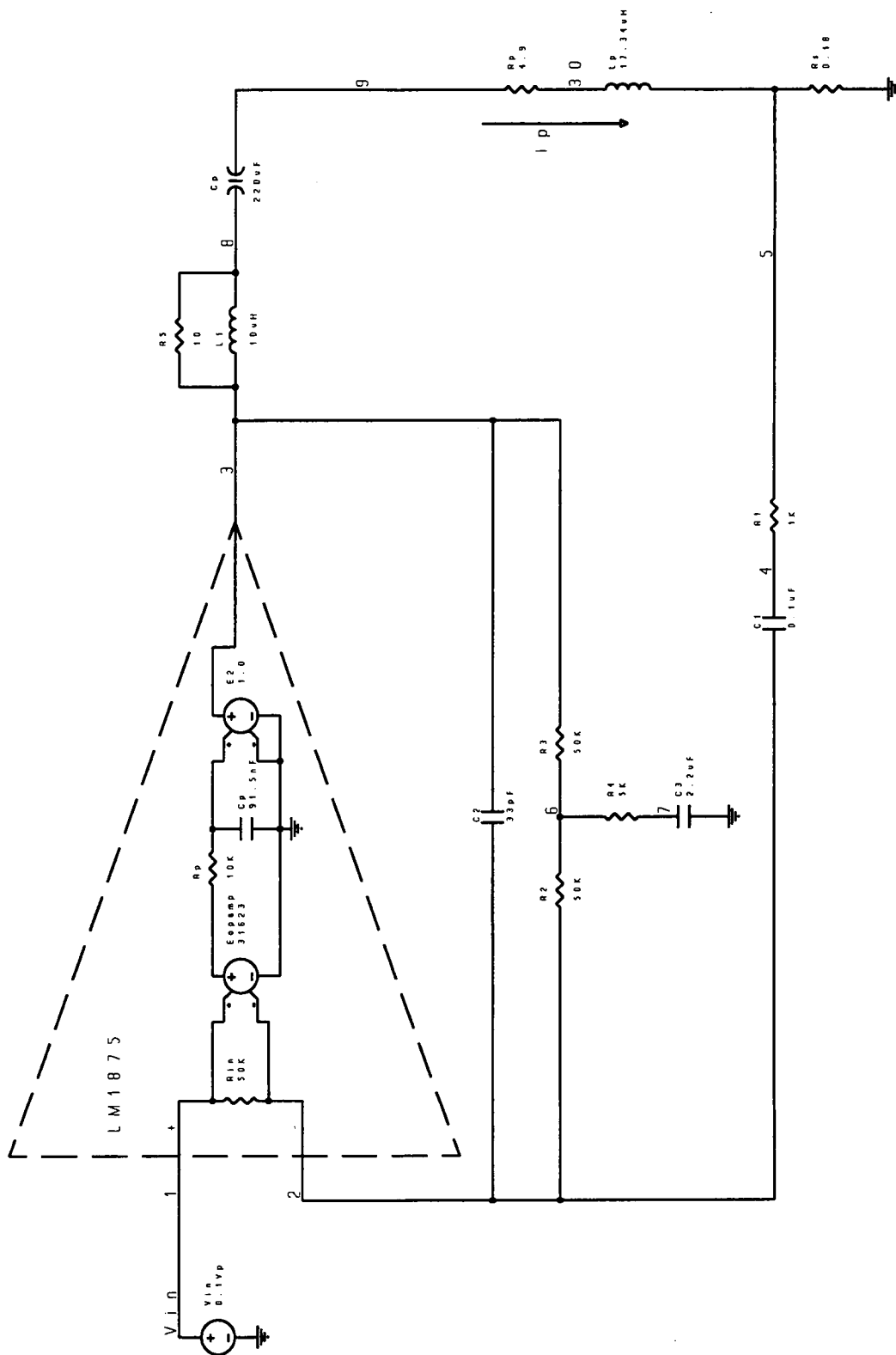


Figure 2.66. Second order amplifier model.

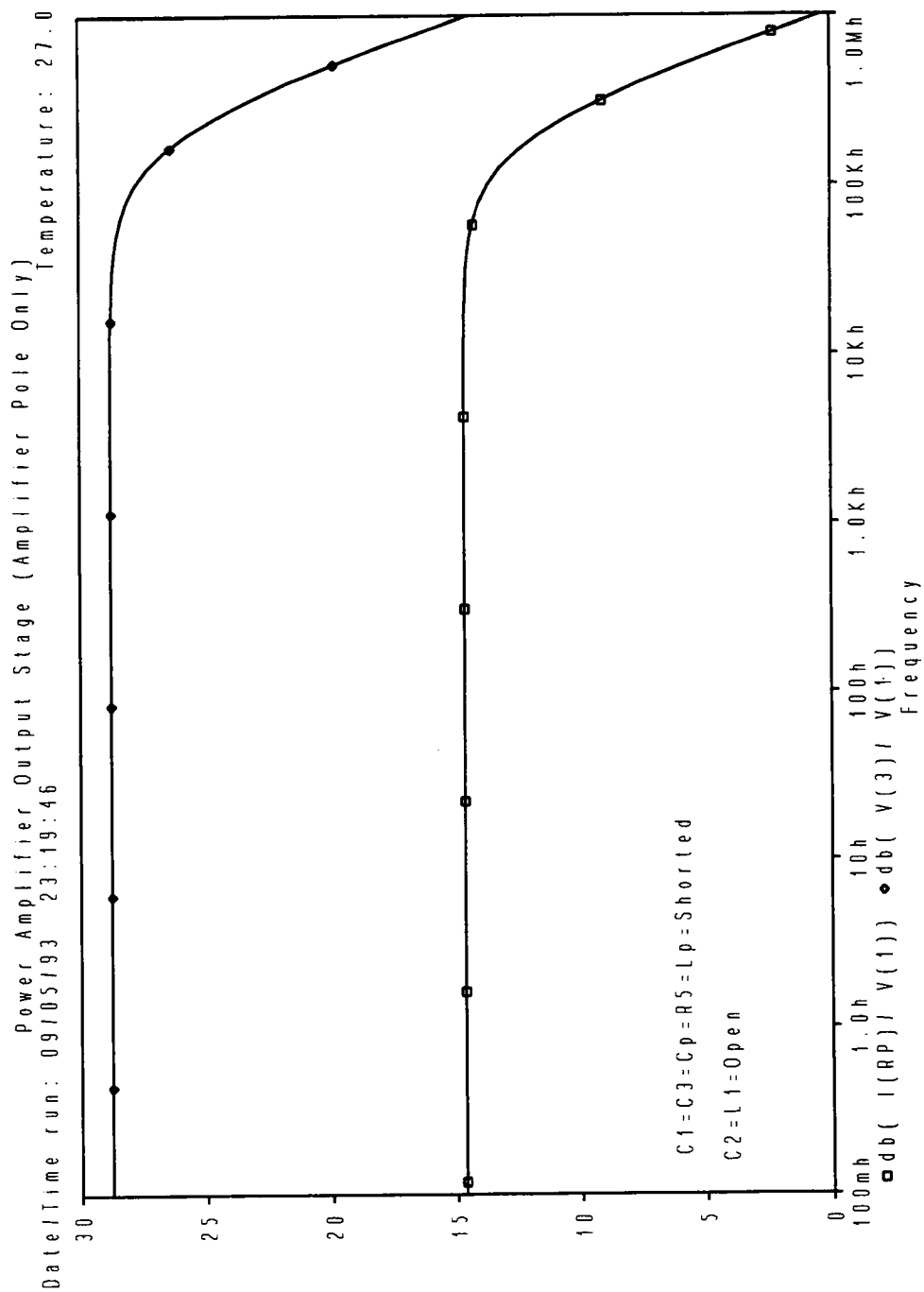


Figure 2.67. Magnitude response, amplifier pole only.

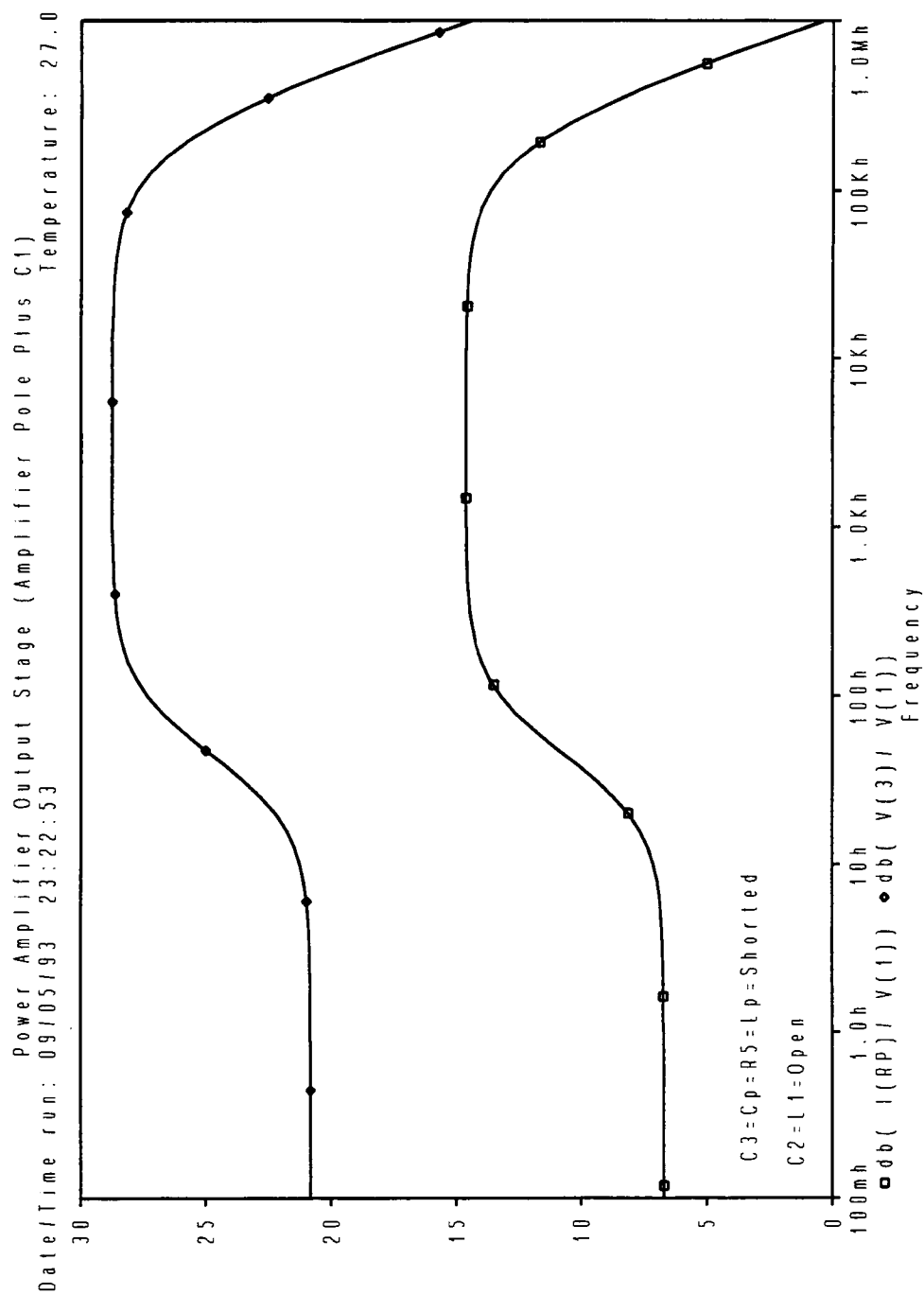


Figure 2.68. Magnitude response, C1 only.

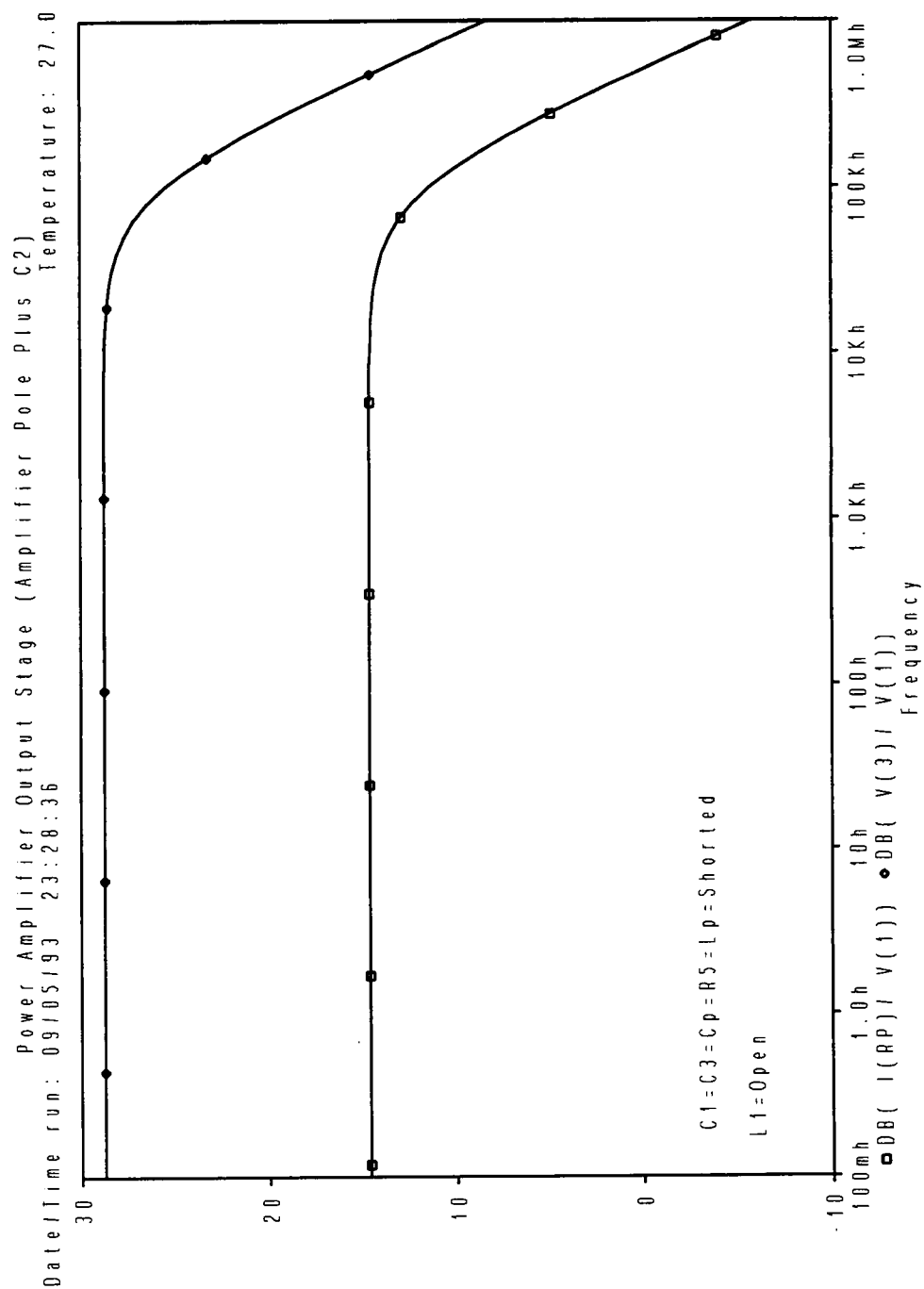


Figure 2.69. Magnitude response, C2 only.

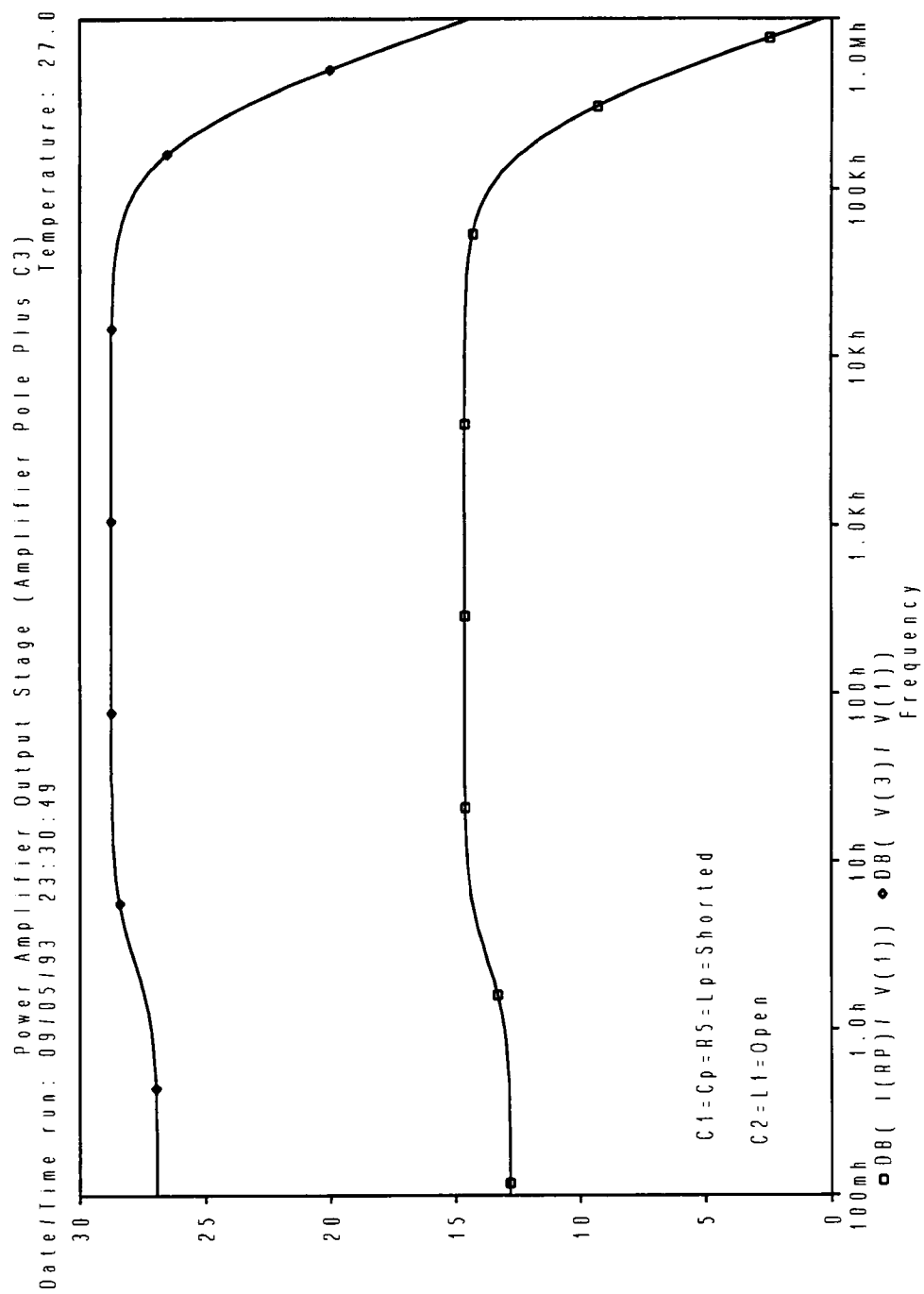


Figure 2.70. Magnitude response, C3 only.

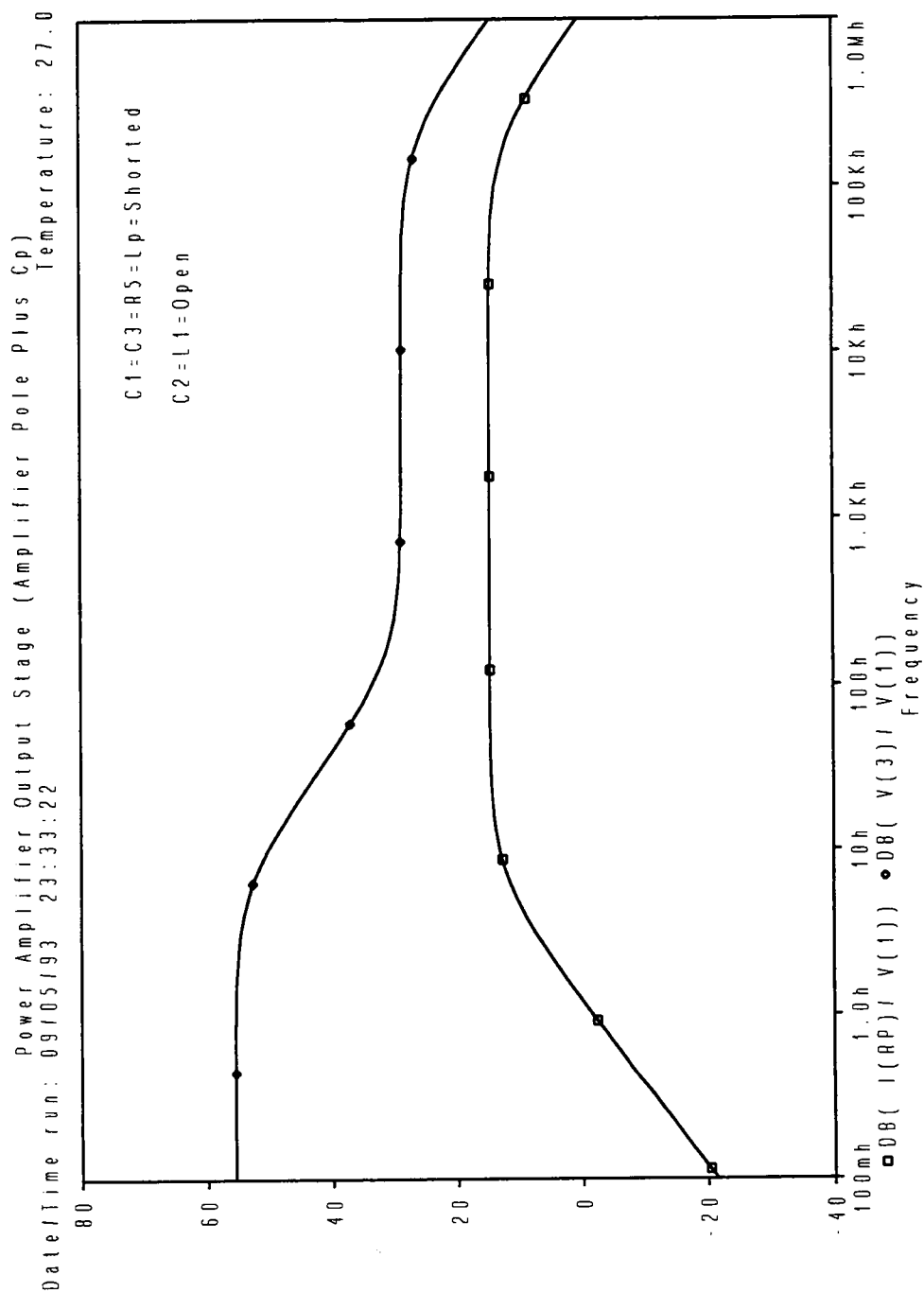


Figure 2.71. Magnitude response, Cp only.

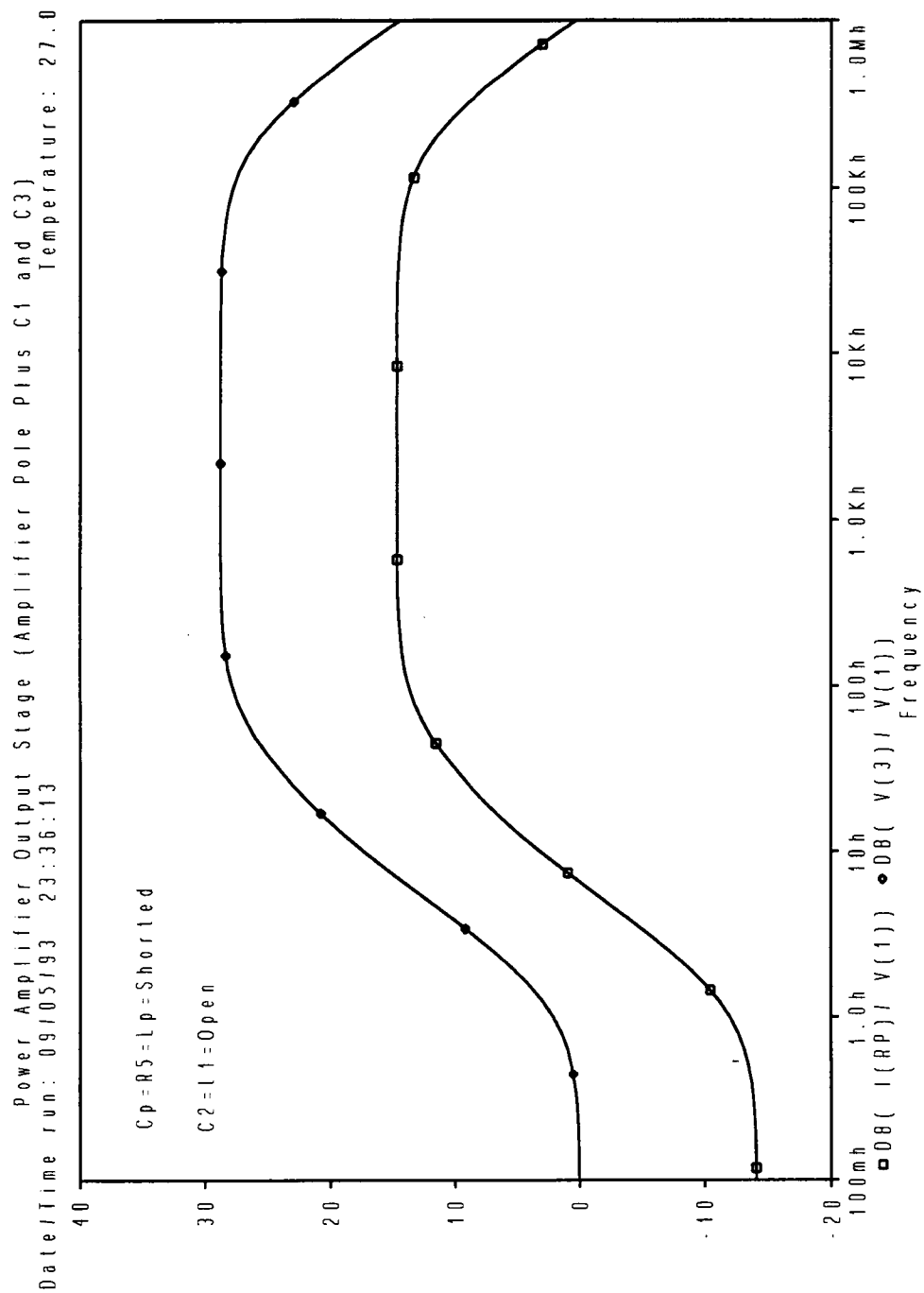


Figure 2.72. Magnitude response, C1 and C3.

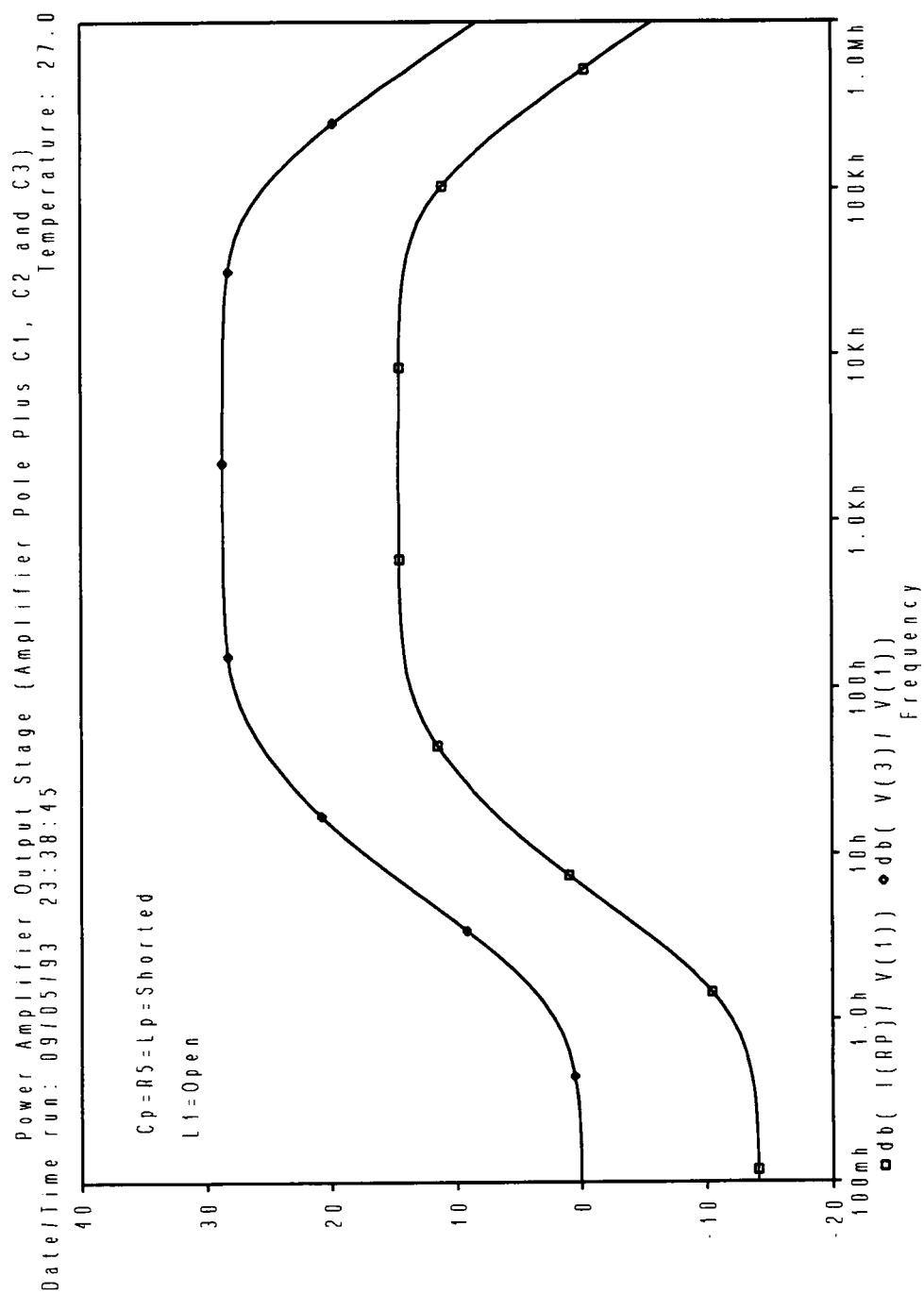


Figure 2.73. Magnitude response, C1, C2, and C3.

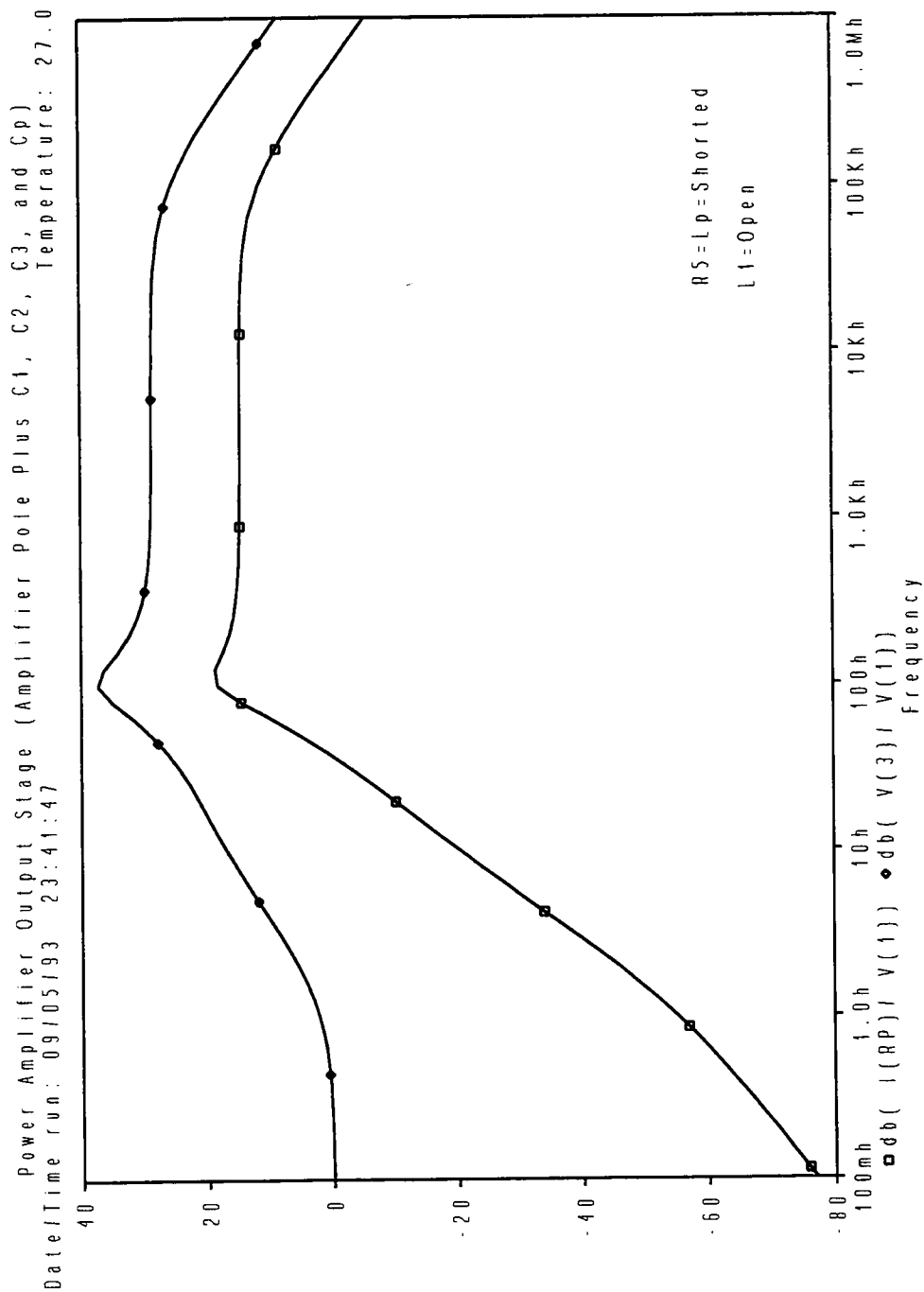


Figure 2.74. Magnitude response, C1, C2, C3, and Cp.

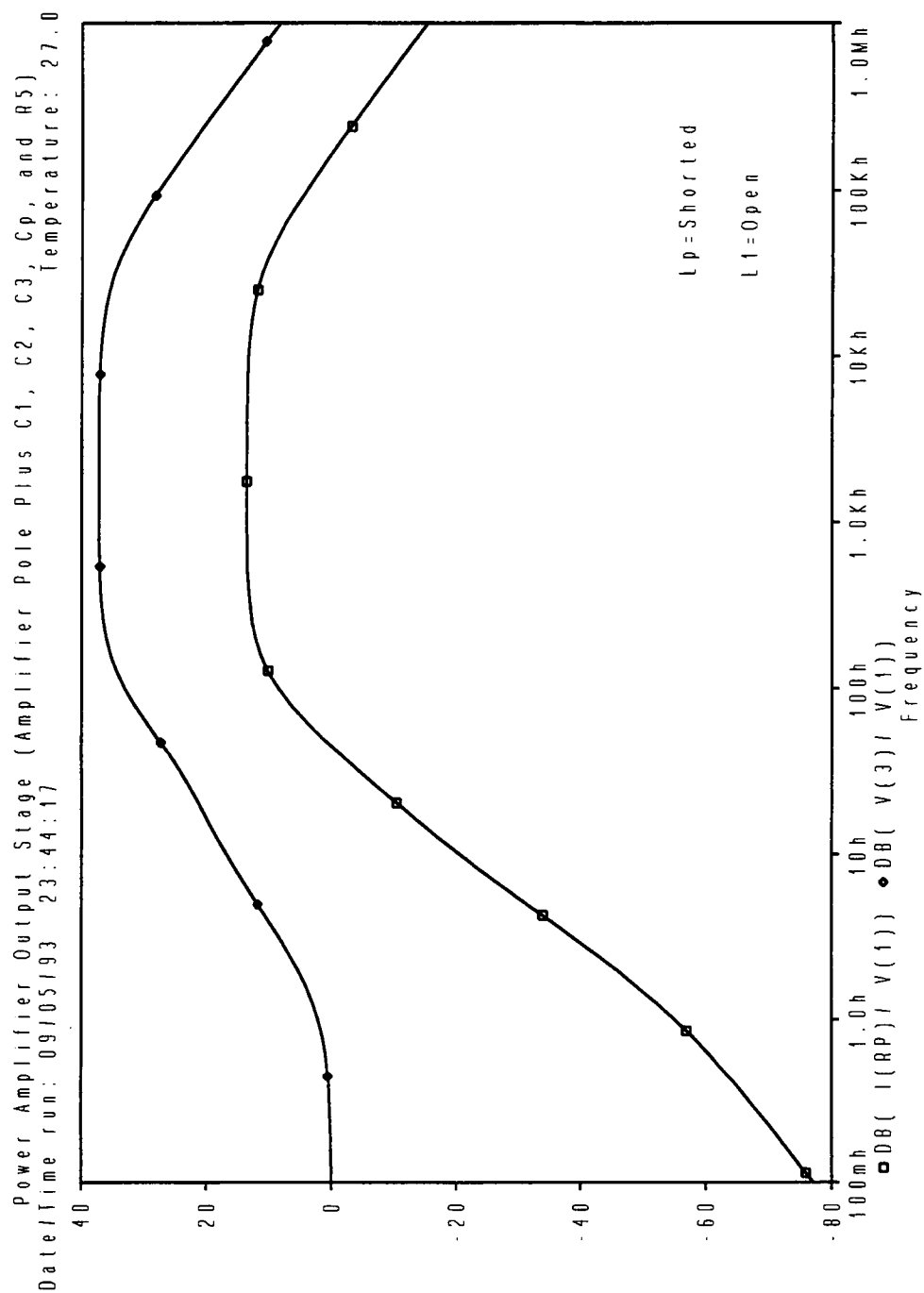


Figure 2.75. Magnitude response, C1, C2, C3, Cp, and R5.

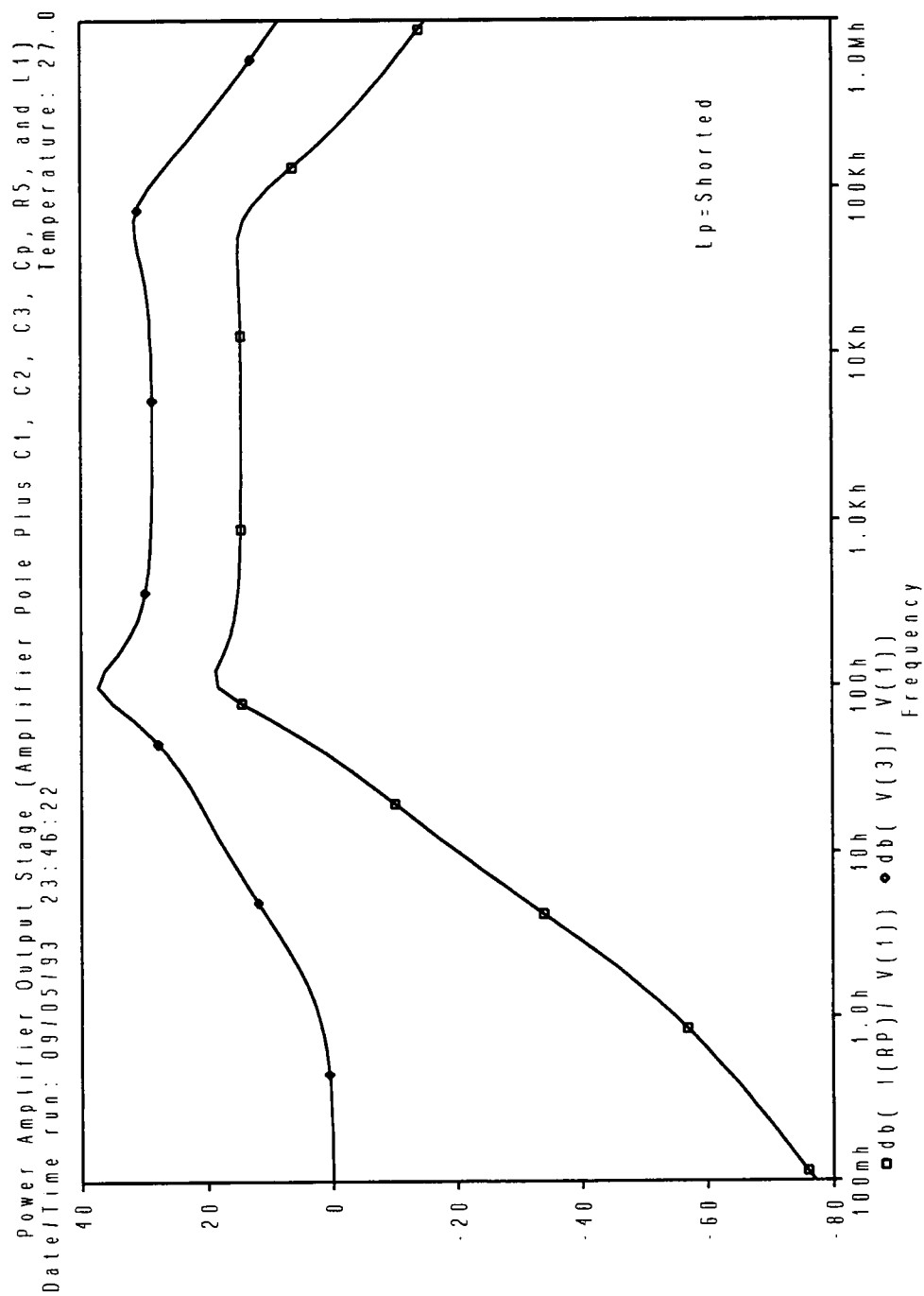


Figure 2.76. Magnitude response, C1, C2, C3, Cp, R5, and L1.

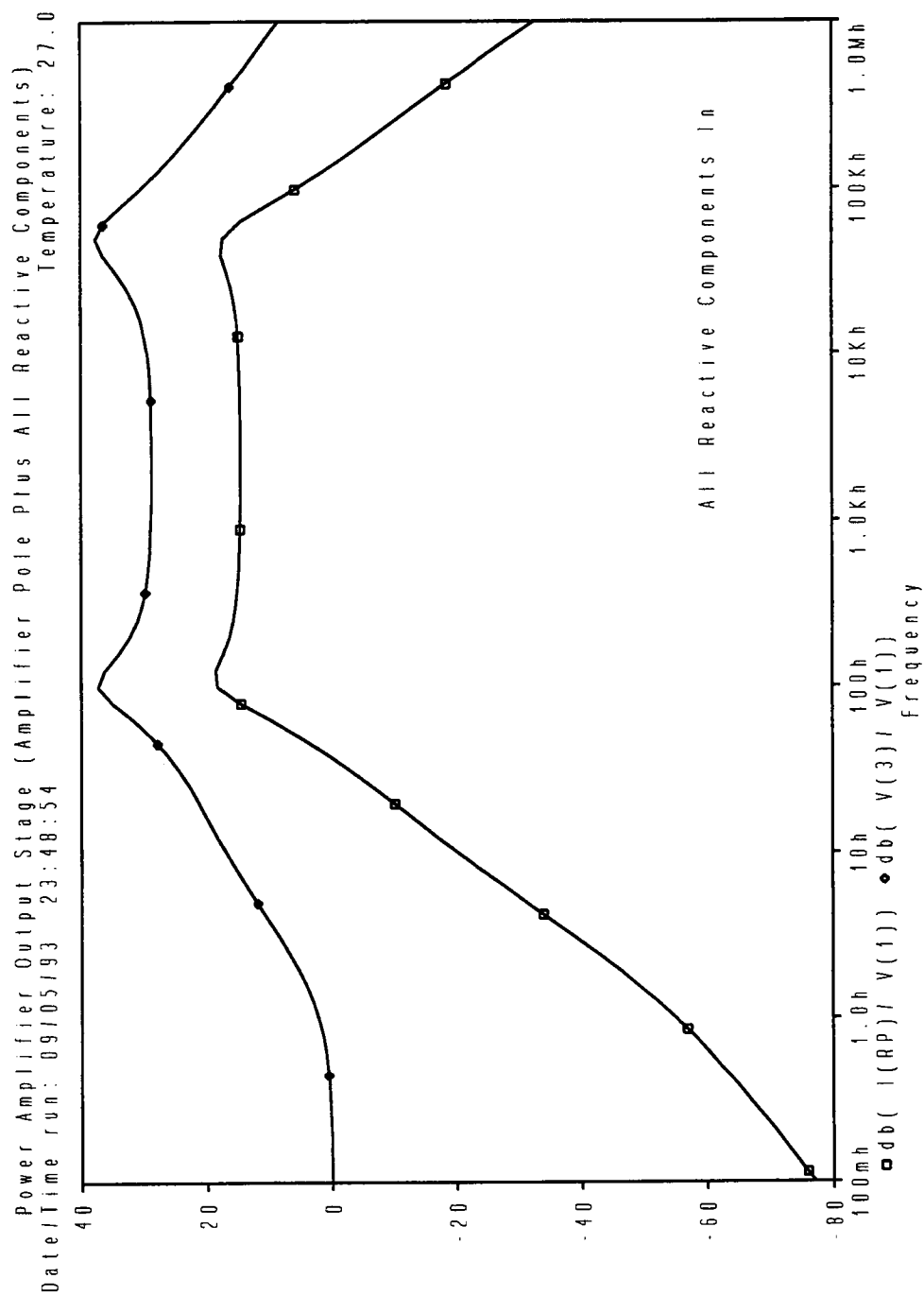


Figure 2.77. Magnitude response with all reactive components.

The midband gain in Figure 2.77 was measured at 14.57db during simulation which corresponds to a transconductance gain of 5.35 amps/volt. This is 3.8% lower than predicted by equation 2.30. This error is caused by the increased impedance of the transformer primary ($R_p = 4.9\Omega$) which was assumed to be 4Ω in the derivation of equation 2.30.

From Figures 2.67 through 2.77 it can be seen that the capacitors C_1 , C_3 , and C_p control the low frequency behavior of the response while C_2 adds an additional 20db per decade high frequency roll off. C_1 and C_3 each add a pole-zero pair (Figures 2.68 and 2.70 respectively) to the response. The peaking in the response at 100Hz in Figure 2.74 is associated with the addition of C_p which contributes a zero in the voltage response (Figure 2.71) at a frequency of $f_{\text{zero}} = 1/2\pi C_p(R_p + R_s)$. This zero in the voltage response due to C_p also contributes a pole in the loop response. Multiple PSPICE simulations revealed that the peaking at 100Hz grew larger as the zero in the voltage response associated with C_p moved higher in frequency. This was accomplished by decreasing the size of C_p . If this zero frequency decreased, the peaking in the response also decreased. This peaking could be completely removed by moving the zero in the voltage response (Figure 2.71) associated with C_p to a frequency less than or equal to the pole in the current response (Figure 2.68) associated with C_1 . Figures 2.73 through 2.77 show the addition of this effect does cause the peaking at 100Hz. The addition of R_s in series with C_p (Figure 2.75) reduces the frequency of the zero (voltage response) associated with C_p to a frequency lower than the pole (current response) associated with C_1 and the peaking is minimized. Figure 2.76 shows the response with $L_1 = 10\mu\text{H}$ included in parallel with

$R_s = 10\Omega$ (this network is recommended by National Semiconductor for use with the LM1875 amplifier to present the amplifier output with a high impedance at high frequencies to prevent oscillation). L_1 shorts out R_s at low frequencies which moves the zero in the voltage response associated with C_p back to $1/2\pi C_p(R_p + R_s)$ so the peaking is still present.

The high frequency end of the response is controlled by the open-loop pole of the LM1875 amplifier, C_2 , L_1 , and L_p . This can be seen in Figures 2.76 and 2.77. The open-loop pole of the amplifier, along with C_2 , contribute an additional 40db per decade roll off. The effect of L_1 and L_p can be determined by examining the impedance between nodes 3 and 5 in Figure 2.66. Figure 2.78 shows this circuitry. Figure 2.79 shows the response of Figure 2.78 with L_p shorted. L_1 creates an impedance pole-zero pair which is responsible for the peaking observed in Figure 2.76. Figure 2.80 shows the response of Figure 2.78 with L_1 open while Figure 2.81 shows the complete response. This increasing impedance between nodes 3 and 5 at approximately 40KHz requires additional voltage from the amplifier output to maintain the required transformer primary current I_p (and V_b). This effect results in a zero in both the voltage and current closed-loop response at approximately 40KHz, and can be seen in Figure 2.77.

Although the peaking in the frequency response is undesirable, its location at approximately one decade above and below the frequency range of interest will render its influence negligible. The peaking is approximately 4db above the midband gain which is acceptable from an amplifier design standpoint, as long as the phase margin remains within acceptable limits. This peaking does indicate a loss of phase margin and it will be

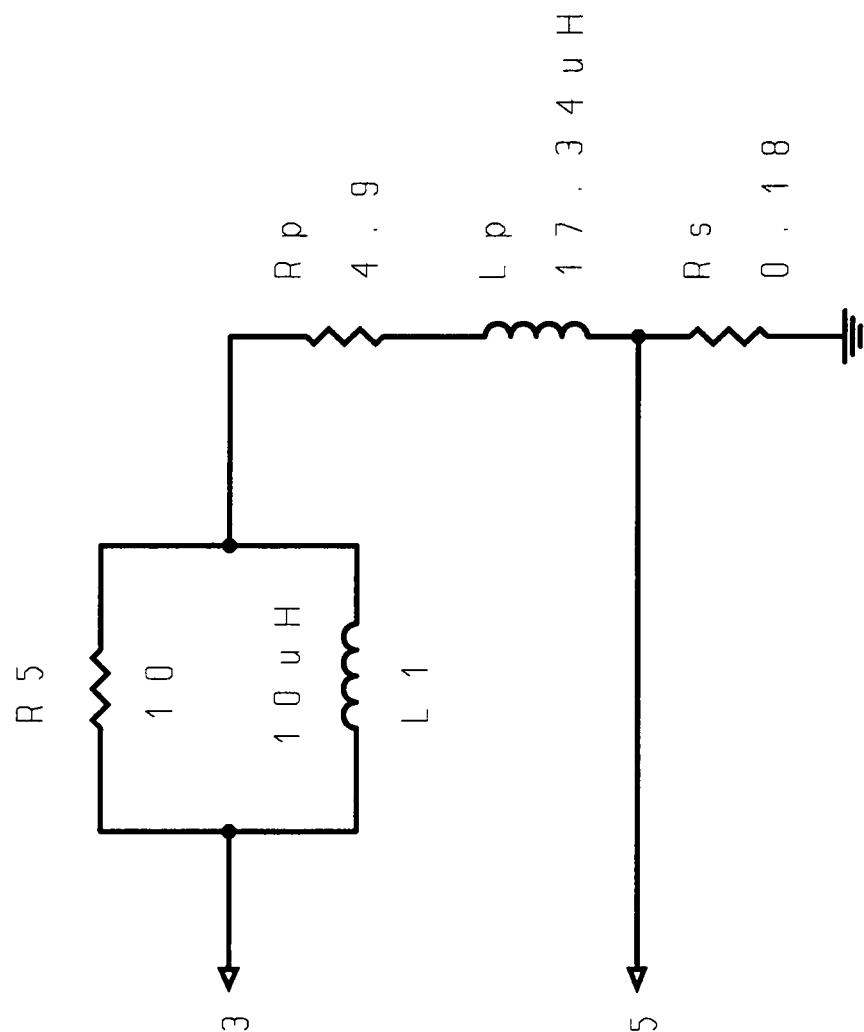


Figure 2.78. Node 3 to 5 circuitry.

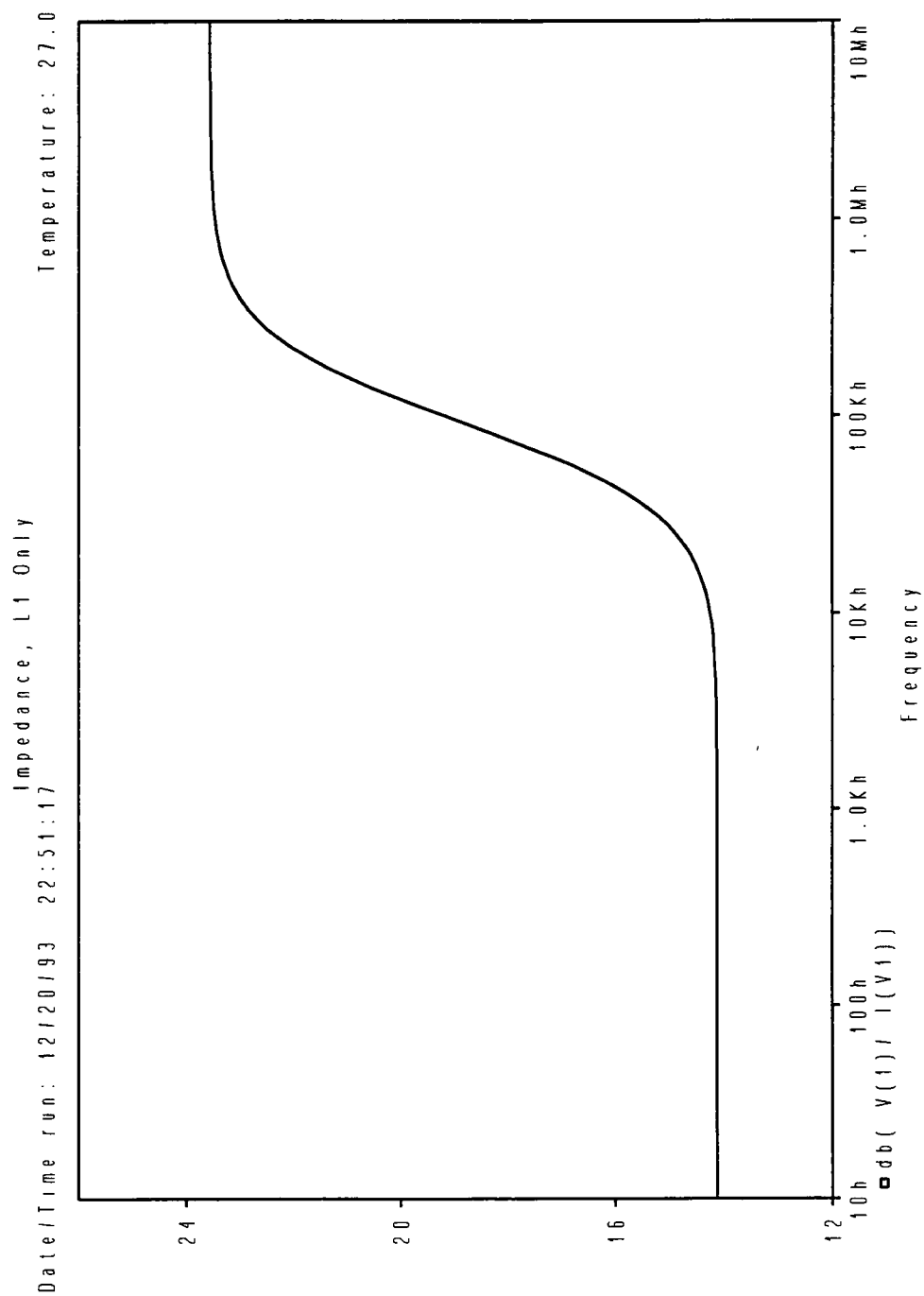


Figure 2.79. Node 3 to 5 impedance, L_p shorted.

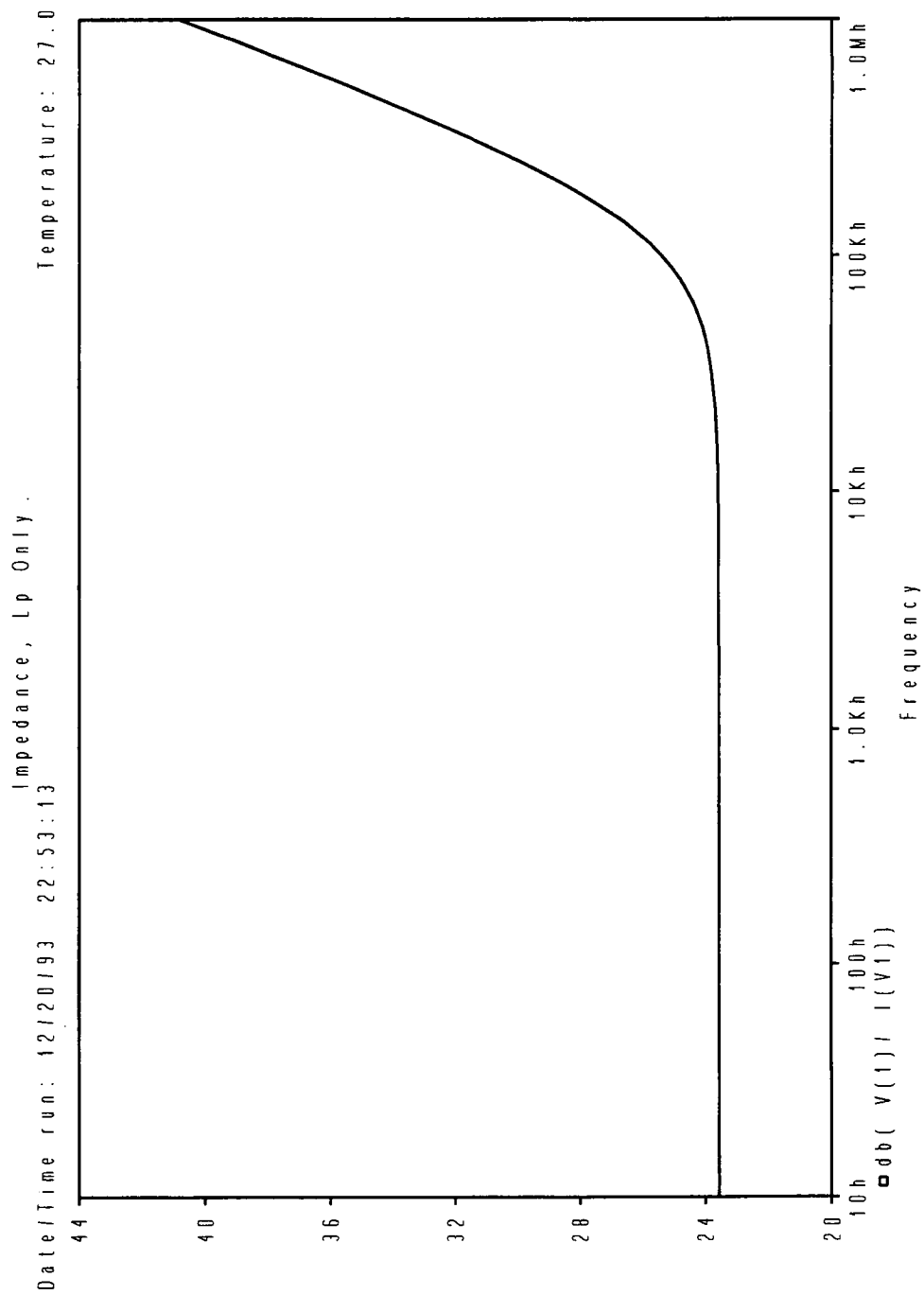


Figure 2.80. Node 3 to 5 impedance, L_1 open.

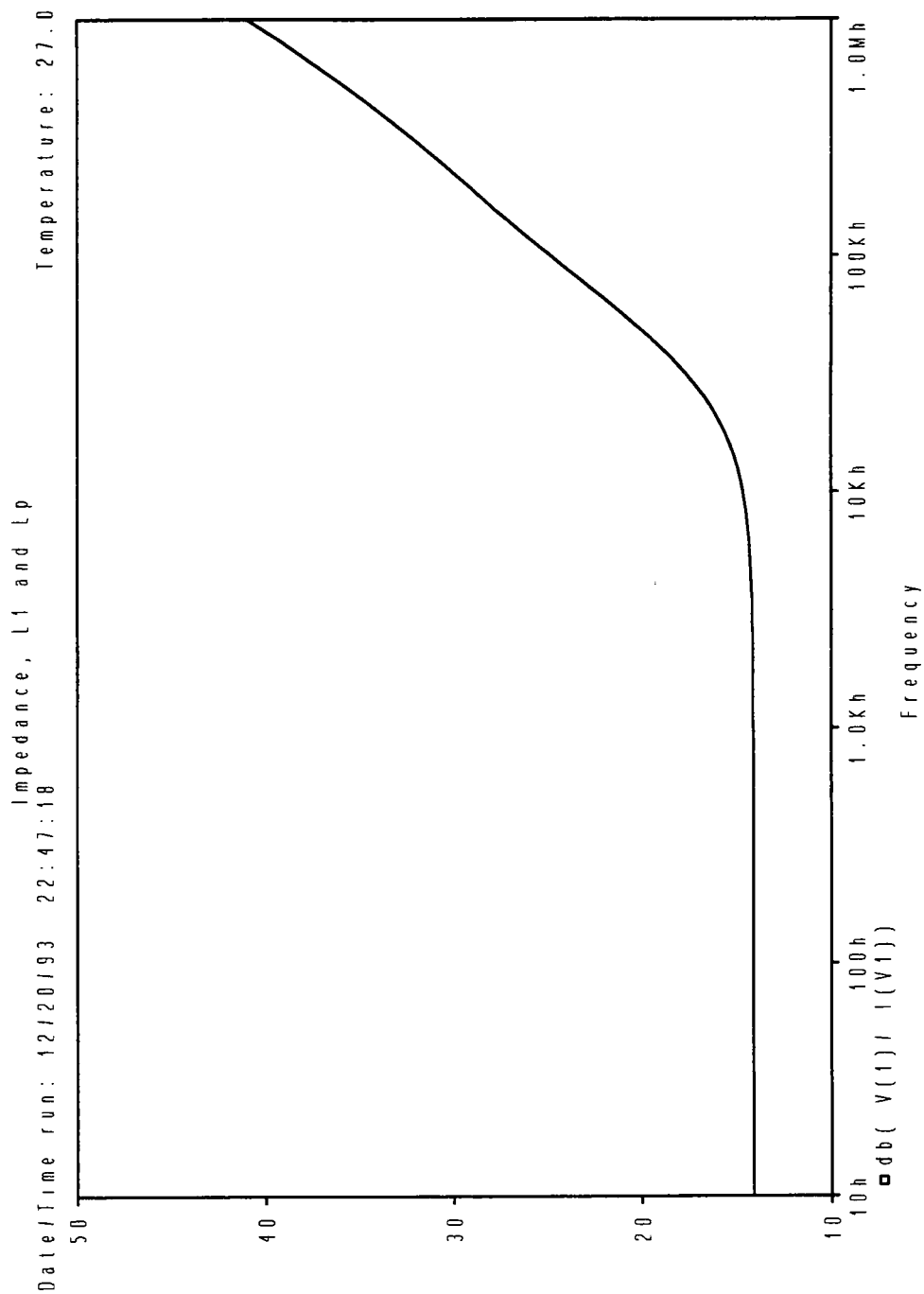


Figure 2.81. Node 3 to 5 impedance, L_1 and L_p .

necessary to examine this. This is the topic of the next section.

2.4.3 Power Amplifier Feedback Loop Analysis

Having developed an acceptable model (Figure 2.66) for the overall amplifier, this model can now be used to study the stability against oscillations of the circuit. To verify the amplifier stability, the model shown in Figure 2.66 is modified as shown in Figure 2.82 in order to study the loop transmission.

In order to accurately simulate the loop transmission, the feedback loop is broken at node 5 and a test voltage inserted as shown in Figure 2.82. Given the small value (0.18Ω) of R_s , this is the most convenient place to break the loop without upsetting the loop loading conditions. When the feedback loop is broken, the impedance levels at the point where the loop is broken must not change or the analysis will be invalid. The impedance from node 5 to ground is so small that the insertion of the test voltage at node 5 in Figure 2.82 will not affect the impedance levels at this node. With the noninverting input to the LM1875 amplifier grounded, the loop transmission to be simulated is $V(5)/V(1)$. Although the overall magnitude response was $I(R_p)/V(1)$, to be dimensionally consistent the return voltage as a function of loop gain, given an input test voltage, is required in this analysis to verify stability.

Two quantities are important when discussing the stability of a feedback amplifier, (1) gain margin, and (2) phase margin. Gain margin is defined as the difference between the loop transmission ($T(f)$) and unity gain at the frequency where the phase shift from

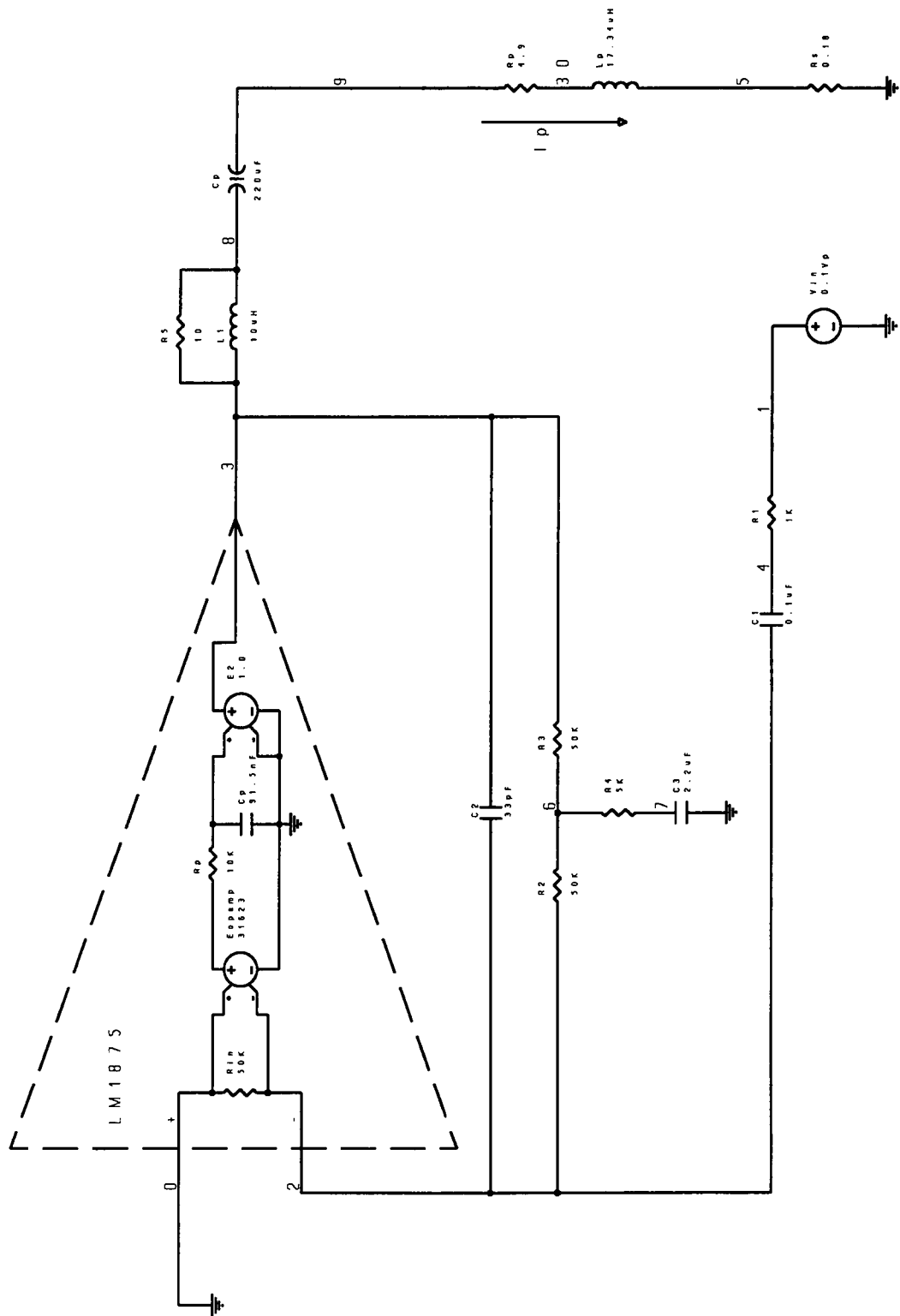


Figure 2.82. Loop transmission model.

input to output is 180° . Phase margin is defined as the difference between the phase angle of the output signal and 180° at a loop transmission ($T(f)$) gain of 0db. In order to adapt these definitions to the circuit of Figure 2.82, which is a bandpass amplifier, it will be necessary to measure the gain margin at the frequencies where the phase shift is $\pm 180^\circ$ away from the midband phase shift of -180° , or 0° and -360° , and to measure phase margin at both the upper and lower 0db gain crossings.

Simulation of the circuit in Figure 2.82 results in the loop transmission magnitude and phase curves shown in Figures 2.83 and 2.84 where the points required to determine the gain and phase margin at the upper and lower frequency points are labeled in each figure. From Figures 2.83 and 2.84 the gain margin at 0° is seen to be $G.M._0 = 17.8\text{db}$ and the gain margin at -360° is $G.M._{-360} = 51.4\text{db}$. Likewise, the phase margin at the lower frequency 0db gain crossing is $P.M._{\text{lower } 0\text{db}} = 38.9^\circ$ and the phase margin at the upper 0db gain crossing is $P.M._{\text{upper } 0\text{db}} = 43.0^\circ$. A large value of phase margin indicates a more stable closed loop response with smaller peaking (smaller overshoot in the step response) and a small value of phase margin indicates a less stable response with larger peaking (larger overshoot in the step response). This can be seen from Figure 2.77 where the lower frequency peaking that is due to a phase margin of $P.M._{\text{lower } 0\text{db}} = 38.9^\circ$ and is larger than the high frequency peaking where the phase margin is $P.M._{\text{upper } 0\text{db}} = 43.0^\circ$. In both cases the phase margin is greater than or equal to 38.9° which indicates a stable closed loop response.

Although the results of this simulation indicate a stable response, it was necessary to verify the accuracy of the loop transmission simulation with the prototype experimental

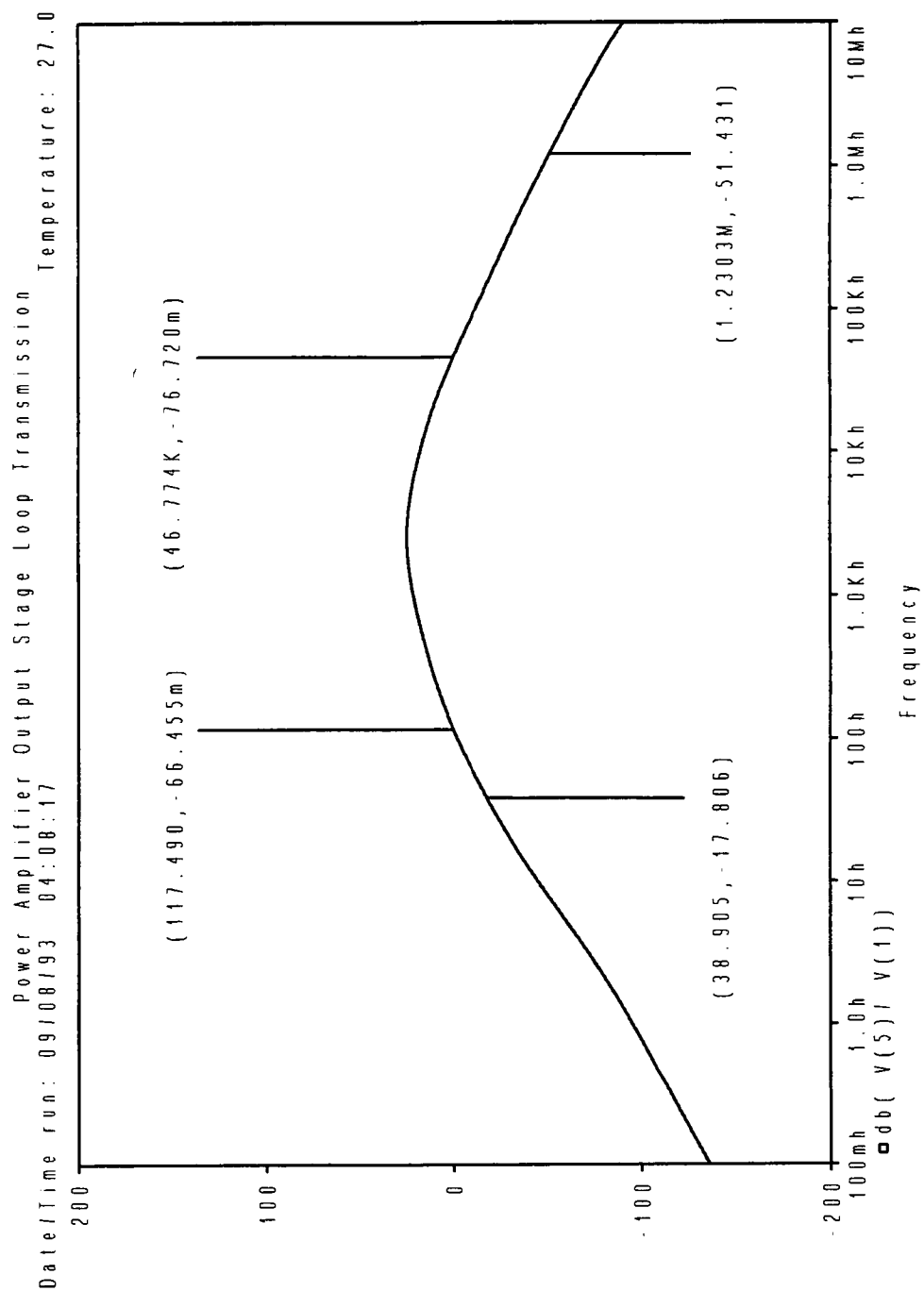


Figure 2.83. Loop transmission magnitude response.

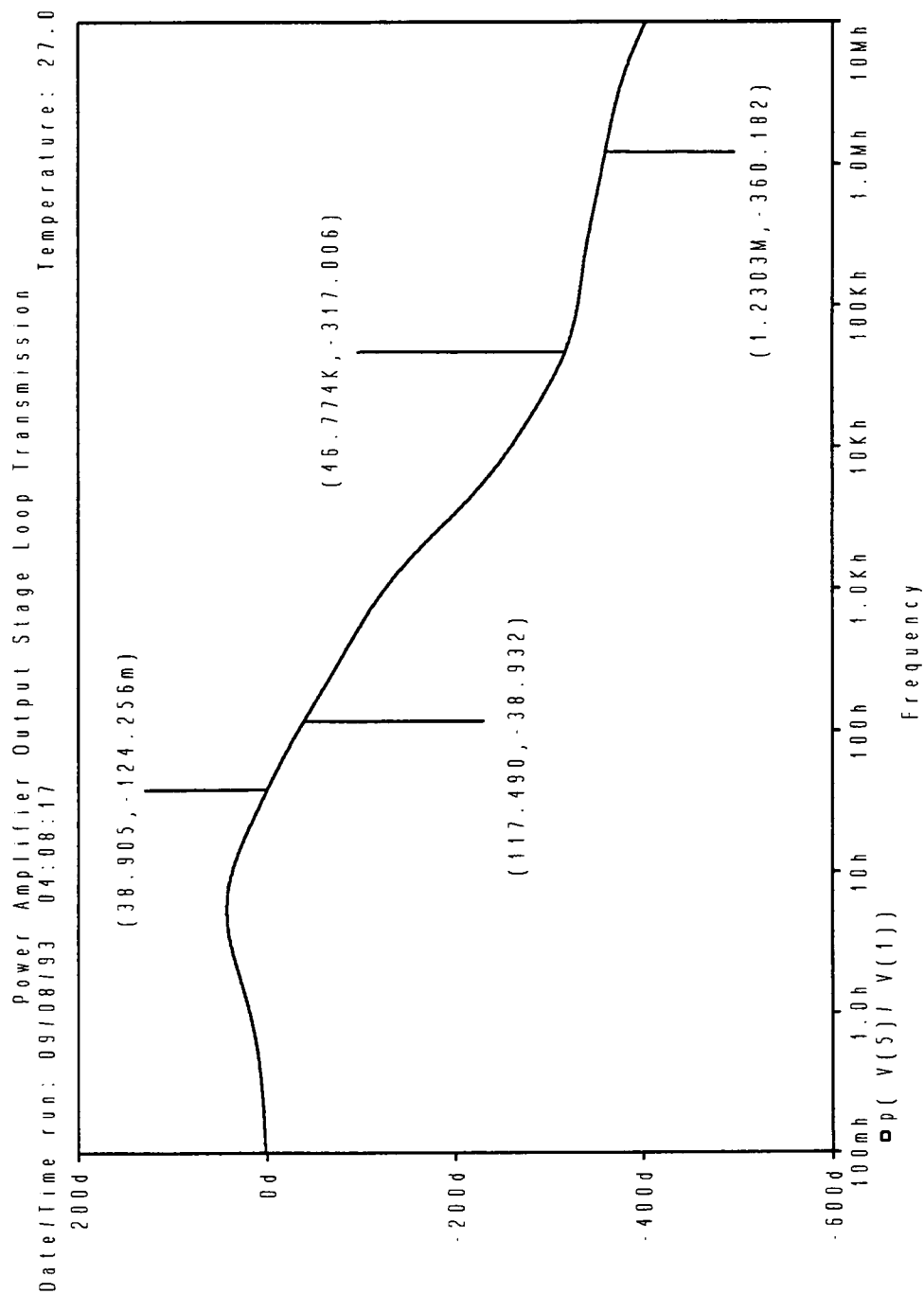


Figure 2.84. Loop transmission phase response.

loop transmission. This was accomplished by grounding the noninverting input of the LM1875, lifting the leg of R_1 in Figure 2.82 connected to node 5 and applying a test voltage. The amplitude and phase of the return voltage at node 5 was measured and recorded. As before, the phase of the return voltage at node 5 was measured with respect to the positive slope zero crossing of test voltage. The data acquired from this experiment is shown in Table D.1 in Appendix D. A bode plot of the data given in Table D.1 is shown in Figures 2.85 and 2.86. The magnitude response shown in Figure 2.85 was derived using $db = 20 \log_{10}(V(5)/V(1))$ where $V(1) = 0.01 V_{peak}$.

Comparing Figures 2.85 and 2.86 with Figures 2.83 and 2.84 shows good agreement so the results of the loop transmission analysis imply that the closed loop response of the overall amplifier will be stable. This is indeed the case with the prototype amplifier which showed no tendency to oscillate. This also means that the printed circuit board layout used for the amplifier is acceptable because the output amplifiers are high current circuits and board layout is important to minimize ground loops and parasitics that could result in spurious oscillation.

2.4.4 Output Current Measurement

In order to provide the user a measurement of output current, the circuit shown in Figure 2.87 was designed to provide an isolated, analog ground referenced AC voltage that is proportional to output current. Transformers T1 (channel 1) and T2 (channel 2) in Figure 2.87 are connected in series with the secondary of their respective output

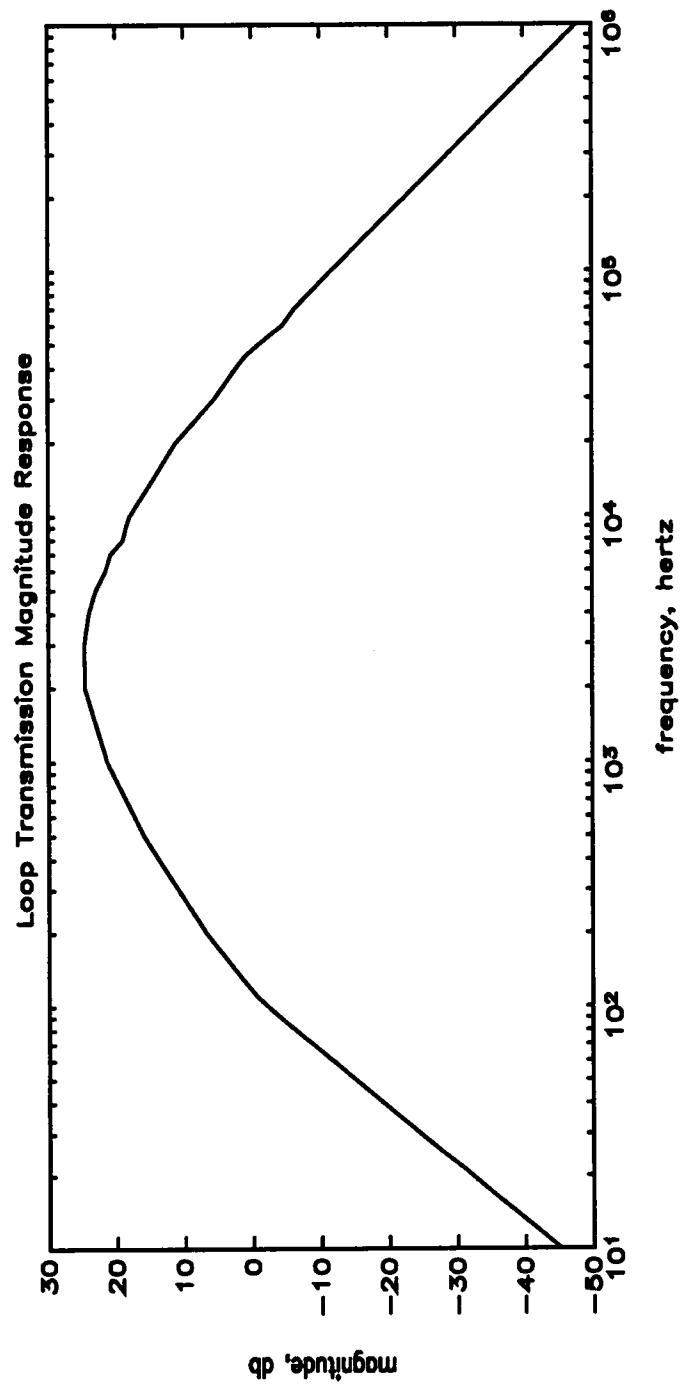


Figure 2.85. Experimental loop transmission magnitude response.

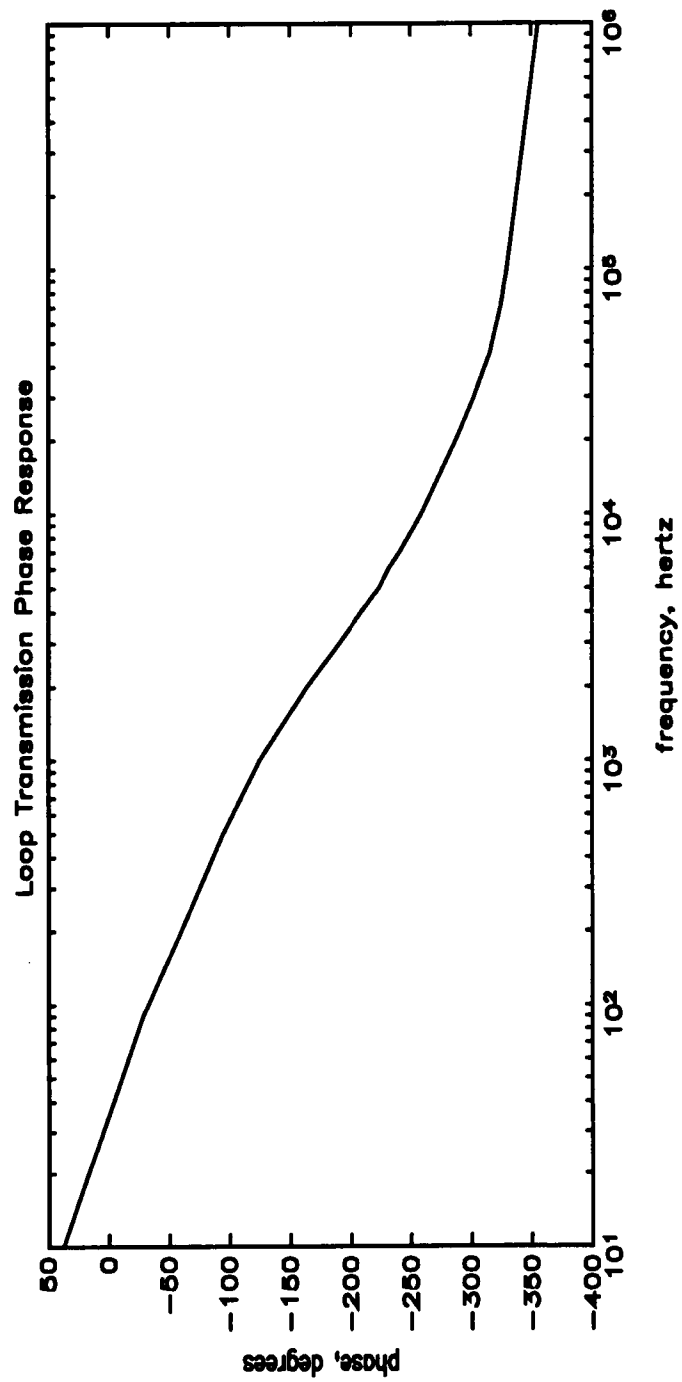


Figure 2.86. Experimental loop transmission phase response.

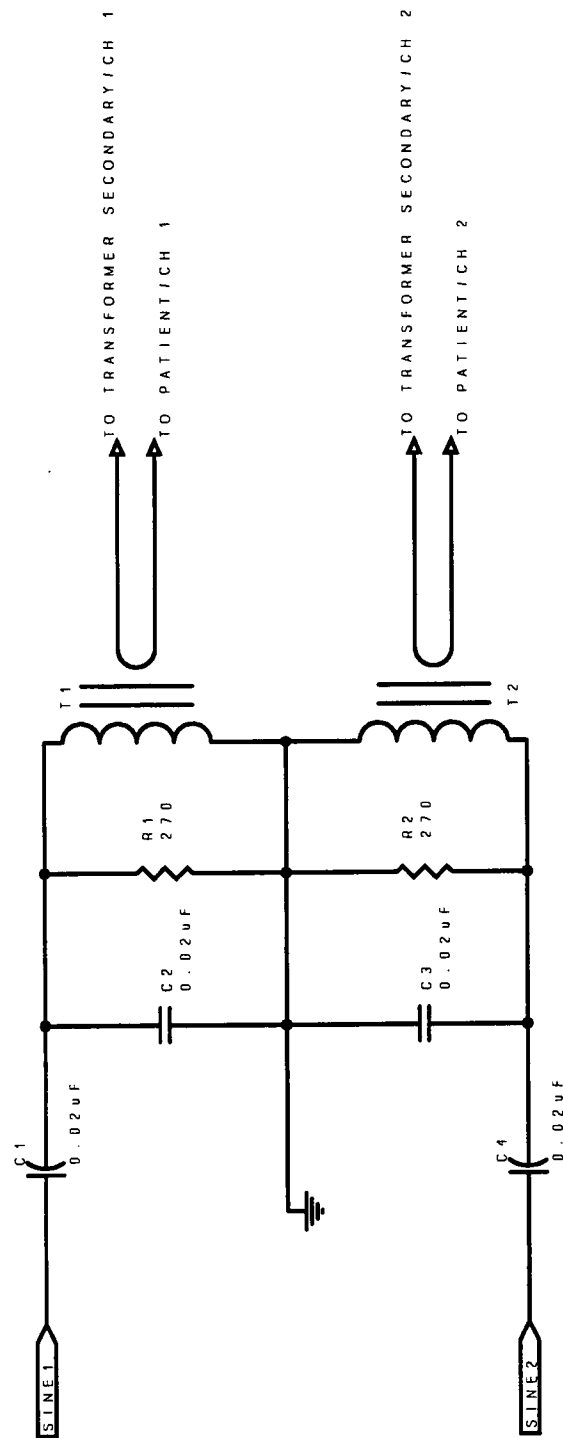


Figure 2.87. Isolated current to voltage converter.

transformers and the patient. This can be seen by referring to Figure 2.53 where T2 in Figure 2.53 is T1 in Figure 2.87. T1 and T2 consist of a 200 turn secondary wound on a torodial core with a single turn of 18 #a.w.g. wire used as the primary. R_1 and R_2 are burden resistors used to convert the secondary currents to voltages. C_2 and C_3 provide high frequency filtering while C_1 and C_4 ac couple the outputs to the remaining signal processing circuitry.

With a measured full-scale output current of 50mA rms flowing in the primary, the secondary voltage was measured at 70mV rms. This results in an effectively measured secondary current of 260 μ A rms. These measurements result in a current ratio for T1 and T2 in Figure 2.87 of 192.3:1.

The circuitry shown in Figure 2.88 was designed to provide a dc voltage proportional to the rms value of the output current waveforms which are pure sine waves and amplitude modulated sine waves. Root mean square measurement gives an indication of the energy content of a particular wave shape and is the most appropriate measurement technique for this instrument.

The output signals SINE 1 and SINE 2 in Figure 2.87 are amplified by U1 and U2 in Figure 2.88. The AD711's are configured as ac noninverting voltage amplifiers by the addition of C_1 and C_3 in their feedback paths. In this configuration, the dc gain of U1 and U2 is unity so the only dc voltage present at either output is due to the input offset voltage which is 3mV maximum referred to the output. R_2 and R_4 provide gain adjustments for each channel due to errors in transformer coupling and resistor tolerances. The output signals of U1 and U2 are ac coupled to the inputs of the AD736 RMS-to-DC

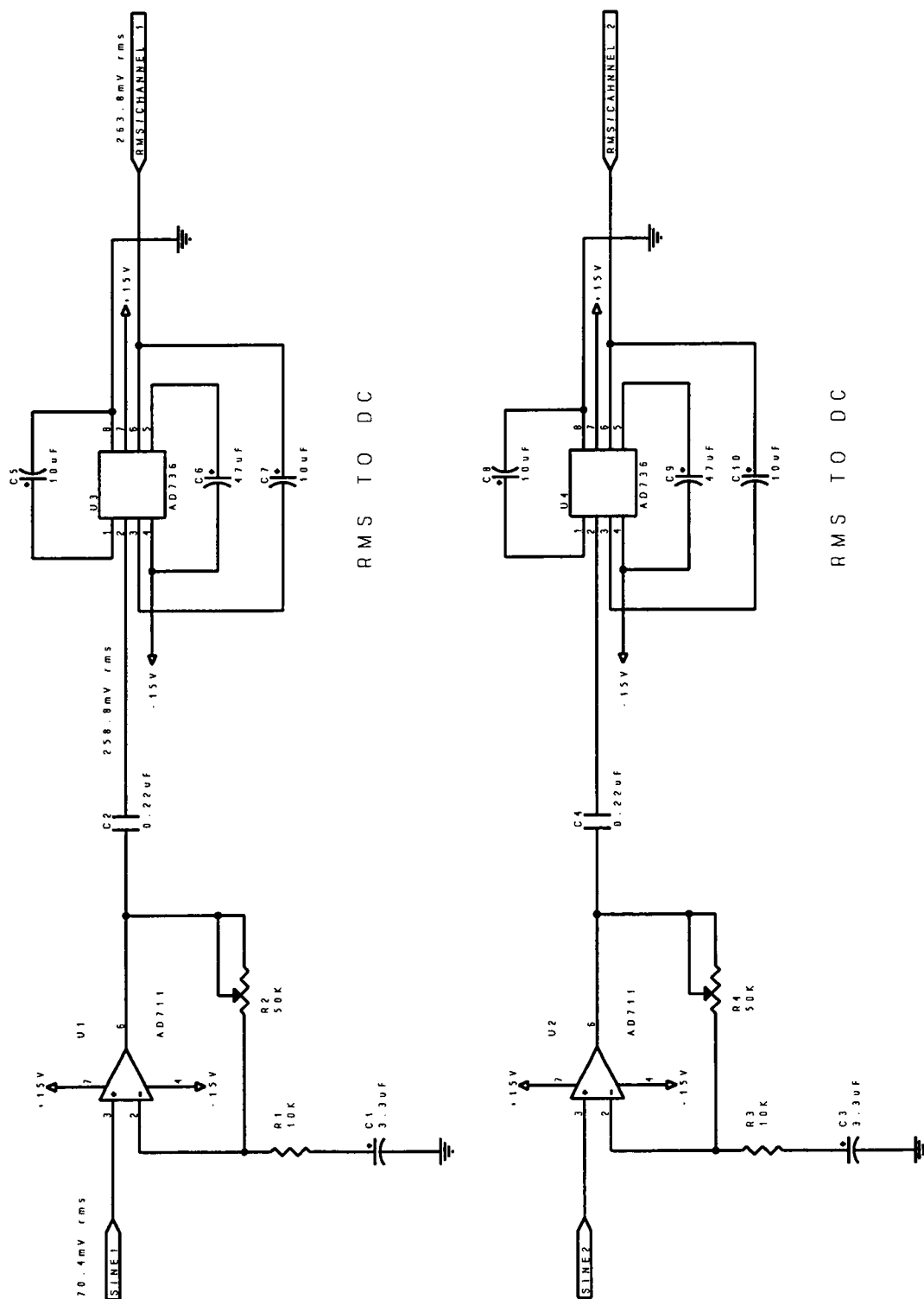


Figure 2.88. RMS-to-DC converter.

converters. With each output channel producing 50mA rms, R_2 and R_4 are adjusted to provide 200mV dc on the output (pin 6) of the respective RMS-to-DC converter. This adjustment provides calibration of the full-scale output of the AD736 and at the same time acts as an external error trim. The remaining errors are (1) nonlinearity, (2) drift over temperature, (3) drift versus supply voltage variation, and (4) crest factor. Before proceeding with the detailed error analysis of Figure 2.88, an understanding of crest factor, which is major source of error in the AD736, is necessary.

Crest factor is the ratio of peak signal current to its theoretical rms current. The theoretical rms value is defined as

$$I_{rms} = \sqrt{\frac{1}{T} \int_0^T i^2(t) dt} \quad \text{Eq. 2.57}$$

where $i(t)$ is the waveform in question and T is the period of $i(t)$. Given $i(t) = A_m \sin \omega t$, which is a pure sine wave with frequency ω rad/s, evaluating equation 2.57 for I_{rms} results in an rms value of $A_m/1.414$. The crest factor for a pure sine wave is therefore

$$C.F. = \frac{PEAK}{RMS} = \frac{A_m}{\frac{A_m}{\sqrt{2}}} = \sqrt{2} = 1.414 . \quad \text{Eq. 2.58}$$

The output waveforms produced by this instrument are pure sine waves and amplitude modulated sine waves. In the modulated treatment mode, the output current waveform is an amplitude modulated sine wave. The generation of this waveform was described in section 2.3 and is shown in Figure 2.49. The gain of the summer circuit is

1/2 so the mathematical expression for the amplitude modulated waveform in terms of output current is

$$I(t) = \frac{1}{2} (A_p \sin(2\pi f_1 t) + B_p \sin(2\pi f_2 t)) \quad \text{Eq. 2.59}$$

where A_p and B_p are the peak amplitudes of channel 1 and channel 2 respectively, f_1 and f_2 are the frequencies of the respective channels, and t is the independent variable time. Substituting $I(t)$ in equation 2.59 into equation 2.57 yields

$$I_{rms} = \sqrt{\frac{1}{4T} \int_0^T (A_p \sin(2\pi f_1 t) + B_p \sin(2\pi f_2 t))^2 dt} \quad \text{Eq. 2.60}$$

Using $A_p = B_p = 70.711\text{mA}$ peak (50mA rms), $f_1 = 5000\text{Hz}$, $f_2 = 4800\text{Hz}$, and $T = 5\text{msec}$ (beat frequency = 200Hz), equation 2.60 gives the rms value of the amplitude modulated waveform as

$$I_{rms} = 35.3555 \text{ mA} \quad \text{Eq. 2.61}$$

Substituting this value into equation 2.58 along with a peak value of 70.711mA we find the crest factor of the amplitude modulated waveform as

$$C.F. = \frac{70.711 \text{ mA}}{35.3555 \text{ mA}} = 2.00$$

Eq. 2.62

so the AD736 RMS-to-DC converters in Figure 2.88 must be able to convert waveforms with crest factors in the range $1.414 \leq C.F. \leq 2.0$ without significant loss of accuracy.

Returning to the error analysis of Figure 2.88, Table 2.3 shows the data sheet specifications (only the previously mentioned error sources are shown) for the AD736. The $\pm 15\text{V}$ supplies that power the AD736's in Figure 2.88 have a tolerance of $\pm 10\%$ so the worst case supply voltage variation expected would be 3V. Assuming a 200mV rms full-scale input voltage, the individual error contributions of the AD736 are

Temperature drift error $= \pm 0.7\text{mV} \pm (200\text{mV}) 0.7\%$

(0 to 70 °C) $= \pm 0.7\text{mV} \pm 1.4\text{mV}$

$= -2.1\text{mV to } +2.1\text{mV}$

Supply voltage drift error $= +0.1\% (3\text{V}) = +3\text{mV}$

Nonlinearity error $= +0.35\% (200\text{mV}) = +700\mu\text{V}$

Crest factor error $= 0.7\% (200\text{mV}) = 1.4\text{mV}$

Table 2.3**AD736 Error Specifications**

Conversion Accuracy	Conditions	MIN	TYPICAL	MAX	Units
0 to 70 °C	@ 200mV rms			0.7 / 0.7	±mV/ ± % of reading
versus supply voltage	$V_s = \pm 5V$ to $\pm 16.5V$	0	+0.06	+0.1	% / V
Non - linearity, 0 - 200mV	@100mV rms	0	+0.25	+0.35	% of reading
Crest Factor 1 to 3	@200mV rms		0.7		% additional error

where the individual error terms add in rms fashion so the total error is found as

$$V_e = \sqrt{(2.1mV)^2 + (3mV)^2 + (700\mu V)^2 + (1.4mV)^2} = 4mV . \quad \text{Eq. 2.63}$$

The full-scale output of 200mV dc corresponds to a full-scale output current of 50mA rms. An error of 4mV corresponds to an output current error of

$$I_{oe} = \left(\frac{50mA \text{ rms}}{200mV} \right) = 1mA \text{ rms} \quad \text{Eq. 2.64}$$

or a full-scale error of 2%. The development of this error is based on worst case error specifications and in general the circuit will not see such extremes. Over the 15 to 35 °C temperature range for which the instrument is designed, the error contributed by temperature drift would be substantially smaller, being typically $\pm 1mV$. Also, a supply voltage variation of $\pm 3V$ would result in an error of 120mV using the typical error specification of 0.06% / V in Table 2.3. The nonlinearity error would also be smaller, with a typical error contribution of 500 μV . If these typical errors are summed as in Equation 2.63, the result is an error of approximately 1.8mV which corresponds to an output current error of 450 μA rms or 0.9% of full-scale.

The capacitors C_5 through C_{10} in Figure 2.88 set the low frequency pole to approximately 2Hz. If the instrument is in the modulated treatment mode and the beat frequency is set to 2Hz or less, the output of the AD736 will follow the input signal peaks resulting in a flickering display (the display is discussed in a later section).

2.5 Control Logic and Safety Circuitry

This section describes the logic circuitry that is used to control the various operating modes of the instrument, output current measurement display, treatment timer, and safety related circuitry. The control logic is CD series CMOS operating at 0V (logic 0) and +5V (logic 1) logic levels.

The controls available to the user are shown in Table 2.4. These controls convert user inputs into logic signals that are used throughout the instrument to control and monitor the instrument's operation.

2.5.1 Control Logic

The instrument controls (switches) are grouped together according to functionality. For example, the start / stop switches, modulated / unmodulated switches, 5KHz / 2.5KHz switches, and channel 1 / channel 2 switches are grouped together to simplify instrument operation.

In order to provide the necessary logic signals from the different switch groups, the circuit shown in Figure 2.89 was developed. This same circuit is used for the following groups: modulated / unmodulated, 5KHz / 2.5KHz, and channel 1 / channel 2.

Table 2.4
User Controls

Control	Description	Indicator
Start	Start treatment	LED
Stop	Stop treatment	LED
Modulated	Modulated output waveform	LED
Unmodulated	Unmodulated output waveform	LED
5KHz	5KHz carrier frequency	LED
2.5KHz	2.5KHz carrier frequency	LED
Channel 1	Channel 1 current display	2 digit display
Channel 2	Channel 2 current display	2 digit display
Treatment Time	Thumbwheel switches	4 digit display

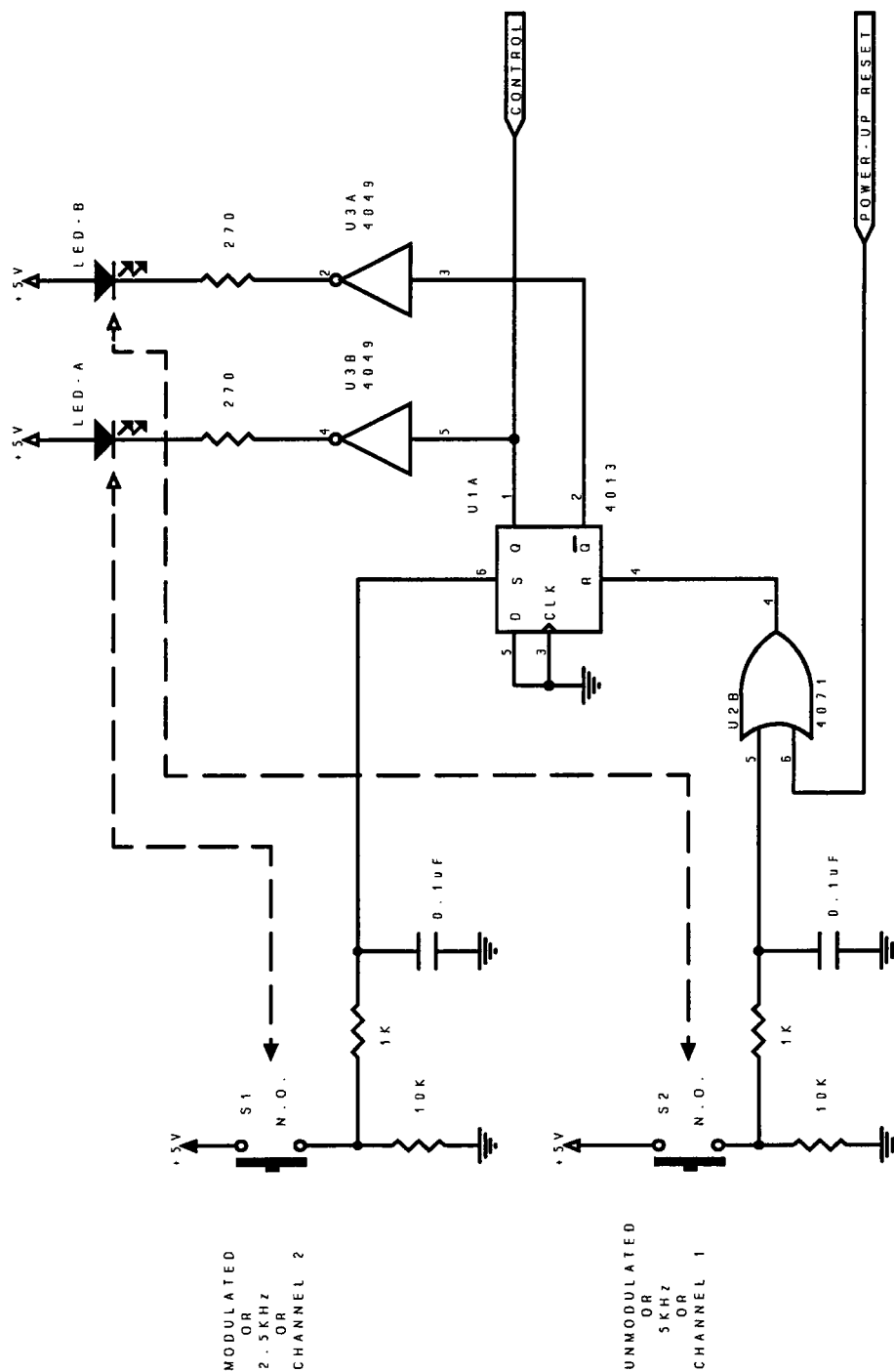


Figure 2.89. Switch control logic.

When power is applied to the instrument, the circuit shown in Figure 2.90 provides a reset pulse for all control logic. The diode provides a discharge path around the $50\text{K}\Omega$ resistor to quickly discharge the $2.2\mu\text{F}$ capacitor in the event of a brief power loss. This forces a system reset when power is restored. Referring to Figure 2.89, this reset pulse, applied to one input of the 4071 OR gate, clears the Q output of the 4013 D flip-flop (logic 0). In this state, LED-A is off, LED-B is on, and the CONTROL signal is low. It should be noted that LED-A is part of the S1 assembly and LED-B is part of S2. The CONTROL signal, depending on the particular group of switches under consideration, connects to the logic control of a CD4053 analog switch. For example, if the circuit in Figure 2.89 is the modulated / unmodulated group, then the CONTROL signal in Figure 2.89 connects to the MOD / UNMOD signal in Figure 2.49.

The 4053 analog switch in Figure 2.49 is configured to switch signals in the $\pm 5\text{V}$ range based on a logic control signal in the 0V to 5V range. Since the CONTROL signal (MOD/UNMOD in Figure 2.49) is 0V at power-up, Z_0 is connected to Z and Y_0 is connected to Y in Figure 2.49. In this condition the CH2 INTENSITY and CH1 INTENSITY signals are pure unmodulated sine waves. If switch S1 in Figure 2.89 is pressed, this sets the Q-output of the 4013 to logic 1 (+5V). Referring to Figure 2.49, Z_1 and Y_1 would now be connected to Z and Y and the amplitude modulated signal present on pin 6 of the AD711 appears as the CH1 INTENSITY and CH2 INTENSITY signals. The $1\text{K}\Omega$ - $0.1\mu\text{F}$ low-pass filters in Figure 2.89 are used to filter the contact bounce noise produced during switching and the $10\text{K}\Omega$ resistors provide a discharge path for the capacitors when the switches are open.

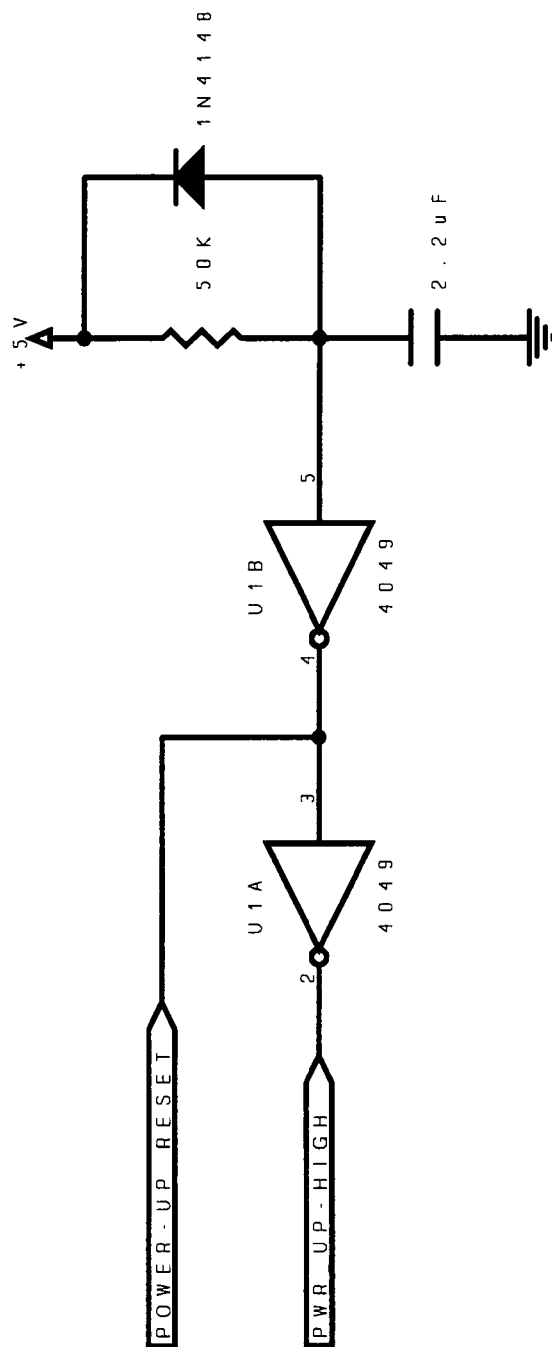


Figure 2.90. Power-up reset.

The remaining switch groups, 5KHz / 2.5KHz and channel 1 / channel 2, use the same circuitry as shown in Figure 2.89, with the exception of where each group's CONTROL signal connects, as shown in Figure 2.91. For the 5KHz / 2.5KHz group, the CONTROL signal connects to the signal 5KHZ in Figure 2.91. At power-up this signal is a logic 0 so X_0 (-5V) is connected to X in Figure 2.91. The FREQUENCY SELECT signal in Figure 2.91 connects to the same signal in Figure 2.4. Since this signal is -5V, the multiplexer output frequency will be 500KHz. Pressing S1 in Figure 2.89 switches the CONTROL signal to a logic 1 which switches FREQUENCY SELECT in Figure 2.91 to +5V. In this state, the multiplexer output frequency will be 250KHz.

For the channel 1/channel 2 group, the CONTROL signal connects to CHANNEL 1 in Figure 2.91. At power-up, RMS/CHANNEL 1 is connected to Y in Figure 2.91. This CURRENT DISPLAY signal is sent to a meter circuit that displays the output current in mA rms on an LED display. This switching arrangement allows one meter circuit to be used for both channels.

The operation of the Z_0 , Z_1 , Z, and control C switch group in Figure 2.91 was explained in section 2.3 with the exception of the signal RUN-ENABLE. This signal is a logic 0 until all operating and safety considerations are satisfied and its generation will be discussed in section 2.5.3. The start/stop group is intimately related to the treatment timer circuitry and will be discussed in that section.

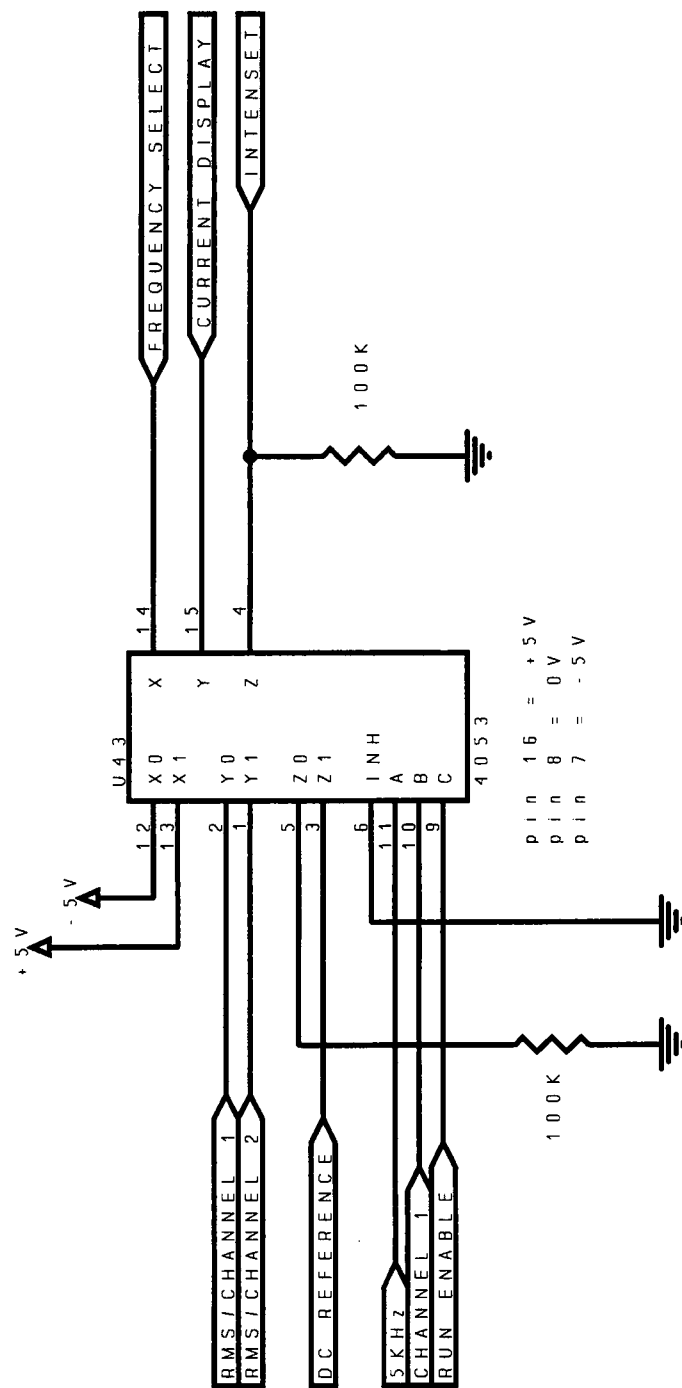


Figure 2.91. Switching control.

2.5.2 Treatment Timer

The purpose of the treatment timer is to provide a variable treatment time up to a maximum of 59 minutes and 59 seconds. The amount of time required is selected by 4 thumbwheel switches on the front panel of the instrument. When the start switch is pressed, the thumbwheel setting is loaded into a counter/display driver integrated circuit and the selected time is displayed on a 4-digit LED display. The timer is configured as a down counter so the display decrements once each second until a count of 00:00 is reached at which time the instrument stops treatment. If the stop switch is pressed at any time during treatment, the counter is reset to 00.00 and treatment stops.

The timer is based on an ICM7217B 4-digit programmable up/down counter. The complete timer circuit along with the start/stop logic is shown in Figure 2.92. The LOAD COUNTER (LC) and LOAD REGISTER (LR) inputs in Figure 2.92 are biased at 2.5V for normal operation by R_3 and R_4 . When the start switch is pressed, LC and LR are connected to +5V which initiates a load sequence. During this load sequence, the BCD inputs, pins 4 through 7, multiplex the data present on the thumbwheel switches into the internal counter and register. This is accomplished automatically by the 7217B by sequentially driving pins 25 through 28 high and storing this information in the appropriate register. The synchronization of digits is controlled by the 7217B. When the start switch is released, the segment drivers update the LED's with the data contained in the counter and normal operation resumes. The device is configured as a down counter by strapping pin 10 (UP/DN) low which causes the internal counter to be decremented

one count at each rising edge of pin 8 (COUNT INPUT). Pin 9 (STORE) is strapped low which transfers the contents of the counter to the latches which drive the seven segment outputs.

The seven segment outputs are multiplexed at a duty cycle of 25:1 and a nominal frequency of 2.5KHz to reduce power consumption. This multiplex frequency is set by an internal capacitor but can be changed by adding a capacitor between pin 13 (SCAN) and ground, but was not necessary in this application. Three status pins, CARRY (pin 1), ZERO (pin 2), and EQUAL (pin 3) are provided to indicate the status of the internal registers. CARRY and EQUAL are not used and will not be discussed. The status signal ZERO (pin 2), is logic 1 as long as the internal counter contains any number other than zero. When the counter reaches zero, ZERO switches to logic 0 (active low) to signal external circuitry.

At power-up, the signal PWR-UP-HIGH is low for approximately 110msec. The circuit that generates this signal is shown in Figure 2.90. This drives pin 14 (RESET) of the 7217B low which resets the IC. A reset of the 7217B clears the internal counter to zero and all LED's will show zero. Also, the status signal ZERO (pin 2) will be low in this state. With ZERO low, the output of U2B will also be low. U2A and U2B are provided to increase the drive of the ZERO output which is designed to drive 1 TTL equivalent load and they also maintain the proper logic sense of the ZERO output. With the output of the U2B low, U2C's output will be high and D₄, the start LED, will be off. The output of U4B will be low so D₃, the stop LED, will be on. The count input to the 7217B is generated by U4A and U4, U5, U6, U7, D₅, and R₉. The 1MHz signal comes

from the master oscillator shown in Figure 2.2. This signal swings from +5V to -5V so D_5 is provided to clip the negative portion and R_9 provides a dc path to ground. U4D buffers this signal so its output is a 1MHz square wave swinging from 0V to +5V. This clock signal is AND'ed with the buffered ZERO output so the output of U4A is logic 0 as long as the ZERO output is low. In this state the count input is disabled and no counting occurs. The output of U4A connects to U7, an RDD104 programmable divider configured as a divide-by-10000. The output of U7 will then be 100Hz. This drives a cascade connection of two 4017's configured individually as divide-by-10's, so from the output of U4A to the output of U5 the circuit provides a divide-by-10 function. The output of U5 drives the count input on the 7217B at 1Hz and acts as the clock input.

When the start switch is pressed, the 7217B is loaded with the data on the thumbwheel switches and ZERO goes high. This enables U4A and its associated divider provides a 1Hz clock input to the 7217B which begins counting down. The output of U2C is low so D_4 , the start LED, is on. As long as the stop switch is not pressed, the output of U2D is high, as is the output of U4B, and the stop LED is off. If the stop switch is pressed, the output of U2D goes low, which resets the 7217B to zero. ZERO goes low, the count input is inhibited, and the circuit remains in this state until the start switch is pressed.

Since the rising edge of the signal ZERO is not synchronized with the rising edge of the 1MHz signal present at the output of U4D, an error of 0.5 μ sec maximum is possible at the output of U4A. For example, if the signal ZERO goes high 50nsec after a trailing edge on the output of U4D, the first rising edge on the count input would occur

approximately 0.5 seconds later. This is because U5, U6, and U7 divide the output of U4A (1MHz) by 10^6 which is the same as multiplying the period of U4A's output by 10^6 or $(0.5\mu\text{sec}) (10^6) = 0.5\text{sec}$. This results in a 30 second error for the full treatment time of 60 minutes. If the time difference between the rising edge of ZERO and the rising edge of the 1MHz output of U4D is assumed to be a normal or gaussian random variable, then the probability of actually observing a 30 second error would be small with an error of 15 seconds being typical.

2.5.3 Safety Circuitry

Safety circuitry is included in the instrument that resets the output current to zero in the event of a power failure or treatment mode change. In the event of a power failure during operation, the dc supplies that power the constant current output amplifiers drop out of regulation causing erratic and uncontrollable output currents which are applied to the patient. Also, the same patient will respond differently to a modulated output current than an unmodulated current. This section describes the analog and digital circuitry that monitors the condition of the power supplies and the treatment mode controls, and resets the instrument in the event of a power failure or operating mode change.

The basic safety circuit functionality can be summarized by assuming the instrument is reset at power-up and the input to the manual gain control is 0V. When a treatment time is loaded, the intensity control must be rotated to the minimum setting at which point the DC REFERENCE in Figure 2.48 is connected to the manual gain control

Y inputs in Figure 2.47 and the instrument is actively producing output current. If, at any time, the treatment mode is changed from modulated to unmodulated or the carrier frequency is changed, the instrument resets the output to zero and the user must reset the intensity control by rotating it to the minimum setting. The user can switch between channel 1 and channel 2 output current displays without resetting the instrument. If the stop switch is pressed, the instrument resets the output current and the treatment timer to zero.

In order to reset the output current to zero in the event of a mode change, and ensure proper logic control of the instrument, the circuitry shown in Figure 2.93 was developed. Referring to Figure 2.93, at power-up, the signal POWER-UP RESET provides a 110msec reset pulse that resets the Q output of the D FLIP-FLOP to logic 0. The signal STOP, is normally logic 0 unless the stop switch is pressed at which time it becomes a logic 1 and resets the flip-flop. The signal ZERO, explained in the preceding section, is logic 0 immediately after power-up and remains logic 0 until the treatment timer is loaded with a valid time. The 4013's set (S) and reset (R) inputs are activated by a high level (logic 1) so ZERO holds the FLIP-FLOP in a reset state until a valid treatment time is loaded. The origin of the signals ZERO and STOP are shown in Figure 2.92. When the treatment timer is loaded, ZERO switches to a logic 1, and as long as the stop switch is not pressed, the reset input (pin 10) of the flip-flop is logic 0. To set the Q output to logic 1, the user must rotate the intensity pot (R_2) to its minimum setting which toggles U1B's output. U1B's output toggles when the DC REFERENCE goes below approximately 50mV. This small threshold insures the DC REFERENCE is small and therefore the

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output current will be small. U1B's output clocks the flip-flop when it toggles and the logic 1 present on the D input is transferred to the Q output. With ZERO at logic 1, this sets the output of U5D to logic 1. This signal, RUN ENABLE in Figure 2.93, connects to pin 9 of the 4053 analog switch shown in Figure 2.91. With RUN ENABLE at logic 1, Z_1 in Figure 2.91 is connected to Z and the DC REFERENCE is passed (now called INTENSET) to the manual intensity control multipliers. This state (RUN ENABLE = logic 1) is shown schematically in Figure 2.47.

To detect treatment mode changes, the circuit composed of R_5 , R_6 , C_1 , C_2 , U6A, U6B, and U3B in Figure 2.93 was developed. The signal CONTROL in Figure 2.89 corresponding to the modulated/unmodulated or 5KHz / 2.5KHz switch groups connects to the signals MOD/UNMOD or 5KHz in Figure 2.93. For example, if the switch group is 5KHz / 2.5KHz, the signal CONTROL in Figure 2.89 connects to the signal 5KHz in Figure 2.93. Likewise, CONTROL for the modulated/unmodulated switch group connects to the signal MOD/UNMOD in Figure 2.93. Any transition, low-to-high or high-to-low, is detected by U6A or U6B and its associated circuitry. For example, if the signal 5KHz makes a low-to-high transition, pin 5 of U6B follows this transition with no delay. The signal at pin 6 of U6B is delayed approximately 100msec (the voltage recognized by U6B as a logic 1) by the low-pass filter formed by R_6 and R_7 . During this transient phase, the input to the 4030 exclusive or gate is 1,0 and its output is logic 1. When C_2 is fully charged (actually when the voltage on C_2 passes the logic 1 input threshold of U6B), the input to U6B is 1,1 and its output will be logic 0. If 5KHz now makes a high-to-low transition, R_6 and C_2 delay the discharge of pin 6 and a pulse is also generated during this

discharge phase. The operation of the MOD/UNMOD detector is identical to that just described. The outputs of these detector's are OR'ed together by U3B. The output of U3B is OR'ed with the remaining reset signals by U3C whose output connects to the reset (R) input of the flip-flop.

The circuitry in Figure 2.93 controls the safety related functions of mode changes and power-up initialization but does not monitor the power supply. The circuit shown in Figure 2.94 was designed to monitor the power supply and switch off the relay that connects the outputs of the LM1875 power amps and the transformer primary's in the event of a power failure. The basic idea behind the circuit in Figure 2.94 is to compare a lightly filtered voltage, that decays rapidly, to a heavily filtered voltage, that remains longer than the lightly filtered voltage, after a power interruption. Referring to Figure 2.94, the anodes of D_1 and D_2 are connected to the secondary of the low-voltage isolation transformer, which has a center-tapped secondary and is modeled as VAC1 and VAC2 in the figure. SW1 is used to model the power-on switch of the instrument. With SW1 closed, D_1 and D_2 rectify the ac voltage which is filtered by R_1 and C_1 . The dc level at node 4 (top of C_1) is approximately 8V dc with 4Vp-p ripple. R_2 , R_3 , and C_2 form a filtered voltage divider that reduces this to approximately 2.3V dc with 40mVp-p ripple at the inverting input to U1A (node 5). The approximate time constants of nodes 4 and 5 are 5.6msec and 39msec respectively, neglecting R_2 and D_3 . If SW1 is now opened, C_1 will rapidly discharge into R_1 . When the voltage at node 4 reaches a level approximately 0.6V below the voltage at node 5, D_3 begins to conduct, which effectively reduces the time constant at node 5 to R_1C_2 or approximately 560 μ sec. D_3 therefore reduces the time

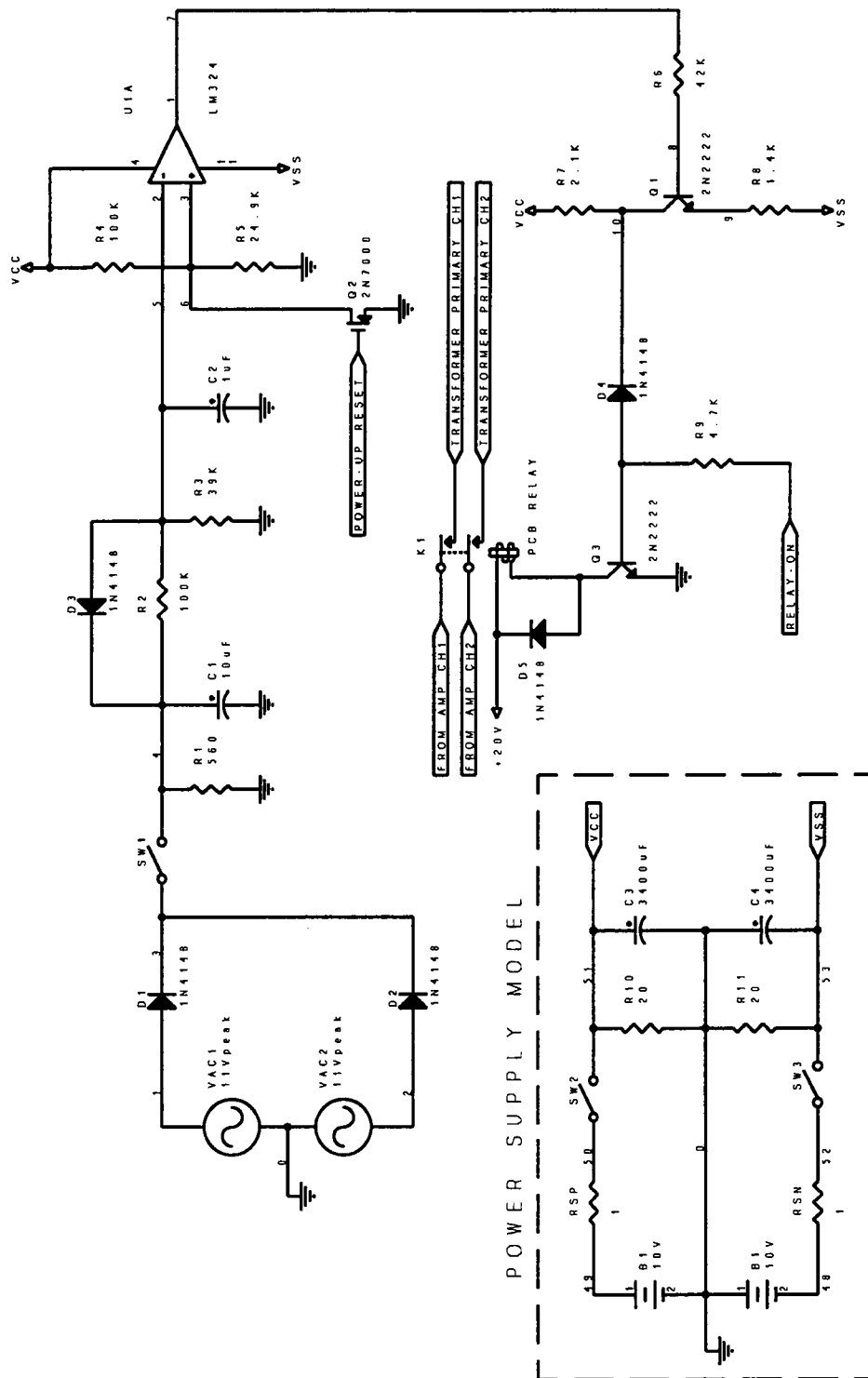


Figure 2.94. Power failure detection circuit.

required to discharge C_2 by bypassing R_2 .

The voltage divider formed by R_4 and R_5 sets the voltage at the noninverting input of U1A (which is configured as a comparator) to approximately 2.0V dc. The voltages V_{CC} and V_{SS} come from the unregulated logic power supply which are very heavily filtered and are approximately ± 10 V dc. Under normal instrument operation, the regulated ± 5 V supplies, which use V_{CC} and V_{SS} in Figure 2.94 as unregulated inputs, draw approximately ± 0.5 A. These unregulated supplies have 3400 μ F of filter capacitance each. An equivalent load of 20 Ω per supply is required which results in an equivalent time constant of 68msec for the ± 10 V dc unregulated supplies. To model these unregulated supplies, the circuitry shown in Figure 2.94 in the box POWER SUPPLY MODEL was used. R_{10} and R_{11} draw load currents equivalent to the actual instrument and SW2 and SW3 model the instrument power switch. Under normal operation, the inverting input of U1A is at approximately 2.3V dc, the noninverting input is at 2.0V dc, and the output (node 7) of U1A is at the negative saturation level for the LM324 which is V_{SS} [16] or -1.0V dc. When SW1 is opened (SW2 and SW3 also open at the same time) and node 5 discharges past the voltage on the noninverting input of U1A, its output (node 7) switches to positive saturation which is $V_{CC}-1.5$ V [16] or 8.5V dc. The timing relationship between nodes 4, 5, and 6 in Figure 2.94 is shown in Figure 2.95. This figure shows the circuit response to closure of SW1, SW2, and SW3 at 20msec and opening of the same switches at 500msec. Note how quickly node 5 decays with respect to node 6. Figure 2.96 shows the relationship between the output, and inverting and noninverting inputs to U1A. The model used for the LM324 (U1A) is one supplied by National Semiconductor Corporation

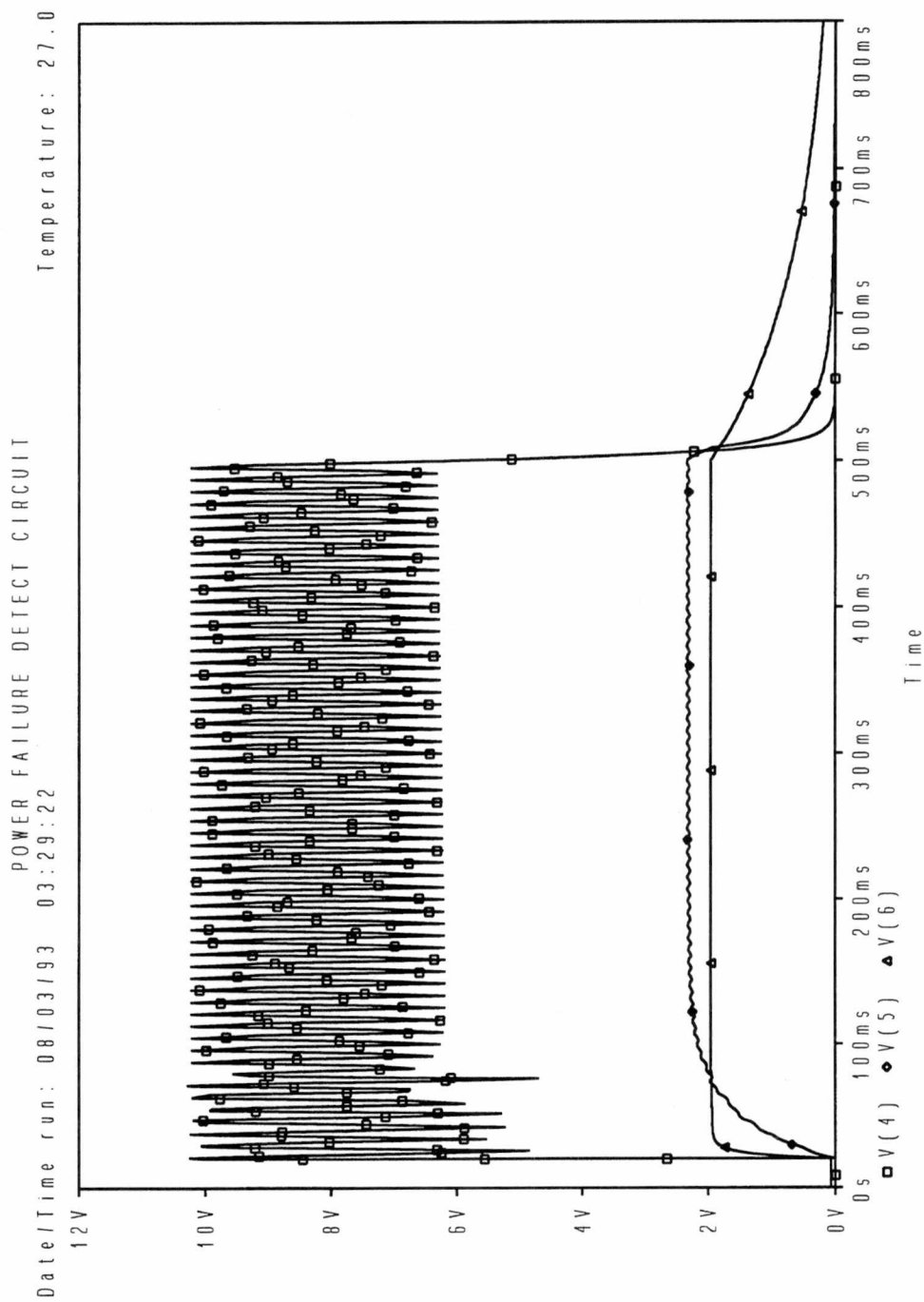


Figure 2.95. Power detect passive timing.

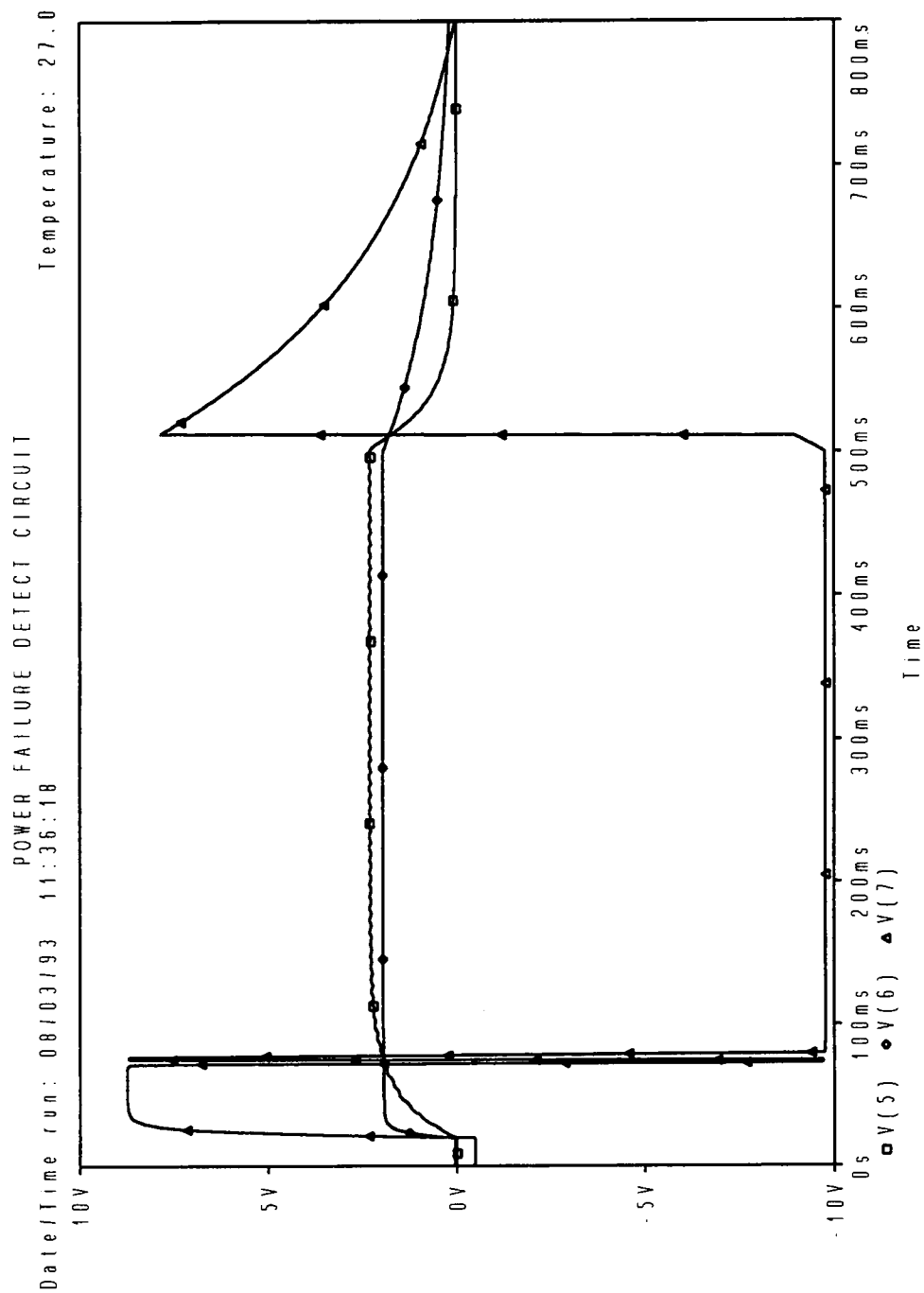


Figure 2.96. Power detect active timing.

for use with their parts and a complete description, along with the PSPICE source files used to generate the response curves in this section, can be found in Appendix E. The output (node 7) of U1A in Figure 2.94 drives the base of an NPN (Q_1) transistor configured as a common emitter amplifier. The collector of this amplifier drives the cathode of D_4 to approximately -1.5V when the output of U1A goes high. With its cathode at -1.5V, the anode of D_3 will be -0.8V so Q_3 , the drive transistor for K1, will have its base-emitter junction reverse biased and the relay shuts off, regardless of the voltage present on the signal RELAY-ON, which is a 0V to +5V logic level and is derived as shown in Figure 2.92. As long as U1A's output is low, Q_1 will be off, its collector will be high, and D_4 will be reverse biased. This allows RELAY-ON to control Q_3 as long as the incoming power is good. Figure 2.97 is a plot of the collector voltage of Q_1 during the power-up/power-down sequence.

At power-on, the voltage at the noninverting input of U1A in Figure 2.94 rises faster than the voltage on its inverting input. This can be seen in Figure 2.95 where V(5) in this figure is node 5 voltage in Figure 2.94. This causes the output of U1A to saturate high until V(5) becomes larger than V(6). Also, at approximately 80msec in Figures 2.95 and 2.96, the ripple on V(5) causes the output of U1A to oscillate at the crossover of V(5) and V(6). This noise also appears at the collector of Q_1 as shown in Figure 2.97. After approximately 80msec this transient settles out to a steady state until power is lost. To prevent this uncontrolled transient, Q_2 , an enhancement-mode MOSFET, was added to the noninverting input of U1A in Figure 2.94. The gate of Q_2 is driven by the signal POWER-UP RESET shown in Figure 2.90. This signal is a logic 1 (+5V) for

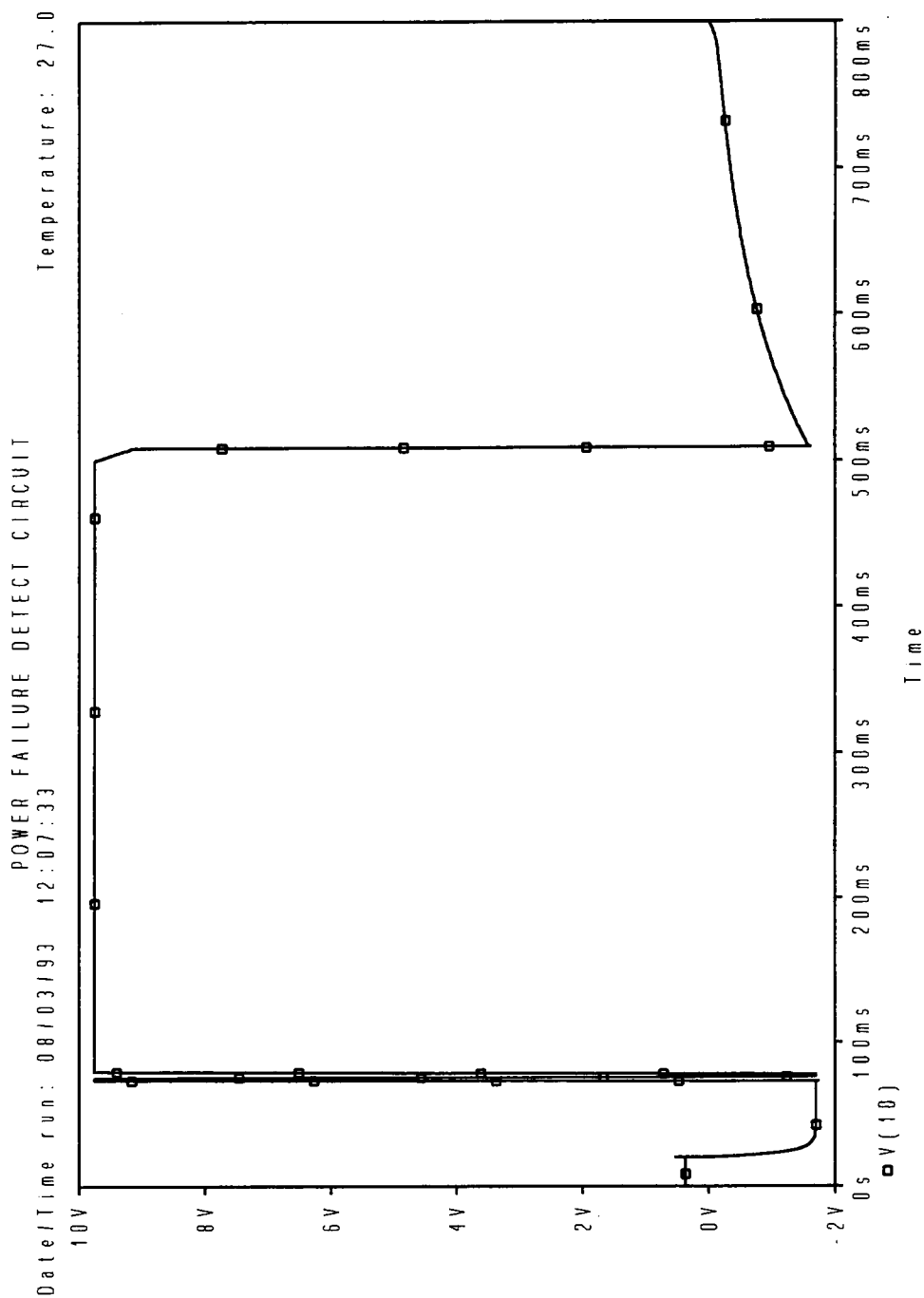


Figure 2.97. Collector voltage of Q_1 .

approximately 110msec after power-on at which time it switches to logic 0 (0V). With a gate-to-source voltage of +5V, Q_2 acts as a closed switch between node 6 and ground, and therefore holds node 6 low for 110msec. This allows node 5 to stabilize at 2.3V and thus prevents the transients shown in Figures 2.96 and 2.97. The results of the addition of this delay are shown in Figures 2.98 and 2.99. It should be noted that Q_2 was not actually used in the PSPICE simulation. The action of Q_2 was modeled as a switch between the noninverting input of U1A and R_4 in Figure 2.94. This switch was held in an open state for 100msec then closed for all time thereafter. This allows R_5 to hold the voltage at node 6 near ground until the switch closes. The PSPICE source file used for these simulations is shown in Appendix E.

2.5.4 Measurement Conversion and Display

Section 2.4.4 described circuitry that measures the actual output current on each channel of the instrument and provides a dc voltage proportional to the rms value of these currents. The circuit in Figure 2.100 was developed to convert and display these dc voltages.

The circuit is based on the ICL7107 which is a dual-slope integrating analog-to-digital converter designed to interface directly to a 3 1/2 digit LED display. Also, included in this IC is an auto-zero circuit that keeps the input referred offset voltage under $10\mu\text{V}$. When the ICL7107 is connected to a 3 1/2 digit display (4, seven-segment LED's), the count displayed is

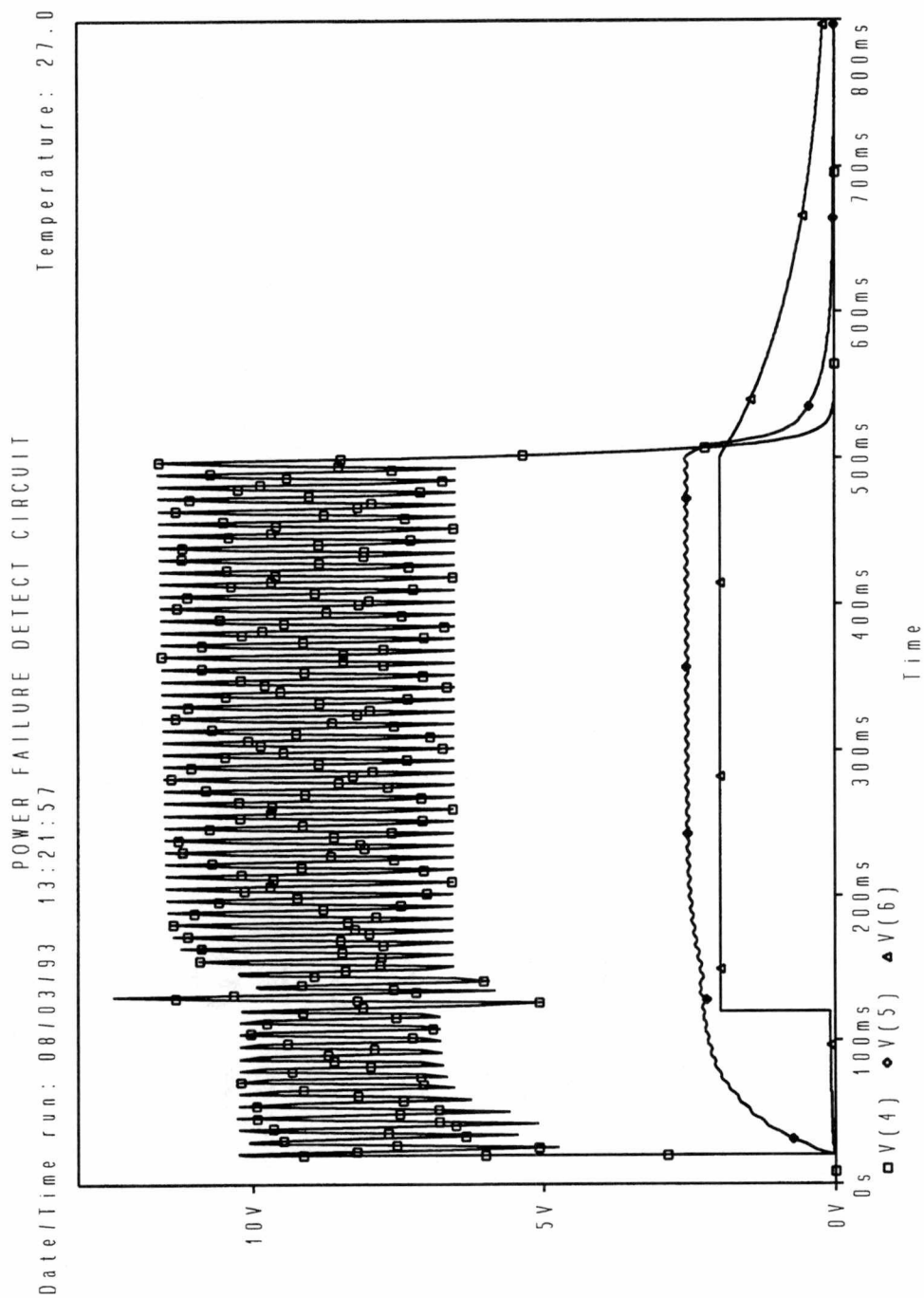


Figure 2.98. Power detect passive timing with delay.

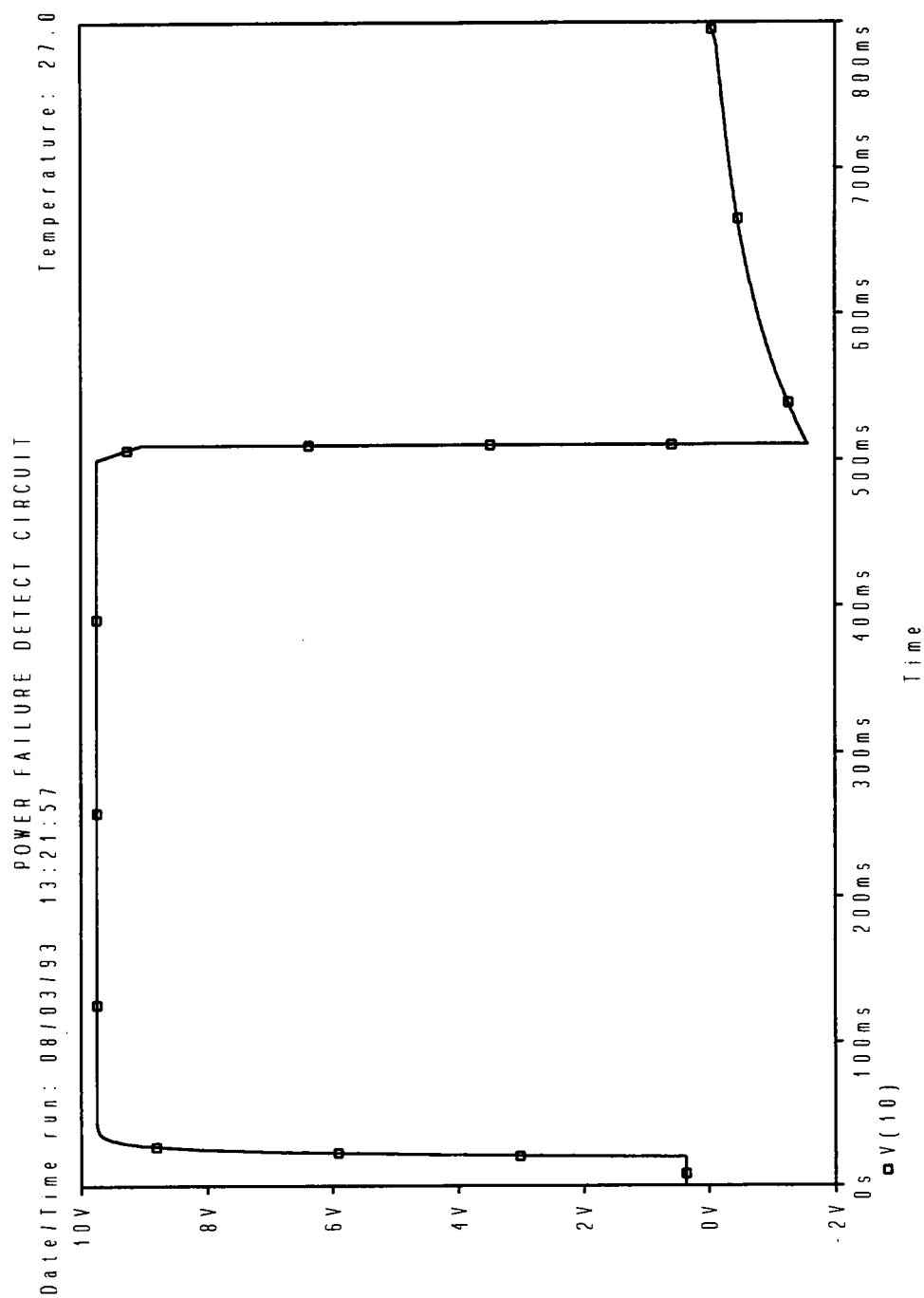


Figure 2.99. Power detect comparator timing with delay.

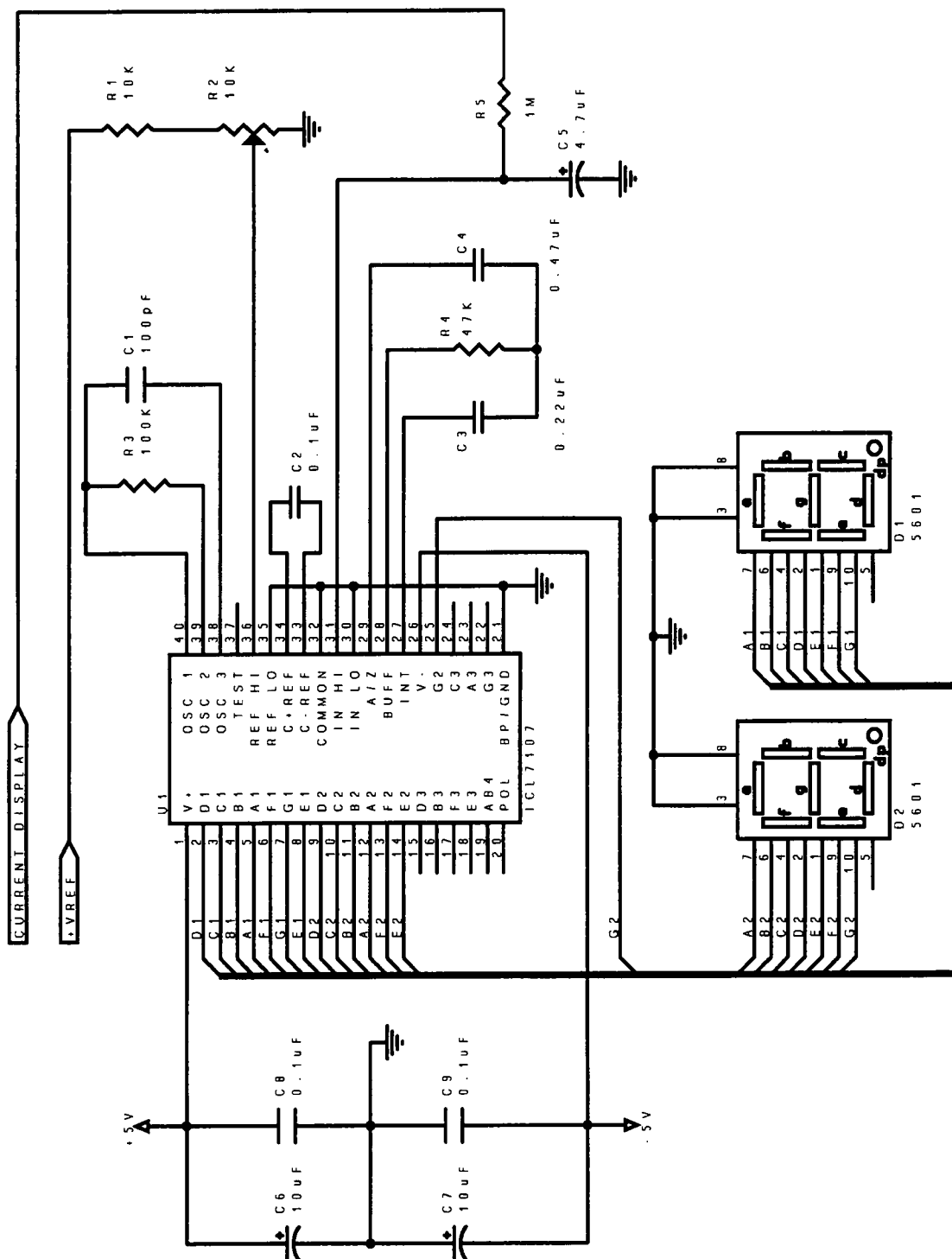


Figure 2.100. Measurement conversion and display.

$$\text{Digital count} = 1000 \left(\frac{V_{\text{input}}}{V_{\text{ref}}} \right) \quad \text{Eq. 2.65}$$

but only two LED's, units (D1) and tens (D2), are used in Figure 2.100. This changes the count displayed to

$$\text{Digital count} = 100 \left(\frac{V_{\text{input}}}{V_{\text{ref}}} \right) \quad \text{Eq. 2.66}$$

where $V_{\text{input}} = \text{CURRENT DISPLAY} = 200\text{mV}$ dc as described in section 2.4.4 and V_{ref} is the dc voltage present on pin 36 (REF HI) of the ICL7107. In order to provide a full-scale digital count of 50 with $V_{\text{input}} = 200\text{mV}$, V_{ref} in Equation 2.66 is set to 400mV . This is accomplished in the circuit of Figure 2.100 by adjusting R_2 until pin 36 (REF HI) is at 400mV with respect to pin 32 (COMMON). The signal $+V_{\text{REF}}$ in Figure 2.100 is $+2.5\text{V}$ and its generation was explained in section 2.2.2. Calibrated in this manner, a count of 50 on the display corresponds to an input voltage of $V_{\text{input}} = 200\text{mV}$ so the conversion precision is

$$\frac{50 \text{ counts}}{200 \text{ mV}} = \frac{1 \text{ count}}{4 \text{ mV}} \quad \text{Eq. 2.67}$$

or 1 count/mA rms of output current. The error analysis of the RMS-to-DC measurement circuitry in section 2.4.4 showed an error of 4mV which is identical to the resolution of the circuit in Figure 2.100. This is also the reason the output current display is limited to

two digit's as it would make no sense to provide a display with more significant digits than the measurement circuitry is capable of providing.

The values of the components C_1 through C_4 and R_3 through R_5 in Figure 2.100 are the values suggested by the manufacturer for a 200mV full-scale input and three conversions per second. The only value that deviates from the manufacturer's suggestions is that for C_5 , whose value of 4.7 μ f was determined experimentally to allow the display to return to a count of 00 from a full-scale count of 50 in approximately 1 second. A complete description of the ICL7107 can be found in the Intersil Component Data Catalog, 1987 on pages 2-1 through 2-12.

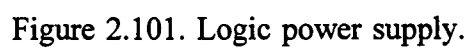
2.5.5 Instrument Power Supplies

To minimize noise, loading effects, and errors caused by ground currents, the instrument uses three separate dc power supplies. All three supplies are mounted on one single-sided printed circuit board, the layout of which is shown in Appendix F. The outputs of these supplies are routed to the various circuit boards as needed with wiring harnesses. The ground layout is a star configuration with all ground leads returned to the same point on the power supply circuit board. This minimizes errors by allowing the large nonlinear ground currents produced by the output amplifiers to bypass the sensitive analog ground return paths. All three supplies utilize linear IC regulators in TO-220 packages which are mounted to a large, finned aluminum heat sink.

Figure 2.101 shows the $\pm 5\text{V}$ logic power supply that powers the signal generation logic. This supply draws $\pm 0.5\text{A}$ during operation of the instrument so the regulators U1 and U2 must dissipate $(10\text{V}-5\text{V})(0.5\text{A}) = 2.5\text{W}$ per regulator. These regulators are rated at a maximum dissipation capability of 20W when mounted on an infinite heat sink so 2.5W is well within the capabilities of these devices.

Figure 2.102 shows the $\pm 15\text{V}$ analog supplies and the $\pm 20\text{V}$ output power amplifier supplies. U1 (LM317T) and U2 (LM337T) are the positive and negative regulators used to provide regulated power to the constant current output amplifiers. With the values shown [17], the adjustment range of these regulators are $\pm 16.5\text{V}$ to $\pm 22.0\text{V}$. With the instrument producing an output current of 50mA rms , the current drawn by U1 and U2 in Figure 2.102 is $\pm 0.65\text{A}$. They both are rated at 1.5A maximum before internal current limiting circuitry shuts each down. At 0.65A , each must dissipate $(28\text{V}-20\text{V})(0.65\text{A}) = 5.2\text{W}$. Both are rated at 15W so 5.2W , which is well within the 15W rating. U3 and U4 provide $+15\text{V}$ and -15V respectively to the analog circuitry. They are each rated at an output current of 1A and a power dissipation of 20W . During instrument operation, they each draw 0.2A so each must dissipate 2.6W which is within rated capabilities. The diodes in Figures 2.101 and 2.102 protect the IC regulators in the event that a voltage is applied to the output pin with the power off.

The regulators in Figure 2.101 and 2.102 are all mounted on an extruded aluminum heat sink that is approximately 4 inches long by 3 inches high with 7 fins 3 inches high that extend $1\frac{3}{4}$ inches from the back surface of the heat sink. The total power dissipation of the regulators is $(2.5\text{W})(2) + (5.2\text{W})(2) + (2.6\text{W})2$ or 20.6W . At an



ambient temperature of 23 °C, the instrument was operated at a full-load output current of 50mA rms/channel for 60 minutes which resulted in regulator tab temperatures of 40 °C. This is an increase of 17 °C so the heat sink has a thermal resistance of $17\text{ °C} / 20.6\text{W} = 0.825\text{ °C/W}$. As an example, the LM317T regulator in Figure 2.102 has a junction to case thermal resistance of 12 °C/W in a TO-220 plastic package. The case to ambient thermal resistance is 0.825 °C/W so the junction to ambient thermal resistance is 12.825 °C/W. At a maximum dissipation of 5.2W, the junction temperature will be $(12.825\text{ °C/W})(5.2\text{W}) = 66.69\text{ °C}$ above ambient. With an ambient temperature of 23 °C the junction temperature will be 89.69 °C. Since the maximum rated operating temperature of the instrument is 35 °C, the junction temperature will be $35\text{ °C} + 66.69\text{ °C} = 101.79\text{ °C}$ at this ambient temperature. The LM317T is rated for a maximum junction temperature of 150 °C so the device has room to spare even at this elevated temperature. Similar calculations performed on the remaining regulators show smaller junction temperature rise due to the smaller power dissipation.

2.6 Operation Summary

Any prospective user of the instrument described in this thesis should be warned that this instrument is capable of producing current levels that can result in harm or fatality of a patient if used incorrectly. Under no circumstances should the instrument be used to treat the thoracic or cranial regions of a human patient. It should not be used in a location where diathermy equipment is in use, or in a very humid or wet environment.

The instrument should be operated only by a licensed medical doctor or physical therapist experienced in the use of electrical apparatus designed for use on human patients.

The instrument line cord is a standard three conductor cable that mates to a male receptacle on the rear panel of the instrument. This line cord is plugged into a standard 120VAC, 60Hz power line receptacle. Before turning on the instrument power, the electrodes should be connected to the appropriate connectors located on the front panel of the instrument. With the electrodes connected to the instrument, the power switch to the instrument can be switched to the ON position. The user should wait at least five minutes after power has been applied before starting treatment to allow the circuitry to stabilize.

The electrodes are rubber-coated circular aluminum disks three inches in diameter that are attached to the ends of a six to eight foot dual conductor cable. The surface that will contact the patient should be cleaned with isopropyl alcohol then moistened with a clean damp sponge. These electrodes are attached to the area to be treated as shown in Figure 1.1 and held in place by nylatex strap. This strap should be tight enough that no movement of the electrodes can occur but not tight enough to cause patient discomfort. Correct placement and restraint of the electrodes is very important because if the electrodes were to be removed during treatment, the contact area will decrease during the removal and since the instrument is designed to deliver a constant current, the current density in the electrode will increase, resulting in a stinging sensation and patient harm.

With the electrodes correctly attached to the patient, the desired treatment time is selected by the thumbwheel switches on the front panel of the instrument. Although

circuitry in the instrument prevents any output current irrespective of the intensity setting when the start switch is pressed, it is a good idea to rotate the intensity control to its minimum position before pressing the start switch. This will prevent harm to the patient in the event the safety circuitry is not functioning properly. Before pressing the start switch, the desired carrier frequency and modulation mode should be selected by pressing the appropriate switches. At power-up, the selected modulation mode is unmodulated, the carrier frequency is 5KHz, and channel 1 is selected for the output current display. The user can now press the start switch, rotate the intensity control slightly clockwise, then counterclockwise to the minimum position to reset the safety circuitry. The intensity control is now active and the output current will track the setting of the intensity control. The actual output current is displayed in milliamperes on the two digit LED display in the upper left hand corner of the front panel.

The beat frequency is set by rotating the beat frequency control to the desired position where a full counterclockwise setting corresponds to a beat frequency of 1Hz and a full clockwise setting corresponds to a beat frequency of 200Hz. The beat frequency should be adjusted to the desired setting after the output current is set to the required amplitude.

CHAPTER 3

RESULTS

In order to evaluate the design of the instrument outlined in this thesis, a working prototype was developed. This prototype consisted of four circuit boards housed in a NEMA rackmount enclosure. A single-sided printed circuit board was designed for both the power supply and output power amplifier assemblies. This was necessary due to the large currents associated with these circuits and for physical reasons due to the large heatsinks required for the voltage regulators and power amplifiers. The oscillator, filtering, and gain control circuitry were built on a separate circuit board using wire-wrap techniques. All control logic, displays, and user controls were also built on a separate circuit board using wire-wrap techniques. Power to the separate boards was supplied using 18 a.w.g. wiring harnesses and signals are transferred between boards with ribbon cable.

Before discussing the results of testing the instrument prototype, the conditions under which the instrument was tested should be stated. To simulate a patient load, each output was loaded with a 250Ω , 5W ceramic resistor. With the instrument set to the unmodulated mode, the full-scale output of each channel was then calibrated to 50mA rms which was measured using a TDS 420 Tektronix digitizing oscilloscope with a Tektronix P6021 ac current probe. With the full-scale output current calibrated, the gain of the respective channel measurement circuitry was adjusted until the output current display read 50. The modulated treatment mode was then selected and the gain of the summer circuit in Figure 2.49 was adjusted until the output current display read 35. The ambient

temperature at which this calibration was performed was 24 °C.

After calibration, the instrument was operated for 60 minutes at a full-scale output current of 50mA rms and a carrier frequency of 5KHz and 2.5KHz (60 minutes at each carrier frequency) in the unmodulated treatment mode. This test was repeated for both carrier frequencies in the modulated treatment mode. During each phase of this test the output voltage and current of each channel was observed using a Tektronix TDS 420 oscilloscope and the temperature of the power supply and power amplifier heatsinks were monitored using a Simpson model 758 temperature probe. Observation of the output waveforms revealed a low frequency amplitude modulation (distortion) of the output current on both channels in the unmodulated treatment mode. This distortion modulated the amplitude of the output currents by $\pm 10\%$ at a full-scale output current of 50mA rms and the frequency of the modulation was found to correspond to the beat frequency setting. At lower output current levels this distortion was proportionately smaller, with an output current of 50mA rms producing the largest distortion. The fact that the frequency of the modulation corresponded to the beat frequency setting and the amplitude of the modulation increased at larger output current levels suggested a board layout problem on the power amplifier assembly. To verify this assumption, one power amplifier was disabled while the other was operated at full-scale. The result was a clean sine wave that was not affected by either the beat frequency or current amplitude settings. This result suggests that the printed circuit layout for the amplifier board shown in Appendix B requires a larger ground plane to reduce this distortion to acceptable levels. Although the amplitude of the distortion is large ($\pm 10\%$) at full-scale, the fact that its frequency tracks

the beat frequency setting would render it imperceptible to the patient.

The final temperature of the power supply heatsink, measured between the tabs of the $\pm 20\text{V}$ regulators (highest dissipation) after four hours of continuous operation at full-scale output, was 40°C . This temperature is well within the temperature range of all regulators used and was acceptable. The temperature of the power amplifier heatsink was measured at 120°C after four hours of continuous operation at full-scale. This large temperature increase was unacceptable and the addition of forced air cooling was required. A series of louvers were cut into the bottom panel of the instrument directly under the power amplifier heatsink fins and a small cooling fan was installed above the heatsink which provided forced air across the heatsink. After the addition of the fan, the instrument was operated at full-scale output for four hours and the final temperature of the power amplifier heatsink was measured at 60°C which was found to be acceptable. No other problems were encountered during the operation of the instrument with all circuitry performing as expected.

In order to provide a better understanding of the output capability of the instrument, measures other than rms current are useful. One such measure is the maximum output power the instrument is capable of delivering and another is the amount of charge per half-cycle of the output waveform. The amount of charge stored in the tissues approaches zero for a symmetrical bipolar waveform such as the sinusoids produced by this instrument as long as the treatment time is much longer than the period of the waveform so a measurement of output capability in terms of charge is not as useful for this instrument as it would be for an instrument that produces a unipolar waveform.

Assuming a 250Ω resistive load, at full-scale the average power delivered per channel is I^2R or $(50\text{mA rms})^2 \times 250\Omega = 0.625\text{W}$ so the total output power delivered by both channels is $P_{\text{Total}} = 1.25\text{W}$. To determine the charge stored per half-cycle it is necessary to represent the output current waveform as

$$i(t) = A_m \sin(\omega t) \quad \text{Eq. 3.1}$$

where A_m is the peak amplitude of the sinusoid and ω is the frequency in rads/s. The charge stored per half-cycle can now be found as

$$Q_{\text{half-cycle}} = \int_0^{\frac{T}{2}} i(t) dt \quad \text{Eq. 3.2}$$

where $i(t)$ is given by equation 3.1 and T is the period of the sinusoid. Solving equation 3.2 using $i(t)$ in equation 3.1 results in

$$Q_{\text{half-cycle}} = \frac{A_m}{\omega} - \frac{A_m \cos\left(\frac{\omega T}{2}\right)}{\omega} \quad \text{Eq. 3.3}$$

where $A_m = 70.711\text{mA}$ (50mA rms) and $\omega = 2\pi f$. At 5KHz the charge stored per half-cycle is therefore $Q_{5\text{KHz}} = 4.5\mu\text{Coulomb}$. From symmetry the charge stored per half-cycle at a carrier frequency of 2.5KHz is $Q_{2.5\text{KHz}} = 2Q_{5\text{KHz}} = 9.0\mu\text{Coulomb}$.

3.1 Instrument Waveforms

In order to verify instrument operation during treatment, the output waveforms produced in both the modulated and unmodulated treatment modes at both carrier frequencies are shown in this section. The measurements are separated into two categories, (1) steady state response and (2) transient response. Steady state response is defined here as the response of the instrument during continuous operation at particular mode/carrier frequency, with no control that would result in reset of the instrument being operated during the measurement. Transient response is defined as the response of the output waveforms (instrument safety circuitry) to a change in treatment mode, carrier frequency, or loss of line power during continuous operation.

The measurements shown in this section were performed using a Tektronix TDS 420 digital oscilloscope with a standard 10:1 voltage probe for voltage measurements and a P6021 current probe at a scale factor of 2mA/mV for the current measurements. Each output channel of the instrument was loaded with a 250 Ω resistor and calibrated at 50mA rms per channel to simulate a patient load. The measurements were performed with the instrument producing a full-scale output current of 50mA rms per channel. Table 3.1 shows the relationship between the following figures and the treatment mode/carrier frequencies for continuous operation. Table 3.2 shows the same relationships for the transient response measurements.

Table 3.1**Continuous Measurements**

Figure	Carrier Frequency	Treatment Mode	Beat Frequency	Instrument Channel
3.1	2.5KHz	Unmodulated	NA	1
3.2	5.0KHz	Unmodulated	NA	1
3.3	2.3KHz	Unmodulated	200Hz	2
3.4	4.8KHz	Unmodulated	200Hz	2
3.5	2.5KHz	Modulated	200Hz	1, 2
3.6	5.0KHz	Modulated	200Hz	1, 2

Table 3.2**Transient Measurements**

Figure	Carrier Frequency	Treatment Mode	Beat Frequency	Instrument Channel	Reset Cause
3.7	2.5KHz	Unmodulated	NA	1	Mode
3.8	5.0KHz	Unmodulated	200Hz	2	Carrier Frequency
3.9	2.5KHz	Modulated	200Hz	1	Mode
3.10	5.0KHz	Modulated	200Hz	2	Carrier Frequency
3.11	2.5KHz	Unmodulated	NA	1	Power Supply
3.12	5.0KHz	Modulated	NA	2	Power Supply

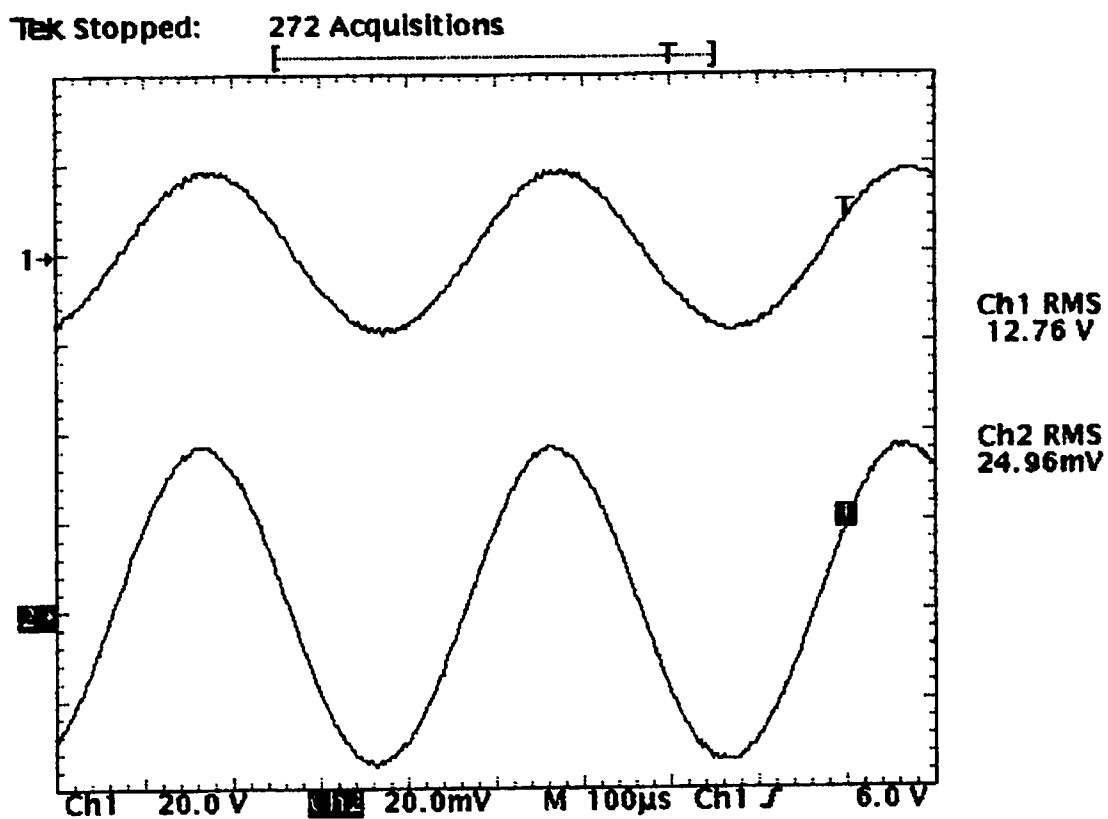


Figure 3.1. Channel 1 output voltage and current, unmodulated, 2.5KHz.

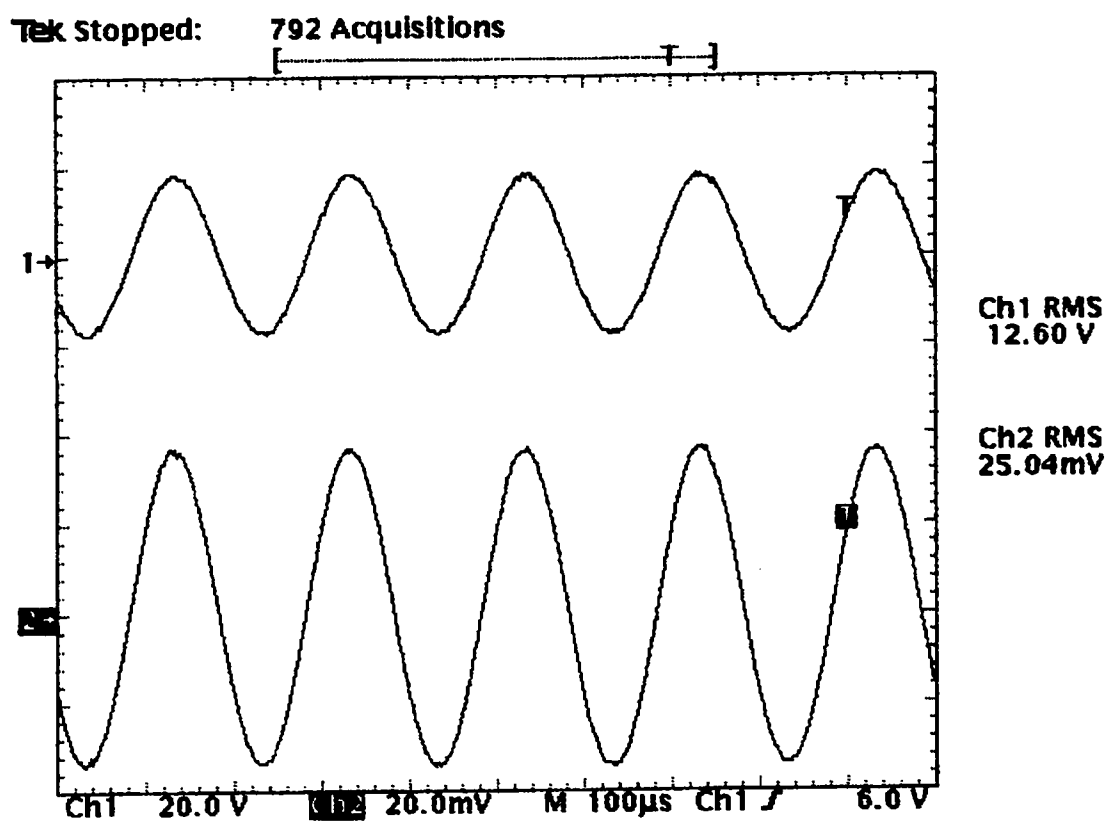


Figure 3.2. Channel 1 output voltage and current, unmodulated, 5.0KHz.

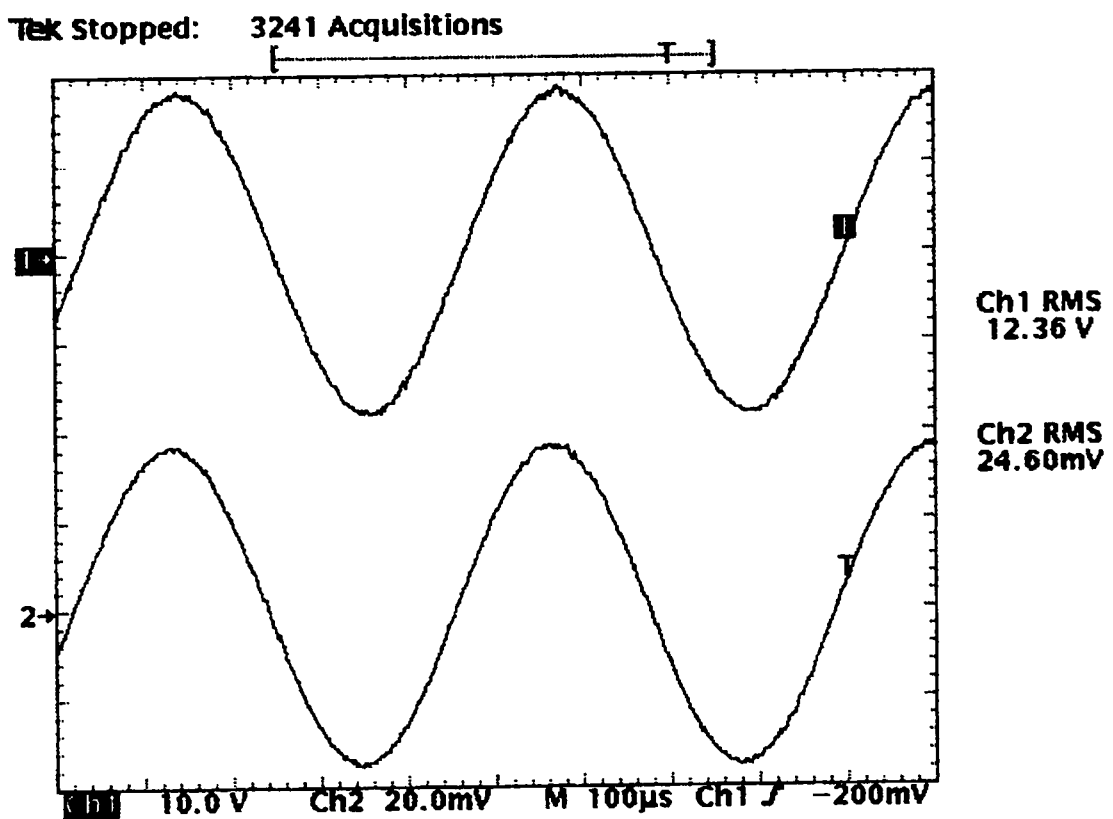


Figure 3.3. Channel 2 output voltage and current, unmodulated, 2.3KHz.

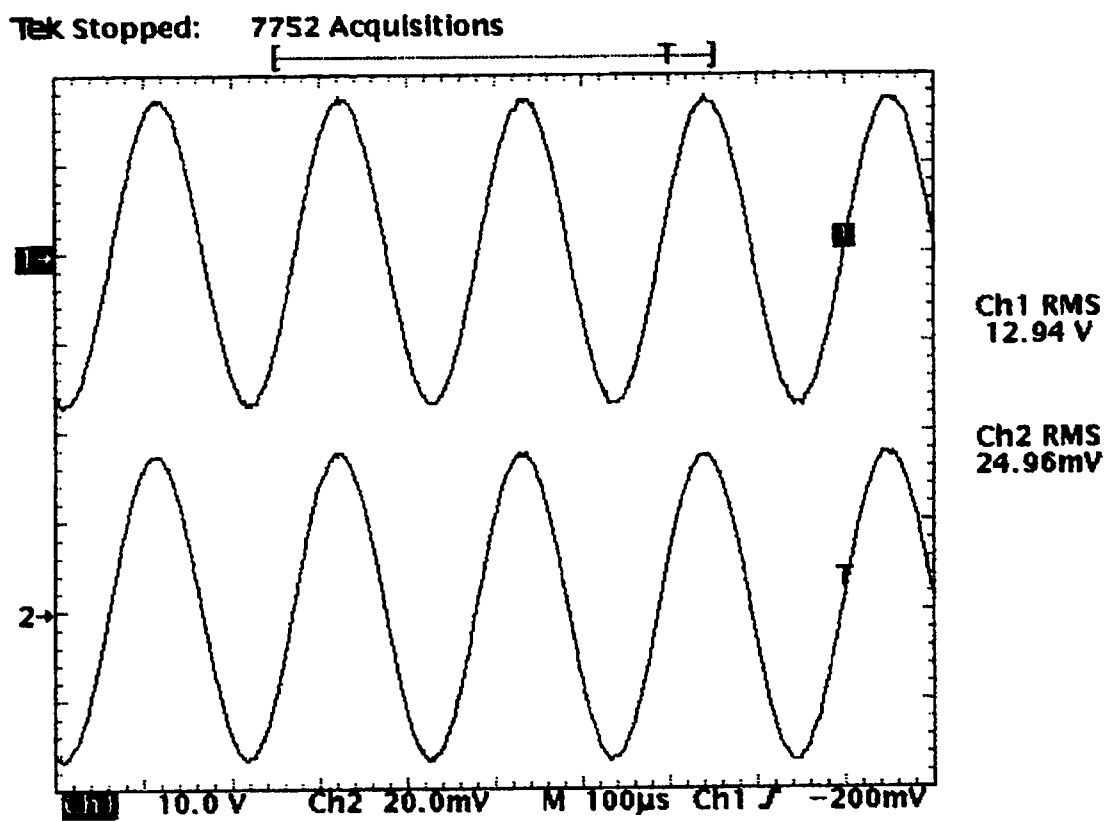


Figure 3.4. Channel 2 output voltage and current, unmodulated, 4.8KHz.

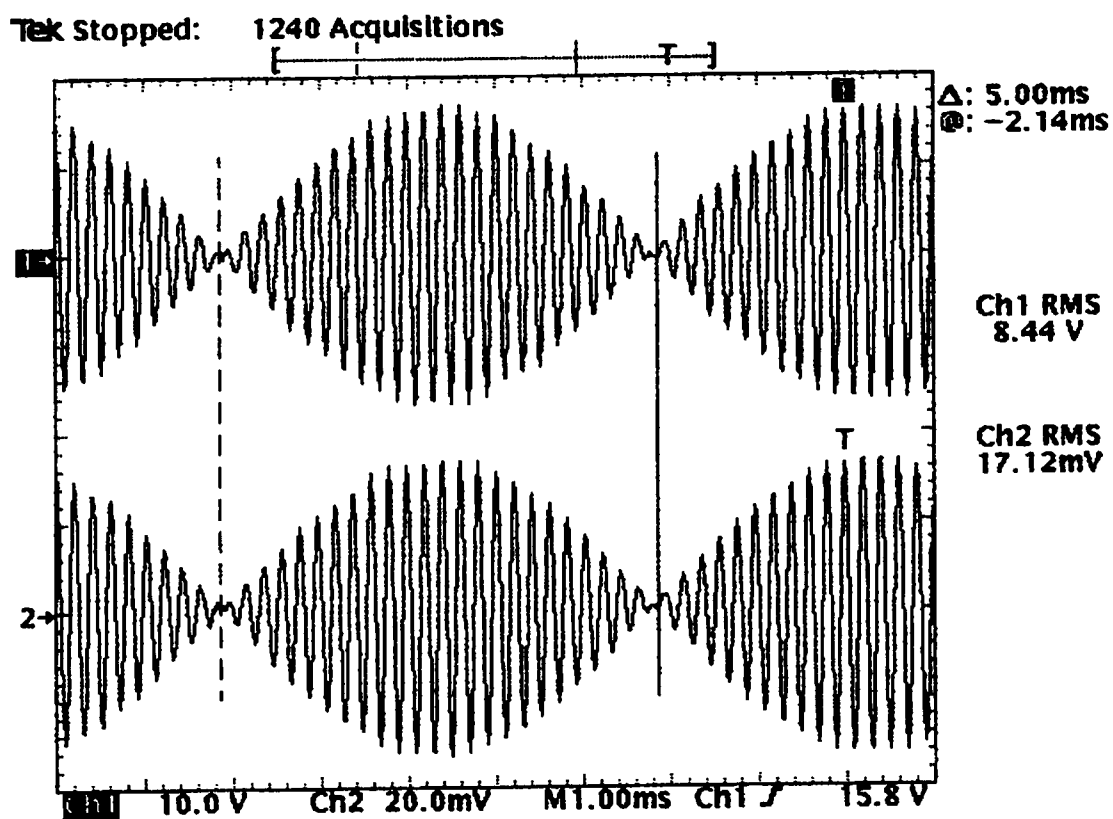


Figure 3.6. Channel 2 output voltage and current, modulated, 5.0KHz.

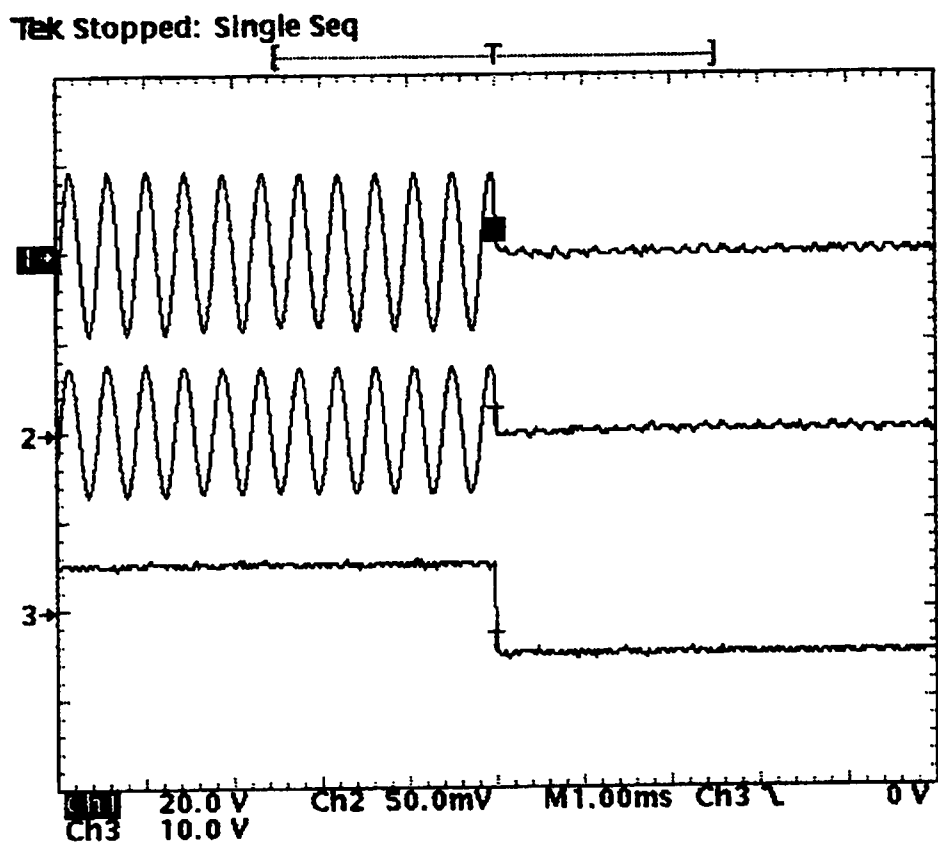


Figure 3.7. Transient response to treatment mode change, unmodulated, 2.5KHz.

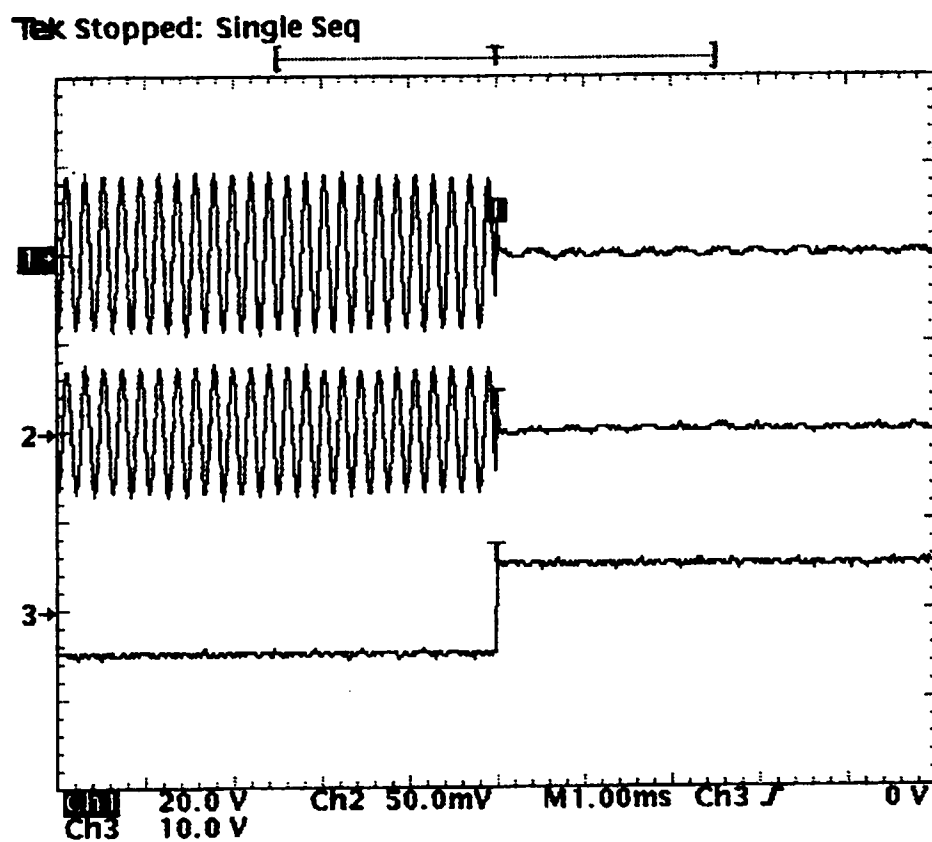


Figure 3.8. Transient response to carrier frequency change, unmodulated, 5.0KHz.

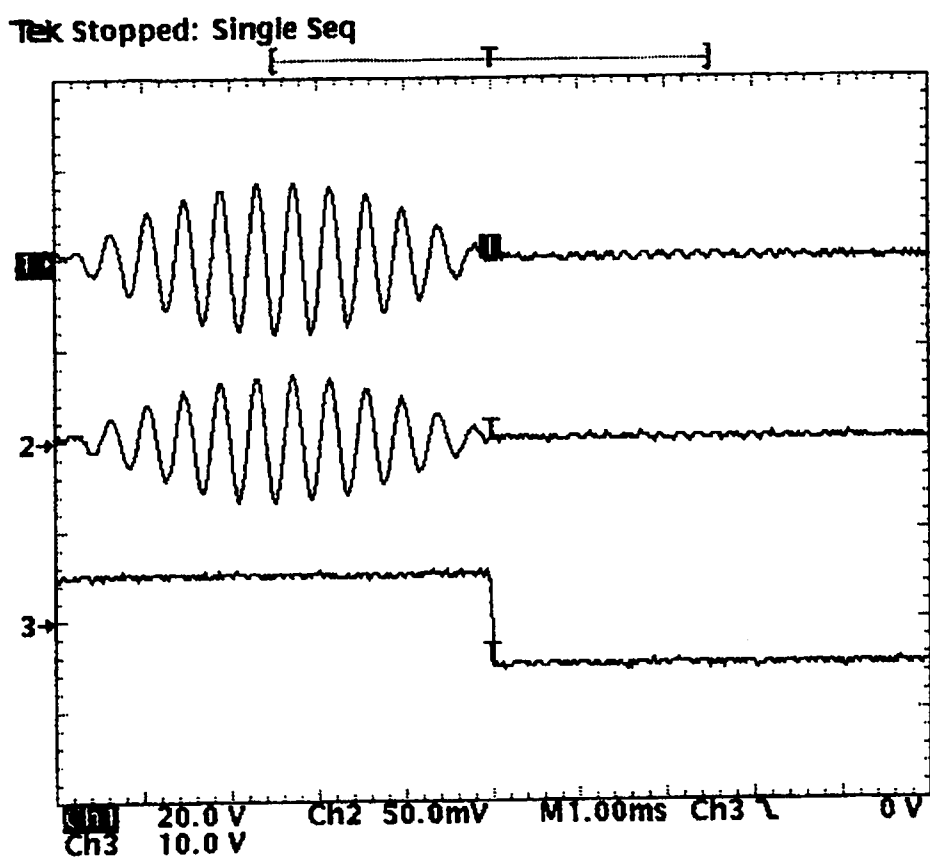


Figure 3.9. Transient response to treatment mode change, modulated, 2.5KHz.

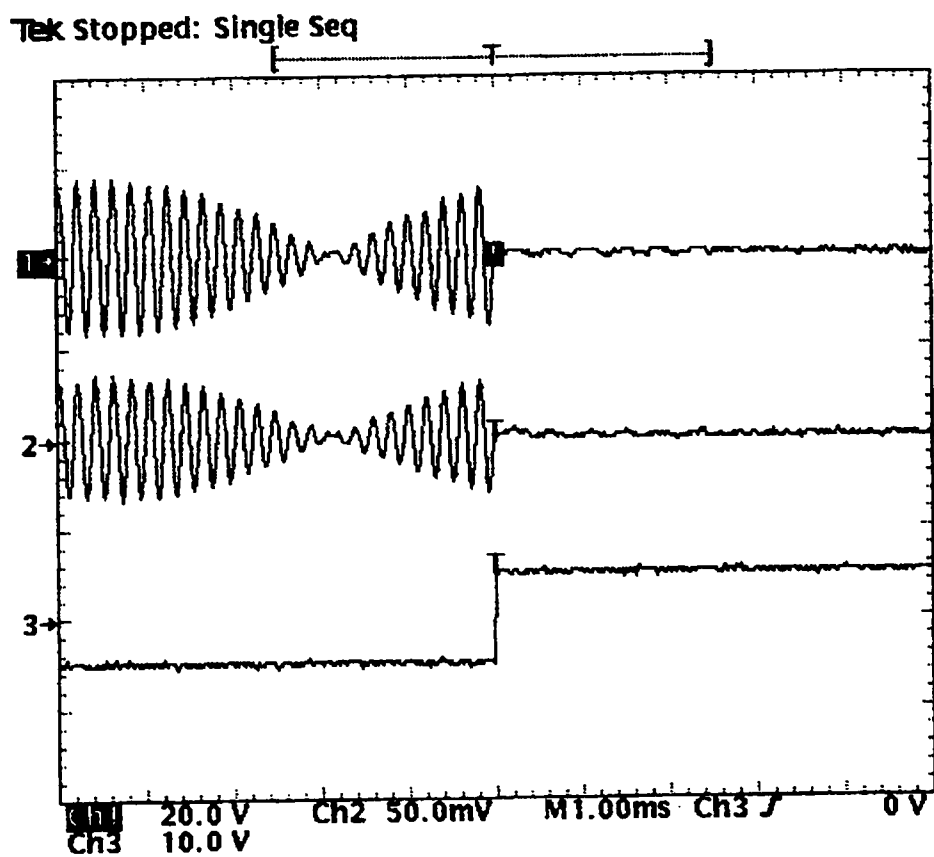


Figure 3.10. Transient response to carrier frequency change, modulated, 5.0KHz.

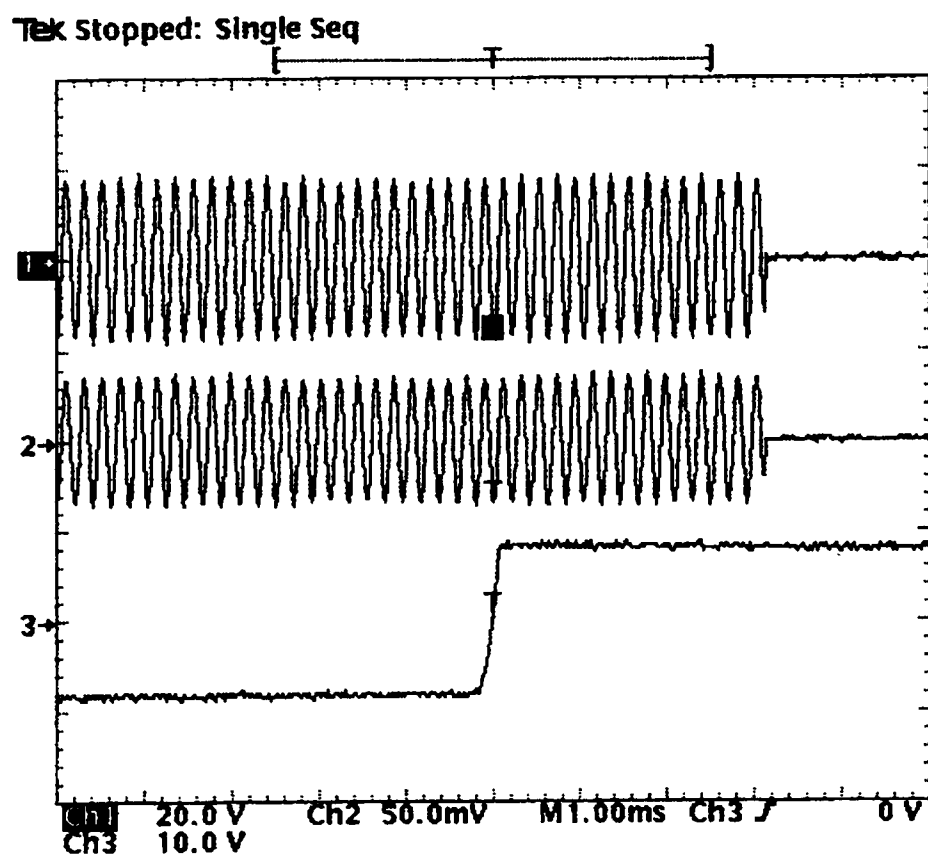


Figure 3.11. Transient response to power supply failure, unmodulated, 5.0KHz.

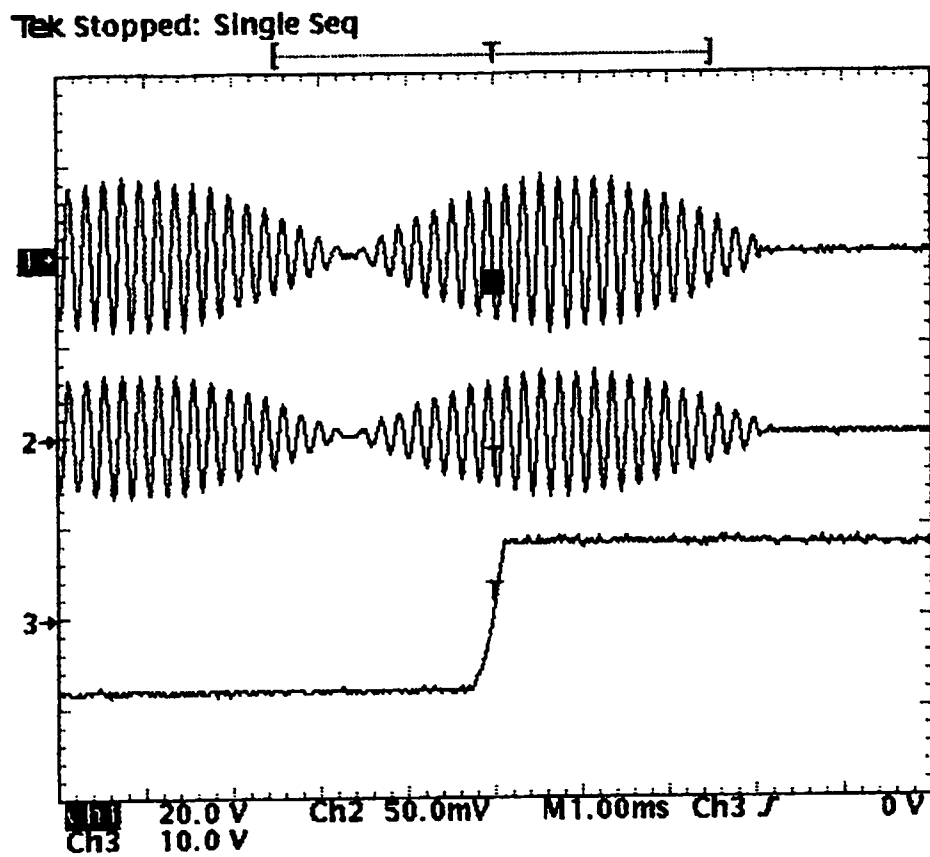


Figure 3.12. Transient response to power supply failure, modulated, 5.0KHz.

3.2 Current Regulation

In order to determine the drive capabilities of the instrument, the load resistance of each channel was varied over the range 125Ω to $1K\Omega$ while the output was set to its full-scale value. The load resistance values used were 125Ω , 167Ω , 250Ω , 500Ω , 667Ω , and $1K\Omega$ respectively. Each channel was calibrated at a nominal output current of 50mA rms with a load resistance of 250Ω . Figure 3.13 shows the change in current as the load resistance is varied from 125Ω to $1K\Omega$. Figure 3.14 shows the percent change (% deviation from 50mA rms) in output current over the same load resistance range. To determine a specification on the load resistance the instrument is capable of driving within a error band of $\pm 2\%$, Figure 3.14 is redrawn in Figure 3.15 with altered horizontal and vertical axes. From Figure 3.15 it can be seen that the instrument is capable of driving a load resistance of between 175Ω and 375Ω with an error of $\pm 2\%$ at full-scale.

If the instrument is to regulate the output current, then when the load resistance is doubled, to produce the same output current would require an output voltage of twice the previous amplitude. In the same manner, decreasing the resistance by a factor of two would require the voltage be halved. With the secondary of the output transformer loaded with a 250Ω resistor, the voltage measured at 50mA rms was 6.32 V rms. Changing the load resistance to 500Ω produced a load voltage of 12.76 V rms which shows the amplifier does a good job of regulating the transformer secondary current despite large load impedance changes.

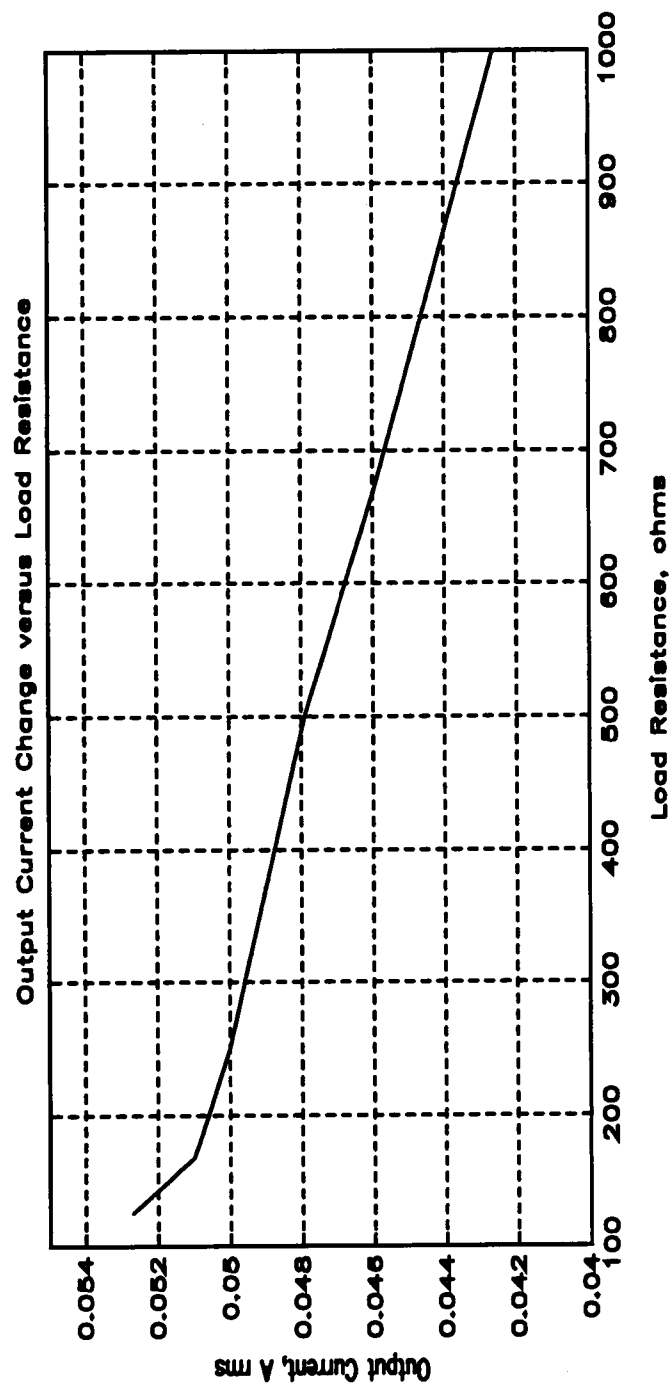


Figure 3.13. Output current change versus load resistance.

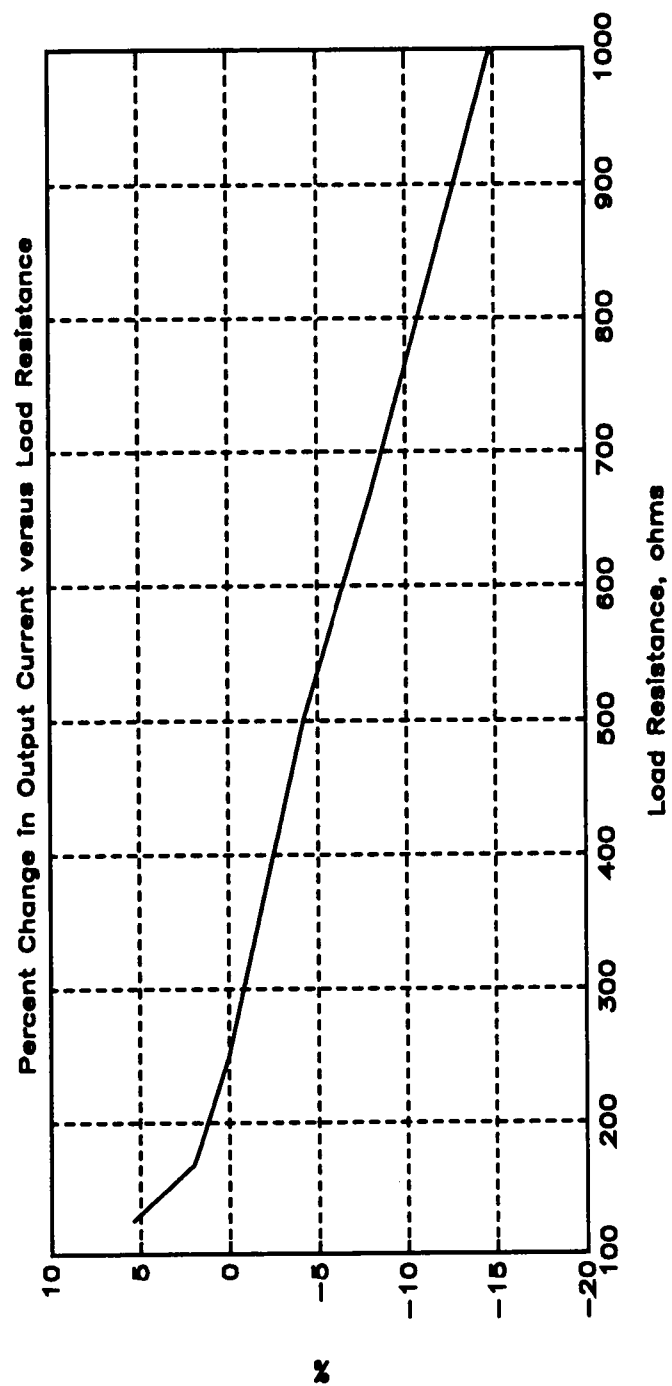


Figure 3.14. Percent change in output current versus load resistance.

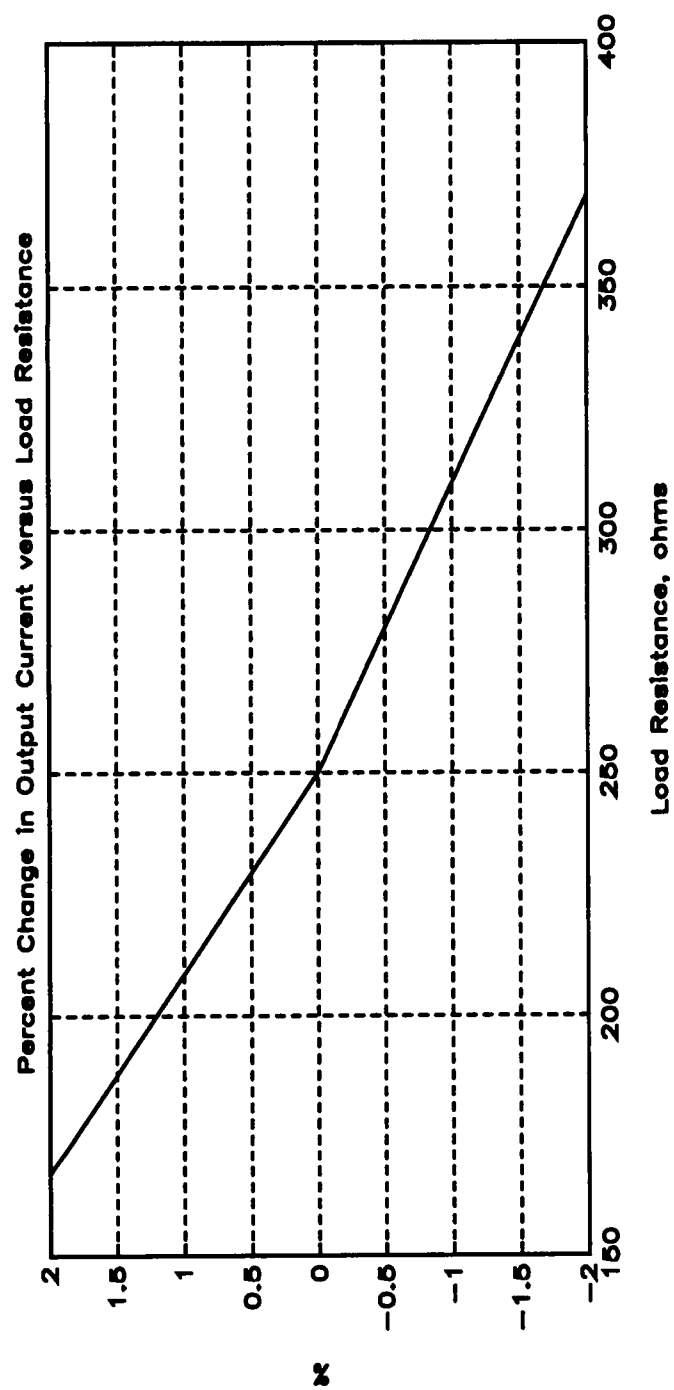


Figure 3.15. Output current change, $\pm 2\%$ full-scale.

Equation 2.29 gives the midband gain as a function of load resistance from the noninverting input of the LM1875 amplifier to the primary of T1 in Figure 2.53. This equation can be rewritten in terms of the secondary current in order to compare the experimentally observed current regulation and the predicted current regulation. With the secondary current of T1 in Figure 2.53 is equal to the primary current divided by the turns ratio, equation 2.29 can be solved for $I_{\text{secondary}}$ which gives

$$I_{\text{secondary}} = \frac{76375 V_{\text{input}}}{(13500 + R_{\text{load}}) N} \quad \text{Eq. 3.4}$$

With $N = 11.18$ from equation 2.28 and $V_{\text{input}} = 100\text{mV rms}$ (input voltage used during the development of Figure 3.13), equation 3.4 simplifies to

$$I_{\text{secondary}} = \frac{683.14}{(13500 + R_{\text{load}})} \quad \text{Eq. 3.5}$$

Figure 3.16 shows a plot of equation 3.5. Comparing Figure 3.13 with Figure 3.16 shows that equation 3.5 predicts a smaller secondary current change versus load resistance than was experimentally observed (Figure 3.13). This discrepancy is due to the ideal amplifier and transformer assumptions used in the derivation of equation 3.5.

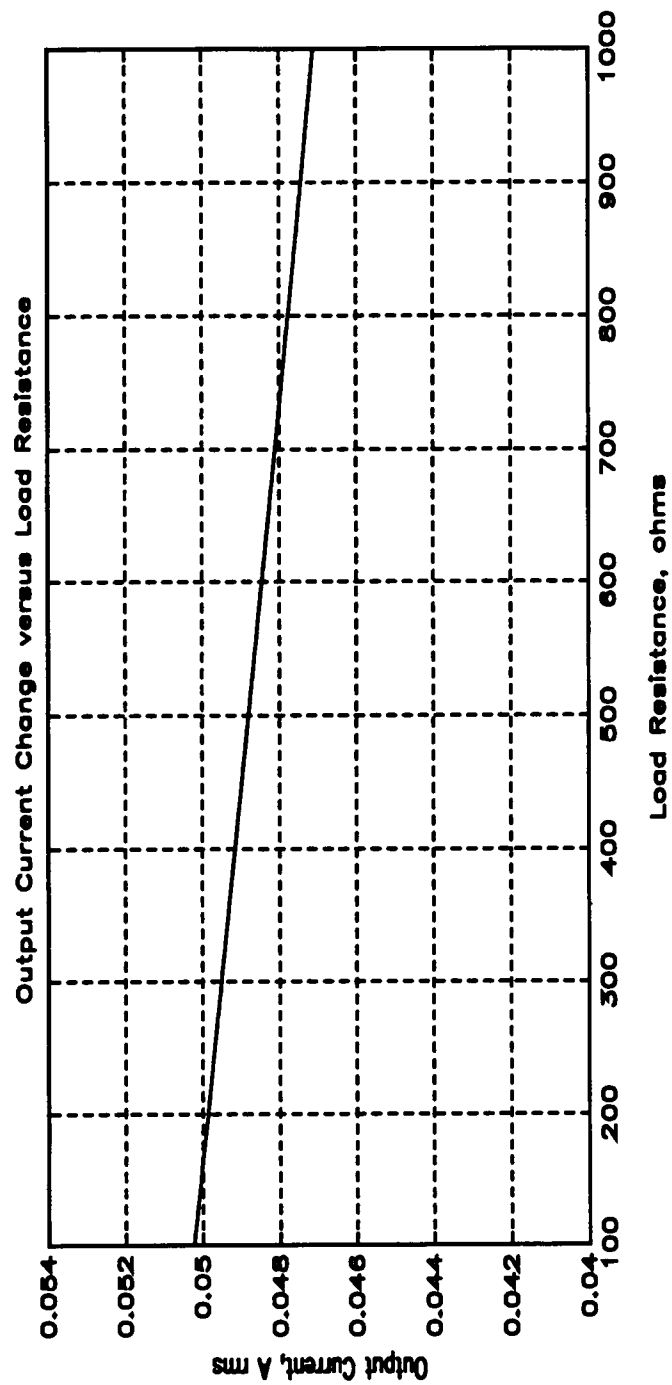


Figure 3.16. Output current change versus load resistance predicted by equation 3.5.

CHAPTER 4

CONCLUSIONS

AND SUGGESTIONS FOR

FURTHER WORK

This thesis has described a muscle stimulator that is safe and efficient in regard to the engineering required to design the instrument. Many, but not all, operating scenarios that could result in harm to the patient due to lack of adequate engineering were considered. Safety circuitry was included in the instrument to prevent these possibilities. One such scenario that was discussed, but for which no circuitry was included to prevent, is the possibility of the electrodes coming loose from the patient during treatment. This causes the electrode-patient contact area to decrease and the current density in the remaining area to increase. As the contact area continues to decrease, the current density continues to increase resulting in a stinging sensation. This, in the authors own experience, is a very painful process for which some provision should be made. Circuitry that monitors the output voltage and current waveforms as a function of setpoint would be required as would electrodes that could detect where the electrode surface was or was not in contact with the patient. One suggestion would be to monitor both the output voltage and current waveforms with an analog multiplier (output power) and compare a dc representation (RMS-to-DC converter) of this with the setpoint. If the output of this detector signal became greater than the setpoint by say 10%, the instrument would shut down the output amplifiers. This would only work for a constant current stimulator if the

load impedance rises during the removal of the electrodes while the instrument is actively producing output current. During one such experiment at very "low" current levels, the author was unable to detect any output waveform changes on himself. This indicates that proper detection would require a special type of electrode as described previously. It was felt that the research into these required electrodes was beyond the scope of this work and was therefore not included.

As a final note, very little information was available in the university library on the medical aspects of such an instrument. It is hoped that this thesis will further medical knowledge by making available results that can serve as a starting point for further research into the efficacy of muscle stimulators.

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APPENDICES

APPENDIX A

PSPICE Source File For Constant Current Power Amplifier

The following PSPICE source file was used to analyze the closed loop behavior of the ideal constant current power amplifier.

Ideal Amplifier Model

VIN 1 0 DC 1 AC .1V

XOPTTEST 3 1 2 ideal_amp

R1 5 4 1K

R2 2 6 50K

R3 6 3 50K

R4 6 7 5K

R5 3 8 10

RP 9 5 4

RS 5 0 0.18

C1 4 2 0.1uF

C2 2 3 33pF

C3 7 0 2.2uF

CP 8 9 220uF

L1 3 8 10uH

.AC DEC 10 0.10 1MEG

.subckt ideal_amp 6 1 2

* connections: | | |

* output | |

* +input |

* -input

Eopamp 6 0 1 2 1000MEG

Iopen1 1 0 0A ; Redundant connections made at inverting and

Iopen2 2 0 0A ; noninverting terminals

.ends ideal_amp

.PROBE

.END

APPENDIX B

Suggested Amplifier Printed Circuit Board Layout

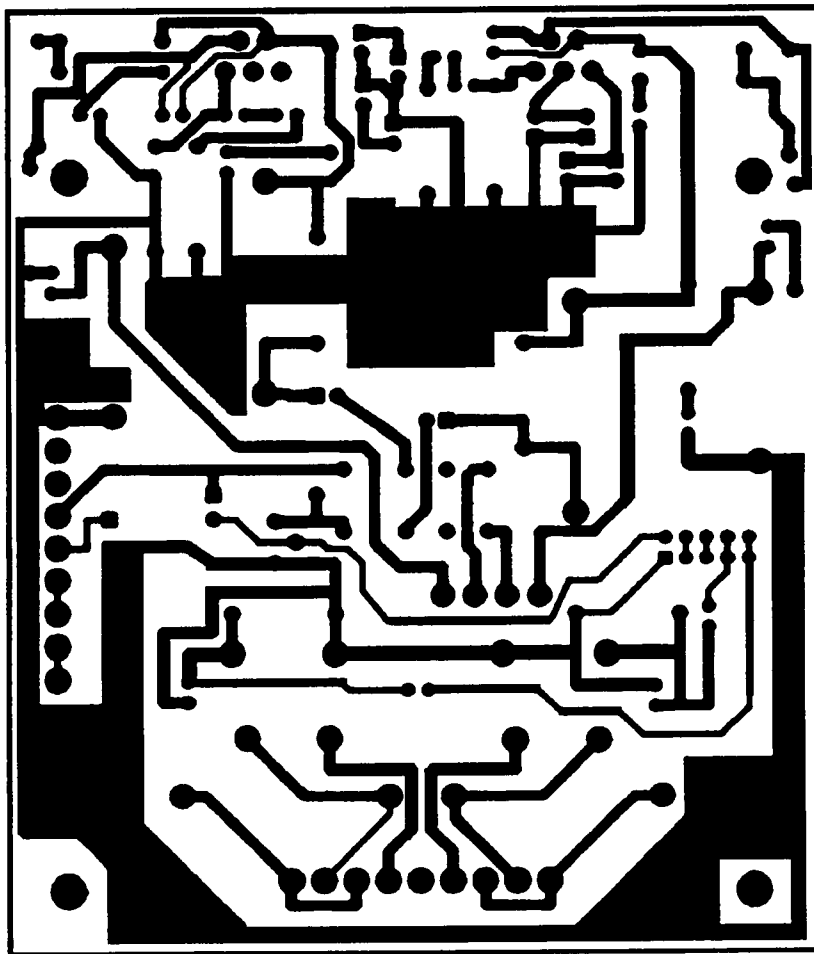


Figure B.1. Suggested power amplifier printed circuit board layout.

APPENDIX C

Table C.1

Power Amplifier Transfer Function

Experimental Data

Frequency	Ip, Amps	Phase, degrees
1.000E+01	9.582E-03	158
9.000E+01	7.935E-01	110
1.000E+02	8.256E-01	87
1.100E+02	7.876E-01	71
2.000E+02	6.657E-01	17
5.000E+02	5.590E-01	5.6
1.000E+03	5.439E-01	2.2
2.000E+03	5.404E-01	0.9
3.000E+03	5.403E-01	-0.5
4.000E+03	5.408E-01	-0.8
5.000E+03	5.416E-01	-1.2
6.000E+03	5.431E-01	-2.0

Table C.1

Continued

Frequency	Ip, Amps	Phase, degrees
7.000E+03	5.440E-01	-3.0
8.000E+03	5.456E-01	-4.2
9.000E+03	5.475E-01	-5.0
1.000E+04	5.495E-01	-5.2
2.000E+04	6.111E-01	-10.1
3.000E+04	7.427E-01	-15.3
4.000E+04	8.792E-01	-25.6
4.500E+04	9.123E-01	-34.0
5.000E+04	9.641E-01	-40.0
6.000E+04	6.863E-01	-68.0
7.000E+04	5.365E-01	-93.0
1.000E+05	3.207E-01	-140.0
1.000E+06	3.589E-01	-166.2

APPENDIX D

Table D.1

Power Amplifier Loop Transmission

Experimental Data

Frequency	V(5), Volts	Phase, degrees
1.000E+01	5.474E-05	37.6
9.000E+01	6.244E-03	-28.3
1.000E+02	7.608E-03	-32.6
1.100E+02	9.210E-03	-36.4
2.000E+02	2.160E-02	-60.0
5.000E+02	6.243E-02	-95.0
1.000E+03	1.160E-01	-125
2.000E+03	1.682E-01	-164
3.000E+03	1.701E-01	-191
4.000E+03	1.579E-01	-209
5.000E+03	1.399E-01	-224
6.000E+03	1.193E-01	-232

Table D.1

Continued

Frequency		
7.000E+03	1.088E-01	-241
8.000E+03	8.868E-02	-248
9.000E+03	8.435E-02	-254
1.000E+04	7.933E-02	-259
2.000E+04	3.596E-02	-288
3.000E+04	1.868E-02	-303
4.000E+04	1.296E-02	-312
4.500E+04	1.098E-02	-316
5.000E+04	8.814E-03	-318
6.000E+04	5.911E-03	-322
7.000E+04	4.825E-03	-325
1.000E+05	2.617E-03	-330
1.000E+06	4.038E-05	-356

APPENDIX E

PSPICE Source Files For Power Fail Detect

The following PSPICE source files were used to analyze the behavior of the power fail detect circuit with and without a time delay.

POWER FAIL DETECT CIRCUIT WITHOUT DELAY

VSW 20 0 PULSE(0 1 20M 1u 1u 0.5)

SW1 4 3 20 0 POWERON

VP 49 0 DC 9.50V

RSP 49 50 1

SW2 50 51 20 0 POWERON

C3 51 0 3400uF

R10 51 0 20

VN 48 0 DC -9.5

RSN 48 52 1

SW3 52 53 20 0 POWERON

C4 53 0 3400uF

R11 53 0 20

R4 51 6 100K

R5 6 0 24.9K

VAC1 1 0 SIN(0 11 60 0 0)

VAC2 0 2 SIN(0 11 60 0 0)

D1 1 3 DIODE

D2 2 3 DIODE

R1 4 0 560

C1 4 0 10uF

R2 4 5 100K

D3 5 4 DIODE
 R3 5 0 39K
 C2 5 0 1uF
 XOPAMP 6 5 51 53 7 LM324
 R6 7 8 42K
 Q1 10 8 9 QDV
 R7 51 10 2.1K
 R8 53 9 1.4K
 .TRAN .01 1
 .MODEL DIODE D IS=10.00E-15 RS=1 IKF=0 N=1 XTI=3 EG=1.110
 .MODEL QDV NPN IS=1E-7 BF=100
 .INCC LM324.CIR
 .END

POWER FAIL DETECT CIRCUIT WITH DELAY

VSW 20 0 PULSE(0 1 20M 1u 1u 0.5)
 SW1 4 3 20 0 POWERON
 VSWD 21 0 PULSE(1 0 100M 1u 1u 2)
 SWD1 6 0 21 0 POWERON
 VP 49 0 DC 9.50V
 RSP 49 50 1
 SW2 50 51 20 0 POWERON
 C3 51 0 3400uF
 R10 51 0 20
 VN 48 0 DC -9.5
 RSN 48 52 1
 SW3 52 53 20 0 POWERON
 C4 53 0 3400uF
 R11 53 0 20
 R4 51 6 100K

R5 6 0 24.9K
VAC1 1 0 SIN(0 11 60 0 0)
VAC2 0 2 SIN(0 11 60 0 0)
D1 1 3 DIODE
D2 2 3 DIODE
R1 4 0 560
C1 4 0 10uF
R2 4 5 100K
D3 5 4 DIODE
R3 5 0 39K
C2 5 0 1uF
XOPAMP 6 5 51 53 7 LM324
R6 7 8 42K
Q1 10 8 9 QDV
R7 51 10 2.1K
R8 53 9 1.4K
.TRAN .01 1
.MODEL DIODE D IS=10.00E-15 RS=1 IKF=0 N=1 XTI=3 EG=1.110
.MODEL QDV NPN IS=1E-7 BF=100
.INCC LM324.CIR
.END

APPENDIX F

Suggested Power Supply Printed Circuit Board Layout

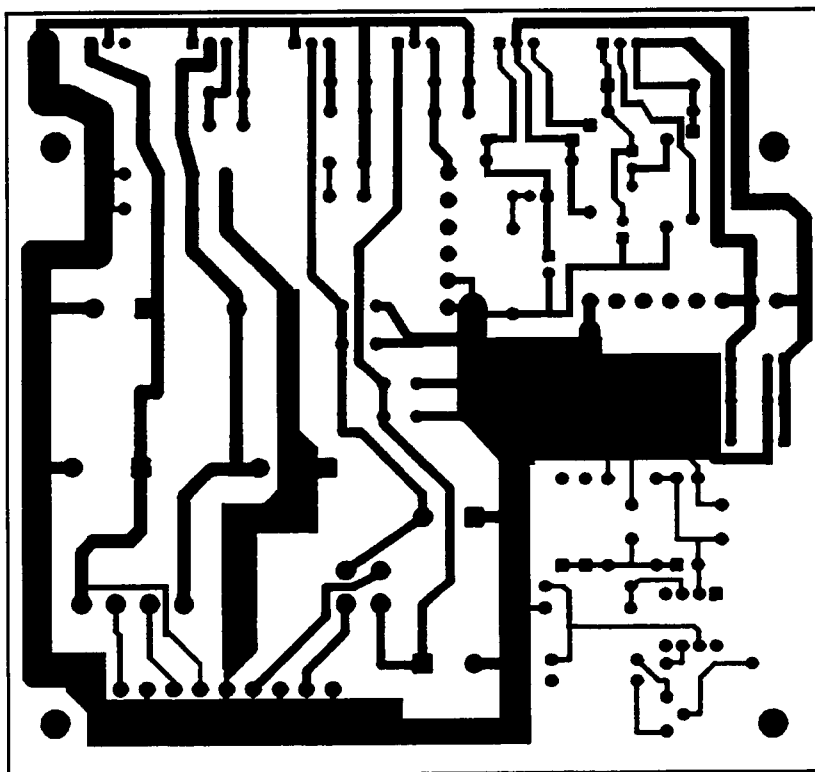


Figure F.1. Suggested power supply printed circuit board layout.

VITA

Barry E. Martin was born in Summerville, South Carolina, on August 15, 1962. He was graduated from McMinn Central High School in June 1980 and attended The University of Tennessee, Chattanooga, receiving the Bachelor of Science degree in Electrical Engineering in May 1987. He also attended the University of Tennessee, Knoxville, receiving the Master of Science degree with a major in Electrical Engineering in May 1994. He is married and has one daughter.

His professional experience includes three years with Chattanooga Corporation as a medical electronics design engineer, five years as Assistant Professor of Electronics at Cleveland State Community College, and consulting contracts with TRW, M&M Mars, Bowater Southern, and Siemens Power.