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Design of a Cost-efficient Reconfigurable Pipeline ADC

**A Dissertation
Presented for the
Doctor of Philosophy Degree**

The University of Tennessee, Knoxville

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December 2007**

ACKNOWLEDGEMENTS

I take this opportunity to express my deep gratitude to my advisor, Dr. Syed K. Islam, for valuable guidance and close cooperation during my Ph.D. education. The numerous discussions, suggestions and encouragement for the past several years have helped me to finish this work. His careful reading and corrections made this manuscript readable. I would like to thank my committee member, Dr. Mohamed Mahfouz, for funding the chip fabrication and providing the financial support for the Ph.D. education. Without his help, this design could not have been completed in such a smooth way. I would also like to thank my other committee members: Dr. Benjamin Blalock and Dr. Ethan Farquhar, for their endless encouragement and helpful advice about my proposal and dissertation.

I would like to thank all of my co-workers at Analog VLI & Device laboratory and the Center for Musculoskeletal Research for their help and friendship. They are Rajagopal Vijayaraghavan, Mo Zhang, Chiahung Su, Amihul Huque, Touhidur Rahman, Rafiqul Haider, Sazia Eliza, Taheo Oh and Tim Grundman in Analog Device & VLSI Laboratory, Gary To, Boyd Evans, Emily Pritchard, Linda Sargent, Mike Kuhn and Brandon Merkl in CMR.

Special Thanks are given to my wife, Ke Jiang, for her continuous support of my

work and my life. Without her, nothing could be done.

Last but never the least, I would like to thank my mother, my mother-in-law, my father-in-law, my brother, my sisters and my nephews for their love, encouragement and support.

ABSTRACT

Power budget is very critical in the design of battery-powered implantable biomedical instruments. High speed, high resolution and low power usually cannot be achieved at the same time. Therefore, a tradeoff must be made to compromise every aspect of those features. As the main component of the bioinstrument, high conversion rate, high resolution ADC consumes most of the power. Fortunately, based on the operation modes of the bioinstrument, a reconfigurable ADC can be used to solve this problem. The reconfigurable ADC will operate at 10-bit 40 MSPS for the diagnosis mode and at 8-bit 2.5 MSPS for the monitor mode. The ADC will be completely turned off if no active signal comes from sensors or if an off command is received from the antenna.

By turning off the sample hold stage and the first two stages of the pipeline ADC, a significant power saving is achieved. However, the reconfigurable ADC suffers from two drawbacks. First, the leakage signals through the extra off-state switches in the third stage degrade the performance of the data converter. This situation tends to be even worse for high speed and high-resolution applications. An interference elimination technique has been proposed in this work to solve this problem. Simulation results show a significant attenuation of the spurious tones. Moreover, the transistors in the OTA tend to operate in weak inversion region due to the scaling of the bias current. The transistor in

subthreshold is very slow due to the small transit frequency. In order to get a better tradeoff between the transconductance efficiency and the transit frequency, reconfigurable OTAs and scalable bias technique are devised to adjust the operating point from weak inversion to moderate inversion.

The figure of merit of the reconfigurable ADC is comparable to the previously published conventional pipeline ADCs. For the 10-bit, 40 MSPS mode, the ADC attains a 56.9 dB *SNDR* for 35.4 mW power consumption. For the 8-bit 2.5 MSPS mode, the ADC attains a 49.2 dB *SNDR* for 7.9 mW power consumption. The area for the core layout is 1.9 mm² for a 0.35 micrometer process.

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ABBREVIATIONS

3G	Third Generation
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
ASK	Amplitude Shift Keying
BPF	Band Pass Filter
BW	Bandwidth
CDMA	Code Division Multiple Access
CMFB	Common Mode Feedback
CMRR	Common Mode Reject Ratio
DAC	Digital to Analog Converter
DNL	Differential Nonlinearity
DR	Dynamic Range
ENOB	Effective Number of Bits
ESSCIRC	European Solid-State Circuits Conference
FDA	Food and Drug Administration
FFT	Fast Fourier Transform
FOM	Figure of Merit
GSM	Global System for Mobile Communication
IA	Instrumentation Amplifier
IC	Integrated Circuit
ICMR	Input Common Mode Range
INL	Integral Nonlinearity
ISSCC	International Solid-State Circuits Conference
JSSC	Journal of Solid-State Circuits

LCL	Lateral Collateral Ligament
MCL	Medial Collateral Ligament
MDAC	Multiplying Digital to Analog Converter
MIS	Minimum Invasive Surgery
MSPS	Mega Samples per Second
MTTF	Mean Time To Failure
NMOS	N-type Metal Oxide Semiconductor (Field Effect Transistor)
OTA	Operational Transconductance Amplifier
PDK	Process Design Kit
PMOS	P-type Metal Oxide Semiconductor (Field Effect Transistor)
PTAT	Proportional To Absolute Temperature
RMS	Root Mean Square
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SHA	Sample and Hold Amplifier
SMA	Subminiature version A
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SOC	System On Chip
THA	Total Hip Arthroplasty
THD	Total Harmonic Distortion
VLSI	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

In this chapter, the biomedical background of the project is introduced in section 1.1. Then, the reconfigurable ADC concept, used to solve the power-speed-resolution tradeoff, is discussed with the operation modes of the bioinstrument in this section as well. The pipeline ADC architecture is selected after a comparison among the most popular ADC topologies in section 1.2. The research goal and contribution of this work is also listed in sections 1.3 and 1.4, respectively. The overview of the whole dissertation is given in section 1.5.

1.1 Research Motivation

The use of prosthetic joint implants to treat patients with severe osteoarthritis and other joint degenerative diseases began in the early 70s. During the knee joint implant surgery, surgeons needed to perform accurate resections depending on various instruments such as spacer block, tensioner and tram adapter. These instruments provided valuable information about the gap shape and size during the bone resection process. However, the feedback of these instruments, such as the spacer block, is qualitative and

the degree of tightness of the ligaments is inaccessible [1].

Despite the rapid development of *in vivo* telemetry sensor based instruments in biological and physiological areas, only a few of these systems [2-5] have been designed for orthopedic applications and none of them can be used for Minimum Invasive Surgery (MIS) [6].

The first published research [2] on using sensors and biotelemetry in orthopedics focused on obtaining *in vivo* data from Total Hip Arthroplasty (THA) patients. Bergmann *et al* used 3 strain gauges to measure the 3 orthogonal force components acting on the prosthetic head postoperatively [2]. All the electronic components (14 active and 21 passive) were integrated using thick film hybrid technology instead of monolithic integrated circuit. Due to the large volume and geometry of the implant, it was not difficult to allocate adequate space for the sensors and electronics. At the same time, Davy *et al* [7] and Kotzar *et al* [8] developed a similar hip prosthesis to monitor various loading conditions of patients. In 2002, Claes *et al* reported an 18-channel strain gauge measurement system for stress monitoring system for dental implants [5]. The system can monitor up to 18 strain gauge channels (six abutments) during a two days period. Furthermore, an ASIC chip also has been developed for the monitor system after the prototype developed using commercial chips [9].

The trend of using ASIC to replace the commercial chips in design of biomedical instruments shows the great advantage of ASIC in the following features:

--Small size: In order to develop a fully functional biomedical instrument, several different functional commercial chips and off-chip components are needed which lead to a large device area. On the other hand, part of the functionality of the chip will never be used and lead to low cost efficiency.

--Low-power consumption: Power consumption is very critical for battery-powered instruments, especially for implantable instruments that do not have the provision to replace the battery. ASIC can be designed to use minimum power with the same functionality of the commercial chips.

--Flexible functionality: The functions of the ASIC can be tailored to fulfill exactly the necessary function without redundancy.

--Long term reliability: The Mean Time To Failure (MTTF) of ASIC is much better than the MTTF of board-level and thick-film-hybrid based instruments.

The spacer block, used to adjust the Medial Collateral Ligament (MCL) and the Lateral Collateral Ligament (LCL) during the bone resection in figure 1.1, can give surgeons qualitative feedback about the flatness of the bone. The balance of the MCL and LCL can only be adjusted by the experience of the surgeons.

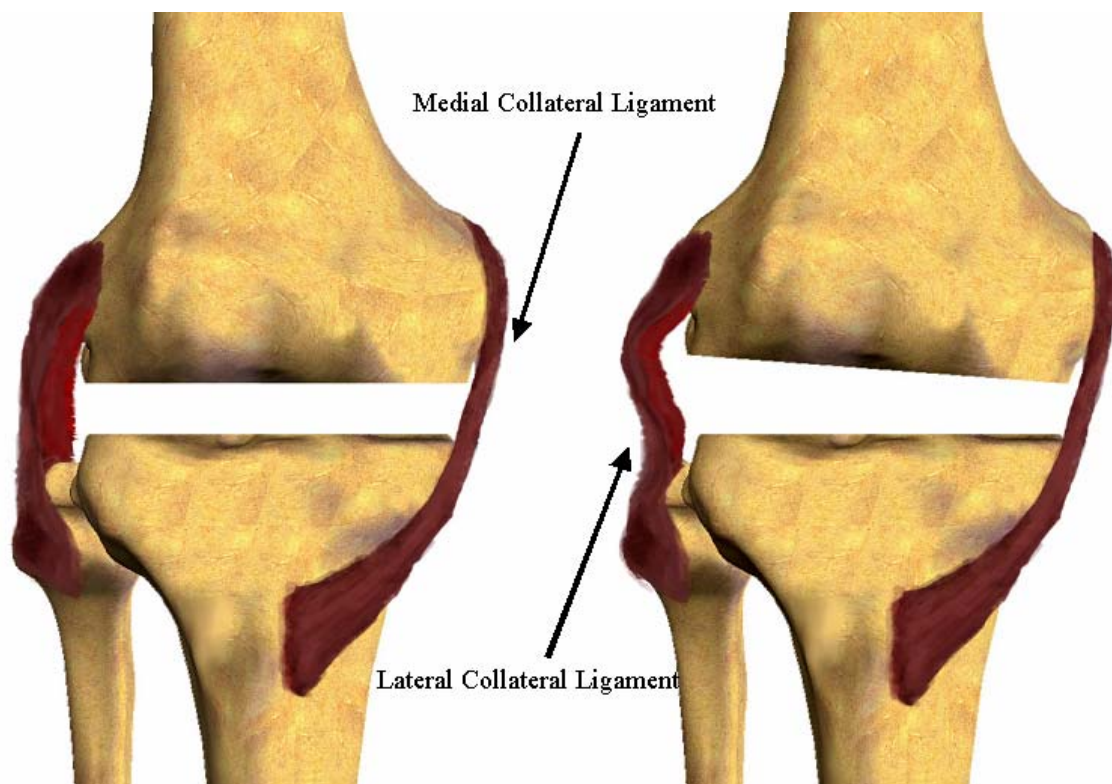


Figure 1.1 Knee joint balance between Medial Collateral Ligament (MCL) and Lateral Collateral Ligament (LCL). The right one shows an imbalance joint due to the loose LCL.



Figure 1.2 Traditional space blocker (left) and newly designed sensor and ASIC technique enhanced space blocker model (right)

A new spacer block [1], shown in figure 1.2 with a traditional one, is designed by taking advantage of the sensor, the ASIC and the telemetry technology. The sensors and chips are on the top surface with a battery inside the spacer block, and the antenna is also designed to fit in the handle. The surface of the instrument was encapsulated by epoxy with full FDA compliance.

The system block diagram is shown in figure 1.3 [10]. The system can be partitioned into three parts based on their functions. The first part is the sensor array. There are 30 strain-sensing micro-cantilevers distributed evenly on the two sides of the spacer block's top plate. The Wheatstone bridge configured sensors convert the physical strain to a resistance change and then to a voltage signal under a DC excitation.

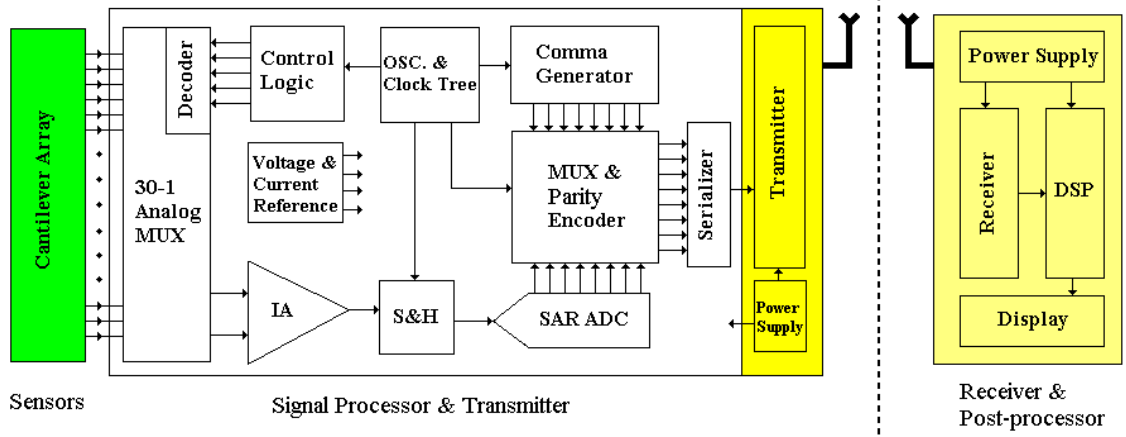


Figure 1.3 Sensor signal processing chip block diagram

The signal processing part shown in the middle of figure 1.3 includes two chips, one chip for signal processing [10] and another for signal transmission. The signal-processing chip amplifies the signal from the sensors and digitizes the analog signal to digital domain. The transmitter chip sends out the signal using ASK modulation with 335MHz carrier frequency. The receiver part receives and recovers the data remotely. Then the data will be post-processed by software and shown graphically on the display.

Three versions of the signal-processing chip [10-12] have been developed for this project. All of them have an embedded SAR ADC for signal digitizing. The 8-bit 1.54 MSPS SAR ADC is power-efficient and suitable for medium conversion rate and

medium resolution, but with the increasing number of sensors and high accuracy requirement, SAR ADC is no longer the best choice for this application. A high resolution, high speed ADC should be developed to replace it. It is well known that high resolution, high speed ADC consumes huge power. For battery-powered or implantable instruments, power consumption is very critical. A trade-off must be made to compromise every aspect of the system. Fortunately, the instruments underdeveloped are not necessary to work all the time. Their operations can be categorized into three different modes: diagnosis mode, monitor mode, and off mode.

During the diagnosis mode, surgeons need to know the pressure profile in the knee with high resolution, so all the sensor data are collected with a large bandwidth. For the monitor mode, most of the sensors will be turned off and only some of the sensor data are collected with coarse resolution to monitor the pressure range. When the patients are sleeping or not moving, the system is completely turned off. The multi-mode operations of this bioinstrument require the ADC to have corresponding actions. Therefore, the requirements for the ADC are reconfigurable both in conversion rate and in resolution.

Besides the biomedical application, reconfigurable ADCs have extensive applications in sensor signal processing, SOC and telecom area. In some autonomous wireless ‘listening’ devices (acoustic, vibration, etc) [13, 14] where the incoming signal is inactive most of the time, it is desirable to tune the ADC to low speed and low

resolution to save power, and increase the speed and resolution only when an active signal is detected. For wireless mobile communications, different networks, such as GSM, CDMA2000, WCDMA, are co-existed in the same area. This fact leads to a need for multi-standard mobile terminals. Such mobile terminals will have to accommodate to wideband wireless local area networks as well as 3G standards [15, 16]. The ADCs in such mobile terminals have to handle different baseband signals as well as different dynamic range requirements. Typically, the bandwidth may vary from 200kHz to 20-40 MHz and dynamic range may vary roughly between 6-12 bits, depending on the standard supported. A reconfigurable ADC fulfilling these requirements is in great demand.

1.2 Comparison of ADC Topologies

Since there are many ADC topologies and each of them have different applications, a comparison of these ADCs can help us to choose the most suitable architecture. The comparison of ADC topologies is shown in table 1.1.

After the ADC concept was initially published in the middle 50's [17, 18], different topologies have been developed since then. Flash ADC is good for high speed, low resolution applications. The number of comparators will increase exponentially with the number of bits, leading to a huge amount of power and area consumption. Integration-type ADC is in the opposite direction. The resolution can be high, but the conversion time increases exponentially with the number of bits. As mentioned previously, SAR

Table 1.1 Comparison of ADC Topologies

	Flash	Pipeline	Cyclic	SAR	$\Sigma \Delta$	Integration
Speed	Fastest	Fast	Medium	Medium	Low-medium	Low
Resolution	Lowest	Medium	Medium	Medium	High	Medium-high
Area	Largest	Medium	Smallest	Small	Medium	Medium
Power Efficiency	Lowest	Highest	Low	High	Medium	Medium
Reconfigurability	Low	High	Highest	Medium	High	Medium

ADC is good for medium speed and medium resolution applications [19].

In addition, there are two other very important types of ADC: sigma-delta ADC and pipeline ADC. Both of them are very popular with sigma-delta mainly focusing on high resolution and pipeline focusing on high speed. Moreover, they are also very easy to reconfigure in resolution and conversion rate but in different manners.

Sigma-delta ADC uses oversampling to trade bandwidth with low noise (high resolution), so the resolution can be very high but the input signal bandwidth it can processing is low. Sigma-delta ADCs can be used in either high resolution, small bandwidth or low resolution, large bandwidth applications. Instead, pipeline ADCs fit the requirements perfectly. It can work in high resolution, high conversion rate and low

resolution, low conversion rate mode. A brief summary for different types of ADC is shown in table 1. It should be noted that not all the topologies of ADC are compared here. Some structures such as folding were not compared due to popularity.

1.3 Research Objective

The research goal of this work is to design a reconfigurable pipeline ADC that can be embedded in the sensor signal-processing chip. In the mean time, the ADC should only add a small extra cost in terms of power and area without degrading the performance when compared with traditional pipeline ADCs. In other words, it should be cost-efficient. Moreover, this reconfigurable ADC should have three different modes corresponding to the bioinstrument operations:

- a) High speed, high resolution mode: ADC works at 40 MSPS sampling rate with 10-bit resolution.
- b) Low speed, low resolution mode: ADC works at 2.5 MSPS sampling rate with 8-bit resolution.
- c) Power off mode: ADC is completely off.

1.4 Original Contribution

A reconfigurable ADC that can work in either high speed, high resolution mode or low speed, low resolution mode is proposed in this work. For the reconfigurable ADC,

the following techniques are used to improve the performance in different configurations.

a) Interference elimination technique for the reconfiguration stage.

This technique is treated in detail in section 4.1.

b) Reconfigurable OTA for transistor operation region adjustment.

This technique is treated in section 4.2.

c) Reconfigurable scalable bias technique for different configurations.

This method is treated in section 4.1 and section 6.1.3.

1.5 Dissertation Overview

In **Chapter 1**, some biomedical background for this work and the problems met during the design of a sensor signal processing system are introduced. Then, some popular ADC topologies are reviewed with different aspects of characteristics. Once the ADC structure is chosen, a thorough search for reconfigurable ADCs are carried out, and their design methods and performance are compared in **Chapter 2**. Pipeline ADC structure and theories are treated in **Chapter 3**. Based on prior designs, an improved design with new features such as interference elimination technique, reconfigurable opamp, and scalable bias technique are developed. The details about the development are given in **Chapter 4**. Nonidealities with emphasis on fundamental limitations, such as noise and matching, are treated in **Chapter 5**. The prototype implementation is presented in **Chapter 6**. High performance OTAs, high-speed comparators, bias generation and distribution circuit and layout design are given in this chapter as well. Measurement

results of the reconfigurable pipeline ADC are illustrated in **Chapter 7** with the comparison with different ADCs. Discussions and conclusions are summarized in **Chapter 8**. The future work is listed in **Chapter 9**.

CHAPTER 2

LITERATURE REVIEW

As a key component of modern electronic products, ADC is in high demand in communication, consumer electronics, biomedical instruments, and various measurement instruments. Different requirements for different applications keep pushing ADC to higher speed and higher resolution. A large volume of literatures about ADC has been published in the past 30 years but very few of them are related to reconfigurable ADCs. In this chapter, the ADC reconfigurability is described in section 2.1. Some of the best papers about reconfigurable ADCs are selected and their features are explained in section 2.2. The performance parameters of these ADCs are also summarized in section 2.3. In order to compare these designs, different figure of merits are introduced in section 2.4. The problems generated during the reconfiguration are listed in section 2.5.

2.1 Reconfigurability of ADC

2.1.1 Reconfigurability on Conversion Rate

The most famous example about reconfigurable ADC on conversion rate is the time-interleaved ADC [20]. For this type of ADC, identical channels are combined

together in the time-interleaved manner and every channel is a complete ADC. The conversion can take place several times in one clock cycle depending on how many channels in the system. The conversion rate can be varied by altering the number of parallel channels but this approach suffers from distortions caused by mismatch among the different parallel channels [21]. Furthermore, sampling clock skews for different channels will finally limit the linearity to 10 bits for 20 MHz input frequency [22]. One solution for this problem is using only one sample and hold circuit for all the channels, but this solution will make the design of sample and hold extremely challenge since it will work in a much higher frequency.

There are some other configurations on the conversion rates. For a pipeline ADC, by turning off the latter stages and connecting the outputs of the first several stages to their inputs, the ADC changes to a algorithm cyclic ADC and the conversion rate is decreased [23]. By scaling the OTA bias current, the conversion rate can be scaled accordingly [24, 25]. If the conversion rate reconfiguration range is very large, the OTA tends to work in weak inversion, hurting the transit frequency. In order to alleviate this problem, the ADC can be designed to work in one clock period and then rest in the following several clock periods. The speed can be decreased and the average power consumption is decreased too. The combination of power scaling the period skipping technique is used in [26]. The penalty of this method is that a complex clock scheme should be generated.

For sigma-delta ADC, the configuration is easier. By keeping the oversampling ratio constant and changing the sampling frequency, the signal bandwidth can be altered [16, 27, 28]. A combination of pipeline mode and sigma-delta mode ADC was presented in [29]. The dynamic range is high but the signal bandwidth is small due to oversampling. The design is very complex with a considerable area overhead due to the configuration between pipeline mode and sigma-delta mode.

2.1.2 Reconfigurability on Conversion Resolution

One approach for reconfigurable on conversion resolution is using the sigma-delta modulator. The resolution of the sigma-delta ADC is decided by decimation filtering and different decimation filters can be implemented for different resolutions. It is possible to trade signal bandwidth for accuracy by adjusting the oversampling ratio [30-34]. However, it is very challenge to implement the decimation filter due to the high oversampling ratio. Therefore, this approach is usually used for the low signal bandwidth.

For the pipeline ADC, there are two approaches to configure the resolution. First one is turning off the latter stages [23, 35]. Another one is turning off the first several stages and reroute the input signal to the configuration stages [36]. These two approaches each have their own pros and cons. The first method is very easy and needs minimum hardware to configure, but gains no power benefit from it. The second one will need some extra hardware, such as wires and switches but huge power can be saved because

the first several stages are power hungry blocks. However, these extra routing wires and switches bring some interference to the configuration stages and deteriorate the overall performance.

2.2 Design Examples in Prior Arts

2.2.1 Gulati's Design

Gulati's design was published in 2001 [29]. This design can change its architecture between pipeline and sigma-delta modes. It can also vary its circuit parameters, such as size of capacitors, length of pipelines, and oversampling ratio. Moreover, the bias currents are varied in proportion to the sampling frequency. Opamp scaling and opamp sharing between two consecutive stages are used in pipeline mode.

The ADC can be configured in the range of 6-16 bits. The ADC architecture is illustrated in figure 2.1. The main concept of this design is that since the basic construction units (OTAs, comparators) of both pipeline ADC and sigma-delta ADC are almost the same, they can be regrouped to have different functions. The method has several disadvantages. First, since the OTAs and the comparators are optimized for some particular situations, they may not have maximum efficiency in other operation mode. Second, reconfigurations between two completely different modes (pipeline and sigma-delta) need more switches to switch back and forth, leading to a large area and more interference.

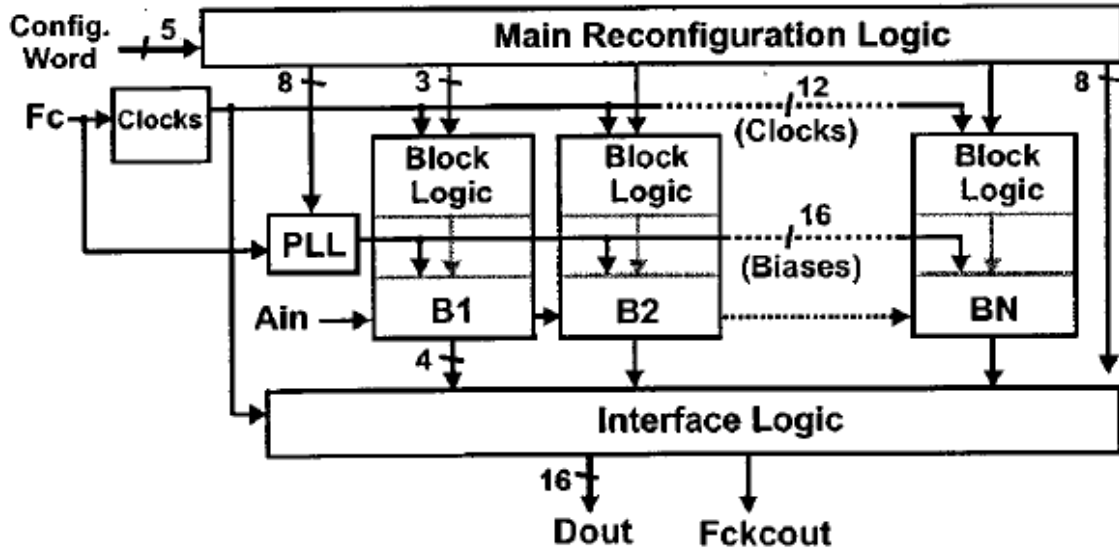


Figure 2.1 Block diagram of Gulati's design [29]

2.2.2 Anderson's Design

Anderson's design was published in 2005 [23, 37]. This design has 8 configurations with top performance of 10-bit 80MSPS. This design has reconfigurability in both conversion rate and resolution. The resolution reconfiguration was realized by turning off the latter stages and the conversion rate reconfiguration was implemented by changing stage 2 and stage 4 for cyclic ADC. The block diagram of this design is shown in figure 2.2. One of the drawbacks of this design is there is no OTA power scaling involved [38], so the power efficiency is low.

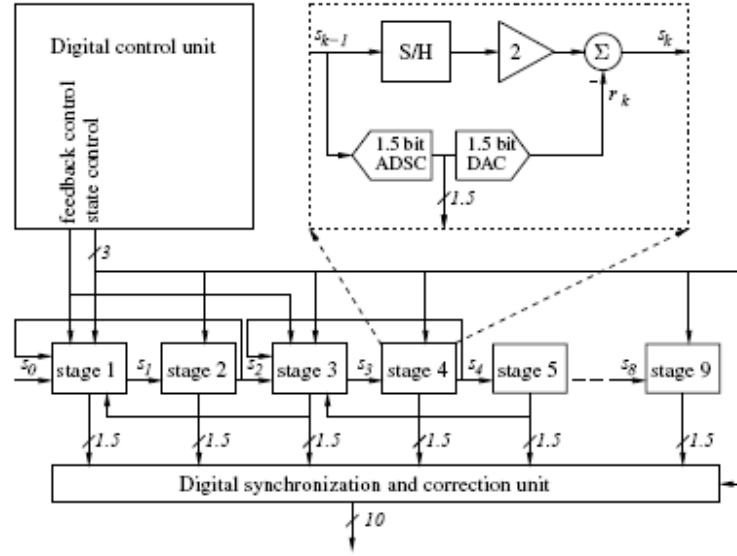


Figure 2.2 Block diagram of anderson's design [23]

2.2.3 Audoglio's Design

Audoglio's design was published in Sept. 2006 in ESSCIRC [36]. This design has 4 different configurations in resolution. The maximum sample rate is 20 MSPS. This design can only vary the resolution, but the method used to reconfigure the ADC is very similar to this work. The pipeline is power-efficient due to power scaling in consecutive stages. Turning off the first several stages instead of later stages leads to huge power savings. Even the structure of this work is similar to Audoglio's design, but the concept was already developed before this paper. The block diagram of the design is illustrated in figure 2.3. In this design, opamp sharing between two consecutive stages is extensively involved. Very sophisticated digital background calibrations were implemented in this design to improve the ADC performance.

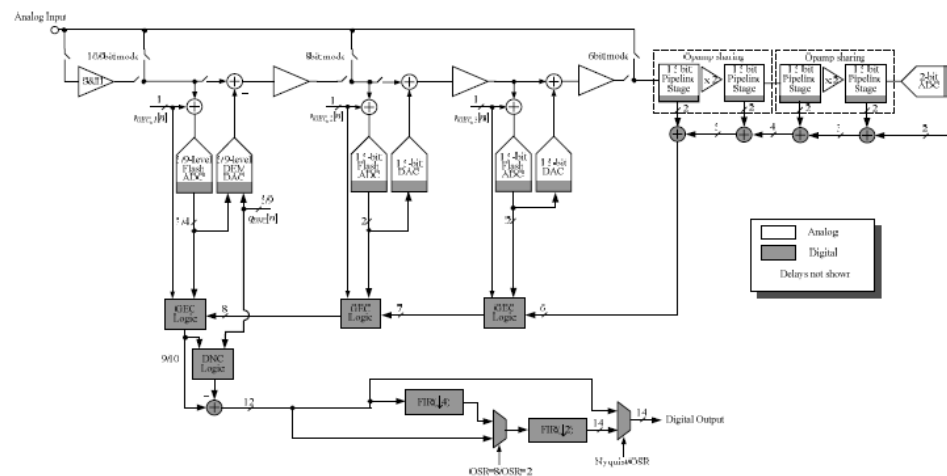


Figure 2.3 Block diagram of Audoglio’s design [36]

2.2.4 Ahmed's Design

Ahmed's design was published in Dec. 2005 on JSSC[26]. This ADC can only be configured on conversion rate. However, this design has the largest range on conversion rate. It can work from 50 MSPS to 1 KSPS. The conversion rate ratio is up to 50K. It's very hard to scale the power corresponding to each conversion rate only depending on the bias scaling over such a large ratio. The author uses two methods to solve this problem. First, for low conversion rate, the ADC only works for one clock period and rests for several clock periods depending on the configuration. The average power can be decreased since the ADC is off during most of the time. Second, since the OTA in the ADC is working periodically, they should be powered on rapidly when employed. The timing and block diagram of the ADC is shown in figure 2.4.

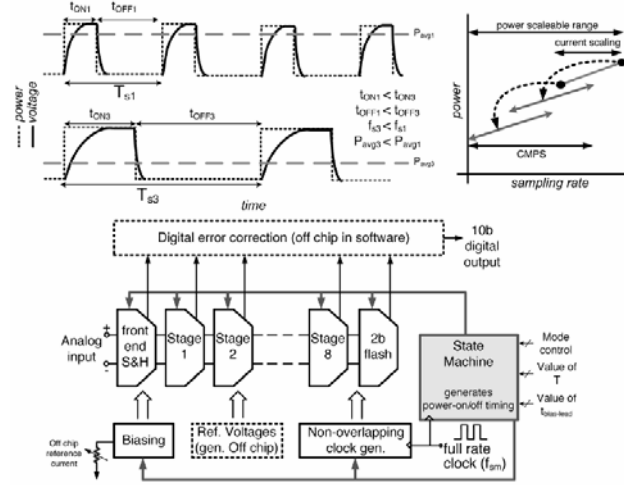


Figure 2.4 Timing and Block diagram of Ahmed's design [26]

Table 2.1 Reconfigurable ADC Performance Summary

Ref.	Bits (b)	f_s (MHz)	Power (mW)	VDD (V)	ENOB (b)	Area (mm ²)	Process (μ m)	Configuration	Comments
[25]	14	10-40	72.8	2.8	10.4	1.15	0.18	Rates	Calibration
[24]	12	20-140	97	1.8	10.4	0.86	0.18	Rates	
[26]	10	1k-50	35	1.8	8.8	1.2	0.18	Rates	
[29]	6-16	2.62	24.6	4.6		79.8	0.6	Rates, resolution	Pipeline
		10	17.7	4.6					$\Sigma \Delta$
[39]	9	40	425	1.8	6.9	5.9	0.25	Interchange stage	
[23]	6,8,10	80	94	1.8	9.1	1.9	0.13	Rates, resolution	Cyclic, pipeline
[36]	6-10	20	8	1.8	9.1	3.2	0.18	Rates	Opamp share, calibration
[16]	-	20	37	1.8	9.3	1	0.18	Rates, resolution	$\Sigma \Delta$
This work	8,10	2.5-40	35.4	2.5	9.2	1.9	0.35	Rates, resolution	Pipeline

2.3 Summary of Prior Arts

Besides the designs mentioned in the previous several sections, there are still some innovative designs, but they will not be treated in detail. The performances of the best designs are listed in table 2.1.

Since each design has different configurations, different processes and supply voltage, it is very hard to justify which one is the best, but some crude observations based on table 2.1 are listed below.

a) Design [39] consumes largest power and has the lowest ENOB. The area is also relatively large when compared with other designs. The reason is that this design can interchange stages between any two stages. More switches and wires are needed to route among stages, leading to a large area and low resolution.

b) Design [36] has the lowest power consumption. This design uses a large-scale digital calibration circuit to improve the analog performance. The OTA usually consumes most of the power in ADC for fast settling, but in design [36], small OTAs were implemented and errors caused by unsettled signals were measured with a digital circuit and finally subtracted from the digital output word.

c) This work's power consumption is not the lowest, but still very low.

d) Design [29] has the largest area. Part of the reason is that this design uses a 0.6 μm process. Another reason is due to complex configuration between pipeline and sigma-delta.

e) This work's area is not lowest, but part of the reason is to account for the large feature size of the process. The process used in this work is TSMC 0.35 μm , but the minimum size for this PDK is 0.4 μm . The area is the smallest in all designs when normalized with the process feature size.

f) The reconfigurable ADC of this work is cost-efficient due to relatively low power and small area.

2.4 ADC Figure of Merit

For traditional ADCs, figure of merit (FOM) is used to evaluate similar designs [40]. However, for reconfigurable ADCs, one ADC may have several FOM values for different configurations. Fair comparison among these ADCs remains a formidable mission. In this section, different figure of merits are first introduced. Based on the previous FOMs, a new FOM that can be used to evaluate the reconfigurable ADC is devised.

If we consider the speed and accuracy of the ADC, the basic performance metric for ADC can be defined as [41]

$$FOM1 = \frac{P}{f_s} \quad (2.1)$$

where f_s is the sampling frequency. FOM1 is mainly considering the energy consumed for one conversion. Another figure of merit, which involves the quantization steps, can

represent the power-speed-accuracy tradeoff better. It can be defined as [42]

$$FOM2 = \frac{P}{f_s \cdot 2^{ENOB}} \quad (2.2)$$

The FOM2 can be treated as “energy per conversion-step”. It is well known that for each extra bit in the resolution, the power consumption will increase four times to maintain the same speed. A figure of merit that considered this factor has been proposed as [43]

$$FOM3 = \frac{P}{f_s \cdot 2^{c \cdot ENOB}} \quad (2.3)$$

However, in practice, $c=1$ is good enough to compare ADCs over many technologies, topologies, speeds and resolutions [41].

The FOMs expressed in equation 2.2 and 2.3 only consider the power constraint for data converters. However, the area factor is also an important parameter to evaluate the cost efficiency of a data converter. For different technologies, the area for the same design will be different. The area must be normalized by its feature size in order to reflect the area efficiency. The new figure of merit is expressed in equation 2.4. It becomes obvious that the more complicated the reconfiguration, the larger the area and the smaller the FOM4.

$$FOM4 = \frac{P \cdot A}{f_s \cdot 2^{ENOB} \cdot L_{\min}^2} \quad (2.4)$$

2.5 Problems in Reconfigurable ADC

High performance ADCs are very sensitive to noise and interference. Any noise source could dominate the overall performance. Reconfigurable ADCs are more vulnerable than traditional ones due to more wires and switches for reconfiguration. For example, for an off-state switch, if the isolation of the switch is -60 dB and there is a 10 dBm signal at one terminal, one will get a -50 dBm signal at the other terminal. This interference may potentially limit the resolution one can get from an ADC. For high speed and high resolution data converters, the isolation is even worse due to the capacitive characteristic between source and drain terminals. In this work, dummy switches [44] are used to eliminate these interferences with minimum penalties.

Another important issue in conversion rate reconfiguration is how to scale the bias in OTAs for a large conversion rate ratio. Since the OTAs are usually optimized to operate in the highest conversion rate, they may not work appropriately when the bias is scaled down for lower speed because the device sizes are not scaled accordingly. A reconfigurable OTA and reconfigurable bias scheme are also developed to solve this problem.

CHAPTER 3

PIPELINE ADC ARCHITECTURE

In this chapter, the performance metrics used to evaluate the ADC converters are described in section 3.1. The conventional pipeline ADC architecture and transfer function is treated in detail in section 3.2. The important sub-circuits of the pipeline ADC are illustrated in section 3.3.

3.1 ADC Performance Metrics

3.1.1 ADC Static Performance Metrics

Due to non-ideal circuit elements in the actual implementation of ADC, the code transition points in the transfer function will be moved back and forth as illustrated in figure 3.1. The step size in the non-ideal data converter deviates from the ideal size Δ and this error is called the differential nonlinearity (DNL). The total deviation of an analog value from the ideal value is called integral nonlinearity (INL). These two parameters include the errors from quantization noise, thermal noise, flicker noise, mismatch, distortions, temperature-induced short-term drift, aging and offset.

The quantization step Δ can be expressed as

$$\Delta = \frac{V_{FS}}{2^B} \quad (3.1)$$

where V_{FS} is the full-scale input range and B is the resolution of the converter. The quantization step is the same as the voltage range of Least Significant Bit (LSB). Then the function DNL and INL can be defined as

$$DNL(i) = \frac{V_{in}(D_i) - V_{in}(D_{i-1}) - \Delta}{\Delta} \quad (3.2)$$

$$INL(i) = \sum_{k=1}^i DNL(k) \quad (3.3)$$

where $V_{in}(D_i)$ and $V_{in}(D_{i-1})$ represent the input voltage corresponding the output code D_i and D_{i-1} .

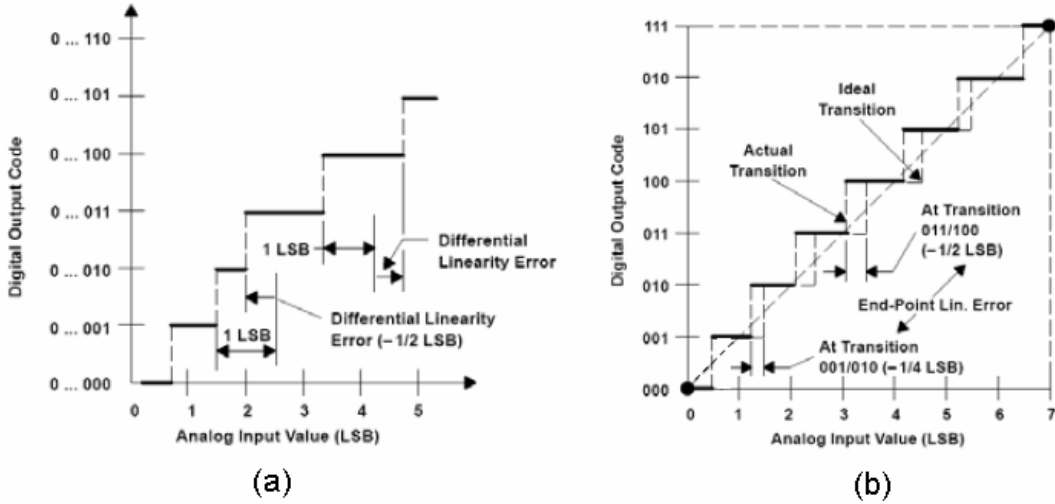


Figure 3.1 (a) Differential nonlinearity and (b) integral nonlinearity

3.1.2 ADC Dynamic Performance Metrics

3.1.2.1 Signal-to-noise Ratio

The Signal-to-noise Ratio (SNR) is the ratio of the power of the fundamental frequency and the total noise power, excluding the harmonic components. For a sinusoidal signal, the average power of maximum input amplitude is given by

$$P_s = \frac{(2^{B-1} \cdot \Delta)^2}{2} \quad (3.4)$$

where B is the bits of data converter. For a uniformly distributed spectrum of quantization noise, the variance can be expressed as

$$\bar{e}^2 = \int_{-\Delta/2}^{+\Delta/2} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12} \quad (3.5)$$

The SNR can be calculated as

$$SNR = 10 \log \frac{P_s}{\bar{e}^2} = 10 \log \frac{\frac{(2^{B-1} \cdot \Delta)^2}{2}}{\frac{\Delta^2}{12}} = 6.02B + 1.76 \text{ dB} \quad (3.6)$$

3.1.2.2 Dynamic Range

The Dynamic Range (DR) is the input power range for which the SNR is greater than zero, i.e.

$$DR = 10 \log \frac{\text{Maximum Signal Power}}{\text{Smallest Detectable Signal Power}} \quad (3.7)$$

3.1.2.3 Spurious Free Dynamic Range

The Spurious Free Dynamic Range (*SFDR*) is the ratio of the power of the signal and the power of the largest spurious frequency. It can be expressed in dBc as

$$SFDR = 10 \log \frac{\text{Signal Power}}{\text{Largest Spurious Power}} = 10 \log \frac{X_1^2}{X_s^2} \quad (3.8)$$

where X_1 is the RMS value of the fundamental frequency and X_s is the RMS value of the largest spurious frequency. The harmonic tones usually limit the *SFDR* in data converters.

3.1.2.4 Total Harmonic Distortion

The Total Harmonic Distortion (*THD*) is the ratio of the total harmonic distortion power and the power of the fundamental frequency. It can be expressed as

$$THD = 10 \log \frac{\text{Total Harmonic Distortion Power}}{\text{Signal Power}} = 10 \log \left(\frac{\sum_{i=2}^{\infty} X_i^2}{X_1^2} \right) \quad (3.9)$$

where X_i is the RMS value of the k -th harmonic component.

3.1.2.5 Signal-to-noise and Distortion Ratio and Effective Number of Bits

The Signal-to-noise and Distortion Ratio (*SNDR*) is the ratio of the power of the fundamental frequency and the total noise and distortion power. The *SNDR* is a more realistic parameter to evaluate the merit of a data converter. The relationship between

SNR and $SNDR$ can be expressed as $SNDR=SNR-THD$, where all these parameters are in their absolute values. The effective number of bits ($ENOB$) is a measure based on the $SNDR$ of an ADC with a full-scale sinusoidal input signal. They can be expressed as

$$SNDR = 10 \log \frac{\text{Signal Power}}{\text{Noise and Distortion Power}} \quad (3.10)$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (3.11)$$

3.2 Pipeline ADC Architecture

3.2.1 Conventional Pipeline ADC Architecture

The conventional pipeline ADC is illustrated in figure 3.2. The ADC has several stages, each containing a sub-ADC, a DAC, a subtractor and a residue gain amplifier. Each stage performs a sample and hold operation and a coarse analog-to-digital conversion to generate n bits digital output. The quantization result is converted back into analog domain and used to compute the residue. The quantization error (residue) was amplified 2^n times to bring the amplitude to full-scale range. The residues propagate through subsequent stages to resolve further less significant digital output. All the digital output from each stage are finally combined together to obtain the digital output.

The transfer function for a 2-stage pipeline ADC is also shown in the lower right corner of figure 3.2. Two bits are resolved for each stage. The blue line is the residue of

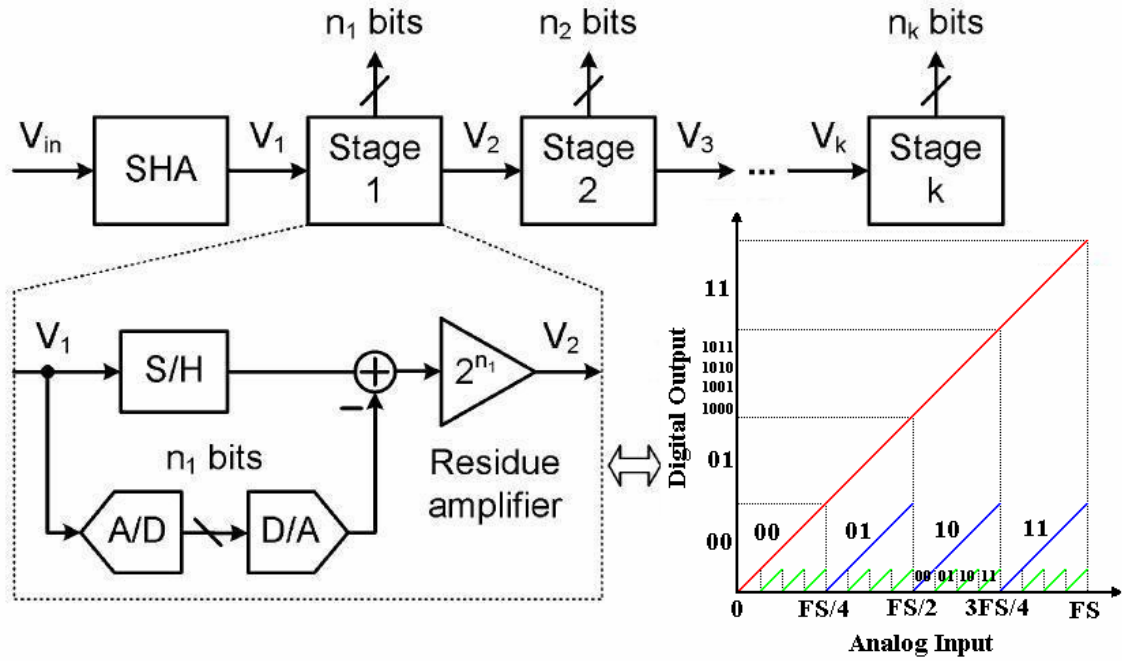


Figure 3.2 Conventional ADC Architecture and its transfer function.

the first stage and the green line is the residue of the second stage. If no amplification between each stage, the signal level will decrease 2^n times, making the latter stages susceptible to noise and interference. The quantization noise is not noise-look for a ramp input. The first reason is that the random assumption is only valid for a large amount of quantization steps. The second reason may be that the signal is not “active” enough.

How to choose the best resolution for each stage is still an unsolved problem. The number of bits per stage has a large impact on the speed, power and accuracy requirements of each stage [45]. The rule of thumb is choosing lower bits per stage for

high-speed data converters and choosing larger bits per stage for high-resolution data converters. For lower bits per stage, the sub-ADC comparators and the gain amplifier requirements are more relaxed, and the speed of each stage is faster due to smaller feedback factor for a given technology. For larger bits per stage, the matching can be relaxed for the front-end of the ADC. It can be proved that for additional bit in first stage, the DNL can be improved by 1 LSB and the INL can be increased by 0.5 LSB [46, 47]. A more detail analysis about the resolution per stage can be found in [45].

If each stage resolves only one bit, the transfer function is inherently linear. There is only one comparator required for the sub-ADC. The offset of the comparator will move the decision level from the ideal location causing saturation in the residue for the subsequent stage. One solution for this problem is introducing redundancy in the sub-ADC. One comparator is added in the sub-ADC for one more decision level. If the gain of the residue amplifier is still two, then the effective bit for this stage is still one. However, the resolution for the sub-ADC is $\log_2 3 = 1.59$. For simplicity, this architecture is usually called as 1.5b per stage architecture [45, 48, 49].

The 1.5b per stage architecture sub-ADC has two thresholds and can tolerate the offset of comparators as large as $V_{ref}/8$. Each stage resolves two bits with one bit redundancy. The transfer function of this architecture [45] is shown in figure 3.3.

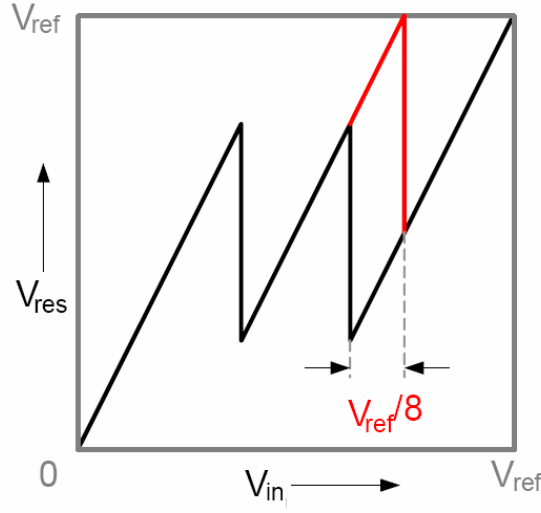


Figure 3.3 1.5b per stage architecture transfer function.

3.2.2 Pipeline ADC Analysis

Each pipeline stage has the function to resolve n bit for digital output, and then generate the residue voltage for further process. The block diagram for each stage is shown in figure 3.4a with its equivalent model in figure 3.4b. The DAC, subtraction block and gain element are usually referred as Multiplying DAC (MDAC) [50].

The residue V_{res} and digital output D can be expressed as

$$V_{res} = -G \cdot (V_{in} - V_{DAC}) = -G \cdot \varepsilon_q \quad (3.12)$$

$$D = V_{in} + \varepsilon_q \quad (3.13)$$

where ε_q is the quantization noise added by the sub-ADC.

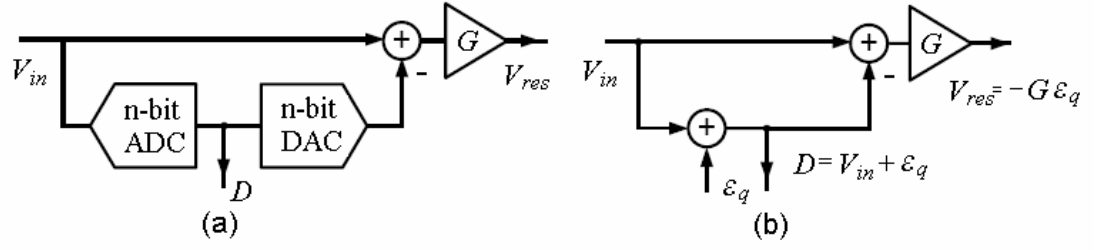


Figure 3.4 Pipeline stage block diagram (a) and its equivalent model (b).

The pipeline ADC model based on stage analysis is shown in figure 3.5. The output of the pipeline ADC is calculated by

$$D_{out} = V_{in,ADC} + \varepsilon_{q1} \left(1 - \frac{G_1}{G_{d1}}\right) + \frac{\varepsilon_{q2}}{G_{d1}} \left(1 - \frac{G_2}{G_{d2}}\right) + \dots + \frac{\varepsilon_{q(n-1)}}{\prod_{i=1}^{n-2} G_{di}} \left(1 - \frac{G_{n-1}}{G_{d(n-1)}}\right) + \frac{\varepsilon_{qn}}{\prod_{i=1}^{n-1} G_{di}} \quad (3.14)$$

where ε_i ($i=1 \sim n$) is the quantization noise added by each stage. If the analog gain G_i ($i=1 \sim n-1$) matches the digital gain G_{di} ($i=1 \sim n-1$) exactly, all the quantization noise, except the last stage, will be canceled out, leading to the digital output expression as

$$D_{out} = V_{in,ADC} + \frac{\varepsilon_{qn}}{\prod_{i=1}^{n-1} G_i} \quad (3.15)$$

$$B_{ADC} = B_n + \sum_{i=1}^{n-1} \log_2 G_i \quad (3.16)$$

where B_n is the number of bits of the last stage. Some observations from the above expressions can be summarized as follow:

- 1) The only difference between the analog input and digital output is the

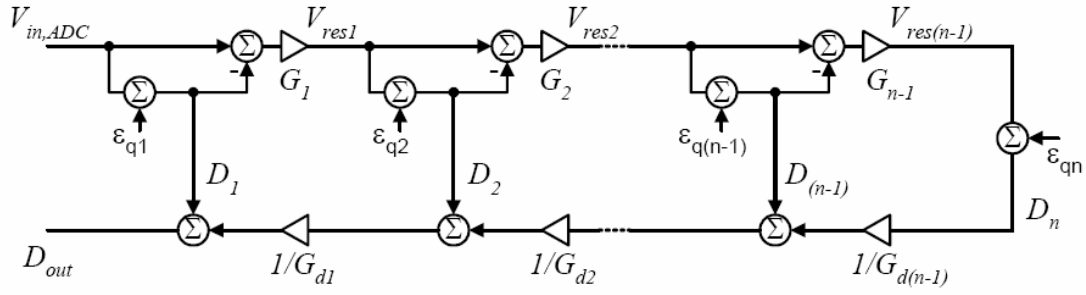


Figure 3.5 Pipeline ADC model

quantization noise from the last stage. The quantization noise is the limitation that prevents the designer getting a higher resolution in ideal analysis. In reality, one can cascade more stages in the pipeline, but the resolution usually is limited to 12 bits due to the mismatch or other noise sources. Those issues will be addressed in the next chapter.

2) The aggregate resolution is only determined by the overall gain between each stage.

The resolution by simply adding the number of bits from each stage is usually larger than the aggregate resolution due to redundancy. The redundancy can be removed by digital correction which will be addressed in chapter 6.

3.3 Sample and Hold Amplifier

Sample and Hold Amplifier (SHA) is a controversial block in pipeline ADC. In theory, it is not a required element because the gain amplifier for the first stage also have sample and hold function. Furthermore, SHA, to some extent, is not welcome because it suffers from significant power, noise, area and distortion penalties. A design example

without dedicated SHA can be found in [51]. However, in practice, a dedicated SHA was implemented to relax the dynamic requirements for the following stage. Unlike the latter stages which deal with settled DC signal, the first stage will have to process a high frequency input signal up to the Nyquist frequency (maybe even larger for down-sampling application) if no SHA exists. The comparators must distinguish the small input signal within the time period, where the change of the input signal is less than $V_{ref}/8$ for 1.5b per stage architecture. Moreover, the on-resistance of the sampling switch must be small enough to minimize the voltage drop on the switch in order to decrease the signal-dependent charge injection. A SHA can give the ADC a large tolerance to component nonidealities by providing a stable settled voltage.

3.3.1 Charge Redistribution SHA

The charge redistribution SHA [52] is shown in figure 3.6. The circuit is implemented in full differential circuit but is shown in single-ended mode for analysis. The operation of the SHA can be divided into two clock phases, the sampling phase $\Phi1$ and the hold phase $\Phi2$. The equivalent circuit for each phase is illustrated in figure 3.7.

During the sampling phase $\Phi1$, the input signal is sampled to the capacitor C_s passively. The OTA is disconnected from the input and can be used to set the common mode voltage during this half cycle. At the end of $\Phi1$, the charge stored in C_s is $V_i * C_s$.

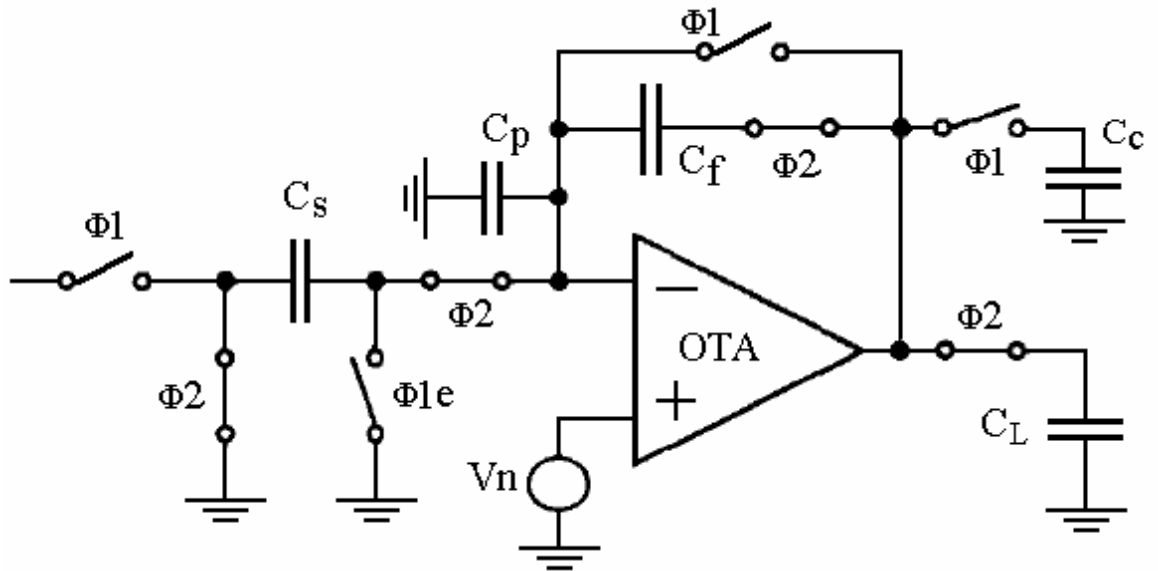


Figure 3.6 Charge redistribution Sample and hold amplifier

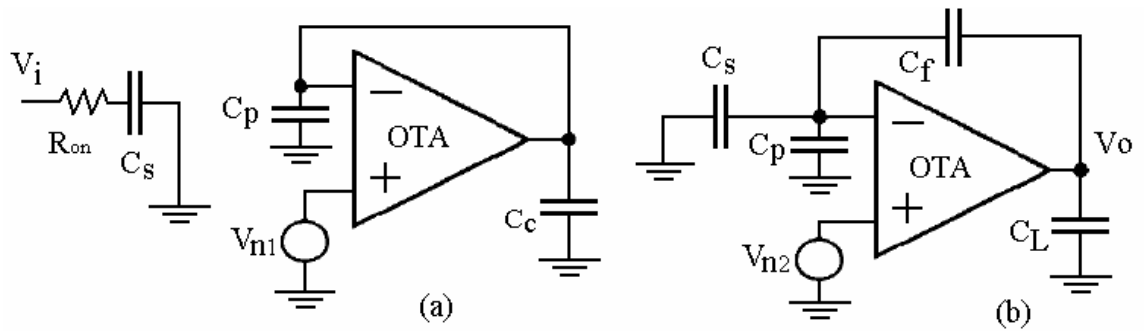


Figure 3.7 Charge redistribution SHA equivalent circuit during sampling phase (a) and hold phase (b).

During the hold phase Φ_2 , the OTA force the summing node voltage to be equal to positive input terminal except a small error voltage. The charge stored in C_s will transfer to C_f . Based on the charge conservation law, the output voltage of the OTA can be expressed as

$$V_o = V_i \frac{C_s}{C_f} \quad (3.17)$$

Unlike the flip-around SHA, the input common-mode voltage of charge redistribution SHA will not change during the transition from the sampling to the hold phase. This characteristic is particularly favored by the telescopic OTA since it does not have large Input Common Mode Range (ICMR). This will lead to a slightly larger output range and dynamic range. However, this architecture does suffer from two penalties, matching and settling [22].

Matching [53, 54] limitation is dominant in high resolution pipeline ADC. From the above expression, the gain of the SHA depends on the matching of two capacitors, C_s and C_f . For modern fine-line technologies, a 0.1% or even better matching is achievable. Unfortunately, this matching limit only allows the pipeline ADC to gain 10 bits resolution without digital calibration.

Charge redistribution SHA also suffers from slow settling when compared with

flip-around SHA. The feedback factor for clock phase $\Phi 2$ can be expressed as

$$F = \frac{C_s}{C_s + C_f + C_p} \quad (3.18)$$

and the -3 dB bandwidth of figure 3.6(b) is

$$\omega_{-3dB} = \omega_u \cdot F = \frac{g_m}{C_{Leff}} F \quad (3.19)$$

where $C_{Leff} = C_L + (1 - F)C_f$. From the equation above, one can conclude that the small feedback factor leads to a small -3 dB bandwidth, resulting in slow settling.

3.3.2 Flip-around SHA

The same capacitor is used for both sampling and hold in flip-around SHA [47, 55]. During the sampling phase $\Phi 1$, input signal is sampled into the capacitor C_s and for the hold phase $\Phi 2$, the input terminal of sampling capacitor is disconnected from the input and then connected to the output. The other terminal is disconnected from ground and connects to the OTA summing node. The flip-around SHA is shown in figure 3.8 with its two phase equivalent circuits shown in figure 3.9.

The feedback factor of the flip-around SHA hold phase $\Phi 2$ can be expressed as

$$F = \frac{C_s}{C_s + C_p} \quad (3.20)$$

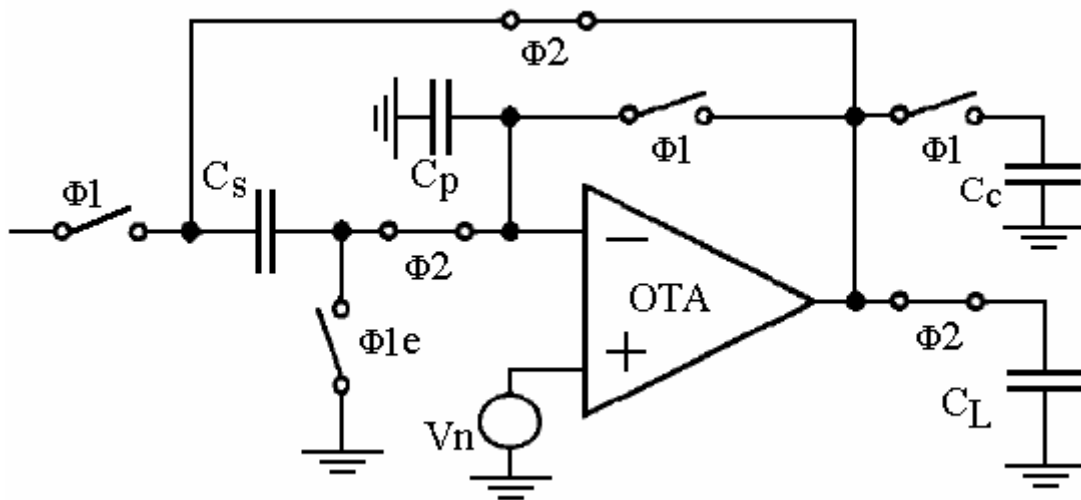


Figure 3.8 Flip-around Sample and hold amplifier.

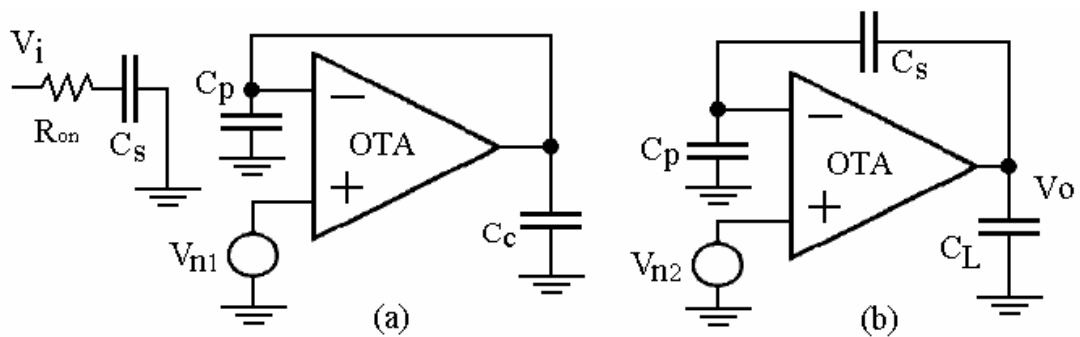


Figure 3.9 Flip-around SHA equivalent circuit during sampling phase (a) and hold phase (b).

and the -3 dB bandwidth for figure 3.9b is

$$\omega_{-3dB} = \omega_u \cdot F = \frac{g_m}{C_{Leff}} F \quad (3.21)$$

where $C_{Leff} = C_L + (1 - F)C_s$. When compared with charge redistribution SHA, flip-around SHA has a large feedback factor and a small effective load, and both leading to a fast settling.

For the flip-around SHA, the sampling and hold capacitor are the same. Therefore, there is no matching problem. However, it does suffer from a penalty. One should notice that the polarity of the capacitor would change during the transition from sampling and hold. The outcome is that the common mode voltage for the OTA input will change during the transition as well. This drawback will exclude the use of the telescopic OTA in the flip-around SHA due to lack of large $ICMR$ and $CMRR$.

3.3.3 Bootstrapped Sampling Switch

For low voltage applications, the on-resistance of the complementary switch (PMOS and NMOS pair) is very large and also signal dependent, leading to a longer settling time and a larger distortion. If there is a small battery with one terminal tied to the input signal and another terminal tied to the sampling switch gate, then there is always a fixed voltage between the gate and the source. The on-resistance of the sampling switch will keep constant and the linearity is improved. However, the gate

voltage can exceed the supply voltage, bringing more stress on the gate oxide, but this method is proved to be safe for long-term use in practice [46, 47, 56]. Since the voltage between the gate and the source is always equal to the power supply voltage, the on-resistance is small and thus a smaller NMOS transistor instead of complementary switch can be used as the sampling switch.

A charged capacitor has a similar function as of a battery, and can be used to fulfill this task. The clock boosting circuit [57, 58] is shown in figure 3.10. In this scenario, C_I is first charged to V_{DD} during the hold period, and then disconnected from the ground and the power supply at the end of the hold period, and then connected to the gate and source of the sampling switch during the sampling period. Therefore, a constant voltage is applied on the switch despite the changing of the input signal level. The waveform of the gate voltage when a sinewave is applied is shown in figure 3.11 [56].

3.4 Sub-ADC

As shown in figure 3.2, each pipeline stage contains a sub-ADC. The sub-ADC is a low-resolution flash ADC. For 1.5b per stage architecture, there are 2 comparators and 3 decision levels. The sub-ADC is illustrated in figure 3.12. When the input signal is larger than $V_{ref}/2$, the output digital code is 11. When the input signal is larger than $-V_{ref}/2$ and smaller than $V_{ref}/2$, the output digital code is 01. When the input signal is smaller than $-V_{ref}/2$, the output digital code is 00.

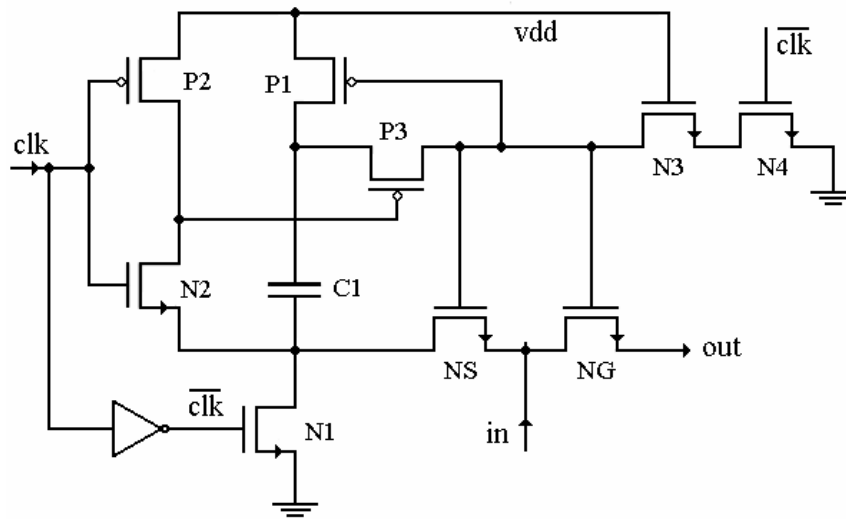


Figure 3.10 Bootstrapped clock generation circuit.

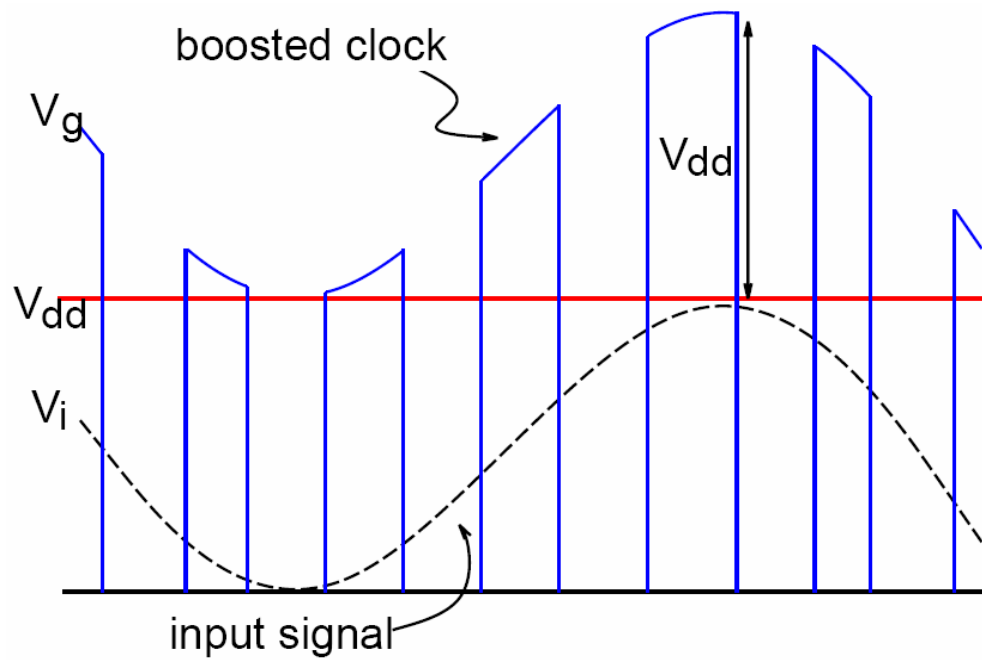


Figure 3.11 Boosted clock with the input signal.

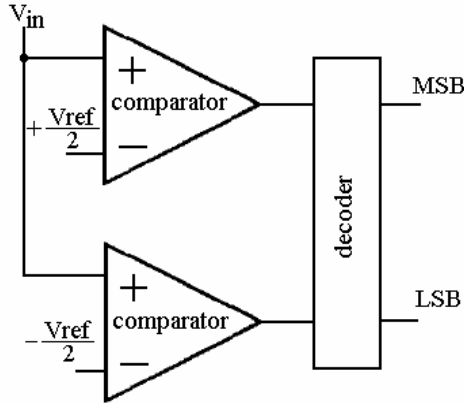


Figure 3.12 Block diagram of sub-ADC.

The analog-to-digital conversion and digital to analog conversion in each stage must finish in a half clock cycle (during the sampling phase). The speed of comparators in the sub-ADC should be very fast in order to avoid metastability. Fortunately, the offset voltage of the comparators can be as large as $V_{ref}/8$ due to the redundancy.

3.5 Multiplying DAC

As shown in figure 3.2, the circuitry including a DAC, a subtractor and a sample and hold amplifier is also referred as Multiplying DAC (MDAC) [50]. The MDAC used in this work is shown in figure 3.13.

During phase Φ_1 , the input is sampled in the two sampling capacitors C_s and C_f , and the low resolution ADC will also resolve the digital output. Then, during the hold

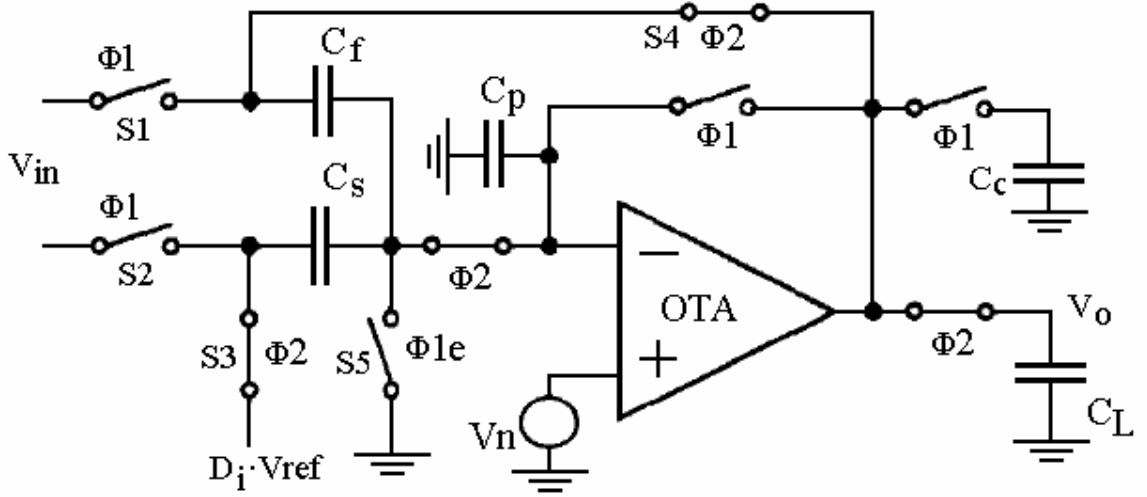


Figure 3.13 The Multiplying DAC in each pipeline stage.

phase Φ_2 , based on the ADC result, the switch S_3 will connect to $+V_{ref}$, $-V_{ref}$ or ground and the switch S_4 will connect to the output. The charge on C_s will transfer to C_f . Since the charge is conserved during these two clock periods, the expression for the output voltage can be calculated as

$$V_o = (1 + \frac{C_s}{C_f})(V_{in} - D_i \cdot \frac{V_{ref}}{2}) \quad (3.22)$$

where D_i is derived base on the sub-ADC result. If the sampling capacitors C_s is equal to C_f , the interstage gain will be equal to 2. From the above equation, the digital output is converted back to analog domain and then subtracted from the input signal, and amplified twice to obtain the residue voltage V_o .

As mentioned in section 3.2.2, the quantization noise for each stage except the last stage is cancelled out if the analog interstage gain is equal to the digital gain. The mismatch between C_s and C_f alters the gain slightly from its ideal value, thus mix the quantization from each stage to the residue signal. For a 10 bits ADC, the matching of the first pipeline stage requires a 9-bit accuracy, and for each following stage, the accuracy will relax for one more bit. These requirements usually are easy to satisfy when only matching is considered as the main error source.

CHAPTER 4

DESIGN OF RECONFIGURABLE PIPELINE ADC

In this chapter, the reconfiguration method on resolution was described in section 4.1. The problem resulting from the reconfiguration and its solving method are also treated in detail in this section. Then, the bias scaling and the reconfigurable OTA techniques for reconfiguration on conversion rate are illustrated in section 4.2.

4.1 Configuration on Resolution

As mentioned in previous chapters, two configurations on resolution are implemented with a 10-bit configuration for diagnosis mode and an 8-bit configuration for monitor mode. There are two ways to configure the ADC resolution either by turning off the last stage or the first two stages and the sample hold stage. The former method is very simple to implement and will not affect other pipeline stages. The latter one will cut the signal path and re-route the input signal to the third stage. By doing this, maximum power can be saved but extra interference can potentially degrade the performance. An analysis related with power and interference is carried out in detail.

4.1.1 Power Distribution in Pipeline Stages

In a pipeline ADC, the requirements for the sample and hold stage are the strictest and then gradually relaxed for the latter stages. For example, for a 10-bit ADC, the sample and hold output must have a 10-bit accuracy (0.1% error is allowed) and for the first stage, the output of the gain amplifier must have a 9-bit accuracy (0.2% error is allowed). In order to achieve this accuracy, a large amount of current must be pumped from the OTA to get both a large bandwidth and a large slew rate. For the latter stages, the power of OTAs can be scaled down by compromising the tradeoff between power and noise. The power consumption of each stage in this ADC is illustrated in figure 4.1. Therefore, it is advantageous to turn off the first two stages and the sample hold stage instead of the last stage in terms of power efficiency. The reconfiguration scheme is shown in figure 4.2

In figure 4.2a, the last stage does not need to generate residue. Therefore, only a two bits flash ADC is implemented. Less benefit will be achieved by turning off this stage. On the contrary, in figure 4.2b, stage 1 and 2, the two most power hungry stages, can be shut down to achieve the same function. Moreover, for low speed application, the sample and hold stage can also be eliminated due to the slow input signal, leading to further power saving.

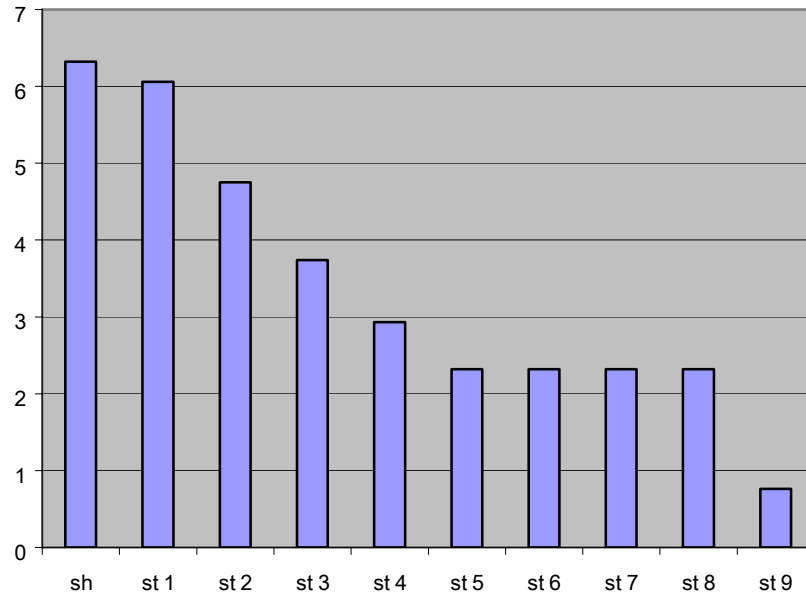


Figure 4.1 Power consumption of pipeline ADC stages.

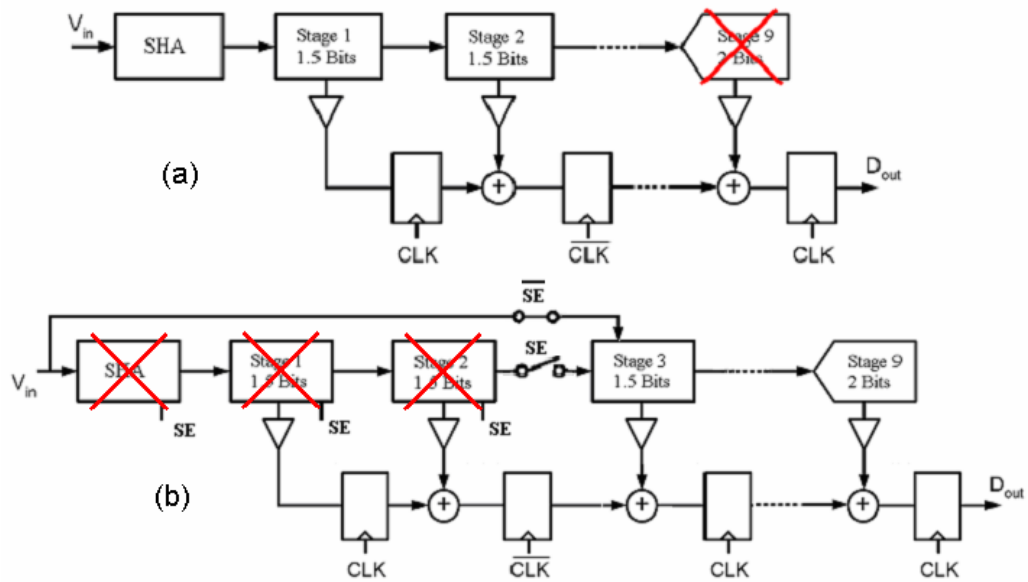


Figure 4.2 Two reconfiguration schemes for pipeline ADC.

4.1.2 Off-state Switch Model

The second reconfigurable method was chosen for its power efficiency in this work. However, extra routing switches and wires bring interferences to the third stage. In the conventional architecture, the third stage only receives a pair of differential signals (residue) from the second stage, but it will need one more input pair from the original signal for reconfiguration. Even if the switches in one pair of signals are off during a certain configuration, the signals still can leak from one terminal to another terminal.

The off switch is modeled as in figure 4.3. There are 4 parasitic capacitors associated with the switch. Two parasitic paths exist from the source terminal to the drain terminal. One path is from source to gate by C_{gs} and then gate to drain by C_{gd} . In this path, one can increase the driver size to give a better ground for the gate but it cannot increase too much due to the charge sharing in the clock boost circuit. Another path is from the source to the body by C_{bs} and then body to the drain by C_{bd} . The leakage caused by this path can be reduced by increasing the number of body contacts. The signal leakage problem will be aggravated for the high conversion rate due to the small impedance at high frequency.

Figure 4.3b shows the equivalent circuit of an off state MOS switch with the load. Z_s models the impedance seen by the off-state switch. The load includes the sampling

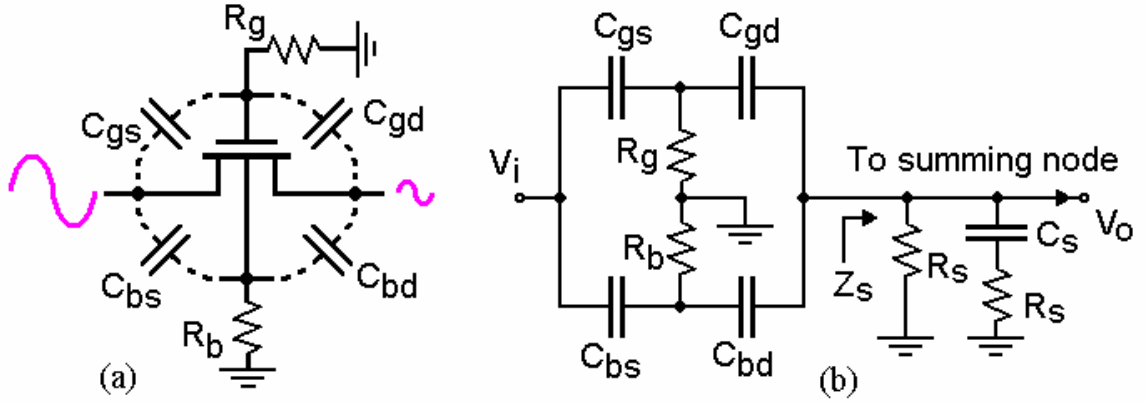


Figure 4.3 An off state switch (a) and its equivalent circuit (b).

switch, the sampling capacitor and the switch used for bottom plate sampling. The transfer function from the input to the output of the off-state switch can be expressed as

$$H_{sw}(s) = \frac{\frac{s^2 C_{gs} C_{gd}}{GA} + \frac{s^2 C_{bs} C_{bd}}{GB}}{\frac{1}{Z_s} + sC_{gd} + sC_{bd} - \frac{s^2 C_{gd}^2}{GA} - \frac{s^2 C_{bd}^2}{GB}} \quad (4.1)$$

where $Z_s = \frac{R_s(1 + sR_s C_s)}{1 + s2R_s C_s}$, $GA = \frac{1}{R_g} + sC_{gs} + sC_{gd}$, $GB = \frac{1}{R_b} + sC_{bs} + sC_{bd}$. The Matlab

simulation result indicates that the isolation of the off state switch tends to be worse for higher frequency. The simulation result is illustrated in figure 4.4.

4.1.3 Interference Elimination Techniques

Since the leakage problem cannot be avoided, a method must be devised to alleviate it. It is well known that one of the OTA's important characteristics is high input

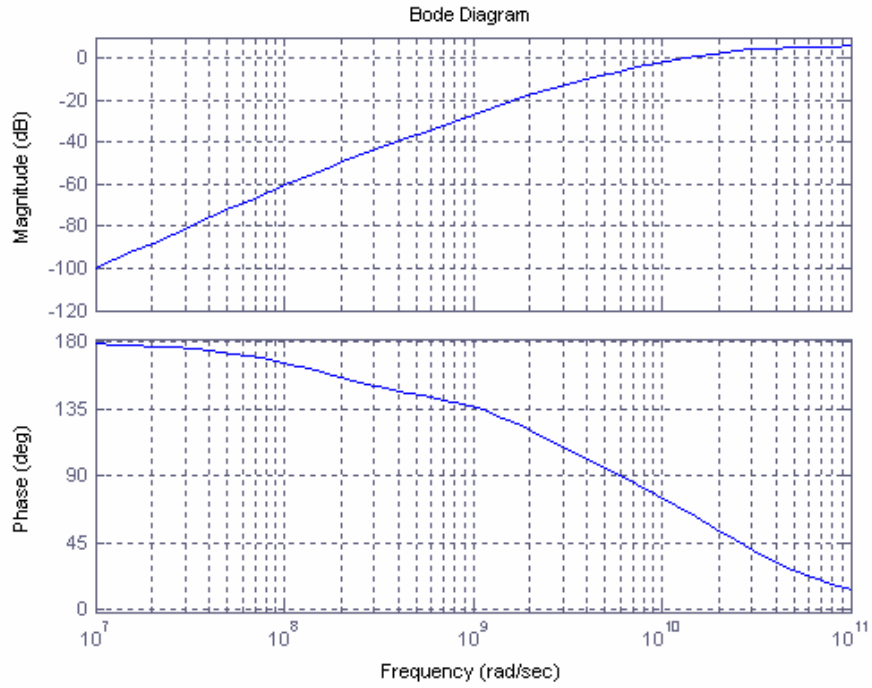


Figure 4.4 The isolation of an off-state switch versus frequency.

Common Mode Reject Ratio (*CMRR*). If the leakage signal can be converted to a common mode signal appearing on both input terminals of the OTA, the interference will be attenuated and the leakage problem of reconfiguration can be ignored. A crude estimation of the attenuation can give us a qualitative understanding of this method. If the isolation of the off switch is -50 dB (an exaggeration); the *CMRR* of OTA is 60 dB; and the signal power on the source terminal is 10 dBm (710 mV RMS for 50Ω impedance), then the interference power on the drain terminal is -100 dBm (2.32 μ V RMS for 50Ω impedance). This interference level is much smaller than the thermal noise and can be ignored.

A circuit [44] that can transfer the single-ended interference to a common mode signal is shown in figure 4.5. For the 10-bit configuration mode, the $\Phi 8b$ will turn off the main switch but part of signal 'sig8bp' still can pass through the 'off' switch, appearing on the positive terminal of the OTA. In the mean time, the same amount of signal 'sig8bp' leakage will show up on the OTA's negative terminal through an always-off dummy switch. Then, the common mode signal is rejected by the OTA. The same attenuation mechanism also happens for the signal 'sig8bn'. Figure 4.6 shows the FFT analysis before (red line) and after (blue line) interference elimination for the same input signal. The harmonic tones before interference elimination is clearly larger than the blue line, which is after interference elimination.

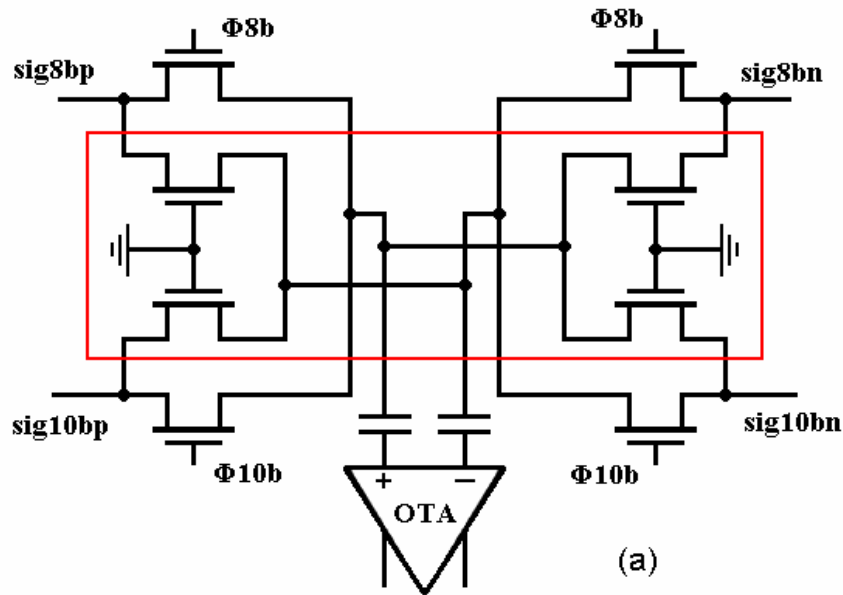


Figure 4.5 Interference elimination circuit in pipeline stage 3.

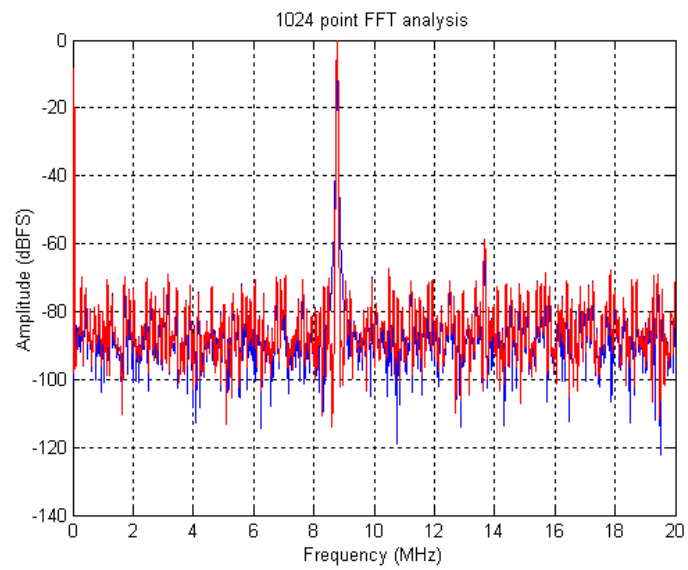


Figure 4.6 FFT analysis of the output signal before (red) and after (blue) interface elimination technique.

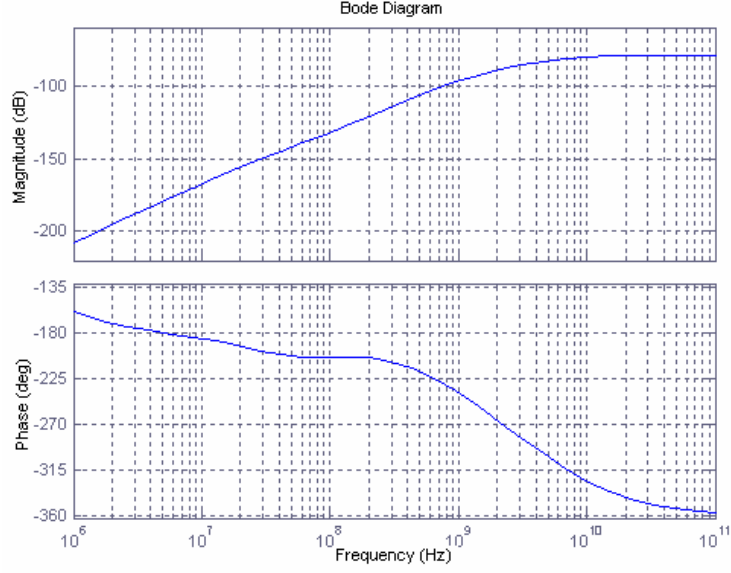


Figure 4.7 Matlab simulation result of off-state switch transfer function with OTA

The off-state switch leakage signal transfer function with OTA is expressed as

$$H(s) = H_{sw}(s)H_{CMRR}(s) = H_{sw}(s) \cdot \frac{1 + 2g_m(R_{tail} + \frac{1}{sC_p})}{\frac{\Delta g_m}{g_m} + \frac{\Delta R_o}{R_o}} \quad (4.2)$$

where the first term is the previous derived expression for off-state switch without OTA and the second term is the $CMRR$ of the OTA. The Matlab simulation result is illustrated in figure 4.7.

4.2 Configuration on Conversion Rate

4.2.1 Transconductance Efficiency and Transit Frequency Tradeoff

The OTAs in the pipeline stages are optimized for 40MSPS to achieve the best performance. When the ADC operates in the 2.5 MSPS mode, the bias current is scaled down to save power [59]. The overdrive voltage for the transistors in the OTA can be expressed as

$$V_{ov} = \sqrt{\frac{2I}{\mu C_{ox}} \cdot \frac{L}{W}} \quad (4.3)$$

If the bias current I is scaled down and the aspect ratio is still kept constant, the overdrive voltage will decrease and the operation region of MOS transistors will change from strong inversion to moderate inversion, or even to weak inversion. In figure 4.8, the green dotted line shows the $2/V_{ov}$ expressed in the above equation. However, the real transconductance efficiency (blue line) is significantly deviated from the green line when V_{ov} is smaller than 0.15 V. The reason is that for moderate or weak inversion, the square law for I-V characterization is no longer valid. The transistor acts more like a bipolar transistor other than as a MOS transistor. The expression for a transistor operating in weak inversion is described as

$$I_{ds} = I_{d0} \frac{W}{L} \exp\left(\frac{V_{gs}}{nV_T}\right) \quad (4.4)$$

$$g_m = \frac{I_{ds}}{nV_T} \quad (4.5)$$

The main difference of the above expression when compared with a bipolar

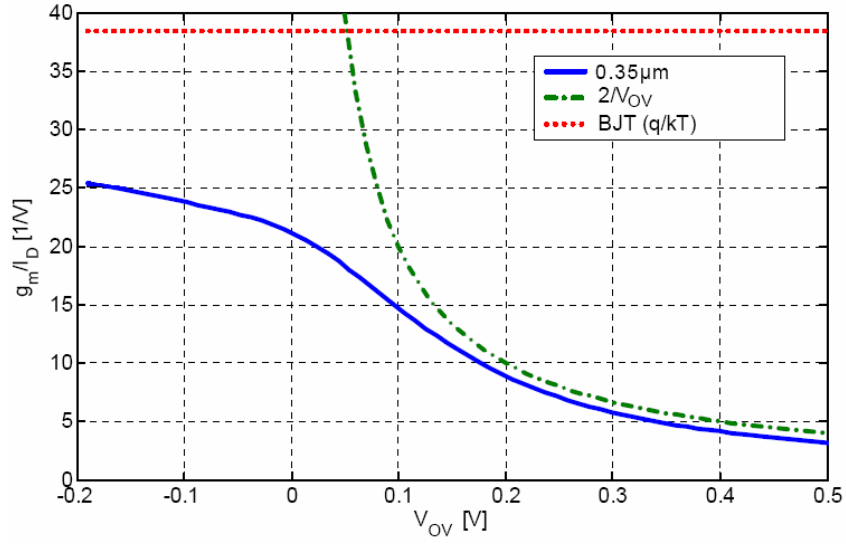


Figure 4.8 Transconductance efficiency (g_m/I_D) versus overdrive voltage in 0.35 μm process.

transistor is the extra factor n . This value depends on technologies but usually is very close to 1.5.

In the weak inversion region, the transconductance efficiency (g_m/I_D) is very high as shown in figure 4.8 [60, 61]. Low power can be achieved if the MOS transistors are biased in this region. However, the transit frequency f_T of the device degrades considerably when operating in weak inversion. The main reason is that the parasitic capacitors do not change, but the currents are decreased. The transit frequency f_T is shown in figure 4.9 with the overdrive voltage V_{ov} (also known as V_{dsat} in some other literatures).

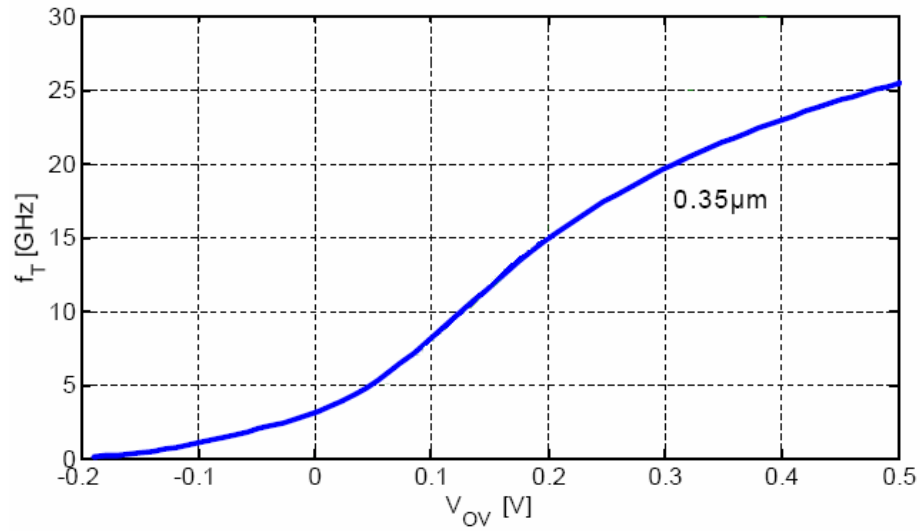


Figure 4.9 Transit frequency (f_T) versus overdrive voltage in 0.35 μm process

The tradeoff between the transconductance efficiency and the speed must be made. The optimum operating point is in the moderate inversion region. High transconductance efficiency still can be achieved without losing a significant amount of speed.

4.2.2 Reconfigurable OTA

If the MOS transistors in OTA are expected to work in moderate inversion region regardless of the bias condition, they should be sized accordingly, namely, the OTA need some kind of reconfigurability.

The OTAs in SHA and first two stages only work in high speed and high resolution mode and are turned off for low speed and low resolution application. They do

not need to be reconfigured. However, the OTAs in pipeline stage 3 through stage 8 have to work in both modes and need to be reconfigured. Unlike digital circuits which have large noise margin, analog circuits are hard to be reconfigured due to being vulnerable to noise and interference. The OTA cannot afford frequent reconfiguration due to the extra wires and switches. Therefore, the OTAs have two configurations corresponding to two operation modes of the ADC in this work. The reconfigurable OTA is illustrated in figure 4.10.

If the square law model is assumed to be still valid for the moderate-inversion operation, the aspect ratio can be calculated as

$$\frac{(\frac{W}{L})_l}{(\frac{W}{L})_h} = (\frac{V_{ov,h}}{V_{ov,l}})^2 \cdot \frac{I_l}{I_h} \quad (4.6)$$

where $(\frac{W}{L})_l$, $V_{ov,l}$ and I_l are the transistor aspect ratio, overdrive voltage and bias current for low speed mode, respectively. $(\frac{W}{L})_h$, $V_{ov,h}$ and I_h are the transistor aspect ratio, overdrive voltage and bias current for high speed mode, respectively. If the overdrive voltage is 200 mV for high-speed mode and 100 mV for low speed mode, and the bias current is scaled down by 16 times, the aspect ratio for low speed mode should be 1/4 of the high speed mode based on equation 4.6. Namely, 3/4 of the transistors should be turned off. Since the operation in moderate inversion deviate from the ideal

square law mode, some adjustment should be made based on the simulation results. However, the estimation by the above equation should be a good start point in practice.

During reconfiguration, the rules of thumb to avoid distortions and interferences are listed below.

a) No switch can be added to the signal path where large DC current will flow through. In the OTA, if we add a switch in series with the transistors, then large quiescent current will flow through this switch leading to a large voltage drop across it. In order to minimize the voltage drop, the size of the switch must be increased leading to a large parasitic capacitor. These capacitors finally limit the speed again and make the situation even worse.

b) Only PMOSs in the active load can work in weak inversion since they are not in the signal path. The nondominant poles associated with those PMOSs will also decrease but only have minor effect on the unity gain bandwidth.

c) For a MOSFET, the main parasitic capacitor is the gate to channel capacitor. The parasitic capacitor can be minimized by preventing generation of the inversion layer in the channel. In order to do that, the gates of the disabled transistors should be properly connected to a certain potential to avoid the form of inversion layer.

The topology of reconfigured OTAs in stage 3 through stage 8 is shown in figure 4.10. Gain boosting amplifiers are not used due to the relaxed accuracy requirement and

relatively large DC gains for low bias current. The device in the red rectangle will be turned off during 8-bit low speed mode.

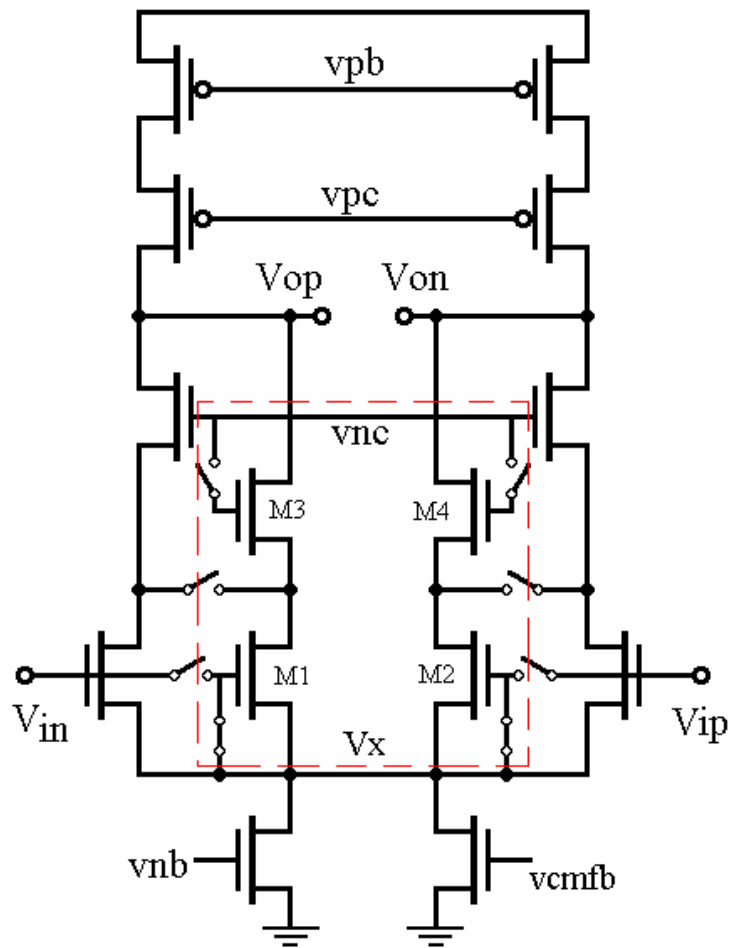


Figure 4.10 A reconfigurable telescopic cascode OTA used in stage 3 to stage 8.

CHAPTER 5

NONIDEALITIES IN RECONFIGURABLE PIPELINE ADC

In this chapter, the nonidealities in pipeline ADC are treated in great detail with the emphasis on noise and matching. The overall input referred thermal noise and flicker noise expressions are derived in section 5.1. The random mismatch of transistor and capacitors are analyzed in section 5.2. All the other nonidealities, including finite OTA gain, finite OTA bandwidth, slew rate and charge injection are discussed in section 5.3.

5.1 Noise Limitation in Reconfigurable Pipeline ADC

Noise and matching are two fundamental limitations of data converters [22]. They cannot be eliminated but can be reduced by pumping more current for lower noise and enlarge the device size for a better matching.

There are several types of noise sources appearing in the pipeline ADC. Thermal noise and flicker noise are two dominate noise sources. Thermal noise is white noise and is distributed evenly with frequency up to 1000 GHz [62]. Flicker noise, also known as

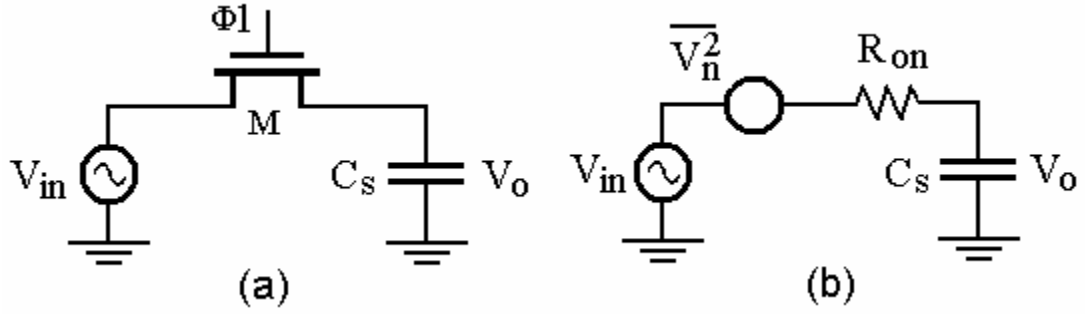


Figure 5.1 Sample and hold circuit (a) and its equivalent model during sample period.

1/f noise or pink noise, will decrease with the increasing of the frequency.

5.1.1 Thermal Noise in Pipeline ADC

5.1.1.1 Thermal Noise in Sampling Circuit

A simple sample and hold circuit is illustrated in figure 5.1a, and its equivalent model is shown in figure 5.1b. When the Switch M is off, the signal V_{in} is sampled on the capacitor C_s . However, the noise generated by the equivalent on-resistance of M is also sampled on the sampling capacitor. The thermal noise power spectral density function and the total noise voltage on the C_s can be shown as [63]

$$S(f) = 4kTR_{on} \quad (5.1)$$

$$v_n^2 = \int_0^\infty 4kT \cdot R_{on} \cdot \left| \frac{1}{1 + 2\pi f \cdot R_{on} C} \right| df = \frac{kT}{C} \quad (5.2)$$

where k is Boltzmann constant and T is absolute temperate.

From the above equation, one should know that the only way to decrease the

noise is to increase the value of the sampling capacitor and moreover, the total noise is not related to the value of the switch on-resistance. Another important observation is that since the sampling transistor is working in the triode region, the thermal noise expression is $4kTR_{on}$ instead of $\frac{8kT}{3g_m}$.

5.1.1.2 Thermal Noise in OTA

The input-referred noise spectral density of the OTA can be expressed as

$$S(f) = 2 \cdot \frac{8}{3} \cdot \frac{kT}{g_m} (1 + n_t) \quad (5.3)$$

where n_t models the noise contribution from transistors other than the input pair, g_m is the transconductance of the input transistor. Since fully differential OTAs were used in this work, the noise is doubled. In order to decrease the thermal noise in the OTA, a larger g_m is preferred for the input differential pair.

5.1.1.3 Thermal Noise in MDAC

There are two main noise sources in the MDAC shown in figure 5.2. One is from the sampling switch and another is from the OTA. The noise of the sampling switch is already sampled into the input sampling capacitor. Therefore, only the OTA noise needs to be referred back to the input. The noise voltages during the sampling period and the hold period are uncorrelated and their noise power should be added together. The equivalent circuits for different clock phase are shown in figure 5.3.

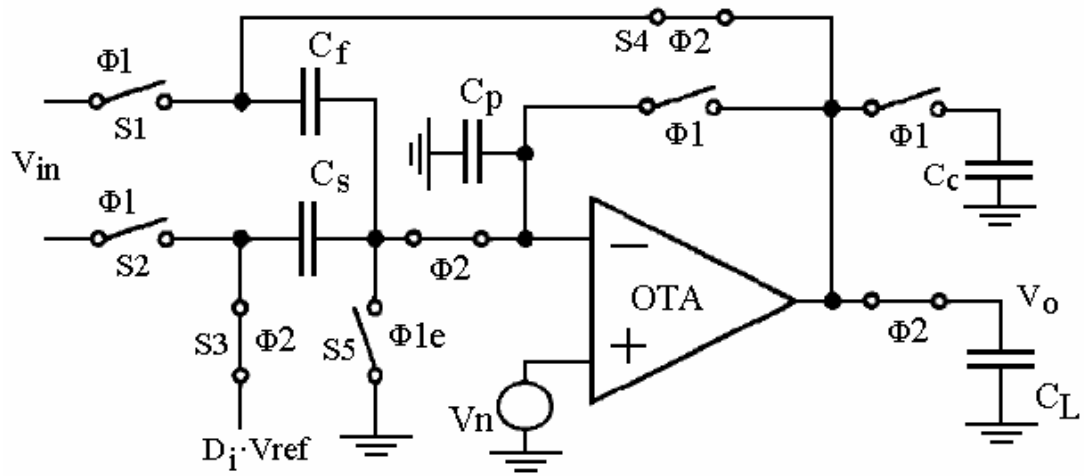


Figure 5.2 Switch capacitor MDAC in pipeline stages.

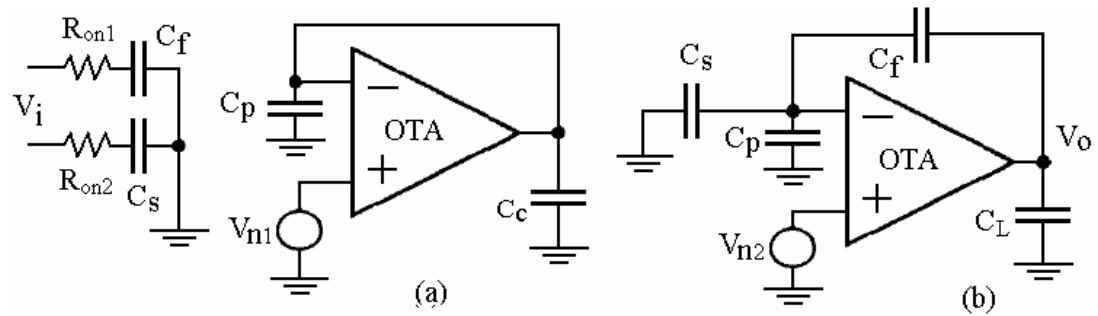


Figure 5.3 The equivalent circuit of MDAC for sampling phase (a) and for hold phase (b)

During sampling phase $\Phi 1$, the feedback factor of the OTA is $F_1=1$. The equivalent load capacitor is $C_{L,1}=C_c+C_p$. The Unity gain bandwidth for a one pole OTA is $\omega_u = g_m / C_{L,1}$. The -3 dB bandwidth is $\omega_{-3dB} = \omega_u \cdot F_1$ and the noise bandwidth is

$$BW_{n1} = \frac{\omega_{-3dB}}{4} = \frac{g_m}{4(C_p + C_c)} \quad (5.4)$$

The total noise power can be calculated as

$$v_{n,1}^2 = S(f) \cdot BW_{n1} = \frac{8}{3} \cdot \frac{kT}{g_m} (1 + n_t) \cdot \frac{g_m}{4(C_p + C_c)} = \frac{2}{3} \cdot \frac{kT}{C_p + C_c} (1 + n_t) \quad (5.5)$$

During the hold phase $\Phi 2$, the feedback factor of the OTA is $F_2 = \frac{C_f}{C_s + C_p + C_f}$.

The equivalent load capacitor is $C_{L,1}=C_L+(1-F_2)C_f$. The noise bandwidth is

$$BW_{n2} = \frac{\omega_{-3dB}}{4} = \frac{g_m}{4((1 - F_2) \cdot C_f + C_L)} \cdot F_2 \quad (5.6)$$

The total noise power can be calculated as

$$v_{n,2}^2 = \frac{8}{3} \cdot \frac{kT}{g_m} (1 + n_t) \cdot \frac{g_m}{4((1 - F_2) \cdot C_f + C_L)} \cdot F_2 = \frac{2}{3} \cdot \frac{kT}{C_L + F_2 \cdot C_p} (1 + n_t) \cdot F_2 \quad (5.7)$$

Based on the charge conservation law, the total noise voltage appearing on the output at the end of hold phase is

$$V_{n,o}(z) = \frac{1}{F_2} \cdot v_{n,2}(z) - \frac{C_p}{C_f} \cdot v_{n,1}(z) \cdot z^{-\frac{1}{2}} \quad (5.8)$$

where the first term corresponds to the output referred OTA noise during the hold phase and the second term corresponds to the output referred OTA noise during the sampling phase. As mentioned previously, these two terms are not correlated and the noise power will be added together. The noise can be referred to the input by dividing the voltage gain $1+C_s/C_f$. The input referred noise can be expressed as

$$\begin{aligned}
 v_{n,in,OTA}^2 &= \left(\frac{C_s + C_p + C_f}{C_f} \cdot \frac{1}{1 + \frac{C_s}{C_f}} \right)^2 \cdot v_{n,2}^2 + \left(\frac{C_p}{C_s} \cdot \frac{1}{1 + \frac{C_s}{C_f}} \right)^2 \cdot v_{n,1}^2 \\
 &= \frac{2}{3} (1 + n_t) \left[\frac{C_s + C_p + C_f}{C_s + C_f} \cdot \frac{C_f}{C_s + C_f} \cdot \frac{kT}{C_L + (1 - F_2) \cdot C_f} + \left(\frac{C_p}{C_s} \cdot \frac{C_f}{C_s + C_f} \right)^2 \cdot \frac{kT}{C_p + C_c} \right]
 \end{aligned} \tag{5.9}$$

From the above equation, it should be noticed that the parasitic capacitor associated with the summing node plays a very important role in the noise performance of MDAC. If the parasitic capacitor C_p is zero, then the OTA thermal noise in the sampling noise will not contribute to the total input referred noise. The OTA thermal noise in the hold phase is also smaller due to the large feedback factor. The parasitic capacitor is mainly from the C_{gs} of the input differential pair. Since the channel width of the input pair is very large in order to get a large transconductance, the C_{gs} of the input pair is comparable with the sampling and feedback capacitor.

If we count the thermal noise of the sampling switch, the input referred noise from the MDAC can be expressed as

$$v_{n,MDAC}^2 = \frac{2}{3}(1+n_t) \left[\frac{C_s + C_p + C_f}{C_s + C_f} \cdot \frac{C_f}{C_s + C_f} \cdot \frac{kT}{C_L + (1-F_2) \cdot C_f} + \left(\frac{C_p}{C_s} \cdot \frac{C_f}{C_s + C_f} \right)^2 \cdot \frac{kT}{C_p + C_c} \right] + \frac{kT}{C_s + C_f} \quad (5.10)$$

The above expression is not very meaningful for observation. A reasonable simplification can give the direction for the optimization of the noise performance. The following assumptions are given for simplification: $C_s = C_p/3 = C_f = C$, $C_c = C_L$. The load capacitor has three parts. The dominant one is the sampling capacitor of the following stage. If the pipeline stage is scaled by a factor $2/3$, this part will contribute $4C/3$. If the capacitor from the common mode feedback circuit and sub-ADC contribute $2C/3$, the load capacitor C_L is equal to $2C$. If the excessive noise factor is 0.5 for telescopic OTA, then the above expression can be rewritten as

$$v_{n,in,MDAC}^2 \approx 0.23 \cdot \frac{kT}{C} + 0.01 \cdot \frac{kT}{C} + 0.5 \cdot \frac{kT}{C} \approx 0.74 \cdot \frac{kT}{C} \quad (5.11)$$

In the above expression, the first term is the noise from the hold phase of the OTA. The second term is the noise from the sampling phase of the OTA and the third term is the noise from the sampling switch. The second term is very small and can be neglected without introducing much error.

The effects of the parasitic capacitor on the noise performance are illustrated in

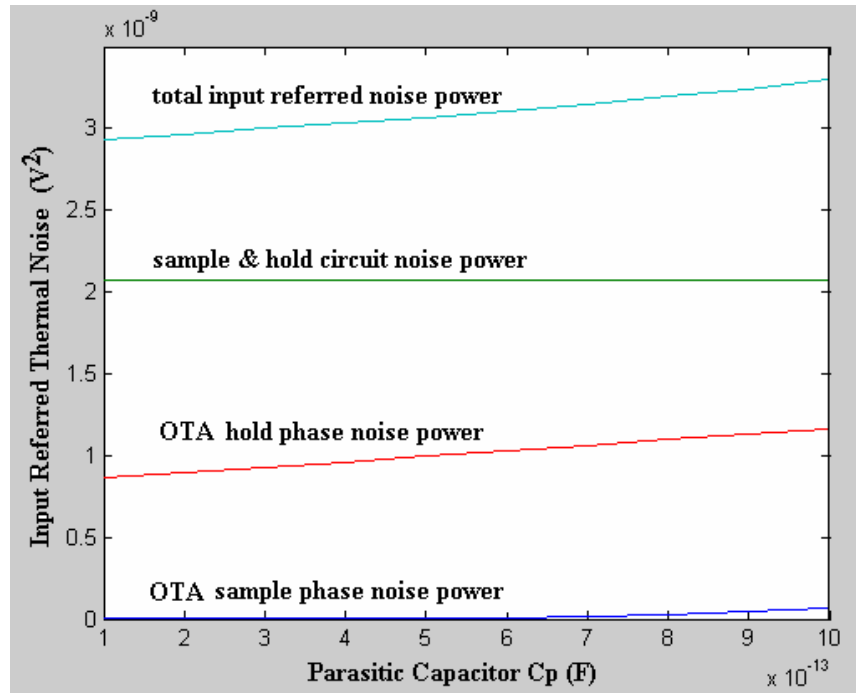


Figure 5.4 Input referred noise components in MDAC

figure 5.4. Minimizing the parasitic capacitor can improve the noise performance.

The noise analysis in this section and latter sections are based on a single ended version of fully differential structures for simplifications. The noise results should be multiplied by two for a fully differential circuit.

5.1.1.4 Thermal Noise in SHA

The thermal noise analysis in SHA is very similar with in MDAC. The flip-around SHA and its equivalent circuits are shown in figure 3.8 and 3.9 in chapter 3. The derivation for the noise performance is not repeated here and only the final result is given

$$v_{n,in,SHA}^2 = \frac{2}{3} \cdot (1 + n_t) \left[\left(1 + \frac{C_p}{C_s} \right)^2 \cdot \frac{kT}{C_L + C_p + \frac{C_p C_L}{C_s}} + \left(\frac{C_p}{C_s} \right)^2 \cdot \frac{kT}{C_p + C_c} \right] + \frac{kT}{C_s} \quad (5.12)$$

Similar assumptions can be made for the SHA. The noise factor is 1 for folded-cascode OTA. The sampling capacitor C_s is equal to $2C$ for the same noise level as the MDAC of the stage 1. The parasitic capacitor C_p is still $C/3$. C_L and C_c keep same value of stage 1 MDAC. Then the expression can be simplified as

$$v_{n,in,SHA}^2 \approx \frac{2}{3} \cdot \frac{kT}{C} + \frac{1}{63} \cdot \frac{kT}{C} + \frac{1}{2} \cdot \frac{kT}{C} \approx \frac{7}{6} \cdot \frac{kT}{C} \quad (5.13)$$

5.1.1.5 Thermal Noise in Pipeline ADC

Once the noise expressions for SHA and each stage are obtained, the overall input-referred noise can be derived. Since there is a gain (2x) between two consecutive stages, the noise contribution from latter stages will be attenuated by the gain. If the sampling capacitors are kept the same for all the stages, the noise from the last several stages is negligible, but the power efficiency is low for this scenario. If the sampling capacitor is scaled by a factor of two, each stage will have equal noise contribution and the total input referred noise is very large leading to high thermal noise level and low resolution. The detail analysis on the sampling capacitor and power scaling can be found in [38]. In this design, a factor of 0.75 was chosen to account for the tradeoff between the noise and the power. The noise mode for the pipeline ADC is illustrated in figure 5.5, and

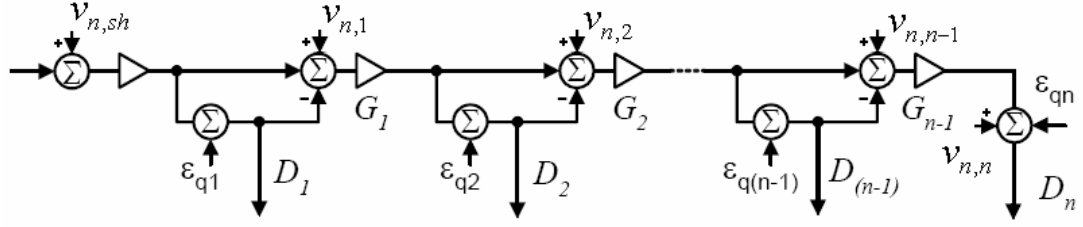


Figure 5.5 Pipeline ADC model for noise analysis.

the total input referred noise expression is given by

$$v_{n,tot}^2 = v_{n,SHA}^2 + v_{n,1}^2 + \frac{v_{n,2}^2}{G_1} + \dots + \frac{v_{n,n-1}^2}{G_{n-2}} + \frac{v_{n,n}^2}{G_{n-1}} \quad (5.14)$$

If the noise and gain in the above expression were replaced by the value calculated in the last two sections, the new expression can be given as

$$v_{n,tot}^2 = \left(\frac{7}{6} + \frac{7}{5} \sum_{n=1}^9 \left(\frac{2}{3} \right)^{n-1} \right) \cdot \frac{kT}{C} = 3.4 \cdot \frac{kT}{C} \quad (5.15)$$

The noise power should be doubled and the noise voltage is multiplied by $\sqrt{2}$ for full differential pipeline ADC.

5.1.2 Flicker Noise in Pipeline ADC

Flicker noise is the dominant noise for the low frequency range and its effects are not well discussed in the prior literature due to two reasons. First, for some communication applications, the signals are modulated on the carrier frequency and bandpass filters are usually employed to remove the flicker noise. Second, one can use

Correlated Double Sampling (CDS) technique to cancel the low frequency noise [64]. However, for some applications, which deal with wide band signals, flicker noise must be taken into account.

The input referred flicker noise power spectral density function for a MOSFET can be expressed as

$$S(f) = \frac{K_F}{C_{ox}^2 WL} \frac{1}{f} \quad (5.16)$$

where K_F is a process-dependent parameter and has a value of $10^{-32} \text{ C}^2/\text{cm}^2$ for PMOS and $4 \times 10^{-31} \text{ C}^2/\text{cm}^2$ for NMOS [65]. The flicker noise is decreased with the frequency and the corner frequency where the flicker noise is equal to the thermal noise is about 500 kHz to 1 MHz for sub-micron technologies [62]. Flicker noise is mainly due to the random trapping on the silicon surface and PMOS has a lower value than NMOS because its channel is buried under the surface.

The corner frequency can be calculated by making the thermal noise power spectral and flicker noise power spectral equal. The equation can be expressed as

$$f_c = \frac{6I_D K_F}{8kTC_{ox}^2 WL V_{ov}} \quad (5.17)$$

If all the parameters in the above expression were substituted by the parameters provided by the technology files, the corner frequency can be obtained. In this work, the

drain current of the input pair is 300 μA , C_{ox} is 0.9 fF/ μm^2 , W is 220 μm , L is 0.6 μm and V_{ov} is 200 μV . The input pair consists of PMOSFETs. The corner frequency is about 250 KHz which is very close to the value in [62]. Similarly, the corner frequency for the NMOS and PMOS in the cascode stage can be obtained as 12 MHz and 160 KHz, respectively. These values will be used as the integral upper limit for the total flicker noise.

5.1.2.1 Flicker Noise in OTA

For flicker noise, one cannot use n_t to model the noise contribution from the transistors other than the input pair because of different noise bandwidth. The derivation for the overall noise expression is very cumbersome. The flicker noise expression for the folded-cascode OTA used in SHA is expressed as

$$S(f) = \frac{K_{FP}}{C_{OX}^2 W_1 L_1} \frac{1}{f} + \frac{K_{FP}}{C_{OX}^2 W_2 L_2} \frac{1}{f} + \frac{K_{FN}}{C_{OX}^2 W_3 L_3} \frac{1}{f} \quad (5.18)$$

where the first term is the flicker noise power from the input PMOS pair, the second term is the contribution from the PMOS in cascode stage and the third term is the contribution from the NMOS in cascode stage. The flicker noise expression for the telescopic OTA used in stage 1 and 2 is expressed as

$$S(f) = \frac{K_{FN}}{C_{OX}^2 W_1 L_1} \frac{1}{f} + \frac{K_{FP}}{C_{OX}^2 W_2 L_2} \frac{1}{f} \quad (5.19)$$

where the flicker noise corner frequency is 10 MHz for the OTA NMOS input pair and

80 KHz for the PMOS of current sink load. For the OTA used in other stages, the expression is same as the above expression, but the corner frequency is 4 MHz for the NMOS input pair and 40 KHz for the PMOS load.

5.1.2.2 Flicker Noise in SHA

Similar derivations are carried out for flicker noise. The only difference between the derivation for thermal noise and flicker noise is the noise bandwidth. Since the flicker noise corner frequency is much smaller than that of the thermal noise bandwidth, the integral upper limit is the corner frequency and the lower limit cannot be zero due to no definition for zero's logarithm. Then the lower limit is set to 10^{-3} Hz (1000 seconds is a reasonable observation period for biomedical applications). The SHA circuit and its equivalent circuit are shown in figure 3.8 and 3.9 in chapter 3.

The total flicker noise power at the input terminal of the OTA during the sampling phase and hold phase are the same and can be expressed as

$$v_f^2 = \int_{f_0}^{f_1} \frac{K_{FP}}{C_{OX}^2 W_1 L_1} \frac{1}{f} df + \int_{f_0}^{f_2} \frac{K_{FP}}{C_{OX}^2 W_2 L_2} \frac{1}{f} df + \int_{f_0}^{f_3} \frac{K_{FN}}{C_{OX}^2 W_3 L_3} \frac{1}{f} df \quad (5.20)$$

by substituting $f_0=10^{-3}$ Hz, $f_1=250$ KHz, $f_2=160$ KHz and $f_3=12$ MHz into the above expression. The new expression is expressed as

$$v_f^2 \approx \frac{19K_{FP}}{C_{OX}^2 W_1 L_1} \left(1 + \frac{W_1 L_1}{W_2 L_2} + \frac{19}{23} \frac{W_1 L_1}{W_3 L_3} \frac{K_{FN}}{K_{FP}}\right) \quad (5.21)$$

Based on the charge conservation law, the total noise voltage appeared on the

output at the end of hold phase is

$$V_{n,o}(z) = \frac{1}{F_2} \cdot v_{f,2}(z) - \frac{C_p}{C_s} \cdot v_{f,1}(z) \cdot z^{-\frac{1}{2}} \quad (5.22)$$

where the first term corresponds to the output referred OTA noise during hold phase and the second term corresponds to the output referred OTA noise during the sampling phase. Unlike the thermal noise, the flicker noise is a low frequency noise. The noise during sampling phase and hold phase are closely related. If the sampling frequency is much higher than the flicker noise corner frequency, the noise will be partially cancelled out. If the flicker noise phase shift during the sample and hold phase are neglected (a little bit optimistic). Then, the above expression can be rewritten as

$$V_{n,o} = \frac{C_s + C_p}{C_s} \cdot v_{f,2} - \frac{C_p}{C_s} \cdot v_{f,1} = v_f \quad (5.23)$$

Since the gain for SHA is equal to 1, the input referred flicker noise power is v_f^2 .

5.1.2.3 Flicker Noise in MDAC

The MDAC circuit and its equivalent circuit are shown in figure 5.2 and 5.3. The flicker noise expressions during the sampling phase and hold phase are same and can be expressed as

$$v_f^2 = \int_{f_0}^{f_1} \frac{K_{FN}}{C_{OX}^2 W_1 L_1} \frac{1}{f} df + \int_{f_0}^{f_2} \frac{K_{FP}}{C_{OX}^2 W_2 L_2} \frac{1}{f} df = \frac{K_{FN}}{C_{OX}^2 W_1 L_1} \ln \frac{f_1}{f_0} + \frac{K_{FP}}{C_{OX}^2 W_2 L_2} \ln \frac{f_2}{f_0} \quad (5.24)$$

since the flicker noise during the sampling phase and hold phase are correlated, the

flicker noise voltage at the output can be expressed as

$$V_{n,o} = \frac{C_s + C_p + C_f}{C_s} \cdot v_f - \frac{C_p}{C_s} \cdot v_f = \frac{C_s + C_f}{C_s} \cdot v_f \quad (5.25)$$

The noise can be referred back to the input by dividing the gain of MDAC. The gain is $1 + C_s/C_f$.

$$v_{n,f,in} = \frac{C_f}{C_s} \cdot v_f = v_f \quad (5.26)$$

5.1.2.4 Flicker Noise in pipeline ADC

Once the flicker noise for each stage and the sample hold stage are known, they can be referred back to the input of the ADC. Another way to calculate the input referred flicker noise is to normalize the flicker noise of each stage with the thermal noise of this stage and then add a factor to thermal noise, and then refer back to the input.

5.1.3 Thermal Noise and Quantization Noise

These two kinds of noise essentially do not have any relationship. Quantization noise is only dependent on resolution. Thermal noise can be increased or decreased by design. However, the most power-efficient optimum point is to make them equal. Therefore, the overall SNR will decrease by 3 dB, about a 0.5-bit loss. If one tries to invest 4X power to cut the noise by half, an extra 0.1~0.2 bit may be gained. If the thermal noise is two times larger, a 0.5 bit may be lost. In other words, both over and

under design are costly. If other noise sources and nonidealities are also considered, a 9.0~9.2 ENOB out of 10 bits can be achieved with the maximum power efficiency.

5.2 Matching Limitation in Reconfigurable Pipeline ADC

The mismatch has been modeled using a statistical analysis which treats the errors as random variables. All of the models have assumed that the errors were random, uncorrelated and normally distributed. Systematic mismatch is assumed to be eliminated by design techniques and will not be considered here.

5.2.1 Mismatch Model in Transistors

Due to its random nature, the mismatch is usually described in terms of variance. The most widely accepted description of the variation in some parameter P between two “identical” rectangular devices could be expressed as [21, 53, 54]

$$\sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_p^2 \cdot D^2 \quad (5.27)$$

where A_p is a dimension parameter, S_p is a space parameter, and D is the distance between the two devices. Once the process-dependent constants A_p and S_p have been measured, this relationship can be used to predict matching characteristics of various devices. The mismatch due to distance is proved to be very small [53]. Therefore, the second term in the above expression can be neglected.

There are two important parameters for a MOS transistor. They are threshold voltage V_T and gain factor K . The mismatch of these parameters should be considered as the main sources of mismatch. Threshold voltage mismatch is mainly due to oxide thickness, substrate doping, etc. Gain factor mismatch is a result of differences in oxide thickness and mobility. Its typical value can be as high as 10% [65]. The threshold voltage mismatch can be described by

$$\sigma^2(V_T) = \frac{A_{V_T}^2}{WL} \quad (5.28)$$

where $A_{V_T}^2$ is a process dependent parameter and obtained by experiment. The gain factor includes both the K' (μC_{ox}) and the transistor dimensions W and L . The variance can be written as

$$\frac{\sigma^2(K)}{K^2} = \frac{A_K^2}{WL} + A_{KWL}^2 \left(\frac{1}{W^2} + \frac{1}{L^2} \right) \quad (5.29)$$

5.2.2 Current Mirror Mismatch

In fully differential OTA, properly biased current mirrors act like active load for the cascode amplifier. The mismatch between the current mirror transistors induce current mismatch for different branches. Since the OTA is fully differential, there is no systematic mismatch between the two branches. For two transistors in a current mirror, mismatch is indicated by ΔV_T and ΔK . The relative variation in the output current $\Delta I_o/I_o$ is more interesting. The variation of current I_o can be calculated by

$$\Delta I_o = g_m \Delta V_T + \frac{\Delta K}{K} I_o \quad (5.30)$$

Since in strong inversion, g_m can be expressed as $2I_o/V_{ov}$, the normalized output current variation can be expressed as

$$\frac{\Delta I_o}{I_o} = \frac{2}{V_{ov}} \Delta V_T + \frac{\Delta K}{K} \quad (5.31)$$

If one wants to make the current variation small, the transistors must be biased at large values of V_{ov} . Namely, the transistors need to work in strong inversion, and the W/L ratio should be small for a given amount of current.

5.2.3 Offset Voltage due to Mismatch

The offset voltage of a fully differential OTA is caused by several factors. First one is the mismatch of the threshold voltage and the gain factor of input pair. The second one is the mismatch of the threshold voltage and the gain factor of current mirror load.

The offset voltage induced by the input pair can be expressed as

$$V_{os1} = \Delta V_{T,in} + \frac{V_{ov,in}}{2} \frac{\Delta K_{in}}{K_{in}} \quad (5.32)$$

where the subscript *in* means the input pair. From the equation 5.32, one can draw an opposite conclusion that the bigger the overdrive voltage, the smaller the offset. The current mismatch in the active current mirror load will also introduce offset voltage to the input. The mismatch current obtained in the previous section will be referred back by the

transconductance of the input pair. Then the offset caused by the current mismatch can be expressed as

$$V_{os2} = \frac{\Delta I_o}{g_{m,in}} = \frac{V_{ov,in}}{V_{ov,cm}} \Delta V_{T,cm} + \frac{V_{ov,in}}{2} \frac{\Delta K_{cm}}{K_{cm}} \quad (5.33)$$

where the sub-script *cm* means current mirror. The overall offset of an OTA is the addition of the two offset voltages and is expressed as

$$V_{os} = \Delta V_{T,in} + \frac{V_{ov,in}}{V_{ov,cm}} \Delta V_{T,cm} + \frac{V_{ov,in}}{2} \left(\frac{\Delta K_{in}}{K_{in}} + \frac{\Delta K_{cm}}{K_{cm}} \right) \quad (5.34)$$

if the ΔV_T and ΔK are substituted with the expression defined in section 5.2.1, the more fundamental expression for offset voltage is described as

$$\begin{aligned} \sigma^2(V_{os}) = & \frac{A_{V_{T,in}}^2}{W_{in} L_{in}} + \left(\frac{V_{ov,in}}{V_{ov,cm}} \right)^2 \cdot \frac{A_{V_{T,cm}}^2}{W_{cm} L_{cm}} + \\ & \left(\frac{V_{ov,in}}{2} \right)^2 \cdot \left(\frac{A_{K_{in}}^2}{W_{in} L_{in}} + A_{KWL_{in}}^2 \left(\frac{1}{W_{in}^2} + \frac{1}{L_{in}^2} \right) + \frac{A_{K_{cm}}^2}{W_{cm} L_{cm}} + A_{KWL_{cm}}^2 \left(\frac{1}{W_{cm}^2} + \frac{1}{L_{cm}^2} \right) \right) \end{aligned} \quad (5.35)$$

for a given process, A_{V_T} , A_{KWL} and A_K is fixed. The only thing one can do to minimize the offset voltage is altering the aspect ratio of the input pair and current mirror load. Increasing the area of the input pair can decrease the offset caused by the threshold mismatch. Increasing the W/L ratio of the input pair will decrease the overdrive voltage and then lead to a smaller offset. Increasing the overdrive voltage of the current mirror load can also reduce the offset. Fortunately, all this methods used to decrease the offset have the same optimum directions as decreasing the overall noise performance.

5.2.4 Capacitor Mismatch

For two identical capacitors, similar expressions can be obtained. A 0.1% or better matching can normally be achieved for 0.35 μm CMOS process. This matching can lead to a 10-bit data converter without using an expensive trimming process. Like noise in ADC, capacitor mismatch is also due to random variation and is a fundamental limitation for ADC performance. However, mismatch between sampling and feedback capacitors can be decreased or even eliminated by digital calibration.

5.3 Other Nonidealities in Reconfigurable ADC

5.3.1 Error Caused by Finite OTA Gain

For an ideal OTA, the close loop gain is set exactly by the passive components in the feedback network. If the OTA gain is finite, the gain will deviate from the ideal value determined by the loop gain T . In the sample and hold amplifier of MDAC (shown in figure 5.6), the close loop gain can be calculated as

$$A_{v,CL} = \frac{V_o}{V_i} = -\frac{C_s}{C_f} \cdot \frac{1}{1 + \frac{1}{F \cdot A_v}} \cong -\frac{C_s}{C_f} \left(1 - \frac{1}{F \cdot A_v}\right) \quad (5.36)$$

where $F = \frac{C_f}{C_s + C_f + C_p}$ is feedback factor, $A_v = \frac{V_o}{V_s}$ is open loop gain. For the last step

in the above expression, a Taylor series expansion is applied and all the higher terms are omitted.

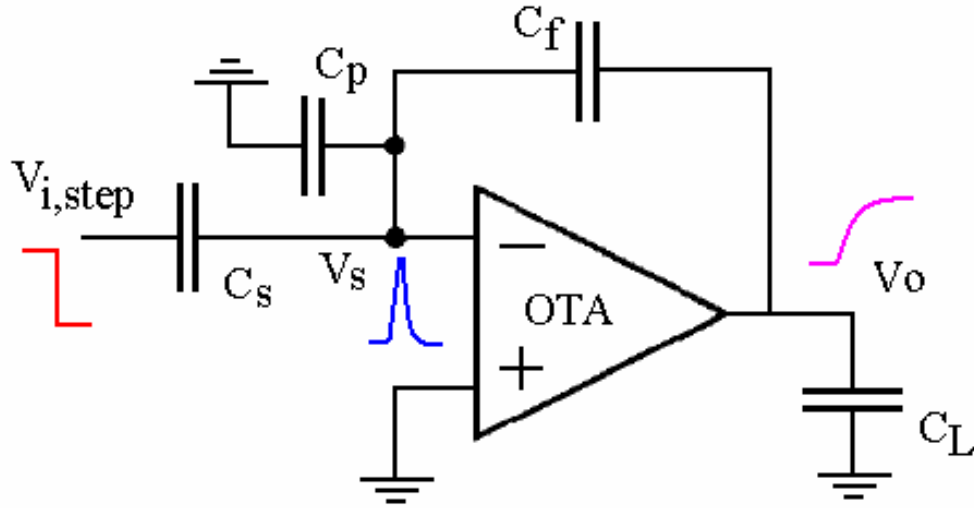


Figure 5.6 Sample and hold amplifier in MDAC

If the open loop gain A_V is finite, and then the loop gain T ($T = FA_V$) is even smaller. Close loop gain will deviate from its ideal value by $1/T$. Recall the D_{out} equation 3.14 in 3.2.2. If the analog path gain is not equal to the digital path gain, the quantization noise from each stage cannot be totally canceled out. More distortion will be brought to the residues and subsequently the final result. The completely settled signal is shown with the ideal closed loop gain in figure 5.7. The static error should be smaller than 0.1% for a 10-bits converter. If 0.03% error is allocated for static error due to finite OTA gain, and also assumes $C_s = C_f = C_p$, the minimum OTA open loop gain is 80 dB [66]. The OTA gain can be decreased for the latter stage due to the relaxed accuracy requirement. For the SHA and the first two pipeline stages, gain boost techniques are used to boost the gain. Gain boost techniques are not used for stage 3 to stage 9.

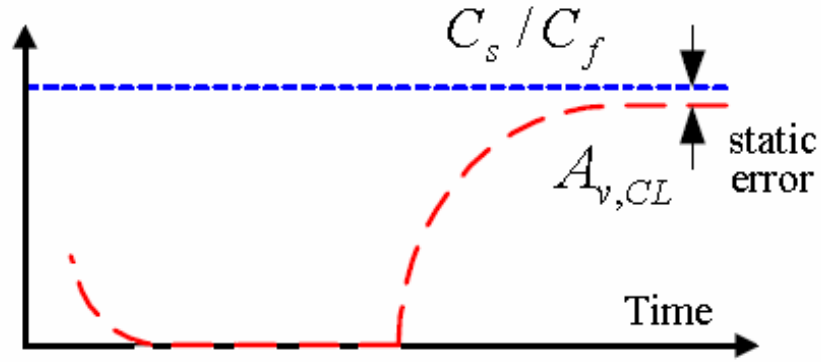


Figure 5.7 Static error due to finite OTA gain

The OTA open loop gains for different pipeline stages are listed in table 5.1 based on several assumptions. The first assumption is that only the errors caused by finite OTA gain are considered in this table. Therefore, these values are the minimum value for each OTA and a much larger OTA gain may be needed for precision settling. Another assumption is that the feedback factor is assumed to be $1/3$.

5.3.2 Error Caused by Finite OTA Bandwidth

For a finite OTA bandwidth, the signal may not be completely settled at the end of the sampling period. The unsettled signal will increase the gain error. This error also should be smaller than 0.1%. For a linear one pole settling (this is true for the OTA used in this work), the output voltage is given by

Table 5.1 Minimum DC gain requirements for 7~10b 40MSPS ADC

B	ε	OTA (A_v) (dB)
7	0.00781	52
8	0.00391	58
9	0.00195	64
10	0.00098	70

$$V_o(t) = -V_{i,step} \cdot \frac{C_s}{C_f} \cdot (1 - e^{-t_s/\tau}) \quad (5.37)$$

and $\varepsilon = e^{-t_s/\tau}$, where t_s is half period of sampling clock, $\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{F \cdot \omega_u}$, ω_{-3dB} is -3 dB bandwidth of the closed loop amplifier, and ω_u is the unity gain bandwidth of the open loop amplifier. For a 40 MSPS data converter, the bandwidth requirements for OTA are listed in table 5.2.

5.3.3 Error Caused by OTA Slew Rate

The results in the previous section are valid if the settling is entirely linear, but for most practical cases, the settling is slew rate limited. If slewing happens, the -3 dB bandwidth must be higher to compensate the time loss during slewing. For the circuit in figure 5.6, if a voltage step is applied on the input, then the output step is

Table 5.2 Minimum Bandwidth requirements for 7~10b 40MSPS ADC

B	ε	t_s/τ	OTA (f_u) (MHz)
7	0.00781	4.85	186
8	0.00391	5.54	212
9	0.00195	6.24	239
10	0.00098	6.93	265

$$V_o(t) = -V_{i,step} \cdot \frac{C_s}{C_f} \quad (5.38)$$

The voltage step at the summing node of the OTA is $V_s = FV_o$. Once V_s is larger than the overdrive voltage of the input pair, slewing begins [63]. In a typical pipeline converter, V_o is usually more than 1 V and F is about 1/3, so V_s is around 330 mV. The overdrive voltage of input differential pair is usually 150 mV~200 mV. Therefore, slewing is unavoidable in 1.5b per stage architecture.

5.3.4 Error Caused by Charge Injection

A conducting MOS switch has a large amount of mobile charge stored in its channel. This charge is distributed between source and drain terminals based on the impedance seen by it during the transistor turning off [67-69]. Moreover, the injected charge is also signal dependent. Bottom plate sampling is used to alleviate this problem.

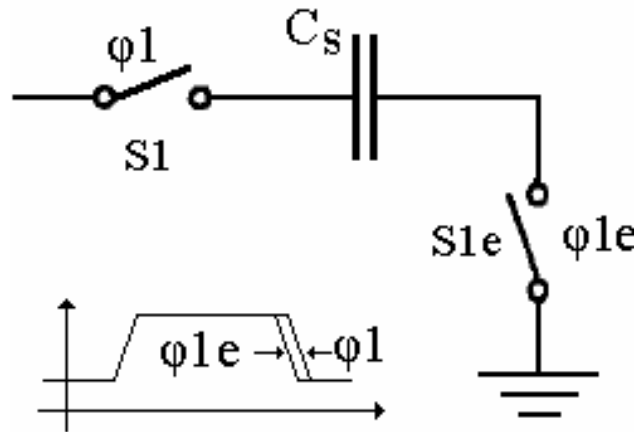


Figure 5.8 Bottom plate sampling and its timing diagram.

The model for bottom plate sampling is shown in figure 5.8.

First, the switch $S1e$ is turned off. The charge stored in the channel will inject into sampling capacitor C_s , but since the switch is grounded, the amount of charge injected is fixed. Then turn off switch $S1$, no charge will inject into C_s because the bottom plate of the capacitor is floating.

For a fully differential circuit, the equal amount injected charge appears on both terminals of the OTA and thus is rejected. The fully differential bottom plate sampling circuit implementation is illustrated in figure 5.9.

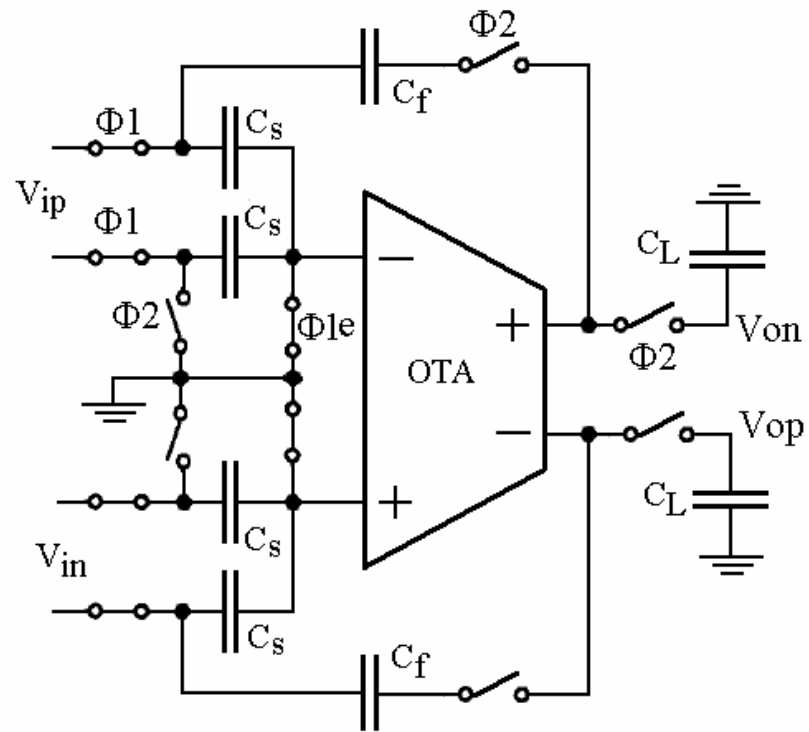


Figure 5.9 Fully differential implementation of bottom plate sampling.

CHAPTER 6

PROTOTYPE IMPLEMENTATION

For switch capacitor data converters, OTAs and comparators are the fundamental building blocks. They are treated in great detail in section 6.1 and section 6.2, respectively. Bias generation and distribution networks are also very important and will be described in section 6.3. The digital correction circuit to remove the redundancy in the digital code is illustrated in section 6.4. Some important rules about layout design are listed in section 6.5.

6.1 OTA Design

As mentioned in the previous chapters, the performance of OTAs has a significant impact on the overall performance of data converters. The open loop gain, small signal bandwidth, large signal slew rate, output range and input CMRR must be maximized under certain power and area constraints. On the contrary, the equivalent input referred noise should be minimized.

6.1.1 Folded Cascode OTA in SHA

In this work, three different OTAs are implemented to fit different stage requirements. A gain-booster folded cascode OTA was implemented for the sample and hold stage. This selection was based on the sample and hold topology. The flip-around sample and hold circuit will change its input common mode voltage during the transition from the sample period to the hold period. The telescopic OTA is not suitable due to its small input common range. Since sample and hold stage is in front of all pipeline stages, it is worthwhile to use a folded cascode OTA and invest more power to improve its performance. The OTA used in the sample and hold stage is shown in figure 6.1.

There are two disadvantages to use folded cascode OTAs. The first one is power penalty. The folded cascode OTA consumes twice the power than its telescopic counterpart to get the same symmetrical slew rate. The other penalty is larger excess noise factor n_t . For the circuit shown in figure 6.1, both M3 and M5 contribute excess noise. Therefore, it is a good practice to make the transconductance of M3 and M5 small to reduce the excess noise factor without degrading the output range. However, the bias for this OTA is easier to design and the input common range and CMRR are larger.

For the 0.35 μm process used in this work, the intrinsic gain ($g_m r_o$) is roughly 15~20 for 250 mV~300 mV V_{DS} . The overall gain is about $(g_m r_o)^2$, namely, 52 dB without gain boosting. This value is too small for high resolution data converters. The gain can be

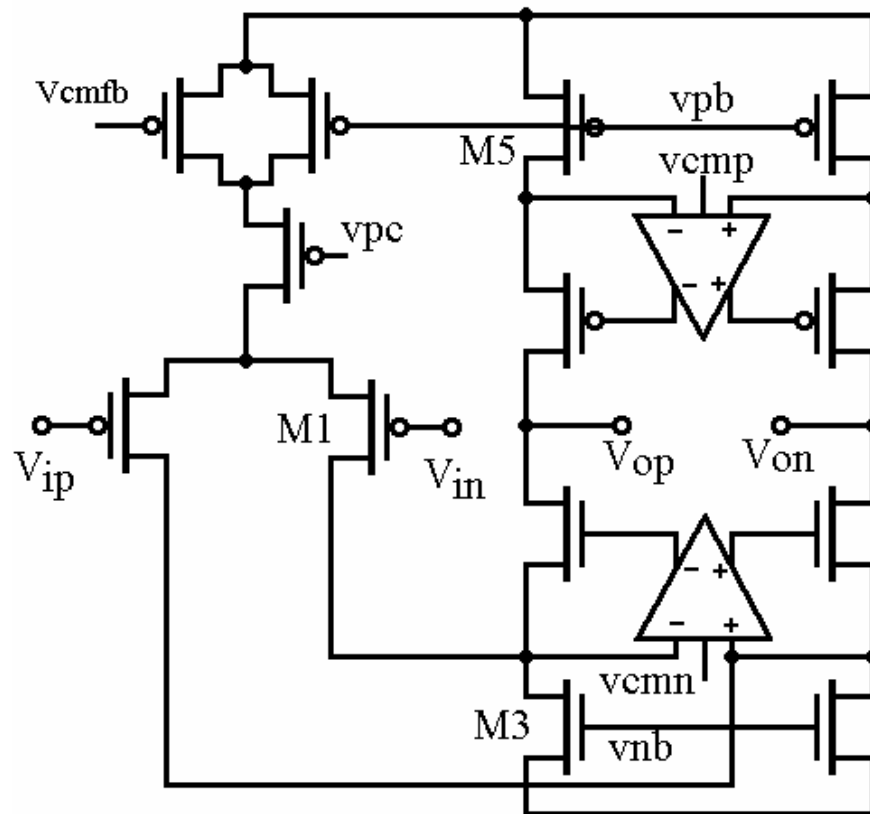


Figure 6.1 A folded cascode OTA used in sample and hold stage.

improved to $(g_m r_o)^4$, namely, 104 dB with the aid of gain boosting technique [70]. One drawback of the gain boosting technique is the potential slow settling due to the doublet, but one can always eliminate it by moving the doublet to some place where it is larger than closed loop -3dB bandwidth and smaller than open loop nondominant pole [70]. The gain boosting amplifier is also a folded cascode OTA but with a smaller bias current.

The input common mode range is roughly from zero to $V_{DD} - V_{tp} - 3V_{ovp}$. The output common mode range is from $2V_{ovn}$ to $V_{DD} - 2V_{ovp}$. The unity gain bandwidth is expressed as

$$\omega_u = \frac{g_{m1}}{C_L} \quad (6.1)$$

where C_L is the output load capacitor which is not shown in figure 6.1. The slew rate is given by

$$SR = \frac{I_b}{C_L} \quad (6.2)$$

where I_b is the bias current for the input differential pair. The dynamic settling is limited by either small signal bandwidth or large signal slew rate whichever is smaller. For linear one pole settling, in order to avoiding slewing, the slew rate must be larger than the maximum slope at the output [22], i.e.

$$SR \geq \frac{d}{dt} V_o(t) = V_{step} \cdot \beta \cdot \omega_u \quad (6.3)$$

The equation 6.3 can be rearranged to get a better understanding of the condition to avoid slewing.

$$\frac{SR}{V_{step} \cdot \omega_u} = \frac{\frac{I_b}{C_L}}{V_{step} \cdot \frac{g_{m1}}{C_L}} = \frac{\frac{I_b}{g_{m1}}}{V_{step}} = \frac{V_{ov1}}{V_{step}} \geq \beta \quad (6.4)$$

This constraint is hard to be satisfied because the input transistor is usually biased at low overdrive voltage to get larger transconductance. Therefore, slewing is unavoidable.

The input referred noise spectral density function is given by

$$S(f) = \frac{8}{3} kT \cdot \frac{1}{g_{m1}} (1 + n_t) = \frac{8}{3} kT \cdot \frac{1}{g_{m1}} \left(1 + \frac{g_{m3} + g_{m5}}{g_{m1}}\right) = \frac{8}{3} kT \cdot V_{ov1} \left(1 + \frac{V_{ov1}}{V_{ov3}} + \frac{V_{ov1}}{V_{ov5}}\right) \quad (6.5)$$

In order to minimize the noise, the transconductance of input transistors should be maximized and the transconductance of M3 and M5 should be minimized. If equal currents are flowing through M1, M3 and M5, overdrive voltage can be used to optimize the noise performance of the OTA as well.

For a fully differential OTA, a Common Mode Feedback (CMFB) circuit is required to stabilize the output common mode voltage. For the main amplifier, a switch capacitor CMFB circuit is used for a large output range. The switch capacitor CMFB circuit is shown in figure 6.2. The value of C_1 and C_2 in CMFB is chosen in such a way

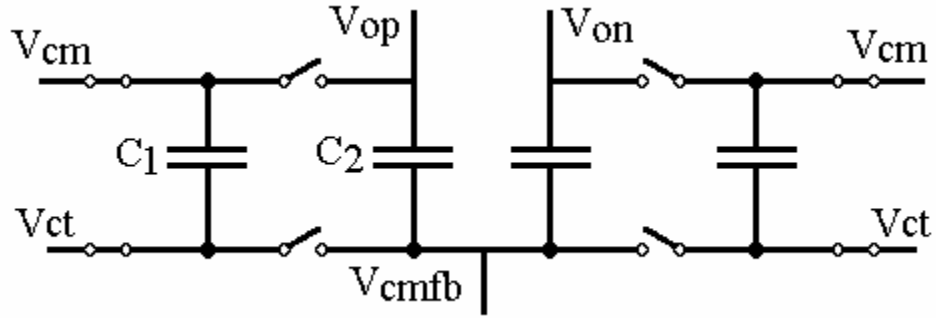


Figure 6.2 Switch capacitor common mode feedback circuit.

that they will not significantly load the OTA and also maintain a large loop gain for common mode feedback path. A continuous time CMFB circuit [71] is implemented in the gain-boosting amplifier since large output range is not required.

The bias circuit for folded cascode OTA is illustrated in figure 6.3. The two currents are originated from the global bias generation circuit which will be introduced in section 6.3. v_{pc} (v_{cmp}) is the output common mode voltage for the PMOS booster. v_{nc} (v_{cmn}) is the output common mode voltage for the NMOS booster. v_{ct} is the reference voltage for the switch mode CMFB. The simulated frequency response bode plots are shown in figure 6.4.

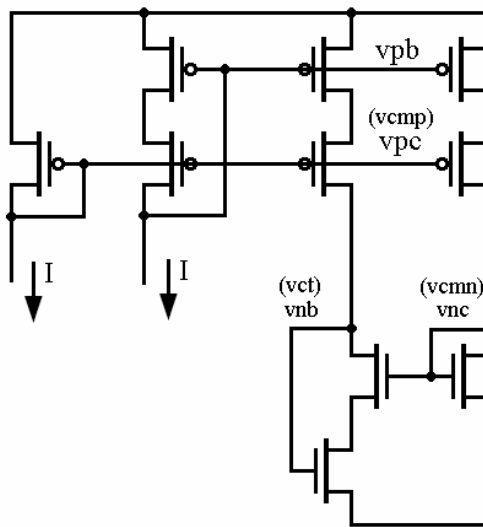


Figure 6.3 Bias circuit for folded cascode OTA

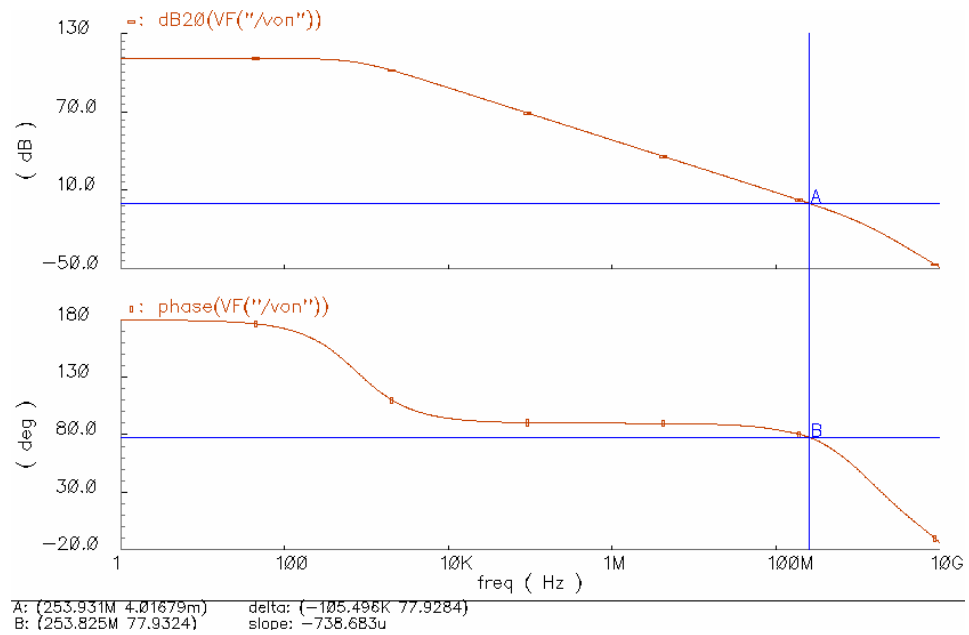


Figure 6.4 bode plot of folded cascode OTA for 4 pF load.

6.1.2 Telescopic Cascode OTA in First Two Pipeline Stages

In the first and second pipeline stages, telescopic cascode OTAs with gain boosting are implemented. There are 5 transistors stacked from the power rail to the ground rail in this architecture. The output range is about 300 mV smaller than the folded cascode OTA, but fortunately, the excess noise factor is much smaller than the folded cascode OTA. Therefore, the overall dynamic range (DR) of a telescopic cascode OTA is larger than the folded one. The telescopic cascode OTA circuit is shown in figure 6.5.

The input common mode range is roughly from $2V_{ovn} + V_{tn}$ to $V_{op(n)} + V_{tn} - V_{ovn}$. This range could be very small when output swing is large. The output common mode range is from $3V_{ovn}$ to $V_{DD} - 2V_{ovp}$. The unity gain bandwidth is still expressed as

$$\omega_u = \frac{g_{m1}}{C_L} \quad (6.6)$$

where C_L is the output load capacitor which is not shown in figure 6.5. The slew rate is given by

$$SR = \frac{I_b}{C_L} \quad (6.7)$$

where I_b is the bias current for the input differential pair.

The input referred noise spectral density function is given by

$$S(f) = \frac{8}{3} kT \cdot \frac{1}{g_{m1}} (1 + n_t) = \frac{8}{3} kT \cdot \frac{1}{g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}}\right) = \frac{8}{3} kT \cdot V_{ov1} \left(1 + \frac{V_{ov1}}{V_{ov3}}\right) \quad (6.8)$$

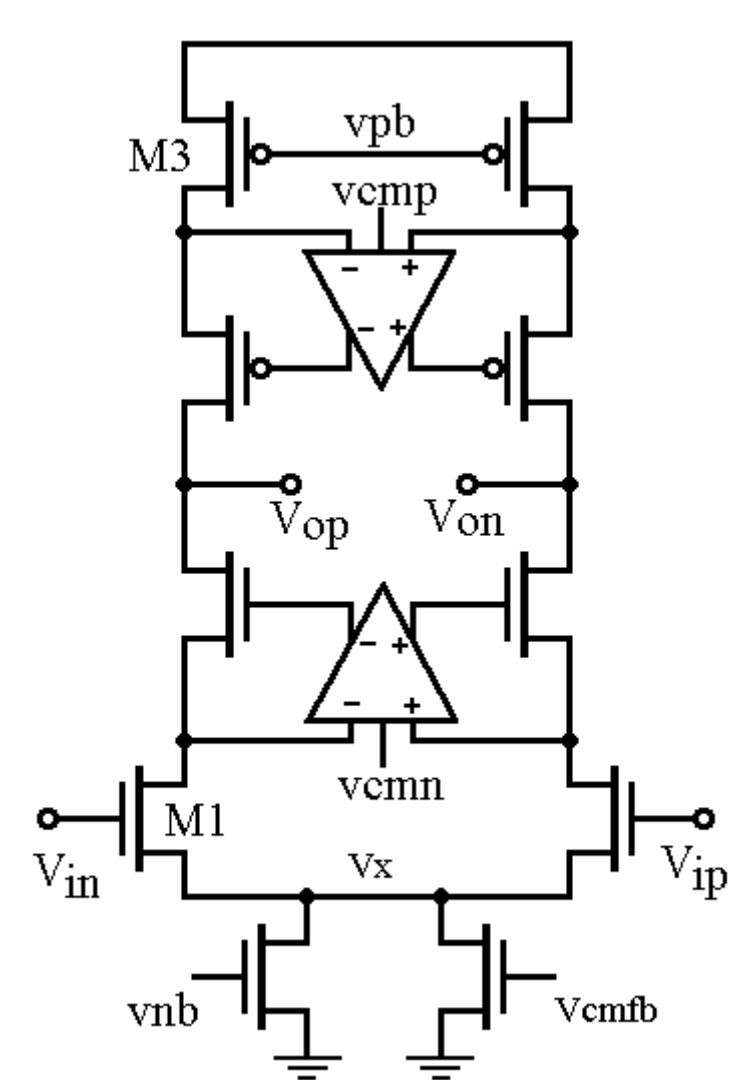


Figure 6.5 A telescopic cascode OTA used in stage 1 and 2.

It is obvious that the noise factor for telescopic OTA is smaller than folded OTA from equation 6.8.

The bias circuit for the telescopic OTA shown in figure 6.6 is more complicated than the folded OTA. Since the bias voltage for the low side cascode transistor is floated and changes with the input common mode voltage, this bias voltage must have the ability to track the input common mode change. In figure 6.6, v_{cmn} is the common mode voltage for the NMOS booster, v_{cmp} is the common mode voltage for the PMOS booster, v_{ct} is the reference voltage for the switch mode CMFB and V_X is the common source node of the input differential pair which can track the input common mode voltage.

The simulated parameters of OTAs in section 6.1.1 and 6.1.2 are illustrated in table 6.1.

6.1.3 Reconfigurable Telescopic Cascode OTA

The design of reconfigurable OTA has been described in section 4.2.1 and will not be discussed here. The bias circuit of the reconfigurable ADC also needs to change its aspect ratio to accommodate the bias current change. The bias current is scaled down 16 times and the aspect ratio for the NMOS transistors only shrinks 4 times. The overdrive voltage is about 100 mV and the NMOS transistors are operating in moderate inversion.

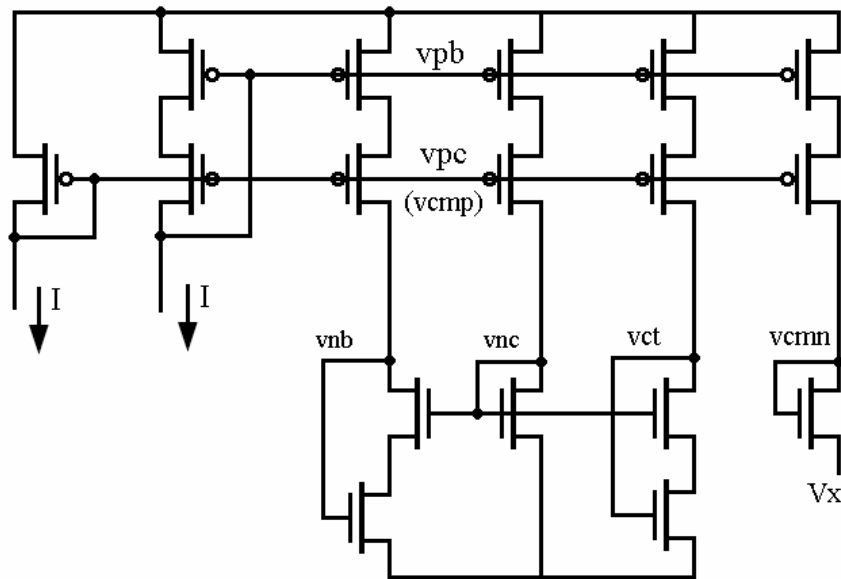


Figure 6.6 Bias circuit for telescopic OTA

Table 6.1 Comparison between folded cascode OTA and telescopic cascode OTA

	Folded cascode OTA	Telescopic cascode OTA
A_v (dB)	104	117
f_u (MHz)	254*	309*
PM (°)	78	76
nt	1.25	0.52
DR (dB)	75	73
Power (mW)	5.6	3.3

* test results with 4pF load capacitor and 2.5 V power supply.

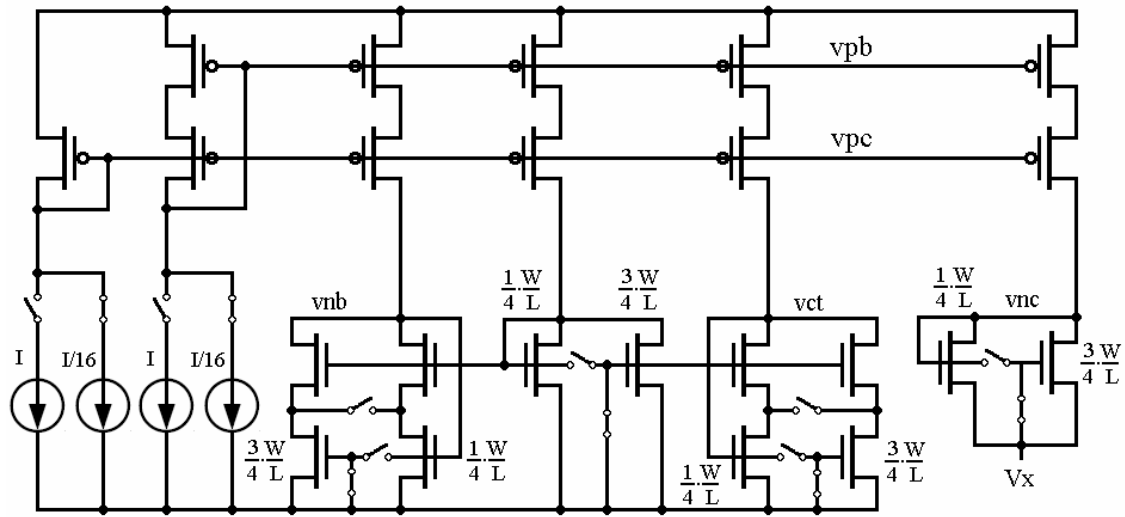


Figure 6.7 Bias circuit for reconfigurable OTA.

The principles for the reconfiguration are still applied here. The reconfigurable bias circuit is shown in figure 6.7.

6.2 Comparator Design

High performance comparators should have the ability to amplify a small input voltage to a level large enough to be detected by digital circuits within a short time [22]. Therefore, both high gain and high bandwidth is needed. These two requirements are usually contradictory. High gain yields low bandwidth and vice versa. Fortunately, unlike OTA, comparators do not need feedback and therefore have no stability problem. One can always use several cascaded low gain stages to get a large gain and fast speed.

Positive feedback latches can improve the gain and speed dramatically but their input offsets are relatively large, in the range of 15~25 mV. Therefore, the best architecture for comparators is several low gain cascaded pre-amplifiers followed by a digital latch [72]. For pre-amplifiers, the overall gain is the multiplication of individual stage gain as shown in equation 6.9 and the speed decreases with stage number linearly instead of exponentially as shown in equation 6.10.

$$A = \prod_{i=1}^n A_i \quad (6.9)$$

$$\tau = \sum_{i=1}^n \frac{A_i}{\omega_{ui}} = \frac{n \cdot A_0}{\omega_{u0}} \quad (6.10)$$

Metastability will happen when the output of pre-amplifier is smaller than the offset of the latch. A gain of 16~20 for the pre-amplifiers is large enough to avoid metastability. The comparator used in this work is shown in figure 6.8.

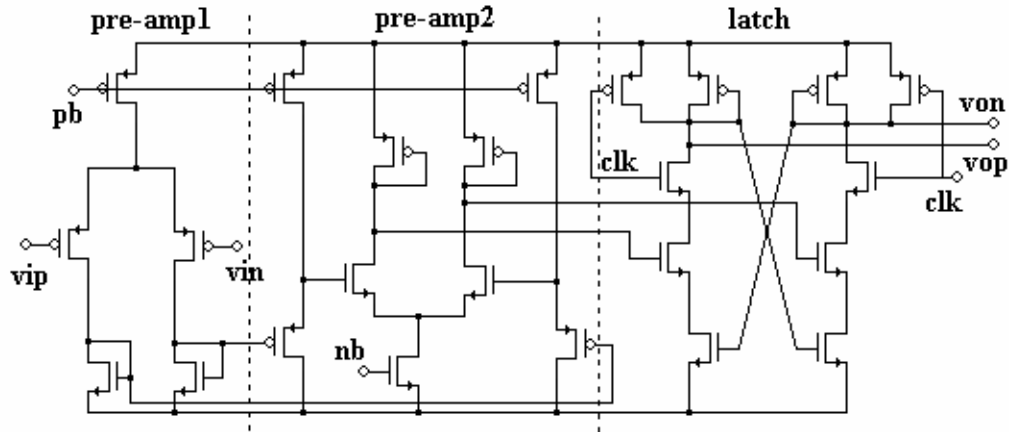


Figure 6.8 A comparator used in sub flash ADC.

6.3 Global Bias Generation and Distribution

For all the pipeline stages, the biases are from the same source. The quality of this current source affects all the OTAs' performance. The circuit shown in figure 6.9 is used to generate the current reference. The voltage at the negative input terminal of OTA is a bandgap voltage reference. The current flow through the resistor R is given by v_{cmi}/R . Since the on-chip resistor can have as large as $\pm 20\sim 30\%$ deviation and large temperature coefficient, an off-chip resistor is used to achieve a stable current reference.

It is advantageous to deliver current instead of voltage over long distance due to voltage drop and interference. The current is mirrored and distributed to each pipeline stage by the distribution network. The distribution network is shown in figure 6.10.

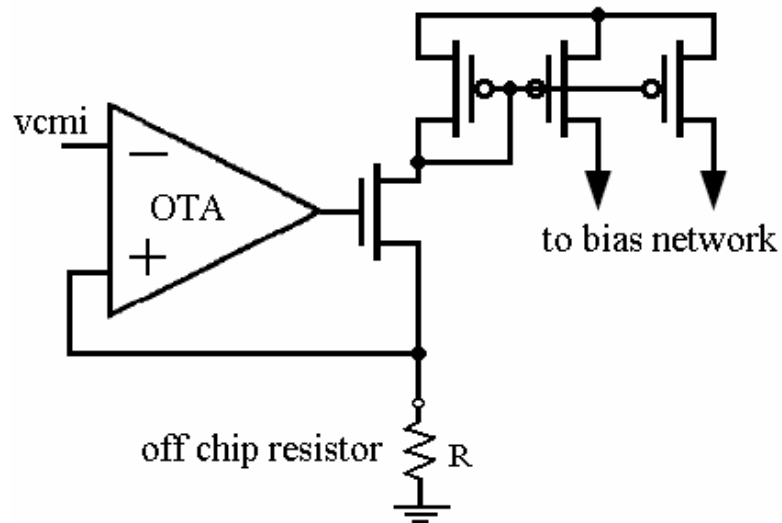


Figure 6.9 Reconfigurable bias generation circuit.

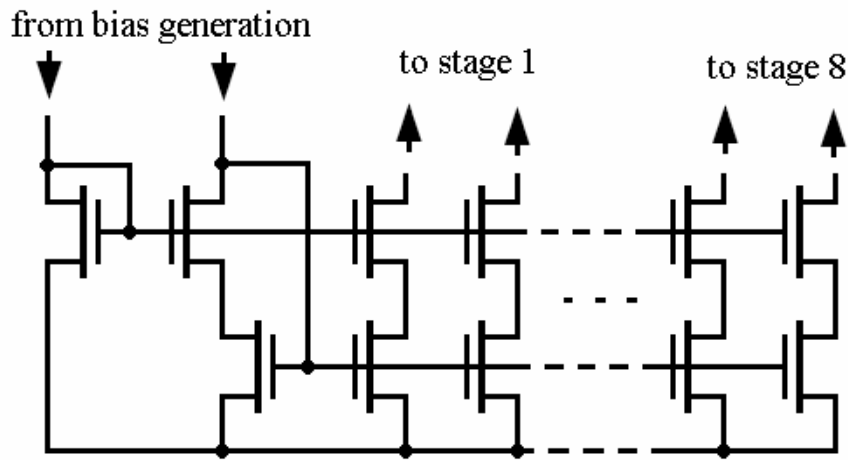


Figure 6.10 Bias replica and distribution.

6.4 Digital Correction

For a 1.5b per stage architecture, the digital output lines coming out of each stage are two in number but the effective bit is only one. Therefore, there is some redundancy in the digital output code. Digital correction circuit [73] can be used to remove the redundancy, but before correction can be made, delays must be added to the digital output of the previous stages to remove the timing skew. In figure 6.11, the first and second stages need delay 5 clock cycles for a 10-bit data converter. The third and fourth stages need delay 4 clock cycles and the later stages have similar delay procedures. Therefore, the final digital output is valid 5 clocks later than the analog input. This is one of the drawbacks of pipeline ADCs. A 10 bits full adder is implemented to remove the redundancy. Since the propagation of the carry is fast, no carry look-ahead structure is used in the adder design.

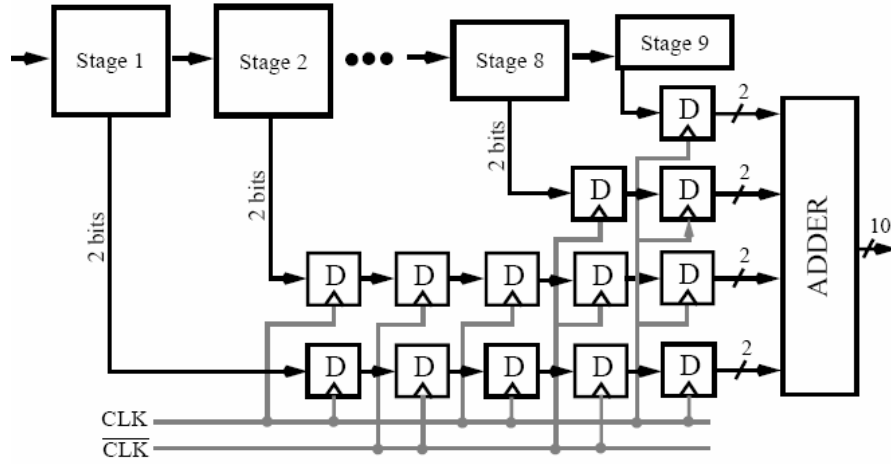


Figure 6.11 Digital correction circuit.

6.5 Layout Design

The layout design is very critical in the implementation of a data converter. The first step is a floorplan under a specific area constraint. A small, compact layout is always favored due to the high cost of silicon real estate. The data converter can be partitioned into analog part and digital part. These two parts are placed well separated. Moreover, in each pipeline stage, the sub-ADC is considered as a digital circuit and the residue gain amplifier is a very sensitive analog circuit. These two blocks are placed on each side of the sampling and feedback capacitors.

The global clock and bias are placed in the middle of the data converter. Since pipeline stages are relatively independent, they can be put together sequentially. Four global reference signals, V_{cmi} , V_{cmo} , V_{refp} , V_{refn} , are routed around the pipeline stages. The

line width of these four signals is very wide since they will carry a significant amount of current during settling. These metal lines are composed of several small metal lines connected to each other every 100 μm . Common centroid symmetrical layout, dummy device, nwell shielding, guard ring and on-chip MOS cap are extensively used throughout the layout design process. The final layout is shown in figure 6.12. The micrograph of the chip is shown in figure 6.13.

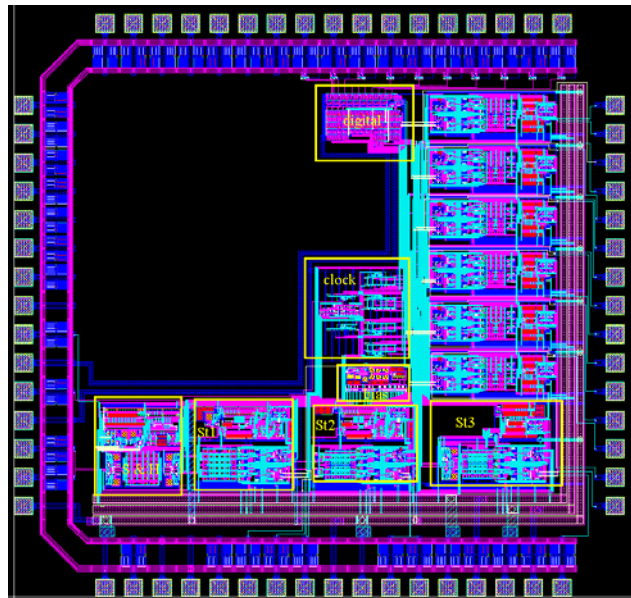


Figure 6.12 Reconfigurable ADC layout.

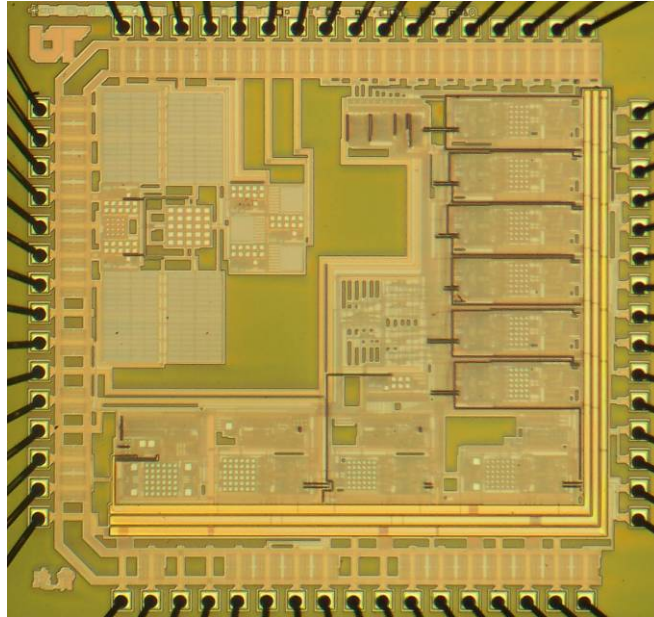


Figure 6.13 Micrograph of reconfigurable ADC chip

CHAPTER 7

PROTOTYPE MEASUREMENTS

In section 7.1, the measurement environment setup is introduced with emphasis on both hardware and software. The performance parameters are described in detail in section 7.2 for 10-bit and 8-bit configuration, respectively. Then, the performance is summarized in section 7.3. The comparison of this work with other reconfigurable ADCs, conventional pipeline ADCs and all ADCs are carried out in section 7.4.

7.1 Test Environment Setup

7.1.1 Test Boards

Test board design is very critical for high speed, high-resolution data converter measurements. A good layout of various components and critical paths can improve the signal integrity which leads to better test results.

There are mainly four important signal paths in this design. The first one is the power supply and ground. The DC voltage coming from the power supply is very noisy due to the built-in switching mode characteristics. A linear regulator can greatly reduce

voltage ripples in the power supply. Furthermore, a low pass filter isolates the digital and analog power supplies. The digital and analog ground planes are also separated by an inductor. The second signal path is for the input signal. The input signal is connected to the board by a SMA female connector and then converted to a differential signal by a balun. The input impedance for the ADC is matched to $50\ \Omega$ to reduce reflection. The input matching network is shown in figure 7.1. The third signal path is the clock which is generated by a square wave crystal oscillator. The path from the oscillator to the chip is kept as short as possible. The fourth paths are for the reference voltages, the input and the output common mode voltages. These four voltage references are buffered and filtered by opamps and big tantalum capacitors. A two layer FR-4 PCB with ground plane on both sides is shown in figure 7.2.

7.1.2 Test Instruments

See Table 7.1

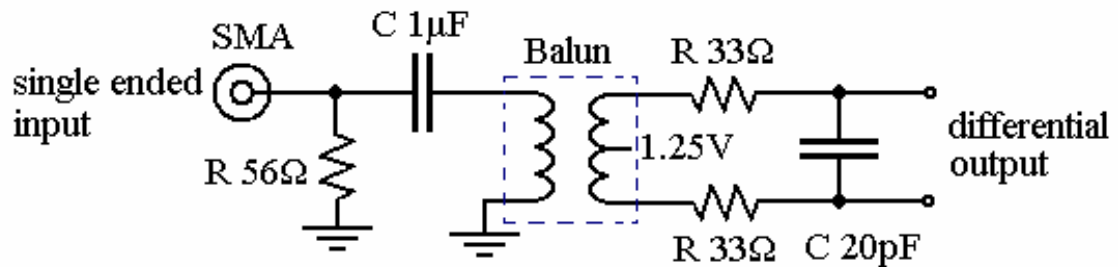


Figure 7.1 Input matching network for ADC Test.



Figure 7.2 Reconfigurable ADC Test Board.

Table 7.1 Test Instruments

TYPE	Features
Tektronix TLA 5204B Logic Analyzer	136 channels, 2G Timing, 32M memory for each channel.
Agilent E3631A Triple Output DC Power Supply	0~6V; 0~25V; 0~25V.
Agilent 33220A Waveform Generator	Maximum 20 MHz Sinewave.
Tektronix AFG3102 Arbitrary Function Generator	Maximum 100 MHz sinewave
Agilent 34401A Digit Multimeter	6.5 bits
Agilent MSO6052A Mixed Signal Oscilloscope	500MHz Bandwidth, 4Gsample per second.
Lenovo Thinkpad Laptop	With Matlab V6.1.450

Table 7.2 Test Board Components

Component	Type	Value	Digikey No.	Comment
ADC Chip	-	-	-	DUT
PCB	-	-	-	Two layer, FR4
Balun	ADT 1-1 WT	-	-	Minicircuits
Band Pass Filter	SBP-10.7+	10.7MHz center frequency	-	Minicircuits
Clock Oscillator	CB3-3C-40M0000	40MHz	CTX280CT-ND	Surface mount
Regulator	TPS79601	-	296-13761-1-ND	Output adjustable
Amplifier	AD8032	-	AD8032ARZ-ND	2 opamps
Voltage Reference	ADR380	2.048 V	ADR380ARTZ-REEL7CT-ND	
	ADR381	2.5 V	ADR381ARTZ-REEL7CT-ND	
Resistor	-	Various values	-	Metal film
Capacitor	-	Various values		Ceramic,tantalum
Inductor	-	1 μ H	PCD1187CT-ND	

7.1.3 Components

See Table 7.2

7.1.4 Test Software

In order to measure the static parameters of data converters, a low speed signal should be applied to the ADC input to minimize the dynamic effects. INL and DNL are two main parameters to evaluate how good the linearity is. One can apply a ramp voltage to the input to obtain the INL and the DNL. However, a very linear ramp generator is very difficult to build and this method is not practical for measurement of high-resolution data converters. In practice, a high purity sinewave is relatively easy to achieve. The

histogram method (Code Density Measurement) [74] based on statistics is used to calculate the DNL and INL. The Matlab program for the DNL and INL measurements is mainly based on the Maxim application note 2085 [75]. When using this method, the applied sinewave amplitude must exceed the full scale of the input signal. The result is somewhat amplitude dependent, but this effect is minor.

The dynamic parameters are obtained by Fast Fourier Transform (FFT) analysis. Since noncoherent test is used, the number of periods in one measurement period is not an integer. Therefore, a window function must be employed to decrease the spectrum leakage. A Hann window is used for its good tradeoff between spectrum leakage and spectrum resolution. By summing up the frequency bins of the signal, the harmonics and the noise separately, *SNR*, *SNDR*, *SFDR* and *THD* can be calculated. The Matlab program for dynamic data processing is based on another Maxim application note 729 [76].

7.1.5 Test Setup

See Figure 7.3 for a photo of the test setup.

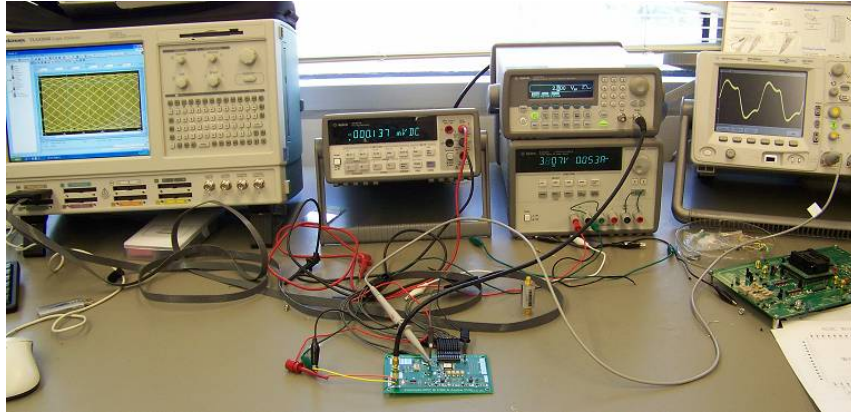


Figure 7.3 Test Setup for testing of ADC.

7.2 Test Results

7.2.1 Test Results of 10b, 40MSPS Mode

7.2.1.1 Static Test Results

Figure 7.4 and Figure 7.5 illustrate the DNL and INL when applying a 193 KHz sinewave to the ADC input. An accurate result is achieved by collecting 2,097,152 data points. The DNL and INL usually indicate the static linearity of the ADC. It mainly reflects the matching of the sampling and hold capacitors and the gain error caused by the OTA DC voltage gain. For the test results in this chapter, there is no calibration involved. The low DNL and INL indicate that the ADC has good matching.

Since the DNL and INL is amplitude dependent for code density measurement, the results in table 7.3 show that the DNL and INL will change with the input amplitude

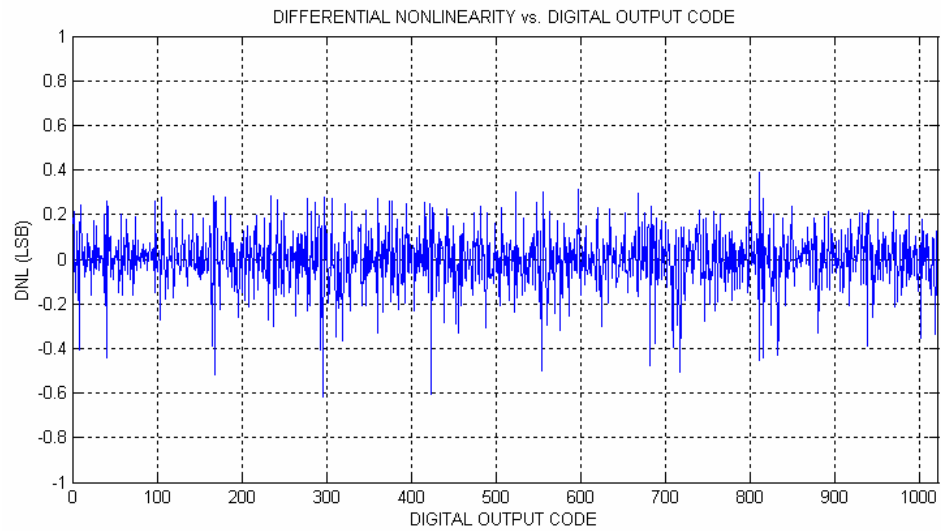


Figure 7.4 Differential nonlinearity (0.3890/-0.6156 LSB)

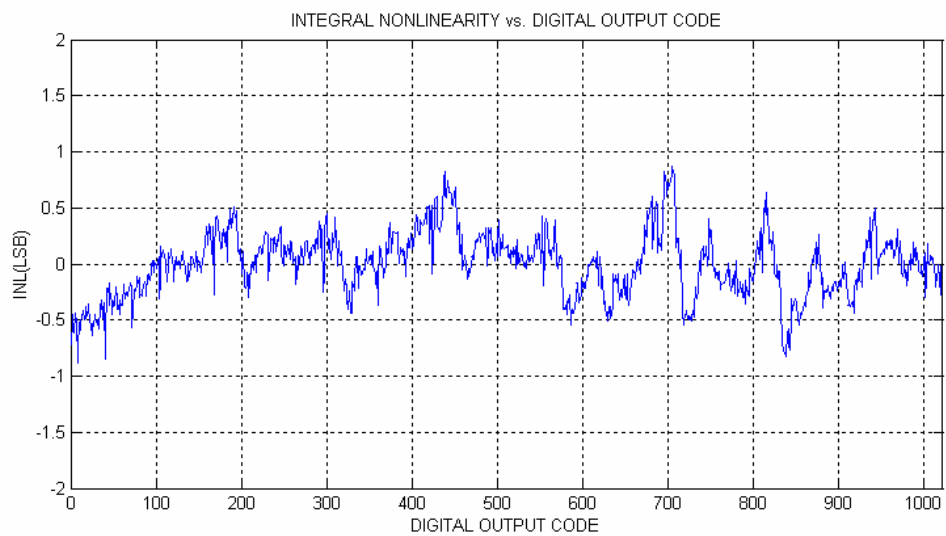


Figure 7.5 Integral nonlinearity (0.8669/-0.8789 LSB).

Table 7.3 DNL and INL with input amplitude at 811 KHz

Input Amplitude (FS)	DNL (LSB)	INL (LSB)
1.0021	0.3980/-0.6031	0.7254/-0.8123
1.0039	0.3612/-0.6036	0.7170/-0.7774
1.0057	0.4215/-0.6313	0.6902/-0.7899
1.0090	0.3788/-0.6187	0.7433/-0.8294

but do not show strong positive or negative correlation with the amplitude when the amplitude is just above the full scale.

The DNL and INL is mainly an evaluation of the nonlinearities for the low frequency input signal. When operating for the high frequency input signal, the DNL and INL tend to be worse due to the error caused by settling and charge injection. The DNL and INL for the lower frequency are also large as shown in table 7.4. The main reason is that the input signal is AC coupled before feeding into the balun. Therefore, distortion is introduced by this zero for the low frequency input.

7.2.1.2 Dynamic Test Results

In order to get a better frequency resolution, a 16,384 points FFT analysis was carried out. Figure 7.6 illustrates the FFT plot for a 1,119 KHz input sinewave. Figure 7.7 illustrates the FFT plot for a 10,700 KHz input sinewave with a Band Pass Filter (BPF). The signal generator used during the measurement has a large 3rd order harmonic for high frequency. A band pass filter was used to decrease the third order harmonic. In these FFT

Table 7.4 DNL and INL with input frequency

Input Frequency (KHz)	DNL (LSB)	INL (LSB)
137	0.5354/-0.6939	2.2545/-3.1807
161	0.5205/-0.7174	1.1405/-1.8529
193	0.3890/-0.6156	0.8669/-0.8789
225	0.3996/-0.6421	1.0845/-0.8408
251	0.4182/-0.6251	1.2529/-1.1290
315	0.3907/-0.7143	1.1583/-0.9098
428	0.5510/-0.6673	1.2498/-1.0103
811	0.3980/-0.6031	0.7254/-0.8123
1675	0.4984/-0.6783	1.4230/-0.7797
3824	0.5207/-0.7126	0.9543/-1.4952

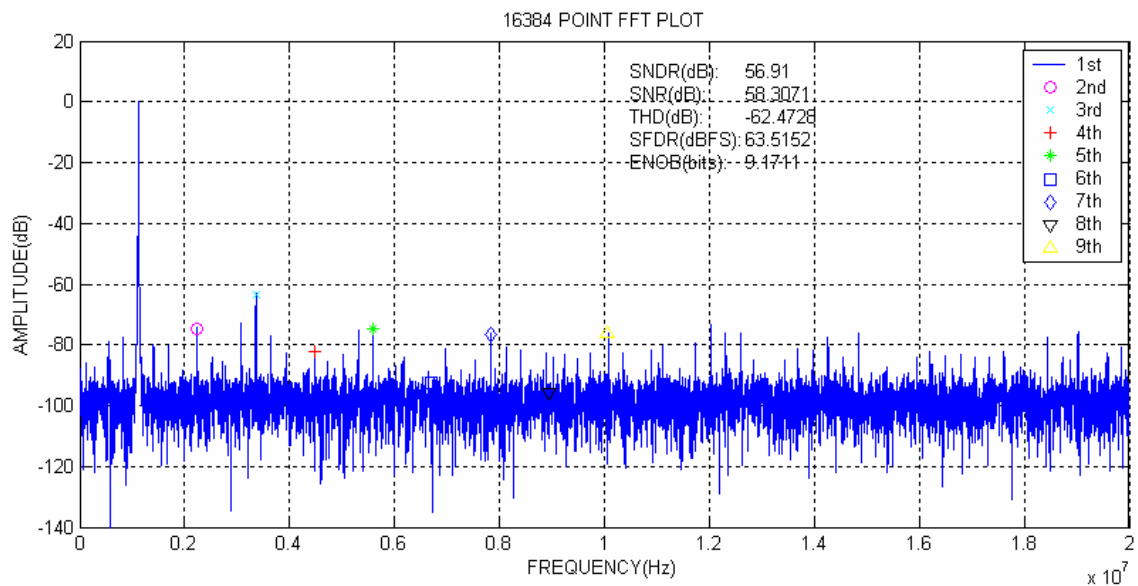


Figure 7.6 16,384 points FFT analysis at 1,119 KHz

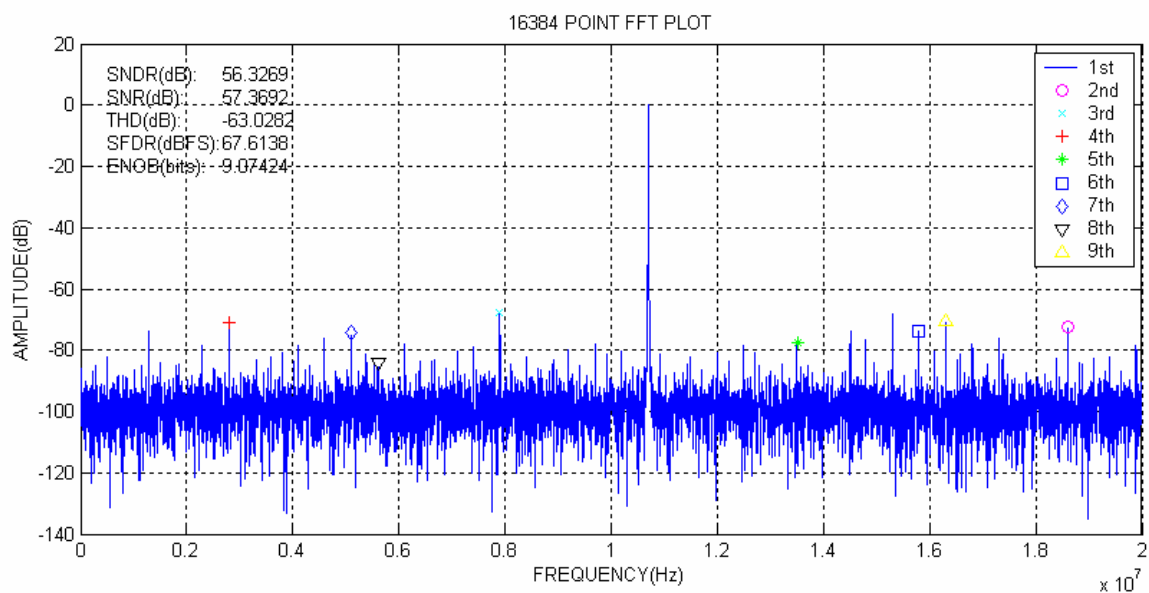


Figure 7.7 16,384 points FFT analysis at 10,700 KHz with BPF

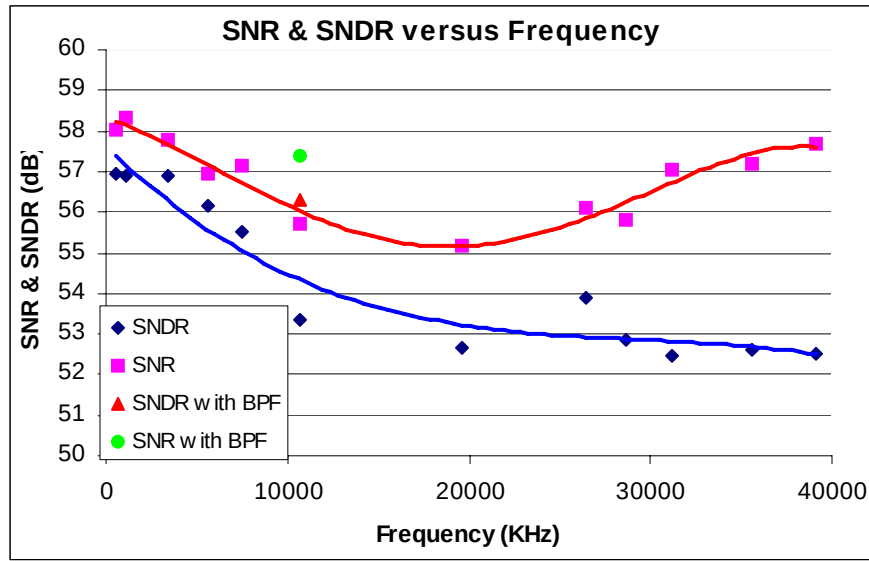


Figure 7.8 SNR and SNDR with input signal frequency.

plots, 2nd to 9th order harmonics are also labeled with different symbols and colors.

Figure 7.8 shows the *SNR* and *SNDR* with the input frequency derived from FFT analysis. The decrease of *SNDR* with input frequency in figure 7.8 is mainly caused by the increase of the distortions. The harmonics power is increased with the frequency as shown in figure 7.9 (Minus sign before *THD* is removed in order to plot with *SFDR*). The red triangle and green dot in figure 7.8 indicate the *SNDR* and *SNR* at 10,700 KHz input signal with band pass filter. The 2-3 dB *SNDR* and *SNR* loss due to nonlinearity of the input signal make the test results at high frequency worse than its real values.

The ENOB with the frequency is shown in figure 7.10. The *EONB* is decreased

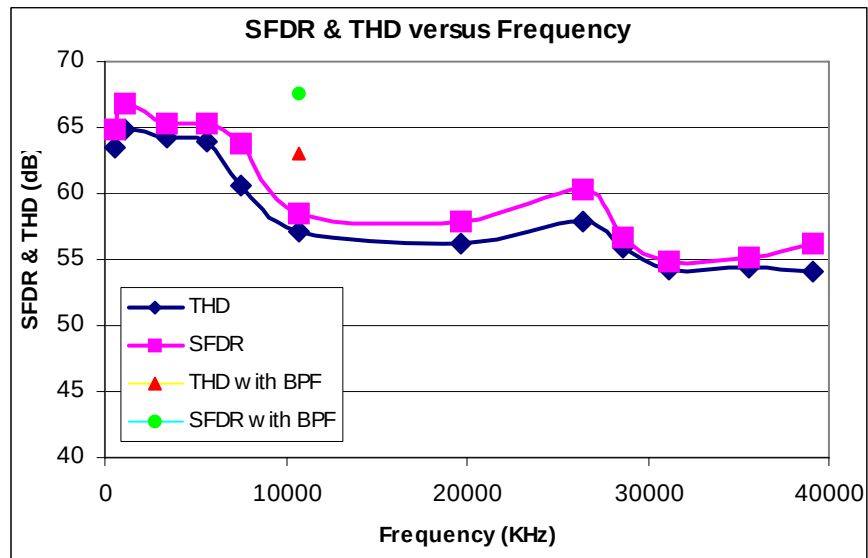


Figure 7.9 SFDR and THD with input signal frequency.

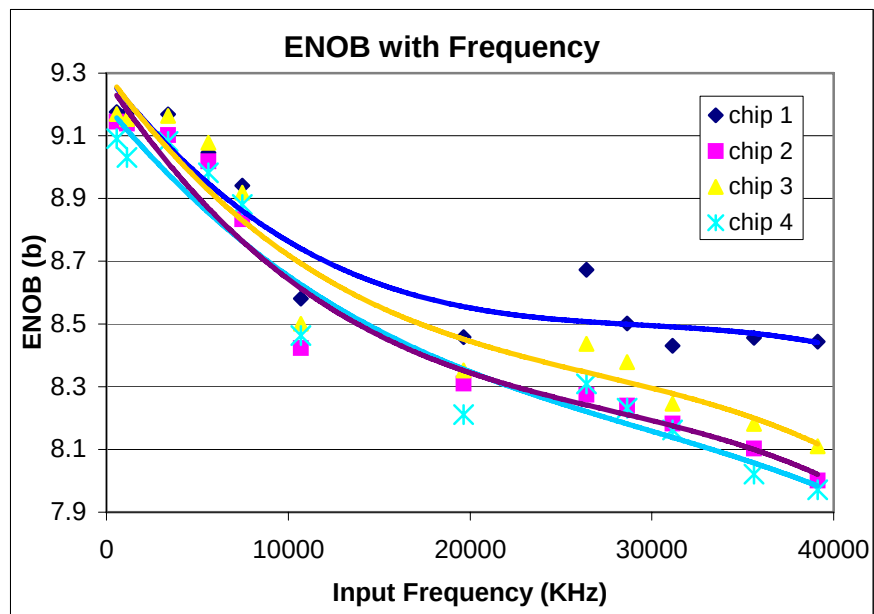


Figure 7.10 ENOB with input signal frequency.

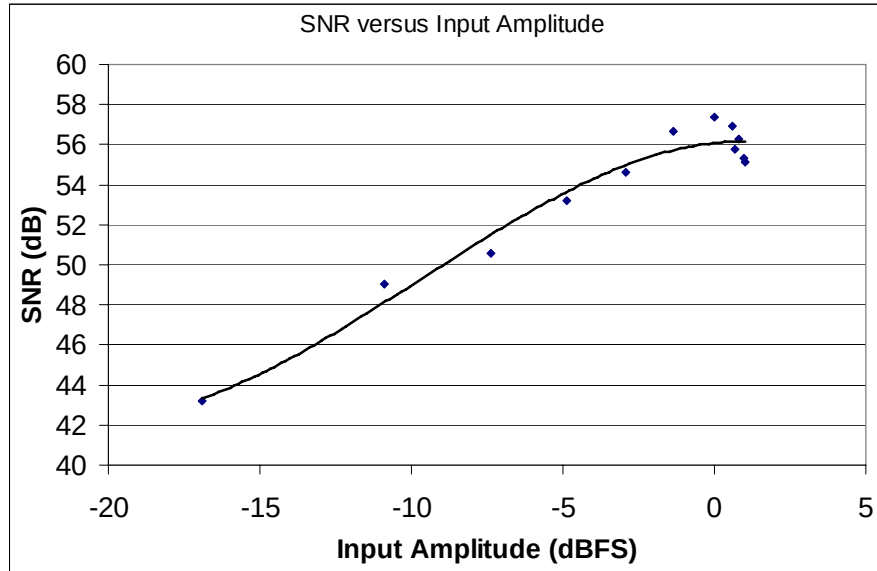


Figure 7.11 SNR with input signal frequency at 10,700 KHz with BPF.

gradually with the input frequency. As mentioned previously, using of the BPF can improve the *ENOB* by 0.5 bit.

The *SNR* with the input amplitude at 10,700 KHz with band pass filter is shown in figure 7.11. The *SNR* drops at high input amplitude due to distortions caused by saturation.

7.2.2 Test Results of 8b, 2.5MSPS Mode

7.2.2.1 Static Test Results

Figure 7.12 and Figure 7.13 illustrate the DNL and INL when applying a 247 KHz sinewave to the ADC input. An accurate result is achieved by collecting 524,288

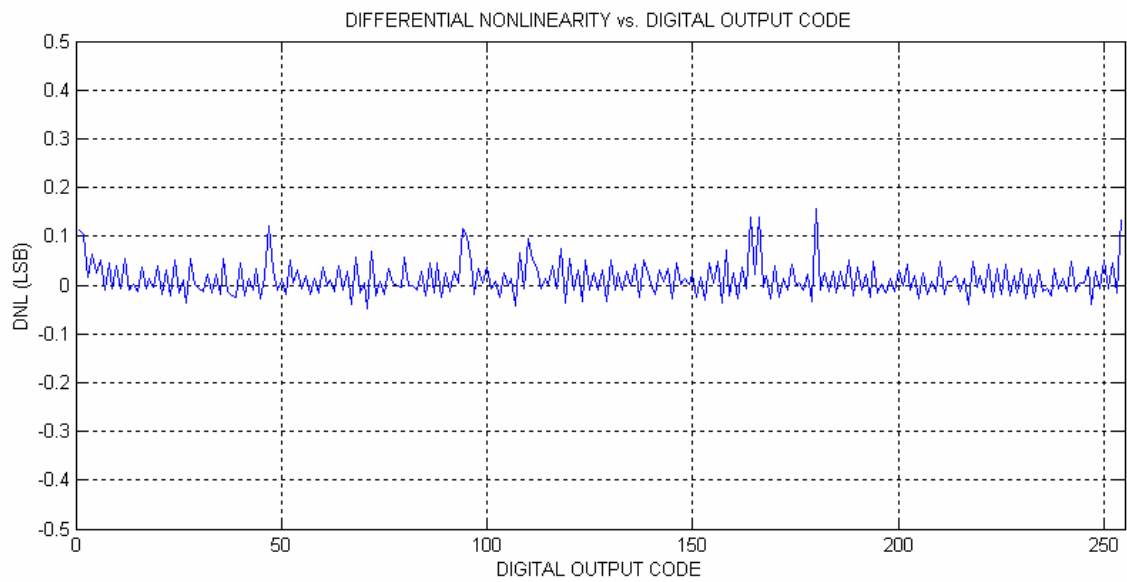


Figure 7.12 Differential nonlinearity (512K data points, 0.1577/-0.0483)

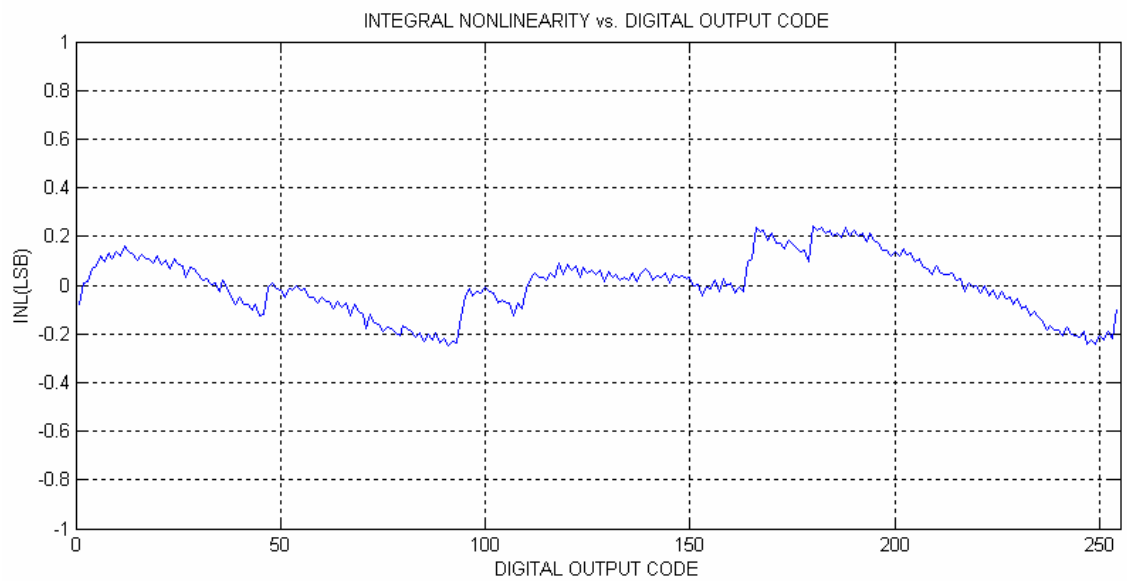


Figure 7.13 Integral nonlinearity (512K data points, 0.2442/-0.2477).

data points. The DNL in figure 7.12 is 0.1577/-0.0483 LSB. The INL in figure 13 is 0.2442/-0.2477.

Several codes have significant larger DNL than other codes. The possible reason is that the random mismatch of sampling and hold capacitors in one of the middle stages is relatively larger than the others. One may also notice that the average of DNL is deviated from zero. However, this effect does not show up in the INL function. The reason is due to the algorithm used to calculate the INL. Two algorithms are popular to calculate the INL. One is the end-point fit algorithm and another is the best-straight-line fit algorithm. The latter one was used in this work.

The DNL and INL value for different input frequencies are summarized in table 7.5. The DNL and INL do not show strong correlation with the input frequency when compared to table 7.4. The DNL and INL tend to be worse when sampling clock frequency and input signal frequency are correlated. Attention must be paid when

Table 7.5 DNL and INL with input frequency

Input Frequency (KHz)	DNL (LSB)	INL (LSB)
247	0.1577/-0.0483	0.2442/-0.2477
351	0.2332/-0.1453	0.2918/-0.3644
517	0.2080/-0.1082	0.2554/-0.3117
777	0.2093/-0.1433	0.2695/-0.4097
1000	0.1827/-0.0445	0.2758/-0.3206

selecting the input frequency. Otherwise, not only the DNL and INL but also SNR and SNDR will be deteriorated.

7.2.2.2 Dynamic Test Results

In order to get a better frequency resolution, an 8,192 points FFT analysis was carried out. Figure 7.14 illustrates the FFT plot for a 361 KHz input sinewave. Figure 7.15 illustrates the FFT plot for a 1,619 KHz input sinewave. Since 1619 KHz input frequency is larger than half of the sampling frequency (Nyquist frequency), the FFT spectrum is folded back and overlapped with 881 KHz spectrum.

The 2nd to 9th order harmonics are also labeled on the figures with different symbols and colors. All the dynamic parameters such as *SNR*, *SNDR*, *THD*, *SFDR* and *ENOB* can be extracted from FFT analysis at each input frequency.

The power of the harmonics for same input frequency is in the same level when figure 7.6 and 7.7 are compared with figure 7.14 and 7.15. However, the noise floor is increased about 15 dB. There are two reasons for this extra 15 dB noise floor increase. The first one is due to the 12 dB quantization noise difference between 8 bits and 10 bits. Another one is due to the data points of the FFT analysis. The decrease of FFT data points from 16,384 to 8,192 adds extra 3 dB on the noise floor.

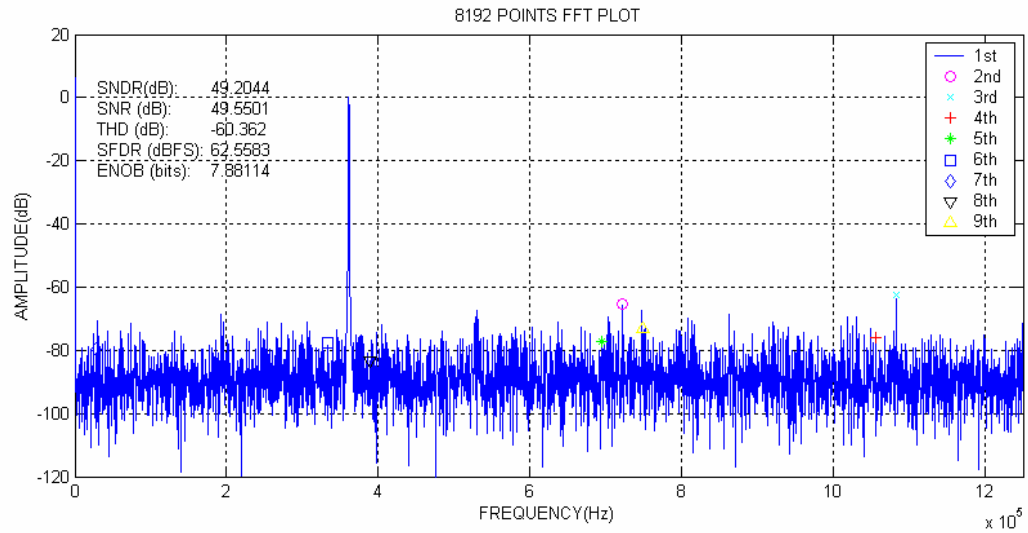


Figure 7.14 8,192 points FFT analysis at 361 KHz

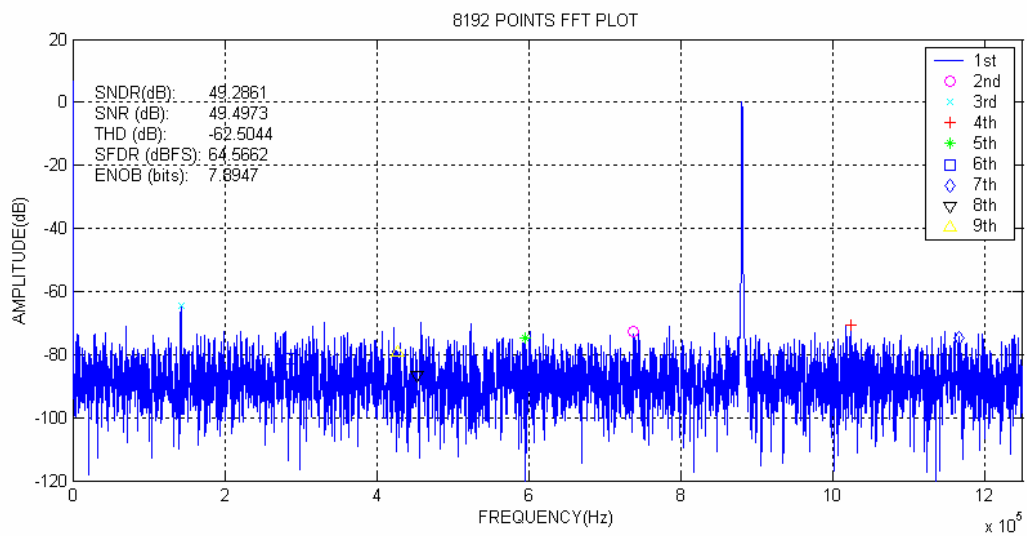


Figure 7.15 8,192 points FFT analysis at 1619 KHz (spectrum fold back due to larger than Nyquist frequency)

The first data point in figure 7.16 shows smaller SNR and $SNDR$ values. The main reason is still due to the distortion caused by the input-matching network. This effect will diminish with the increase of the input frequency. The SNR and $SNDR$ values are almost kept constant as shown in figure 7.16 excluding the first data point. It indicates that the distortions caused by dynamic settling only have minor effects on the final results.

Since the ADC is fully differential, the even order harmonics should be canceled. The third harmonic is the main spurious tone. The entire test results in this work show that the third harmonic limits the Spurious Free Dynamic Range. However, due to random mismatch, the second harmonic also contributes a significant power to the total harmonic distortion. The $SFDR$ and the THD are plotted in figure 7.17 as a function the input frequency. The minus sign of the THD is removed intentionally to plot the $SFDR$ and the THD in the same figure. However, the THD is always negative by definition.

Figure 7.18 shows the $ENOB$ with input signal frequency for different chips. The $ENOB$ is almost constant for the entire frequency range except the first data point due to distortion caused by the zero of the input matching network. The $ENOB$ is also related to the DNL and INL. The low DNL and INL in table 7.5 have good agreement with the high $ENOB$ in figure 7.18.

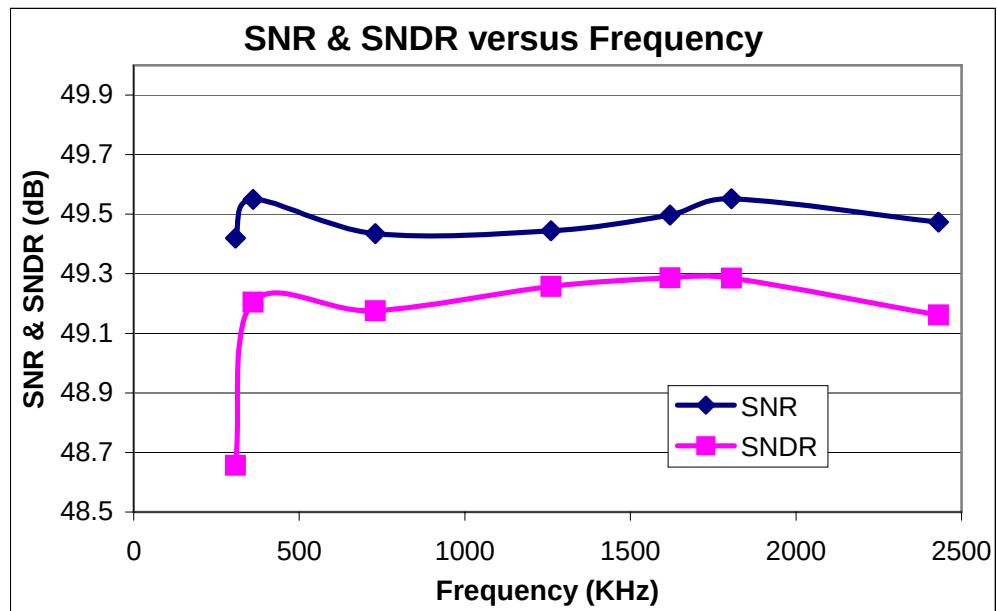


Figure 7.16 SNR and SNDR with input signal frequency

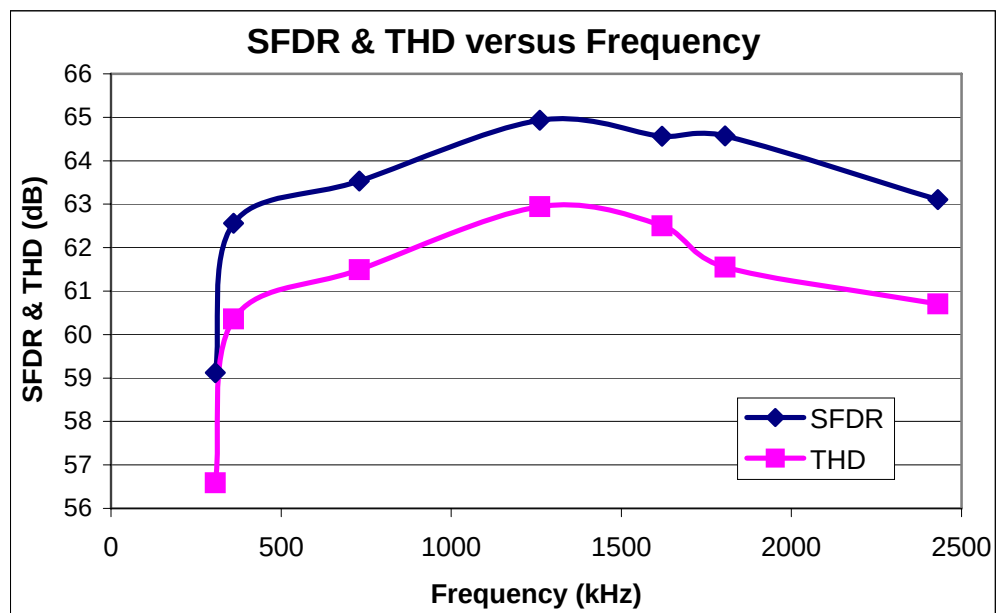


Figure 7.17 SFDR and THD with input signal frequency

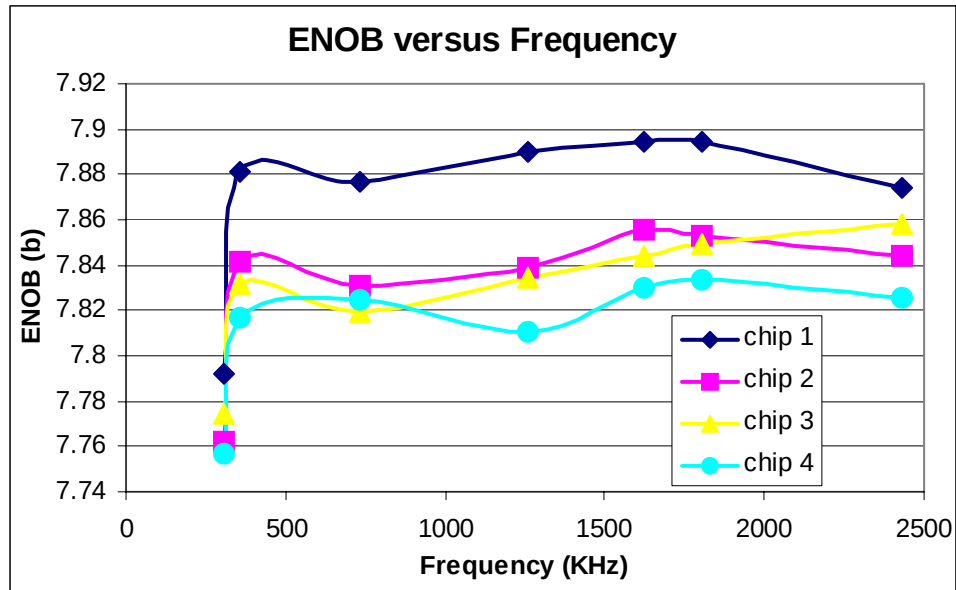


Figure 7.18 ENOB with input signal frequency

Figure 7.19 shows the SNR with the input amplitude at 361 KHz input frequency. Since the quantization noise and thermal noise will not change with the input signal amplitude, the SNR will change linearly with the input signal power in dB. The curve in figure 7.19 shows a perfect match with the prediction by the theory.

7.3 Performance Summary

The performance of the reconfigurable ADC is summarized in table 7.6. The dynamic parameters were obtained when ADC operated at 1,119 KHz input signal for 10b, 40 MSPS mode and at 361 KHz input signal for 8b, 2.5 MSPS mode. The static parameters were obtained when ADC operated at 193 KHz input signal frequency for 10b 40 MSPS mode and at 247 KHz input signal frequency for 8b, 2.5 MSPS mode.

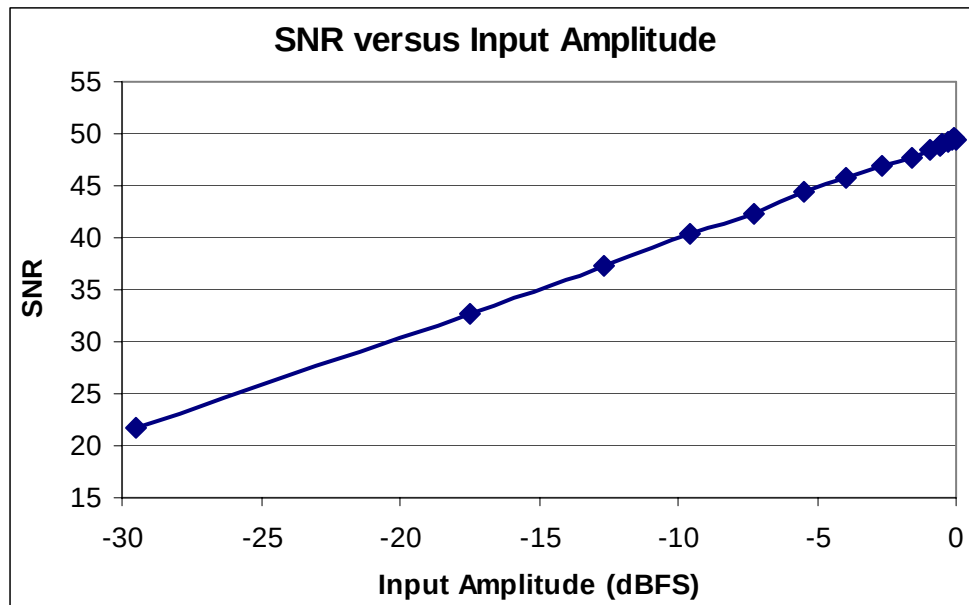


Figure 7.19 SNR with input amplitude at 361 KHz input frequency.

Table 7.6 Reconfigurable ADC Performance Summary

Sample Rate (MHz)	40	2.5	Sample Rate (MHz)	40	2.5
Resolution (b)	10	8	Resolution (b)	10	8
SNR (dB)	58.31	49.55	DNL (LSB)	0.39/-0.62	0.16/-0.05
SNDR (dB)	56.91	49.20	INL (LSB)	0.87/-0.88	0.24/-0.25
ENOB (b)	9.17	7.88	Supply Voltage (V)	2.5	2.5
SFDR (dBFS)	63.52	62.56	Power (mW)	35.4	7.9
THD (dB)	-62.47	-60.36	FOM1 (pJ)	885	3160
Reference pk-pk (V)	1.94	1.94	FOM2 (pJ)	1.51	13.23

7.4 ADC Performance Comparison

7.4.1 Comparison of Reconfigurable ADC

The reconfigurable ADC listed in table 2.1 is redrawn in table 7.7 with the FOM4 and the test results of this work. From table 7.7, reference [24] has the smallest value of FOM4, this work has the second smallest value of FOM4. The unit for FOM4 is energy·area per conversion. That means how much energy and area one should invest in order to get a conversion. The small value of FOM4 indicates the more cost-efficient of the converters. The FOM4 for each reconfigurable ADC is also shown in figure 7.20 with its *SNDR*.

7.4.2 Comparison of Reconfigurable ADC with Conventional Pipeline ADC

The bandwidth of this work's ADC is illustrated with the entire pipeline ADCs published in the past eleven years in ISSCC and VLSI conference in figure 7.21. The trend shows that the *SNDR* will decrease with the increase of the bandwidth. The ADC of this work lies in the middle of this trend [77].

FOM1 shown in figure 7.21 is the evaluation of energy per conversion. With the increase of resolution, the energy needed to invest to get a conversion is increased. The correlation between the power consumption and resolution is positive. This design is also in that trend but with relatively low power efficiency when compared with the latest state-of-art ADC published in ISSCC.

Table 7.7 Comparison of Reconfigurable ADC Performance

Ref.	Bits (b)	f_s (MHz)	Power (mW)	VDD (V)	ENOB (b)	Area (mm ²)	Process (μ m)	Configuration	FOM4
[25]	14	10-40	72.8	2.8	10.4	1.15	0.18	Rates	47.8
[24]	12	20-140	97	1.8	10.4	0.86	0.18	Rates	13.6
[26]	10	1k-50	35	1.8	8.8	1.2	0.18	Rates	58.2
[29]	6-16	2.62	24.6	4.6		79.8	0.6	Rates, resolution	
		10	17.7	4.6					
[39]	9	40	425	1.8	6.9	5.9	0.25	Interchange stage	8398.3
[23]	6,8,10	80	94	1.8	9.1	1.9	0.13	Rates, resolution	240.7
[36]	6-10	20	8	1.8	9.1	3.2	0.18	Rates	72.0
[16]	-	20	37	1.8	9.3	1	0.18	Rates, resolution	90.6
This work	8,10	2.5-40	35.4	2.5	9.2	1.9	0.35	Rates, resolution	23.3

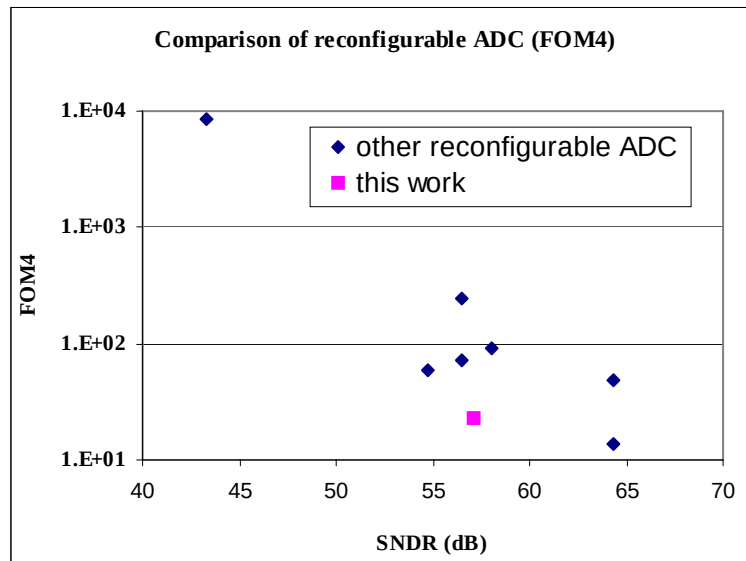


Figure 7.20 Comparison of reconfigurable ADC

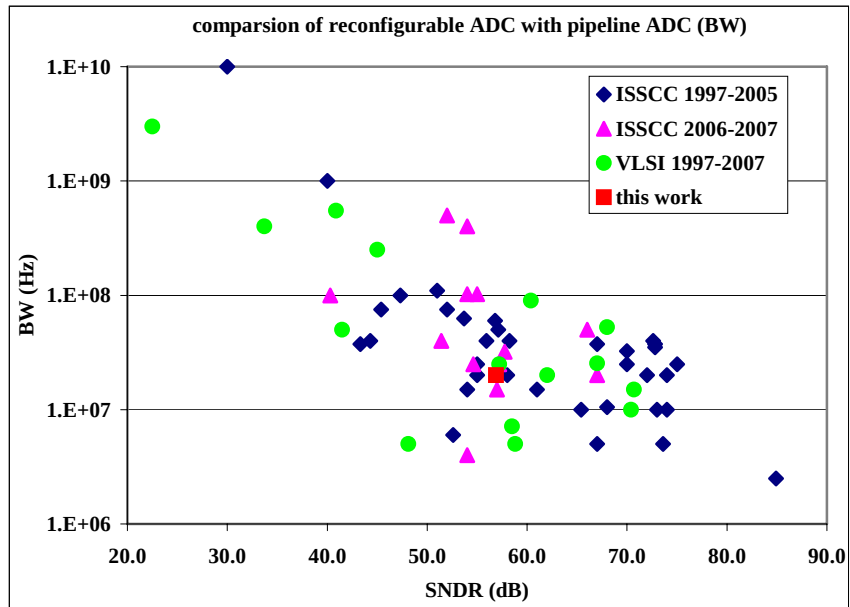


Figure 7.21 Bandwidth Comparison of reconfigurable ADC with pipeline ADC

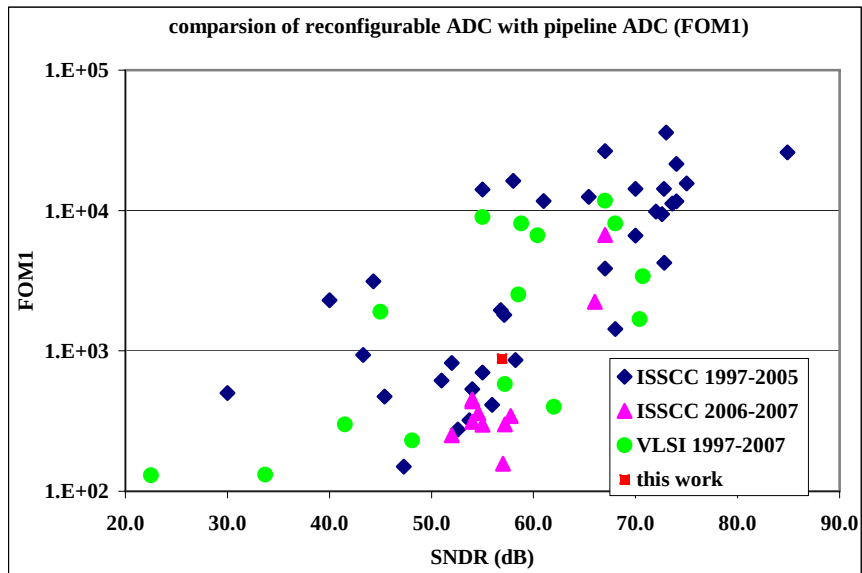


Figure 7.22 FOM1 comparison of reconfigurable ADC with pipeline ADC

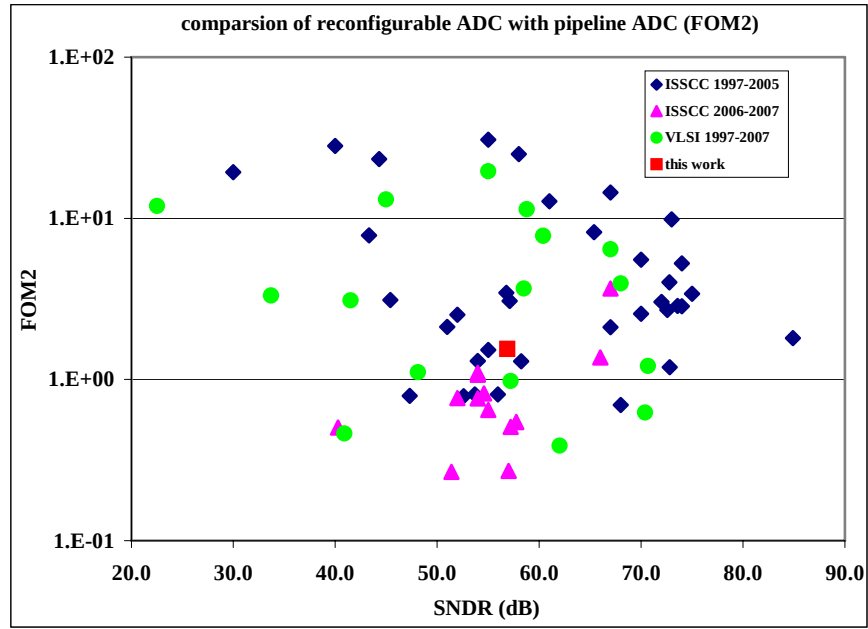


Figure 7.23 FOM2 comparison of reconfigurable ADC with pipeline ADC

FOM2 is the evaluation of energy per conversion-step. It looks like that the FOM2 in figure 7.23 is more random than FOM1 and BW in figure 7.22 and 7.21. However, smaller FOM2 always means better power efficiency.

7.4.3 Comparison of Reconfigurable ADC with All ADC

The trend of the negative correlation between BW and SNDR is making more sense when compared with all the ADCs regardless of the architectures. For the previous plot in figure 7.21, the span of $SNDR$ and BW is too small for pipeline ADC. The performance of this work is still comparable with other ADCs as shown in figure 7.24.

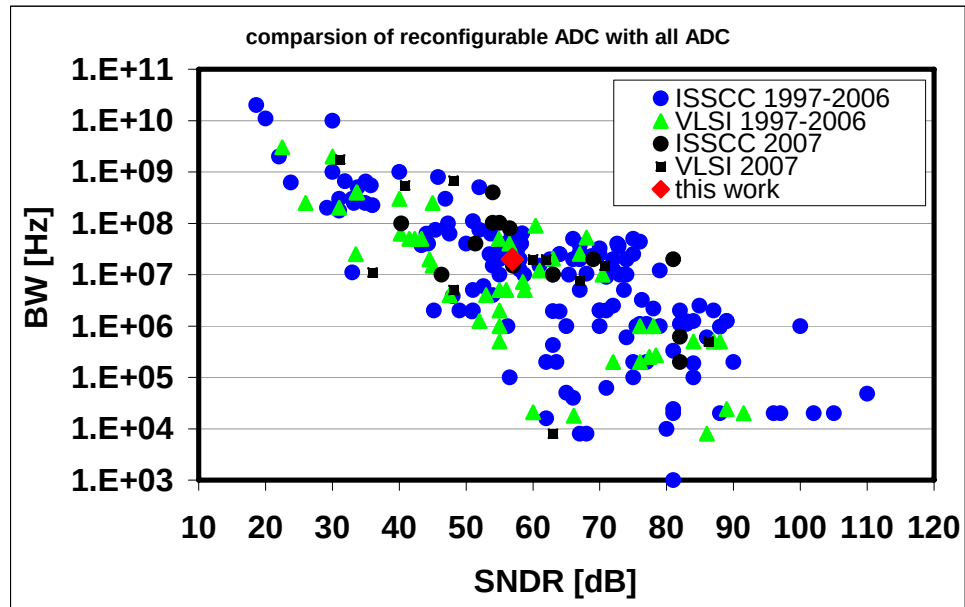


Figure 7.24 Bandwidth comparison of reconfigurable ADC with all ADC

The power efficiency of data converters with SNDR for all the ADCs is shown in figure 7.25. The positive correlation is clearly shown in this figure. For the same SNDR, the lower the data point, the higher the power efficiency.

It seems that there is no correlation between FOM2 and *SNDR* as shown in figure 7.26. However, the latest published results in ISSCC and VLSI have lower FOM2 regardless of the *SNDR*. The trend is that the FOM2 moves down for the latest design. This design is also considered a good design when compared with other ADCs.

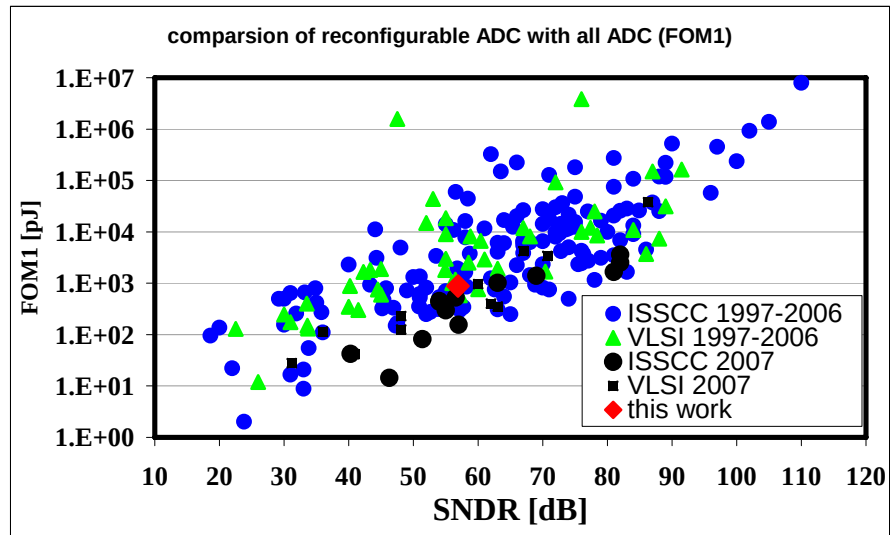


Figure 7.25 FOM1 comparison of reconfigurable ADC with all ADC.

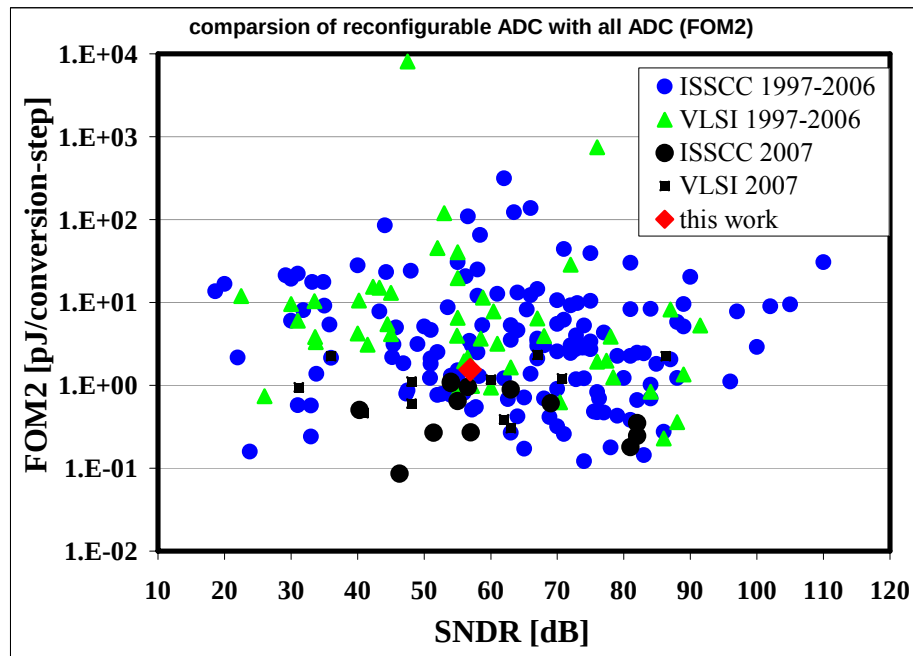


Figure 7.26 FOM2 comparison of reconfigurable ADC with all ADC.

CHAPTER 8

CONCLUSIONS

Design methodology, prototype implementation and measurement results are presented in the previous chapters. In this chapter, some unaddressed issues are first discussed in section 8.1, and then conclusions are drawn based on the measurement results in section 8.2.

8.1 Discussions

The configurations on the conversion rate and resolution described in this work can be extended to other forms depending on applications. For this work, two configurations are implemented based on the requirements of the bioinstrument. With the help of the interference elimination technique, one can always route the input signal to the stage 2 or the stage 4, then a 7~10 bits reconfigurable ADC can be realized. If more configurations on the conversion rate are needed, a low-resolution current steering DAC can be designed, by turning on or off those switches, different bias current could be obtained. One problem with the OTAs is that they cannot afford complicated reconfigurations and their power efficiency may not be very high for every speed configuration.

The integrated circuit chip developed in this work will either work in operating rooms or stay inside human bodies. The temperature variation in both cases is very small, so no temperature compensation circuits were employed in this work. The temperature range is targeted from 0 to 70 °C.

For the OTA bias, the bias currents are generated from the voltage reference and off-chip resistors. For wide range temperature applications, one can use constant g_m bias scheme to replace the bias generation circuit in this work.

Since noncoherent sampling is employed, a window function must be applied before the FFT analysis. Different window functions have different effects on resolution and spectrum leakage. A Hann window function (another name is raised cosine) was applied during the FFT analysis of this work. There is a possibility that other windows may lead to better results.

The voltage reference [78] and reference buffer are not implemented on chip. For a pipeline ADC, two voltage references are required to give an upper and lower bound for full-scale signal. The voltage references should be very stable. The pipeline stages may draw a large amount of transient current during the conversion. Therefore, the impedance of reference buffers must be very small. The -3 dB bandwidth and slew rate must be large for fast transient response.

The pipeline ADC requires a differential input. Therefore, a balun (or transformer) is used to convert the signal from single-ended to differential with AC coupling. However, attention must be paid on the signals which applied on the input. For low frequency signals, a significant attenuation and distortion will corrupt the signals. For high frequency signals, attenuation is observed during the measurement.

The signal generator (Tektronix AFG 3102) has a very large third order harmonics. This harmonic tone in the signal tends to limit the linearity of the test results. For 10.7 MHz signal, a band pass filter was applied during the measurements. The *SNDR* gains 3 dB (0.5 bit in *ENOB*) with the BPF. The measurement results beyond 10.7 MHz in this work could improve a 0.5 bit by using BPF.

The telescopic OTAs in pipeline stages require different common mode voltages for input and output. The input common voltage is set to 1 V and output common voltage is set to 1.25 V.

There is also another possible way to maintain the inversion coefficient of the transistors in OTA [79, 80]. Chen *et al* report an innovative circuit that can alter the transistor bias by tracking the temperature change to keep it operating in constant inversion coefficient. This circuit has a better tradeoff on decreasing the variation of

small signal bandwidth and large signal slew rate over constant current and constant g_m bias schemes. The only problem with that circuit is that the floating NPN transistors are used to generate the PTAT voltage which may not be available in most of the CMOS technologies.

8.2 Conclusions

The developed ADC chip in this work achieves 0.39/-0.62 LSB DNL, 0.87/-0.88 LSB INL, 56.9 dB SNDR and 9.2 bits ENOB under 2.5 V power supply for 10b, 40MSPS mode with 35.4 mW power consumption and 0.16/-0.05 LSB DNL, 0.24/-0.25 LSB INL, 49.2 dB SNDR and 7.9 bits ENOB for 8b, 2.5MSPS mode with 7.9 mW power consumption. The total area for this chip is about 1.9 mm² with a 0.35 μ m technology.

The performance of the reconfigurable ADC can fulfill the requirements of the bioinstrument in terms of resolution, conversion rate, linearity, power and area constraints.

The FOM4 of this work is the second best among all the reconfigurable ADCs reported. The FOM1 and FOM2 of this work are among the best when compared to the published results in ISSCC and VLSI in the past 11 years.

The interference elimination technique for reconfiguration is proved to be very useful. This technique will work even better for high-resolution applications. Moreover, this technique can be used for more configurations in resolution in theory.

The reconfigurable OTA and scalable bias technique make an optimum tradeoff between power efficiency and speed. This technique can be extended to more configurations by careful design.

CHAPTER 9

FUTURE WORK

In this chapter, the future work of this design is addressed. A number of suggestions for future works related to this dissertation are presented. In particular, three components are identified and discussed in details. The reference and reference buffers are treated in section 9.1. The possible integration of the reconfigurable pipeline ADC with the signal processing IC is illustrated in section 9.2. The clock scheme and all the other potential works are listed in section 9.3.

9.1 Reference and Reference Buffers

In this design, the reference voltages are generated using off-chip components. The reference buffer is also off-chip. These circuit blocks can be integrated on-chip to decrease the number of off-chip components. There are 4 reference voltages needed in the reconfigurable ADC. They are v_{refp} , v_{refn} , v_{cmi} and v_{cmo} . The values for these references are 1.75 V, 0.75 V, 1 V and 1.25 V, respectively. These reference voltages can be generated using the circuit shown in figure 9.1.

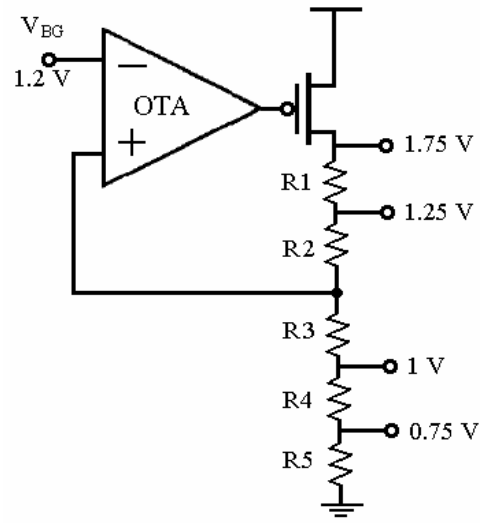


Figure 9.1 Circuit used to generate the reference voltages.

In this circuit, the bandgap reference voltage can be generated by combining a PTAT voltage with a negative TC V_{be} voltage. The circuit used to generate this voltage can be found in [10].

The OTA used in figure 9.1 can be a one-stage or a two-stage OTA. For a two-stage OTA, the compensation could be a problem due to three gain stages in the feedback loop. For a one-stage OTA, the voltage gain is relatively small, leading to an inaccurate static voltage. Since only the difference voltage between v_{refp} and v_{refn} is the main concern, the absolute inaccurate static voltage will not affect the results as long as these voltages are in the OTA output voltage range.

The requirements for the reference buffers are high bandwidth, large slew rate and high gain. These requirements are very challenge to be fulfilled especially under certain power constraints. There are total 4 reference buffers needed and the input voltage range is from 0.75 V to 1.75 V. If one buffer design can fit this voltage range, the input stage should be a complementary input pair. Moreover, in order to obtain high gain, cascode structure can be used. The slew rate can be improved by increasing the tail current of the input stage. The output stage should provide large transient current while only maintain a small quiescent current. Then a class AB output stage could be the best choice to meet the requirements.

9.2 Reconfigurable ADC Application in Signal Processing IC

As mentioned in chapter 1, the reconfigurable ADC developed in this work is mainly used to replace the SAR ADC in the cantilever array signal-processing IC. However, changes must be made for the other components in the IC to incorporate the reconfigurable pipeline ADC. The reconfigurable pipeline ADC requires a differential input and the signal for the previous SAR ADC is single ended. There are two ways to solve this problem. First method is converting the signal from single-ended to differential using a balun and another way is using a full differential instrumentation amplifier to replace the classic three opamp IA. Moreover, the digital circuit used to process 8-bit signal should be revised accordingly in order to process either 8-bit or 10-bit data depending on the ADC operation mode.

9.3 Clock Scheme and Other Work

The reconfigurable ADC of this work requires two clocks for different configurations. They are 40 MHz and 2.5 MHz. The 2.5 MHz clock can be obtained by dividing the 40 MHz using a simple divider. In this work, this divider was not implemented because various clock frequencies other than these two clock frequencies were used to test the reconfigurable ADC.

For the reconfigurable ADC, some pins are dedicated for testing. For field applications, these pins can be removed and the whole chip can be packaged in a 24-pin SOP package to reduce the volume of bioinstrument.

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VITA

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