

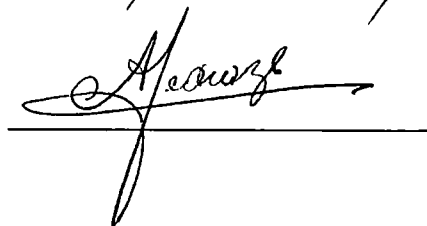
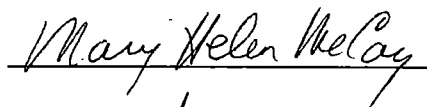
To the Graduate Council:

I am submitting herewith a thesis written by James Intrater entitled "Materials and Materials Processing Issues in the Fabrication of a Discrete, High-Power, Surge-Arresting Device." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Metallurgical Engineering.

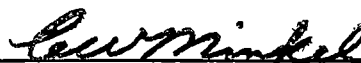


Narendra Dahotre, Major Professor

We have read this dissertation
and recommend its acceptance:



Accepted for the Council:



Associate Vice Chancellor and
Dean of The Graduate School

**MATERIALS AND MATERIALS PROCESSING ISSUES IN THE
FABRICATION OF A DISCRETE, HIGH-POWER, SURGE-
ARRESTING DEVICE**

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

James Intrater
May 1999

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ABSTRACT

Devices were designed and constructed that would demonstrate the ability to act as surge suppressors for electrostatic discharge. In addition, materials selection efforts combined with the selection of fabrication processes helped demonstrate that Cu and even more so, W metallization in conjunction with a glass filler phase would show measurable performance as a lightning surge suppressor. Microscopy and data support the actual device performance and indicate that for a lightning pulse, W, as opposed to Ag and Cu, is required for device metallization due to its high melting point. Glass, as opposed to an organic polymer, is needed as a filler due to its resistance to pulse-induced disintegration.

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NOMENCLATURE

μm	micron
μs	microsecond
Σt_i	summation of separate but successive dielectric path lengths
Ag	silver
Al_2O_3	aluminum oxide
Cu	copper
I	current
IR	infrared
Ω	ohms
$\text{k}\Omega$	kilo-ohms
K_s	dielectric strength
Mo	molybdenum
ns	nanosecond
p-n junction	positively doped-negatively doped interface
V	volt
V_b	dielectric breakdown voltage
V_c	clamp voltage
V_p	peak voltage
W	tungsten
W	watt

Abbreviations

AC	alternating current
ESD	electrostatic discharge
IC	integrated circuit
MGDF	microgap dielectric filled
MOV	metal oxide varistor

DEFINITIONS

Capacitance	Attenuation of a signal through its inductive charge coupling with a passive electrical component leading to parasitic loss in signal integrity.
Clamp voltage	Approximately steady-state voltage reached after collapse from the peak voltage in the voltage vs. time plot of an surge suppressor during its activation, just prior to switching off.
Dielectric	Though a misused term, generally refers to an electrically insulating material.
Dielectric breakdown	The switching from a relatively electrically insulative to relatively electrically conductive state of a material, through the application of a quantifiable, adequate voltage.
ESD	Electrostatic discharge. The release of a static charge, often from the human body, which impinges upon an electrically conductive surface.
Peak voltage (Voltage peak)	Maximum voltage reached in the voltage vs. time plot of an surge suppressor during its activation.
Surge suppressor	A circuit protection device which switches from a relatively electrically insulative to relatively electrically conductive state, in response to a given over-voltage, so as to drain excessive current through itself and away from a given electronic component.
Trigger	Instigation of switching of a surge suppressor from a relatively electrically insulative to relatively electrically conductive state.
Trigger voltage	Minimal applied voltage, under specific test conditions, which will successfully activate a surge suppressor to switch "on".
Zener diode	A specific, solid-state surge suppression device.

Section 1

Background

Voltage surge-induced electronic failures represent a multibillion dollar problem for the U. S. and world microelectronics industry [1-3]. Such voltage surges can harm or destroy delicate electronic components, principally integrated circuits (ICs). Conventionally, in the actual electronic circuit containing the IC, the present approach taken to "deflect" the excessive current associated with the over-voltage event from hitting the IC device is to place a surge arrestor in parallel with it. These vary from metal oxide varistors (MOV) to diodes to gas discharge tubes with each satisfying various operating parameters including trigger voltage, "clamping" voltage and response time.

The present development project was able to markedly upgrade a particular ESD surge-suppressor to make it capable of suppressing a higher power over-voltage event, using materials substitution and materials processing modification. This work entailed the substitution of both higher melting point metallization and gap filling phase, as well as improved processing, as required, in order to allow for production-level fabrication of devices.

Such devices are required in a variety of sizes and footprints that can provide for one or more signal-to-ground shunt connections per unit device. These devices will be able to be surface-mounted to PC boards for a variety of protection scenarios for over-voltage events occurring in the vicinity of delicate electronics.

- **Surge Voltage**

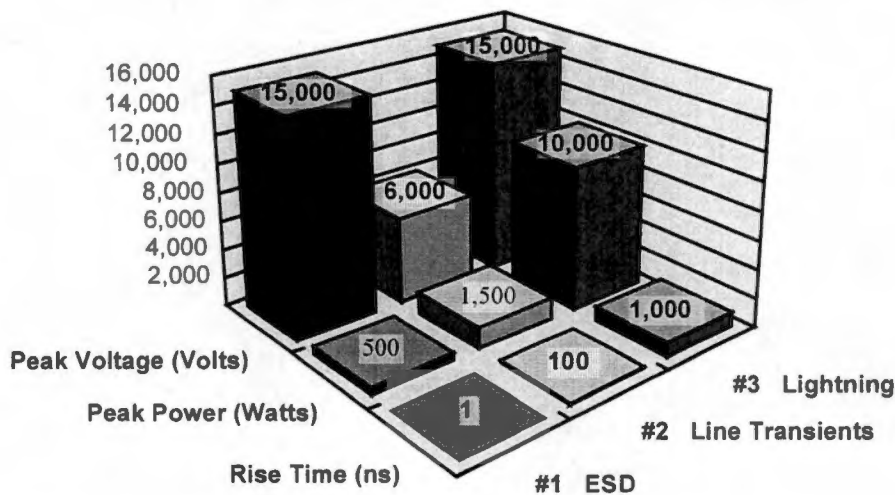
The three basic over-voltage threats are shown quantitatively in Figure 1. Electrostatic discharge (ESD) typically occurs when a person (e. g., technician, repairman) comes in direct physical contact with an operating electronic system, and static charge jumps off his/her body. Line transients are surges in AC power lines that can also induce voltage in an adjacent line. Switching response can also induce line transients. Finally, there are lightning strikes that hit either a stationary object, such as a building, or a mobile object, such as an aircraft or a missile, suddenly overloading the system's electronics. At peak power, each of these threats can destroy an IC at the local or system level.

Figure 2 illustrates two typical over-voltage-induced, non-recoverable damage events that can strike an IC. In case 1, the gate oxide in a transistor structure will be so heavily overloaded as to rupture and become filled with metal from the gate contact. In case 2, the gate metal itself can be melted and fuse open. In either case, the over-voltage can lead to excessively high ionization or resistive

heating [4]. Such failures constitute half of all "cradle-to-grave" failures of IC's. The general conclusion is that protection of the devices must be accomplished by using discrete components whose sole function is to divert over-voltage-generated current away from the IC or critical, voltage-sensitive hardware.

The growing trend in IC susceptibility to over-voltage-induced damage is extremely critical. As Figure 3 shows, the IC industry is moving toward finer circuit line widths and lower operating voltages. Accordingly, coupled with higher signal speed trends, it becomes necessary to develop surge suppressors that can exhibit low 'holding' or 'clamp' voltages once triggered into a conducting state (see below), minimal capacitance and minimal leakage current.

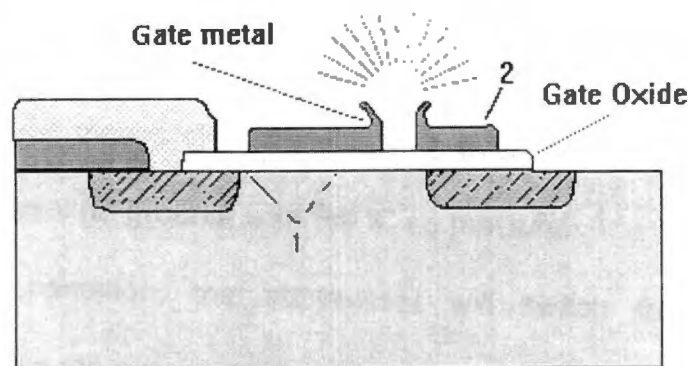
Three Voltage Surge Threats



Characteristics

Threat

Fig. 1- The three primary sources of voltage surges. The fastest rise time pulse is electrostatic discharge (ESD).



ESD Damage Mechanisms MOS

1. Gate oxide rupture.
2. Gate metal fusing.

Fig. 2- Two common mechanisms by which ESD can lead to permanent damage to the IC. In this case, transistor disrepair. From [4].

Reasons for Growth in ESD-Related Problems

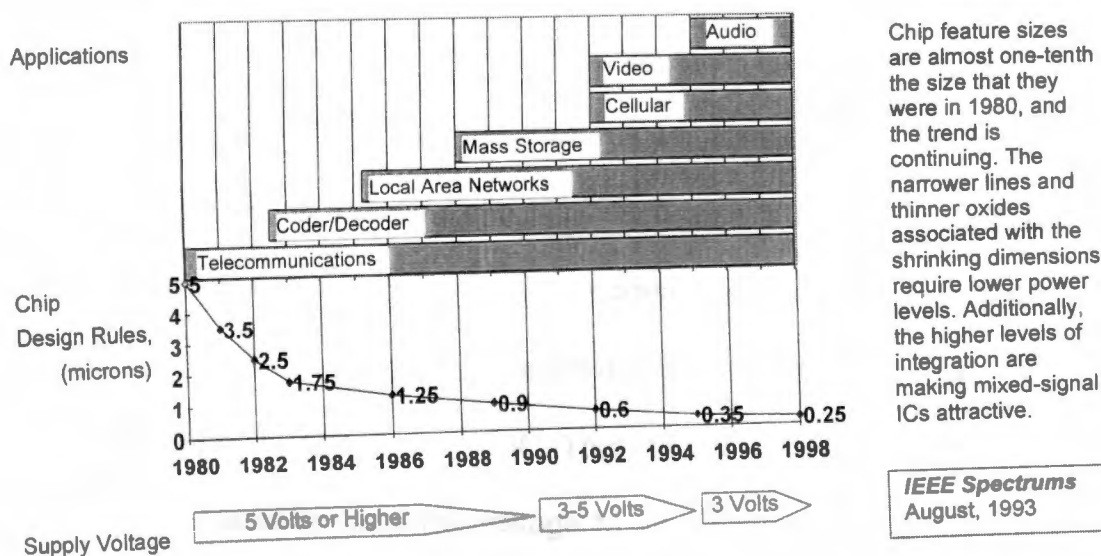


Fig. 3- Growing trend in IC line widths and operating voltages. This trend amplifies the criticality of protection against transient voltage surge.

material) at the voltage peak. The voltage then falls to the clamp voltage level until the over-voltage surge falls fully to the normal operating level of the circuit being protected.

It is desirable for a surge suppressor to exhibit the following behavior.

1. Switch from insulating to conducting as quickly as possible after the over-voltage is applied to the circuit. This is known as the suppressor's "response time".
2. Exhibit a reproducible clamp voltage that is between the normal operating voltage of the IC or hardware circuit it is protecting and the voltage that will threaten to irreparably damage the circuitry. This is often called the "threat voltage".
3. Exhibit minimal leakage current and minimal capacitance during normal voltage operation of the circuit being protected. Low capacitance is a paramount issue in particular in higher speed circuits, because fast signals will be more susceptible to distortion due to capacitance interaction with circuit elements [5] (see Figure 6).

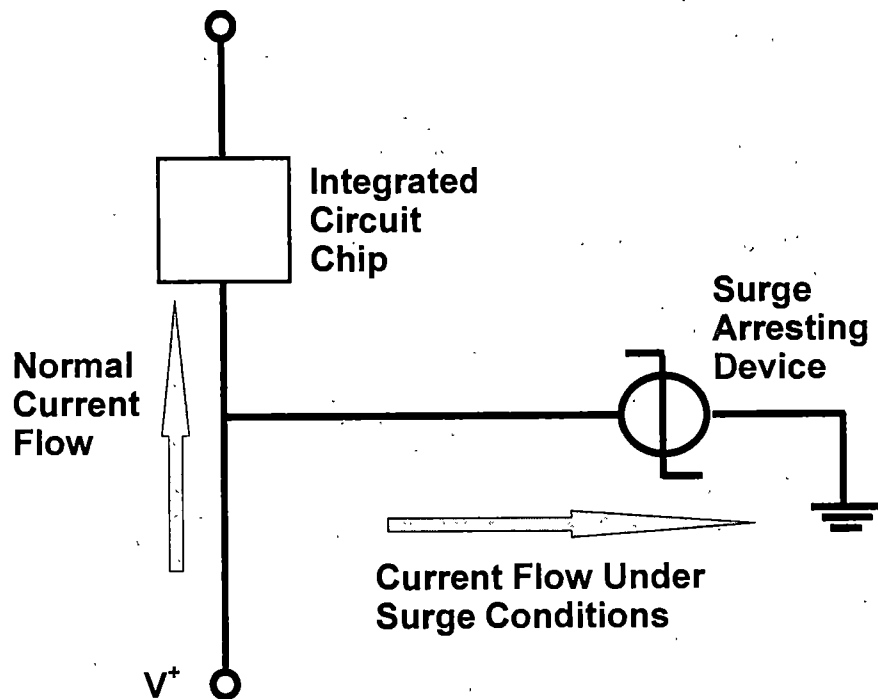


Fig. 4- Simplistic schematic depicting the use of a surge suppressor placed in parallel to the IC with respect to ground.

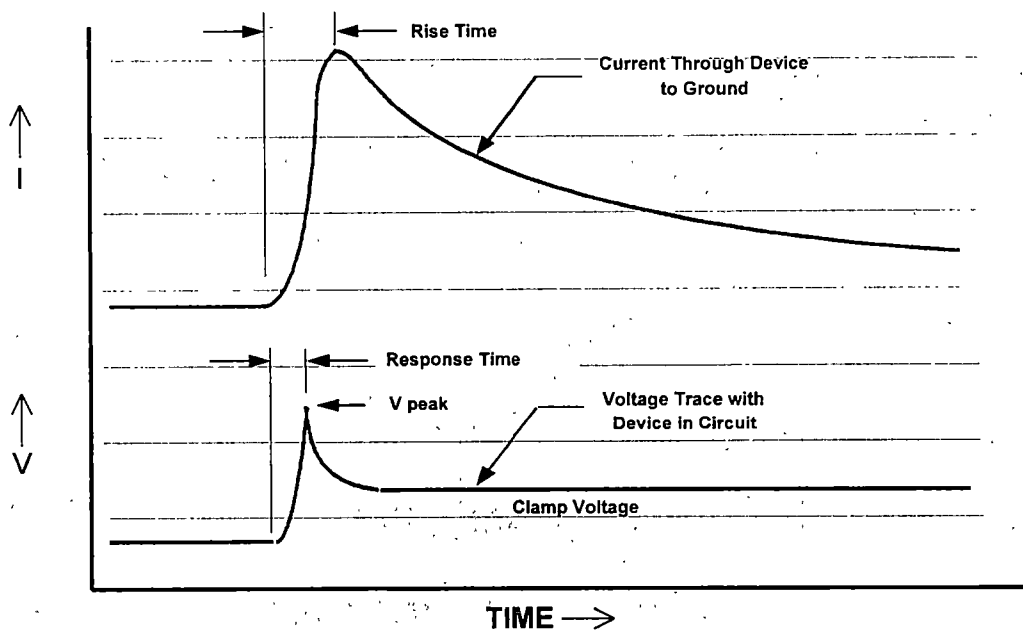


Fig. 5- A waveform trace indicating that a rapidly applied over-voltage surge will trigger a surge arresting device to switch from an insulating state to a conducting state.

- **Surge Suppressors**

A surge suppressor is a device that will switch from an insulating to conductive state at a given nominal "threat" voltage. This behavior can be depicted in a plot of current (I) vs. Voltage (V) as shown in Figure 7. Preferably, this switching is fully reversible, after the over-voltage event is over.

Two popular, commercially available surge suppression devices are diodes and varistors. In the case of diodes, there are two principal types: avalanche and tunneling. Avalanche diodes consist of a p-n junction aligned in the direction of current flow n-to-p. At a given voltage, electrons begin to flow across the junction colliding with the lattice and liberating more electrons into the current flow.

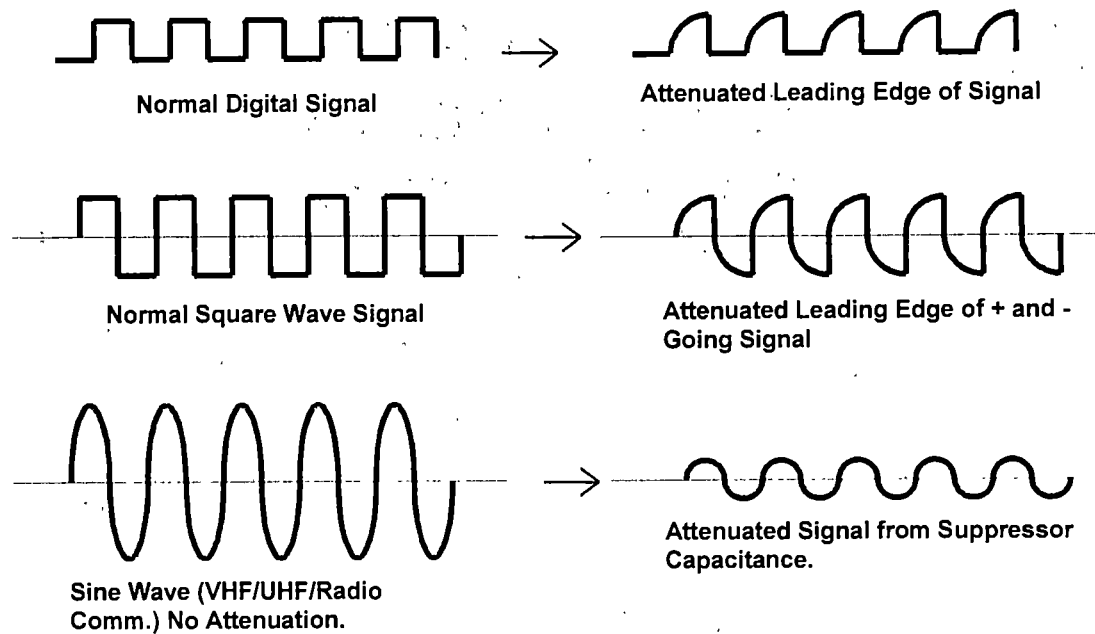


Fig. 6- Square and sinusoidal input signals vs. signals distorted by capacitance in parallel to the circuit.

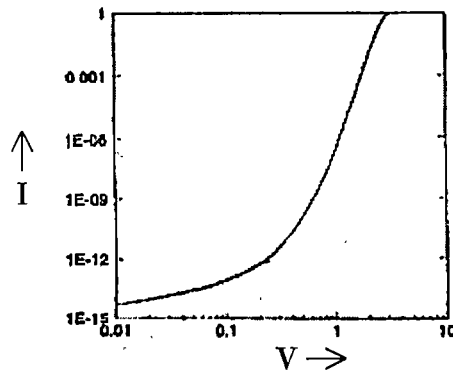


Fig. 7- I-V curve showing sudden change in resistance of suppressor over a narrow voltage range.

Tunneling diodes can be made as p-to-n devices with additional doping of the parent semiconductor, over the doping scenario used for an avalanche diode. Tunneling is a basic phenomenon that exhibits a sharp non-ohmic response (change in resistance versus voltage) at voltages that are in large part a function of the doping concentration and doping transition thickness [6-10].

Most varistors are zinc oxide (ZnO) based compositions. The electronic microstructure of correctly processed zinc-oxide varistors is described as follows.

Each grain has a negative charge at the grain boundary that in turn induces a positive charge in a region just beneath it in the grain itself. This is known as the depletion zone because it is depleted of negative charges. This polarized surface represents an electrical barrier to conduction where there are isolated negative charges on the grain surface, but they are held down by the induced Faraday charge beneath it in the depletion zone. This is known as a Schottky barrier. Between grains is an electrically insulating intergranular phase, and on the opposing sides of the intergranular phase are mirror images of a Schottky barrier. This is known as a double-Schottky barrier (Figure 8). Its significance lies in the fact that the overall electrical energy barrier required to be crossed is not merely the surface charge/depletion one dipole, but also the adjacent grain's own surface n-p/p-n junction structure. In short, the mirroring of the Schottky barriers is part of the overall conduction barrier level [11-12].

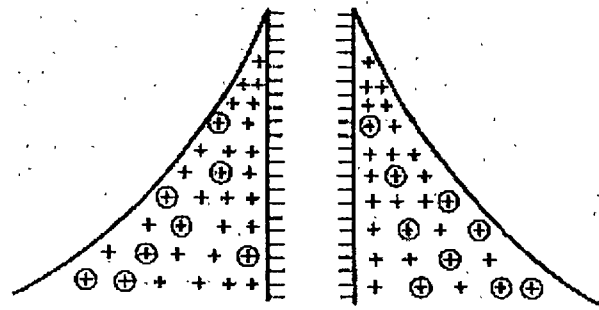


Fig. 8- Depiction of double-Schottky barrier. Center vertical region is grain boundary.

The general theory of the insulating to conducting transition in such a microstructured material is the overcoming of the energy barrier established by the Schottky barrier so as to liberate the free electrons from the grain surface and re-supply them from the over-voltage itself. Once the charge is both liberated from the Schottky barrier and given sufficient potential, it will cross over the intergranular phase via thermionic emission at low voltages and tunneling at higher voltages. This potential must also be sufficient to propagate an electron past the next Schottky barrier it sees and so on. Because this transition can occur over a small change in voltage, this provides a stark contrast between the material's insulating and conductive state. This general behavior is comparable to solid state diodes in that the double Schottky barrier can be considered to be opposing p-n junctions. The clamping voltage of a ZnO varistor will clearly vary

with overall thickness (i. e. total number of grain boundaries per direction) [13-15].

- **Present Suppressor Concept**

To date, Oryx Technology Corp. (Fremont, CA) has successfully designed devices for the suppression of ESD transient voltage events. As depicted in Figure 9, this device is essentially a micro-spark gap with a dielectric or "net" dielectric filler placed in the gap (MGDF).

The utility of this simple design includes:

1. Simple means of regulating the dielectric filler thickness, and
2. In-plane grounding of the over-current.

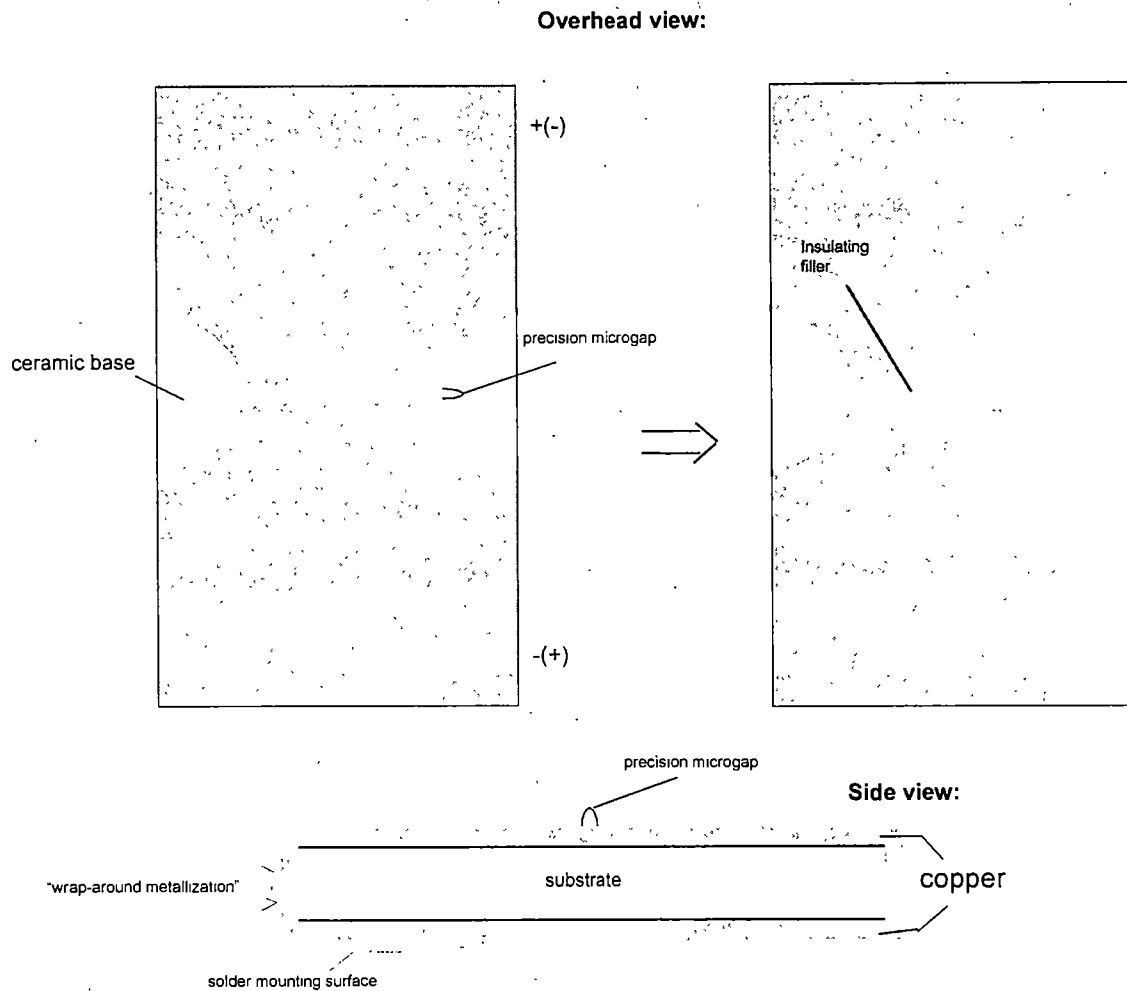


Fig. 9- Overhead and side views of a single signal line-to-ground surface-mount component prepared with a microgap.

- **Theory of Device Behavior**

The MGDF device behaves in a manner completely consistent with dielectric breakdown theory. Other surge suppressors (e. g., Zener diodes and varistors) achieve high non-linearity of resistance versus voltage through specific conduction mechanisms such as quantum tunneling and double Schottky barrier collapse. The MGDF device displays non-ohmic resistive change through the design of an insulator or insulator/conductor composite in which a sufficient number of its valence band electron population can be forced into its dielectric structure's conduction band. In simpler terms, an insulator is only an insulator until sufficient voltage is applied across it to liberate a representative number of its internally-bound electrons. **This process is termed "dielectric breakdown"** [16-18]. In reality, there is clear indication that this breakdown is accompanied by thermionic emission (i. e. transfer of thermally emitted electrons) across the dielectric space [19]. This can be considered equivalent to electrons from the signal contact being injected directly into the conduction band of the dielectric phase.

Dielectric breakdown can occur in approximately 1 ns and is accompanied by a several order of magnitude drop in the resistivity of the dielectric being evaluated. Breakdown occurs at a given potential across the dielectric known as the "breakdown voltage". By definition, the breakdown voltage is given by

$$V_b = K_s \times t, \quad (1)$$

where K_s is the material's inherent property known as its dielectric strength given in terms of potential/distance (e. g., V/mm), and t is the thickness of the dielectric sample being evaluated (Fig. 10) [16-18]. A material of thickness, t , will require a voltage be established across it equivalent to the thickness times the dielectric strength of the material. This means that, due to the rapid rise time of the voltage pulse, traditional dielectric strength values taken under steady-state conditions will be approximate.

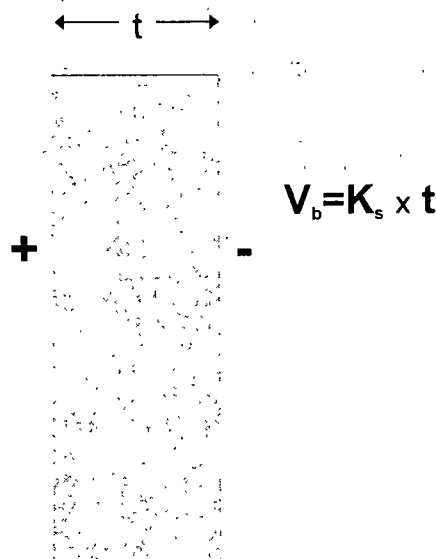


Fig. 10- Simple depiction of dielectric breakdown conditions.

When applying an ESD pulse across a given dielectric of a given thickness and with a given characteristic dielectric strength, breakdown will occur when the breakdown voltage is reached. The breakdown event, as recorded on an adequately fast oscilloscope, will be characterized by a peak voltage and a clamp voltage. The actual time of switching of the dielectric is not necessarily the time necessary for the peak voltage to be reached. However, for the sake of discussion, we will assume that it is.

The peak voltage will follow the breakdown voltage in the manner represented in equation (1). During the breakdown event, the dielectric becomes a conductor and excess current flows through the suppressor and away from the IC. Once the peak is reached, the voltage will collapse to a nominal voltage range within a finite time period shortly after. This voltage is an inverse measure of the conductance of the suppressor, that is the degree to which the suppressor converts to a conductor and how fast. The voltage that is recorded at this point is termed the "clamp voltage", which by definition is the voltage across the IC being protected while the breakdown event is being maintained.

Such a concept can be put to use in the design and fabrication of a surge suppressor provided that the following criteria are met.

- The breakdown event must be fully recoverable, that is the suppressor must become a full insulator after the over-voltage event ceases.
- The suppressor, as largely characterized by its composition and configuration (including thickness) must exhibit adequately low peak voltage, clamp voltage, time of activation (response time) and any other performance parameters of application-specific interest (e. g., leakage current and/or capacitance).

By introducing conductive particles into a dielectric matrix one is geometrically establishing a material which can undergo dielectric breakdown not through its entire thickness but only through the net dielectric path length (Fig. 11). This is the path that must be crossed in the intervening dielectric space between neighboring conductive particles within the composite because the electrons in the conductive particles are already in a liberated state. Ignoring second order effects such as inter-conductive particle scattering, equation (1) becomes

$$V_b = K_s \times \sum t_i \quad (1)$$

where t_i is the conductive particle interparticle distance.

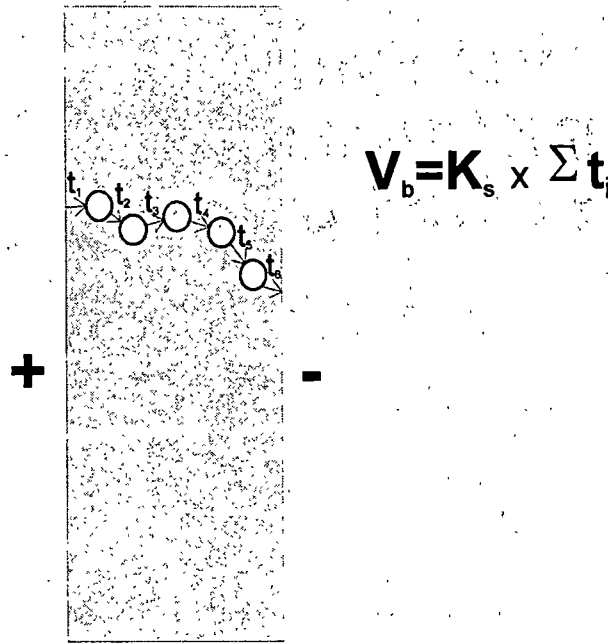


Fig. 11- Model of dielectric breakdown of composited structure. A "net" dielectric path must be crossed in order to achieve complete dielectric breakdown.

The benefit of such an approach to a MGDF design is the ability to generate a suppressor with acceptably low peak and clamp voltage values while having substantial overall thickness as opposed to the thickness required to obtain the same performance using an unfilled dielectric. The primary advantage would thus be substantial engineering simplification due to the use of a material whose operational thickness is far easier to reproducibly fabricate. Through laser micromachining, however, unfilled dielectric fillers have been shown to provide respectable suppression performance. The use of unfilled dielectric fillers allows for simplification of the filler phase formulation and application.

- **Applications**

A MGDF suppression device with higher power-handling capability has potential use in suppressing line transients and lightning strikes.

As opposed to diodes and varistors, two advantages of the MGDF concept are

1. extremely low leakage current, owing to a lack of phenomena that tend to introduce this (e. g., tunneling), and
2. extremely low capacitance during normal applied voltage, because phenomena that tend to introduce this (e. g., double-Schottky barrier structure) are absent.

Figure 12 shows a comparison of a baseline square wave passed in parallel to the various suppressors evaluated. This figure illustrates the severe damage to the clarity and amplitude of the input signal when diodes and varistors are employed. However, MGDF imparts essentially no noticeable signal attenuation. This is a paramount performance advantage of MGDF in that as IC development and operation tend toward high signal speeds, such capacitance-induced signal damage becomes an ever-increasing first order threat to chip performance.

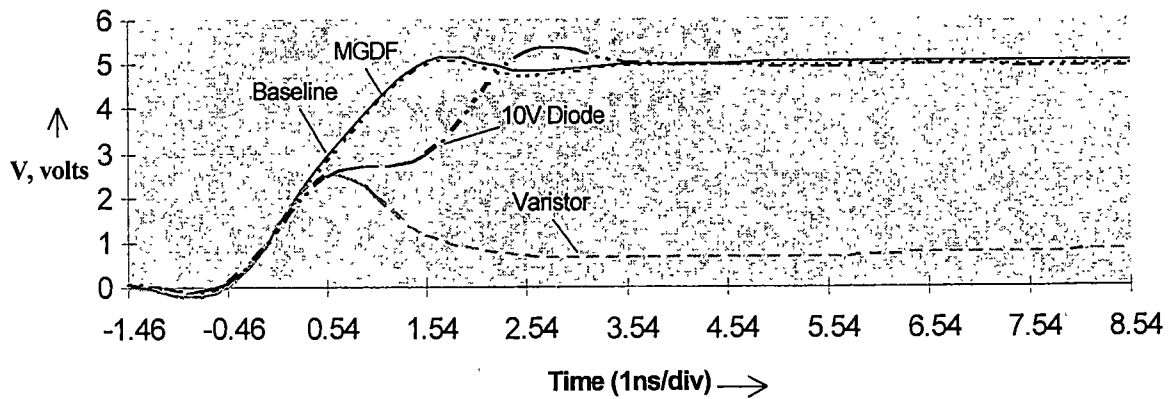


Fig. 12- Square input signals transmitted in parallel to various surge suppressors. From [20].

- **Implications for Defense-Based Systems**

Military electronics are vulnerable to exposure to an electromagnetic pulse (EMP). Such a pulse can either be generated by nuclear detonation or when lightning flashes in the general vicinity of an object such as a stationary missile or one in flight. The EMP interacts with a system in much the same manner as radio waves excite an antenna. The net effect is a current flowing on the skin and cabling of the system. The current transients are damped sinusoidally. Electronic circuits are the most sensitive components of a system. The EMP transient may cause upset or burnout of interface electronics. One hardening technique is to provide surge suppression at the input to the electronics box. The suppression device is typically a Zener diode. The disadvantage of the Zener diode is that its capacitance increases with its power handling capability. Large capacitance degrades the normal operational signal [4]. Another disadvantage is that two back-to-back Zener diodes are required to achieve bi-directional surge

suppression capability. EMP's are generally specified by equivalent current. A conservative EMP can generate 8000 amps over a $3\ \mu\text{s}$ pulse with a rise time of 100 ns [21].

As EMP represents a higher power voltage transient than ESD, there exist certain materials selection and processing issues in the attempt to create a similar device with high power handling capability.

- **Current Microgap Fabrication**

The primary method that has been investigated for the fabrication of the aforementioned microgaps is diamond wafer sawing. In the present study, Nd:YAG laser micromachining was evaluated. During such laser processing a short wavelength beam impinges upon the circuit metal surface, and a non-thermal, ablative process will remove metal in such a manner as to form a non-conductive trench as shown in Figure 13.

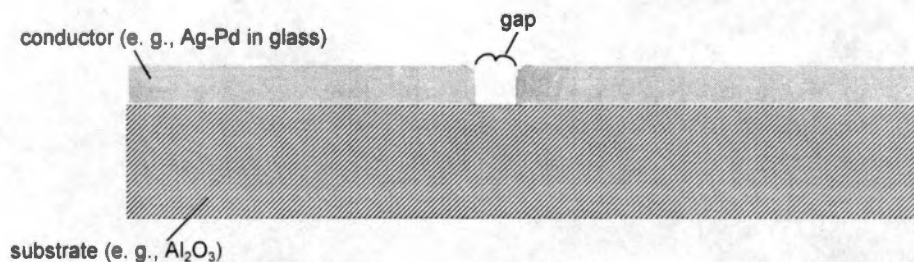


Fig. 13- Cross-section of microgap cut into the conductor on the substrate.

- **Pulsed, IR Laser Machining**

As opposed to more traditional and conventional industrial lasers (e. g., most CO₂ lasers), Nd:YAG lasers can provide for greater cut resolution, due to a shorter wavelength. When operated in a high pulse frequency mode, short bursts of laser light instigate thermal evaporation and sublimation from the cut surface with a substantially reduced thermal field. The minimization of thermal input on the cut surface allows for sharper cut surfaces to be formed without melt-induced cutting distortions. [21-22].

- **Circuit Metal Conductivity**

It should be noted that circuit metallization thickness must be adequate so that the pre-cut circuit not provide any detectable resistance of a high frequency pulse to the suppression path. Any resistance would increase the clamp voltage of the switched closed microgap because it will impede the discharge of the over-voltage from its peak value (see Fig. 14).

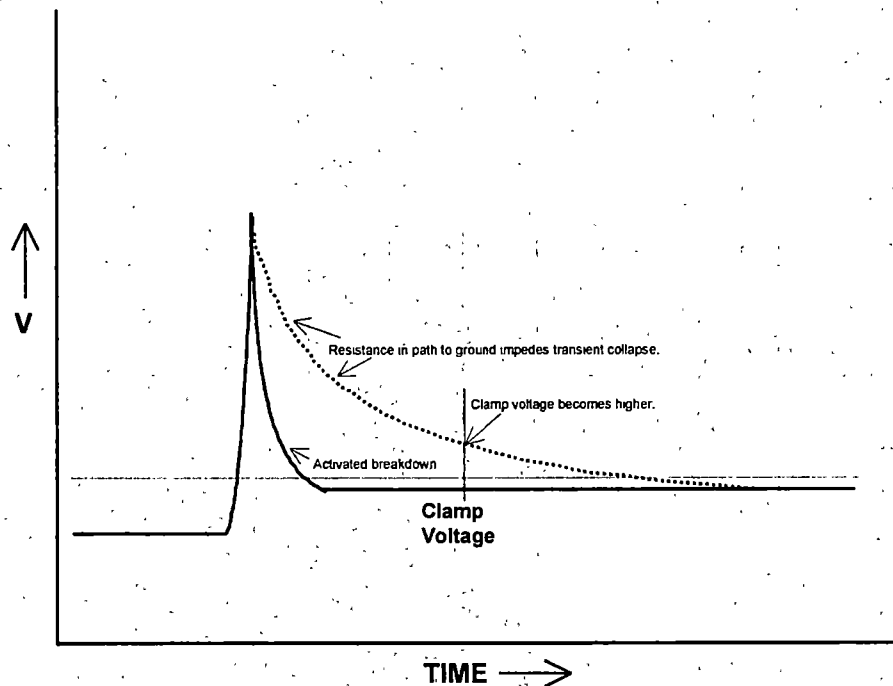


Fig. 14- Contribution to clamp voltage due to resistance of device.

A key factor in determining micromachining rate, gap width tolerance control and gap cutting resolution is metallization thickness. In order that a microgap fully open a circuit path, the gap must be cut clean through the circuit. Microgaps will be machined into the circuits through Nd:YAG laser machining. This step will include the large task of optical system customization for this application.

- **Previous Work**

The present ESD suppressor is being made by Bussmann Corp. (St. Louis, MO) by diamond wafer saw cutting of gaps approximately 25 μm in width (0.001"). These gaps are presently being cut into a thick film metallization that

consists of 90 wt. % Ag-10 wt. % Pd in a glass frit matrix. The substrate being used is a low-temperature glass tape structure [24]. This was chosen over the more conventional Al_2O_3 because of its lesser wear on the diamond wafer saw, which inevitably must score through the metallization/substrate interface in order to ensure that all gaps are cut fully through. These gaps are being filled with polymer-based dielectric ink compositions that are then cured in place.

Section 2

Technical Objectives

Research to date has shown that an ESD surge suppressor can be fabricated by wafer sawing of gaps into a device array built onto a circuit board substrate. The design of the device includes wrap-around metallization for connection of its surface mount pads to the suppression circuit region. In order to fabricate devices in a commercial arena, it is important to develop a manufacturing scenario that will have the following feature.

- Desired performance parameters,
- Low unit cost of fabrication,
- High volume fabrication capacity,
- High fabrication throughput,
- High yield

In order to redesign the existing device capable of suppressing a higher power over-voltage event, it is necessary to make materials substitutions in the device design. A comparison of the relevant materials is presented in Table I.

Table I. Comparison of Metallization and Gap Filler Materials

	Metallization	Matrix of Filler Phase
Present Design	Ag-Pd	organic polymer
Temperature Limit	approximately 1,000°C	~250°C
Proposed Design #1	Copper	Inorganic glass
Temperature Limit	$T_m=1,083^\circ\text{C}$	~500°C range
Proposed Design #2	Tungsten	" "
Temperature Limit	$T_m=3,410^\circ\text{C}$	" "

In adapting such a device to handle the substantially greater amount of energy and peak power of a line transient or a lightning strike event, certain materials selection changes were investigated. Concurrent with these changes was the introduction of laser micromachining of the device gaps.

The primary limitations of the presently designed device are those materials issues which make such components incapable of surviving the power associated with the switching and grounding response of current associated with substantially higher transient over-voltage strikes.

In order to allow for the most conservative approach to developing a higher power surge-suppressor, the following changes to device materials selection are proposed.

First, the substrate selected for the device was 96 wt. % Al_2O_3 (CeramTec, Inc., North Mansfield, MA). This is a simple-to-process, readily available and commercially-acceptable substrate material [25-28]. In addition, conventional thick film metallization inks are available for metallization of the ceramic with refractory metals having reasonably low electrical resistivity [29]. These are principally Mo and W-based pastes [30-32]. Second, one key metallization evaluated was tungsten-based due to tungsten's extremely high melting point. In those areas away from the gap region, where soldering is to take place, conventional electroless-nickel plating can be performed [33]. Third, the gap-filling material, that is the dielectric switching material, was switched from an organic polymer to an inorganic glass in order to substantially reduce if not fully eliminate the susceptibility to thermal decomposition of the switching/breakdown phase during its electrically closed/current draining period. As compared to an ESD event, a line transient or lightning strike will provide substantially greater current density through the dielectric during breakdown.

It should be noted that the use of a glass-based filler phase separately supported the choice of Al_2O_3 over glass tape as the substrate material because it will be expected to undergo more controlled interfacial solubility reactions with the glass ink during its furnace fire-on step [34].

Section 3

Experimental Approach

Al_2O_3 substrates were procured from CeramTec (North Mansfield, MA). These substrates were then thick film metallized using

- copper-based thick film ink, and
- tungsten-based thick film ink.

These substrates were then fired under appropriate conditions for each metallization. The final metallized substrates were then subjected to laser micromachining in order to generate nominal gap widths of 10 and 25 μm through the trace. The laser processing conditions for each metallization were as cited in Table II.

Figure 15 shows a schematic that was generated for the screen printing of Cu and, separately, W metallizations onto 96% wt. Al_2O_3 substrates. The array pattern was set to allow for 1920 device sites on a 4.527" x 4.527" (115 mm x 115 mm) square substrate, 0.025" (0.635 mm) thick and 0.010-0.012" (0.254-0.306 mm) cutting kerf between each row and column. The screen printing and firing of these metallization patterns was performed by Delta V Electronics (Sunnyvale, CA).

Table II. Laser cutting conditions for the different metallizations used.

Metal	Attempted Gap Width, μm	Laser Processing Conditions
W	10	3.4W, 5000 mm/min., 10 kHz
W	25	7.6W, 3000 mm/min., 10 kHz
Cu	10	7.6W, 5000 mm/min., 10 kHz
Cu	25	10 W, 5000 mm/min., 10 kHz
Ag	10	0.9W, 5000 mm/min., 10 kHz
Ag	25	1.3W, 5000 mm/min., 10 kHz

Laser: Nd:YAG, $\lambda=1.06\mu\text{m}$

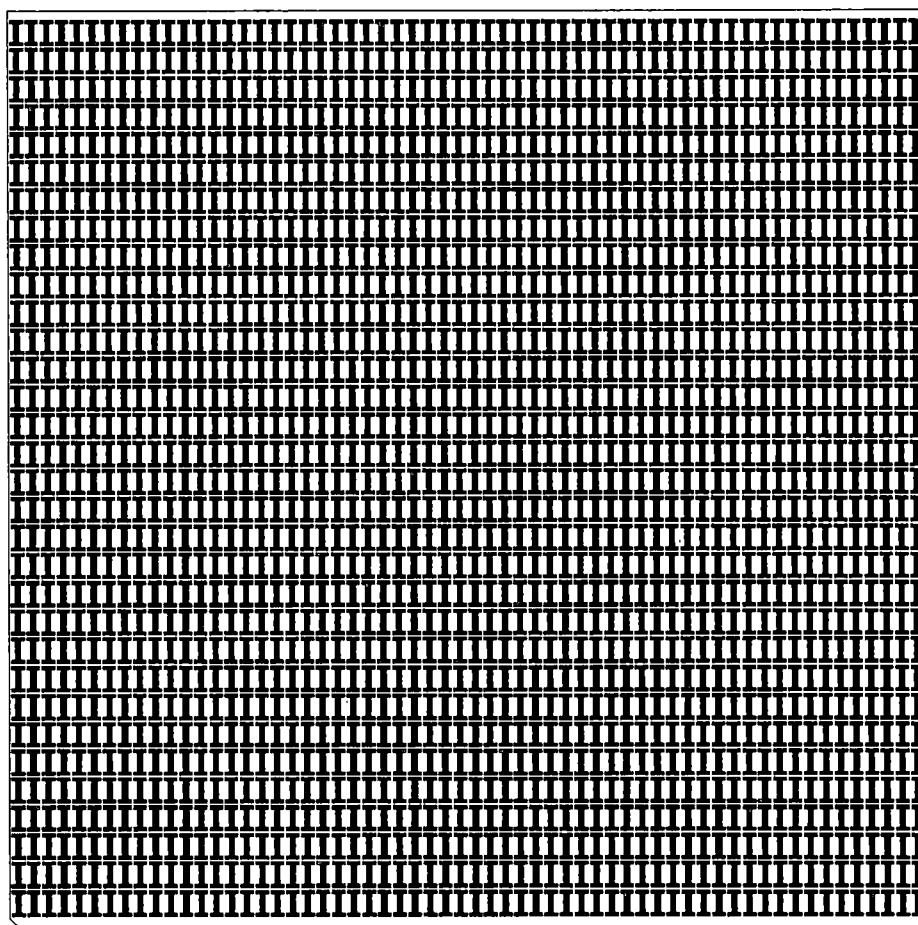


Fig. 15- Schematic of 1920 devices arrayed on a ceramic substrate.

Substrates were fabricated using W and Cu thick film metallization. In the case of W metallization, $\sim 1 \mu\text{m}$ of electroless nickel plating was applied on top for purposes of eventual solderability.

In addition to the copper and tungsten metallized substrates, 1206-style devices were also provided by Bussmann Corp. (St. Louis, MO). These devices were already diced and were fabricated using 90 wt. % Ag-10 wt. % Pd thick film metallization on 96 wt. % Al_2O_3 . Some of these devices had gaps sawed to a nominal width of $25 \mu\text{m}$, while others had no gaps so that laser gap cutting could be performed on them.

As it was believed that only copper and tungsten would be candidates for a high power device, complete substrates were only prepared for the Cu and W metallizations. Profilometry of 54 data points, 27 on each of two different substrates, showed the average metallization thickness of the copper and tungsten to be approximately $18.59 \mu\text{m}$ (standard deviation, $\sigma=1.1 \mu\text{m}$) and $13.07 \mu\text{m}$ ($\sigma=1.4 \mu\text{m}$), respectively. The substantially greater thickness of the copper metallization is believed to be due to the print thickness variability of this particular ink.

A Nd:YAG laser was used to micro-machine gaps into the metallization layers using different gap widths. One substrate each of the copper and tungsten-

metallized substrates as well as 170 of the discrete (already diced) Ag-Pd metallized devices (in a 10 x 17 array of pre-singulated parts) were then sent to Exitech Ltd. (Oxford, UK) for laser gap cutting. Gaps were cut at approximately 10 and 25 μm nominal gap width.

There is a measured difference between attempted gap width and measured gap width. Some of these devices were then tested for their ESD suppression performance.

Gaps were tested under ESD conditions as both air gaps and with an organic polymer filler. In addition, parts were also evaluated under lightning simulation conditions with primary emphasis on the evaluation of copper and tungsten metallization with an inorganic glass filler.

Section 4

Results and Discussion

As the presented microscopy indicates, gap widths do not fully conform to the desired dimensions. Accordingly, those devices with gaps that were prepared for 25 μm width and those for 10 μm width will be referred to as nominal 25 μm and nominal 10 μm , respectively, regardless of the actually observed (and reported) gap width.

Apparent oxidation at the cut surface gave rise to an attempt to clean these regions through plasma etching since oxidation could lead to increased device resistance and therefore higher clamp voltages.¹ Figures 16 to 18 are low magnification photomicrographs (30X) of an entire device top surface for silver, copper and tungsten-metallized 96 wt. % Al_2O_3 , respectively, with nominal 25 μm wide gaps laser machined into them followed by plasma cleaning. The excess metallization on the ends of the Ag-metallized piece is due to a post-firing step performed by Bussmann in order to establish a wrap-around metallization on the edge of each device. This allows for "surface mounting" of these devices to a printed circuit board in a "face-up" orientation.

¹ In the case of Ag, it is possible that the corrosion would have been a sulfate since its oxide is not very stable.

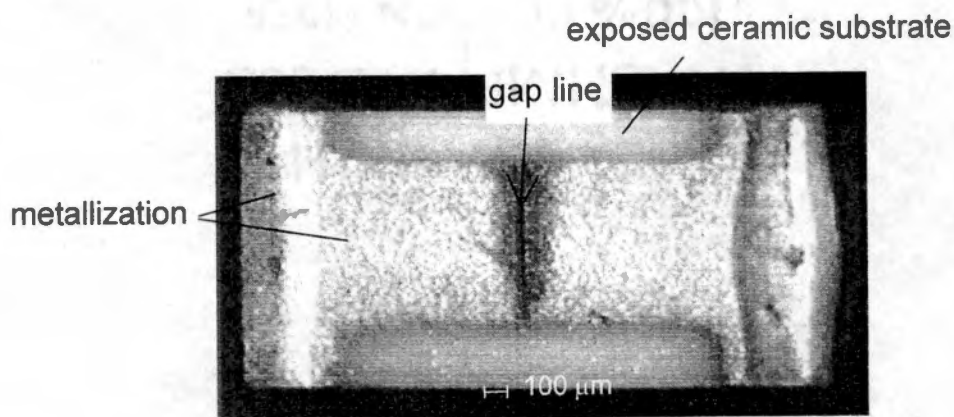


Fig. 16- Top surface of silver-metallized surface with nominal 25 μm laser-machined gap.

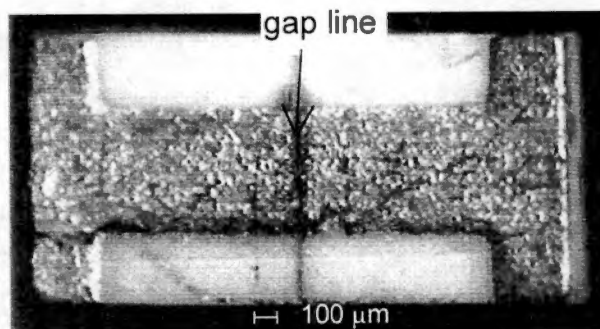


Fig. 17- Top surface of copper-metallized surface with nominal 25 μm laser-machined gap.

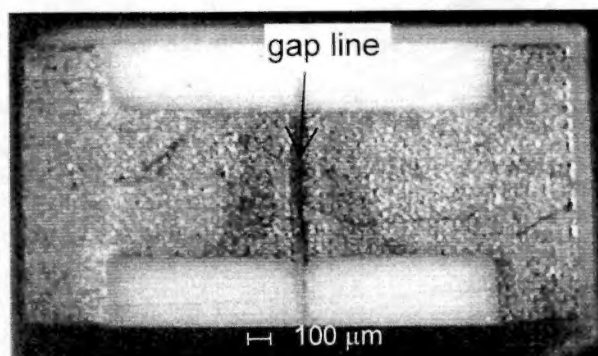


Fig. 18- Top surface of tungsten-metallized surface with nominal 25 μm laser-machined gap.

The laser cut parts exhibited a discoloration at the cut lines. Figure 19 is a reflected light image (100X) of a nominal 10 μm cut on a copper metallization part.

For comparison purposes, some parts were then plasma cleaned @ 300 W, 500 microns pressure in a 10 vol. % H_2 – 90 vol. % He mixture for 40 minutes. This was followed by testing of these parts as air gap, spark arrestors. Subsequent to these tests, other parts were plasma cleaned followed by filling of the gaps with a straight unfilled polymer resin which was then cured @ 100°C for 1 hr. These parts were, in turn, also tested as surge suppression devices. Unfilled gaps from each of the three metallizations, pre- and post plasma cleaned were sent to Surface Science Lab (Mountain View, CA) for top and cross-sectional inspection.

Figure 20 shows a nominal 25 μm gap in copper that started with comparable discoloration to that shown in Figure 18, after plasma cleaning.

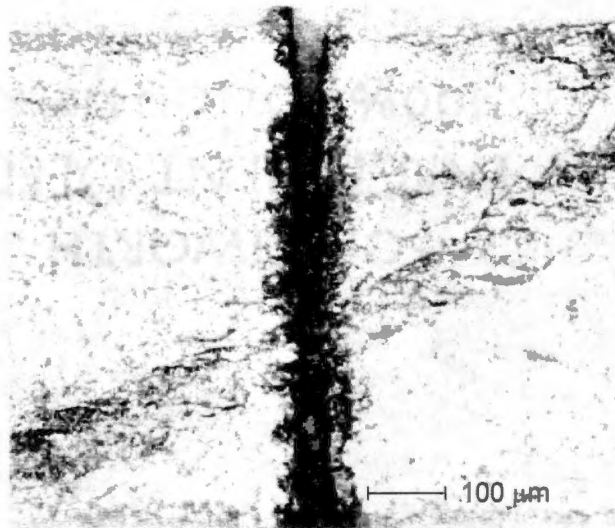


Fig. 19- Optical micrograph of a nominal 10 μm cut in a copper metallization layer.

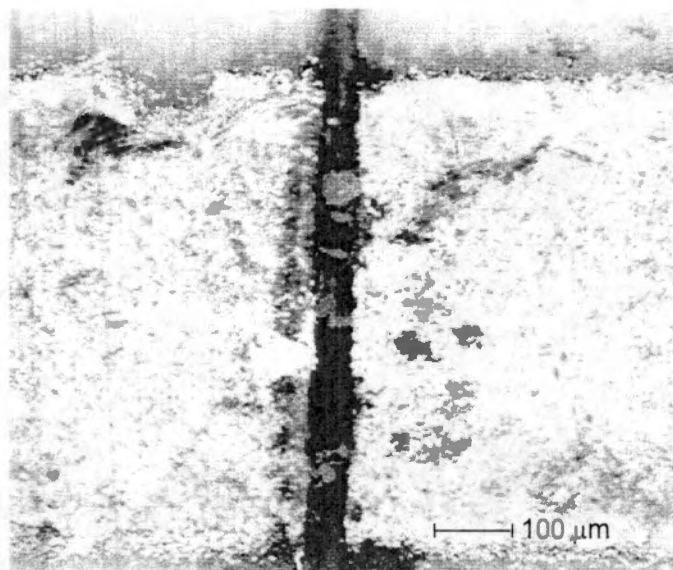


Fig. 20- High magnification optical micrograph of a nominal 25 μm cut in copper metallization layer.

The difference in chemistry at the cut surfaces is more evident through SEM x-ray microprobe analysis. Figure 21 is a higher magnification secondary electron image (840X) of the cross-section of a copper-metallized device cut to a nominal 25 μm width. In this image one can see tapering of the cut from a width of approximately 41.6 μm down to 27.9 μm at the ceramic/metal interface. Also apparent is some undercutting into the substrate. The taper is approximately 40° (included angle). The metallization thickness at the gap is approximately 25.6 μm . Figure 22 is an x-ray dot map for copper.

Of greater note is the presence of scattered lead in the metallization as seen in Figure 23, located in those regions appearing to be depleted of Cu in Figure 22. Lead is present because leaded silicate glasses are generally "fritted" with metal powders in the formulation of metallization inks. This allows for the formation of a liquid phase at or below the metallization temperature, which can migrate to the ceramic/metal interface and establish a chemical transition zone. In addition, this glass can react with the copper powder and partially co-sinter with it.

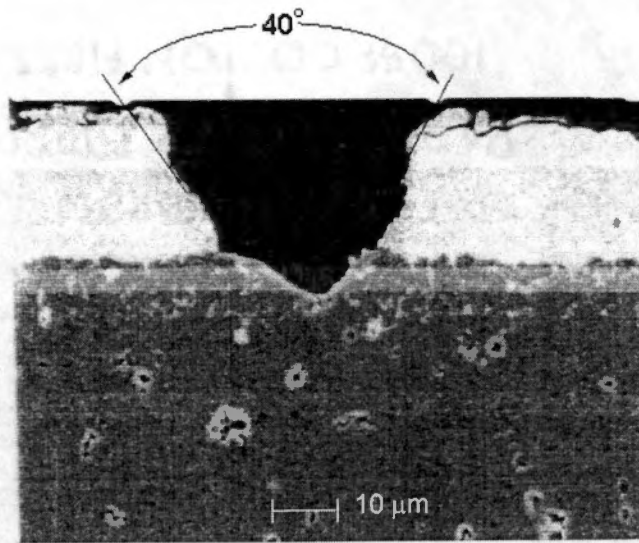


Fig. 21- A secondary electron image of a cross-section of nominal 25 μm cut in copper metallization layer.

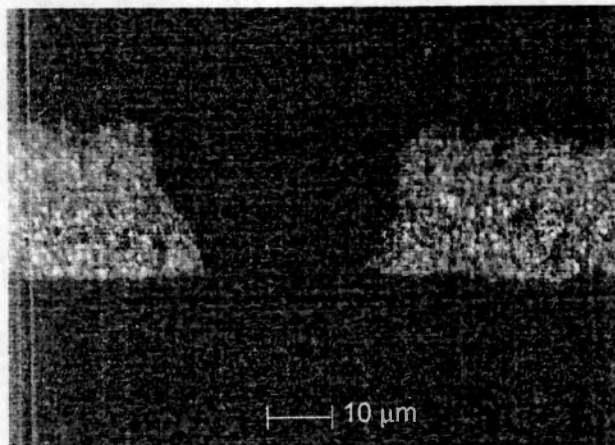


Fig. 22- EDX dot map of Figure 21 for Cu.

Figure 24 is a high magnification micrograph (1,000X) of another copper metallization cut to a nominal 25 μm width. Here one sees a gross over-cutting of the width to approximately 42 μm . The width of the undercut into the ceramic substrate at top is approximately 26-27 μm and thus indicates that perhaps the metal was removed adjacent to this cut (perhaps by fracture of the glassy phase or polishing). The metallization thickness at the gap is approximately 18.1 μm .

Figures 25 and 26 are the high magnification secondary electron image (1,000X) and the corresponding copper dot map for a gap cut to a nominal 10 μm gap width. Some under cutting into the substrate is apparent, as is the voiding in the metallization at the interface and along the left side of the cut region. This may have been induced by specimen polishing. Some dotting at the bottom of the cut would suggest the presence of copper in the gap. Whether this is due to redeposition or a sparse presence in a glassy phase, it is not a continuous electrical shorting path across the gap. The separation of the metallization at the interface is approximately 11.0 μm . The metallization thickness at the gap (immediate right) is approximately 23.5 μm .

Figure 27, as in Figure 22, shows dispersions of a lead-rich phase throughout the metallization layer.

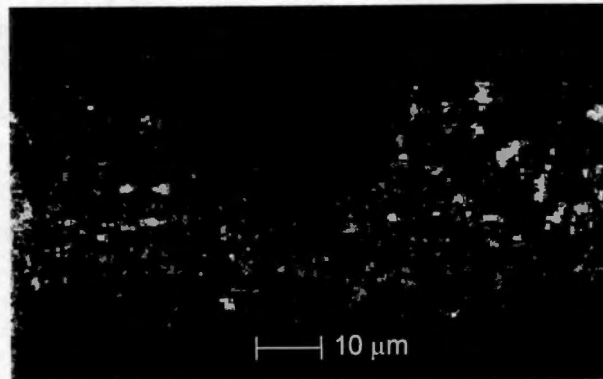


Fig. 23- EDX dot map of Figure 21 for Pb.

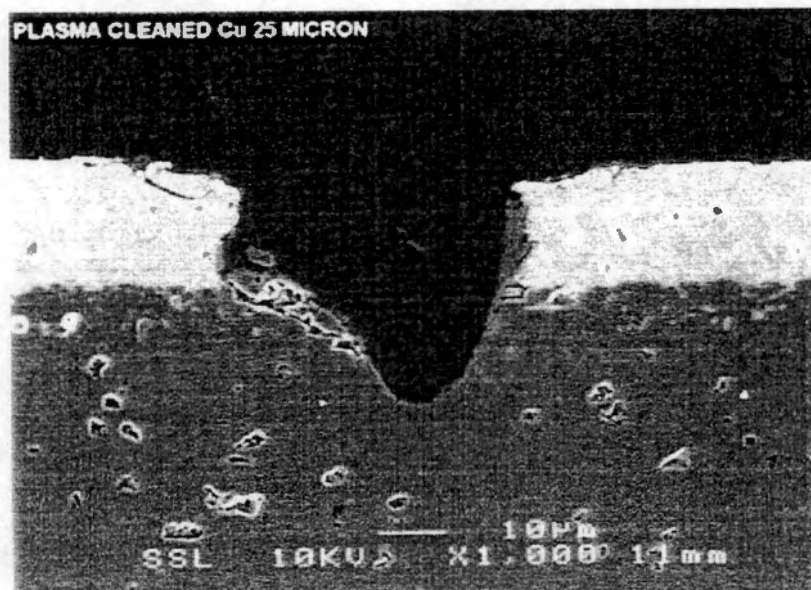


Fig. 24- Secondary electron image of a nominal 25 μm gap attempt in copper.

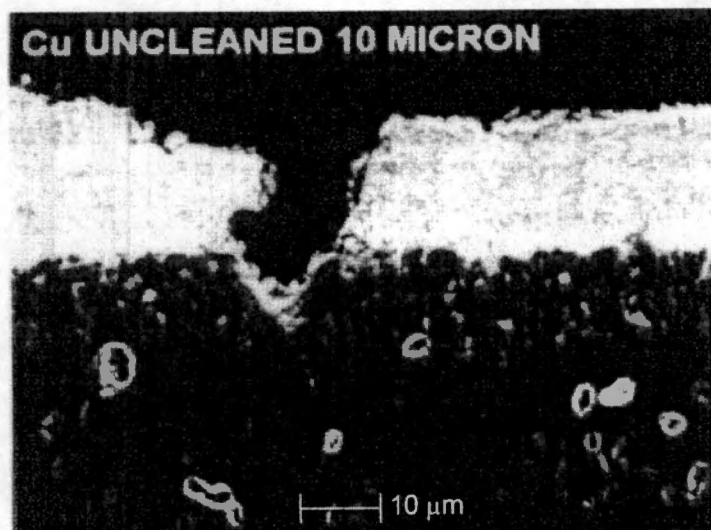


Fig. 25- Secondary electron image of a nominal 10 μm cut in copper metallization layer.

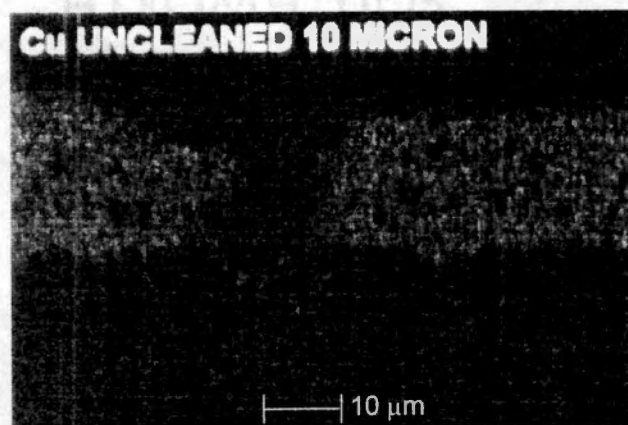


Fig. 26- EDX dot map of Figure 25 for Cu.

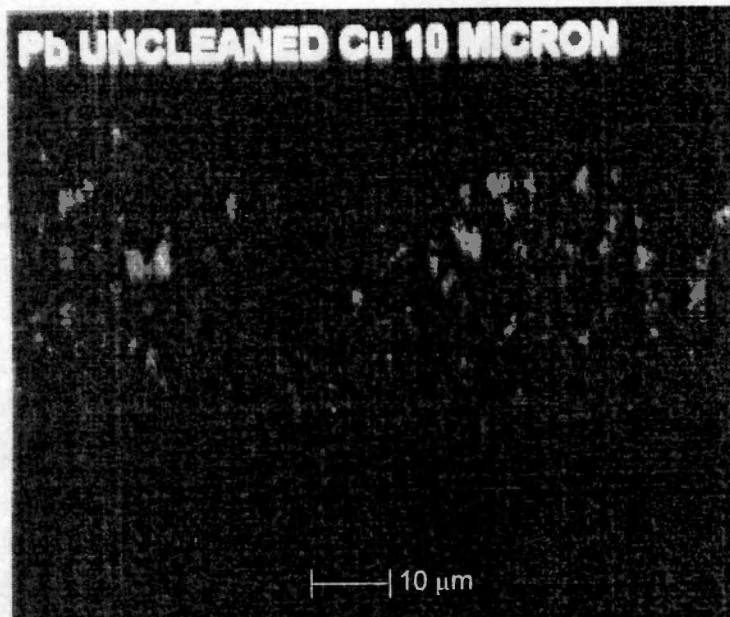


Fig. 27- EDX dot map of Figure 25 for Pb.

Cross-sectional dot mapping of the nominal 10 μm gap in copper for pre- and post-plasma cleaning could not demonstrate the presence or absence of oxygen at the cut surface. Figure 28, however, is a low magnification top view (100X) of the gap cut into the tungsten metallization to a nominal 10 μm width. Figure 29 is a dot map of this region for oxygen. Even after plasma cleaning, oxygen is found on the top of the cut walls adjacent to the gap. As this was the case with all plasma cleaned parts, no further work was explored on plasma gap cleaning.

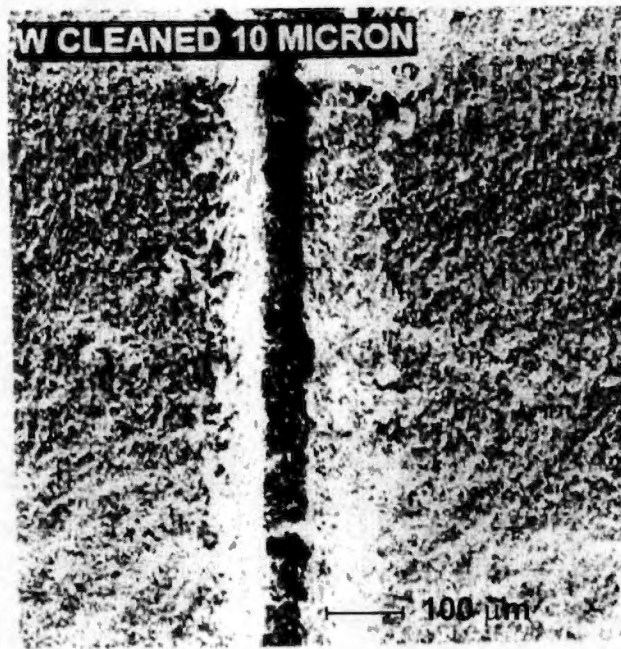


Fig. 28- Top view of a nominal 10 μm gap in tungsten metallization, after plasma cleaning.

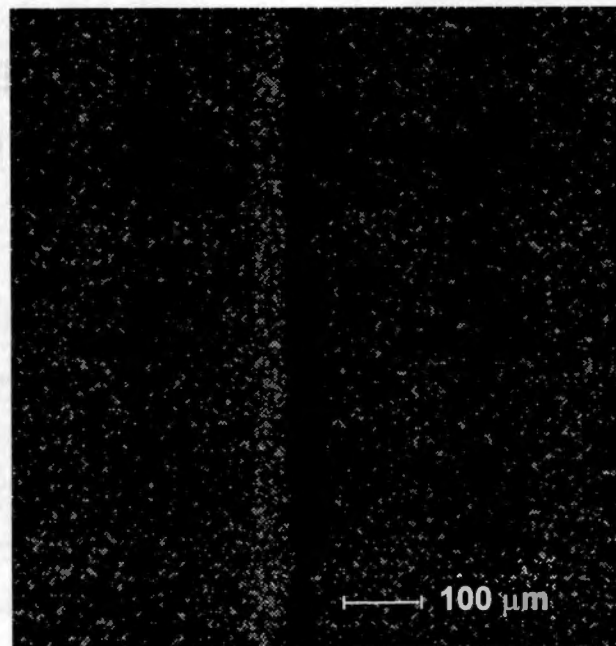


Fig. 29- EDX dot map of Figure 28 for O.

- **Additional Microscopy:**

Other micrographs of interest include Figure 30, a high magnification image (1,000X) of the nominal 25 μm cut in the silver metallization. The cross-section is tapered from 24 down to 18 μm in width at the ceramic surface. In all cases of micromachining of the silver one sees minimal undercutting into the ceramic. The metallization height at the gap is approximately 15.6 to 17.2 μm . This is most likely due to the lower power used to cut the silver combined with aluminum oxide's relatively high melting point. The apparent porosity is actually entrapped glassy phase in the metallization layer.

Figure 31 is a high magnification image (1,000X) of a gap in the tungsten metallization cut for a nominal 25 μm width. The metallization thickness at the gap is approximately 12.8 μm .

The taper in this part is most severe, most likely owing to the high power of cutting and the particular cutting behavior of tungsten. The gap width tapers from ~39.4 μm down to 22.2 μm . This corresponds to an included angle of approximately 70°.

Figures 32 and 33 are high magnification secondary electron and EDX images (1,220X) for Ag cut to an attempted 10 μm in width. In addition, minimal

undercutting into the substrate is seen. The metallization thickness at the gap is approximately 15.5 μm .

Figures 34 and 35 are secondary electron and EDX images (850X) for tungsten cut to a nominal 10 μm gap width. The gap width at bottom is measured to be approximately 13.6 μm . In addition, as with the silver metallization, minimal undercutting into the substrate is seen. The metallization thickness at the gap is approximately 16.1 μm . This cross section shows the gap tapering up from 14.8 μm at the interface to 19.7 μm at top.

A summary of gap dimensions in the show microscopy are shown in Table III. The data is based on a single part for each type selected as a representative part after optical microscope inspection of a diced device array.

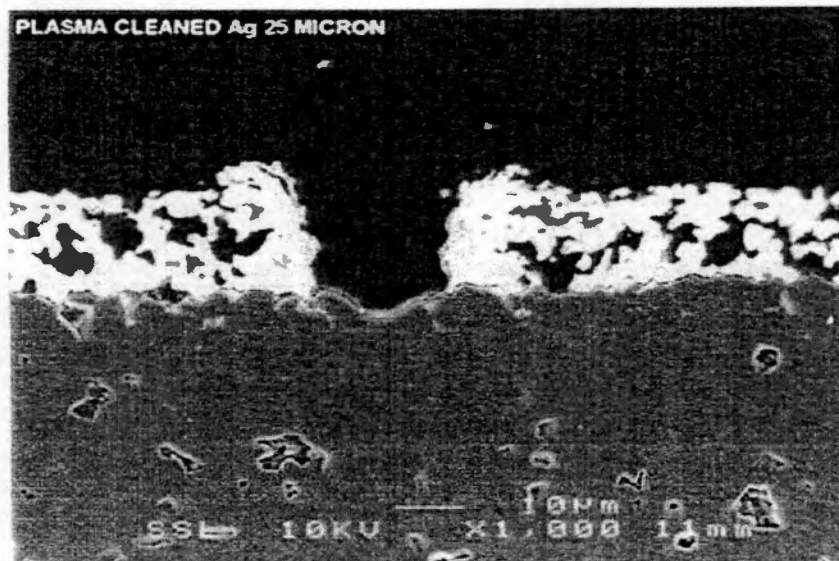


Fig. 30- Secondary electron image of a nominal 25 μm cut in a silver metallization layer.

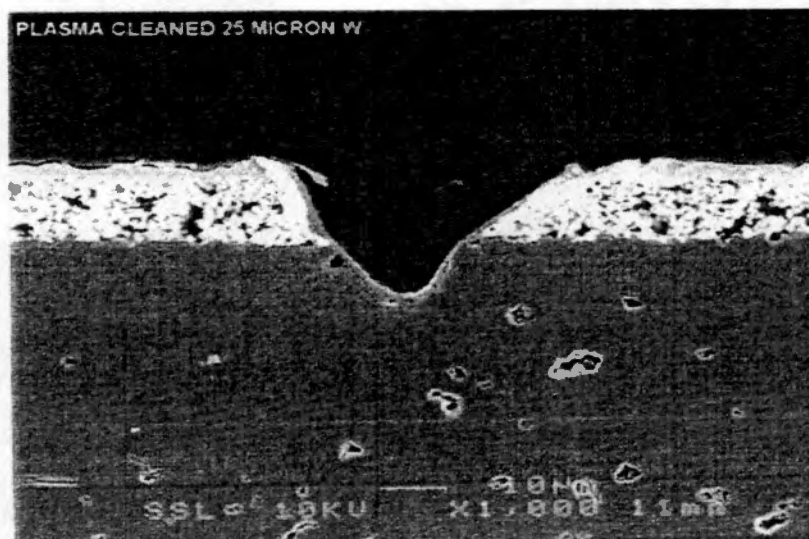


Fig. 31- Secondary electron image of a nominal 25 μm cut in tungsten metallization layer.



Fig. 32- Secondary electron image of a nominal 10 μm cut in silver metallization layer.

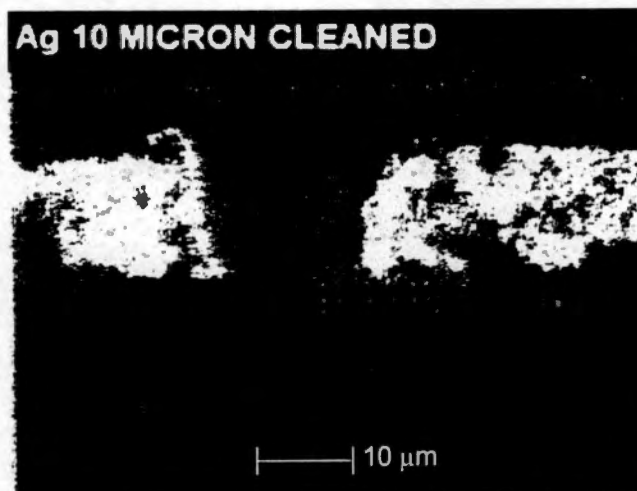


Fig. 33- EDX dot map of Figure 32 for Ag.

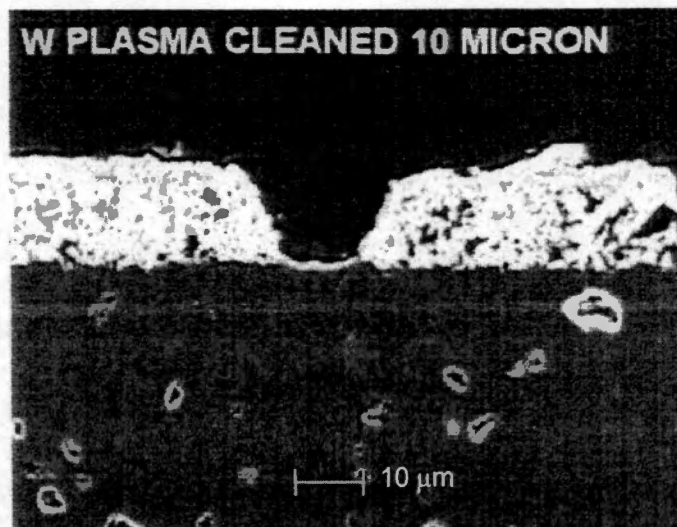


Fig. 34- Secondary electron image of a nominal 10 μm cut in a tungsten metallization layer after plasma cleaning.

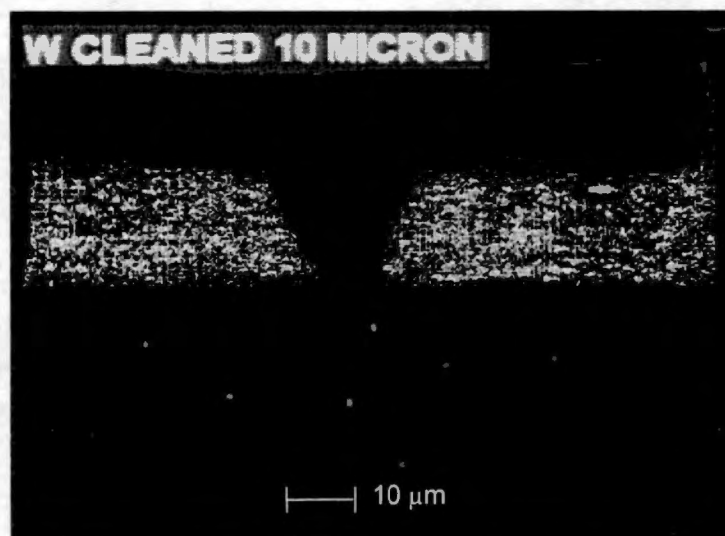


Fig. 35- EDX dot map of Figure 34 for W.

Table III. Measured cut dimensions in the different metals.

metal	nominal gap width (μm)	metallization thickness (μm)	min (μm)	max (μm)
Ag	25	15.6-17.2	18	24
Ag	10	"	14.8	19.7
Cu	25	18.59	27.9	41.6
Cu	10	"	10.9	n. m.
Cu*	25	"	20	30
W	25	13.07	22.2	39.4
W	10	"	13.6	n. m.

{n. m.= not measured}

* separate laser processing discussed further on under lightning testing.

- **ESD Test Data**

10 samples each of the nominal 25 μm gaps in silver, copper and tungsten were placed in a sample holder designed to apply an ESD pulse from the gap side of the device (since the Cu and W metallized parts had no wrap-around metallization) and subjected to 12kV ESD surges (peak power of 840W) per IEC 1000-4 specification using an Oryx Technology Model 700 ESD tester and a Tektronics TDS 644A digital oscilloscope with a Tektronics CT-2 voltage probe. 1004-2 describes a 1 ns. rise-time pulse with 60 ns duration across a 330 Ω resistor.

The sample holder (exploded and assembled views) is depicted in Figure 36. The ESD test set-up is shown in Figure 37. Parts were tested for voltage peak, clamp voltage, peak current and exhibition of any permanent electrical shorting

events. Each part was subjected to 50 ESD pulses and mean parametric values calculated and tabulated.

Tables IV to VI show the summarized test results from the collected data. Appendix A shows the complete data with Table IV-B corresponding to Table IV, and so on. Because the key operational parameters are voltage peak (V_p) and clamp voltage (V_c) the combined means of these values are also presented. Beneath the appropriate data columns for V_p and V_c , and their respective standard deviations, are values for grouped averages followed by averages following the removal of all data points from those samples that exhibited at least one electrical shorting occurrence. All V_p values are presented with a 300V baseline correction due to the impedance of the test system and device holder.

In addition, silver, copper and tungsten parts which were laser cut to 10 μm nominal slot width were also tested for ESD response at 12kV. All of the silver parts demonstrated electrical shorting, even prior to ESD pulsing. Multiple ESD pulses were not found to successfully "blow" these gaps into an electrically open state. One possibility, in looking again at Figure 34, is that the lower power of the laser used to machine the silver eliminated a necessary overcutting in removing the silver completely from the gap and at the interface between the bottom of the gap and the ceramic substrate. This may suggest a need for higher laser power or a greater number of laser pulses per location along the gap cut-line.

The test data for the copper and tungsten parts are displayed in Tables VII and VIII, again with corresponding detailed Tables shown in Appendix A.

In addition to the above-cited data, 39 of the 10 μm gap tungsten pieces and 35 of the 10 μm gap copper pieces were plasma-cleaned and then filled with unfilled polymer. Such a filler has been demonstrated as a successful medium through which to exhibit dielectric breakdown in response to an ESD over-voltage event. In order to successfully serve this purpose, this material must have the following characteristics.

- Be electrically insulating
- Have adequate carbon tracking resistance
- Be able to resist obliteration during the dielectric breakdown stage, and
- Fully recover its electrically insulating state after the over-voltage event is completed and the associated over-current discharged to ground.

Tables IX and X contain the data associated with these tests (again with corresponding detailed Tables shown in Appendix A).

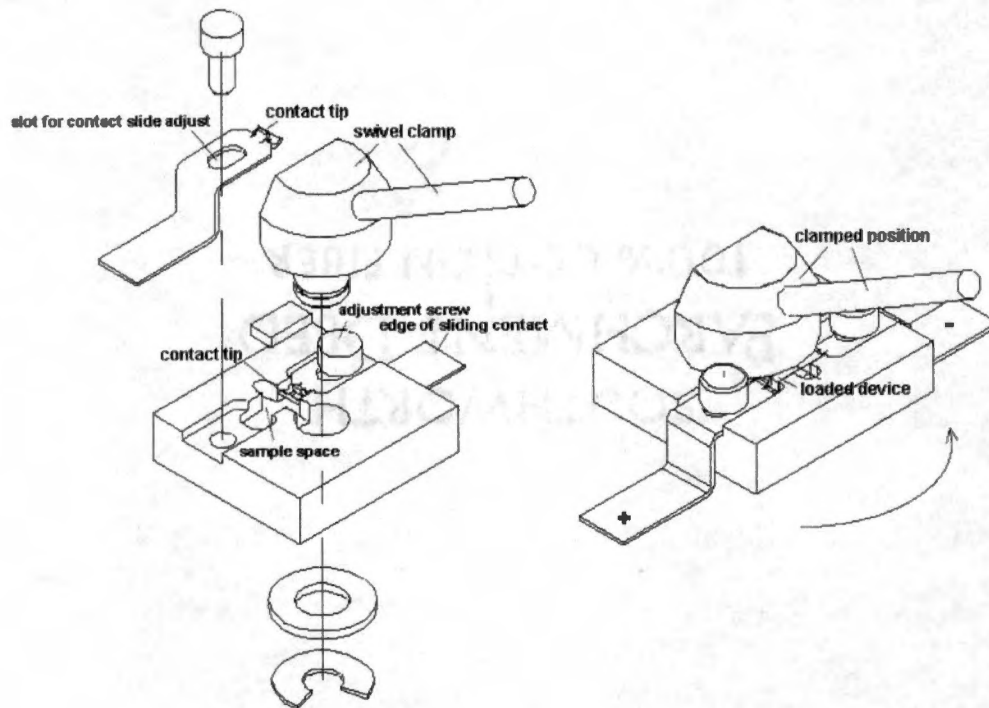


Fig. 36- Schematic of sample test holder.

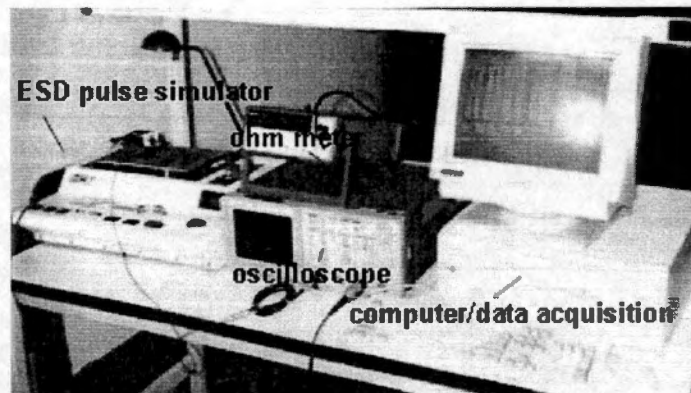


Fig. 37- ESD test set-up.

Table IV. Nominal 25 micron gap in silver thick film, air gap.

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
187.98	17.018	12.4703	1.341

Sample size: 10, # of ESD pulses/sample: 50

Table V. Nominal 25 micron gap in copper thick film, air gap

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
458.24	29.089	42.6488	1.553

Sample size: 10, # of ESD pulses/sample: 50

Table VI. Nominal 25 micron gap in tungsten thick film, air gap

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
651.79	37.545	56.9757	2.55

Sample size: 10, # of ESD pulses/sample: 50

Table VII. Nominal 10 micron gap in tungsten thick film, air gap

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
580.7	33.076	37.5177	2.122

Sample size: 10, # of ESD pulses/sample: 50

Table VIII. Nominal 10 micron gap in copper thick film, air gap

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
270.25	18.9612	20.0375	1.9075

Sample size: 10, # of ESD pulses/sample: 50

Table IX. Nominal 10 micron gap in tungsten thick film with UNFILLED POLYMER

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
455.939	29.7752	36.952	1.9878

Sample size: 39, # of ESD pulses/sample: 50

Table X. Nominal 10 micron gap in copper thick film with UNFILLED POLYMER

Vp mean, volts	Vc mean, volts	Vp sdev, volts	Vc sdev, volts
330.85	28.599	23.1674	2.3687

Sample size: 35, # of ESD pulses/sample: 50

- **Interpretation of ESD Data**

It is difficult to draw strong conclusions from the comparison of metallizations in ESD performance. First, the metallization heights, and therefore gap cross-sections are not identical from metal to metal. Secondly, the different metals and different gap width were cut under different conditions owing to different melting points. This, coupled with different IR interactions, has led to non-identical, and in some cases, distinctly different gap cross-sectional shapes. Table XI is a mixture of data from Table III and clamp and peak voltage values from Tables IV-VIII.

TableXI. Cut dimensions and V_p , V_c values.

metal	nominal gap width (μm)	metallization thickness (μm)	min (μm)	max (μm)	ave. (μm)	V_p	V_c
Ag	25	15.6-17.2	18	24	21	187.98	17.018
Cu	25	18.59	27.9	41.6	34.75	458.24	29.089
Cu	10	"	10.9	n. m.	N/A	270.25	20.038
W	25	13.07	22.2	39.4	30.8	651.79	37.545
W	10	"	13.6	n. m.	N/A	580.7	33.076

The following two primary observations can be made

1. Although exhibiting a slightly wider gap, the 25 micron Cu has starkly lower V_p and V_c values than the 25 micron gap in W.

2. Although exhibiting a substantially narrower gap, the 10 micron Cu has a starkly higher V_p value and a slightly higher V_c value than the 25 micron gap in silver.

The other gaps are not readily compared. The tape in the 10 micron W (Figure 31) is too severe to compare this gap to other ones. The 10 microns gap in Cu (Figure 25) is too irregular to compare. Finally, the 10 micron gaps in Ag were electrically shorted out.

The two cited points do, however, indicate greater abilities for Ag to switch over Cu and Cu to switch in comparison to W. This is possibly explained when considering the voltage vs. time portion of Figure 5. The voltage peak is merely the highest voltage value across the surge suppressor, provided that the device switches on. The actual switching is a more complex phenomenon than merely reaching this voltage value. The current vs. time curve illustrates that some current is in fact draining through the device prior to reaching maximum voltage across the suppressor.

It can therefore be conjectured that successful switching of the device is contingent upon the generation of sufficient current across the gap (in air or through the dielectric filler) so that a self-sustain arc is established until such time as the entire over-voltage event has been grounded. Accordingly, it can be

argued that the lower room temperature electrical resistivities of Ag over Cu (1.59 vs. 1.67 $\mu\Omega\text{-cm}$) and Cu or W (1.67 vs. 5.40 $\mu\Omega\text{-cm}$) allow for decreasing capability of establishing this current density, in that respective order. In addition, the lower melting point of Ag (961.9°C) may allow for its easy spark migration across the gap, which may help instigate efficient arcing of electrons. Further, and as a result, a greater electrical resistance is encountered in the electrons crossing the gap, which in turn increases the clamp voltage, as well.

- **Lightning Pulse Evaluation and Testing**

At this point, it was desired that a much higher power voltage transient be applied across the gaps. Devices were subjected to lightning simulation pulses. The test set-up is depicted in Figure 38. The test designation is IEC1004-5. This specifies an 8 μs rise-time pulse with a 20 μs duration. Testing was performed at 1100V peak and with 300W of peak pulse power. While some peak voltages are found to be greater than 1100V, this is accounted for by circuit impedance.

In order to improve the cross-section of the 25 μm Cu parts, more parts were laser cut to a nominal 25 μm gap width after adjusting the laser cutting parameters to those shown in Table XII. Microscopy shows a definite improvement in device cross-section in the sectioned regions.

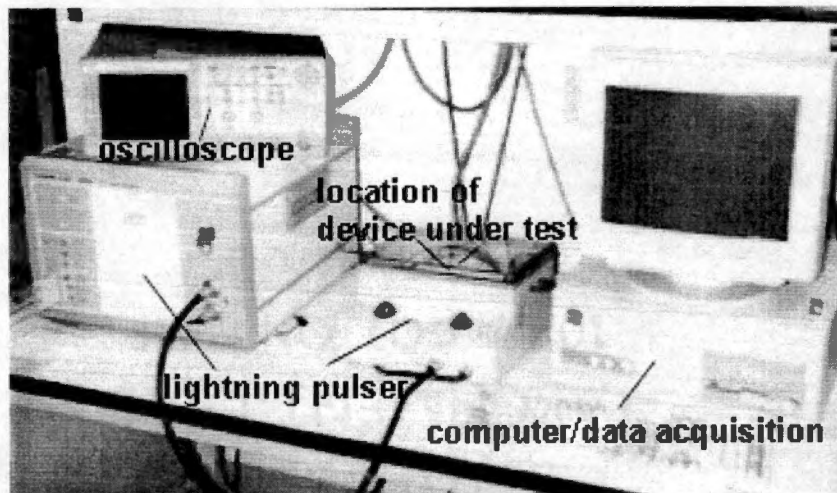


Fig. 38- Lightning pulse test set-up.

Table XII. New laser cutting parameters for nominal 25 μm cuts in Cu metallization.

wavelength	1064 nm
power	2W
amperage	18 A
pulse repetition rate of laser	2 kHz
travel rate of beam	2 mm/sec

Laser machining performed at Microlux Corp. (Santa Clara, CA).

The issues arising from the substantial increase in applied energy and corresponding peak power would be first order threats to the materials survivability under voltage suppression. Principally, the concerns were:

1. likelihood of obliteration of the polymer gap fill, and
2. susceptibility of the gap metals to melt and/or vaporize under triggered conditions.

In developing a workable device design, brief experiments were conducted in order to illustrate these issues. Figure 39 is a low magnification photomicrograph (100X) of a polymer-filled 25 μm wide gap in copper. Through the polymer, one can observe the gap. To the left of the gap, the line of demarcation, delineating the edge of the polymer filler coating, is indicated with a black trace. Figure 40 is a low magnification micrograph (100X) of the same sample after one IEC1004-5 pulse. Here, one can readily observe the loss in transparency of the polymer indicating its partial disintegration. Figure 41, is a micrograph (100X) of the same part after a second pulse. Here, the gap and the immediately surrounding region is exposed with the polymer in this vicinity obliterated.

As discussed earlier, the use of an open air gap, especially at these dimensions, raises strong issues of device reliability because the gap is now exposed to the elements (e. g., debris and moisture) that damage the gap

integrity including possibly leading to metallic migration across the gap. In the presence of moisture and a slight bias voltage, this is particularly the case with silver contacts. However, for the purposes of illustrating the relative susceptibility to melt-erosion, Figures 42-45 are for gaps with no polymer filler phase added.

In the case of an IEC1004-5 level pulse, the melting of contact metal becomes all the more likely. Figure 42 is a silver based gap part after one IEC1004-5 pulse. Here, appreciable melt erosion is apparent. Figure 43, illustrates the same behavior in a 25 μm wide gap Cu part after one pulse. In the case of both the silver and copper metallizations, only a small undercutting into the ceramic substrate remains at the near-gap dimensions. Figure 44 shows a 25 μm gap in tungsten prior to pulsing. Figure 45, illustrates the superior survivability of this tungsten-based device after an IEC1004-5 pulse. Here, only minor melting of a thin nickel layer (conventionally placed onto tungsten for solderability) is observed.

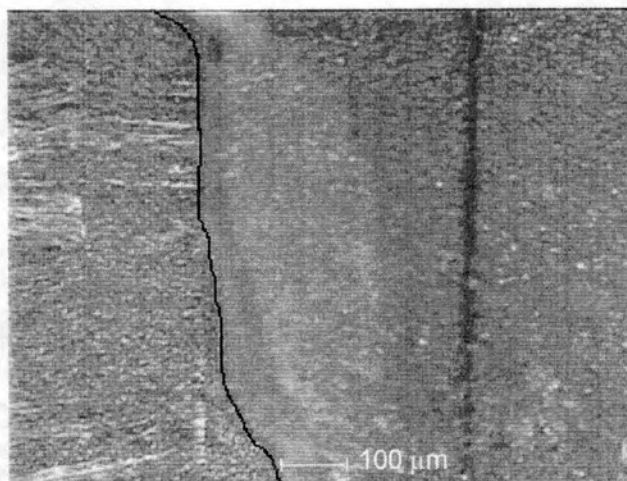


Fig. 39- Photomicrograph of Cu with 25 μm , laser cut gap filled with unfilled polymer, prior to lightning pulsing, demarcation of polymer is drawn in.

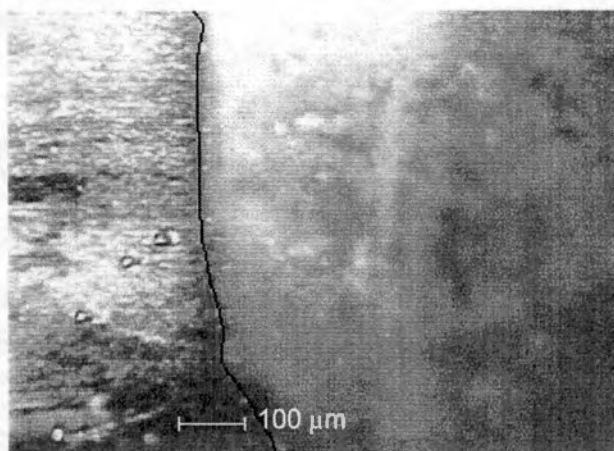


Fig. 40- Figure 39 after 1 lightning pulse.

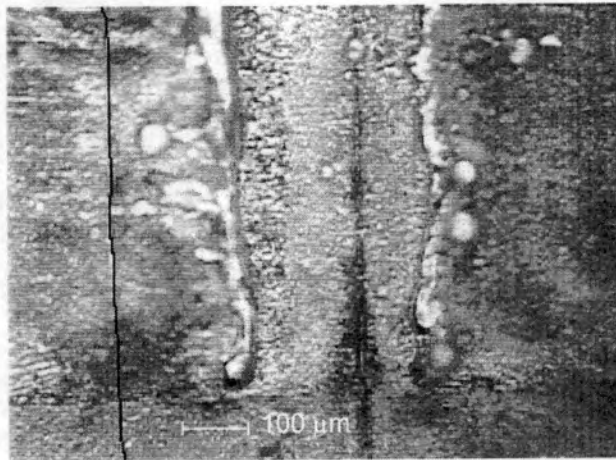


Fig. 41- Figure 39 after 2 lightning pulses.

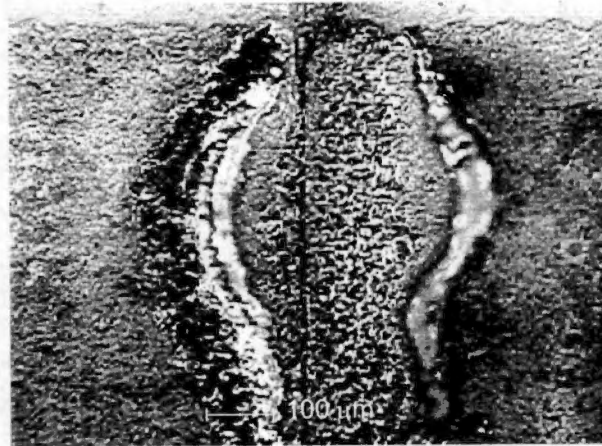


Fig. 42- Saw-cut gap in Ag at 25 μm initial width after pulsing one time.

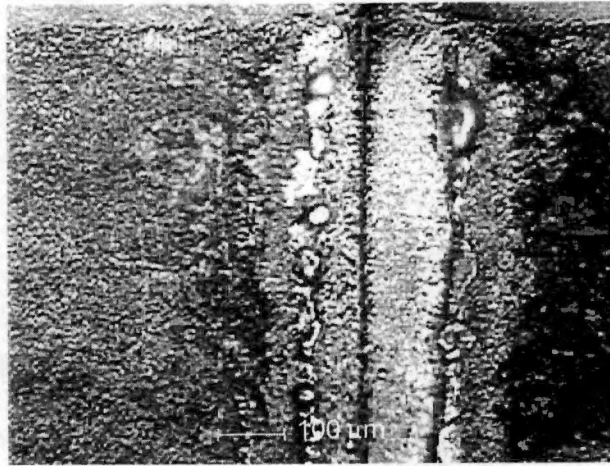


Fig. 43- Laser-cut gap in Cu at 25 μm initial width after pulsing one time.

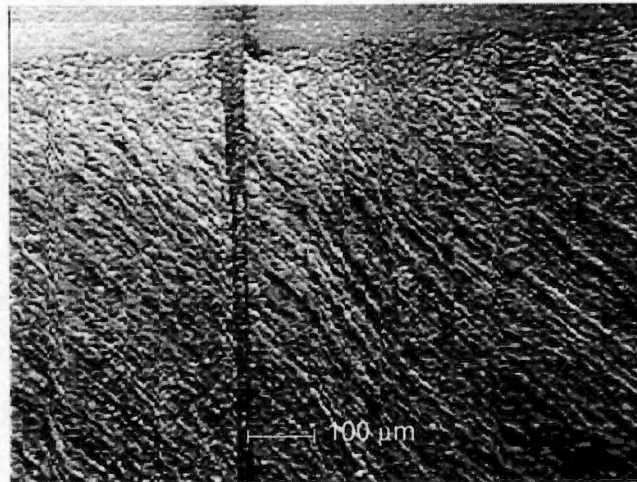


Fig. 44- Laser-cut gap in W at 25 μm initial width prior to pulsing.

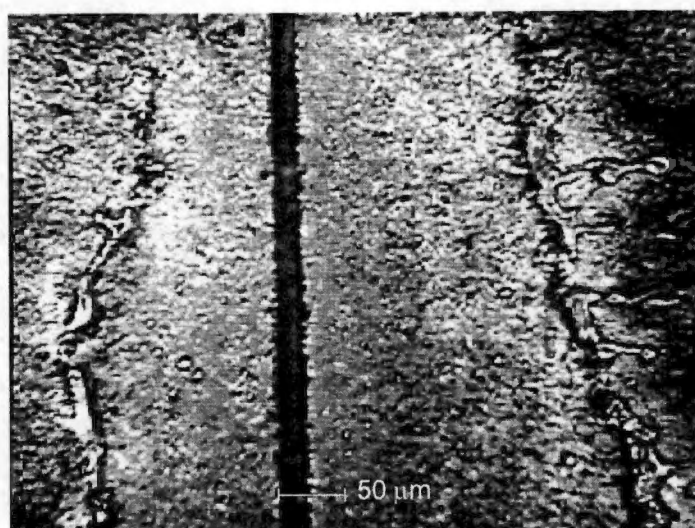


Fig. 45- Part shown in Fig. 44 after pulsing one time.

Brief testing of 1 piece each as an air gap arrestor was carried out. Table XIII shows the results as a function of pulse #.

Table XIII. Air gap testing of different metallization with nominal 25 μm . gap width.

Pulse #	25Ag air	V _{peak} , volts	V _{clamp} , volts	25Cu air	V _{peak} , volts	V _{clamp} , volts	25W air	V _{peak} , volts	V _{clamp} , volts
1		644	47.2		596	57.6		548	71.2
2		864	54		536	60.4		580	63.6
3		1256	57.2		628	45.6		408	58.4
4		nt			792	45.2		376	53.2
5		nt			880	47.6		388	58.4
6					940	47.2		712	57.6
7					1068	49.6		572	56.4
8					1104	47.6		836	55.2
	ave	921.33	52.80	ave	818.00	50.10	ave	552.50	59.25
	st dev	310.00	5.11	st dev	216.67	5.70	st dev	163.03	5.69

nt= no trigger

Figure 46 is a plot of V-peak vs. Pulse # for the above data for Cu and for W.

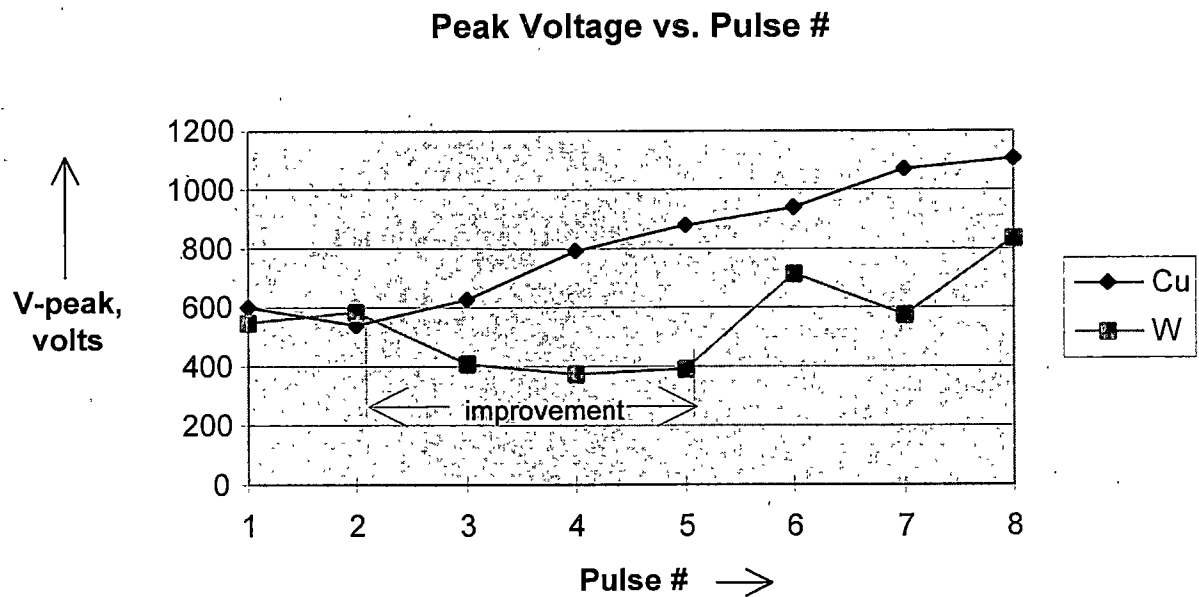


Fig. 46- V-peak vs. Pulse # for Table X data.

A nearly steady increase is seen in device degradation with Cu. W however, appears to initially go through an "improvement" step. This may be indicative of the spraying of controlled amounts of metal into the gap. Microscopy indicates that this should not occur with Cu, because the Cu melts immediately.

Although this data is by no means comprehensive, coupled with the associated microscopy, it gives a first order indication of the potential of contact metals for a higher power device.

We proceeded to focus on copper and tungsten for the remainder of the project. As the unfilled polymer was clearly inadequate for this type of device a commercial inorganic glass paste was chosen instead. This was a -325 mesh powder-based thick film paste of a leaded silicate composition with flow point of 520°C. Toward this end, ten pieces of each metallization at each gap width were hand painted over the gap region with the thick film ink. These parts were then fired at 560°C for 15 minutes.

Figure 47 is a secondary electron image (500X) of an unfilled, 25 μm gap in Cu showing a steeper and smoother cut through the copper than originally shown in the part depicted in Figure 24. Figure 48 is the same image at higher magnification (1,000X). The gap tapers up from 20 to 30 μm in width. This corresponds to an included taper angle of $\sim 28^\circ$.

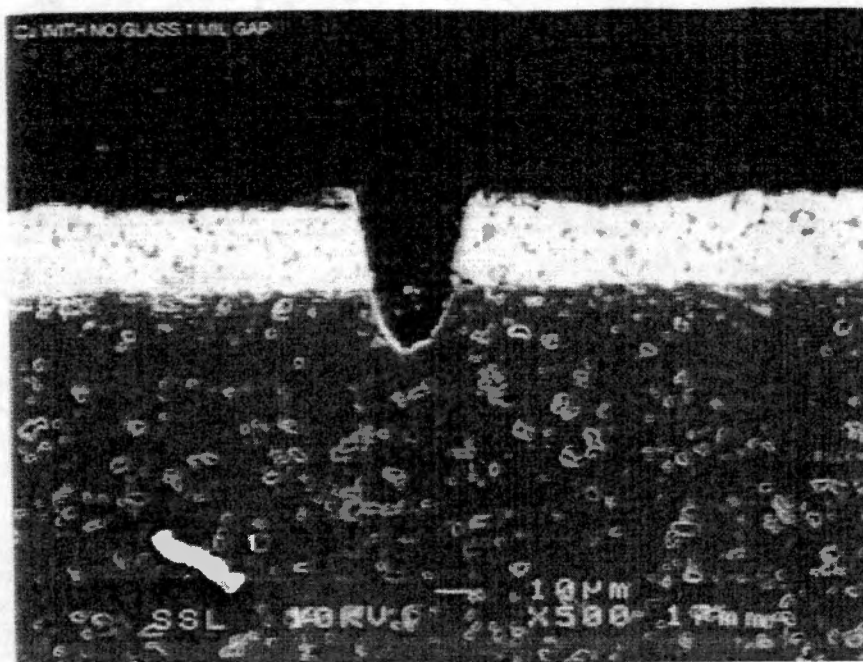


Fig. 47- Secondary electron image of a nominal 25 μm laser-cut gap in Cu prior to application of glass paste.

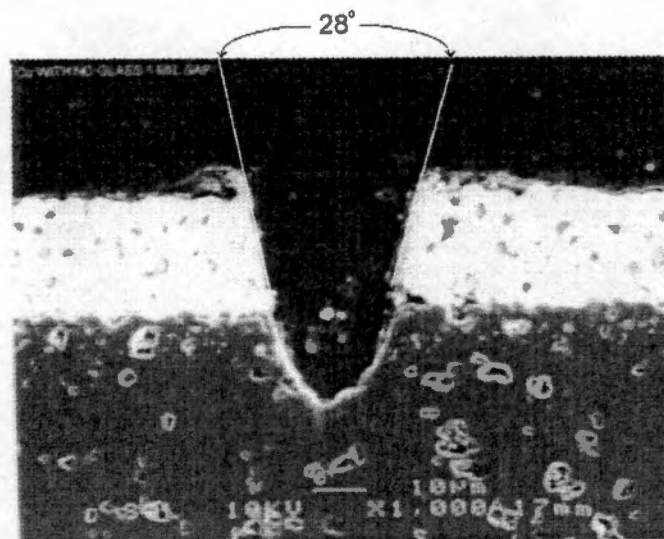


Fig. 48- Higher magnification view of Figure 47.

Figure 49 is a secondary electron image (100X) of a glass-filled 25 μm Cu part showing the mound of fired glass over and into the laser cut gap. Figure 50, is the same image at higher magnification (1,000X) showing complete infiltration and wetting.

It was decided that 5 pulses were adequate to demonstrate the device functionality and that devices failing to trigger on two successive pulses would be defined as "failed". Further testing would expose the test circuitry to excessive, un-suppressed, transient events.

Table XIV shows the data collected from 25 μm laser cut gaps in Cu and in W with a silicate glass filler. The term "no trigger" indicates that there was no successful switching on of the device.

The failure of these devices to trigger indicated that the added dielectric/thermionic emission barrier provided by the glass, made 25 μm of nominal gap width too wide to provide adequate voltage switching sensitivity.

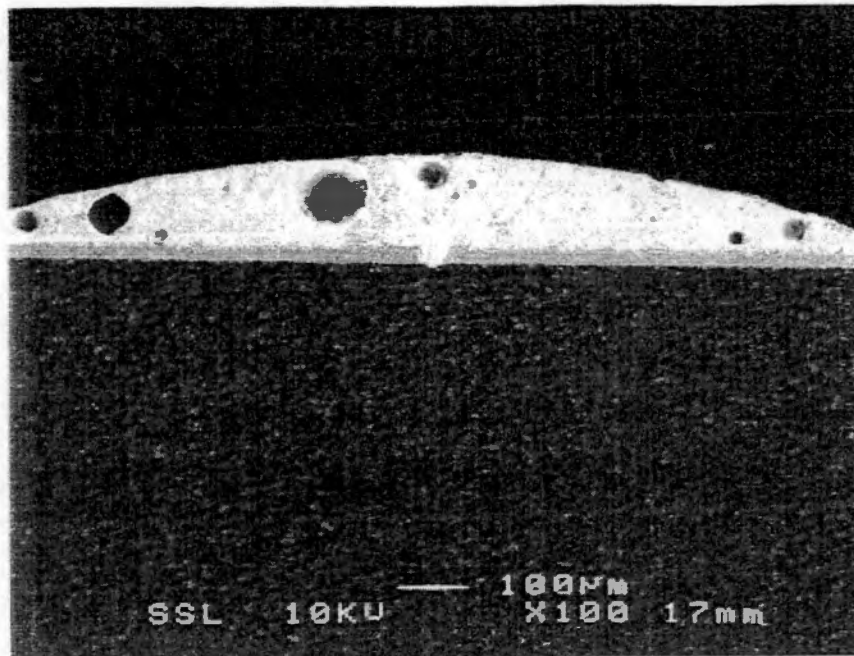


Fig. 49- Image of a gap in Cu with glass.

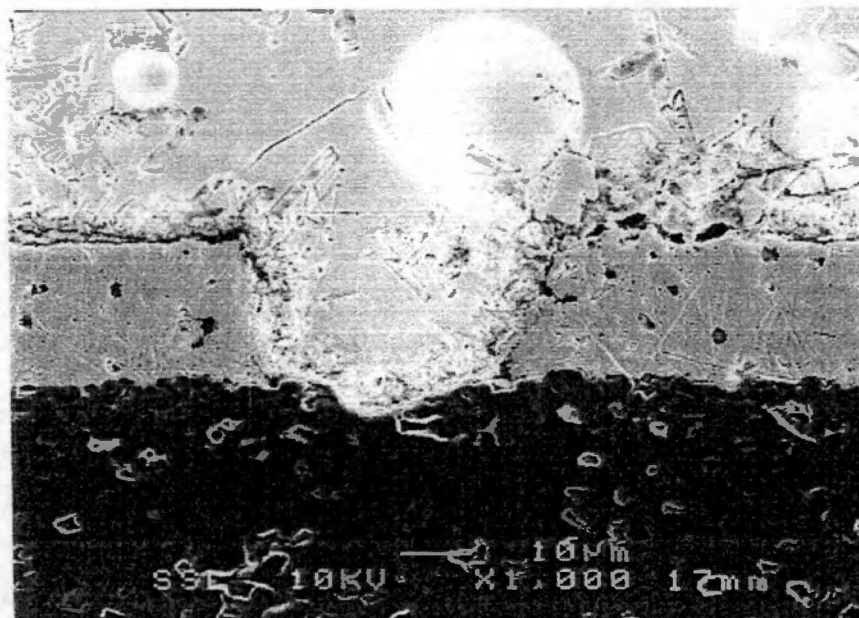


Fig. 50- Same part as Figure 49, at higher magnification.

Table XIV. Data for nominal 25 micron gaps in Cu and in W with glass filler.

25Cu #1	no trigger
	no trigger
25Cu #2	no trigger
	no trigger
25Cu #3	no trigger
	no trigger
25Cu #4	no trigger
	no trigger
25W #1	no trigger
	no trigger

Tables XV and XVI show the test data for 10 μm gaps in Cu and W filled with the silicate glass composition. Data points A, B, C and D are selected and referred to further on since they correspond to particularly illustrative switching events that are characteristic of

1. complete triggering,
2. reluctant triggering,
3. minimal triggering, and
4. non-triggering

of such a device (independent of the metallization used), respectively.

Table XV. Data for nominal 10 micron gap in Cu with glass filler.

Part	Pulse #	V _{peak} , volts	V _{clamp} , volts
10Cu #1	1	1168	74.8
	2	1220	63.2
	3	1216	65.2
	4	1216	65.6
		no trigger	
		no trigger	
ave		1205.00	67.20
st dev		24.74	5.17
10Cu #2	1	568	38.4
		no trigger	
		no trigger	
10Cu #3	1	174	43.4
	2	796	41.2
	3	1216	50.4
		no trigger	
		no trigger	
ave		728.67	45.00
st dev		524.25	4.80
10Cu #4	1	508	66
	2	756	54.4
	3	1064	52.4
		no trigger	
		no trigger	
ave		776.00	57.60
st dev		278.54	7.34
10Cu #5	1	534	42.8
	2	388	47.2
	3	720	50
	4	1108	43.2
	5	1212	44.8
ave		792.40	45.60
st dev		357.50	3.01
10Cu #6	1	674	41.8
		no trigger	
		no trigger	
10Cu #7	1	510	48
	2	384	48.4
	3	1148	54
		no trigger	
		no trigger	
ave		680.67	50.13
st dev		409.60	3.35
10Cu #8	1	1276	56.4
	2	1068	60.8
	3	704	62.8
	4	1072	60.8
	5	1140	59.6
ave		1052.00	60.08
st dev		211.94	2.36

Data Point C

Table XVI. Data for nominal 10 micron gap in W with glass filler.

Part	Pulse #	V _{peak} volts	V _{clamp} volts	
10W #1	1	746	63	
	2	716	60	
	3	664	59.2	
	4	924	58.4	
	5	956	56.8	
ave		801.20	59.48	
st. dev.		130.55	2.30	
10W #2	1	396	58.8	
	2	560	94.4	
	3	1252	60	
		no trigger		Data Point D
		no trigger		
ave		736.00	71.07	
st. dev.		454.33	20.22	
10W #3	1	740	64.4	Data Point A
	2	892	94.8	
	3	1256	83.2	
	4	1264	78	Data Point B
	5	1172	77.6	
ave		1064.80	79.60	
st. dev.		236.16	10.97	
10W #4	1	578	68.8	
	2	no trigger		
	3	no trigger		
10W #5	1	no trigger		
	2	no trigger		
	3	no trigger		
10W #6	1	760	64.4	
	2	1196	58.4	
	3	964	60.4	
	4	748	72.8	
	5	1288	58	
ave		991.20	62.80	
st. dev.		246.66	6.14	
10W #7	1	118	73.6	
	2	638	62.6	
	3	788	56	
	4	896	64	
	5	1004	59.6	
ave		688.80	63.16	
st. dev.		346.60	6.59	
10W #8	1	274	63.6	
	2	468	63	
	3	576	85.6	
	4	848	87.6	
	5	808	86	
ave		594.80	77.16	
st. dev.		239.22	12.68	
10W #9	1	630	56.8	
	2	1156	83.2	
	3	1212	63.2	
	4	no trigger		
	5	no trigger		
ave		999.33	67.73	
st. dev.		321.08	13.77	

Waveforms were recorded for select pulse events in order to better illustrate the switching or non-switching phenomena. First, Figure 51 shows a typical, successful trigger of the device. This corresponds to the data point marked "A" (Table XVI).

Figure 52 shows a pulse in which the device is becoming too resistive to switching and is beginning to lose the sharpness of its voltage peak. This corresponds to data point "B" (Table XVI).

Figure 53 illustrates this to a greater pronouncement. [Data point "C" Table XV.]

Finally, Figure 54 (data point "D" - Table XVI) illustrates a part, whose voltage peak is too high to trigger under the prescribed test conditions.

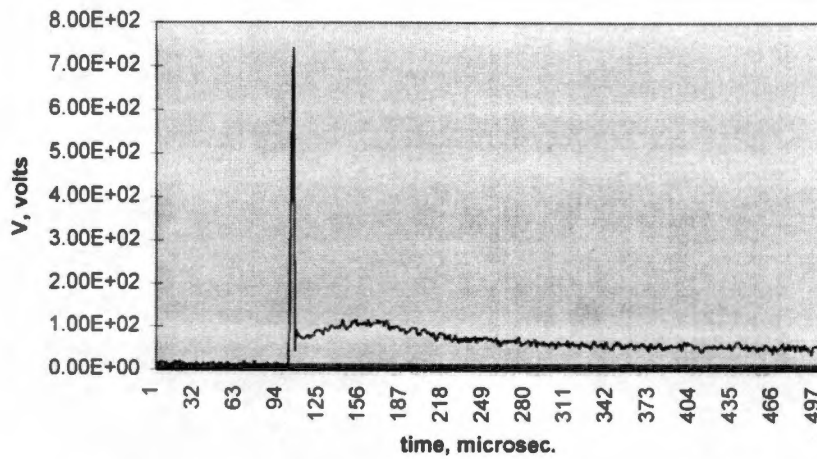


Fig. 51- Successful trigger waveform for data point A.

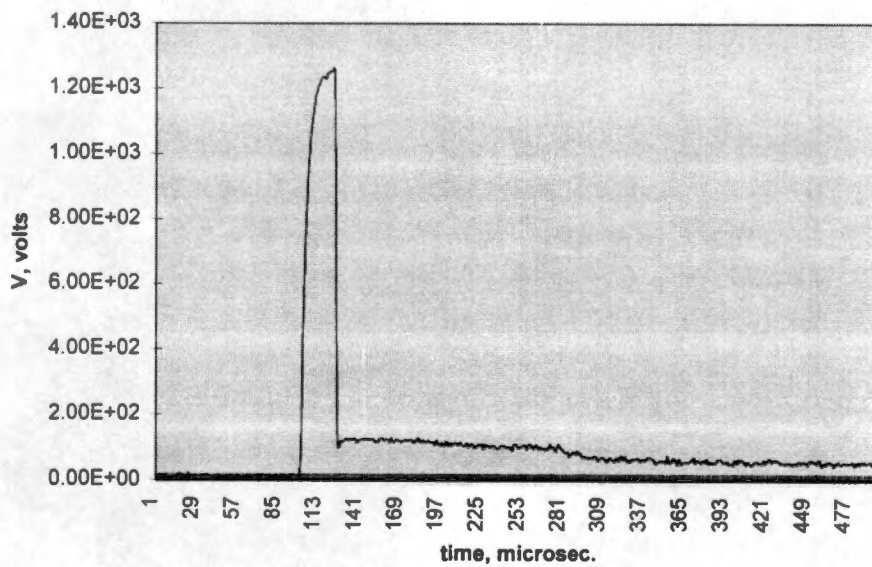


Fig. 52- Waveform exhibiting initial signs of marginal triggering for data point B.

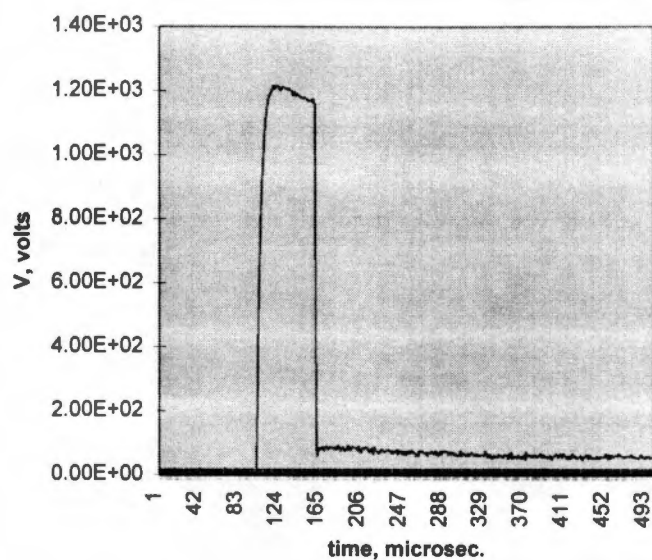


Fig. 53- Waveform exhibiting marginal triggering for data point C.

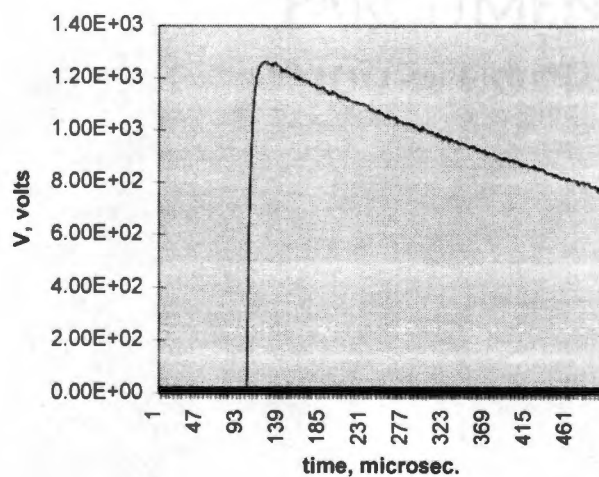


Fig. 54- Waveform exhibiting no triggering for data point D.

Here, there is no first order switching of the device and the voltage simply collapses through the pulse module's internal grounding.

Table XVII shows V-peak values for those Cu and W parts which survived 5 pulses. Out of 9 W parts tested, 5 survived 5 lightning pulses. Out of 8 Cu parts, by comparison, only 2 survived.

A clear, net increase in peak voltage is seen. However, some random events of device stability or even "improvement" are also indicated.

Table XVII. V-peak values for Cu and W parts triggering up to (5) lightning pulses.

Pulse #	10Cu-glass #5	10Cu-glass #8	10W-glass #1	10W-glass #3	10W-glass #6	10W-glass #7	10W-glass #8
1	534	1276	746	740	760	118	274
2	388	1068	716	892	1196	638	468
3	720	704	664	1256	964	788	576
4	1108	1072	924	1264	748	896	848
5	1212	1140	956	1172	1288	1004	808

Figure 55 is a plot of V-peak vs. Pulse # for this data.

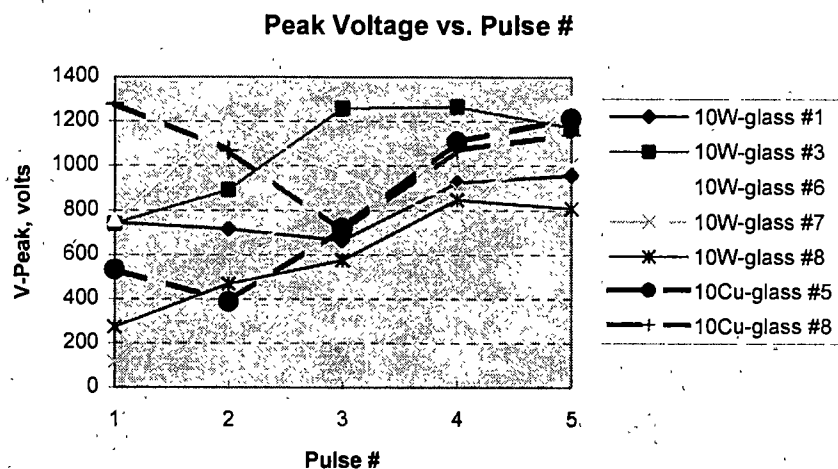


Fig. 55- V-peak vs. Pulse # for Table XIV data.

Section 5

Summary and Conclusions

Microgap surge suppressors were fabricated in Ag, Cu and W thick film metallizations on Al_2O_3 . Most of these gaps were micromachined using Nd:YAG lasers. These parts were tested as ESD suppressors both with no gap filler and with a select, organic polymer filler. Peak and clamp voltage values below 330V and 20V, respectively, were found using nominal 10 μm wide gaps in Cu metallization and an air gap. With unfilled polymer in the gap, these values became ~330V and 29V, respectively. Separately, these parts were evaluated as lightning arrestors with an inorganic glass filler.

While gap widths were attempted at 10 and 25 μm , there were variations in final gap cross-section, namely width and taper angle. The general data, however, indicates that Ag provides superior clamp and peak voltage values for ESD suppression when compared to Cu, even of narrower gap width. W clearly appears to generate higher peak voltage values, perhaps owing to its higher relative electrical resistivity leading to greater high frequency, transient impedance.

W was, however, the most robust material for lightning suppression. This result appears clearly due to its resistance to pulse-induced melting. Out of 9 W parts tested, 5 survived 5 lightning pulses. Out of 8 Cu parts, by comparison, only 2 survived. In addition, W appears to improve in performance on some parts, during the initial few pulses. Cu, by comparison rapidly increases in V-peak value until failure occurs

In the case of either Cu or W, no device triggering occurred in parts having a 25 μm , nominal gap width. Triggering was found to occur at 25 μm nominal gap width if the gap was unfilled or filled with the selected polymer.

The tendency for a part to experience lightning pulse induced failure was illustrated by V vs. time waveforms where spreading of the voltage peak can be clearly seen.

The primary conclusions of this research are that in order to alter the suppression device from operating in response to an ESD pulse to a lightning pulse, higher melting point metallization was required as was a dielectric filler which was inorganic as opposed to polymeric. W performed particularly well as electrode metallization, exhibiting substantially greater resistance to spark-induced erosion than either Ag or Cu.

Section 6

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Figure Credits:

All figures were generated for this thesis except for the following:

Figures 7 and 8 are from Ref. (15).

Section 7

APPENDIX A

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TABLE		PAGE
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VII-B.	Nominal 10 micron gap in tungsten thick film, air gap	A2
VIII-B.	Nominal 10 micron gap in copper thick film, air gap	A3
IX-B.	Nominal 10 micron gap in tungsten thick film with UNFILLED POLYMER	A4
X-B.	Nominal 10 micron gap in copper thick film with UNFILLED POLYMER	A5

Table IV-B. Nominal 25 micron gap in silver thick film, air gap.

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
silg-1	1/19/98	194.4	16.02	9665	35.7	0.88	1340	50	1
silg-2	1/19/98	200.3	17.27	9855	36.7	2.08	0	50	0
silg-3	1/19/98	186.2	16.98	9839	33.9	1.49	4	50	0
silg-4	1/19/98	180.7	14.94	9855	38.1	0.84	6	50	0
silg-5	1/19/98	204.6	18.77	9683	31.1	2.02	1184	50	1
silg-6	1/19/98	187.7	17.74	9854	29.3	1.05	0	50	0
silg-7	1/19/98	194.4	16.82	9708	36	1.22	613	50	1
silg-8	1/19/98	188.6	18.5	9844	29.6	1.91	11	50	0
silg-9	1/19/98	169	15.73	9855	29.3	0.98	6	50	0
silg-10	1/19/98	203.4	17.97	9807	29.7	1.04	113	50	0
Average		190.93	17.074		12.8109	1.351			
Average after filter		187.98	17.018		12.4703	1.341			

Table V-B. Nominal 25 micron gap in copper thick film, air gap

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
cug-1	1/19/98	424.5	31.08	9858	52	1.34	0	50	0
cug-2	1/19/98	426.6	27.67	9858	58.4	1.66	0	50	0
cug-3	1/19/98	462.1	28.29	9838	103.6	1.26	15	50	0
cug-4	1/19/98	592.2	29.62	9858	115.1	1.88	1	50	0
cug-5	1/19/98	418.6	29.6	9851	61.6	1.41	3	50	0
cug-6	1/19/98	440.2	30.53	9859	62.4	1.4	0	50	0
cug-7	1/19/98	463.4	29.76	9856	54.6	1.31	6	50	0
cug-8	1/19/98	465.8	27.73	9858	50.3	1.82	0	50	0
cug-9	1/19/98	465.2	28.54	9859	86.3	1.64	2	50	0
cug-10	1/19/98	423.8	28.07	9842	61.4	1.81	9	50	0
Average		458.24	29.089		42.6488	1.553			
Average after filter		458.24	29.089		42.6488	1.553			

Table VI-B. Nominal 25 micron gap in tungsten thick film, air gap

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
25wg-1	1/20/98	439.8	28.6	9846	55.6	2.83	18	50	0
25wg-2	1/20/98	492.5	27.71	9849	71.9	2.12	15	50	0
25wg-3	1/20/98	1076	58.42	9858	128	3.81	0	50	0
25wg-4	1/20/98	503.4	33.7	9851	59.6	2.08	7	50	0
25wg-5	1/20/98	492.2	34.24	9854	62.9	4.13	0	50	0
25wg-6	1/20/98	495.8	28.56	9848	43	1.2	4	50	0
25wg-7	1/20/98	517.8	32.81	9852	60.5	4.2	2	50	0
25wg-8	1/20/98	474.8	34.12	9849	51.5	1.64	1	50	0
25wg-8	1/20/98	519.8	32.1	9838	54.7	1.9	7	50	0
25wg-9	1/20/98	1399	59.46	9857	226	3.03	4	50	0
25wg-10	1/20/98	546.6	34.33	9851	73.9	1.39	0	50	0
Average		651.79	37.545		56.9757	2.55			
Average after filter		651.79	37.545		56.9757	2.55			

Table VII-B. Nominal 10 micron gap in tungsten thick film, air gap

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
10wg-1	1/20/98	131.3	19.33	5405	12.7306	1.77	4162	50	26
10wg-2	1/20/98	316.7	21.25	9855	30.2018	1.7	2	50	0
10wg-3	1/20/98	823	45.38	9858	46.8740	2.84	5	50	0
10wg-4	1/20/98	366.2	24.69	9855	27.4320	1.4	0	50	0
10wg-5	1/20/98	179.6	19.36	9648	21.3064	1.55	1007	50	2
10wg-6	1/20/98	153.4	19.83	8293	18.2169	1.37	3092	50	10
10wg-7	1/20/98	37.5	-1.412	0.123	9.0019	1.335	0	17	18
10wg-8	1/20/98	14	-2.033	0.123	10.1738	0.446	0	6	7
10wg-9	1/20/98	991	45.5	9857	24.5023	2.64	3	50	0
10wg-10	1/20/98	406.6	28.56	9852	22.5315	2.03	6	50	0
Average		341.93	22.0455		22.2971	1.7081			
Average after filter		580.7	33.076		37.5177	2.122			

Table VIII-B. Nominal 10 micron gap in copper thick film, air gap

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
10cug-1	1/20/98	26.4	-4.17	0.122	6.4675	0.2	0	20	20
10cug-2	1/20/98	197.3	15.06	9857	19.9983	0.77	5	20	0
10cug-3	1/20/98	293.2	19.42	9859	20.3387	2.65	0	20	0
10cug-4	1/20/98	262.9	22.32	9860	16.7220	3.45	1	20	0
10cug-5	1/20/98	342	25.32	9859	22.7641	1.9	0	20	0
10cug-6	1/20/98	333.6	22.64	9859	23.1896	2.15	5	20	0
10cug-7	1/20/98	291.4	17.84	9856	17.3603	1.16	2	50	0
10cug-8	1/20/98	33.5	-3.624	0.122	6.4675	0.162	0	50	50
10cug-9	1/20/98	287.6	18.12	9858	16.4667	0.94	7	50	0
10cug-10	1/20/98	154	19.58	9859	14.8498	2.24	2	50	0
Average		222.19	15.2506		16.4625	1.5622			
Average after filter		270.25	18.9612		20.0375	1.9075			

**Table IX-B. Nominal 10 micron gap in tungsten thick film with UNFILLED
POLYMER**

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
wire-19	1/19/98	5.7	-5.24	0.123	9.2185	0.497	0	20	20
10w-1	1/19/98	230.2	18.76	9755	29.2004	1.08	589	50	1
10w-2	1/19/98	929	43.49	9864	28.3249	2.45	0	50	0
10w-3	1/19/98	227.1	19.04	9863	26.6769	1.2	0	50	0
10w-4	1/19/98	238.8	18.75	9860	21.3210	1.63	5	50	0
10w-5	1/19/98	2.3	-3.272	0.123	7.1585	0.57	0	50	50
10w-6	1/19/98	287.2	17.85	9861	18.2310	0.66	0	50	0
10w-7	1/19/98	210.7	19.35	9862	25.3895	1.16	3	50	0
10w-8	1/19/98	249.8	19.06	9862	25.5440	1.65	1	50	0
10w-9	1/19/98	626.6	41.36	9863	78.1768	3.33	3	50	0
10w-10	1/19/98	966	45.62	9863	64.3749	2.23	6	50	0
10w-11	1/19/98	249.3	19.53	9862	17.5100	1.74	4	50	0
10w-12	1/19/98	563.8	40.53	9862	86.4168	3.06	0	50	0
10w-13	1/19/98	230.2	18.44	9862	28.6854	1.21	5	50	0
10w-14	1/19/98	241.2	19.57	9861	25.9044	1.08	0	50	0
10w-15	1/19/98	215.2	18.57	9649	25.7500	1.72	531	50	1
10w-16	1/19/98	13.5	-2.988	0.123	8.9610	0.529	0	50	50
10w-17	1/19/98	16.6	-2.984	0.123	10.0425	0.554	0	50	50
10w-18	1/19/98	1014	46.62	9862	68.494	2.45	4	50	0
10w-19	1/19/98	233	12.68	9862	23.226	1.29	0	50	0
10w-20	1/19/98	313.2	17.87	9861	19.158	0.69	0	50	0
10w-21	1/19/98	247.4	20.98	9855	24.308	2.97	25	50	0
10w-22	1/19/98	198.1	20.88	9295	18.385	4.24	1717	50	5
10w-23	1/19/98	198	21.53	8449	19.518	3.83	2800	50	10
10w-24	1/19/98	265.6	20.46	9754	23.844	1.71	489	50	1
10w-25	1/19/98	593.7	48.46	9862	39.242	1.71	4	50	0
10w-26	1/19/98	148.2	25.18	6990	19.518	4.29	3463	50	23
10w-27	1/19/98	577.4	46.82	9862	53.044	3.12	2	50	0
10w-28	1/19/98	341.4	23.61	9860	19.930	1.17	5	50	0
10w-29	1/19/98	292.4	20.44	9861	22.660	1.67	3	50	0
10w-30	1/19/98	18.1	-2.808	0.123	10.248	0.444	0	50	50
10w-31	1/19/98	22.4	-2.016	0.123	8.961	0.534	0.0001	50	50
10w-32	1/19/98	290.2	24.01	8874	23.896	2.68	2551	50	8
10w-33	1/19/98	224.8	23.05	8063	28.015	4.54	2777	50	17
10w-34	1/19/98	709	49.23	9862	49.954	5.58	5	23	0
10w-35	1/19/98	378.4	26.72	9862	17.922	1.11	2	50	0
10w-36	1/19/98	192.9	22.13	8624	25.338	2	2942	50	7
10w-37	1/19/98	15.6	-2.828	0.123	14.883	0.592	0.0001	50	50
10w-38	1/19/98	198.2	22.18	9167	20.600	4.13	1864	50	5
10w-39	1/19/98	767	48.81	9861	65.404	2.56	6	50	0
Average		318.555	21.9861		28.836	1.9915			
Average after filter		455.939	29.7752		36.952	1.9878			

Table X-B. Nominal 10 micron gap in copper thick film with UNFILLED POLYMER

Test Ref	Date	Vp mean, volts	Vc mean, volts	K Ω mean	Vp sdev, volts	Vc sdev, volts	K Ω sdev	Pulses	Total Shorts
10c-1	1/19/98	294.2	22.43	9861	21.1314	1.15	18	50	0
10c-2	1/19/98	411	40.43	9862	39.6470	4.08	0	50	0
10c-3	1/19/98	324.6	28.86	9862	20.4646	1.65	0	50	0
10c-4	1/19/98	244.5	25.38	9862	24.6191	6.32	4	50	0
10c-5	1/19/98	298.7	27.98	9862	23.6958	1.19	0	50	0
10c-6	1/19/98	214.5	26.35	9861	23.5420	4.89	0	50	0
10c-7	1/19/98	301.5	20.48	9861	23.9010	0.77	0	50	0
10c-8	1/19/98	286.7	20.7	9861	20.3620	1.11	1	50	0
10c-9	1/19/98	343.5	25.92	9861	23.4907	1.35	0	50	0
10c-10	1/19/98	296.2	21.95	9861	21.6955	1.32	3	50	0
10c-11	1/19/98	306.1	24.86	9861	22.1059	1.28	0	50	0
10c-12	1/19/98	328.9	24.88	9861	19.1823	1.31	0	50	0
10c-13	1/19/98	277.1	24.2	9859	21.9520	2.14	23	50	0
10c-14	1/19/98	153	25.28	9862	20.2594	3.13	4	50	0
10c-15	1/19/98	299.4	21.72	9861	24.4139	0.71	5	50	0
10c-16	1/19/98	297.3	24.96	9862	21.2339	2.26	26	50	0
10c-17	1/19/98	271.8	22.02	9862	21.2339	1.23	4	50	0
10c-18	1/19/98	1188	96.83	9860	28.7222	3.76	0	50	0
10c-19	1/19/98	281	27.31	9860	21.2339	5.42	0	50	0
10c-20	1/19/98	311.7	22.62	9860	22.4649	1	0	50	0
10c-21	1/19/98	432.6	35.64	9860	21.7468	3.01	0	50	0
10c-22	1/19/98	445.8	35.45	9860	15.8998	1.93	0	50	0
10c-23	1/19/98	504.4	48.57	9861	35.9028	1.89	8	50	0
10c-24	1/19/98	296.3	25.53	9860	23.4907	1.94	21	50	0
10c-25	1/19/98	231.4	24.51	9860	25.8500	2.45	0	50	0
10c-26	1/19/98	303.2	25.13	9864	22.6188	2.41	26	50	0
10c-27	1/19/98	329.3	28.91	9860	23.4907	1.48	1	50	0
10c-28	1/19/98	304.6	24.8	9860	20.9262	1.83	3	50	0
10c-29	1/19/98	296.6	25.18	9860	22.5162	5.52	0	50	0
10c-30	1/19/98	326.4	22.26	9860	25.7987	1.02	0	50	0
10c-31	1/19/98	290.6	24.04	9860	20.3620	2.73	0	50	0
10c-32	1/19/98	146	24.35	9861	18.7207	4.09	6	50	0
10c-33	1/19/98	281.2	24.26	9860	21.8494	1.8	4	50	0
10c-34	1/19/98	127.5	23.8	9663	15.1304	3.9	1394	50	1
10c-35	1/19/98	7.8	-3.106	0.122	10.2579	0.525	0.0001	17	17
Average		315.88	27.401		22.7430	2.3496			
Average after filter		330.85	28.599		23.1674	2.3687			

VITA

James Intrater was born in New York City in 1964. He attended public school and, eventually, Rutgers University College of Engineering (Piscataway, NJ) where he received a B. S. in Ceramic Engineering in 1986. Since that time he has been a senior engineer at Advanced Technology, Inc. in Palisades Park, NJ, later promoted to Director of Technology as the company moved to Fremont, CA and changed its name to Oryx Technology Corp. In August, 1996, he registered with the Distant Education program of The University of Tennessee Space Institute in Tullahoma, TN. He has since been working toward a Masters of Science Degree in Metallurgical Engineering.