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I am submitting herewith a thesis written by Karthikeyan Ramamurthi entitled "IMPACT OF PACKAGING TECHNOLOGY ON SYSTEM PARTITIONING." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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**IMPACT OF PACKAGING TECHNOLOGY ON
SYSTEM PARTITIONING**

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Master of Science

Degree

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Karthikeyan Ramamurthi

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ABSTRACT

This thesis emphasizes concurrent consideration of the partitioning of a microelectronic circuit design into multiple dies and the selection of the appropriate packaging technology for implementation of the entire system. Partitioning a large design into a multichip package is a non-trivial task. Similarly, selection of the MCM packaging technology to accommodate a multichip solution can also be puzzling. The interdependencies of these two problems afford the opportunity to achieve a global optimum when considered concurrently. In this work the author addresses the partitioning/MCM technology tradeoff, their interdependency, and previous work in this area [1]. The SUN MicroSparc CPU is used as a demonstration vehicle and is partitioned for different MCM technologies. The preliminary results show that the optimum number of partitions and contents of each partition depend heavily on the choice of MCM technologies for a given application.

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CHAPTER 1

INTRODUCTION

1.1 Microelectronic Systems Overview

Microelectronic systems generally consist of several VLSI chips mounted on to a printed circuit board (PCB). The VLSI chips are conventionally bare dies packaged into plastic or ceramic single chip packages (SCP) as shown in Fig 1.1. There is an enormous inefficiency in size and performance with the traditional SCP-on-PCB approach. The silicon efficiency (which is defined as the ratio of total area occupied by silicon to the total board area) is typically 5% for typical PCBs with several chips [2]. Figure 1.2 shows a PCB with 10 SCPs mounted on it and the area reduction of the board if the SCPs are eliminated and dies directly mounted onto the board [3]. This concept is the essence of the Multichip Module (MCM) i.e. to eliminate the single-chip package and attach several bare dies directly onto one package. The elimination of the SCP results in smaller feature size and thus results in the preferred increase in packaging density, performance and reliability and decrease in system size, weight and power consumption.

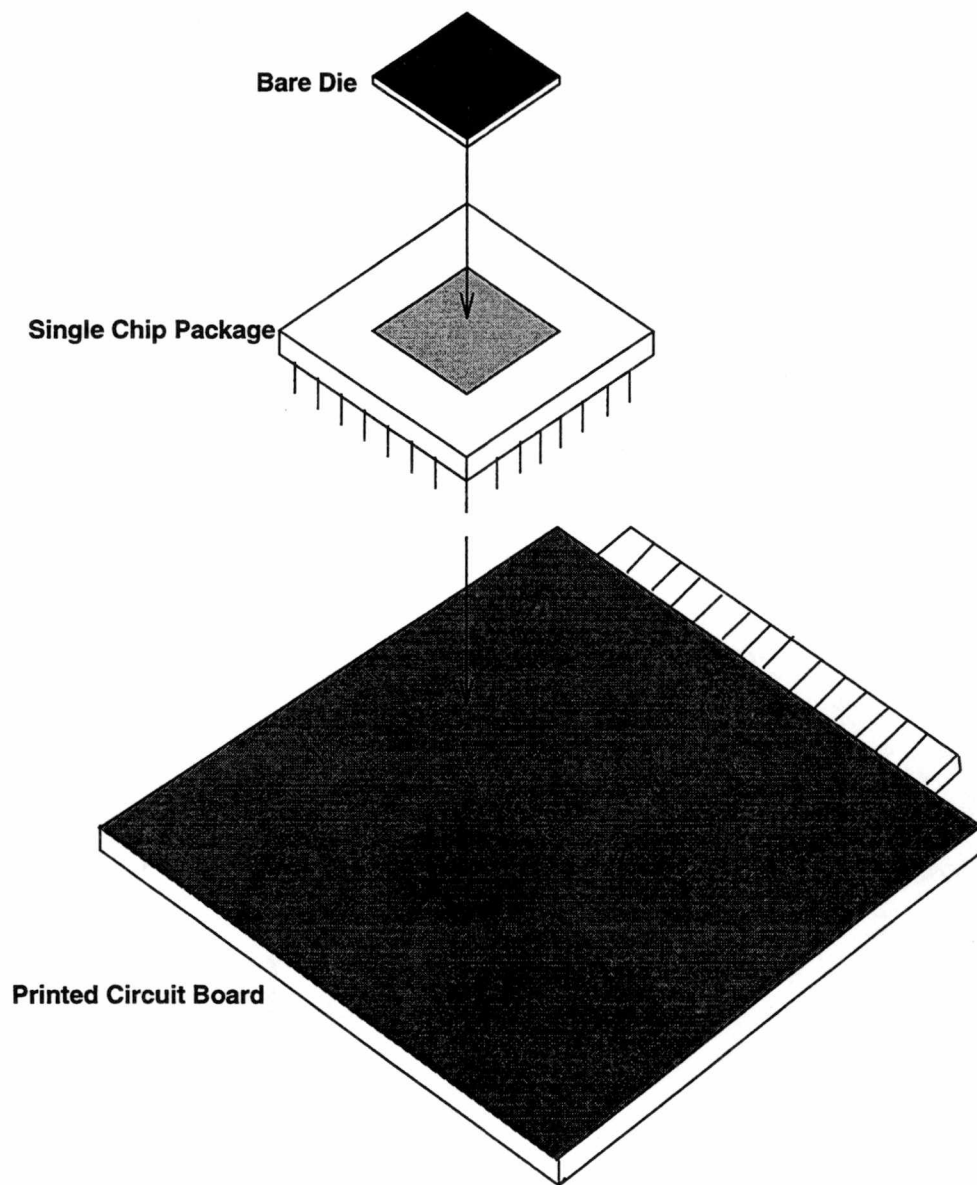
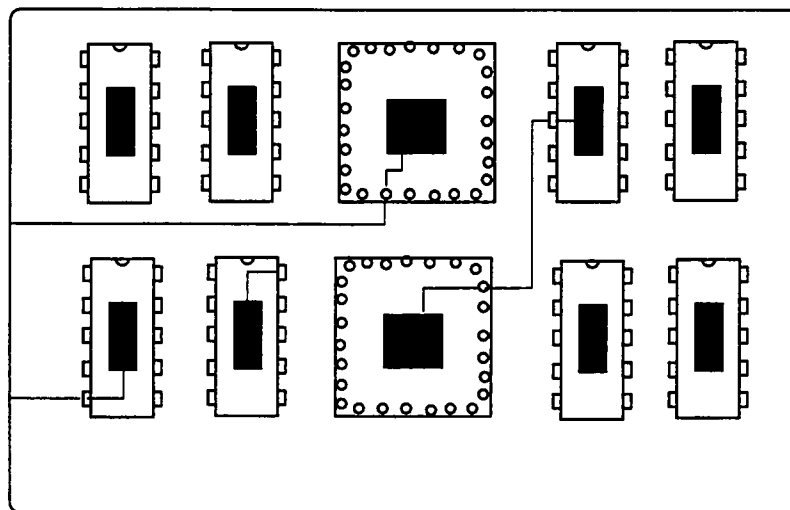
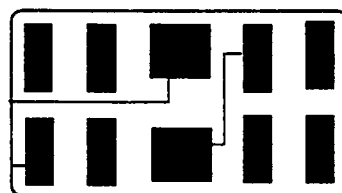


Figure 1.1: *Conventional Packaging Technology (after [2]).*



(a) PCB Implementation



(b) MCM Implementation

Figure 1.2: *Area Savings due to MCM Implementation*

1.2 Motivation

The recent advances in VLSI fabrication techniques allow IC designers to realize a few millions of transistors on a single chip. For example, in microprocessor-based systems, it is necessary for the Central Processing Unit (CPU) and cache memory to be close together to minimize the access time. To achieve this, the designer may decide to place the primary level (L1) cache directly on the CPU chip. The present day CPU chips for workstation applications are already large designs and adding the cache to the CPU increases the design size further. Packaging the entire CPU on a single wafer avoids the performance degradation caused by the secondary interconnect like the PCB. However, due to exorbitant costs and unacceptable yields, wafer scale integration continues to be a technology for the future [4]. The system cost can be improved to a large extent without loss of performance if the large CPU designs are partitioned as several smaller chips and fabricated on a multichip module. Physical partitioning is an extremely important task in reducing the system cost in the design of microelectronic systems.

Figure 1.3 shows the flow diagram of the steps involved in the design of a microelectronic system. The flow diagram on the lefthand side depicts the traditional system design. The designer starts with an architecture of the design which will meet the system requirements. Then the design is partitioned into manageable parts which can be realized as individual chips. The physical design of the ICs follows this step. Finally the designer makes the packaging choice of mounting the SCPs on the PCB. In this design process the system designer

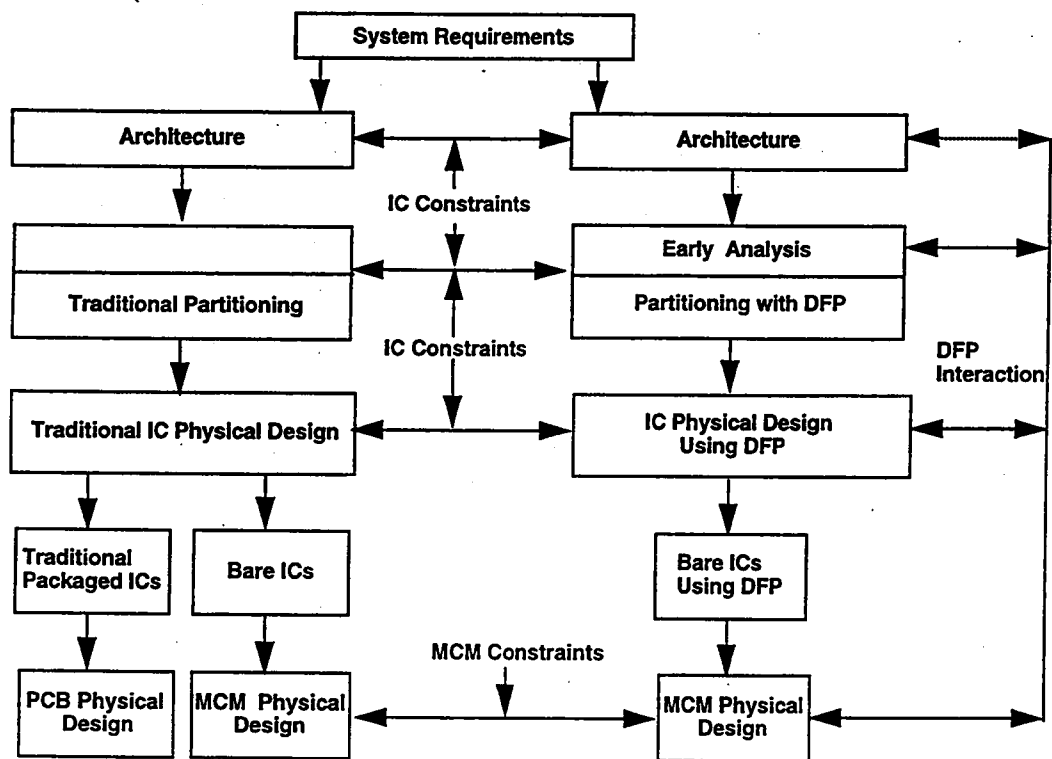


Figure 1.3: *Microelectronic System Design Flow*

considers the packaging issues only at the end of the design cycle. During the IC physical design the designer assumes that the dies will be wire bonded and be mounted on a PCB substrate. These assumptions offer the designer a lower I/O count in the order of a few hundred and a low interconnect density. The result is a sub-optimal system design. The recent revolution in packaging technology offers the system designer advanced packaging features like flip-chip bonding which allows very high I/O count of the order of several hundred. The new interconnect technologies offer very high interconnect densities. In order to take full advantage of the new packaging technologies, the critical packaging issues should be considered early in the design cycle i.e. during the major design steps like Partitioning and IC Physical design. This approach is termed as Design For Packageability (DFP) [5] and the righthand side of the flow diagram in Figure 1.3 shows this approach being applied to microelectronic system design.

The major design costs are committed when the decisions are made in the initial stages of the design cycle [6]. Since packaging should be considered early in the design cycle to realize high performance systems, there is a need to perform an early package analysis.

1.3 Statement of Problem and Approach

This thesis emphasizes concurrent consideration of the partitioning of microelectronic circuit design into multiple dies and the selection of the appropriate packaging technology for implementation of the entire system. Partitioning a

large design into a multiple chips is a non-trivial task. Added to this is the difficult task of selecting an appropriate MCM packaging technology . The inter-dependencies of these two problems afford the opportunity to achieve a optimum solution when considered concurrently.

The impact of bonding technologies such as area array (Flip-Chip, FC) and peripheral (Wire-Bond, WB) on the die size and layout of VLSI dies is discussed in [7] which was focused on the the physical die layout level rather than the system level. A more conceptual trade-off analysis between peripheral and area array bonding in MCMs is presented in [8]. The design is described in terms of gate counts used Rent's rule to establish the number of I/Os for a given circuit size. The above work considered the homogeneous system where all the dies are considered to be of the same size and I/O count. This thesis work tries to establish the interaction of the various packaging alternatives, partitioning and the system performance when more information like the interconnect information between the functional blocks is available. The system is considered to be non-homogeneous where the dies may vary in size and I/O count. The intent of this work is not to promote a new partitioning scheme since numerous techniques have already been described [9], [10]. Our approach is to develop a framework in which various packaging/partitioning choices can be explored and evaluated concurrently. Since performing a detailed evaluation at the system level for various packaging/partitions can turn into a time-consuming task, we have employed an estimation-based, early-analysis technique.

1.4 Goals and Expected Contributions

One of the goals of this work is to use the SUN MicroSparc CPU as a demonstration vehicle and partition this design into multiple chips. The goal also includes the determination of the optimum number of partitions and the best choice of MCM packaging technology. One of the major contributions of this work will be the development of a early analysis tool which will empower the system designer to make critical packaging and partitioning decisions early in the design process. The work will also establish the nature and extent of interaction between the partitioning and packaging in microelectronic system design.

1.5 Chapter Outline

This thesis is comprised of six chapters with Chapter I the introduction. Chapter II describes the multichip packaging options available to the system designer as well as the bonding and interconnect technologies. The impact of the multichip packaging technology on the system performance parameters is also discussed. Chapter III discusses the concept of partitioning as applied to microelectronic system design. The models used for the partitioning problem, the currently available partitioning algorithms and the algorithm used in this work are described in this chapter. This chapter also briefly discusses the different levels of design representation, the need for an early analysis and the interaction of packaging on partitioning. The Design for Packageability methodology is described in detail

in Chapter IV. The models used in the estimation of several performance factors are discussed in that chapter. Chapter V discusses the case study undertaken to substantiate the methodology proposed in this work. Chapter VI summarizes this thesis work, the conclusions arrived and the future work that can be done in this area of research.

CHAPTER 2

MULTI-CHIP PACKAGING

The various multi-chip packaging options available to the microelectronic system designer depends upon (i) the technologies available for bonding chips to the package and (ii) the materials used to fabricate the interconnection layers and substrate. These are described in this chapter.

2.1 Bonding Technology

2.1.1 Wirebond

Single chip packages (SCPs) for microelectronic systems traditionally used wirebond as the the bonding technique. The chips are attached to the substrate with the I/O pads facing up. A special thermally conductive adhesive is used to attach the chips to the substrate. Aluminium wires are used to attached the chip I/O pads and the corresponding metallized pads on the substrate as shown in Figure 2.1.

The primary advantage of wirebonding is that it does not require any new equipment for multichip modules since existing SCP wirebonding equipment can be used. Because of this it is very cost-effective for many low density and low performance applications. The primary disadvantage of this technique is the

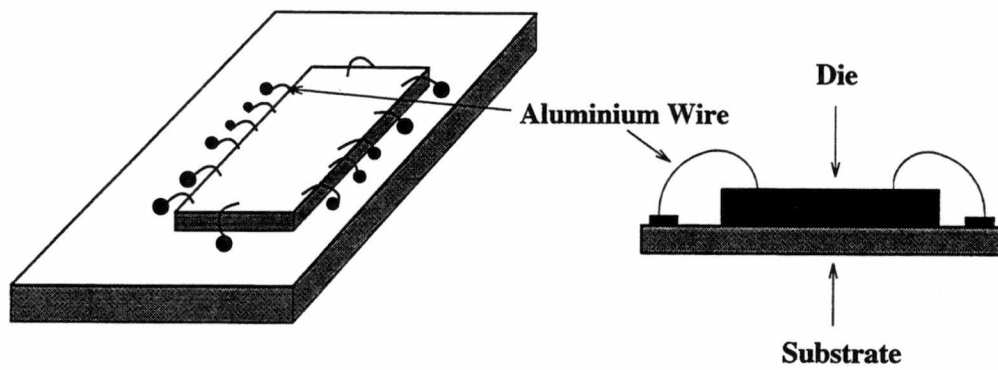


Figure 2.1: *Wire Bonding*

inefficient way of forming the chip connections since this has to be done one pin at a time. The other problem with this technique is the I/O pads must be located on the perimeter of the chip such that area array pads cannot be bonded with this technique. This limits the number of I/O pads that can be accommodated on a given die. The number of I/Os available are of the order of a few hundred [11]. The disadvantage on the electrical performance is the parasitics of the bonding wires which introduce signal degradation.

2.1.2 Flip-chip

In the flip chip bonding technology solder bumps are formed on the I/O pads of the bare dies. The chips are placed face down on the substrate so that the bumps align with contact pads on the substrate surface. The solder is reflowed to form all the contacts simultaneously and attach the bare dies to the metallized substrate as shown in Figure 2.2. The major advantages of flip chip are very low parasitics since there are no leads between the chip and package and very high silicon efficiency. The flip chip technology exhibits self-alignment since any small misalignments in the placement of the chip are automatically corrected due to the surface tension of the solder. In the case of flip chip bonding technology, all the connections between the chip and substrate are completed in parallel in one step, unlike the wirebonding where the connections are made serially. Connections to an area array of I/O pads can be made. Chips with very high pin count of the order of a several hundreds [11] can be handled because of the last two factors

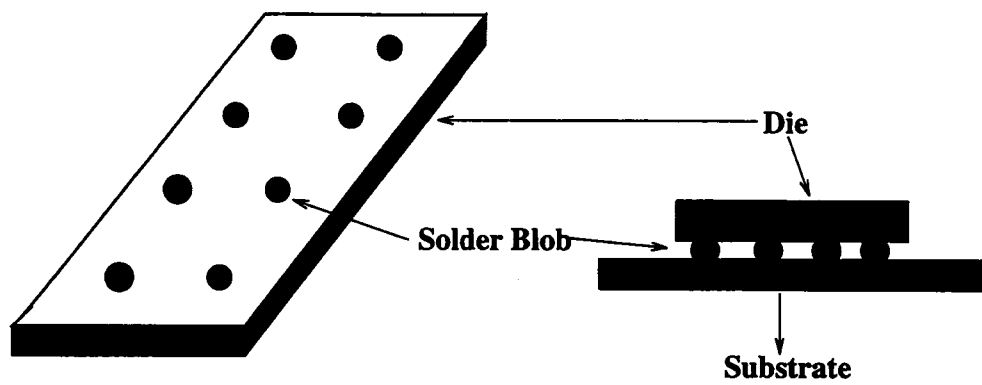


Figure 2.2: *Flipchip Bonding*

mentioned above. Faulty chips can be removed for rework without damaging the chip bond pads. The disadvantage of flip chip technology is that the heat removal from the chips becomes difficult since the back side of the chip is not in contact with the substrate.

2.2 Interconnect Technologies

The microelectronic systems using MCMs are classified as MCM-C (multilayer ceramic), MCM-L (laminated) or MCM-D (deposited thin-film) and are described next.

2.2.1 MCM-C

Packages for high performance computers have used the ceramic multichip module (MCM-C) technology for over a decade [12]. The cross section of the MCM-C substrate is shown in Figure 2.3. The top layer of the MCM-C substrate is used for bonding the chips to the substrate. The metal wiring used for routing interchip connections, connections to module I/O pads, and for supplying power and ground to chips is patterned on each layer. The I/O pads of the module are brazed to the bottom layer.

The ceramic modules are constructed using layers of "greensheet". The greensheet is a mixture of ceramic and glass powder suspended in an organic binder [11]. Holes are punched for the vias and the wiring patterns using molybdenum paste are formed on these layers. A multilayer alumina substrate is obtained

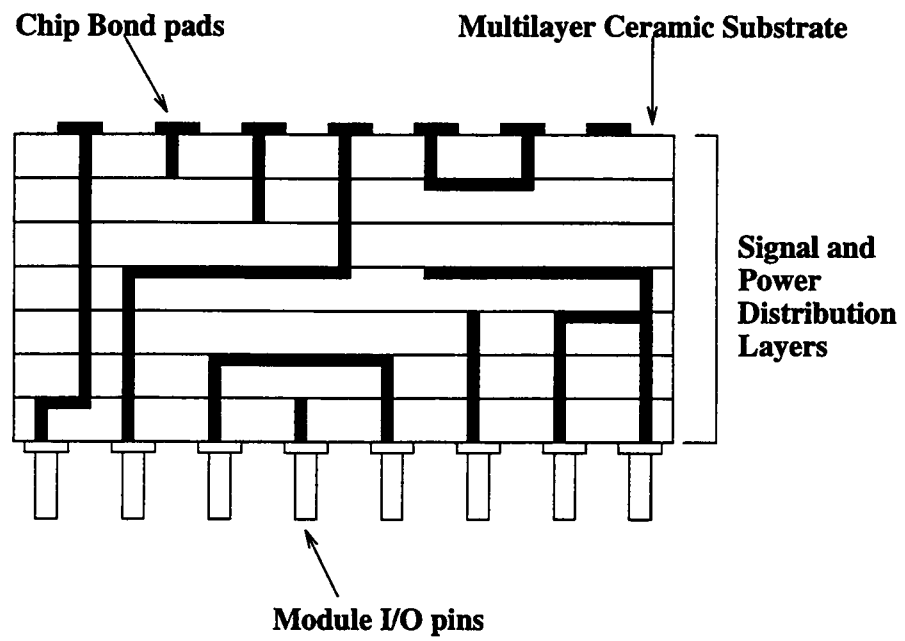


Figure 2.3: *MCM-C Interconnect Technology (after [2]).*

after the layers are stacked together and baked. The major disadvantage of the ceramic substrate is the relatively low wiring density achievable with the screening and punching process used to form the interconnect wiring. Complex designs may require many wiring layers to complete the routing. IBM's recent ceramic module used as many as 63 layers [13]. The advantages of MCM-C are excellent dimensional stability, high reliability and module power dissipation capacity. The cost of this technology is comparable with other MCM substrate technology due to the maturity of the process.

2.2.2 MCM-L

Laminated MCMs basically use finer line width PCB technology. Figure 2.4 illustrates a typical MCM-L substrate. Presently, MCM-L substrate technology offers line width and spacings as fine as 75 microns (3 mils), which is sufficient for several low-cost microelectronic system designs. Among the available substrate technologies MCM-L is the most cost-effective technology for applications which do not require very large routing resources or demand very high performance. This is because MCM-L technology is based on PCB technology which is a mature technology. The disadvantage of MCM-L technology is the poor thermal performance, due to the lower thermal conductivity of the substrate.

2.2.3 MCM-D

MCM-D (Deposited thin film) consists of a substrate over which alternate thin-film dielectric and metallization layers are deposited as shown in Figure 2.5. The

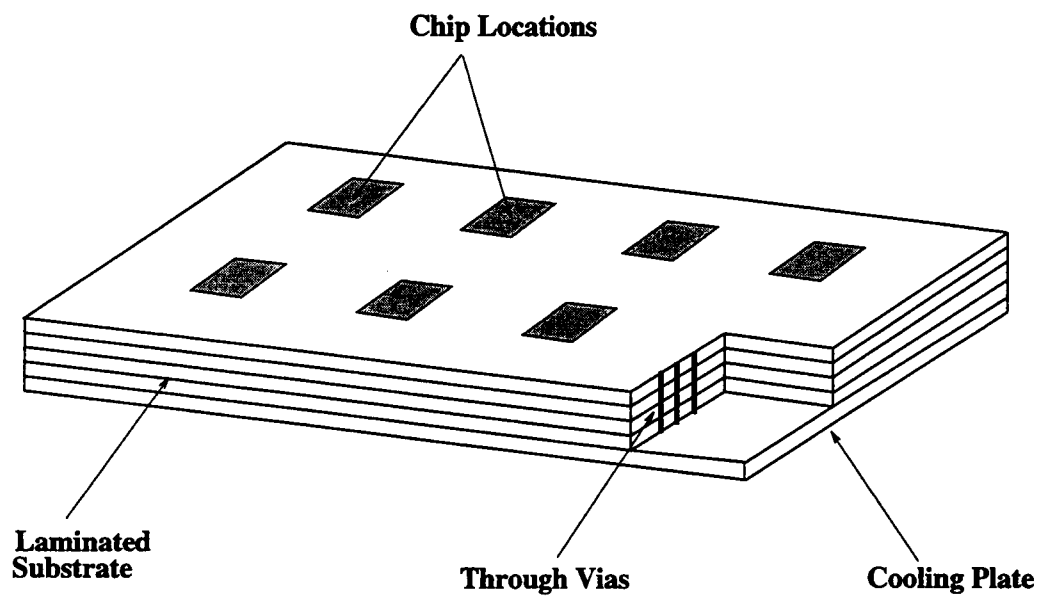


Figure 2.4: *MCM-L Interconnect Technology (after [2]).*

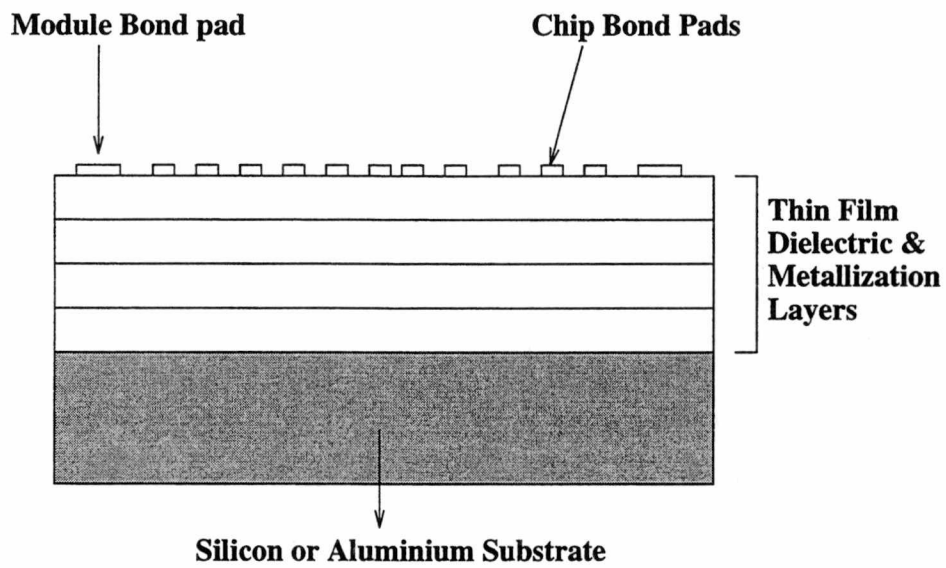


Figure 2.5: *MCM-D Interconnect Technology (after [2]).*

dielectric can be polyimide or silicon. Copper or aluminium is normally used in the metallization layers. The material used for the substrate is ceramic, silicon or aluminium. The wiring capacity is in the order of 1000 inches/sq.inch. Thus the wiring density is comparable to that of on-chip interconnect technology. The prime disadvantage of the MCM-D technology is its high cost mainly due to the lack of vendor infrastructure. Because of the very high wiring capacity offered by the MCM-D technology which exceeds the requirements of most systems, the technology rarely uses more than two signal wiring layers. For applications which require very high interconnect density and operating speeds beyond 200 MHz, MCM-D may become necessary.

2.3 System Impact of Multichip Packaging

The following are the advantages obtained if the microelectronic system is packaged in a multichip module instead of several SCPs on a PCB.

2.3.1 Size

The impact of MCMs on the system size was reported in the development of a digital signal processor (DSP) module consisting of several off-the-shelf chips [14]. Two designs were performed and compared during the development of the DSP module. The first design did not consider the packaging issues but instead focused on hardware and software issues. The DSP module was initially implemented on four printed circuit boards. In the second design the emphasis was on the choice

of package from the early stage of the design. The DSP module was fabricated on a multichip module with a thin film interconnect substrate. The volume reduction achieved in the MCM version was about seventy five times less than the PCB version. The reduction in module size was achieved at the expense of a twofold increase in the cost. The cost is expected to decrease as the production volumes increase for the DSP module and the manufacturing processes for MCMs improve.

In the case of partitioning a large monolithic die into several smaller dies to be packaged in a MCM there is a slight increase in system size. This is due to the need for separation space between the dies. The increase in system size is offset to a great extent by the reduction in cost. The system cost is quite low due to the improvements in the die yield of the smaller dies.

2.3.2 Performance

The system speed was limited by device delays until recently. Now with the higher speed and denser VLSI chips available the packaging becomes a bottleneck for increasing system speed. Considering the next generation processor running at the speed of 200 MHz and the allowable package interconnect delays, the maximum length of an interchip connection can be only 15 cm [14]. A trace on a typical PCB is normally much longer than this. A MCM with 50 or more chips has been fabricated in a 8 cm by 8 cm package [14]. Thus it is evident that use of multichip modules will become inevitable for high speed applications.

The interchip signal delay is comprised of the buffer delay, time-of-flight, rise-time of the received signal, and the settling time of the signal [15]. The buffer delay is directly proportional to the loading capacitance. In MCMs the buffer delays are reduced due to the finer and shorter interchip connections. The time- of- flight of an interchip signal is directly proportional to the length of the interconnection wire, and is thus reduced in MCMs due to the closer chip-to-chip spacing. Parasitic capacitance and inductance in the chip and leads, the resistive losses in the interchip degrade the rise time. Since MCMs eliminate the single chip packages the lead parasitics are significantly reduced. Using MCMs reduces the wire lengths and hence the resistive losses which are directly proportional to the wire lengths are reduced. The settling time depends upon the induced noise which is proportional to the wire length and is thus reduced.

2.3.3 Power Dissipation

Normally, the off-chip drivers contribute to a large portion of power dissipation in the chip. These off-chip pad drivers are designed to be large since they have to charge and discharge the large capacitive loads of the interchip connections of the SCPs on the PCB. The power dissipated by a CMOS off-chip driver is directly proportional to the total load capacitance of the driver. By using an MCM interconnect and flip-chip the load capacitance is greatly reduced due to the finer interchip connections and smaller system size.

The ground bounce is significantly reduced in an MCM due to the reduced

inductance of the power and ground connections. The coupled noise can be reduced by careful physical design. The chip sets specifically designed for MCMs can operate at reduced supply voltages since the noise margins can be lower.

Since power dissipation $P = \sum C * V * f^2$ these chip level modifications will result in a considerable reduction in power consumption. Prolonged battery life, reduced heatsink sizes and increased reliability are the benefits of reduced power consumption.

2.3.4 Reliability

Conventional packaging includes wire bonds from the chip to the SCP, SCP leads, lead-to-board solder joints and plated-through holes (PTHs). These connections are subject to failure due to mechanical and thermal stresses [16]. MCMs will help the system designers to eliminate 50-75% of the failure-prone connections, and replace many of the connections with lower-stress joints [2]. MCMs have become a preferred packaging technology for space applications [17].

2.3.5 Mixed-Technology Integration

The system size can be reduced by using MCMs to integrate the passive components into the substrate [18]. The module yield of the MCMs can be improved by testing and burn-in of the bare dies before assembly. The chips fabricated using the different processes such as analog and digital chips can be integrated on the same MCM module. The chip yield and hence the system yield can be improved by fabricating the memory and logic in separate processes and integrating chips

in one single MCM.

CHAPTER 3

SYSTEM PARTITIONING

3.1 Graph Model for Partitioning

Partitioning is an important step in the design of VLSI systems. The partitioning process involves breaking a large system into smaller subsystems. One of the most important applications of partitioning is circuit packaging where it is used to divide a large design into several chips to satisfy packaging constraints.

In circuit packaging a large circuit is to be divided into many subcircuits that can be implemented in the available MCM technology and IC packages. The packages have a limited size and a limited number of external pins so the partitioning process must limit the size and external connection of each subcircuit.

Several formulations of the partitioning problem including logic partitioning are known to be NP-complete [19]. The computation time for the exact solution of these problems increases exponentially with the number of components in the design and becomes rapidly prohibitive in terms of computation time. For this reason, most of the research in partitioning has concentrated on heuristics which aim at finding a near-optimal solution in a reasonable amount of computation time. The heuristic methods do not guarantee the global optimum solution, but a near optimal solution.

Many factors have to be considered during partitioning since there are some physical constraints which must necessarily be satisfied and there are other factors that need to be optimized. Most of the partitioning techniques are based on a graph model of the design. Figure 3.1(a) shows the simplified version of the net model we use. In our model each net is modeled as an edge in a hypergraph and each functional unit level component is a node in the hypergraph [20]. The partitioning algorithm clusters the functional unit level components into a specified number of separate modules as shown in Figure 3.1(b). After partitioning, each subgraph represents a cluster of components to be placed together on a separate chip as shown in Figure 3.1(c). The main objective of partitioning is to decompose a graph into a set of subgraphs to satisfy some given constraints while minimizing an objective functions, such as the number of edges connecting two subgraphs.

We formulate the partitioning problem as a constraint satisfying problem, so the MCM partitioning can be defined as a partition of the design into a set of chips subject to constraints on area and the I/O pin count. An MCM package can be considered to contain a set of chips with each chip placed in a chip slot. Each chip has constraints on area A_{max} and the maximum number of terminals P_{max} . The system is represented as a hypergraph given as $G = (V, E)$. Each node in the graph denotes a component in the design, and each net represents a net connecting two or more components of the design through their I/O pins.

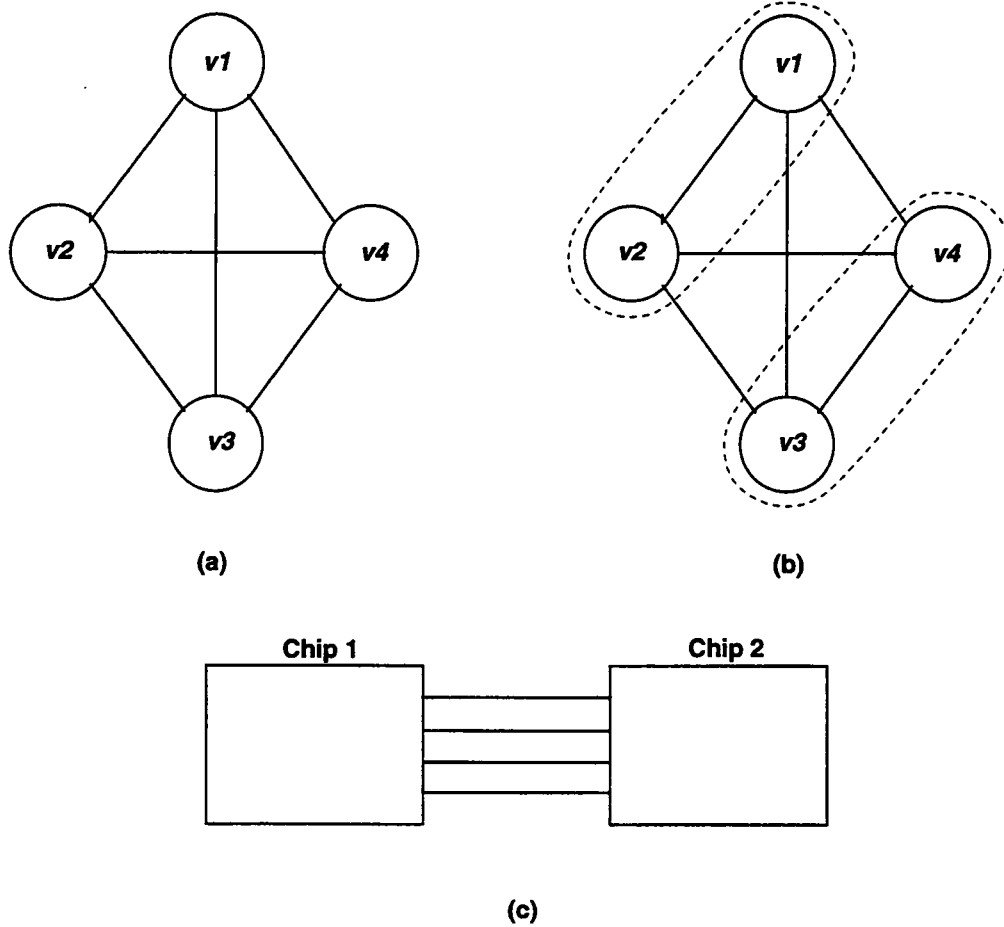


Figure 3.1: (a) *Graph Model for Partitioning* (b) *Clustering of Components during Partitioning* (c) *Physical Representation*

Formally, the partitioning problem can be stated as:

Let $G = (V, E)$ be a hypergraph, where V denotes a set of nodes (corresponding to components), with each node v having some cost associated with it. For example area, power, etc. can be associated as the cost for each node. If A_v is the area of the functional level unit associated with each node of V , then partition V into a set of disjoint subsets $V_1, V_2, \dots, V_k$ subject to the following constraints:

$$\sum_{v \in V_i} P_v \leq P_{max} \quad 1 \leq i \leq k$$

$$\sum_{v \in V_i} A_v \leq A_{max} \quad 1 \leq i \leq k$$

where P_v is the number of nets crossing from any component v in segment V_i to any other segment V_j ($j \neq i$).

3.2 Levels of Design Representation

Partitioning can be performed at different levels of design representation as shown in Figure 3.2. At the functional unit level of design representation there is less amount of data. This allows the system designer to perform an *early analysis* in a short amount of time. The functional unit representation is translated into behavioral and structural levels as the design progresses. There is lots of data to be analyzed at these levels of design representation, which is very time consuming.

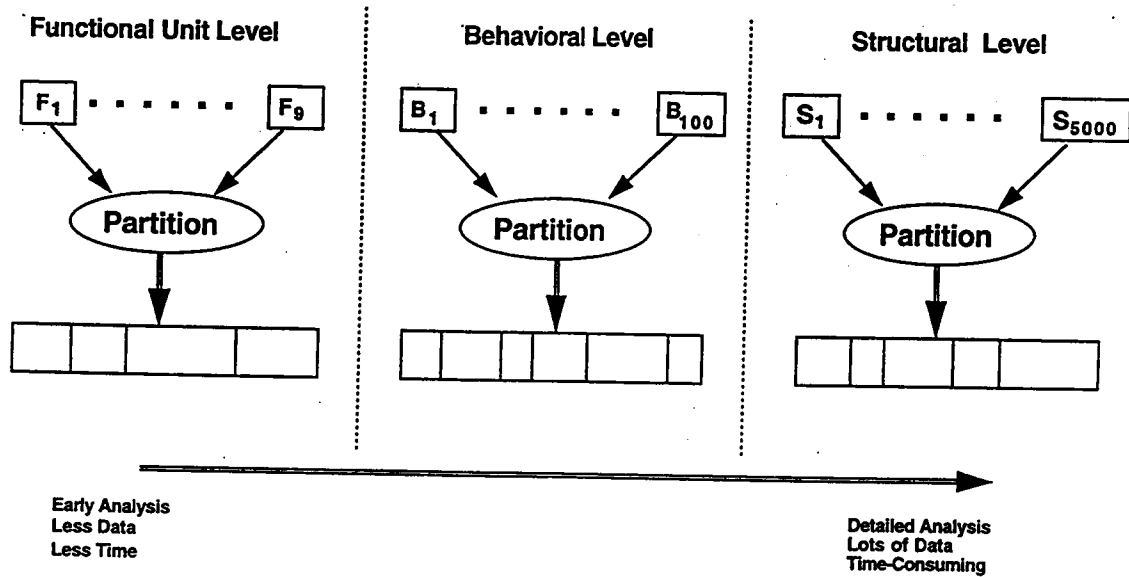


Figure 3.2: *Levels of Design Representation and Partitioning*

3.3 Early Analysis

The various packaging options should be considered from the early stages of system design since packaging plays an important role in the system performance tradeoff. Figure 3.3 shows the costs committed at the different stages of product development. Since 40% of the product cost is determined by the decisions made in the first 10% of the design cycle, critical packaging factors should be explored at the early stages of the design cycle [6]. The early analysis must be done at a high level of design abstraction due to the nature of information available about the design at that time. The basic idea behind the early package analysis is to develop physical models which approximate the models the detail physical tools use later in the design process. Considering the critical packaging issues early in the design cycle and integrating with the overall system design process is termed as Design for Packageability [5]. This concept takes packaging into consideration during chip design for optimizing the overall system performance. Microelectronic system design is highly complex process by itself. The inclusion of package design into the system design calls for a new approach to handle the extra complexity. Early package analysis is the tool to manage this complex system design.

3.4 Algorithmic Methods

Two of the most popular partitioning algorithms are the group migration method developed by Kernighan and Lin [21] or it's modification by Fiduccia and

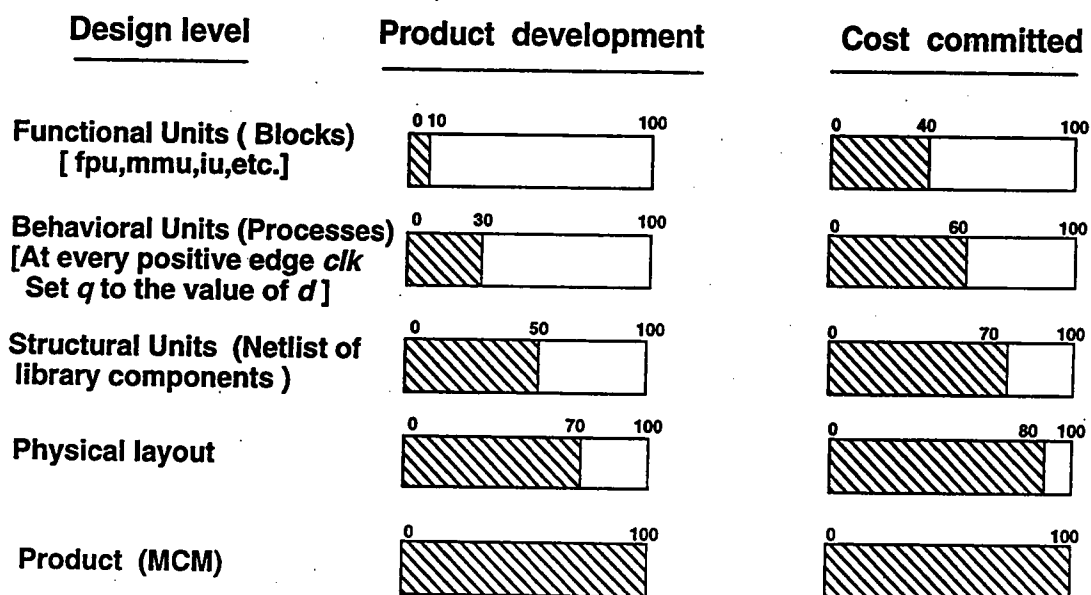
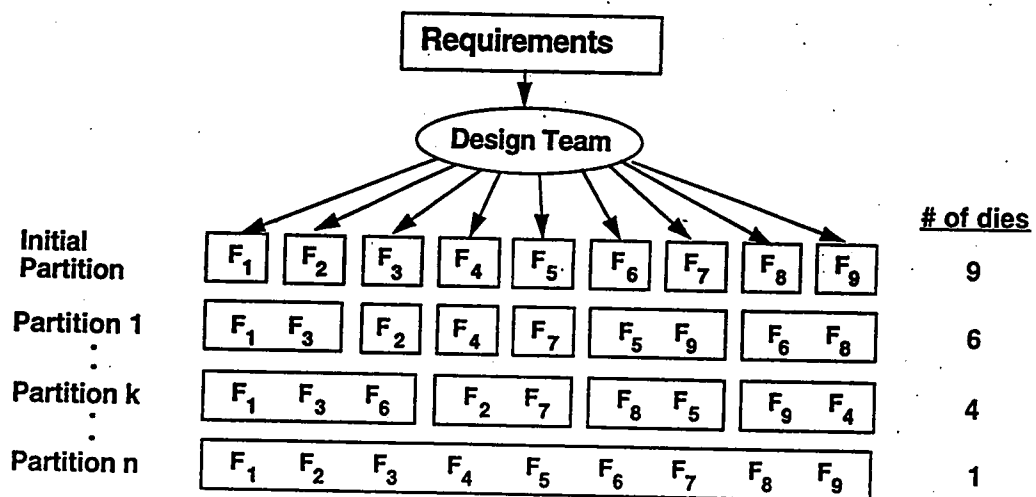


Figure 3.3: *Costs Committed at Different Stages of Product Development*

Mattheyses [22] and the Simulated Annealing method developed by Kirkpatrick et al. [23]. These two algorithms are heuristics which guarantee a near optimal solution in a reasonable amount of time. These algorithms do not guarantee the optimal solution and are used when the design consists of large number of components. The choice of the partitioning algorithm will depend upon the level of abstraction of the design.

3.5 Exhaustive Partitioning

The functional unit level design description of the MicroSparc contains only nine functional units. The number of possible partition candidates is low enough (approx. 21,000) that it is possible to search the solution space exhaustively. This guarantees the best solution will be found. At the early stages of design development it is necessary to find the best solution as major design costs are committed at this stage. At the register transfer level where there are a large number of components, it is more appropriate to use partitioning techniques based on algorithms such as simulated annealing which can guarantee a good solution among several possible solutions. Figure 3.4 shows how the various partitions are determined by clustering the functional units of the design. The algorithm used to generate the partitions is described in detail in [24]. The algorithm starts with an initial partition which consists of all the functional units clustered together to form a single partition. Then the algorithm iteratively generates all the other possible partitions. The partitions range from the single partition where all the



For 9 Functional Units, there are 21,147 possible partitions

Figure 3.4: Exhaustive Partitioning of the MicroSparc Using Clustering of the Functional Unit Level Components

functional units are in one chip to a nine chip partition where each functional unit is a separate chip.

3.6 Effect of Packaging on Partitioning

As a part of this research work we tried to identify the stages in the design cycle which will benefit the most from taking advantage of the new solutions offered by MCM packaging. Figure 3.5 shows how partitioning drives all the system performance parameters such as system cost, size, thermal, power, packaging delay and simultaneous switching noise.

Chip bonding and substrate technologies determine the physical constraints on the partitioning process. It can be seen that the choice of the packaging technology propagates through the partitioning process and then impacts system performance. Thus, there is a need to explore the effect of the various packaging technologies on system partitioning and hence system performance to achieve an optimum system. The main objective of this research work is to study the interaction and impact of the various bonding and substrate technology alternatives on system partitioning and performance.

Partitioning an ultra-large single die into multiple smaller dies housed on a MCM is used as an example; however, this approach can be applied to a larger class of applications using multiple levels of packaging hierarchy.

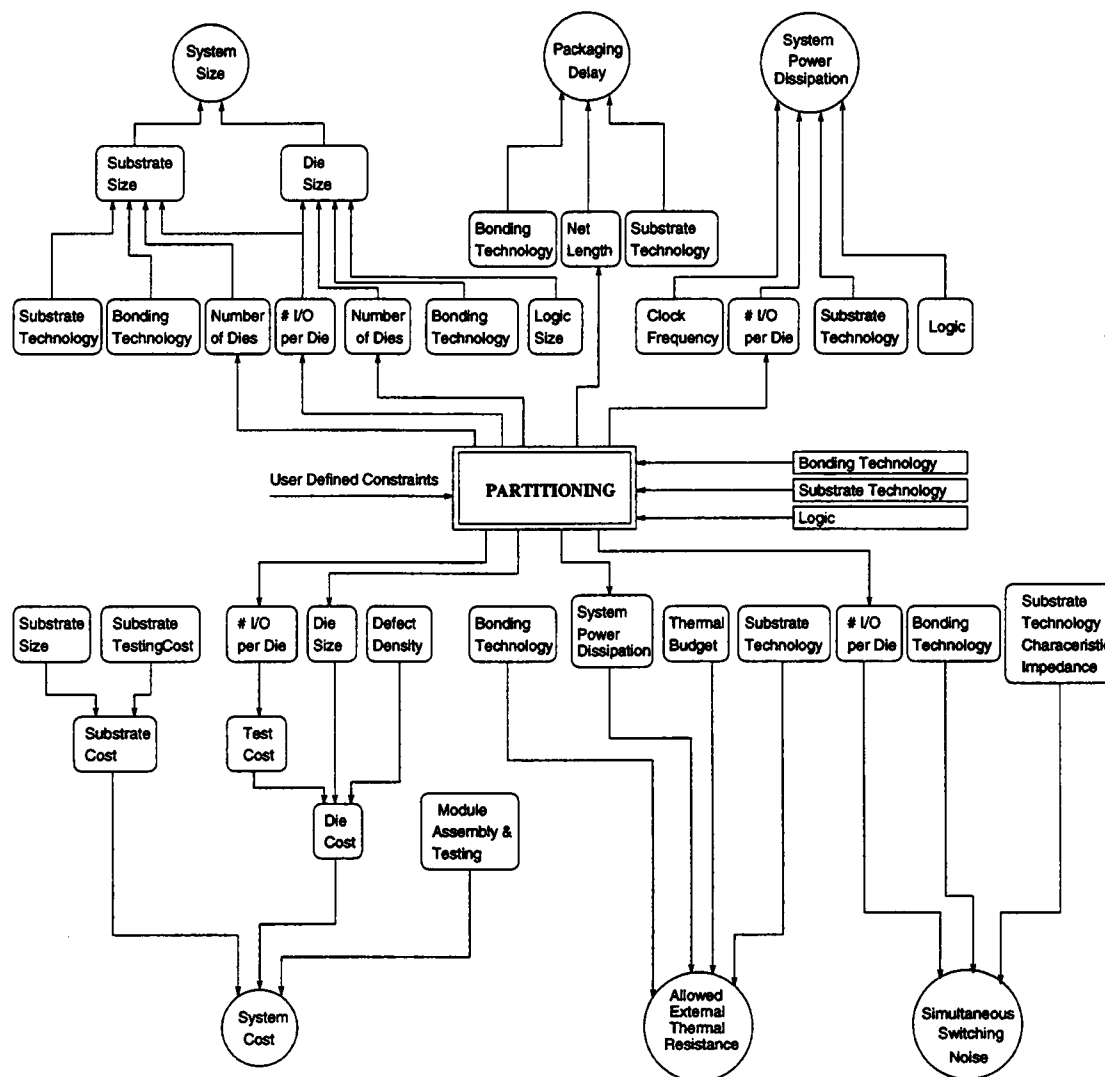


Figure 3.5: *Interaction Between System Performance Parameters and Partitioning Using DFP.*

CHAPTER 4

DESIGN FOR PACKAGEABILITY METHODOLOGY

4.1 Design Flow

The steps involved in our package analysis are shown in Figure 4.1. The user specifies the package and die related information (i.e. bonding technology, maximum die size). The constraint generator derives the I/O constraints from the bonding technology and the maximum die size specified. In the case of wirebond designs the number of I/O that can be accommodated on a given die depends upon the die size and the I/O pitch. For flip chip designs the maximum limit on the number of I/Os not only depend upon the die size and the I/O pitch but also on the escape routing capacity of the substrate. The escape routing refers to the translation of the I/O pads on the die that can escape from the area immediately surrounding the die to find vias, holes, or top layer routing. The escape routing capacity of the substrate depends upon the substrate technology, number of layers and the design rules used. The theoretical maximum number of I/Os that can be escape routed for a given substrate technology is calculated using the simplified relationship given in [25]. The exhaustive partitioner generates the possible candidate partitions. For each candidate partition the die size and die I/O estimates are then calculated for each of the partitions. Next

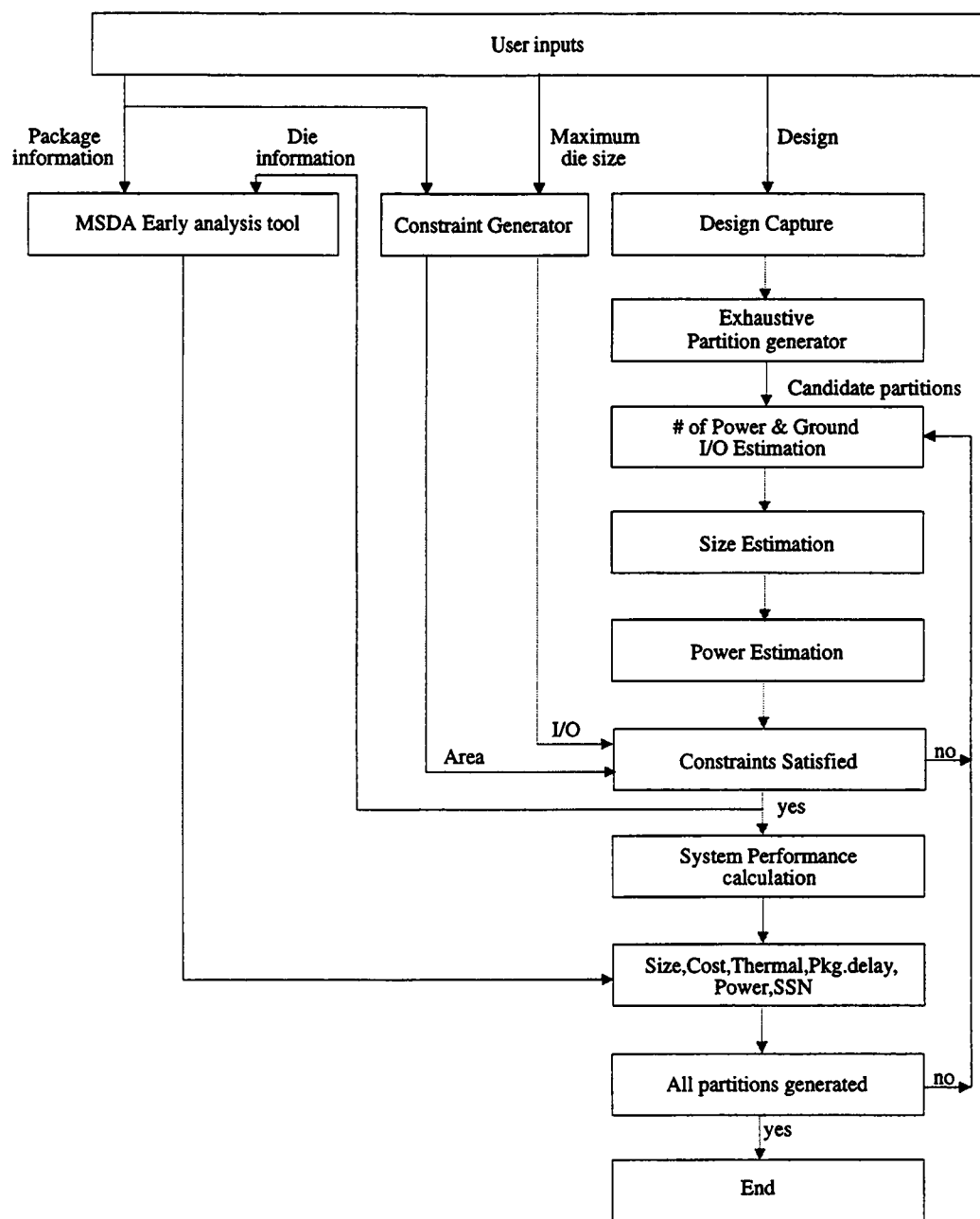


Figure 4.1: *Early Package Analysis Tool - Flow Diagram*

the partitions are verified against the hard constraints of the area of the die and the number of I/Os. These constraints are used to qualify a partition for further processing. Further processing involves estimating the system performance characteristics such as system cost, system size, module power, allowed external thermal resistance, total simultaneous switching noise and the package delay in the module. The MSDA (Multichip System Design Advisor) tool developed by MCC is used to estimate the system performance characteristics.

4.2 Estimation Models

4.2.1 Size Estimation

Die Size

The size of the die is an important issue to the system designer because of the low manufacturing yield of large dies. The cost of the die increases exponentially with the die size. Cost and ever increasing complexity of today's microelectronic systems require the system designer to utilize properly and efficiently the available silicon on a die.

Wirebond Die Size

The layout of wire-bond IC is as shown in Figure 4.2. In this type of die design the circuit core is surrounded by the I/O pads on the perimeter of the die. The interconnection between a gate and an I/O pad consists of the inner-core and

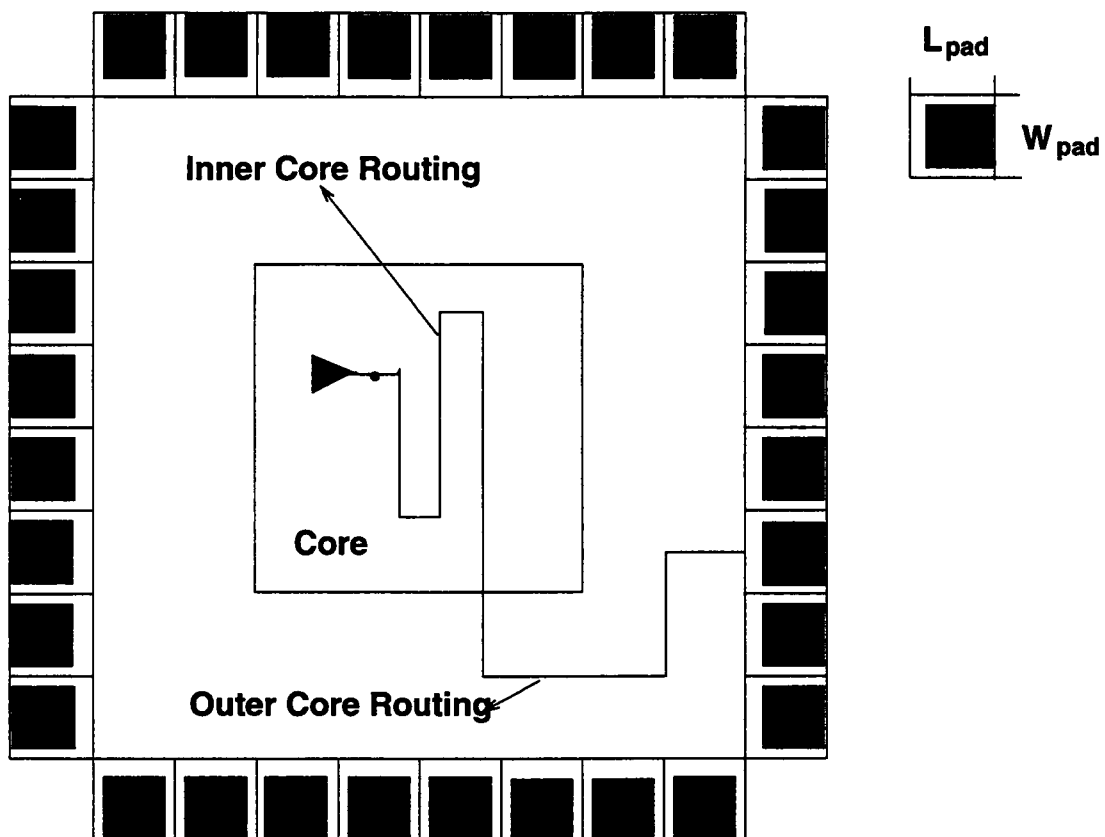


Figure 4.2: *Layout of Wirebond die - Core Routing and I/O Pads*

outer-core segments. The size estimation is similar to the formulations developed in [7] [8]. For a wirebonded die with a single row of bond pads on all four sides, the area of the die A_{die} is given by the maximum of two limits:

$$A_{die} = (2 * L_{pad} + W_{pad} * N_{pad}/4)^2 \quad (4.1)$$

$$A_{die} = (1 + k * N_{pad})A_{core} + N_{pad} * L_{pad} * W_{pad} \quad (4.2)$$

In Equation 4.1 and Equation 4.2 L_{pad} , W_{pad} , N_{pad} are the length, width and the number of I/O pad respectively. A_{core} is the area of the core of the die. k is the fractional increase in the core die area necessary to accommodate redistribution of one I/O to the periphery of the die. Equation 4.1 is the I/O limited die area and Equation 4.2 is the core limited die area. In [7] it was found that the value of k was approximately a constant for three different types of chips synthesized.

Flip-chip Area Array Die Size

Figure 4.3 shows the layout of the flipchip area array chip. The size of the I/O pads in the flip-chip are much smaller than wirebond pads. In the flipchip area array layout the I/O pads do not have to be placed on the perimeter of the chip. This allows the I/O pads to be placed within the chip core right next to the gate that needs to be connected to pads. This reduces the inner core routing between the gates and the I/O pads, resulting in an additional reduction in size. The outer core routing can be totally eliminated in the flipchip area array design.

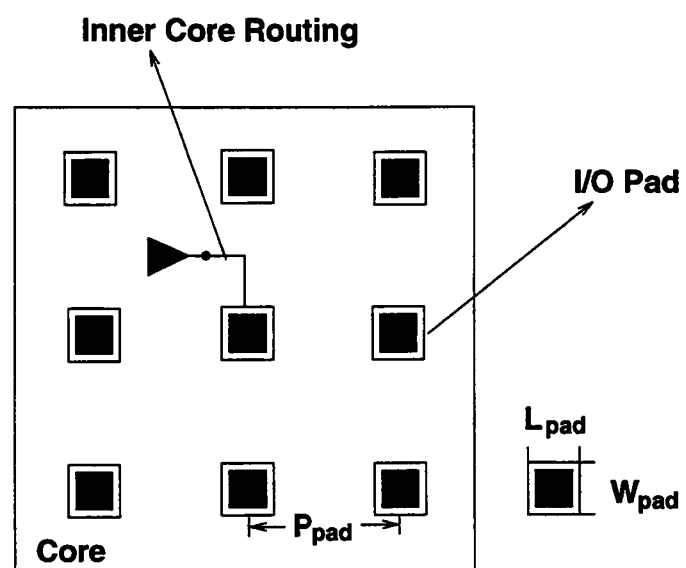


Figure 4.3: *Layout of Flipchip - Core Routing and I/O Pads*

The die area A_{die} is given by the maximum of two limits:

$$A_{die} = (P_{pad} * \sqrt{N_{pad}})^2 \quad (4.3)$$

$$A_{die} = N_{pad} * L_{pad} * W_{pad} + A_{core} \quad (4.4)$$

Equation 4.3 is the I/O limited die area. P_{pad} is the pitch of the I/O pads. Equation 4.4 is the core-limited die area which assumes that active circuitry cannot be placed under the bond pads.

4.2.2 Cost Estimation

The MCM system cost is mainly comprised of the cost of the die in the partition and substrate. So the system cost can be represented by the following equation:

$$\text{System Cost} = f (\text{Cost of Dies in the Partition, Interconnect Cost})$$

Die Cost Models

The simplified models used in the determination of the cost of the dies in the partition are described in the following equations:

$$N_{die} = \frac{\pi * (D_{wafer})^2}{4 * A_{die}} \quad (4.5)$$

In Equation 4.5 N_{die} is the number of dies that can be realized on a single wafer. D_{wafer} is the diameter of the wafer in inches which is an user input to the tool. The area of the die is given by A_{die} and is calculated by the tool and

which depends upon the component size and a rough estimate of the routing area needed.

$$P_{die} = \left[\frac{1 - \exp(-A_{die} * \rho)}{A_{Die}} \right]^2 \quad (4.6)$$

Equation 4.6 is Murphy's yield law [26] where P_{die} is the probability that the dies that can be fabricated on the wafer are good, i.e. not defective. ρ is the defect density, the number of defects that is permitted for the dies to be certified as a good die. The defect density is given as defects/sq.cm and is provided by the user. In the case of flip-chip designs the defects due to wafer bumping is also included in the defect density.

$$C_{die} = \frac{C_{wafer}}{(int)(N_{die} * P_{die})} + \frac{C_{NRE}}{Q} + C_{assm} \quad (4.7)$$

C_{die} in Equation 4.7 is the cost of the die calculated using the simplified models. The wafer cost is given by C_{wafer} . C_{NRE} is the NRE (Non-Recurring Engineering) cost of the design. The quantity of dies to be fabricated is given by Q . C_{assm} is the cost of assembly of a die. C_{wafer} , C_{NRE} , Q , C_{assm} are user inputs to the tool.

$$C_{part} = \sum_{i=1}^n C_{die_i} \quad (4.8)$$

C_{part} in Equation 4.8 is the cost of all the dies in the partition.

Substrate Cost

The predicted interconnect cost model available in the MSDA tool is used to evaluate the cost of the substrate [25]. The interconnect costs are found from the relation between interconnect capacity and cost per sq.inch as shown in Figure 4.4. In the case of PCB a look up table which the user can update was used [25].

4.2.3 Power Dissipation Estimation

The power dissipation of the die is modeled as a combination of the power consumption due to logic, buffer and charging of net capacitances. The power consumption of the logic of the entire design is given as a user input. From this the power consumption of the logic for each die is calculated as a quantity proportional to the ratio of the area of logic in the die to the area of the logic of the entire design. The power consumption due to the buffer and the net capacitance is calculated using the following equation:

$$P = (SC * f) + (V^2 * f * C_L) \quad (4.9)$$

The first term in the Equation 4.9 is the short circuit power dissipation. There is a short circuit between power and ground when the input of a gate is between valid logic levels. If the threshold voltages for the N and P transistors were 1 volt, then there would be conduction when the input was approximately between 1 and 4 volts. The short circuit power dissipation depends upon the characteristics of

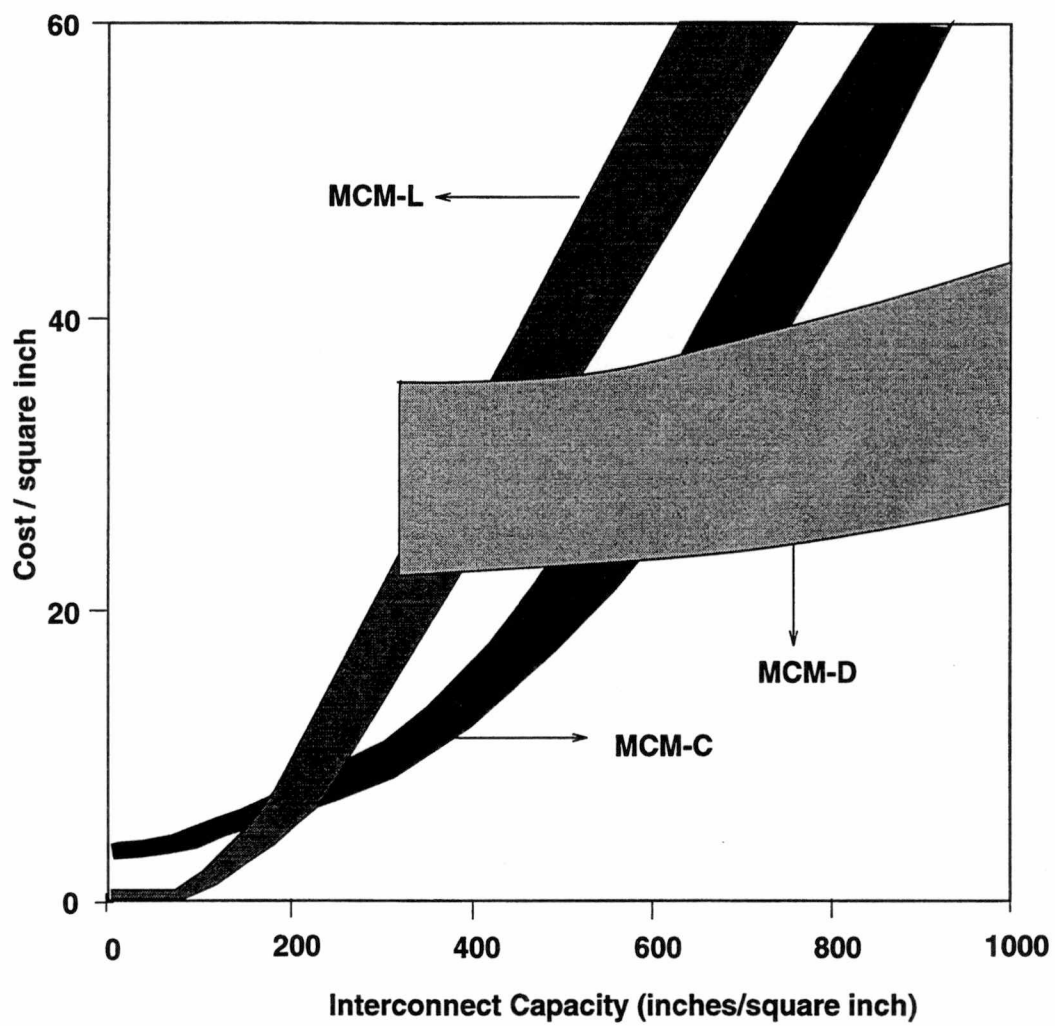


Figure 4.4: *Cost per Square Inch of Major Interconnect Technologies (after [25]).*

of the input signal (i.e. the rise time, the fall time, and the switching frequency). The slower the rise and fall times are, the longer the input is between valid logic levels and so the conduction path exists for a longer time. Also, the more often the input switches, the more often this path exists. For the drivers being used we assume an input risetime of 1ns and the simulations performed [26] show that the short circuit power is linearly dependent on switching frequency. The typical short circuit constant (SC) determined is $10 \times e^{-12}$.

The second term in the Equation 4.9 is the ac switching power consumption. This is due to the charging of the net capacitance when the output of gate switches between the logic levels. The capacitance per unit net length depends upon the type of substrate used in the MCM. The typical values capacitance per unit length for different substrate technologies are 1.46pF, 2.10pF, 1.25pF for MCM-L, MCM-C, MCM-D respectively. The net length is approximated as the diagonal length of the module. It is assumed that half the total number of pins in the die are outputs.

4.2.4 Thermal Resistance Estimation

The MSDA tradeoff analysis tool [25] is used to compute the external thermal resistance associated with each component that has power dissipation and thermal budget defined. The type of cooling used for the system should be considered when the external thermal resistance R_{ext} is computed. The external thermal resistance is a measure of the size of the external heat sink needed for the sys-

tem. The lower the value of the external thermal resistance the larger the heat sink needed to meet the thermal budget criterion. So the size of the heat sink needed is determined by the component having the lowest external thermal resistance which is called as the worst case external thermal resistance. The external thermal resistance for a component is found from the following equation:

$$R_{ext} = \frac{thermalbudget - R_{int} * P_c}{P_m} \quad (4.10)$$

In Equation 4.10 *thermal budget* is the allowed maximum temperature rise over the ambient for the component, we have assumed a value of 55° C. P_c is the power dissipation of the component calculated by the early package analysis tool. R_{int} and P_m are the internal thermal resistance of each component and the total partition power dissipation respectively. The last two quantities are determined by the MSDA tool.

4.2.5 Delay Estimation

The interconnect line on the MCM substrate was modeled as either lumped RLC or a transmission-line based on their lengths. Each line was terminated and a total of eight receivers were assumed for each driver. To determine the chip delay the interconnect line was modeled as RC line. The chip was assumed to be fabricated using a 0.8μ process. The MCM-D process was assumed to have a dielectric constant of 3.5 and trace width of 15μ . The MCM-C process had a dielectric constant of 7.9 and trace width of 76.2μ . For the MCM-L process the

dielectric constant was 3.5 and the trace width was 101.6μ . SPICE was used to simulate the MCM and chip delay models [27]. The simulation results of the chip and MCM delays are shown in Figure 4.5. The delay for the MCM module was computed for the interconnect length equal to the diagonal length of the module. For the monolithic case, the delay was calculated for an interconnect signal line within the die with a length equal to the diagonal length of the die.

4.2.6 Noise Estimation

One of the major problems faced by the system designers in the design of high performance systems is switching, or delta-I noise. The simultaneous switching noise originates when the output drivers switch current drawn from an inductive power distribution system. Switching noise is defined by the expression

$$V_{noise} = n * L_{eff} * \frac{di}{dt} \quad (4.11)$$

In Equation 4.11 V_{noise} is the magnitude of switching noise. n is the number of simultaneously switching drivers. $\frac{di}{dt}$, L_{eff} is the current slew rate of one driver and the effective inductance of the path through which the current flows.

The inductance of bonding leads, single chip packages, power/ground delivery system all contribute to switching noise. The most immediate source of inductance to a switching gate is due to bonds. It is important to decrease the effective inductance of the bonding leads as much as possible. The way to reduce the inductance is to make the length bonds short. For flipchip bonding the bond length

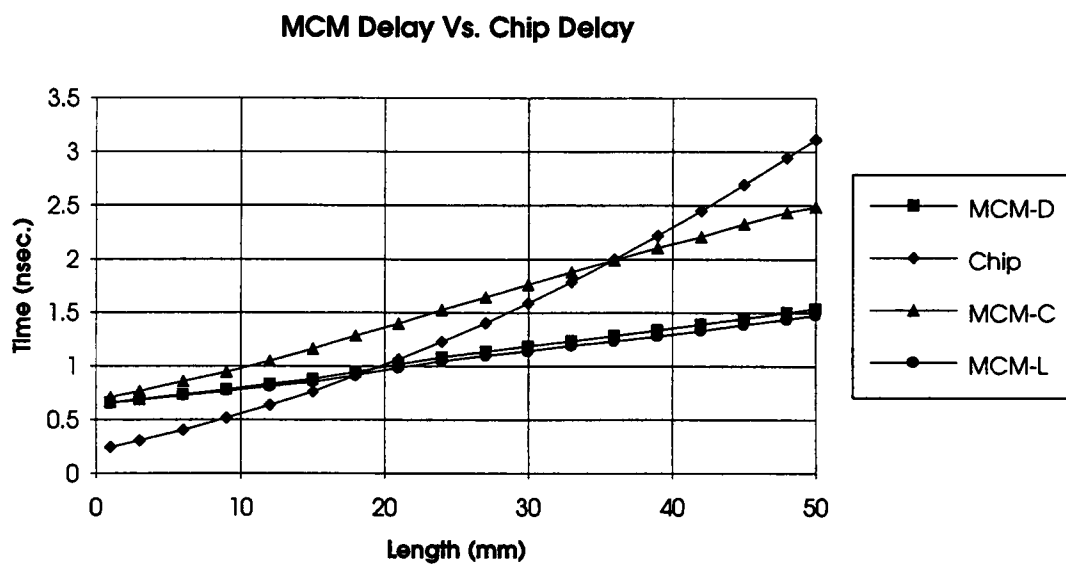


Figure 4.5: *Simulated Delays for Different MCM Substrate and Chip Interconnect Technologies*

is very much small compared to the wirebond.

The number of simultaneously switching drivers n is dependent upon the type of the application. It is calculated from the the ratio of simultaneous switching drivers which is an input to early package analysis tool. The switching noise calculation in performed by MSDA tradeoff analysis is confined to the treatment of switching noise due to bonds [25].

CHAPTER 5

CASE STUDY AND RESULTS

5.1 Demonstration Vehicle

The SUN MicroSparc is used as a demonstration vehicle to illustrate the extent of the interaction. This RISC processor design consists of about 750,000 transistors. This is one of the large industrial example which we have chosen to validate our approach. We choose to represent the MicroSparc design at the functional unit level for two reasons. First, we proposed to perform an early analysis and the design is available only at the functional level of design abstraction during the early stages of design development. Secondly, most of the industrial designs are proprietary and the design is made available to the packaging consultants only at the functional level. The design is described at the functional unit level consisting of the following: integer unit (IU), floating point unit (FU), memory management unit (MMU), data cache (D-CACHE), instruction cache (I-CACHE), s-bus controller (S-BUS-CTL), memory interface unit (MEM-INTF), clock control and buffers (CLK-CTL), and miscellaneous control logic (MISC) as shown in Figure 5.1.

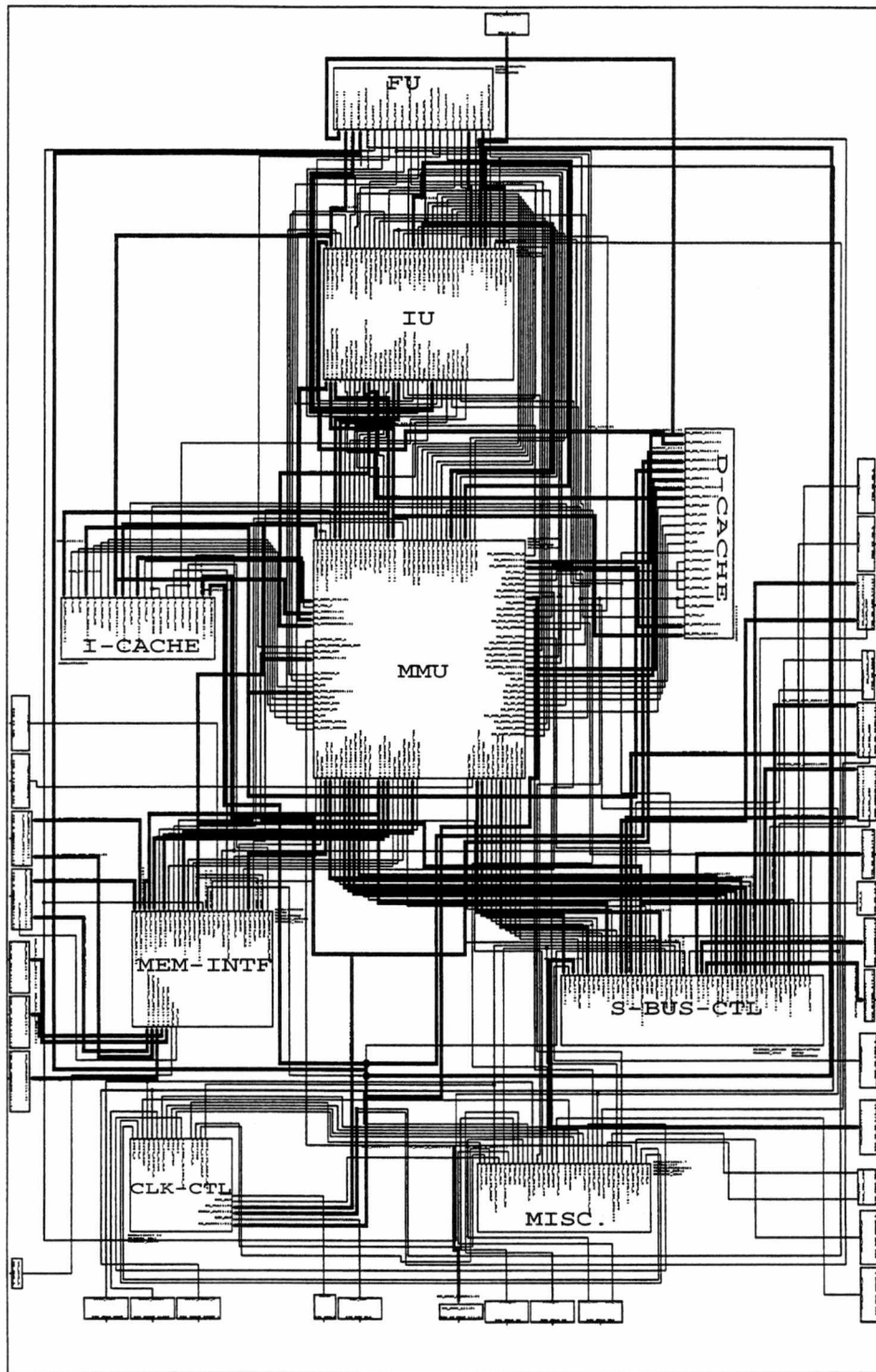


Figure 5.1: *Functional Unit Level Design representation of MicroSparc.*

5.2 Results

We have concurrently considered the following:

- a) Wire-Bond/MCM-C
- b) Wire-Bond/MCM-D
- c) Wire-Bond/MCM-L
- d) Flip-Chip/MCM-C
- e) Flip-Chip/MCM-D
- f) Flip-Chip/MCM-L

The exhaustive partitioner has generated over 21,000 partitions for each type of packaging but only those partitions that meet the die and package constraints have been considered for analysis. The die parameters provided by the user are given in Table 5.1.

5.2.1 Size Analysis

Figure 5.2 shows the size of the partitions which offer the lowest system cost. The flip-chip design using MCM-D exhibits the smallest module size. This is due to the combination of the reduction in die area because of area-array bonding and the reduction in substrate size with the use of MCM-D interconnect.

Table 5.1: *Die Assumptions Provided by the User.*

Property	Value
Signal/Ground (peripheral)	4
Signal/Ground (area array)	6
Bond pad size (peripheral)	200 * 200 (microns)
Bond pad size (area array)	125 * 125 (microns)
Min Bond Pad pitch (peripheral)	200 (microns)
Min Bond Pad pitch (area array)	250(microns)
Wafer Diameter	6 inches
Unusable Wafer Border	0.4 inches
Wafer defect density	3 defects per sq.inch
Processed Wafer cost	\$800
Wafer Bumping cost	\$200
Defects due to Wafer Bumping	0.2 defects per inch
Die Test cost	\$0.01 per I/O

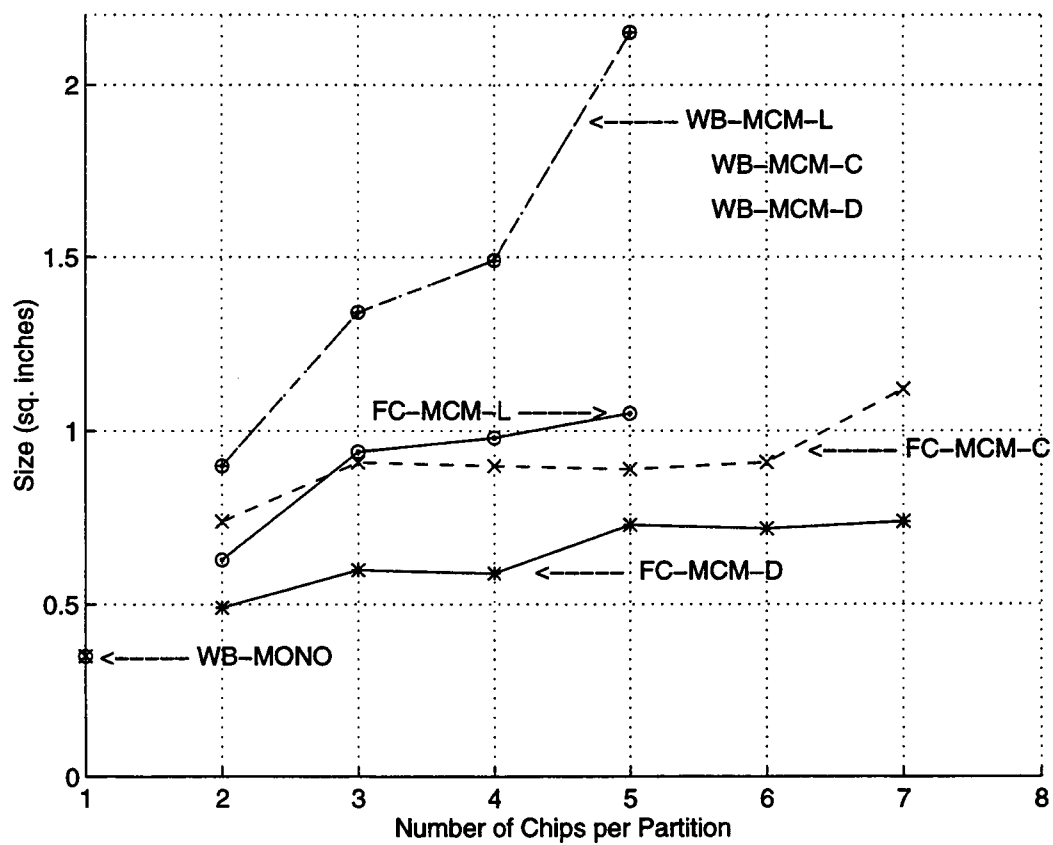


Figure 5.2: *System Size Analysis Results*

5.2.2 Cost Analysis

The result of the cost analysis is shown in Figure 5.3 which displays those partitions satisfying the given constraints with the lowest system cost for a particular number of dies in the die set. The FC/MCM-D design offers the lowest overall system cost for implementing this particular application in a MCM. The system cost is comprised of the die, bonding, substrate and assembly cost. The substrate and assembly cost estimates used in this analysis are discussed in [8]. The flip chip design offers higher I/O count and takes full advantage of the higher interconnect density of the MCM-D. The combination of these two choices reduces the die area (and hence the die cost) considerably as compared to the conventional peripheral wire-bond design. It should be noted that FC/MCM-D design is not highly sensitive to the number of chips in the partition.

The multichip designs implemented in WB/MCM-C and WB/MCM-D exhibit the highest overall system cost. The lower I/O count offered by the peripheral wire-bond design results in larger die area which results in reduced yield and higher die cost.

For this application, the die cost in the wire-bond case dominates the substrate and assembly costs. Therefore, the die set which offers the lowest system cost is the same for the wire-bond designs using any of the three substrates. However, this is not true for the flip-chip designs since their die costs are comparable to the substrate and assembly costs.

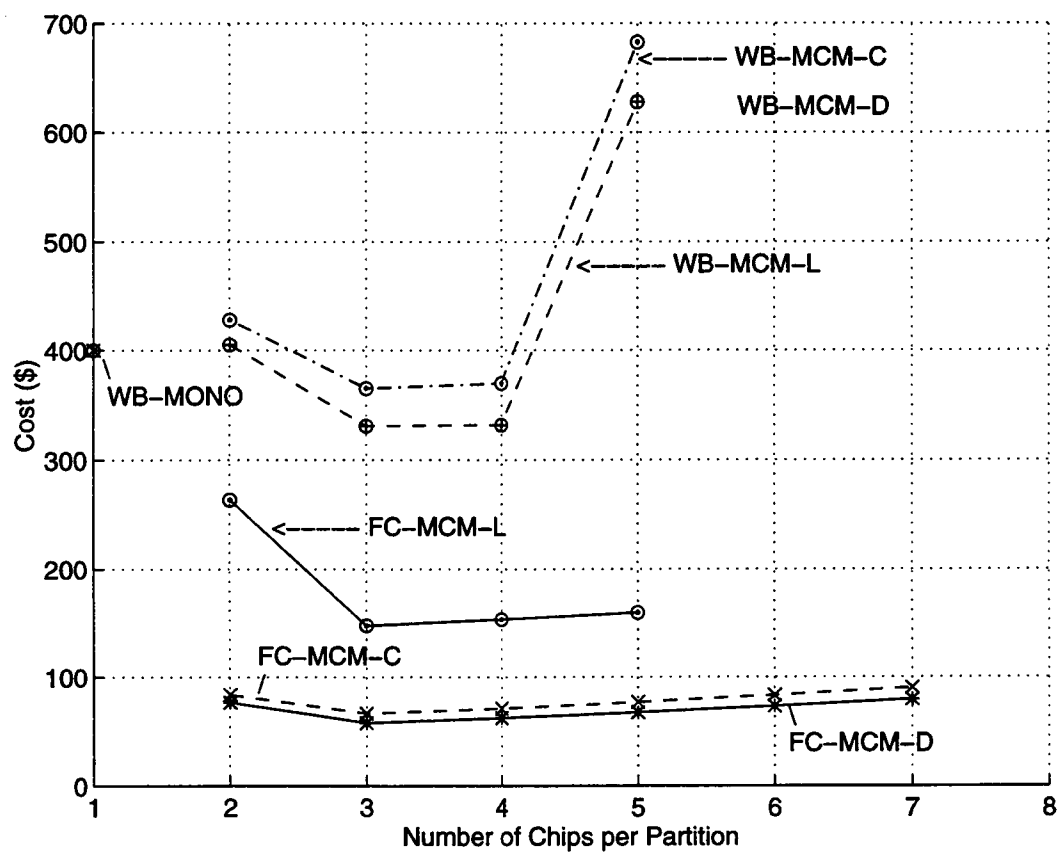


Figure 5.3: *System Cost Analysis Results*

5.2.3 Power Dissipation Analysis

Figure 5.4 shows the total power dissipation of the modules which have the lowest system cost. The flip-chip/MCM-D designs have higher power dissipation compared to the wire-bond designs since the flip-chip designs have more I/Os. The flip-chip/MCM-C has the worst power dissipation due to the higher interconnect capacitance of the substrate. In this particular application, the power dissipation increases with the increase in number of chips due to the increase in the number of outputs in the die-set.

5.2.4 Thermal Resistance Analysis

Figure 5.5 shows the results of the early thermal analysis. The worst-case external thermal resistance of the die in the partition is heavily dependent upon the total power dissipation in the module. Higher values of external thermal resistance indicate less power dissipation inside the MCM. Thus, the external thermal resistance decreases with the increase in the number of chips in the partition. There are some versions of flip-chip/MCM-D where special process techniques (e.g. potting and lapping the completed assembly) result in better external thermal resistance characteristics.

5.2.5 Delay Analysis

Figure 5.6 shows a figure-of-merit for packaging delay of these MCM systems. Among the multichip options the designs which use flip-chip bonding and

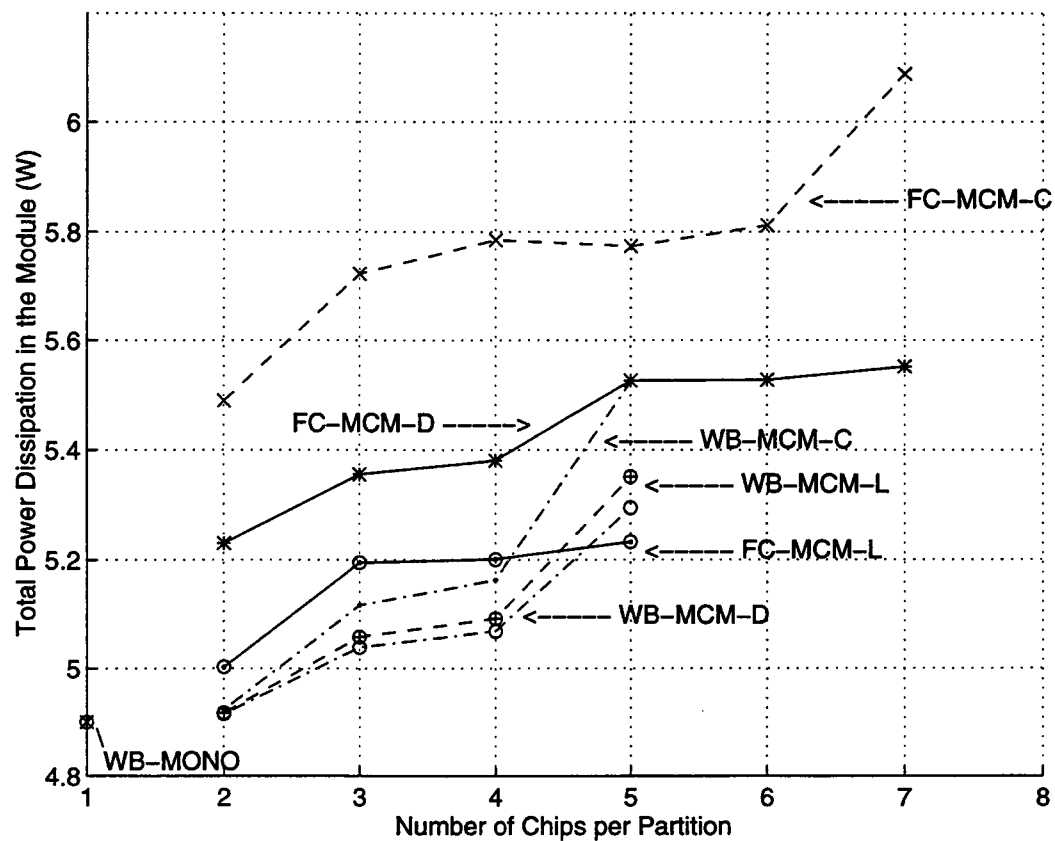


Figure 5.4: System Power Dissipation Analysis Results

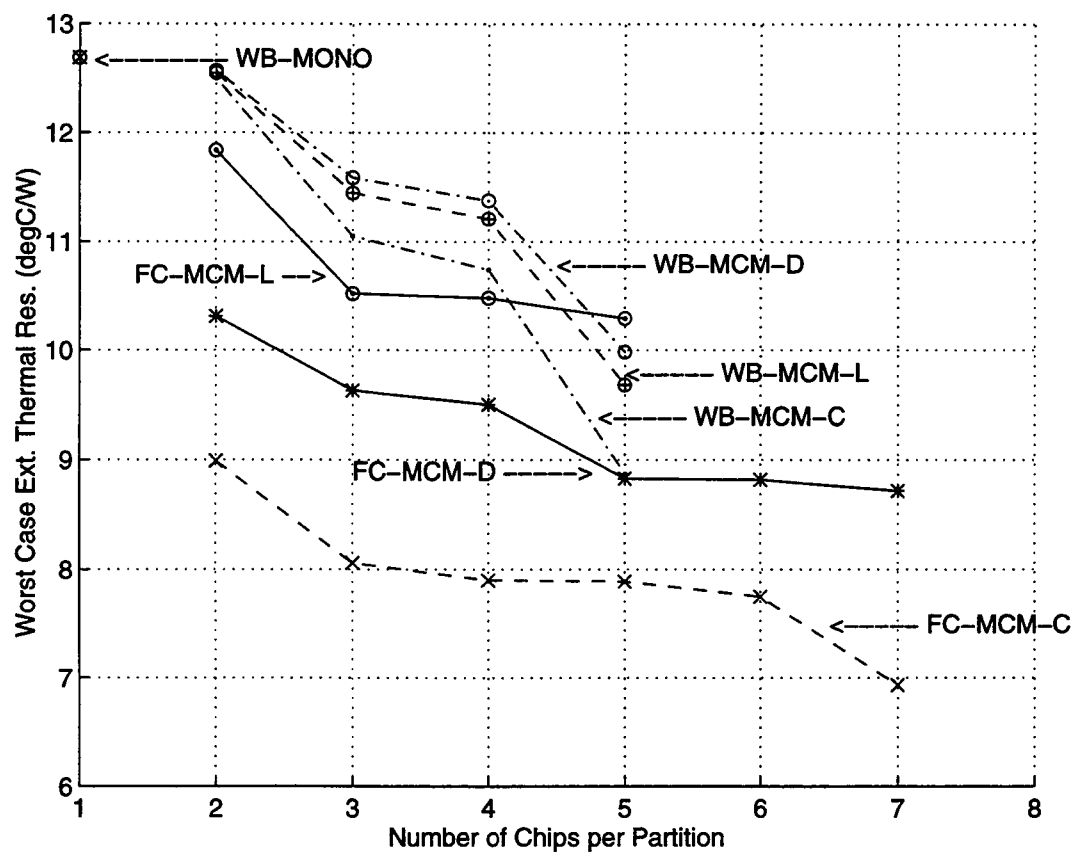


Figure 5.5: *System Thermal Analysis Results*

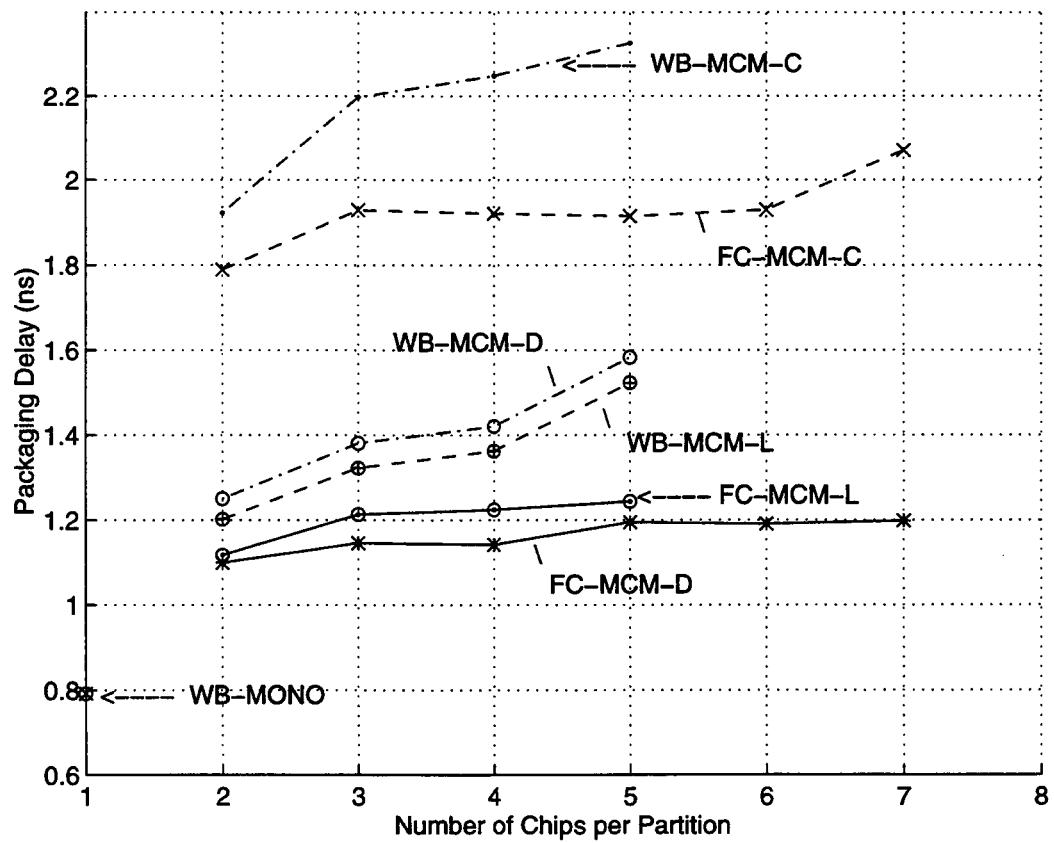


Figure 5.6: *System Delay Analysis Results*

MCM-D substrate have the lowest package delay. This is due to the lower dielectric constant of the MCM-D substrate and the smaller feature size of the flipchip. The interconnect lengths in the MCM design is not long enough to take full advantage of the advanced substrate technologies as shown in Figure 4.5. So the delay for the MCM designs are higher compared to the monolithic design.

5.2.6 Noise Analysis

A measure of the simultaneous switching noise analysis is shown in Figure 5.7. The noise data shown corresponds to the partitions having the lowest system cost. The flip-chip designs have lower inductance and hence have lower switching noise.

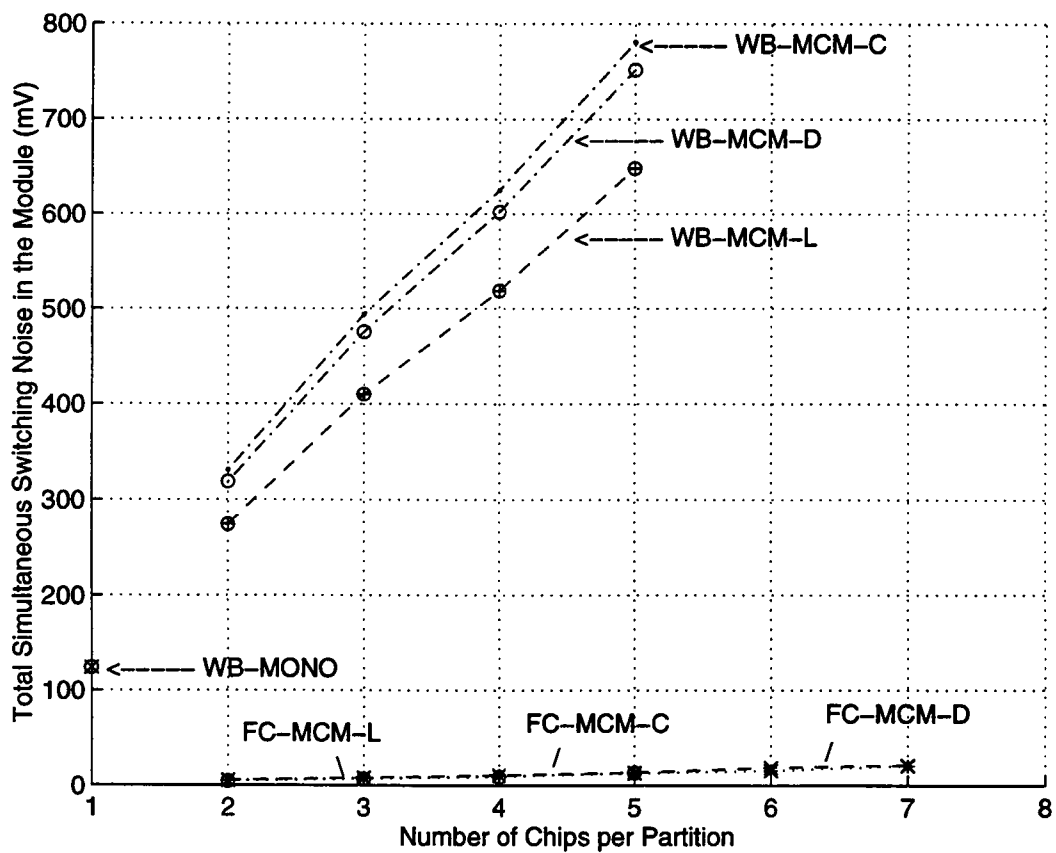


Figure 5.7: *System Noise Analysis Results*

CHAPTER 6

SUMMARY, CONCLUSIONS AND FUTURE WORK

6.1 Summary

The nature and the extent of the packaging technology on the system partitioning has been established in this work. An early package analysis tool has been developed and the SUN MicroSparc design was used as a demonstration vehicle to support the methodology. Each type of MCM technology has a different cost/performance characteristic. It is important to evaluate these technologies for the specific application in hand for the best price/performance. Evaluation and selection of these technologies should not be solely based on the physical and electrical characteristics of the technology itself. Instead it should be based on price/performance of the entire system by considering the interdependency of MCM technologies and partitioning at the system level.

6.2 Conclusions

The performance parameters of cost, size, power, thermal, simultaneous switching noise and package delay for the six different packaging alternatives are shown in Table 6.2. The candidate ranking was arrived by considering an

overall figure of merit of the various system performance parameters. The best partition, consisting of three dies, is shown in Table 6.2.

Table 6.1: *Comparison of System Parameters for Different Bonding and Substrate Technologies.*

	Monolithic	WB MCM-L	WB MCM-C	WB MCM-D	FC MCM-L	FC MCM-C	FC MCM-D
System Cost (\$)	400.05	330.70	365.17	364.94	147.46	66.18	57.45
System Size in^2	0.3488	1.34	1.34	1.34	0.9	0.91	0.6
Module Power (W)	4.9	5.0579	5.1162	5.0388	5.1946	5.7227	5.6963
Ext. Therm. Res. (degC/W)	12.69	11.45	11.05	11.59	10.52	8.06	9.63
SSN	124	410	494.17	476.03	6.85	8.07	7.77
Pkg. Delay (ns)	0.7918	1.3229	2.1792	1.3806	1.2134	1.9289	1.1459
Ranking		4	6	5	2	3	1

Table 6.2: *Contents of the Best Overall Partition.*

Chip	Pins	Area (mm ²)	Modules
1	485	49.428059	D-CACHE, I-CACHE, MMU
2	298	45.510590	FU, IU
3	414	28.451555	MEM-INTF, SBC, CLK-CTL, MISC.

For this particular application, the results indicate that the overall system cost would be reduced by a factor of seven if the single-chip CPU were divided into three chips, bonded using flip-chip technology and interconnected on an MCM-D substrate.

6.3 Future Work

To date, the functionality of the partitions has not been considered by the partitioning tool. There is still a need for an experienced system architect designer to compare the results for the best design architecture. We plan to analyze the cost/performance of the different cache sizes added to the design and perform the detailed analysis of the above candidate designs to verify the validity of the model used in the analysis.

The methodology of partitioning with DFP in mind is applied here to a design described in the functional unit level. We plan to extend this concept to designs described at the behavioral and structural (RTL) levels as well.

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