Lifetime Estimation of IGBTs in a Grid-connected STATCOM

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Dedicated to my sources of inspiration, my parents

Mukunda Reddy GopiReddy

&

Swaroopa Reddy GopiReddy

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ABSTRACT

Lifetime estimation of power semiconductor devices, and IGBT devices in particular, used in the power electronics integrated with power systems has gained technical importance in recent times with increased scope of distributed generation, renewable energy systems and FACTS. Since most of the common failures (wire bond and solder fatigue) are caused by thermo-mechanical stresses, the methodology of lifetime estimation starts with temperature estimation, cycle counting based on rainflow algorithm, and finally degradation calculation based on linear accumulation model.

Different number of RC cells for each packaging layer in the module for the thermal model, including the influence of encapsulant is proposed for temperature estimation of IGBTs in power modules. A modified rainflow algorithm with faster execution time and time dependent temperature calculation is introduced for cycle counting. Finally, the lifetime of the IGBT is estimated during STATCOM operation using real-time load profiles for power factor variation. For a power factor variation data for a building, the lifetime is estimated to be about 3 years. Similarly, a month long arc furnace load data is considered to compare the equivalent temperature based calculation to conventional tests. 4% more degradation is observed in the equivalent temperature based calculation than compared with conventional rainflow algorithm.

A simulation study on the operation parameter dependence on the stresses in a wire is considered to estimate lifetime from Finite Element Analysis (FEA) in COMSOL. Power cycling tests are conducted on two different modules (600 V, 50 A H-bridge module and a 1200 V, 150 A phase leg module) to determine failures and degradation testing for four months. The low power module was tested without any protection circuits and hence failed catastrophically. Wire melt-off or fusing failure was dominantly observed, following by dielectric based short circuit failure. The high power module was tested with protection circuits to prevent catastrophic damage for a maximum of 3.5 months. A maximum of 20%

degradation in static characteristics, with decreased on state resistance was observed in the modules. The degradation is attributed to increased junction temperature as the thermal resistance increases owing to solder fatigue.

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CHAPTER I

INTRODUCTION

Estimation of reliability and lifetime of semiconductor devices is as old as the manufacturing of semiconductors itself. Reliability gives insight about the operational life of the system, maintaining the operating conditions within limits, and scheduling maintenance. Many standards such as Military standards, IEC, JEDEC, etc. have been established and are followed by the manufacturing industries [1][2]. Reliability of power electronics has gained importance with the European automotive initiatives for traction like LESIT (Leistungs Elektronik Systemtechnik und Informations Technologie), a Swiss government funded research program, and the German project, RAPSDRA (Reliability of Advanced Power Semiconductor Devices for Railway Traction Application) [3][4]. Many lifetime estimation models for semiconductors have been developed, initiated by the above mentioned projects.

The lifetime and reliability testing of power semiconductors individually is a mature technology. Standard tests are conducted at constant conditions for Metal oxide semiconductor field effect transistor (MOSFET) and bipolar junction transistor (BJT). But the lifetime of the system and in turn the lifetime of the semiconductor largely depends on the application it is being used for. Hence, it is important to develop methods to estimate reliability based on an application [5][6][8][9][10][11][12][14]. Applications that are considered in reliability calculations for Insulated Gate Bipolar Transistor (IGBT) are adjustable speed drives, matrix converters, electric vehicle applications, aerospace applications, inverters integration for photovoltaic (PV) and wind applications, etc. [5][6][8][9][10][11][12][14].

Reliability of FACTS (Flexible AC Transmission Systems) is an important factor in determining the stability of the power system. However, little research has been found in reliability of IGBTs and the power converters in (FACTS) Flexible AC Transmission Systems applications.

On-line condition monitoring methods to detect degradation in based on monitored parameters is gaining wide application. ABB's MACH sense-p/r system is one such example to condition monitoring of motors based on electrical parameters (current and voltage), vibration and torque readings that are analyzed and send a detailed report to the consumer through wireless data transfer [84]. Similar monitoring system is available for circuit breakers also.

The focus of this work is to estimate lifetime of semiconductors in STATic COMpensator, (STATCOM) application. STATCOM is a shunt connected FACTS device, consisting of a voltage source converter, and a coupling passive element to control the voltage and reactive power [13]. Reactive current compensation for the grid connected STATCOM is achieved by using non-active power compensation theory in this work.

The first step in lifetime estimation is root cause analysis, which is to identify the common failure mechanism and mode analysis in the inverter system. In an inverter, the most unreliable elements are power semiconductors and capacitors [11][14]. With significant research available in the area of capacitor reliability, there is a need to focus on the reliability of power semiconductor modules.

In Silicon (Si) based semiconductors, wafer level failures are least probable to occur due to mature manufacturing technology, if operated within ratings all the time. Packaging failures are the most common failures observed during operation of semiconductors in an application. The

packaging layers of a power semiconductor, their purpose, and the commonly used materials are listed in Table 1.1 and illustrated in Figure 1.1 [15]. Among the packaging layers, cracks in solder and wire bond liftoff, are the two most common failures due to thermal fatigue observed in various applications of power converter.

The methodology used for estimating reliability of semiconductors in power converters in this work consists of estimating the junction temperature, lifetime prediction method, and experimental verification by power cycle testing of the devices. A system overview is presented in Figure 1.2. The data from device characteristics and the operating condition values from the

Table 1.1 Components of power semiconductor packaging

	Packaging Layer	Function	Common materials
1	Base plate	Mechanical strength to insulating substrate Thermal conductivity Surface smoothness to avoid voids	Half hardened OFHC, Cu, Al, CuMoCu laminate etc.
2	Insulating substrate and metallization	Support circuitry Electrical insulation Thermal conductivity Smoothness for adhesion and spacing	Alumina, Aluminum nitride, SiC, SiO_2
3	Bonding Material	Electrical, thermal and mechanical linkage between insulating substrate, metal base-plate and semiconductor chips.	a) Organic Epoxy, Polyamide b)Metallurgical solder c) Silver filled glass
4	Terminal power interconnection	High current withstand capability Low cost and the absence of voids at the interconnection with power chips.	Al wires Gold wires Cu bus bars
5	Encapsulant	Protection of the power chip and wire assembly from chemical reactions due to moisture, chemicals etc. Insulate against high voltage levels.	Silicone gel, silicone, epoxy, Si_3N_4
6	Plastic case and cover	Protect the chip assembly from atmospheric reactions, Electrically insulate	standard packages: INT- A-PAK and double INT-A-PAK.

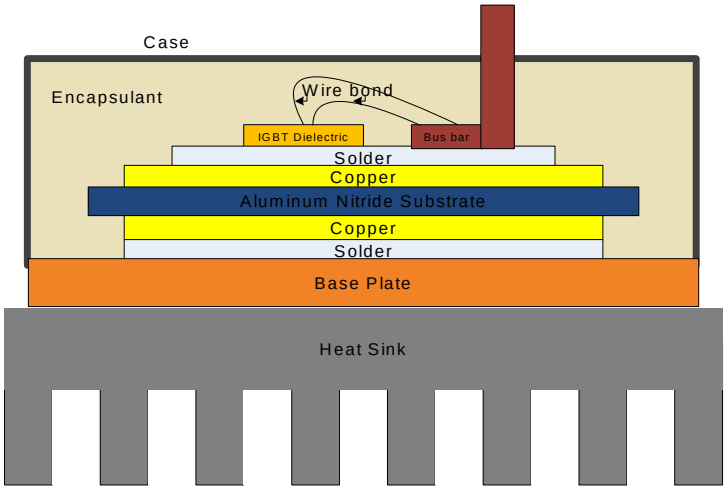


Figure 1.1. IGBT module components.

simulation model are input to the electro-thermal model. The power losses are calculated and the thermal model of the IGBT is used to estimate junction temperatures. The lifetime prediction model is developed from temperature profiles using rainflow algorithm and manufacturer's data for power cycling tests. Miner's rule of linear accumulation of degradation is used to estimate the lifetime for a mission profile. Finally, the power cycling tests are verified using accelerated lifetime testing experiments.

A thermal model development is proposed to overcome some of the drawbacks of existing models, discussed in Chapter 2, listed below

1) Unavailability of temperatures in each layer of package specifically in datasheet thermal models.
2) Thermal coupling in a multi-chip module (especially in Foster and Cauer networks)

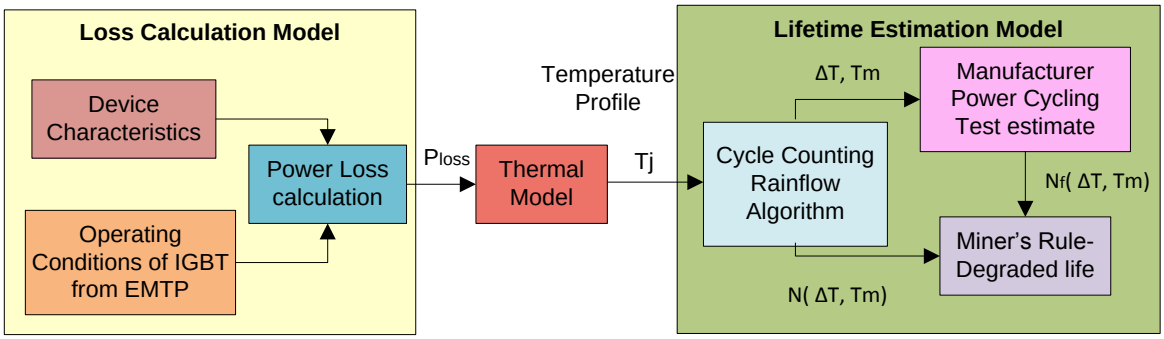


Figure 1.2. Block diagram of the steps involved in lifetime calculation of semiconductor.

3) Computationally exhaustive and time consuming (Finite Element based thermal modeling, Fourier thermal model)
4) Determining number of thermal (RC) time constants for each layer (Cauer network, Elmore technique, Multi-exponential models)
5) Use of same number of time constants for each layer.

The proposed model determines the optimum number of time constants and uses different number of time constants for each layer by using network identification techniques to estimate temperatures accurately, is explained in Chapter 3.

After obtaining the thermal response of different layers of the package, the next step is to estimate the lifetime of each chip. A model relating mean temperature and temperature swing to lifetime, also described as Coffin-Manson-Arrhenius model, is considered to estimate life in this work, for manufacturer's based power cycling data. Cycle counting methods are used to obtain the stress-strain hysteresis cycles for a time-varying load profile. Rainflow algorithm is the most

popular counting algorithm [12], and different approaches have been proposed in literature and will be discussed in Chapter 2. A new rainflow algorithm which is an extension of “Graphical” rainflow algorithm is presented in Chapter 3. A stress model dependent on the operating conditions such as current, voltage, frequency, etc., and the dimensions of the device is proposed as a universal model.

Finally, the lifetime estimation results are verified using power cycling tests. Power cycling tests are accelerated tests where the devices are switched so that the temperature in the device is similar to thermal cycling tests. Power cycling tests are preferred to thermal cycling, as they include switching and are closer to the actual operation of the device. These tests mainly cause wire bond failure while thermal cycles result in solder cracks. Power cycling experimental set up is discussed in Chapter 2. The simulation results for the proposed methods are presented in Chapter 4 while the experimental results are presented in Chapter 5.

1.1 Motivation

With the advent of Flexible AC Transmission Systems (FACTS), power electronics are integrated with power systems to improve stability, improve the transmission capacity within thermal limits, and avoid undesirable loading of certain transmission lines. Thus, FACTS technology ensures better coordinated control and improves system stability and security [17]. The more the power electronics are integrated to power systems in the form of distributed generation system, and FACTS, the more is the concern of their reliability affecting the system reliability. Better reliability of power electronics would further improve the scope of integration to power grid.

North American Electric Reliability Corporation (NERC), in its report on "Reliability Considerations from Integration of Smart Grid," has emphasized considering all the existing devices and systems such as Phasor Measuring Units, FACTS, etc., for assessing reliability of the bulk power system [18]. There is a need to study the individual reliability of these devices/systems to predict their impact on the grid.

Most applications considered for reliability studies have been for vehicular applications. Recently, renewable energy applications are gaining importance in reliability studies [5][6][8][9][10][11][12][14]. This research mainly focuses on the reliability of Insulated Gate Bipolar Transistor (IGBT) devices used in the STATCOM application.

For lifetime estimation of the semiconductors, the various important steps are thermal model development, cycle counting methods, and lifetime models. As most of the failures are caused by thermal fatigue, it is necessary to develop thermal model that estimates temperatures in different layers and materials of the module accurately, less time consuming and computationally exhaustive. Hence, there is a need to develop an accurate simple thermal model.

The temperature excursions estimated are used to obtain the fatigue stress-strain cycles using rainflow algorithm. The conventional rainflow algorithm used in semiconductor lifetime estimation does not consider time dependence of temperature on its cycle information. There is need to consider the equivalent temperature in semiconductor lifetime estimation using rainflow algorithm.

The lifetime estimation models, for solder fatigue and wirebond failures, based on physics of failure have gained technical importance in recent times. There is a need to develop a generalized lifetime estimation model based on the operating parameters of IGBTs.

Finally, power cycling tests are the accelerated tests conducted to detect weaker links, validate the lifetime models for the device under test, and to test and compare new packaging materials with that of conventional methods. DC power cycling tests use a simple circuit and are extensively used in testing reliability. Tests conducted should be analyzed to detect failure mechanisms.

This work is motivated to develop methods and models to overcome the problems associated with accurate lifetime estimation of power semiconductor devices.

1.2 Contributions

The main contributions of this work are listed below

1) Studied the stresses in wirebonds in an IGBT module based on finite element analysis, that is dependent on the operating electrical parameters such as voltage, current, and frequency, and the physical dimensions of the module.
2) Developed new rainflow counting algorithms improving the execution times of existing methods.
3) Applied time-dependent temperature calculation in rainflow algorithm to semiconductor lifetime estimation.
4) Developed different RC cells based thermal model for each layer in the semiconductor module with encapsulant.

1.3 Dissertation Outline

Chapter 1: Introduction

The process of predicting reliability or remaining life involves thermal analysis and application of temperature data to lifetime models. A basic introduction to thermal models of semiconductors and the lifetime is discussed. The motivation of this dissertation is presented to give an understanding about its scope and contribution of the project.

Chapter 2: Literature Review

A literature review of the various methods used in compact thermal models is presented. Estimating the RC thermal networks from deconvolution methods and frequency analysis is analyzed. The need for counting algorithms is discussed in detail. The various counting algorithms and their drawbacks are discussed. The original rainflow algorithm is presented. A literature review on the various lifetime prediction models used for power semiconductors are discussed. The existing lifetime models are discussed. A literature review on various power cycling methods are studied, and a power cycling circuit for testing is chosen for this application.

Chapter 3: Proposed Methods to Improve Lifetime Prediction Models

Lifetime Prediction using different number of RC cells based thermal model, modified Graphical Rainflow algorithm, and the stresses in wirebond due to operation parameters are presented. The RC networks of the thermal model incorporating the impacts of encapsulant to represent the semiconductor is presented. A modified rainflow algorithm for lifetime prediction that overcomes the shortcomings of graphical rainflow method is proposed and explained. Finally, a study on the stresses in wirebonds on operating conditions and design parameters of the module is presented.

Chapter 4: Simulation Results

The results include IGBT related temperature and lifetime simulations for STATCOM operation under power factor correction and harmonic compensation. The results of lifetime prediction of IGBT for a sample load profile using rain flow algorithm are presented.

Chapter 5: Experimental Results

The experimental verification of the thermal model is presented and the accuracy of the model is discussed. The experimental set up of a STATCOM and its loading is discussed. The temperature profiles for power factor correction and harmonic compensation in a STATCOM are experimentally obtained and compared with the simulation results. Power cycling test set up and the failures observed during the tests are presented.

Chapter 6: Conclusion and Future Work

A summary of the proposed methods and their impact on lifetime calculation are discussed in this chapter. Future work to enhance the performance of the proposed methods and overcome some of the drawbacks will be presented.

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

The lifetime of semiconductor materials is based on the stress it can withstand. In semiconductor applications, different thermal expansions of the materials in the package cause different amounts of strain, and since the materials are bonded in a package, these strains cause shearing stresses in the material. Thus, stress is indirectly dependent on temperature. By observing temperatures of the different layers in the package of a semiconductor, and applying lifetime estimation equations, the remaining life of the semiconductors for an application can be found. There is a need to understand the current state of research in reliability studies to be able to apply to the STATCOM application. This chapter presents a literature review of thermal modeling of semiconductor devices, lifetime estimation based on cycle counting, different rainflow algorithms, and power cycling methods.

2.2 Thermal Models

The conduction and switching power losses in the semiconductor devices generate heat in their components. Temperature is an important factor in estimating the lifetime of the inverter system. Temperature rise beyond the rated values will lead to more losses, due to the change in device characteristics with temperature, and will lead to thermal runaway. Thermal management of power converter systems involves heat sink design, and cooling methods (air, liquid).

Equation 2.1 describes the relation between power dissipated and the temperature of two layers of a module [19][21]

$$P = \frac{T_1 - T_2}{Z_{th}} \ , \tag{2.1}$$

where P is the power losses in the device,

T_1 and T_2 are the temperatures of the two layers, example case and ambient, of the device

Z_{th} is the thermal impedance of the device.

Thermal impedance is defined by thermal resistance and capacitance. Thermal resistance is the resistance of the material to heat flow, expressed in Kelvin/Watt. Thermal capacitance is the amount of heat required to bring about a unit change in temperature of a unit mass, expressed in Joules/Kelvin.

For conduction, thermal resistance: $R_{th} = \frac{l}{k \cdot A}$ (2.2)

where l is length, A is area of cross section, k is thermal conductivity

For convection, thermal resistance, $R_{th} = \frac{1}{h \cdot A}$ (2.3)

where h is thermal coefficient of convection

Thermal capacitance: $C_{th} = Q/(\Delta T)$ (2.4)

where Q is the heat energy dissipated, ΔT is the temperature difference.

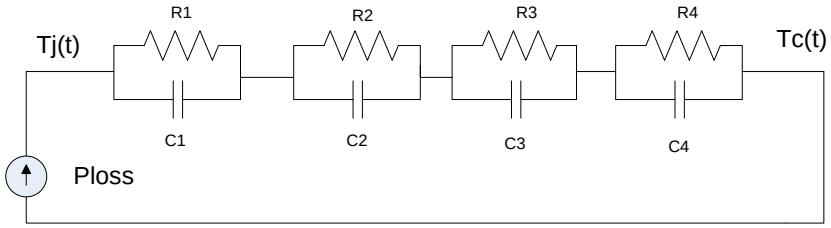
The Foster and Cauer networks are the simplest 1-dimensional RC thermal models. The Foster model, shown in Figure 2.1(a) is the most typical and easiest thermal model to obtain. It is commonly found in manufacturer datasheets. The Cauer model, shown in Figure 2.1(b), is based on the physical properties of the device.

In the Foster model, the individual RC elements do not represent the layer sequence. It is restricted to the specific application given in the datasheets and cannot be extended easily.

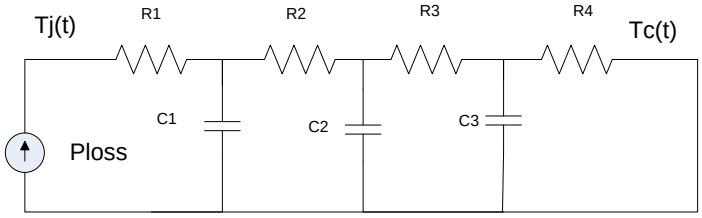
Deriving Foster network: From the thermal impedance curve, usually provided in the datasheet, a curve fit of three to four RC circuits is estimated to curve fit the thermal impedance curve. Thus, Foster network describes the thermal impedance of the whole device, and the individual points in the module cannot be considered [21]. The choice of number of RC circuits is not mentioned in literature, and it is basically a curve fitting model.

2.2.1 Deriving Cauer Network from IGBT Module Dimensions:

Cauer network can be derived from experimental data or from the dimensions of the device. Each layer's thermal resistance and capacitance is found from its dimensions and thermal



(a)



(b)

Figure 2.1. Two commonly used thermal models: (a) Foster Network and (b) Cauer Network.

properties as shown in equations (2.2) through (2.4). Thermal model reduction from the 7-layer RC model to 3 layer RC model is described by Mussalam et al [23].

Cauer network allows adding of further layers by series connection to the model. The Cauer network nodes allow access to internal temperature of the layer sequence [21]. Another difference between Foster and Cauer models is that while the Foster network's node-to-node heat capacitances are not suitable for representing heat flow [19][21], the Cauer network includes only node-to-ground capacitances, and it represents a discretized image of the real heat-flow [19][21][24].

Cauer networks mostly approximate the thermal response of each layer to a corresponding RC network. However, for an accurate model of the thermal network, a network of 2 or more RC circuits is required. Foster and Cauer networks are interchangeable and with the knowledge of one of the networks, the other network can be derived.

Thermal Response Extraction: The thermal dynamic behavior of the device can be obtained from the thermal impedance response from experimental measurements, or physical simulation of the device using 3-D solvers based on finite element, finite differences, etc. While noise is a major concern for experimental measurement of responses, accuracy is a concern for physical simulations. The next section describes the different methods of temperature measurement.

2.2.2 Temperature Measurement

Thermocouple measurement, infrared microscopy and the thermal sensitive electrical parameter (TSP) are commonly used methods to detect junction temperature [20]. Thermocouples require surface contact, but can be as small as 0.25 mm in diameter. They have a response time of about 10 ms, but bad thermal contacts can significantly affect the performance.

Despite this, thermocouples are the most popular of the direct techniques [19]. Optical fibers with phosphor sensors have response times of around 25 ms and can take measurements through the silicone gel, leaving the chip environment virtually unaltered [19]. Infrared microscopy can only be used to detect the unpackaged devices. Thus, to detect junction temperature of IGBTs, the package should be unsealed.

Temperature sensitive parameter (TSP) is defined as an electrical parameter of a semiconductor device that varies directly with junction temperature in an almost linear fashion. The common TSPs are the gate-cathode threshold voltage, on state collector-emitter voltage drop, and collector current [20][22][23][24][25][25]. Table 2.1 describes the temperature sensitive parameters commonly used for several semiconductor devices [20].

The junction temperature estimation using TSP consists of two processes, where one is off-line characterization of the IGBT under test and the other is on-line estimation of junction temperature, based on the characterized data [26]. There is a wide range of the time-constants playing a role in the total thermal time response. Since temperature changes may occur in the

Table 2.1. Common temperature sensitive parameters used for semiconductors.

Temperature sensitive parameter	Semiconductor device
Diode forward voltage, V_f	Diodes, BJT, MOSFET, Thyristor
Saturation voltage, V_{ce_sat}	BJT,IGBT
Gate turn-on Threshold, V_{th}	MOSFET,IGBT
Collector current	BJT, IGBT
dv/dt	IGBT

first 10-100 μs after the power onset and the final stabilization of the increased temperature requires 5-30 min or even more, depending on the mass of the package, the temperature responses are always plotted in logarithmic time scale [29].

Network Identification methods: Some of the early methods calculated the two to three time-constants from thermal response using the geometric and physical data of the device structure. These methods are usually approximate and involve an intuitive effort in realizing the number of time-constants.

Simple Analytical Thermal Method [35] **:**

If the thermal impedance is *Z(t)*

$$Z(t) = \sum_{i=1}^{N} (Z_i - Z_{i-1}) v(t - t_i) \tag{2.5}$$

where $v(t-t_i)$ is the step function at $t=t_i$

The Laplace transform gives

$$Z(s) = \sum_{i=1}^{N} (Z_i - Z_{i-1}) e^{-st_i} \tag{2.6}$$

$$\mathrm{Re}[Z(\omega)] = \sum_{i=1}^{N} (Z_i - Z_{i-1}) \cos\left(\frac{\omega}{2}(t_i + t_{i-1})\right) \times \frac{\sin\frac{\omega}{2}(t_i - t_{i-1})}{\frac{\omega}{2}(t_i - t_{i-1})} \tag{2.7}$$

$$\mathrm{Im}[Z(\omega)] = \sum_{i=1}^{N} (Z_i - Z_{i-1}) \sin\left(\frac{\omega}{2}(t_i + t_{i-1})\right) \times \frac{\sin\frac{\omega}{2}(t_i - t_{i-1})}{\frac{\omega}{2}(t_i - t_{i-1})} \tag{2.8}$$

By back substitution from the time responses at different times, the thermal network is derived.

Network Identification Methods by Deconvolution (NID) by Szekeley [29][30] [31]

Let the response be approximated by sum of exponential terms,

$$a(t) = \sum_{i=1}^{N} a_i (1 - \exp(-t/\tau_i) \tag{2.9}$$

Let $R(z) = \lim_{\delta z \to 0} \frac{\text{magnitudes related to time constants between z and z} + \delta z}{\delta z}$

$$a(t) = \int_{-\infty}^{\infty} R(\zeta)(1 - \exp(-t/\exp(\zeta))d\zeta \tag{2.10}$$

Let $z = ln\ t$ (logarithmic of time) (2.11)

$$a(z) = \int_{-\infty}^{\infty} R(\zeta)(1 - \exp(-\exp(z - \zeta))d\zeta \tag{2.12}$$

This is convolution type integral equation for unknown *R(ζ)* function. By differentiating *a(z)*,

$$M_1 = \frac{d}{dz} a(z) = R(z) \otimes W(z) \tag{2.13}$$

where, *W(z)= exp(z-exp(z)*) and $\otimes$ is convolution operator.

Thus, by deconvolving the differential of the logarithmic time response by the fixed function, *W(z)*, the thermal network can be identified.

Elmore Delay Technique [5]:

In [5] by Ciappa et.al, a modified extraction method is developed. Most extraction methods use deconvolution method or multi-exponential fitting to calculate the thermal time constants. The Elmore technique assumes the IGBT module is a 1-dimensional thermal model as heat flows from top layer to lower layers. However, in the cases where the heat transfers laterally and the thermal interference laterally is significantly high, modified Elmore technique is used. In the

modified Elmore technique, the thermal impedance at each layer obtained from the step response of the Finite Element Modeling (FEM) model of IGBT is described as a first order approximation by two weighted exponentials, to estimate the temperature values close to FEM values described by (2.14).

$$Z_{thi} = \alpha_i R_i \left(1 - \exp(\frac{-t}{\alpha_i R_i C_{1i}})\right) + (1-\alpha_i) R_i \left(1 - \exp(\frac{-t}{(1-\alpha_i) R_i C_{2i}})\right) \tag{2.14}$$

The first time constant, τ_{1i}, R_i C_i is a short time constant (milliseconds) while τ_{2i}, $R_i C_{2i}$ is a long time constant(seconds) to approximate the asymptotic behavior of thermal impedance curve both described in (2.15).

$$\tau_{1i} = \int_0^\infty \left[1 - \frac{Z_{thi}(t)}{R_i}\right] dt \text{ and } \frac{1}{\tau_{2i}} = \frac{1}{R_i} \frac{d}{dt} \left(Z_{thi}(t)\right)_{t=\theta} \tag{2.15}$$

Thus, the thermal impedance can be represented by 2n parallel resistor-capacitance couples and written as

$$Z_{thi} = \sum_{j=1}^{2n} R_j \left(1 - \exp(\frac{-t}{\tau_j})\right) \tag{2.16}$$

The modified Elmore technique is made up of Foster networks used to represent each layer independently and enables thermo-mechanical and reliability investigations.

Disadvantages: For very high frequencies, >100 kHz, the Foster network and hence the modified Elmore technique fails to be accurate.

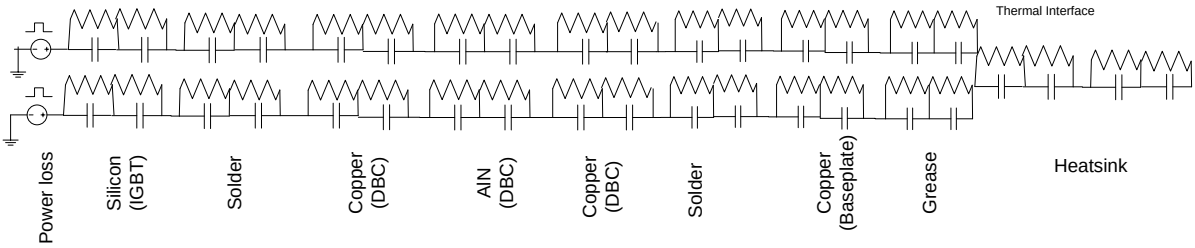


Figure 2.2. Modified Elmore technique applied to compact thermal model of two chips IGBT [3].

Real time based thermal models were also described in [24] by M. Mussalam and C.M. Johnson, using FEM. FEM models though accurate, are limited due to high computation time. Similar methodology as Ciappa's model is used but instead of modified Elmore's method with two RC circuits, multi-exponentials method with four RC circuits is used [5][6][24].

Nyquist Plot[34]: According to Kawka et al, an accurate curve fitting model can be obtained with the number of RC time constants, *n* being no more than 3. Fast Fourier Transform is used to calculate the transient response to particular power dissipation. First, the parameters from the clearly visible circles are determined for each circle. Time constants are obtained by applying ωt=1 in the points where *Imaginary part of [Zth(jω)]* reaches a minimum. "A", the chord of the circle, and α is extracted from the angle at which the center point is seen from the real axis. The curve fit is checked, if an extra circle with parameters tuned is needed for accuracy.

$$Z_{th} = \sum \frac{A_i}{(1 + jw\tau_i)^{1+\alpha_i}} \tag{2.17}$$

This method cannot be transformed as the impedance of an RC thermal network and hence for simulations in SPICE. Notice that the denominator of the thermal impedance function has a

power term (α) which makes it a non-linear expression. Time domain simulations based on the equations is possible.

Compact Thermal Models: Compact thermal models were developed to describe the thermal interference between different chips in a module. Network parameters are deployed using Deconvolution theory from Finite Element Methods (FEM). In [5][6], each layer is represented by two parallel RC networks in series as described by equation (2.10). The thermal impedance matrix and its relation to the temperatures and power dissipations are described in equation (2.18) [28].

$$Z_{thi} = R_1\left(1-\exp(\frac{t}{R_1C_1})\right) + R_2\left(1-\exp(\frac{t}{R_2C_2})\right) \tag{2.18}$$

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ T_{j3} \\ . \\ . \\ . \\ T_{jm} \end{bmatrix} = \begin{bmatrix} Z_{11}Z_{12}.....Z_m \\ Z_{21}Z_{22}.....Z_{2m} \\ ..... \\ . \\ . \\ . \\ Z_{m1}Z_{m2}.....Z_{mm} \end{bmatrix} \begin{bmatrix} P_j \\ P_2 \\ P_3 \\ . \\ . \\ . \\ P_m \end{bmatrix} \tag{2.19}$$

Measurement of temperatures for experimental verification is based on diode sensor.

Fourier based thermal model [32][33] is based on the solution of the heat equation in 2D as shown in (2.20). The solution to (2.20) is of the form shown in (2.21).

$$\alpha_i\left(\frac{d^2T_i(x,y,t)}{dx^2} + \frac{d^2T_i(x,y,t)}{dy^2}\right) + G_i'(x,y,t) = \frac{dT_i(x,y,t)}{dt} \qquad \text{for i=1, 2,..,m} \tag{2.20}$$

$$T(x,y,t) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} T_{mn}(t)\cos\frac{m\pi x}{W}\cos\frac{n\pi y}{L} \tag{2.21}$$

where x, y are the spatial terms, t is time, T_i is the temperature, α_i, G'_i are constants.

Finite Difference Thermal Model: Hefner Model: Reichl, Hefner et al [21]

Hefner model is developed from the thermal heat equations in 3D as described in (2.22).

$$A\rho c \frac{\partial T}{\partial t} = Ak \frac{\partial^2 T(z)}{\partial z^2} \tag{2.22}$$

where ρ is the density of the material with units g/cm^3 and c is the specific heat of the material with units J/gK.

It should be noted that the heat diffusion equation describes the temperature gradient in all three dimensions of the rectangular coordinate plane (x, y, and z).

Thermal Coupling Consideration: The thermal model is derived from the heat equation in 3D in Saber using MAST models. The assumption of y and x axis symmetry simplifies the equation to a one dimensional heat flow in the z direction and is simplified using finite Difference Method.

Chip thermal model: Includes heat source option, i.e. heat dissipated as a function of depth and assumes triangular or trapezoidal heat sources. A quasi-logarithmical grid of evenly spaced nodes (grid) within a segment, where the segment size increases logarithmically with distance from heat source, is used for simulation.

DBC/ base plate: Heat spreading laterally from the silicon chip is assumed to be at 45° and cannot spread laterally beyond the DBC or base plate as shown in Figure 2.3. The effective heat flow approach describes a heat flow area that increases with depth into the package. This is done by combining the components of heat flow area due to cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip.

Thermal coupling: A coupling resistor is placed between the case nodes of the top IGBT chip and diode. The case node is the bottom node of the DBC layer that connects to the base-plate layer. Another coupling resistor is placed between the case nodes of the top IGBT and bottom diode. Finally, a resistor is placed between the case nodes of the bottom IGBT chip and diode.

Another coupling network must be considered between DBC's since each DBC shares a common base-plate. A capacitance is considered between DBC layers and represents the heat capacitance not accounted for in the vertical thermal networks. All remaining volume is accounted for in the periphery nodes.

Disadvantages: The heat transfer at the edges is assumed to be at 45° C when it is supposed to be based on the ratio of their thermal conductivities.

Comparison:

Table 2.2 compares the various thermal models for complexity, accuracy, and multi-chip interfaces. Most of the models are based and curve-fit on FEM analysis in literature and hence complicated. The Elmore technique and multi-exponential methods use a finite number of RC components for all layers of semiconductor packaging.

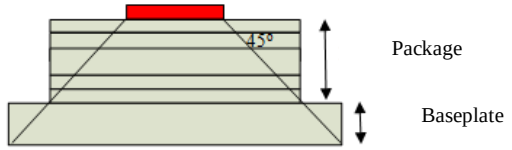


Figure 2.3. Spacing of the thermal nodes within package and base-plate model [21].

Table 2.2. Comparison of different thermal models from literature.

Thermal Method	Computation Complexity in analysis	Individual layer dimensions required	Accuracy (rank)	Experimental input	Multi-chip interface	Comments
Foster	Simplest	No	Universal Less accurate at high frequencies	No	No	Commonly used by manufacturers
Cauer	Less complex	Yes	Universal Accurate	No	No, Difficult 1D	Commonly used
FEM	Less complex, but time consuming			No	modeled	Large computation time and memory
Modified Elmore (Ciappa)[5]	Complex Less time consuming	Yes	Universal More accurate	Experimental validation at certain points	Modeled	Combines FEM and two RC parallel circuits
FEM+ Multi exponential [24]	Complex Less time consuming	Yes	Most accurate	Experimental validation at certain points only	Modeled	Combines FEM and RC parallel (usually 4) circuits.
Fourier(Santi et al)[32]	Complex	Yes	Universal.	No	Modeled	Thermal diffusion based, computation time high
Hefner's model	Complex	Yes	Accurate	No	Modeled	Finite difference method

Number of RC cells

Thermal models are an important factor in lifetime estimation of power semiconductors. Distributed thermal models are used to model the temperature distribution in different layers in the power module. Lumped models are used because of ease of modeling.

Ciappa et al proposed the Elmore technique based RC model to model the lateral distribution of heat using RC- models. Elmore based model uses two RC time constants, to model low frequency and high frequency components. Mussallam et al proposed the multi-exponential model for each layer, using four in their model. In [37], the number of RC cells in a thermal

model is shown to be dependent on the time-constant requirement. For example, for 2 ms time scale, 6 cells were used; 7 cells for 50 us; and 11 for 5 ns. The individual RC values are based on a size ratio that is determined by the user for accuracy. The reference [37] also shows that there are oscillations ("waviness") for a size ratio greater than 4:1. A detailed analysis of the model development was presented.

A new model reduction method was proposed by J. Antonios et al [36], showing the relation between the number of RC cells and the relative error in thermal model for each layer. According to their study, the lower the time constant, the less the number of RC cells required. However, the methodology in optimizing the RC cells was not clear, as their model used 400 RC cells for each layer to accurately model the temperature in an IGBT module. There is a need to systematically determine the number of RC cells in each layer in an IGBT model. Encapsulant is modeled in [38].

2.3 Lifetime Estimation: Stress-Strain Relationship to Lifetime and Rainflow Algorithm

The following section introduces the relationship between stress-strain and the number of cycles to failure. Each strain swing (rise and fall) of same amplitude causes a closed hysteresis loop and is considered as a cycle. The total degradation for a given load profile, is calculated by considering the cumulative effect of each hysteresis loop. In such a case, cycle counting is necessary in order to be able to obtain stresses and also count the number of hysteresis loops in a given profile. Rainflow algorithm is a popular counting algorithm used for semiconductor reliability estimation.

2.3.1 Introduction to Mechanical Stress-Strain

From the temperature profiles, the most common failures, wirebond lift-off and solder fatigue have to be modeled to estimate their respective lifetime and the IGBT lifetime. The stress on the metal (Al wires or solder) determines the degradation and the main cause of failure. Metals expand on heating, and the ratio of increase in length to the original length of the metal is known as strain. This strain causes a stress depending on the type of strain. For elastic strain, the stress and strain are related by Young's modulus. The strain due to thermal expansion is given by [39].

$$\gamma_i = c \times (T(i) - T_0) \times \Delta\alpha \tag{2.23}$$

where *T(i)* is the temperature increment, γ is the strain, $\Delta\alpha$ is the ratio of temperature coefficients between two layers and *c* is the constraint ratio, $c=1/(1-\upsilon)$, where υ is the Poisson ratio.

The strain in different layers of the module causes a shearing stress on the binding, and is given by stress-strain plots. The stress σ for elastic strain is given by

$$\frac{\sigma}{\Delta T} = \Delta\alpha \times E \times C \tag{2.24}$$

where *E* is the Young's modulus of elasticity.

The total strain is the sum of elastic strain, plastic strain and creep as given by (2.25). Plastic strain is the main cause of permanent damage and so most models describe the plastic strain.

$$\varepsilon_{tot} = \varepsilon_{elastic} + \varepsilon_{plastic} \tag{2.25}$$

Linear elastic strain: The portion of strain which can be recovered upon unloading, ε_e, shown in Figure 2.4.

Plastic strain: The portion of strain that cannot be recovered upon unloading ε_p, shown in Figure 2.4. The relation between plastic strain and stress is given by equation (2.26)

$$\varepsilon_p = \left(\frac{\sigma}{k}\right)^{1/n} \tag{2.26}$$

where K is the strength coefficient, n is the strain hardening exponent.

The strength coefficient is defined in terms of true stress at fracture, σ_f and true strain ε_f, as

$$K = \frac{\sigma_f}{\varepsilon_f^n} \tag{2.27}$$

Then plastic strain, $\varepsilon_p = \varepsilon_f \left(\frac{\sigma}{\sigma_f}\right)^{1/n}$ (2.28)

Thus the total strain, the sum of elastic and plastic strains, is given by

$$\varepsilon_t = \varepsilon_e + \varepsilon_p \tag{2.29}$$

Substituting equation (2.2) and equation (2.28) in (2.29), we get

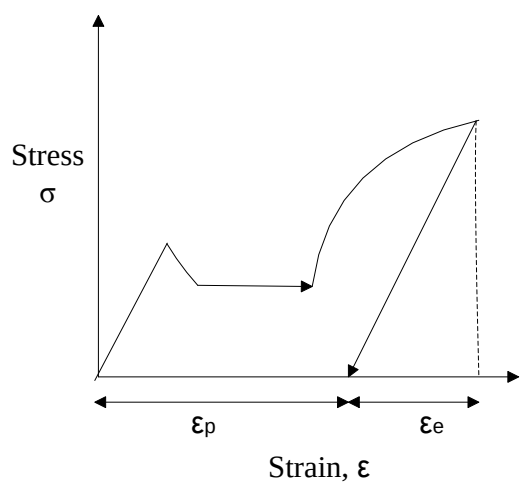


Figure 2.4. Stress-strain plot for plastic and elastic strain.

$$\varepsilon_t = \frac{\sigma}{E} + \varepsilon_f \left(\frac{\sigma}{\sigma_f} \right)^{1/n} \tag{2.30}$$

The lifetime prediction method would result in getting the stress from the stress-strain relationship after getting the strain based on temperature. For variable loads/stresses, most models assume linear accumulation of the cyclic fatigue especially for wire-bond reliability and Anand's model describes a non-linear accumulation [43].

For determining the lifetime, two different approaches are common, [39]

a) Stress-life model- Wohler: Empirical relation (power law) between stress and lifetime are estimates only. $N=10^{(-c/b)} S^{(1/b)}$ for $1000<N< 10^6$.

Disadvantage: This model cannot be used to estimate lifetimes below 1000 cycles. It does not account for plastic strain [39].

b) Strain-life model: For long lifetimes, where stress and strain are linearly related and plastic strain is negligible, stress-life and strain-life models are equivalent. For low cycle fatigue, i.e. high level loads, the cyclic stress-strain response and the material behavior are best modeled by strain-controlled conditions. Crack growth is not explicitly accounted. This model is commonly used in semiconductor lifetime prediction.

For strain-life approach, the material properties, the stress-strain history at the notch, cycle counting, mean stress effect incorporation and damage summation methods are needed.

Stress-Strain relationship: A cyclic inelastic loaded metal has stress-strain in the form of a hysteresis loop, as shown in Figure 2.5. The total width of the loop is $\Delta\varepsilon$ or the total strain range. The total height of the loop is $\Delta\sigma$ or the total stress range. The total strain in terms of amplitudes is given by (2.31) [39]

$$\frac{\Delta\varepsilon}{2} = \frac{\Delta\sigma}{2E} + \left(\frac{\sigma}{2K}\right)^{1/n} \tag{2.31}$$

The factor of 2 in equation (2.31), compared to that in equation (2.30), is due to the inclusion of reversal amplitudes.

For stress-life data, the relation between stress and the cycles to failure N_f is given by

$$\frac{\Delta\sigma}{2} = \sigma'_f (2N_f)^b \tag{2.32}$$

Coffin-Manson plastic strain-life model is

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon'_f (2N_f)^c \tag{2.33}$$

where coefficient, σ'_f, fatigue strength exponent, b, fatigue ductility coefficient, ε'_f, fatigue ductility exponent, c, and E is the modulus of elasticity. The first term accounts for elasticity while the second term accounts for plastic strain.

Thus, the total strain when written in term of cycles to failure N_f, is given by

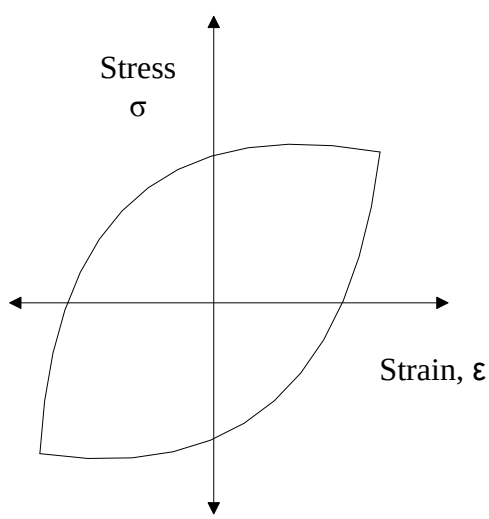


Figure 2.5. Hysteresis Stress-strain plot of a metal.

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma'_f}{E}(2N_f)^b + \varepsilon'_f(2N_f)^c \tag{2.34}$$

Equation (2.34) is the lifetime model based on first principles of physics of the materials and commonly used for solder fatigue.

2.3.2 Crack Growth Rate

For crack length *a*, cycles to failure *N*, and intensity factor *K*, Paris Law is the widely accepted model to describe the region with linear slope of log(*da/dN*) vs. log(*K*) and lies in between 10^{-6} and 10^{-3} in./cycle

$$\frac{da}{dN} = C(\Delta K)^m \tag{2.35}$$

$$N_f = \int_{a_i}^{a_f} \frac{da}{C(\Delta K)^m} \tag{2.36}$$

where a_i and a_f are the initial and final crack lengths, *K* is the stress intensity factor, a function of crack length.

2.3.3 Lifetime Models

The different popular analytical lifetime models used for semiconductors modules are described in Table 2.3 [46]. In this work, the Coffin-Manson-Arrhenius model developed by Held [4] et al is used to estimate lifetime from rainflow analysis of temperature data. Also note that all of these models are analytical models usually curve fit to experimental data or finite element analysis (FEA).

As discussed in Table 2.3, various lifetime models are available in the literature, of which Bayerer's model, based on the curve fit model, is the best lifetime model. It incorporates most of the parameters such as current, voltage, on time, and wirebond width, influencing lifetime for wirebond failure [53]. Most lifetime models are significantly dependent on temperature change, ΔT_j. [46]. C. Bailey and Hu developed a simplified basis function of dimensions of the wire in [50]. A damage based wear out model for wirebond interconnects was proposed by Yang et al [58]. Bayerer's model considers the wire bond diameter, voltage, current, on-time, and the

Table 2.3 Popular lifetime prediction models for various design parameters and variables.

Model Name	**Model for cycles to failure**	**Constants**	**Variables**
Coffin-Manson	$A\times\Delta T_j^{-n1}$	*A, n1*	Temperature swing (ΔT)
Coffin-Manson - Arrhenius	$A\times\Delta T_j^{-n1}\times e^{Ea/(k\times Tm)}$	*A, n, k,* E_a	ΔT, mean temperature, (T_m)
Norris-Landzberg model	$A\times f^{n2}\times\Delta T_j^{-n1}\times e^{Ea/(k\times Tm)}$	*A, n, n2, k,* E_a	ΔT, T_m, , frequency(f)
Bayerer's Model	$k\times\Delta T_j^{\beta 1}\times e^{\beta 2/(Tjmax+273)}\times(t_{on})^{\beta 3}\times I^{\beta 4}\times V^{\beta 5}\times D^{\beta 6}$	*k,β1,β2,β3,β4, β5, β6*	Maximum junction temperature (T_{jmax}), heating time(ton), applied DC current(I), diameter of the bond wire (D) and blocking voltage(V)
First principles model (Held)	$0.5\times[L\times\Delta\alpha\times\Delta T)/(\Upsilon\times\chi)]^{1/c}$	CTE mismatch between the two surfaces near solder joint ($\Delta\alpha$), fatigue exponent (c),	typical lateral size of the solder joint(L), thickness of the solder layer (x) and ductility factor of the solder (Υ)
Black's formula	$A\times I^2\times e^{Ea/(k\times Tm)}$	*A, k,* E_a	Current(I), T_m

junction temperature. The model is an empirical model curve fit to experimental field data where the failures can be attributed to multiple failure mechanisms, and cannot be extrapolated. The authors recommended not generalizing the model and extending it to other power modules [53]. There is a need to develop a generalized lifetime model specific to failure mechanisms that accounts for all the operating parameters in an application.

Most FEM based on thermo-mechanical physics of the materials in the package simulate the behavior of the materials under stress and are helpful in developing models. They involve considering fine meshes (hexagonal, tetrahedral, triangular, etc.) of nano to pico scale since the internal dimensions of the chip/dielectric (mm scale) are very small and have to be simulated for the whole volume of the module, a few centimeter scale. This results in computationally exhaustive and time-consuming simulations. Some of the simulations take as long as 4-5 days [32].

There have been models developed by Lu et al considering the solder fatigue as a function of the device dimensions [50][49]. Ning et al determined the reliability of various packaging materials as a function of the dimensions [51]. There is a need to develop a parameter dependent model incorporating the operating condition parameters, such as Bayerer's model[53], and the physical dimensions of the module [49] [50][51].

A stress model based on the physics of failure on the operating conditions and device parameters is proposed in Chapter 3.

2.4 Cycle Counting

The total width of the loop is $\Delta\varepsilon$ or the total strain range and the total height of the loop is $\Delta\sigma$ or the total stress range. This relation between stress and strain of materials is the basis of counting algorithms. To predict the life of a component subjected to a variable load history, it is necessary to reduce the complex history into a number of events which can be compared to the available constant amplitude test data. The process of reducing a complex load history into a number of constant amplitude events involves cycle counting.

2.4.1 Rainflow Algorithm

Rainflow algorithm is a cycle counting method which identifies closed hysteresis loops in the stress-strain response of a material subjected to cyclic loading. There have been many approaches to counting the cycles. Rainflow algorithm has gained popularity mainly because it provides the average value access [81] and has little relative error [12]. The analogy of rainflow counting first described by Matsuishi and Endo[71] is derived from the rain flowing (dripping) off the pagoda roofs.

The analogy of rainflow counting for a strain-time history is implemented such that the time axis is vertical and the strain-history forms the pagoda roofs. The following steps describe the methodology for rainflow counting, and Figure 2.6 shows supplemental figures for each rule described below. To eliminate the counting of half-cycles, the strain-time history is drawn to begin and end at the strain of greatest magnitude.

A flow of rain is begun at each strain reversal in the history and is allowed to continue to flow unless

a) The rain began at local maxima (peak) and falls opposite local maxima greater than that it came from, described by Figure 2.6(a).
b) The rain began at local minima (valley) and falls opposite local minima greater than that it came from, described by Figure 2.6(b).
c) It encounters a previous flow, described by Figure 2.6(c).

An example for the rain flow algorithm for a profile is described in Figure 2.7.

1) Flow starts at A, minima/valley.
2) The flow A-B falls on local maxima greater than itself, onto D.
3) Flow B-D is the greatest maxima and so the flow continues from D.
4) Flow B-C starting at peak B encounters peak D>B, hence ends (rule a). **(B-C is cycle)**
5) Flow C-D merges with previous flow from AB falling onto D (Rule c).
6) Flow D-E falls on to next minima, onto G.
7) Flow E-F encounters valley G<E and hence ends. **(E-F is cycle)**
8) Flow F-G merges with flow DE onto G.
9) Flow E-G flows onto next minima HI. Where the flow ends since it reached the final point I=A, **(A-D is cycle)**
10) Flow G-H ends as it encounters I<G. **(G-H is cycle)**

Most of the rainflow algorithms in the literature are based on range counting [72]. Instead of using points (peaks or valleys) for comparison, in range counting, two or more ranges are compared for cycle determination. Real-time based rainflow algorithms were developed by Downing [72], also known as three-point rainflow. ASTM standard was established based on Downing's rainflow algorithm [73]. Rychlik proposed a top-level up cycle counting method, which was similar to Downing’s algorithm [75] and Rychlik proved the equivalence of three-

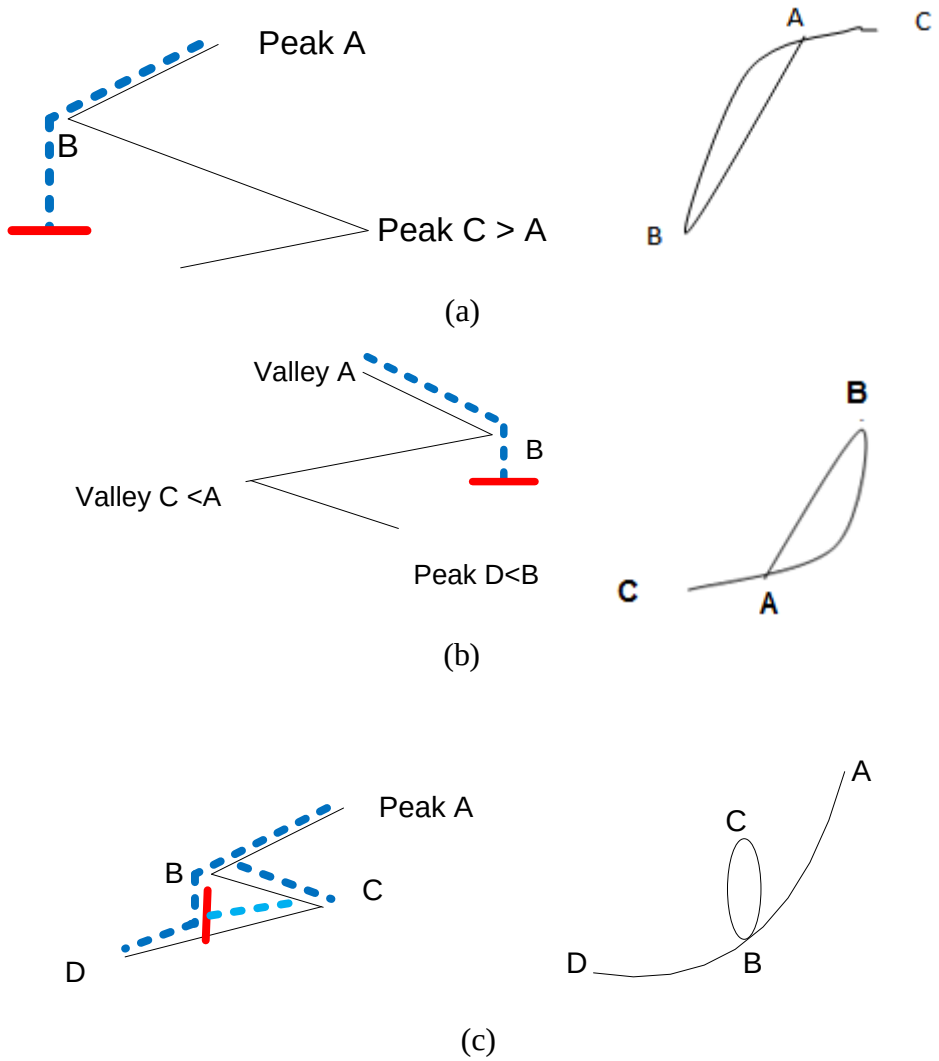


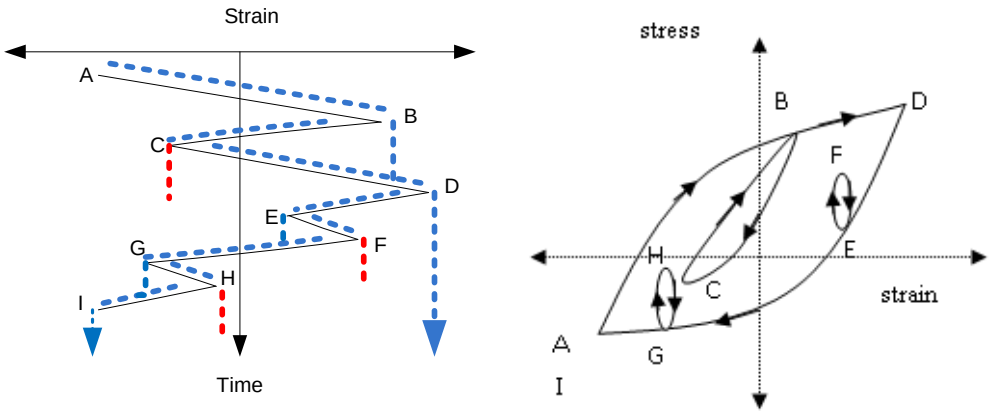
Figure 2.6. Rules for ending of flow in rainflow algorithm

(a) rain starting at peak, A, encounters greater peak, C,

(b) rain starting at valley, A, encounters lesser valley, C,

(c) rain flow starting at C towards D encounters previous flow from AB.

point (Downing) algorithm to the actual definition by Endo and Matsuishi [75]. Hong proposed the modified rainflow algorithm to include the full-cycle effect [76]. By the definition of rainflow algorithm, a sequence/range is not considered as a cycle unless it is closed in the hysteresis loop, even if it appears first in the load sequence. Anthes proposed a rainflow algorithm that counts based on the load sequence [77]. "Four point" valley method proposed by Amzallag et al, is equivalent to "three point" valley algorithm, but considers four points at a time rather than three [78]. It was proposed as a standardized rainflow after a consultation with industry [79] against the ASTM standard or three-point algorithm [72][73][74], and is simple in definition as compared to three-point algorithm. A graphical method was presented recently but for fixed data and not applied to real-time data [80].



(a) (b)

Figure 2.7. "Rainflow" on (a) a load sequence and (b) its stress-strain plot.

2.4.2 ASTM Standard (ASTM E1049-85) [73][74]

The following steps describe the three-point algorithm which is also the ASTM standard [73][74].

X-previous range; *Y* present range; *S*-starting point

1) IF $Y>=X$;
   a) if *X* does not have *S*; *X* is a cycle, discard points that make *X*.
   b) Else if *X* has *S*, *X* is half cycle, move *S* to next point, go to next point
2) Else, $Y<X$; go to next point

2.4.3 Four Point Algorithm [79]

1) Calculate three ranges, $S1=||A(i)-A(i+1)||$, $S2=||A(i+1)-A(i+2)||$, $S3=||A(i+2)-A(i+3)||$
2) If $S2<S1$ & $S2<S3$, cycle formed $S2$, discard points in $S2$, $i=i-1$, go to 1)
3) Else $i=i+1$, Go to 1)

2.4.4 Graphical Rainflow [80]

Graphical method of rainflow is based on some observations from previous rainflow algorithms. As the name suggests, in mathematics, graphical method of solving considers the area "graphically" that best solves the equations. It is well known that the highest "rain flow" cycle is between the highest peak and the lowest valley. This algorithm is based on finding the maxima and minima in a load profile and aimed at working towards individual smaller cycles within the biggest cycle.

1) Check if current point, $A(i)$, is peak or valley. If peak, go to 2), else (valley) go to 5).

2) Find the next peak, $A(m)>A(i)$. If m exists and $m-i>3$, go to 3) else increment position to the next point, $i=i+1$ and go to step 1).
3) Between $A(i)$ and $A(m)$, find the lowest valley $A(v)$.
4) Cycle between A(i) and A(v). Increment position to the next point, $i=i+1$ and go to step 1).
5) Find the next valley, $A(n)<A(i)$. If n exists and $n-i>3$, go to 3), else increment position to the next point, $i=i+1$ and go to step 1).
6) Between $A(i)$ and $A(n)$, find the highest peak $A(p)$
7) Cycle between $A(i)$ and $A(p)$. Increment position to the next point, $i=i+1$ and go to step 1).

The methodology of graphical method is more complex than three-point algorithm or four point algorithm. Graphical method of rainflow algorithm proposed in [79] has many disadvantages and are listed below:

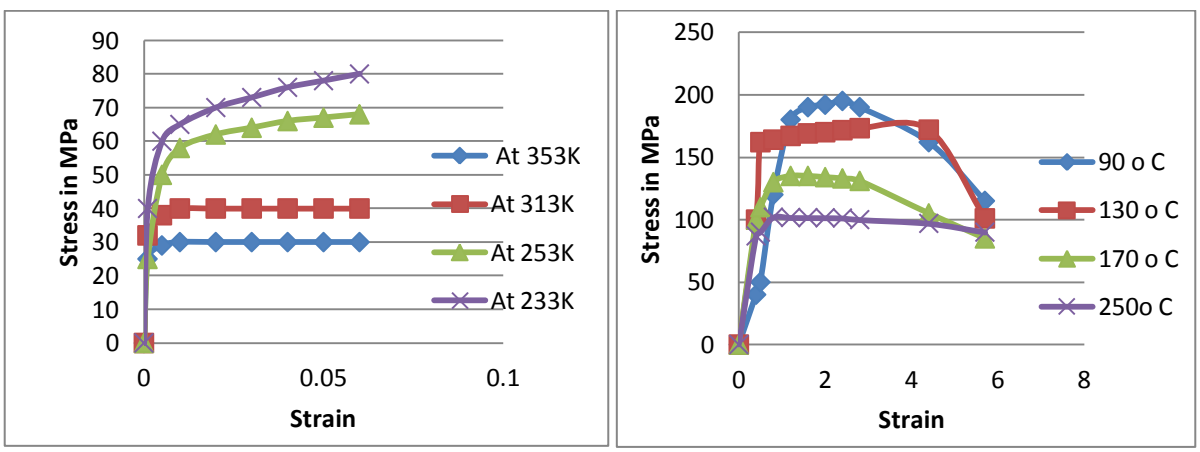
1) It is applicable for fixed data and does not generate the same results as the three-point or four point algorithm.
2) Half-cycles are not considered.
3) The data is not real-time and is fixed. The data should start and end with same strain profile.

The first disadvantage is a major concern in the algorithm itself, as it does not generate the same results as the standard or the four-point algorithm. It cannot be easily extended to real-time data. A new rainflow algorithm based on graphical method of rainflow is proposed in Chapter 3 to overcome the disadvantages of graphical method of rainflow.

2.4.5 Application to Equivalent Temperature-Time Dependent Fatigue Model

The lifetime of a material is dependent on the stress it can withstand. The stress-strain graph of a material is also dependent on the temperature at which it is operating. In other words, the change in temperature (ΔT) causes strain in the materials while the operating temperature or mean temperature affects the stress-strain plot. Figure 2.8 is a plot of stress-strain variation of lead-free solder and Aluminum wire bond at different temperatures [44][45]. As the operating temperature increases, the stress that the solder can withstand decreases. Hence, the mean temperature plays an important role in the lifetime of solder. Similar characteristics are observed with most materials. Rainflow algorithm stores the mean stress of a cycle, amplitude of a cycle, and the number of cycles with same amplitude and mean stress (histogram), after determining if a hysteresis cycle is closed.

Marko Nagode [82] proposed an online model for temperature dependent fatigue calculation



(a) (b)

Figure 2.8. Stress-strain graph variations with temperature of (a) solder [44] and (b) Aluminum for wire bonds [45].

based on the Clormann-Seeger cycle counting and damage estimation for variable temperatures. The algorithm is based on equivalent temperature calculation and recalculation and does not take creep and other effects into account, but it enables quick and improved fatigue life estimates.

The equivalent temperature of a closed loop for 4-point algorithm starting at S_{i+1} reaching S_{i+2} and arriving back at S_{i+1} is calculated as

$$T_{ei} = \begin{cases} \max(T_{ei+1}, T_{ei+2}) & T_{ei+1} > T_t, or, T_{ei+2} > T \\ \dfrac{t_{i+2} - t_{i+1}}{t_p - t_{i+1}} T_{ei+1} + \dfrac{t_p - t_{i+2}}{t_p - t_{i+1}} T_{ei+2} & otherwise \end{cases} \tag{2.37}$$

t_p is the time at which the half cycle is closed, as described by Figure 2.9.

$$t_p = \frac{S_{i+1} - S_{i+2}}{S_{i+3} - S_{i+2}} \left(t_{i+3} - t_{i+2}\right) + t_{i+2} \tag{2.38}$$

Equivalent temperature calculation is preferred over the mean temperature calculation as it

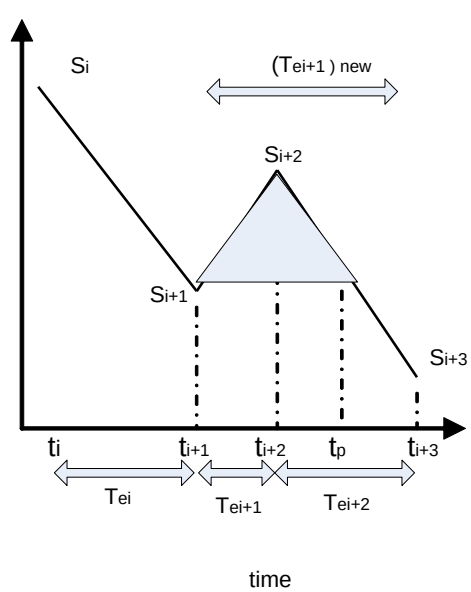


Figure 2.9. Rainflow cycle extraction and equivalent temperature recalculation.

considers the dependence of time and temperature on the lifetime. For example, the equivalent temperature of a cycle whose time period is long is higher than that with shorter time period. Usually the input matrix contains stress or strain information only. For equivalent temperature method, the matrix includes time, stress or strain, temperature at that point and equivalent temperature.

2.5 Power Cycling Tests

Power cycling and temperature cycling are the two most common thermal acceleration tests used in assessing reliability. During power cycling tests, the power to the devices is switched (on and off) so that the temperature in the device would vary (cycle). Power cycling tests are preferred to thermal cycling, as they include switching and are closer to actual operation of the device. For this reason, power cycling tests can be referred to as “Active” cycling tests while temperature cycling can be referred to as “Passive” cycling tests. These two cycling methods suffer from extremely long test times since millions of power cycles are expected in power applications. Acceleration of both methods by increasing temperature variation is controversial due to the activation of different material related mechanisms.

In this work, power cycling tests are considered in order to emulate tests with current conduction, specifically through wirebonds where the thermo-mechanical stresses are caused not only by the differences in thermal expansion coefficients of the different layers the wirebond connects(dielectric to drain copper DBC), but also by the thermal losses in the wires.

Some of the early power-cycling tests found in the literature were developed by the LESIT (LeistungsElektronik Systemtechnik und InformationsTechnologie) project. Power cycling

causes wire bond failure while thermal cycling result in solder cracks. According to references [52][81] fast power cycling leads to wire-bond failure while slow power cycling leads to solder fatigue related failures.

Manufacturers perform power cycling tests according to standards [1] to estimate reliability before releasing the product line to markets. However, the tests are usually done at constant duty cycles and test conditions for voltage and current different from operating conditions of the device in the application.

Military specifications are known for their standardization of test methods and procedures for military applications. However, no standards are available for IGBTs and so designers are forced to use procedures for MOSFET and bipolar transistors [47]. Similarly, Joint Electron Devices Engineering Council (JEDEC) standards JESD22-105C and JESD22-A122 are specified for power cycling of semiconductors. However they do not explain in detail about the dependence of operating conditions, failure criteria/ indicators etc. [1]. Hence there is a need to standardize procedures for power cycling with greater details.

Conducting power cycling tests at each and every operating point is tedious and time consuming. Power cycling tests can also be conducted to obtain the relationship between voltage, current and frequency on the lifetime of the semiconductors. In this chapter, the purpose, procedure, and choice of operating conditions for power cycling tests found in literature are discussed.

2.5.1 Design of Experiment: Planning Power Cycling Tests

The first step in planning power cycling tests is to determine the application of the power converter. For example, some applications need sine PWM, varying pulse width, and others need constant pulse width. The operating conditions (environmental, electrical, mechanical, etc.) have to be considered to be able to accelerate tests as near to operating conditions as possible. The packaging of the semiconductors plays an important role in determining the type of failures to be expected.

Press-pack semiconductors, used for very high power applications, do not have wire bonds, and the failure mode would commonly be caused due to solder joints and pressure contacts. Semiconductor device type, MOSFET, IGBT, diode etc., also determines the common failures. For example, a MOSFET predominantly has oxide related failures while IGBT has latch-up based failures.

The most common failure modes seen in semiconductors are listed in Table 2.4 [16][40]-[42]. Wire bond failures are the most common failures especially in IGBTs and have been the main focus of study in power cycling based tests.

Another important aspect seen in most power cycling tests is to test and compare the lifetime of semiconductors with new packaging materials and technologies. For example, a low temperature joining technique (LTJT) based on sintering of sub-micro silver flakes at temperatures 220°C and pressure of 40 MPA is presented in [63][68]. The melting point of lead free solder is 221° C while lead based solder are 178 ^{o}C. For ΔT=130 K, LTJT devices showed almost four fold higher lifetimes and at ΔT=200 K, almost 10 times improved lifetimes. Another example is [61] where Copper and AlSiC base plate based modules were tested and compared.

The copper base plate based module reached a temperature rise of 20% from initial value and failed. The lamination between substrate and base plate was observed. No failures were observed for AlSiC base plate module.

2.5.2 Parameter Monitoring for Failure Detection

Determining the parameters/indicators of failures to be monitored to ensure proper operation is an important aspect in design of experiments. This can be achieved with the knowledge of failure modes and the effect on various parameters in a circuit. Some of the common failure

Table 2.4. Common failure modes in semiconductors [16][42][40][40][42]

Failure Factor	**Failure Mode**
Diffused Junction Substrate	Decreased breakdown voltage Short circuit Increased leakage current
Gate oxide film Field oxide film	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or V_{th} drift
Die bonding : Chip-frame connection	Open circuit Short circuit Unstable/intermittent operation Increased thermal resistance
Wire bonding: Wire bonding connection Wire lead	Open circuit Short circuit Increased resistance
Input/output pin: Static electricity Surge Over voltage Over current	Open circuit Short circuit Increased leakage current
Passivation : Surface protection film Interlayer dielectric film	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or V_{th} drift Noise deterioration

indicators are temperature, collector-emitter voltage, gate threshold voltage, thermal impedance, collector current, gate current, and breakdown voltage. The choice of these parameters is based on their dependence on temperature. An indicator of solder cracks is thermal resistance R_{thj} while an indicator of wire-bond liftoff is collector-emitter voltage V_{cesat}. Failure modes are interdependent, and power cycling tests therefore require a careful failure analysis [48]. For example, an increase in R_{thj} results in increase in temperature T_{high}, and this will escalate the thermal stress for the bond wires. On the other hand, bond wire lift-off leads to increased V_{c}, which together with the constant current causes increasing losses and raises the upper junction temperature T_{high}, resulting in more thermal stress in solder layers.

The prospect of monitoring these parameters is discussed in [22]. Table 2.5 illustrates the common failure indicators and the percentage drift above which failure is considered to occur. The following section discusses important failure indicators.

Temperature: Since most of the failures are due to thermal impact, monitoring temperature would be a good indicator of failure. A failure is said to have happened when the temperature increases by at least 20% of its initial value for the same operating conditions. The failures that result from temperature increase are short circuit, hot carrier degradation, and thermal hotspot generation.

Voltage: The most common voltage measurements are collector-emitter voltage, gate threshold voltage, and breakdown voltage because they are dependent on temperature and also used as temperature sensing parameters. The collector-emitter saturation voltage is commonly used as TSP to obtain thermal impedance. 5% increase in V_{cesat} is considered to be an indicator of failure, usually wire-bond lift-off [22]. V_{cesat} monitoring during the operation of semiconductors in an

application is difficult and thus, monitoring is conducted off-line. In order to do so, the tests are either momentarily stopped or during the cooling cycle of the device under test (DUT) for measurement of V_{cesat}. The gate threshold voltage is also a TSP and an indicator of gate oxide based failures. A 20% decrease in gate threshold voltage is considered as failure criteria.

Breakdown voltage is also a TSP and indicates passivation based substrate failures. However, breakdown voltage as a failure indicator was not considered widely. The possible reason is that the measurement of breakdown voltage during power cycling operation is difficult because it involves circuit change, from a high current and low voltage circuit used for power cycling to a high voltage, low current circuit to measure breakdown voltage degradation.

Current: Collector current, gate current, and leakage current are the usual indicators of failure. Current measurement is more difficult than voltage measurement and hence is not commonly used. A 20% increase in the conducting current (collector current) is an indicator of thermal hotspot and short circuit failures. A 20% increase in the gate saturation current is an indicator of gate short circuit failure.

Table 2.5. Failure criteria expressed as a percentage increase in monitored DUT parameters [22].

Parameter	**% Degradation for failure**
$V_{ce(sat)}$	5%
$V_{GE(th)}$	20%
I_{on}	20%
T_j	20%
$I_{G(sat)}$	20%
Z_{th}	20%

2.5.3 Circuit Design

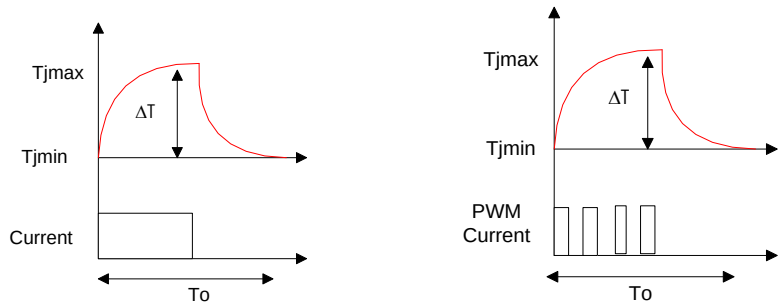
The main function of the power cycling circuit is to maintain current conduction through the semiconductors until the temperature increases to a maximum. Then the power is turned off until the temperature is decreased to minimum temperature. The power cycling circuits are classified as AC and DC circuits based on the current used for testing. Figure 2.10 demonstrates the waveforms of the current and temperature for DC and AC power cycling.

DC circuit [1]: A constant current for a continuous period of time is considered a DC circuit. The DC circuit is simple and easy for monitoring parameters.

AC circuit [1]: A PWM switching sequence for a time until the IGBT rises to a maximum temperature is applied and the device is turned off until it cools to a minimum temperature value. This circuit is usually preferred since it tests the device with the usual operating conditions.

The different circuits used in literature are briefly described below.

a) Inverter-inverter back to back [62]: Two three phase 800 kW identical inverters are arranged in a 'back to back' form with inductors joining the three phases for traction application, as



(a) (b)

Figure 2.10. (a) DC and (b) AC power cycling test concepts.

shown in Figure 2.11(d). With this arrangement, the system currents are made to circulate between the two inverters so that they each can operate to their full power of 800 kW. Only the losses are provided by the DC power supply. No failures were observed in the tests.

Advantages: Applicable to test semiconductors in three-phase inverter application.

Minimal energy input requirement. Only losses in devices are provided by power supply.

Disadvantage: Three phase control is complicated compared to single phase control.

b) Overload current [8]: A constant current at rated value for 20 s and an overload current of 1.5 pu of the motor for 5 s were used for power cycling a motor drive, as shown in Figure 2.11(e) to be able to accelerate the temperature variation and mean temperature within a short period of time. Failures were observed within 15 days.

Advantages: Failures are accelerated to 15 days.

c) Push-pull [3]: Two IGBT modules, rated at 1200 A and 3.2 kV were tested by Siemens in push-pull mode and the gate voltage was turned off after the collector current reached zero to avoid switching losses. The turn-off base plate temperature was maintained at 45°C. The temperature swing of the base plate was adjusted to ΔT_c = 50 K. For the temperature of the IGBT junction, this corresponds to a swing of ΔT_j=60 K and a maximum average value of T_j = 106 °C. A current of about 0.5 per unit, (600 A) is necessary to reach this swing. The ON-time and OFF-time were 50 seconds. Voltages and currents such as V_{CE}, I_C, as well as the base plate, and water temperatures were recorded. Copper and AlSiC base plate based modules were tested and compared. The copper base plate based module reached a temperature rise of 20% from initial value and failed. The lamination between substrate and base plate was observed. No failures were observed for AlSiC base plate module.

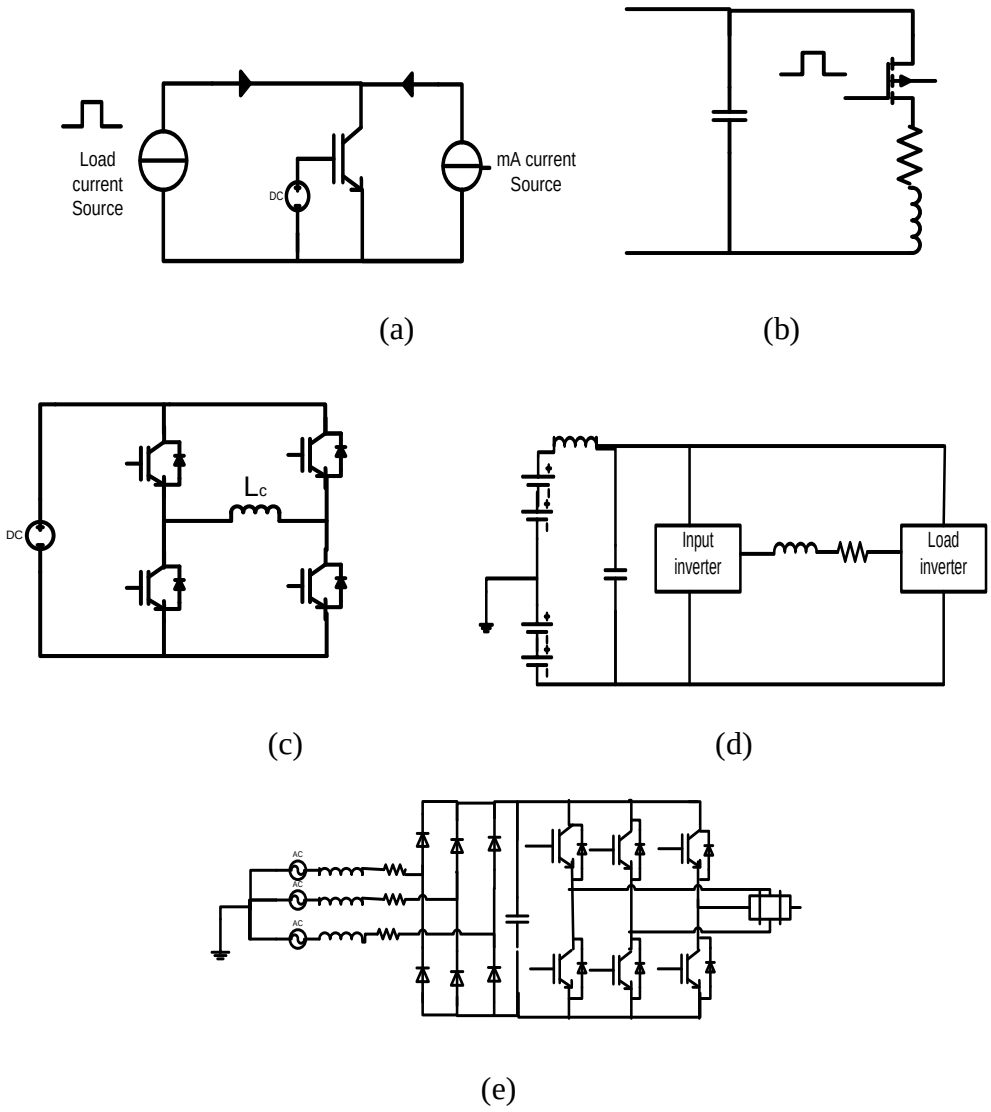


Figure 2.11. (a) Typical power cycling test circuit, (b) Avalanche breakdown testing circuit, (c) Single phase, full bridge with inductive load, (d) Three phase back-back inverters test circuit, (e) Synchronous motor drive test circuit.

Advantage: Single device is tested. The testing times and currents are reasonable. This circuit setup is best suited to test single devices in DC-DC converters.

d) Avalanche mode testing using inductive load on a single device switching is shown in Figure 2.11(b). The MOSFET rated at 180 A is tested at 33 V input voltage, rated at 20 V gate-source voltage, and on resistance of 4 mΩ. The indication of failure is 20% increase in thermal resistance [69].

   Advantage: Single device is tested. The testing times and currents are reasonable.

e) Pulsing current source [4]: A specified load current I_{load} is periodically applied to the IGBT whose gate is permanently set to a constant voltage, as shown in Figure 2.11(a). The gate voltage V_{GE} thereby must be set to a value significantly above the gate-emitter threshold voltage $V_{ge(th)}$ in order to assure a homogeneous current distribution among the IGBT cells in a chip and among paralleled chips. T_{jlow} and T_{jhigh} are the parameters to be set initially in power cycle tests by means of adjusting I_{load}, t_{on}, t_{off} and the cooling to appropriate values.

   V_{GE}= 15 V, current I_{load} between 240 and 300 A, t_{on} = 0.6 to 4.8 s, t_{off} between 0.4 and 5 s were the testing conditions in this test.

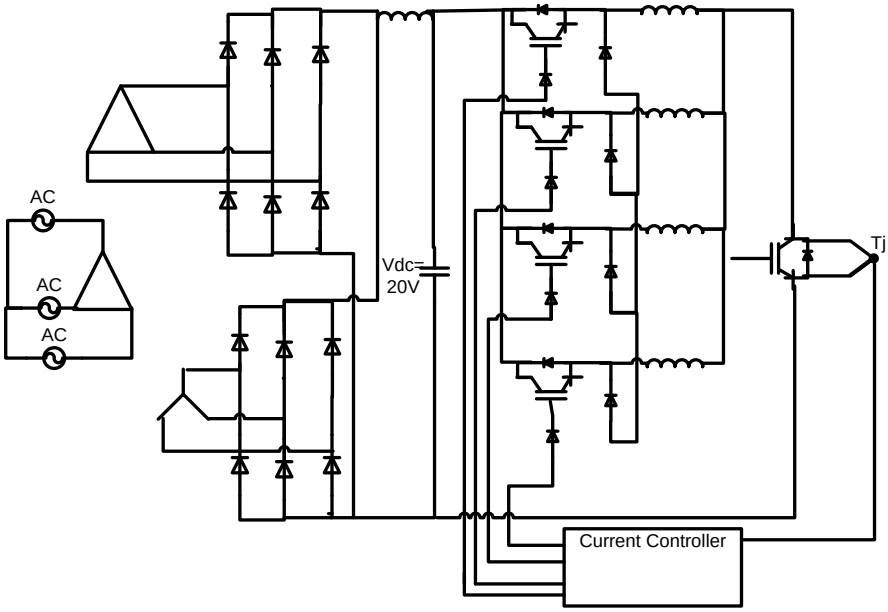
f) Half bridge inverter with inductive load [65]: High current and voltage rated devices are tested. The test is a destructive type of test, with inductive load and short circuit current through the device. The test consists of a 1-quadrant converter with 2 IGBT modules, a DC link capacitor and a load inductance with values typical for traction converter as shown in Figure 2.11(f). In this circuit, the high side IGBT is turned on for the current in the load inductance to increase. When the current source is switched off, the high side module fails. After failure, the path for the current to flow is through the diode of the low side module

resulting in high di/dt. The modules, with 24 IGBT chips and 8 diode chips, are rated at 1200 A, 2.5 kV devices. Both modules (low side and high side) showed similar damage. The top of the housing is broken, the gate unit is destroyed but no parts are ejected. The contact leads are bent.

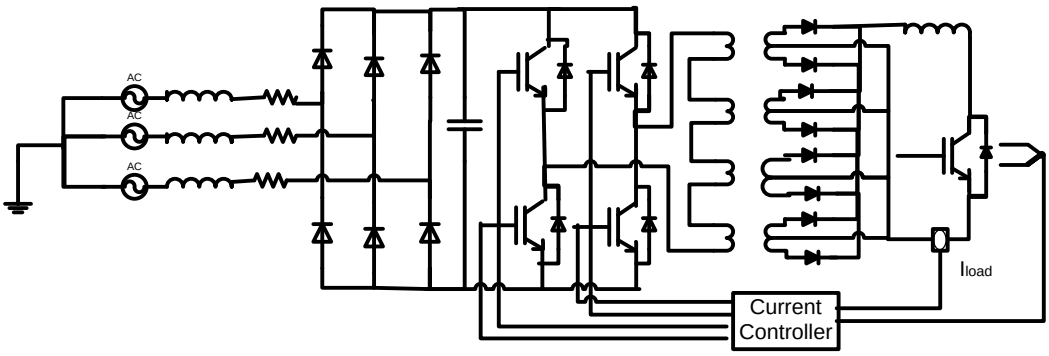
g) Full-bridge inverter with inductive load [70]: The full bridge inverter with inductive load, shown in Figure 2.11(c), has several advantages over other circuits. Inductive loads ensure the distribution of losses between diode and IGBT. Since the power is circulating between the phase legs, the input power required is minimal to supply for device losses only.

   Disadvantage: With purely inductive load, the time for which current is distributed between the diode and IGBT is equal. Hence the diode losses are higher in this circuit than that with resistive load or motor drive load.

h) Low frequency and high frequency topologies [67]: For solder layer degradation type of failure, long periods of temperature cycles of timescale of minutes, while wire-bond stresses are observed for shorter periods of temperature cycles. 3300 V, 1200 A IGBT with V_{ce}=3.8 V and 4.6 kW power dissipation at full power is tested using 3-phase power stepped down. High frequency transformer topology (topology 2) and low frequency topology (topology 1) are proposed. Low frequency topology consists of a 50 Hz, 12 pulse transformer, and rectifiers followed by a multi-phase buck converter with input voltage of 20 V. Due to low voltage, MOSFETs were used. At full load, each of the phases carries 300 A. 100 V, 1220 A MOSFETS from IXYS and diodes rated at 45 V, 400 A are used for converter and rectifier. The high frequency topology, topology 2, consists of a 3 phase rectifier followed by an isolated full bridge with input voltage of 600V. There are four secondary windings, i.e. each



(a)



(b)

Figure 2.12. (a) Low frequency and (b) high frequency topologies for power cycling [67].

phase carries 300 A at full load. 1700 V 400 A IGBTs for full-bridge, 800 V, 20 A diodes for rectifier and 400 A, 45 V diodes are used for secondary side of converter.

Topology 2 is more compact than topology 1 but transformer design is complicated. Topology 1 has the advantage of recovering as it has redundancy but topology 2 fails entirely even if one component fails. A current controller based on junction temperature control is implemented in both cases. To improve reliability, all components are derated to almost 50% to 65%. The MTBF calculated values are greater than 20 years. A prototype power cycling set up, based on boost/buck converter was developed.

2.5.4 Choice of Operating Conditions

Table 2.6 summarizes some of the power cycling tests in terms of their operating conditions, monitored parameters, test circuit, and duration of tests. The importance of operating conditions choice is discussed below based on the operating conditions found in literature.

a) Temperature: The choice of operating temperature plays a major role in the duration of power cycling tests. It is necessary to be able to have very high temperature swings in order to degrade and fail the device faster, and also operate within the ratings of the device. The lower limit on temperature is usually chosen to be around 40 ^{o}C to 50 ^{o}C. The maximum temperature is set between 100 to 150 ^{o}C.

b) Current: In most cases, the current is set to the rated value of the device. Sometimes, in order to accelerate the tests, the current is set to values greater than rated values [8][9]. However, since acceleration of parameters results in completely different failure mechanisms, it is not advisable to use values greater than rated.

c) Voltage: While the same principle of values less than rated applies to voltage condition too, since most of the testing circuits use inductive loads, the voltage is usually low, as low as 1/10 of the rated value.

d) Frequency: The switching frequency plays an important role in determining the severity of the tests for AC circuit based tests. At high switching frequencies, the switching losses are high and result in high dissipation losses, thereby increasing the operating temperature. The tests have to be started at high switching frequencies of at least 1 kHz.

   The frequency of the load or the output frequency also plays an important role in determining the time to failure. For low frequency of the load current, the temperature swing is high as the time for the temperature to rise and fall is also high. Output frequencies as low as 16 mHz were used for testing in literature.

e) Total duration of tests: The tests are required to run until failures are observed. However, some devices might not fail at all during testing. Hence a limit on the maximum test time is essential. From literature, it has been observed that the power cycling tests last from 10 days to 3.5 months. Devices that do not fail after 3.5 months of testing are considered robust and increased severity in the operating conditions is required to accelerate failure. Table 2.6 compares the different power cycling tests in literature and their results based on operating conditions, time to failure, type of failure and circuit.

2.6 Summary

The current state of research in thermal modeling of semiconductors, lifetime prediction, rainflow algorithm, and power cycling for reliability testing of power semiconductors is

presented in this chapter. A comparative analysis of the popular thermal models are compared and presented in Table 2.2. The relation between stress, strain and temperature is shown in section 2.3. The lifetime models found in literature are listed in Table 2.3. A detailed explanation of the working of conventional/original rainflow algorithm and the principle of the popular algorithms are presented in section 2.4. Power cycling test methodology and the most commonly used circuits for power cycling are described in section 2.5. Table 2.6 summarizes the different power cycling tests and tabulates the operating conditions, failure indicators used, temperature swings considered, and the time duration of tests.

Table 2.6. Comparison of different power cycling tests in literature [61-67].

Reference/ method	**Testing profile**	**Measure-ments**	**Cooling**	**Tempera-ture swing and T_{max}**	**Failures and indicators**	**Failure mechanism**	**Circuit**
Hamidi [59]	250 A for 0.9 s and off for 1.3 s	Junction temp. V_{ce}, I_c	Water cooled	$\Delta T=60K$ T_{jmax}=105-115 °C	V_{ce} increase at 400000 cycles	Wire-bond lift-off	Pulse
RCT[60]	500 A for 45 s and 2000 A for 5 s	V_{dc}, I_{ac}, IGBT temp.	Air cooled	ΔT=7K	No failures after 113522 cycles, 1491 hours		1 phase H bridge
High temp Power cycling[3]	200 A for 20 s, off for 40 s	Junction temp V_{ce}, I_c		ΔT=80 K T_{jmax}=150 °C	V_{ce} increase at 42800 and failure at 43,500 cycles	Gate leakage failure	3 phase inverter with current generator
Acc. test for traction [62]	Real-time current profile of traction used. 113 s period	Automatic temp. measure-ments,			No failures after 2200 hours		Two inverters joined by inductors, 800kW power, 60KW losses
High temp swing [63]	Half sinusoidal current by rectifier bridge, different current profiles used	V_{ce} and T_j		ΔT=100 to 150 K	Shown in table below		6 diodes tested

Results	ΔTj (°C)	Heating time	Cooling time	Load current	Failure cycles
PC1:Module 1	105	38	56	18	60k
PC2: Module 2	130	20	70	28	-
PC3: Module 3	155	28	85	32	-
Copper molded	110	21	84	28	3800

Thermo-electric cooling[64]	50 A in 12 s period to maintain 10 to 150 °C	IGBT Tempera-ture	Thermo electric coolers	ΔT=140 K	1427 cycles, 37 hours	Wire bond liftoff	1 phase inverter
Different temp. swings[65]	23 s heating and 5 s cooling cycle	V_{ce}, R_{th}	Water cooled	ΔT=80 K ΔT =110 K	85360 cycles at ΔT=80K 28900 cycles at 110K	Wire-bond liftoff	6 pack IGBT module,2 IGBTs in central H-bridge tested in series

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CHAPTER III

ESTIMATING RELIABILITY OF POWER SEMICONDUCTORS USING RC THERMAL MODEL, MODIFIED GRAPHICAL RAINFLOW ALGORITHM, AND WIREBOND STRESS MODEL

3.1 Introduction

In the first section, thermal model with encapsulant, based on frequency response of the thermal distribution is proposed to overcome some of the drawbacks of existing models, discussed in Chapter 2. The proposed model determines the optimum number of time constants and uses different number of time constants for each layer to estimate temperatures accurately. Encapsulant is usually not modeled in most thermal models. However, it has a delayed thermal response due to high thermal capacitance. The proposed model incorporates the RC model with encapsulant thermal characterization.

In the second section, a modified graphical rainflow algorithm is proposed for real-time continuous data to be used in cycle counting for lifetime estimation. The proposed method is compared with the existing algorithms for execution time and memory used. Finally, an operation parameter dependent wirebond stress model is presented.

3.2 RC Thermal Model with Encapsulation

As already mentioned, there is a need to develop an optimum RC based thermal model. In references [36][37], the number of RC cells in a thermal model is shown to be dependent on the

time-constant requirement. For example, for 2ms time scale, 6 cells were used, 7 cells for 50us and 11 for 5 ns.

Methodology:

The steps in determining the RC cells based thermal model are shown in Figure 3.1. In order to develop the thermal model, the temperature distribution of the device is first obtained from the thermal camera by powering the device with and without encapsulant. The temperature data is converted to frequency response, and the time constants of the device are obtained using frequency response.

3.2.1 Experimental Temperature Distribution

A 1200 V, 150 A, full-bridge power module, CM150DU, is the device under test (DUT). Two modules, one with encapsulant and the other without encapsulant, are considered. Thermocouples are placed between the baseplate and heatsink, under the dielectric area to monitor baseplate temperature. The collector emitter voltage is monitored. The temperature and voltage data is stored in a computer with the help of Keithley Data Acquisition System unit 2701. The power to the circuit is provided by 10 V, 100 A power supply. The dielectric's top layer temperature is measured by thermal camera SCI 620r.

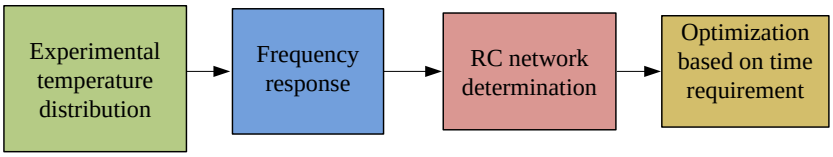


Figure 3.1. Steps in development of RC thermal model development.

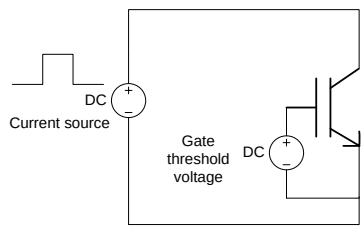


Figure 3.2. DC power cycling test circuit at gate threshold voltage.

The circuit used to test the device for thermal characteristics is shown in Figure 3.2. The device thermal responses are recorded for different power levels, different on-times, different current, and gate voltages. This data is used to estimate, validate and test the thermal model developed.

3.2.2 Frequency Response

The next step after obtaining the experimental thermal data is to obtain the frequency response. From the output temperature response and its input power response, the thermal response data is converted into transfer function represented by (3.1). Its zeroes and poles are estimated in MATLAB.

$$Z(s) = k \times \frac{(1+s/z_0)(1+s/z_1)(1+s/z_2)...(1+s/z_{n-1})}{(1+s/p_0)(1+s/p_1)(1+s/p_2)...(1+s/p_n)} \tag{3.1}$$

where $Z(s)$ is the thermal impedance function in frequency domain, z_0, z_1, $z_{2,\ldots}z_{n-1}$ are the zeroes of the impedance response and p_0, p_1, $p_{2,\ldots}p_n$ are the poles of the impedance function.

Equation (3.1) can be rearranged as

$$Z(s) = \sum_{i=1}^{n} \frac{R_i}{1 + s\tau_i} \tag{3.2}$$

where R_i is the thermal resistance of ith cell, τ_i is the time constant of the ith cell and $\tau_i = 1/p_i$.

The time constants can be estimated from the poles. The individual RC parameters can be estimated by the impedance equation in the form of (3.2). The fit to the exact number of poles is estimated by the least mean square error.

3.2.3 RC Network Determination

The optimization is dependent on the thermal characteristic properties and dimensions of the different materials in the module, and the time requirements of an application. Table 3.1 lists the different materials with their thermal properties and dimensions for the module CM150DU. A single RC based model is not accurate at different frequencies, while a multi-RC model greater than four causes oscillations in the output response [37]. The important factors affecting the number of RC cells in a layer are discussed below.

Table 3.1. IGBT module materials with their thermal properties and dimensions.

Layer	**Layer Material**	**Length (m)**	**Width (m)**	**Height (m)**	**Thermal conductivity (W/m.K)**	**Heat capacity (J/K)**	**Density (kg/m^3)**
Die	Silicon	1.63E-02	9.20E-03	3.0E-4	150	700	2.33E+3
Metallization	Aluminum	1.63E-02	9.20E-03	0.04E-4	230	900	2.70E+3
Die attach	Solder	1.63E-02	9.20E-03	0.4E-4	57	1500	9.00E+3
metallization	Ni-Ag	2.80E-02	23.2E-03	0.4E-4	400		
DBC top	Copper	2.80E-02	23.2E-03	3.0E-4	400	385	8.70E+3
Substrate	Alumina	3.36E-02	30.5E-03	5.0E-4	24	900	3.90E+3
DBC bottom	Copper	12.0E-02	65.0E-03	15E-4	400	385	8.70E+03
Diode	Silicon	1.63E-02	8.45E-03	3.0E-4	150	700	2.33E+03

The lowest time period of interest: The switching frequency and output frequency in an inverter are two important frequencies influencing the thermal characteristics. For dielectrics, metallization layers, and solder layers, the thermal time constant is very low owing to their small thickness (on the order of few μm). For such low time constants, the switching frequency is of significance, and frequency components (RC components) below that frequency have little effect on the thermal response of that material and can be ignored.

Relative error: The optimization is significantly dependent on the relative error allowed in the model estimates, without compromising on the accuracy significantly. In this work, we consider about 5 % relative error is taken as the maximum allowable error.

3.2.4 Example to Demonstrate Thermal Model Development

Consider the thermal response of an IGBT, given in Figure 3.3. The sampling time of the data is at 1 MHz. The transfer function in frequency domain is given by

$$Z(s) = \frac{-58239.0863\,(s+102)\,(s+0.2868)\,(s+1.77e-07)}{(s+5.792e04)\,(s+736.1)\,(s+51.45)\,(s+0.25)}$$

The time constants and the RC parameters are given by Table 3.2. The device's thermal model is represented by Figure 3.4. From the Table 3.2, it can be observed that the lowest time constant is of the order 10^{-5}. This model works efficiently for time scale requirements greater than 10 us. For example, if the time requirement is 2 ms, for accounting for 0.5 kHz of switching frequency, the time constant τ_1 has little influence on the thermal response. The resistance and capacitance of the new model is given by Table 3.3, shown in Figure 3.5. The first RC cell from the previous model is distributed to the second RC cell, in order to minimize the discarding of lower time constant.

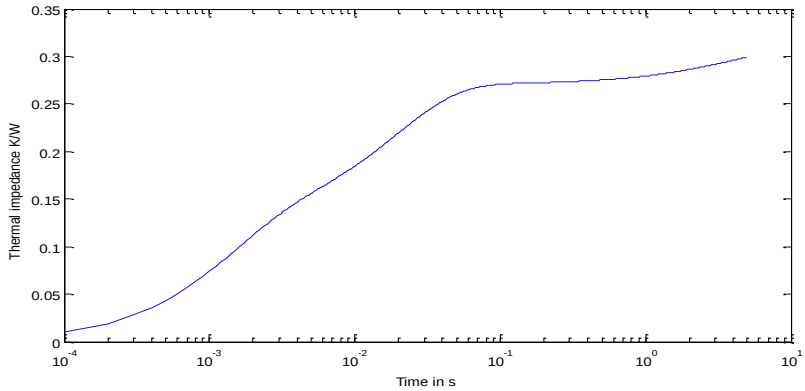


Figure 3.3. Thermal impedance of an IGBT module for 100 W power loss.

Table 3.2. Derived RC parameters from the frequency response.

	Thermal time-constant, τ (s)	Thermal resistance, R (K/Watt)	Thermal capacitance, C, (Joules/Kelvin)
τ_1	0.0000172	0.000384	0.05
τ_2	0.0014	0.107	0.0132
τ_3	0.0194	0.144	0.135
τ_4	4	0.04	100

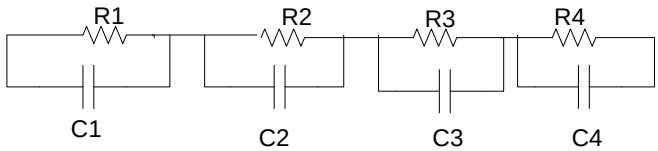


Figure 3.4. RC thermal network of the example temperature profile.

Table 3.3. Derived RC parameters from the frequency response after simplification.

	Thermal time-constant, τ(s)	Thermal resistance, R (K/Watt)	Thermal capacitance, C, (Joules/Kelvin)
τ_{1new}	0.0014	0.107384	0.0182
τ_{2new}	0.0194	0.144	0.135
τ_{3new}	4	0.04	100

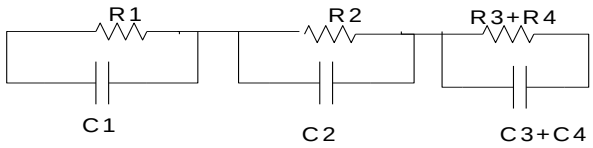


Figure 3.5. RC thermal network of the example temperature profile for a time scale of 2 ms.

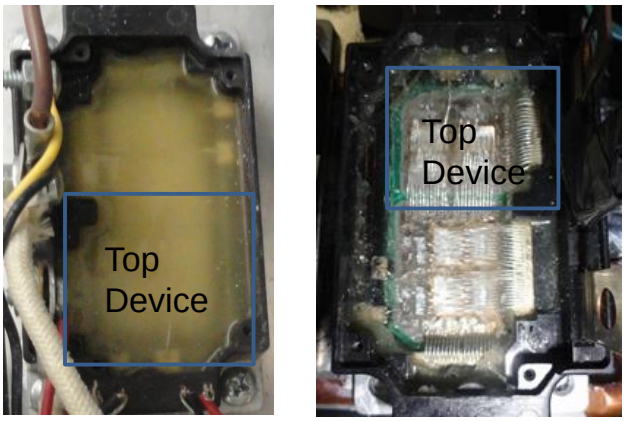
3.2.5 Encapsulant

Usually, RC models do not specifically model the layers above the dielectric that include the encapsulation and the case. Encapsulation plays an important role when considering the thermo-mechanical stresses in the module for fatigue. Encapsulant is filled as a potting material a) to provide mechanical support to the wirebonds, and b) to ensure even temperature distribution throughout the module. The encapsulant has a very high thermal resistance and so prevents the heat conduction in upward direction when the device dielectric is conducting and distributes the heat evenly when the dielectric is not conducting for some time and then eventually cools down.

In order to remove encapsulant, encapsulant from the one of the modules is manually removed. The usual procedure in removing encapsulant involves removal by chemical process using Methylene Chloride, which is a carcinogen [54]. In this work, encapsulant is removed layer by layer until the wires are encountered, and stopped at this point to avoid any physical forces on the wires. Thus, even though all of the encapsulant is not removed, most of the encapsulant is removed from the module, not straining the wires, as shown in Figure 3.6 (b). For simplicity, the module with less-encapsulant will be referred as module without encapsulant.

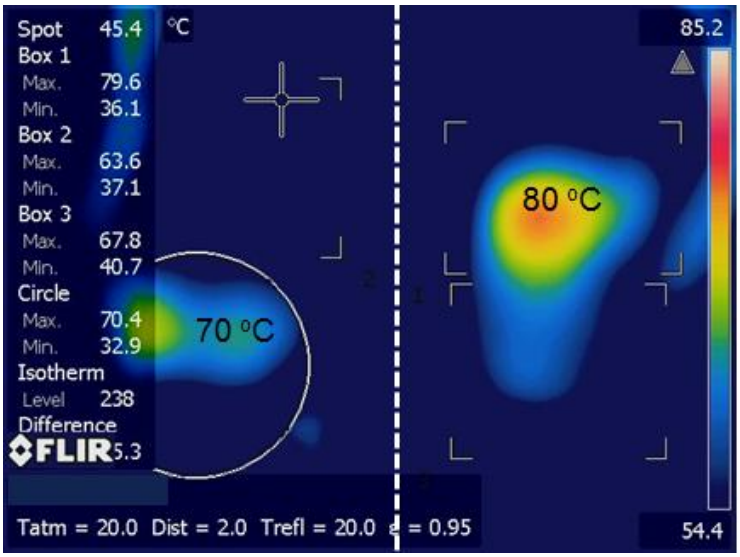
Figure 3.6 shows the two modules considered for comparison of thermal impact of encapsulant. The two modules (module 1 and module 2) are coated with black paint and connected in series such that the power terminals are facing towards the ends, i.e. module 2 is rotated by 180 ^{o}. Hence the top device of module 1 is on the lower end while the top device of module 2 is on the upper end of the figure.

Figure 3.7 shows the thermal image of the modules with encapsulant and without encapsulant when each of the devices is powered by 250 W for 80 s. The dielectric temperature is seen in the image for the module without the encapsulant, in Figure 3.7 (a) and is at a maximum temperature of 80 ^{o} C. The heat from the dielectric is equally distributed by the encapsulant and the top layer is at a temperature of 70 ^{o} C, as shown in Figure 3.7 (b). Since the thermal resistance and capacitance of the encapsulant is high, it takes a long time to heat up and cool down.



(a) (b)

Figure 3.6. Modules (a) with encapsulant and (b) without encapsulant are connected for testing the top device and obtaining thermal images with thermal camera.

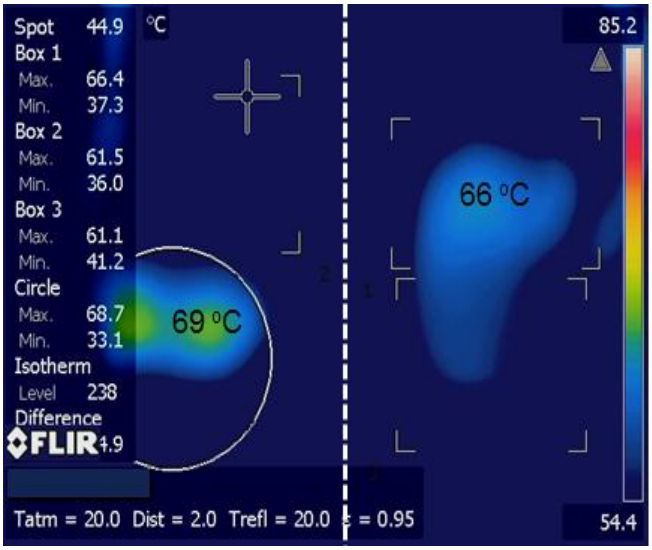


(a) (b)

Figure 3.7 Thermal image of power module CM150DU after 80 s of 250 W power of the module (a) with and (b) without encapsulant.

Figure 3.8 shows the thermal image of the module after the power was switched off to the two modules. Because of high thermal resistance, the encapsulant temperature does not decrease quickly. After 5 seconds, the encapsulant is still at 69 ^{o}C while the temperature of the dielectric with less encapsulant has decreased by 10 degrees the previous highest value.

Figure 3.9 plots the temperatures of the dielectric without encapsulant, dielectric with encapsulant and the encapsulant temperature as seen from this experiment. The dielectric temperature is slightly lower for the module with encapsulant as compared with that of the module without encapsulant because a part of the heat is used to heat the encapsulant, during current conduction. When there are no power losses in the device, the encapsulant is at higher temperature and so the dielectric is also maintained at the same temperature of the encapsulant.



(a) (b)

Figure 3.8. Thermal image of power module CM150DU after 5 s of power off (a) with encapsulant and (b) without encapsulant.

The encapsulant temperature is thus important to consider the overall thermal response of the module.

The RC network equivalent thermal model proposed by Bagnoli et al [38] can be modeled as shown in Figure 3.10. The switching power input denotes the heat source in the dielectric. During the non-conduction period, the encapsulant due to its high thermal time constant continues to increase its temperature. In this model, the encapsulant EVA is used that has a thermal resistance of 0.2 K/W, and a thermal capacitance of 0.5 J/K. This would impact the temperature of the wirebonds during the next conduction period.

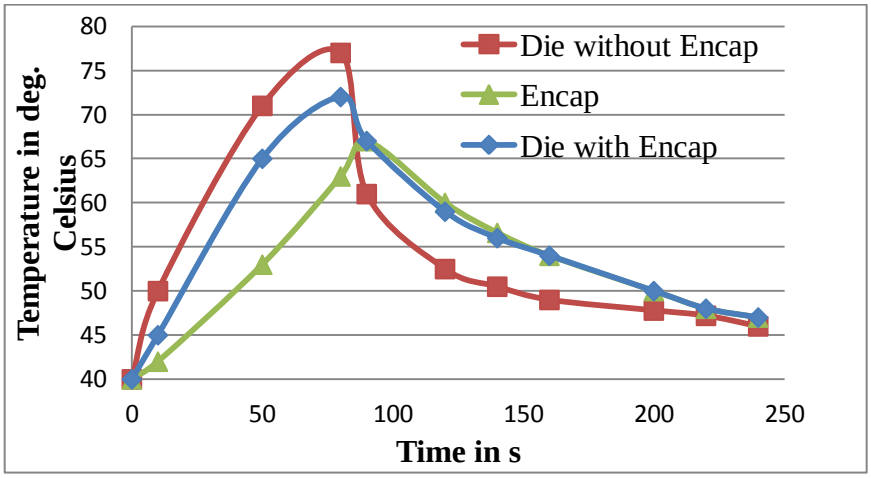


Figure 3.9. Temperature variation of the encapsulant (green) and the die with (blue) and without encapsulant(red).

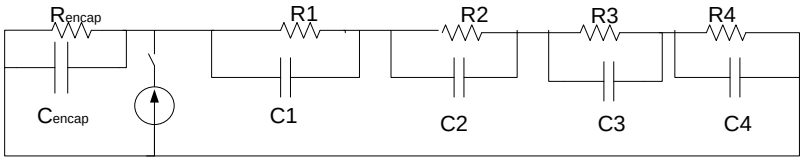


Figure 3.10. Thermal model of the IGBT from Figure 3.3 including the encapsulant, as proposed by [38] Bagnoli et al.

3.2.6 RC Cell Thermal Model of an IGBT

A detailed thermal model of the module for IGBTs, diodes and their coupling thermal impedances will be developed and used to estimate temperatures. The temperatures of different layers are recorded by IR images from a thermal camera. Figure 3.11 is a plot of temperature

with time of junction, substrate and case (baseplate) layers for a power loss of 160 W in the device.

Some materials in the package, base plate materials, with higher dimensions (directly related to mass), have high time constants and the lower frequency time constants can be neglected. For materials with smaller dimensions, ex. solder layer, the lower frequency time-constants play a significant role and a less number of RC time constant based models would best fit their thermal response. This leads to the idea of using different number of RC-networks for each layer are determined based on the time requirement. For a switching frequency of 10 kHz, the time scale of interest is of the order of 100 us. According to Table 3.1, since the dielectric has a time constant of the order of 200 us, would require two RC cells, to characterize the thermal response. Similarly, the minimum number of RC cells for each significant layer is developed. Figure 3.12 is the RC thermal model with different number of RC cells and includes the encapsulant thermal model. The encapsulant has very high thermal resistance and capacitance, and its time constant is

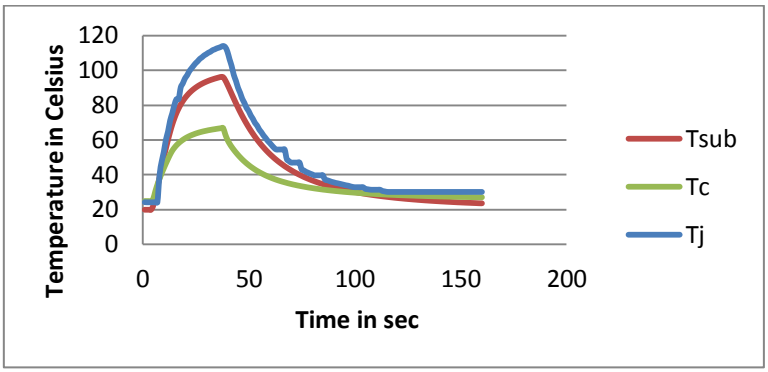


Figure 3.11. Temperatures of the junction, T_j,, substrate T_{sub}, and case, T_c, of the IGBT power module CM150DU for a power pulse of 160 W.

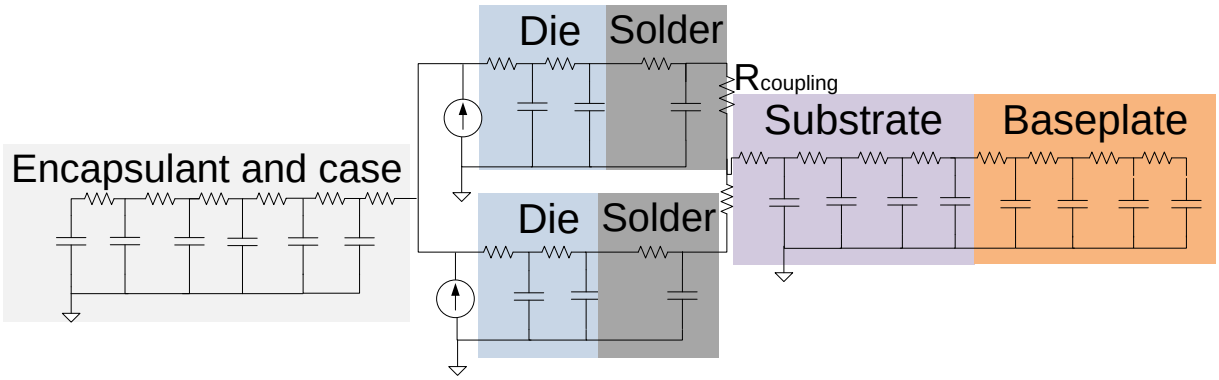


Figure 3.12. RC thermal model of the IGBT module with different number of RC cells and encapsulant thermal model.

very high and hence has the maximum number of RC cells. A systematic method to determine the optimal number of RC-components in each layer is proposed based on the thermal response. Cauer thermal network is used due to its advantages of better thermal distribution representation than Foster network.

The developed simulation model is then used to estimate temperatures of IGBT and diode for power factor correction in STATCOM.

3.3 Proposed Rainflow Methods

3.3.1 Fast Rainflow [88]

Instead of using ranges for cycle counting as in “four-point” [79], and ASTM standard [74], a fast rainflow algorithm based on points is described below. It offers similar accuracies and speeds as 4-point algorithm.

Let four points *A1, A2, A3, A4* be considered as strain load profile for explanation. The ranges are calculated as *s1=A1-A2, s2=A2-A3, s3=A3-A4*, shown in Figure 3.13. From the definition of four-point algorithm, a closed loop is formed if the range *s2* is smaller than range *s1* and *s3*, i.e. $s2 < s1$, $s2 < s3$. The range calculation is best suited when the stress data has positive and negative values. However, for positive values only, as is the case with temperature in semiconductor during operation, the peaks and valleys can be compared. Hence a cycle is formed if a) the current point is a peak, b) if next peak is greater than current peak, $A4 > A2$ and c) the valley before the current point is less than the valley after the current point, i.e., $A1 < A3$. Similarly, a cycle is formed if a) the current point is a valley, b) if the next valley is less than current valley, $A4 < A2$ and c) the peak before the current point is greater than the valley after the current point, i.e., $A1 > A3$.

The algorithm starts with reading the data and should start with at least two points. Let *i* represent the variable describing current position in data matrix *T*. The conditions for checking if

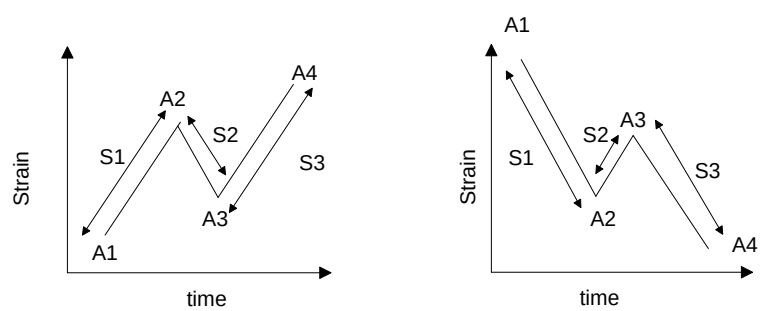


Figure 3.13. Points and ranges in (a) peak cycle formation, (b) valley cycle formation using four-point algorithm.

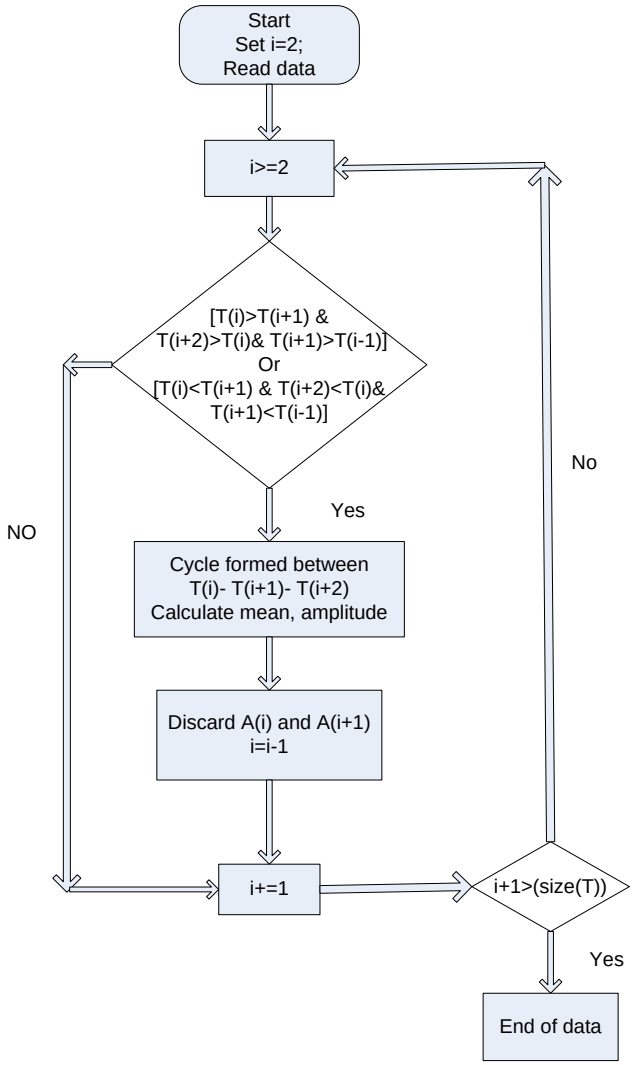


Figure 3.14. Flow chart demonstrating the steps involved in fast rainflow algorithm.

a closed loop is formed, for the current point being a peak or valley, are combined with a single "if" statement.

For real-time data, the cycle counting has to be point by point, no modification of the data should be necessary. Fast rainflow combines the advantages of the three-point and four point algorithms and compares data point-by point but does not calculate the ranges. This reduces the calculation time. The flowchart of the FR algorithm is shown in Figure 3.14.

3.3.2 Cycle Counting using Modified Graphical Rainflow Algorithm[88]

The graphical rainflow method (GRM) is modeled for a fixed data available before the application of the algorithm. The disadvantage of GRM is that it is not accurate in cycle counting especially when there are many loops inside another stress-strain loop.

Let us consider an example profile shown in Figure 3.15 to demonstrate steps involved with GRM. The data starts with a valley, *A1*, as shown in Figure 3.15. When a valley is encountered, the next minimum valley is searched, in Figure 3.15, $A3 < A1$. The points between *A1* and *A2* are less than 3, hence the next point is considered. *A2* is a peak. A peak which is greater than *A2* does not exist. Next point is *A3*, a valley. $A7 < A3$, the number of points between *A3* and *A7* is three.

So the next step is to find a peak greater than the peak after the current valley, in Figure 3.15, $A6 > A4$. A lowest valley between those two peaks is searched, *A5* in the example, and a cycle between the peak, *A4* and the minimum valley point *A4-A5-A6*, is counted. The next point *A4* has only one point between its next peak, *A6*, so *A5* is considered. The same rule applies to *A5* and the next points are considered. Thus the end of data is reached. The total number of cycle counts

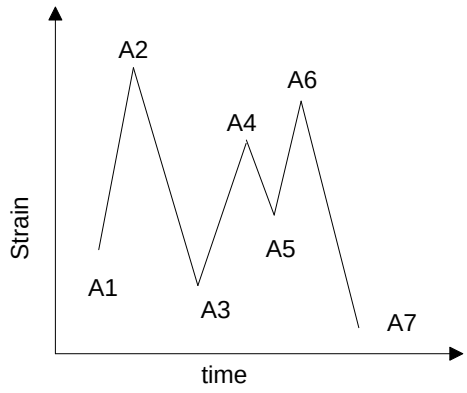


Figure 3.15. Example load profile to show shortcoming of graphical rainflow.

is one. However, according to four-point algorithm, *A3-A6- A7* is also a cycle. From the above discussion, it is clear that the GRM is not accurate. MGRM fixes this shortcoming of GRM.

For data matrix with temperature information, *T*, and the position described by *i*, i.e., *T(i)* represents the value of temperature/stress at point *i*. The following steps describe MGRM.

1) Check if current point, *T(i)*, is a valley or peak. If it is a valley, go to 2; else if it is a peak, go to step 4.

Valley:

2) If a valley, at position *m*, lower than current valley i.e., $T(m) < T(i)$, does not exist, increment *i*. Go to step 10.Else if $T(m) < T(i)$ exists, go to step 3.
3) Find the maximum peak position, *max1* between *T(m)* and *T(i)*. If there exists a value of *T* before the current position *i*, greater than *T(max1)*, then a cycle is formed between *T(i)* and *T(max1)*. Calculate amplitude and mean. Go to step 6.

Peak:

4) If a peak, at position *m*, greater than current peak i.e., $T(m) < T(i)$, does not exist, increment *i*. Go to step 10.

   Else if $T(m) < T(i)$ exists, go to 3.

5) Find the minimum valley position, *min1* between $T(m)$ and $T(i)$. If there exists a value of *T* before the current position *i*, greater than $T(min1)$, then a cycle is formed between $T(i)$ and $T(min1)$. Calculate amplitude and mean. Go to step 6.

Inner Loops:

6) Check the right hand side (RHS) of the cycle for inner cycles, i.e., if $max1-i > 1$ or $min1-i > 1$, there are inner loops, go to step 7. Else go to step 9.

   Similarly check for left hand side inner loops, i.e., if $m-max1 > 1$ or $m-min1 > 1$; inner loops present, go to step 8. Else go to step 9.

7) Right hand side (RHS): Between starting and ending positions $i+1$ and $max1/min1$, perform MGRM.

8) Left Hand Side (LHS): Between starting and ending positions, $max1+1/min1+1$ and *m*, perform MGRM.

9) $i = m$; go to step 10.

10) If *i* reaches end of data consider each range as a half cycle. Calculate mean and amplitude. Else go to step 1.

The difference between the MGRM and FR is that in FR, the process involves applying comparisons point by point while in MGRM, the process involves considering a group of points at a time. Also, load sequence in cycle counting is achieved in MGRM. The other main

difference is that MGRM is applicable for fixed data only and FR is applicable for real-time data. A comparison with other rainflow algorithms is discussed in the next section.

For real-time data, the cycle counting has to be point-by point and no modification of the data should be necessary. The modified graphical algorithm combines the advantages of the three-point and four point algorithms with that of the graphical algorithm. It compares peak data point-by-point maximum peak but does not calculate the ranges thereby reducing the calculation time.

Example to Demonstrate Modified Rainflow Algorithm

Rainflow algorithm can be applied only to peak and valley data that duplicates the pagoda roofs. The original data that is obtained for lifetime analysis in rainflow algorithms should be processed to generate only peaks and valleys. A MATLAB program to find peaks and valleys/troughs in data was programmed. After obtaining the peak-valley data, the data is analyzed for number of cycles using ASTM standard or the three-point rainflow algorithm, 4-point algorithm, graphical rainflow, and modified rainflow algorithms. The results from all the algorithms are expected to be the same since the main concept of rainflow algorithm should be preserved according to the definitions of cycle counting. In order to compare the algorithms for the same load profile, a randomly generated load profile in MATLAB is used. Figure 3.16 demonstrates the random generated profile using MATLAB with 24 extreme points (peaks and valleys) for which the proposed algorithm MGRM is shown to work in a step-by-step manner in Table 3.4. The amplitudes of the profile are named as *A1, A2, A3*.....*A24*, as shown in Figure 3.16. Variables *i, m, min1, max1* and the terms RHS, LHS are as described in the algorithm in

Table 3.4. Modified graphical rainflow algorithm steps for load profile in Figure 3.16.

Modified Graphical Rainflow Algorithm steps for load in Fig. A.1	**Cycle information**
i=1; A1 is valley; A3<A1; m=3; maximum between A1 and A3= A2; T(n<2) >A2 does not exist; i=i+1	
i=2, A2 is peak; no point greater than A(2), increment i	
i=3, A3 is valley; A7<A3, m=7; maximum value between A3 and A7 is A6, max1=6, and check if any value of T(n<3) >A6 exists, A2>A6, "CYCLE" RHS: max1-i>1, inner cycle, perform internal MGRM ini=4, A(inm=4:6)>A4, inm=6; minimum value between 4 and 6, A5, "CYCLE" LHS:m-max1=1, no inner cycle; increment i to m	A3-A6-A7 is a cycle A4-A5-A6 is cycle
i=7, A7 is valley ; no valley lower than A7; increment i	
i=8; A8 is peak; A10>A8, m=10; minimum value beween A8 and A10 is A9, min1=9; T(n<=8)<A9 exists, n=7; "CYCLE" no inner cycles; i=10	A8-A9-A10 is a cycle
i=10; A10 is peak; A16>A10, m=16; minimum between A10 and A16 is A13, min1=13; T(n<10)<A13 exists, n=7; "CYCLE" RHS: min1-i>1, inner cycle, perform internal MGRM ini=11,T(inm=10:13)<A11 is A13, inm=13; maximum value between A10 and A13 is A12; "CYCLE" ini=13, end RHS LHS: m-min1>1;ini=m+1; perform internal MGRM ini=14; T(14) is peak, A16>A14, inm=16; minimum value between A14 and A16 is A15; "Cycle" ,ini=inm ini=16, end LHS i=m;	A10-A13-A16 is a cycle A11-A12-A13 is a cycle A14-A15-A16 is a cycle
i=16; no point greater than A(16), increment i	
i=17; A19<A17; m=19; maximum value between A17 and A19=A18; max1=18; T(n<17)<A19 exists, n=13; "CYCLE" m-i=1, no inner cycles; i=m	A17-A18-A19 is a cycle
i=19; A21<A19;m=21; maximum value between A21 and A19=A20; max1=20; T(n<19)<A21 exists, n=13; "CYCLE" RHS: max1-i=1, no inner cycles; LHS: m-max1=1, no inner cycles; i=m	A19-A20-A21 is a cycle
i=21; no point lower than A(21), increment i	
i=22; A22 is peak ; A24>A22, m=24; minimum value beween A22 and A24 is A23, min1=23; A(n<=22)<A23 exists, n=21; "CYCLE" no inner cycles; i=23; end of data	A22-A23-A24 is a cycle

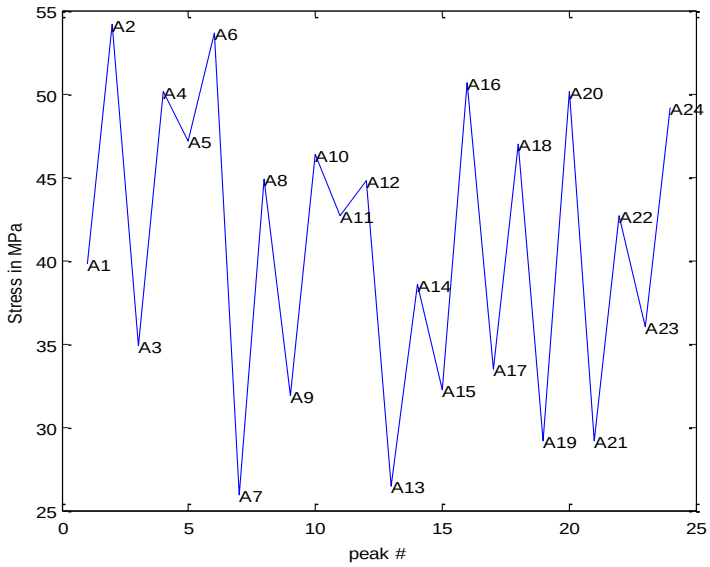


Figure 3.16. Random load waveform for explaining MGRM algorithm.

section 3.4. Variables *ini, inm* are used to describe variables *i and m*, in the inner loops in RHS and LHS.

3.3.3 Comparison with Other Rainflow Algorithm Approaches[87]

Rainflow Counting algorithms are one of the best counting methods. The new modified-graphical rainflow algorithm will be compared with a) ASTM standard, b) four point valley, c) graphical rainflow method (GRM), and d) fast rainflow algorithm as shown in Table 3.5. The comparison would give a better understanding of the drawbacks of the algorithms.

Real time Analysis:

The original rainflow algorithm was valid for a fixed data set. Real-time analysis using rainflow algorithm was considered and is an important property for rainflow algorithm. The

GRM and MGRM are developed for fixed data set and if used for real-time data, are very slow and complex.

Execution Time:

Execution time is the shortest for four-point algorithm and the fast rainflow algorithm. The execution time depends on the code of the execution. The MGRM and GRM algorithms have higher execution times due to the use of many functions to find minimum and maximum values. The three-point or ASTM standard has execution times higher than four-point algorithm.

Accuracy:

All the rainflow algorithms should count the same cycles since the principle of counting is the based on loop formation in stress-strain hysteresis plot. However, the GRM algorithm is not accurate when there are more loops within a stress-strain loop. The MGRM proposed in this paper addresses the drawbacks in GRM in this aspect.

Memory Usage:

In all of the rainflow algorithms, there is a need to store the data for unclosed stress-strain loops, i.e., half cycle information, and the closed loop information (range and mean). In GRM and MGRM, the analysis is based on comparing peaks and troughs separately. This requires more memory compared to other algorithms, as the information has to be passed to both peak and trough analysis.

Load Sequence:

By the definition of rainflow algorithm, a sequence/range is not considered as a cycle unless it is closed in the hysteresis loop, even if it appears first in the load sequence. Anthes first considered the load sequence in his algorithm [77]. The ASTM and four-point algorithms do not

follow load sequence, i.e., the cycles are counted only when half cycles are closed depending on the occurrence of closing ranges. The GRM and hence the MGRM algorithms are modeled to count cycles based on the load sequences. Load sequence plays an important role in damage during crack growth. The crack opening values depend strongly on the order of the load sequence [76].

Complexity:

The four-point algorithm, and hence the FR, are the simplest in terms of code implementation and concept. It involves less comparisons and conditions. The ASTM standard based on three-point algorithm is a little complex as it has conditions related to starting points. The GRM has more conditions than the ASTM standard. MGRM is the most complex of algorithms in implementation as its implementation is based on cycle counting of the inner loops.

Table 3.5. Rainflow algorithms comparison for execution time, memory usage, and load sequence efficiency [87].

Algorithm	Execution time	Memory used	Accuracy	Complexity	Load sequence	Real-time data
ASTM	1% higher than FR	Low	High	Less Complex	No	Yes
Fast Rainflow (FR)	Lowest	Low	High	Simplest	No	Yes
4-point	Low	Low	High	Simplest	No	Yes
Graphical	15% higher than FR	Low	Low	Complex	Yes	No
Modified Graphical (MGRM)	>20% higher than FR	Medium	High	Most complex	Yes	No

3.3.4 Example to Demonstrate the Equivalent Temperature Calculation in Conjunction with Rainflow Algorithm

Table 3.6 illustrates the difference in the mean calculations for the signal in Figure 3.17 for conventional and equivalent temperature based calculations. Four closed cycles are determined by the four-point algorithm criterion. The mean temperatures using conventional calculation method and equivalent temperature calculation are shown in the 6th and 9th columns of Table 3.6. It also displays the equivalent time values from the calculations. A difference in the mean temperature calculation can be observed for the second and third cycles where the mean temperatures by conventional calculation are 57.0^{o}C and 54.2^{o}C, while that by equivalent temperature method are 58.7^{o}C and 55.3^{o}C. Since lifetime is dependent on temperature

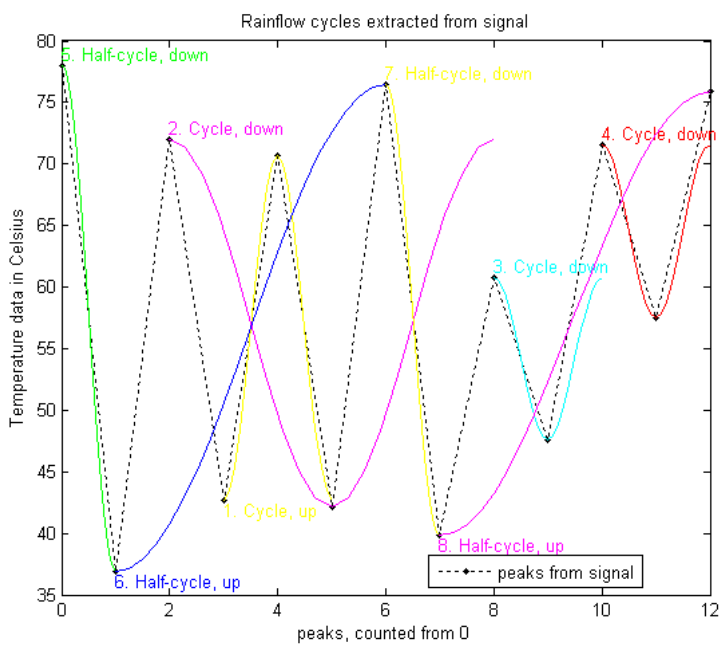


Figure 3.17. Rainflow algorithm of a signal with cycle's information from code available in MATLAB [83].

Table 3.6. A step by step analysis of rainflow algorithm with and without equivalent temperature calculation applied to the example profile in Figure 3.17.

Start and end extreme points	Points (Range) considered	Cycle formed using Four-point rainflow	Conventional rainflow			Equivalent temp calculation		
			Start and end times	Amplitude	Mean temp	Equiv. start and end times	Ampli-tude	Mean Temp
1-2	77.96-36.93	-	3-9	-	-	3-9	-	-
2-3	36.93-72.03	No	9-18	-	-	9-18	-	-
3-4	72.03-42.71	No	18-21	-	-	18-21	-	-
4-5	42.7-70.7	Yes	21-24	28	56.7	21-24	28	56.58
3-6	72.04-42.17	Yes	18-27	29.87	57.10	18-21.05	29.87	58.7
2-7	36.9-76.46	No	9-30	-	-	9-19.15	-	-
7-8	76.46-39.82	No	30-36	-	-	19.15-36	-	-
8-9	39.82-60.8	No	36-42	-	-	36-42	-	-
9-10	60.8-47.58	Yes	42-48	13.22	54.19	42-48	13.22	55.3
8-11	39.82-71.54	No	36-51	-	-	36-43.34	-	-
11-12	71.54-57.48	Yes	51-57	14.06	64.51	43.34-57	14.06	64.82
12-13	57.48-75.8	No	57-60	-	-	57-44.04	-	-

amplitude (gradient), ΔT, and mean temperature, T_m, even a slight difference in temperatures for a large number of load points would affect the overall lifetime, as can be seen from temperature dependent stress-strain plots[44][45].

3.4 Impact of Operating Parameters on Stresses in a Wirebond

The main failures observed in a wirebond are bond-flexure which is popularly known as the heel crack failure and the bond shear failure. Bond shear failures can be classified as 1) that between a bond-pad and wire, and 2) that between bond pad and dielectric substrate [55]. In this work, wire lift-off failure in a wire connecting a silicon dielectric and a copper connector pad is considered for analysis. Figure 3.18 illustrates the block diagram describing the methodology of the lifetime model development. First, experiments to collect temperature data in the power

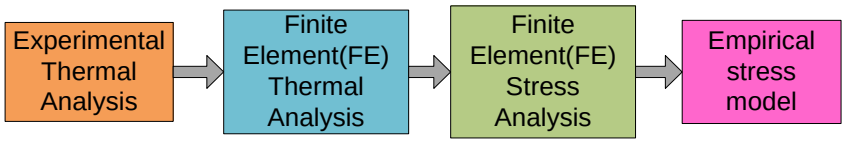


Figure 3.18. Block diagram illustrating the methodology of lifetime model development.

module are conducted. The finite element (FE) based thermal model in COMSOL is calibrated based on the experimental results. The calibrated thermal model input is used to estimate the mechanical von Mises stresses in the wire. The von Mises stress, which is the equivalent stress due to the individual stress components in all three directions (X, Y, Z), is considered for analysis. The FE stress analysis is used to estimate the stress dependence on operating parameters. Finally, a lifetime model based on stress-life relationship from Basquin's model is used to estimate the lifetime of the wire bond [55].

The methodology involves conducting finite element analysis of semiconductor modules with different dimensions for different operating conditions.

3.5 Summary

The basic idea and methodologies of the proposed methods was presented. The lifetime prediction using rainflow algorithm is discussed in this chapter. A new rainflow algorithm is proposed with better execution times. The methodology to determine stresses dependent on operating conditions, obtained from FEA was presented for study. The next chapter, Chapter 4, presents the simulation results for the methods and models developed in this chapter.

CHAPTER IV

SIMULATION RESULTS

4.1 Introduction

This chapter presents the simulation results of the proposed methods in Chapter 3. First, the optimum RC based thermal model developed in Chapter 3 is considered for results under various conditions. Then the wirebond model is developed based on the simulations in COMSOL. In the next section, the STATCOM operation is simulated for power factor correction and diode bridge rectifier load compensation. Finally, the proposed rainflow algorithms are compared and the lifetimes of STATCOM based on proposed rainflow algorithms are presented.

4.2 Thermal Model of Power Semiconductor

The thermal model was developed in Chapter 3. The developed thermal model is considered to estimate the temperatures for different frequencies to emphasize the importance of the number of RC time constant.

4.2.1 Impact of Frequency on Thermal Model

Let us consider the model at different frequencies of 0.1 Hz, 50 Hz, and 1 kHz. Each frequency is chosen to consider for power cycling, line frequency and switching frequencies usually encountered in power electronics applications.

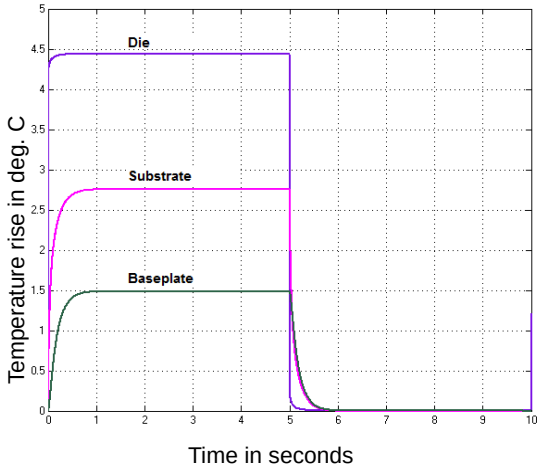


Figure 4.1. Temperature rise with respect to the bottom layers of the die, substrate and the baseplate at 50 Hz.

Figures 4.1-3 are the simulated temperature estimation from MATLAB model for the dielectric, substrate, and the baseplate for 0.1 Hz, 50 Hz, and 1 kHz respectively. For high frequency, at 1 kHz, the dielectric temperature has oscillations because the thermal time constant of the dielectric is very low due to its low mass and reaches equilibrium temperature faster and also cools down quickly. The substrate thermal response has oscillations up to 50 Hz; and at 1 kHz, it almost remains constant. The baseplate has oscillations at 0.1 Hz, and due to high thermal time constant, remains constant at 50 Hz and 1 kHz. The frequency of the power loss input to the thermal model thus determines the thermal oscillations seen on different layers.

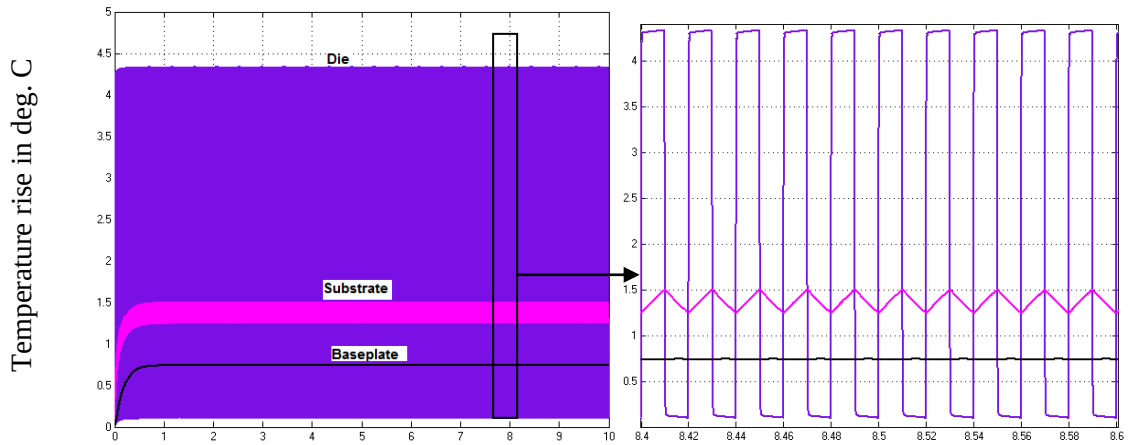


Figure 4.2. Temperature rise with respect to the bottom layers of the die, substrate and the baseplate at 50 Hz.

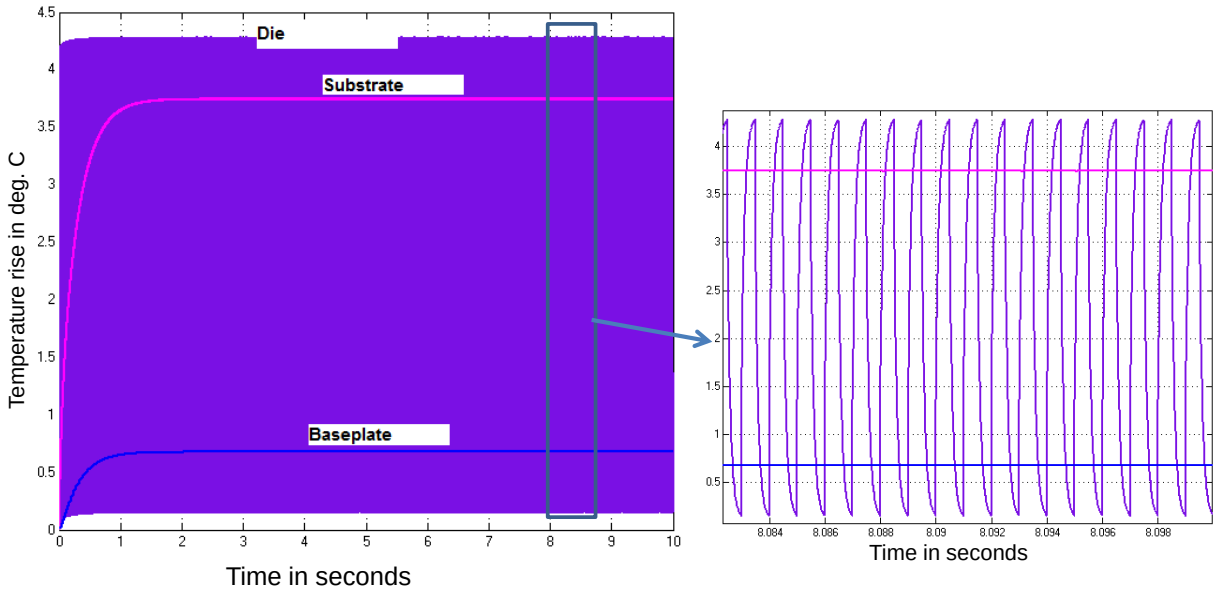


Figure 4.3. Temperature rise with respect to the bottom layers of the die, substrate and the baseplate at 1 kHz frequency.

4.2.2 Impact of number of RC cells

Figure 4.4 presents the minimum number of RC cells varying for different layers in the module, at different operating frequency. For the substrate and baseplate, the number of RC cells required to model the thermal response increases with frequency, as the thermal time response is slow. For the dielectric and solder, the thermal time constant is low (fast response) and hence only one RC cell is sufficient to model the thermal response. The encapsulant has a high thermal time constant owing to its high thermal resistance. The different number of RC thermal network is modeled to have a relative error less than 5%.

4.2.3 Thermal Model of IGBT

The importance of encapsulant consideration in the thermal model was discussed in Chapter 3.

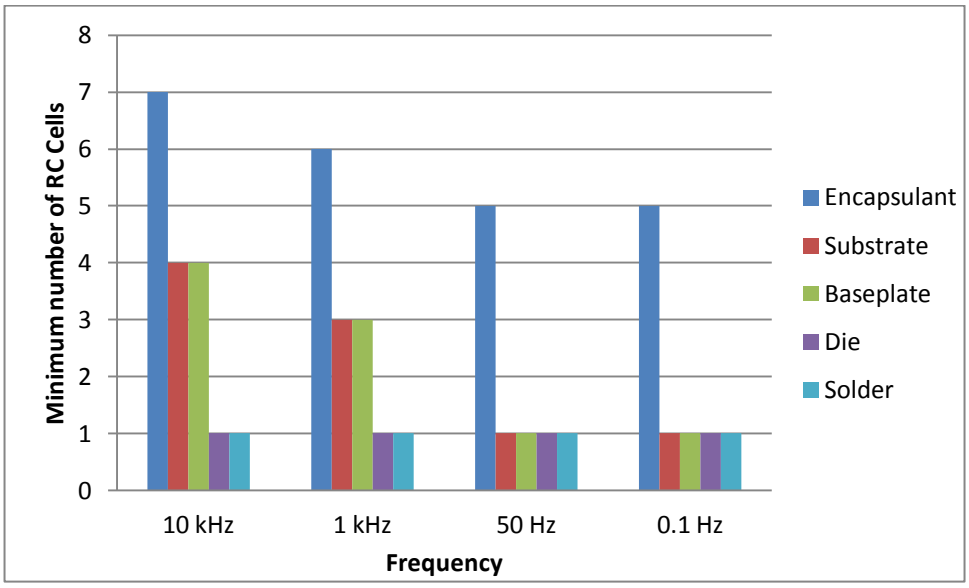


Figure 4.4. Minimum number of RC cells for different layers at frequencies of 10 kHz, 1 kHz, 50 Hz and 0.1 Hz.

In this section, the simulation results of the thermal model of the IGBT device are presented.

Figure 4.5 shows the temperature of the device with the encapsulant. The dielectric temperature as shown in Figure 4.5(a) varies from 30 ^{o}C to 55 ^{o}C, the solder temperature varies from 28 to 40 ^{o}C. Since the dielectric and solder have low thermal time response, they have oscillations at the switching frequency. The baseplate and the substrate have high thermal time response and hence do not have oscillations at the switching frequency. The encapsulant temperature is shown in Figure 4.5(e).

4.3 Impact of Operating Parameters on Stresses in a Wirebond

A fast simulation FEA method to study the thermo-mechanical behavior of the semiconductor packaging materials based on stress relationship with temperatures is developed. Extensive simulations to develop a model dependent on dimensions and operating conditions are proposed [90].

4.3.1 Wire Model

The wires in a power module usually connect a) the power chip (IGBT or diode) to the top copper layer of the DBC (Dielectric-Copper) b) power chip to another power chip (IGBT-IGBT/Diode), and c) the copper DBC to the terminal connections (Copper-Copper). Figure 4.6(a) is a Microsemi H- bridge power module with four IGBT with anti-parallel diodes. The wires are bonded on silicon active devices IGBTs and diodes via bond-pads [15][55]. The silicon dielectrics are soldered to the metallized copper (usually the drain or collector of the devices) of the direct bonded copper (DBC) with titanium, nickel and silver (Ti-Ni-Ag) that serve the purposes of providing oxidation prevention, wetting and solderability. The metallization on

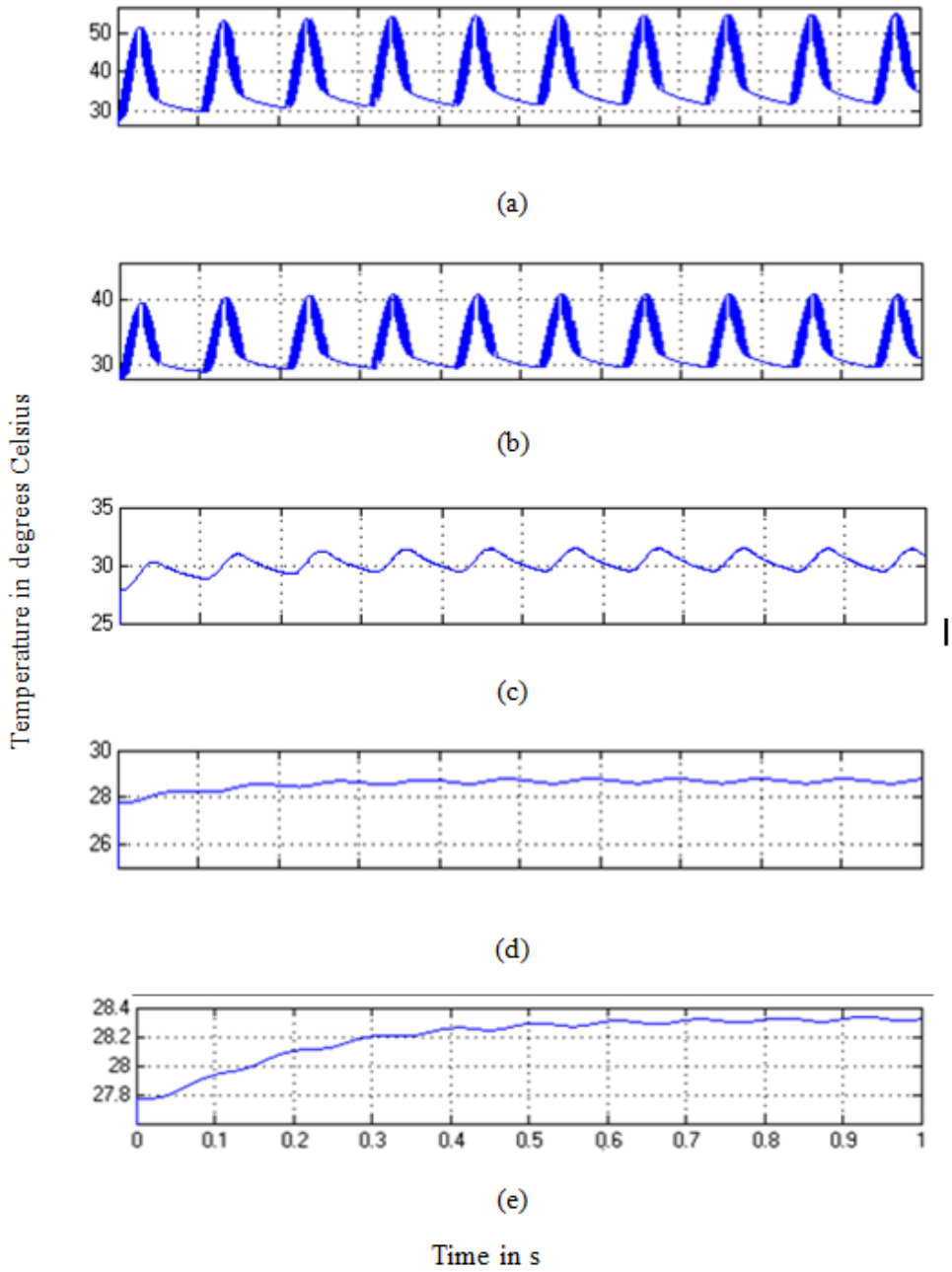
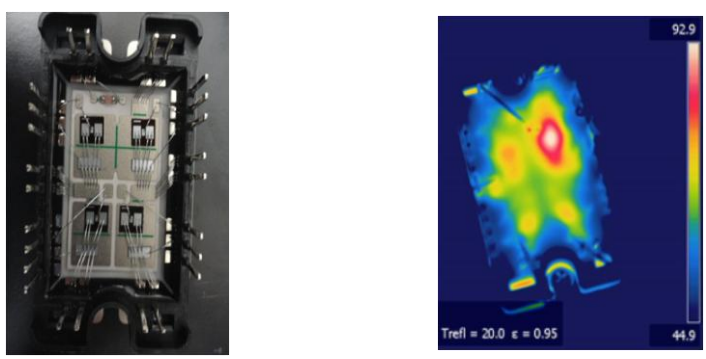


Figure 4.5 Temperatures of a device in a phase leg module at 1 kHz switching frequency and 60 Hz operating line frequency, for power loss input of 100 W for (a) the die, (b) solder, (c) substrate, (d) baseplate, and (e) encapsulant.

copper of DBC are usually nickel and silver for improving wet ability and conductivity [55][56]. While a great amount of research is directed towards solder fatigue, there is a growing research interest in studying the optimality of wire bonds.

As previously mentioned, the first step is to develop a thermal model in FE based on experiments. Single pulse DC power cycling tests [70] are considered for temperature analysis. The losses in the IGBT are varied from 25 W to 150 W with different currents (10-50 A), case temperatures (20-60 ^{o}C) and on-times until a maximum temperature of 100 ^{o}C is reached. The thermal images are taken using a FLIR SC620 infrared camera. This data is used to develop a FE based thermal model.

Figure 4.6(b) illustrates the temperature distribution in the wire for a conduction power loss of 75 W and current of 33 A. The temperature is highest at the dielectric, almost 96 ^{o}C. The



(a) (b)

Figure 4.6. (a) IGBT device and (b) its thermal image when upper left IGBT is power cycled to a temperature of 100 ^{o}C by a total power of 75 W.

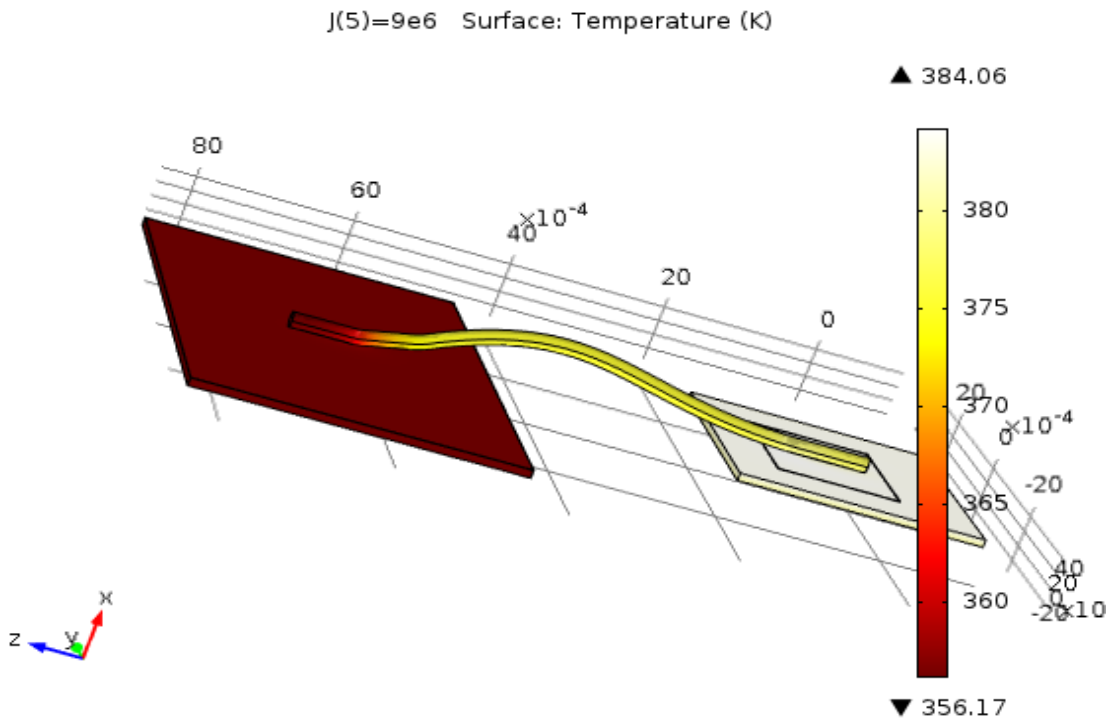
relationship between temperature and current parameters to stress is determined using finite element analysis in COMSOL.

Consider, for simplicity, the wire connection between an active device and a copper connector pad as it undergoes a wide variation of temperatures. Figure 4.7 demonstrates a wirebond model simulated in COMSOL for finite element analysis. It consists of a wire bonded to a silicon chip on one end and a copper connector pad on other end. The dimensions and materials of the model are described in Table 4.1.

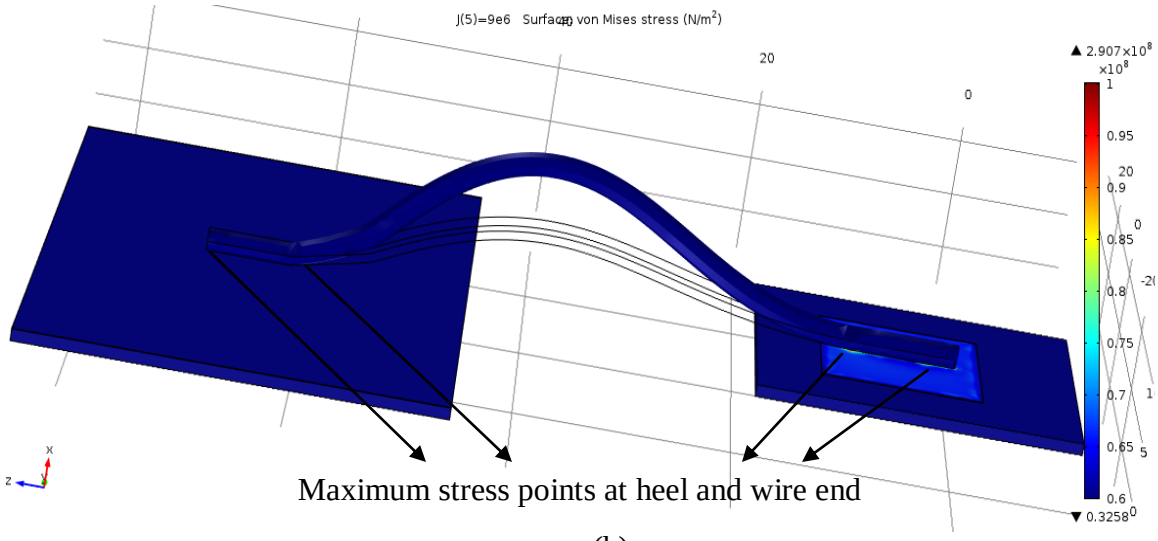
The main inputs to the thermal model are the current density, *J*, heat flux coefficient, external temperature of the module/copper plate, and power loss in the silicon dielectric. Current density is input from the bond pads to the wire and the current exits through the copper metallization. The total current density is calculated for the 50 A rated device as the current divided by the silicon dielectric area, approximately a maximum of 1.5×10^{7} A/m^{2}. Heat transfer through the module is accounted by the heat flux boundary condition that limits the temperature increase in the system based on heat transfer coefficient. The heat flux is calculated by ($q/A/\Delta T$). For a maximum power loss of 100 W, the maximum heat transfer coefficient at the dielectric is 2.5×10^{5} W/ (K.m^{2}).

Table 4.1 Dimensions and materials of wire model in COMSOL

	Material	**Area(l×w) mm^2**	**Thickness mm**
IGBT Die	Silicon	7.05×6.6	0.1
IGBT bond pad	Aluminum	3×2	0.004
Connector pad	Copper	7.4×3.9	0.1
Metallization	Silver	7.4×3.9	0.004
Wire	Aluminum	Length- 6.5 mm	Radius-0.1 mm



(a)



(b)

Figure 4.7. Simplified wire connection model between copper pad and silicon die, and (a) the wire temperature in K and (b) stress in N/m^2 for 9×10^6 A/m^2, 100 W losses in the silicon die.

Similarly, the wire has a boundary condition of heat transfer. The boundary condition of the minimum temperature of the module is power loss dependent, i.e., for high power losses, the minimum temperature of the substrate or dielectric and copper plate. The relationship is given by

$$T_{dbc} = P_{loss} \times R_{th} + T_{amb} \tag{4.1}$$

where R_{th} is the thermal resistance of the dielectric, P_{loss} is the power loss, T_{amb} is the ambient temperature. T_{dbc} is the Direct Bonded Copper (DBC) temperature. The dependence of power loss on voltage and current density is modeled.

To develop the electrical parameter based model, current density, J, voltage, V, (power loss, T_{ext}), ambient temperature T_{ref}, time (T_{max}) and the heat flux, h_c are varied. Figure 4.6(a) shows the temperature in the wire when the copper plate is at a temperature of 343 K, for 9×10^6 A/m^2, and 100 W losses in the silicon dielectric. The temperature is the highest on the dielectric and the wire gets heated based on the current it carries. The temperature of the copper plate is bounded based on the experimental results and the thermal heat transfer vertically and laterally. Figure 4.6(b) shows the stress in the wire for the temperature in Figure 4.6(a). The maximum stress points are observed in the heel and the wire end both on silicon and copper connector. These four points are considered for comparison and analysis in this work. The tensile strength of aluminum is 450 MPa. The principal stresses in three directions are below the tensile strength of aluminum.

Figure 4.8 compares the temperature of the silicon dielectric due to 100 W power loss and currents varying from 30 A to 50 A. The results show good fit between the simulation and experimental results.

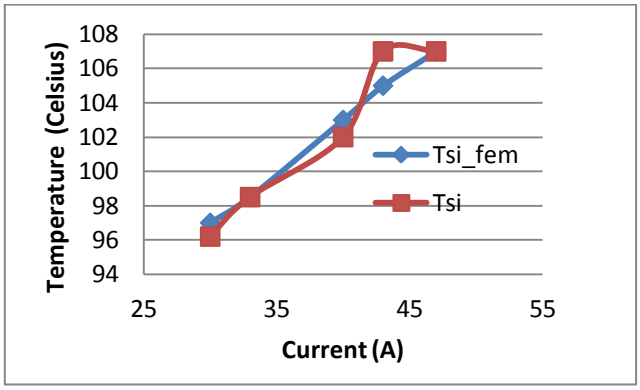


Figure 4.8. Comparison of FEM simulation and experimental temperatures of the silicon die for a 120 W of power loss in die and with currents varying from 30 A to 50 A.

4.3.2 Finite Element Simulation Results for Stress in the Wire

Influence of Electrical Operation Parameters

To study the impact of individual operating parameters, the wire model is simulated. The generic parameters during simulation are a current density of 8×10^6 A/m^2, power loss in the semiconductor dielectric is 100 W, the radius of the wire is 100 um, and the length is 6 mm. The linear thermal expansion model is used to study stresses as short term tests are conducted. For the mechanical stress analysis, the lower boundary of the silicon and copper plates are fixed so that they cannot be displaced. Only the wire undergoes displacement in vertical direction.

Current: Let us consider the dependence of current density on the stress in the wire. For a varying current density from 3×10^4 A/m^2 to 3×10^5 A/m^2, the power loss in the dielectric also varies as the power loss is linearly dependent on the current. The temperature varies from 393 K

to 300 K. Figure 4.9 shows the stress variation with current density. The stress in the wire especially at the bonding is a result of two thermal stresses; one due to the power loss in the silicon dielectric, and the other due to conduction losses in the wire when current flows through it. The power loss on the silicon dielectric has a dominant effect on the overall stress than the current based losses in the wire itself. Hence, an almost linear relationship is observed between the current density and power loss in the silicon dielectric. Maximum stresses are observed on the wire bonds on the silicon side due to the high temperature on the silicon dielectric due to power loss. The stresses vary from 110 MPa to 260 MPa.

Maximum Temperature: The temperature gradient, ΔT, is an important parameter in stress-life equations. In order to study its impact, the maximum temperature is varied from 50 ^{o}C to 100 ^{o}C by varying the heat flux of the system. Figure 4.10 illustrates the stress variation with the flux variation. It can be observed that the variation of stress is dominant on the silicon side. Even though the variation with respect to heat flux is of the decreasing exponential, the dependence of

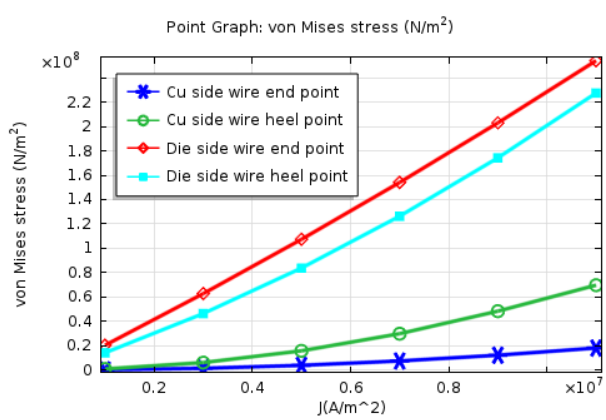


Figure 4.9. Stress variation with current density variation from 1×10^{6} to 8×10^{6} A/m^{2}.

maximum temperature on the stress is linear.

Power Loss: The stress is linearly dependent on the power loss in the silicon device. Figure 4.11 shows the stress variation from 50 W to 200 W. The copper connector plate is almost at a constant stress as the power loss in silicon i.e., has maximum effect on stresses on the silicon

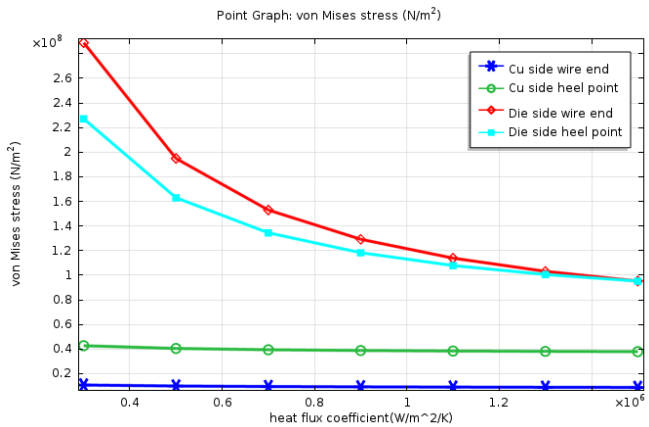


Figure 4.10. Stress variation with heat flux coefficient variation from 3×10^6 to 1.5×10^6 W/(m^2.K).

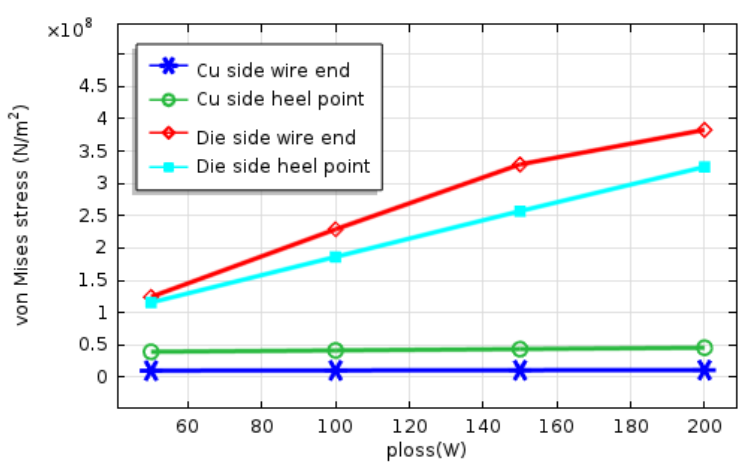


Figure 4.11. Stress variation with power loss varying from 50 W to 200 W.

side bonding of the wire.

Ambient Temperature: Consider the ambient temperature varying. Figure 4.12 shows the stress variation for ambient temperature variation from 293 K to 333 K (20-60 ^{o}C). The temperature of the wire is influenced by the power loss on silicon dielectric side and on the heat transfer from the silicon dielectric to substrate on the copper side, apart from the ambient temperature. For a power loss of 100W, the temperature of the different points in the wire varies linearly as ambient temperature varies. However, the stress is constant. For a linear elastic region operation, the stress is due to the strain caused by the difference in temperatures, ΔT. For a constant rise in temperature, the temperature gradient, ΔT is also constant. Hence the stress is

Figure 4.12. Stress variation with ambient temperature, T_{ref}, from 293 K to 343 K.

constant.

Cumulative Influence of Operation Parameters on Stresses in the Wire:

Let us consider the finite element analysis of the model for a set of experimental data obtained from power cycling tests with different conditions. Figure 4.13 is a plot of three parameters current density (J), power loss, and the heat flux, varying simultaneously at point 35 which is the point on the heel of the wire end connected to the silicon dielectric. The effect of current density and heat flux is predominant while that of power loss is less visible from the plots. In this case, since the power loss and the heat flux are varied simultaneously, the power loss influence on temperature and hence stress is reduced. The overall stress equation dependent on the various parameters can be written as

$$\sigma(t, T_{amb}) = A\Delta T = A(T_{\max} - T_{\min}) \tag{4.2}$$

$$T_{\max} = f(P_{loss}, T_{\min}, J, h_c, t_{on})$$

$$= (\{P_{loss} + (J \times A_w)^2 \times R_w)\} \times t_{on}/h_c + T_{min} \tag{4.3}$$

$$T_{\min} = g(P_{loss,} R_{th}, T_{amb}, t_{off}) = (P_{loss} \times R_{th} + T_{amb}) \tag{4.4}$$

where P_{loss} is the power loss in the silicon dielectric, J is the current density, h_c is the heat transfer coefficient of the system, R_{th} is the thermal heat resistance of the DBC, t_{on} and t_{off} are the on and off times of the power switch, T_{min} and T_{max} are the maximum and minimum temperatures of the point of interest on the wire at the heel or wire end, R_w is the resistance of the wire, A_w is the cross sectional area of the wire, A is the proportionality constants.

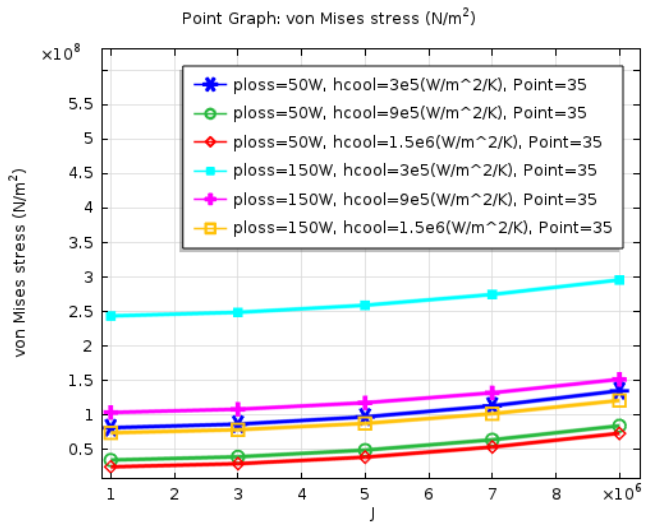


Figure 4.13. Stress variation with power loss in die, p_{loss}, and heat flux coefficient, h_c.

The lifetime equation for number of cycles, N, based on stress, σ, life is given by Basquin's equation [1] can be used to calculate the lifetime.

$$N = A\sigma^{-m} \tag{4.5}$$

where m is obtained from Basquin's equation or power cycling data.

4.4 STATCOM Simulation in EMTP

EMTP-RV is a computer program for the simulation of electromagnetic, electromechanical and control systems transients in multiphase electric power systems [66]. To simulate STATCOM in EMTP, a simple two-bus system was developed with source and load as shown in Figure 4.14. A three-phase sinusoidal voltage source, V_s, of 480 V line-line voltage is connected to a load, drawing a current, i_l. The STATCOM is connected in shunt between the source and

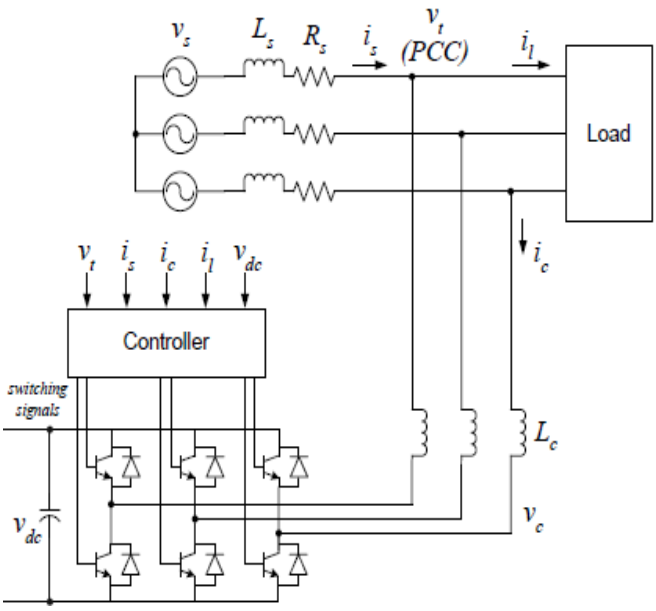


Figure 4.14. STATCOM model connected to grid.

load via a coupling inductance L_c, so that it provides the necessary reactive current for the respective functions of the STATCOM such as power factor correction, harmonic elimination, etc. The controller of the STATCOM in this work is based on non-active power compensation theory [27].

4.4.1 Power Factor Correction

The simulated results of currents and voltages are obtained from EMTP, and the average losses are calculated based on the look-up table values from characteristic tests conducted at different voltage, current, and temperatures to estimate the average temperature rise in the IGBT junction.

Figures 4.15 illustrate the STATCOM operation for power factor correction. For power factor correction, the peak load current is 100 A at 30° lagging power factor.

4.4.2 Analytical Loss Calculation

Table 4.4 describes the list of parameters used for analytical calculation methodology.

The general equations for average conduction losses in IGBT and diode [83] are given by (4.6) and (4.7) for inverter current I_a

$$\left(P_{cond_i}\right) = I_a \times \frac{V_{on_i}}{2\pi} + \frac{I_a \times R_{on_i}}{8} + I_a \times \frac{M}{2} \times \frac{V_{on_i}}{4} + \frac{I_a \times R_{on_i}}{3\pi/2} \times PF \tag{4.6}$$

$$\left(P_{cond_d}\right) = I_a \times \frac{V_{ond}}{2\pi} + \frac{I_a \times R_{ond}}{8} + I_a \times \frac{M}{2} \times \frac{V_{ond}}{4} + \frac{I_a \times R_{ond}}{3\pi/2} \times PF \tag{4.7}$$

Power Factor Correction

For a lagging/leading power factor current drawn by the load, the real power is provided by

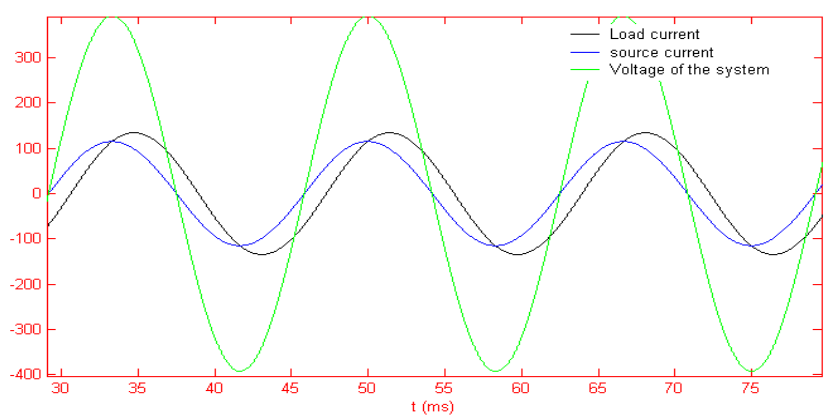


Figure 4.15. Source voltage, load and source currents of the system for power factor of 0.8.

the source while the reactive power is provided by the STATCOM, i.e. the magnitudes of the source and inverter currents are $i_{active}=i_s=i_l \times cos(\Phi)$ and $i_{nonactive}=i_c=\pm i_l \times sin(\Phi)$ respectively.

When an inverter is operating to compensate for reactive power, to maintain unity power factor of the grid, the losses are given by

$$\left(P_{cond_i}\right)=I_l \times \sin(\phi) \times \left(\frac{V_{on_i}}{2\pi}+\frac{I_l \times R_{on_i}}{8}\right) \tag{4.8}$$

$$\left(P_{cond_d}\right)=I_l \times \sin(\phi) \times \left(\frac{V_{on_d}}{2\pi}+\frac{I_l \times R_{on_d}}{8}\right) \tag{4.9}$$

Table 4.2. List of parameters and descriptions.

I_l	load current of the system
I_a	inverter phase current
Φ	power factor angle of the load
M	modulation index
R_{fd}	on state resistance of diode
R_{oni}	on state resistance of IGBT
V_{on_d}	forward voltage drop across the diode
V_{on_i}	forward voltage drop across the IGBT
E_{on_test}	turn on switching losses from test conditions
E_{off_test}	turn off switching losses from test
V_{DC}	DC voltage across the switch during the current operation
V_{DC_test}	DC voltage across the switch with the test conditions from the datasheet
h	harmonic number
I_{ctest}	current across the IGBT during test conditions
I_h	h^{th} harmonic current
f_{sw}	switching frequency
PF	power factor of the inverter

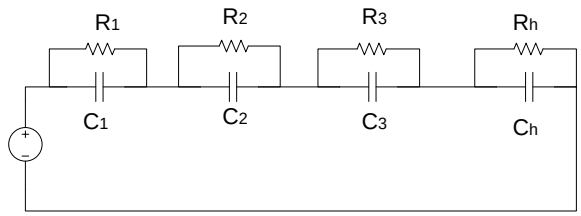


Figure 4.16. Foster based thermal model of the device.

4.4.3 Thermal Model

Foster model of the IGBT was used for the thermal model as shown in the Figure 4.16. The calculation of junction and case temperatures were based on the datasheet values of the thermal resistances of the IGBTs and diodes. The heat sink used by PP150T120 inverter was modeled to characterize temperature nearest to its actual value. The air flow speed is 1500 LFM (Linear Feet per Minute) as stated in the datasheet. The temperature gradient in the device is caused due to the wave shape of the current and also due to the thermal time constant associated with the thermal model during heating and cooling. It is directly dependent on the power losses in the device. The mean temperature can be obtained by considering the thermal model with purely resistive elements. It is also dependent on the power loss in the device.

4.4.4 STATCOM Simulation Results

Power Factor Correction

The IGBT temperature is linearly dependent on the inverter current for reactive compensation. From the analytical equations, this can be attributed more to the high switching losses than

conduction losses. Even though the temperature is related to square of the current in the conduction losses, the greater magnitude of switching losses contribute to a more linear relation between current and temperature [86][87].

Figure 4.17 illustrates the junction temperature variation of the IGBT with power factor obtained from linear relation between inverter current and load current and sine of the power factor angle. The negative values of power factor are used to indicate lagging power factor. As the load current increases, the temperature of IGBT also increases.

4.4.5 Lifetime Estimation for Power Factor Correction

One of the most common methods of testing reliability of semiconductors is by power cycling tests. The typical model of predicting the number of cycles to failure of an IGBT based power cycling capability is given by Arrhenius and Coffin-Manson laws of degradation

$$N_f(T_m, \Delta T_j) = A \times \Delta T_j^{\alpha} \times \exp^{(\frac{Q}{RT_m})} \tag{4.10}$$

where A, α are constants and are module dependent, R is the gas constant (8.314 J1mol.K), T_m is the mean junction temperature in one power cycle expressed in Kelvin, and the internal energy Q is $7.8*10^4$ $Jmol^{-1}$ (or about 0.8eV). ΔT_j is the variation of the junction temperature.

By curve fitting the supplier's power cycling data to that of (4.10), the constants are derived as α equals -6.14, for mean temperature, T_m of 25 ^oC, A=1300. The constant values were obtained by curve fitting the manufacturer's data for power cycling to (4.10). The lifetime of the IGBT from (4.10) is shown in Figure 4.18 for power factor compensation operation by the STATCOM. As the load power factor varies from 1 to 0, the temperature gradient and mean temperature both

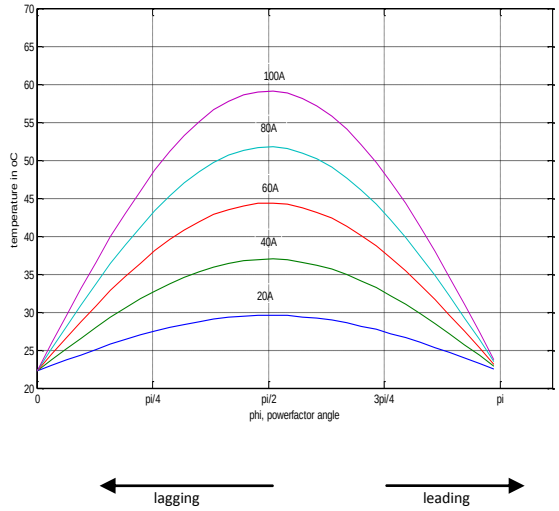


Figure 4.17. Temperature of IGBT varying with power factor of load.

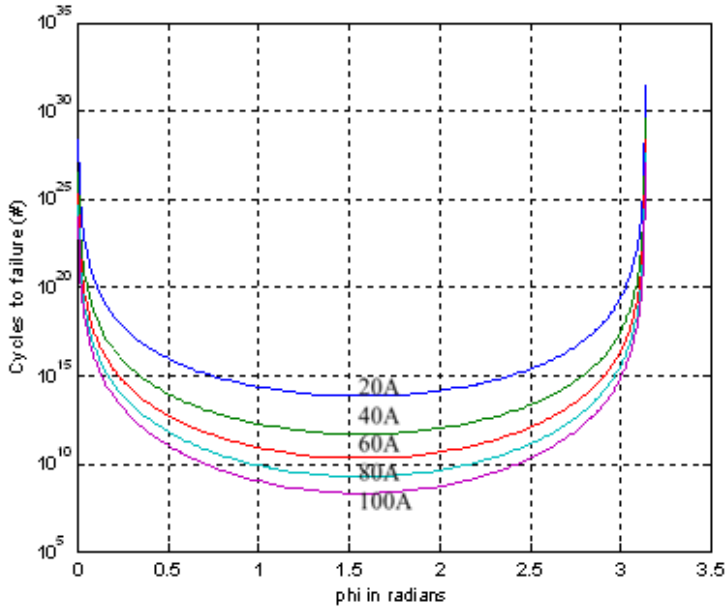


Figure 4.18. Lifetime of IGBT in terms of number of cycles to failure varying with power factor angle of the load.

increase as the power losses increase with inverter current. Hence the lifetime of the IGBT is inverted with respect to the mean temperature profile obtained in Figure 4.17[87].

4.5 Lifetime Prediction Using Rainflow Algorithm for a Power Factor Varying Load Profile

4.5.1 Using Proposed Rainflow Algorithms for a Power Factor Varying Load [88]

Rainflow algorithm is used in estimating the lifetime of semiconductors, especially for electric vehicles and wind applications [3]-[12]. The algorithm counts the temperature data that constitute a closed stress loop as a cycle and calculates the mean and amplitude of the temperature data. The temperature swing and mean values are used in lifetime estimation using Coffin-Manson's lifetime equation first proposed by RAPSDRA [4] for power semiconductors. Linear cumulative model is used to estimate the lifetime.

Most of the research using rainflow algorithm uses the MATLAB code available [84]. The ASTM standard uses 3-point based algorithm, and the MATLAB code available uses a mean temperature calculation that is independent of the time of the temperature.

Load profile for the power factor correction data is based on power measurements for short periods of time, in this case 5 minutes. This gives us an idea about the lifetime degradation of the semiconductors in 5 min. and can be extrapolated to estimate the lifetime. Figure 4.19 is a plot of power factor data. For a load of 100 A, the power factor for 5 minutes decreases with time. As the power factor decreases, the STATCOM provides the necessary reactive power and the temperature of the IGBT, CM150DU is calculated from the thermal model. The temperature data of the IGBT is shown in Figure 4.19. The power factor data is a continuous value. However, in

one cycle of line frequency current of 60 Hz, the temperature of the IGBT increases during the positive cycle and decreases during the negative cycle, as shown in Figure 4.20. The lower IGBT of the phase leg conducts during the negative cycle.

The remaining life linear accumulation of the fatigue damage is given by

$$RL = 1 - \sum \frac{N(\Delta T)}{N_f(\Delta T)} \tag{4.11}$$

Using the new rainflow algorithm, the number of cycles and their distribution is shown in Figure 4.21. Using (4.10) and (4.11), the remaining life for the load profile shown in Figure 4.18 is $1.9*10^6$ cycles which is about 3.4 years [88].

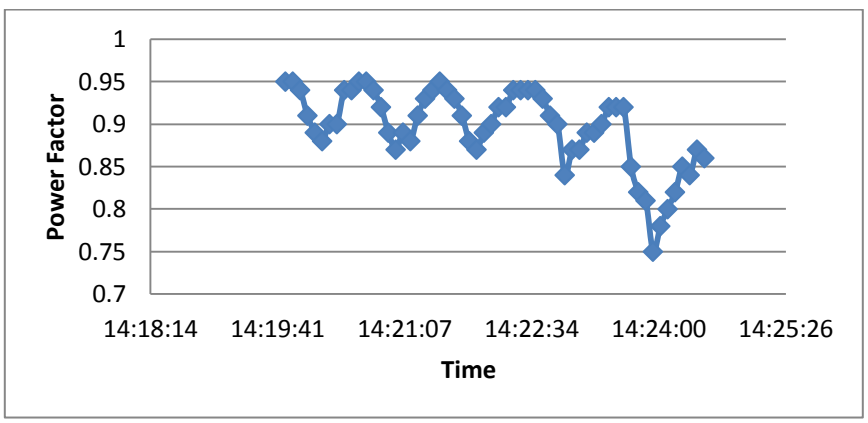


Figure 4.19. Power factor variation of the 5 minute load data of a building.

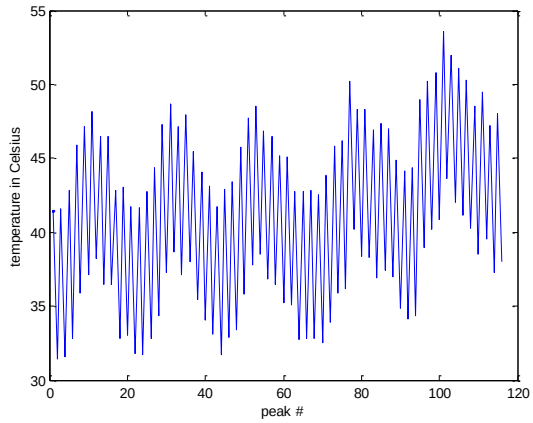


Figure 4.20. Temperature of the IGBT of STATCOM for load profile of Figure 4.19.

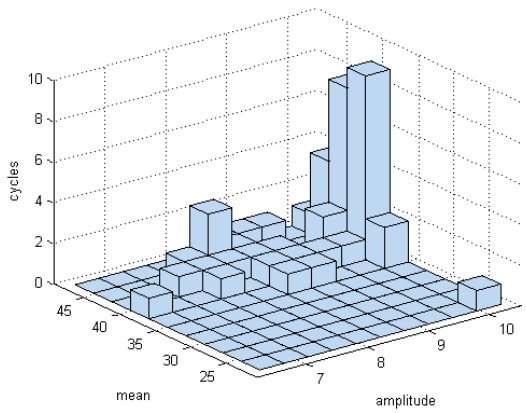


Figure 4.21. Temperature cycle measurement from rainflow algorithm for the 5 minute power factor variation load data in Figure 4.18.

4.5.2 Lifetime Estimation of IGBT in a STATCOM for an Arc furnace Load using Equivalent Temperature Rainflow Algorithm[89]

A STATCOM is a voltage source converter connected to the grid to provide reactive compensation and harmonic elimination. In order to estimate the lifetime of an IGBT in a STATCOM, a long term load variation for a power system should be obtained. In this case, an arc furnace based industrial load in Brazil, whose power factor values are monitored every 15 minutes throughout the day over a period of a month, shown in Figure 4.22, is considered for analysis and lifetime estimation of IGBT. Every day during the weekdays from 19:30 hrs to 23:30 hrs the arc furnace load is switched off and the capacitor banks are used to provide reactive compensation of the grid current. During these off-peak hours, the output power is low but reactive power is injected into the grid, resulting in low leading power factor. It is assumed that STATCOMs connected in parallel compensate for overall reactive power of the load and a single STATCOM can compensate the maximum rated power, 180 kVA.

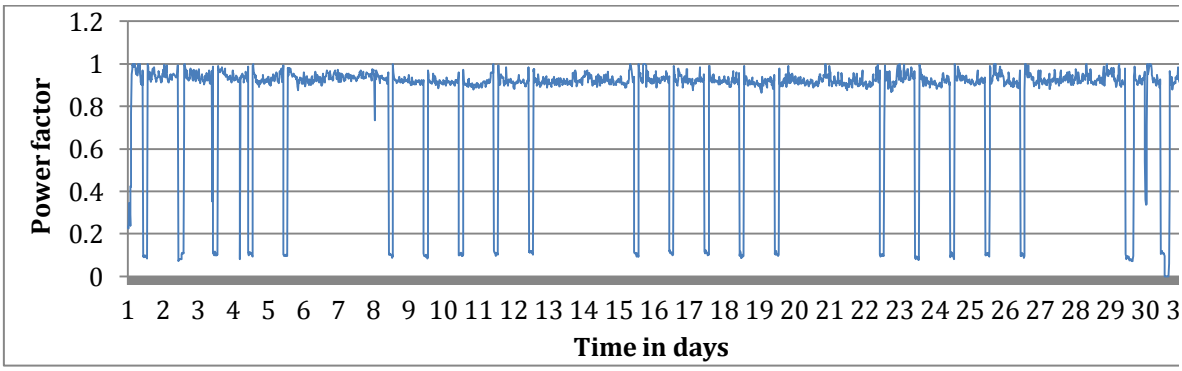


Figure 4.22. Arc furnace based industrial load power factor variation monitored for every 15 minutes for a period of month.

The IGBT current and temperature distribution while maintaining unity power factor of the power system is shown in Figure 4.23 and Figure 4.24, respectively. The temperature varies from 40°C to a maximum of 100°C. This temperature profile of a semiconductor is applied to fast rainflow algorithm in conjunction with equivalent temperature calculation [81].

The total cycles for the load profile are 533 using four-point rainflow algorithm. Degradation is calculated with and without equivalent temperature calculation, and the histogram plots are shown in Figure 4.25(a) and (b) respectively. For conventional rainflow algorithm calculation, the degradation accounts for 0.029% degradation for the month while the degradation calculation with equivalent temperature calculation accounts for 0.033%. This emphasizes the importance of

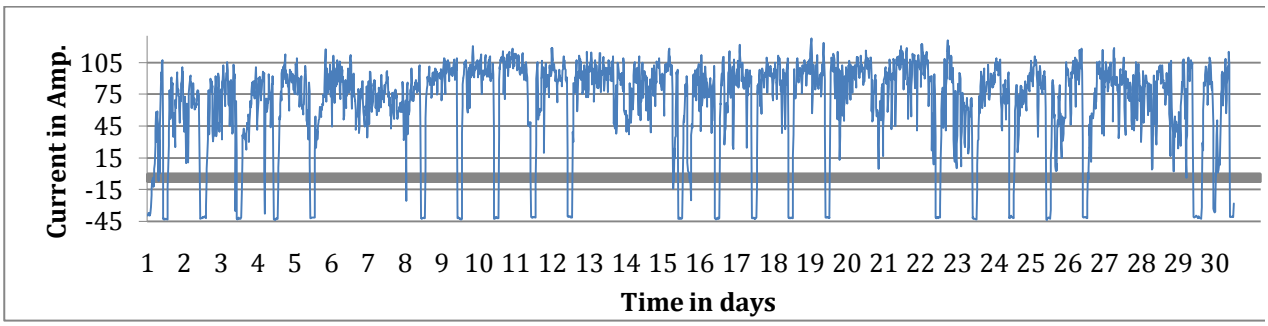


Figure 4.23. Inverter current in amperes for unity power factor of the load.

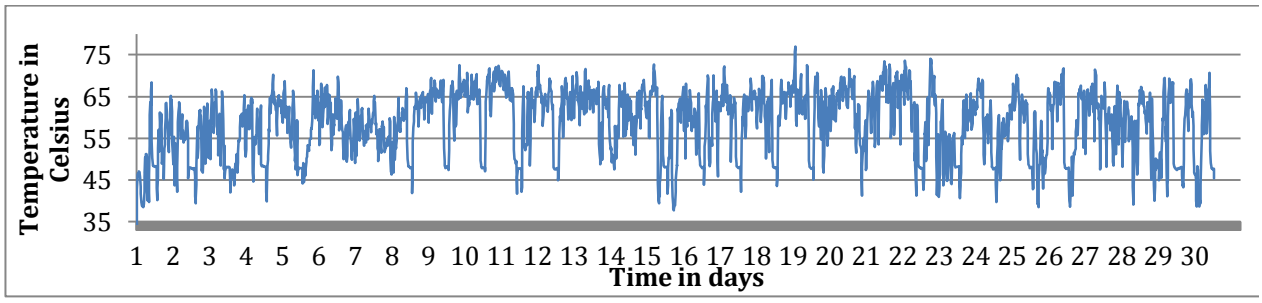
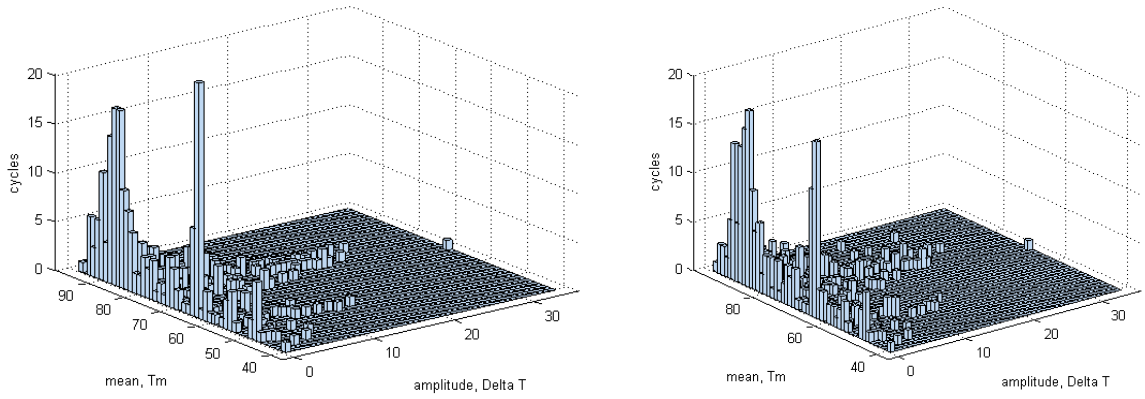


Figure 4.24. IGBT temperature variation for the reactive compensation of the load.

equivalent temperature based lifetime calculation for semiconductors in long-term calculations.

4.6 Summary

This chapter presented the simulation results of the proposed thermal model with encapsulant, modified rainflow algorithm, and the stress model of a wire. The thermal model is simulated at different operating conditions. The operating parameter based wirebond stress model is analyzed based on the finite element simulations in COMSOL. A STATCOM is simulated in EMTP and MATLAB, and the results for power factor correction are presented. Finally, using the proposed rainflow algorithm and the equivalent temperature calculation method, lifetime estimation of an arc furnace load is simulated in MATLAB and compared with the conventional methods.



(a) (b)

Figure 4.25. Rainflow histogram of load profile in Figure 4.22 with (a) conventional calculation and (b) equivalent temperature calculation.

CHAPTER V

EXPERIMENTAL RESULTS

5.1 Introduction

This chapter presents the experimental set up and the results for the temperature measurements of the STATCOM operation for power factor correction. The next section presents the experimental set up for DC power cycling tests and the testing of two different modules. It presents the failures observed in the power module when tested with no protective circuits and presents the degradation in the high current rated IGBT module tested with protective circuits.

5.2 STATCOM Experimental Setup

A STATCOM connected to the 480 V line-line grid is set up, as shown in Figure 5.1 at Oak Ridge National Laboratory (ORNL). The inverter, APS PP150T120 consisting of three Powerex IGBT modules (CM150DU-24F) rated at 1200 V, 150 A, is connected to DC voltage source of 800 V. A fan is installed to run at a maximum speed of 1500 LFM for heat removal from the inverter system.

In order to simulate reactive power compensation, the inverter was tested off-grid to feed purely inductive loads. A thermistor is placed in the inverter between Phase A and B IGBT modules to monitor temperature. The inverter is controlled using dSPACE and the temperature is monitored.

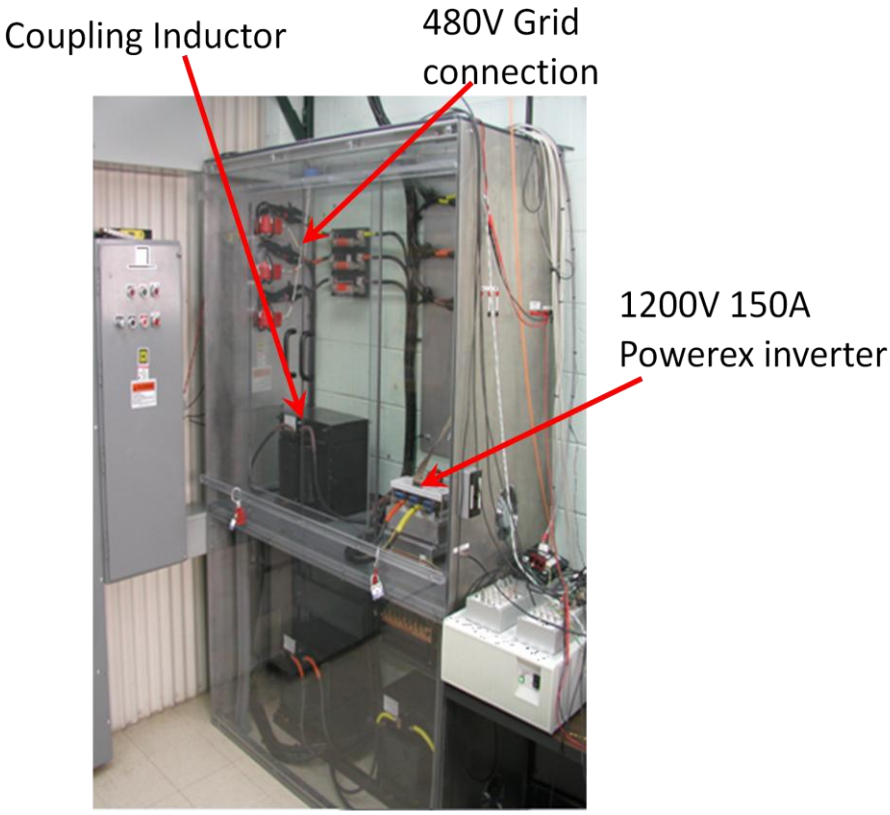


Figure 5.1. STATCOM setup at ORNL.

Figure 5.2 compares the temperature data at different inverter loads for reactive compensation by analytical calculation, simulation and experimental results. The analytical data and simulated data are closer than experimental data. The experimental data was from a thermistor placed in between phase A and B and not directly from IGBT module A. Hence, the experimental temperature is lower than actual IGBT temperature.

5.3. Power Cycling Test Setup

Power cycling tests to evaluate the dependence of frequency, current and voltage on lifetime for STATCOM operation are proposed.

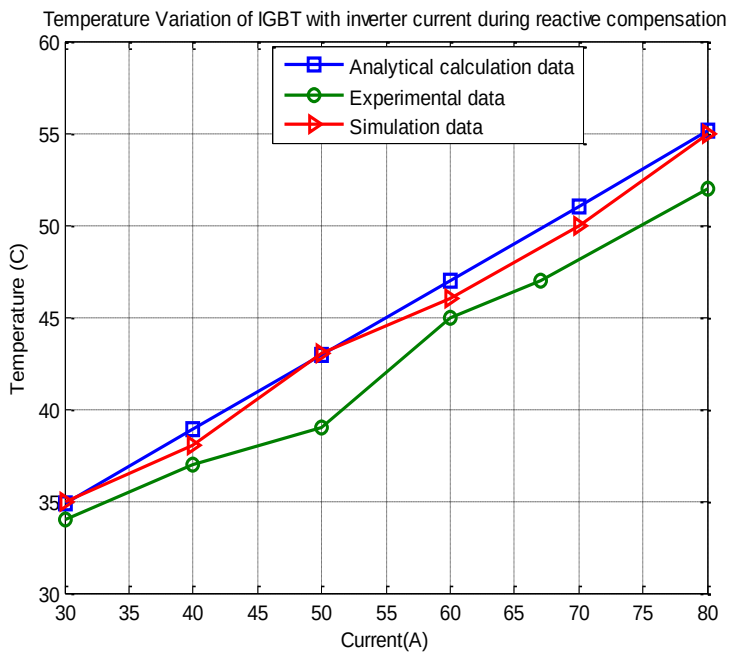


Figure 5.2. Comparison of temperature data at different inverter loads for reactive compensation by analytical calculation, simulation and experimental results.

The basic requirements of power cycling test circuits [14] are

1) Testing must include switching losses associated with the IGBT

2) Both IGBTs and free-wheeling diodes must be tested

3) The test setup must be kept as simple as possible

4) Equipment and energy costs must be kept to a minimum

5) The test duration must be as short as possible

6) Load current magnitude and waveform, and the variation in ΔT_j must be as representative as possible of service conditions.

One of the simplest circuits for a single device testing for accelerated DC power testing is shown in Figure 5.3 [70]. A high current source provides current to the devices at low gate voltages, nearer to threshold voltage, such that the collector-emitter voltage is high at rated currents which results in higher power losses, in the device. In order to accelerate failures, the device should be operated at its rated values of temperature, and current.

Two different modules were tested. First, four samples of the H-bridge 50 A 600 V IGBT module was tested without the protection circuits. Then, the phase leg module CM150DU rated at 1200 V, 150 A was tested with all protection circuits to prevent catastrophic failure of the devices.

IGBT devices were tested at their rated currents and power dissipation to accelerate degradation. For multiple devices testing, devices are connected in series and parallel. The current from the 50 V, 100 A Magna-Power power supply is used to provide 100 A, such that 50 A passes through each IGBT. The voltage is set to a maximum of 20 V on the power supply, as the on-state voltage drop in each IGBT is less than 7 V. The gate voltages on the devices are set closer to threshold voltage, to ensure the devices are conducting but also have a higher voltage drop.

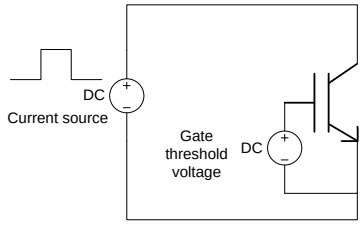


Figure 5.3. DC power cycling test circuit at gate threshold voltage.

5.3.1 Operating Conditions Determination

Since the temperature is the cause of most failures in power semiconductors, it is important to determine the operating conditions based on the maximum temperature requirement of the test design. The on and off times of the power supply are determined by the temperature rise and fall of the device. In this case, the device is cycled at high temperature values, from 80 to 120 ^{o}C. For a fan based cooling system, the on and off times of the power supply are set to 18 s and 22 s respectively, that is automatically controlled by the control signals. IGBT devices in the H-bridge module APTGF50H60T3G rated at 600 V, 50 A, were tested at their rated currents for gate voltage of 7 V and higher power dissipation to accelerate degradation. The phase leg module CM150DU rated at 1200 V 150 A was tested at 100 A, at gate voltage of 9 V.

5.3.2 Measurements

Apart from temperatures, the collector emitter voltage, V_{ce}, the collector current, I_c, and the gate voltage, V_g of the DUT are recorded. The case temperature is measured by a fast time response (10-20 msec) T-type thermocouple. The thermocouple is placed between the heat sink and the base plate right under the device being tested. The collector-emitter voltage and the gate voltage are measured by Keithley DAQ. The collector current is measured by LEM's HTB100 current sensor capable of measuring currents as high as 100 A. All the measurements are monitored by Keithley Data Acquisition (DAQ) System unit 2701, and stored in a computer by MATLAB.

5.3.3 Protection Circuits

It is necessary to shut off the testing as soon as the failure criterion is reached to prevent catastrophic damage. The protection circuits for out of limit collector-emitter voltage, collector current, gate voltage and temperature are designed. The limit values are selected based on the failure criteria in Table 2.5. The power supply trip, for beyond limit collector-emitter voltage, collector current, gate voltage and temperature values, is triggered by the DAQ when the parameter values are beyond the limits.

Apart from the power supply trip, a ground fault trip is initiated when the ambient temperature reaches to 60 ^{o}C to prevent over- temperature operation by a temperature sensor switch. The test set up is placed in a metallic mesh box to allow air circulation and prevent any hazard to adjacent equipment and personnel. An automatic text message alert is sent to cell phone of the concerned personnel when the power supply is tripped or ground fault interrupt. Figure 5.4 shows the test

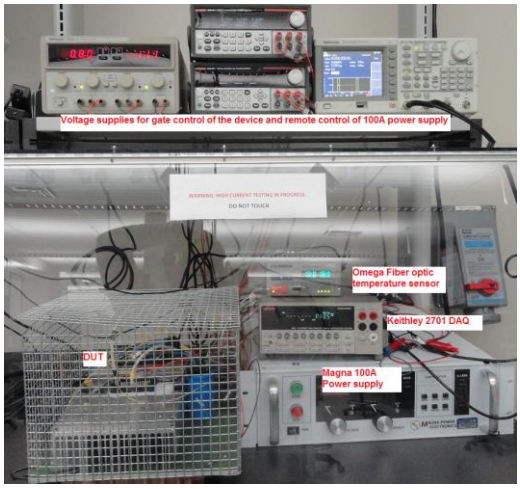


Figure 5.4. DC power cycling test set up in the CURENT power electronics laboratory.

set up in the power electronics laboratory at the University of Tennessee, Knoxville.

5.4 RESULTS AND DISCUSSION

5.4.1 Failures in 600 V, 50 A IGBT module under DC power cycling

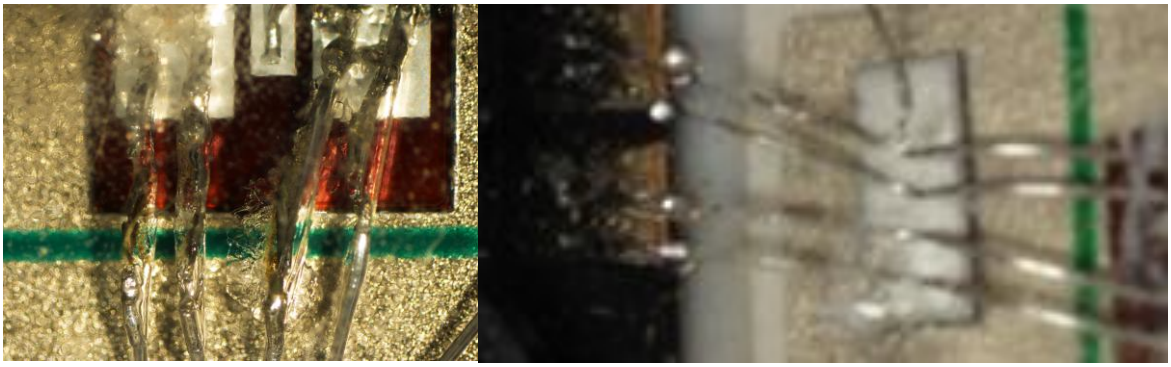
The H bridge modules rated at lower current failed catastrophically as protection circuits were not implemented during their testing. The following section discusses the various failures observed in the devices. Three main failures were dominantly observed; a) short circuit, b) open circuit, c) emitter/source metallization degradation and d) wire bond melt off. With high temperatures especially on the dielectrics during failures, the encapsulant is blackened due to carbonation. The following sections discuss each of the observed failures with detailed analysis.

Wirebond Related Failures

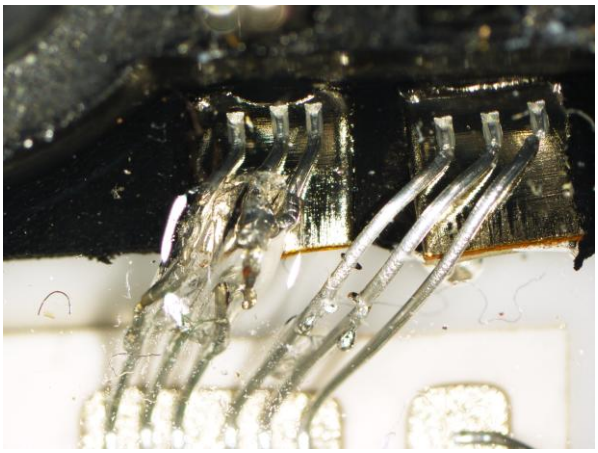
In some cases, the failures observed were a combination of wirebond melt-down and short-circuit of the device. The maximum number of cases of failure was observed in wire melt-off, as shown in Figure 5.5. The wire melt-off occurred in the middle region of the wirebond where the loop height is the maximum. Two main reasons can be attributed for wire-melt-off. They are: a) maximum temperature in the wire is at the midpoint [58] and b) the encapsulant in the device affects the wirebond temperature as explained in Chapters 3 and 4. Most of the dielectric damage and source metallization degradation occurred under the wire bond.

One of the devices that had the emitter wires connecting the IGBT dielectric to the busbar through the diode had a significant wire melt down, shown in Figure 5.5(b). This device was tested for avalanche testing prior to DC power cycling. In avalanche testing of a single device with anti-parallel diode, the diode is stressed in reverse bias due to the inductance. The emitter wires connected to the terminal pins/busbars are stressed during current conduction not only

during IGBT conduction but also during the diode conduction. Hence, the emitter wires connecting to the terminals were stressed more than the emitter wires connecting the IGBT and the diode. This infers that the terminal pin/busbar connecting wires are the most stressed in a module, if the device were operating under reactive load conditions. Thus, for reactive loads, wirebond failures are more predominant than dielectric related failures.



(a) (b)



(c)

Figure 5.5. Wire melt-off with (a) encapsulant blackening at the midpoint of the wire, at the maximum loop height (b) at the source terminals, and (c) at the drain terminal connection.

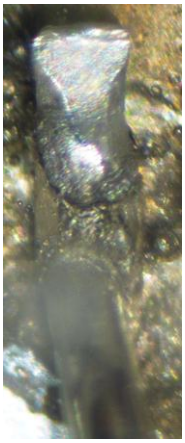


Figure 5.6. Wire crack failure in an IGBT device.

Figure 5.5(c) shows a similar terminal wire connections melt-off failure but on the drain/collector side. In this test, however, the H-bridge module was operated as two parallel phase legs in order to test all the four devices in the module. The common collector/drain connection for the two phase legs was stressed with almost 1.5 times its rated current and ran for 1000 cycles before the wire melt-off on the wires. This type of test gives an insight as to the how many cycles of overload current conditions it can withstand in case of its operation as STATCOM, during emergency situations.

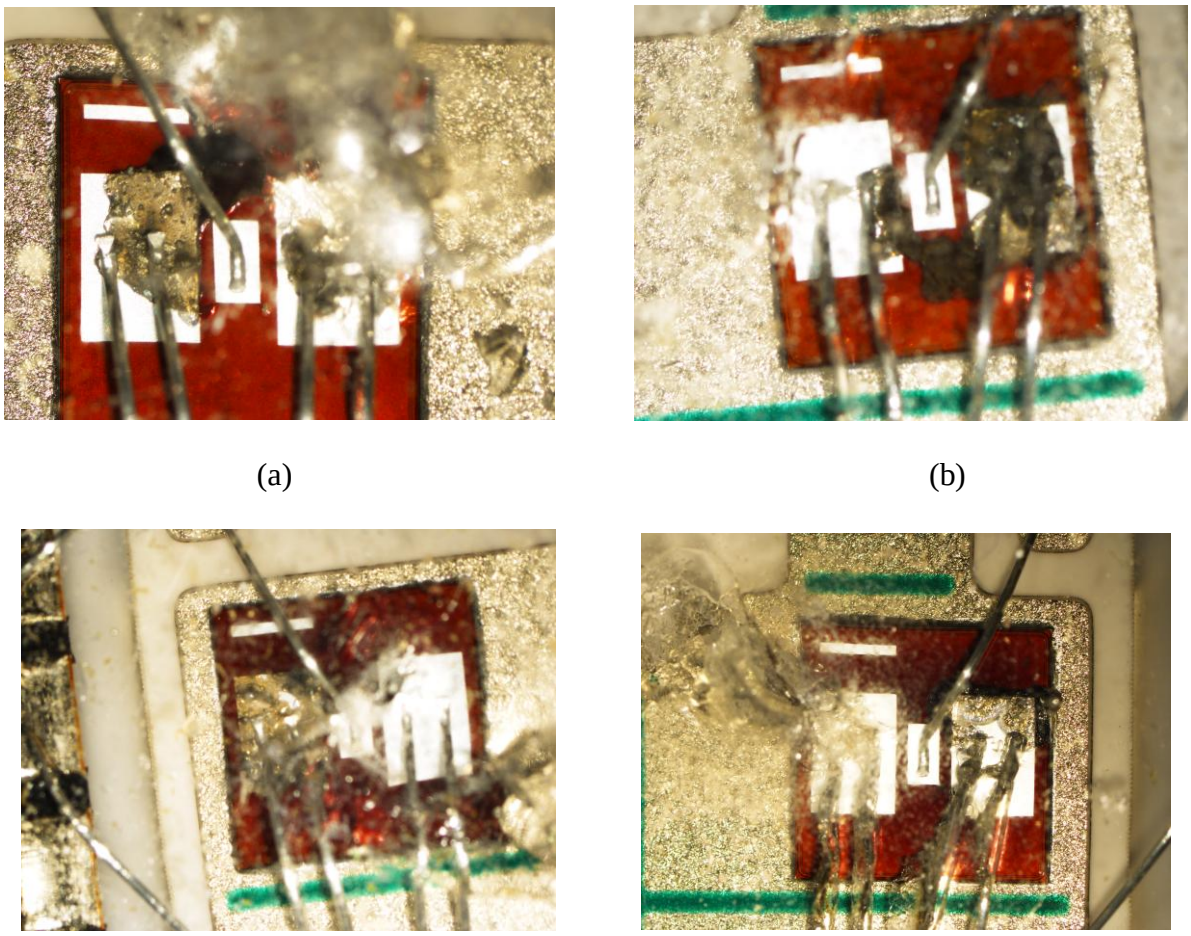
Another type of wire related failure observed was the cracking of the wire at the bond heel, as shown in Figure 5.6. The device failed open. For the wire melt-off seen in Figure 5.5, the devices failed short, drawing high currents at high temperatures and thus causing wire melt-down.

Dielectric Related Failures

The dielectric bond pads closer to the outer edges of the substrate failed more frequently than the dielectrics placed towards the center of the substrate, as shown in Figure 5.7. The failure mechanism in each of the devices is different.

One of the devices failed open, as shown in Figure 5.7(a). It had wire-bond lift-off and wire crack on the leftmost bond-pad. The temperature degradation can be observed to have extended beyond the bond pads, as seen from the figure, indicating a dielectric based failure.

The device in Figure 5.7(b) failed short. The blackening is observed not only of the encapsulant but also due to the burnout of the dielectric underneath. The dielectric burnout seems



(a) (b)

(c) (d)

Figure 5.7. Die damage in different devices under test showing that the die bond pads on the outer edges of the device had frequent failures than the inner die bond-pads.

to have extended up to the wirebond on the adjacent bond pad. The wire melt-off was observed in the wires connected to these bond pads.

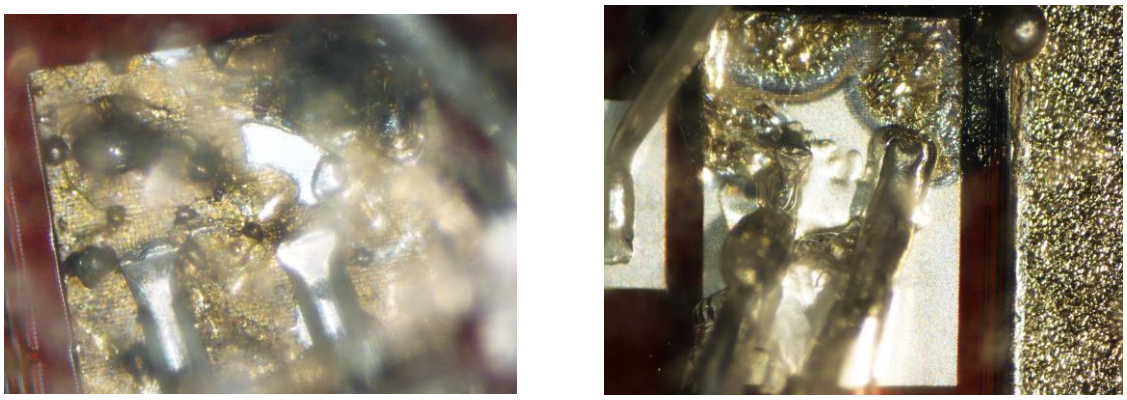
The device in Figure 5.7(c) failed short. The device has dominantly source/emitter metallization burn-off concentrated only to the bond pad. No wire related failure/degradation was observed.

The device in Figure 5.7(d) failed short. The degradation is predominant in the areas beyond the bond pads. The dielectric had different failure mechanism causing degradation, as shown in Figure 5.8(a).

Source metallization degradation was observed, as shown in Figure 5.8(b). The device itself was not damaged completely. These failures, as shown in Figure 5.8, were observed on the device dielectric itself but not in the wirebonds.

5.4.2 Degradation in 1200 V, 150 A Phase-leg IGBT Module

Three 1200 V, 150 A phase leg modules were tested with the protection circuits and monitoring system, to study the degradation behavior carefully without catastrophically



(a) (b)

Figure 5.8. (a) source metallization melt-down and (b) dielectric degradation.

damaging the device. The tests were conducted continuously on one module for 3.5 months (250000 cycles), while the other two modules were tested for 2 months and one month respectively. The upper case cover was removed on the first device under test (DUT), in order to check the degradation of encapsulant with time.

The changes in static characteristics were observed, as shown in Figure 5.9. The collector emitter voltage decreased, by as high as 20% at very high currents. This degradation was observed in all the modules that were tested.

The decreased collector-emitter voltage at high currents in the degraded modules can be attributed to higher junction temperatures in the dielectric due to solder fatigue [91]. Solder fatigue increases the thermal resistance between DBC and the baseplate and hence causes higher junction temperatures. At high junction temperatures, the on-state resistance of the device decreases. Thus, the degradation in these modules is due to solder fatigue.

Most power cycling tests in literature [65][91] have described solder fatigue initiated degradation that eventually causes wire bond failures due to increased junction temperatures.

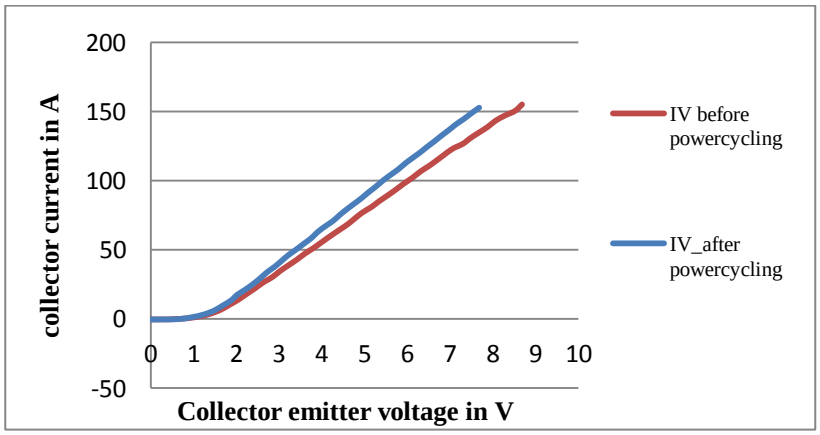


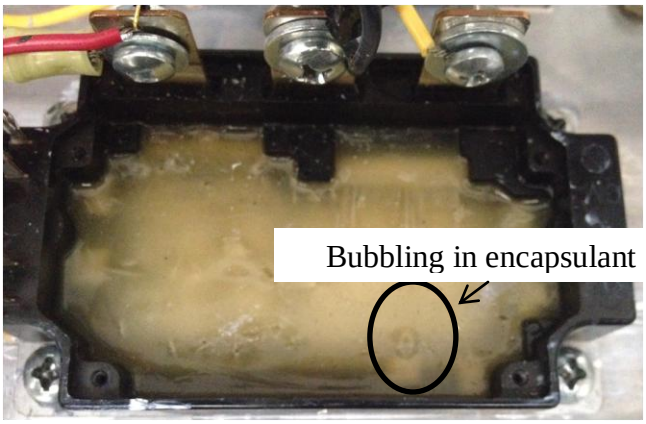
Figure 5.9. Change in static characteristics at V_{ge}=15 V after cycling for 200,000 power cycles.

However, in these tests since the static characteristics of the devices have been monitored, the impact of the degradation at various currents can be estimated. The observed degradation is permanent. Further continuation of the tests might result in wire failures.

Cracks in the encapsulant were observed after testing the device for more than a month. The number of cracks increased as the tests continued. Figure 5.10 shows the breaks in encapsulant after 150,000 and 200,000 cycles. Figure 5.10 (a) shows the bubble formation in the encapsulant before cracking. If the tests are continued, the bubble would develop into a crack. However, with less stresses, there is a possibility that the bubble might not rupture.

5.4. Summary

The failures and degradation observed in the two different modules after power cycling tests are presented. Different failures related to the wirebond and the dielectrics were observed during the testing of the H-bridge module without protection circuits. The dominant wire bond failure was wire melt down while short circuit failure on the dielectric was dominant. The degradation in the static characteristics of the high power module with protection is attributed to increased junction temperature due to solder fatigue.



(a)

(b)

Figure 5.10. Cracks in encapsulant after (a) 150,000 cycles and (b) 200,000 cycles.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this work, lifetime estimation of IGBT in STATCOM applications is presented for power factor correction, with an RC thermal model with encapsulant consideration and rainflow algorithms using equivalent temperature calculation.

Encapsulant has an impact on the overall temperature of the power device and should be considered in RC models specifically to estimate the temperatures of the wirebonds. A different number of RC based thermal model per each layer, considering encapsulant thermal characteristics, was proposed and used in this work. Higher the frequency of interest, higher are the number of RC cells required. Also, the lower the thermal time constant of the layer, lower is the number of RC cells.

Rainflow algorithms are used to count the stress-strain cycles, (amplitude and mean values) formed from the hysteresis loop. A novel rainflow algorithm for cycle counting is presented that reduces the execution time. Application of equivalent temperature calculation to semiconductor lifetime estimation using rainflow algorithm, considers the time-dependent temperature information and hence provides accurate temperature data for lifetime estimation. These algorithms were applied to power factor correction by STATCOM.

As the power factor of the load decreases, the inverter losses increase and the temperature increase is inverted parabolic in shape, with a maximum temperature rise at $\Phi = 90^{o}$. The losses in the inverter are proportional to the load current and the power factor angle. The impact of

power factor correction on the temperature of the IGBT is presented through analytical calculations, simulation and by experimental results. The lifetime of the IGBT is inversely related to the temperature. The lifetime of the IGBT is based on linear cumulative degradation assumption. For a power factor variation load profile for a building's load data, the lifetime was estimated at around 3 years. The degradation in IGBT for an arc furnace load profile using conventional rainflow algorithm is 4% less than that of the equivalent temperature algorithm.

A study on the stresses in the wirebond connecting a dielectric and DBC was simulated based on operating parameters. Square of the current, the voltage drop, the minimum temperature, and maximum temperature are the dominant parameters affecting the stresses in the wirebond.

DC power cycling tests were conducted at threshold gate voltages and near rated current in two different modules. 25% degradation in the static characteristics due to increased thermal resistance owing to solder fatigue was observed. Cracks in the encapsulant after one month long period of testing were observed for the module with the case top open. Different failures in the devices tested without protection circuits were observed. Wire melt-off was the dominant failure in most of the devices tested, followed by dielectric related failures. Most of the devices failed short. The open circuit fault in the device was observed in conjunction with wire crack and lift-off. Reactive loads result in wirebond related failure because of emitter/source wires shared by the diode and IGBT. The tests were conducted to be able to develop and validate a wirebond model. However, wire bond lift-off failures were not dominant in the failures observed in the tests. Including switching losses in the devices through AC power cycling, increasing the on-times (> 20s) [92] and better cooling methods would increase the probability of wirebond failures in IGBTs, which should be considered for future work.

6.2 Contributions

The main contributions of this work are listed below

1) Developed new rainflow counting algorithm improving the execution times of existing methods.
2) Application of time-dependent temperature calculation in rainflow algorithm to semiconductor lifetime estimation.
3) Developed different number of RC network thermal model for each layer in the semiconductor module with encapsulant.
4) Studied the impact of electrical operating parameters on the stresses in the wirebond based on finite element simulations.

6.3 Future Work

The power cycling tests conducted resulted in solder fatigue and not directly in wire bond failure. It is important to understand that it is difficult to have a single failure in the device. In many cases, the failures are a combination of two or more failure mechanisms. The developed model was for wire lift-off while the observed failures were wire melting or fusing and the dielectric related failures. The failures that were observed in the power cycling tests should be considered for model development. Including switching through AC power cycling would cause wirebond failures due to higher temperature gradients through the different layers in the module.

Setting up AC power cycling tests and studying the impact of reactive loads on device degradation should be considered for future work. DC power cycling and AC power cycling tests

would enable testing new packaging materials and can be used to test wideband gap semiconductor modules.

The development of lifetime estimation model for solder with operating parameter dependent, and the study of multi-failure initiation should be considered for future work. Most of the failures in semiconductors are caused by simultaneous degradation of more than one failure mechanism. However, in the literature, only one failure at a time is considered for modeling semiconductor lifetime. Developing an integrated failure model considering simultaneous degradation would make a significant contribution towards accurate lifetime models.

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