To the Graduate Council

I am submitting herewith a thesis written by Nicolas Williams entitled "Optimized I/O Drivers' Design, Development, and Verification for MCMs " I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this dissertation
and recommend its acceptance:

Accepted for the Council

Associate Vice Chancellor and
Dean of the Graduate School

OPTIMIZED I/O DRIVERS: DESIGN, DEVELOPMENT, AND VERIFICATION FOR MCMS

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Nicolas Jon Williams
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DEDICATION

This thesis is dedicated to my wife and daughter

Melissa Ann Williams

and

Sarah Marie Williams

whom I love with a passion that time only strengthens

ACKNOWLEDGEMENTS

There are several people to whom I am grateful for their help in completing this thesis. First, I would like to thank DARPA and the USAF for their generous financial support during the research of this thesis Dr. Don Bouldin for his support and in obtaining funding to get the ICs and MCMs fabricated and his patience during the endless fabrication cycle I especially want to acknowledge the overall contribution of my major professor, Dr. James Rochelle, whose motivation, patience, and his mentoring support throughout this research effort was instrumental to its completion I would like to acknowledge my parents for the educational opportunities they gave me

Without the sacrifices that my wife, Melissa, and daughter, Sarah, have unselfishly made, I would have never been able to complete this thesis To them, I am greatly indebted. Finally, I want to acknowledge Jesus Christ, my Savior, for making this effort possible and meaningful

ABSTRACT

The Multichip Module (MCM) package environment presents a different environment than that for which most Integrated Circuit (IC) drivers are designed The MCM-D environment was studied, modeled, and new IC drivers were designed for inter-die (IC to IC) interconnections MCM and IC traces (interconnects) were modeled in HSPICE® using lossy transmission lines From the modeling results, new IC drivers were designed for incorporation in a test system designed to study various driver-net-load combinations for different delays and signal integrity Four different test strategies were developed to measure the delay of MCM traces, and a test strategy was developed to test the need for electrostatic discharge (ESD) protection between inter-die (IC to IC) traces.

The drivers were fabricated via MOSIS on Hewlett-Packard's 0 5-μm CMOS-14B process, and they have been solder-bumped by MCNC for area-array I/O Four of these ICs were to be assembled on an MCM-D substrate being fabricated by Micro Module Systems via MIDAS This thesis describes the modeling procedure and results and the test design and layout considerations of both the IC and the MCM Testing of the IC drivers and the MCM-D environment was never completed due to problems in the ICs that were fabricated The problems with the IC are described and possible solutions are discussed

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1. INTRODUCTION

High performance computing has had the greatest need for advanced packaging due to the requirements of complex and high-density connections Multichip Module (MCM) technology is being developed to alleviate this packaging problem Soon the performance of many other types of systems will be limited by their package and it is anticipated that MCMs will appear in a wider range of systems [1]

The Air Force requires new electronic systems that are smaller and lighter to reduce the payload size and weight This results in reduced launch costs MCMs allow a reduction in the average spacing between Integrated Circuits (ICs) compared to conventional methods, and they allow multiple dies to be directly placed on a module substrate with laminated interconnect (MCM-L), ceramic interconnect (MCM-C), or deposited interconnect (MCM-D) layers [2] The main goals of MCMs are better performance by reducing the overall size of the system, reducing the signal delay between ICs, and reducing the number of external connections [1].

The advantages of MCMs:

Compared to PCBs

- Reduction in overall size and increased system speed
- Increased number of interconnections in a given area
- Large number of input/output (I/O) are possible with array I/O and flip chip technology

Compared to partitioning a large IC

- Smaller IC sizes result in the yield per IC increasing dramatically and thus reducing the overall cost of the system
- Different technologies can be mixed such as CMOS, Gallium Arsenic, and bipolar

The disadvantages of MCMs:

Compared to partitioning a large IC

- Increased delays in interconnections that are split across ICs
- Current manufacturing volumes not as high as ICs

MCMs are especially advantageous when they are combined with area-array I/O and flip-chip technology Area-array I/O is when the I/O pads of the IC are not distributed around the periphery of an IC but are distributed across the entire area of the IC as shown in Figure 1 Flip-chip technology is a type of IC connection in which small beads of solder are applied to the pads on the MCM. The IC is then flipped over and connected to the MCM through these solder bumps, see Figure 2 on page 3

The MCM-D package has the best performance compared to the MCM-L and MCM-C packages. The focus of this study will be on the comparison between an IC environment and the MCM-D environment Since most IC drivers were designed for driving an IC trace rather than an MCM trace, new drivers need to be designed to take advantage of MCM technology

Performance comparisons of IC and MCM traces with respect to delay, rise time, power, signal quality, and driver size are presented in section 2 (Interconnect Modeling) Design details and simulation results for the test IC and the test MCM are described in section 3 (Test Chip and MCM Design)

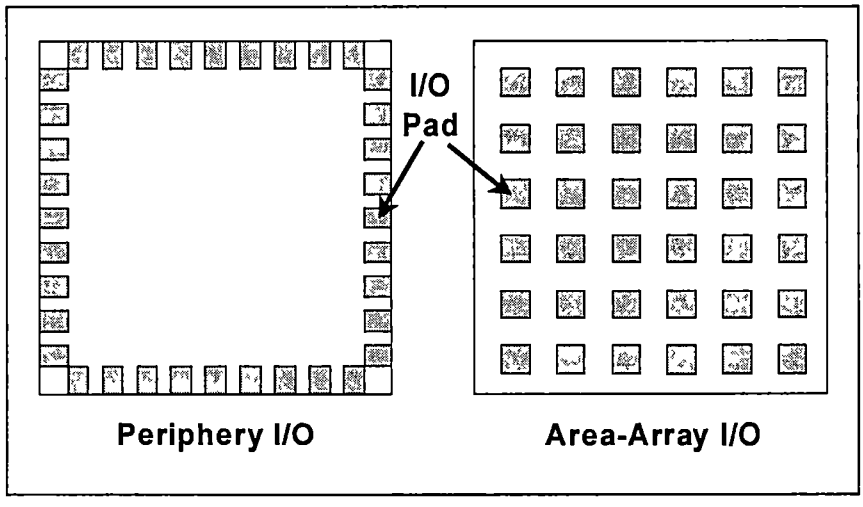


Figure 1: Types of IC I/O

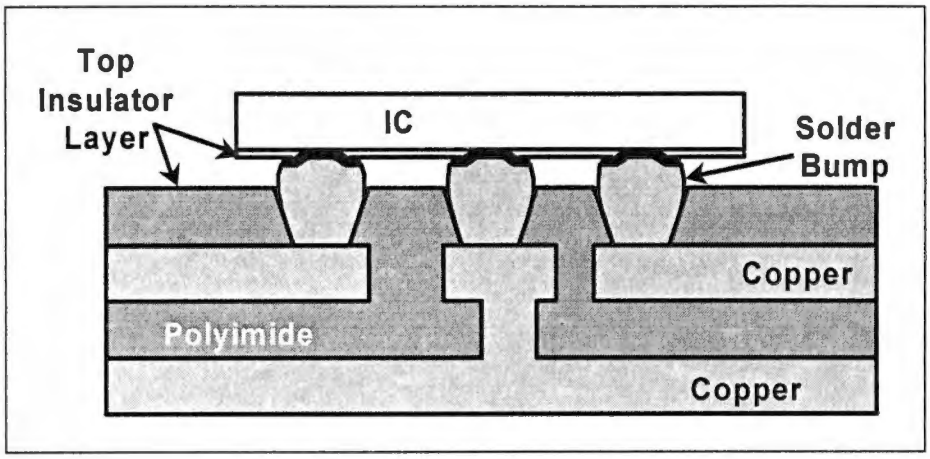


Figure 2: Flip chip solder bump connections.

2. INTERCONNECT MODELING

Case Study 1

Introduction

In case study 1, a performance comparison between IC and MCM traces is presented First, performance criteria are defined and the different process environments are described Then, modeling parameters are developed and verified Interconnect model components are described and simulation measurement techniques are discussed Simulation results are then presented.

Certain terms need to be defined to explain their specific application in this case study A trace is defined as any length of interconnect, connection, or wire residing either on an IC or on an MCM Delay in static logic circuits is typically measured as the delay between the time at which the input waveform is 50% of full value and the time at which the output waveform is at 50% of full value If one assumes ideal symmetrical switching of all gates at Vdd/2, then the total delay from one node to another is just the sum of the 50%-50% delay of all of the intermediate nodes The time required for a signal to change from 10% of full value to 90% of full value is typically defined as the rise time In this study, all delays that are presented are 50%-50% delays and all rise and fall times that are presented are 10%-90% rise and fall times.

MCM Process Description

Micro Module System's MCM-D process consists of an aluminum substrate with 2 copper interconnect layers, 2 copper power planes, and a copper pad layer. Figure 3 on page 5 shows a cross-section of an MMS MCM and its layers Polyimide is used as the dielectric ($\varepsilon_r = 3\ 5$), and MMS supports trace widths of 16 μm with 50 μm, 62 μm, and 75 μm pitches The top interconnect layer was used for all MCM traces (Y-signal layer) in this case study Appendix D on page 75 contains the MMS process specifications

IC Process Description

The Hewlett-Packard 0 5 μm CMOS-14B process used in this study and for the fabrication of the test ICs has a minimum transistor gate length of 0 6 μm, a single polysilicon layer, and three aluminum metal

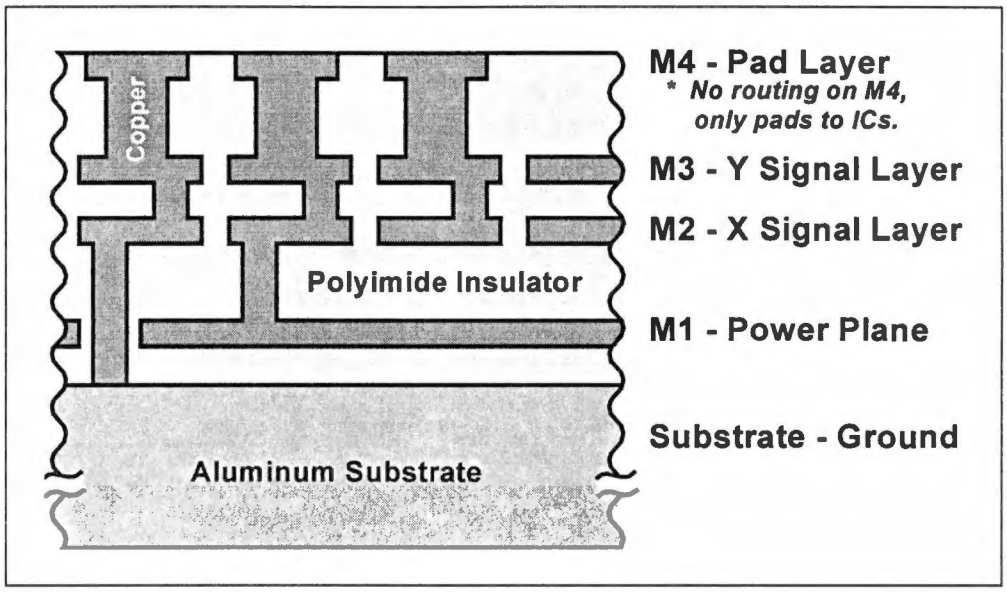


Figure 3: MMS MCM-D process cross section.

interconnect layers. Only the top metal layer was used for the interconnect case study. The geometry of an IC trace in the HP process is shown in Figure 4 on page 6. Appendix E on page 78 contains the HP process specifications and the parametric test results for a single wafer run.

Transmission Line Parameters

To model the IC and MCM traces as lossy transmission lines, the electrical properties of the trace need to be measured or calculated, specifically the resistance, capacitance, and inductance per unit length. The capacitance and inductance are measured between the trace and the ground plane. The delay of a signal through a trace is affected by the material of the trace, its geometry, its length, and the dielectric material around the trace. The geometry of a rectangular trace is shown in Figure 5 on page 6.

The first order "parallel plate" capacitance between the rectangular trace and the ground plane is shown as Equation 1 on page 7. The capacitance of the wire increases with the width of the wire but decreases the farther the wire is from the ground plane. This equation does not incorporate the effects of fringing. Fringing effects can be modeling as the combination of a parallel plate and a cylindrical wire with a diameter of H_{int} [3] and the equation incorporating second order fringing effects can be found in [4].

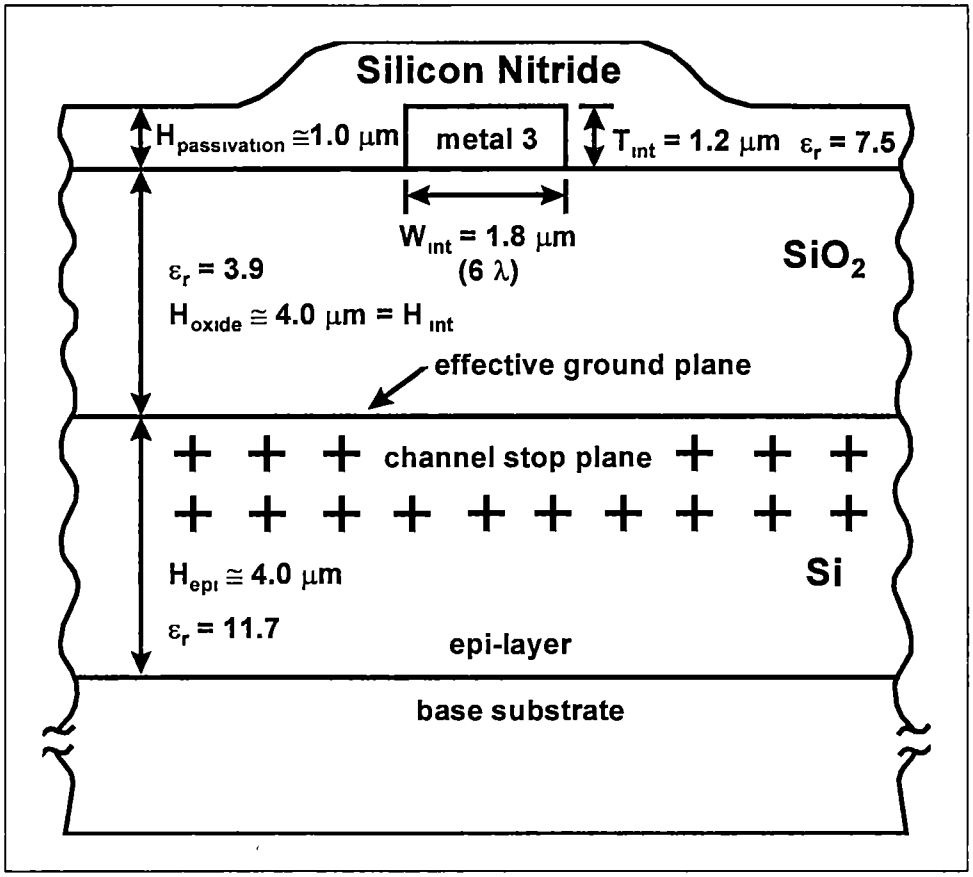


Figure 4: HP's IC trace geometry

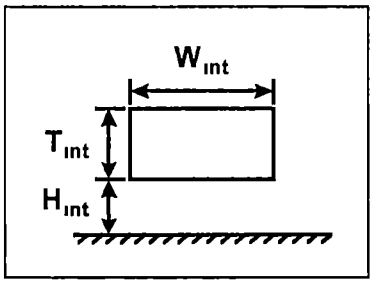


Figure 5: Trace geometry

$$C_{int} = \varepsilon_{ox} \cdot \frac{W_{int} \cdot L_{int}}{H_{int}} \quad (1)$$

W_{int} = the width of the wire.
L_{int} = the length of the wire
H_{int} = the distance between the wire and the ground plane
ε_{ox} = the dielectric constant of the material between the wire and the ground plane

The resistance of the trace is defined in equation 2 The resistance of the trace decreases as the trace gets wider and thicker but increases with its length There is a trade-off between the resistance and capacitance of the trace with respect to its width As the width of a trace increases, its resistance decreases, but its capacitance increases Because of this tradeoff, the delay of a trace is best improved by increasing its distance from the ground plane and/or by increasing its thickness If fringing effects are included, the capacitance of a trace increases with thickness [4], but the rate of increase in capacitance with respect to trace thickness is much slower than the rate at which the resistance decreases with the trace's thickness as in Figure 6 on page 8

$$R_{int} = \rho \cdot \frac{L_{int}}{W_{int} \cdot T_{int}} \quad (2)$$

W_{int} = the width of the wire
L_{int} = the length of the wire
T_{int} = the thickness of the wire
ρ = the resistivity of the wire, a material constant

The transmission line parameters needed for modeling are the resistance, capacitance, and inductance per unit length of the trace With HSPICE®, the transmission line parameters can be specified directly or HSPICE can calculate them by defining the geometry of the trace. HSPICE calculates the electrical parameters from closed form expressions for transmission line modeling for a limited number of physical geometries [8] These expressions have been optimized for typical geometries used in ICs, MCMs, and PCBs via measurements and comparisons with several different electromagnetic field solvers [8] After the

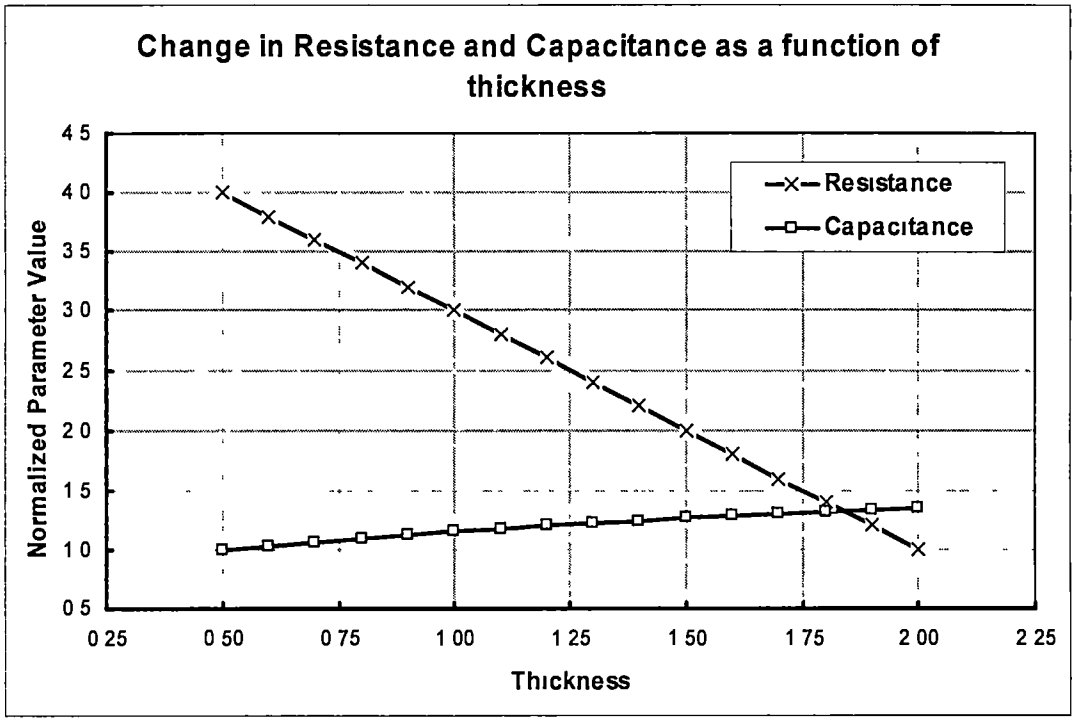


Figure 6: Trace capacitance and resistance as a function of thickness

electrical parameters are specified or calculated, HSPICE models a lossy transmission line as a distributed series of RLC circuits

Since no measured electrical transmission properties were available for the HP CMOS-14B process, the physical geometry method was used to allow HSPICE to calculate the transmission line parameters of the IC trace The IC trace was modeled as a 1 2 μm thick aluminum conductor 4 μm above an ideal ground plane (see Figure 4 on page 6).

To verify that the electrical parameters calculated by HSPICE were realistic, capacitance estimates were calculated using various equations from the interconnect literature Equation 3 is the modified parallel plate capacitance equation and it was used to calculate the capacitance per length for a trace with the uniform dielectric material surrounding the trace [4]

Fooks and Zakarevicius [5] derived a capacitance expression for a microstrip trace over a dielectric with air above the trace The IC trace actually has a thin silicon nitride layer above it and does not exactly

fit the definition of a microstrip Although thin silicon nitride has a higher dielectric constant (ε_r = 7 5), its effect was assumed to be minimal because of its thickness. To be conservative, the capacitance of the trace was calculated from the uniform dielectric case The details of the capacitance calculation for a microstrip are shown in Appendix A on page 72.

$$C_{int} = \varepsilon_{ox} \cdot \left(\frac{W_{int}}{H_{int}} - \frac{T_{int}}{2 \cdot H_{int}} + \frac{2 \cdot \pi}{\ln\left[1 + \frac{2 \cdot H_{int}}{T_{int}} \cdot \left(1 + \sqrt{1 + \frac{T_{int}}{H_{int}}} \right) \right]} \right) \quad (3)$$

H_{int} = distance between the trace and the ground plane (4.0 μm)
W_{int} = width of the trace (4 8 μm)
T_{int} = thickness of the trace (1 2 μm)
ε_{ox} = dielectric Constant (3 9 (8 85 10-14) Farad/cm)

Table 1 on page 10 shows the capacitance calculated for the uniform dielectric case and the microstrip case From the table, the capacitance calculated from the literature agrees with the capacitance calculated by HSPICE's Physical Transmission Model, which gives us the confidence to use the HSPICE calculated transmission line parameters The capacitance of the trace increases almost linearly at 0.1 pF/cm for each micron of width This results in only a 60% difference in capacitance between 1 8 μm wide IC trace and the 14 4μm wide IC trace The difference in resistance is more than 680% indicating that the resistance is going to have a more dominating effect than the capacitance on performance

After the case study, Phillips Labs calculated the capacitance using a specialized field solver that takes into effect the silicon nitride layer The capacitance for a 1 8 μm wide IC trace was calculated at 1 47 pF/cm This is 39% more than the uniform dielectric case and indicates that the silicon nitride layer has a greater effect than first assumed Although the capacitance of the trace that was calculated from the uniform dielectric case is less than the actual capacitance, it resulted in a more favorable bias towards the IC traces compared to the MCM traces.

Table 1: IC capacitance (pF/cm)

	W = 1.8 μm	W = 4 8 μm
HSPICE Physical Transmission Model (Uniform Dielectric all SiO_2)	0 93	1 27
Modified Parallel Plate (Ref [3], Eq 4 5)	0 90	1 16
HSPICE Physical Transmission Model (Microstrip air and SiO_2)	0.65	0.95
Microstrip Equations (Ref [5], Ch 3 & 4)	0 66	0 95

MMS supplied the measured electrical properties for the signal layers in their MCM-D process, so no calculation of MCM electrical parameters was needed Table 2 on page 11 shows the transmission line parameters for the IC and MCM traces The inductance is approximately the same for the IC (W = 14 4 μm) as for the MCM (W = 16.0 μm) The capacitance of the MCM is about half the value of the IC This difference is because the Y-signal trace of the MCM is farther away from the ground plane (H = 23 5 μm) than the IC trace (H= 4 0 μm) The main performance difference results from the order of magnitude difference between resistance of the IC and MCM This difference results in higher losses in the IC trace and lower 3dB frequencies in its response The main reason for the differences in the resistances is that the MCM trace is about 4 0 μm thick while the IC trace is about 1 2 μm thick and the resistance of the trace is inversely proportional to its thickness The material of the trace also was a reason for the difference The material used in the IC for traces is aluminum while the material used in the MCM is copper Aluminum has a bulk resistivity of 2 8 μΩ cm while copper has a bulk resistivity of 1 7 μΩ cm, which is a reduction of 60% of bulk resistance Currently, most IC process use copper instead of aluminum but the MCM traces are still thicker than the IC traces

Transistor Model

The transistor models used for the case study were level 3 and level 13 model extractions of a past HP fabrication run (N56S run) [7] A simple two-stage driver was modeled to verify if the level 3 model parameters were accurate enough for the case study Figure 7 on page 11 shows the two-stage driver used to verify the transistor models The circuit was simulated with HSPICE using the level 3, level 13, and proprietary internal HP models The results were compared and were nearly identical Figure 8 on page 12 shows the extracted SPICE level 3 transistor model parameters that were used

Table 2: IC and MCM transmission line parameters

	R Ω/cm	C pF/cm	L nH/cm	Z_o Ω
CMOS14TB Metal 3[†]				
W = 1 8 μm - 6 λ	203 0	0 93	6 05	96
W = 4 8 μm - 16 λ	76 0	1 27	4 77	71
W = 14 4 μm – 48 λ	26.0	2 25	3 07	37
MMS Y-signal[‡]				
W = 16 μm	2 4	1 20	3 50	58

[†] These values were predicted by HSPICE physical transmission line model assuming 1 2 μm thick Al conductor, 4 μm above an ideal ground plane. Conductor resistivity was adjusted to obtain 0 037/square sheet resistivity to agree with CMOS14TB process specifications [7]

[‡] Micro Module Systems D500 process specifications [6]

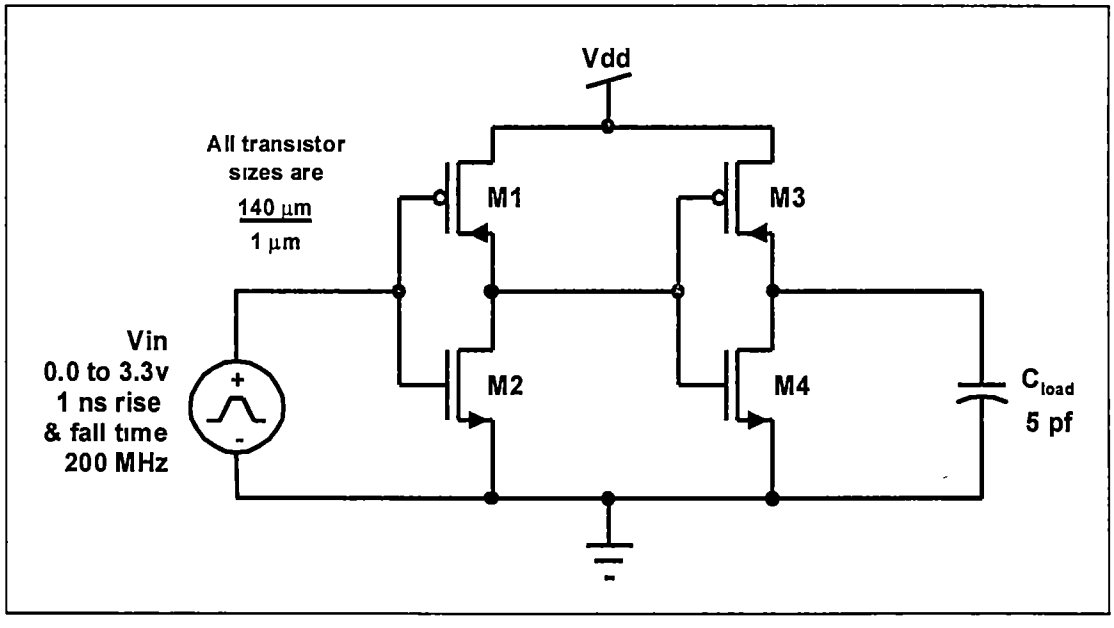


Figure 7: Transistor model verification circuit

```
* N56S SPICE LEVEL3 PARAMETERS

 MODEL CMOSN NMOS LEVEL=3 PHI=0 700000 TOX=1 0000E-08 XJ=0 200000U TPG=1
+ VTO=0 7812 DELTA=2 4510E-01 LD=4 0510E-08 KP=1 8847E-04
+ UO=545 8 THETA=2 5170E-01 RSH=2 1290E+01 GAMMA=0 6200
+ NSUB=1 3810E+17 NFS=7 0710E+11 VMAX=1 8610E+05 ETA=2 2420E-02
+ KAPPA=9 6720E-02 CGDO=3 66E-10 CGSO=3 66E-10
+ CGBO=4 0161E-10 CJ=5 4E-04 MJ=0 6 CJSW=1 5000E-10
+ MJSW=0 32 PB=0 99
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 4 1360E-07

 MODEL CMOSP PMOS LEVEL=3 PHI=0 700000 TOX=1 0000E-08 XJ=0 200000U TPG=-1
+ VTO=-0 9197 DELTA=2 4830E-01 LD=6 7120E-08 KP=4 4546E-05
+ UO=129 0 THETA=1 7800E-01 RSH=3 4290E+00 GAMMA=0 5230
+ NSUB=9 8260E+16 NFS=6 4990E+11 VMAX=3 0560E+05 ETA=1 7820E-02
+ KAPPA=6 3410E+00 CGDO=3 66E-10 CGSO=3 66E-10
+ CGBO=4 2772E-10 CJ=9 3191E-04 MJ=0 51 CJSW=1 5E-10
+ MJSW=0 193 PB=0 95
* Weff = Wdrawn - Delta_W
The suggested Delta_W is 4 6180E-07
```

Figure 8: SPICE level 3 transistor models

Having validated the transistor models, the transmission line algorithms for three different SPICE simulators were compared This was done to get a better understanding of transmission line modeling and to make sure that the simulator produced realistic results. Figure 9 on page 13 shows the system diagram of the circuits used in the transmission line comparison and the interconnect performance study The absolute error tolerance for voltages was set to $5x10^{-8}$, the relative error tolerance for voltages was set to $5x10^{-5}$, and the maximum time step was set to 2 ps After these settings, very similar results were obtain from the Berkley SPICE version 3f4, PSPICE version 6 0 (Jan 1994), and HSPICE version 93A circuit simulators

Operating Parameters

A 200 MHz clock with a 1 ns risetime was used as the drive signal for the case study. HSPICE was used to simulate the system with traces being modeled as lossy transmission lines and transistors being modeled with level 3 models The IC drivers and receivers were modeled without any electrostatic discharge (ESD) protection circuits

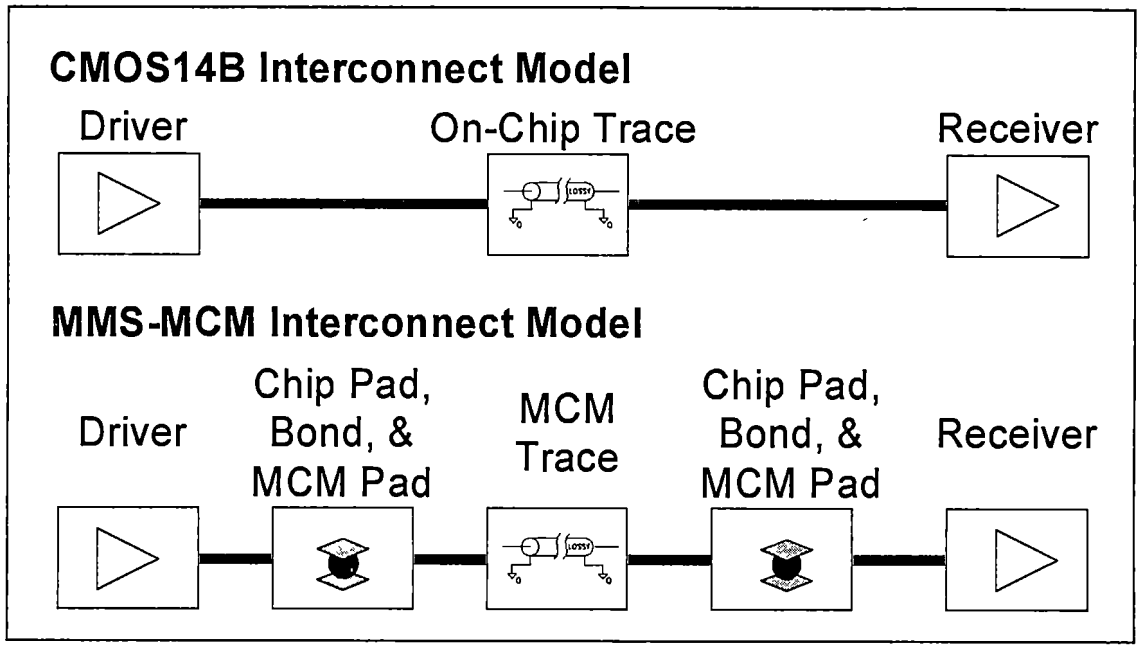


Figure 9: System diagram for the interconnect response study

Interconnect Model Components

Driver Model

The driver used for the interconnect modeling study is a simple two-stage tapered driver A tapered driver is an even number of inverters connected in series with each inverter having larger transistors than the inverter before it The geometric growth rate of each inverter is the taper factor Jaeger [8] and Mead and Conway [9] derived the optimum taper factor with respect to the propagation delay as $e \approx 2\ 72$ The optimum taper factor derived with respect to the power-delay product was 4 25 [10] A taper factor of 3 0 was chosen to correspond more to Jaeger's findings, because propagation delay was one of the main goals of the case study

Figure 10 on page 14 shows the driver circuit used in the case study This is a 1x driver that has a taper factor of 3, e g , transistors M3 and M4 are 3 times larger than transistors M1 and M2. For a driver of size Nx, transistors M1 and M2 have M=3 N and transistors M3 and M4 have M=9 N, i e , for a 3x driver, transistors M1 and M2 have M=9 and transistors M3 and M4 have M=27

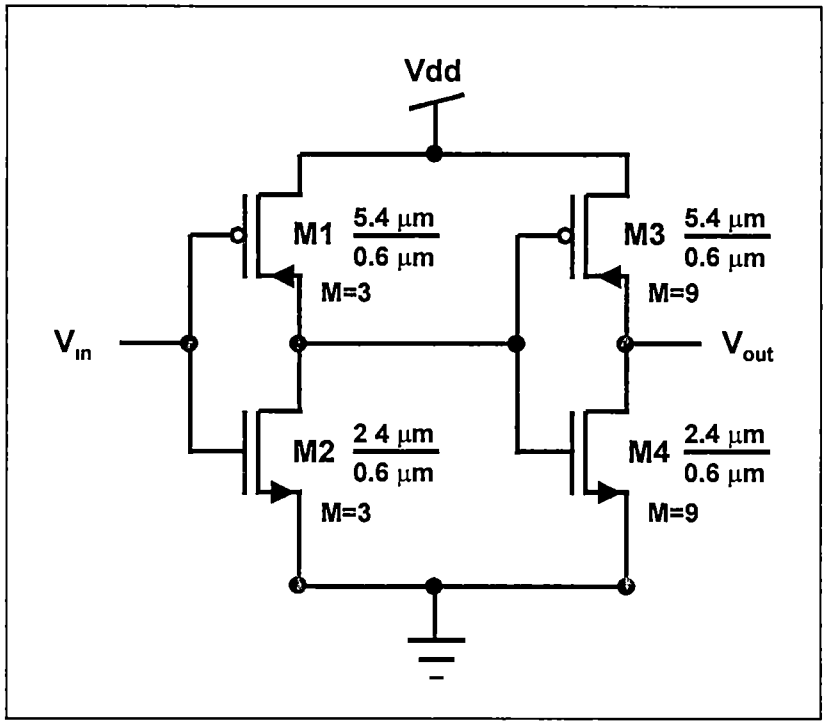


Figure 10: Tapered driver circuit used in interconnect study

Pad and Bond Model

The pad and bond model is shown in Figure 11 on page 15 The IC pad is represented as a single capacitor, which is the plate capacitance between the top metal layer on the IC and the substrate for a 100 µm by 100 µm square pad Appendix B shows the calculations for the pad capacitance for both the IC and the MCM The MCM pad model is also represented as a single capacitor, which is the plate capacitance between the pad layer and the power plane layer on the MCM for a 100 µm by 100 µm square pad The solder bump model consists of an inductor and a split capacitor This model was taken from Franzon's book [1] along with rule of thumb values for the inductance and capacitance values. The solder bump bond offers two orders of magnitude reduction in bond inductance compared to a wire bond The resistance of the bond was not modeled because of its low magnitude and because the bond was dominated by its inductance and capacitance values Any effects of the vias from the pad layer to the Y-signal layer of the MCM were neglected

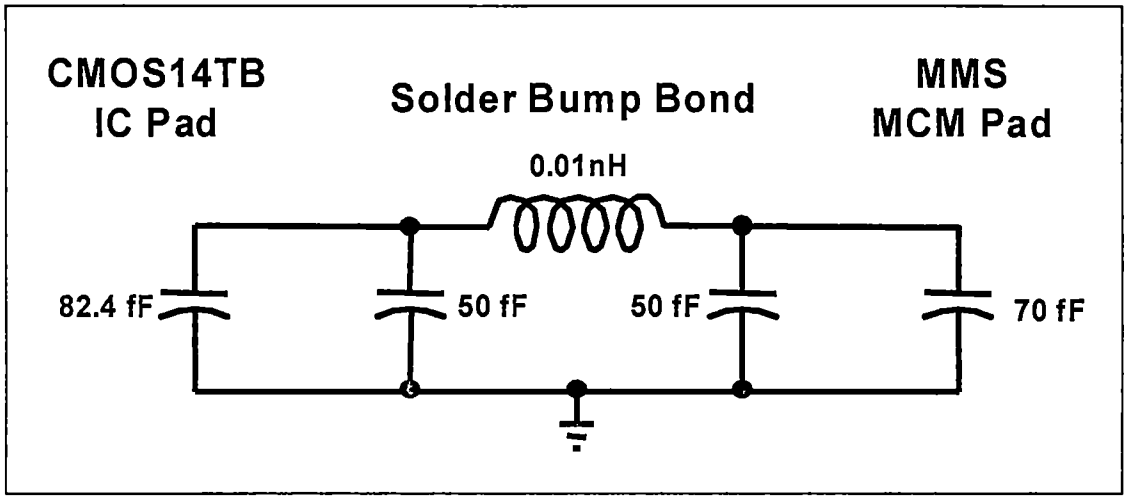


Figure 11: Pad and bond model

Receiver Model

The receiver model used in the case study is shown in Figure 13 on page 16, which is a basic inverter The inverter represents the typical input transistor size found in the EPOCH standard cells For the study, it was assumed that the drivers that were designed would be used with EPOCH standard cells The inverter represents a typical single load that the driver needs to drive

Simulation Measurement Techniques

To extract measurements for delay and risetime, the HSPICE command **.MEASURE** was used There are five fundamental measurement modes that can be used during DC, AC, and transient analyses [9]

- Risetime, Falltime, and Delay
- Average, RMS, Minimum, Maximum, and Peak to Peak.
- Find-When
- Parameter Evaluation
- Relative Error.

Figure 12 on page 16 gives examples of the commands typically used to measure simulated delay and risetime These **.MEASURE** commands can compute a differential measurement of time (Transient), voltage (DC), or frequency (AC) between a trigger value and a target value *Risedelay1* is the delay that is measured as the difference in time between signals V(1) and V(7) when they are both rising for the first

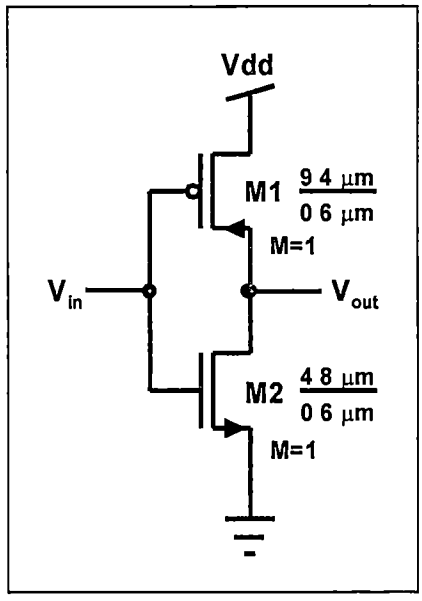


Figure 13: Receiver circuit

```
MEASURE TRAN risedelay1 TRIG v(1)  RISE=1 VAL=1 65v TARG v(7)  RISE=1 VAL=1 65v
MEASURE TRAN risetime1 TRIG v(7)  RISE=1 VAL=0 33v TARG v(7)  RISE=1 VAL=2 97v
MEASURE TRAN falldelay1 TRIG v(1)  FALL=1 VAL=1 65v TARG v(7)  FALL=1 VAL=1 65v
MEASURE TRAN falltime1 TRIG v(7)  FALL=1 VAL=2 97v TARG v(7)  FALL=1 VAL=0 33v
```

Figure 12: HSPICE measurement commands

time and at the time when they both become 1 65 v (50% of the supply voltage) *Risetime1* is the risetime that is measured as the difference in time between when the signal V(7) would reach 0.33 v (10% of the supply voltage) as the signal rises for the first time and when the signal V(7) would reach 2 97 v (90% of the supply voltage) as the signal rises for the first time The **.MEASURE** command is very powerful because it can also measure a value after a certain time or it can measure a value after another signal has reached a certain value or sequence

HSPICE computes the total power dissipated in the circuit by summing the power dissipated in the active devices, passive devices, independent sources, and dependent sources The power dissipated in each device is computed by multiplying the voltage across the element and its corresponding branch current HSPICE then computes the average power by calculating the area under the total power dissipation curve and dividing by the periods of interest (usually the length of the transient analysis) The average power of

the system can be calculated in HSPICE by including the **.MEASURE AVG POWER** command The average power computed by HSPICE was validated by calculating the average power manually by including a resistor and capacitor between Vdd and the circuit under test (CUT) as shown in Figure 14 After the system has settled to steady state, the current through the resistor approaches the average current used by the CUT and can be multiplied by Vdd to get the average power Figure 15 on page 18 shows the current through the resistor R1 The resistor value is small enough that there is negligible attenuation of Vdd and the resulting time constant of the integrator is 10 ns The average current measured through the resistor was 7 5 mA, resulting in an average power dissipated of 24 8 mW HSPICE computed the average power dissipated at 23 3 mW The percent error is only 6 11%, which validates HSPICE's computed average power to first order

Simulation Results - IC

The CMOS-14B interconnect model described by Figure 9 on page 13 through Figure 13 on page 16 has been simulated over a range of transmission line lengths, trace widths, and driver sizes, using a 200 MHz clock signal with a 1 ns rise time and fall time.

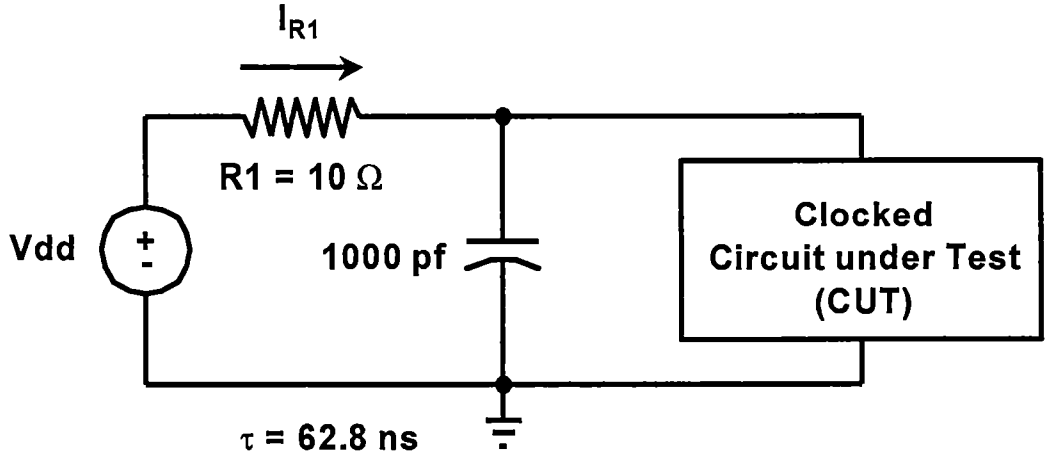


Figure 14: Circuit for measurement of total power consumption of a circuit

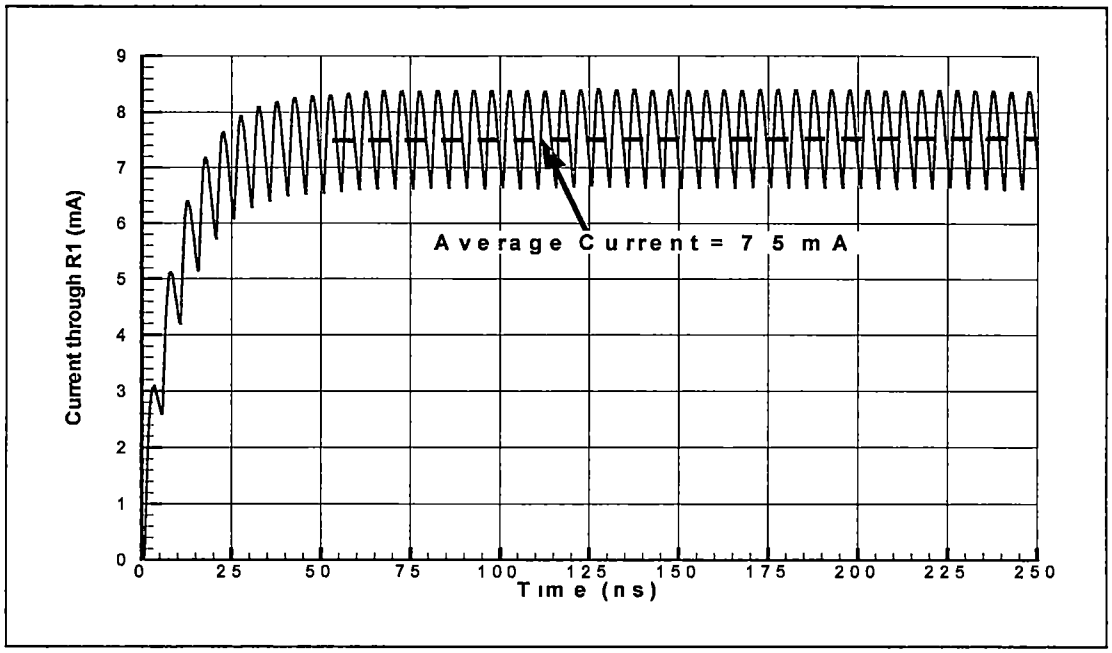


Figure 15: Average current used in the power consumption measurement

Figure 16 on page 19 shows the signal response at the input of the receiver for a 1 8 µm wide trace on an IC For the 4 cm long trace with a width of 1 8 µm, the 1x through 4x driver cannot fully drive the signal This is true for any size driver The resistance of the trace is too large (203 0 Ω/cm), which results in an effective time constant for the trace being less than the clock frequency Using a simple distributed RC analysis (see appendix C on page 74), the effective time constant of the 1 8 µm wide trace is 7.8 ns, which is greater than the pulse width of the clock even if the risetime was zero (2 5 ns) The impedance of the trace doesn't allow the line to charge up to Vdd during the clock pulse Figure 17 on page 20 and Figure 18 on page 20 show that the time required to charge the trace is not dependent on Vdd or the risetime, but is dependent on the impedance of the trace

The on-chip interconnect response for a 4 8 µm wire width is shown in Figure 19 on page 21 The impedance of this trace is still so large that the 4x driver cannot fully charge up the trace during the clock cycle. The effective time constant is 4 0 ns using a simple distributed RC analysis, which is greater than the pulse width The signal will charge the line as much as it can during each clock cycle and after a few clock cycles, the signal will oscillate around Vdd/2 (1 64 volts) The signal will swing about 3 0 volts from 0 15 volts to 3 15 volts This is enough to switch the receiver but its noise margin is reduced by 0 3 volts

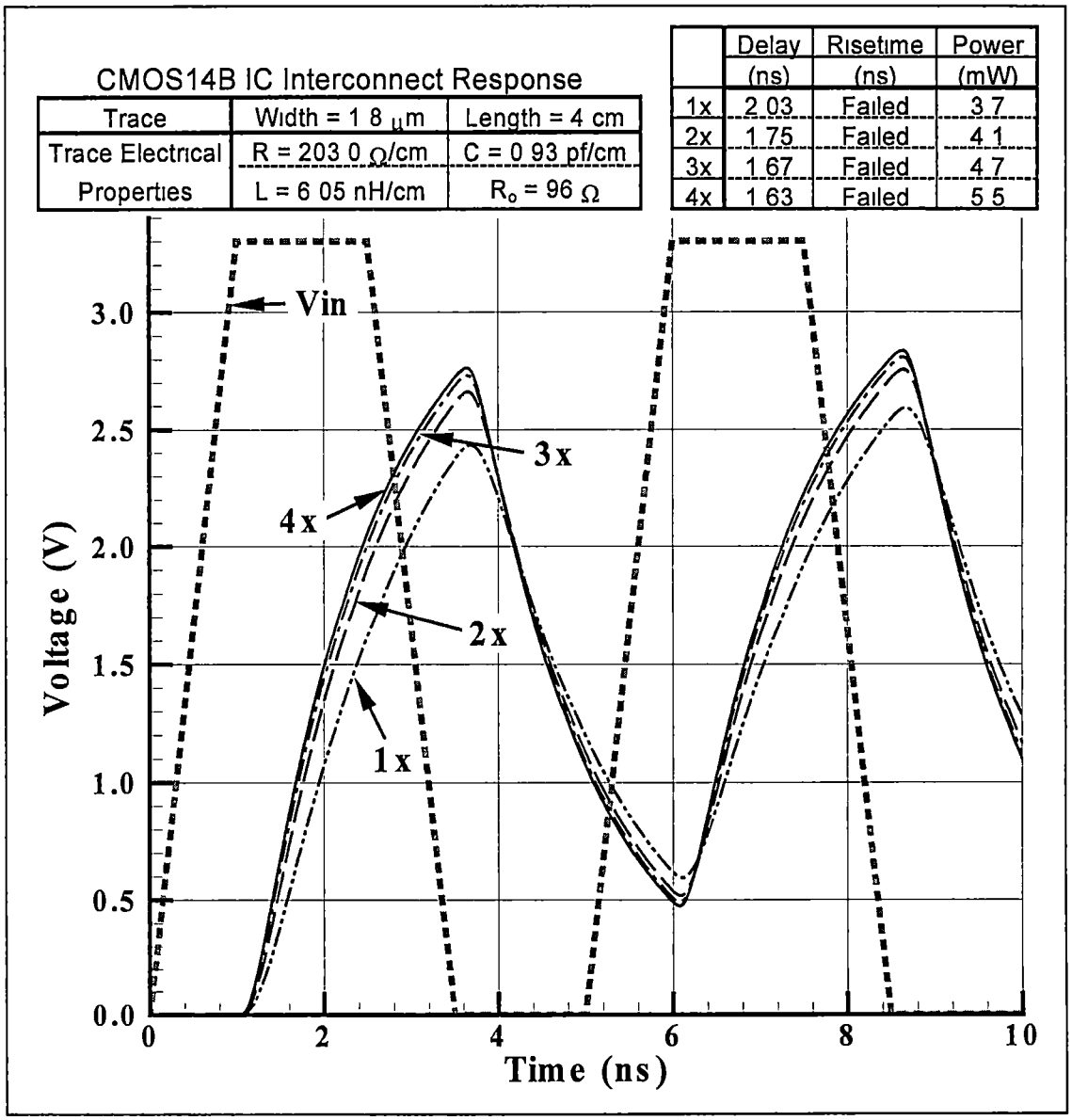


Figure 16: IC interconnect responses for different driver sizes of a 1 8 μm wide trace

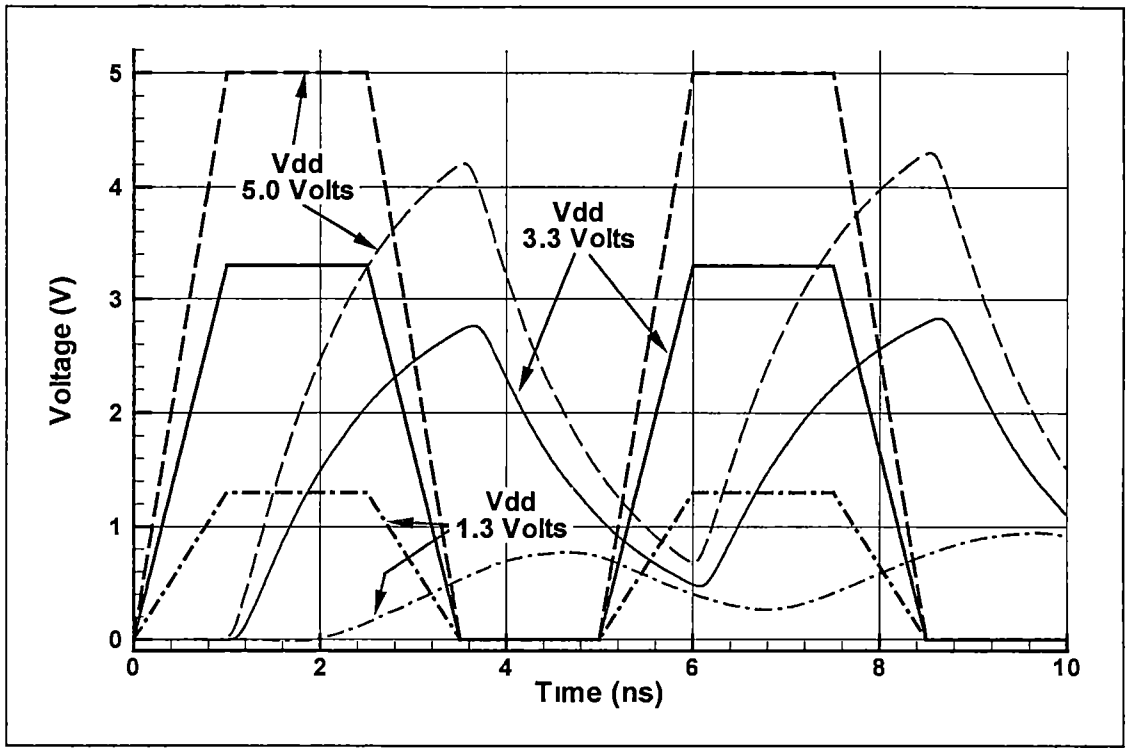


Figure 17: IC interconnect response for a 1x Driver and a 1 8 μm wide trace with a 1 ns risetime and with varying Vdd

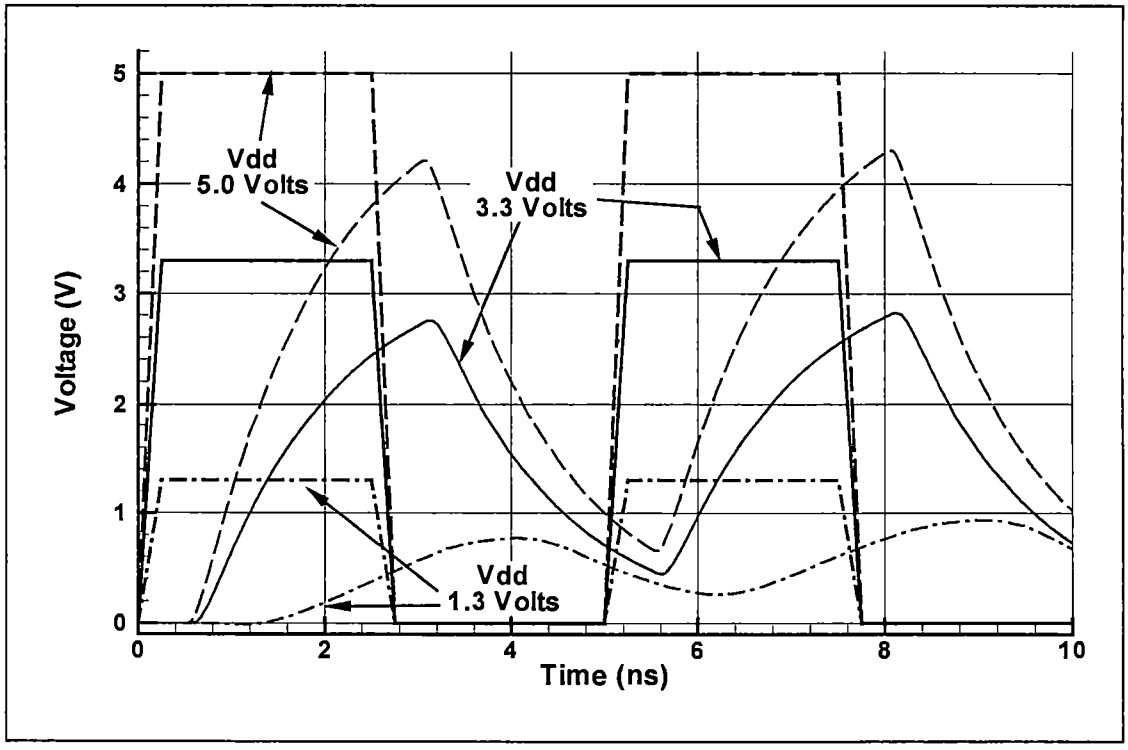


Figure 18: IC interconnect response for a 1x Driver and a 1 8 μm wide trace with a 0 25 ns risetime and with varying Vdd

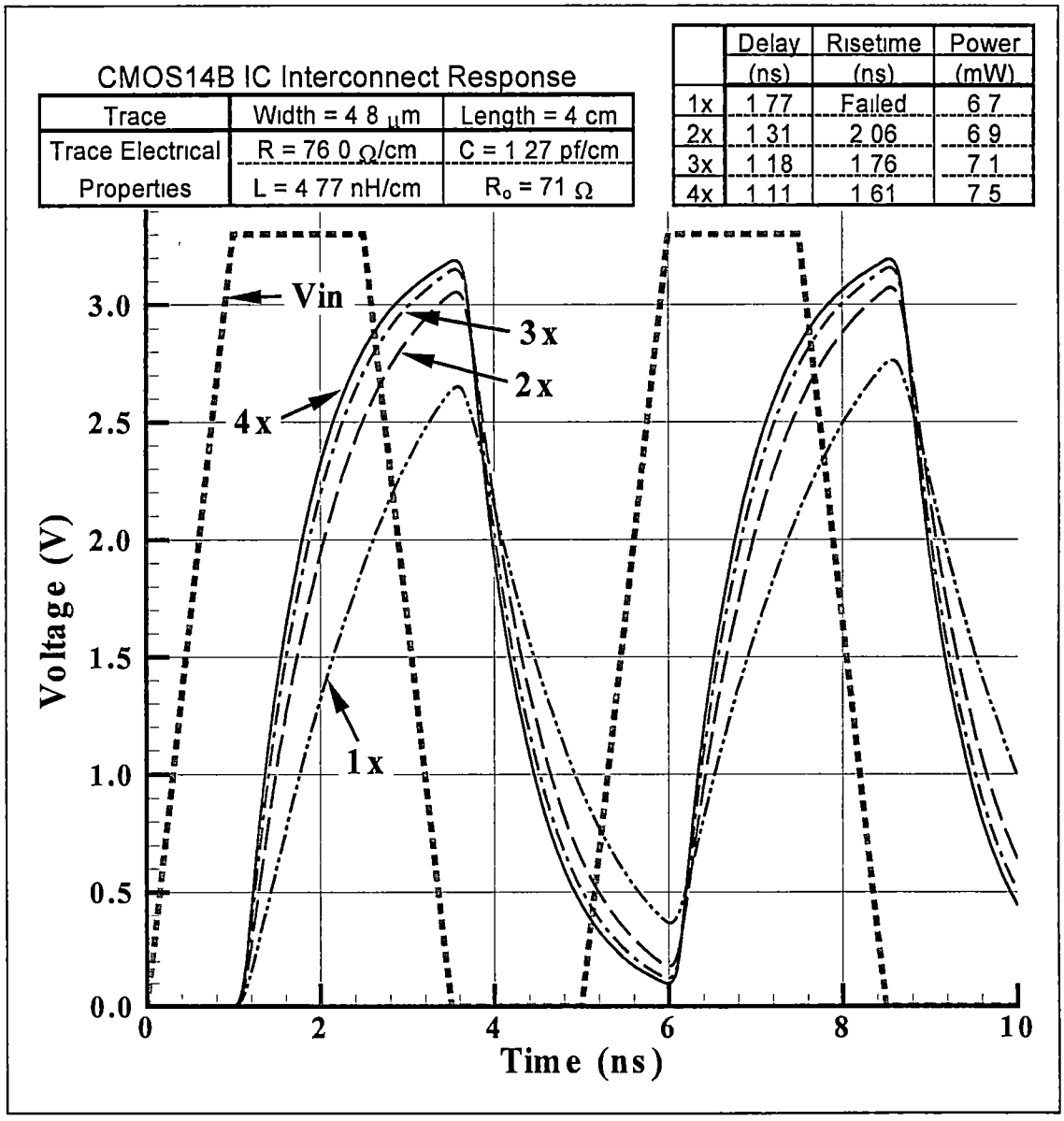


Figure 19: IC interconnect responses for different driver sizes of a 4 8 μm wide trace

Figure 20 on page 23 shows the on-chip interconnect response for a 14 4 μm wire width, which is only 11% less than the width of the MCM trace The 6x driver has a large enough driving force to drive the 4 cm trace while the 3x and 1x driver do not For a 4 cm trace, a driver size of 6x or greater is needed

Increasing the driver size does not always decrease the delay of a trace The delay of a trace is affected by two limitations the current driving capability of the driver and the impedance of the trace Figure 21 on page 24 through Figure 23 on page 24 show the signal response of the on-chip interconnect for 1 8 μm, 4 8 μm, and 14 4 μm wire widths driven by a 100x driver The 100x driver cannot fully charge up the 1 8 μm and 4 8 μm wide traces A 100x driver or any size driver cannot charge up those traces because the response of the system is limited by the resistance of the trace The resistance of the trace is so large that it limits the current available to charge and discharge the capacitance and inductance of the trace In the case of the 1 8 μm and 4 8 μm wide traces, the impedance of the trace dominates the delay One approach to solve this problem is to insert a buffer periodically along the trace to reduce its length to a length that can be driven effectively. Buffer insertion was not considered during this study because buffers can only be inserted for an IC trace and not an MCM trace Once the driver is large enough to charge the trace, increasing its size does not dramatically decrease delay times For the 100x driver, the size of the driver is 16 5 times larger than the 6x driver but the delay was decreased only 27% to 0 72 ns

Simulation Results - MCM

The MCM interconnect response at the input of the receiver for a 1x driver with trace lengths from 0 5 cm to 4 0 cm is shown in Figure 24 on page 25 The 1x driver can drive an MCM trace up to 1 0 cm For the 4 0 cm trace, the flattening of signal at 1 2 ns and 0 8 volts is the result of reflections on trace due to its lossy transmission characteristics Improper termination causes reflections to be transmitted back down the trace and causes delays in the signal If the reflection occur before the signal gets to the switching voltage (1 65 volts), then these reflections will have a significant effect on delay

Figure 25 on page 26 shows the MCM interconnect response for a 2x driver at the input of the receiver for trace lengths from 1 0 cm to 4 0 cm The 2x driver can drive an MCM trace up to 2.0 cm in length without appreciable degradation of signal quality and distortion due to reflections Transmission reflections can be seen in the response of the 3 0 cm and 4.0 cm trace lengths.

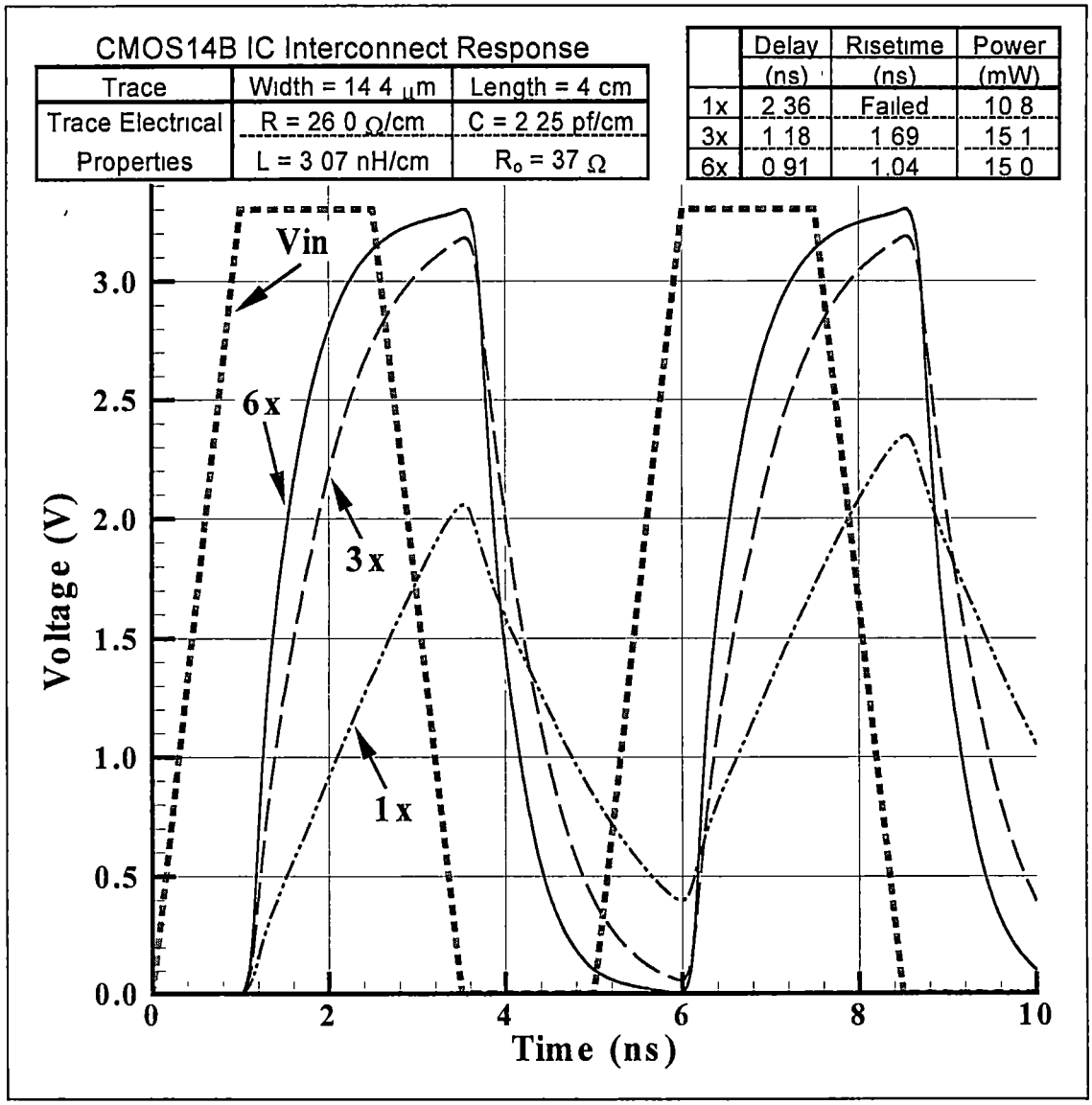


Figure 20: IC interconnect responses for different driver sizes of a 14 4 μm wide trace

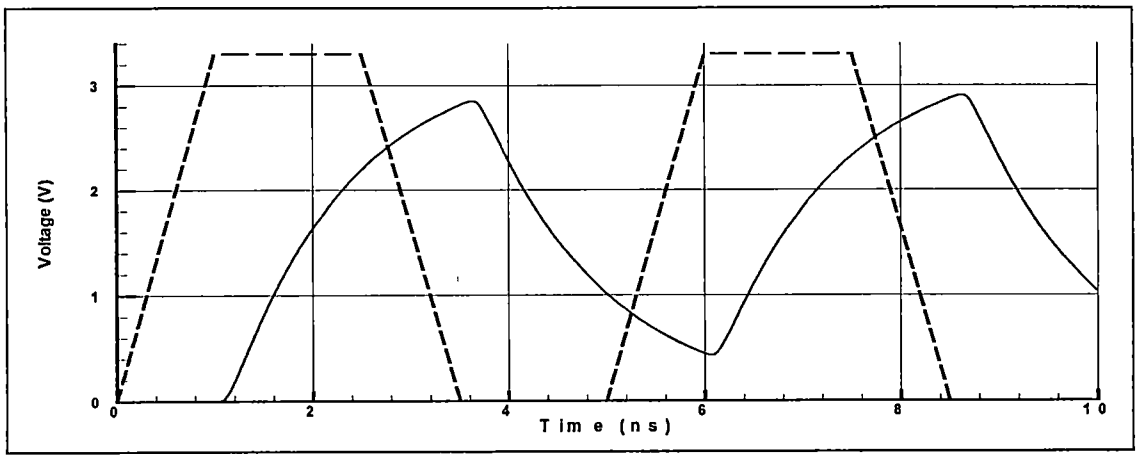


Figure 21: IC interconnect response for a 100x Driver and a 1 8 μm wide trace.

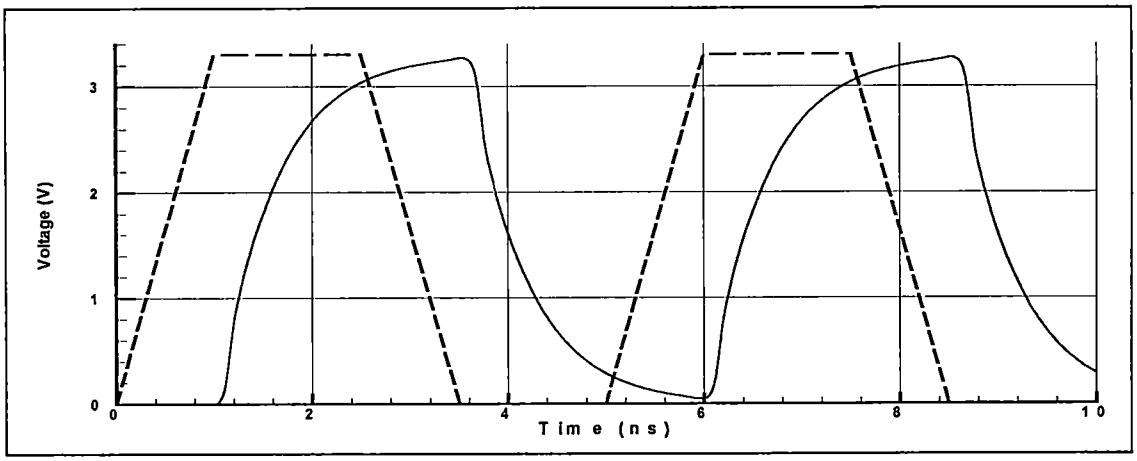


Figure 22: IC interconnect response for a 100x Driver and a 4 8 μm wide trace

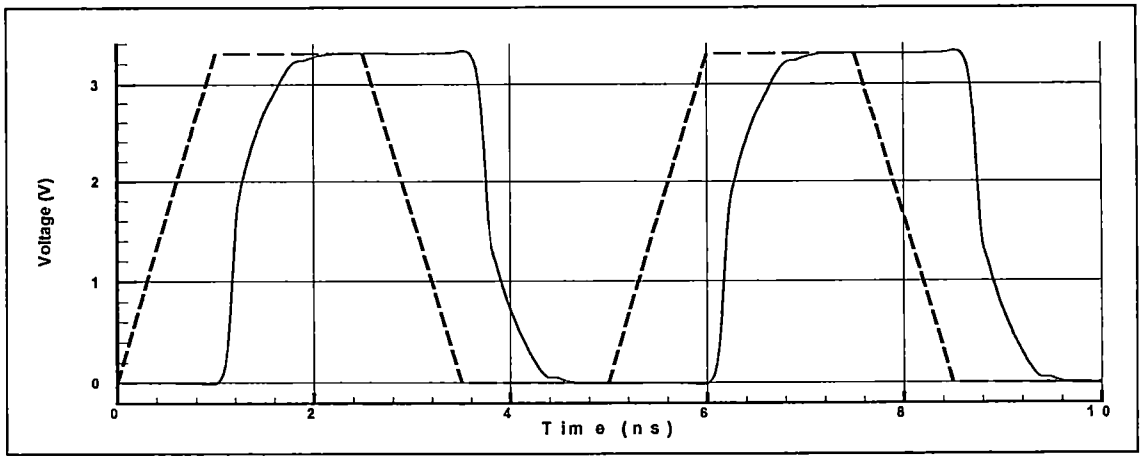


Figure 23: IC interconnect response for a 100x Driver and a 14 4 μm wide trace

MMS MCM Interconnect Response

Trace	Width = 16 0 μm	1x Driver
Trace Electrical Properties	R = 2 4 Ω/cm	C = 1 2 pf/cm
	L = 3 5 nH/cm	R_o = 58 Ω

Length (cm)	Delay (ns)	Risetime (ns)	Power (mW)
0 5	0 58	0 55	3 5
1 0	0 70	0 79	4 8
2 0	0 93	1 29	7 4
3 0	1 14	1 80	9 5
4 0	1 35	2 36	10 9

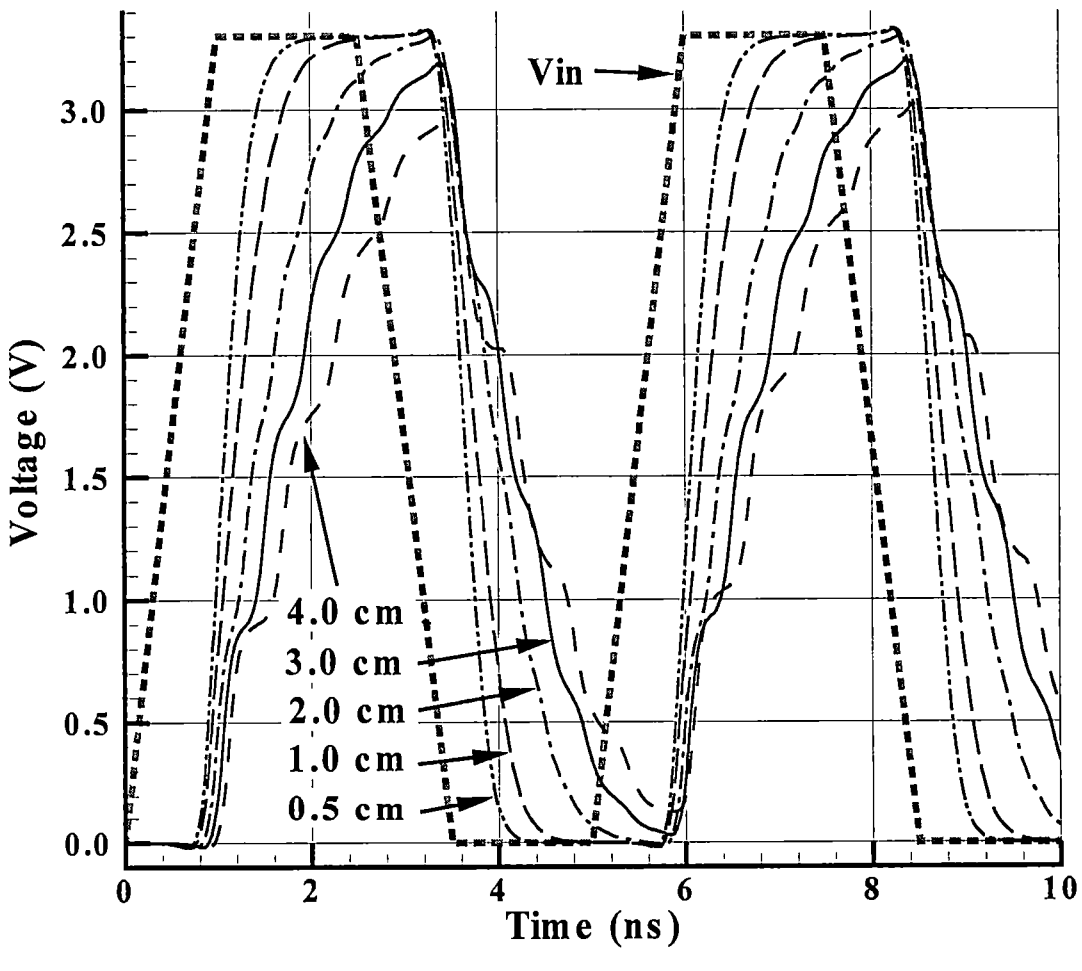


Figure 24: MCM interconnect response for a 1x driver and various trace lengths

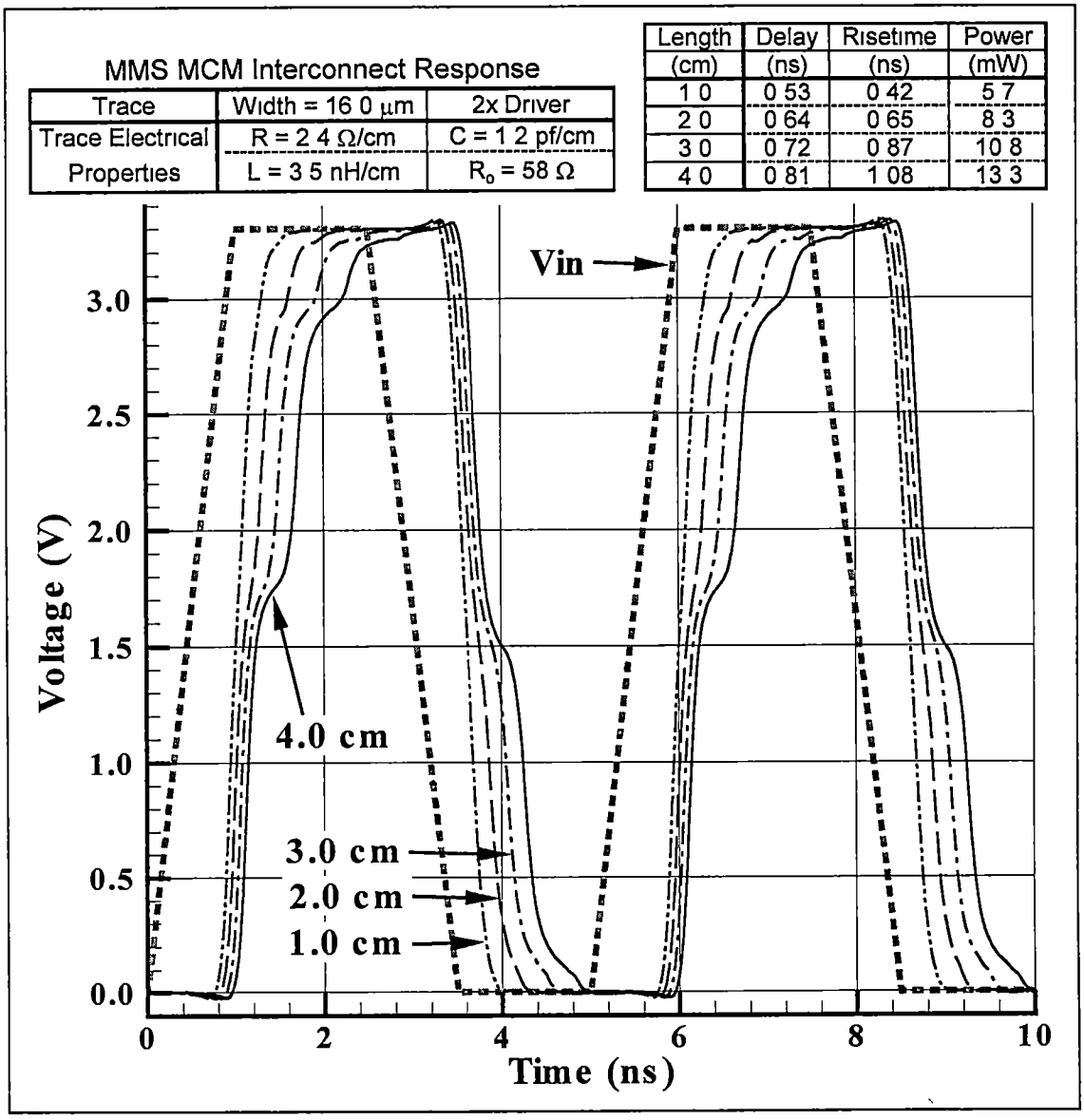


Figure 25: MCM interconnect response for a 2x driver and various trace lengths

The MCM interconnect response at the input of the receiver for a 3x driver with trace lengths from 2 0 cm to 4 0 cm is shown in Figure 26 on page 28 The 3x driver can drive an MCM trace of at least 4 0 cm in length Notice that the reflections don't occur until the signal is greater than 2 5 volts This is because the driver is strong enough to charge the trace before the reflections occur The 3x driver is 20% faster than the 2x driver for the 2 0 cm trace

Figure 27 on page 29 shows the MCM interconnect response for a 4x driver at the input of the receiver for trace lengths from 3 0 cm to 5 0 cm During the falling transition of the signal at 4 ns, the signal undershoots considerably This is caused by reflections due to mismatched termination The 4x driver's response for trace lengths from 4 0 cm to 8 0 cm is shown in Figure 28 on page 30 The 4x driver can drive an MCM trace of at least 8 0 cm in length but the undershoot that occurs for the 8 0 cm trace decreases the noise margin by approximately 0 3 volts

Figure 29 on page 31 shows the MCM interconnect response versus different driver sizes for a 4 cm trace, which is the same length as the traces used for the IC simulations The 3x and 4x driver can drive the 4 cm trace but 4x driver is exhibiting significant overshoot which is due to reflections The 1x and 2x driver are not strong enough to drive the trace The MCM interconnect response for 3x to 6x drivers for a 4 cm trace is shown in Figure 30 on page 32 Starting with the 3x and larger driver sizes, there are significant increases in undershoot and ringing due to transmission line reflections

These reflections are the result of the mismatches of impedance between the output resistance of the driver and the characteristic impedance of the trace Figure 31 on page 33 shows the output on-resistance of the two-stage tapered driver for various sizes With sizes greater than 2x, the output resistance is less than the characteristic impedance of the trace and this results in greater undershoot, see Figure 30 on page 32 The undershoot is more noticeable on the downward swing of the signal because the output resistance is greater than the characteristic impedance of the MCM trace Termination can be used to reduce transmission line reflections

The main types of termination are series and parallel termination With parallel termination, a resistor is placed from the signal node to ground at the receiving end of the transmission line, and its resistance is equal to the characteristic impedance of the transmission line If the resistance matches the characteristic

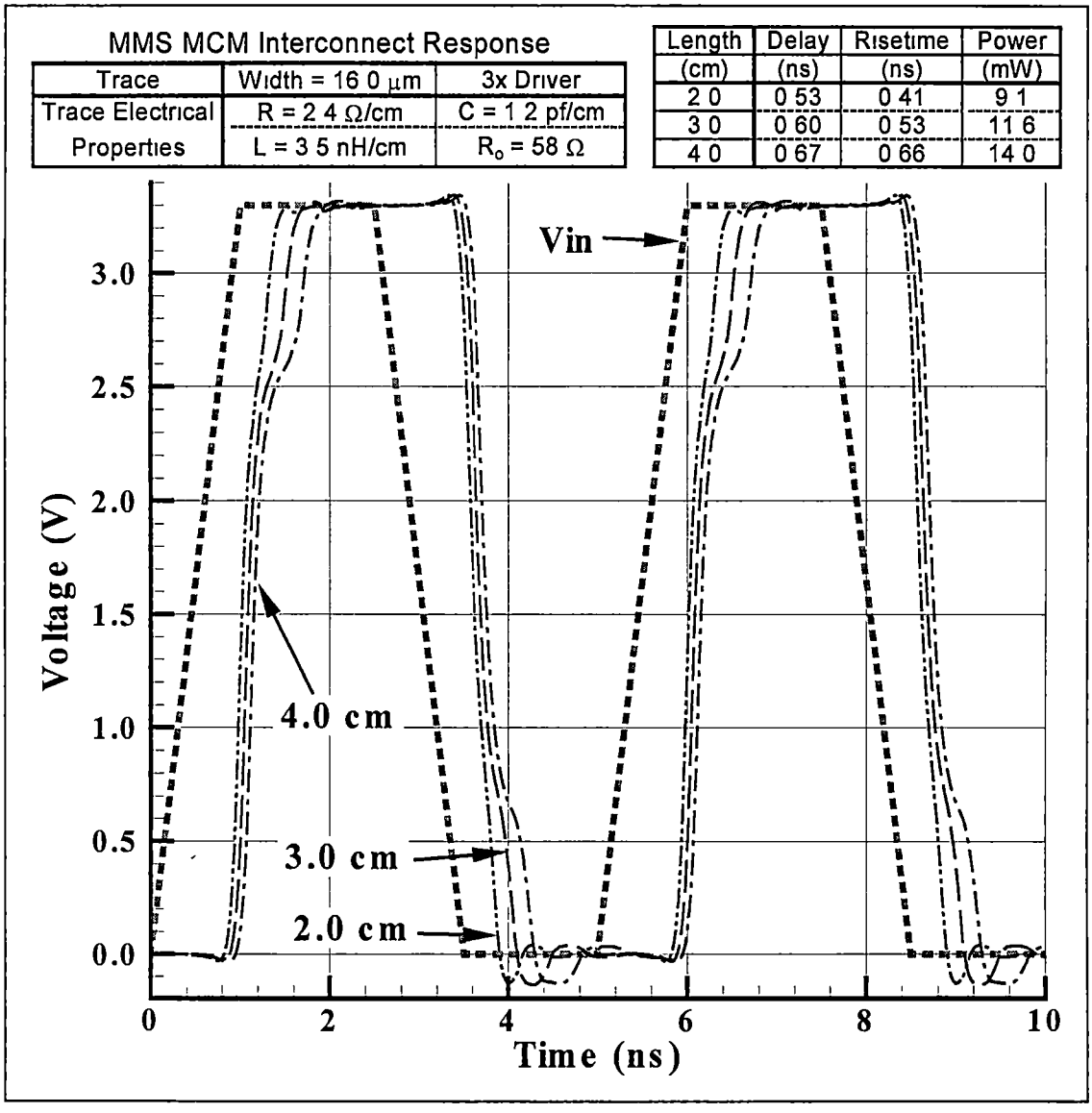


Figure 26: MCM interconnect response for a 3x driver and various trace lengths

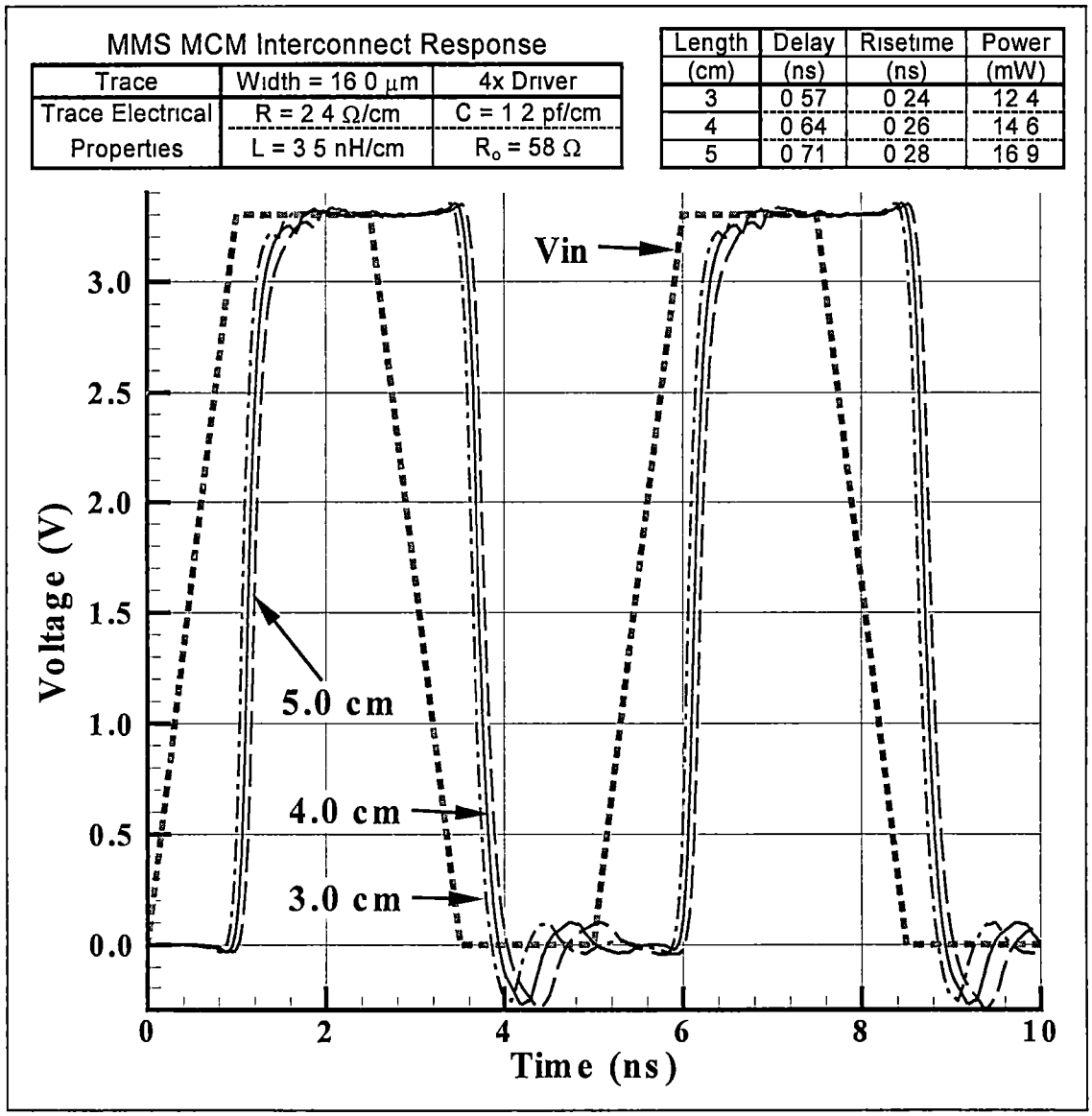


Figure 27: MCM interconnect response with a 4x driver and various trace lengths

MMS MCM Interconnect Response

Trace	Width = 16 0 μm	4x Driver
Trace Electrical Properties	R = 2 4 Ω/cm	C = 1 2 pf/cm
	L = 3 5 nH/cm	R_o = 58 Ω

Length (cm)	Delay (ns)	Risetime (ns)	Power (mW)
4	0 64	0 26	14 6
6	0 77	0 32	18 8
8	0 91	0 45	22 8

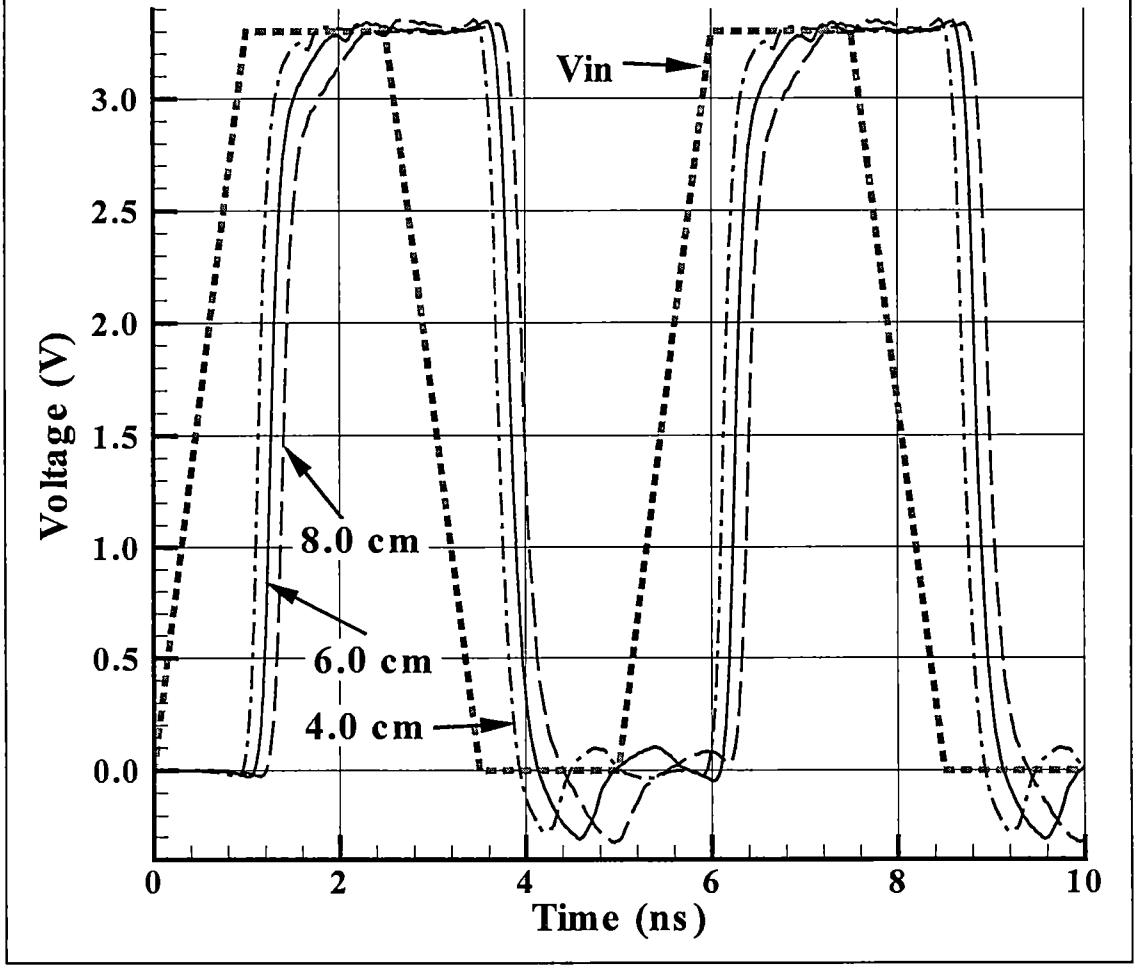


Figure 28: MCM interconnect response for a 4x driver and very long trace lengths

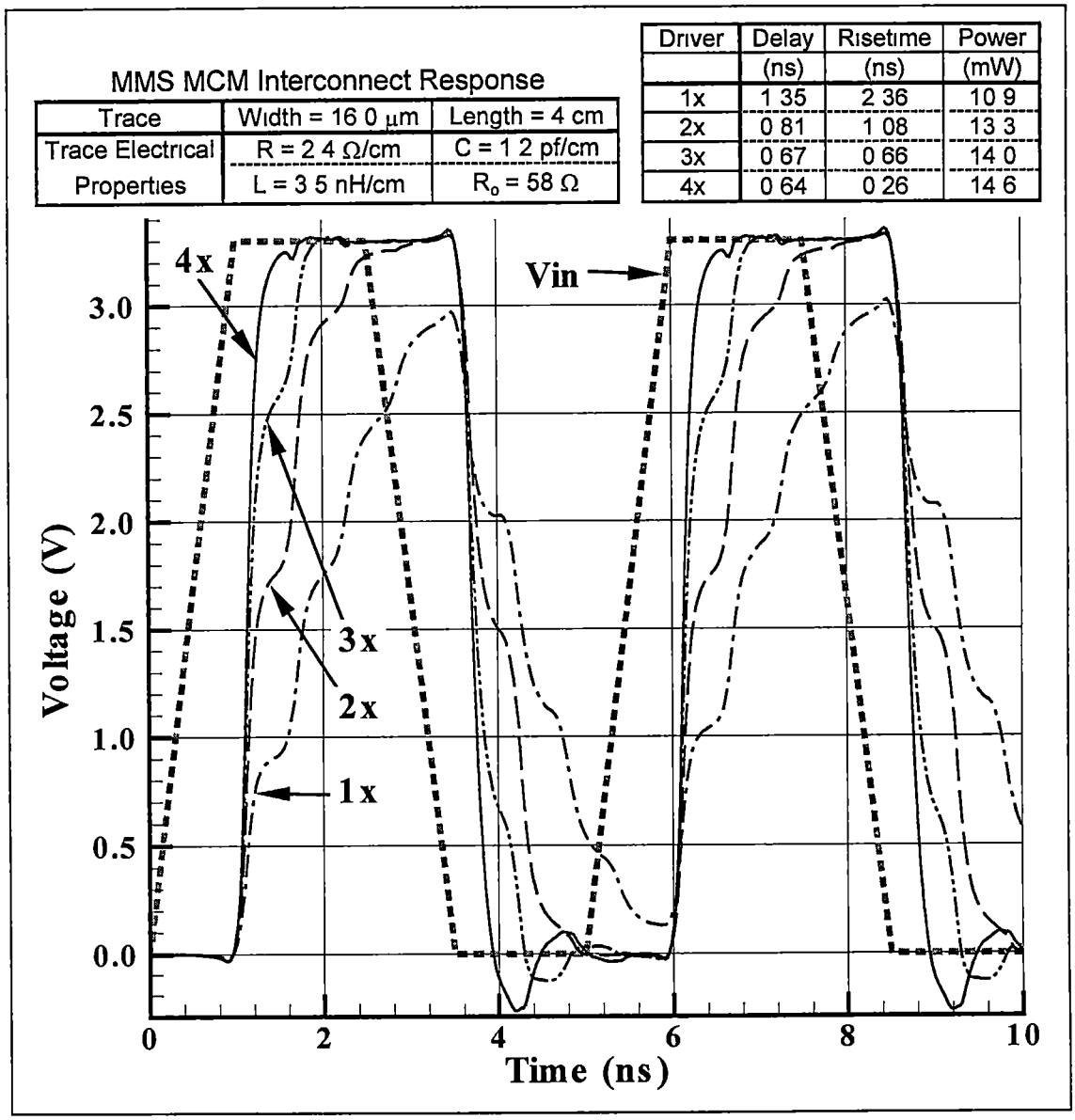


Figure 29: MCM interconnect responses for 1x, 2x, 3x, and 4x drivers of a 4 cm long trace

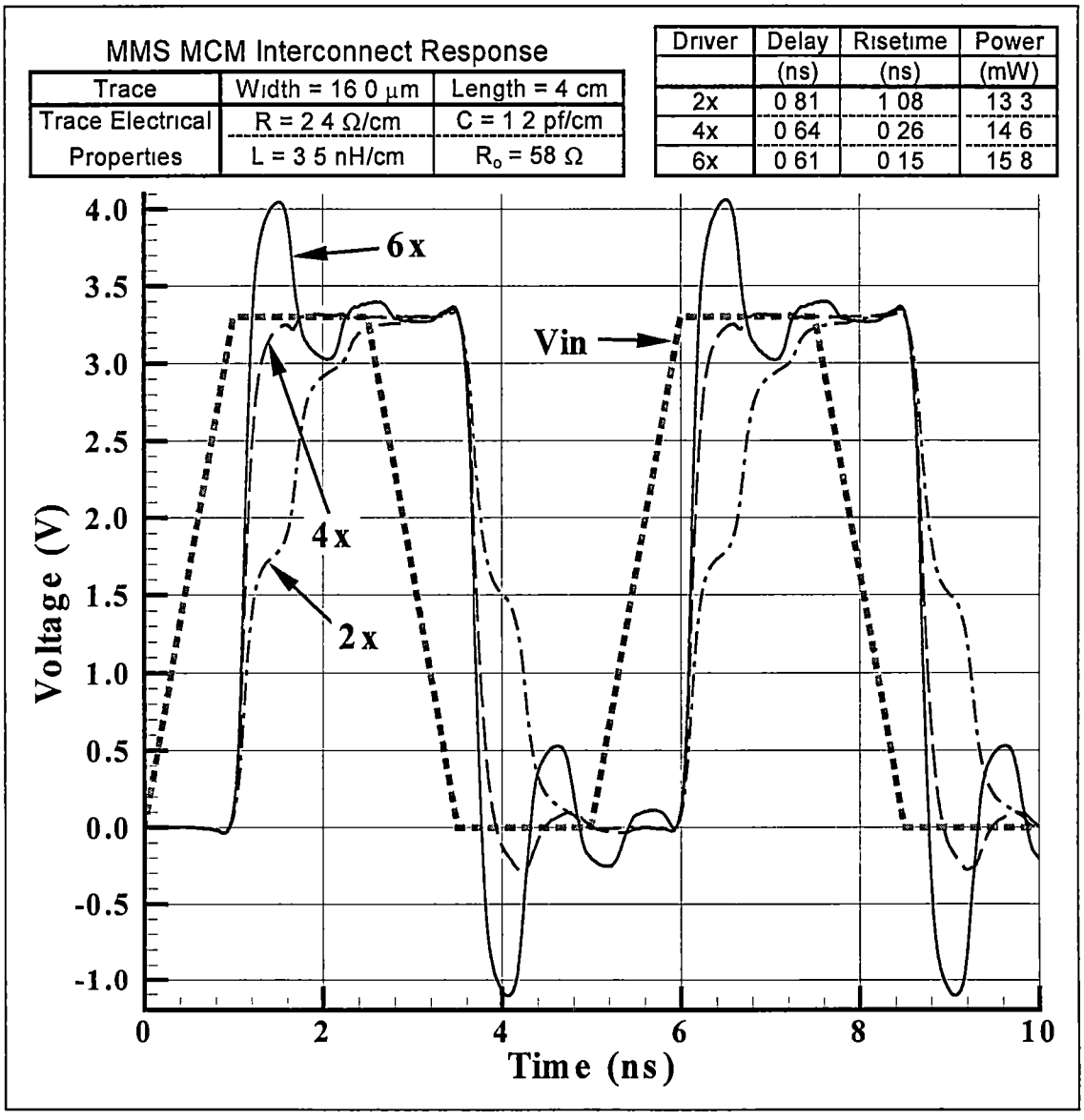


Figure 30: MCM interconnect responses for 2x, 4x, and 6x drivers of a 4 cm long trace

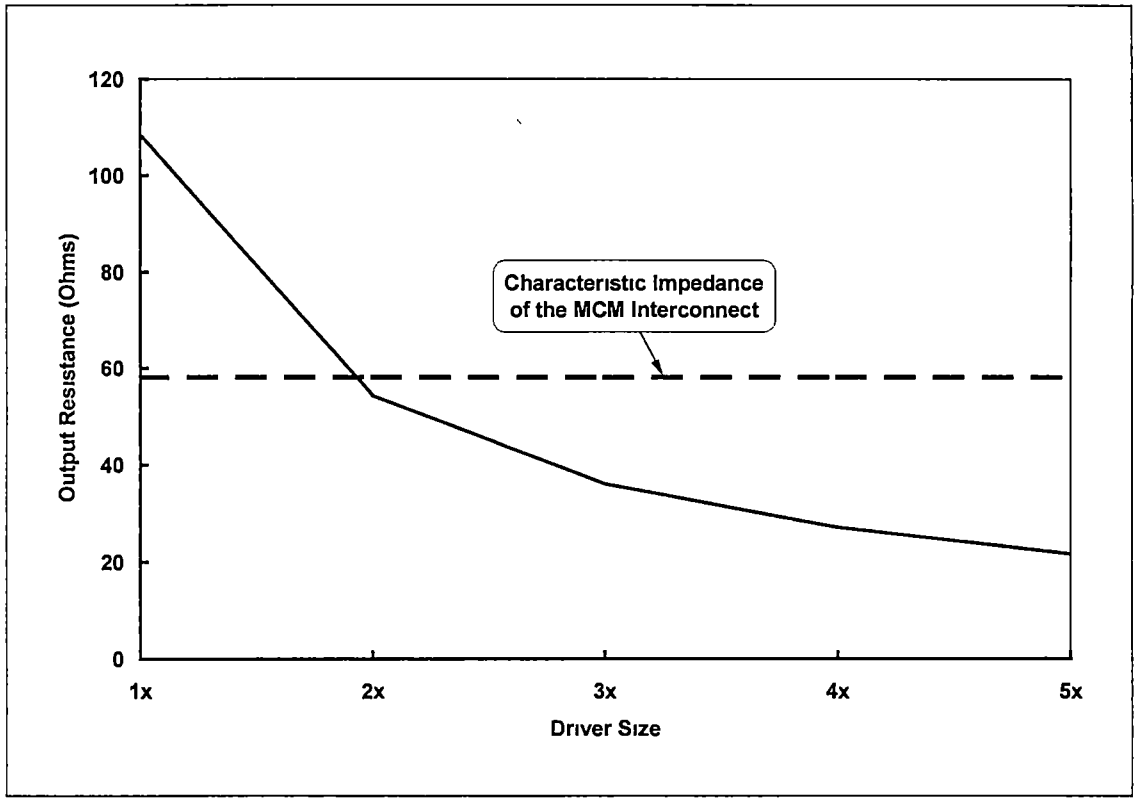


Figure 31: Output resistance of various drivers

impedance then no reflections will occur but the signal will only rise to Vdd/2 due to voltage division Since it was a requirement to have a driver that has an output range that spans from 0 to Vdd, parallel termination was not a viable solution even though it eliminates the reflections

Series termination is when a resistor is placed in series with the source end of the transmission line and its resistance is made equal to the characteristic impedance of the transmission line minus the output resistance of the driver The purpose of the series termination is to delay the reflections long enough so that they will occur after the signal has reached Vdd/2, allowing the receiver to switch without any delay The output resistance of the driver is a form of series termination and its effect can be seen in Figure 32 on page 34 The flattening of the signal near 1 65 volts at the output of the driver is an indication of series termination [3] This extra delay is the result of reflections canceling part of the signal and delaying the signal This delays the signal by a constant amount every time there is a reflection

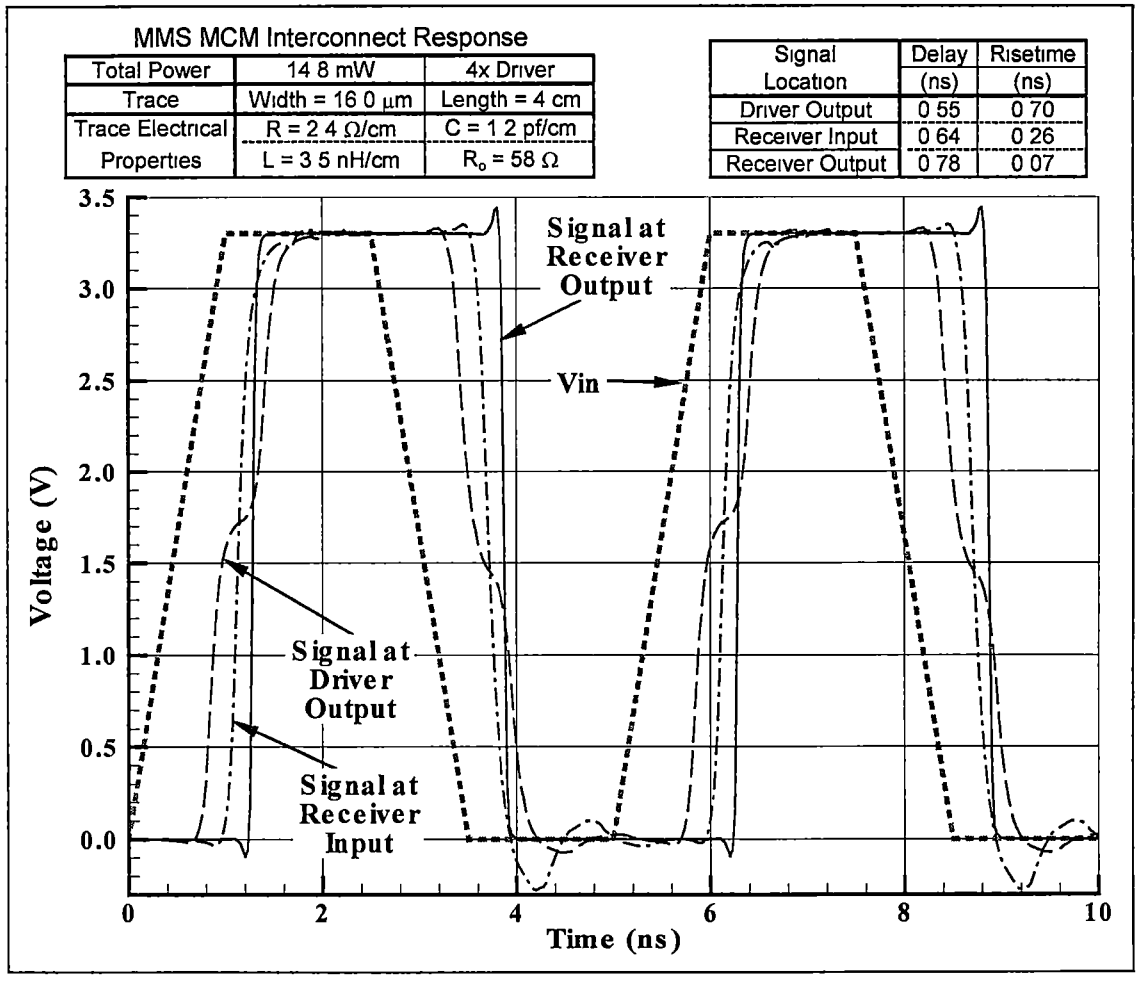


Figure 32: MCM interconnect response with a 4x driver and extra long trace lengths

Since the receiver switches very fast, the output of the receiver sharpens the signal transitions and greatly improves the signal quality, see Figure 32 on page 34 It was decided that no termination would be used and that care would be taken to limit the overshoot and undershoot with limiting diodes and let the switching speed of the receiver restore the signal quality

Table 3 on page 36 summarizes the MCM interconnect results for various drivers and interconnect length For the 2 cm to 4 cm traces, the delay is approximately equal at 0 62 ns For the 4x driver, the delay increases 60 ps for each centimeter increase in trace length while average power increases 3 3 mW for each centimeter increase in trace length The average power increases 2 0 mW for each centimeter increase in trace length for the 1 cm to 4 cm traces. The risetime decreases as the driver size increases This is due to its driving strength

Table 4 on page 36 shows the results from the comparison between the interconnect response of an IC and an MCM Although it is uncommon to have a 4 cm trace on an IC, the comparison was made with a moderate trace length for an MCM The MCM trace has at least an order of magnitude less resistance, allowing the same delay for longer MCM trace lengths compared to IC trace lengths A 4 cm length trace on an MCM has the same delay as a 2 3 cm trace on an IC for a 6x driver and equal trace widths A caveat is that the length of a trace on an IC is shorter than the trace on an MCM when a large IC is partitioned into smaller ICs and placed on an MCM The main purpose of the first case study is not to demonstrate that an MCM trace is a better than an IC trace, but to show that it is possible to create longer MCM traces and still have the same delay that the original IC trace had before partitioning This is possible because the MCM trace has lower resistance and capacitance than the IC trace Another advantage in moving a trace from an IC to an MCM is the savings in area on the IC as shown in Table 4 on page 36 Compared to an IC trace of comparable width, the MCM trace has 33% less delay, 70% faster risetime, 30 times less IC area, dissipates about the same amount of power, and requires a smaller driver

Table 3: MCM interconnect response

Interconnect Length	Driver Size	Interconnect Capacitance with IC & MCM pads	T_{rise}	T_{delay}	Average Power
(cm)		(pF)	(ns)	(ns)	(mW)
1	1x	1 7	0 70	0 79	4 8
2	2x	2 9	0 65	0 64	8 3
3	3x	4 1	0 53	0 60	11 6
4	4x	5 3	0 26	0 64	14 7
6	4x	7 7	0 32	0.77	18 8
8	4x	10 1	0 45	0 91	22 8

Conditions

200 MHz clock
100 µm x 100 µm CMOS14TB metal 3 pads
CMOS14TB driver
One CMOS14TB receiver without ESD protection
MMS Y-signal (w=16 µm) interconnect
HSPICE lossy transmission line modeling

Table 4: Interconnect case study 1 results

Interconnect Length = 4 cm, F_{clk} = 200 MHz

	CMOS14TB	CMOS14TB	MMS-MCM
	W=4 8 µm	W=14 4 µm	W=16 µm
Chip Interconnect Area (μm^2)	192,000	576,000	20,000
Total Capacitance (pF)	5 1	9 0	5 3†
Total Resistance (Ω)	304	104	9 6
Driver Size	4x	6x	4x
T_{rise} (ns)	1 6	1 0	0 3
T_{delay} (ns)	1 1	0 9	0 6
Average Power (mW)	7 5	15 0	14.7

† Includes on-chip pad capacitance

Case Study 2

Introduction

After it was established from case study 1 that a longer MCM trace can have the same delay as a shorter IC trace, the examination of how delay correlates to the length of the trace was studied Different length traces on an IC and MCM were compared using the 50%-50% delay and 10%-90% risetime Several papers [1, 2, 3] have indicated that the delay on the IC increases exponentially with length while the delay on the MCM increases linearly with length This concept is usually modeled as a lumped RC circuit for the IC trace and as a lossless transmission line for the MCM trace

Operating Parameters

In this modeling study, the IC trace and MCM trace are both modeled as lossy transmission lines Figure 9 on page 13 shows the system diagram for the IC and MCM traces As in case study 1, the top layer metal conductor parameters of the HP CMOS-14B process was used for the IC interconnect modeling, while the MMS Y-signal conductor parameters were used for the MCM interconnect modeling, see Table 2 on page 11 A 200 MHz clock with a 1 ns risetime was used as the drive signal for this case study. HSPICE was used to simulate the system with traces being modeled as lossy transmission lines and transistors being modeled with level 3 models The IC drivers and receivers were modeled without any electrostatic discharge (ESD) protection circuits. A 6x drivers was used for both IC traces and MCM traces as shown in Figure 10 on page 14

Simulation Results

Figure 33 on page 38 shows the delay and risetime versus trace length for both the IC and MCM The delay through the IC trace increases exponentially with length while the delay through the MCM trace increases linearly The delay of the MCM trace increase 68 ps for each centimeter increase, while the delay of the IC doubles every 3 cm A 10 cm MCM trace has the same delay as a 4 cm IC trace

Figure 34 on page 39 shows the IC interconnect response at the input of the receiver for a 6x driver and trace length from 0 5 cm to 10 cm The 6x driver can only drive trace length up to 2 5 cm The IC interconnect response at the output of the receiver is shown in Figure 35 on page 40

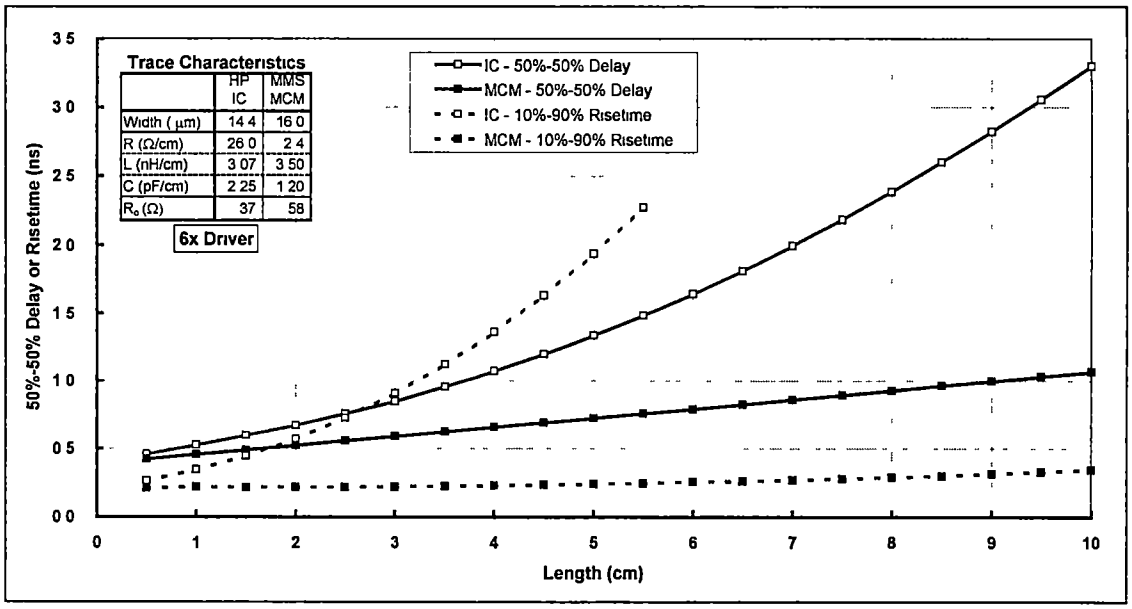


Figure 33: IC and MCM delay and risetime for trace lengths 0 5 to 10 cm

CMOS14B IC Interconnect Response

Trace	Width = 14 4 µm	6x Driver
Trace Electrical Properties	R = 26 0 Ω/cm	C = 2 25 pf/cm
	L = 3 07 nH/cm	R_o = 37 Ω

at the Input of the Receiver

Length (cm)	Delay (ns)	Risetime (ns)	Power (mW)
0 5	0 46	0 26	8 6
2 5	0 75	0 73	15 0
5 0	1 34	1 94	17 5
7 5	2 18	*Failed*	16 1
10 0	3 30	*Failed*	15 2

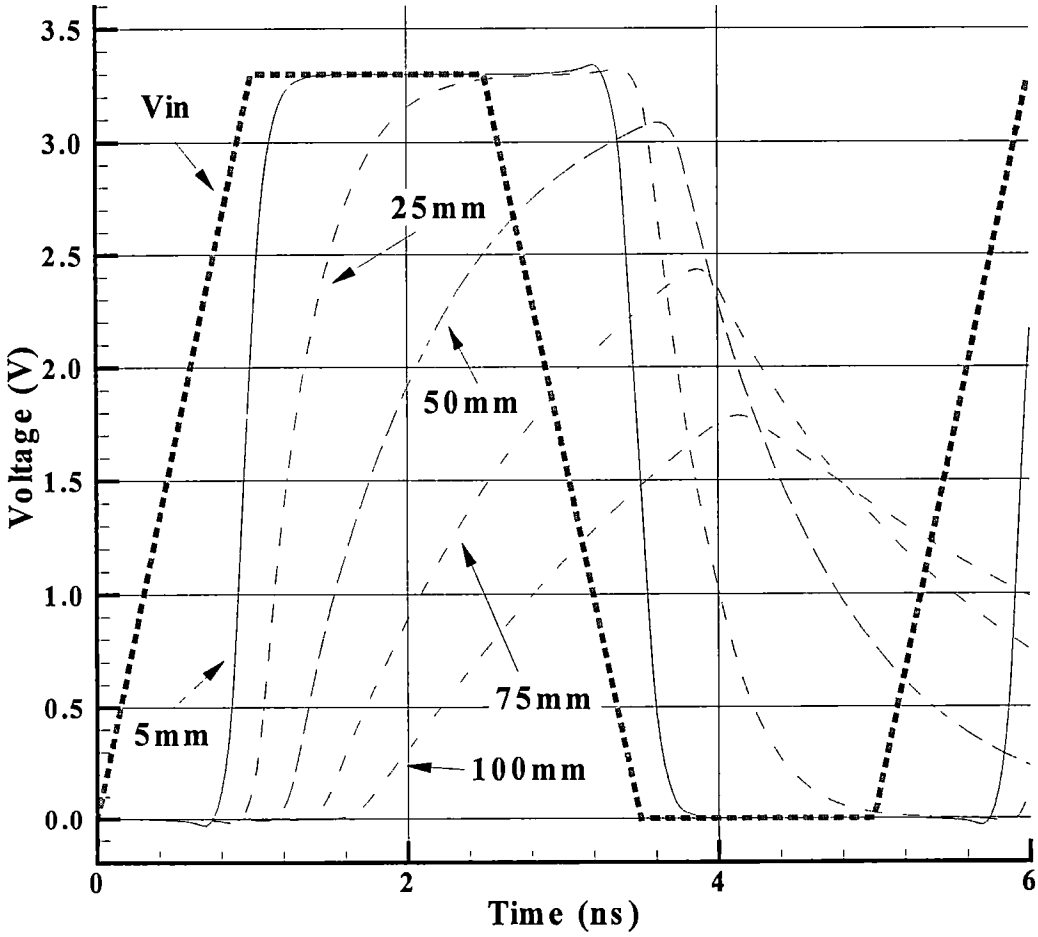


Figure 34: IC interconnect responses at the input of the receiver for a 6x driver with varying trace lengths.

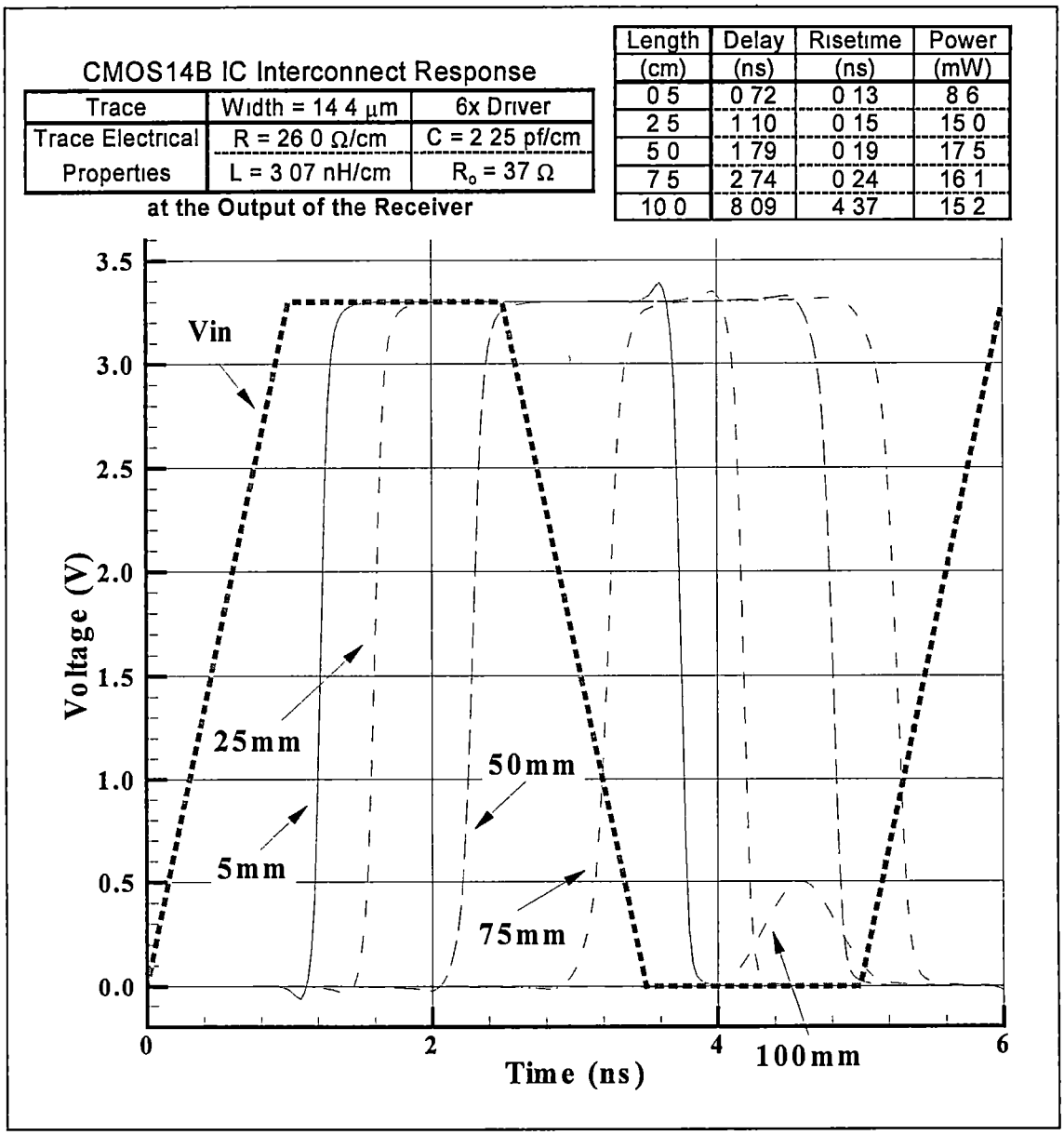


Figure 35: IC interconnect responses at the output of the receiver for a 6x driver with varying trace lengths

The MCM interconnect responses at the input of the receiver for a 6x driver and trace length from 0 5 cm to 10 cm is shown in Figure 36 on page 42. The 6x driver can drive trace lengths up to 10 cm but some overshoot occurs with trace lengths greater than 5 cm Figure 37 on page 43 shows the MCM interconnect response at the output of the receiver The overshoot of the signal at the input of the receiver does not propagate to the output of the receiver

The delay of the IC increases exponentially because the effective time constant of the trace is near the clock frequency This is due to the impedance of the IC trace Bakoglu [3] states that a transmission line behaves as a distributed RC circuit if the total resistance of the trace is greater than $5*Z_o$ where Z_o is the characteristic impedance of the trace For the 14 4 μm width IC trace, it behaves as a distributed RC circuit when it is longer than 7 1 cm The length at which the MCM trace behaves as a distributed RC circuit is 120 8 cm The frequency at which a line is driven can influence whether the trace behaves as an RC transmission line for low frequencies or as a low-loss transmission line for high frequencies [10] Equation 4 describes the characteristic impedance of a transmission line as a function of frequency, and equation 5 distinguishes the two cases described above

$$Z_o(\omega) = \sqrt{\left(\frac{R + j\omega L}{j\omega C}\right)} \tag{4}$$

$$\begin{aligned} &RC\,case: \\ &\qquad \omega << \frac{R}{L}\ (also\ R >> \omega L) \\ &Low-loss\,case: \\ &\qquad \omega >> \frac{R}{L}\ (also\ R << \omega L) \end{aligned} \tag{5}$$

The R/L frequency for the 14 4 μm width IC trace is 1.3 GHz, which according to equation 5 indicates that it behaves as an RC transmission line at 200 MHz The R/L frequency for the 16 0 μm width MCM trace is 109 MHz, which indicates that it behaves more as a low-loss transmission line or just a simple time-delay element Using simple distributed RC analysis, the effective time constant for 14 4 μm width

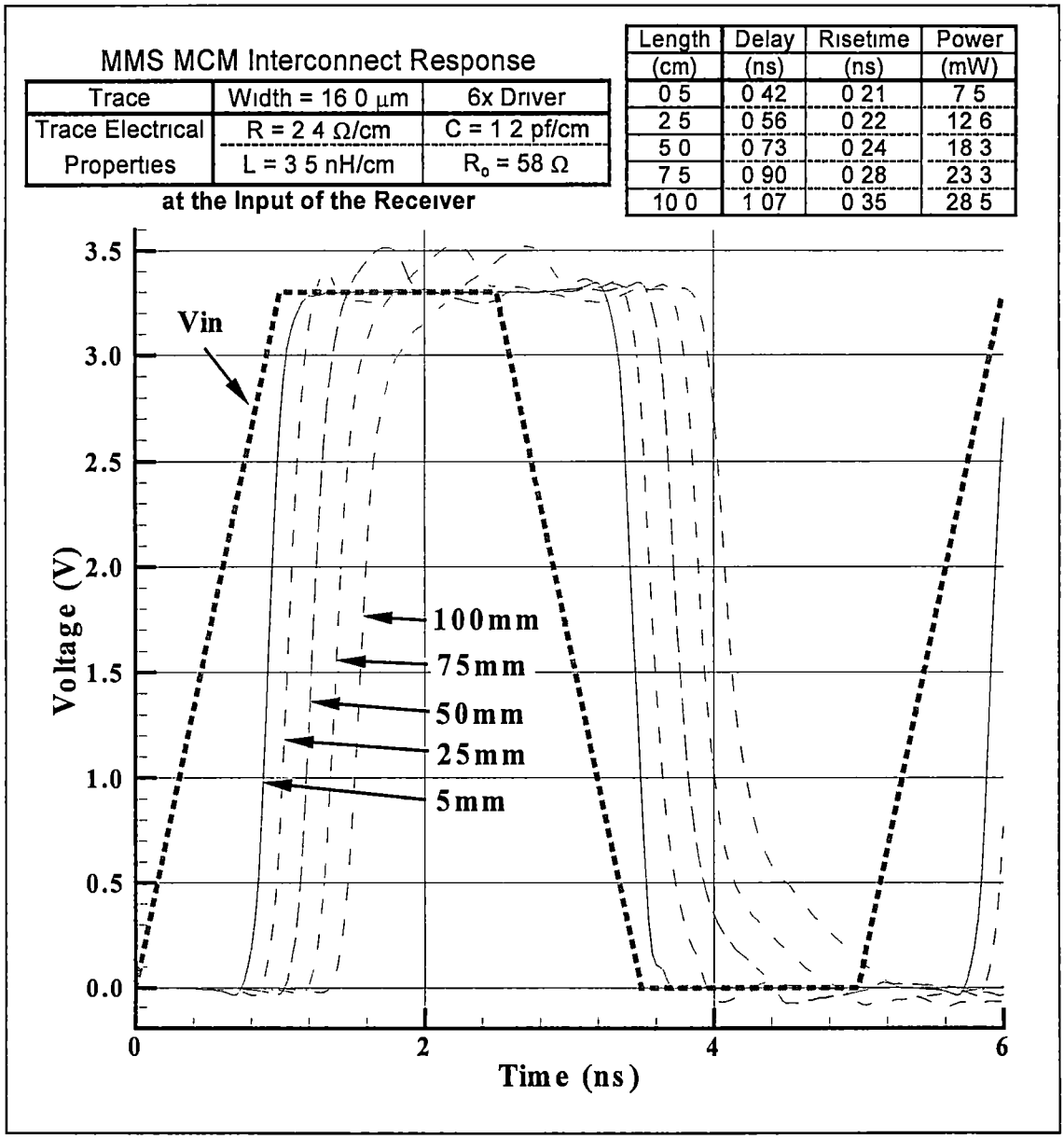


Figure 36: MCM interconnect response for a 6x driver at the input of the receiver with varying trace lengths

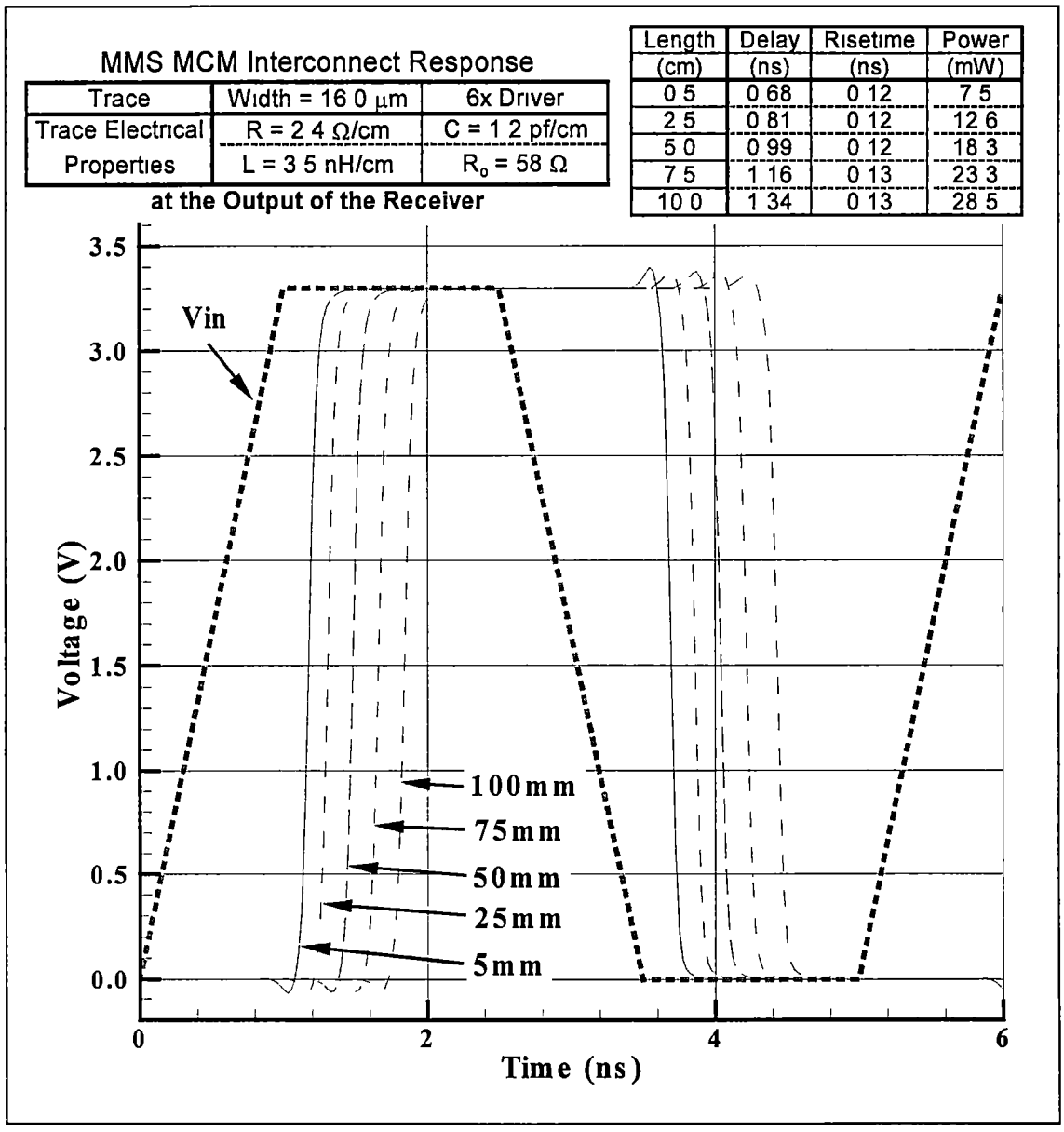


Figure 37: MCM interconnect response for a 6x driver at the output of the receiver with varying trace lengths

IC trace is 1.4 ns for a 3 cm trace and 2 4 ns for a 4 cm trace This demonstrates that the trace impedance becomes the dominant limitation to the delay and that the trace cannot be fully charged up during the 2 5 ns pulse of the 200 MHz clock Table 5 on page 45 shows the 3 dB frequency of a distributed RC trace having the impedance parameters listed in Table 2 on page 11 The details of the 3 dB frequency calculation can be found in Appendix C on page 74

The MCM interconnect responses at the input of the receiver for a 6x driver and trace length from 15 cm to 55 cm is shown in Figure 38 on page 46 The 6x driver can drive trace lengths up to 25 cm but the signal quality degrades sharply for lengths over 15 cm The poor signal quality degrades the noise margin and introduces the possibility of multiple switching during its transition Figure 39 on page 47 shows the MCM interconnect response at the output of the receiver The 550 mm trace response does not even charge the line to a high enough voltage to switch the receiver

Figure 40 on page 48 shows the delay and risetime for very long MCM trace lengths. From the risetime and the delay at the receiver output, the relationship between trace length and risetime approaches exponential behavior at about 18 3 cm, the same trace length at which the effective time constant of the MCM trace becomes greater than 2 5 ns For trace lengths longer than 15 cm, the trace cannot be charged up completely because of the impedance of the trace

The peculiar bend in the delay curve at the receiver input in Figure 40 on page 48 is because the signal requires one clock cycle to charge the trace up to an average voltage large enough to switch the receiver. If the driver cannot fully charge the trace, the trace voltage swings symmetrically around the average voltage of the signal (Vdd/2) after several clock periods It can be seen in Figure 38 on page 46 for a 550 mm trace that the signal is climbing to an average voltage of 1 65 volts allowing the trace voltage to switch the receiver

Table 5: 3 dB frequency and effective time constants of distributed RC circuits

Trace Length (cm)	IC 1.8 μm 3 dB Freq MHz	IC 4.8 μm 3 dB Freq MHz	IC 14.4 μm 3 dB Freq. MHz	MCM 16 μm 3 dB Freq MHz	IC 1.8 μm Effective τ ns	IC 4.8 μm Effective τ ns	IC 14.4 μm Effective τ ns	MCM 16 μm Effective τ ns
1	2,045.4	4,001.1	6,602.0	136,871.4	0.5	0.2	0.2	0.0
2	511.5	1,000.5	1,650.4	33,522.3	2.0	1.0	0.6	0.0
3	227.2	444.5	733.3	14,895.2	4.4	2.2	1.4	0.1
4	127.9	250.1	412.6	8,380.8	7.8	4.0	2.4	0.1
5	81.8	160.1	264.1	5,364.0	12.2	6.2	3.8	0.2
6	56.8	111.1	183.3	3,723.6	17.6	9.0	5.5	0.3
7	41.8	81.7	134.7	2,736.4	24.0	12.2	7.4	0.4
8	32.0	62.5	103.2	2,095.3	31.3	16.0	9.7	0.5
9	25.3	49.4	81.5	1,655.5	39.6	20.2	12.3	0.6
10	20.5	40.0	66.0	1,341.0	48.9	25.0	15.1	0.7
14				684.1				1.5
18				413.9				2.4
22				277.0				3.6
26				198.4				5.0
30				148.9				6.7
34				116.0				8.6
38				92.8				10.8
42				76.0				13.2
46				63.4				15.8
50				53.6				18.6

MMS MCM Interconnect Response

Trace	Width = 16 0 µm	6x Driver
Trace Electrical Properties	R = 2 4 Ω/cm	C = 1 2 pf/cm
	L = 3 5 nH/cm	R_o = 58 Ω

at the Input of the Receiver

Length (cm)	Delay (ns)	Risetime (ns)	Power (mW)
15 0	1 42	0 75	32 9
25 0	2 14	2 00	21 4
35 0	2 89	*Failed*	17 1
45 0	3 73	*Failed*	20 4
55 0	5 41	*Failed*	21 1

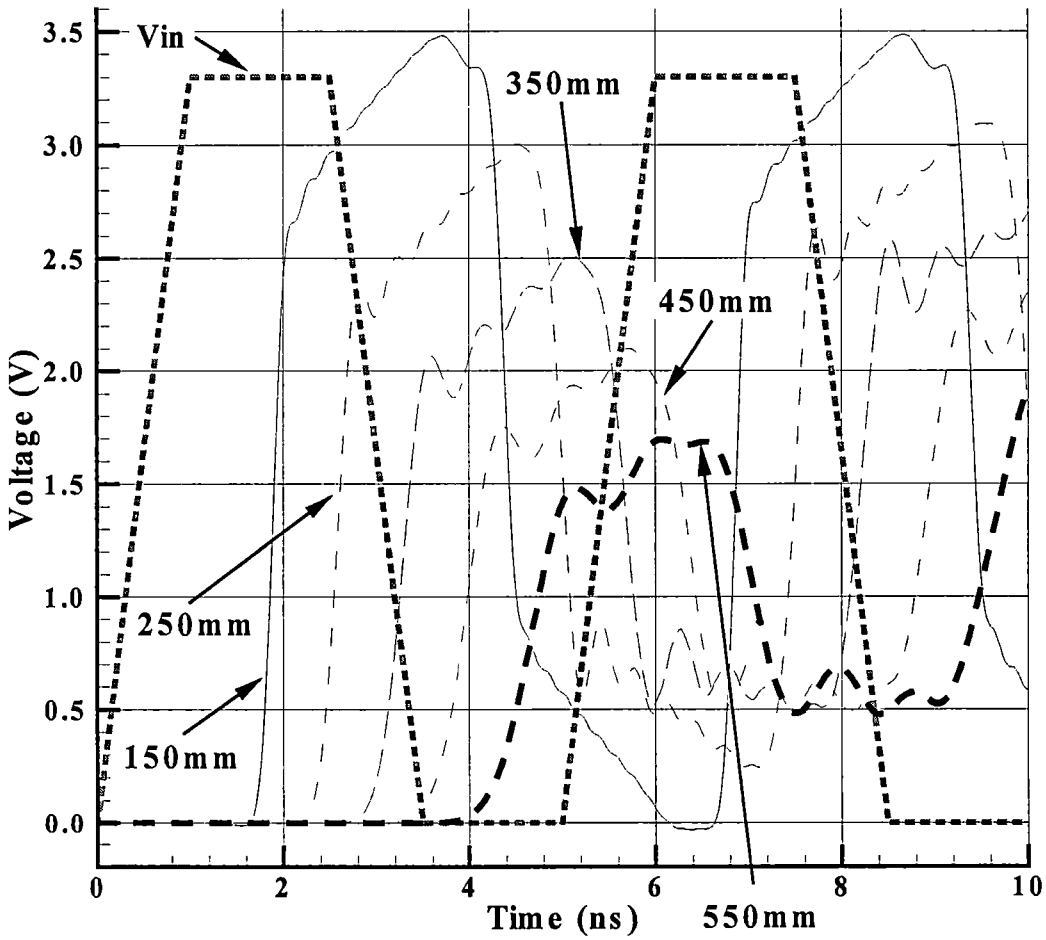


Figure 38: MCM interconnect response for a 6x driver at the input of the receiver and driving very long trace lengths

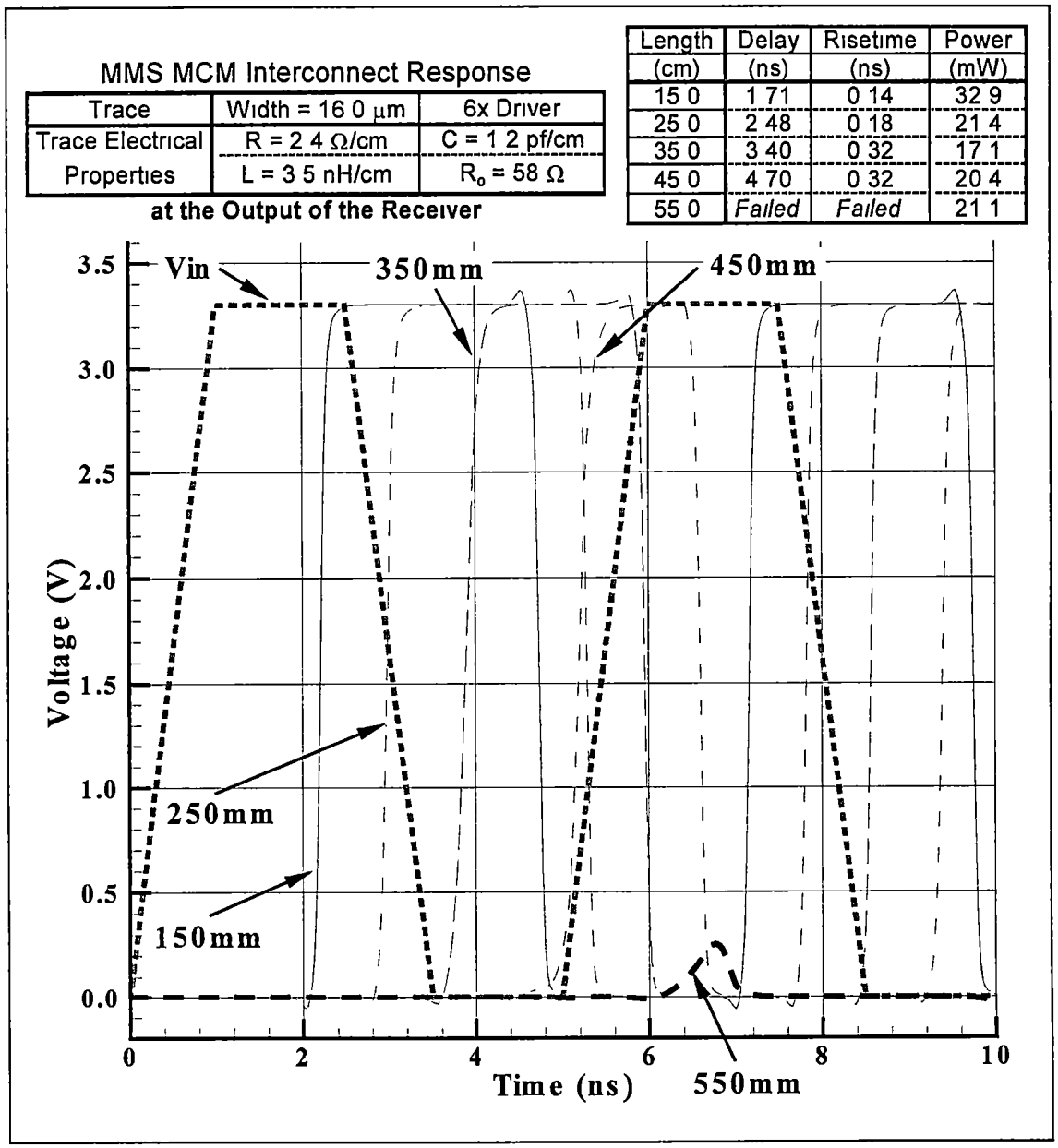


Figure 39: MCM interconnect response for a 6x driver at the output of the receiver and driving very long trace lengths

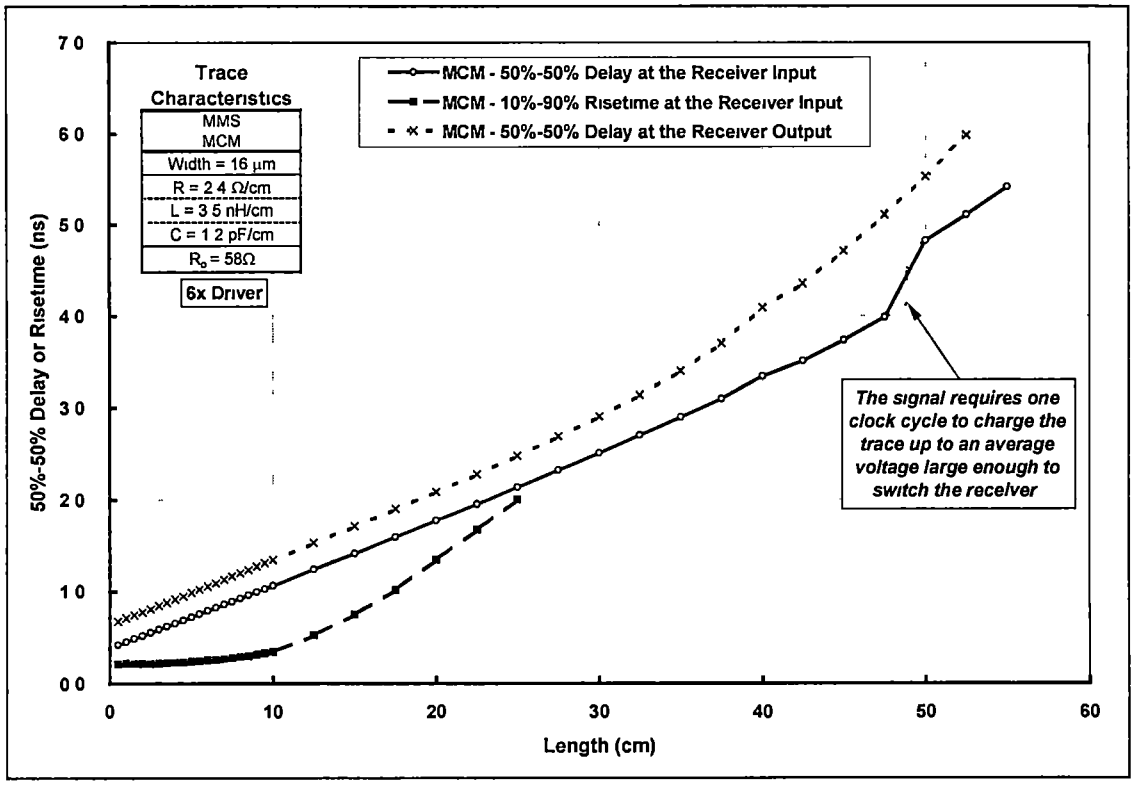


Figure 40: Delay and risetime for very long MCM trace lengths,

3. Test Chip and MCM Design

Introduction

Electronic simulations are only as accurate as the parameters used in the modeling To verify the modeling parameters and simulation results, a test chip and MCM were designed and fabricated The main objective of the project was to optimize the inter-die drivers for an MCM-D environment utilizing flip chip array I/O Some of the issues that were examined were the signal quality of a signal through an MCM trace, maximum reliable clock frequency for a trace of a certain length, and the accuracy of the modeling parameters used to model the MCM trace and IC driver The IC was manufactured in March of 1997 while the MCM was manufactured in June 1998 The packaged system was to be finished and ready for testing by October 1998, but due to problems with the fabricated IC, it was decided not to package the system

Test Strategies

The trace delays of short to moderate length MCM traces were less than 2 ns, so on-chip test circuits were needed to measure the delays without expensive high speed equipment Four test strategies were formulated to measure the trace delay. With four different measurements, results that are more reliable could be obtained In addition to the delay measurements, a test was designed to determine whether input ESD protection is needed on the receivers of inter-die traces A delay baseline measurement was also included to measure the delay of the driver and its corresponding circuitry.

The test system consisted of an MCM with four ICs connected with varying lengths of MCM traces. Due to manufacturing costs, each IC had to be identical and needed measurement circuits that were independent of trace length The measurement circuits had to work with direct feedback through the MCM trace and from a signal from a different IC The available signal I/O was limited to 144 signal pads on the MCM This required that most of the output signals needed to be multiplexed To reduce the required I/O, output from each counter was limited to the most significant bit To increase the number of different drivers available for testing, tri-state drivers where designed so that multiple drivers could be connected together and then selected to test different driver sizes

Figure 41 shows the circuit used for the trace delay measurement To measure the delay corresponding to the trace on the MCM, two types of circuits were used *around-the-IC* measurement circuit and *IC-to-IC* measurement circuit The *around-the-IC* measurement circuit included four different test strategies for measuring delay while the *IC-to-IC* measurement circuit included only two test strategies The *around-the-IC* measurement circuit required direct feedback through an MCM trace The signal path involves the signal going through the driver, onto the MCM for a specific distance, and then back onto the same IC, making a feedback loop The *IC-to-IC* measurement circuit does not have a direct feedback path Its signal path involves the signal going through the driver, onto the MCM for a specific distance, and then onto a different IC Two different test circuits were used to verify whether feedback affected the delay through the MCM trace

The delay that is measured includes the delay of the MCM trace, the driver and the measurement circuit. A base delay circuit was included that consisted of the *around-the-IC* measurement circuit but its feedback path did not include an MCM trace but an internal IC trace This allowed the delay of the driver and the measurement circuitry to be measured and removed from the trace delays.

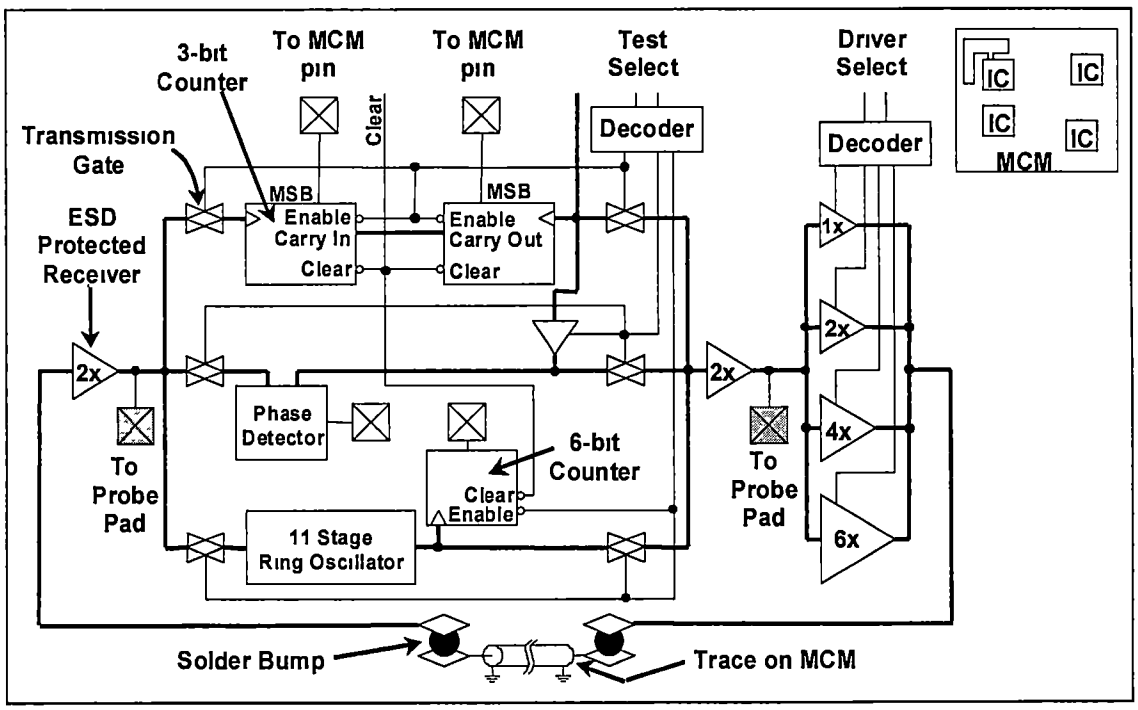


Figure 41: *Around-the-IC* measurement circuit

A decoder was used in conjunction with transmission gates to select the different test strategies This allowed the maximum flexibility in different test strategies while minimizing the number of I/O required Four tri-state driver sizes were used (1x, 2x, 4x, 6x) to allow multiple delay measurements for different driver sizes The tri-state drivers allowed four times more measurements without the cost of the extra I/O. The load of the four drivers was substantial enough that a 2x driver was needed to drive the signal from the different tests to the tri-state drivers A 2x receiver was used to provide ESD protection at the point at which the signal enters the IC again, after traversing the MCM substrate.

Split Clock Test

The first test strategy included two 3-bit counters with the clock being split between them The system clock went to the first counter immediately on the IC but also traveled off the IC, onto the MCM, and then back on to the IC to the other 3-bit counter This introduced an effective delay between the clock of the first counter and the clock of the second counter The second counter was incremented from the carry-out signal of the first counter This simulated the effect of partitioning a digital circuit and having the system clock split among different ICs The test procedure consisted of increasing the system clock until the second 3-bit counter stops counting This measures the upper limit of the clock frequency

Probe Test

The Split Clock Test strategy does not measure delay, rise time, or signal quality directly The upper operating frequency is the only result that is gained Therefore, a second test strategy was used to measure the signal quality Probe pads are connected to the trace at the point at which the signal enters the drivers and at the point at which the signal enters the IC again, after traversing the MCM substrate The probe design is shown in Figure 42 on page 52 Since the probe that used for the testing had not yet been purchased, we wanted to allow for the maximum amount of flexibility during testing The probe pad was designed to handle dual wire probes that ranged from 250 μm to 500 μm spacing In addition, the signal pad was repeated on the other side of the ground pad so that the probe could be positioned from either side of the MCM without rotating the MCM The probe pads sit on the top-most layer of the MCM to allow probing with a high-speed probe and a microprobe station

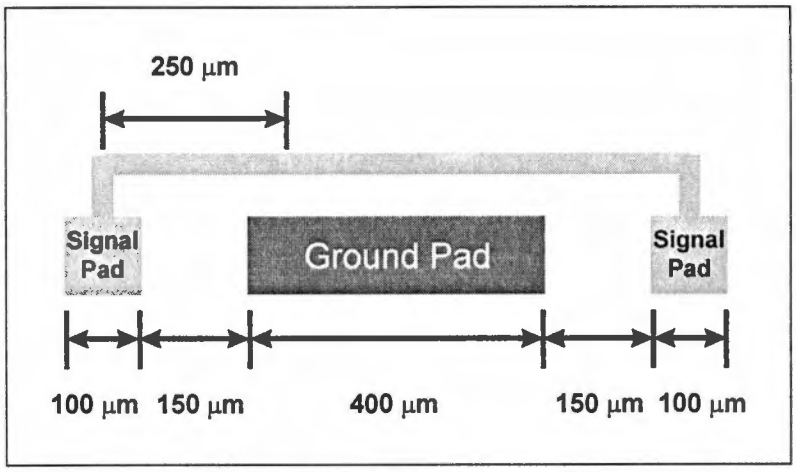


Figure 42: Probe pad layout.

Phase Detector Test

The third test strategy was to use a phase detector to measure the delay between the clock and the clock after it has traveled a specific distance on the MCM. The phase detector consists of a simple Exclusive-OR (XOR) circuit. The XOR of the two signals produces a signal that has a duty cycle proportional to the delay as long as the delay is less than half the period. Figure 43 on page 53 shows the resultant signal for two signals that are delayed. The output of the XOR was sent through a low pass filter and an average voltage could be measured that is proportional to the delay between the signals. This is a very simple way to measure the delay of the MCM trace. Figure 44 on page 53 shows the simulated delay and the resultant output voltage of the phase detector and the low-pass filter. The *around-the-IC* measurement circuit shown in Figure 41 on page 50 was used for the modeling with a clock frequency of 100 MHz. For the 1x driver, the phase detector saturates when the delay approaches 3.0 ns. For the 1x driver, a delay can be measured up to 3 cm because the 1x driver does not have the strength to drive more than a 3 cm trace. The different slope of the delay for traces less than 3 cm is because the trace delay is less than the rise time. Since the risetime is greater than zero, the pulse difference between the two signals do not extend from 0 to Vdd, and therefore its average value is less than expected than if the risetime was zero. The differences in rise and fall times cause the pulse widths resulting from the rising edges to be different from the pulse widths resulting from the falling edges. This accounts for some of the non-linearity in the simulated results.

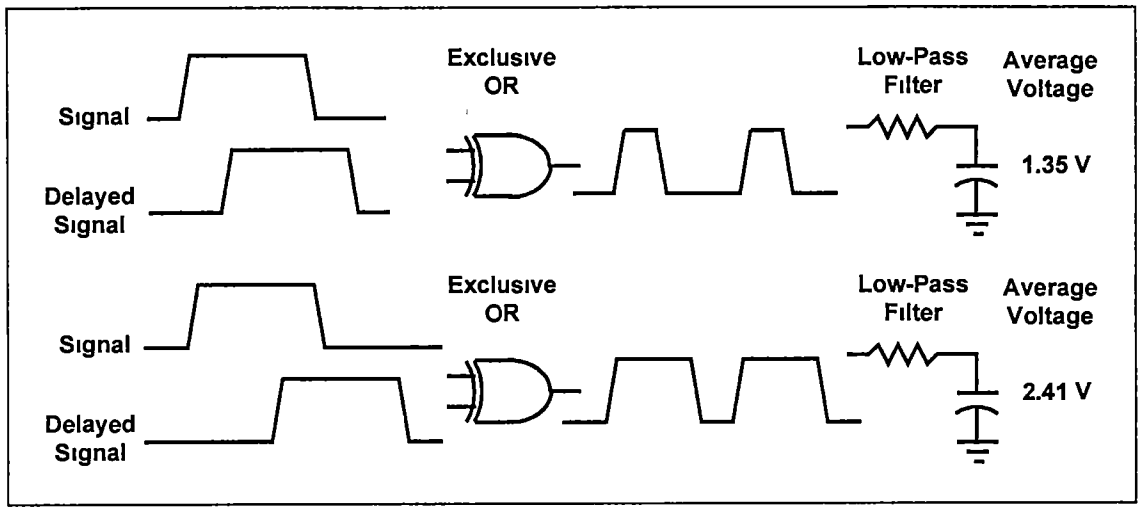


Figure 43: Exclusive-OR phase detector

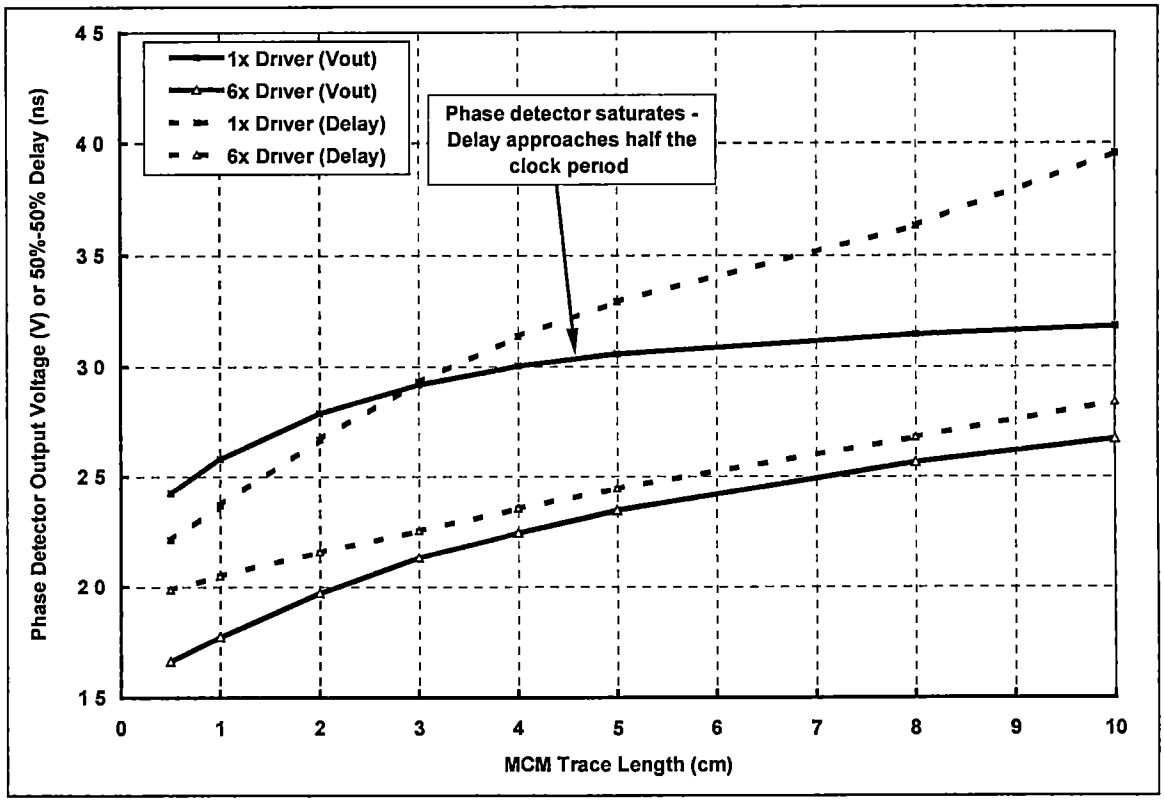


Figure 44: Phase detector modeling results

Ring Oscillator Test

The fourth delay test strategy consisted of an 11-stage ring oscillator with a delay introduced in the oscillator by a trace on the MCM The longer the MCM trace, the longer the delay, and therefore the lower the oscillating frequency of the ring oscillator The circuit for the ring oscillator test is shown in Figure 45. The oscillating frequency is measured by the most significant bit of a 6-bit counter, which runs at 1/64th the frequency Figure 46 on page 55 shows simulated results for the ring oscillator versus varying MCM trace lengths The 1x driver result is non-linear because it can only drive traces of length less than 2 cm The oscillating frequency for small traces for the 4x and 6x drivers is non-linear because the delay of the trace is non-linear because it is less than the risetime of its signal

Input ESD Protection Test

The input ESD protection test circuit is shown in Figure 47 on page 55 This test is to determine whether ESD protection is needed for receivers that are connected only to ICs on the MCM The Vdd of the unprotected receivers were connected to a separate power pin If the transistors were damaged due to ESD and caused a short from power to ground, then the whole IC would not power up In addition, all external signals coming from or going to MCM pins have ESD protection

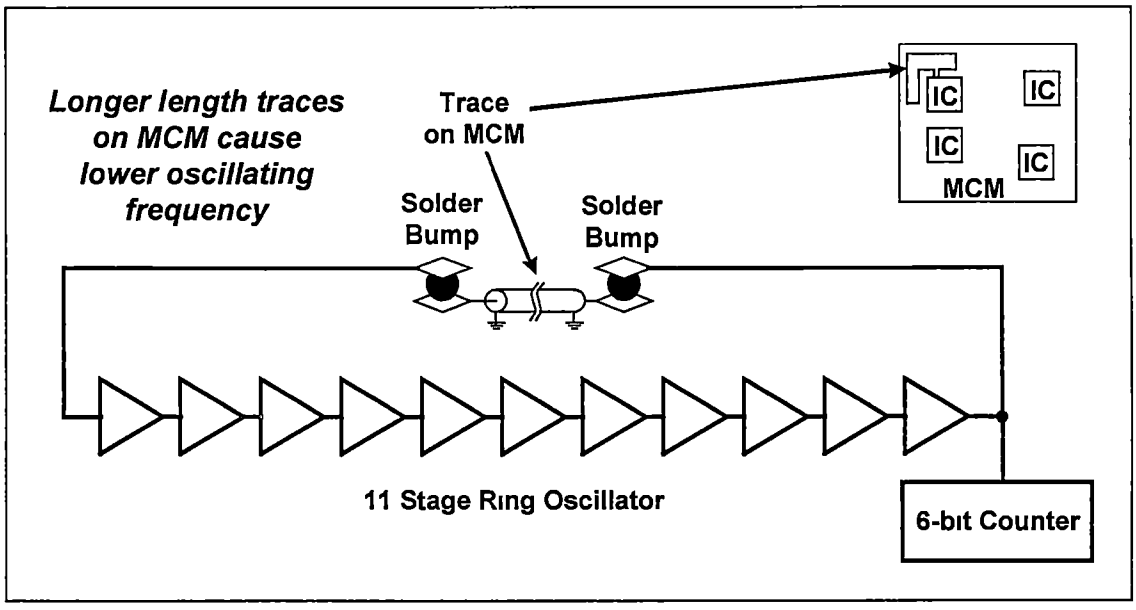


Figure 45: Ring oscillator test circuit

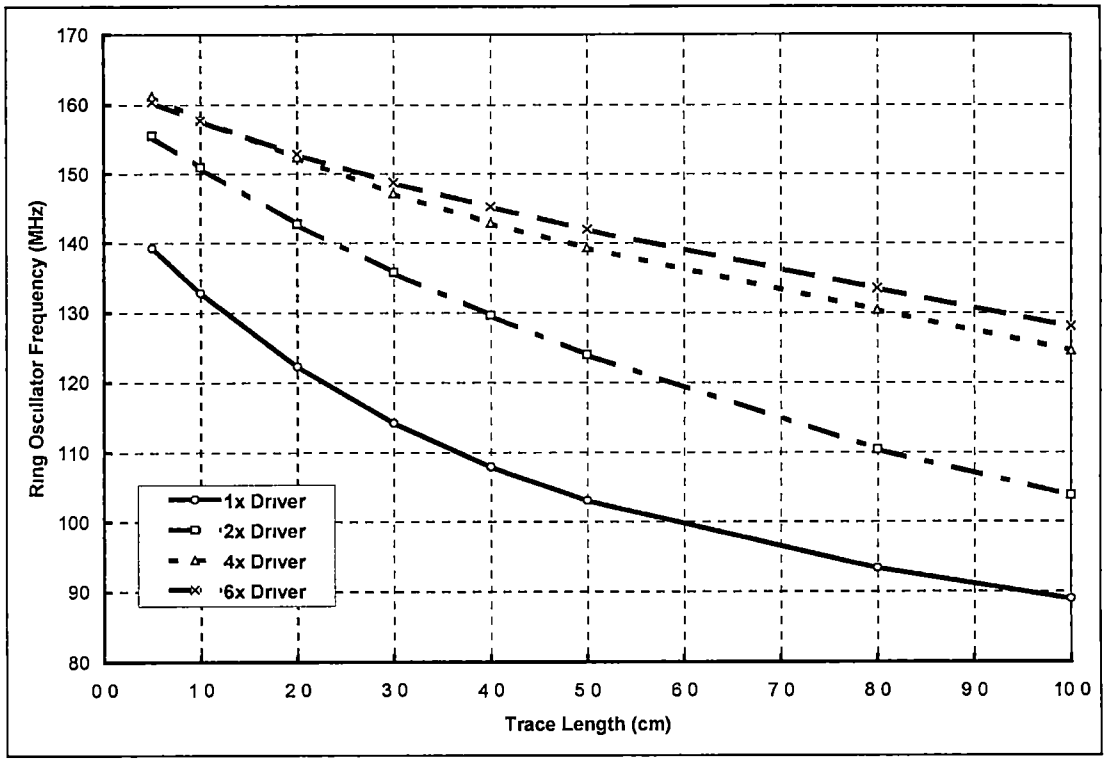


Figure 46: Ring oscillator modeling results

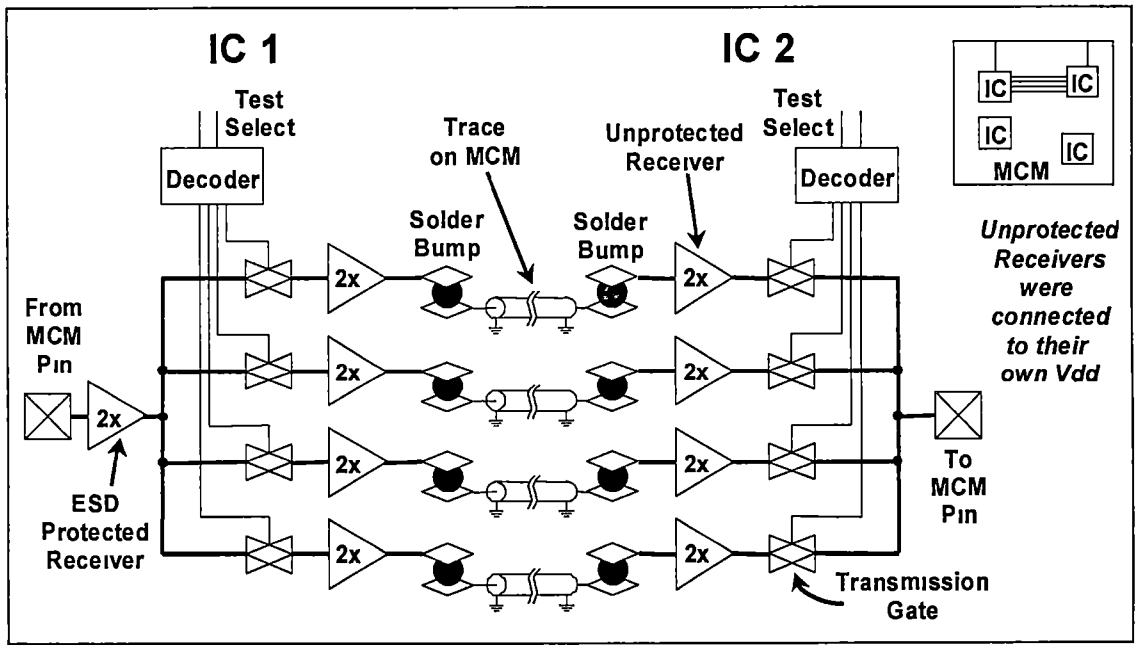


Figure 47: Input ESD protection test circuit

MCM Layout

Figure 48 on page 57 shows the layout of the MCM with the four ICs and the MCM traces Included on the MCM are decoupling capacitors to reduce the power and ground transients incurred during switching One major obstacle was to realize specific length traces on the MCM from IC to IC All automatic routers are designed to give the shortest route or the route with the smallest delay and none of them handle the situation of a specific length route Mentor Graphics® was used for the MCM layout and routing Inexperience with the Mentor system and short deadlines led to a solution involving drawing the trace paths in a general CAD package called AutoCAD® The trace paths were then translated to Mentor Graphics file formats via software developed personally The majority of the time required for the layout of the MCM was in the definition of the IC, the signals, and the design of the probe pads. After the 16 specific length MCM traces were routed manually, the remaining 84 signals were routed automatically by Mentor Graphics Mentor Graphics uses a maze router for its automatic routing

IC Partition and Layout

The IC was partitioned into eight modules, see Figure 49 on page 57 The IC had two *around-the-IC* measurement modules each containing the *around-the-IC* measurement circuit shown in Figure 41 on page 50, and two *IC-to-IC* measurement modules each containing just the probe pad connections and the split counter test from the *around-the-IC* measurement circuit A phase detector calibration section was included to allow a known delay to be connected and its resulting voltage to be measured The base delay measurement module contains the *around-the-IC* measurement circuit but without the MCM trace Its feedback was connected internally inside the IC and it allowed measuring the delay of all of the transmission gates, drivers, buffers, and receivers The control signals module contained the driver and test select lines, and the input ESD protection test module contained the input ESD test circuit

The IC layout shown in Figure 50 on page 58 was done using MAGIC, an IC layout editor by the University of California at Berkley The size of the active circuit is only a small part of the IC, and none of the active circuitry was placed under a pad Future studies might examine the effects of placing active circuitry under a pad, which is possible with solder bump connections.

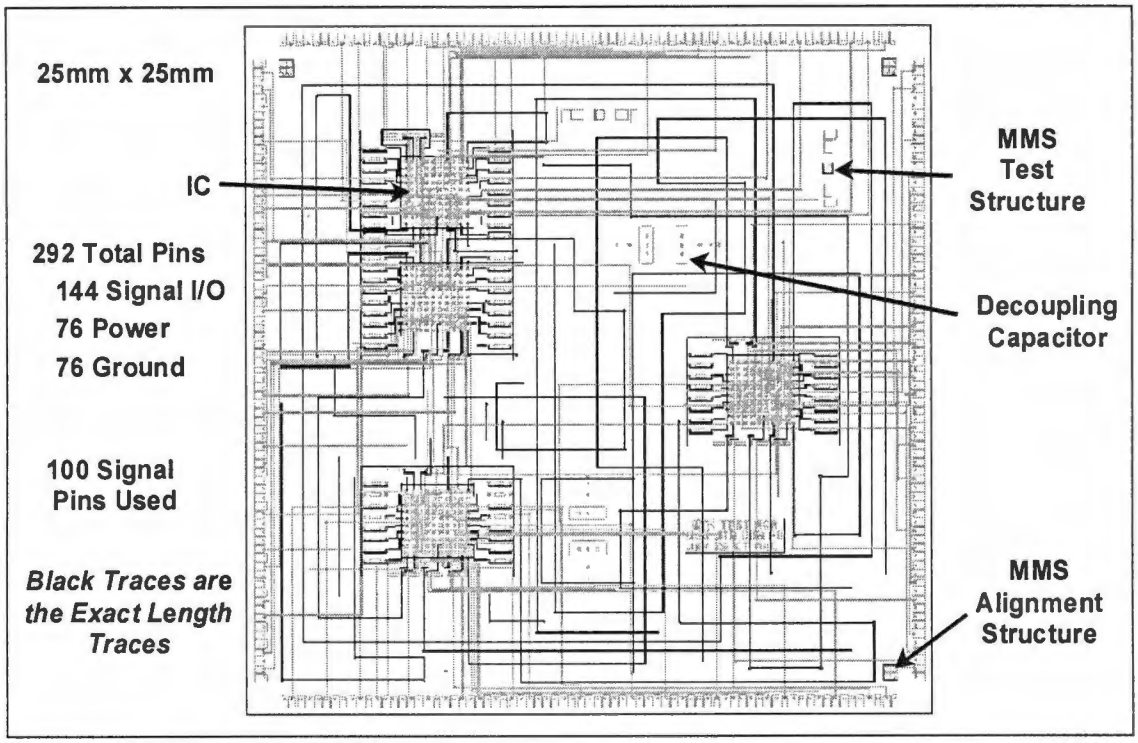


Figure 48: MCM layout.

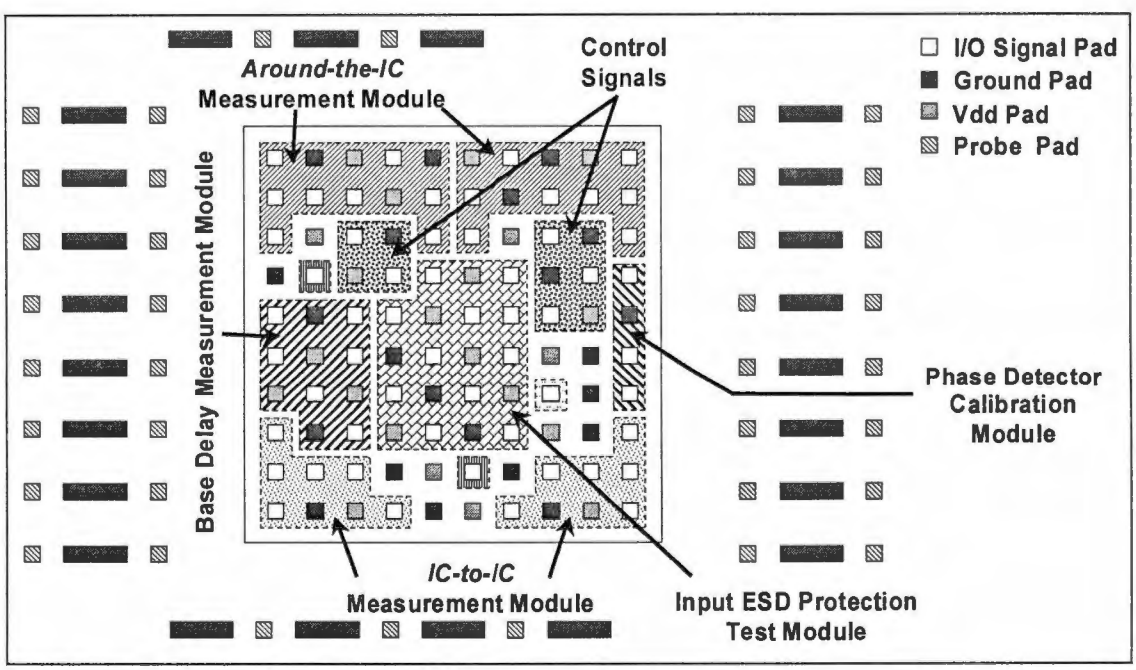


Figure 49: IC partitioning with probe pad sites.

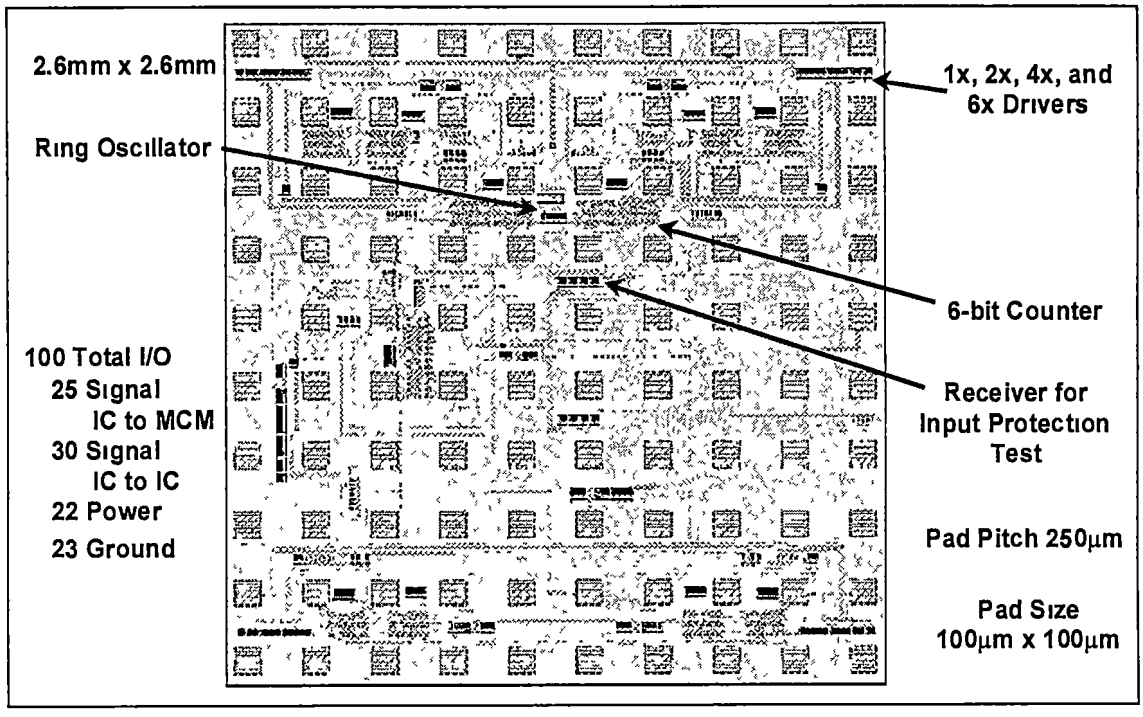
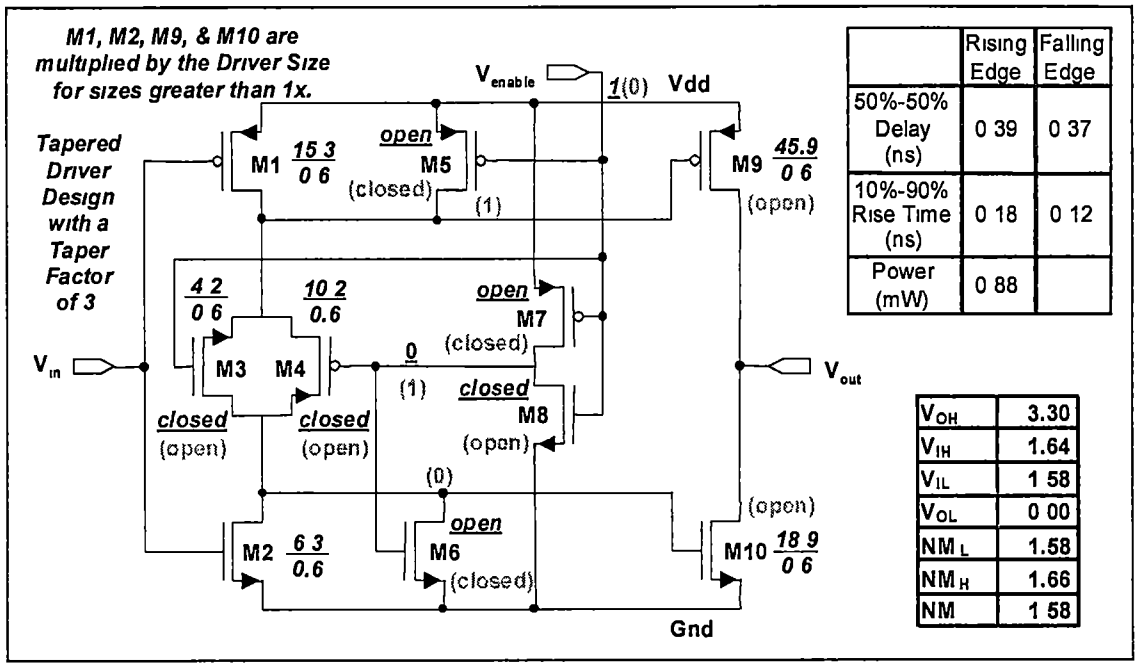


Figure 50: IC layout

Tri-state Driver

The 1x tri-state driver is shown in Figure 51 on page 59 The two stage driver uses M1, M2, M9 and M10 as the driving transistors and all the other transistors are used to tri-state the driver To enable the driver, V_{enable} needs to be set to 1. This opens M5 and M7 while it closes M3 and M8, which opens M6 and closes M4 With M3 and M4 closed, the drains of M1 and M2 are connected, resulting in a two-stage driver configuration When V_{enable} is set to 0, M5 and M7 close while M3 and M8 become opened This opens M9 and M10, setting the output in a tri-state condition



	Rising Edge	Falling Edge
50%-50% Delay (ns)	0 39	0 37
10%-90% Rise Time (ns)	0 18	0 12
Power (mW)	0 88	

V_{OH}	3.30
V_{IH}	1.64
V_{IL}	1 58
V_{OL}	0 00
NM_L	1.58
NM_H	1.66
NM	1 58

Figure 51: 1x tri-state driver

4. RESULTS

The IC was submitted for fabrication to MOSIS in December 1996 It was fabricated by Hewlett-Packard in April of 1997 The MCM was submitted to MIDAS for fabrication in May 1997 The MCM was fabricated by MMS in March of 1998 This is when the first problem was noticed. Full chip simulations showed that the 3-bit counters had setup time problems that caused glitches during its operation The 1-bit version of the circuit is shown in Figure 52 on page 61 The glitches don't show up during the simulation of the 1-bit counter but shows up when three 1-bit versions are cascaded to make a 3-bit counter, see Figure 53 on page 61 This glitch could have been eliminated by connecting the output of the counter to a latch that is clocked near the frequency of the output, 6 MHz in this case This shows the danger of grabbing a circuit from a book and using it without properly studying it and making sure it works as described in technology you are using A new counter was designed without an enable that does not have this glitch, see Figure 54 on page 62 From the simulation results shown in Figure 55 on page 62, this counter does not have any setup time problems in the 0 5 µm technology

The MCMs and ICs were sent to MCNC for assembly in September 1998 To assembly the IC with the MCMs, solder bumps were added to the IC wafers, then each wafer was sawed into individual ICs The ICs were then heated to slightly melt the solder bumps and they were flipped over and attached to the MCMs When the array I/O for IC was laid out, it was not taken into consideration the fact that the ICs where flipped upside down This resulted in the IC's I/O not matching correctly with the I/O footprint on the MCM Figure 56 on page 63 shows the footprint on the MCM, the layout of the IC's I/O, and that the IC pads will not match up correctly when flipped Figure 57 on page 63 shows the correct orientation for the IC's I/O so that it would match up with the MCM footprint when the IC was flipped over

Since the ICs and the MCMs could not be assembled, five ICs were packaged into 44 lead J-shaped chip carriers (CCJ04403) by Spectrum Semiconductor Materials, Inc in November 1998, see Figure 58 on page 64 The IC was going to be placed in a PLCC socket and partially tested to make sure they were known good die As the test structure was being created, the layout was examined again and it was

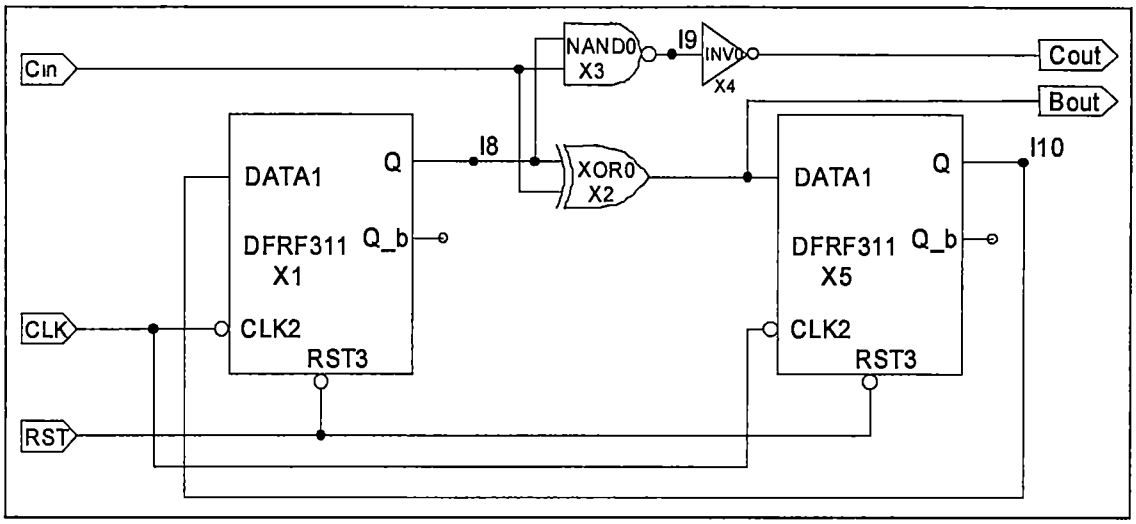


Figure 52: 1-bit counter with enable

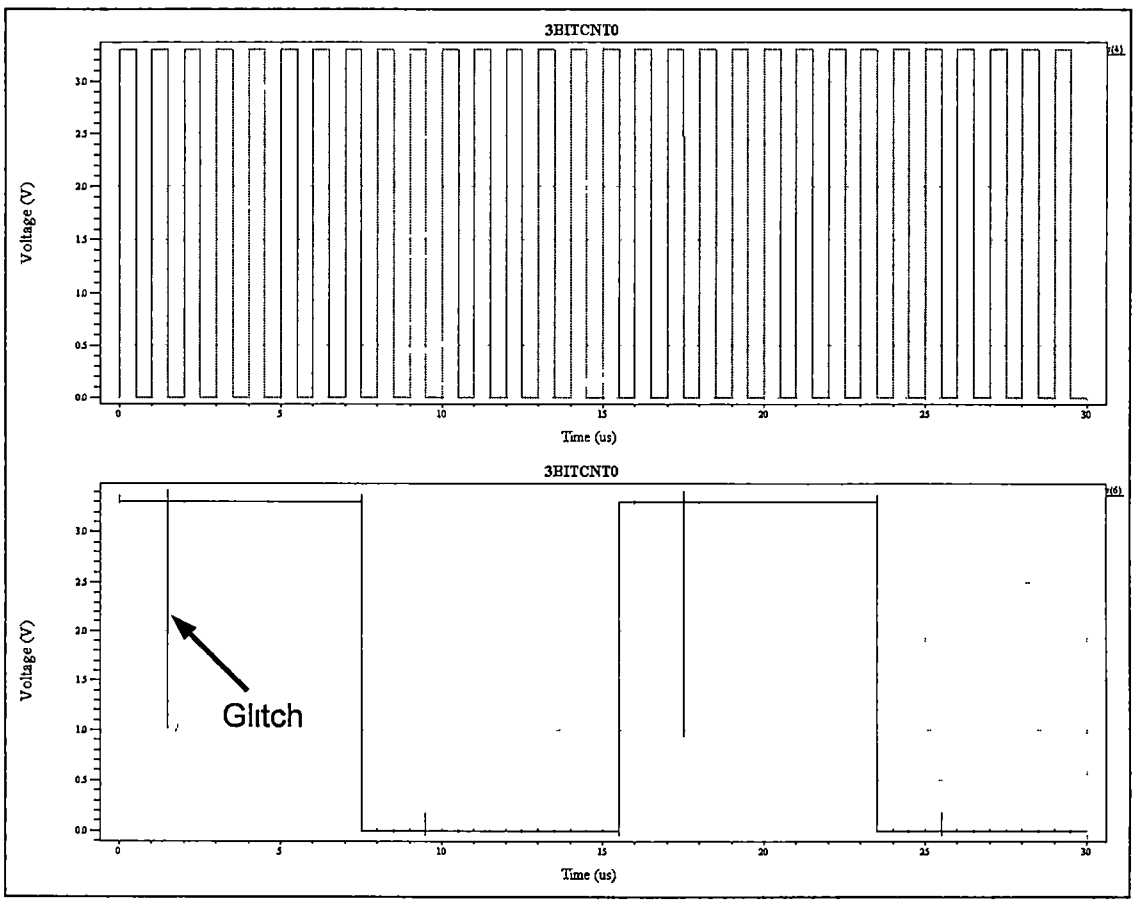


Figure 53: 3-bit counter simulation.

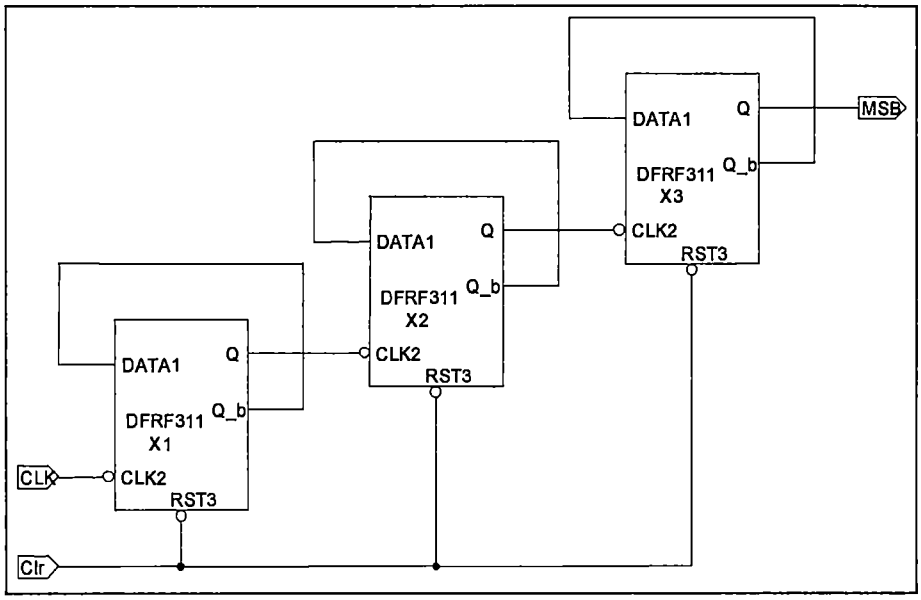


Figure 54: Corrected 3-bit counter

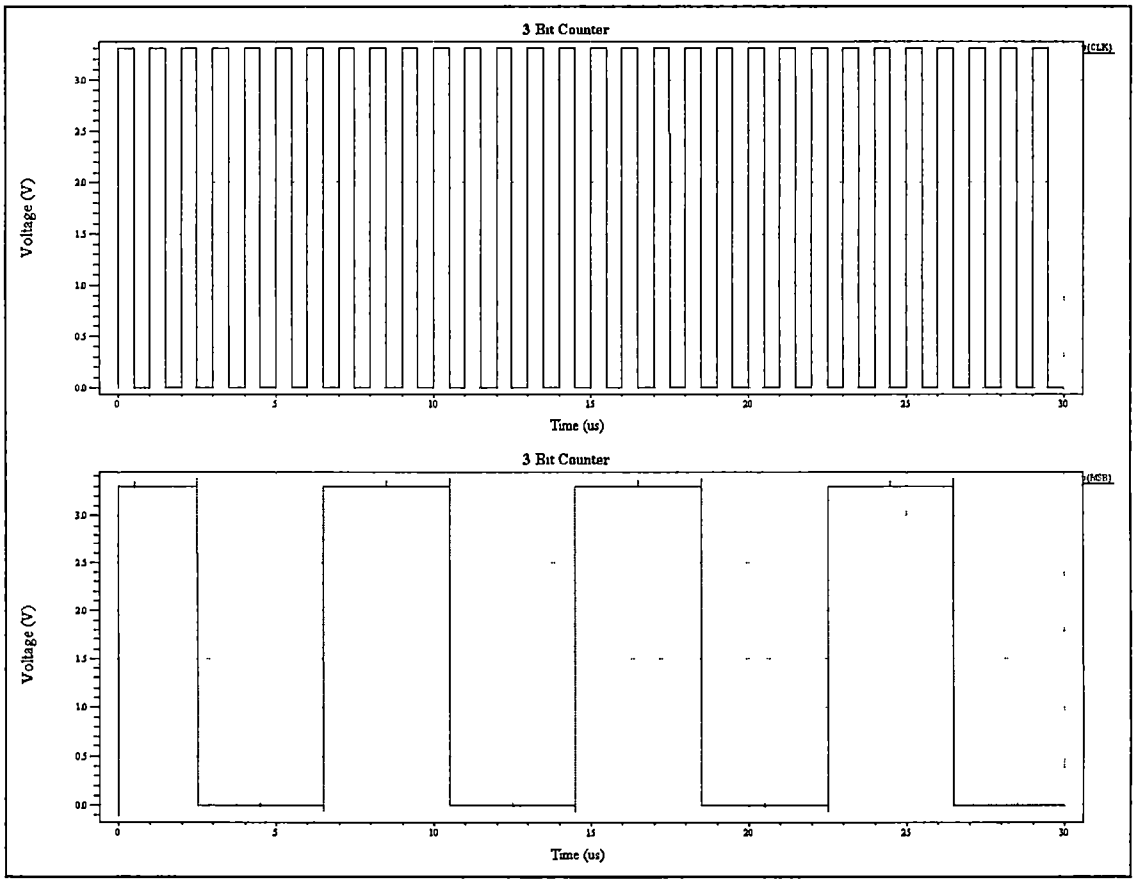


Figure 55: Corrected 3-bit counter simulation

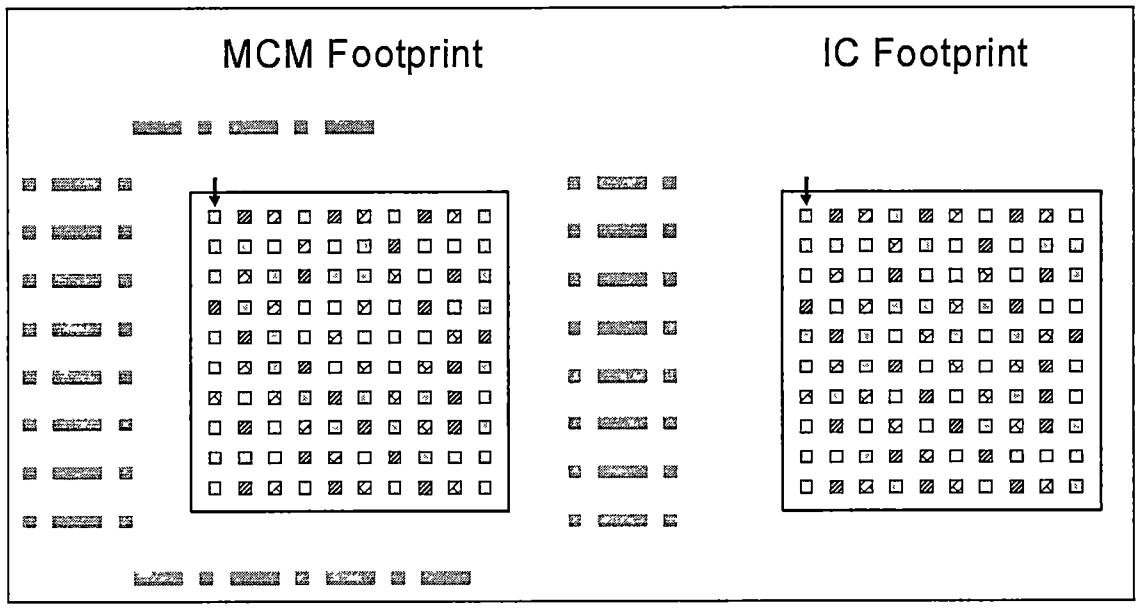


Figure 56: MCM and IC orientation

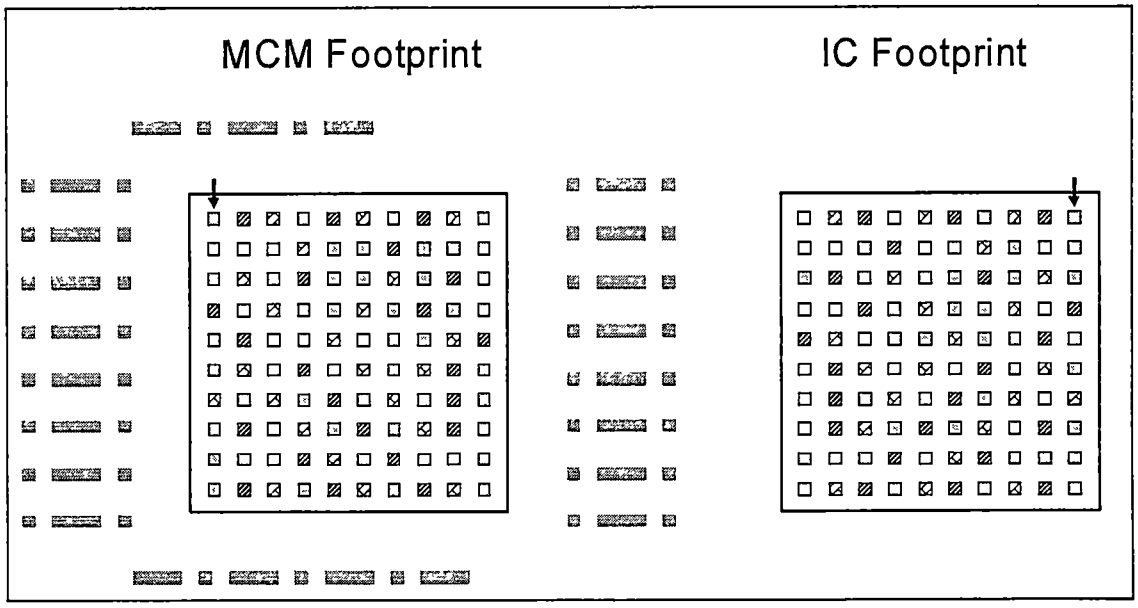


Figure 57: MCM and IC with the correct orientation

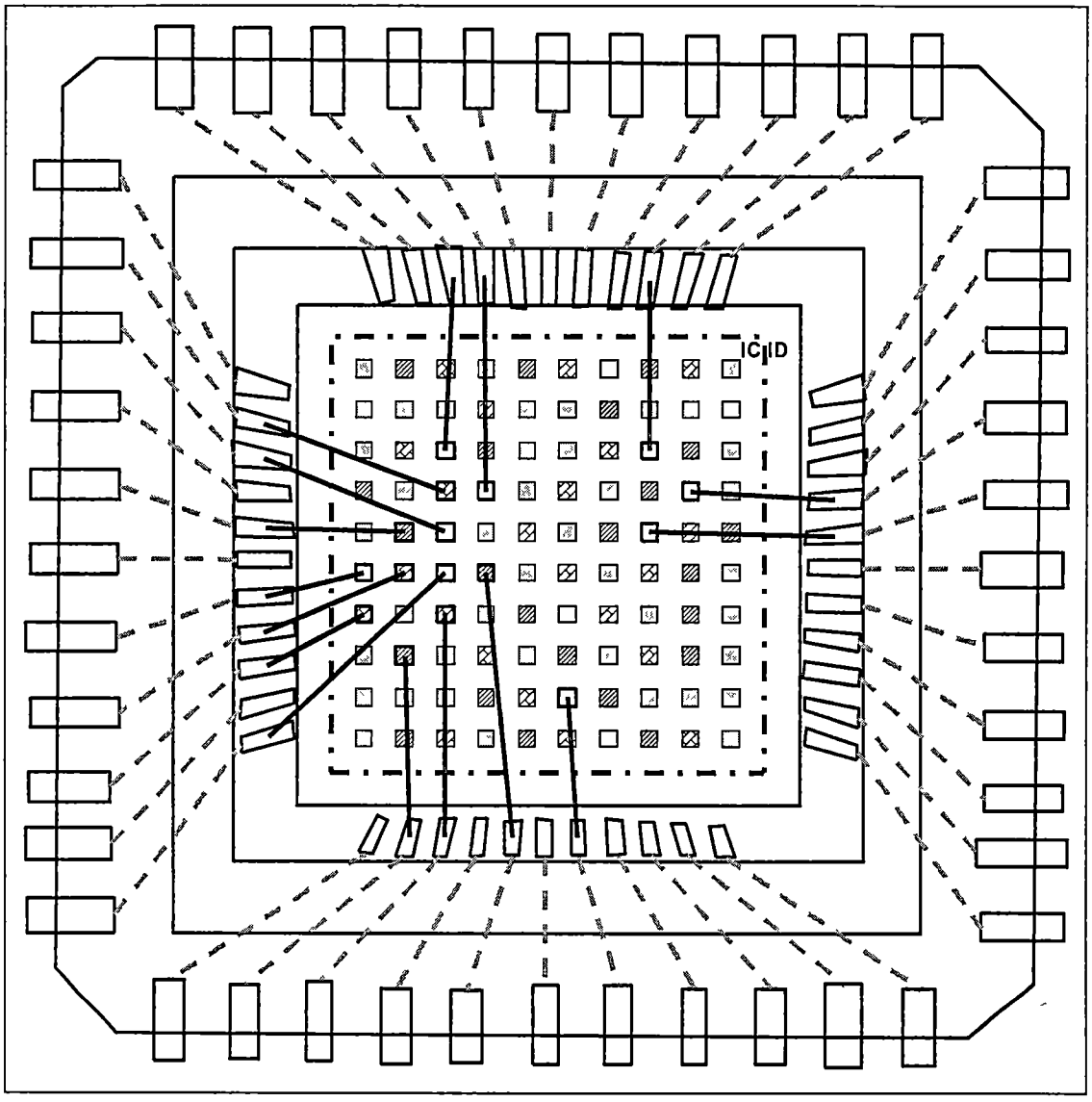


Figure 58: IC die wire bonded in CCJ04403 package

discovered that Vdd was not connected for the test selection decoder and that Clear was not connected to the ring oscillator counter, see Figure 59 on page 66 Both of these connections were floating which meant that testing the IC would be useless Due to time and financial constraints and that a whole wafer is needed for adding the solder bumps, the IC was not resubmitted for fabrication with the layout corrected The problems in the layout clearly show the major problems that can happen when a full verification procedure is not followed The layout was checked for design rule errors but no layout versus schematic checks were made and no post-layout simulations were performed Both of these checks would have caught the layout mistakes and the setup time problems

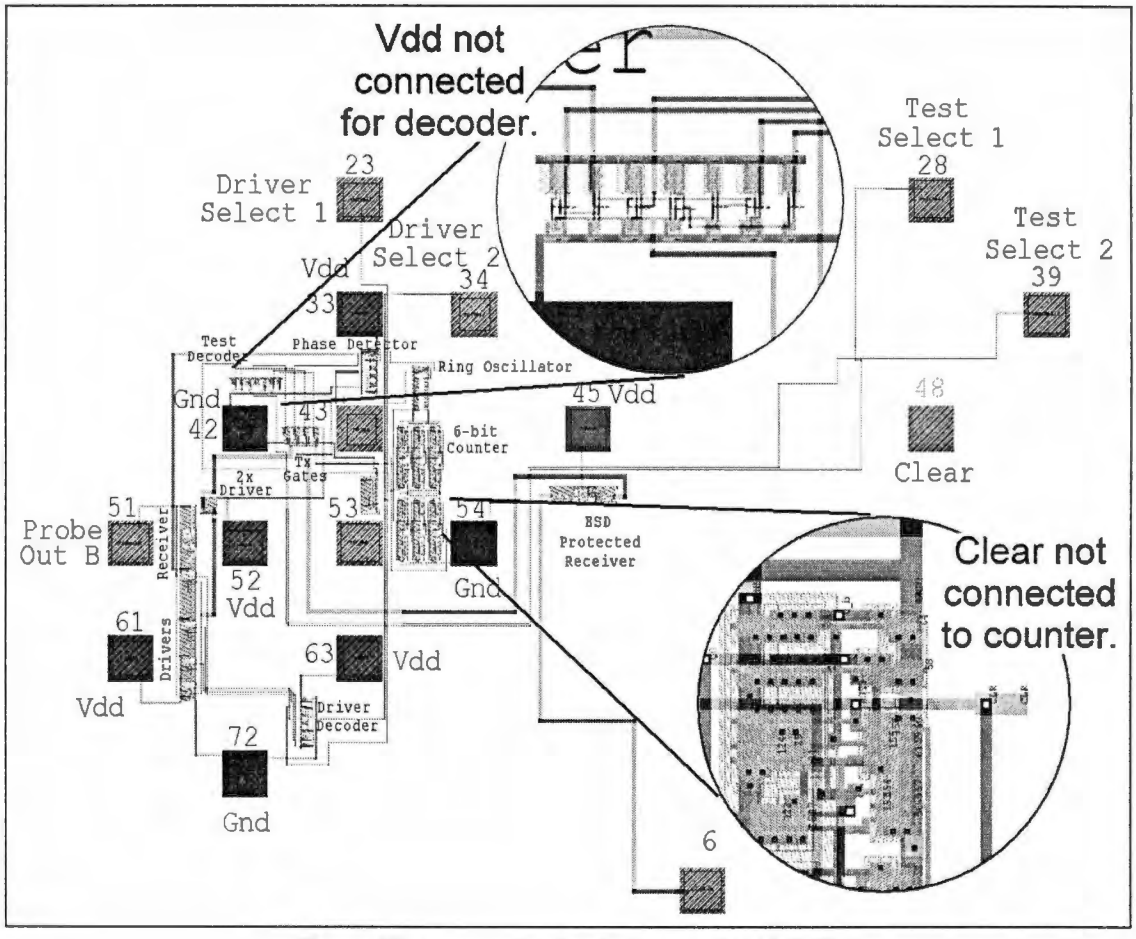


Figure 59: Layout mistakes in the wire bonded IC.

5. SUMMARY

The Multichip Module (MCM) package environment presents a different environment than that for which most Integrated Circuit (IC) drivers were designed The objective of this project was to design optimized I/O drivers for inter-die (IC to IC) traces on an MCM-D substrate

The Hewlett-Packard's 0 5-μm CMOS-14B IC process and MMS MCM-D processes were characterized and modeled with HSPICE® using lossy transmission lines From the modeling, it was found that MCM traces (2 4 Ω/cm) are much less resistive than IC traces (26 0 Ω/cm) because the MCM traces are thicker than IC traces and the conductor used (copper) is less resistive than the aluminum conductors used in ICs The difference in resistance dominated the difference in signal response between an IC trace and an MCM trace A 4 cm length trace on an MCM has the same delay as a 2 26 cm trace on an IC for a 6x driver and equal trace widths

The delay of the IC traces varied exponentially with trace length while the delay of the MCM traces varied linearly because the effective 3 dB frequencies of the IC traces were near the clock frequency (200 MHz) while the effective 3 dB frequencies of the MCM traces were much higher than the clock frequency From the simulations, a 4 cm MCM trace has 33% less delay and 70% faster risetime than an 4 cm IC trace of comparable width and dissipates about the same amount of power

From the modeling results, new IC drivers were designed for incorporation in a test system designed to study various driver-net-load combinations for different delays and signal integrity The drivers were fabricated via MOSIS on Hewlett-Packard's 0 5-μm CMOS-14B process and were solder-bumped by MCNC for area-array I/O Four of these ICs were going be assembled on an MCM-D substrate fabricated by Micro Module Systems via MIDAS but they were not due to layout problems in the IC.

Four different test strategies were developed to measure the delay of MCM traces, and a test strategy was developed to test the need for ESD protection between IC to IC traces A phase detector and ring oscillator was used to measure delay directly and two 3-bit counters with a split clock was used to

measure the upper clock frequency per trace length Problems in the IC consisted of setup time problems in the counter, which caused extra counts The array I/O for the IC was not mirrored to take into consideration the fact that the IC is flipped when attached to the MCM The ICs were packaged for functionality testing but the Vdd of the test selection decoder and the clear for the counters were not connected, making it impossible to test the IC The assembled ICs and MCM were going be tested and the measured results were going be correlated with those obtained via simulation This experimental verification would have allowed us to improve our modeling and give us the capability to design a variety of I/O drivers that can be used with various MCM-D applications

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[6] Micro Module Systems D500 process specifications A copy of this specification can be found in Appendix D

[7] Hewlett-Packard's 0.5-micron CMOS-14B process specifications Run N56S A copy of this specification can be found in Appendix E.

[8] *Transmission Lines*, HSPICE User's Manual Volume 2 - Elements and Models, Meta-Software, Version H92, 1992

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APPENDICES

APPENDIX A

Microstrip Capacitance Calculation

1. First compute equivalent thin-strip widths

$\mu m \equiv 10^{-6}\ m \quad \varepsilon_0 = 8.854\ 10^{-2}\ \frac{pF}{cm} \quad t = 1.2\ \mu m \quad h = 4\ \mu m$

$$w_{prime}(w) = w + \frac{t}{\pi}\left[(1+\ln(4)) - \frac{1}{2}\ln\left[\left(\frac{t}{h}\right)^2 + \left[\frac{1}{\pi\left(\frac{w}{h}+1.1\right)}\right]^2\right]\right] \quad \text{Eq. 4.5}$$

For w = 1.2μm, t/h = 0.3

$w_{prime}(1.8\ \mu m) = 3.098\ \mu m$

For w = 4.8μm, t/h = 0.3

$w_{prime}(4.8\ \mu m) = 6.135\ \mu m$

2. Compute free space capacitance

$\frac{w_{prime}(1.8\ \mu m)}{h} = 0.774$

$\frac{C_0}{\varepsilon_0} = 2.666$ Table 3.1

$\frac{w_{prime}(4.8\ \mu m)}{h} = 1.534$

$\frac{C_0}{\varepsilon_0} = 3.648$ Table 3.1

3. Compute the effect of the dielectric layer

$\varepsilon_r = 3.9$

$y = 1 - \frac{1}{\varepsilon_r}$

$x(w) = \ln\left(\frac{w_{prime}(w)}{h} + 0.125\right)$

$$Q = \begin{bmatrix} 6.51309\ 10^{-01} & -2.2516\ 10^{-02} & -3.32199\ 10^{-03} & -3.85162\ 10^{-03} \\ 6.65212\ 10^{-02} & -1.26976\ 10^{-03} & -6.8053\ 10^{-05} & -1.03524\ 10^{-03} \\ 1.64039\ 10^{-02} & 2.59784\ 10^{-03} & 2.74253\ 10^{-04} & 6.52501\ 10^{-04} \\ 3.95737\ 10^{-04} & 6.69075\ 10^{-04} & 6.84457\ 10^{-05} & 3.34213\ 10^{-04} \\ -1.84365\ 10^{-03} & -2.11987\ 10^{-04} & 2.1372\ 10^{-05} & -9.56514\ 10^{-05} \\ -1.54945\ 10^{-05} & -9.69139\ 10^{-05} & -2.71033\ 10^{-05} & -3.65429\ 10^{-05} \\ 6.53285\ 10^{-05} & 2.47087\ 10^{-05} & 4.08141\ 10^{-06} & 1.01064\ 10^{-05} \end{bmatrix}$$

$$q(w) = \sum_{i=0}^{6}\sum_{j=0}^{3} Q_{i,j}\, x(w)^i\, y^j \quad \text{Eq. 3.43}$$

$$\varepsilon_{eff}(w) = 1 + q(w)(\varepsilon_r - 1) \quad \text{Eq. 3.45}$$

$q(1.8\ \mu m) = 0.6244579$

$\varepsilon_{eff}(1.8\ \mu m) = 2.811$

$q(4.8\ \mu m) = 0.6688981$

$\varepsilon_{eff}(4.8\ \mu m) = 2.94$

4. Compute effective capacitance model

$$C(w) = \frac{C_0}{\varepsilon_0}\varepsilon_{eff}(w)\varepsilon_0 \quad \text{Eq. 3.6}$$

For w = 1.8 μm

$C_{1.8} = 2.666\ \varepsilon_{eff}(1.8\ \mu m)\varepsilon_0$

$C_{1.8} = 0.66\ \frac{pF}{cm}$

For w = 4.8 μm

$C_{4.8} = 3.648\ \varepsilon_{eff}(4.8\ \mu m)\varepsilon_0$

$C_{4.8} = 0.95\ \frac{pF}{cm}$

APPENDIX B

Pad Capacitance Calculations

Constants

$aF \equiv 10^{-18}$ $um \equiv 10^{-6}$ $pF \equiv 10^{-12}$ $fF \equiv 10^{-15}$ $nF \equiv 10^{-9}$ $cm \equiv 10^{-2}$

Chip Pad Capacitance for Run: N56S

Fringe Capacitance	Area Capacitance	
$C_{fm3} = 31 \left(\frac{aF}{um}\right)$	$C_{am3} = 7 \left(\frac{aF}{um^2}\right)$	**Metal 3 to the substrate.**
$C_{fm2} = 77 \left(\frac{aF}{um}\right)$	$C_{am2} = 11 \left(\frac{aF}{um^2}\right)$	**Metal 2 to the substrate.**
$C_{fm1} = 86 \left(\frac{aF}{um}\right)$	$C_{am1} = 36 \left(\frac{aF}{um^2}\right)$	**Metal 1 to the substrate.**

$Pad_{length} = 100\ um$ $Pad_{area} = Pad_{length}^2$

$Pad_{cap\_m1} = Pad_{area} C_{am1} + 4 C_{fm1} Pad_{length}$

$Pad_{cap\_m2} = Pad_{area} C_{am2} + 4 C_{fm2} Pad_{length}$

$Pad_{cap\_m3} = Pad_{area} C_{am3} + 4 C_{fm3} Pad_{length}$

$Pad_{cap\_m1} = 394.4 \cdot fF$ $Pad_{cap\_m2} = 140.8 \cdot fF$ $Pad_{cap\_m3} = 82.4 \cdot fF$

MCM Pad Capacitance for the MMS process.

Area Capacitance — **Area capacitance values are from the power plane to the substrate.**

$C_{a\_x} = 0.7 \left(\frac{nF}{cm^2}\right)$ **X Signal Layer to the substrate**

$C_{a\_y} = 0.7 \left(\frac{nF}{cm^2}\right)$ **Y Signal Layer to the substrate**

$Pad_{length} = 100\ um$ $Pad_{area} = Pad_{length}^2$

$Pad_{cap\_x} = Pad_{area} C_{a\_x}$ $Pad_{cap\_y} = Pad_{area} C_{a\_y}$

$Pad_{cap\_x} = 70 \cdot fF$ $Pad_{cap\_y} = 70 \cdot fF$

APPENDIX C

Distributed RC Analysis

Global definitions

$sec \equiv 1t \qquad hertz \equiv \frac{2\pi}{sec} \qquad Mhz \equiv 10^{6}\ hertz \qquad nH = 1\ 10^{-9}\ henry$

Transmission Parameters for MMS-MCM 16 um Trace Width

$k = 0\ 9 \qquad R_0 = 2\ 4\ \frac{\Omega}{cm} \qquad C_0 = 1\ 20\ \frac{pF}{cm} \qquad L_0 = 3\ 50\ \frac{nH}{cm}$

$Len_k = (k+1)\ cm \qquad R_k = R_0\ Len_k \qquad C_k = C_0\ Len_k \qquad L_k = L_0\ Len_k$

$n = 50 \qquad i = 0\ n \qquad min = 10^{6} \qquad max = 10^{12}$

r is a log ratio of maximum and minimum frequencies

$r = \ln\left(\frac{max}{min}\right) \qquad s_i = min\ e^{i\frac{r}{n}}\ hertz \qquad dB(\alpha) = 20\log(|\alpha|)$

Frequency Response

$$Dist\_RC(s,k) = \frac{1}{\cosh\left(\sqrt{s\ R_k\ C_k}\right)}$$

Frequency Response of a Distributed RC circuit

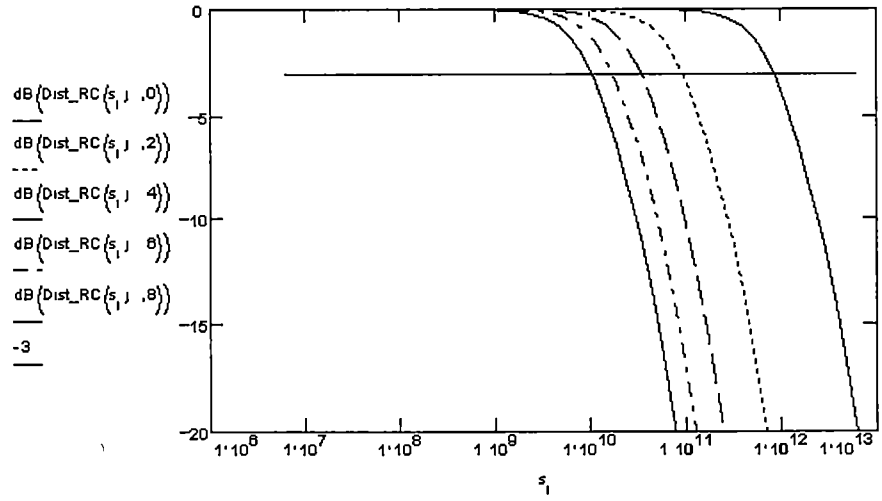
The negative value is so that the vector will be in ascending order. The LINTERP function requires all vectors to be ascending.

$Dist\_RC\_vx_{i,k} = dB\left(Dist\_RC\left(s_{i,j},k\right)\right)$

$Dist\_RC\_\omega_{3db_k} = linterp\left[(-Dist\_RC\_vx)^{<k>},s,3\right]$

$Len^{T} = (1\ 2\ 3\ 4\ 5\ 6\ 7\ 8\ 9\ 10)\cdot cm$

$Dist\_RC\_\omega_{3db}{}^{T} = (134024\ 33506\ 14892\ 8376\ 5365\ 3723\ 2735\ 2094\ 1655\ 1341)\cdot Mhz$



APPENDIX D

MMS MCM Specifications

Micro Module Systems (MMS)
10500 Ridgeview Court
Cupertino, CA 95014-0736

NOTE Currently the MIDAS offers the MMS D500 process on Aluminum Below references other options available directly from the foundry

MECHANICAL CHARACTERISTICS

Substrate Material Aluminum, Ceramic*, Silicon*
Substrate Size 6"
Conductor Metal Copper
Dielectric Material Polyimide
Signal Layers 5 (2 signal, 2 planes, 1 pad)
Signal Type MicroStrip
Signal Pitch 3 options· 75, 62 and 50 um
* These substrates are Engineering only The Aluminum substrate exists as a part of a qualified process.

Number of Modules/Substrate (Based on MIDAS Standard Sizes)
25mm sq 12
37mm sq 6
47mm sq 4

Layer Thicknesses (All values in µm)

LAYER	Aluminum	Ceramic	Silicon
Substrate	1270 0 (50mil)	635 0 (25mil)	635.0 (25mil)
Planarization	n/a	40 0	n/a
Via1	6 0	6 0	6 0
Via2	12.0	12.0	12 0
Via3	5 5	5 5	5 5
Via4	12 0	12 0	12 0

ELECTRICAL CHARACTERISTICS

Dielectric Constant (on all via layers) 3 5

Sheet Resistivity (All values in mOhms/sq)

LAYER	Aluminum	Ceramic	Silicon
Substrate	<0.05	n/a	n/a
Met0	n/a	9 0	9 0
Met1	9 0	9.0	9.0
Met2	4 5	4 5	4 5
Met3	4 5	4 5	4 5
Met4	2 0	2 0	2 0

Power Plane Capacitance (nF/cm**2)

Substrate to Met1A	Aluminum >0 70	Ceramic	Silicon >0 70	
X/Y Layer Characteristics				
Layer	75um pitch	62um pitch	50um pitch	Units
MET2 (X-Signal)				
Width (drawn)	16 0	16 0	16 0	um
Width (final)	19 0	19 0	19 0	um
Space (final)	56 0	43 0	31 0	um
Impedance	50 0	50 0	50.0	Ohms
X-Talk (adjacent lines)	1 9	2 9	3 9	%
Resistance	2 4	2 4	2 4	Ohms/cm
Capacitance	1 2	1 2	1 2	pF/cm
Inductance	3 0	3 0	3 0	nH/cm
MET3 (Y-Signal)				
Width (drawn)	20 0	20 0	20 0	um
Width (final)	23 0	23 0	19 0	um
Space (final)	52 0	39 0	31 0	um
Impedance	58 0	58 0	69 0	Ohms
X-Talk (adjacent lines)	3 2	4 8	9 1	%
Resistance	2 0	2 0	2 4	Ohm/cm
Capacitance	1 0	1 0	1 1	pF/cm
Inductance	3.4	3 4	3 5	nH/cm

THERMAL CHARACTERISTICS

Thermal Resistance (cm^2-degC/W), Junction (Si IC) to Case (Substrate Backside)

Substrate Material (Typ Density)	No Thermal Vias	With Thermal Vias
Al	1 70	0 75
Si	1 75	0 80
Ceramic	1 75	0 80

DESIGN CONSIDERATIONS

1)	Chip to Chip Spacing	500 µm min 2250 µm max
2)	Die Pad Pitch	
	3 Options	150, 124, 114 µm (w/out fan out)
3)	Via Spacing	Via 1,2 80 µm min (w/ 50 µm pitch)
		Via 3,4 50 µm min (w/ 50 µm pitch)
4)	Via Diameter.	20 µm drawn, 25 to 55 µm final, depending on polyimide thickness
5)	Min Feature Size.	50 µm standard minimum
	(Top Layer)	(smaller possible)
6)	Die Wirebond Pad·	100x600 µm standard
		100x300 or 200x200 µm min
7) Min Edge Connect Pad		200x400 µm standard
		100x300 or 200x200 µm min

mmstech82394v2jp

APPENDIX E

MOSIS Parametric Test Results

RUN: N56S VENDOR. HP-NID
TECHNOLOGY· SCN05H FEATURE SIZE: 0.5
mıcrons

INTRODUCTION: Thıs report contaıns the lot average results obtaıned by MOSIS from measurements of the MOSIS test structures on each wafer of thıs fabrıcatıon lot. The SPICE parameters obtaıned from sımılar measurements on a selected wafer are also attached

COMMENTS Hewlett Packard CMOS14TB run.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.9/0.60			
Vth		0.71	-0 90	Volts
SHORT	5 4/0.60			
Vth		0.59	-0 84	Volts
Vpt		9 4	-8.6	Volts
Vbkd		10.9	-8.7	Volts
Idss		2259	-1106	uA
WIDE	36/0.60			
Ids0		18 1	-4 9	pA
LARGE	50/50			
Vth		0 71	-0 93	Volts
Vjbkd		11.7	-10.1	Volts
Ijlk		-11.7	3 1	pA
Gamma		0 62	0 49	V^0 5
Delta length (L_eff = L_drawn-DL)		0 08	0.13	mıcrons
Delta wıdth (W_eff = W_drawn-DW)		0 41	0 46	mıcrons
K' (Uo*Cox/2)		72 6	-22.2	uA/V^2

COMMENTS. Delta L varıes wıth desıgn technology as a result of the dıfferent mask bıases applıed for each technology. Please adjust the delta L ın thıs report to reflect the actual desıgn technology of your submıssıon.

Desıgn Technology	Delta L
SCN_SUBM (lambda=0 3), CMOSH, HP_CMOS14TB	no adjustment
SCN (lambda=0.35)	add 0.1 um

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

PROCESS PARAMETERS	N+DIFF	P+DIFF	N\PLY	POLY	MTL1	MTL2	MTL3	N WELL	UNITS
Sheet Resistance	2.4	2.1	699	2 6	0.08	0.07	0.03	821	ohms/sq
Width Variation (measured - drawn)	-0.40	-0.35		-0.08	0.34	0.24	-0.18		microns
Contact Resistance	2 3	2.1		2 6		0 61	0 62		ohms
Gate Oxide Thickness	96								angstrom

COMMENTS: N\PLY is n-well under poly.

CAPACITANCE PARAMETERS	N+DIFF	P+DIFF	POLY	METAL1	METAL2	METAL3	UNITS
Area (substrate)	537	926	87	36	11	7	aF/um^2
Area (poly)				58	13	8	aF/um^2
Area (metal1)					31	10	aF/um^2
Area (metal2)						28	aF/um^2
Area (N+active)			3585	59	15	7	aF/um^2
Area (P+active)			3637				aF/um^2
Fringe (substrate)	205	229		86	77	31	aF/um
Fringe (N+active)			38				aF/um
Fringe (poly)				55	36	41	aF/um
Fringe (metal1)						61	aF/um
Fringe (metal2)						66	aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1 0	1.30	Volts
Vinv	1 5	1.46	Volts
Vol (100 uA)	2.0	0.20	Volts
Voh (100 uA)	2.0	3.03	Volts
Vinv	2 0	1 56	Volts
Gain	2.0	-15.85	
Ring Oscillator			
DIV4 (31 stages)		137.22	MHz

==========

SPICE Model Parameters for 0.8 um CMOS
and Other Submicrometer Technologies

Summary

Completely new data gathering and parameter optimization strategies for submicrometer technologies are under development at MOSIS. As these strategies are tested and proven to be accurate, new sets of submicrometer SPICE parameters will be made available. During the transition, and for some period thereafter, Level=3 parameters will continue to be provided. Unfortunately, for the reasons stated in the file submicron-spice-parameters.inf (located in the MOSIS FTP access: ftp/pub/mosis/info), we are not able to guarantee the accuracy of these Level=3 parameters in submicrometer technologies. Designers should begin thinking about making a transition away from Level=3 model parameters.

MOSIS will continue offering BSIM model parameters, Level=4, along with the Level=3 parameters. We will be supplying Level=28 (BSIM2) and

```
Level=47 (BSIM3 v2) in the near future to improve simulation
performance in submicrometer technologies
================================================================

 N56S SPICE LEVEL3 PARAMETERS

 MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=1.0000E-08 XJ=0.200000U TPG=1
+ VTO=0.7812 DELTA=2 4510E-01 LD=4 0510E-08 KP=1.8847E-04
+ UO=545 8 THETA=2.5170E-01 RSH=2 1290E+01 GAMMA=0.6200
+ NSUB=1.3810E+17 NFS=7.0710E+11 VMAX=1.8610E+05 ETA=2.2420E-02
+ KAPPA=9.6720E-02 CGDO=3.66E-10 CGSO=3.66E-10
+ CGBO=4.0161E-10 CJ=5 4E-04 MJ=0 6 CJSW=1.5000E-10
+ MJSW=0.32 PB=0.99
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 4.1360E-07


 MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=1 0000E-08 XJ=0 200000U TPG=-1
+ VTO=-0.9197 DELTA=2 4830E-01 LD=6.7120E-08 KP=4.4546E-05
+ UO=129.0 THETA=1 7800E-01 RSH=3 4290E+00 GAMMA=0 5230
+ NSUB=9.8260E+16 NFS=6.4990E+11 VMAX=3.0560E+05 ETA=1.7820E-02
+ KAPPA=6.3410E+00 CGDO=3 66E-10 CGSO=3.66E-10
+ CGBO=4 2772E-10 CJ=9.3191E-04 MJ=0 51 CJSW=1.5E-10
+ MJSW=0 193 PB=0.95
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 4 6180E-07

================================================

N56S SPICE BSIM1 (Berkeley Level 4, HSPICE Level 13) PARAMETERS

NM1 PM1 DU1 DU2 ML1 ML2
*
*PROCESS=HP
*RUN=n56s
*WAFER=97
*Gate-oxide thickness= 100 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 0 9/0 6, 1.8/0.6, 5 4/0 6, 1.8/1 8, 1.8/5.4
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=8-Sep-1995
*
*NMOS PARAMETERS
*
-6.67767E-01,-9.88313E-03,-3 29367E-02
 8.60647E-01, 0 00000E+00, 0.00000E+00
 8 17935E-01,-4 65708E-02, 4.75791E-02
 4 25774E-02, 3 52629E-02,-2.77046E-03
-6 14649E-05, 1 89078E-02,-1.18479E-02
 5.83829E+02,1.40291E-001,5.07562E-001
 3.29586E-01, 9.77520E-02,-9.32319E-02
 1 99382E-02, 3.61973E-02,-2 86830E-03
 1.29121E+01,-8.28086E+00, 6.90864E+00
 7 54028E-04,-3.43366E-03, 5 18763E-04
 2 37991E-04,-1 61033E-03,-5.39861E-03
-6 35761E-03,-3 86200E-03, 5.33022E-03
-5 68012E-04, 1.22523E-03, 2.85097E-04
 6 84165E+02,-2.54285E+01, 9.21339E-01
 4.89160E+00,-1 90933E+00, 7.94142E+00
```

```
 4 83048E+00, 4.02423E+00,-5 33716E+00
 7 20765E-03,-1.37194E-04,-3 70674E-03
1.00000E-002, 2.70000E+01, 5 00000E+00
3.63E-010,3 63E-010,4.52505E-010
1 00000E+000,0.00000E+000,0.00000E+000
1 00000E+000,0.00000E+000,0 00000E+000
0 00000E+000,0.00000E+000,0 00000E+000
0.00000E+000,0.00000E+000,0 00000E+000
*
* Gate Oxide Thickness is 100 Angstroms
*
*
*PMOS PARAMETERS
*
-6 59693E-02,-1.78327E-02,-2.45473E-03
 7 68179E-01, 0.00000E+00, 0.00000E+00
 2 85648E-01,-1 64579E-02, 3.08917E-02
-6.62532E-02, 2 49518E-02, 4.62778E-04
-7.90844E-03, 1 92294E-02,-2.34646E-03
 1.41704E+02,2.14000E-001,5 34406E-001
 1.95407E-01, 6.22059E-02,-5.94668E-02
 8.56390E-03, 1 39477E-02, 7.65802E-04
 6.79470E+00,-1.43654E+00, 6.56475E-01
 1.08483E-04,-1 24539E-03, 9.77240E-05
 4.33468E-04, 1 42453E-04,-1.71650E-03
 8.73535E-03,-1.31646E-03, 4.78072E-04
 3.06834E-04, 4.41194E-04, 3.49198E-04
 1.47746E+02, 1.78644E+01, 1.24739E-01
 6.09155E+00,-1.61404E-01, 1 24507E+00
-3.18656E-01, 2.79732E+00, 1.71058E+00
-1.22826E-03, 1 06181E-04, 1.07711E-03
1.00000E-002, 2.70000E+01, 5.00000E+00
5.540E-010,5.54E-010,4 67045E-010
1.00000E+000,0.00000E+000,0.00000E+000
1 00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
*N+ diffusion:.
*
2 4,    7.732100e-04,    2.900000e-10,    1e-08,    0.8
0.8,    1.10106,    0.26,    0,    0
*
*P+ diffusion:·
*
2.1,    9.319100e-04,    1.563700e-10,    1e-08,    0.85
0 85,    0 487073,    0.47848,    0,    0
*
*METAL LAYER -- 1
*
0 08,    2 6e-05,    0,    0,    0
0,    0,    0,    0,    0
*
*METAL LAYER -- 2
*
0 07,    1.3e-05,    0,    0,    0
0,    0,    0,    0,    0
```

VITA

Nicolas Williams was born in Fort Leavenworth, Kansas on October 3, 1969 He attended The University of Tennessee at Knoxville, where he received a Bachelor of Science in Electrical and Computer Engineering in 1993. He then entered the Master's program in Electrical Engineering at The University of Tennessee at Knoxville A Master of Science in Electrical Engineering was received in May 2000 He is presently working with Tanner Research, Inc as a Product Manager His primary work involves marketing and development of complete EDA solutions for mixed signal and analog design on a PC computer