A Low-Power, Laser-Based Delta-Sigma Modulator for the Measurement of Atmospheric Gas Composition

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Abstract

With the increased attention on monitoring the atmospheric gas composition, new ways of accurately measuring these concentrations are needed. Along with the needed increase in measurement accuracy; size, space, and power reduction are also essential in modern systems. As semiconductor technology has advanced, the abilities to meet the previously mentioned criteria are becoming more realizable.

Instrumentation used to measure the atmospheric composition is traditionally large, taking up much needed space and using larger amounts of power. While the larger instrumentation provides the necessary accuracy, the other constraints are sacrificed. For this reason, a smaller, yet highly accurate solution is needed. The proof-of-concept (POC) solution that is proposed in this thesis is a delta-sigma (ΔΣ) modulator designed in a 0.5 micron (μm) bulk CMOS process. Using a 1.55 micron (μm) laser as the signal input while using a specified reference, the delta-sigma modulator will use oversampling and noise shaping to provide an accurate, one-bit digital output count that correlates the difference between the reference signal and the intensity of the laser signal that is input to the system. This allows for the possibility of a high resolution output, with high accuracy, and significant reductions in space used and power consumed.

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Chapter 1

Introduction

1.1 Motivation

Beginning in the 18th century, the first scientific studies to determine the gas composition of the Earth's atmosphere were conducted. In 1774, Joseph Priestly used an inverted container elevated above his work table to capture gases that were given off during various experiments. The gases were sealed inside the container using a pool of water or mercury. The gas was tested to see if it could sustain a flame or support life. Priestly found that a mouse would pass away when put into a container that could not support a flame. He then discovered that placing a green plant inside this container while exposing it to sunlight would "refresh" the air, permitting a flame to be sustained or a mouse to survive several times longer than before. What he discovered is now known as photosynthesis and oxygen [1]. Other chemists during this time were also conducting experiments and discovered carbon dioxide, hydrogen, and nitrogen to be among the other elements that comprised what they called air [1].

The discoveries of these individual elements led to more research into their effects on human health as well as their environmental impacts. In the 19th century, scientists started to hypothesize that the different gases that comprised the atmosphere could affect the climate. Joseph Fourier performed experiments that determined that the atmosphere allowed energy from the Sun to penetrate and reach the surface but would not let the infrared radiation escape back into space, thus keeping the Earth warmer than it would be

without this atmosphere [2]. In 1859, carbon dioxide and water vapor had been found to be the main contributors to the "greenhouse effect" [3]. While water vapor is a large component of the atmosphere, carbon dioxide was determined to be more influential in the Earth's long-term equilibrium temperature. In 1896, Svante Arrhenius completed his mathematical calculations that modeled the effect of removing half of the CO_2 in the atmosphere. It was found that removing half of the CO_2 concentration would reduce global temperatures by as much as 4 – 5 °C [4]. This was one of first times that a numerical value could be linked to the temperature of the Earth due to a specific amount of a certain gas in the atmosphere.

In 1938 it was observed by Callendar that over the last century that the atmospheric CO_2 concentration had risen approximately 10%. Along with this rise in CO_2 concentration, the surface temperature had also increased over the same time span [5]. This data collected by Callendar demonstrates that knowing the concentration of CO_2 in the atmosphere can give a direct correlation in monitoring and explaining surface temperature fluctuations.

By the late 21st century, computer models simulating the effects of increased atmospheric CO_2 substantiated earlier claims by scientists. Along with these models, ice core samples helped give scientists a window into the past to study the levels of CO_2 that were present in the soil. These ice core samples gave 150,000 years of history and they revealed that the climate had an up-down-up-down cycle with respect to temperature and CO_2 levels [6].

With the conclusion that monitoring the concentration of gases in the atmosphere is of great importance, specifically greenhouse gases, the ability to collect high resolution data becomes vital. Traditional chemical methods of measuring atmospheric composition have proven to have a major disadvantage. This disadvantage is the ability to only provide point monitoring measurements. Many times, more than a single point is needed in order to observe concentration changes over a period of time or in a specified area or volume. One method of retrieving atmospheric composition data is through laser detection. Using high powered pulsed lasers in conjunction with a differential absorption technique gives the ability to acquire a distribution of the gases in a large area [7].

Some concerns arise when looking at the laser detection methods currently in use. The first problem to be addressed is the large high-powered lasers that are necessary to perform accurate measurements. With the increasing need for reducing power costs along with physical size in sensing systems, the power of the laser need to be scaled down. With this scaling down of laser power, the sensing network must also be appropriately designed to accept these smaller laser signals.

As previously mentioned, the majority of laser based detection systems currently in use are large, as shown in Figure 1.1. These bulky systems are primarily dependent on large printed circuit board (PCB) designs with discrete parts and transistors. By lowering the laser power, and therefore the detectable signal, the size and the power consumption of the receiving networks can be significantly reduced, and ideally all placed on a single die. This reduction will be accomplished by using a silicon (Si) based bulk CMOS process to design the new network. This scaling down of transistors, reduced system

size, and scaled voltage supplies lead to creating an entire systems-on-a-chip (SOC). These SOCs can provide extremely high-resolution signal processing while still maintaining the desired reductions in size, power consumption, and weight. These are all critical factors when migrating these systems into aircraft or small satellite applications.



Figure 1.1 (Left) NASA Glenn-Lear 25 aircraft. (Middle) Lidar installed on the aircraft with sensor head assembly and (Right) dual aircraft racks [8].

Aircraft or small satellites are not the only applications that could benefit from reducing the size and the power of current gas concentration detection systems. The oil and gas industry could use this technology to measure levels of combustible gases in pipelines or in drilling wells. The buildup of certain gases would present possible explosive scenarios, but with a small reliable detection system in place constantly monitoring these gases, catastrophic events can be avoided.

1.2 Research Goal

Given that gases have specific radiation absorption patterns versus different wavelengths of light, it can be conceived that penetrating an air column via light source

with a known wavelength will produce an expected amount of that light to be absorbed and scattered by the gas. The transmittance pattern for different atmospheric gases is shown in Figure 1.2.

With the idea that atmospheric gases absorb certain wavelengths of light, the goal of this project was to design a delta-sigma modulator (ΔΣ) that will accurately measure the gas composition of the atmosphere via laser absorption and a photo-diode with a peak wavelength response of 1.55 μm. The photons entering the photo-diode will be stored as a charge and then converted into a low current signal over a period of time. This low-current signal is then sent to an integrator to transform the low-current signal into a voltage. The resulting voltage signal is then passed on to a switched capacitor resistor network. The signal voltage is compared with a reference signal voltage that is also the input to the switched capacitor resistor. This technique is known as correlated double sampling (CDS). In this proof-of-concept design, the reference signal voltage is off chip, giving the ability to find the most optimum reference level for accurate comparing. After the switched capacitor resistor, a comparator will give an output of “1” or “0”. A “1” is when the reference voltage is larger than the signal voltage, and a “0” is the contrary condition.

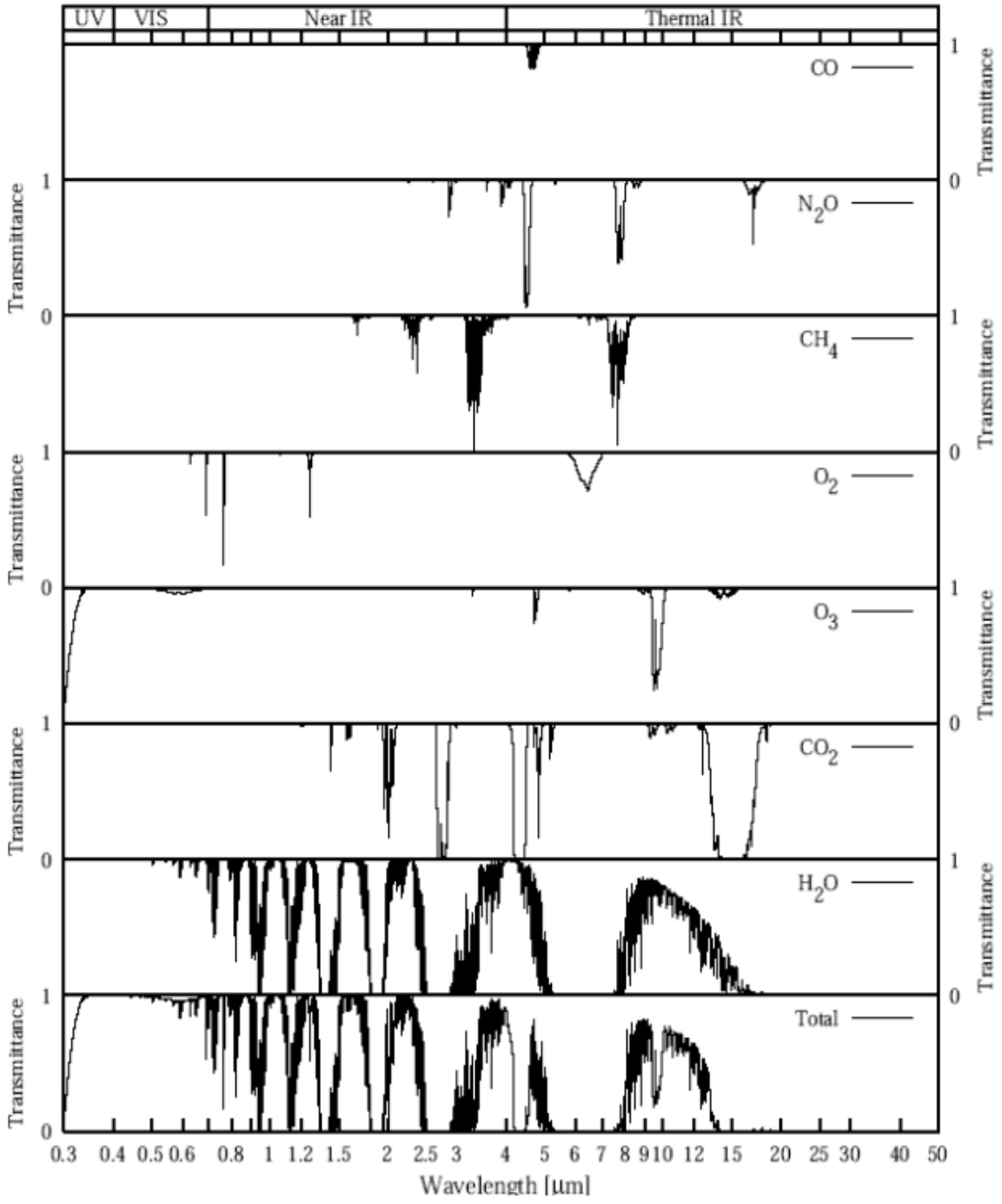


Figure 1.2 Atmospheric gas transmittance versus wavelength [9].

These “1” or “0” outputs are then used in a ratio comparing the number of “1’s” that are output to the total possible number of “1’s” in a given period. The basic structure of the proposed design is shown in Figure 1.3. This period is determined by the clock speed. The output resolution is determined by the number of clock counts in a user defined time period. For example, a clock of 10 MHz, and a time period of 100 µs with single count of “1” in that time period, the network provides 10 bit resolution (1 count in 1000 possible counts or 1/1024). A considerable advantage to using this type of circuit is that the proportional output gives a practically real time reading of the gas composition. A dynamic range of ~30 dB (1 nA – 31 nA) is the desired input range with a target laser power of ~10 -30 mW. Radiation hardening and extreme temperature performance are of interest for future small satellite and space applications, but were not a major focus of this design.

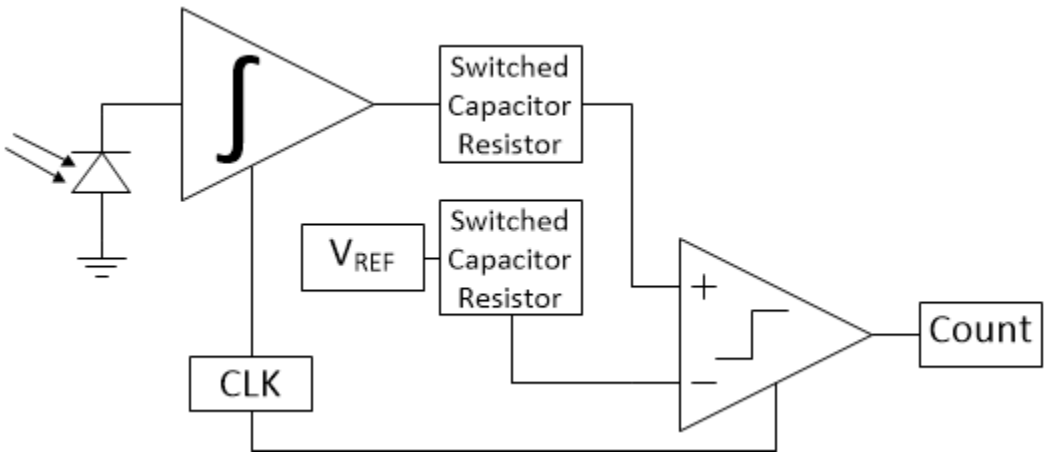


Figure 1.3 Proposed delta sigma modulator design.

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1.3 Thesis Overview

The remainder of this thesis is ordered as follows: Chapter 2 will discuss the theory and operation of ΔΣ modulators along with state of the art ΔΣ modulator designs. Chapter 3 will discuss the design of the individual blocks, any changes that were needed to those blocks during simulation, and the simulation results. Chapter 3 will also contain images of layout and overall size of the network. Chapter 4 will discuss the testing methods and the results of those lab tests. Chapter 5 will conclude the thesis and discuss plans for future work on this project.

Chapter 2

Literature Review

2.1 Delta-Sigma Modulation

Delta-sigma (ΔΣ) modulators are analog-to-digital converters (ADCs) known for their capability of producing high-resolution digital outputs while consuming low amounts of power and low silicon die area. These circuits employ techniques called oversampling and noise shaping to achieve their high signal-to-noise ratios (SNR). While both oversampling and noise shaping can greatly improve SNR, oversampling will largely limit the delta-sigma to low and medium speed cases [11].

The use of ΔΣ modulation is prevalently found in precision temperature measurement, high fidelity audio processing, CMOS imaging, and biomedical sensing applications [13]. The basic operation of a ΔΣ Modulator along with the techniques of oversampling and noise shaping will be discussed in more detail in the following sections.

2.1.1 Basics of Delta-Sigma Modulation

In the past, the ΔΣ modulator appeared to be too complex to fully understand, and therefore has been avoided. The elegance of the ΔΣ modulator is that while the mathematical theory is complicated, the operation and building blocks are quite simple. This allows a general discussion on how the ΔΣ modulator operates without getting lost in the difficult, hard to understand numerical analysis [11].

The basic building blocks of the ΔΣ modulator are an integrator, a comparator, a difference amplifier, a switch, and a voltage reference. There are digital components such as a DSP (digital signal processor) that acts as a low pass filter [11]. These basic blocks are shown in Figure 2.1 below. Other terms that apply to ΔΣ modulators are quantization, noise shaping, and decimation which will be discussed in the following sections.

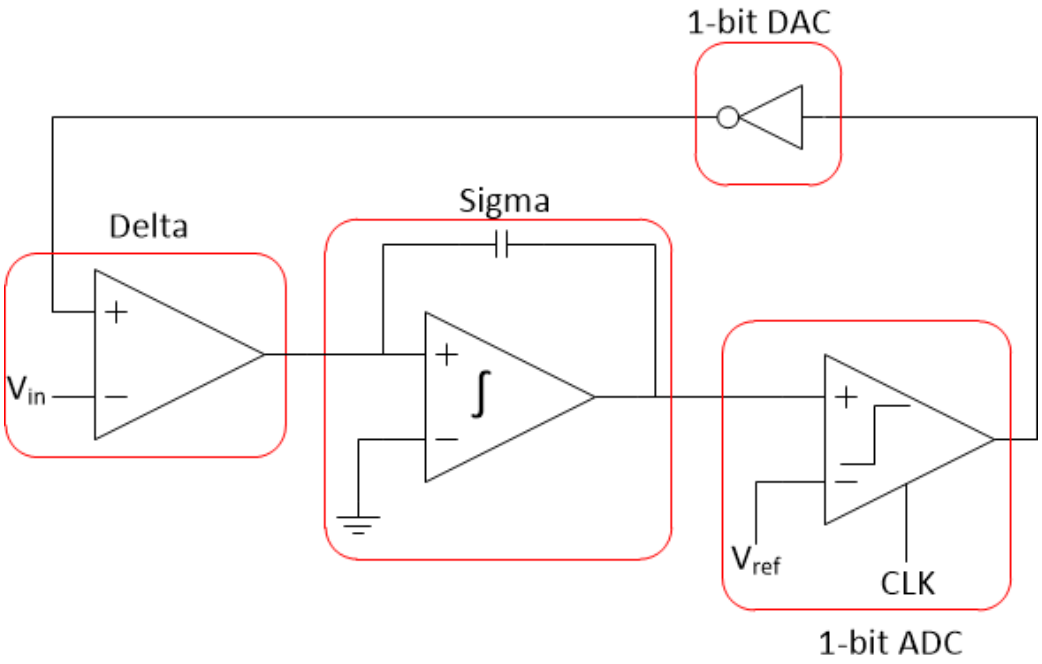


Figure 2.1 Diagram of single stage delta-sigma modulator [10].

The basic ΔΣ modulator can be considered as a 1-bit sampling system. With several samples of the input signal taken due to the oversampling, these samples can be collected and averaged over a specified time to obtain a digital output that represents the analog

input signal [12]. Although it is considered a 1-bit system, the oversampling and noise shaping will provide high SNR similar to that of multi-bit systems.

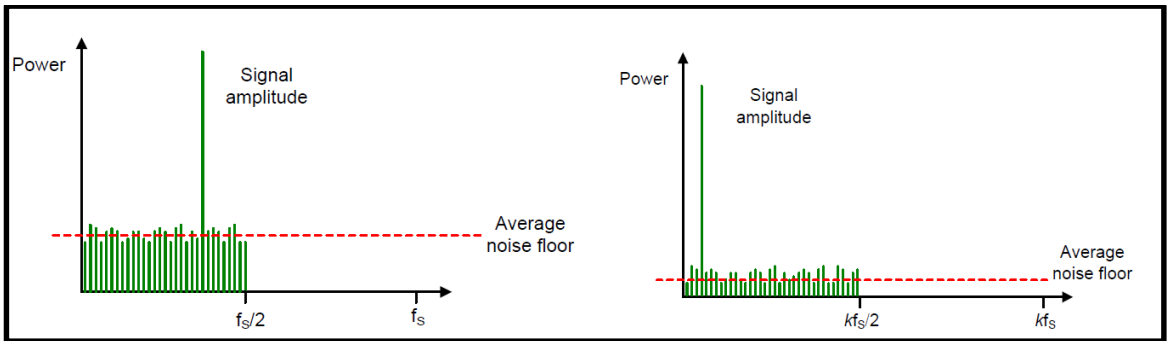
With analog signals and CMOS processes getting progressively smaller, the networks that process these signals must have good noise characteristics. With a small signal, the signal-to-noise ratio is reduced, leading to possible erroneous senses due to noise coupling onto the small input signal. This is the reason for the increased use of the ΔΣ modulator in sensitive or precise applications.

2.1.2 Oversampling

Oversampling, refers to a technique in which the input signal is sampled several times faster than the Nyquist rate of f_S. When this oversampling occurs, it effectively expands the noise energy over a larger frequency range. An example of the FFT of an input sine wave (a) and then the oversampled FFT of the same sine wave (b) are shown in Figure 2.2. The large tone is the frequency of the sine wave which is however surrounded by a large amount of random quantization noise. Quantization noise is the error introduced when a continuous time input signal with an infinite amount of states is digitized and converted into a discrete time signal with a finite amount of states based on the resolution of the converter. This noise causes the analog-to-digital conversion to lose data, introducing error and distortion. Not only is the noise itself random, but the magnitude is also random, ranging from ±LSB [13]. Given (2.1), it could be inferred that increasing the number of bits (N) will increase the SNR [13].

$$SNR = 6.02N + 1.76dB \tag{2.1}$$

However, with a ΔΣ modulator, the distribution of the noise from oversampling causes the noise floor to have a lower magnitude while the magnitude of the signal is the same. This lowers the RMS noise, allowing better detection and processing of the desired signal [11]. This property will effectively increase the SNR without having to increase the number of bits.



(a) (b)

Figure 2.2 (a) Typical FFT of sine wave input. (b) FFT of oversampled sine wave, with oversampling ratio *k* [10].

2.1.3 Noise Shaping

Through the use of feedback from the digital-to-analog (DAC) converter, the quantized output from the integrator is kept close to the comparator reference voltage. When the output of the comparator switches from low to high or high to low, the linear DAC then responds by changing the input reference voltage of the difference (delta) amplifier which is then applied to the integrator. The feedback forces the average output

to be equal to the input over the specified integration period of N clock cycles. Referring back to Figure 2.1, it displays the system that is described above while Figure 2.3 illustrates the noise shaping being discussed. By "summing" the error voltage applied to the integrator, the signal gets low-pass filtered, while the noise is high-pass filtered, essentially pushing the quantization noise into much higher frequencies, thus effectively increasing the signal to noise ratio [10, 13]. To improve this noise shaping, multi-order delta-sigma modulators are created using multiple integration and summing stages [16, 17].

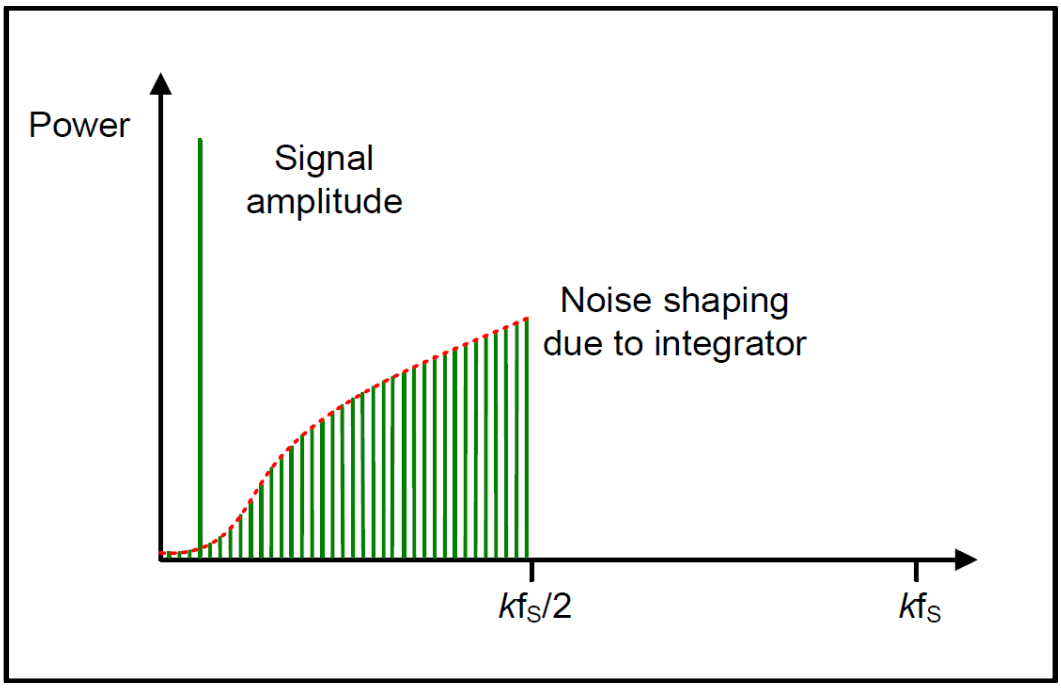


Figure 2.3 Output spectrum with noise being pushed away from signal due to integrator [10].

2.1.4 Multi-Order System

With one stage, the ΔΣ modulator performs extremely well. However, some applications need even better performance. One way is to cascade the integration and the summing stages together to improve the SNR [11]. Looking at Figure 2.4, it shows how the performance of a one stage versus a two stage ΔΣ modulator performs. As Figure 2.4 shows, the 2nd order ΔΣ modulator pushes the quantization noise out further than the 1st order ΔΣ modulator.

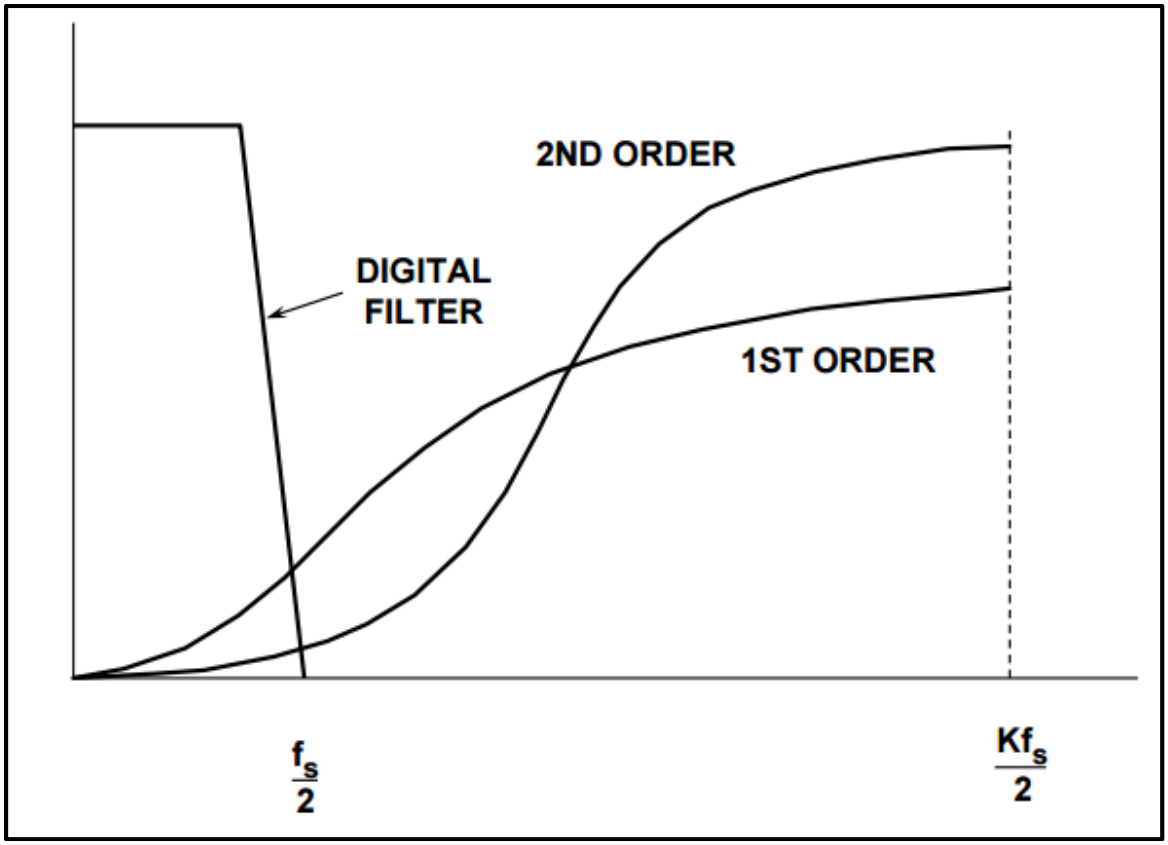


Figure 2.4 Comparison of 1st order and 2nd order ΔΣ modulator [11].

This will effectively increase the SNR. With each doubling of the oversampling ratio and an increase in the order of the converter, the SNR will increase. This increase is shown in (2.2) where L is the number of stages such as 1, 2, 3, etc.

$$3(2L+1)dB \tag{2.2}$$

A 15 dB increase in SNR occurs when a 2nd order modulator is used. This increase is shown graphically in Figure 2.5.

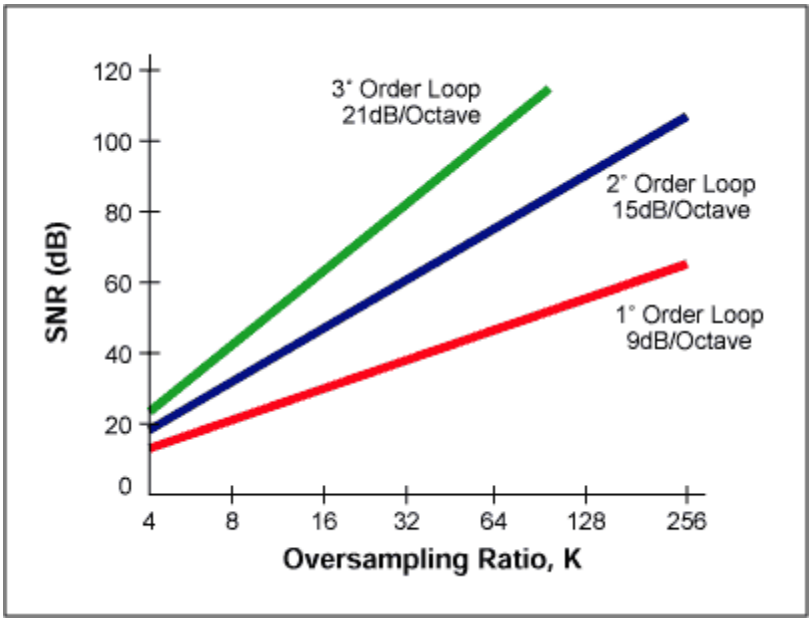


Figure 2.5 Increase in SNR due to doubling of oversampling ratio (k) [13].

2.2 Current State of Technology

Delta-sigma modulators have been used in a variety of applications and conditions over the course of their history. However, they are traditionally used in applications where high resolution was needed but on low frequency signals. With the increase in high frequency applications in the industrial and the consumer markets, delta-sigma modulators are now being put into moderate to high frequency applications, albeit with less resolution than the low frequency designs. The following sections will explore some of the new areas of research for delta-sigma modulator applications and their improvement in dynamic range and bandwidth [10].

2.2.1 Multi-Bit Quantizers

As discussed previously, delta-sigma modulators can have increased performance when the order is increased. This increase in order does create problems, such as increased quantization noise in the signal band and possible instability [16]. An area of research aimed at increasing the dynamic range without adding the complexity of multi-order systems is the multi-bit quantizer. In the traditional delta-sigma modulator, the output is 1-bit that is averaged. The multi-bit quantizer outputs a multi-bit data stream instead of a 1-bit data stream. This increase in resolution will reduce the signal-band quantization noise (in the range of 6 dB) and improve the stability of the higher order loop filters [10, 16]. Multi-bit quantization is a substitute for the oversampling and the noise shaping previously found in the classic ΔΣ modulator topologies. With the smaller oversampling ratio, the multi-bit design can be used in wider band applications. This also reduces power consumption. One of the shortcomings of multi-bit quantizers is an

increase in non-linearity which is due to mismatches in the DAC [16, 17]. The multi-bit design requires the DAC to have the same order of linearity as the overall converter. To achieve this, a technique called dynamic element matching is used, but this technique requires large power and large die area to be implemented [16]. Although this may require higher power, some studies have shown that using a multi-bit quantizer of up to 4 bits is more power efficient than increasing the order of the modulator since an increase in the order means to add another integrator into the loop [23].

2.2.2 VCO-Based Quantizer

With CMOS technology scaling down in feature size, circuit designers are trying to increase the digital portions of sensing circuits. One of the newest ideas for ΔΣ modulators is the voltage controlled oscillator (VCO) based designs. These new designs are largely digital circuitry with an intrinsic noise shaping quality coupled with anti-distortion properties [24]. While the VCO can have some non-linear behavior, this is reduced by placing it in the analog feedback path. The VCO also provides an additional order of noise shaping, similar to additional order delta-sigma modulators providing higher order noise shaping at the output [18]. With the VCO performing as a multi-bit quantizer, it is the limiting block in terms of performance of this topology. Along with a very linear VCO being needed, a linear DAC is also necessary for proper performance of this design, similar to the multi-bit quantizer [10].

Chapter 3

Design and Simulation

3.1 Photodiode Basics

A photodiode is a device that has a PN junction or a PIN structure that is in reverse bias. The reverse bias prevents current from flowing, except for a small dark current, and also increases the depletion region making it more sensitive to light input. These attributes are why the PIN structure was used for this application. The PIN structure consists of a highly doped p^+ region and a highly doped n^+ region with an intrinsic region (un-doped) between the p^+ and n^+ regions. When a photon with high enough energy to exceed the bandgap of the semiconductor material is incident on the photodiode, it creates an electron/hole pair. The hole goes towards the anode and the electron goes to the cathode. This creates drift, which in turn creates the desired photo current. The ideal operation of this device is that one photon produces one electron, but this is not seen in real applications.

For this design, the photodiode of choice is the Hamamatsu 6854-01. The dark current associated with this photodiode is typically 400 pA and having a shunt capacitance of 1-1.5 pf. The data sheet shows that the capacitance stays within this range, regardless of the reverse voltage. The responsivity, R_e, is measured in A/W, or amperes per watt of incident radiant power. For this device, the responsivity at the desired wavelength (λ=1.55 μm) is .95 A/W. This stands to reason, that a 1 nW powered laser

will produce 1 nA of photocurrent, suitable for this proof of concept design. Figures 3.1 and 3.2 show the basic structure of a PIN photodiode and the model used for simulation.

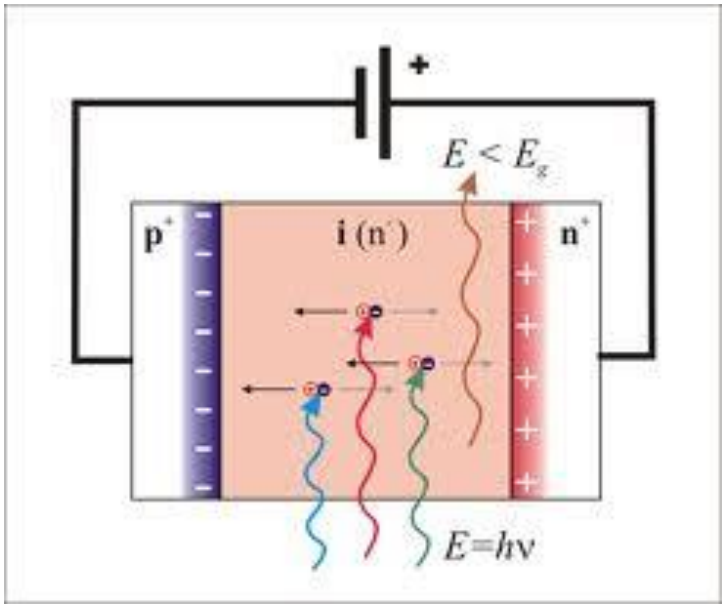


Figure 3.1 Basic structure and operation of PIN photodiode [21].

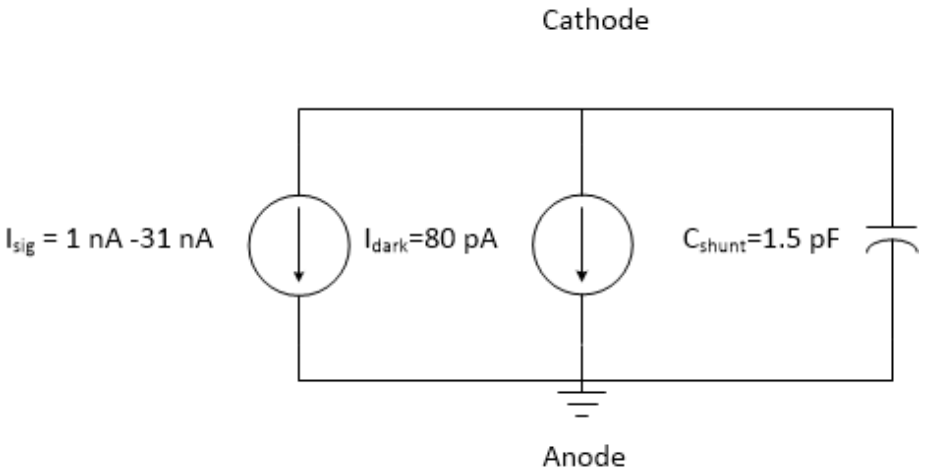


Figure 3.2 Model used in simulation for photodiode.

3.2 Start-Up Circuitry

The first block in the proposed network is the start-up circuitry. Start-up circuitry is necessary in self-biased circuits. When the circuit is turned on, there are two conditions that can arise. One of these conditions is that the circuit will bias up correctly without any other considerations needed. The other condition is when the biasing does not set up properly, thus no current flows and the circuit fails to operate. This latter condition must be avoided, and therefore makes start-up circuitry necessary. The design of the start-up circuitry will be covered in the following section.

3.2.1 Start-up Design

The first part of this system is composed of the start-up biasing along with a beta multiplier. Originally, minimum length devices were used, but their size was altered in order to avoid negative effects of channel length modulation. Channel length modulation arises when the device operates in the saturation region. A condition called pinch off occurs when the drain voltage gets larger and larger. This pinch-off shortens the inverted channel, and therefore causes the output resistance to consequently decrease. Along with decreasing output resistance, the current increases, causing mismatching in current mirror and amplifier design. For these reasons, minimum channel length devices were avoided in the sensitive blocks of the overall network. While some blocks did not used minimum size devices, digital blocks did use minimum size devices due to their robustness with respect to sizing effects.

The operation of this circuit begins when V_{DD} is supplied at time t_0. At t_0, MSU 3 is off, while MSU 1 and MSU 2 are on, forming a voltage divider. As the drain voltage

on MSU 1 increases, this increases the gate voltage of MSU 3, turning it on. This then allows M1 to begin turning on as the drain/gate voltage increases. Once the source voltage exceeds the gate voltage, MSU 2 and MSU 3 turn off. This will prevent an unwanted state. MSU 1 and MSU 2 were designed with large channel lengths to increase the resistance so that DC leakage current would be avoided. Figure 3.1 shows the startup circuit. In Figure 3.1, M3 and M4 are identically sized p-type devices to form a current mirror with a ratio of 1:1. To calculate the appropriate size for M2, start by using Kirchoff's Voltage Law around M2 and M1.

$$V_{GS1} = V_{GS2} + (I_{ref} \cdot R_1) \tag{3.1}$$

Solving the drain current equation for V_{GS} when a MOSFET is in saturation gives the following equation,

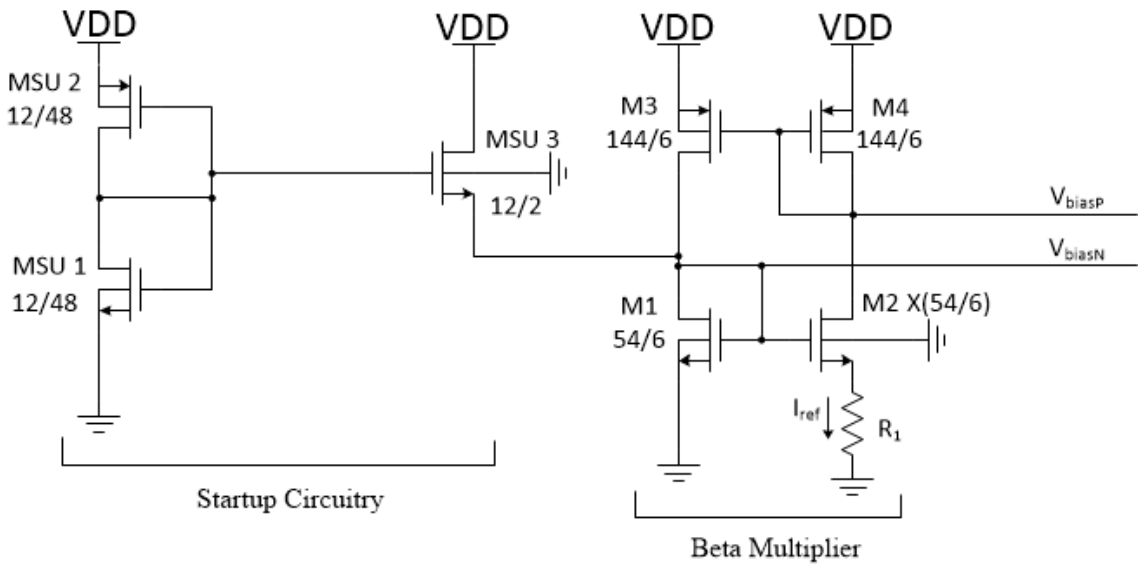


Figure 3.1. Start-up biasing and beta multiplier circuitry. All W/L ratios are multiplied by a factor of 300E-9 [15].

$$V_{GS} = \sqrt{\frac{2I_D \cdot L}{\mu_n \cdot C_{ox}{}' \cdot W}} + V_{th} \tag{3.2}$$

Substituting this into (3.1) gives,

$$\sqrt{\frac{2I_D \cdot L}{\mu_n \cdot C_{ox}{}' \cdot W}} + V_{th} = \sqrt{\frac{2I_D \cdot L}{\mu_n \cdot C_{ox}{}' \cdot XW}} + V_{th} + (I_{ref} \cdot R_1) \tag{3.3}$$

Isolating I_{ref} gives,

$$I_{ref} = \sqrt{2I_D \mu_n C_{ox}{}' \frac{W}{L}} \left[\sqrt{\frac{2I_D \cdot L}{\mu_n \cdot C_{ox}{}' \cdot W}} - \sqrt{\frac{2I_D \cdot L}{\mu_n \cdot C_{ox}{}' \cdot XW}} \right] \tag{3.4}$$

An assumption for *X* needs to be made in (3.4). The assumption is that *X* is a perfect square multiplier (4, 9, 16, etc.) of the W/L ratio to obtain proper current matching. The transconductance, g_m is equal to $1/R_1$ as shown in (3.5). When setting $g_m = 1/R_1$, this is also called a constant-g_m design.

$$g_m = \frac{1}{R_1} = \sqrt{2I_D \mu_n C_{ox}{}' \frac{W}{L}} \tag{3.5}$$

Solving (3.4) leads to the following equation, and given that I_{ref} is chosen to be 3μA, the value of the multiplying factor, *X*, can then be found.

$$I_D = \frac{2I_D}{1} - \frac{2I_D}{X} \tag{3.6}$$

In order to comply with (3.6), *X* must be 4. This implies that the W/L ratio for the M2 transistor must be 4 times larger than the M1 transistor's W/L ratio in order to supply the required 3 μA. The increase in the width of the M2 transistor also ensures that $V_{GS1} > V_{GS2}$. This has the effect of using less gate to source voltage to conduct I_{ref}, therefore satisfying the condition $V_{GS1} > V_{GS2}$. This design is called the β multiplier, where,

$$\beta = \frac{\mu_n C_{ox}{}' W}{2} \frac{W}{L} \tag{3.7}$$

The resistor value R_1 needs to be found using (3.8) whereas before I_{ref} is 3 µA, W/L is 9, $\mu_n C_{ox}'/2$ is a given process parameter of 57.8 µA/V^2, and X is the multiplying factor of 4.

$$I_{ref} = \frac{2}{R_1^2 \cdot \frac{\mu_n C_{ox}{}' W}{2} \frac{W}{L}} \left(1 - \frac{1}{\sqrt{X}}\right)^2 \tag{3.8}$$

The value of the tail resistor R_1 is found to be approximately roughly 18 kΩ. A resistance of 5 kΩ was used for ease of scalability, then put in series to be approximately 20 kΩ.

3.2.2 Start-Up Simulation

In order to verify that the bias current was being generated in the start-up circuitry, a simulation was performed and the DC operating points of the network was observed. Figure 3.2 shows the bias current in the branch with the 20 kΩ resistance. This simulation confirms that the start-up circuitry is performing as expected.

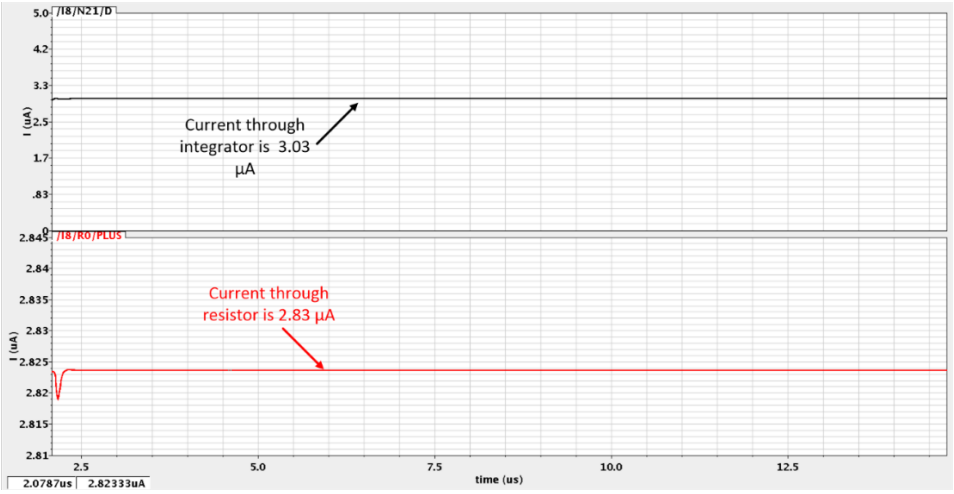


Figure 3.2 Current in the bias network. The network was designed for 3 µA, and simulation suggested it produced ~2.83 µA in the β multiplier.

3.3 Integrator

The next block in the system was the integrator. This integrator will be the interface between the photodiode input and the delta-sigma modulator. The integrator will take an input charge and output a voltage based on a set integration time. With a photodiode responsivity of ~1, and the target laser signal of 1 nW, the minimum signal current would therefore be ~1 nA. Since the minimum signal is small, the amplifier design will need to have sufficient gain in order to properly process the signal in the next stages. The proposed circuit in the following section will provide sufficient gain, as well as plenty of bandwidth and stable operation.

3.3.1 Integrator Design

The proposed design is the dual cascode with an active load topology. This design will provide the necessary high gain due to increasing the load resistance with the cascoded MOS devices. Along with increasing the load resistance for gain, the cascoding scheme will reduce the Miller capacitance effect which will further increase the bandwidth of the amplifier. The schematic of the dual cascode design is shown in Figure 3.3. In order to find the gain of the amplifier, the output impedance needs to be calculated first. This is most easily done when drawing the small signal model, as shown in Figure 3.4. The resistance looking into the drain of M2 is shown in (3.9)

$$r_{in2} = g_{m2} r_{ds2} r_{ds1} \tag{3.9}$$

Similarly, solving for the resistance looking into M3, one can find,

$$r_{in3} = g_{m3} r_{ds3} r_{ds4} \tag{3.10}$$

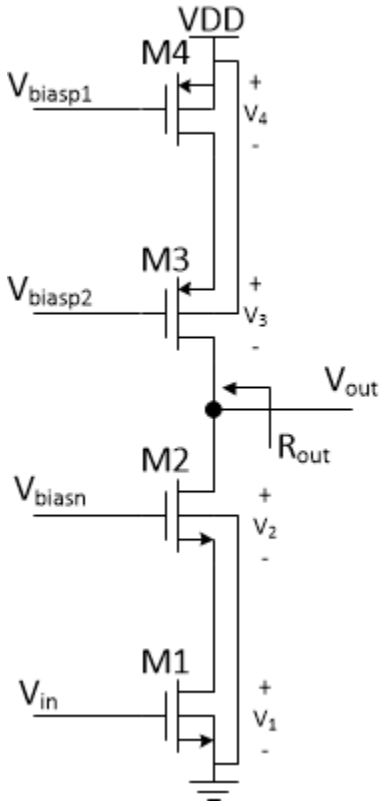


Figure 3.3 Cascode amplifier with active load.

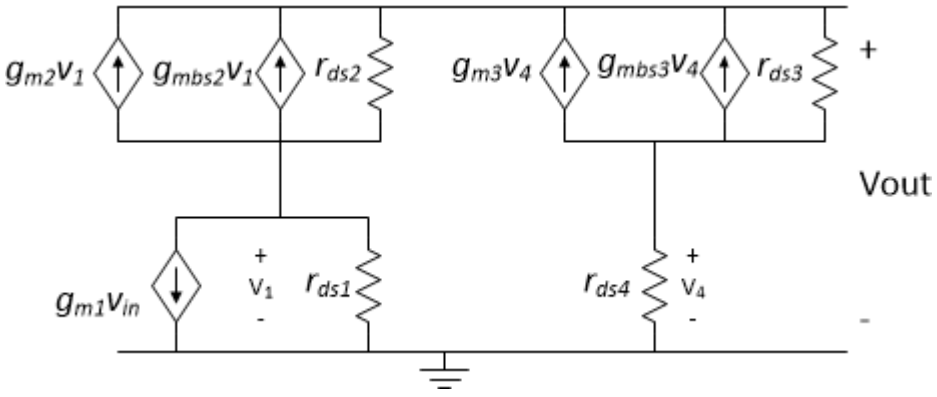


Figure 3.4 Small signal model of the cascode active load amplifier.

In order to solve (3.9) and (3.10), the expressions for g_m must be defined.

$$g_{mn} = \sqrt{2I_D \frac{\mu_n C_{ox}'}{2} \left(W/L\right)_n} \tag{3.11}$$

$$g_{mp} = \sqrt{2I_D \frac{\mu_p C_{ox}'}{2} \left(W/L\right)_p} \tag{3.12}$$

Given that $\mu_n C_{ox}$' is approximately ~3 times that of $\mu_p C_{ox}$', the $(W/L)_p$ must also be ~3 times the $(W/L)_n$ in order to maintain proper transconductance matching. Once the devices are properly sized and g_m is calculated, the resistance of the channel, r_{ds}, needs to be obtained. For simple approximations, (3.13) is used to calculate r_{ds}. As discussed in the previous section, channel length modulation effects the channel resistance, and is represented in (3.13) as λ. From the process parameters, λ is ~.35 and I_D is 3 µA.

$$r_{ds} = \frac{1}{\lambda I_D} = \frac{1}{(.35)(3\ \mu A)} = 952\ k\Omega \tag{3.13}$$

Solving (3.11) and (3.12) with a $(W/L)_n$ of 3 and a $(W/L)_p$ of 9, the transcoductances are 32.25 µA/V and 31.95 µA/V respectively. The output resistance can now be solved by the following equation,

$$r_{out} \cong r_{in2} || r_{in3} = 14.36\ M\Omega \tag{3.14}$$

Since the gain is defined as the negative transconductance of the common source amplifying stage times the output resistance, the voltage gain is therefore,

$$A_v = -g_{m1} r_{out} = -926 \tag{3.15}$$

where g_{m1} is 64.5 µS due to a (W/L) ratio of 12. This result matches with the expression (3.16) for the predicted maximum gain.

$$\frac{g_{m1}}{g_{out}} = \frac{64.5 \cdot 10^{-6}}{69.64 \cdot 10^{-9}} = 926 \tag{3.16}$$

After finding that this design will provide sufficient gain, the feedback capacitor needs to be sized correctly so that the integration of the input signal does not saturate before the integration time is reset. To find the capacitor value that is needed, the voltage change on the output needs to be established. The lowest voltage that is to be used on the output is 800 mV. This is very close to the threshold voltage of ~700 mV. Any lower than the 800 mV limit and the performance of the delta-sigma modulator will be affected due to transistors operating close to cut off (cut off is V_{gs}-V_{th} = *0*). For easy design considerations, the maximum voltage that is wanted is 3 V on the output. Equation (3.17) shows how the capacitor was sized,

$$C = dt\frac{I}{dV} \tag{3.17}$$

The integration time, *dt*, is 12.8 µsec corresponding to a 7 bit resolution. The change in voltage is found from the difference between the maximum output and the minimum output voltages. With a goal of 30 dB for the input dynamic range and the smallest signal being 1 nA, the upper limit current is therefore 31 nA, or *I* in (3.17). The capacitance is needed to meet these specifications is ~180 fF. A capacitance of 200 fF was implemented due to ease of design and layout. A reset switch is placed in parallel with the feedback capacitor in order to reset the integration time for another sample to be taken. The final schematic is shown in Figure 3.5.

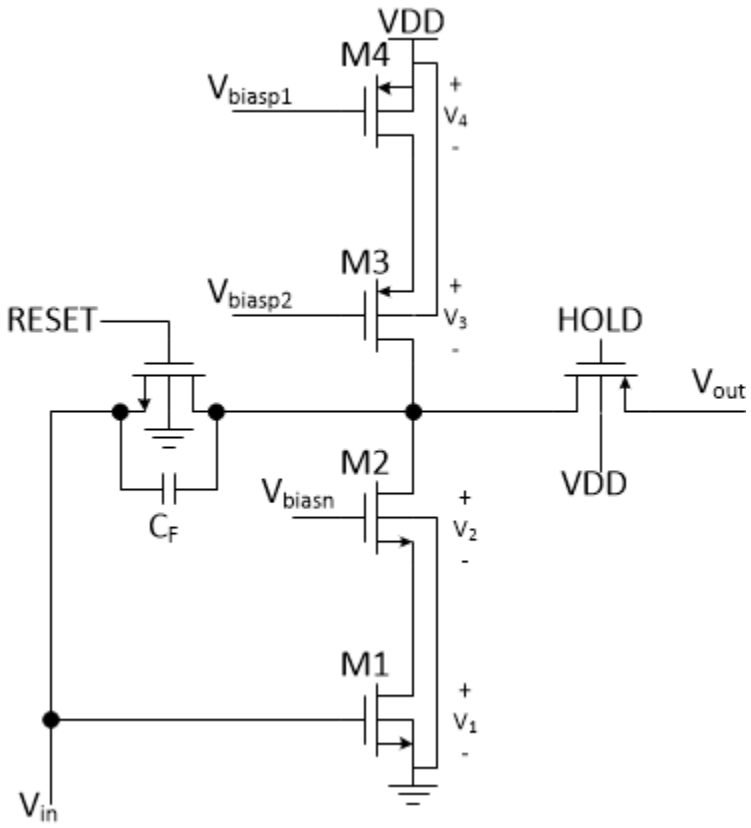


Figure 3.5 Full integrator schematic with RESET and HOLD.

3.3.2 Integrator Simulation

This section will discuss pre- and post-layout simulations along with any problems that were discovered and addressed.

Once the design had been settled on for the integrator and the start-up/biasing network, the schematic was then constructed and simulated. The first initial simulation showed that the desired dynamic range of 30 dB on the input can be achieved. In fact, a dynamic range of 31.16 dB (1 nA- 31 nA) seems to be realizable. However, this design exhibited what appeared to be charge injection problems with the sample-and-hold

transistor. This is shown in Figure 3.6. With charge injection, some of the charge is dumped out of the transistor and causing the output voltage to jump, in some cases significantly. The ΔV_i (change in signal voltage from integrator) was measured at the edge of the hold signal going high. The difference was the largest when the input signal was 31 nA and the smallest at 1 nA, corresponding to a ΔV_i of 40 mV and 16 mV, respectively. This difference was too large, as the DSM would be able to sense this difference, and would lead to improper correlation with the output when using an off chip reference voltage. In order to rectify this problem, a dummy switch was added in series with the output of the sample and hold device. The use of the dummy switch is a commonly used technique in sample and hold circuits, especially when poor switches are used. The concept is to use a switch in series with the drain and the source connected together, and a perfectly overlapping complementary signal to the signal of the original switch. When the original switch turns off, half of the channel charge is injected to the dummy switch. Since only half of the charge from the hold transistor is sent to the dummy switch, the dummy needs to only be ½ the size of the hold switch. The charge injected by the hold transistor is the same as the charge induced by the dummy switch. When the dummy transistor switches off, it injects half of its charge in both directions [15]. Starting with half the size of the original switch, simulations can be done to determine the most effective sizing combination. Once the dummy switch had been implemented, the problem of driving the sample and hold switch and the dummy switch arose. For proper operation of the dummy switch, an overlapping square wave

complimentary signal needs to be generated. In an effort to avoid putting multiple signals off chip, a pseudodifferential CMOS differential switch driver was implemented [20].

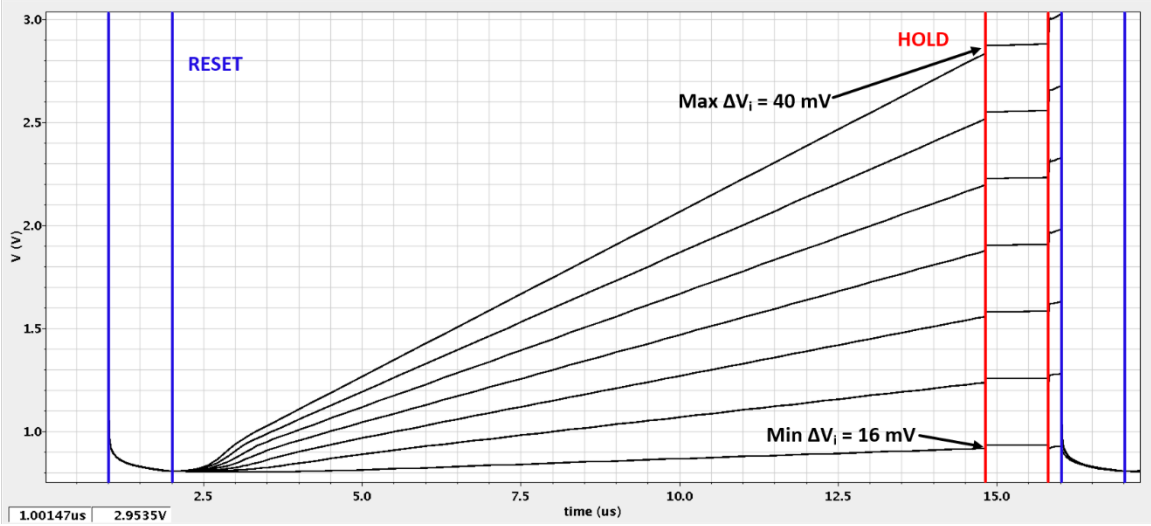


Figure 3.6 Charge injection on hold transistor output.

This switch driver schematic is shown in Figure 3.7. Using the hold signal as the input to this pseudodifferential switch, this will create the desired hold signal as well as a complimented signal to switch the dummy switch correctly. The output of this switch driver is shown in Figure 3.8. After implementing the dummy switch and differential switch driver, a pre-layout simulation was performed, and is shown in Figure 3.9. As the figure shows, the charge injection has almost been completely eliminated for all simulated inputs while maintaining the same input dynamic range.

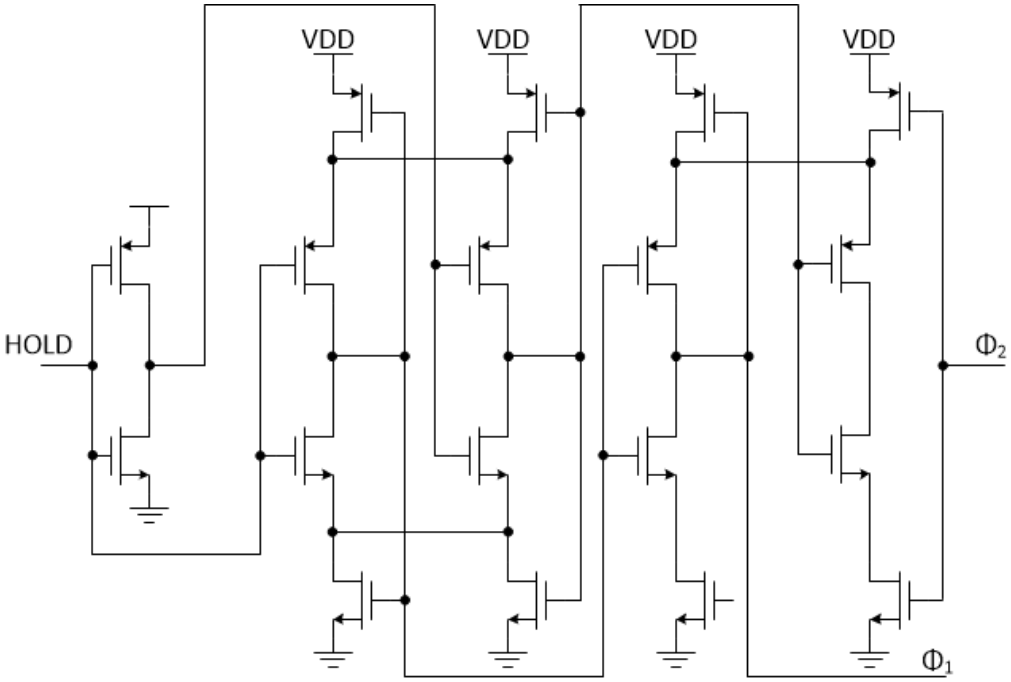


Figure 3.7 Schematic of pseudodifferential CMOS switch driver [20].

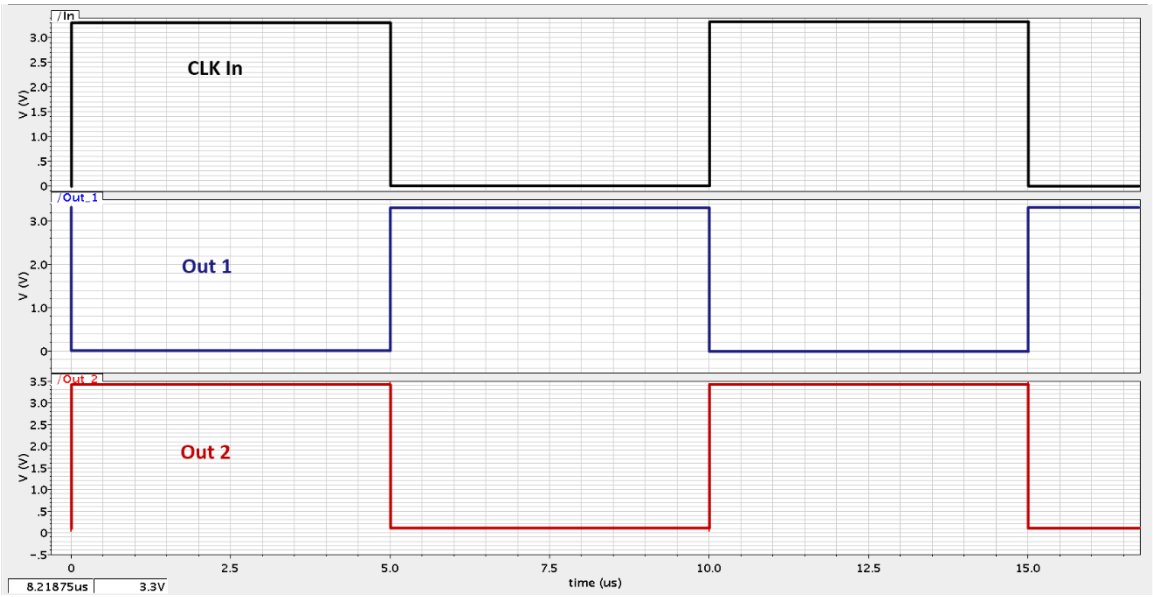


Figure 3.8 Simulation of Pseudodifferential CMOS Switch Driver with HOLD signal as input.

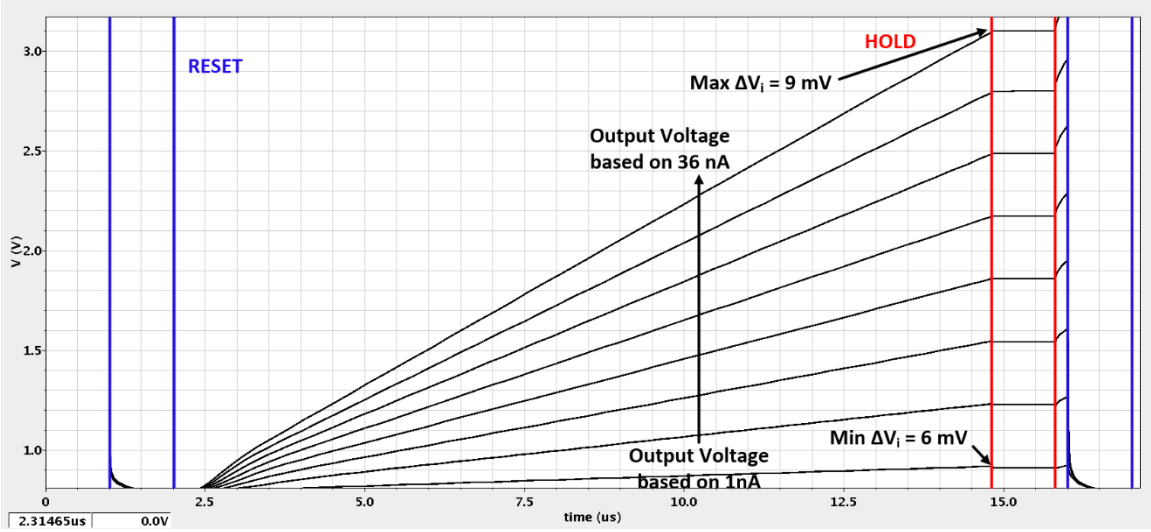


Figure 3.9 Pre-layout integrator simulation with dummy switch.

After completing the simulations for pre-layout, layout of this topology was done. The layout along with dimensions are shown in Figure 3.10. The switches were surrounded by guard rings in the layout to provide insulation against noise coupling and for better switch performance. The current mirroring part of the circuit was laid out using the common centroid technique. This improves matching between devices, so that current is the same in both branches. Each PMOS and NMOS network were also put into guard rings to improve performance due to the drawbacks of the single-well process being used and the sensitivity of the inputs. This technique of using the guard rings also protects against possible noise coupling and interference. A post-layout simulation was done to assess the effects of trace length resistance and capacitance. This is shown in Figure 3.11.

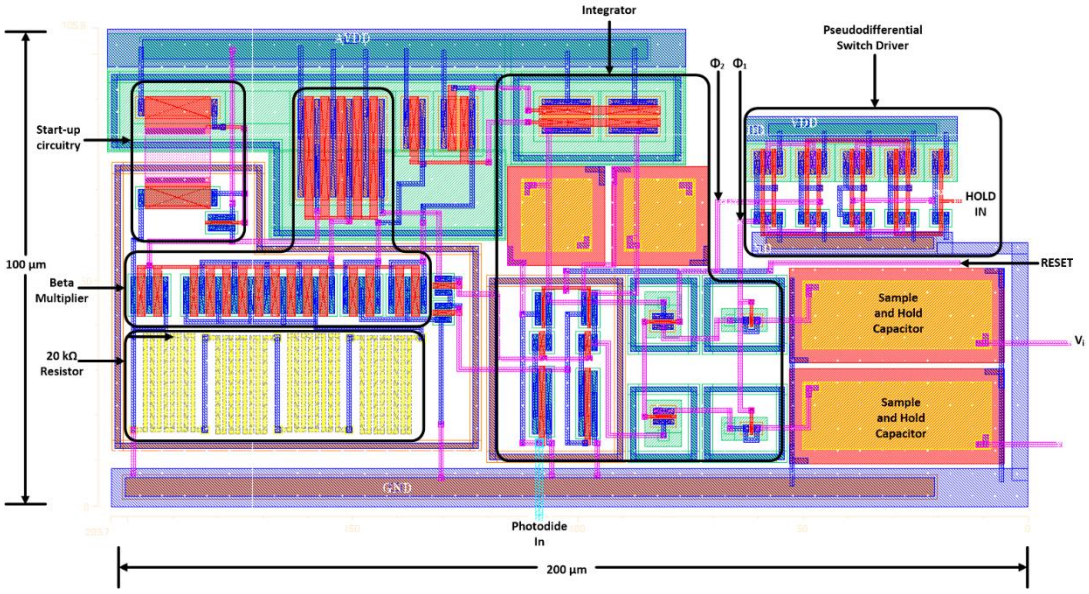


Figure 3.10 Layout of integrator. Dimensions are 200 µm x 100 µm.

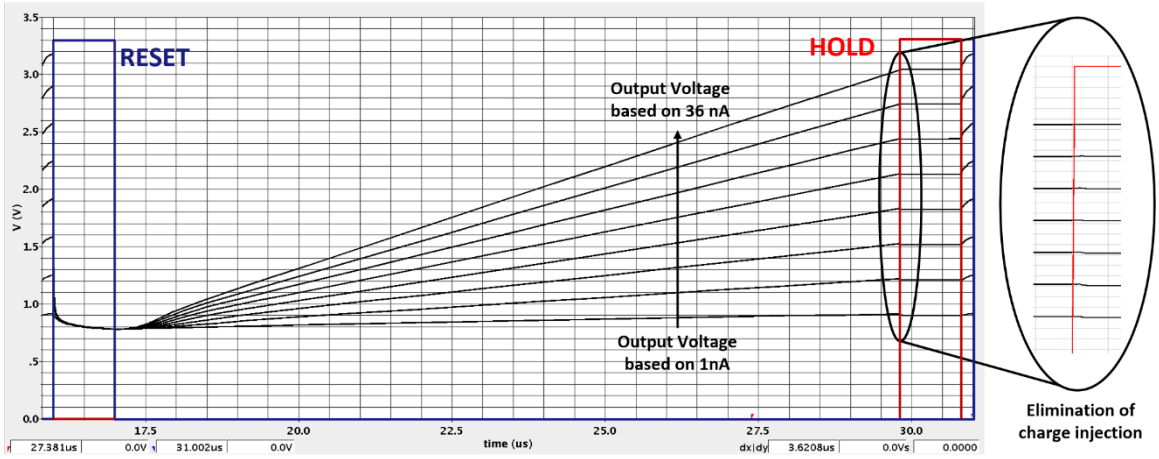


Figure 3.11 Post-layout integrator simulation.

3.4 Delta-Sigma Modulator

This part of the network is where the differencing (delta, Δ) and the summing (sigma, Σ) takes place, which was previously shown in Figure 2.1. The circuit takes the output from the integrator and compares it to the off chip reference voltage. It converts the input voltages into a current, via a linear voltage-to-current circuit. The circuit then makes a comparison between the signal input and the reference input, and gives a count when the signal input is greater than the reference.

3.4.1 Delta-Sigma Design

In order to begin sensing the input from the integrator, a circuit that will convert the integrator output signal voltage and the reference voltage to a usable current is necessary. In order to compare the reference and the output signal from the integrator, the difference of their converted currents will have to be taken. The current mirror used to detect the difference in these currents is shown in Figure 3.12. The difference in the currents I_{SIG} and I_{REF} is summed in the output capacitor (C_{Bucket}), referencing the sigma portion of the circuit. This difference is then averaged out over time to converge to a constant value when the feedback of the comparator is added. The circuit converges at the point shown in (3.18) [13].

$$I_{REF} = I_{SIG} = \frac{V_{REF,shift}}{R_{REF}} = \frac{V_{SIG,shift}}{R_{SIG}} \tag{3.18}$$

Where $V_{REF,shift}$ and $V_{SIG,shift}$ are

$$V_{REF,shift} = VDD - V_{THP} - V_{REF} \tag{3.19}$$

$$V_{SIG,shift} = VDD - V_{THP} - V_{SIG} \tag{3.20}$$

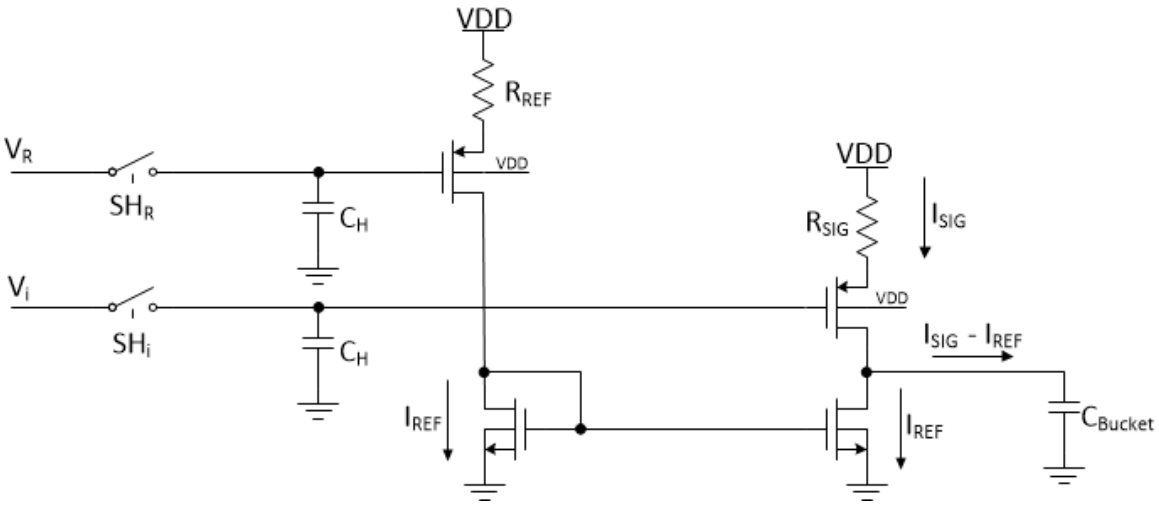


Figure 3.12 Linear voltage-to-current, current subtracting circuit. V_i is the signal voltage input and V_r is the reference voltage [15].

Using 3.18, it can be determined that the ratio of resistances, R_{SIG}/R_{REF}, gives the necessary information in order to determine the light intensity on the photodiode. In order to implement the resistors, a switched-capacitor resistor topology is used. This technique will not only save valuable die space, but also will provide more accurate sensing [15]. This switched capacitor resistor is shown in Figure 3.13. This circuit is built to be as symmetrical as possible. If it is built symmetrical, ideally any power supply noise, ground noise, or any coupling effects each branch in the same way, negating these effects. Sizing of the capacitors is not a critical design step, but it is also not trivial. The only rule that needs to be followed is that the C_{Cup} capacitor must be a third to a half the bucket capacitor size. This ensures that the bucket capacitor will never be overcharged, since the charge from the cup capacitor can only be discharged into the bucket capacitor once every clock cycle [15].

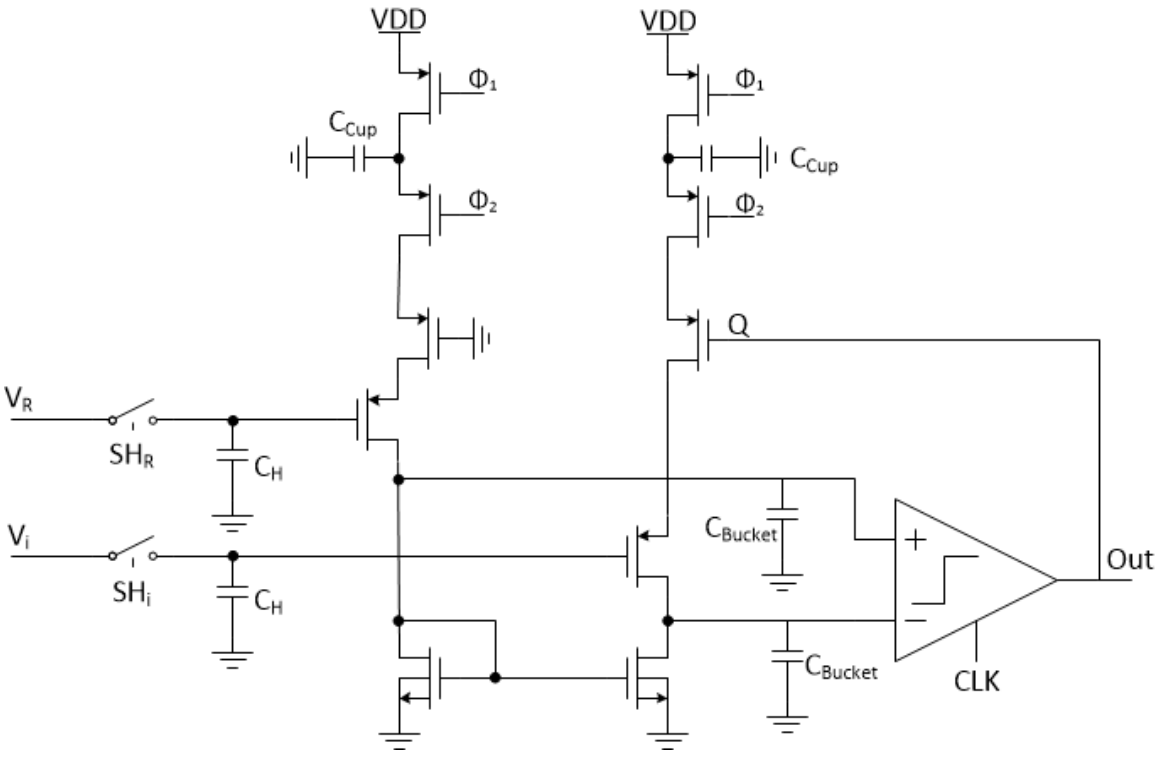


Figure 3.13 Switched capacitor resistor implementation [15].

The two upper PMOS transistors are controlled from an on chip non-overlapping clock. This allows the charge to be stored in C_{Cup}, and then subsequently that charge is directed into C_{Bucket}.

In the topology of Figure 3.13, the number of output counts is not linearly related to the input signal voltage. The feedback signal needs to be a function of the reference voltage, otherwise the counts will be non-linear and this sensing network is unreliable. A suitable topology is shown in Figure 3.14. Once again, the two bucket capacitors appear across both inputs to the comparator. This is done in order to ensure that any noise that

effects one input will have the same or similar effects to the other input, therefore canceling those effects.

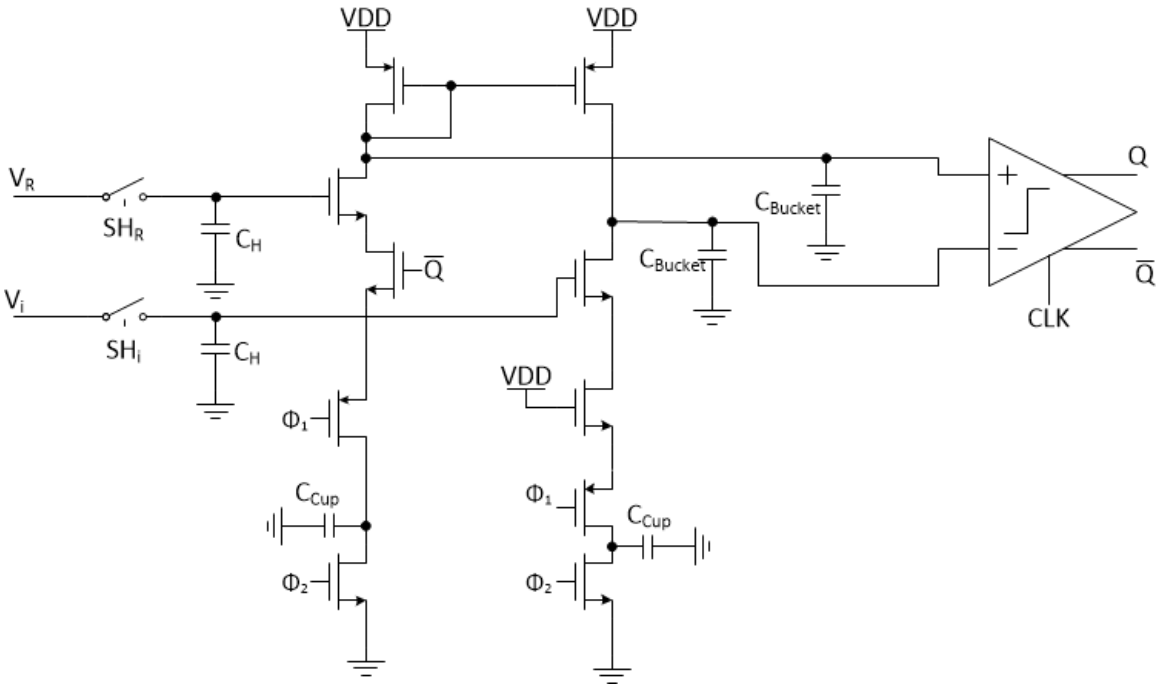


Figure 3.14 NMOS switched capacitor [15].

One thing to note is that if this bucket capacitor is too large, instability will occur due to the large capacitance in the feedback path [15].

3.5 Comparator

The comparator for this delta-sigma modulator needs to be able to quickly decide whether the signal input is larger than the reference signal and give the corresponding output. It needs to be able to sense small voltage changes and compare them. Kickback noise is reduced due to the design isolating the input devices from latching.

3.5.1 Comparator Design

The topology in Figure 3.15 shows a scheme that can accomplish the above mentioned goals. When Φ_2 is driven high, the outputs of the comparator are shorted to ground and are zero. On the falling edge of Φ_2, the comparator will then choose which of the bucket capacitors has the higher voltage. If the reference voltage capacitor is higher, then the count output will be a 1, and vice versa if the signal voltage is higher. This is shown in Figure 3.16. There is an SR latch on the output of the comparator. While it is not necessary, it helps prevent errors in the output of the comparator [15]. The latch also allows the output to swing faster. As the figure shows, when the signal is higher than the reference, Q_{not} goes high while Q goes low on the falling edge of Φ_2. Q_{not} is then fed back to the switched capacitor resistors in order to allow the bucket capacitor to be filled back up. Once the simulations were completed, the delta-sigma modulator was then put into layout. Once again, all devices were surrounded by guard rings to help prevent coupling of different signals or noise. The layout is shown in Figure 3.17. The majority of this layout was done using the common centroid technique in order to minimize mismatch.

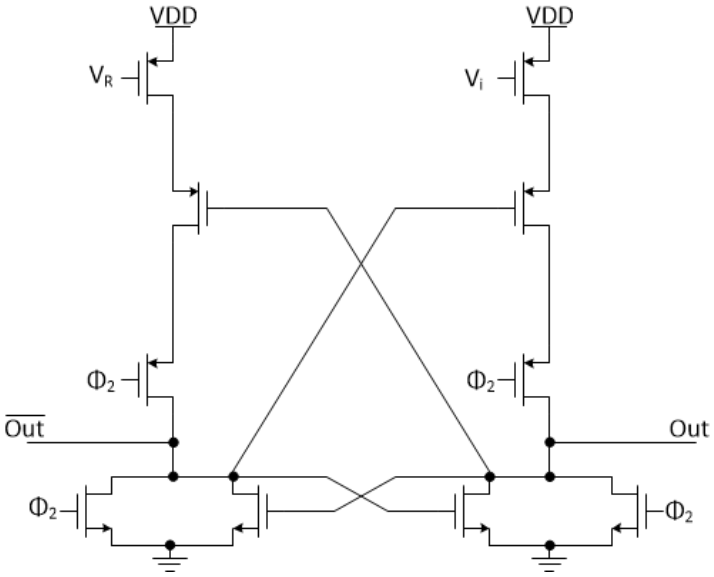


Figure 3.15 Comparator design to reduce noise effects while providing quick sensing [15].

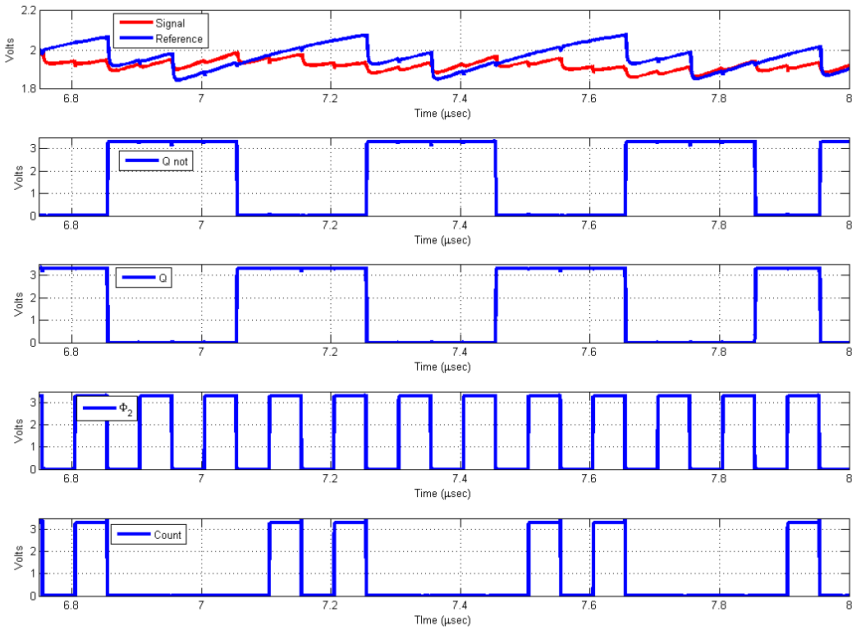


Figure 3.16 Simulation of comparator displaying the selection behavior between the reference and signal voltage.

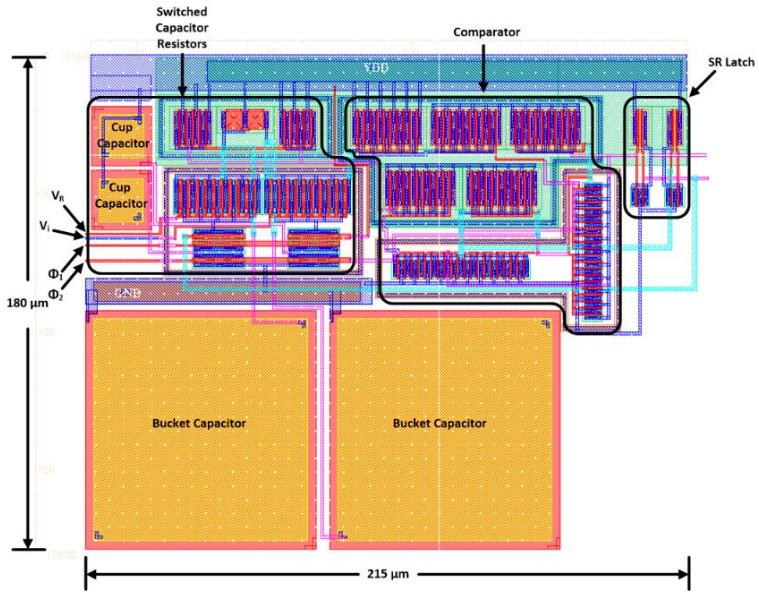


Figure 3.17 Delta-sigma modulator layout. Dimensions are 215 µm x 180 µm.

3.6 Delta-Sigma Modulator Simulation

Post-layout simulations were then run to ensure that the circuit was still operating according to the pre-layout simulations. The results are shown in Figure 3.18 and Figure 3.19 shows the linearity using the integrator and on chip oscillator. These simulations show that the circuit has suitable linearity, however the simulation using the the on chip integrator performed worse. One of the reasons for the lower linearity is that the lower range of signals, ~.8 V, is close to the threshold voltage of the devices, thus causing possible non-linearities with the devices operating near the cut-off region.

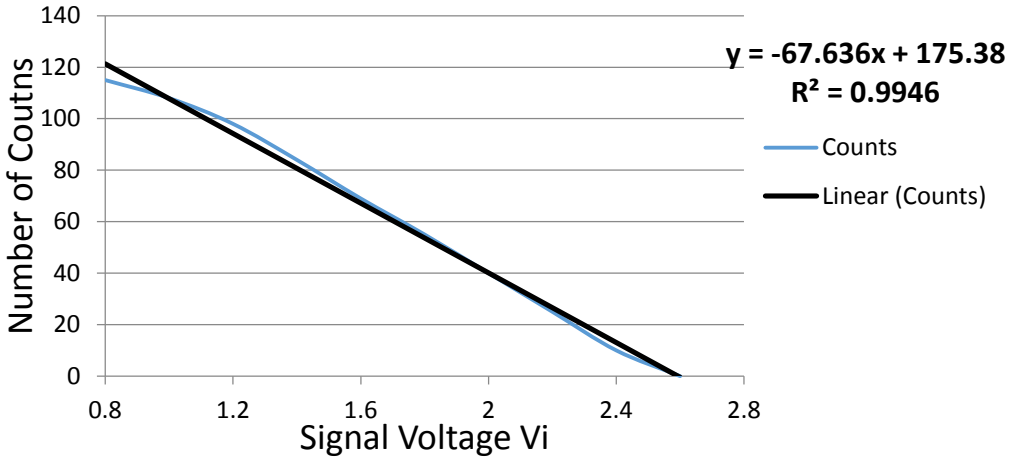


Figure 3.18 Linearity of delta-sigma modulator post layout with an ideal off chip clock. Rise and fall times were set to 100 fs.

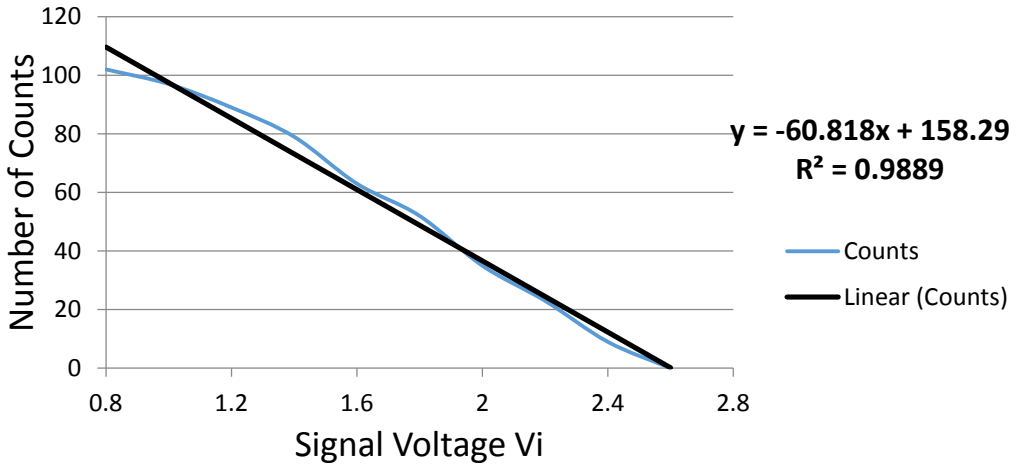


Figure 3.19 Linearity of delta-sigma modulator post layout with on chip oscillator at 10 MHz.

Chapter 4

Testing and Results

4.1 Testing Procedures

The first part of testing was done in order to check chip functionality. If the chip does not function as designed, then a redesign would have been necessary, along with a subsequent tape out. The first check that was made was to look at a micrograph of the chip and verify by eye that the chip did not have any obvious defects. A micrograph of the final chip is shown in Figure 4.1. Once the chip was confirmed to be free of any visual defects, a test board was designed.

A printed circuit board (PCB) was then designed in order test the desired chip functionality. A picture of the test board is shown in Figure 4.2. The inverters were used to sharpen the off chip clock, reset, and hold signals. They were also placed on the output of the delta-sigma modulator in order to sharpen the output pulses, so that RC constant effects are reduced when probed with the oscilloscope. To create a 2.6 V reference signal, a potentiometer was used. Using this divider, the potentiometer was then fine tuned to reach exactly 206 V. To simulate the signal input voltage, the same technique as setting the reference was used. The signal voltage potentiometer was then incremented in 200 mV steps from .8 V to 2.6 V to match the simulation. An off chip clock of 10 MHz was generated using an Agilent 33220 signal generator. At each 200 mV interval the number of output pulses was counted then tabulated in Excel to observe the output linearity.

While using the same off chip clock, the SNR, SFDR, and ENOB were then tested. The 2.6 V

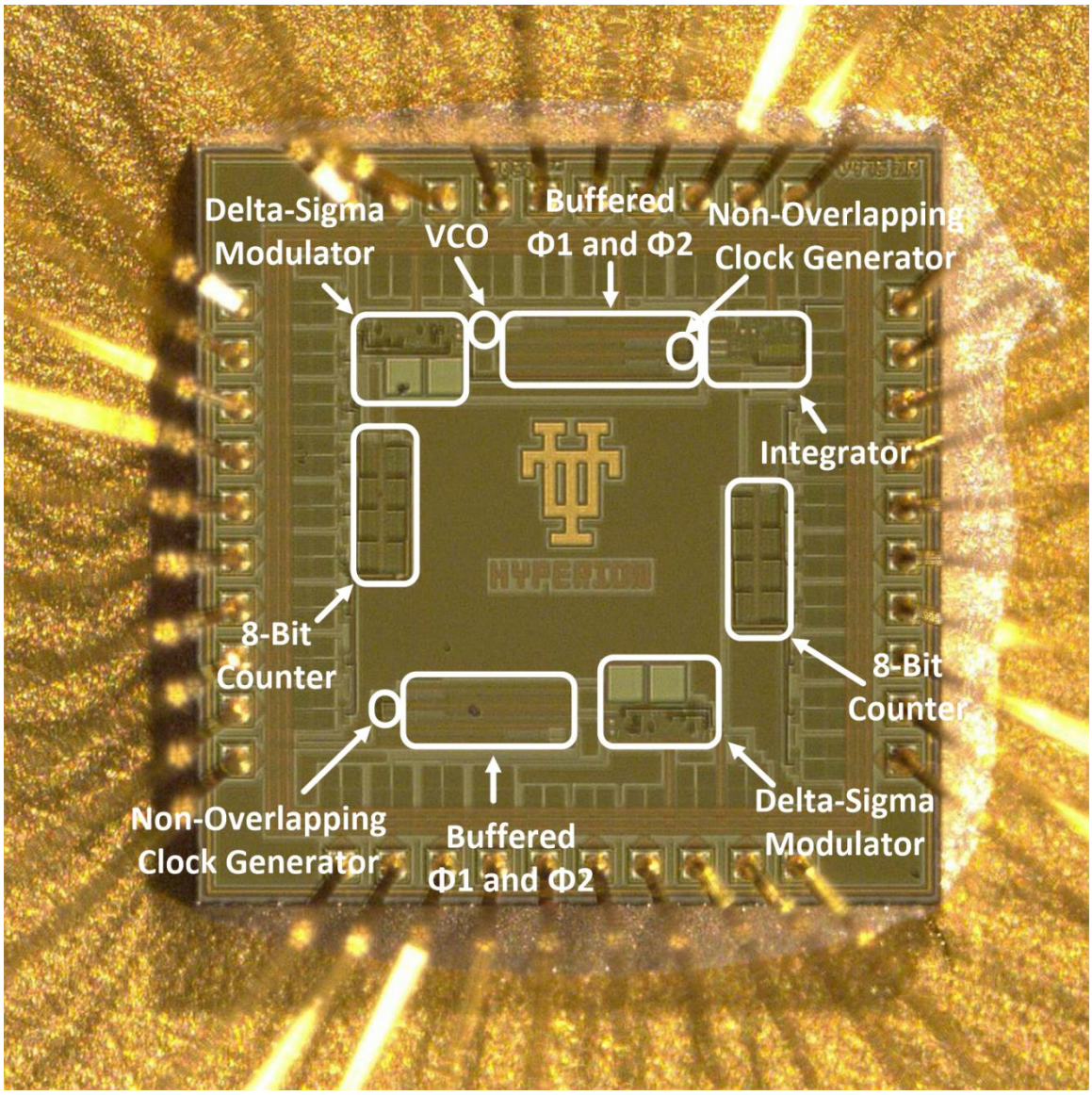


Figure 4.1 Micrograph of Hyperion chip.

reference was maintained, but the signal potentiometer was removed and a sine wave was then implemented. Since the application will be low frequency, a 500 Hz sine wave was

used. An offset of 1.7 V was applied with an amplitude of 900 mV. This allows a full swing from 1.7 V to 2.6 V and from 1.7 V down to 800 mV, simulating the range of the

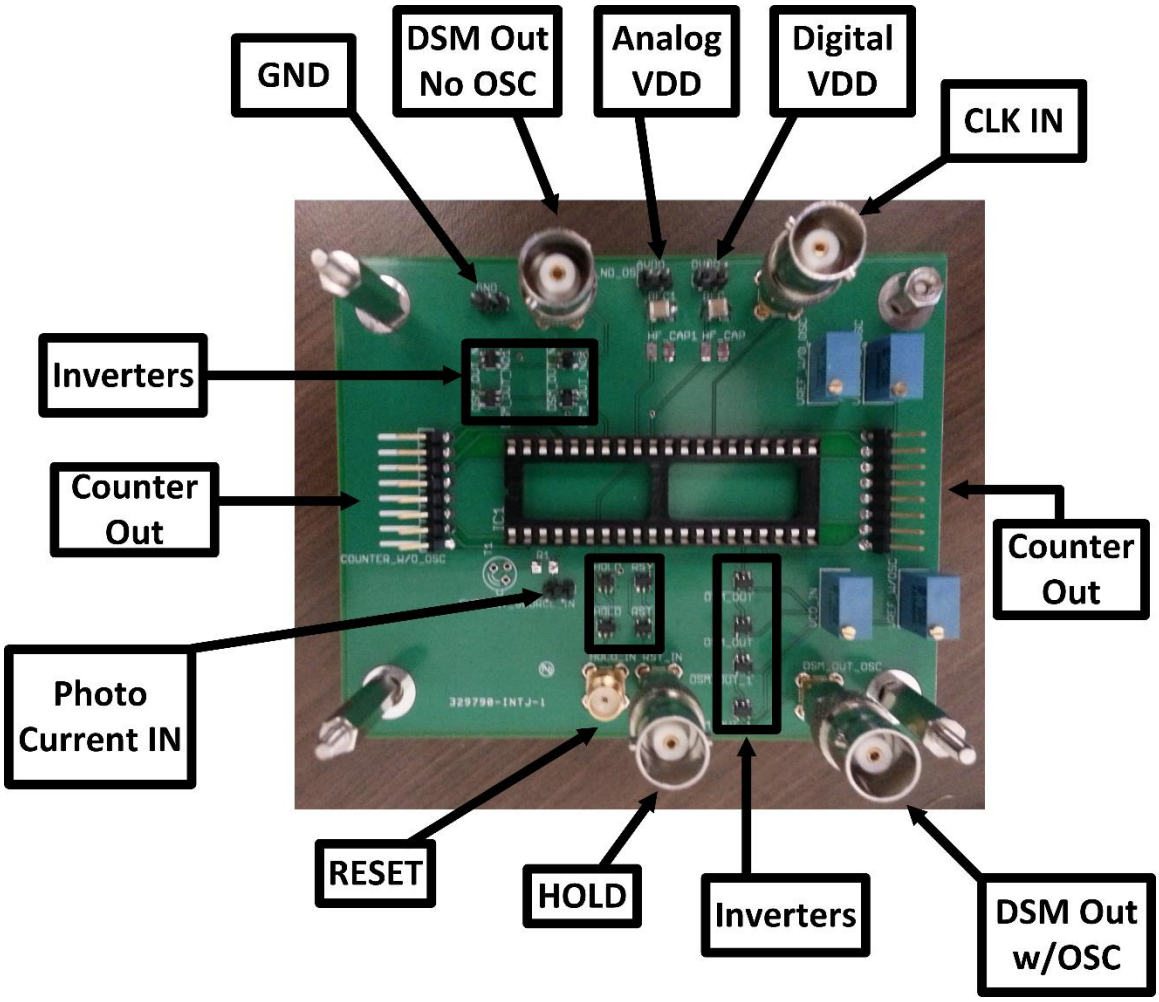


Figure 4.2 PCB test board.

signal input voltages. The output sine wave was observed along with analyzing the FFT of the output signal.

Initial tests showed that the ΔΣ modulator output counts performed as expected when compared with post-layout simulations. The SNR SFDR, and ENOB however

performed worse when compared with the simulation results. These lower figures could be due to higher frequency input signal than designed for or input sine wave distortion.

In order to test the integrator, the necessary hold and reset signals needed to be created using LabView 2013 software by National Instruments. Using a clock of 10 MHz and a resolution of 7 bits, the necessary integration time is 12.8 μs.

4.2 Results

This section will discuss and display the test results of the chip that were presented in the previous sections. Initial tests show that the chip is working favorably. The delta-sigma modulator was tested with signal input voltages ranging from .8 V to 2.6 V. These results are comparable to the post layout results in Figure 3.18, where the R^2 value was .995. The following figures show the output counts of the ΔΣ modulator at certain signal voltages, as well as graphing the counts to observe linearity. After testing the output count linearity, the chip was tested in order to find the SNR, SFDR, and ENOB figures. As discussed before, the sine wave had a frequency of 500 Hz with an offset of 1.7 V and an amplitude of 900 mV. The results are shown in Figure 4.8.

The integrator was the next block that needed to be tested on the bench. Simulating photodiode currents ranging from 1 nA to 31 nA was performed using a Kiethley 2636A current source. The results are shown in Figures 4.9 and 4.10.

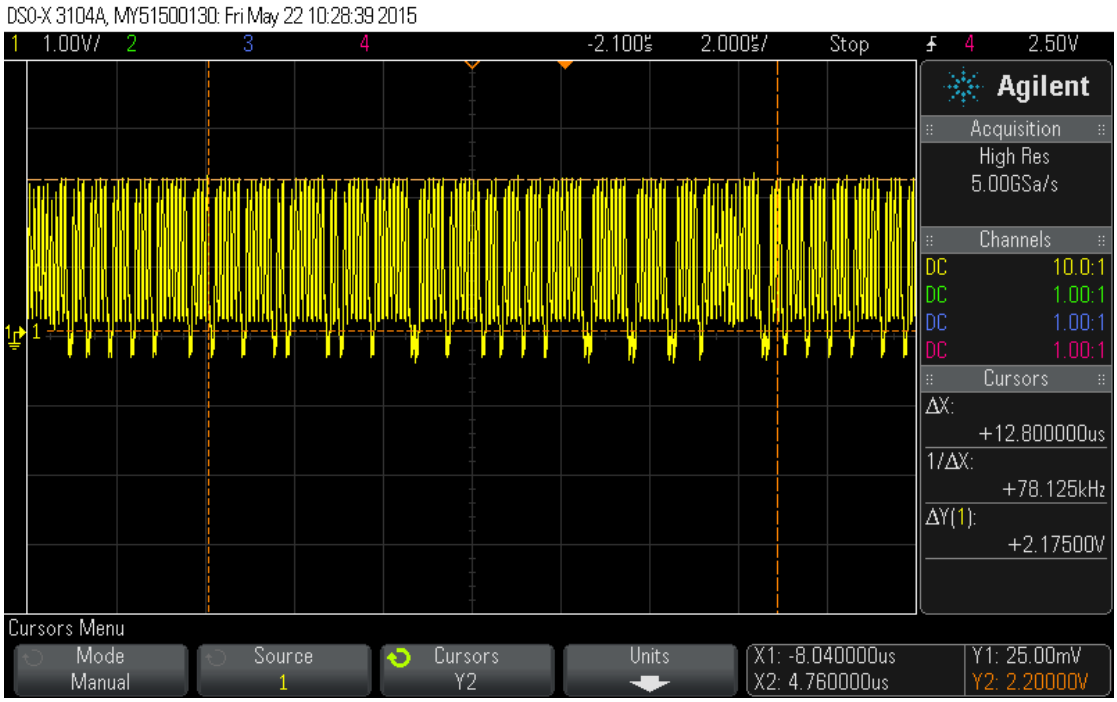


Figure 4.3 Output counts with signal of 800 mV. Cursers are measuring 12.8 µs.

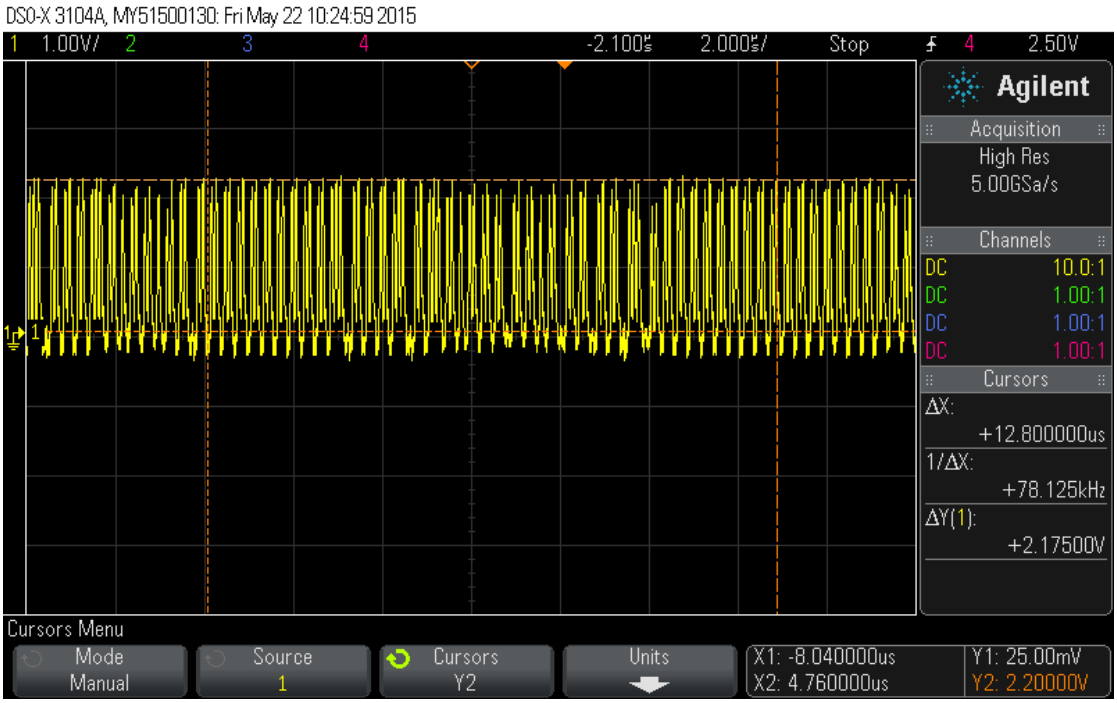


Figure 4.4 Output counts with signal of 1.4 V. Cursers are measuring 12.8 µs.

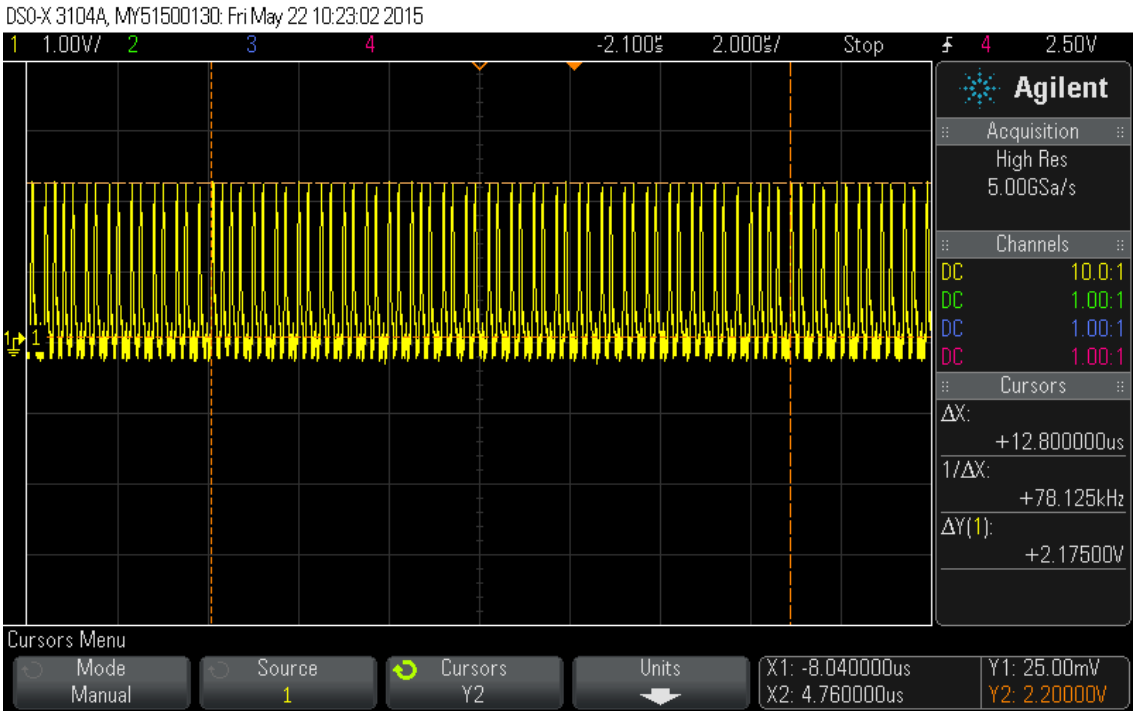


Figure 4.5 Output counts with a signal voltage of 2 V.

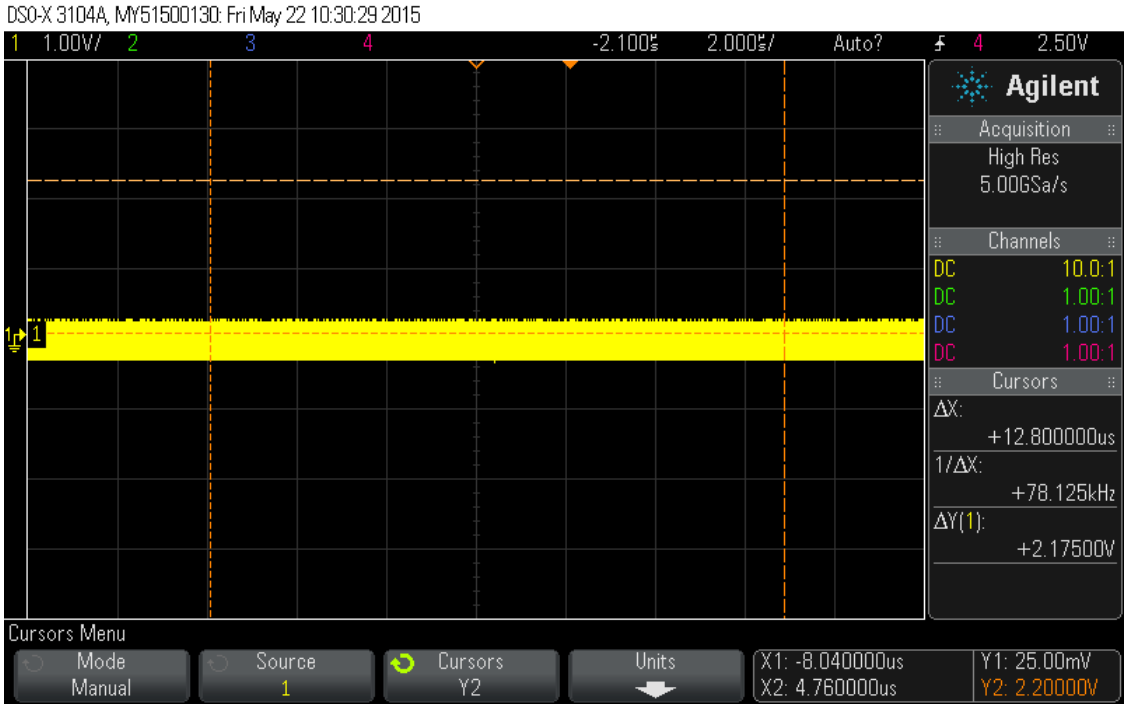


Figure 4.6 Output counts with a signal voltage of 2.6 V.

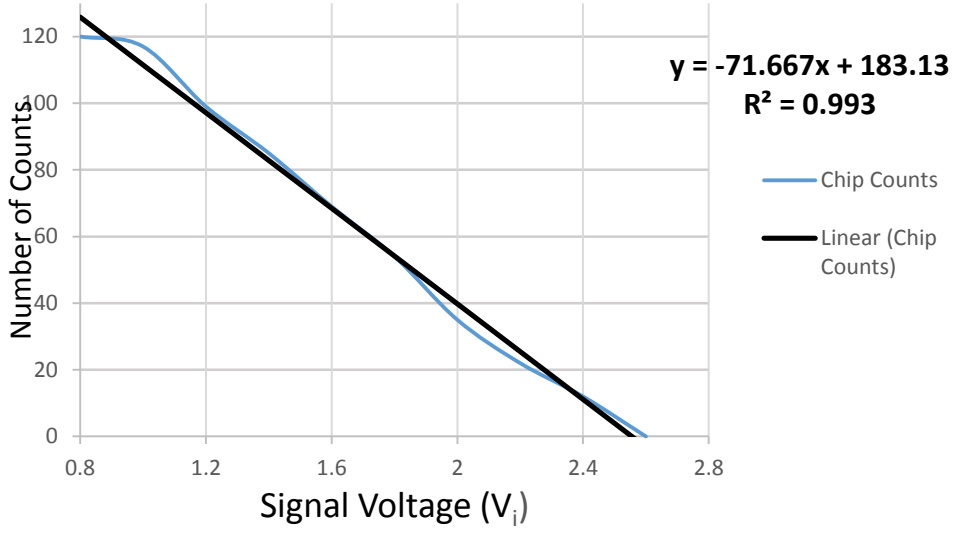


Figure 4.7 Testing linearity in delta-sigma modulator with off chip clock.

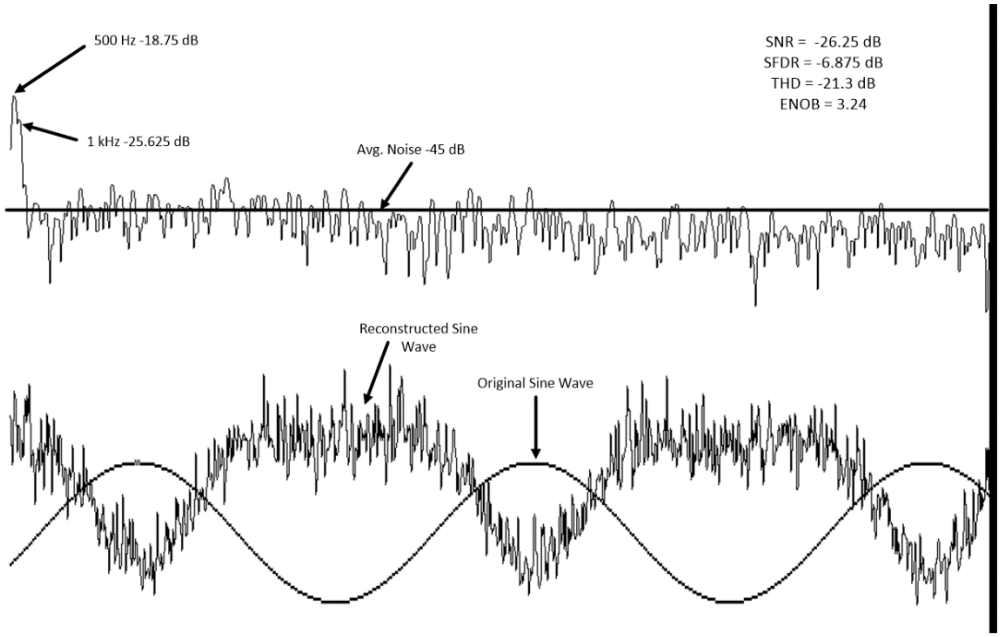


Figure 4.8 Measurement of SNR, SFDR, THD, and ENOB.

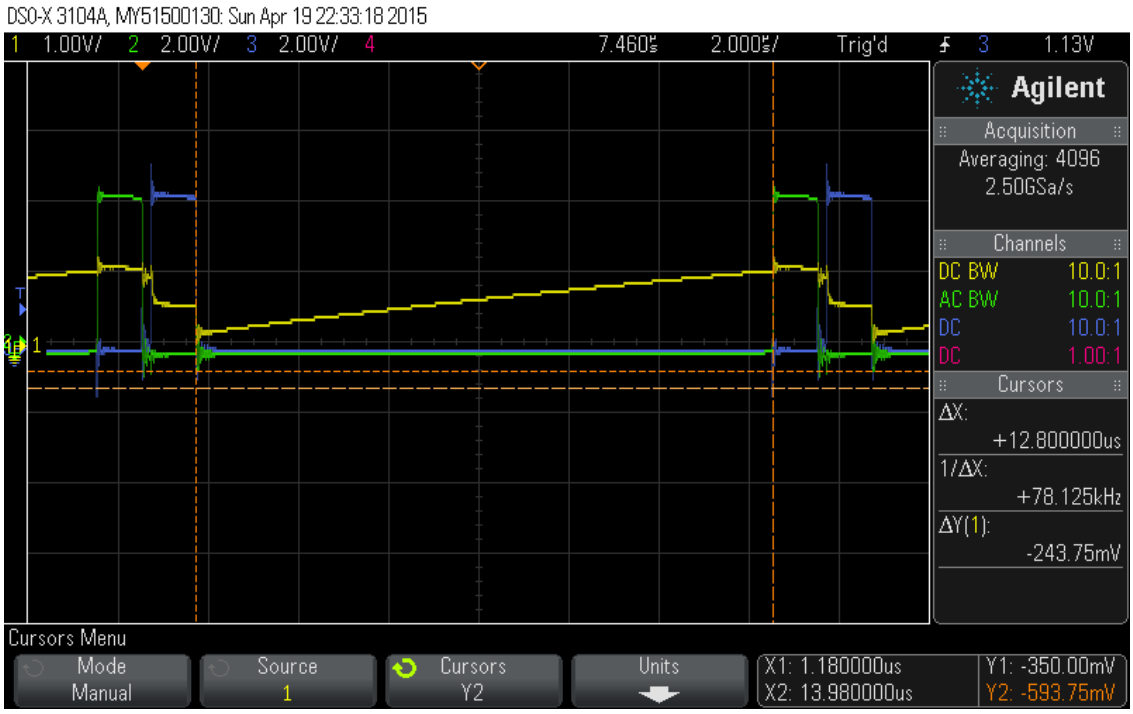


Figure 4.9 Integrator simulation with no photodiode input.

As Figure 4.9 shows, the integrator is integrating and then resetting as the simulation suggested it should. The issue is that there should be no charge available to charge the gate-source (C_{gs}) capacitance. Leakage current from the RESET switch could explain this charging of the C_{gs} capacitance. However, there is no pin available on chip in order to test the RESET switch for this possible leakage.

After observing the results in Figure 4.9, a 25 nA current was then used in order to see if the operation of the integrator changed. The operation of the integrator changed when the 25 nA current was applied. This is shown in Figure 4.10. When the current is applied, the integrator rises to the DC level that is being set by the Kiethley current source. With the current source setting the DC voltage on the input to the integrator

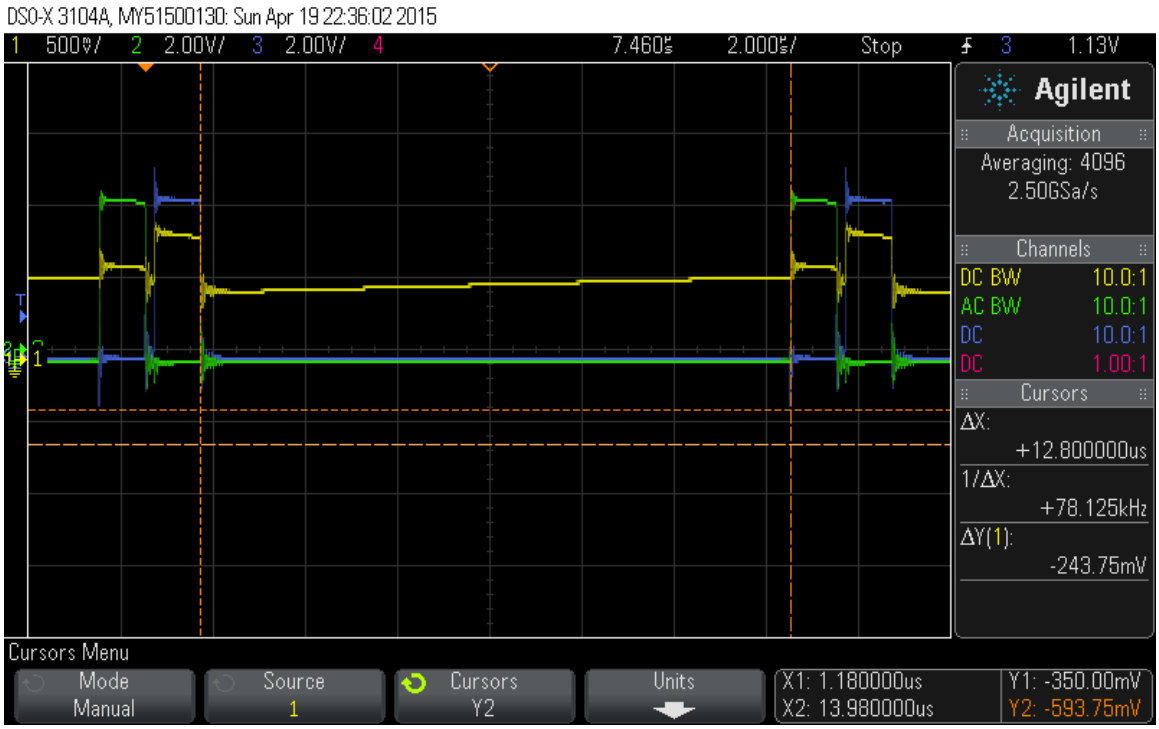


Figure 4.10 Input of 25 nA applied to the integrator.

at approximately 0.66 V, the integrator then only resets to this voltage level as shown in Figure 4.10.

While physical size, laser power reduction, and circuit power reduction were the main goals of this project, no certain specification for power consumption was set. However, when reducing the circuit from discrete parts to an SOC, the reduction in power usually follows. Table 1 shows the power consumption estimate for the entire system.

Table 4.1 Power consumption estimation.

	ΔΣ Modulator and Comparator	Integrator
Current	4.25 mA	226 μA
VDD	3.3 V	3.3 V
Power	14.025 mW	754.8 μW

Chapter 5

Conclusions and Future Work

5.2 Conclusions

This thesis presents a system-on-a-chip design that can accurately measure the gas composition of the atmosphere. The desired input dynamic range from the photodiode is 30 dB and the achieved dynamic range in simulation is 31.13 dB. However, the integrator did not work as simulation suggested it should on the laboratory bench and different methods were used to try and discover why it did not perform correctly. No reason was found and with no probe points on any of the nodes of the integrator, it is difficult to find the answer.

High output count linearity of .993 (.9949 truncated value) was achieved in order to correlate this count to the input light intensity versus the reference signal. While providing high output linearity, die area and power consumption were greatly reduced when compared with current atmospheric gas composition sensing systems. Future work on this system could further improve performance for greater accuracy, resolution, and also extreme temperature and radiation environments.

5.3 Future Work

Future development on this network is needed. This POC design shows that this circuit can be put onto a chip with success according to pre- and post-layout simulation results as well as the laboratory bench testing results. The following are suggestions for future development and improvements to the core network design.

5.3.1 Faster Clock and Clock Edges

One area that can be further developed without much effort is to increase the frequency of the main clock signal so that the network switches faster allowing more counts, which in turn allows increased resolution on the output from the network. Increased resolution on the output will give a greater confidence to the end user knowing that the circuit has taken the appropriate amount of counts so that the output directly corresponds to the correct input voltage. A faster clock will also allow the reduction of capacitor values, which in turn results in reduced CMOS ship area. This translates to greater area being available to put more onto one chip, or multiple ΔΣ modulators being placed on one chip.

5.3.2 Multi-Well Process

As was discussed in the problems section, one major hurdle that took some time to solve was the switching problem on the Switched Capacitor Network. This slow switching, was translating into a very non-linear mapping between the signal input and output count. This can be at least partially mitigated by using a multi-well process that would allow for better isolation of the switches. Another contributing factor, is the larger channel CMOS process used is moderately large in comparison to more modern processes which contributes to larger device capacitances and slower operating speeds. A smaller process could provide significantly sharper clock edges, which would increase the accuracy of the switched capacitor network.

5.3.3 On-Chip Reference

The reference voltage was moved off chip so that this value could be dialed in precisely to achieve the most linear response. Once this value is determined, putting this on-chip frees up a pin that can be used for other signals. This was not critical for this stage, but needs to be considered for developing a self-contained system-on-a-chip.

5.3.4 Rad-Hard and Temperature Sensitivity

While this POC design did not need to be RAD-hard or perform in extreme temperatures, these environments need to be considered in future designs. In silicon, as the temperature increases, the threshold voltage decreases and the thermal voltage increases. This can cause the transistor to then turn on when it should be off if the threshold has dropped significantly. Not only does thermal and threshold voltage change with a rise in temperature, but the electron and the hole mobilities decrease which can lower the drain current well below the designed levels. However, if temperature has increased enough to lower the threshold voltage significantly while V_{GS} is low, the threshold voltage change will dominate, and cause drain current to increase. Once this point is reached, drain current will continue to rise along with rising temperature. Another problem, the phenomena of hot carrier injection (HCI) can also result from increases in ambient temperature conditions, which could be encountered in space applications or other extreme locations on Earth. A radiation hardened design was not considered in this phase of the design, but the resistance to radiation could be evaluated and tested for improvement and reliability in this area.

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Appendix

In order to understand a ΔΣ ADC in more depth an example is usually helpful. A block diagram showing the basic structure of a typical ΔΣ ADC is shown in Figure A.1 below. The difference between the input X and the feedback signal W is the first part of the circuit. This is the delta operation. This delta value B then goes into the integration block. This integration block then passes this summed value C to the comparator where the output of the comparator D goes through a digital filter and through a 1 bit DAC (digital to analog converter) that is in a feedback loop to the difference node at the input. The feedback loop forces the average of the output signal W to be equal to the input signal X.

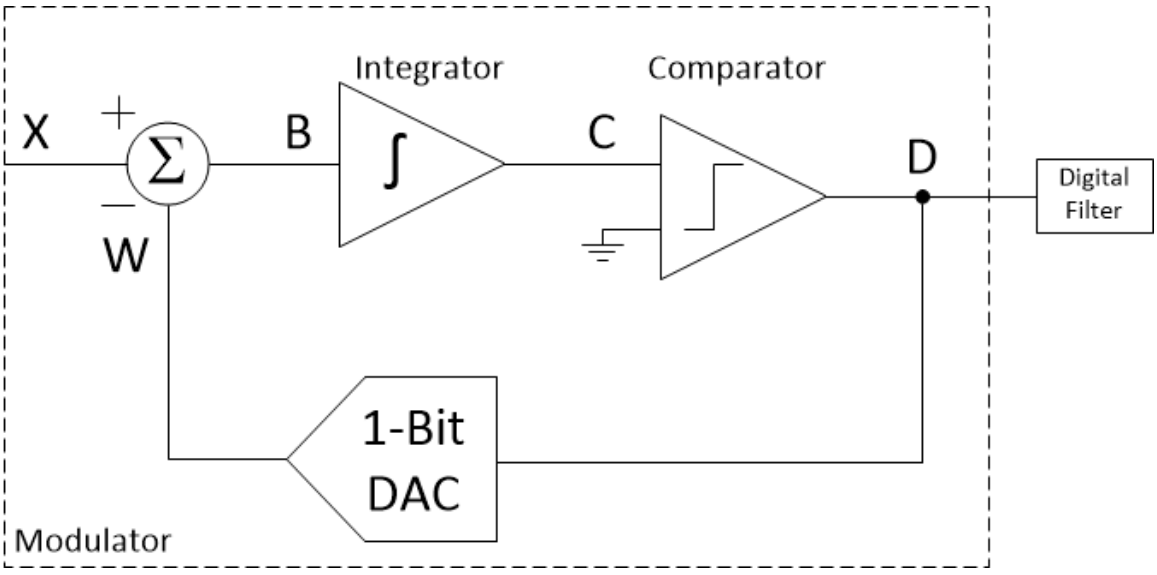


Figure A.1 Block Diagram of Typical ΔΣ Modulator [25].

The table below will go through a numerical example and demonstrate the power that this averaging scheme has. The input, X, has a DC value of 3/8. This table will show the resultant values at each stage of the modulator.

Table A.1 Conversion example of a typical ΔΣ modulator.

Sample (n)	X (INPUT)	B ($A-W_{n-1}$)	C ($B+C_{n-1}$)	D (0 or 1)	W (-1 or +1)
0	3/8	0	0	0	0
1	3/8	3/8	3/8	1	+1
2	3/8	-5/8	-2/8	0	-1
3	3/8	11/8	9/8	1	+1
4	3/8	-5/8	4/8	1	+1
5	3/8	-5/8	-1/8	0	-1
6	3/8	11/8	10/8	1	+1
7	3/8	-5/8	5/8	1	+1
8	3/8	-5/8	0/8	0	-1
9	3/8	11/8	11/8	1	+1
10	3/8	-5/8	6/8	1	+1
11	3/8	-5/8	1/8	1	+1
12	3/8	-5/8	-4/8	0	-1
13	3/8	11/8	7/8	1	+1
14	3/8	-5/8	2/8	1	+1
15	3/8	-5/8	-3/8	0	-1
16	3/8	11/8	8/8	1	+1
17	3/8	-5/8	3/8	1	+1
18	3/8	-5/8	-2/8	0	-1

As the table shows, at sample 0, the input is 3/8 while all other nodes are at 0. Since the value at C is greater than ground, the output is a +1. This continues from sample 1 through 16 (sample 0 is discarded since it is a start-up condition). When adding the values from the W column and dividing by the number of samples, in this case 16, the

answer is 6/16 = 3/8. This pattern will then repeat over the next 16 samples and again, the output will once again converge 3/8. This is obviously an ideal case where no quantization noise has corrupted the input signal. The digital filter on the output of the comparator is there to filter this quantization noise so that the SNR is much higher than without filtering.

Vita

Christopher Crowder was born in Knoxville, TN to the parents of James and Deborah Crowder. He is the only child. His education began at Sterchi Elementary School in Kindergarten. He attended Sterchi through the 5th grade, and then went to Gresham Middle School through 8th grade, and then went on to Knox Central High School. In high school, Chris participated in football and baseball where he was a team captain his junior and senior years. He graduated among the top of his class in May of 2006, and then enrolled at the University of Tennessee in August of 2006. Chris's initial interests were in Biology and Chemistry, so he declared his major to be Bio-Chemistry, Cellular and Molecular Biology (BCMB). After spending three and a half years in this field, Chris got a part-time job as an electrician with a local electrical company. This sparked Chris's interest in how electronics and power systems operated. He changed his major from BCMB to electrical engineering in the summer of 2010. He received his bachelor's degree with a major in electrical engineering in December of 2013. Directly after receiving his bachelor's degree, he accepted a GRA position under Dr. Syed Kamrul Islam in the Analog, VLSI and Devices Laboratory in January of 2014. Chris graduated with a Master's of Science from the University of Tennessee in May 2015. Chris hopes to find an electronics design job close to Knoxville, where all his friends and family live.