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I am submitting herewith a thesis written by Suheng Chen entitled “G⁴-FET Based Voltage Reference.” I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Dr. Benjamin J. Blalock

Dr. Benjamin J. Blalock, Major Professor

We have read this thesis
and recommend its acceptance:

Dr. Syed K. Islam

Dr. M. N. Ericson

Accepted for the Council:

Anne Mayhew

Vice Provost and Dean of Graduate Studies

(Original signatures are on file with official student records)

G^4 -FET BASED VOLTAGE REFERENCE

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Abstract

A precise and stable voltage reference is essential to analog/mixed-signal SoC (system-on-a-chip) applications. The most commonly used voltage reference in standard CMOS processes, the bandgap voltage reference, is limited due to output drift in wide temperature range applications. The temperature drift associated with the bandgap voltage reference is non-linear, thus temperature compensation is difficult. A new reference circuit, the JFET-based voltage reference, is proven to be more temperature stable. However, the JFET-based voltage reference requires a specialized Bi-CMOS process with additional fabrication steps to alter the channel doping for selected devices. The purpose of this thesis is to investigate the feasibility of the JFET-based voltage reference circuit topology in a CMOS-compatible process. The novel G^4 -FET device fabricated on a standard PDSOI (partially-depleted silicon-on-insulator) CMOS process is chosen as an alternative to the JFET device. A theoretical development of the G^4 -FET is summarized and results of device characterization are presented. Based on device characterization, all four gates of the G^4 -FET device are exploited to achieve an equivalent circuit operation without requiring any additional process steps. Results from this characterization are used to design an improved voltage reference based on G^4 -FETs and test results from a prototype reference circuit are shown including output temperature coefficient, output noise, and power supply rejection. The output voltage achieves approximately constant output variation with temperature over the temperature range of $-5\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, implying that the circuit may be readily temperature compensated, in this case by an inverse-PTAT (proportional-to-absolute-temperature) current. Finally, suggestions for improved reference performance and fully monolithic compatibility are given.

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Chapter 1 INTRODUCTION

1.1 Voltage Reference Applications

Voltage reference circuits are required to generate a stable and precise voltage level, to reject disturbance from the power supply, and to have low drift over temperature and time [4]. In an analog/mixed-signal system, the voltage reference is a critical building block because it has a direct impact on the performance and accuracy of the overall system, especially for a data conversion system. For example, in a digital-to-analog converter (DAC), the tolerance of the voltage reference directly translates to the resolution of the DAC. For example, a ± 5 mV error at the DAC input is translated to 0.1% or 10-bits accuracy if the full-scale range is 5 V. Although such a voltage reference can be generated off-chip, it is preferable to generate it on-chip in a fully integrated system, especially for SoC applications.

1.2 Voltage Reference Requirements

There are several key aspects in evaluating a voltage reference circuit. These include the power supply rejection (*PSR*), temperature drift, and long-term stability. Thermal hysteresis, noise, and power consumption are also important.

Depending on system specifications, some requirements for a voltage reference may take precedence to others. For example, in applications such as high-resolution converters, noise and short-term stability are important issues. If the converter is used in a temperature sensor application, its temperature behavior is also of concern.

Consequently, these key aspects of voltage reference circuits are the decisive parameters to evaluate whether this critical building block meets the system specification. Each of these parameters is described in more detailed in the following sections.

1.2.1 Power Supply Rejection

To ensure the robustness of a system, a “qualified” voltage reference circuit must reject fluctuations in supply voltage and generate a clean reference voltage. *PSR* is often used to evaluate how well a voltage reference circuit rejects noise or spurious signals at a given frequency coupled on the supply rails, which can be expressed in dB as a function of frequency as

$$PSR(f) = 20 \cdot \log \frac{V_{OUT}}{V_{SUPPLY}(f)}. \quad (1.1)$$

The PSR over a wide frequency range describes the susceptibility of the voltage reference circuit to power supply noise. In addition, the PSR can be used to estimate the variation of reference voltage due to supply noise.

1.2.2 Temperature Drift

To provide a useful voltage reference over a wide temperature range, a well-controlled voltage over temperature range is important to system accuracy. Temperature coefficient (TC) is used to describe how much the output voltage drifts with temperature [5]. The TC at 25 °C is given by:

$$TC(25\text{ }^{\circ}\text{C}) = \frac{1}{V_o(25\text{ }^{\circ}\text{C})} \frac{dV_o}{dT} \times 10^6 \quad [ppm/^{\circ}\text{C}]. \quad (1.2)$$

Ranging from a few parts per million (ppm)/°C to hundreds of ppm/°C, temperature requirements vary with application. This variation in reference voltage over temperature directly affects the accuracy of a system. For example, an 8-bit analog-to-digital converter (ADC) using a reference voltage of 3.3 V operating over a 60 °C temperature span requires that the drift of the voltage reference with temperatures be less than 32 ppm/°C (107 μV/°C). For the ADC to operate over a 100 °C temperature range, the tolerance in temperature drift goes down to 19.5 ppm/°C (64 μV/°C). This illustrates the stringent requirements placed on voltage references in wide temperature range applications.

1.2.3 Thermal Hysteresis and Long-term Stability

Voltage reference circuits often exhibit a phenomenon in which the output drifts after temperature cycles, known as thermal hysteresis. Thermal hysteresis is often described by the following equation:

$$V_{REF_HYSTERESIS} = \frac{V_{REF}(25\text{ }^{\circ}\text{C}) - V_{REF}(25\text{ }^{\circ}\text{C}_{-cycle})}{V_o(25\text{ }^{\circ}\text{C})} \times 10^6 \quad [ppm/^{\circ}\text{C}] \quad (1.3)$$

where

$V_{REF}(25\text{ }^{\circ}\text{C})$ = Initial V_{REF} value at 25 °C, and

$$V_{REF}(25\text{ }^{\circ}\text{C_cycle}) = V_{REF} \text{ at } 25\text{ }^{\circ}\text{C} \text{ after a complete temperature cycle.}$$

Here, room temperature (25 °C) has been selected as a baseline temperature. In addition to thermal hysteresis, long-term stability is also important, particularly for repeatability within a system. The long-term stability in a voltage reference circuit is mainly because of “random walk” phenomenon [6] and increases with the *square root* of the elapsed time, usually expressed in ppm/1000 hours.

1.2.4 Additional Specifications

There are many other parameters in evaluating voltage reference circuits. One important parameter is the initial accuracy, which is often hard to achieve due to process variations. Power consumption is an important factor especially in battery-powered applications. Output noise from a reference circuit will compromise accuracy in data conversion systems. In addition, dynamic issues like start-up behavior must be considered in the design of robust reference circuits.

1.3 Organization of the Thesis

The importance and requirements of a voltage reference circuit have been briefly reviewed. In the next chapter several common voltage reference circuit topologies including a bandgap voltage reference, a voltage reference based on threshold difference and a JFET-based voltage reference will be briefly discussed. A performance comparison is then provided. In the third chapter, the design and implementation of the G^4 -FET reference circuit is presented on the basis of theoretical development derived from G^4 -FET device characterization. In the fourth chapter, test setups and characterization of the G^4 -FET reference circuit are presented. In the final chapter, possible enhancements and future work are discussed.

Chapter 2 VOLTAGE REFERENCE CIRCUIT REVIEW

This chapter reviews three on-chip voltage reference topologies widely used in integrated circuit (IC) design. In addition, a performance comparison is given to aid in selecting a circuit topology for this work. This work seeks to find a precise voltage reference suitable for on-chip implementation in a silicon SoC-compatible fabrication process.

2.1 Voltage Reference Circuit Topologies

Depending on their availability in the target fabrication process, accurate elements are often employed to generate a stable reference voltage. Examples include the forward-bias diode voltage (V_D) and thermal voltage (V_T), both of which are available in most standard CMOS processes by creating a parasitic PNP bipolar device. In multi-threshold CMOS processes, the threshold voltage difference is often more tightly controlled over process variations as opposed to absolute threshold voltages, providing another accurate element with which a reliable reference voltage can be generated. In the following sections some important reference circuit topologies using different accurate elements are reviewed.

2.1.1 Bandgap Voltage Reference

The bandgap voltage reference circuit is widely used for generating a temperature stable on-chip voltage reference. It combines the positive TC ($\sim 85 \mu\text{V}/^\circ\text{C}$) of the thermal voltage with the negative TC ($\sim 2 \text{ mV}/^\circ\text{C}$) of the forward-bias diode voltage in a weighted fashion to achieve a voltage output with zero TC at a given temperature [5].

Figure 2-1 shows a basic implementation of the bandgap voltage reference. The left part of the circuit is a V_T -based current reference generating a current proportional to the thermal voltage. With the $n\text{MOS}$ device M1 matched with M2, and the $p\text{MOS}$ device M3 matched with M4, the currents flowing into both legs are equivalent. The voltage at node A is the same as at node B because the voltage drops from V_{DD} are equal. Applying Kirchhoff's Voltage Law (KVL) in the bottom loop, yields

$$V_{D1} = IR_1 + V_{D2} \quad (2.1)$$

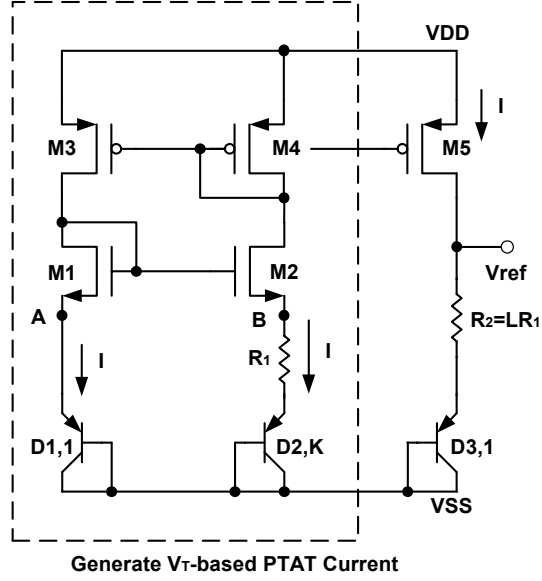


Figure 2-1 Basic Bandgap Reference Circuit

where the voltage across the diode-connected BJT, V_{D1} and V_{D2} , can be derived from the basic forward biased diode equation

$$I_D = I_S \cdot e^{V_D / nV_T} \quad (2.2)$$

as

$$V_{D1} = nV_T \ln \left(\frac{I_D}{I_S} \right) \quad (2.3)$$

$$V_{D2} = nV_T \ln \left(\frac{I_D}{K \cdot I_S} \right) \quad (2.4)$$

where

I_S = reverse saturation diode current,

n = non-ideality factor, and

K = ratio of junction area of diode D_1 and D_2 .

Substituting (2.3) and (2.4) into (2.1) and solving for I yields

$$I = V_T \cdot \frac{n \cdot \ln K}{R_1}. \quad (2.5)$$

Since $V_T = kT/q$ where k and q are independent of temperature (T), the current (I) is proportional to absolute temperature (PTAT).

The current, I , is mirrored to the output branch and flows into R_2 and D_3 to generate the output voltage, written in the equation

$$V_{REF} = I \cdot (LR_1) + V_{D3} = V_T \cdot \frac{n \cdot \ln K}{R_1} \cdot LR_1 + V_{D3} = V_T \cdot (nL \cdot \ln K) + V_{D3} \quad (2.6)$$

where

L = resistor ratio of R_2 and R_1 .

The variation in V_{REF} with temperature of the bandgap voltage reference is given by

$$\frac{dV_{REF}}{dT} = nL \cdot \ln K \cdot \frac{dV_T}{dT} + \frac{dV_{D3}}{dT}. \quad (2.7)$$

By choosing the factor L and K , the TC of the output voltage can be made zero at a certain temperature and the vicinity TC can be quite low.

However, the output voltages from the bandgap reference are not constant at all temperatures because the PTAT current only cancels the TC of V_D in the first order. The V_D can be written in the device physics equation [7],

$$V_D = V_T \cdot \ln \frac{I}{B' n_i^2 T \bar{\mu}_n} \quad (2.8)$$

where

V_T = the thermal voltage,

n_i (intrinsic carrier concentration) = $\sqrt{DT^3} e^{-(V_{G0}/V_T)}$,

$\bar{\mu}_n$ (electron mobility) = CT^{-n} , and

B' is temperature-independent quantity.

It can be seen both the term n_i and $\bar{\mu}_n$ are temperature dependent and non-linear. This explains why the output voltage of bandgap reference exhibits zero TC at a selected temperature (T_0), and the TC at other temperatures will be non-zero. The output voltage across a range of temperatures

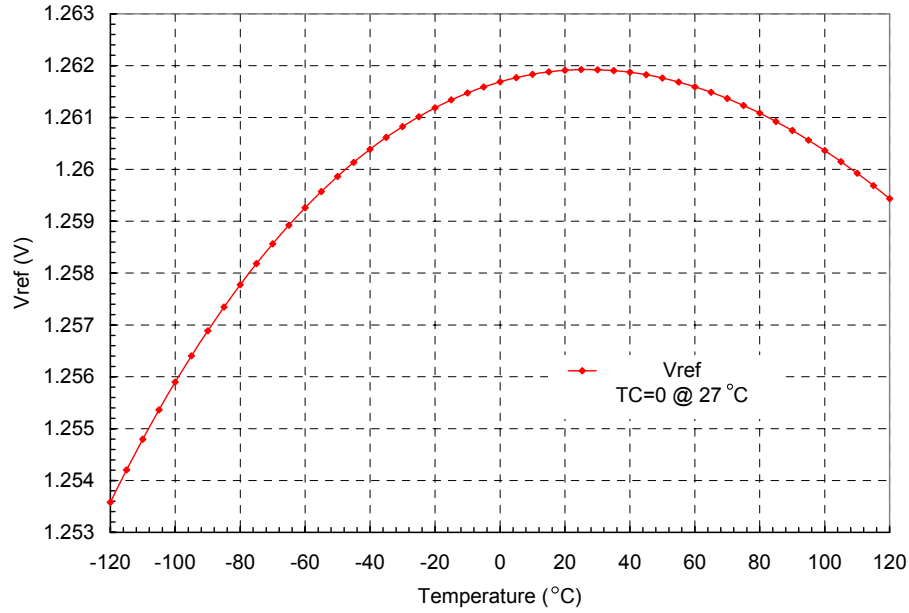


Figure 2-2 Variation of Bandgap Reference Output Voltage with Temperature

displays a curve, namely curvature error. The output voltage of the bandgap reference can be expressed as [7]

$$V_{OUT} = V_{G0} + V_T (\gamma - \alpha) \left(1 + \ln \frac{T_0}{T} \right) \quad (2.9)$$

where γ and α are circuit parameters. Assuming $\gamma = 3.2$ and $\alpha = 1$, the bandgap reference voltage at temperatures from -120 °C to 120 °C is shown in Figure 2-2. The curvature error inherent with the bandgap voltage reference causes the difficulties of achieving low TC in a wide temperature range.

In applications that require higher precision, the curvature compensation technique is employed to correct the error. With curvature compensation and post-process trimming, the TC that a bandgap voltage reference achieves can be very low. The TC of Song and Gray's CMOS bandgap reference [8] approaches 10 ppm/°C after employing the curvature compensation technique.

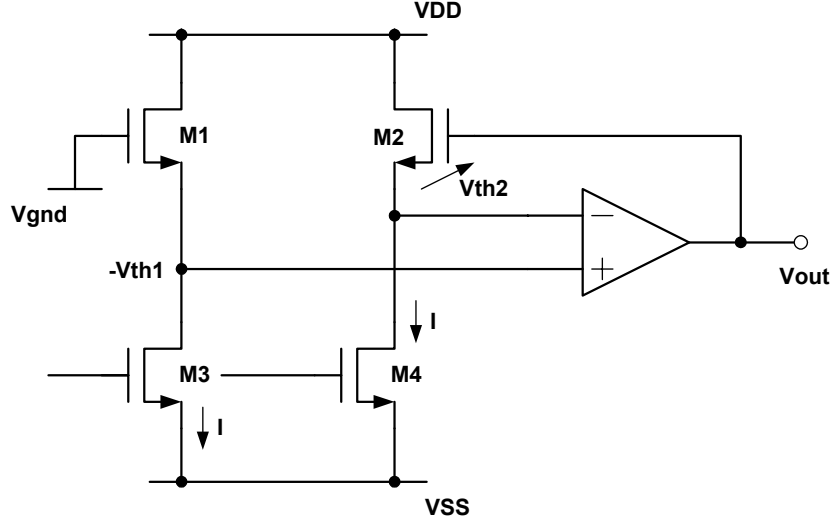


Figure 2-3 Threshold Difference Reference Circuit

2.1.2 Voltage Reference Based on Threshold Difference

Another topology is the voltage reference based on threshold difference. In some multi-threshold processes, an additional implant step provides select transistors with different threshold voltages. Although absolute accuracy of threshold voltage is still difficult to achieve, the relative accuracy of the threshold difference is fairly high, hence the threshold difference can be used to generate voltage reference [9].

Figure 2-3 shows the circuit generating voltage from the threshold difference of M1 and M2. The transistors M1 and M2 have different threshold voltages, V_{th1} and V_{th2} , respectively. For transistor M1, there is one threshold voltage drop from gate to source. Hence, the positive input of the opamp (operational amplifier) is $-V_{th1}$. Assuming an ideal opamp, the negative input of the opamp is also equal to V_{th1} . Therefore the output voltage is

$$V_{OUT} = -V_{th,1} + V_{th,2} \quad (2.10)$$

Song and Kim's voltage reference [10] reported the temperature coefficient of 33.8 ppm/°C over temperature range of -50 °C to 75 °C. This technique, however, requires some special process steps to obtain multiple threshold voltages are not often available in standard processes.

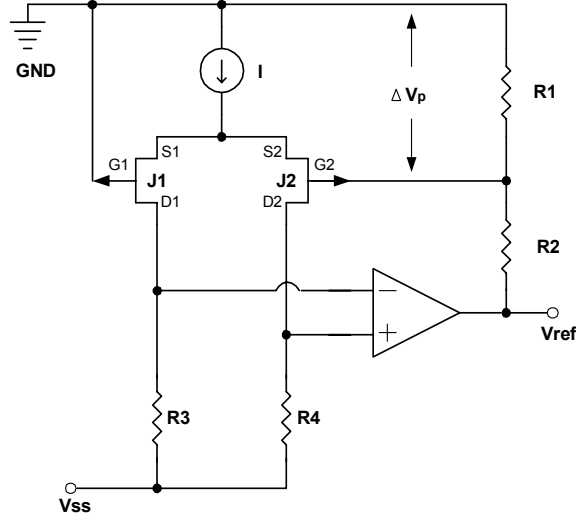


Figure 2-4 JFET Reference Circuit [1]

2.1.3 JFET Voltage Reference

Somewhat similar to the voltage reference circuit based on threshold difference, the JFET voltage reference circuit by Bower and Tippie [1] uses the difference of pinch-off voltages to generate the reference voltage. Figure 2-4 shows an implementation of this voltage reference circuit using depletion-mode P-channel JFETs.

The core of the JFET voltage reference consists of two JFETs with the same channel width and length, one of which has an extra channel implant to raise its pinch-off voltage. Their drains are connected to the opamp, with the resistors $R3$ and $R4$ being the same size, causing equal currents to flow into both legs. The JFETs operate in the saturation region and their difference in gate-to-source voltages equals the difference of their pinch-off voltages [1]. The output can be defined as the pinch-off voltage difference of two JFETs amplified by the resistor gain factor of $(1+R1/R2)$.

The pinch-off voltage of a JFET device is given by [11]

$$V_p = a^2 \left[\frac{q \cdot N_A \left(1 + \frac{N_A}{N_D} \right)}{2\epsilon} \right] - \Psi_0 \quad (2.11)$$

where

a = half channel thickness,
 q = electron charge,
 N_A = effective channel doping,
 N_D = effective gate doping,
 ε = dielectric constant of the silicon, and
 Ψ_0 = built-in junction voltage.

The built-in junction voltage, Ψ_0 , can be written as

$$\Psi_0 = kT/q \ln \left(N_A N_D / n_i^2 \right) \quad (2.12)$$

where

k = Boltzmann's constant,
 T = temperature in K, and
 n_i = the *intrinsic carrier density* of silicon.

The intrinsic carrier density can be expressed as [11]

$$n_i = \sqrt{N_C N_V} \cdot e^{\left(-\frac{E_g}{2kT} \right)} \quad (2.13)$$

where

N_C (*effective density of states in the conduction band*) = $2.8 \times 10^{19} \text{ cm}^{-3}$ for silicon, at 27 °C,
 N_V (*effective density of states in the valence band*) = $1.04 \times 10^{19} \text{ cm}^{-3}$ for silicon, at 27 °C, and
 E_g = energy bandgap of Si.

Substituting (2.13) and (2.12) into (2.9), it can be seen the variation of pinch-off voltage is non-linear with temperature. However, this non-linearity will be cancelled in the difference (ΔV_p) of pinch-off voltages V_{p1} and V_{p2} .

$$\begin{aligned}
 \Delta V_p &= \left\{ a^2 \left[\frac{q \cdot N_A \left(1 + \frac{N_A}{N_D} \right)}{2\varepsilon} \right] - \Psi_0 \right\}_2 - \left\{ a^2 \left[\frac{q \cdot N_A \left(1 + \frac{N_A}{N_D} \right)}{2\varepsilon} \right] - \Psi_0 \right\}_1 \\
 &= qa^2 / 2\varepsilon \left[N_{A2} \left(1 + N_{A2} / N_D \right) - N_{A1} \left(1 + N_{A1} / N_D \right) \right] - kT/q \left[\ln(N_{A2} / N_{A1}) \right]
 \end{aligned} \quad (2.14)$$

where

N_{A1} is the higher effective channel doping of the first JFET, and

N_{A2} is the lower effective channel doping of the second JFET.

The variation of ΔV_P with temperature is given by

$$\frac{d(\Delta V_P)}{dT} = -\left(\frac{k}{q}\right) \cdot \ln(N_{A2}/N_{A1}). \quad (2.15)$$

This result is only dependent on the channel doping of both JFETs and is independent of temperature. After compensating using a PTAT current source, a low TC reference voltage can be readily achieved. Given their first-order linearity with temperature before PTAT compensation, the JFET-based reference circuit avoids the curvature error observed in bandgap voltage references [1].

The commercial voltage reference series ADR29X and ADR42X by Analog Device Inc. are based on this JFET based approach. They achieve a TC of approximately 10 ppm/°C with low thermal hysteresis, low power consumption, and good long-term stability [12].

2.2 Performance Comparison

Table 1 shows the comparison of the three different reference topologies presented in this chapter. This comparison includes TC , thermal hysteresis, noise, power consumption, extra process steps, and long-term stability. The comparison focuses on the pros and cons associated with different designs, instead of comparing parameters from any specific implementation.

In standard CMOS processes, the bandgap reference is the most common approach available. The JFET-based reference is superior in terms of TC , long-term stability, and noise performance. However the JFET device is not readily available in most standard CMOS processes thus limiting the use of this improved topology.

Table 1 Performance Comparison of Different Reference Circuits (T=−40 °C to 85 °C)

	TC [ppm/°C]	Hysteresis [low/fair/high]	Noise [high/low]	Power Consumption [high/fair/low]	Extra process steps [yes/no]	Long- term Stability
Bandgap	~10	Fair	High	High	No	Fair
Threshold Difference	~40	Fair	Low	Fair	Yes	Good
JFET Reference	~5–10	Low	Low	Low	Yes	Good

Chapter 3 DESIGN OF THE G^4 -FET REFERENCE CIRCUIT

Inspired by the JFET reference circuit's low temperature drift, long-term stability, and low noise, this chapter explores the use of the G^4 -FET device, a novel four gate transistor fabricated in a standard PDSOI CMOS process, in a voltage reference circuit to meet the requirements of CMOS-based SoC applications.

Section 3.1 introduces the G^4 -FET device structure and its operation. Sections 3.2 and 3.3 present the theoretical development and design of the G^4 -FET-based voltage reference circuit.

3.1 G^4 -FET Device and Operation

The G^4 -FET is a novel device that was introduced as the MOS-JFET [2][14] because it combines the features of both the MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) and JFET (Junction Field Effect Transistor). The device can be fabricated in a standard PDSOI CMOS process without additional processing steps. The MOS-JFET was later renamed G^4 -FET, emphasizing that it has the maximum achievable number of gates. The four gates include two lateral junction gates that are similar to the gate of a JFET and two MOS gates at the top and bottom of the channel.

The G^4 -FET makes it possible to fabricate a JFET-like device in a standard PDSOI process. This makes it possible to design JFET-based circuits in standard SOI CMOS processes. This chapter briefly introduces the G^4 -FET structure and presents the design and implementation of a G^4 -FET reference circuit on the basis of theoretical development derived from G^4 -FET device characterization. With the G^4 -FET device modes of operation being quite versatile, emphasis is placed on how the G^4 -FET can be used as a JFET device with additional control via the poly (top) gate in this reference circuit.

3.1.1 Device Description

The structure of a G^4 -FET device is similar to a normal MOSFET device. The N-channel G^4 -FET can be derived from a P-channel MOSFET with explicit body ties and vice versa for the P-channel G^4 -FET. Figure 3-1 shows the device structure of a P-channel MOSFET compared to an N-channel G^4 -FET device and its schematic symbols [2]. The G^4 -FET devices are fabricated in a standard PDSOI process. The P+ source and drain diffusions of the MOSFET on both sides of the gate become the junction gates in the G^4 -FET, and the two N+ body terminals in the

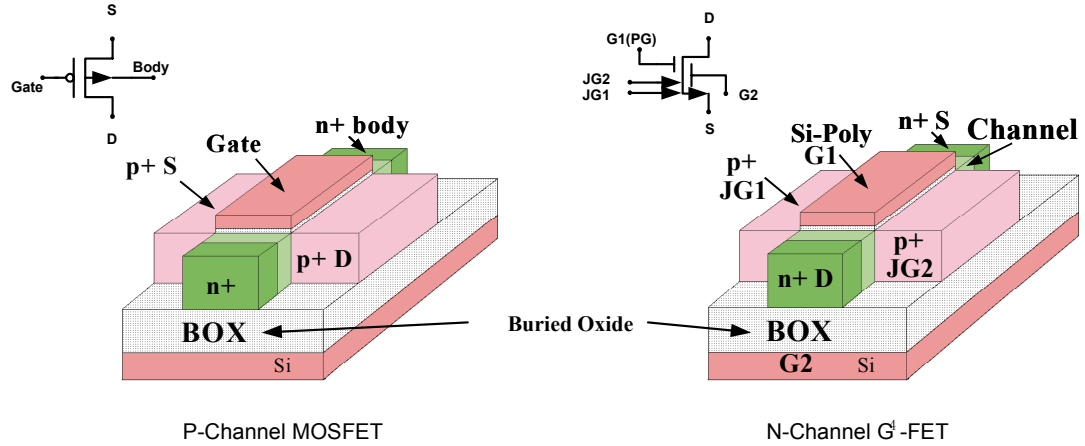


Figure 3-1 Device Structure: MOSFET vs. G⁴-FET [2]

MOSFET become the source and the drain of the G⁴-FET. The current in the G⁴-FET flows perpendicular to what would be the MOSFET current flow; thus, the width of MOSFET becomes the length of the G⁴-FET, and the length of MOSFET becomes the width of the G⁴-FET channel. Since both devices have the same structure, no extra processing steps are necessary to fabricate the G⁴-FET in a standard PDSOI process.

3.1.2 N-channel G⁴-FET Device Operation

In order to understand the operation of the G⁴-FET, devices of different sizes were characterized using an HP4145B semiconductor parameter analyzer. Figure 3-2 shows the drain current versus drain-to-source voltage (I_D vs. V_{DS}) of an N-channel G⁴-FET device with channel width of 0.35 μm and length of 1.5 μm . Figure 3-3 shows the drain current versus the junction gate voltage (I_D vs. V_{JG}) with different top gate biases of an N-channel G⁴-FET device with channel width of 3 μm and length of 2.4 μm .

For simplicity, the junction gates are tied together. In Figure 3-2, the top gate bias and junction gate biases are varied. In the lower part of the figure, the top gate is fixed at zero volts and the junction gate voltage is varied. Applying a negative voltage at the junction gate, the drain current is lowered until the channel is pinched off, demonstrating normal JFET-mode operation. For the upper part of the figure, the junction gate voltage is fixed at zero volts and the top gate is accumulated. The increasing drain current demonstrates accumulation-mode operation. It is clearly seen that both junction gates and the top gate have the capability of varying the drain current by modulating the conduction channel.

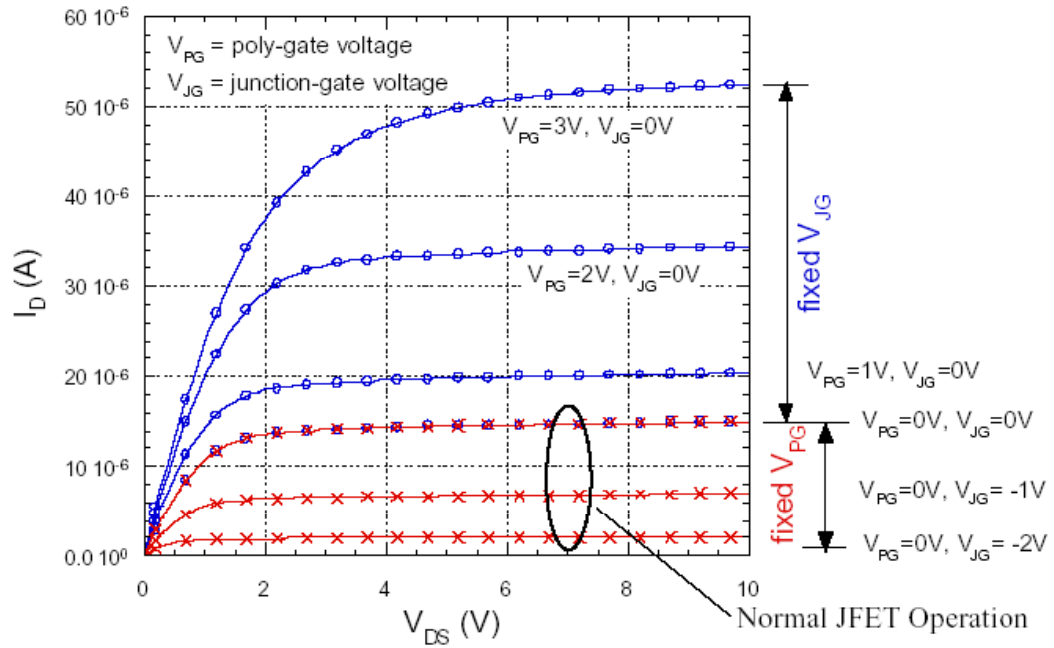


Figure 3-2 I_D vs. V_{DS} for a N-channel G^4 -FET (0.35 $\mu\text{m}/1.5 \mu\text{m}$) [3]

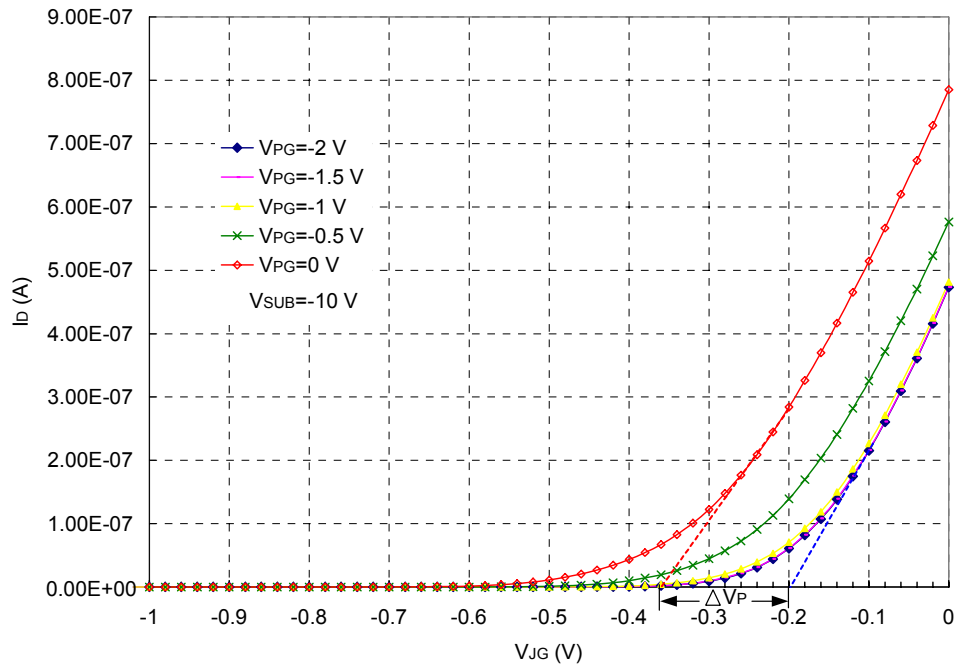


Figure 3-3 I_D vs. V_{JG} for an N-channel G^4 -FET at Triode Region (3 $\mu\text{m}/2.4 \mu\text{m}$)

In Figure 3-3, the G^4 -FET device is biased in the triode region by setting the voltage across the drain-to-source to be 50 mV to extract the pinch-off voltage. The top gate is swept from -2 V to 0 V and the back gate is biased at -10 V to achieve JFET mode operation [14].

It can be seen that the G^4 -FET has a different saturation current under different top gate biases. Using the linear extrapolation method to estimate the pinch-off voltages, Figure 3-3 shows a pinch-off voltage difference (ΔV_p) of about 160 mV can be established between 0 V and -2 V top gate biases. This characterization suggests using G^4 -FET as a JFET device and using two MOS gates, the top gate and the back gate, to adjust the pinch-off voltage. As will be shown, this ability to adjust the pinch-off voltage will be exploited to achieve the pinch-off voltage difference without additional process steps.

3.1.3 P-channel G^4 -FET Device Operation

The P-channel G^4 -FET is a complementary device to the N-channel G^4 -FET. Characterization shows the P-channel G^4 -FET fully functional. However, compared to the N-channel G^4 -FET, the P-channel G^4 -FET is less attractive in this process due to its larger pinch-off voltage magnitude.

Figure 3-4 shows the V_{DS} versus I_D of a P-channel G^4 -FET with channel width of $0.4\ \mu\text{m}$ and length of $0.9\ \mu\text{m}$. The source voltage is held at 0 V and the drain voltage is swept from -5 V to 0 V, with the back gate biased at 0 V. It can be seen from the figure that the device was not saturated with the drain voltage at -5 V, which indicates the P-channel G^4 -FET is more difficult to saturate compared to N-channel G^4 -FET due to its higher $|V_p|$.

Figure 3-5 shows the I_D versus V_{JG} and I_{JG} versus V_{JG} of the same G^4 -FET device. The top gate is biased at 0 V and the drain voltage are set to -4 V and -3 V. The junction gate is swept from 0 V to 5 V. It shows avalanche breakdown occurs at a V_{JG} of 3.7 V and 4.5 V, respectively. This also shows that the breakdown voltage decreases with increased drain voltage.

In the JFET reference circuit, the devices are required to operate in the saturation region. The P-channel G^4 -FET is difficult to use because it requires a much higher supply voltage to achieve saturation operation. The N-channel device is preferred because it has a much lower saturation voltage and higher junction gate breakdown voltage.

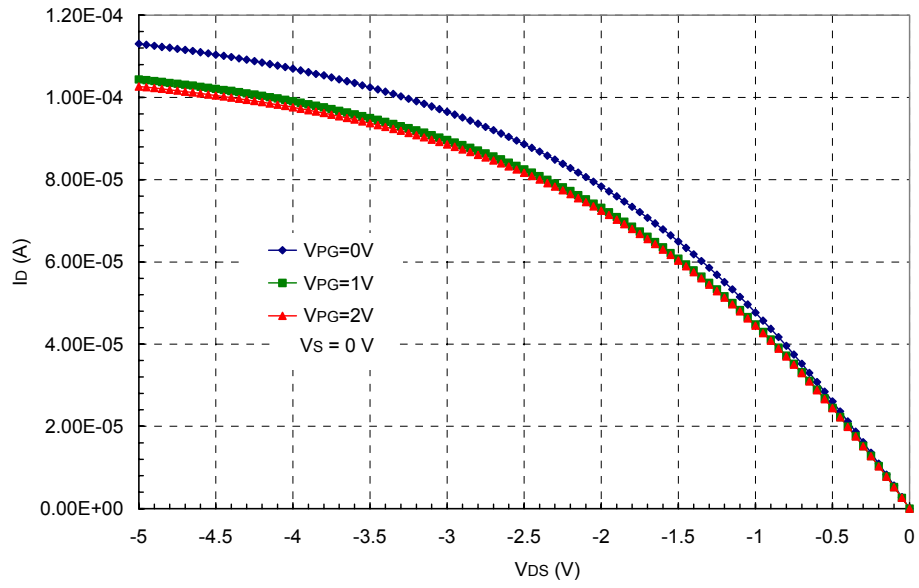


Figure 3-4 V_{DS} vs. I_D for a P-channel G^4 -FET (0.4 μ m/0.9 μ m)

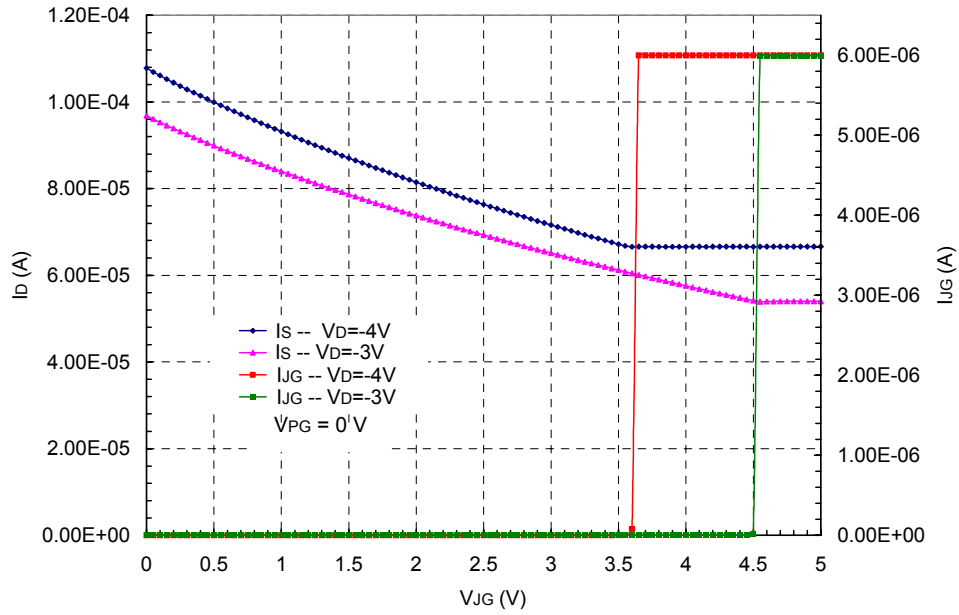


Figure 3-5 I_D vs. V_{JG} and I_{JG} vs. V_{JG} for a P-channel G^4 -FET (0.4 μ m/0.9 μ m)

3.2 Temperature Behavior of G⁴-FET Pinch-off Voltage Difference

The motivation of using the JFET reference circuit is to obtain an output with constant TC at different temperatures, as seen in Section 2.1.3. The G⁴-FET is uniquely different from the JFET device in that it has two MOS gates, the top gate and the back gate, both of which have the capability of modulating the conduction channel. Whether or not the G⁴-FET device can substitute JFET device to generate a constant TC voltage within a reference circuit is of interest.

The temperature behavior of the G⁴-FET device is analyzed based on the G⁴-FET saturation model [15]. According to the state of operation of the G⁴-FET device at which the model is extracted, the model can be used to predict the G⁴-FET device saturation operation with the top gate and the junction gate depleted, and the back gate neutralized, being biased at 0 V.

3.2.1 G⁴-FET Pinch-off Voltage Difference versus Temperature

The pinch-off voltage of the G⁴-FET device can be written as [15]

$$V_P = W \cdot (E_{Pjg} + \varphi_{vp} (V_{g1} - k_{vp})^2 + E_{Pg1}) \quad (3.1)$$

where

E_{Pjg} = effective pinch-off field for the junction gates,

φ_{vp} = fit parameter for pinch-off,

k_{vp} = fitting constant pinch off,

E_{Pg1} = effective pinch-off field for top gate, and

W = is the channel width of the device.

For two equally sized G⁴-FET devices, E_{Pjg} and E_{Pg1} are constants independent of temperature. Their pinch-off voltage difference can be expressed as

$$\Delta V_P = \{W[E_{Pjg} + \varphi_{vp} (V_{g1} - k_{vp})^2 + E_{Pg1}]\}_2 - \{W[E_{Pjg} + \varphi_{vp} (V_{g1} - k_{vp})^2 + E_{Pg1}]\}_1 \quad (3.2)$$

$$= W(\varphi_{vp} \cdot C_1 + C_2) \quad (3.3)$$

where $C_1 = (V_{g1} - k_{vp})^2$, and

$$C_2 = [(E_{Pjg})_2 - (E_{Pjg})_1] + [(E_{Pg1})_2 - (E_{Pg1})_1].$$

Both terms C_1 and C_2 are independent of changes of temperature. The parameter φ_{vp} can be written in the similar form as (2.12)

$$\varphi_{vp} = A \cdot (kT/q) \ln(N_A N_D / n_i^2). \quad (3.4)$$

Substituting (3.4) into (3.3) yields

$$\Delta V_p = W \left(C_1 \cdot A \cdot (kT/q) \cdot \ln(N_A N_D / n_i^2) + C_2 \right). \quad (3.5)$$

Because the intrinsic carrier density of silicon, n_i , is non-linear with temperature, the TC of the voltage reference will not be constant. In addition, observe the derivative of ΔV_p is positive. This indicates the pinch-off voltage difference of two G^4 -FET devices would increase as the temperature goes up, showing an opposite trend compared to that of JFET voltage reference. However, given that the G^4 -FET model is still in its early development phase, additional experimental work is needed to verify this analysis.

3.2.2 Alternative Back Gate Bias

As discussed above, when the back gate of the G^4 -FET device is biased neutrally, at 0 V, the theoretical TC of the output is not constant. To potentially achieve a better TC at the output, back gate bias effects need to be explored, since this is not currently included in the G^4 -FET saturation model.

Comparing the JFET device with the G^4 -FET device, the difference is the two additional MOS gates. Applying a positive bias at the top gate will accumulate the top channel, while a negative bias will deplete the top channel. The same is true for back gate biasing. To achieve a more JFET-like behavior, depleting the top gate and the back gate with a negative bias is preferred so that the conduction is in the middle of the channel and away from the MOS gates. This is sometimes called “volume conduction mode” [16].

Due to the immaturity of the G^4 -FET model, exploration of an alternative back gate bias to achieve constant TC should be made based on experiments. Because the level of negative back gate bias needs to be decided iteratively on an operating G^4 -FET reference circuit, relevant experiments and results will be presented in the next chapter.

3.3 Design of the G^4 -FET Reference Circuit

3.3.1 Schematic of the G^4 -FET Reference Circuit

Figure 3-6 shows the main part of the G^4 -FET reference circuit, inspired by the “Brokaw Cell” [17]. The core of the circuit is a source-coupled G^4 -FET differential pair with its drains connecting separately to the inverting and non-inverting input terminals of an opamp. The tail

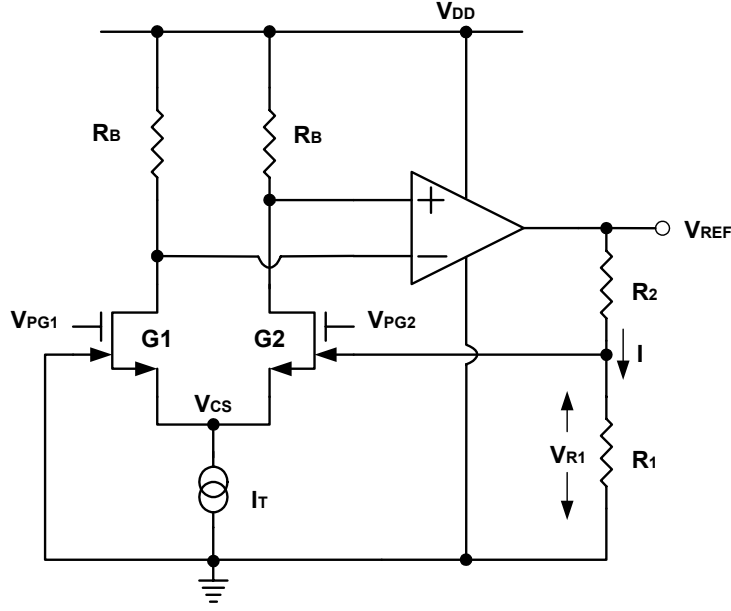


Figure 3-6 G^4 -FET Reference Circuit

current (I_T) and the resistors (R_B) establish the quiescent current, and the negative feedback established by the opamp forces I_T to split evenly between the G^4 -FETs. The circuit uses a single-rail power supply. Assume the two G^4 -FETs, G_1 and G_2 , are perfectly matched. Their drains are connected to the opamp, thereby fixing them to the same voltage. With equal size resistors, R_B , the currents flowing into both legs are equal. The current of each leg is a half of the tail current, I_T . Both G^4 -FETs top gates are depleted to operate in JFET-mode in the saturation region ($V_{DS} > V_{DS,SAT}$, set by R_B and I_T). With the G^4 -FET saturation model formed from the first-order JFET theory, the saturation current can be expressed by the equation below [15]:

$$I_D = I_{DSS} (1 - V_{GS} / V_P)^2. \quad (3.6)$$

The voltage across the resistor R_I is

$$\begin{aligned} V_{R1} &= V_{GS1} - V_{GS2} = \left(V_P - V_P \cdot \sqrt{\frac{I_D}{I_{DSS}}} \right)_1 - \left(V_P - V_P \cdot \sqrt{\frac{I_D}{I_{DSS}}} \right)_2 \\ &= V_{P1} - V_{P2} - V_{P1} \sqrt{\frac{I_D}{I_{DSS1}}} + V_{P2} \sqrt{\frac{I_D}{I_{DSS2}}}. \end{aligned} \quad (3.7)$$

The saturation current I_{DSS} can be written as

$$I_{DSS} = (W/L) \cdot \beta \cdot (V_p)^2 \quad (3.8)$$

where W is channel width, L is channel length and β is the transconductance parameter.

Substituting (3.6) into (3.10), the voltage V_{R1} can be written as:

$$\begin{aligned} V_{R1} &= V_{P1} - V_{P2} - V_{P1} \cdot \sqrt{\frac{I_D}{(W/L) \cdot \beta \cdot (V_{P1})^2}} + V_{P2} \cdot \sqrt{\frac{I_D}{(W/L) \cdot \beta \cdot (V_{P2})^2}} \\ &= V_{P1} - V_{P2} - \sqrt{\frac{I_D}{(W/L) \cdot \beta_1}} + \sqrt{\frac{I_D}{(W/L) \cdot \beta_2}} \\ &= V_{P1} - V_{P2} + \sqrt{\frac{I_D}{(W/L)}} \cdot \left(\sqrt{\frac{1}{\beta_2}} - \sqrt{\frac{1}{\beta_1}} \right) \\ &= \Delta V_p + C \end{aligned} \quad (3.9)$$

where C is the combined term consisting of constants independent of temperature changes.

Then the output voltage of this reference circuit is simply

$$V_{REF} = (1 + R2/R1) \cdot (\Delta V_p + C). \quad (3.10)$$

It is worth noticing that the two G⁴-FETs are depletion-mode devices, thus the current start to flow whenever the circuit is powered on. This indicates the G⁴-FET voltage reference does not require any start up circuits.

3.3.2 Circuit Design Process

With the G⁴-FET differential pair being the core of the reference circuit, the design effort focuses on properly biasing the devices to operate in JFET mode and to achieve a pinch-off voltage difference for circuit output. In this work, the design is based on device characterization results. After multiple experiments, a systematic approach was developed for designing the G⁴-FET reference circuit.

The first step is to determine the top gate bias in order to create a desirable ΔV_p . Then, with the G⁴-FET device biased at saturation region, the appropriate tail current level can be chosen. After these, the rest of the components in the circuit can be decided accordingly.

Table 2 Pinch-off Voltage vs. Top Gate Bias

V_{PG} (V)	$V_{PINCH-OFF}$ (V)
0	-0.36
-0.5	-0.28
-1.0	-0.21
-1.5	-0.20
-2.0	-0.20

3.3.2.1 G^4 -FET Pinch-off Voltage Control Using Top Gate Bias

In order to achieve different pinch-off voltages for the JFETs in Bower's JFET based reference circuit [1], additional process steps are required to alter the doping level of one of the JFETs. Substituting the G^4 -FET devices for the JFET, the pinch-off voltage can be altered by simply adjusting the MOS gate bias. In Figure 3-3, the G^4 -FET device demonstrates different pinch-off voltages under different top gate biases. By establishing a voltage difference across the top gates of two G^4 -FET devices, a desired pinch-off voltage difference (ΔV_P) can be generated.

Table 2 shows the pinch-off voltages under different top gate biases for a single G^4 -FET device. The pinch-off voltage is extracted using the double derivative method [18]. It is observed that the pinch-off voltage changes with the top gate bias until the top gate bias surpasses 1.5 V, where the pinch-off voltage saturates. This suggests for the G^4 -FET differential pair, that biasing one of the top gates to 0 V and the other top gate to -2 V will spread out their pinch-off voltage difference relatively wide. Setting the difference of top gate biases (V_{shift}) more than 2 V is unnecessary in this reference circuit due to previously discussed saturation effect. Applying this top gate bias scheme on the G^4 -FET differential pair with equally sized devices of 3- μ m/2.4- μ m (W/L), a pinch-off voltage difference of roughly 160 mV can be achieved. Additionally, because of the saturation effect, this top gate bias scheme comes with some susceptibility to fluctuations on the V_{shift} .

Figure 3-7 shows a circuit implementation to generate an output voltage that is input voltage shifted down by a defined voltage, V_{shift} . All the resistors are the same size. The output voltage can be found as follows

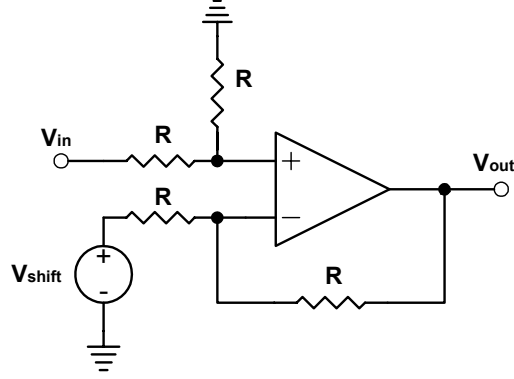


Figure 3-7 Level Shifter Circuit

$$V_+ = \frac{V_{in}}{2}, \quad \text{and} \quad (3.11)$$

$$V_- = \frac{V_{out} + V_{shift}}{2}. \quad (3.12)$$

Since $V_+ = V_-$ due to the negative feedback action, then

$$V_{out} = V_{in} - V_{shift}. \quad (3.13)$$

3.3.2.2 Determining the Tail Current

With the top gate bias determined, the next step is to find the tail current. When the reference circuit is operating properly, the voltage at each G⁴-FET drain and junction gate is fixed. The voltage at the common source node floats to adjust the V_{GS} voltage to accommodate the current. In the design, the proper current level of the G⁴-FET device is found by characterizing the device in the saturation region.

Figure 3-8 graphs the drain current in relation to the junction gate voltage, I_D versus V_{JG} , with different top gate biases. This is similar to the characterization shown in Figure 3-3 except the device is operating in the saturation region by biasing the drain at 3 V. Even though the device is saturated, the drain current is still small due to the small W/L. To avoid forward biasing the junction gate of the G⁴-FET, the drain current needs to be less than 1.5 μA , requiring the tail current to be between 2–3 μA .

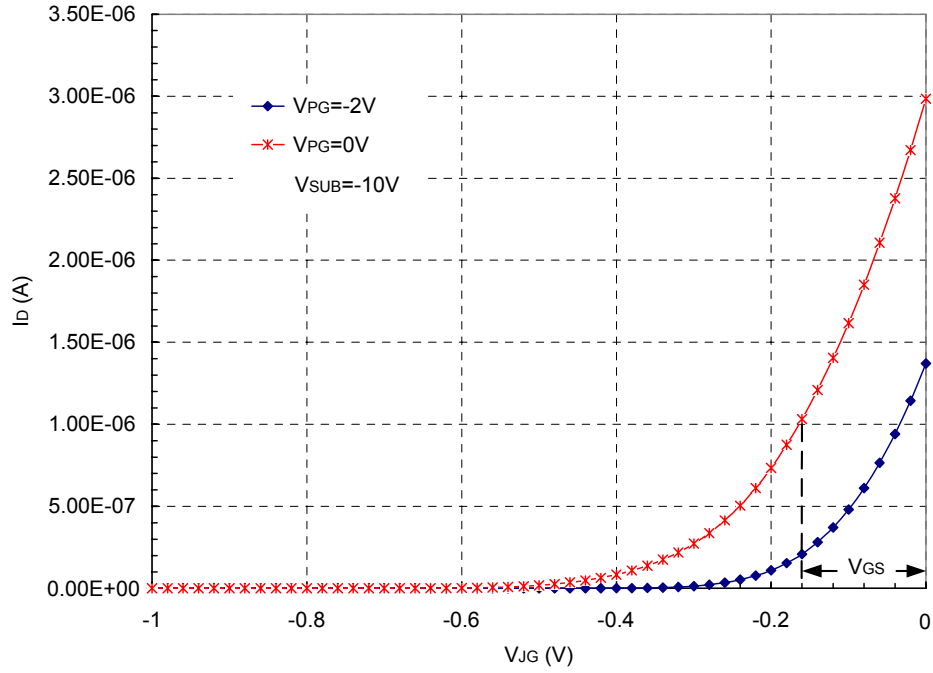


Figure 3-8 I_D vs. V_{JG} for an N-channel G^4 -FET at Saturation Region ($3\ \mu\text{m}/2.4\ \mu\text{m}$)

3.3.2.3 Other Circuit Components

With the tail current selected, the common source voltage, V_{CS} , can be estimated from the saturation current equation, shown in (3.6). To get a more accurate value of the common source voltage, the V_{GS} of G_I can be found using the relationship of I_D and V_{JG} , shown in Figure 3-8. The voltages at the input terminals of the opamp are chosen accordingly for sufficient voltage headroom to keep the G^4 -FET devices saturated. The resistor value of R_B can then be calculated using

$$R_B = \frac{V_{DD} - (V_{CS} + V_{DS})}{\left(\frac{1}{2}\right) \cdot I_S}. \quad (3.14)$$

In order to reduce the number of input terminals of the reference circuit, a single-supply opamp is preferred. By careful design, the main reference circuit and the opamp can share the same power supply. In this circuit, V_{DS} of the G^4 -FET is set to approximately 3–3.5 V to guarantee saturation operation. Choosing V_{DD} to be 6 V, the common-mode input voltage of the

opamp is well within the input common-mode range. With V_{DD} at 6 V, the resistor R_B can be calculated to be about 500 k Ω . To make sure the circuit has a low dropout voltage, a rail-to-rail input/output opamp is chosen.

The voltage at the junction gate of G_2 corresponds to the pinch-off voltage difference, which is about 160 mV. Using equation (3.10), the resistor ratio (R_2/R_1) is set to provide an arbitrary output voltage of approximately 1.8 V.

3.3.3 Circuit Implementation

The schematic of the G^4 -FET reference circuit and the top gate biasing circuit are shown in Figure 3-9 and Figure 3-10, respectively. The part numbers and sizes are labeled on the figures. The purpose of this work is to prove circuit functionality before monolithic implementation. Because the G^4 -FET is a novel and complicated device with immature model support, in the prototype circuit all of the components are discrete parts except for the on-chip G^4 -FET differential pair to allow maximum flexibility. The opamp chosen is the AD8532 [19], an opamp with rail-to-rail input/output range and single supply of 2.7 V–6 V.

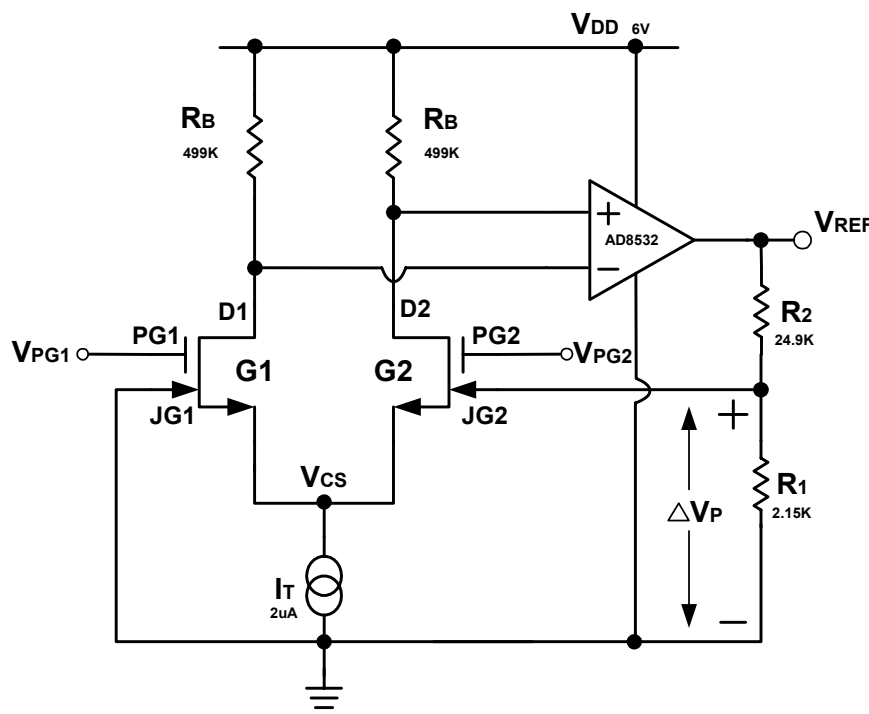


Figure 3-9 Implementation of G^4 -FET Reference Circuit

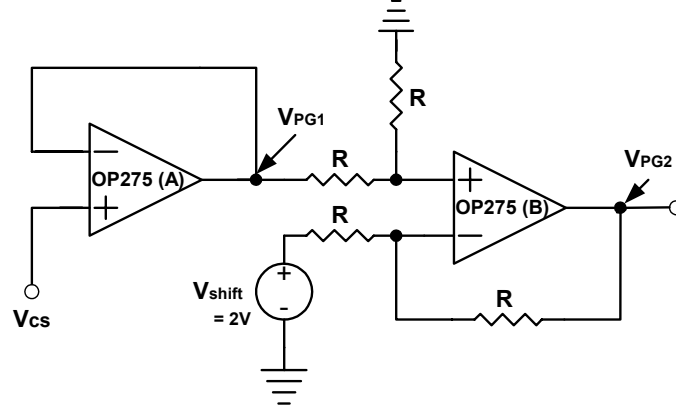


Figure 3-10 Top Gate Biasing Circuit of G^4 -FET Reference

The opamps used in the top gate bias circuit shown in Figure 3-10 are OP275 [20], a dual commercial opamp with JFET input stage. The unity-gain feedback configuration requires the opamp to be unity-gain stable. The top gate bias of G_2 can be negative after the negative shift of 2 V, which requires the opamp to work with complementary supplies. The OP275 operates with dual supplies of ± 15 V.

3.3.4 Frequency Compensation

3.3.4.1 Stability Analysis

In order to evaluate the stability of the G^4 -FET voltage reference, the loop gain was analyzed [21]. As Figure 3-11 shows, the loop gain (T) equals the product of voltage gain and the junction gate to drain voltage gain, times the resistor string (R_1 , R_2) attenuation factor.

Thus,

$$T = -2 \cdot A_{OPAMP_OL} \cdot \left(\frac{R_1}{R_1 + R_2} \right) \cdot \left(\frac{V_B}{V_A} \right), \quad (3.15)$$

where

$$\frac{V_B}{V_A} = \frac{-g_m \cdot R_B}{1 + g_m R_S} = \frac{-g_m \cdot R_B}{1 + g_m \cdot \left(\frac{1}{g_m} \right)} = -g_m R_B / 2. \quad (3.16)$$

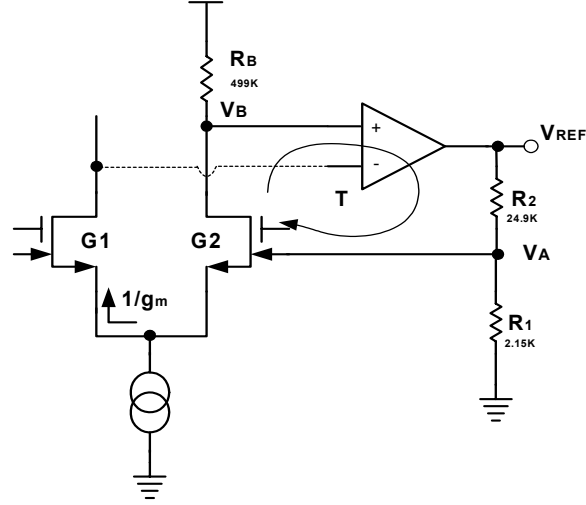


Figure 3-11 Loop Gain Analysis

The junction gate to channel transconductance (g_m) can be estimated from the measurement of I_D versus V_{JG} when the device is biased in saturation region. For the tail current of 2 μA , the transconductance is approximated as

$$g_m \cong \frac{\Delta I_D}{\Delta V_{JG}} = 3.2 \mu A/V. \quad (3.17)$$

The open loop voltage gain of opamp is 25k (V/V), from the AD8532 datasheet [19]. Thus, the loop gain estimate is approximately 3.2k (V/V) at mid-band.

To estimate the pole locations of T , assume a low frequency pole and a high frequency pole. The low frequency pole (f_l) is inside the opamp. Its frequency can be estimated by correlating the gain bandwidth with the open loop gain of the opamp,

$$f_1 = \frac{GBW}{A_{OL}} = \frac{22 \text{ MHz}}{25K} \cong 88 \text{ Hz}. \quad (3.18)$$

The second pole (f_2) at the node V_B affects the stability of the system. The parasitic capacitor at node V_B is sum of the input capacitance of the opamp and the G^4 -FET's drain parasitic capacitance. The total capacitance at node V_B is estimated to be approximately 5 pF. Thus, the frequency of the second pole is

$$f_2 = \frac{1}{2\pi R_B C_{total}} \cong 64 \text{ kHz} . \quad (3.19)$$

Then the loop gain frequency response is

$$T(f) = 3.2K \cdot \frac{1}{\left(1 + jf/88\right)} \cdot \frac{1}{\left(1 + jf/64k\right)} . \quad (3.20)$$

The bode plots of $T(f)$ plotted using MATLAB are shown in Figure 3-12. Note that the phase margin is near 20 degrees. Therefore, in its current form, the circuit is marginally stable.

3.3.4.2 Lag Compensation

To ensure the stability of the reference circuit, some form of compensation is required. In order to maintain the low-frequency loop transmission magnitude, lag compensation is preferred,

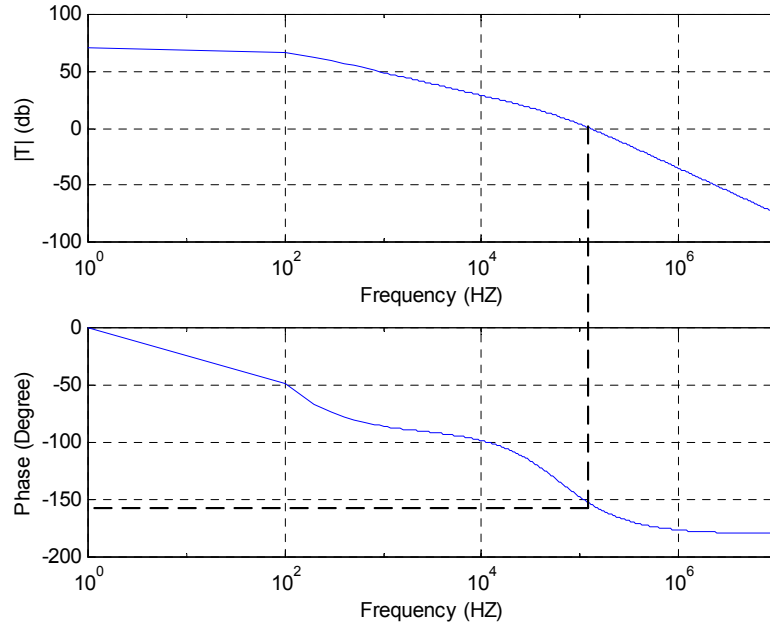


Figure 3-12 Closed-loop Frequency Response of the Un-compensated G^4 -FET Reference Circuit

which incorporates a serially connected resistor and capacitor to create a pole-zero-pole complex to improve the loop gain phase margin.

Of the two major poles, compensation is focused on moving the second pole because the first pole is inside the opamp. A resistor-capacitor is added between the two input terminals of the opamp so that the second pole is shifted to low frequency. A compensation resistor of 22 kΩ and capacitor of 1 μF are selected, as shown in Figure 3-13. A new pole and zero are created, described below:

$$f_p^c = \frac{1}{2\pi \left(R_B \parallel \frac{R_C}{2} \right) \cdot 2C_C} \cong 8.12 \text{ Hz} \quad (3.21)$$

$$f_z^c = \frac{1}{2\pi R_C C_C} \cong 7.23 \text{ Hz} \quad (3.22)$$

With this compensation scheme, the second pole is shifted to very low frequency. The frequencies of the created zero and pole are close, so that they essentially cancel each other. The result is a single pole closed-loop response. Figure 3-14 shows the phase margin is improved to nearly 80°.

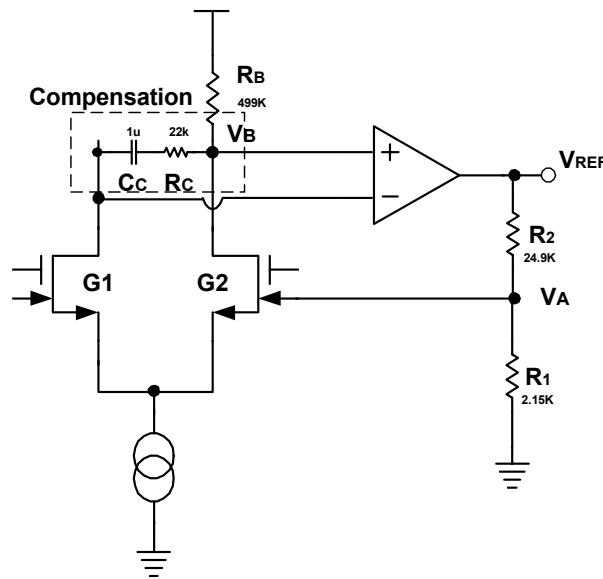


Figure 3-13 Stability Improvement with Lag Compensation

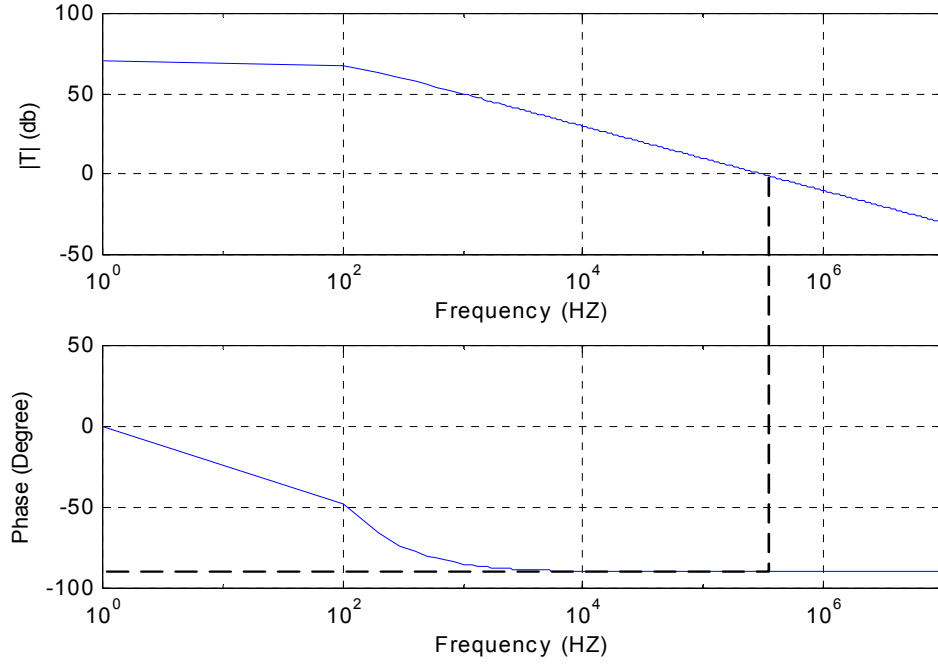


Figure 3-14 Bode Plot of the Compensated G^4 -FET Reference Circuit

3.4 Board Level Implementation

Figure 3-15 shows the backside of the test board for this reference circuit. The test board was built using a copper clad board and “dead bug” technique [22]. The 15-V complementary supplies the top gate biasing circuit and the 6-V supplies the V_{DD} of the core G^4 -FET voltage reference. Capacitors of 10 μ F, 1 μ F, and 0.1 μ F are used in bypassing the supply noise. The 2-V DC shift is also provided off-board using a power supply. The wires on the bottom are connected to the on-chip G^4 -FET differential pair.

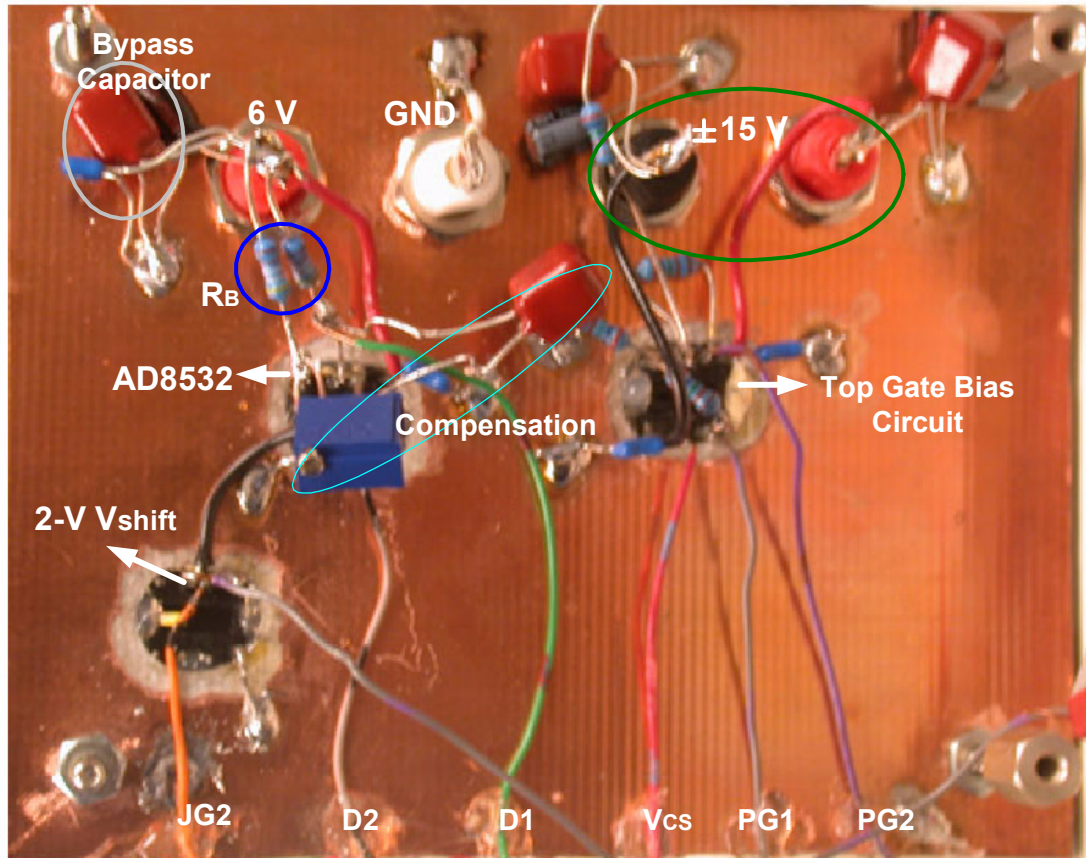


Figure 3-15 G^4 -FET Voltage Reference Test Board

Chapter 4 VOLTAGE REFERENCE TEST AND CHARACTERIZATION G⁴-FET

This chapter presents the testing and characterization of the G⁴-FET voltage reference. The temperature testing is the major part of the testing and is focuses a determining the optimum back gate bias to achieve a constant dV_{OUT}/dT over temperature. The temperature behavior of the reference circuit and its thermal hysteresis are characterized. The end of Section 4.1 discusses the operating temperature range of the circuit. Section 0 shows the *PSR* and noise characterization of this implementation of the reference circuit to help demonstrate the capabilities of this design.

4.1 Temperature Testing

4.1.1 Test Setup

Figure 4-1 shows the basic setup for temperature testing. In order to simplify the testing, only the on-chip G⁴-FET differential pair was inside the temperature chamber, and other circuit components were left outside the chamber. This is appropriate since the G⁴-FET differential pair is the core of the circuit that primarily determines temperature behavior of the reference circuit and serves to predict the potential performance of a fully integrated version. When taking the measurements at different temperatures, a wait period of approximately 20 minutes was used before taking each measurement to allow thermal gradients on the chip to stabilize.

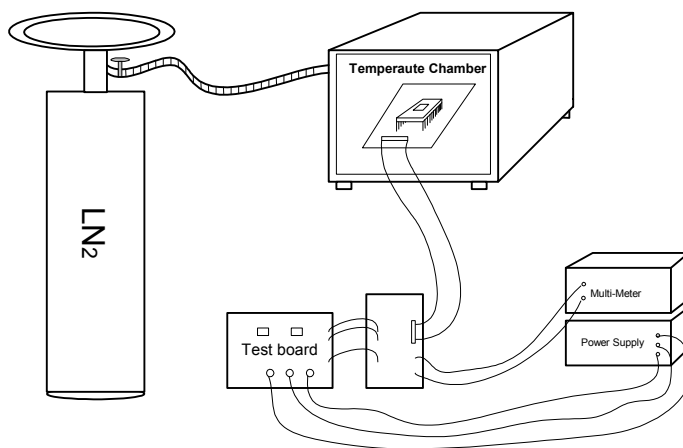


Figure 4-1 Temperature Testing Setup

4.1.2 Back Gate Biases for Constant TC

In this testing, the output voltage from the G^4 -FET reference circuit in the temperature range of -25°C to 75°C was measured. The desired temperature characteristic is a straight line.

As discussed in 3.2.2, a negative bias at the back gate is applied to deplete the back channel to operate the G^4 -FET device more JFET-like manner. Figure 4-2 shows the output from the voltage reference with the back gate bias of 0 V and -6.5 V. Observe the significant non-linearity when the back gate is biased neutrally (0 V), as predicted from the analysis using the G^4 -FET saturation model in Section 3.2.1. With the back gate biased more negatively, the output is much closer to the linear trend-line (dotted line). Also, the output voltage increases with temperature, which matches the analysis in Section 3.2.1.

To further improve the linearity, more negative potential is applied at the back gate to further deplete the back gate. Figure 4-3 shows the linearity is further improved at a back gate bias of -10 V, compared with the back gate bias of -6.5 V. However, the negative back gate bias compromises the operating range of the circuit. Further discussions on this phenomenon are provided in later sections.

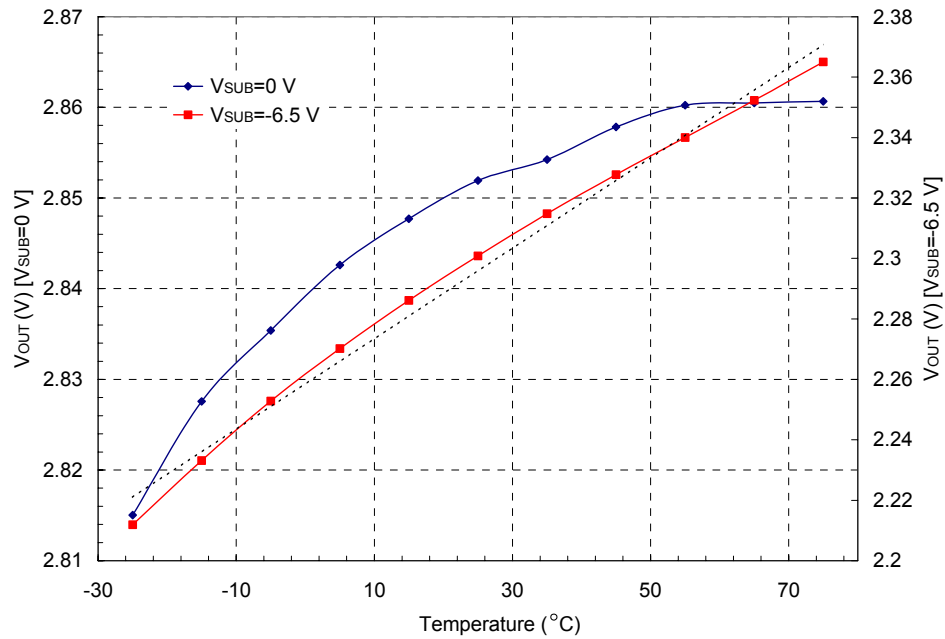


Figure 4-2 Linearity Improvement with Back Gate Bias: $V_{\text{SUB}}=0$ V vs. $V_{\text{SUB}}=-6.5$ V

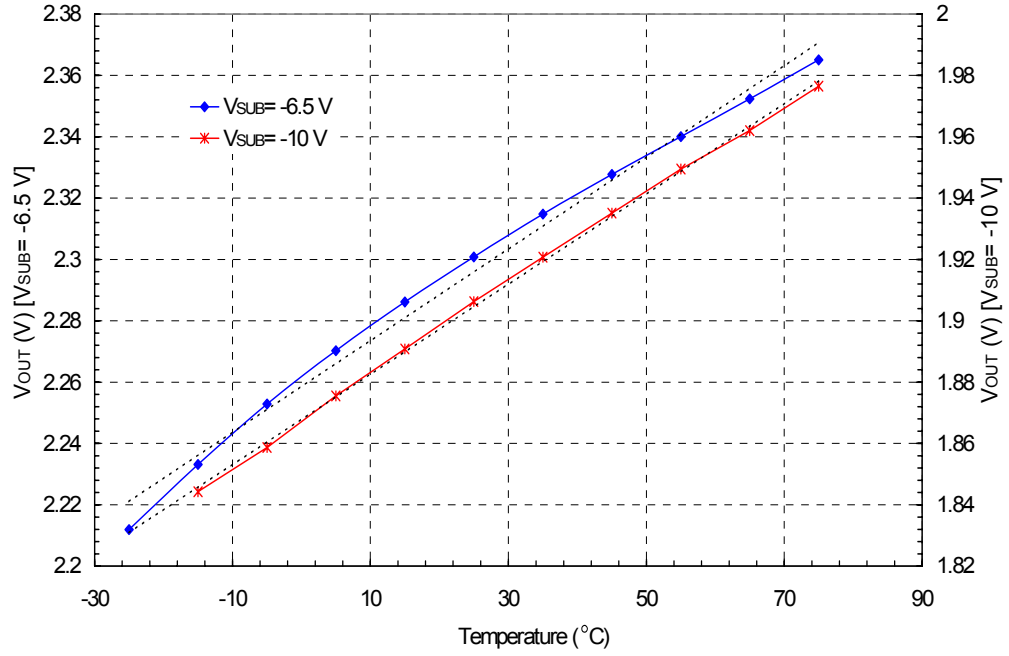


Figure 4-3 Linearity Improvement with Back Gate Bias: $V_{SUB} = -6.5$ V vs. $V_{SUB} = -10$ V

4.1.3 Output Voltage and TC

The G^4 -FET based voltage reference's output was measured over -5 °C to 85 °C with the back gate bias at -10 V. Figure 4-4 shows the output voltage of the G^4 -FET reference circuit with G^4 -FET differential pair from two different chips. Observed the slope (dV_{OUT}/dT) of each output voltage is near constant. Although there is some small voltage shift between the two measurements and slight difference in slope, both output voltage curves display good linearity.

The TC of the output voltage generated by the G^4 -FET voltage reference circuit, in its current state, can be calculated using Equation (1.2). If the output voltage were perfectly linear, the TC at different temperatures would be constant. Figure 4-5 shows the TC derived from the two sets of output voltage data measured above. Noted that the TC curves from two different chips have slight offset due to small mismatches of the absolute output voltage. The variance of TC is within ± 100 ppm/°C in the temperature range of -5 °C to 85 °C and less than ± 50 ppm/°C in the temperature range of 15 °C to 65 °C.

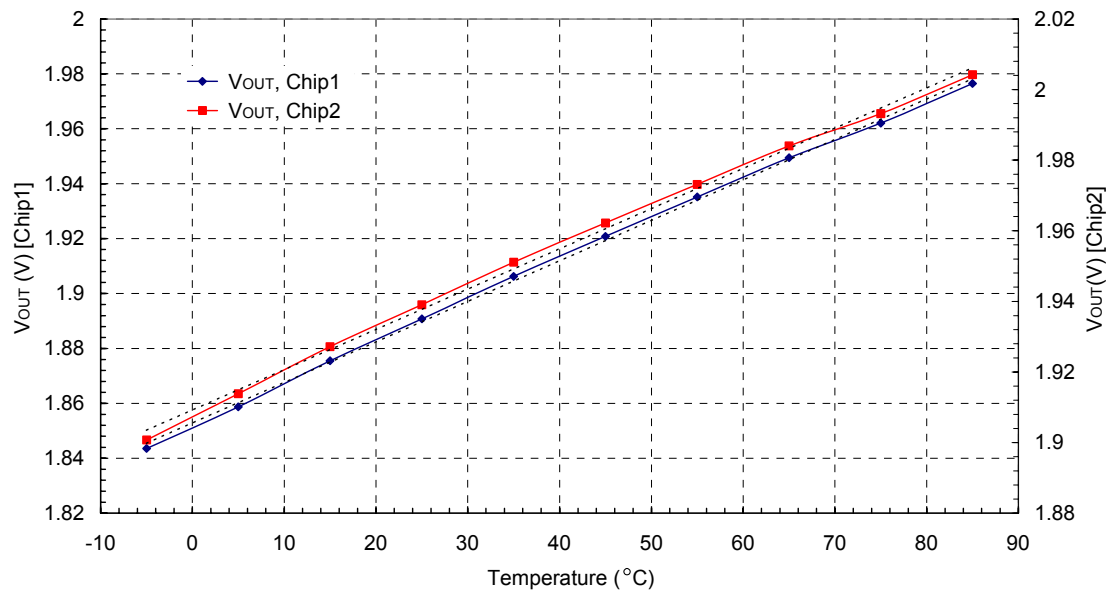


Figure 4-4 Output Voltage of the G^4 -FET Reference Circuit

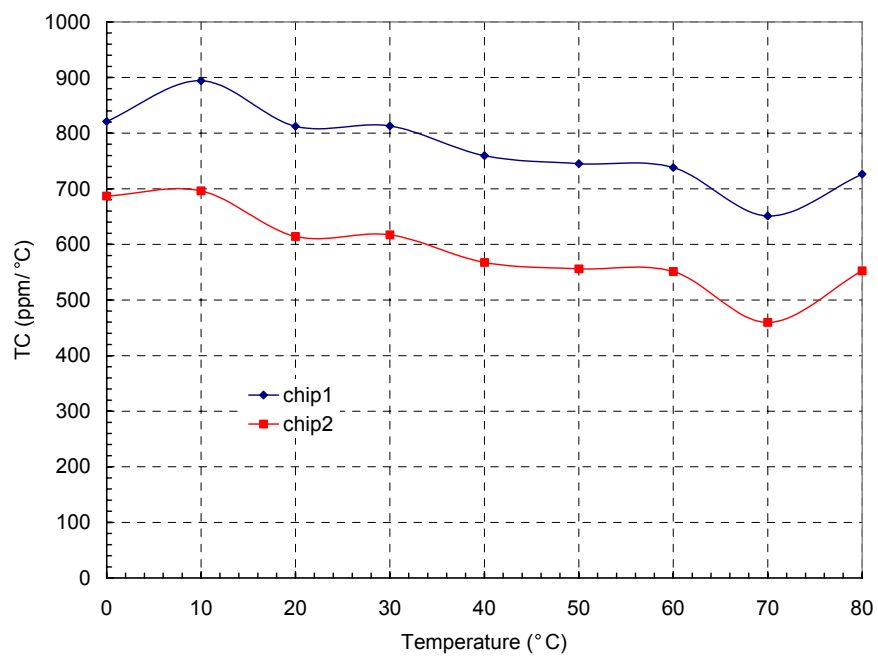


Figure 4-5 TC of the G^4 -FET Reference Circuit

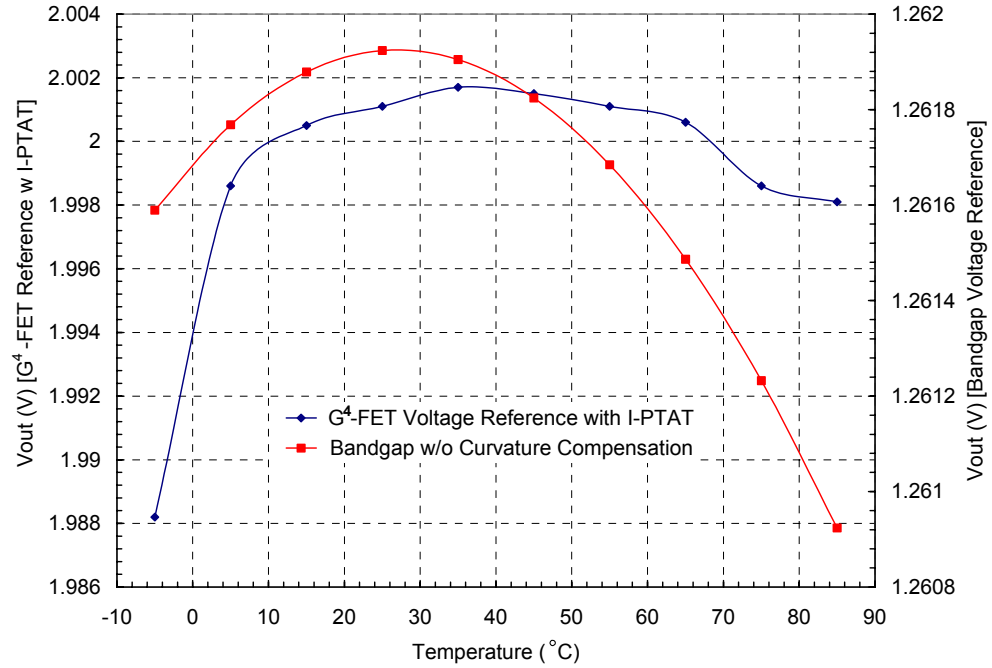


Figure 4-6 Bandgap vs. G4-FET Voltage Reference

Figure 4-6 shows the theoretical TC the current G^4 -FET voltage reference can achieve compared to the TC of a bandgap reference voltage without employing any curvature compensation. It can be seen the output voltage from the G^4 -FET voltage reference does not exhibit as significant rolling off within its operating range, implying a lower TC the G^4 -FET voltage reference can achieve. Suggestions for expanding the operating temperature range are provided in the last chapter.

4.1.4 Thermal Hysteresis

Besides the temperature drift, the thermal hysteresis is another factor impacting the short-term stability of a voltage reference circuit. The phenomenon of thermal hysteresis occurs when the circuit output voltage drifts from an initial value at a given temperature after temperature cycling. The standard method to evaluate thermal hysteresis is to take measurements at room temperature before and after an entire temperature cycle normalized these with the measurement at room temperature. The thermal hysteresis is expressed as:

$$V_{O_HYSTERESIS} = \frac{V_o(25^\circ\text{C}) - V_o(25^\circ\text{C_cycle})}{V_o(25^\circ\text{C})} \times 10^6 \quad (4.1)$$

where

$$V_o(25^\circ\text{C}) = V_o \text{ at } 25^\circ\text{C}, \text{ and}$$

$$V_o(25^\circ\text{C}) = V_o \text{ at } 25^\circ\text{C} \text{ after a temperature cycle.}$$

The output voltage (V_o) measurements were taken at 25°C before and after the temperature cycling from -25°C to 75°C . The thermal hysteresis from six temperature measurements was determined. From these results the mean is 390 ppm and the standard deviation is 180 ppm .

4.1.5 G^4 -FET Reference Circuit Operating Range

With the back gate being bias at -10 V , the output from the G^4 -FET reference circuit shows almost constant output voltage slope (dV_{OUT}/dT) across the temperature. However, there is limitation inherently associated with the circuit. It is known that the pinch-off voltage of the G^4 -FET device changes with temperature. Referring to the linear extrapolation method used to estimate pinch-off voltage in Figure 3-3, the change in pinch-off voltage is due to the shifting of I_D versus V_{JG} characteristic with respect to temperature. Figure 4-7 shows the I_D versus V_{JG} characteristic of one of the G^4 -FET devices in the differential pair, with the top gate biased at either 0 V or -2 V , at a temperature of 27°C and 75°C . Observe that the curves move to the rightward as the temperature decreases. For a fixed drain current, this corresponds to a decreased voltage at the junction gate with respect to the source. To accommodate the drain current with falling temperature, the junction gate voltage will reach zero at a certain point. Further decreasing the temperature will force the junction gate to source voltage to 0 V , or potentially positive to accommodate the current.

For the device to operate properly, forward biasing the junction gate must be avoided. The V_{GS} of either G^4 -FET should not be higher than 0 V . This directly translates to limited range of operating temperature.

In the actual circuit, the current source I_T is replaced with an $n\text{MOS}$ device of a current mirror. To avoid forcing the $n\text{MOS}$ device into linear region, the V_{GS} of the G^4 -FET needs to be even lower than a $V_{DS,SAT}$, which is about 250 mV .

The back gate bias also affects the temperature limitation of the G^4 -FET voltage reference. The more negative voltage applied to the back gate, the lower the drain current flowing

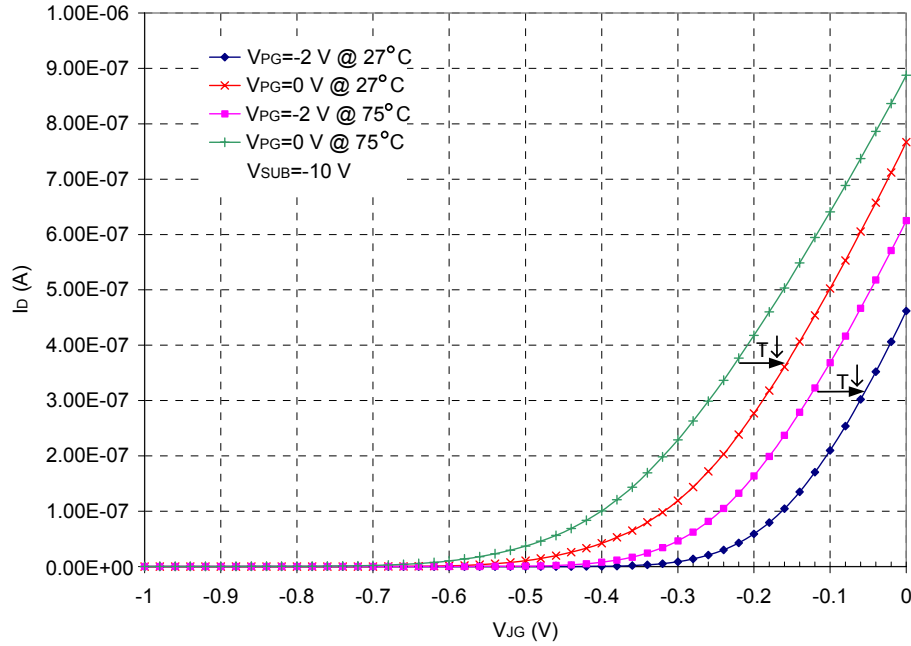


Figure 4-7 Characterization of I_D vs. V_{JG} for an N-Channel G^4 -FET at 27 °C and 75 °C

through the channel. Figure 4-8 shows the I_D versus V_{JG} with different back gate bias conditions. As the back gate bias becomes more negative, the drain current curves are shifted downward. For a fixed drain current, this also corresponds to less negative junction gate voltage with respect to the source. Thus, with the back gate biased at -10 V, the G^4 -FET voltage reference, in its current form, should not be used for temperature below -7 °C.

4.2 Other Testing

4.2.1 Power Supply Rejection

PSR was measured using the SR770 FFT network analyzer and the Agilent 33250 function generator. The function generator can output a sinusoid signal on top of a DC voltage up to 9 V, which is more than sufficient for the V_{DD} of the G^4 -FET reference circuit of 6 V. Thus, the function generator may readily be used to inject a small amplitude (AC) noise onto V_{DD} while powering the G^4 -FET based voltage reference. For a given noise frequency, the output spectrum is measured to determine the PSR using the expression

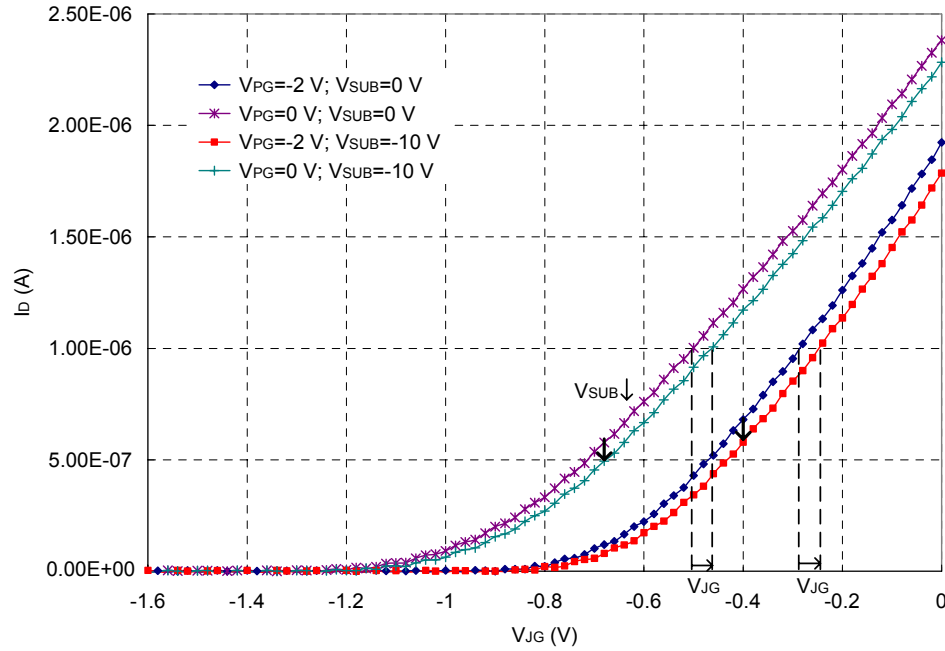


Figure 4-8 Characterization of I_D vs. V_{JG} for an N-Channel G^4 -FET: $V_{SUB} = 0$ V and $V_{SUB} = -10$ V

$$PSR = 20 \cdot \log \frac{\Delta V_{OUT}}{\Delta V_{SUPPLY}}. \quad (4.2)$$

Figure 4-9 shows the PSR at frequencies from 10 Hz to 100k Hz, where the best PSR is near -40 dB and the worst case PSR is above 0 dB. Also observe that the PSR at low frequencies tend to be worse than those at higher frequencies. This characterization shows the PSR of the G^4 -FET voltage reference, in its current form, is not optimistic.

Using an alternate method to estimate PSR may provide insight on improving PSR in this circuit. Noise on the supply rail creates fluctuations at the inputs of the opamp in this circuit, which are propagated to the output. For the opamp, these fluctuations are seen as common-mode voltage signals that would be suppressed by common mode rejection. Consequently, the output fluctuation due to the noise can be estimated by multiplying the noise input voltage by the loop gain divided by the opamp's $CMRR$ (common mode rejection ratio) as following:

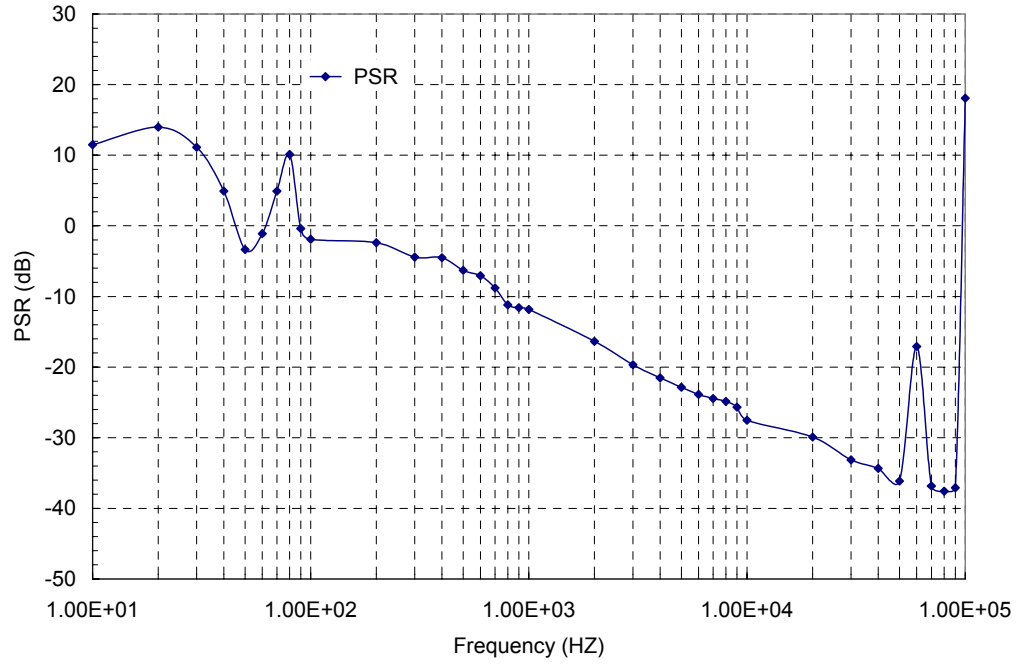


Figure 4-9 PSR of the G⁴-FET Reference Circuit

$$PSR_{EST} \cong 20 \cdot \log \frac{T}{CMRR} \quad [dB]. \quad (4.3)$$

Recall that the loop gain, T , calculated in (3.15), is approximately 3.2k (V/V). Therefore the high loop gain is the main reason that this reference circuit does not have good PSR at low frequencies. As the loop gain magnitude rolls off after the dominant pole frequency of around 100 Hz, the circuit shows better rejection to high frequency supply noise. By lowering the loop gain T one decade, without losing ability of establishing the negative feedback to stabilize the circuit, an improvement of approximately 20 dB on the PSR can be achieved.

To summarize, for the G⁴-FET voltage reference have better PSR , a lower loop gain is preferred. In addition, the $CMRR$ of the opamp has a big impact on the supply noise rejection.

4.2.2 Noise Performance

The output noise from the G⁴-FET reference circuit was measured using the SR770 FFT network analyzer. Figure 4-10 shows the rms noise spectral density at the output in the frequency

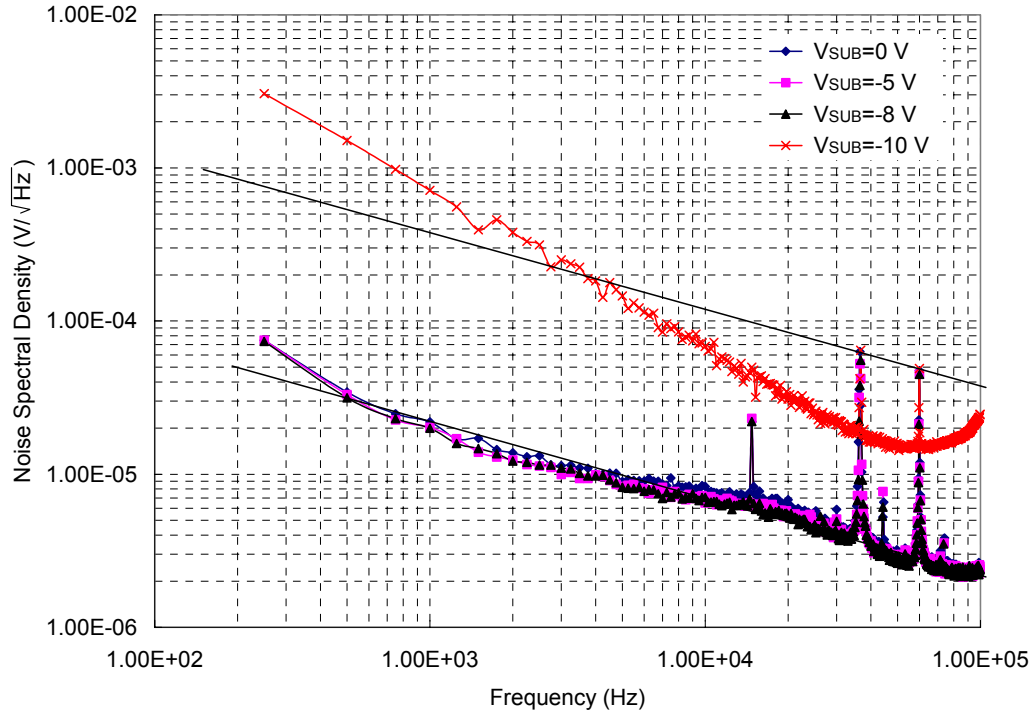


Figure 4-10 Noise Voltage Density of the G⁴-FET Reference Circuit

range of 10 Hz to 100 kHz, with the back gate biased at different voltages (0 V, -5 V, -8 V, and -10 V). It can be observed that the output noise of the G⁴-FET voltage reference is relative high.

Multiple sources of noise contribute to the total noise observed at the output of the reference circuit. From the $1/f$ noise characteristic observed in Figure 4-10, flicker noise from the G⁴-FET devices appears to dominate the output noise. Given the small gate area G⁴-FET devices used in this circuit, some considerable flicker noise is expected. Also, the discrete implementation adds to the output noise. The opamp AD8532 is not a low noise amplifier, and extra noise is also injected at the top gate of each G⁴-FET from the OP275 used in the top gate biasing circuit. To lower the noise from the G⁴-FET voltage reference, larger gate-area G⁴-FETs are required, using higher current and larger g_m , to lower the overall noise from the G⁴-FET devices.

Finally, it is interesting to note that the back gate bias changes the slope of output noise characteristics. With the G⁴-FET device being the major noise source, these measurement results highlight the peculiarities of the G⁴-FET noise characteristic, particularly back gate bias dependent flicker noise slope.

Chapter 5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis investigates the possibilities of implementing an on-chip reference similar to the JFET-based voltage reference but on SoC-compatible technology such as SOI CMOS processes. The JFET-based voltage reference is a new voltage reference providing low TC , good long-term stability, low thermal hysteresis, and low noise. This research is focused on using a novel four-gate transistor, the G^4 -FET, available in PDSOI as a substitute of the JFET device to construct the voltage reference circuit.

In this work, the G^4 -FET voltage reference is designed and implemented with an on-chip G^4 -FET differential pair and supporting discrete circuit components. Optimizing the TC and linearity of the output using different back gate biasing schemes is experimentally demonstrated. The measurements show that with a back gate bias of -10 V, the TC of this voltage reference is near constant at ± 50 ppm/ $^{\circ}\text{C}$ in 15 – 65 $^{\circ}\text{C}$ temperature range.

The measurements of the G^4 -FET based voltage reference also show the G^4 -FET device has numerous differences with the JFET device. The difficulty of achieving a perfectly constant TC compromises the circuit's operating range. The output noise from the circuit is rather high, mainly due to the $1/f$ noise from small gate area G^4 -FET devices. However, there exist ample opportunities for improving the circuit performance. With larger W/L-ratio G^4 -FET devices, the operating range can be improved and the noise performance may be improved significantly.

The G^4 -FET voltage reference demonstrated in this work is the first reported G^4 -FET circuit application. In the development of the reference circuit, it is shown that this four-gate device can create many circuit opportunities. With better understanding of the device and improved device modeling, many exciting circuit opportunities can be created.

5.2 Future Work

5.2.1 Re-Size G^4 -FET Differential Pair

The size of the G^4 -FET devices used in this work is $3\text{-}\mu\text{m}/2.4\text{-}\mu\text{m}$ (W/L), due to limited component availability. With the device biased in JFET-like operation, the saturation current is very low (1 – 1.5 μA). As discussed in 4.1.5, the circuit has limited operating temperature range at cold temperatures. With larger size G^4 -FET devices and higher saturation current, the operating

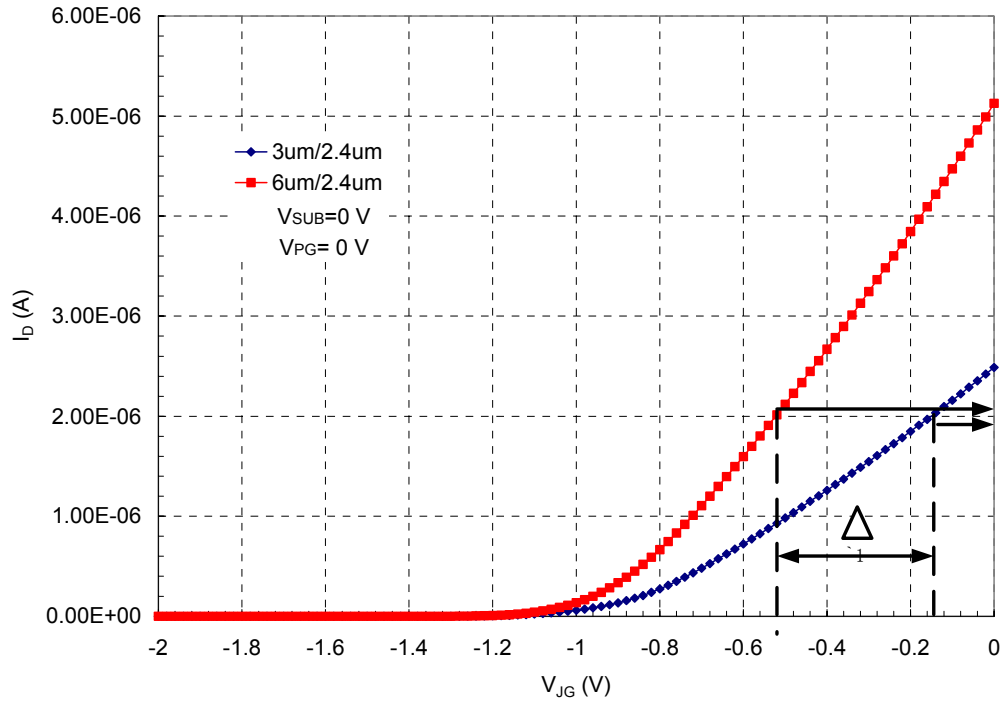


Figure 5-1 Expanded Operating Range with Lager Size G⁴-FET Based on I_D vs. V_{JG} of N-channel G⁴-FET (3 $\mu\text{m}/2.4 \mu\text{m}$ and 6 $\mu\text{m}/2.4 \mu\text{m}$)

temperature range can be expanded. Figure 5-1 shows the I_D versus V_{JG} of G⁴-FET devices of 3- $\mu\text{m}/2.4\text{-}\mu\text{m}$ compared to 6- $\mu\text{m}/2.4\text{-}\mu\text{m}$. With the larger size G⁴-FET there is a broader V_{JG} range below 0 V at a given current compared to the smaller device. Thus more headroom is provided to accommodate colder temperate operation using the larger G⁴-FET. In addition, the output noise performance can be significantly improved using the larger gate area device because the output noise mainly consists of $1/f$ noise, which can be reduced further by increasing the bias current and associated g_m .

Also, with a larger size G⁴-FET differential pair, iterative characterization and measurements similar to those described in this work can determine the size of G⁴-FET devices to achieve better performances (wider operating temperature range, lower TC , and much lower noise) in a fully integrated implementation. Also, with an improved G⁴-FET model having the capability of modeling the back gate behavior, simulations can be employed in the design process instead of solely relying on characterization.

5.2.2 Fully Integrated Implementation

The ultimate goal of this work is to have the G^4 -FET voltage reference as a new on-chip reference circuit for SoC applications. After obtaining more satisfactory measurements with larger size G^4 -FET devices, a fully integrated monolithic G^4 -FET voltage reference is the next step.

The fully integrated implementation requires an inverse-PTAT current to compensate the output from the G^4 -FET voltage reference circuit to generate the final reference voltage. There are other requirements posed on the remaining of circuit components. The opamp in the output stage is required to have low noise and high $CMRR$, with rail-to-rail input/output being an option. To achieve an improved PSR , the loop gain (T) magnitude can be reduced. In addition, the selection of biasing resistor (R_B) needs to be carefully evaluated to ensure the stability of the voltage reference circuit. Again, a better G^4 -FET model would facilitate the design process, especially in the fully integrated implementation.

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Vita

Suheng Chen was born in Fuzhou, China on January 17, 1979. He grew up in Fuzhou and graduated from the Fuzhou No.3 High School in 1997. In the same year, Suheng entered Fuzhou University to pursue a degree in Computer Engineering. His studies were focused on computer architecture and digital design. In July 2001, Suheng completed his undergraduate study with a Bachelor of Science in Computer Engineering.

After completion of his undergraduate study, Suheng began work on the Master of Science in Electrical Engineering degree at Mississippi State University, Starkville. After one year of study, Suheng transferred to the University of Tennessee, Knoxville, and joined the Integrated Circuits & Systems Laboratory under the direction of Dr. Benjamin. J. Blalock. His main responsibility is providing analog and mixed-signal CAD support and physical design/verification.

On Jan 14 2004, Suheng was married to Chunlei Zhang. Upon completion of his master's degree, Suheng will pursue a job in the field of analog and mixed-signal circuit design. Suheng is also a martial-art enthusiast, currently ranks green belt (Yonkyu) in Jujitsu.