A SiGe BiCMOS LVDS Driver for Space-Borne Applications

A Thesis Presented for the

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Degree

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DEDICATION

The following thesis is dedicated to my parents who always supported my childhood dreams of becoming a man of science.

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ABSTRACT

When designing an integrated circuit for use during an interstellar mission, certain precautions must be made. The electronics on any off-earth mission will be exposed to wide temperature swings and harmful radiation due to being outside of the Earth's protective ionosphere. It is crucial that any data path present be immune to these detrimental effects.

The introduction of galactic radiation can not only cause the onboard electronics to fail due to device degradation and single event latchup but can also lead to background radiation being coupled into the signal path as unwanted noise, degrading the signal to noise ratio. Unwanted noise can cause total failure by increasing the noise level thus decreasing the signal to noise ratio below one or by causing errors such as single event upsets.

The wide temperature swing can cause device degradation and eventually failure. This issue is commonly mitigated by the introduction of an environment chamber but such an enclosure adds unnecessary mass and typically requires a large amount of current to effectively keep the electronics in an Earth-like temperature. The large current implies high power dissipation which is an unnecessary strain on the battery and can shorten the lifetime of a mission where every kilowatt-hour is crucial to success.

The solution to these two non-trivial obstacles is to design an electronic circuit such that it can operate in a wide range of temperatures and can withstand the galactic radiation that it will inevitably encounter during its mission's lifetime. The following thesis will document the design, simulation, and testing of a SiGe BiCMOS low voltage differential signal driver for space borne applications.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

Since the beginning of recorded history, communication has played a crucial role in the development of mankind. The necessity to express one's self in a clear and effective manner has helped civilization become what it is today. Without a means to successfully transfer an idea from one person to the next, the world would come to a complete stand-still. This basic concept of transmitting information from one to another permeates every fiber of our modern society. From the smart-phone in one's pocket to the Global Positioning System in one's car, humans are slaves to communication.

The idea of being able to successfully pass information from one person to the next is perfectly analogous to electronic circuits that pass usable signals from one functional block to the next. If one is in an engaging conversation in a quiet room with a peer or coworker and suddenly a loud motor kicks on in the background, one might have trouble discerning one word from the other. The ratio of how loud the person is talking relative to how loud the motor is running can be defined as the signal to noise ratio. If the signal, the voice, becomes too low or the noise, the motor, becomes too high so that the signal to noise ratio approaches one, it becomes next to impossible for the listener to make out any helpful, discernible information transmitted by the speaker.

The concept of the signal to noise ratio is a common analytical method to describe how well a data path can transmit said signal. Unwanted noise can enter the signal path through electromagnetic coupling, also known as electromagnetic interference. This phenomenon can be observed by tuning one's radio to a frequency on which no station is transmitting data. The static hiss that emanates from the speakers is universal background radiation coupling into the signal path of the radio. Another example of the presence of universal background radiation would be to change one's television to an empty channel. The television "snow" is in fact electromagnetic radiation left over from the Big Bang. This background radiation pervades the entire universe and can be seen in the image developed by scientists working on the Wilkinson Microwave Anisotropy Probe project

after nine years of collecting data, Figure 1 [1]. The probe, which was launched in 2001, was designed to detect the temperature differences in the Cosmic Microwave Background radiation when the universe was only a few hundred thousand years old. In order to measure the universe's geometry and evolution, while putting the Big Bang model through its most stringent test to date, the collected data was compiled over nine years and shows an oval shaped image of the universe in an infantile state. This "baby picture" shows a balanced distribution of energy throughout the entirety of existence over several frequency bands from 23 GHz to 94 GHz, thus proving the existence of a universe evenly saturated with cosmic radiation. The background radiation found throughout the universe can lead to the cumulative damage of integrated devices caused by ionizing radiation over time.

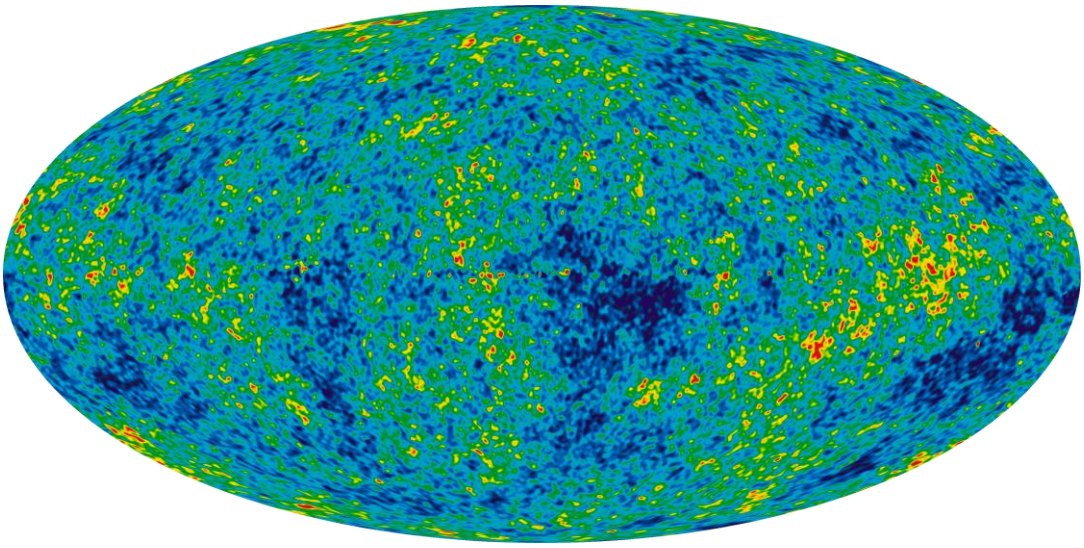


Figure 1 WMAP Image [1]

The universal background cosmic radiation is not the only source of radiation induced errors. Cosmic rays, first discovered in 1912 by Victor Hess, are high energy particles that originate in outer space and travel at speeds close to that of light. The Earth is constantly being bombarded by many forms of galactic rays from all directions. While most cosmic rays are the nuclei of atoms, ranging from Hydrogen to Plutonium, the term also applies to high energy electrons, positrons, and other subatomic particles. It is believed that most galactic cosmic rays obtain their high energy from supernova explosions, one of the most violent and powerful phenomenon known to man. A cosmic ray impacting an integrated circuit can have many detrimental effects on the operation of said circuit including single-event upsets, single-event latchup, and single-event transient among others that can cause errors and device degradation. It is therefore necessary that any electronic circuit, integrated or discrete, be able to withstand these negative effects.

Thus the need for an extreme environment integrated circuit capable of collecting the output of an electronic system and successfully transmitting a clean version of it to a diagnostic tool, e.g. an oscilloscope, came about.

1.2 Thesis Scope and Organization

The primary focus of this thesis is the design, simulation, and testing of an integrated low voltage differential signaling (LVDS) driver in a silicon-germanium manufacturing process. The driver is intended to be used in extreme environments that include wide temperature swings and radiation. The goals of this thesis are to present a viable LVDS design for use in extreme environments and to experimentally verify its functionality and viability.

Chapter 2 will discuss various output driver technologies and radiation and temperature effects, as well as a literature review of some current LVDS architectures. Chapter 3 will provide information about the manufacturing process to fabricate the integrated circuit in addition to the design of the final circuit with simulation results that exhibit a working design. Chapter 4 reveals the results of testing the LVDS driver and

discusses the results. Chapter 5 concludes the thesis and presents recommendations to improve future designs with similar specifications and requirements.

CHAPTER 2: BACKGROUND

2.1 Output Driver Technologies

In an electronic system, there are always inputs and outputs. The inputs, while usually close to an ideal waveform be it square or sine, are typically supplied to the system through a signal generator or possibly an oscillatory crystal reference. The outputs from various mathematical functions, however, are commonly less than ideal and require some form of buffering. There are many types of buffers, both analog and digital, that while performing the same basic task of providing a clean and stable output, vary in their execution of the task. The following sub-sections will discuss common output buffer architectures and their inherent advantages and disadvantages while highlighting the justifications of choosing the low voltage differential signaling circuit topology.

2.1.1 Early Digital Logic

Bipolar transistors were the first three-terminal devices to become available through high-volume manufacturing, leading to one of the earliest forms of digital logic known as resistor-transistor logic or RTL. The simplest form of RTL is the single switch inverter, comprised of an *npn* Bipolar Junction Transistor (BJT) and two resistors, one at the gate and one at the collector, as seen in Figure 2. The main achievement of RTL was being the first generation of digital logic to include a switching device. While an extremely important milestone in electronics history, the technology was quickly replaced by higher-performance circuits due to RTL's relatively large power consumption. Though accomplishing the goal of inverting a signal and providing low output resistance through the use of the collector resistor, the logic gate required significant power dissipation due to the BJT requiring base current to fully turn on [3]. Other drawbacks associated with using RTL include bulkiness, low speed, limited fan-out, and poor noise margin [6]. One of the most important criteria to judge a digital gate on is its noise margin, the measured immunity of a gate to correctly read an input logic

level. With a poor noise margin, the gate becomes unusable in a high performance system.

The next step in the evolution of digital logic was to include diodes into the various logic gates, creating Diode-Transistor Logic (DTL). DTL is an amalgamation of the older Diode Logic (DL) and RTL technologies. Though beneficial in creating simple OR gates, the inclusion of the diode requires an amplifying stage as noted in Figure 3. The amplifying stage is required due to the signal degradation associated with the diode network producing a weak ‘1’. DTL is an improvement over RTL due to the logic being performed by diodes instead of resistors, thus increasing the amount of potential inputs. However, the switching speed is limited due to charge storage in the base of the device after coming out of saturation (switching the output from ‘1’ to ‘0’). DTL offers better noise margins and greater fan-out ability than RTL but it is not an appropriate choice for high-performance designs. The search for a faster and more power efficient logic gate led to many different families of logic, each with their own advantages and drawbacks.

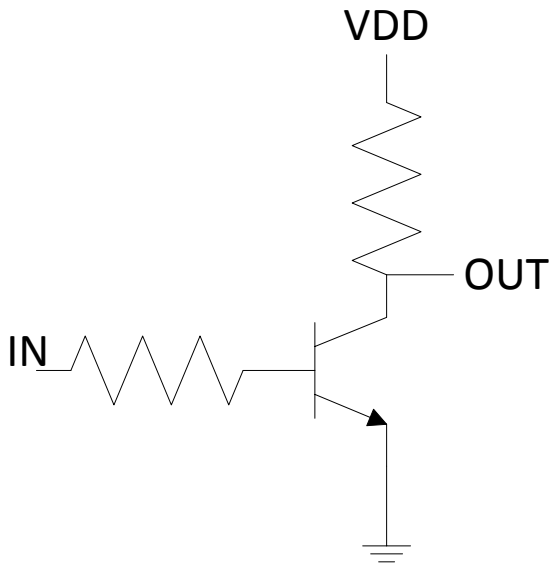


Figure 2 RTL Inverter

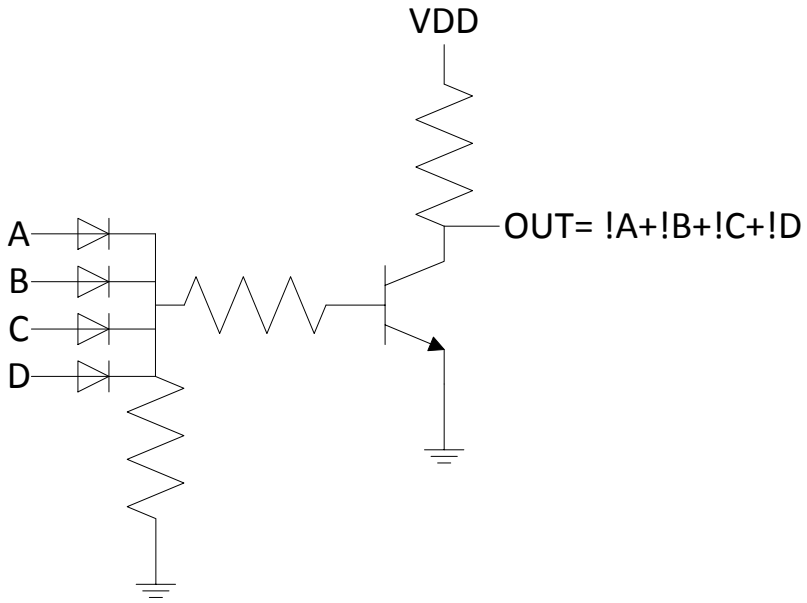


Figure 3 DTL OR Gate

2.1.2 Transistor-Transistor Logic

Transistor-Transistor Logic (TTL) refers to the construction of logic gates through the use of BJTs. The slow speed of older generations of digital logic coupled with the need to build faster, more complex electronic machines to solve everyday problems led to TTL's creation. TTL is very closely related to DTL; in fact if one were to look at a DTL NAND gate, as demonstrated in Figure 4, the opposing diodes at the gate of the amplifying BJT could be replaced with single BJT for each input to accomplish the same job. If the DTL NAND gate was converted to a TTL NAND gate, the circuit would look similar to Figure 5. The chip area saved by removing the bulky diodes is enough to justify the switch from DTL to TTL. This vast improvement over the older DTL technology is the main reason for its lack of use in modern digital electronics. The reduction in area is extremely beneficial but this is not the only improvement brought about by the introduction of TTL. The switching speeds of TTL gates are greatly improved over DTL because of the introduction of a totem pole output circuit to replace the pull-up resistor on the output. The totem pole output stage is greatly responsible for the speed improvement. When the lower switch of the totem pole is turned off, there is a current path for the stored charge to dissipate through, allowing the device to turn off much faster than the output device in an analogous DTL gate. The totem pole output stage not only improves turn-off time but turn-on time as well. The charging of the output capacitance, or load, is done through a diode instead of a resistor so there is a very small RC delay compared to previous technologies. While the speed improvements of TTL over past technologies provide a step forward in the ever changing evolution of electronics, the noise margins inherent in TTL are worse than those found in DTL. Overall, TTL is a worthwhile choice for high-speed applications but not a great choice for high-precision applications such as the one presented in this thesis.

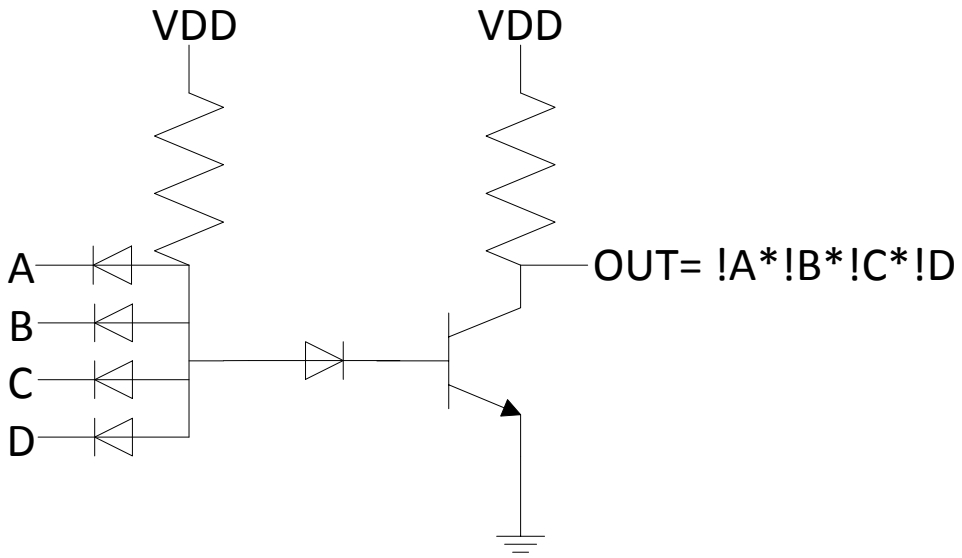


Figure 4 DTL NAND Gate

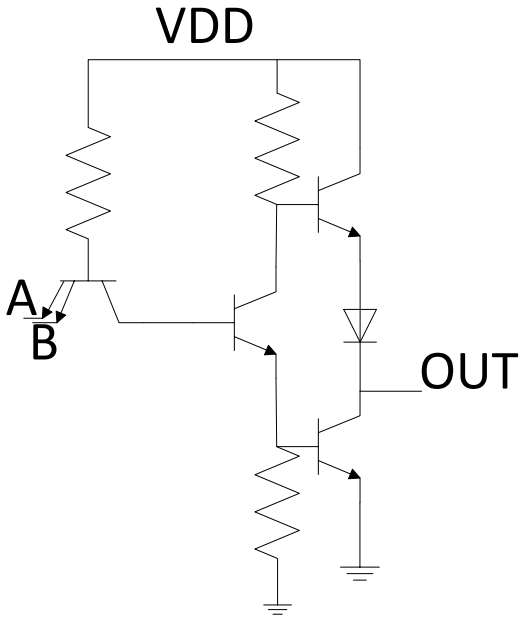


Figure 5 TTL NAND Gate with Totem Pole Output Stage

2.1.3 Emitter-Coupled Logic

As digital logic evolved from DL to DTL to TTL, there was a secondary path being researched that eventually led to the logic family known as Emitter-Coupled Logic (ECL). The most basic element in an ECL gate is the emitter-coupled pair, which the logic family takes its namesake. The emitter-coupled pair, also known as a current switch, consists of two identical BJTs whose emitters are tied to a common current source and are each loaded by identical resistors, Figure 6. The input logic is applied to the base of Q1 and a reference voltage, typically −1.0 V, is applied to the base of Q2. If the logic applied to the base of Q1 is just a few hundred milli-Volts less than the reference voltage, then all of the current supplied by the common current source flows through Q2. On the other hand, if the applied logic signal is only a few hundred milli-Volts greater than the reference voltage, all of the supplied current flows through Q1. Thus the name of current switch becomes apparent due to the emitter-coupled pair switching the current back and forth between two transistors, providing the necessary binary states for digital logic computations. Multiple BJTs can be added in conjunction to the input transistor to create much larger, complex logic gates, Figure 7.

The ECL architecture employs a clever method to improve switching speeds. As discussed earlier in the previous subsection, one reason why the past technologies are not still widely used is their poor switching performance. The current switch transistors operate in the forward-active region with either a relatively large collector current or a very small collector current, close to the cutoff region. By avoiding operation in the saturation region, the charge storage in the base and subsequent charge sweeping never take place leading to an immense improvement in switching performance with speeds approaching single digit nanosecond response times. The improvement in speed is also helped by the relatively small logic swing of ECL, typically ranging from 0.2 V to 0.8 V, which leads to faster load capacitance charging when compared to other logic families. While the backbone of the ECL logic family is the current switch, Figure 6, the fan-out performance needs improvement. To improve the fan-out performance of the technology, an emitter follower is added to the output level shifting the output signal down by one base-emitter drop, typically 0.7 V, and ensuring that the logic levels at the input and

output of the gates are the same. The output resistance of the logic gate is also improved by the addition of the emitter-follower, yielding a low output impedance. This low output impedance allows the logic gate to have a higher fan-out ability and lends itself to driving controlled impedance lines, i.e. a coaxial cable. Since the architecture of ECL is inherently differential (current-switch), the logic family makes ECL perfectly suited for differential applications unlike TTL, DTL, and DL that can only operate in single-ended applications.

Though the attractive increase in switching speeds is very tantalizing for a high speed designer, nothing good comes without a penalty elsewhere. The high performance switching characteristics of ECL come at the cost of a significant increase in power consumption. The total power dissipation of an ECL gate is independent of the current logic state the gate is presently in, due to the current switch never entering the saturation or cutoff regions. The current source tied to the emitter-coupled pair will always force current to flow through one of the devices which in turn will cause current to flow through one of the output stages. The amount of power dissipated will obviously increase with the addition of more devices to provide the necessary drive strength and required complexity.

Positive-reference emitter-coupled logic (PECL) can be considered a child of emitter-coupled logic. The main difference between PECL and ECL is how the logic gates are referenced. In ECL, the logic gates are all supplied the necessary currents from a negative 5.2 V power supply rail, while in PECL, the power supply rail is a positive 5 V. The rise of PECL in digital systems was due to the need of additional negative voltage rails for ECL to interface with any of the current logic families. To avoid the added necessity of extra integrated voltage regulators or off-chip power supplies, the ECL logic family was augmented to work off the same positive power supply as the rest of the electronic systems were currently using. This made interfacing between various logic families simpler while maintaining the wonderful speed performance of ECL. While the incredible speed of this logic family is attractive, it does not bode well for applications where low power operation is a necessity, such as deep space missions.

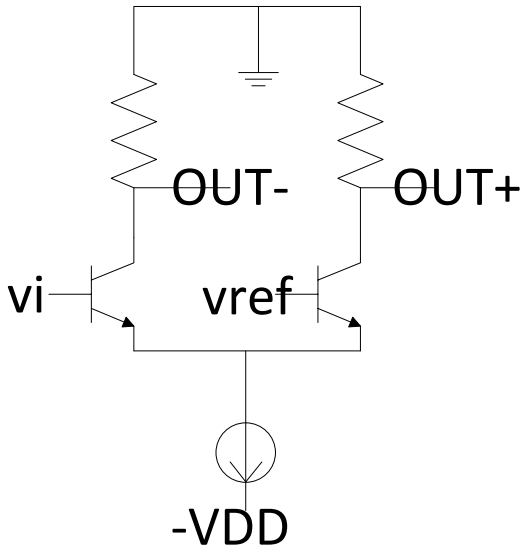


Figure 6 Emitter-Coupled Pair

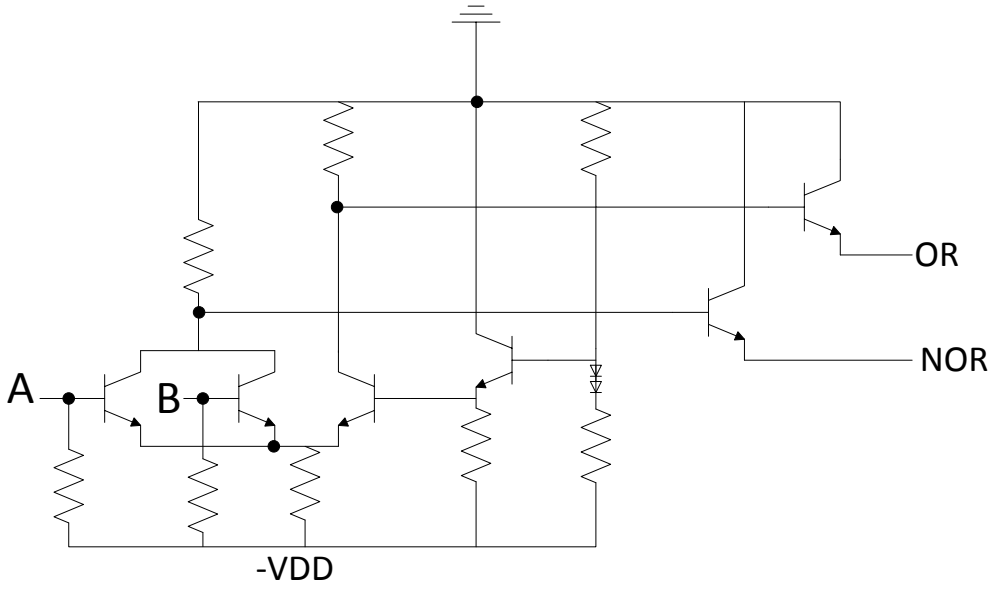


Figure 7 ECL OR-NOR Gate

2.1.4 Complementary Metal-Oxide-Semiconductor

The logic families in the previous sub-sections were mostly constructed out of bipolar junction technologies because the metal-oxide-semiconductor (MOS) manufacturing process to build field effect transistors (FET) was still in its infancy, causing the cost to be much higher when implementing a TTL function in MOS-based logic. As TTL grew in popularity due to its blazing fast switching speeds, chip density, and comparatively low cost, another form of transistors was maturing with leaps and bounds from focused research. The MOS term refers to the physical structure of the field-effect transistors (FET), Figure 8, which is very different from the bipolar structure, Figure 9. The main difference between the MOS and BJT structures is the replacement of the base with a gate. As mentioned previously, the BJT can be viewed as two back to back *pn* junction diodes. The diodes are so close to each other that when the device is properly biased, they couple charge from the emitter through the base and to the collector. Thus, there is always some DC current drawn in through the base. The constant current draw leads to higher power dissipation. The problem of high power dissipation is somewhat mitigated in the MOS structure through the use of an isolated metal gate.

The metal gate rests atop a thin layer of oxide, typically SiO_2 in standard bulk Complementary Metal-Oxide-Semiconductor (CMOS) processes, which then sits above the semiconducting material, Si, revealing the aptly titled name of metal-oxide-semiconductor. As a voltage is applied to the gate and then increased, assuming the drain and source of the device are properly biased, a current will start to flow from drain to source. None of the drain-to-source current however is from the gate; the voltage applied to the gate creates an electric field and by manipulating this electric field, the device can operate in several modes of operation.

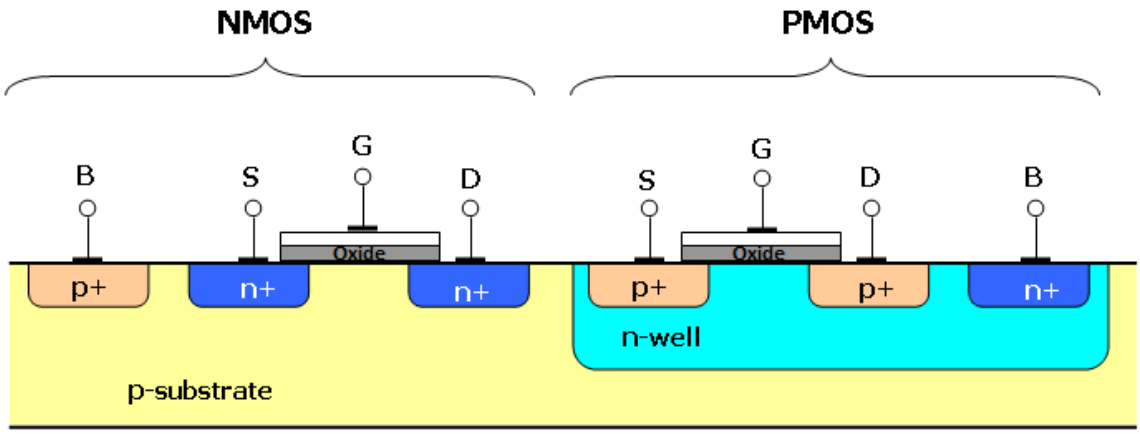


Figure 8 CMOS Structure

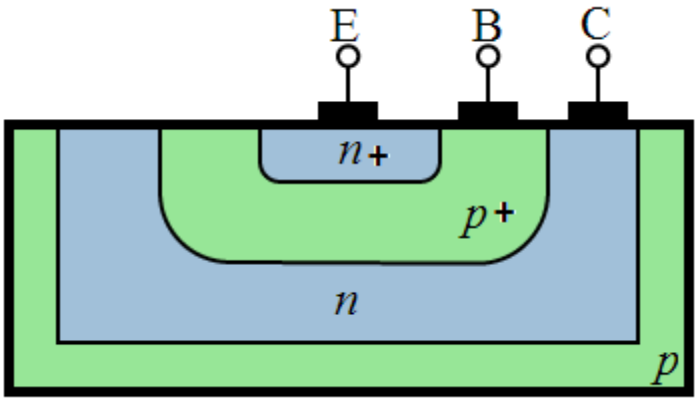


Figure 9 BJT Structure

The three standard modes of operation for a MOSFET are cutoff mode, where the device is not conducting any current, ohmic or linear, where the device acts as a linear resistor, and saturation, where the device acts somewhat like a current source. For digital logic designs, the concerning area of operation is the saturation region where the device is fully turned on and is conducting the maximum amount of current. The amount of current a device can output directly impacts its switching performance, i.e. how fast it can charge the load capacitance. If the load capacitance is very large, the device will take longer to charge the load, leading to slower, less than ideal rise and fall times. The other MOSFET mode of operation one needs to know about for digital design is the cutoff regime. During cutoff, the device is fully turned off and ideally conducts no current. While this is true for larger devices, as the technology continues to scale down below the 50- nm barrier, leakage current becomes an ever increasing problem due to drain-induced-barrier-lowering and gate-induced-drain-leakage [9]. Though these are problems that require engineers to create devices of great ingenuity, the problem of leakage current in short-channel devices is outside the scope of this thesis. The proposed circuit has been developed in a 180-nm long-channel process, which is just outside the short-channel regime.

Due to fabrication-related difficulties during the infancy of MOS technology, *p*-type devices or PMOSFET's were the most prevalent and the first to be commercially available in integrated circuit manufacturing processes [2]. Although NMOS technology was available there were too many issues with the manufacturing process to make it a viable option. This led to nearly a decade of designs relying on only one type of device inherently slower than an NMOSFET because the PMOS utilizes holes to conduct while the NMOS relies on electrons that have greater mobility in the silicon lattice structure. Though the use of only *p*-type devices was certainly not ideal, the manufacturing researchers eventually understood the process associated with manufacturing *n*-type devices enough to start reliably fabricating them in large numbers [2]. The use of NMOS technology rapidly overtook the lower performance PMOS technology and directly translated to higher circuit performance.

The first forms of MOS logic were very power inefficient and as devices started to scale down rapidly with increasingly complex and compact designs being fabricated, power dissipation became an increasingly important issue in Very Large Scale Integration (VLSI). The high power dissipation can be attributed to the pull-up resistor in NMOS logic and the pull-down resistor in PMOS logic. A simple NMOS inverter, Figure 10, utilizes a single resistor in series with a single NMOS. When a HIGH logic signal is applied to the gate of the NMOS, the device begins to conduct and all of the current flows from the drain to the source, bypassing the output node and causing the output to see a LOW logic signal. When a LOW logic signal is applied to the gate of the NMOS, the device will turn off and all of the current will flow through the pull-up resistor and charge the load capacitance, yielding a HIGH output signal. In this set-up, there will always be DC current flowing through the pull-up resistor resulting in constant power dissipation. The PMOS version of this inverter behaves similarly but with the input-output traits reversed. The resistor in the NMOS/PMOS inverter could be replaced with a properly biased device in the ohmic region though this would still require some constant DC current to flow.

The ingenious engineers and researchers, after years of improvements to the manufacturing process, came to the conclusion that in order to yield low-power, high-speed logic circuits the NMOS and PMOS technologies should be combined to form the widely popular CMOS technology. The foundation of the CMOS logic family, the inverter, can be seen in Figure 11. When the input logic signal, which is applied to both the NMOS and PMOS gates, is HIGH, the bottom NMOS leaves the cutoff region and quickly enters the saturation region while the top PMOS enters the cutoff region. This action causes no current to flow through the PMOS and allows the load capacitance to quickly discharge through the NMOS to ground, resulting in a LOW output logic signal. When the input logic signal is switched to LOW, the top PMOS quickly leaves the cutoff region and enters saturation while the bottom NMOS quickly turns off. This induces a drain-to-source current in the PMOS whose only path is into the load capacitance, quickly raising the output logic signal to HIGH.

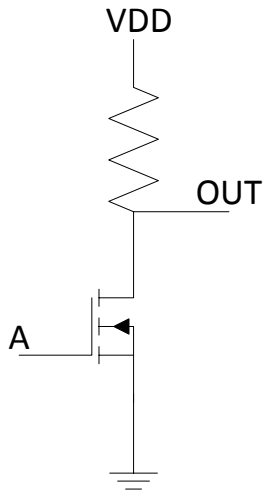


Figure 10 NMOS Logic Inverter

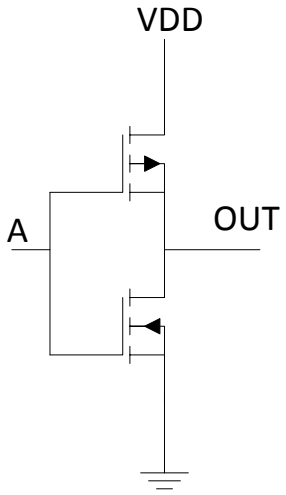


Figure 11 CMOS Inverter

The inherent advantages of CMOS technology are many. One of the most important attributes of the complementary MOS logic family is the lack of charge storage time. As discussed previously, the logic families based on bipolar technology are susceptible to slower speeds due to storage of the minority carriers in the base region and the requirement of sweeping this stored charge out before being able to fully switch off, with the exception of ECL and PECL. The CMOS family is immune to charge storage because of its unique gate-oxide interface, Figure 8, which is drastically different from bipolar devices. The CMOS logic family is also unique in that it has a full rail-to-rail voltage swing at the output, unlike many of the bipolar logic families which have small output voltage swings when compared with their supply rails. The input logic levels are also much higher and wider than the bipolar logic families, making the CMOS family slightly more immune to intermittent voltage spikes and sags which can artificially trigger a false state change. A third and incredibly important achievement of CMOS logic is its very low static power dissipation. In an NMOS-resistor inverter, Figure 10, the very large pull-up resistor is constantly dissipating power regardless of the input logic level. Replacing the resistor with a PMOSFET greatly reduces the power dissipation because the on-resistance of the PMOS is far less than the discrete resistor when the input logic level is LOW. When the input logic signal is HIGH, the PMOS is completely off and no current flows through it. This topology is known as a class AB amplifier or push-pull amplifier because the two devices operate over half of the input waveform. The push-pull buffer is widely used throughout electronics as a popular solution for buffering a signal off-chip.

While the CMOS solution for buffering a signal off-chip looks extremely attractive due to its low static power consumption, large output swing, and fast speeds, it does suffer from some drawbacks. First, the CMOS configuration is a single-ended output. This means that it will be slightly more susceptible to noise coupling into the output unlike ECL whose output is differential. The differential signal helps to reject noise since both signal paths will be affected simultaneously in a common-mode fashion, Figure 12. While CMOS technology has the ability for fast switching speed, the full rail-

to-rail output signal becomes a detriment as the speeds are increased over 100 MHz. As the switching speed is increased closer and closer to the edge of CMOS's abilities, the output signal begins to degrade. The first notable sign of degradation is the rounding of the square wave output signal. When the output buffer is switching rapidly, there is less time to charge the load capacitance fully and eventually the signal will no longer reach the necessary levels to be considered a properly working CMOS buffer. This will be covered in more detail in Chapter 3 when discussing the design of the LVDS driver. So, while the CMOS logic family is widely used throughout the electronics industry and is suitable for many applications, the speed, power, and noise requirements for this work cannot be met with a single-ended push-pull CMOS topology.

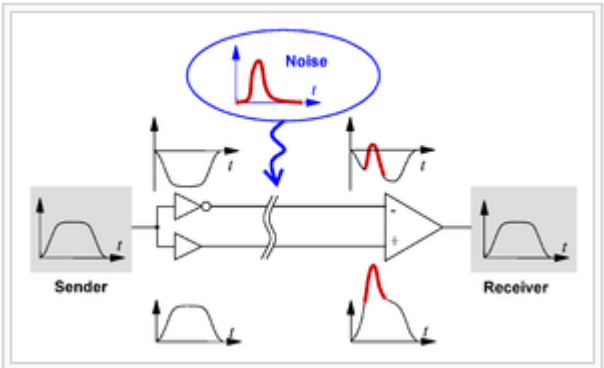


Figure 12 Differential Signal Rejecting Noise

2.1.5 Low Voltage Differential Signaling

The low voltage differential signaling (LVDS) buffer is at its most basic structure considered a switchable current source, much like an ECL structure, Figure 13. The LVDS output structure is optimized for low-power and high-speed operation [7]. The core structure of the LVDS output driver is comprised of two parallel sets of BJT's in series. The top BJT of one leg and the bottom BJT of the other leg have a common gate signal, while the remaining two BJT's have a complimentary gate signal. The input signal to the output buffer is typically a full rail-to-rail signal in order to push the devices into to the saturation region. Where the other logic families' output signal is typically a voltage waveform, the LVDS output buffer's output signal is a current square wave.

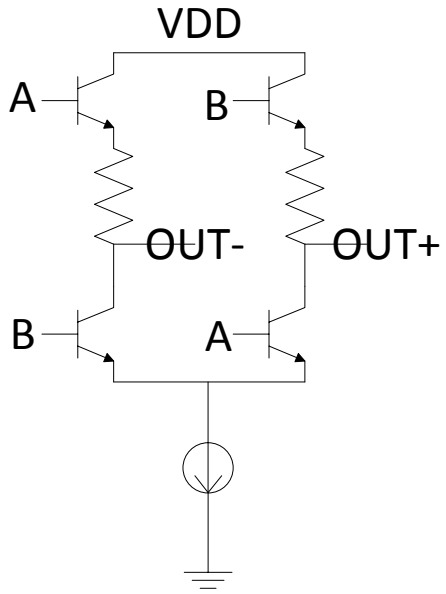


Figure 13 LVDS Core

The proper amount of current, 3.5 mA (per the LVDS standard found in Table 1 [6]), is supplied to the internal switches through the use of a current source. The current source is designed such that it supplies a constant 3.5 mA to the switches and flows through the top switch, out through the connected cable and back through the lower switch. The output impedance of this structure is typically 100 Ω and the output node must be terminated by a resistor of equivalent value [7]. When the 3.5 mA flows through the termination resistor, it creates a ±350 mV voltage signal, depending on which switches are activated. This voltage signal can then be interpreted by a LVDS input structure which will not be discussed since it is outside the scope of this thesis.

The LVDS output buffer structure has several advantages that make it an appropriate choice for the work presented in this thesis. The switchable current source is a rather simple structure and can be implemented fairly compactly on chip. Since it outputs a current signal, the buffer can operate at very fast speeds, outperforming the CMOS push-pull buffer. It not only outperforms the CMOS buffer in speed but in power consumption as well. The faster the CMOS push-pull amplifier switches, the more power is consumed due to its class-AB operation, while the LVDS output structure has a constant power draw over frequency equal to roughly 1.2 mW. Since the buffer is inherently differential, the noise immunity is vastly improved over single-ended solutions and can easily drive long lengths of twisted-pair cables. This feature of LVDS lends itself to be very useful in off-Earth missions where instruments and sensors may be far away from their electronic system interface. The ability to drive signals over long distances is one of the main reasons LVDS became popular in the early 1990's when digital communication systems began to increase in use. A speed versus distance chart comparing popular signaling technologies can be seen in Figure 14 [11]. Figure 15 shows a comparison of the popular signaling technologies output signal levels [17]. It is in Figures 14 and 15 that we can truly see why the LVDS buffer technology is a worthwhile choice for this work.

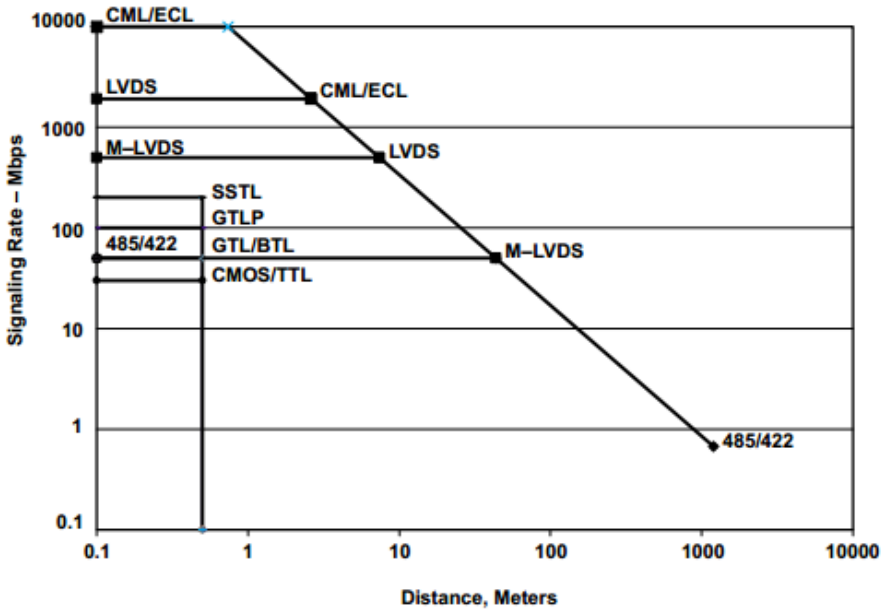


Figure 14 Comparison of Signaling Speeds and Distances [11]

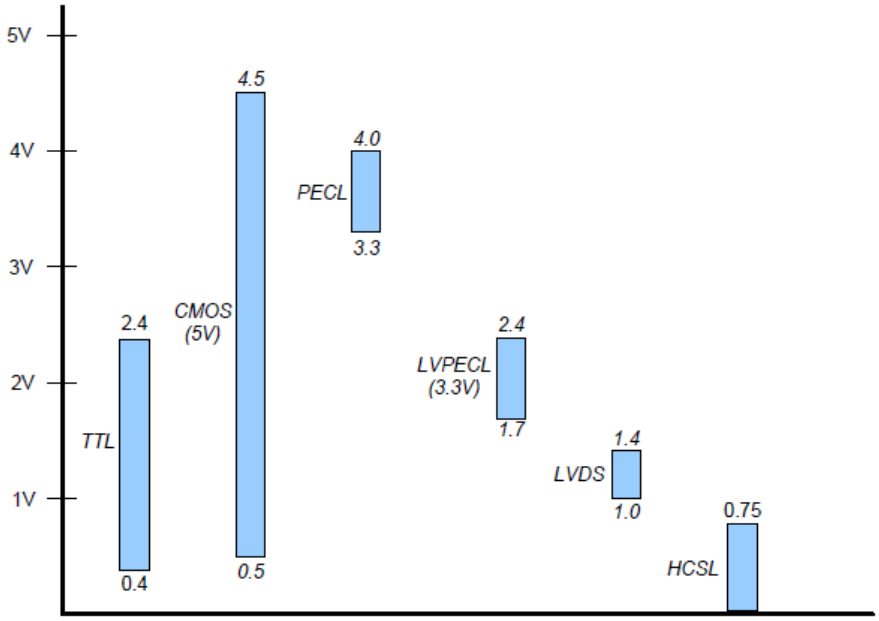


Figure 15 Comparison of Logic Output Voltage Levels [17]

Table 1 LVDS Parameters [6]

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\lvert V_{od} \rvert$		250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\lvert V_{od} \rvert$				25	mV
Offset Output Voltage			1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\lvert V_{os} \rvert$				25	mV
Differential Output Impedance			80		120	Ω
Output Current		Short together			12	mA
Output Current		Short to GND			40	mA
Input Voltage Range	V_i		0		2.4	V
Differential Input Voltage	$\lvert V_{id} \rvert$		100			mV
Input Common-Mode Current		LVDS Input $V_{OS} = 1.2V$		350		µA
Threshold Hysteresis				70		mV
Differential Input Impedance	R_{in}		85	100	115	Ω

2.2 Radiation and Temperature Effects

There are many potential sources of negative effects on electronics. The two most important points of discussion for this work are temperature and radiation. While temperature and radiation effects are not very important for most consumer electronics on Earth, if those same electronics were to leave the protective environment of the Earth's magnetosphere, it would be difficult to discern whether the extreme temperatures or the hazardous radiation caused failure. The protective atmosphere of the Earth not only provides the inhabitants with a somewhat constant temperature but it also protects from harmful cosmic rays and background radiation that is present throughout the universe.

A semiconductor, be it MOSFET or BJT, is made out of some type of semiconducting material. Bulk CMOS processes are typically produced with Silicon but some manufacturing process also use more exotic materials such as Silicon-Germanium. While these are both different types of materials, they are equally at risk for negative effects due to change in temperature. For most designs, assuming a temperature of 300 K (or 27 °C) is adequate but not for electronics that will experience wide temperature swings such as sensors on the Curiosity rover currently on Mars. Any space-borne mission can encounter environments that reach drastically low temperatures like those seen on the dark side of Earth's Moon, −153 °C, or on Venus, 460 °C. While these temperatures are rather extreme, they are points of great interest for scientists interested in the formation of our solar system. It would be incredibly dangerous to send a human explorer to either of these regions so the science community develops robots to visit these alien terrains for us. Designing electronics to operate in these harsh environments is no easy task due to the rapid change in performance of transistors and other electronic components.

As temperature increases in a long-channel MOSFET, the threshold voltage of the device drops by approximately 1 mV/°C [10]. As the device technology is scaled ever downward, the rate of change of the threshold voltage decreases slightly. A BJT will experience a similar effect; its base-emitter voltage required to turn the device on will drop as temperature rises by approximately 2 mV/°C, which is slightly worse than the performance of a MOSFET. This decrease in threshold and base-emitter voltage can

cause total device failure if the ambient temperature the device is operating in raises too high. The device will experience thermal runaway where it cannot be turned off unless power is no longer supplied and will eventual destroy itself. Thermal runaway is defined as an increase in the device's temperature causing more current to flow through the device which in turn heats the device up further causing even more current to flow. This self-reinforcing cycle is potentially hazardous unless a proper mitigation scheme is used. In a typical Silicon manufacturing process the point of failure for transistors is around 125 °C [10].

As temperature increases, other negative effects begin to take hold. One important change is that the mobility of the carriers in the Silicon lattice decreases. The carrier mobility directly determines the transconductance parameters of a MOSFET and the relationship can be seen in the following equations:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-1.5} \text{ and } KP(T) = KP(T_0)\left(\frac{T}{T_0}\right)^{-1.5} \text{ where } KP(T) = \mu(T)C'_{OX} \qquad [10]$$

The decrease in mobility not only affects the transconductance of the device negatively but also causes the drain current to go down [10].While the decreased mobility causes drain current to go down, the decrease in threshold voltage causes the drain current to go up. When the gate-source voltage is low, the changes in threshold voltage dominate and the drain current increases with temperature. However, at higher gate-source voltages, the mobility dominates and the drain current decreases [10]. While electromigration is another issue necessary to mitigate, it has less to do with the transistors' operation and more with the amount of interconnects present in the layout of the circuit. The operation of devices in a cold environment can actually improve the performance of a circuit due to carrier mobility increasing though the threshold voltage of a MOSFET will increase as temperature decreases, though hot carrier effects at cold temperature can compromise device reliability [9]. It is very easy to see that designing a circuit to operate successfully through wide temperature swings is anything but trivial. Designing circuits to operate in a radioactive environment can be even more troublesome.

There are several different types of radiation present in the universe and they are known as gamma rays, X-rays, alpha particles, beta particles, electrons, positrons,

neutrons, and protons [9]. Gamma rays and X-rays are short-wavelength forms of photons or electromagnetic radiation. A gamma ray has its origin in nuclear interaction while an X-ray originates from charged-particle collisions [9]. They both interact with matter the same way in that they are lightly ionizing and highly penetrative but leave no activity in the material being irradiated [9]. Alpha particles are the nuclei of helium atoms that are of high energy, they strongly interact with matter, and are heavily ionizing but they have low penetrative power and travel in straight lines [9]. They are capable of traveling about 23 microns in silicon. Beta particles, electrons, and positrons are small particles that contain a charge and can more easily penetrate materials than alpha particles but are more easily deflected [9]. They have a high velocity, often approaching the speed of light which indicates they are lightly ionizing. Neutrons have the same mass as protons but unlike protons, neutrons contain no charge. They are therefore incredibly difficult to stop but release a gamma ray when they are captured [9]. A proton is considered the nucleus of a hydrogen atom and contains a charge of 1 unit. Its mass is roughly 1800 times that of an electron and consequently drastically hard to deflect [9].

The particles listed above are present throughout the universe but there are a few main sources of radiation in space that could affect electronics. The first is trapped radiation which consists of a very broad spectrum of energetic charged particles trapped in the Earth's magnetic field that forms the radiation belts [9]. Cosmic rays are low fluxes of energetic heavy ions extending to energies beyond the TeV and include all ions in the periodic table [9]. Solar flares are eruptions on stars that produce energetic protons with a smattering of alpha particle, heavy ions, and electrons [9]. Each source of radiation is capable of significantly altering the performance of electronics.

While circuits based off of MOS technology are extremely useful for low-power and high-speed applications, they are rather weak when it comes to radiation performance. Their vulnerability to radiation effects is due mostly to their physical structure. When a NMOS device is being properly operated and a form of radiation strikes the gate-oxide interface, e.g. a heavy proton penetrates the insulating oxide layer, an electron-hole pair will form due to the ionizing radiation. The electron will travel out through the metal gate while the hole is trapped in the oxide. If the device is in a highly

radioactive environment, more and more holes will get trapped in the oxide and will create a positive charge above the silicon. This charge trapping has the effect of shifting the threshold voltage of the device downward towards zero [9]. If the total ionizing dose (TID) is quite large, then the NMOS might not be able to turn off due to the threshold voltage shift even if the gate-source voltage is zero; this is a significant issue in NMOS technology. The issues associated with ionizing radiation are only made worse when in a high ambient temperature, causing the threshold voltage to shift even more negatively. However, if the device is then powered down, annealing effects at high temperature can mitigate TID effects. Modern CMOS processes tend to be somewhat immune to TID-induced threshold voltage shift due to thin gate oxide. Unlike older CMOS processes with thick gate oxide there is very little area for charge trapping in the thin oxide. The primary concern in modern CMOS processes is the TID-induced drain-to-source leakage due to charge trapping along the STI edge. It is therefore extremely necessary to properly design any circuit that might see these extreme environments.

2.3 Literature Review

Several integrated LVDS output buffer topologies have been presented in the literature [11]-[15]. These papers addressed different aspects of designing an integrated LVDS output driver and their operation. However, none of the reviewed items had any design criteria necessary to operate in a harsh environment of wide temperature swings and radiation. While only one paper utilizes a true Bi-CMOS approach, Koo et. al, the rest of the literature is based on bulk CMOS manufacturing processes. Though Koo et. al utilize bipolar technology to accomplish their goals in a 90-nm process, the reasons for utilizing the technology are vastly different from the ones presented in this work. Furthermore, Koo et. al. make no mention of whether their BJT devices are of the SiGe flavor and it is therefore assumed they are standard silicon BJT's. They rely on the bipolar switches in order to obtain higher ESD protection while maintaining a small feature size [11]. Three of the five papers reviewed with the exceptions of Gupta et. al and Koo et. al are manufactured in a 180-nm CMOS process; Gupta et. al manufactured their device in a 0.8-µm CMOS process. Each of the papers reviewed presents a similar

solution to the low-power, high-speed challenge as the one presented in this work. While the maximum output frequency of each reviewed circuit is different, they are all capable of attaining the required speeds of the presented work. Gupta et. al is the only paper reviewed that mentioned results over temperature though they only show results for the common mode output voltage from −50 °C to 125 °C and do not mention how the LVDS buffer operates over temperature.

CHAPTER 3: METHODOLOGY

3.1 IBM 7WL PDK

The proposed LVDS buffer presented in this work was developed in the IBM 7WL Process Design Kit (PDK). The 7WL PDK is a BiCMOS process that is intended for high-performance applications. This PDK offers 7 layers of metal routing, 1.8-V and 3.3-V CMOS devices as well as Silicon Germanium Heterojunction Bipolar Transistors (HBT's). The 3.3-V CMOS devices along with the SiGe HBT's are used in the LVDS buffer. There are several flavors of HBT's in the PDK that include high breakdown, standard performance, and high performance. Unlike the CMOS devices in this PDK, the HBT's can only be constructed to 11 different emitter sizes. This limits the amount of design decisions that can be made when sizing the HBT's but the CMOS devices can be sized from the minimum gate length and width of 180 nm to > 260 nm, respectively. The PDK has two forms of trench isolation to keep substrate leakage current from affecting neighboring devices (crosstalk) and to improve radiation immunity, Deep Trench Isolation (TI) and Shallow Trench Isolation (STI). Both of these isolation trenches will be used in the final design to improve device performance.

3.2 Circuit Design

The following sub-sections will detail the design decisions associated with creating a LVDS that can withstand the wide temperature swings of space along with preventative methods to improve radiation immunity. The sub-sections will include the first attempted design to validate the workings of the LVDS output driver and will end with a final design that can successfully operate from 80 MHz to 250 MHZ and over the temperature range of −50 °C to 125 °C in a radioactive environment.

3.2.1 Basic Design

The initial design for this work was intended to discover which type of transistor would best suit the needs of this project, i.e. overall switching performance and current drive. The first design was a simple recreation of the switchable current source as seen in Figure 13 except that the NMOS devices were replaced with *npn* HBT's, Figure 16. The choice to switch from MOS to HBT technology came about by studying each device's structure. The *npn* HBT's are much less susceptible to TID through their removal of STI edges and their lack of the gate-oxide interface as mentioned in the previous section. While the initial design shows potential for meeting the requirements of the final design, the HBT's used show poor switching performance and the inability to meet the output voltage of 350 mV across the 100 Ω termination resistor even though they are being supplied with 3.5 mA through use of a current mirror, Figure 17. Though the waveform looks very similar to a working LVDS design, the differential voltage only reaches ±170 mV, only half of what is required per the LVDS standards put forth by the American National Standards Institution (ANSI) and is seen in Table 1. The poor switching performance displayed by the HBT's is attributed to the charge storage in the base when the device is being turned off. This is displayed in the results, Figure 17, where the devices can be seen having difficulty turning off quick enough, causing the differential voltage across the termination resistor to be diminished significantly.

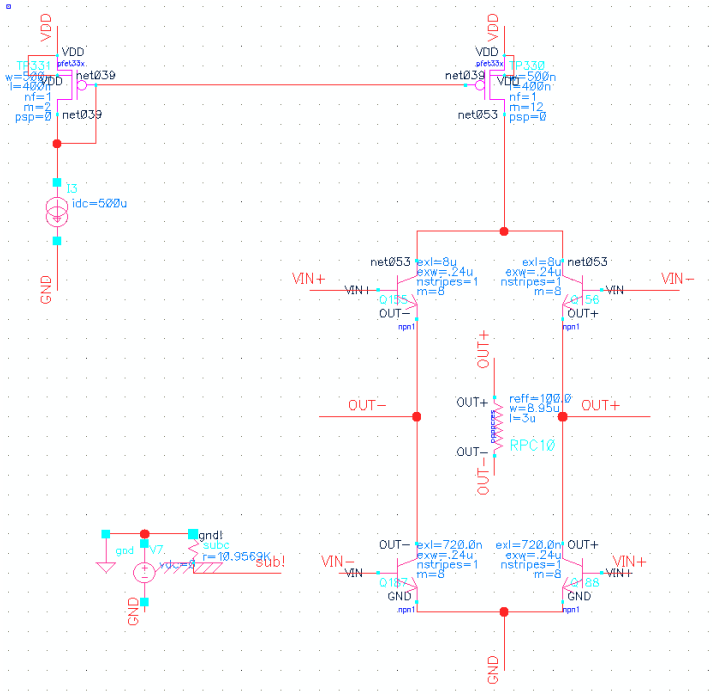
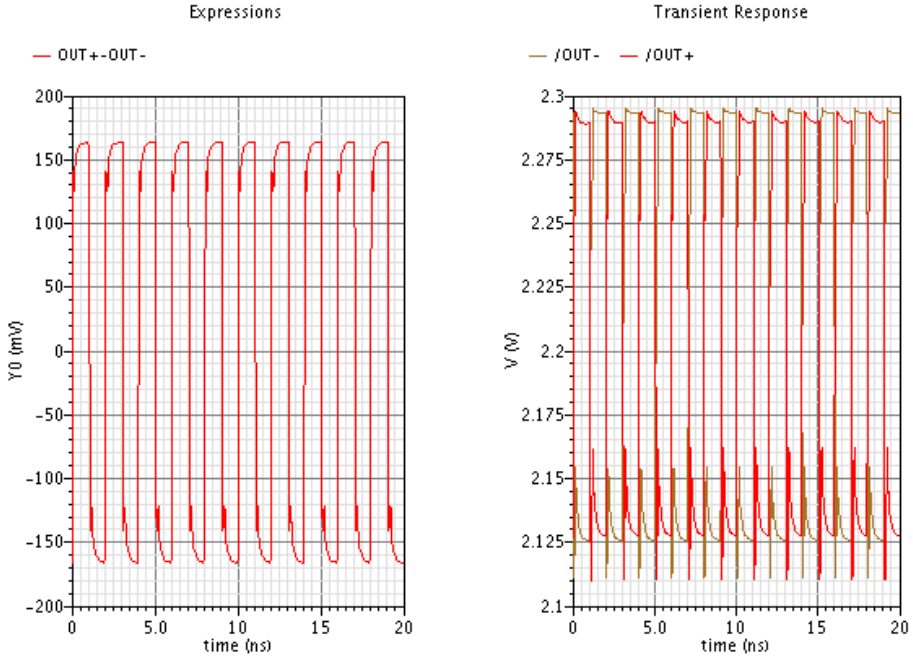


Figure 16 Initial LVDS Buffer Design to Test Functionality



(a) (b)

Figure 17 Basic LVDS Design Simulation Results at 250 MHz: (a) Differential Output (b) Single Ended Output

The initial LVDS buffer design does not meet the differential output voltage specifications but also has difficulty maintaining the common-mode output voltage of 1.25 V necessary to properly interface with an LVDS receiver. Though this is an issue, the intention of the initial design was to provide basic switching functionality and not to meet all of the LVDS standards. The buffer, while not properly functioning, gives great insight into the next steps required to design a working output driver.

The output common-mode voltage can be set through the use of a common-mode feedback (CMFB) circuit, which is a fairly popular and effective method found in the literature. It was therefore chosen to be included in the design in order to meet the LVDS standard operating specifications. The CMFB designed for this work, Figure 18, places two 50 kΩ resistors in parallel with the output nodes to sample the output common-mode voltage. The sampled voltage is then applied as the input to one transistor of a differential pair with the other transistor's input is tied to a reference voltage of 1.25 V. The differential pair then compares the two voltages and if there is a discrepancy, the current flowing through either leg will be adjusted accordingly causing the common-mode output voltage to swing back to 1.25 V. The CMFB is required to be very fast in order to hold a stable output voltage of 1.25 V. The fast speed requirements can cause issues with stability so a compensation network is added into the feedback loop. The compensation network consists of a resistor in series with a capacitor that help to maintain a stable common-mode output voltage, Figure 19. An AC analysis of the CMFB amplifier in Cadence shows that the gain of the amplifier is stable over a wide frequency with a phase margin of approximately 70 degrees, Figure 20. A phase margin of 60 degrees is the ideal value since it results in the fastest settling time, thus a phase margin of 70 degrees is acceptable. The AC analysis was performed using the Spectre tool in the Virtuoso Analog Design Environment window. After performing the AC analysis, the AC magnitude and phase can be plotted by selecting the two nodes needed to calculate these values. In the case of the CMFB amplifier, the two nodes used were the input and output of the differential amplifier, VREF and the drain of the output device. The stability of the CMFB amplifier can be seen in the figures throughout the next several sections. Upon

finding a successful solution to the output common mode voltage issue, the next dynamic issue to be addressed is the switching performance of the LVDS driver.

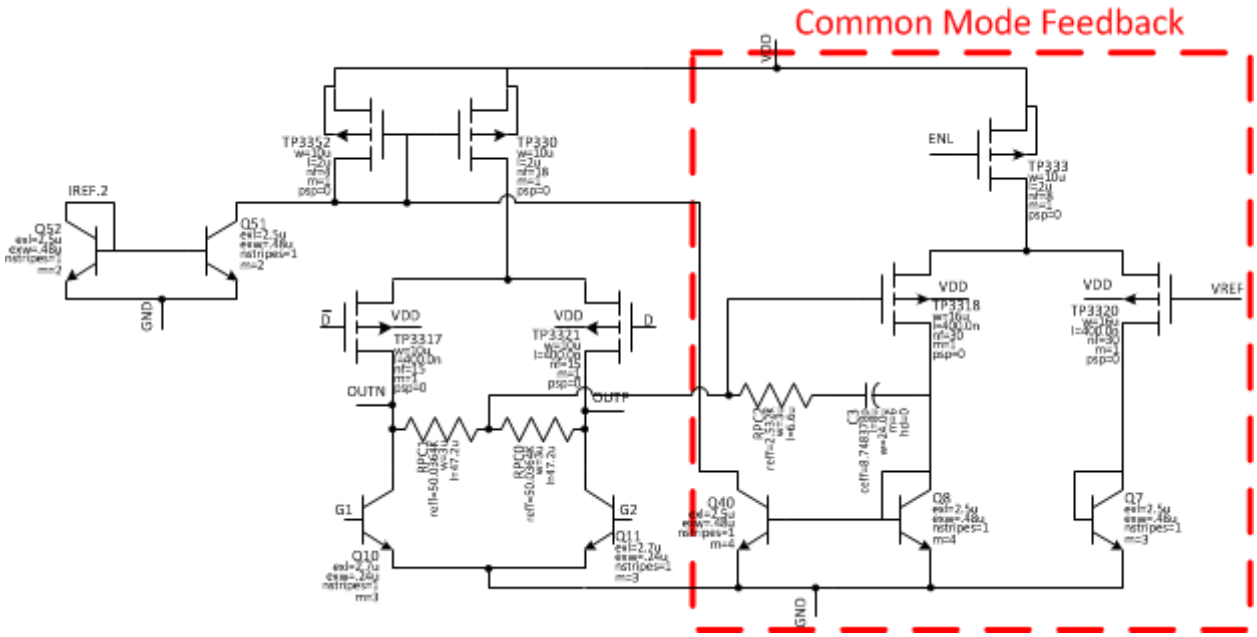
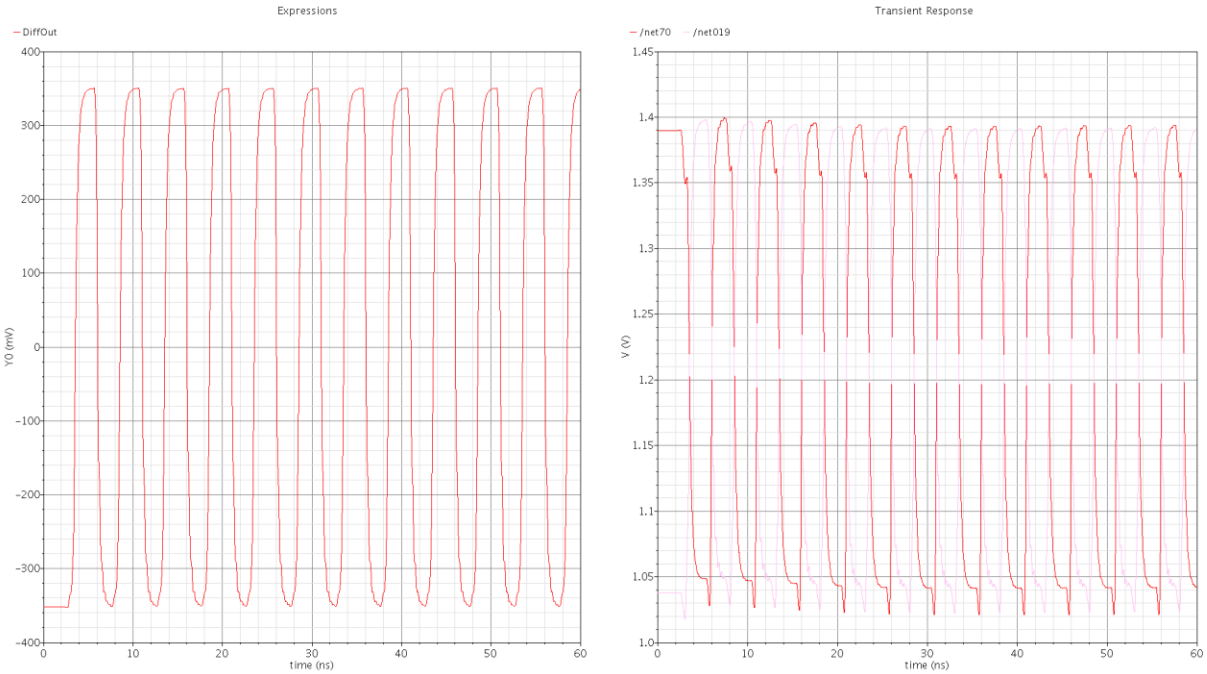


Figure 18 LVDS Output Buffer with CMFB



(a) **(b)**

Figure 19 LVDS Buffer Output at 250 MHz with CMFB: (a) Differential Output (b) Single Ended Output

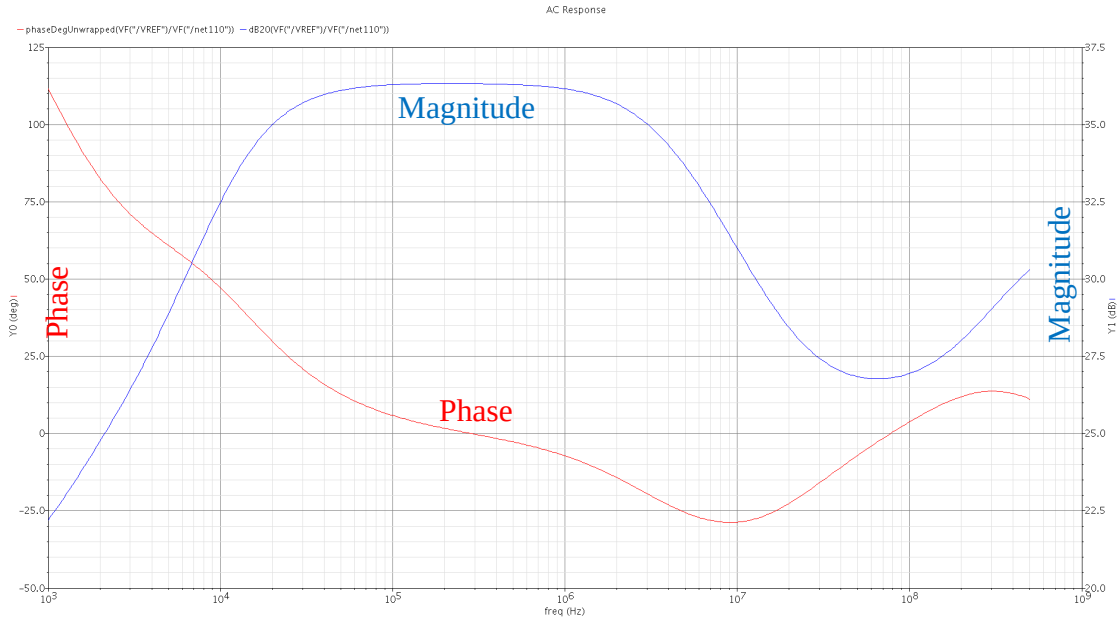


Figure 20 AC Analysis of CMFB Amplifier

3.2.2 Radiation Tolerant Design

Due to the requirement of operating in a radioactive environment and performing at high-speeds, a solution must be found to mitigate the poor switching performance of the HBT only design while still being tolerant to radiation effects detailed in the previous section. The first attempt at improving the switching performance of the basic LVDS buffer structure was to replace the two top switches with straight-gate PMOS's because TID would have little to no effect on their ability to turn off. Unlike the straight-gate PMOS, the straight-gate NMOS would not be viable for use in a radioactive environment so a different approach was taken, replacing the lower two devices of the switchable current source with annular gate NMOS's. The annular gate NMOS's removes the STI edge between the source and drain which mitigates the buildup of trapped positive charge along the STI edge resulting from ionizing radiation, Figure 21.

A large amount of work was done by a colleague, Dr. Robert Greenwell, to create an annular gate NFET in the 7WL PDK which does not come standard with this PDK. After many hours of battling with the PDK, Dr. Greenwell successfully created an annular gate device that could be simulated with the Analog Environment simulator. The created device was of only one size with width of 6 µm and length of 190 nm. The annular device simulated well and was expected to be a final solution for creating a rad-hard LVDS buffer. However, due to complications with the PDK when trying to perform extracted simulations, the work done by Dr. Greenwell was ultimately decided to be left behind for a device that could be used in parasitic extraction simulations.

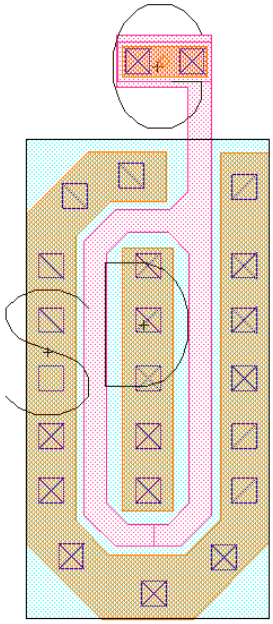


Figure 21 Annular Gate NFET

After many discussions with my mentors, Dr. Blalock and Dr. Britton, it was decided that the top two switches in the LVDS core would remain PFET's and the bottom two switches would become *npn* HBT's, Figure 23. Both of these devices should be able to withstand the harsh radioactive environment present outside of the earth's protective magnetosphere. While the steps towards creating a radiation-hardened design are taking a positive move forward, the issue of switching speed presented in the previous subsection has yet to be resolved. An additional circuit that interfaces with the rad-hard LVDS core circuitry to help sweep the stored charge out of the base of the HBT's was devised, Figure 22. The switching-helper circuit minimizes the on-off voltage swing of the two bottom HBT's, Q11 and Q10, by only allowing their base-emitter voltages to reach approximately 900 mV and thus only providing enough voltage at the base to get the device to operate in the forward-active region and avoid the speed penalties associated with operating in the saturation region.

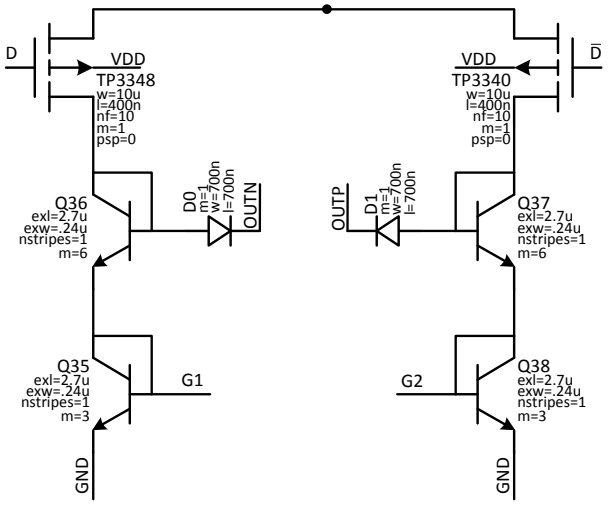


Figure 22 Circuit to Assist with the Turn Off of HBT's

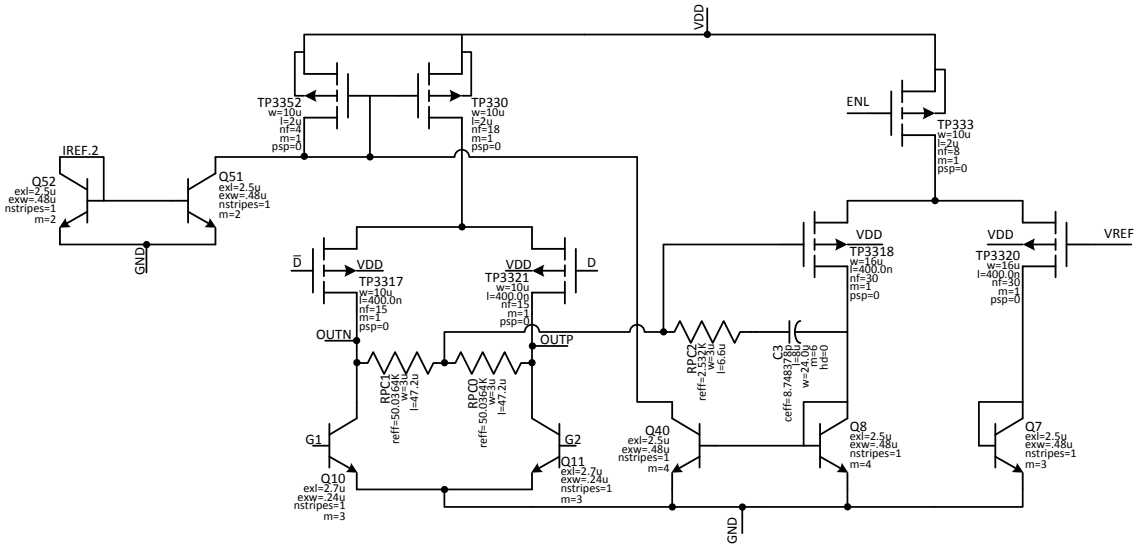


Figure 23 Radiation Tolerant LVDS with CMFB

3.2.3 Final Design

The final design of the LVDS buffer required that it be able to interface with the output of a phase-locked loop (PLL) and that it is able to be turned off as to not draw any unnecessary current. The data presented to the LVDS output driver are two differential 1.8-V CMOS signals from a CMOS divider after being selected a multiplexer. This multiplexer also controls whether or not the LVDS output buffer is powered. Assuming the LVDS driver is powered, the 1.8-V CMOS signals travel through a set of 3.3-V CMOS OR gates that provide a level shift to 3.3-V CMOS and additional buffering, Figure 24. The OR gate needed to be rad-tolerant as well so a radiation hardening technique was used known as the inverted-source technique [20]. The inverted-source technique works through the use of additional hardening circuit that is simply another inverter whose input is the same as the input to the logic gate and whose output is tied to the source of the NMOS of the logic gate. The concept behind the inverted-source technique is that when the logic level is LOW the output is HIGH, and creates a negative gate-source voltage on the NMOS tied to the output of the logic gate. This ensures the NMOS is fully turned off and reduces the leakage current.

The 3.5 mA necessary to create the ±350 mV differential signal across the termination resistor is provided to the circuit through a set of current mirrors that accept an input current of 50 µA, Figure 25. The final design also includes some glue logic that accepts a 3.3-V CMOS logic signal and can turn the LVDS buffer ON or OFF. This is accomplished through a set of inverted-source inverters that enable or disable a PFET to collapse the supply rail. The voltage reference for the CMFB is a simple resistive divider with values of 3 kΩ and 1.85 kΩ resulting in a voltage of 1.25 V between them when supplied by 3.3-V power rails. The final layout of the complete LVDS buffer can be seen in Figure 26. The layout measures 220 µm x 220 µm and fits within the two output pads for the differential signal to be taken off-chip. In the layout of the LVDS driver, common centroid layout was utilized in the current mirrors to ensure consistent current draw across the wafer and chip. The common centroid method was not used however in the placement of the core circuitry because the switchable current source relies on a large signal swing to turn the core devices on and off. Unlike an analog design, where small

signals are used to place the devices in the exact bias condition and matching across a single chip is essential, this concept is more related to a digital design.

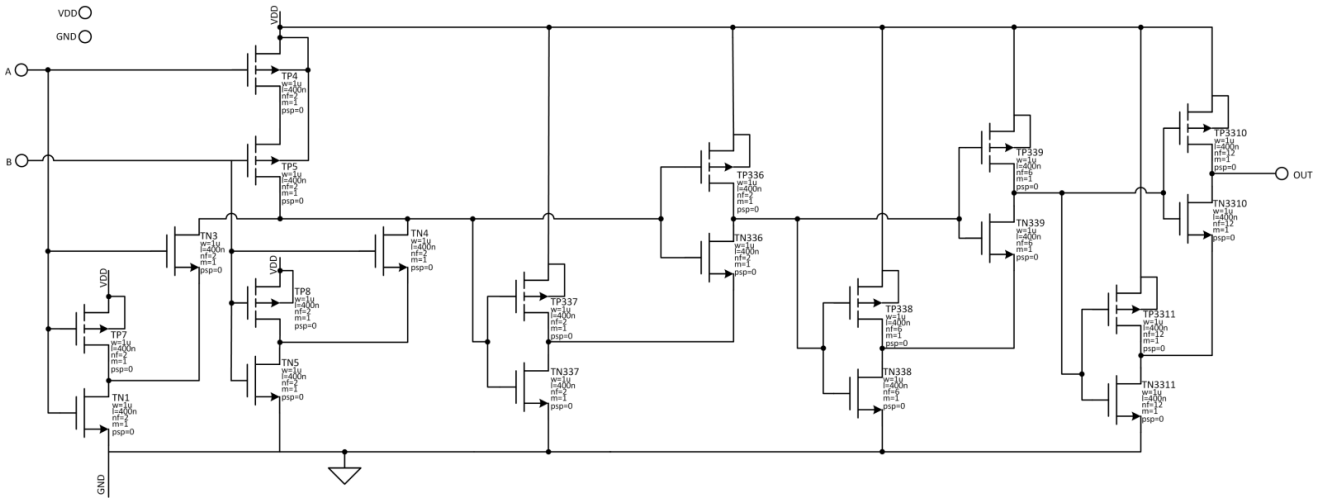


Figure 24 Radiation Tolerant OR Gate

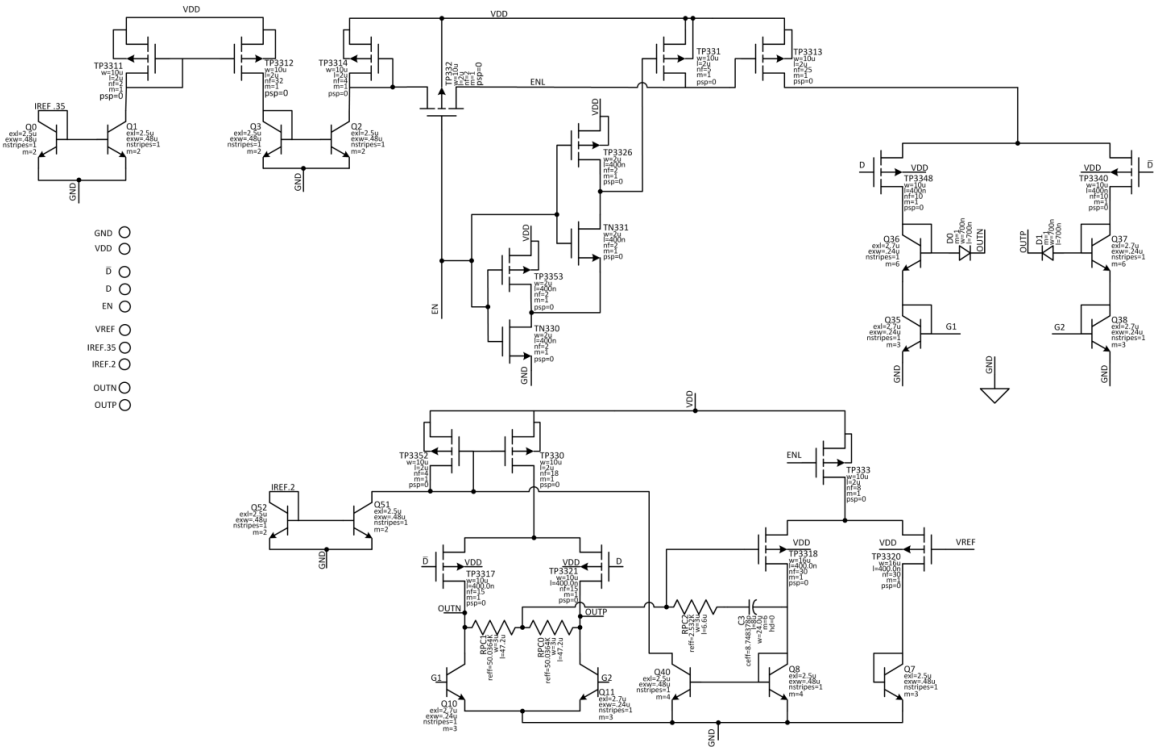


Figure 25 Final LVDS Buffer Design

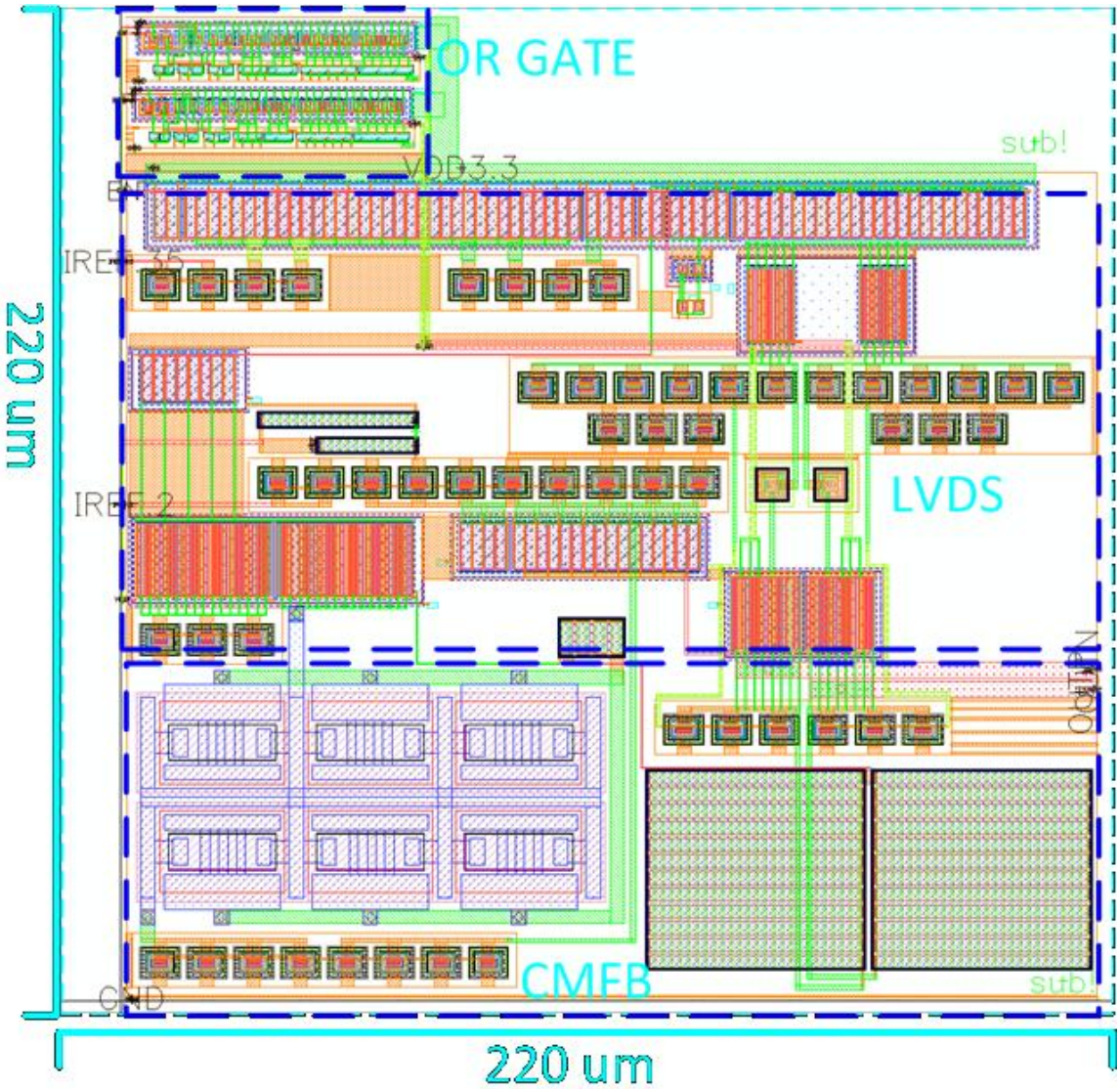


Figure 26 Final LVDS Buffer Layout

3.3 Final Design Simulations

The following sub-sections will detail the simulations performed to validate the final LVDS buffer design before the device was sent out for fabrication. The validations included a frequency sweep from 80 MHz to 250 MHz, a temperature sweep from −50 °C to 125 °C, and a power supply voltage sweep from 3.0 V to 3.6 V. Meeting the validation criteria should ensure successful operation of the LVDS buffer once it has been fabricated and can then be experimentally verified. All simulations presented in the following sub-sections are post-layout extracted simulations. In the following simulation results figures, the leftmost waveform is the differential output signal of the LVDS driver and the rightmost waveforms are single-ended signals at each side of the shunt 100-Ω termination resistor driven by the LVDS buffer circuit.

3.3.1 Frequency Sweep

The simulations in which the output frequency of the LVDS buffer was swept from 80 MHz to 250 MHz show the differential signal is capable of reaching the ±350 mV across the termination resistor in all cases. At 250 MHz there is some rounding of the output waveform; this can be attributed to the use of the SiGe HBT's and their poor performance while switching off. As the frequency is decreased the performance of the buffer improves because the HBT's have more time to turn-off resulting in a flatter waveform peak.

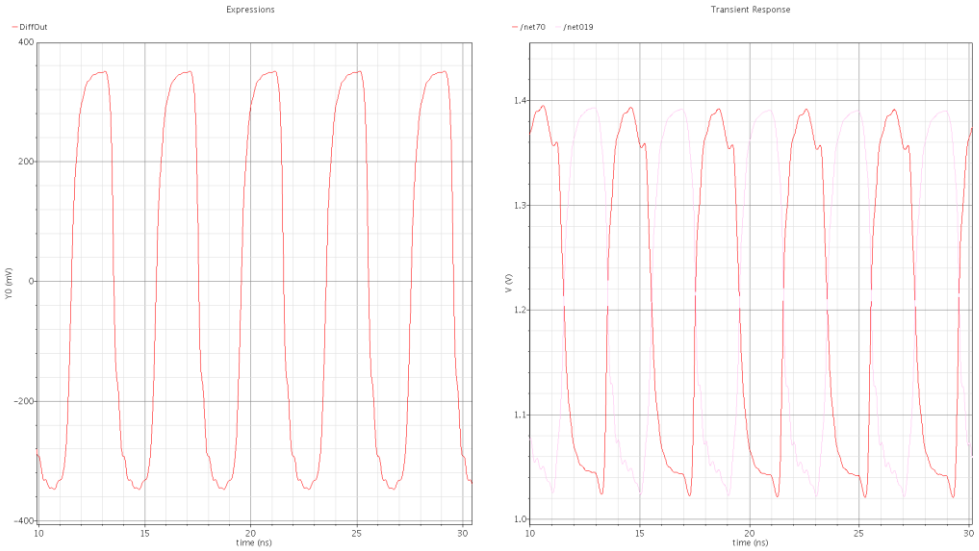


Figure 27 LVDS Final Design Output at 250 MHz

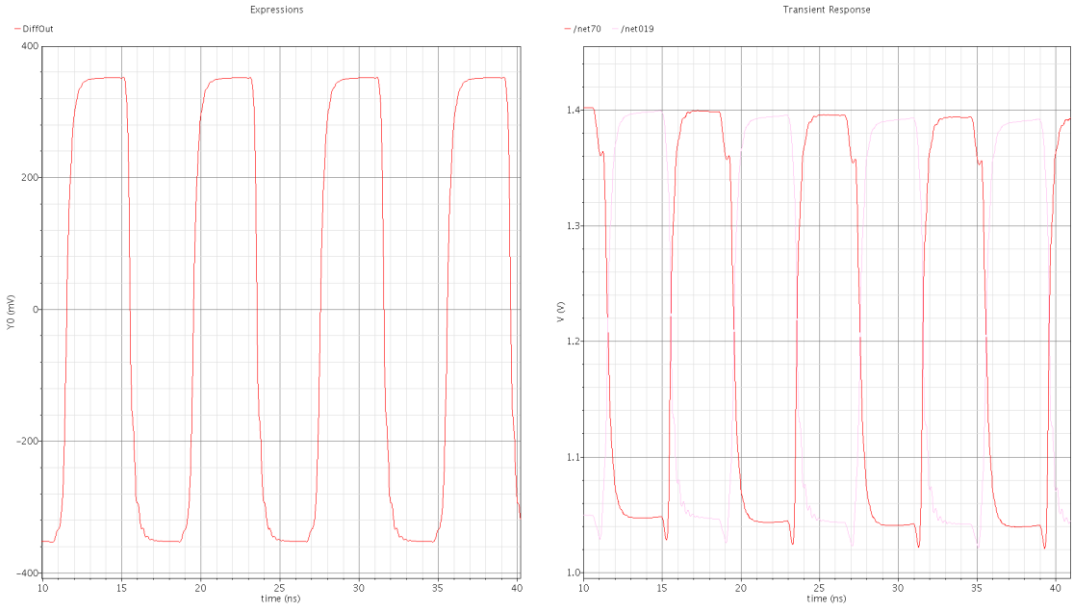


Figure 28 LVDS Final Design Output at 125 MHz

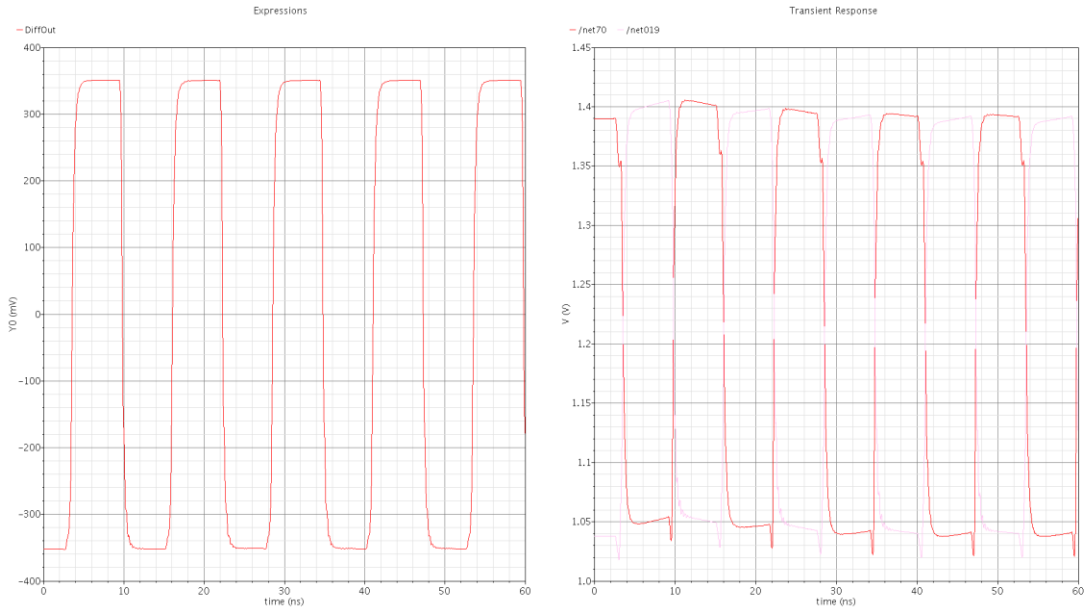


Figure 29 LVDS Final Design Output at 80 MHz

3.3.2 Temperature Sweep

The simulations in which the operating temperature of the LVDS buffer was swept from −50 °C to 125 °C show the differential signal is capable of reaching the ±350 mV across the termination resistor in all cases. The common-mode output voltage is shown to be stable across temperature as well. The temperature sweep does not affect performance as the frequency increases.

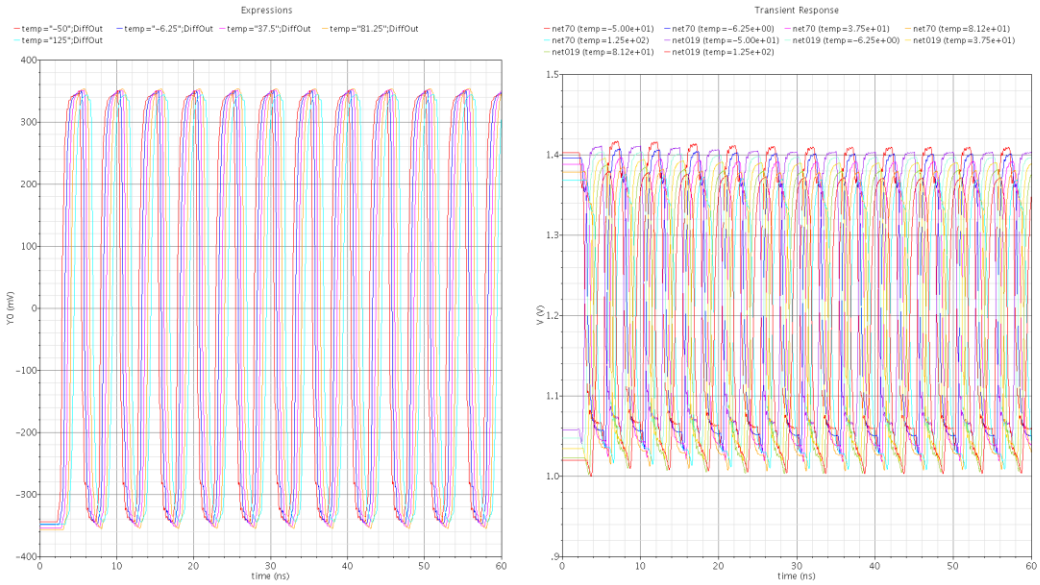


Figure 30 LVDS Final Design Output at 250 MHz from −50 °C to 125 °C

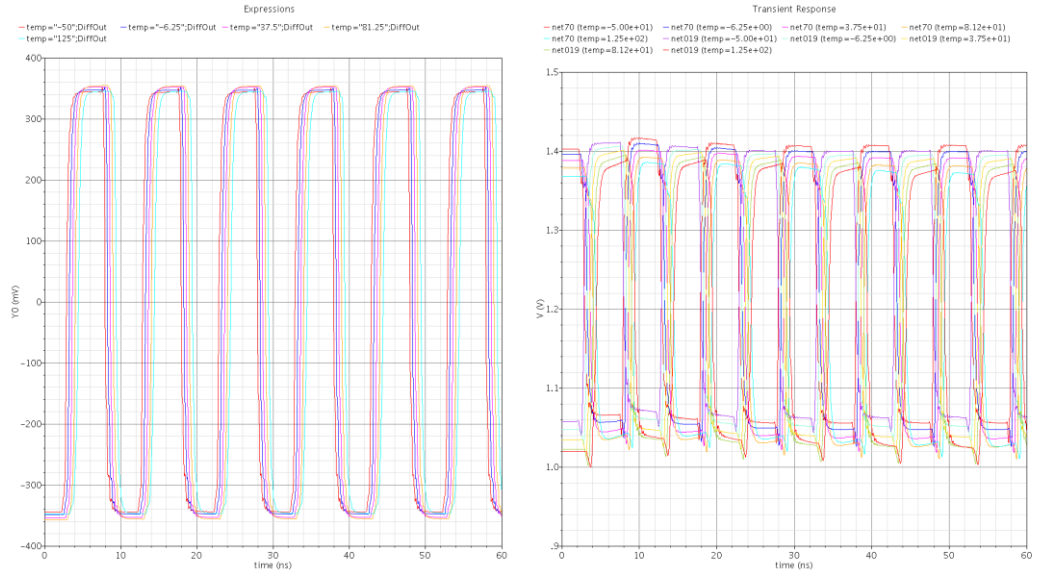


Figure 31 LVDS Final Design Output at 125 MHz from −50 °C to 125 °C

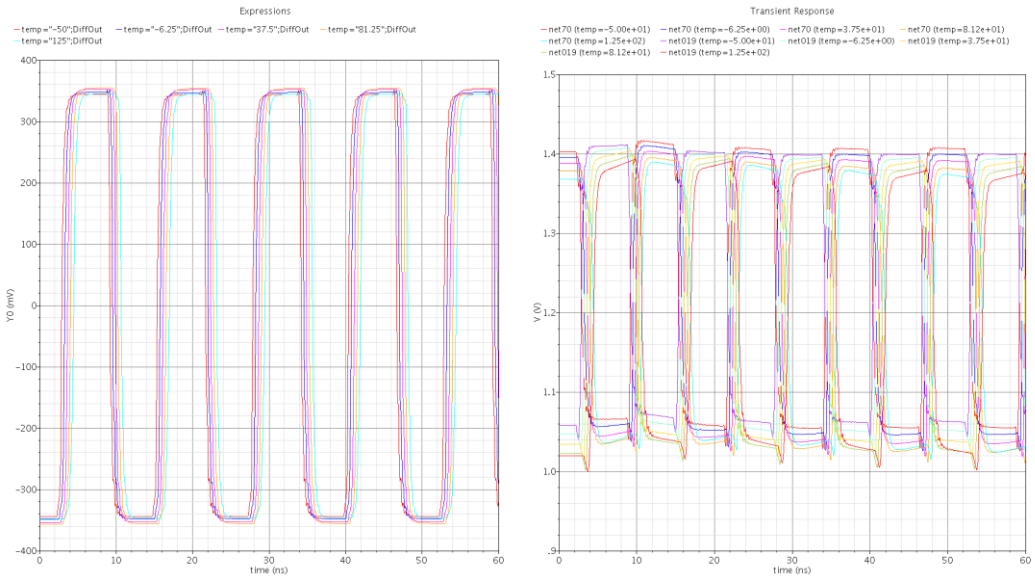


Figure 32 LVDS Final Design Output at 80 MHz from −50 °C to 125 °C

3.3.3 Voltage Sweep

The simulations in which the power supply voltage of the LVDS buffer was swept from 3.0 V to 3.6 V (± 10% VDD) show the differential signal is capable of reaching the ± 350 mV across the termination resistor in all cases. The common-mode output voltage is not flat over the voltage variation because it is a resistive divider network but it never swings too high or low to be considered outside the standard LVDS parameters. The voltage sweep does not affect performance as the frequency increases.

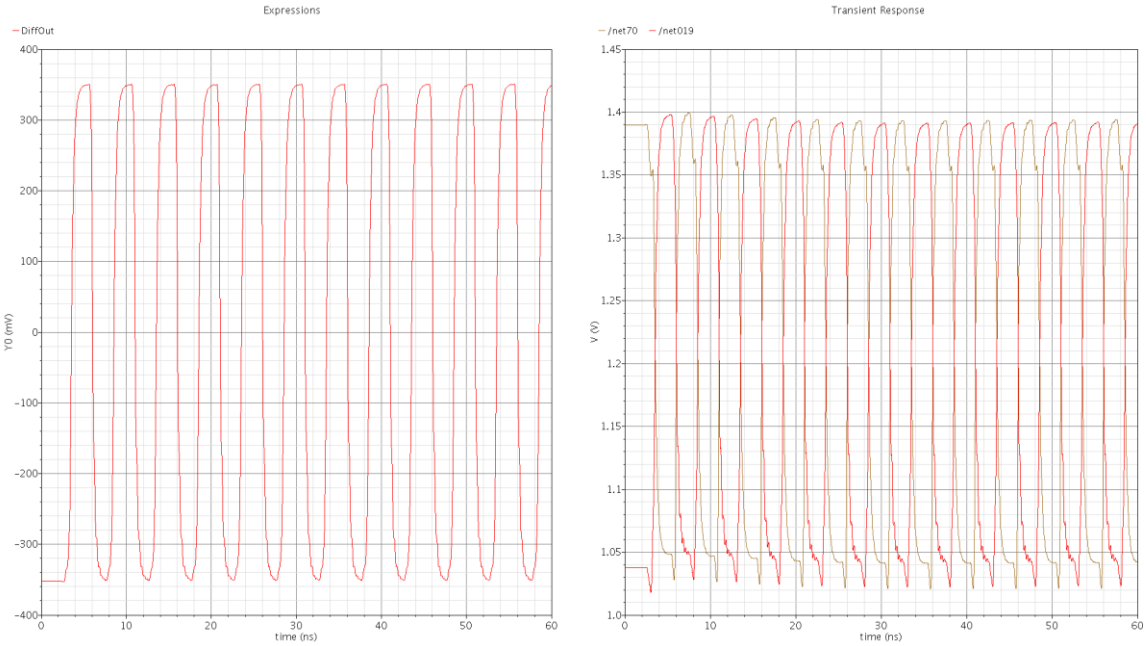


Figure 33 LVDS Final Design Output at 250 MHz and 3.3 V Power Supply

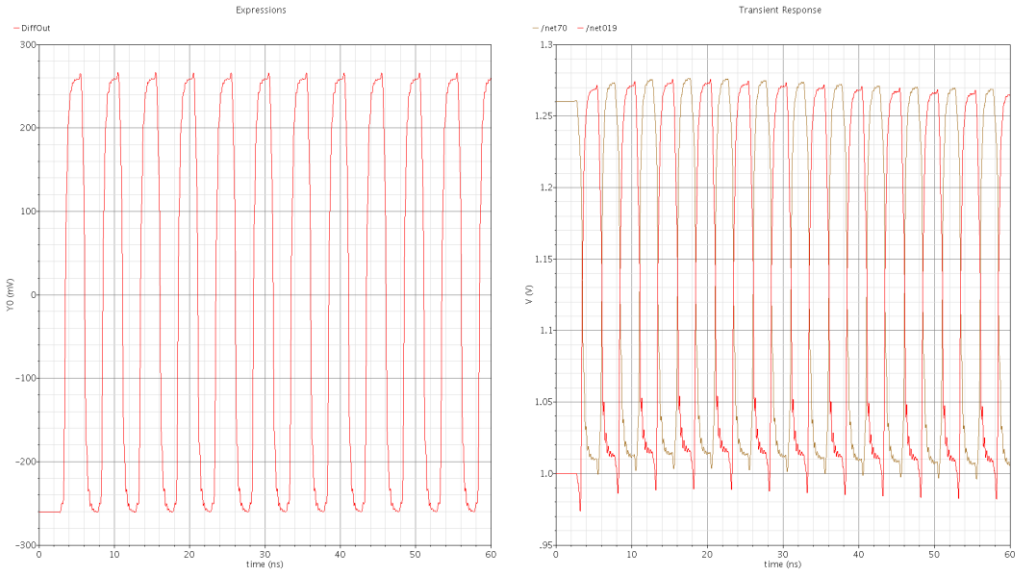


Figure 34 LVDS Final Design Output at 250 MHz and 3.0 V Power Supply

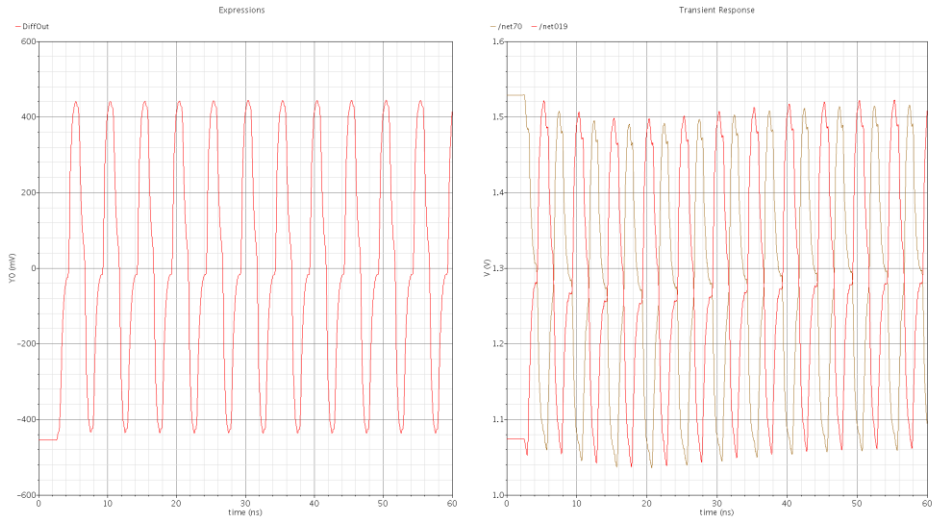


Figure 35 LVDS Final Design Output at 250 MHz and 3.6 V Power Supply

CHAPTER 4: RESULTS AND DISCUSSION

The following section exhibits the experimental test results of the manufactured LVDS output buffer. The buffer was tested over temperature, voltage, and frequency to fully validate its operation. A test board was designed to accommodate the integrated circuit and provide the necessary bias currents and supply voltages, Figure 36. The test results only show one of the differential signals although both signals were validated; it was deemed necessary to only show one of the waveforms. The validation of the LVDS buffer's output at higher frequencies was rather difficult. The board was not properly designed with a 100-Ω transmission line and was therefore subject to some reflections and signal degradation when terminated with a 100-Ω resistor. The probes used to measure the signal are also responsible for some of the signal degradation, i.e. their associated capacitance. The LVDS driver is not intended to drive heavy capacitive loads and in simulation the largest capacitive load driven was 3 pF while the probes used to measure the signal have an associated capacitance of 9 pF to 15 pF. One might comment on the difference between the upper and lower peaks in the results. The cause of the asymmetrical slewing is directly caused by the asymmetrical design of the LVDS core circuitry. The MOSFET's and HBT's have different switching behaviors and this is the cause of the difference in the waveforms. Figures 37-60 show the LVDS buffer's output over various frequencies, temperatures, and voltage supplies. Although some of the experimental plots show non-ideal output signals only four of the waveforms can be considered outside of the LVDS standard parameters, Figures 52, 53, 55, and 57 Figures 52 and 53both show waveforms that do not reach a proper voltage level and are powered with 3 V instead of 3.3 V. Figures 55 and 57 are both powered by 3.6 V instead of 3.3 V and their output waveforms exceed the necessary voltage. With 24 waveforms presented only 1/6 of them show failure and these four plots are either underpowered or overpowered, the rest of the images show a properly functioning LVDS driver capable of operating over a wide set of temperatures and frequencies.

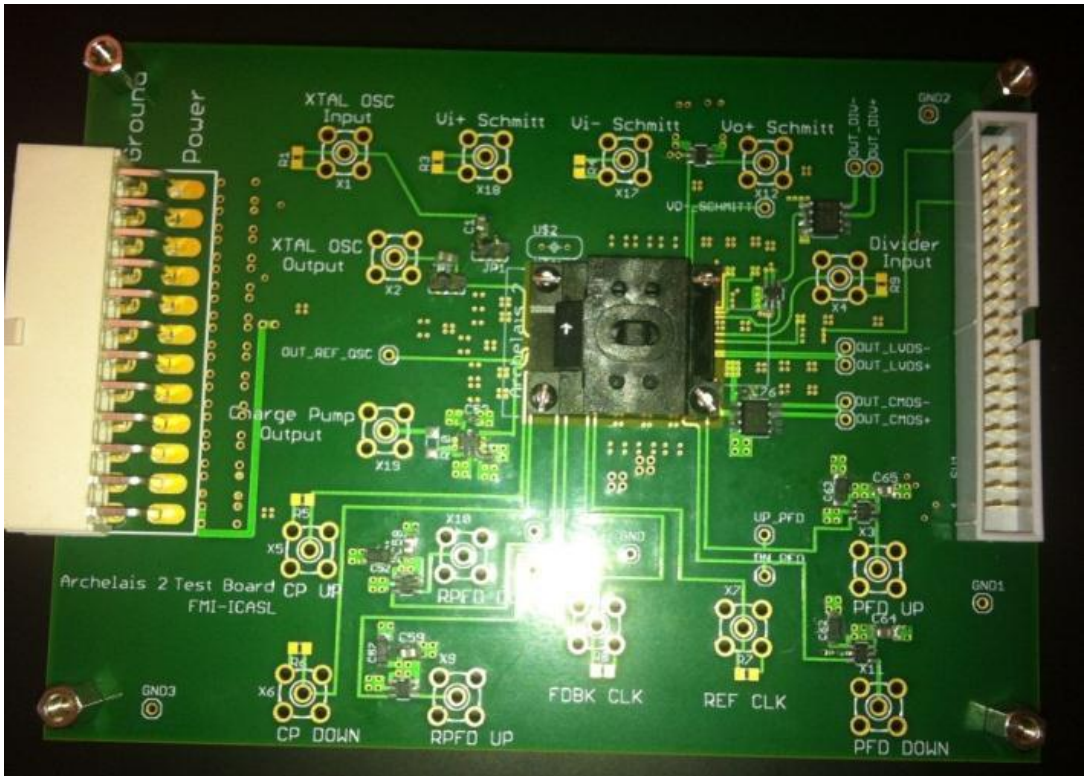


Figure 36 Test Board for Experimental Validation

4.1 Test Results

4.1.1 Temperature and Frequency Sweep at 3.3 V Power Supply

The following experimental test results show the single-ended output terminated with a 100-Ω resistor when subjected to ambient temperatures of −55 °C to 125 °C and with the operating frequency swept from 117 kHz to 200 MHz. The operation of the LVDS output buffer can be seen to operate properly over these test conditions when operating with the nominal DC power supply.

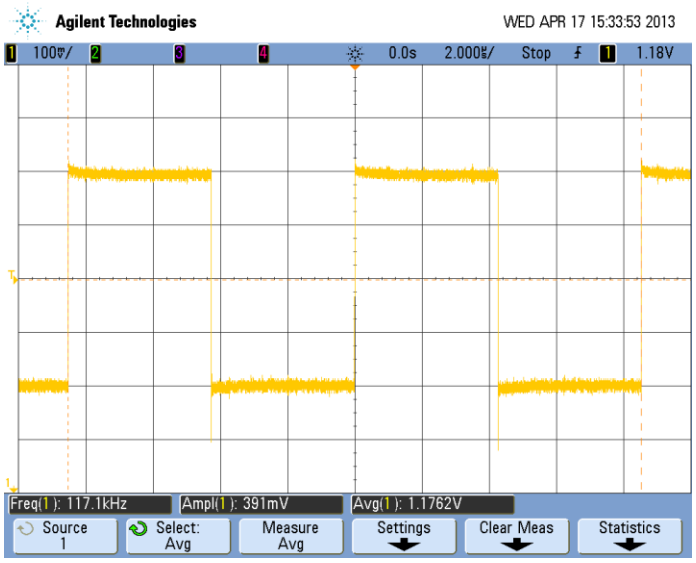


Figure 37 LVDS Output at −55 °C and 117 kHz

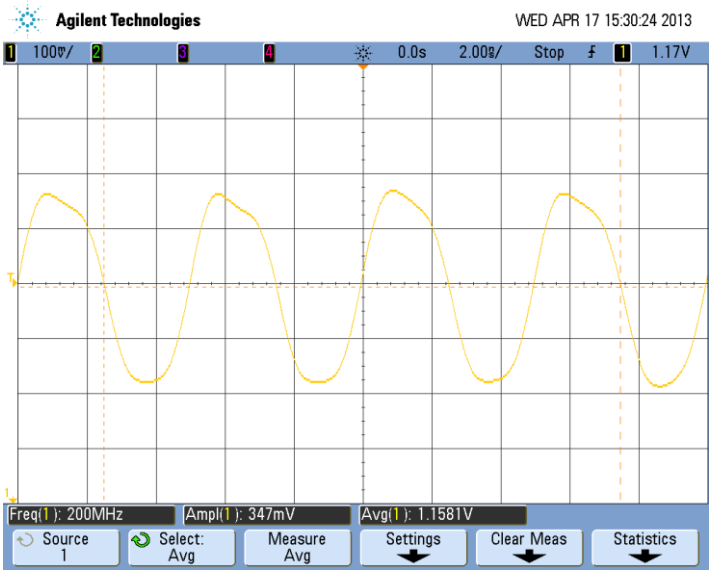


Figure 38 LVDS Output at −55 °C and 200 MHz

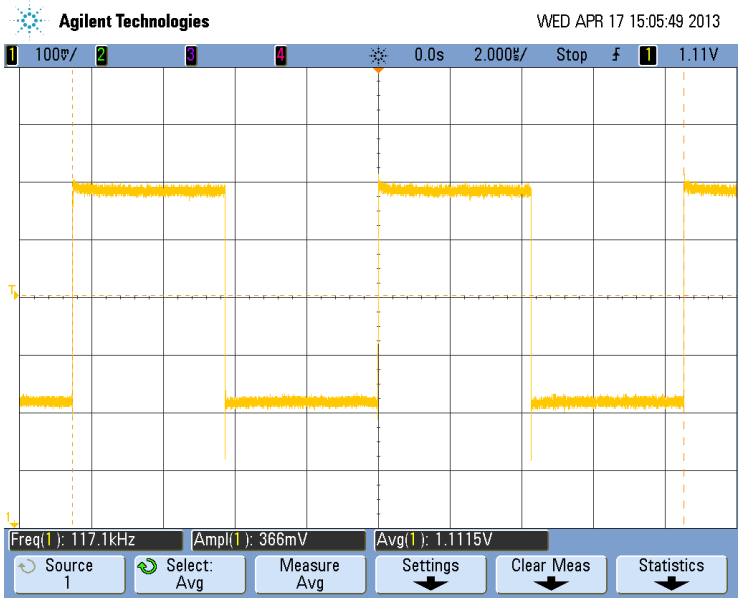


Figure 39 LVDS Output at 27 °C and 117 kHz

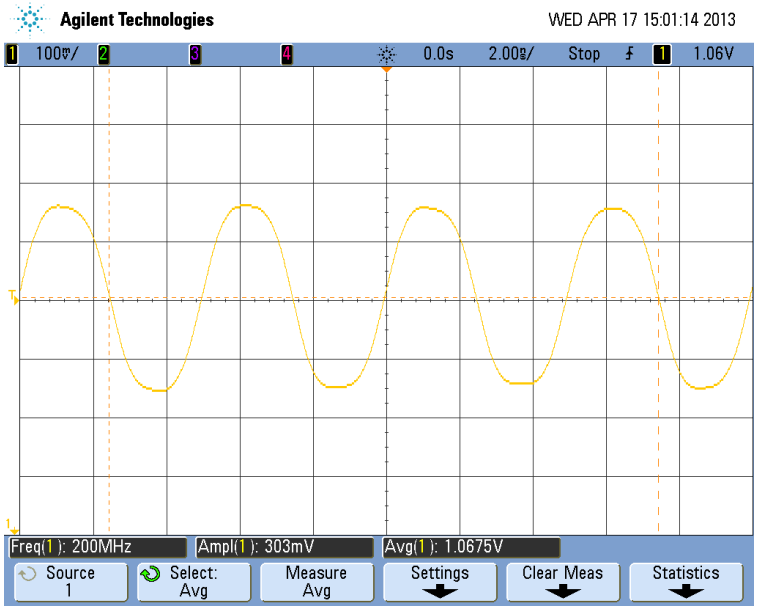


Figure 40 LVDS Output at 27 °C and 200 MHz

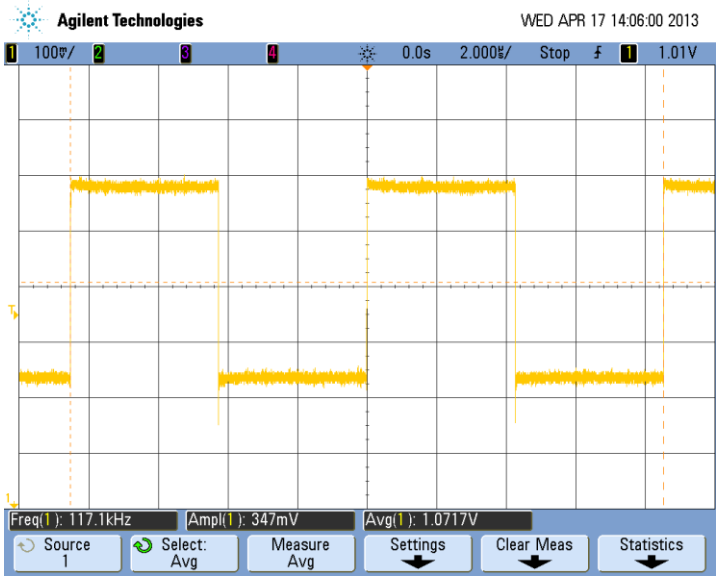


Figure 41 LVDS Output at 85 °C and 117 kHz

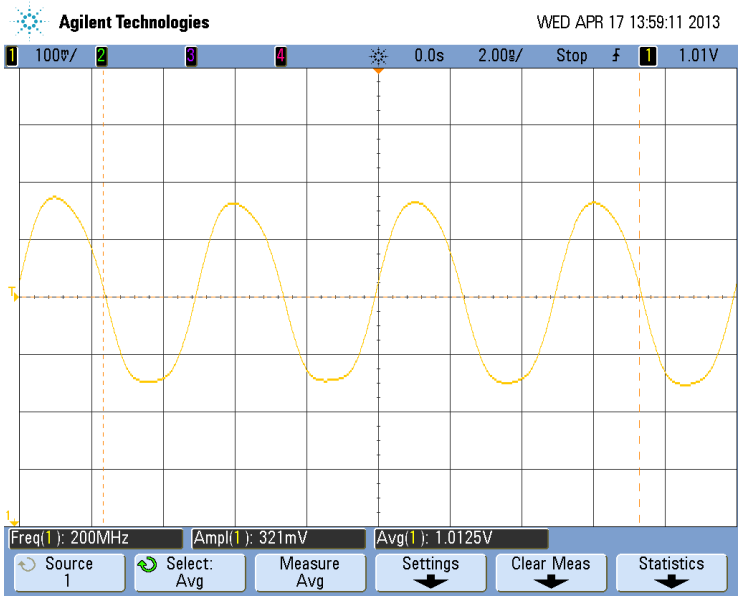


Figure 42 LVDS Output at 85 °C and 200 MHz

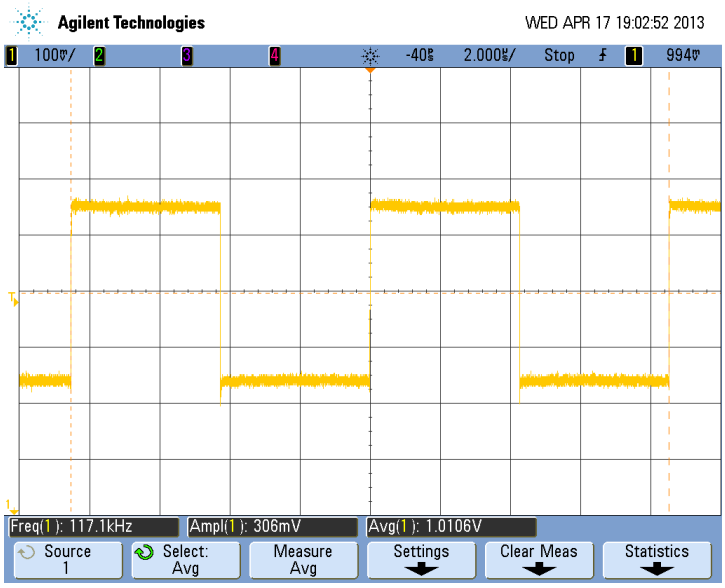


Figure 43 LVDS Output at 125 °C and 117 kHz

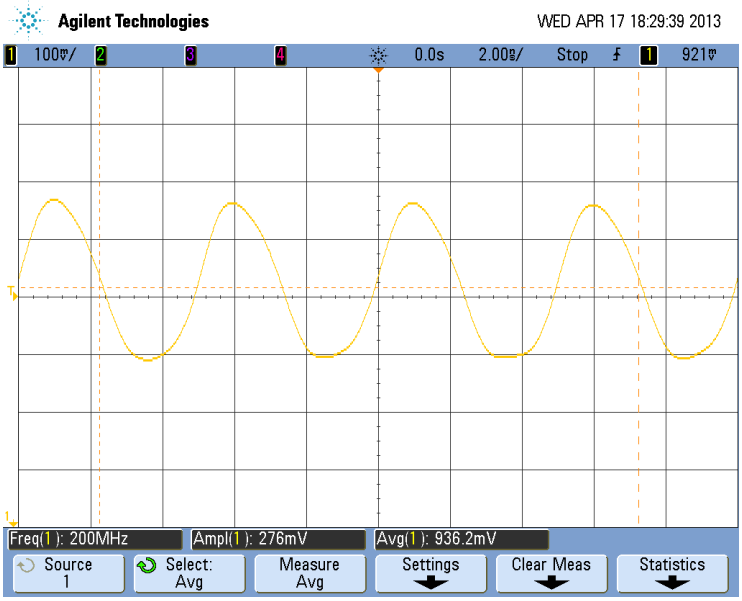


Figure 44 LVDS Output at 125 °C and 200 MHz

4.1.2 Temperature and Frequency Sweep at 3.0 V Power Supply

The following experimental test results show the single-ended output terminated with a 100-Ω resistor when subjected to ambient temperatures of −55 °C to 125 °C, the operating frequency swept from 117 kHz to 200 MHz, and the DC power supply operating at −10% (3.0 V). The operation of the LVDS output buffer can be seen to operate properly over these test conditions even when operating below the nominal DC power supply.

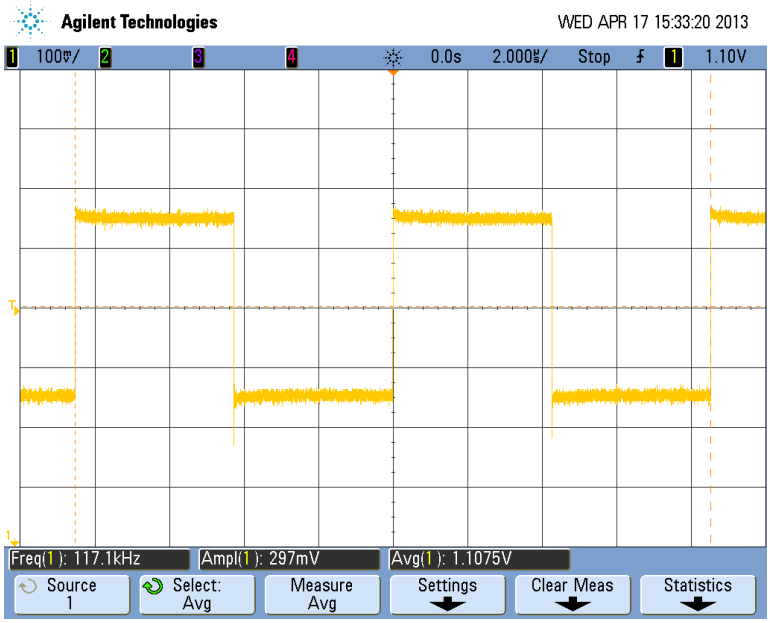


Figure 45 LVDS Output at −55 °C and 117 kHz

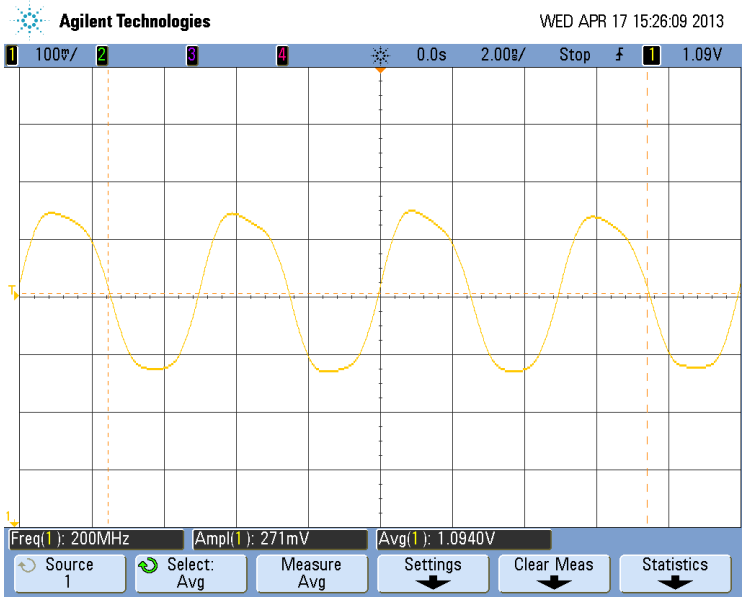


Figure 46 LVDS Output at −55 °C and 200 MHz

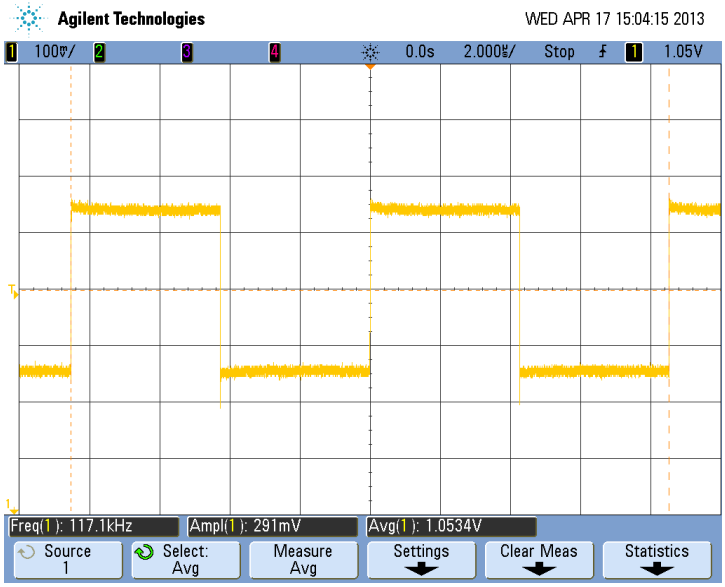


Figure 47 LVDS Output at 27 °C and 117 kHz

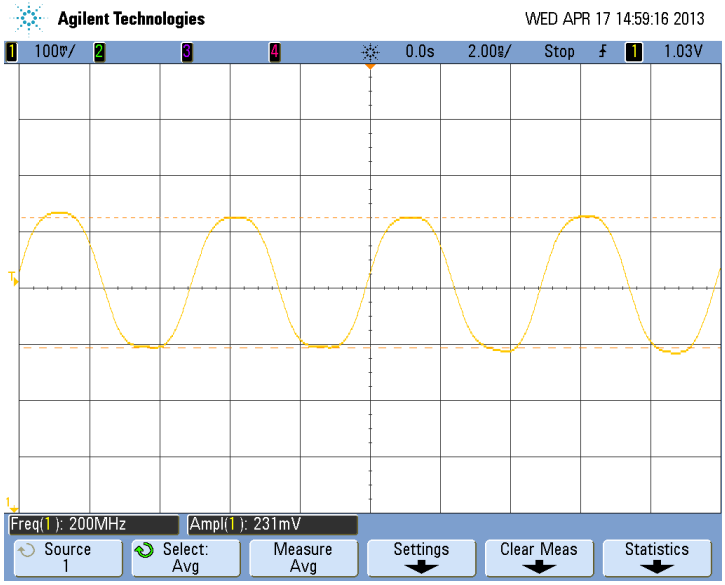


Figure 48 LVDS Output at 27 °C and 200 MHz

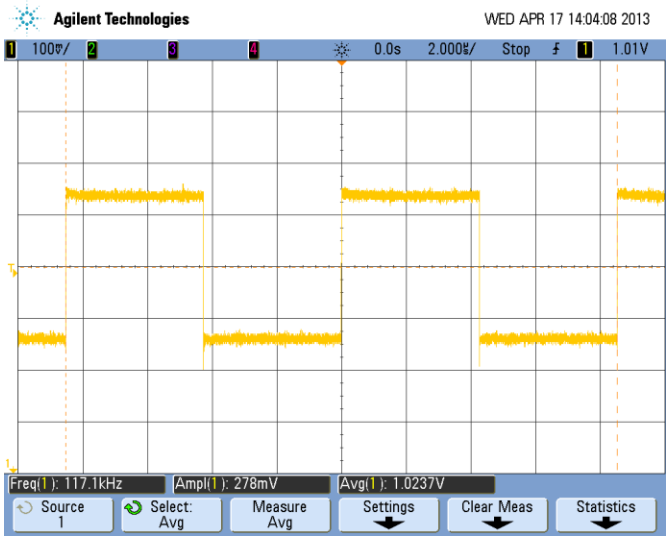


Figure 49 LVDS Output at 85 °C and 117 kHz

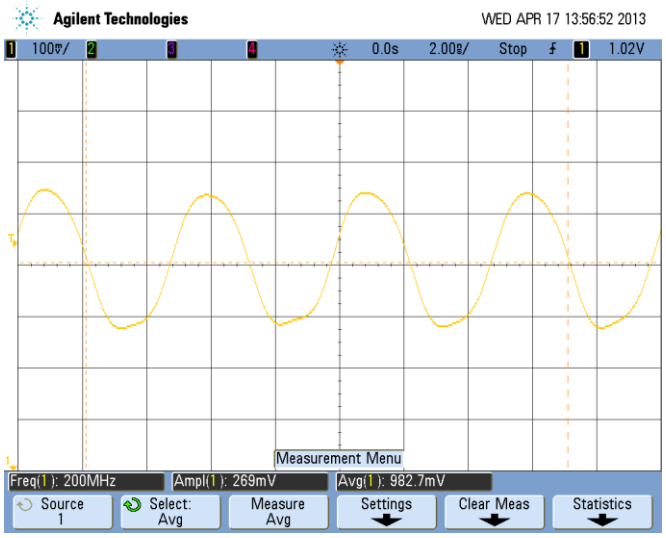


Figure 50 LVDS Output at 85 °C and 200 MHz

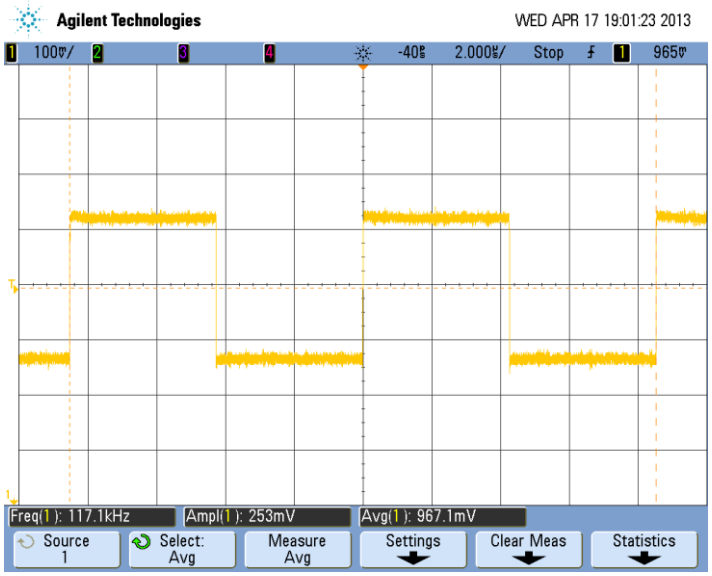


Figure 51 LVDS Output at 125 °C and 117 kHz

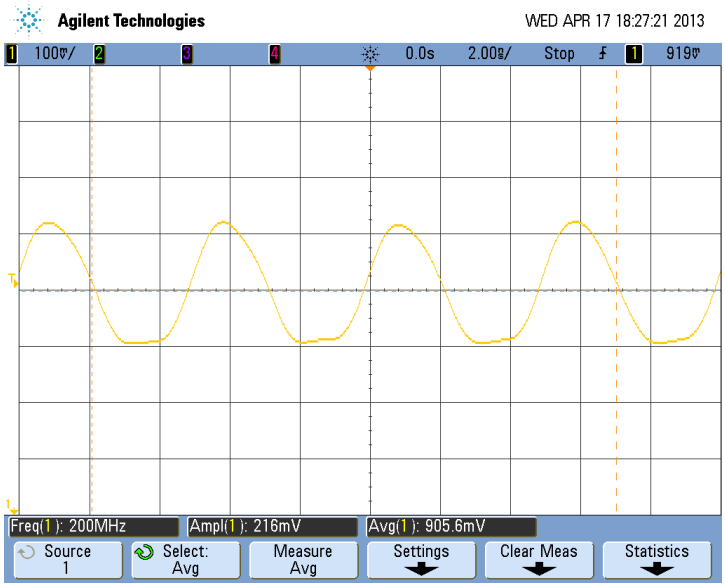


Figure 52 LVDS Output at 125 °C and 200 MHz

4.1.3 Temperature and Frequency Sweep at 3.6 V Power Supply

The following experimental test results show the single-ended output terminated with a 100-Ω resistor when subjected to ambient temperatures of −55 °C to 125 °C, the operating frequency swept from 117 kHz to 200 MHz, and the DC power supply operating at +10% (3.6 V). The operation of the LVDS output buffer can be seen to operate properly in most of these test conditions even when operating above the nominal DC power supply. The output failure can be attributed to the higher DC power supply level which causes the current supplied by the current mirrors to increase which leads to a larger output swing, especially at colder temperatures.

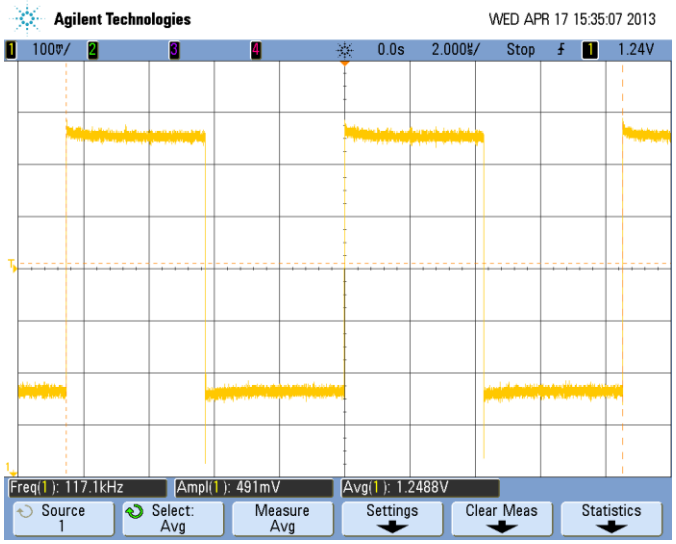


Figure 53 LVDS Output at −55 °C and 117 kHz

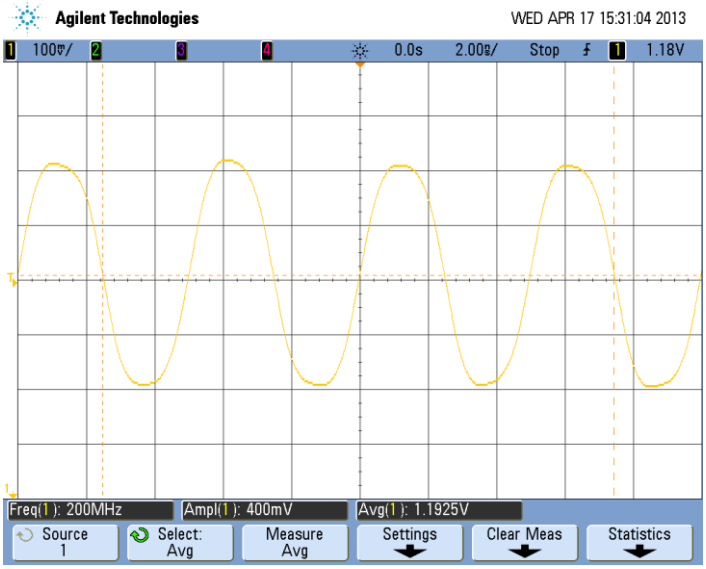


Figure 54 LVDS Output at −55 °C and 200 MHz

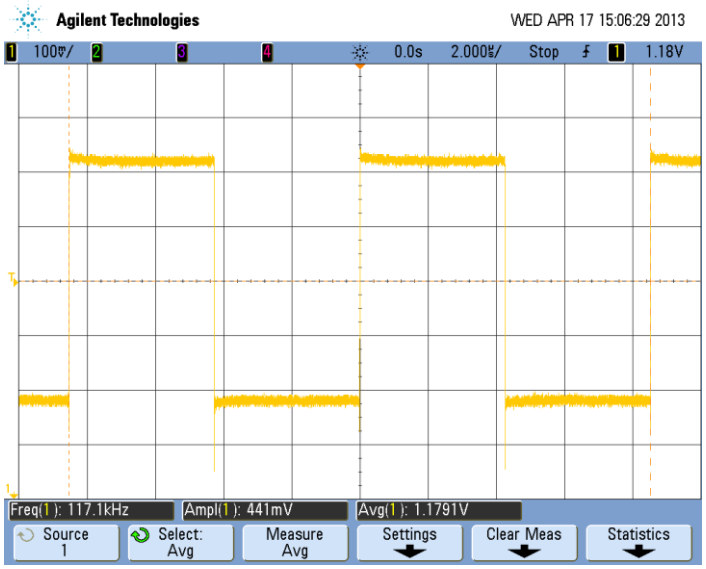


Figure 55 LVDS Output at 27 °C and 117 kHz

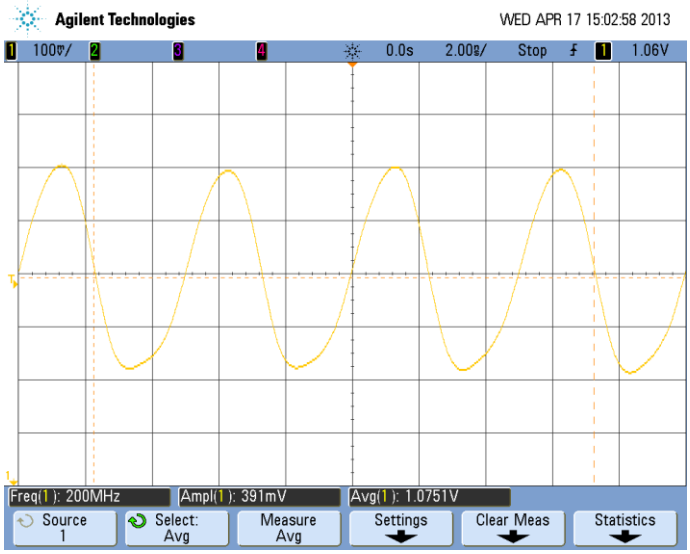


Figure 56 LVDS Output at 27 °C and 200 MHz

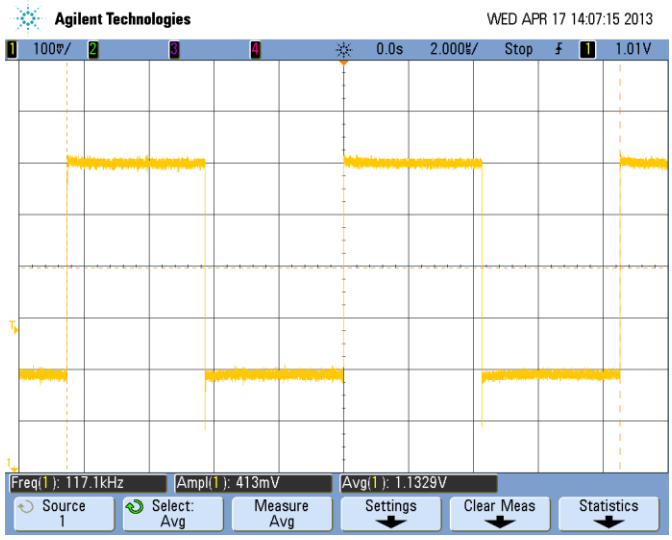


Figure 57 LVDS Output at 85 °C and 117 kHz

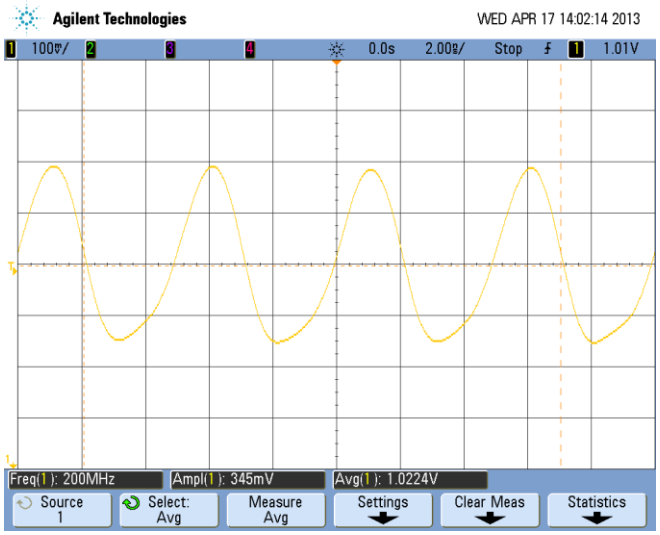


Figure 58 LVDS Output at 85 °C and 200 MHz

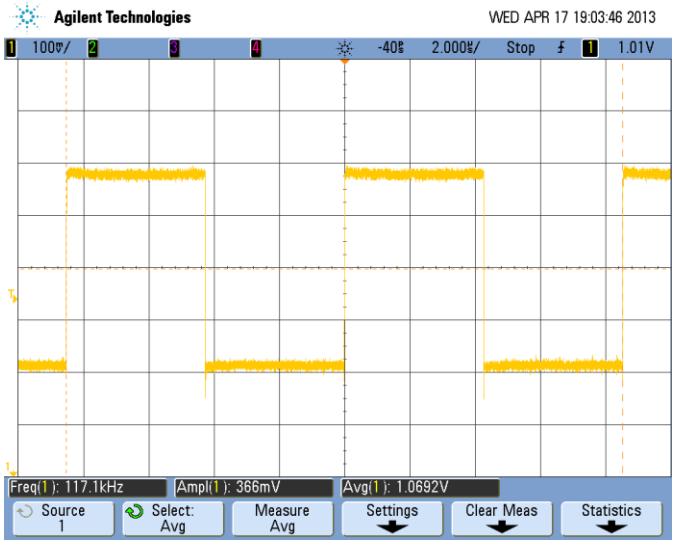


Figure 59 LVDS Output at 125 °C and 117 kHz

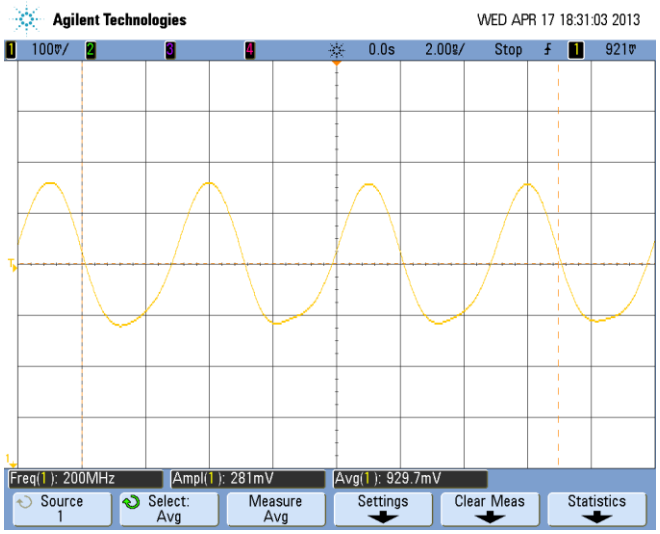


Figure 60 LVDS Output at 125 °C and 200 MHz

CHAPTER 5: CONCLUSIONS AND RECOMMENDATIONS

In conclusion, a LVDS output driver that can operate in the harsh environment of space has been presented. The LVDS driver has been successfully validated and operates over a temperature range of −55 °C to 125 °C and over a frequency range of 117 kHz to 200 MHz. Though the driver has yet to be tested for its TID immunity, it is expected to perform adequately during irradiation due to design choices to use SiGe HBT's and the inverted source technique. It is evident in Section 4.1.1 that the LVDS buffer has an output that matches all the criteria of the LVDS standards as put forth by ANSI. The common mode voltage is slightly lower than it was designed to be. This is attributed to the use of resistors. While the ratio remains constant over temperature, the manufacturing process tends to not be extremely accurate when building transistors. In future designs of the presented LVDS buffer, a bandgap reference should be used to ensure a stable common-mode output voltage instead of a resistive divider, Figure 61. The Widlar bandgap voltage reference is capable of producing a stable output voltage over temperature.

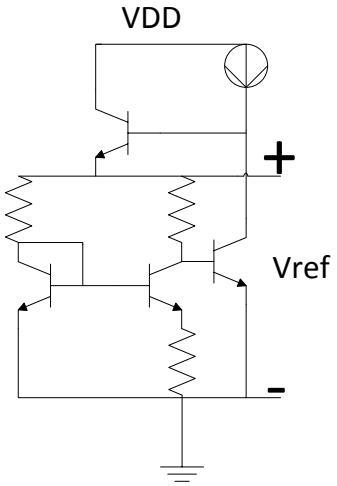


Figure 61 Widlar Bandgap Voltage Reference [18]

The OR gate chosen to perform the level shifting and buffering before the signal is passed to the LVDS core circuitry is a cause of the issues seen in the 3.6 V experimental test data. When the LVDS circuitry is powered with 3.6 V, the CMOS divider that feeds the data to the OR gate is still operating at 1.8 V due to the on-chip voltage regulator that powers the 1.8-V circuitry. When the 1.8-V CMOS logic signal is applied to the input of the OR gate, it is just barely able to make the OR gate switch states. This leads to the OR gate switching slower than if the applied logic signal were closer to 3.6 V. This was a design oversight and was not caught in simulations. A solution to this problem for future iterations of this design would be to replace the OR gate with a true level shifter. This can be accomplished using an array of source followers or a circuit similar to Figure 62.

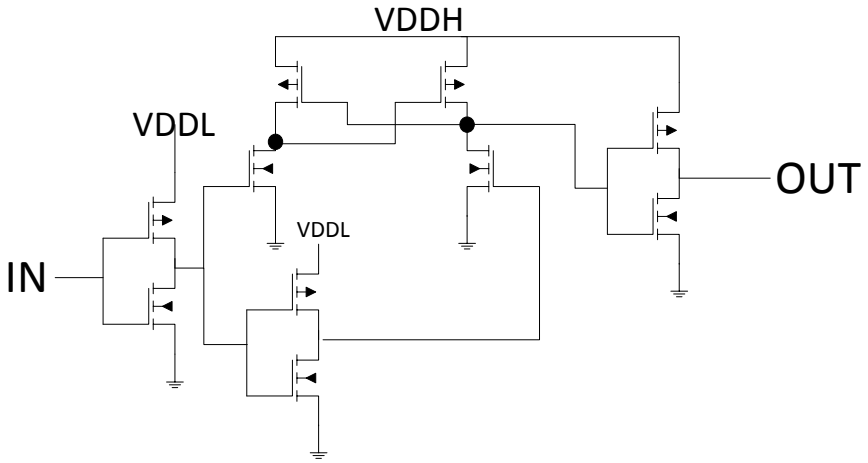


Figure 62 Conventional CMOS Level Shifter Design [19]

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APPENDIX

The following images showcase differential measurements of the integrated LVDS driver solution. Figure 63 shows the waveform that a LVDS receiver would see at its input while Figures 64 and 65 display the extremely fast rise and fall times of roughly 2 ns.

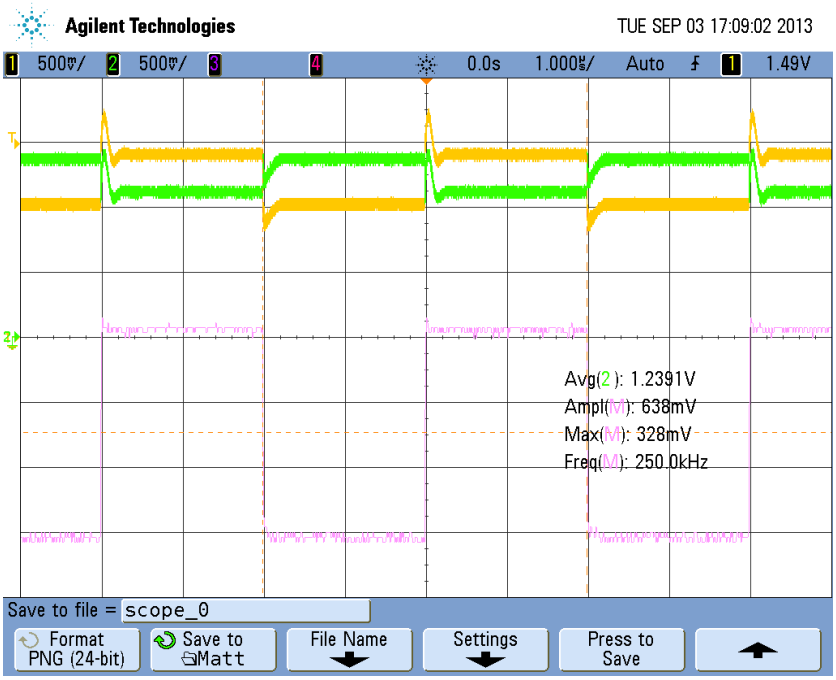

Figure 63 Differential Measurement

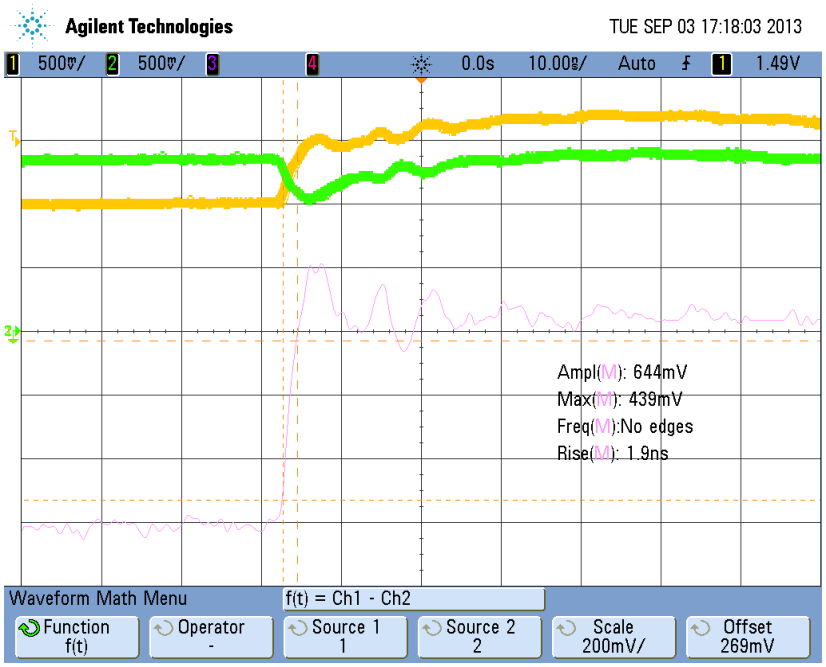

Figure 64 Rise Time Measurement

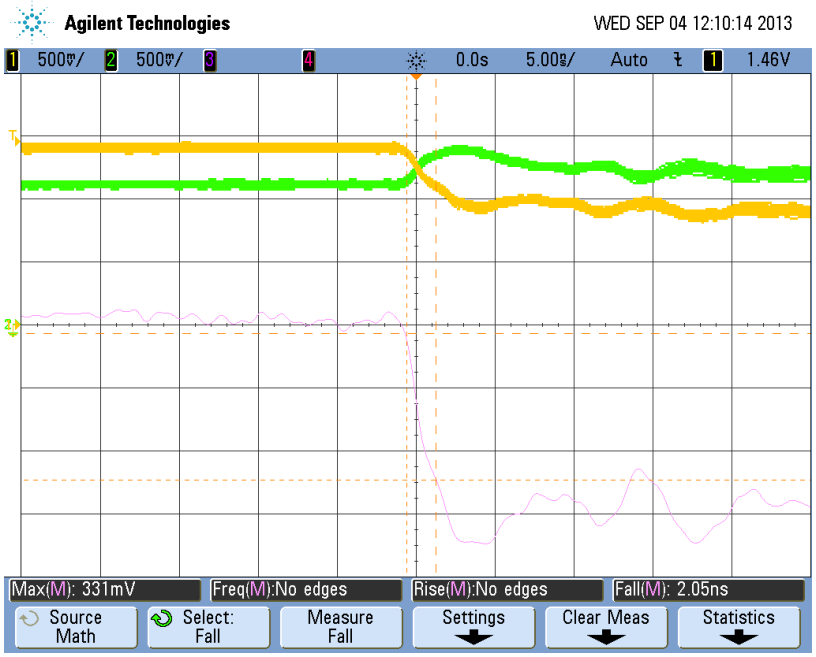

Figure 65 Fall Time Measurement

VITA

Matthew Ian Laurence was born on December 25, 1987 in West Islip, NY. After moving to Knoxville, TN at the age of 4, he spent the next 21 years as a resident. He attended Farragut High School and graduated in 2006. Upon graduating high school he began his undergraduate studies at the University of Tennessee, Knoxville where he graduated in May 2011 with a Bachelor of Science in Electrical Engineering. During the summer of 2011, he joined the Integrated Circuits and Systems Laboratory headed by Dr. Benjamin J. Blalock and began his graduate studies under his tutelage. After a year of graduate studies he accepted an internship at the Jet Propulsion Laboratory in Pasadena, CA where he was mentored by Dr. Mohammad Mojarradi and his group of engineers in the Advanced Instrument and Electronics unit. He graduated from the University of Tennessee, Knoxville with a Master of Science in Electrical Engineering in December 2013 and began a full time career at JPL as an Electronics Engineer under his mentor from the previous summer.