To the Graduate Council:

I am submitting herewith a thesis written by Jeremy Ross Jackson entitled "Silicon-on-Insulator Power Management Integrated Circuit for Thin-Film Solid-State Lithium-Ion Micro-Batteries." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Dr. Benjamin J. Blalock
Major Professor

We have read this thesis
and recommend its acceptance:

Dr. Syed K. Islam

Dr. Donald W. Bouldin

Accepted for the Council:

Anne Mayhew
Vice Provost and
Dean of Graduate Studies

(Original signatures are on file with official student records.)

SILICON-ON-INSULATOR POWER MANAGEMENT INTEGRATED CIRCUIT FOR THIN-FILM SOLID-STATE LITHIUM-ION MICRO-BATTERIES

A Thesis Presented for the

Master of Science Degree

The University of Tennessee, Knoxville

Jeremy Ross Jackson

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DEDICATION

This thesis is dedicated to my grandfather, Roland B. Butterfield, II, who was always there to give a helping hand whenever I needed it most.

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ABSTRACT

This thesis presents the design and implementation of a power management integrated circuit (IC) that is capable of both current and voltage charging thin-film, solid-state, lithium-ion micro-batteries. The power management system has been fabricated using a single-poly, 0.35-µm, partially-depleted, silicon-on-insulator process (PD-SOI). The system contains a temperature stable current charger (current generator and a 4-bit current-mode DAC), a regulated voltage supply (voltage amplifier), and a voltage monitoring circuit (2-bit flash ADC). Experimental results of the first version of the power management system show proper functionality was obtained. The current charger produced a 2% worst-case variation in output current over the temperature range 0–100°C. The regulated voltage output was measured to be 4.4 V and the digital outputs of the flash ADC transitioned at 3.45 and 4.76 V.

TABLE OF CONTENTS

Chapter Page

I. **Introduction and Overview 1**
Introduction 1
Overview 3

II. **Micro-Battery Power Management System Concepts 4**
Micro-Battery Structure 4
Current Source 5
Voltage Source 11
Low-Resolution ADC 13

III. **Design of Micro-Battery Power Management System Components 17**
Programmable Current Source 17
Current Generator 17
Current Output DAC 22
Regulated Voltage Source 35
Micro-Battery Voltage Monitor 37

IV. **Micro-Battery Power Management System – Measured Results 43**
Test Setup 43
Micro-Battery Current Charger 45
Micro-Battery Voltage Charger 52
Micro-Battery Voltage Monitor 56

V. **Conclusion 60**
Conclusion 60
Future Work 60
Bandgap Voltage Reference 61
Beta-Multiplier Current Reference 66
4-Bit Flash ADC 68

LIST OF REFERENCES 72

APPENDIX 77

VITA 79

LIST OF FIGURES

Figure Page

Figure 1.1: Reduction in spacecraft mass and volume over time. 2
Figure 2.1: Cascode current mirror. 8
Figure 2.2: Wide-swing, low-voltage cascode current mirror. 9
Figure 2.3: Self-biased cascode current mirror. 10
Figure 2.4: Minch cascode current mirror. 11
Figure 2.5: Schematic of series voltage regulator. 12
Figure 2.6: Basic flash ADC architecture. 14
Figure 2.7: Single stage of pipelined converter. 15
Figure 2.8: Successive-approximation (SAR) ADC architecture. 16
Figure 3.1: Beta-multiplier current reference topology. 18
Figure 3.2: Drain current plotted from weak to strong inversion. 18
Figure 3.3: Hole mobility in bulk silicon vs. temperature. 21
Figure 3.4: Comparison of R_{sq} calculated using Arora's mobility equation, SPICE simulations, and measured results, all compared to thermal voltage U_T. 23
Figure 3.5: Current-mode DAC topology. 24
Figure 3.6: Sample and hold circuit illustrating charge injection. 25
Figure 3.7: Input slew-rate control circuit applied to each of the DAC inputs. 27
Figure 3.8: Simulation of input slew-rate control circuit. 27
Figure 3.9: Simulation results of start-up and active conditions of DAC output. 28
Figure 3.10: V_{GS}-multiplier biasing the LVCCM of the DAC output stage. 30
Figure 3.11: I_{DS} vs. V_{DS} curve showing regions of operation of an *n*MOS transistor. 32
Figure 3.12: Simulated DC sweep of current charger output at room temperature for selected input codes. 33
Figure 3.13: Simulation of DAC mid-scale output plotted against temperature. 34
Figure 3.14: Calculated *IC* of M_1 and M_2 devices of beta-multiplier current reference. ..35
Figure 3.15: Regulated voltage source using a voltage amplifier. 36
Figure 3.16: Two-bit flash ADC architecture. 38
Figure 3.17: Comparator architecture used in the flash ADC. 39
Figure 3.18: Simulation of comparator hysteresis window with V_{inv} = 2.5 V. 40
Figure 3.19: Simulation of propagation delay of comparator. 41
Figure 3.20: Flash ADC simulation by sweeping V_{Batt}. 42
Figure 4.1: System level diagram of micro-battery power management system. 43
Figure 4.2: Copper ground plane test board used in taking measurements. 44
Figure 4.3: Off-chip 10-µA bias current generator. 45
Figure 4.4: Measured DC sweep of V_{Batt} at room temperature for each DAC code. 46
Figure 4.5: Measured transfer cure of the programmable current charger. 48
Figure 4.6: Measured DNL of programmable current charger. 48
Figure 4.7: Measured INL of programmable current charger. 49
Figure 4.8: Temperature comparison of 50 and 750-nA I_{charge} currents. 50
Figure 4.9: Comparison of current charger output and p-well R_{sq}. 51

Figure 4.10: Ideal and calculated PTAT voltage reference across temperature. 52
Figure 4.11: Cadence properties window of resistor. 55
Figure 4.12: Current charger output for a mid-scale input to show glitches. 56
Figure 4.13: Simulation of overall gate capacitance of comparator input devices. 57
Figure 4.14: Full system-level transient simulation of power management IC. 58
Figure 4.15: Chip micrograph of the micro-battery power management IC. 59
Figure 5.1: Bandgap voltage reference circuit. 62
Figure 5.2: Voltage difference of 1× and 8× diode sizing for ESD and PN diodes.....64
Figure 5.3: Measured I–V characteristics of 1× and 8× ESD diodes.....65
Figure 5.4: Simulation of bandgap reference temperature performance. 66
Figure 5.5: Beta-multiplier self-biased current reference. 67
Figure 5.6: 4-bit flash ADC architecture with priority encoder.....69
Figure 5.7: Transient simulation of 4-bit flash ADC with priority encoder. (Digital output levels scaled to show transitions—normally logic '1' = 3.3 V.).....70
Figure A-1: Design flow process…… 78

CHAPTER 1

INTRODUCTION AND OVERVIEW

Introduction

Recent successes in the effort to miniaturize spacecraft components using microelectromechanical systems (MEMS) technology, integrated passive components, and low power electronics have driven the need for very low power, low profile, low mass micro-power sources for micro/nanospacecraft applications [1]. The power sources chosen to combat this problem are rechargeable, thin-film and micro-scale batteries prepared using microelectronic fabrication techniques. A number of thin-film micro-batteries have been documented in literature and of these, rechargeable lithium (Li) batteries have shown the best performance of cycle life and shelf life [2]. These Li-Ion micro-batteries are proving themselves to be useful in more applications than expected.

Due to the complications and safety requirements needed to send a human into deep space, unmanned space flights aimed at exploring the far reaches of the universe are underway. However, the cost of launching a spacecraft into outer space is proportional to its mass, so efforts are being made to achieve the goal of "microspacecrafts" as shown in Figure 1.1. Power electronics generally contribute considerably to the mass and volume of the total avionics systems, which can be problematic for applications leveraging miniaturized components [1]. As power electronics miniaturize, the power sources must also decrease in size in order to meet this goal of microspacecrafts.

Micromachining manufacturing methods have made MEMS-based sensors and actuators a reality and there is a push for power sources small enough to fit on a microchip to power them [2]. Because of this, there is a growing interest in the development, fabrication, and volume manufacturing of these micro-power sources [3]. With the enhancement of power sources on the same microchip as MEMS, energy efficiency could be maintained due to low power transmission losses, cost would decrease due to reduced complexity of electrical connections and packaging, and the

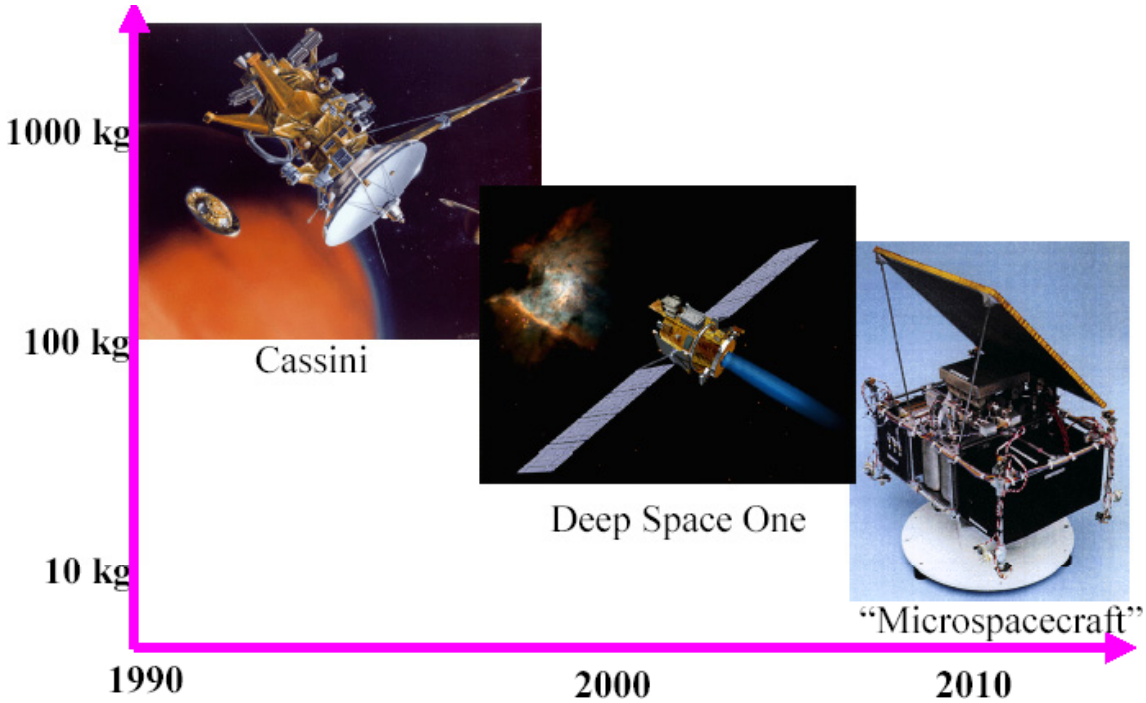

Figure 1.1: Reduction in spacecraft mass and volume over time.

micro-power cells could be arrayed to achieve different combinations of operating voltages for an integrated circuit [2].

Circuit designers could also benefit from the use of micro-battery structures. One possibility in the case of low current applications is for a micro-battery to act as an on-chip power supply [4]. Something being investigated at JPL is the use of thin-film micro-batteries to act as momentary CMOS memory backup in the event of system power failure [1]. Analog circuit designers could also utilize micro-batteries as voltage shifters or as on-chip, low noise, reference voltages. This is a vast area that has yet to be explored fully for use in CMOS analog circuit design for system on a chip (SOAC) applications.

As one can see, the use of a micro-battery structure is only limited by the imagination of the user. The one thing missing from all the literature dealing with micro-power sources, however, is the design of a power management IC capable of recharging these micro-batteries.

Overview

This thesis provides a detailed overview of a power management IC designed for solid-state, Li-Ion micro-batteries using a standard 3.3-V/0.35-µm, single-poly, PD-SOI process. The power management design consists of a programmable current charger, a constant voltage charger, and a voltage monitoring circuit that reads the micro-battery's voltage during the current charging process. The programmable current charger is designed using a temperature stable, low-level current reference that feeds into a current-mode digital-to-analog converter (DAC), which uses a new technique to bias low-voltage cascode current mirrors (LVCCM). The voltage charger is designed using voltage amplifier techniques and the voltage monitoring circuit is designed using a low-resolution flash analog-to-digital converter (ADC) architecture.

Contained in this thesis are four main sections. Chapter 2 starts with a brief description of the micro-battery structures that are currently being developed by researchers at JPL. Also included in this chapter are descriptions of the different circuit designs that were considered when investigating the design of this micro-battery power management system.

Chapter 3 provides an in-depth analysis of the topologies chosen to implement this system including first-order theory and simulation results where applicable. A comparative discussion of alternate topologies is also presented.

Chapter 4 gives the measured results achieved from first-run silicon as well as presents the test setup used in taking these measurements. The measured results are compared against theoretical and simulated results obtained from the previous chapter.

Chapter 5 provides conclusions for this work and details the enhancements that were made for the first revision of this system. Figure A-1 contains the typical design flow used in designing each component of this power management IC.

CHAPTER 2

MICRO-BATTERY POWER MANAGEMENT SYSTEM CONCEPTS

Micro-Battery Structure

The batteries that are to be charged with this power management system are thin-film, solid-state, Li-Ion micro-batteries. Numerous papers have been written on processing procedures and characterization of these types of micro-batteries [1]–[8]. The power management IC presented in this thesis is targeted for use on the micro-batteries developed at JPL.

JPL researchers have been trying to develop a processing technique aimed at integration of micro-battery cells directly on-chip. The fabrication process used by JPL is based upon the Oak Ridge National Laboratory (ORNL) process. This process calls for annealing the sputtered films at 700°C in order to crystallize the cathode film [1]. This high temperature anneal makes it almost impossible to fabricate cells on temperature sensitive substrates (such as ICs), so JPL has pushed for developing a lower annealing temperature process on the order of 300°C, which is more compatible with CMOS technology. Using this lower annealing temperature, they have fabricated cells with slightly reduced capacity cathodes but maintained excellent cycle life.

Just recently, JPL has found an improved method of fabrication for micro-battery cathodes that requires less processing steps [7]. The energy storage capability of a micro-battery is limited by the amount of active material present [2]. The volume of active electrode material that can be deposited by sputtering is limited and the process is slow. The new method uses electrophoretic deposition (EPD), which is much faster and has shown to produce cells with a factor of ten increase in discharge capacities [7].

Micro-batteries that have been made available for this project have a reported capacity of 50 nAh. The full-rated voltage for a cell is 4.25 V with a normal operating condition between 3 and 4.25 V. A cell is overcharged if its voltage is above 4.4 V and in deep discharge for a voltage level below 2 V. The normal charge rate is 50 nA or 1 capacity (1 C) of the micro-battery with efficient charge rates as low as 0.1 C [5].

Two charging methods are needed when charging a Li-Ion micro-battery—current charging and voltage charging [5]. The necessity to charge micro-batteries at or below 50 nA requires the design of a low-level current reference. The voltage charger is given the task of maintaining a 4.25-V voltage bus to trickle charge a micro-battery to complete its charging cycle once it reaches full voltage capacity, or storing unused micro-batteries. Since a fully charged micro-battery is 4.25 V, this system has to operate with a 5-V supply, but recall that a 3.3-V/0.35-µm technology is being used to fabricate this system. This requires the use of dual V_{DD} supply rails denoted by V_{DDH} and V_{DDL} for the 5 and 3.3-V supplies, respectively, and carefully designed circuit topologies.

The micro-battery's voltage state during the current charging process has to be monitored so that when the micro-battery reaches 4.25 V, it can be transitioned from current charging to voltage charging. A low-resolution ADC was chosen to create the digital output representation of a micro-battery's voltage state.

Current Source

Current references are one of the basic building blocks of analog circuitry. Requirements desired from most current references are high output impedance, low temperature sensitivity over a broad temperature range and good power supply rejection. CMOS current references that perform well over temperature or require small area to implement have been reported [9]–[14]. For this power management system, it is desired to have a low-level current reference that occupies a small area and is insensitive to temperature variations.

In MOS transistors, the temperature dependence of the drain current originates from various physical parameters such as threshold voltage (V_{TH}), mobility (μ), and thermal voltage (U_T). The mobility dependence of carriers in the conduction channel on temperature is given by

$$\mu(T) = \mu(T_0) \times \left(\frac{T}{T_0}\right)^{-1.5} \tag{2.1}$$

where T is the absolute temperature in Kelvin and T_0 is 300K [15]. Some circuits reduce the effects of temperature on mobility by generating a proportional-to-absolute temperature (PTAT) voltage reference that can be used to produce an output current that is proportional to $T^{0.5}$, and therefore only slightly increases with temperature [10].

A common way to produce a PTAT voltage reference is to use bipolar transistors, but the only bipolar transistor available in a standard CMOS process is a parasitic vertical bipolar. These vertical bipolar transistors are poorly modeled, so an all CMOS topology seems better suited to design a current reference. Sansen *et al.* developed an 800-nA current reference based off a bipolar PTAT voltage source implemented using floating MOSFETs operating in weak inversion [10]. This circuit uses several weakly inverted MOSFETs to generate the PTAT source, which in turn requires a large aspect ratio for those devices, consuming a large amount of chip area. Measured results of this system show 3% temperature dependence between 0 and 80°C with a MOSFET acting as the current defining element.

To further reduce the temperature insensitivity of this type of design, Lee and Park [11] tried to completely cancel out the mobility dependence in the output current by multiplying a current that is proportional to mobility and a current that is inversely proportional to mobility with a CMOS square root circuit. The CMOS square root circuit uses four *p*MOS transistors operating in weak inversion, which again requires a large area. The result of this work is a 1.7% variation of output current (285 nA at 60°C) over a temperature range 0–75°C.

A well-known current reference proposed by Vittoz and Fallrath [9] is expanded upon by eliminating the need for a space-consuming resistor [12]. In lieu of a resistor, the new topology calls for a MOSFET operating in triode or linear mode of operation. This circuit topology uses weak inversion MOSFETs to set up a PTAT voltage source across the linear MOSFET. This circuit is capable of producing extremely low reference currents (5 nA with a 3-V supply at 20°C), but occupies a large area due to the aspect ratio of the linear MOSFETs needed to create a large resistance used in generating a low-level reference current.

Another possible method of generating an on-chip current reference is explored in [13] using a switched-capacitor network. The motivation for a switched-capacitor circuit is to avoid relying on physical parameters of MOS transistors and IC resistors to set an accurate reference current. In addition, capacitance per unit area can be substantially independent of temperature. The value of the reference current generated using Torelli's switched-capacitor circuit is given by [13]

$$I = \frac{C \times V_{Ref}}{f_{clk}} \tag{2.2}$$

where C is the value of the capacitance, and f_{clk} is the clock frequency in Hz. One of the problems associated with this method of current generation is a ripple in the output current at the switching frequency. This output current is also directly dependent on the reference voltage (V_{Ref}) applied, but can be adjusted by varying the clock frequency.

Instead of trying to just obtain first-order temperature effect cancellation of a current reference, some designs try to compensate for second-order temperature effects as well [14]. The proposed circuit by Fiori and Crovetti uses only five MOSFETs operating in strong inversion saturation and two resistors to cancel second-order temperature effects. Simulated results of this circuit show that a 13.65-μA reference current with less than 0.5% variation of current output over the temperature range from –30 to 100°C has been developed in a 0.35-μm process. This circuit can be very compact because it requires only MOSFETs operating in strong inversion saturation to be used, which normally translates to transistors with small aspect ratios.

Once a low-level reference current topology has been chosen, the reference current can be scaled accordingly using weighted current mirrors. The application for this power management system dictates that it should be able to charge multiple micro-batteries at one time. This can be achieved by designing a low-resolution current-mode DAC to scale the reference current. We set the limit for the number of micro-batteries to be charged at once to 15, which means the DAC needs to be capable of maintaining 4-bit accuracy if binary weighted current mirrors are used.

When charging either a single or multiple micro-batteries at a time, the current charging output must remain a high impedance node to efficiently deliver current to the micro-battery. Cascode current mirrors provide an improvement of output resistance over simple current mirrors. The small-signal output resistance (R_o) of the cascode current source in Figure 2.1 is given by

$$R_o = r_{o2}(1 + g_{m2} r_{o4}) + r_{o4} \approx g_{m2} r_o^2 \tag{2.3}$$

where $r_o = r_{o2} = r_{o4}$ is the MOSFET small-signal output resistance and g_m is the MOSFET small-signal transconductance. If M_1 and M_2 were removed from Figure 2.1, a simple current mirror would be left whose small-signal output resistance would be equal to r_{o4}.

Although this cascode current mirror provides high output impedance, it does not allow for a high output voltage swing. The dynamic range of this cascode current mirror with respect to V_{DD} is limited to less than

$$V_{OUT} = V_{DD} - 2V_{SD,Sat} - |V_{THP}| \approx V_{DD} - 1.3V \tag{2.4}$$

where $V_{SD,Sat}$ is the saturation voltage of a *p*MOS transistor and V_{THP} is the *p*MOS threshold voltage. Recall that the full voltage capacity of a micro-battery is 4.25 V. If the 5-V supply were used to bias this cascode current mirror, there would not be enough

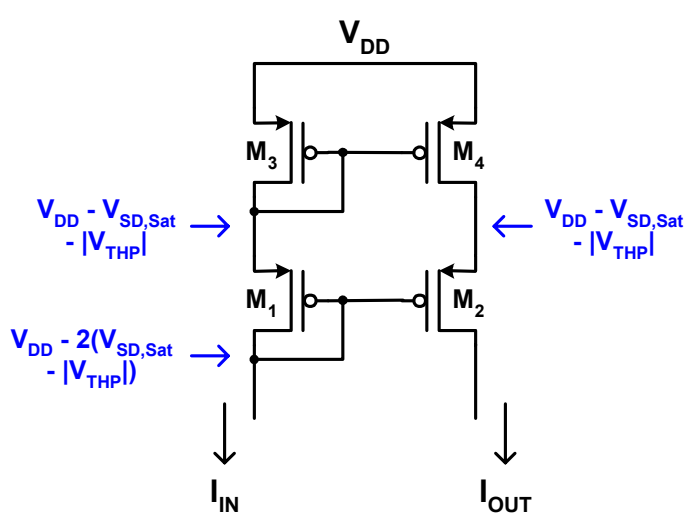

Figure 2.1: Cascode current mirror.

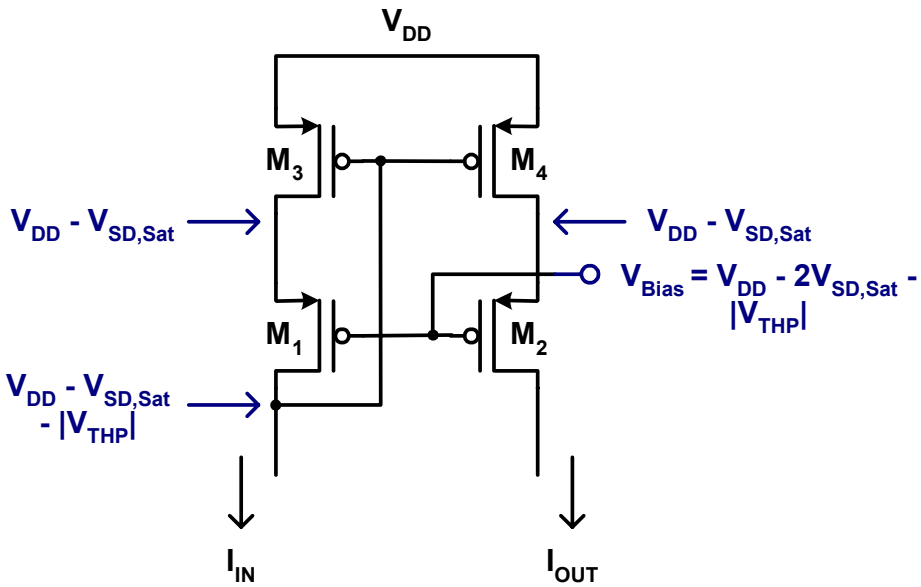

Figure 2.2: Wide-swing, low-voltage cascode current mirror.

headroom to charge a micro-battery fully with this current mirror. Alternate schemes of biasing cascode current mirrors for wide-swing or low-voltage applications exist [16]–[20].

The typical wide-swing, low-voltage cascode current mirror is presented in Figure 2.2. For this wide-swing current mirror to work efficiently, V_{Bias} must be set at $V_{DD} - 2V_{SD,Sat} - |V_{THP}|$, leaving a $V_{SD,Sat}$ across mirror devices M_3 and M_4. This is called a wide-swing current source because the minimum voltage across the current source for proper operation is $2V_{SD,Sat}$ [16], which is one threshold voltage drop less than the regular cascode mirror shown in Figure 2.1. This current mirror is dependent on the voltage of V_{Bias} remaining constant and only works well for a small variation of input current. For a large change of the input current, additional circuitry is required to track the V_{SG} of the cascode devices M_1 and M_2, so the current mirror's output characteristics do not vary [19].

One approach to increase the dynamic range of a current mirror without extra biasing voltages is the self-biased structure shown in Figure 2.3. Assuming that the threshold voltage of the devices are similar, [18] shows that the mirror devices M_3 and M_4

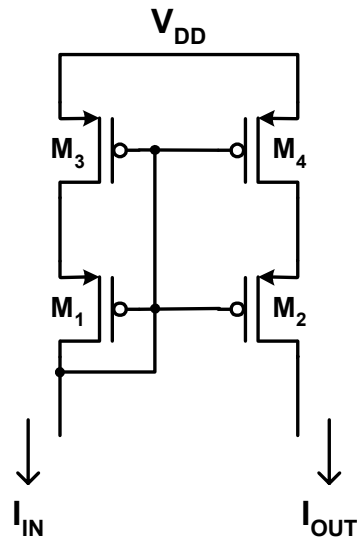

Figure 2.3: Self-biased cascode current mirror.

are in the triode or linear region and the cascode devices M_1 and M_2 are in saturation. This topology allows for simple implementation and high output voltage swing, but having the mirror devices biased in the linear region lead to some disadvantages [19]. Linear mode MOSFETs have a high susceptibility to transistor mismatch causing current gain errors and output impedance is reduced compared to a conventional cascode current mirror.

Minch developed a circuit that biases the mirror devices in a cascode current mirror right at the edge of saturation, thus optimizing its dynamic range [20]. A schematic of this circuit is shown in Figure 2.4. The values of the aspect ratios n and m are described in the paper. The circuit operates by using the input current and a ratio of the input current to set up an exact $V_{SD,Sat}$ voltage drop across device M_4. M_5 then acts as a level shifter, which creates a voltage of $V_{DD} - V_{SG} - V_{SD,Sat}$ on the gate of M_5. The gate voltage on M_5 is used to bias the gate voltages of the cascode devices M_7 and M_9 of the current mirror. The mirror devices M_6 and M_8 in the output of the current mirror now have the optimum headroom ($V_{SD,Sat}$) to provide for the largest dynamic range possible from a cascode current mirror.

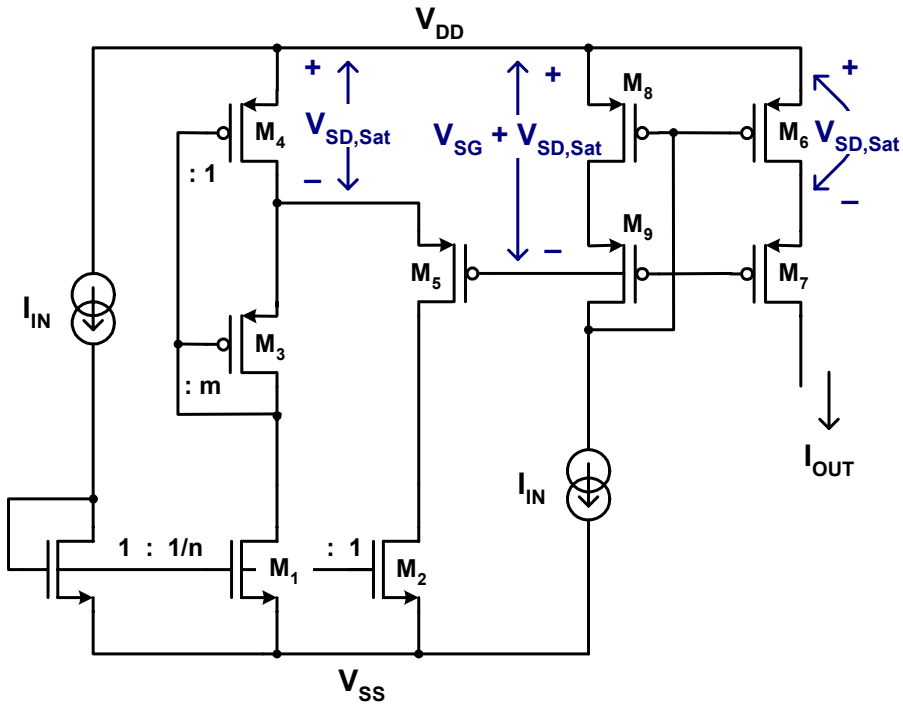

Figure 2.4: Minch cascode current mirror.

An advantage of this circuit is that a replica of the input current is being used to generate the $V_{SD,Sat}$ voltage reference. This means that as the input current changes over a wide range, the $V_{SD,Sat}$ voltage reference will adaptively bias itself to accommodate any level of inversion—weak, moderate, or strong. One disadvantage of this circuit is reduced output impedance of the current mirror compared to a normal cascode current mirror because the mirror devices are biased right at the edge of saturation. This will be explained in more detail in Chapter 3.

Voltage Source

Once a micro-battery has been current charged up to 4.25 V, it has to be transitioned to a voltage charger to complete its charging process. The voltage charger needs to output a constant voltage of 4.25 V and be able to trickle charge and/or store multiple micro-batteries attached to it at one time. The exact values for resistance and capacitance of these micro-batteries have not yet been established, but the resistance is

estimated to be as high as 1 GΩ. For this reason, extra caution needs to be taken in designing the voltage source to handle a large variation of capacitance and resistance.

An ideal voltage amplifier provides infinite input impedance, zero output impedance, and a steady output voltage regardless of loading conditions. If a voltage sample-voltage sum feedback amplifier is designed properly, the voltage gain is determined by the feedback network, the output resistance (R_o) is decreased, the input resistance (R_i) is increased, and the voltage gain remains constant for changes in circuit parameters [21]. This type of configuration is ideally suited for voltage amplifiers.

Voltage regulators are widely used components that accept a poorly specified DC input voltage and produce from it a constant, well-specified output voltage that can then be used as a supply voltage for other circuits [22]. The most common voltage regulator is the series regulator shown in Figure 2.5. The output of this voltage regulator is based off the ratio of the resistors and the reference voltage (V_{Ref}) given by

$$V_{Out} = V_{Ref} \frac{R_1 + R_2}{R_2} \tag{2.5}$$

Low drift and offset are essential for the op-amp so that the output voltage (V_{Out}) is as stable as possible. Very low output impedance will be produced at V_{Out}, which is a requirement for a good voltage source.

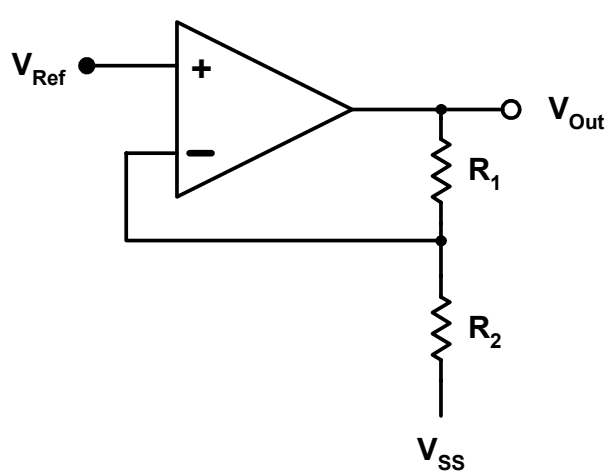

Figure 2.5: Schematic of series voltage regulator.

The voltage sources described above are generally used to drive low resistive loads with a large amount of current output. In contrast, for this application of voltage charging micro-batteries, a high output current availability is not needed from the voltage regulator. The micro-batteries would have been current charged at a rate of 50 nA before they are transitioned to the voltage charger. As long as the voltage charger node is at the same potential as the micro-batteries right before they are connected, each micro-battery should not draw more than 50 nA of current from the voltage charger node. The purpose of the voltage charger is to provide a decaying current supply to each micro-battery until their full capacity of 50 nAh is reached. In the worst-case scenario, the voltage charger would need to be able to provide 50 nA of current to each of the 15 micro-batteries at one time.

Low-Resolution ADC

To be able to monitor the micro-battery voltage while current charging, a low-resolution ADC is required. The accuracy of a digitized signal is dependent on the number of samples taken and the resolution, or number of quantization levels, of the converter [16]. The resolution required of an ADC is dependent on its application. The finer the range of interest, the more resolution required. The sampling rate of an ADC is defined by the Nyquist criterion, which states that the sampling rate must be at least two times the highest frequency of the analog signal for it to be reconstructed accurately in the digital domain. The analog signal that is of interest in this application is the slow, continuous ramping of the micro-battery voltage as it is being current charged. Current charging times for micro-batteries have been reported to be greater than 30 minutes [5].

Probably the four most popular architectures for ADC conversion are the flash, pipeline, successive approximation (SAR), and sigma-delta ($\Sigma\Delta$) converters. Each of these ADC converters is intended for different applications, but all of them require one or more steps involving comparison of an input signal with a reference [17].

The flash converter is the most straightforward ADC architecture. It requires a set of 2^n comparators to measure an analog signal to n-bit resolution. An example of a flash ADC architecture is shown in Figure 2.6, where FS is the full-scale input and A_{IN} is the

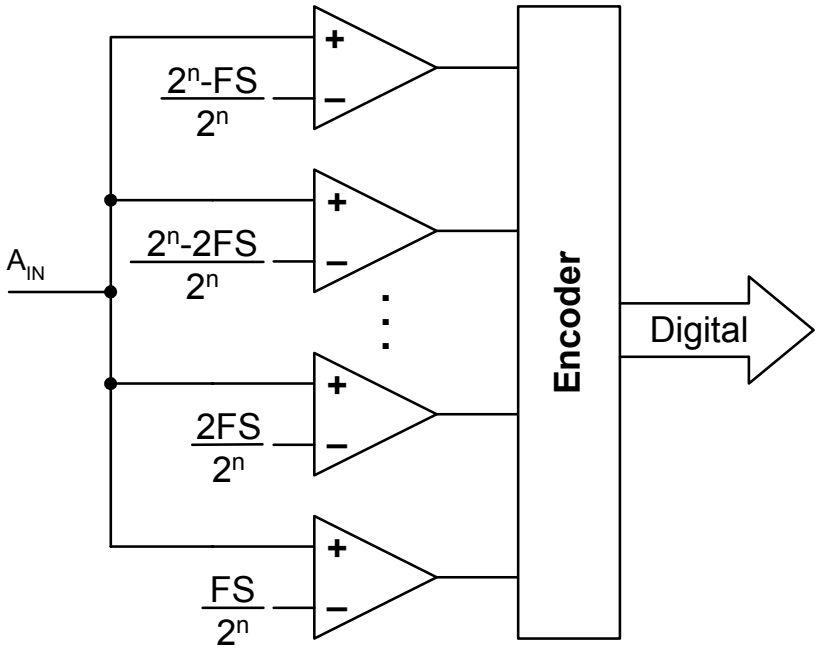

Figure 2.6: Basic flash ADC architecture.

analog input. For a 3-bit flash ADC, eight comparators would be needed, each of which is biased with a discrete voltage value spaced 1 LSB apart. The analog input signal is compared against the discrete voltage values to simultaneously generate 2^n discrete digital output states. The digital output is in the form of thermometer code and is usually converted to binary form using an encoder. The benefit of the flash architecture is that the conversion only takes one ADC cycle. The disadvantage of this type of architecture is the large number of carefully matched and properly biased comparators needed to generate a high-resolution output.

Pipelined or pipelined-flash converters divide the conversion process over several consecutive stages. Each stage normally consists of a sample-and-hold circuit, an *m*-bit ADC (flash converter), and an *m*-bit DAC. The *m*-bit flash converter converts the sampled signal from the sample-and-hold circuit to digital data. This digital output forms one of the significant bits of the digital output. The same digital output is fed back into the DAC whose output is subtracted from the original sampled signal. The residual analog signal is then amplified (*k*) and sent to the next stage in the pipeline to undergo the

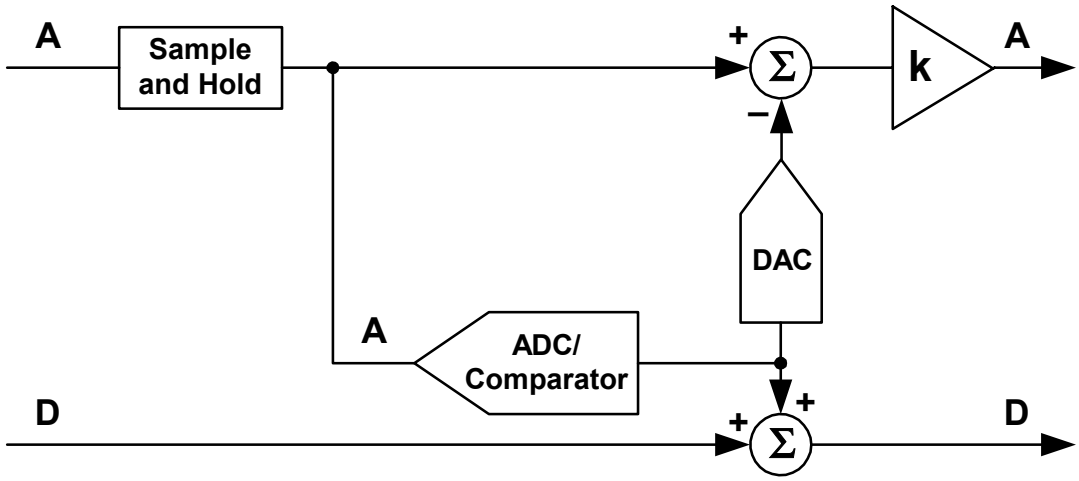

Figure 2.7: Single stage of pipelined converter.

same process. This process continues until the desired resolution is acquired. An example of a single stage of a pipelined ADC is shown in Figure 2.7.

The pipelined converter with p pipeline stages, each with an m-bit flash converter, can produce a resolution of $n = p \times m$ bits using $p \times (2^m – 1)$ comparators [17]. This corresponds to a higher resolution of pipelined converters compared to flash converters for the same number of comparators. The total conversion time increases though from one to p cycles for pipelined converters. However, since each stage samples and holds its input, p conversions can take place simultaneously so the total throughput of the pipelined converter can be equal to the flash converter, now with added p cycle latency.

The SAR converter uses a single comparator over many cycles to generate its digital output. The SAR compares the unknown sampled voltage against a known voltage. If the sampled voltage is higher than the known voltage, the SAR will set the significant bit. If the sampled voltage is lower than the known voltage, the SAR does not set the significant bit. This process repeats by using successively smaller weights in binary progression until the desired resolution, n, is reached. An example of a SAR ADC is shown in Figure 2.8. The limitation of the SAR is that it takes n comparison cycles to generate n-bit resolution, compared to p cycles for the pipelined converter and one cycle for the flash converter.

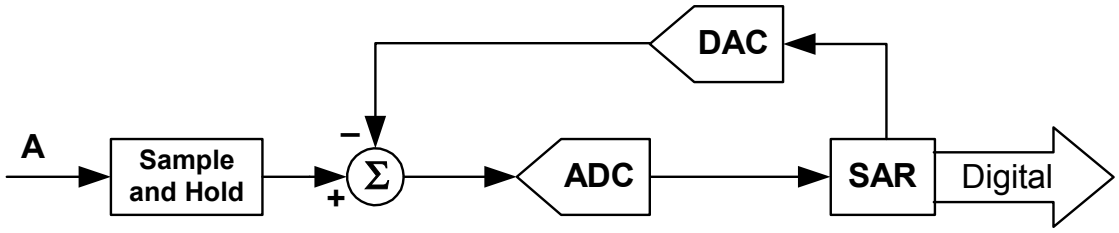

Figure 2.8: Successive-approximation (SAR) ADC architecture.

The ΣΔ converter is advantageous to use when a high resolution, on the order of 20+ bits, is needed. It is able to have such high resolution because of a process known as noise-shaping in which the low-frequency noise components are pushed to higher frequencies beyond the input signal bandwidth. The limitation of this type of converter is the latency associated with its digital output, which is significantly higher than the other architectures presented, and the digital filtering overhead required to produce a parallel-bit binary output word.

Now that some possible circuit topologies have been investigated, this information can be used in collaboration with our system requirements to design a power management IC for micro-batteries. The three main components of the design are a programmable low-level current charger, a constant voltage charger, and a voltage monitoring circuit.

CHAPTER 3

DESIGN OF MICRO-BATTERY POWER MANAGEMENT SYSTEM COMPONENTS

Programmable Current Source

To be able to charge micro-batteries effectively, a low-level current source with a high output impedance across a wide range of output currents is desired. This output current also needs to have low temperature sensitivity so that it is able to function accurately in a variety of environments. For these reasons, the current source chosen for this project encompasses two different parts; a temperature stable, low-level current generator (400 nA) and a 4-bit current output DAC with a novel output stage, dubbed the "V_{GS}-multiplier," which ensures a high output impedance over a large range of output current.

Current Generator

Different current reference circuits were discussed in the previous chapter, but one design stood out due to its low sensitivity to temperature variations when used for this application. Shown in Figure 3.1 is a beta-multiplier current reference with the *n*MOS devices M_1 and M_2 operating in weak inversion. This architecture of the beta-multiplier with weakly inverted devices functions as a PTAT voltage reference [9].

MOSFETs operating with a V_{GS} less than V_{T0} are said to be operating in weak inversion or sub-threshold mode as shown graphically in Figure 3.2. In this region of operation, diffusion current dominates and the drain current becomes an exponential function of the gate voltage. It is important to size M_1 and M_2 of Figure 3.1 such that for a given current level, the devices are guaranteed to remain in weak inversion in order for the PTAT reference to properly function.

To better illustrate analytically where the region of weak inversion exists, an inversion coefficient was first introduced by Vittoz [23] and then later expanded upon by Binkley *et al.* [24]. The simplified definition of inversion coefficient (*IC*) is

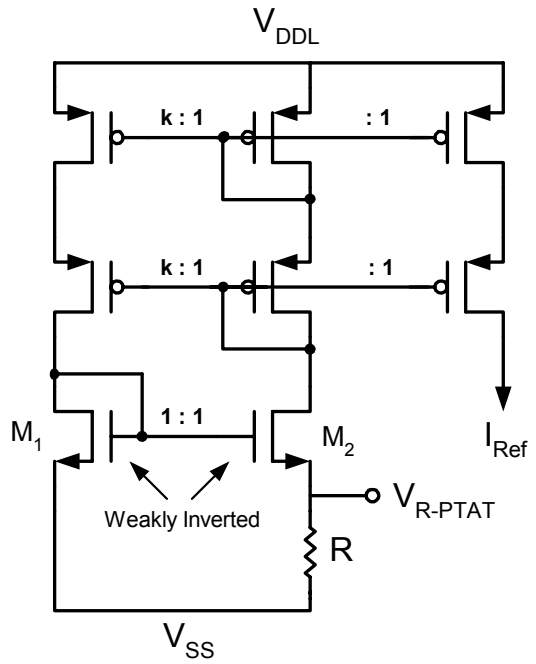

Figure 3.1: Beta-multiplier current reference topology.

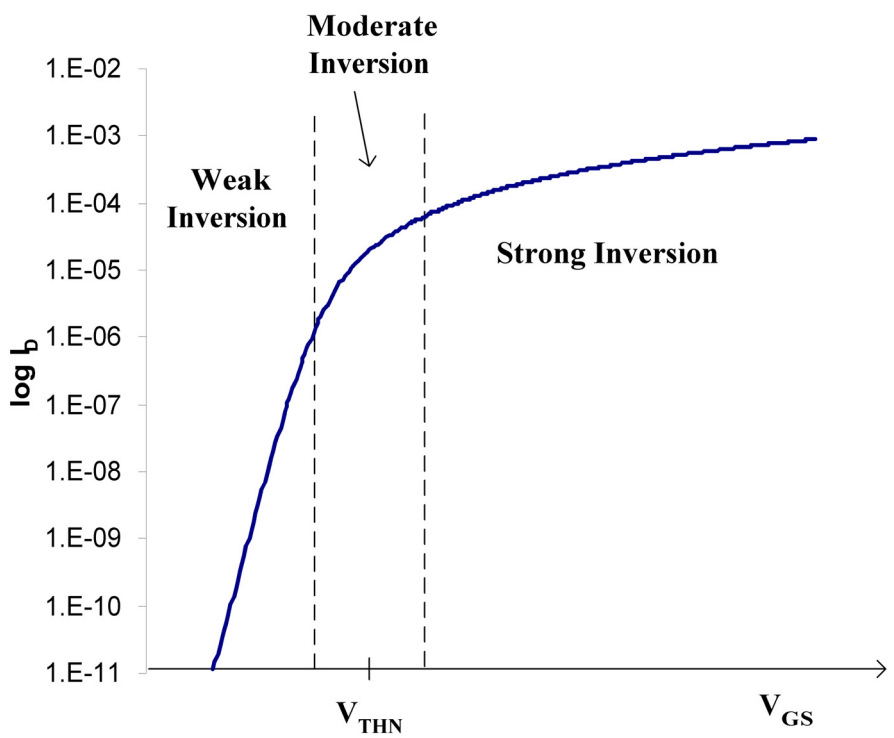

Figure 3.2: Drain current plotted from weak to strong inversion.

$$IC = \frac{I_D}{I_o\left(\frac{W}{L}\right)} \tag{3.1}$$

where I_D is the drain current, W and L are the effective channel width and length respectively, and I_o is a process dependent current known as the technology current. The technology current is defined as the drain current for a device with an aspect ratio of unity, $W/L = 1$, which is biased at the center of moderate inversion where $IC = 1$. According to Vittoz's definition [23], a device is weakly inverted if its IC is less than 0.1, moderately inverted for an IC between 0.1 and 10, and strongly inverted for an IC greater than 10. For this design, an aspect ratio of 120 was used to ensure that both devices would remain in weak inversion for drain currents less than 1 μA.

The equation for an n-channel MOSFET operating in weak inversion is given by [25]

$$I_{D,Weak} = 2n\mu_n C'_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{GS}-V_{THN})}{nkT}} \tag{3.2}$$

where μ_n is the electron mobility, C'_{ox} is the gate oxide capacitance per unit area, k is Boltzman's constant, T is the temperature in Kelvin, q is the electron charge, V_{THN} is the nMOS threshold voltage, and n is the process dependent sub-threshold slope factor. Summing the voltages around the bottom half of Figure 3.1 using Kirchoff's Voltage Law (KVL) yields

$$V_{GS1} = V_{GS2} + V_{R-PTAT} \tag{3.3}$$

where

$$V_{R-PTAT} = I_{D2} \times R = I_{Ref} \times R \tag{3.4}$$

Solving for V_{GS} from (3.2) gives

$$V_{GS} = nU_T \ln\left(\frac{I_{D,Weak}}{I_{DO}}\right) + V_{THN} \tag{3.5}$$

where U_T is equal to the thermal voltage (kT/q) and $I_{DO}=2n\mu_n C'_{ox} W/L$. Substituting (3.5) into (3.3) and solving for the PTAT reference voltage yields

$$V_{R-PTAT} = nU_T \ln\left(\frac{I_{D1}}{I_{D2}}\right) = nU_T \ln(k) = I_{Ref} \times R \qquad \textbf{(3.6)}$$

The cascode *p*MOS current mirror in Figure 3.1 provides the k ratio of the currents so that M_1 and M_2 devices have different drain currents allowing for a systematic V_{GS} offset. By sizing these two devices the same, it is possible to symmetrically layout the MOSFETs allowing for better matching, which will cause less error associated with random V_{GS} mismatch of the *n*MOS pair. For this design, a current ratio of $k = 2$ was implemented in the *p*MOS current mirror in order to limit the size of the resistor needed to generate a low-level reference current (I_{Ref}) of 400 nA.

P-well resistors with high sheet resistivity (ρ) exist in the SOI process selected to fabricate this power management system. This allows a low-level current to be produced without the required resistor consuming a large chip area. In addition, the temperature coefficient associated with the p-well resistor tracks that of the generated PTAT reference voltage to provide temperature stable operation of the current reference. For a different technology without a high resistivity p-well option, the PTAT reference voltage generated by the weakly inverted MOSFETs can be reduced by connecting the body terminals of M_1 and M_2 together. The new equation for the PTAT reference voltage would then be given by [9]

$$V_{R-PTAT} = U_T \ln(k) = I_{Ref} \times R \qquad \textbf{(3.7)}$$

The only difference between (3.6) and (3.7) is the absence of the sub-threshold slope factor in (3.7). This means that either an equivalent low-level reference current can be generated using a lower resistivity resistor option or a dimensionally smaller resistor can be implemented to generate the same I_{Ref}.

Mobility of bulk silicon in a semiconductor is determined by various scattering mechanisms. The two most important mechanisms are lattice scattering and impurity scattering [26]. Lattice scattering results from thermal vibrations of the lattice atoms at

any temperature above absolute zero. At higher temperatures, lattice scattering dominates and the mobility decreases with increasing temperature. The hole mobility in p-type, bulk silicon is given by [27]

$$\mu_p = 54.3T_n^{-0.57} + \frac{1.36\times10^8 T^{-2.23}}{1+\frac{N}{2.35\times10^{17}T_n^{2.4}}0.88T_n^{-0.146}} \quad \textbf{(3.8)}$$

where T_n is T/300 K and N is the impurity concentration. This equation was obtained by Arora *et al.* through experimental data over the temperature range 250 to 500K [27]. Due to the limitation of the temperature range in deriving (3.8), measured results of p-well resistors for this SOI process were obtained and compared against the derived equation as seen in Figure 3.3. Notice that the two curves track well within the 250 to 500K temperature range and then start to deviate at lower temperatures. This broad temperature range from –150 to 150°C was chosen for measurement purposes because of

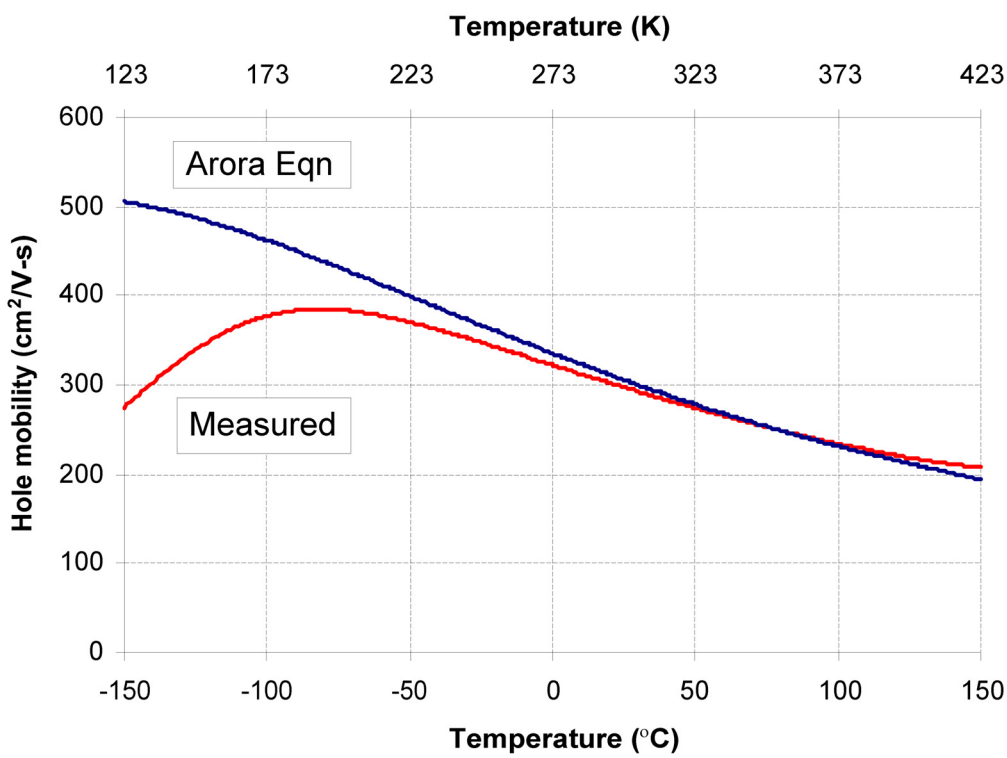

Figure 3.3: Hole mobility in bulk silicon vs. temperature.

the possible extreme environments in which this system might operate.

Resistivity, ρ, of bulk silicon is dependent on its mobility and concentration of majority carriers, p [26]:

$$\rho = \frac{1}{q\mu_p p} \tag{3.9}$$

The resistance per square (R_{sq}) for an IC resistor can be found by dividing its resistivity by the thickness of the silicon island. Once the R_{sq} is known, then an integrated circuit resistor of any value can be made by varying its aspect ratio.

$$R = R_{sq}\left(\frac{L}{W}\right) \tag{3.10}$$

Figure 3.4 shows a comparison plot of the resistance per square calculated using the mobility equation in (3.8), SPICE simulations with a process specific, first-order temperature coefficient term, and measured results across temperature. Also included in this figure is a plot of the thermal voltage across temperature. Recall from (3.6) that the only temperature dependent term in the PTAT reference is the thermal voltage, U_T. Notice how well the thermal voltage tracks the measured R_{sq} curve from 0 to 100°C, which in turn will provide the current reference generator with temperature stable operation over this temperature range. Simulation results of the current reference output show a 7% change in I_{Ref} from 0 to 100°C.

Current Output DAC

In order for the generated 400-nA reference current to be scaled to different levels to charge one to N micro-batteries in parallel, it is fed into a current-mode DAC. The 4-bit DAC consists of a series of binary-weighted current mirrors driven by MOSFET switches ($S3$–$S0$) and is shown in Figure 3.5. Using four bits, it is possible to produce 16 different continuous current output levels ranging from 0 to 750 nA in 50-nA steps. When charging micro-batteries at a normal rate of 1 C (50 nA), up to 15 micro-batteries can be charged simultaneously given a full-scale input to the DAC.

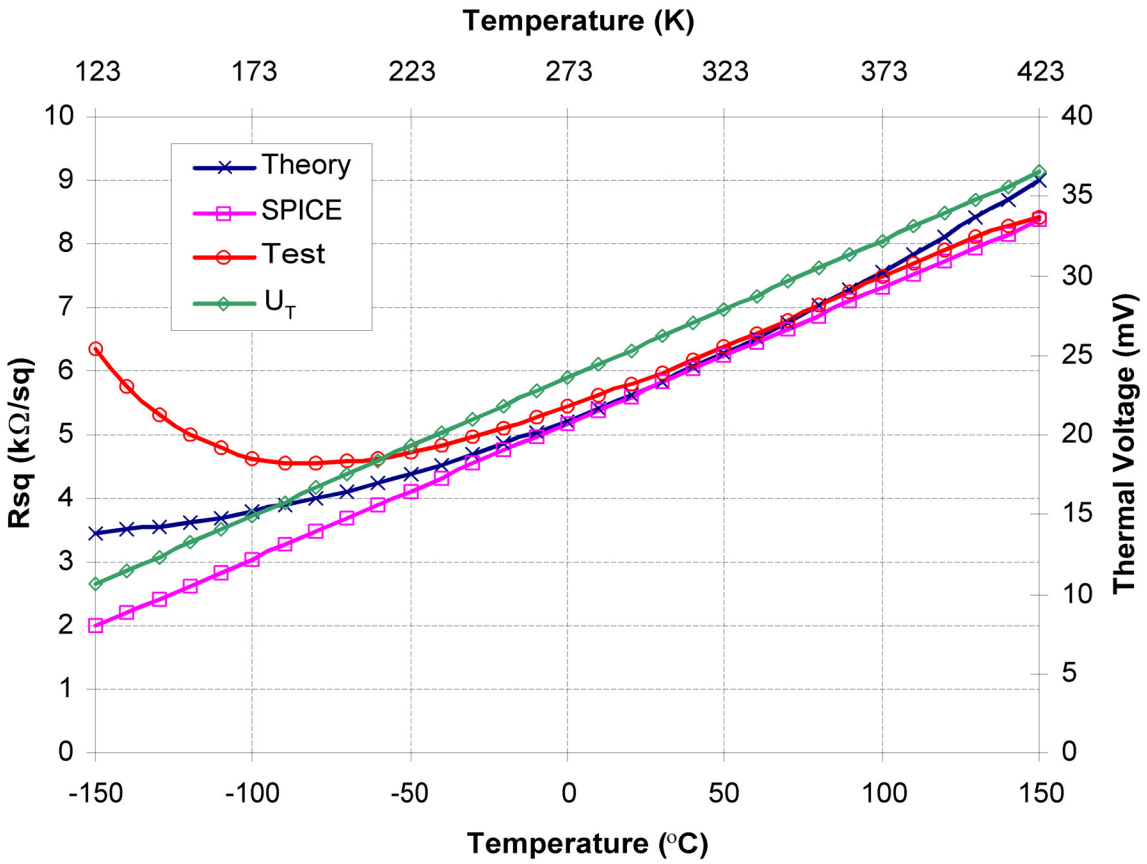

Figure 3.4: Comparison of R_{sq} calculated using Arora's mobility equation, SPICE simulations, and measured results, all compared to thermal voltage U_T.

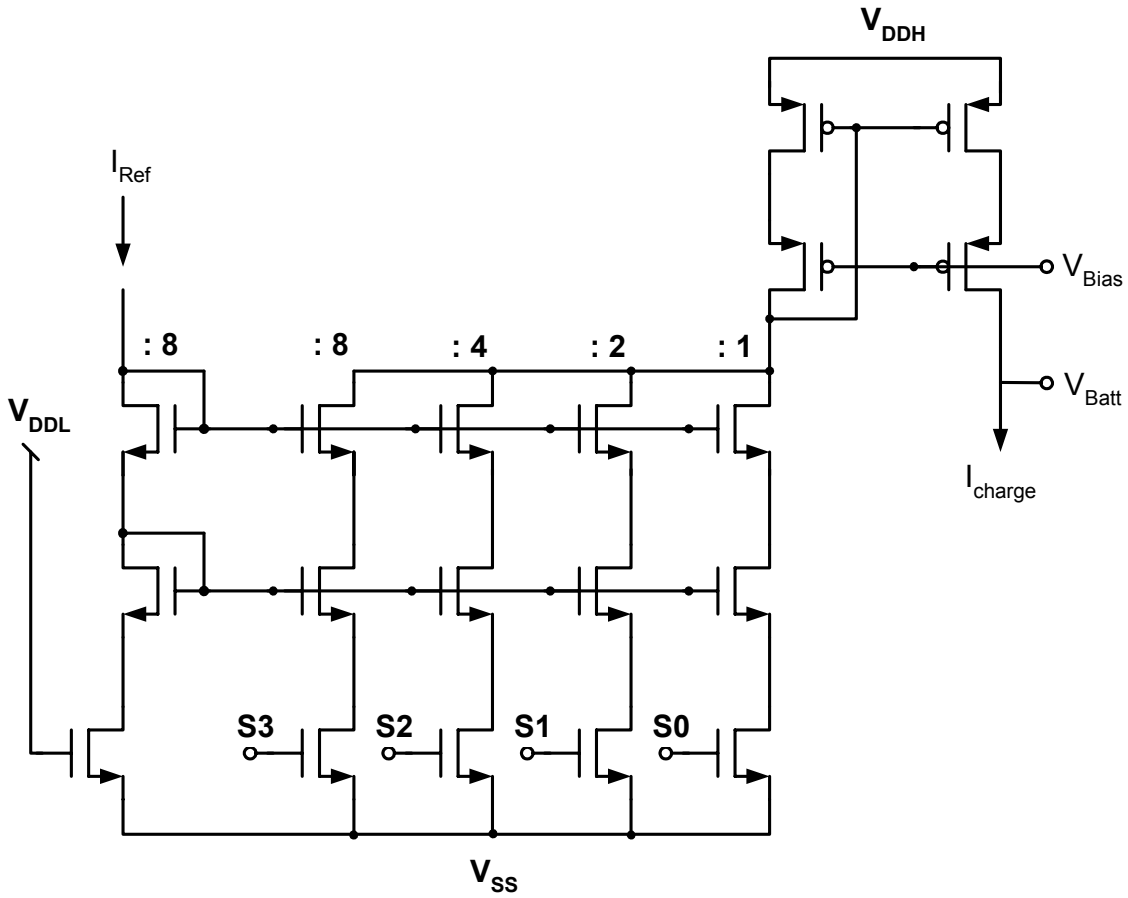

Figure 3.5: Current-mode DAC topology.

Another key component to this design is the ability to interchange between continuous current charging and pulse-width modulated (PWM) current charging. By applying a PWM voltage input to the switches of the DAC, it is possible to charge micro-batteries at an average rate lower than that made possible by the least significant bit (LSB) of the DAC (50 nA). For instance, a 10% duty cycle input can be applied to *S*0 of the DAC producing an overall effect of charging at 5 nA or a 0.1 C rate. Experimental results have shown that pulse-charging increases the cycle life of Li-Ion batteries due to improved replating of Lithium [28].

Most often charge injection issues do not arise unless dealing with a sample and hold topology where switched capacitors are utilized. For the sample and hold case, shown in Figure 3.6, the inversion layer charge is dumped into the holding capacitor when the switch is opened. The error associated with this type of setup is a positive voltage spike at the output as the hold capacitor (C_H) is injected with a small surge of current. The problem then of course is how to minimize the inversion layer charge, which will in turn minimize errors associated with charge injection. Usually, the effect of charge injection when a switch is closed is not taken into consideration because the signal source is driving C_H through the MOS switch.

Wegmann *et al.* [29] show that a rapid variation of the gate voltage causes a variation of the MOSFET surface potential because the amount of mobile charges cannot change instantaneously. The surface potential induces an immediate variation of the depletion width, which compensates the excessive charge. Equilibrium corresponding to the new gate voltage is reached by the subsequent charge flow to drain and source. This

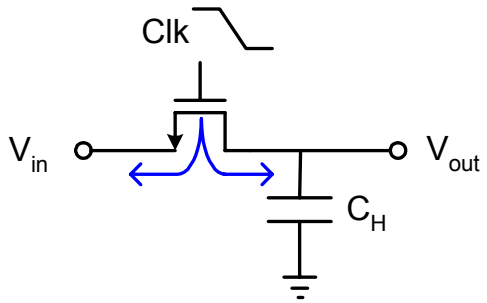

Figure 3.6: Sample and hold circuit illustrating charge injection.

is "charge injection." This undesirable effect had to be examined and minimized for this system since a low-level output current is desired and severe current output transients could damage micro-batteries.

The equation for charge injection is given by [30]

$$Q_{ch} = W \times L \times C'_{ox}\left(V_{GS} - V_{TH}\right) \tag{3.11}$$

where Q_{ch} is the total charge in the inversion layer. From this equation, it is clear that the physical size of the switch and the V_{GS} voltage are both factors that the designer can manipulate to minimize the charge in the inversion layer. What is not evident in this equation, however, is how the charge is shared between the source and drain of the device. In most cases, it is assumed that half the excess charge is shared equally between the source and drain. In reality, the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as the impedance seen at each terminal to ground and the transition time of the clock [29].

To help minimize the total charge in the inversion layer of the input switches in the DAC, the lower 3.3-V supply voltage, V_{DDL}, was used as the switching voltage instead of the higher 5-V supply voltage, V_{DDH}. In addition, all the switches were sized identically instead of sizing them with their respective binary-weighted value, like the cascode devices above them, thus reducing their effective area. Also, charge injection decreases when a slow transient is applied to the input of a switch compared to a fast transient [29]. For this reason, an input slew-rate control circuit consisting of an inverter buffer and a capacitor were added before each switch input as shown in Figure 3.7.

The inverter buffer consists of a short L inverter (fast) followed by a longer L inverter (slow). A capacitor is added to further slow the input transient response to the DAC. The purpose of the slew-rate control buffers is to ensure symmetrical inputs to each switch and slow the rise and fall time of the digital inputs, so the circuit has more time to dissipate each switch's inversion layer charge. A simulated response of the slew-rate control circuit is shown in Figure 3.8. As the switch input transitions high, the first inverter transitions low immediately followed by the second inverter which has to charge the capacitor at its output, slowing its rise time.

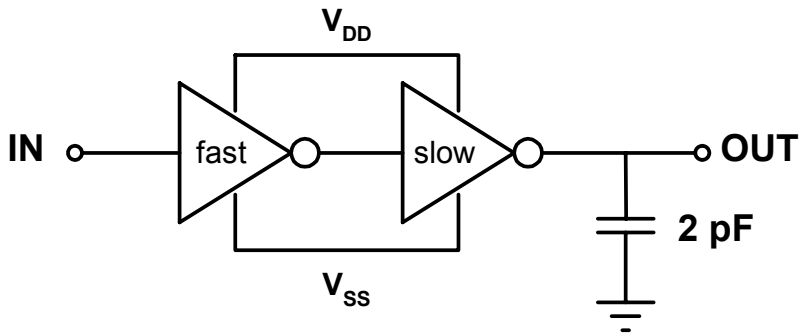

Figure 3.7: Input slew-rate control circuit applied to each of the DAC inputs.

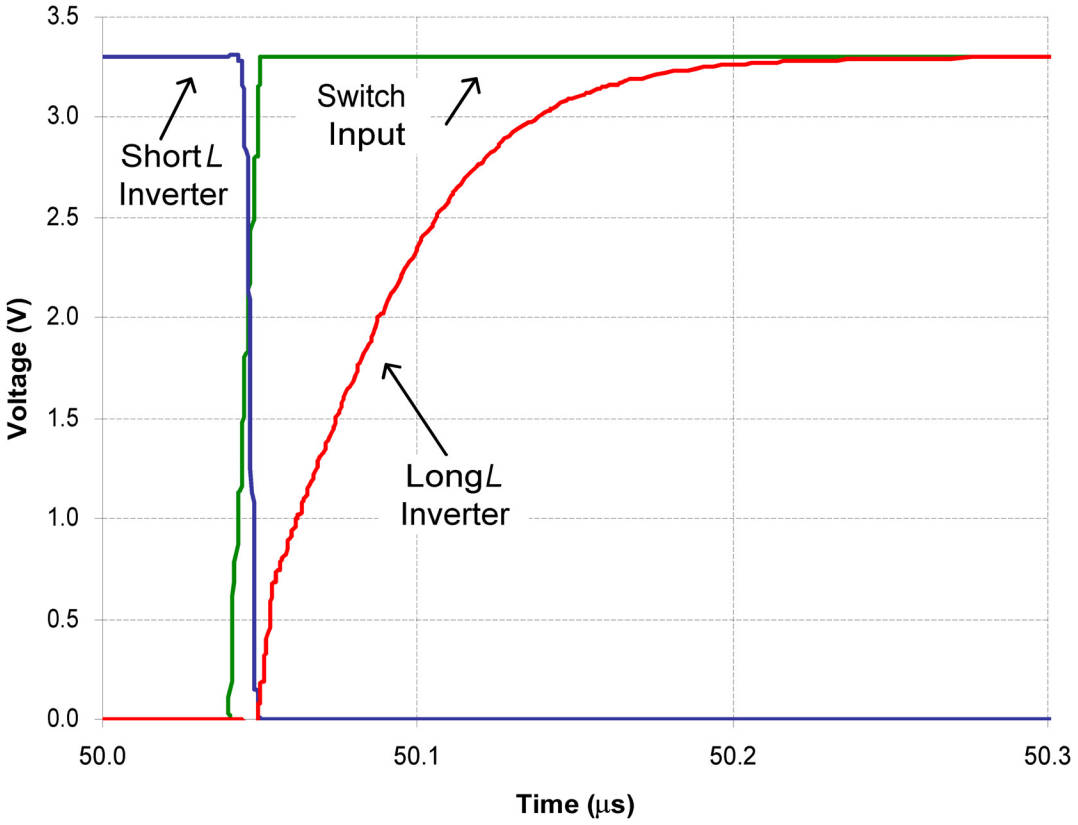

Figure 3.8: Simulation of input slew-rate control circuit.

Two different situations arise in simulating the DAC design of Figure 3.5 when the switching voltages are applied to the inputs (*S*3-*S*0). When the DAC is in a steady-state or start-up condition where no initial voltage has been applied to a given switch, there is a delay in the output current response. This delay occurs on the rising edges of the output current pulses as seen in Figure 3.9 and is due to an initial charging of all capacitances associated with a given switch's cascode devices and any parasitics within the output current path.

The other condition seen in Figure 3.9 involves the DAC being in an active state where all the capacitances and cascode devices have been fully charged prior to the next switch cycle. The difference between the two states is the delay associated with capacitance charging that is no longer present in the active state. This situation was simulated by including an initial full-scale input pulse to the DAC ('1111') before individually pulsing the inputs to the switches.

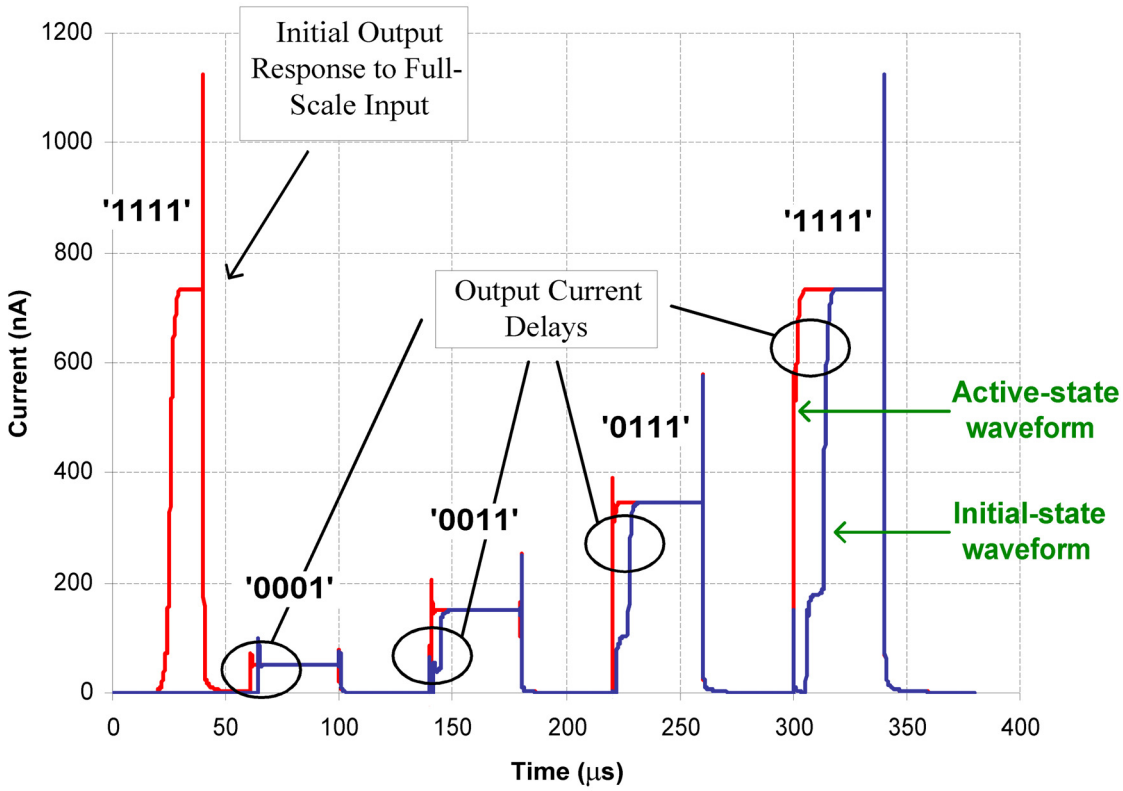

Figure 3.9: Simulation results of start-up and active conditions of DAC output.

Figure 3.9 also shows how much charge injection affects the output current when a switch is open or closed. When the circuit is operating in the initial-state condition, an input switch closing does not affect the output current because its charge injection is just transferred to the uncharged capacitances that are inherently present in the system. For the active-state condition, the charge injection associated with a switch closing does affect the output current because the circuit's stray capacitances are already pre-charged by the initial pulse input. For both active and initial conditions, a switch opening contributes to an overshoot of output current due to charge injection. From Figure 3.9 it looks like the charge injection from a switch opening is proportional to the output current, but this is not the case. The large current spike occurring at the end of the simulation comes from the combination of all four input switches opening simultaneously, so all the switches' charge injection is being summed at the output (400-nA overshoot).

Despite the lengths taken to reduce charge injection into the system by including the input slew-rate control circuit, minimizing the sizing of the input switches, and using the lower supply voltage as the switching supply, the DAC still seems to produce considerable charge injection. However, without the input slew-rate control circuit applied to the input switches of the DAC, the output current overshoot is 1.85 μA. This equates to almost a factor of five reduction in the overshoot of output current with the addition of the input slew-rate control circuitry. The current overshoots in the output current would also not be so obvious if larger current levels were being output since channel charge is not dependent on the current level. If the DAC were providing a 10-μA output current, a 400-nA overshoot would only equate to a 4% change of the output current. The overshoot in the initial output response to a full-scale input and the final pulse in Figure 3.9 can be further reduced by opening the input switches in a controlled manner. Offsetting the switch openings in time would decrease the amount of overshoot of the output current that a micro-battery would have to sink at one time.

The output stage of the DAC consists of a LVCCM biased by V_{Bias} shown previously in Figure 3.5. A cascode current mirror provides for higher output impedance (R_o) of the current charger compared to a single output device. High output impedance is

important for the system because we want to mimic the operation of an ideal current source, which theoretically has infinite output impedance. The LVCCM scheme was used because a fully charged micro-battery has a voltage capacity of 4.25 V and the current source needs to provide adequate headroom to charge to this level. A regular cascode current mirror would only provide a charging capability up to $V_{DDH} - |V_{THP}| - 2V_{SD,Sat}$. For a standard 0.35-µm SOI process, this would equate to approximately 1.3 V below the V_{DDH} supply voltage (3.7 V). For the case of the LVCCM used in this design, the micro-batteries can charge to approximately $2V_{SD,Sat}$ (500 mV) below the V_{DDH} supply voltage or 4.5 V.

The bias voltage for the LVCCM is generated using the "V_{GS}-multiplier" [31] shown biasing the output stage of the DAC in Figure 3.10. The op-amp senses the gate voltage of M_{10} and M_{11} with respect to V_{DD} (V_{SG}) with its non-inverting input. Assuming an ideal op-amp with no error voltage between the two input terminals of the op-amp, the inverting input is at the same voltage as the non-inverting input, V_{SG} down from V_{DD}. This is an accurate assumption if the op-amp has a large open-loop gain and negligible offset. The resistor divider between the V_{DD} supply voltage and the inverting input sets

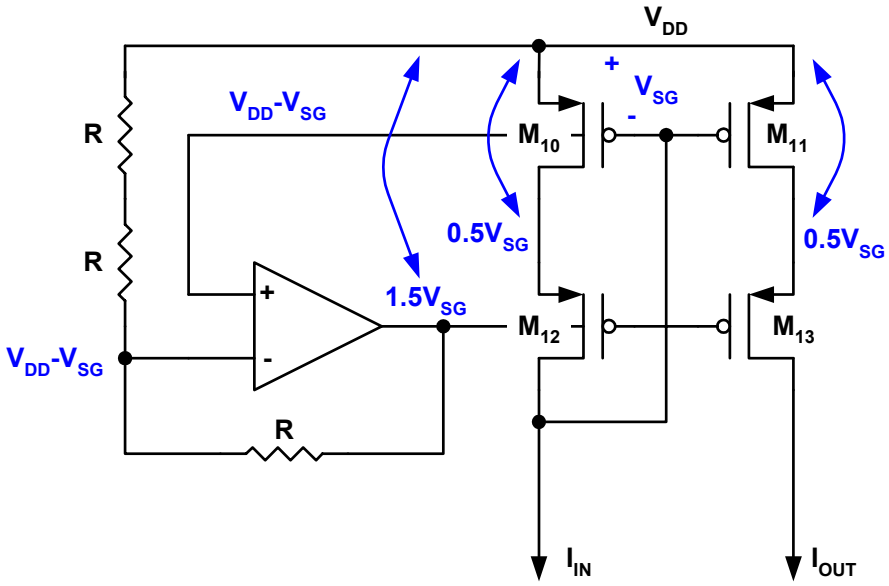

Figure 3.10: V_{GS}-multiplier biasing the LVCCM of the DAC output stage.

up a current that flows through the resistor between the inverting input and the output of the op-amp. If all the resistors are equally sized, then the output of the op-amp and the gates of M_{12} and M_{13} are forced to be $1.5V_{SG}$ down from V_{DD}. This leaves the mirror devices M_{10} and M_{11} with $0.5V_{SG}$, which is greater than $V_{SD,Sat}$, for their voltage headroom (V_{SD}) in the LVCCM.

The novelty of this circuit comes in its ability to provide adequate headroom for M_{10}–M_{13} to remain in saturation from weak to strong inversion, over a wide range of input currents, and over a broad temperature range while still providing high output impedance. Some other LVCCM bias circuits have been developed [23], [20], [32], but none encompass all the benefits of the V_{GS}-multiplier. Minch describes a method that biases the current source devices of a LVCCM right at the edge of saturation where $V_{SD} = V_{SD,Sat}$ [20]. This, however, does not deliver the highest output impedance possible from the current mirror.

The output resistance of the Minch current mirror shown in Figure 2.4 is

$$R_o = r_{o7}\left(1 + g_{m7} r_{o6}\right) + r_{o6} \tag{3.12}$$

where r_{o6} is the small-signal output resistance of the device biased at the edge of saturation. The V_{GS}-multiplier does an opposite trade-off by biasing the current source device a little farther into the saturation region thus reducing the current mirror's overall output voltage swing, but provides higher output impedance. The output resistance of the V_{GS}-multiplier shown in Figure 3.10 has the same form as (3.12)

$$R_o = r_{o13}\left(1 + g_{m13} r_{o11}\right) + r_{o11} \tag{3.13}$$

but r_{o11} is greater than r_{o6} of the Minch circuit since M_{11} is biased further into saturation than M_6.

To help illustrate graphically where $V_{DS,Sat}$ is located and how it pertains to output impedance, Figure 3.11 shows a typical I_{DS} vs. V_{DS} curve for an *n*MOS device. The area to the left of the pinch-off locus is known as the linear or triode region of operation in which a resistive channel directly connects the source and drain of the MOSFET. Once the channel has reached the pinch-off point for a given V_{GS}, the drain current becomes

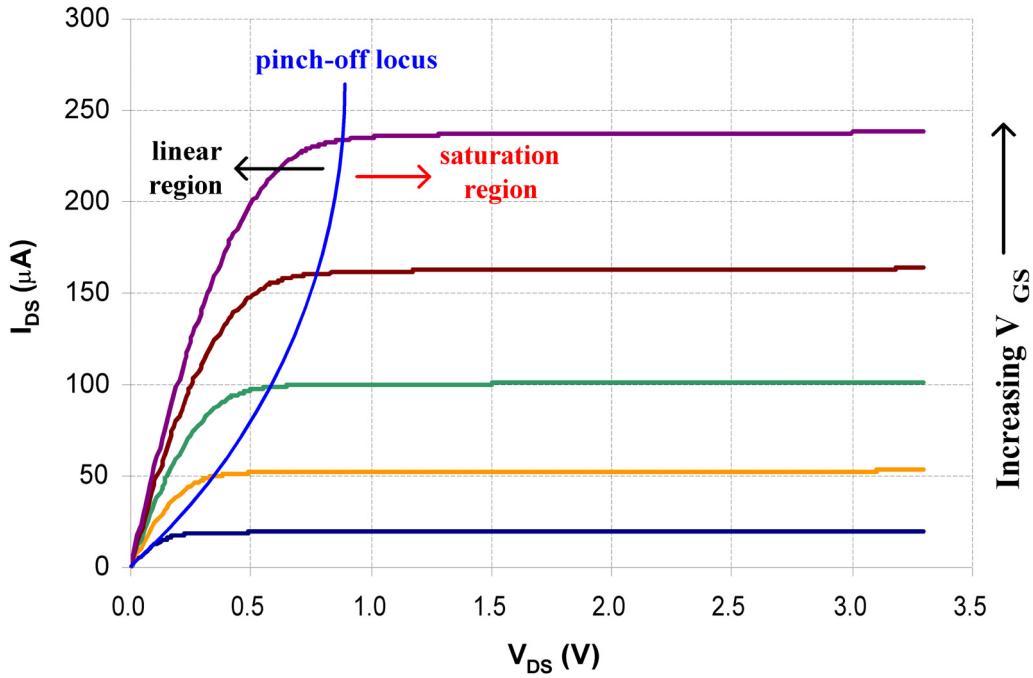

Figure 3.11: I_{DS} vs. V_{DS} curve showing regions of operation of an *n*MOS transistor.

constant if short-channel effects are neglected [33]. This region of constant current is known as the saturation region of operation. The intersection of the pinch-off locus and a given V_{GS} curve defines a MOSFET's $V_{DS,Sat}$ voltage [33]. A transistor's output impedance can by found by finding the slope of the curve at a given point. As the slope flattens out in the saturation region, the output impedance reaches its maximum; hence the reason for higher output impedance in the V_{GS}-multiplier over the Minch circuit.

The temperature stable beta-multiplier current reference, the DAC with input slew-rate control circuitry, and the V_{GS}-multiplier comprise the current charger in this design. Figure 3.12 shows a DC simulation of the current charger output at room temperature as the micro-battery voltage (V_{Batt}) is swept from 0 to 5 V. The three curves in the figure represent the output current generated by a 1 LSB input, a mid-scale input, and a full-scale input into the DAC. The current charging profile associated with these inputs remains flat over the entire battery voltage range, 0–4.25 V, indicative of the current charger's high output impedance. Above 4.5 V, the cascode devices start to fall

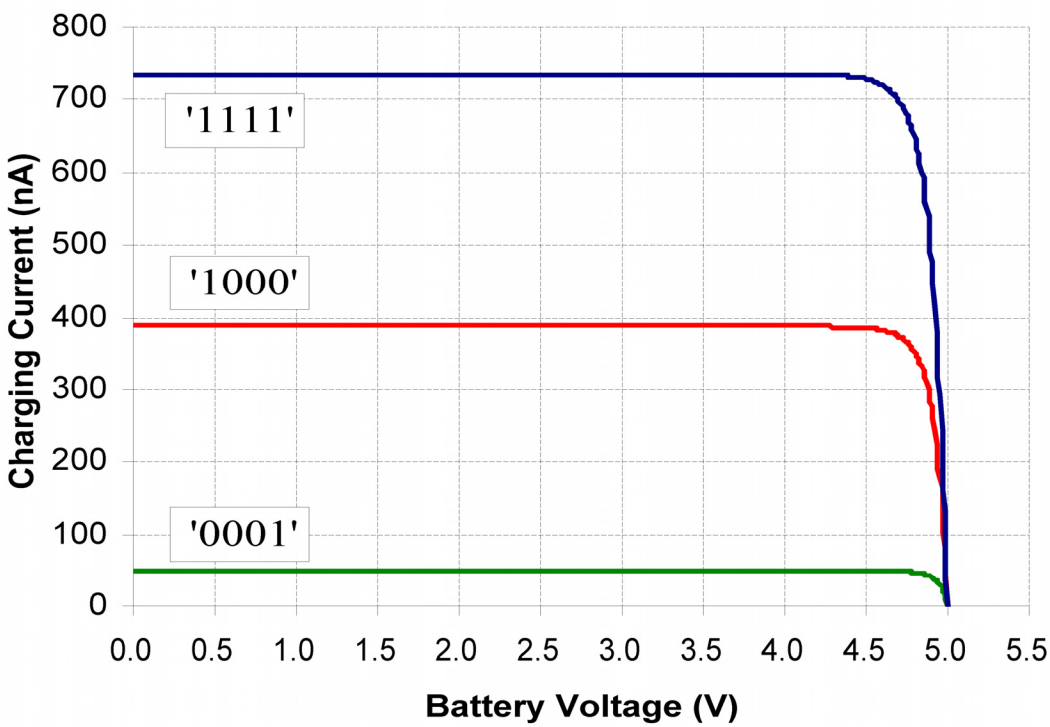

Figure 3.12: Simulated DC sweep of current charger output at room temperature for selected input codes.

out of saturation as the battery voltage nears the upper supply voltage, V_{DDH}, turning off the output stage of the DAC.

The charger output current as a function of temperature is dependent mainly on the beta-multiplier reference current. Figure 3.13 shows a simulation of how the charger output for a mid-scale input varies with temperature. Notice that at lower temperatures, the charger output current starts to increase because the reference current increases. This might not be an accurate representation of how the actual current reference will operate since the resistor parameters used in simulations were not modeled for low temperature situations.

Recall from (3.1) that the *IC* is temperature dependent on I_o, which is described by

$$I_o = 2n\mu_o C'_{ox} U_T^2 \qquad \textbf{(3.14)}$$

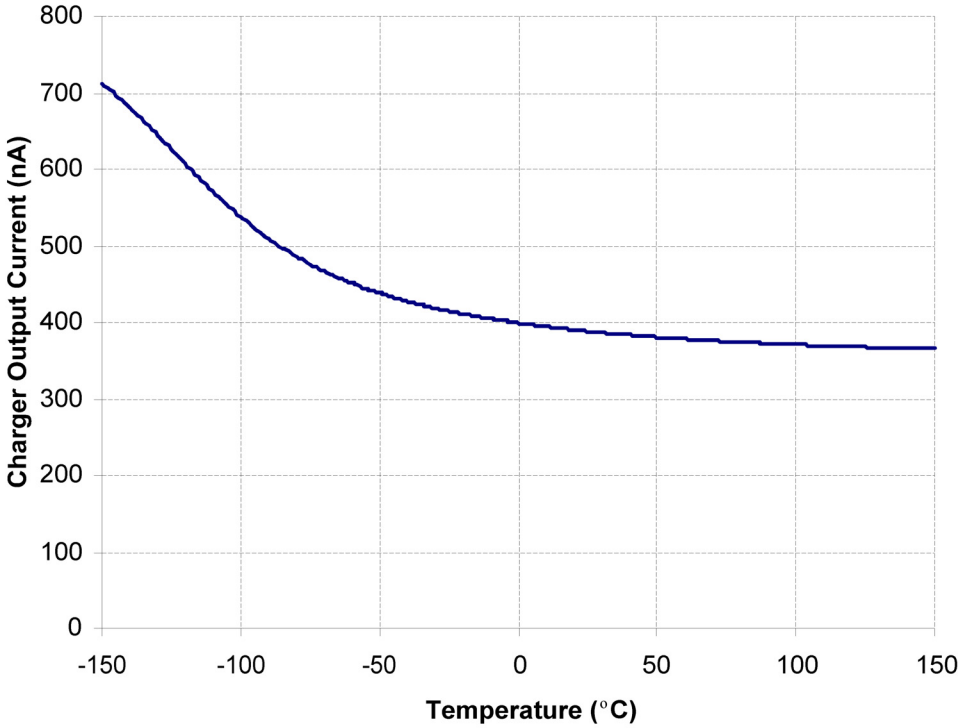

Figure 3.13: Simulation of DAC mid-scale output plotted against temperature.

Based off experimental resistance measurements, the hole mobility was determined (Figure 3.3) and used to find the technology current for this process. Calculations show that I_o is proportional to temperature, which corresponds to inverse temperature proportionality to IC, assuming a constant I_D. Therefore, as temperature decreases, devices are moved from weak inversion slightly into moderate inversion (Figure 3.14), which will cause a shift in the reference current. Note that as M_1 and M_2 of the current generator (Figure 3.1) move well into moderate inversion for temperatures below –100°C, the generated reference voltage is no longer a PTAT voltage, thus temperature compensation against the p-well resistor is no longer achieved. For an extreme temperature case of –100°C, the devices M_1 and M_2 are at the transition point between weak and moderate inversion (IC = 0.1) so the reference voltage can still be assumed PTAT.

The largest contributor to the shift in output current at low temperatures in Figure 3.13 is the temperature dependence of the p-well resistor used in the beta-multiplier

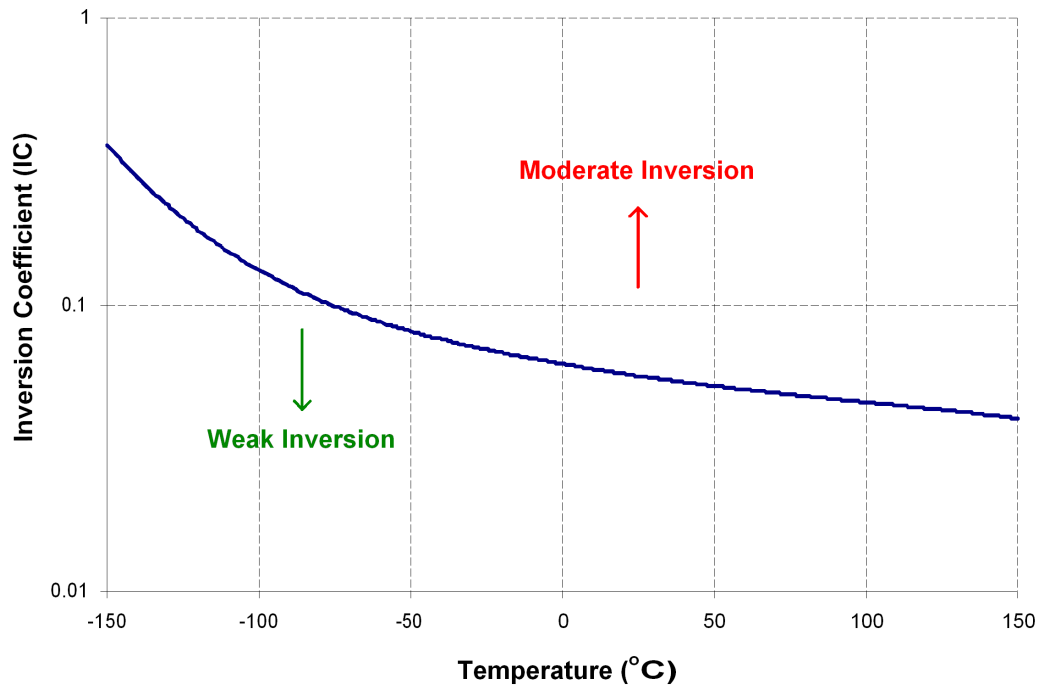

Figure 3.14: Calculated *IC* of M_1 and M_2 devices of beta-multiplier current reference.

current reference. Measured results of the resistance per square of a p-well resistor (Figure 3.4) show that as the temperature decreases the resistance increases. Assuming that the PTAT reference created by the weak inversion MOSFETs has not changed, this increase in resistance would cause a decrease in the output current, not an increase as seen in Figure 3.13. Remember however, that the simulated p-well resistance against temperature does not display the same low-temperature effects as the measured p-well resistance (Figure 3.4), hence the discrepancy between the expected output current and the simulated output current seen in Figure 3.13 for temperatures below 0°C.

Regulated Voltage Source

As well as being current charged, micro-batteries also need to be voltage charged to complete their charging cycle [5]. The methodology for charging these Li-Ion micro-batteries is to provide them with a constant current or PWM current charge until they reach full voltage capacity (4.25 V) and then switch them to a constant voltage charge. During the constant voltage charging phase, the current delivered by the regulated

voltage source decays exponentially to zero (trickle charge) until full capacity of the micro-battery has been reached (50 nAh).

The optimum situation for constant voltage charging would be to have an ideal voltage source available on-chip to charge the micro-batteries. Since this is not possible, an alternative method must be used to provide a constant voltage low impedance node with a variable current output capability. The regulated voltage source shown in Figure 3.15 was designed using a operational transconductance amplifier (OTA) to meet these criteria. This type of op-amp configuration represents a voltage-sample, voltage-sum amplifier that can provide low output impedance due to the nature of negative feedback [21].

The desired output of this amplifier (V_{Reg}) coincides with the full voltage capacity of a micro-battery (4.25 V). The non-inverting input of the op-amp is driven by an input reference voltage chosen to be equal to a bandgap voltage reference, 1.2 V, for quick conversion to an on-chip reference in the future. For a 1.2-V non-inverting input and V_{Reg} = 4.25V, the ratio of resistors can be found by using

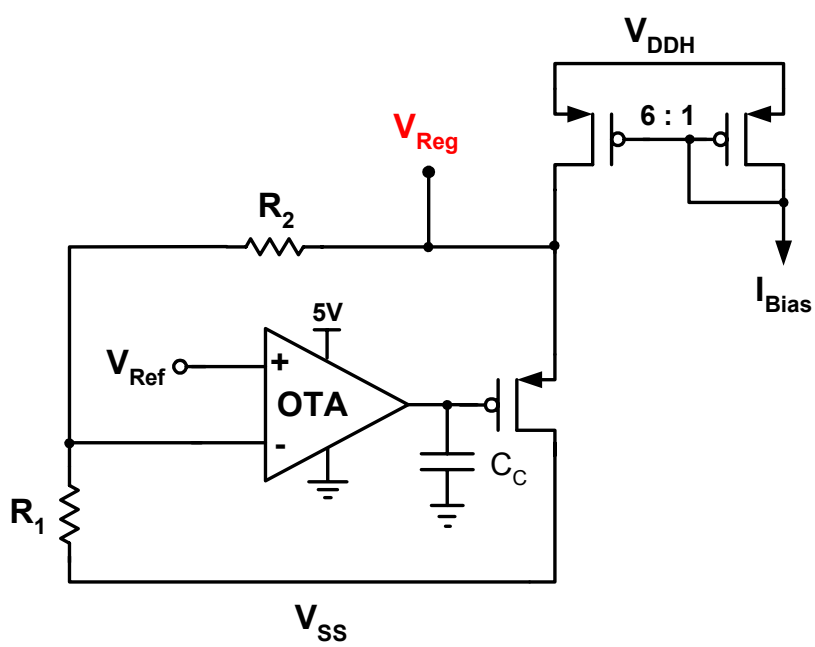

Figure 3.15: Regulated voltage source using a voltage amplifier.

$$V_{Reg} = V_{Ref} \times \left(1 + \frac{R_2}{R_1}\right) \Rightarrow \frac{V_{Reg}}{V_{Ref}} - 1 = \frac{R_2}{R_1} \cong 2.5 \qquad \textbf{(3.15)}$$

The voltage loop needs to be capable of providing a stable operating voltage for multiple micro-batteries connected to V_{Reg} at one time. Simulation results show that the regulated voltage source can drive a resistive load as low as 70 kΩ. With the addition of a compensation capacitor (C_C) that is provided off-chip, the voltage source can handle capacitive loads up to 100 μF at its output without compromising loop stability. As further testing of micro-batteries is done and its capacitance is determined as a function of both voltage and number of charge cycles, this external compensation capacitance could be moved on-chip.

Micro-Battery Voltage Monitor

A micro-battery's voltage needs to be monitored during the current charging process so that when it reaches its full voltage capacity, it can be transitioned to constant voltage charging. The digital representation of a micro-battery's voltage state is sent to a microcontroller that decides to continue current charging a micro-battery or to transition it to the voltage charging source. The microcontroller bases its decision from three different voltage level states of the micro-battery—undercharged, normal, and overcharged. Since only three states are needed by the microcontroller to make its decision, a 2-bit output from the voltage monitor is all that is needed.

To be able to continuously monitor the micro-battery's voltage state a 2-bit flash ADC, shown in Figure 3.16, was designed. Flash converters typically have the highest speed of any type of ADC and they are relatively easy to design due to their simple topology. The disadvantage of the flash ADC is the amount of physical layout area they consume. For every bit of increased resolution in a flash ADC, the area occupied by it doubles [16]. Since this design only has a 2-bit output, D_0 and D_1, the amount of area needed is minimal. The output of a flash ADC is given in thermometer code and typically is converted to binary code using an encoder to minimize the number of output

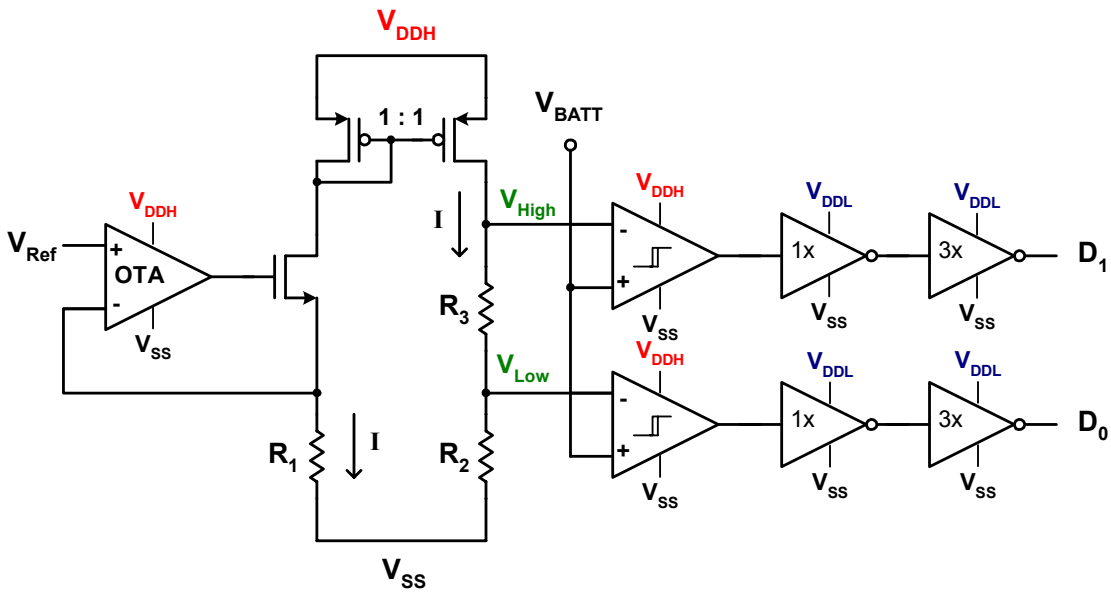

Figure 3.16: Two-bit flash ADC architecture.

pins. For this application, only three voltage levels need to be distinguished so no encoder is needed.

The conversion from an analog to digital signal in the flash ADC is done by using comparators fed by reference voltages. The two reference voltages that are needed to determine a micro-battery's state are 3 and 4.25 V. A micro-battery with a voltage level below 3 V is undercharged, between 3 and 4.25 V is normal, and above 4.25 V is overcharged [34]. The reference voltages for the comparators are set by passing a fixed current (I) through a resistor ladder.

The current, I, is generated through a negative feedback loop using the OTA's reference input voltage, V_{Ref}, and R_1. Again, the reference voltage was chosen to be 1.2 V for easy conversion to an on-chip bandgap voltage reference. Using a 1 to 1 ratio of currents in the *p*MOS current mirror in Figure 3.16, the same current, I, flows through the resistor ladder. The ratio of resistors to set the comparator voltage references is determined by

$$V_{Low} = V_{Ref}\left(\frac{R_2}{R_1}\right) = 3\,V \qquad \textbf{(3.16)}$$

and

$$V_{High} = V_{Ref}\left(\frac{R_2 + R_3}{R_1}\right) = 4.25\ V \tag{3.17}$$

The decision-making aspect of the flash ADC is left up to the comparator. If the non-inverting input of a comparator is larger than its inverting input, then it outputs a logic 1, whereas if the inverting input is larger than its non-inverting input, it outputs a logic 0. Most comparators consist of three stages; a preamplification stage, a decision circuit consisting of a positive feedback loop, and an output buffer [16]. Measurements used to characterize a comparator are its gain, offset voltage, propagation delay, and hysteresis window. The comparator design for this flash ADC is shown in Figure 3.17. Note that the upper supply voltage used for this comparator is V_{DDH} (5 V) in order to handle a 4.25-V reference input. The use of the output level shifter in the comparator is to limit the voltage that is supplied to the next gate in this 3.3-V process to avoid gate

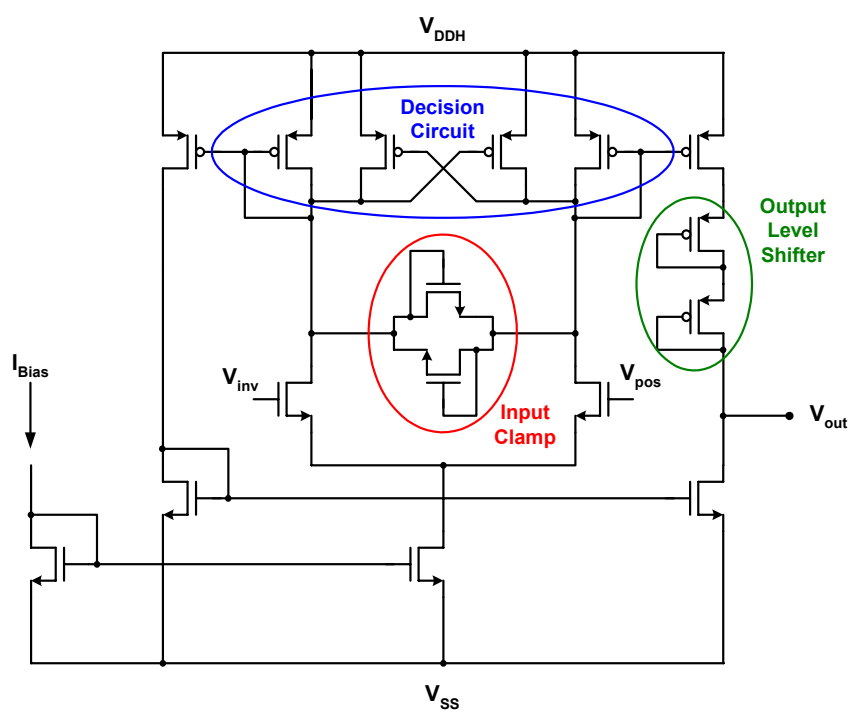

Figure 3.17: Comparator architecture used in the flash ADC.

oxide breakdown. The input clamp is included to ensure that the drain nodes of the input pair are never more than a V_{THN} voltage of each other to minimize transient recovery time.

The micro-batteries are expected to reach full capacity after being charged for approximately an hour [5]. This translates into a slow ramp that the inverting input (V_{inv}) of the comparator will see as the micro-battery voltage increases. For this reason, it is not necessarily important to have an extremely fast comparator stage. We also expect the micro-battery voltage to be steady as it is being charged so that we can use a small hysteresis window.

A simulation of the hysteresis characteristic of the comparator is shown in Figure 3.18. The inverting input, V_{inv}, was held at mid supply (2.5 V) while V_{pos} was swept from both below and above 2.5 V. Switching of the comparator output occurs approximately 6 mV above and below 2.5 V yielding a 12-mV hysteresis window. The sharp transitions of this simulation plot also allude to the high gain of the comparator. Gain of a

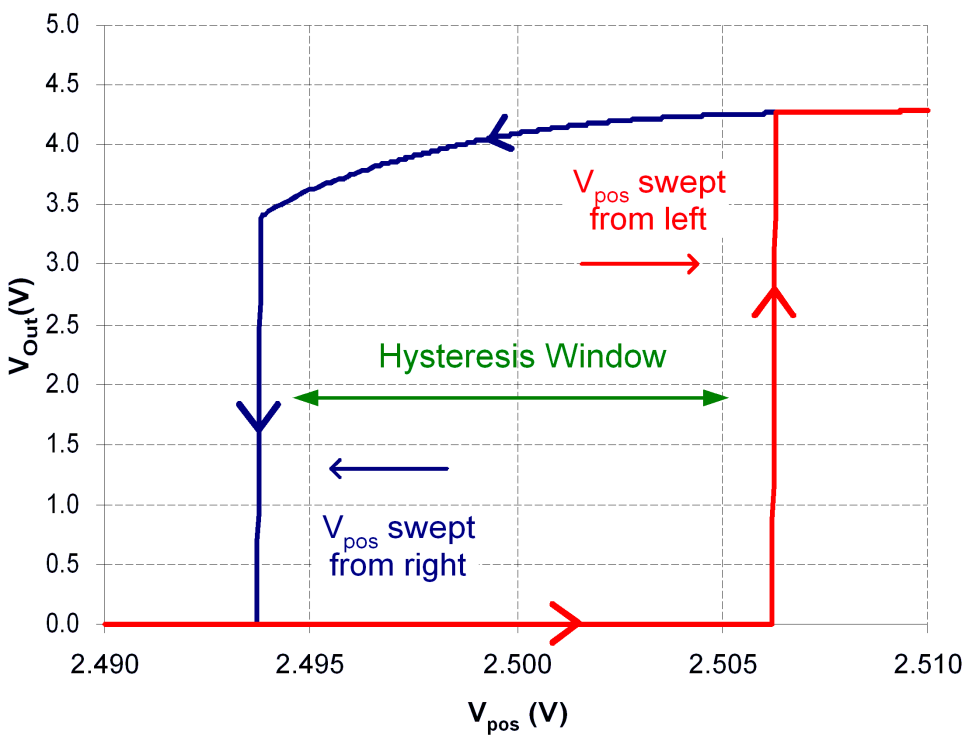

Figure 3.18: Simulation of comparator hysteresis window with V_{inv} = 2.5 V.

comparator is determined by calculating the derivative of the DC transfer curve. Through simulations, the gain of this comparator was found to be approximately 77 dB, which results in a 400-µV resolution. The output voltage (V_{Out}) in this plot does not reach up to the 5-V supply voltage due to the voltage shifters at the output of the comparator.

Propagation delay is the time difference between the V_{pos} input crossing the V_{inv} input and the output changing states. Figure 3.19 shows the simulated propagation delay for the comparator shown in Figure 3.17 to be approximately 150 ns, easily sufficient for this application. This simulation displays an almost worst-case scenario where V_{pos} is applied at a level just 20 mV above the reference level, V_{inv} = 2.5 V, and then suddenly taken away. The reason for the long delay time in this comparator is that single high-gain stage comparators exhibit a longer propagation delay time than those having several cascaded low-gain stages [16].

A 3.3-V digital output buffer is included after each comparator's output in order for the flash ADC to be able to drive an off-chip load. The buffer consists of a 1×

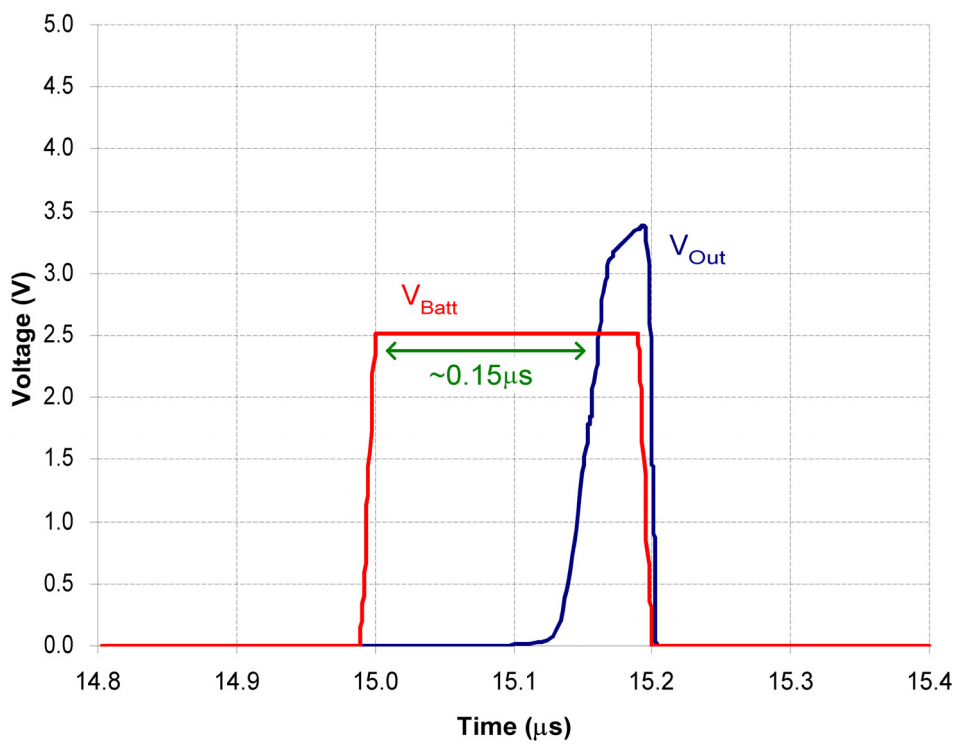

Figure 3.19: Simulation of propagation delay of comparator.

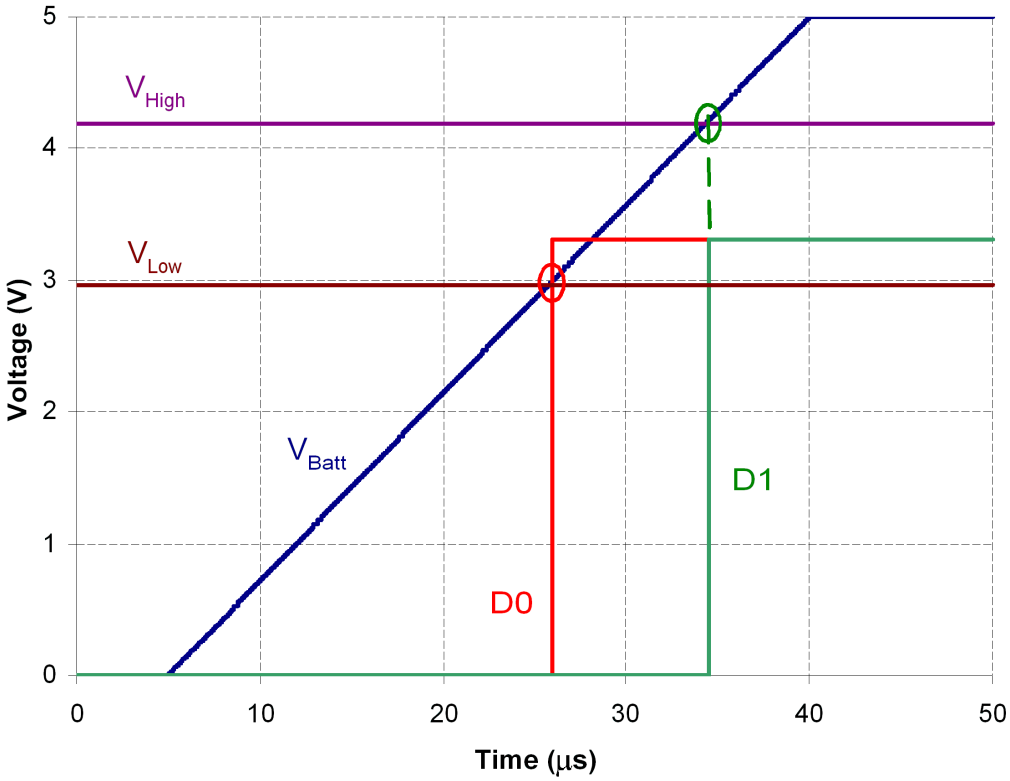

Figure 3.20: Flash ADC simulation by sweeping V_{Batt}.

inverter followed by a 3× inverter. Simulation results for the entire flash ADC are shown in Figure 3.20. The micro-battery voltage, V_{Batt}, was swept from 0 to 5 V and plotted against the reference voltages to show the switching points of the digital outputs of the ADC. Notice that the comparators change state immediately following V_{Batt} increasing past a given comparator voltage reference level (V_{Low} and V_{High}).

CHAPTER 4

MICRO-BATTERY POWER MANAGEMENT SYSTEM – MEASURED RESULTS

Test Setup

A system level diagram of the micro-battery power management system is shown in Figure 4.1. Two external references are required for the system to function properly, a 10-µA bias current (I_{BiasN}) and a 1.2-V reference voltage (V_{INP}). Four outputs of this power management IC need to be measured, the two digital outputs from the voltage monitoring ADC (D_0 and D_1), the charger current output (I_{charge}), and the voltage regulator output (V_{Reg}).

The system operates by attaching one or more micro-batteries to I_{charge} and inputting a 4-bit digital word to the DAC to choose the level of current charging (0–750 nA). The flash ADC continuously monitors the voltage level of the micro-

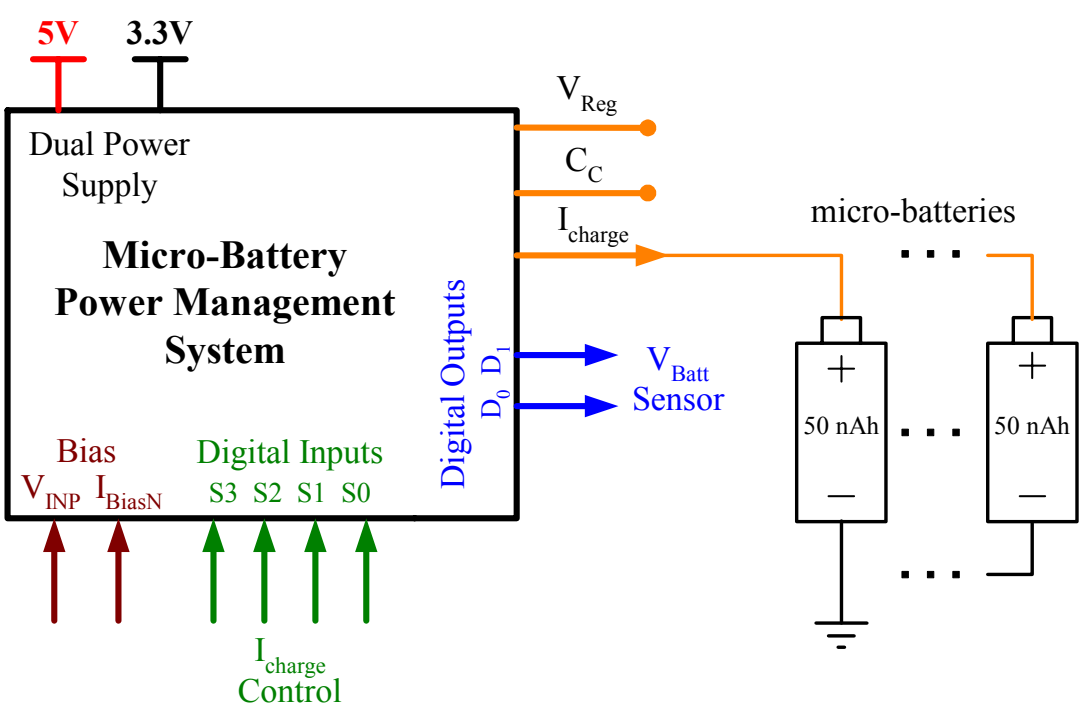

Figure 4.1: System level diagram of micro-battery power management system.

batteries attached to the I_{charge} node and outputs a digital representation of the micro-battery's voltage state via D_0 and D_1. The voltage regulator output V_{Reg} should output a constant voltage equal to 4.25 V and be able to support multiple micro-batteries at one time without loss of voltage integrity. A compensation capacitor (C_C) node from the voltage regulator circuit is padded out off-chip. This allows external compensation of the voltage regulator loop so stability is maintained when driving a large capacitive load.

A test board was built for this system using a solid copper ground plane board, shown in Figure 4.2. Each digital input was created using a triple pole, triple throw (3P3T) switch. For each switch, two of the switch poles are connected to V_{DDL} and to V_{SS} to simulate a logic '1' and logic '0', respectively, for constant current charging testing. The third pole of each switch is connected to a common BNC connector that drives all the inputs to the DAC. The common BNC input can be driven by a function generator to simulate PWM current charging.

The 10-µA bias current generated off-chip is input to I_{biasN}, where it is mirrored on-chip to provide current biases for multiple cells. It is created using the configuration

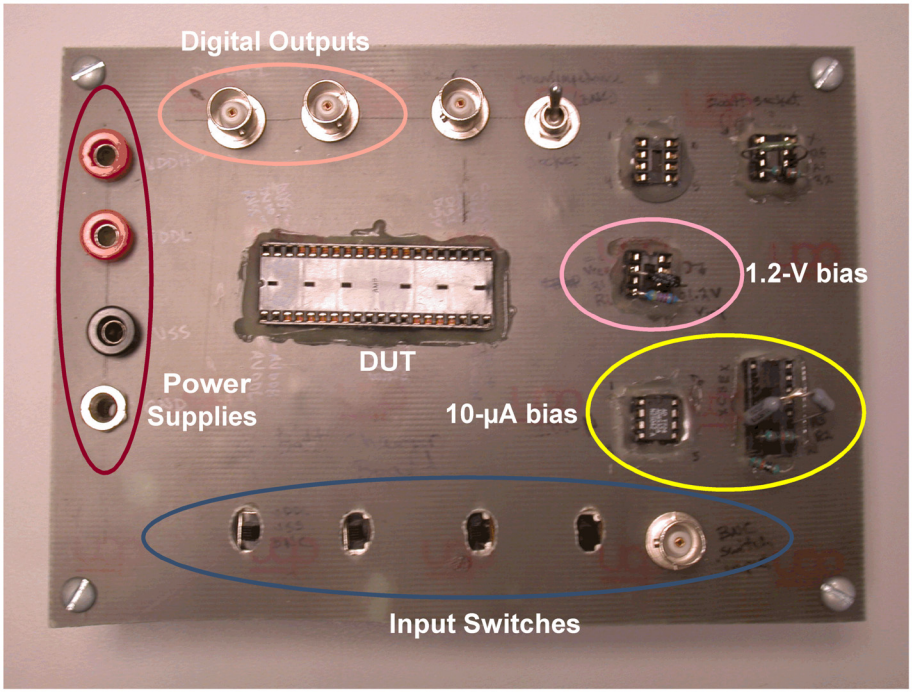

Figure 4.2: Copper ground plane test board used in taking measurements.

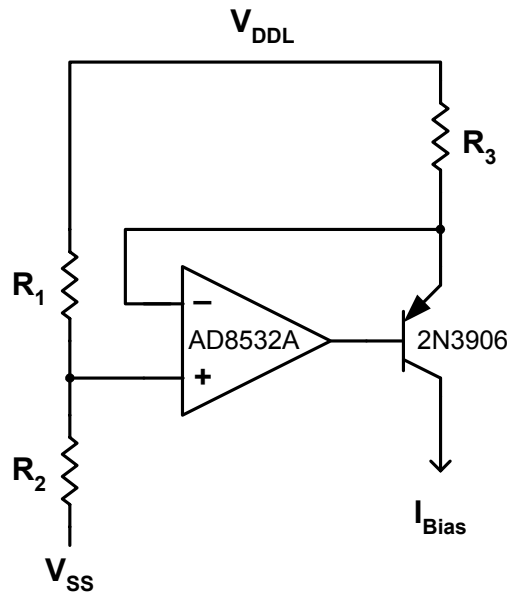

Figure 4.3: Off-chip 10-µA bias current generator.

shown in Figure 4.3. The bias current output (I_{Bias}) is set by the ratio of the resistors

$$I_{Bias} = V_{DDL} \frac{R_1}{(R_1 + R_2)R_3} \tag{4.1}$$

The 1.2-V reference is generated using a ratio of two resistors and a ceramic bypass capacitor to filter out any noise at this node.

Micro-Battery Current Charger

A Keithley 2400 SourceMeter® was used to measure the current charger output because it can act as both a voltage source and current meter at the same time with current measuring capabilities as low as 10 pA. Sweeping the voltage source of the Keithley mimics the response of a micro-battery increasing voltage as it is being current charged. DC sweeps to test the current charger output were measured in this manner. A typical DC sweep of the current charger output from 0 to 5 V at room temperature for each DAC input code is presented in Figure 4.4. Also included in this figure are labels

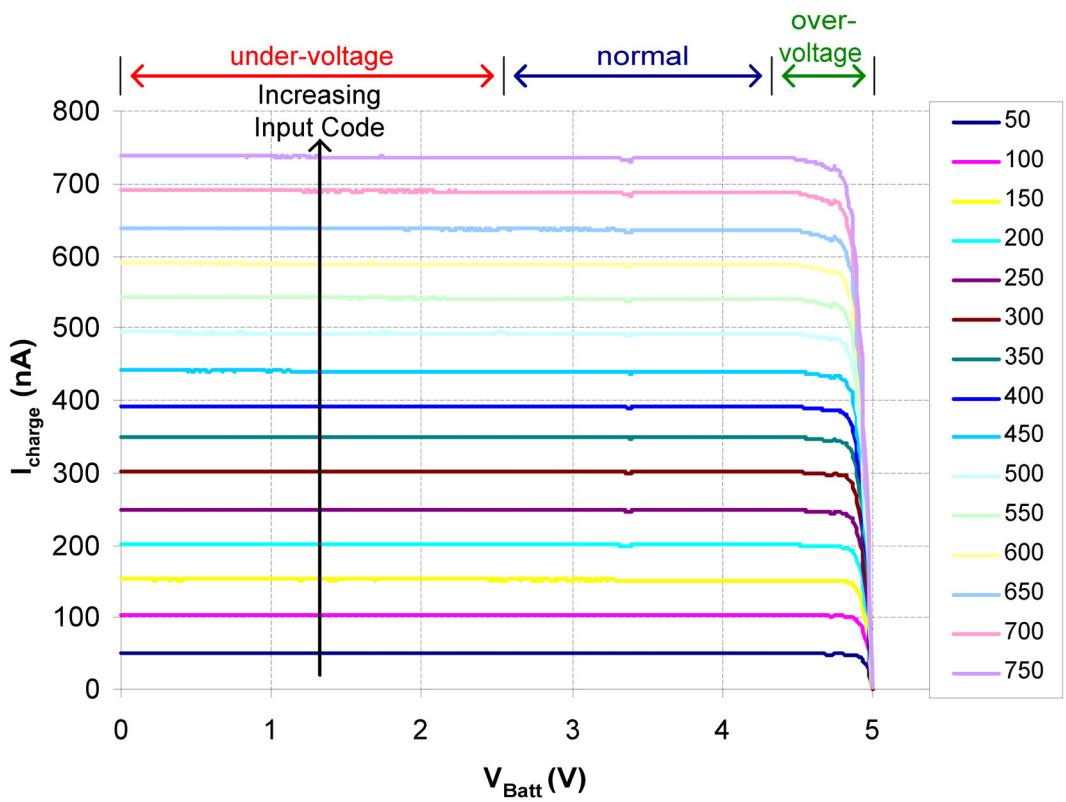

Figure 4.4: Measured DC sweep of V_{Batt} at room temperature for each DAC code.

distinguishing between the three different operating regions for a micro-battery—under-voltage, normal, and over-voltage.

From Figure 4.4, it is obvious that as the DAC input code increases, the amount of charger output current increases as well. The output current remains constant over most of the swept range until V_{Batt} approaches the V_{DDH} supply voltage (5 V). This constant current output is indicative of a high impedance output stage of the DAC made possible by the use of a cascode current mirror. Another thing to note from this figure is the wide range of current that is being sourced by the output stage of the DAC while maintaining a large voltage swing at the output of the current mirror because of the use of the V_{GS}-multiplier. The charger current starts to fall off at higher voltages because the output stage of the DAC is being shut-off.

Before continuing with the explanation of the performance of the current charger, some definitions of DAC performance merits need to be clarified. In a DAC, the offset

error (E_{off}) is defined to be the output that occurs for the input code that should produce zero output. The gain error (E_{gain}) is the difference at the full-scale value between the ideal and actual curves when the offset error has been reduced to zero. The absolute accuracy of a converter is defined to be the difference between the expected and actual transfer responses [35]. The absolute accuracy includes the offset, gain, and linearity errors. An n-bit accuracy implies that the converter's error is less than the full-scale value divided by 2^n–1.

After both the offset and gain errors have been removed, the integral nonlinearity (INL) and the differential nonlinearity (DNL) errors can be found. INL is defined to be the deviation of the output from a straight line [35]. The straight line used as comparison can be either a line through the endpoints of the converter's transfer response, or the best-fit straight line such that the maximum difference is minimized. INL measurements made on this DAC used the endpoint line comparison.

DNL is defined as the difference between the ideal and nonideal values of a DAC's transfer curve. The DNL specification measures how well a DAC can generate uniform analog LSB multiples at its output [16]. Generally, a DAC will have less than ±0.5 LSB of DNL if it is to be n-bit accurate. If the DNL for a DAC is less than ±0.5 LSB, then the DAC is guaranteed to be monotonic [35]. A monotonic DAC is one in which the output always increases as the input increases, as is the case in Figure 4.4.

Testing of this system was done with three samples of test chips. A plot of the transfer curve of the programmable current charger output is shown in Figure 4.5. These data points where taken from the same measurement data in Figure 4.4 for a V_{Batt} equal to 4 V. Each chip's output current for a given DAC input is compared with the ideal transfer curve. Looking at this transfer curve alone does not give much insight into the performance of the DAC other than the measurements of offset and gain error and reiterating that it is monotonic. The measured offset error for all three chips is 0.002 LSB. The gain error varied from –0.2 to 0.08 LSB across the 3-chip sample.

To better understand how well this DAC performs, measurements of the DAC's DNL and INL will be presented. Figure 4.6 shows the DNL characteristics of the programmable current charger over a 3-chip sample measured at room temperature. The

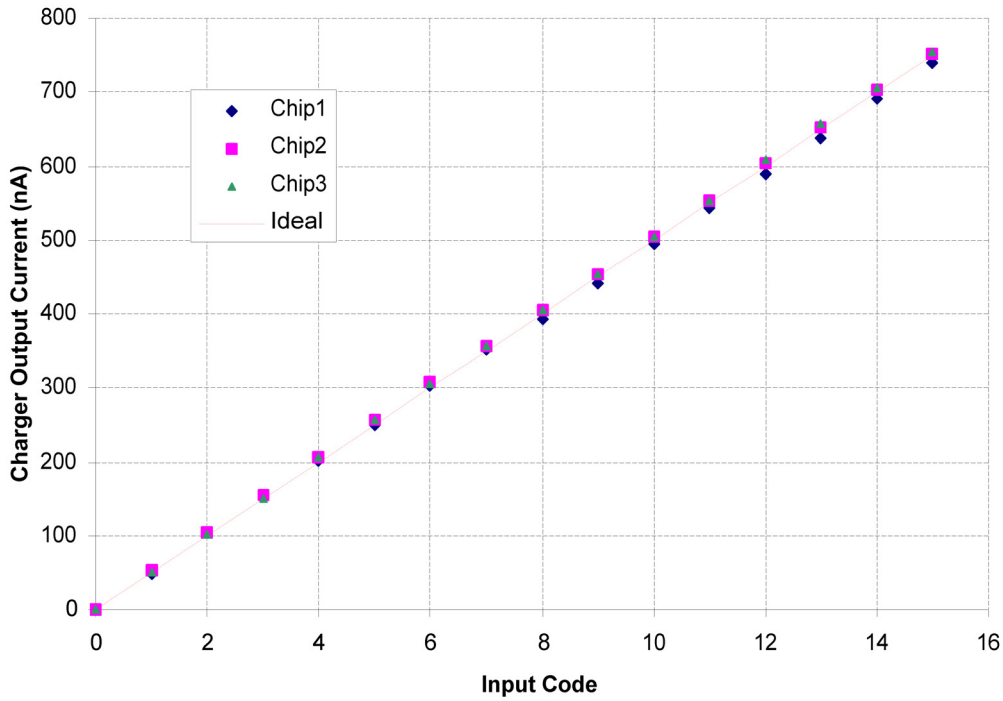

Figure 4.5: Measured transfer cure of the programmable current charger.

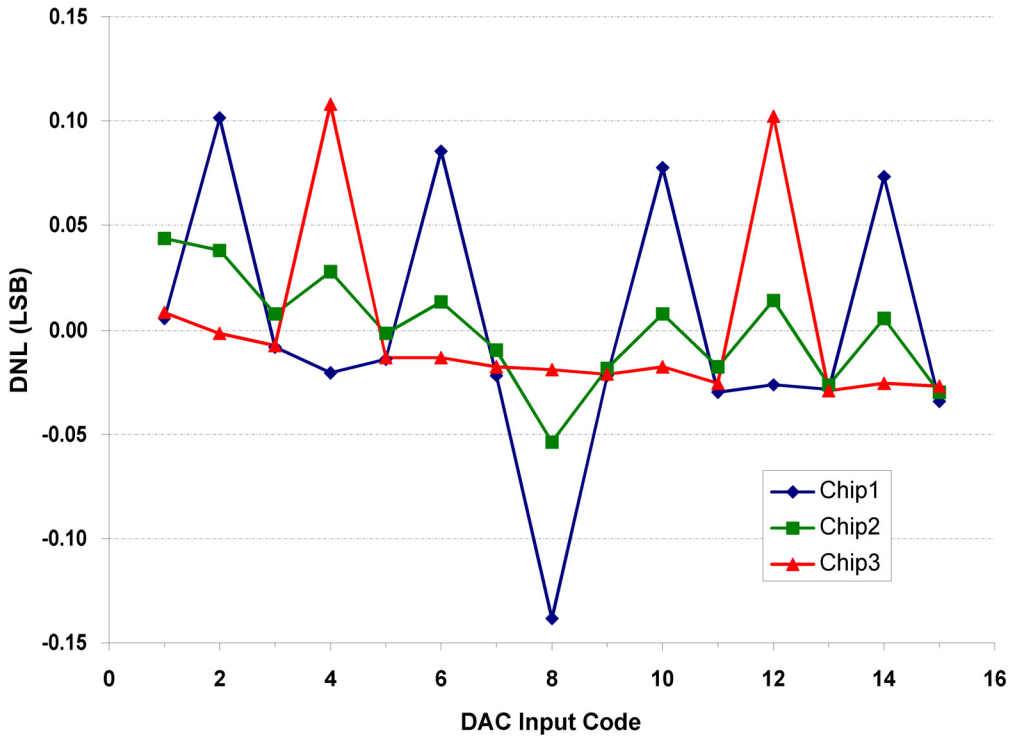

Figure 4.6: Measured DNL of programmable current charger.

monotonic nature of the DAC is once again illustrated through this figure because the worst-case DNL from all three chips is –0.15 LSB. This figure also alludes to the high accuracy of this DAC. For a 4-bit DAC to have 4-bit accuracy, the worst-case DNL would have to be less than ±0.5 LSB. Since the LSB for this DAC is –0.15, the DAC can actually achieve approximately 6-bit accuracy with 4-bit resolution.

The INL measurements of the programmable current charger are shown in Figure 4.7. The worst-case INL for the 3-chip sample is 0.15 LSB indicating that the measured transfer curve does not deviate much from the ideal transfer curve once the gain and offset errors are removed. It is common practice to assume that a converter with *n*-bit resolution will have less than ±0.5 LSB of DNL and INL [16].

Temperature tests on the programmable current charger were also done to see how well it performed over temperature variations. As seen in Figure 4.8, the current charger performed extremely well over the temperature range 0–100°C. The figure

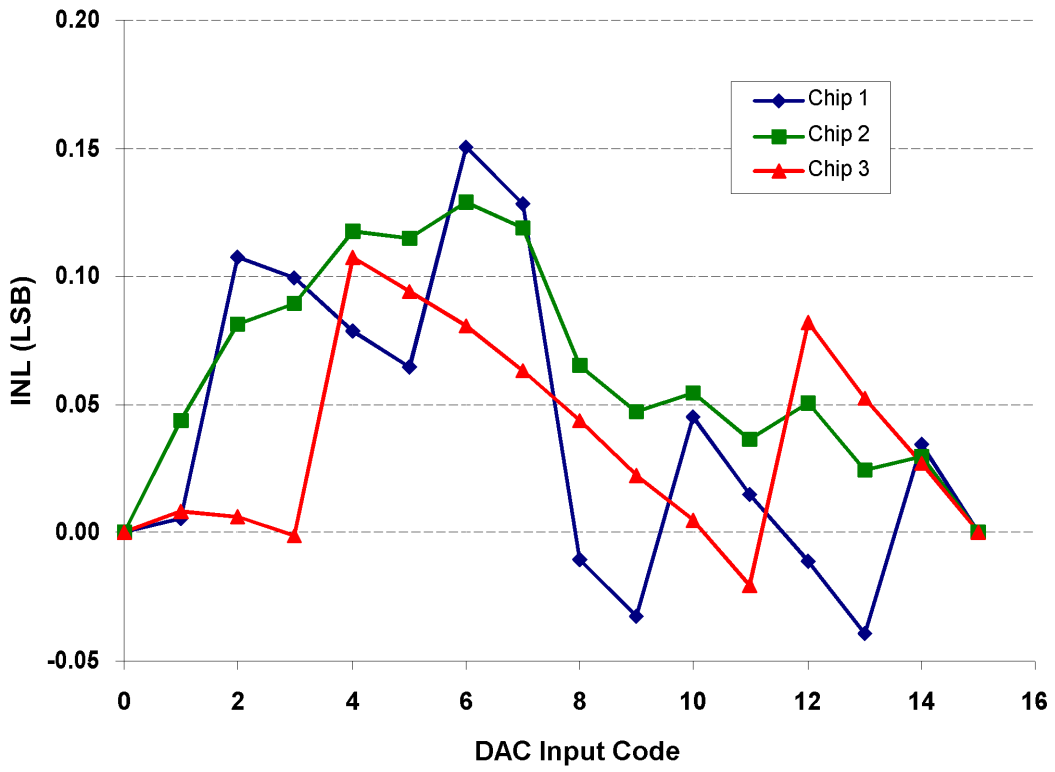

Figure 4.7: Measured INL of programmable current charger.

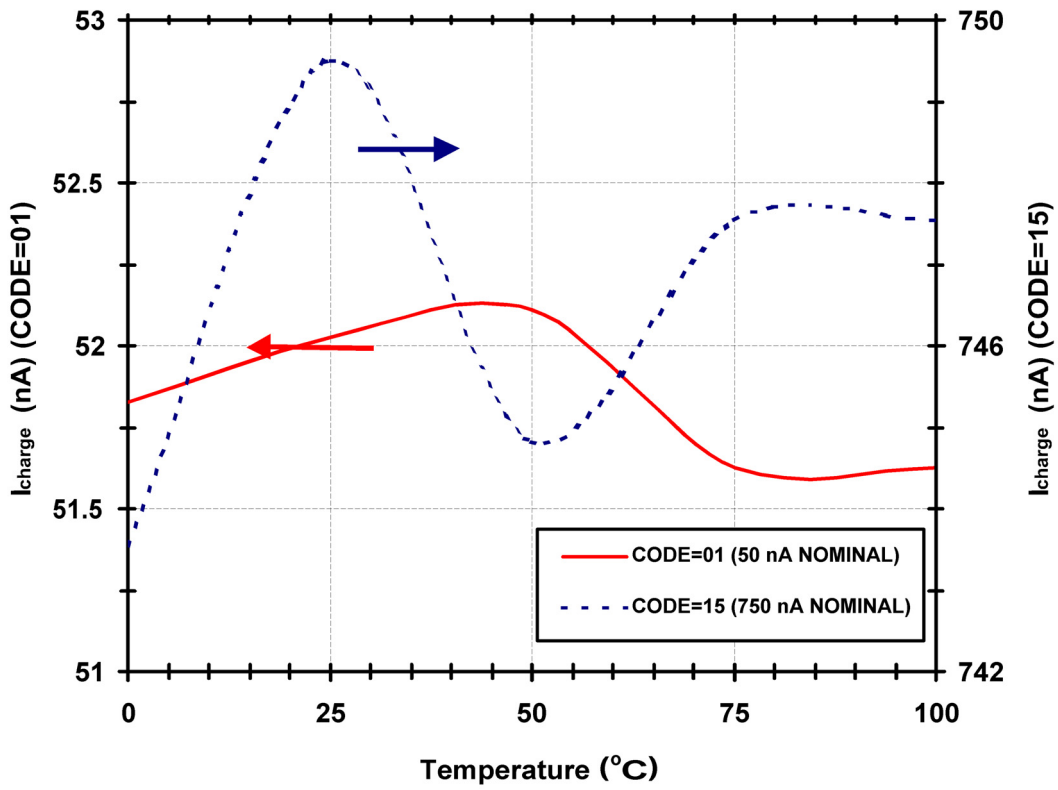

Figure 4.8: Temperature comparison of 50 and 750-nA I_{charge} currents.

compares the temperature variation of the output current for the two extreme cases, DAC input code of 1 and 15. For an input code of 1 and 15, there is a 2.1% and 1.2% deviation in output current over this temperature range, respectively, which is 5% less than expected from simulation results. This is the first temperature stable, low-level current reference fabricated on SOI that has been found to date in the literature [9]–[14]. As will be seen later in the chip micrograph, the programmable current reference only occupies an area of 0.15 mm^2 (300 µm × 500 µm).

Below 0°C, the current charger output starts to fall off as seen in Figure 4.9. This is opposite from what was simulated earlier (Figure 3.13) as expected. Also included in Figure 4.9 is a plot of the measured resistance per square of a p-well resistor across temperature that was shown already in Figure 3.4. As the resistance varies with temperature so does the output current. Remember that back in Chapter 3, a constant I_D was assumed when deriving Figure 3.14. In actuality, the output current level decreases

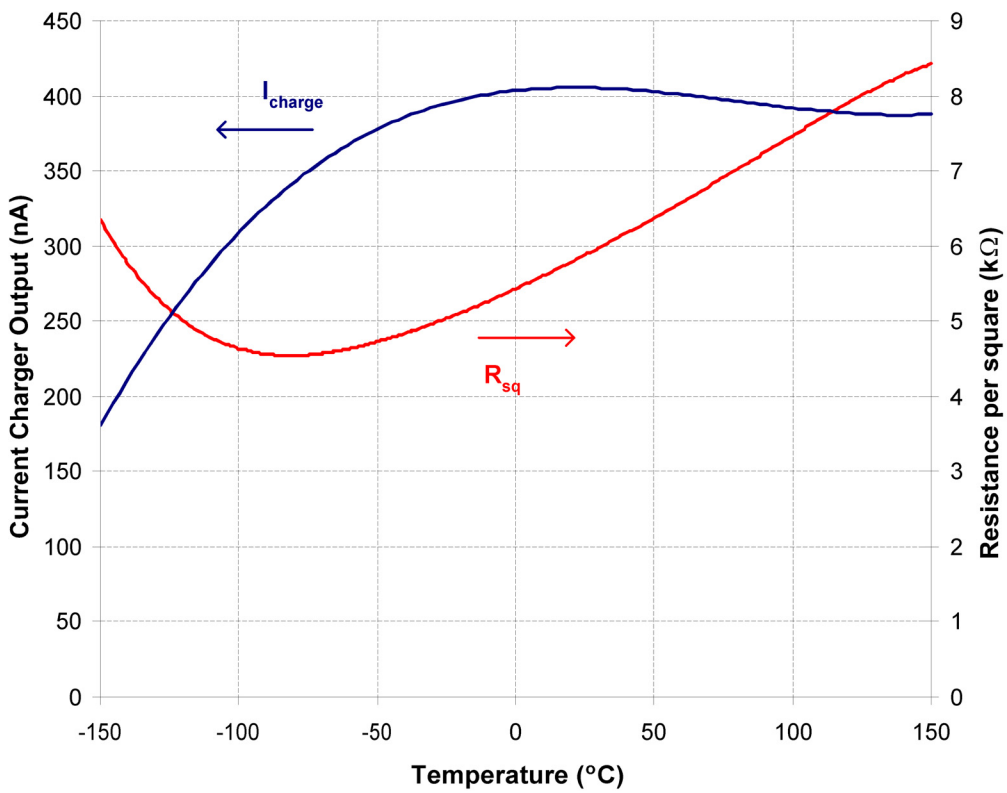

Figure 4.9: Comparison of current charger output and p-well R_{sq}.

with temperatures below 0°C. This decrease in output current keeps M_1 and M_2 of Figure 3.1 in weak inversion based of off (3.1), maintaining a PTAT voltage reference.

To better illustrate this point, Figure 4.10 shows the calculated PTAT voltage reference across temperature compared to the ideal PTAT voltage reference created by equating U_T (kT/q) over temperature. This voltage was not padded off-chip so a direct measurement could not be made. Instead, a measured resistance value was multiplied by the measured charger output current to give the calculated PTAT voltage. Both the calculated and ideal PTAT references have similar slopes concluding that the reference voltage remains a PTAT reference over this temperature range and the p-well resistor is the cause for the decrease in output current at lower temperatures. Using another current defining element other than a p-well resistor with a linear behavior at low temperatures will allow for a constant current output over a greater variation of temperature.

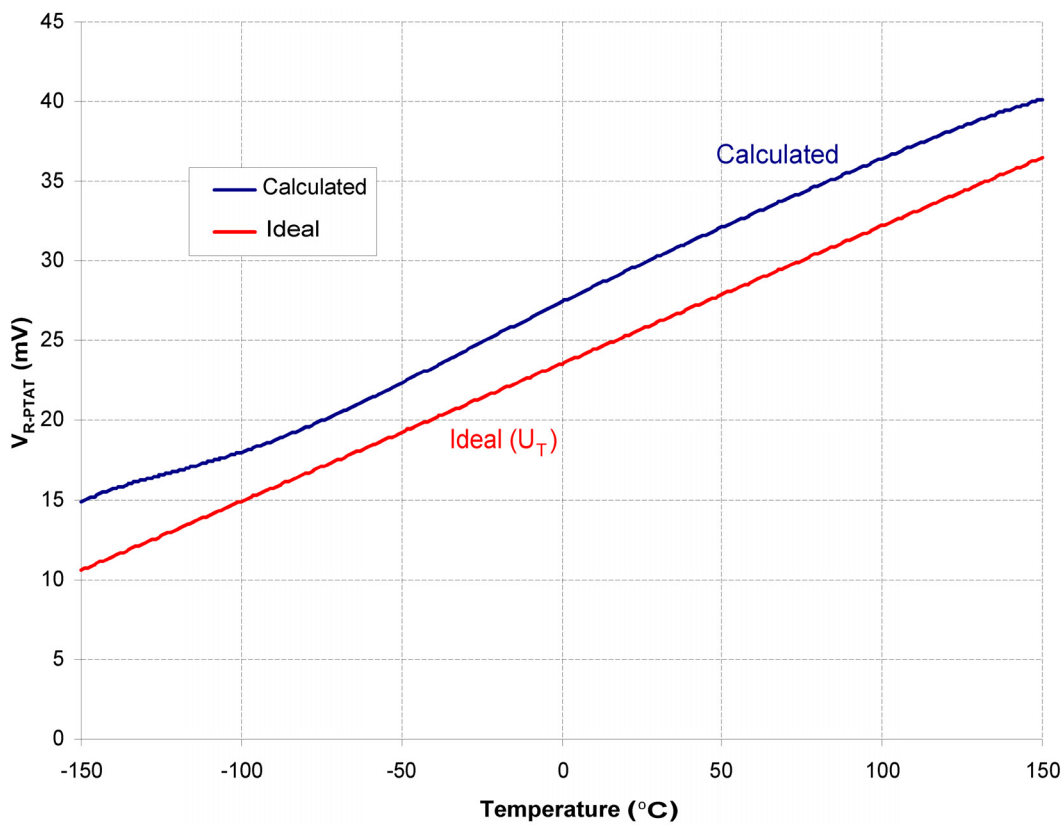

Figure 4.10: Ideal and calculated PTAT voltage reference across temperature.

Micro-Battery Voltage Charger

Measured results of the voltage charger output V_{reg} shown in Figure 3.15 across the 3-chip sample reveal that all three chips had approximately the same 4.4-V output voltage. This excellent correlation between the chips means that the output was very precise, but not very accurate since the designed output was 4.25 V. Even though the measured results deviate less than 4% from the designed voltage, this can still cause problems for the micro-batteries. Overcharging a micro-battery leads to capacity loss with a significant increase in micro-battery resistance due to cathode degradation. Lithium metal also is deposited on the anode and releases hydrogen gas when a micro-battery is overcharged [5].

Something that might not be obvious to the reader so far is the importance of the transition from current to voltage charging due to the limited capacity of the micro-battery (50 nAh). Ignoring overcharging effects for the moment, the output voltage of the voltage regulator and the voltage of the micro-battery after it has been current charged must match very closely. The mechanism by which the micro-battery's voltage state is known is the voltage monitoring ADC. This means that the voltage state denoted by a '11' digital transition at the output of the flash ADC in Figure 3.16 must correspond to the output voltage of the voltage regulator. Any mismatch between these two voltages can possibly create a situation through which a micro-battery can be flash-charged or discharged.

For instance, if the micro-battery voltage monitor transitioned to a '11' digital output at 4.2 V and the micro-battery was then transitioned to the 4.4-V regulated voltage source without any voltage loss in the transfer, the voltage potential difference between the micro-battery and the regulated voltage supply would be 0.2 V. This voltage difference would result in the voltage regulator supplying a large amount of current to the micro-battery so that the micro-battery's voltage would equalize to the voltage regulator output voltage. This instant rush of current can be quite large and result in damaging the micro-battery or degrading its capacity. The same would be true in the opposite case, but the micro-battery would have to source a large amount of current to reduce its voltage instantly.

Upon looking into the source of the 4% deviation in the output voltage of the regulator, a problem with our Cadence layout extraction method was discovered. For the preliminary design of the voltage regulator, a resistor model that modeled both first-order temperature and voltage coefficients was used. The modeled resistance was based on providing an aspect ratio and the resistance per square for the resistor in the netlist file. When translating the design into Cadence software, the aspect ratios of the resistors used in the design were directly ported over and entered into their respective resistor model in Cadence.

Cadence extraction methods for the process design kit (PDK) used to fabricate this system are based on the Spectre simulation tool. In our laboratory, SmartSpice is

preferred over Spectre for simulations, so the extracted netlists from Cadence are run through a perl script that converts the Spectre netlist to a SmartSpice compatible netlist. Through the process of extracting a netlist from either a schematic or a layout view, Cadence removes the aspect ratios of the resistors and only reports a resistance value. In order to include temperature and voltage effects of the resistors in simulations, the aspect ratio of the resistors had to be entered manually into the extracted netlists. The aspect ratios entered into the netlist were the aspect ratios reported in the schematic view of Cadence.

The problem lies in that the aspect ratio and the resistance per square given by Cadence does not relate directly to the resistance value generated by Cadence. Recall from (3.10) that the resistance of an IC resistor is

$$R = R_{sq}\left(\frac{L}{W}\right) \tag{4.2}$$

Figure 4.11 shows the properties window for a resistor used in the voltage regulator circuit. Using equation (4.2) with the reported W, L, and *Rho* (same as R_{sq}) parameters from this window yields a resistance of 30.2 kΩ and does not equal the overall resistance value reported by Cadence (25.6066 kΩ). Cadence uses a factor to scale either the effective width or length thus reducing the overall resistance that is not evident in this properties window. So, when copying the reported W and L factors from this window to include in our SmartSpice simulations, a higher resistance value was used in simulations compared to what was fabricated, offsetting certain voltage and current levels defined by resistors. This same problem relates to all of the resistors used throughout the system including the current charger and flash ADC. This problem can be easily remedied by changing the resistor model used in simulations to accept resistance and width values instead of length and width values.

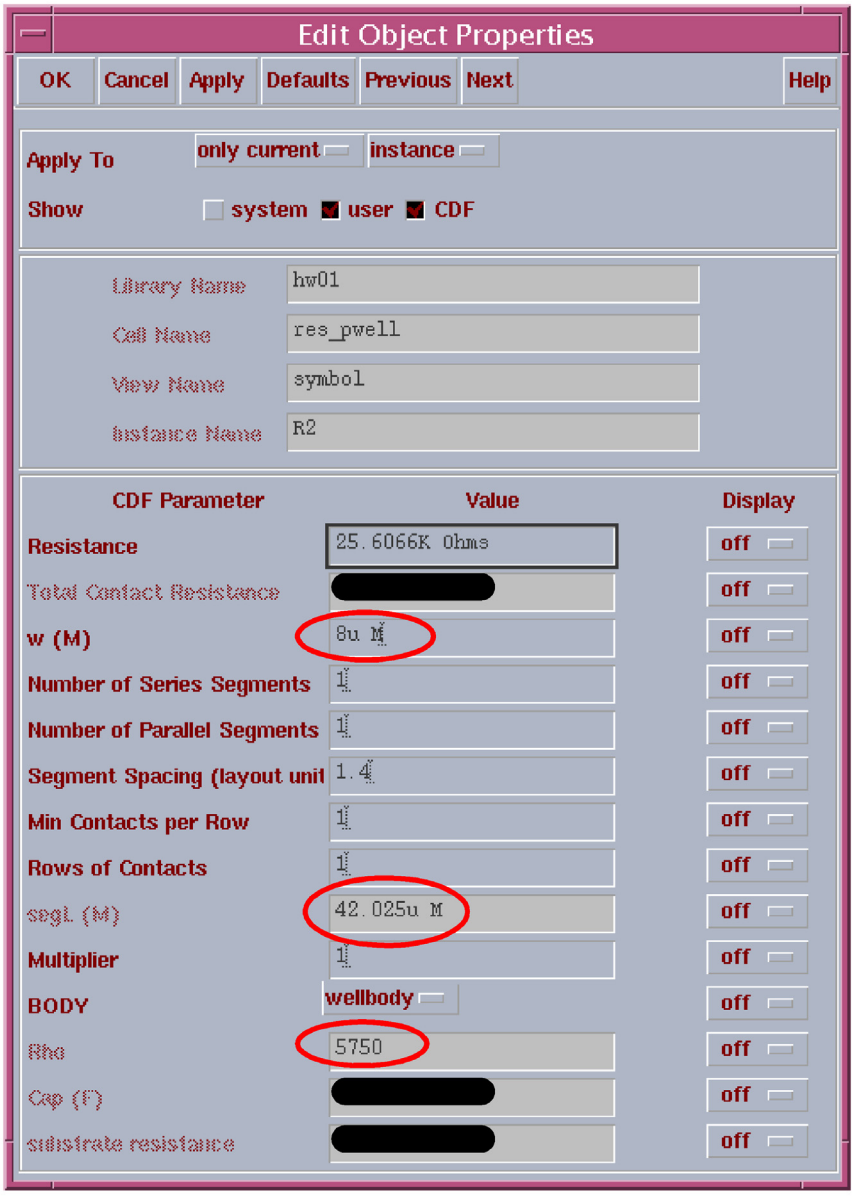

Figure 4.11: Cadence properties window of resistor.

Micro-Battery Voltage Monitor

The transition points of the of the flash ADC were also at a higher voltage than expected due to the aforementioned problem with the aspect ratio of the resistors. The typical transition points for D_0 and D_1 as V_{Batt} is swept from 0 to 5 V are approximately 3.45 and 4.76 V, respectively. Both of these values correspond to a 9% error compared to the Cadence simulated output voltages (3.17 and 4.36 V). The difference between the micro-battery voltage associated with the transitioning of D_1 (4.76 V) and the voltage regulator output (4.4 V) is 360 mV. This voltage difference is enough to cause the micro-battery to flash discharge as it is transitioned from current to voltage charging as discussed earlier.

Looking back at Figure 4.4 closer reveals two glitches in the output current at approximately V_{Batt} equal to 3.4 and 4.7 V. An enlarged plot of these two glitches for a mid-scale DAC input (400 nA) is shown in Figure 4.12. At first it was believed that the

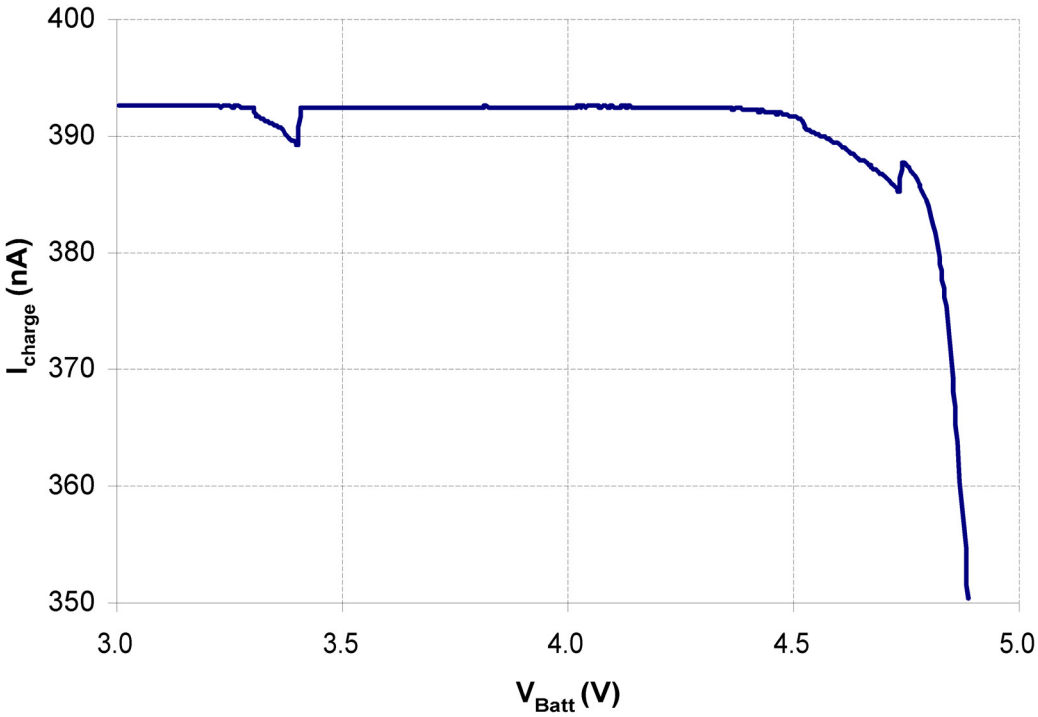

Figure 4.12: Current charger output for a mid-scale input to show glitches.

two dips in output current were an artifact of the measuring equipment because simulated DC sweeps of the charger output did not show this phenomena. However, recall that the 2-bit flash ADC that monitors the micro-battery voltage is also connected to the same I_{charge} node and its digital outputs transition at 3.45 and 4.76 V.

The 2-bit flash ADC contains two comparators whose non-inverting inputs (V_{Batt}) are connected to I_{charge} that compare the micro-battery voltage against two set voltage reference levels shown previously in Figure 3.16. As the micro-battery voltage increases, the gate voltages of the non-inverting input transistors (V_{pos}) in the comparators also increase, Figure 3.17. This increase in gate voltage with respect to the source causes the accumulation layer to become depleted followed by the creation of an inversion layer. The accumulation and inversion layers have similar capacitance values denoted by C'_{ox} described earlier. The change from accumulation to depletion, however, adds a depletion capacitance in series with the oxide capacitance [16] causing an overall decrease in capacitance value as seen in Figure 4.13. Upon the creation of the inversion layer, the

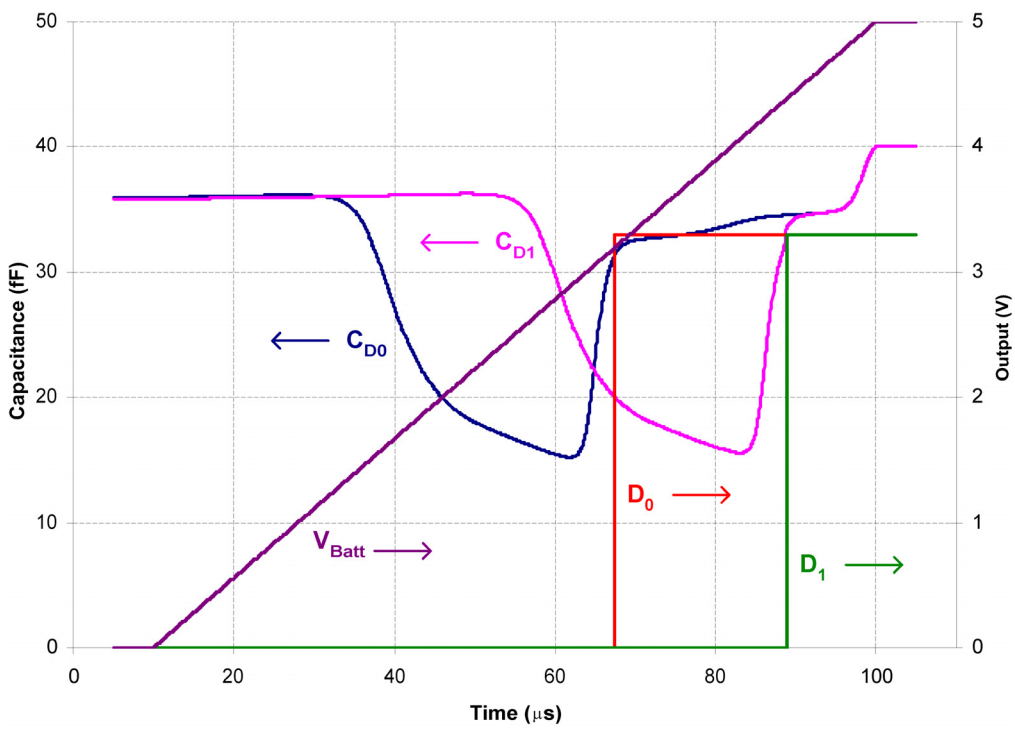

Figure 4.13: Simulation of overall gate capacitance of comparator input devices.

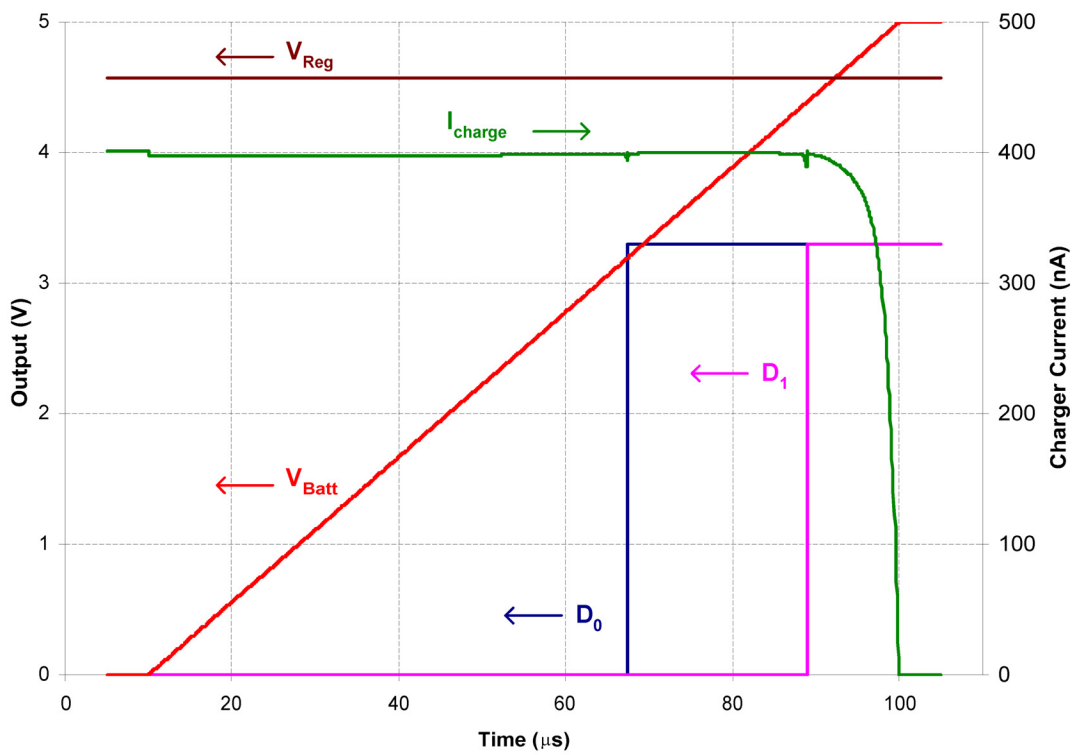

Figure 4.14: Full system-level transient simulation of power management IC.

overall gate capacitance value returns to C'_{ox}. As the capacitance changes, some of the current from the charger output will flow to the gate of the comparator inputs to reestablish equilibrium, causing what appears to be a dip in the output current characteristic in Figure 4.12.

Figure 4.14 shows a system-level transient simulation of the power management system. In this transient simulation, the correlation between the glitches in the output current and the digital output transitions is apparent. These same dips in current, however, are not visible in the simulated DC sweep of the system shown previously in Figure 3.12. In a real-life application, when current charging actual micro-batteries, this glitch in output current will not be so prominent. The amount of current needed to charge the gate capacitance of the comparators is given by

$$I = C\frac{dV}{dt} \tag{4.3}$$

The measured rise time of the micro-battery voltage as it is being current charged is in terms of tens of minutes. The measured charger current output results were obtained in seconds, corresponding to a much faster rise-time. A comparison of the effect of the rise time of a micro-battery compared to the magnitude of the current glitches was done in simulations. Results from this simulation show that as the rise time is decreased, the size of the glitches reduces. This result follows what one would expect from (4.3).

The chip micrograph of the power management IC is shown in Figure 4.15. This micrograph contains the programmable current charger, the voltage charger, and the 2-bit flash ADC, which occupies an area less than 0.34 mm^2 (excluding bond pads). Common centroid techniques were used when doing layout to maximize transistor matching where needed.

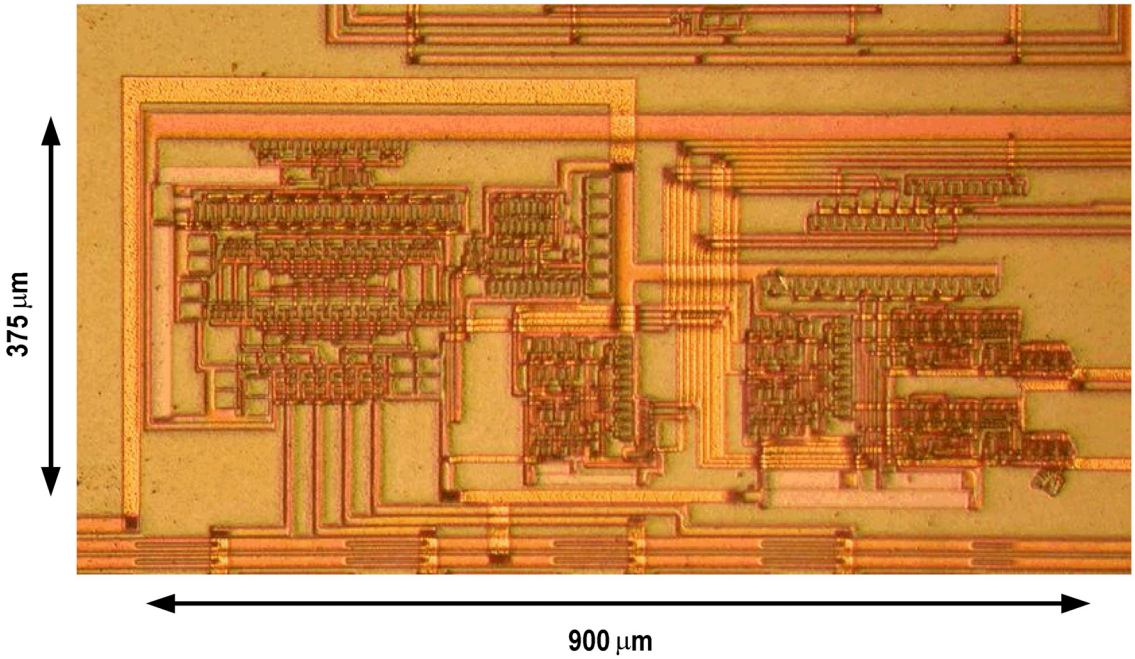

Figure 4.15: Chip micrograph of the micro-battery power management IC.

CHAPTER 5

CONCLUSION

Conclusion

This thesis presented the design and analysis of a power management IC for solid-state, thin-film, Li-Ion micro-batteries developed at JPL. The power management IC was implemented in a 0.35-μm, single-poly, PD-SOI CMOS process. Measured results revealed that a power management IC able to charge micro-batteries has been developed. Working first-pass silicon showed proper functionality of this power management IC for use on micro-batteries, even though some voltages in the voltage charger and flash ADC were higher than expected. Fixing the Cadence-induced resistor sizing error is good reason for a design revision that will provide for more accurate voltage output levels.

Temperature tests of the current charger showed that the current output was accurate and insensitive to temperature variations in the range 0–100°C. The regulated voltage supply worked properly but contained an offset error due to improper resistor sizing when converting the Cadence netlist extraction into a SmartSpice compatible netlist used for simulations. This is easily remedied by modifying the resistor model used for simulation purposes. The 2-bit flash ADC that monitors the micro-battery during the current charging phase also experienced the same resistor sizing problem causing the digital outputs to transition at higher voltages than expected. However, the digital outputs of the flash ADC did transition in the correct method as the micro-battery voltage increased.

Future Work

Some of the improvements that can be made for this system have already been implemented in a second version of the power management IC and will be discussed next. We received the latest release PDK for the first revision of this power management IC. The Cadence resistor sizing problem in the new PDK was remedied and the reported W and L values of the resistor now correlates with that of the total output resistance

reported by the Cadence properties window. Due to a delay in the fabrication schedule, measured results of the first revision power management IC are not presented in this thesis.

Part of this work was done in collaboration with the University of Idaho, also under contract with JPL. The requirement of their system is to design a microcontroller that provides the digital inputs to this system ($S3$–$S0$) and reads its digital outputs (D_0 and D_1). Per request from the University of Idaho, the 2-bit micro-battery voltage monitoring ADC was replaced with a 4-bit ADC for the first revision of this system. With the addition of two more bits of resolution, a more accurate representation of a micro-battery's voltage state can be obtained.

In addition, for the original IC to operate two external biases are needed; a 1.2-V voltage reference (V_{INP}) and a 10-µA current bias (I_{BiasN}). The first revision of this IC contains an on-chip bandgap voltage reference and beta-multiplier current reference to provide the 1.2-V and 10-µA biases, respectively. With these two additions, the IC should be able to work autonomously without any external biasing other than the required voltage supplies (V_{DDH}, V_{DDL}, and V_{SS}).

Bandgap Voltage Reference

Many circuits contained in this system relied on the use of a voltage reference (V_{INP}). As described earlier, the voltage reference was set to 1.2 V for a quick conversion to an on-chip bandgap voltage reference in the future. Bandgap voltage references combine the positive temperature coefficient (TC) of the thermal voltage, U_T, with the negative TC of the diode forward voltage in a circuit to achieve a voltage reference with a theoretically zero TC [16]. Figure 5.1 shows a schematic of the bandgap voltage reference design that was implemented in this system.

Assuming no mismatch between the nMOS pair, M_1 and M_2, the V_{GS} drop of these devices will be the same for a given current level, I. Summing the voltages around the bottom loop using KVL, ignoring any mismatch between M_1 and M_2, yields

$$V_{D1} = I \times R + V_{D2} \tag{5.1}$$

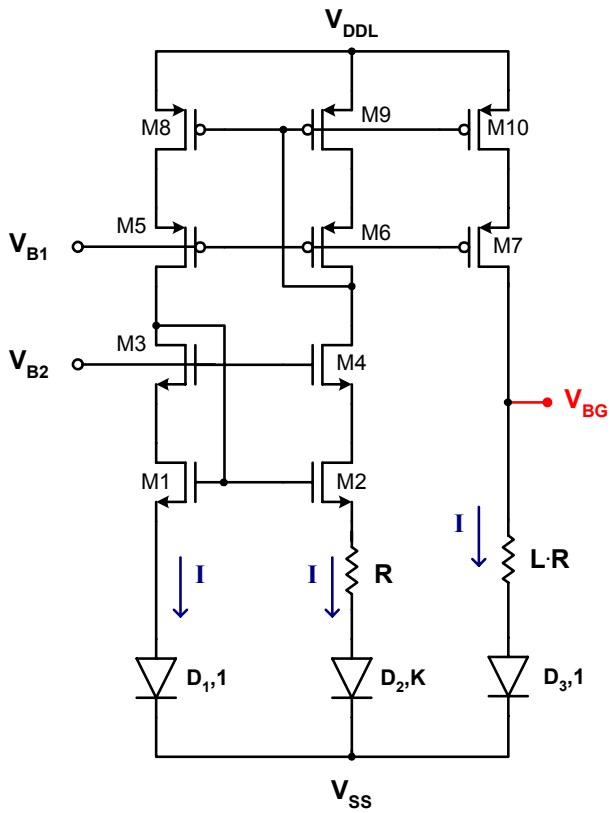

Figure 5.1: Bandgap voltage reference circuit.

where V_{D1} and V_{D2} are the diode drops associated with D_1 and D_2, respectively. The equations for the current through D_1 and D_2 are

$$I_{D1} = I_S e^{\frac{V_{D1}}{nU_T}} \tag{5.2}$$

$$I_{D2} = K \times I_S e^{\frac{V_{D2}}{nU_T}} \tag{5.3}$$

where I_S is the saturation current, K is the size ratio of the diodes ($K = D_2/D_1 = 8$), and n is very close to 1. Solving (5.2) and (5.3) in terms of voltage gives

$$V_{D1} = nU_T \ln\left(\frac{I_D}{I_S}\right) \tag{5.4}$$

$$V_{D2} = nU_T \ln\left(\frac{I_D}{K \times I_S}\right) \quad \textbf{(5.5)}$$

Substituting (5.4) and (5.5) into (5.1) and solving for I yields

$$I = \frac{nU_T \ln(K)}{R} = \frac{nU_T \ln(8)}{R} \quad \textbf{(5.6)}$$

For this bandgap voltage reference, an I of 10 μA is chosen to limit the size of R needed to generate the voltage reference.

Using a one to one ratio in the *p*MOS current mirror, the same 10-μA I flows in the output branch of the circuit into $L \times R$ and D_3. The bandgap reference voltage (V_{BG}) is then equated by

$$V_{BG} = I \times L \times R + V_{D3} \quad \textbf{(5.7)}$$

where $V_{D3} = V_{D1}$. Substituting (5.6) into (5.7) and solving for the bandgap voltage yields

$$V_{BG} = nLU_T \ln(K) + V_{D3} \quad \textbf{(5.8)}$$

The *TC* of the bandgap reference is equal to zero when

$$\frac{dV_{BG}}{dT} = nL \ln(K)\frac{dU_T}{dT} + \frac{dV_{D3}}{dT} = 0 \quad \textbf{(5.9)}$$

where the *TC* of the thermal voltage is 0.085 mV/°C and the *TC* of the diode forward voltage is approximately –2 mV/°C. This is true when

$$nL \ln(K) = \frac{2}{0.085} = 23.5 \quad \textbf{(5.10)}$$

For $K = 8$ and $n = 1$, L equates to approximately 11.3 to achieve a zero *TC*. The output voltage desired from the bandgap reference is 1.2 V, so the value of L needs to be decreased from 11.3 to 9 to achieve this voltage at the cost of increased *TC*.

The diodes in the circuit of Figure 5.1 could be implemented using any type of diode structure, but chips from a previous run using the same process contain 1× and 8×

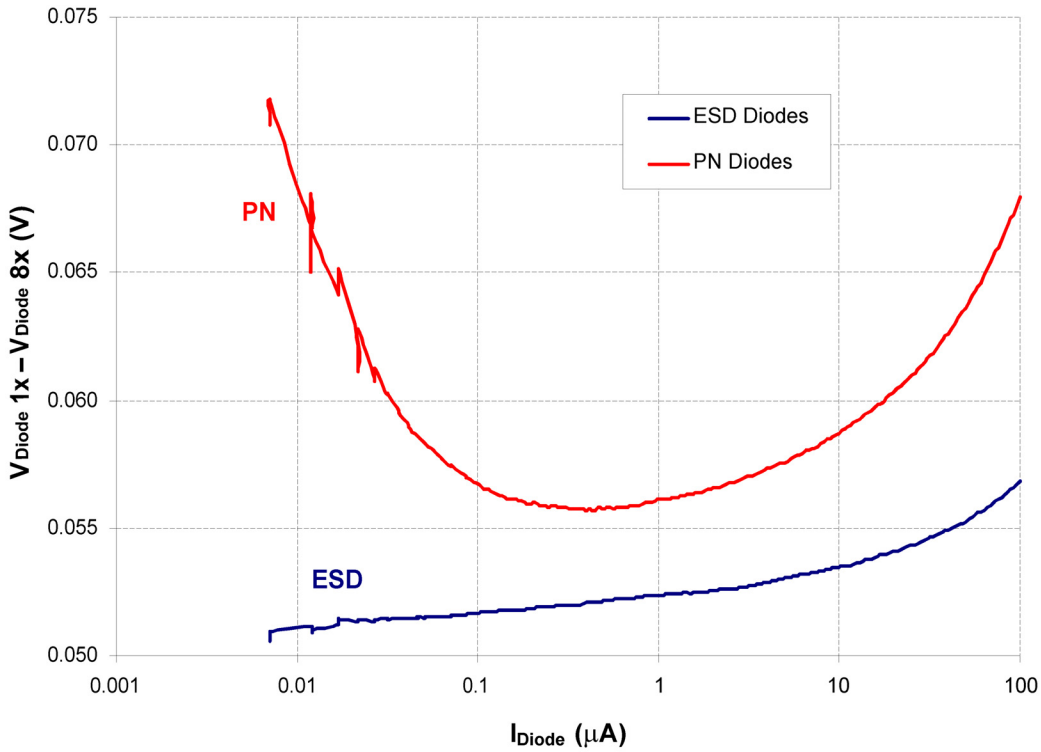

Figure 5.2: Voltage difference of 1× and 8× diode sizing for ESD and PN diodes.

samples of ESD and PN diodes. Measurements were done on these diodes to determine which would be better suited for the bandgap reference. Figure 5.2 shows a measured comparison plot of the DC characteristics of the PN and ESD diodes at room temperature. This figure was created by measuring the difference between the 1× and 8× voltage values for a given current level. The ESD diode pair has a smaller slope of its 1× and 8× voltage difference when compared to the PN diodes. This means that slight variations in the current I through the diodes should have negligible effect on the voltage across R of Figure 5.1.

Figure 5.3 shows the measured I–V characteristics of the ESD diode pair at room temperature. For a given current value (I_{Diode}), the voltage across the diodes (V_{Diode}) changes due to the sizing difference, setting up a voltage drop across the resistor R. For an I_{Diode} of 10 μA, the voltage difference of the diode pair is 54 mV, which can also be discerned from the ESD diode voltage difference in Figure 5.2 at a 10-μA current level.

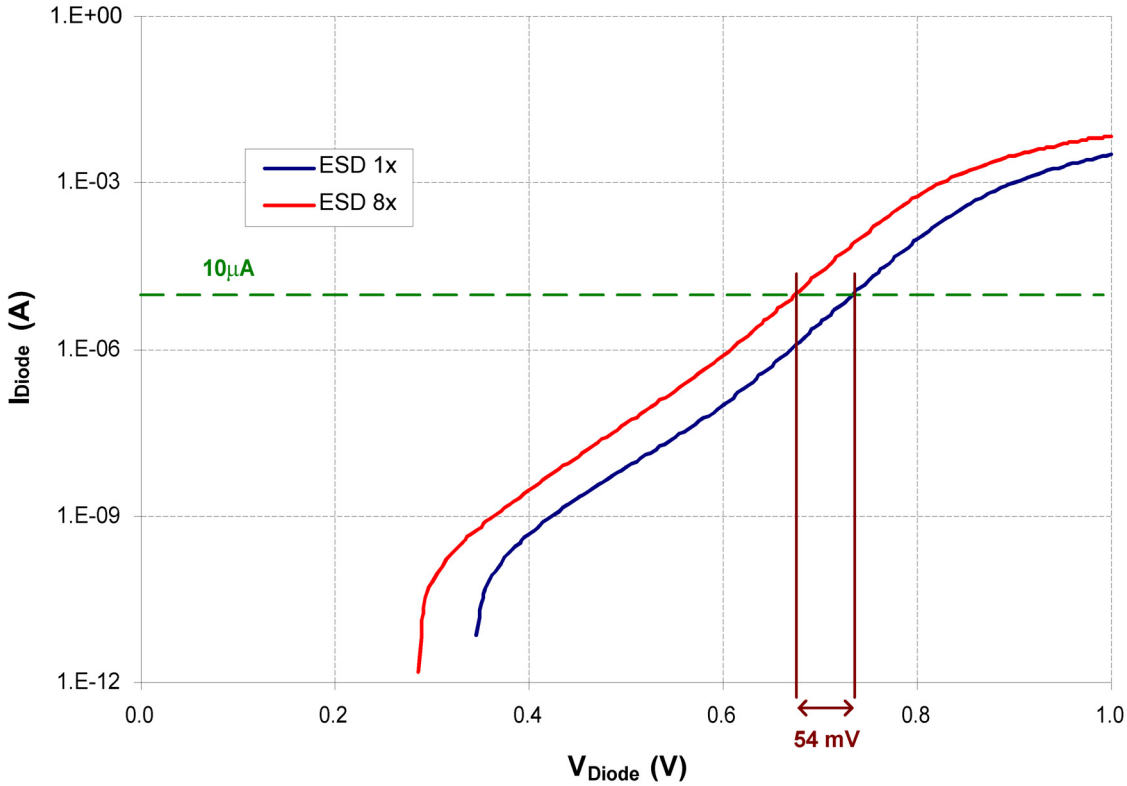

Figure 5.3: Measured I–V characteristics of 1× and 8× ESD diodes.

In order to generate the wanted 10-μA current, the *R* of Figure 5.1 needs to be 5.4 kΩ, which can be provided by a parallel combination of resistors using the p-well resistor option.

Simulations of the bandgap voltage reference are shown in Figure 5.4. The output voltage across temperature is presented along with its corresponding temperature coefficient. A generic diode model and a resistor model with first-order temperature effects were used in these simulations. Remember from Figure 3.4 that the resistor model used in simulations does not track measured resistance values below –50°C. Between 0–100°C, the temperature coefficient of the bandgap output voltage is approximately –100 ppm/°C, which should provide for a stable voltage reference across temperature variations in this range.

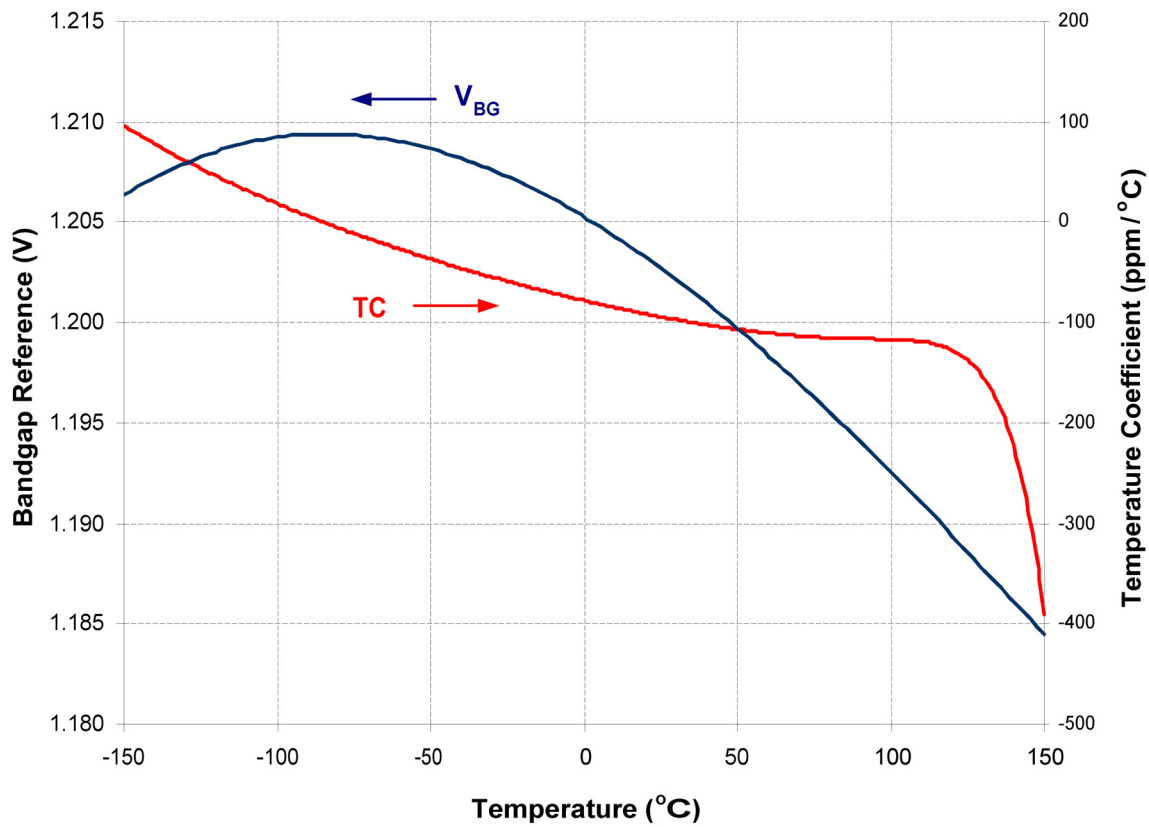

Figure 5.4: Simulation of bandgap reference temperature performance.

Beta-Multiplier Current Reference

A beta-multiplier self-biased current reference topology was chosen to provide the 10-µA current reference on chip. The schematic of the current reference is shown in Figure 5.5. This topology looks similar to the low-level current reference used in the current charger of the micro-battery system, but in this topology, all MOSFETs are biased in strong inversion.

Summing the voltages around the bottom half of the loop yields

$$V_{GS1} = V_{GS2} + IR \tag{5.11}$$

Using the first-order theory square-law equation

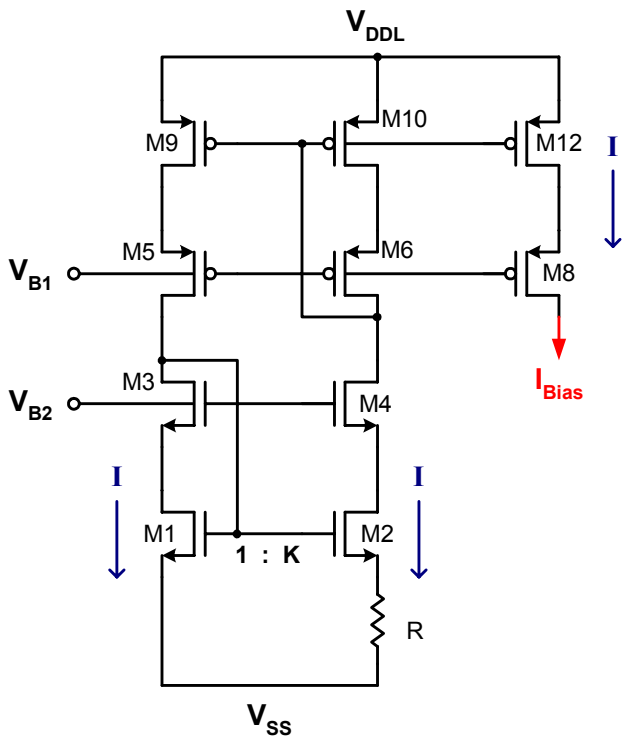

Figure 5.5: Beta-multiplier self-biased current reference.

$$I = \frac{\beta}{2}\left(V_{GS} - V_{THN}\right), \tag{5.12}$$

the V_{GS} voltages of M_1 and M_2 can be written in terms of current I as

$$V_{GS1} = \sqrt{\frac{2I}{\beta_1}} + V_{THN} \tag{5.13}$$

and

$$V_{GS2} = \sqrt{\frac{2I}{K \cdot \beta_1}} + V_{THN} \tag{5.14}$$

where $\beta_1 = \mu_n C'_{ox}(W/L)_1$, $\beta_2 = K \times \beta_1$, and V_{THN} is the nMOS threshold voltage. Note that here, thanks to SOI's unique isolation properties, body effect is eliminated to provide

$V_{THN1} = V_{THN2}$ (assuming perfect matching). Solving for I in (5.12) using (5.13) and (5.14) gives

$$I = \frac{2}{R^2 \beta_1}\left(1 - \sqrt{\frac{1}{K}}\right)^2 \qquad \textbf{(5.15)}$$

The K size factor in the current mirror M_1 and M_2 must be greater than 1 for this design to work. The same current flows through both M_1 and M_2, but since M_2 has a larger area, the V_{GS} voltage drop of M_2 is smaller than M_1, allowing for a voltage drop across the resistor R. Simulations show that using a K = 1.5 and a R = 6.4 kΩ gives the desired 10-μA bias current.

4-Bit Flash ADC

To increase the resolution of the micro-battery voltage output, the 2-bit flash ADC from the first chip was increased to a 4-bit flash ADC. This higher resolution voltage monitoring circuit will be used by a microcontroller to determine if a micro-battery's capacity has been degraded to a point where it is no longer useful as a battery as well as monitor its voltage through the current charging process. A micro-battery will either fail as a short or open circuit depending on the circumstances of its degradation due to repetitive deep discharge cycles [5].

The schematic of the 4-bit flash ADC is shown in Figure 5.6. This schematic resembles that of the 2-bit flash ADC shown previously in Figure 3.16. The basic principle of operation is the same but now with more comparators and reference levels established to distinguish between smaller voltage changes. Since a higher number of comparators were used in the new voltage monitor, the 16-bit temperature code output from the flash ADC had to be converted to a 4-bit binary output form using a priority encoder.

Simulation results of the upgraded flash ADC with priority encoder is shown in Figure 5.7. The simulation was performed by sweeping the micro-battery voltage (V_{Batt}) from 0 to 5 V and viewing the digital output (D_0–D_3) transitions. The digital outputs were scaled from their nominal 3.3-V output, representing a logic '1', to a level that is

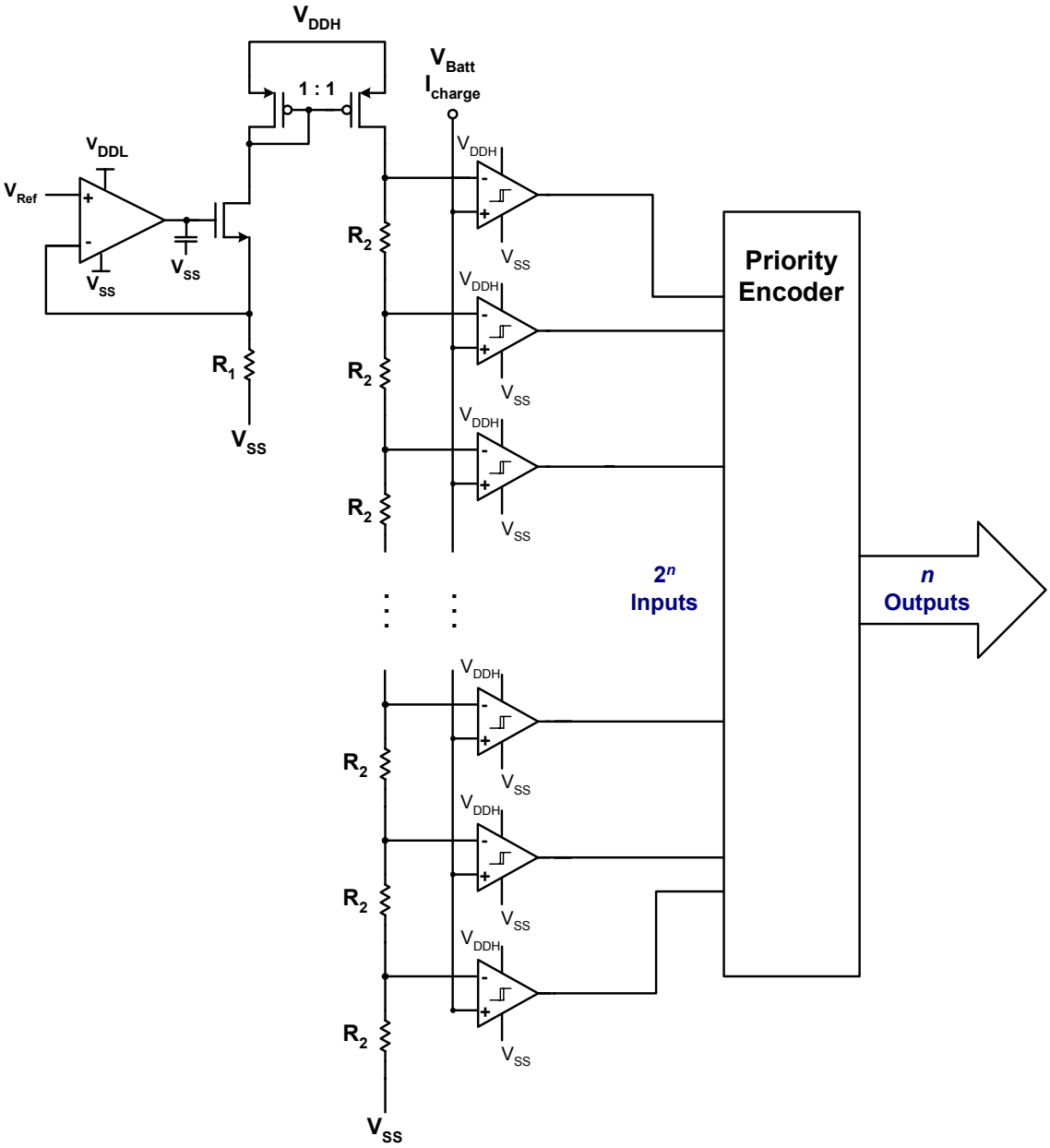

Figure 5.6: 4-bit flash ADC architecture with priority encoder.

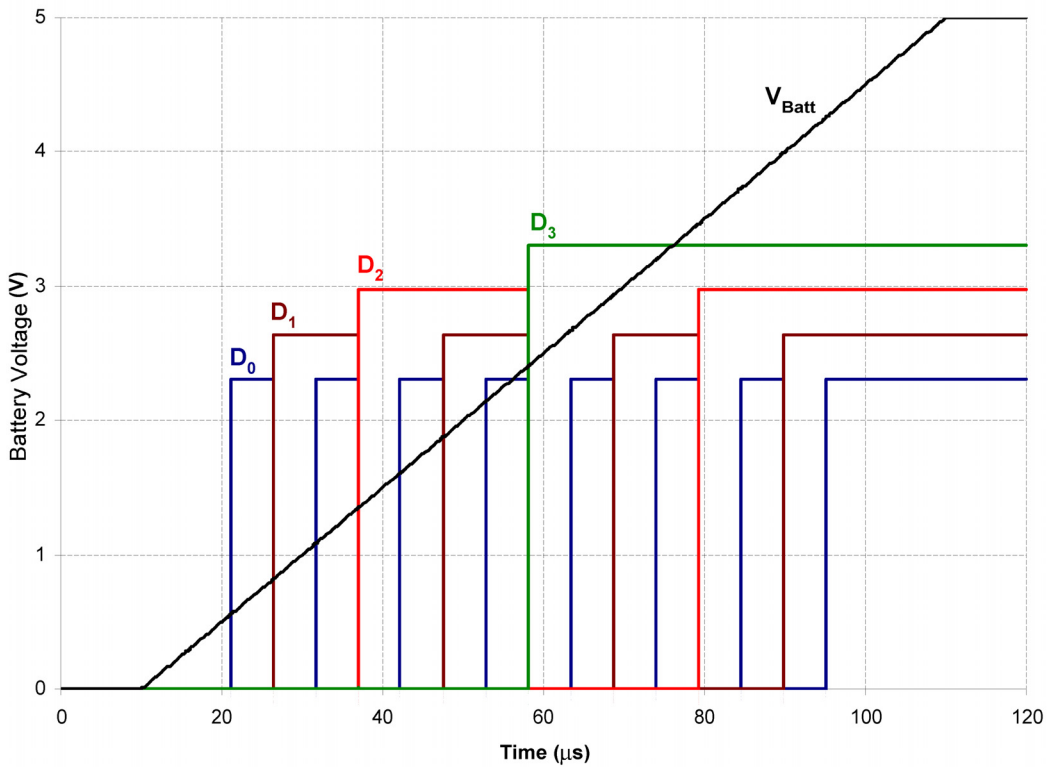

Figure 5.7: Transient simulation of 4-bit flash ADC with priority encoder. (Digital output levels scaled to show transitions—normally logic '1' = 3.3 V.)

better suited for viewing the details of their switching voltages. To better illustrate the digital transition points, Table 5.1 provides a list of the digital output transition points as V_{Batt} is swept from 0 to 5 V. As the micro-battery voltage reaches the specified level in the table, the output transitions to the corresponding digital output state.

Table 5.1: Tabulated digital output transitions from 4-bit flash ADC.

V_{Batt} (V)	D_3 D_2 D_1 D_0
0	0 0 0 0
0.553	0 0 0 1
0.817	0 0 1 0
1.081	0 0 1 1
1.344	0 1 0 0
1.608	0 1 0 1
1.873	0 1 1 0
2.139	0 1 1 1
2.404	1 0 0 0
2.668	1 0 0 1
2.931	1 0 1 0
3.195	1 0 1 1
3.463	1 1 0 0
3.725	1 1 0 1
3.993	1 1 1 0
4.258	1 1 1 1

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APPENDIX

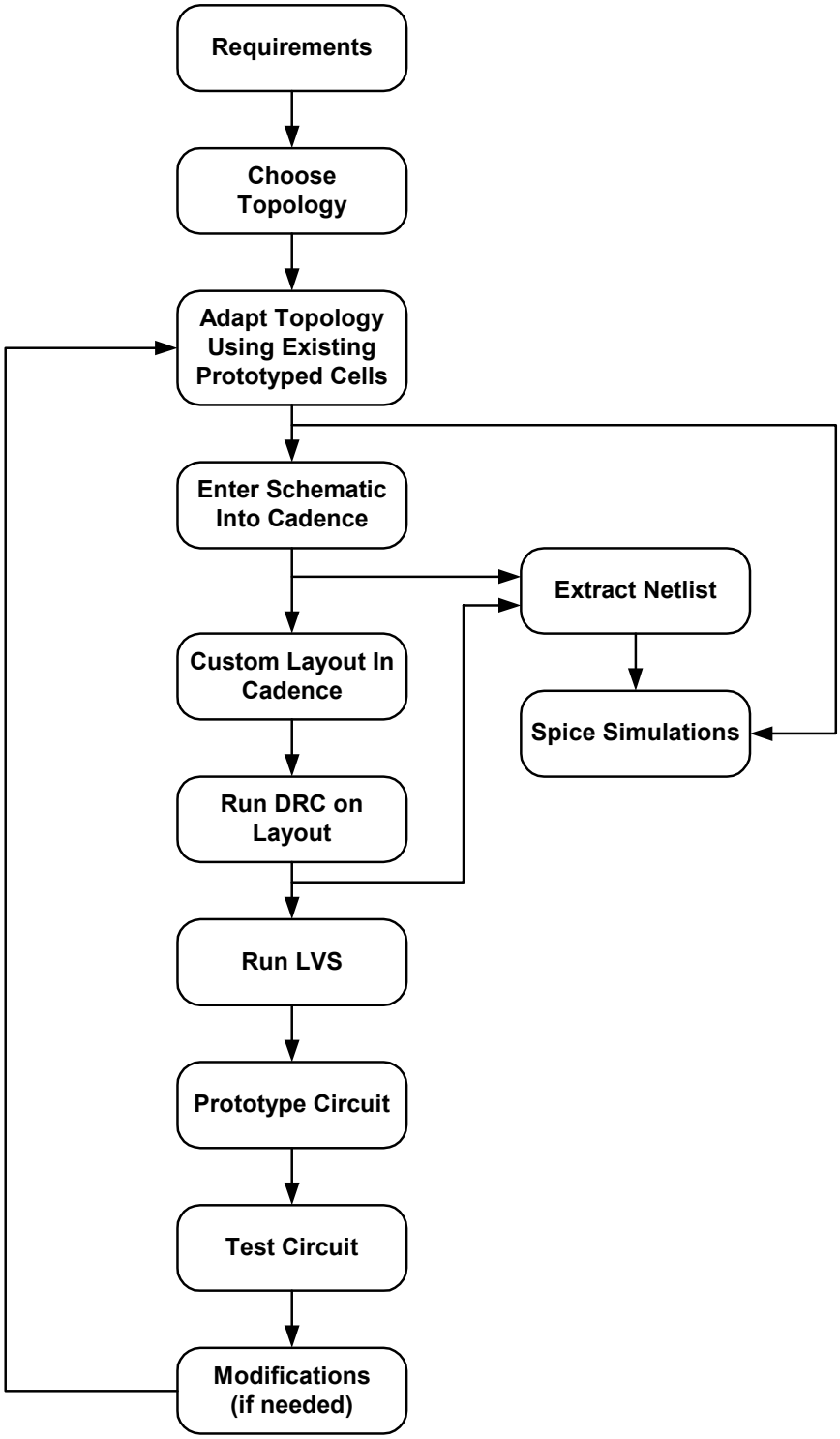

Figure A-1: Design flow process.

VITA

Jeremy Jackson was born in Shreveport, Louisiana on September 12, 1979. He grew up in South Texas after having lived briefly in New Jersey. His high-school career took place in Memphis, Tennessee where he attended Houston High School from which he graduated in 1997. Jeremy attended the University of Tennessee, Martin for two years on an academic scholarship and transferred to the University of Tennessee, Knoxville to complete his studies in Electrical Engineering. His studies were focused in both analog and digital design. He completed his undergraduate degree in May 2002 with a Bachelor of Science in Electrical Engineering, graduating *Magna Cum Laude*.

After completion of his undergraduate degree, Jeremy began work on the Master of Science in Electrical Engineering degree at the University of Tennessee, Knoxville. He worked as a graduate research assistant in the Integrated Circuits & Systems Laboratory under the supervision of Dr. B.J. Blalock during his time as a master's student. Jeremy was awarded the Analog Devices Fellowship his first year as a master's student, which facilitated an intern position for him at the Analog Devices Inc. design facility in Greensboro, North Carolina.

Upon completion of his master's degree, Jeremy will pursue a job in the field of analog/mixed-signal circuit design.