GaN vs. Si for Class D Audio Applications

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For my little brother,

Carson Ryan Sangid.

Remembering you is

the best part of my day.

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Abstract

The demands and applications of modern power electronics are quickly moving past the maximum performance capabilities of Silicon devices. As the processing of Wide Bandgap (WBG) materials matures and the commercial availability of WBG devices grows, circuit designers are exploring many applications to exploit the performance benefits over traditional Silicon devices. This work examines the under-explored application of GaN-based Class D audio by providing a side-by-side comparison of enhancement-mode GaN devices with currently available Silicon MOSFETs. It is suggested that GaN in Class D audio will allow for lower heat radiation, smaller circuit footprints, and longer battery life as compared to Si MOSFETs with a negligible trade-off for quality of sound.

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List of Nomenclature

ϵ_r	Relative permittivity or dielectric constant
η	Efficiency
μ	Electron mobility
ω_0	Critical angular frequency given in units of rad
$\mathrm{SNR}_{\mathrm{dB}}$	SNR given in units of dB
A_v	Voltage gain
A_{mid}	Mid-band voltage gain
$A_{v(\mathrm{dB})}$	Voltage gain in units of dB
d	Duty cycle
E_c	Energy at the bottom edge of the conduction band
E_g	Bandgap energy
E_v	Energy at the top edge of the valence band
f_0	Critical frequency given in units of Hz
f_{clk}	Clock frequency
f_{high}	High cutoff frequency
f_{low}	Low cutoff frequency

f_{sw}	Switching frequency
f_{test}	Frequency of test signal
k	Small signal gain constant
m	Some arbitrary number belonging to the set of all integers
n	Some arbitrary number belonging to the set of all integers
P_{in}	Input power
P_{loss}	Lost power
$P_{out(max)}$	Maximum output power
P_{out}	Output power
Q_g	Gate charge
$R_{DS(ON)}$	On-state drain-to-source resistance
R_{fb}	Feedback Resistor
R_{in}	Input Resistor
R_{load}	DC load impedance
s	Laplace transform variable or complex variable
T_{max}	Maximum temperature
v_s	Carrier velocity
V_{dd}	FET logic positive supply voltage
$V_{do(RMS)}$	RMS voltage of distortion of AC signal output
$V_{DS(max)}$	Maximum DC drain-to-source voltage before breakdown
$V_{GS(max)}$	Absolute maximum gate-source voltage rating

V_{GS}	Gate to source voltage for FET device
$V_{in(RMS)}$	RMS voltage of AC signal input
v_{in}	AC signal input voltage
$V_{no(RMS)}$	RMS output voltage of noise with grounded input
$v_{out(max)}$	Maximum AC signal output voltage
$V_{out(peak)}$	Peak amplitude of AC signal output voltage swing
$V_{out(RMS)}$	RMS voltage of AC signal output
v_{out}	AC signal output voltage
$V_{so(RMS)}$	RMS output voltage before peaking when driven by a test sine-wave
V_{ss}	FET logic negative supply voltage
V_{TH}	Gate to source threshold voltage for FET device
2-D	Two dimensional
2DEG	Two dimensional electron gas
AC	Alternating current
AC	Alternating current
ADC	Analog to digital converter
AlGaN	Aluminum Gallium Nitride
AM	Amplitude modulation
BJT	Bipolar junction transistor
BTL	Bridge-tied load
CoolMOS®	Superjunction MOSFET, registered trademark of Infineon Technologies

DAC	Digital to analog converter
DC	Direct current
DIP	Dual in-line package
eGaN®	Enhancement-mode GaN, registered trademark of EPC
EMI	Electro-magnetic interference
EPC	Efficient Power Conversion (Company Name)
FET	Field-effect transistor
FOM	Figure of Merit
FPGA	Field-programmable gate array
GaN	Gallium Nitride
HCI	Hot carrier injection
HEMT	High-electron-mobility transistor
HiFi	High fidelity
HS	Heat sink
IC	Integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-gate bipolar transistor
IMD	Intermodulation distortion
LC	Inductor and Capacitor
LDO	Low-dropout regulator
LED	Light-emitting diode

MOSFET	Metal-oxide-semiconductor field-effect transistor
NexFET™	N-channel power MOSFETs, registered trademark of Texas Instruments
PCB	Printed circuit board
PCM	Pulse code modulation
PDM	Pulse density modulation
PWM	Pulse width modulation
RF	Radio frequency
RLC	Resistor, Inductor, and Capacitor
RMS	Root mean square
RQ	Figure of merit for FET devices, the product of on-resistance and gate charge
SE	Single ended
Si	Silicon
SiC	Silicon Carbide
SNR	Signal to noise ratio
THD	Total harmonic distortion
THD+N	Total harmonic distortion plus noise
USB	Universal Serial Bus
WBG	Wide bandgap

Chapter 1

Introduction

The demands and applications of modern power electronics are quickly approaching a plateau of (what appears to be) the maximum performance capabilities of Silicon (Si) devices. Motivated by the desire for increased efficiency, new wide bandgap (WBG) materials are now competing directly with the matured technology of Si which has proven to be limited with respect to "blocking voltage capability, operation temperature, and switching frequency [1]."

As the processing of GaN matures and the abundance of commercially available choices grow, circuit designers are exploring many applications that could exploit the performance benefits of GaN over traditional Silicon devices. For this thesis, enhancement-mode GaN FETs are examined in a Class D audio amplifier. It has been shown that GaN provides an opportunity to improve the Si-based Class D audio amplifier with less heat radiation, smaller circuit footprint, and longer battery life [2]. This thesis will add supplemental information suggesting that these performance improvements of using GaN over Si can be leveraged with negligible trade-off for quality of sound in Class D audio applications.[1]

[1] For this work, sound quality will be quantified by the total harmonic distortion (THD) and the signal to noise ratio (SNR); these metrics are further defined in Section 2.4.4

1.1 Motivation

Scouring through Google search engine and The University of Tennessee Library's online database for 'WBG," "SiC" or "GaN," combined with "Class D audio," yields an extremely limited pool of cite-worthy pieces. This was initially discussed as potential reason to pass on the selected topic. However, this left considerable space for this work to ask and answer simple questions that might influence designers on choosing a GaN device for their Class D audio amplifier and contribute publications to fill the void.

The inherent performance benfits of using GaN over Silicon in power electronics switching circuits with respect to faster switching speeds, higher power density, and higher power efficiency have been widely discussed in other previous works [1]; yet, little is shown to support the sonic advantages or disadvantages of using GaN in Class D audio. What is shown for GaN enhancement-mode power high-electron-mobility transistors (HEMTs) is that a higher rate of quantum traps at the gate-drain surface and also in the buffer region lead to the undesirable phenomena of a dynamic $R_{DS(ON)}$ [3].[2] This generation and regeneration of charge carriers can be seen in any electronic amplifier and categorized as low frequency noise within the audio band with either a brown or pink noise color [4]. It can then be assumed that the audio performance of a GaN-based Class D audio amplifier could be less than that of the traditional Silicon examples; furthermore, no sources exist to either prove or disprove this assumption.

1.2 Goals

The goals of this work are: (a.) to provide a side-by-side comparison of GaN and Si devices in a Class D audio amplifier; (b.) demonstrate any benefits of using GaN over Si; (c.) categorize any application specific disadvantages to GaN over Si; and (d.) contribute literature to this under-explored application of GaN. This was accomplished by developing a Class D audio amplifier with multiple interchangeable output stages designed for each selected FET device. An experimental test was designed explore the performance of each device and also

[2] Note that topics specific to enhancement-mode GaN devices such as the dynamic $R_{DS(ON)}$ will be omitted from the body of this thesis, please see Appendix A for a brief overview of GaN devices.

to evaluate whether the device material had any significant impact on the overall sound quality of the amplifier.

Chapter 2

Background and Literature Review

2.1 Overview of Power Electronics Themes

2.1.1 Power Electronics Switching Circuits

In general, power electronics is the process and control of electric power from source to load. The fundamental block within the field of Power Electronics is the switching converter (See Figure 2.1 [5]). The basic switching converter contains input and output power ports as well as controller inputs. The converter can be designed as a *dc-dc converter*, *ac-dc rectifier*, *dc-ac inverter*, or perhaps an *ac-ac cycloconverter*. Regardless of the designed task of the converter, the operation is similar: a raw input power is processed as determined by the control input resulting in a power output with conditioned voltage, current, or frequency [5, 6].

The main performance metric for a power electronics circuit is the ability to convert the input power to the output with minimal power lost between these two points. This is the efficiency of the converter and given by Equation (2.1).

$$\eta = \frac{P_{out}}{P_{in}} \tag{2.1}$$

The losses of a converter can be modeled with Equation (2.2) [5].

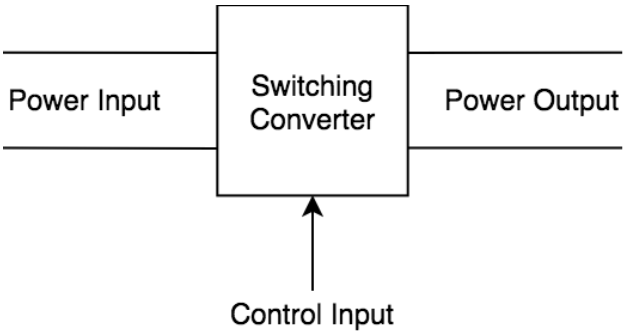


Figure 2.1: Switching converter, basic block diagram

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right) \tag{2.2}$$

In modern power electronics, the processing of power is typically completed by active devices made of some semiconducting material.[1] In cases where FETs are selected as the active device, the circuit will be designed so that the transistor will only operate in either fully-on ($V_{GS} \gtrapprox 2 \cdot V_{TH}$) or fully-off ($V_{GS} < V_{TH}$), where V_{GS} is the gate to source voltage and V_{TH} is the gate to source threshold voltage required to activate the FET device. This is called "switch-mode" operation and because of this within Power Electronics Engineering the semiconducting devices are simply called "switches" [5].

A major source of power losses in a converter are the switching losses inherent to the chosen switch. In an ideal switch, the transition from fully-on to fully-off and *vice verse* would be instantaneous. This is not the case for devices in practical applications where transition times can be on the order of nanoseconds up to microseconds. The reason for this delay is the amount of charge required by the devices to move between states. The charge must be applied to the gate of the device to move to fully-on and then the charge must be removed to transition to fully-off state. There are additional parasitic charges that must be satisfied and are inherent to the device's construction such as the body diode's reverse recovery charge. Because the energy associated with these charges is not directly commuted to the output of the converter, they exist as losses [5, 6]. [2]

[1] Only FETs will be evaluated within this thesis, other semiconductor devices such as diodes, IGBTs, BJTs, or thyristors will be omitted from the discussion.

[2] Other significant sources of losses in a converter include device conduction loss and inductor losses consisting of core loss and copper loss [5].

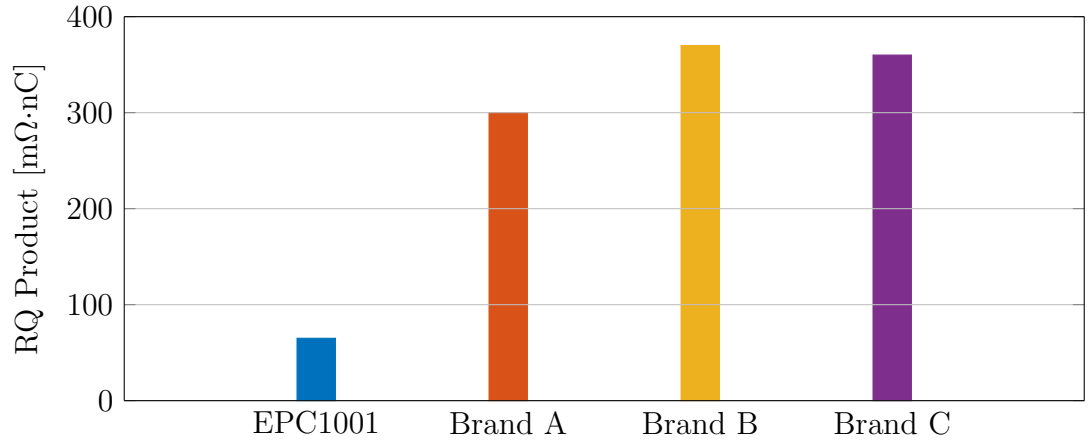
For device designers, the main goal for improvements has been to minimize the associated losses and increase the overall efficiency in application. A device that requires smaller charges will turn on and off faster; a device with lower drain-to-source resistance will dissipate lower power while on; and a device that can switch faster will require a smaller inductor and result in lower inductor related losses. Recent improvements with power devices include how CoolMOS® and IGBTs have surpassed the theoretical maximum conductivity of simple verticle majority carrier devices [7]. However, the current leaps that are being made with Silicon devices are small strides compared to the performance upgrades offered by GaN and other WBG alternatives.

2.1.2 GaN Power Electronics Devices

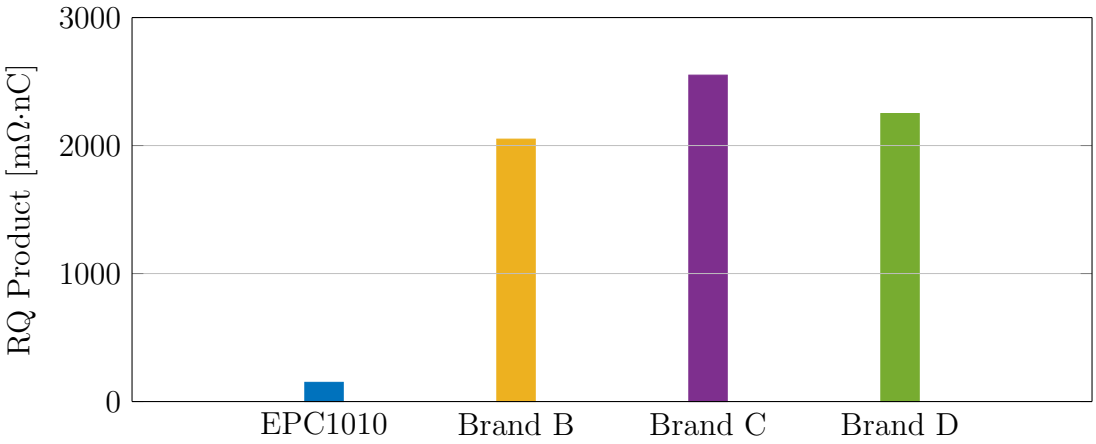
GaN HEMTs first made an immediate impact in RF applications with the introduction of devices by Eudyna Corporation in Japan in 2004. The use of these first GaN devices was limited because of their depletion-mode (normally-on) operation. The main problem with depletion-mode devices is that in the event of a controller or system level fault, there is a short circuit between drain and source which could damage the power source, power load, or the device itself. It was not until 2009 that EPC introduced the first examples of enhancement-mode GaN on Si substrates. These EPC devices were designed to be drop-in improvements for their Si counterparts [7].

The enhancement-mode GaN devices immediately showed a higher performance in switching applications. One of the main reasons for this performance boost was the capability for a higher critical electric field than silicon. This allowed for GaN devices to block higher drain-to-source voltages with a lower on-state resistance as compared to Si devices [7].

In Si power MOSFETs, there exists a trade-off between the ability to conduct current and the gate charge (Q_g) required to to transition from OFF to ON states. The RQ product ($R_{DS(ON)} \times Q_g$) is a figure of merit (FOM) that is used to evaluate this trade-off between different technologies or processes, where the lower RQ product is typically more desirable. Figure 2.2 shows the RQ product of the original EPC eGaN® devices of 100 V and 200 V ratings, EPC1001 and EPC1010 respectively, compared to that of the benchmark Si devices available at the time of EPC's release. Lidow [7] notes that although Si had made "great"



(a) 100 V Devices



(b) 200 V Devices

Figure 2.2: RQ Products for 100 V and 200 V EPC eGaN® compared with unnamed benchmark Si devices at time of EPC's release

improvements prior to this comparison, Si could not "come close" to the FOM achieved by EPC's first generation enhancement-mode HEMTs.[3]

2.2 Common Audio Power Amplifier Classes

This section provides an overview of many common topologies of audio power amplifiers and discusses their unique balance of the trade-off of sound quality and power efficiency.

[3] For further information on the current processing capabilities, device structure, and applications of GaN, the reader should visit Appendix A where a brief survey of recent works has been compiled.

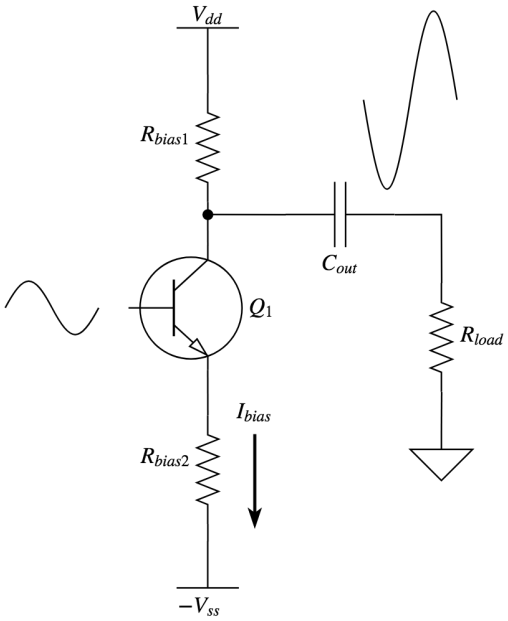


Figure 2.3: Common Class A audio power amplifier schematic

2.2.1 Class A

Class A audio power amplifiers characteristically have the greatest performance with respect to distortion, but also have the lowest efficiency when compared to the other classes of audio power amplifiers. A common Class A output stage is shown in Figure 2.3. The bias resistors (R_{bias1} and R_{bias2}) control the DC bias current of Q_1 as well as the voltage and current swing capable of being delivered to the load. By supplying a separate constant DC bias current to the base of Q_1 (through network not shown in the figure) the device is always on. It is because of this, there are no artifacts in the output signal resulting from switching noise or crossover distortion; however, nearly all the dc bias current is blocked by C_{out} and travels through the emitter of Q_1 making a significant impact on the total efficiency (η). The ideal efficiency of a Class A power amplifier is $\eta = 25\,\%$; however, in pracital applications, values of $\eta < (15\,\% \sim 20\,\%)$ are more likely to be seen [8].

The losses in a Class A occur mostly in the output transistors and this presents a design challenge for applications of higher power delivery to the speaker load. Additionally, devices capable of large power dissipation and techniques for thermal management consume spacial volume, making Class A an impractical selection for applications where power density is a

concern. Typical applications for Class A amplifiers are in HiFi (high fidelity) audio systems designed for low power operation or any power level where low distortion takes precedence to either efficiency or the system's spacial volume.

2.2.2 Class B and AB

Class B amplifiers offer a considerable improvement to the efficiency of the Class A amplifier, but at a cost to signal fidelity. Both Class B and AB use either a push-pull or complementary arrangement of devices. A complementary arrangement is shown in Figure 2.4, where two complementary devices (n-type and p-type) are used [8].[4] A push-pull arrangement uses two devices of same type (typically n-type), and is driven a pair of complementary signals, meaning: two coherent signals with a 180° difference in phase angle. In either arrangement, the higher-side device sources current to the load and a lower-side device sinks current while each device conducts for only a half cycle. This method results in a much higher ideal efficiency $\eta = 78.5\,\%$, which is a $3\times$ improvement to Class A [2].

The higher efficiency is a trade-off resulting in higher distortion. Because the devices require some energy to move from cut-off mode to linear operation, a gap exists between the devices turning on and off in which both devices are not in linear operation. This effect introduces some deviation of the output signal from the input signal and is categorized as crossover distortion. The Class AB amplifier attempts to mitigate the effect of crossover distortion of the Class B by maintaining a small constant current bias through the output devices. A common Class AB output stage is shown in Figure 2.4. The diodes provide a base-emitter bias voltage in addition to R_{bias1} and R_{bias2} providing the bias current needed so that both devices conduct within the "crossover region [9]."

Though Class B and AB amplifiers are more efficient than the Class A, there still exisist significant instantaneous power dissipation when the output signal is at midrail forcing large voltage drops across the devices [2]. Because of this, consideration must still be given to thermal management for higher power applications. Class AB audio power amplifiers are

[4] The output stage schematic diagram in Figure 2.4 is a general case and does not include the resistors between the emitter of each device and C_{out} which is to prevent the phenomenon of thermal runaway occurring during extended duration of high current loading of the devices.

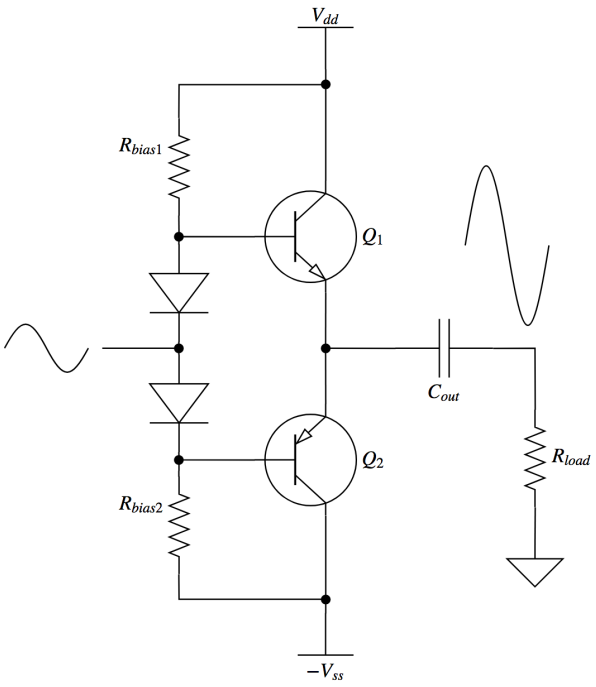


Figure 2.4: Common Class AB complementary audio power amplifier schematic

widely used in many applications, demonstrating a balanced trade-off between signal fidelity and efficiency.

2.2.3 Class D

The main advantage that Class D has over the other amplifier classes is a far lower power dissipation, but this comes as a trade-off since Class D can also be described as having the poorest sound quality. However, lower power dissipation translates directly to less heat, smaller circuit footprint, and longer battery life [2].

In a Class D amplifier, an input signal is modulated into a binary series of pulses known as a pulse code modulation (PCM) signal. There are several methods for generating the PCM signal and this topic is discussed further in Section 2.3.1. The PCM signal and it's complementary PCM signal are then used to drive a push-pull output stage.

A common Class D output stage is shown in Figure 2.5. In the figure, Q_1 and Q_2 are ideally only in either cut-off or fully-on modes of operation, yielding a theoretical efficiency of $\eta = 100\,\%$ [2]. However, an efficiency of $100\,\%$ is not achievable in practical applications since

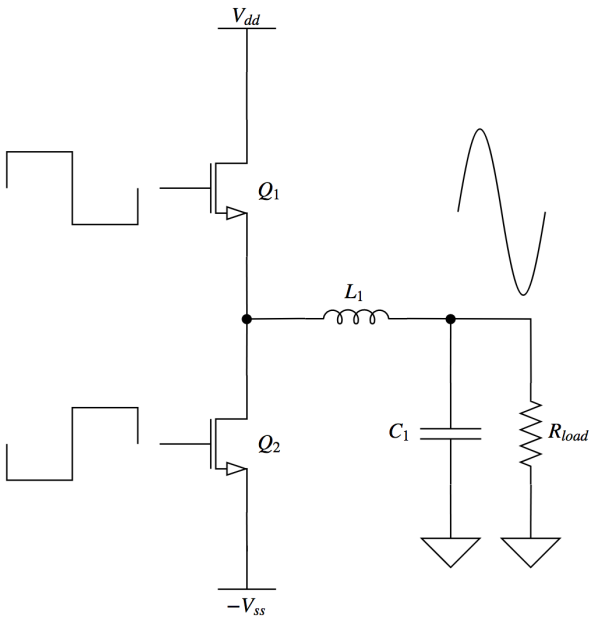


Figure 2.5: Common Class D power amplifier schematic

the devices are not ideal. Power losses in a Class D amplifier parallel that in a synchronous buck converter and consist of device switching and conduction losses, losses associated with the inductor L_1, and other less significant sources.

The voltage at the switching node (where the source of Q_1 meets the drain of Q_2 and the inductor L_1) is a square wave, swinging from negative to positive supply voltage rail. Commonly an LC low-pass filter is used to remove the ultrasonic harmonic content from the PCM and return the signal to it's orginal integrity [9]. It is nearly impossible to remove all the switching artifacts from the signal which is the largest source of noise and distortion for this class of amplifiers. Typical uses of the Class D audio power amplifier include those where the need for efficiency dominates the need for signal fidelity; such as: automotive applications, personal devices (*i.e.* phones, tablets, ...), televisions, and small consumer-grade audio.

2.3 Introduction to Class D Audio Power Amplifiers

The term "Class D" was originally proposed in 1959 by Baxandall [10] with suggested improvements upon the design of a Class C LC-oscillator; however, Leach [9] gives credit to the concept of a Class D amplifier to a valve-based circuit published in a 1930 patent

by Burnice D. Bedford. The circuit described by Baxandall [10] consists of two bipolar transistors with a common RLC load where the current phase angle between devices is 180° and a very small voltage drop exists on the devices during conduction. Overtime, the meaning of "D" in Class D has been obfuscated to the point that some authors will continue discussions as though the "D" is of relation to "Digital;" but, it should be noted that the signifigance of "D" is that it was merely the letter following "C" in the English alphabet [9]. The original Class D output stage by Baxandall [10] is still consistent with the those available in current times.

2.3.1 Modulation Methods

In general, the concept behind all Class D signal modulation methods is similar: an audio input signal is modulated into a pulse stream. The frequency of these pulses and/or their width is correlated to the amplitude of the original signal. The main difference between these modulation methods is the balance of sound quality versus power efficiency.

Pulse Width Modulation

Pulse Width Modulation (PWM), the most common type of modulator in Class D audio, compares an audio signal to a triangle or sawtooth-wave to generate the PCM signal. The sawtooth-wave has a static frequency and is the carrier signal. The duty cycle of the output PCM is dynamic and corresponds to the amplitude of the input audio signal. A duty cycle of $d = 50\,\%$ occurs when the input signal is at the 0 V AC midpoint. The signal must have a smaller amplitude than the carrier sawtooth-wave to avoid "full modulation," in which the duty cycle is $d = 100\,\%$ or $d = 0\,\%$ [2]. See the example waveforms in Figure 2.6 and an example open-loop, single-ended schematic in Figure 2.7.

A major advantage of PWM is a minimum Signal to Noise Ratio (SNR) of 100 dB at carrier frequencies below 300 kHz. This method allows for a low inherent noise floor and switching speeds that minimize switching losses (often the most significant source of power losses in switching circuits). The disadvantages of PWM include: added distortion in the PCM generation, electro-magnetic interference (EMI) from the static switching frequency

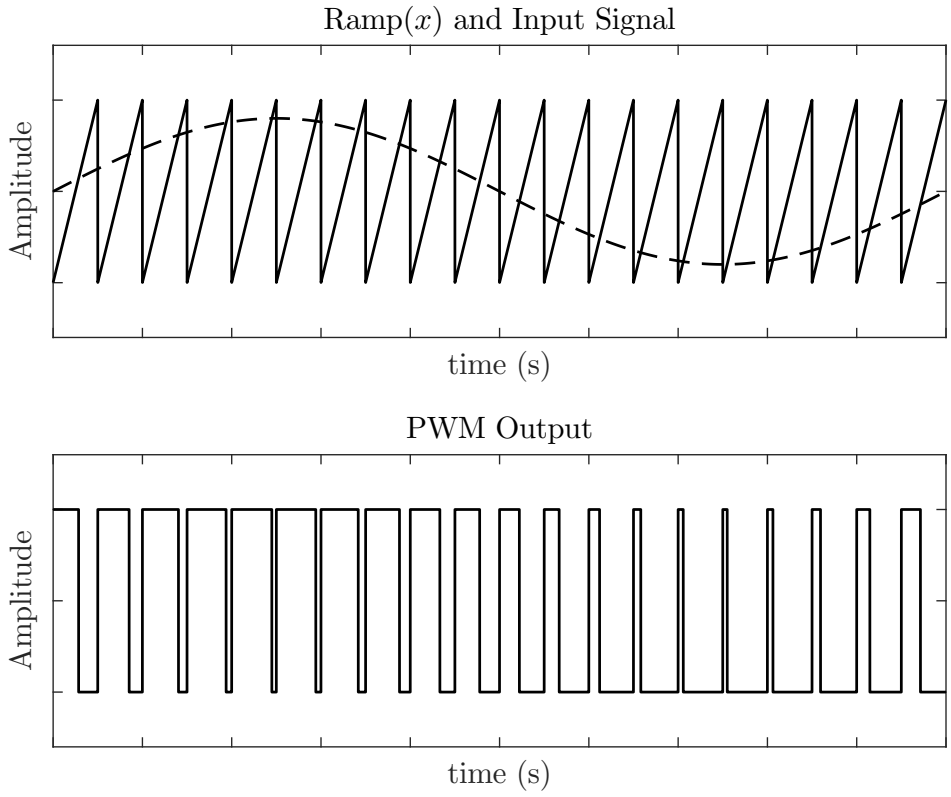


Figure 2.6: PWM sampling waveforms

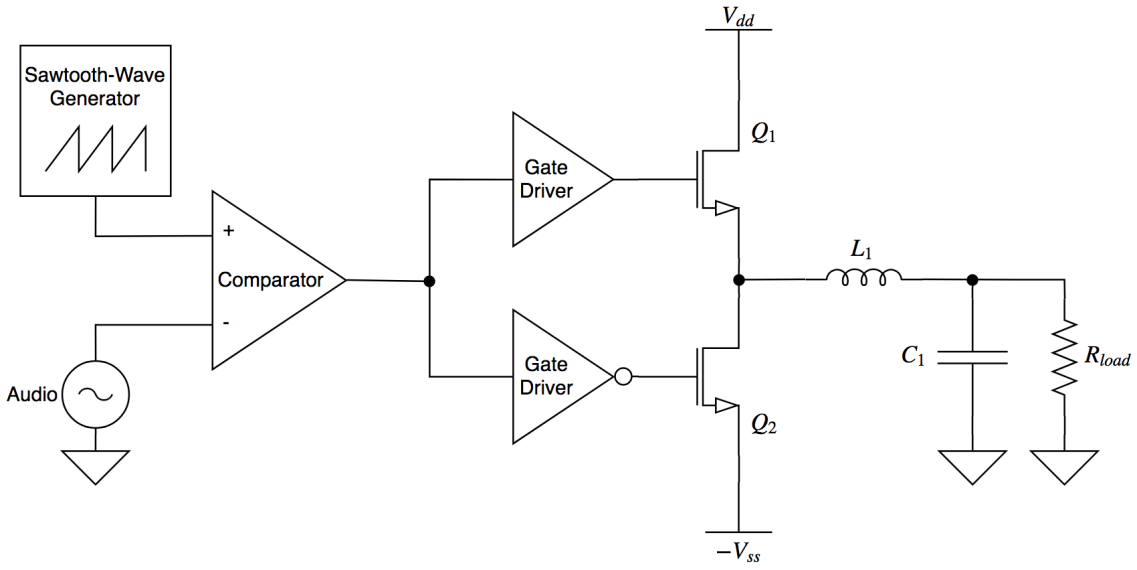


Figure 2.7: Simple PWM based Class D schematic

in the AM-bands used in radio transmission (between 540 kHz to 1600 kHz), and extremely narrow pulses at minimum signal swings. In typical applications, the RLC properties of the output devices prevent the output transistors from turning fully on at $\lim_{d\to 100\,\%}$ or turning fully off at $\lim_{d\to 0\,\%}$, making the circuit incapable of "full modulation." This effect limits deliverable power to the speaker load to some amount less than the theoretical maximum [2].

Pulse Density Modulation

Pulse Density Modulation (PDM) is less popular than PWM and uses a single-bit $\Sigma\Delta$ analog-to-digital converter (ADC) to generate the PCM used to drive the output stage [2, 11].[5] In this topology the switching frequency is dynamic and results in a varied density of pulses proportional to the amplitude of input signal and the frequency tuning of the integrator. An example waveform and schematic are shown in Figures 2.8 and 2.9.

The switching contributions from EMI to noise and distortion are much lower than compared to PWM. There are two main reasons for this: (a.) the ultrasonic energy is spread over a range of frequencies rather than the single switching frequency and (b.) the typical clock frequency of the system is greater than 1 MHz, shifting the noise well above the audio band [2].

Though the sound performance of PDM are often superior to PWM, this comes at a trade-off. In order to achieve this performance, oversampling of a minimum 64× is required [2]. This results in switching speeds of the output devices that can approach the clock frequency of the system ($f_{clk} \gtrapprox 1\,\text{MHz}$). Therefore, having a significant impact on the efficiency (η) of the output stage due to switching losses.

Self-oscillating PWM

Self-oscillating PWM amplifiers, due to their relatively recent emergence within practical applications, are the least common of the three topologies discussed [2]. At the center of every self-oscillating Class D amplifier is a hysteretic controller that can be used to generate a PWM signal. This removes the need for clock or timer ICs for control or carrier signal generation, limiting the necessary components; thus, minimizing the overall circuit footprint.

[5] This modulation method is also known as $\Sigma\Delta$ or $\Delta\Sigma$-modulation.

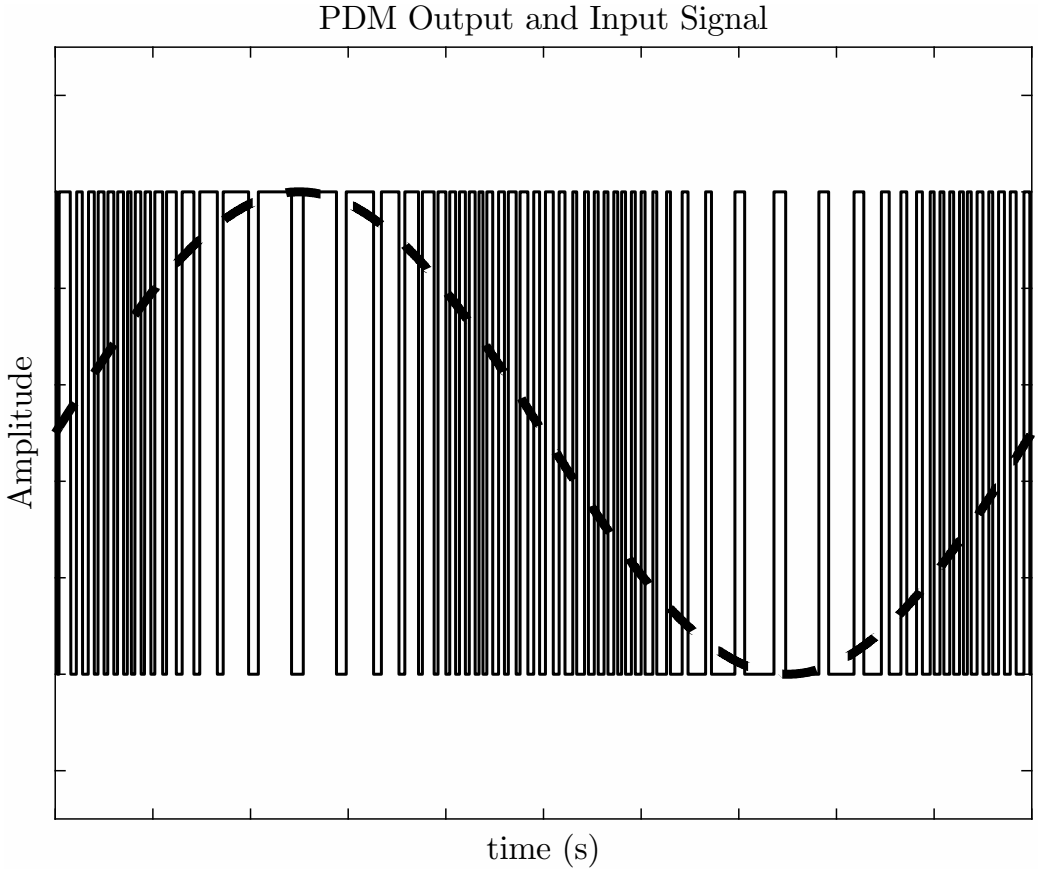


Figure 2.8: PWM sampling waveforms

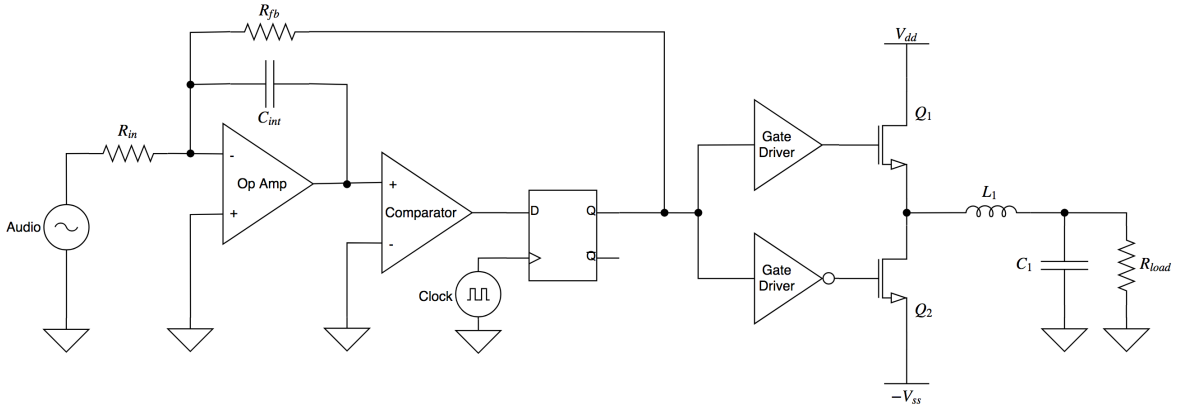


Figure 2.9: $\Sigma\Delta$-modulation based Class D schematic

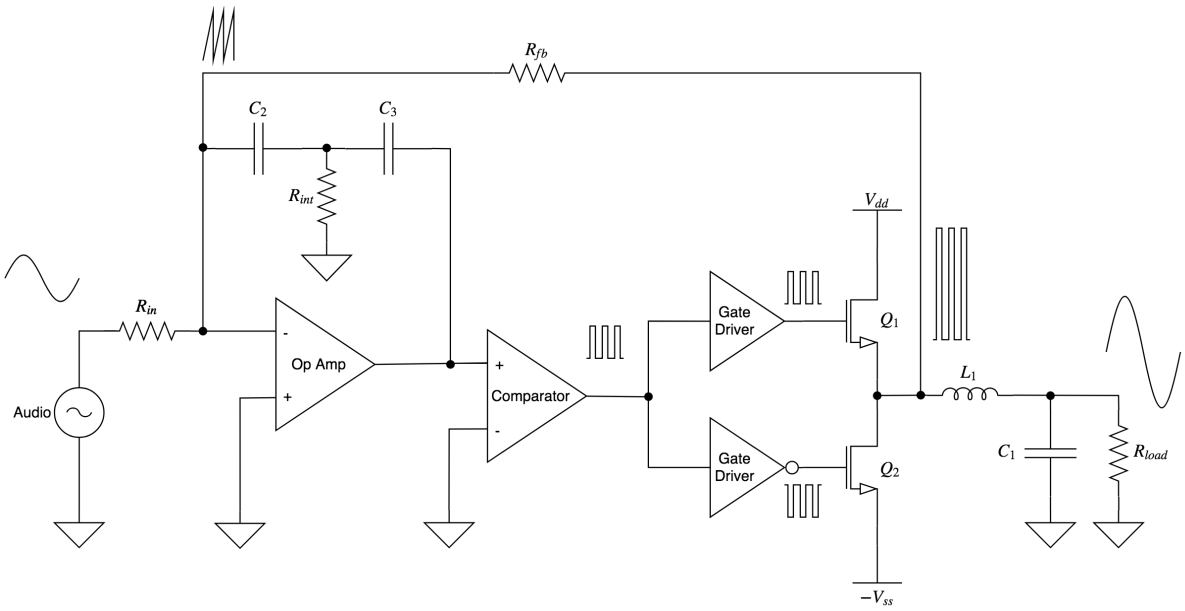


Figure 2.10: Self Oscillating Class D schematic

Additionally, the modulation signal is not discretized in the same sense as in PDM and there is no quantization noise yielding SNR performance on the order of "100 dB or better [12]." An example schematic is shown in Figure 2.10.

2.3.2 Load Configurations

The load configuration of the Class D amplifier can be organized as either single ended (SE) or differential. Additionally, the amplifier system can operate with any number of channels depending on the application; most common are dual channels for stereo operation or single channel for monoblock operation.

Single Ended (SE)

SE operation is has the output stage with the fewest component count. In the example circuits of Section 2.3.1 are all shown with SE output stages, consisting of positive and negative voltage buses, a half-bridge, push-pull switching circuit, and an LC low-pass filter before a resistive load.

In some applications, a SE output stage can operate on a single power supply; however this could lead to a DC bias voltage of $V_{dd}/2$ across the speaker load [2]. A DC blocking

capacitor must be used in this case since any DC bias will lead to power losses in the load and could also damage the speaker. Typically, a SE output stage will use complementary power supplies to avoid using a large DC blocking capacitor. The maximum output swing of a SE output is limited by the formula shown in Equation (2.3).

$$v_{out(max)} = \frac{|V_{dd}| + |V_{ss}|}{2} \tag{2.3}$$

The reason for this is that the opposite terminal of the load is tied to signal ground which should be the middle point between the complementary supplies. A differential load configuration can be used to increase the output voltage swing; however, this configuration increases the component count by a factor of 2.

Differential

Differential configuration consists of a speaker load connected between two half-bridge switching stages as shown in Figure 2.11. Because of this connection, the circuit is often referred to as a Bridge-Tied Load (BTL) in audio applications.[6] In this configuration, a single supply bus can be used just as easily as complementary voltage rails, all without a DC blocking capacitor.

The BTL output stage does consume much more space than the SE option; besides double the component count with respect to output transistors, inductors, and capacitors, the BTL also requires additional support circuitry for control logic and gate driving. However, if there is space to use the BTL connection, there can be many benefits of this configuration. One of these benefits is due to "pumping" currents from the LC-filter which travel through the load to the complementary half-bridge. This effect creates a local current loop minimizing ripple on the voltage buses [2]. The ripple across the load is also significantly reduced due to interleaving of the switching behavior. Also in this configuration, the effective switching frequency is double that of the tuned switching frequency. This means the tuned switching frequency must be reduced to achieve a similar efficiency of SE operation at the effective switching frequency [13].

[6] In other applications, such as motor drives, the BTL configuration is also called an *H-bridge* configuration because the shape of the schematic representation resembles the capital letter "H".

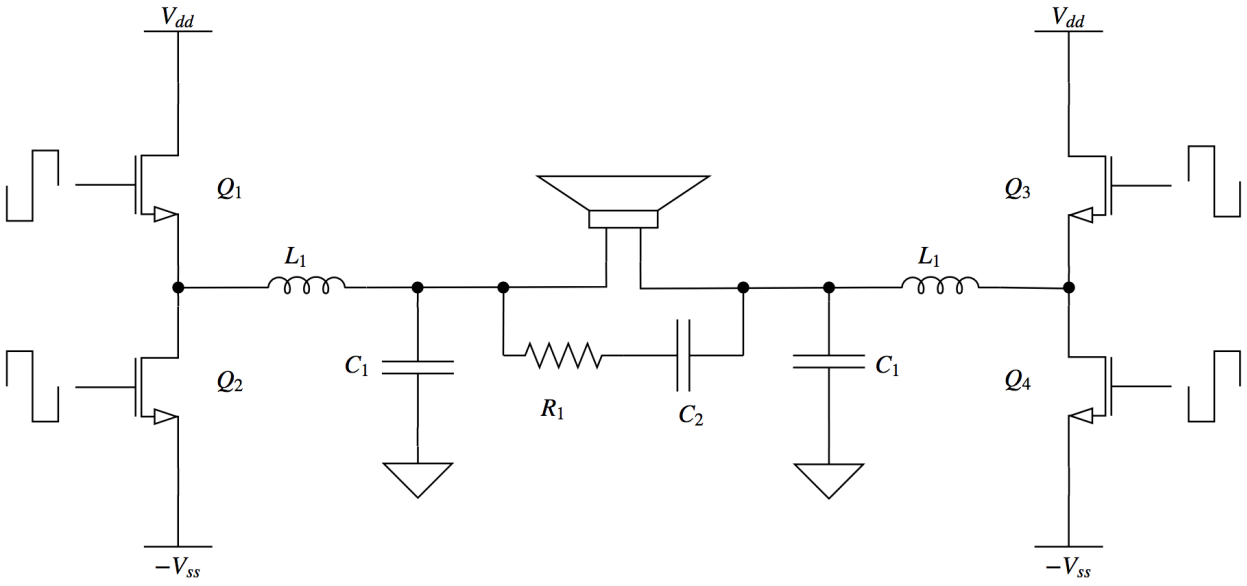


Figure 2.11: BTL configuration

2.4 Audio Amplifier Performance Metrics

The performance of an audio amplifier is an evaluation of design trade-offs. The main trade-off for any audio amplifier is sound quality for efficiency. As described in Section 2.2, an amplifier with better distortion and noise ratios will also be expected to have lower power efficiency. This section will describe the main performance metrics and how they are examined.

2.4.1 Power Measurements

The main power measurements of an audio amplifier consist of power rating and efficiency. These measurements can all be achieved using the example test setup shown in Figure 2.12. Note that in this setup, the load resistance is most commonly $R_{load} = 8\,\Omega$; however, other values can be used for these evaluations, for example: $16\,\Omega$, $4\,\Omega$, or $2\,\Omega$ [9].

Power Rating

Power rating is measured by using a test input and monitoring the output of the amplifier. For the test setup in Figure 2.12, a sine-wave is applied to the input (v_{in}) at a frequency

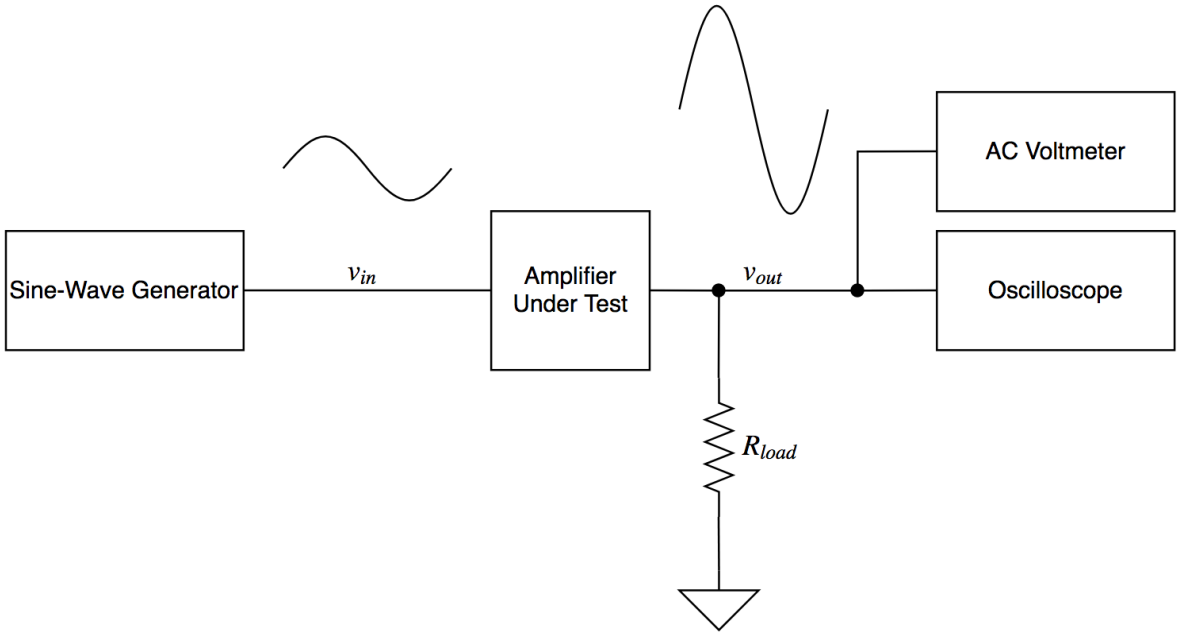


Figure 2.12: Test setup for power and voltage measurements

of $f_{test} = 1\,\text{kHz}$. While monitoring the output (v_{out}) with the oscilloscope, the amplitude of the sine-wave is increased until the output (v_{out}) begins to clip on both the maximum and minimum peaks. The amplitude is then scaled back until the peak clipping is unnoticeable. This is the experimentally maximum peak-to-peak v_{out} deliverable to the load.

For a SE amplifier the max v_{out} can be approximated by Equation (2.3) given previously in Section 2.3.2, and for a BTL amplifier the max v_{out} can be approximated by Equation (2.4).

$$v_{out(max)} = |V_{dd}| + |V_{ss}| \tag{2.4}$$

The output power can then be calculated by Equation (2.5), where the peak voltage from the oscilloscope is $V_{out(peak)}$ and the RMS voltage read from the AC Voltmeter is $V_{out(RMS)}$ [9].

$$P_L = \frac{V_{out(peak)}^2}{2R_{load}} = \frac{V_{out(RMS)}^2}{R_{load}} \tag{2.5}$$

Efficiency

Efficiency (η) measurements are more necessary with evaluations of Class D audio amplifiers than with the other common classes discussed in Section 2.2. This is because Class D amplifiers are specifically designed for high-efficiency applications, where as other classes are designed for sound quality and often have very low efficiency ratings. Using the previous test setup in Figure 2.12, the efficiency evaluation would also monitor the power delivered to the *Amplifier Under Test* from the lab bench power supplies (P_{in}). The efficiency can be determined using Equation (2.6).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out(RMS)}^2}{R_{load}P_{in}} \tag{2.6}$$

For the case of Class D amplifiers, typical experimental efficiency of $\eta = 90\,\%$ or greater at full power can be observed [2]. Major sources of the power losses preventing the circuit from achieving a unity efficiency include: switching losses, conduction losses, inductor losses, as well as losses in peripheral and control circuitry among other sources [2, 5].

2.4.2 Voltage Gain

The voltage gain or amplifier gain can be determined by using the previously described test setup in Figure 2.12 and is defined as the ratio of the output signal voltage (v_{out}) to the input signal voltage (v_{in}). These signals can be monitored either as peak-to-peak or RMS voltages, but consistent units must be maintened between the two signals. The voltage gain ratio is shown by Equation (2.7) [9].

$$A_v = \frac{v_{out}}{v_{in}} \tag{2.7}$$

In most cases, the amplifier's voltage gain is given in units of dBs rather than V/V. The units can be converted by using Equation (2.8) [9].

$$A_{v(\mathrm{dB})} = 20 \cdot \log(A_v) \tag{2.8}$$

An audio amplifier's specified gain is usually given for a 1 kHz sine-wave test input and is typically on the order of 26 dB [9].

2.4.3 Frequency Response

Using the same test setup as in the previous sections (Figure 2.12), the Frequency Response of a system can be characterized. This evaluation will determine the upper and lower cutoff frequencies, f_{high} and f_{low} respectively, of the audio amplifier. These cutoff frequencies can be observed by sweeping the frequency f_{test} of a test sine-wave input until the voltage gain A_v is 3 dB below the mid-band voltage gain A_{mid} [9].

There are two types frequency response evaluations: small-signal and large-signal. The small-signal bandwidth is observed while driving an 8 Ω load with 1 W and large-signal bandwidth is observed while driving a load at full power. The large-signal bandwidth can be narrower than the small-signal bandwidth if the amplifier is slewing [9].

The slew rate of an amplifier is often evaluated if there is indication of slewing during the large-signal bandwidth tests. A 10 kHz square-wave is applied to the input v_{in} of the amplifier and the output v_{out} is observed on an oscilloscope. The slope of the rise and fall transitions observable at the output v_{out} is the slew rate. Typical slew rates are within the range of 5 V/µs to 40 V/µs [9].

2.4.4 Noise Measurements

The signal-to-noise ratio (SNR) is the ratio of the system's maximum RMS output before peaking when driven by a sine-wave ($V_{so(RMS)}$) to the system's total noise with the input terminal grounded ($V_{no(RMS)}$). The SNR is given by Equation (2.9). A typical audio amplifier's SNR is 90 dB and sometimes greater [9].

$$\text{SNR} = 20 \log \left[\frac{V_{so(RMS)}}{V_{no(RMS)}} \right] \tag{2.9}$$

SNR measurements can be conducted with an audio analyzer. Audio analyzers are specialized test equipment designed to provide quantitative information on specific

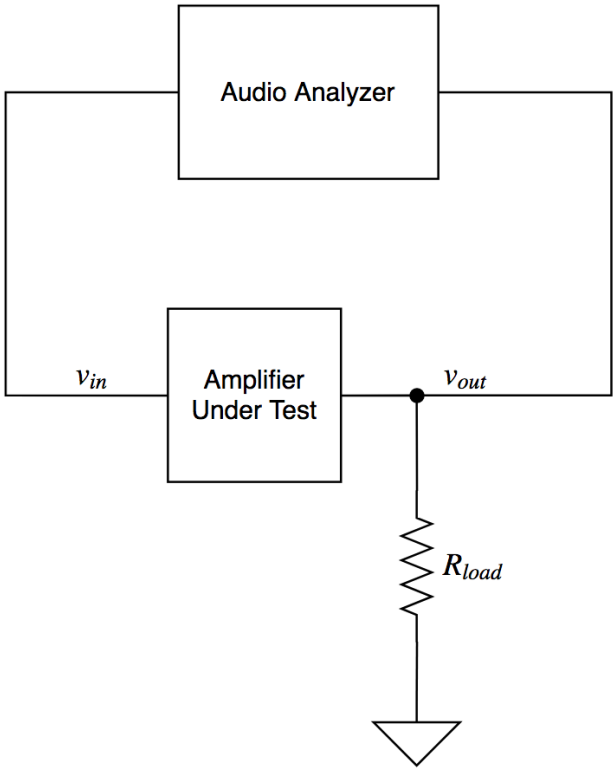


Figure 2.13: Test setup for noise and distortion measurements

performance metrics of an audio electroacoustic system. An example test setup using an audio analyzer is shown in Figure 2.13.

2.4.5 Distortion Measurements

If a sine-wave is applied to the input of an ideal audio amplifier, it is expected that the output should be a coherent sine-wave (inverted or non-inverted) containing identical harmonic content with a designed amount of gain. However, an ideal audio amplifier is not achievable in practice. Any practical audio amplifier will texture the original input signal with some additional harmonic content which will be observable within the output signal. This additional harmonic content is categorized as harmonic distortion.

Harmonic distortion is quantified by the Fourier series of some fundamental frequency of an AC signal plus the n-th order harmonics and their energy levels. The main types of harmonic distortion measurements are Total Harmonic Distortion (THD) and Total Harmonic Distortion plus Noise (THD+N). Using the test setup in Figure 2.13, the audio

analyzer can help determine either of these distortion metrics. For any case when measuring distortion, the sine-wave generator must be able to produce a near sterile sine-wave, free from distortion and noise. It is often possible with less than high-quality signal generators that the generated sine-wave contains more distortion additives than the amplifier under test [9].

The ideal RMS voltage of the amplifier's output with a sine-wave test input $V_{in(RMS)}$ with some applied gain A_v is given as $V_{so(RMS)} = A_v V_{in(RMS)}$. In the non-ideal case, the output signal also contains the RMS voltage with some degree of added distortion $V_{do(RMS)}$. So, the non-ideal output is then the sum of the ideal case and the distortion, $V_{RMS} = V_{so(RMS)} + V_{do(RMS)}$. These values are used to calculate the THD of the amplifier shown in Equation (2.10) [9]. This equation shows that THD is often shown as a percentage of the ratio of the RMS voltage due to distortion over the total RMS voltage of the amplifier's output.

$$\text{THD} = \frac{V_{do(RMS)}}{V_{so(RMS)} + V_{do(RMS)}} \times 100\,\% \tag{2.10}$$

Where THD only accounts for distortion related to the Fourier series, THD+N includes both the RMS voltage of the harmonic distortion and the RMS voltage for all noise. Because of this, THD+N is always a higher percentage than THD measurements for the same test signal. THD+N is also the inverse of the SNR when given in units of V/V. Since SNR is typically given in units of dB, the THD+N can often be determined from Equation (2.11).

$$\text{THD+N} = \left[10^{\frac{\text{SNR}_{\text{dB}}}{20}}\right]^{-1} \times 100\,\% \tag{2.11}$$

Another type of distortion often used to determine the performance of an audio amplifier in classes other than Class D is intermodulation distortion (IMD). The reason that this metric is not shown for Class D amplifiers is the characteristically poor performance of this class of amplifier with respect to this measurement. IMD is determined by summing two sine-waves at the input and observing the harmonic content of the output of the amplifier. In an ideal case, the output will only contain the sum of the original input sine-waves. In the non-ideal cases, the output will contain components of sine-waves besides those applied to

the input. These components will be related to $nf_1 \pm mf_2$ where f_1 and f_2 are the frequencies of the two applied sine-waves and n and m are positive integers [9].

2.5 GaN in Class D Audio Applications

The main design trade-off for Class D audio amplifiers is: cost *versus* size *versus* sound quality [7]. The main sources for diminished sound quality as distortion are dead-time and phase shift by the output filter. Because the output FETs do not turn on and off instantaneously, the control circuit implements a dead-time technique that ensures that one transistor is fully off before the opposing one turns on by inserting a delay or advancement between control signals rising and falling edges. This prevents shoot-through current which is described as a short duration of a low DC impedance path between the positive and negative (or ground) supply voltage rails as both output devices are operating in the ohmic region. Shoot-through current is directly related to power losses in the devices.

The phase shift by the output filter is due to the size of the circuit elements, both physical and by value. With lower switching speeds, large capacitors and/or inductors must be used to attenuate the switching artifacts. These larger passives not only add to the cost and size of the circuit, but create a more dramatic phase shift. A larger phase shift will limit the loop gain of the feedback network and decrease the region of stable operation. The feedback network is used to compensate for any signal errors generated within the system; thus, a lower feedback loop gain will limit the effects of compensation and restrict the system fidelity [7].

The two main areas of improvement for Class D amplifiers are miniaturization in size and higher power efficiency. The focus on these areas has led to recent advancements including filter-less output stages and purely digital input systems. The filter-less Class D demonstrated that there is no need for a LC-filter on the output stage since the human ear and speaker will act as low-pass filters [9]. The digital input Class D allows the amplifier to directly interface with a digital audio source without the need for a digital-to-analog converter (DAC) [14]. Examples of these advancements can be found available for purchase commercially as integrated circuits (ICs) or complete systems.

A currently emerging approach to address improvements to circuit size and efficiency is the use of WBG power devices in the output stage. The balance of trade-offs in Class D audio has also been limited by the performance capabilities of the output FETs. Output FETs capable of switching at much higher speeds would allow for smaller passive circuit elements in the output filter and lower the dead-time needed in order to prevent shoot-through current. In order to improve the FET, the gate charge must be reduced and the carrier velocity must be increased; which is not a possibility with the current state-of-the-art Silicon devices. This is why, we must explore the option of using newly developed WBG technology to replace Silicon FETs.

Recent improvements in processing (further reviewed in Appendix A) have allowed for a multitude of WBG devices suitable for many different applications to be commercially available to circuit designers. The immediate availability coupled with the inherent performance improvements to traditional Silicon devices is motivating designers to find many opportunities to enhance traditional discrete circuit designs with WBG technology.

2.5.1 A 25 W PDM Class D Audio Amplifier

A 2016 publication compared Si and GaN output stages for a single ended, open loop, Class D amplifier with an FPGA-based (field-programmable gate array) PDM and BTL [11]. The devices selected were the GaN Systems HEMT and a Texas Instruments NexFET™ device. The characteristics of the devices in this study are given in Table 2.1.

The Altera FPGA would sample audio signal at 48 kHz and up-sample to 12.5 MHz before passing the sampled data to a second order PDM. The FPGA also controlled the dead-time and any delay. The controller also had an option of sending gate signals with a switching frequency of either $f_{sw} = 1.1\,\text{MHz}$ or $f_{sw} = 360\,\text{kHz}$.

Table 2.1: Comparison of selected output devices published by Chung et al. [11]

Manufacturer	Part Number	Material	$V_{DS(max)}$ [V]	I_D [A]	$R_{DS(ON)}$ [mΩ]	Q_G [nC]	RQ Product [mΩ·nC]
GaN Systems	GS61004B	GaN	100	30	15.0	6.6	99.0
Texas Instruments	CSD19537Q3	Si	100	50	12.1	16.0	193.6

Table 2.2: Approximate experimental results published by Chung et al. [11]

Manufacturer	Part Number	Material	f_{sw}	THD+N [%]
GaN Systems	GS61004B	GaN	1.1 MHz	0.5
GaN Systems	GS61004B	GaN	360 kHz	0.2
Texas Instruments	CSD19537Q3	Si	1.1 MHz	1.1
Texas Instruments	CSD19537Q3	Si	360 kHz	0.9

Table 2.2 shows the THD+N results that could be approximated from the article's figures shown in Figures 2.14 and 2.15. The tabulated results are for the two separate switching frequencies with a 1 kHz test signal and at a power output of 10 W (which is $0.4 \times P_{out(max)}$ where $P_{out(max)} = 25\,\text{W}$) and $f_{test} = 1\,\text{kHz}$.

This paper does provide some helpful information while comparing Si to GaN; however, it is never fully explained why the THD+N increases with switching frequency. According to all simple mathematical models, the further the switching frequency is away from the corner frequency of the output filter, the lower the THD+N should be. One explanation to consider is that at some switching frequency and output amplitude, the distortion due to dead-time (t_{dt}) becomes greater than the contributions of switching noise. Regardless, this phenomena is not clearly identified in the publication.

2.5.2 A 150 W Self-Oscillating PWM Class D Amplifier

A 2015 publication by Duraij et al. [15] demonstrates the experimental results of a GaN-based self-oscillating Class D amplifier. This amplifier was capable of delivering 150 W to a 4 Ω load. The paper does not divulge many details on the circuit topology or other performance metrics. Duraij et al. [15] claims the lowest THD measured was at 7 W with THD = 0.0034 %. Additional details from the publication include the challenges to design and layout an experimental PCB with higher switching frequencies and the potential need for higher order loop filters to further decrease distortion due to EMI.

2.5.3 Summary of Literature Reviewed

A large challenge with comparison of audio amplifiers is the lack of standards for performance metrics. To evaluate the THD, one could use a test sinusoid at the input of the amplifier of

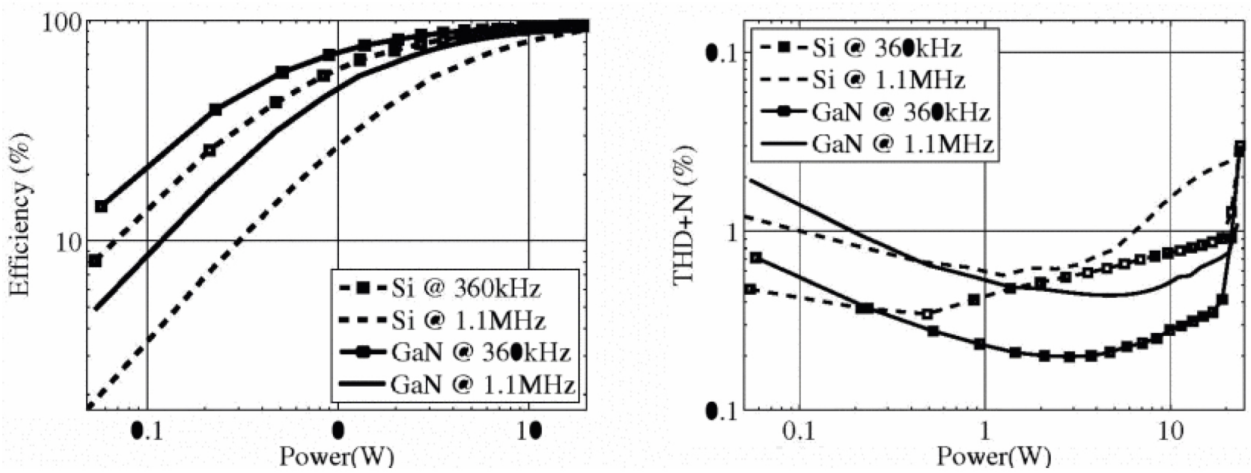


Figure 2.14: Efficiency and THD+N versus power published by Chung et al. [11]

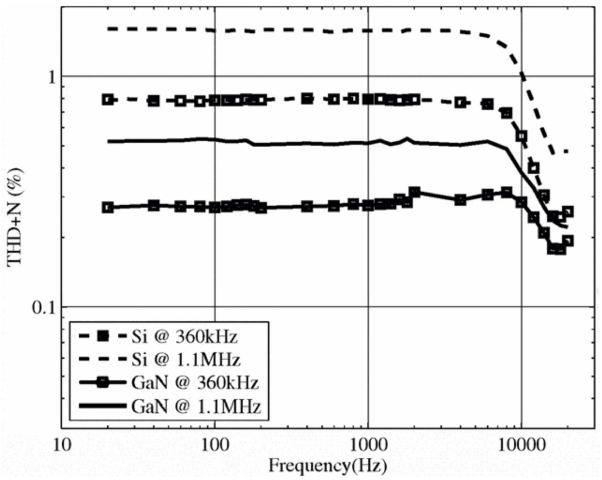


Figure 2.15: THD+N versus input frequency published by Chung et al. [11]

Table 2.3: Summary of reviewed circuits

Author	Material	Efficiency [%]	THD [%]
Duraij et al. [15]	GaN	98.0	0.008
Chung et al. [11]	GaN	82.2	0.800
Chung et al. [11]	Si	67.0	0.500

any frequency and any fraction of max output power. The THD could also be demonstrated by ratio of the voltage sum of many harmonics or only one harmonic to the fundamental test frequency described in the text by Leach [9]; and in other applications THD can be defined as a ratio of current harmonics rather than as voltage as in the text by Mohan et al. [6].

Due to this perceived inconsistency, the metrics used to compare the literature reviewed in this text will be the best claimed or interpreted THD performance levels consistent with typical operating levels. Typical operating levels is defined as an output power in the range of $1/5\ P_{max}$ to $3/5\ P_{max}$. This definition assumes the dynamic range of the music with respect to volume and that a listener will not operate the amplifier at full power. Furthermore, if possible, the THD will be determined by the voltage ratio of the third harmonic to the fundamental frequency. The efficiency of the reviewed amplifiers will simply be determined by the greatest value shown within figures or the text of the reviewed literature. The audio amplifiers reviewed offer a very wide range of performance with respect to these metrics and are summarized in Table 2.3.

Chapter 3

Class D Amplifier Design

An experimental Class D audio amplifier was designed for the side-by-side comparison of GaN and Si output devices. This section outlines the third and final completed design. Other designs explored but not included in this section were are a closed-loop PWM design detailed in Appendix C and a FPGA-based design detailed in Appendix D.

3.1 Device Selection

Limited by the max voltage capabilities of the initially available test equipment, the selection of devices was focused on those with V_{DS} ratings of 60 V. The 60 V category provided many options for Silicon devices and included a GaN device recommended specifically by EPC for Class D audio applications, the EPC2031 eGaN®-FET. The Texas Instruments NexFET™ CSD18534KCS was selected for the designed ultra-low Q_G, which for this device was lower than that of the selected EPC device. The Infineon OptiMOS™-3 IPA093N06N3 G was also chosen for this comparison since it was the least expensive device available through Digi-Key® with comparable I_D and V_{DS} ratings to the selected EPC device. The selected devices are summarized in Table 3.1.

Shown in Figure 3.1 are the RQ products for the selected devices. The contrast between RQ products is considerably less than that noted in article by Lidow [7] and shown in Section 2.1.2. Though the gap between the devices is less than previous examples, note that the gap still exists.

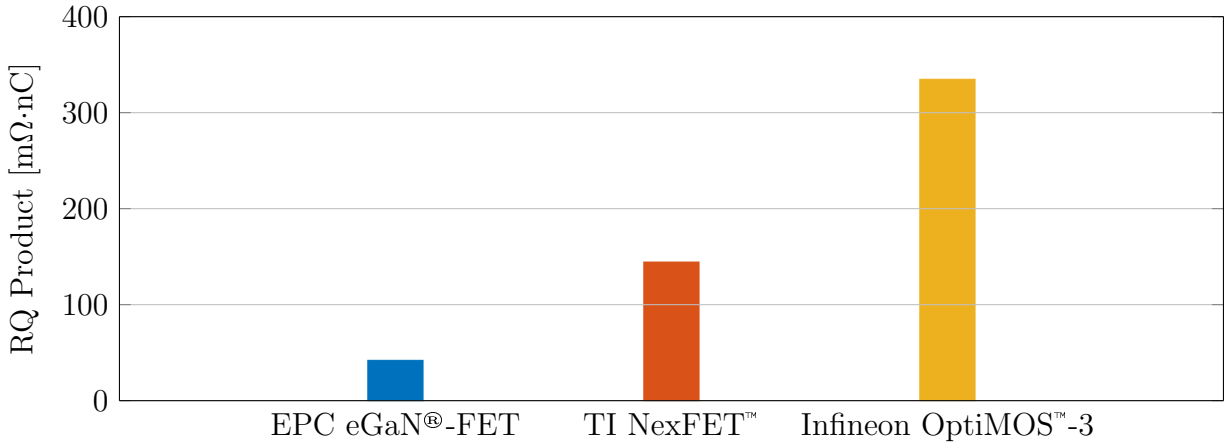


Figure 3.1: RQ Products for selected output devices

3.2 FET Daughter Cards

The most critical design condition was the ability to have a side-by-side comparison of GaN and Si. The challenge in this feat was that a Si gate driver could not be used with a GaN device due to the difference in gate-source voltage threshold (V_{TH}) and absolute maximum gate-source voltage ($V_{GS(max)}$) ratings. The first conclusion was to design separate circuits as in the reviewed circuit by Chung et al. [11]. However, variations between circuit elements and routing geometry could introduce some inconsistencies in measurements and ultimately skew the comparison.

The approach taken in this study is create modular daughter cards. A separate, interchangeable card could be made for each pair of devices and their respective packaging. This approach would limit the variations between circuits to a handful of components and most consistent PCB routing geometry.

The general circuit for the daughter cards is shown in Figure 3.2. A gate driver IC with both high-side and low-side driving capabilities necessary for driving a half-bridge would be

Table 3.1: Comparison of selected output devices

Manufacturer	Part Number	Material	V_{DS} [V]	I_D [A]	$R_{DS(ON)}$ [mΩ]	Q_G [nC]	Cost [USD]
EPC	EPC2031	GaN	60	48	2.0	21	$7.46
Texas Instruments	CSD18534KCS	Si	60	73	7.6	19	$1.58
Infineon	IPA093N06N3	Si	60	43	9.3	36	$1.28

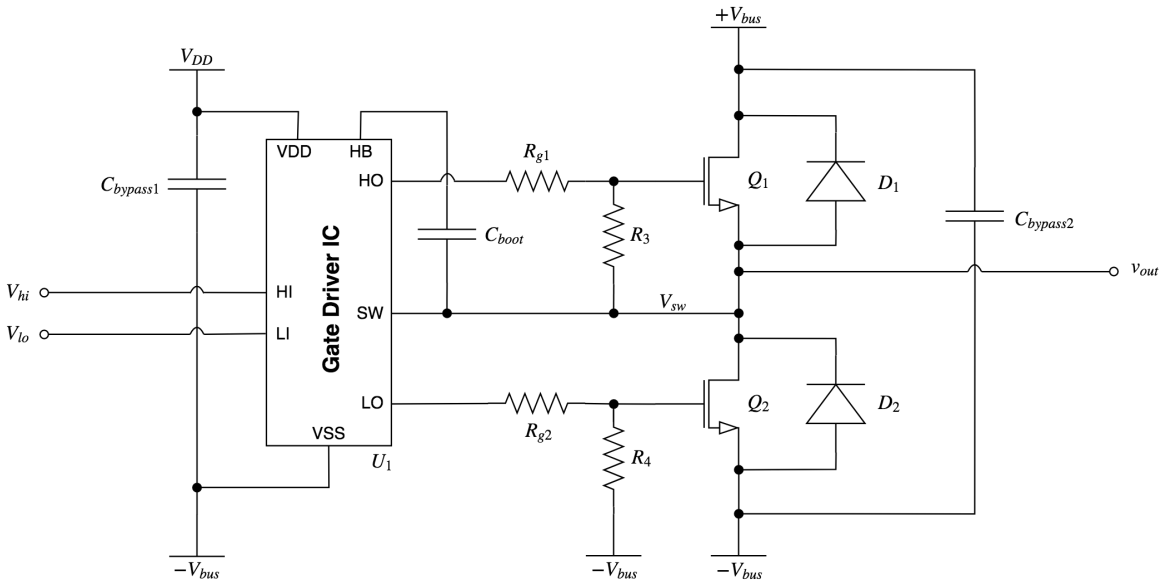
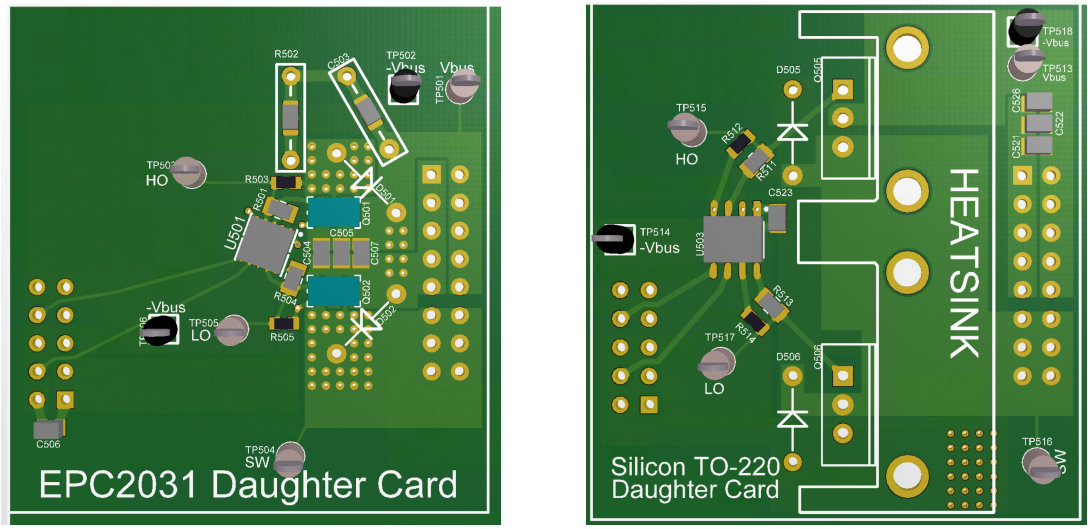


Figure 3.2: Daughter card schematic diagram

the center of the circuit. This would be either the Texas Instruments UCC27211 for the Si devices or Texas Instruments LM5113 for GaN. The gate driver would behave as a level shift and/or add conditioning to the control signals coming from the main board (V_{hi} or V_{li}) to the appropriate V_{GS} required by the devices and also with the current necessary to quickly charge or drain the device's gate to minimize switching losses.

The unique daughter card for each device package allowed for special consideration of PCB routing in order to avoid or at least limit the non-ideal effects of power loops. As can be seen in Figure 3.3, the orientation and placement of components is seemingly unorthodox. This is so that the high $\frac{di}{dt}$ signals have path lengths as short as possible. This limits the effects of cross-talk and EMI generated from the reactive forces (V) of parasitic loop inductances (L_{par}) and the fast change in currents seen in Equation (3.1). The Altium® schematic of the daughter cards can be found in Figure C.11 Appendix C.

$$V = L_{par}\frac{di}{dt} \tag{3.1}$$



(a) EPC daughter card **(b)** TO-220 Si daughter card

Figure 3.3: FET daughter cards

3.3 Controller

The International Rectifier IRS2092 was selected as the central controller for the experimental circuit design. Using a controller allowed the design to focus on the comparison of output FETs rather than a full design and evaluation of an audio amplifier. The IRS2092 is a unique IC that did not include co-packaged or co-die output FETs which is typical of the vast majority of Class D ASICs. The features of the IRS2092 include: self-oscillating PWM, dead-time control, floating input and high-side gate drive, under-voltage lockout, and over-current protection. A functional diagram of the Infineon IRS2092 controller can be seen in Figure 3.4.

The design iterations were highly simplified due to a dictated approach in the International Rectifier application note by Honda et al. [16]. The most unique feature outlined in the note by Honda et al. [16] was the ability to synchronize the self-oscillating frequency to an external clock. This provides greater control over the typically static switching frequency of the system, minimizes errors due to delay between the sampled and summed nodes of the feedback loop, and would allow for more precise frequency data points during evaluation.

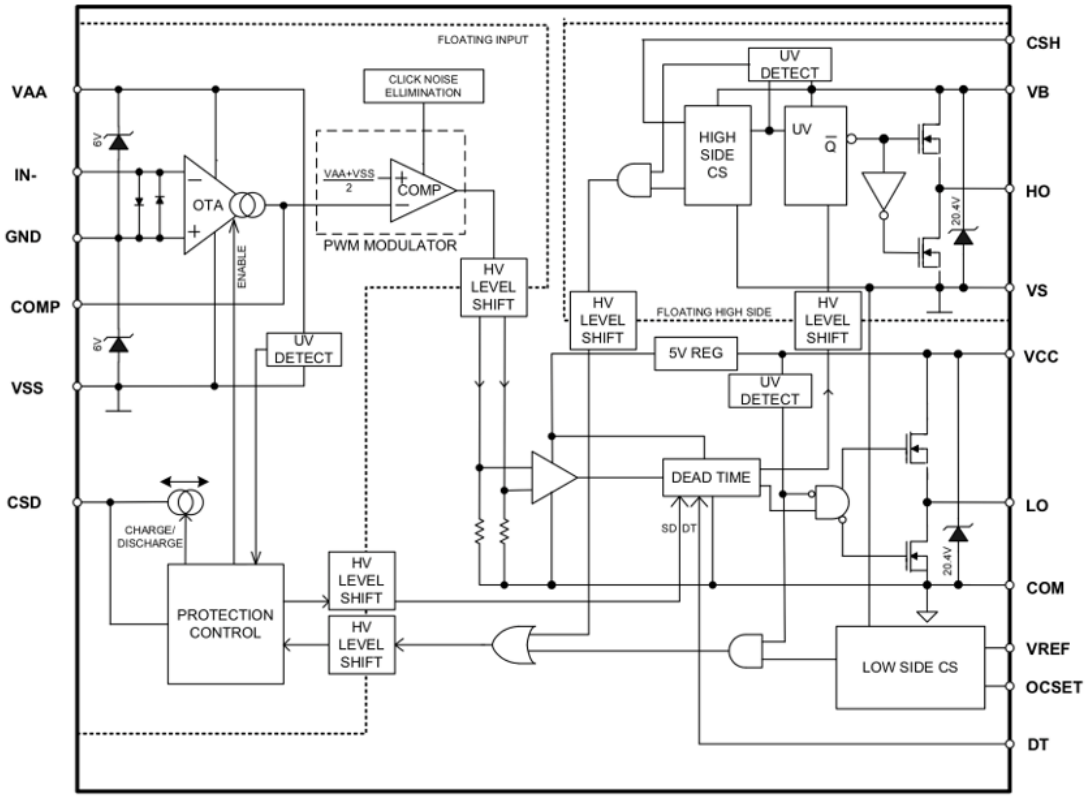


Figure 3.4: Infineon IRS2092 functional diagram [16]

3.4 Frequency Response

The signal bandwidth of an audio amplifier is often consistent with the audio band from 20 Hz to 20 kHz, which is the range of frequencies observable by a normal human ear. The frequency response of the designed system would also follow this format, but designing some margin of error to allow room for some unaccounted RLC properties in the experimental circuit. A block diagram of the IRS2092 with the RLC discrete components and control loop is shown in Figure 3.5.

3.4.1 Low Frequency Pole

The low cutoff frequency of the amplifier's bandwidth (defined by Equation (3.2)) was designed to be $f_{low} \leq 10\,\text{Hz}$. Using Figure 3.5, the low cutoff frequency could be calculated from C_3 and R_{IN}. Because the feedback control was dictated by the IRS2092 application

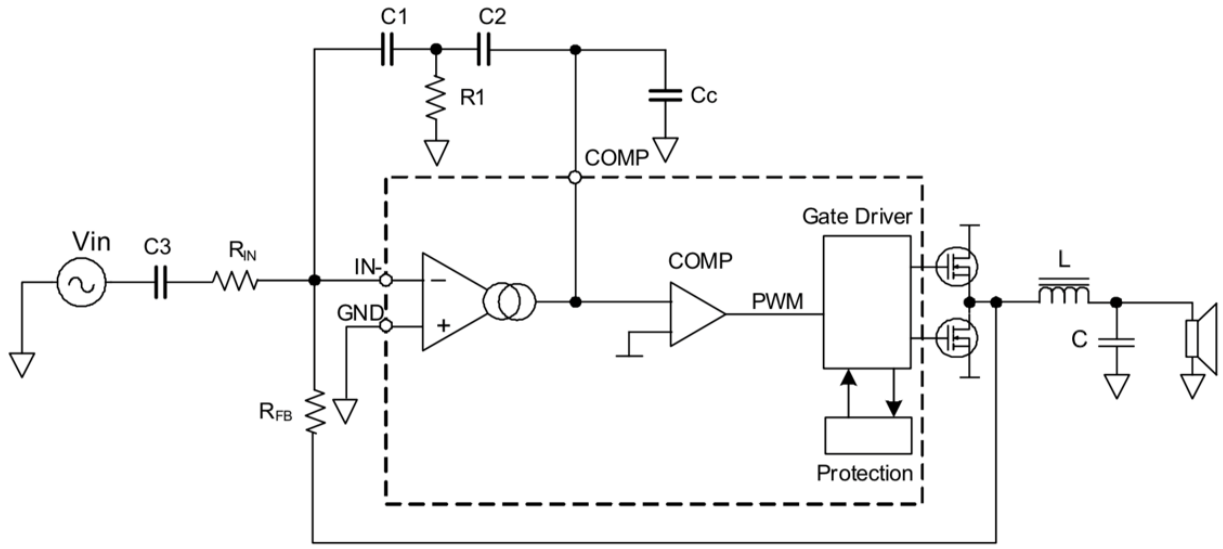


Figure 3.5: Infineon IRS2092 control loop design [16]

notes, R_{IN} was defined to be 1 kΩ [16].

$$f_{low} = \frac{1}{2\pi R_{IN} C_3} \tag{3.2}$$

By solving Equation (3.2) for C_3 and using known values, the minimum value for C_3 could be determined:

$$\begin{aligned} C_3 &= \frac{1}{2\pi R_{IN} f_{low}} \\ &= \frac{1}{2\pi(1\,\text{k}\Omega)(10\,\text{kHz})} = 10\,\mu\text{F} \end{aligned} \tag{3.3}$$

3.4.2 High Frequency Pole

The pole oriented around the output LC-filter of Figure 3.5 determines the high cutoff frequency (f_{high}) of the system. To allow some design margin, the frequency associated with this pole would be tuned to $\geq 25\,\text{kHz}$. The pole can be defined by the interaction of the inductor L and capacitor C in Equation (3.4), where f_{high} is the critical frequency in Hz,

ω_{high} is the critical frequency in rad·s^{-1} and $\omega_{high} = 2\pi f_{high}$ [17].

$$f_{high} = \frac{\omega_{high}}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{3.4}$$

The quality factor (Q) is related to the values of R_{load}, C, and L. This relationship is shown by Equation (3.5). The quality factor of a Class D audio amplifier is typically defined as $Q = 1/\sqrt{2}$ [9, 17].

$$Q = R_{load}\sqrt{\frac{C}{L}} \tag{3.5}$$

Furthermore, the damping ratio (ζ) can also be described by the relationships between Q, R_{load}, C, and L. This is shown in Equation (3.6) [9].

$$\zeta = \frac{1}{2Q} = \frac{1}{2R_{load}\sqrt{\frac{C}{L}}} \tag{3.6}$$

Equation (3.5) can be solved for both L and C, this is shown in Equations (3.7) and (3.8).

$$L = \frac{R_{load}\sqrt{2}}{\omega_{high}} \tag{3.7}$$

$$C = \frac{1}{\omega_{high}R_{load}\sqrt{2}} \tag{3.8}$$

If $f_{high} \geq 25\,\text{kHz}$ and the load is defined as $R_{load} = 8\,\Omega$, the values of L and C could be calculated.

$$L = \frac{R_{load}\sqrt{2}}{\omega_{high}} = \frac{(8\,\Omega)\sqrt{2}}{2\pi(30\,\text{kHz})} \approx 60\,\mu\text{H} \tag{3.9}$$

$$C = \frac{1}{\omega_{high}R_{load}\sqrt{2}} = \frac{1}{2\pi(30\,\text{kHz})(8\,\Omega)\sqrt{2}} \approx 470\,\text{nF} \tag{3.10}$$

Furthermore, the transfer function of the LC-filter along with the load resistance R_{load} can be modeled by the transfer function in Equation (3.11) [17].

$$H(s) = \frac{\frac{1}{LC}}{s^2 + \frac{s}{(R_{load})C} + \frac{1}{LC}} \tag{3.11}$$

3.4.3 Integrator Pole

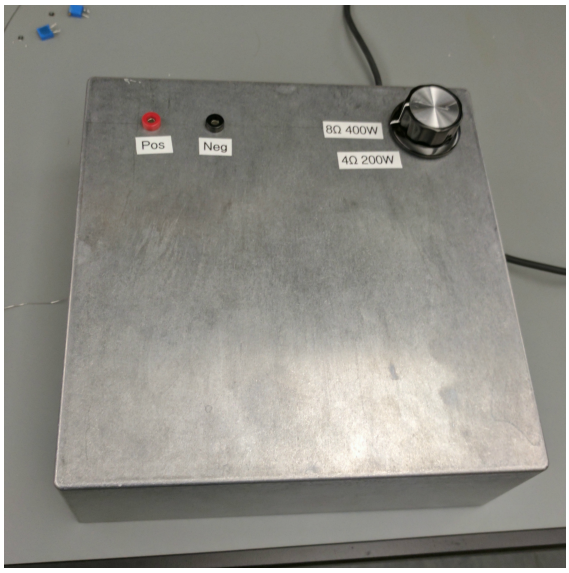
The pole determined by the integrator feedforward path determines the switching frequency of the audio amplifier. The values for C_1, C_2, and R_1 were dictated by the IRS2092 application notes and summarized in Table 3.2. The value for the compensation capacitor C_c was also given in the application notes to be a minimum of 1 nF for stable operation [16].

3.5 Experimental Load Construction

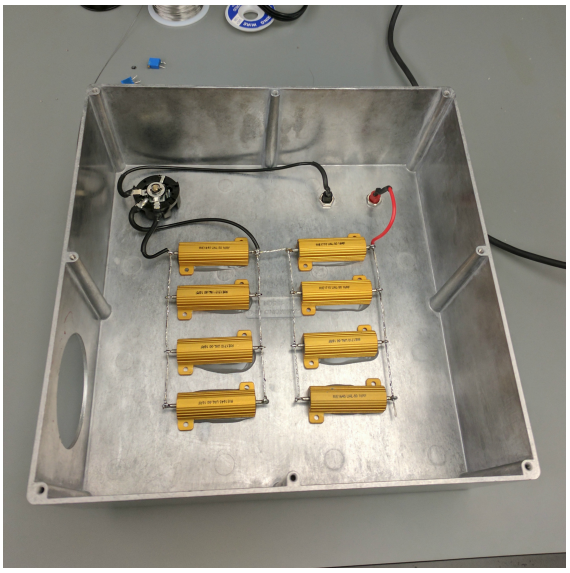
When experimentally evaluating audio amplifiers, actual speakers are rarely used [9]. Instead large power resistors are often used. There are advantages and disadvantages to this approach. The main advantage is avoiding noise pollution in the lab space. A related advantage is that often noise pressure at high power output can be dangerous to those individuals in close proximity of the amplifier under test. The main disadvantage of this approach is that a power resistor does not accurately model the LC properties inherent to a

Table 3.2: Integrator passives for target switching frequency [16]

f_{sw} [kHz]	$C_1 = C_2$ [nF]	R_1 [Ω]
500	2.2	200
450	2.2	165
400	2.2	141
350	2.2	124
300	2.2	115
250	2.2	102
200	4.7	41.2
150	10	20.0



(a) Project box exterior with load switch



(b) Project box interior and wiring

Figure 3.6: Experimental load construction

speaker and driver. However, using large power resistors as a load in this study still facilitates the SI *versus* GaN comparison.

An experimental load was created using an array of $8 \times 16\,\Omega$ power resistors rated at 25 W each. The resistors were fixed to the top of a large aluminum project box with 3M™ TC-2707 thermally conductive epoxy adhesive. The resistors were then electrically connected with a 2 position switch allowing for a toggle between $8\,\Omega$ and 400 W to $4\,\Omega$ and 200 W. A large hole was drilled on the side of the project box for a chassis mount fan, but was deemed unnecessary in application. The interior and exterior of the experimental load is shown in Figure 3.6.

3.6 Final Design Considerations

Since the efficiency benefits of GaN over Si have been well cataloged, any fine tuning to the circuit will have priority to minimize any contributors to distortion and noise rather than enhance power efficiency. The sound quality is most negatively impacted by dead-time, inductor saturation, and the switching transients [7, 18].

3.6.1 Dead-time

The dead-time should be only long enough to prevent shoot-through current since THD $\propto {}^{t_{dt}}/_{T_{sw}}$, where t_{dt} is total dead-time in a switching period and T_{sw} is the duration of a switching period. The dead-time (delay or advance in gate drive signal), is typically tuned so that each upper and lower device are fully off before the opposite device begins to turn on. This adds distortion to the audio signal in a somewhat similar method to crossover distortion discussed for Class B amplifiers.

3.6.2 Inductor Saturation

The inductor should have a very large saturation current to limit the contributions to distortion. The threshold for an inductor's current saturation is due to non-linearities in the voltage-current characteristics intrinsic to the component; therefore, at any current load there exists some non-linear degree of current saturation through the inductor which increases as the current load approaches the current saturation threshold. This effect also leads to non-linear contributions to the total THD of the system. Because of this, the THD component due to inductor current saturation can be approximated by Equation (3.12) where L_0 is the inductance at zero DC current, V_o is the amplitude of the output signal, f_{in} is the input signal frequency, R is the DC impedance of the speaker, and I_{sat} is the saturation current of the inductor [18].

$$\begin{aligned} \text{THD} &= \frac{V_{third\ harmonic}}{V_{fundamental}} \times 100\,\% \\ &= \frac{3 \cdot L_0 V_o^2 \cdot 0.1 \cdot 2\pi f_{in}}{4 \cdot R^3 I_{sat}^2} \times 100\,\% \end{aligned} \tag{3.12}$$

3.6.3 Gate Resistor

The gate resistor should also be large enough to prevent any significant voltage and current oscillations when the devices are turned on and off. These oscillations are due to high $\frac{di}{dt}$ and $\frac{dv}{dt}$ transitions which can cause EMI within the circuit. A higher gate resistance will slow the turn on and off transitions and limit the EMI. The gate resistances were initially chosen to

be 10 Ω, then these values were experimentally optimized to achieve similar turn on and off transition times between devices (this is further discussed in Section 4.1.1).

3.7 Design Summary

The final test board PCB and highlighted sections are summarized in Figure 3.7. The Altium® schematics, PCB assembly drawings, and additional 3-D rendering of the experimental test board can be seen in Figures 3.8 to 3.11.

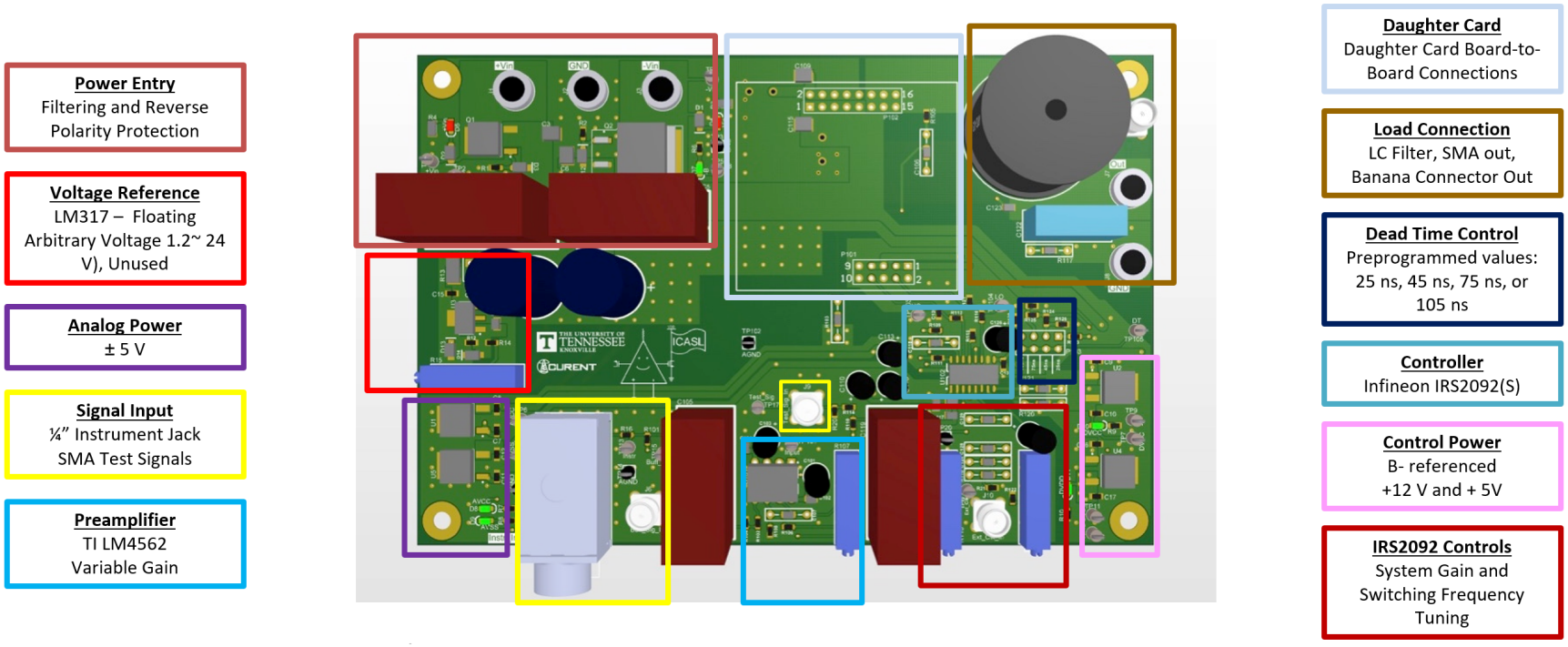


Figure 3.7: 3-D render of experimental test board with highlighted sections

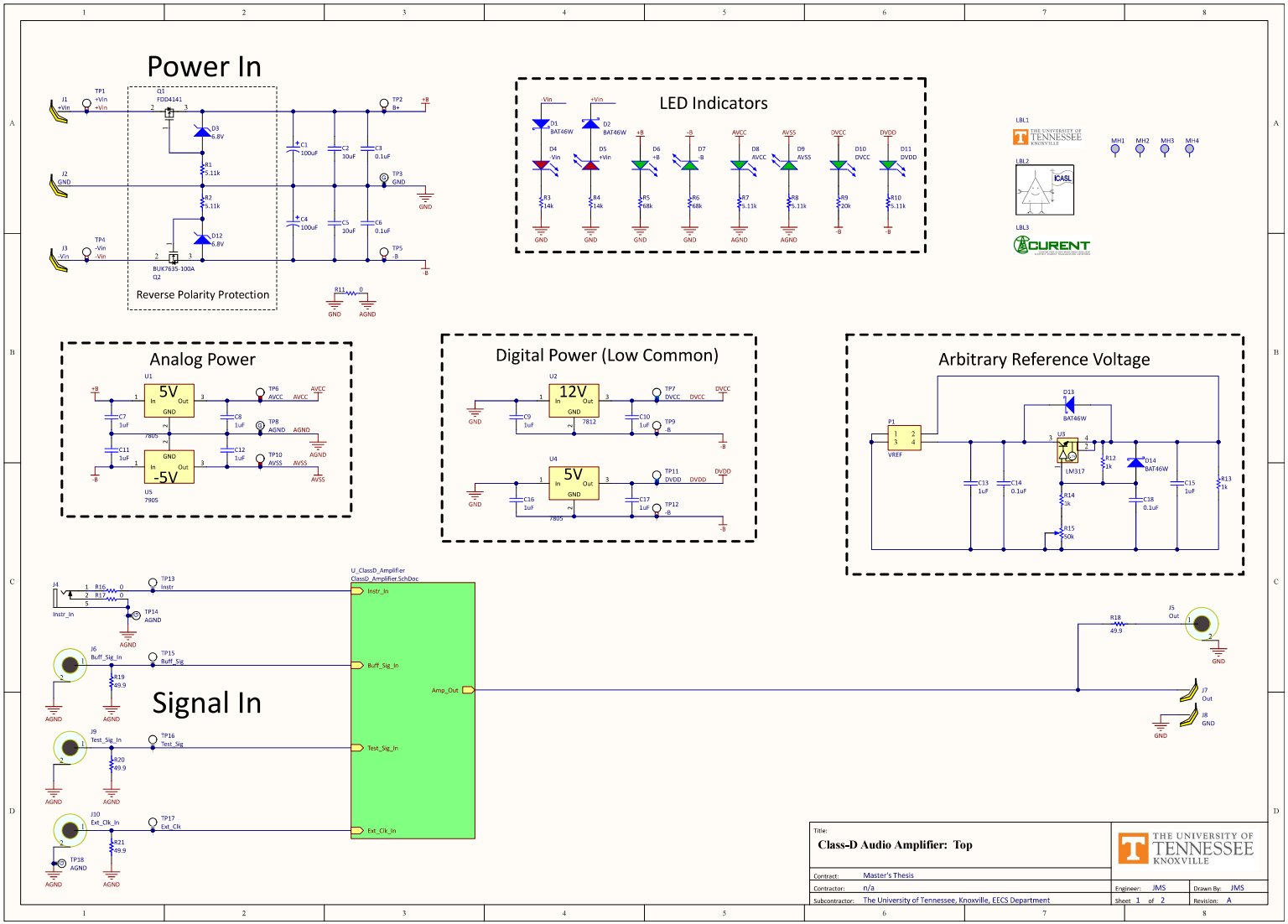


Figure 3.8: Test board schematic page 1

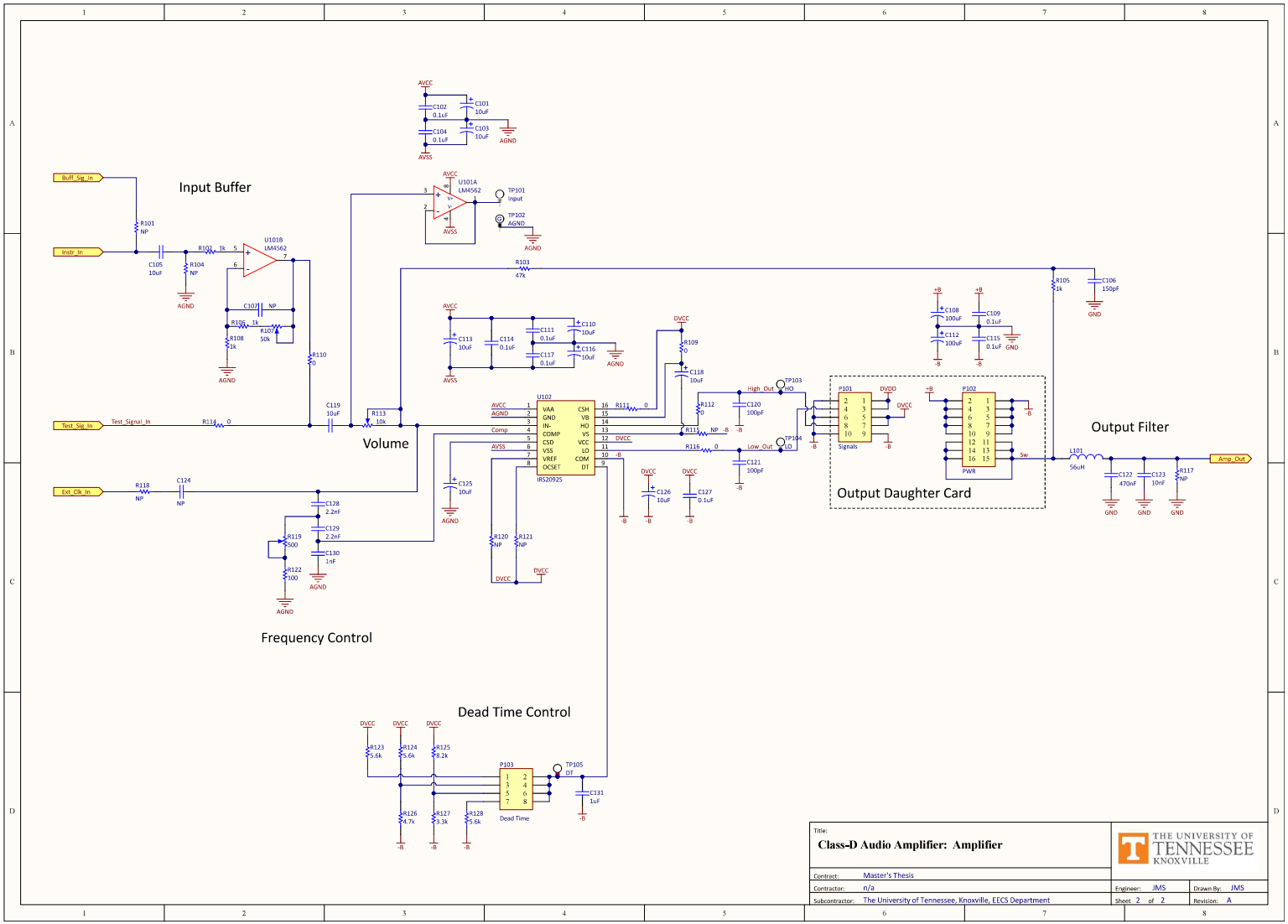


Figure 3.9: Test board schematic page 2

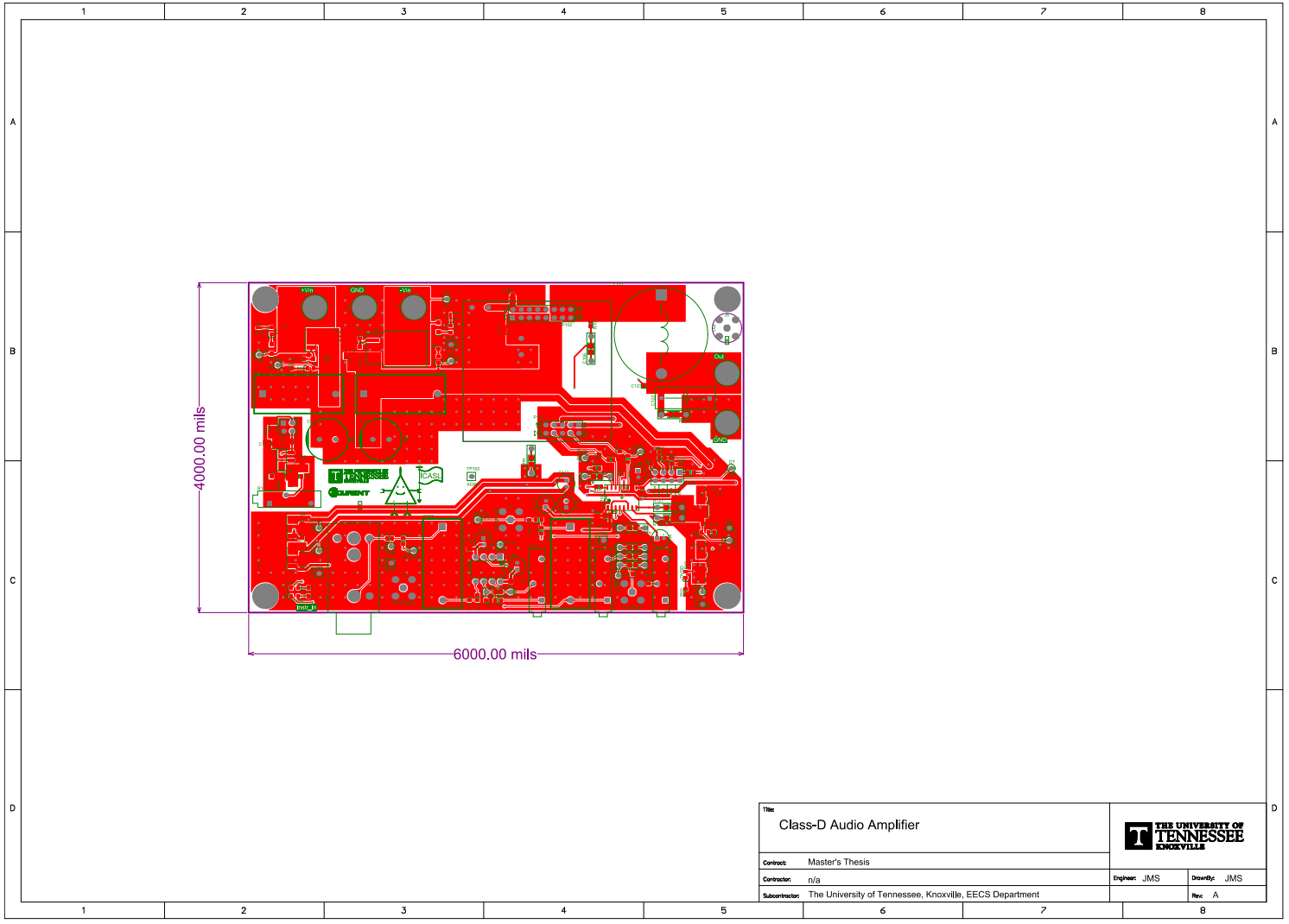


Figure 3.10: Test board PCB layout top layer with top silkscreen

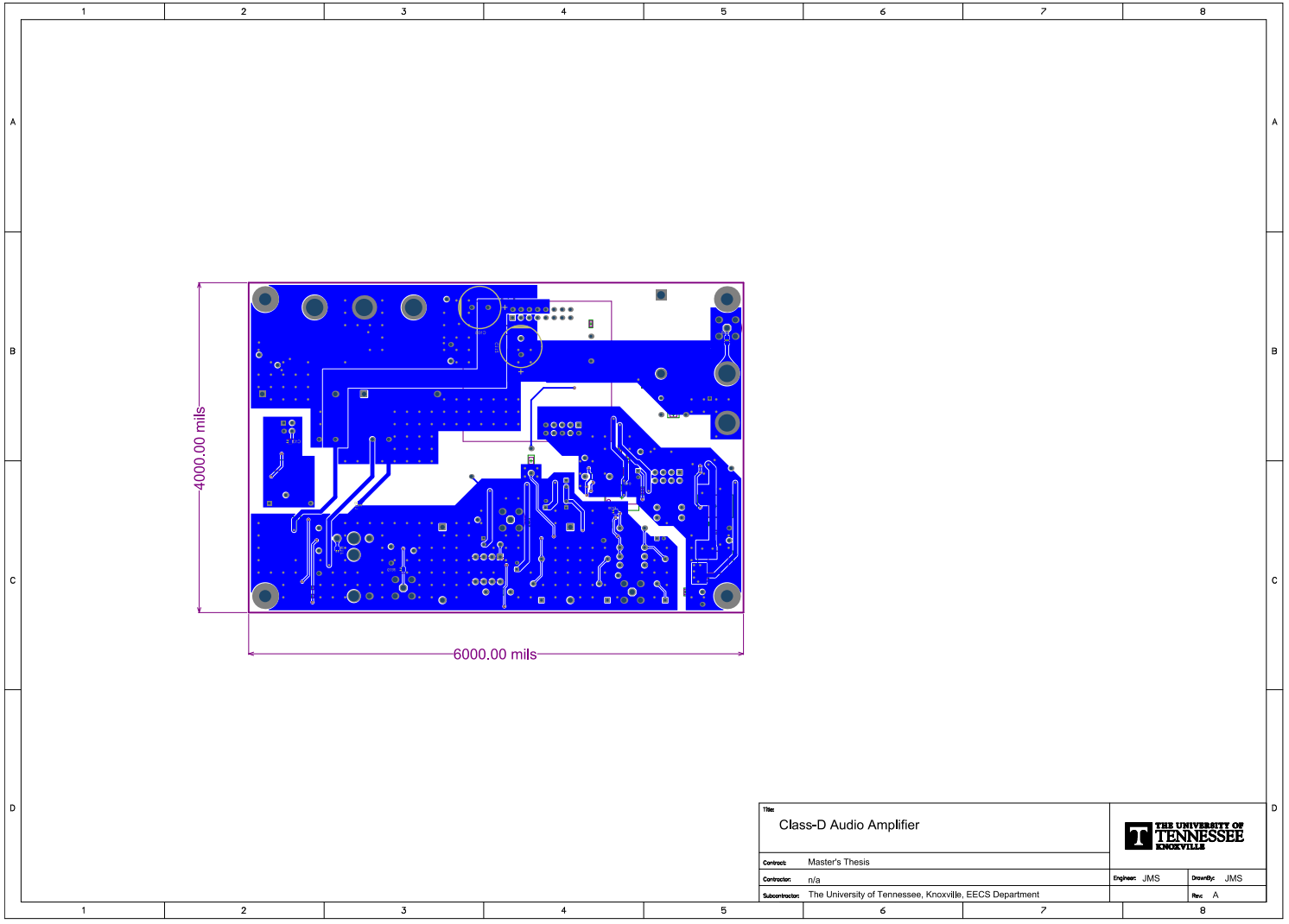


Figure 3.11: Test board PCB bottom layer

Chapter 4

Experimental Results

The goal of the experimental evaluation is to compare the performance of the GaN and Si Class D output daughter cards to each other and then compare the test results to that within the literature reviewed. To achieve these comparisons performance metrics such as THD, SNR, and power efficiency were observed over a wide range of operating points. The methods and techniques for observing these performance metrics are outlined in Section 2.4. A primary test would sweep the switching frequency and output power while monitoring THD, SNR, and power efficiency. A secondary test would evaluate voltage gain and frequency response at a switching frequency and output power level that are optimal for the desired metric.

The equipment used for these evaluations includes:

- Agilent 33250A — 80 MHz Function Generator
- Audio Precision APx515 — Audio Analyzer
- Dell OptiPlex 9010 — Windows Machine
- Fluke 87V — Digital Multimeter
- Keithley 2231A-30-3 — Triple Channel Power Supply
- Keysight 34465A — Benchtop Digital Multimeter
- Keysight InfiniiVision MSOX4024A — 200 MHz Mixed Signal Oscilloscope
- Stanford Research SR770 — FFT Network and Spectrum Analyzer

4.1 Primary Evaluation

This primary test used the Audio Precision APx515 Audio Analyzer to apply a test signal to the input while monitoring the output signal in order to measure THD and SNR. While the amplifier was operating, the input power, output power, and power to certain sections (*e.g.* gate drive, controller, analog power) would be monitored to examine the efficiency and power distribution of the circuit. The efficiency and power distribution data is more deeply examined in Appendix B.

Due to limitations of the test equipment, the highest load power deliverable was determined to be 12.5 W. Because the fundamental control element to the self-oscillating amplifier was the loop hysteresis, the maximum oscillating frequency is highly impacted by any delay [12, 16]. By using the built-in gate driver of the IRS2902 to drive the separate gate driver on the daughter cards, approximately 20 ns of delay was added to the circuit, thus limiting the maximum switching frequency to 450 kHz. Due to these constraints, the evaluated switching frequencies were only within the range of 150 kHz to 450 kHz. This range was separated into four steps spanning 100 kHz and the output power was swept from $1/5 \cdot P_{max}$ to P_{max} with five steps each spanning $1/5 \cdot P_{max}$.

Note: For the purpose of simplifying this analysis, only the case for $f_{sw} = 150$ kHz will be discussed in this Chapter. Other cases are included in Appendix B for an analysis of power measurements.

4.1.1 Sound Quality

The initial test evaluated the noise spectrum of the amplifier's output with each device daughter card with the input grounded. This would show the noise that was characteristic of the amplifier and output devices without any coloration from the signal generator. A spectrum analyzer was used to observe the output noise with a span from approximately 10 Hz to 25 kHz. The results are shown in Figure 4.1.[1]

[1] The spike at 15.6 kHz was determined to be EMI from the CRT display of the SR770 network analyzer

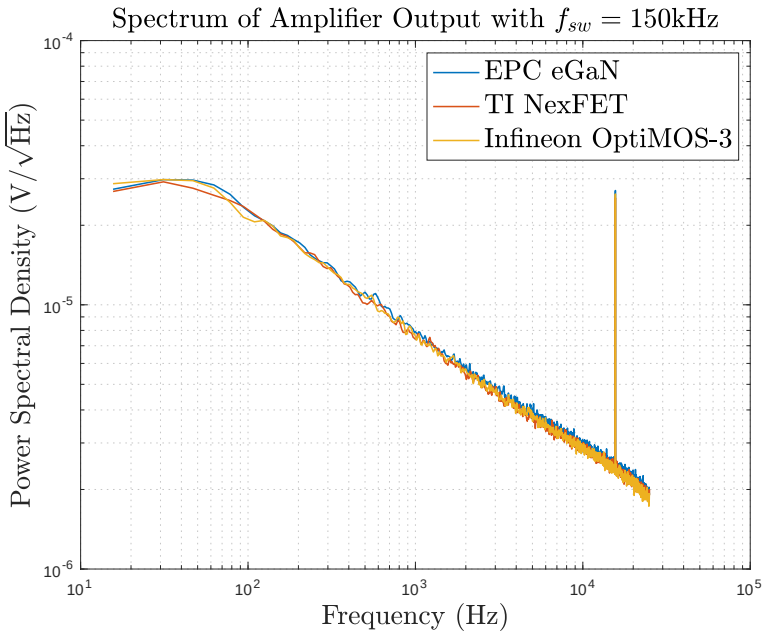


Figure 4.1: PSD of amplifier output with input grounded and $f_{sw} = 150$ kHz

Within the spectrum analysis, the noise color appears to be consistent between each device. The noise corner frequency was not captured by the spectrum analyzer and must exist beyond the span of the demonstrated results. When integrating the power spectral density (PSD) from 20 Hz to 20 kHz, the noise floor was determined to be approximately 540 μV_{rms} for each device. Also, when a test signal was applied to the input, the SNR measured approximately 82 dB for each device.

The largest sources of distortion in Class D audio are (a.) dead-time, (b.) inductor saturation, and (c.) the switching transients [7, 18]. The contributions of these sources to the total THD of the audio amplifier with each unique device daughter card was minimized to the extent practically possible given the constraints of the evaluation comparison. For each set of devices: (a.) the dead-time was a constant 21 ns (also the shortest setting capable of the IRS2092) and $t_{dt}/T_{sw} = 0.63\,\%$ when $f_{sw} = 150$ kHz; (b.) the selected inductor had a saturation current of 17 A, which was greater than 3× the max peak-to-peak current observed; and (c.) the gate series resistance was tuned to achieve switch node rise and fall times within the range of 30 ns to 50 ns each so that similar switching EMI could be expected.

It can be seen in the THD vs. power measurements of Figure 4.2 that each set of devices was consistent with the other sets. These trends were also consistent with the reviewed

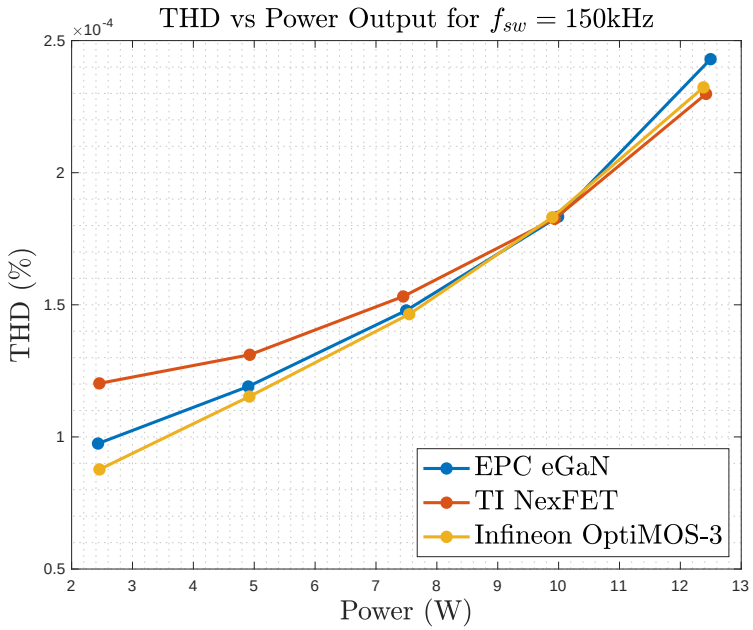


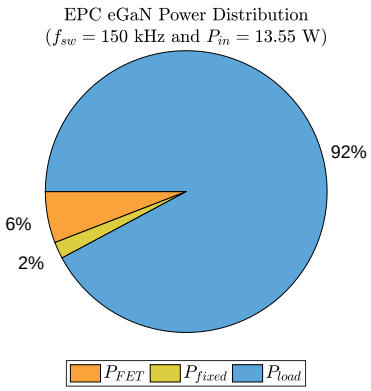
Figure 4.2: THD vs. output power for $f_{sw} = 150$ kHz

literature. Furthermore, for all switching frequencies tested (150 kHz to 450 kHz) the devices had similar trends with a lowest THD of 0.008 % and a highest of 0.025 %.

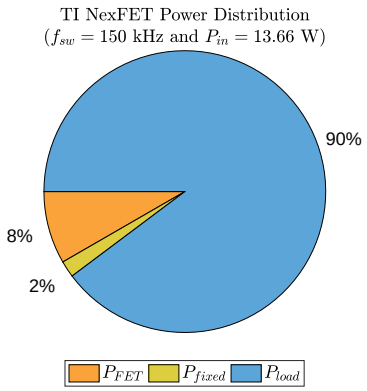
It is very difficult to rank the performance of the evaluated devices with respect to THD. In fact, the measured THD values for all data points were so very similar for each case that perhaps the largest contributors to the overall THD and noise could have been circuit elements and effects that were common between each device's evaluation (*e.g.* dead-time, inductor saturation, etc.). Furthermore, the lowest observed THD was also only an order of magnitude above what was specified by the Audio Precision APx515 audio analyzer with 0.0005 %. What should be deducted from the THD measurements, as well as the PSD analysis, is that for the test conditions the output devices (both GaN and Si) have negligible effect on the overall sound quality of the audio amplifier.

4.1.2 Efficiency

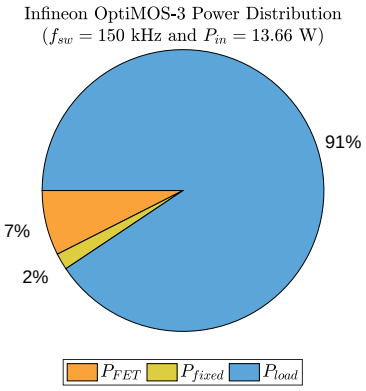
While measuring the THD, the input power and output power were monitored in order demonstrate the efficiency at each data point. The power losses of the system can be



(a) EPC eGaN®-FET



(b) Texas Instruments NexFET™



(c) Infineon OptiMOS™-3

Figure 4.3: Power distribution analysis

approximately modeled by Equation (4.1) [5].

$$P_{loss} = P_{pasives} + P_{fixed} + P_{FET} \tag{4.1}$$

For the evaluated circuit, P_{fixed} largely consists of the low-dropout regulators (LDOs) power losses. These (LDOs) are used to regulate multiple low voltage supply rails and to source current needed for indicator LEDs on the test PCB. The power distribution of the individual test boards is shown in Figure 4.3 for the case of $P_{load} = 12.5\,\mathrm{W}$. Since the losses due to passives components ($P_{passives}$) where determined to be $< 1\,\%$ of the total measured losses, $P_{passsives}$ are neglected within Figure 4.3.

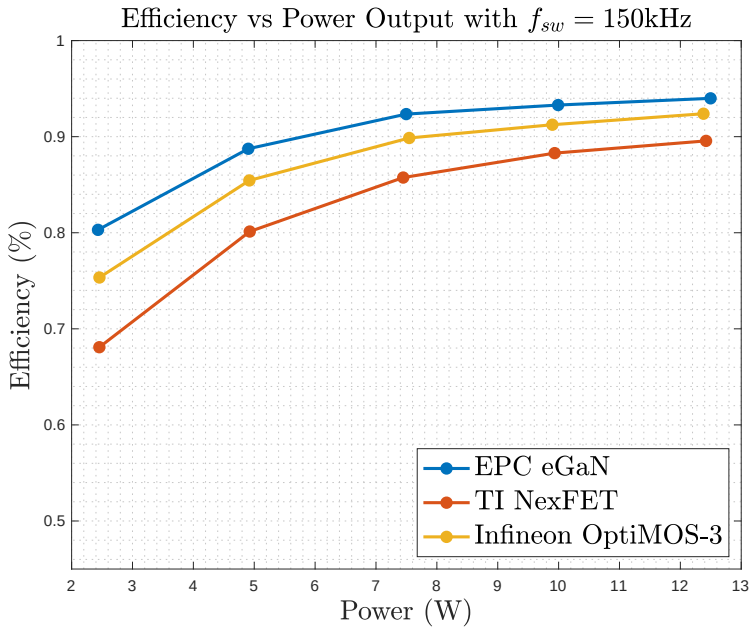


Figure 4.4: Efficiency vs. output power for $f_{sw} = 150$ kHz

Figure 4.4 shows the observed efficiency during the sweep of the output power. The trends were consistent among devices and with data in the literature reviewed. It was also verified that for any of the test cases of this experiment, GaN exhibited superior efficiency to either Si devices. Further analysis of the efficiency measurements and power distribution can be seen in Appendix B.

In addition to being more efficient, the GaN devices are much smaller than the TO-220 packages used for the same V_{DS} and I_D rated Si devices. The condensed packaging and logical pad layout allow for the gate drive and peripheral components to be more densely populated on the daughter card PCB. The difference in device volume density is even more apparent when including the package specific heat sinks (HS). This is shown along with the power density of the output stage in Table 4.1

Table 4.1: Daughter Card physical comparison

Daughter Card	Area [in^2]	Volume with HS [in^3]	Power Density [W/in^3]
EPC2031	0.2539	0.0555	$18.0 \cdot P_{out}$
TO-220	1.8750	2.5781	$0.39 \cdot P_{out}$

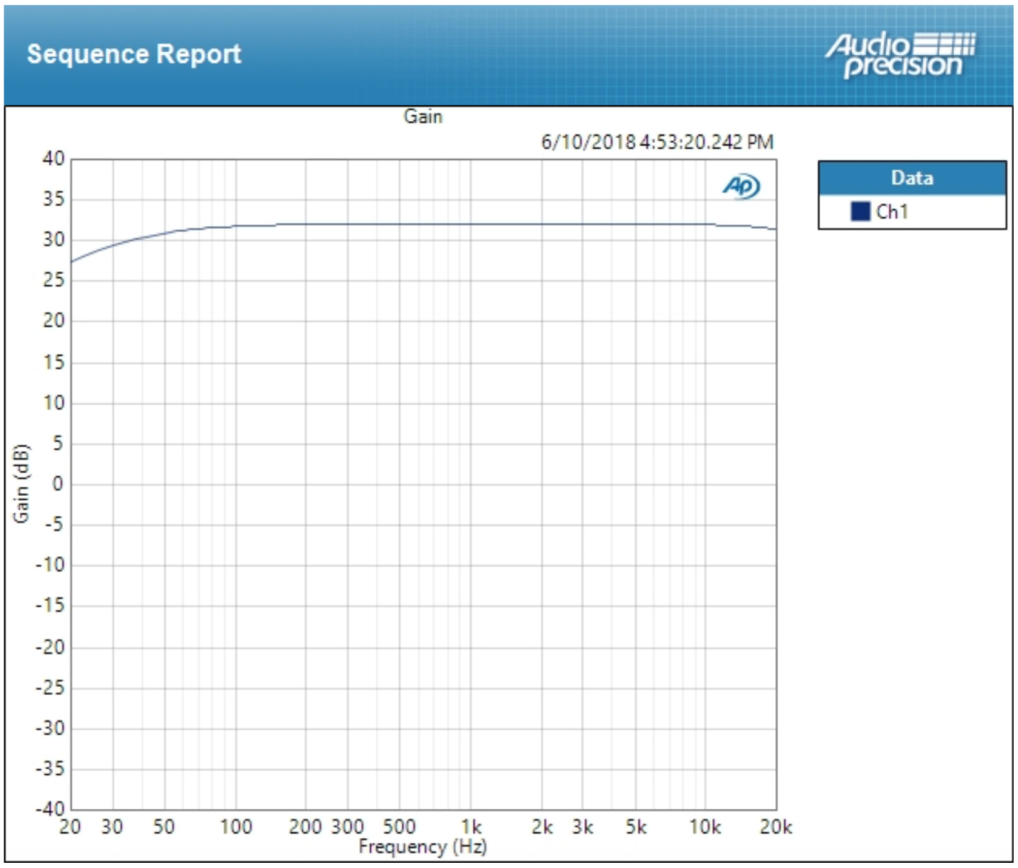


Figure 4.5: Gain bandwidth of experimental amplifier with $f_{sw} = 150\,\text{kHz}$ and $f_{test} = 1\,\text{kHz}$

4.2 Secondary Evaluations

The performance of the amplifier is also quantified by the midband voltage gain and voltage gain bandwidth (GBW). Using the automated tests of the Audio Precision APx515, the gain bandwidth was determined to be approximately 25 Hz to 25 kHz with an $8\,\Omega$ load and a midband voltage gain of 26 dB (shown in Figure 4.5). Figure 4.6 shows the input and output waveforms amplifier with $f_{sw} = 150\,\text{kHz}$ and $f_{test} = 1\,\text{kHz}$ for max power of 12.5 W and $A_v = 32\,\text{dB}$. A maximum midband gain of 122 dB was achieved achieved by increasing the volume control with a $50\,\text{mV}_{\text{pp}}$ input test signal and an $8\,\Omega$ load (shown in Figure 4.7).

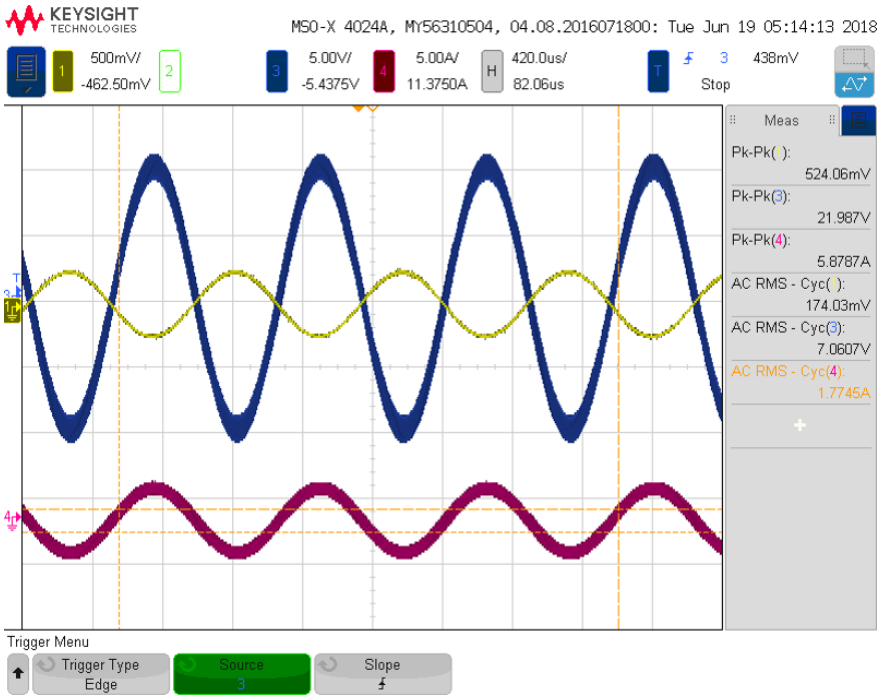


Figure 4.6: Experimental waveforms of input and output signal with $f_{sw} = 150\,\text{kHz}$ and $f_{test} = 1\,\text{kHz}$. Input voltage (yellow), output voltage (blue), and output current (magenta)

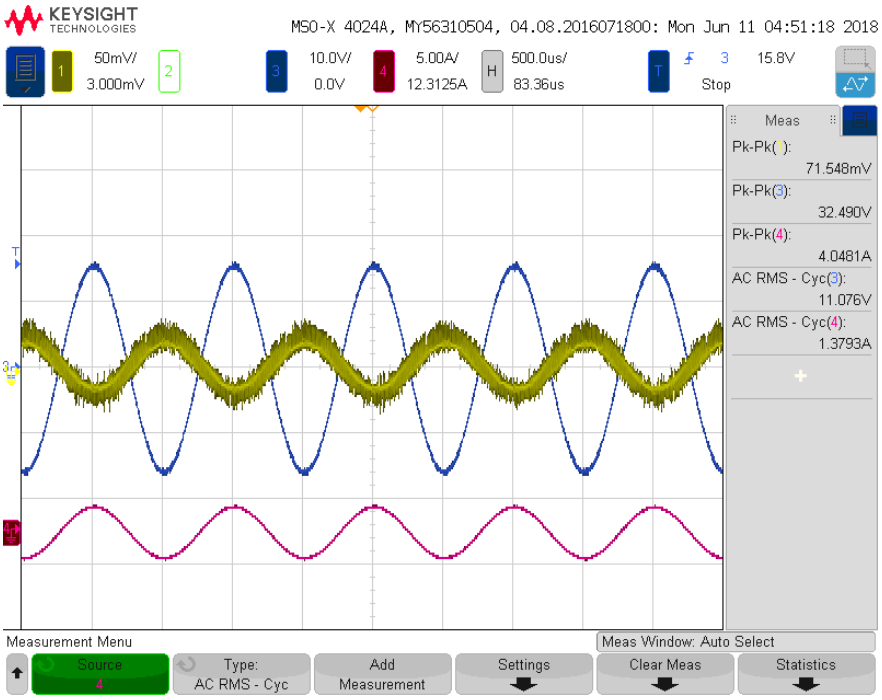


Figure 4.7: Experimental waveforms demonstrating maximum gain of 122 dB with $f_{sw} = 150\,\text{kHz}$ and $f_{test} = 1\,\text{kHz}$. Input voltage (yellow), output voltage (blue), and output current (magenta)

Table 4.2: Amplifier performance summary

Parameter	Symbol	Observed	Condition
Maximum Output Power	$P_{out(max)}$	12.5 W	4 Ω load
Output Power Efficiency	η	94 %	Max with GaN-FET
Total Harmonic Distortion	THD	0.008 %	Min with OptiMOS™-3
Signal-to-Noise Ratio	SNR	82 dB	$f_{test} = 1$ kHz
Midband Voltage Gain	A_{mid}	122 dB	$f_{test} = 1$ kHz
Low Cutoff Frequency	f_{low}	25 Hz	$f_{test} = 1$ kHz
High Cutoff Frequency	f_{high}	25 kHz	8 Ω load

4.3 Summary of Experimental Evaluations

A summary of all the measured performance metrics of the experimental Class D amplifier is shown in Table 4.2. The lowest performance was with respect to the SNR observed, which could be improved by using higher order filters in the feedback loop and output stage and EMI shielding from a possibly noisey environment [15].

4.4 Comparison with Literature Reviewed

Using the metrics defined in Section 2.5.3, the designed amplifier performed similarly or better than the literature reviewed with respect to THD and efficiency (see Table 4.3). This work had very similar performance to the circuit of Duraij et al. [15]. As previously discussed, the THD and SNR for a ΣΔ-based (or PDM) Class D audio amplifier should be superior to a PWM or self-oscillating PWM Class D amplifier, while the efficiency should be inferior. However, when comparing this work with the literature reviewed, the ΣΔ-based amplifier by Chung et al. [11] had significantly lower performance in all these metrics. What has been

Table 4.3: Comparison of this work with literature reviewed

Author	Material	Efficiency [%]	THD [%]
Duraij et al. [15]	GaN	95.0	0.008
Chung et al. [11]	GaN	82.2	0.800
Chung et al. [11]	Si	67.0	0.500
** This work	Si	92.4	0.008
** This work	GaN	94.0	0.010

Table 4.4: Comparison of this work with commercially available amplifiers

Manufacturer	Model	Class	Power [W]	THD [%]	Cost [USD]
NAD	D 3020	D	30	0.005	$399.00
Schiit	Lyre 3	AB	9	0.010	$499.00
McIntosh	MHA150	AB	50	0.005	$4500.00
** This work		D	12.5	0.008	TBD

discussed in this work is that the impact of dead-time, inductor saturation, and switching transients has a much greater impact on the THD than the devices chosen. The data in the article by Chung et al. [11] does not support this, since it is claimed that GaN has superior THD performance as well as efficiency. This article does not consider any contributions to the distortion besides the devices and their intrinsic properties and could be a possible reason for significantly inferior performance.

This work is also compared to some commercially available audio amplifiers in Table 4.4; and again, this comparison is based on the metrics defined in Section 2.5.3. Note that the unit cost of the experimental amplifier has not yet been determined, but perhaps an adventure beyond this thesis could lead to determining those values.

Chapter 5

Conclusions

5.1 This Work

There are several reasons why GaN has thus far not made a significant impact on Class D audio. The cost of the evaluated EPC eGaN®-FET was $7.46 and the closely performing Infineon OptiMOS™-3 was $1.28. It is difficult to determine if the increase in efficiency and higher power density can justify the nearly 6× increase in cost. Another significant obstacle for GaN in Class D audio is the lack of commercially available and GaN compatible Class D ASICs and controllers. Since this evaluation used an ASIC Class D audio controller intended for use with Si devices, a series gate driver for GaN devices needs to be used in order for the GaN devices to be evaluated. If there were a Class D controller for GaN, perhaps GaN could achieve much greater THD performance than a similar circuit with Si devices.

There is a relation of the device costs and the availability of GaN compatible ASICs and controllers, and the only path to achieving a low cost and high application environment for GaN is: to continue to explore these new applications; demonstrate GaN superiority over traditional Si devices across; and to increase the demand for GaN devices. This work explores the use of GaN in Class D audio applications by demonstrating a negligible difference in sound quality from a side-by-side comparison of GaN and Si FETs. The superior efficiency of GaN during these evaluations suggest that GaN will allow for lower heat radiation and longer battery life than Si MOSFETs. The smaller package size and logical pad layout of

the GaN devices led to smaller circuit footprints and a higher power density in application. Therefore, GaN could lead to significant improvements within Class D audio applications.

5.2 Future Work

Future work is proposed to increase the power levels of the conducted evalation. A recent upgrade to the laboratory space will allow for an expanded 50 W evaluation of the tested devices. Additional tests for 100 V and 40 V devices at power levels of 100 W and 30 W power levels respectively will also be conducted. The evaluations of an extended power range and alternate devices will provide further support of the work in this thesis; and perhaps, motivate a design and implementation of the first GaN compatible ASIC for Class D audio applications.

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Appendices

A Survey of GaN Power Electronics Devices

A.1 Introduction to WBG

Wide Bandgap (WBG) is in reference to a wider energy gap of the material, which is the electrical potential between the highest filled electron orbital at steady state and the closest unfilled orbital. This is shown mathematically as $E_g = E_c - E_v$; where E_g is the energy gap, E_c is the energy level of the conduction band, and E_v is energy level of the valence band. Within the energy gap, there exist no wavelike orbital for an electron to exist; therefore, this region is known as the "Forbidden Band [19]." Because of this there must be a finite quantity of energy required to elevate or excite the electron from the valence band to the higher state conduction band. The distance of the bandgap is directly proportional to the strength of electrical field required to force the semiconductor into breakdown [20].

The WBG materials currently receiving the greatest attention are Silicon Carbide (SiC) and Gallium Nitride (GaN). A summary of these materials' properties compared to that of Si is provided in Table A.1 and visually within Figure A.2.

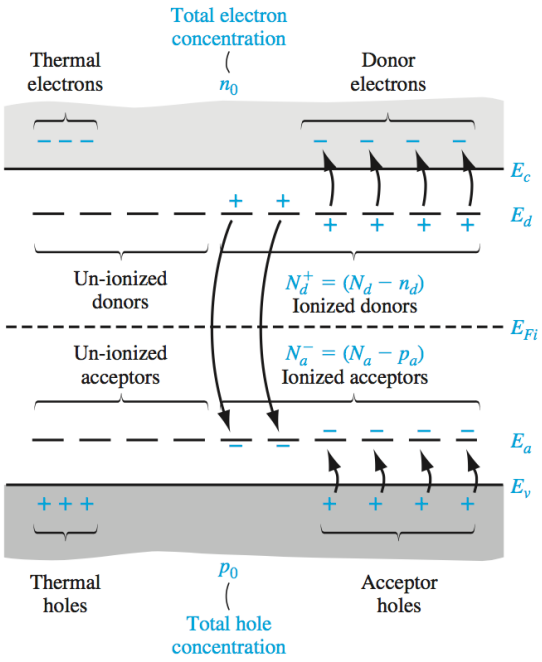


Figure A.1: Energy-band diagram [21]

Table A.1: Comparison of semiconducting materials [22]

	μ [cm^2/(V·s)]	v_s [cm/s]	ϵ_r	E_g [eV]	BFM ratio*	JFM ratio†	T_{max} [°C]
Si	1300	1×10^7	11.4	1.1	1.0	1.0	300
SiC	260	2×10^7	9.7	2.9	3.1	60	600
GaN	1500	2.2×10^7	9.5	3.4	24.6	80	700

* Baliga's figure-of-merit: $BFM = \epsilon\mu E_g^2$
† Johnson's figure-of-merit: $JFM = \frac{E_c v_s}{2\pi}$

The primary obstacle preventing these WBG materials from equal market share with their Si equivalents is the immaturity of processing and fabrication, which is directly related to cost. It can be seen that the demand for Si alternatives, specifically that of GaN, has continually increased and the processing is quickly maturing due to LED manufacturing and the performance within high-frequency and high-voltage applications of GaN-based heterojunction high electron mobility transistors (HEMTs) [1].

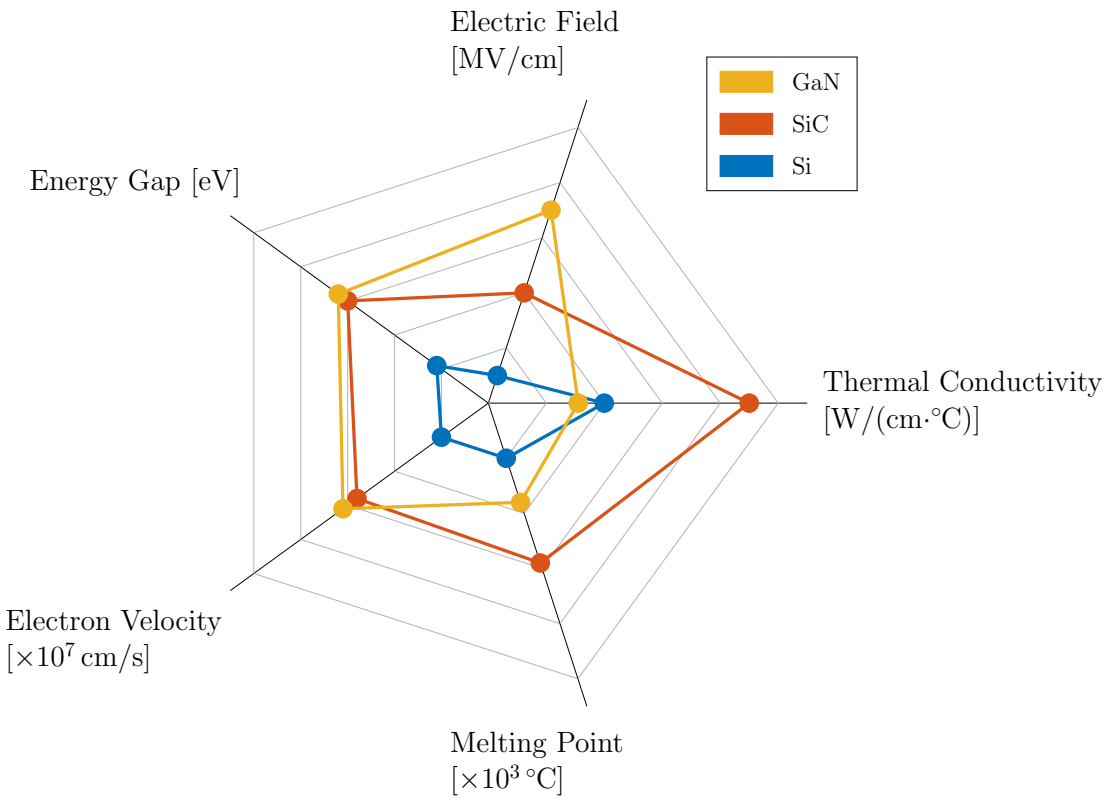


Figure A.2: Summary of Si, SiC, and GaN relevant material properties [23]

An overview of current GaN technology was previously cataloged in a survey of the most prominent WBG advances by Millán et al. [1]. It was established that the main interest in GaN was rooted in the material's "wide bandgap, large critical electric field, high electron mobility, and reasonably good thermal conductivity." The improvements of GaN processing have overcome the rarity of quality free-standing GaN substrates by the development of processes which include the growth of epilayers on foreign substrates such as SiC, sapphire, and Si.

In the area of GaN rectifiers, the massive reverse voltage blocking capabilities were noted by Millán et al. [1]; where breakdown voltages upwards of 9.7 kV for vertical devices grown on sapphire substrates were recorded. Millán et al. [1] predicted upcoming technologies to include 600 V Schottky Diodes that could compete with SiC rectifiers due to the availability of high-temperature vapor phase epitaxy free-standing GaN substrates.

The processing techniques of GaN transistors has yielded a higher mobility by the existence of a 2-D electron gas (2DEG) between the heterostructure of AlGaN/GaN. Since the conduction bands between AlGaN and GaN are discontinuous at this junction, the 2DEG concentrates and increases the mobility to ranges of 1200 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$ to 2000 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$. These HEMTs are normally-on devices or depletion mode, requiring a negative gate bias to force the 2DEG out of the heterostructure. The main improvements that the HEMT process needs to overcome in order to achieve an increase in electrical performance, as described by Millán et al. [1], was the suppression of drain current collapse and an increase control of the bulk and surface trap densities to increase the gate-drain breakdown voltage (V_{gd}).

Considering depletion mode devices are not widely useful in power electronics applications, research has been increasing to produce normally-off or enhancement mode GaN HEMTs. The recessed-gate structure has been one way to achieve this goal. As demonstrated by Saito et al. [24] (Figure A.3), the AlGaN layer directly beneath the gate can be optimized for thinness so that the 2DEG cannot form. Without the 2DEG, the threshold voltage needed to turn on the device becomes positive. The use of fluorine- or chlorine-based plasma provides another solution. As the halide plasma enters the AlGaN barrier, the threshold voltage begins to shift. The plasma does damage the AlGaN barrier during this process, but moderate temperature annealing can recover the barrier. It is then described by Millán et al. [1] that

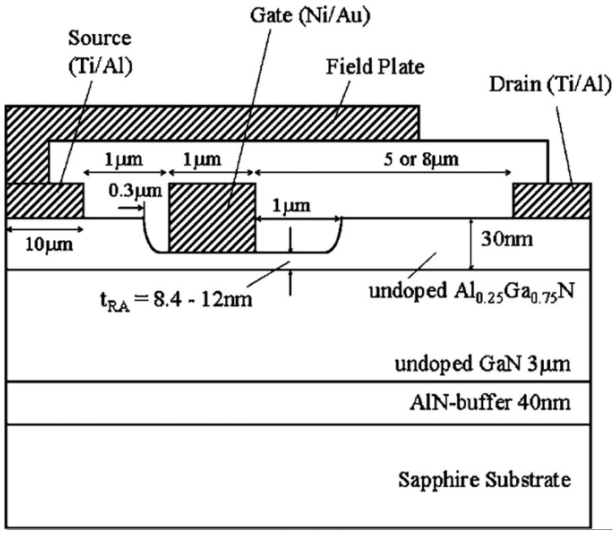


Figure A.3: Recessed-gate GaN HEMT [24]

approaches using both techniques, recessed-gate and plasma treatment, simultaneously have successfully yielded high-performance normally-off AlGaN/GaN HEMTs.

With development of enhancement mode GaN transistors, the lateral structure of GaN MOSFETs (see Figure A.4) have shown great performance with the high-voltage switching applications of power electronics. The lateral organization of layers results in an offset of the conduction band that minimizes the probability of hot carrier injection (HCI), where an electron or hole can possess sufficient kinetic energy to tunnel through a potential barrier forming a space charge that will degrade or destroy a device [25].

Millán et al. [1] describes a major design obstacle of the enhancement mode GaN transistor which is the dynamic on-state resistance. Dynamic on-state resistance is a temporary increase in the drain to source resistance when a device is initially turned on.

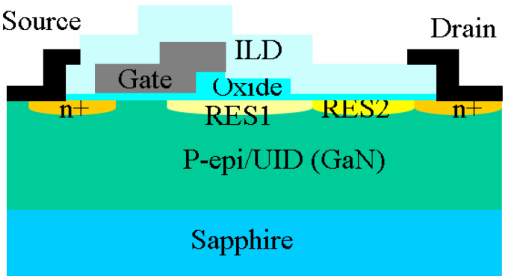


Figure A.4: Lateral GaN hybrid MOS-HFET [25]

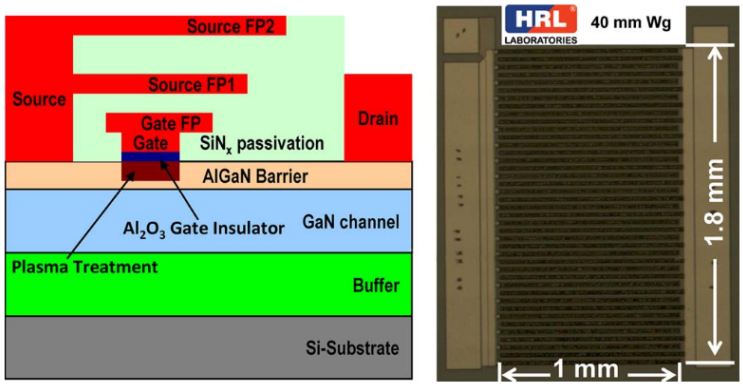


Figure A.5: (Left side) Cross-sectional schematic of device structure and (right side) microscopy top view photograph of GaN-on-Si FET [26]

This dynamic resistance must be managed with proper design considerations at both the circuit and device level in order to mitigate the resulting effect known as current collapse.

A.2 Recent Technologies

A 1.2 kV GaN-on-Si FET was developed by Chu et al. [26] with special attention given to the dynamic ON-resistance measured at the time directly after switching from OFF to ON state. The dynamic ON-state resistance is typically discussed in reference to current collapse, a major obstacle of GaN transistor implementation previously noted by Millán et al. [1]. A halide plasma treatment of Fluorine- and Chlorine-based gas depleted the 2DEG beneath the gate, making the device normally-on. The Chlorine was shown to improve the device's transconductance and threshold hysteresis during a V_{GS} sweep. The magnitude of reverse breakdown voltage (V_{br}) was attributed to the high-resistivity buffer layer, halide plasma treatment, and an Al_2O_3 gate dielectric. The device layer organization is shown in Figure A.5. Dynamic ON-resistance was evaluated by measuring the static ON-resistance at $t = 5\,\mu s$ from device turn on at $t = 0$. It was determined that the examples using using multiple field-plates that provide greater control of the electric field at high blocking voltages would also have a lower dynamic ON-resistance to static ON-resistance ratio. It was also determined that the device with the most field-plates exhibited this performance metric closest to that of an commercial-off-the-shelf Si MOSFET (See Figure A.6).

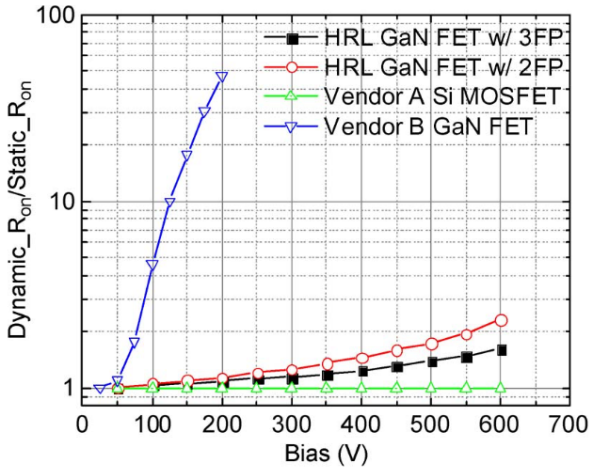


Figure A.6: Comparison between multiple devices of the ratio between dynamic ON-resistance and static ON-resistance at varied operating biases [26]

A 1.7 kV hybrid MOS-HFET on Si substrate with "state-of-the-art" Ti/AlSi/Mo-based ohmic electrodes was described by Ikeda et al. [27] (See Figure A.7). Previous experiments were evaluated showing that the thickness of the epitaxial layer was proportional to the reverse breakdown voltage (V_{br}). The gate-to-drain length (L_{gd}) could be optimized to further increase V_{br}, but this method was shown to increase the specific on-state resistance (P_{on}) of the device. So, the use of a thin undoped "(u)-GaN" channel layer on top of a high-resistivity carbon-doped GaN layer would maximize V_{br} while minimizing the influence of L_{gd} to P_{on}. The resulting parameters of this experiment were $P_{on} = 7.1\,\mathrm{m\Omega{\cdot}cm^2}$ for $L_{gd} = 12\,\mu\mathrm{m}$ and $V_{br} = 1.7\,\mathrm{kV}$ for $L_{gd} = 18\,\mu\mathrm{m}$.

A 1.6 kV Vertical GaN-based trench MOSFET was developed by Oka et al. [28] on a free-standing GaN substrate. The advantage of the free-standing GaN substrate is that the breakdown voltage is proportional to the drift region thickness without sacrifice to the size

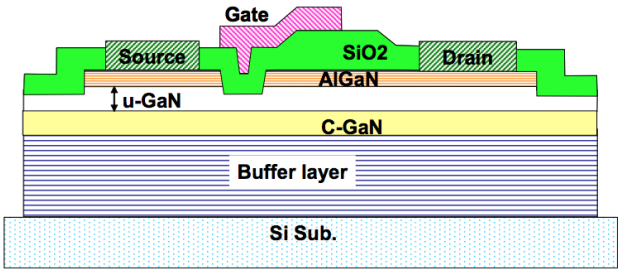


Figure A.7: AlGaN/GaN hybrid MOS-HFET [27]

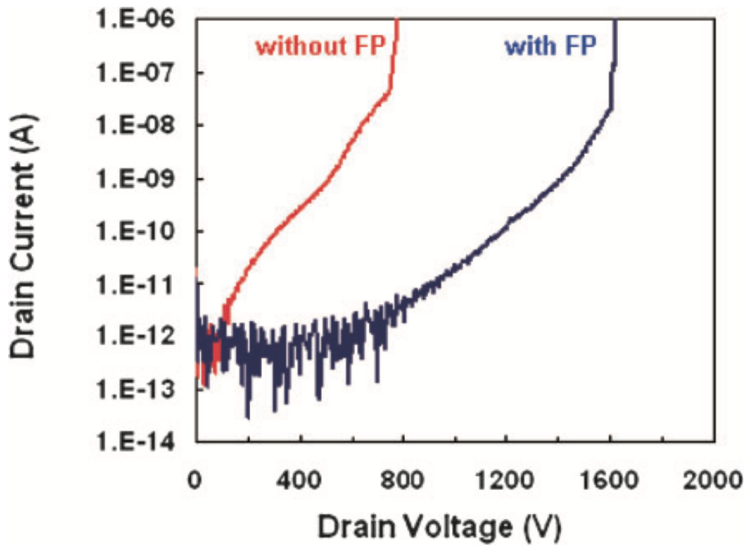


Figure A.8: Off-state I-V characteristics for both with and without field plates [28]

of the device. This leads to greater power density than that compared to other available substrates for GaN devices. This device used a buried p-body and source stack to minimize the cell pitch. The cell pitch, distance between source electrodes, is also the active region. Field plate edge terminations were used to reduce the electric field at the edge of the p-n junction and also to reduce current crowding. The effect of the field plates on the leakage current is shown in Figure A.8. The observation was made that field plates would significantly reduce the device's off-state leakage current which was a result of the reduction in electric field at the edge. This also correlated to an increase in potential blocking voltage. The resulting parameters were a $V_{br} = 1.6\,\text{kV}$ and $P_{on} = 12.1\,\text{m}\Omega\cdot\text{cm}^2$.

A 1.5 kV vertical GaN transistor on Bulk GaN was developed by Nie et al. [29]. It was predicted that bulk GaN substrates would make it possible to "realize the material limit potential of GaN including true avalanche breakdown capability and to create vertical architectures that do not suffer from thermal management issues associated with thin film surfaces, and provide increased number of die on a wafer." The use of the more common foreign substrates (sapphire, Si, and SiC) has made the fabrication of vertical devices difficult and demonstrates larger defect densities. By using edge termination and other processing techniques typical of vertical p-n devices, it was shown that homoepitaxial growth on GaN substrates can result in high-performance vertical GaN power transistors. The layer

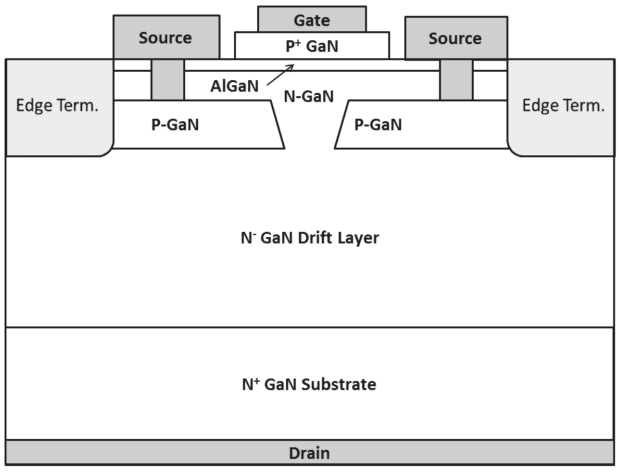


Figure A.9: Vertical GaN on bulk GaN [29]

organization of the transistor developed is shown in Figure A.9. This particular device compares to that of Oka et al. [28] with the junction termination and the shorting of the buried p-layers to the source terminals. The resulting parameters were a $V_{br} = 1.5\,\text{kV}$ and $P_{on} = 2.2\,\text{m}\Omega{\cdot}\text{cm}^2$.

As described previously by Chu et al. [26], the obstacle of current collapse in GaN devices has become a major obstacle. However, the structure designed by Kaneko et al. [30] has proven to completely eliminate current collapse in a GaN-on-Si transistor. The hybrid drain embedded gate injection transistor (HD-GIT) uses an additional p-GaN region in close proximity to the drain electrode (see Figure A.10). The holes injected from this region during the off-state release trapped electrons which eliminates current collapse. By optimizing the thickness of the AlGaN layer beneath the p-GaN region along with the 2DEG, the normally-off operation can be established. The depth of the recessed gate is used to control the V_{TH}. It was noted by Kaneko et al. [30] during experimental evaluations that the addition of the p-GaN did not negatively affect the reverse conduction nor increase the voltage offset during reverse bias. This was attributed to the sheet carrier concentration of the AlGaN in this region. Figure A.11 compares the ratio of dynamic ON-resistance to the static ON-resistance at $t = 4.5\,\mu\text{s}$ from device turn on at $t = 0$. Through these evaluations it was determined that the HD-GIT structure was free from current collapse during operation to a maximum blocking voltage of 850 V.

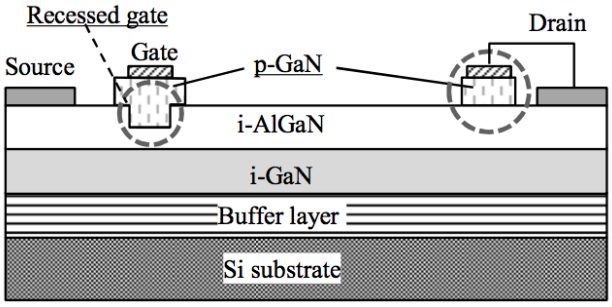


Figure A.10: Proposed HD-GIT layer organization [30]

The most recent experimentation evaluated is the development of vertical fin power FETs. Designed by Sun et al. [31], fifty fins measuring 100 µm × 0.18 µm each were grown on bulk GaN substrate and demonstrated performance metrics comparable to commercially available enhancement mode GaN FETs. The device organization is shown in Figure A.12. Field plates with edge termination helped to control the off-state leakage current and helped to achieve a $V_{br} = 800\,\text{V}$. The specific on-state resistance was shown to be $P_{on} = 0.36\,\text{m}\Omega{\cdot}\text{cm}^2$.

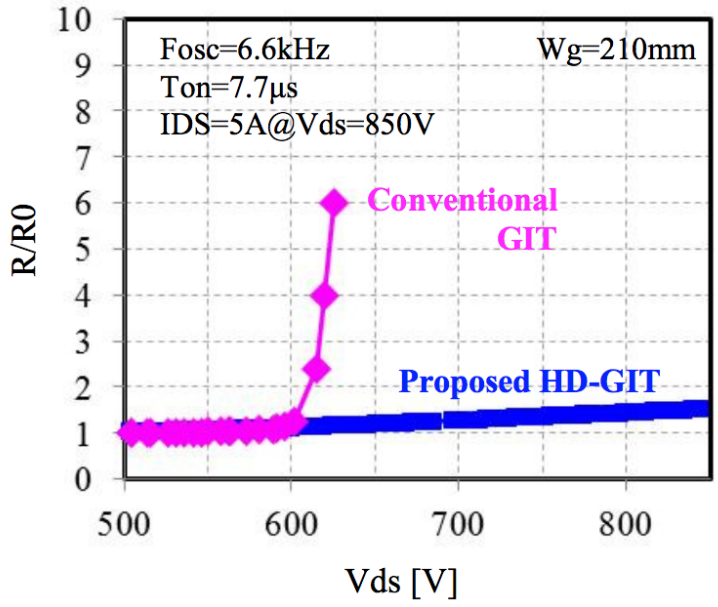


Figure A.11: Comparison between multiple devices of the ratio between dynamic ON-resistance and static ON-resistance at varied V_{DS} [30]

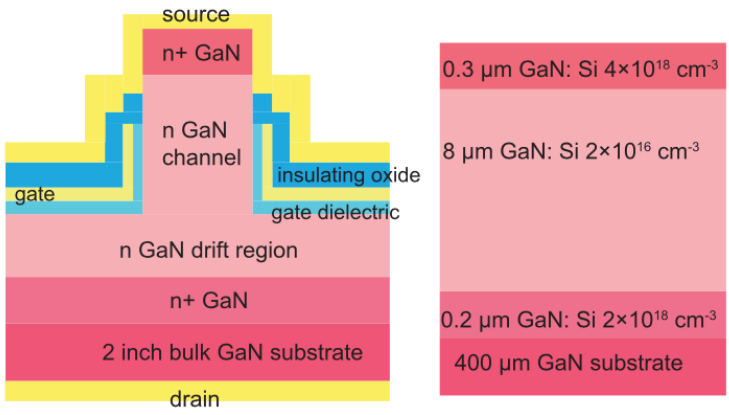


Figure A.12: (Right side) Layer organization of proposed vertical fin power FET and (left side) beginning epi-structure [31]

A.3 Summary

The experimental results of multiple GaN devices have been discussed which should lead to the conclusion that GaN is being elevated to compete directly with Si devices for power electronics circuits. The main performance benefits of GaN is the ability to perform at higher temperatures, higher blocking voltages, and the option to switch faster with comparable losses to the current generation Si power electronic devices. It should be noted that the processing and fabrication of GaN has dramatically improved over recent years and will continue to do so as long as the demand for high-performance alternatives to Si exist.

B Efficiency Analysis

Because of the Class D amplifier's similarities to the synchronous buck converter, an analysis of the power measurements can be made through the lens of a power electronics engineer.

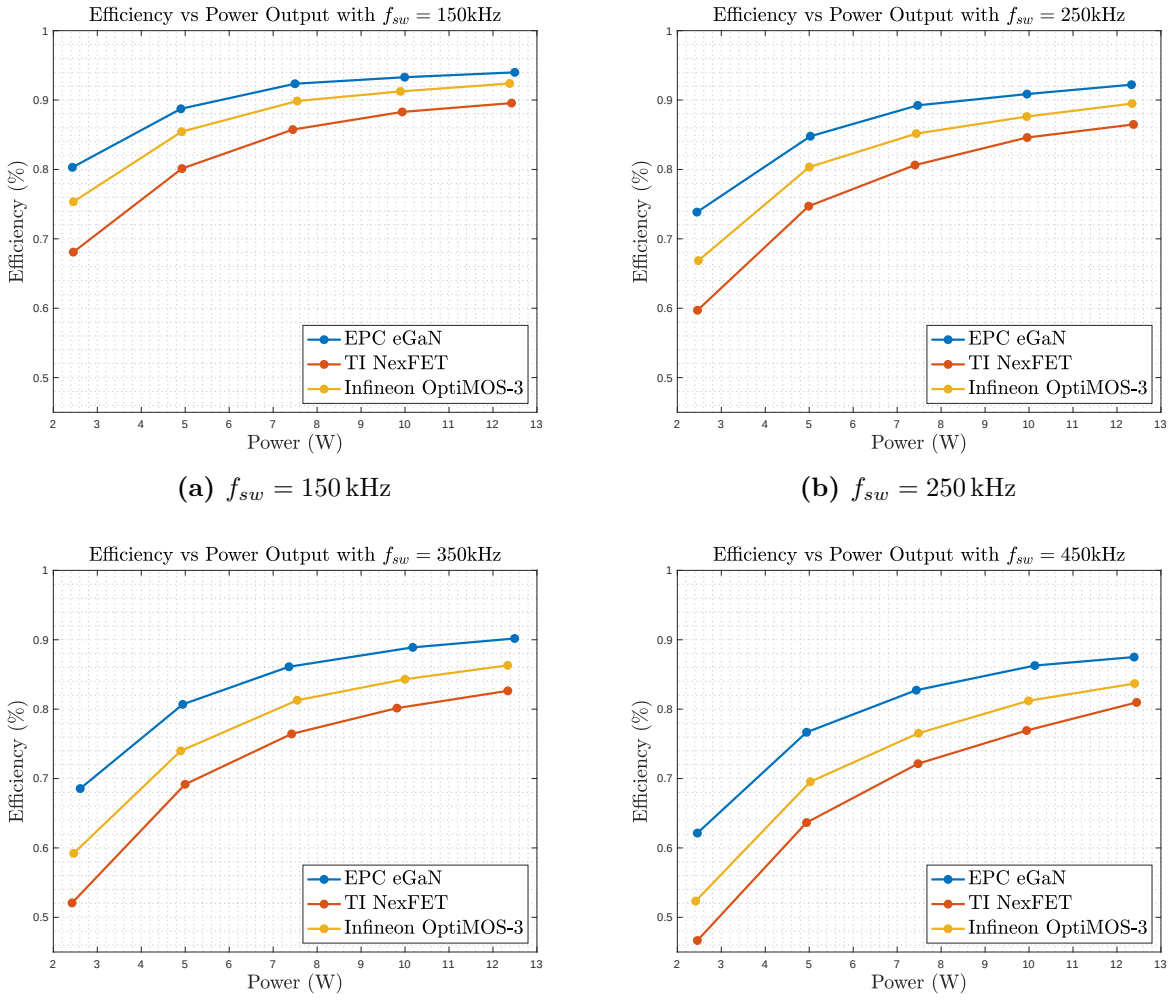
The test results of the primary evaluation (Section 4.1) are organized to demonstrate the relationship of efficiency with output power in Figure B.1 and efficiency with switching frequency in Figure B.2. It can be understood from these figures that for all devices the efficiency increases with output power, but decreases with switching frequency. It has been shown previously that P_{sw} is largely dependent on the switching speed [5, 6]. Some loss factors increase with output power; however, their contributions are often dominated by the output power in the efficiency calculations.

Because of the similarities to the synchronous buck converter, the simple buck converter loss model can be applied to the Class D audio amplifier. The loss model is not entirely accurate for the Class D audio amplifier though, but is accurate enough to predict the performance of the Class D audio amplifier under certain conditions. The main differences between the simple buck converter loss model and the Class D audio amplifier are with respect to the the duty cycle and switching frequency. The duty cycle is dynamic in Class D applications, but assumed to be static for the simple buck converter loss model. Within the PDM and self-oscillating Class D the switching frequency is also dynamic, impacted by the instantaneous amplitude of the input signal. Because of these dynamics, an effective duty cycle is assumed to be $D = 50\,\%$ and an effective switching frequency will be assumed to be equal to the switching frequency for the case of grounded input.

In the simple buck converter loss model, the largest source of losses are due to the power devices (P_{FET}) [5, 15]. The total losses of the MOSFET can be defined by Equation (B.1).

$$P_{FET} = P_{sw} + P_{cond} + P_{gd} \tag{B.1}$$

The losses during transition between on and off states is given by the switching loss (P_{sw}) shown in Equation (B.2), where C_{oss} is the output capacitance and t_f is the fall time [32]. These values are intrinsic to the device and given in the manufacturer datasheet. These



(a) $f_{sw} = 150\,\text{kHz}$ **(b)** $f_{sw} = 250\,\text{kHz}$

(c) $f_{sw} = 350\,\text{kHz}$ **(d)** $f_{sw} = 450\,\text{kHz}$

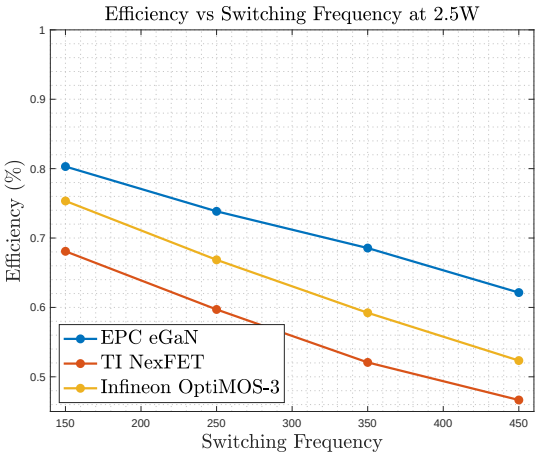
Figure B.1: Efficiency versus output power for 60 V devices

values along with other device parameters needed for the loss model are summarized in Table B.1.

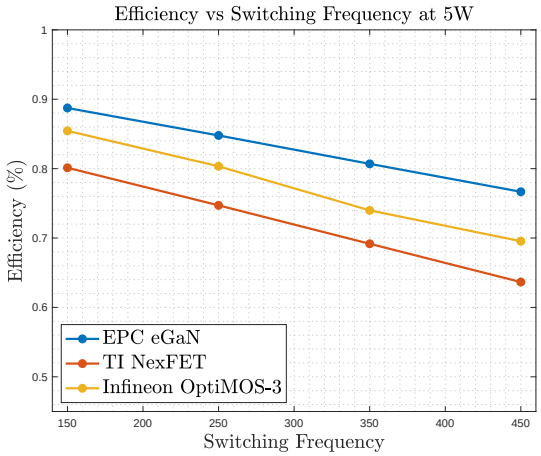
$$P_{sw} = C_{oss} \cdot V_{bus}^2 \cdot f_{sw} + I_D \cdot V_{DS} \cdot t_f \cdot f_{sw} \tag{B.2}$$

The conduction losses (P_{cond}) of the switches can be modeled by Equation B.3 [32].

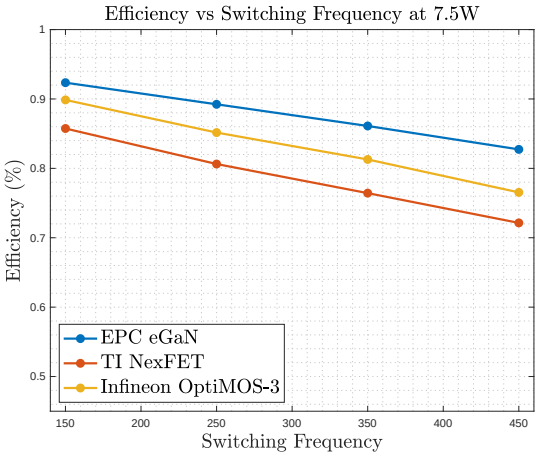
$$P_{cond} = \frac{R_{DS(ON)}}{R_{load}} \cdot P_{out} \tag{B.3}$$



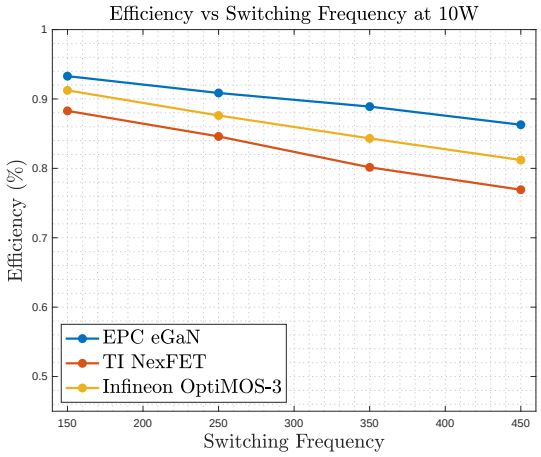
(a) $P_{out} = 2.5\,\mathrm{W}$



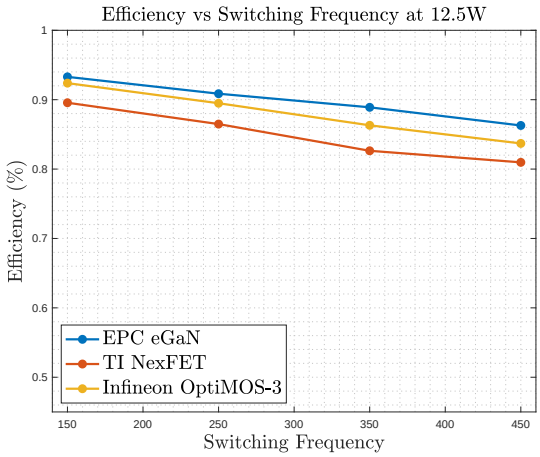
(b) $P_{out} = 5\,\mathrm{W}$



(c) $P_{out} = 7.5\,\mathrm{W}$



(d) $P_{out} = 10\,\mathrm{W}$



(e) $P_{out} = 12.5\,\mathrm{W}$

Figure B.2: Efficiency versus switching frequency (f_{sw}) for 60 V devices

Table B.1: Summary of device characteristics contributing to power losses

Manufacturer	Part Number	Material	V_{DS} [V]	t_f [ns]	$R_{DS(ON)}$ [mΩ]	Q_{rr} [nC]	C_{oss} [pF]
EPC	EPC2031	GaN	60		2		980
Texas Instruments	CSD18534KCS	Si	60	2.4	8	68	164
Infineon	IPA093N06N3	Si	60	5	9.3	40	640

The gate driver losses (P_{gd}) from charging and discharging the gate in order to turn on or off the device are given in Equation (B.4) [32].

$$P_{gd} = 2 \cdot Q_g \cdot V_{GS} \cdot f_{sw} \tag{B.4}$$

Another significant source of losses is due to the reverse recovery of the low side FET's body diode. This loss does not contribute to the GaN device power loss model because they are constructed without a body diode similar to the traditional Si MOSFETs. The power lost in the body diode reverse recovery (P_{rr}) can be estimated by Equation B.5 [5].

$$P_{rr} = Q_{rr} \cdot V_{DS} \cdot f_{sw} \tag{B.5}$$

External to the switching devices, the inductor's low frequency copper loss contributes to the overall losses of the output stage and is proportional to the output power. As the current load increases (I_{RMS}), the losses within the inductor also increase. The 56 µH ABRACON inductor has a copper resistance (R) of 26 mΩ and the associated losses can be calculated with Equation (B.6) [5].

$$P_{cu} = I_{RMS}^2 R \tag{B.6}$$

The synchronous buck converter loss model exhibited a $< 10\,\%$ average difference from the experimental values for the cases of the EPC eGaN®-FET and Infineon OptiMOS™-3. This 10 % difference was also within tolerance of the device parameters given in their datasheets. The model for the Texas Instruments NexFET™ followed the loss trend correctly, but included an offset to the values skewing the average percent difference. This could be due to the model's linearization of what are non-linear losses. The evaluation demonstrated that the buck converter loss model can be used to predict the losses in the design phase

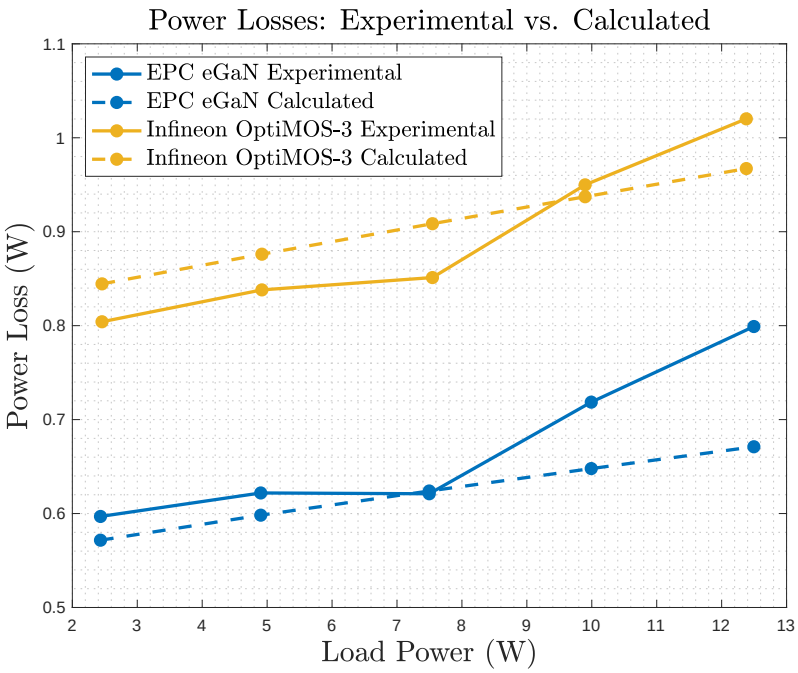


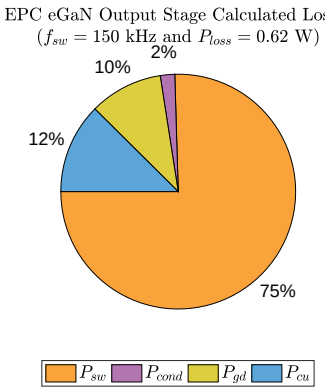
Figure B.3: Power losses, calculated versus experimental with $f_{sw} = 150\,\text{kHz}$

of a Class D audio amplifier with some success. The case of the EPC eGaN®-FET and Infineon OptiMOS™-3 are shown in Figure B.3 for the evaluated power levels with a switching frequency of $f_{sw} = 150\,\text{kHz}$. Furthermore, the predicted loss distribution of the FETs is given for the evaluation of $f_{sw} = 150\,\text{kHz}$ and $P_{load} \approx 12.5\,\text{W}$ in Figure B.4.

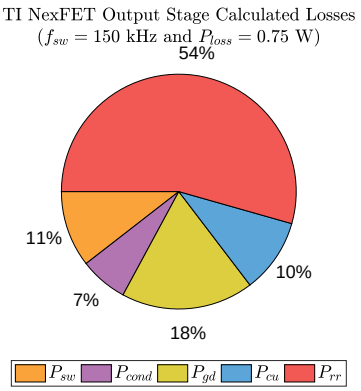
The loss measurements and calculations were further verified by monitoring the case temperature for each case. This was done by use of a FLIR thermal camera and/or with a thermocouple directly on the case (see Figure B.5). The losses could be calculated from the temperature by the Equation (B.7), where P_{tot} is the total power lost, ΔT is the change in temperature, and R_θ is the thermal resistivity of the material.

$$P_{tot} = \frac{\Delta T}{R_\theta} \tag{B.7}$$

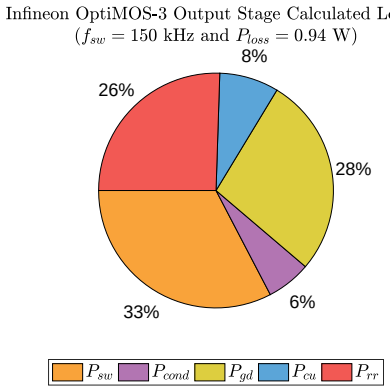
Using figures given in the datasheets for junction-to-case resistivity $R_{\theta JC}$ and junction-to-ambient resisitivity $R_{\theta JA}$, Equation (B.7) could be organized for the change in temperature from junction to case and junction to ambient. Then, two equations could be solved for



(a) EPC eGaN®-FET



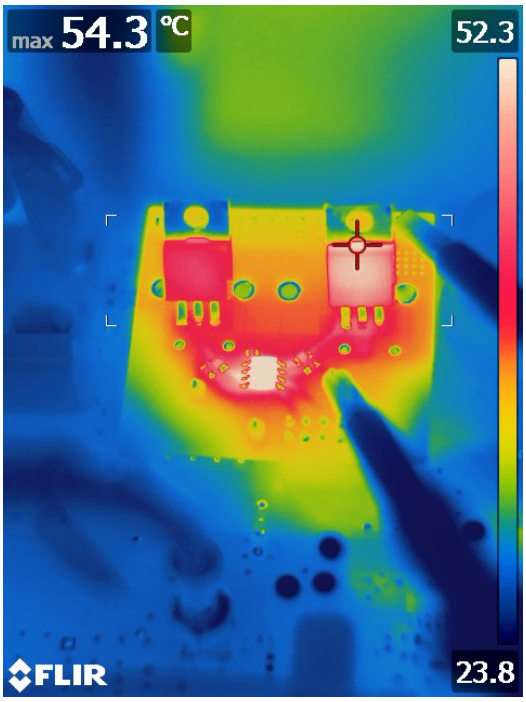
(b) Texas Instruments NexFET™



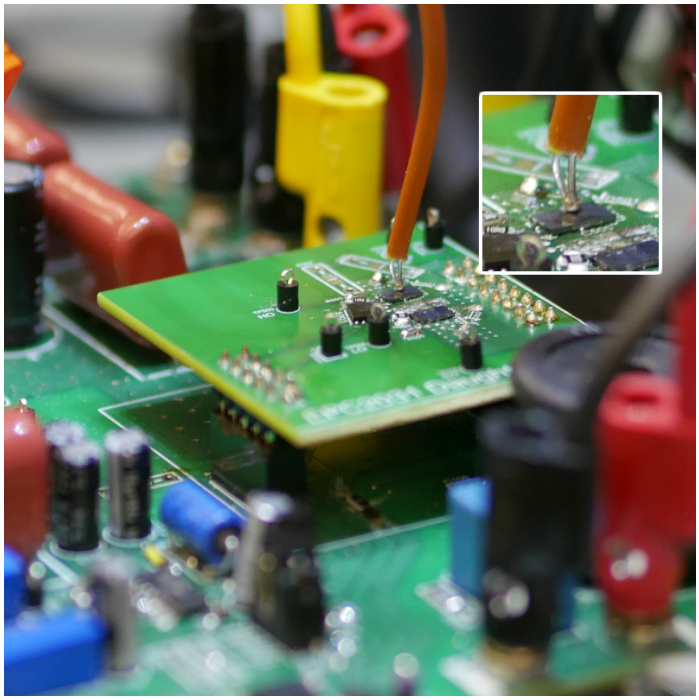
(c) Infineon OptiMOS™-3

Figure B.4: Calculated Power Losses

two unknowns yielding a power loss that was consistent with both the calculated and experimental results.



(a) Thermal image of TI NexFET™



(b) Fluke thermocouple on EPC eGaN®-FET

Figure B.5: Temperature monitoring techniques

C Closed-loop PWM-based Design

The following section describes an abandoned closed-loop design similar to the circuit shown in Figure C.1. To avoid redundancy, circuit elements similar to the experimental circuit described in Chapter 3 will be omitted. This section includes page-sized images of the PCB schematic followed by an 3-D render of the PCB. All of these images were generated in the Altium® Designer environment.

C.1 Sawtooth-Wave Generator

The sawtooth-wave generator was the centerpiece of this PWM design and designed using example circuits in the textbook by Kennedy [4]. The circuit selected was a 555-type timer IC configured to operate as an astable multivibrator. The Texas Instruments LMC555 was selected with max frequency operation of 3 MHz. Using the functional diagrams of the 555-type timer and design discussion found in the text by Kennedy [4], a sawtooth-wave generator was designed that could operate with frequency range of 250 kHz to 1.5 MHz controlled by a potentiometer [4]. The ability to sweep the frequency range of the multivibrator would

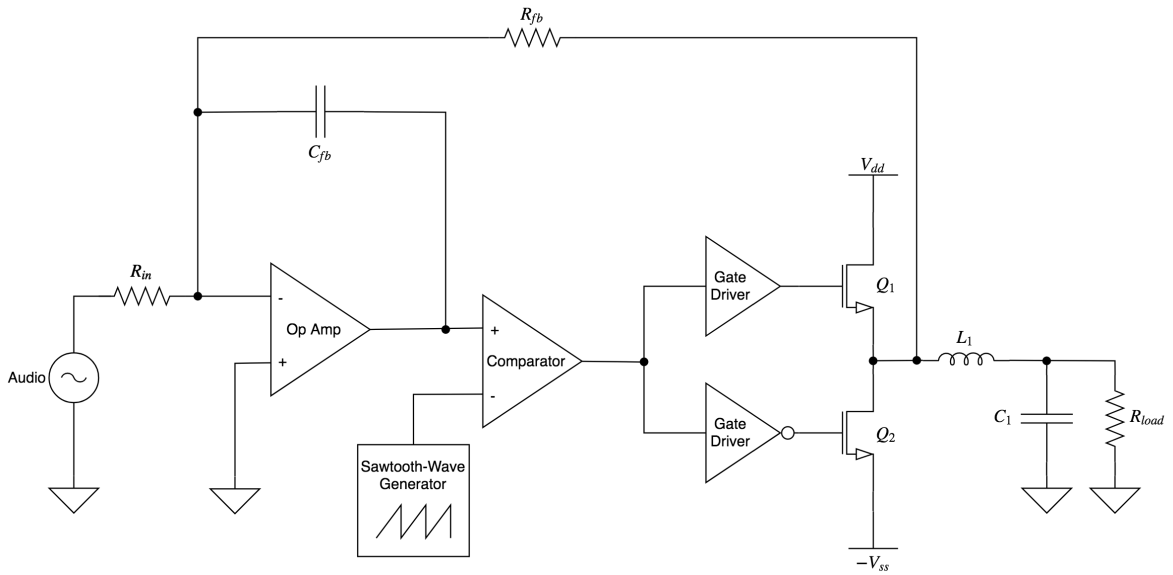


Figure C.1: Closed-loop PWM-based Class D audio amplifier functional diagram

allow the effective switching frequency of the amplifier to be optimized for the unique output stage with respect to THD+N and η.

C.2 Integrator and Feedback Calculations

The pole of the integrator in Figure C.1 can be calculated by Equation (C.1), where k is the small signal gain constant [9].

$$\omega_0 = 2\pi f_0 = \frac{k}{R_{fb}C_1} \tag{C.1}$$

The transfer function of the system can be defined by Equation (C.2) [9].

$$\frac{v_{out}}{v_{in}} = -\left(\frac{R_{fb}}{R_{in}}\right)\left(\frac{1}{1+s/\omega_0}\right) \tag{C.2}$$

C.3 Simulations

Once the values of the passive elements were determined, a circuit model was constructed within LTSpice® for simulations. Models for the Texas Instruments LM5113 GaN Gate Driver and the Efficient Power Conversion EPC2031 eGaN® FET were imported and used in this simulation. This circuit is shown in Figure C.2. The transient responses of this simulation for v_{in} and v_{out} are also shown. Figure C.3 shows the onset of clipping from a 20 Hz input sine-wave to demonstrate the simulated bandwidth of the system. Figure C.4 demonstrates the midband gain of $A_{mid(\mathrm{dB})} \approx 28\,\mathrm{dB}$ with a 10 kHz, $1\,V_{pp}$ input sine-wave. Figure C.5 shows a negligible attenuation to output amplitude as the input signal frequency is set to 30 kHz.

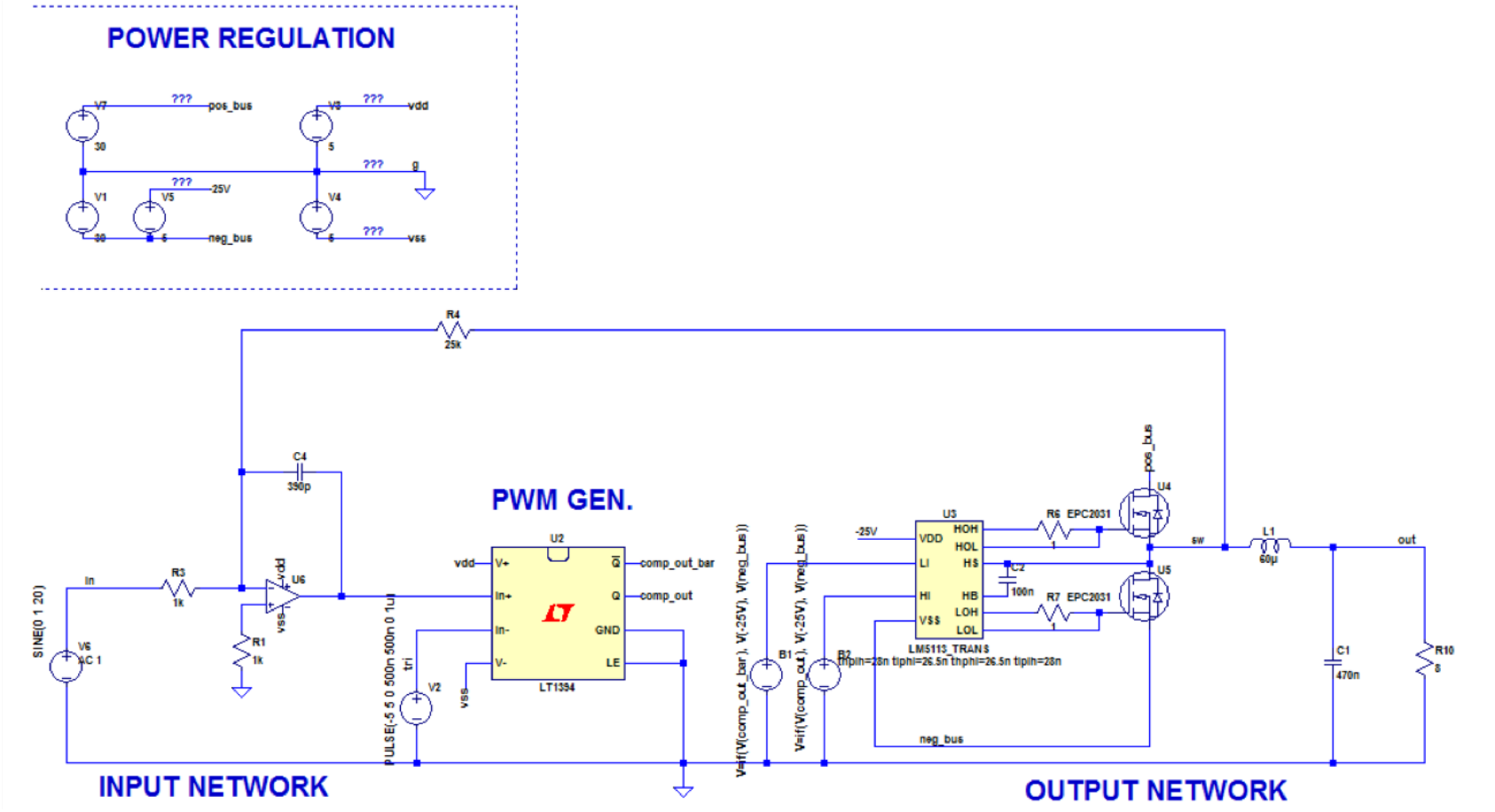


Figure C.2: LTspice® circuit model

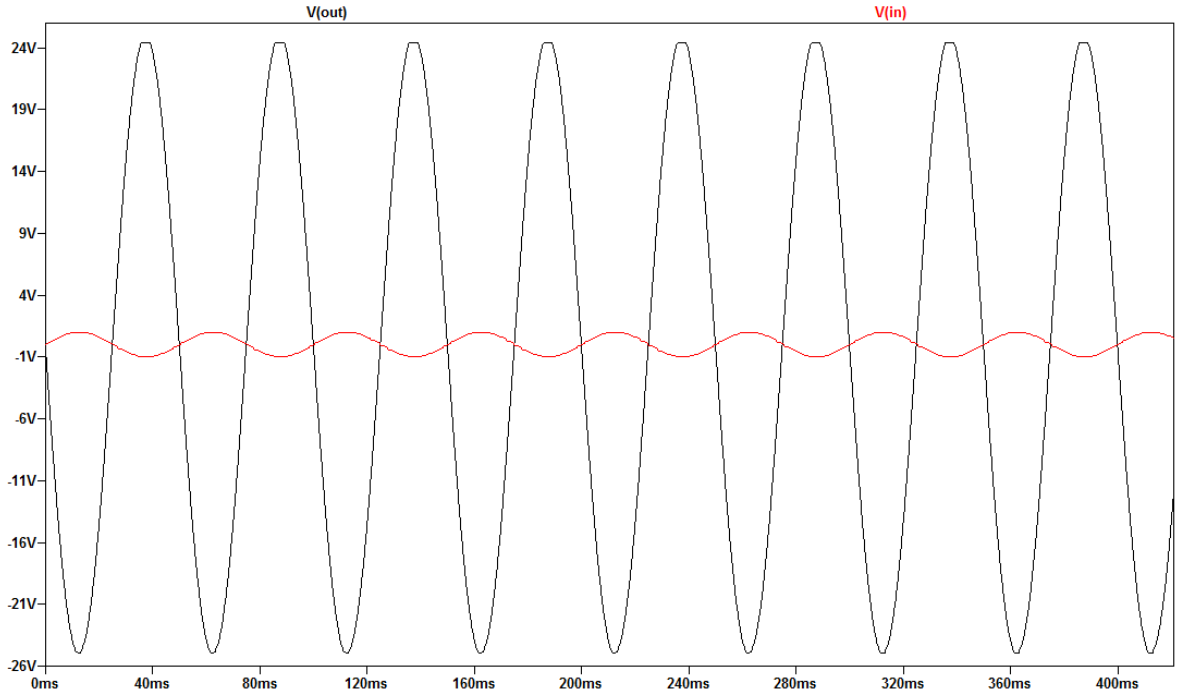


Figure C.3: LTspice® full power transient response with 20 Hz test signal

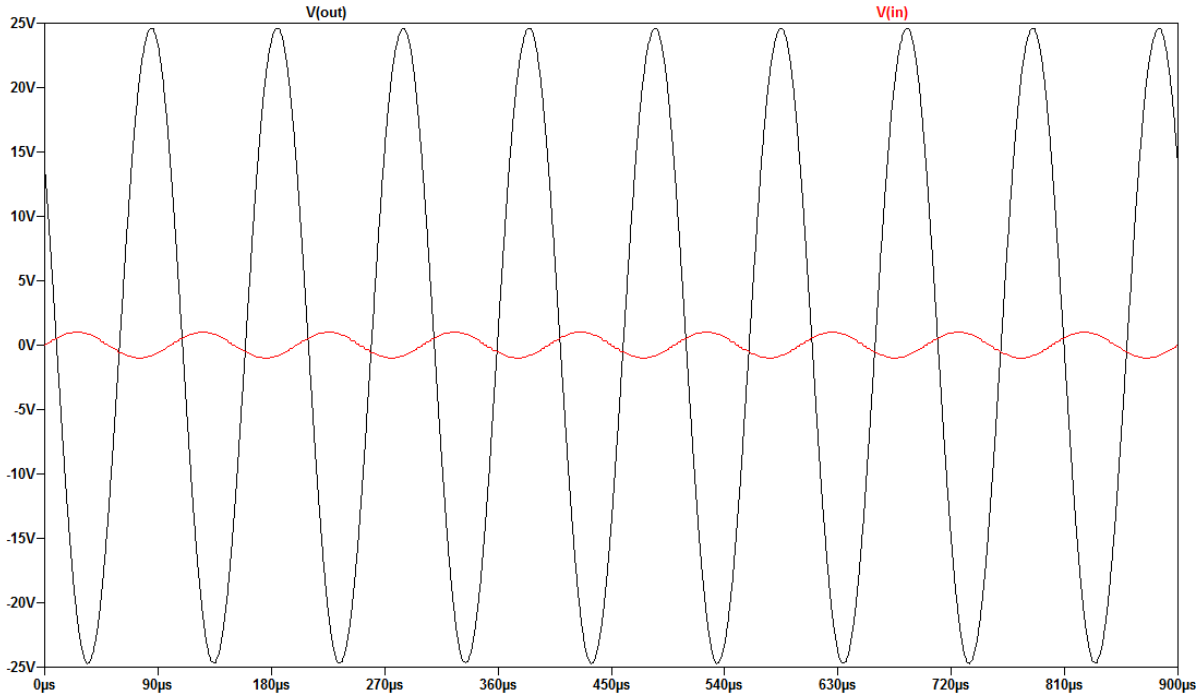


Figure C.4: LTspice® full power transient response with 10 kHz test signal

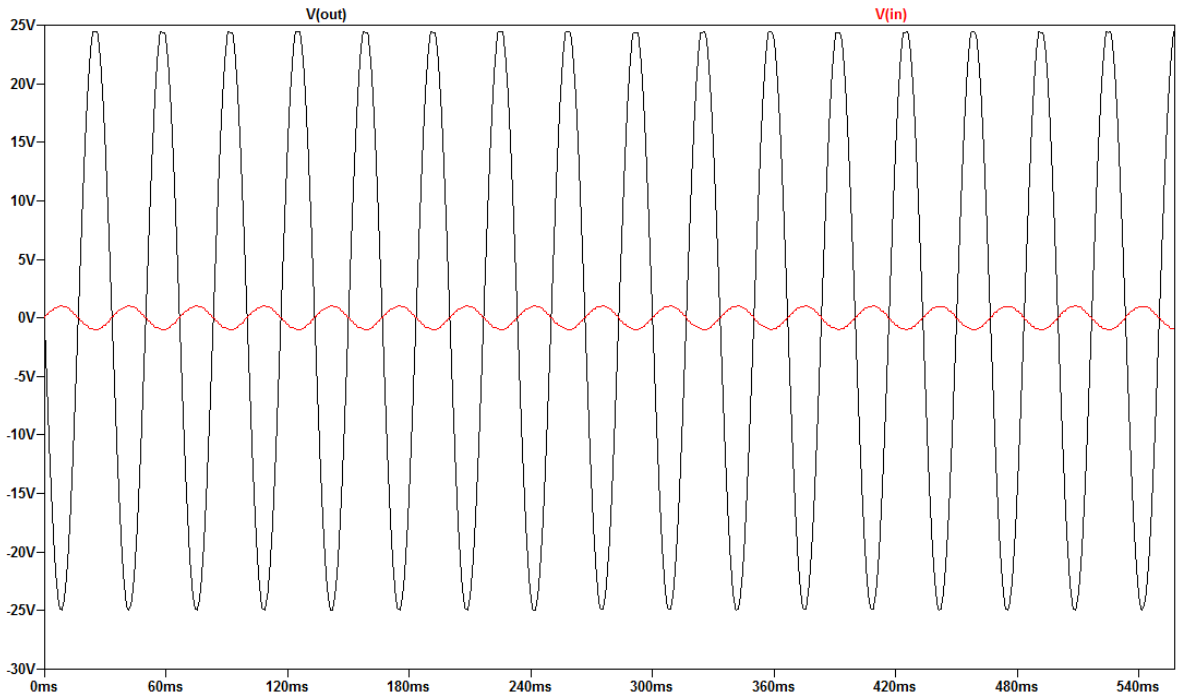


Figure C.5: LTspice® full power transient response with 30 kHz test signal

C.4 Schematic and PCB

The Altium® schematics are shown in Figures C.6 to C.12, consisting of:

1. Figure C.6 Top Level
2. Figure C.7 Power Management
3. Figure C.8 PWM Sampling
4. Figure C.9 PWM Generator Daughter Card
5. Figure C.10 Output Filters
6. Figure C.11 FET Daughter Cards
7. Figure C.12 3-D Render of PCB

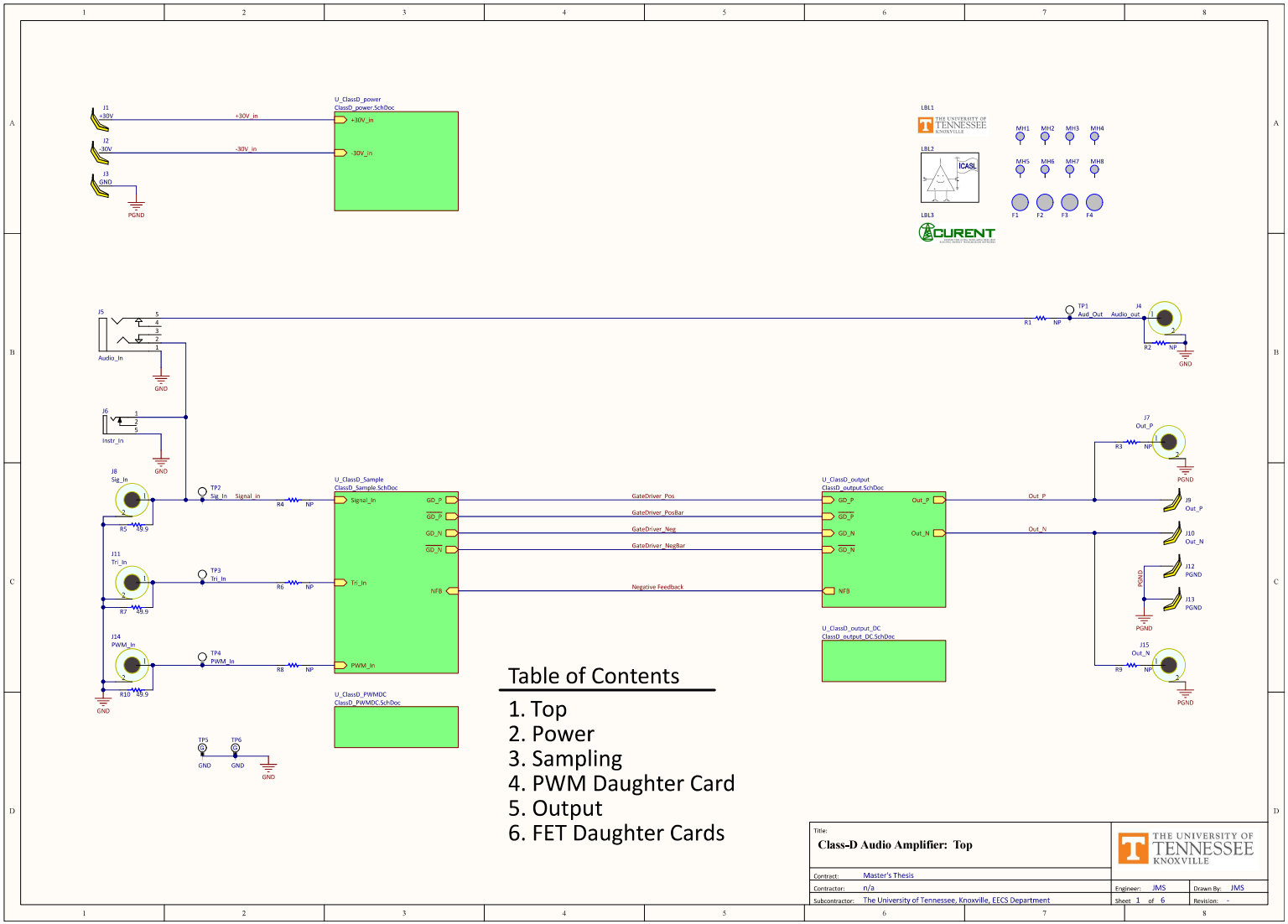


Figure C.6: Initial test board schematic page 1

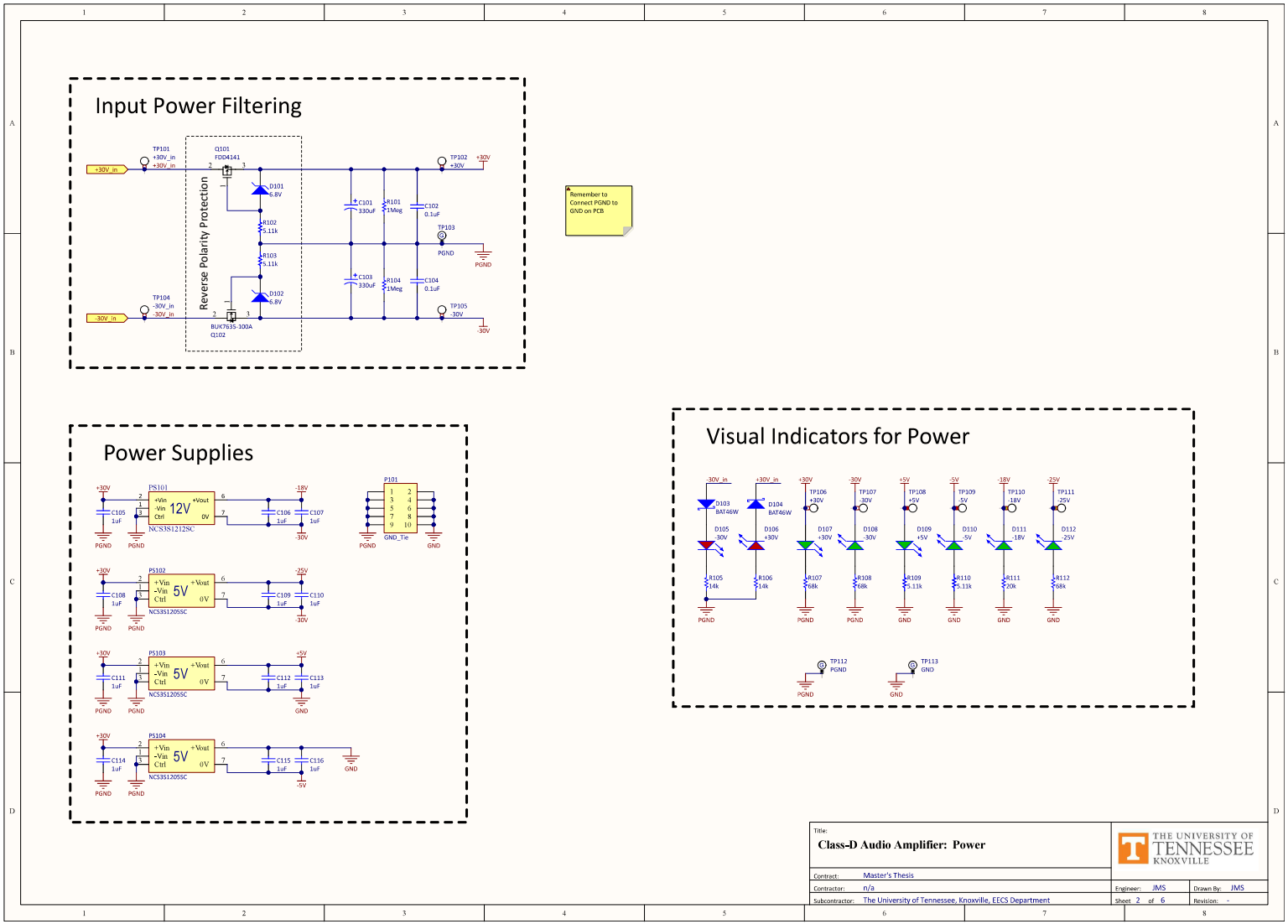


Figure C.7: Initial test board schematic page 2

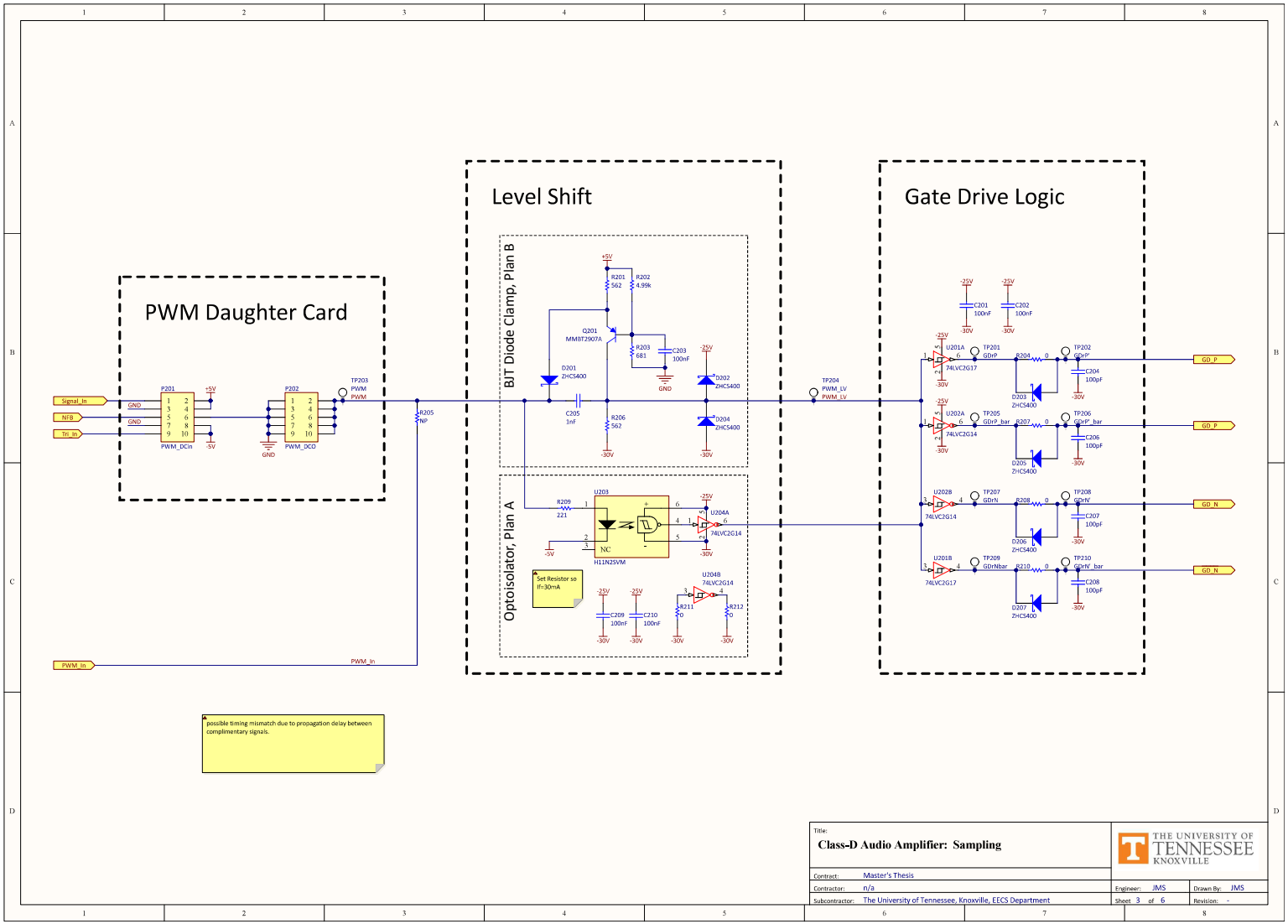


Figure C.8: Initial test board schematic page 3

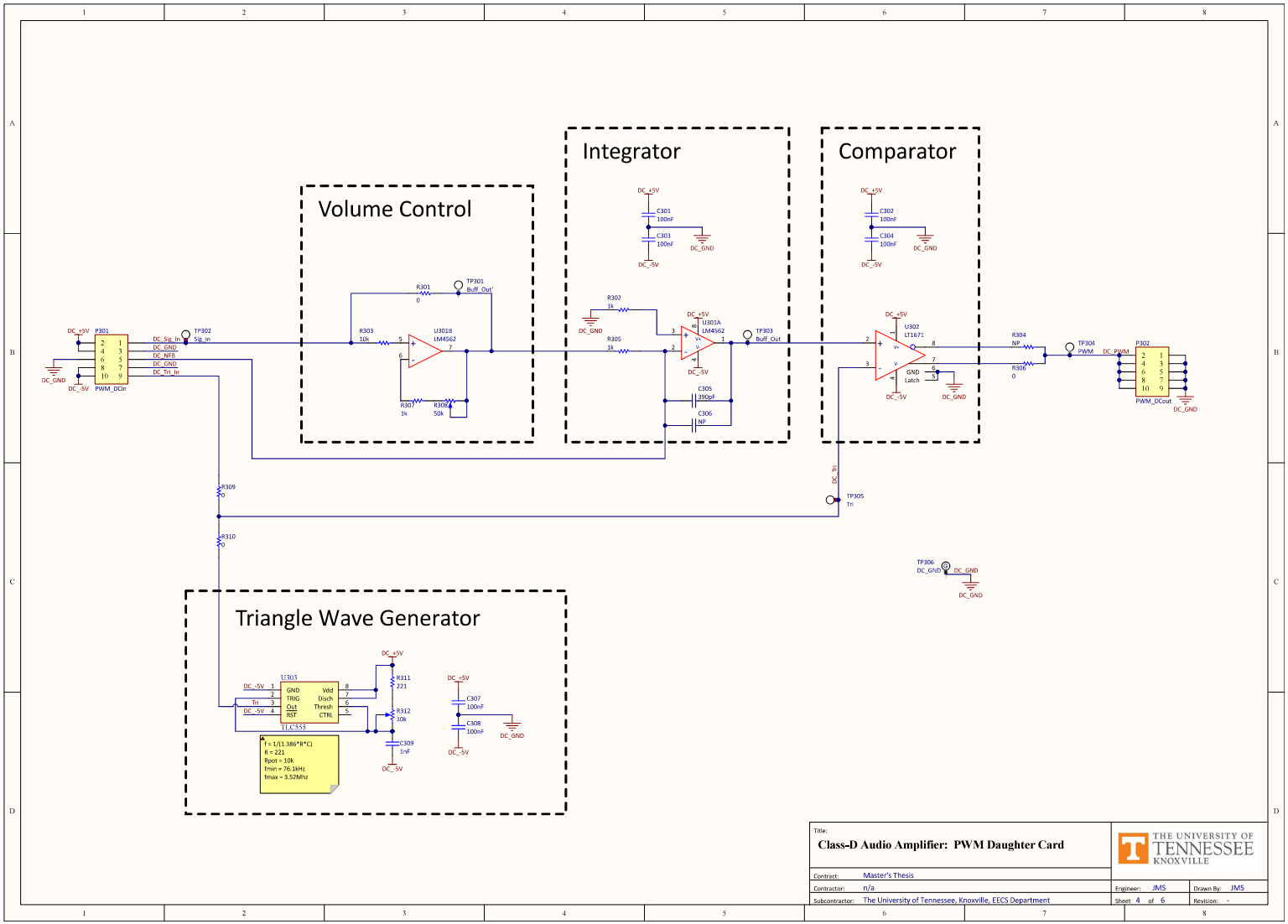


Figure C.9: Initial test board schematic page 4

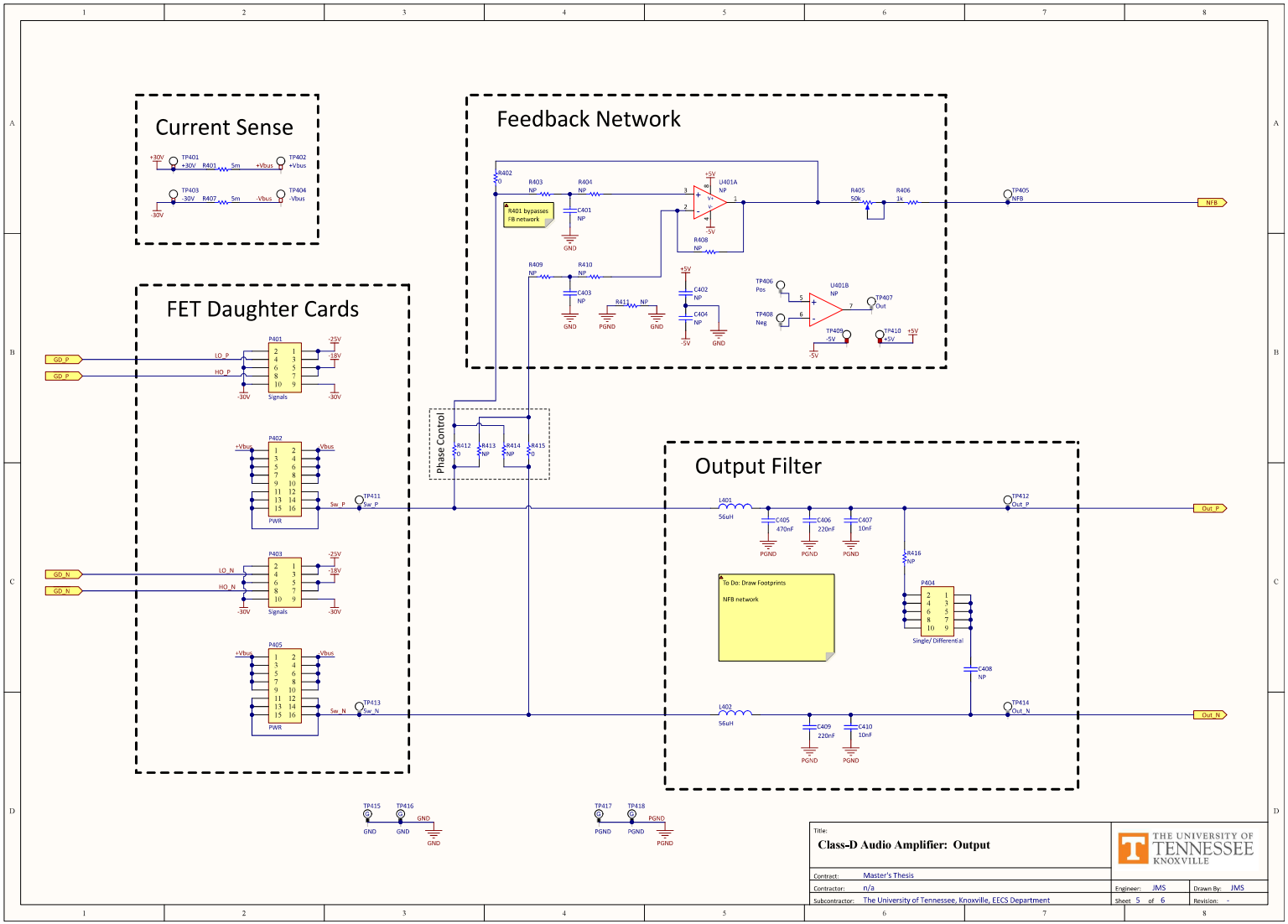


Figure C.10: Initial test board schematic page 5

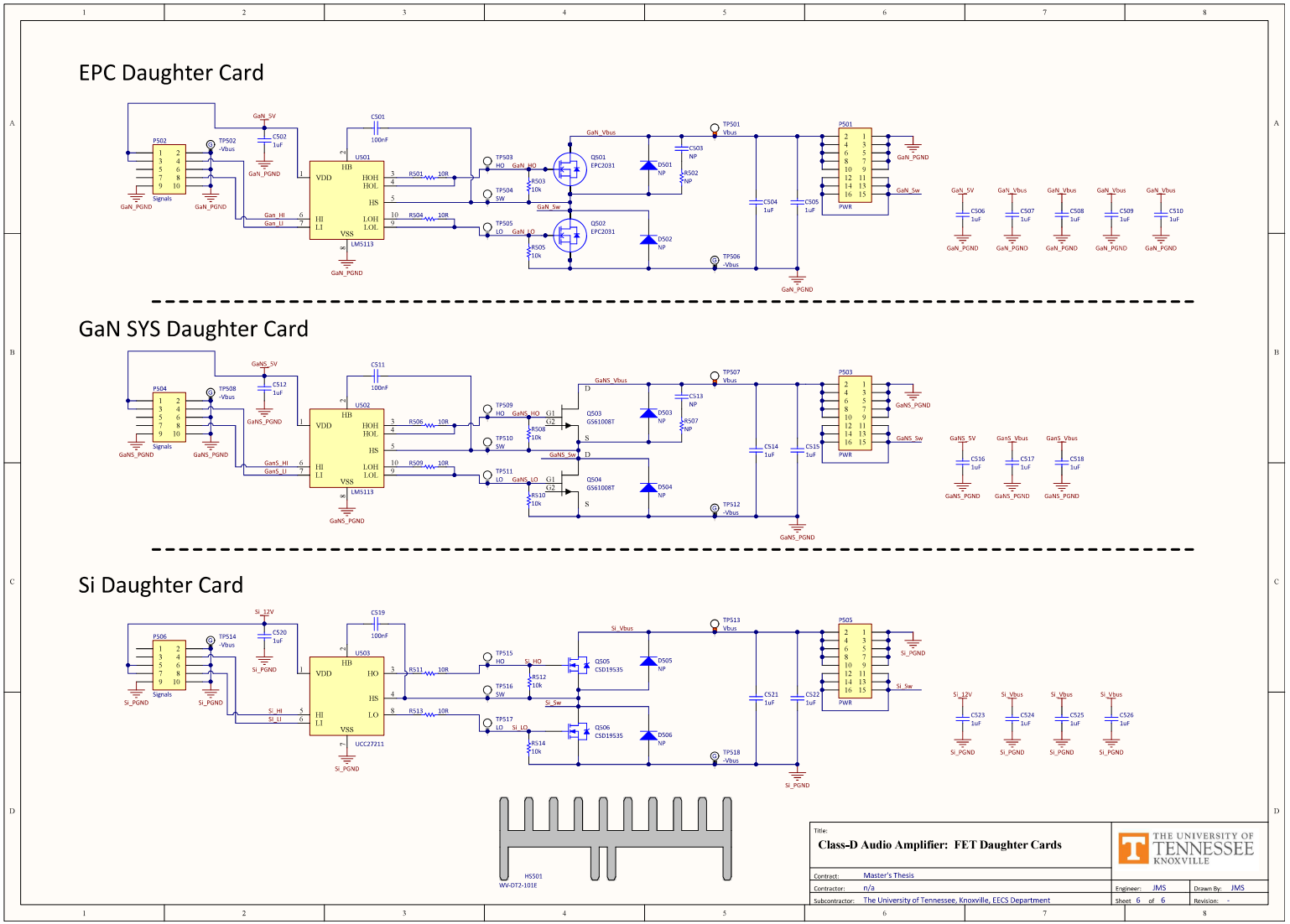


Figure C.11: Initial test board schematic page 6

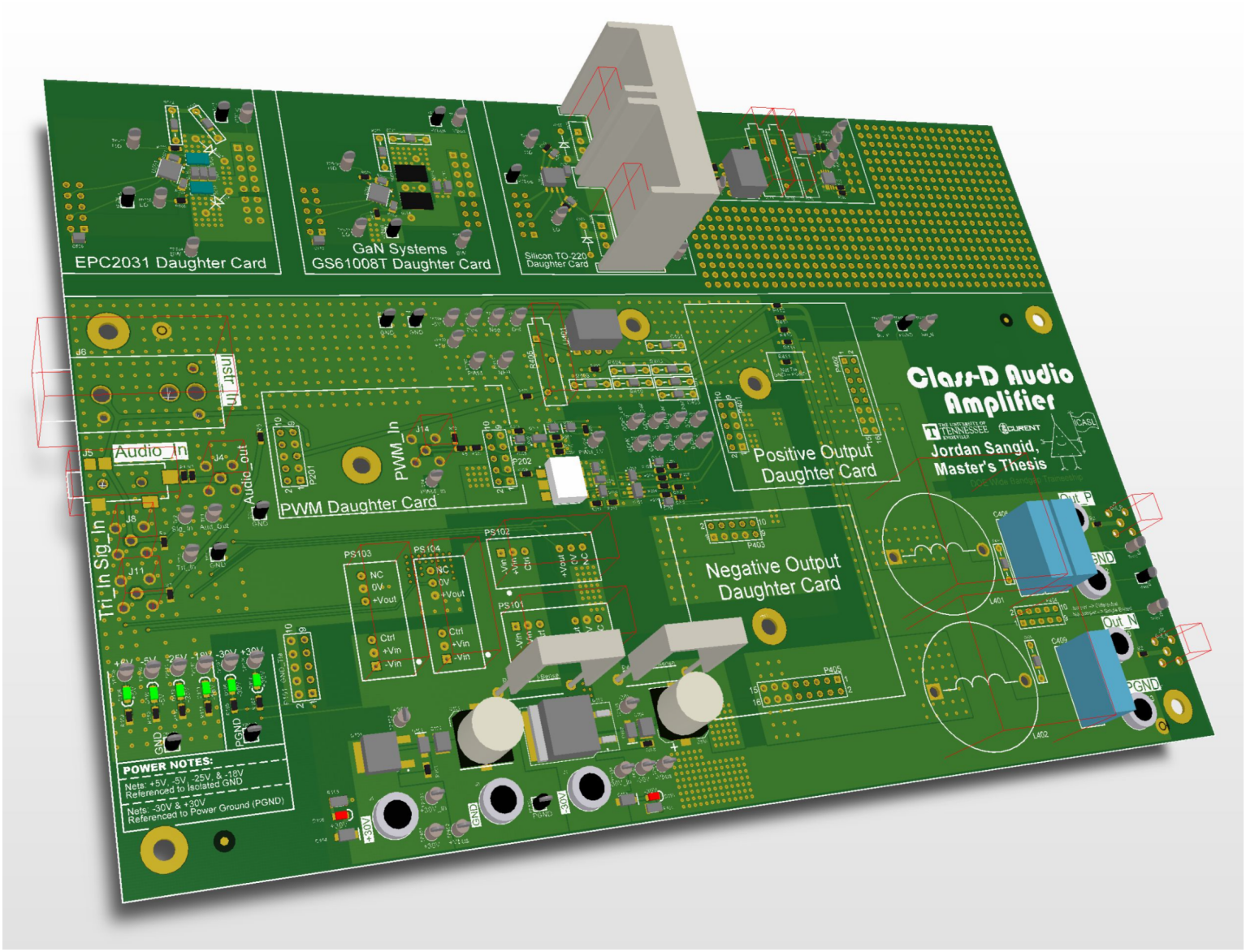


Figure C.12: 3-D rendering of initial PCB design

C.5 Experimental Results

Though this design was not ultimately used, some satisfactory waveforms were gathered. For the oscilloscope screen capture in Figure C.13 probes were attached to the test bench function generator input, the sawtooth-wave (really triangle-wave) generator, and the buffer and inverter following the low voltage level shift. This demonstrates the 555-type timer could output 3 MHz and the comparator could accurately sample the input signal of 1 kHz and 5 V_{pp} and could be seen at the lower logic level of -30 V to -25 V. Figure C.14 shows a closer look of the input and output waveforms of the level shift to buffer/inverter signal path.

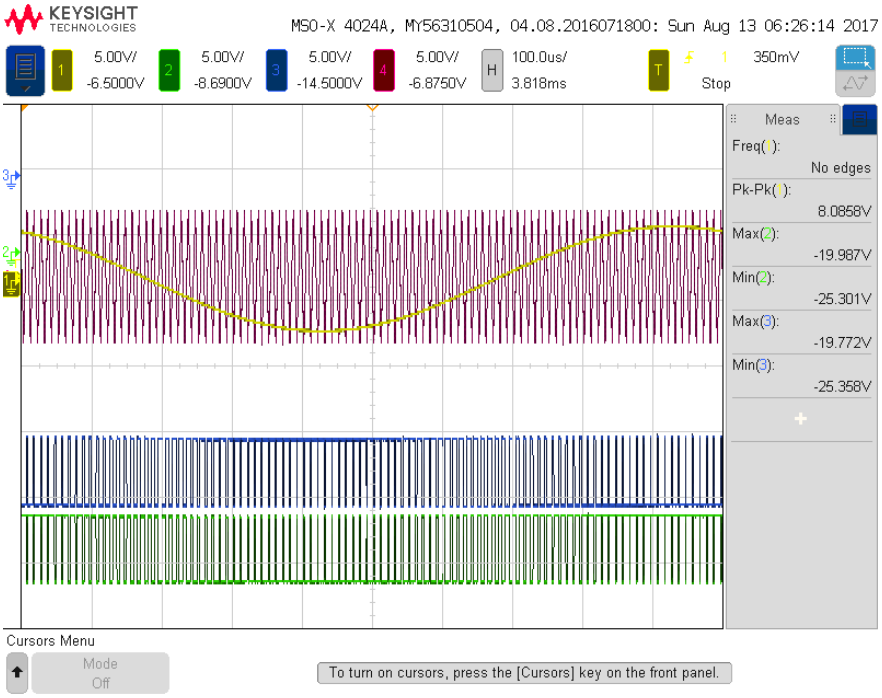


Figure C.13: Waveforms of PWM generation with 1 kHz, 10 V_{pp} input sine-wave: Input (Yellow), Triangle-wave (Magenta), Schmitt Buffer (Green), Schmitt Inverter (Blue)



Figure C.14: Waveforms of level shift and buffers with 3 MHz, 5 V_{pp} input squarewave: Input (Yellow), Level Shift (Magenta), Schmitt Buffer (Green), Schmitt Inverter (Blue)

D FPGA-centered Design

After the previous PWM design in Appendix C was abandoned, a different approach was evaluated. The goal of the FPGA centered design was to have a common controller for the audio amplifier and minimize the component count from the original PWM-based design. Since there was an extremely limited selection of Class D controller ASICs that allowed for external output FETs, an FPGA was used for this purpose.

A block diagram of the proposed circuit by Mitchell [33] is shown in Figure D.1. The chosen FPGA was the Digilent® CMOD A7™ developer board due to its low cost and the ability to fit in a 48-pin double DIP socket. The CMOD A7™ uses the Xilinx® Artix®-7 FPGA. Once the FPGA was programmed, the design was experimentally implemented on a prototype board.

One disadvantage of the CMOD A7™ board was the on-board ADC (XADC). For audio applications, typical resolution of 20-bits or greater are desired and the XADC was limited to 12-bits. Finer resolution (more bits) is needed to lower the quantization noise floor; therefore, increasing the noise ceiling of system SNR. For an ideal ADC, the SNR due to the quantization noise floor can be approximated by the empirical formula $SNR = 6.02N + 1.76\,\text{dB}$ where N is the number of bits [34]. The SNR of a 20-bit ADC can be approximated to be 122 dB, where as a 12-bit ADC SNR is 74 dB. This provided an unnecessary limit to the design prior to implementation.

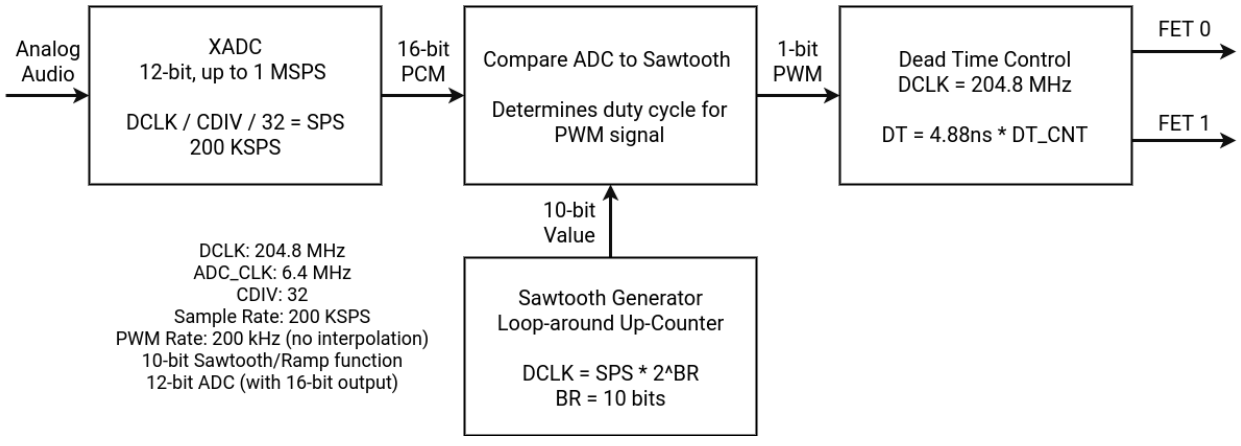


Figure D.1: Block diagram of FPGA-based design [33]

This FPGA-based design was also abandoned once a larger design challenge was discovered. In the operating condition, the developer board was held referenced to the lowest voltage potential on the board, which could be as low as $-30\,\mathrm{V}$ in the planned evaluations. This prevented the ability for quick in-circuit programming since this would also tie any computer connected via USB to the same low potential reference causing probable damage to the connected computer if the test power supplies were not properly isolated. Even though the test bench power supplies were totally isolated, this was an unneccessary precaution with a risk of damage to personal property. The FPGA-based circuit was sidelined, with lessons learned, to pursue a third and final design with a central controller.

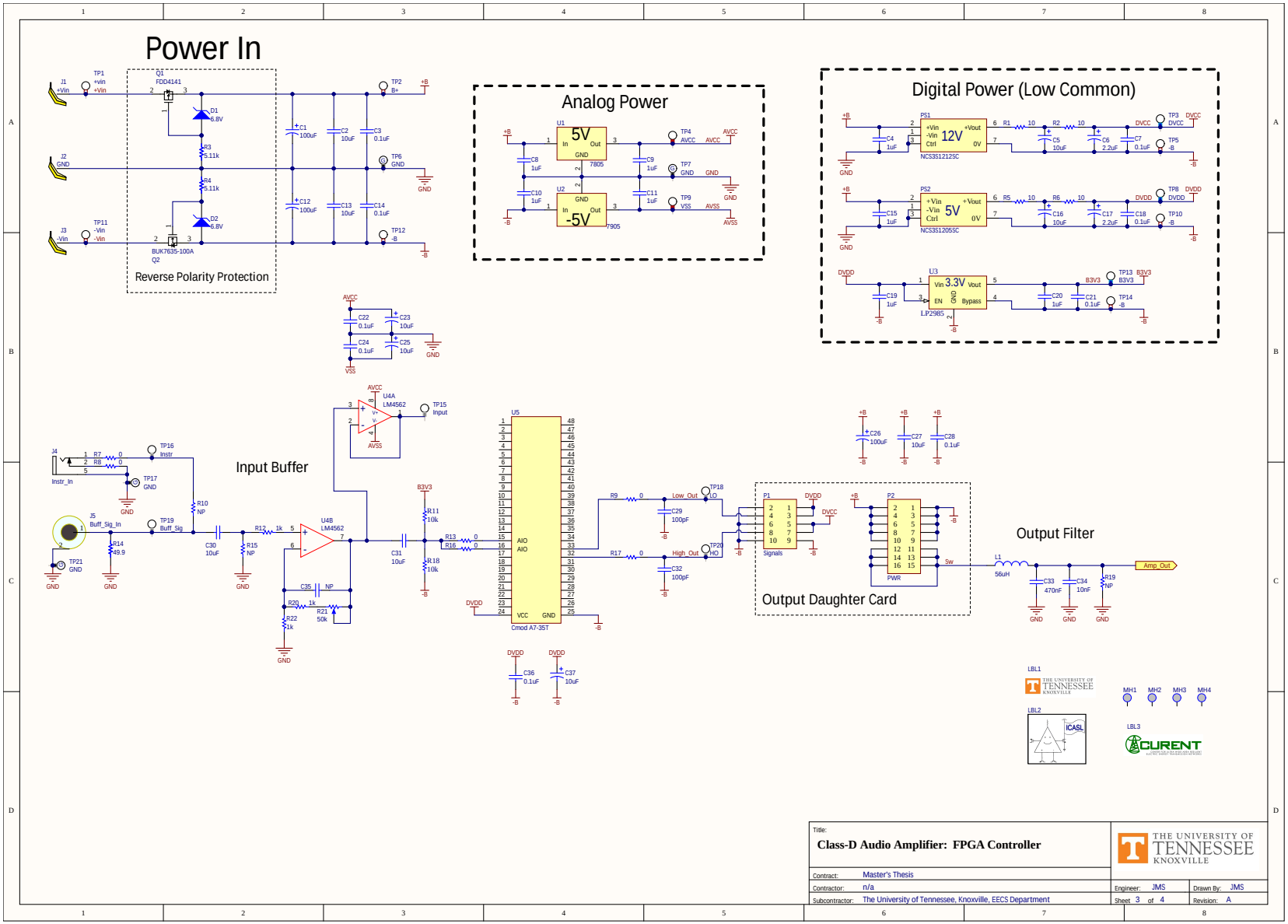


Figure D.2: FPGA-based test board schematic [33]

Vita

Jordan Michael Sangid was born in Knoxville, TN, in 1986 and graduated from Farragut High School in Farragut, TN in 2004. He earned a Bachelor's of Arts Degree from The University of Tennessee, Knoxville in 2009 majoring in History and minoring in Religious Studies. Jordan worked as a manager and live sound engineer at two Knoxville music venues before accepting an Electrical Engineering intern position at Uster Technologies, AG in 2013. During this internship, Jordan attended additional college courses leading to a Bachelor's of Science Degree from The University of Tennessee, Knoxville in 2016 majoring in Electrical Engineering. In the last semester of his 2016 Bachelor's Degree, Jordan began working with Professor Benjamin J. Blalock in the Integrated Circuits and Systems Laboratory (ICASL) research group, where he was invited to stay post graduation for a Master's Degree in Electrical Engineering under the Department of Energy Wide Bandgap Traineeship program. Using printed circuit board (PCB) design and troubleshooting experience gained from the position at Uster Technologies, Jordan held an integral role in many projects leading to a multitude of successful PCB designs (> 20) and exposure to a vast array of unique systems and technology including: SiC-based power converters, cryogenic capable power inverters for flight applications, Si and WBG device characterization, ultra-low-powered mixed-signal circuits, cryogenic capable mixed-signal circuits for flight applications, analog multilayer perceptron neural networks, as well as electroacoustics and audio amplifier design. After this thesis project, he continues to work for Dr. Blalock as a Ph.D. student.