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I am submitting herewith a thesis written by Gary To entitled "Development of the Telemetrical Intraoperative Soft Tissue Tension Monitoring System in Total Knee Replacement with MEMS and ASIC Technologies." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Biomedical Engineering.

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**Development of the Telemetrical Intraoperative Soft
Tissue Tension Monitoring System in Total Knee
Replacement (TKR) with MEMS and ASIC Technologies**

**A Thesis
Presented for the
Masters of Science Degree
The University of Tennessee, Knoxville**

**Gary To
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Dedication

This thesis is dedicated to my mother and my sister.

Acknowledgements

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Abstract

The alignment of the femoral and tibial components of the Total Knee Arthroplasty (TKA) is one of the most important factors to implant survivorship. Hence, numerous ligament balancing techniques and devices have been developed in order to accurately balance the knee intra-operatively. Spacer block, tensioner and tram adapter are instruments that allow surgeons to qualitatively balance the flexion and extension gaps during TKA. However, even with these instruments, the surgical procedure still relies on the skill and experience of the surgeon. The objective of this thesis is to develop a computerized surgical instrument that can acquire intra-operative data telemetrically for surgeons and engineers. Microcantilever is chosen to be used as the strain sensing elements. Even though many high end off-the-shelf data acquisition components and integrated circuit (IC) chips exist on the market, yet multiple components are required to process the entire array of microcantilevers and achieve the desired functions. Due to the size limitation of the off-chip components, an Application Specific Integrated Circuit (ASIC) chip is designed and fabricated. Using a spacer block as a base, sensors, a data acquisition system as well as the transmitter and antenna are embedded into it. The electronics are sealed with medical grade epoxy.

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Abbreviations and Acronyms

ADC	Analog to Digital Converter
ASIC	Application Specified Integrated Circuit
ASK	Amplitude Shift Keying
DAC	Digital to Analog Converter
DSP	Digital Signal Processing
MEMS	Microelectromechanical system
MUX	Multiplexer
MCU/ μ C	Microcontroller
RX	Receiver
TX	Transmitter
TKA	Total Knee Arthroplasty
SOC	Silicon On Chip
mm	millimeters
s	seconds
g	gravity

Chapter 1

Introduction and Previous Work

1.1 Introduction

The use of prosthetic joint implants to treat patients with severe osteoarthritis and other joint degenerative diseases began in the early 70's. The designs of the implant were primitive and the surgical procedure was not well developed. Complications such as components loosening and infection were commonly observed. Technological advancements of the past decade have had tremendous impact in improving the biomechanical performance and longevity of Total Knee Arthroplasty (TKA) with implant design, material selections and instrumentations. However, premature failure of the prosthesis remains an unsolved problem. Failure is mainly attributed to malalignment of the implant components and the ligaments imbalance, which leads to uneven loading on the polymeric component and causes wear [1]. Ligament imbalance is caused by the unequal tensions between the lateral and medical collateral ligaments (figure 1). Surgeons balance the tension of the soft tissues surrounding the knee joint by releasing attachment sites of the ligaments intra-operatively.

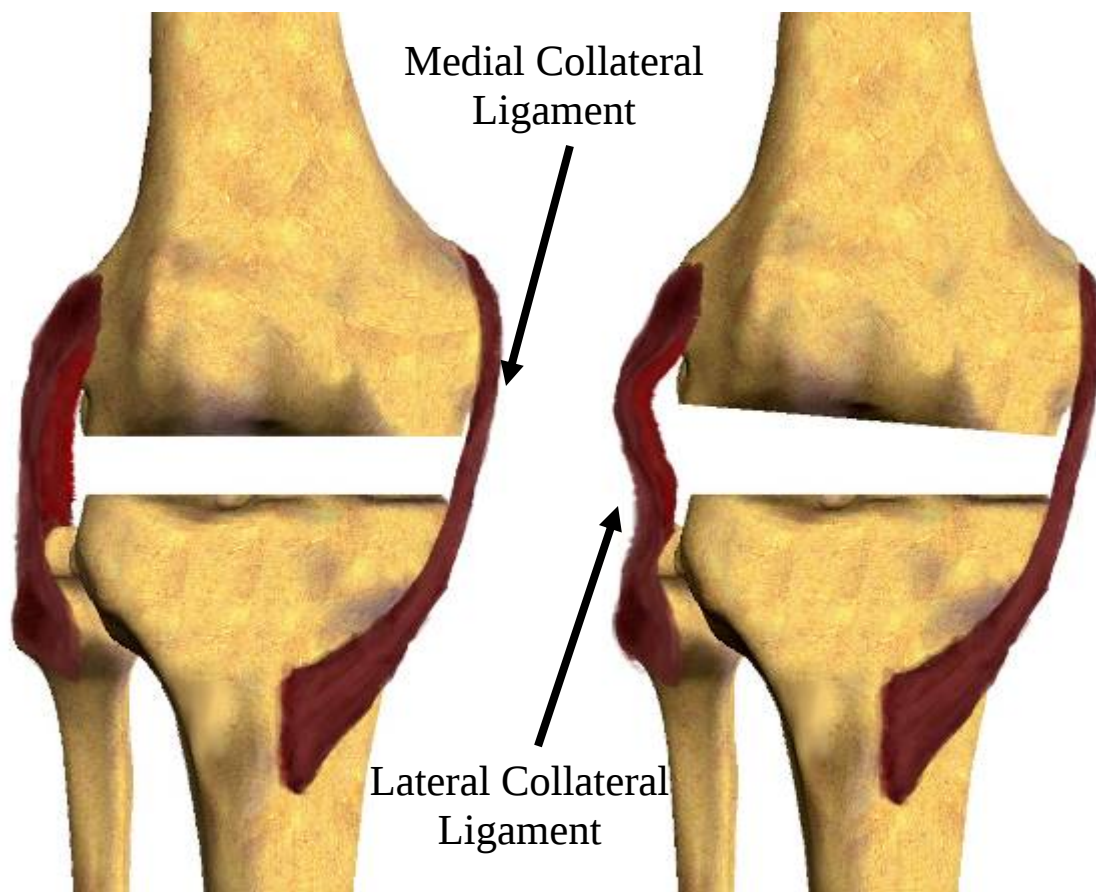


Figure 1 - The knee joint on the right shows a balance in tension between lateral collateral ligament (LCL) and medium collateral ligament (MCL). The figure on the left shows an imbalance knee joint, which the LCL is looser than the MCL.

There are numerous types of balancing techniques, which depend on the surgeons' preferences, the orthopaedic companies and the types of implant sbeing used. In general, these methods can be classified into two types, anatomical and instrumental, which will be discussed in the following paragraphs. The goal of these methods is to align the implants with the mechanical axis of the lower extremity by resecting the femur and tibia such that the gap between the two bones remains rectangular with the same gap size during extension and flexion (figure 2). In case of varus/valgus deformity, angular compensation is made for the resection.

Anatomical balancing techniques use bone landmarks to justify the resection, thus achieving the desired gap size. This method is not reliable due to the variability of the skeletal structures among patients [2]. The success rate solely depends on the surgeon's skill and experience. On the other hand, instruments have been developed in attempt to assist surgeons to perform more accurate resections [3,4]. Various instruments such as the spacer block, tensioner and tram adapter (figure 3) were experimented and used in surgeries. These instruments provide valuable information about the gap shape and size during the bone resection process. Although there is no existing study showing the effectiveness and potential of these instruments, it is generally favoured by surgeons as a gap assessment tool for verification of their resections.

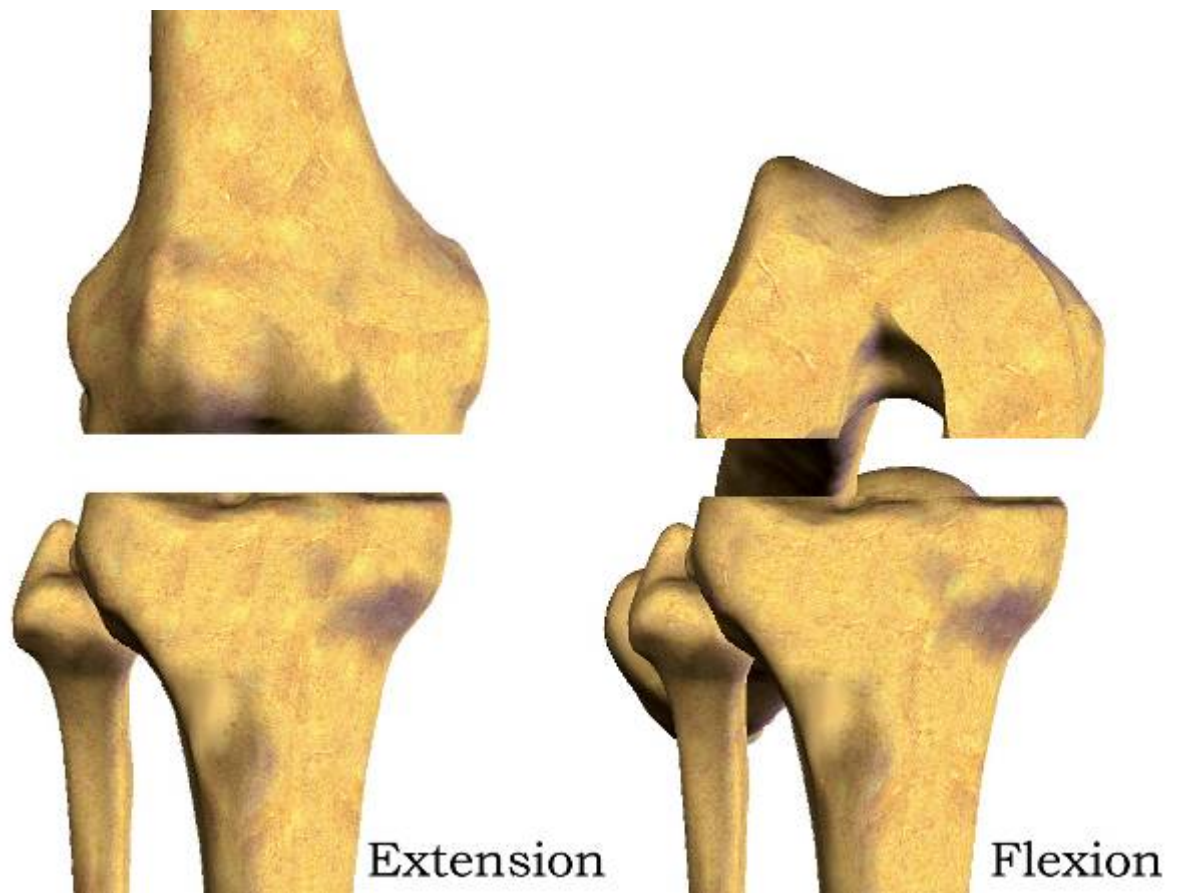


Figure 2 - This figure illustrates the ideal bone cut for the femur and tibia during a TKA surgery. The cut of the femur is parallel to the cut on the tibia during extension and 90° flexion.

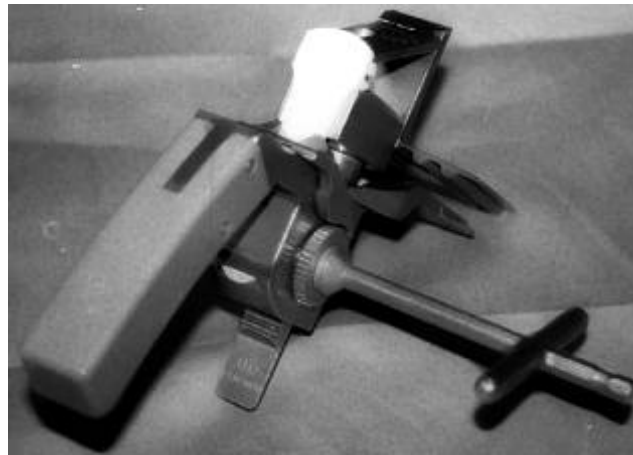
Nonetheless, the feedback from an instrument such as a spacer block and tram adapter is qualitative and the degree of tightness of the ligaments is inaccessible. Although the tensioner gives quantitative information about the medial and lateral gap, the value reflects only the tension in medial and lateral sides in general. Information such as stress distribution is not available, which can be very useful with a patient with a knee deformity. The stress distribution profile could provide suggestions and clues to what attachment sites of the ligament should be released. Additionally, the surgeons would be able to access the detail effect of the release on the flexion and extension profiles.

Despite the pros and cons of each method, it is still the surgeon's skill that determines the outcome of the surgery. Even though some surgeons can determine the gap information by touching and feeling, yet this is earned from many years of experience. The majority of the surgeons, however, have not yet acquired such knowledge. Hence, there is a demand for an intra-operative checking system that provides immediate evaluation of the resections. Additionally, this type of instrument can also serve as a learning and training tool.

Traditional incision for the TKA surgery, which is approximately 8 to 12 inches in length, can fully expose the knee. This aids the accuracy to the bone resection as the surgeons can visually determine the shape and size of the cut. Minimum Invasive Surgery (MIS) has become increasingly popular recently among patients because of cosmetic reasons and a faster healing rate.



A



B



C

Figure 3 - Examples of surgical instrument used in soft tissue balancing in TKA.
A. Spacer block; B. Tensioner; C. Tram Adapter

With MIS, the knee is partially exposed with a 3 to 4 inches incision (figure 4). Regardless of its popularity, MIS is a much complicated surgical procedure. The small incision limits the visible judgment of the resection and placement of the prostheses. In the case of a patient with varus or valgus deformity, it became very difficult to correctly align the components with such limited visibility. Furthermore, many instruments become obsolete because of the size. Hence, the principles of the intra-operative balancing system should be miniature in size and biologically inert such that it can be incorporated easily into any of the instruments depending on the surgeon's preference.

The development of a surgical instrument with quantitative feedback such as compartmental pressure can potentially minimize the errors during surgery. Eventually, this type of sensing system will be embedded into the implant itself, where researchers can easily monitor the performance of the implant. Unlike implants, the instrument is exposed to less extreme conditions and design modifications can be made easily without operating on the patient. Therefore, the research here focuses on developing a wireless intra-operative pressure monitoring system. Augmentation of a surgical instrument is an intricate process due to the limitations of material and space. As a result, the spacer block is chosen for this research as the initial prototype, because it has a relatively large volume for housing the sensors and electronics.



Figure 4 - This picture illustrates the small incision from a MIS surgery

1.2 Previous Research

1.2.1 Research in telemetry system within human body

There has been a lot of effort devoted to developing intelligent sensing medical instruments, especially in the blood pressure and gastrointestinal monitoring area. Various sensors have been developed to observe different physiological parameters. These sensors along with the electronics are usually sealed into a capsule or pill. The data is transmitted wirelessly to a personal computer after the patient swallows the pill. The first wireless monitoring system in the medical research field dated back in 1957. Jacobsen, Mackay, and Zworykin developed the Endoradiosondes (radio-pills) that are used to monitor pressure, pH and temperature for the gastro-esophageal tract [5]. In order to minimize the electronics to encapsulate, a single L-C oscillator is used as a sensor where one of the components are sensitive to the parameters to be measured. Since then, sensors, actuators and electronics have become more sophisticated, complex telemetry devices are developed for implantable drug delivery systems [6], intra-corporeal neuromuscular stimulators [7], and implantable glucose sensors for diabetics [8,9].

1.2.2 Research in orthopedics

Despite the rapid development of in vivo telemetry sensors in the biological and physiological areas, there are only a small amount of these

systems realized in the orthopedics community. There are many difficulties to overcome in implementing these systems. For instance, one of the most researched areas in orthopedics is the stress and contact area on the implant. The sensor required for these measurements is much different from those described previously. Additional, advanced signal processing is often necessary in order to get any meaningful data, therefore, microcontroller (MCU) based system architecture is generally required.

The first published research on using sensors and biotelemetry in orthopedics focuses on obtaining in vivo data from Total Hip Arthroplasty (THA) patients. Due to the large volume and geometry of the implant, it is not difficult to allocate enough space for the sensors and electronics. Bergmann embedded strain gages into the neck of the femoral component to measure strain of the patients postoperatively. The instrument is powered by inductive coil and the data is sent using a radio frequency (RF) telemetry system embedded in the shaft of the femoral component [10,11,12,13]. The data is received and processed in a personal computer. Davy and Kotzar have also developed a similar hip prosthesis to monitor various loading conditions of patients postoperatively [14,15].

While the instrumented hip is being developed to access the in vivo load of the hip joint, other researchers have begun to look into determining the load across the knee joint. The first implant that has been designed to monitor knee

joint load is in fact for distal femoral replacement. The system is similar to the instrumented hip. Bassey, Littlewood and Taylor used 4 strain gages arranged in 2 half-bridge configurations and embedded in the internal cavity of the intramedullary extension of the prosthesis, where the axial strain of the femoral component is measured [16,17,18].

In 1996, Kaufman developed the first prototype of instrumented knee prosthesis and tested in a cadaver study [19]. Recently, D'Lima and Colwell from Scripps Clinic Center for Orthopaedic Research and Education modified a tibial prosthesis from DePuy. The tibia tray is separated into upper and lower halves, where the upper portion acts as a load cell. Four supports located at the antero-medial, antero-lateral, postero-medial and postero-lateral connect the upper and the lower halves of the tibia tray. Four strain gages from Microstrain Inc. are sandwiched at the support. The electronics and the telemetry components are embedded into the stem [20,21]. This system is also powered using inductive coupling and power was transmitted using a coil worn around the leg of the subject. The data was collected via a wireless RF system.

Besides of instrumented implants, a few researchers have investigated the use of pressure sensors to monitor intra-operative pressure, and utilize the data as a feedback during surgery. In 1998, Wallace, Harris, Walsh and Bruce used Tekscan K-scan sensors to assess the tibiofemoral contact stresses intra-operatively [22]. Wasielewski, Galat and Komistek used a pressure mapping

system from Novel and attached it to the proximal surface of the tibial trials component with silicone adhesive. It was used intra-operatively for soft tissue balancing, and the results were correlated to postoperative assessment through fluoroscopic analysis [3,4]. The sensors map is connected to a data acquisition system and the force and pressure profile is shown on a computer monitor. Harris, Morberg, Bruce and Walsh investigated the two different pressure measurements techniques in vitro. The femoral and tibial components are cemented onto a saw bone, and the ultra-high-molecular-weight polyethylene (UHMWPE) is placed in between. They are then put onto a servo-hydraulic mechanical testing system. Tekscan K-scan 4000 and Fiji pressure sensitive film are positioned on top of the UHMWPE and tested with different loadings [23]. Recently, Crottet, Maeder and others have developed a force sensing device for intra-operative ligament balancing. The device consists of a sensitive plate on each condyle and a tibial base plate. Each sensitive plate has 3 deformable bridge instrumented with thick-film piezoresistive strain gages. The instrument was then tested by a surgeon in a cadaver experiment [24].

These state-of-the-art designs, however, have their limitations. The number of sensors used are often limited because of the restricted space. Increasing the number of sensors complicates the data acquisition process; results with excessive wirings causes difficulties with the implementation of telemetry system. Novel design for the data acquisition and processing system

is needed for intra-operative application in order to achieve real-time measurements.

1.2.3 Research in MEMS/IC based measuring system

The progression in microelectromechanical systems (MEMS) can potentially solve these limitations. MEMS generally refers to devices on the order of micrometers, where traditional physics does not always hold true and the coupling of different physics domains are always required. However, due to the coupling nature, they are excellent candidates for sensor devices in terms of their sensitivity and repeatability. The minimization of the sensing units allow more sensors to be packed in the same amount of space, providing more information than a single load cell. It ensures that the malfunction of one sensor will not jeopardize the entire system.

MEMS is a fabrication dependent process. There are many different types of MEMS structures; and depending on their intended applications, a custom fabrication technique is often required for them. The most common MEMS pressure sensor is the silicon based diaphragm that is used to measure gas or liquid pressure, and their fabrication methods are well documented. However, these sensors are not made for direct strain sensing [25,26]. The initial stage of strain measuring sensors research is geared towards measuring residual stress during fabrication and packaging [27]. They are designed to sense either the

change in resistance or capacitance resulting from strain within the MEMS structure. It is not popular in other applications since a strain gage is much more simple and straightforward. However, there is a growing interest in strain measuring MEMS arrays; especially in the area of tactile sensing [28,29]. Instead of having one MEMS sensor, a tactile sensor is fabricated in the fashion of an array to map the strain within an area. These tactile sensor arrays are commonly used as a grasp force control, object imaging or artificial skin for robots [30,31,32]. Xu et al. has recently fabricated a flexible tactile sensor, which he demonstrated as wrapping around cylindrical robot fingers [33]. Despite these fantastic researches, the solution to MEMS strain sensing is still not completely clear. One of the issues is that these sensors are usually embedded inside certain type of composite. While the sensor behaves differently within the composite due to the change of boundary conditions, the composite also acts as a stress shielding material. A lot of mathematical modeling on composite shear lagging can be found in literature [34,35], yet the experimental results are sometimes far from theoretical. Eaton looked into the analytical solution for large diaphragm deflection and built-in stress [36]. The author reports discrepancy between the solution and the actual experimental data, and contributes that imprecise data from the composite's young's modulus and residual stress. Besides the inherent nonlinearity and residual stress from the MEMS devices, the percentage variation of the elements in the composite and the method used

to form the composite are also factors that can affect the outcome of the sensor performance.

However, MEMS sensors can also be very difficult to calibrate. Hence, it is necessary to have controlled electronics to correct these problems. Most of the ligament balancing systems described earlier utilized surface-mounted off-the-shelf components. Off-the-shelf integrated circuits (IC) or chips offer simplified, technologically advanced components. They are usually packaged a function with multiple adjustable alternatives so as to allow the user to program the IC to their needs. Moreover, these applications often require more than one of these multi-function chips in a MCU based architecture system. With the limited working space of these implants and instruments, it is desirable to extract each of the necessary functions for the application. Even so, a vast amount of circuitry is required to realize these functions. With very large scale integration (VLSI) of the circuit, this application specified integrated circuit (ASIC) becomes achievable.

Chapter 2

Approach

The following paragraphs outline the design process of developing the instrumented spacer block. First, the design parameters and functional requirements of the instrument are examined. Based on these requirements, the basic architecture of the system is formulated. The later chapters will discuss the choice of sensors, electronics, preliminary testing and result, ASIC design and testing, and system testing.

2.1 Functional requirements

2.1.1 Stress measurement

The instrument should be able to map the medial and lateral compartmental stress distribution of the knee joint during surgery. Hence, the instrument is required to process multiple inputs from different sensors. According to previous study, the intra-operative pressure of the knee joint can range from 40 N/cm² to 150 N/cm² [3,4]. The sensors need to be able to sustain three to four times of the stress. The electronics are required to function

normally in this environment, and display no adverse effect on the readout signal from sensors.

2.1.2 Data Transmission

The sizes and equipment of an Operating Room (OR) vary among hospitals; therefore, the system should produce the least interference to the current surgical equipment and OR settings. Unnecessary wiring should be avoided so as to give more freedom, mobility and convenience to the surgeons. The data should be transmitted wirelessly from the spacer block to the base station, where the computer slices and decodes the signal and displays the stresses. The protocol for telemetry should avoid commonly used wireless bands or the cell phones' to reduce interference.

2.1.3 Bio-compatibility

The material of the instrumented spacer should remain the same as the original. However, the packaging of the sensors and the electronics should be biocompatible material approved by FDA.

2.2 System Architecture

In order to acquire a stress mapping of the joint compartment, the architecture of the sensing system has to be realized. As the goal of this

instrument is to assess the gap size and the tightness of the medial and lateral compartments, strain sensing elements are used. The system architecture is illustrated in figure 5.

An arrays strain sensing elements are used for each condyle. The system composes of several major components, which are the battery and power control, MCU, multiplexer (MUX), signal conditioning, analog to digital converter (ADC), transmitter (TX), antenna, receiver (RX), digital input/output (DI/O), digital signal processing (DSP) and Display. The battery supplies the power necessary for each component. The MCU controls the activities of all the components. MUX is essentially an analog switch that accesses the readouts from multiple sensing elements and multiplexes them into one single channel. The signal conditioning portion involves filtering high frequency noise and amplification of the signal. The ADC converts the analog signal into digital signal and submits it to the TX. The TX modulated the signal with a carrier frequency and broadcast it out through the antenna. The RX acquires and demodulates the transmitted signal. The demodulated digital signal is input into the computer through DI/O and the data is reconstructed with DSP. The details of each component will be discussed later. For the prototype of the instrument, the spacer block is chosen as the basic design because of its simple geometry and large volume (Figure 6). The choice of sensor, which will be discussed in chapter 3, is very important to the system because the electronics are built based on the signal from the sensor.

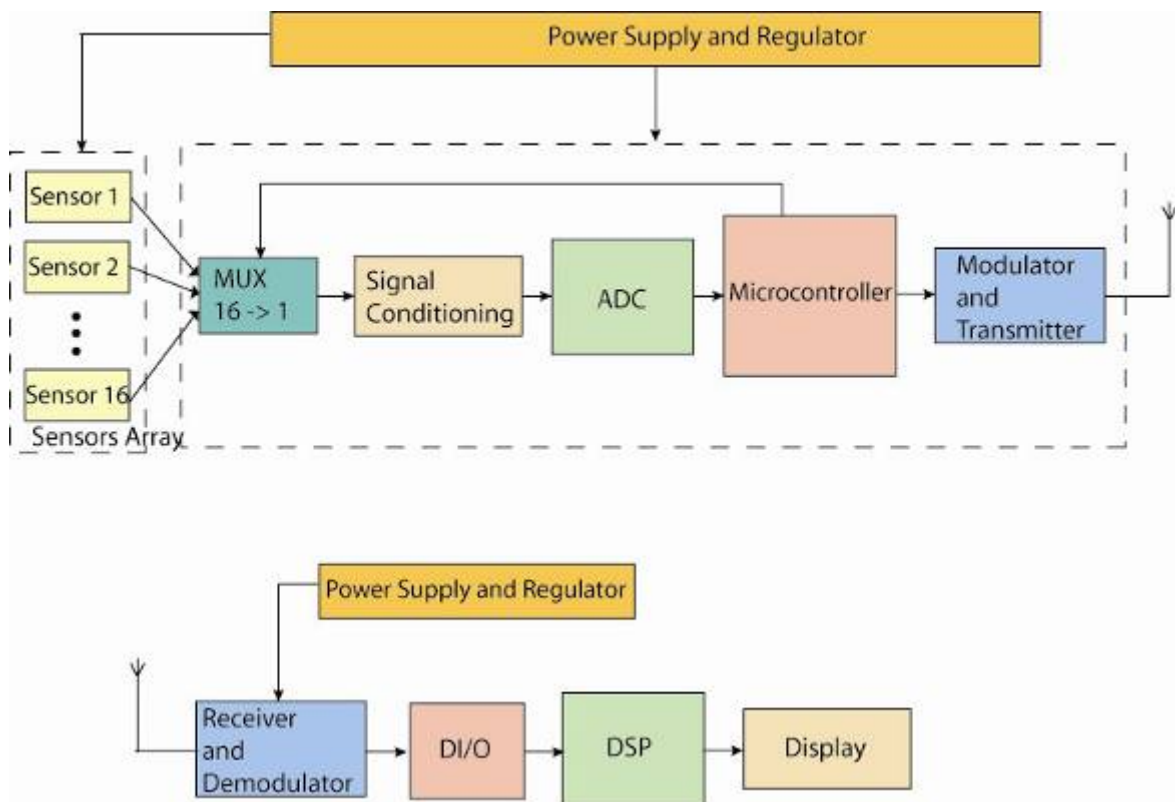


Figure 5 - System architecture of the instrumented spacer block. The top blocks demonstrate the functional components that will be placed on the spacer, while the bottom blocks represent the functions at the base station.

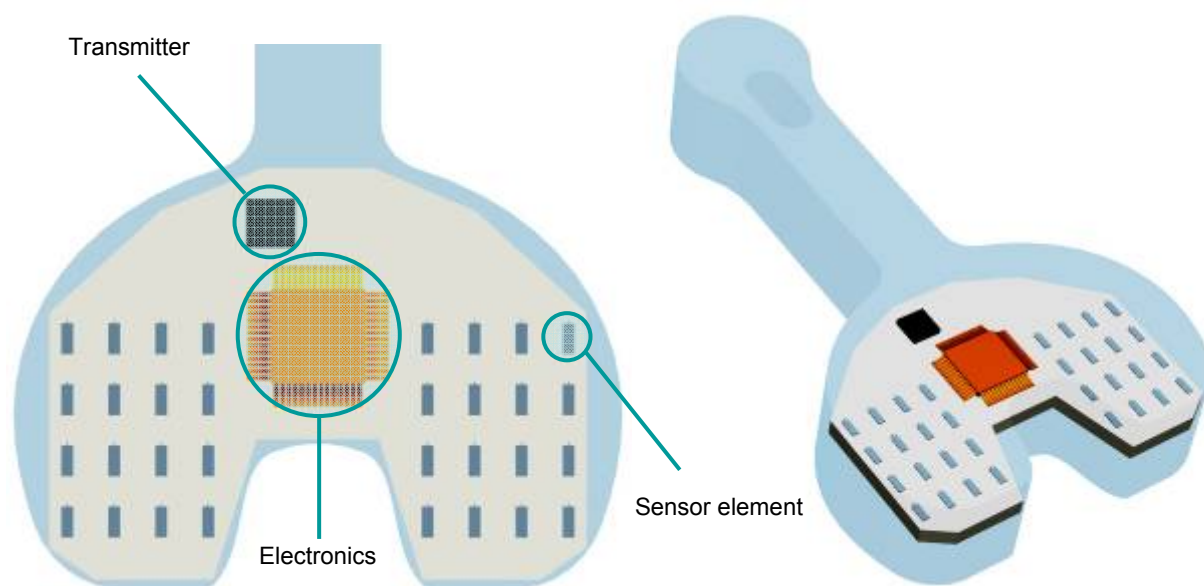


Figure 6 - Illustration of the instrumented spacer block with sensors, readout electronics and the TX

Chapter 3

Sensor Selection

Since forces and stress cannot be measured directly by any means, it is necessary to choose a measurement that can be observed and mathematically related to forces or stress. In general, mechanical forces are measured using displacements, acceleration, or electromagnetic field. Strain (ε), which is a measurement of the deformation of a body, is calculated by dividing the original length of the body (l_0) with the displacement of the deformation (δl).

$$\varepsilon = \frac{\delta l}{l_0} \quad (1)$$

It is a measurement commonly used to derive stress in a static system through Hooke's law, which states the stress is directly proportional to strain.

$$\sigma_{ij} = \sum_{kl} c_{ijkl} \bullet \varepsilon_{kl} \quad (2)$$

where σ_{ij} is the stress tensor, c_{ijkl} is the 4th order tensors of the elastic properties of the material and ε_{kl} is the strain tensor.

3.1 Strain Gauge

Therefore, sensors that are capable of measuring strain are needed in order to obtain information relating to stress. Initially, the use of strain gauges was considered because it is a well established, fairly simple and accurate sensor for strain measurement. The strain gauge is usually attached to the body of the object. An example of a typical strain gauge is shown in figure 7. As stress is applied to the body and deformed, it deforms the coils in the gauge. Due to the piezoresistive effect from the deformation of the wire coil from stress, it will lead to a change in resistance of the gauge. The resistance of a material is determined by the following governing equation 3.

$$R = \frac{\rho l}{A} \quad (3)$$

Where R is the resistance, ρ is the electrical resistivity of the material, l is the length and A is the cross sectional area. The strain and the change in resistance are related by the gauge factor (G).

$$G = \frac{\Delta R / R_u}{\varepsilon} \quad (4)$$

Where ΔR is the change in resistance from deformation and R_u is the resistance of the gauge without any deformation. The gauge factor can be considered the sensitivity of the gauge.

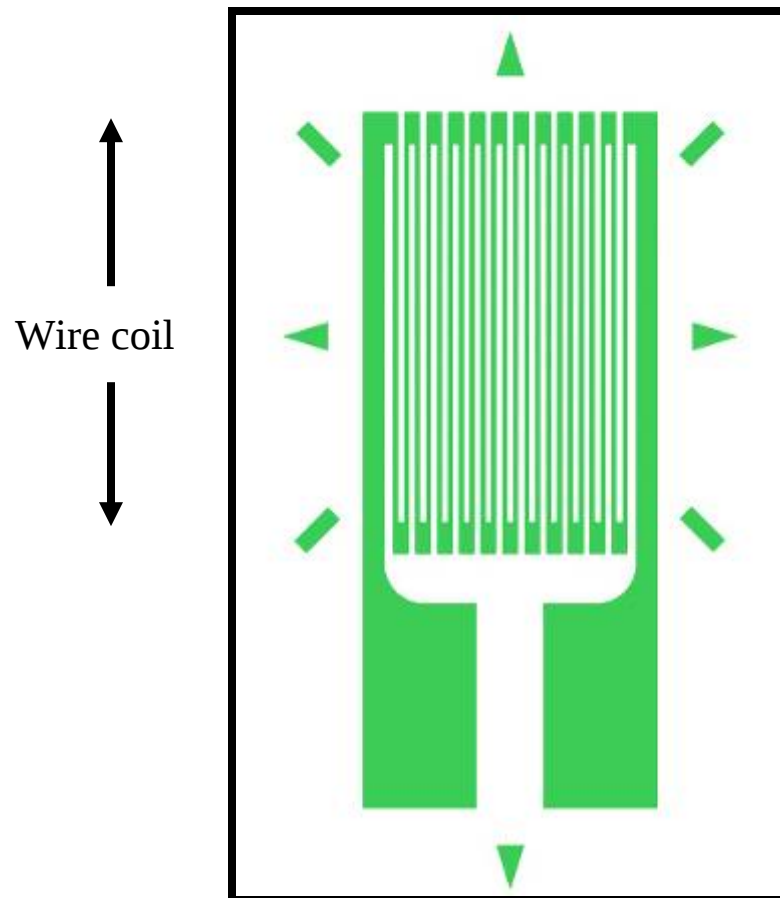


Figure 7 - Illustration of a typical strain gauge. The metallic wire coil is embedded within an insulating flexible backing.

The change in resistances can be measured with a Wheatstone bridge. An example of the circuit is shown in figure 8. Voltage is applied to V_{dd} and grounded at V_{ss} . Typically, the strain gauge is attached to one side of the leg, which will be R_4 in the figure. R_1 , R_2 and R_3 are resistors with known values such that the ratio of the leg R_1/R_4 is equal to the ratio of the other leg R_2/R_3 . In this case, the bridge is balanced, and no voltage or current will pass thru V_A and V_B . The changes in resistance from the deformation will imbalance the bridge. Thus, voltage will pass through V_A and V_B . This voltage (V_{ab}) can be calculated by the following equation.

$$(5)$$

Although the functional aspect of a strain gauge fits with the requirements stated earlier in chapter 2, there are two reasons that it cannot be used. First of all, an ordinary strain gauge is not designed to measure axial strain. Although there are a few special gauges that are designed for measuring in-plane strain, the sensor area is very large. This is not preferable with the limited working space. In order to measure the in-plane strain of the spacer block with typical gauges shown in figure 7, they will have to be adhered vertically inside the instrument. Also, the data will be inaccurate if the gauges do not align perfectly at a right angle. Additionally, this configuration makes the circuit board design extremely difficult. Secondly, in order to maintain a good gauge factor,

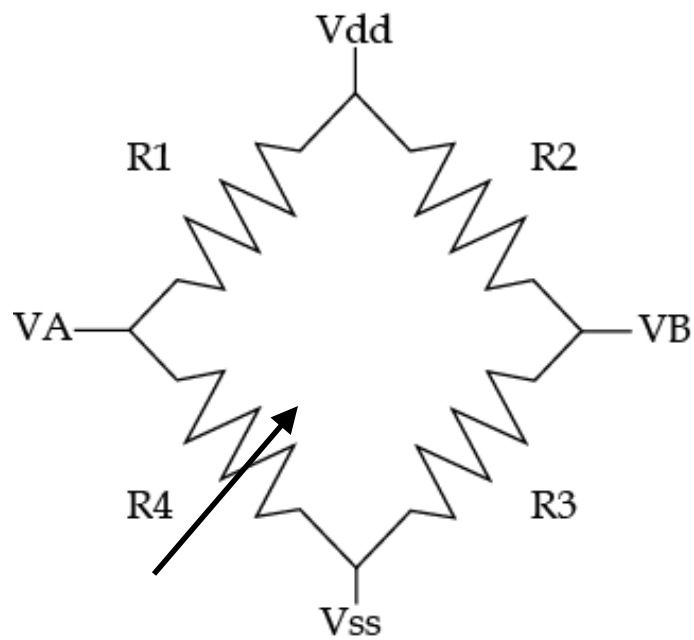


Figure 8 - Wheatstone bridge circuit. Voltage is applied to V_{dd} and grounded at V_{ss} . R_4 represents the resistance of the sensor, while R_1 , R_2 and R_3 are known. By observing the differential signal V_A and V_B , the change of R_4 can be measured.

there is a trade off between the width and length of the gauge design. It is translated to a trade off between the thickness and the number strain gauge with the configuration mentioned above. In order to pack more sensors to get the stress profile and keep the thickness to a minimum such that it can be fit into the spacer block, an alternative strain sensor is needed.

3.2 MEMS based Strain Sensor

To resolve the limited space constraint of the instrument, the use of a MEMS based strain sensor is investigated. As mentioned in chapter 1, a MEMS sensor generally couples several different physic domains together, such as mechanical and electrical. Hence, depending on the design and the intended use, mechanical strain can be measured by coupling with electrical parameters such as the change in resistance, capacitance or charge.

Piezoelectric sensors are usually made from piezoelectric ceramic or single crystal material. It generates charge when a mechanical force is applied. According to Gautschi, a piezoelectric sensor is extremely sensitive to strain and it has excellent linearity compared to capacitive or resistive based sensors [37]. However, a typical piezoelectric sensor is incapable of taking a static measurement. A constant load will generate a fixed amount of charges. There is a constant loss of electrons from the interface with electronics and reduction of the internal resistance of the sensor, resulting in an inaccurate signal. The knee

joint is in a pseudo-static condition during surgery and the strain is close to constant. Therefore, the piezoelectric sensor is not suitable for this application

The design and structure for capacitive and resistive type of MEMS strain sensor is very similar. The major difference between the two is in the readout circuitry. There are usually two conductive parts to the capacitive based sensor, where the parts are separated with a layer of dielectric material. For example, as shown in figure 9, the capacitance (C) of a parallel plate capacitor is related to the geometry of the plate and the dielectric constant of the material (ϵ_r).

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \quad (6)$$

Where ϵ_0 is the permittivity of free space, A is the surface area of the plate and d is the distance between the plate. When mechanical stress is applied to the sensor, the structure deforms, thus changing the distance between the conductive parts and the amount of dielectric material in between them. The capacitive sensor is usually excited with alternating current (AC) power. The change in capacitance is measured by determining the attenuation of the AC signal or the frequency shift in a resonant circuit.

On the other hand, the principle of the piezoresistive sensor is similar to the strain gauge discussed earlier. However, unlike strain gauges, the change in resistance is not only affected by the geometrical deformation of the metallic foil.

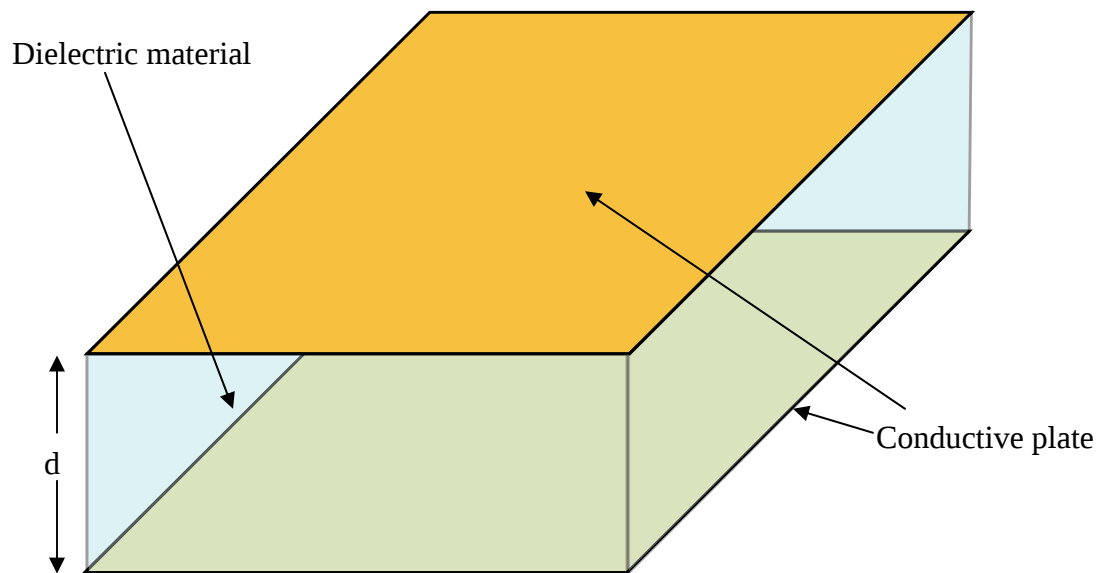


Figure 9 - Example of a parallel plate capacitor

The resistivity of piezoresistive material for MEMS such as germanium, polycrystalline silicon, amorphous silicon, silicon carbide, and single crystal silicon are also affected by the deformation. Hence, the gauge factor of MEMS strain sensor is at least 2 orders of magnitude higher than conventional strain gauges [38].

Since capacitive and piezoresistive MEMS sensors are potential candidates for this application, it is important to investigate both of them and decide the best method. In this thesis, the focus is on the piezoresistive type MEMS as the sensing element for the instrument and the implementation of its readout circuit.

As mentioned earlier, MEMS is a fabrication based process. In general, the parameter of interest dictates the design of the MEMS structure. There are quite a few of structures developed to measure strain. The most common structures for a piezoresistive sensor is the microcantilevers beam. It has been used extensively in many areas associated with physical, chemical, thermal, biological and acoustic sensing. It is also commonly used as the probes in atomic force microscopy analysis, for cell and molecule detection. Microcantilever beam is suitable for this particular application. The axial stress causes the microcantilever to deflect, hence changing the resistance of the beam. However, since the length of the microcantilever is in the micron scales, it will be broken easily through direct contact with the bone. Hence, a protective

medium is necessary to protect the microcantilever beam from collapsing by external force. Charles Hautamaki demonstrated that embedded microcantilever beam in composites can be used as strain sensors [39]. The microcantilever beam also has the advantage of flexibility, where it can be arranged into any custom mapping array. In the following paragraphs, we will look into the modeling theory and computer simulations of microcantilever.

3.3 Theory Fundamental

The behavior of a cantilever beam undergoing deflection is well documented with different scenarios of loadings and supports. However, does this still apply to the cantilever beam in the microscopic level?

The Stoney's formula is frequently used to model the microcantilever [40].

$$\sigma = \frac{EH^2}{6R(1-\nu)} \quad (7)$$

Where σ is the surface stress of the beam, E is the Young's Modulus of the microcantilever's material, H is the thickness, R is the radius of curvature of the deflation, and ν is the Poisson's ratio. Recently, there are people questioning the accuracy of the Stoney's formula and provide various improved versions of the equation. Especially in a lot of biomedical or chemical research areas, as the microcantilever has a thin film coating on top of the silicon to facilitate bonding of

molecules of interest onto the cantilever. Nonetheless, the equation shown in the following is the most common form for modeling [41].

$$\sigma_d = \frac{E_s H_s^2 \delta}{4h_d(1-\nu_d)L^2} \quad (8)$$

Where σ_d is the surface stress of the thin film, E_s is the Young modulus of the thick film, H_s is the thickness of the thick film, δ is the deflation of the beam, h_d is the thickness of the thin film, ν_d is the Poisson's ratio of the thin film and L is the length of the beam.

As for this system, Stoney's formula is not applicable because it is used to describe the relationship between cantilever free end deflection and the changes of the surface stress. An encapsulated microcantilever beam has a fully constrained boundary condition, which is different from the Stoney's formula model. Because of the small size of the microcantilever and the macro forces the cantilever measures, it is assumed that the force applied is evenly distributed across the cantilever beam. The support of the composite under the cantilever further complicates the model of the cantilever beam as the force travels through the two materials of different moduli. A free body diagram of the microcantilever beam is illustrated in figure 10. The support from the composite (S) is assumed to be non-rigid and is a function of the applied load (F).

$$S = f(F) \quad (9)$$

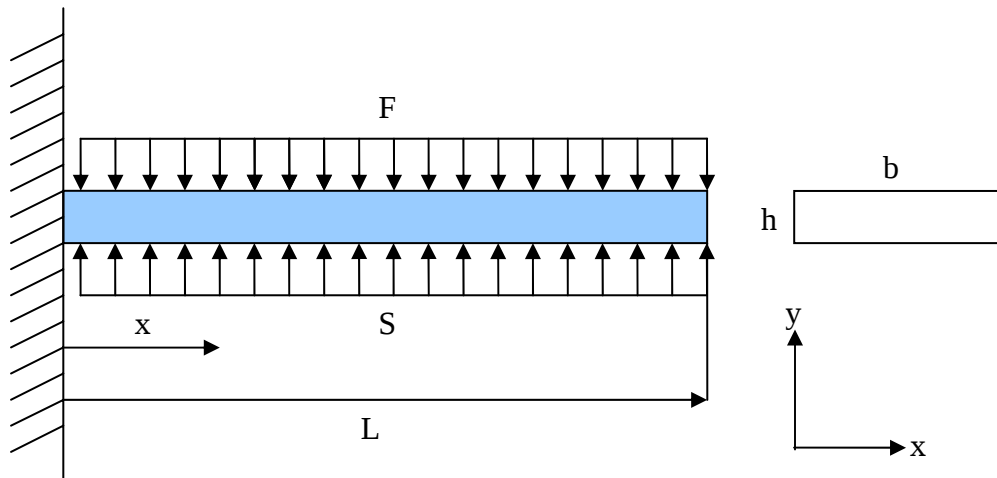


Figure 10 - Free body diagram of an encapsulated microcantilever beam

The net force (w) applied to the microcantilever should be,

$$w = F - S \quad (10)$$

Hence, the problem is reduced to a free end cantilever with even load.

Using the governing elastic beam equation,

$$0 = EI \frac{d^4 y}{dx^4} - T \frac{d^2 y}{dx^2} + \rho A \frac{d^2 y}{dt^2} \quad (11)$$

where E is the Elastic Modulus, I is the moment of inertia, T is the tension, ρ is the density of the material and A is the cross-sectional area of the beam. Assuming there is no tension in the beam and applying the following boundary conditions to the equation,

$$y(0, t) = 0$$

$$y'(0, t) = 0$$

$$y''(L, t) = 0$$

$$y'''(L, t) = 0$$

It yields the characteristic equation for deflection of the microcantilever for this particular system.

$$y = \frac{w}{24EI} (x^4 - 4L^3 x + 3L^4), \quad 0 \leq x \leq L \quad (12)$$

Where y is the deflection, L is the length of the beam. The moment of inertia for the rectangular shaped beam is defined as:

$$I = \frac{bh^3}{12} \quad (13)$$

where b is the width and h is the thickness of the beam.

As defined earlier in equation 3, the resistance of an object is related to its geometry. Substituting equation 3 into equation 12, the resistance of the deflected beam is:

$$R = \frac{2E\rho h^2 y}{w(x^4 - 4L^3x + 3L^4)}, \quad 0 \leq x \leq L \quad (14)$$

However, it is important to notice that the resistance calculated here is solely based on the mechanical aspect of the problem. As mentioned earlier, the piezoresistive effect of the semiconductor material involves the internal change of resistivity of the material when stress is applied.

The normal stress (σ) at any point of the cantilever is,

$$\sigma = \frac{w(L-x)^2}{2} \left(\frac{b/2}{I} \right) = \frac{bw(L-x)^2}{I}, \quad 0 \leq x \leq L \quad (15)$$

The change in resistivity tensor (d_i) of an isotropic piezoresistive material is related to applied stress tensor

$$\begin{pmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \\ d_5 \\ d_6 \end{pmatrix} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \begin{pmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{yx} \\ \tau_{xz} \\ \tau_{xy} \end{pmatrix} \quad (16)$$

where π_{ij} is the piezoresistive coefficient of the material.

Hence,

$$\Delta R/R_u = \pi_L \sigma_L + \pi_T \sigma_T \quad (17)$$

where π_L , π_T are the transversal and longitudinal piezoresistive coefficient of the material respectively, which are different depending on the crystal orientation of the material, and σ_L , σ_T are the stress in the corresponding directions.

The voltage drop (V) across a piezoresistive element is governed by the following equation.

$$V = R_0 I (1 + \pi_L \sigma_L + \pi_T \sigma_T) \quad (18)$$

where R_0 is the resistance of the material at stress free state, I is the applied current to the material.

Combining equation 15 and 18, yields

$$V = R_0 I \left(1 + \frac{\pi_L b w (L - x)^2}{I} \right) \quad (19)$$

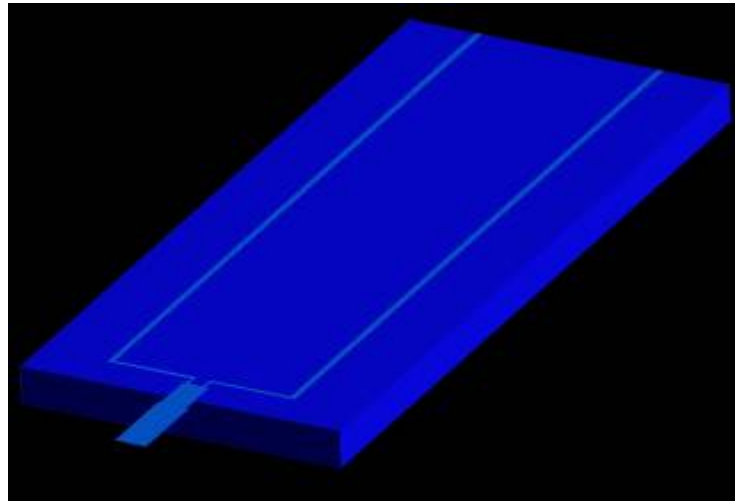
One of the major assumptions of this calculation is that the support reaction force is a function of the applied load. However, this function varies with the composite used for encapsulation. The shear lagging model mentioned in the introduction can only interpret a rough representation of this function. Moreover, the mechanical properties of the composite can also vary with the mixing and curing method, and the proportion used for each part. Computer simulation is used to attempt in examining the use of the piezoresistive microcantilever.

3.4 Finite Element Analysis

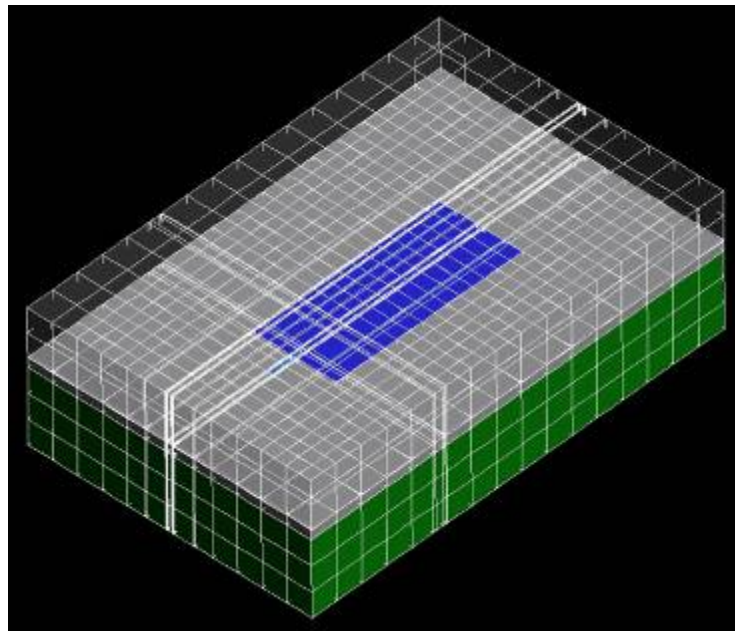
Finite element analysis (FEA) is used to investigate the amount of strain, stress and the piezo-resistive effect with different loading conditions applied on the microcantilever beam. Coventor (Coventor, Inc., Cary, NC) is a FEA simulation program that provides solvers for models in the scale of micro or nano-meters. It also allows direct coupling of solvers from different energy domains. Unlike other FEA packages, the model used for simulation here is created using standard MEMS fabrication steps, including one or more cycles of lithography, material deposition, and etching depending on the shape and the complexity of the feature. Since there is no information regarding the fabrication process of the commercially available microcantilever, a 200x50x5 microns microcantilever model is created according to the process shown in figure 11. Single crystal silicon (SCS) is used as the material for the microcantilever and it is mounted onto FR4, which is a common fiber glass material for circuit board, and embedded within a box of medical grade composite material (EP42HT2). Step 0 creates a substrate layer of FR4. Steps 2, 4, 9 and 10 simulate the encapsulated environment of the microcantilever. Steps 3, 5 through 8 are the processes to create the microcantilever with two leads for power and grounding. The mask layers are then designed, and the FEA model is created based on the processes and the masks. The cantilever model and the FEA model is meshed with a Manhattan brick element, as shown in figure 12.

Number	Step Name	Action	Layer Name	Material Name	Thickness	Mask Name	Photoresist	Etch Depth	Mask Offset	Sidewall Angle
0	Substrate	Substrate	Circuit Board	FR4	1574.8	SubstrateMask				
1	Base	Sequence								
1.1	Planar Fill	Planar Fill	Base	SILICON_100	200					
1.2	Front, Last Layer Etch	Straght Cut				Base	+	200	0	0
2	Spacer	Sequence								
2.1	Planar Deposit	Planar Fill	Spacer	EP42HT2	0					
2.2	Front, Last Layer Etch	Straght Cut				Spacer	-	200	0	0
3	Sequence	Sequence								
3.1	Planar Fill	Planar Fill	Cantilever	CRYSTALSILICON	5					
3.2	Front, By depth Etch	Straght Cut				Cantilever	+	5	0	0
4	Planar Fill	Planar Fill	Spacer2	EP42HT2	0					
5	Stack Material	Stack Material	Leadspacce	CRYSTALSILICON	2					
6	Straght Cut	Straght Cut				Leadspacce	+	2	0	0
7	Planar Fill	Planar Fill	Leadspacce	CRYSTALSILICON	0					
8	Front, Last Layer Etch	Straght Cut				Cantilever	+	2	0	0
9	Planar Fill	Planar Fill	Leadspacce	EP42HT2	0					
10	Planar Fill	Planar Fill	Spacer	EP42HT2	1000					

Figure 11 - Simulated fabrication process used by Coventor to create FEA model. The process above created a microcantilever with SCS and surrounded by medical grade composite material. The thickness of the microcantilever is 5 micron as shown in step 3.



A



B

Figure 12 - In figure A, the figure shows a simple cantilever design. In figure B shows the meshed model of the cantilever mounted on FR4 and embedded inside the composite

A distributed load is applied on the top surface of the composite and a potential difference of 3V was applied across the microcantilever. According to previous studies from Dr. Waseiewski, the ideal intra-operative compartment pressure is between 10 and 40 kPa, but it can also go up to 140kPa [3,4].

The simulated result of the von Mises stress is shown in figure 13. A query is set to retrieve the information around the microcantilever. The stress at the neck and the tip of the microcantilever are probed on the top surface and the neutral axis sections. Figure 14 shows the von Mises stress of these locations against the applied pressure from 0 to 150 kPa. Among the four locations, the neutral axis neck region of the microcantilever is the most sensitive; and it is the only region which experienced higher stress than the applied load. The response at the surface tip of the microcantilever indicates that it has the smallest von Mises stress. They indicate that the highest stress and least deflection occur at $x=0$, and vice versa at $x=L$ as shown in figure 15. The data also indicates a linear relationship between the applied stress and the stress on the microcantilever. However, this data does not describe the transient response of the microcantilever with the applied load. Drifting of the microcantilever is also not taken into consideration in this simulation. Additionally, the change of material properties results from the deformation or strain such as dislocation, also the plane slipping effect of the crystal structure is not included in this simulation.

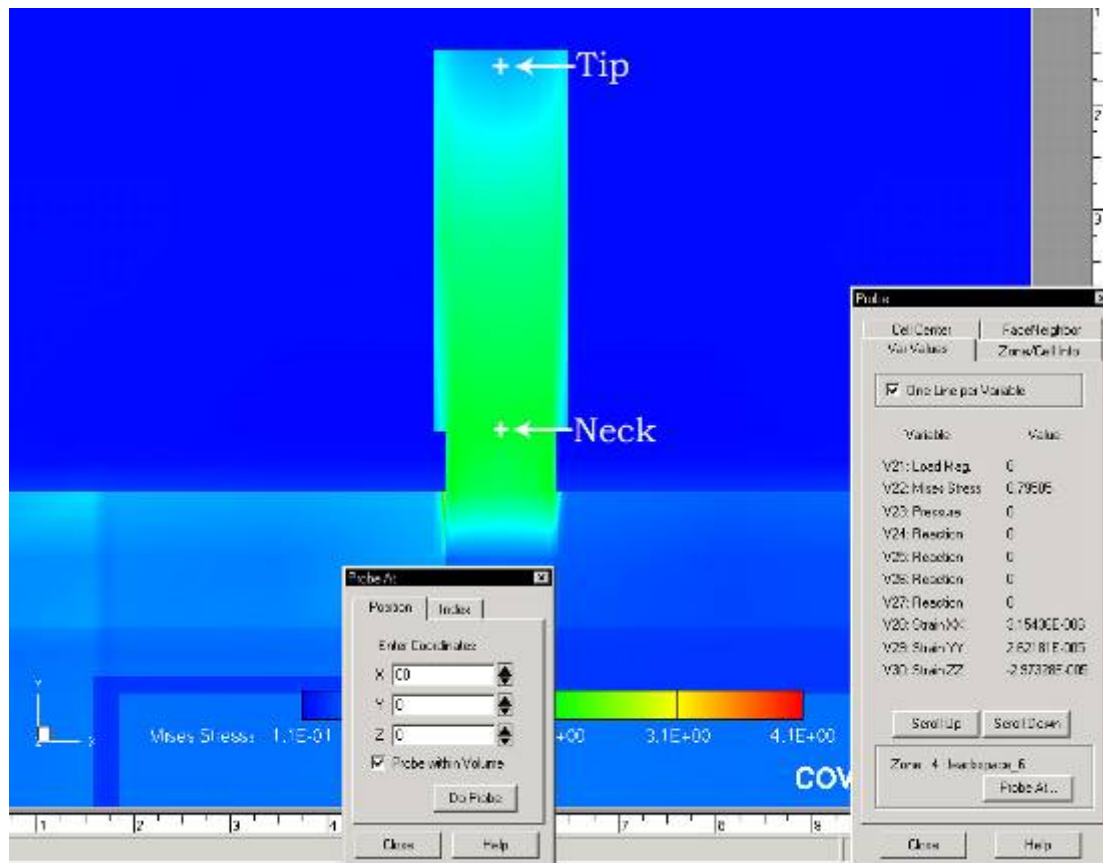


Figure 13 - Location of the probing points for the FEA

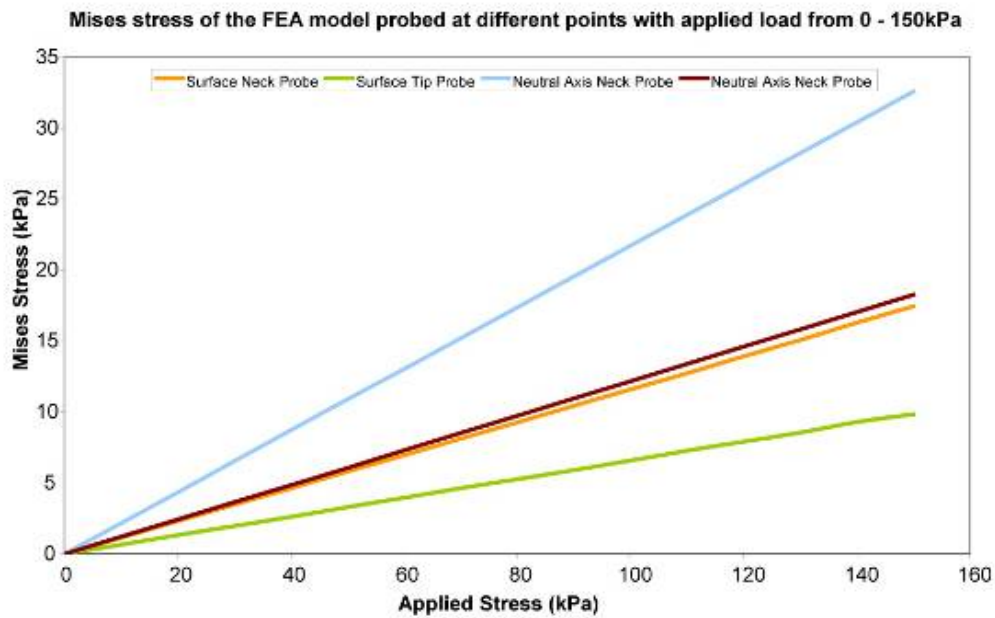


Figure 14 - Von Mises stress of FEA model

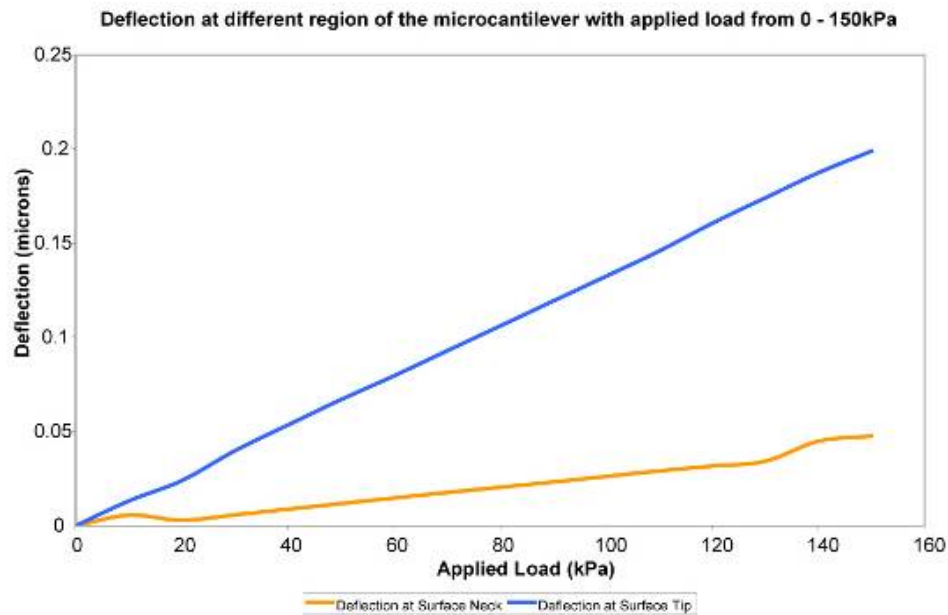


Figure 15 - Deflection measured at different regions

The result from the FEA only gave us a rough idea about the response of the microcantilever encapsulated within the composite. A lot of parameters used in the simulation, however, do not reflect the properties of the microcantilever in the real world. For example, the Young's Modulus of silicon based piezoresistive material can vary from 130 to 390 GPa [42,43]. The resistivity of the material also varies with the amount of doping. The piezoresistive coefficient of material changes depending on the orientation of the crystal structure. Hence, experimental data of the microcantilever is necessary for the electronics interface.

There are various companies that manufacture off-the-shelf piezoresistive microcantilevers. Veeco (Veeco Instrument, CA) produces a piezoresistive microcantilever with thermo compensation. However, the company terminated all production in 2004. Cation (Cation A/S, Denmark) also produces piezoresistive microcantilevers. Nonetheless, the microcantilevers are fabricated in an array 4 or 8, which reduces the flexibility of the system design. Furthermore, the microcantilevers are embedded within their chip with only a small opening. Thus, it is not suitable for macro stress measurement. There are also a few companies who are in development of their microcantilever products. Nascatec (Nascatec Technologies GmbH, Munich) produces piezoresistive microcantilevers upon request. The microcantilever has the Wheatstone bridge fabricated within the sensor itself (figure 16).

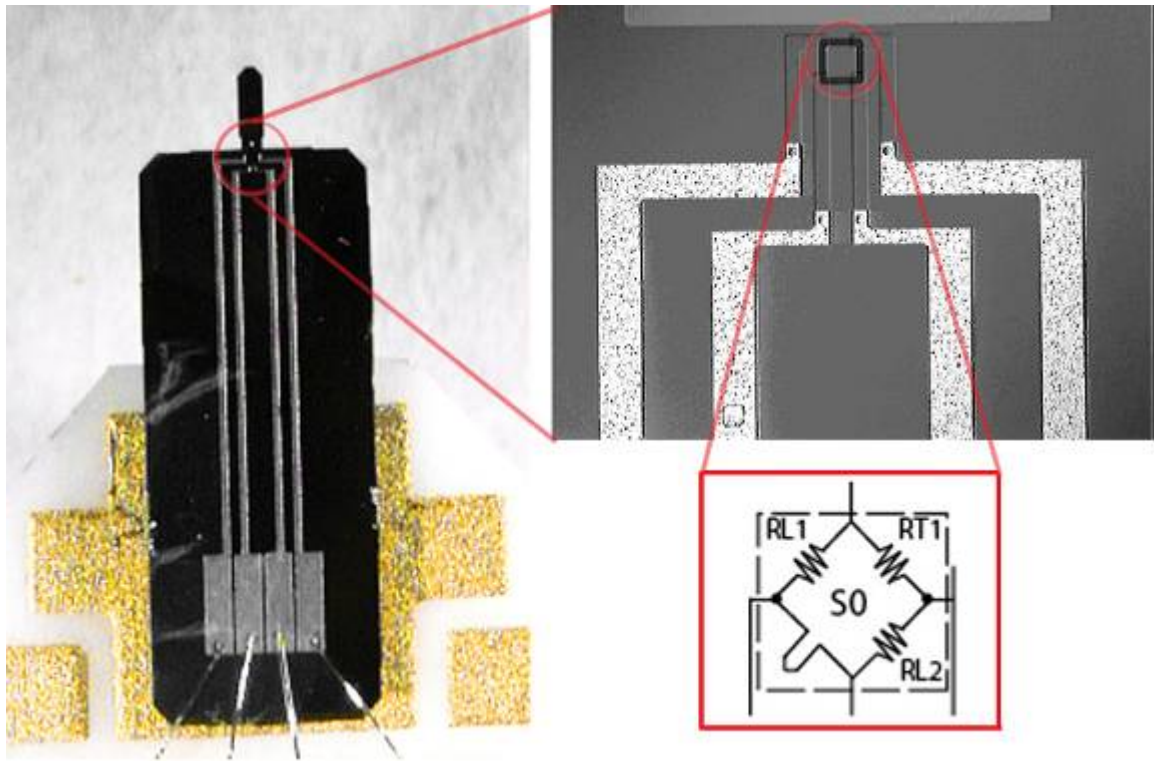


Figure 16 - Microcantilever from Nascatec, The pads assignment on the microcantilever from left to right is: Vdd, VA, Vss, VB

As seen on figure 16, there are 4 pads on the microcantilever that are connected to the 4 junctions of the bridge circuit. The 4 pads can be connected to the circuit board by wire-bonding. The pad pitch and the pad width on the microcantilever are roughly 60 and 40 microns respectively. 20 microns of aluminum wire and a wedge (4WNS4-2010-W5C-M00) are used with the wire-bonder (KNS 4523) for wire-bonding. Upon preliminary testing, it is noticed that the build-in bridge is slightly imbalanced. It could be due to improper handling of the sensors. In order to balance the bridge, an extra resistor is attached parallel to the resistor of the sensor leg (figure 17). The signal bandwidth of the microcantilever is less than 50Hz.

3.5 Composite Encapsulation

Since the microcantilever is a very fragile sensor, it is necessary to encapsulated it within some type of protective material to limit the deflection and avoid being broken by physical contact. There are several requirements for the properties of the composite material. Since the composite comes into contact with most of the sensors and electronics, it has to be electrically insulated to avoid cross talking between the components. The sensors are resistive based so heat generation is unavoidable when voltage is applied to them. The composite should have negligible thermo expanding effect in order to reduce stress on to the sensor. Additionally, the instrument comes into contact with

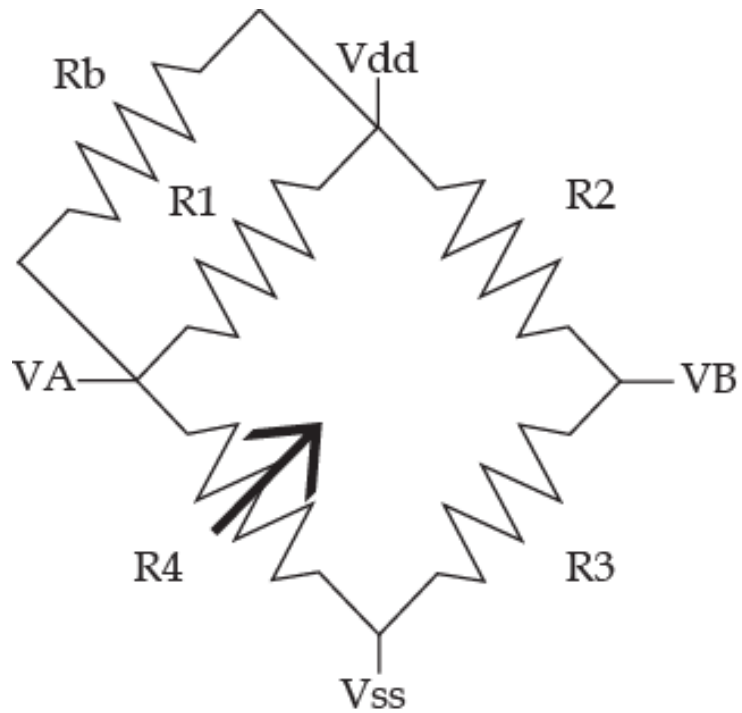


Figure 17 – Schematic for balancing built in Wheatstone bridge for Nascatec microcantilever. R_b is the balancing resistor placed parallel to R_1 in between V_{dd} and V_A

human tissues and body fluid during surgery. Thus, it has to be biocompatible. Class IV materials are those that have passed the systemic injection test, intracutaneous test, and implantation test from the Food and Drug Administration (FDA). The composite is required to be able to withstand at least one type of standard sterilization method, for instance, ethylene oxide, gamma radiation, steam, autoclave, or chemical.

Based on these parameters, it is obvious that bio-metallic composites cannot be used for encapsulation because of its conductive nature. Bio-ceramic materials are also unsuitable because they require extremely high temperature to reach the molten state. It will damage the sensors and electronics upon applying the material. Bio-polymeric materials have the potential to fit with all the criteria. Most of the polymers can be polymerized at either room temperature or a slightly elevated temperature.

Biocompatible epoxy is chosen as the encapsulation material for the microcantilever beam for the stress shielding purpose. There are multiple factors that influence the performance and properties of the epoxy. A reasonable modulus is necessary to transmit the force to the sensor; and homogeneity is essential to ensure even load distribution. Bubbles from mixing or from a curing by-product need to be eliminated above the microcantilever to ensure proper loading transfer. It is also undesirable to have bubbles underneath the microcantilever beam as they can potentially affect the amount of deflection with

the same loading condition. Residual stresses introduced by shrinkage of the encapsulating material during a heat cure were minimized so that the cantilever's sensing capability is not adversely affected.

There are four types of epoxies (EP30MED, EP21LV, EP42HT-2 and EP3HT) by Master Bond (Master Bond Inc., NJ) that are Class IV approved by the FDA. EP3HT is a one part epoxy. However, the viscosity of the epoxy is too high that it is difficult to distribute evenly across a large surface area. Hence, it was not used in any of the encapsulation experiments. The rest of them are 2 part mixed epoxy. The ratios for each epoxy for A to B are as follows: EP21LV 1:1, EP42HT-2 5:2, and EP30MED 4:1. Several batches of these epoxies were mixed to evaluate the best kind of sensor encapsulation.

The epoxies were mixed in beakers using a stir bar at room temperature for 5 minutes. It was then set on a hot plate which was heated to 60°C for 5 minutes. The elevated temperature would facilitate diffusion of air bubbles within the epoxy and rise to the surface of the mixture. The sample was stirred slowly during the heating process. The samples were then pipetted into a petri dish and allowed to cure for 3 days. The samples were observed under the microscope (figure 18). It can be seen that EP21LV and EP42HT-2 have more bubbles than EP30MED. It can be related with the mixing method. The heating increased the polymerization rate of the epoxies, thus decreasing the working time significantly.



Figure 18 - Air bubbles trapped during encapsulation (top to bottom: EP42HT-2, EP30MED. EP21LV)

EP21LV and EP42HT-2 became extremely difficult to work with since they are very viscous already. As a result, the air was trapped inside the mixture during the preparation. Additionally, due to the viscous nature and the limited working time at elevated temperature of the EP21LV and EP42HT-2, it is difficult to get a homogeneous mix of the parts. This will affect the quality of the mechanical properties of the composite.

EP30MED, on the other hand, remains relatively thin and behaves as a Newtonian liquid even with the use of the hot plate for a relatively long period of time; thus allowing more working time for the preparation of the epoxy and achieve a homogeneous mix of the epoxy.

It is obvious that the EP30MED should be used for encapsulation material because of its biocompatibility, good mechanical and electrical properties, and long preparation time.

The next test was to investigate the effect of the microcantilever after encapsulation. EP30MED was mixed according to the mixing method listed above. A microcantilever was attached to a piece of printed circuit board (PCB), which is made from fiber glass material, FR4. A well was made for the microcantilever to sit in. The resistance measurement of the microcantilever was taken. The mixed epoxy was slowly transferred from the beaker to the well. The well was designed that there will be roughly 2mm thick of epoxy above the microcantilever (figure 19). The epoxy was let to cure for one week.

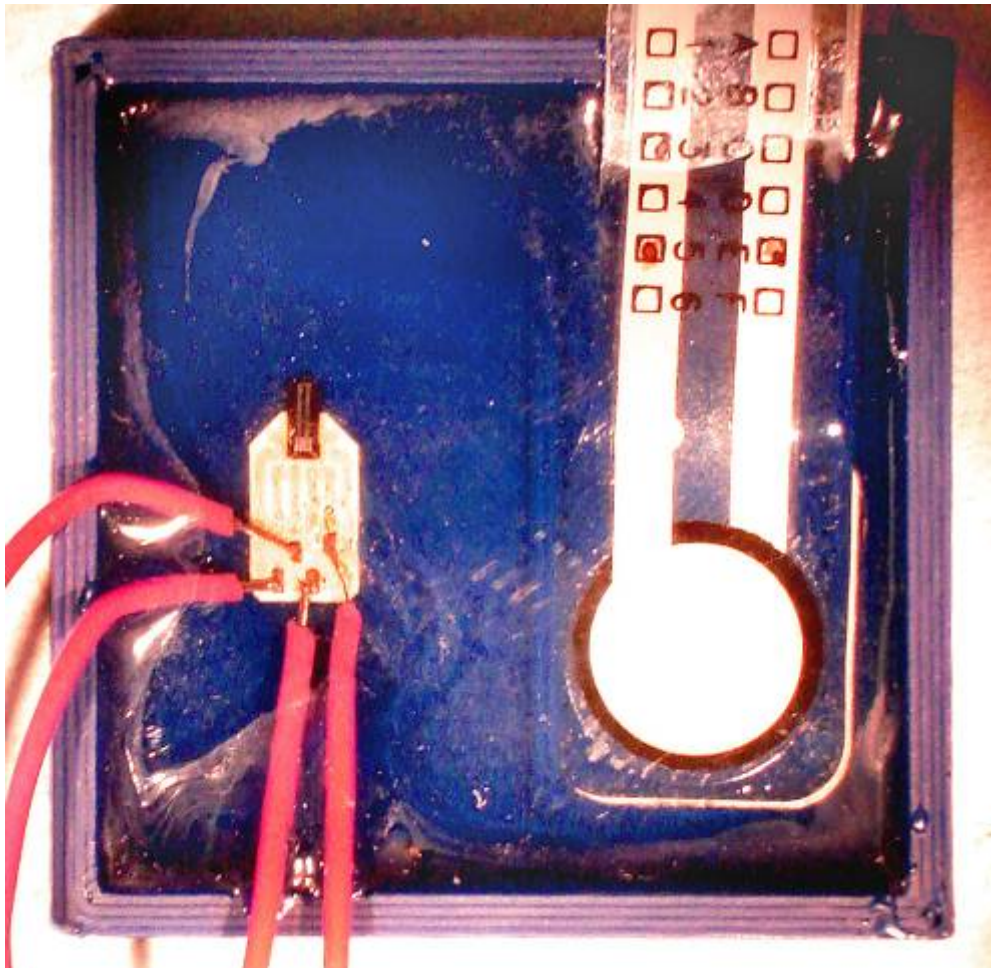


Figure 19 – Microcantilever and force sensitive resistor (FSR) encapsulated with 2mm of epoxy

The resistances of the microcantilever were recorded. If there is a drastic change in the values, it implies that the encapsulation induced deformation to the microcantilever. Since we cannot measure the resistance of the specified leg of the bridge independently without the parallel circuit of the bridge, the values shown are going to be bigger than the actual resistance. As shown in table 1, the resistances change are very small, indicating the curing of epoxy only put a small amount of residual stress to the sensor. It is also noticeable that the resistances between the microcantilevers are not consistent, which is possibly due to many factors such as manufacturing. The effect of the encapsulation can be minimized by the parallel resistor R_b as illustrated in figure 17.

The amount of stress protection from the encapsulation was also experimented. The encapsulated microcantilever was tested under the Instron tensile testing machine (figure 20). The strain rate is set to $20\mu\text{m}/\text{minute}$. The microcantilever was connected to the readout circuit, which will be discussed in the next chapter. The same test was conducted 8 times to ensure reliability of the data. On the last trial, the microcantilever was broken at around $473\mu\text{m}$ of extension at the load head, which is approximately 9.77MPa . The current drawn from a microcantilever is roughly 0.0025A , and the sensing area is assumed to be 15mm^2 . The average result is shown in the orange curve in figure 21. This demonstrated that encapsulated microcantilever can be used as strain sensor as

Table 1 – Comparison of resistance $V_{dd} \rightarrow VA // V_{dd} \rightarrow VB \rightarrow VA$ prior and after epoxy encapsulation

Before Encapsulation	After Encapsulation
1.085k	1.097k
0.735k	0.742k
0.969k	0.980k
0.723k	0.722k
0.685k	0.690k
0.674k	0.687k
0.721k	0.726k
0.729k	0.734k
0.719k	0.712k



Figure 20 – Experiment setup of the encapsulated microcantilever with Instron tensile machine

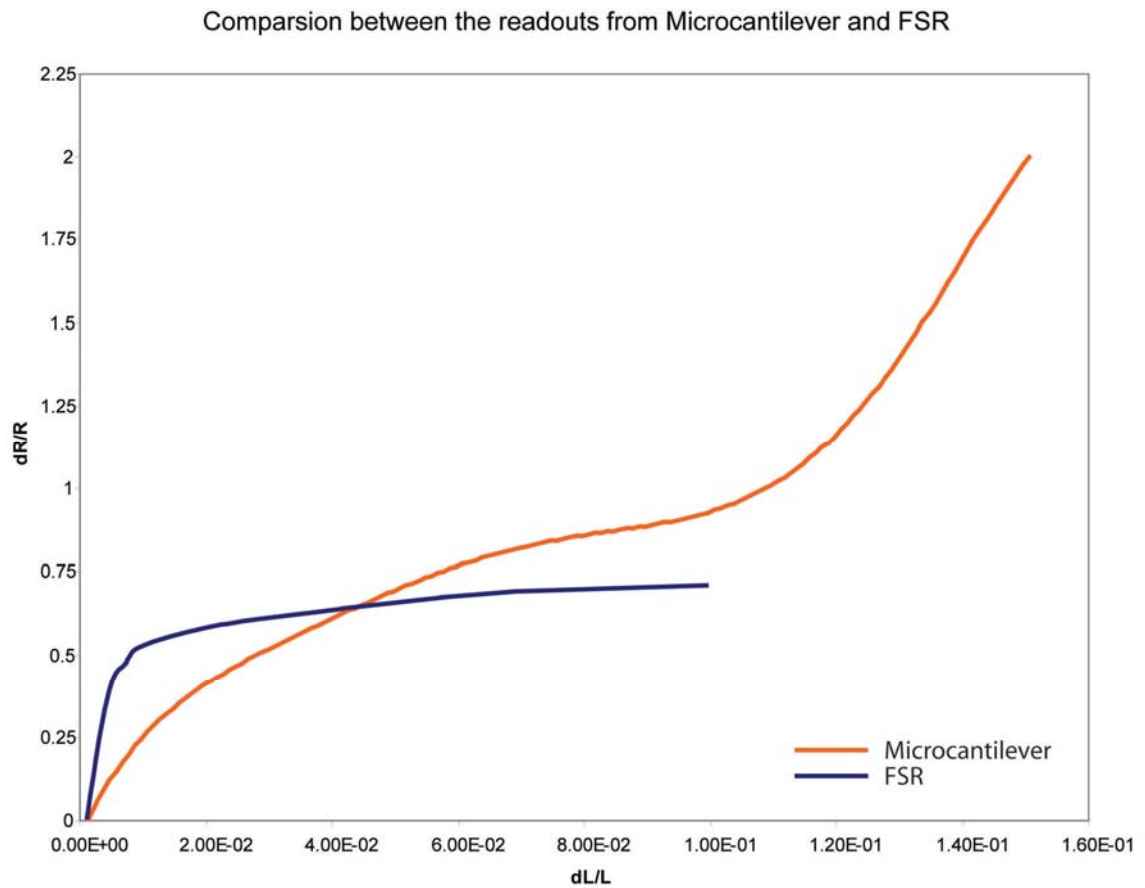


Figure 21 – Comparison between the readout from microcantilever and FSR

it works well beyond the stress recorded from previous intraoperative study, which is 30 to 150 kPa. The commonly used FSR was loaded under the same condition, which reaches saturation at the early stage (Figure 21). The properties of the microcantilevers encapsulated within 2mm of EP30MED epoxy is shown in table 2. The RSS error of the microcantilever is calculated to be +/- 0.873mV.

Another reason that we prefer MEMS device rather than FSR is size. The size of MEMS is significantly smaller than FSR and it is capable of resolving stress pattern in higher resolution. The size of the microcantilever sensor is approximately 0.25mm^2 and its base is about 32mm^2 . On the other hand, if the sensing area of FSR is approximately 78mm^2 , the surrounding seal adds the total area to 100mm^2 .

Table 2 - Properties of microcantilever encapsulated in 2mm of EP30MED

Parameter	Value
Range	0 – 300 kPa
Input	0 – 3.3V +/- 1%
Linearity	0.625mV/kPa (over range)
Repeatability	0.6444mV/kPa (over range)
Sensitivity	0.35455mV/kPa (over range)

Chapter 4

Electronics Design

As mentioned in previous sections, MCU based architecture requires various electronic components. However, the specification of these components is not clear and commercial testing and evaluation PCB that fits with the desired design of the system is not available. Therefore, scaled up prototypes are needed to determine and test the specification of these components.

4.1 Realization of the system

The system is designed based on the system architecture in figure 5 and the data collected from the testing of the microcantilever. Initially, photolithography was used to fabricate the circuit board that is used to test the response of the microcantilever. The masks were designed in Illustrator (Adobe) and printed onto a transparency. The copper board was exposed to light with the mask placed on top of it. After the exposure, it was placed into the developer to develop. The region exposed to light was etched away by stripper. It is a few simple steps for one-sided PCB. However, it became a very complicated

process for multi-layers PCB, which is necessary for advanced circuit design as in the prototype testing board. Misalignment of the vias that connect the layers together is common without the mask aligner and small and high precision drills. Hence, PCB design software, Easy-PC (Number one Systems, U.K.) was used to design the circuit layout and then exported it as gerber files and sent to the company to fabricate.

4.2 Initial Design of the Evaluation PCB

According to the system architecture, the initial design of the evaluation PCB consists of two double layer PCBs, which are designed based on their functionality. The first one is a MUX board (figure 22). Four pads were allocated for each microcantilever for wire bonding which includes power, ground and two outputs from the bridge. The output pads were connected to a dual 16-channels-to-1 analog MUX (ADG726, Analog Device). Since it is capable of opening two corresponding channels simultaneously, the differential outputs from the microcantilever can be obtained. This dual channel selection function is controlled by signal CS. Four more addressing signals (A0 to A3) are needed to control the switching between different channels for the MUX. The addressing signals are generated from a MCU, which is the center piece of the second board. The MCU board consists of the power supply and regulator circuit, which minimize the DC power noise and control the power source to the components at +3.3V.

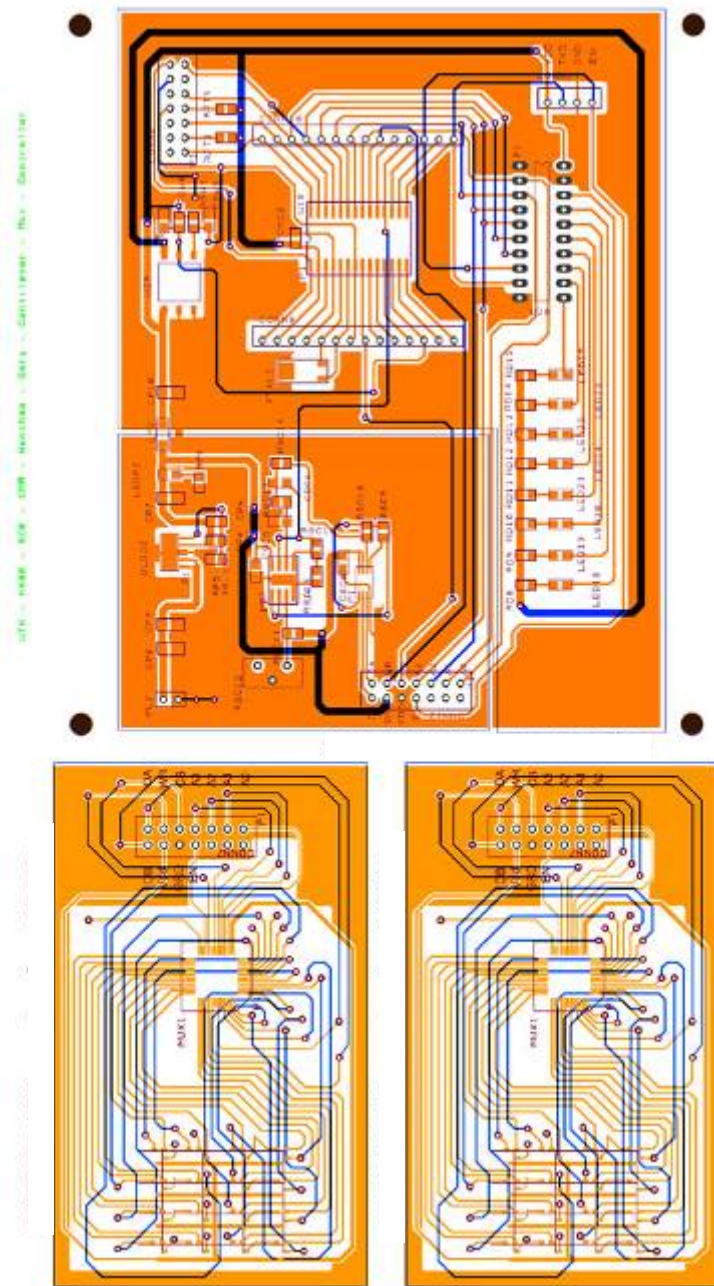


Figure 22 – PCB layouts for MUX and MCU Boards (Orange indicates top layer and blue indicates the bottom layer)

A second order low pass filter (LPF) using Sallen Key Topology with cut off frequency at 200Hz was designed (figure 23) [44]. An instrumental amplifier (INA331A2) is used for amplifying the signal. The gain is adjustable by connecting it to a potentiometer. A 16-bit ultra-low power MCU (MSP430, Texas Instrument) is used for addressing the MUX and functions as an ADC. A 10-pin joint test action group (JTAG) connector is used to connect the MCU to the computer and another 10-pin JTAG connector is connected to the MUX board. A buffer and a set of light emitting diodes (LEDs) were implemented to monitor the control signals from the MCU. The soldered boards are shown in figure 24.

A crystal oscillator (OSC) at 32.768 kHz was used as the clock for the system. A relatively low frequency OSC was selected on purpose for this prototype, so that the control signals are slow enough for inspection on the LEDs display. The MCU was programmed through the JTAG from a personal computer according to the functional block diagram in figure 25. Enable (EN) and write enable (WR) signals are sent to the MUX and TX when the MCU is powered up. The MCU sends out 5 addressing signals to the MUX board to control the channels to be opened for data. The acquired analog data was then passes through the LPF and amplified at the INA. The signal is then returned to the MCU. The MCU functions as an ADC and converts the analog signal into a digital signal. Each digital word from this ADC is 12 bits; however, only 10 bits is used. The digital signal is written temporarily into the RAM in the MCU.

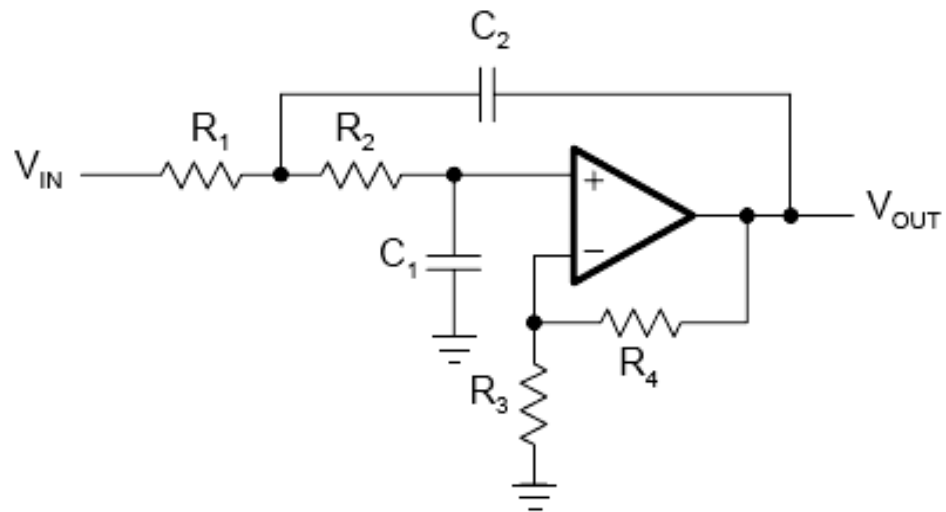


Figure 23 - LPF (Sallen Key Topology)

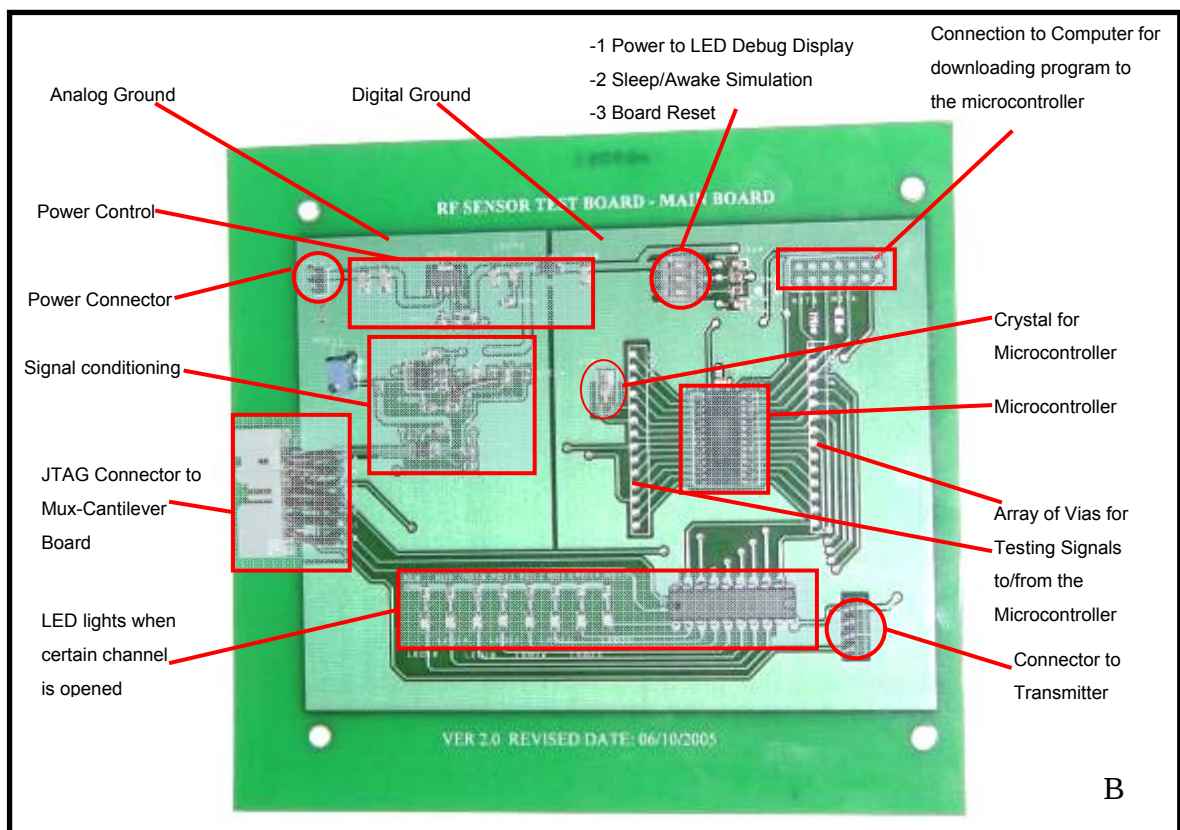
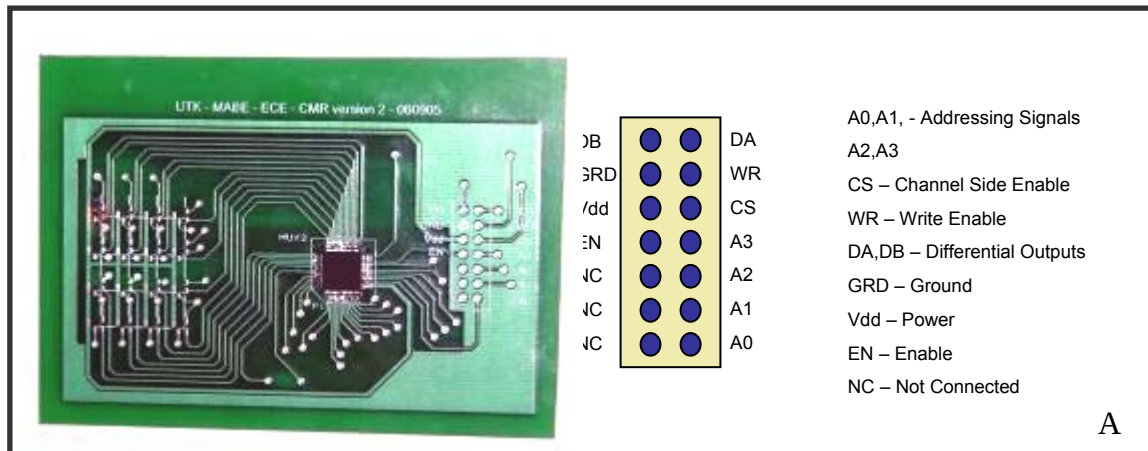


Figure 24 – Detail design and components of the MUX and MCU boards

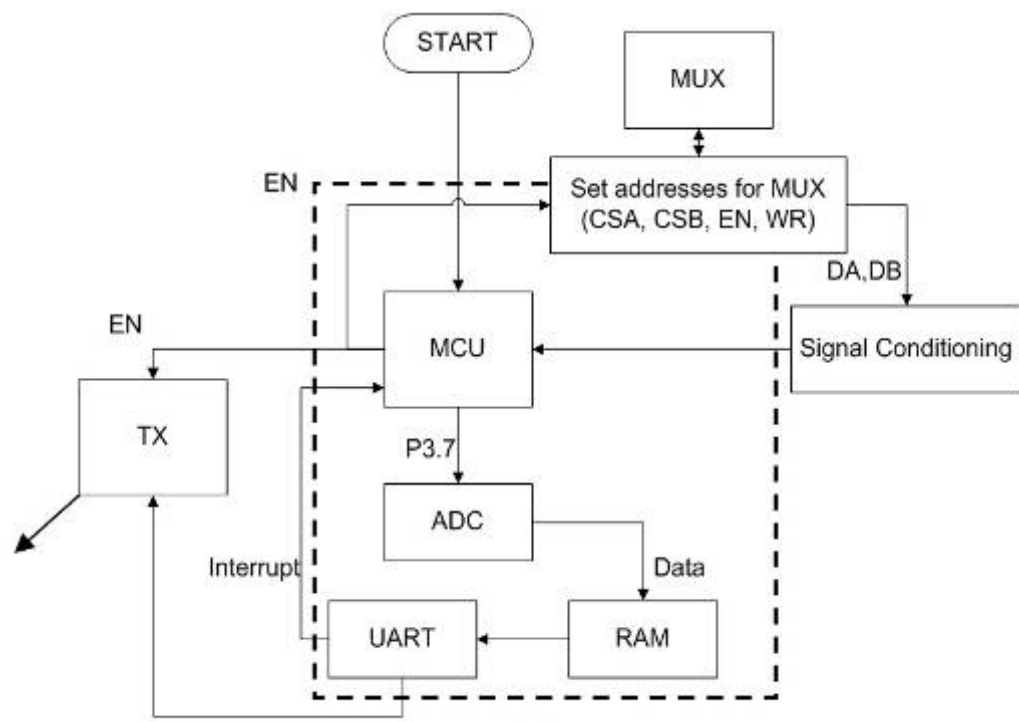


Figure 25 – Functional blocks of MCU

Universal asynchronous receiver/transmitter (UART) is established as the communication protocol between the MCU and the TX. The MCU registers every 8 bits of data and sends it to the TX for transmission. An interrupt signal is sent to MCU to clear the RAM after the TX has sent the signal.

The PCBs were debugged and several design errors and misconnections were resolved. The functions of the LPF and the amplifier were accessed. The cut off frequency observed from the fast Fourier transform (FFT) window of an oscilloscope was approximately 200 Hz. Using the frequency divider of the MCU, the control and addressing signals to the MUX works very well from the LEDs display. An encapsulated microcantilever was mounted onto the MUX board, which was then connected to the MCU board through JTAG. The sensor signal was monitored after the INA prior to the ADC. As the sensor was pushed with a finger tip, an immediate response was observed with the oscilloscope. The second iteration of the evaluation PCB was designed with 2 additional boards which hold the TX and RX. Before going into the details of the PCBs, it is necessary to provide information regarding the RF components selection and investigations with the carrier frequencies.

4.3 Carrier frequency selection and wireless communication protocols

The wireless communication between the TX and RX relies on the propagation of the electromagnetic (EM) waves, and its characteristic is dependent on the frequency used. The digital signal is mixed with the carrier frequency at the TX and then propagates through the antenna to the RX. Noise can be introduced during the transmission. Therefore, it is preferable to use the band of frequencies with the least interference for the carrier.

Kuhn et al. measured the EM interference in an OR during knee surgeries using various antennas and spectrum analyzer [45]. Figure 26 shows the power spectrum from 200 MHz to 2.5 GHz, measured intraoperatively during the surgeries. Two peaks were observed at 872 and 928 MHz, which correspond to the CDMA-2000 uplinks and downlinks in the US cellular band. The peak at 1.95GHz is also from the US cellular band. There is a noticeable peak at 2.4 GHz, which is corresponded to the WLAN and Bluetooth devices. Based on the electrical properties of the human tissue and the EM interference existing the OR, lower frequencies are more favourable to use as the carrier frequencies for the wireless communication of the device [45].

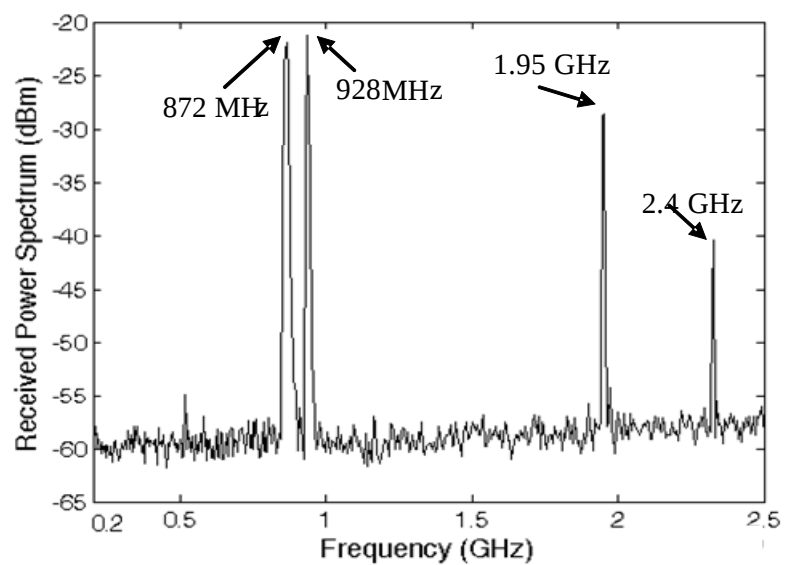


Figure 26 – EM interferences in OR

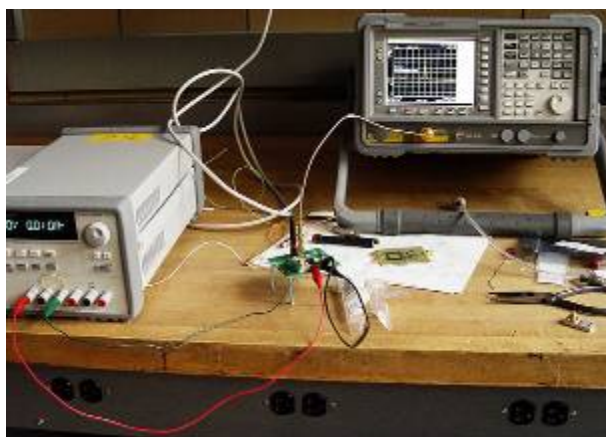
4.4 Second iteration of the evaluation system

Based on the requirements and results from earlier, a crystal referenced phase lock loop (PLL) TX (MAX1472) from Maxim-IC was chosen. It modulates the incoming signal and operates in the range of 300MHz to 450MHz (depending on the crystal) with a data rate of 100kbps. The TX uses the Amplitude Shift Keying (ASK) modulation method. With limited working space, ASK modulation was used due to its simplicity of the circuit as opposed to PSK or FSK, which require more components to perform the modulation function. There are also a few ASK TXs that are manufactured from other companies. However, MAX1472 has the smallest package size (3mmx3mm) with only a few off chip components, which is ideal for the system. The corresponding part (MAX1473) is used as the RX.

The second iteration of the testing boards includes the corrected MUX and MCU PCBs and the TX and RX boards. The TX and RX boards are shown in figures 27. The TX and RX circuits were designed and tested based on the manufacturer's specification. With the 13.56MHz crystal (XTAL) reference, the TX operates at 433.92MHz. It was connected to a +3.0V DC power supply at the Vdd and the Data_In terminal, and grounded at the Vss. The sub-miniature version A (SMA) connector of antenna_out was connected to the spectrum analyzer. (Figure 28a) The peak of about +10dBm was observed around 434 MHz (Figure 28b).



Figure 27 – TX PC Board (Top) and RX PC Board (Bottom)



(A)

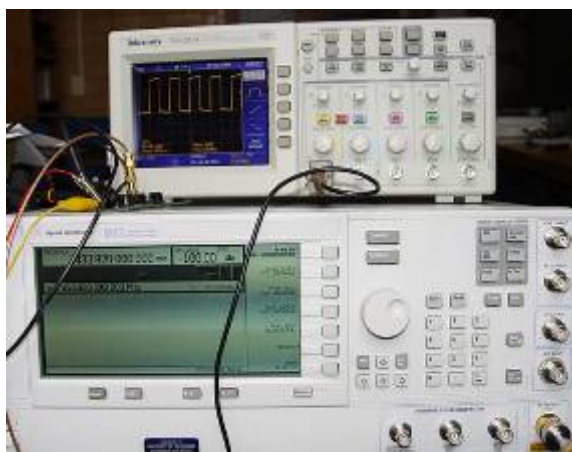


(B)

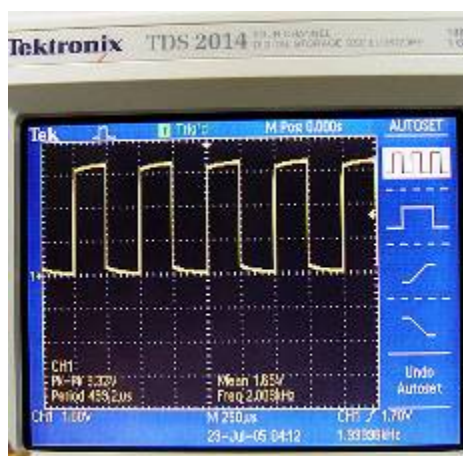
Figure 28 – A: TX experiment setup; B: the peak is detected at 433MHz

In order for the RX to operate at 433.92 MHz, a 6.6152MHz reference XTAL is used. A +3.3V DC power is connected to the Vdd terminal and grounded at Vss. It is then connected to a signal generator (Aligent E8257D), which is set to an output frequency of 433.92MHz at a power level of -100dBm. The modulation of the generator is set to a 2 kHz 100% amplitude-modulated (AM) square wave. An oscilloscope is connected to the Data_out terminal of the RX. (Figure 29a) A 2 kHz square wave is verified from the oscilloscope (Figure 29b). By reducing the signal level from the signal generator, the sensitivity of the RX was accessed, which was -115.6dBm or 0.2% bit error rate (BER). These two experiments demonstrated the performances of the TX and RX alone, and the next step is to establish communication between the TX and the RX.

Both the TX and RX were connected to a +3.3V DC power supply. A 1/4 wave whipped antenna was connected to the reverse polarity SMA on the TX board. A 200 Hz square wave created from the signal generator was applied to the Data_in terminal at the TX end. The input signal was also connected to the oscilloscope (Figure 30a). At the receiving end, the Data_out terminal was connected to an oscilloscope (Figure 30b). Figure 30c is the resulting display on the oscilloscope. Channel 1, the yellow signal, comes from the signal generator and was probed at the Data_in terminal at the TX side. Channel 2, the blue signal, is the Data_out from the RX side. The digital communication between the TX and the RX was satisfactory.



(A)

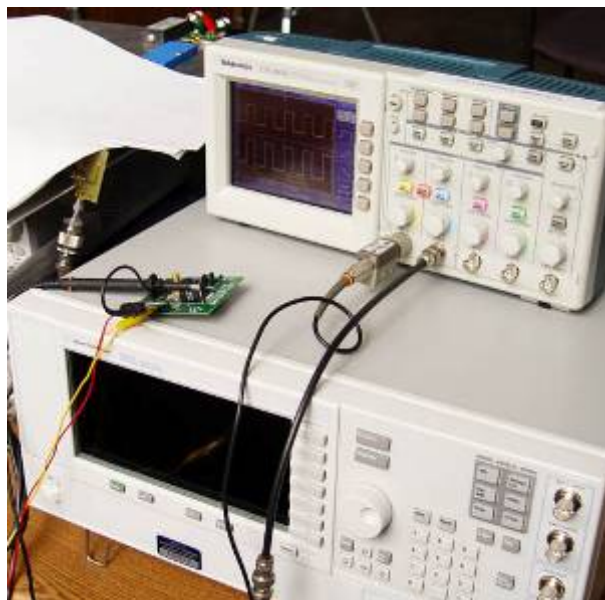


(B)

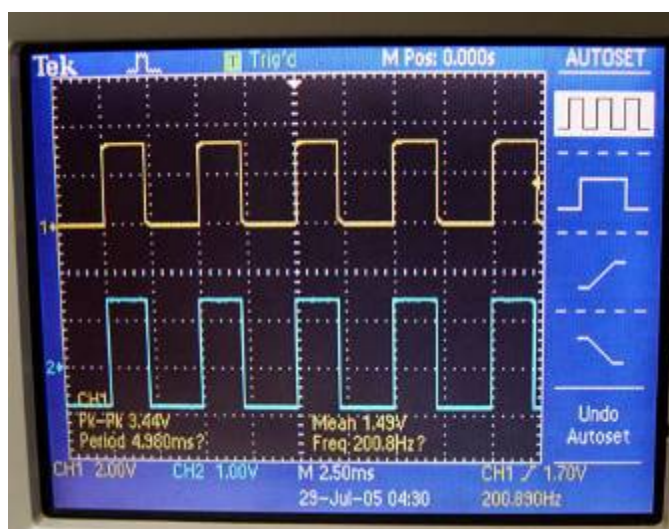
Figure 29 – A: RX experiment setup (A); B: received square wave



(A)



(B)



(C)

Figure 30 – A: TX setup; B: RX setup; C: Side by side comparison of the transmit and receive signal

After the testing of the RF communication components, the next step was to incorporate them with the MUX and MCU boards. There was not any error with the second iteration of the MUX and MCU PCBs. A +3.3V power supply was applied to all the boards. The setup was shown in figure 31. The MCU PCB was connected to the MCU PCB through JTAG. The digital data output from the MCU was feed to the data_in terminal of the TX PCB. The RX was connected to a DI/O card from National instrument and was connected to the computer. A 200Hz sine wave was applied to all channels on the MUX board. Hence, upon reconstructing the signal on the receiver side, it should become a 200 Hz sine wave. The signal prior to the modulation on the transmission side and after the modulation on the receiving side was monitored on the oscilloscope. Based on the observation from the oscilloscope, the transmitting and receiving signals looks identical. However, these data were logic ones and zeros. Therefore, they cannot be interpreted without DSP.

One concern was that the data stream was resampling at the RX and that one bit could be sampled multiple times depending on the sampling rate of the DI/O. Hence, if the signal contained the same bit consecutively, the computer would not be able to separate the different bit as there is no sync information for synchronizing the resample data into bits. It is also not economical to allocate an extra TX to transmit the sync information. A self synchronization technique was used to re-clock the signal. A stream of single bit alternating logic zeroes and

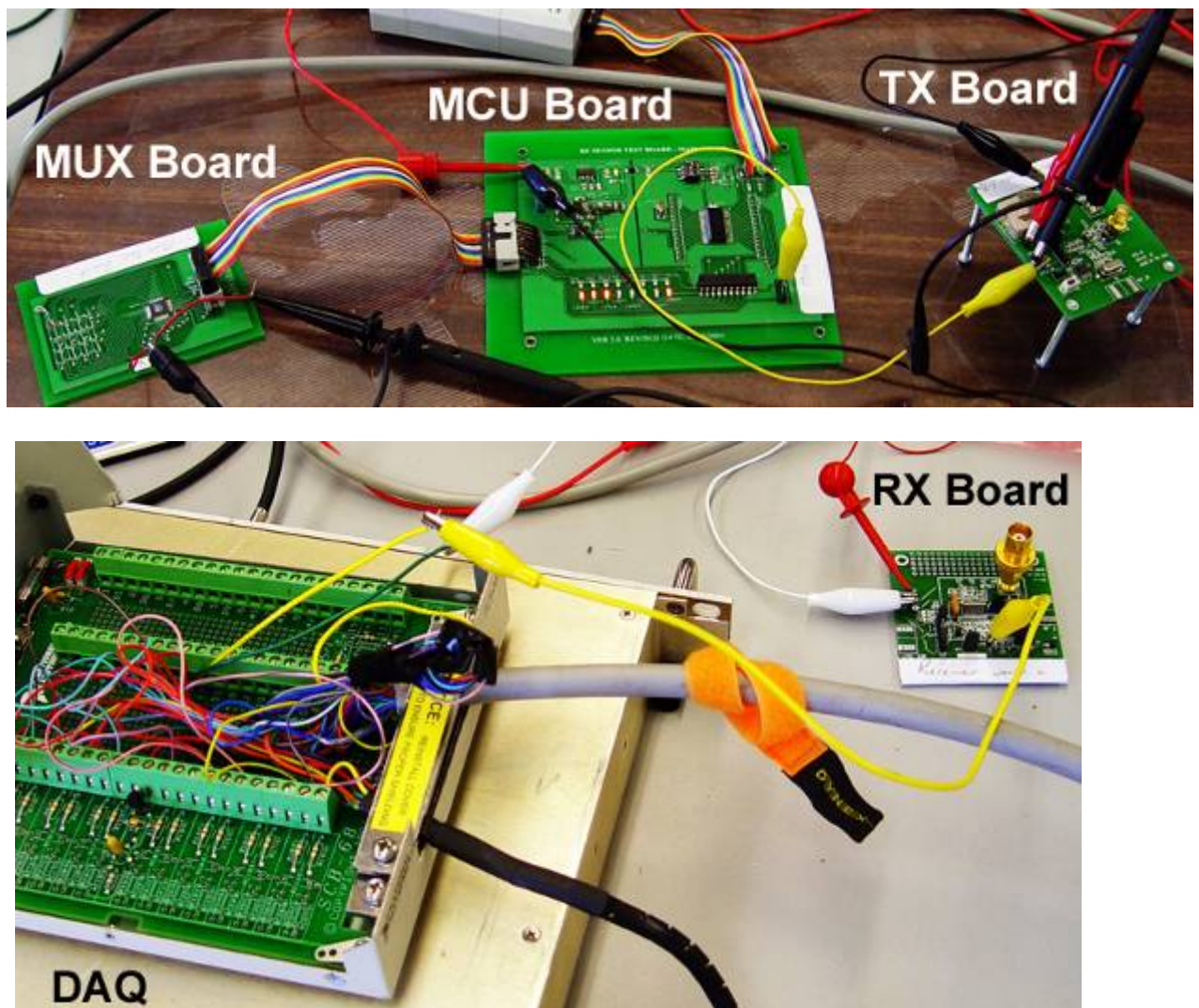


Figure 31 – Board level experiment setup.

ones was sent from the TX to the RX. The computer counts the number of times that each bit was sampled. The average count of 1 bit of data was used to interpret the counts for different numbers of bits. The conversion from number of counts versus number of bits was then established.

In order for the RX to recognize the beginning of the data stream, a 10 bit comma signal was then introduced. The comma signal was generated from the MCU at the beginning of every multiplexing cycle, or in other words, every other 16 channels. The DSP program was written in MATLAB. First, the program establishes a connection with the DI/O card. The computer then stores the data sampled at DI/O. The program searches for the 10 bit comma signal in the stored data. At least 2 comma signals are needed for each set, as it guarantees that it captures the data for all 16 channels. These data were then extracted and the comma signals were discarded. Since the UART submits 8 bit of data from the MCU to the TX at a time, each channel will have 16 bit word. However, only the last 10 bit represents the actual data. Next, we want to check if the extracted data has the information for 16 channels and assume that there is no bit synchronization error. The total number of bits should be 256. The next step is to eliminate the 6 extra bits from the data of each channel. The data is then sliced and converted from binary to decimal. The reconstructed sine wave is shown in figure 32.

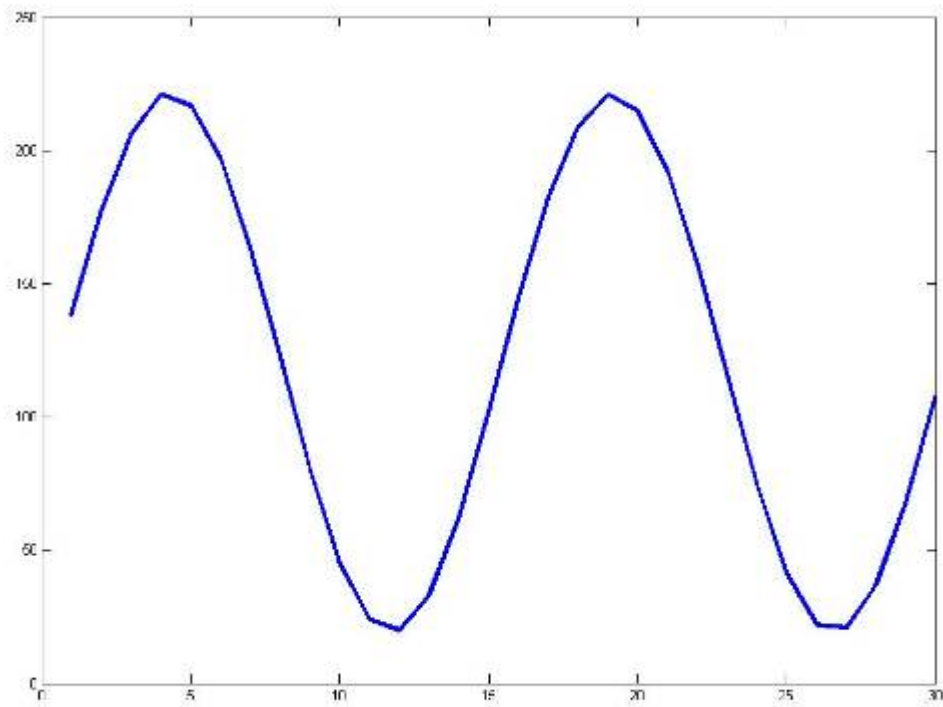


Figure 32 – Reconstructed signal

Chapter 5

ASIC Design

As seen in figure 31, the entire system consists of three different PCBs, of which the total areas for components are well over the geometry that any instrument would allow. The biggest challenge is the vast amount of components required to perform the function as well as the amount traces needed to connect them together. One of the solutions to resolve this problem is to increase the number of layers of the PCB instead of the standard double layers. An attempt was made to migrate the system to a 6 layer PCB. However, there is only enough surface area to fit half of the intended system. Additionally, there is not enough area for vias which connects the traces in between layers.

Commercially available ICs are usually packed with multiple functionalities from which the user can pick. Despite of the high quality and ease-of-use, they are not tailored to perform the specific functions needed for the system. Hence, multiple components are always needed in order to achieve the desired functions. It is definitely not preferable with limited working space. Moreover,

noise can be introduced to the system through the connecting traces and vias. As the MEMS signal is usually very small, it should be avoided as much as possible.

There are two methods that can reduce the number of components and retain all the necessary functions at the same time. The first method is to use field-programmable gate array (FPGA). FPGA is a semiconductor based IC that has programmable logic components, such as simple logic gates and math functions. The interconnections between the logic components are also programmable. The requirements of the system are first decided and then the schematic of the system is designed. The description of the system is translated into the computer for simulation, using hardware description language (HDL). The synthesis program then maps the design into a netlist and then translates it into gate level description and checks to ensure the translation is corrected. The design is laid out in the FPGA and then simulated and debugged.

The second option is designing a fully customized application specified integrated circuit (ASIC) for the system. Unlike the commercial available general purposed ICs, ASIC is custom designed for the application. Like FPGA, ASIC design begins with establishing the system requirements and schematic design. The design is modeled and simulations are also conducted to test the design. ASIC is a hierarchical design process, which starts from low level parts and builds up to high level components and functional blocks. The layout design of

the ASIC locates at the top level of the hierarchy. Simulations are done in different levels to ensure proper functions and interconnections between parts. The final output from the design is a set of photomasks for standard IC fabrication. The design flowchart is illustrated in figure 33 [46].

FPGA is a more economical option than a full-custom ASIC design. However, it is usually slower than ASIC due to latency and pre-routing, which the technology is based on. Complex system design is usually not feasible. The packages of FPGA are in generally large to allow the user to have enough pins for their application. FPGA consumes much more power than ASIC, which is not suitable for a low-power system. ASIC also can incorporate a much higher density of logic on one chip than FPGA. Moreover, FPGA is only economical for scaled up prototypes which were done earlier in the previous chapter. Also, after the initial design cost, ASIC chip is much more cost-effective than FPGA in production level.

Although the system is not very complex, the surface area and the cost are important factors for this system. Due to the high power consumption, FPGA is highly undesirable. Hence, the full custom ASIC design method is used.

5.1 First iteration of the ASIC design

Based on the test results from the scaled up prototypes in the previous chapters, the following functions are incorporated into the first iteration of

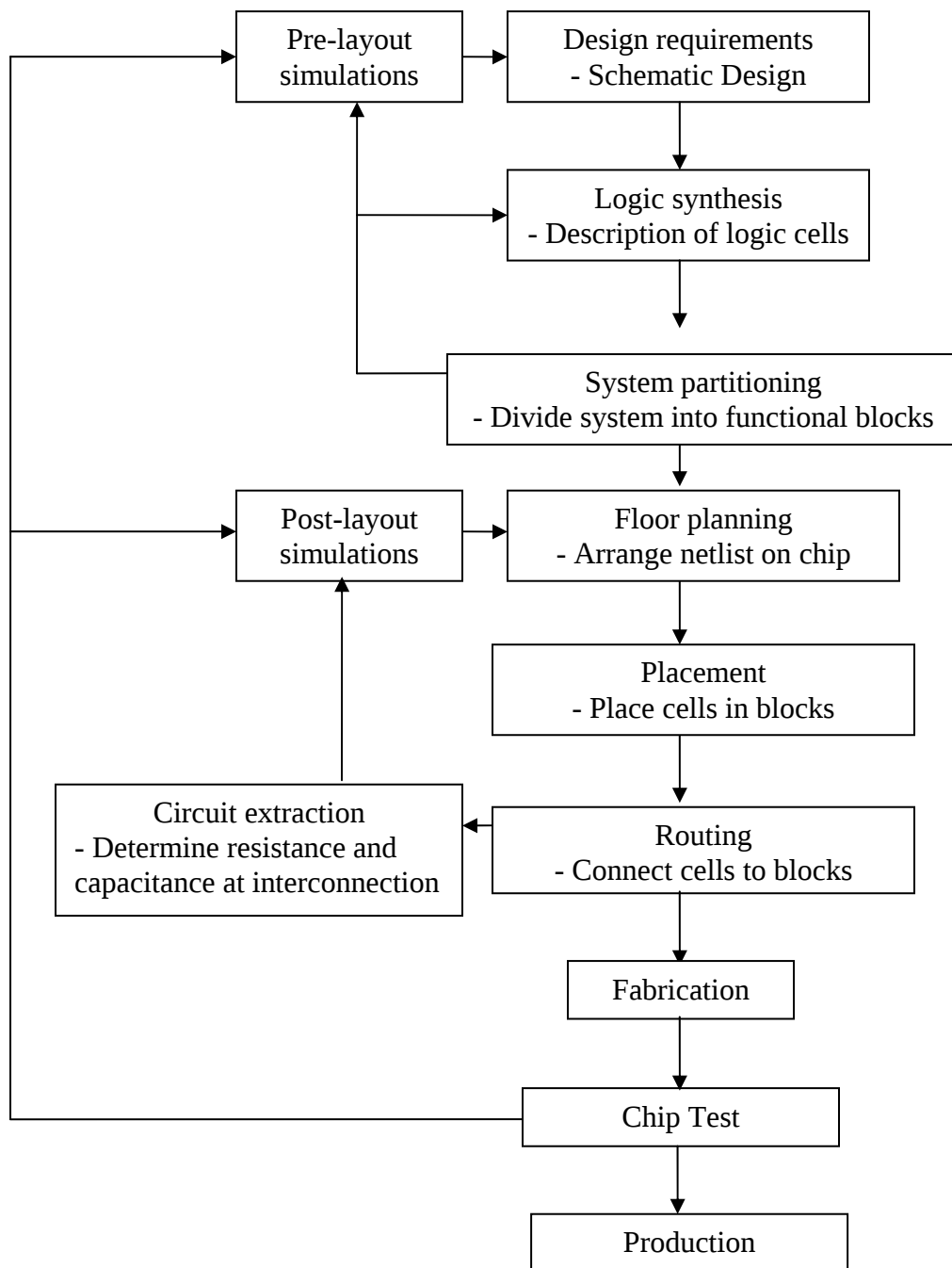


Figure 33 – Design flow of ASIC

the ASIC design.

- Clock network (CLKNET)
- Signal amplification
- Sample and Hold (S&H) circuit
- ADC

Typically, the instrument is used for 10 to 15 minutes during surgery. Therefore, the ASIC was designed to use +3V battery power (CR2032, Panasonic).

5.1.1 CLKNET

The most important part of the ASIC design is the CLKNET. The ASIC logic is based on the raising edge of the clock or control signals. Hence, improper clock timing can jeopardize the results regardless of how well other components perform. The input of the CLKNET circuit is connected to the output of an oscillator (OSC). The circuit generates various controlling and addressing signals based on the frequency of the OSC. In this design, the CLKNET controls the operation of the ADC, which will be discussed in later section.

5.1.2 Signal Amplification

An INA was implemented to amplify the differential sensor signal from mV

range to full scale (FS) and reject the common mode signals [47]. Hence, a reference voltage is needed. Ideally, the reference voltage should be one half of the FS to obtain the maximum dynamic range. However, taking into consideration that there are more components later in the chain (e.g. ADC and DAC), the range should be set under the maximum possible FS to allow margin for error correction. Therefore, the voltage reference is designed to be adjustable with an external potentiometer. The gain of the INA is also set to be adjustable. The circuit diagram of a typical three operational amplifiers (op-amp) configuration INA is shown in figure 34. V1 and V2 are the differential signals from the Wheatstone bridge of the microcantilever. The internal resistance (R) of the INA is $20\text{k}\Omega$ and the external resistor (R_{gain}) is adjustable based on the level amplification needed. The gain (A) is a function of the ratio between the internal and external resistances, which is given in the following equation.

$$A = \left(1 + \frac{2R}{R_{gain}} \right), \text{ where } R = 20\text{k}$$

This configuration is suitable for the application since it has very high input impedance and common mode rejection ratio (CMRR), very low DC offset and low noise, and the gain is easily adjustable with a single resistor.

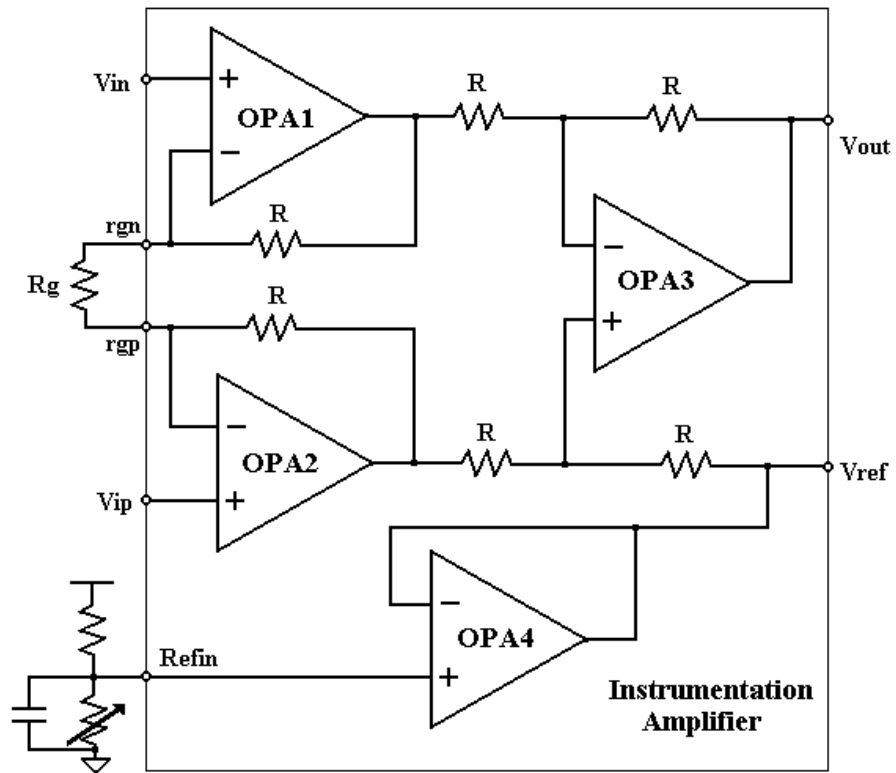


Figure 34- Circuit Diagram from INA

5.1.3 S&H circuit

The primary function of the S&H circuit is to sample and hold the analog signal constant during the conversion period of the ADC [48]. The instantaneous value of the analog signal is sampled periodically. During the conversion process, the ADC requires the input analog signal to be held steady for a small period of time so that it can compare the converted signal with the original signal for error. If the signal is allowed to change during the conversion period, the converted signal will not be able to converge and the digital word output will not be the true representation of the analog input.

A simplified S&H circuit consists of a switch and a capacitor. When the switch is closed, the input signal is stored in a sampling capacitor. The switch is then disconnected during the conversion period. The switch is closed again after the conversion and a new value is set. The rate at which the switch is opening and closing is the sampling rate of the ADC. The rate is dependent on the conversion rate of the ADC, which is different based on the ADC design.

5.1.4 ADC Selection

As mentioned above, there are many different types of ADC, which are selected based on the requirements of the system. The primary design issue with ADC is the tradeoff between speed and resolution. Fast ADC, such as flash ADC design, is capable of converting the signal in a single cycle, but the

resolution is limited. Slower ADC design such as sigma-delta method allows up to 24 bits resolution, but it requires multiple stages and cycles for a single conversion. The system here requires a moderate speed conversion and resolution. Hence, Successive Approximation Register (SAR) logic ADC is the optimal choice between these two parameters [49].

5.1.5 SAR Architecture

SAR ADC consists of 4 major parts, which are a comparator, a register, a DAC and the SAR logic circuit [50]. It works as a trial and error method to convert analog signal into digital word. The block diagram of a SAR ADC is illustrated in figure 35. The digital word of the reference voltage (V_{ref}) is set at the middle of the FS of the ADC at the beginning of the conversion period. In the first cycle, the signal from the S&H circuit (V_{in}) is compared to the V_{DAC} with a high accuracy comparator. The SAR logic is very similar to the binary search algorithm. It decides the logic zeros and ones based on the following rules:

- $V_{in} > V_{DAC} \rightarrow \text{output} = 1;$
 - o New V_{DAC} is set to $V_{DAC} + \frac{1}{2} V_{DAC}$
- $V_{DAC} < V_{in} \rightarrow \text{output} = 0$
 - o New V_{DAC} is set to $V_{DAC} - \frac{1}{2} V_{DAC}$

The most significant bit (MSB) of the register records the output from the logic circuit. Depending on the output of the comparator, V_{DAC} will either increase or

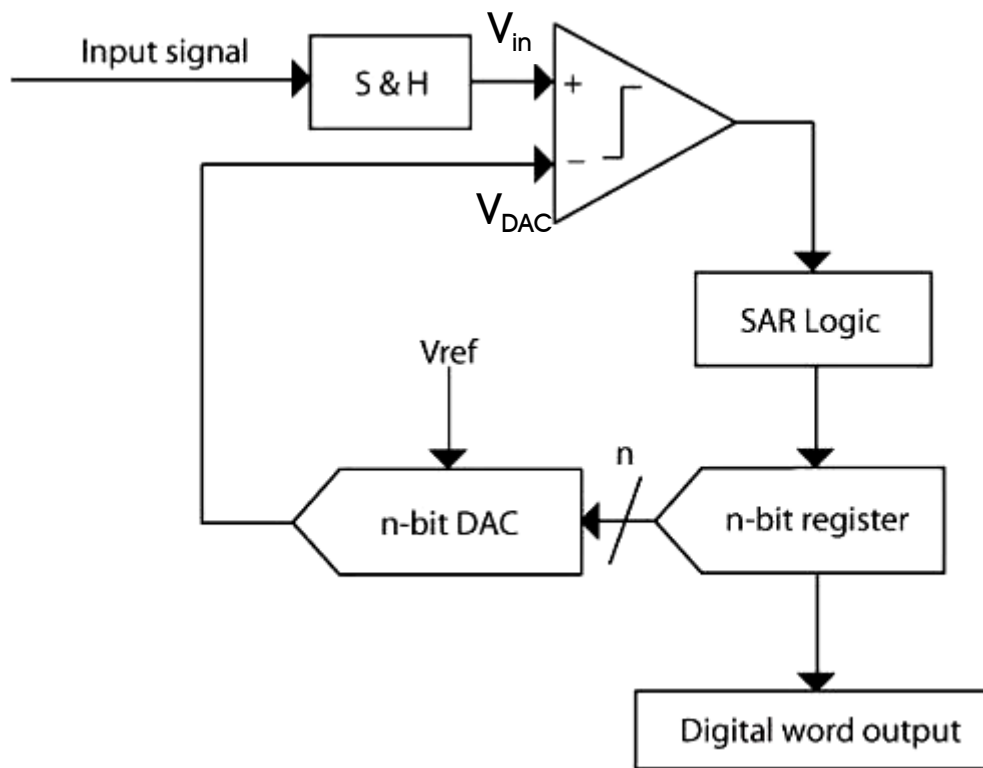


Figure 35 - schematic for SARADC architecture

decrease by one half of the value of itself. This completes the first cycle of the conversion. The cycles are repeated n -times until the least significant bit (LSB) is converted. Hence, a n -bit SAR ADC requires n cycles of conversion to reach the result.

SAR ADC can be considered as the middle ground of the trade off between speed and resolution. It does not work as fast as the flash ADC. It requires n -cycles to complete the conversion. It does not go as high resolution as the sigma delta ADC since it will require too many clock cycles, which makes it impractical. However, there is no pipelined delay at the end of the conversion period since the data corresponding to the edge of the sampling clock is immediately available. This makes it very easy to implement in a multiplexed application as compared to other ADC types. Also, SAR ADC is extremely power and space efficient. It requires the least components and very low power dissipation, which makes it the ideal method for low-power application. Hence, an 8-bit SAR ADC is implemented into the system.

5.1.6 ADC design and implementation

As mentioned before, the CLKNET provides the trigger for all the components within the ASIC. The timing for the trigger for the ADC is very important. The relationship between the clocks for the S&H circuit (shClk), ADC reset (adcReset) and DAC (dacClk) is illustrated in figure 36. The shClk triggers

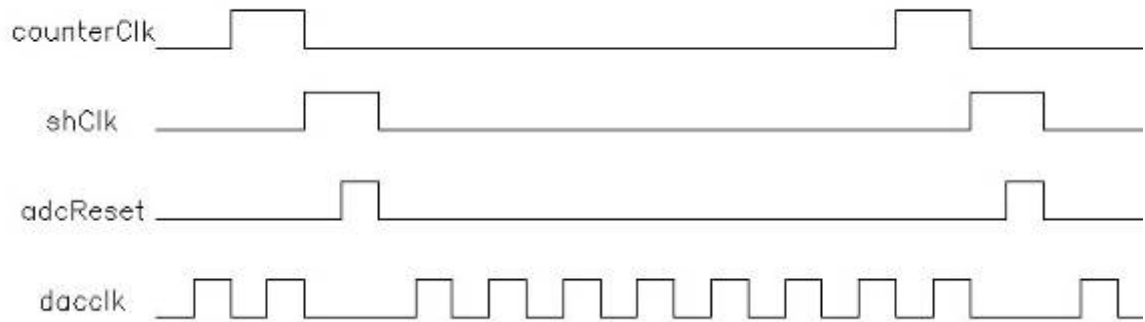


Figure 36 - timing diagram for the 8bit ADC

the S&H circuit to sample and holds the analog value from the sensor. The register of the ADC is reset at the rising edge of the `adcReset`. The DAC requires a trigger on every conversion period. Hence, there are 8 triggers for the `dacClk` in between two triggers from the `shClk`.

The overall accuracy and linearity of the ADC depends on two components, which are the DAC and the comparator [51]. Their design will be discussed in the following paragraphs.

Since the MSB transition of the DAC represents the largest excursion of the output, the settling time of the DAC is determined by the MSB setting, as the DAC has to settle within the resolution of the overall converter. The linearity of the DAC also determines the linearity of the ADC. Hence, switch capacitive DAC design, which is based on the principle of charge redistribution, is used. The capacitive DAC consists of an array of binary weighted capacitors and a dummy capacitor. The accuracy of the ADC requires a high resolution comparator for comparing the hold value with the testing value. Figure 37 shows the schematic of an 8 bit SAR ADC design based on charge redistribution [52]. The following paragraphs detail the implementation of the SAR ADC

5.1.6.1 Sampling and Holding

During sampling, switch A (SA) is closed and connected to the ground. Switch B (SB) is connected to the sampled voltage (V_{in}). The other switches (S8

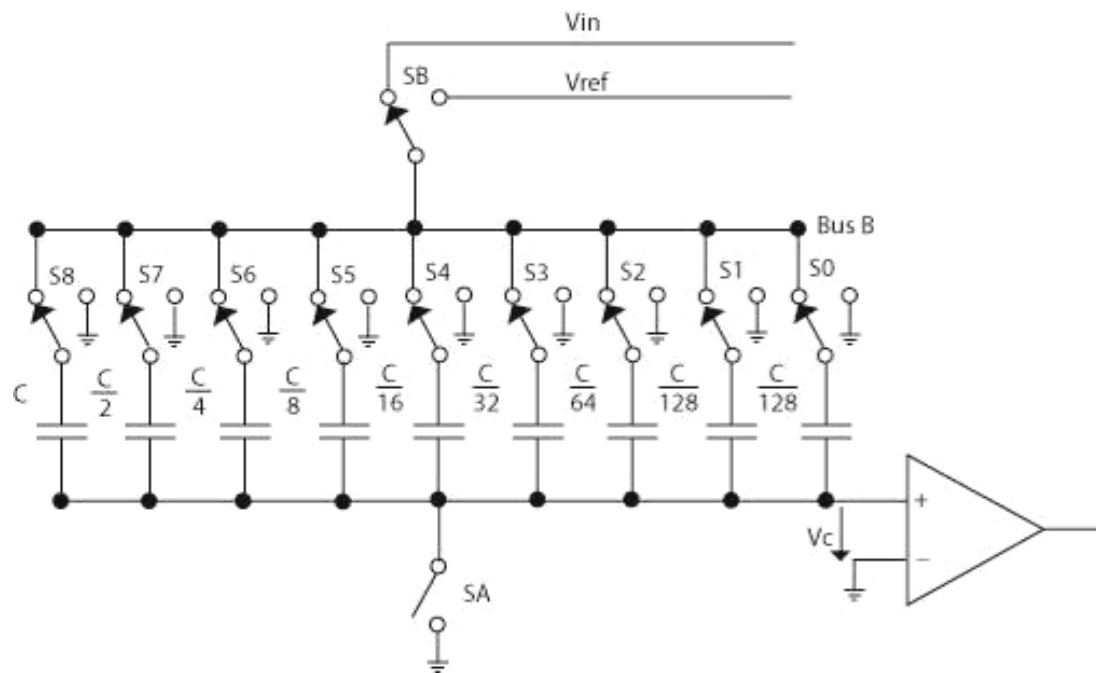


Figure 37 - SAR ADC design based on charge redistribution

– S0) are connected to the common bus B. This configuration charges the lower plates of the capacitors. The total charge (Q_{in}) is equal to,

$$Q_{in} = -2C \times V_{in}$$

After the sampling, SA is opened, SB is connected to V_{ref} and S8 to S0 are connected to the ground. Hence, a voltage of $-V_{in}$ is applied to the input of the comparator, thus achieving the hold function.

5.1.6.2 Charge redistribution and conversion

The conversion begins by first connecting the largest capacitor (C) to V_{ref} thru S8, which forms a 1:1 capacitance divider with the S7-S0 that are still connecting to the ground. The input voltage of the comparator (V_c) becomes

$$V_c = -V_{in} + V_{ref} / 2$$

With a high resolution comparator, the MSB is determined. If the V_{in} is greater than $V_{ref}/2$, V_c will be less than 0, which results in a high output from the comparator and the logic 1 will be established for the MSB. On the other hand, if the V_{in} is less than $V_{ref}/2$, V_c will be greater than 0, resulting in a low output that corresponds to logic 0 will result from the comparator.

The next step then connects $C/2$ to V_{ref} . The next bit is determined by comparing V_{in} to either $V_{ref}/4$ or $(3/4)V_{ref}$. If the logic output is 1 from the MSB, S8 is then connected to ground to discharge C. V_c then becomes

$$\begin{aligned} V_c &= -V_{in} + bit8 \times V_{ref} / 2 + V_{ref} / 4 \\ &= -V_{in} + (3/4)V_{ref} \end{aligned}$$

If the MSB is equal to logic 0, V_c becomes

$$V_c = -V_{in} + V_{ref} / 4$$

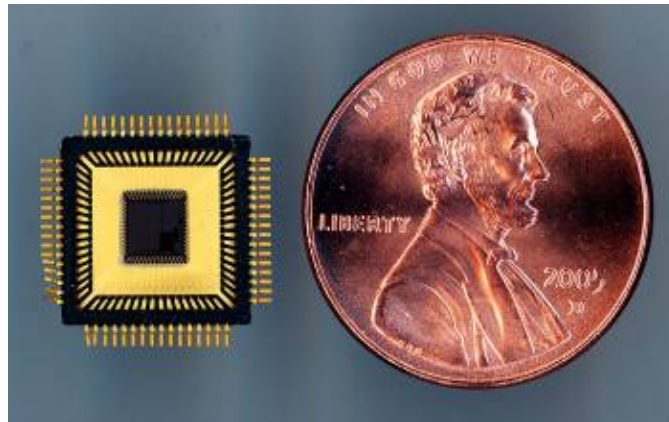
The process continues until all bits are determined. For the 8 bit ADC, the equation for V_c of the LSB is

$$\begin{aligned} V_c &= -V_{in} + bit8 \times V_{ref} / 2 + bit7 \times V_{ref} / 4 + bit6 \times V_{ref} / 8 + bit5 \times V_{ref} / 16 + \dots \\ &\quad bit4 \times V_{ref} / 32 + bit3 \times V_{ref} / 64 + bit2 \times V_{ref} / 128 + bit1 \times V_{ref} / 256 \end{aligned}$$

The ASIC chip is simulated with Cadence's Spectre. Transient analysis, AC analysis and noise analysis results show that the whole chip works very well under different process corners and a $-40\sim 85^\circ\text{C}$ temperature range. The layout is done using Cadence Virtuoso with clean Design Rule Check (DRC) and Layout vs. Schematic (LVS). The parasitic parameters were extracted and used in post-layout simulation. The pre and post-layout simulation does not show much difference due to the good floor plan and optimized place and route. The ASIC is designed for the $0.35\mu\text{m}$ Taiwan Semiconductor Manufacturing Company (TSMC) fabrication process and packaged with 64 pins Thin Quad Flat Pack (TQFP) package. The chip size is 3mm^2 and the package size is 10mm^2 .

A PCB designed to test the ASIC is fabricated to access the performance of the ASIC (Figure 38), which includes the clock generator, reset generator, power regulator, and manual channel selection for the addressing signals, signal input connectors and various testing points for the ADC, DAC, and INA. Four chips were tested with two using a 32.768 kHz OSC and two using a 1.544 MHz OSC. The CLKNET performs very well. The INA was also accessed. The open loop gain of the INA is about 60 dB. It has a unit gain bandwidth greater than 2.4 MHz, as shown in figure 39a. Even though minor overshoot is observed with the step input, the settling time is very fast as shown in figure 39b. The phase margin is approximately 45°. The S&H circuit of the ADC is tested with input ranging from 200mV to 2.4V for a 3.3V power supply. In figure 40, the S&H circuit is set to hold the value for an extended amount of time. The characteristic of the S&H can be observed from figure 40a (slower OSC). With faster OSC, the S&H period becomes too small to observe from the oscilloscope (figure 40b).

Since the ADC consists of multiple parts, several probing points were added during the design phase of the chip to assess these areas. The DAC feedback mechanism of the SAR ADC performs very well. Digital code was manually input to the DAC and the analog voltage output was observed. Figure 41 shows the linear relationship between the digital code and its analog voltage. The red line indicates the ideal transfer function and the blue dots are the collected data. There is a sudden jump at 700mV due to the fact that it is a

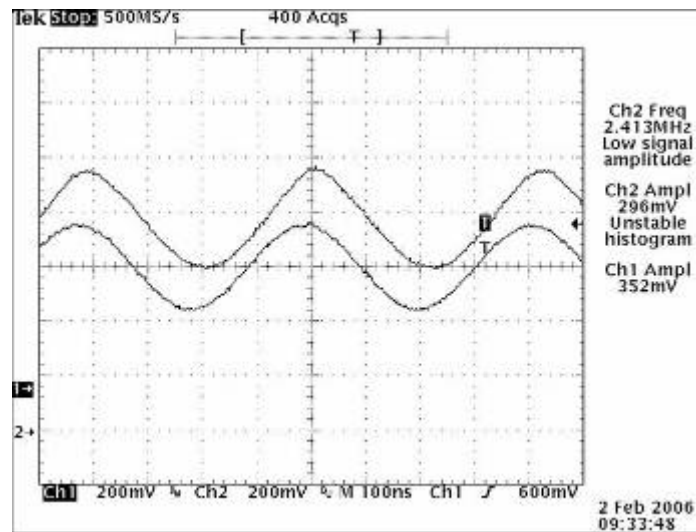


(A)

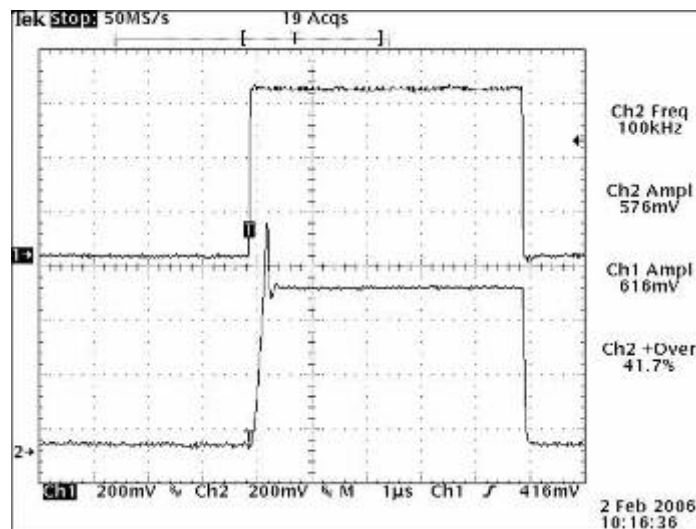


(B)

Figure 38 –A: the fabricated IC and package; B: the PC board for evaluating the IC

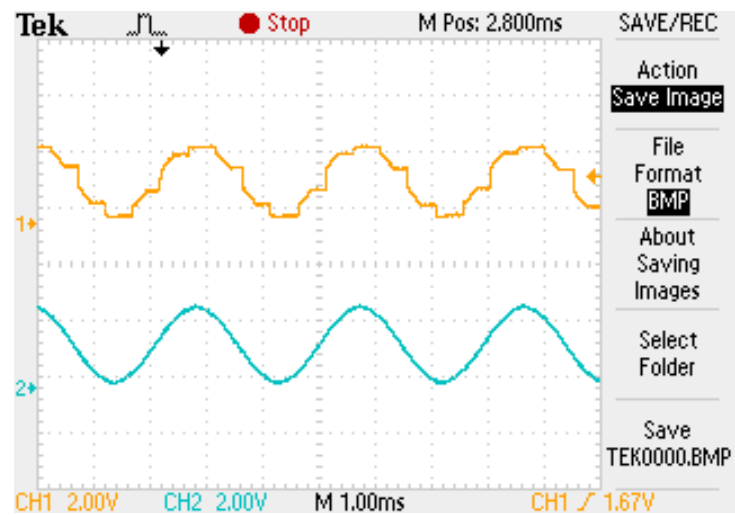


(A)

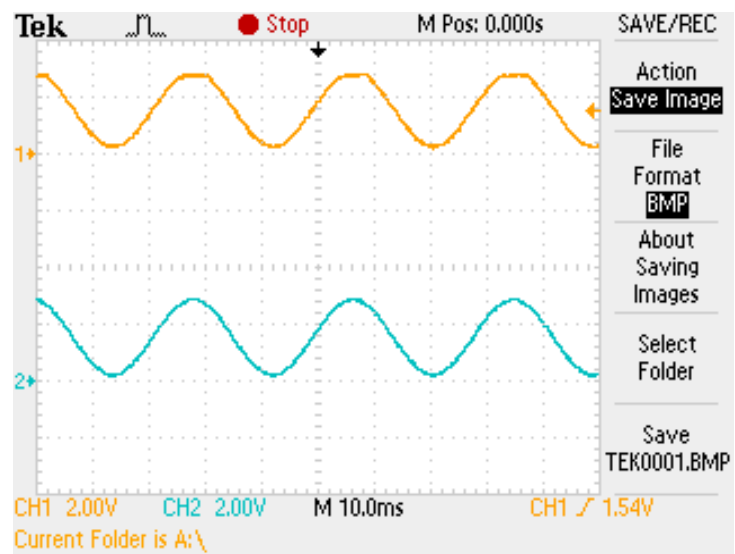


(B)

Figure 39 – A: Unit gain Bandwidth of the INA; B: Settling error and phase margin of the INA



(A)



(B)

Figure 40 – A: S&H with 32.768kHz OSC; B: S&H with 1.544kHz OSC

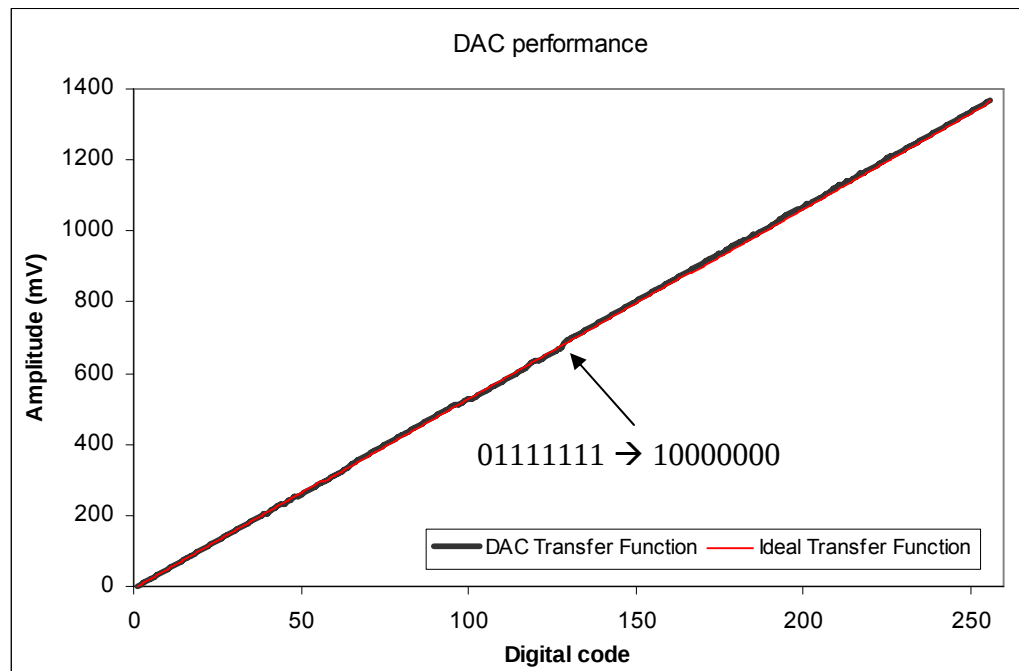


Figure 41 – Linearity of the DAC (Black: Data; Red: ideal transfer function)

complete switch of the binary code from 01111111 to 10000000. The differential nonlinearity (DNL) and the integrated nonlinearity (INL) of the DAC were tested (figure 42). DNL represents the error from 1 LSB for every step and INL represents the error between the output and the ideal conversion line. The jump occurred at 700mV can be seen as the large amplitude change from the DNL and INL figures.

The comparator of the ADC, however, is not performing as expected. A sine wave is given to the ADC for conversion. However, two of the ADCs do not respond to the input at all, as shown in figure 43a. Since the amplitude dropped to half of the original in each bit cycle, it is an indication that the comparator is not working. The other two chips seem to perform the conversion; however, the comparator does not perform well. As shown in figure 43b, difficulties were experienced with the input when the amplitude is closed to zero crossing.

5.2 Second iteration of the ASIC design

The second iteration of the ASIC design includes all the features and corrections of mistakes in the first design as well as integrating more functions such as MUX and its control signals, parallel inputs to serial output (PISO), parity check and comma generator.

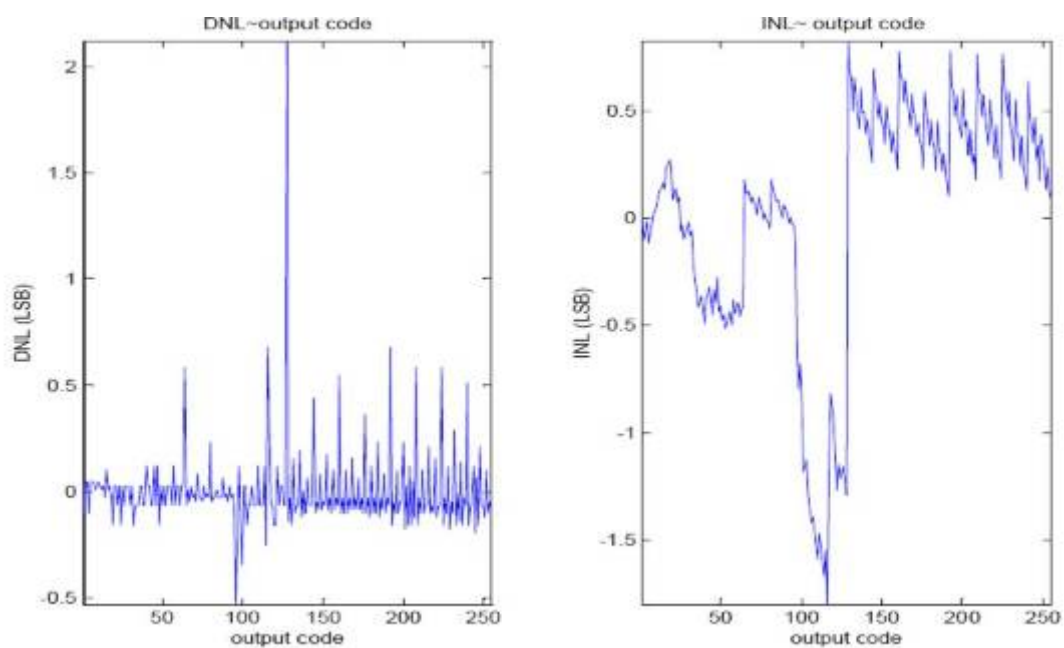
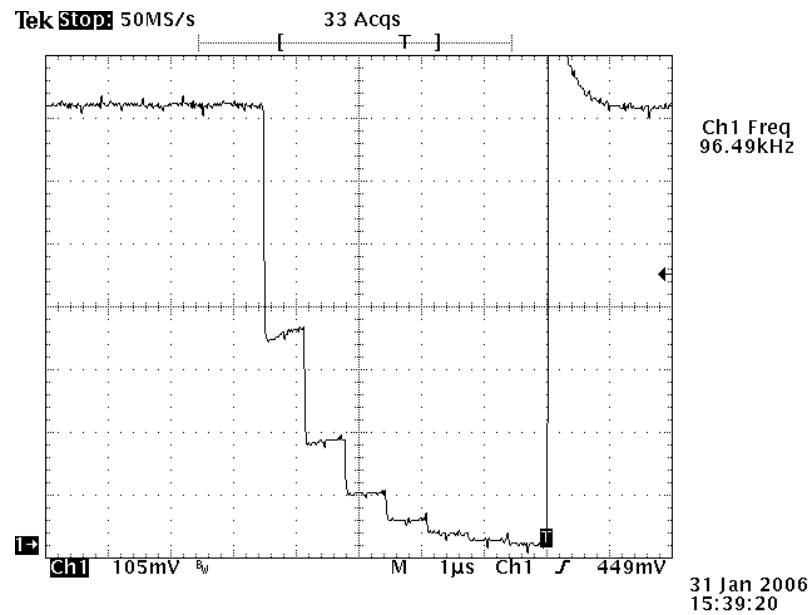
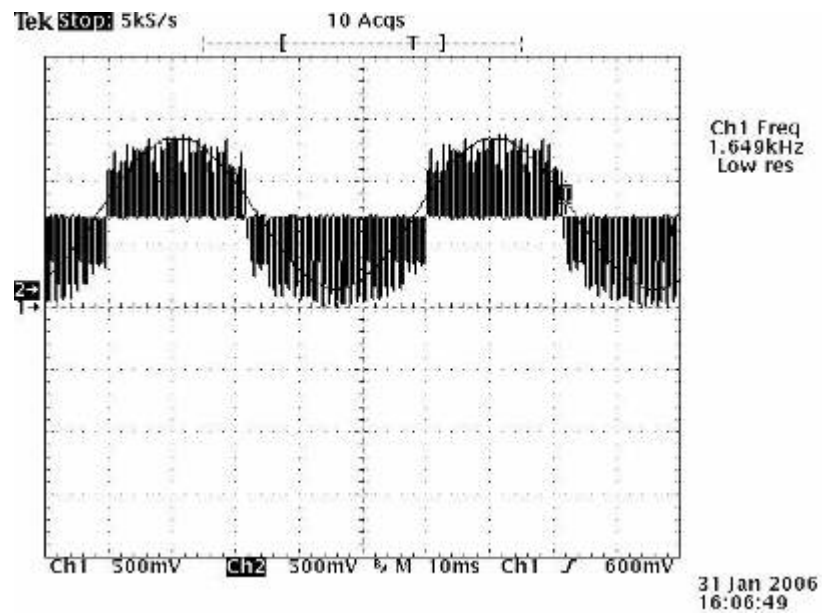


Figure 42 - DNL (left) and INL (right) of the DAC



(A)



(B)

Figure 43 – A: No response from the ADC; B: Comparator malfunction when the input is close to zero

5.2.1 MUX

A MUX using time division multiplexing was implemented. Since the output from the microcantilevers has two differential outputs, it requires twice the inputs for the multiplexer. However, since one side of the bridge remains constant, a new readout method is used to reduce the number of inputs. The schematic is shown in figure 44a. R2 and R3 is a half bridge that is constantly connecting INA. The MUX switches between different sensors for the other input of INA. A 5 bit decoder is designed for signal selection. Only 30 channels are used because a comma signal is necessary for the RX to recognize the beginning bit of the signal. Two channels of the MUX are used by the comma signal. The revised functional block diagram is shown in figure 44b.

5.2.2 ADC

From the previous ADC design, there is a major design issue related to the metastability of the comparator, which is the ability of the comparator to make a decision of whether the input voltage is larger or smaller than the reference voltage. The output of the comparator is either logic HI or LO depending on the result from the comparison. In order to achieve such logic output, the input voltage must be sufficiently large enough to push it in one direction or the other. However, there is a chance that the comparator is unable to make a decision. As the result from the previous design indicated, the comparator is incapable of

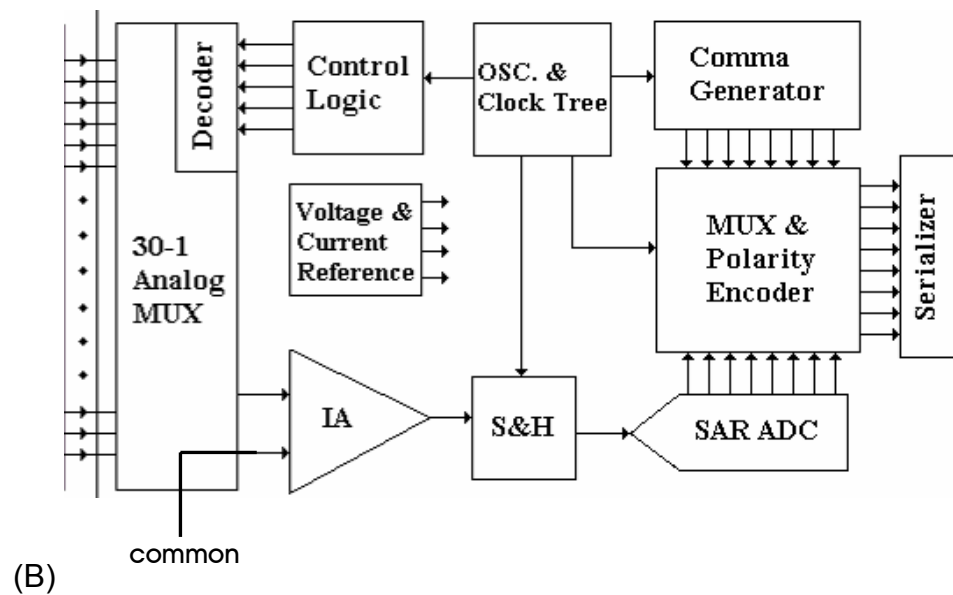
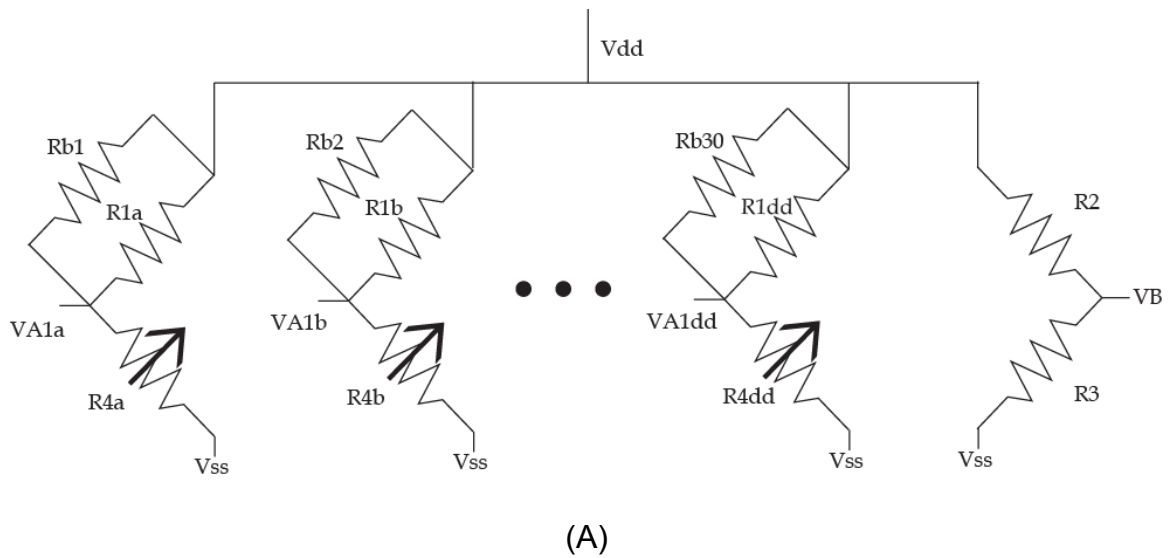


Figure 44 – A: Readout Circuit for multiple microcantilevers; B: Revised functional block diagram

distinguishing the input near zero crossing of the sine wave. A metastable output is highly undesirable since the output is completely random and impossible to correct in signal processing. In order to resolve this problem, the new ADC design added a regenerative latch at the output of the comparator [53]. In this case, the input only needs to start it in one direction, and the regenerative latch drives it to the decision. The second additional component of the ADC is the PISO. In the previous version the digital output was in parallel, which requires 8 channels to complete each output. The PISO component converts the multi-parallel outputs into one single serial output. Parity check is also introduced as a bit integrity check. An even number of ones in the data will result as logic zero for the parity bit and one for an odd number of ones.

5.2.3 CLKNET

The general function of CLKNET is the same as the previous ones. However, an additional network was needed for the triggering of the MUX. The 5 bit addressing signals were designed as a part of the new CLKNET.

5.2.4 Comma Generator

In order for the receiver to distinguish the beginning and end of the serial data, a comma generator is introduced. The comma generator generates a comma signal of 11001100 and 00110011 at the end of each MUX period. The

parity bit check of these two signals is opposite to the input signals from the sensor channels, which will be one.

The second iteration of the ASIC was also designed in Cadence (figure 45). Three systems were implemented. One system was from the first iteration with fixed mistakes, but without the latched amplifier for the ADC. The second system is a discrete version of the new system, in which the components are separated from each other and they can only be connected externally. It also contains various probing points for debugging and testing. The third system is the complete system with the minimum amount of input and output pins. This ASIC was also fabricated with 0.35 μ m TSMC process and packaged with TQFP-80 (14mm x 14mm) as shown in figure 46. A PCB testing board was also designed for testing of the chip (figure 47).

5.2.5 CLKNET Test

The oscillator is 12.352MHz. CLK13M/P75, which is the clock input to the chip and has a square wave with frequency at 12.352MHz from the oscillator. CLK842out/P76 is frequency of each of the 16 channels. A square wave with frequency at 772kHz is observed. For the 5 bit addressing signals, A0 to A4, their frequencies are 42.888kHz, 21.444kHz, 10.722kHz, 5.361kHz, 2.6805kHz respectively. The frequency for DAC reset, ADC clock and the serial enable

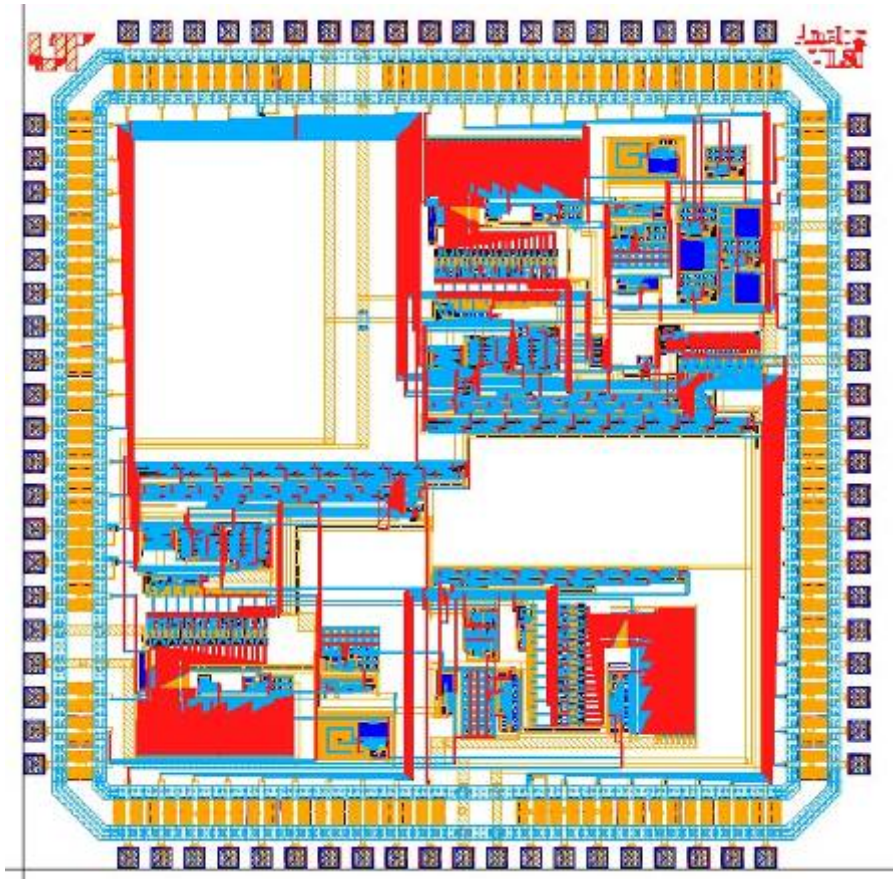
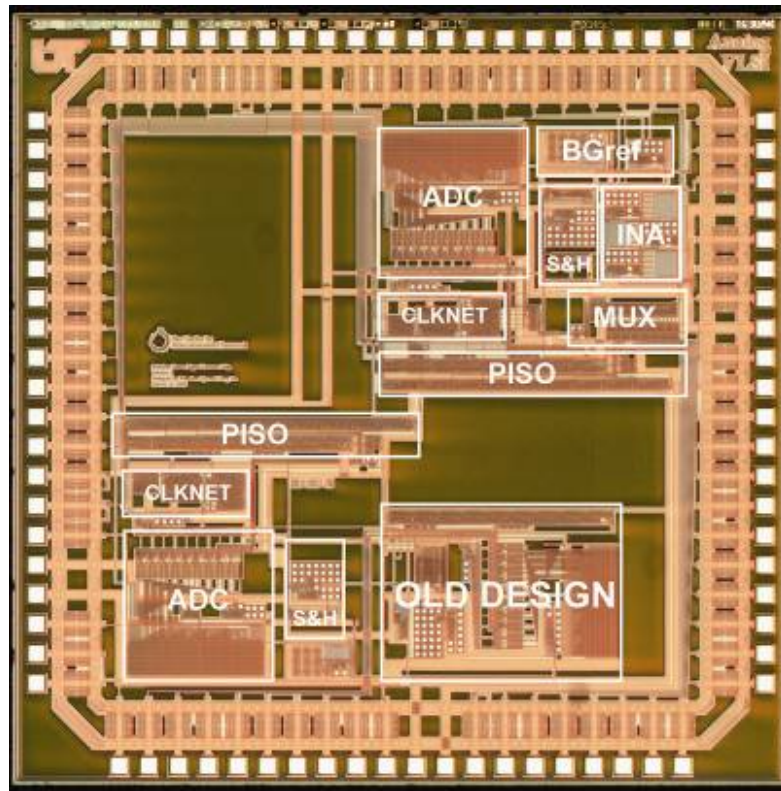
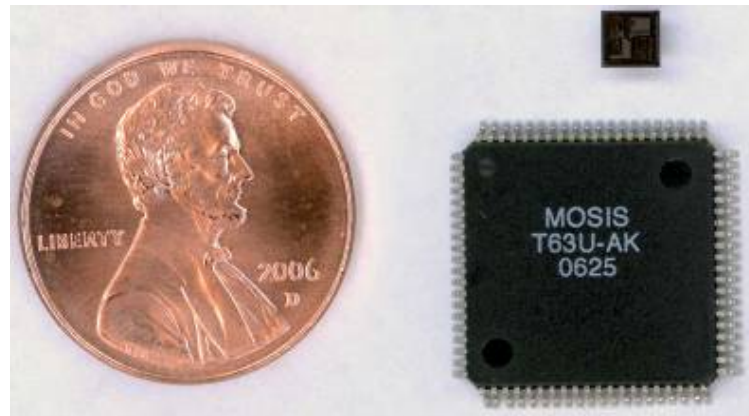


Figure 45 - Layout of the second version of ASIC



(A)



(B)

Figure 46 – A: The micrograph of the ASIC (A); B: the IC and its package

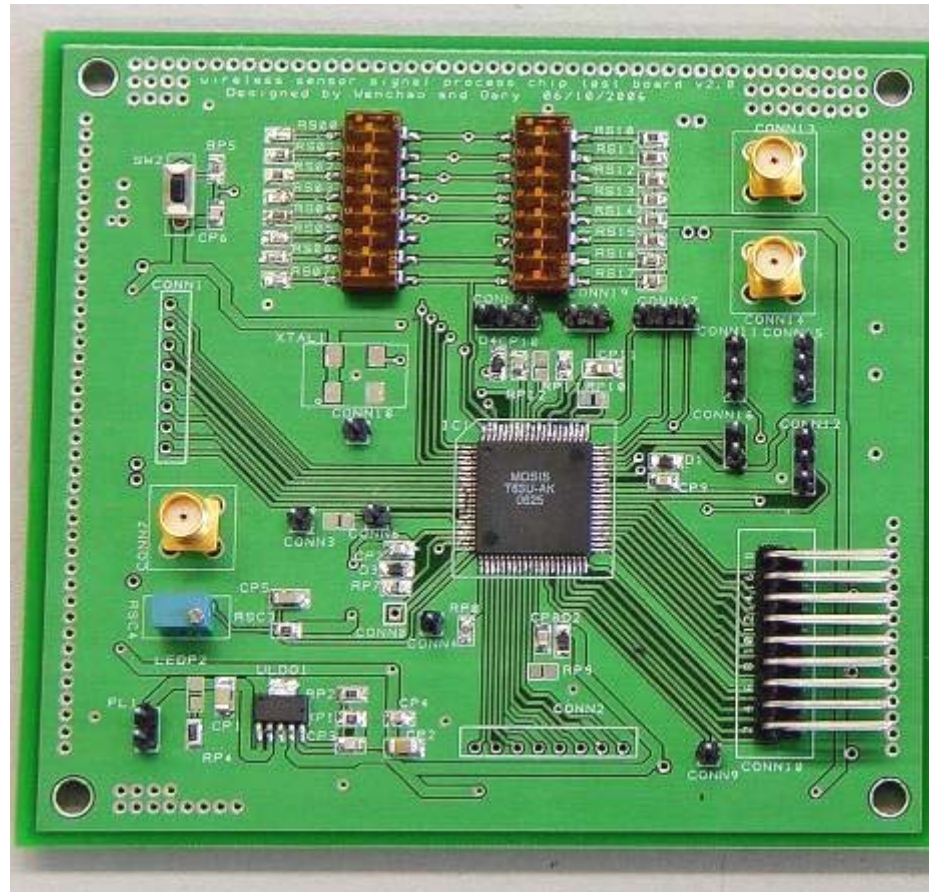


Figure 47 – Evaluation PC board for the second version of the ASIC

signal is at 85.7758kHz. From the logic analyzer, the timing of each pulse train was observed (figure 48).

5.2.6 Band gap reference and S&H Test

The band gap reference is a technique that is used to generate a stable voltage reference that is independent to the temperature [54,55]. It was measured to be 1.249V. The S&H circuit for the ADC performs well, even with the high frequency input clock (figure 49a). The input range of the S&H circuit is 80 to 2580mV.

5.2.7 ADC Test

The comparator of the ADC with regenerative amplifier was tested. Sine waves with different frequencies were applied to the input of the ADC and the output was monitored. The conversion of 5k sine wave was observed (figure 49b). The oscilloscope shows a rough result of the comparator as it compares and converges to the hold signal. The input sine wave frequency was reduced to 1k (figure 49c). The result shows that the comparator is sensitive to identify small changes in the input voltage. Although the results observed from the oscilloscope reveal decent performance from the comparator, more testing is needed to collect precise measurements to further access the performance of the ADC. The input of the chip was connected to a function generator, and the output was

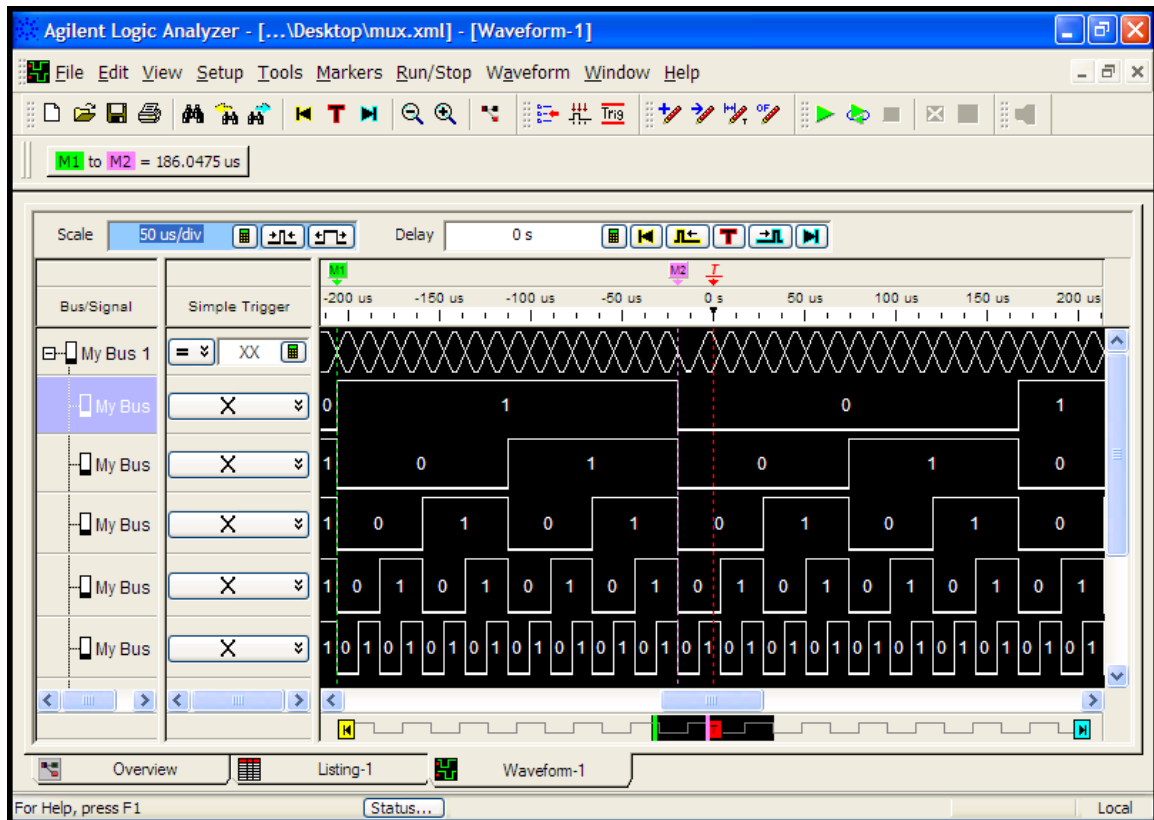
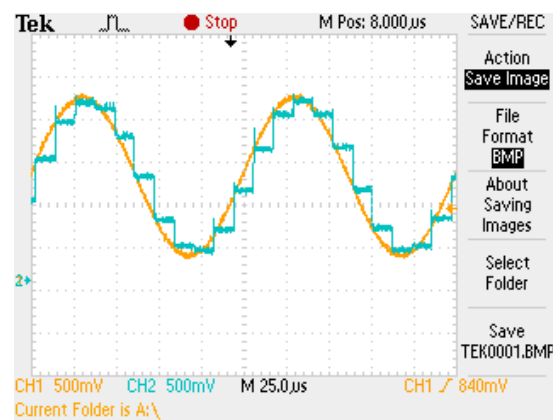
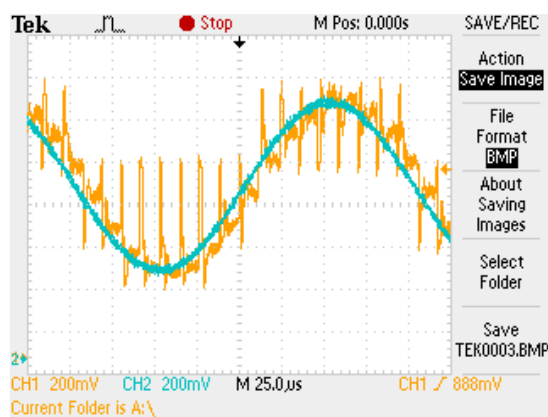


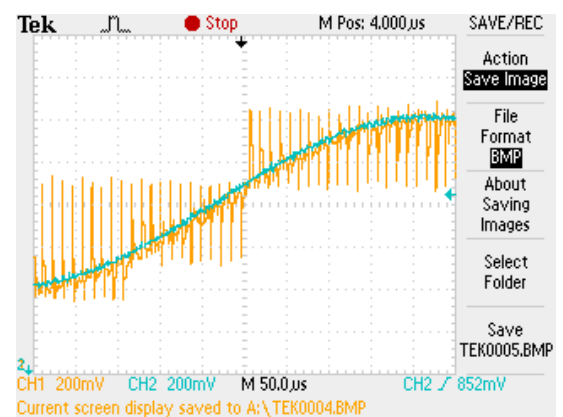
Figure 48 - Timing analysis of the CLKNET



(A)



(B)



(C)

Figure 49 – A: Performance of the S&H circuit at high frequency input; B: Conversion of the ADC at high frequency (Blue: input signal; Yellow: output response observed at the register); C: Conversion of the ADC at low frequency (Blue: input signal; Yellow: output response observed at the register)

connected to a logic analyzer. Sine waves at various frequencies were applied and the data was stored within the analyzer. The data was then analyzed with MATLAB. The digital code output was restored to the full scale range. Each data set was clipped and the frequency domain of the data was calculated. The signal to noise and distortion ratio and the effective number of bits was accessed. A point score histogram or code density test was utilized to evaluate the differential nonlinearity and integral nonlinearity of the ADC (figure 50) [52]. This approach is performed in the amplitude-domain of an ADC. A dynamic and repetitive signal is applied to the ADC, generating a corresponding distribution of digital codes at the output of the converter. The histogram shows how many times each different digital code word appears on the output. In the case of a sinusoidal signal, the histogram would reveal a bathtub distribution. The digitized information is then sorted into code bins. Each code bin represents a single output code. Depending on the input signal, the number of samples, or hits for each bin are collected. Any deviation from the corresponding output code distribution results in various errors that may be estimated with the histogram method. These error parameters include first and foremost DNL and INL. For an ideal ADC, each code bin width should correspond to a bit width of $FSR/2^N$, where N is the resolution of the ADC and FSR is the full-scale range of the ADC in volts. Due to the limitation of the oscilloscope, the FSR of the ADC cannot be precisely determined. The FS ranges approximately from 200 to 1589mV.

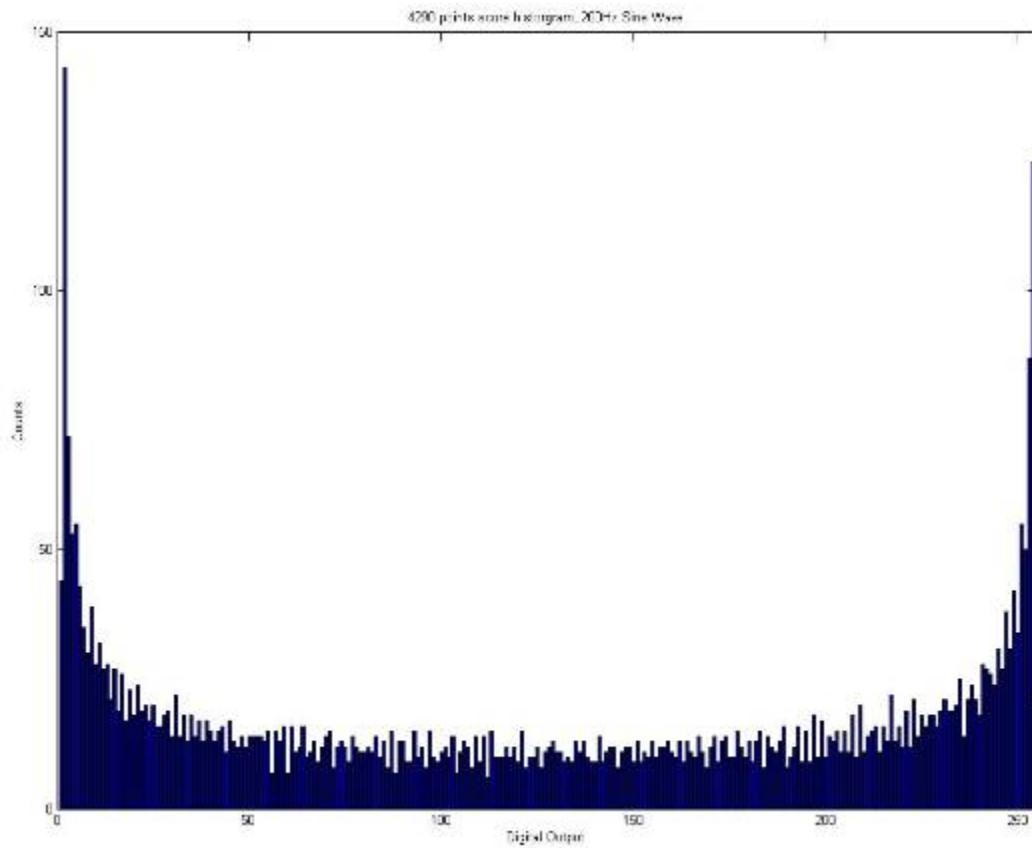


Figure 50 – Code density histogram of a 100 Hz sine wave sampled at 1.25 MSPS

The MUX was disabled and a sine wave of frequencies of 100, 200, 400, and 1kHz were input to the chip. The output of the ASIC was connected to a data acquisition card (NI PCIe-6259, National Instrument), which was connected to the PC. The DSP was carried out with MATLAB. Since the TX and RX do not transfer the clock data, a self synchronization method is used to recover the timing information. The data was over-sampled with the depth that each set contains two sets of comma signals. The over sampled data was reduced and converted to a binary signal. The comma signals were detected and the string of data between the comma signals was extracted. The data was then checked with polarity. The comma signals and the polarity bits were removed, and the string of data was transformed into a matrix. The binary data was converted to decimal. The signal was reconstructed and the characteristic of the ADC was calculated. The signal to noise and distortion ratios (SNDR) of the ADC at these frequencies are 45.3682, 42.3878, 40.7787 and 41.9988 dBFS respectively. The effective numbers of bits (ENOB) are 7.2439, 6.7654, 6.4815, and 6.6842 bits. A survey indicates that there can be up to three bits difference on some of the ADC design. The average difference from the survey was 1.43 bit [56].

As observed from the data collected, the SNDR and the ENOB drops as the frequency increases. This can contribute by two factors. First, the frequency of the OSC, which governs the sampling rate, did not increase with the increasing of the data rate. Hence, less code bin are sampled during a period of

the signal. Secondly, the memory depth of the logic analyzer did not increase with the frequencies tested; this can contribute to insufficient data points. This leads to a far less desirable point score histogram.

Differential Non-Linearity (DNL) Error is the difference between the actual measured width of the step and the ideal value of 1 LSB. The Integral Non-Linearity (INL) error represents the deviation of the actual transfer function from a straight line, such as gain and error. The results are shown in figure 50 to 53. The DNL error is roughly plus or minus 5 LSB with a standard derivation of 0.19, which indicates a monotonic transfer function with no missing code. The INL error is plus 1.28 or minus 0.17LSB with a standard derivation of 0.33. In order to avoid saturating the signal, the amplitude of the signal is slightly less than the FS. This costs an offset to the ADC transfer function characteristic, which is reflected in the INL figures 51 to 54.

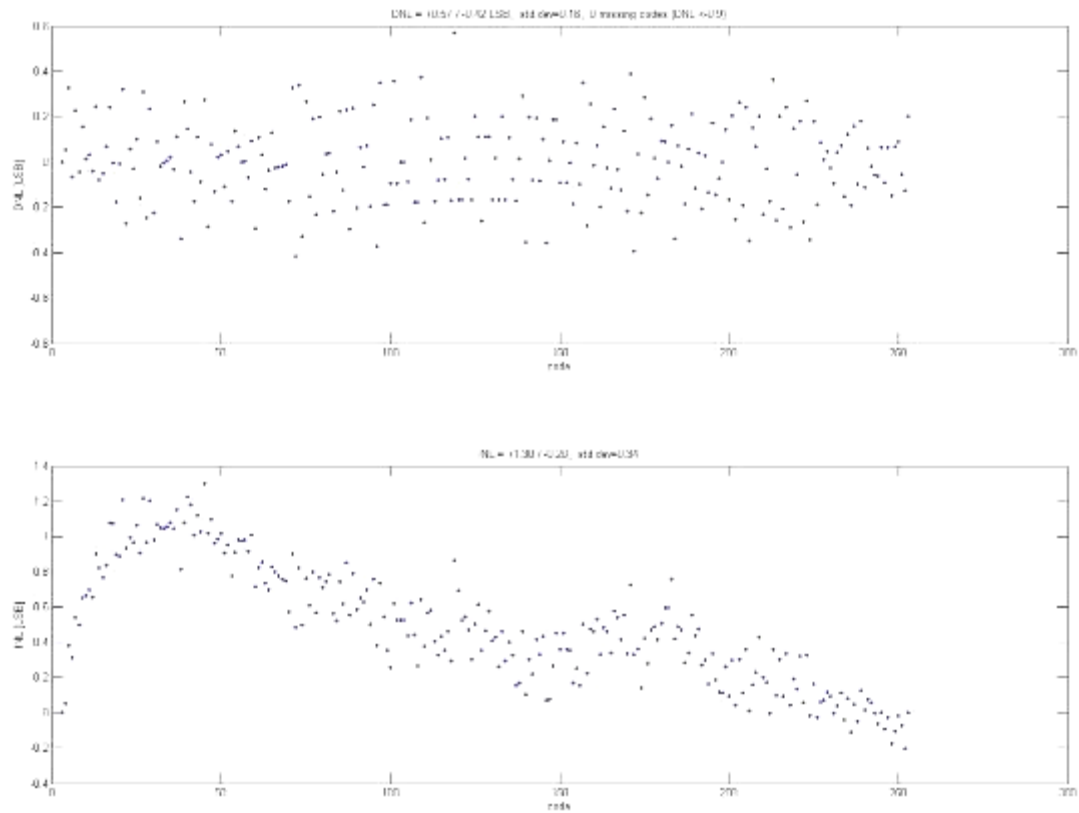


Figure 51 – DNL (Top) and INL (Bottom) of the ADC with 100Hz sine wave

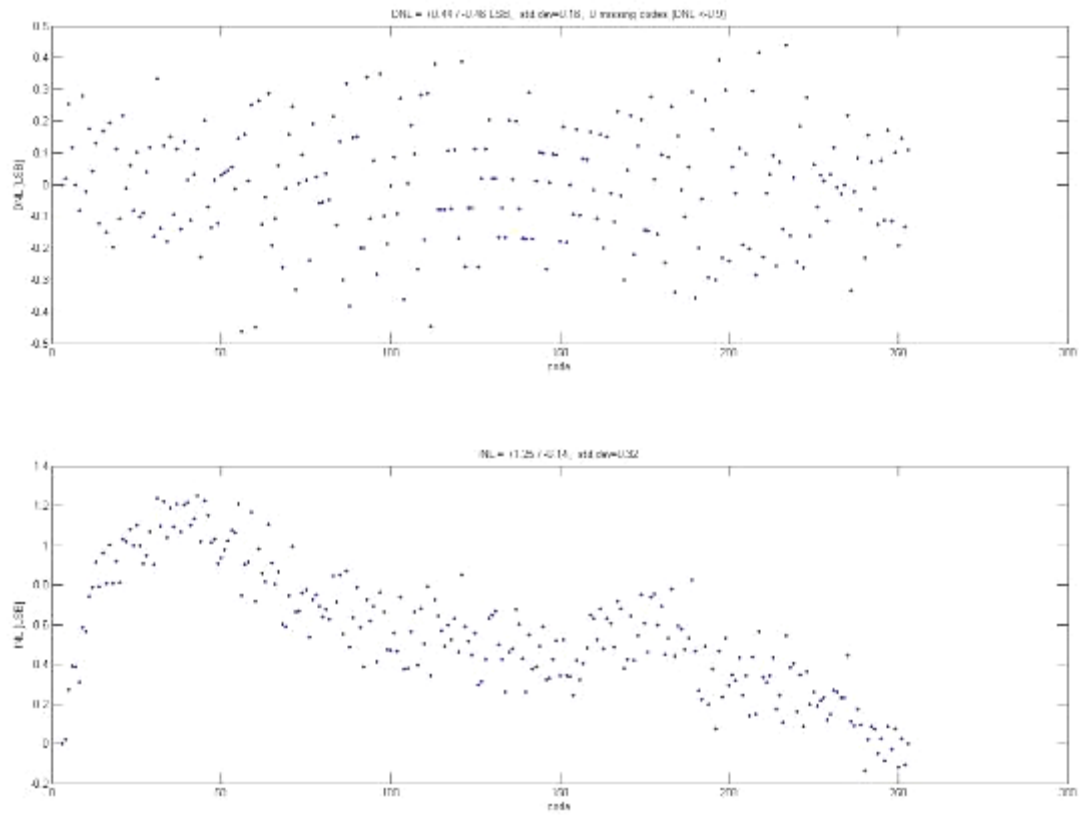


Figure 52 – DNL (Top) and INL (Bottom) of the ADC with 200Hz sine wave

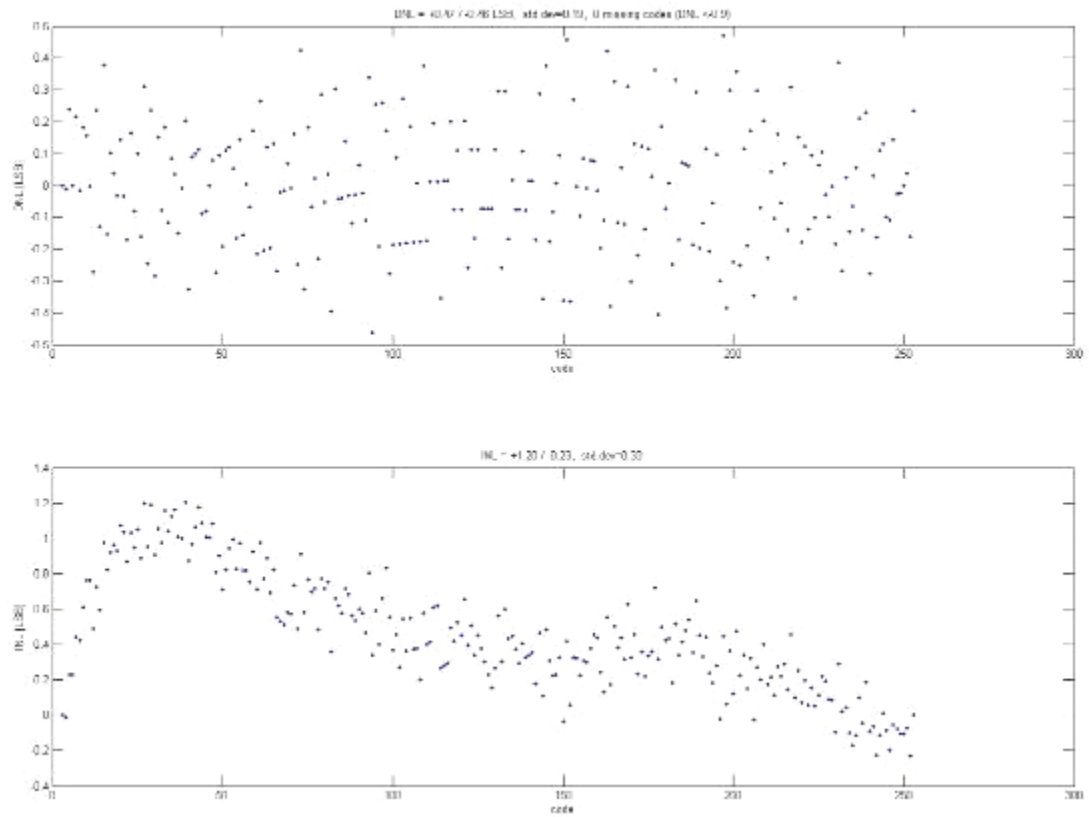


Figure 53 – DNL (Top) and INL (Bottom) of the ADC with 400Hz sine wave

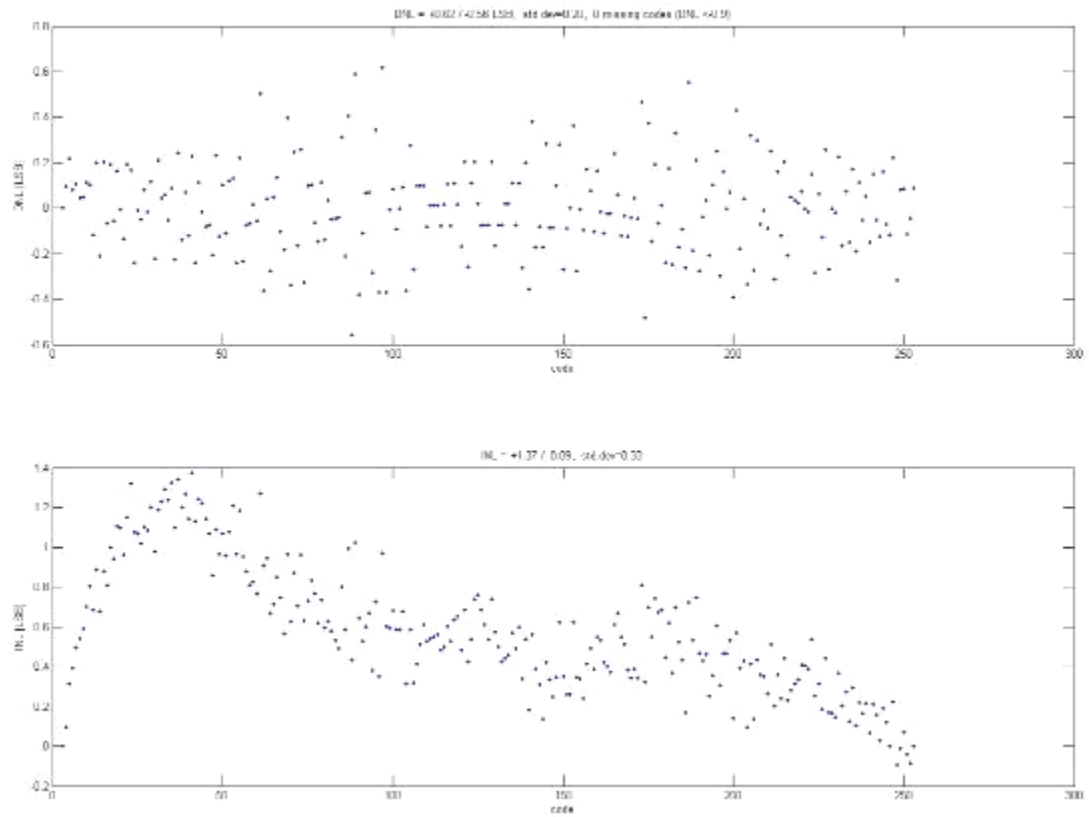


Figure 54 – DNL (Top) and INL (Bottom) of the ADC with 1kHz sine wave

5.2.8 INA Test

The detail of the performance of the INA was assessed. The INA DC output bias is 1.224V, as observed at INAref/P67. A differential signal was generated with a signal generator and a DC power source. A sine wave with 20mV peak to peak (p-p) with 1.224V offset and high impedance load output was applied to the positive input of the INA. The negative input of the INA was connected to the DC power, which was set at 1.224V. The frequency of the sine wave was increased manually and the root mean square of the voltage output was recorded. Three different external resistors, with values at 300, 510 and 1kW, were used to test the gain of the INA, which were 41, 72 and 104 respectively. The plot of the INA gain was plotted in figure 55. Based on the response shown in figure 56, the phase margin is estimated to be 65 degrees.

5.2.9 MUX Test

Due to the limitation of the packaging, only sixteen channels are connected with pins. A sine wave is input at one of the channels and the output of the MUX was observed. Figure 57 shows the output from the MUX with only one channel input. Each channel is opened for 11.65 μ s. There is a mismatch of the on-resistances of the MUX as shown in figure 58. The resistances decrease with the channels. This results from the difference in length of the trace metal

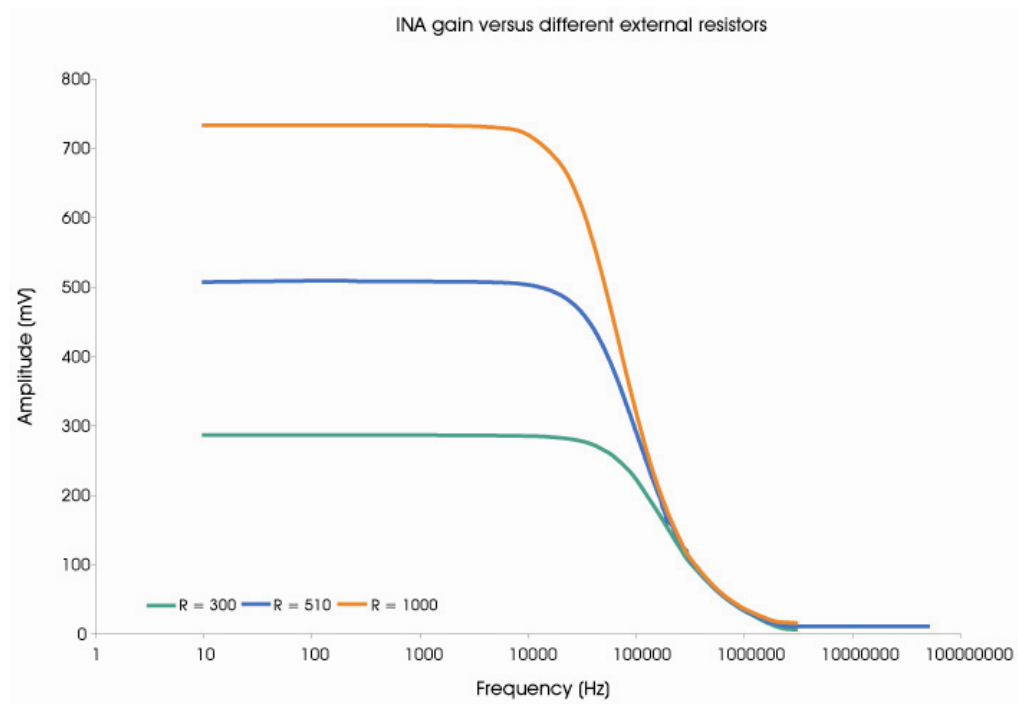


Figure 55 – INA gain with different gain resistors

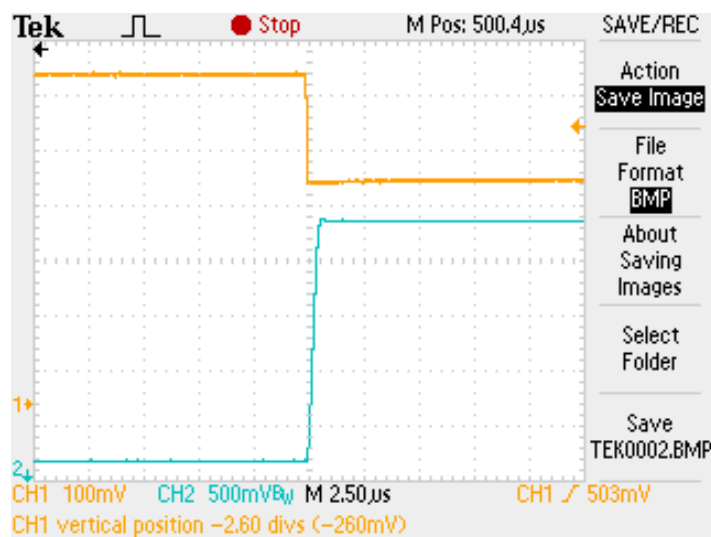


Figure 56 – Output response of the INA (Yellow: input signal, Blue: output signal)

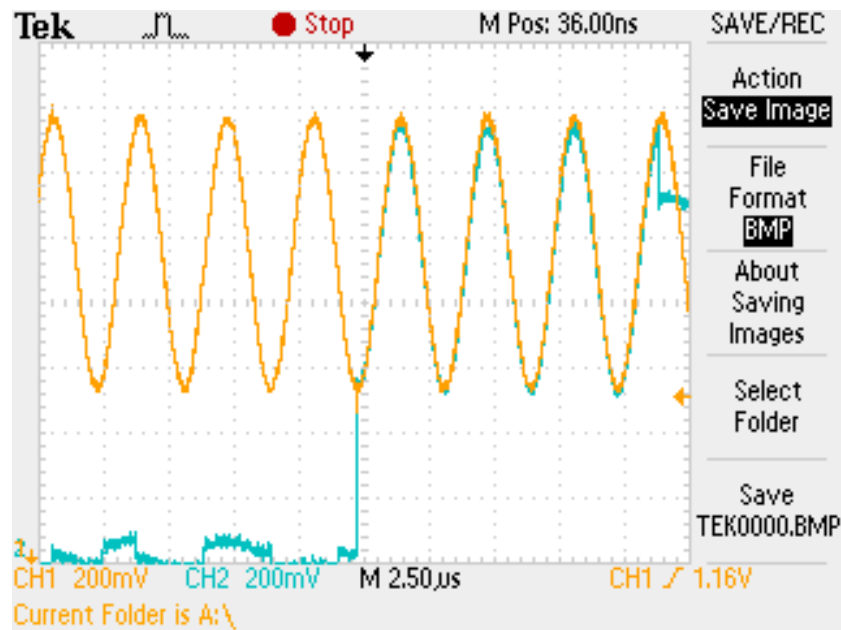


Figure 57 – Output response of the MUX (Yellow: input signal; Blue: output signal)

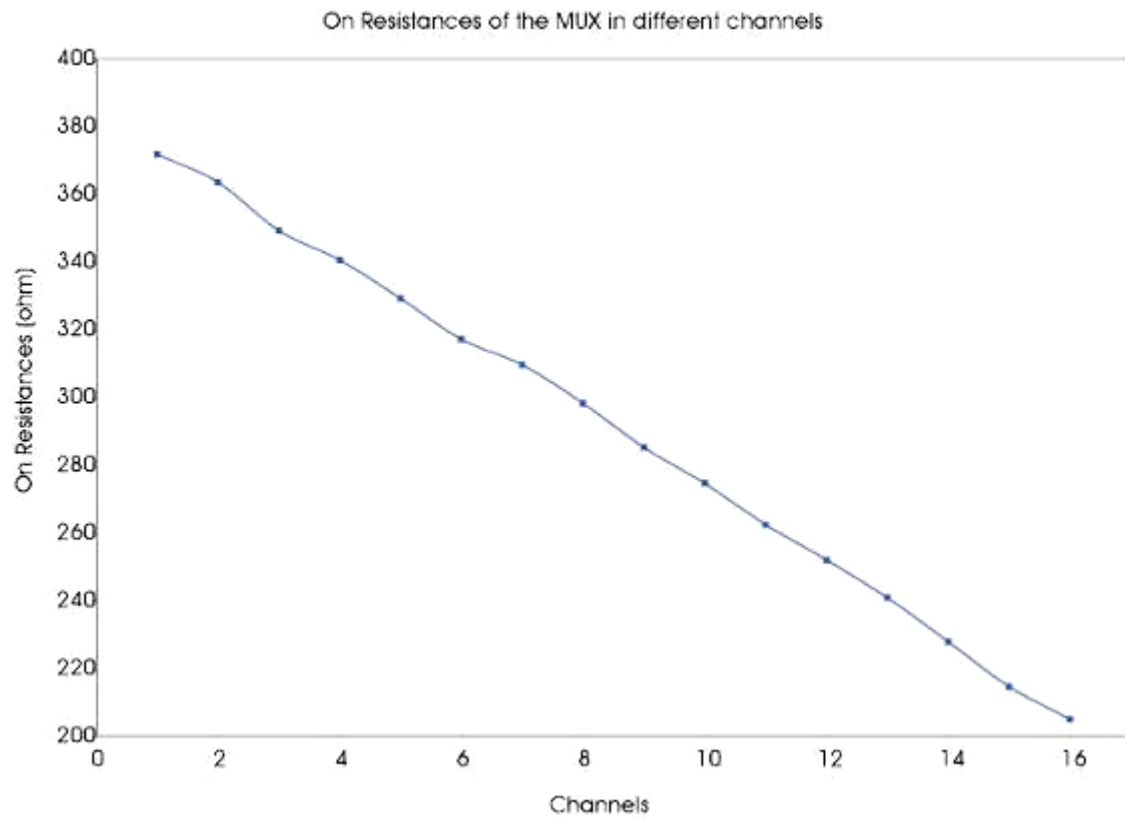


Figure 58 - Measurement of analog switch on-resistance

within the ASIC. Table 3 shows the length of metal used in each channel. These resistances by the metal connection were ignored by the simulation tools. Hence, the mismatch was never discovered during the simulation and verification during the design. The simulated resistances of the traces were recalculated and their resistances are similar to the experimental results obtained in figure 58. Hence, the on-resistances of the MUX is closed to 0 ohm and appeared to be a straight line.

5.2.10 New and Old Systems Test

The second system on the ASIC without discrete point was tested by applying a sine wave signal at one of the channels and importing the data into PC for processing. The result was the same as the discrete version of the design. The corrected system from the first iteration was also tested. However, metastability was still observed with the ADC without the latch comparator configuration.

Table 3 - Length of the metal connection in different channels

Channel	Metal (um)
1	2725
2	2607
3	2467
4	2344
5	2205
6	2094
7	2015
8	1848
9	1701
10	1568
11	1419
12	1292
13	1144
14	1008
15	851
16	725

5.3 System Testing

A testing PCB was built to evaluate the system performance of the electronics (figure 59). The goal is to evaluate the different building blocks of the system after they are connected together. Since this board is built with the goal of evaluation, many probing points were established for debugging the system.

The overall error of the ASIC can be evaluated by comparing the input waveform from the signal generator to the output digital code. A 100Hz 20mV p-p sine wave was applied to the inputs of the system. All sixteen inputs should receive the same input such that the output from the MUX to the ADC is a single sine wave function. The gain resistor is 510 ohm, which gives the system a gain of 72. The digital output of the system was sampled with a data acquisition card into the computer, where the decoding was performed. The timing delay is corrected and the result is shown in figure 60 and 61. The root mean square error of the system is 0.1145mV at input, or 8.25mV after amplification. The result from here shows that the error is slightly higher than 1 LSB, which is approximately the same as the error calculated for the ADC in section 5.2.7. As a result, we can conclude the major source of error came from the SAR ADC. The overall system RSS error includes both microcantilever (2mm EP30MED encapsulation) and ASIC is +/- 8.29mV, which is approximately +/- 1.79kPa.

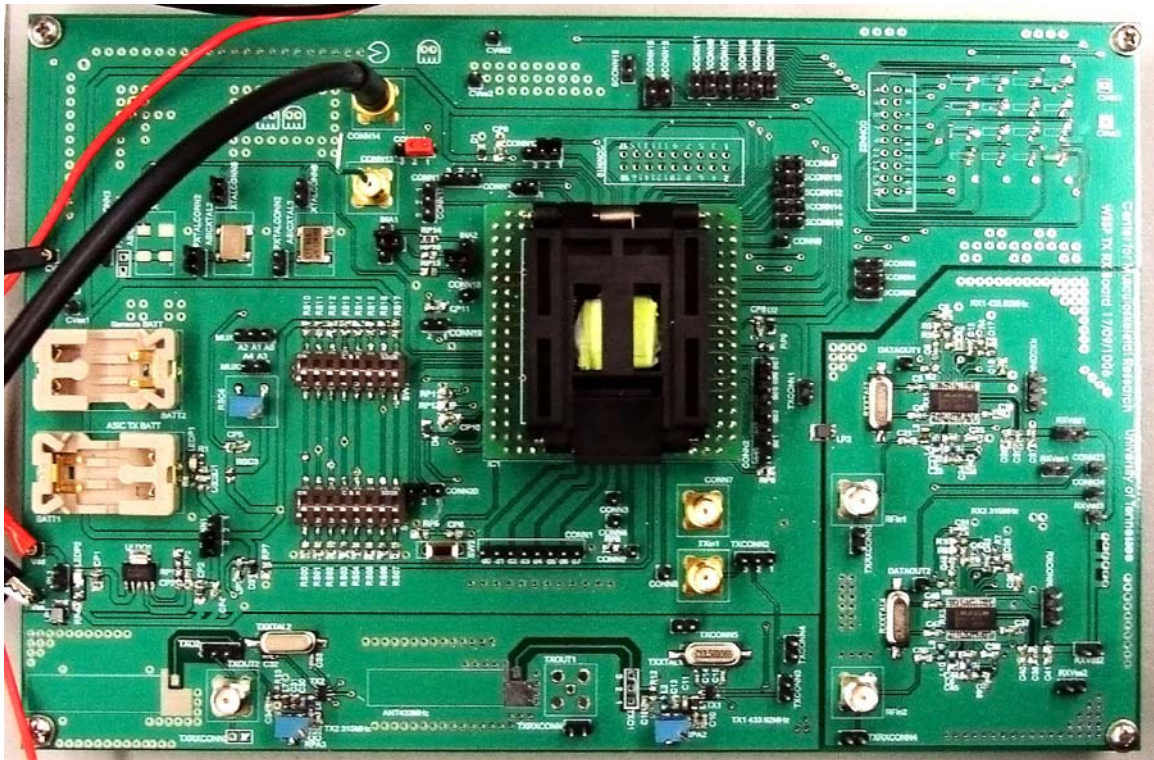


Figure 59 - System evaluation board

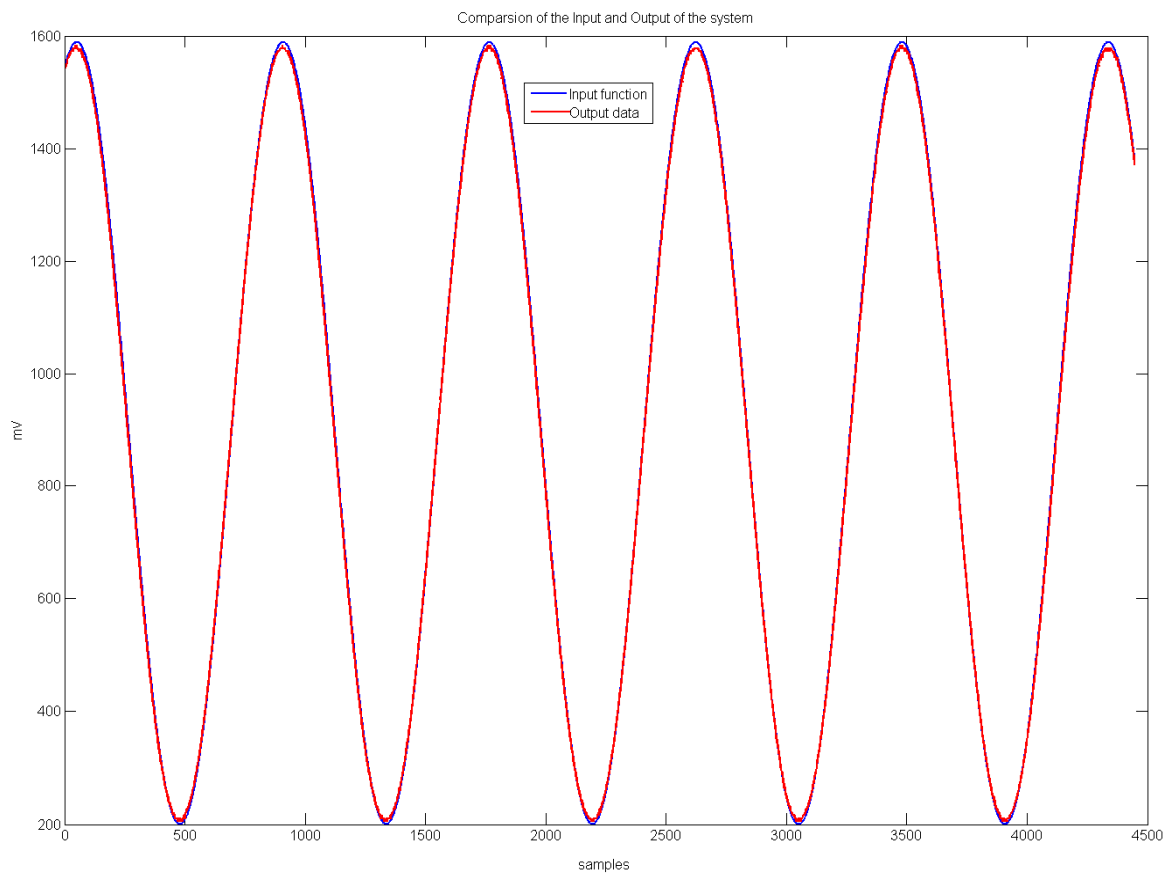


Figure 60 – Comparison between the input waveform and the reconstructed output signal (Blue: input, Red: reconstructed output)

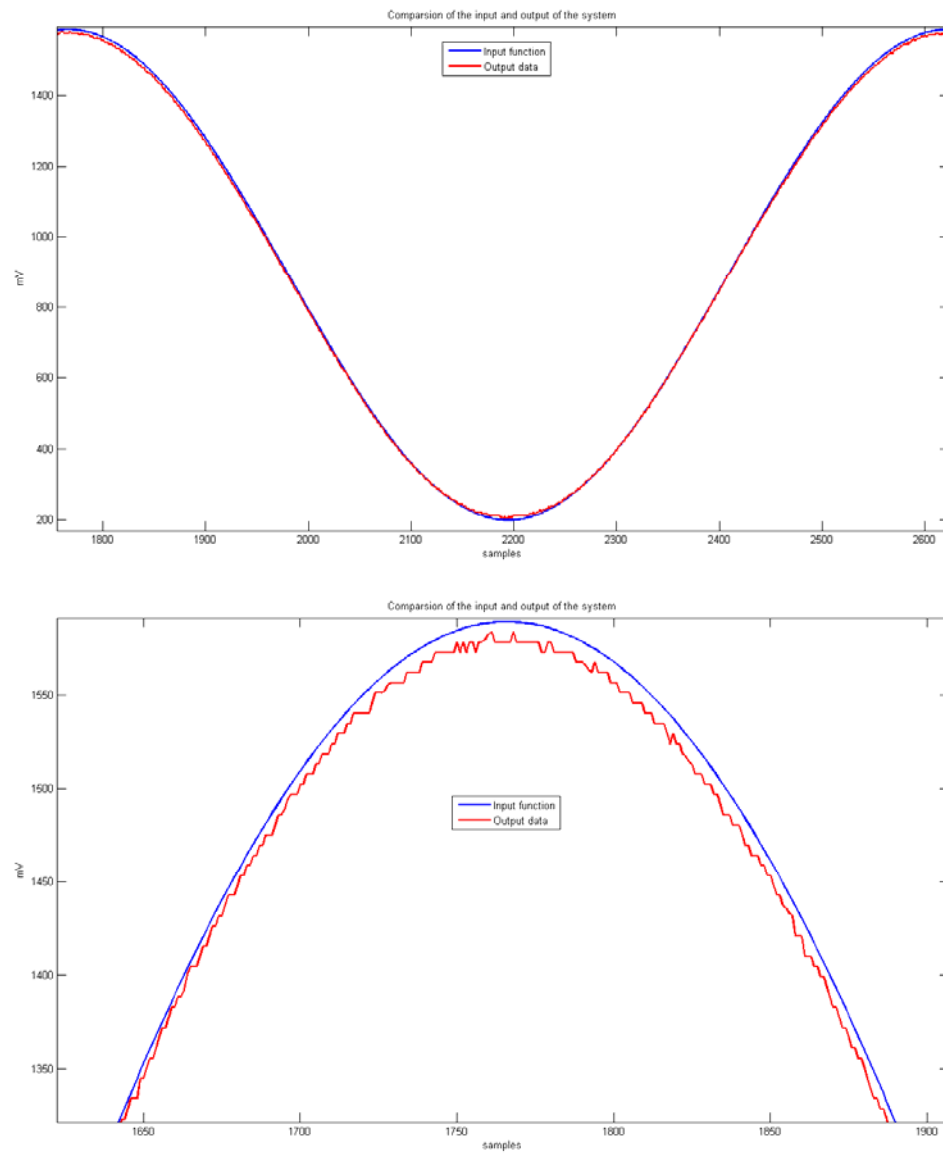


Figure 61 – Close up diagrams showing the errors created from the system (Blue: input, Red: reconstructed output)

Chapter 6

Conclusion and Future work

6.1 Conclusion

The work in this thesis demonstrates the use of a MEMs device such as microcantilever to measure the axial strain of macroscopic force with epoxy encapsulation. It is a big leap for orthopedic research, as the strain sensor has significantly reduced in size as well as increasing the resolution of the measuring surface. It has also shown the procedures and steps to design and implement a measuring system with ASIC technology. These innovations show the feasibility to implement a highly accurate and compact system in a size limited environment, such as surgical instrument. It is crucial to avoid direct contact between the sensors, electronics, and living human tissues. Biocompatible epoxy served several purposes in this system: protecting the sensors, sealing the electronic components from water, body fluids, and preventing possible allergic reaction from the materials. It has also shown that a piezoresistive microcantilever has a higher range of operation and is highly customizable as compared to FSR. The sensitivity of the sensor is determined by the thickness of the encapsulating epoxy. The readout electronics have been tested and verified.

The system properties are concluded in table 4. The feasibility of transmitting data via a telemetric system was also demonstrated.

6.2 Future Work

The future iteration of the design should integrate the wireless communication into the system. As mentioned before, due to the limitation of the packaging, only one half of the input leads to the MUX were wired to the package. The next iteration of the ASIC design should bring out all thirty input channels. Secondly, the size of the packaging should be reduced to only necessary input and outputs leads and eliminate those that are used for debugging. The coin batteries should be replaced with compact rechargeable lithium batteries. Additionally, the surface resolution can further be improved by reducing the size of the microcantilever. An automatic bridge balancing system can be realized with a series of resistors and a DAC to balance the bridge automatically at the start up of the system. Lastly, the discrete data gathered from each condylar compartment on the spacer should be converted into a smooth continuous surface stress function via bicubic Interpolation [57].

Table 4 - System parameters

Parameters	Values
Analog input channels	16
Analog MUX switching frequency	Oscillator dependent
A/D Converter input range	~ 200mV – 1589mV
A/D Converter resolution	8bit
A/D Converter rate	772 kHz
Band gap reference	1.249V
INA gain	Gain resistor dependent
INA phase margin	65°
INA Unit gain bandwidth	~ 2.4 GHz
A/D ENOB	7.24 bit
A/D SNDR	45.4 dB
A/D SFDR	56.4 dB
DNL	+0.57/-0.42 LSB
INL	+1.3/-0.2 LSB
Power supply	2.6 – 4.4V
Error checking	Parity bit evaluation
Carrier frequency	315 or 433.92MHz
Data Rate	100kbps max.
Range	Up to 10m
Modulation	ASK
Output method	RS232C

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APPENDIXES

Appendix A –Material Properties of Epoxies

Technical Data Sheet

MASTER BOND POLYMER SYSTEM EP42HT-2

Two Component, Room Temperature Curable, Heat Resistant Epoxy Adhesive, Sealant, Coating & Casting System Featuring Resistance to Medical Type Sterilization Including Radiation, Chemicals and Steam. Meets USP Class VI Requirements.

Product Description

Master Bond Polymer System EP42HT-2 is a room temperature curable two component epoxy, adhesive, sealant, coating and casting material featuring high temperature resistance along with outstanding chemical resistance. It is widely used in medical devices because of its capability of withstanding repeated sterilizations, including radiation, ethylene oxide, chemical sterilants, and steam. In addition, it fully complies with the testing requirements of USP Class VI plastics. While EP42HT-2 is a superior adhesive, sealant and coating, it is also castable to thicknesses exceeding 2-3 inches. EP42HT-2 cures readily at ambient or more quickly at elevated temperatures. One particularly popular cure schedule is “overnight” at room temperature followed by 2-4 hours at 150-200°F.

It has an easy to use 100:40 mix ratio by weight or 100:50 by volume. The cured epoxy compound is resistant to various types of sterilizations, inorganic and organic acids, alkalis, organic solvents and aromatic hydrocarbons. EP42HT-2 is an excellent electrical insulator. Especially noteworthy is its serviceability from - 60°F up to 450°F, combined with resistance to steam, chemicals and radiation. Aside from its widespread use in the medical industry, EP42HT-2 is also used in electronics, electrical, fiberoptic and optical as well as OEM type applications. To optimize physical properties including heat resistance, a post cure of 100-130°C for 2-3 hours is recommended.

Product Advantages

- Convenient non-critical 100:40 mix ratio by weight or 100:50 by volume.
 - Contains no solvents.
 - Convenient cure schedules at both ambient and elevated temperatures.
 - Outstanding resistance to medical sterilants, radiation, ETO, chemicals and steam.
 - Excellent chemical resistance to acids, alkalis and many solvents.
-

Appendix A – Material Properties of Epoxies, 141

- Superior thermal stability; serviceable up to 450°F.
- Castable to thicknesses exceeding 2-3 inches.
- Conforms to the requirements for a USP Class VI plastic.
- Available in amber-clear and black as a Class VI system.
- Service temperature -60°F/450°F

Product Properties

- Mix ratio, by weight, part A to part B..... 100/40
- Mix ratio, by volume, part A to part B 100/50
- Viscosity, mixed, 75°F, cps..... 3500
- Working life after mixing, 100 gram mass, 75°F, minutes..... 45-60
- Cure schedule
 - 75°F, 24-48 hrs
 - 200°F, 2-3 hrs
- Tensile strength, 75°F, psi..... >12,000
- Elongation, 75°F, %..... 3.4
- Tensile lap shear, Al/Al, 75°F, psi..... >2000
- Tensile modulus psi..... >450,000
- Coefficient of thermal expansion, in/in x 10⁻⁶/°C..... 35-40
- Volume resistivity, 75°F, ohm-cm..... >10¹⁴
- Dielectric constant, 75°F (60Hz)..... 3.8
- Service temperature range, °F -60 to 450°F
- Hardness, Shore D >75
- Shelf life at 75°F, in unopened containers..... 6 months
- Parts A and B available in syringes, pints, quarts, gallons and five gallon containers.

Special Chemical Resistance Data

Resistant at Room Temperature, 77°F (immersion): Acetic acid (10%), Ammonium hydroxide (29%), Butyl alcohol, Calcium hypochlorite (5%), Citric acid (10%), Cottonseed oil, Distilled water, Ethylene glycol, Formaldehyde (37%), Gasoline (98% octane), Hydrochloric acid (10%), Hydrogen peroxide (20%), Lard, Linseed oil, Mineral oil, Phosphoric acid (10%), Propylene glycol, Sea water, Sodium hydroxide (20%), Sodium hydroxide (50%), Sodium sulfite (1%), Sour crude oil, Sulfuric acid (10%), Tap water, Toulene, Zinc hydrosulfite (1%).

Resistant at 200°F (immersion): Citric acid (10%), Ethylene glycol, Hydrochloric acid (10%), Mineral oil, Phosphoric acid (10%), Propylene glycol.

Satisfactory Resistance to Spillage Above 200°F: Carbon tetrachloride, Ethyl alcohol, Gasoline, Hydrochloric acid (10%), O-dichlorobenzene (10%), Sodium hydroxide (10%), Sulfuric acid (10%), Tap water, Xylene.

Preparation of Compound and Bond Surfaces

Master Bond Polymer System EP42HT-2 is prepared for use by thoroughly mixing part A with part B in a noncritical 100 to 40 mix ratio by weight or 100 to 50 by volume. Mixing should be done slowly to avoid trapping air. The working life of a mixed 100 gm batch is 45-60 minutes. It can be further lengthened by using shallow mixing vessels or mixing smaller size batches. All bonding surfaces should be carefully cleaned, degreased and dried to obtain maximum bond strength. Certain metal or plastic surfaces should be mechanically or chemically etched in order to maximize bond strength. Castings can be accomplished in rubber, plastic or metal molds after application of appropriate mold releases. When casting, vacuum degassing may be necessary to eliminate all air bubbles.

Application and Assembly

For potting and casting the EP42HT-2 is readily pourable. For bonding or sealing EP42HT-2 can be conveniently applied with a brush, paint roller, spatula or knife. Enough mixed adhesive should be applied to obtain a final adhesive bond line thickness of 4-6 mils. This can be accomplished by coating one surface with an adhesive film 4-6 mils thick or by coating the two surfaces, each with a 2 to 3 mil thick layer of adhesive. Porous surfaces may require somewhat more adhesive to fill the voids than non-porous ones. Thicker glue lines do not increase the strength of a joint but do not necessarily give lower results since EP42HT-2 does not contain any volatiles. The parts to be bonded should then be pressed together with just enough pressure to maintain intimate contact during cure.

Cure

Master Bond Polymer System EP42HT-2 can be cured at room temperature or at elevated temperatures as desired. At room temperature, Master Bond Polymer System EP42HT-2 develops 85% of its maximum bond strength within 24-48 hours. The bond strength then increases continuously for another 2-3 days. Faster cures can be realized at elevated temperatures, 2-3 hours at 200°F for full strengths. When potting, the thicker the section, the faster the rate of cure.

Handling and Storage

All epoxy resins should be used with good ventilation. Skin contact should be minimized. To remove resin or hardener from skin use mild solvent then wash

with soap and water. If material enters the eyes, flood with water and consult a physician. Optimum storage is at or below 75°F in closed containers. No special storage conditions are necessary. Containers should however be kept closed when not in use to avoid contamination. Cleanup of spills and equipment is readily achieved with acetone or xylene employing proper precautions of ventilation and flammability.

Master Bond Inc.

Adhesives, Sealants & Coatings • 154 Hobart Street • Hackensack, N.J. 07601-3922 • Tel: 201-343-8983

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Technical Data Sheet

MASTER BOND POLYMER ADHESIVE EP30 MEDICAL

Low Viscosity, Two Component Epoxy Adhesive For High Performance General Purpose Bonding, Coating and Sealing for Medical and Food Grade Applications

**Conforms Title 21 U.S. Code of Federal Regulations, FDA Chapter 1,
Section 175.105 and 175.300 Requirements
Now Meets USP Class VI Specifications**

Product Description

Master Bond Polymer Adhesive EP30 Medical is a low viscosity, two component epoxy adhesive for general purpose bonding formulated to cure at room temperature or more rapidly at elevated temperatures, with a four (4) to one (1) mix ratio by weight. This adhesive is 100% reactive and does not contain any solvents or other volatiles. It is especially recommended where low viscosity is required for ease of application and bonded assemblies must exhibit superior dimensional stability. The EP30 Medical has exceptionally low linear shrinkage. (0.0003 inches/inch.)

Master Bond Polymer Adhesive EP30 Medical produces high strength, rigid bonds which are remarkably resistant chemicals including water, oil and most organic solvents, as well as sold sterilants ETO and gamma radiation. Adhesion to both similar and dissimilar materials including metals, glass, ceramics, wood, vulcanized rubbers and many plastics is excellent. The hardened adhesive is an electrical insulator. Color of part A is clear, part B clear. The temperature range is -60 to 250°F.

Product Advantages

- Convenient mixing: easy-to-use mix ratio, four (4) to one (1) by weight, very low viscosity.
 - Easy application: contact pressure only required for cure; adhesive spreads evenly and smoothly.
 - Versatile cure schedules: ambient temperature cures or fast, elevated temperature cures as required.
 - High bonding strength to a wide variety of substrates.
 - Superior durability, and chemical resistance particularly to sterilants.
-

Appendix A – Material Properties of Epoxies, 145

- Biocompatible as per USP Class VI testing.
- Conforms Title 21 U.S. Code of Federal Regulations, FDA Chapter 1, Section 175.105 and 175.300 Requirements.

Product Properties

- Mixing ratio, by weight, parts A to B 4/ 1
- Part A properties, typical viscosity, cps at 25°C 600-700
- Part B properties, typical viscosity, cps at 25°C 400
- Working life after mixing, 75°F, 100 gram mass, minutes 30-35
- 200 gram mass, minutes 20-25
- Cure schedule, room temperature: 85% of maximum strength developed within 24-48 hours
- Ultimate strength attained after 5-7 days
- Cure schedule, elevated temperatures: at 40°C (104°F) 16-24 hours
- Or 100°C (212°F) 2-3 hours
- Bond strength, shear, aluminum to aluminum, room temperature cure, 75°F, psi 3200
- Bond strength, shear, aluminum to aluminum, room temperature cure, 75°F, psi
- After 30 days water absorption 3120
- Tensile strength >9500
- Volume resistivity >10¹⁴
- Dielectric strength 440 volts/mil
- Tensile modulus 400,000
- Service temperature range, °F -60°F to +250°F
- Shelf life at 75°F, in unopened containers 1 year
- Parts A and B available in pint, quart, 1 (one) gallon and 5 (five) gallon containers.

Preparation of Adhesive and Bonding Surfaces

Master Bond Polymer Adhesive EP30 Medical is prepared by thoroughly mixing part A with part B. in a four (4) to one (1) mix ratio by weight. Mixing should be done slowly to avoid entrapping air. The low viscosity of the two components makes mixing easy. The working life of a mixed 100 gram batch is approximately 30 to 35 minutes and that of a 200 gram batch 20-25 minutes. It can be substantially lengthened by using shallower mixing vessels or mixing smaller size batches. All bonding surfaces should be carefully cleaned, degreased and dried for obtaining maximum bond strengths. Also when bonding to certain metal surfaces, vulcanized rubbers, etc., chemical etching should be employed for optimal adhesion and environmental durability. Non-porous surfaces should be roughened with sandpaper or emery paper for hard materials.

Adhesive Application and Assembly

Master Bond Polymer Adhesive EP30 Medical can be conveniently applied with a brush, paint roller, spatula, knife, etc. Enough mixed adhesive should be applied to obtain a final adhesive bond line thickness of 3-5 mils. This

can be accomplished by coating one surface with an adhesive film 3-5 mils thick or by coating the two surfaces, each with a 1.5 to 2.5 mil thick layer of adhesive. Porous surfaces may require somewhat more adhesive to fill the voids than non-porous ones. Thicker glue lines do not increase the strength of a joint but do not necessarily give lower results as the EP30 Medical adhesive system does not contain any volatiles. The parts to be bonded should then be pressed together with just enough pressure to obtain and maintain intimate contact during cure.

Cure

Master Bond Polymer Adhesive EP30 Medical can be cured at room temperature or at elevated temperatures as desired. At room temperature Master Bond Polymer Adhesive EP30 Medical develops 85% of its maximum bond strength within 24-48 hours. The bond strength then increases continuously for about a week. Faster cures can be realized at elevated temperatures, e.g., 16-24 hours at 40°C (104°F) or 2-6 hours at 100°C (212°F) for full strengths. Remove excess adhesive promptly before it hardens with a spatula. Then wipe with rag and solvent such as trichloroethylene, toluene or lacquer acetone. The thinner the section of epoxy, the slower the rate of cure.

Handling and Storage

All epoxy resins should be used with good ventilation, also skin contact should be minimized. Master Bond Polymer Adhesive EP30 Medical employs a low toxicity-low skin irritation "safety" hardener. To remove resin or hardener from skin, use solvent, then wash with mild soap and water. If material enters the eyes, flood with water and consult a physician. Optimum storage is at or below 75°F in closed containers. No special storage conditions are necessary. Containers should however be kept closed when not in use to avoid contamination. Cleanup of spills and equipment is readily achieved with chlorinated, aromatic or ketone solvents employing proper precautions of ventilation and flammability.

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Technical Data Sheet

MASTER BOND POLYMER SYSTEM EP21LV

Versatile Two Component, Low Viscosity Epoxy System For High Performance Bonding, Sealing, Coating, Encapsulation & Casting. Conforms Title 21, U.S. Code of Federal Regulations, FDA Chapter 1, Section 175.105 & 175.300 for Food Applications

Meets USP Class VI Specifications for Medical Applications

Product Description

Master Bond Polymer System EP21LV is a two component, low viscosity epoxy resin system for high performance bonding, sealing, coating, encapsulation and casting. It is formulated to cure readily at room temperature or more quickly at elevated temperatures. It has a very forgiving 1 to 1 mix ratio by weight or volume. In fact, EP21LV has the unusual characteristic of being able to adjust the properties of the cured system by altering the mix ratio. Adding more A part (e.g. 2:1 mix ratio) gives a more rigid cure (enhanced machinability) while adding more B part (e.g. 1:2 mix ratio) gives a more forgiving cure (greater impact resistance). The EP21LV produces high strength, durable bonds which hold up well to thermal cycling and resists many chemicals including water, oils, fuels, acids, bases and salts. It is serviceable over the wide temperature range of -65°F to +250°F. It bonds well to a variety of substrates including metals, glass, ceramics, wood, rubbers, and many plastics. Once cured, EP21LV is an outstanding electrical insulator. This, coupled with its low viscosity, makes it an excellent encapsulating and potting epoxy. As a Class VI epoxy, EP21LV has a wide range of uses as an adhesive, sealant or coating in the medical industry. In addition, it meets FDA requirements for food compatibility. EP21LV contains no solvents or diluents. While the standard color of the cured material is amber-clear, a wide variety of additional color choices are also available.

Advantages

- Convenient mixing: non critical 1:1 mix ratio by weight or volume.
 - Variable mix ratio feature allows adjusting the type of cure. Adding more A (e.g. 2:1) gives a more rigid cure while adding more B (e.g. 1:2) gives a more forgiving cure.
 - Easily applied; product flows evenly and smoothly without application of pressure, wets surfaces and fills volumes quickly and completely.
 - Ambient temperature cures or fast elevated temperature cures as required.
 - High bonding strength to a wide variety of substrates.
 - Superior physical strength properties.
 - Good electrical insulation properties; ideal for potting and encapsulation.
-

Appendix A – Material Properties of Epoxies, 148

- Fully meets UPS Class VI requirements for medical applications.
- Fully meets FDA requirements for food related applications.

Product Properties

- Mixing ratio, weight or volume, parts A to B 1/1
- Mixed viscosity, 75°F, cps 7000-8000
- Working life after mixing, 75°F, 200 gram mass, minutes 60-75
- 1 quart mass, minutes 35-40
- Cure schedule, room temperature, 90% of maximum strength developed within 24-36 hours
- 150°F, 90% of maximum strength developed within 3-4 hours
- Bond strength, shear, aluminum/aluminum
- Room temperature cure, 75°F, psi >2900
- After 30 days water immersion, 75°F, psi >2800
- Tensile strength, 75°F, psi 7600
- Elongation %, 75°F 4.8
- Tensile modulus, 75°F, psi 320,000
- Hardness, Shore D >70
- Coefficient of thermal expansion, in/in x 10⁻⁶/°C 53
- Dielectric constant, 75°F, (1 KHz) 2.89
- Volume resistivity, 75°F, ohm-cm 10¹⁵
- 24 hour water boil, % weight gain 3.2
- Service temperature range, °F -65°F to +250°F
- Shelf life at 75°F, in unopened containers (Commercial Grade) 1 year
- Shelf life at 75°F, in unopened containers (Food or Medical Grade) 6 months
- Parts A and B available in pints, quarts, 1(one) gallon, and 5(five) gallon containers.

Preparation of Compound and Bond Surfaces

Master Bond Polymer System EP21LV is prepared for use by thoroughly mixing part A with part B in a noncritical one-to-one (1:1) mix ratio by weight or volume. Mixing should be done slowly to avoid trapping air. The working life of a mixed 200 gm batch is 60-70 minutes and that of a 1 quart batch is 35-40 minutes. It can be further lengthened by using shallow mixing vessels or mixing smaller size batches. All bonding surfaces should be carefully cleaned, degreased and dried to obtain maximum bond strength. Also when bonding to metal surfaces especially, chemical etching should be employed when the bonded joints are to exhibit optimal environmental durability. Nonporous surfaces can be advantageously roughened with sandpaper or emery paper for hard materials. Castings can be accomplished in rubber, plastic or metal molds after application of approximate mold releases.

Application and Assembly

For potting and casting the EP21LV is readily pourable and can be processed by conventional methods to produce high quality castings. For bonding or sealing, EP21LV can be conveniently applied with a brush, paint roller, spatula, knife, etc. Enough mixed adhesive should be applied to obtain a final adhesive bond line thickness of 3-5 mils. This can be accomplished by coating one surface with an adhesive film 3-5 mils thick or by coating the two surfaces, each with a 1.5 to 2.5 mil thick layer of adhesive. Porous surfaces may require somewhat more adhesive to fill the voids than non-porous ones. Thicker glue lines do not increase the strength of a joint but do not necessarily give lower results as the EP21LV epoxy resin system does not contain any volatiles. The parts to be bonded should then be pressed together with just enough pressure to maintain intimate contact during cure. In addition, Master Bond Polymer System EP21LV can produce excellent protective coatings on both metallic and nonmetallic surfaces. Since this epoxy resin compound does not contain any solvents or other volatiles, thick coatings (10 mils and more) can readily be deposited with only one application. Furthermore, such coatings are free from pinholes and other defects.

Cure

Master Bond Polymer Adhesive EP21LV can be cured at room temperature or at elevated temperatures as desired. At room temperature, Master Bond Polymer Adhesive EP21LV develops 90% of its maximum bond strength within 24-36 hours. The bond strength increases continuously for 1-2 days. Faster cures can be realized at elevated temperatures e.g., 3-4 hours at 150°F, 60-75 minutes at 250°F or 30-40 minutes at 300°F for realizing about 90% of ultimate strength. At room temperature bonds then continue to gain in strength with full strength reached within 1 day. Remove excess adhesive promptly before it hardens with a spatula. Then wipe with a rag and solvent such as xylene, toluene or lacquer thinner. The thinner the layer of epoxy, the slower the cure.

Handling and Storage

All epoxy resins should be used with good ventilation and skin contact should be minimized. Master Bond EP21LV employs a low toxicity hardener. To remove resin or hardener from skin, use solvent, then wash with mild soap and water. If material enters the eyes, flood with water and consult physician. Optimum storage is at or below 75°F in closed containers. No special storage conditions are necessary. Containers should however be kept closed when not in

use to avoid contamination. Cleanup of spills and equipment is readily achieved with aromatic or ketone solvents employing proper precautions of ventilation and flammability.

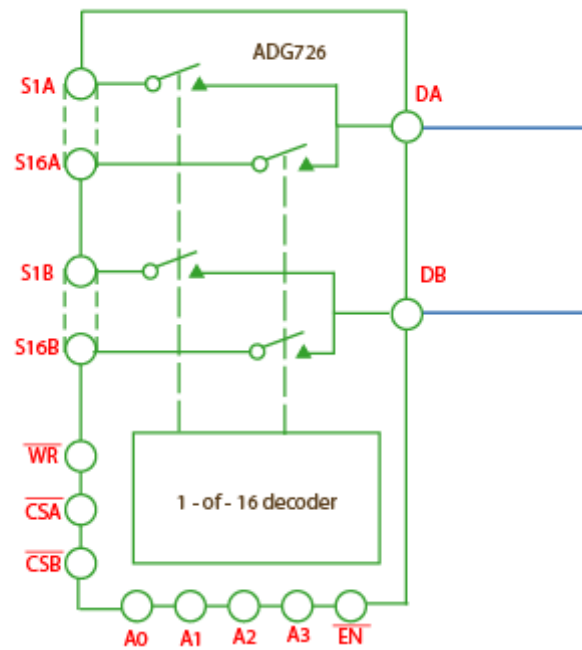
Master Bond Inc.

Adhesives, Sealants & Coatings • 154 Hobart Street • Hackensack, N.J. 07601-3922 • Tel: 201-343-8983

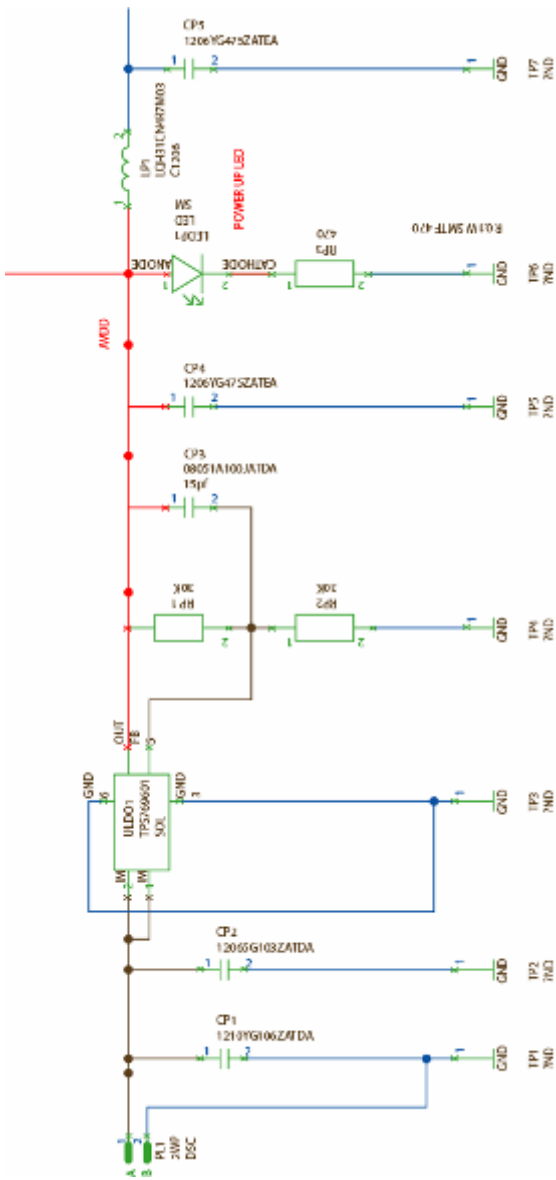
Internet Address: <http://www.masterbond.com>

➔Notice: *Master Bond believes the information on the data sheets are reliable and accurate as is technical advice provided by the company. Master Bond makes no warranties (expressed or implied) regarding the accuracy of the information, and assumes no liability regarding the handling and usage of this product.*

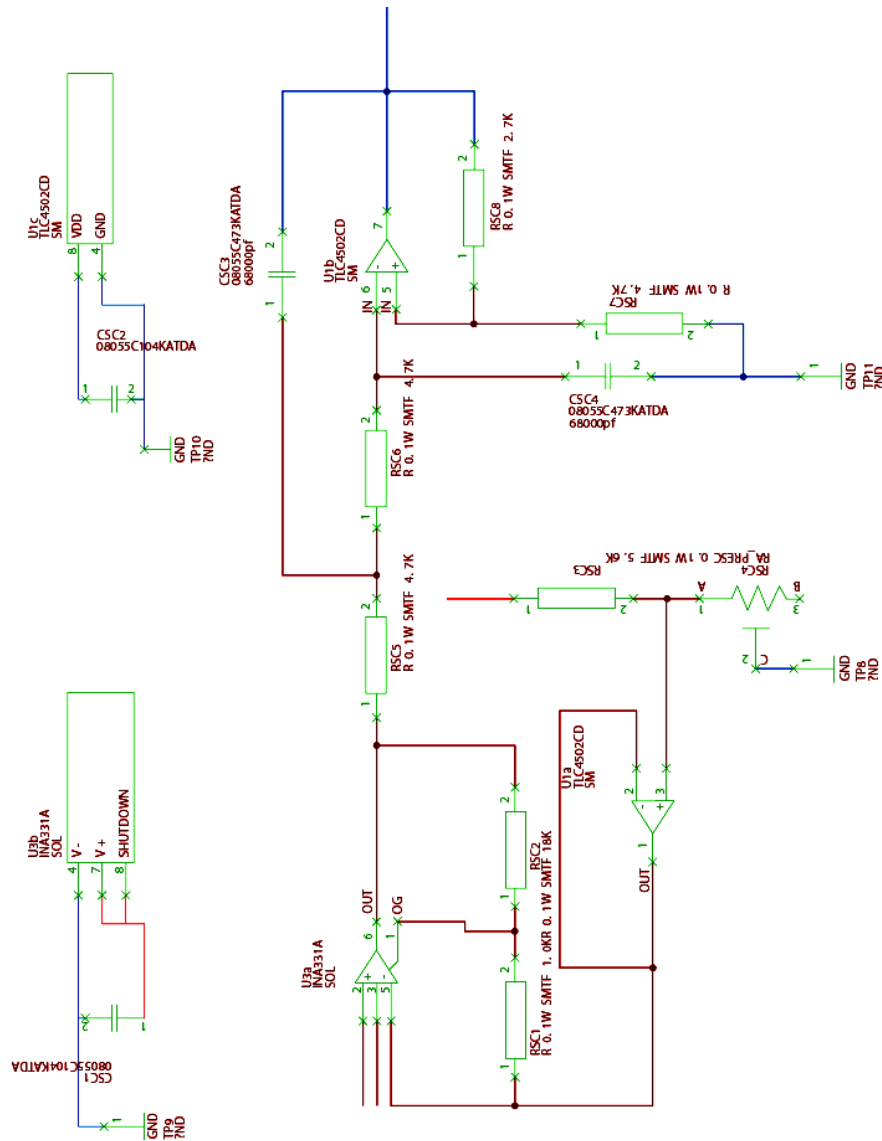
Appendix B – Schematic and PCB Layout



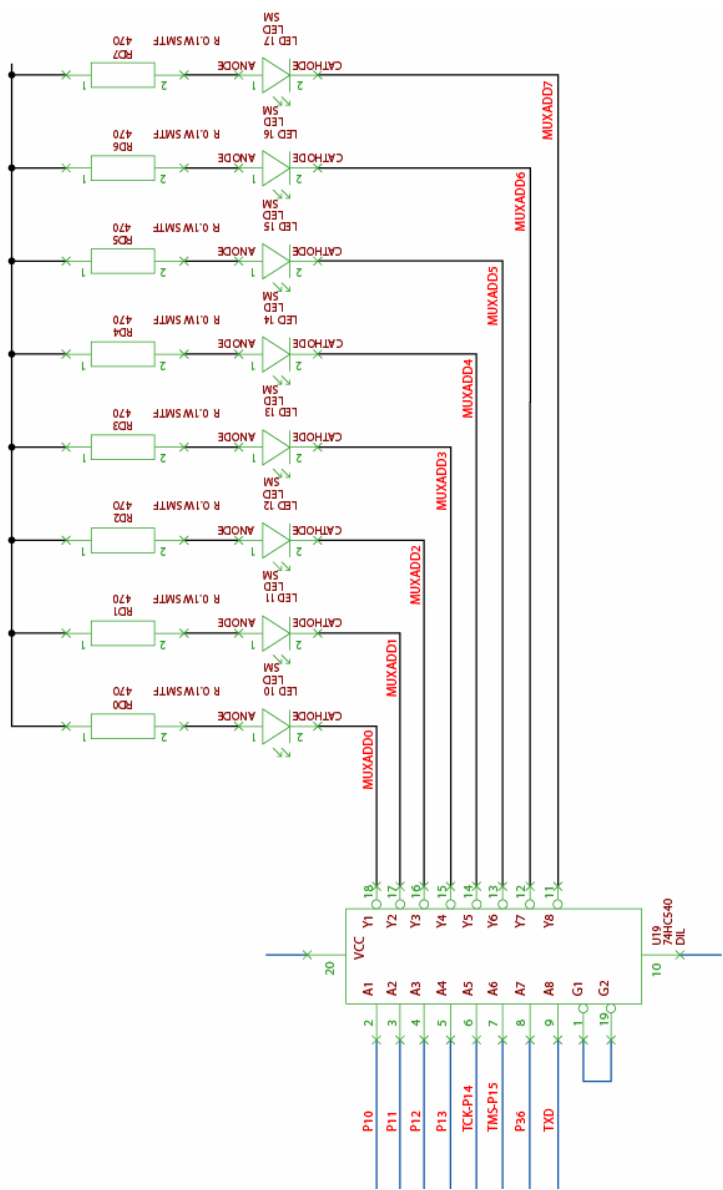
MUX circuit schematic



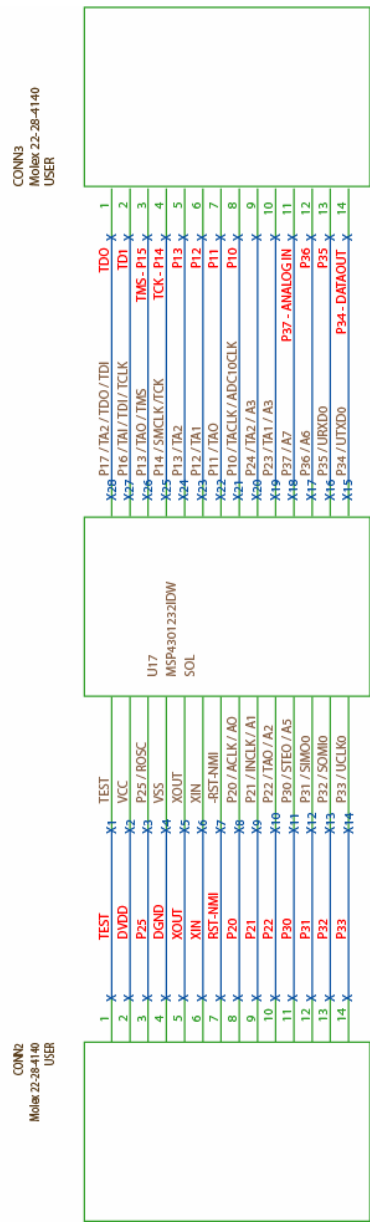
Power control circuit schematic



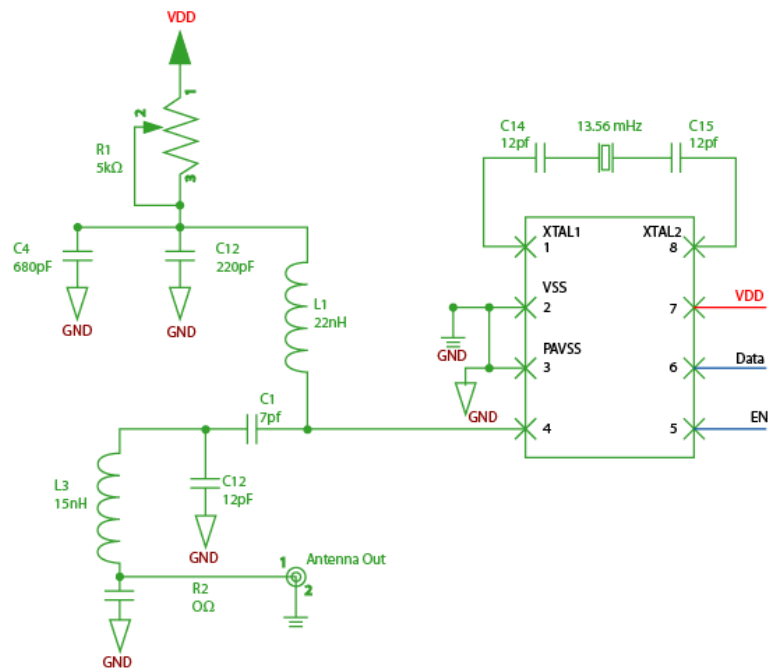
Signal conditioning circuit schematic (LPF and INA)



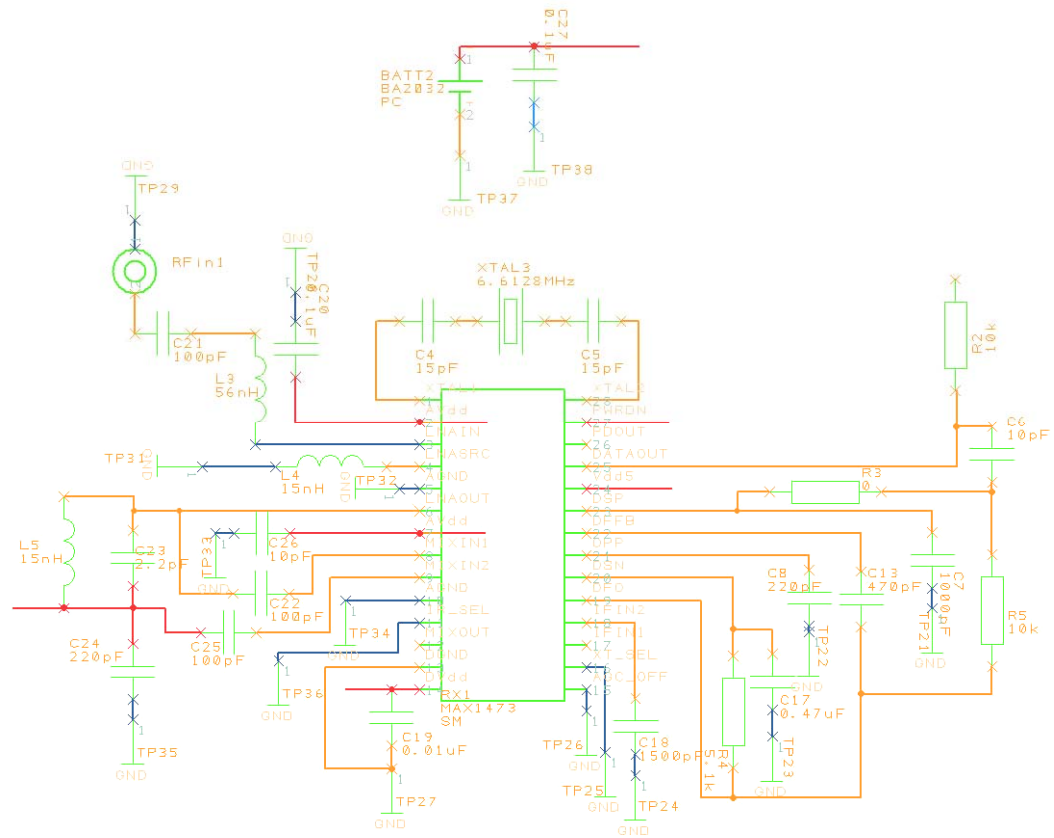
LED display circuit schematic



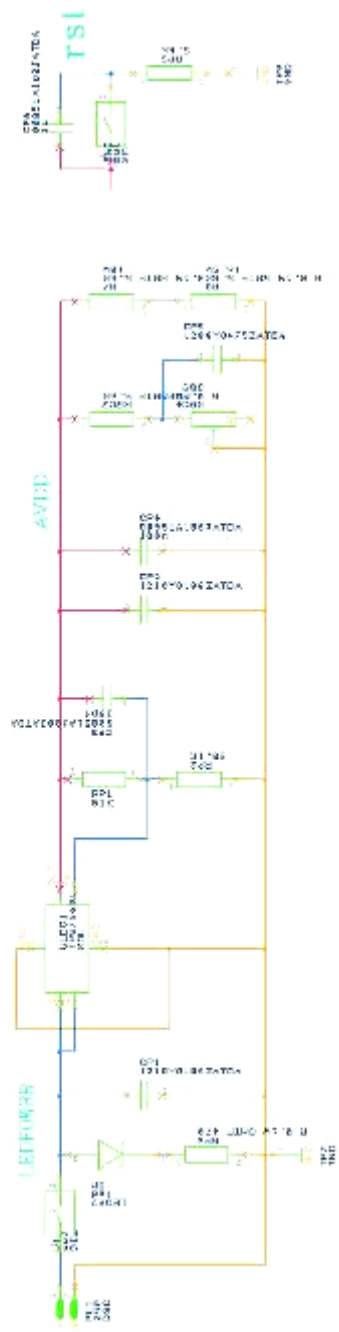
MCU circuit schematic



TX circuit schematic

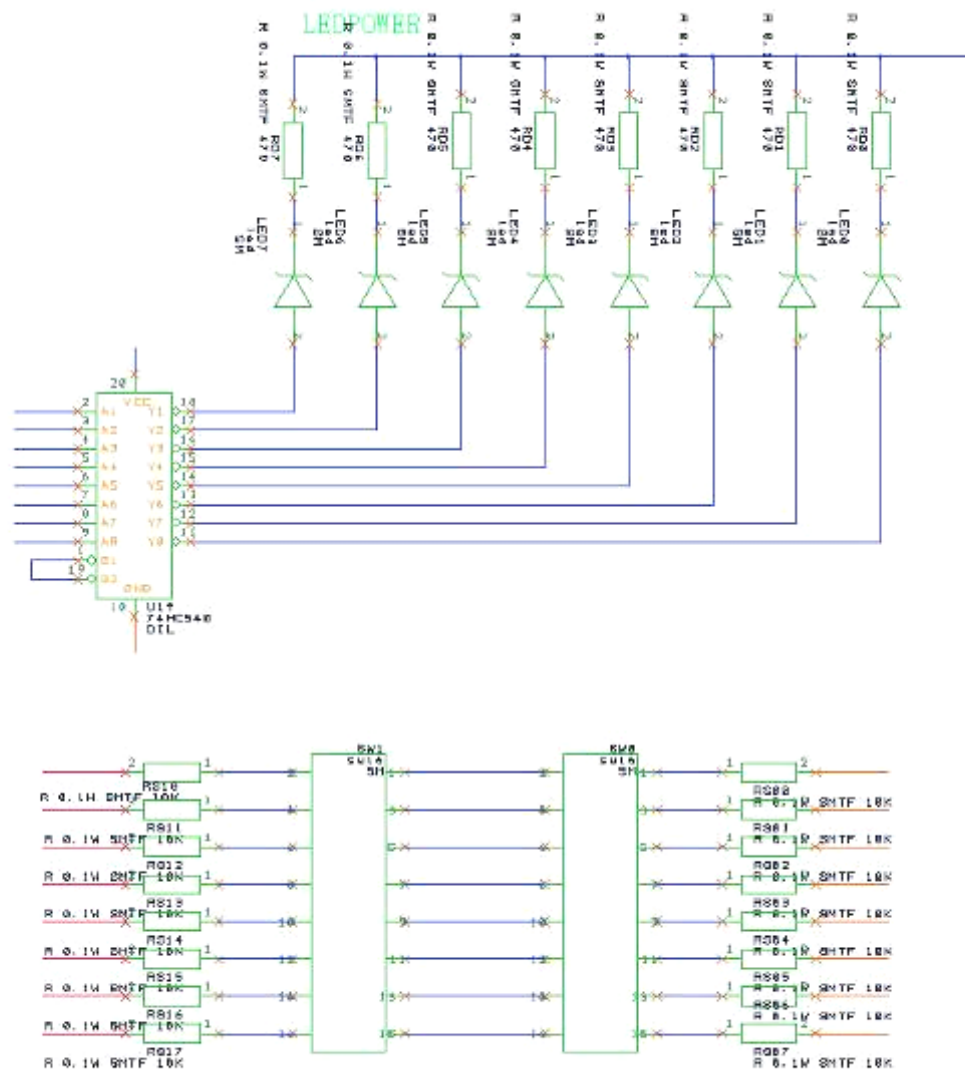


RX circuit schematic

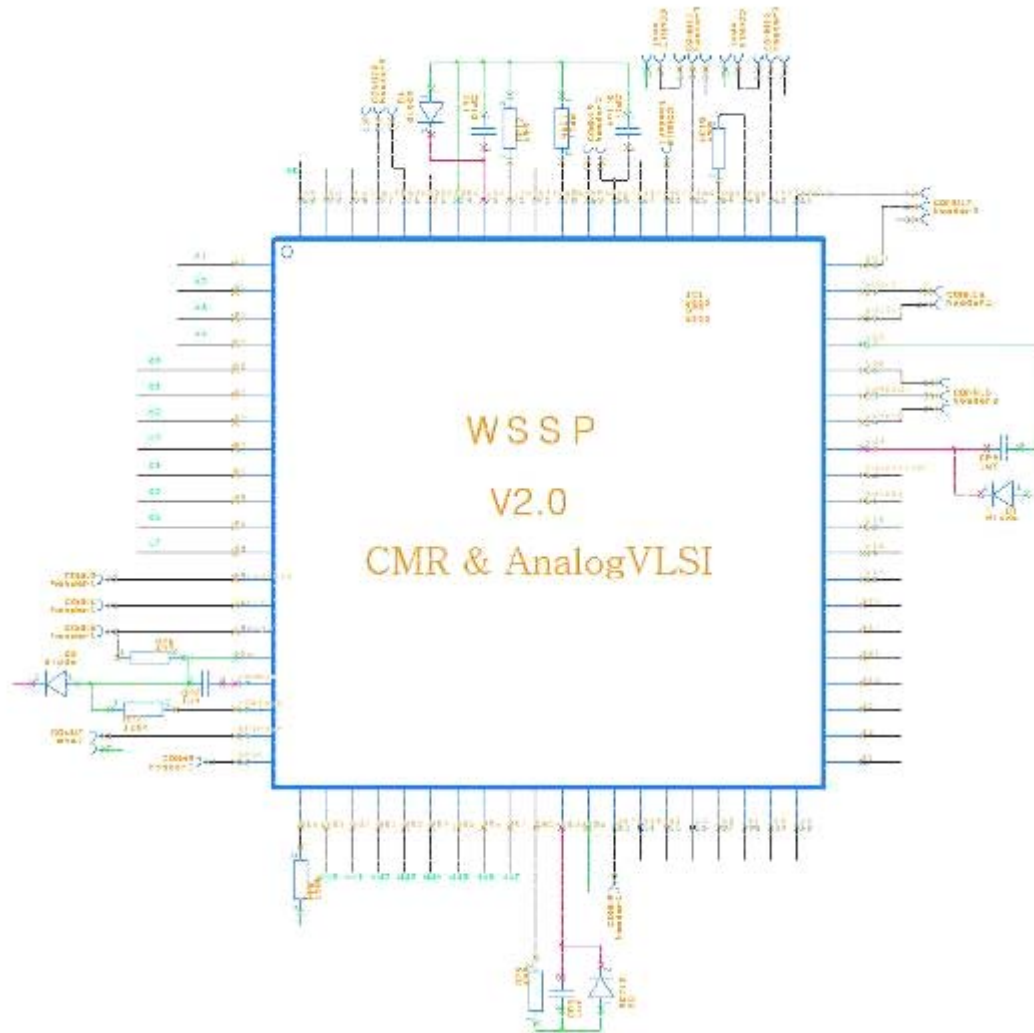


Power and reset circuit schematic

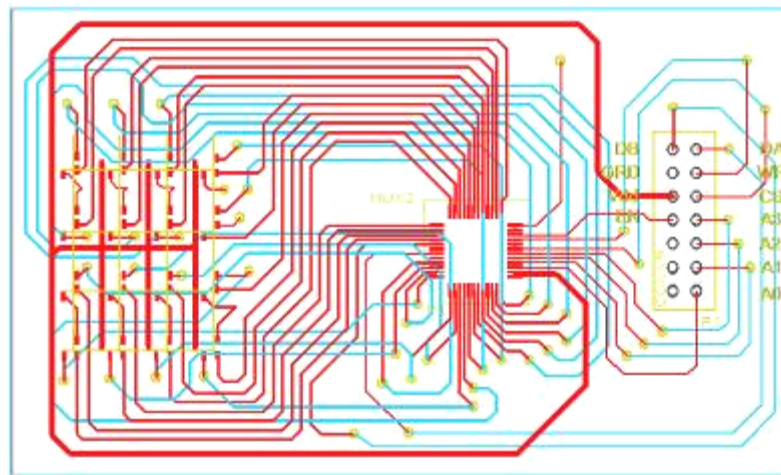




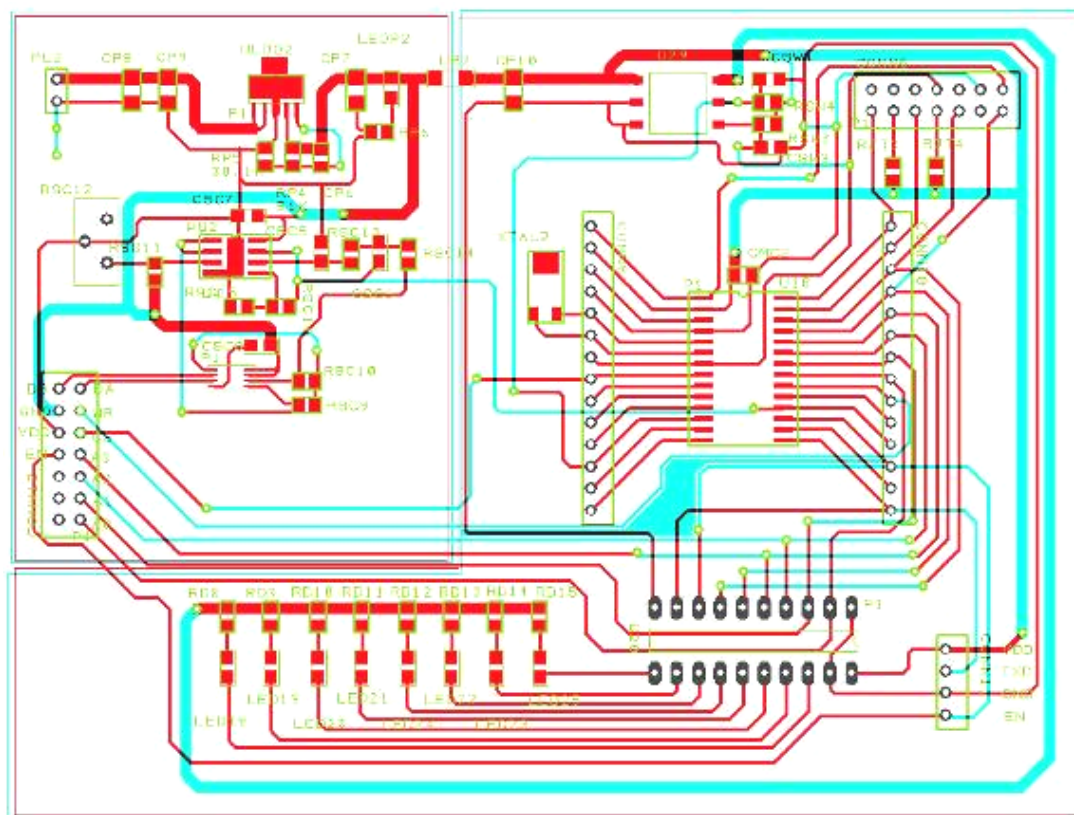
Led display and dac test circuit schematic



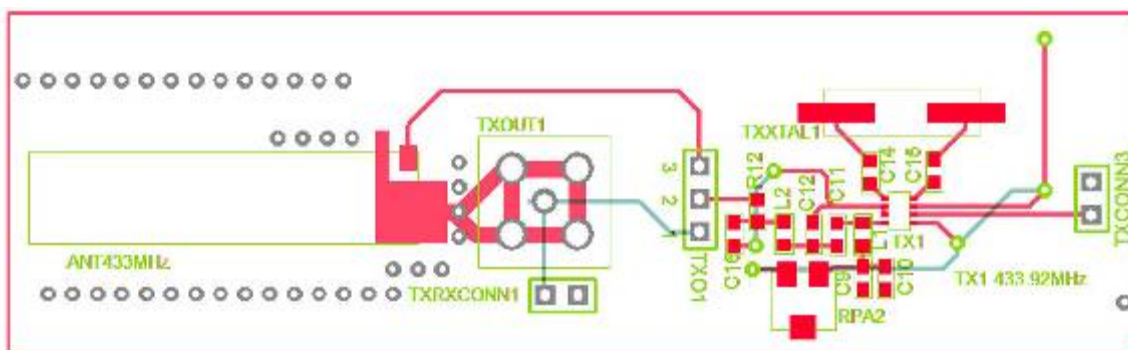
ASIC version 2 evaluation schematic



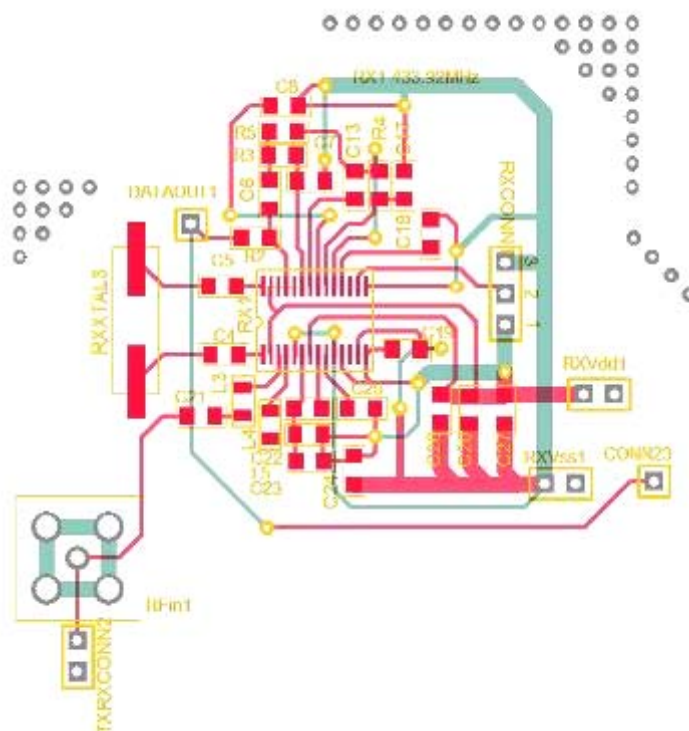
PCB Layout for MUX Board Evaluation



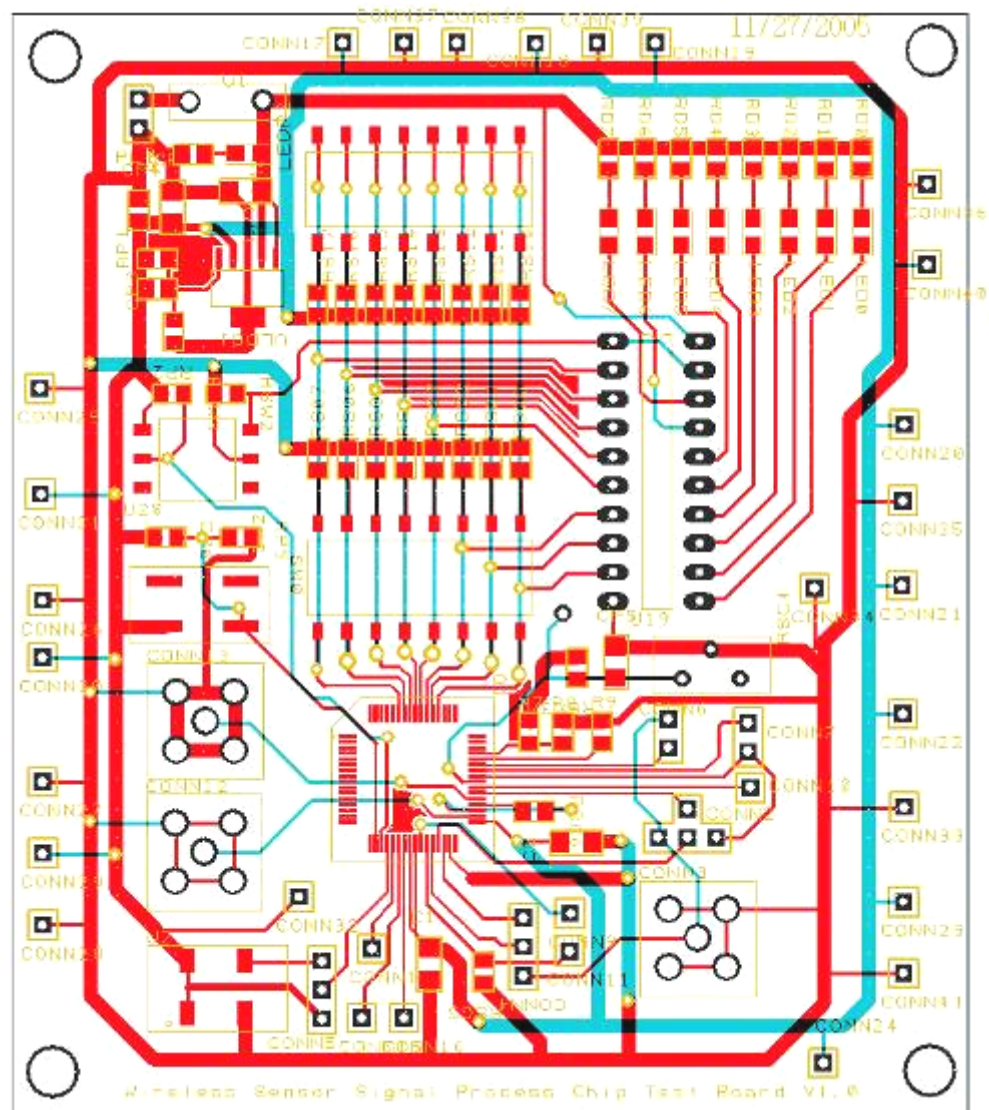
PCB Layout for MCU Board Evaluation



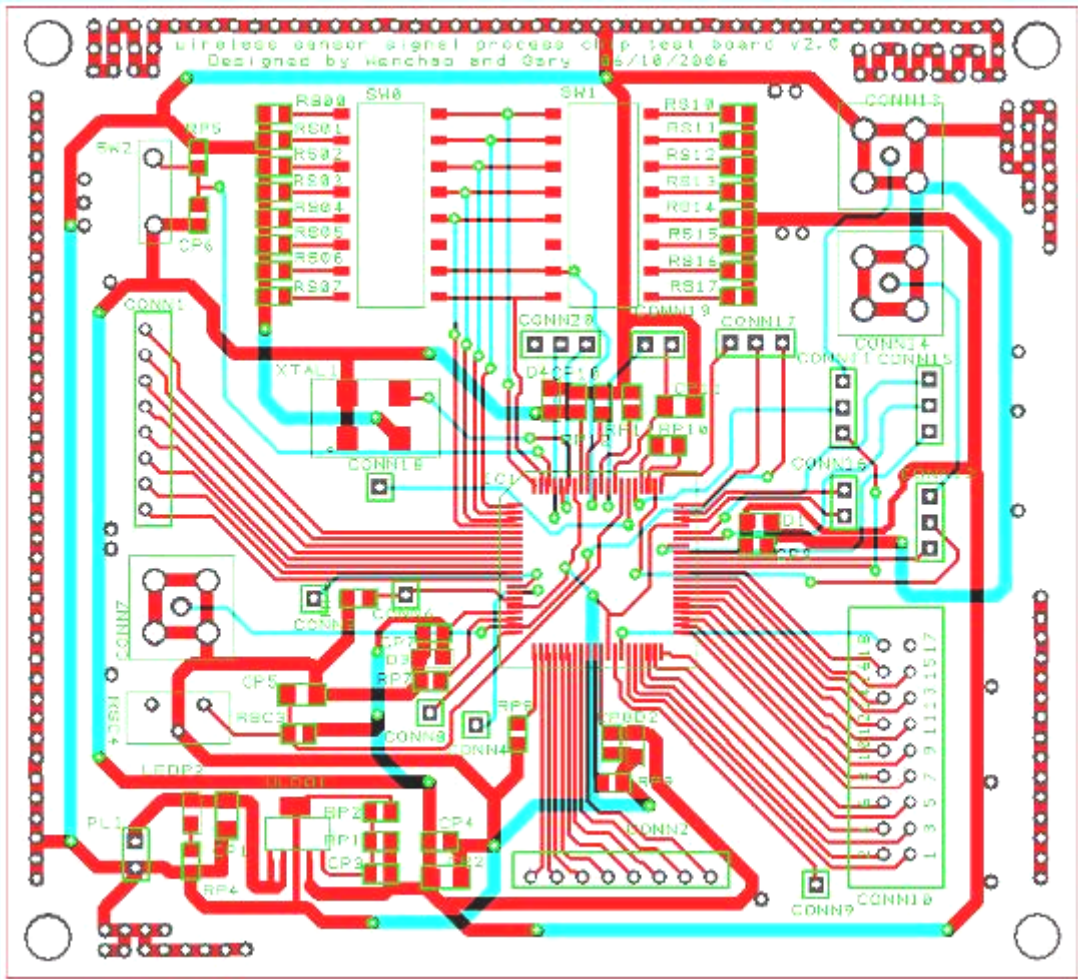
PCB Layout for TX Board Evaluation



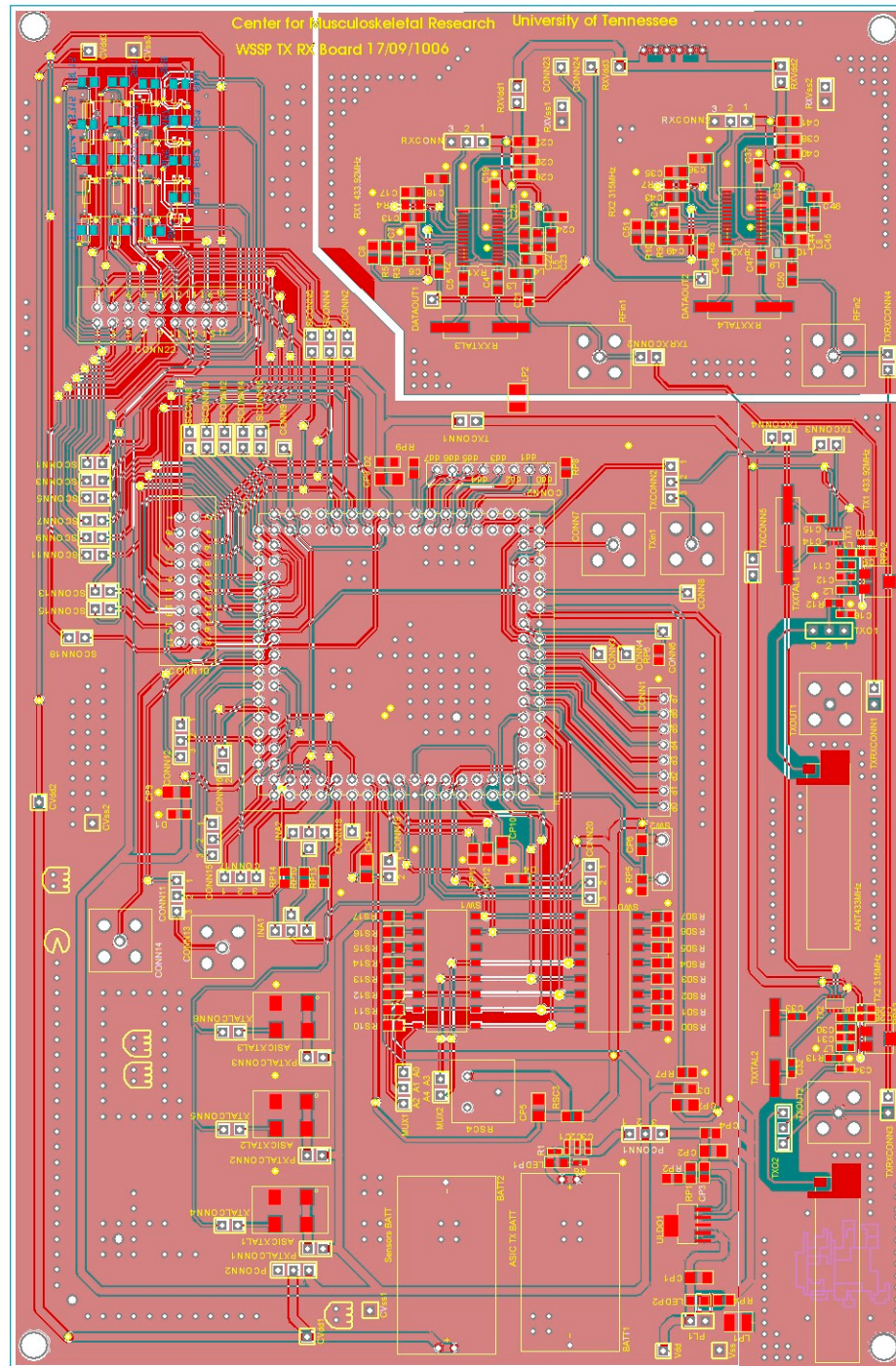
PCB Layout for RX Board Evaluation



PCB layout for the ASIC version 1 evaluation

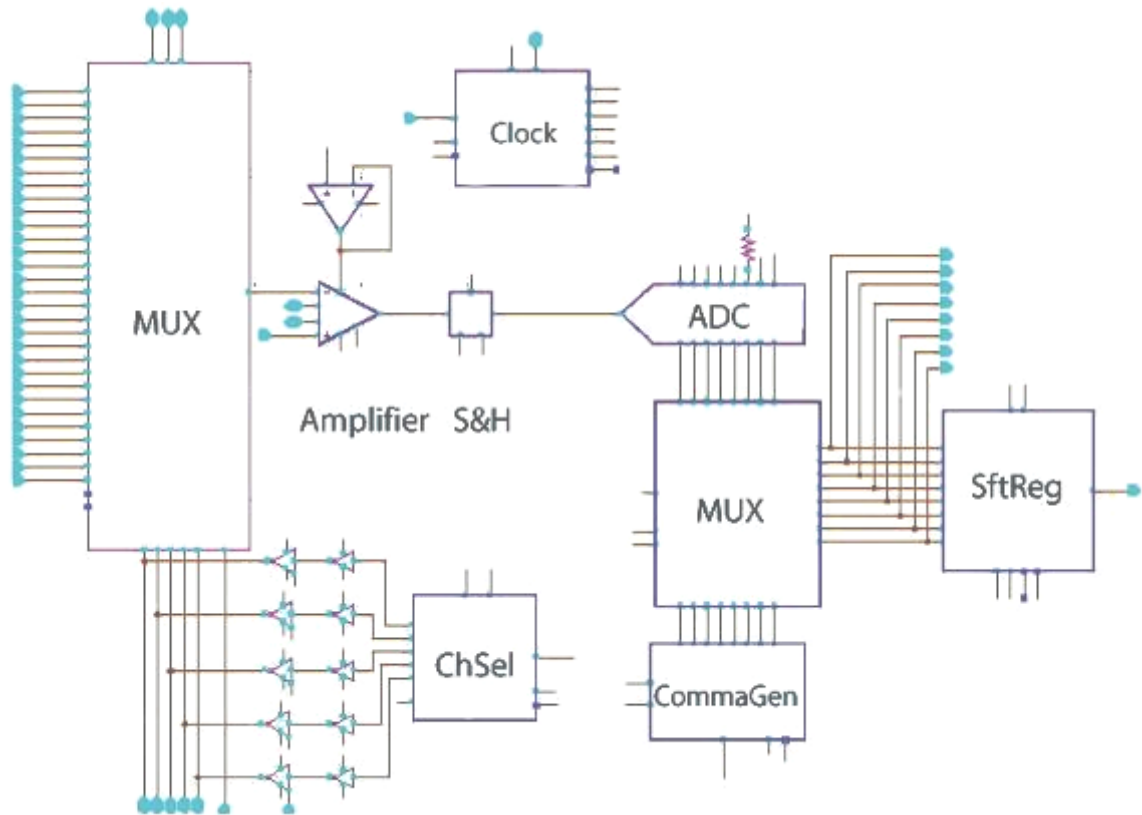


PCB layout for the ASIC version 2 evaluation

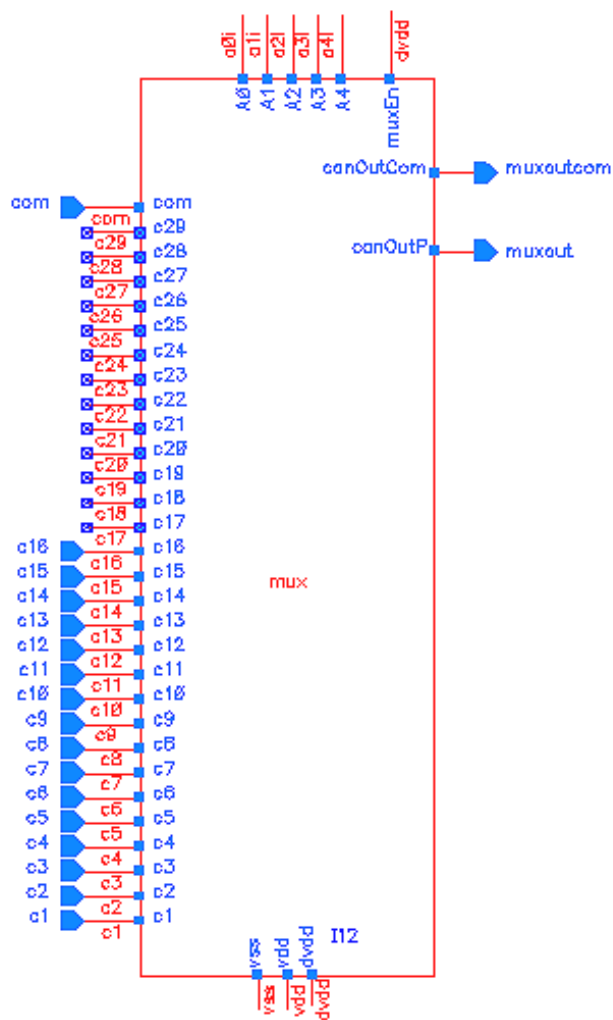


PCB layout for the ASIC system evaluation

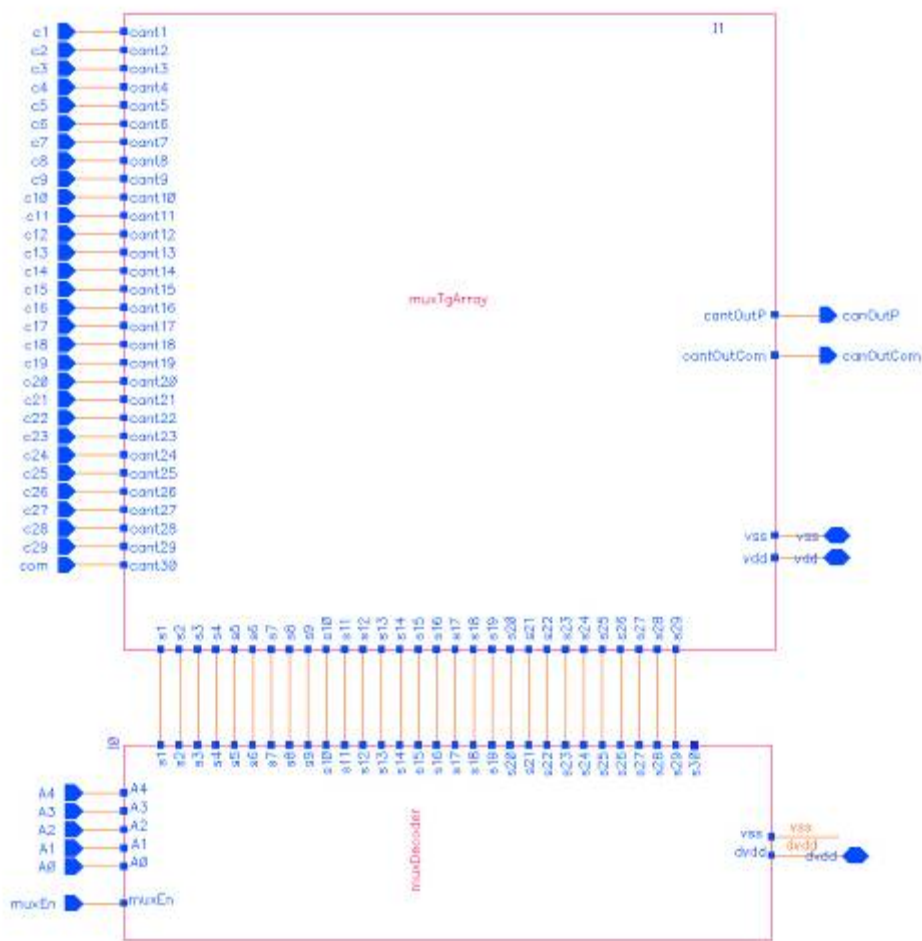
Appendix C – ASIC Schematics



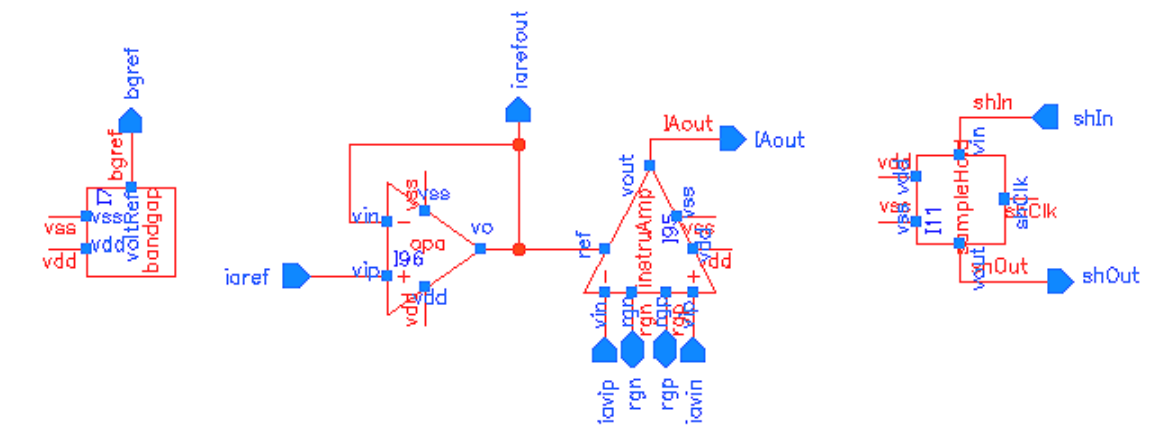
High level design schematic for ASIC



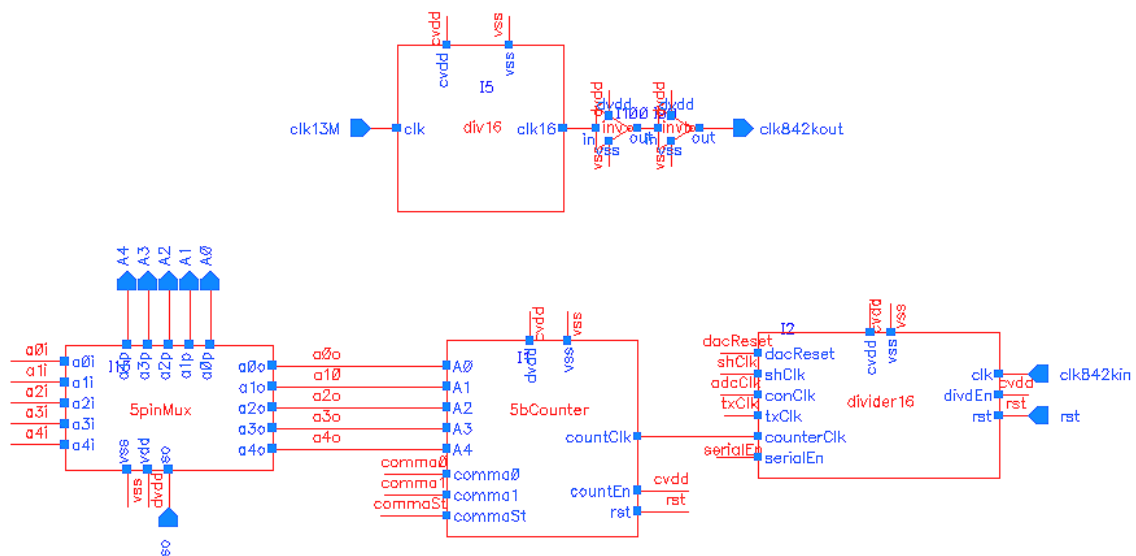
High level schematic for 30 – 1 MUX



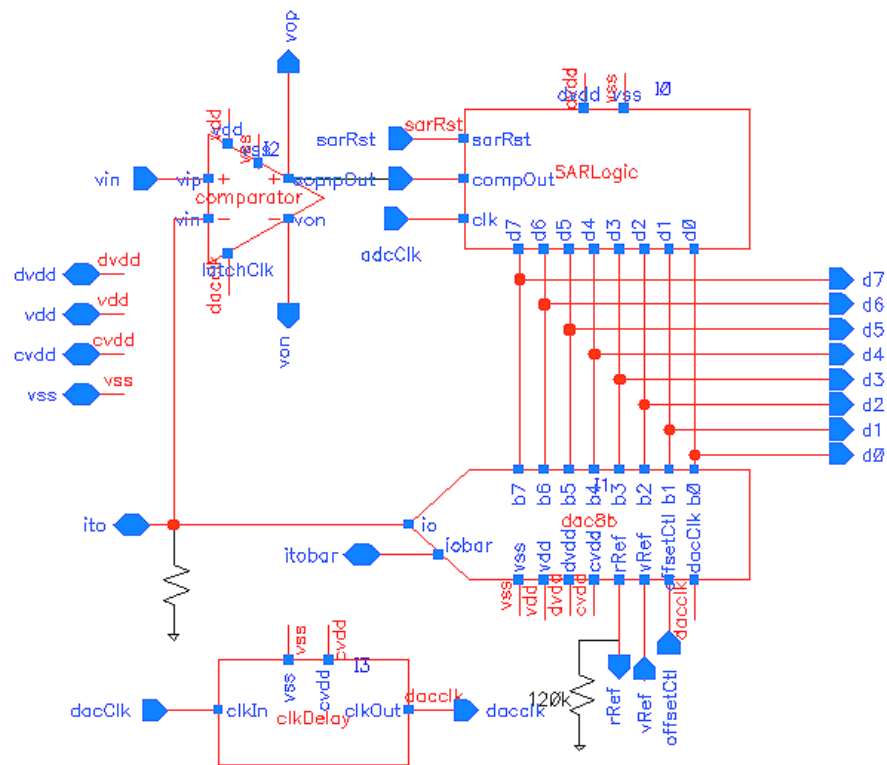
High level schematic for MUX and its decoder



High level schematic for INA



High level schematic for CLKNET



High level schematic for SAR ADC

Appendix D – Decoding and Analysis Code

```
clear all;
clc;

% Variable Sampling Rate and Number of Samples
samplingRate = 1250000;
numSamples = 14000;

% Set up connection to NIDAQ card
a1 = analoginput('nidaq','Dev1');
% Number of Channels
chan1 = addchannel(a1,0);
% Voltage input range
chan1.InputRange = [-10 10];
% Set Sampling Rate and Number of Samples
set(a1,'SampleRate',samplingRate);
set(a1,'SamplesPerTrigger',numSamples);
% Determine Threshold level
run = 1;
di = zeros(numSamples,1);
start(a1);
pause(0.15);
data = getdata(a1);
midLevel = min(data)+((abs(min(data))-abs(max(data)))/2);
for ii = 1:numSamples
    if data(ii) > midLevel
        di(ii) = 1;
    else
        di(ii) = 0;
    end
end
stop(a1);

% Declare variables to count number of 1s, 0s and Rising Edges
% while run == 1;
%     tic
%     start(a1);
%     pause(0.15);
% Setup matrix for data storage
di = zeros(numSamples,1);
%     code = zeros(numSamples,1);
binWidth1 = 0;
binWidth0 = 0;
```

```

% numREdge = 0;
jj = 1;

% Sample data and determine the logic level and store in di (ditial input)
data = getdata(a1);
for ii = 1:numSamples
    if data(ii) > midLevel
        di(ii) = 1;
    elseif data(ii) < midLevel
        di(ii) = 0;
    end

    if ii > 1
        % At rising edge (di(ii) > di(ii-1))
        % call function binCourt and court the binWidth0 (number of zeros); and
        % assign binary code to it. The binary data is stored in code.
        % Reset binWidth0 and Start court for binWidth1
        % Record the number of Rising Edge
        if di(ii) > di(ii-1)
            % [binCode, bitinc] = binCourt2(binWidth0, 0);
            [binCode, bitinc] = binCourt(binWidth0, 0);
            if isempty(binCode)
                continue;
            end
            code(jj:jj-1+bitinc)=binCode;
            jj = jj+bitinc;
            binWidth0 = 0;
            binWidth1 = binWidth1 + 1;
        % numREdge = numREdge + 1;
        % Continue to register number of 1s to binWidth1 until the falling edge
        elseif di(ii) == 1 & di(ii-1) == 1
            binWidth1 = binWidth1 + 1;
        % if binWidth1>93
        % binWidth1
        % end
        % At falling edge (di(ii) < di(ii-1))
        % call function binCourt and court the binWidth1 (number of ones); and
        % assign binary code to it. The binary data is stored in code.
        % Reset binWidth1 and Start court for binWidth0
        elseif di(ii) < di(ii-1)
            % [binCode, bitinc] = binCourt2(binWidth1, 1);
            [binCode, bitinc] = binCourt(binWidth1, 1);
            if isempty(binCode)
                continue;
            end
            % code(ii:ii+bitinc-1)=binCode;
            code(jj:jj-1+bitinc)=binCode;
            jj = jj+bitinc;
            binWidth1 = 0;

```

```

        binWidth0 = binWidth0 + 1;
% Continue to register number of 0s to binWidth0 until the next rising edge
        elseif di(ii) == 0 & di(ii-1) == 0
            binWidth0 = binWidth0 + 1;
%             if binWidth0>93
%             binWidth0
%             end
        end
    end
end
n=0;
comma=0;
[r_code, c_code] = size(code);
for ll = 1:1:c_code-18
    con1=(code(ll)==1)&(code(ll+1)==1)&(code(ll+2)==0)&(code(ll+3)==0);
    con2 =(code(ll+4)==1)&(code(ll+5)==1)&(code(ll+6)==0)&(code(ll+7)==0)&(code(ll+8)==1);
    con3=(code(ll+9)==0)&(code(ll+10)==0)&(code(ll+11)==1)&(code(ll+12)==1);
    con4=
(code(ll+13)==0)&(code(ll+14)==0)&(code(ll+15)==1)&(code(ll+16)==1)&(code(ll+17)==1);
    if con1&con2&con3
        n=n+1;
        comma(n)=ll;
    end
end
% check if there are code missing between two commas
nn=0;
[row_comma, column_comma]=size(comma);
for kk=1:1:(column_comma-1)
    if comma(kk+1)-comma(kk)~=288
        nn=nn+1;
        commaErr(nn)=comma(kk);
    end
end
if nn >2
    continue;
end
%Polarity check
polWrgCnt=0;
polWrgMtx=0;
jjj=0;
for iii=comma(1):9:(c_code-18)
    dataXor12=xor(code(iii),code(iii+1));
    dataXor34=xor(code(iii+2),code(iii+3));
    dataXor56=xor(code(iii+4),code(iii+5));
    dataXor78=xor(code(iii+6),code(iii+7));
    dataXor1234=xor(dataXor12, dataXor34);
    dataXor5678=xor(dataXor56, dataXor78);
    dataXor=xor(dataXor1234, dataXor5678);

```

```

        if code(iii+8)==(~dataXor)
            polWrgCnt=polWrgCnt+1;
            jjj=jjj+1;
            polWrgMtx(jjj)=iii;
        end
    end

%delete comma bits and save to data matrix
kl=comma(1);
mm=1;
dataNoComma=0;
while kl<=comma(column_comma)
    if mod(kl-comma(1),288)==0
        kl=kl+18;
    else
        dataNoComma(mm)=code(kl);
        mm=mm+1;
        kl=kl+1;
    end
end

% delete polarity bits and save data to matrix
[row_dataNoComma, column_dataNoComma]=size(dataNoComma);
%   if column_dataNoComma ~= 540
%       continue;
%   end
mn=1;
ij=1;
dataFin=0;
while mn<=column_dataNoComma
    if mod(mn,9)==0
        mn=mn+1;
    else
        dataFin(ij)=dataNoComma(mn);
        ij=ij+1;
        mn=mn+1;
    end
end

%convert binary data to decimal data
[row_dataFin, column_dataFin]=size(dataFin);
%   if column_dataFin ~= 480
%       continue;
%   end
lm=0;
dataNu(1)=0;
dataAcc=0;
for jk=1:8:(column_dataFin-18)
    lm=lm+1;

```

```

    for kl=0:1:7
        dataAcc=dataAcc+dataFin(jk+kl)*(2^kl);
    end
    dataNu(lm)=dataAcc;
    dataAcc=0;
end

[row_dataNu, column_dataNu]=size(dataNu);
op=0;
channel=0;
for op = 1:1:column_dataNu
%     if column_dataNu ~= 60
%         continue;
%     end
    channel(op)=dataNu(op);
end
% Display total number of rising edge & reset
% disp(numREdge);
% numREdge = 0;
% Stop acquisition
stop(a1);

% Clear figure and plot
clf;
plot(channel);
%axis([1 numSamples -0.5 1.5])
drawnow
toc
% end %(while loop)
function [binCode, bitinc] = binCourt(x,y)

u11 = 11; u12 = 14;
u21 = 21; u22 = 28;
u31 = 32; u32 = 41;
u41 = 49; u42 = 54;
u51 = 62; u52 = 67;
u61 = 75; u62 = 80;
u71 = 87; u72 = 93;
u81 = 97; u82 = 160;
if x <=u12 %u11>=11
    if y == 1
        binCode = 1;
    elseif y == 0;
        binCode = 0;
    end
    bitinc = 1;
end
end

```

```
if x >= u21 & x <= u22
    if y == 1
        binCode = [1,1];
    elseif y == 0
        binCode = [0,0];
    end
    bitinc = 2;
end

if x >= u31 & x <= u32
    if y == 1
        binCode = [1,1,1];
    elseif y == 0
        binCode = [0,0,0];
    end
    bitinc = 3;
end

if x >= u41 & x <= u42
    if y == 1
        binCode = [1,1,1,1];
    elseif y == 0
        binCode = [0,0,0,0];
    end
    bitinc = 4;
end

if x >= u51 & x <= u52
    if y == 1
        binCode = [1,1,1,1,1];
    elseif y == 0
        binCode = [0,0,0,0,0];
    end
    bitinc = 5;
end

if x >= u61 & x <= u62
    if y == 1
        binCode = [1,1,1,1,1,1];
    elseif y == 0
        binCode = [0,0,0,0,0,0];
    end
    bitinc = 6;
end

if x >= u71 & x <= u72
    if y == 1
        binCode = [1,1,1,1,1,1,1];
    elseif y == 0
        binCode = [0,0,0,0,0,0,0];
    end
end
```

```
    end
    bitinc = 7;
end

if x >= u81
    if y == 1
        binCode = [1,1,1,1,1,1,1,1];
    elseif y == 0
        binCode = [0,0,0,0,0,0,0,0];
    end
    bitinc = 8;
end

if
x>u12&x<u21|x>u22&x<u31|x>u32&x<u41|x>u42&x<u51|x>u52&x<u61|x>u62&x<u71|x>u72&x<
u81
    binCode = [];
    bitinc = [];
end
```

```
close all;
clear all;
clc;

V_upper = 1589
V_lower = 200

% read in data file

%serial=csvread('200_1589_100hz_sine.csv',2,0);

% find the dimensions of matrix
[row_serial, column_serial]=size(serial);

% delete unused data (oversampled data), only save the clock and useful data to a(i,j)

k=0;

for j=1:(row_serial-1)
    if serial(j,2)~=serial(j+1,2)
        k=k+1;
        a(k,1)=serial(j,2);
        a(k,2)=serial(j,1);
    end
end
% delete the data when clock is low, and save the data to b(m)
[row_a, column_a]=size(a);

m=0;

for i=1:(row_a-1)
    if a(i,1)==1
        m=m+1;
        b(m)=a(i,2);
    end
end

% find comma, and save comma location to matrix comma(n)
comma=0;
n=0;

[row_b, column_b]=size(b);

for l=1:(column_b-18)
    con1=(b(l)==1)&(b(l+1)==1)&(b(l+2)==0)&(b(l+3)==0);
    con2 =(b(l+4)==1)&(b(l+5)==1)&(b(l+6)==0)&(b(l+7)==0)&(b(l+8)==1);
    con3=(b(l+9)==0)&(b(l+10)==0)&(b(l+11)==1)&(b(l+12)==1);
    con4= (b(l+13)==0)&(b(l+14)==0)&(b(l+15)==1)&(b(l+16)==1)&(b(l+17)==1);
    if con1&con2&con3
```

```

        n=n+1;
        comma(n)=l;
    end
end

% check if there are code missing between two commas
nn=0;

[row_comma, column_comma]=size(comma);

for kk=1:1:(column_comma-1)
    if comma(kk+1)-comma(kk)~=288
        nn=nn+1;
        commaErr(nn)=comma(kk);
    end
end

% check the ploarity to see how many data is wrong from the first comma
polWrgCnt=0;
jj=0

for ii=comma(1):9:(column_b-18)
    dataXor12=xor(b(ii),b(ii+1));
    dataXor34=xor(b(ii+2),b(ii+3));
    dataXor56=xor(b(ii+4),b(ii+5));
    dataXor78=xor(b(ii+6),b(ii+7));
    dataXor1234=xor(dataXor12, dataXor34);
    dataXor5678=xor(dataXor56, dataXor78);
    dataXor=xor(dataXor1234, dataXor5678);

    if b(ii+8)==(~dataXor)
        polWrgCnt=polWrgCnt+1;
        jj=jj+1;
        polWrgMtx(jj)=ii;
    end
end

%delete comma bits and save to data matrix
% ll=comma(1);
% mm=1;
%
% while ll<=comma(column_comma)
%     if mod(ll-comma(1),288)==0
%         ll=ll+18;
%     else
%         dataNoComma(mm)=b(ll);
%         mm=mm+1;
%         ll=ll+1;
%     end

```

```
% end

% replace comma bits with zeros
l1=comma(1);
l2=1;

while l1<=comma(column_comma)
    if mod(l1-comma(1),288)==0
        for l3=1:1:18
            dataNoComma(l2)=0;
            l2=l2+1;
            l1=l1+1;
        end
    else
        dataNoComma(l2)=b(l1);
        l2=l2+1;
        l1=l1+1;
    end
end

% delete polarity bits and save data to matrix
[row_dataNoComma, column_dataNoComma]=size(dataNoComma);
nn=1;
ij=1;

while nn<=column_dataNoComma
    if mod(nn,9)==0
        nn=nn+1;
    else
        dataFin(ij)=dataNoComma(nn);
        ij=ij+1;
        nn=nn+1;
    end
end

%convert binary data to decimal data
[row_dataFin, column_dataFin]=size(dataFin);
lm=0;
data(1)=0;
dataAcc=0;

for jk=1:8:(column_dataFin-8)
    lm=lm+1;
    for kl=0:1:7
        dataAcc=dataAcc+dataFin(jk+kl)*(2^kl);
    end
    data(lm)=dataAcc;
    dataAcc=0;
end
```

```

end

% data interpolation during comma
data(1)=[];

for m1=2:1:lm-2;
    if data(m1)==0
        data(m1)=data(m1-1)*3/4+data(m1+2)/4;
        data(m1+1)=data(m1-1)/4+data(m1+2)*3/4;
    end
end

% fft of the data
Y=fft(data);
N=length(Y);
Y(1)=[];
power=10*log10(abs(Y(1:N/2)).^2);
power = power - max(power);
nyquist=1/2;
freq=(1:N/2)/(N/2)*nyquist;figure(2);
plot(freq,power), grid on;

% nu_data = round(data(75:4362)); % 400Hz Sine Wave 200 - 1589mV sigbin 20
% nu_data = round(data(129:4418)); % 200Hz Sine Wave 200 - 1589mV sigbin 10
nu_data = round(data(50:4338)); % 100Hz Sine Wave 200 - 1589mV sigbin 5
Y2=abs(fft(nu_data));
N2 = length(Y2);
Y2(1) = [];
powerAna = Y2(1:end/2)/N*2;
% powerAna = powerAna - max(powerAna);
cycles = 4;
sigbin = cycles + 1;
noise = [powerAna(1:sigbin-1), powerAna(sigbin+1:end)];
SNR = 10*log10(powerAna(sigbin)^2/sum(noise.^2))
ENOB = ((SNR)-1.76)/6.02

% nuDataSize = size(nu_data);
% CourtBin(1:255) = 0;
% for bin = 1:1:255
%     for dataCourt = 1:1:nuDataSize(2)
%         if bin == nu_data(dataCourt)
%             CourtBin(bin) = CourtBin(bin)+1;
%         end
%     end
% end
% bar (CourtBin, 'DisplayName', 'CourtBin', 'YDataSource', 'CourtBin'); figure(gcf)

minbin=min(nu_data);

```

```

maxbin=max(nu_data);
% histogram
h= hist(nu_data, minbin:maxbin);
% cumulative histogram
ch= cumsum(h);
% transition levels
T = -cos(pi*ch/sum(h));
% linearized histogram
hlin = T(2:end) - T(1:end-1);
% truncate at least first and last bin, more if input did not clip ADC
trunc=2;
hlin_trunc = hlin(1+trunc:end-trunc);
% calculate lsb size and dnl
lsb = sum(hlin_trunc) / (length(hlin_trunc));
dnl = [0 hlin_trunc/lsb-1];
misscodes = length(find(dnl<-0.9));
% calculate inl
inl= cumsum(dnl);
% plot
figure(3); clf;
subplot(2,1,1);
plot(linspace(minbin+trunc, maxbin-trunc, length(dnl)), dnl, '.');
xlabel('code');
ylabel('DNL [LSB]');
title(sprintf('DNL = +%.2f / %.2f LSB, std.dev=%.2f, %d missing codes (DNL <-0.9)', max(dnl),
min(dnl), std(dnl), misscodes));
subplot(2,1,2);
plot(linspace(minbin+trunc, maxbin-trunc, length(dnl)), inl, '.');
xlabel('code');
ylabel('INL [LSB]');
title(sprintf('INL = +%.2f / %.2f, std.dev=%.2f', max(inl), min(inl), std(inl)));

```

Vita

Gary To was born in Hong Kong on 17th October, 1982. He spent the first 16 years of his life in Hong Kong. He attended Chan Sui Ki (La Salle) Secondary School and passed the O-level exam. He graduated from the University of Tennessee, Knoxville, with an undergraduate degree in Biomedical Engineering in spring 2004. He continued with graduate studies after his graduation. During his free time, Gary enjoys playing piano, designing web design, and contemporary and wedding photography.
