A Sub-Threshold Low-Power Integrated Bandpass Filter for Highly-Integrated Spectrum Analyzers

A Thesis Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Benjamin David Roehrs
May 2017

Copyright © 2017 by Benjamin David Roehrs
All rights reserved.

Acknowledgements

My greatest thanks and highest praise is to my heavenly Father. I have been given what I am not worthy of, and what I deserve has been mercifully withheld. For this, may Your praise ever be on lips. Proverbs 16:2-3

I would like to thank my dear wife Katie for her loving support and understanding when the days were long and the nights were short. Your love, encouragement, and patience during this season have manifested themselves in the most vivid reflection of God's love in my life.

I wish to express how honored I am to have had the privilege of working with Dr. Blalock, Dr. Britton, and Dr. Ericson. Without their unmatched experience, continual support, and sincere interest in my success as a student, none of this would have been possible. I have garnered a veritable fortune of knowledge from them, both inside and outside of the lab, and count it a joy to have advanced my education under their instruction.

Thanks and sincere appreciation to Dr. Ericson and Oak Ridge National Laboratory for their interest in and funding of this work. I'm grateful to have been involved, and hope that this work is worthy to have been the first step in the MISA project.

I'm thankful for the life-long support of my parents, David and Lois Roehrs. Throughout my life you've demonstrated the kind of selfless work ethic that I aspire to now. Thank you for always spurring me onward and upward.

Special thanks to Gavin Long, whose measurement data collection and overall continuation of this work for the MISA project have been greatly appreciated. I'd also like to thank my ICASL colleagues who were quick to assist in any way.

Abstract

Low-power analog filter banks provide frequency analysis with minimal space requirements, making them viable solutions for integrated remote audio- and vibration-sensing applications. In order to achieve a balance between the length of deployable service and system performance, a critical requirement of such remote sensor networks is low-power consumption, due to the constraints imposed by on-board battery cells.

In this work, the design and implementation of a sub-threshold complementary metal-oxide semiconductor (CMOS) integrated low-power tunable analog filter channel for Oak Ridge National Laboratory is presented. Project specifications required a tunable, high-order, monolithic bandpass filter channel with small chip area and low power consumption. With initial design focusing on the audio frequency spectrum, the 8th order filter channel presented in this work provides an effective Q-factor of 4.5 and a minimum dynamic range (DR) of approximately 85 dB, while allowing for tuning across a range of center frequencies from 2 kHz to 100 kHz, with power consumption of a single 8th order filter channel measured at $155\,\mu$W, nominally. An integrated analog G_m-C filter topology was selected for this application. Functionally, the high-Q bandpass filter transfer function is implemented via four cascaded 2nd order filter cells, resulting in a single 8th order filter channel, fabricated in 130-nm 1.2 V CMOS technology, suitable for use in monolithic integrated spectral analysis applications.

Table of Contents

1 Introduction **1**

1.1 Motivation 1

1.2 Thesis Organization 3

2 Background & Literature Review **4**

2.1 System Requirements 4

2.2 Design Considerations 4

2.3 System Topology 6

3 Filter Design and Simulation **8**

3.1 Filter Characteristics 8

3.2 Macro-Model Filter Simulation 10

3.3 Filter Implementation in 130-nm 1.2 V CMOS 12

3.3.1 Technology Current Extraction 13

3.3.2 OTA-C^4 Simulation with CMOS Models 15

3.3.3 Simulating the Effective Transconductance 19

3.3.4 Filter Cell Optimization 21

3.3.5 Feed-Forward Prevention 26

3.4 8th Order Filter Channel Topology 28

3.4.1 Channel Current Bias 30

3.5 Fabrication in 130-nm 1.2 V CMOS 33

4 Test Measurements and Post-Fabrication

Verification **35**

4.1 MISA Filter Channel Evaluation Setup 35

4.2 MISA Filter Channel Linear Range 39

4.3 Filter Spectral Response 40

4.3.1 $f_c = 2$ kHz 41

4.3.2 $f_c = 10$ kHz 44

4.3.3 $f_c = 50$ kHz 45

4.3.4 $f_c = 100$ kHz 47

4.4 Filter Order Comparison 49

4.4.1 $f_c = 2$ kHz 50

4.4.2 $f_c = 10$ kHz 51

4.4.3 $f_c = 50$ kHz 52

4.4.4 $f_c = 100$ kHz 53

4.5 Variable Filter Gain 53

4.6 Total Harmonic Distortion 55

4.6.1 $f_c = 10$ kHz 56

4.6.2 $f_c = 100$ kHz 57

4.7 Filter Performance Summary 59

5 Conclusion **61**

5.1 Thesis Summary 61

5.2 Recommendations for Future Work 62

References **64**

Appendices **68**

A OTA-C^4 Transfer Function Derivation **69**

B Supplementary Measurement Data: Chips 3-5 **72**

B.1 2 kHz 72

B.1.1 Chip 3: Ch. 1 and Ch. 2 72

B.1.2 Chip 4: Ch. 1 and Ch. 2 73

B.1.3 Chip 5: Ch. 1 and Ch. 2 74

B.2 10 kHz 75

B.2.1 Chip 3: Ch. 1 and Ch. 2 75

B.2.2 Chip 4: Ch. 1 and Ch. 2 76

B.2.3 Chip 5: Ch. 1 and Ch. 2 77

B.3 50 kHz 78

B.3.1 Chip 3: Ch. 1 and Ch. 2 78

B.3.2 Chip 4: Ch. 1 and Ch. 2 79

B.3.3 Chip 5: Ch. 1 and Ch. 2 80

B.4 100 kHz 81

B.4.1 Chip 3: Ch. 1 and Ch. 2 81

B.4.2 Chip 4: Ch. 1 and Ch. 2 82

B.4.3 Chip 5: Ch. 1 and Ch. 2 83

Vita **84**

List of Figures

1 Initial high-level topology of the MISA filter channel. 6

2 Ideal Voltage-Controlled Current Source Macro Model. 8

3 Schematic of the 2nd order OTA-C^4 [1]. 9

4 Macro-model based simulation of the 2nd order OTA-C^4 filter spectral responses at —— $f_c = 2$ kHz, —— $f_c = 5$ kHz, and —— $f_c = 10$ kHz, demonstrating the ability to adjust the filter center frequency across the initial required operational frequency spectrum. 12

5 Simulation test bench used to obtain and verify the technology current characteristic of the utilized 130-nm CMOS process. 13

6 I_D vs. V_{GS}, illustrating the exponential relationship between I_D and V_{GS} in sub-threshold operation. —— Trace 1: $(W/L) = 160/130\,n\text{m}, mult = 1$, —— Trace 2: $(W/L) = 10/1\,\mu\text{m}, mult = 1$, and —— Trace 3: $(W/L) = 10/1\,\mu\text{m}, mult = 100$. 14

7 Simplified OTA used for initial simulations. 16

8 OTA-C^4 implemented in 130-nm CMOS [1]. 17

9 MISA filter cell implemented in 130-nm CMOS, with a cascode current-bias section, utilized to balance the tail currents of the input differential pair. 18

10 Test bench used to obtain the effective transconductance of a MISA OTA cell. 20

11 Simulated plot of I_{out} vs. $V_{in,dif}$, illustrating the change in output current that corresponds to a change in differential input voltage when biased with 15 nA of input current. 21

12 Simulated filter spectral responses comparing the - - - 2nd order response without RHPZ cancellation, —— 2nd order response with RHPZ cancellation, - - - 8th order response without RHPZ cancellation, and —— 8th order response with RHPZ cancellation at $f_c = 10$ kHz. 28

13 8th order MISA filter channel topology consisting of four MISA filter cells cascaded in series, with unity-gain buffering between each filter cell. . . . 30

14 Simulated filter spectral response comparison between the —— 2nd order, —— 4th order, —— 6th order, and —— 8th order outputs of the MISA filter channel under unity-gain Simulated Theoretical Bias conditions for $f_c = 10$ kHz. 31

15 Schematic of the Minch current mirror cell used to bias each filter cell within a MISA filter channel. 32

16 Block diagram illustrating the common centroid technique utilized to layout the capacitors of the OTA-C^4 filter cell with unit capacitors. 33

17 Microscope photograph of a bare die MISA-01 chip with the layout of a MISA filter channel overlaid with section labels. 34

18 Single channel schematic overview of the MISA evaluation circuit. Note that this circuit topology was utilized for each channel of the MISA evaluation PCB. 36

19 Section label overlay of the MISA evaluation PCB. 38

20 MISA evaluation PCB fully populated with bias circuits, peripheral I/O, and IC "open-top" socket. 39

21 $V_{out,p-p}$ vs. $V_{in,p-p}$ linearity range, illustrating a linear output versus input response up to approximately 110 $\mathrm{mV_{p\text{-}p}}$, and the 1 dB compression point beginning at approximately 140 $\mathrm{mV_{p\text{-}p}}$. 40

22 Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) under —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 2$ kHz. 41

23 Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) under —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 2$ kHz. 43

24 Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 10$ kHz. 44

25 Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 10$ kHz. 45

26 Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 50$ kHz. 46

27 Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 50$ kHz. 47

28 Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias, — Measured Theoretical Bias, and — Simulated Theoretical Bias conditions for $f_c = 100$ kHz. . . . 48

29 Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias, — Measured Theoretical Bias, and — Simulated Theoretical Bias conditions for $f_c = 100$ kHz. . . . 49

30 — 2nd order, — 4th order, — 6th order, — 8th order, and — 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 2$ kHz. 50

31 — 2nd order, — 4th order, — 6th order, — 8th order, and — 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 10$ kHz. 51

32 — 2nd order, — 4th order, — 6th order, — 8th order, and — 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 50$ kHz. 52

33 — 2nd order, — 4th order, — 6th order, — 8th order, and — 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 100$ kHz. 53

34 Variable filter gain spectral response of Chip 1 - Ch. 1 demonstrating the ability to bias the MISA filter channel for varying amounts of filter gain. — 0 dB, — 3 dB, — 6 dB, — 9 dB, and — 12 dB filter gain settings are demonstrated above for $f_c = 10$ kHz. 54

35 Total harmonic distortion measurement of Chip 1 — Ch. 1 (left) and — Ch. 2 (right) under Corrected Bias conditions for $f_c = 10$ kHz. . . 56
36 Total harmonic distortion measurement of Chip 2 — Ch. 1 (left) and — Ch. 2 (right) under Corrected Bias conditions for $f_c = 10$ kHz. . . 57
37 Total harmonic distortion measurement of Chip 1 — Ch. 1 (left) and — Ch. 2 (right) under Corrected Bias conditions for $f_c = 100$ kHz. . 58
38 Total harmonic distortion measurement of Chip 2 — Ch. 1 (left) and — Ch. 2 (right) under Corrected Bias conditions for $f_c = 100$ kHz. . 58
39 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias and — Measured Theoretical Bias, and — Simulated Theoretical Bias. 72
40 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias and — Measured Theoretical Bias, and — Simulated Theoretical Bias. 73
41 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias and — Measured Theoretical Bias, and — Simulated Theoretical Bias. 74
42 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias and — Measured Theoretical Bias, and — Simulated Theoretical Bias. 75
43 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with — Measured Corrected Bias and — Measured Theoretical Bias, and — Simulated Theoretical Bias. 76

44 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias. 77
45 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias. 78
46 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias. 79
47 Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias. 80
48 Filter spectral response of Chip 3 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz. . . . 81
49 Filter spectral response of Chip 4 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz. . . . 82
50 Filter spectral response of Chip 5 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz. . . . 83

1 Introduction

1.1 Motivation

In remote sensor network applications, low power consumption is critical in achieving a long service life for a given device. As digital data acquisition performance is advanced via current state-of-the-art Analog-to-Digital Converters (ADCs), justification for an alternative approach based on low-power analog filter design is warranted. Referring to the widely available and acknowledged "ADC Performance Survey 1997-2016" by Boris Murmann, a quick comparison between digital and analog approaches can be made in order to inform such a design decision [2]. While a perfect comparison of figures of merit between an ADC and an analog filter is tenuous, approximations extracted from the ADC performance survey may apprise the designer to the performance trade-offs to be expected.

If the dynamic range (DR) of an analog bandpass filter is defined as the difference in magnitude between the filter's center frequency and the root mean square (rms) noise floor, then a comparison can be made between the filter and an ADC exhibiting similar performance. Setting the benchmark for the dynamic range comparison to 80 dB, referring to the ADC performance survey yields several candidates amongst state-of-the-art ADCs that meet this performance requirement. In order to match this dynamic range specification, the power dissipated ranges from 3.5 mW in the best case, up to approximately 25 mW in the worst case. By taking additional performance metrics associated with these devices, such as Signal-to-(Noise + Distortion) (SNDR), Eq. 1.1 can be used to obtain an estimate of the required Effective Number

of Bits (ENOB) [3]. Of the ADCs that meet the 85 dB dynamic range benchmark, the corresponding SNDR values of these devices result in an average ENOB of 14 bits.

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.1}$$

The analog filter approach presented in this work not only achieves the specified 85 dB dynamic range bench mark - it exceeds it. However, a significant difference between the presented analog filter approach and the ADC approach is the power consumption required to offer such performance. The 8th order analog filter designed and implemented in this work nominally consumes 155 μW of power, and surpasses the 85 dB dynamic range benchmark. In a remote sensing network, this difference in power consumption corresponds to a significant disparity in length of deployable service. Assuming the power capacity of a single AA battery to be 2 Ah, the MISA filter channel presented in this work may operate continuously for approximately 20,000 hours, which translates to a deployable service life of $\sim$2.39 years without any implementation of a power management strategy.

Previously-reported low-power analog filter designs provide the adjustability required for center frequency tuning, in addition to low-power operation [1]. However, the integrated tunable analog filter presented in this work improves upon the performance of such filter designs while maintaining comparable low power consumption, offering an improved dynamic range, cancellation of an inherent complex right-half-plane zero for increased filter stability, and evaluation of an integrated higher-order filter channel.

1.2 Thesis Organization

This thesis presents the design process for the implemented integrated tunable analog bandpass filter channel, the core functional block suitable for monolithic integrated spectrum analysis applications, covering the initial functional requirements, design steps, simulation verification, implementation in 130-nm 1.2 V CMOS technology, and finally the measured post-fabrication testing results.

Chapter 2 provides design context via general background information, as well as an examination of previous generations of integrated tunable bandpass filters. In Chapter 3, the design methodology is examined, including the 2nd order filter transfer function derivation, macro-model based simulation, implementation and simulation in 130-nm 1.2 V CMOS technology, as well as simulation of an 8th order filter channel. Chapter 4 presents and analyzes measurement data from 2 chips, out of a sample set of 5 chips, under predetermined bias conditions, with the remaining data contained in Appendix B. Chapter 5 concludes this work by evaluating the success of the implemented design and discussing potential design improvements relevant to future advancement of this research.

2 Background & Literature Review

2.1 System Requirements

The initial system requirements consisted primarily of a monolithic bandpass filter exhibiting high-Q factor, low power consumption, and operational across the audio frequency range. At the onset, the desired Q-factor of the system was set at between 3 and 5, regardless of the topology chosen. A high Q-factor was crucial in order for the filter to function as the core functional block in an integrated spectrum analyzer. The operational frequency spectrum originally decided upon was 2 kHz to 10 kHz, with the final filter cell design demonstrating functionality across all frequencies in this spectrum. However, the upper end of this range was extended to 100 kHz once the project was under way, and simulation proved the feasibility of such an extension after interest was expressed. Due to the potential for multiple applications, design requirements stipulated that the resulting filter cell offer dynamic tunability and repeatability across the operational frequency spectrum. While no strict power consumption constraints were assigned, low power consumption was considered a presupposition in the design effort, as justification for an analog filter approach predicated upon such performance. Regarding area constraints for an integrated circuit, the maximum die area appropriated was 36 mm^2.

2.2 Design Considerations

Similar to the discussion in Section 1.1, analog filter banks have traditionally been the preference for high-performance remote sensing applications due to the

high level of operational precision offered while consuming a minimal amount of power. Specifically concerning the audio frequency spectrum, analog filters have been utilized in many cochlear implants, as they are well-suited for such battery-powered applications [4, 5].

When limited to battery power, designing a filter with a wide dynamic range presents a formidable challenge due to noise vulnerabilities and limited voltage headroom [1]. Precision tuning is also an obstacle in low-power filter designs due to process variation. However, implementing device sizes that are sufficiently larger than the minimum device feature size will aid in better matching within an integrated circuit, as well as improving wafer-to-wafer matching. Increasing device size within reason reduces the percent variation between matched components, as the effects of device edge irregularities are minimized in large geometry devices [6].

A common method with which to implement a low-power integrated filter is the transconductance-capacitance (G_m-C) topology [7]. Concerning system requirements in this work, G_m-C filter topologies excel in leveraging sub-threshold operation to reduce power consumption. Additionally, G_m-C filters satisfy the requirement for dynamic programmability, as the transconductance values are readily controlled via adjustment of bias currents [1]. However, G_m-C filters are subject to constraints in dynamic range resulting from the limited linear range of the sub-threshold input differential pair [8, 9]. In order to mitigate this problem, several methods of transconductor linearization have been reported, including source degeneration, gate degeneration, and the addition of linearizing "bump" transistors to the input differential pair [9]. The G_m-C filter topology presented as the operational transconduc-

tance amplifier (OTA) capacitively coupled current conveyor (OTA-C^4) also utilizes capacitive division to keep an input signal within the transconductor's linear range [1]. Given the performance of the OTA-C^4, this topology was selected as the foundational design upon which the monolithic integrated spectrum analyzer (MISA) filter would be based.

2.3 System Topology

Upon determining the bandpass filter topology, determining system level details became the next priority. Illustrated below in Fig. 1, the initial high-level system topology incorporated the flexibility of cascading four 2nd order filters in series to achieve a single 8th order channel, or taking the 2nd order outputs independently.

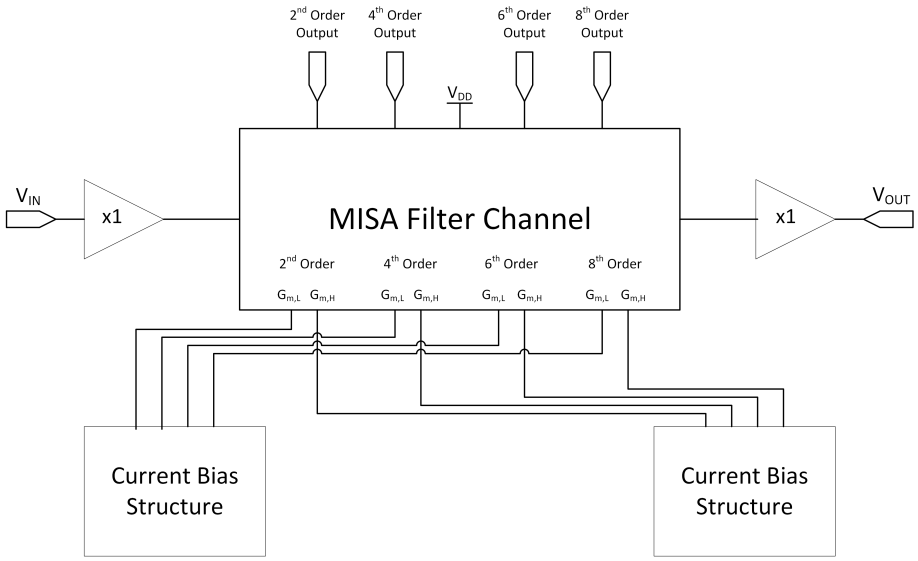

Figure 1: Initial high-level topology of the MISA filter channel.

When hosted on an evaluation printed circuit board (PCB), the input and output of the MISA filter channel would be unity-gain buffered by an op-amp capable of driving it's input and output rail-to-rail. The unity-gain buffer would serve as a line of defense between the MISA filter channel and it's host environment, in addition to aiding the signal drive strength both onto and off of the evaluation PCB. A key difference between the MISA filter channel and the foundational OTA-C^4 is found in the CMOS process node. The MISA filter channel was implemented in 130-nm CMOS, rather than the 0.35-μm CMOS process node reported previously [1]. The smaller CMOS process node would present a new design challenge, as the native supply voltage scales with the process node accordingly. A lower process-defined supply voltage would also reduce the available voltage headroom, thus impeding the dynamic range of the MISA filter channel. The design process of the MISA filter channel is examined in the following section.

3 Filter Design and Simulation

3.1 Filter Characteristics

Taking the familiar form of a bandpass filter, the reported transfer function of the 2nd order OTA-C^4 is defined as follows [1].

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}\frac{s\tau_l(1 - s\tau_f)}{1 + s(\tau_l + \tau_f(\frac{C_O}{C_2} - 1)) + s^2\tau_h\tau_l} \tag{3.1}$$

In order to intuitively verify the second order bandpass filter transfer function of the OTA-C^4, an ideal voltage-controlled current source was used to simulate an ideal OTA. This OTA "macro model", depicted in Fig. 2, was used in simulation with only 2 variables of interest: transconductance and capacitance.

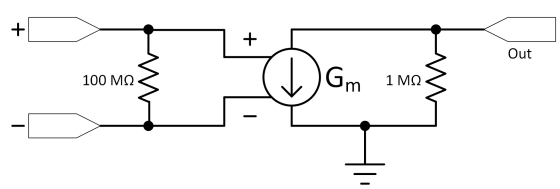

Figure 2: Ideal Voltage-Controlled Current Source Macro Model.

The macro model was then implemented in the OTA-C^4 filter topology, as seen in Fig. 3, in order to simulate the transfer function, and verify the ability to independently adjust corner frequencies.

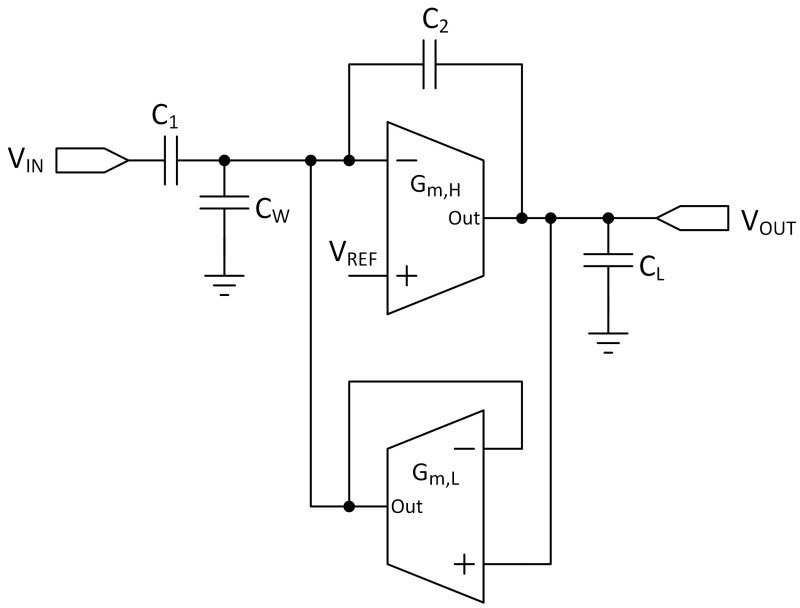

Figure 3: Schematic of the 2nd order OTA-C4 [1].

Based on the above topology, Eq. 3.2 - 3.5 were used to approximate the required capacitor values for the circuit in order to simulate the filters spectral response [1].

$$C_2 = \frac{N \cdot q}{4V_L} 10^{\frac{DR}{10}} \tag{3.2}$$

$$C_1 = 2C_2 A_{v,Q} \tag{3.3}$$

$$C_T = 4C_2 Q_{max}^2 = C_1 + C_2 + C_W \tag{3.4}$$

$$C_O = C_2 + C_L \tag{3.5}$$

Note: q is the charge of an electron, and N is the number of noise sources in the

transconductors, Q_{max} is the maximum Q-factor achievable with the 2nd order filter cell, and $A_{v,Q}$ is the filter gain when biased for maximum Q-factor [1]. Initially, in order to size C_2 without any prior calculations of simulated data, estimations were required for the linear input range, V_L, and the number of noise sources in the transconductors. The dynamic range, DR, of the filter was selected to be a minimum of 80 dB for each 2nd order filter cell. Informed by these estimations, the initial approximations for capacitance values would allow for simulated bandpass transfer function verification with the macro-model based OTA-C^4. However, before simulating with the macro-model approach, symbolic SPICE was used to verify the transfer function of the OTA-C^4 independent of any CMOS process device models. By means of substitution, the symbolic SPICE transfer function was then derived and arranged in the closed-form transfer function reported in Eq. 3.1 [1]. This transfer function derivation process is presented in detail in Appendix A.

3.2 Macro-Model Filter Simulation

After verifying the bandpass transfer function of the OTA-C^4 by hand, Eq.'s 3.6 and 3.7 were utilized to estimate the low- and high-side transconductances, which relate to the respective corner frequencies of interest via Eq. 3.9.

$$\tau_l = \frac{C_2}{G_{m,L}} \tag{3.6}$$

$$\tau_h = \frac{C_O C_T - C_2^2}{C_2 G_{m,H}} \tag{3.7}$$

$$\tau_f = \frac{C_2}{G_{m,H}} \tag{3.8}$$

$$\tau = \frac{1}{2\pi f_c} \tag{3.9}$$

The first attempts at choosing capacitor values for the OTA-C^4 resulted in impractically large capacitor values, which would present yield issues if fabricated, and required excessively high transconductances in order to obtain the correct operational frequency spectrum. Multiple iterations resulted in the design parameters which yielded the following plot, Fig. 4, which verified the 2nd order bandpass transfer function, and demonstrated the ability to tune the center frequency of the filter across the initial frequency spectrum of interest (2 - 10 kHz).

Centered at frequencies ranging from 2-10 kHz, the macro-model based simulation provided excellent Q-factor and dynamic range while demonstrating independent adjustment of corner frequencies, and thus the center frequency of the filter. However, due to the ideal nature of the macro model, the Q-factor achieved would prove to be optimistic, and the transconductances required to obtain the same filter characteristics using 130-nm CMOS models could not be obtained with a single OTA using identical device properties for both the low- and high-side transconductors while maintaining operation in weak inversion. Nonetheless, simulating with the macro model proved to stand as an efficient means of verifying filter characteristics for a given set of capacitor values.

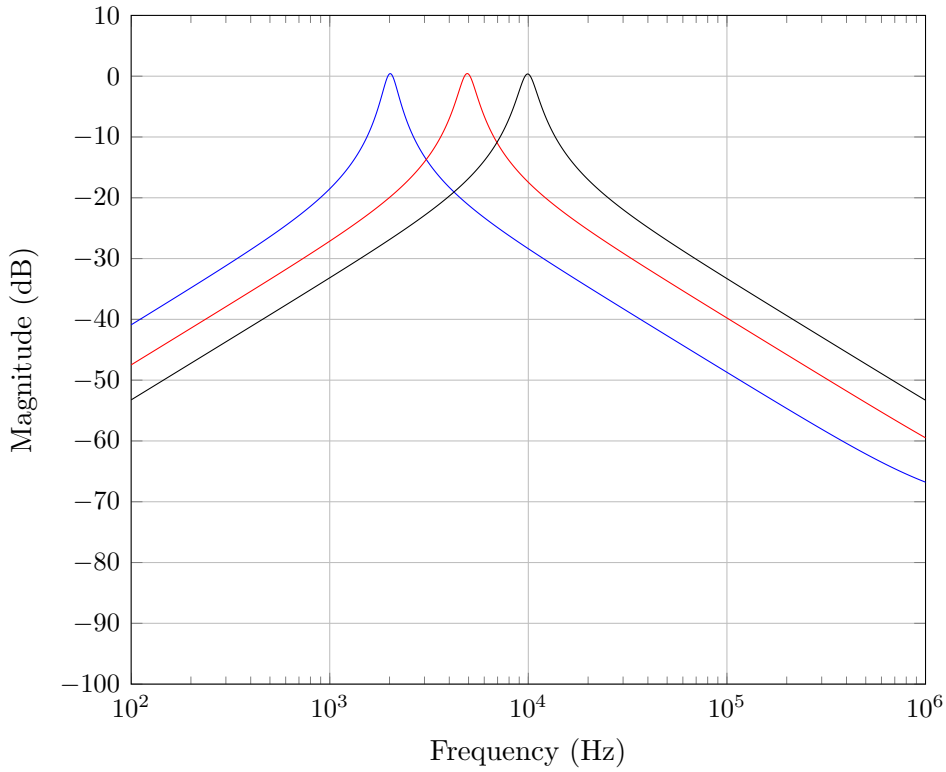

Figure 4: Macro-model based simulation of the 2nd order OTA-C^4 filter spectral responses at —— $f_c = 2$ kHz, —— $f_c = 5$ kHz, and —— $f_c = 10$ kHz, demonstrating the ability to adjust the filter center frequency across the initial required operational frequency spectrum.

3.3 Filter Implementation in 130-nm 1.2 V CMOS

Upon proving the viability of the OTA-C^4 as a foundational solution to the project requirements with macro model simulation and transfer function verification, efforts began to implement and verify the design using device models from the 130-nm 1.2 V CMOS process design kit. In order to take advantage of the benefits offered in sub-threshold operation, the transconductors within the OTA-C^4 needed to be sized according to inversion coefficient to ensure operation in weak inversion remained constant over the range of required input bias currents. The first step in designing

by inversion coefficient required extracting the inherent technology current from the 130-nm CMOS device models for each type of device utilized in the design.

3.3.1 Technology Current Extraction

Utilizing the test bench schematic illustrated by Fig. 5, V_{DS} of an nFET was set such that the device under test operated in saturation, while V_{GS} was swept in order to observe the corresponding change in drain current, I_D. The technology current, or "on-current", is defined as the drain current of a minimum channel length device with the process supply voltage applied to the gate and drain of the transistor, while the source and body are grounded [10].

The resulting drain current versus gate voltage plots from the test bench in Fig. 5 are illustrated below in Fig. 6, along with the relevant device geometry information such as width, length, and multiplicity factor.

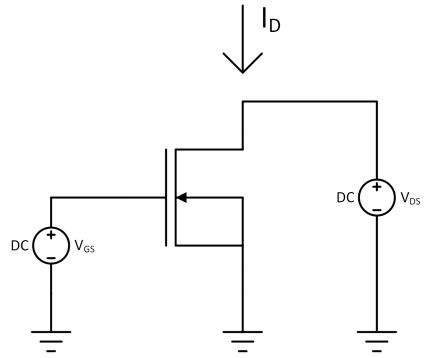

Figure 5: Simulation test bench used to obtain and verify the technology current characteristic of the utilized 130-nm CMOS process.

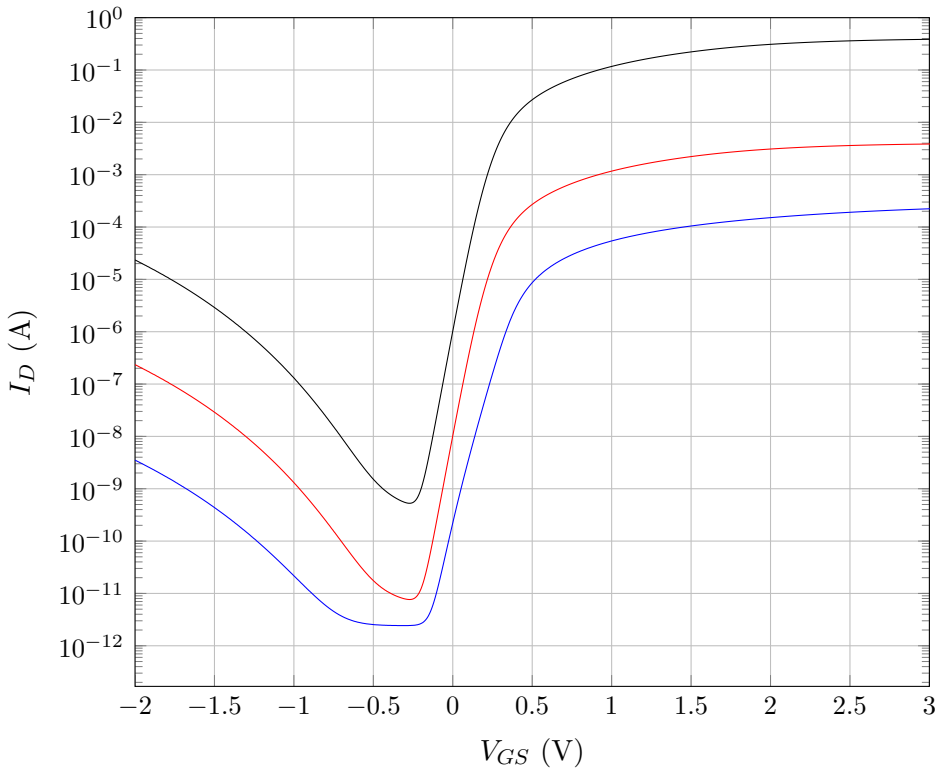

Figure 6: I_D vs. V_{GS}, illustrating the exponential relationship between I_D and V_{GS} in sub-threshold operation. —— Trace 1: $(W/L) = 160/130\,n\text{m}, mult = 1$, —— Trace 2: $(W/L) = 10/1\,\mu\text{m}, mult = 1$, and —— Trace 3: $(W/L) = 10/1\,\mu\text{m}, mult = 100$.

The following equation for inversion coefficient was then used to extract an approximate value for technology current, I_0 [10].

$$IC = \frac{I_D}{2n\mu C'_{OX} U_T^2 \left(\frac{W}{L}\right)} = \frac{I_D}{I_0 \left(\frac{W}{L}\right)} \tag{3.10}$$

The technology currents were calculated to be approximately $0.7\,\mu$A and $0.22\,\mu$A for nFET and pFET devices, respectively. For conclusive verification, this was compared and found to be consistent with the data provided within the 130-nm CMOS pro-

cess documentation. With the technology current known, device feature sizes were selected according to Eq. 3.10 to ensure operation far enough into weak inversion throughout the range of input bias currents.

In order to achieve sufficient device gain, avoid small channel effects, and improve device matching, the minimum gate length chosen for use in the OTA-C^4 was 0.5-μm in size, approximately 3.8$\times$ larger than the minimum device feature size. With an accurate method with which to ensure sub-threshold operation across the desired range of input bias currents, the OTA-C^4 schematic was built up in Cadence utilizing the 130-nm 1.2 V CMOS device models.

3.3.2 OTA-C^4 Simulation with CMOS Models

Before implementing the OTA-C^4 with 130-nm CMOS device models, a simplified OTA, seen in Fig. 7, without the added complexity of input-linearizing transistors was constructed for the purpose of examining the relationship between input bias current and the corresponding transconductance obtained. The simplified OTA proved helpful when exploring the limits of available transconductance for a given bias current, but as expected, exhibited a reduced linear transconductance range without the symmetric "bump" devices included on the input differential pair.

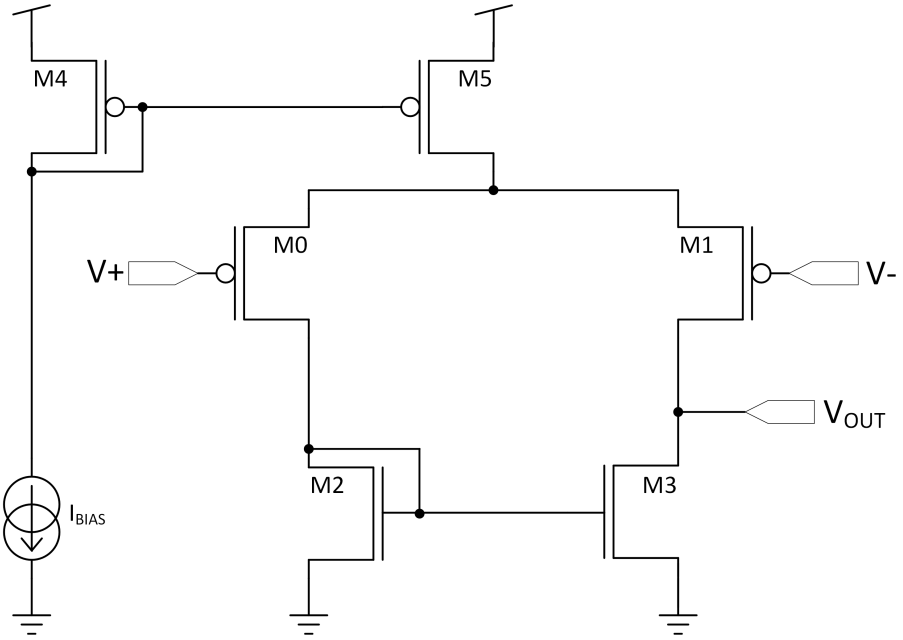

Figure 7: Simplified OTA used for initial simulations.

After this initial simulation step, Fig. 8 below illustrates the OTA-C^4 as implemented and simulated with 130-nm CMOS models. In the OTA-C^4 topology, the V+ terminal of the high-side transconductor controls the filter's dc operating point. In this work, this dc operating point was set to the mid-supply voltage, +0.6 V.

Due to the disparity between the constant dc level set by the non-inverting terminal of the high-side transconductor and the time-varying input signal on the inverting terminal, an imbalance in the tail currents of the input differential pair resulted. In order to balance the input differential pair tail currents, a low-voltage cascode current mirror was implemented in place of the original current bias design reported by the OTA-C^4 [1].

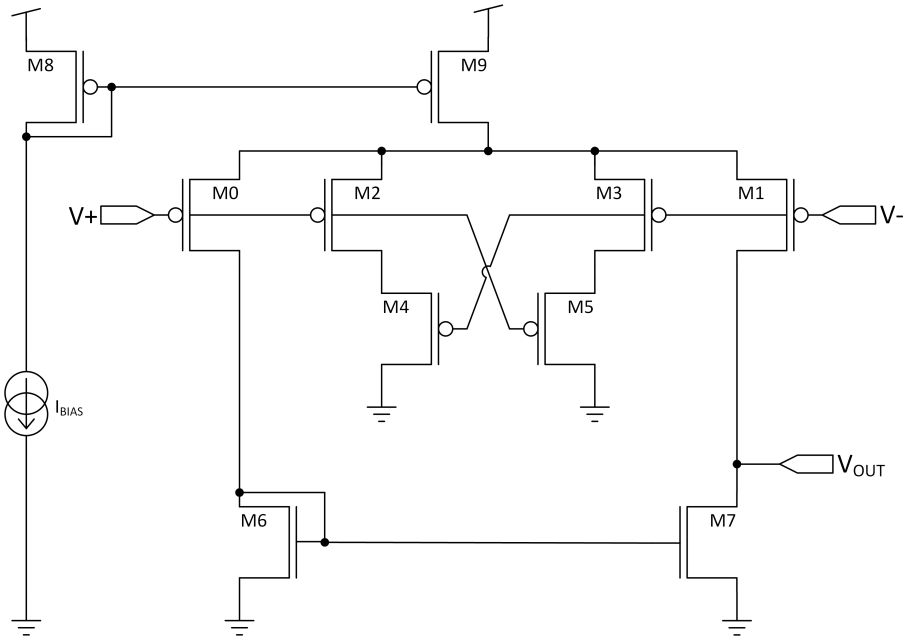

Figure 8: OTA-C^4 implemented in 130-nm CMOS [1].

With the low-voltage cascode current mirror, the output impedance of the mirror is increased, which aids in maintaining a constant balanced output current regardless of the loading conditions. Fig. 9 below illustrates the schematic of the MISA OTA, which is used to form a 2nd order MISA filter cell. The resulting device properties of the MISA filter cell implemented in the MISA-01 chip are presented below in Table 1, organized by reference designator as they appear in Fig. 9.

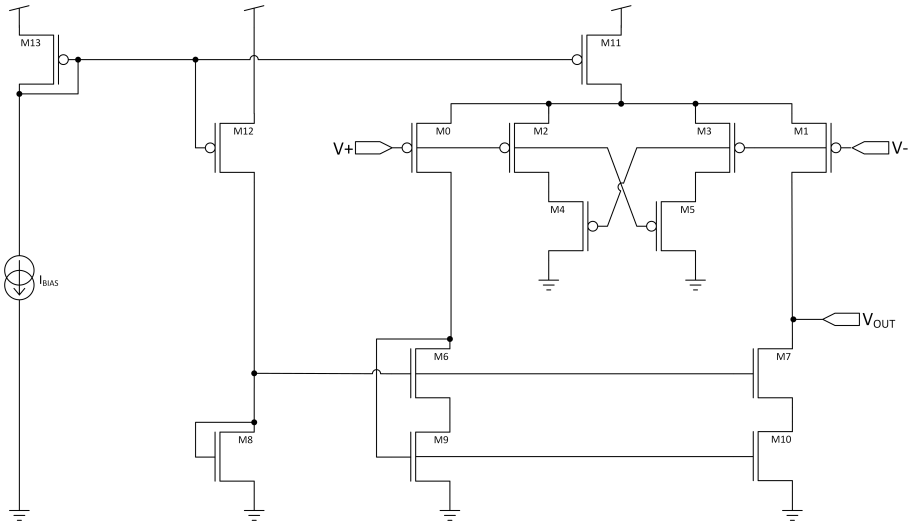

Figure 9: MISA filter cell implemented in 130-nm CMOS, with a cascode current-bias section, utilized to balance the tail currents of the input differential pair.

Table 1: MISA Filter Cell Device Specifications

Reference Designator	Device Type	Device Properties
M0 - M5	pfet	$\frac{W}{L} = \frac{30\,\mu\text{m}}{1\,\mu\text{m}}, nf = 1$
M6 - M7	nfet	$\frac{W}{L} = \frac{10\,\mu\text{m}}{0.5\,\mu\text{m}}, nf = 1$
M8	nfet	$\frac{W}{L} = \frac{2\,\mu\text{m}}{1\,\mu\text{m}}, nf = 2$
M9 - M10	nfet	$\frac{W}{L} = \frac{20\,\mu\text{m}}{10\,\mu\text{m}}, nf = 1$
M11 - M13	pfet	$\frac{W}{L} = \frac{20\,\mu\text{m}}{20\,\mu\text{m}}, nf = 4$

3.3.3 Simulating the Effective Transconductance

Transconductance is the primary mechanism by which the center frequency of G_m-C filters is dynamically adjusted; therefore, the relationship between input bias current and the transconductance obtained must be known in order to select capacitor values for a desired range of filter center frequencies. The following equation defines how the "effective" transconductance of the MISA OTA can be experimentally calculated for a given input bias current.

$$G_{m,eff} \approx \frac{I_{out,2} - I_{out,1}}{V_{in,dif2} - V_{in,dif1}} \tag{3.11}$$

By sweeping the differential input voltage on the MISA OTA, the resulting slope of the output current versus differential input voltage waveform yields an approximate value of the"effective" transconductance at a given bias point, via Eq. 3.11. However, this approximation is only accurate when the slope is taken at two points along which the change in output current and input differential voltage is linear, as demonstrated in Fig. 11. Relative to the "simplified" OTA used for initial testing, the MISA OTA has a linear range that is approximately four times greater than that of a standard differential pair due to the transconductance-linearizing effect of the cross-coupled "bump" devices [1, 8]. The following test bench schematic, Fig. 10, illustrates how the range of available "effective" transconductance values were simulated for a given bias current while maintaining sub-threshold device operation.

Maintaining a mid-supply reference voltage (+0.6 V) on the positive terminal of the MISA OTA, the input voltage applied to the negative terminal was swept

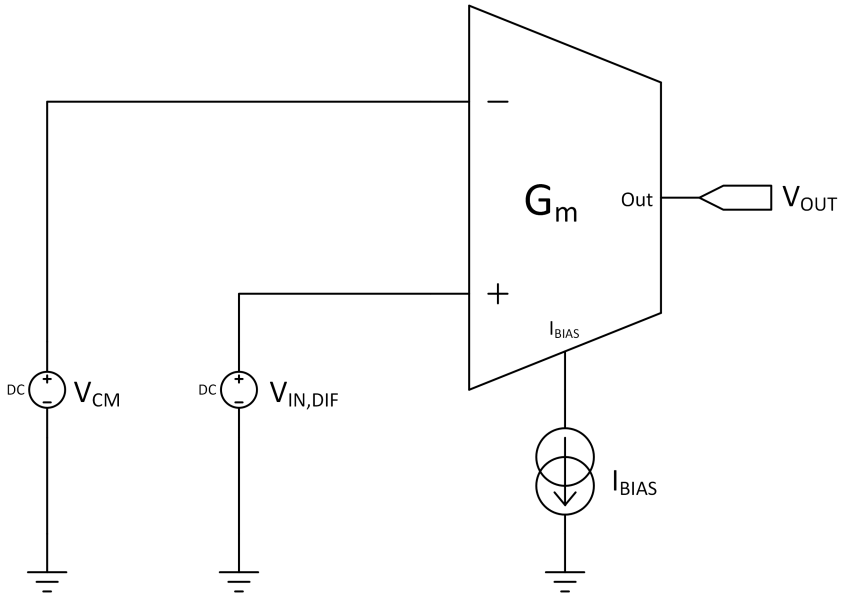

Figure 10: Test bench used to obtain the effective transconductance of a MISA OTA cell.

in order to observe the change in output current with respect to differential input voltage.

The range of input bias currents that maintain the required sub-threshold operation constraint was found by increasing the bias current until the MISA OTA moved into moderate inversion, consequently changing the filter transfer function. Across the linear range shown below in Fig. 11, the slope of the output current versus differential input voltage waveform approximates the effective transconductance of the MISA OTA.

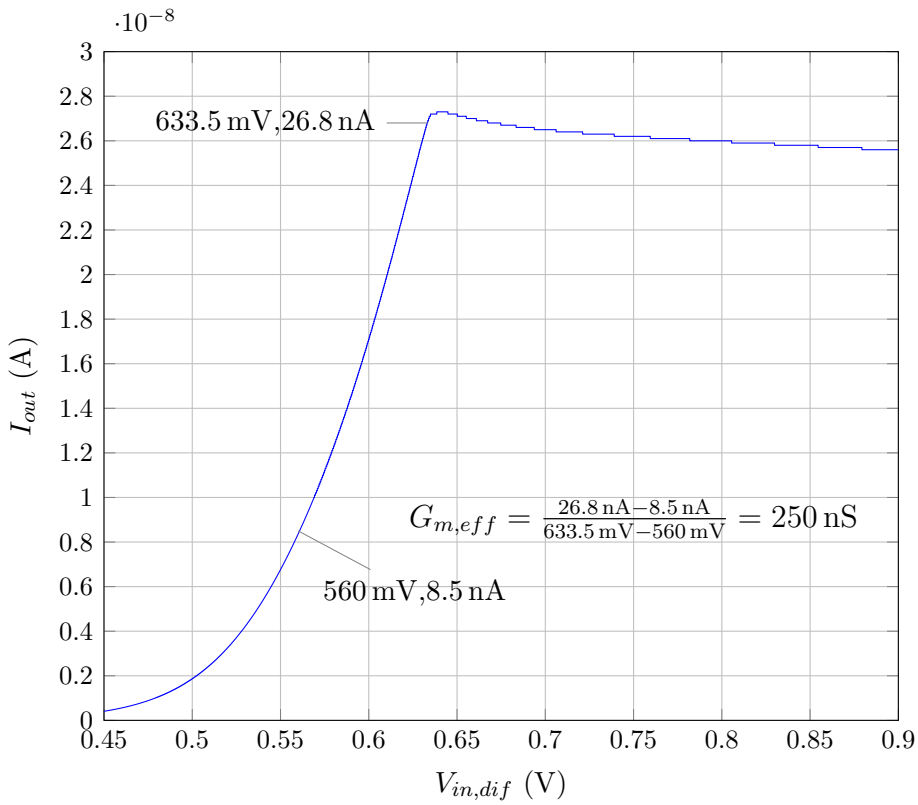

Figure 11: Simulated plot of I_{out} vs. $V_{in,dif}$, illustrating the change in output current that corresponds to a change in differential input voltage when biased with 15 nA of input current.

3.3.4 Filter Cell Optimization

With the basic relationship between input bias current and effective transconductance of an individual MISA OTA established, the capacitor values could be optimized to achieve a specific range of corner frequencies while maintaining device operation in weak inversion. Constrained by the range of transconductance values possible under the sub-threshold operational requirement, the MISA filter cell capacitor values were calculated accordingly. In combination with the capacitors defined

by Eq. 3.2 - 3.5, the transconductance values necessary for a desired time constant, and thus corner frequency as related by Eq. 3.9, were again estimated via Eq. 3.6 and 3.7 [1].

Although useful to obtain an estimate for the range of transconductances required, Eq.'s 3.6 - 3.7 define control of the independently-adjustable corner frequencies of the 2nd order MISA filter cell, with no consideration of filter characteristics such as gain and Q-factor. Concerning Q-factor, the independently-adjustable time constants defined above must be controlled such that a constant ratio between the low- and high-side transconductances is established, therefore allowing the high and low corner frequencies to form a single center frequency. Eq. 3.12 below defines this constant ratio of transconductances, R, which must be maintained in order to provide a consistent bandpass filter transfer function (Eq. 3.1) throughout the desired frequency spectrum.

$$R = \frac{G_{m,H}}{G_{m,L}} \tag{3.12}$$

With the necessary ratio of transconductances established, Eq. 3.13 and 3.14 define the relationship between center frequency and the low- and high-side transconductances, respectively [1].

$$G_{m,L} = \sqrt{\frac{C_O C_T - C_2^2}{R}} 2\pi f_c \tag{3.13}$$

$$G_{m,H} = R \cdot G_{m,L} \tag{3.14}$$

Additionally, varying the ratio of transconductances, R, impacts characteristics of

the 2nd order bandpass filter transfer function, and may be used to optimize for gain or Q-factor, with the highest Q-factor achieved when R is defined by Eq. 3.15 [1].

$$Q_{max} \Rightarrow R = \frac{G_{m,H}}{G_{m,L}} = \frac{C_L}{C_2} \tag{3.15}$$

With an emphasis in this work placed on obtaining a high Q-factor, the following derivation provides the relationship between the integrated capacitors, transconductance values, and Q-factor. Beginning with Eq. 3.16, the standard normalized 2nd order bandpass transfer function is rearranged by distributing ω_0 to allow all terms to be grouped by polynomial order, resulting in Eq. 3.17.

$$\frac{s\left(\frac{\omega_0}{Q}\right)}{s^2 + s\left(\frac{\omega_0}{Q}\right) + \omega_0^2} \tag{3.16}$$

$$\frac{s\left(\frac{1}{Q\omega_0}\right)}{s^2\left(\frac{1}{\omega_0^2}\right) + s\left(\frac{1}{Q\omega_0}\right) + 1} \tag{3.17}$$

The relationship between center frequency, ω_0, and the respective low- and high-corner frequency time constants τ_h and τ_l, is defined below in Eq. 3.18.

$$\omega_0 = \frac{1}{\sqrt{\tau_h \tau_l}} \tag{3.18}$$

The 1st order terms of the OTA-C^4 transfer function, Eq. 3.1, and Eq. 3.17 are then set equal to one another in Eq. 3.19, providing a convenient method with which to derive a closed-form expression defining Q-factor of the 2nd order bandpass filter.

$$\frac{1}{\omega_0 Q} = \tau_l + \tau_f \left(\frac{C_O}{C_2} - 1 \right) \tag{3.19}$$

Substituting Eq. 3.18 into Eq. 3.19 yields an expression for Q-factor dependent on 2 variables: capacitance and transconductance. This expression is seen below in Eq. 3.20, after ω_0 is distributed in order to isolate Q.

$$\frac{1}{Q} = \frac{\tau_l}{\sqrt{\tau_h \tau_l}} + \frac{\tau_f}{\sqrt{\tau_h \tau_l}} \left(\frac{C_O}{C_2} - 1 \right) \tag{3.20}$$

$$\frac{1}{Q} = \sqrt{\frac{\tau_l}{\tau_h}} + \frac{\tau_f}{\sqrt{\tau_h \tau_l}} \left(\frac{C_O}{C_2} - 1 \right) \tag{3.21}$$

Inserting Eq. 3.6 and 3.7 into Eq. 3.21, Eq. 3.22 replaces each time constant expression with the respective transconductance and capacitive terms.

$$\frac{1}{Q} = \sqrt{\frac{\frac{C_2}{G_{m,L}}}{\frac{C_O C_T - C_2^2}{C_2 G_{m,H}}}} + \frac{\frac{C_2}{Gm,H}}{\sqrt{\left(\frac{C_O C_T - C_2^2}{C_2 G_{m,H}} \right) \frac{C_2}{G_{m,L}}}} \left(\frac{C_O}{C_2} - 1 \right) \tag{3.22}$$

Eq. 3.23 and 3.24 provide algebraic simplification such that the complex denominators are removed from both terms.

$$\frac{1}{Q} = \sqrt{\frac{\frac{C_2^2 G_{m,H}}{G_{m,L}}}{C_O C_T - C_2^2}} + \frac{\frac{C_2}{Gm,H}}{\sqrt{\frac{C_O C_T - C_2^2}{G_{m,H} G_{m,L}}}} \left(\frac{C_O}{C_2} - 1 \right) \tag{3.23}$$

$$\frac{1}{Q} = \sqrt{\frac{\frac{C_2^2 G_{m,H}}{G_{m,L}}}{C_O C_T - C_2^2}} + \frac{\frac{C_2 \sqrt{G_{m,H} G_{m,L}}}{G_{m,H}}}{\sqrt{C_O C_T - C_2^2}} \left(\frac{C_O}{C_2} - 1 \right) \tag{3.24}$$

In Eq. 3.25, the complex numerators are simplified in both terms, allowing for regrouping of variables such that like terms are conveniently organized.

$$\frac{1}{Q} = \frac{C_2\sqrt{\frac{G_{m,H}}{G_{m,L}}}}{\sqrt{C_O C_T - C_2^2}} + \frac{C_2\sqrt{\frac{G_{m,L}}{G_{m,H}}}}{\sqrt{C_O C_T - C_2^2}}\left(\frac{C_O}{C_2} - 1\right) \tag{3.25}$$

In Eq. 3.26, like terms have been collected and rearranged, from which Eq. 3.5 may be substituted for C_O, and terms may be expanded and simplified accordingly.

$$\frac{1}{Q} = \frac{C_2}{\sqrt{C_O C_T - C_2^2}}\left[\sqrt{\frac{G_{m,H}}{G_{m,L}}} + \sqrt{\frac{G_{m,H}}{G_{m,L}}}\left(\frac{C_O}{C_2} - 1\right)\right] \tag{3.26}$$

Simplification yields Eq. 3.27, a concise, closed-form expression for Q-factor of the 2nd order filter that is dependent only on transconductance and capacitance [1].

$$Q = \frac{\sqrt{C_O C_T - C_2^2}}{C_L\sqrt{\frac{G_{m,L}}{G_{m,H}}} + C_2\sqrt{\frac{G_{m,H}}{G_{m,L}}}} \tag{3.27}$$

Informed by the simulated and calculated results in Sec. 3.3.3 concerning the range of effective transconductances possible when using the MISA OTA, as well as Eq. 3.2 - 3.5, the capacitor values selected for implementation in the MISA filter cell are provided below in Table 2.

The preceding derivation provided insight concerning the effect on Q-factor observed from adjusting the ratio of capacitors relative to one another, resulting in a ratio of $1:12$ between the smallest on-chip capacitor, C_2, at 5 pF, and the largest, C_W, at 60 pF. Inserting the MISA filter cell capacitor values into Eq. 3.27, the maximum theoretical Q-factor per 2nd order filter cell is approximately 2.15.

Table 2: 2nd order MISA Filter Cell Capacitor Values.

Capacitor	Value
C_1	15 pF
C_2	5 pF
C_W	60 pF
C_L	30 pF

3.3.5 Feed-Forward Prevention

As seen in the OTA-C^4 transfer function Eq. 3.1, a right-hand-plane zero exists in the numerator. In terms of the characteristic shape of the frequency response, this forms a shelf-like response at higher frequencies. This zero in the transfer function is caused by a feed-forward interaction, in which a direct path exists between the input and output of the filter via a small feedback capacitor. At high frequencies, the input signal is transferred to the output without inversion from the transistor's channel.

Without compensation, this can result in oscillation and overall system instability, as the current injected onto the output through the feedback capacitor increases with frequency, eventually equalling the controlled current source of the transistor, $g_m \cdot V_{gs}$. When this occurs, the current from the capacitor is fully absorbed by the transconductance of the transistor, and the output of the amplifier in the Laplace domain is zero. At this point, because the output voltage equals the input voltage,

both the current in the feedback capacitor and the current in the voltage-controlled current-source are defined by V_{gs}.

In order to restrict the current through the feedback capacitor to a unidirectional flow from the output to the input and block the feed-forward path, a source-follower is placed in series with the feedback capacitor. The sizing of the source-follower devices is set such that the C_{gs} of the source-follower is much smaller than the feedback capacitance, thus moving the right-half-plane zero to a much higher frequency, at which it does not directly interfere with the desired bandpass transfer function [11]. This technique for right-half-plane zero compensation was chosen instead of implementing a nulling resistor or an active resistor due to the straightforwardness and robustness of the implemented source-follower scheme over a wide range of bias currents, in addition to concerns about the required area, accuracy, and matching of an on-chip resistor.

Fig. 12 below illustrates the simulated effects of including the source follower within the feedback loop, resulting in reduction of the characteristic shelf at high frequency down to the noise floor of the device, therefore maximizing the available dynamic range.

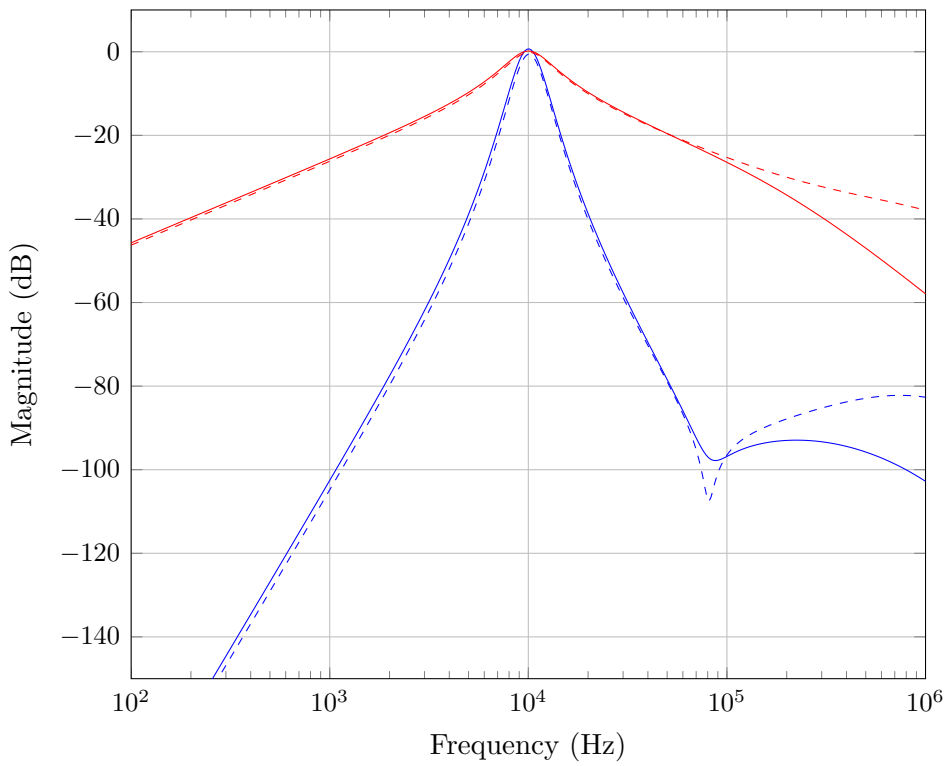

Figure 12: Simulated filter spectral responses comparing the - - - 2nd order response without RHPZ cancellation, —— 2nd order response with RHPZ cancellation, - - - 8th order response without RHPZ cancellation, and —— 8th order response with RHPZ cancellation at $f_c =$ 10 kHz.

3.4 8th Order Filter Channel Topology

Despite demonstrating operation at and above unity gain across the operational frequency spectrum of interest, the Q-factor provided by a single 2nd order MISA filter cell was not sufficient for integrated spectral analysis applications. Therefore, implementing four 2nd order MISA filter cells cascaded in series, as seen below in Fig. 13, yields an 8th order bandpass filter channel, with a greatly improved dynamic range. The closed-form expression for Q-factor derived earlier, Eq. 3.27, is formally

defined only for a 2nd order bandpass filter. However, this derivation is still valid in describing the Q-factor of the 8th order bandpass filter channel transfer function, as the channel is comprised of identical 2nd order filter cells, with the same Q-factor characteristics. Additionally, the 8th order filter channel was implemented such that no individual 2nd order filter cell within the channel could be modified independently; but rather, adjustments to the filter were applied to each filter cell within the channel. The term $Q_{effective}$, defined below in Eq. 3.28 as the -3 dB bandwidth relative to the center frequency, will be used in order to describe the effective quality factor obtained with an 8th order filter channel [12].

$$Q_{effective} = \frac{f_c}{BW_{-3\,\text{dB}}} \tag{3.28}$$

Additionally, 2 identical unity-gain operational amplifiers were implemented between the output of each MISA filter cell and the input of the next. The two integrated op-amps served to buffer the output of each MISA filter cell within the channel off-chip, and into the next filter cell, respectively. The op-amps which buffer the output of each filter cell off-chip are not shown in 13. Buffering between each MISA filter cell in the channel was included in order to decouple the output capacitance of the previous filter cell from the input capacitance of next filter cell, and ensure that each filter stage was capable of driving the capacitive load of the next filter cell.

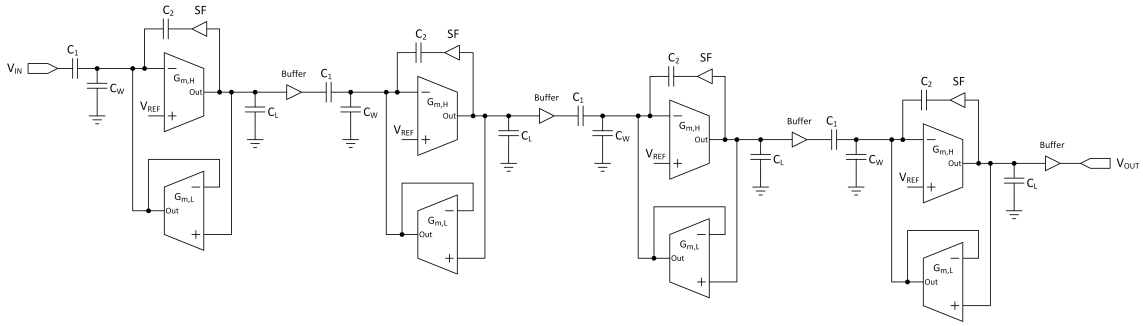

Figure 13: 8th order MISA filter channel topology consisting of four MISA filter cells cascaded in series, with unity-gain buffering between each filter cell.

Fig. 14 readily illustrates the improvement in $Q_{effective}$ obtained from connecting the filters in series by providing a comparison between the transfer functions of a single 2nd order MISA filter cell and that of 4 MISA filter cells cascade-connected in series. The inclusion of the unity-gain op-amp buffers between each MISA filter cell provided visibility to the 2nd, 4th, 6th, and 8th order outputs of each filter cell within a MISA filter channel.

3.4.1 Channel Current Bias

The reported floating-gate bias scheme of the OTA-C^4 was not considered practical for this application; therefore a more traditional current source was utilized. Similarly, a standard, low-voltage cascode current mirror was not a good candidate for the MISA current bias cell, as the range of required bias currents was too great to maintain operation in saturation while using a single circuit implemented with the same device properties. Due to the required operational frequency spectrum, a highly dynamic current bias structure was required in order to ensure accurate and

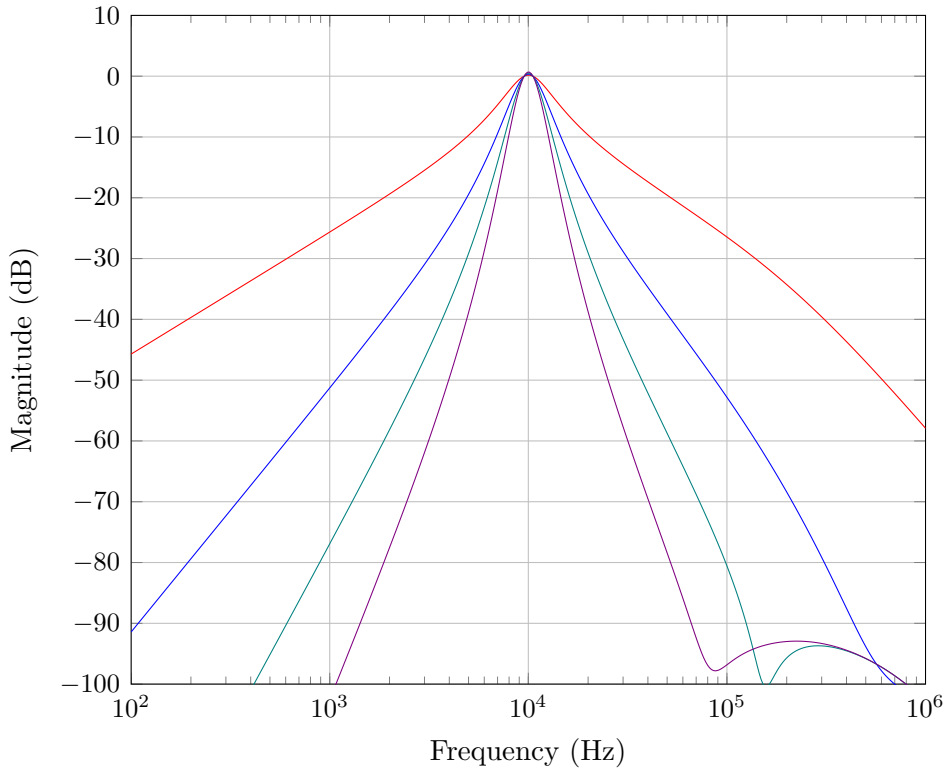

Figure 14: Simulated filter spectral response comparison between the —— 2nd order, —— 4th order, —— 6th order, and —— 8th order outputs of the MISA filter channel under unity-gain Simulated Theoretical Bias conditions for $f_c = 10$ kHz.

predictable bias currents, which in turn are used to set the effective transconductances of the filter cells. The Minch current mirror proved to be the needed current bias circuit, as its dynamic performance ensured operation in saturation from 18 μA down to 15 nA of input bias current [13]. Fig. 15 illustrates the schematic of the Minch current mirror implemented as the current bias cell in the MISA filter channel.

Regarding the overall system topology for a filter channel, each MISA current bias cell mirrored five output currents from its input bias current. Of the five output currents of the MISA current bias cell, four outputs were connected to the respective

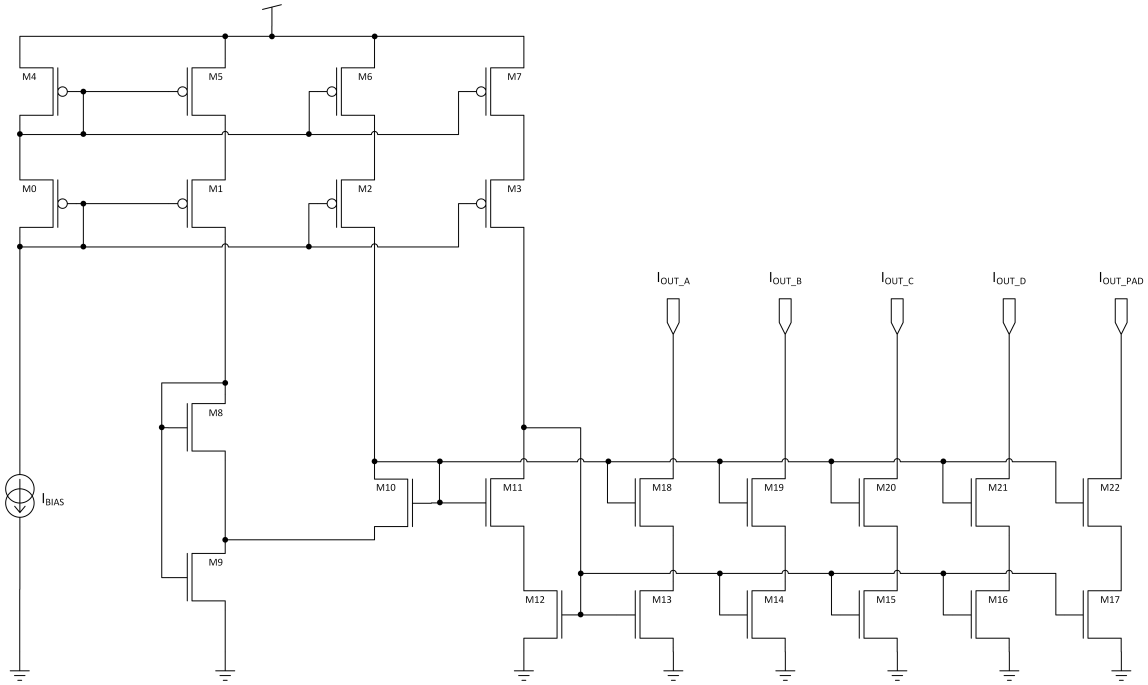

Figure 15: Schematic of the Minch current mirror cell used to bias each filter cell within a MISA filter channel.

inputs at each of the four stages in the MISA filter channel, ensuring each filter cells' transconductors received identical bias currents, therefore improving the accuracy of the resulting center frequencies at each filter stage. The remaining output current was connected directly to an output pad on the MISA-01 chip and connected to a high-value resistor, allowing for measurement of the output bias current. Four MISA current bias cells were implemented in each channel in order to independently control the bias currents of all low-side transconductors, high-side transconductors, source-follower stages, and output op-amp buffers within a MISA filter channel in unison and with a high degree of accuracy.

3.5 Fabrication in 130-nm 1.2 V CMOS

In implementing the MISA filter channel in 130-nm CMOS, obtaining a high degree of matching between the on-chip capacitors of the MISA channel filter was of primary importance. In an effort to reduce variation in filter cell capacitance both locally within a channel and between individual chips, a common-centroid capacitor array was implemented.

Figure 16: Block diagram illustrating the common centroid technique utilized to layout the capacitors of the OTA-C^4 filter cell with unit capacitors.

Illustrated below in Fig. 16, a unit cell of approximately 5 pF was selected, with the appropriate number of unit cells combined in parallel to achieve the capacitor values listed in Table 2. Ideally, placing "dummy" unit capacitor cells with no connection around the perimeter of the common-centroid capacitor array reduces edge-defects in fabrication, thus improving the matching of the interior capacitor array. However, in order to fit 4 MISA filter cells in series within the MISA-01 pad-frame, the perimeter "dummy" capacitors were not included.

A microscope photograph of a MISA-01 bare die is provided below in Fig. 17, along with a super-imposed layout view of a single MISA filter channel, identifying the individual sub-circuits implemented within a filter channel and the stand-alone test cells included on the MISA-01 chip. In addition to two 8th order MISA filter channels, the MISA-01 chip contains two individual 2nd order filter cells, a single op-amp cell, and the associated current bias structures required by each test cell.

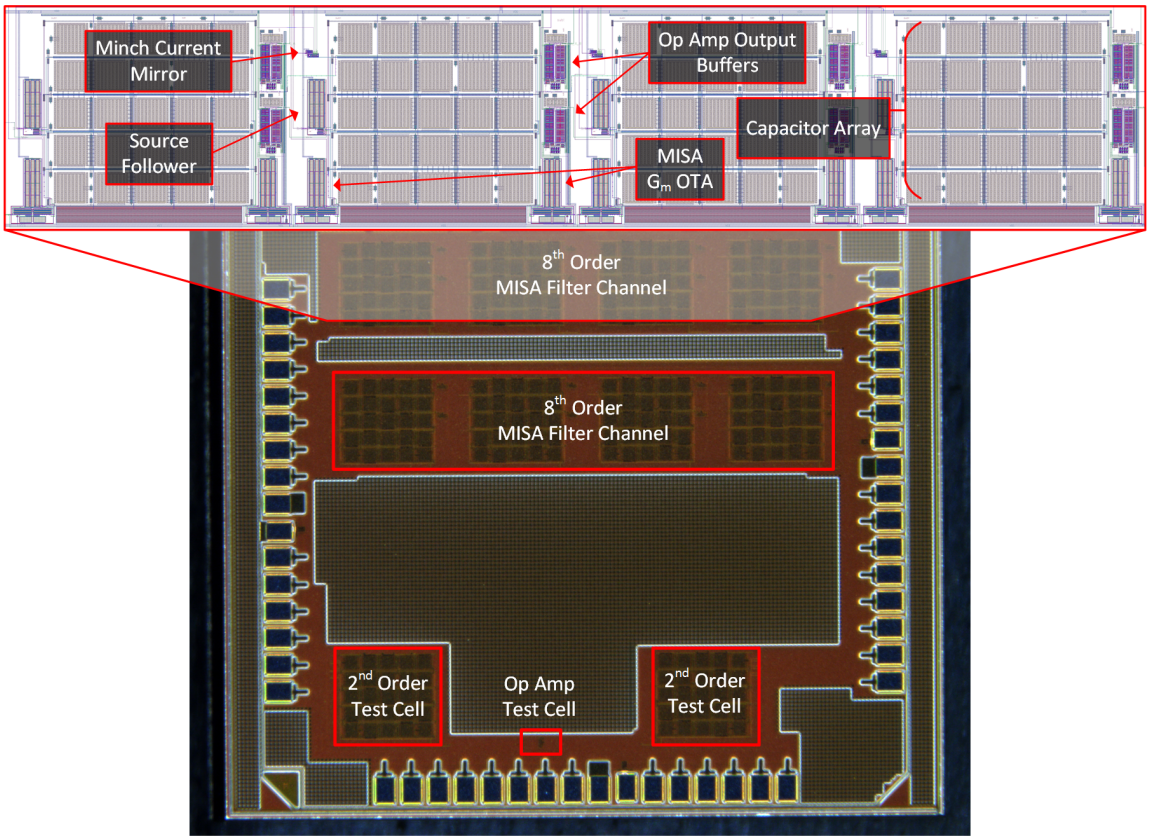

Figure 17: Microscope photograph of a bare die MISA-01 chip with the layout of a MISA filter channel overlaid with section labels.

4 Test Measurements and Post-Fabrication Verification

Within the following sections of this work, the terms "Measured Corrected Bias", "Measured Theoretical Bias", and "Simulated Theoretical Bias" are used to describe the bias conditions under which the performance of the MISA chip was evaluated. The term "Theoretical" indicates ideal bias conditions in which filter performance degradation due to parasitics is not taken into consideration. The term "Measured" indicates that the corresponding data was physically measured on the lab bench, and includes parasitic non-idealities and fabrication process variation. The term "Corrected" refers to a bias condition which began with the theoretical value, but then required manual adjustment to correctly position the center frequency of the filter. Lastly, "Simulated" refers to the use of a computer based simulation tool, and unless otherwise noted, also does not account for parasitic non-idealities that degrade theoretical performance. Identical to the "Simulated Theoretical Bias" conditions, the term "Measured Theoretical Bias" refers to the bias conditions calculated and obtained via simulation, which were then recorded as the standard "expected" values upon which tuning the MISA filter channel is based.

4.1 MISA Filter Channel Evaluation Setup

The 6 mm x 6 mm MISA-01 die were packaged in a 64-pin Quad Flat No-lead (QFN) package, which was hosted on an evaluation printed circuit board (PCB) via an "open-top" socket. The 4-layer test PCB contained the necessary peripheral

devices to buffer a signal in and out of the Device Under Test (DUT), provide adjustable current bias conditions, and power down test cells and filter channels when not in use to isolate power consumption measurements to a single channel. Seen below in Fig. 18, the basic signal chain implemented includes LEMO connectors for signal I/O, AC-coupled input and output unity gain buffers, and a voltage-trimmed op-amp current bias.

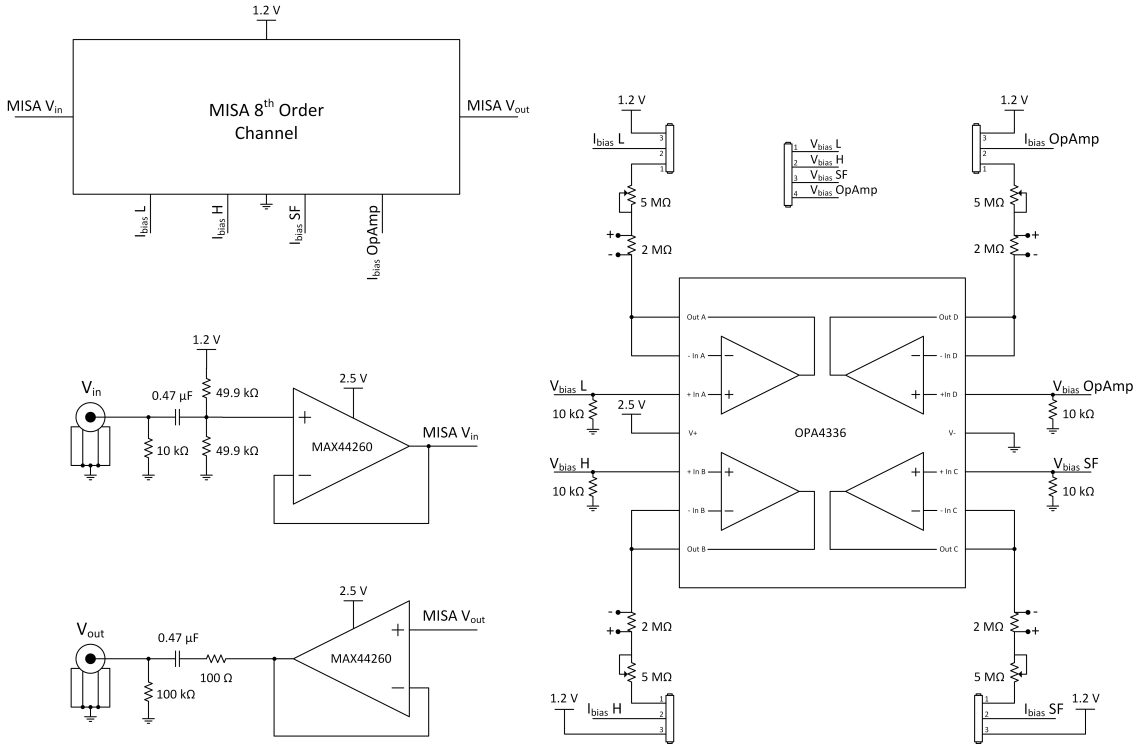

Figure 18: Single channel schematic overview of the MISA evaluation circuit. Note that this circuit topology was utilized for each channel of the MISA evaluation PCB.

The DUT is powered by an isolated 1.2 V supply rail, as specified by the CMOS process design kit. The MAX44260 op-amps utilized as unity-gain I/O buffers were selected for their low-distortion, low voltage-noise performance, in addition to provid-

ing rail-to-rail input and outputs. By setting the voltage supply for the I/O buffers is set at 2.5 V, which in combination with rail-to-rail input and output capabilities, ensures that the buffers do not degrade the dynamic range of the DUT, which is confined to a 1.2 V supply rail. Three-pin headers are placed in-line with the current bias circuit, providing the option to tie the input drain of the on-chip current bias structures to a 1.2 V supply rail, and effectively shut down the on-chip bias structure, or to the op-amp controlled current bias on the evaluation PCB. A 25-turn 5 MΩ potentiometer connected in series with a low-tolerance 2 MΩ resistor to the output of the PCB op-amp current bias allows the bias current to be calculated via a voltage measurement across the 2 MΩ resistor. When lower bias currents are required, a positive voltage may be applied to the V+ terminal of the op-amp current bias, which places a positive potential between the bias resistors and ground, thus lowering the potential difference across the resistors and reducing the bias current. Through the use of I/O headers, jumpers may be placed such that a filter channel or any peripheral I/O device can be shut down or placed in a low-power state when not in use, allowing for a high-level of test and measurement configurability. Fig. 19 below provides descriptive overlays above the MISA-01 evaluation PCB, illustrating the location and high-level functionality of the major test circuit components.

The HP3589A Spectrum/Network Analyzer was utilized as the primary piece of test equipment for measuring filter spectral response due to it's low frequency measurement performance and LabView-controllable data capture capabilities. The Swept Network mode of the HP3589A was utilized to measure filter spectral response, whereas the Swept Spectrum mode was used to obtain Total Harmonic Distortion

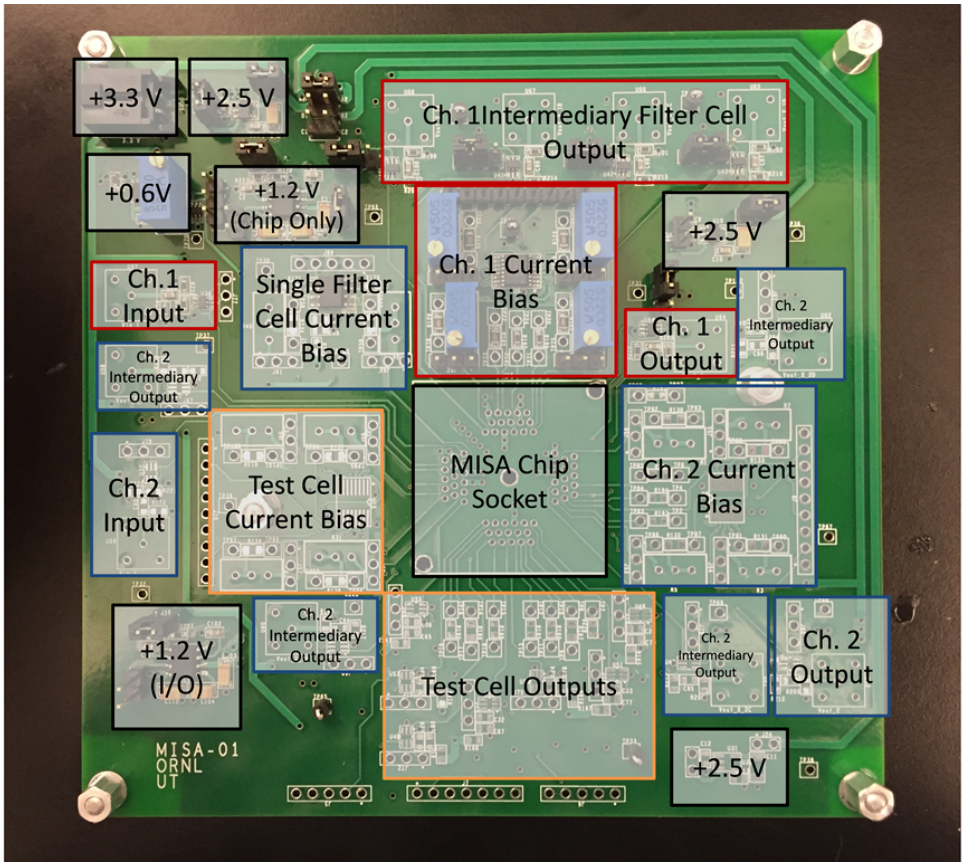

Figure 19: Section label overlay of the MISA evaluation PCB.

data. For all filter spectral response measurements, the input stimulus signal was set at 70 $mV_{p\text{-}p}$, unless otherwise specified. Once the correct bias conditions were set, an average of 10 scans was acquired and exported by LabView as a raw data file. A DC power supply was required to provide the global +3.3 V voltage rail for the evaluation PCB, from which all other voltage rails were generated. An Agilent 33522A Function/Arbitrary Waveform Generator was utilized to provide an input stimulus when testing the linear range of the MISA filter. Fig.20 below shows the MISA-01 Evaluation PCB fully populated, with filter I/O connected to the HP3589A.

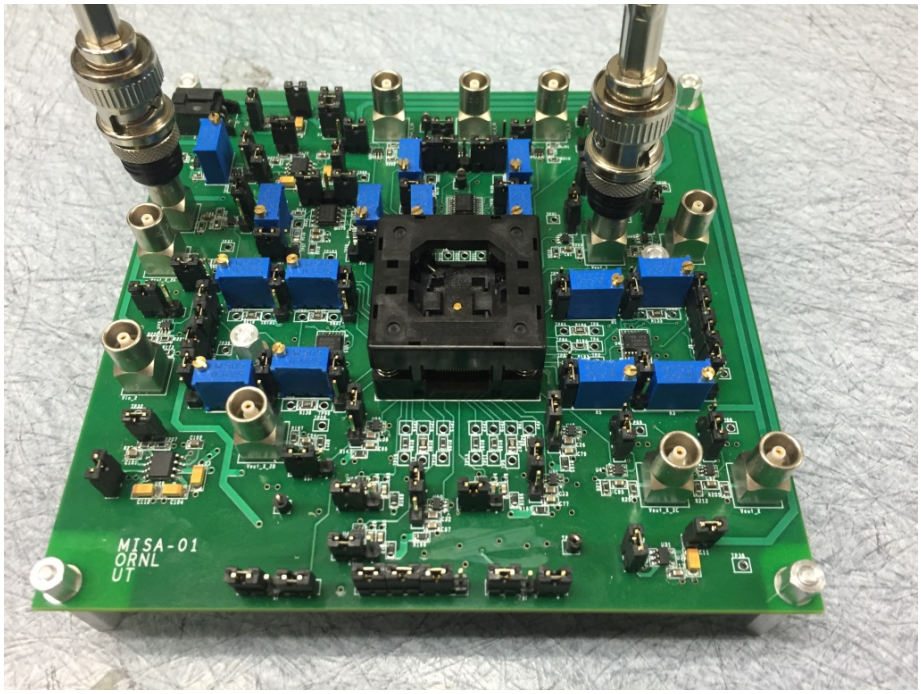

Figure 20: MISA evaluation PCB fully populated with bias circuits, peripheral I/O, and IC "open-top" socket.

4.2 MISA Filter Channel Linear Range

As discussed in Section 3.3.2, the benefit of adding symmetric "bump" transistors to the input differential pair of an OTA is an improved filter dynamic range via the linearization of the transconductors [1, 8]. Seen below in Fig. 21, as the input signal amplitude continues to increase, the output signal eventually stops tracking its theoretical response to the input stimulus, and the gain starts to drop off. At some point, with a large enough input signal, the output signal of the filter no longer increases, and the filter output is considered fully saturated, at which point the filter's response to input signals is nonlinear, resulting in distortion of the input signal [14]. The point at which the filter output deviates from the expected theoretical response

by 1 dB is the compression point of the filter, which was measured to be at an input voltage of approximately 140 $mV_{p\text{-}p}$.

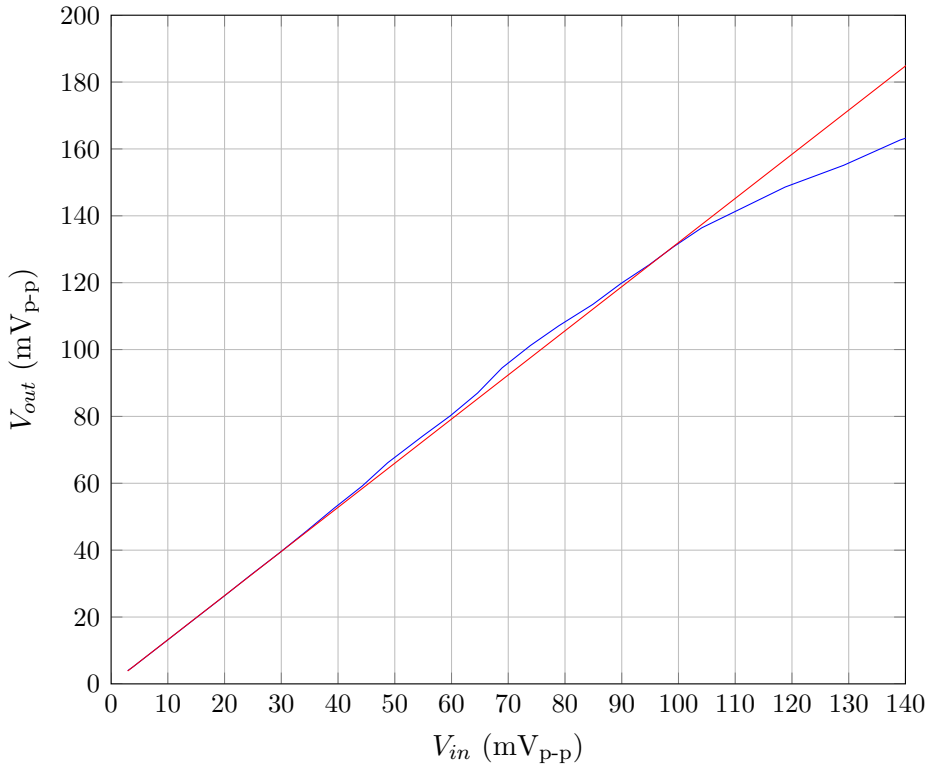

Figure 21: $V_{out,p-p}$ vs. $V_{in,p-p}$ linearity range, illustrating a linear output versus input response up to approximately 110 $mV_{p\text{-}p}$, and the 1 dB compression point beginning at approximately 140 $mV_{p\text{-}p}$.

4.3 Filter Spectral Response

Filter spectral response measurements are presented in this section, organized according to center frequency, chip tested, and channel. The measurement data from two of the five chips tested is presented in the body of this work, with the data

of the remaining three chips presented in Appendix B. Measurements were taken at 4 different center frequencies of interest: 2 kHz, 10 kHz, 50 kHz, and 100 kHz. The data from each channel of a single chip is presented adjacent to one another, with Ch. 1 always on the left, and Ch. 2 on the right.

4.3.1 $f_c = 2$ kHz

The $f_c = 2$ kHz filter spectral response of Chip 1, Ch. 1 and Ch. 2, is presented below in Fig. 22. In Ch. 1, the Measured Theoretical and Corrected Bias waveforms match well, but the gain and $Q_{effective}$ of the Simulated Theoretical waveform were unattainable.

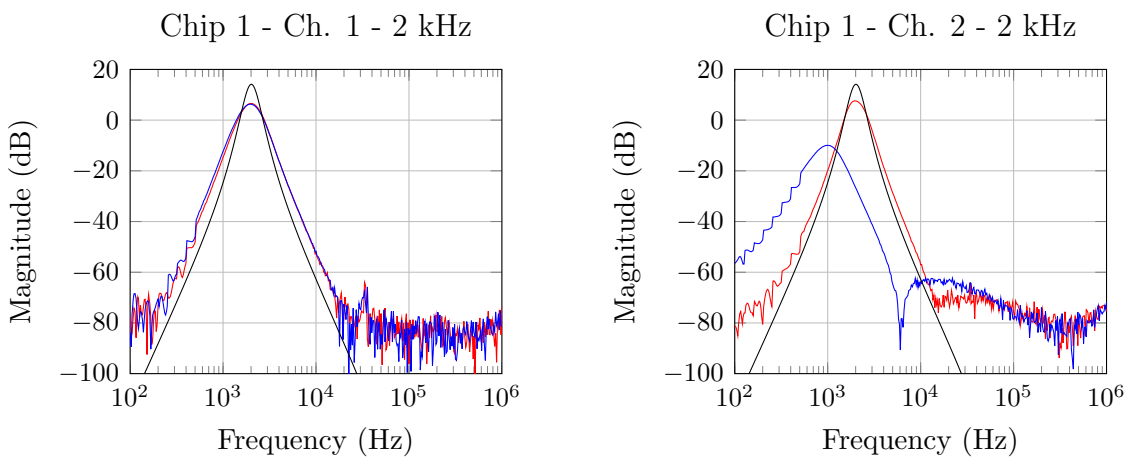

Figure 22: Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) under —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 2$ kHz.

The Measured Theoretical Bias waveform of Ch. 2 varies significantly from the Simulated Theoretical Bias waveform, whereas the Measured Corrected Bias wave-

form closely matches its $Q_{effective}$ without the additional gain. The primary reason behind this variation is due to the bias conditions required to set the filter center frequency at 2 kHz, the lowest value in its intended operational range. The low-side transconductance for a center frequency of 2 kHz requires a bias current of approximately 15 nA. Only slight variation between the device properties of a fabricated MISA filter channel and the ideal device properties is required to render the Theoretical Bias conditions ineffective, particularly when biased at low frequencies.

The issue is most pronounced at low frequencies because at the low bias currents associated with low frequency operation, the output devices in the Minch current mirror are on the border between linear and saturated operation, and thus the output bias currents are subject to undesired variation. However, minimal tuning of the low-side bias current is required to offset any effects from device mismatch and bias the Minch current mirror such that all output devices are saturated as expected. This is demonstrated by the difference between the Measured Theoretical and Measured Corrected Bias conditions of Chip 1, Ch. 2 at $f_c = 2$ kHz. Increasing the low-side bias current by approximately 2.67 nA brought the filter spectral response back into the expected characteristic bandpass shape.

The filter spectral response of Chip 2 at $f_c = 2$ kHz, illustrated below in Fig. 23, demonstrates a close match in Ch. 1 in terms of shape between the Measured Theoretical and Measured Corrected Bias conditions, but a significant disparity in filter gain exists. However, an additional 8 dB of gain was obtained after adjustment, but matching the simulated gain at $f_c = 2$ kHz was not possible.

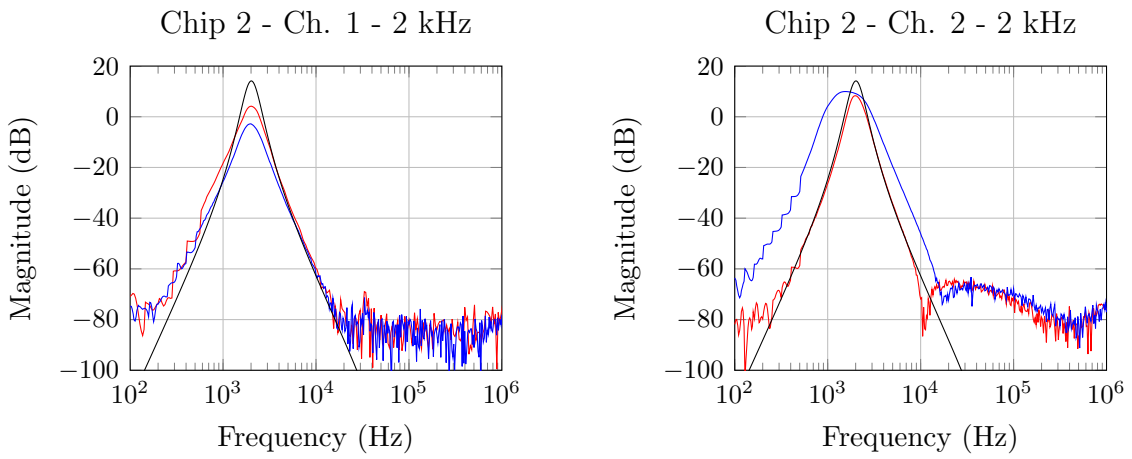

Figure 23: Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) under —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 2$ kHz.

In Ch. 2 of Chip 2, the Theoretical Bias conditions were not accurate for the same reasons as discussed above - the current bias structure was not fully saturated under Theoretical Bias conditions, resulting in a severe filter performance degradation. Similarly, a low-side bias current increase of approximately 1.5 nA restored the filter spectral response to the expected characteristic shape. Compared to Ch. 1, Ch. 2 offered more gain, but at the expense of dynamic range, as the high-side filter corner exhibited slight peaking at higher frequencies. However, lowering the gain of the filter cell removes the high frequency peaking, and restores the expected dynamic range to the filter spectral response. In general, the MISA filter channel was most vulnerable to variation in terms of filter gain and characteristic shape at $f_c = 2$ kHz than at higher frequencies. This vulnerability can be addressed in future design efforts by resizing the devices in the filter current bias cell to lower $V_{ds,sat}$, thus improving the bias current stability at the low end of the operational frequency spectrum.

4.3.2 f_c = 10 kHz

At f_c = 10 kHz, the differences in filter gain and shape under Measured and Simulated Bias conditions were much less significant. Seen below in Fig. 24, the filter spectral response of Chip 1 under Measured Theoretical Bias conditions exhibits a slight degradation in $Q_{effective}$ in Ch. 1 and f_c accuracy in Ch. 2.

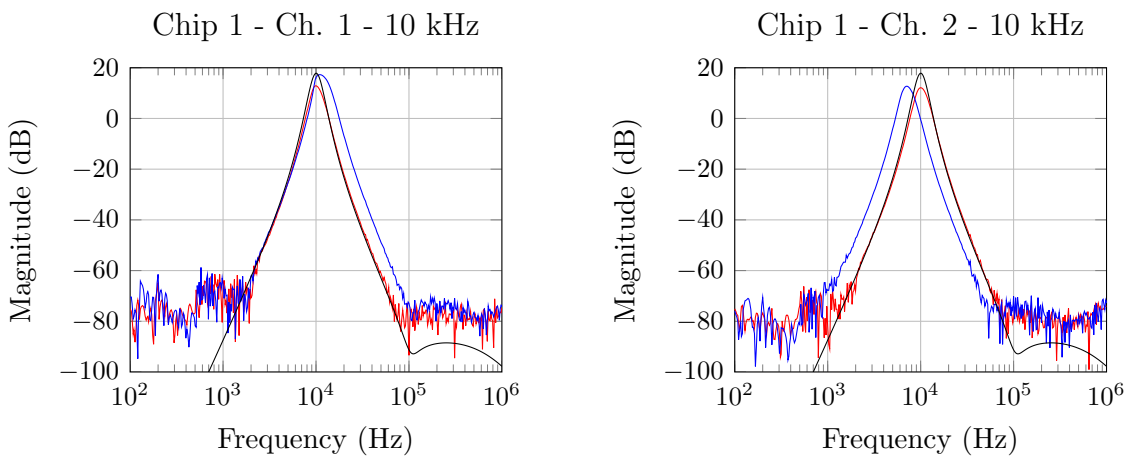

Figure 24: Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for f_c = 10 kHz.

However, after adjustment, the filter spectral response under Measured Corrected Bias conditions proved extremely accurate when compared to the Simulated Theoretical Bias response, excluding a slight loss of filter gain. The filter spectral response of Chip 2 at f_c = 10 kHz, seen below in Fig. 25, demonstrates the trade-off between $Q_{effective}$ and filter gain. The filter spectral response of both Ch. 1 and Ch. 2 exhibit filter gain under Measured Theoretical Bias conditions that is nearly identical to the gain observed in the Simulated Theoretical Bias waveform, but at the expense of $Q_{effective}$.

Once adjusted under Measured Corrected Bias conditions, both filter spectral responses closely match the Simulated Theoretical Bias waveform in terms of $Q_{effective}$ and overall characteristic shape. Compared to operation at $f_c = 2$ kHz, the output devices in the filter current bias structure at $f_c = 10$ kHz are operating sufficiently far enough into saturation, providing an overall more accurate and stable filter spectral response. Additionally, no undesired peaking occurs in the filter spectral response at higher frequencies, resulting in a more consistent dynamic range.

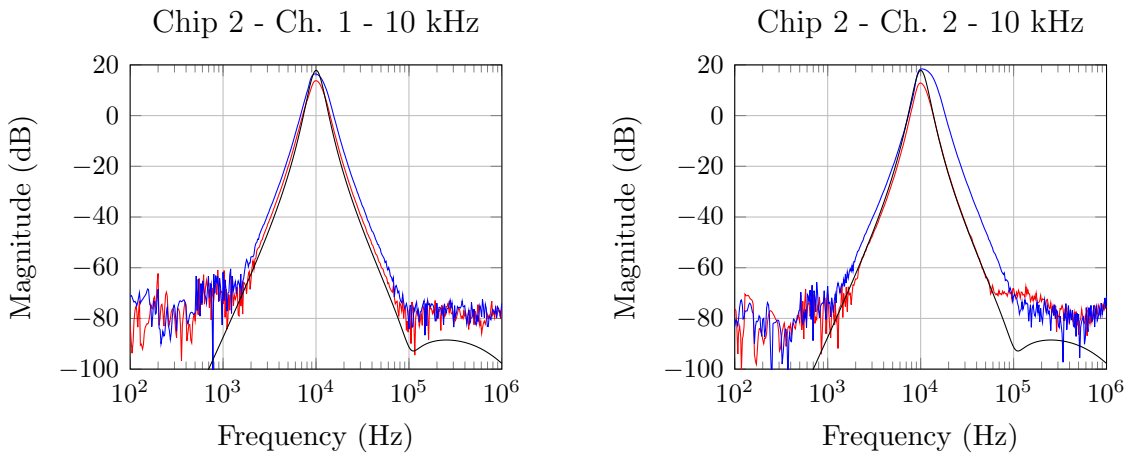

Figure 25: Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 10$ kHz.

4.3.3 $f_c = 50$ kHz

The $f_c = 50$ kHz filter spectral response of Chip 1, Ch. 1 and Ch. 2 is presented below in Fig. 26. Comparing the filter spectral responses under Measured Theoretical Bias and Measured Corrected Bias conditions, filter gain remains consistent, whereas

the $Q_{effective}$ improves under the Corrected Bias conditions. However, the measured spectral responses of both channels under Corrected and Theoretical Bias conditions exhibit a high degree of matching in terms of filter gain and $Q_{effective}$ relative to the Simulated Theoretical Bias waveforms. The only degradation observed is the high-side corner of the filter channel, which drops down to the measurement baseline more gradually than in the Simulated Theoretical Bias waveform.

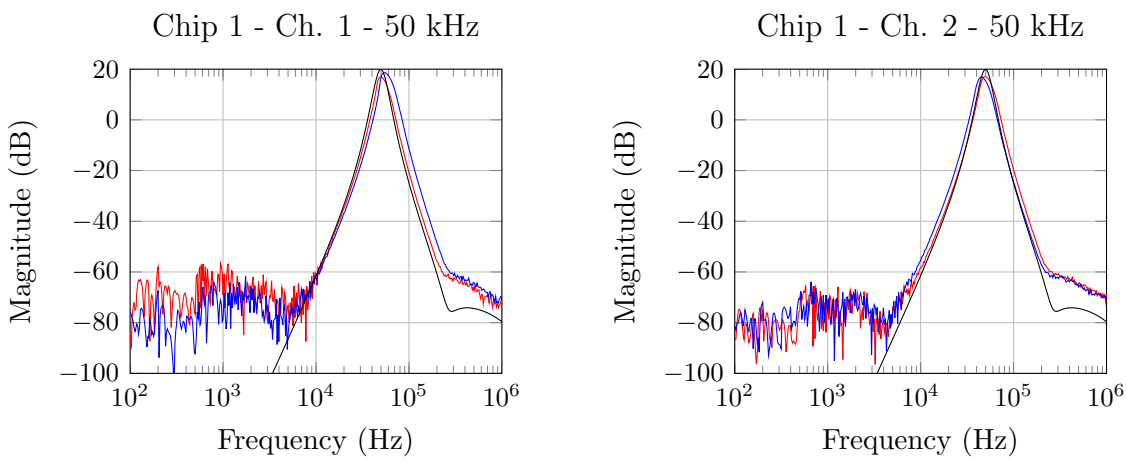

Figure 26: Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 50$ kHz.

Seen below in Fig. 27, Chip 2's filter spectral response at $f_c = 50$ kHz demonstrates similar performance to that of Chip 1. Filter gain remains consistent between Simulated and both Measured waveforms, with the primary improvements obtained in $Q_{effective}$ under the Corrected Bias condition. The same gradual return to measurement baseline of the high-side filter corner is observed as well.

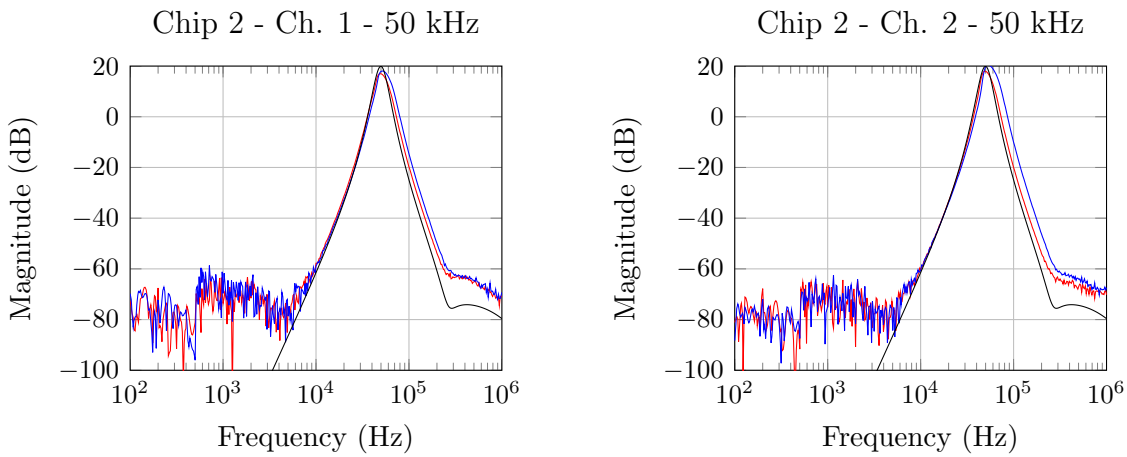

Figure 27: Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 50$ kHz.

4.3.4 $f_c = 100$ kHz

At $f_c = 100$ kHz, the MISA filter channel is operating at it's highest specified frequency. Illustrated below in Fig. 28, the filter spectral responses of Chip 1, Ch. 1 and Ch. 2, under both Measured Theoretical Bias and Measured Corrected Bias conditions match the Simulated Theoretical waveform quite well in regards to filter $Q_{effective}$. However, under Measured Theoretical Bias conditions, the filter gain was approximately 15 dB lower than the Simulated Theoretical Bias waveform. Once adjusted under Measured Corrected Bias conditions, the filter gain was increased, with the overall filter characteristic shape and $Q_{effective}$ remaining consistent.

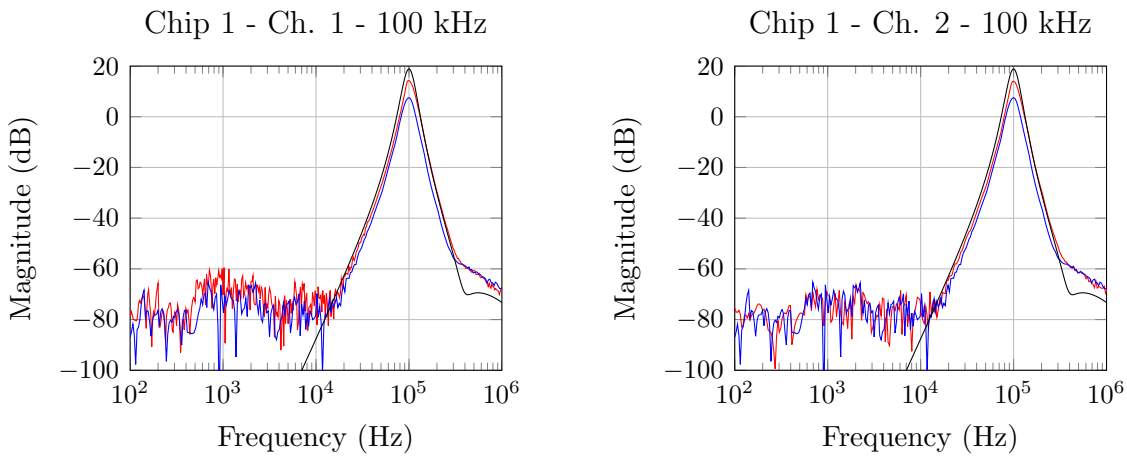

Figure 28: Filter spectral response of Chip 1 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz.

The $f_c = 100$ kHz filter spectral response of Chip 2, Ch. 1 and Ch. 2, is seen below in Fig. 29. Much like the performance of Chip 1, the differences between Measured Theoretical Bias and Measured Corrected Bias are slight, and manifest themselves only in filter gain. Although the filter gain of the Simulated Theoretical Bias waveform is not obtainable, the overall characteristic shape and $Q_{effective}$ are quite consistent under each bias condition.

Both channels of Chip 1 and Chip 2 exhibit the same gradual drop-off of the high-side filter corner back to measurement baseline as that seen at $f_c = 50$ kHz. However, similar to the high frequency peaking observed on the high-side filter corner at $f_c = 2$ kHz, this gradual return can be greatly improved by reducing the filter gain.

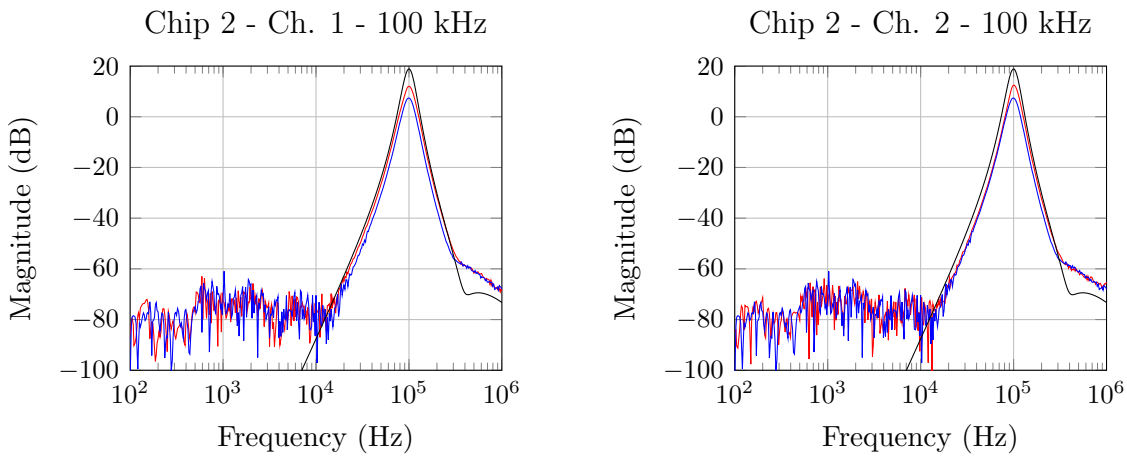

Figure 29: Filter spectral response of Chip 2 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz.

4.4 Filter Order Comparison

The following section will compare the 2nd order, 4th order, 6th order, 8th order, and 16th order filter spectral responses of the MISA filter channel. The outputs of each intermediary stage of the standard 8th order filter channel are overlaid in order to illustrate the gains in $Q_{effective}$ obtained by raising adding filters together in series. Two channels are connected together under the same bias conditions in order to provide the 16th order filter channel. The filter order comparisons are made at the same four center frequencies as the filter spectral responses presented in the preceding section - 2 kHz, 10 kHz, 50 kHz, and 100 kHz. All measurements are presented under the Measured Corrected Bias conditions, as process variation made the use of Measured Theoretical Bias conditions ineffective when connecting two channels together to form a 16th order channel.

4.4.1 $f_c = 2$ kHz

Fig. 30 below illustrates the filter order comparison for Chip 1 and Chip 2 at $f_c =$ 2 kHz. The improvements in $Q_{effective}$ obtained after each intermediary filter stage is connected are significant. The 2nd order spectral response exhibits peaking at high frequencies, starting at approximately 200 kHz. While not ideal, this high frequency peaking occurs at frequencies that are nominally 100× higher than the fundamental frequency. However, with each filter stage connected, the high frequency peaking is diminished greatly.

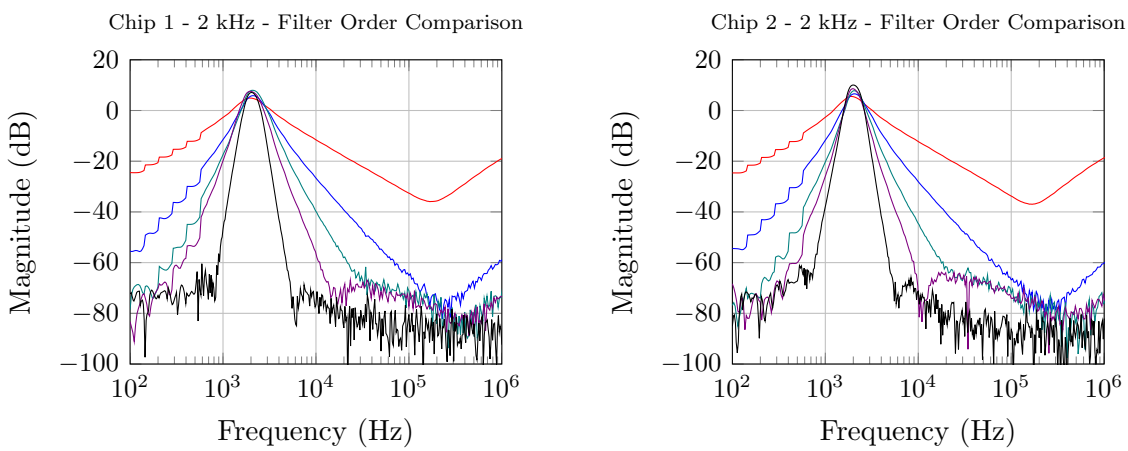

Figure 30: —— 2nd order, —— 4th order, —— 6th order, —— 8th order, and —— 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 2$ kHz.

The same filter shape and overall performance characteristic of Chip 1 is observed in Chip 2, with the exception that the 16th order spectral response of Chip 1 is arguably more symmetric than that of Chip 2. Additionally, both Chip 1 and Chip 2 exhibit the same high-frequency peaking in the 4th order spectral response as that

seen in the 2nd order spectral response, even though it begins at approximately -80 dB and slopes upward from 300 kHz and on.

4.4.2 f_c = 10 kHz

The filter order comparison at $f_c = 10$ kHz for Chip 1 and Chip 2 is seen below in Fig. 31. At $f_c = 10$ kHz, due to assured saturation of the devices in the filter current bias structure, the characteristic shape of the spectral responses are much more symmetric than those at $f_c = 2$ kHz.

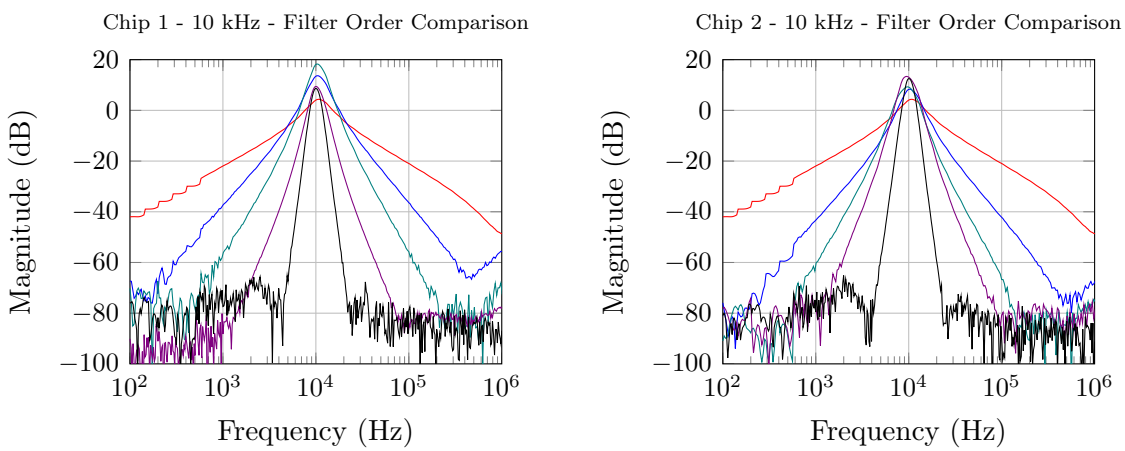

Figure 31: —— 2nd order, —— 4th order, —— 6th order, —— 8th order, and —— 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 10$ kHz.

Although still present, the high-frequency peaking in the 2nd order waveform is still present, but it occurs beyond 1 MHz, and thus is out of the plot range. Comparatively, the 4th order spectral response of Chip 1 exhibited worse high-frequency peaking than Chip 2, resulting in a degraded dynamic range at high frequency.

4.4.3 $f_c = 50$ kHz

At $f_c = 50$ kHz, the filter spectral response order comparison for Chip 1 and Chip 2, seen below in Fig. 32 illustrates good symmetry between the waveforms. For both Chip 1 and Chip 2, the measurement baseline tends to be more consistent for all intermediary filter orders when compared to the data at lower center frequencies presented earlier in this work.

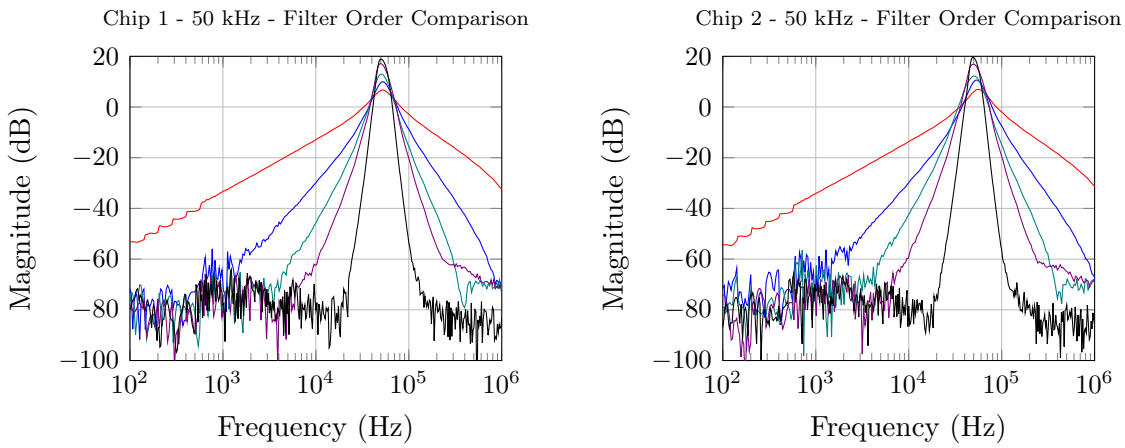

Figure 32: —— 2nd order, —— 4th order, —— 6th order, —— 8th order, and —— 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 50$ kHz.

Seen in both Chip 1 and Chip 2, the spectral response of the 8th order filter stage exhibits the same gradual return to measurement baseline observed earlier in Section 4.3.3. However, in this instance, such behavior on the high-side filter corner is not present in the 6th order spectral response. As concluded earlier, this can be improved by reducing the filter gain.

4.4.4 $f_c = 100$ kHz

The Chip 1 and Chip 2 filter order comparison at $f_c = 100$ kHz, seen below in Fig. 33, demonstrates a high degree of symmetry in addition to a consistent measurement baseline, which results in a more reliable dynamic range measurement. Similar to the filter spectral response order comparison at $f_c = 50$ kHz, the 6th order filter stage is free of any high-frequency measurement baseline degradation, whereas the 8th order filter stage exhibits such.

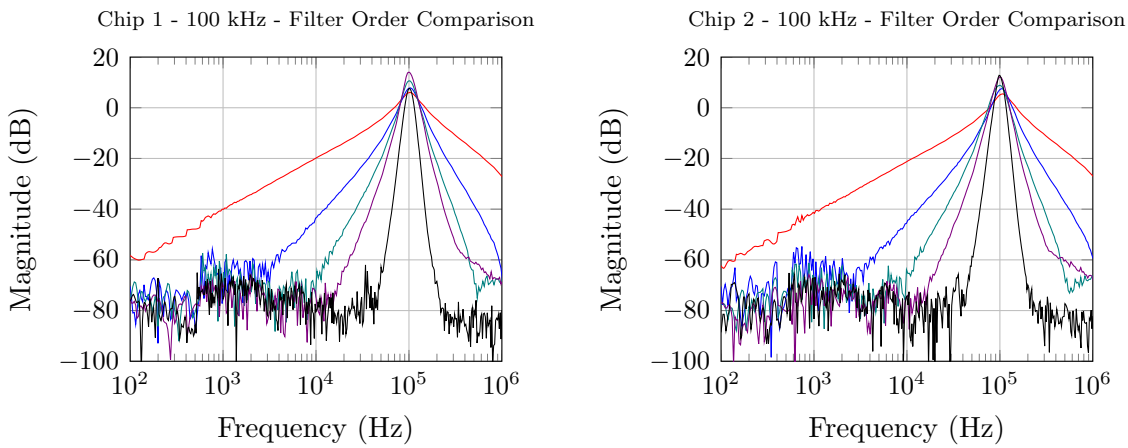

Figure 33: —— 2nd order, —— 4th order, —— 6th order, —— 8th order, and —— 16th order filter spectral responses of Chip 1 (left) and Chip 2 (right) under Measured Corrected Bias conditions for $f_c = 100$ kHz.

4.5 Variable Filter Gain

In addition to offering a tunable range of operational frequencies, the MISA filter channel provides the ability to adjust filter gain as well. This functionality is demonstrated below in Fig. 34, which illustrates a MISA filter channel spectral

response overlay at $f_c = 10$ kHz of filter gain settings from 0 dB to 12 dB, incremented in 3 dB step sizes. Although higher filter gain settings of 20 dB have been measured, the %THD (discussed in the following section) improves dramatically as filter gain is reduced.

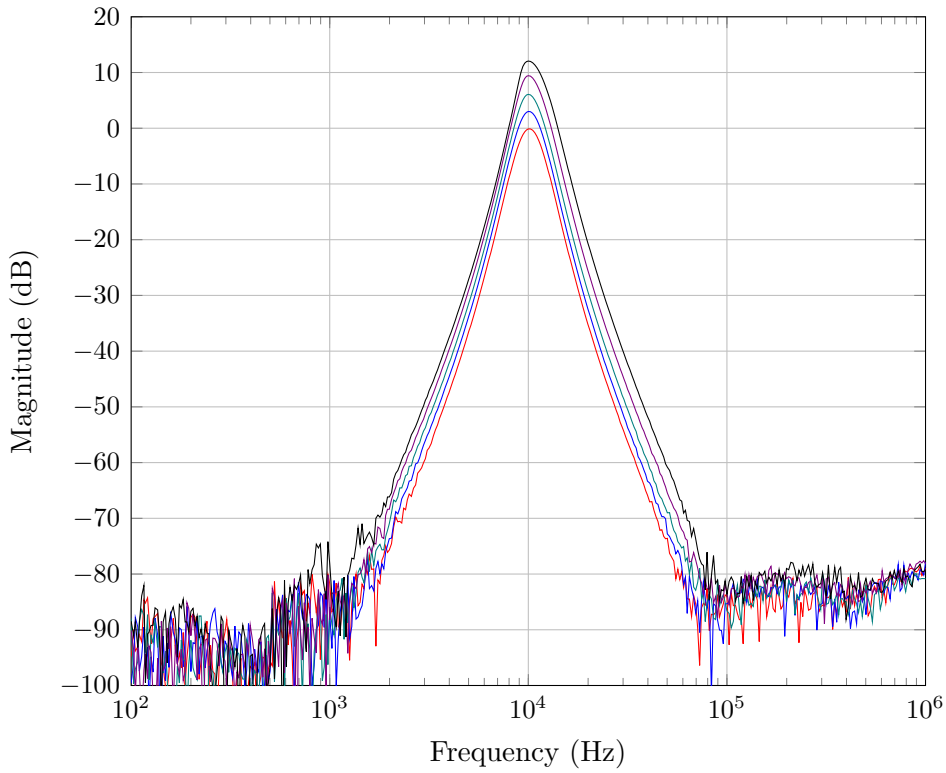

Figure 34: Variable filter gain spectral response of Chip 1 - Ch. 1 demonstrating the ability to bias the MISA filter channel for varying amounts of filter gain. —— 0 dB, —— 3 dB, —— 6 dB, —— 9 dB, and —— 12 dB filter gain settings are demonstrated above for $f_c = 10$ kHz.

Additionally, $Q_{effective}$ is more consistent at lower gain settings, resulting in a characteristic filter shape that is more symmetric around the center frequency in general.

4.6 Total Harmonic Distortion

Total Harmonic Distortion (THD) provides a meaningful comparison of the undesired harmonic content of a signal to the desired fundamental signal content [15]. Calculated as a percentage of signal amplitude, %THD is the ratio of the sum of all harmonic signal power to the power of signal's fundamental frequency. The same HP 3589A Spectrum/Network Analyzer used to obtain filter spectral response data was also used to measure THD. The following equations, which detail how to calculate THD, were provided in the HP 3589A Operator's Guide [16].

$$10^{h/10} = v \tag{4.1}$$

$$v_1 + v_2 + ...v_n = s \tag{4.2}$$

$$10 \cdot log\,(s) = d \tag{4.3}$$

$$\%THD = 100 \cdot 10^{d/20} \tag{4.4}$$

Each of the measurements presented were obtained with a 70 $mV_{p\text{-}p}$ sine wave input stimulus, with the MISA filter biased to provide unity gain. THD measurements at two center frequencies, set one decade apart at f_c = 10 kHz and 100 kHz, are presented in the sections below. The resolution bandwidth of the HP3589A was set to 150 Hz, and an average of 10 scans was acquired for each measurement. Similar to the presentation format of preceding sections, data from Chip 1 will be shown on the left, with data from Chip 2 on the right.

4.6.1 $f_c = 10$ kHz

The %THD performance of Chip 1 and Chip 2 at $f_c = 10$ kHz is shown below in Fig. 35. Two harmonics of the fundamental frequency were consistently observed at 20 kHz and 30 kHz, respectively. The third harmonic at 40 kHz was not visible in each measurement due to the noise floor of the test equipment. The %THD of Chip 1 at $f_c = 10$ kHz was calculated to be approximately 0.578% for Ch. 1 and 0.598% for Ch. 2.

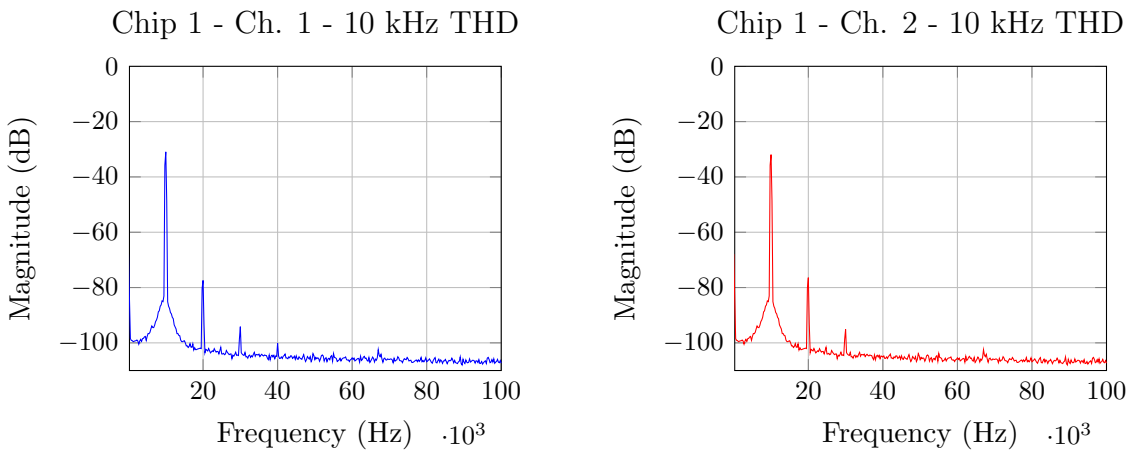

Figure 35: Total harmonic distortion measurement of Chip 1 —— Ch. 1 (left) and —— Ch. 2 (right) under Corrected Bias conditions for $f_c = 10$ kHz.

For Chip 2, seen in Fig. 36 below, the %THD was calculated to be 0.506% for Ch. 1 and 0.667% for Ch. 2. In Chip 2, the second harmonic at 20 kHz is nearly 10 dB stronger in magnitude than observed in Chip 1.

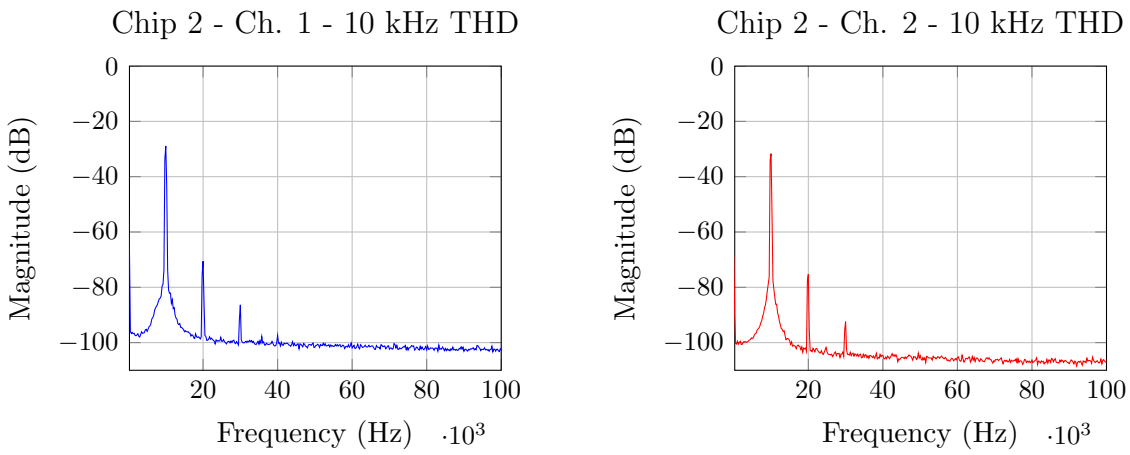

Figure 36: Total harmonic distortion measurement of Chip 2 —— Ch. 1 (left) and —— Ch. 2 (right) under Corrected Bias conditions for $f_c = 10$ kHz.

4.6.2 $f_c = 100$ kHz

In Fig. 37 below, the measured THD for Chip 1, Ch. 1 and Ch. 2 is illustrated. The first and second harmonics of the fundamental at 200 kHz and 300 kHz, respectively, were observed in both channels of Chip 1. The THD was calculated to be approximately %0.583 for Ch. 1, and 0.541% for Ch. 2. The third harmonic at 400 kHz was not observed in either measurement due to the noise floor of the test equipment. The THD for Chip 2, Ch. 1 and Ch. 2, is seen below in Fig. 38. In Ch. 1, the second harmonic was not observed, despite utilizing the same test equipment setup for each measurement. The THD of Chip 2 was calculated to be approximately 0.401% in Ch. 1 and 0.30% in Ch. 2.

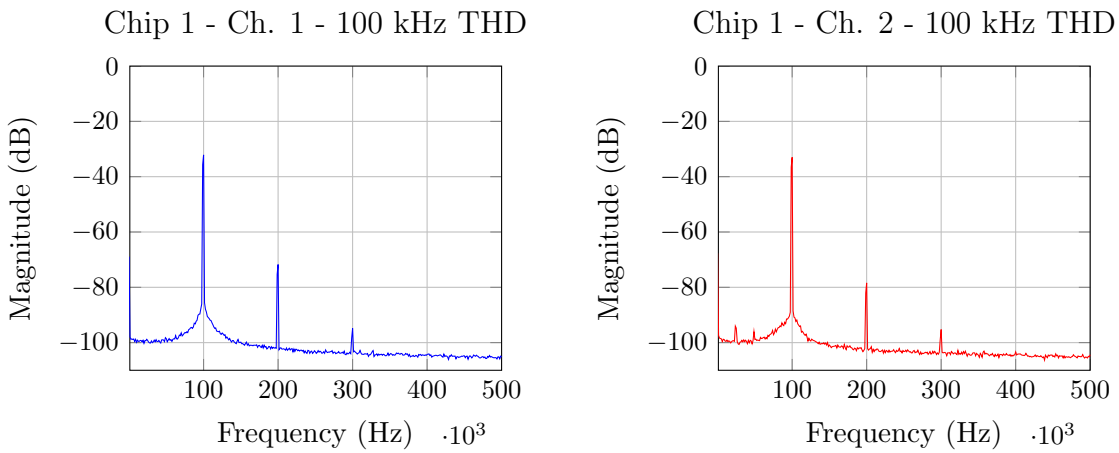

Figure 37: Total harmonic distortion measurement of Chip 1 —— Ch. 1 (left) and —— Ch. 2 (right) under Corrected Bias conditions for $f_c = 100$ kHz.

The %THD measured in Ch. 2 of Chip 2 was lower than that of Ch. 1, despite the presence of the second harmonic. This is due to the comparative strength of the fundamental frequency.

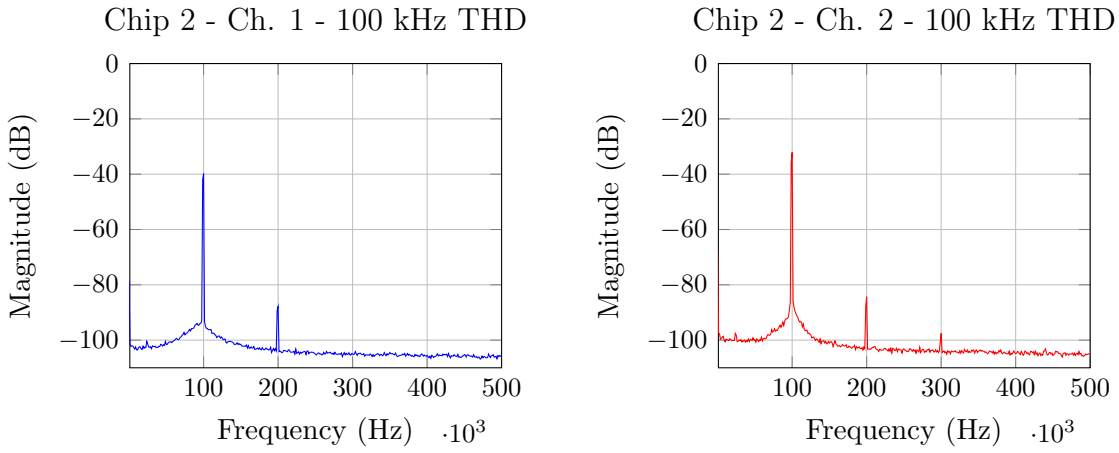

Figure 38: Total harmonic distortion measurement of Chip 2 —— Ch. 1 (left) and —— Ch. 2 (right) under Corrected Bias conditions for $f_c = 100$ kHz.

4.7 Filter Performance Summary

Key performance metrics from the MISA filter channel measurements are presented below in Table 3. Organized by filter center frequency, the measured $Q_{effective}$, %THD, dynamic range, and power consumption are provided. As reported in Sec. 1.1, the MISA filter channel exhibits a high dynamic range, especially considering the low power consumption. Throughout the required spectrum of operational frequencies, the measured dynamic range proved to be the most consistent figure of merit, increasing only slightly with filter center frequency. Although the highest-achieved $Q_{effective}$ was not obtainable across the entire range of operational frequencies, only low-frequency performance was hindered in this regard.

Table 3: MISA Filter Channel Performance Summary

f_c	$Q_{effective}$	%THD	DR	Power
2 kHz	3.2 - 3.4	0.973% - 1.250%	85 dB	78 μW
10 kHz	3.7 - 4.3	0.506% - 0.667%	92 dB	90 μW
50 kHz	4.7 - 5.0	0.20% - 0.3%	96 dB	155 μW
100 kHz	4.8 - 5.2	0.30% - 0.55%	96 dB	256 μW

Similar to the performance trend observed with $Q_{effective}$, the measured %THD improved as center frequency increased, exhibiting the worst performance at the lowest filter center frequency of interest. However, power consumption scaled accordingly with the increase in filter center frequency - an issue that may only be

addressed in any future work. Overall, with the exception of low-frequency %THD and $Q_{effective}$ performance, the measured MISA filter channel performance metrics match very well with the pre-fabrication simulation results.

5 Conclusion

5.1 Thesis Summary

In conclusion, the design and implementation of a monolithic integrated tunable analog 8th order bandpass filter channel in a commercially available 130-nm 1.2 V CMOS process was presented in this work in conjunction with measurement data from the fabricated design. With respect to the original project design requirements, this work accomplishes the design task of implementing a low-power, tunable analog bandpass filter channel with a high effective Q and an operational frequency spectrum from 2-100 kHz. The foundational design of the OTA-C^4 proved to be a robust filter topology upon which to implement the MISA filter channel, with key performance improvements contributed by this work in regards to dynamic range, right-half-plane zero cancellation for increased filter stability, power consumption, and investigation of a higher order filter topology (up to 16th order).

The device models of the 130-nm 1.2 V CMOS process proved to be accurate, with obtainable filter gain remaining as the primary discrepancy between simulated and measured results. The most pronounced short-coming of the 8th order MISA filter channel is the degraded $Q_{effective}$ when measuring filter spectral responses at the lowest end of the specified operational frequency spectrum. Although the Minch current bias cell performs well in terms of output current matching across a wide range of input bias currents, the lowest input bias currents resulted in a bias stability degradation at low frequency, as the output devices of the current bias cell began to stop operating sufficiently far enough into saturation. This design issue may be

readily improved in any future designs by resizing the devices of the Minch current mirror in order to ensure device saturation at lower input bias currents.

5.2 Recommendations for Future Work

Future design revisions of this integrated bandpass filter channel design would benefit from modifications to the filter current bias structure, as well as the size and range of capacitor values. Concerning the Minch current bias structure, the device sizing was set such that the channel length was approximately 2× the minimum device feature size. An increase in the channel length to 4× the minimum device feature size would provide a more conservative design, and strengthen device matching over process variation. Monte Carlo analysis would be required to justify any resulting matching improvements gained from increasing the device channel length, as the devices may be subject to undesired fluctuations in threshold voltage due to the utilization of halo implants in the channels of the devices in the implemented 130-nm 1.2 V CMOS process [17]. In order to continue the use of the filter topology presented yet improve the Q-factor of each individual 2nd order stage, the capacitor C_W was determined to be the most efficacious variable to adjust. However, a design trade-off must be made, as increasing C_W increases the spread of on-chip capacitor sizes, which could correspondingly decrease matching between filter channels both locally on the same chip, as well as between individual chips if appropriate consideration is not given during layout. To counter this risk, the inclusion of "dummy" unit capacitors around the perimeter of the common-centroid capacitor array would minimize the effects of any deviations in device boundary conditions, as edge-device

boundary conditions differ from those of inner elements [18].

Lastly, further design efforts would allow for the remaining functionality, such as automated control of filter bias currents and digital back-end signal processing, of a monolithic integrated spectrum analyzer to be obtained, with the MISA filter channel providing the fundamental core functionality required by such an application.

References

[1] B. Rumberg and D. W. Graham, "A low-power and high precision programmable analog filter bank," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 59, no. 4, pp. 234–238, April 2012.

[2] B. Murmann. ADC performance survey 1997-2016. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[3] B. Razavi, "Introduction to A/D conversion," 2012. [Online]. Available: http://www.seas.ucla.edu/brweb/teaching/215D_S2012/ADC1.pdf

[4] A. Katsiamis, E. Drakakis, and R. Lyon, "A biomimetric, 4.5 μw, 120+db, log-domain cochlea channel with AGC," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3, pp. 1006–1022, March 2009.

[5] J. Georgiou and C. Toumazou, "A 126- μw cochlear chip for a totally implantable system," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 430–443, February 2005.

[6] J. C. Daly and D. P. Galipeau, *Analog BiCMOS Design: Practices and Pitfalls*, 1st ed. CRC Press, 2000.

[7] Y. Papananos, T. Georgantas, and Y. Tsividis, "Design considerations and implementation of very low frequency continuous-time CMOS monolithic filters," ser. IEE Proceedings - Circuits, Devices and Systems, vol. 144, no. 2, April 1997, pp. 68–74.

[8] P. M. Furth and H. A. Ommani, "Low-voltage highly-linear transconductor design in sub-threshold CMOS," ser. Proceedings of the IEEE Midwest Symposium on Circuits and Systems, Sacramento, CA, vol. 1, August 1997, pp. 156–159.

[9] R. Sarpeshkar, R. F. Lyon, and C. Mead, "A low-power wide-linear-range transconductance amplifier," *Analog Integrated Circuits and Signal Processing*, vol. 13, no. 1/2, pp. 123–151, May/June 1997.

[10] D. M. Binkley, B. J. Blalock, and J. M. Rochelle, "Optimizing drain current, inversion level, and channel length in analog cmos design," *Analog Integrated Circuits and Signal Processing*, vol. 47, no. 2, pp. 137–163, May 2006.

[11] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. McGraw-Hill Education, 2000.

[12] E. J. Kennedy, *Operational Amplifier Circuits: Theory and Applications*, 1st ed. Holt, Reinhart and Winston, Inc., 1988.

[13] B. A. Minch, "A low-voltage MOS cascode current mirror for all current levels," *IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 619–622, August 2002.

[14] A. M. Niknejad, "Lecture 9: Intercept point, gain compression and blocking - RFIC," 2005. [Online]. Available: http://rfic.eecs.berkeley.edu/~niknejad/ee142_fa05lects/pdf/lect9.pdf

[15] R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*, 4th ed. McGraw-Hill Education, 2011.

[16] *HP 3589A Operator's Guide*, Hewlett-Packard Company, August 1991.

[17] R. Wittmann, "Miniaturization problems in CMOS technology: Investigation of doping profiles and reliability," Ph.D. dissertation, Technischen Universität Wien, January 2007.

[18] F. Maloberti, "Layout of analog CMOS integrated circuits - part 2: Transistors and basic cell layout," 2016. [Online]. Available: http://ims.unipv.it/Courses/download/AIC/Layout02.pdf

Appendices

A OTA-C^4 Transfer Function Derivation

The output transfer function of the OTA-C^4 from symbolic SPICE is provided below in Eq. A.1 [1].

$$\frac{V_{out}}{V_{in}} = \frac{s^2\left(C_2C_1\right) - s\left(C_1G_{m,H}\right)}{s^2\left(C_WC_L + C_WC_2 + C_LC_2 + C_LC_1 + C_2C_1\right) + s\left(C_LG_{m,L} + C_2G_{m,H}\right) + G_{m,L}G_{m,H}} \tag{A.1}$$

Dividing out and distributing the product $G_{m,L}G_{m,H}$ from the denominator, in addition to collecting the terms C_2 and C_L from the 2nd order denominator term, yields Eq. A.2. Note that an additional term, C_2^2, must be included so that it may be subtracted from the 2nd order denominator in order to cancel the same term created by collecting C_2.

$$\frac{V_{out}}{V_{in}} = \frac{s^2\left(\frac{C_2C_1}{G_{m,L}G_{m,H}}\right) - s\left(\frac{C_1G_{m,H}}{G_{m,L}G_{m,H}}\right)}{s^2\left(\frac{C_2(C_1+C_2+C_W)+C_L(C_1+C_2+C_W)-C_2^2}{G_{m,L}G_{m,H}}\right) + s\left(\frac{C_LG_{m,L}}{G_{m,L}G_{m,H}} + \frac{C_2G_{m,H}}{G_{m,L}G_{m,H}}\right) + 1} \tag{A.2}$$

Bringing the term $1/G_{m,L}$ out of the 2nd order denominator and canceling like terms in the 1st order numerator and denominator results in Eq. A.3.

$$\frac{V_{out}}{V_{in}} = \frac{s^2\left(\frac{C_2C_1}{G_{m,L}G_{m,H}}\right) - s\left(\frac{C_1}{G_{m,L}}\right)}{s^2\left(\frac{1}{G_{m,L}}\right)\left(\frac{C_2(C_1+C_2+C_W)+C_L(C_1+C_2+C_W)-C_2^2}{G_{m,H}}\right) + s\left(\frac{C_L}{G_{m,H}} + \frac{C_2}{G_{m,L}}\right) + 1} \tag{A.3}$$

C_1 is collected from the 1st and 2nd order terms in the numerator and rearranged such that it functions as a constant. In the 1st order term of the denominator, an extra

term, $C_2/G_{m,H}$ is included so that it may be subtracted from the existing $C_2/G_{m,H}$ term, which is modified to be $C_L C_2 + {C_2}^2/C_2 G_{m,H}$. This modified term allows for the cancellation of the included $C_2/G_{m,H}$ term. The result of this expansion, which allows for later substitution, is seen in Eq. A.4 below.

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{1} \cdot \frac{s^2\left(\frac{C_2}{G_{m,L}G_{m,H}}\right) - s\left(\frac{1}{G_{m,L}}\right)}{s^2\left(\frac{C_2}{G_{m,L}}\right)\left(\frac{(C_2+C_L)(C_1+C_2+C_W)-C_2^2}{C_2 G_{m,H}}\right) + s\left(\frac{C_2}{G_{m,L}} + \left(\frac{C_L C_2 + C_2^2}{C_2 G_{m,H}} - \frac{C_2}{G_{m,H}}\right)\right) + 1} \tag{A.4}$$

The 1st and 2nd order terms of the numerator are then rearranged, resulting in the distribution of the minus sign to the constant C_1 in order to maintain the correct polarity of the expression as a whole. Additionally, the expression is multiplied by the term $1/C_2$, which is also collected with the term C_1 outside of the expression, such that the variable C_2 can be included in the 1st order numerator term and the existing C_2 in the 2nd order numerator term can be squared. In the denominator, Eq.'s 3.5 and 3.4 are substituted into the 2nd order term where appropriate. In the 1st order denominator term, the term $C_2/G_{m,H}$ is collected from the term expanded in Eq. A.4 above. The result of these operations are Eq. A.5.

$$\frac{V_{out}}{V_{in}} = \frac{-C_1}{C_2} \cdot \frac{s\left(\frac{C_2}{G_{m,L}}\right) - s^2\left(\frac{C_2^2}{G_{m,L}G_{m,H}}\right)}{s^2\left(\frac{C_2}{G_{m,L}}\right)\left(\frac{C_O C_T - C_2^2}{C_2 G_{m,H}}\right) + s\left(\frac{C_2}{G_{m,L}} + \frac{C_2}{G_{m,H}}\left(\frac{C_L+C_2}{C_2} - 1\right)\right) + 1} \tag{A.5}$$

In the 1st order denominator term of Eq. A.5, Eq. 3.5 is substituted in where appropriate. The result is seen below in Eq. A.6.

$$\frac{V_{out}}{V_{in}} = \frac{-C_1}{C_2} \cdot \frac{s\left(\frac{C_2}{G_{m,L}}\right) - s^2\left(\frac{C_2^2}{G_{m,L}G_{m,H}}\right)}{s^2\left(\frac{C_2}{G_{m,L}}\right)\left(\frac{C_O C_T - C_2^2}{C_2 G_{m,H}}\right) + s\left(\frac{C_2}{G_{m,L}} + \frac{C_2}{G_{m,H}}\left(\frac{C_O}{C_2} - 1\right)\right) + 1} \tag{A.6}$$

The 1st and 2nd order terms of both the numerator and denominator in Eq. A.6 are equivalent to a time-constant expression. In the numerator, Eq. 3.6 is substituted into the 1st and 2nd order terms, and Eq. 3.8 is substituted into the 2nd order term. In the denominator, Eq.'s 3.6 and 3.7 are substituted into the 2nd order term, and Eq.'s 3.6 and 3.8 are substituted into the 1st order term where appropriate. With these substitutions, the transfer function below matches Eq. 3.1, the reported 2nd order bandpass transfer function of the OTA-C^4 [1].

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} \cdot \frac{s\tau_l(1 - s\tau_f)}{1 + s(\tau_l + \tau_f(\frac{C_O}{C_2} - 1)) + s^2\tau_h\tau_l} \tag{A.7}$$

B Supplementary Measurement Data: Chips 3-5

B.1 2 kHz

B.1.1 Chip 3: Ch. 1 and Ch. 2

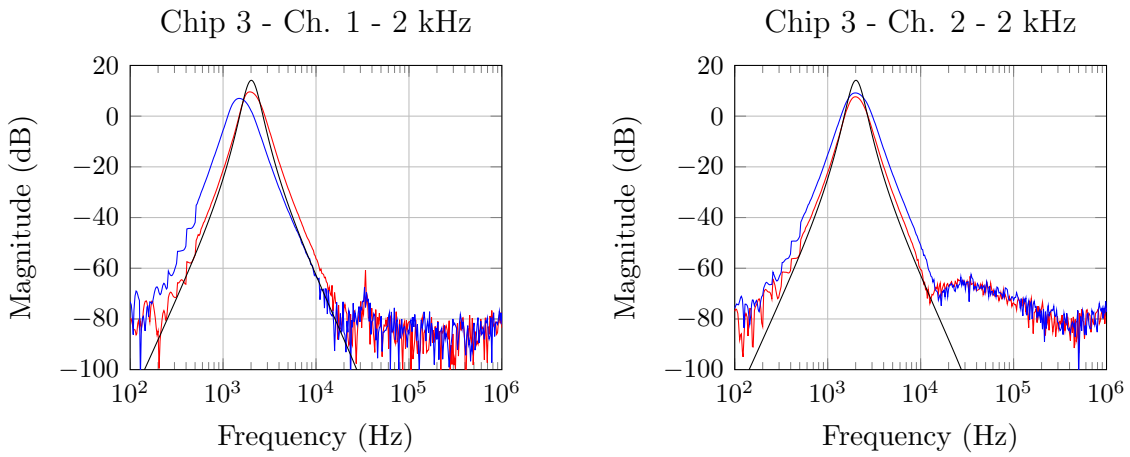

Figure 39: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.1.2 Chip 4: Ch. 1 and Ch. 2

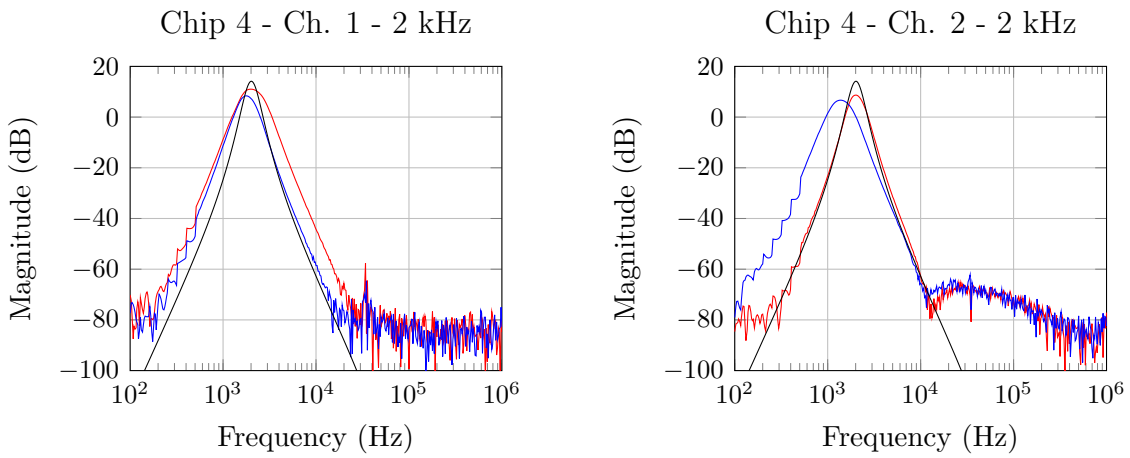

Figure 40: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.1.3 Chip 5: Ch. 1 and Ch. 2

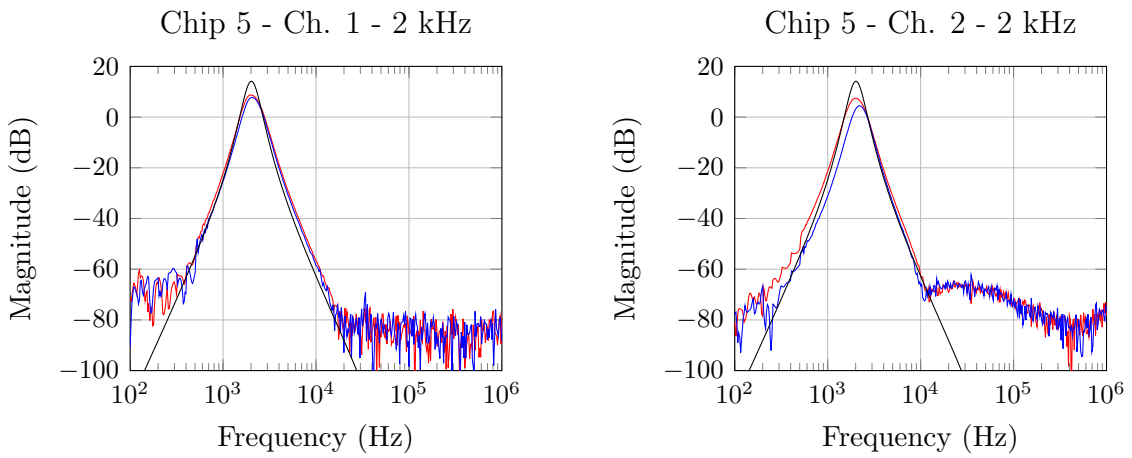

Figure 41: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.2 10 kHz

B.2.1 Chip 3: Ch. 1 and Ch. 2

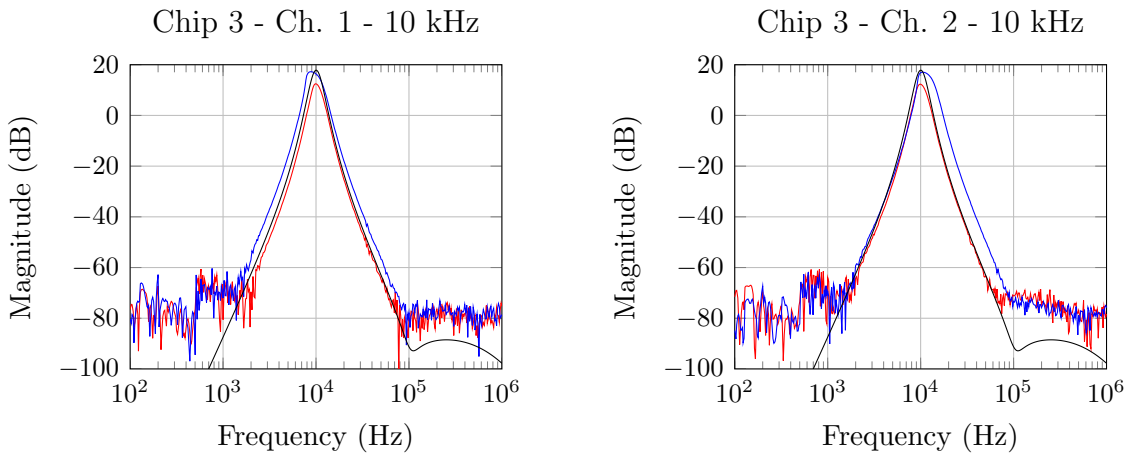

Figure 42: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.2.2 Chip 4: Ch. 1 and Ch. 2

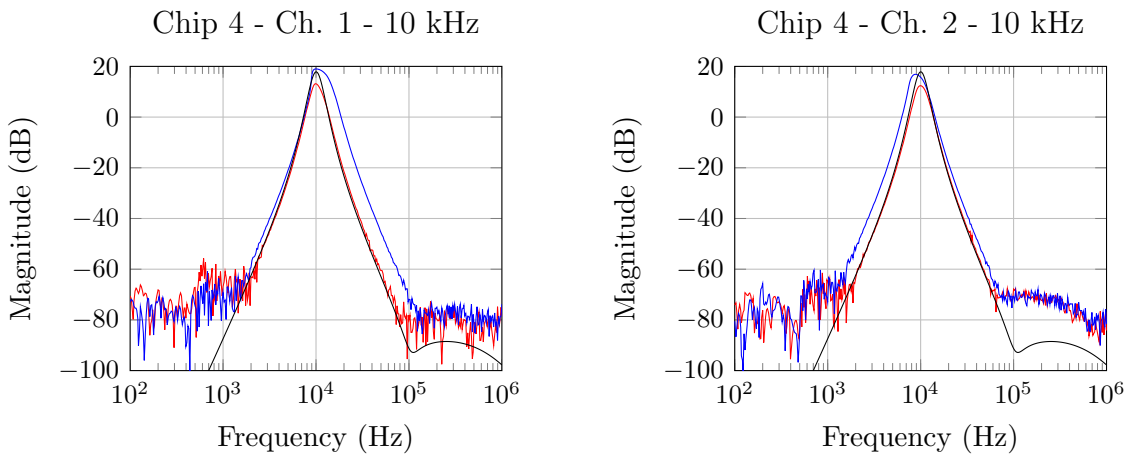

Figure 43: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.2.3 Chip 5: Ch. 1 and Ch. 2

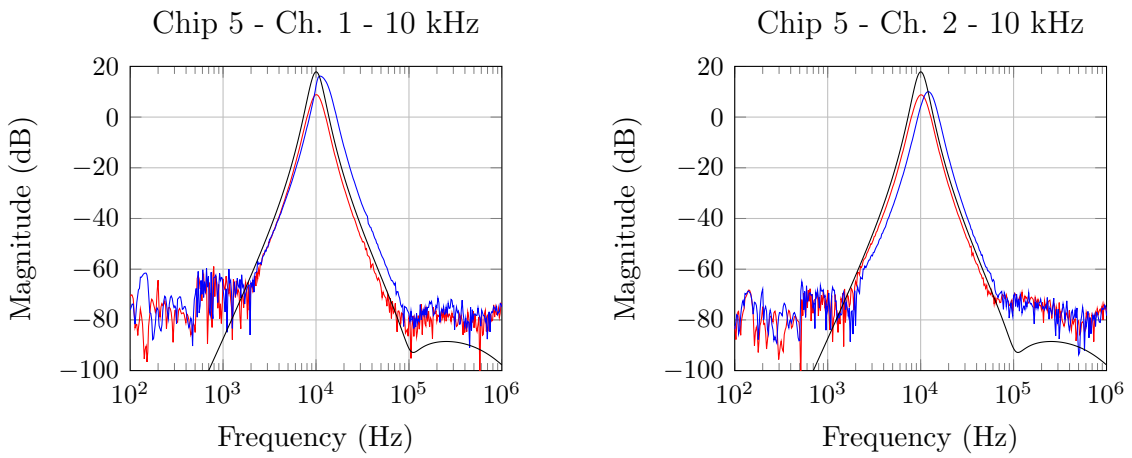

Figure 44: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.3 50 kHz

B.3.1 Chip 3: Ch. 1 and Ch. 2

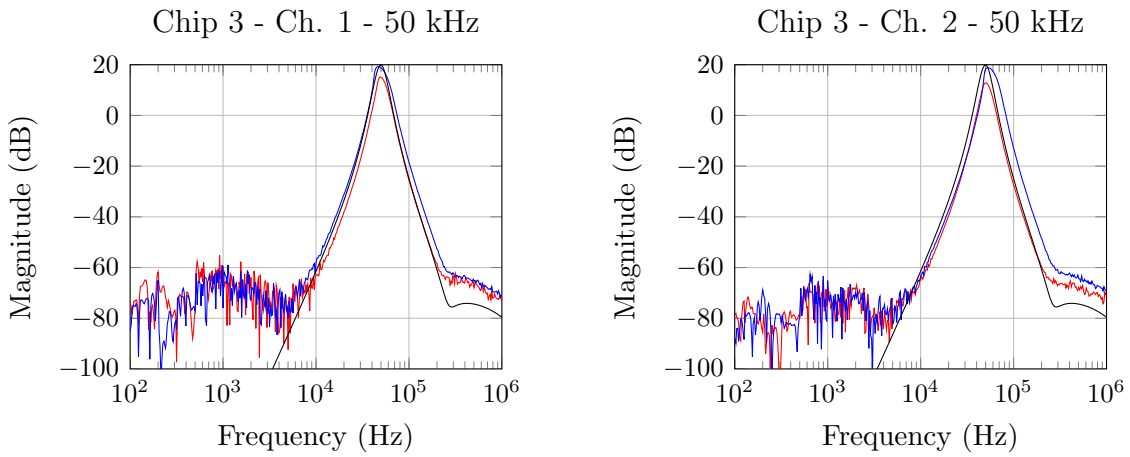

Figure 45: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.3.2 Chip 4: Ch. 1 and Ch. 2

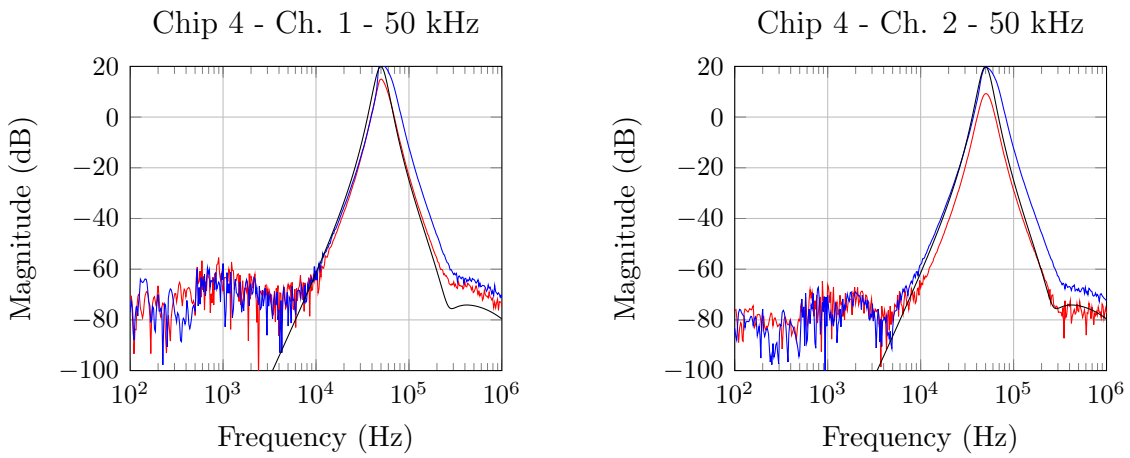

Figure 46: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.3.3 Chip 5: Ch. 1 and Ch. 2

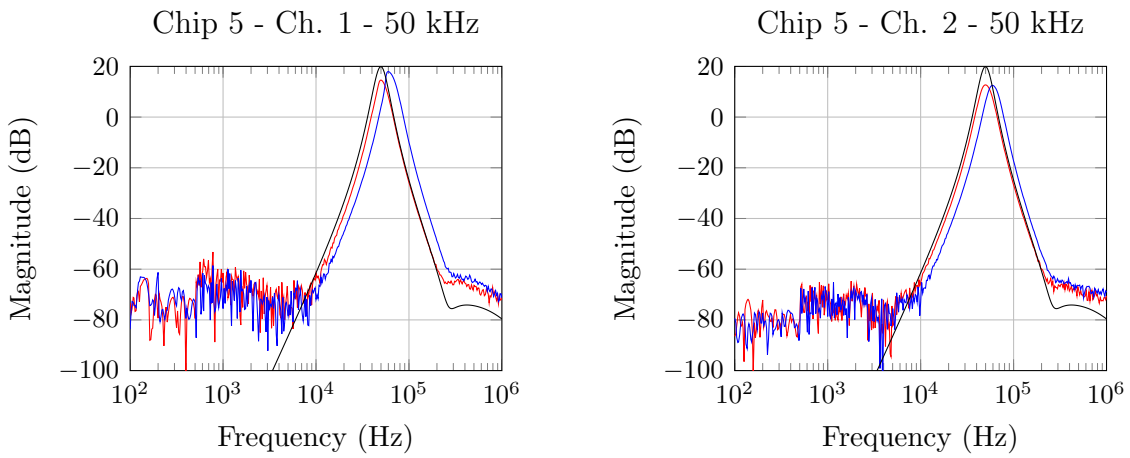

Figure 47: Filter spectral response of Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias and —— Measured Theoretical Bias, and —— Simulated Theoretical Bias.

B.4 100 kHz

B.4.1 Chip 3: Ch. 1 and Ch. 2

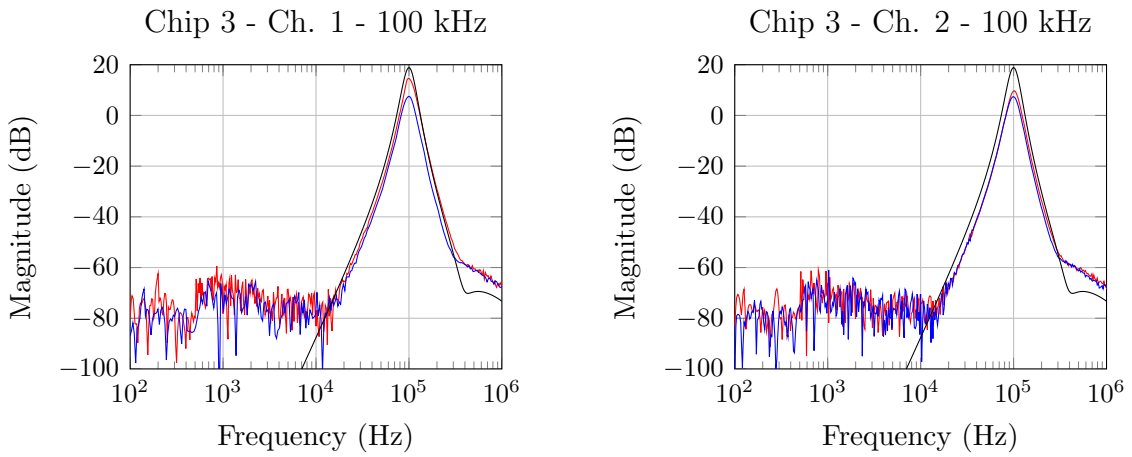

Figure 48: Filter spectral response of Chip 3 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz.

B.4.2 Chip 4: Ch. 1 and Ch. 2

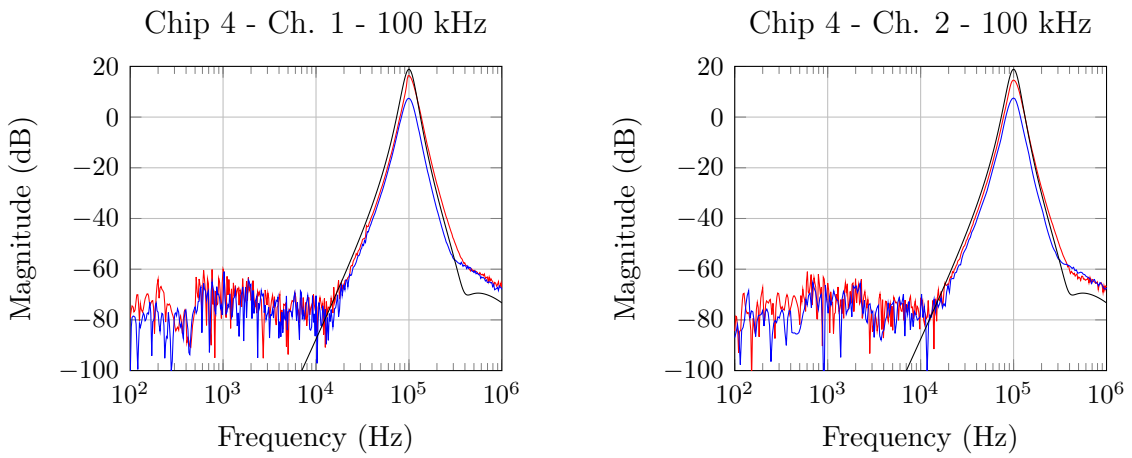

Figure 49: Filter spectral response of Chip 4 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz.

B.4.3 Chip 5: Ch. 1 and Ch. 2

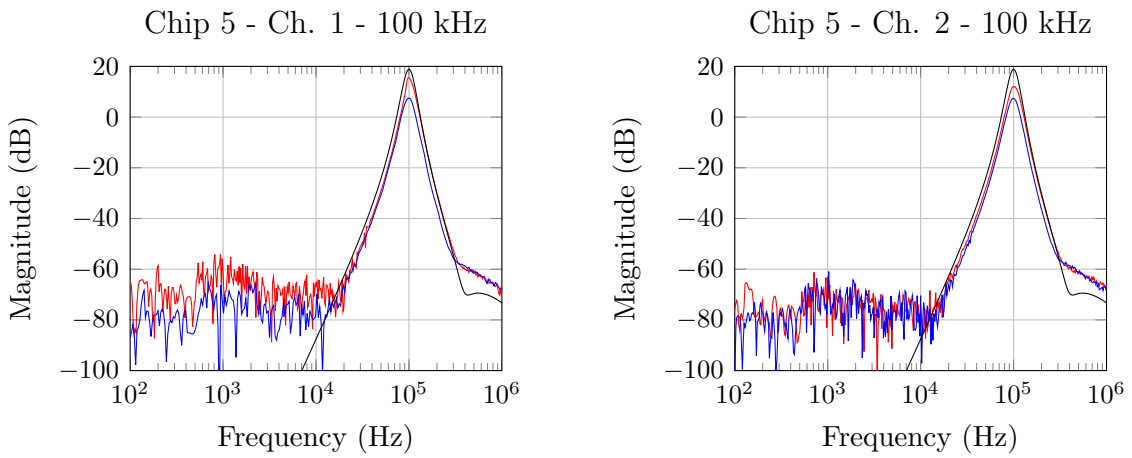

Figure 50: Filter spectral response of Chip 5 - Ch. 1 (left) and Ch. 2 (right) with —— Measured Corrected Bias, —— Measured Theoretical Bias, and —— Simulated Theoretical Bias conditions for $f_c = 100$ kHz.

Vita

Benjamin David Roehrs (Ben) was born in Memphis, TN on October 12th, 1989. He attended Houston High School in Germantown, TN, where he graduated in 2008, having been awarded the Min H. Kao Scholarship for Electrical & Computer Engineering at the University of Tennessee, Knoxville. During his undergraduate studies, he interned with Clinton Utility Board, BMW Manufacturing Co. LLC, and BMW M GmbH in Munich, DE before deciding to continue his education in electrical engineering by pursuing a graduate degree. Before beginning graduate studies, he spent a semester working in the Electronics R & D department at Siemens Medical Solutions in Knoxville, TN.

During his first semester of graduate coursework in the Spring semesters of 2015, he held the position of graduate teaching assistant and research assistant to Dr. Benjamin Blalock in the Integrated Circuits and Systems Laboratory at UTK. Within this group, Ben was offered the opportunity to work under Dr. Nance Ericson and Dr. Charles Britton at Oak Ridge National Laboratory while fulfilling the research requirements for his master's degree.