Energy-efficient and Power-dense DC-DC Converters in Data Center and Electric Vehicle Applications Using Wide Bandgap Devices

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Abstract

The ever increasing demands in the energy conversion market propel power converters towards high efficiency and high power density. With fast development of data processing capability in the data center, the server will include more processors, memories, chipsets and hard drives than ever, which requires more efficient and compact power converters. Meanwhile, the energy-efficient and power-dense converters for the electric vehicle also result in longer driving range as well as more passengers and cargo capacities. DC-DC converters are indispensable power stages for both applications. In order to address the efficiency and density requirements of the DC-DC converters in these applications, several related research topics are discussed in this dissertation.

For the DC-DC converter in the data center application, a LLC resonant converter based on the newly emerged GaN devices is developed to improve the efficiency over the traditional Si-based converter. The relationship between the critical device parameters and converter loss is established. A new perspective of extra winding loss due to the asymmetrical primary and secondary side current in LLC resonant converter is proposed. The extra winding loss is related to the critical device parameters as well. The GaN device benefits on device loss and transformer winding loss is analyzed. An improved LLC resonant converter design method considering the device loss and transformer winding loss is proposed.

For the DC-DC converter in the electric vehicle application, an integrated DC-DC converter that combines the on-board charger DC-DC converter and drivetrain DC-DC converter is developed. The integrated DC-DC converter is considered to operate in different modes. The existing dual active bridge (DAB) DC-DC converter originally designed for the charger is proposed to operate in the drivetrain mode to improve the efficiency at the light load and high

voltage step-up ratio conditions of the traditional drivetrain DC-DC converter. Design method and loss model are proposed for the integrated converter in the drivetrain mode. A scaled-down integrated DC-DC converter prototype is developed to verify the design and loss model.

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1 Introduction

This chapter starts with the background of data center power converters. The DC-DC intermediate bus converter (IBC) in the high voltage power architecture for the data center is exhibited. The topology candidates of IBC are compared after that, and the LLC resonant converter shows the advantages. Then, the opportunities and challenges of LLC resonant converter are discussed. In the EV application, the future requirements of efficiency and power density are demonstrated. Followed by that, the limitations of state of the art power conversion architecture in EV is explained. The research objectives and approaches are summarized in the end of each part. The dissertation organization is presented at last.

1.1 DC-DC Converters in Data Center Application

1.1.1 Background

In 2010, about 67 TWh electricity, or 2.2% of all generated electricity, was consumed by data centers in the United States; this equates to about $3.3 billion in electricity bills [1] [2]. The power required to support the computing infrastructure in large data centers can reach up to several tens of MW [3], but the power efficiency is very low. Figure 1-1 shows an example of power flow in a data center. Nearly half of the power is lost in the power delivery path, resulting in the end-to-end efficiency below 50% [4]. The main reasons are that there are many cascaded power conversion stages, and the efficiency of each power stage is low. Because all the power dissipation results in heat, additional power is needed to operate the cooling system to remove the heat, which further reduces the system efficiency.

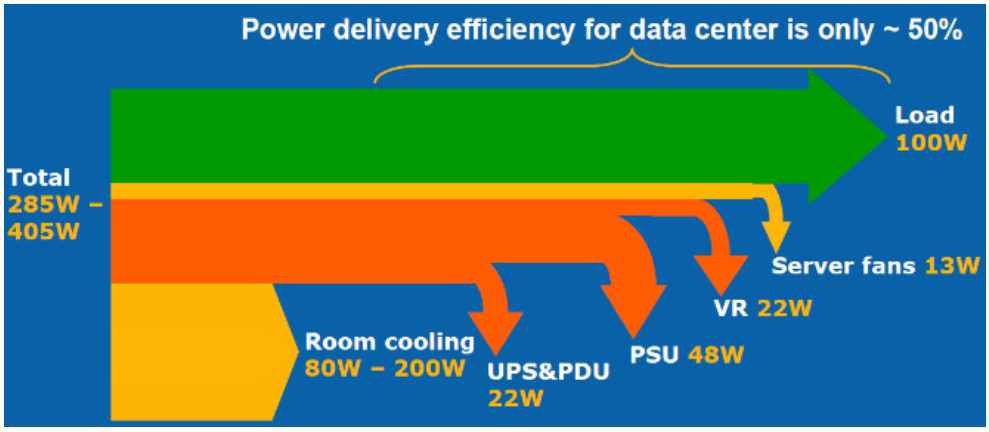


Figure 1-1. Power flow in the server.

Since the early 90's, governmental agencies started establishing regulations to encourage the energy efficiency, such as U.S. Energy Star [5], Climate Savers [6], and 80 PLUS [7]. The 80 PLUS program, shown in Figure 1-2, is a typical program that provides tiers of efficiency requirements for the AC-DC Power Supply Unit (PSU) shown in Figure 1-3. The minimum Bronze 80 PLUS specification requires power supplies in computers or servers to be 80% or greater at 10, 20, 50 and 100% of load. The latest efficiency requirement is the TITANIUM program released in 2012. It provides the highest efficiency requirement for the PSUs. When the input AC voltage is in the 230 V range from the grid, the efficiencies are required to achieve 91% at full load and 96% at peak load. Currently, the efficiencies are updated by some new industry products tested by the 80 PLUS program [9] [10], therefore the highest-performing industry benchmarks are already beyond TITANIUM.

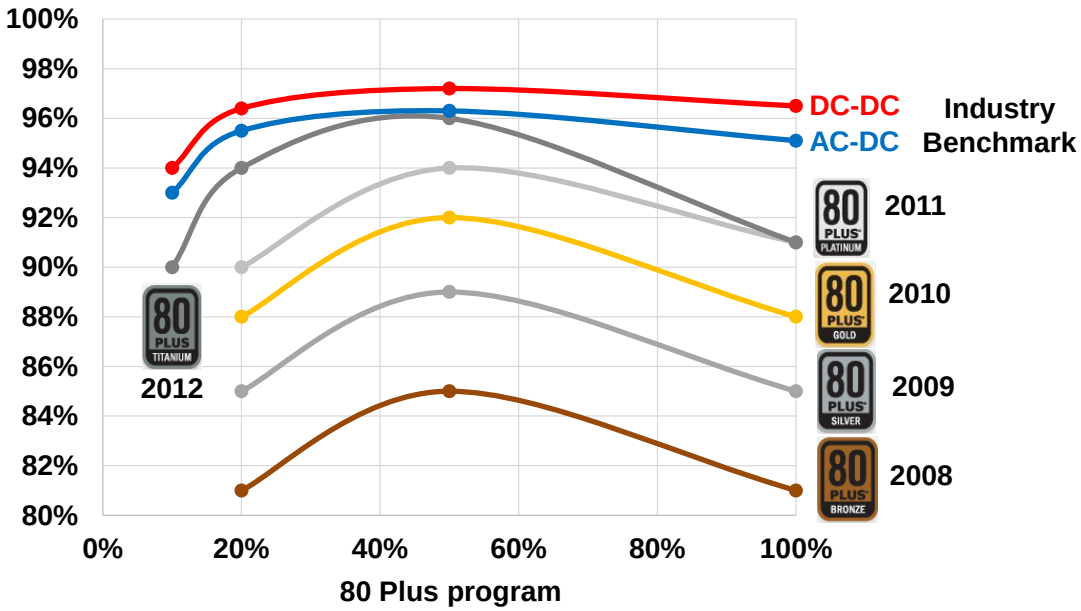


Figure 1-2. 80 PLUS program efficiency and the industry current benchmark [7].

Figure 1-3. AC-DC Power Supply Unit (PSU).

The power density requirements for PSUs are also increasing in recent years. Due to the growing demand of the computing system capacity and performance, the power consumption of each server unit is getting higher, but the space for the PSUs is limited. Figure 1-4 shows a typical server. Spaces I and II are designed for the PSUs. Usually the height of the PSUs is determined by the server height, such as 1U (1.75 inches) or 2 U (3.5 inches), but the length and width are determined by the PSUs size requirement. As is shown in Figure 1-4, the two PSUs account for

nearly one third of the total space of the server. If the PSU size could be reduced, there would be more space for memory or hard drives, and the data processing and storage capability would be enhanced. As a result, higher power density allows more computing components, or an overall smaller footprint, for the existing server. The power density trend of the industry products is illustrated in Figure 1-5. The typical power density of the AC-DC converter was in the 5W/in^3 range more than fifteen years ago [11]. Nowadays, the power density reaches about 40 W/in^3 range with discrete component technologies and 120 W/ in^3 with integrated component technologies [12]. On the DC-DC converter, because of the widely adopted soft-switching technology, the power density has been pushed to 380 W/in^3 [12]. As this trend continuous, the power density is expected to be pushed even higher in the near future.

Figure 1-4. A typical server with PSUs spaces shown by red-dashes I and II.

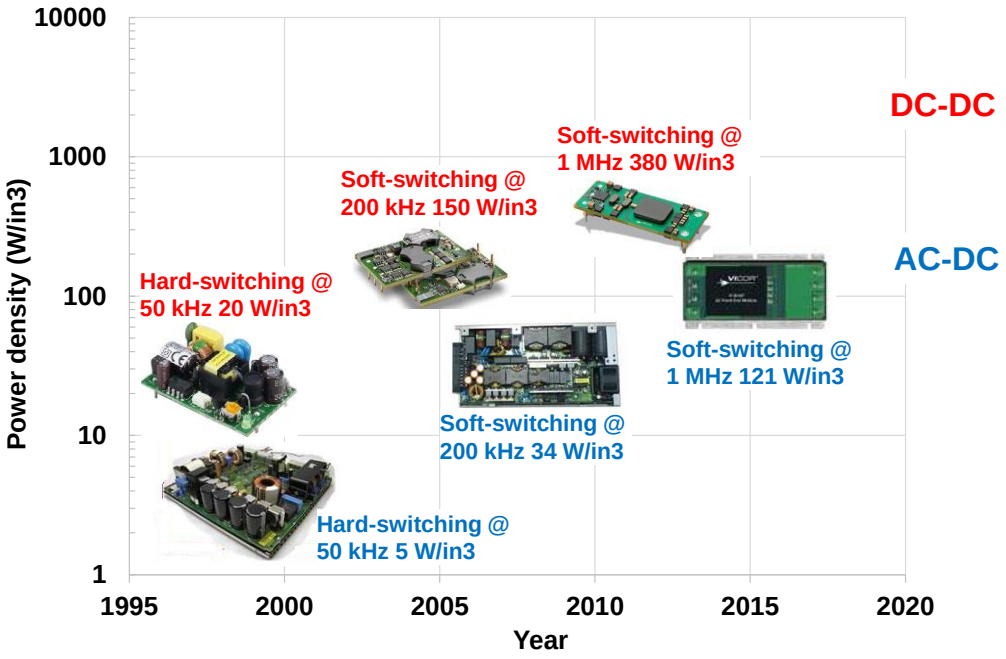


Figure 1-5. Power density trend of the industry products.

In the data center, the power is delivered from the AC electric grid to the low voltage DC electronic load, such as CPU, memory, hard drive and chipset. There are many power delivery architectures proposed or applied in data centers, including AC distribution, rack level DC distribution, and facility level DC distribution [13]. The facility level AC power delivery architectures is widely applied today, as shown in Figure 1-6. The three phase 480 V AC voltage from the electric grid first connected to the AC UPS, and then distributed by the single phase 120 V AC bus to the rack. There are several blades in the rack, and each blade consists PSUs. The PSUs convert the power from the single phase 120 V AC to the 12 V DC on-board voltage to the voltage regulators (VR). The drawback of this architecture is that there are some redundant power conversion stages, so that the overall efficiency is poor. Recently, a 400 V high voltage DC (HVDC) power delivery architecture is attracting attention. As shown in Figure 1-7, by removing several

redundant power conversion stages from the AC power delivery architecture, and pushing the efficiency of each stage with the state of the art technology, the overall efficiency has been improved by 10%, which is equal to 15% loss reduction [14]. The power converters are simplified to three power stages: the three phase 480 V AC to 400 V DC rectifier, the 400 V DC to 12 V DC intermediate bus converter (IBC), and the 12 V DC to 1.x V DC voltage regulator. Compared to the regulated DC-DC converter in the PSU, the IBC can be an unregulated DC-DC converter that has a fixed voltage transfer ratio. The IBC operates like a DC-DC transformer providing galvanic isolation between the high voltage bus and low voltage on-board bus. Since no regulation is required during the normal operation condition, the IBC can be designed at the optimal operation point to achieve high efficiency and high power density.

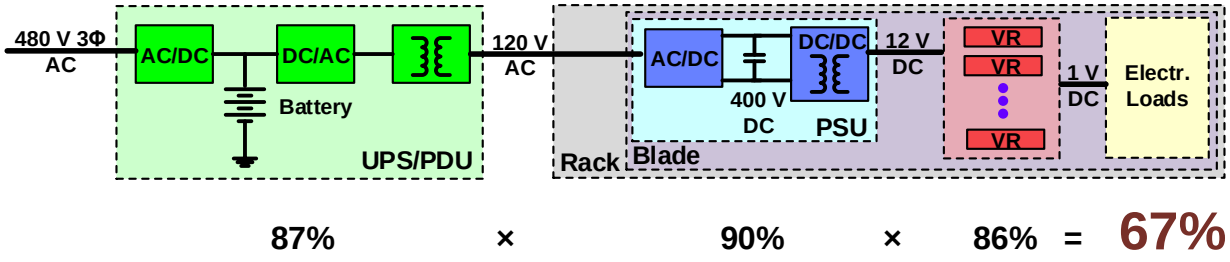


Figure 1-6. AC power delivery architecture.

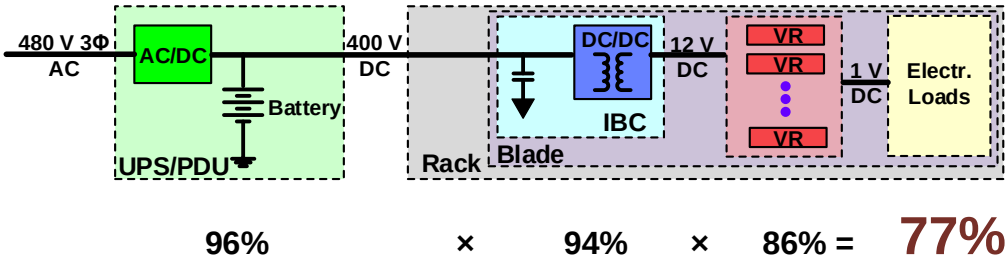
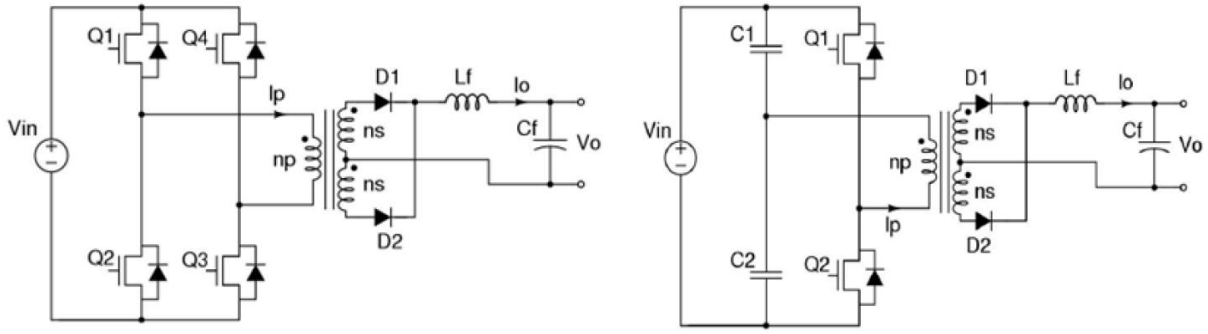


Figure 1-7. High voltage DC power delivery architecture.

1.1.2 Limitations of PWM DC-DC Converter in the IBC Stage

Soft-switching PWM DC-DC converters, such as phase shift full bridge PWM converter [15]-[17] and asymmetry half bridge PWM converter [18]-[20], shown in Figure 1-8, are widely applied in the power supply products. They can achieve zero-voltage-switching (ZVS) so that low switching loss and high frequency can be realized. ZVS can be achieved by the device junction capacitance and the transformer leakage inductance, so that no additional components are added. However, there are some drawbacks of soft-switching PWM converters, such as non-ZVS at light load, high turn-off current for devices, and non-zero-current-switching (ZCS) of the Synchronous Rectifier (SR) devices [8].



(a) Phase shift full bridge PWM converter (b) Asymmetry half bridge PWM converter

Figure 1-8. Soft-switching PWM DC-DC converters [8].

One significant limitation of the soft-switching PWM DC-DC converter in the data center application is the hold-up time requirement. In Figure 1-9, the AC-DC PSU is required to maintain the regulated DC output voltage during T_H, which is usually equal to 20 ms when the AC input voltage is lost [21]. For the IBC in the high voltage DC power delivery architecture, it also needs

to satisfy the regulated DC output voltage for 20 ms when the DC bus voltage is reducing. During the hold-up time, all the energy transported to the load comes from the DC bulk capacitor. The size and capacity of the capacitor are determined by the converter power rating and the input voltage range. The relationship between hold-up time capacitance and size versus minimum input voltage of a 300 W IBC is exhibited in Figure 1-10 and Figure 1-11. The high density power converter requires small capacitor, but small capacitor leads to wider input voltage. Therefore, in order to meet the hold-up time requirement, the IBC needs to have the capability of wide input voltage.

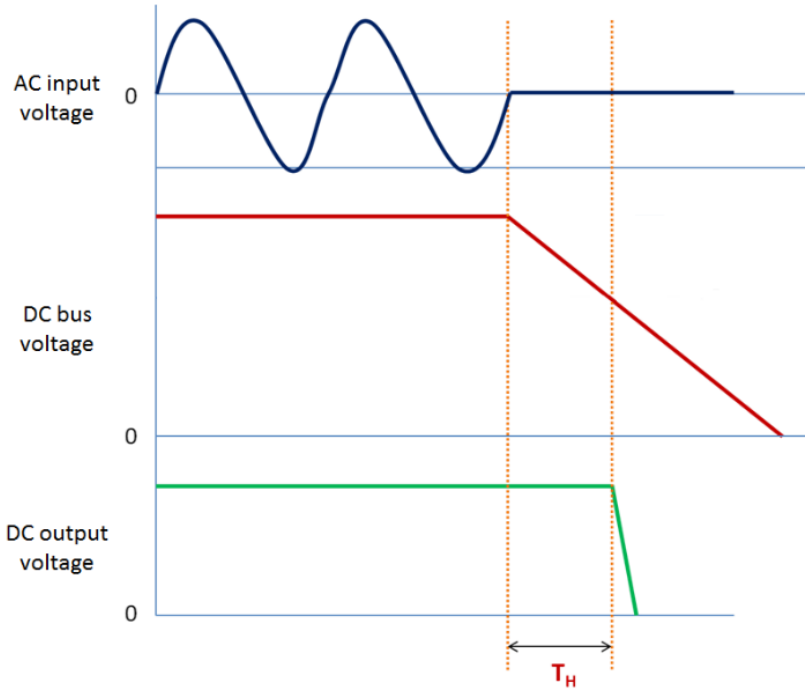


Figure 1-9. Hold-up time requirement [22].

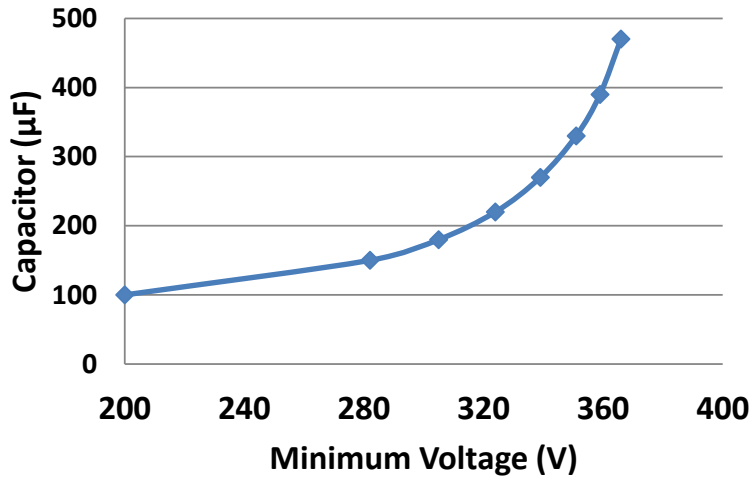


Figure 1-10. Minimum DC bus voltage vs. capacitance.

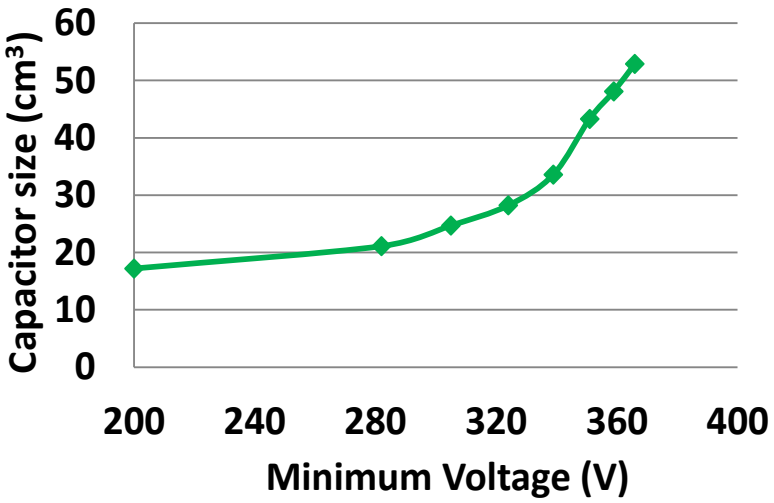


Figure 1-11. Minimum DC bus voltage vs. capacitor size.

The soft-switching PWM DC-DC converters have to sacrifice the normal operation efficiency under wide input voltage condition. The reason is that the design needs to meet the minimum input voltage operation point to achieve wide input voltage operation capability with high duty cycle, but the converter has to work in normal high input voltage operation point with low duty cycle. A

design and efficiency comparison of an asymmetrical half bridge PWM converter in different input voltage ranges is demonstrated in Figure 1-12 [8], where V_o is the output voltage and P_o is the output power. If the converter is design at 400 V point, the efficiency reaches the maximum value, while it is designed for the wide input voltage range, the efficiency drops.

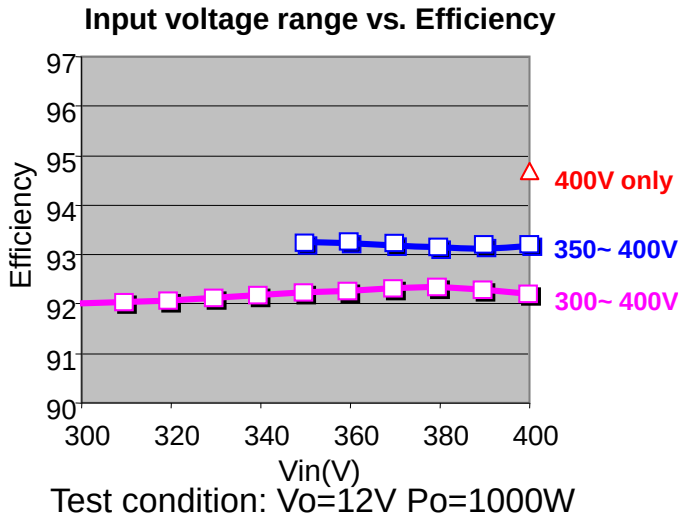


Figure 1-12. Comparison of asymmetry half bridge converter in different input voltages [8].

1.1.3 Limitations of Series and Parallel Resonant Converters in the IBC Stage

Besides the PWM DC-DC converter, resonant DC-DC converter can be also applied in the IBC stage. In the resonant converter, the resonant tank is combined with different capacitors and inductors. Simple resonant tanks consist of two or three resonant components. The two most popular resonant topologies are series resonant converter (SRC) and parallel resonant converter (PRC), which have one inductor and one capacitor in the resonant tank.

Figure 1-13 shows the topology of the series resonant converter [23]-[25], and the voltage gain is shown in Figure 1-14. In the SRC, when the switching frequency is higher than the resonant

frequency, the voltage of the switch node of the phase leg is lagging the current; the impedance of the resonant tank at the switching frequency is inductive. The devices can achieve ZVS. Based on the voltage gain in Figure 1-14, the SRC has the wide input voltage operation capability, and the operation region is on the right hand side of the resonance where the switching frequency is higher than the resonant frequency in order to achieve the device ZVS realization. The SRC needs to be designed at the nominal operation voltage V_{in_nor} and also satisfy the operation region until the minimum input voltage V_{in_min}. However, as can be seen from the voltage gain, when the quality factor Q is low, which means the converter is in the light load, the switching frequency needs to be high to keep the output voltage regulated. With a wide range of the switching frequency, the change of the voltage gain is small at light load. Besides, the SRC also has the issue of large circulating current. The circulating current flows in the resonant tank instead of being transferred to the output, which induces additional device conduction loss. Therefore, although SRC has a good capability to handle the wide input voltage, it is not a good candidate for IBC in consideration of hold-up time requirement.

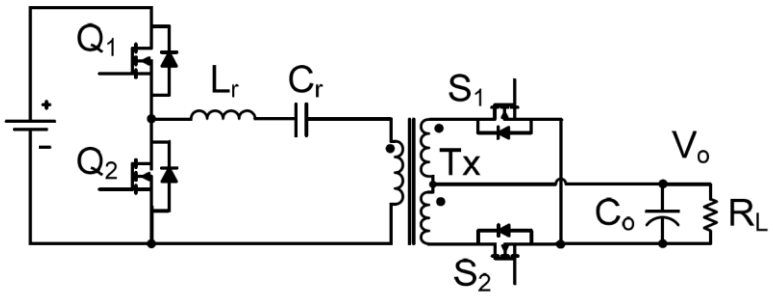


Figure 1-13. Series resonant converter.

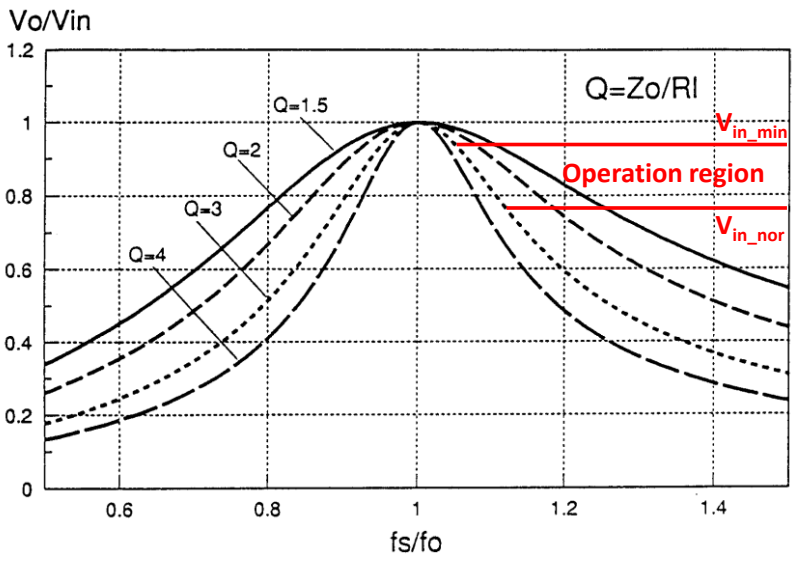


Figure 1-14. Voltage gain of SRC.

Figure 1-15 shows the topology of the parallel resonant converter (PRC) [26]-[29], and the voltage gain is shown in Figure 1-16. Similar to SRC, the operating region is designed on the right hand side of the resonance for PRC to achieve ZVS. PRC also has a good capability to handle the wide input voltage, and at light load there is no voltage regulation issue as the SRC. For example, if the converter is designed at full load and V_{in_max}, assuming Q is equal to 3. When the converter works in the light load condition, Q will increase to 10 or even higher. The increase of switching frequency to keep the output voltage regulated is small. However, the issue for the PRC is that the circulating current is high, even at the no load. The reason is that, different from the condition that the load is in series with resonant tank in SRC, the load is in parallel with capacitor or inductor in the PRC. Therefore, even there is no load, the resonant tank still exhibits a low impedance in certain switching frequency range. Therefore, PRC is not a good candidate for IBC due to the high circulating current.

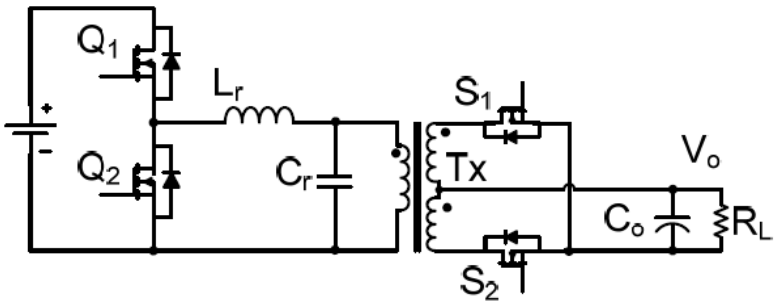


Figure 1-15. Parallel resonant converter.

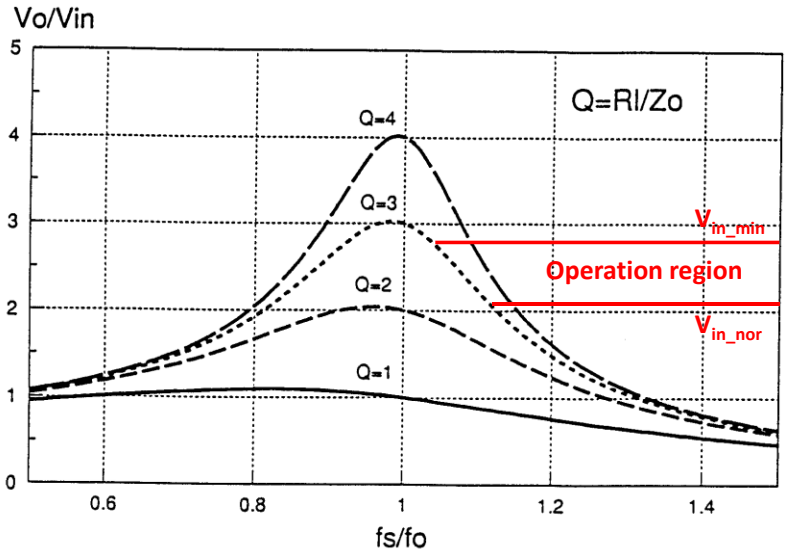


Figure 1-16. Voltage gain of PRC.

1.1.4 Opportunities and Challenges of LLC Resonant Converter

When the resonant tank includes three components, the LLC resonant converter can be derived by paralleling the load with one of the two inductors, shown in Figure 1-17. LLC resonant converter is proposed in 1990 [30], and then has drawn a lot of attentions since 2002 due to its advantages in the data center application [31]-[33]. Based on the LLC resonant tank, different

technologies, such as three-level structures, two-phase interleaved structure, over-current protection, etc. are applied for different applications [34]-[36].

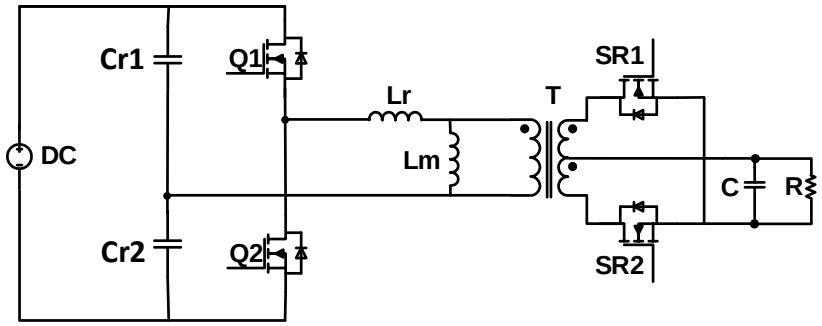


Figure 1-17. Half bridge LLC resonant converter.

The voltage gain of the LLC resonant converter has been discussed in [32] shown in Figure 1-18. According to the voltage gain, there are two resonant points of the LLC resonant tank. From the left to right, the first resonant point is achieved by resonant capacitor C_r and the combination of L_r and L_m. The second resonant point is achieved by C_r and L_r. The device can realize ZVS when the converter operates in the decreasing voltage gain region. By changing the switching frequency, the LLC resonant converter can either work in the boost mode or buck mode, and realize ZVS in both modes and the whole load range. The LLC resonant converter can be designed at the second resonant point, which is the optimal operation point to achieve high efficiency, because the primary side device can achieve ZVS and the secondary side device achieve both ZVS and ZCS. When the converter works in the hold-up time condition, the LLC resonant converter can operate in boost mode to maintain the output voltage. As a result, LLC resonant converter supports the wide input voltage without sacrificing the efficiency at the nominal operation condition, and the circulating current can be minimized by properly design of the resonant tank.

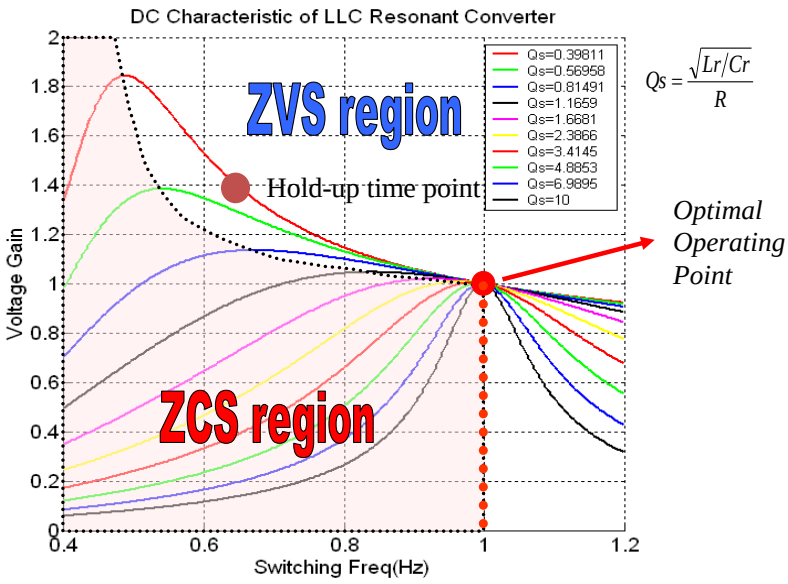


Figure 1-18. Voltage gain of LLC resonant converter [32].

When the LLC topology is applied in the unregulated IBC, it has better performance at high switching frequency. The converter input and output voltage ratio is determined by the transformer turns ratio only. First, the switching frequency is equal to the resonant frequency. Primary side device achieves ZVS and secondary size device achieves both ZVS and ZCS. The SR current is symmetrical with primary side driving signal, therefore there is no special consideration on the SR control. The SR driving can directly utilize primary side driving signal. The controller works under fixed nearly 50% duty cycle. Only during the hold-up time period, the controller needs to regulate the output voltage. The LLC resonant converter is considered as a good candidate for the IBC stage.

However, there are still challenges for the unregulated LLC resonant converter.

1. The primary side device can achieve ZVS during the entire load range; the penalty is that the magnetizing current is set to keep ZVS of all the devices. The magnetizing current

circulates in the primary side without delivering any power to the load, inducing additional device conduction loss. Therefore, high device conduction loss is one of the challenges.

2. The high frequency transformer winding loss is another challenge of the LLC resonant converter. The air gap induced fringe effect loss and terminal loss become severe when the frequency is high. The asymmetrical primary and secondary side current leading to the unevenly distributed magnetic field between the windings also increases the winding loss.
3. The selection of dead time impacts the converter loss in high frequency. Large dead time results in smaller effective energy transfer time from input to load, therefore the RMS current will be high. Smaller dead time resulting in high peak magnetizing current to realize ZVS, which also increase the RMS current equivalently. Therefore proper dead time selection is necessary.

1.1.5 Opportunities of Gallium Nitride Devices

Newly emerged wide bandgap (WBG) semiconductor devices, such as Silicon Carbine (SiC) and Gallium Nitride (GaN) devices, provide the desirable features of low specific on-state resistance, low junction capacitance, and increased junction temperature [38] [39]. The WBG device's superior performance is due to the excellent material properties, shown in Table 1-1 [40]. E_G is the bandgap energy; E_{BR} is the critical electric field for breakdown in the crystal; V_s is the saturated drift velocity; μ is the mobility of electrons. High critical electric field of the WBG devices leads to high blocking voltage with low on-state resistance; large bandgap of WBG material results in a high temperature capability; high saturated drift velocity leads to high switching speed capability [41]-[43]. Therefore, WBG power semiconductor devices have the potential to provide low conduction loss, low switching loss and high temperature capability.

Table 1-1. Semiconductor material properties [40]

Properties	Si	SiC	GaN
E_G (eV)	1.12	3.2	3.4
E_{BR} (MV/cm)	0.3	3.5	3.3
V_s ($\times 10^7$ cm/s)	1.0	2.0	2.5
μ (cm^2/Vs)	1500	650	990-2000

GaN based high electron mobility transistors (HEMTs) offers even better specific on-state resistance than the Si and SiC devices, shown in Figure 1-19 [40], because of the lateral structure device with two-dimensional electron gas (2DEG). The device structure is illustrated in Figure 1-20 [44]. The 2DEG is a gas of electrons free to move in two dimensions, but tightly confined in the third. It occurs when the GaN and AlGaN join together to form a heterojunction, and the 2DEG exists in the interface between the two materials. That is also the reason that GaN gains additional mobility (μ). The 2DEG has more than two times of the electron mobility than the GaN material itself (from 990 cm^2/Vs to about 2000 cm^2/Vs [40]). The 2DEG creates the short circuit between drain and source until the electrons in the 2DEG is depleted and the semi-insulating GaN material starts to block the voltage [45]-[47]. Therefore, GaN device is a normally-on, or depletion mode, device intrinsically. In order to turn off the device, a negative voltage relative to gate and source is needed.

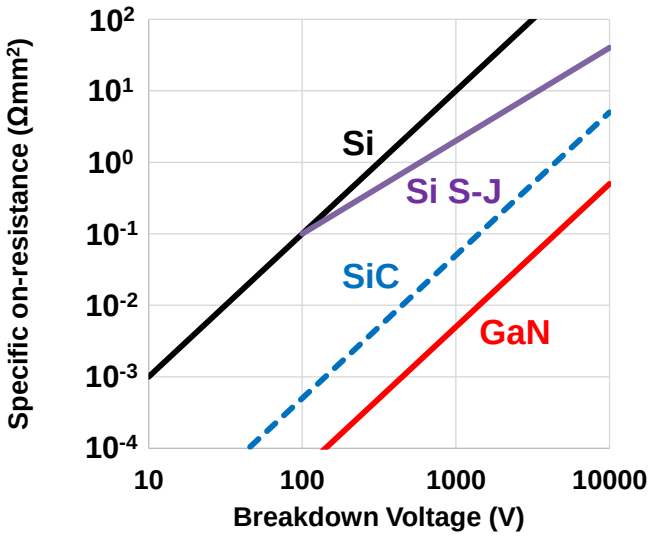


Figure 1-19. Theoretical limitation of specific on-state resistance vs. blocking voltage [40].

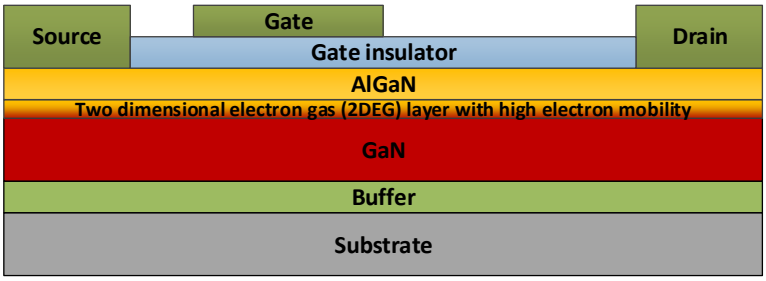


Figure 1-20. Lateral structure of GaN device [44].

In the real application, the depletion mode power devices are not suitable for the voltage source converter due to the failure of short circuit when the auxiliary power supply stops working. A normally-off, or enhancement mode, device would not suffer this limitation. Recent efforts on GaN technology has yielded low voltage enhancement mode GaN devices (eGaN FETs) [48]. The small junction capacitance and zero reverse recovery charge allow these devices to have faster switching speed and lower switching loss. As the blocking voltage of GaN HEMT increases above

600 V, the depletion mode GaN HEMT has been developed in a cascode structure with a low voltage power MOSFET to allow the device to behave like an enhancement mode device [49]. Comparing with Si MOSFET, the cascode GaN HEMT has lower on-state resistance and smaller junction capacitance as well. Therefore, the application of the eGaN FETs and the cascode GaN HEMT has the potential to reduce the device loss and improve the LLC resonant converter efficiency.

1.1.6 Summary

Increasing demands on high efficiency and high power density propel the development of data center power supplies. The limitation of PWM DC-DC converter in the IBC stage is that the optimal operation point cannot be design in the normal operation point due to the hold-up time requirement. The resonant converter can meet the wide input voltage range to support the hold-up time requirement, however, the difficult light load voltage regulation for SRC and the high circulating energy for PRC are the two main issues. LLC resonant converter is a good candidate in the IBC stage. It supports wide input voltage range with small circulating energy and good regulation capability. However there are also challenges including high device conduction loss, high transformer winding loss and optimal dead time selection. The opportunities of GaN devices are discussed, which have the capabilities to improve the LLC resonant converter efficiency.

1.2 DC-DC Converters in EV Application

1.2.1 Background

Internal combustion engines (ICE) are the dominant sources of power for vehicles, where the carbon generation is inevitable. Concerns about reducing emissions and the greenhouse effect attract increasing attention to electric vehicles (EVs). Meanwhile, EVs also have the potential to

increase energy security by diversifying the fuel utilization and decreasing the dependence on petroleum. Another important advantage of the EV is the very high efficiency of the electric traction system. The battery-to-wheel efficiency is about 85%, while the tank-to-wheel efficiency in ICE vehicles is only about 20% [50]. The energy cost of using ICE vehicles is about 12 cents per mile, comparing 2 cents per mile with EVs. Therefore, the popularity of the electric vehicles is gradually increasing. Figure 1-21 shows the projected cumulative sales targets in several countries. Together these targets add up to 5.9 million in sales by 2020, and the overall market will be more than $300 billion [51] [52].

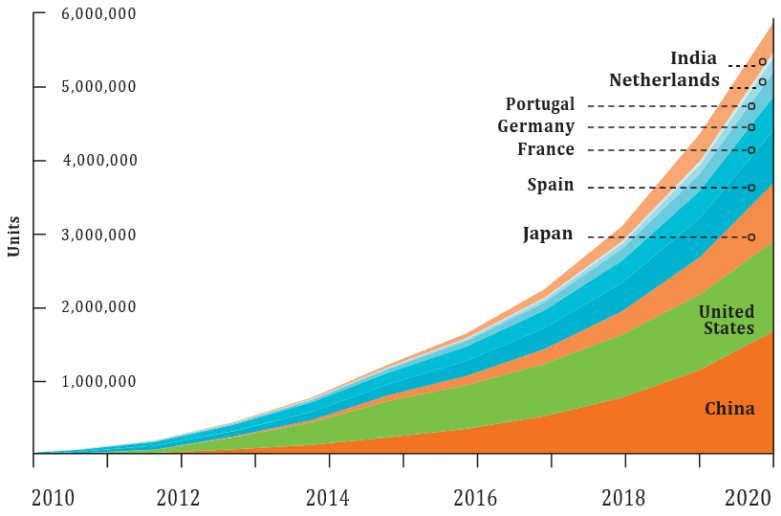


Figure 1-21. EV sales targets [51].

Improvements of power electronics in EVs are required on the cost, specific power, power density and efficiency. The traction system delivers power from the battery to the wheel to drive the vehicles. Table 1-2 shows the status and the future trend on the electric traction drive system. Comparing the status in 2010 with the future in 2020, the cost is expected to reduce 58%. The

specific power and power density are expected to increase 32% and 54%. The loss is expected to reduce 40% [53]. These trends and requirements push the progress of the power electronics technologies in the EV application.

Table 1-2. Trend of the traction drive system [53]

Traction drive System (55 kW peak power for 18 sec; 30 kW continuous power; 15 year life)				
Year	Cost ($/kW)	Specific Power (kW/kg)	Power Density (kW/L)	Efficiency (%)
2010	19	1.06	2.6	>90
2013	16	1.15	3.1	>91
2015	12	1.2	3.5	>93
2020	8	1.4	4.0	>94

The on-board charger transfers the energy from the electric grid to the battery. It makes the charging flexible and convenient, therefore the vehicle can be charged wherever the electric outlet is provided and the power requirement is satisfied. However, the on-board charger adds extra weight, volume and cost to the vehicle, therefore it is usually designed within several kilowatts range. But, considering the charging time, the several-kilowatt on-board charger leads to longer charging time. It is preferable that the on-board charger can achieve higher power without much weight increase. Besides, the galvanic isolation from the utility grid is a favorable option in the charger circuits because of safety reasons [54]-[56], so that the isolated on-bard charger is widely applied in the state of the art EVs.

The traction drive system and the on-board charger are the two significant power electronic components, which constitute the power conversion architecture in the EVs. The capability of these two parts mostly determines the vehicle's charging and driving performance. High efficiency,

high power density and low cost are the three forces to drive the improvement of the power conversion architecture under the hood.

1.2.2 State of the Art Power Conversion Architecture in EV

Similar to the data center power delivery architecture, there is also a state of the art power conversion architecture in EVs, shown in Figure 1-22. There are mainly three parts including traction drive converter with drivetrain DC-DC and inverter, on-board charger, and the low power DC-DC converter working for 12 V loads. These three parts are independent to each other.

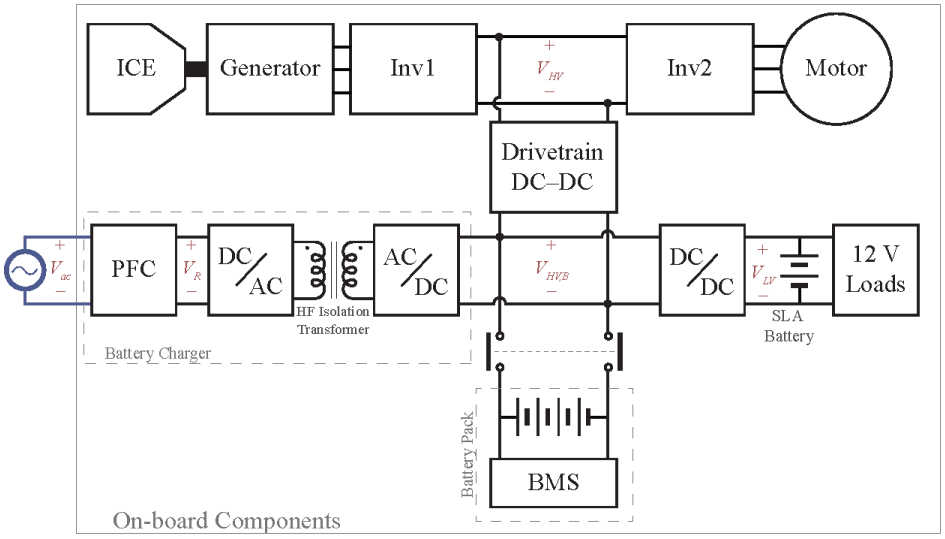


Figure 1-22. State of the art power conversion architecture in EV.

The bidirectional drivetrain DC-DC converter is applied as the interface between the battery voltage and a regulated DC voltage for the motor drive inverter. It serves to increase the battery pack voltage to a higher regulated DC bus voltage. This configuration allows the decoupling of battery and motor, and serves to increase the operating range and efficiency of the electric drive,

composed of motor and inverter. The boost converter is an additional converter in the traction drive system; therefore, it should be robust, small, and high efficiency. The application of the boost converter should increase the overall system efficiency, without sacrificing much of the size and weight.

The structure of the on-board battery charger is similar to the PSU discussed in Section 1.1.1. It provides the power from the AC grid to the battery. As is mentioned before, based on some current standards [55] [56], the isolation is necessary for this stage for the safety reasons. In the on-board charger, the AC power is rectified by the front-end PFC converter to the DC voltage and meet the THD and power factor requirement. The second DC-DC converter is for the isolation and to output the regulated DC voltage. As a result, two power conversion stages are necessary to fulfill these functions and requirements. Besides there are also many passive components in the on-board charger such as the EMI filter, the inductor and the isolation transformer, which have a negative impact on the converter size and weight.

The low power DC-DC converter for the 12 V loads is for other electrical or electronic devices on the vehicle, such as lighting and entertainment. The power is originally from the auxiliary lead-acid battery in the ICE vehicles and some previous HEVs. But it is being integrated in the power conversion architecture to use the power from the main battery directly.

The advantage with the independent power conversion stages is that they have separate functions to handle the power for difference purposes, and different power converters are used to decouple individual elements from the system through DC buses. From the manufacture's point of view, different power stages can be provided by different suppliers. The independent design of each converter can be based on the requirements for input/output voltage range and power levels.

The maintenance of the power converter stages is also convenient. It is a modularized concept that has been already widely accepted by the industry.

1.2.3 Limitations and Challenges

Although there are advantages for the state of the art power conversion architecture, the limitation is that the power conversion stages only realize the single-function and generic design without consideration of the actual system operation. The single-function converters lead to extra cost, size and weight of the power electronics under the hood. It is preferable that the single-function converters can be combined into one.

The drivetrain DC-DC converter and the on-board charger are separated, however they never operate at the same time, and they share the same battery bus voltage. In other words, the input voltage of the isolated DC-DC converter in the on-board charger has the similar voltage range with the input voltage of the drivetrain DC-DC converter. Consequently, although these two converters are separated with the single function, it is possible to combine the two DC-DC converters into one. Moreover, the existing on-board charger usually has low power handling capability so as to the low charging time. If the on-board charger can be integrated in the traction drive and take the advantages of the high power capability, fast charging can be achieved.

Besides, if the charger and the drivetrain DC-DC converter are combined, the charger DC-DC converter can be designed as bidirectional as well to work in the drivetrain mode. Traditional drivetrain DC-DC converters are normally single phase boost converters designed as general, single-purpose converters which are optimal for their ability to meet high power demand with a minimum semiconductor cost. These converters suffer from poor efficiency at light load and at high voltage step-up ratios, both of which are frequent operating modes for the vehicle. Therefore,

if the charger DC-DC converter can be designed with high efficiency for the drivetrain mode, the efficiency of drivetrain DC-DC converter at the conditions of light load and high voltage step-up ratios can be improved.

The challenges is on the design methods to combine the on-board charger and drivetrain DC-DC converters to realize an integrated DC-DC converter. The design of the integrated DC-DC converter needs to consider the optimization in the different operation modes, by making the charger DC-DC converter efficiently work at light load and high voltage step-up ratio, and making the drivetrain DC-DC converter satisfy the wide load range up to full load.

1.2.4 Summary

The 10-year future trend of the efficiency, power density and cost is propelling the development of the EV power converters. The state of the art power conversion architecture in the EV is realized by different single-function converters, which leads to extra cost, size and weight. It is possible to combine the on-board charger and the drivetrain DC-DC converter, because they share similar input/output voltages and never operate at the same time. The challenges will be the design methods of the converter integration and the converter design to obtain high efficiency in different operation modes.

1.3 Research Objectives and Approaches

The objective of the research work in DC-DC converter in data center application is to develop the design and loss analysis approaches to improve the efficiency of LLC resonant converter with GaN devices. The objective of the research work in DC-DC converter in electrical vehicle application is to develop the design and loss analysis approaches for the integrated DC-DC converter, and utilize the DAB converter to improve the efficiency of traditional drivetrain DC-

DC converter in light load and high voltage step-up condition. Combing together, the overall objective is to develop the design and loss analysis approaches to improve the efficiency of the DC-DC converters

The approaches are:

1. To establish the relationship of device parameters with device loss and transformer winding loss for LLC resonant converter.
2. To derive the optimal device selection and dead time selection method by considering the device parameters and the impact of transformer winding loss.
3. To investigate the magnetic design for both LLC and integrated DC-DC converter.
4. To derive the design method and loss model of integrated DC-DC converter in the targeted operation region.

1.4 Dissertation Organization

The dissertation is organized as follows:

Chapter 2 reviews the previous research activities on the DC-DC converters in data center and EV applications. To address the challenges in the unregulated LLC resonant converter, previous work focuses on the device selection and application criteria, the winding structure design and improvement, and the device loss based dead time optimization. In the EV application, some of the integrated converter topologies have been proposed before. Most of the integrations were on the motor side, and quite few were on the DC-DC side.

Chapter 3 provides an analytical loss model of the LLC resonant converter that establishes the relationship between the device parameters and converter loss. After that the GaN device impact on the converter loss is analyzed and compared with the Si-based converter. Then, a new

perspective of extra winding loss due to the asymmetrical primary and secondary side currents is proposed. The extra winding loss under the GaN device design and Si device design is also compared. The prototype test verifies the loss improvement of the GaN device based converter.

Chapter 4 analyzes the soft-switching behavior of the 600 V cascode GaN HEMT. Detailed switching transient in each time interval are presented. The gate drive impact on the soft-switching behavior is qualitatively discussed. Extra switching loss has been revealed for the cascode GaN HEMT, where the outside switching waveform behaves with a soft-switching shape. The thermal test verifies the existence of the extra switching loss.

Chapter 5 proposes an improved LLC resonant design approach with an optimal dead time selection that considers both device loss and winding loss. In addition, an external inductor design technique is proposed to reduce the device loss and transformer winding loss. The test results show the efficiency improvement by applying the external inductor.

Chapter 6 discusses the integrated DC-DC converter design for the EV application. A dual function magnetic component needs to meet requirements for both the transformer in the on-board charger and the inductor in the bidirectional drivetrain DC-DC converter. The design approach of the integrated magnetic components is discussed. After that, a design method for the integrated DC-DC converter in traction drive mode has been proposed. The integrated DC-DC converter operates as the DAB converter in the targeted operation region to improve the efficiency in the light load and high voltage step-up ratio condition. The test result verifies the efficiency improvement by applying the DAB converter.

Chapter 7 summarizes the dissertation and the contributions, and provides the suggestions on the future work.

2 Literature Review

As discussed Chapter 1, the challenges of the LLC resonant converter are the high device conduction loss, high transformer winding loss and the dead time optimization. The related previous research work in these aspects will be reviewed in this chapter. For EV DC-DC converter, in order to address the challenges and the limitations of the state of the art separated power converters under the hood, the converter integration of the charger and drivetrain converter was studied before. Several integrated converter topologies will be reviewed in this chapter.

2.1 Device and Magnetics of LLC Resonant Converter

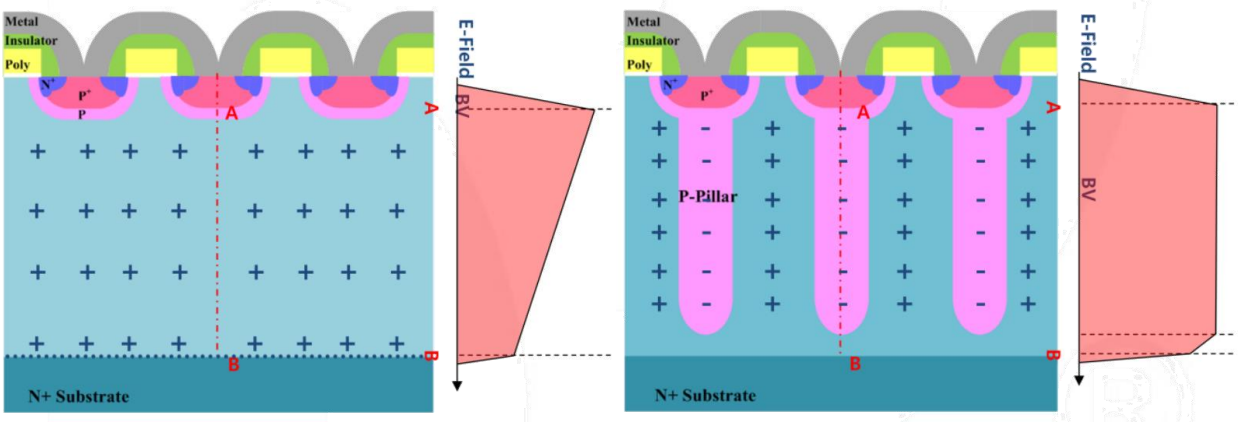
2.1.1 Device Related Technologies for Device Loss Reduction

LLC resonant converter can realize the device ZVS in the entire load range, therefore the switching loss only includes the device turn-off loss, which is small for the power MOSFETs. The conduction loss is the dominant in the device loss.

Several research efforts have been spent on reducing the device conduction loss, one of which is to reduce the device on-state resistance through reforming the device structure. Super junction MOSFETs have greatly improved the specific on-state resistance of high voltage power MOSFET [57]-[66]. For conventional high voltage MOSFETs, the voltage blocking capability in the drain drift region is determined by drift region doping and its thickness, shown in Figure 2-1(a) [63]. The thick and lightly doped epitaxial drift region is needed to support higher breakdown voltage, which also contributes high on-state resistance. This results in about 95% of the device resistance, while in the low voltage MOSFET, only about 30% of the transistor resistance is in the drain drift region [61]. The intrinsic resistance of a conventional epitaxial drift region for a given breakdown

voltage is the “silicon limit line” in Figure 1-19, which was a barrier to improved performance in high-voltage MOSFETs.

Figure 2-1(b) shows the structure of the super junction that overcomes the challenge of the high resistance of the drift region [63]. Vertical P-Pillars are inserted into the drift region. When the transistor is blocking the voltage, an electrical field is built up to drive the charge toward the contact regions between P and N. The space charge layer builds up along the physical PN-junction across the whole PN-Pillared structure. The drift region is completely depleted and the voltage sustaining layer is formed by the P-Pillars and N^- epitaxial layer. Equivalently, the PN-junction and N^- drift region for voltage blocking is expanded. The super junction MOSFET provides a new power device technology to achieve one-third of specific on-state resistance compared with the standard MOSFET. The device conduction loss is dramatically reduced [64]-[66].



(a) Standard MOSFET (b) Super junction MOSFET

Figure 2-1. Cross section structure of standard and super junction MOSFET [63].

The opportunities of the GaN devices has been discussed in Chapter 1. Significant research efforts have been spent on GaN HEMTs and GaN converters in recent years. The static characteristic and switching performance of eGaN FETs and cascode GaN HEMTs were evaluated in [67]-[70], which showed ultra-fast switching speed and low switching loss. Hard-switching GaN-based power converter such as synchronous buck converter, boost converter and inverter demonstrated great efficiency improvement over the Si based counterparts in [71]-[76]. While the GaN HEMTs show significant advantages in hard-switching converters, they also have benefits in soft-switching converters. The eGaN FETs were compared with Si MOSFETs in a dual active bridge converter in [77]. The combination of the GaN and Si devices achieved the lowest total loss. In [78], eGaN FET and Si MOSFET were each applied in the 1.2 MHz unregulated isolated resonant converters. The eGaN-based converter improved the efficiency from 95% of the Si design to 96%. A 5 MHz soft-switching resonant converter with 89.4% efficiency demonstrated high switching frequency capability of the eGaN FETs in [79].

Device figure-of-merit (FOM) is an effective way to evaluate the device performance and select the proper devices for different applications [80]. The FOM is usually derived from the device loss model as well as the converter loss model. Different device loss model result in different FOMs, and certain FOM can only be applied to certain converter topology. A device FOM for the LLC resonant converter was proposed in [37]. Due to ZVS operation of LLC resonant converters, the turn-on loss of MOSFETs is eliminated. The turn-off loss, gate-driving loss and conduction loss need be considered to derive the proper FOM. The FOM of MOSFETs for LLC resonant converters is derived from (2.1) and (2.2), and expressed in (2.3). In (2.1), the first portion represents the turn-off loss, the second portion represents the conduction loss and the third portion

represents the driving loss. The FOM described in (2.3) can be applied to choose the suitable primary side devices for LLC resonant converters.

$$P_{loss} = \frac{V_{in}I_{off}}{2}\frac{(Q_{gd}+Q_{gs2})R_g}{V_{plt}} \times f_s + \frac{I_0^2}{n^2}\frac{\pi^2}{4}R_{on} + Q_g V_{gs} f_s \tag{2.1}$$

$$K_{loss} = 1 + \frac{V_{gs}}{V_{plt}-V_{th}}\frac{2V_{plt}V_{gs}}{V_{in}I_{off}R_g} \tag{2.2}$$

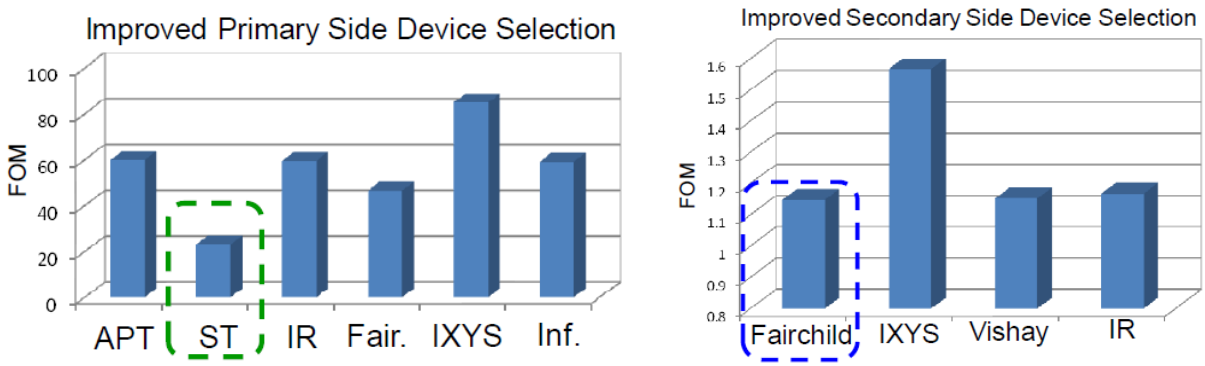
$$FOM = (Q_{gd} + K_{loss}Q_{gs2})R_{on} \tag{2.3}$$

For the secondary side devices, assume there is no body diode conduction when proper secondary side driving scheme is applied, and also assume that the device realize ZCS turn off when the converter operates at resonance. The FOM is derived from (2.4) and expressed in (2.5)

$$P_{loss\_SR} = I_{rms\_SR}^2 R_{on\_SR} + Q_{g\_SR}V_{gs\_SR}f_s \tag{2.4}$$

$$FOM = Q_{g\_SR}R_{on\_SR} \tag{2.5}$$

Based on the derived FOM for both primary side and secondary side devices, the device loss comparison and selection is shown in Figure 2-2 [37]. The devices with the minimum FOM can be selected. Besides, the results in Figure 2-2 is from a 1 kW LLC resonant converter. If the converter specification changes, the LLC FOM will be still suitable but will result in different device selection results. It should be noted that, there are still some limitations of the above FOM. First, the turn-off loss in (2.1) is overestimated, since most of the energy is stored in the device output capacitance during the turn-off transition. But, it is assumed in the (2.1) that the entire energy is dissipated in the channel. Second, the output capacitance for different devices will lead to different RMS current so as to different conduction loss, which is not considered in (2.1).



(a) Primary side device selection (b) Secondary side device selection

Figure 2-2. The device selection with FOM [37].

Besides the proper device selection method to minimize the device loss, device paralleling is also an effective way to reduce the loss, especially on the secondary side devices with low voltage and high current output [37]. The device paralleling leads to low conduction loss but usually high driving loss when the switching frequency is high. The driving loss is considered with different gate source voltages and gate charges. As shown in (2.4), the device driving loss and conduction loss need to be combined together to determine the minimum secondary side device loss. One issue that was not discussed in [37] is that the paralleling of secondary side device will also increase the overall output capacitance that participate in ZVS transition. Therefore, the number of the device in paralleling needs to be carefully investigated.

In sum, in order to reduce the device loss, super junction power MOSFET was developed to replace the standard MOSFET. The newly emerged GaN device demonstrated great potential to reduce the device loss based on previous research efforts. The device selection criteria and device paralleling was previously applied in the Si-based LLC resonant converter. The GaN device benefits on the LLC resonant converter loss will be discussed in the Chapter 3. A relationship of

device and converter design parameters to the device loss is established based on the analytical model of LLC resonant converter. The factors that have not been considered in the previous work, such as device output capacitance impact, will be taken into consideration.

2.1.2 Magnetics Related Technologies for Winding Loss Reduction

In the high frequency LLC resonant converter, the transformer loss accounts for a large part of the overall converter loss [37]. For the high frequency and high current transformer, the proximity effect and skin effect leads to high AC resistance so as to high transformer winding loss. In order to have a clear insight on the causes of transformer winding loss, according to the previous discussion [81]-[92], the transformer winding loss can be roughly break down to the pure winding loss, the terminal loss and the fringe effect loss.

The pure winding loss refers to the loss that happens regularly on the transformer windings. Usually, in order to simplify the design and loss analysis, when the copper thickness of the PCB winding is equal to one penetration depth, and the interleaving winding structure is applied, the AC winding resistance is approximately equal to the DC winding resistance [81]. However, more detailed research based on the FEA simulation found that the winding loss has been underestimated. There are still high current density areas on the surface or at the corner of the windings [82] [83]. A new perspective of the transformer winding loss based on the minimum electric and magnetic energy principle was discussed in [85]. The mechanism of current sharing among parallel windings was studied. In order to have a uniformly distributed current among the windings, the asymmetrical winding structure was applied [85]. Further, a hybrid PCB winding structure to reduce the winding loss was proposed in [86] shown in Figure 2-3. The primary side winding uses Litz wire instead of the PCB copper. The Litz wire has good capability to minimize the eddy current effect. But the winding structure is more complicated than the conventional PCB winding structure. The winding

paralleling approach was also applied in the research in order to reduce the winding loss. However, due to the eddy current effect, the current in the paralleled winding was not shared evenly. The design of PCB windings in parallel for planar transformer to have evenly shared current was discussed in [89].

Usually, the transformer can be either assembled on the power board or integrated in the power board. Both of these approaches will inevitably induce the transformer winding terminals. The PCB winding is usually based on the multilayer structure, but the devices and components are on the top or bottom layer of the power board, therefore the current in the middle layer of the PCB winding needs to find a path to the surface of the power board, which will be the transformer winding terminals. The drawback of the existence of transformer winding terminals is that the high frequency eddy current effect induces high winding terminal loss [84]. The currents in adjacent terminals with opposite directions attract each other. Thus, high losses and hot spots on the terminals are generated, which deteriorates the efficiency significantly. In order to reduce the terminal loss, in [84] and [86], the secondary side windings were separated with several PCBs in stack, and the devices and other components were mounted on each transformer winding. In that way, there was no high frequency AC terminals connected together, while the DC output terminals were connected together, shown in Figure 2-3. Another approach is the matrix transformer, which was discussed in [87] and [88] to reduce the terminal loss. The transformer is divided into two in parallel, and all the secondary side windings are on the top or bottom layer of the PCB winding. The secondary side current can directly flow through the devices and components on the top or bottom. There is no current flowing from the middle layers, therefore no terminal loss. Besides, the benefit of this approach is that the transformer winding can also be easily integrated with the power board, shown in Figure 2-4.

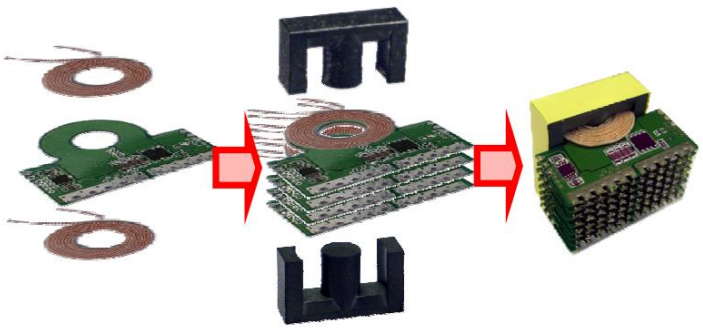


Figure 2-3. Hybrid transformer winding and separated secondary winding structure [84] [86].

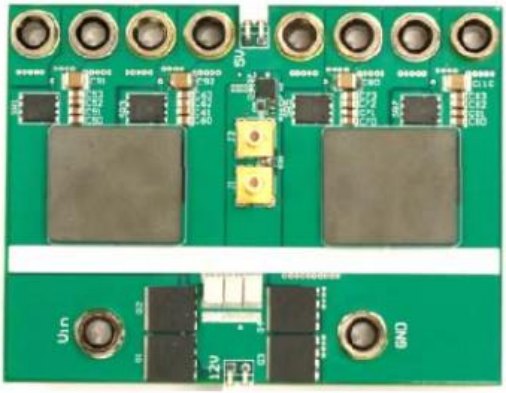


Figure 2-4. LLC resonant converter with matrix transformer [87] [88].

In order to achieve ZVS of the device during the entire load range, sufficient magnetizing current is necessary. The magnetizing inductance in the transformer provides the current. A large gap is required to achieve the designed magnetizing inductance [84] [85]. When the windings that carry the high frequency current are close to the air gap, the fringe effect loss is induced. The fringing flux penetrates the PCB winding, and high eddy current is generated inducing high winding loss shown in Figure 2-5. Meanwhile, the fringe effect winding loss is also related to the gap distance [84]. Large air gap induces large fringe effect winding loss. The solution to the fringe

effect loss is either to arrange the windings far away from the air gap or use the distributed air gap core [84].

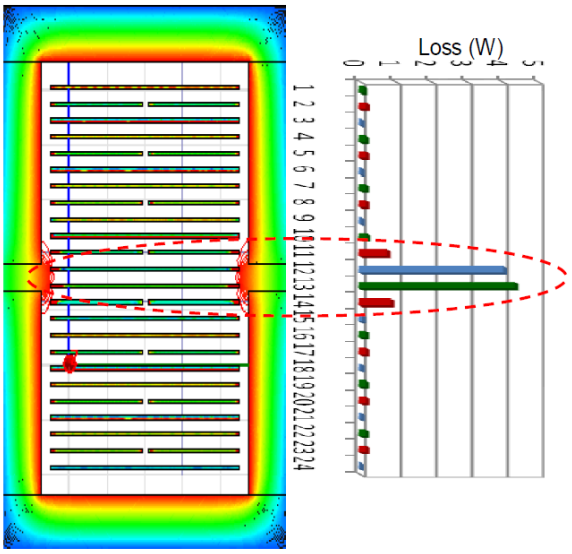


Figure 2-5. Fringe effect loss due to the air gap [84].

In sum, previous research efforts on the LLC transformer were mainly on the different winding structures and layouts. The device impact on the transformer winding loss has not been analyzed, which means if a better device is applied in the LLC resonant converter, it will reduce the transformer winding loss. Moreover, for the high power density, a commonly accepted approach is that the magnetizing inductance should be integrated in the transformer by an air gap. However, the air gap results in high fringe effect loss as well as the asymmetrical primary and secondary side current induced winding loss. The device impact on the transformer winding loss and the asymmetrical primary and secondary side current induced winding loss will be discussed in Chapter 3. An external inductor approach to reduce the winding loss will be discussed in Chapter 5.

2.1.3 Device Loss Based Dead Time Optimization

Dead time selection, as well as the magnetizing inductance selection, in the LLC resonant converter is critical to the converter loss. Large dead time results in smaller effective energy transfer time from input to load, therefore the RMS current will be high in order to deliver the same amount of energy. Smaller dead time results in high peak magnetizing current to achieve ZVS, which also increases the primary side RMS current equivalently.

The first high frequency LLC resonant converter design procedure was discussed in [93], the design flow chart is shown in Figure 2-6. In this flow chart, the LLC resonant converter design was based on switching frequency, transformer turns-ratio and device selection. The dead time was selected to guarantee ZVS operation of the devices only.

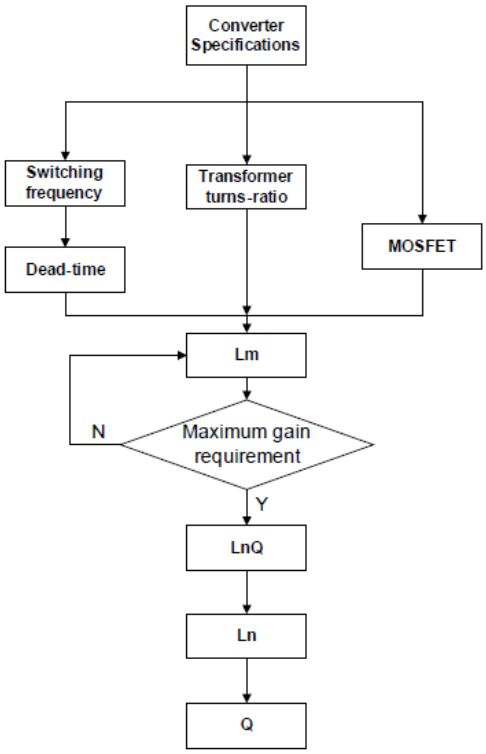


Figure 2-6. Design flow chart without dead optimization [93].

An improve design approach considering the dead time optimization was discussed in [33]. The design flow chart is shown in Figure 2-7. The dead time optimization was extracted to be an independent design step. The impact of the dead time to the converter current was discussed in [33]. The optimal dead time leads to the minimum RMS current. The limitations of this design approaches are that, first, although the device junction capacitance was considered in the design, it was only considered as a lumped capacitance C_j. The specific value of the capacitance, the numbers of the devices in parallel and the relation between the capacitance and on-state resistance were not considered. The impacts of primary side device output capacitance and secondary side device output capacitance were not analyzed. Second, there was no discussion on the dead time optimization based on the transformer winding loss, and the device was not the only impact factor on the dead time. An improved dead time optimization considering both device loss and transformer winding loss will be discussed in Chapter 5.

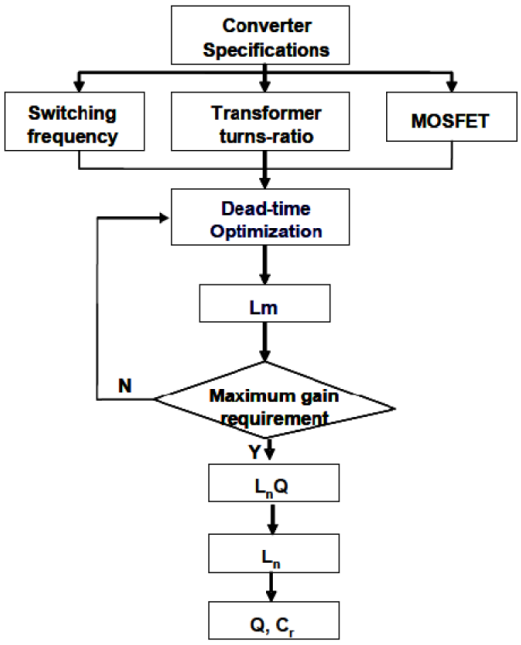


Figure 2-7. Design flow chart with dead optimization [33].

2.2 Integrated Converter for EV Application

In the state of the art power conversion architecture in plug-in hybrid electrical vehicle (PHEV) or electrical vehicle (EV) shown in Figure 1-22, the drivetrain converter and on-board charger are separated, but the devices and passive components that participate in the operation of both traction mode and charging mode are similar, and both of the converters are connected to the battery. Therefore, it is possible to integrate two converters together to reduce the number of system components, size, weight and cost. The integrated topologies can be classified as the motor side integration and the DC-DC converter side integration. Most of the previous integration approaches were based on the motor side integration. The reason was that in the EV drive train, the battery output voltage is directly connected to the input of the inverter, and the inverter is connected to the motor. Therefore, if the power flows reversely from the motor winding to the battery, it becomes a battery charger. In some EVs nowadays, a bidirectional DC-DC converter is usually applied between the battery and the inverter to regulate the battery voltage and improve the inverter and motor efficiency. Besides, an isolated DC-DC converter is applied in the charger for safety reasons. Therefore the converter integration is also possible to achieve in the DC-DC side integration.

The concept of the integrated converter in EV application is firstly proposed in 1985 [94]. The topology is shown in Figure 2-8. It is based on the silicon-controlled rectifier (SCR) and diode to realize the motor drive inverter. When in the charging mode, the motor winding behaves as the inductor, and the inverter is used as the rectifier with the THD and power factor requirement. The maximum power rating was 3.6 kW at 220 volts and the efficiency was around 80% to 86 %, which is relatively low compared with the state of the art technology.

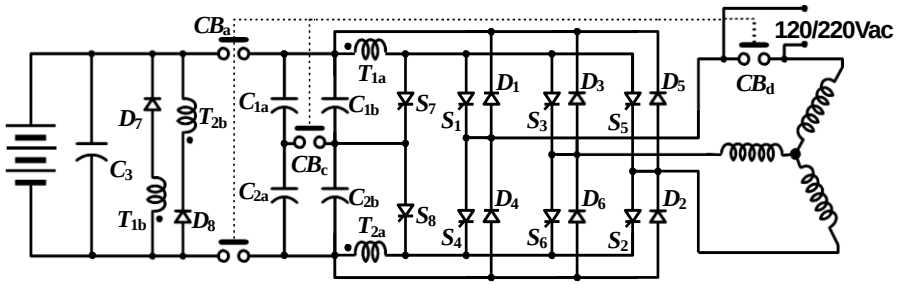


Figure 2-8. SCR based integrated converter [94].

A patent of integrated motor drive and charger based on an induction motor was published in 1994 [95]. The idea is to use the motor winding as a set of inductors during charging mode to constitute a boost converter with unity power factor. Figure 2-9 shows the schematic of the integrated converter. By adding some extra relays, the machine windings are reconfigured to be inductors in the charging mode. The detailed operations are: when K1 is closed and K2 and K2' are open, the converter is under the traction mode; when K1 is open and K2 and K2' are closed, the converter is under charging mode. In this topology, the battery voltage should be more than maximum line-line peak voltage in the input to guarantee unity power factor. Besides, a line filter is used to eliminate the switching ripples and spikes from the line side current.

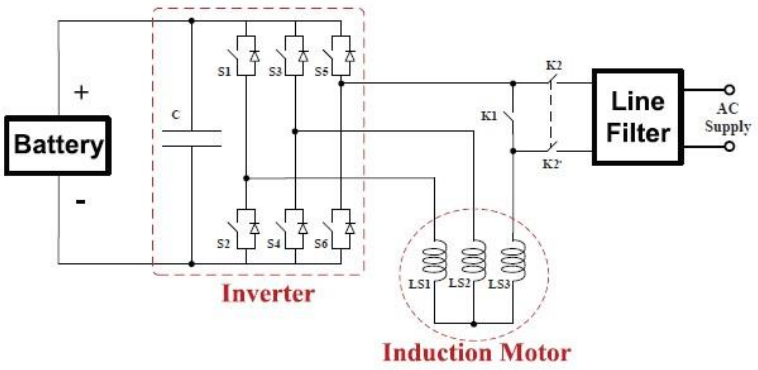


Figure 2-9. Integrated converter based on induction motor [95].

A non-isolated integrated charger was described in [96]. The authors use the three-phase inverter as a single phase leg in the charging mode, see Figure 2-10. The switches S2, S4 and S6 operate at the same time as a single bottom switch in the boost converter and the switches S1, S3 and S5 operate as a single top switch in the boost converter. Therefore, the circuit is a single-phase boost converter. All three windings of the motor are used in charging. Additional power rectifier and line filter are necessary during charging. The drawback is the additional rectifier and line filter are added and they also limit the charging power capacity of the charger.

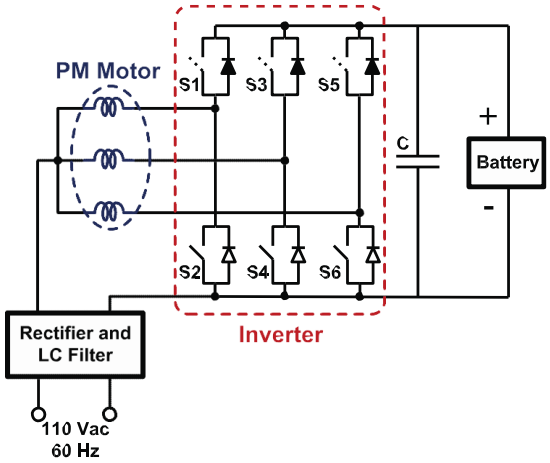


Figure 2-10. Integrated converter based on PM motor [96].

In the hybrid electrical drive system, a bidirectional DC-DC converter is applied as the interface between the battery and motor drive. An auxiliary inverter and an induction machine transfer the energy from the engine to the battery when the vehicle is running. Figure 2-11 exhibits a solution that the bidirectional DC-DC converter, the auxiliary motor and inverter are considered to behave as the on-board charger [97]. The auxiliary inverter and motor are in parallel with the main inverter and motor in the charging mode.

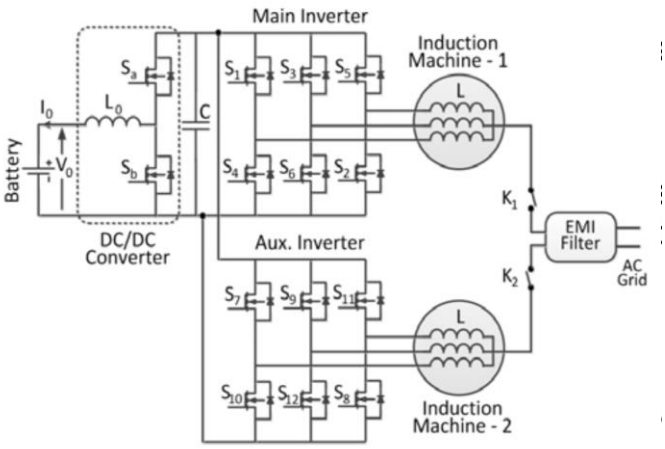


Figure 2-11. Motor side integration with the existence drive train DC-DC converter and auxiliary inverter [97].

Above typical examples belongs to the motor side integration. There are also some extensions based on the above topologies. The fundamental concepts that utilize the motor winding and the inverter are the similar [98]-[103].

A DC-DC side integration was presented in [104], which is based on a non-isolated DC-DC converter in charger integrated with the drivetrain DC-DC converter. The topology is shown in Figure 2-12. The converter can operate in non-inverting buck-boost mode to transfer the energy from V_{AC} to V_{batt}, and a diode rectifier is in front of that. The converter can also operate in the boost mode from V_{batt} to the V_{hv}, and the buck mode when the vehicle is in regenerative breaking.

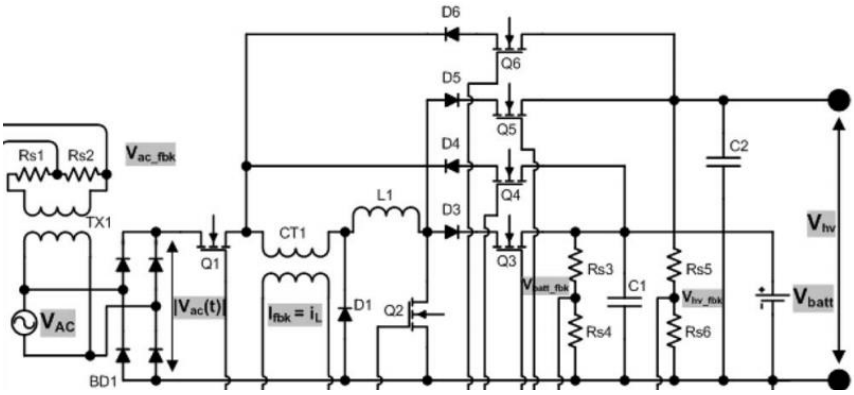


Figure 2-12. Charger DC-DC converter and drivetrain DC-DC converter integration [104].

According to the literature review on the integrated charger and drivetrain converter, most of the integrated topology are based on the motor side integration since the motor winding and the inverter can be directly utilized as a PFC converter in the charging mode. Very few case shows the DC side integration. An isolated DC-DC converter usually exists in the on-board charger in the state of the art electrical vehicle. No previous publication presents the integration of the drivetrain DC-DC converter and the isolated DC-DC converter in the charger. Chapter 6 will presents a novel DC-DC converter topology that integrates drivetrain DC-DC converter and the isolated DC-DC converter, and describe the different operation modes and design method.

2.3 Summary

In order to address the challenges in the high device loss and transformer winding loss of the LLC resonant converter, the literatures in several aspects have been reviewed. First, the invention of the super junction structure greatly reduce the on-state resistance of the high voltage power MOSFETs. The newly-emerged GaN devices showed great improvements on the converter efficiency and power density in previous research efforts. But the GaN devices benefits in LLC resonant converter were not discussed before. Second, the device selection criteria is useful to

select a device that best fits the converter in certain specifications. The FOM of LLC converter was proposed for the primary and secondary side device selection. However, the impact of the device parameters on the current was not considered in the derivation of the FOM. Third, device paralleling helps to reduce the conduction loss. However, in the high frequency converter, the driving loss and the output capacitance will have the significant impacts on the converter efficiency. It is necessary to investigate device paralleling impact in the GaN-based LLC resonant converter.

For the transformer winding loss, the literatures on the pure winding loss, terminal loss and the fringe effect loss are reviewed. The pure winding loss can be reduced by hybrid winding structure using Litz wire; the winding terminal loss can be reduced by matrix structure transformer; and the fringe effect loss can be reduced by keeping the winding far from the air gap or by reducing the air gap. The common accepted concept is that the magnetizing inductance should be integrated in the transformer by air gap. However, the integrated magnetizing inductance results in high fringe effect loss as well as the extra winding loss due to the asymmetrical primary and secondary side current, which was not analyzed in the previous work.

In the first high frequency LLC resonant converter design procedure, the dead time was selected to guarantee ZVS operation of the devices only. In the improved design approach afterwards, the impact of the device parameters are considered, and the dead time optimization was extracted to be an independent design step. The limitations are that, the device junction capacitance was only considered as a lumped capacitance C_j without specific impact of either primary side devices or secondary side devices. Besides, there was no discussion of the impact of transformer winding loss on the dead time selection.

Several integrated topologies in EV application are reviewed. Most of them are based on the motor side integration; simply utilize the motor winding as the inductor and the inverter as the

rectifier in the charging mode. Usually, an extra line filter is also necessary for THD and power factor requirements. One previous research work studied the DC side integration with a non-isolated DC-DC converter in the charger and a drivetrain DC-DC converter. No previous publication presents the integration of the drivetrain DC-DC converter and the isolated DC-DC converter in the charger. A novel integrated DC-DC converter topology based on the state of the art power conversion architecture in the EV will be discussed in this dissertation.

3 GaN Device Impact on LLC Resonant Converter

The benefits of GaN devices on LLC resonant converter will be discussed in device loss and transformer winding loss. First, the GaN device static and switching performance is characterized to obtain some necessary data, such as the turn-off loss, that supports the GaN-based LLC resonant converter design and loss analysis. Second, the analytical loss model of LLC resonant converter at resonance is provided. The relationship between the device parameters and converter loss is established. The procedure of the relationship derivation is also clearly explained. Third, the loss analysis and comparison in 400-to-12 V, 300 W, 1 MHz LLC resonant converter between Si device and GaN device are discussed. Fourth, a new perspective on the extra transformer winding loss due to the asymmetrical primary side and secondary side current is proposed. The device and design parameters are tied to the winding loss based on the winding loss model in the Finite Element Analysis (FEA) simulation. Finally, in order to verify the GaN device benefits experimentally, 400-to-12 V, 300 W, 1 MHz GaN-based and Si-based LLC converter prototypes are built and tested. 1% efficiency improvement, which is 24.8% loss reduction, is achieved in the GaN-based converter. Test results also show the RMS current and the corresponding dead time in LLC resonant converter to validate the derived relationship. .

3.1 600 V Cascode GaN Device Static and Switching Characteristic

Before the discussion of GaN device application in converter, the device static and switching performance is characterized to obtain some necessary information that support the design and loss analysis, such as on-state resistance, reverse characteristics, blocking capability and switching loss.

Figure 3-1 shows the cascode structure GaN HEMT. A low voltage (LV) Si MOSFET is connected with a high-voltage (HV) normally-on GaN HEMT in the cascode configuration to

make the overall device work as a normally-off device. The cascode structure allows the resulting device to exhibit the benefits of both the LV Si MOSFET and HV GaN HEMT: the LV Si MOSFET provides positive and rugged gate-source voltage and the HV GaN HEMT has high voltage blocking capability and fast switching speed. The HV GaN HEMT is driven by the drain-source voltage of the LV Si MOSFET. The LV Si MOSFET can be directly driven by a traditional gate driver, which also has much smaller driving loss compared with a 600 V Si MOSFET.

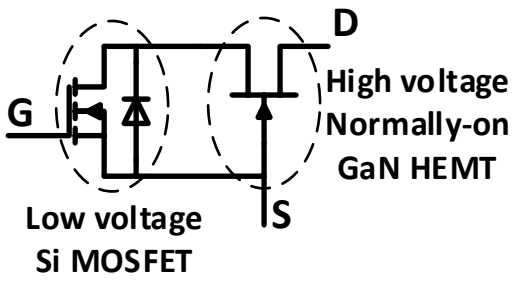
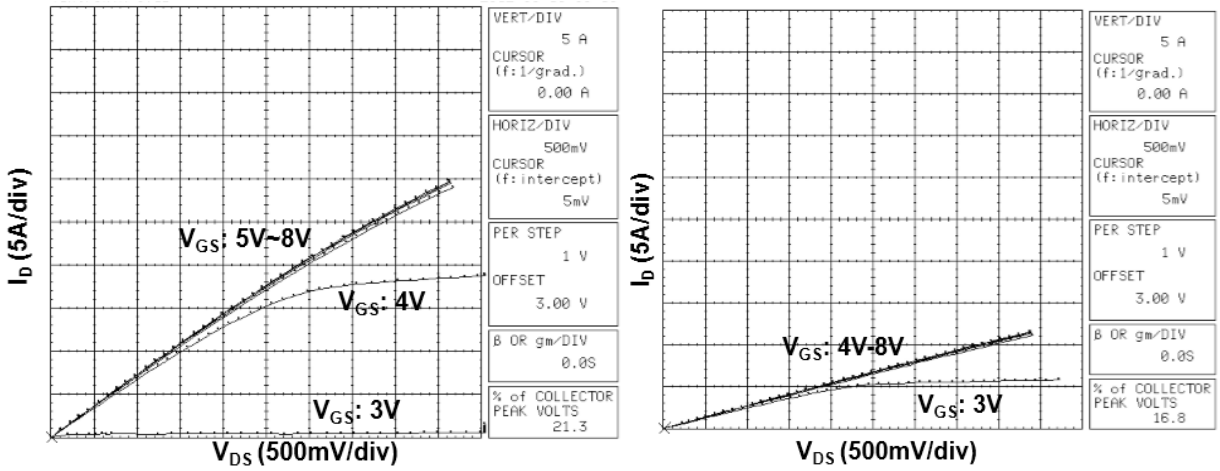


Figure 3-1. Cascode structure GaN HEMT.

3.1.1 Static Characterization

The device output characteristics are tested at different temperatures of the device tab, which are assumed as the junction temperatures due to the ultra-low thermal resistance. Figure 3-2 shows the output characteristics at 25 °C and 200 °C. The gate-source voltage is swept from 3 V to 8 V. When the temperature is higher, the device fully turns on at lower gate-source voltage.

The on-state resistance can be derived from the device output characteristics. Figure 3-3 shows the on-state resistance at different temperature when the gate-source voltage is 5 V as an example.



(a) Output characteristic at 25 °C (b) Output characteristic at 200 °C

Figure 3-2. Output characteristics.

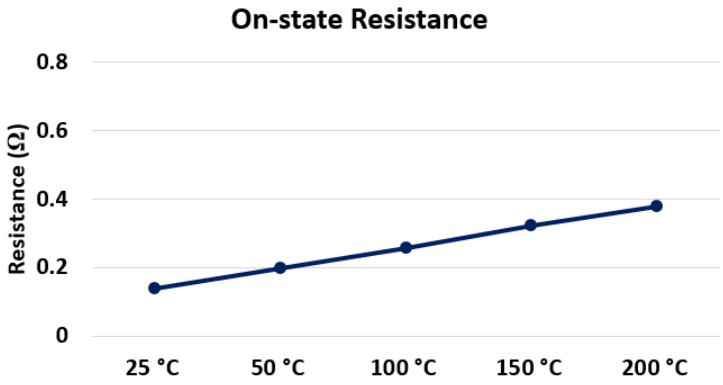
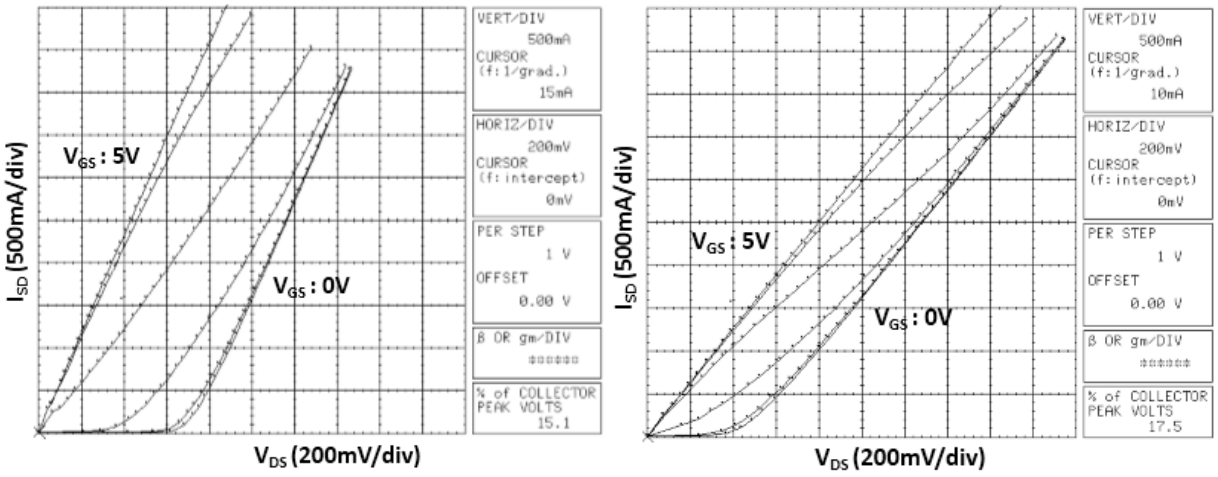


Figure 3-3. On-state resistance vs. temperature.

The reverse characteristics in Figure 3-4 show the forward voltage of the equivalent body diode at different current ratings, when the gate-source voltage is zero. The equivalent body diode is formed by the body diode of the LV Si MOSFET and the channel of the HV normally-on GaN HEMT when the entire cascode device is reverse biased. Besides, when the gate-source voltage is increasing, the device gradually carries the reverse current from source to drain. According to the

test curves, the value of reverse on-state resistance is similar with the on-state resistance derived from the output characteristics at each corresponding temperature. Therefore, when the device is fully turned on, it can be considered as a resistor. On the other hand, the turn-on threshold voltage of the equivalent body diode changes in different temperature, and the forward voltage at 2 A current changes as well, which are shown in Figure 3-5.



(a) Reverse characteristic at 25 °C (b) Reverse characteristic at 200 °C

Figure 3-4. Reverse characteristics.

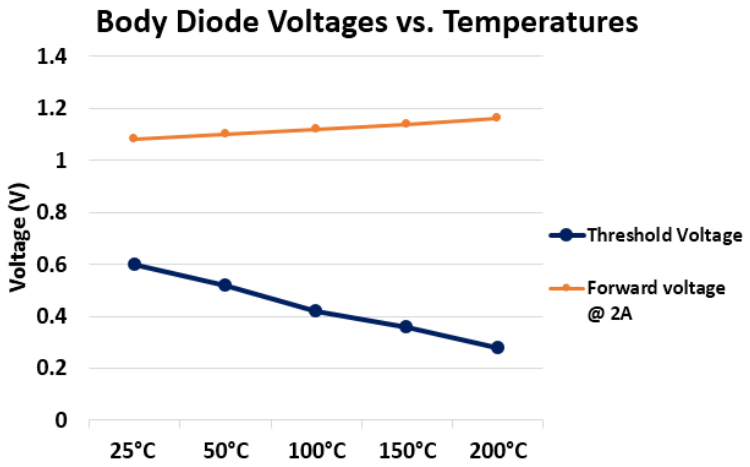
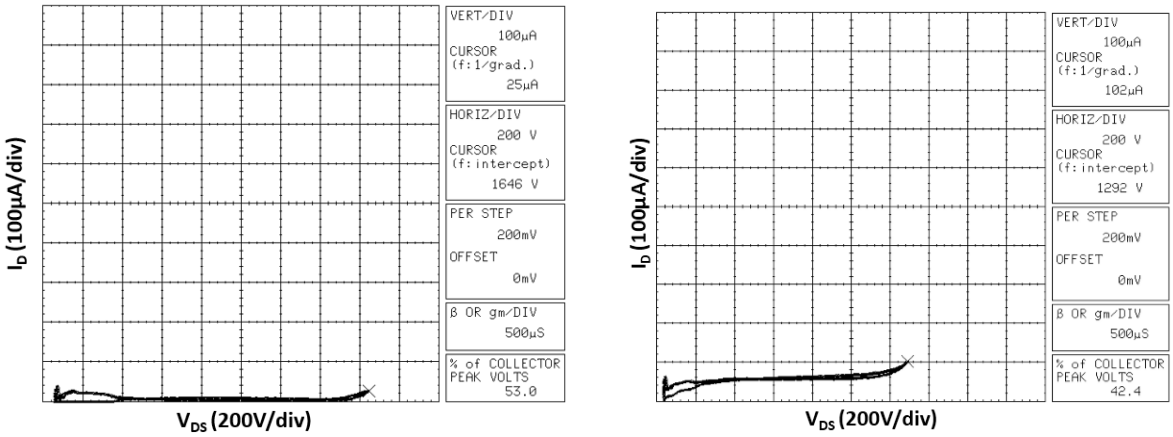


Figure 3-5. Body diode threshold voltage and forward voltage vs. temperatures.

The 600 V cascode GaN HEMT samples show very good voltage blocking capability at 25 ºC. Figure 3-6(a) indicates that the blocking voltage is 1646 V when the leakage current is 25 μA. The results in Figure 3-6(b) were from experiments at 200 ºC. It still has a good voltage blocking capability of 1292 V. 10 devices are tested in order to obtain a more reliable value. The average voltage blocking capability is 1641 V/25 μA at 25 ºC, and 1294 V/102 μA at 200 ºC. In the datasheet of TPH3006PS, the maximum transient drain-source voltage is specified at 750 V (for 1 μs, 0.1 duty cycle). Moreover, since the device voltage is rated at 600 V, the leakage current capability at 600 V is shown in Figure 3-7.



(a) Voltage blocking characteristic at 25 °C (b) Voltage blocking characteristic at 200 °C

Figure 3-6. Voltage blocking characteristics.

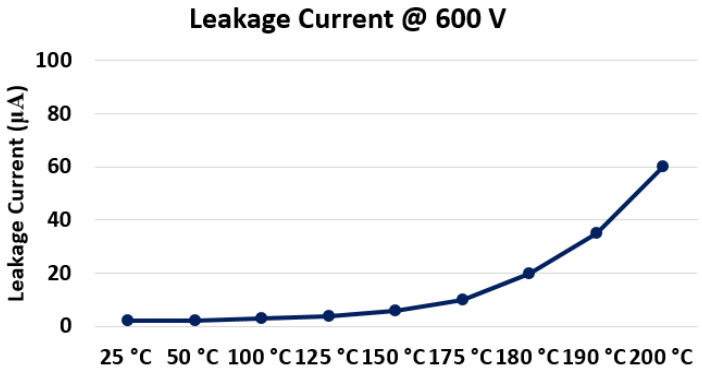


Figure 3-7. Leakage current @ 600 V vs. temperature.

3.1.2 Switching Characterization

A double pulse tester is built to evaluate the switching performance of a cascode GaN HEMT and to provide loss references in the converter design and loss analysis. In the double pulse tester, a SiC Schottky diode is applied as the upper switch, and the gate driver is IXDN609. The schematic is shown in Figure 3-8, and the test setup is shown in Figure 3-9.

Due to the very fast switching speed, a Kelvin connection is necessary to reduce the common source inductance between the gate driver loop and power loop. The cascode GaN HEMT package also provides a source tab to split the gate driver loop and power loop.

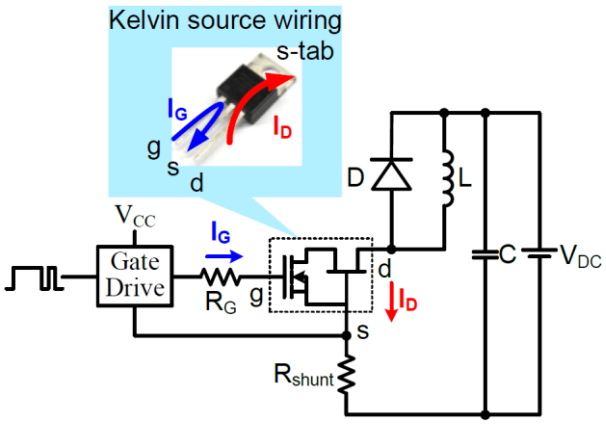


Figure 3-8. Schematic of double pulse tester.

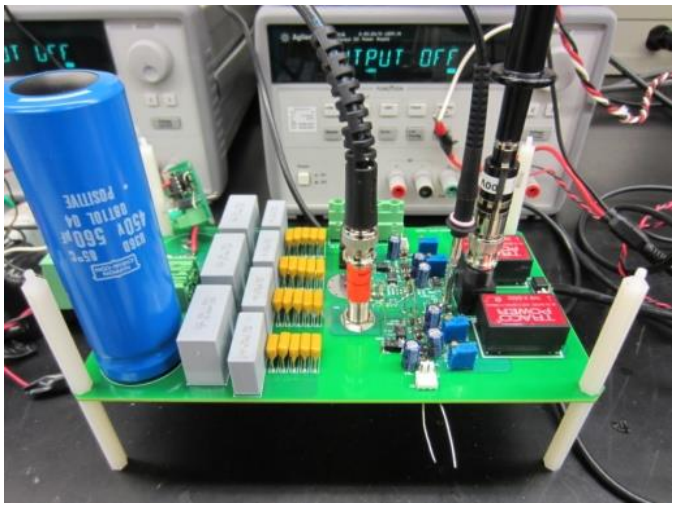


Figure 3-9. Double pulse test setup.

The switching performance of the device-under-test (DUT) is tested with a dc bus voltage of 400 V and a load current of 11 A. Figure 3-10 shows the turn-on switching transient using the gate voltage of 0 V / 13.5 V and the gate resistance of 0 Ω to push the switching speed. For the turn on transient, the dv/dt reaches 140 V/ns, and the di/dt reaches 9.6 A/ns. For the turn off transient, shown in Figure 3-11, the dv/dt reaches 42 V/ns, and the di/dt reaches 2.4 A/ns. The turn off switching speed is slower than turn on switching speed because the DUT junction capacitance needs to be charged by the inductor current during turn off. The turn on switching energy is 4.3 µJ, and the turn off switching energy is 8.1 µJ.

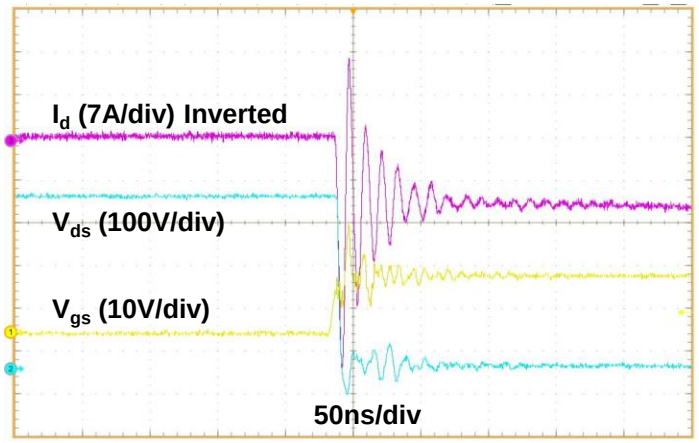


Figure 3-10. Turn-on switching waveforms.

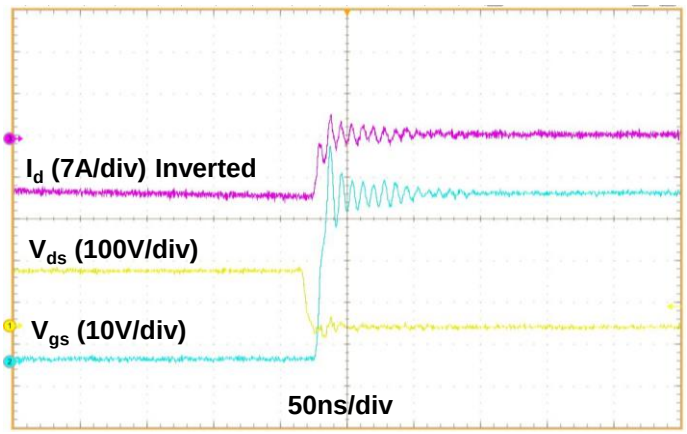


Figure 3-11. Turn-off switching waveforms.

The DUT is also tested with various gate source voltage V_{gs} and gate resistance R_g under the same voltage and current conditions. Figure 3-12 and Figure 3-13 show the measured turn-on and turn-off switching energy with various V_{gs} and R_g. The switching speed can be reduced with smaller V_{gs} or larger R_g to compromise for the circuit limitations (e.g. isolator dv/dt immunity in a phase leg configuration, gate ringing caused by di/dt on common source inductance), but the switching energy is increased accordingly. The real turn-off energy in the soft-switching is derived by the measured turn-off energy minus the output capacitance energy in the datasheet.

Based on the device static and switching performance characterization, necessary data, such as on-state resistance, reverse characteristics, blocking capability and switching loss are obtain for the next step design and loss comparisons.

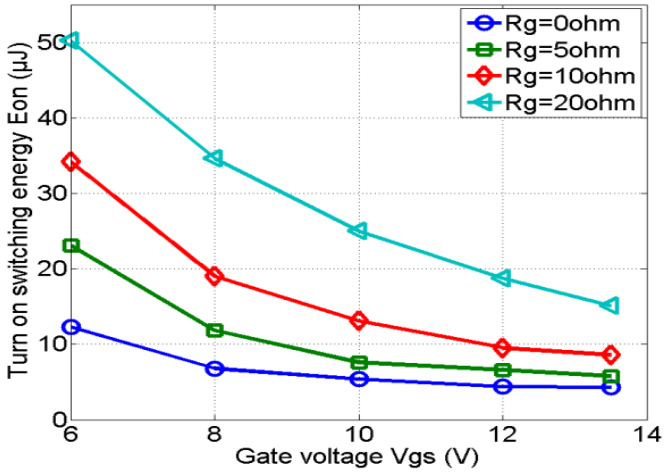


Figure 3-12. Turn-on switching energy.

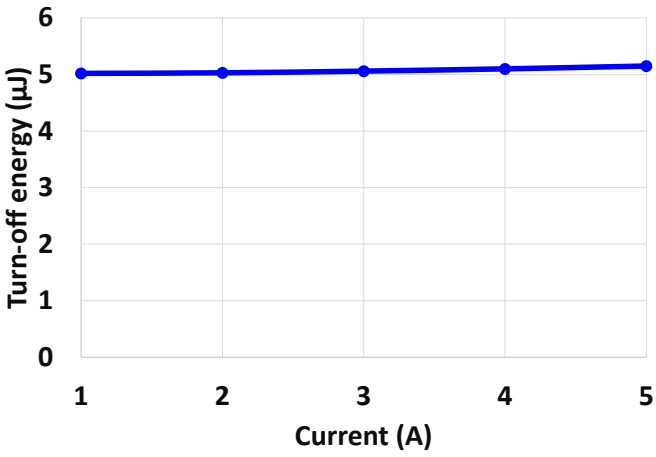


Figure 3-13. Turn-off switching energy.

3.2 Analytical Loss Model of LLC Resonant Converter at Resonance

The LLC resonant converter operating at resonance realizes high efficiency at high frequency due to the soft-switching of both primary side and secondary side devices. Since the voltage gain is equal to 1, it is widely applied as DC-DC transformer (DCX) with voltage ratio determined by

the transformer turns ratio. For the high frequency DCX LLC resonant converter, the primary side device loss mainly includes conduction loss, driving loss and turn-off loss, while the secondary mainly consists of conduction loss and driving loss. Among these loss components, the conduction loss is the dominant. This section first establishes the relation of the device and converter design parameters to the converter RMS current in order to evaluate the impact of those parameters on device conduction loss. After that, different GaN and Si devices are compared by using the established relations as a general example. Finally, the specific GaN and Si devices are selected with the optimal loss. The GaN device loss benefits are quantified.

The half bridge LLC resonant converter topology is shown in Figure 3-14, and the primary side waveforms at the resonant point are shown in Figure 3-15. During the dead time (t_1 to t_2), the resonant current is equal to the peak magnetizing current. The peak magnetizing current discharges the output capacitance of Q2 and then voltage at the switching node *a* drops to zero. After that, Q2 turns on to realize ZVS.

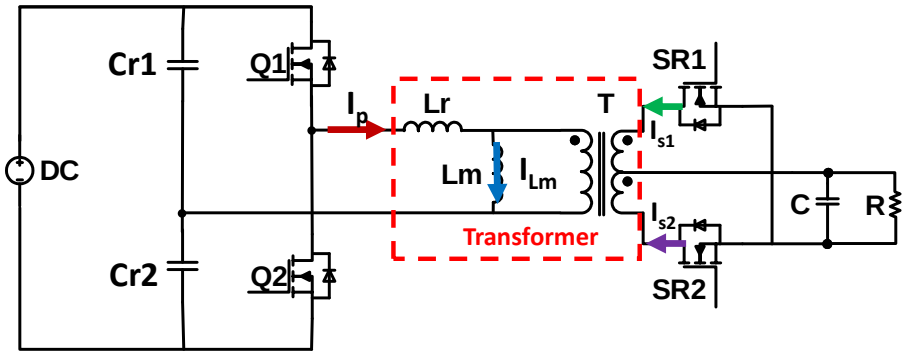


Figure 3-14. LLC resonant converter topology.

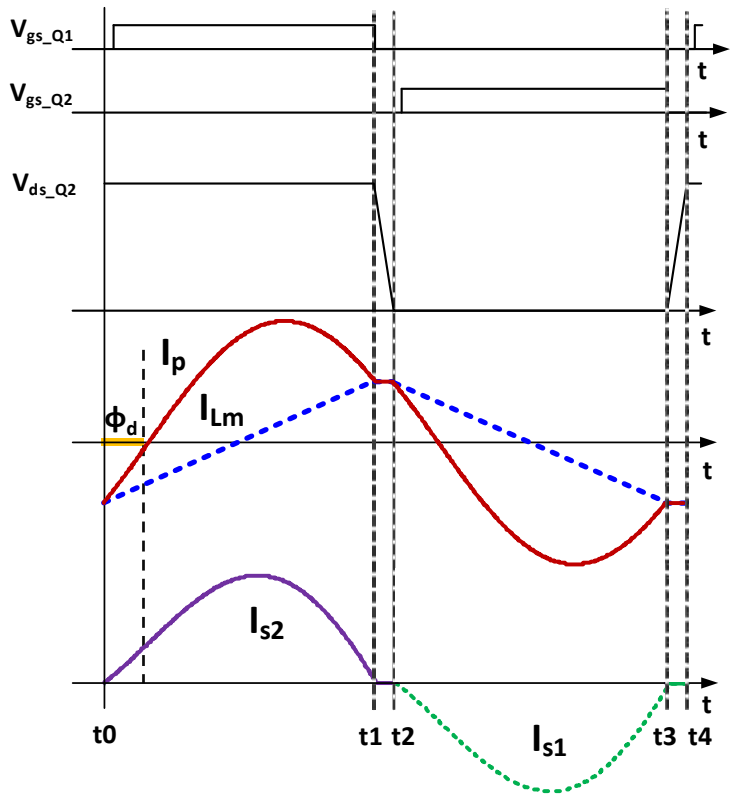


Figure 3-15. Primary side waveforms at resonance.

In order to guarantee ZVS of the devices, sufficient peak magnetizing current and dead time are needed to ensure that all the parasitic capacitances are discharged, including the output capacitance of the primary side devices, the output capacitance of the SR devices, and the transformer winding capacitance. During the dead time (t_1 to t_2), since the magnetizing inductance is large, it can be approximated as a current source. For the primary side half bridge topology, the devices ZVS process is described by the charge balance equation

$$i_{Lm\_pk}T_d = 2C_{pri\_oss}V_{in} + C_w * V_{in} + \frac{1}{N}2nC_{sec\_oss} * 2V_o \qquad (3\text{-}1)$$

where I_{Lm_pk} is the peak magnetizing current; T_d is the dead time; C_{pri_oss} is the primary device effective output capacitance; C_{sec_oss} is the secondary side device effective output capacitance; C_w

is the transformer winding capacitance; n is the number of SR devices in parallel; N is the transformer turns ratio; V_{in} is the input voltage; V_o is the output voltage. The transformer turn ratio is approximately considered as

$$N = \frac{\frac{V_{in}}{2}}{V_o} \tag{3-2}$$

According to the LLC topology in Figure 3-14, the voltage across the magnetizing inductance is the primary side voltage of the ideal transformer, which is equal to NV_o. Considering t_0 to t_1 in Figure 3-15, the peak magnetizing current is expressed as

$$i_{Lm\_pk} = \frac{NV_o\left(\frac{T_s}{2} - T_d\right)}{2L_m} \tag{3-3}$$

By combining (3-1) and (3-3), the magnetizing inductance is expressed in (3-4), which relates the device output capacitance, the transformer winding capacitance, the dead time, and the switching period.

$$L_m = \frac{T_d\left(\frac{T_s}{2} - T_d\right)}{4\left(2C_{pri\_oss} + \frac{1}{N^2} * 4nC_{sec\_oss} + C_w\right)} \tag{3-4}$$

where L_m is the magnetizing inductance and T_s is the switching time period.

The secondary side current I_{s1} or I_{s2} in Figure 3-15 is equal to the primary side current I_p minus the magnetizing current I_{Lm}. The average rectified current on the secondary side is the load current, therefore considering the half switching time period and the dead time we have

$$N \cdot \frac{2}{T_s} \int_0^{\frac{T_s}{2} - T_d} (I_p - I_{Lm})\, dt = \frac{V_o}{R_L} \tag{3-5}$$

$$I_p = \begin{cases} \sqrt{2} I_{RMS\_P} sin(\omega_0 t - \Phi_d) & (0 < t < \frac{T_s}{2} - T_d) \\ I_{Lm\_pk} & (\frac{T_s}{2} - T_d < t < \frac{T_s}{2}) \end{cases} \tag{3-6}$$

$$I_{Lm} = \begin{cases} -I_{Lm\_pk} + \frac{NV_o}{L_m} t & (0 < t < \frac{T_s}{2} - T_d) \\ I_{Lm\_pk} & (\frac{T_s}{2} - T_d < t < \frac{T_s}{2}) \end{cases} \quad (3\text{-}7)$$

The primary side sinusoidal RMS current at resonance is derived based on the above equations as

$$I_{RMS\_P} = \sqrt{\frac{V_0^2 \pi^2 T_s^2}{8 R_L^2 N^2 (T_s - 2T_d)^2} + \frac{1}{2} I_{Lm\_pk}^2} \quad (3\text{-}8)$$

Adding the magnetizing current during the dead time, the total primary side RMS current can be expressed as

$$I_{RMS\_P\_total} = \sqrt{\frac{V_0^2 \pi^2 T_s^2}{8 R_L^2 N^2 (T_s - 2T_d)^2} + (\frac{1}{2} + \frac{2T_d}{T_s}) I_{Lm\_pk}^2} \quad (3\text{-}9)$$

The secondary side RMS current at resonance is calculated based on the RMS current definition which is expressed as

$$I_{RMS\_S\_total} = \sqrt{\frac{1}{T_s} \int_0^{\frac{T_s}{2} - T_d} ((I_p - I_{Lm}) \cdot N)^2 dt} \quad (3\text{-}10)$$

Solving (3-10), the secondary side RMS current is derived as

$$I_{RMS\_S\_total} = N \sqrt{\frac{T_s - 2T_d}{2T_s} [I_{RMS\_P}^2 + (\frac{1}{3} - \frac{8}{\pi^2}) I_{Lm\_pk}^2]} \quad (3\text{-}11)$$

From (3-9) and (3-11), the dead time and the peak magnetizing current impact both primary and secondary side RMS current. Under the predetermined converter specifications and switching frequency, one tradeoff in the design of LLC resonant converter is between the dead time and the peak magnetizing current. As is shown in (3-1), sufficient peak magnetizing current is necessary to achieve device ZVS turn-on during the dead time. However, magnetizing current is the circulating current in the primary side of converter which brings additional loss. High peak magnetizing current induces high RMS current leading to high device conduction loss and high

transformer winding loss, especially at light load or no load condition. Large dead time is not preferable as well, since large dead time results in smaller effective energy transfer time from input to load, which increases the RMS current at full load. Therefore, low peak magnetizing current and small dead time are preferable. That means the overall device capacitance participating in the resonance during the dead time is necessary to be small. In order to have a quantified relations directly between the device and RMS current, (3-9) or (3-11) is combined with (3-1) to get

$$I_{RMS\_P\_total} = \sqrt{\frac{V_0^2\pi^2T_s^2}{8R_L^2N^2(T_s-2T_d)^2} + (\frac{1}{2}+\frac{2T_d}{T_s})(\frac{2C_{pri\_oss}V_{in}+C_wV_{in}+\frac{1}{N}2nC_{sec\_oss}*2V_o}{T_d})^2} \quad (3\text{-}12)$$

$$I_{RMS\_S\_total} = N\sqrt{\frac{T_s-2T_d}{2T_s}[\frac{V_0^2\pi^2T_s^2}{8R_L^2N^2(T_s-2T_d)^2} + (\frac{5}{6}-\frac{8}{\pi^2})(\frac{2C_{pri\_oss}V_{in}+C_wV_{in}+\frac{1}{N}2nC_{sec\_oss}*2V_o}{T_d})^2]} \quad (3\text{-}13)$$

where R_L is the load resistance; $I_{RMS\_P\_total}$ is the primary side total RMS current through the L_r shown in Figure 3-14; $I_{RMS\_S\_total}$ is the secondary side total RMS current through SR1 (or SR2) shown in Figure 3-14. From (3-12) and (3-13), the relation of the device and design parameters to the converter RMS current is established.

In LLC resonant converter, since the conduction loss is dominant in the device total loss due to the soft-switching, it is preferable to select devices with low on-state resistance to achieve low conduction loss. However, under the same device structure and blocking voltage, low on-state resistance usually means large die size and high output capacitance. According to (3-1), (3-12) and (3-13), high output capacitance requires high peak magnetizing current and large dead time which ultimately brings high RMS current. Consequently, both the on-state resistance and output capacitance have direct impacts on the device conduction loss, which is different from the hard-switching converter that the on-state resistance and output capacitance compromise between the conduction loss and switching loss. Because of the high figure-of-merit, i.e. demonstrating a lower

output capacitance for the similar on-resistance with Si devices, GaN devices have the potential to outperform Si devices in the LLC resonant converter.

3.3 Device Parameters Impact and GaN Device Benefits in LLC Resonant Converter

Based on the relations developed previously, the GaN HEMTs and Si MOSFETs are respectively applied in the two LLC resonant converters with the same specifications shown in Table 3-1.

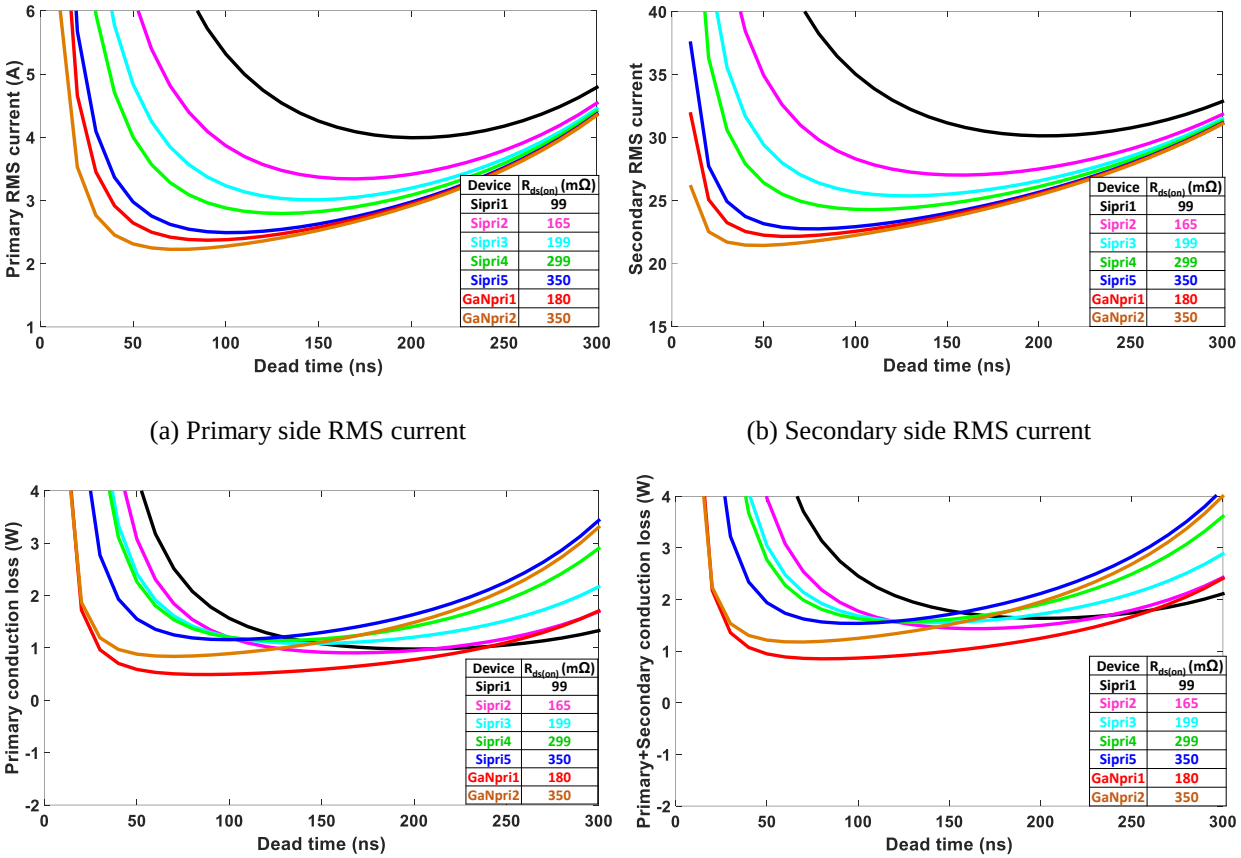
Table 3-1. LLC converter specifications

Power Rating	300 W
Input Voltage	400 VDC
Minimum Input Voltage (with AC mains off)	300 VDC
Output Voltage	12 VDC
Switching frequency	1 MHz

600 V GaN HEMT and Si CoolMOS are selected for the primary side devices; 40 V eGaN FET and Si OptiMOS are selected as the secondary side devices. In order to have a fair comparison between GaN and Si, the device parameters need to be carefully selected. The on-state resistances are selected at the same junction temperatures and certain gate-source voltages from the datasheet. Since the device output capacitance has the nonlinear characteristic, according to (3-1), the charge equivalent capacitance can be applied in the equations. The primary side equivalent output capacitance C_{pri_oss} is derived from the total charge divided by 400 V. The total charge is obtained from the integral of the nonlinear output capacitance curve from 0 V to 400 V. The secondary side equivalent output capacitance C_{sec_oss} is derived at 24 V in the same approach.

In order to investigate how the device output capacitance impacts device loss, the established relations in (3-12) and (3-13) are utilized. Assuming the selection of secondary side devices is fixed, the primary and secondary side RMS current versus the dead time based on (3-12) and (3-13) are plotted in Figure 3-16(a) and Figure 3-16(b) with different Si and GaN devices. From *Sipri1* to *GaNpri2*, the charge equivalent output capacitances decrease monotonically while the on-state resistances increase significantly either for Si or GaN devices. The minimum RMS currents and the corresponding dead times decrease along with the output capacitances. Further, the conduction loss curves for the primary side devices are shown in Figure 3-16(c). Comparing *Sipri5* with *GaNpri1* which have the similar equivalent output capacitances, the *GaNpri1* demonstrates almost half of the conduction loss of *Sipri5*. For the devices that have similar on-state resistances, e.g. *Sipri4* and *GaNpri2*, the GaN device still shows lower conduction loss than the Si device at the minimum loss point due to lower RMS current shown in Figure 3-16(a). Besides, as can be seen in Figure 3-16(c), the GaN devices earn the benefits because of the low RMS current caused by ultra-low output capacitances in the range that the dead time is below 250 ns. When it goes higher, the on-state resistance starts to take over. Finally, one issue in the design using (3-12) and (3-13) is that it is not straightforward to determine the optimal dead time from Figure 3-16(a) and Figure 3-16(b) directly, as the optimal dead times change. For example, when applying *GaNpri2*, the converter can achieve minimum primary RMS current at 70 ns whereas minimum secondary RMS current at 50 ns. Therefore, the optimal dead time determination requires the consideration of overall device conduction loss. The secondary side devices applied in this example are BSC027N04LS. It is selected due to its low on-state resistance without consideration the output capacitance impact. The combined primary and secondary side device conduction loss are shown in Figure 3-16(d). The optimal dead times are close to those in Figure

3-16(c). The reason is that the secondary side device loss is much lower than the primary side and the impact on the dead time is still dominated by the primary side.



(a) Primary side RMS current

(b) Secondary side RMS current

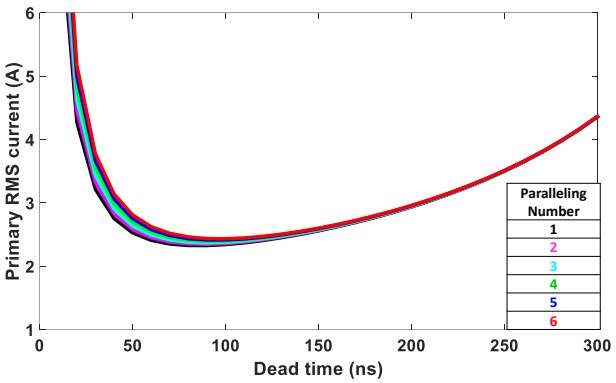
(c) Primary side device conduction loss

(d) Primary side+Secondary side device conduction loss

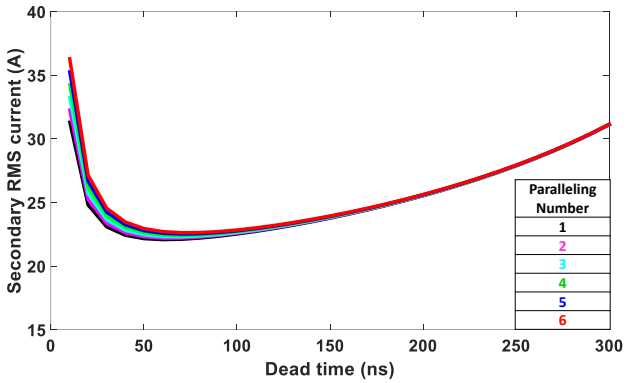
Figure 3-16. RMS current and conduction loss versus dead time for different primary side devices.

In the example shown above, the secondary side devices are predetermined in order to show the impact of the primary side devices and select the ones with lowest loss. To achieve the high efficiency requirement, secondary side device selection and the number of device in parallel also need to be optimized. Based on the example above, there are seven different primary side devices

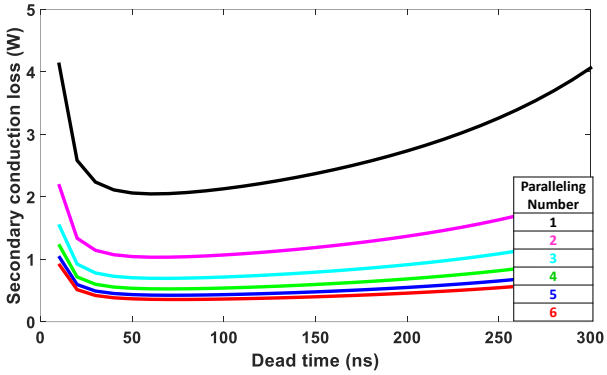
in total resulting seven curves either in RMS current or conduction loss. If four different secondary side devices are considered and the number of device in parallel is from one to six, there will be more than one hundred cases need to study which is complicated. Therefore, a study on how the secondary side device impact the converter RMS current is necessary. In (3-12) and (3-13), the $C_{sec\_oss} \cdot 2V_o$ is multiplied by the number of device in parallel n and divided by the transformer turns ratio N. Since N is large in a 400 V-12 V converter, the impact of secondary side device is reduced. For example, based on the datasheet, the equivalent charge of primary side 199 mΩ device at 400 V is 131 nC, and it is 44 nC for one secondary side device. By having four secondary side devices in parallel, the total charge moving during the dead time is 22 nC, while the primary side has 262 nC. The output charge is much less for the secondary side than the primary side. Figure 3-17(a) illustrates the variations of primary and secondary RMS currents along with the secondary side device in parallel when the primary side devices are fixed. The current difference is smaller than 0.4 A and 2 A respectively. Although Figure 3-17(a) and Figure 3-17(b) only show the case of device paralleling, the fundamental reason for the small current variation is due to the high transformer turns ratio that reduces the impact of the secondary side output capacitance. Thus, if other devices are considered in the design, the results are similar. It seems that the more devices in parallel the smaller device loss since the currents keep almost the same. However the driving loss is the main constrain on the number of the paralleling devices as shown in Figure 3-17(c). Thus, the secondary side device output capacitances have small impact on the RMS current when the transformer turns ratio is high in 400 V-12 V converter. The loss analysis and optimization process can be simplified, as the driving loss is the main constraint on the secondary side device loss.



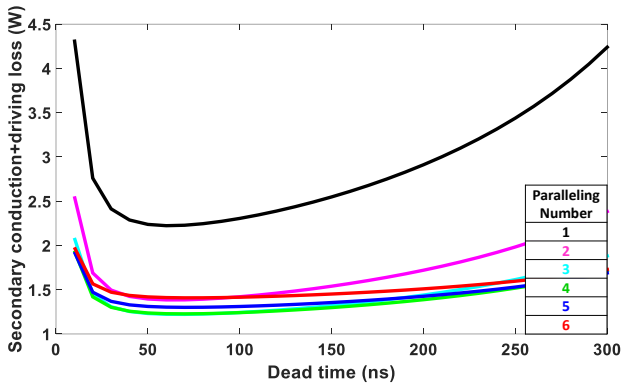
(a) Primary side RMS current



(b) Secondary side RMS current



(c) Secondary side device conduction loss



(b) Secondary side device conduction loss+driving loss

Figure 3-17. RMS current and conduction loss versus dead time for secondary side devices in parallel.

After the general example analysis is presented above, it is necessary to quantify the GaN benefits by comparing the specific GaN and Si devices in LLC resonant converters. By applying the analysis approach shown above, the devices achieving lowest loss are selected, and four devices in parallel are chosen for the secondary side. The device key parameters are shown in Table 3-2 and Table 3-3. In the following comparison, the device total loss including the conduction loss, driving loss and turn-off loss will be considered.

Table 3-2. Primary side Si and GaN devices based on datasheet

Primary device	Voltage rating (V)	$R_{ds(on)}$ (mΩ) @25 °C/50 °C	Charge equivalent output capacitance (pF)	Gate charge (nC)
IPP60R199CP (Si)	600	180/225 @10V	327 @400V	33 @10V
TPH3006PS (GaN)	600	150/178 @8V	115 @400V	11 @8V

Table 3-3. Secondary side Si and GaN devices based on datasheet

Secondary device	Voltage rating (V)	$R_{ds(on)}$ (mΩ) @25 °C/50 °C	Output charge (nC)	Gate charge (nC)
BSC027N04LS (Si)	40	2.9/3.2 @5V	43@25V	25
EPC2015 (GaN)	40	3.2/3.6 @5V	23@25V	9.5

The primary side and secondary side RMS current for the selected GaN and Si devices are plotted in Figure 3-18. As shown in Figure 3-18, the minimum primary side RMS current for the Si-based design occurs at 130 ns, while the minimum for the GaN-based design is at 80 ns. Figure 3-19 shows the secondary side RMS current through each device. For the Si design, the minimum RMS current is at 130 ns dead time, while the GaN design shows 70 ns. Since the RMS current change between 70 ns and 80 ns is small in both primary side and secondary side devices, the 80 ns is selected as the optimal dead time in the design.

The device loss breakdowns and comparison are shown in Figure 3-20 and Figure 3-21. The primary side device loss includes conduction loss, turn-off loss and driving loss. The conduction loss is dominant. For the secondary side devices, since the gate driving signal is tuned with the primary side gate driving signal in converter at resonance, theoretically, there is no body diode forward conduction loss and device turn-off loss. The total loss is dominated by conduction loss and driving loss. According to results, the GaN device loss demonstrates around 50% reduction compared with the Si device.

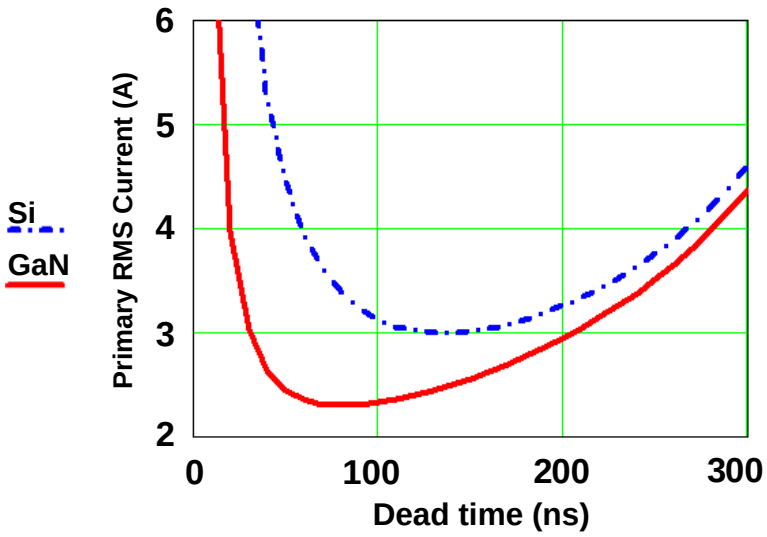


Figure 3-18. Primary side loss comparison.

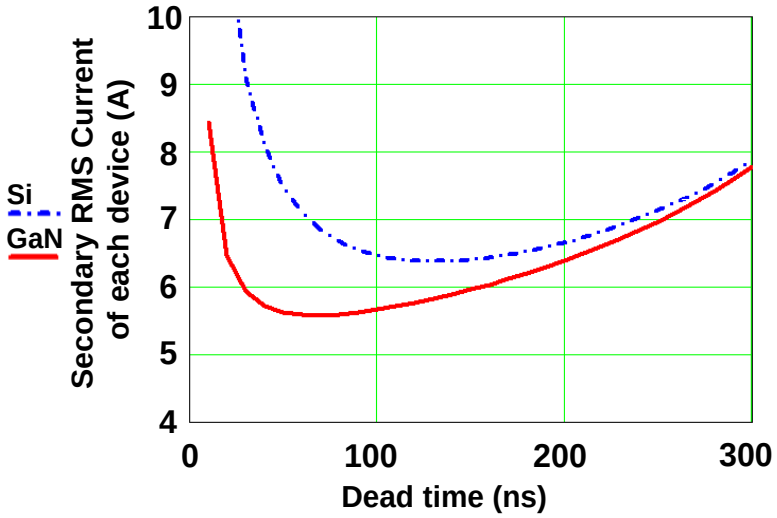


Figure 3-19. Secondary side loss comparison.

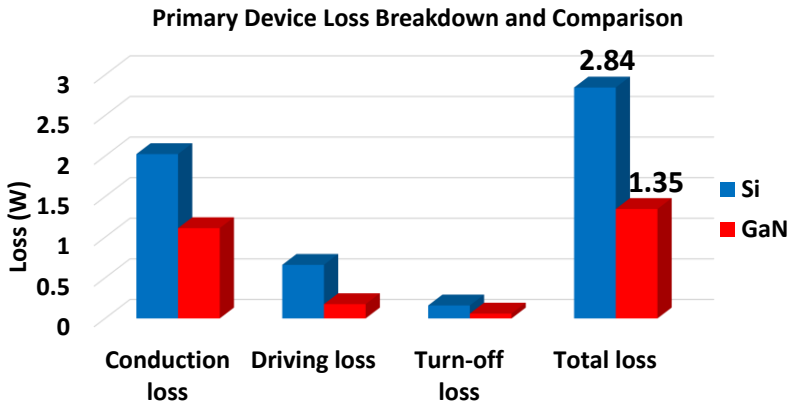


Figure 3-20. Primary device loss breakdown and comparison.

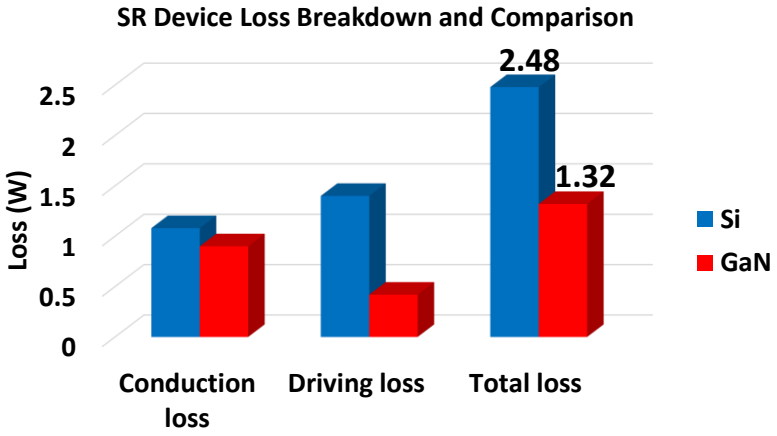


Figure 3-21. Secondary device loss breakdown and comparison.

The impact of primary side devices paralleling will be analyzed as well. Device paralleling results in the increase of primary side output capacitance, which has more impact to the RMS current than the secondary output capacitance based on (3-10) and (3-11).

Figure 3-22 and Figure 3-23 illustrate the primary and secondary side RMS currents versus the dead time with two primary side devices in parallel for both GaN and Si designs. The primary

and secondary side loss breakdown and comparison with two primary devices in parallel are shown in Figure 3-24 and Figure 3-25. The conduction loss reduction of the Si design compared with the one in Figure 3-20 is very small. The reason is that although the equivalent on-state resistance is reduced by half, the RMS current increases. Since it is even lower than the increases of driving loss and turn-off loss, the total loss for the primary side devices with two in parallel increases by 0.58 W in the Si design. For the GaN design, the total primary side devices loss decreases by 0.2 W, which still show benefits to the Si design. However when more than two GaN devices are paralleled in this example, the total loss will increase, shown in Figure 26. The reduction of conduction loss is even smaller due to the increase of RMS current.

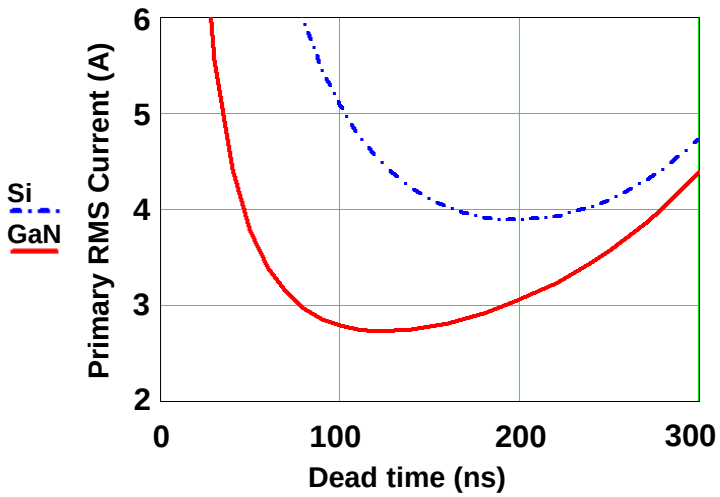


Figure 3-22. Primary side loss comparison with two primary side device in parallel.

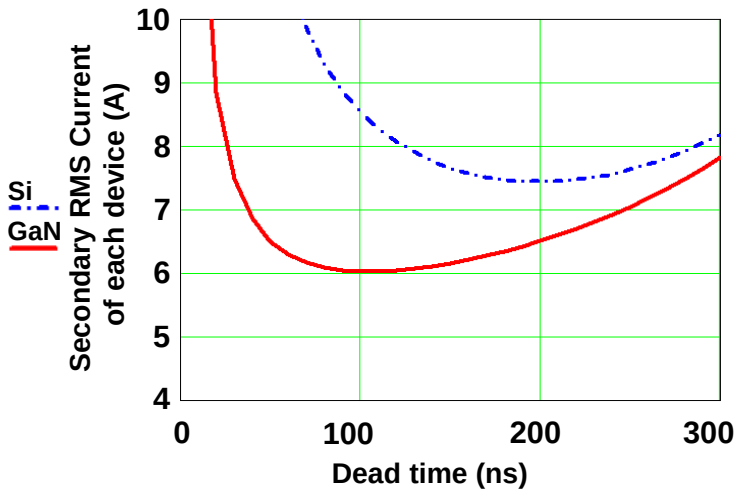


Figure 3-23. Secondary side loss comparison with two primary side device in parallel.

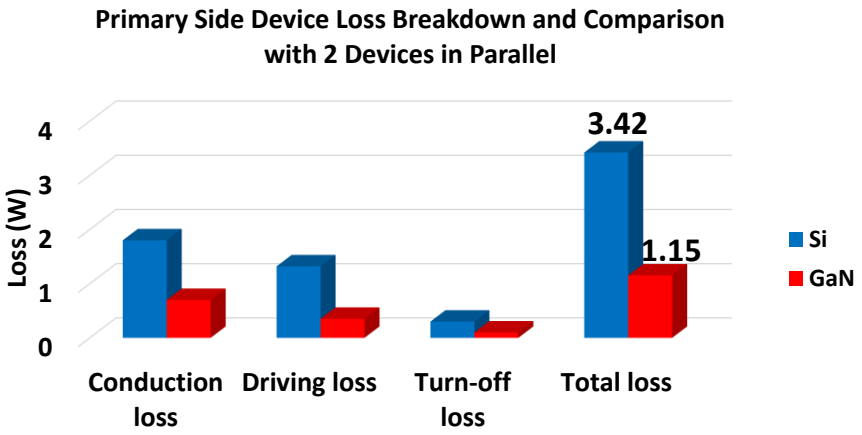


Figure 3-24. Primary device loss breakdown and comparison with two device in parallel.

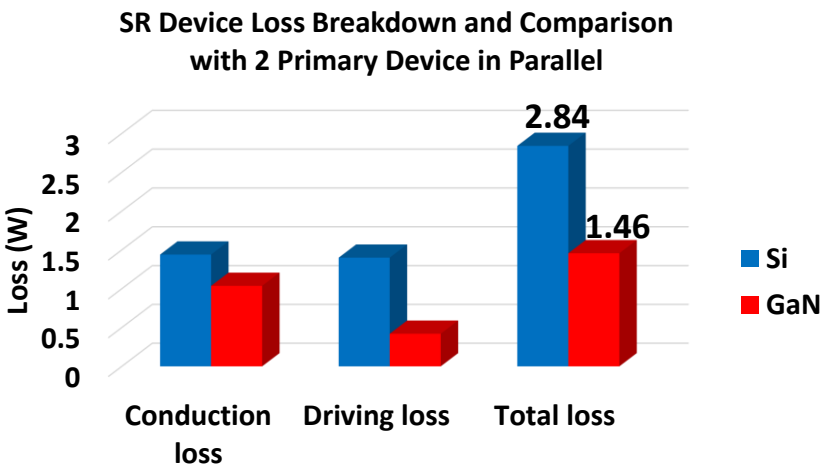


Figure 3-25. Secondary device loss breakdown and comparison with two device in parallel.

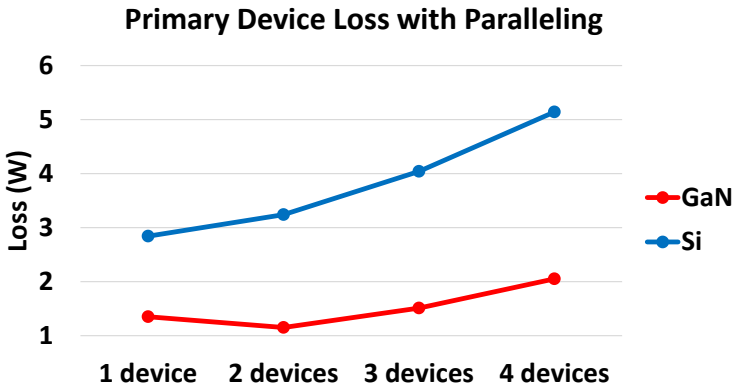


Figure 3-26. Primary device loss vs. the number of device in parallel.

3.4 An Improved Device Selection Approach for LLC Resonant Converter

A device selection approach for LLC resonant converter has been proposed in [37], which is reviewed in Section 2.1.1. Owing to ZVS operation of LLC resonant converters, the turn-on loss of MOSFETs is eliminated. Thus, the turn-off loss, gate-driving loss and conduction loss have been considered. However, the impact of device parameters on converter RMS current has not

been considered in that approach. Therefore, it is too general to consider the constant current I_o in (3-14). An improved device selection approach considering the device output capacitance is discussed in this section.

In the LLC resonant converter, the primary side device loss expressed in [37] is

$$P_{loss} = \frac{V_{in} I_{off}}{2} \frac{(Q_{gd}+Q_{gs2})R_g}{V_{plt}} f_s + \frac{I_0^2}{N^2} \frac{\pi^2}{4} R_{on} + Q_g V_{gs} f_s \tag{3-14}$$

where V_{in} is the input voltage; I_{off} is the turn-off current; Q_{gd} is the gate-drain charge; Q_{gs2} is the partial gate-source charge, which can be found on the datasheet; R_g is the gate resistance; V_{plt} is the miller plateau voltage; f_s is the switching frequency; I_o is the output current; N is the transformer turns ratio; R_{on} is device on-state resistance; Q_g is the gate charge; V_{gs} is the gate-source voltage. Considering the device output capacitance impact as shown in (3-12) and (3-13), and the turn-off loss dissipated in the device channel, (3-14) can be expressed as,

$$P_{loss} = \left(\frac{V_{in} I_{off}}{2} \frac{(Q_{gd}+Q_{gs2})R_g}{V_{plt}} - \frac{1}{2} Q_{oss_E} V_{in}\right) f_s + \left(\frac{V_0^2 \pi^2 T_s^2}{8 R_L^2 N^2 (T_s - 2T_d)^2} + \left(\frac{1}{2} + \frac{2T_d}{T_s}\right)\left(\frac{2Q_{pri\_oss} + Q_w + \frac{1}{N} 4n Q_{sec\_oss}}{T_d}\right)^2\right) R_{on} + Q_g V_{gs} f_s \tag{3-15}$$

where Q_{ossE} is the energy equivalent output charge; Q_{pri_oss} is the primary side equivalent charge; Q_{sec_oss} is the secondary side equivalent charge; Q_w is the equivalent winding charge.

In the previous proposed device selection approach, i.e. figure-of-merit (FOM), a power MOSFET die is treated as a composition of several thousands of elementary cells [80]. Based on the cell structure assumption, it can be concluded that for a given MOSFET a large number of elementary cells are paralleled inside. Paralleling more elementary cells would achieve a smaller R_{dson} value but a larger gate charge, which satisfy the following relationship:

$$R_{dson} = \frac{R_{dson\_sp}}{N_{cell}} \tag{3-16}$$

$$Q_g = Q_{g\_sp} N_{cell} \tag{3-17}$$

where R_{dson_sp} and Q_{g_sp} are the specific on-state resistance and specific gate charge. Other equivalent charges in (3-15) have the same form in (3-17). Substitute (3-16) and (3-17) to (3-15), we have.

$$P_{loss}(N_{cell}) = \left(\frac{V_{in} I_{off}}{2} \frac{(Q_{gd\_sp} + Q_{gs2\_sp}) R_g}{V_{plt}} - \frac{1}{2} Q_{ossE\_sp} V_{in}\right) N_{cell} f_s + \left(\frac{V_0^2 \pi^2 T_s^2}{8 R_L^2 N^2 (T_s - 2T_d)^2} + \left(\frac{1}{2} + \frac{2T_d}{T_s}\right)\left(\frac{2Q_{pri\_oss\_sp} N_{cell} + Q_w + \frac{1}{N} 4n Q_{sec\_oss\_sp} N_{cell}}{T_d}\right)^2\right) \frac{R_{on\_sp}}{N_{cell}} + Q_g N_{cell} V_{gs} f_s \tag{3-18}$$

The switching related loss increases along with the increase of N_{cell} and the conduction related loss decreases along with the increase of N_{cell}. Therefore, when

$$\frac{dP_{loss}(N_{cell})}{dN_{cell}} = 0 \tag{3-19}$$

The minimum loss P_{loss_min} can be derived.

However, the derived equation for P_{loss_min} is very complicated and not practical for design. In order to simplify the equation, some non-dominant parts can be cancelled. For the cascode GaN devices, the turn-off loss dissipation in the channel is negligible because of the internal cascode structure mechanism [105], especially when the external turn-off resistance is close to zero. For the Si MOSFET, the turn-off loss is also very low when the external turn-off resistance is small. Figure 3-27 illustrates the turn-off loss percentage of the conduction loss at 1 Ω turn-off resistance. The turn-off loss is only 8% of the conduction loss at the optimum point. Besides, the winding charge is assumed constant in the device selection.

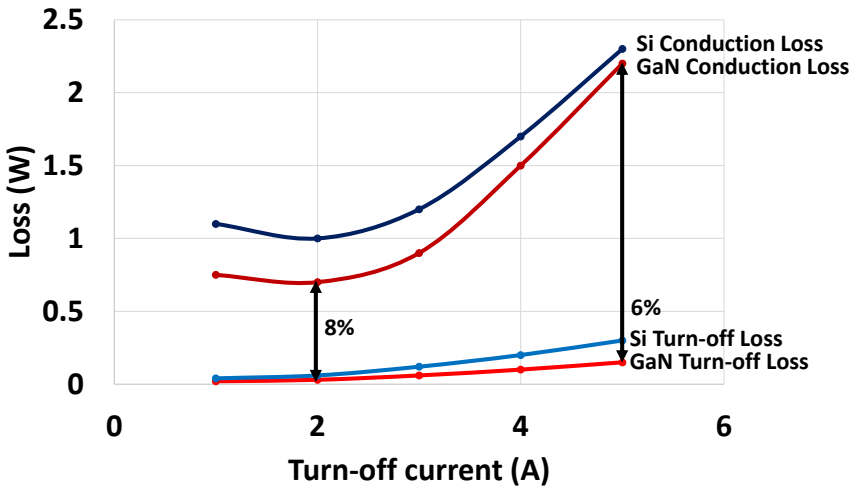


Figure 3-27. Turn-off loss percentage of conduction loss.

Therefore, (3-18) is simplified as,

$$P_{loss}(N_{cell}) = \left(\frac{V_0^2\pi^2T_s^2}{8R_L^2N^2(T_s-2T_d)^2} + \left(\frac{1}{2}+\frac{2T_d}{T_s}\right)\left(\frac{2Q_{pri\_oss\_sp}N_{cell}+\frac{1}{N}4nQ_{sec\_oss\_sp}N_{cell}}{T_d}\right)^2\right)\frac{R_{on\_sp}}{N_{cell}} + Q_gN_{cell}V_{gs}f_s \tag{3-20}$$

Calculate (3-19), N_{cell_min} and $P_{loss\_min\_sp}$ can be derived as,

$$N_{cell} = T_d\left(\frac{K_1R_{on\_sp}}{K_2R_{on_{sp}}\left(2Q_{pri\_oss\_sp}+\frac{4n}{N}Q_{sec\_oss\_sp}\right)^2+Q_{g\_sp}V_{gs}f_sT_d^2}\right)^{\frac{1}{2}} \tag{3-21}$$

$$P_{loss\_\min\_sp} = \frac{2}{T_d}\left\{K_1R_{on\_sp}\left[K_2R_{on\_sp}\left(2Q_{pri\_oss\_sp}+\frac{4n}{N}Q_{sec\_oss\_sp}\right)^2+Q_{g\_sp}V_{gs}f_sT_d^2\right]\right\}^{\frac{1}{2}} \tag{3-22}$$

$$K_1 = \frac{V_0^2\pi^2T_s^2}{8R_L^2N^2(T_s-2T_d)^2} \tag{3-23}$$

$$K_2 = \frac{1}{2}+\frac{2T_d}{T_s} \tag{3-24}$$

Substitute (3-16) and (3-17) back to (3-22), we have the minimum loss in terms of the device on-state resistance and equivalent charges.

$$P_{loss\_\min} = \frac{2}{T_d}\{K_1 R_{on}[K_2 R_{on}(2Q_{pri\_oss} + \frac{4n}{N}Q_{sec\_oss})^2 + Q_g V_{gs} f_s T_d^2]\}^{\frac{1}{2}} \quad (3\text{-}25)$$

In the case that *N* is large, (3-25) can be further simplified as,

$$P_{loss\_\min\_simple} = \frac{2}{T_d}\{4K_1 K_2 R_{on}^2 Q_{pri\_oss}^2 + K_1 R_{on} Q_g V_{gs} f_s T_d^2]\}^{\frac{1}{2}} \quad (3\text{-}26)$$

The improved primary device selection method for LLC resonant converter are provided based on (3-25) and (3-26). Four cases are compared in a 400 V-12 V, 300 W, 1 MHz LLC converter shown in the Figure 3-28. The blue bar is calculated based on (3-18), which has a full consideration on all loss parts; the orange bar is based on (3-25), which neglects the turn-off loss; the green bar is based on (3-26), which neglects the secondary side device equivalent charge; the yellow bar is based on the device selection in [37], which did not consider the primary and secondary side device charges. As can be seen, the blue, orange and green bars have the same trend for different devices. The (3-26) based green bar can well represents the results in the device selection in the LLC resonant converter.

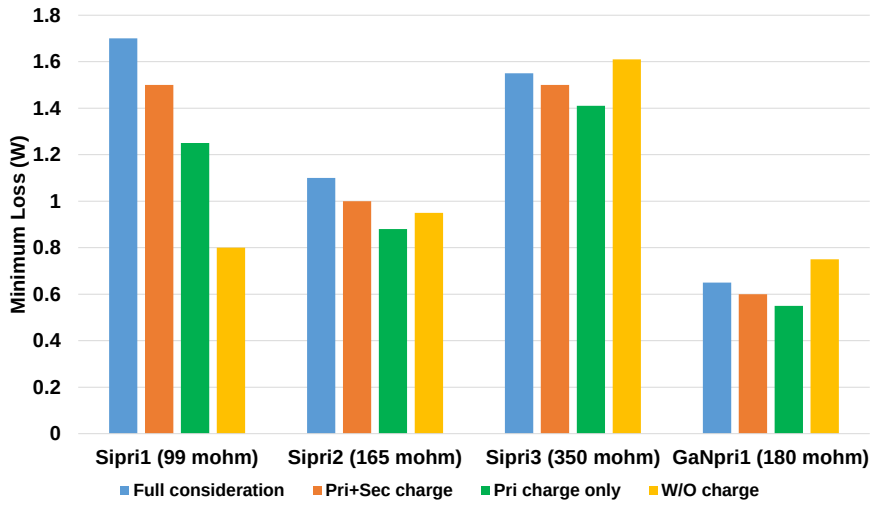


Figure 3-28. Comparison on different device selection approaches.

3.5 Transformer Winding Loss Reduction by Applying GaN Devices

The transformer loss, especially the winding loss, is another significant loss mechanism in the high frequency LLC resonant converter. In the LLC resonant converter, the inductance L_m that builds the current to help ZVS of the devices is usually realized by the transformer magnetizing inductance, therefore the magnetizing current is part of the transformer primary side current, and the secondary side current is equal to the primary side current minus the magnetizing current, shown in Figure 3-29. Due to the existence of the magnetizing current, a phase shift angle exists between the primary side and secondary side current. One particular issue in the LLC transformer winding loss which has not been discussed before is the extra winding loss induced by the asymmetrical primary side and secondary side current with the existence of the magnetizing current, which will be analyzed in this section.

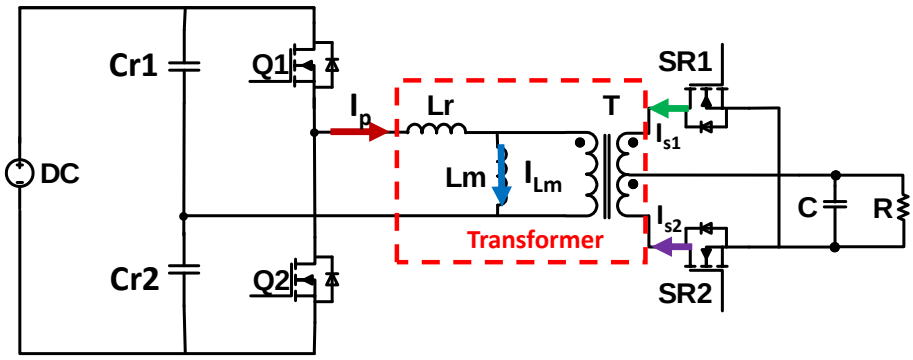


Figure 3-29. Magnetizing inductance in transformer.

As mentioned in Section 2.1.2, the transformer winding loss in high frequency LLC resonant converter usually includes pure winding loss, terminal loss and fringe effect loss. The asymmetrical primary side and secondary side current mainly increases the pure winding loss.

When a transformer winding carries high frequency current, the eddy current effects become severe, leading to the unevenly distributed current as well as the high winding loss. Interleaving winding structure helps to reduce the pure winding loss by cancelling the magnetic field (*H* field) between some of the windings where the transformer primary side current and secondary side current exist in the same amplitude and opposite direction. However, in the LLC resonant converter, the scenario of the interleaving winding structure is different. In order to achieve high power density requirement for the LLC resonant converter, the two inductors in the resonant tank are usually integrated in the transformer, shown in Figure 3-29. L_r is realized by the transformer leakage inductance, and L_m is realized by the transformer magnetizing inductance with the air gap between the cores. Due to this structure, the transformer primary side current I_p contains the magnetizing current I_{Lm}, considered as the circulating current, and the secondary side current I_s is the difference between I_p and I_{Lm} that really delivers the power from the input to the load. Due to the existence of I_{Lm}, there is a phase angle Φ_d, as shown in Figure 3-30, which is determined by,

$$\emptyset_d = \arcsin\left(\frac{-I_{Lmpeak}}{\sqrt{2}I_{RMS\_P}}\right) = \arcsin\left(\frac{-Q/T_d}{\sqrt{2}I_{RMS\_P}}\right) \tag{3-27}$$

where I_{priRMS} is the primary side RMS current; I_{Lmpeak} is the peak magnetizing current, Q is the total charge during the soft-switching transient; T_d is dead time.

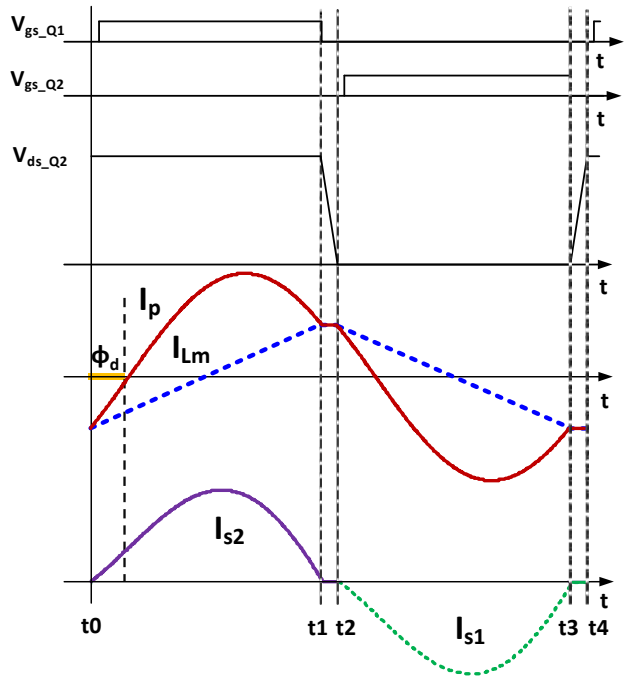


Figure 3-30. Converter waveforms with phase angle.

The transformer winding thickness is usually selected in the vicinity of one penetration depth at certain switching frequency. Under that condition, the winding loss is impacted by the *H* field distribution between the windings. The mutually cancelled *H* field are easily obtained by primary side and secondary winding interleaving. For example, according to the Ampere's law, the *H* field in the shaded area in the interleaving winding structure shown in Figure 3-31 is close to zero, because the I_p and I_s are symmetrically in the same amplitude and the opposite direction. However, as to the LLC transformer, I_p and I_s are asymmetrical with the existence of Φ_d. It is difficult to achieve zero *H* field, and even in the Φ_d period, the *H* field is intensified during certain time range.

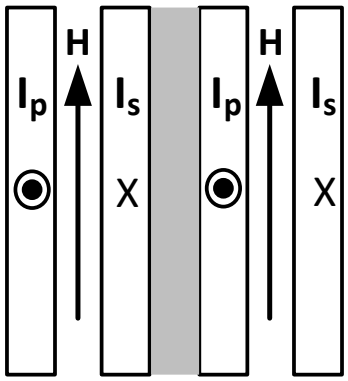


Figure 3-31. Interleaving winding structure with H cancellation.

In order to investigate the Φ_d impact on the pure winding loss, Ansys Maxwell 2D simulation is applied. Among all the simulation solvers, the eddy current solver is not suitable for this simulation, because it only works for the sinusoidal current excitation. With the symmetrical primary side and secondary side current, if there is no center-tap for the transformer and the current is the sinusoidal waveform, the eddy current solver can be applied. In the LLC resonant converter case, with the center-tapped structure, the secondary side current is the half wave current. Beside of this, there is phase different between the primary side and secondary side current, therefore only the magnetic transient solver can be applied in this simulation.

A 16:1 center-tapped transformer winding is modeled in the Maxwell 2D simulation, shown in Figure 3-32. The transformer converts positive/negative 200 V square wave voltage to positive/negative 12 V square wave voltage. There are sixteen turns in series as the primary side winding, and four turns in parallel as one secondary side winding. The geometry model is axisymmetric about Z axis (or RZ plane). Each PCB winding is a 70 μm or 2oz copper. The width of the primary side winding is 1 mm, and the secondary winding is 5 mm. The space between the PCB windings is 0.127 mm. The magnetic transient solver is applied in the simulation. The

primary side excitation is the sinusoidal current excitation that simulates the primary side resonant current. The secondary side excitation is half wave current excitation with 50% duty cycle to simulate the secondary side current.

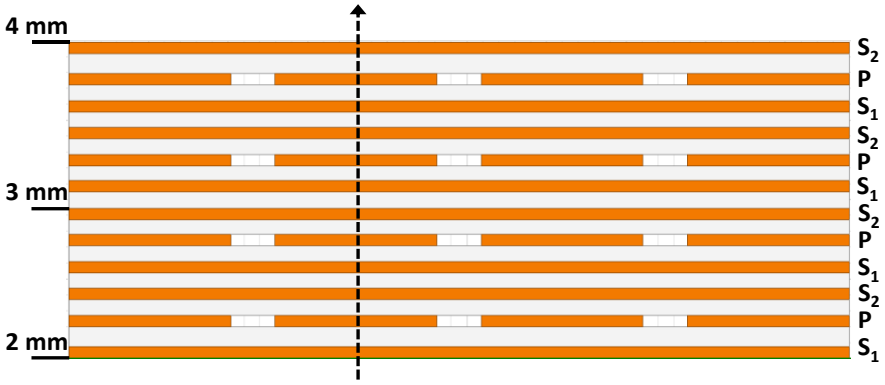


Figure 3-32. 2D transformer winding structure in simulation.

Figure 3-33 and Figure 3-34 show the simulation results when the Φ_d is equal to 0 and 0.7 rad respectively. As can be seen, the transient winding loss is also shaped as the sinusoidal waveform. In Figure 3-33, the minimum winding loss point reaches close to zero when the primary side and secondary side current reaches to zero. In Figure 3-34, the minimum loss happens when the primary side current reaches zero. However it is still around 2 W due to asymmetrical current. According to the simulation results, when the Φ_d=0.7, the corresponding peak magnetizing current is about 2.1 A. The asymmetrical current case at Φ_d=0.7 shows 3.03 W pure winding loss, compared with the 1.77 W pure winding loss in the symmetrical current (Φ_d=0) case.

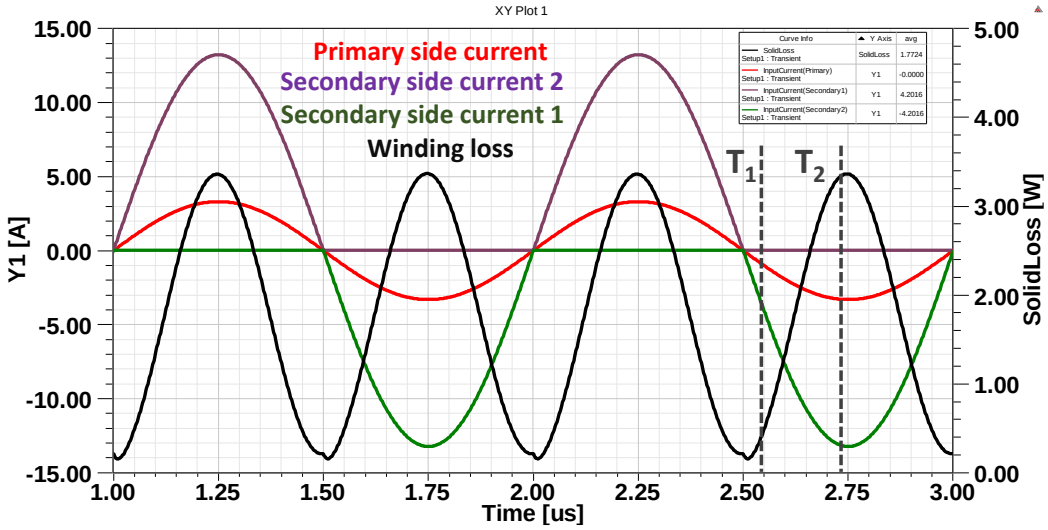


Figure 3-33. Simulation results @ $\Phi_d=0$.

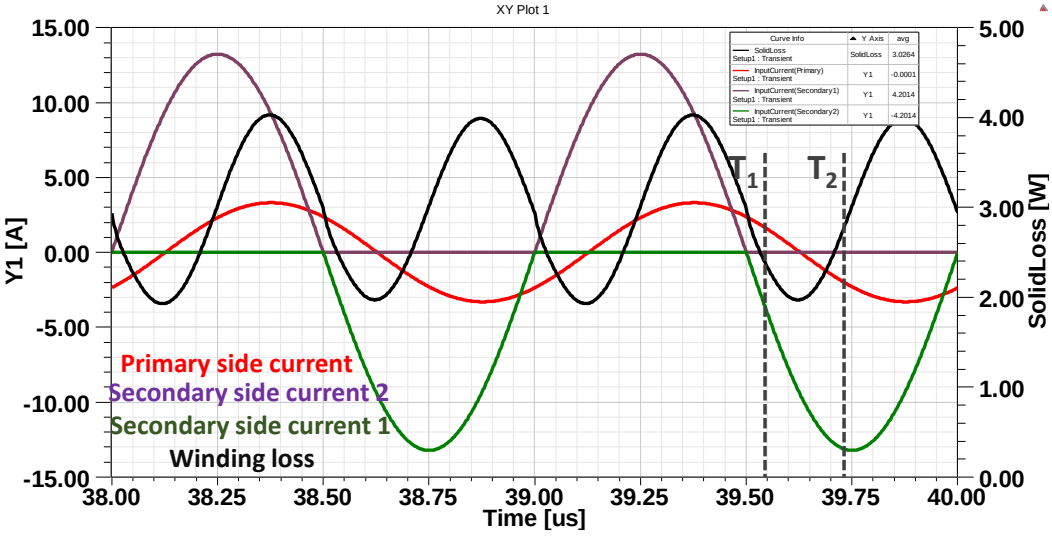


Figure 3-34. Simulation results @ $\Phi_d=0.7$.

There are two special time points selected in Figure 3-33 and Figure 3-34. In Figure 3-34, the first one T_1 is selected inside the Φ_d range to investigate the H field and current density distribution. The second one T_2 is selected when one of the secondary side current reaches to the negative peak

value. The T_1 and T_2 in Figure 3-33 follows the same time point. Figure 3-35 and Figure 3-36 show the H field distribution along with the examine line depicted in Figure 3-32 at Φ_d =0 and Φ_d =0.7 respectively. Figure 3-37 and Figure 3-38 show the current distribution along with the examine line depicted in Figure 3-32 at Φ_d =0 and Φ_d =0.7 respectively. The reference direction of among the Figure 3-33, Figure 3-34, Figure 3-37 and Figure 3-38 is presented in Table 3-4.

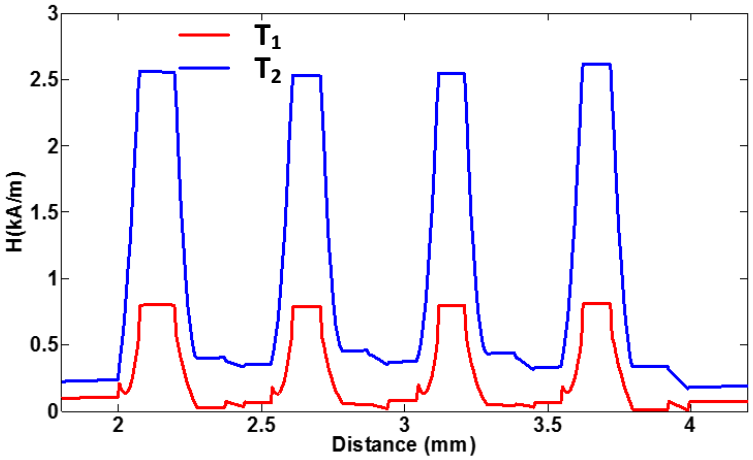


Figure 3-35. H field distribution @ Φ_d =0.

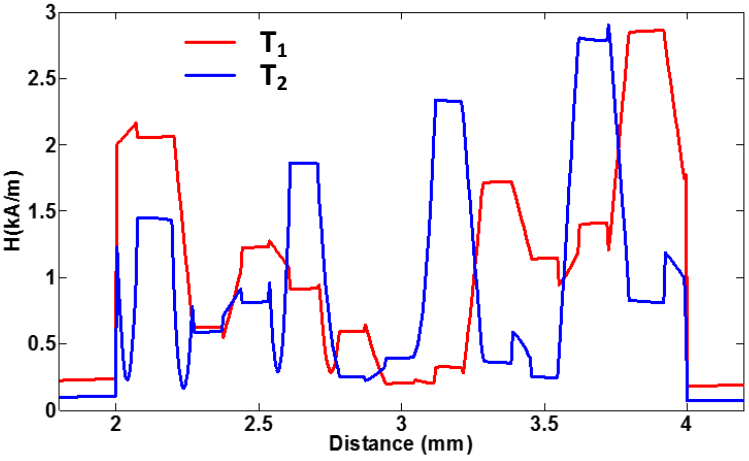


Figure 3-36. H field distribution @ Φ_d =0.7.

Table 3-4. Current waveform and current density reference direction

Primary current in simulation waveforms	Primary current density distribution	Secondary current simulation waveforms	Secondary current density distribution
Negative	Negative	Negative	Positive
Positive	Positive	Positive	Negative

There are two interesting phenomena:

1. The *H* field distribution in Figure 3-35 is a typical distribution in the interleaving winding structure. The H field distribution at both T_1 and T_2 in Figure 3-36 is intensified at some region where they are close to zero in Figure 3-35.
2. In the Φ_d =0 case in Figure 3-37, the current distribution of the primary side winding and secondary side winding are distributed with symmetrically secondary side positive and primary side negative. However, as to the T_1 time point in the Φ_d =0.7 case in Figure 3-38, based on the reference direction shown in Table 3-4, the secondary side current distribution direction should be positive because the current waveform is negative. However, the current distribution direction shows part of negative. The secondary negative current distribution induces higher primary positive current distribution, therefore higher primary side winding loss.

The winding loss simulation has been done from Φ_d =0 to Φ_d =0.8 cases, Figure 3-39 shows the simulation results of the pure winding loss versus Φ_d. The loss increase becomes higher when the Φ_d is large. The simulation results helps to analyze the GaN device benefits to transformer winding loss.

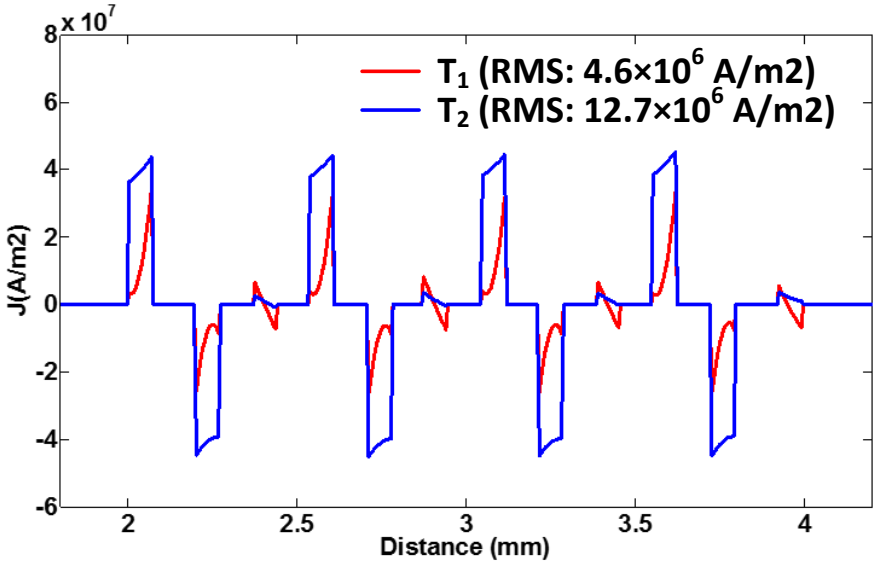


Figure 3-37. Current density distribution @ Φ_d =0.

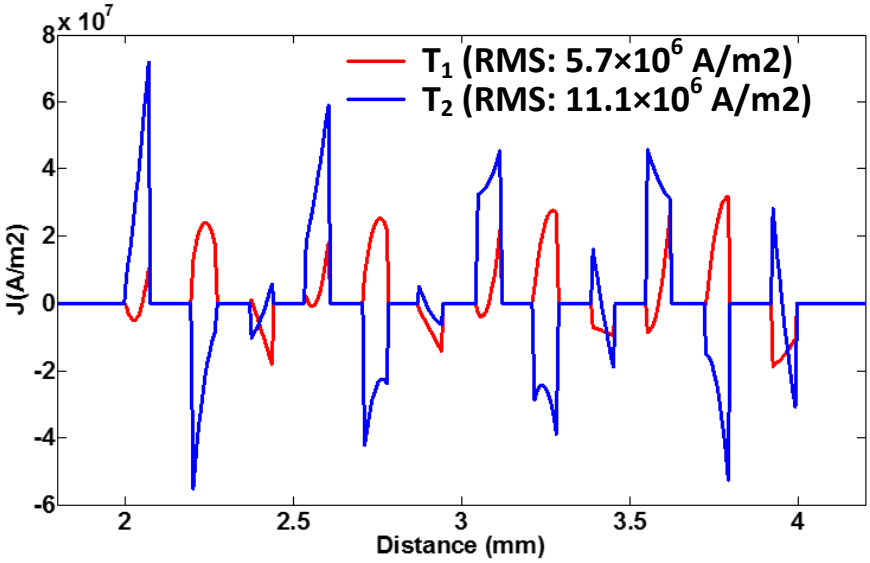


Figure 3-38. Current density distribution @ Φ_d =0.7.

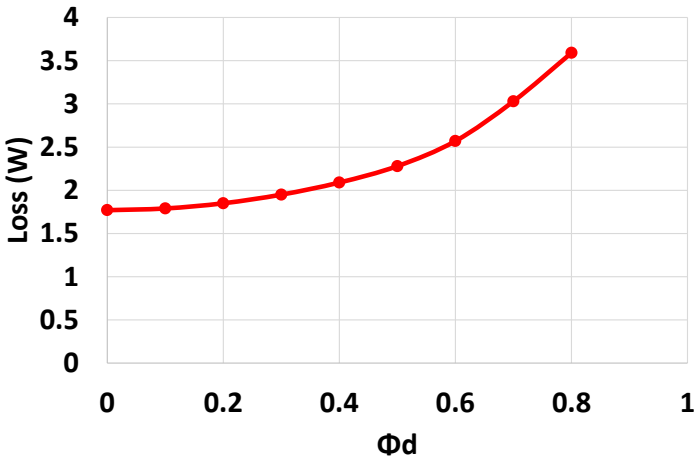


Figure 3-39. Pure winding loss versus Φ_d.

By the curve fitting method, Φ_d and the winding loss shown in Figure 3-39 is expressed as

$$P_{winding} = 2.593\emptyset_d^4 - 0.387\emptyset_d^3 + 1.309\emptyset_d^2 + 0.159\emptyset_d + 1.767 \quad (3\text{-}28)$$

Combining the (3-27), (3-1) and (3-8), the Φ_d is expressed with device capacitance and dead time,

$$\emptyset_d = \arcsin\left(\frac{-(2C_{pri\_oss}V_{in}+C_w*V_{in}+\frac{1}{N}2nC_{sec\_oss}*2V_o)/T_d}{\sqrt{\frac{V_0^2\pi^2T_s^2}{8R_L^2N^2(T_s-2T_d)^2}+\frac{1}{2}\cdot\left(\frac{2C_{pri\_oss}V_{in}+C_wV_{in}+\frac{1}{N}2nC_{sec\_oss}*2V_o}{T_d}\right)^2}}\right) \quad (3\text{-}29)$$

Substitute (3-29) to (3-28), an expression that relates the winding loss and dead time as well as the device parameters can be derived and plotted in Figure 3-40.

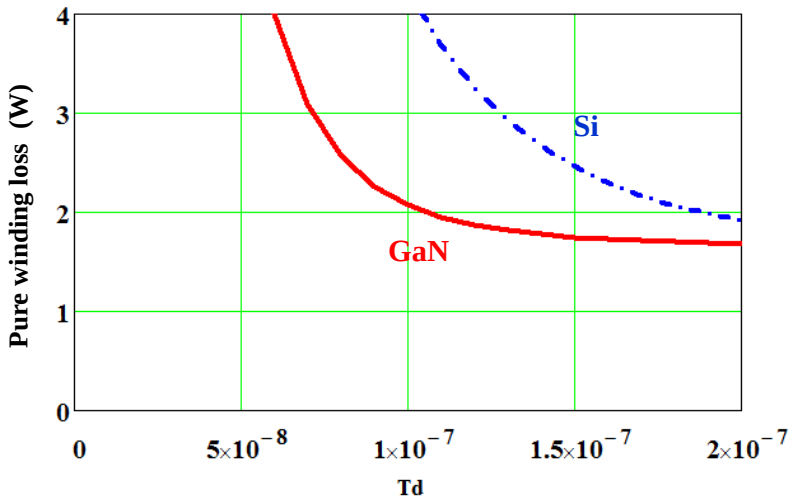


Figure 3-40. Winding loss vs. dead time.

According to Figure 3-40, when the dead time is large, the required peak magnetizing current is low and therefore the Φ_d is approaching to zero. The winding loss is also approaching its lowest value, which satisfies the curve shown in Figure 3-39. The above approach shows that the Φ_d behaves as an intermediate variable. Φ_d has a direct relationship with the winding loss, which is proved by the FEA simulation. On the other hand, Φ_d is related to the converter RMS current and peak magnetizing current, then to the device parameters and the dead time. Consequently, the relationship between the device parameters and the winding loss is established in the LLC resonant converter.

In Figure 3-40, if both the Si case and GaN case pick the same dead time, the Si case has more than 1.5 W more winding loss compared with the GaN case. The impact of the asymmetrical primary side and secondary side current leads to improved LLC resonant converter design approach considering both the impact of device parameters and asymmetrical currents, which will be discussed in Chapter 5.

3.6 Overall Loss Breakdown and Experimental Verification

Based on the analysis of the GaN device impact on device loss and transformer winding loss shown previously, the overall loss breakdown and comparison between Si-based and GaN-based converters with the specifications shown in Table 3-1 are shown in Figure 3-41. Both the primary side and secondary side device losses are reduced by around 50%; the transformer loss reduction is 18%; the capacitor ESR loss reduction is 30% which is due to the reduced RMS current.

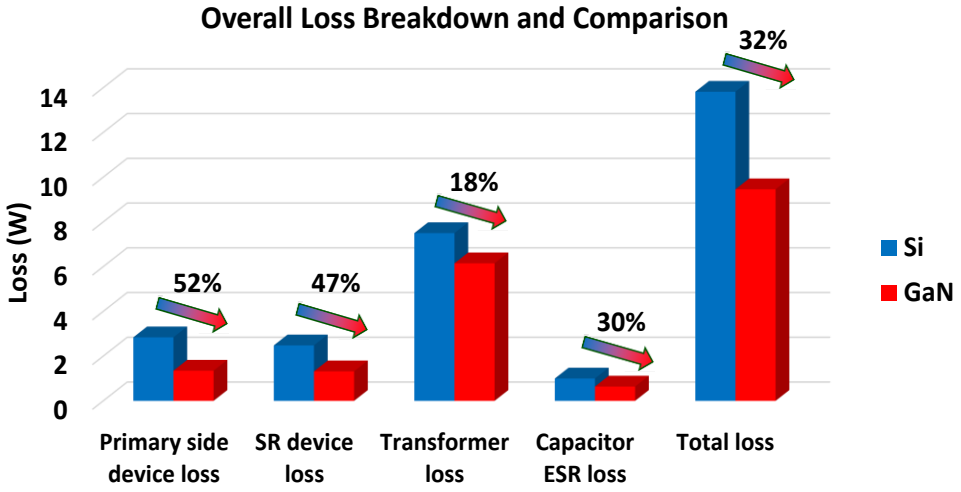
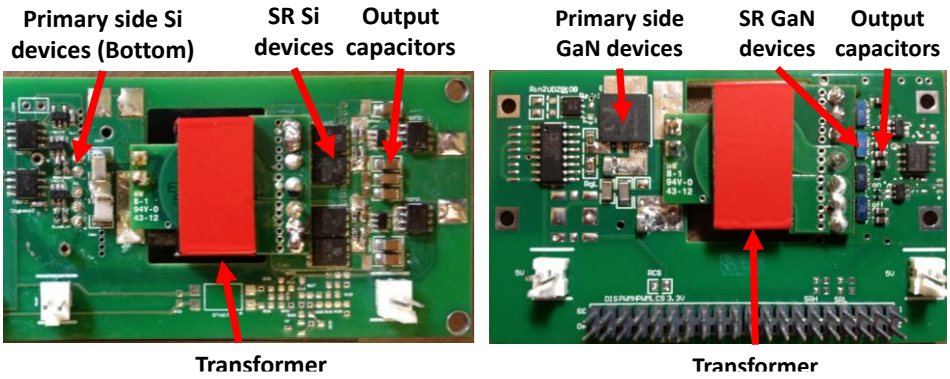


Figure 3-41. Overall loss breakdown and comparison.

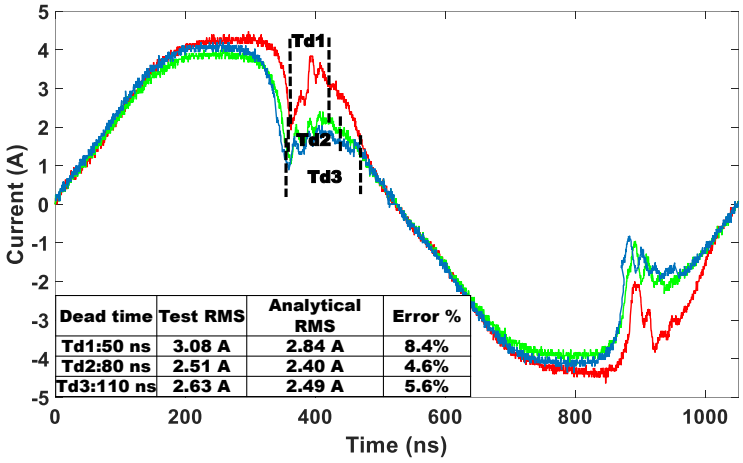
Both Si-based and GaN-based 400 V-12 V/300 W/1 MHz LLC resonant converter prototype are built, shown in Figure 3-42. A 16:1 turns ratio ER23/5/13 N49 ferrite planar transformer was constructed. The PCB windings were designed with 2 oz copper thickness and 12 layers. The gate drivers are ADUM3223 for the primary side and LM5114 for the secondary side. The prototypes are tested using FPGA-based digital controller. The dead time was set as 130 ns for the Si-based converter, and 80 ns for the GaN-based converter.



(a) Si-based LLC resonant converter (b) GaN-based LLC resonant converter

Figure 3-42. LLC resonant converter prototypes.

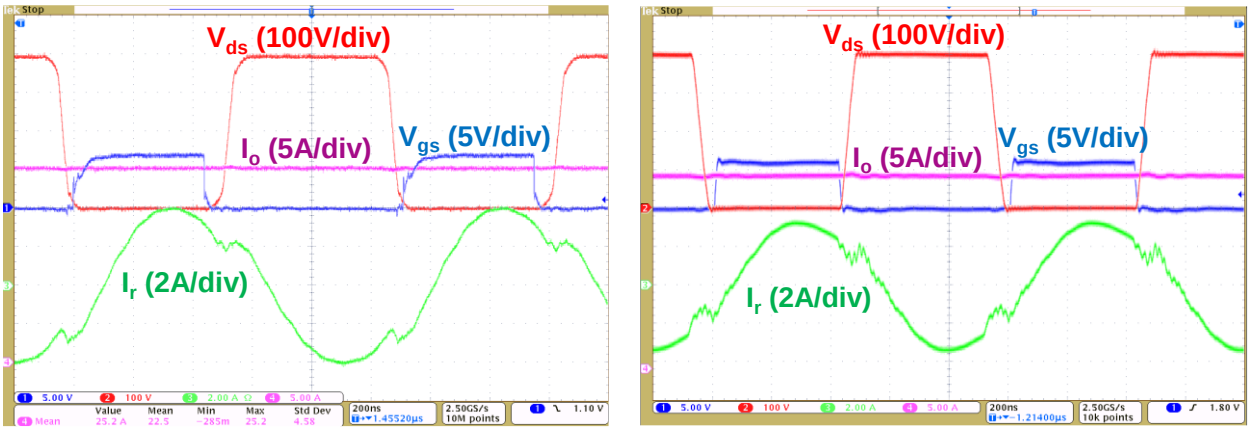
In order to verify the established relations in (3-12) and (3-13), the primary side current in three different dead time cases have been tested in the GaN based LLC resonant converter shown in Figure 3-42(b) at full load. In order to guarantee the critical ZVS of the devices, when the dead time changes, the magnetizing inductance of the transformer also need to be changed. The waveforms are plotted in Figure 3-43. The green waveform shows the optimal dead time T_{d2} and RMS current. T_{d1} is shorter than T_{d2} leading to higher RMS current due to higher peak magnetizing current. T_{d3} is longer than T_{d2} leading to higher RMS current as well due to the shorter energy transfer time.



Dead time	Test RMS	Analytical RMS	Error %
Td1:50 ns	3.08 A	2.84 A	8.4%
Td2:80 ns	2.51 A	2.40 A	4.6%
Td3:110 ns	2.63 A	2.49 A	5.6%

Figure 3-43. Primary side current with different dead times.

The waveforms of the two converters at full load are shown in Figure 3-44. The GaN-based converter demonstrates shorter drain-source voltage falling time. The peak magnetizing current of the GaN-based converter is also lower than that of the Si-based converter. The measured primary side RMS current is 2.99 A for the Si design, and 2.35 A for the GaN design. The average value of the output current in the Si-based converter is 25.2 A, and for the GaN-based converter is 25.3 A. It should be noted that since the layout for the power loops and the values of the passive components are not exactly the same in both prototypes, the resonances are not the same. As the switching frequency needs to track the resonant frequency, the switching frequency was set as 930 kHz for the Si design, and 1MHz for the GaN design. Applying (9) by changing the switching period from 1000 ns to 1075 ns, the Si case minimum RMS current reduces from 3.01 A only to 2.94 A. Therefore, the impact to the RMS current and conduction loss is small.

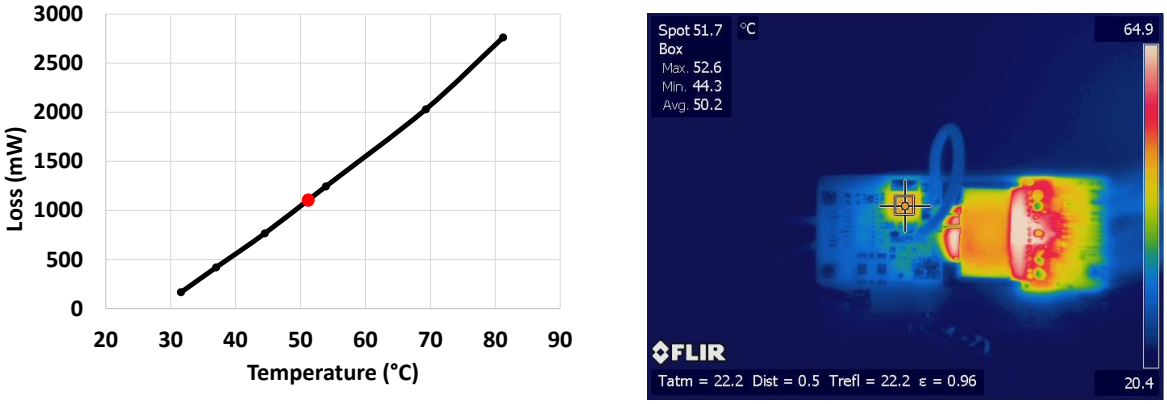


(a) Si-based LLC converter waveforms (b) GaN-based LLC converter waveforms

Figure 3-44. LLC converter waveforms.

In order to verify the device analytical loss, thermal test was applied on the GaN-based converter prototype. First, a benchmark between the device loss and temperature was established. 8 V DC voltages were added as the gate-source voltages on the both top and bottom cascode GaN devices in Figure 3-42(b). By implement the DC current to the device and measuring the drain-source voltage, the device conduction loss can be obtained. Meanwhile, the device surface temperature can be measured by a thermal imaging camera. An Agilent E3631A power supply supplied the DC current, and the drain-source voltage was measured by an Agilent 34410A 6 ½ digits high precision digital multimeter. The temperature was measured by a FLIR SC620 thermal imaging camera. The device was under the same air cooling condition when it was running at the full load. The primary side GaN device loss versus temperature was derived in Figure 3-45(a). The thermal image at the full load is shown in Figure 3-45(b), and the measured device temperate and the corresponding loss is dotted in Figure 3-45(a). The loss verification of the secondary side devices were done in the same method. Table 3-5 compares the measured loss and the analytical loss of the devices. One particular issue is that error percentage of the GaN primary side device is

high. The investigation in Chapter 4 shows that the cascode GaN device has the turn-on loss during the soft-switching transient. By compensating the extra loss, the error percentage drops to 6%. Therefore, the test of the device loss verifies the analytical results.



(a) Device loss versus temperature (b) Primary side GaN device thermal image

Figure 3-45. Primary side current with different dead times.

Table 3-5. Comparison between measured and analytical loss

	Measured loss (W)	Analytical loss (W)	Error percentage based on measured loss
Si primary	1.51	1.42	6%
Si secondary	0.35	0.31	11%
GaN primary	1.14	0.675 (1.075)	41% (6%)
GaN secondary	0.18	0.165	8%
Si total	14.5	13.82	5%
GaN total	10.9	9.46 (10.26)	13% (6%)

The efficiencies were measured for Si-based and GaN-based converter under different load condition shown in Figure 3-46. The GaN based converter demonstrates 96.8% peak efficiency and 96.6% full load efficiency, which is about 1% higher than the Si based converter.

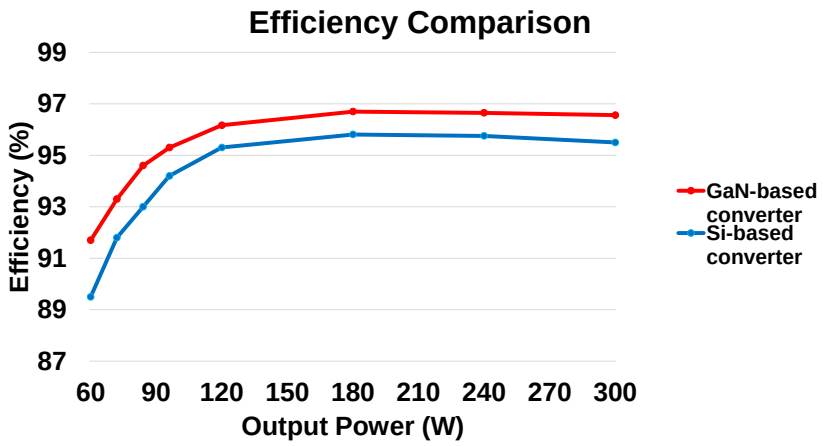


Figure 3-46. Efficiency curves and comparison.

3.7 Summary

In order to understand the GaN device benefits in a LLC resonant converter, this chapter first establishes the relation of device and design parameters to the device loss, and then quantifies the loss reduction by comparing GaN-based and Si-based designs. Due to the low effective output capacitance of GaN devices, the GaN-based design demonstrates around 50% device loss reduction compared to the Si based design. Next, a new perspective on the extra winding loss due to the asymmetrical primary side and secondary side current is proposed. The device and design parameters are tied to the winding loss based on the winding loss results in FEA simulation. The winding loss is reduced by 18% in the GaN-based design. Finally, the overall analytical loss breakdown illustrates the 32% total loss reduction of the GaN-based LLC resonant converter. A thermal test was applied to evaluate the device loss in the GaN-based prototype. The test results verified the analytical device loss. 1% efficiency improvement, which is 24.8% loss reduction, is achieved in the 400-to-12 V GaN-based converter at 1 MHz and 300 W.

4 Soft-switching Behavior of 600 V Cascode GaN HEMT

This chapter investigates the soft switching transient of the cascode GaN HEMT in detail. Several interesting phenomena the soft-switching transient is discussed. The channel current drops to zero quickly during the turn-off transient due to the internal feedback of the cascode structure, which leads to extremely low turn-off loss. However, switching energy loss is observed on the internal normally-on GaN HEMT during the turn-on transient, despite the external waveforms of the cascode GaN HEMT exhibiting ZVS. Based on the simulation, a possible solution can be to increase the gate-source capacitance or add another capacitor on the gate source terminals of the internal normally-on GaN HEMT In that way, the loss can be mitigated. Thermal tests were implemented to evaluate the switching loss during the soft-switching transient. The test results show that there are about 400 mW of switching loss at 1 MHz. The loss value is nearly constant as the load current is varied.

4.1 Soft-switching Behavior Analysis for the Cascode GaN HEMT

The half-bridge, or phase-leg structure, is widely applied in power electronics. Figure 4-1 shows a phase-leg structure based on the cascode GaN HEMTs. Intrinsic device capacitances and body diodes are included. An inductor is placed between the phase-leg and the mid-point of the DC voltage bus. By switching between Q1 and Q2 conduction intervals with nearly 50% duty cycle, the inductor current can be made as a triangular wave shape. The inductor L is usually large, which can be considered as a current source during the soft-switching transient.

Analysis presented here focuses on the switching interval when Q1 is turning off and Q2 is turning on. The soft switching transient starts when there is a turn-off gate signal applied on Q1. There are five intervals in total. The switching behaviors of Q1 and Q2 during each interval are

addressed individually in the following subsections. Figure 4-2 shows simulated waveforms of the switching transient, with the different intervals labeled. Simulations are carried out in LTSPICE using a manufacturer-supplied circuit model of a commercially available GaN device. In the following discussion, and as shown in Figure 4-1, $V_{gs\_MOS\_Q1}$, $V_{gd\_MOS\_Q1}$ and $V_{ds\_MOS\_Q1}$ are the gate-source voltage, gate-drain voltage and drain-source voltage of the LV Si MOSFET. $V_{gs\_GaN\_Q1}$, $V_{gd\_GaN\_Q1}$ and $V_{ds\_GaN\_Q1}$ are the gate-source voltage, gate-drain voltage and drain-source voltage of the normally-on GaN HEMT. V_{gs_Q1}, V_{gd_Q1} and V_{ds_Q1} are the gate-source voltage, gate-drain voltage and drain-source voltage of the entire cascode device. The Q1 internal LV Si MOSFET is defined as MOS_Q1, and the Q1 internal HV normally-on GaN HEMT is defined as GaN_Q1. The definitions for Q2 are the same.

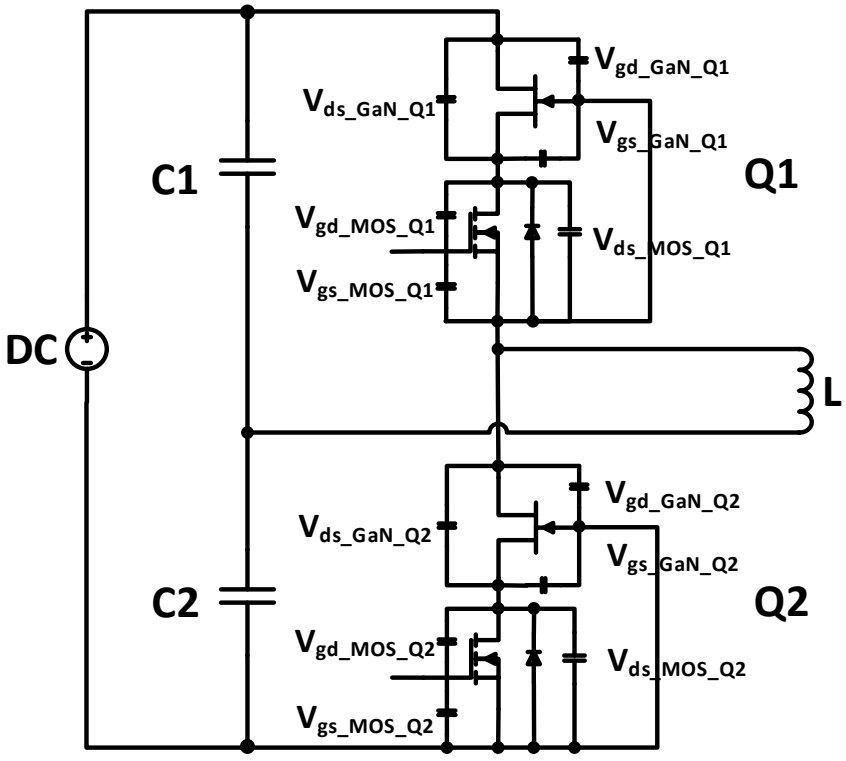


Figure 4-1. Phase-leg structure with inductive load.

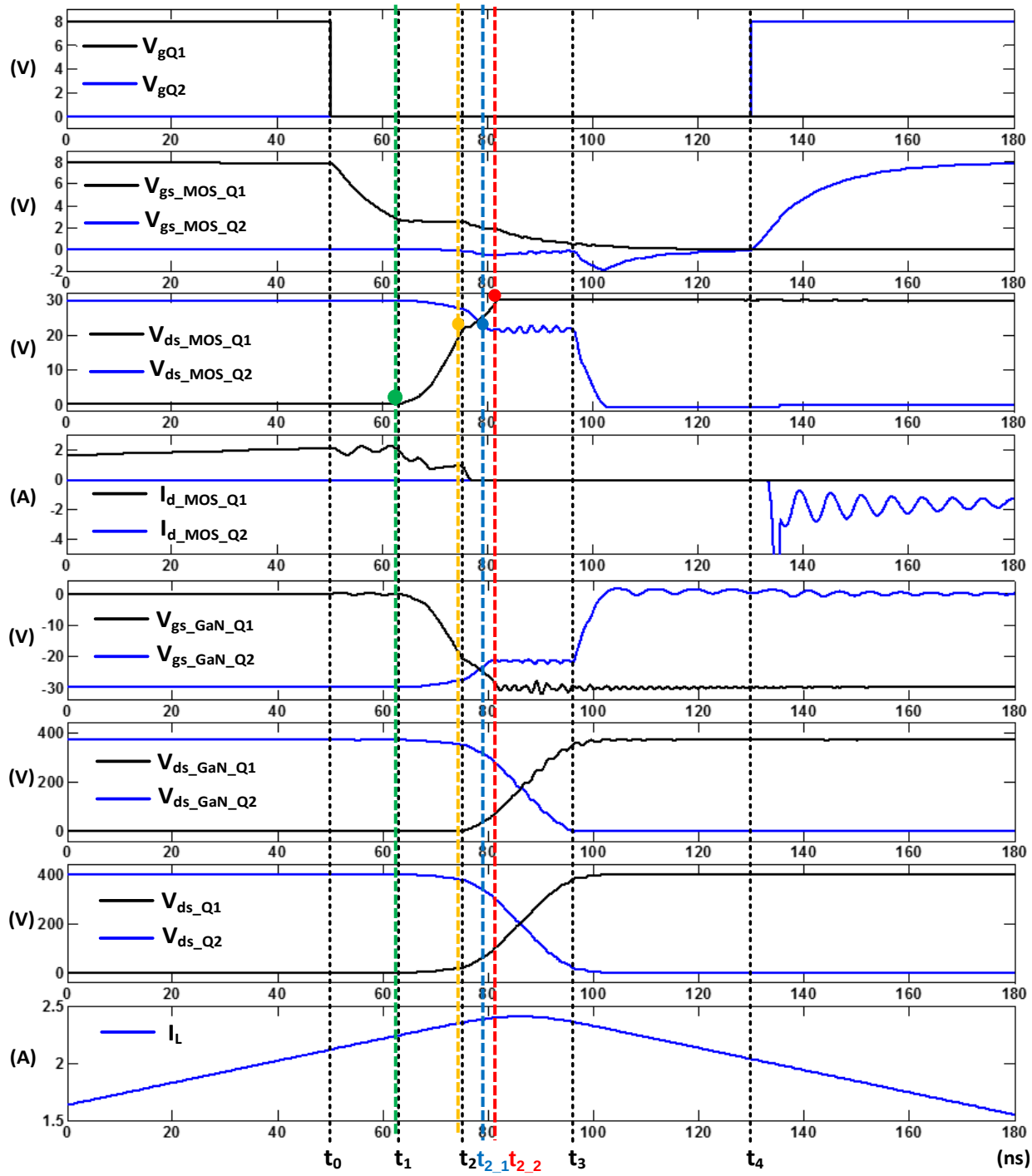


Figure 4-2. Simulation waveform in the soft-switching transition.

Interval I (t_0~t_1):

Q1: Prior to the beginning of this interval, Q1 is on. The device can be modeled as two on-state resistances in series: that of the GaN_Q1 and that of the MOS_Q1. At t_0, the gate signal V_{g1} is dropped to zero. The input capacitance of MOS_Q1 begins to discharge through the gate drive loop and $V_{gs\_MOS\_Q1}$ starts to decrease. A small part of the channel current is diverted to charge the C_{gdm1} due to the change of $V_{gs\_MOS\_Q1}$. During this interval, since $V_{gs\_MOS\_Q1}$ is still higher than the Miller voltage and threshold voltage, so the MOS_Q1 remains in the linear region. There is no significant change in $V_{ds\_MOS\_Q1}$, and GaN_Q1 is still in fully on-state, carrying all the inductor current I_L. Figure 4-3 shows the equivalent circuit in this interval.

Q2: Q2 remains in the off-state during this interval.

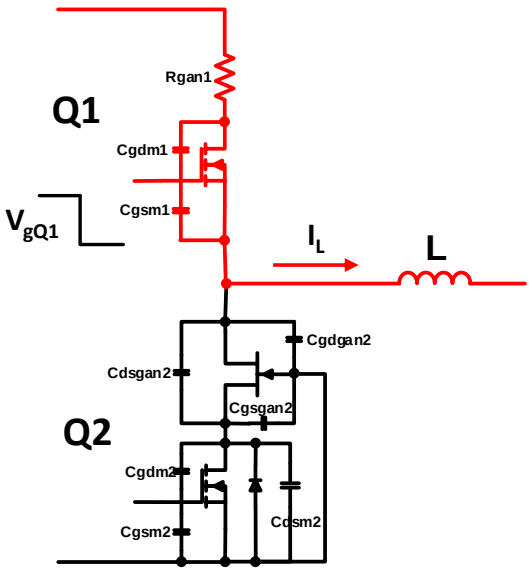


Figure 4-3. Equivalent circuit in Interval I.

Interval II (t_1~t_2):

Q1: $V_{gs\_MOS\_Q1}$ continues to decrease, leading the MOS_Q1 to go into the saturation region. The channel current carrying capability of the MOS_Q1 is reduced. Part of the inductor current starts to charge the output capacitance of MOS_Q1, including C_{dsm1} and C_{gdm1}. At the same time, the input capacitance of GaN_Q1 is being charged as well. As a result, $V_{ds\_MOS\_Q1}$ starts to increase, and $V_{gs\_GaN\_Q1}$ starts to decrease to a negative value. Before $V_{gs\_GaN\_Q1}$ is above the pinch-off voltage, the channel of GaN_Q1 is still fully on, therefore the increase of $V_{ds\_MOS\_Q1}$ induces an increase in V_{ds_Q1}. In the saturation region, the MOS_Q1 channel can be modeled as a voltage controlled current source, satisfying the equation $i_{ch} = g_m(V_{gs\_MOS\_Q1} - v_{th})$.

Q2: Following the increase of V_{ds_Q1}, V_{ds_Q2} starts to decrease. The discharging current from Q2 shares part of the inductor current. As can be seen in the equivalent circuit in Fig. 5, the junction capacitances of GaN_Q2 and MOS_Q2 become a capacitive divider. $V_{ds\_MOS\_Q2}$ and $V_{ds\_GaN\_Q2}$ are both decreasing with gradients depending on the ratio of the capacitive divider. During this interval, GaN_Q2 is in off state, since $V_{gs\_GaN\_Q2}$ is still below the pinch-off voltage. Figure 4-4 shows the equivalent circuit in this interval.

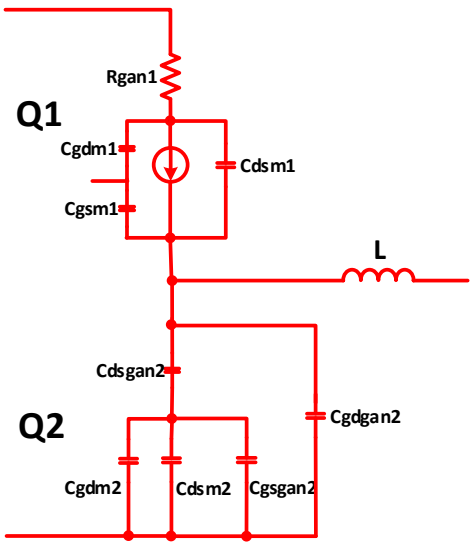


Figure 4-4. Equivalent circuit in Interval II.

Interval III (t_2~t_3):

Interval III, equivalent circuit shown in Figure 4-5, exhibits several interesting phenomena of cascode devices. First, the channel current of Q1 drops to zero very quickly due to the internal feedback of the cascode structure, which leads to extremely small turn-off loss. Second, MOS_Q1 will go into the avalanche mode during this interval if $V_{ds\_MOS\_Q1}$ rises to the breakdown voltage before V_{ds_Q1} reaches the DC bus voltage. Finally, for Q2, there is switching energy loss on GaN_Q2 during ZVS turn-on transient, although the external waveforms of the cascode GaN HEMT exhibit ZVS.

Q1: $V_{gs\_MOS\_Q1}$ continues to decease below the threshold voltage until the channel of the MOS_Q1 is entirely off. The excess current continues to charge the output capacitance of the MOSFET as well as the input capacitance of GaN_Q1. With the decrease of $V_{gs\_GaN\_Q1}$, the channel current carrying capability of GaN_Q1 is reduced. Excess current starts to charge the output capacitance of GaN_Q1, causing $V_{ds\_GaN\_Q1}$ to increase.

At the same time, GaN_Q1 channel current drops to zero quickly as well. This phenomenon brings extremely low turn-off loss of GaN_Q1. The internal mechanism is: during this interval, the channel of the MOS_Q1 has already entered the cut-off region. As long as the channel of the GaN_Q1 remains on, the GaN_Q1 channel current will continue to change the MOS_Q1 output capacitance, leading to the further increase of $V_{ds\_MOS\_Q1}$. If this current is large, $V_{gs\_GaN\_Q1}$ quickly moves below the pinch-off voltage, and the GaN_Q1 channel is rapidly shut off. This internal feedback accelerates the channel current quickly dropping to zero. Additionally, the current flowing through C_{dsgan1} also contributes this phenomenon. Due to this mechanism, GaN_Q1 channel current drops to zero in nearly the same time as the MOS_Q1 channel current. During a very short time period in this interval, the channel current of the GaN_Q1 drops to zero rapidly, and $V_{gs\_GaN\_Q1}$ drops below the pinch-off voltage. The excess current continues charging the junction capacitance, and $V_{ds\_GaN\_Q1}$ increases during the remainder of the interval.

In Figure 4-2, starting from the red dot, $V_{ds\_MOS\_Q1}$ reaches 30 V, which is the breakdown voltage of MOS_Q1, before V_{ds_Q1} increases to the DC bus voltage. This causes MOS_Q1 to go into the avalanche mode. The current path in this mode is shown in Figure 4-8. The reason for this phenomenon is that the sum of the $C_{oss\_MOS\_Q1}$ and $C_{iss\_GaN\_Q1}$ is smaller than the $C_{oss\_GaN\_Q1}$. This capacitance ratio also causes additional loss on Q2 during ZVS turn-on transition.

Q2: $V_{gs\_GaN\_Q2}$ starts to increase from negative voltage (with the decrease of $V_{ds\_MOS\_Q2}$) in the last interval. When it reaches the pinch-off voltage, it remains clamped there. The reason is that if $V_{gs\_GaN\_Q2}$ goes above the pinch-off voltage, GaN_Q2 will go into the saturation region. The charge stored in the C_{dsgan2} will be discharged in the GaN_Q2 channel, forming the channel current. Since at this time, the channel of the MOS_Q2 is in off-state, most of the GaN_Q2 channel current has to go back to the C_{dsgan2}, and part of the current will inevitably charge the output capacitance of

MOS_Q2, leading to the increase of $V_{ds\_MOS\_Q2}$. With the increase of $V_{ds\_MOS\_Q2}$, $V_{gs\_GaN\_Q2}$ will be pushed below the pinch-off voltage, and the channel is closed again. After that, due to the load current discharging capability, $V_{ds\_MOS\_Q2}$ will still decrease again, pulling $V_{gs\_GaN\_Q2}$ back above the pinch-off voltage. The device repeats the above process. As a result, the above internal mechanism determines that $V_{gs\_GaN\_Q2}$ (also the negative $V_{ds\_MOS\_Q2}$) is clamped at the pinch-off voltage. As shown in Figure 4-2, there are some small oscillations of the $V_{gs\_GaN\_Q2}$ near the pinch-off voltage. These oscillations imply that the GaN_Q2 operates between the saturation state and pinch-off state. In the saturation state, there will be the channel current from drain to source of the GaN_Q2, which is formed by the charge stored in the output capacitance. That induces extra loss during ZVS turn-on transient of Q2. The gate-source voltage clamping at the pinch-off voltage is another unique phenomenon to the cascode structure device in a soft switching transient. By the end of this interval, $V_{ds\_GaN\_Q2}$ reaches zero.

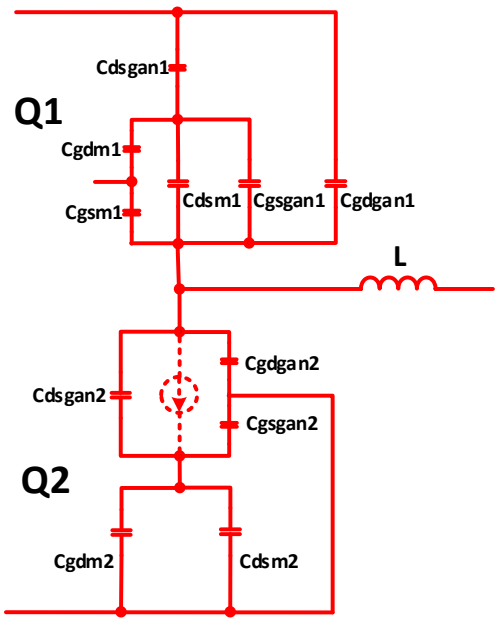


Figure 4-5. Equivalent circuit in Interval III.

Interval IV (t_3~t_4):

Q1: Since the channels of the both GaN_Q1 and MOS_Q1 are already shut off during the last interval, $V_{gs\_MOS\_Q1}$ and $V_{ds\_\_Q1}$ continue to decrease and increase respectively to finish the turn-off transition. Moreover, after $V_{ds\_\_Q1}$ increases to the DC bus voltage, MOS_Q1 leaves the avalanche mode. $V_{ds\_MOS\_Q1}$ will go back down to the voltage determined by the voltage distribution on the internal junction capacitances, and also keep GaN_Q1 at the pinch-off state.

Q2: When $V_{ds\_GaN\_Q2}$ drops to zero, $V_{gs\_GaN\_Q2}$ (also the negative $V_{ds\_MOS\_Q2}$) continues to increase from the pinch-off voltage to zero. The channel of GaN HEMT is entirely open and conducts the current together with the body diode of MOS_Q2. During this interval, V_{ds_Q1} increases to the DC bus voltage. The equivalent circuit is shown in Figure 4-6.

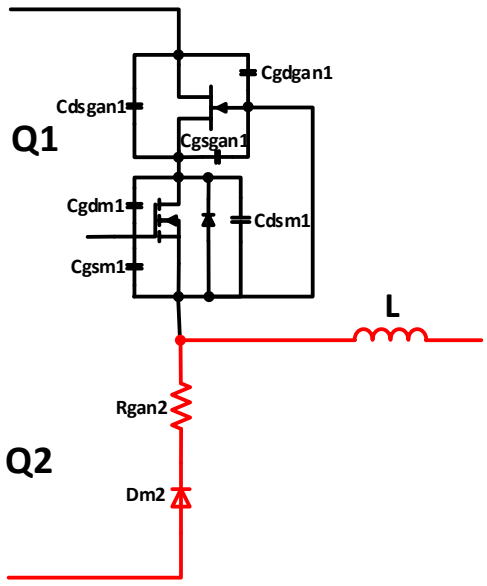


Figure 4-6. Equivalent circuit in Interval IV.

Interval V (after t_4):

After some dead time, positive gate-source voltage is applied on the MOS_Q2 and the channel is on. The current goes through the channels of MOS_Q2 and GaN_Q2. The soft switching transient is finished. The equivalent circuit is shown in Figure 4-7.

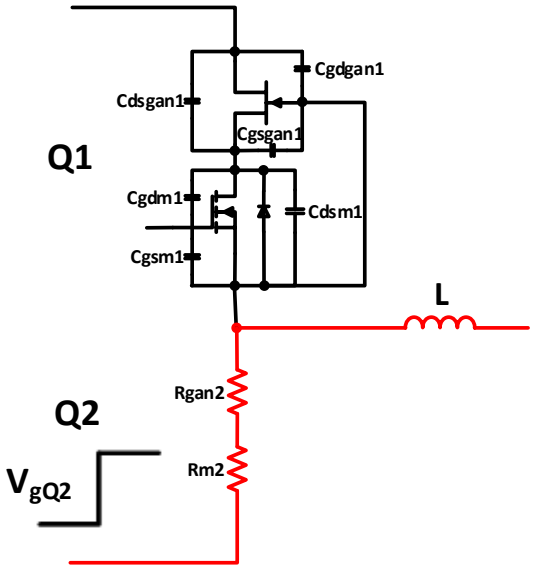


Figure 4-7. Equivalent circuit in Interval V.

Figure 4-2 demonstrates some of the critical time points during the soft-switching transient such as t_1, t_2, t_{2_1}, and t_{2_2}. The detailed equivalent circuit and current flow paths are shown in Figure 4-8. Special attention should be paid on t_{2_2}~t_3 period of Q1. During this time interval, the LV Si MOSFET of Q1 goes into the saturation region until the drain-source voltage of Q1 GaN HEMT finishes the transition. Another special time interval is t_{2_1}~t_3 of the soft-switching Q2 device. During this time interval, the energy stored in the output capacitance of the Q2 GaN HEMT is dissipated in the channel. The hard-switching turn-on of Q2 GaN HEMT happens, due to the

improper ratio of the sum of LV Si MOSFET output capacitance and internal GaN HEMT input capacitance to the internal GaN HEMT output capacitance.

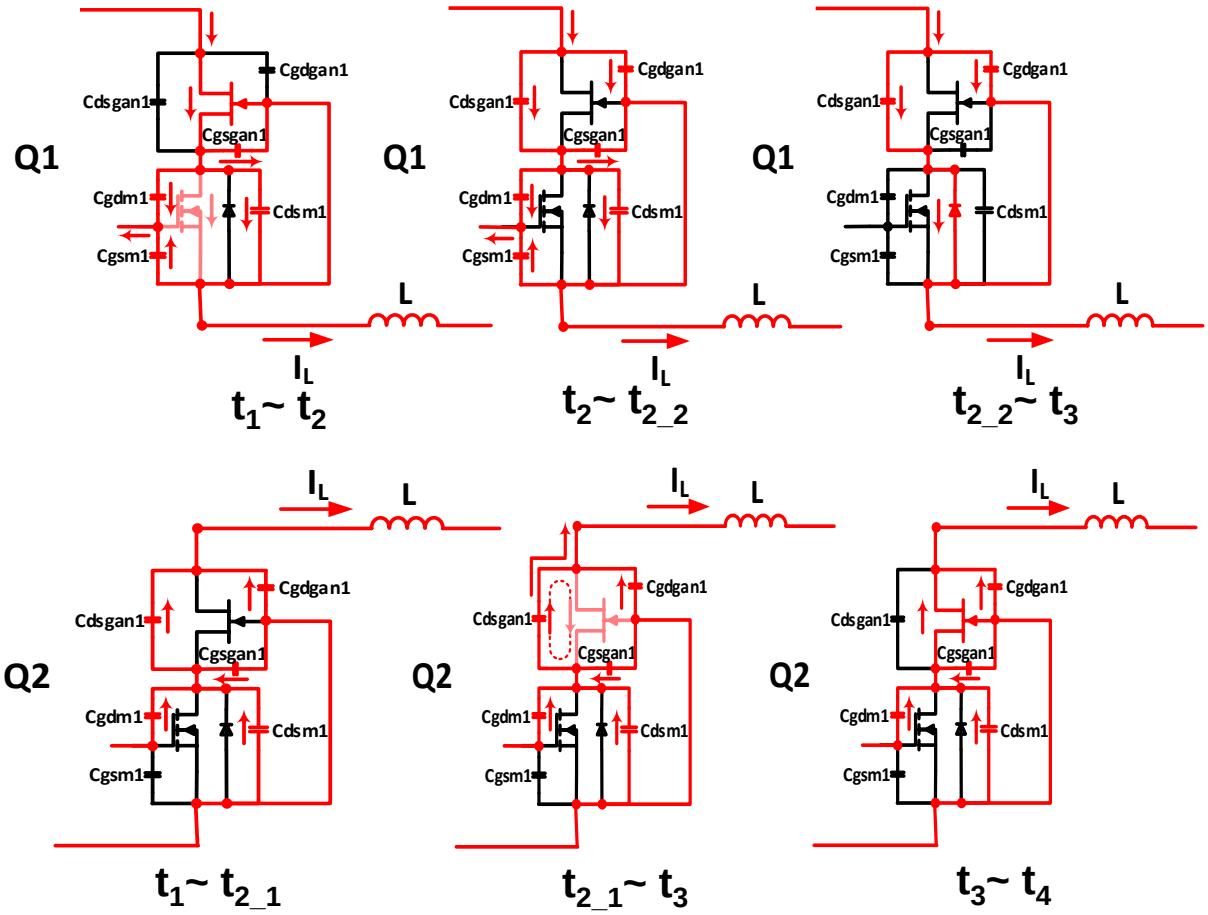


Figure 4-8. Detailed equivalent circuit and current flow paths.

4.2 Soft-switching Transient Discussion

4.2.1 Gate Driver Impact on the Soft-switching Transient

Gate driver is very important in a hard-switching transient, since it controls the switching performance of the devices. But the gate driver partially participates in the device soft-switching

transient. Only in interval I and interval II of the Q1 turn-off transient, the device behavior is influenced by the gate driver as well as the load current, while in the other intervals, the device is influenced by the load current only. On the other hand, the increase of V_{ds_Q1} is the dominant factor that determines the decrease of V_{ds_Q2}, because the Q1 behavior is initially controlled by the gate driver. In other words, the hard turn-off of Q1 determines the soft turn-on of Q2, and the Q1 turn-off time determines the soft-switching transient time.

A strong gate driver capability leads to a shorter miller plateau time and shorter rise time of drain-source voltage of LV Si MOSFET, which is also a shorter fall time of the gate-source voltage of the normally-on GaN HEMT. As a result, the channel of the normally-on GaN HEMT closes quickly. After its channel is closed, a larger load current leads to shorter charging time of the output capacitances and thus faster switching speed. Figure 4-9 plots the gate resistance versus the simulated turn-off loss. Figure 4-10 plots the gate resistance versus the soft-switching transient time, which determines the length of the dead time.

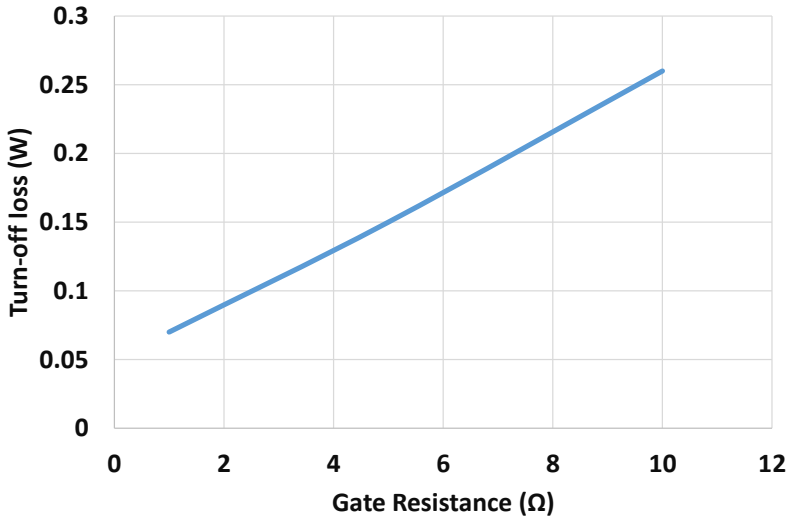


Figure 4-9. Turn-off loss versus gate resistance.

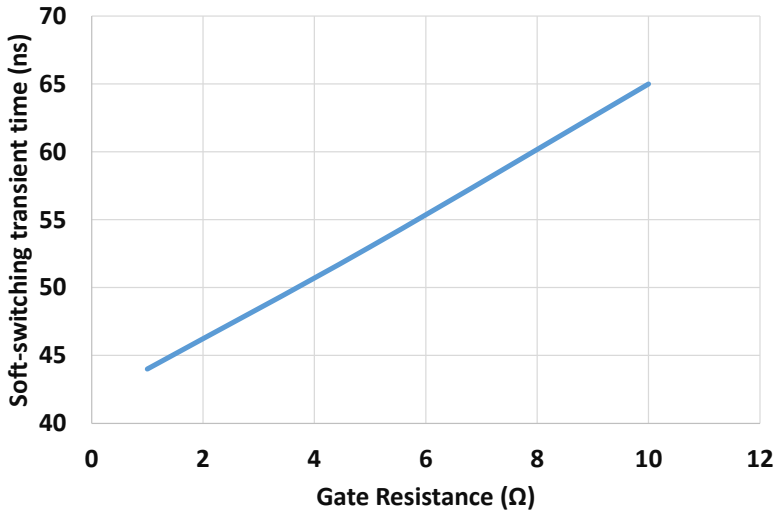


Figure 4-10. Soft-switching transient time versus gate resistance.

4.2.2 Switching Loss during ZVS Turn-on Transient.

The previous analysis showed qualitatively that some switching energy loss will be present on GaN_Q2 during interval III of the Q2 turn-on transient. Based on the switching transient discussion of interval III, the junction capacitance of Q2 is discharged by the load current. $V_{ds\_MOS\_Q2}$ and $V_{ds\_GaN\_Q2}$ are decreasing at the same time. If the sum of the MOS_Q2 output capacitance and the GaN_Q2 input capacitance is lower than the GaN_Q2 output capacitance, $V_{gs\_GaN\_Q2}$ (also the $V_{ds\_MOS\_Q2}$) will quickly reach the pinch-off voltage level, creating the pinch-off clamping phenomenon. A portion of the energy stored in the output capacitance of the GaN_Q2 will be dissipated in the channel when $V_{gs\_GaN\_Q2}$ oscillates near the pinch-off voltage during this time period. Meanwhile, $V_{ds\_GaN\_Q2}$ keeps decreasing to zero.

In order to avoid energy dissipation in the channel, $V_{gs\_GaN\_Q2}$ should be always below the pinch-off voltage before $V_{ds\_GaN\_Q2}$ drops to zero, so that the GaN_Q2 channel remains fully off. A possible solution is to increase gate-source capacitance of the GaN_Q2 or, equivalently, to increase

drain-source capacitance of MOS_Q2 as shown in Figure 4-11. Since the commercial devices used here are enclosed in a PQFN package which includes both devices, and there are no external pins for the gate and drain nodes of the GaN_Q2, the effect of this additional capacitance is analyzed through simulation.

Three different values of capacitance are added in the GaN device model separately, which are paralleled with the gate-source capacitance of the normally-on GaN HEMT. Figure 4-12 shows the simulation results with the original GaN model and different capacitance-added GaN models. With the additional capacitance, the rise time of $V_{gs\_GaN\_Q2}$ is extended. In both the 900 pF case and 2000 pF case, the $V_{gs\_GaN\_Q2}$ remains below the pinch-off voltage until $V_{ds\_GaN\_Q2}$ decreases to zero. Therefore, during t_{2_1}~t_3 interval, the channel of the GaN_Q2 in the off state, and the energy stored in the output capacitance will not be dissipated in the channel. There is no turn-on loss on GaN_Q2. Additionally, the 2000 pF case shows higher off-state voltage of the $V_{gs\_GaN\_Q2}$ (lower $V_{ds\_MOS\_Q2}$), which means the LV Si MOSFET does not reach avalanche during the turn off transient.

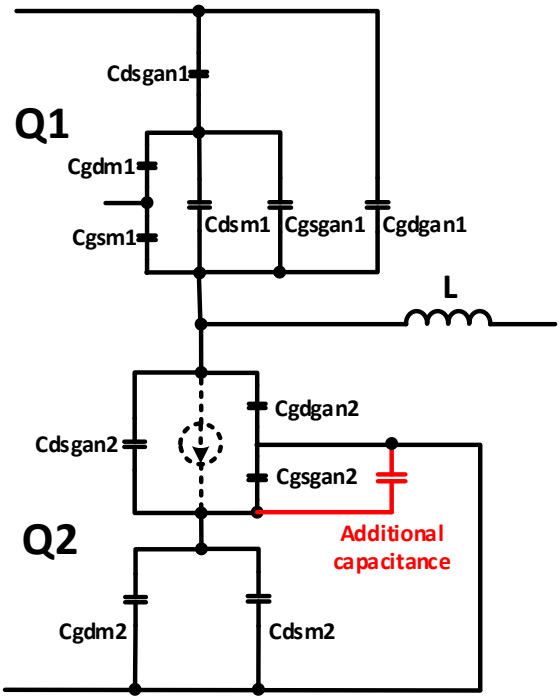


Figure 4-11. Circuit diagram with the additional capacitance.

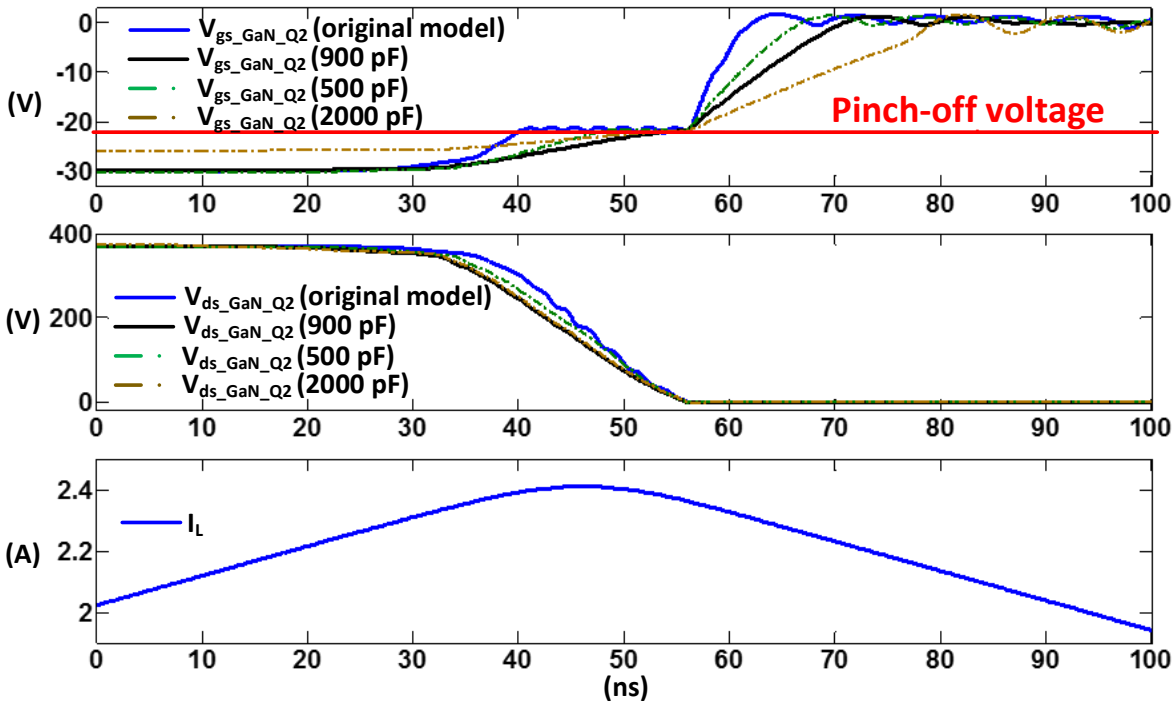


Figure 4-12. Simulation waveforms with different additional capacitance.

4.3 Experimental Verification of Extra Switching Loss in Soft-switching Transient

A thermal test is used to approximate loss in the switching devices during operation. In order to set up a benchmark for the loss evaluation during the switching operation, a relationship between the device power loss and resulting temperature must be established.

As is shown in Figure 4-13, a PQFN packaged cascode GaN HEMT is soldered on a PCB. The device shown is the upper device in the phase-leg structure, and the lower device is on the other side of the PCB. In the thermal test, positive DC voltages are applied on the gate and source nodes of both cascode GaN devices through the gate driver, keeping the devices in on-state. By applying the DC drain current to the device and measuring the drain-source voltage, the device conduction loss can be obtained with the product of drain current and drain-source voltage. Meanwhile, the device surface temperature is measured by a thermal imaging camera. An Agilent E3631A DC power supply supplies the DC drain current, and the drain-source voltage is measured by an Agilent 34410A 6 ½ digit high performance digital multimeter. The temperature is measured by a FLIR SC620 thermal imaging camera. The device is under natural cooling without fan. During the test, the gate-source voltage was kept at 8 V. The drain current was increased from 0.5 A to 2.5 A, resulting in a power loss which increased from 35.1 mW to 1218.75 mW. A thermal image taken at 2.5 A DC current is shown in Figure 4-14. The device surface temperature reaches 88.8 °C. The device loss versus the temperature and the on-state resistance versus temperature are plotted in Figure 4-15 and Figure 4-16. These curves are then used for device loss evaluation under switching operation. The board used for the temperature-loss test is applied in the device switching operation, therefore, there is no significant difference in physical distribution of losses in the temperature-loss test and the switching operation test.

Under exact the same test environment, the prototype shown in Figure 4-13 is operated with an inductor load at 400 V DC input and 1 MHz switching frequency. The gate-source voltage is 8 V and the external gate resistor is 1 Ω. The inductor value was changed to accommodate different inductor peak currents and RMS currents. Figure 4-17 shows the test waveforms at 21 μH inductance with peak current at 2.1 A and RMS current at 1.57 A. During the test, the device is working under the critical ZVS without body diode conduction. The device loss, therefore, can be considered as the combination of the conduction loss, the switching loss and the driving loss on the internal gate resistance. The overall device loss is derived from the device temperature measured by the thermal imaging camera and the loss-temperature relation shown in Figure 4-15.

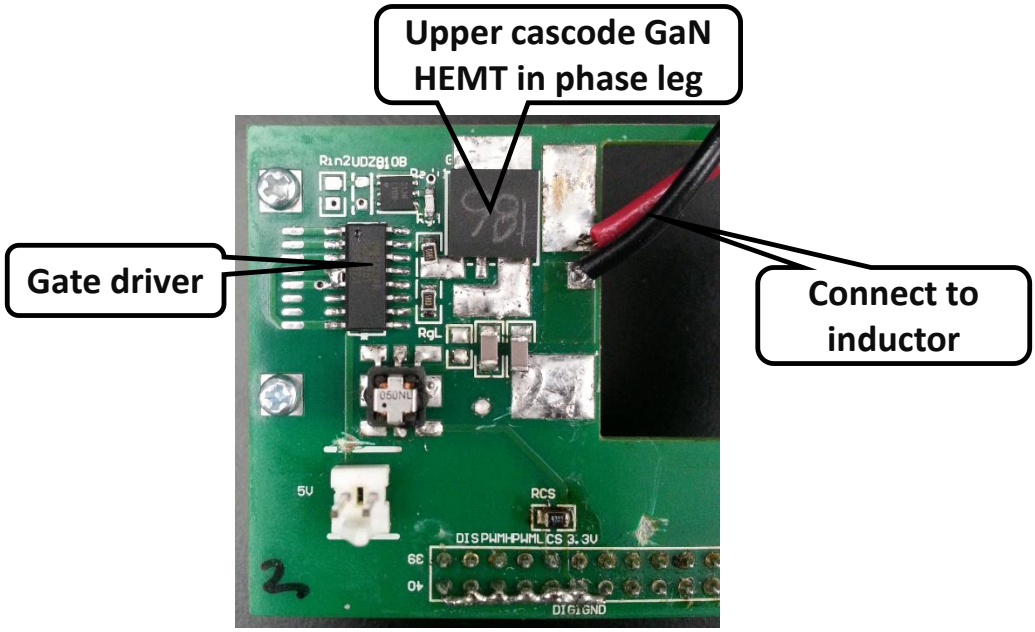


Figure 4-13. Hardware for test.

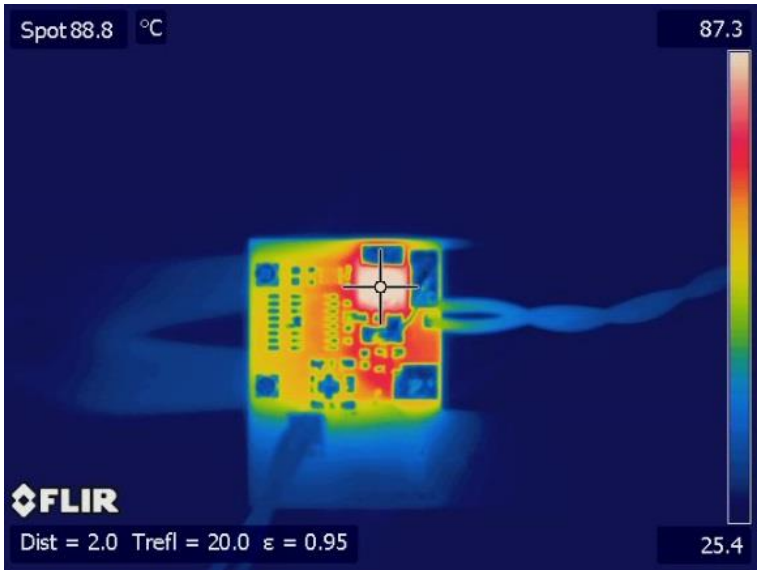


Figure 4-14. Thermal image at 2.5 A DC current with natural cooling.

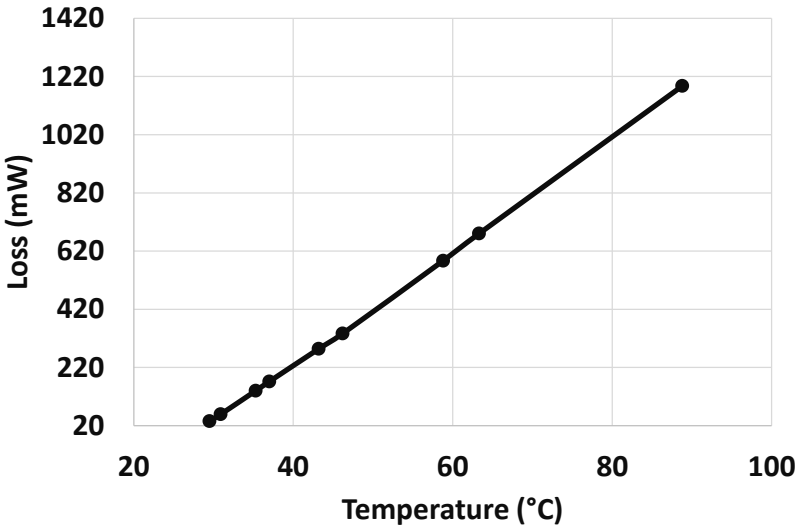


Figure 4-15. GaN device loss versus temperature.

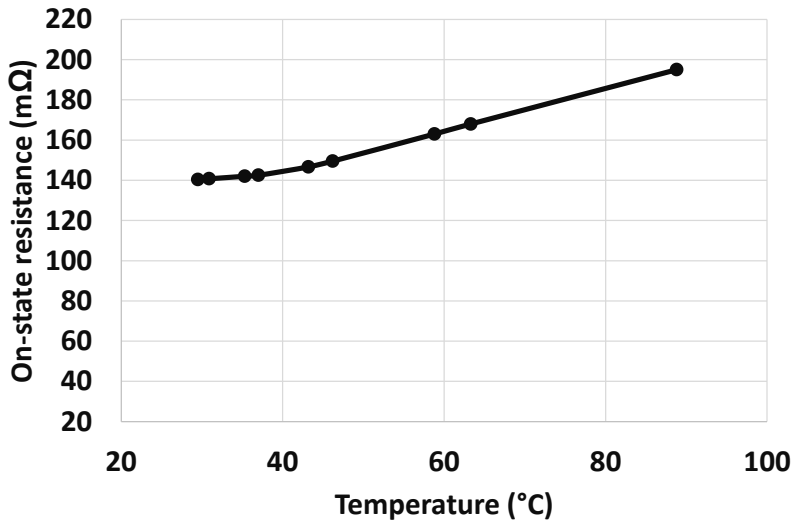


Figure 4-16. GaN device on-state resistance versus temperature.

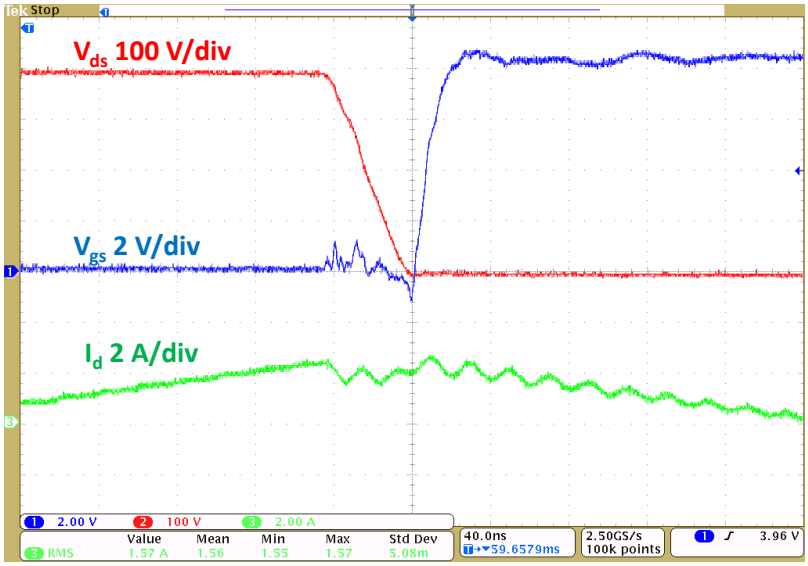


Figure 4-17. GaN device Waveforms at critical ZVS condition.

In order to evaluate the switching loss in the critical ZVS operation mode, it is necessary to obtain the conduction loss and the driving loss first. The conduction loss is determined by the device RMS current and the on-state resistance. The device RMS current is calculated by the inductor RMS current and the device on-time duty cycle, and the on-state resistance is derived from Figure 4-16 at the measured device temperature. Table 4-1 summarizes all the data from the test. The difference between the device loss and the device conduction loss is defined as extra loss, which includes the switching loss and driving loss. Since, for the cascode device, the gate driver is driving a LV Si MOSFET, the driving loss is very small. Based on the device datasheet, the driving loss at 8 V gate-source voltage and 1 MHz switching frequency is 88 mW, therefore, the power dissipation on the device internal gate resistance is about 44 mW since the device inner gate resistance is approximate to the total outer gate resistance. Based on above analysis, the switching loss accounts for about 90% of the extra loss, which is about 400 mW.

Table 4-1. Summary of the GaN test results

Inductor RMS current (A)	Device on-time duty cycle	Device RMS current (A)	Device measured temperature (°C)	Device loss (mW)	Device conduction loss (mW)	Extra loss (mW)
0.925	0.43	0.607	53.6	493.38	54.52	435.35
1.57	0.44	1.04	59.8	613.91	177.50	436.41
1.97	0.45	1.32	66.2	738.33	297.83	440.50
2.66	0.46	1.80	82.4	1053.3	609.83	443.47

In order to further consolidate the findings, a 600 V enhancement mode Si MOSFET is selected to perform similar thermal test in the soft-switching transient. Since the Si MOSFET is not in a cascode structure, the measured loss in the critical soft-switching condition only includes the conduction loss, turn-off loss, and the driving loss on the device internal gate resistance. A Si

MOSFET of the same PQFN package of GaN HEMT from TOSHIBA is selected to have the similar thermal features with cascode GaN HEMT. The devices are shown in Figure 4-18. The device parameters are shown in Table 4-2.

Based on the GaN test approach discussed above, the Si MOSFET is tested on the same board and configuration with the natural cooling. The loss versus temperature curve is plotted in Figure 4-19. Similarly, the Si device is tested under critical ZVS condition at 1 MHz. The device total loss is measured by the temperature and estimated by the relations in Figure 4-19. The test results are shown in Table 4-3. The device has gate charge at 30 nC at gate-source voltage of 8 V, and the inner gate resistance is 6 Ω. In the test circuit, the total external gate resistance is 3 Ω, therefore two thirds of driving loss, which is about 160 mW, are dissipated on the device itself. The turn-off loss is measured by the double pulse test. With the compensation of energy stored in the output capacitance, the turn-off loss energy dissipated in the channel is about 0.072 μJ/A. At 1 MHz switching frequency, it is about 72 mW/A. As can be seen in the Table 4-3, the extra loss is positive for the first test point and negative for the next three test point. The absolute value is lower than 1.1% of the measured total device loss. The conclusion is that for the enhancement Si MOSFET, there is no extra turn-on loss dissipated on the device.

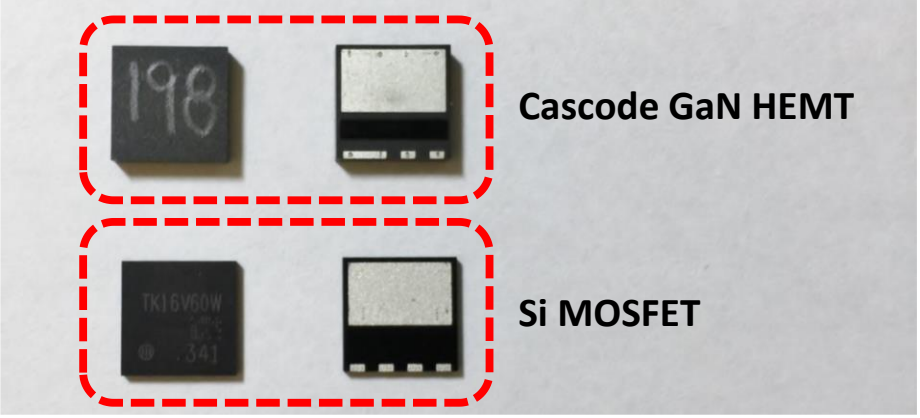


Figure 4-18. Cascode GaN HEMT and Si MOSFET in the test.

Table 4-2. PQFN GaN and Si parameters

	Voltage rating (V)	Rdson (mΩ) @25 °C	Charge equivalent output capacitance (pF)	Gate charge (nC)
TK16V60W (Si)	600	160	296 @400V	30
TPH3006PS (GaN)	600	150	115 @400V	9.3

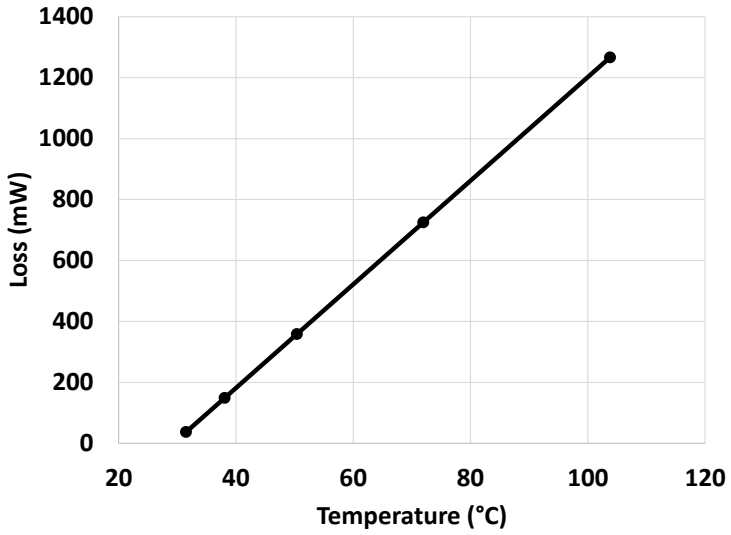


Figure 4-19. Si device loss versus temperature.

Table 4-3. Summary of the Si test results

Inductor RMS current (A)	Device on-time duty cycle	Device RMS current (A)	Device measured temperature (°C)	Device loss (mW)	Device conduction loss (mW)	Extra loss (mW)
0.58	0.4	0.38	44.6	260.1	25.25	2.85
1.15	0.41	0.77	53.1	404.5	101	-0.50
1.73	0.42	1.15	65.3	611.9	238.16	-2.26
2.31	0.43	1.54	82.4	902.6	455.75	-1.15

4.4 Summary

The soft-switching behavior of the cascode GaN HEMT was investigated in detail in each switching interval. Several interesting phenomena of cascode devices have been discussed. The channel current drops to zero quickly during the turn-off transient due to the internal feedback of the cascode structure, which leads to extremely small turn-off loss. On the other hand, there is switching energy loss on the internal normally-on GaN HEMT during the device ZVS turn-on transient, although the external waveforms of the cascode GaN HEMT exhibit ZVS. By increasing the gate-source capacitance of the internal normally-on GaN HEMT, it has been observed through simulation that these additional losses can be mitigated.

Since it is not possible to experimentally measure the channel current of the internal normally-on GaN HEMT independent of the parasitic capacitances, thermal tests are used to evaluate the switching loss. The tests were conducted in four different inductor current cases at 1 MHz switching frequency. The switching loss accounts for about 90% of the extra loss, which is about 400 mW.

In order to have deeper insight on the switching loss in the soft-switching transition, future work should focus more on the quantitative analysis based on the analytical model. Meanwhile, it is also valuable to study the operation condition dependency of the switching loss in the soft-

switching transition based on different switching frequencies, different load current and different DC bus voltage. Finally, it is observed that adding additional capacitance may be able to reduce losses in the internal GaN HEMT during a ZVS transition.

5 Magnetics Consideration for Efficiency Improvement of LLC Resonant Converter

This chapter discusses two magnetic related topics. The first topic is about an improved LLC resonant converter design method with optimal dead time selection considering transformer winding loss. A new perspective of extra winding loss due to the asymmetrical primary side and secondary side current is proposed in Chapter 3. The extra winding loss is related to the phase difference between the primary side and secondary side current, then it can be related to the device parameters and dead time. Therefore, the LLC resonant converter design method should also consider the transformer winding loss. In the second topic, a new design method will be proposed on applying an optimal designed external inductor in the resonant tank rather than using the transformer magnetizing inductance. By applying the external inductor and removing the air gap in the transformer, the asymmetrical current induced transformer winding loss and the fringe effect induced transformer winding loss can be minimized. Since the external inductor only processes a small amount of the circulating power rather than the entire power, the additional size and loss are low. The design and loss analysis of the external inductor will be discussed. The test results and the efficiency improvement will be presented.

5.1 Improved LLC Design Method Considering Transformer Winding Loss

The classical LLC resonant converter design flow chart is shown in Figure 5-1. When the converter specification is determined, several aspects need to be considered in order to get a high efficiency and high power density LLC resonant converter design. The transformer turns ratio is easy to obtain for the unregulated LLC resonant converter, since the converter behaves as a DC-DC transformer at resonance. Therefore, the input and output voltage ratio is the transformer turns

ratio. The switching frequency determines the transformer size and weight. High switching frequency will have smaller transformer size, however the transformer winding loss will be increased due to the fringe effect loss and terminal loss. Meanwhile, the reduced transformer size will also bring less winding area and high winding resistance. From the device point of view, high switching frequency results in high driving loss. Additionally, the device conduction loss will be increased. The reason is that the dead time period will account higher portion of the switching period, reducing the effective energy transfer time, leading to higher RMS current. Based on the power efficiency and density requirement, several switching frequency candidates can be selected. For each switching frequency, several device candidates are selected, and then based on the loss model and analysis discussed in Section 3.2 and 3.3, the dead time and the magnetizing inductance are selected. The transformer design is another significant part. The core material is selected based on the switching frequency and core loss. The power density requirement is the constraint of the core size. The winding design need to reach the goal of the low winding loss and the copper area or the PCB winding thickness is also impacted by the core window area. There will be some iterations in the transformer design. When the core size is fixed, the core air gap determines the magnetizing inductance value L_m. The resonant inductor L_r is realized by the transformer leakage inductance which is determined by the winding structure. Fortunately, in the unregulated LLC resonant converter, there is no strict requirement to design the L_r, due to no strict requirements on the output voltage regulation during the normal operation condition. For whatever L_r, a C_r is selected to fit the resonant frequency to the switching frequency. Then, the L_m and L_r combination are checked to ensure the ability to meet the hold-up time regulation requirement. If not, other solutions should be investigated to change the L_r. When the designs at different switching

frequencies are finished, compare the different results and pick one that best fit the efficiency and power density requirement.

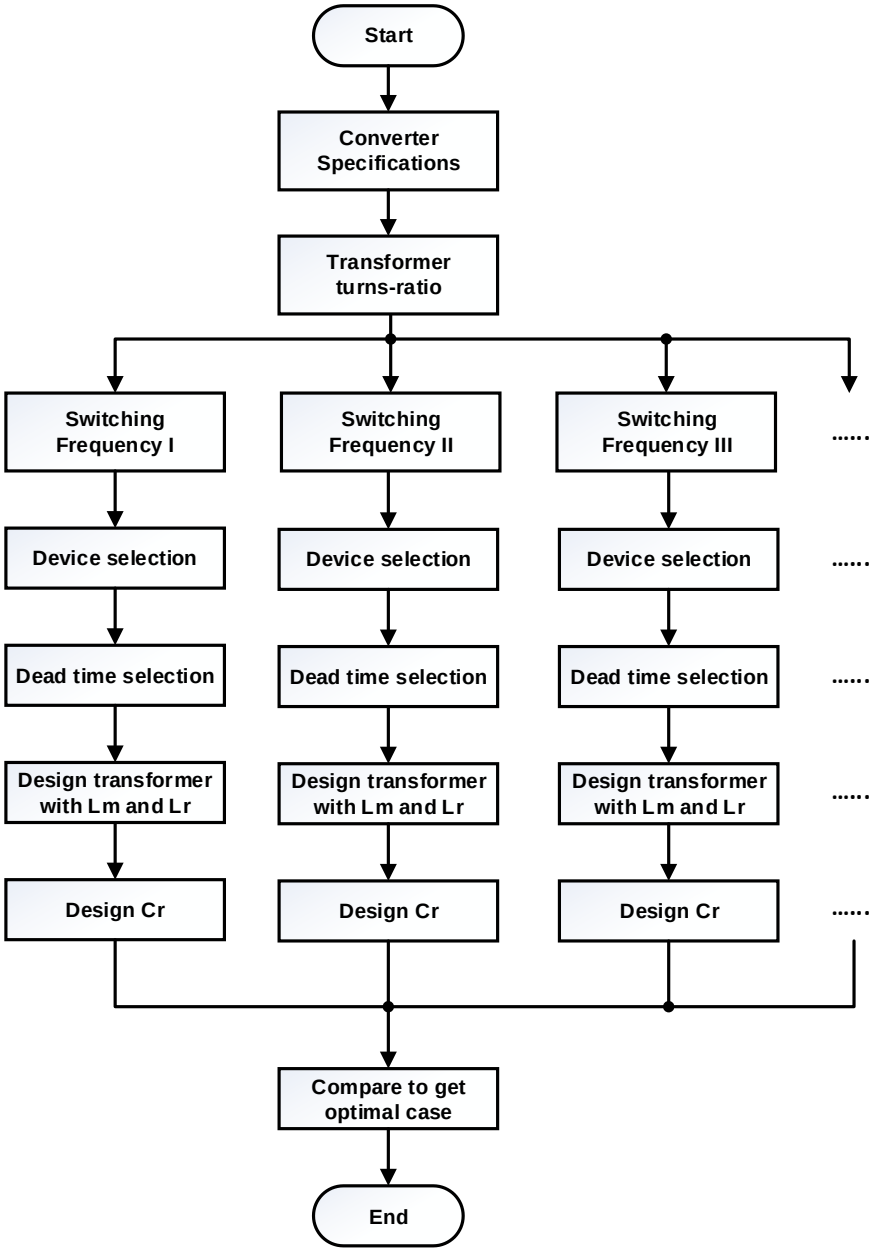


Figure 5-1. Classical unregulated LLC resonant converter design flow chart

The discussion in Section 3.5 propose a new perspective on the extra winding loss which is due to the asymmetrical primary side and secondary side current, where a phase shift Φ_d exists. The numerical relationship between the Φ_d and the winding loss of a predetermined transformer can be derived from the FEA simulation results, shown in Figure 3-39. After applying (3-28) and (3-29), the winding loss is connected with the dead time based on the Si and GaN devices, shown in Figure 3-40. Combining the dead time related RMS current from Section 3.2 and the dead time related winding loss from section (3.5), an improved LLC resonant converter design approach with optimal dead time selection considering both device loss and winding loss will be discussed.

Assuming the pre-selected devices, the dead time related total loss is express as,

$$P(t_d) = I_{priRMS}(t_d)^2 R_{dson\_pri} + I_{secRMS}(t_d)^2 R_{dson\_sec} + P_{winding}(t_d) \qquad (5\text{-}1)$$

where I_{priRMS} is the primary side RMS current; I_{sec_RMS} is the secondary side RMS current; R_{dson_pri} is the primary side device on-state resistance; R_{dson_sec} is the secondary side device on-state resistance; $P_{winding}(t_d)$ is the dead time related winding loss. Based on this equation, for pre-selected devices, the minimum device conduction loss and winding loss can be derived with the optimal dead time. For an optimal converter design, different devices can be applied then.

In the classical design of LLC resonant converter in Figure 5-1, $P_{winding}$ is usually considered as constant during the selection of t_d when the winding geometry and operation frequency are fixed. However, according to Figure 3-40, since the Φ_d changes with different dead time, it also has impact on the pure winding loss, and the Φ_d is fundamentally determined by the device parameters and dead time. Based on the (5-1) shown above, Figure 5-2 and Figure 5-3 plot the sum of the device and winding loss with constant pure winding loss and dead time dependent pure winding loss respectively. In Scenario I in the Figure 5-2, the pure winding losses in two cases are derived when Φ_d is equal to zero, since usually Φ_d is not considered in the winding loss calculation. In the

Scenario II, the pure winding losses are obtained from Figure 3-40 at the points where t_d equals to 80 ns for GaN and 130 ns for Si. The loss in Scenario I is apparently underestimated. The optimal dead time point in Scenario II will be considered as the lowest device loss point in the classical design method. In fact, no matter how much the pure winding loss is considered during the design procedure, optimal dead time point is always around 80 ns for the GaN case and 130 ns for the Si case. However, if the dead time depended pure winding loss is considered during the design, the dead time is further extended and the sum of the loss is lower than that in Figure 5-2 Scenario II, as depicted in Figure 5-3. As mentioned before, larger dead time results in smaller effective energy transfer time from input to load, resulting in higher RMS current and higher loss. But the pure winding loss reduction caused by the increase of t_d (decrease of I_{Lmpeak} and Φ_d) overcomes that. As a result, the real optimal dead time point is about 120 ns for GaN case and 150 ns for Si case.

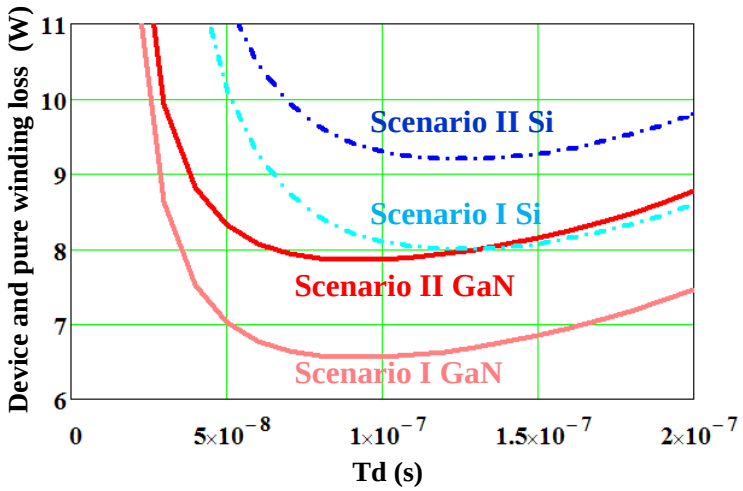


Figure 5-2. Device and winding loss versus dead time with constant winding loss.

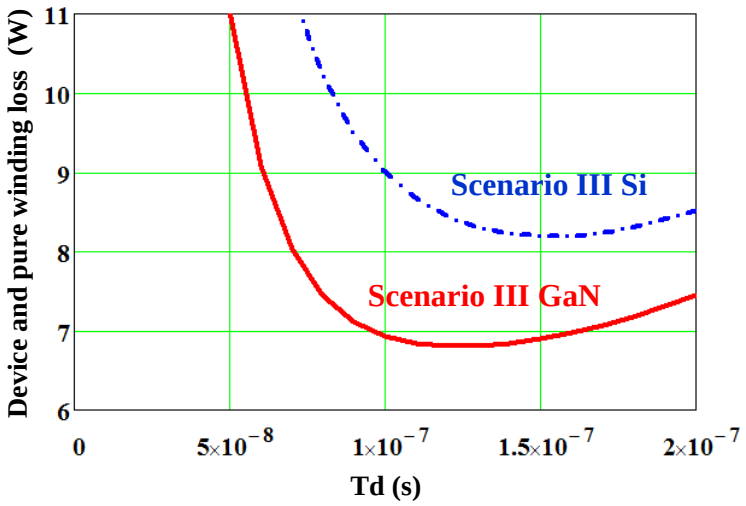


Figure 5-3. Device and winding loss versus dead time with dead time depended winding loss.

The above example explains how the dead time dependent winding loss impacts the optimal dead time selection during the design to pick the minimum loss point. The design procedure is summrized as follows,

1. Different from the classical design procedure shown in Figure 5-1, after the switching frequency is picked, the transformer core size and winding size should be determined first, since the relationship between winding loss and dead time is based on a predetermined transformer. Usually, in the DC-DC converter module design, the transformer size is limited by the converter size or the power density. There are also industry standards for the converter module such as one quarter brick, eighth brick and sixteenth brick. Therefore the transformer size selection is narrowed down, even with the customized designed core. But the transformer design iteration mentioned in the classical design procedure will also happen. In order to simplify the design, the Φ_d impact is not necessary to consider in this step,

2. Determine the winding loss-Φ_d curve by using FEA simulation or some analytical approximate solution. And then derive the winding loss-dead time curve or expression.
3. Select different device candidates for the design and comparison.
4. Combine the device loss-dead time curve and the winding loss-dead time curve to derive the overall loss-dead time curve, and select the optimal dead time, which considers both the device loss and dead time depended winding loss.
5. After deriving the dead time, the value of magnetizing inductance can be obtained, and the air gap can be calculated based on the core.
6. Obtain the L_r and C_r based on the switching frequency equal to resonant frequency.

The improved design method by considering both the device and winding loss is shown in Figure 5-4.

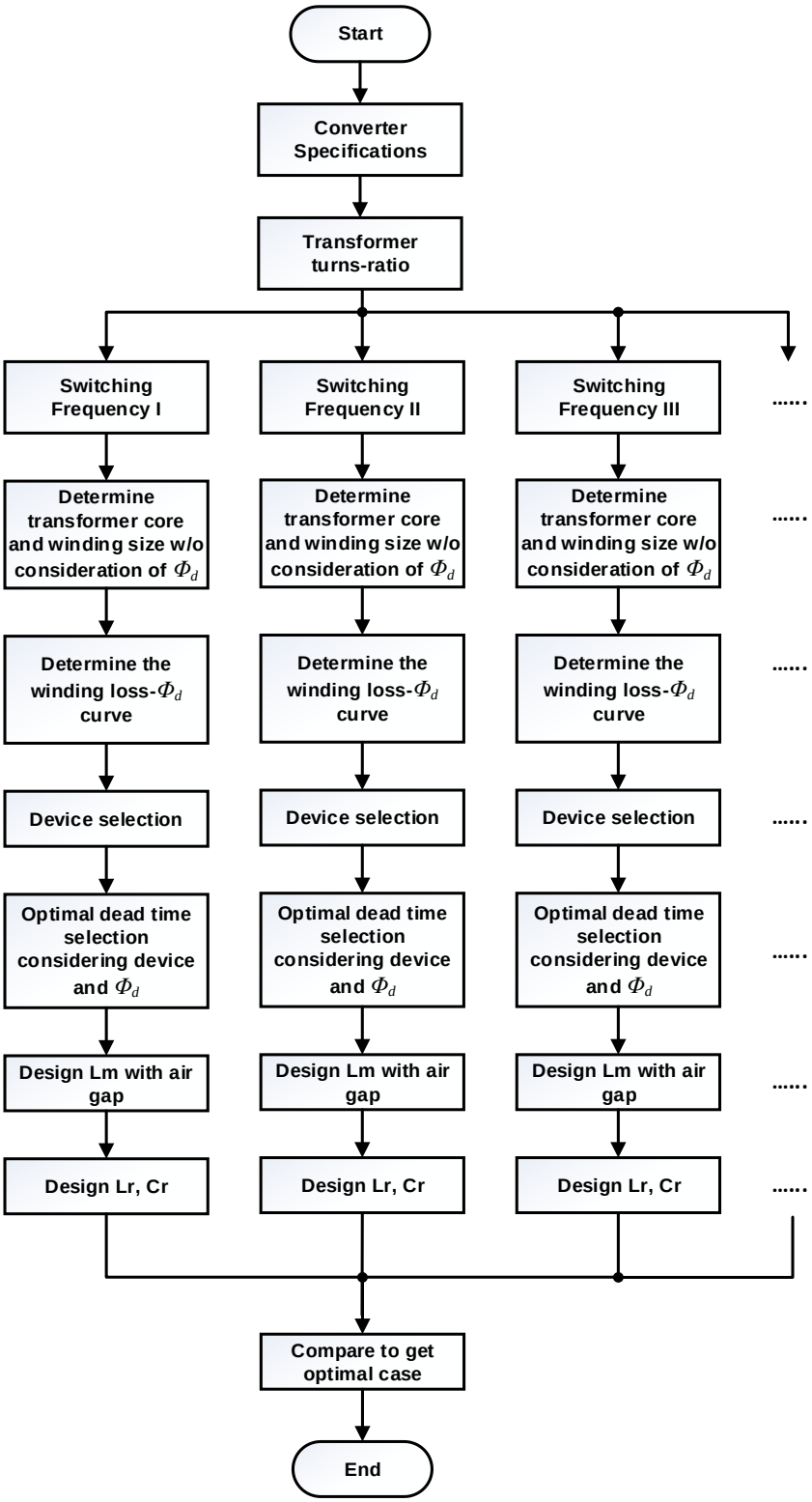


Figure 5-4. Improved LLC converter design approach with optimal dead time selection considering both device loss and winding loss.

5.2 External Inductor for Efficiency Improvement

According to the literature review and analysis in Section 2.1.2, there are some drawbacks when the inductor in the resonant tank utilizes the transformer magnetizing inductance. First, the large air gap is necessary to achieve low magnetizing inductance and high peak magnetizing current for ZVS operation. When the transformer winding is close to the air gap, fringe effect loss will be induced, which becomes severe for the high frequency and high current condition. The solution to the fringe effect loss is usually either to arrange the windings far away from the air gap or use the distributed air gap core. These will increase the complexity of the LLC transformer design and implementation. The FEA simulation derives the fringe effect loss in the transformer of the 300 W LLC resonant converter discussed in Chapter 3 is about 2.3 W.

Another drawback is the extra winding loss due to the asymmetrical primary and secondary side current. Since the magnetizing current exists, there is a phase different between the primary side and secondary side winding. Even in the interleaving winding structure, the *H* field cannot be cancelled, resulting in extra winding loss. FEA simulation results prove that there is about 1.3 W extra winding loss in the transformer based on Figure 3-39 in Section 3.5. Therefore, the overall loss from these two drawbacks is about 3.6 W.

It is interesting to investigate if the total magnetic component loss can be reduced when the LLC resonant tank inductor is extracted from the transformer. The topology of the external inductance based LLC resonant converter is shown in Figure 5-5. L_m is extracted from the transformer, therefore the transformer air gap can be removed, and the magnetizing current is negligible. The primary and secondary side current are symmetrical. Then the interleaving winding structure can help to reduce the eddy current effect winding loss. Based on the above analysis, 3.6

W of winding loss can be minimized. But the external AC inductor will have additional loss. Thus, the design of the external AC inductor needs to be optimized.

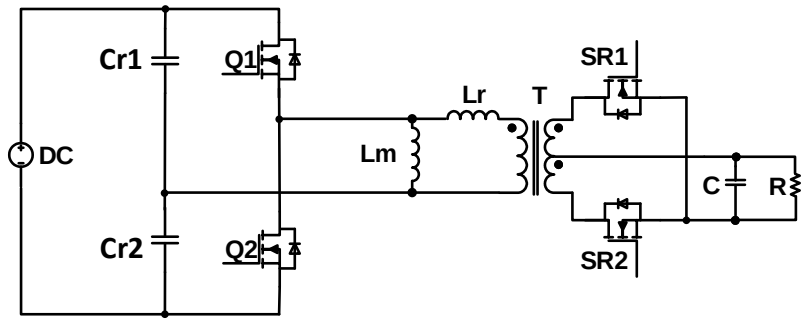


Figure 5-5. Unregulated LLC resonant converter with extraction of L_m.

The AC inductor is widely applied in the PWM or resonant DC-DC converters to help ZVS realization of the devices. The inductor core B-H operation range is in the first and third quadrant, which has both positive and negative swings, shown in Figure 5-6. The transformer magnetizing inductance in the LLC resonant converter has the similar operation function. However, since the transformer core needs to process the entire power of the converter, the core window area needs to be large enough. The turns of transformer winding are constrained by the turns ratio, but for the external AC inductor, the winding turns are more flexible. The core flux density ΔB is also flexible for the AC inductor design. The core window area can be also reduced because the inductor only process the primary side current for the device soft-switching. The specification for the AC inductor in this design is shown in Table 5-1.

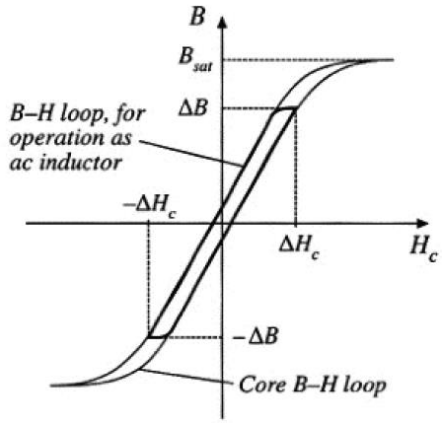


Figure 5-6. AC inductor B-H operation region [81].

Table 5-1. AC inductor Specifications

Inductance	20 uH
Switching frequency	1 MHz
Maximum current	2.2 A
RMS current	1.5 A

The *Core-Window Area Product* inductor design method is applied. There are three physical constrains for this method, which are the core cannot be saturated; the wire area is limited by the current density; and the wire must fit through core window. Considering these three physical constrains, the equation is expressed as,

$$A_e W_a > \frac{I_{rms} I_{max} L}{K_u J_{max} B_s} \tag{5-2}$$

where A_e is the core effective area; W_a is the core window area; I_{rms} is the RMS current flowing through the winding; I_{max} is the maximum current; L is the inductor; K_u is the winding fill factor; J_{max} is the maximum current density; B_{max} is the maximum flux density. K_u is considered as 0.65 for this solid wire winding inductor. The variables are the core geometry, the maximum current

density and the targeted flux density. The AC inductor design flow chart is shown in Figure 5-7. The current density is considered as the outer iteration loop. For each current density, several flux densities will be considered in the inner iteration loop. For each flux density, different core geometries are applied. Here, the core geometry can be customized as well, but the selection of standard core geometries from manufactures are versatile enough. Then, based on the flux density and the specifications, the core air gap and number of turns are defined. The wire gauge is considered along with the core fill factor to determine the standard wire gauge for the inductor winding. After that, the core loss and winding loss are calculated. After the flux density and current density iteration loops are done, there will be different design results. The optimal design will be assessed by considering the acceptable loss and size. Then the optimal AC inductor design is finished.

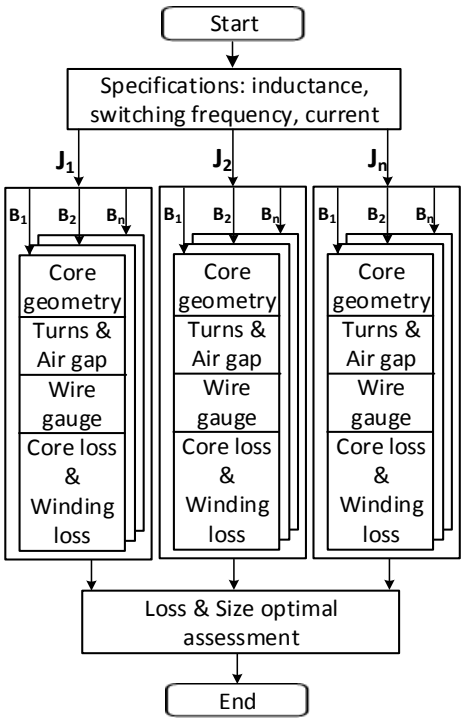


Figure 5-7. AC inductor optimal design flow chart.

Figure 5-8 shows the design results for different targeted flux densities when the allowable current density is below 9 A/mm^2. As can be seen, the available cores for 0.05 T flux density are fewer than for 0.1 T flux density. This is because some of the cores do not satisfy (5-2) when the flux density is low. However, according to Figure 5-8, these cores feature lower core loss and smaller core size of the AC inductor. When the targeted flux density increases to 0.2 T, the total loss of the same size of the inductors increases a lot due to the increased core loss.

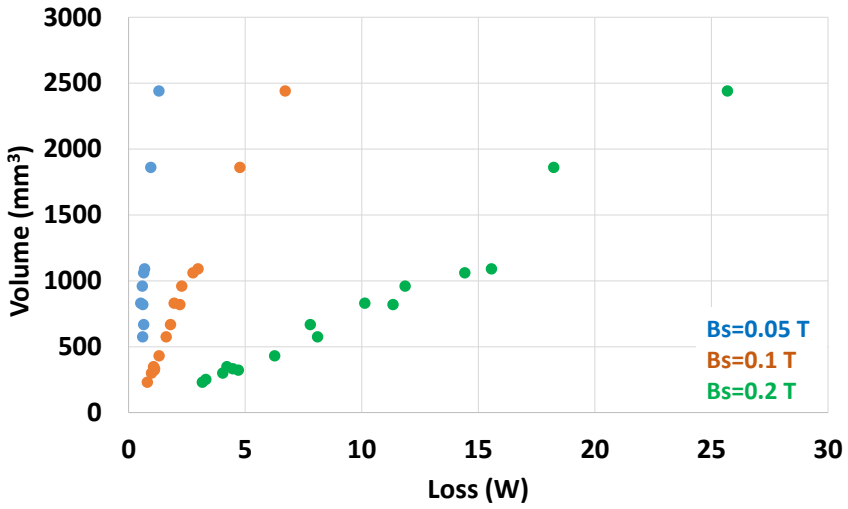


Figure 5-8. Design results for different flux densities.

Based on the design result shown in Figure 5-8, the AC inductor design results are shown in Table 5-2. The calculated core loss is 0.7 W and the calculated winding loss is 0.4 W. The LLC resonant converter hardware with the external inductor is shown in Figure 5-9. The external inductor is in parallel with the input of the transformer, which is only one fourth of the size of main power transformer. Based on the analytical results, the loss that the external inductor brings is about 1.1 W. Therefore, the total loss reduction is 2.5 W. The efficiency comparison for the GaN

LLC prototype with external inductor and without external inductor are shown in Figure 5-10. At full load condition, the efficiency improvement or the loss reduction is about 0.5%, which is equal to 1.5 W. It is lower than the analytical value. Part of the reason is that, as shown in Figure 5-9, the external inductor is built of the solid wire. It is difficult to wind the wire far away from the air gap. Therefore, the fringing effect loss is induced. A PCB winding that the winding thickness can be perfectly controlled is preferable to avoid the air gap and obtain more loss reduction for the external inductor.

Table 5-2. AC inductor design results.

Inductance	20 uH
Switching frequency	1 MHz
Core material	3F4
Core type	ER14.5/3/7
Air gap	0.7 mm

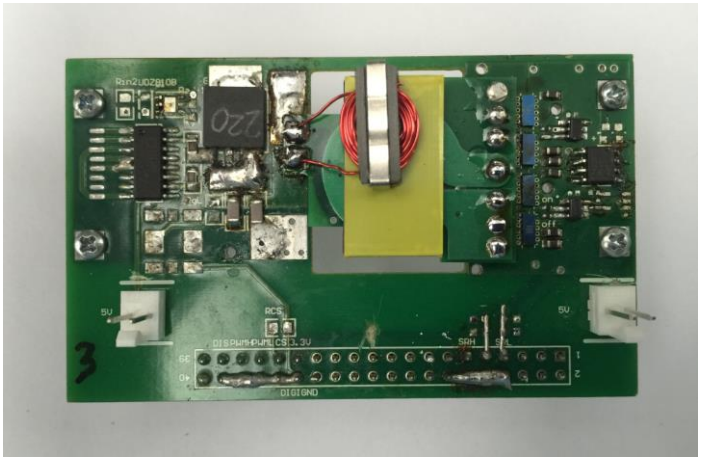


Figure 5-9. LLC resonant converter hardware with external inductor.

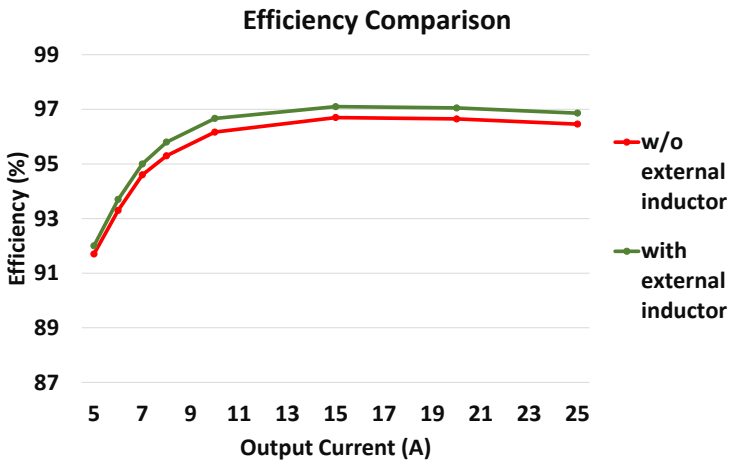


Figure 5-10. LLC resonant converter hardware with external inductor.

5.3 Summary

An improved LLC resonant design method with an optimal dead time selection that considers both the impact of device loss and winding loss is proposed. Adding to the classical design method that only consider the device loss in the dead time selection, the improved design method also considers the extra winding loss induced by asymmetrical primary side and secondary side current. A design of extracting the magnetizing inductance out of the transformer is proposed to reduce the transformer winding loss. Since the external inductor only deals with the circulating current in the primary side instead of the entire power of the converter, the inductor size is small, which is only one fourth of the size of main power transformer. The benefit is that the transformer without the air gap can reduce the winding loss due to the elimination of the fringing effect and asymmetrical primary and secondary side current. An external inductor is design and built for the GaN based LLC resonant converter. The test results on the efficiency demonstrates about the 0.5% efficiency improvement.

6 Development of Integrated DC-DC Converter in EV Application

Chapter 3 to Chapter 5 discuss the design method and loss model for the LLC resonant converter efficiency improvement using advanced device and magnetics technologies. This chapter presents a novel integrated DC-DC converter for electrical vehicle (EV) application. In the state of the art power conversion architecture in EV nowadays, the on-board charger and powertrain converter are designed and operated separately, which induces extra cost, size and weight of the power electronics under the hood. A novel DC-DC converter that integrates the isolated DC-DC converter in the on-board charger and the powertrain DC-DC converter are proposed. The converter operates as both boost converter and dual active bridge (DAB) converter. That the boost converter serves as the drivetrain converter and the DAB converter serves as the isolated converter for the on-board charger. A dual function magnetic component serves both the inductor of the boost converter and the transformer of the DAB converter. Furthermore, the traditional drivetrain DC-DC converter (boost converter) is usually designed for full load, suffering from poor efficiency at light load and high voltage step-up ratios. A new operation approach is proposed for the integrated converter, with the DAB used in traction drive mode so that the converter can cover the light load and high voltage step-up region with high efficiency. A general design approach and loss model are presented in this chapter. The test results are shown after that verifying the benefits of the DAB converter in the traction drive mode.

6.1 Integrated DC-DC Converter Topology

The state of the art power conversion architecture in EVs is based on the separate converter function blocks, shown in Figure 6-1. Each block realizes its function independently. In the traction drive system, a bidirectional DC-DC converter is applied as the interface between the battery pack and the motor drive inverter. This DC-DC converter serves to increase the battery pack voltage to

a higher regulated DC bus voltage, so that this configuration allows the decoupling of battery and motor, and increases the operating range and efficiency of the traction drive system. The bidirectional DC-DC converter is required to be robust, small, and high efficiency. It should increase the overall system efficiency without sacrificing size and weight of the traction drive system. The on-board battery charger is another significant part in the EV. There are several power conversion processes in the charger. The AC input voltage is rectified to the unregulated DC voltage, which then goes to the power factor correction DC-DC converter to have the regulated DC output voltage, while the input AC power quality requirement, such as the power factor and THD, is satisfied. After that, the DC voltage is galvanically isolated with the battery side voltage through an isolated DC-DC converter. In the state of the art power conversion architecture, the drivetrain DC-DC converter and the on-board charger are usually separated in different locations, which result in extra cost, size and weight of the power electronics under the hood. Therefore, it is preferable to combine the two power converters together. As can be noticed in Figure 6-1, the drivetrain DC-DC converter and the on-board charger share the same battery voltage V_{HVB}. If the input DC voltage in the charger V_R can share with high voltage DC bus in the powertrain V_{HV}, the drivetrain DC-DC converter can share some of the components with the on-board charger. Therefore, an integrated DC-DC converter can be realized.

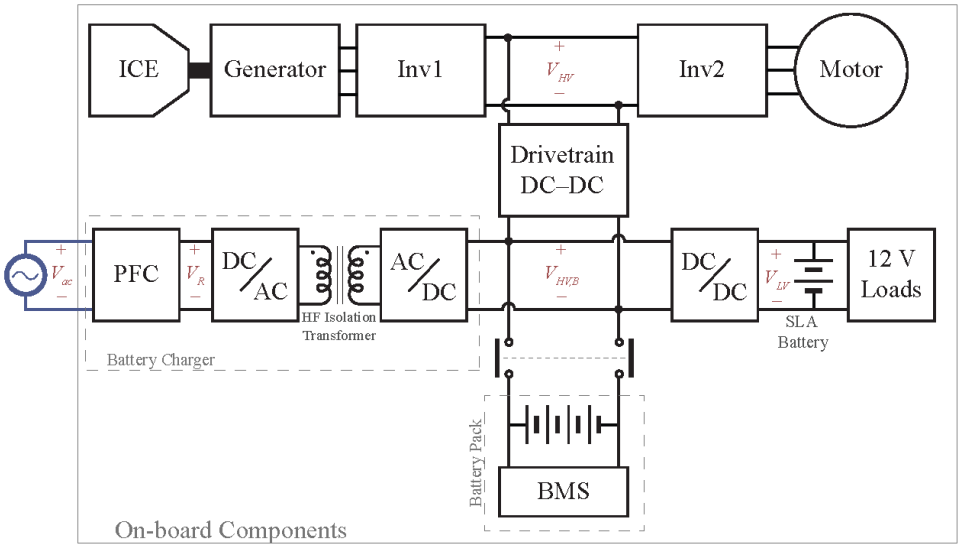


Figure 6-1. State of the art power conversion architecture.

An integrated DC-DC converter topology is proposed in Figure 6-2. The contactors K_1 and K_2 are already part of the battery and control the converter operation mode. Figure 6-3 shows the integrated DC-DC converter in the traction drive mode. The auxiliary switches *K1* and *K2* are on. *S21*, *S22* and *L1* constitute one boost converter, and *S23*, *S24* and *L2* constitute a second paralleled boost converter. The two boost converters can be controlled in the interleaved scheme so that the equivalent current ripple to the battery can be reduced. In other words, the current ripple requirement can be met with smaller inductances than with a single converter. Figure 6-4 shows the integrated DC-DC converter in the on-board charger mode. The auxiliary switches *K1* and *K2* are off. The integrated converter changes into an isolated DAB DC-DC converter, which regulates the output voltage from the input high voltage DC bus. The power flows from the high voltage DC bus to the battery.

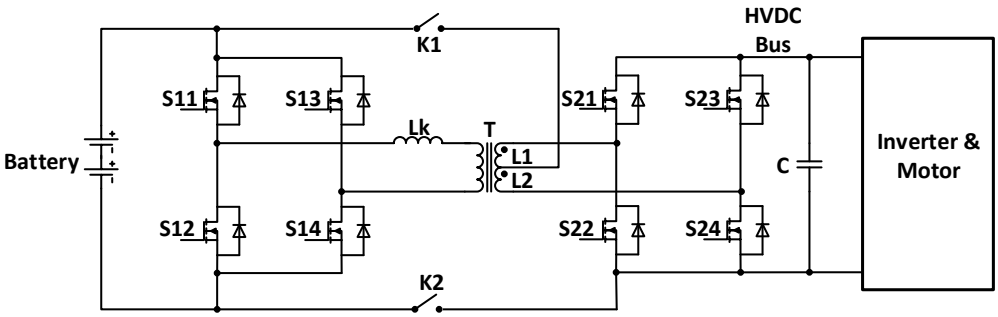


Figure 6-2. Integrated DC-DC converter topology.

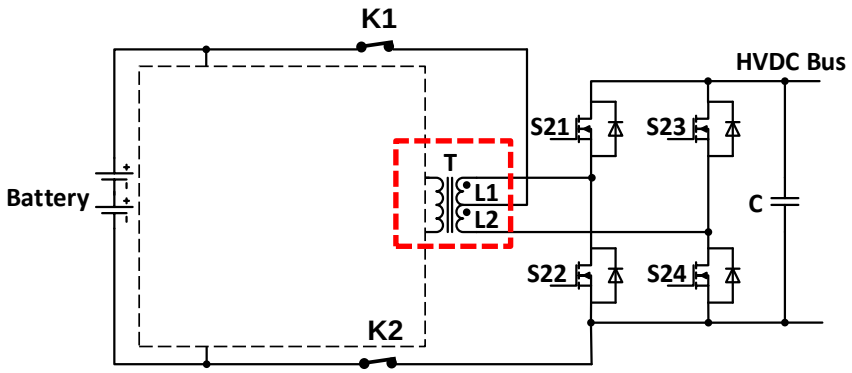


Figure 6-3. Integrated DC-DC converter in traction drive mode.

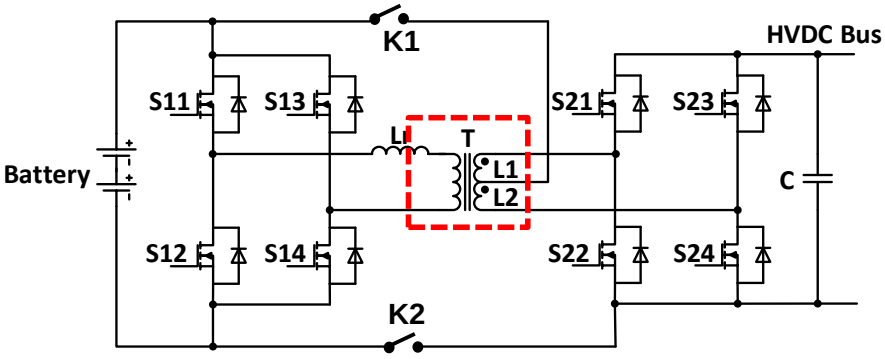


Figure 6-4. Integrated DC-DC converter in on-board charger mode.

The objective of the research work in this chapter is to develop a general design methodology and loss model for the proposed integrated DC-DC converter. It can also improve the efficiency for the light load and high voltage step-up condition of the traditional drivetrain DC-DC converter by operating as a DAB converter with the power flowing from the battery to the HVDC bus. The power rating of the state of the art drivetrain DC-DC converter, such as 2010 Prius, is 27 kW [106]. The commercially available on-board charger is usually rated at 3.3 kW or 6.6 kW. In this research work, a scale-down integrated DC-DC converter is considered for the design in order to verify the proposed topology, design methodology and the loss model. The specifications are shown in Table 6-1 and Table 6-2.

Table 6-1. Specifications of boost converter in traction drive mode

Input voltage	200 Vdc
Output voltage	260-500 Vdc
Current ripple	below 40% of average input current (peak-to-peak)
Power rating	2.5 kW

Table 6-2. Specifications of DAB converter in charger mode

Input voltage	450 Vdc
Output voltage	200 Vdc
Power rating	660 W

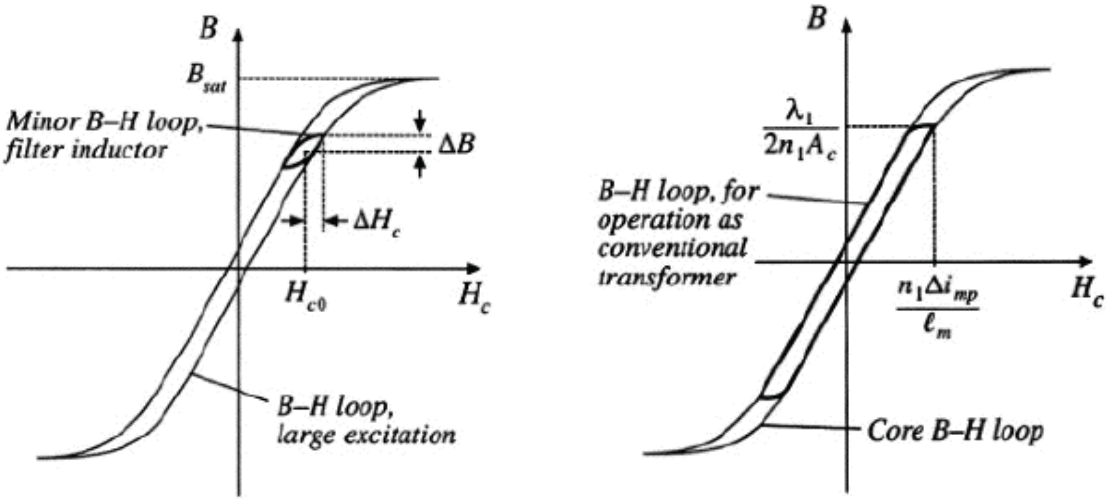
6.2 Design Consideration for Dual Function Magnetic Component.

6.2.1 Worst Case Consideration

One of the design challenges of the integrated DC-DC converter is the dual function magnetic component indicated by the red dashed boxes in Figure 6-3 and Figure 6-4. The boost inductor

utilizes the magnetizing inductance of the transformer. The voltage and current excitation to the boost inductor and the DAB transformer are different, therefore the magnetic operation regions are different. A good dual function magnetic component design will take the magnetic operation regions in both converters into consideration. In addition to the voltage and current excitation, the power processing capabilities of the dual function magnetic component in different operation modes are different because the power rating of the traction driver converter is usually higher than the on-board charger.

The difference between the inductor and transformer is that the flux density-magnetic field curve (*B*-*H* curve) of the inductor operates in the first quadrant of the *B*-*H* plane with a DC bias, but the *B*-*H* curve of the transformer operates in the first and third quadrants, as shown in Figure 6-5 [81]. The design of the dual function magnetic component can start with a transformer design and let the boost inductor to stay within the peak flux density or start with a boost inductor design and let the transformer to stay within the peak flux density. Therefore, the first step is to estimate the worst case operation in terms of the peak flux density to avoid the core from saturation.



(a) B-H curve for the inductor (b) B-H curve for the transformer

Figure 6-5. B-H curve operation regions [81].

For the *n*-turn magnetic component, Faraday's Law can be expressed as:

$$v = n\frac{\Delta\Phi}{\Delta t} \tag{6-1}$$

When it is applied in the transformer, the expression will be:

$$V_{in} = n\frac{2*B_{tr\_max}A_e}{D_{tr\_max}\frac{T_S}{2}} \tag{6-2}$$

and we have:

$$B_{tr\_max} = \frac{V_{in\_tr}D_{tr\_max}}{4nA_ef_s} \tag{6-3}$$

where V_{in_tr} is the transformer input voltage; B_{tr_max} is the max flux density; D_{tr_max} is the duty cycle; f_s is the switching frequency; A_e is the effective area of the core; n is the turns.

For the inductor, assuming it is an inductor with air gap, we have

$$LI_{peak} = nB_{L\_max}A_e \tag{6-4}$$

$$V_{in\_L} = L\frac{\Delta I}{\Delta t} \tag{6-5}$$

and

$$B_{L\_max} = \frac{V_{in\_L} D_{L\_max} I_{peak}}{\Delta I n A_e f_s} \tag{6-6}$$

where V_{in_L} is the transformer input voltage; B_{L_max} is the max flux density; D_{L_max} is the duty cycle; f_s is the switching frequency; A_e is the effective area of the core; n is the turns.

Comparing with the transformer in the DAB mode, the boost inductor has higher peak current so as to the higher peak flux density, therefore the transformer in the boost inductor mode is considered as the worst case which will be designed first.

6.2.2 Boost Inductor Design and Comparison

Both the powder core material and nanocrystalline material are considered in the boost inductor design. An improved powder core inductor design approach considering the analytical soft-saturation model is proposed in [107], which will be discussed in detail in this dissertation. The size and the loss are compared. The powder core inductor is designed by the proposed inductor design approach in [107], and the nanocrystalline core inductor is designed by the classic linear inductor design approach.

For the boost inductor design, the first step is to calculate the required inductance value on the basis of the peak inductor current at the full load. When the main switch of the boost converter is on, the inductor voltage and current can be expressed as,

$$V_{in} = L\frac{\Delta I}{DT_s} \tag{6-7}$$

The relation between input and output voltage for the boost converter is,

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{6-8}$$

The peak-to-peak current should be below 40% of the average input current,

$$\Delta I \leq \frac{0.4P_{out}/\eta}{V_{in}} \tag{6-9}$$

Combining (6-13), (6-14) and (6-15), the required inductance value should be,

$$L \geq \frac{T_s V_{in}^2 (V_{out}-V_{in})}{V_{out}*0.4(P_{out}/\eta)} \tag{6-10}$$

where V_{in} is the input voltage; V_{out} is the output voltage; L is the boost inductor; ΔI is the peak-to-peak current; D is the duty cycle; T_s is the switching period; P_{out} is the output power; and η is the efficiency.

Based on the above calculation, an inductor needs to meet the specifications shown in Table 6-3.

Table 6-3. Inductor Specification

Inductance	480 μH
Average input DC current	12.5 A
Peak current	15 A
Current ripple	40%

To design the boost inductor shown in Table 6-3, several magnetic materials are considered, including *Nanocrystalline FT-3M*, *High Flux 26μ*, *High Flux 14μ* and *Iron Power-8*. *High Flux* powder materials from Magnetics [108] are made for the high DC biasing capability of the inductor, allowing to reduce the inductor size. Therefore, it fits for the application of high current and high power boost inductor. Iron powder is another material that can provide high flux density, but it

yields to higher loss compared with *High Flux* material. Permeability is a critical characteristic as well, which keeps the stability of the inductance in high DC bias.

The nanocrystalline core inductor is designed by the linear inductor design method, the *AP* method. The core material is *HITACHI FT-3M*, which has a high saturation flux density of 1.2 T. Although it is lower than the saturation flux density of *High Flux 26μ*, by adding the air gap, the turns of the nanocrystalline core inductor are fewer than those of the *High Flux* powder core inductor. According to (6-11), the inductance is determined by the relative permeability, the vacuum permeability, the turns, the effective core area and the effective magnetic length. Assuming that the nanocrystalline core and the powder core have the same effective core area and the same effective magnetic length, The relative permeability of *High Flux 26μ* core at high DC bias already drops to about 40% of the initial permeability, which needs more turns to maintain the similar inductance with the nanocrystalline core inductor.

The inductor with the air gap usually has the fringing flux and fringing effect. As mentioned before, fringing flux can cause many problems. Fringing flux can reduce the overall converter efficiency by generating eddy currents that cause localized heating in the windings. Besides, the fringing effect also increases the inductance which is designed by the regulator equation for inductor calculation. Therefore, when designing inductors, fringing flux must to be taken into consideration. A fringing effect factor is provided in [109], which has an impact on the basic inductor design equations. The inductance is dependent on the effective length of the magnetic path, which is the sum of the air gap length and the core magnetic path length. The final determination of the air gap size requires consideration of the fringing flux effect which is a function of the gap dimension, the shape of the pole faces, and the shape, size, and location of the winding. The fringing flux decreases the total reluctance of the magnetic path length and, therefore,

increases the inductance by a factor to a value greater than that calculated. The fringing flux factor and the inductor after the factor compensation are

$$F = (1 + \frac{l_g}{\sqrt{A_c}} ln \frac{2G}{l_g}) \tag{6-11}$$

$$L_{real} = F(\frac{\mu_r \mu_0 N^2 A_e}{L_e}) \tag{6-12}$$

where F is the fringing flux factor; l_g is the air gap; A_c is the core effective area; G is the length in the dimension shown in Figure 6-6;

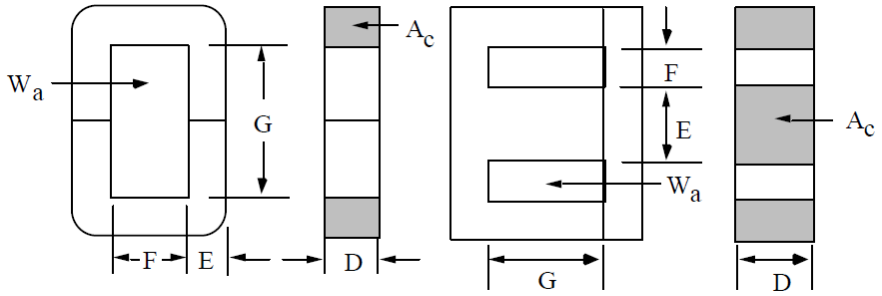


Figure 6-6. Dimension of C and E cores [109].

As an example, the inductor design results and comparison at 20 kHz based on the specification in Table 6-3 are shown in Figure 6-7. According to the design results, the nanocrystalline material inductors have the advantage of lower loss and size. With a selected core with the fixed core geometry, the fringing flux factor increases with the increase of the air gap. Figure 6-8 shows the fringing flux factor versus the air gap based on (6-11). Therefore, when the air gap increase, the real inductor based on (6-12) increase as well.

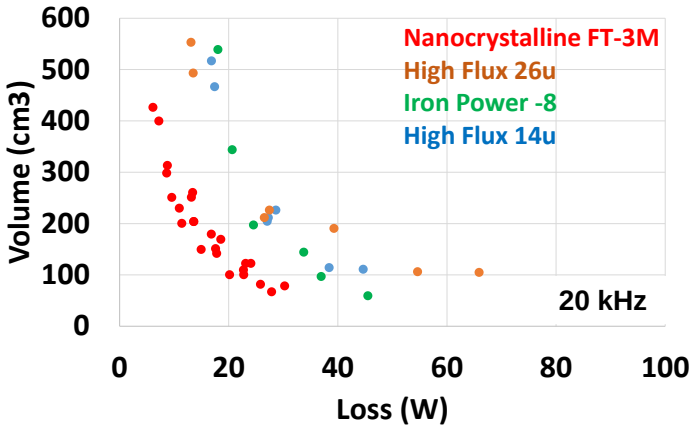


Figure 6-7. Weight vs. Loss between different materials.

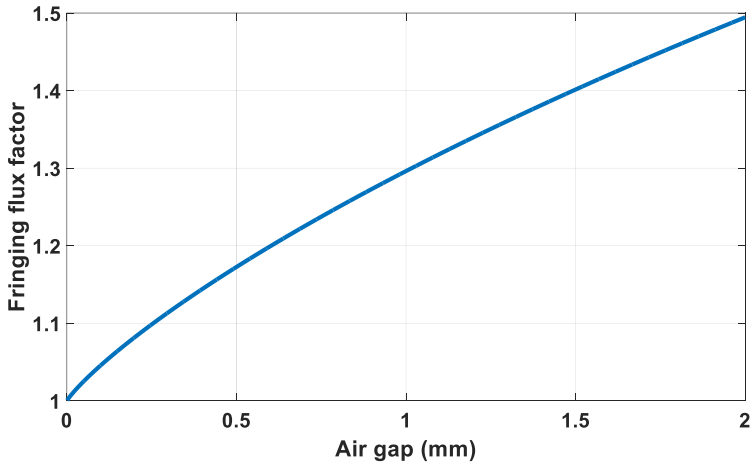


Figure 6-8. Fringing flux factor versus air gap.

6.3 Operation Region Targeted Design for the Integrated DC-DC Converter

6.3.1 Motivation of Operation Region Targeted Design

Traditional traction drive DC-DC converters in the EVs, usually the bidirectional boost converters, are designed as general, single-purpose power stages are sized for the ability to meet

high power demand with a minimum semiconductor cost. This approach suffers from a lack of consideration of the vehicle long-time operation profile. Figure 6-9 shows the general frequency of different operation regions based on to standard vehicle test cycles, US supplemental federal test procedure (EPA US06) and US federal test procedure 72 (UDDS). The x-axis and y-axis are the motor speed and torque respectively. The colors demonstrate the vehicle operation time. As can be seen, the vast majority of operation time is at low torque and at intermediate or high motor speeds. This correlates to frequent operation at low power and high voltage. It is preferable that the vehicle can operate in these frequent operation regions with high efficiency. However, the bidirectional drivetrain DC-DC converter is usually designed to meet high power demand with low cost. Therefore, they often suffer from low efficiency at light load and high step-up ratio, which encompasses to the vast majority of operating regions.

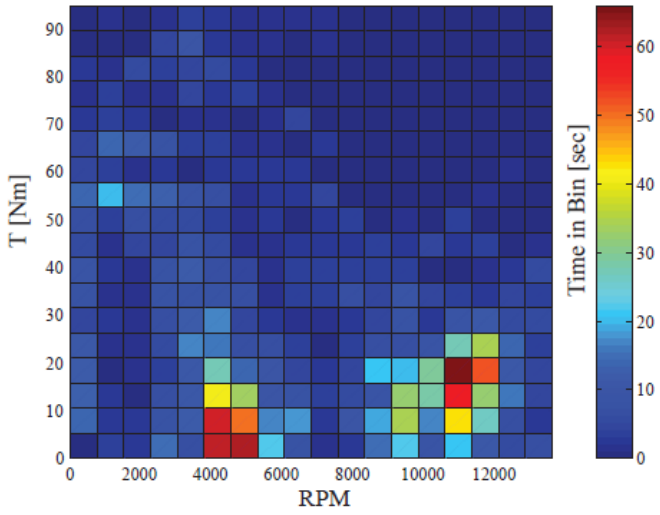


Figure 6-9. Frequency of different operation region based on two standard vehicle test cycles.

The proposed integrated DC-DC converter has multiple operation modes which enables the optimization of the power converter at the light load and high step-up voltage ratio condition, where the frequent operation regions stay in Figure 6-9. The integrated converter can operate as a boost converter in the traction mode, and at light load and high step-up voltage ratio condition where the boost converter has poor performance, the DAB converter can take over. Thus, the DAB converter is required to be designed optimally in the targeted long-time operation region so that it can improve the efficiency of the overall drivetrain system. The expected operation mode of the integrated DC-DC converter is shown in Figure 6-10. The converter in boost mode is designed for full load, and the DAB mode is used to achieve high efficiency when input and output voltage ratio is at or close to the transformer turns ratio. In this condition, the devices achieve ZVS allowing high efficiency operation.

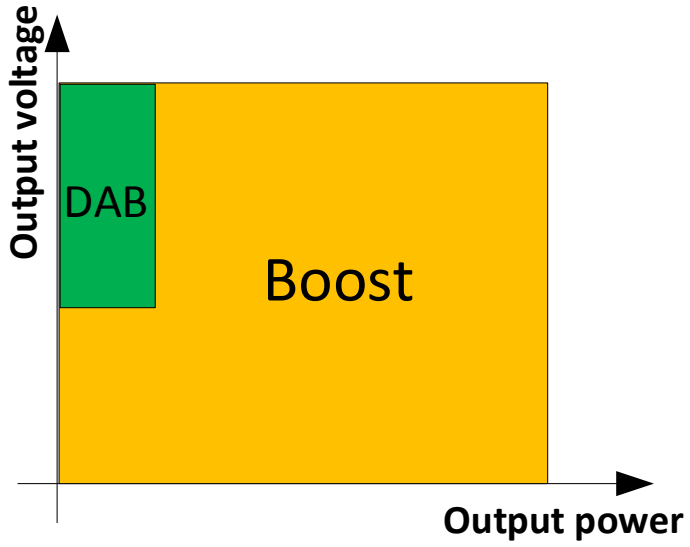


Figure 6-10. Expected operation mode of the integrated DC-DC converter.

6.3.2 Design Methodology for Integrated DC-DC Converter in Traction Mode

The design flow chart for the integrated DC-DC converter in traction drive mode is shown in Figure 6-11. The process combines boost converter design and DAB converter design. According to Figure 6-11, the dual function magnetic component worst operation mode estimation is the first step. As mentioned before, the converter in the boost mode uses the magnetizing inductance of the DAB isolation transformer as its power inductor. Therefore, the dual function magnetic component needs to satisfy both operation conditions. As is discussed in 6.2.1, the power rating of the boost converter is usually higher than the DAB converter in this typical application, and the high inductor current usually requires high peak flux density of the core. The saturation limit of the dual function magnetic component is defined by the boost inductor.

Then the process first designs the boost converter. Based on the specification shown in Table 6-1, the converter nominal operation points can be determined with input voltage, output voltage, output power, required inductor current ripple and the duty cycle. Several switching frequencies are selected in the design to have a basic understanding on the converter loss and size. The switching frequency is considered as the outer loop of the design. For each switching frequency, combining with the specifications, the boost inductance is calculated. After that, the inductor is designed by the linear inductor design approach or the proposed nonlinear inductor design approach for the powder core inductor in 6.2.2. The core material, core geometry, number of turns are determined. The core loss and winding loss are derived and compared in order to have the desired design. After the inductor design is finished, the power devices will be selected based on the conduction loss and winding loss. The thermal and cooling performance of the inductor and devices need to be evaluated as well.

After the inductor design and the power device selection are finished and iterated in several switching frequencies, the integrated DC-DC converter in boost mode will show the achievable size and efficiency. There will be many design results. The desired design is selected based on either power density requirement or the power efficiency requirement. After the design is selected, the contour for the voltage, power and efficiency can be plotted for the integrated DC-DC converter in the boost mode.

DAB converter design is the second part of the design process. The nominal operation points can be derived from the specifications shown in Table 6-2 including input voltage, output voltage and output power. Again, the switching frequency is the outer loop of the design. For each switching frequency, the transformer is first designed to determine the turns ratio and the number of turns for the primary side and secondary side. After that, the core loss and winding loss need to be evaluated. The transformer core is previously selected based on the boost inductor. If the core loss is high, the switching frequency can be reduced or the core size needs to be changed. Then, the new core in the boost inductor needs to be revaluated. The winding loss is impacted by the core winding fill factor and the wire gauge. If the winding loss is high, a higher the fill factor is required, which will reduce boost inductor winding fill factor. There will be some iteration on the design to achieve a preferred tradeoff in the performance in both boost mode and DAB mode.

Evaluation of the leakage inductance is another critical design step, since it is used in the soft-switching of both primary and secondary side devices for the DAB converter. There are three main constraints for the leakage inductance determination. First, under certain specifications and switching frequency, the leakage inductance determines the achievable peak output power of the DAB mode converter. Second, when the output power is fixed, the leakage inductance impacts the converter RMS current. When the leakage inductance is small, the converter RMS current is small.

Third, large leakage inductance is needed to help the device ZVS realization. Tradeoff iteration will be made when deciding the leakage inductance for the device soft-switching.

After considering the device loss and thermal performance, similar with the boost mode converter design, there will be many possible design results for different switching frequencies. Since the size of the secondary bridge and the magnetics is already determined by the converter in the boost mode, only the efficiency needs to be assessed for the integrated DC-DC converter in DAB mode. When the design is determined, the voltage power and efficiency contour can be plotted.

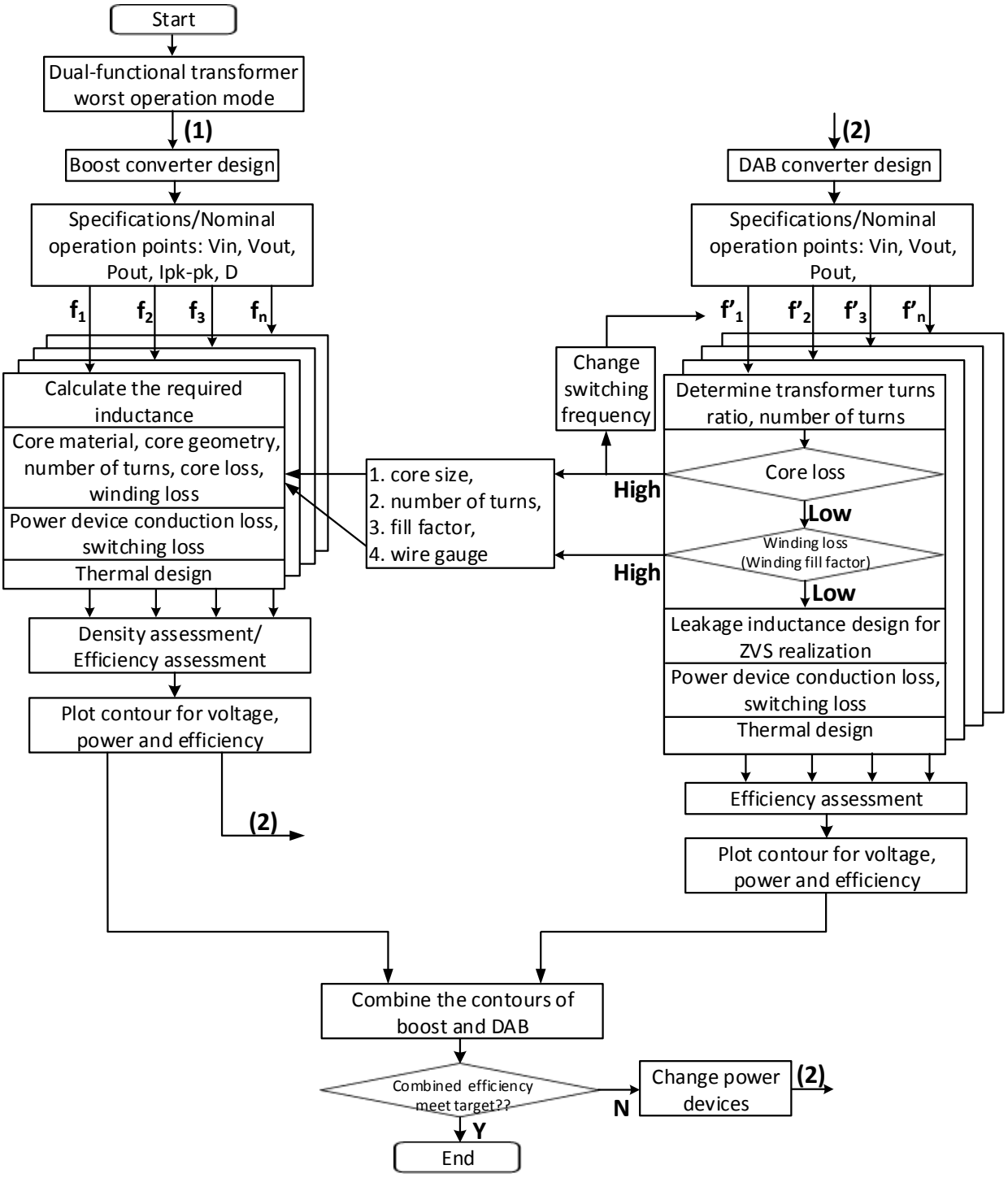


Figure 6-11. Design methodology for the integrated DC-DC converter in traction drive mode.

After both contours of boost mode and DAB mode are plotted, two contours are combined together. The efficiency is compared in the operation region for both boost converter mode and DAB converter mode. If the DAB converter mode fails to improve the efficiency at the region where the boost converter has the poor efficiency, the design of the DAB converter will be iterated.

For the boost inductor design, several magnetic materials are compared in different switching frequency, as is discussed in Section 6.2.2. The *nanocrystalline FT-3M* core is selected as the material with low loss and small size shown in Figure 6-7. After that, 40 mΩ, 80 mΩ, and 160 mΩ SiC MOSFET are considered in the design. As an example, the 80 mΩ device loss and the corresponding nanocrystalline inductor loss are combined in different switching frequencies shown in Figure 6-12. The 40 mΩ and 160 mΩ devices design cases show similar distribution with Figure 6-12. With lower switching frequency, the device switching loss and core loss density are reduced, however the inductance and core size are increased to keep the required ripple current. The total core loss is increased. Based on the design results, 50 kHz is selected as the switching frequency of the boost converter. The loss breakdown for the integrated DC-DC converter in boost mode is shown in Figure 6-13. The maximum loss occurs on the main SiC MOSFET. A 260 V-500 V output voltage range and 0-2.5 kW output power range are applied in the design to calculate the boost efficiency at different operation points. The efficiency contour is shown in Figure 6-14. The boost efficiency demonstrates above 98% from one third of the load to full load. When the output voltage is high and the power is more than half load, the efficiency is slightly reduced due to the increased device switching loss and conduction loss. Note that when the converter is in the light load during the wide output voltage range, the efficiency drops below 96%. Especially when the output voltage is near 500 V, the efficiency is about 94%. It is obvious that the boost converter in light load and high voltage step-up ratio suffers from the poor efficiency.

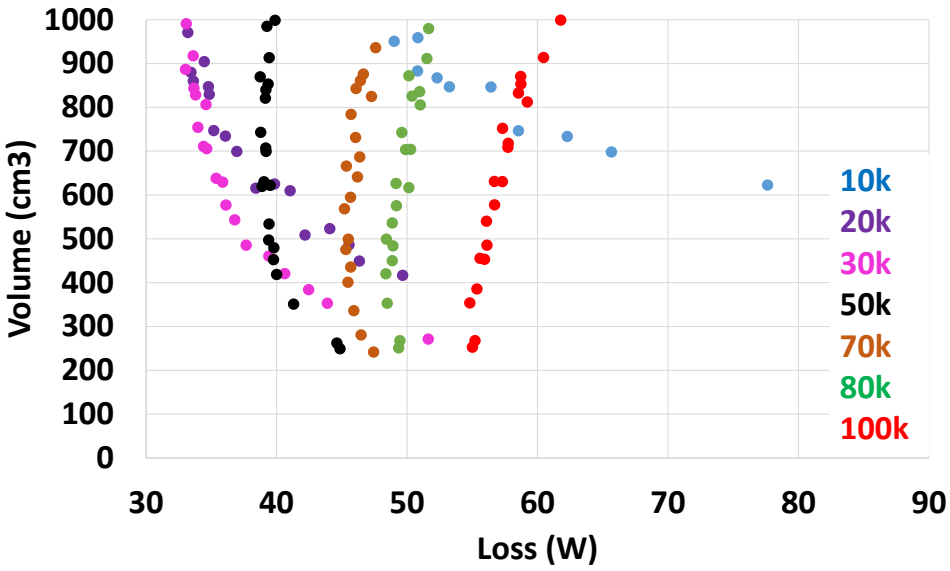


Figure 6-12. Boost inductor and 80 mΩ SiC MOSFET combined loss and solid volume.

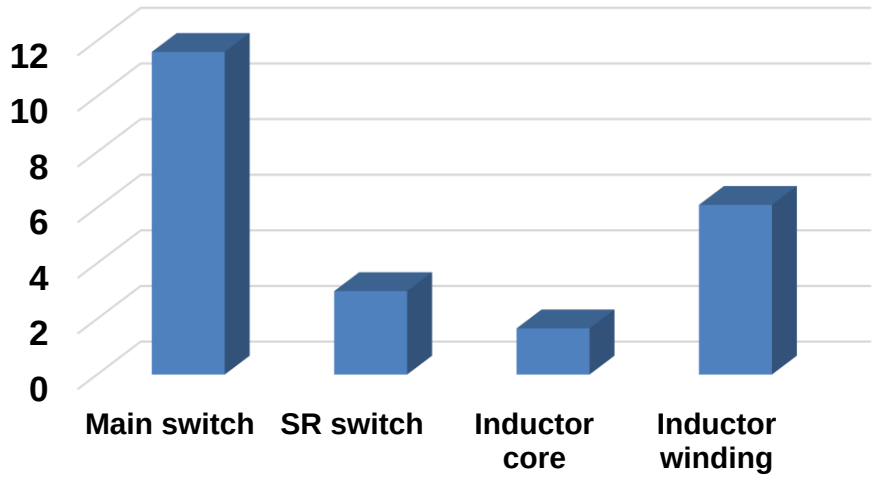


Figure 6-13. Loss breakdown for the integrated DC-DC converter in boost mode at 200 V-450 V/2.5 kW.

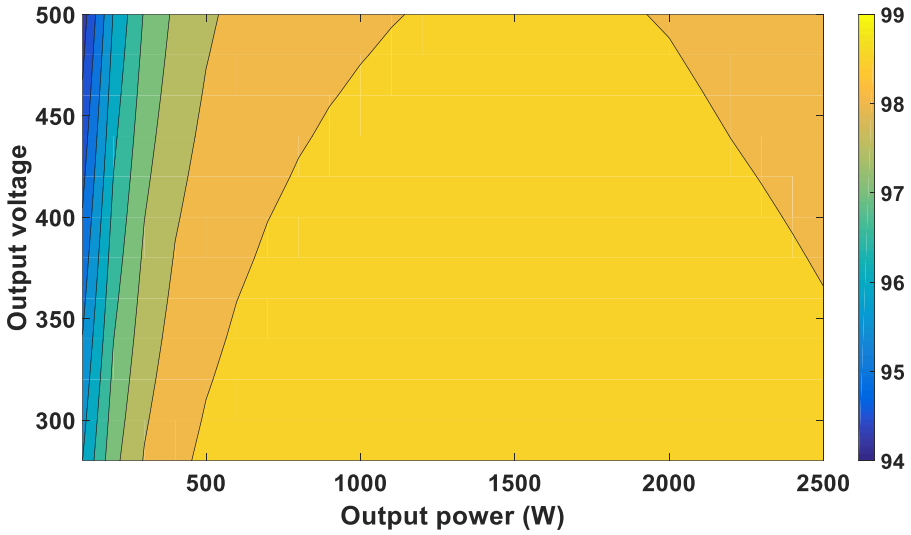


Figure 6-14. Efficiency contour for the integrated DC-DC converter in boost mode.

The scaled-down DAB converter is designed based on the specifications shown in Table 6-2. Different switching frequencies are also selected in the design. Since the secondary side turns for nanocrystalline transformer is determined in the boost converter design, the primary side number of turns is calculated based on the turns ratio to match the nominal input and output voltage of the converter in DAB mode, which is 20:45. In this case, the optimal operation point is 200 V input and 450 V. The core size is determined in the boost design and evaluated in the DAB operation condition with three different switching frequencies. The maximum core loss is below 4 W, which is considered as an acceptable value. Since current flow through the secondary side winding, used for the boost mode, is much higher in the boost design, the fill factor for the boost winding is 0.8, while for the primary side the fill factor is 0.2. The contour of the output voltage, output power and efficiency for the converter in DAB mode is shown in Figure 6-15. In the wide load range from 60 W to 660 W, the DAB can achieve efficiency above 95% efficiency. The contour of the converter in the boost mode in the same range is shown in Figure 6-16. Comparing Figure 6-15

and Figure 6-16, the converter in the DAB mode has higher efficiency in the wide operation range than the boost converter. The combined efficiency contour for the integrated DC-DC converter is plotted in Figure 6-17. By applying the converter in DAB mode, the efficiency of the boost converter in the operation regions of light load and high voltage step-up ratio is improved.

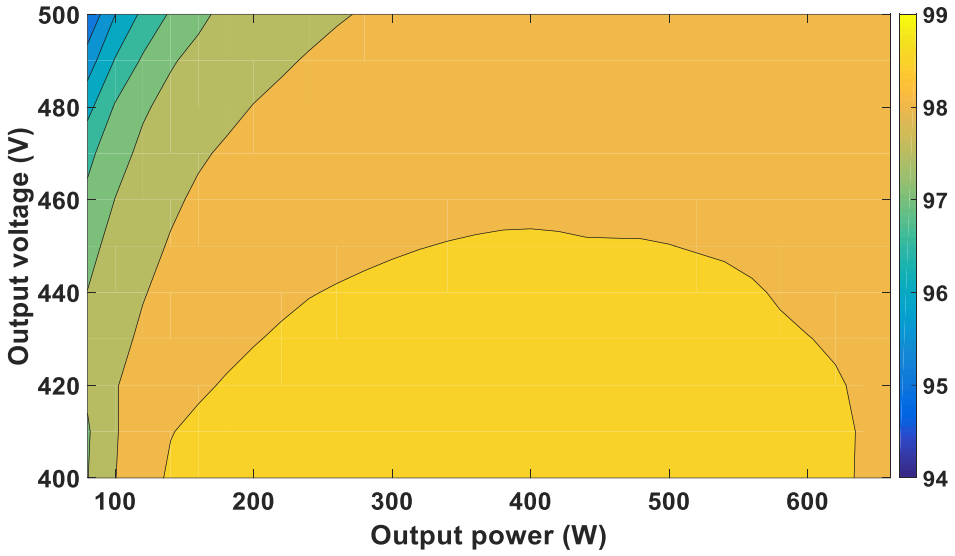


Figure 6-15. Efficiency contour for the integrated DC-DC converter in DAB mode.

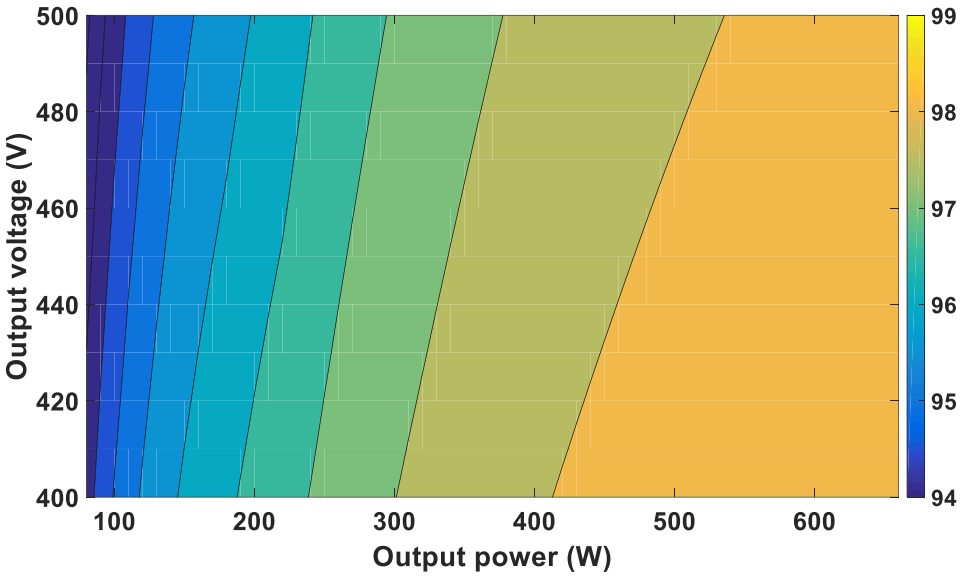


Figure 6-16. Efficiency contour for the integrated DC-DC converter in boost mode in the targeted operation region.

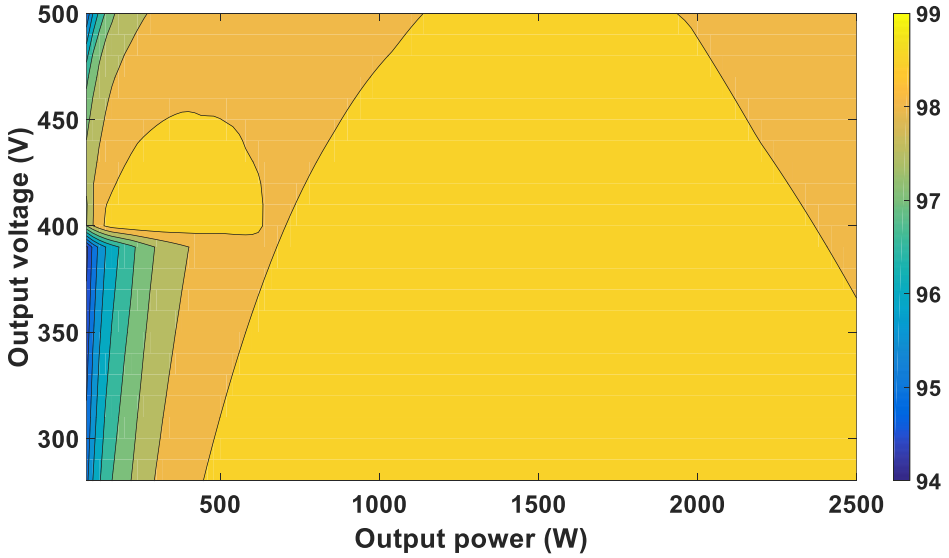


Figure 6-17. Combined efficiency contour for the integrated DC-DC converter.

6.4 Experimental Verification

In order to verify the design methodology for the proposed integrated DC-DC converter in the traction drive mode, an integrated converter prototype with rated 2.5 kW Boost and 660 W DAB was built. CREE C2M0080120D SiC MOSFETs are used as the devices for both primary side and the secondary side. The integrated transformer is built using Nanocrystalline FT-3M core with size of F3CC006.3. The primary side of the transformer is built with 20 turns using 16.5 equivalent AWG Litz wire and the secondary side is built with 45 turns using 14 equivalent AWG Litz wire. The leakage inductance is 70 μH using the transformer leakage inductance. The controller is realized by Xilinx FPGA. The DAB converter hardware is shown in Figure 6-18. There are four identical phase leg modules and two series transformers that constitute the DAB converter. The interleaved boost converter is realized by the left two phase leg module.

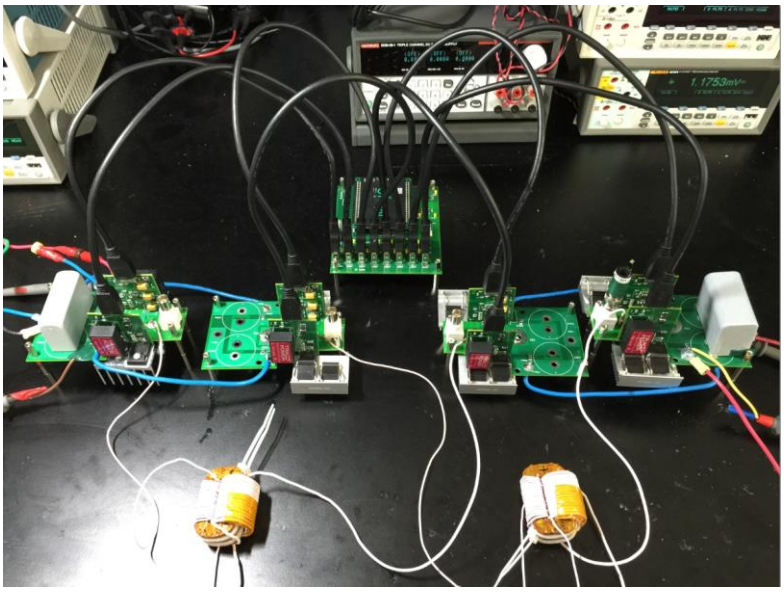


Figure 6-18. DAB converter hardware with boost converter using the left phase leg module.

The test waveforms for the boost and DAB converter at the full load are shown in Figure 6-19 and Figure 6-20. In Figure 6-19, the gate source voltage and the drain source voltage are measured on the main switch. I_L is the inductor current. In Figure 6-20, the device gate source voltage and drain voltage are measured as well. V_{pri} is the transformer primary side voltage and I_{Lk} is the current flowing the leakage inductance, which is also the transformer primary side current.

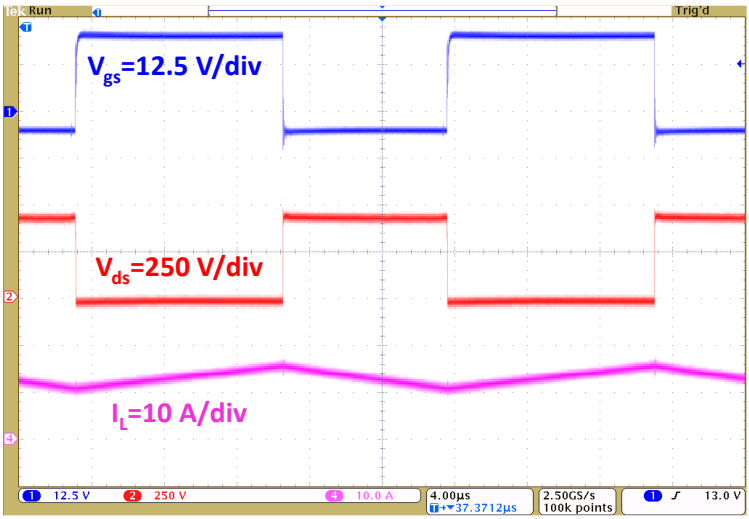


Figure 6-19. Boost converter waveforms at 200 V-450 V/2.5 kW.

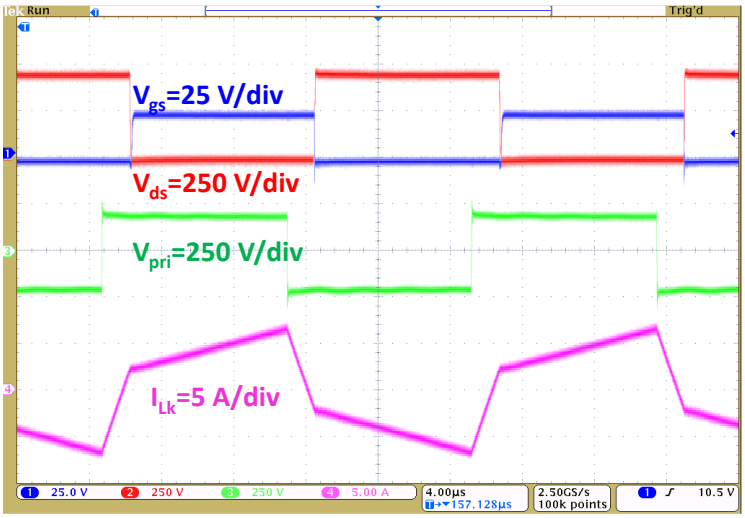
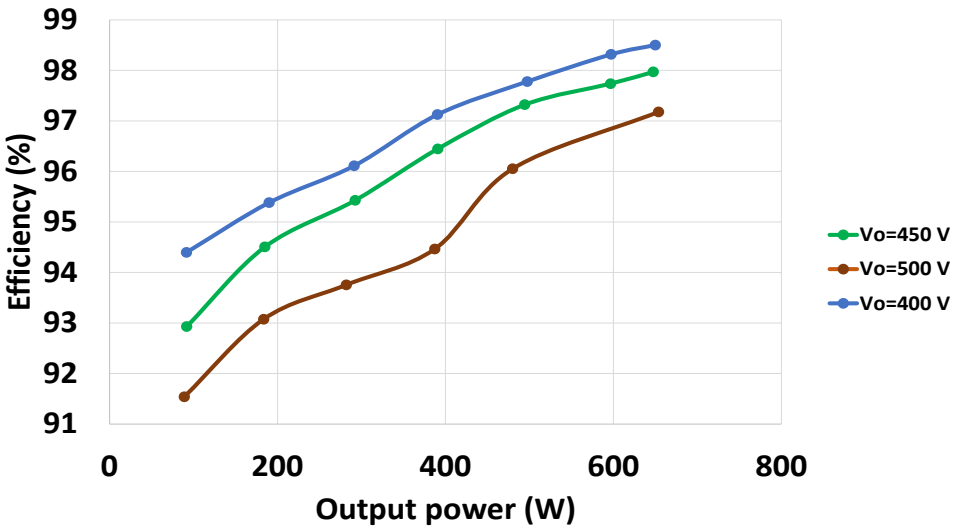
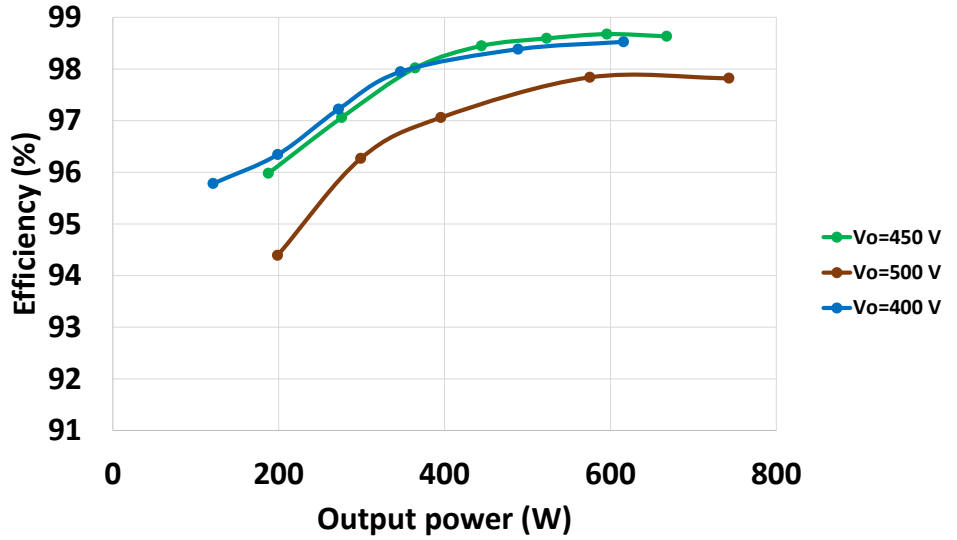


Figure 6-20. DAB converter waveforms at 200 V-450 V/660 W.

The efficiency is measured in both boost and DAB converter. For the boost converter, the efficiency is measured from 100 W to 660 W at 400 V, 450 V and 500 V output voltage. For the DAB converter, the efficiency is measured from 100 W to 660 W at 400 V, 450 V and 500 V output voltage. The efficiency curves are shown in Figure 6-21. The DAB converter demonstrates the higher efficiency than the boost converter in the light load region. It is verified that the integrated DC-DC converter in DAB mode can be optimally designed for the targeted operation region to take with higher efficiency.



(a) Boost efficiency curves



(b) DAB efficiency curves

Figure 6-21. Efficiency curves for boost and DAB converter.

6.5 Summary

In this chapter, the topology of the integrated DC-DC converter has been discussed. The two different operation modes and their equivalent circuits are presented in both the on-board charger

mode and traction drive mode. The main challenge of the integrated converter is the combination of the boost inductor in traction drive and the transformer in on-board charger. The integrated magnetic component is considered as a dual function magnetic component. It has been analyzed that the saturation limit of the dual function magnetic component is when it operates as the high current boost inductor. The design approach of the boost inductor is discussed after that. The nanocrystalline core inductor has lower loss, weight and size. A design methodology for the integrated DC-DC converter is proposed in this chapter for the traction drive mode. The integrated DC-DC converter in DAB mode is optimally designed for the targeted operation region to take over the boost converter with higher efficiency. An integrated converter prototype with rated 2.5 kW Boost and 660 W DAB was built and tested. The results show the capability of the DAB converter to improve the light load efficiency.

7 Conclusions and Future Works

This chapter concludes the research work discussed in Chapter 3~6, and presents the future work.

7.1 Conclusions

This dissertation studies the energy-efficient and power dense DC-DC converters in data center and electric vehicle applications. The main research contributions are summarized as follows.

First, the relationship between the device parameters and LLC resonant converter device loss has been established. An analytical loss model has been derived. Based on the loss model, the GaN device impact on the LLC resonant converter loss is analyzed. Due to the small output capacitance and small input charge, the GaN-based converter design can achieve low dead time and low peak magnetizing current, therefore the converter RMS current is reduced. Compared with the Si-based converter with the same specifications, the GaN-based converter has about 50% device loss reduction.

Second, a new perspective of the extra winding loss due to the asymmetrical primary side and secondary side current in the LLC transformer has been proposed. Usually interleaving winding structure helps to reduce the eddy current effect winding loss by cancelling the *H* field between the windings where the transformer primary side current and secondary side current exist in the same amplitude and opposite direction. However, in the LLC resonant converter, due to the existence of the magnetizing current, there is a phase different between the primary side and secondary side windings. Simulation results proves that there is about 1.3 W extra winding loss in a 300 W LLC resonant converter. The extra winding loss reduces along with the reduction of the

phase different as well as the peak magnetizing current. By applying the GaN device, about 18% transformer loss has been achieved.

Third, the soft-switching behavior of the cascode GaN HEMT was investigated in detail. Several interesting phenomena of cascode devices have been discussed. The channel current drops to zero quickly during the turn-off transient due to the internal feedback of the cascode structure, which leads to extremely small turn-off loss. On the other hand, there is switching energy loss on the internal normally-on GaN HEMT during the device ZVS turn-on transient, although the external waveforms of the cascode GaN HEMT exhibit ZVS. The thermal test verifies that there are about 400 mW extra loss in the soft-switching at 1 MHz.

Fourth, an improved LLC resonant design approach with an optimal dead time selection that considers both the impact of device loss and winding loss is proposed. Adding to the classical design approach that only consider the device loss in the dead time selection, the improved approach also considers the extra winding loss induced by asymmetrical primary side and secondary side current.

Fifth, a new design approach of extracting the magnetizing inductance out of the transformer has been proposed. Due to the integration of the inductance in the resonant tank inside the transformer, the LLC transformer suffers high fringe effect loss and high extra winding loss. By applying the external inductor and removing the air gap in the transformer, the asymmetrical current induced transformer winding loss and the fringe effect induced transformer winding loss can be eliminated. Since the external inductor only processes a small amount of the circulating power rather than the entire converter power such as transformer, the additional size and loss is low. The design and loss analysis of the external inductor is presented. The GaN based LLC

resonant converter with external inductor is built. The test results shows 0.5% improvement on the converter efficiency.

Sixth, in the EV application, a new integrated converter with isolated DC-DC converter and drivetrain DC-DC converter is studied. The most challenge part of the designing is the dual function magnetic component that integrates the transformer of the charger and the inductor of the drivetrain converter. The dual function magnetic component has been designed with different magnetic materials. An inductor design result is presented. The nanocrystalline core inductor has lower loss, weight and size.

Seventh, a new operation region targeted design for the integrated DC-DC converter is proposed. Traditional drivetrain DC-DC converter (boost converter) is usually designed for full load suffering from poor efficiency at light load and high voltage step-up ratios. The integrated DC-DC converter can operate in the DAB mode to cover the operation region of the boost mode which as poor efficiency. A design methodology is proposed for the integrated converter in the DAB mode where the converter is optimally designed with high efficiency for the targeted operation region. A scaled-down integrated DC-DC converter hardware prototype is built to verify the design methodology and the loss model. The test results show higher efficiency of the DAB converter than the boost converter at its light load and high voltage step-up ratios condition.

7.2 Future works

The suggestions on the future work focuses on the following parts:

(1) Analytical winding loss model of the asymmetrical primary and secondary side current

The extra transformer winding loss for the high frequency LLC resonant converter is discussed in this dissertation. Since the magnetizing current is part of the transformer primary side

winding current, a phase different exists in the primary and secondary side current. The extra winding loss is because of the non-cancelable magnetic field when the primary side current and the secondary side current are not in phase and not in the opposite direction. It leads to the complicated magnetic field distribution and current density distribution. Therefore, the discussion of the extra winding loss is based on qualitative analysis and simulation results.

An analytical loss model is necessary for more accurate transformer winding loss analysis for the LLC resonant converter. It is preferable to derive the relations between the winding loss and the phase difference. In that way, the derived relation can be applied in the improved LLC resonant converter design methodology discussed in 5.1. The optimal dead time can be obtained by the analytical loss model of both device loss and transformer winding loss.

(2) Mega-hertz LLC resonant converter

High power density and advanced package technique are necessary for the Mega-hertz LLC resonant converter. Increasing switching frequency is necessary to reduce the converter size and improve the power density. High switching frequency also requires advanced package technique to reduce the layout parasitics. One of the critical improvements with the GaN power transistor is the very low junction capacitance and very fast switching speed. Therefore, GaN power transistors can operate at very high frequency to greatly improve the power density without much penalty of power loss. Compared with the high frequency (e.g. 1.7 MHz) Si power MOSFET based converter, the GaN-based converter is expected to operate at even higher frequency (e.g. 3 MHz) with similar device loss. Future work can be done on the very high frequency DC-DC converter to take advantage of the superior switching performance of the GaN power transistor. Based on this, the gate driver design, the magnetics design and the converter layout will be changed as well. A resonant gate driver will be necessary to reduce the gate driver loss as well as the heat dissipation.

NiZn ferrite material is required because the MnZn ferrite cannot support such high frequency. The transformer core needs to be a customized design. A new winding structure is required because the AC impedance of the traditional winding structure will be changed. The layout can be even more critical to reduce the high frequency AC resistance.

(3) Non-linear inductor in kilo-hertz LLC resonant converter

An external inductor can be applied to reduce the transformer winding loss instead of having the magnetizing inductance to support ZVS of the primary side devices. One step further on this solution, it is interesting to investigate if the current for the device ZVS realization can be reshaped. Normally, since the L_m is a linear inductor, the inductance value stay the same during the LLC resonant converter operation. The current flows through the L_m is a triangle waveform, which is independent from the load condition. That current circulates in the primary side device and does not deliver the power to the output. Therefore, the cost of device ZVS realization is the circulating current that induces the device conduction loss. Even in the no load condition, the circulating current induced conduction loss also exists.

The circulating current can damped by increasing the inductance L_m. When L_m is higher, the peak current is low and the RMS current is low. However, the low peak current requires large dead time to discharge the energy in the device output capacitance. Thus, it is preferable if the current can be reshaped: when the device is on to deliver the power, the peak current is small, and when the device is ZVS transition in the dead time, the peak current is high. A nonlinear inductor can realize that function. The nonlinear inductor allows the flux density operating from the linear region to the non-linear region, and the inductance changes accordingly. However, the drawback of the nonlinear inductor is the high core loss because the magnetic core operates in the entire *B*-*H* range. Especially in the mega-hertz converter, it is not reasonable unless an ultra-

low loss for the high frequency magnetic material in the future. For low frequency converter, such as several tens of kilo-hertz LLC resonant converter, the benefits of the nonlinear inductor to reduce the converter loss will emerge. An optimal design of the nonlinear inductor is also necessary to maximize the loss reduction benefits.

(4) Intelligent operation mode control and the systematic efficiency optimization for the integrated DC-DC converter

As is discussed in Chapter 6, since the integrated DC-DC converter consists both boost and DAB converter, there are several operation modes for the integrated DC-DC converter. It can operate as two boost converters interleave, one single boost converter, DAB converter. The boost converter is competent for the high power and wide output voltage operation region, which refers to the vehicle in the acceleration mode. The DAB converter can achieve high efficiency when the input output voltage ratio is close to the transformer turns ratio. Therefore, it can be targeted designed for the poor efficiency region for the boost converter. The different operation modes for the integrated DC-DC converter corresponds each operation region that can achieve high efficiency.

It is necessary that the different operation modes need to be intelligently and seamlessly changed according to the vehicle operation conditions. A control algorithms need to be developed to optimally choose the best operation mode for the integrated DC-DC converter. Further, the design of the integrated DC-DC converter also needs to consider the overall traction drive efficiency and operation condition including the inverter and motor. It is possible that although the integrated DC-DC converter optimally operate at certain region, the motor drive system efficiency is low. Therefore, a systematic efficiency optimization of the entire traction drive system is necessary.

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