To the Graduate Council:

I am submitting herewith a thesis written by Abdullah A. Bagersh entitled "Analysis and Design of a High Voltage Amplifier to Drive Capacitive Loads." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

T. V. Blalock, Major Professor

We have read this thesis
and recommend its acceptance:

Accepted for the Council:

Vice Provost
and Dean of The Graduate
School

STATEMENT OF PERMISSION TO USE

In presenting this thesis in partial fulfillment of the requirements for a Master's degree at The University of Tennessee, Knoxville, I agree that the Library shall make it available to borrowers under rules of the Library. Brief quotations from this thesis are allowable without special permission, provided that accurate acknowledgment of the source is made.

Permission for extensive quotation from or reproduction of this thesis may be granted by my major professor, or in his absence, by the Head of Interlibrary Services when, in the opinion of either, the proposed use of the material is for scholarly purposes. Any copying or use of the material in this thesis for financial gain shall not be allowed without my written permission.

Signature Abdullah Bafaqeh

Date 8/13/85

ANALYSIS AND DESIGN OF A HIGH VOLTAGE AMPLIFIER TO DRIVE CAPACITIVE LOADS

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Abdullah A. Bagersh

August 1985

I dedicate this thesis to my father Abubaker Bagersh and my mother Fozia Baobied for all their love and support and also to my grandfather Salem Bagersh who has given us so much of himself over the years.

ACKNOWLEDGEMENTS

I would first like to thank Dr. T. V. Blalock for patiently guiding me throughout my academic career, for being a source of support and advice everytime I approached him with a problem and for giving me the opportunity to work with him. It truly has been a pleasure.

I extend many thanks to Drs. R. E. Bodenheimer and J. M. Rochelle for being on my thesis committee and for teaching me so much during my association with them. I would also like to thank Dr. T. M. Moriarty for the challenging work and all the help, it has been a great learning experience.

Thanks are due to Denise Smiddy for being so patient and doing a superb job of typing the thesis. Many thanks to Bobby Bodenheimer for the unrelentless proof reading of the thesis and help with the computer. Without the technical services staff, Jim Barnes, Len Adkins and Jack Watson, a lot of the work would not be possible - many thanks for all the help. Last but not least, I thank my sister, Sana, for all the love and care she has given me during my work.

ABSTRACT

An amplifier capable of driving a capacitive transducer (~500 pF) up to 300 V and 150 kHz was designed and implemented. Design equations describing the frequency response, the transient response, input impedance, output impedance and power dissipation have been presented. The results from these design equations are compared with the experimental results and SPICE computer simulation results.

The driver amplifier shown in this thesis has a worst case rise time of ~0.9 μs. As signal level decreases the rise time also decreases. The bandwidth of the driver amplifier is ~700 kHz at low signal levels and decreases to about 450 kHz at high signal levels. The slew rate is calculated to be ~1180 V/μs and at worst case conditions the pulse response showed no slewing indicating a slew rate >600 V/μs. Good correlation was observed between the hand analysis, SPICE analysis and experimental results.

TABLE OF CONTENTS

CHAPTER PAGE

LIST OF FIGURES

FIGURE PAGE

CHAPTER 1

INTRODUCTION

The use of high voltage driver amplifiers is often required in ultrasonic instrumentation. In many cases, a capacitive load in the form of a transmitting transducer will have to be driven. A driver used for such applications would have to drive voltages up to 300 V and frequencies as high as 150 kHz into a capacitance that may be greater than 500 pF. These requirements may differ depending on the characteristics and operating conditions of the transducer. A driver amplifier to drive such transducers to these high voltages and frequencies will be the subject of this thesis.

In this application, the transducer is air-loaded and since ultrasound in air is attenuated strongly as frequency increases a practical limit was set at 150 kHz for this application [1, 2, 3]. The 300 V limit was set by the voltage handling capability of the transducer, in this case a Polaroid electrostatic ultrasonic transducer [4, 5]. The capacitance of this microphone is in the range of 400-500 pF.

Having an amplifier drive the microphone makes the system versatile because different signal generators with different capabilities such as amplitude, frequency, and gating control can be used to drive the amplifier at low signal levels. The amplifier would have a fixed gain and a fixed frequency response and be used as a block in the chain of instrumentation. This driver amplifier has to be efficient in power usage because the size of

the power supply increases as the power consumption increases. This is relevant in this case since the ultimate goal is to have a portable unit.

The simulation program, SPICE [6] (Simulation Program with IC Emphasis), will be used to confirm the hand analysis results, supplement the experimental results and offer an in-depth study of the transient response.

The organization of the thesis is as follows:

Chapter 2 presents the design background, design considerations and a specific set of design goals. The frequency response and stability analysis of the general circuit model is also given.

Chapter 3 covers the details of the amplifier design starting with the choice of configuration and leading to the complete theoretical and numerical analysis of the frequency response, transient response and power dissipation of the final circuit design.

Chapter 4 presents the SPICE results, the experimental results and whenever possible a comparison of these with the hand analysis results developed in Chap. 3.

Chapter 5 puts forward some conclusions and offers suggestions for further work.

CHAPTER 2

DESIGN BACKGROUND

The basic guidelines for the design of the driver amplifier were briefly introduced in Chap. 1. Before proceeding further, a more specific set of goals must be outlined. These goals will dictate the design approach. The following are design considerations for the amplifier:

1. A variable load in the range of 0-1000 pF will have to be accommodated. The amplifier should be stable against oscillations for all loads with minimum adjustment of components.
2. The output voltage should have a dynamic range of 150 V peak for frequencies up to 150 kHz, and since the load current increases as the frequency increases, power devices will be required in the output stages.
3. Since sinusoidal signals of up to 150 kHz and fast pulses will be driven into the microphone, faithful reproduction of these signals requires a risetime that corresponds to approximately twice the highest frequency (150 kHz), and a slew rate that does not compromise the risetime.
4. A high power efficiency must be achieved since portability (battery operation) is an objective.

A non-inverting feedback amplifier configuration can be used, leading to a stabilized voltage gain that is nearly independent of parameter

variations of amplifier components. For efficient power consumption the amplifier will be divided into a high and a low voltage section. The higher power dissipation will now occur only at the output stages since the high voltage sources supply the output stage only. This allows the use of slower, more expensive, less readily available power transistors at the output stages only. Four different power supplies will therefore be necessary, however with the addition of dc-dc converters, two voltage sources only will be needed. Dividing the amplifier in this manner will require voltage gain in the output stage.

2.1 Design Goals

The following are the basic specifications to be met in the design of the driver amplifier. The choice of these values will be explained during the numerical design section of Chap. 3.

1.	Voltage gain, A_{CL}	150 V/V
2.	Frequency response	> 300 kHz
3.	Slew rate	> 600 V/μs
4.	Output drive into 500 pF	~ 300 V pk-pk.

2.2 Frequency Response and Stability Analysis

The general circuit model of a feedback amplifier can be seen in Fig. 2.1. It can be used to determine the frequency response of the amplifier if the forward path transfer function is known. The load impedance has to be included in this analysis since an important critical frequency occurs at the output node. The expression for the forward path voltage gain, $A_{o\ell}(f)$, will

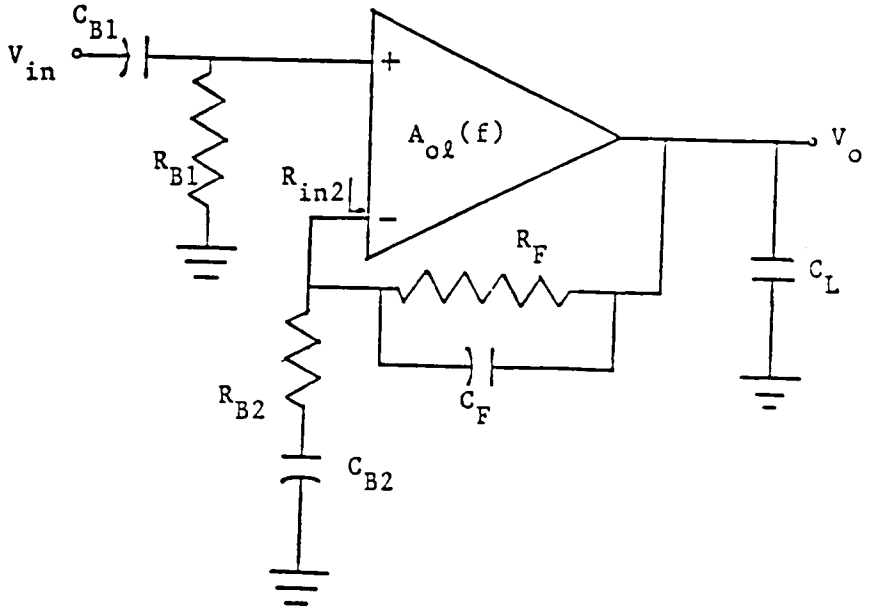

Figure 2.1. General circuit model of a feedback amplifier used to analyze the overall frequency response and oscillation stability.

include the dependence on the load and the effect of impedances in the feedback path.

The high frequency response of the amplifier will not depend on the capacitors C_{B1} and C_{B2} because these capacitors are essentially short-circuits at high frequencies. The forward-path frequency domain transfer function is

$$A_{o\ell}(f) = A_o\left(\frac{1}{1 + jf/f_1}\right)\left(\frac{1}{1 + jf/f_2}\right)\left(\frac{1}{1 + jf/f_3}\right)\ldots, \qquad (2.2\text{-}1)$$

where f_1, f_2, etc., are the critical frequencies in the forward path of the amplifier and A_o is the midband open-loop voltage gain or forward-path gain. The closed loop voltage gain, $A_{CL}(f)$, from feedback amplifier analysis, is

$$A_{CL}(f) = A_{CL}^{ideal}(f)\ \frac{-T(f)}{1 - T(f)}\ , \qquad (2.2\text{-}2)$$

where T(f) is the loop transmission of the amplifier. The value of T(f) is frequency dependent and, for stability against oscillations, the phase of T(f) must not shift by more than 360° while the magnitude is still greater than unity. The phase margin which is the amount of phase which remains to be shifted before 360° degrees is reached when the magnitude of the loop gain is unity, describes the relative stability of the system. The ideal closed-loop gain, A^{ideal}_{CL}, for a voltage-sample voltage-sum amplifier is equivalent to the inverse of the gain from the output node to the summing node when the

loop transmission, T(f), is taken in the limit as $T(f) \to \infty$. Therefore, from Fig. 2.1

$$A_{CL}^{ideal}(f) = \frac{Z_f + R_{B2}}{R_{B2}} , \tag{2.2-3}$$

where

$$Z_f = \frac{R_F}{1 + j2\pi R_F C_F f} . \tag{2.2-4}$$

The loop transmission, T(f), is obtained by grounding the input, breaking the feedback loop at a point where the loading effect is negligible, injecting a test signal, and then observing the return signal. From Fig. 2.1, the loop gain is, therefore,

$$T(f) = A_{o\ell}(f) \cdot \frac{R_{B2} \| R_{in2}}{Z_f + R_{B2} \| R_{in2}} . \tag{2.2-5}$$

The ideal closed loop gain, after substituting Eq. (2.2-4) into Eq. (2.2-3) gives

$$A_{CL}^{ideal}(f) = \frac{R_F + R_{B2}}{R_{B2}} \frac{\left(1 + jf/f_z\right)}{\left(1 + jf/f_p\right)} , \tag{2.2-6}$$

where

$$f_z = \frac{1}{2\pi\left(R_{B2} \| R_F\right) C_F} \quad , \tag{2.2-7}$$

and

$$f_p = \frac{1}{2\pi R_F C_F} \quad . \tag{2.2-8}$$

In the expression for T(f), f_z and f_p will be in the denominator and numerator, respectively. The purpose of having the capacitor C_F is to place f_p at a frequency that allows for the cancellation of a pole in the expression for the loop transmission, thereby improving or optimizing the frequency response of the driver ampliifer. The presence of multiple poles in the loop transmission, T(f), causes a more rapid shift in phase towards 360° and even with the presence of a dominant pole in the loop transmission, the higher poles could degrade the phase margin. The use of the capacitor C_F, however, is optional since the response of the driver amplifier might already be satisfactory.

At low frequencies the capacitor C_F and the device capacitances will essentially be open-circuits, but the capacitors C_{B1} and C_{B2} will become important. The capacitor, C_{B2}, is important because in addition to controlling the low frequency response it also causes the inverse of A^{ideal}_{CL} to approach unity as the frequency approaches zero. This means that at

very low frequencies, the loop transmission, T(f), will increase towards the value of the forward-path gain, A_0, causing a consequent improvement in quiescent point stability.

The low frequency response is obtained by considering the capacitors C_{B1} and C_{B2}. The low frequency transfer function is

$$A_{CL}(f) = A_{CL}^{mid}\left(\frac{1 + jf/f_{LZ}}{1 + jf/f_{LP1}}\right)\left(\frac{jf/f_{LP2}}{1 + jf/f_{LP2}}\right), \tag{2.2-9}$$

where a low critical frequency associated with a zero occurs at

$$f_{LZ} = \frac{1}{2\pi\left(R_F + R_{B2}\right)C_{B2}}, \tag{2.2-10}$$

and a low critical frequency associated with a pole occurs at

$$f_{LP1} = \frac{1}{2\pi R_{B2} C_{B2}}. \tag{2.2-11}$$

The critical frequency due to the capacitor C_{B1} is

$$f_{LP2} = \frac{1}{2\pi R_{B1} C_{B1}}. \tag{2.2-12}$$

CHAPTER 3

AMPLIFIER DESIGN

In Chaps. 1 and 2, an introduction to the design goals and a design background were presented. In this chapter, these general requirements will be used, along with the feedback and stability analysis results, to achieve a more detailed design.

3.1 Design Development

The most important section of the driver amplifier is the output stage. Unlike the usual amplifier designs, high voltages will have to be driven thus leading to severe non-linear effects in the output transistors because of capacitance and quiescent current change with drive and it will also lead to important power dissipation considerations. The presence of feedback will make the operation all the more interesting due to its attempts to correct the distortion. The load being capacitive and the large base-collector capacitances of the output power devices will require large charging currents, especially at high frequencies, and the driver amplifier will have to respond and supply these currents. The amplifier will be divided into a high voltage and a low voltage section as explained in Chap. 2.

3.1.1 High Voltage Section

From the high output voltage swing requirements placed on this driver amplifier, a complementary output stage is the logical output configuration to be used. In Fig. 3.1, a complementary emitter-follower

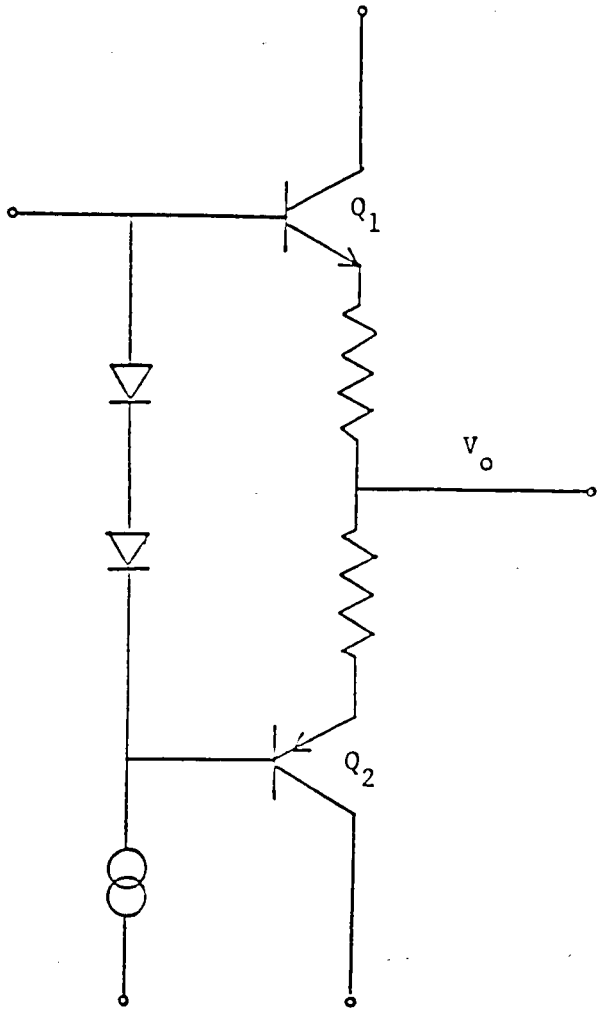

Figure 3.1. Complementary emitter-follower configuration.

configuration is shown. This configuration is used in many operational amplifier and power amplifier designs, and is capable of supplying large amounts of current to resistive loads. Emitter-follower configurations, however, have difficulty driving capacitive loads because of their tendency to develop a negative input resistance thus leading to oscillation. In addition, using this configuration would mean that high voltages would be present at the bases of the output transistors, requiring an additional high voltage gain stage between the level-shifting stage and output stage.

Alternatives to this configuration are available and one is the common-emitter complementary output stage shown in Fig. 3.2. Transistors Q_1 and Q_2 are level-shifting stages and the voltage between the bases of these two transistors sets the quiescent current at the output stage. Transistors Q_3 and Q_4 must have breakdown voltages that are in excess of twice the supply voltage because at the peak voltage swings one or the other transistor has twice the peak voltage across it, but transistors Q_1 and Q_2 must only have breakdown voltages of

$$V_{breakdown} \geq V_{supply} \quad (3.1\text{-}1)$$

It will therefore be necessary to have power transistors in the output stage since peak currents in the range of 50-100 mA will be supplied to the total load capacitance.

High voltage power devices have relatively low f_T's and have high collector to base capacitances, C_{ob}, because of the large area required for the power dissipation capability. With large gains at the output stage, which

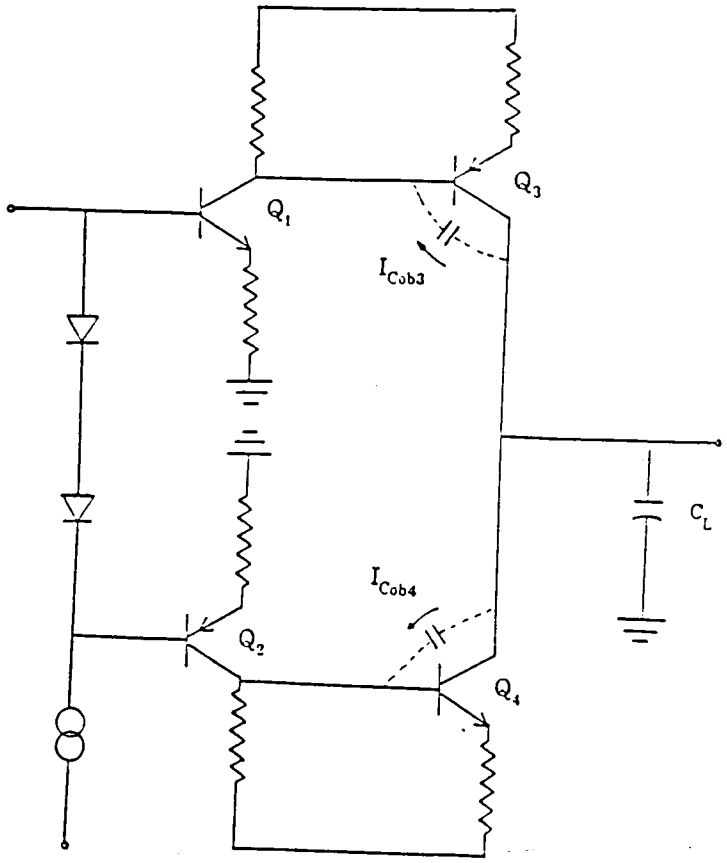

Figure 3.2. Common emitter complementary output configuration.

consists of transistors Q_3 and Q_4, pole interaction will be present and because of the consequent large time constants at the output stage the overall frequency response will be determined there. As the frequency of the output signal increases, the current required to charge up the load and the output device capacitances will increase proportionally as predicted by the equation for displacement current through a capacitor. For a sinusoidal voltage of maximum amplitude V_{max}, the peak current required is

$$i_p = 2\pi f C V_{max} \qquad (3.1\text{-}2)$$

The current also increases proportionally with an increase in capacitance, C. Large C_{ob} values thus increase the amount of current required by the output transistors. This additional current will flow through the C_{ob}'s of transistors Q_3 and Q_4 and are shown as I_{Cob3} and I_{Cob4} in Fig. 3.2, and this leads to a lower power efficiency. Reducing these capacitances will in some cases improve the power efficiency substantially. This improvement can be achieved by using power MOS transistors. In addition to lower gate-drain capacitances than bipolar base-collector capacitances, the MOS device is also generally thermally stable because the channel resistance increases with temperature thereby stabilizing the output current. The only minor drawback of MOS devices is that the gate voltage to bias the MOS device is much greater than that required to bias a bipolar, which leads to an increased quiescent current in the pre-output stage. The advantages however might outweigh the disadvantages, and this configuration is shown in Fig. 3.3.

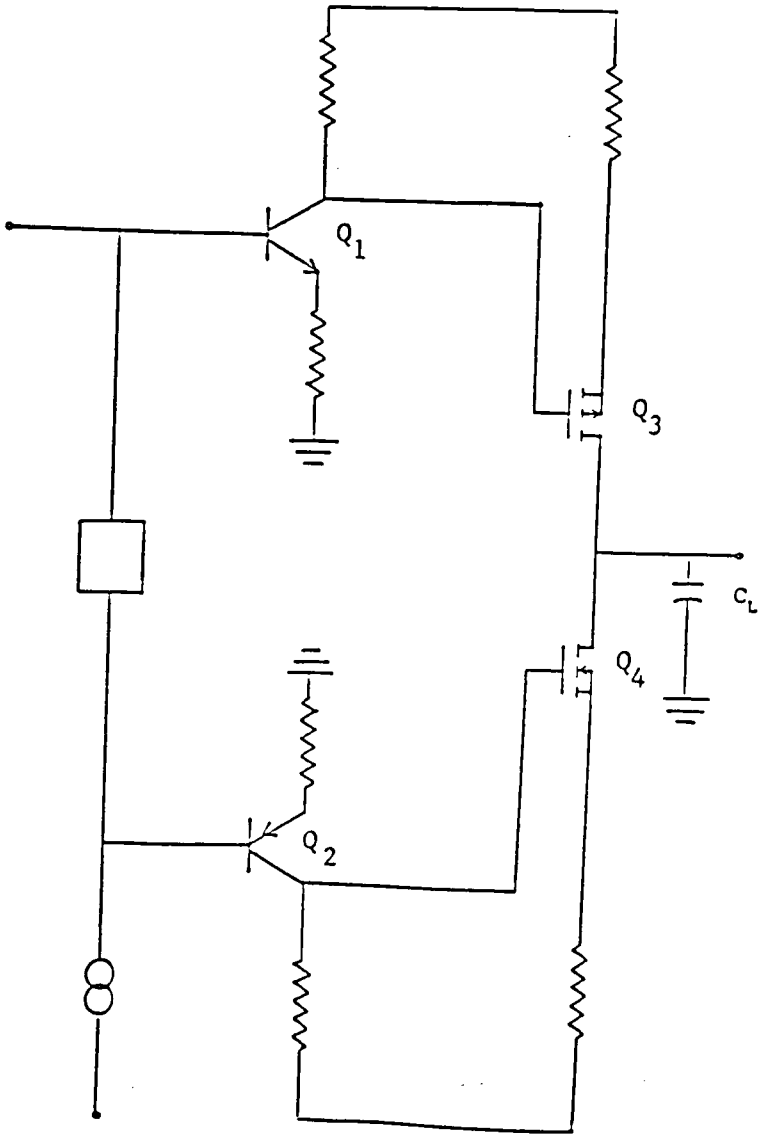

Figure 3.3. Complementary common-drain output stage.

Yet another alternative is a complementary cascode output stage shown in Fig. 3.4. The advantages and problems of this configuration will be briefly mentioned in Chap. 4 because this configuration has potential to be a fast output configuration.

The configuration implemented in this design is the one shown in Fig. 3.2 because of its inherent oscillation stability characteristics that are due to the Miller effect at the output stage rendering the amplifier stable under all load conditions. The analysis and results developed here should be applicable to similar circuit configurations and others driving capacitive loads.

3.1.2 Low Voltage Section

The design of the low voltage section does not involve any special design considerations for its configuration. A straight forward design is a differential input stage followed by a cascode stage and then a buffer stage between the low and high voltage sections of the amplifier. A very high frequency response is achievable with this type of design and is important in this application since the overall response of the amplifier is dominated by that of the high voltage section and any negative effects from the low voltage section are avoided. Voltage mixing feedback is implemented with a differential input stage so that a stabilized voltage gain is achieved. In Fig. 3.5 the driver amplifier is shown in its entirety.

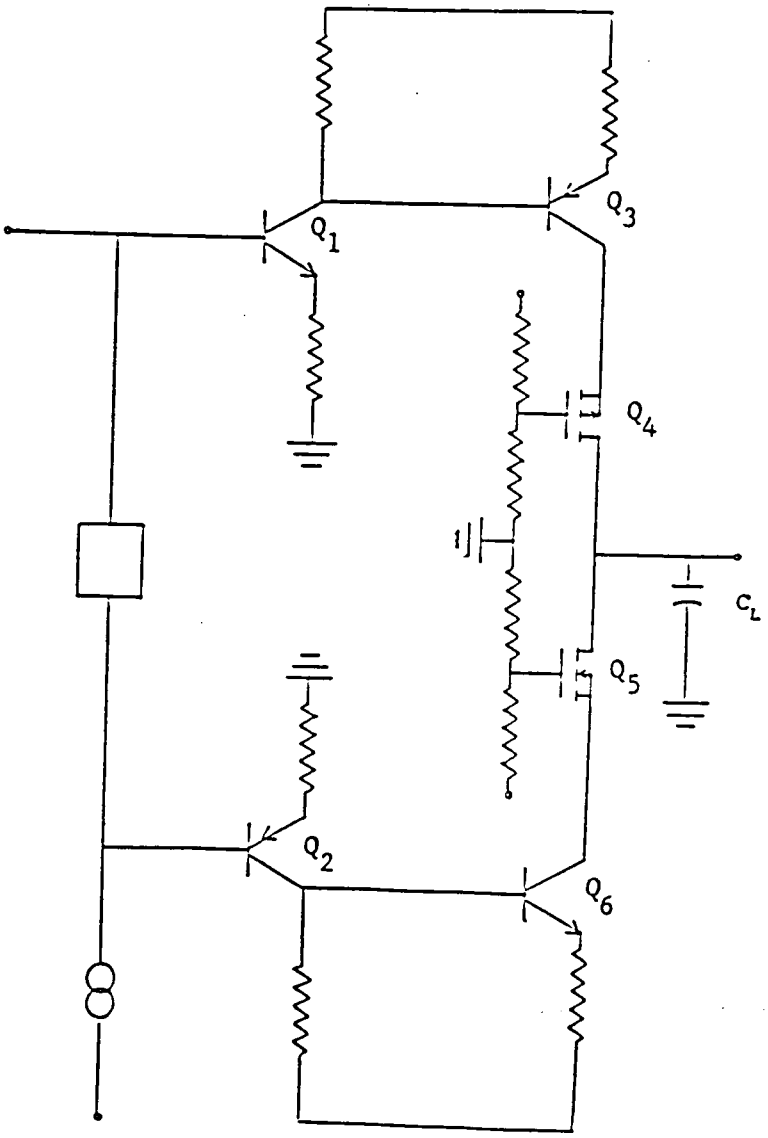

Figure 3.4. Complementary cascode output stage.

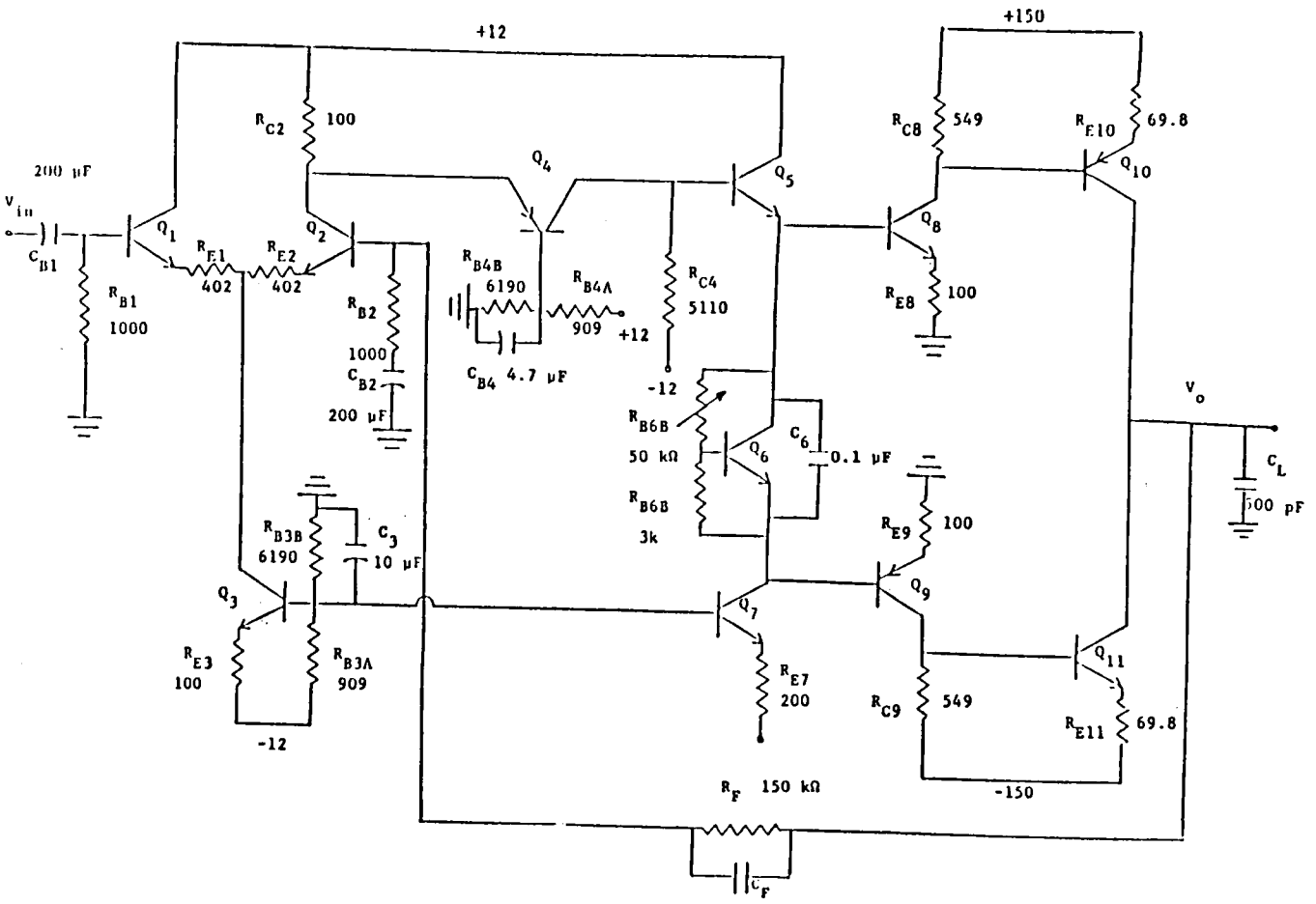

Figure 3.5. Complete schematic of driver amplifier. (note: All resistor value in Ωs unless otherwise indicated)

3.2 Design Equations

3.2.1 Frequency Response

In this section, design equations that allow an approximate determination of the small-signal frequency response and oscillation stability of the driver amplifier are developed. The midband gain of the amplifier, from Eqs. (2.2) and (2.6), is

$$A_{CL}^{mid} = \frac{R_F + R_{B2}}{R_{B2}} \quad \frac{|T_{mid}|}{1 + |T_{mid}|} \qquad (3.2\text{-}1)$$

The midband loop transmission T_{mid} is calculated by breaking the feedback loop between the base of transistor Q_2 and the feedback resistor R_F. The resistance looking towards R_F is very large but towards the base of transistor Q_2 is much smaller comprising R_{B2} in parallel with the base impedance of Q_2. This calls for injecting a current into the base of transistor Q_2 and then measuring the returned signal which in this case is the current flowing through R_F. The small-signal midband loop-gain, T_{mid}, is

$$T_{mid} = \frac{I_r}{I_t} = 2\left(R_{B2} \| R_{in2}\right)\left(A_2\right)\left(A_4\right)\left(A_5\right)\left(A_8\right)\left(A_{10}\right)\left(\frac{1}{R_F}\right), \qquad (3.2\text{-}2)$$

where the factor of two is a consequence of both signal paths at the output stage, being on at the same time and where A_2-A_{10} are the voltage gains of the respective transistor stages. Equal gains have been assumed in both

output stage paths. However, as the signal level increases and one of the paths starts turning off, the factor of two will start decreasing eventually becoming unity. This gain change caused by a change in signal level is not present for the emitter-follower complementary output configuration. The loop transmission T_{mid} will become T_{midh} at high signal levels and will be approximately half the value of T_{mid}. The base impedance of transistor Q_2 is

$$R_{in2} = \left(\beta_2 + 1\right)\left(r_{e1} + r_{e2} + R_{E1} + R_{E2} + \frac{R_{B1}}{\beta_1 + 1}\right). \tag{3.2-3}$$

The voltage gain of transistor Q_2 stage is

$$A_2 = - \frac{\left(R_{C2} \| r_{e4}\right)\left(\beta_2 + 1\right)}{R_{in2}}, \tag{3.2-4}$$

and that of transistor Q_4 is

$$A_4 = \frac{R_{C4} \| r_{o4} \| R_{in5}}{r_{e4}}, \tag{3.2-5}$$

where r_{o4} and R_{in5} are the output and input impedances of transistors Q_4 and Q_5, respectively. The output impedance of transistor Q_4 is large due to the ac-grounded base, and the input impedance of transistor Q_5 is large because of the large total emitter resistance of Q_5 that is multiplied by (β_5 + 1). The impedance looking towards the collector of the V_{BE} multiplier is

equivalent to the impedance at its emitter (see Appendix A for the derivation). The capacitor, C_6, across the V_{BE} multiplier insures that the multiplier is a short-circuit to ac signals. The voltage gain of transistor Q_5 stage is approximately unity and that of transistor Q_8 is

$$A_8 = - \frac{R_{C8} \| \left[\left(\beta_{10} + 1 \right) \left(R_{E10} + r_{e10} \right) \right] \| r_{o8}}{r_{e8} + R_{E8}} , \tag{3.2-6}$$

where

$$r_{o8} = r_{ce8} \left\{ \frac{1 + \left[R_{e8} \| \left(r_{e8} + \frac{R_{b8}}{\beta_{8+1}} \right) \right] / r_{ce8}}{1 - \left(\frac{\beta_8}{\beta_{8+1}} \right) \left(\frac{R_{e8}}{R_{e8} + r_{e8} + \frac{R_{b8}}{\beta_{8+1}}} \right)} \right\} , \tag{3.2-7}$$

and where R_b and R_e are the total resistances at the base and emitter, respectively [7]. This equation is applicable for any stage if the subscripts are changed appropriately.

The voltage gain of transistor Q_{10} stage is

$$A_{10} = - \frac{R_F \| r_{o10} \| r_{o11}}{r_{e10} + R_{E10}} , \tag{3.2-8}$$

where r_{o10} and r_{o11} are the output impedances of transistors Q_{10} and Q_{11}, respectively, and can be determined from Eq. (3.2-7) after r_{ce} is determined from the following equation,

$$r_{ce} \approx \frac{V_A}{I_C} , \tag{3.2-9}$$

where V_A is the Early voltage of the transistor and I_C is the collector current in milliamperes.

To find the transfer function and closed-loop oscillation stability of the driver amplifier, the poles and zeroes of the system must be determined. These are approximated by obtaining the time constants at each node and relating them to the critical frequencies by

$$f_p = \frac{1}{2\pi \tau_{node}} . \tag{3.2-10}$$

The time constant, τ_{node}, is the product of the total resistance and total capacitance in parallel at that node except when interaction requires the determination of effective time constants. The time constant at the base of transistor Q_2 is

$$\tau_{B2} = \left(R_{B2} \| R_{in2} \| R_F \right) \left(C_F + C_{in2} \right) , \tag{3.2-11}$$

where

$$C_{in2} = C_{ob2}\left(1 - A_2\right) + \left(C_{\pi 2} - C_{ob2}\right)\left(1 - A_{2cc}\right) , \tag{3.2-12}$$

and where C_{0b} is defined as the base to collector capacitance of any transistor,

$$C_{\pi 2} = \frac{1}{2\pi\, r_{e2} f_{T2}} , \tag{3.2-13}$$

and A_{2cc} is the voltage gain of transistor Q_2 from its base to its emitter and is given by

$$A_{2cc} = \frac{R_{E1} + R_{E2} + r_{e1} + \dfrac{R_{B1}}{\beta_{1+1}}}{r_{e1} + r_{e2} + R_{E1} + R_{E2} + \dfrac{R_{B1}}{\beta_{1+1}}} . \tag{3.2-14}$$

The time constant at the collector of transistor Q_2 is

$$\tau_{c2} = \left(R_{C2} \| r_{e4}\right)\left[C_{ob2} + C_{\pi 4} - C_{ob4}\right] , \tag{3.2-15}$$

but since the resistance at the collector of transistor Q_2 is approximately r_{e4}, then

$$f_{c2} \approx f_{T4} . \tag{3.2-16}$$

At the base of transistor Q_5, the time constant is

$$\tau_{B5} = R_{C4}\left[C_{ob4} + C_{ob5} + \left(C_{\pi 5} - C_{ob5}\right)\left(1 - A_{5cc}\right)\right] . \tag{3.2-17}$$

The capacitance $(C_{\pi 5} - C_{ob5})(1 - A_{5cc})$ is negligibly small since the voltage gain A_{5cc} is very close to unity. At the base of transistor Q_8, the time constant is

$$\tau_{B8} = \left(r_{e5} + \frac{R_{C4}}{\beta_{5+1}}\right)\left(C_{in8} + C_{o5} + C_{ob7} + C_{ob9}\right) , \tag{3.2-18}$$

where

$$C_{in8} = C_{ob8}\left(1 - A_8\right) + \left(C_{\pi 8} - C_{ob8}\right)\left(1 - A_{8cc}\right) , \tag{3.2-19}$$

$$C_{o5} \approx \frac{1}{2\pi f_{T5}\left(r_{e5} + \dfrac{R_{C4}}{\beta_{5+1}}\right)} , \tag{3.2-20}$$

and

$$A_{8cc} = \frac{R_{E8}}{r_{e8} + R_{E8}} . \tag{3.2-21}$$

The critical frequency associated with τ_{B8} is very high since the impedance at that point is very low. It was found that there is negligible pole

interaction between the collector and the base nodes of Q_8; and therefore these nodes will be considered as independent. When considering the frequency response of transistors Q_{10} and Q_{11}, pole interaction is very important because of the high voltage gains of these transistors and also because of their large capacitances. As will be shown later, the presence of pole interaction and the large time constant at the bases of Q_{10} and Q_{11} is very advantageous because it allows the system to remain stable without load capacitance.

The transistors Q_{10} and Q_{11} have different base-collector capacitances, C_{ob}, and different current gains, β, and this will cause the response to be different for the positive and negative transistions of the output voltage since at high signal levels only one transistor is on at a time. At low signal levels, however, both the NPN and PNP output transistors are on, or partially on and the signal at the output is the sum of the signals through both paths. To make the analysis simpler, the frequency response of the worst case path only will be used.

To apply the approximate results of pole interaction [7, 8] the base and collector time constants must be determined and then combined. For the path through transistor Q_{10}, the time constant at the base of transistor Q_{10} is

$$\tau_{B10} = \left[R_{C8} \| \left(\beta_{10} + 1\right)\left(r_{e10} + R_{E10}\right)\right]\left[C_{ob8} + C_{in10}\right] , \qquad (3.2\text{-}22)$$

where

$$C_{in10} = C_{0b10}\left(1 - A_{10}\right) + \left(C_{\pi 10} - C_{ob10}\right)\left(1 - A_{10cc}\right) , \tag{3.2-23}$$

and where A_{10cc}, the voltage gain from the base to emitter of transistor Q_{10} is

$$A_{10cc} = \frac{R_{E10}}{R_{E10} + r_{e10}} . \tag{3.2-24}$$

At the collector of transistor Q_{10} the time constant is

$$\tau_{c10} = \left[R_F \| r_{010} \| r_{011}\right]\left[C_L + C_{ob10} + C_{ob11}\right] . \tag{3.2-25}$$

The time constants τ_{c10} and τ_{B10} interact and give the overall time constants after being combined. The dominant time constant is therefore [2]

$$\tau_1 = \tau_{B10} + \tau_{c10} \tag{3.2-26}$$

and the higher time constant is

$$\tau_2 = \left(R_{in10} \| R_{c8}\right)\left(R_F \| r_{010}\right)\left\{ \frac{\left[C_{ob8} + \left(C_{\pi 10} - C_{ob10}\right)\left(1 - A_{10cc}\right)\right]\left[C_L + C_{ob11}\right]}{\tau_1} \right.$$

$$\left. \frac{+ C_{ob10}\left[C_L + C_{ob11} + C_{ob8} + \left(C_{\pi 10} - C_{ob10}\right)\left(1 - A_{10cc}\right)\right]}{\tau_1} \right\} . \tag{3.2-27}$$

A critical frequency associated with a zero that causes phase shift occurs at

$$f_{zo} = -g_{m10}/C_{ob10} \tag{3.2-28}$$

To obtain the frequency response through transistor Q_{11}, Eqs. (3.2-22) through (3.2-27) are employed after changing to the appropriate subscripts. The critical frequency associatd with the zero in Eq. (3.2-28) is not included in the frequency response because it occurs at a very high frequency.The oscillation stability of the system is controlled by the small signal response. The large signal response affects the risetime of the output pulse response. The small-signal loop transmission is

$$T(f) = T_{mid}\left(\frac{1}{1 + jf/_{f1}}\right)\left(\frac{1}{1 + jf/_{f2}}\right)\left(\frac{1}{1 + jf/_{fb2}}\right)\left(\frac{1}{1 + jf/_{fb5}}\right)\left(\frac{1}{1 + jf/_{fb8}}\right). \tag{3.2-29}$$

If f_1 is much lower than all the other critical frequencies, then the system transfer function can be roughly approximated as a single-poled function with a crossover frequency occuring at

$$f_c = T_{mid} \cdot f_1 \ . \tag{3.2-30}$$

The stability of the system is affected by how close f_c is to the lowest non-dominant pole in T(f), deteriorating as that pole approaches f_c. A rough estimate of the closed loop high frequency -3 dB point can be obtained from

Eq. (3.2-30) but for more accurate results, it is necessary to obtain the results from the complete expression of T(f) given in Eq. (3.2-29).

3.2.2 Input and Output Impedances

The input and output impedances of the driver amplifier are determined by using Blackman's Theorem [7], which states that the closed loop impedance across any two terminals in the circuit is obtained by finding the open loop impedance looking into the terminals and the loop transmissions with the terminals shorted and left open. The following equation is then applied

$$Z^{c\ell} = Z^{o\ell} \frac{1 - T_{sc}(f)}{1 - T_{oc}(f)} , \qquad (3.2\text{-}31)$$

where $T_{sc}(f)$ and $T_{oc}(f)$ are the short-circuited and open circuited loop transmissions, respectively. The input and output impedances have the form of Eq. (3.2-31) and the impedances refer to the input terminals in one case and the output terminals in the other.

The loop transmissions, $T_{sc}(f)$ and $T_{oc}(f)$ are calculated in the same way as the system loop transmission, T(f). The effect of feedback on the input and output impedances is seen by examining T_{oc} and T_{sc}. For a voltage summing amplifier, T_{oc} approaches zero causing the closed loop input impedance, $Z_{in}{}^{c\ell}$, to be a factor of $(1 - T_{sc})$ greater than the open-loop input impedance, $Z_{in}{}^{o\ell}$. For a current summing amplifier, however, $T_{sc}(f)$ is zero

and the input impedance is reduced by a factor of $(1 - T_{oc})$. This approach also illustrates the effect of feedback on the output impedance, and in the case of a voltage sampling amplifier, $T_{sc}(f)$ is zero and the open loop output impedance is divided by $(1 - T_{oc})$. For the specific case here, the open loop input impedance over a wide frequency range is

$$Z_{in}^{o\ell} = R_{B1} \| R_{in1} \ , \tag{3.2-32}$$

where R_{in1} is approximately equal to R_{in2}. The loop transmissions $T_{sc}(f)$ and $T_{oc}(f)$ will be approximately equal since the presence of R_{B1} does not allow $T_{oc}(f)$ to approach zero, therefore

$$Z_{in}^{c\ell} \approx Z_{in}^{o\ell} \ . \tag{3.2-33}$$

For the output impedance, $T_{sc}(f)$ is zero and the output impedance of a common-emitter stage is used to characterize the open loop output impedance of the driver amplifier. The open loop output impedance is [App. D]

$$Z_{out}^{o\ell} \approx \frac{R_L' \left(1 + R_b j2\pi f C_{ob} \right)}{1 + R_b j2\pi f C_{ob} \left[R_L \left(\frac{1}{R_L'} + \frac{2}{R_b} + 2 g_m' \right) \right]} \ , \tag{3.2-34}$$

where R_L is equal to $R_F \| r_{o10} \| r_{011}$, R_b is the total equivalent resistance at the bases of transistors Q_{10} and Q_{11}, g_m' is the transconductance including the

effect of the emitter resistors R_{E10} and R_{E11} and C_{ob} is the average value of C_{ob10} and C_{ob11}. The open circuit loop transmission $T_{oc}(f)$ is equal to the no-load system loop transmission, $T^{NL}(f)$, leading to an output impedance that is

$$Z_{out}^{c\ell} = Z_{out}^{o\ell} \frac{1}{1 - T_{oc}(f)} \quad . \tag{3.2-35}$$

3.2.3 Transient Response

To determine the frequency response of the amplifier, the small signal characteristics of the active devices were used. The response of the circuit to large signals is quite different from the small signal response and the circuit displays limitations not observable at low signal levels. Studying the transient response of the driver amplifier allows these effects to be determined and corresponding design decisions to be made. In most amplifiers, the large signal response is usually limited by slewing and occurs in most cases at the dominant node. Since the voltage across a capacitance cannot change instantaneously with a finite charging current, in response to a step input the output voltage will change at a fixed rate controlled by the available amount of current and the total capacitance of that node. In most amplifiers the dominant node usually occurs between the differential input stage and the common-emitter gain stage and slewing therefore occurs at that node [7,8,9,10,11]. The slew rate for a constant charging current I is obtained from the charging equation of a capacitor, where dV/dt is the slew rate,

$$S.R = \frac{dV}{dt} = \frac{I}{C} \tag{3.2-36}$$

From Eq. (3.1-2), the maximum frequency that can be amplified without slewing is

$$f_{max} = \frac{S.R}{2\pi V_m} , \tag{3.2-37}$$

where V_m is the maximum output voltage. The feedback will attempt to correct distortion, of which slewing is one type, causing the input stages to supply all the current to charge the capacitor so that the output voltage will follow the input voltage as closely as possible. The signals in the forward path reflect the effect of the feedback in correcting the distortion. The error signal, which is the difference between the input voltage and an attenuated version of the output voltage is a function of the distortion at the output. The error signal becomes the correction signal after amplification.

For the driver amplifier being analyzed here, the large capacitance is at the output and so it is expected that the slew limiting will occur there. In the event of a step input, the output stage requires a large amount of current to charge the capacitor up to a high voltage. Since the driver amplifier has a finite risetime due to the time constants, the slew rate must be high enough so that the time constant response won't be limited. If the current is limited at a level that is below the required amount, then slewing in the output step response would occur. One observes from Fig. 3.5 that

the amount of current available to the load depends on how much Q_{10} or Q_{11} is turned on; This current is

$$I_L = \frac{\Delta V_{E10}}{R_{E10}} = \frac{\Delta V_{E11}}{R_{E11}} \quad , \tag{3.2-38}$$

Theoretically, ΔV_{E10} is limited by how low the base voltage of transistor Q_{10} can be and that limit is the base voltage of Q_8, therefore ΔV_{E11} can go as low as V_{B8}. Since the voltage gain of transistor Q_8, A_8 is finite and the voltage at the base of transistor Q_8 is limited by the saturation of transistor Q_4, then the base voltage of transistor Q_{10} can go as low as the saturated collector voltage of transistor Q_4. If the required load current is achieved before Q_4 saturates then slewing will not be observable. The maximum slew rate is therefore,

$$S.R = \frac{\left(\Delta V_{B5}\right)_{max}\left(A_8\right)}{\left(C_{TOTAL}\right)\left(R_{E10}\right)} \quad , \tag{3.2-39}$$

where C_{TOTAL} is the load capacitance plus the C_{ob}'s of transistors Q_{10} and Q_{11}. The feedback, if sufficient loop transmission is available, will always respond to supply the load current, I_L, that is required to charge the load up with a risetime equivalent to that of the system. Current multiplication exists between transistors Q_8 and Q_{10} and also between transistors Q_9 and Q_{11} and relates the currents I_{c10} and I_{c8} by

$$\Delta I_{c10}^{max} = \Delta I_{c8}^{max} \cdot \quad k \ , \tag{3.2-40}$$

where

$$k = \frac{R_{C8}}{R_{E10}} \ . \tag{3.2-41}$$

Eq. (3.2-39) therefore becomes

$$S.R = \frac{\Delta V_{B5}^{max} \cdot \quad k}{C_{TOTAL} \cdot \quad R_{E8}} \ . \tag{3.2-42}$$

The slew rate can therefore be controlled by adjusting the parameters in Eq. (3.2-42). The slew rate can thus be set to a high value if the variables in Eq. (3.2-42) are adjusted correctly and oscillation stability is maintained. If one needs to reduce the large transient voltages and currents without decreasing the slew rate, a low-pass filter can be placed at the input to reduce the risetime of the input signal thereby allowing adequate output voltage response with the consequent reduction in transient currents because of the reduced error signal [12]. The output risetime is now approximately given by

$$\tau_r = \sqrt{\tau_{input}^2 + \tau_{amp}^2} \tag{3.2-43}$$

indicating a decreased bandwidth; however, as long as the bandwidth is more than twice the highest frequency of interest, this decrease in

bandwidth can be tolerated in exchange for the decrease in transient currents.

3.2.4 Power Dissipation

At high voltage levels, even low current flow means that substantial power dissipation in the high voltage section will occur. In this section, the necessary equations which give the power dissipation in the high voltage output stages are determined so that devices that can safely handle those power dissipation levels can be chosen.

The quiescent power dissipation in the output stage is equal for both transistors Q_{10} and Q_{11} and is given by

$$P_{Q_{10}} = P_{Q_{11}} \approx I_Q |V_H| \ , \tag{3.2-44}$$

where I_Q is the quiescent dc current at the output and V_H is the voltage of the high voltage supply. The quiescent power dissipated in the pre-output stage which consists of transistors Q_8 and Q_9 and have equal power dissipation that can be expressed as

$$P_{Q8} = P_{Q9} = \left[V_H - \left(I_{Q10} R_{E10} + V_{BE10} \right) \left(1 + \frac{R_{E8}}{R_{C8}} \right) \right] \left[\frac{I_{Q10} R_{E10} + V_{BE10}}{R_{C8}} \right]. \tag{3.2-45}$$

For a sinusoidal signal, the voltage and current at the output are 90° out of phase due to the capacitive load. For maximum signal levels, the output devices are on and off alternately and in Fig. 3.6 the output voltage

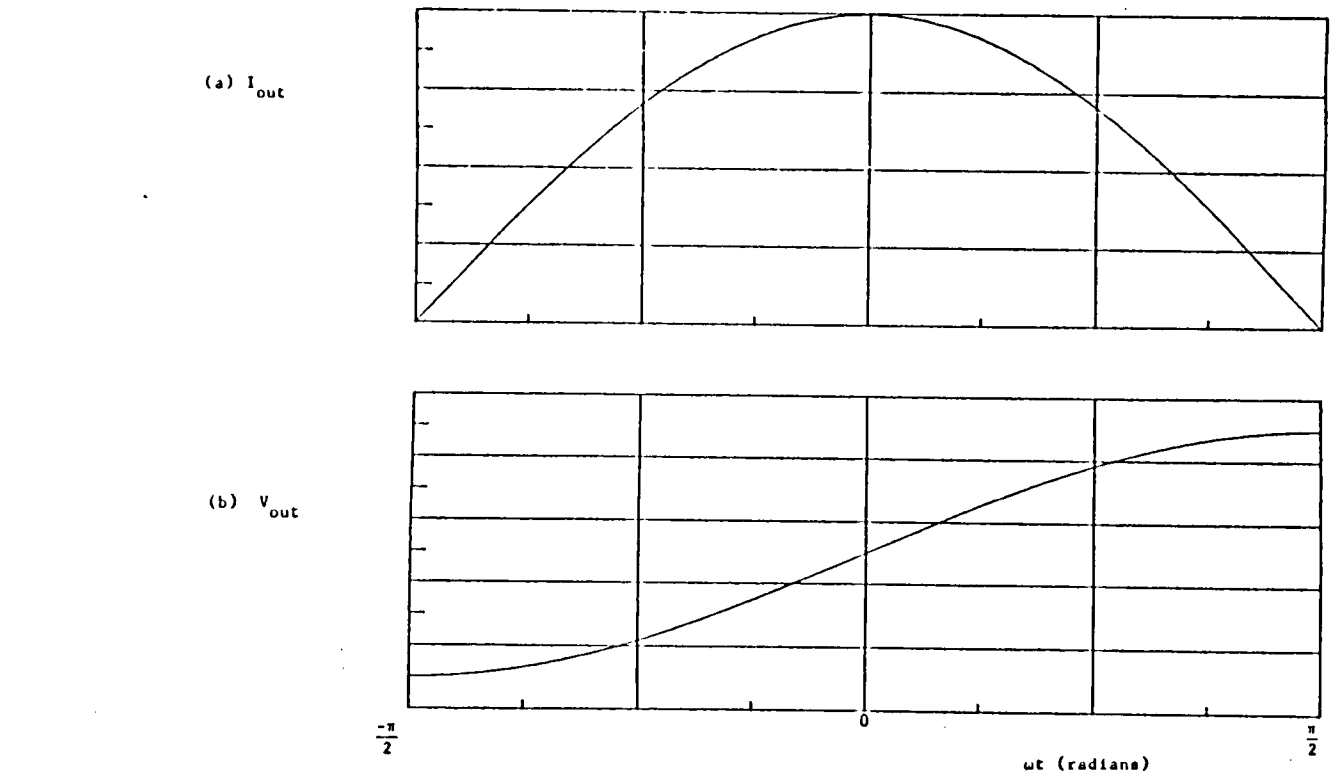

Figure 3.6. The relationship between the current and voltage at the output node when transistor Q_{10} is on: (a) The current through transistor Q_{10} and (b) the voltage at the output-collector of Q_{10}.

and current are shown when Q_{10} is on. Due to the symmetry of the circuit, the power dissipated in each half cycle is identical, hence the same results will hold true for both portions. For a sinusoidal voltage at the output which is expressed as

$$v_o = V_m \sin \omega_m t \ , \tag{3.2-46}$$

where V_m is the maximum output voltage and ω_m is the maximum frequency of interest, the following equation predicts the current at the output:

$$i_o = C_{TOTAL} V_m \omega_m \cos \omega_m t \ , \tag{3.2-47}$$

and the maximum current will be defined as

$$I_m = C_{TOTAL} V_m \omega_m \ . \tag{3.2-48}$$

The instantaneous power dissipation of one of the output transistors is

$$P_{io} = \left(V_{HP} - i_o R_E - v_o \right) i_o \ , \tag{3.2-49}$$

where V_{HP} is the positive power supply and the subscripts $\underline{i}$ and $\underline{o}$ indicate instantaneous and output, respectively. Substituting the expressions for i_o and v_o given by Eqs. (3.2-46) and (3.2-47) into Eq. (3.2-49), P_{io} then becomes

$$P_{io} = \left(V_{HP} - I_m R_E \cos \omega_m t - V_m \sin \omega_m t \right) I_m \cos \omega_m t \ , \qquad (3.2\text{-}50)$$

or

$$P_{io} = V_{HP} I_m \cos \omega_m t - I_m^2 R_E \cos^2 \omega_m t - \frac{I_m V_m}{2} \sin 2\omega_m t \ . \qquad (3.2\text{-}51)$$

The output transistors are chosen depending on their power-handling capability and the maximum average power dissipated by the transistors. The average power dissipated in the output transistors, Q_{10} and Q_{11} is found by integrating Eq. (3.2-51) over one period with $P_{io} = 0$ on the second half cycle. The average value of P_{io} for transistor Q_{10} or Q_{11} is thus

$$\bar{P}_{io} = \frac{1}{2\pi} \int_{-\pi/2}^{\pi/2} P_{io} \, d\omega_m t = \frac{V_{HP} I_m}{\pi} - \frac{I_m^2 R_E}{4} + \frac{I_m V_m}{4\pi} \ , \qquad (3.2\text{-}52)$$

where the bar over the variable indicates an average value. The maximum average power can be found by taking the derivative of P_{io} with respect to I_m, setting the expression equal to zero and then solving for I_m, which is the current that gives maximum P_{io}. The derivative of Eq. (3.2-52) with respect to I_m is

$$\frac{d \bar{P}_{io}}{d I_m} = \frac{V_{HP}}{\pi} - \frac{I_m R_E}{2} + \frac{V_m}{4\pi} \ . \qquad (3.2\text{-}53)$$

Setting the right hand side of Eq. (3.2-53) to zero and solving for I_m gives

$$I_m = \frac{2}{R_E}\left(\frac{V_{HP}}{\pi} + \frac{V_m}{4\pi}\right) . \qquad (3.2\text{-}54)$$

The maximum P_{io} is obtained by substituting the value of Eq. (3.2-54) into Eq. (3.2-51).

The power dissipation in the pre-output stage under the same conditions is determined for transistor Q_8 and a similar analysis holds for transistor Q_9. The dynamic collector current of transistor Q_8 from Eq. (3.2-49) is

$$i_{c8} = \frac{I_{C10}}{k} = \frac{I_m \cos \omega_m t}{k} , \qquad (3.2\text{-}55)$$

where k is the current multiplication factor between transistors Q_8 and Q_{10} and the base current of transistor Q_{10} is assumed negligible. The instantaneous power dissipation in transistor Q_8 is

$$P_{i8} = v_{ce8} \cdot i_{c8} , \qquad (3.2\text{-}56)$$

where the instantaneous voltage, v_{ce8} across Q_8 is

$$v_{ce8} = V_{HP} - i_{c8} R_{C8} - i_{c8} R_{E8} . \qquad (3.2\text{-}57)$$

The expression in Eq. (3.2-57) can also be written as

$$P_{i8} = \frac{V_{HP} I_m}{k} \cos \omega_m t - \frac{\left(R_{C8} + R_{E8}\right) I_m^2}{k^2} \cos^2 \omega_m t \ . \qquad (3.2\text{-}58)$$

Integrating Eq. (3.2-58) yields the average power dissipated in transistor Q_8 and is

$$\overline{P}_{i8} = \frac{2 V_{HP} I_m}{\pi k} - \frac{\left(R_{C8} + R_{E8}\right)}{4k^2} I_m^2 \qquad (3.2\text{-}59)$$

Taking the derivative of Eq. (3.2-59) with respect to I_m, setting the expression to zero, and solving for I_m gives

$$I_m = \frac{4 V_{HP}}{\pi\left(R_{C8} + R_{E8}\right)} \ , \qquad (3.2\text{-}60)$$

and subsituting into Eq. (3.2-59) yields the maximum average power dissipated in transistor Q_8. In Appendix B the derivation for calculating the thermal stability and heat sink requirements are shown.

3.3 Numerical Analysis

The design equations presented in the previous sections are used in this section to numerically specify the driver amplifier design. The choice of components values and devices will be explained where necessary. The

bias conditions and characteristics of the devices used are shown in Table 3.1. All the following calculations will refer to Table 3.1 and Fig. 3.5, p. 18.

3.3.1 Frequency Response and Stability

Due to the large output voltage swing, the overall closed loop gain of the amplifier will have to be high so that the input for maximum output voltage will not be prohibitively large. The feedback resistor, R_F will also have to be quite large so that it will not load down the output at high voltage swings. For an R_F of 150 kΩ and an R_{B2} of 1kΩ. The ideal closed-loop gain is

$$A_{CL}^{ideal} = \frac{150 + 1}{1} = 151 \ . \qquad (3.3\text{-}1)$$

To obtain the actual closed loop gain, one must first determine the loop gain, T(f). For $T >> 1$, the midband closed loop gain will be close to $A_{CL}{}^{ideal}$. When the maximum voltage is desired at the output, the input voltage will only have to be 1 V_{peak} and the current supplied from the output stage to the feedback resistor, R_F, will be 1 mA peak. The individual stage gains must be determined before T_{mid} and T_{midh} can be obtained. From Eq. (3.2-3), the input impedance of transistor Q_2 is

$$R_{in2} = \left(151\right)\left(6.5 + 6.5 + 402 + 402 + \frac{1\,k\Omega}{151}\right) = 124.4\,k\Omega \ , \qquad (3.3\text{-}2)$$

and from Eq. 3.2-4, the voltage gain of the transistor Q_2 stage is

Table 3.1 Parameters and operating conditions of the semi-conductor devices used in the hand analysis of the driver amplifier.

Transistor	Type	I_c(mA)	r_e(Ω)	C_u(pF)	C_{ob}(pF)	f_t(MHz)	β
Q_1, Q_2	MP311	4	6.5	82	2	300	150
Q_3	2N4401	7.5	3.5	226	6	200	80
Q_4	MPSH81	2.8	9.3	29	0.8	600	80
Q_5	2N5962	3.8	6.8	233	3	100	800
Q_6	2N4401	3.6	7.2	110	6	200	80
Q_7	2N4401	3.8	6.8	117	6	200	80
Q_8	2N6515[1]	0.57	46	70	6	50	80
Q_9	2N6519[1]	0.57	46	70	6	50	80
Q_{10}	2N6123[2]	4.5	5.8	470	60[4]	58	20-30
Q_{11}	TIP50[3]	4.5	5.8	1400	30[4]	20	40-44

[1] Three of each are connected in parallel for higher power dissipation, both have power dissipation of 0.6 W and breakdown voltages of 150 V.
[2] Breakdown voltage = 350 V, power dissipation = 35 W.
[3] Breakdown voltage = 400 V power dissipation = 40 W.
[4] These are average values.

$$A_2 = \frac{-\left(151\right)\left(100 \| 9.3\right)}{124.4\ \text{k}\Omega} = -0.01 \ . \tag{3.3-3}$$

The voltage gain of Q_4 is

$$A_4 \approx \frac{5110}{9.3} = 550 \ , \tag{3.3-4}$$

and of Q_8 is

$$A_8 \approx - \frac{549 \| [(21)(75.6)]}{115} = -3.8 \tag{3.3-5}$$

R_{C8} was chosen to be 549 Ω so that the current multiplication factor, k will be of a value that gives the necessary slew rate without being so large as to limit the frequency response at the collector of Q_8. The output resistance of transistor Q_8 can be neglected since it is much higher than R_{C8}. The voltage gain of the transistor Q_{10} stage at small signal levels from Eqs. (3.2-7) and (3.2-9) is

$$A_{10} = \frac{-150\ \text{k}\Omega \| 603\ \text{k}\Omega \| 320\ \text{k}\Omega}{75.6} = -1152 \ . \tag{3.3-6}$$

The emitter resistor of transistor Q_{10}, R_{E10}, was chosen to be 69.8 Ω so that it will stabilize the output quiescent current and not be so large as to drop significant voltage across it and limit the output voltage swing. The value of R_{E10} also affects the multiplication factor, k, and therefore the slew rate; so R_{E10} must be chosen appropriately. The small-signal midband loop gain is therefore

$$T_{mid} = 2\left(992\right)\left(-0.01\right)\left(550\right)\left(-3.8\right)\left(-1152\right)\left(\frac{1}{150k}\right) = -316 . \qquad (3.3\text{-}7)$$

For large signals levels one of the output transistors turns-off and the midband loop transmission, T_{mid} will be reduced by a factor of two; however, the voltage gain of transistors Q_{10} or Q_{11} increases when the other transistor turns off causing an increase in the output impedance as described by Eqs. (3.2-7) and (3.2-9). The large-signal loop gain is, therefore,

$$T_{midh} \approx -183 . \qquad (3.3\text{-}8)$$

To obtain the frequency response, the critical frequencies associated with all the nodes must be determined. At the base of transistor Q_2, the critical frequency is

$$f_{B2} = \frac{0.159}{992\left(2pF + 80pF\left(1 - 0.992\right)\right)} = 61\ MHz . \qquad (3.3\text{-}9)$$

At the collector of transistor Q_2, the critical frequency is

$$f_{c2} \approx 600 \text{ MHz} \ . \tag{3.3-10}$$

At the base of Q_5,

$$f_{B5} = \frac{0.159}{5.110\left(0.8 \text{ pF} + 3 \text{ pF}\right)} = 8.2 \text{ MHz} \ , \tag{3.3-11}$$

and at the base of Q_8,

$$f_{B8} = \frac{0.159}{13\left(6 \text{ pF} + 18 \text{ pF} + 22 \text{ pF} + 28 \text{ pF} + 86.4 \text{ pF}\right)} = 47 \text{ MHz} \ . \tag{3.3-12}$$

For the output transistors, Q_{10} and Q_{11} at small signal levels, the time constant at the base is

$$\tau_{B10} = \left[549 \parallel (20)(70)\right]\left[18 \text{ pF} + 0.0693 \ \mu\text{F} + 50 \text{ pF}\right] = 32 \ \mu\text{s} \tag{3.3-13}$$

and at the output node,

$$\tau_{c10} = \left(150 \text{ k}\Omega \parallel 320 \text{ k}\Omega \parallel 602 \text{ k}\Omega\right)\left(500 \text{ pF} + 60 \text{ pF} + 20 \text{ pF}\right) = 51 \ \mu\text{s} \ , \tag{3.3-14}$$

where an average value for C_{ob10} was used, and the output resistance was calculated using Eq. (3.2-7). From Eq. (3.2-6), the dominant time constant is

$$\tau_1 = 32\ \mu s + 51\ \mu s = 83\ \mu s\ , \tag{3.3-15}$$

corresponding to a critical frequency of

$$f_1 = 1.9\ kHz\ , \tag{3.3-16}$$

and the secondary time constant is found by using Eq. (3.2-27) and is

$$\tau_2 = \frac{460(87\ k\Omega)\left[86\ pF\left(520\ pF\right) + 60\ pF\left(590\ pF\right)\right]}{83\ \mu s} = 39\ ns\ , \tag{3.3-17}$$

corresponding to a critical frequency of

$$f_2 = 4.2\ MHz\ . \tag{3.3-18}$$

The frequency dependent loop transmission of the driver amplifier is thus

$$T(f) = -316\left(\frac{1}{1 + jf/1.9\ kHz}\right)\left(\frac{1}{1 + jf/4.2\ MHz}\right)$$
$$\left(\frac{1}{1 + jf/8.2\ MHz}\right)\left(\frac{1}{1 + jf/61\ MHz}\right)\left(\frac{1}{1 + jf/47\ MHz}\right) \tag{3.3-19}$$

Using numerical methods, the unity gain crossover frequency is approximately 590 kHz and the phase margin is 77°. Using numerical methods and Eqs. (2-2) and (3.2-1), the midband closed loop gain is

$$A_{CL}^{mid} = 151 \ \frac{316}{317} = 150.5 \ , \tag{3.3-20}$$

and the high frequency -3 dB point is at 795 kHz. At large signal levels, T_{midh} is substituted for T_{mid} and the value of the time constant at the base of transistor Q_{10} becomes

$$\tau_{B10}^{HL} = 460\left(18\ pF + 0.057\ \mu F\right) = 26.2\ \mu s \ . \tag{3.3-21}$$

and at the collector of transistor Q_{10}, the time constant is

$$\tau_{c10}^{HL} = 67\ k\Omega\left(580\ pF\right) = 39\ \mu s \ . \tag{3.3-22}$$

The dominant time constant is

$$\tau_1^{HL} = 65\ \mu s \ , \tag{3.3-23}$$

therefore

$$f_1^{HL} = 2.44\ k\Omega \ , \tag{3.3-24}$$

and the secondary critical frequency is at

$$f_2^{HL} = 5.9\ \text{MHz} \ . \tag{3.3-25}$$

At high signal levels, the loop transmission is

$$T^{HL}(f) = -183\left(\frac{1}{1+jf/2.44\ k\Omega}\right)\left(\frac{1}{1+jf/5.9\ MHz}\right)\left(\frac{1}{1+jf/8.2\ MHz}\right)\left(\frac{1}{1+jf/47 MHz}\right)\left(\frac{1}{1+jf/61\ MHz}\right) \tag{3.3-26}$$

The unity gain crossover frequency is now at 445 kHz and the phase margin is 82°. The closed loop -3 dB high frequency point is 520kHz. With no load at small signal levels, the loop transmission is

$$T^{NL}(f) = -316\left(\frac{1}{1+jf/4\ kHz}\right)\left(\frac{1}{1+jf/21\ MHz}\right)\left(\frac{1}{1+jf/8.2\ MHz}\right)\left(\frac{1}{1+jf/47\ MHz}\right)\left(\frac{1}{1+jf/61\ MHz}\right) \tag{3.3-27}$$

The crossover frequency is now at 1.25 MHz and the phase margin is 76°, so the system is stable without the load.

The low frequency response is obtained from Eqs. (3.2-9) through (3.2-12) after substituting the component values. The low frequency response described by Eq. (2-10) is

$$A_{CL}^{LF}(f) = A_{CL}^{mid}\left(\frac{1+jf/.003}{1+jf/0.8}\right)\left(\frac{jf/0.8}{1+jf/0.8}\right). \tag{3.3-28}$$

The low frequency closed loop -3 dB point is ~ 1.6 Hz.

3.3.2 Input and Output Impedances

The equations in section 3.2.2 allow the determination of the input and output impedances of the driver amplifier. The input impedance, from Eqs. (3.2-32)and (3.2-33) and the fact that $R_{in1} \approx R_{in2}$, is

$$Z_{in}^{c\ell} = 1\ \text{k}\Omega \parallel 124.4\ \text{k}\Omega \approx 1\ \text{k}\Omega\ , \tag{3.3-29}$$

over a wide frequency range. The open loop output impedance from Eq. (3.2-31) is

$$Z_{out}^{c\ell} = \frac{87\text{k}\left(1 + \text{jf}/8.6\ \text{MHz}\right)}{1 + \text{jf}/3.8\ \text{kHz}}. \tag{3.3-30}$$

Using the no-load loop gain $T^{NL}(f)$, after assuming a single-pole system and Eq. (3.2-35) the closed loop output impedance is

$$Z_{out}^{c\ell} \approx \frac{87\ \text{k}\Omega\left(1 + \text{jf}/8.6\ \text{MHz}\right)}{\left(1 + \text{jf}/3.8\ \text{kHz}\right)\left(1 + \dfrac{316}{\left(1 + \text{jf}/4\ \text{kHz}\right)}\right)}. \tag{3.3-31}$$

which simplifies to

$$Z_{out}^{c\ell} \approx \frac{87\ \text{k}\Omega\left(1 + \text{jf}/8.6\ \text{MHz}\right)\left(1 + \text{jf}/4\ \text{kHz}\right)}{317\left(1 + \text{jf}/3.8\ \text{kHz}\right)\left(1 + \text{jf}/1.3\ \text{MHz}\right)}. \tag{3.3-32}$$

The pole and zero close to 4 kHz are close enough to each other to cancel out giving a $Z_{out}^{c\ell}$ of

$$Z_{out}^{c\ell} \approx 275\ \frac{\left(1 + \text{jf}/8.6\ \text{MHz}\right)}{\left(1 + \text{jf}/1.3\ \text{MHz}\right)}. \tag{3.3-33}$$

3.3.3 Transient Response

The frequency response of the driver amplifier, in a proportional manner, dictates the pulse response of the amplifier, but as mentioned earlier, fast transition signals are affected by slewing and are best studied using the pulse response. High frequency sinusoids also have fast transitions and the slew rate necessary to get a non-slewing signal for maximum frequency and maximum voltage out, using Eq. (3.2-37) is

$$\text{S.R} > 2\pi\left(150\ \text{kHz}\right)\left(150\ \text{V}\right) = 140\ \text{V}/\mu\text{s}\ , \tag{3.3-34}$$

where f_{max} is 150 kHz and V_{max} is approximately 150 V. The slew rate of the driver amplifier being considered here, from Eq. (3.2-42) is

$$S.R = \frac{\left(9\right)\left(7.86\right)}{100\left(600\ pF\right)} = 1180\ V/\mu s\ , \tag{3.3-35}$$

where k is 7.86, $\Delta V_{B5}{}^{max}$ is 9 V and C_{TOTAL} is the load capacitance plus the average of the C_{ob}'s of transistors Q_{10} and Q_{11} which comes to approximately 600 pf. The slew rate of the driver amplifier is more than sufficient to reproduce an undistorted sinusoid at 150 V and 150 kHz

3.3.4 Power Dissipation Calculations

The design equations of section 3.2.4 will be used to determine the power dissipated in the high voltage section at both quiescent and dynamic conditions. The quiescent current in the output stage can easily be adjusted with the potentiometer, R_{B6A} of the V_{BE} multiplier. Setting the current of the output transistors, Q_{10} and Q_{11} to approximately 4.5 mA will give the following results. The output quiescent dissipation from Eq. (3.2-44) is

$$P_{Q10} = P_{Q11} \approx 4.5\ mA\left(150\ V\right) = 0.86\ W\,. \tag{3.3-36}$$

The quiescent power dissipation in transistors Q_8 and Q_9 is

$$P_{Q8} = P_{Q9} = \left\{150 - \left[(4.5\ mA)(69.8) + 0.65\right]\left[1 + \frac{100}{549}\right]\right\}\cdot \tag{3.3-37}$$

$$\left\{\frac{(4.5\ mA)(69.8) + 0.65}{549}\right\} = 0.26\ W$$

From Eq. (3.2-48) the maximum output current for $V_m \approx 150$ V and $f_m \approx$ 150 kHz is

$$I_m = 2\pi\left(150\right)\left(150\,\text{kHz}\right)\left(600\text{pF}\right) = 85\ \text{mA}. \tag{3.3-38}$$

The instantaneous power dissipation using Eq. (3.2-51) becomes

$$P_{io} = 12.8\cos\omega_m t - 0.51\cos^2\omega_m t - 6.4\sin^2\omega_m t\ . \tag{3.3-39}$$

The maximum output voltage swing, V_m was approximated to be 149 V. From Eq. (3.2-54) the current that gives the maximum power dissipated is

$$I_m = \frac{2}{70}\left(\frac{150}{\pi} + \frac{149}{4\pi}\right) = 1.7\,\text{A}\ . \tag{3.3-40}$$

The maximum current used in this case from Eq. (3.3-38) is only 85 mA and conditions of maximum power dissipation are never reached. The average power dissipated at 85 mA will therefore be used as an upper limit which from Eqs. (3.2-52) and (3.3-38) is

$$\overline{P}_{io} \approx 5\ \text{W}. \tag{3.3-41}$$

The same will hold true for transistors Q_8 and Q_9 and the upper limit for transistor Q_8 from Eq. (3.2-60) is

$$\overline{P}_{i8} = 1\ \text{W}\ . \tag{3.3-42}$$

The output transistors must therefore have a power dissipation greater than 5 W. Transistors Q_8 and Q_9 must have a dissipation that is larger than 1 W. Heat-sinking is very important in all the transistors because as the power dissipation increases, the base-emitter voltage of the devices drops by about 2mV/°C. This leads to an increase in current and a consequent increase in temperature that causes thermal instability and damage to the devices. With sufficient heat-sinking, this problem is avoided and to make accurate calculations in order to determine these effects, the equations presented in Appendix B can be used.

CHAPTER 4

EXPERIMENTAL AND SPICE ANALYSIS RESULTS

This chapter presents the experimental results, the computer simulation (SPICE) results and a comparison of these results with the hand analysis results of Chap. 3. The computer simulation (SPICE) results are used to confirm and supplement the hand analysis results in the determination of loop transmission, oscillation stability, closed-loop gain, input and output impedances, and transient performance. SPICE analysis can be useful after the circuit modelling is determined to be accurate. Design changes can be implemented much more easily on SPICE than on an actual circuit and the subsequent change in performance can be observed from the simulation results.

4.1 Frequency Response and Oscillation Stability

The hand analysis results predict that when Eq. (3.3-19) is solved for the circuit shown in Fig. 3.5, p. 18 the unity gain crossover frequency for the loop transmission, T(f), is 590 kHz and the phase margin is 77°. These results are for a load capacitance of 500 pF. SPICE results, shown in Fig. 4.1, indicate that the crossover frequency is 620 kHz and the phase margin is 80°. The closed-loop high frequency -3 dB point, from the hand analysis, is 795 kHz. The SPICE results shown in Fig. 4.2, indicate a closed-loop high frequency -3 dB point at 820 kHz. When the load is removed, solving Eq. (3.3-27) gives a loop transmission unity gain crossover frequency at 1.25

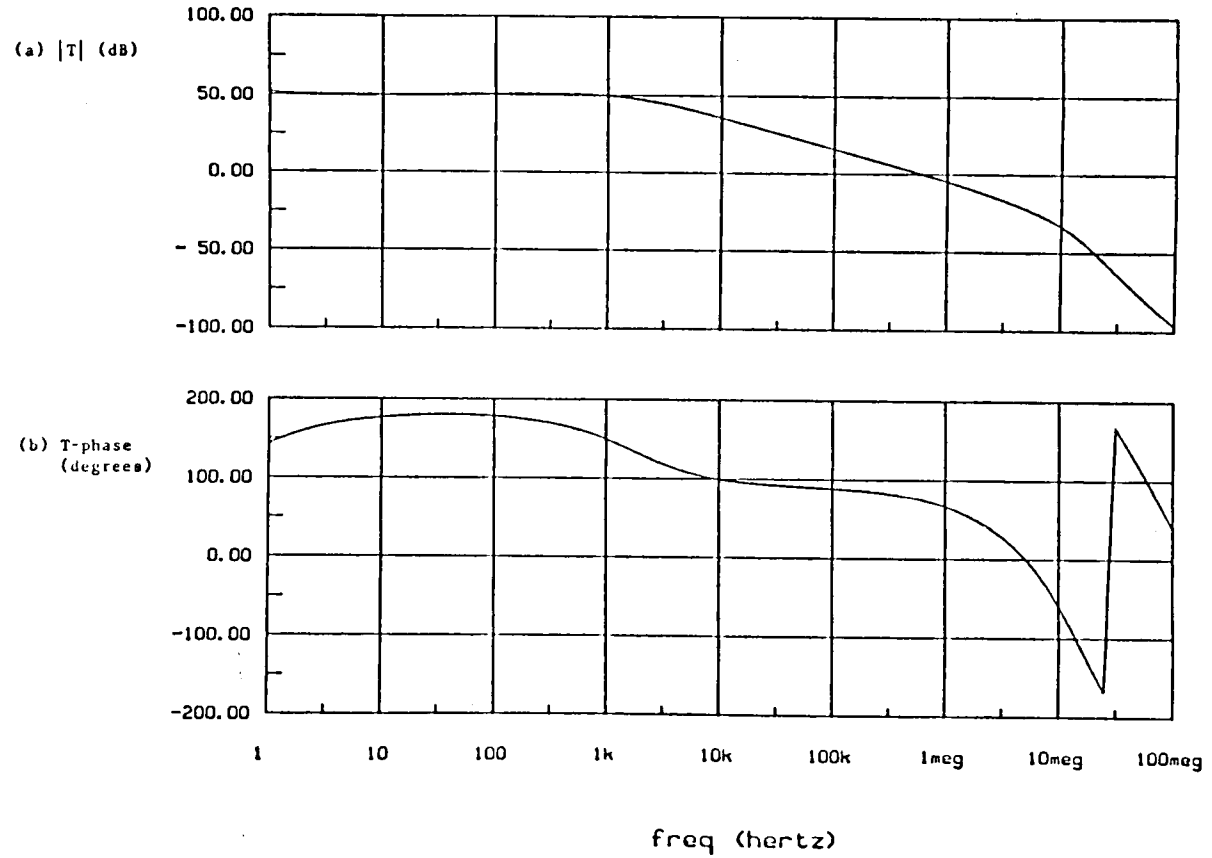

Figure 4.1. The magnitude (a) and the phase (b) of the small-signal loop transmission with a load capacitance, C_L, of 500 pF. (from SPICE)

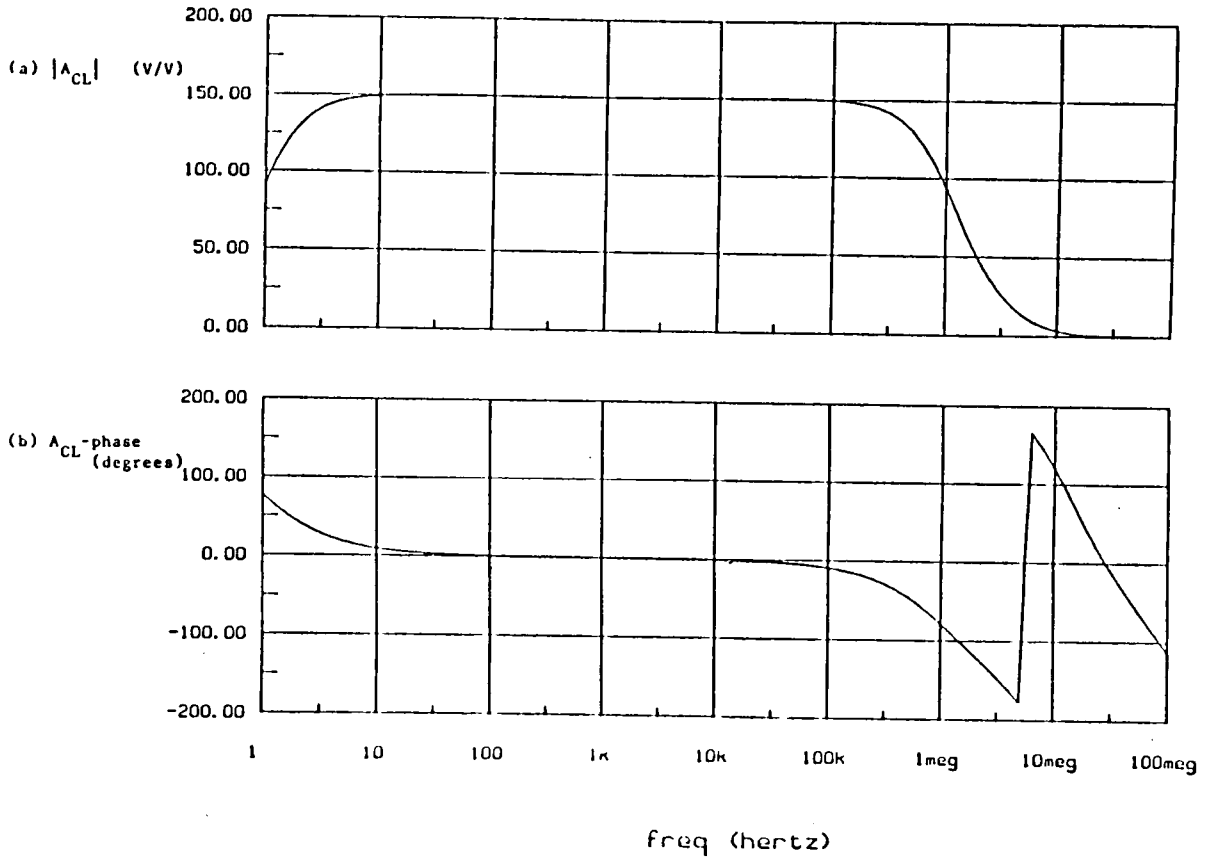

Figure 4.2. The magnitude, (a), and the phase, (b), of the small-signal closed-loop gain, A_{CL}, when the load capacitance, C_L, is 500 pF. (from SPICE)

MHz and a phase margin of 76°. The closed-loop high frequency -3 dB point is therefore 1.7 MHz. SPICE results for a no-load condition indicate, from Figs. 4.3 and 4.4., that the loop transmission unity gain frequency is 1.5 MHz, the phase margin is 79.4° and the high frequency -3 dB point is 2 MHz. The calculated midband loop transmission, T_0 is -316 and SPICE gives a T_0 of ~ -316 (50 dB). In Fig. 4.5, the closed loop high frequency -3 dB point as a function of output voltage is shown. The high frequency -3 dB point was measured by observing the frequency at which the sinusoidal output voltage dropped to 0.707 of its peak value. The closed-loop low frequency -3dB point from Eq. (3.3-28) is ~1.5 Hz whereas the SPICE result indicates a -3 dB point at ~1.3 Hz.

4.2 Input and Output Impedances

The midband input and outut impedances were measured, but since enough confidence in the SPICE results has been established because of the close correlation in the previous section between SPICE and the hand analysis, it will be sufficient to use the SPICE results as confirmation for high frequencies. The hand analysis results for the input impedance show that $Z_{in}{}^{c\ell}$ is ~1 kΩ over a wide frequency range, see Eq. (3.3-29). SPICE results for the input impedance are shown in Fig. 4.6 where the impedance is ~1 kΩ to over 10 MHz. The output impedance from Eq. (3.3-33) has a critical frequency at 1.3MHz and the rolloff rate is 20 dB/decade. The SPICE results shown in Fig. 4.7, however, indicate that the response is quite different from that predicted by the hand analysis for frequencies above 1 MHz. The simple two-transistor hybrid-π model used for the hand

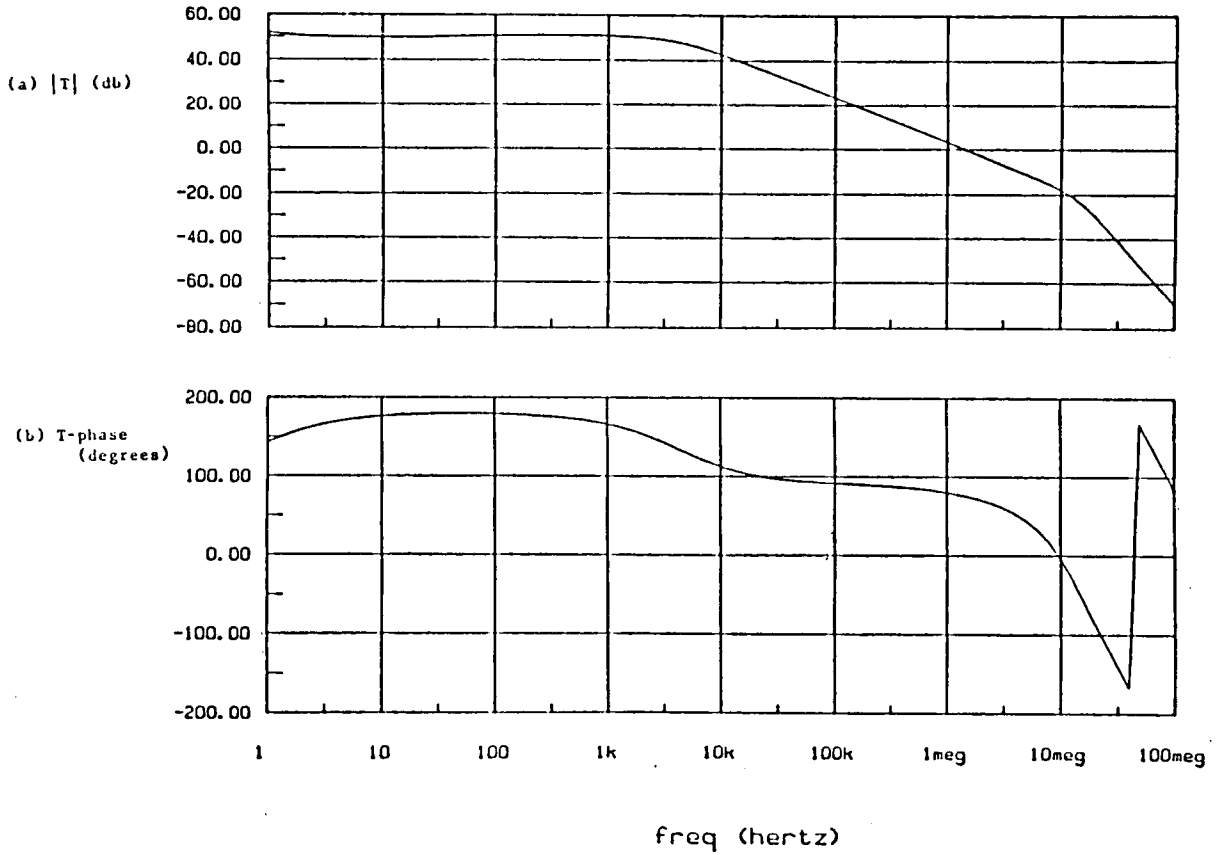

Figure 4.3. The magnitude, (a), and the phase, (b), of the small-signal loop transmission, T, when the load is $C_L = 0$ pF. (from SPICE)

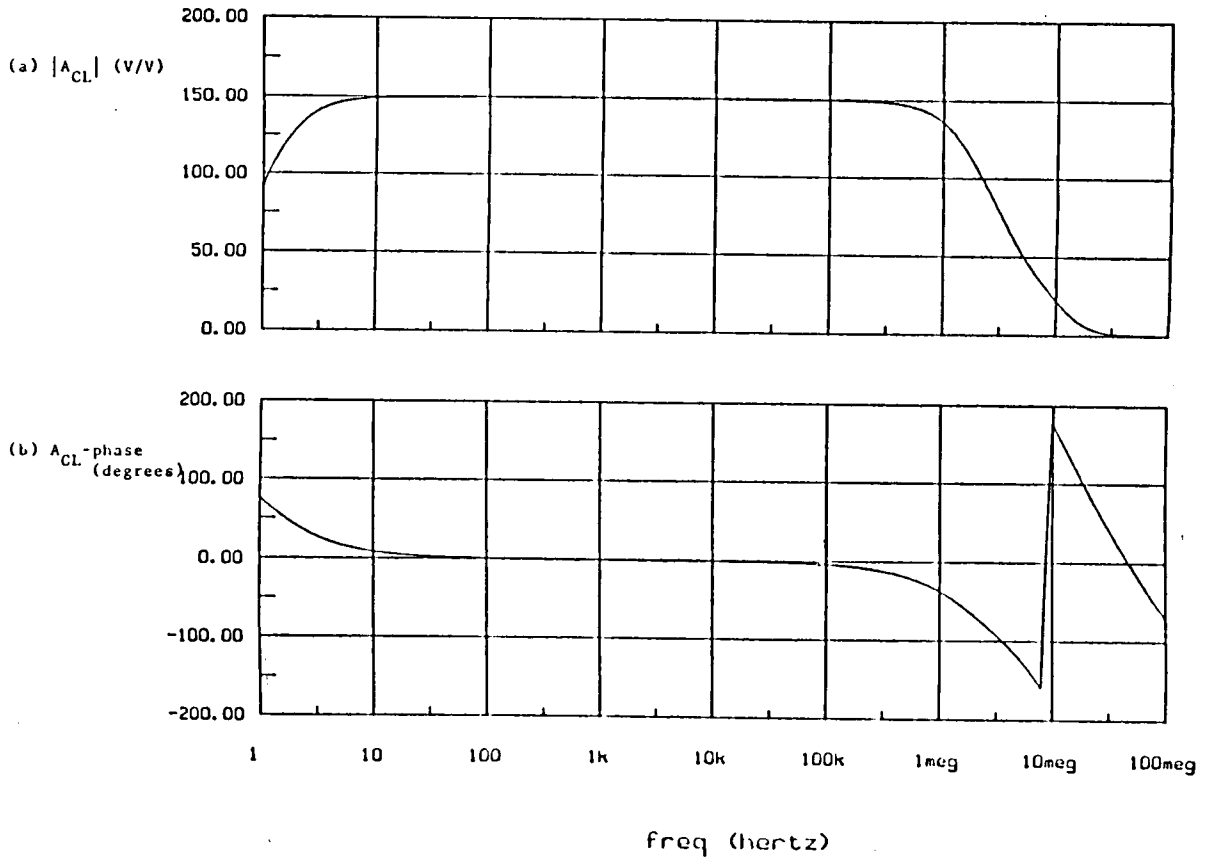

Figure 4.4. The magnitude, (a), and the phase, (b), of the small-signal closed-loop gain, A_{CL}, when the load is $C_L = 0$ pF. (from SPICE)

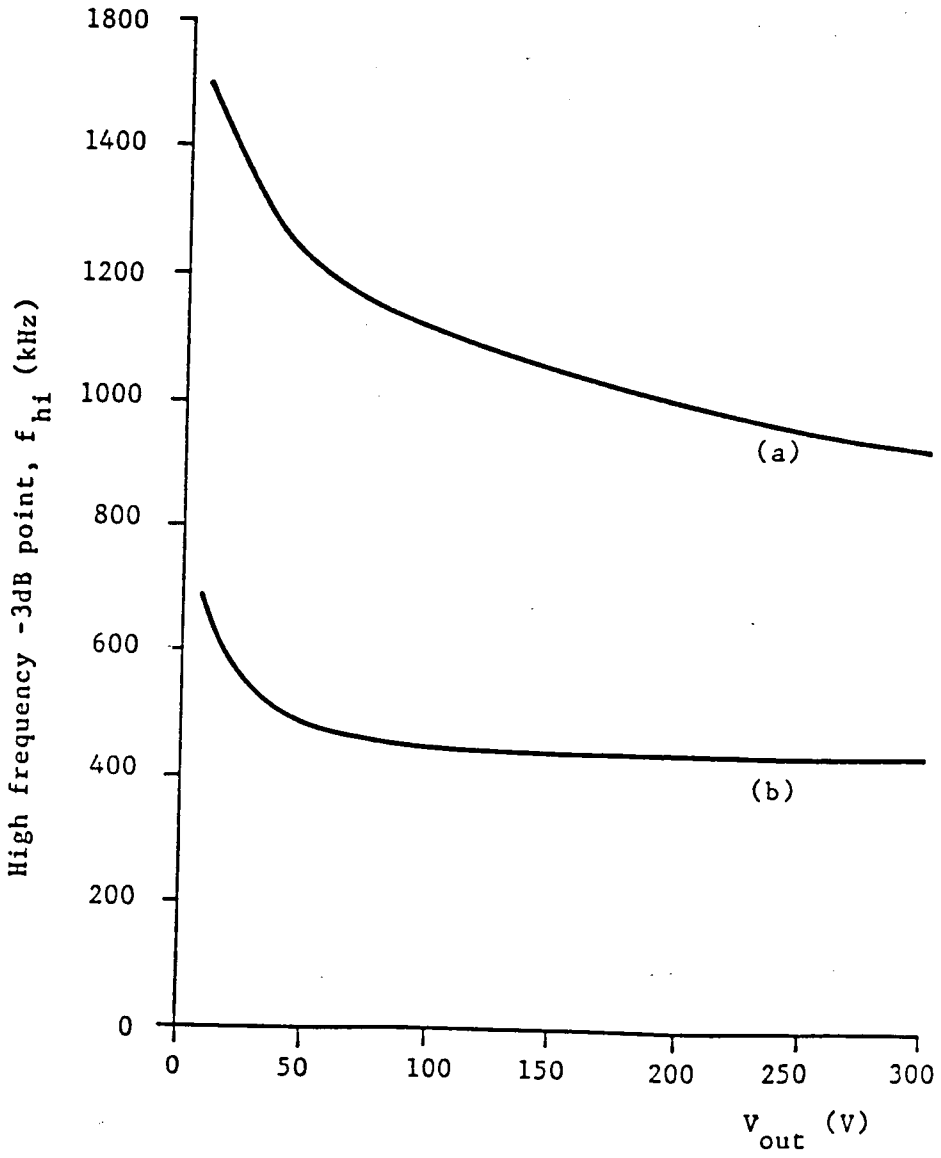

Figure 4.5. The measured high frequency -3dB point vs. output voltage for the driver amplifier: (a) with $C_L = 0$, and (b) with $C_L = 500$ pF.

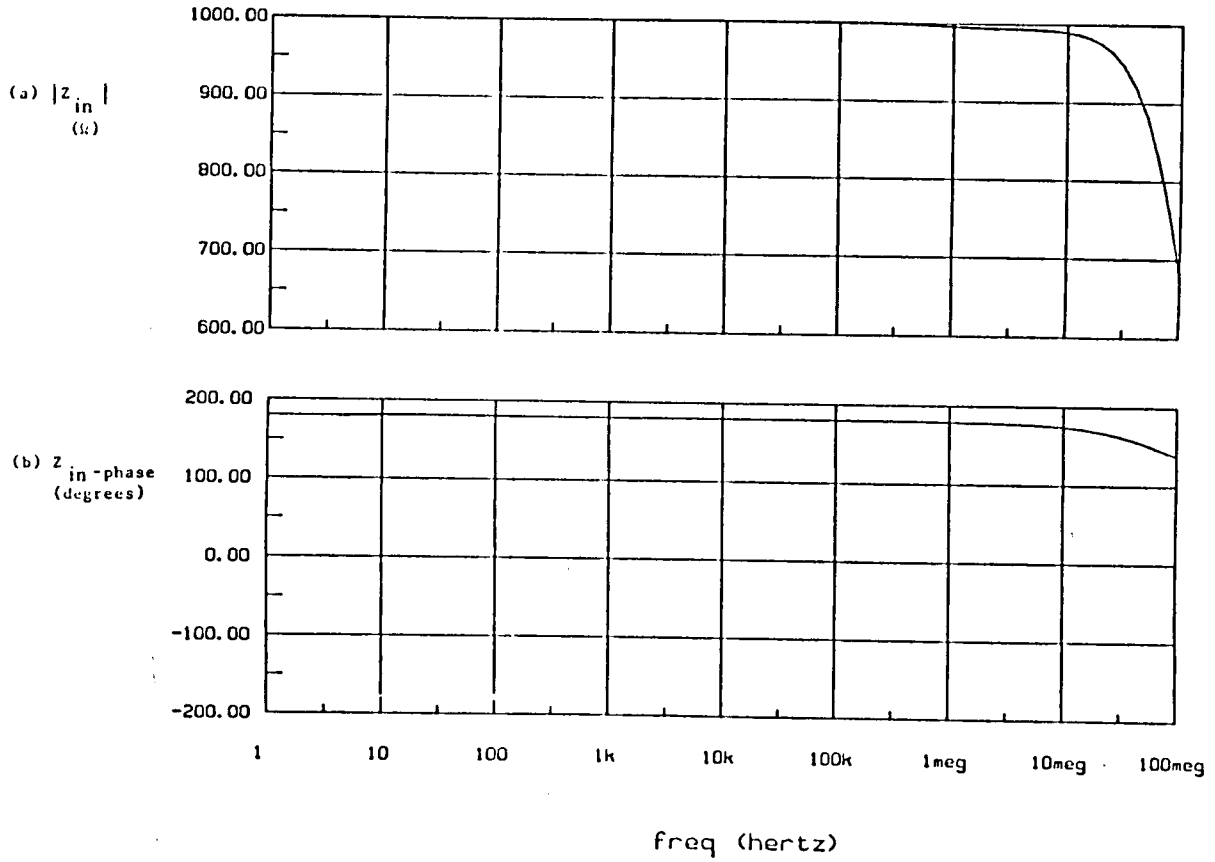

Figure 4.6. The magnitude, (a), and the phase (b), of the input impedance. (from SPICE)

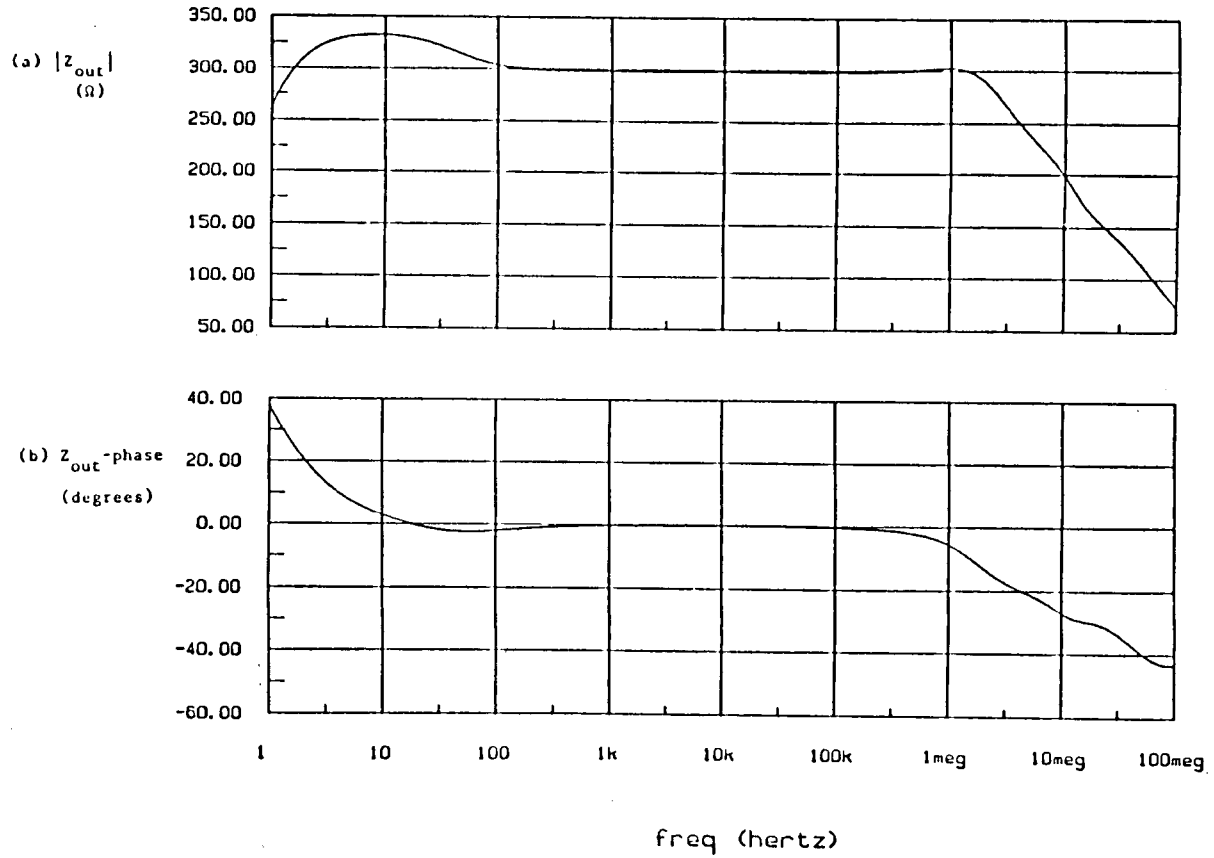

Figure 4.7. The magnitude, (a), and the phase, (b), of the output impedance; obtained with the load disconnected. (from SPICE)

analysis is therefore not rigorous enough and does not predict the unusual ~4 dB/decade rolloff that starts at ~1 MHz as predicted by the SPICE results. The 4 dB/decade rolloff is probably due to a complex series of poles and zeroes and is a result of the complex interaction between loop transmission and open-loop output impedance. The circuit model and the derivation of $Z_{out}^{o\ell}$ are presented in Appendix D. The SPICE model takes into consideration these complex effects that cannot reasonably be included in the hand analysis. The midband output impedance from the SPICE analysis is ~300 Ω, from the hand analysis is approximately 275 Ω and measured is approximately 350 Ω.

4.3 Transient Response

The transient response of the driver amplifier is determined by observing the response of the driver amplifier to a step input. The output has a risetime that is related to the frequency response and drive conditions. These risetimes can be predicted by converting from the frequency domain to the time domain but this could be time consuming. If slewing occurs, the output risetime will be due to a combination of the frequency response and slewing and to a first order approximation the two responses can be combined as the square root of the sum of the squares.

From the hand calculations, the slew rate is ~1180 V/μs. A 300 V pulse at the output takes 0.25 μs to reach its final value due to slewing only. The risetime is approximately 0.7 μs (obtained from f_{hi} using a first-order approximation) and the slewing response will not be distinguishable from the time constant response and therefore, the combined risetime, to a first-

order approximation, is ~0.76 μs. For a sinusoid of 300 V pk-pk and a frequency of 150 kHz, no slewing should be observable because the slew rate necessary for the sinusoid is much lower than the slew rate of the driver amplifier.

The SPICE results for the response of the amplifier at the positive transition of a 300 V output pulse, and the current turn-on signal at the emitter of transistor Q_{10} are shown in Fig. 4.8. The same information for the negative transition is shown in Fig. 4.9. The signals in Figs. 4.8(a) and 4.9(a) are the current turn-on signals. The measured signals under the same conditions as those of Figs. 4.8 and 4.9 are shown in the oscilloscope photographs, Figs. 4.10 and 4.11. The positive and negative excursions of the emitter voltages for transistors Q_{10} and Q_{11}, from SPICE analysis are approximately ± 27.5 V, whereas the measured excursions from Figs. 4.10 and 4.11 are ~±26 V and these convert to currents of ±393 mA for the SPICE results and ±370 mA for the measured results. The SPICE results give rise times and fall times which are a little below 1 μs and the measured rise times and fall times are ~0.9 μs.

The SPICE analysis results for the response to a 300 V pk-pk sinusoid at 150 kHz at the output is shown in Fig. 4.12. Fig. 4.12(a) shows the positive current turn-on signal at the emitter of transistor Q_{10}, and Fig. 4.12(c) is that at the emitter of Q_{11} and the output signal is shown in Fig. 4.12(b). The current turn-on signals are not significantly distorted in the half-cycles when the signals are on and hence slewing is not occuring. The measured sinusoidal signals under the same conditions as those for Fig.

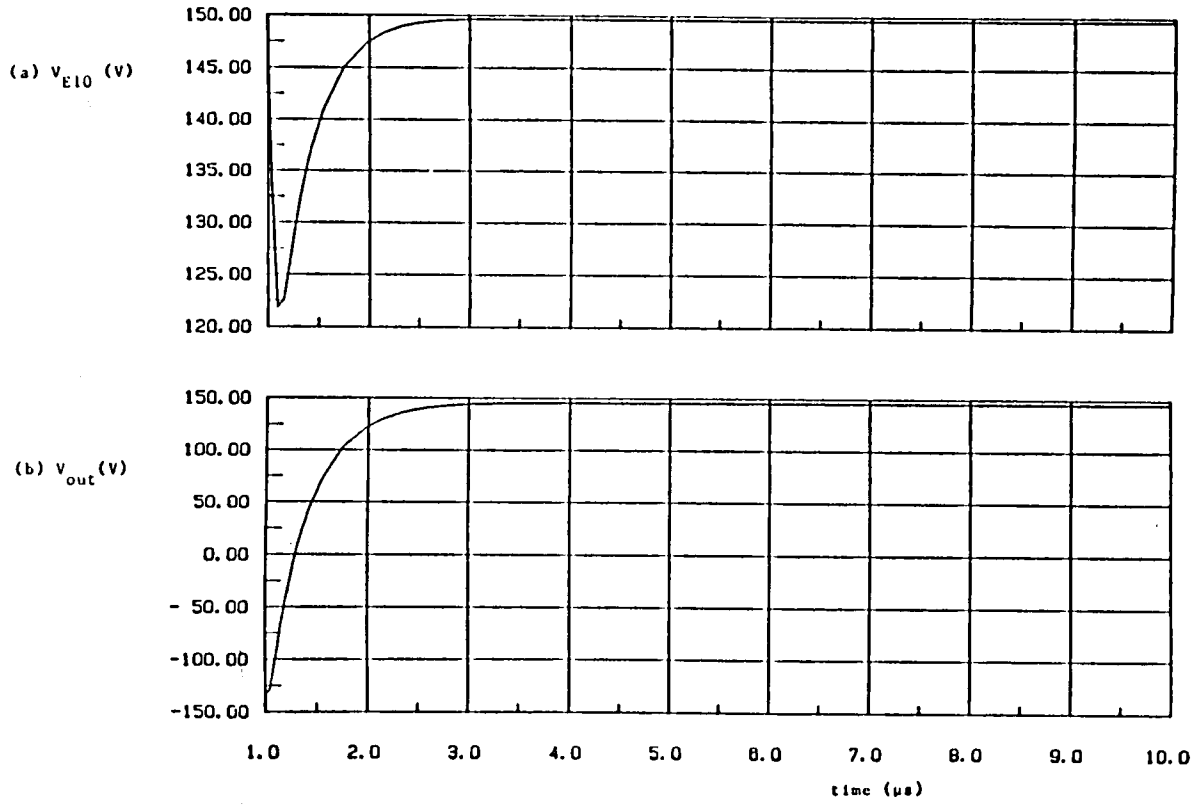

Figure 4.8. Transient response of the amplifier when the load is 500 pF: (a) The current turn-on signal at the emitter of transistor Q_{10} when the output is 300 V and at the positive transition, (b). (from SPICE)

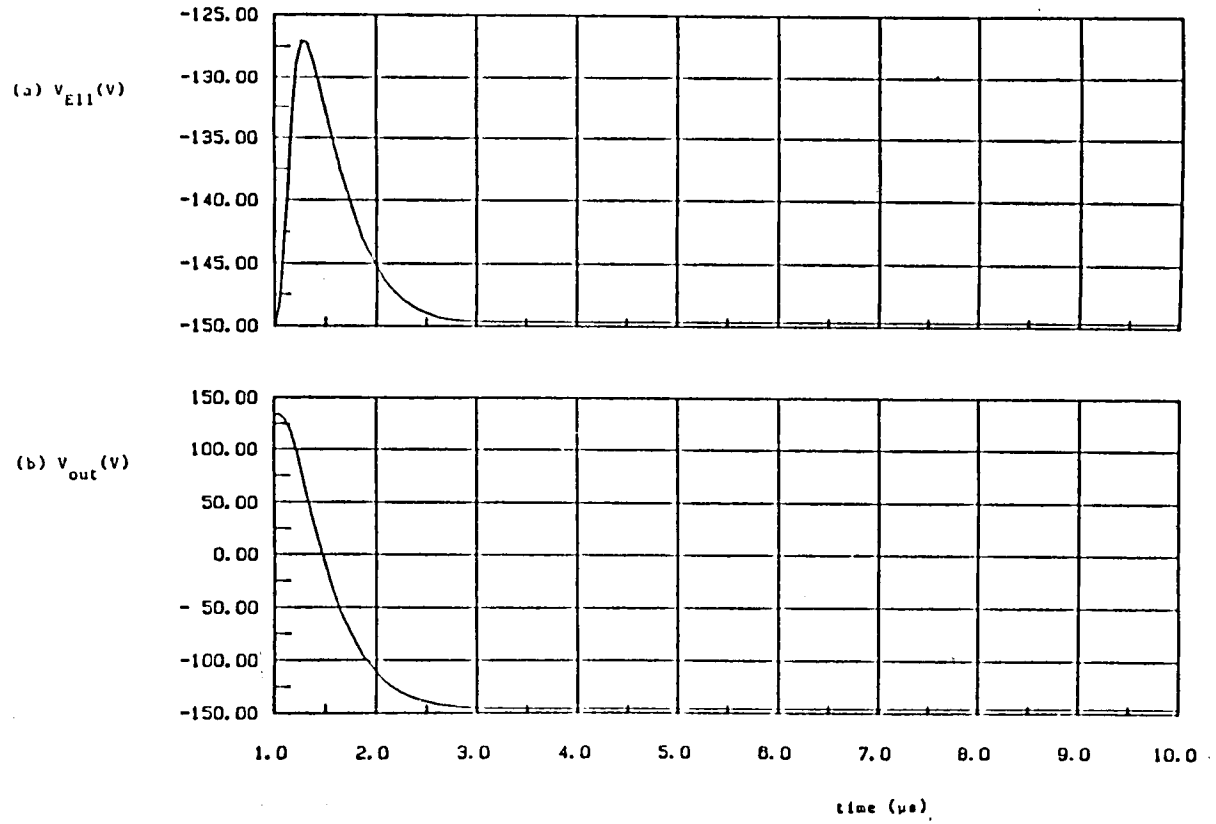

Figure 4.9. Transient response of the amplifier when the load is 500 pF: (a) The current turn-on signal at the emitter of transistor Q_{11} when the output is 300 V and at the negative transition, (b). (from SPICE)

(a)

(b)

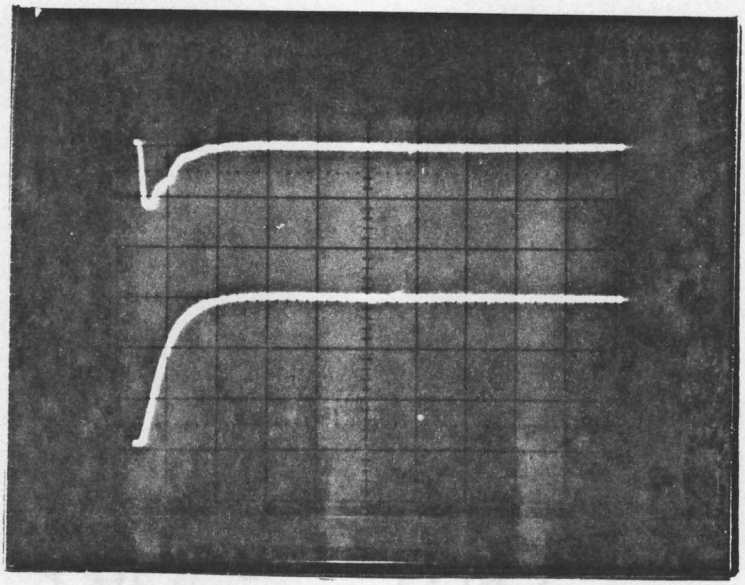

Figure 4.10. Experimental results for amplifier with load, C_L = 500 pF and time scale is 1μs/div: (a) Voltage at the emitter of transistor Q_{10}, V_{E10} at 20 V/div., and (b) Voltage at the output node with scale = 100 V/div.

(a)

(b)

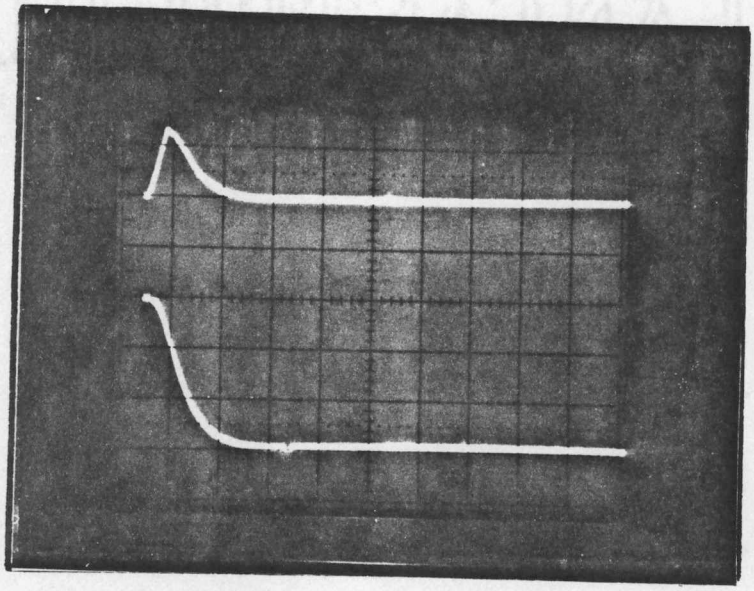

Figure 4.11. Experimental results for amplifier with load C_L = 500 pF and time scale = 1 μs/div: (a) Voltage at the emitter of transistor Q_{11}, V_{E11} at 20 V/div., and (b) voltage at the output node with scale = 100 V/div.

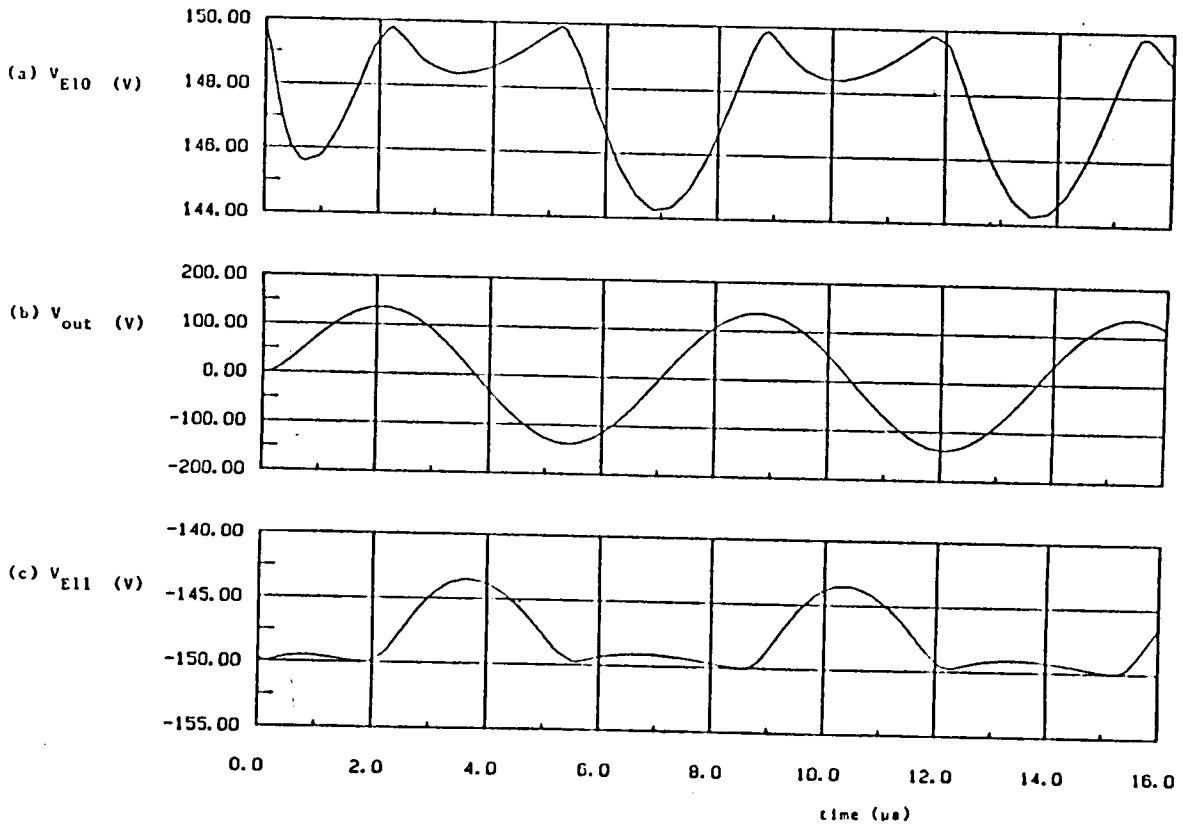

Figure 4.12. The response of the amplifier to a sinusoidal signal when the load is 500 pF: (a) The current turn-on signal at the emitter of transistor Q_{10}, (b) The output signal and (c) The current turn-on signal at the emitter of Q_{11}. (from SPICE)

4.12 are shown in Fig. 4.13 and give currents of +100 mA and -130 mA, whereas SPICE results indicate peak currents of +86 mA and -107 mA.

The signals observed within the amplifier, according to the SPICE analysis, are shown in Fig. 4.14. The output voltage is a pulse of ~300 V pk-pk and the measured equivalent of Fig. 4.14 is shown in Fig. 4.15. Figs. 4.14(a) and 4.15(a) show the error voltage i.e., the voltage between the bases of transistors Q_1 and Q_2. The error signal is a positive pulse for the positive transition of the output voltage and a negative pulse for the negative transition of the output voltage. The error voltage pulses are $\sim \pm 2$ V in amplitude and the approximate time constant decay indicates that the output voltage is dominated by the time constant response and not the slewing response. The measured amplitudes from Fig. 4.15(a) are also $\sim \pm 2$ V. Figs. 4.14(b) and 4.15(b) are the signals at the emitter of transistor Q_5, which is approximately equal to the error voltage times the large signal voltage gain of the low voltage section. The SPICE analysis shows signals of $\sim \pm 10$ V whereas the measured amplitudes are $\sim \pm 6$ V. Parts (c) and (d) are the SPICE analysis results in Fig. 4.14 and the measured signals in Fig. 4.15 for the collectors of transistors Q_8 and Q_9 respectively. These voltages are approximately equivalent to the voltage at the emitter of transistor Q_5 times the large- signal voltage gains of transistors Q_8 and Q_9. The SPICE analysis indicates voltage excursions of approximately ± 34 V whereas the measured excursions are ± 28 V.

The SPICE transient response at small signal levels is shown in Fig. 4.16, and the actual response at the same signal levels is shown in Fig. 4.17.

(a)

(b)

(c)

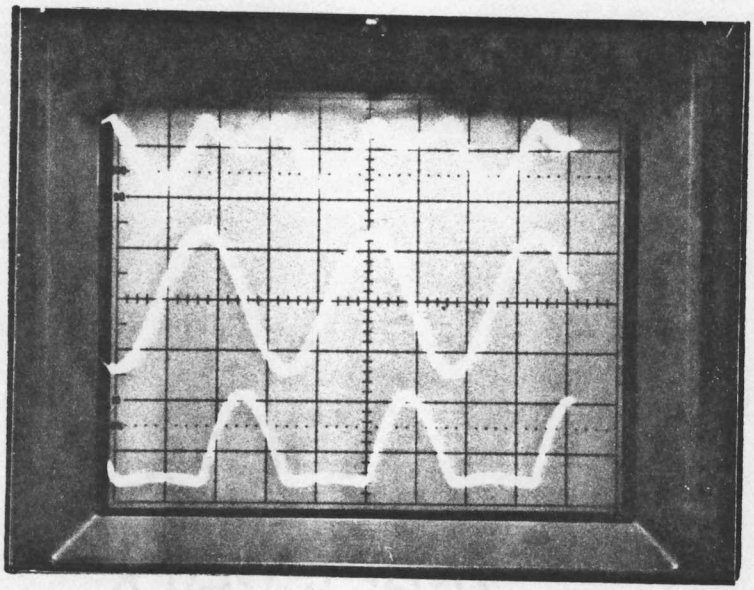

Figure 4.13. Experimental results of amplifier for a sinusoidal signal and load C_L = 500 pF. Time scale is 2 μs/div: (a) Voltage at the emitter of transistor Q_{10}, V_{E10}, at 5 V/div., (b) voltage at the output node at 100 V/div., and (c) voltage at the emitter of transistor Q_{11}, V_{E11}, at 5 V/div.

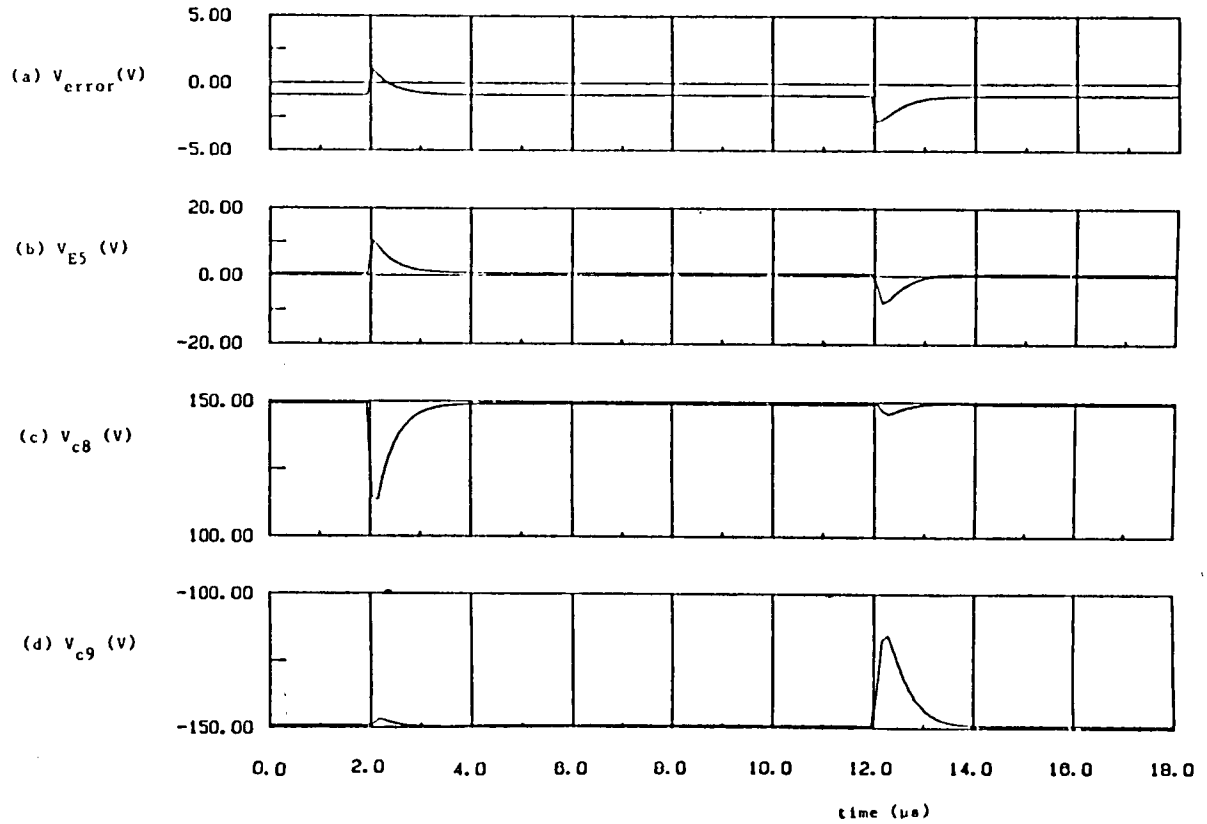

Figure 4.14. The transient response within the amplifier when the load is 500 pF and the output voltage is a 300 V pulse that starts at time t = 2μs and ends at time t = 12μs: (a) the error voltage, V_{error}, (b) the voltage at the emitter of transistor Q_5. (c) The voltage at the collector of Q_8 and (d) the voltage at the collector of Q_9. (from SPICE)

(a)

(b)

(c)

(d)

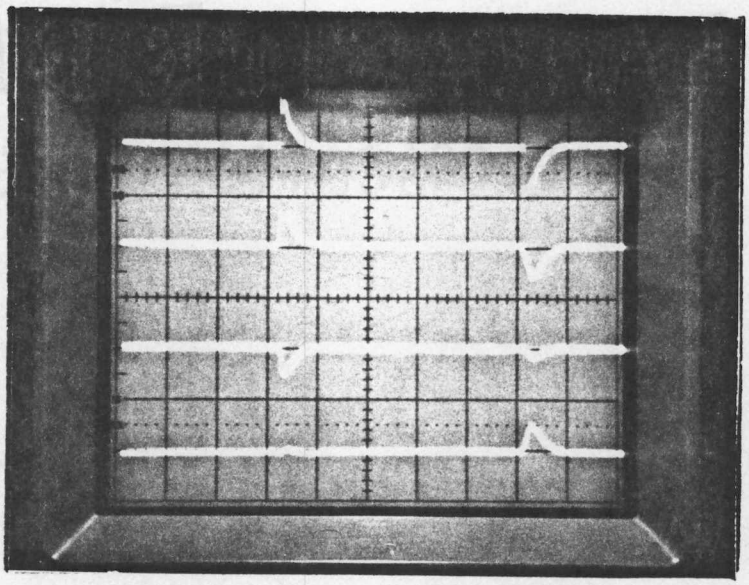

Figure 4.15 Experimental results of amplifier with load C_L = 500 pF, an outut voltage of 283 V pk-pk and time scale shown is 2 μs/div., (b) voltage at the emitter of transistor Q_5, V_{E5} with a scale of 10 V/div., (c) Voltage at the collector of transistor Q_8, V_{c8} at 50 V/div., and (d) voltage at the collector of transistor Q_9, V_{c9} at a scale of 50 V/div.

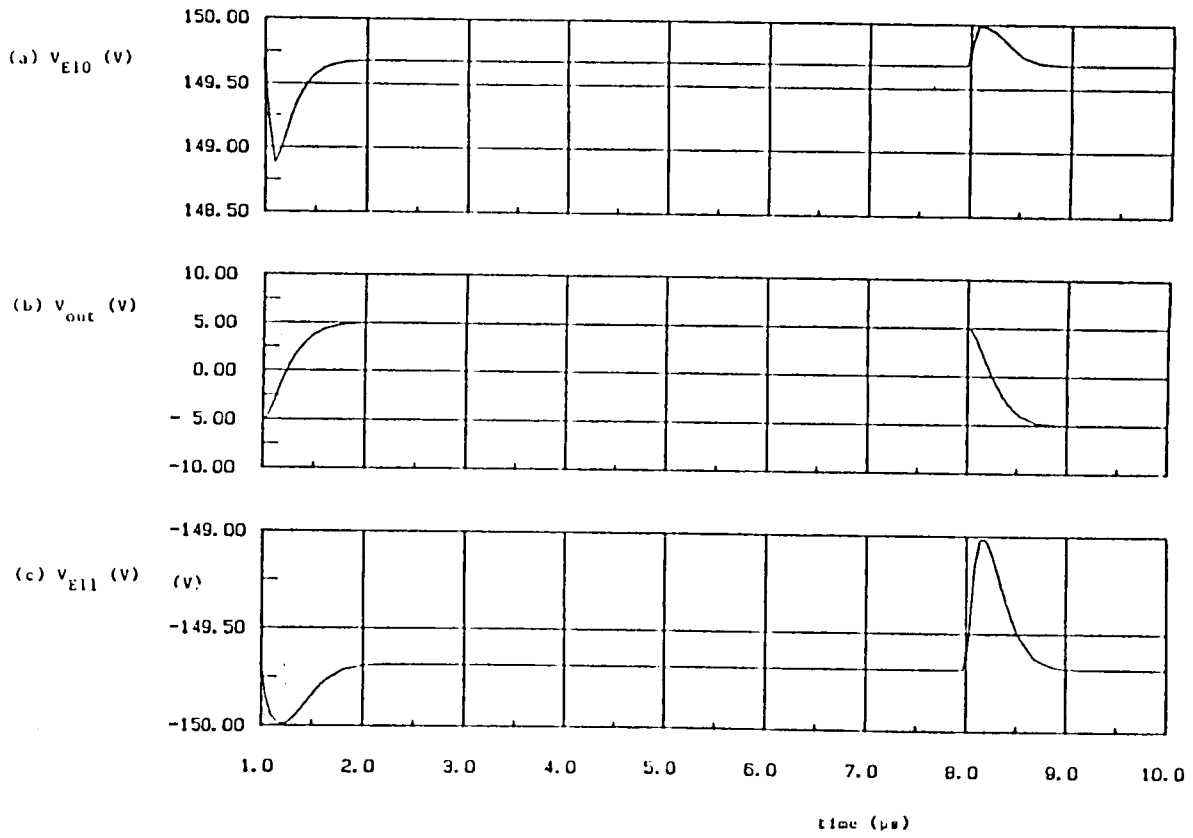

Figure 4.16. The transient response of the amplifier when the load is 500 pF: (a) The current turn-on signal at the emitter of transistor Q_{10}, (b) The output voltage and (c) The current turn-on signal at the emitter of transistor Q_{11}. (from SPICE)

(a)

(b)

(c)

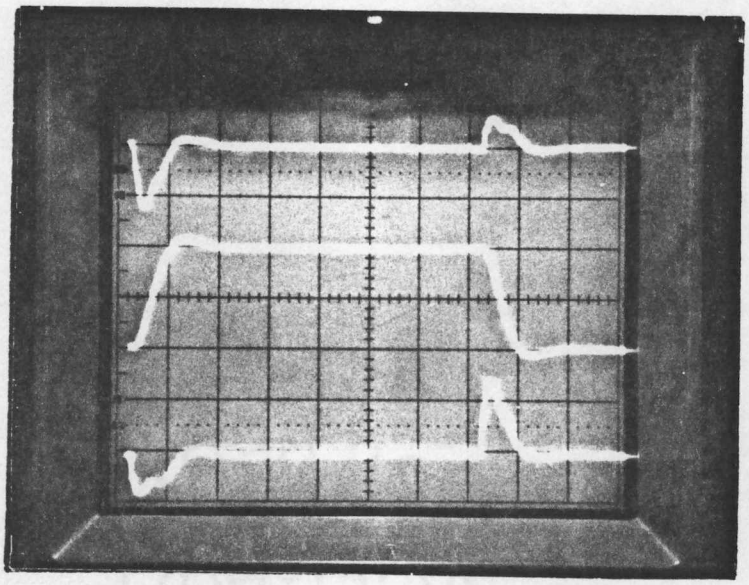

Figure 4.17. Experimental results of amplifier with load C_L = 500 pF and a time scale of 1 μs/div.: (a) Voltage at the emitter of transistor Q_{10}, V_{E10} at 0.5 V/div., (b) Voltage at the output node at 5 V/div., and (c) Voltage at the emitter of transistor Q_{11}, V_{E11} at 0.5 V/div.

Parts (a) and (c) show the current turn-on signals at the emitters of transistors Q_{10} and Q_{11}, respectively. Part (b) shows the output voltage and is 10 V pk-pk for both Figs. 4.16 and 4.17. The negative excursion of the voltage at the emitter of transistor Q_{10}, from SPICE, is ~0.83 V and the positive excursion at the emitter of transistor Q_{11}, from the SPICE analysis is ~0.75 V. From Fig. 4.17 the actual voltage excursions are approximately 0.7 V and 0.73 V, respectively. The slight overshoot present in the output voltage shown in Fig. 4.17 is there because the parasitic capacitances on the prototype at the other important nodes such as the bases of transistors Q_5 and Q_2, increase the respective time constants thereby degrading the phase margin. The overshoot is absent from the output voltage shown in Fig. 4.16 because these parasitic capacitances were not added to the SPICE circuit model.

The positive and negative transitions of the output voltage at small signal levels with no load are shown in Figs. 4.18 and 4.19 and are from the SPICE results and actual measured voltages, respectively. In Figs. 4.20 and 4.21, the no-load positive and negative output voltage transitions at high signal levels are shown, respectively. Fig. 4.20 consists of the SPICE results and Fig. 4.21 consists of the actual measured voltages. The measured risetime as a function of output voltage for the driver amplifier with and without a load is shown in Fig. 4.22.

4.4 Conclusion

In Table 4.1, a comparison between the hand analysis results, SPICE analysis results, and experimental results for a few of the performance

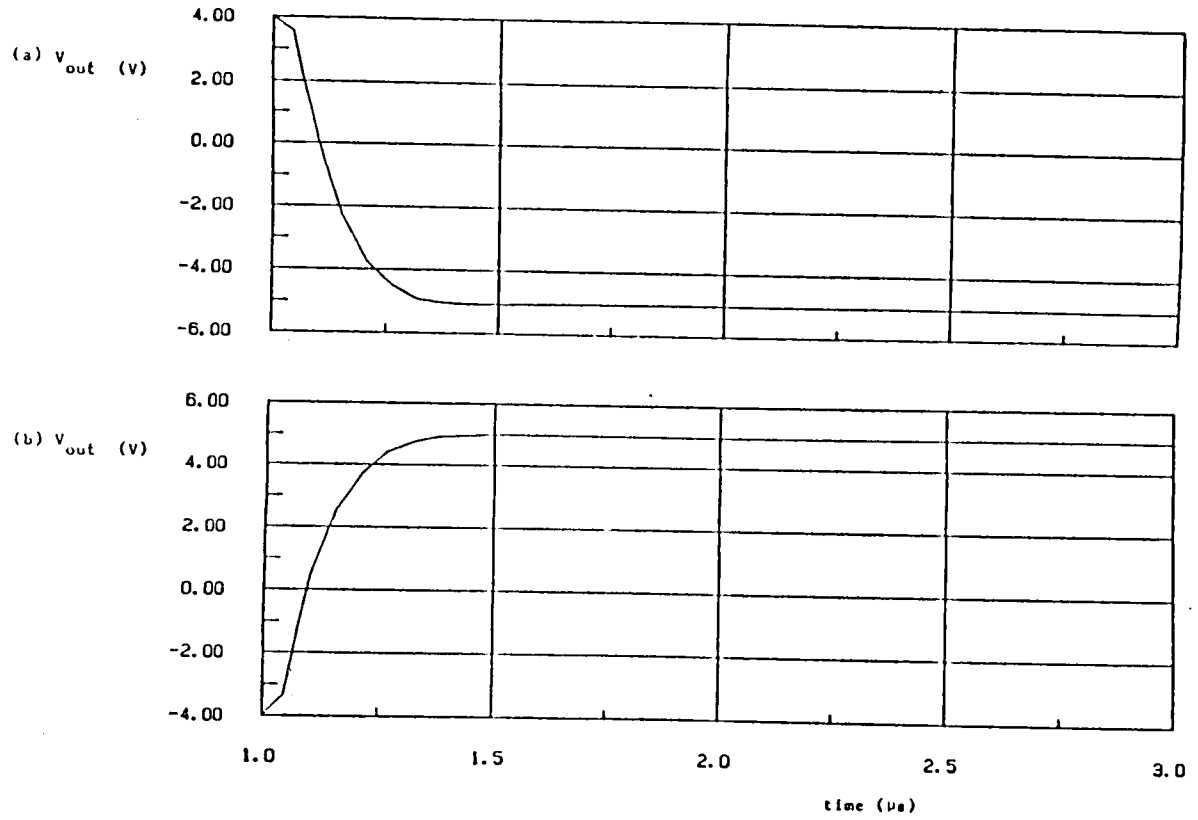

Figure 4.18. The small-signal transient response of the amplifier with the load disconnected: (a) The negative transition and (b) The positive transition of the output voltage. (from SPICE)

(a)

(b)

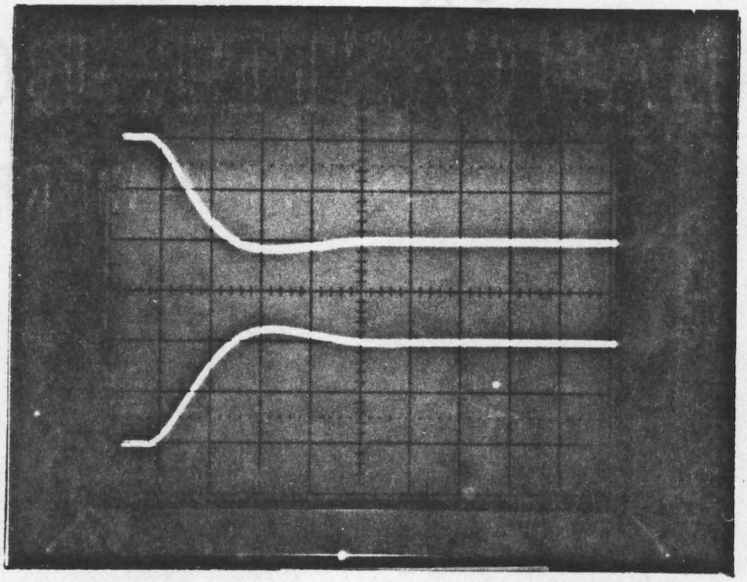

Figure 4.19. Experimental results of amplifier with load C_L = 0 pF; time scale is 0.2 μs/div.: (a) Voltage at the output node during the negative transition; scale is 5 V/div., and (b) Voltage at the output node during the positive transition; scale is 5 V/div.

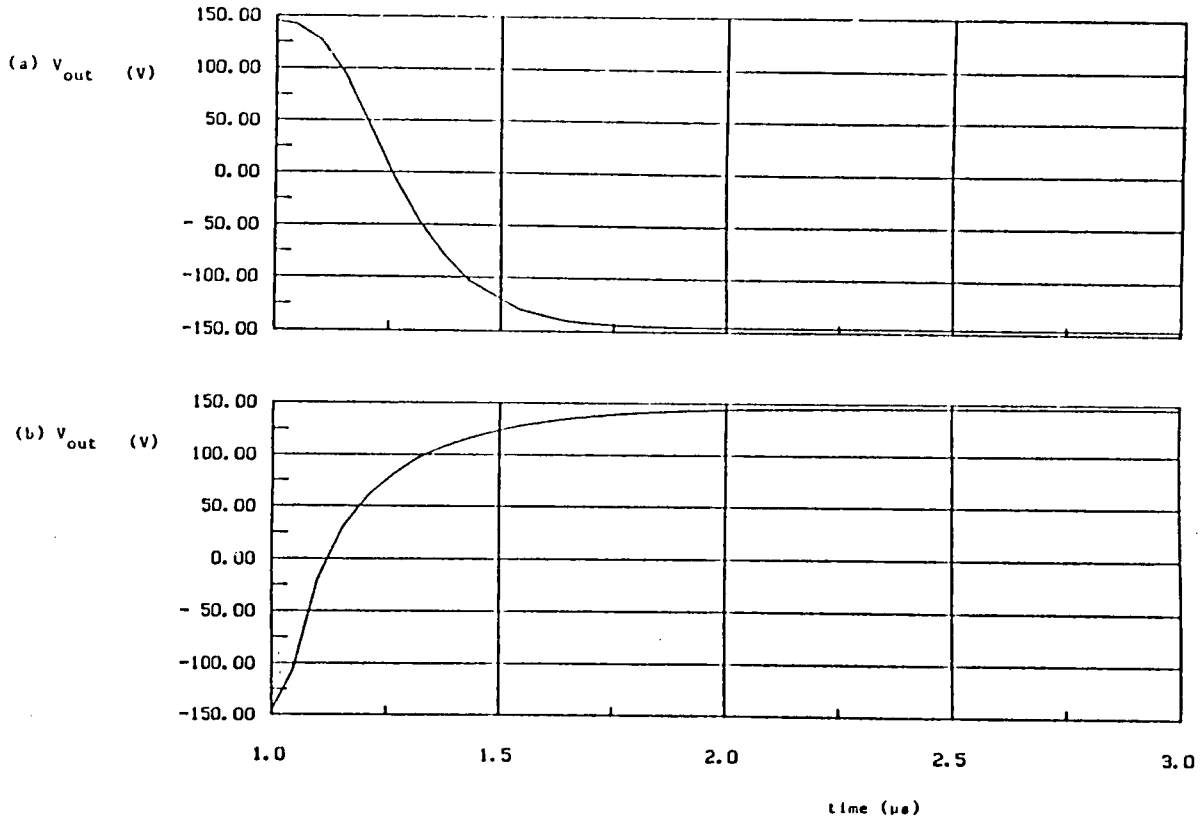

Figure 4.20. The large signal transient response of the amplifier with the load disconnected: (a) The negative transition and (b) The positive transition of the output voltage (from SPICE)

(a)

(b)

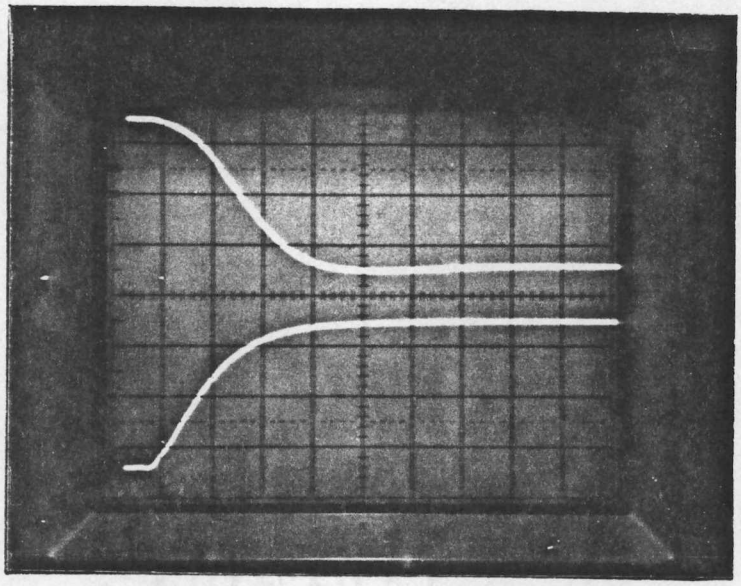

Figure 4.21. Experimental results of amplifier with load $C_L = 0$ pF; time scale is 0.2 μs/div., (a) Voltage at the output node during the negative transition; scale is 100 V/div., and (b) Voltage at the output node during the positive transition; scale is 100 V/div.

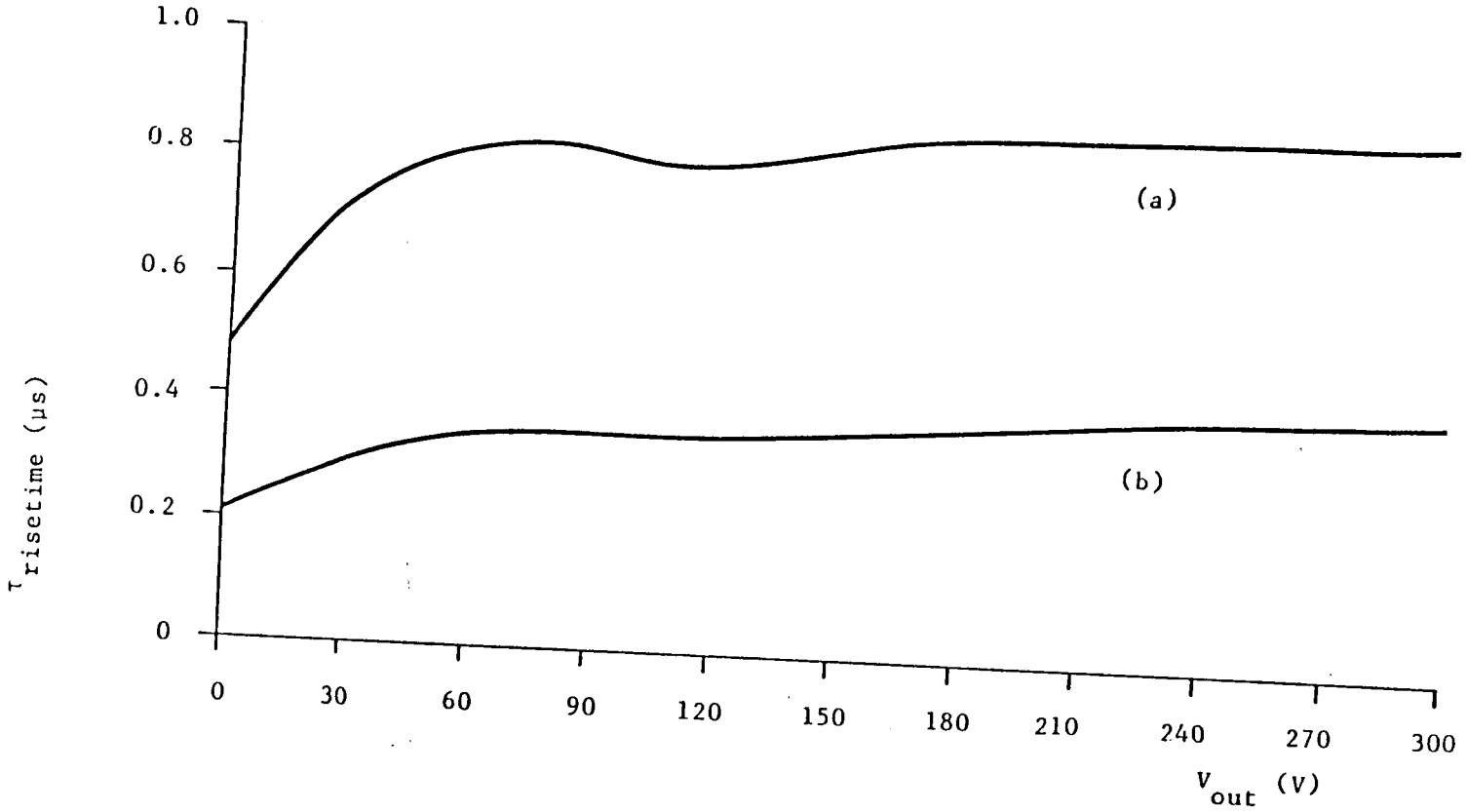

Figure 4.22. Measured risetime vs. output voltage for the driver amplifier: (a) with $C_L = 500$ pF, and (b) with $C_L = 0$.

Table 4.1. Comparison of hand analysis, SPICE analysis and experimental results

Quantity (small-signal)	HAND ANALYSIS	EXPERIMENTAL	SPICE
Midband loop transmission, T_{mid}	-316	–	-316
Midband closed-loop gain, A_{CL}	150.5	~ 150	150.4
C_L = 500 pF			
Loop transmission unity gain frequency	590 kHz	–	620 kHz
phase margin	77°	–	80°
Closed-loop high frequency -3 dB point	795 kHz	~ 700 kHz	820 kHz
C_L = 0			
Loop transmission unity gain frequency	1.25 MHz	–	1.5 MHz
phase margin	76°	–	79.5°
Low frequency -3 dB point	~ 1.5 Hz	~ 2 Hz	1.3 Hz
Input impedance (midband)	~ 1 kΩ	~ 1 kΩ	~ 1 kΩ
Output impedance (midband)	275 Ω	350 Ω	300 Ω

characteristics of the driver amplifier are shown. In getting the driver amplifier to work, several important construction techniques have to be followed, some of which are the following:

1. A good ground bus has to be implemented.
2. High and low voltage grounds should be separated.
3. Filter all power supplies.
4. Minimize lead lengths.
5. Minimize parasitic capacitances.
6. Output transistors must be provided with heat sinks to conduct heat away from the output transistors leading to thermal stability. A higher thermal stability can be achieved if the base-emitter voltage drops are compensated for by mounting the V_{BE} multiplier onto the heat sink or output transistor. A two-diode biasing network when mounted on the heat sink gives better compensation than the one diode compensation.

The cascode complementary output configuration was implemented and tested. The following problems were observed:

1. A distortion mode displaying hysteresis effects was triggered whenever the output drive increases beyond a certain point. The pre-output stage had unity gain when this effect was observed. It could have been a slew-induced effect and therefore an increase in the gain of the pre-output stage may be a solution to this problem.

2. Maintaining oscillation stability for various loads is not trivial because of the inherent high frequency performance of the cascode output configuration.

The advantages of this configuration are the following:

1. It could be more suited for higher frequency applications because there is no Miller effect in the output stage.
2. The output devices can be changed without any change in the bias condition.
3. It can be thermally stable if the output devices are MOSFETs.

CHAPTER 5

CONCLUSIONS

The driver amplifier developed in this thesis is used to drive capacitive loads that are at least as high as 500 pF. Driving higher loads requires a few minor adjustments in order to increase the bandwidth and slew rate. The design equations presented in Chap. 3 can be used to modify the driver amplifier for applications with different requirements.

The driver amplifier shown in Fig. 3.5 is capable of driving a 300 V pk-pk sinusoidal signal with a frequency of 150 kHz into a capacitive load that is at least 500 pF. A 300 V pk-pk step output can also be driven into the same load with no visible slewing. The amplifier is stable for any load and voltages higher than 300 V can be driven if the high voltage power supply voltages are increased and the output devices replaced with higher breakdown voltage devices.

The driver amplifier has a worst-case high frequency -3 dB point at ~450 kHz and a worst-case risetime of ~0.9 μs. The slew rate is much higher than that required to produce no distortion as can be seen in the step response and high voltage, high frequency sinusoidal response in Chap. 4.

As shown in Table 4.1, the hand analysis results, SPICE analysis results and experimental results agree to within 20%.

5.1 Suggestions for further work

Extending from the work presented here, areas could be investigated further. The following are a few suggestions that if implemented could improve the performance of this amplifier or generate more information useful for other applications.

1. The cascode complementary output configuration could be further studied to fully utilize its potential and also to apply it in driving a variety of loads.
2. The distortion mechanisms in the driver amplifier need to be more clearly identified and quantified.
3. More accurate SPICE modeling of the power transistors would be very useful in many applications.
4. A study of the quasi-complementary output configuration could perhaps lead to the development of a driver with a greater insensitivity to load changes.

LIST OF REFERENCES

LIST OF REFERENCES

1. Shields, F. D., Bass, H. E., and Bolen, L. N., "Tube method of sound-absorption measurement extended to frequencies far above cutoff," J. Acoust. Soc. Am., Vol. 62, No. 2, August 1977.

2. Bass, H. E., and Shields, F. D., "Absorption of sound in air: High-Frequency measurements," J. Acoust. Soc. Am., Vol. 62, No. 3, September 1977.

3. Bass, H. E., and Keeton, R. G., "Ultrasonic absorption in air at elevated temperatures," J. Acoust. Soc. Am., Vol. 58, No. 1, July 1975.

4. Ciarcia, S. A., "Home In on the Range! An Ultrasonic Ranging System," BYTE, November 1980.

5. Ciarcia, S. A., "An Ultrasonic Ranging System," BYTE, October 1984.

6. HPSPICE User's guide, Hewlett Packard Co., August 1983.

7. J. F. Pierce, T. J. Paulus, Applied Electronics, Colombus, Ohio: Charles E. Merrill Publishing Co., 1972.

8. Solomon, J. E., "The monolithic Op Amp: A Tutorial Study," IEEE J. Solid-State Circuits, Vol. SC-9, Dec. 1974.

9. Allen, P. E., "Slew Induced Distortion in Operational Amplifiers," IEEE J. Solid-State Circuits, Vol. SC-12, No. 1, February 1977.

10. Chuang, C. T., "Analysis of the Settling Behaviour of an Operational Amplifier," IEEE J. Solid-State Circuits, Vol. SC-17, No. 1, February 1982.

11. P. R. Gray, R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 2nd ed., John Wiley & Sons, New York, 1984.

12. Leach, W. M., "Suppression of Slew-Rate and Transient Intermodulation Distortions in Audio Power Amplifiers," Journal of the Audio Enginering Society, Vol. 25, No. 7/8, July/August 1977.

13. Haas, G. C., "Design Factors and Considerations in Full Complementary Symmetry Audio Power Amplifiers," Journal of the Audio Engineering Society, Vol. 16, No. 3, July 1968.

14. Kindlmann, P. J., "High-Voltage 'Video' Amplifier for Driving Piezoelectric Transducers," IEEE Trans. Instr. Meas., Vol. IM-20, No. 2, May 1971.

15. Rosenstark, S., "Loop Gain Measurement in Feedback Amplifiers," Int. J. Electronics, Vol. 57, No. 3, 1984.

16. Getreu, I., Modeling the Bipolar Transistor, Tektronix, Inc., 1976.

17. Blicher, A., Field-Effect and Bipolar Power Transistor Physics, Academic Press, New York, 1981.

18. Oxner, E. S., Power FETs and Their Applications, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1982.

19. Motorola Power Data Book, Motorola, Inc., 1982.

20. MOSPOWER Design Catalog, Siliconix, Inc., 1983.

21. CMOS/DMOS Databook, Supertex, Inc., 1983.

22. Transistor Databook, National Semiconductor Corp., 1982.

23. D. A. Hodges, H. G. Jackson, Analysis and Design of Digital Integrated Circuits, McGraw-Hill, New York, 1983.

APPENDICES

APPENDIX A

OUTPUT IMPEDANCE OF A V_{BE} MULTIPLIER

The model used to determine the output impedance is shown in Fig. A.1. A test current, I_t, is injected into the collector and the voltage at the collector is obtained. The current through resistor R_1 is

$$I_{R1} = \frac{V_C - V_B}{R_1} , \tag{A.1}$$

where V_B is the base voltage. The collector current is approximately

$$I_C \approx \frac{V_{BE}}{r_e} . \tag{A.2}$$

The sum of the currents at the collector is

$$I_t - I_{R1} - I_C = 0 . \tag{A.3}$$

The base current of the transistor is assumed much smaller than I_{R1} thus

$$I_{R1} \approx I_{R2} . \tag{A.4}$$

The emitter voltage is equivalent to

$$V_E = I_t R_L , \tag{A.5}$$

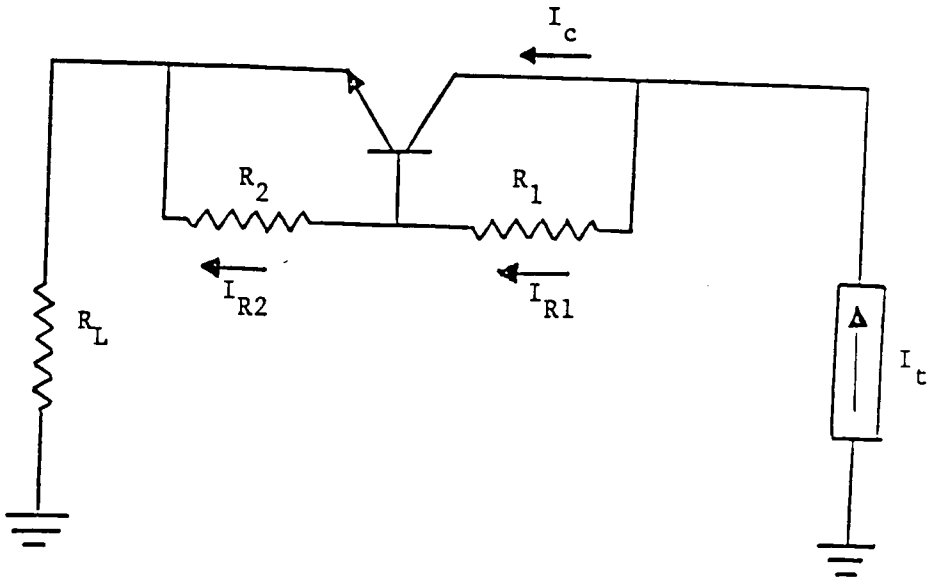

Figure A.1. Circuit used to determine output impedance of V_{BE} multiplier.

and the current through R_2 is equal to I_{R1} and is expressed as

$$I_{R2} = I_{R1} = \frac{V_{BE}}{R_2} \quad . \tag{A.6}$$

The test current, I_t, can be expressed as

$$I_t = \frac{V_{BE}}{r_e} + \frac{V_C - V_B}{R_1} \quad , \tag{A.7}$$

since the base voltage V_B is

$$V_B = I_t R_L + V_{BE} \quad . \tag{A.8}$$

Substituting Eq. (A.8) into (A.7) gives

$$I_t = \frac{V_{BE}}{r_e} + \frac{V_C}{R_1} - \frac{I_t R_L}{R_1} - \frac{V_{BE}}{R_1} \quad . \tag{A.9}$$

The base-emitter voltage can be expressed as

$$V_{BE} = \left(I_t - I_C\right) R_2 \quad , \tag{A.10}$$

and substituting Eq. (A.2) into Eq. (A.10) and solving for V_{BE} gives

$$V_{BE} = I_t R_2 \frac{r_e}{r_e + R_2} \quad . \tag{A.11}$$

Substituting Eq. (A.11) into (A.9) and solving for V_C/I_t gives the output impedance which is

$$R_{out} = R_1 + R_L - \frac{R_2 R_1}{r_e + R_2} + \frac{R_2 r_e}{r_e + R_2} \quad . \tag{A.12}$$

If $R_2 >> r_e$, and $R_L >> r_e$; then R_{out} becomes

$$R_{out} \approx R_L \quad . \tag{A.13}$$

If $R_L = 0$, the output impedance from Eq. (A.12) becomes

$$R_{out} = \frac{r_e\left(R_1 + R_2\right)}{r_e + R_2} \quad . \tag{A.14}$$

APPENDIX B

THERMAL STABILITY AND HEAT SINK REQUIREMENTS

Thermal instability in a power output stage occurs when the heating of a transistor due to the power dissipated in it causes the base-emitter voltage, V_{BE}, to drop by 2mV/°C which in turn causes more current to flow through the transistor and therefore cause more heating. This cycle, once started, can destroy the output transistors. This effect can be limited by negative feedback in the form of unbypassed emitter resistors and by adequate heat-sinking to dissipate the heat. The following derivation is closely related to that of Haas [6].

For thermal stability, the power dissipated in the device at or just after the peak junction temperature due to the dc bias at that moment must be less than the power dissipated when the signal is present. The dc bias at or just after the peak junction temperature is not equal to the initial dc bias. Referring to Fig. 3.5, the change in the output current for transistor Q_{10} is

$$\Delta I_o = \frac{\Delta V_{BE10}}{R_{E10}} \quad . \tag{B.1}$$

The power dissipated due to the bias current is

$$P_{bias} = \left[V_H - \left(I_o + \Delta I_o \right) R_{E10} \right] \left(I_o + \Delta I_o \right) \quad , \tag{B.2}$$

where V_H is the high voltage supply, I_o is the bias current before heating occurs, and R_{E10} is the emitter resistor of transistor Q_{10}. The change in the base-emitter voltage, V_{BE}, due to heating is

$$\Delta V_{BE10} = \Delta T_j \cdot K_{BE} , \tag{B.3}$$

where K_{BE} is equal to 2 mV/°C. The change in the junction temperature, ΔT_j, is

$$\Delta T_j = P_s \cdot \theta_{jA} , \tag{B.4}$$

where θ_{jA} is the thermal resistance between the transistor junction and free air and this includes the thermal resistance of the packaging, the insulation and the heat sinks.

For thermal stability the following has to hold

$$P_s > V_{CE10}\left(I_o + \Delta I_o\right) . \tag{B.5}$$

From Eq. (B.1), (B.3) and (B.4); Eq. (B.5) becomes

$$\left(P_s - V_{CE10} \cdot I_o\right) > V_{CE10} \cdot \frac{P_s \theta_{jA} K_{BE}}{R_{E10}} . \tag{B.6}$$

Using Eq. (B.6), one can solve for the required thermal resistance, θ_{jA} if R_{E10} is known or for R_{E10} if the thermal resistance is known.

APPENDIX C

SPICE ANALYSIS

The circuit used for the SPICE analysis is shown in Fig. C.1. All the input listings for the different analysis executed are included. A complete SPICE output, however, is included for the closed-loop gain determination only. The contents of this appendix are ordered as follows:

Analysis output for closed-loop gain

Input listing for the transient response

Input listing for the loop transmission

Input listing for the input impedance

Input listing for the output impedance

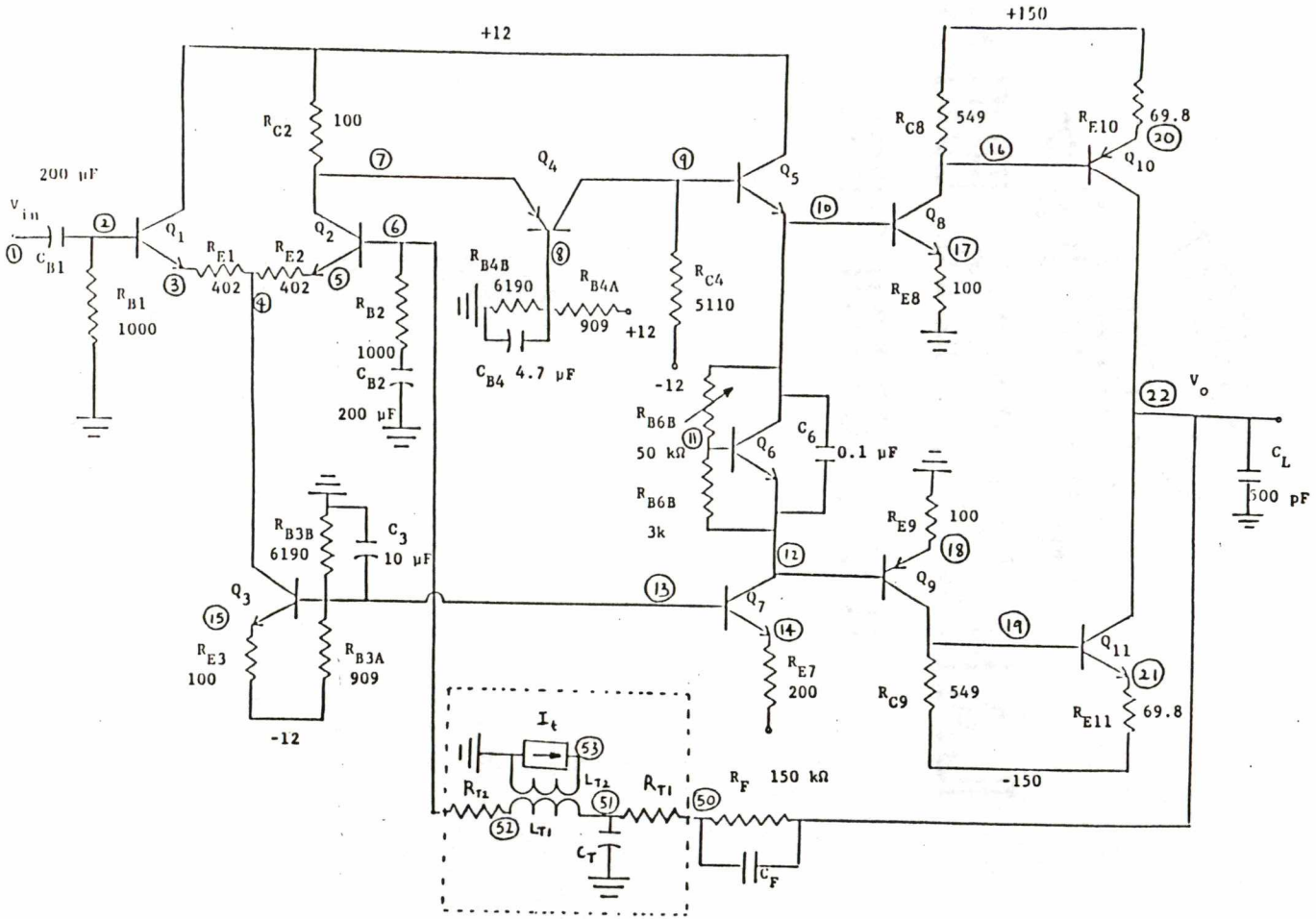

Figure C.1. Schematic of driver amplifier with nodes numbered for SPICE simulation. (Insert shows additional circuitry required to obtain the loop transmission).

****** 07/22/85 ******** HPSPICE (2.0 2330) ******** 16:25:51 ******

HIGH VOLTAGE DRIVER AMPLIFIER FOR CAPACITIVE LOADS

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
*
*--------------------------------------------------------------------
*This is the SPICE program listing and results for the driver
*amplifier being analyzed here.  This specific listing and the results
*are for the closed-loop gain, ACL.  The external file, MODELS, will
*contain the semi-conductor device models and will be linked with
*this file using the .INCLUDE command.  The protoboard parasitic
*capacitances are not included in this circuit model, but can
*easily be added as capacitors at the nodes in question.
*
*---THE SUBSEQUENT PROGRAM LISTINGS ARE THE ONES USED FOR
*---OBTAINING THE OTHER CHARACTERISTICS OF THE AMPLIFIER
*---PERFORMANCE.  THE DOCUMENTATION HERE HOLDS FOR THE OTHER
*---LISTINGS TOO.
*===The external file MODELS is also common to all the other listings.
*--------------------------------------------------------------------
*
*The independent sources are:
VLP 25 0 12
VLN 26 0 -12
VHP 27 0 150
VHN 28 0 -150
VSIG 1 0 AC
IOFF 6 0 -25.13U
*
*
.options nopage
*
*The external capacitors of the circuit are:
CC 2 1 200U
CB2 29 0 200U
CB3 13 0 10U
CB4 8 0 4.7U
C6 10 12 0.1U
```

```
CL 22 0 500PF
CF 6 22 1F
*
*
*The external resistors of the circuit are:
RB1 2 0 1K
RE1 3 4 402
RE2 4 5 402
RE3 26 15 100
RB3A 26 13 909
RB3B 13 0 6.19K
RB2 6 29 1K
RC2 25 7 100
RB4A 25 8 909
RB4B 8 0 6.19K
RC4A 9 26 5.11K
RB6A 10 11 2.45K
RB6B 11 12 3K
RE7 14 26 200
RC8 27 16 549
RE8 17 0 100
RE9 18 0 100
RE10 27 20 69.8
RE11 28 24 69.8
RC9 28 19 549
RF 22 6 150K
*
*
*The transistors in the circuit are:
Q1 25 2 3 MP311
Q2 7 6 5 MP311
Q3 4 13 15 Q2N4401
Q4 9 8 7 MPSH81
Q5 25 9 10 Q2N5962
Q6 10 11 12 Q2N4401
Q7 12 13 14 Q2N4401
Q8 16 10 17 Q2N6515
Q14 16 10 17 Q2N6515
Q15 16 10 17 Q2N6515
Q9 19 12 18 Q2N6519
Q16 19 12 18 Q2N6519
Q17 19 12 18 Q2N6519
Q10 22 16 20 Q2N6123
Q11 22 19 24 TIP50
*
*
*The following are the SPICE commands:
*INCLUDE MODELS
```

```
.MODEL MP311 NPN BF=260 BR=5 RB=130 RC=2 RE=0.5 TF=30PS
+TR=20NS CJE=4PF CJC=3.5PF IS=1E-14 VAF=100 VAR=10
+IK=50M NE=1.5

.MODEL Q2N3904 NPN BF=250 BR=1.3 RB=150 RC=2 RE=.6 TF=15.9PS
+TR=20NS CJE=4PF CJC=3.5PF IS=6.5E-14 VAF=180 VAR=8 IK=40M
+NE=1.4

.MODEL MPSH81 PNP BF=80 BR=2.3 RB=50 RC=5 RE=.3 TF=120PS
+TR=100PS CJE=3.1PF CJC=.8PF IS=3.5E-16 VAF=41 VAR=9 IK=15M
+NE=3

.MODEL Q2N5962 NPN BF=1000 BR=10 RB=60 RC=3 RE=.7 TF=155PS
+TR=10NS CJE=3PF CJC=4PF IS=5E-14 VAF=72 VAR=40 IK=20M NE=1.2

.MODEL Q2N6515 NPN BF=80 RB=20 RC=1 RE=.2 TF=3NS TR=20NS CJE=5PF
+CJC=6PF IS=1PA VAF=100 IK=40M NE=2

.MODEL Q2N6519 PNP BF=80 RB=20 RC=1 RE=.2  TF=3NS TR=25NS CJE=5PF
+CJC=8PF IS=1PA VAF=100 IK=40M NE=2

.MODEL Q2N4401 NPN BF=150 BR=1.8 RB=200 RC=1.3 RE=0.4 TF=70PS
+CJE=12PF CJC=4.5PF IS=1E-14 VAF=150 VAR=14 IK=80M NE=2

.MODEL Q2N3906 PNP BF=300 BR=2 RB=50 RC=2 RE=0.6 TF=20PS TR=20NS
+CJE=4PF CJC=3.5PF IS=1E-14 VAF=150 VAR=10 IK=40M NE=1.4

.MODEL Q2N6123 PNP BF=50 RB=500 RC=3 RE=1 TF=2500PS CJE=10PF
+CJC=100PF VAF=500 IS=1E-11 IK=1 NE=3
.MODEL TIP50 NPN BF=44 RB=600 RC=3 RE=1 TF=7600PS CJE=10PF CJC=65PF
+VAF=1000 IS=1E-11 IK=400M NE=2.2
** END OF ../MODELS/circuit_file
.AC DEC 10 1 100MEG
.PRINT AC VM(22) VP(22)
*.GRAPH AC VM(22) VP(22)
.END
```

**** BJT MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

	MP311	Q2N3904	MPSH81	Q2N5962	Q2N6515	Q2N6519	Q2N4401
TYPE	NPN	NPN	PNP	NPN	NPN	PNP	NPN
IS	1.00D-14	6.50D-14	3.50D-16	5.00D-14	1.00D-12	1.00D-12	1.00D-14
BF	260.000	250.000	80.000	1000.000	80.000	80.000	150.000
NF	1.000	1.000	1.000	1.000	1.000	1.000	1.000
VAF	1.00D+02	1.80D+02	4.10D+01	7.20D+01	1.00D+02	1.00D+02	1.50D+02
IKF	5.00D-02	4.00D-02	1.50D-02	2.00D-02	4.00D-02	4.00D-02	8.00D-02
NE	1.500	1.400	3.000	1.200	2.000	2.000	2.000
BR	5.000	1.300	2.300	10.000	1.000	1.000	1.800
NR	1.000	1.000	1.000	1.000	1.000	1.000	1.000
VAR	1.00D+01	8.00D+00	9.00D+00	4.00D+01	0.00D+00	0.00D+00	1.40D+01
RB	130.000	150.000	50.000	60.000	20.000	20.000	200.000
RE	.500	.600	.300	.700	.200	.200	.400
RC	2.000	2.000	5.000	3.000	1.000	1.000	1.300
CJE	4.00D-12	4.00D-12	3.10D-12	3.00D-12	5.00D-12	5.00D-12	1.20D-11
TF	3.00D-11	1.59D-11	1.20D-10	1.55D-10	3.00D-09	3.00D-09	7.00D-11
CJC	3.50D-12	3.50D-12	8.00D-13	4.00D-12	6.00D-12	8.00D-12	4.50D-12
TR	2.00D-08	2.00D-08	1.00D-10	1.00D-08	2.00D-08	2.50D-08	0.00D+00

**** BJT MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

	Q2N3906	Q2N6123	TIP50
TYPE	PNP	PNP	NPN
IS	1.00D-14	1.00D-11	1.00D-11
BF	300.000	50.000	44.000
NF	1.000	1.000	1.000
VAF	1.50D+02	5.00D+02	1.00D+03
IKF	4.00D-02	1.00D+00	4.00D-01
NE	1.400	3.000	2.200
BR	2.000	1.000	1.000
NR	1.000	1.000	1.000
VAR	1.00D+01	0.00D+00	0.00D+00
RB	50.000	500.000	600.000
RE	.600	1.000	1.000
RC	2.000	3.000	3.000
CJE	4.00D-12	1.00D-11	1.00D-11
TF	2.00D-11	2.50D-09	7.60D-09
CJC	3.50D-12	1.00D-10	6.50D-11
TR	2.00D-08	0.00D+00	0.00D+00

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	.0000	(2)	-.0102	(3)	-.6931	(4)	-1.7624
(5)	.1619	(6)	.8637	(7)	11.2590	(8)	10.4896
(9)	1.3137	(10)	.6616	(11)	.0281	(12)	-.6691
(13)	-10.5271	(14)	-11.2246	(15)	-11.2499	(16)	149.1389
(17)	.1645	(18)	-.1710	(19)	-149.1148	(20)	149.6859
(22)	-.0011	(24)	-149.6841	(25)	12.0000	(26)	-12.0000
(27)	150.0000	(28)	-150.0000	(29)	.8637		

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VLP	-1.557D-02
VLN	1.560D-02
VHP	-6.069D-03
VHN	6.138D-03
VSIG	0.000D+00

TOTAL POWER DISSIPATION 2.21D+00 WATTS

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

	Q1	Q2	Q3	Q4	Q5	Q6	Q7
MODEL	MP311	MP311	Q2N4401	MPSH81	Q2N5962	Q2N4401	Q2N4401
IB	1.02E-05	1.94E-05	5.38E-05	-3.30E-05	3.97E-06	2.62E-05	2.65E-05
IC	2.65E-03	4.77E-03	7.45E-03	-2.61E-03	3.85E-03	3.58E-03	3.85E-03
VBE	.683	.702	.723	-.769	.652	.697	.698
VBC	-12.010	-10.395	-8.765	9.176	-10.686	-.634	-9.858
VCE	12.693	11.097	9.488	-9.945	11.338	1.331	10.556
BETADC	260.410	246.192	138.384	78.993	967.657	136.818	145.564
GM	9.75E-02	1.69E-01	2.65E-01	8.88E-02	1.30E-01	1.32E-01	1.42E-01
RPI	2.54E+03	1.34E+03	4.81E+02	7.83E+02	6.51E+03	9.87E+02	9.78E+02
RX	1.30E+02	1.30E+02	2.00E+02	5.00E+01	6.00E+01	2.00E+02	2.00E+02
RO	3.97E+04	2.17E+04	2.03E+04	1.79E+04	2.12E+04	4.00E+04	3.96E+04
CPI	9.30E-12	1.15E-11	3.81E-11	1.59E-11	2.48E-11	2.85E-11	2.92E-11
CMU	1.37E-12	1.44E-12	1.95E-12	3.41E-13	1.63E-12	3.68E-12	1.88E-12
CBX	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CCS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
BETAAC	247.787	226.351	127.316	69.503	844.104	130.661	138.978
FT	1.45E+09	2.08E+09	1.05E+09	8.70E+08	7.81E+08	6.54E+08	7.27E+08

	Q8	Q14	Q15	Q9	Q16	Q17	Q10
MODEL	Q2N6515	Q2N6515	Q2N6515	Q2N6519	Q2N6519	Q2N6519	Q2N6123
IB	2.76E-06	2.76E-06	2.76E-06	-2.87E-06	-2.87E-06	-2.87E-06	-6.85E-05
IC	5.46E-04	5.46E-04	5.46E-04	-5.67E-04	-5.67E-04	-5.67E-04	-4.43E-03
VBE	.497	.497	.497	-.498	-.498	-.498	-.547
VBC	-148.477	-148.477	-148.477	148.446	148.446	148.446	149.140
VCE	148.974	148.974	148.974	-148.944	-148.944	-148.944	-149.687
BETADC	197.707	197.70	197.707	197.639	197.639	197.639	64.695
GM	2.10E-02	2.10E-02	2.10E-02	2.18E-02	2.18E-02	2.18E-02	1.71E-01
RPI	9.37E+03	9.37E+03	9.37E+03	9.01E+03	9.01E+03	9.01E+03	3.78E+02
RX	2.00E+01	2.00E+01	2.00E+01	2.00E+01	2.00E+01	2.00E+01	5.00E+02
RO	4.55E+05	4.55E+05	4.55E+05	4.38E+05	4.38E+05	4.38E+05	1.46E+05
CPI	6.99E-11	6.99E-11	6.99E-11	7.24E-11	7.24E-11	7.24E-11	4.41E-10
CMU	1.05E-12	1.05E-12	1.05E-12	1.39E-12	1.39E-12	1.39E-12	1.74E-11
CBX	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CCS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
BETAAC	196.602	196.602	196.602	196.493	196.493	196.493	64.473
FT	4.71E+07	4.71E+07	4.71E+07	4.70E+07	4.70E+07	4.70E+07	5.93E+07

	Q11
MODEL	TIP50
IB	8.86E-05
IC	4.44E-03
VBE	.569
VBC	-149.114
VCE	149.683
BETADC	50.079
GM	1.70E-01
RPI	2.92E+02
RX	6.00E+02
RO	2.59E+05
CPI	1.31E-09
CMU	1.13E-11
CBX	0.00E+00
CCS	0.00E+00
BETAAC	49.604
FT	2.05E+07

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

FREQ	VM(22)	VP(22)
1.000E+00	9.210E+01	7.663E+01
1.259E+00	1.074E+02	6.427E+01
1.585E+00	1.201E+02	5.306E+01
1.995E+00	1.297E+02	4.328E+01
2.512E+00	1.366E+02	3.499E+01
3.162E+00	1.413E+02	2.812E+01
3.981E+00	1.445E+02	2.251E+01
5.012E+00	1.466E+02	1.797E+01
6.310E+00	1.479E+02	1.432E+01
7.943E+00	1.488E+02	1.141E+01
1.000E+01	1.493E+02	9.081E+00
1.259E+01	1.497E+02	7.228E+00
1.585E+01	1.499E+02	5.754E+00
1.995E+01	1.501E+02	4.581E+00
2.512E+01	1.502E+02	3.647E+00
3.162E+01	1.503E+02	2.903E+00
3.981E+01	1.503E+02	2.311E+00
5.012E+01	1.504E+02	1.838E+00
6.310E+01	1.504E+02	1.460E+00
7.943E+01	1.504E+02	1.159E+00
1.000E+02	1.504E+02	9.179E-01
1.259E+02	1.504E+02	7.254E-01
1.585E+02	1.504E+02	5.712E-01
1.995E+02	1.504E+02	4.471E-01
2.512E+02	1.505E+02	3.468E-01
3.162E+02	1.505E+02	2.648E-01
3.981E+02	1.505E+02	1.970E-01
5.012E+02	1.505E+02	1.396E-01
6.310E+02	1.505E+02	8.963E-02
7.943E+02	1.505E+02	4.444E-02
1.000E+03	1.505E+02	1.617E-03
1.259E+03	1.505E+02	-4.112E-02
1.585E+03	1.505E+02	-8.605E-02
1.995E+03	1.505E+02	-1.356E-01
2.512E+03	1.505E+02	-1.923E-01
3.162E+03	1.505E+02	-2.593E-01
3.981E+03	1.505E+02	-3.401E-01
5.012E+03	1.505E+02	-4.389E-01
6.310E+03	1.505E+02	-5.612E-01
7.943E+03	1.505E+02	-7.133E-01

1.000E+04	1.504E+02	-9.035E-01
1.259E+04	1.504E+02	-1.142E+00
1.585E+04	1.504E+02	-1.441E+00
1.995E+04	1.504E+02	-1.816E+00
2.512E+04	1.504E+02	-2.289E+00
3.162E+04	1.504E+02	-2.883E+00
3.981E+04	1.503E+02	-3.630E+00
5.012E+04	1.502E+02	-4.569E+00
6.310E+04	1.501E+02	-5.751E+00
7.943E+04	1.499E+02	-7.238E+00
1.000E+05	1.496E+02	-9.105E+00
1.259E+05	1.490E+02	-1.145E+01
1.585E+05	1.482E+02	-1.439E+01
1.995E+05	1.470E+02	-1.806E+01
2.512E+05	1.450E+02	-2.264E+01
3.162E+05	1.420E+02	-2.830E+01
3.981E+05	1.374E+02	-3.525E+01
5.012E+05	1.308E+02	-4.363E+01
6.310E+05	1.216E+02	-5.355E+01
7.943E+05	1.094E+02	-6.494E+01
1.000E+06	9.457E+01	-7.751E+01
1.259E+06	7.827E+01	-9.084E+01
1.585E+06	6.208E+01	-1.044E+02
1.995E+06	4.744E+01	-1.181E+02
2.512E+06	3.517E+01	-1.318E+02
3.162E+06	2.542E+01	-1.458E+02
3.981E+06	1.793E+01	-1.605E+02
5.012E+06	1.235E+01	-1.764E+02
6.310E+06	8.287E+00	1.660E+02
7.943E+06	5.386E+00	1.460E+02
1.000E+07	3.339E+00	1.229E+02
1.259E+07	1.919E+00	9.648E+01
1.585E+07	9.944E-01	6.825E+01
1.995E+07	4.659E-01	4.068E+01
2.512E+07	2.047E-01	1.529E+01
3.162E+07	8.773E-02	-7.999E+00
3.981E+07	3.766E-02	-2.998E+01
5.012E+07	1.644E-02	-5.129E+01
6.310E+07	7.366E-03	-7.224E+01
7.943E+07	3.405E-03	-9.275E+01
1.000E+08	1.630E-03	-1.125E+02

JOB CONCLUDED

```
HIGH VOLTAGE DRIVER AMPLIFIER FOR CAPACITIVE LOADS
*
*This listing is for obtaining the transient response
*of the driver amplifier
*
VLP 25 0 12
VLN 26 0 -12
VHP 27 0 150
VHN 28 0 -150
*
*VSIG will be changed as different inputs are required
*
VSIG 1 0 pwl 0 0 1ns -.0333 1u -.0333 1.001u .0333 8u .0333
+8.001u -.0333 11u -.0333
IOFF 6 0 -25.13U
*
*
CC 2 1 200U
CB2 29 0 200U
CB3 13 0 10U
CB4 8 0 4.7U
C6 10 12 0.1U
CL 65 0 500PF
*
*
RB1 2 0 1K
RE1 3 4 402
RE2 4 5 402
RE3 26 15 100
RB3A 26 13 909
RB3B 13 0 6.19K
RB2 6 29 1K
RC2 25 7 100
RB4A 25 8 909
RB4B 8 0 6.19K
RC4A 9 26 5.11K
RB6A 10 11 2.45K
RB6B 11 12 3K
RE7 14 26 200
RC8 27 16 549
RE8 17 0 100
RE9 18 0 100
RE10 27 20 69.8
RE11 28 24 69.8
RC9 28 19 549
RF 22 6 150K
*
*
```

```
Q1 25 2 3 MP311
Q2 7 6 5 MP311
Q3 4 13 15 Q2N4401
Q4 9 8 7 MPSH81
Q5 25 9 10 Q2N5962
Q6 10 11 12 Q2N4401
Q7 12 13 14 Q2N4401
Q8 16 10 17 Q2N6515
Q14 16 10 17 Q2N6515
Q15 16 10 17 Q2N6515
Q9 19 12 18 Q2N6519
Q16 19 12 18 Q2N6519
Q17 19 12 18 Q2N6519
Q10 60 16 20 Q2N6123
Q11 61 19 24 TIP50
*
VIPO 60 22 0
VINE 61 22 0
VIO 22 65 0
*
.INCLUDE MODELS
.TRAN 55NS 11U
*.PRINT TRAN V(10) V(17) V(16) V(20)
*.PRINT TRAN V(22) V(2,6) I(VIO)
.GRAPH TRAN V(22) V(16) V(20) V(10) V(17) V(2,6) I(VIO) v(24)
.END
```

```
HIGH VOLTAGE DRIVER AMPLIFIER FOR CAPACITIVE LOADS

*
*This listing is for obtaining the loop transmission of
*the driver amplifier.
*
*
VLP 25 0 12
VLN 26 0 -12
VHP 27 0 150
VHN 28 0 -150
VSIG 1 0 AC 0
IOFF 6 0 -25.13U
*
*
CC 2 1 200U
CB2 29 0 200U
CB3 13 0 10U
CB4 8 0 4.7U
C6 10 12 0.1U
CL 22 0 500PF
*
*
RB1 2 0 1K
RE1 3 4 402
RE2 4 5 402
RE3 26 15 100
RB3A 26 13 909
RB3B 13 0 6.19K
RB2 6 29 1K
RC2 25 7 100
RB4A 25 8 909
RB4B 8 0 6.19K
RC4A 9 26 5.11K
RB6A 10 11 2.45K
RB6B 11 12 3K
RE7 14 26 200
RC8 27 16 549
RE8 17 0 100
RE9 18 0 100
RE10 27 20 69.8
RE11 28 24 69.8
RC9 28 19 549
RF 22 50 150K
*
*
Q1 25 2 3 MP311
Q2 7 6 5 MP311
```

```
Q3 4 13 15 Q2N4401
Q4 9 8 7 MPSH81
Q5 25 9 10 Q2N5962
Q6 10 11 12 Q2N4401
Q7 12 13 14 Q2N4401
Q8 16 10 17 Q2N6515
Q14 16 10 17 Q2N6515
Q15 16 10 17 Q2N6515
Q9 19 12 18 Q2N6519
Q16 19 12 18 Q2N6519
Q17 19 12 18 Q2N6519
Q10 22 16 20 Q2N6123
Q11 22 19 24 TIP50
*
*
RT1 50 51 1
RT2 52 6 1
CT 51 0 1000
LT1 51 52 10K
LT2 53 0 10K
KT LT1 LT2 1
IT 53 0 AC
*
*
.INCLUDE MODELS
.AC DEC 10 1 100MEG
.PRINT AC VM(50,51) VP(50,51)
.PRINT AC VM(6) VM(7) VM(9) VM(10) VM(16)
.PRINT AC VM(16) VM(22)
*.PLOT AC VM(50,51) VP(50,51)
.GRAPH AC VDB(50,51) VP(50,51)
.END
```

```
HIGH VOLTAGE DRIVER AMPLIFIER FOR CAPACITIVE LOADS
*
*This program listing is for obtaining the input
*impedance of the driver amplifier
*
VLP 25 0 12
VLN 26 0 -12
VHP 27 0 150
VHN 28 0 -150
ISIG 1 0 AC
IOFF 6 0 -25.13U
*
RDC 1 0 1T
*
CC 2 1 200U
CB2 29 0 200U
CB3 13 0 10U
CB4 8 0 4.7U
C6 10 12 0.1U
CL 22 0 500PF
*
*
RB1 2 0 1K
RE1 3 4 402
RE2 4 5 402
RE3 26 15 100
RB3A 26 13 909
RB3B 13 0 6.19K
RB2 6 29 1K
RC2 25 7 100
RB4A 25 8 909
RB4B 8 0 6.19K
RC4A 9 26 5.11K
RB6A 10 11 2.45K
RB6B 11 12 3K
RE7 14 26 200
RC8 27 16 549
RE8 17 0 100
RE9 18 0 100
RE10 27 20 69.8
RE11 28 24 69.8
RC9 28 19 549
RF 22 6 150K
*
*
Q1 25 2 3 MP311
Q2 7 6 5 MP311
```

```
Q3 4 13 15 Q2N4401
Q4 9 8 7 MPSH81
Q5 25 9 10 Q2N5962
Q6 10 11 12 Q2N4401
Q7 12 13 14 Q2N4401
Q8 16 10 17 Q2N6515
Q14 16 10 17 Q2N6515
Q15 16 10 17 Q2N6515
Q9 19 12 18 Q2N6519
Q16 19 12 18 Q2N6519
Q17 19 12 18 Q2N6519
Q10 22 16 20 Q2N6123
Q11 22 19 24 TIP50
*
*
.INCLUDE MODELS
.AC DEC 10 1 100MEG
.PRINT AC VM(2) VP(2)
*.PLOT AC VM(2) VP(2)
.GRAPH AC VM(2) VP(2)
.END
```

```
HIGH VOLTAGE DRIVER AMPLIFIER FOR CAPACITIVE LOADS
*
*This listing is for obtaining the output impedance
*of the driver amplifier
*
VLP 25 0 12
VLN 26 0 -12
VHP 27 0 150
VHN 28 0 -150
VSIG 1 0 AC 0
ISIG 0 22 AC
IOFF 6 0 -25.13U
*
*
CC 2 1 200u
CB2 29 0 200u
CB3 13 0 10U
CB4 8 0 4.7u
C6 10 12 0.1U
*
*
RB1 2 0 1K
RE1 3 4 402
RE2 4 5 402
RE3 26 15 100
RB3A 26 13 909
RB3B 13 0 6.19K
RB2 6 29 1K
RC2 25 7 100
RB4A 25 8 909
RB4B 8 0 6.19K
RC4A 9 26 5.11K
RB6A 10 11 2.45K
RB6B 11 12 3K
RE7 14 26 200
RC8 27 16 549
RE8 17 0 100
RE9 18 0 100
RE10 27 20 69.8
RE11 28 24 69.8
RC9 28 19 549
RF 22 6 150K
*
*
Q1 25 2 3 MP311
Q2 7 6 5 MP311
Q3 4 13 15 Q2N4401
Q4 9 8 7 MPSH81
```

```
Q5 25 9 10 Q2N5962
Q6 10 11 12 Q2N4401
Q7 12 13 14 Q2N4401
Q8 16 10 17 Q2N6515
Q14 16 10 17 Q2N6515
Q15 16 10 17 Q2N6515
Q9 19 12 18 Q2N6519
Q16 19 12 18 Q2N6519
Q17 19 12 18 Q2N6519
Q10 22 16 20 Q2N6123
Q11 22 19 24 TIP50
*
*
.INCLUDE MODELS
.AC DEC 10 1 100MEG
.PRINT AC VM(22) VP(22) VDB(22)
*.PLOT AC VM(22) VP(22) VDB(22)
.GRAPH AC VM(22) VP(22) VDB(22)
.END
```

APPENDIX D

DETERMINATION OF THE OPEN-LOOP OUTPUT IMPEDANCE OF THE COMMON-EMITTER COMPLEMENTARY OUTPUT STAGE

The open-loop output impedance is used to determine the closed-loop output impedance of the driver amplifier by Blackman's theorem. A test current is injected into the output and the voltage developed at the output divided by the test current gives the output impedance. The hybrid-π model that is used to determine the open-loop output impedance is shown in Fig. D.1.

The following assumptions and simplifications will be used:

1. The base-collector capacitances, C_{ob10} and C_{ob11} are both replaced with a value $(C_{ob11} + C_{ob10})/2$
2. The base-emitter voltages are equal, $V_{be10} = V_{be11}$.
3. The total base resistances of Q_{10} and Q_{11} are equal and are $R_{b10} = R_{b11} = R_B \parallel [(\beta+1)(r_e + R_E)]$, where R_B is the resistance of the bases and R_E is the emitter resistance.
4. The transconductances of the two transistors take the unbypassed emitter resistance into consideration. This leads to $g_{m10} = g_{m11} = 1/(r_e + R_E)$.
5. The output impedances of Q_{10} and Q_{11}, V_{o10} and V_{o11}, are obtained from Eq. (3.2-7) and take into consideration, the base and emitter resistances.

Summing the currents at the node with voltage V_o gives

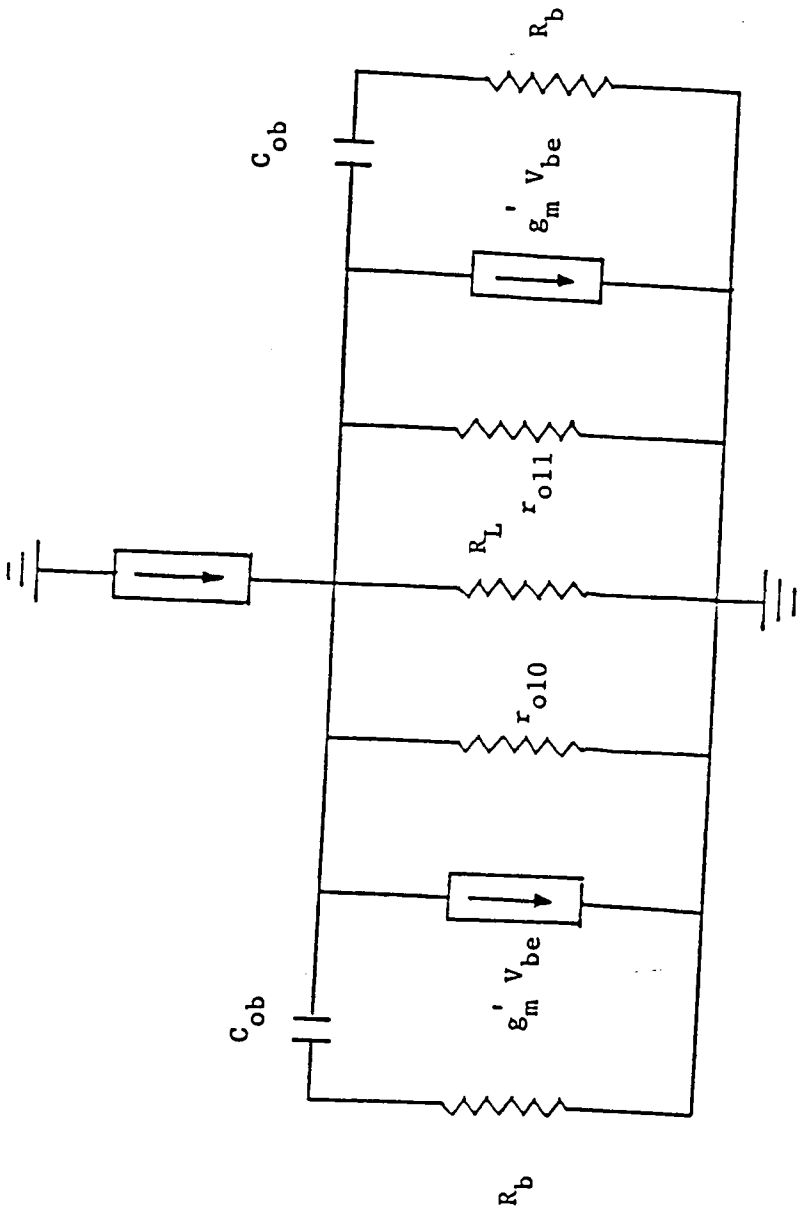

Figure D.1. Hybrid-π model of complementary common-emitter output stage used to determine open-loop output impedance.

$$I_t = \frac{2V_o}{R_b + \dfrac{1}{j2\pi f C_{ob}}} + 2g_m' V_{be} + \frac{V_o}{R_L \| r_{o10} \| r_{o11}} \quad . \tag{D.1}$$

Now the base-emitter voltage is equal to

$$V_{be} = \frac{V_o R_b j2\pi f C_{ob}}{1 + R_b j2\pi f C_{ob}} \quad , \tag{D.2}$$

so substituting Eq. (D.2) into Eq. (D.1) and solving for V_o/I_t gives the output impedance as

$$Z_{out}^{o\ell} \approx \frac{R_L' \left(1 + R_b j2\pi f C_{ob}\right)}{1 + j2\pi f C_{ob} \left[2 R_L' + 2 g_m' R_b R_L' + R_b\right]} \quad , \tag{D.3}$$

where

$$R_L' = R_L \| r_{o10} \| r_{011} \quad .$$

Re-arranging Eq. (D.3) gives

$$Z_{out}^{o\ell} \approx \frac{R_L' \left(1 + R_b j2\pi f C_{ob}\right)}{1 + j2\pi f C_{ob} R_b \left[1 + \dfrac{2 R_L'}{R_b} + 2 g_m' R_L'\right]} \quad , \tag{D.4}$$

and from Eq. (D.4), it is clear that after assuming $2g_m' R_L' >> (1 + 2 R_L/R_b)$; the capacitance C_{ob} is effectively multiplied by twice the Miller gain, $2 g_m' R_L'$.

VITA

Abdullah A. Bagersh was born in Addis Ababa, Ethiopia on January 11, 1962. He was graduated from the Sandford English Community School in Addis Ababa, Ethiopia in June 1978 and then entered the University of Tennessee in June 1979. He received his Bachelor of Science degree in Electrical Engineering in August 1982. He was a teaching Assistant starting in September 1982 and a Research Assistant starting in June 1984 and received the Master of Science degree in Electrical Engineering in August 1985.