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I am submitting herewith a thesis written by Bryan Scott Puckett entitled "A Low Dead Time Variable CMOS Delay for the Nuclear Weapons Identification System." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

T.V. Blalock, Major Professor

We have read this thesis
and recommend its acceptance:

Accepted for the Council:

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and Dean of The Graduate School

A Low Dead Time Variable CMOS Delay for the Nuclear Weapons Identification System

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Bryan Scott Puckett

August 1998

Acknowledgments

I would like to thank my ORNL mentor Dr. Mike Paulus for his time, patience, technical advice, and most of all for his encouragement throughout this project. I would like to thank my major professor Dr. T. V. Blalock for his guidance and support during both my undergraduate and graduated studies. I would like to thank Dr. Rochelle for serving on my committee. I would also like to thank the people who made it possible for the UT/ORNL joint program to provide such a rich educational experience.

I would also like to thank my wife Nicole for all of her understanding and support through this stressful and busy time.

This research project was sponsored by the U.S. Department of Energy and performed at Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corporation for the U.S. Department of Energy under Contract No. DE-AC05-96OR22464.

Abstract

The architecture and performance of a new CMOS based, low dead time, variable delay is described. This delay was developed to provide capability for channel synchronization in the Nuclear Weapons Identification System (NWIS) front-end electronics ASIC. The delay is variable over a 500ns range in smaller than 100ps steps. Low dead time is achieved by using a switched parallel channel architecture. The delay channels are feedback stabilized using a phase locked loop (PLL) locked to a crystal reference. A prototype has been fabricated in the 1.2u AMI process and tested to evaluate its performance.

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Chapter 1 Introduction

1.1 NWIS Overview

1.1.1 Historical Overview

The Nuclear Weapons Identification System (NWIS) is an emerging technology developed at the Oak Ridge National Laboratory to inspect nuclear warheads and warhead components. NWIS uses active neutron interrogation (measurement of the response of a fissile assembly to a neutron flux) to produce time and frequency domain signatures of the device under test. These signatures are highly correlated to the physical design and fissile content of the device under examination. NWIS is useful for stockpile management and can also be configured so that design details are not revealed, making it useful for treaty verification. Some of the advantages of NWIS are its short acquisition times, the background radiation independence of some its signatures, its ability to detect omission of as little as 5% of fissile mass and its configurability to be non-revealing (Mihalczo 1994). From its inception in 1984 until 1996, use of the NWIS system was very limited due to the bulky hardware, slow sample rates and low processing power. A version of NWIS that became operational in 1996 (Figure 1) greatly improved the size, sampling rate, and processing speed and has been used to take measurements of 17 different weapons systems (Figure 2) (Mihalczo 1996).

Currently work is being done to further reduce the size and power consumption of NWIS in order to produce a highly portable laptop based system (Figure 3) that can be easily deployed in the field (Mihalczo 1997).

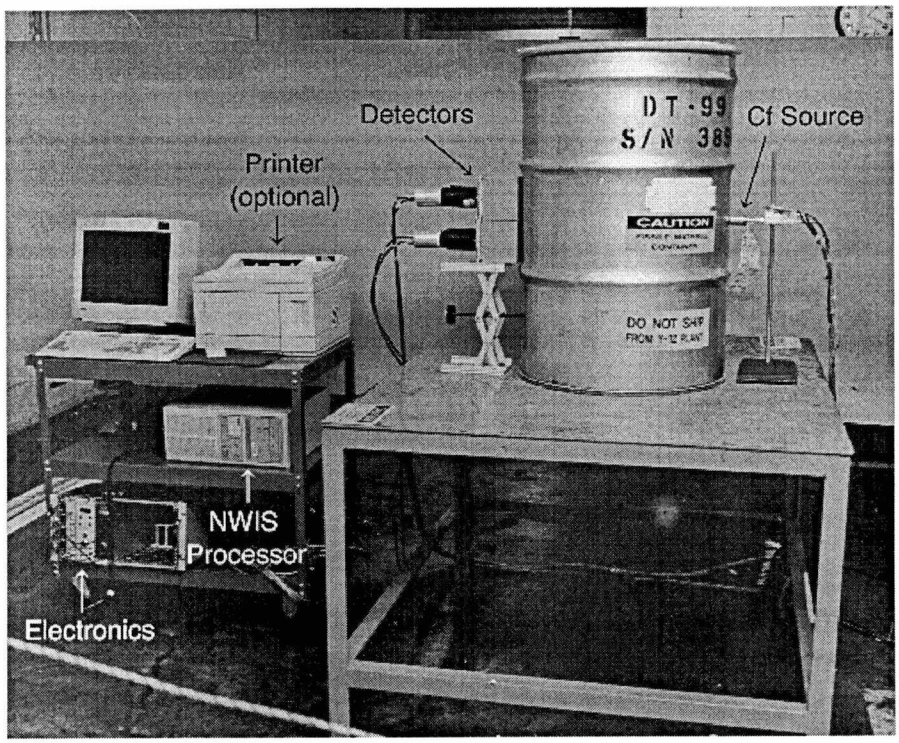


Figure 1: Picture of Current NWIS

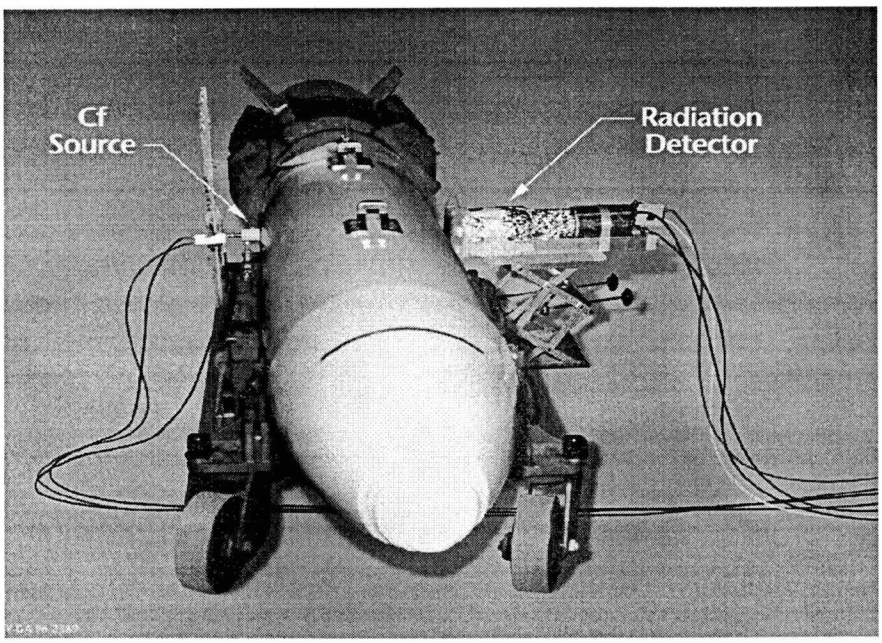


Figure 2: NWIS Inspection of a Weapon System

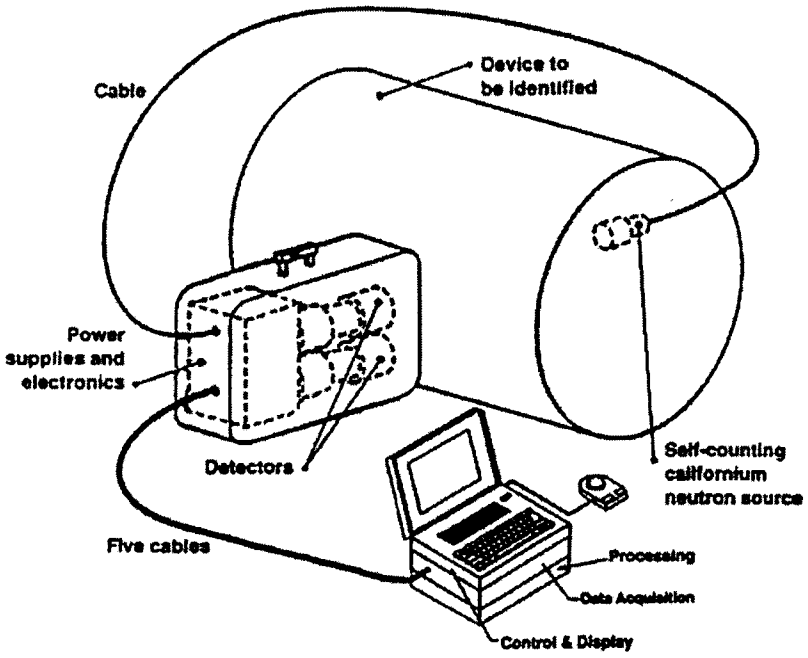


Figure 3: Theoretical Sketch of a Laptop Based NWIS

1.1.2 System Description

NWIS measures the response of a fissile assembly to a neutron flux produced by a ^{252}Cf source. ^{252}Cf is a spontaneous fission source which emits neutrons and gamma rays. As seen in Figure 4, neutrons from the ^{252}Cf source penetrate the object under test and induce fission multiplication in the fissile material resulting in the emission of more neutrons and gamma rays. These emitted particles, along with particles from the source, are detected by an array of two to four scintillators attached to photomultiplier tubes (PMTs) (Mihalczo 1995). The scintillators are made of an organically doped material (in this case liquid or plastic) which emits photons when struck by energetic particles.

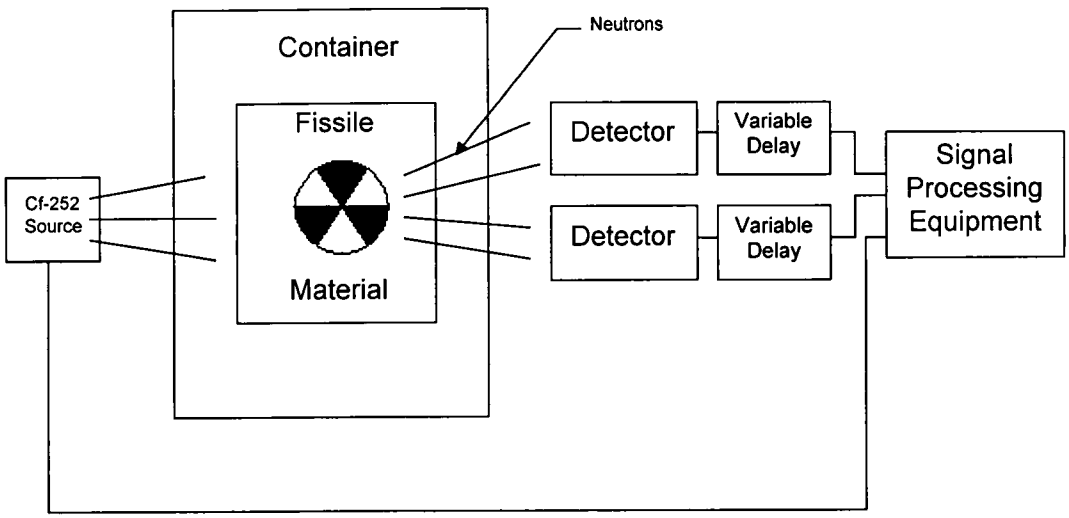


Figure 4: NWIS system diagram

1.1.3 Time Signatures

The particles collected by the detectors fall into three categories: directly transmitted, scattered, and induced. The directly transmitted particles pass through the container with no interaction. The scattered particles undergo Compton scattering and transfer some of their energy to the atom with which they interact. The induced particles are produced when a particle from the source is scattered by an atom in the fissile material and loses enough energy to trigger the fission of that atom. The fission results in the release of more particles that in turn can induce further fissions resulting in a multiplication effect. The typical distribution in arrival times at the detectors for these particles is shown in Figure 5. (Mihalczo 1997)

1.1.4 Role of Adjustable Delay

In order to accurately measure NWIS time and frequency signatures, the signal processing delays must be calibrated so that data from simultaneous events

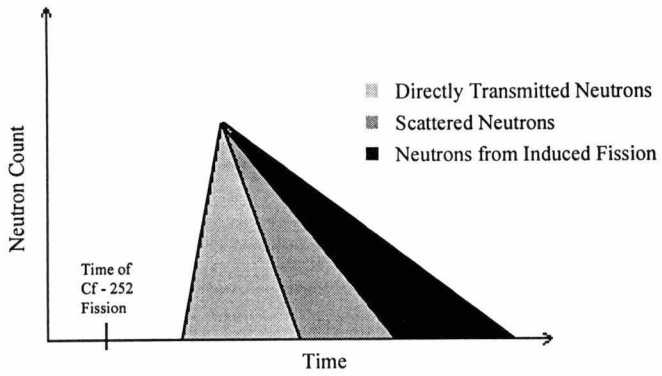


Figure 5: Time Analysis Signature Plot

arrive at the data collection system at the same time. This synchronization requirement necessitates a variable delay in each channel since compensation must be made for time of flight differences and cabling differences. It is desirable for the channels to be synchronized to a resolution of 100ps or less. Earlier NWIS implementations used cables to generate the required delays with variability being achieved by changing cables. These cable delays resulted in large bulky hardware. The current NWIS delay lines are composed of off-the-shelf monolithic distributed inductor-capacitor (LC) delay lines such as the Data Delay MDU13H-50. Variability is accomplished by switching fixed delays in to and out of the circuit.

1.1.5 Need for a CMOS Delay

In order to construct a highly portable laptop based version of NWIS, it is desirable to collect all of the front-end electronics onto one CMOS Application Specific Integrated Circuit (ASIC). Putting the front-end electronics on an ASIC would greatly reduce its size, but would require that all of the circuitry (including the variable delay) be implemented using a standard CMOS process. Thus a CMOS variable delay implementation is needed.

1.2 Delay Overview

Most monolithic variable delays can be classified into one of two types: digitally generated delays or analog delays.

1.2.1 Digitally Generated Delays

Digitally generated delays are typically synchronous devices that are controlled by a system clock. This type of delay includes counter-based delays, shift register based delays and Charge Coupled Device (CCD) based delays.

Counter based delays (Figure 6) use a digital counter to count up to (or down from) a predefined number. When the specified value is reached the output circuitry is activated. Adjustability is accomplished by selection of different counter values. Since it is difficult to control and count very high frequencies, these are typically used for delay resolutions greater than 10ns. (Pesor 1990) Also, since the delay is not externally triggered, the start of the delay can be in error by up to one clock cycle.

Shift register based delays (Figure 7) consist of a series of memory cells connected so that data from one cell is shifted to the next cell when a clock pulse is

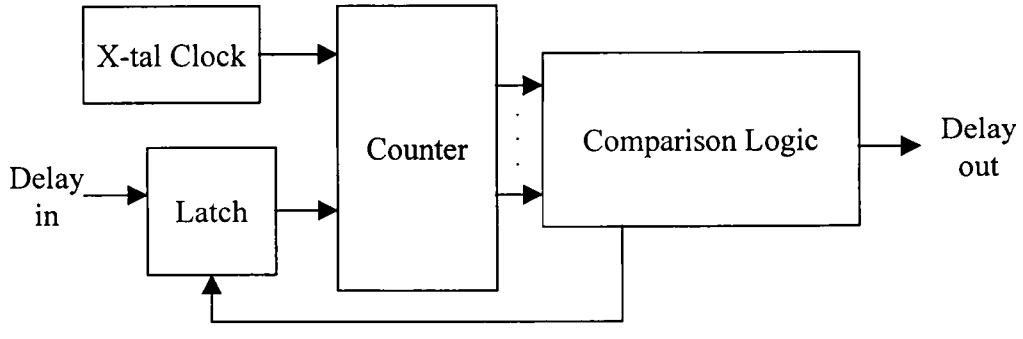


Figure 6: Counter Based Delay Block Diagram

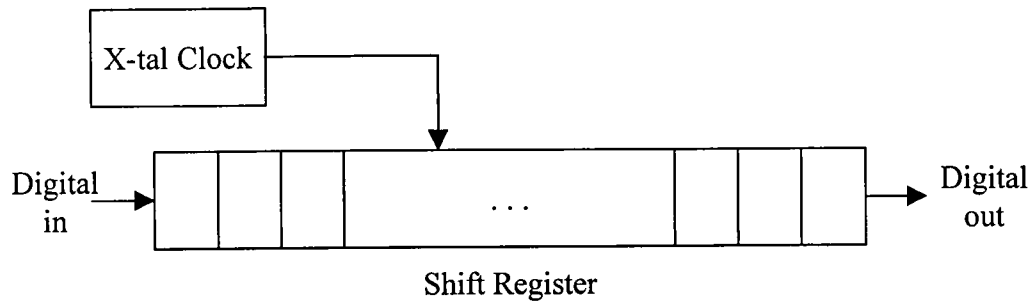


Figure 7: Shift Register Based Delay Block Diagram

applied. The memory cells can be an arbitrary number of bits wide (i.e. a 16 bit word could be delayed rather than just one bit) making this type of delay more flexible than a single bit delay. The shift register can be used in at least two different ways. The data can be shifted through the register itself (Dejhan 1990) or the register can be used to sequentially select memory addresses in which the data is stored and then read back after the pre-determined number of clock cycles (Sarkar 1993). This type of delay is also typically limited to a step size of greater than 10ns (Pesor 1990) and is not externally triggered.

Charge Coupled Device (CCD) based delays (Figure 8) are very similar to the shift register based delays in that data is sequentially shifted from the input through multiple memory position to the output. CCDs have the advantage that the data is not limited to digital values but may be sampled analog data.

1.2.2 Analog Delays

Analog delays are typically asynchronous devices that are externally triggered. This type of delay includes ramp and comparator delays and switched path delays.

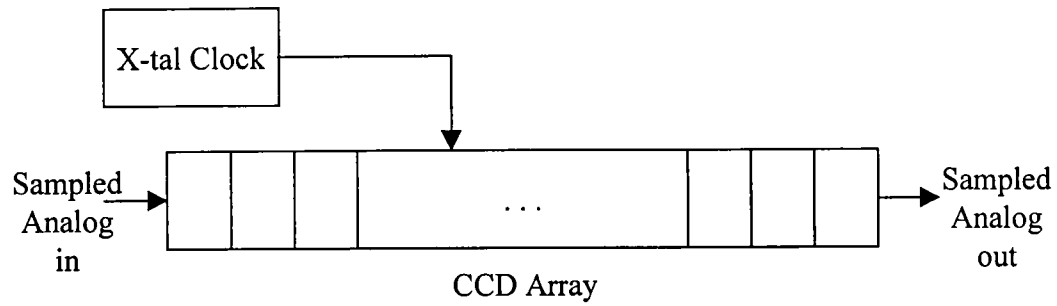


Figure 8: CCD Based Delay Block Diagram

Ramp and comparator delays (Figure 9) utilize a linear voltage ramp that begins at a preset initial value when the delay is triggered. The output is simply a comparator that fires when the ramp voltage is equal to the reference voltage (Feldman 1991). Variability is accomplished by changing the reference voltage or by changing the charging rate of the voltage ramp. This type of delay can be made to produce delay steps of less than 10ps (Feldman 1991). Dead time is a major problem in ramp and comparator delays since they can not be retriggered until after a set period of time has elapsed. This "dead" time is equal to the delay time plus a short recovery time.

Switched path delays (Figure 10) typically use passive LC delay elements and are varied by switching the signal path through or around a given element. This type

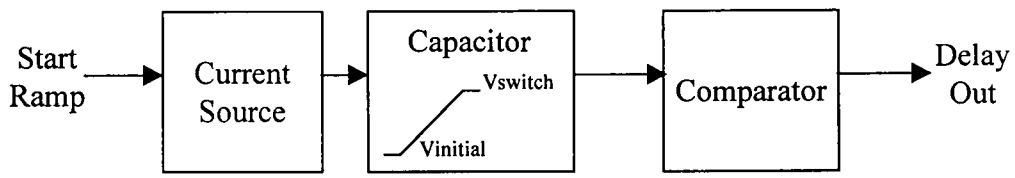


Figure 9: Ramp and Comparator Delay Block Diagram

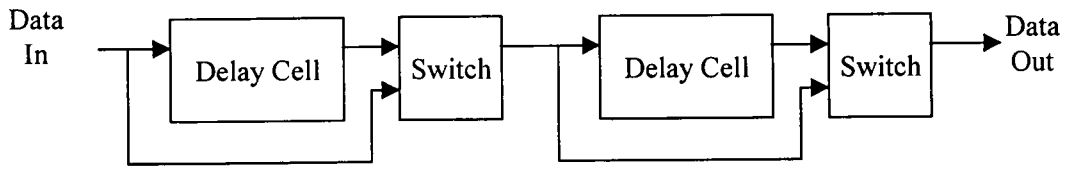


Figure 10: Switched Path Delay Block Diagram

of delay is extremely stable and can be used for small step sizes. Unfortunately, LC delay elements usually require a large amount of chip area and are not available in standard CMOS processes.

1.2.3 Selected Topology

Since the NWIS timing information is asynchronous data, the digitally generated delays are inadequate and an analog-based delay is needed. The requirement that the delay be implemented in a CMOS technology eliminates the LC type of delay and suggests that a ramp and comparator type of delay should be used. However, ramp and comparator delays have an associated dead time. This dead time could result in the loss of a large number of physics events and thus must be minimized.

Paulus and Mihalczo suggest an improved CMOS delay in ORNL ERID 0027 (patent pending). This improved delay is a system in which multiple variable delay lines are placed in parallel channels and a circular shift register switches the input to a new delay channel for each pulse, thus greatly reducing the dead time (Figure 11). The number of channels required will depend on the desired delay time and the

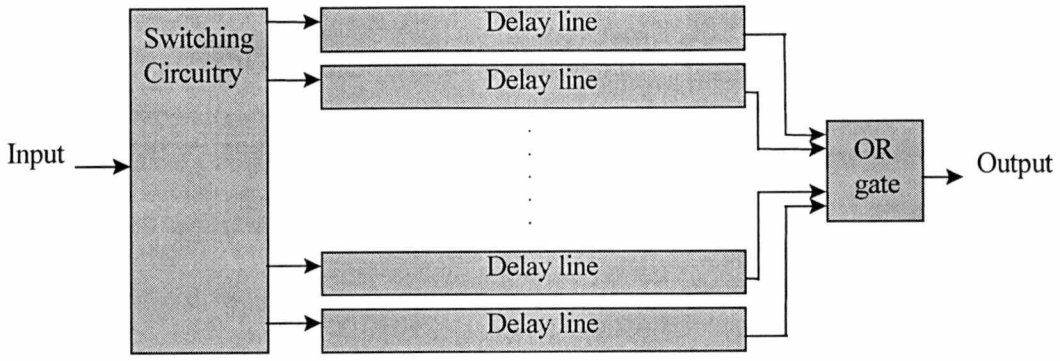


Figure 11: Dead Time Reduction Circuit

allowable dead time. A large number of parallel channel (> 1000) could be used to achieve almost arbitrarily small dead times.

1.3 Project Overview

The objective of this thesis project is the development of a CMOS based delay with a low dead time. The new NWIS delay should meet the following specifications:

500ns maximum delay, adjustable in 100ps steps

Jitter ≤ 50ps FWHM

Temperature coefficient < 150 ppm/ °C

Input pulse width 2ns-3ns

Compatible with 200MHz throughput (5ns between pulses).

Walk in the delay is not a major concern since the signal amplitude is constant.

This document is organized as follows:

Chapter 2 gives a basic description of the delay system,

Chapter 3 gives a detailed analysis of the basic delay element,

Chapter 4 gives simulation and layout details,

Chapter 5 gives the experimental results,

Chapter 6 is the conclusion.

Chapter 2 Delay System Description

2.1 System overview

In order to test the parallel channel concept, a 16-channel prototype delay system (Figure 12) was developed. The prototype consists of 16 parallel coarse-adjust delay channels, a fine-adjust delay element, and switching and pulse conditioning circuitry. Each of the 16 channels is a switched path delay in which delay cells are switched into or out of the signal path. All of the delay cells are based on a basic delay element whose propagation delay is feedback stabilized. This feedback stabilization compensates for temperature and device variations, and is accomplished using a Phase Locked Loop (PLL) to establish the bias voltages for the delay elements. The signal path is sequentially directed through the 16 parallel channels by a circular shift register and the 16 outputs are OR-ed back together before

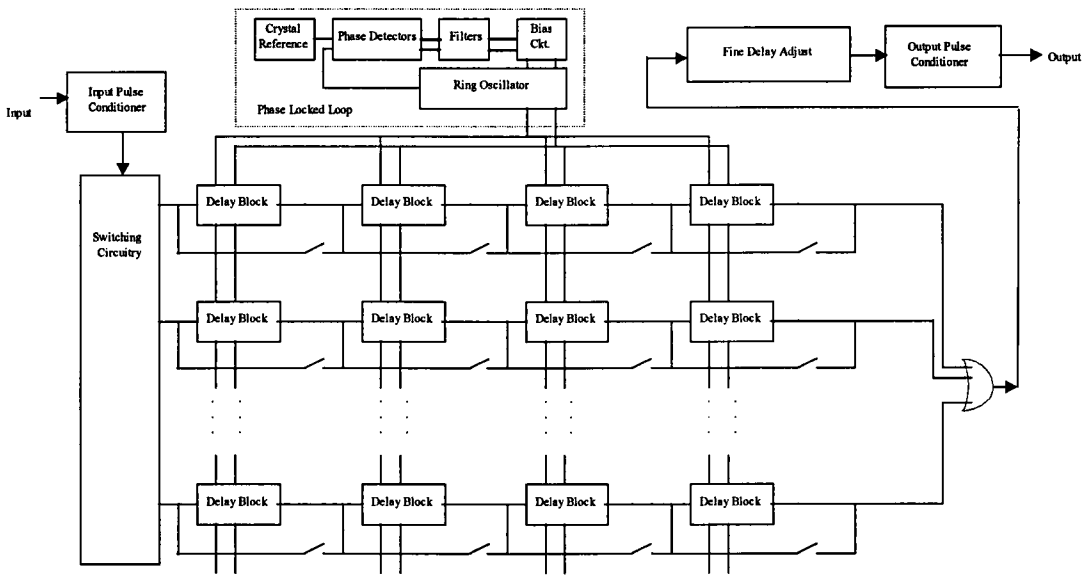


Figure 12: Prototype Delay System Block Diagram

going though the fine-adjust element to the output circuitry. The fine delay adjust cell is a modified basic delay element in which the propagation delay can be varied in sub-nanosecond steps. Each of the system elements will be discussed in more detail below.

The configuration used in the prototype should have a throughput of approximately 14MHz compared to a throughput of approximately 1.8MHz for an equivalent non-parallel delay. The throughput could be increased to approximately 25MHz by duplicating the fine adjust element and moving it into the parallel path architecture. This was not done in the prototype so that the properties of the fine adjust delay element could be evaluated without the potential of perturbations caused by channel to channel cross talk.

2.2 Starved inverter basic delay element

The basic delay element (Figure 13) is a variation of the ramp and comparator type of delay that is composed of a current starved CMOS inverter (Christiansen

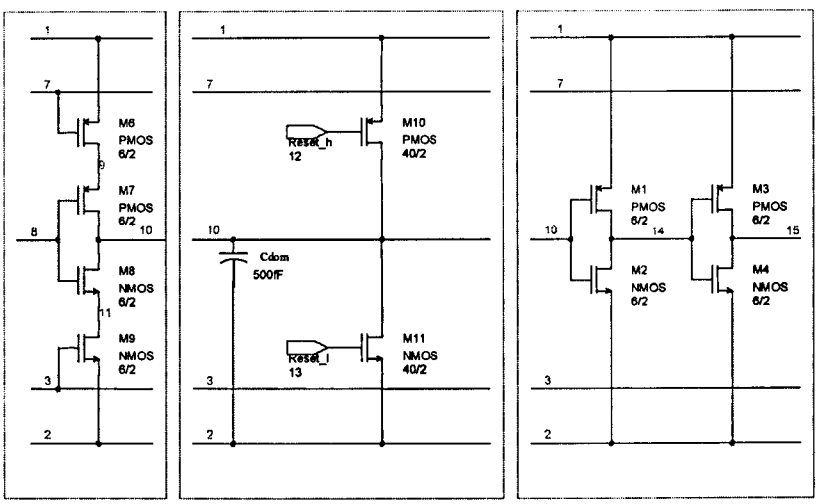


Figure 13: Starved Inverter Basic Delay Element

1995), a dominant node capacitance, and an output buffer. The current source for the voltage ramp in the basic delay element is a starved CMOS inverter (M6-M9). The charging current is set by simple current mirrors (M6 and M9) placed on the sources of the transistors comprising the inverter. The bias voltages and thus the currents in M6 and M9 are set by the Phase Locked Loop (PLL) bias control circuit (discussed below). When the voltage at Node 8 is a logical 1 (V(8) = 5V) the simple current mirror formed by M9 is active and current flows through M8 and M9. When the voltage at Node 8 is a logical 0 (V(8) = 0) the simple current mirror formed by M6 is active and current flows through M6 and M7.

The transistors in the starved inverter are designed to minimize the capacitance at nodes 9 and 11, since charge storage at these nodes introduces non-linearity in the voltage ramp when the inverter switches. This phenomenon is described in detail in Chapter 3.

Depending upon the logical input at Node 8, the starved inverter either charges or discharges C_{dom} (a nominally 500fF poly-poly capacitor). The ramp voltage at Node 10 is given to first order by

$$v_{10}(t) = v_{10}(0) + \frac{i}{C_{dom}} t$$

where $v_{10}(0)$ is the initial voltage at Node 10 , i is the charging current, and C_{dom} is the dominant node capacitance. Transistors M10 and M11 rapidly charge or discharge C_{dom} when the delay element is reset.

The output of the delay element is a buffer consisting of two CMOS inverters

in series that are designed so that their transition points are at approximately 2.5V. Since the switch point of the buffer is highly dependent on device parameters, the use of a comparator was explored in a previous prototype. By using a differential input comparator the switch point can be set by the ratio of two resistors which is reasonably device independent. It was determined that the required area and bias current for a comparator with sufficient speed was impractical due to the large number of buffers needed in the system.

2.3 Phase Locked Loop Bias Control

A Phase Locked Loop (PLL) bias circuit is used to set the bias levels for the basic delay current sources. As shown in Figure 14, the PLL is composed of two Z-state phase-frequency detectors (Wolaver 1991), two passive low-pass filters, a differential pair bias circuit, and a ring oscillator. The two phase detector outputs are of opposite polarity so that differential operation may be used to reduce common mode pickup on the control voltage nodes.

The Z-state digital phase-frequency detectors (Figure 15) operate as charge

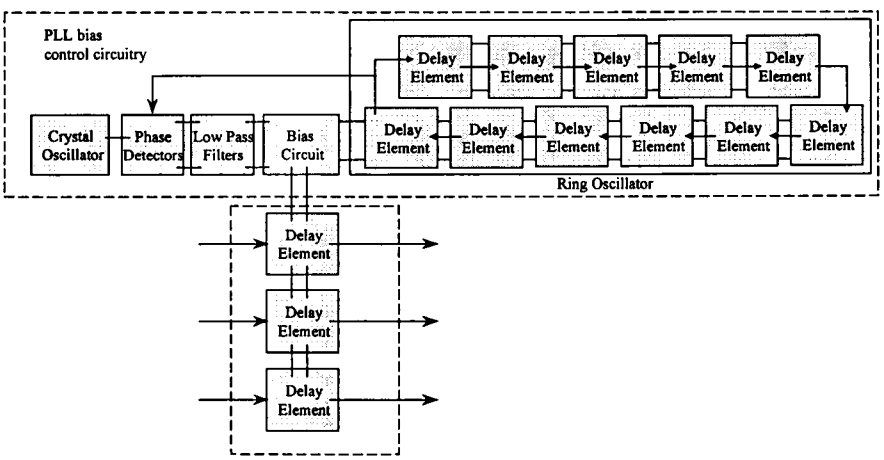


Figure 14: PLL Block Diagram

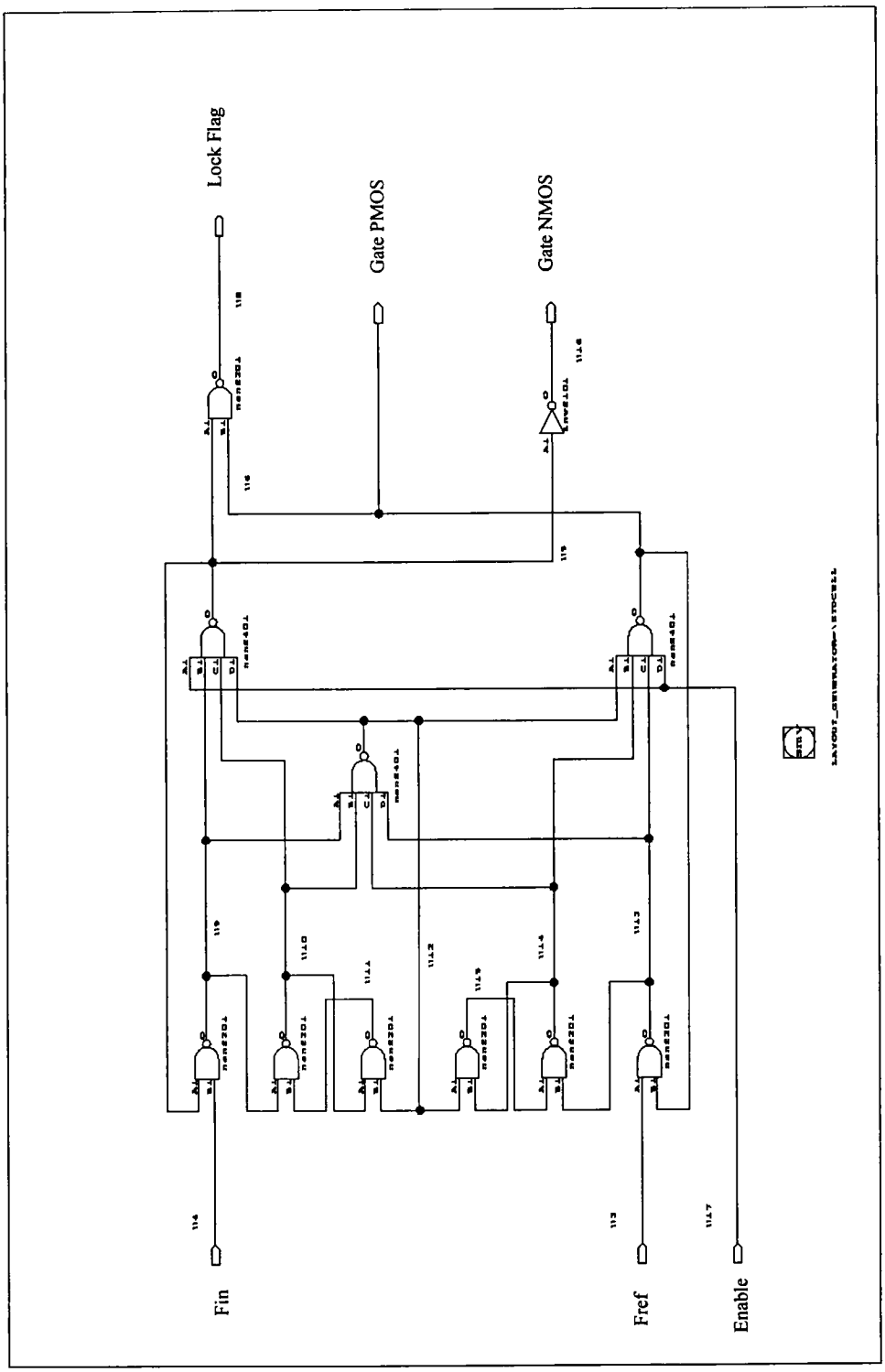


Figure 15: Phase-Frequency Detector Schematic

pumps which are active only when the input signal and reference signal are out of phase (or are of different frequency). When the signals are out of phase, the phase detectors pump charge into or out of the low-pass filters (which act as integrators), thus changing the control voltages applied to the voltage controlled oscillator (VCO) and bringing the VCO's output signal into lock with the reference. Once lock is achieved, the charge pumps are no longer active and the outputs of the phase detectors are in a high impedance state. (Johns 1997)

The low pass (LP) filters were implemented off chip using a Resistor-Capacitor (RC) configuration (Figure 16). Since the filters are connected to charge pump type phase detectors, they operate as integrators. The time constants of the filters were chosen to be large (1ms) since the reference frequency is static and a low phase noise was desired.

The filtered control voltages generated by the phase detectors and LP filters are used to switch the tail current of a differential pair (M8-M9 of Figure 17) into or out of an n-channel reference diode (M13). This diode-connected, n-channel transistor generates a reference gate voltage for the n-channel starving transistors (M9

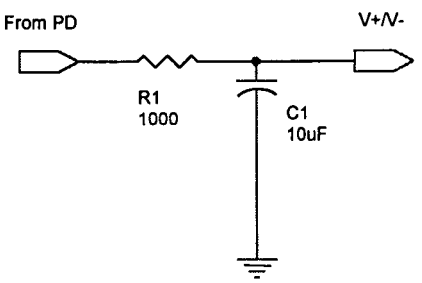


Figure 16: Low Pass Filter Schematic

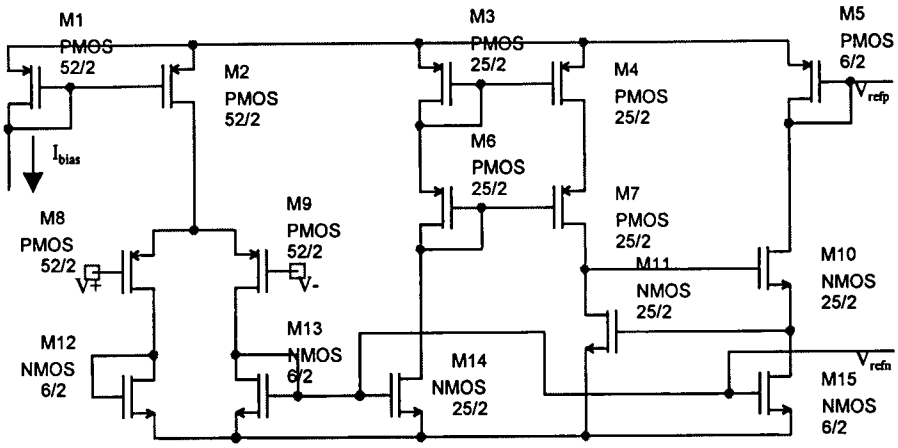


Figure 17: Differential Pair Bias Control Circuit

of Figure 13) in the delay elements and for the regulated cascode current mirror (M3, M4, M6, M7, M10, M11, M14, M15) which biases the p-channel reference diode (M5). The p-channel diode produces the reference gate voltage for the p-channel starving transistors (M6 of Figure 13) in the delay elements.

As shown in Figure 18, the ring oscillator is composed of eleven basic delay elements. The Ring oscillator combined with the differential pair bias circuit produces a Voltage Controlled Oscillator (VCO). By locking the output signal of the VCO to the signal generated by a crystal reference, a stable ring oscillator output frequency is achieved. Since the period of the ring oscillator output signal is the reciprocal of the output frequency, a stable output frequency means a stable output period. The period of oscillation for a ring oscillator is equal to twice the delay around the ring, thus a stable output period results in a stable average delay through the basic delay elements that make up the ring. The basic delay elements in the delay lines are exact copies of the delay elements in the ring and are supplied the same bias voltages, thus their delay is also set to a stable value (Paulus 1998).

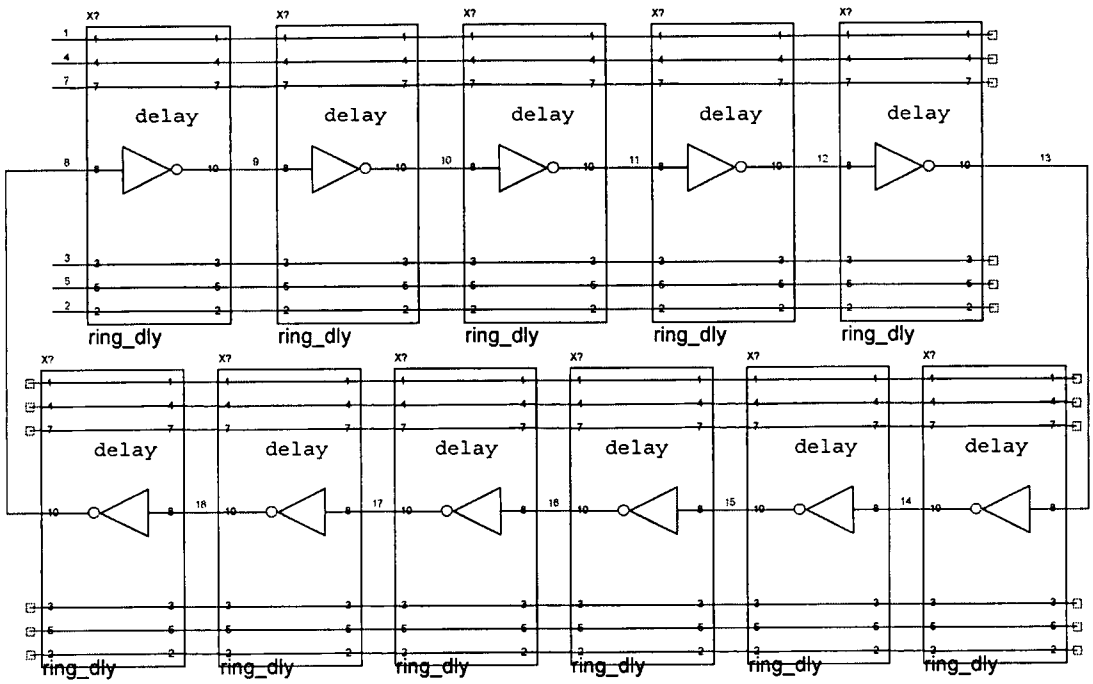


Figure 18: Ring Oscillator Block Diagram

2.4 Adjustable Delays

Delay adjustability is accomplished using a two-tiered scheme. The first adjustment scheme provides coarse adjustability and the second adjustment scheme provides fine adjustability.

The coarse adjustment scheme switches various delay cells into or out of the signal path (Figure 19). The cells have delays that are binarily weighted multiples of the 24ns delay provided by the basic delay element. The 1x delay cell is composed of an elementary delay element in series with an inverter. The 2x, 4x, and 8x cells are 2, 4, and 8 basic delay elements in series, respectively. All of the delay cells are non-inverting so that switching the cell into the circuit does not result in an inversion.

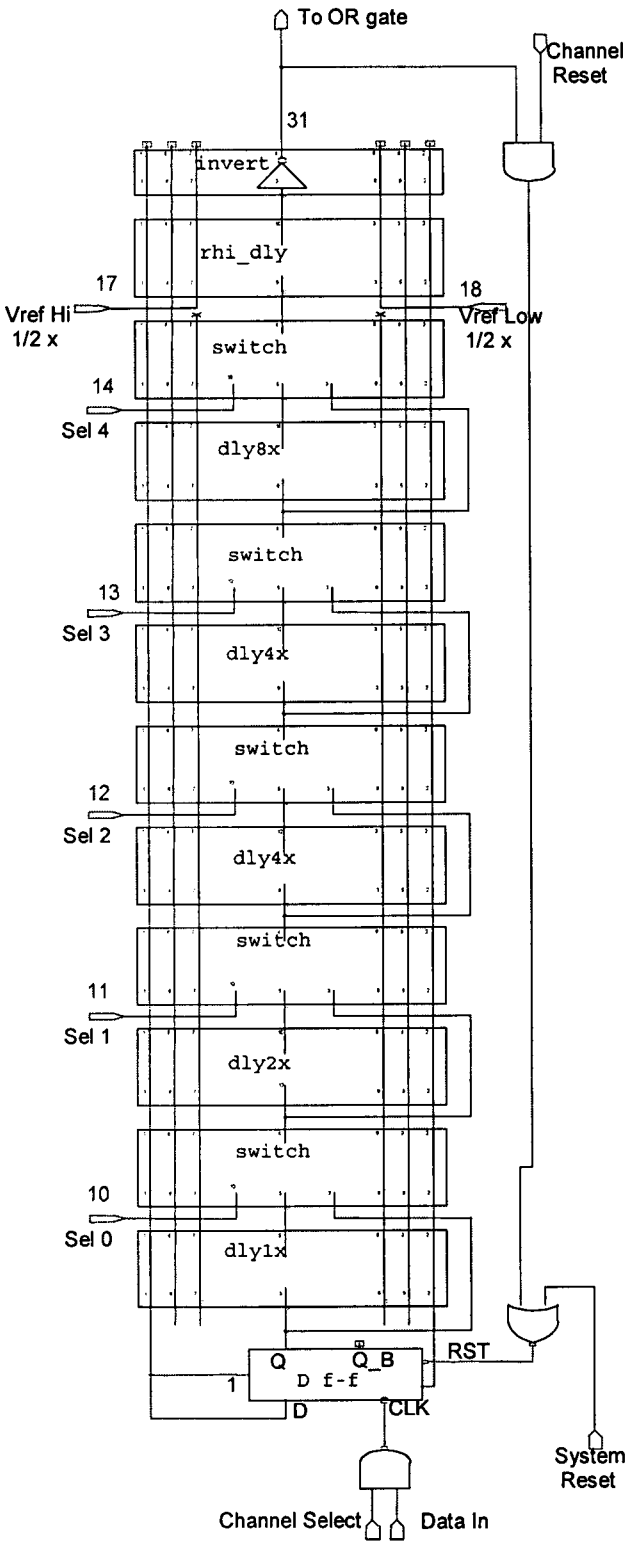


Figure 19: Coarse Adjust Delay Channel

Analog switches are used to switch the signal path either through the delay cells or around them (Figure 20). The bypass path has a dummy delay element connected to it so that the load seen by the preceding delay element is approximately the same when the current delay element is bypassed as when it is in the signal path.

Fine adjustment is accomplished by scaling the reference current for the starving mirrors on two elementary delay elements. The current in the first fine adjust delay element can be switched from 1 times the normal current to 2 times the normal current, resulting in a delay change equal to ½ of the normal elementary delay (approximately 12ns). The current in the second fine adjust delay element can be switched from 1 times the normal current up to 2 times the normal current in 256 binarily weighted steps by means of a switchable current mirror. The switchable

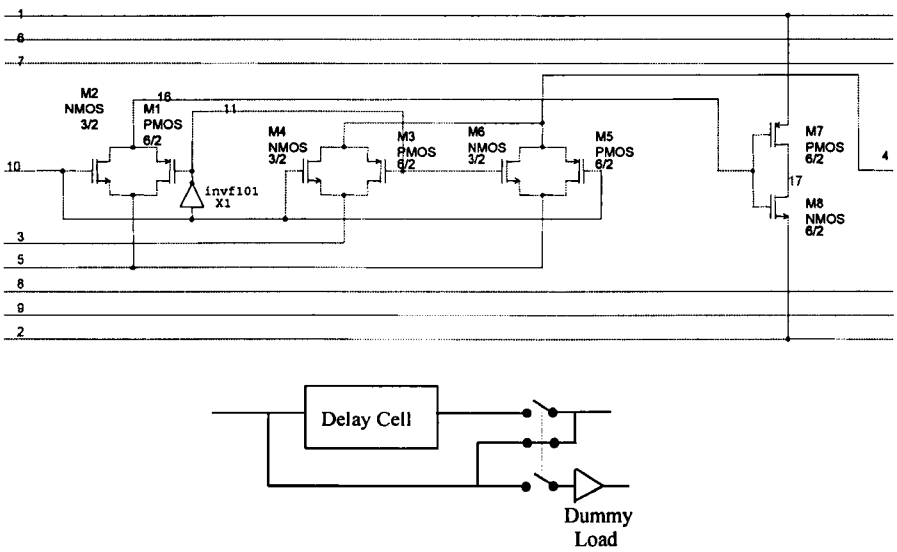


Figure 20: Switch Diagram and Schematic

mirror is composed of 9 regulated cascode current mirrors (Geiger 1990) with n-channel transistors used to turn the separate mirrors on or off (Figure 21). The reference diode has a multiplicity of 256 (256 minimum size transistors connected in parallel). The largest mirror transistor also has a multiplicity of 256 and is always turned on; thus, the minimum output current of the mirror is equal to the reference current. The other 8 mirror transistors are binarily weighted with multiplicities from 1 to 128 and can be switched on or off to control the output current.

2.5 Parallel Switching and Output Circuitry

The delay signal path is sequentially directed through the 16 parallel channels by a circular shift register and the outputs are recombined with an OR gate.

The circular shift register (Figure 22) is made of sixteen D flip-flops with the D input of each flip-flop connected to the Q output of the previous flip-flop. The

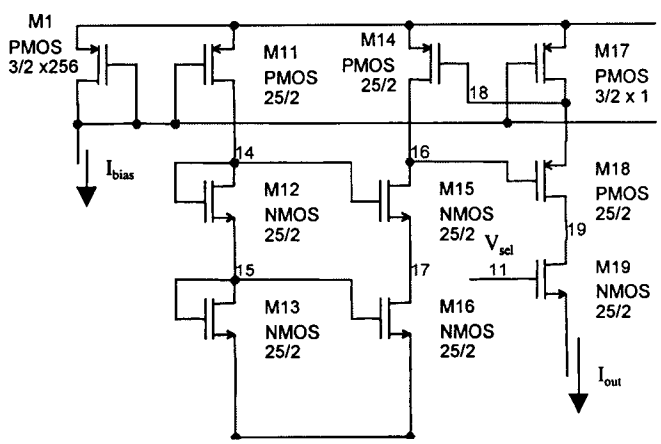


Figure 21: Regulated Cascode Current Mirror Schematic

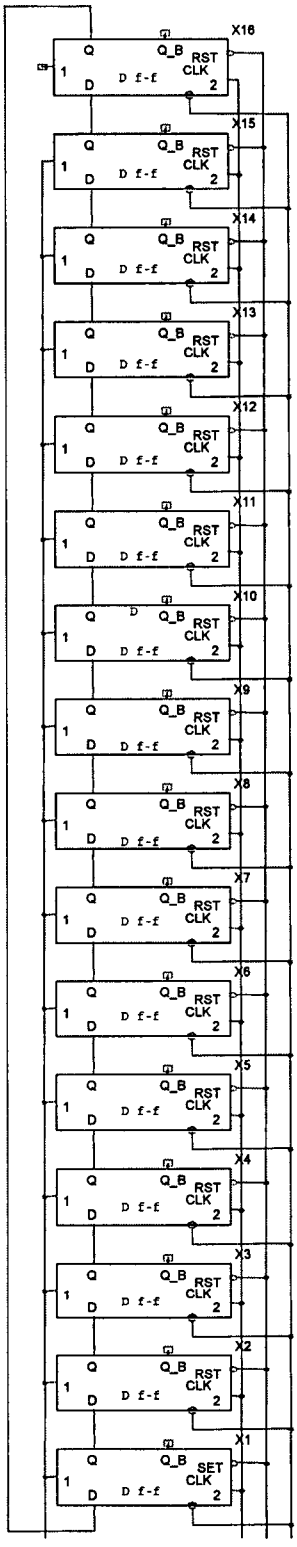


Figure 22: Circular Shift Register

clocks are connected in parallel so that the data is shifted in a circular fashion when a clock edge is detected. The set node of the first flip-flop and the reset nodes of the rest of the flip-flops are also connected in parallel, thus the register resets into a state with only the first flip-flop set. A falling edge on the clock input causes the logic '1' to be shifted to the next position in the register. The Q outputs of the flip-flops are used to select the active delay channel (a logic '1' indicates that the channel is active).

The outputs of the parallel channels are recombined by an OR gate. This 16-input OR is composed of four 4-input NOR gates and one 4-input NAND gate (Figure 23).

The pulse width of the input and output signals are set using an edge sensitive one-shot. The one-shots are composed of a D flip-flop with an elementary delay element providing feedback from the Q output back to reset (Figure 24).

The signal produced by the input one-shot is routed through buffers to supply the drive needed for a 16-gate fan out for the barrel register clock and for the delay line input flip-flops. The signals produced by the output one-shot and the ring oscillator are buffered to enable them to drive output pins.

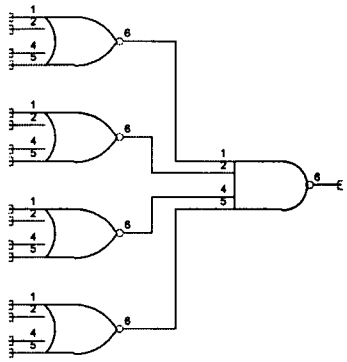


Figure 23: OR Gate Implementation

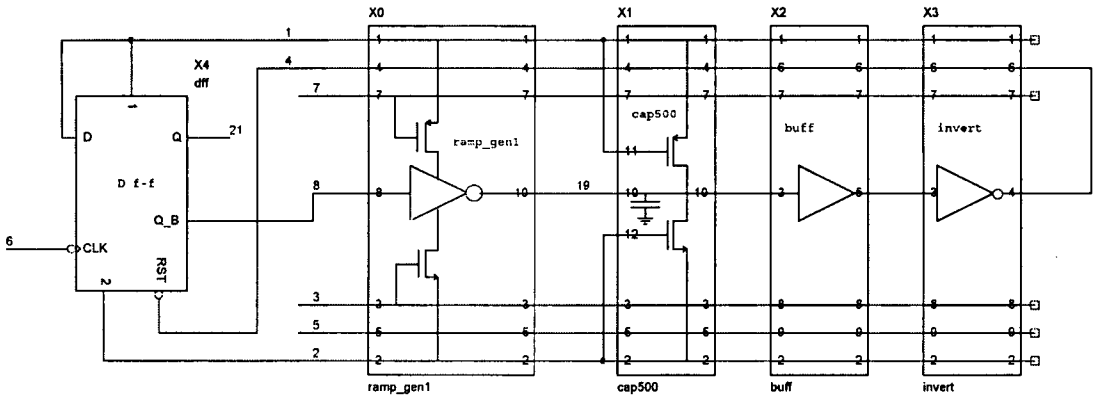


Figure 24: One-Shot Block Diagram

Chapter 3 Theoretical Analysis of the Basic Delay Element

3.1 Theory of Operation

The basic delay element is a variation of the ramp and comparator delay. Ramp and comparator delays use a linear voltage ramp that begins at some preset initial value and increases linearly over time after the delay is triggered. When the voltage ramp reaches the switch point of the comparator, the comparator fires producing the output pulse. The delay time for a linear ramp is given by,

$$T_d = \frac{\Delta V}{dv/dt} + T_{dcomp} \quad (1)$$

where, $\Delta V = V_{switch} - V_{initial}$ and T_{dcomp} is the comparator propagation delay. For a given circuit ΔV and T_{dcomp} are typically fixed, thus the only available means for adjusting the delay time is to change the slope of the voltage ramp (dv/dt). The slope of the voltage ramp is given by

$$dv/dt = \frac{i}{C_{dom}}, \quad (2)$$

where i is the charging current and C_{dom} is the dominant node capacitance. Thus, the expression for the delay becomes,

$$T_d = (\Delta V)\frac{C_{dom}}{i} + T_{dcomp}. \quad (3)$$

3.2 Delay element

The basic delay element (Figure 25) is a starved inverter based ramp and comparator delay. This section will investigate the properties of the charging current

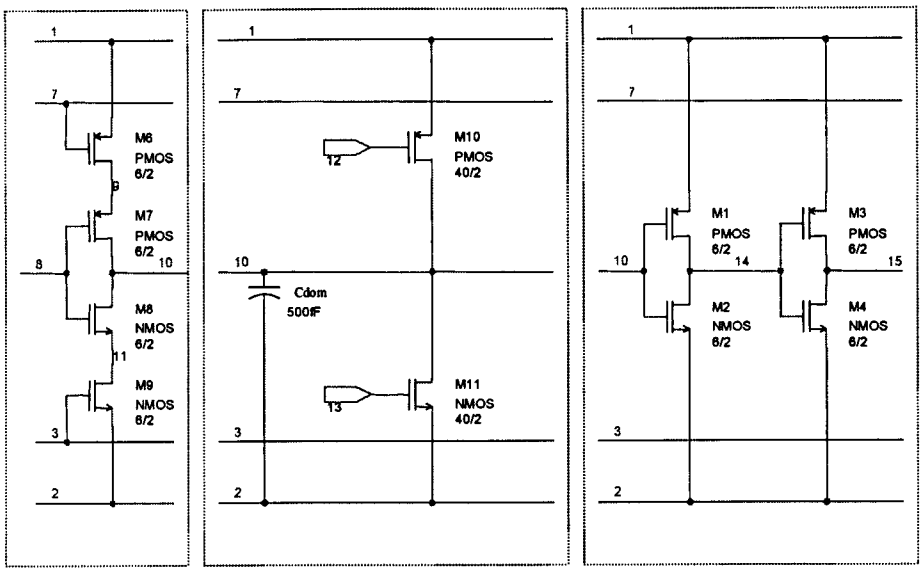


Figure 25: Basic Delay Element

as the starved inverter is switched and the starving mirror transistor moves from the ohmic region to equilibrium in the saturation region.

3.2.1 Starving Current

For the purposes of this calculation, the only transition that will be considered is the transition in which the voltage at node 10 (v_{10}) starts high and ramps down. However, the calculations for the opposite transition would be analogous. When the complete gradual channel approximation (Gray 1993) transistor modeling equations are used, the differential equations describing the voltages at nodes 10 and 11 are a second order system of nonlinear equations. In order to de-couple the equations, only the most simple transistor equations are used. These simple equations omit the body effect in M8 (Vsb on M9 is zero) and the channel length modulation in both transistors. Also, the parasitic capacitances coupling nodes 10 and 11 to the substrate are primarily depletion capacitances and are highly voltage dependent. Thus, to

simplify the solution of the differential equations, these capacitors are assumed to have a constant value equal to the largest value attained over the voltage range under consideration. A schematic of the simplified circuit used for the calculations is shown in Figure 26. All numerical calculations for the delay element will assume that the starving current is set to produce the basic delay time (i.e. 50uA charging current).

3.2.1.1 Charge injection

As the inverter (M7 and M8) switches, a small amount of charge is added to the dominant node (node 10) due to charge injection. This charge produces a positive voltage step of approximately

$$\begin{aligned}\Delta V &= V_{switch}(C_{gd7} + C_{gd8})/(C_{gd7} + C_{gd8} + C_{dom}) \\ &= 5(2.7fF + 2.7fF)/(2.7fF + 2.7fF + 500fF) = 53mV\end{aligned} \quad \textbf{(4)}$$

at Node 10 and a voltage step of approximately

$$\begin{aligned}\Delta V &= V_{switch}(C_{gs8})/(C_{gs8} + C_{sb8} + C_{db9} + C_{gd9}) \\ &= 5(2.7fF)/(2.7fF + 2.9fF + 2.9fF + 2.7fF) = 1.2V\end{aligned} \quad \textbf{(5)}$$

at Node 11. It will be assumed that this is an instantaneous transition so that $v_{10}(0) =$ 5.053V and $v_{11}(0) = 1.2$V.

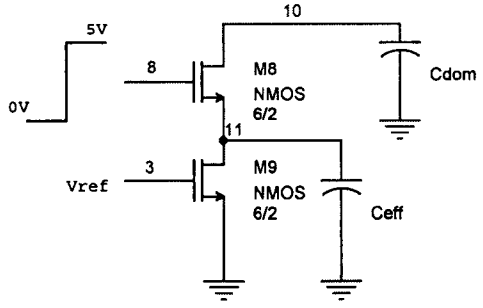


Figure 26: Simplified Schematic

3.2.1.2 Ohmic region with charge storage

For the circuit under consideration, the charge injection onto node 11 is sufficient to bring M9 out of the ohmic region almost immediately, however in order to keep this analysis general the equations for the ohmic region will still be developed with the assumption that $v_{11}(0) = 0$. The differential equation describing the voltage at node 11 (v_{11}) is

$$\frac{dv_{11}}{dt} = \frac{I_{D8} - I_{D9}}{C_{eff}} = \frac{k'\left(\frac{W}{L}\right)_8 \left[(5 - v_{11}) - v_t\right]^2 - k'\left(\frac{W}{L}\right)_9 \left[2(v_{ref} - v_t)v_{11} - v_{11}^2\right]}{C_{eff}}. \quad (6)$$

Let $X_8 = k'\left(\frac{W}{L}\right)_8$, and $X_9 = k'\left(\frac{W}{L}\right)_9$. Substituting these into (6) and collecting powers of v_{11} yields

$$\frac{dv_{11}}{dt} = \frac{1}{C_{eff}}\left\{(X_8 + X_9)v_{11}^2 + \left[2X_8(v_t - 5) - 2X_9(v_{ref} - v_t)\right]v_{11} + X_8(v_t - 5)^2\right\}, \quad (7)$$

which is of the form

$$\frac{dv_{11}}{dt} = \frac{1}{C_{eff}}\left\{cv_{11}^2 + bv_{11} + a\right\} \qquad \text{where,} \quad (8)$$

$$c = (X_8 + X_9), \quad (9)$$

$$b = \left[2X_8(v_t - 5) - 2X_9(v_{ref} - v_t)\right], \text{ and} \quad (10)$$

$$a = X_8(v_t - 5)^2. \quad (11)$$

(8) can be solved by separation of variables to yield

$$t + K_1 = C_{eff}\left(\frac{2}{\sqrt{q}}\right)\tan^{-1}\left(\frac{2cv_{11}+b}{\sqrt{q}}\right) \quad \text{, for } q>0 \tag{12}$$

or

$$t + K_2 = \left(\frac{C_{eff}}{\sqrt{-q}}\right)\ln\left(\frac{2cv_{11}+b-\sqrt{-q}}{2cv_{11}+b+\sqrt{-q}}\right) \quad \text{, for } q<0, \text{ where } q = 4ac - b^2. \tag{13}$$

Solving (12) for v_{11} yields

$$v_{11} = \frac{\sqrt{q}}{2c}\tan\left[\frac{\sqrt{q}}{2C_{eff}}(t+K_1)\right] - \frac{b}{2c} \tag{14}$$

and solving (13) for v_{11} yields

$$v_{11} = \frac{\left(b+\sqrt{-q}\right)Exp\left(\frac{\sqrt{-q}}{Ceff}(t+K_2)\right) - b + \sqrt{-q}}{2c\left(1 - Exp\left(\frac{\sqrt{-q}}{Ceff}(t+K_2)\right)\right)}. \tag{15}$$

Using AMI process data, numerical values for the constants (9) – (11) can be calculated giving

$$c = 206E\text{-}6A/V^2 \tag{16}$$

$$b = -1065E\text{-}6A/V \tag{17}$$

$$a = 2044E\text{-}6A \tag{18}$$

$$C_{eff} = 11.2fF \tag{19}$$

$$q = 4ac\text{-}b^2 = 0.550031E\text{-}6A^2/V^2 . \tag{20}$$

Since q > 0 in this region of operation, we can substitute (16) – (20) into (14) to obtain:

$$v_{11} = 1.8\tan[3.311E10(t + K_1)] + 2.585 \quad \textbf{(21)}$$

Using the initial condition $v_{11}(0) = 0$, K_1 is found to be –2.907E-11 thus

$$v_{11} = 1.8\tan[3.311E10(t - [2.907E-11])] + 2.585. \quad \textbf{(22)}$$

Using (12), the time at which M9 goes into saturation t_{sat} is found to be

$$t_{sat} = 4.742E-12.$$

Figure 27 shows a plot of v_{11} for $0 < t < t_{sat}$.

Now that v_{11} has been determined, the dominant node voltage (v_{10}) can be calculated for this region of operation. The differential equation describing v_{10} is

$$\frac{dv_{10}}{dt} = \frac{-k'\left(\frac{W}{L}\right)_8 [(5 - v_{11}) - v_t]^2}{C_{dom}} \quad \textbf{(23)}$$

Replacing v_{11} in (23) using (14) and simplifying yields

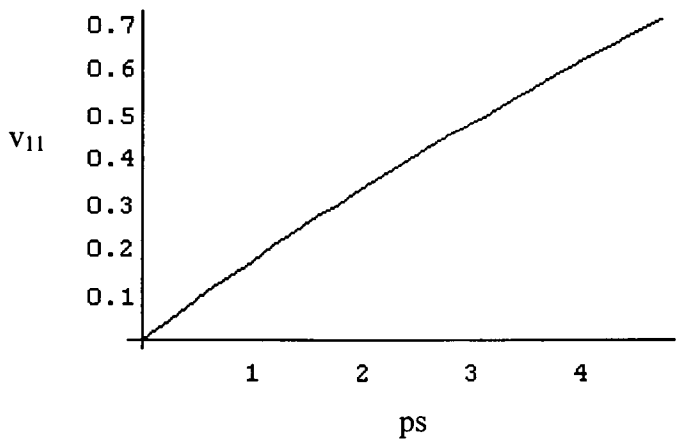


Figure 27: Plot of v_{11} for $0<t<t_{sat}$

$$\frac{dv_{10}}{dt} = \frac{-k'\left(\frac{W}{L}\right)_8\left[\left(5 - v_t + \frac{b}{2c}\right) - \frac{\sqrt{q}}{2c}\tan\left[\frac{\sqrt{q}}{2C_{eff}}(t + K_1)\right]\right]^2}{C_{dom}}. \quad \textbf{(24)}$$

(24) can be solved by separation of variables to give a solution of

$$v_{10} = \frac{-k'\left(\frac{W}{L}\right)_8}{C_{dom}}\left\{\begin{aligned}&\left[\left(5 - v_t + \frac{b}{2c}\right)^2 - \frac{q}{4c^2}\right]t + \left(10 - 2v_t + \frac{b}{c}\right)\left(\frac{C_{eff}}{c}\right)\log\left(\cos\left[\frac{\sqrt{q}}{2C_{eff}}(t + K_1)\right]\right)\\&+ \frac{\sqrt{q}C_{eff}}{2c^2}\tan\left[\frac{\sqrt{q}}{2C_{eff}}(t + K_1)\right] + Q\end{aligned}\right\}$$

(25)

Evaluating the constants results in

$$v_{10} = -2.064E8\left\{\begin{aligned}&0.23805t + 2.028E - 10\log(\cos[3.3107E10(t - 2.907\text{E-}11)])\\&+ 9.7864E - 11\tan[3.3107E10(t - 2.907\text{E-}11)] + Q\end{aligned}\right\} \quad \textbf{(26)}$$

Using the initial condition $v_{10}(0) = 5.053$V it is found that Q = -2.4228E-8, thus

$$v_{10} = -2.064E8\left\{\begin{aligned}&0.23805t + 2.028E - 10\log(\cos[3.3107E10(t - 2.907\text{E-}11)])\\&+ 9.7864E - 11\tan[3.3107E10(t - 2.907\text{E-}11)] - 2.4228\text{E-}8\end{aligned}\right\}$$

Figure 28 shows a plot of v_{10} for $0<t<t_{sat}$.

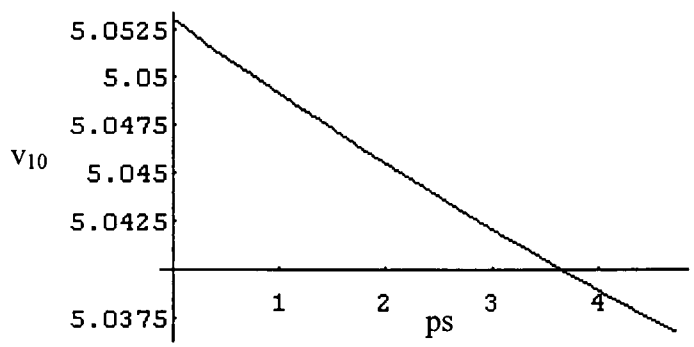


Figure 28: Plot of v_{10} for $0<t<t_{sat}$

3.2.1.3 Saturation region with charge storage

Once the starving transistor moves into the saturation region, the modeling equation for M8 changes and the new differential equation describing v_{11} is

$$\frac{dv_{11}}{dt} = \frac{I_{D8} - I_{D9}}{C_{eff}} = \frac{k'\left(\frac{W}{L}\right)_8 \left[(5 - v_{11}) - v_t\right]^2 - k'\left(\frac{W}{L}\right)_9 \left[v_{ref} - v_t\right]^2}{C_{eff}} \quad (27)$$

or

$$\frac{dv_{11}}{dt} = \frac{X_8\left[(5 - v_{11}) - v_t\right]^2 - X_9\left[v_{ref} - v_t\right]^2}{C_{eff}}. \quad (28)$$

Collecting powers of v_{11} yields

$$\frac{dv_{11}}{dt} = \frac{1}{C_{eff}}\left\{X_8 {v_{11}}^2 + 2X_8(v_t - 5)v_{11} + X_8(v_t - 5)^2 - X_9(v_{ref} - v_t)^2\right\}, \quad (29)$$

which is also of the form

$$\frac{dv_{11}}{dt} = \frac{1}{C_{eff}}\left\{c{v_{11}}^2 + bv_{11} + a\right\} \quad (30)$$

where,

$$c = X_8, \quad (31)$$

$$b = 2X_8(v_t - 5), \text{ and} \quad (32)$$

$$a = X_8(v_t - 5)^2 - X_9(v_{ref} - v_t)^2. \quad (33)$$

Using AMI process data, numerical values for these constants can be calculated.

$$c = 103.2E\text{-}6A/V^2 \quad (34)$$

$$b = -918.48E\text{-}6A/V \quad (35)$$

$$a = 1991.45E\text{-}6A \quad (36)$$

$$q = 4ac\text{-}b^2 = -2.154E\text{-}8A^2/V^2 \quad (37)$$

Since q<0 in this region of operation, we can substitute (34) – (37) into (10) to obtain:

$$v_{11} = \frac{(-7.717E-4)Exp((1.310E10)(t+K_2))+(1.065E-3)}{(2.064E-4)(1-Exp((1.310E10)(t+K_2)))} \quad (38)$$

Using the initial condition $v_{11}(t_{sat}) = 0.711$, K_2 is found to be 2.463E-11 thus

$$v_{11} = \frac{(-7.717E-4)Exp((1.310E10)(t+2.463E\text{-}11))+(1.065E-3)}{(2.064E-4)(1-Exp((1.310E10)(t+2.463E\text{-}11)))} \quad (39)$$

Figure 29 shows a plot of v_{11} for $t > t_{sat}$ and Figure 30 shows a plot of v_{11} over both regions of operation.

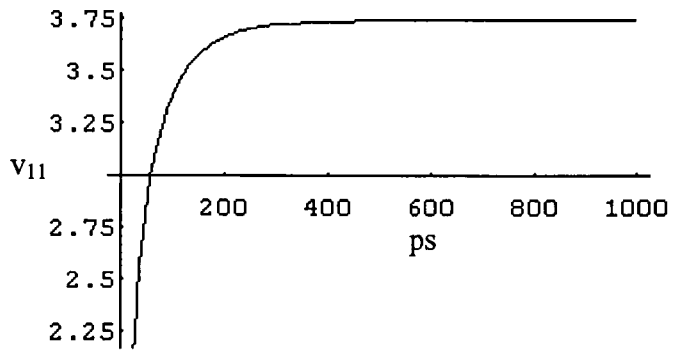


Figure 29: Plot of v_{11} $t>t_{sat}$

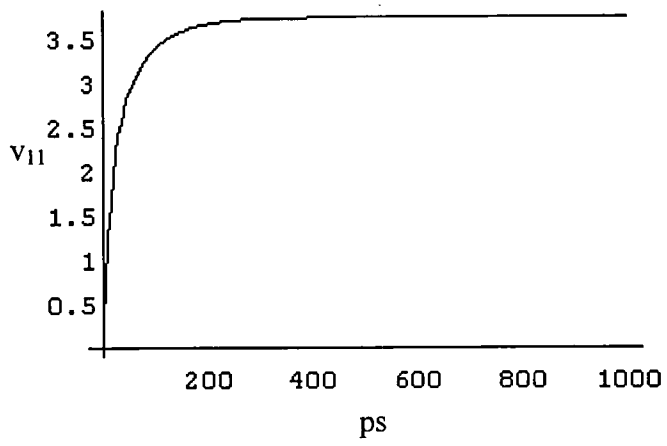


Figure 30: Plot of v_{11} for $t > 0$

Now that v_{11} has been determined for $t>t_{sat}$, the dominant node voltage (v_{10}) can be calculated for this region of operation. The differential equation describing v_{10} is

$$\frac{dv_{10}}{dt} = \frac{-k'\left(\frac{W}{L}\right)_8 \left[(5 - v_{11}) - v_t\right]^2}{C_{dom}} \qquad \textbf{(40)}$$

Replacing v_{11} in (40) using (15) yields

$$\frac{dv_{10}}{dt} = \frac{-k'\left(\frac{W}{L}\right)_8}{C_{dom}} \left[5 - v_t - \left(\frac{\left(b + \sqrt{-q}\right) Exp\left(\frac{\sqrt{-q}}{Ceff}(t + K_2)\right) - b + \sqrt{-q}}{2c\left(1 - Exp\left(\frac{\sqrt{-q}}{Ceff}(t + K_2)\right)\right)} \right) \right]^2 \qquad \textbf{(41)}$$

(41) can be solved by separation of variables to give a solution of

$$v_{10} = \frac{-k'\left(\frac{W}{L}\right)_8}{C_{dom}} \left(\begin{array}{l} \dfrac{qCeff}{\sqrt{-q}\left(e^{\left[\frac{\sqrt{-q}}{Ceff}(t+K_2)\right]}-1\right)} + \\ \dfrac{t\left[(b+10c)^2 - 2\sqrt{-q}(b+10c) - q - 4cv_t\left(b+10c-\sqrt{-q}\right) + 4c^2 v_t{}^2\right]}{4} \\ + Ceff(b+10c-2cv_t)\ln\left(1-e^{\left[\frac{\sqrt{-q}}{Ceff}(t+K_2)\right]}\right) \end{array} \right) + Q \tag{42}$$

Evaluating the constants results in

$$v_{10} = \frac{3.18523E-2}{-1+1.38087Exp[(1.31025E10)t]} - (1.04336E8)t + Q \tag{43}$$

using the initial condition $v_{10}(t_{sat})$ = 5.0367V equation 38 becomes

$$v_{10} = \frac{3.18523E-2}{-1+1.38087Exp[(1.31025E10)t]} - (1.04336E8)t + 4.96937. \tag{44}$$

Figure 31 shows a plot of v_{10} for $t > t_{sat}$ and Figure 32 shows a plot of v_{10} over both regions of operation.

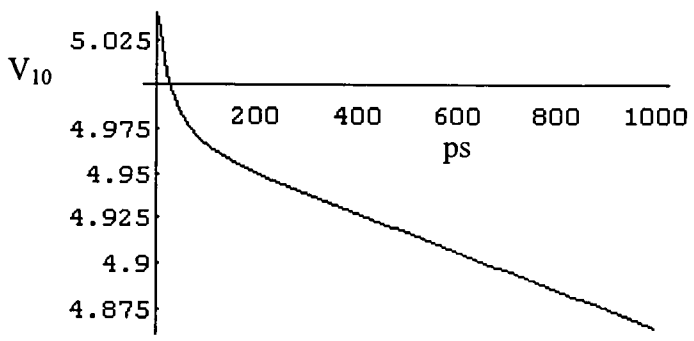


Figure 31: Plot of v_{10} for $t > t_{sat}$

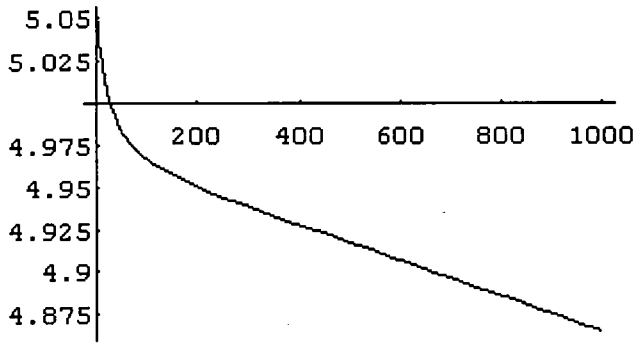


Figure 32: Plot of v_{10} for $t > 0$

By comparing Figure 32 with the SPICE plot shown in Figure 33 (See source file in the Appendix) it can be seen that the simplified model used describes the actual behavior of the circuit reasonably well.

3.2.1.4 Saturation region in equilibrium

Once v_{11} reaches equilibrium, the starving mirror transistor (M8) operates as a constant current source that sinks all of the current flowing through M9. In this state dv_{10}/dt is constant and v_{10} is a linear ramp.

3.2.2 Observations

The calculations in section 3.2.1.3 suggest the dominant source of non-linearity (which results in an effective offset voltage) in the voltage ramp at Node 10 is the charge storage at Node 11. Thus care was taken in the layout to minimize the stray capacitance at this node. It was seen in section 3.2.1.1 that for this particular design, charge injection had little effect on the initial dominant node voltage ($v_{10}[0]$).

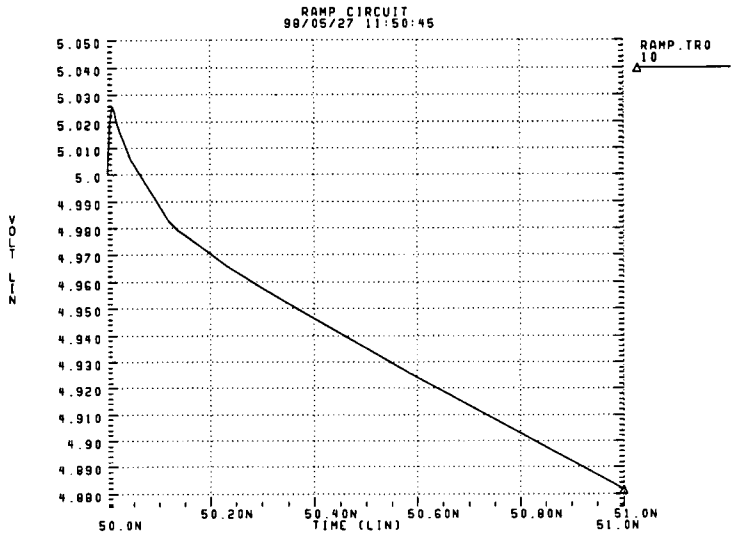


Figure 33: SPICE Plot of v_{10}

Also, the charge injection actually improved the linearity of the voltage ramp by rapidly charging the stray capacitance at Node 11 and thus bringing M9 out of the ohmic region almost immediately. This suggests that it might be advantageous to add a small amount of capacitance in parallel with C_{gs8} in order to enhance the charge injection at node 11. If the charge injection were increased so that v_{11} would reach its equilibrium value almost immediately, the non-linearity caused by the charge storage could be greatly reduced. The charge required for Ceff would then be supplied by the charge injection instead of being removed from Cdom.

Chapter 4 Layout and Simulation

The main purpose of the prototype was to test the dead time reduction architecture, the delay adjustment scheme, and the feedback stabilization to see if these techniques are compatible with the desired delay specifications. The specifications are:

500ns maximum delay, adjustable in 100ps steps

Jitter ≤ 50ps FWHM

Temperature instability of at most 150 ppm/° C

Input Pulse Width 2-3 ns

200 MHz throughput (the prototype has only 16 channels and thus is designed for a throughput of approximately 14MHz)

In the design and layout of the various components of the prototype system (Figure 12, page 12) the above specifications were the determining factors for most of the design decisions.

4.1 Tools and Technology

The Prototype System was fabricated using the 1.2u AMI ABN process provided by MOSIS. This process is a standard n-well CMOS process with two polysilicon and two metal layers. The process offers a NPN device which was not used in this project. Some of the process parameters provided by MOSIS for the run in which the prototype chip was fabricated are given in Figure 34.

PROCESS: American Microsystems, Inc. 1.2 micron ABN.

RUN: N7AB SUBMISSION DATE: 10/22/97

MINIMUM TRANSISTOR PARAMETERS W/L=1.8/1.2

PARAMETER	N-CHANNEL	P-CHANNEL	UNITS
Vth	0.55	-1.05	Volts
Delta length (L_eff = L_drawn-DL)	0.13	-0.11	microns
Delta width (W_eff = W_drawn-DW)	1.10	1.19	microns
K' (Uo*Cox/2)	34.4	-11.5	uA/V^2

PROCESS PARAMETERS

PARAMETER.	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Sheet Resistance	53.5	75.8	30.7	21.2	0.05	0.03	1513	ohms/sq
Width Variation (measured - drawn)	-0.75	-0.89	-0.03	0.35	0.32	-0.08		microns
Contact Res.	65.9	35.9	23.8	15.2		0.05		ohms

Gate Oxide Thickness 306 angstrom

CAPACITANCE PARAMETERS

PARAMETER	N+ACTV	P+ACTV	POLY	POLY2	METAL1	METAL2	UNITS
Area (substrate)	290	290	38		21	13	aF/um^2
Area (poly)				611	45	23	aF/um^2
Area (poly2)					45		aF/um^2
Area (metal1)						41	aF/um^2
Area (N+active)			1129	718	49	25	aF/um^2
Area (P+active)			1113	713			aF/um^2
Fringe (substrate)	338						aF/um

Ring Oscillator Freq.
MOSIS (31-stage,5V) 67.65 MHz

Figure 34: MOSIS PARAMETRIC TEST RESULTS

The majority of the circuit was laid out (Figure 35) using the public domain cad tool Magic (Mayo 1990) running on a Sun workstation. The SPICE netlist extractions were performed using a modified version of the extraction utility provided with Magic Release 6.3.

Some of the digital circuitry was laid out using View Logic's schematic capture tool to map the design to standard cells, followed by automatic placement and routing done with the Lager IV 2.0 software package. These software packages generated a cell that could be opened and modified using Magic.

Spice simulation was performed using HSPICE Release 96.3.1 (Meta-Software 1996) on a Sun workstation. The device models used for the simulation are HSPICE Level 13 models from previous AMI runs provided by MOSIS.

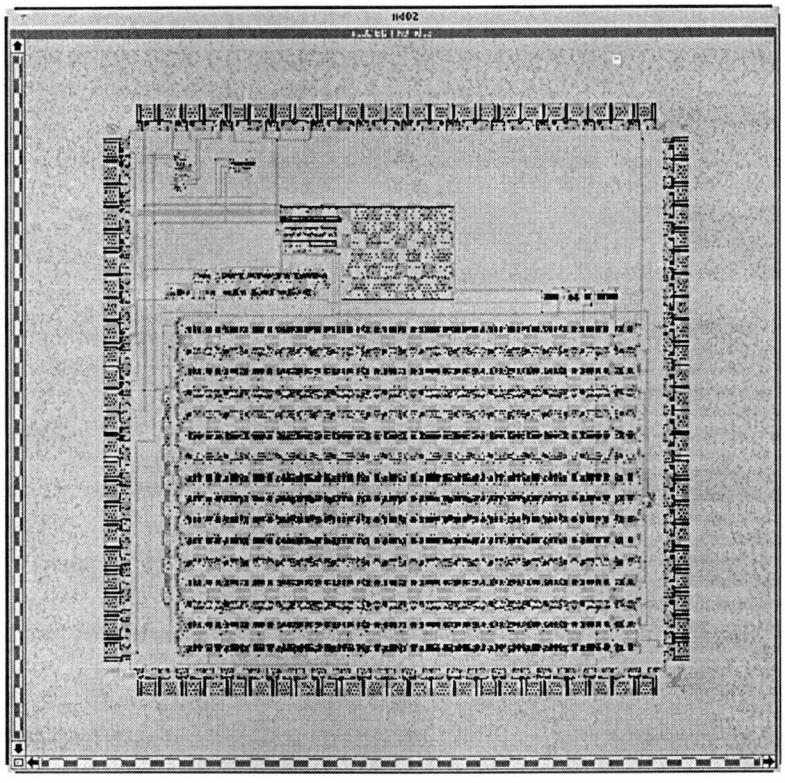


Figure 35: Magic Layout of Prototype Chip

4.2 Basic Cell Design

4.2.1 Basic Delay Element

The principal design issues for the basic delay element are linearity, matching and jitter. Non-linearity in the basic delay element has little impact on the coarse adjust delay circuitry but can have a large impact on the fine adjust delay circuitry. The coarse adjust delays are simply copies of the basic delay elements used to created the ring oscillator, thus any non-linearity in the coarse adjust delay elements is also in the ring oscillator elements and would be compensated for by the feedback in the PLL. Since the non-linearity produces an effective initial offset voltage at the dominant node, the starving current will be set at a lower than expected value in order to maintain the correct propagation delay. Thus, due to the PLL control, the coarse adjust delay elements will still have the correct delay values. However, the reduced starving current will greatly affect the step sizes produced by the fine adjust delay element since these steps are obtained by variable scaling of the starving current.

Matching between all of the delay elements is critical since the delay elements in the delay line operate open loop based on a bias that is set up in the PLL. If the delay elements in the delay lines are not well matched to the delay elements in the ring oscillator the feedback regulation scheme will be ineffective.

Jitter produced by the delay elements is expected to be the dominant source of jitter in the delay system. The total jitter contribution of all of the delay elements must be considerably less than the total jitter allowed for the system in order to accommodate other noise sources in the system such as phase noise in the PLL.

4.2.1.1 Linearity

Linearity is limited by two phenomena: charge storage at the source of M8 (Figure 36 A) and the finite output impedance of the starved inverter. Non-linearity produced by the charge storage issue discussed in Chapter 3 can be reduced by minimizing the capacitance at Nodes 9 and 11. Thus, the transistors making up the starved inverter (M6-M9 of Figure 36 B) were laid out using interdigitation so that the capacitance at nodes 9 and 11 is minimized while the W/L ratios of the transistors are as large as possible for this minimum capacitance.

The increased W/L ratios reduced the gate to source voltages of the transistors allowing transistors M8 and M9 (M6 and M7) to remain saturated for a larger swing of the ramp voltage (v_{I0}). While both of the active transistors (M8 and M9 or M6 and M7) are saturated, the starved inverter looks like a cascode current mirror and thus the output impedance is much higher than that of a simple mirror. Once the active transistor that is part of the inverter (M7 or M8) goes into the ohmic region this enhancement of the output impedance is lost and the starving mirror looks like a simple mirror in series with a resistor. Thus the reduced gate to source voltages produced by the interdigitation, help increase the linear region of the voltage ramp.

4.2.1.2 Matching

Matching concerns would motivate the use of larger than minimum size transistors for the delay element in order to reduce the effects of process variations; however,

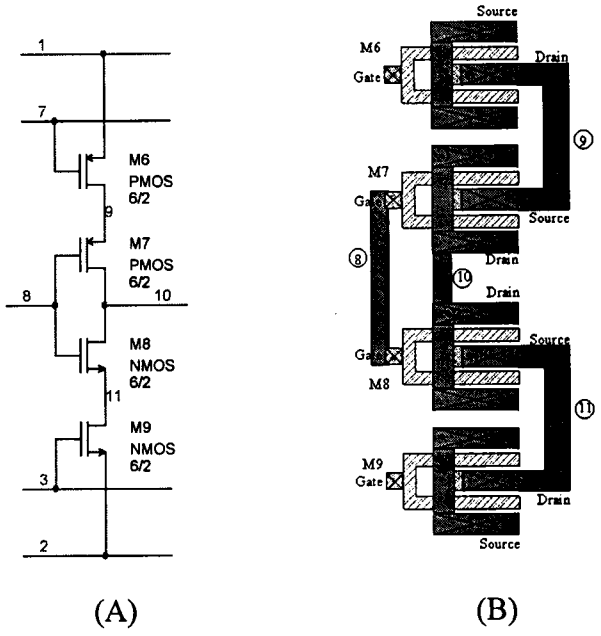


Figure 36: Layout of Starved Inverter Showing Interdigitation

larger transistors would not allow minimization of the capacitance at nodes 9 and 11 as discussed above. Thus, the minimum size interdigitated transistors were used since the nonlinearity produced by the charge storage appeared to be the dominant concern. All of the delay elements are exact duplicates of each other to make the matching as good as possible for this minimum transistor size. Figure 37 shows the simulated voltage ramp at Node 10 obtained from the post-layout extraction.

4.2.1.3 Jitter

Jitter was investigated by finding the noise at the output of the inverter and using the slope of the voltage ramp to relate the voltage noise to jitter. The

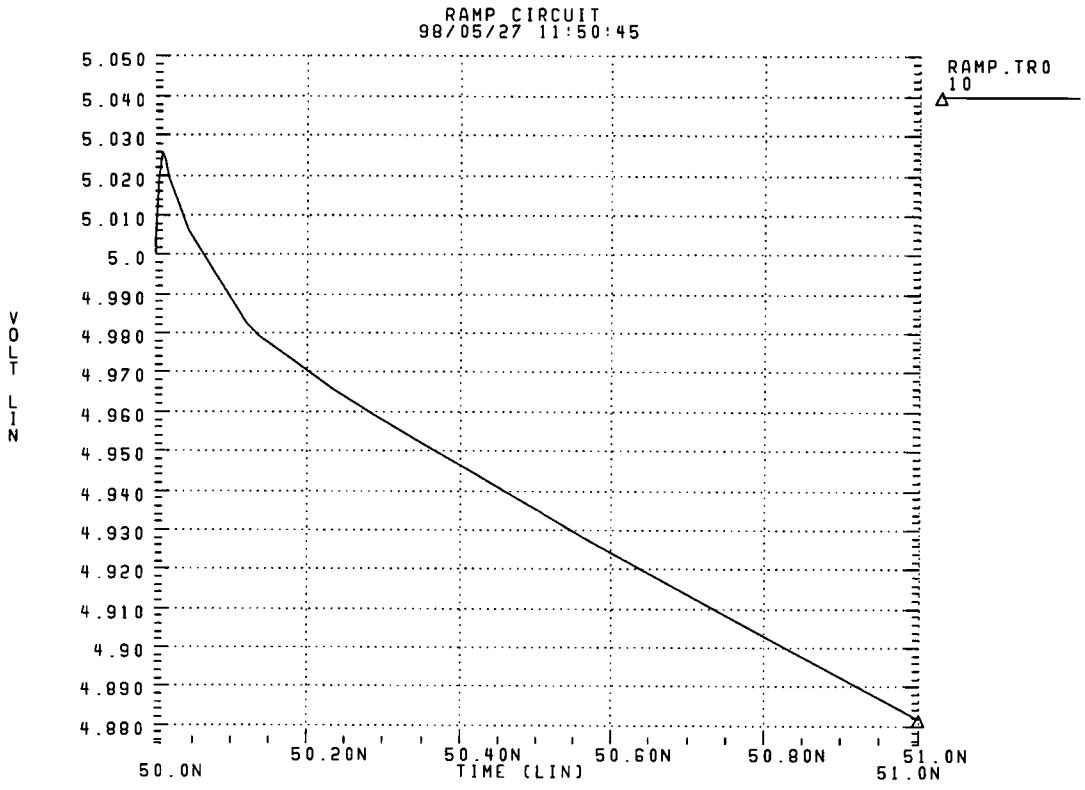


Figure 37: Plot of v_{10} From the Post-layout Extraction

relationship between the rms voltage noise (σ_v) and the rms jitter (σ_t) is given by

$$\sigma_t = \sigma_v \left(\frac{dv}{dt} \right)^{-1}$$

and is illustrated in Figure 38 (Bedwell 1976). Using this relation and the noise at the inverter output obtained from HSPICE we find σ_t for a single delay element to be

$$\sigma_t = \sigma_v \left(\frac{i}{C} \right)^{-1} = \left(56.348 \times 10^{-6} v\right) \left(\frac{50 \times 10^{-6} A}{500 \times 10^{-15} F} \right)^{-1} = 0.56348 \; ps \; rms .$$

Assuming the noise sources are independent, we can calculate an estimate for the maximum jitter of the delay system due to the delay elements. The maximum jitter

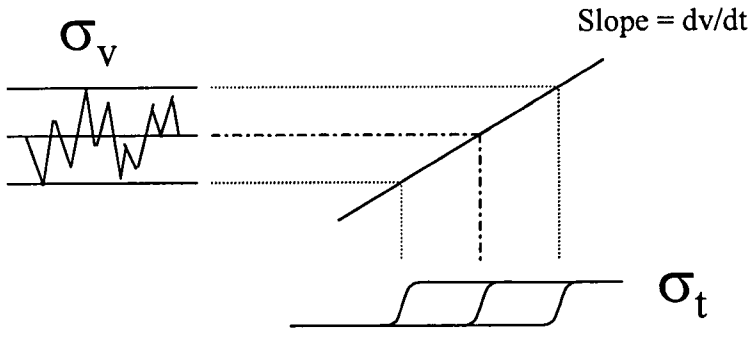


Figure 38: Illustration of the Voltage Noise to Jitter Relation

occurs at the maximum delay setting since this switches all of the coarse adjust delay elements into the signal path and gives the minimum voltage slope for the fine adjust delay elements. The system jitter can be approximated by adding the jitter of the 13 delay elements in quadrature. Thus,

$$\sigma_{tsys} = \sqrt{13 \cdot \sigma_t^{\,2}} = \sqrt{13}\sigma_t = 2.0316\ ps\ rms.$$

For a gaussian shape, FWHM = $2.355\sigma_t$ thus, the 50ps FWHM maximum jitter specification results in an allowable σ_t of 21.23ps, which leaves some room for other sources of noise in the system such as phase noise in the PLL.

4.2.2 PLL

The principal design issues for the Phase Locked Loop are temperature stability, obtaining lock and low phase noise. Temperature stability was addressed by locking the PLL to a crystal oscillator reference. The crystal oscillators used have a temperature stability of ± 100PPM over the temperature range 0°C to 70°C. The choice of a Z-state phase-frequency detector almost assures that lock will be attained

(Best 1997) provided that the reference frequency is within the VCO's frequency range. The phase noise is affected by the choice of the low pass filter, the noise characteristics of the various PLL components, and the layout. A large time constant for the low pass filters was chosen since the PLL is to be locked to a signal with a static frequency. This reduces the noise bandwidth of the system at the expense of response time. The differential control of the VCO improves the noise characteristics by improving rejection of any common mode pickup at the control inputs. Since the control circuitry is located physically near the phase detectors, there is a potential for pickup from both the reference signal and the feedback signal from the ring oscillator. Physical layout of the phase detector is important for further noise reduction. The layout of the prototype is functional but not optimal.

The main components of the PLL are the phase detectors, the low pass filters and the ring oscillator. The phase detectors and the ring oscillator are implemented on-chip and the low pass filters are implemented off-chip.

4.2.2.1 PD's

The phase detector design (Best 1997) was captured and mapped to standard cells using View Logic software. Pre-layout simulation of the phase detectors was performed using VSIM (Figure 39). Two input signals of different frequencies were applied to the inputs of the phase detector (N4 and N3), and the gate voltages of the charge pump transistors (N6 and N16) were observed. Once the proper functionality was confirmed, the Lager IV 2.0 place and route software was used to generate the magic layout (Figure 40) using a standard cell library. The charge pump transistors

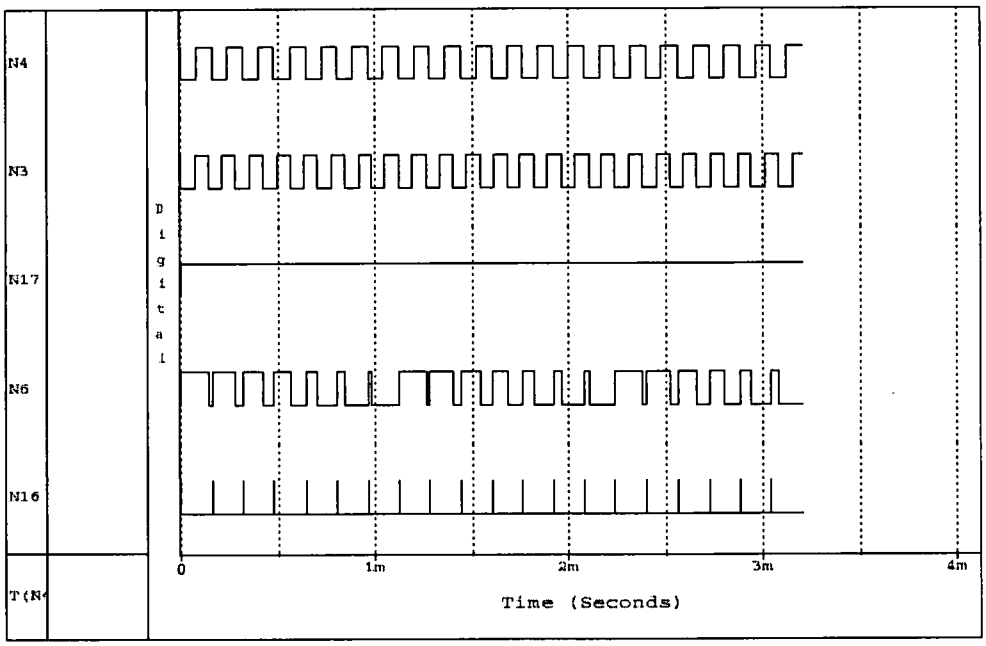


Figure 39: VSIM Simulation of the Phase Detector

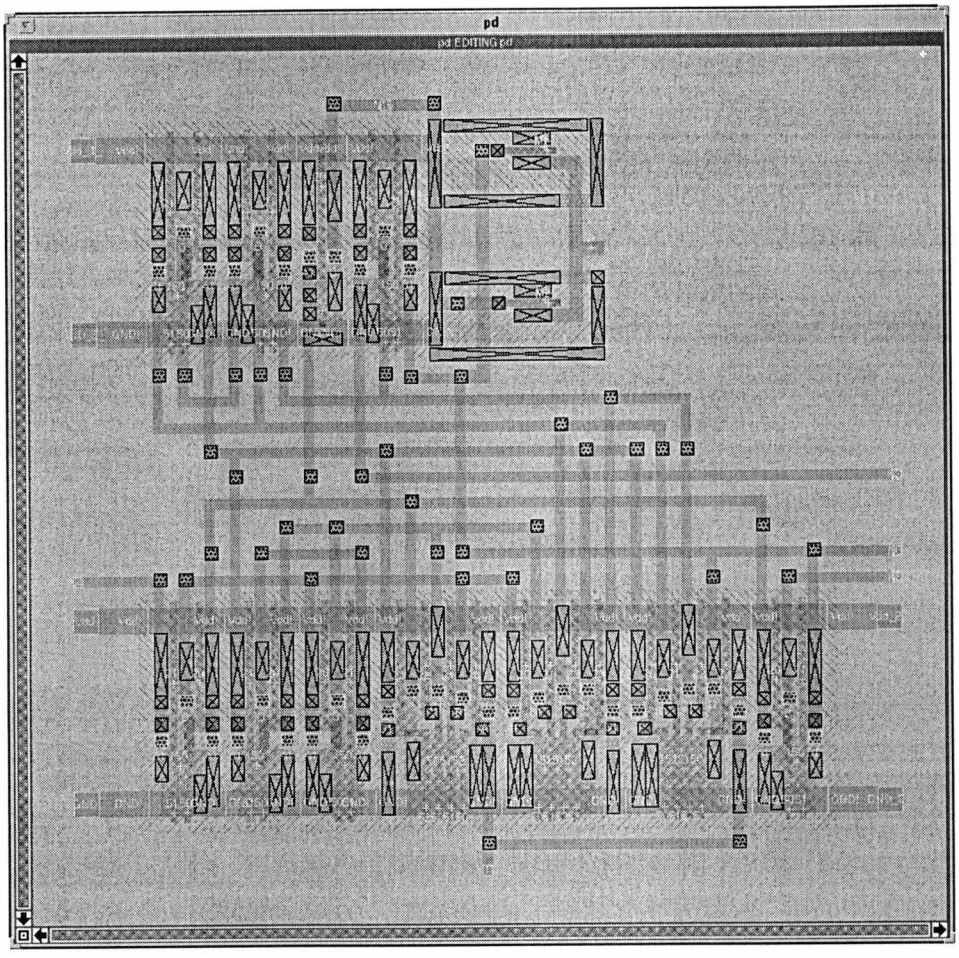


Figure 40: Magic Layout of the Phase Detector

(in the upper right hand corner of Figure 40) were added manually using Magic. A HSPICE netlist was then extracted and used for the post-layout simulation.

4.2.2.2 Ring Oscillator

The ring oscillator is constructed from eleven basic delay elements. The number of elements in the ring must be odd in order to supply the 180 degrees of phase shift required for oscillation. A large number of elements in the ring is desirable so that averaging of the single element propagation delays occurs. The actual number of elements was chosen mostly for convenience. It was decided that a delay of approximately 25ns would be used for the basic delay time. Then an easily obtained crystal frequency of 1.818MHz was chosen. Since the period of oscillation is 2 times the delay around the ring, the number of required delay elements could easily be determined. Post layout simulation of the ring oscillator was performed with the loop "broken" in order to avoid convergence problems. A voltage step from 0V to 5V was applied to the input of the broken ring and the propagation of the signal was observed. The same process was repeated with a voltage step from 5V to 0V.

4.2.2.3 Low Pass Filters

The low pass filters (Figure 41) are RCR passive filters. The initial design used RC filters (Figure 16, p.17). However, during testing of the prototype chip, a large amount of pickup noise was found at the VCO control inputs which appears to cause the PLL to never achieve lock. The Phase Detectors activate on every cycle and the ring oscillator output is phase shifted with respect to the reference signal. The

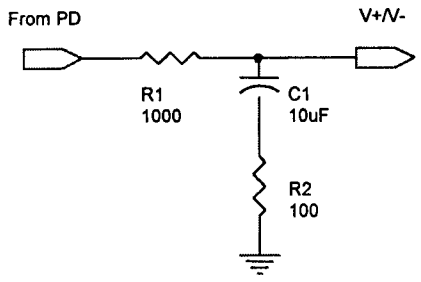


Figure 41: Modified Low Pass Filter Schematic

design of the low pass filters was modified to an RCR, which is the configuration typically used for dynamic reference signals (Best 1997). The RCR combination that produced the most stable lock was then found empirically. The combination finally chosen was R_1=1K, C=1uF, and R_2=47 for both filters.

4.2.3 One-shots and Buffers

In order to accept the narrow input pulses (2-3ns) and to present a consistent pulse width at the output, edge triggered one-shots are used to shape the input pulse and the output pulse. The one-shots are composed of a D flip-flop with a basic delay element and an inverter in the reset feedback path (Figure 42). The propagation delay

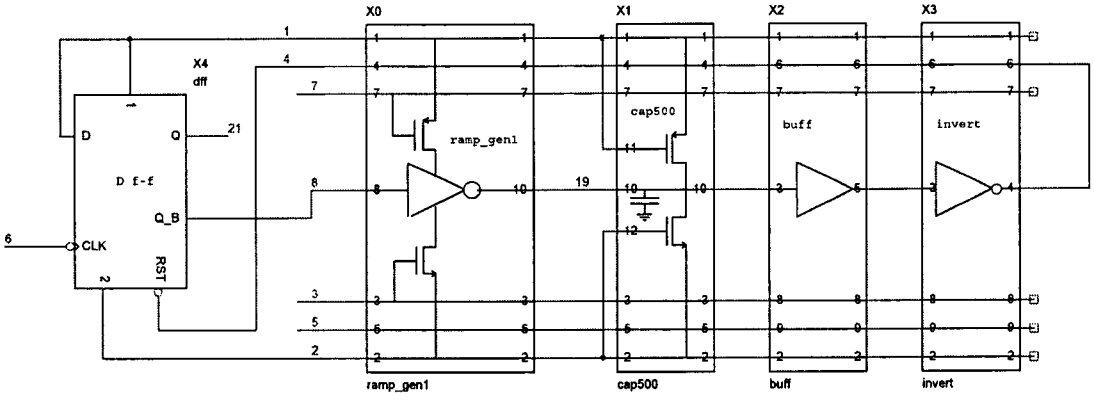


Figure 42: One-Shot Schematic

for a standard cell D flip-flop in the 1.2u process is approximately 0.5ns which is more than adequate to capture the 2ns input pulse. Thus a standard cell flip-flop was used since it was readily available and fully tested. After being laid out in Magic, a post-layout extraction was simulated using HSPICE (Figure 43) to confirm functionality. A falling edge signal was applied to node 6 and the output pulse was observed at node 21.

Buffers were used to provide the input pulse with the current drive required for the fan out to the16 clock inputs of the circular shift register and to the 16 signal inputs of the delay lines. Buffers were also used on all off chip output lines to

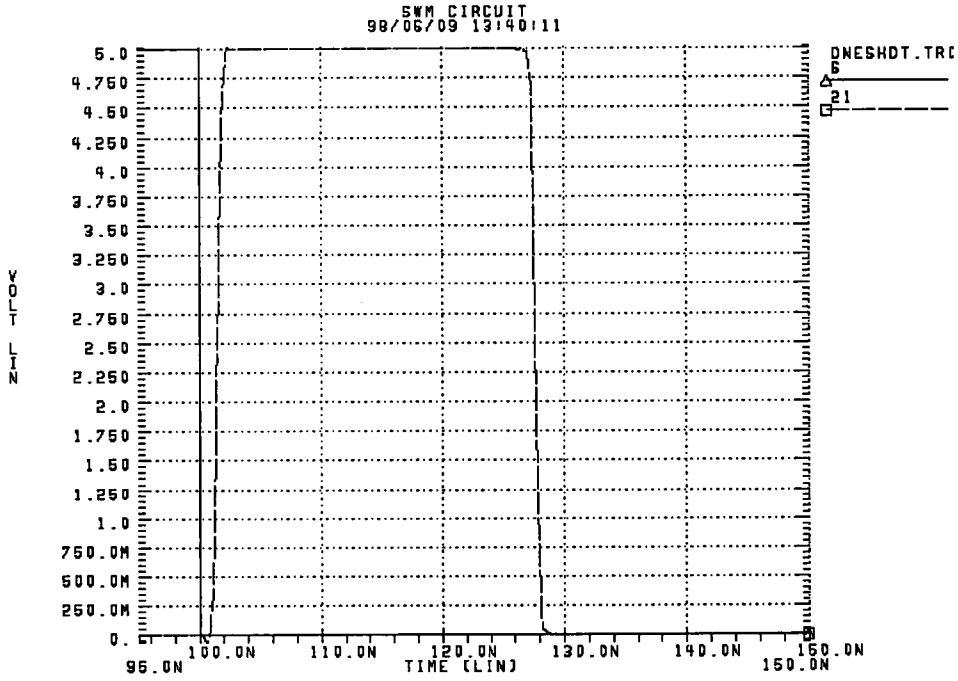


Figure 43: HSPICE Simulation of the One-shot Circuit

provide the drive needed for the output pads, package pins and off chip traces. The buffers are composed of a cascade of exponentially weighted CMOS inverters (Figure 44). The exponential weighting results in a minimized propagation delay through the buffer (Uyemura 1988).

4.2.4 Circular Shift Register

The circular shift register is composed of 16 standard cell D flip-flops connected as shown in Figure 22 (page 23). The requirements for the performance of the flip-flops are not demanding, thus the standard cells were used for convenience. The HSPICE simulation from the post-layout extraction is shown in Figure 45. This simulation was performed by supplying a reset pulse (4) to the register and then applying a clock signal (3). The propagation of the logic '1' state was then observed as it shifted from flip-flop to flip-flop.

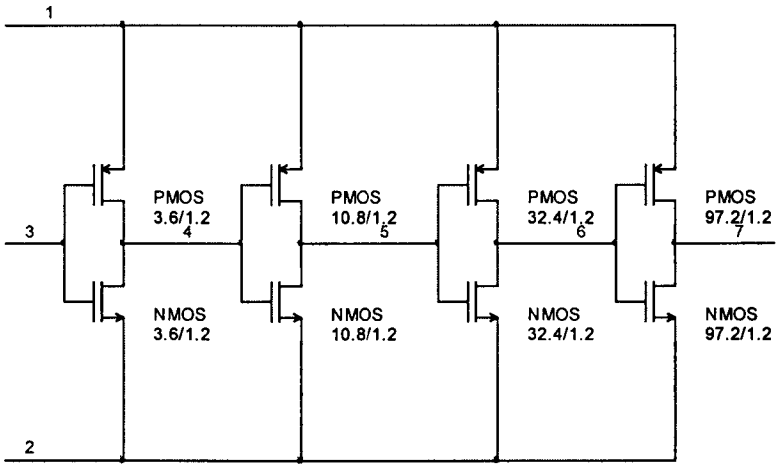


Figure 44: Buffer Schematic

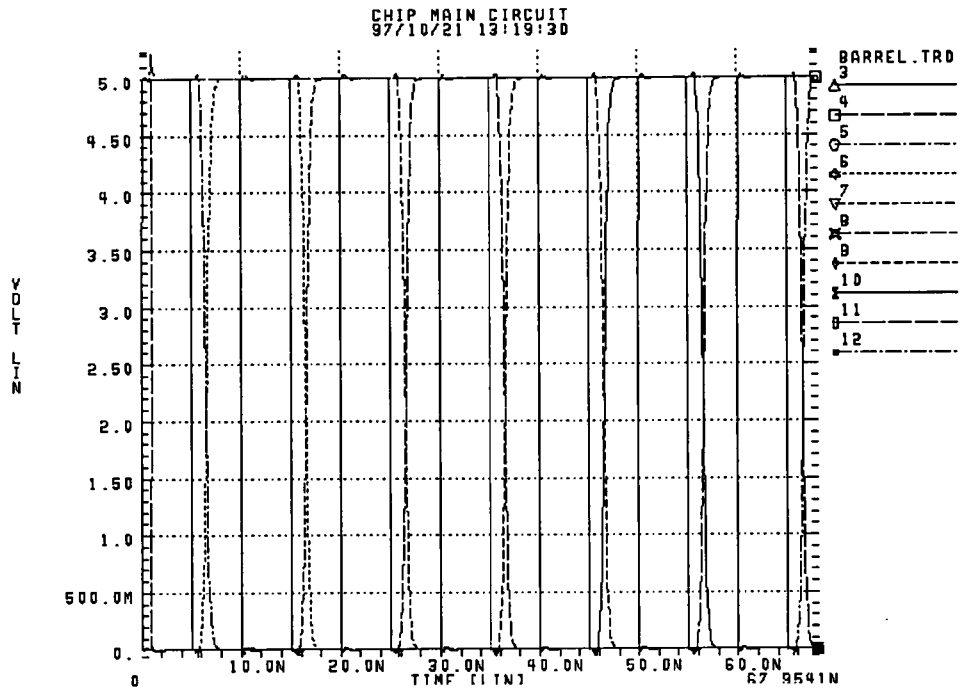


Figure 45: HSPICE Simulation of the Circular Shift Register

4.2.5 Delay Line

The basic delay elements were used to construct each of the coarse adjust delay cells and a switch cell was implemented. These cells and some standard logic cells were then used to construct a coarse adjust delay line (Figure 19 page 20) The HSPICE extraction of the delay line was simulated by applying a signal and tracing the propagation of the pulse though the delay line for the all of the possible switch settings.

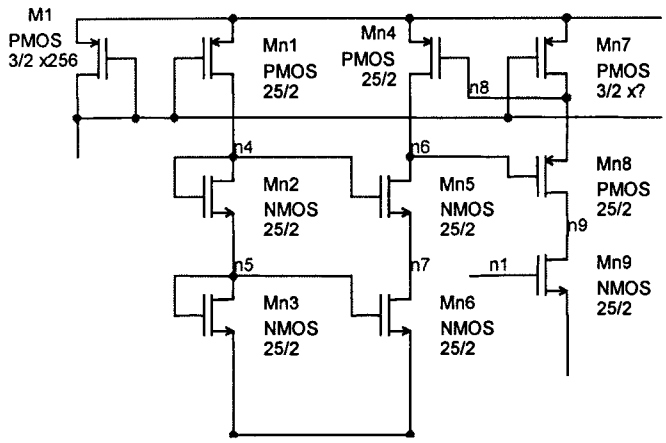
4.2.6 OR Gate

The main concern in the OR gate is to minimize the propagation delay for a rising edge signal. The OR gate is made using four standard cell NAND gates and one

standard cell NOR gate. All of the gates were 4 input devices thus, the resulting OR configuration is a 16 input gate. The NAND/NOR configuration was chosen to minimize the propagation delay of the standard cells when the input to the OR gate is a rising edge. Custom gates could be designed to further optimize this cell.

4.2.7 Switchable Mirror

The principal design issues for the switchable mirror are output impedance, linearity of the current control (stage to stage matching) and absolute matching to the reference current. Regulated cascode current mirror stages are used to provide very high output impedances. In order to improve the linearity of the current control in the switchable mirror, the regulated cascode current mirrors (figure 46) are exact copies of one another with the exception of the mirror transistors. Thus, the bias voltages applied to the mirror transistors are well matched. The mirror transistors themselves are composed of multiple copies of the minimum size mirror transistor connected in parallel. The layout was done in a "checker board" pattern (Figure 47) in order to reduce the effects of process and temperature variations across the chip. Matching of the mirror stage output currents to the reference current is determined by the sizing of Mn8 in the regulation circuits. The gate to source voltage of Mn8 determines the drain to source voltage of Mn5 and thus affects the matching of the cascode mirror supplying current to Mn4. The gate to source voltage of Mn4 sets the drain to source voltage of Mn7. Ideally, Mn8 should be sized to set V_{dsn7} equal to V_{gsn7} and thus balance the mirror. In this design, all of the Mn8 transistors were sized to balance the mirror at an output current of 1 times the reference current. For better matching and



Note: n is the reference number of the specific stage of the switchable current mirror

Figure 46: Regulated Cascode Current Mirror Stage

R	1	R	1	R	1	R	1	R	1	R	1	R	1	R	1
1	R	1	R	1	R	1	R	1	R	1	R	1	R	1	R
2	3	2	4	2	3	2	5	2	3	2	4	2	3	2	4
R	1	R	1	R	1	R	1	R	1	R	1	R	1	R	1
1	R	1	R	1	R	1	R	1	R	1	R	1	R	1	R
2	6	2	3	2	4	2	3	2	7	2	3	2	4	2	3
R	1	R	1	R	1	R	1	R	1	R	1	R	1	R	1
1	R	1	R	1	R	1	R	1	R	1	R	1	R	1	R
2	3	2	4	2	3	2	8	2	3	2	4	2	3	2	6
R	1	R	1	R	1	R	1	R	1	R	1	R	1	R	1
1	R	1	R	1	R	1	R	1	R	1	R	1	R	1	R
2	5	2	3	2	4	2	3	2	5	2	3	2	4	2	3

Note: Only ¼ of the layout scheme is shown due to space limitations

Figure 47: Layout Scheme of the Switchable Mirror Transistors

linearity, the Mn8 transistors should be sized separately in order to balance each of the mirrors for its designed output current. An operating point (.OP) analysis was done using the post-layout HSPICE extraction in order to investigate the current flow in the individual mirrors. Table 1 gives the results from this simulation.

4.3 Top Level Layout and Simulation

The top level of the prototype chip (Figure 48) was constructed by connecting the individual sub system cells to each other and to the pad frame. The delay lines were laid out in a manner such that most of the common connections between the delay lines were made by simply tiling the delay line cell in a 16x1 array.

A pad-to-pad simulation was performed on the HSPICE extraction for the entire chip. To aid convergence, the ring oscillator was again "broken" and the control voltages were set manually. The chip was reset and then a pulse train was applied to the input pad. The response of the output (Figure 49) to this input signal was simulated for a variety of delay settings. Exhaustive simulation for all switch settings was not performed since simulation time for each run was in excess of 3 hours.

Table 1 Simulated Currents in the Stages of the Switchable Current Mirror

Reference Number (n)	Mulitplicity of Mirror	Switch Transistor	Simulated Current (uA)
9	1	M99	0.2015
8	2	M89	0.4026
7	4	M79	0.8045
6	8	M69	1.6073
5	16	M59	3.2104
4	32	M49	6.4102
3	64	M39	12.7915
2	128	M29	25.5018
1	256	M19	50.7732
R	256	--	50

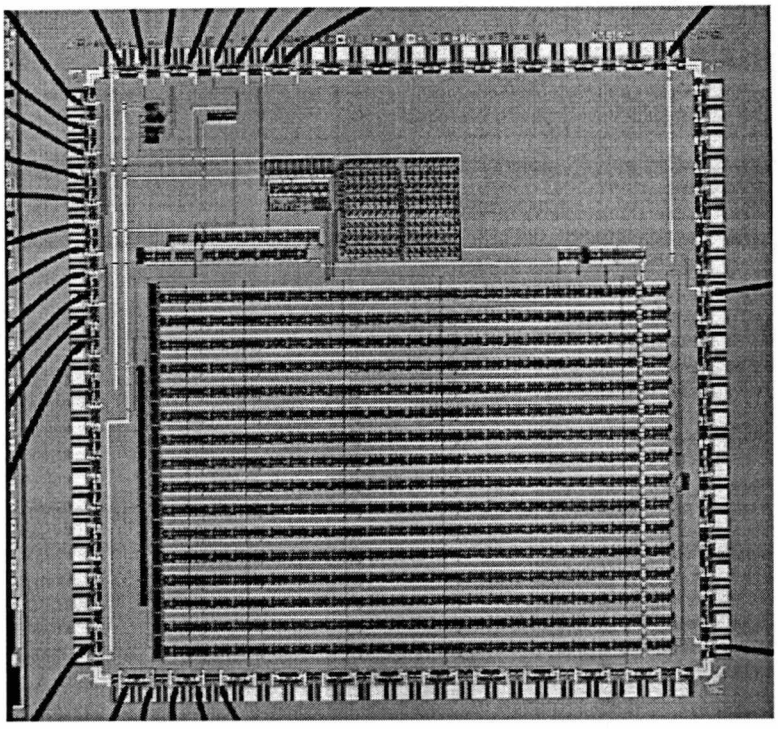


Figure 48: Photograph of Prototype Delay Chip

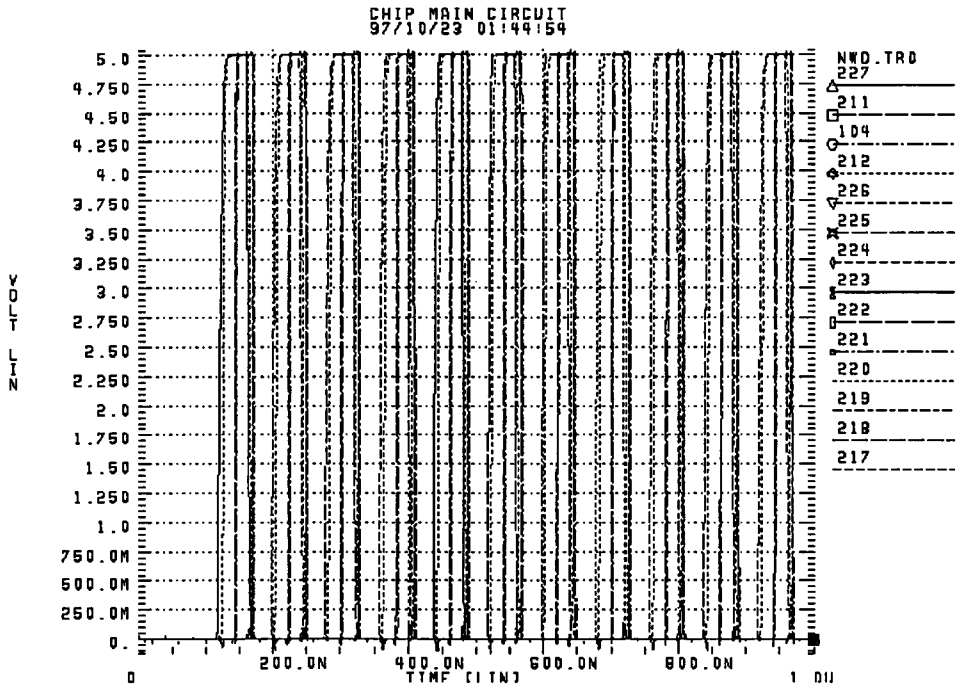


Figure 49: HSPICE Pad-to-pad Simulation of the Prototype Chip

Chapter 5 Experimental Results

A test board (Figure 50) was constructed to allow the evaluation of the prototype chip. The test circuit (Figure 51) consists of a bank of switches, a current source, the two low pass filters, and buffers for the ring oscillator output and signal output. The switches supplied the control signals for the variable delay and the current sink provided a stable bias current for the chip. The buffers were used to provide the necessary drive for the cables used to connect to the scope and other equipment.

The prototype chip was evaluated to determine its characteristics in the following areas: coarse adjust, fine adjust, jitter, temperature stability, and throughput. The experimental setup used to collect the data for the coarse adjust, fine adjust, jitter, and temperature stability measurements is shown in Figure 52. It

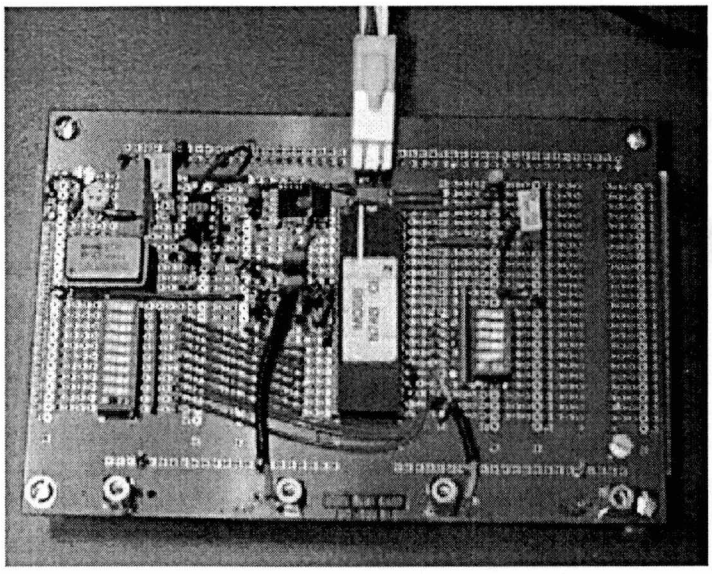


Figure 50: Prototype Test Board

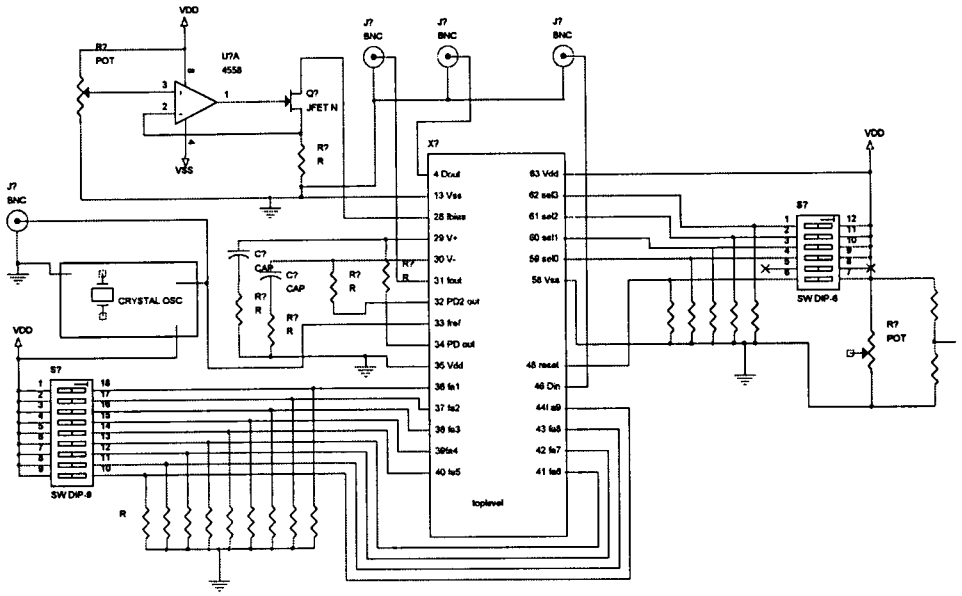


Figure 51: Test Circuit Schematic

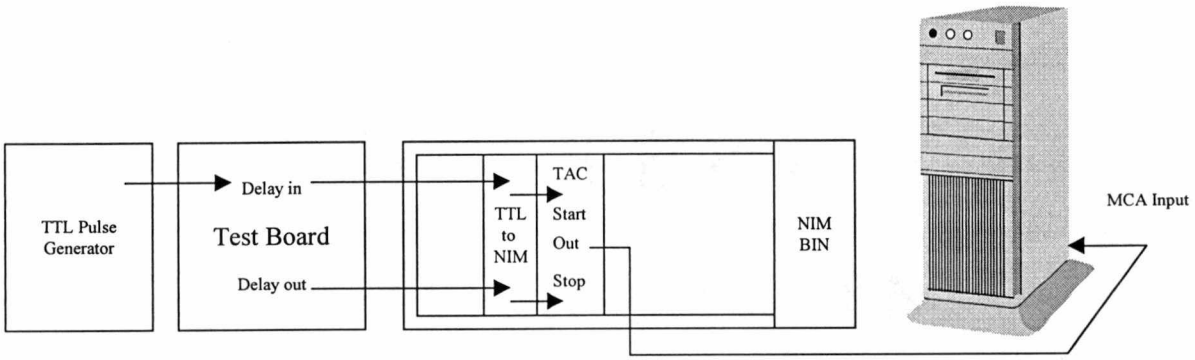


Figure 52: Test System Block Diagram

consists of a pulser, a dual TTL to NIM (Nuclear Instrument Module) Fast Logic (Knoll 1989) converter, a Time to Amplitude Converter (TAC), and a PC based Multi-Channel Analyzer (MCA). An oven was added for the temperature measurements. The pulser provides the input to the delay prototype and the start pulse for the TAC. The output of the delay chip provides the stop for the TAC. The output of the TAC is a pulse whose amplitude is proportional to the time between the start pulse and the stop pulse. This output signal is connected to the MCA which statistically bins the amplitudes of the pulses to produce a time spectrum.

5.1 Coarse Adjust Measurements

The coarse adjust was examined by taking spectra for each of the coarse adjust delay settings and observing the shift of the centroid of the time spectrum for each switch setting. When using the MCA, the full-scale setting may be adjusted to increase the time range at the expense of time resolution. The time range of the MCA required to observe each of the delay shifts was so large that the time resolution was worse than 1ns. Thus, the data could not be taken very precisely.

The coarse adjust data (Figure 53) agrees well with the expected behavior within the resolution that could be measured. The 1x delay shift is very near 24ns the 2x delay shift is approximately 48ns, and the 4x delay shifts are about 96ns. The poor resolution of the experimental setup doesn't allow precise confirmation of the delay steps.

5.2 Fine Adjust Measurements

For the fine adjust measurements, the same setup was used as for the coarse adjust measurements. However, in order to get the required resolution to measure the less than 100ps steps produced by the fine adjust, the time range of the experimental setup was changed. The start pulse of the TAC was delayed using cable delays so that the minimum setting of the fine adjust delay produced a spectrum near the bottom of the array of bins in the MCA. Then the full-scale adjustment of the TAC was set so that the maximum setting of the fine adjust produced a spectrum near the

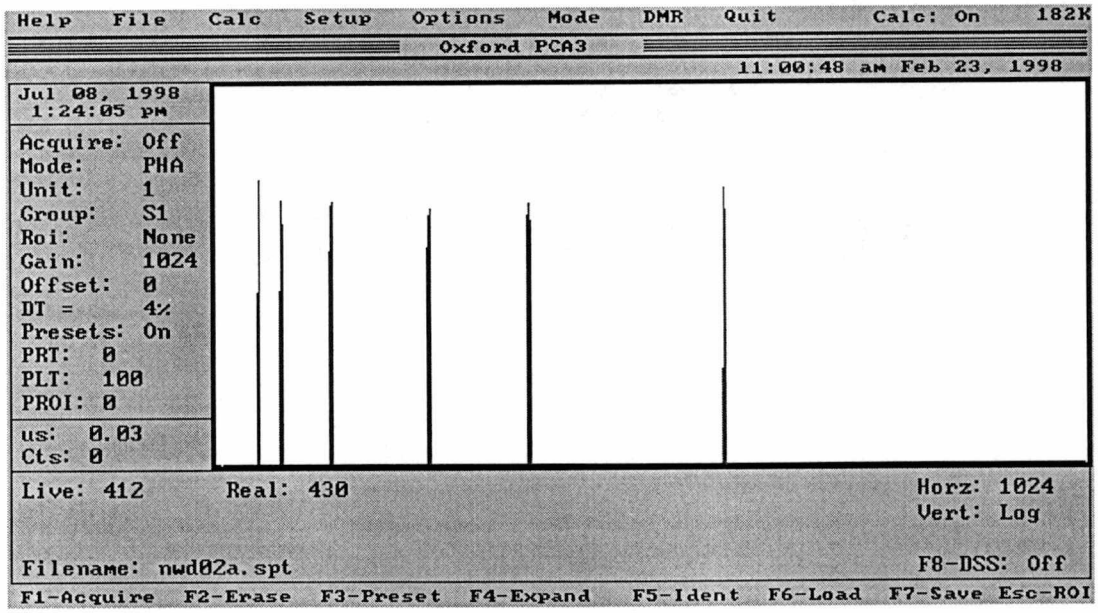


Figure 53: Coarse Adjust Data

top of the array of bins in the MCA. These settings produced a resolution of approximately 50ps per MCA channel, thus the 100 ps steps could be measured reasonably well by taking a statistical average.

The shifts of the time spectrum centroids are plotted verses the fine adjust control code in Figure 54. Since the data was taken over a three day period, some drift in the delay for a particular setting was observed from one day to the next as a result of temperature variations. In order to form a continuous plot, data for the last three delay settings from the previous day was retaken so that the amount of shift was known and could be compensated for in the plot. A theoretical curve is also included on the plot and shows very close agreement between the experimental values and the calculated values.

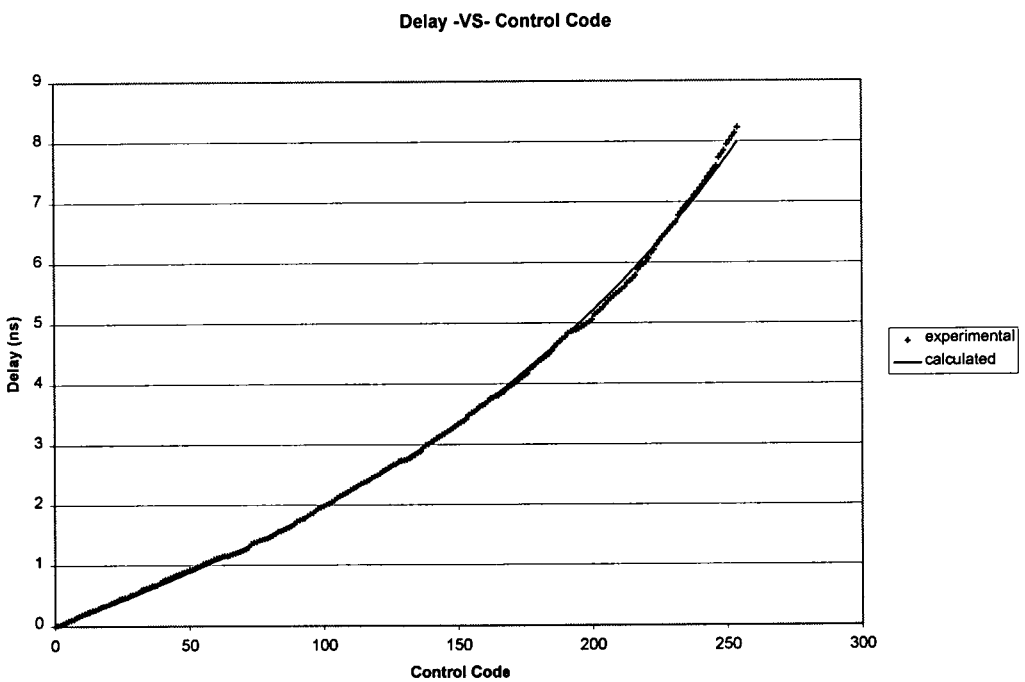


Figure 54: Fine Adjust Data Plot

5.3 MCA FWHM jitter measurement

The jitter produced by the experimental setup was investigated by replacing the prototype delay with a cable delay and acquiring a spectrum. The resulting background spectrum (Figure 55) was almost entirely confined to a single MCA bin suggesting that the jitter measured using the prototype delay is dominated by the jitter produced by the prototype and the contribution of the rest of the equipment in the experimental setup is negligible. Thus the width of the MCA time spectra is a direct measurement of the jitter in the prototype delay system. The measured jitter was a disappointing 2.5ns FWHM which is 50 times larger than the specified 50ps FWHM. The multi-peaked shape of the time spectra (Figure 56) suggested the possibility of channel to channel delay variations. In order to examine this possibility, a second circular shift register was constructed and synchronized with the on-chip shift register. This off-chip register was used to gate the output of the TAC so that only

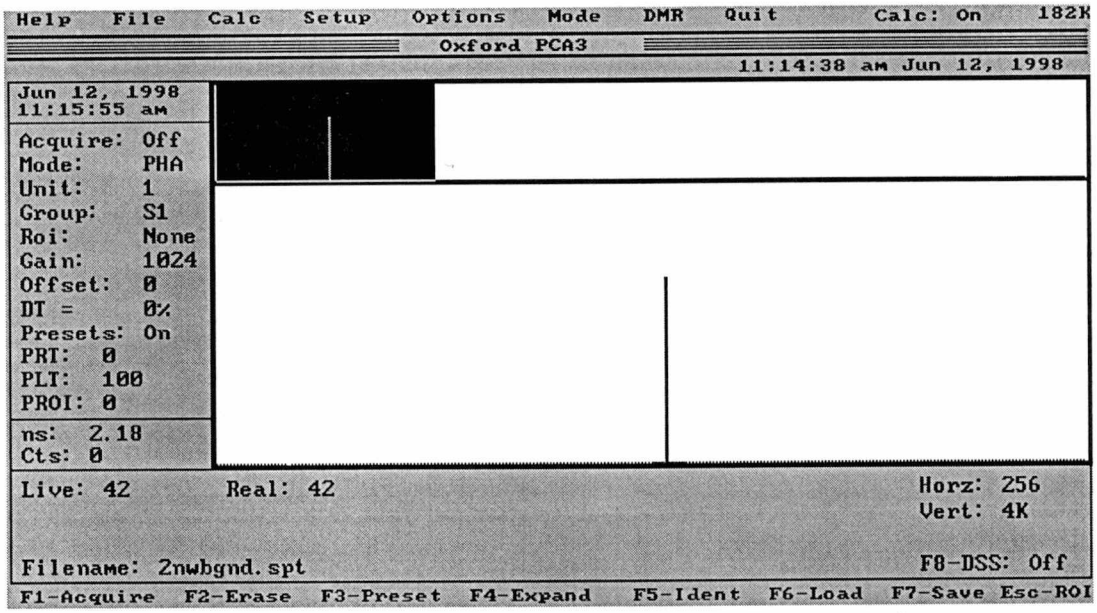


Figure 55: Jitter Background Spectrum

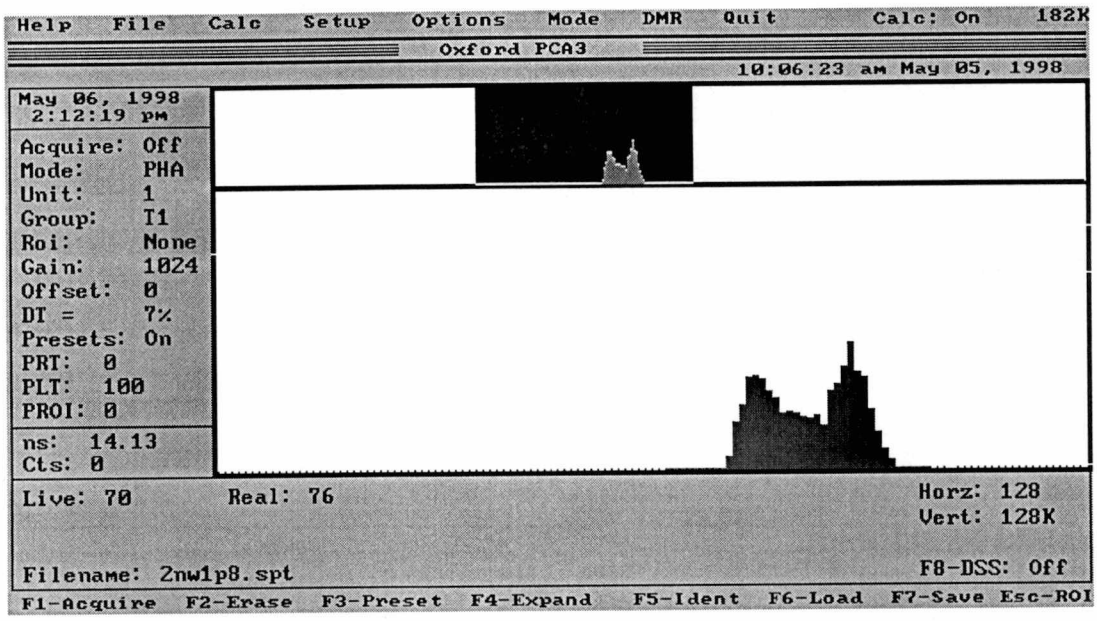


Figure 56: Prototype Delay Jitter Spectrum

the pulses produced by a single channel (every sixteenth pulse) were collected. The resulting spectra (Figure 57) were slightly narrower and slightly time shifted with respect to each other indicating a small amount of channel to channel variation. The single channel spectra exhibited a two-peak shape suggesting a bi-stable operation. This is possibly due to the large amount of noise in the phase locked loop caused by pickup. Another possible source of jitter is the perturbation of the bias lines caused by pulse propagation in the delay channels. When a delay element switches, the bias lines providing the mirror gate voltages for the starved inverter are perturbed. This perturbation can affect the adjacent delay elements as well as the ring oscillator. Perturbing the bias in the ring oscillator affects the frequency of oscillation and the feedback in the PLL causes a correction to be made to the control voltages. Since the

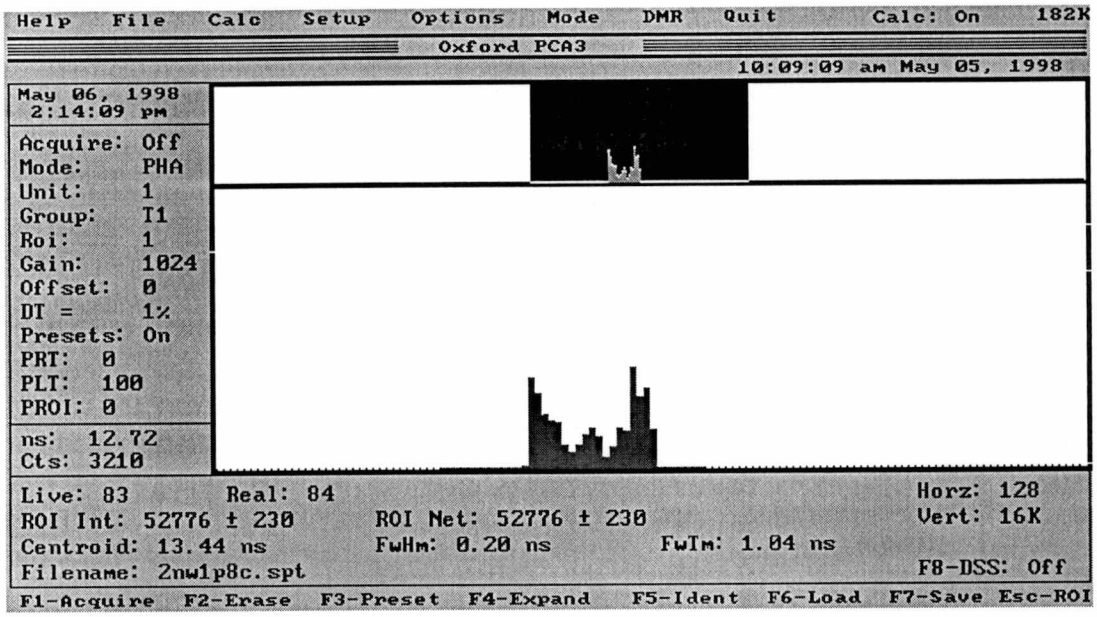


Figure 57: Single Channel Jitter Spectrum

perturbation is momentary, the correction is not truly needed, and the PLL is knocked slightly out of lock. Thus the bias line perturbations can have a significant effect on the jitter of the system. Future work should address this bias line cross talk.

5.4 Temperature Stability Measurements

The temperature stability of the prototype was evaluated by placing the test board in a temperature-regulated oven. The shift in the centroid of the time spectrum was measured for a range of temperatures from 30C to 70C for two delay settings with the system under PLL control and for one delay setting with the system operating in the open loop configuration. A trend line was fit to each of the data sets (Figure 58) in order to observe the slope of the data. The oscillator frequency was

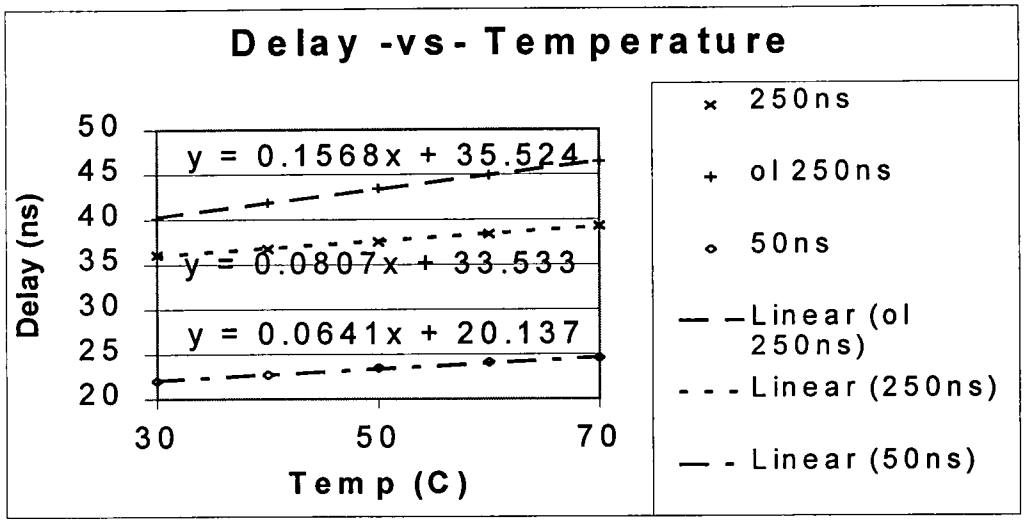


Figure 58: Delay –vs- Temperature Plot

also recorded over the 30C to 70C temperature range and is plotted in Figure 59.

The observed temperature variation for the closed loop configuration was much larger than expected. The open loop measurement resulted in a variation of 627ppm/°C and the 250ns closed loop measurement resulted in a variation of 323 ppm/°C. The full-scale delay (500ns) temperature variation could not be measured due to limitations of the experimental equipment. However, by linearly interpolating the temperature variation based on the 50ns and 250ns data sets, an estimate of 210ppm/°C can be made for the full-scale temperature variation. The feedback control only reduced the temperature variation by about a factor of two and resulted in a full-scale temperature variation that is almost a factor of two larger than the desired specification of 150ppm/°C. The feedback control only stabilizes the delay coarse adjust delay elements. There are several other sources of temperature variation in the circuit that are not regulated including: the analog switches, the OR gate, the oneshots, and the fine adjust delay element.

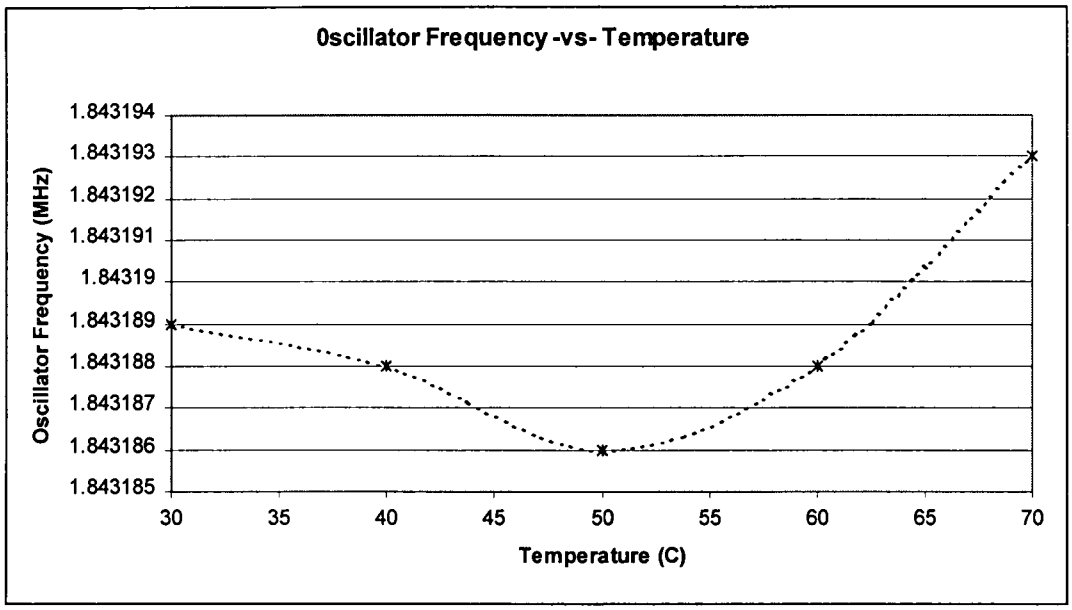


Figure 59: Oscillator Frequency –vs- Temperature Plot

5.5 Throughput Measurements

The throughput was measured by setting the oscilloscope so that multiple output pulses could be observed on the display. The input pulse frequency was then increased until the output pulses were no longer uniform but had missing pulses. These gaps indicated the loss of an input pulse due to dead time. The prototype throughput should be approximately 14MHz. The observed throughput was approximately 13.5MHz which agrees reasonably well with the expected value.

Chapter 6 Conclusion

6.1 Summary

A new low dead time adjustable delay architecture was implemented in the 1.2u AMI process. The delay uses multiple delay channels to reduce dead time and feedback control to stabilize the delay time in each channel. A two tiered adjustment scheme consisting of a 24ns step coarse adjust and a 100ps step fine adjust is used to vary the delay. The coarse adjustment is accomplished by switching delay cells into and out of the signal path. The fine adjustment is accomplished by varying the current in two starved inverter based ramp and comparator delays. The prototype was evaluated and shows some promise. The prototype performed well in the areas of high throughput and adjustability, but was disappointing in the areas of jitter and temperature stability. The disappointing jitter may be caused by pickup noise in the control voltages of the PLL that results in a poor lock and/or by crosstalk between delay elements and the ring oscillator through the bias lines. The full-scale temperature variation is approximately twice the specified variation of 150 ppm/°C. This temperature variation probably has several sources including the following unregulated components: the oneshots, the analog switches, the buffers, the OR gate, and the fine adjust delay.

6.2 Future work

6.2.1 Low noise layout (buffering and isolation)

Further work should be done to improve the isolation between delay channels.

Currently, the propagation of a pulse through a delay element perturbs the bias voltages that set the starving currents in the entire circuit. These perturbations affect surrounding delay cells and also disturb the lock of the PLL. These bias lines should be filtered and possibly buffered between delay cells. It might be possible to use current mirrors for isolation. The control voltage lines could be used to set up the current in a mirror at each delay cell that would mirror the control current into a diode to generate an isolated control voltage. It also might be possible to place a unity gain voltage buffer between the bias lines and the delay cells. Buffering should at least be done between the PLL bias control circuit and the delay elements so that the PLL can not be knocked out of lock by the propagation of a pulse through the delay elements.

The prototype was also plagued by pickup noise in the VCO control voltage lines. This pickup is caused by placement of the VCO output frequency pad next to the control voltage input pads. Future layouts should avoid this problem by taking care to ensure good spatial separation of the control voltages and any external signal. The control voltage nodes should be physically well separated from both the reference signal input and the ring oscillator output. Guard rings should also be placed between the various components of the PLL.

6.2.2 More channels

The prototype delay system has only 16 channels and the fine adjust delay element is not paralleled thus the theoretical throughput is approximately 17MHz. In order to reach the desired 200MHz throughput, the number of delay channels will have to be increased to more than 100 and the fine adjust delay element must be

moved into the parallel channels. The use of an even larger number of channels can result in very high throughputs. The fine adjust delay element must be made part of the parallel path since the dead time of the fine adjust alone restricts the throughput to less than 42MHz.

6.2.3 PLL study

The PLL should be studied more. It is highly probable that the poor performance of the PLL is the cause of the poor jitter performance of the delay system and may contribute to the poor temperature stabilization. A better layout may be sufficient to improve the PLL since on an earlier prototype chip, the PLL locked cleanly using only an RC filter. The use of a Delay Locked Loop (DLL) (Christiansen 1995) might also be considered to see if the elimination of the ring oscillator could reduce the noise in the system.

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Appendix

Appendix

Spice Source Code for the Starved Inverter

Circuit Analysis File
Filename: ramp.cir

```
ramp_gen circuit
**************************************
*<LAMBDA=0.6U>
*
**************************************
*
* 23 June 97
*
**************************************
*ANALYSIS CARDS
**************************************
*
.op
.option POST
*.probe tran i(m1) i(m2) i(m4) i(m5)
*.probe tran i(m6) i(m7) i(m8) i(m9)
*.TEMP -55 -25 0 25 50 75 100 125
.TRAN .5n 200n
*.DC VIN 0 5 .01
*.AC DEC 10 10 100GIG
*.NOISE V(10) VIN 10

****************************************
*  signal sources
****************************************


VIN 8 0 PWL(0 0 50n 0 50.01n 5)

**************************************
*BIAS SOURCES
**************************************
*
vdd 1 0 dc 5v
vss 2 0 dc 0v

ibias 7 0 50u
ibias2 0 3 50u

cdom 10 0 500f


M60 7 7 1 1 CMOSP W=3.60U L=1.20U AD=7.92P PD=12.00U AS=13.68P
PS=21.60U
```

```
M90 3 3 2 2 CMOSN W=3.60U L=1.20U AD=7.92P PD=12.00U AS=13.68P
PS=21.60U


****************************************
*MAIN CIRCUIT
****************************************


****************************************
.include "ami_n77h.l13"
****************************************

.include "ramp_gen1.spice"

.end
```

Magic Extraction File
Filename: ramp_gen.spice

```
* ramp_gen1.spice
*
* File Location         /msd25/puckett/magic/2nwisdly
* File Created          Wed Jun 10 09:48:13 1998
* Ext2spice Version     ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*           Options     -m -n -M -N -h
*
****** top level cell is /msd25/puckett/magic/2nwisdly/ramp_gen1.ext
M6 9 7 1 1 CMOSP W=3.60U L=1.20U AD=7.92P PD=12.00U AS=13.68P
PS=21.60U
M7 10 8 9 1 CMOSP W=3.60U L=1.20U AD=13.68P PD=21.60U AS=7.92P
PS=12.00U
M8 10 8 11 2 CMOSN W=3.60U L=1.20U AD=13.68P PD=21.60U AS=7.92P
PS=12.00U
M9 11 3 2 2 CMOSN W=3.60U L=1.20U AD=7.92P PD=12.00U AS=13.68P
PS=21.60U
C1 10 8 1.0F
C2 10 0 22.0F
C3 11 0 1.0F
C4 1 0 50.0F
C5 2 0 51.0F
C6 3 0 19.0F
C7 7 0 19.0F
C8 8 0 19.0F
C9 9 0 1.0F
*** Node Listing for subckt:  ramp_gen1
** N0                          ==  IdealGND
** N1                [U=3]     ==  N1
** N2                [U=3]     ==  N2
** N3                [U=1]     ==  N3
** N4                [HIDE]    ==  N4
```

```
** N5                  [HIDE]     ==  N5
** N7                  [U=1]      ==  N7
** N8                  [U=2]      ==  N8
** N9                  [U=2]      ==  N9
** N10                 [U=2]      ==  N10
** N11                 [U=2]      ==  N11
*************************************************************
*
* Model Definitions for HSPICE
*
*************************************************************
```

Device Models
Filename: ami_n77h.l13

```
================================================

* N77H SPICE BSIM1 (Berkeley Level 4; HSPICE Level 13) PARAMETERS

*
*PROCESS=AMI
*RUN=n77h
*WAFER=01
*Gate-oxide thickness= 296 angstroms
*DATE=15-Sep-1997
*
*NMOS PARAMETERS
*
.MODEL CMOSN NMOS LEVEL=13 VFB0=
+ -8.85576E-01, 2.17315E-02, 8.11386E-02
+  7.31313E-01, 0.00000E+00, 0.00000E+00
+  8.50535E-01,-1.50278E-01, 3.26765E-03
+  5.40966E-02, 2.17468E-02,-3.68896E-02
+ -8.95037E-03, 1.82423E-02, 4.43876E-03
+  5.95169E+02,2.48622E-001,1.12331E-000
+  6.53743E-02, 1.08945E-01,-7.15899E-02
+  6.56661E-02, 2.23113E-01,-8.22110E-03
+  8.73255E+00,-5.97832E+00, 8.68908E+00
+  1.42076E-04,-5.86673E-03, 9.14482E-04
+  7.41308E-04, 2.63804E-04,-1.64151E-03
+  5.95229E-04,-3.29592E-03, 9.36018E-04
+ -1.90892E-02, 1.70718E-02, 4.12640E-03
+  6.54948E+02, 1.00160E+02,-3.13475E+01
+ -6.13467E+00, 8.39334E+00, 1.09669E+01
+  5.74788E+00, 2.98902E+00, 3.14387E+00
+  5.48526E-03,-2.68932E-03, 1.81137E-03
+ 2.96000E-002, 2.70000E+01, 5.00000E+00
+ 2.17532E-010,2.17532E-010,3.92111E-010
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
```

```
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 54.4,    2.773500e-04,    1.341300e-10,    1e-08,    0.96971
+ 0.96971,    0.54186,    0.1,    0,    0
*
* Gate Oxide Thickness is 296 Angstroms
*
*
*PMOS PARAMETERS
*
.MODEL CMOSP PMOS LEVEL=13 VFB0=
+ -1.20249E-01,-3.55598E-02, 9.71674E-02
+  6.93380E-01, 0.00000E+00, 0.00000E+00
+  2.93797E-01, 5.26674E-02, 9.92145E-02
+ -4.96957E-02, 7.77685E-02, 1.90456E-03
+ -1.19553E-02, 6.34928E-02,-7.36259E-03
+  1.91287E+02,-9.34675E-003,1.12931E-000
+  1.22122E-01, 3.37828E-02,-5.56294E-02
+  2.93742E-03, 2.34980E-01,-1.56653E-02
+  7.49195E+00,-2.77634E+00, 2.58615E+00
+ -6.09108E-04,-5.76845E-04,-9.19940E-04
+  3.90868E-04,-2.28107E-03,-9.67425E-06
+  5.63234E-03,-2.13456E-03, 3.48755E-04
+ -1.64611E-03, 4.47515E-03, 2.53747E-03
+  1.89527E+02, 1.29438E+02,-2.06775E+01
+  5.90121E+00, 3.07946E+00, 4.11198E+00
+  3.35992E-01, 1.06946E+01,-9.89154E-01
+ -2.91542E-03,-9.82441E-03, 4.76267E-03
+ 2.96000E-002, 2.70000E+01, 5.00000E+00
+ 5.00000E-011,5.00000E-011,3.93406E-010
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 1.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 0.00000E+000,0.00000E+000,0.00000E+000
+ 72.5,    2.980600e-04,    2.001600e-10,    1e-08,    0.80989
+ 0.80989,    0.46657,    0.1,    0,    0
*
*N+ diffusion::
*
*.MODEL PC1_DU1 R
*+ RSH=54.4 COX=0.000277 CAPSW=1.34e-10 W=0 DW=0
*
*P+ diffusion::
*
*.MODEL PC1_DU2 R
*+ RSH=72.5 COX=0.000298 CAPSW=2e-10 W=0 DW=0
*
*METAL LAYER -- 1
*
*.MODEL PC1_ML1 R
*+ RSH=0.06 COX=2.6e-05 CAPSW=0 W=0 DW=0
*
*METAL LAYER -- 2
*
*.MODEL PC1_ML2 R
*+ RSH=0.03 COX=1.3e-05 CAPSW=0 W=0 DW=0
```

Vita

Bryan Puckett was born on July 25, 1968 in Lubbock, Texas. Most of his childhood was spent in Portland, Tennessee where he graduated from Highland Academy in 1987. Bryan continued his education at Southern College of Seventh-Day Adventists. He graduated in 1991 with a B.S. in Mathematics and a second major in Physics. He attended Vanderbilt University for two years studying graduate Physics. After Vanderbilt, he attended the University of Tennessee at Knoxville where he received his B.S.E.E. in December of 1995 and his Master of Science in Electrical Engineering in August of 1998.