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I am submitting herewith a thesis written by Bradley David Miser entitled "Design of a Wide-Swing Cascode Beta Multiplier Current Reference." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Design of a Wide-Swing Cascode Beta Multiplier Current Reference

A Thesis
Presented for the
Master of Science
Degree

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Bradley David Miser
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Abstract

This thesis presents a study of the design of a wide-swing, cascode β multiplier current reference to be used as a biasing circuit. The current reference has been fabricated in a 0.5μm CMOS technology. First, a review of wide-swing cascode current mirrors and current-source self-biasing is covered. Then, the process of designing a current reference that is both wide-swing and has high output resistance is presented. Simulation and measurement results from the current reference are detailed. Improvements upon the current reference are also suggested.

Table of Contents

Chapter 1: Introduction and Overview …….....1
1.1: Introduction…….....…1
1.2: Scope of Thesis…….....1
1.2.1: Current Source Requirements…….....1
1.2.2: Contributions of Current Work…….....2
1.3: Organization of Thesis…….....2

Chapter 2: Current Reference Fundamentals……..…….....…..4
2.1: Introduction…….....……4
2.2: Current Reference Performance Metrics…….....….4
2.2.1: Example of a Current Reference…….....….4
2.2.2: Wide-Swing Cascode Current Mirror……..8
2.2.2.1: Improved Voltage Swing…….……8
2.2.2.2: High Output Resistance……10
2.2.3: Current Source Self-Biasing…….....11
2.2.3.1: β Multiplier Referenced Self-Biasing……11

Chapter 3: Designing Wide-Swing Cascode Current References……...16
3.1: Introduction…….....16
3.2: Designing a Wide-Swing, High Output Resistance β Multiplier……..16
3.2.1: Setting Current Value…….....17
3.2.2: Converting β Multiplier to Wide-Swing Cascode……19
3.3: Stability Analysis of Wide-Swing Cascode β Multiplier……..23
3.4: Layout of the Wide-Swing Cascode β Multiplier……..28

Chapter 4: Current Reference Simulation Results…….……29
4.1: Introduction……29
4.2: Simulation Methodology……...29
4.3 Simulation Results……31
4.3.1 DC Output Voltage Sweep……31
4.3.2 Start-Up Simulations……..33
4.3.3 Stability Simulations……..33

Chapter 5: Current Reference Measured Results……41
5.1: Introduction…….....41
5.2: Testing of the Fabricated Wide-Swing β Multiplier…….....…41
5.2.1: Testing Methodology…….....41

5.2.2: Measured Results…….....42
5.2.2.1: DC Output Voltage Sweep…….42
5.2.2.2: DC Start-Up Test……...45
5.2.2.3: Temperature Sweep……...47

Chapter 6: Conclusion…….....49
6.1: Conclusion…….....49
6.2: Future Work…….....49

References…….....51

Vita…….....…55

List of Figures

Figure 1: Example of a Current Reference ……5
Figure 2: Current Reference with Transistor Small-Signal Model…….……...6
Figure 3: Wide-Swing Cascode Current Mirror [1]...……9
Figure 4: β Multiplier Current Reference (Start-Up Circuit Not Shown) [1]……...12
Figure 5: Wide-Swing Cascode β Multiplier Current Reference ……21
Figure 6: NMOS Negative-Feedback Loop …….24
Figure 7: Layout of Wide-Swing Cascode β Multiplier Current Reference…….28
Figure 8: Current Reference Schematic for Simulations.……..…30
Figure 9: DC Output Voltage Sweep.…….……..32
Figure 10: Transient Start-Up Simulation ……34
Figure 11: Start-Up Test With Zero Initial Current……..35
Figure 12: Current Inserted For Stability Simulations…….….37
Figure 13: Schematic for Stability Simulations.……...38
Figure 14: Stability Simulation of NMOS Feedback Loop……...……...39
Figure 15: Stability Simulation of PMOS Feedback Loop……..40
Figure 16: Test Setup for Output DC Voltage Sweep……..43
Figure 17: Measured Output Current of the Fabricated β Multiplier……...44
Figure 18: Output Current of Fabricated β Multiplier over Power Supply Sweep……...46
Figure 19: Output Current of β Multiplier versus Temperature……...48
Figure 20: Programmable Resistor for β Multiplier ……50

Chapter 1

Introduction and Overview

1.1 Introduction

A current reference is often needed to bias critical analog signal processing building blocks such as operational amplifiers and comparators. Designing a current reference that meets all of the design criteria needed is a considerable task in itself. A constant current over a large voltage range is typically required. Also, the current should not vary significantly over a large temperature range, depending on the circuit application. So, this thesis will focus on the design process of a current reference that meets these demands.

1.2 Scope of Thesis

1.2.1 Current Source Requirements

The focus of the remainder of this work is the design process of a current reference that can provide a constant current bias over a large voltage range. Additionally, this current reference should provide a relatively small variation in output current over a large temperature range. For this thesis, the current source will be tested over a range of 0 to 100 $°C$. The desired current output will be 20 μA using a power

supply voltage of 5 V. In order to maintain a constant current value over a wide range of output voltage, the current reference will need to have a high output resistance and low minimum compliance voltage.

1.2.2 Contributions of Current Work

The design approach for this current source begins with hand calculations to determine the needed transistor sizes in order to meet all of the design criteria. Once the circuit is designed, many simulations using SMARTSPICE must be performed to determine the performance of the circuit. Improvements are made based on these simulation results. After the circuit design was finalized, the current reference was fabricated in a 0.5 μm CMOS process. Hardware testing is then used to determine the performance of the fabricated circuit. These results are compared to the simulations of the design. The goal of this project is to design a current reference that will output a constant current over a large voltage and temperature range. How well the circuit operates over temperature and output voltage range is not strictly specified. This work however, provides a design example that may be utilized by others in the field.

1.3 Organization of Thesis

Chapter two contains an overview of current reference fundamentals. A description of important performance metrics of current references is covered. First, an example current reference is introduced. The wide-swing cascode current mirror is also

described. Finally, chapter two concludes with a discussion of current source self-biasing.

Chapter three describes designing wide-swing, high output resistance current references. This chapter deals with designing a wide-swing β multiplier that utilizes a wide-swing current mirror bias. A feedback stability analysis is also covered.

Chapter four covers the simulations of the wide-swing cascode β multiplier current reference. Simulations were performed in order to determine how well the current reference performs for the desired characteristics.

Chapter five discusses the measured results of the final current reference design. This chapter covers the testing of the fabricated circuit. The testing methodology and results are included.

The conclusions of the thesis are given in chapter six. A review of the results from this work and a discussion of further work that may be pursued are included. This future work may improve upon the current design.

Chapter 2

Current Reference Fundamentals

2.1 Introduction

Chapter two focuses on the fundamentals of current references. It begins with a definition of a current source. A current reference is either a source or a sink. The rest of the chapter focuses on the two major building blocks of the current reference to be designed in chapter three.

2.2 Current Reference Performance Metrics

2.2.1 Example of a Current Reference

One example of a current reference is shown in Figure 1. This current source utilizes an operational amplifier (op amp) or an operational transconductance amplifier (OTA) and a transistor to provide a voltage to the resistor R. A reference voltage, say provided by a bandgap reference[1], is applied to the non-inverting input of the op amp. If the op amp is close to ideal, then the voltage at the inverting input will be equal to the reference voltage. Since an actual op-amp will have a small input offset voltage, this will actually be the reference voltage plus the input offset voltage. The inverting input is tied to the top of the resistor, which causes the reference voltage plus the input offset voltage

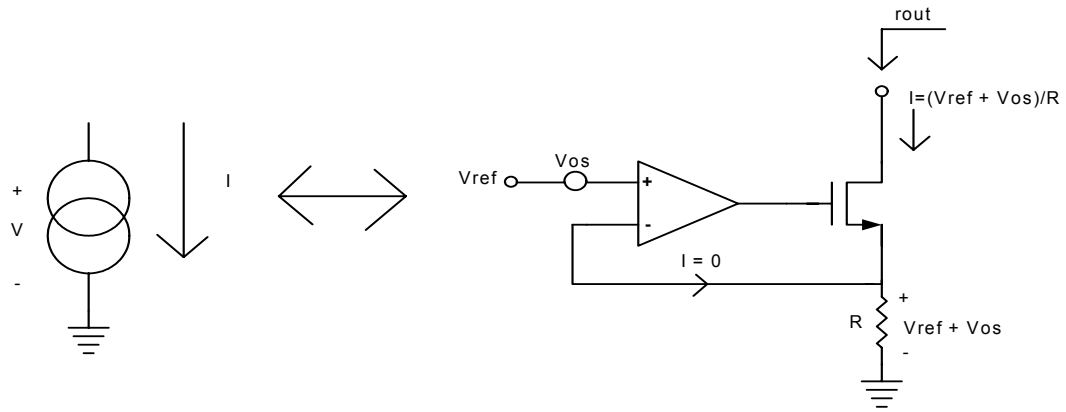

Figure 1: Example of a Current Reference

to be applied to the top of the resistor. This voltage produces a current approximately equal to the reference voltage plus the offset voltage divided by the resistance value. Because there is no current going into the inverting input of a high input impedance op amp, then the current flowing through the resistor will also be the drain current of the transistor. So, this current source produces an output current based on the resistor value and the reference voltage.

Two of the most important parameters of a current reference are its small-signal output resistance and its minimum output voltage requirement (also know as compliance voltage) to maintain its output resistance. High output resistance is desired, as is low minimum output voltage. The small-signal output resistance of this current source can be found by inserting the small-signal model for the transistor as seen in Figure 2. Direct analysis can be used to find the output resistance [30]. From Figure 2, the analysis is as follows.

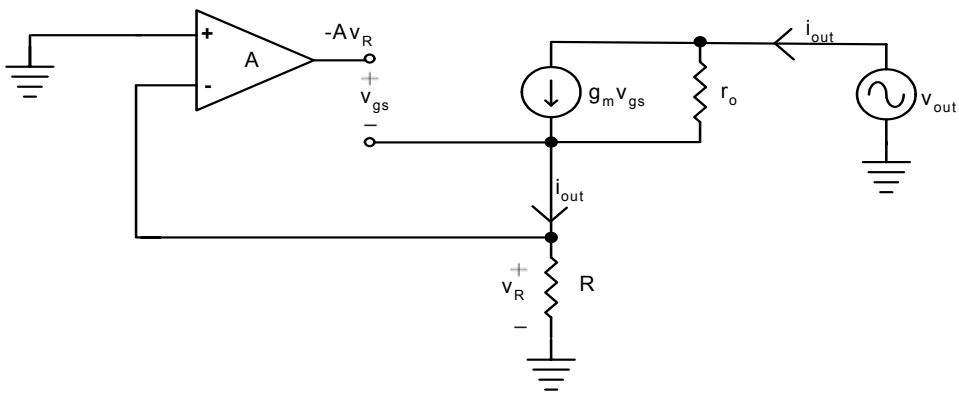

Figure 2: Current Reference with MOSFET Small-Signal Model

$$i_{out} = g_m v_{gs} + \frac{v_{out} - v_R}{r_o} \tag{2.1}$$

$$v_{gs} = -Av_R - v_R = -v_R(1 + A) \tag{2.2}$$

$$i_{out} = \frac{v_R}{R} \tag{2.3}$$

Substituting equations 2.2 and 2.3 into equation 2.1 and solving for $\frac{v_{out}}{i_{out}}$, the output resistance is provided below.

$$R_o = \frac{v_{out}}{i_{out}} = r_o(1 + g_m R[1 + A] + \frac{R}{r_O}) \tag{2.4}$$

This result reduces to approximately

$$R_o \cong g_m r_O R(1+A) \tag{2.5}$$

since A can be quite large. So, the output resistance of the current source is determined by the open-loop gain of the op-amp, the small-signal parameters of the transistor, and the resistor R. Thus, very high small-signal output resistance, easily well over 10 MΩ, can be achieved.

The minimum output voltage swing would be the voltage across the resistor, or the reference voltage, plus the saturation voltage of the transistor. Since the reference voltage depends on the resistor value, it could cause a high minimum output voltage.

Another important consideration is the fact that on-chip resistors have a high tolerance value. Some on-chip resistors compatible with standard CMOS can vary as much as 30% from the desired value [1]. Considering that the output current of this current source depends very much upon the resistor value, an accurate current value would be impossible to achieve if the resistor had a high tolerance. One option to correct this problem may be to use a programmable resistor could be used.

The simplest way to achieve an accurate current using the circuit shown in Figure 1 would be with discrete off-chip parts since discrete resistors can have a tolerance as low as 1% (metal-film). But, often times, it is desirable to have a fully integrated on-chip current reference. As just discussed, an accurate current value could be achieved using a programmable resistor. The disadvantage to using the current source in Figure 1 on-chip is the fact that it would be rather large since an entire operational amplifier, or at least an OTA is needed.

This chapter will discuss building blocks and design techniques that may be used to improve on the current source in Figure 1. These will be used in chapter three to design a smaller current reference that has higher output resistance and a low minimum output voltage that is not dependent on a fabricated resistor.

2.2.2 Wide-Swing Cascode Current Mirror

The first important circuit that needs to be covered for the design of a wide-swing cascode β multiplier current reference is the wide-swing cascode current mirror. A thorough treatment of current mirror basics and cascode connections can be found in the Baker, Li, and Boyce text [1]. As the name implies, the wide-swing cascode current mirror has both a wide output voltage swing and high output resistance.

2.2.2.1 Improved Voltage Swing

A detailed analysis of the wide-swing cascode current mirror, seen in Figure 3, will now be given. The first step in the design is to realize that the voltage needed at the drain of M_5 is $(2\Delta V + V_{THN})$, where $\Delta V = V_{GS} - V_{THN}$. This can be shown because of the fact that one ΔV is needed at the drain of M_2 in order to get the desired output voltage constraint. So, if the voltage at the drain of M_5 is $(2\Delta V + V_{THN})$, then the voltage at the drain of M_2 is one gate-to-source voltage lower. This gives the following result.

$$V_{D,\,M2} = V_{S,\,M4} = (2\Delta V + V_{THN}) - V_{GS} = (2\Delta V + V_{THN}) - (\Delta V + V_{THN}) = \Delta V \quad (2.6)$$

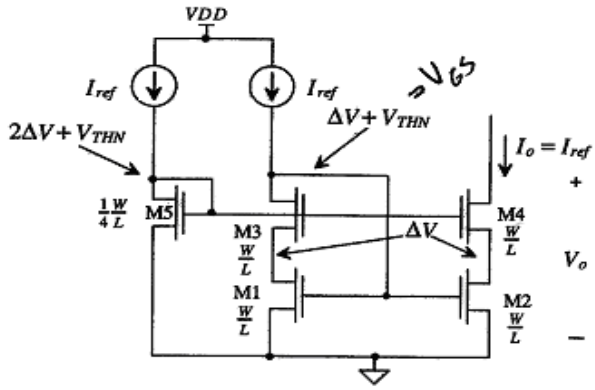

Figure 3: Wide-Swing Cascode Current Mirror [1]

Once again, ΔV is also needed across M_4 to keep it saturated. This gives $V_{o,\,min}$ as 2ΔV, the minimum possible compliance voltage for a cascode configuration.

An explanation of how transistor sizing can affect the output voltage constraint will now be discussed. Since the drain and gate of M_5 are tied together, this means that the voltage at the drain of M_5 is equal to its gate-to-source voltage. The drain voltage of M_5 was earlier said to be $(2\Delta V + V_{THN})$. Using the saturated drain current equation for transistor M_5, this voltage will be substituted in for V_{GS} below.

$$I_{D,\,5} = \frac{\beta_5}{2}(V_{GS,\,M5} - V_{THN})^2 = \frac{\beta_5}{2}(2\Delta V + V_{THN} - V_{THN})^2 \text{, neglecting body-effect} \quad (2.7)$$

$$I_{D,\,5} = \frac{\beta_5}{2}(2\Delta V)^2$$

Transistor M_1 will be sized so its gate-to-source voltage is still equal to the typical value of $(\Delta V + V_{THN})$. Again, the drain current equation is used for M_1 in equation 2.8.

$$I_{d,\,1} = \frac{\beta_5}{2}(V_{gs,\,M1} - V_{THN})^2 = \frac{\beta_1}{2}(\Delta V + V_{THN} - V_{THN})^2 = \frac{\beta_1}{2}(\Delta V)^2 \qquad (2.8)$$

Since the two drain currents are both equal to I_{ref} as seen in Figure 3, the needed ratio between transistors M_1 and M_5 can now be found by equating the two drain currents and solving for $\frac{\beta_5}{\beta_1}$. This is seen in the following equation.

$$I_{D,\,5} = I_{D,\,1} = I_{ref} \qquad (2.9)$$

$$\frac{\beta_5}{2}(2\Delta V)^2 = \frac{\beta_1}{2}(\Delta V)^2$$

$$\frac{\beta_5}{\beta_1} = \frac{1}{4}$$

So, the gate-drain tied transistor M_5 must have a size one fourth that of M_1 in order to supply the correct voltage to the gate of M_4. This will give the desired output voltage constraint [1].

2.2.2.2 High Output Resistance

The wide-swing cascode current mirror offers high output resistance. The analysis can be found in Baker, Li, and Boyce [1]. The output resistance of a cascode connection is approximately

$$R_O \cong g_{m4} r_{O_2} r_{O_4} \tag{2.10}$$

Using the cascode connection raises the output resistance significantly since the output resistance of a simple two transistor current mirror is only one r_O.

2.2.3 Current Source Self-Biasing

It has been shown so far in this chapter that some of the desirable characteristics of current references may be achieved using the wide-swing cascode current mirror. These characteristics include high output resistance and low minimum output voltage. In addition, reference current generation that is independent of supply voltage is highly desirable. Since power supplies sometimes fluctuate, a solution is needed. A method called current source self-biasing will be introduced in this section that improves upon these design parameters [1].

2.2.3.1 β Multiplier Referenced Self-Biasing

The design technique that will be utilized in the final current reference is called β multiplier referenced self-biasing. As the name indicates, this is a self-biasing technique that will improve upon power supply dependency. A simple β multiplier referenced self-biasing circuit is shown in Figure 4. This circuit structure with source degenerated (by resistor 'R') output device (M2) that is referred to as a simple β multiplier is loaded by a

simple NMOS current mirror loaded by a simple PMOS current mirror with an additional mirroring device (M6) to copy I to the reference's output. A resistor has been attached between the source of M_2 and V_{SS}. Also, the transistor M_2 has been sized a factor of K times the size of M_1. Normally, the lengths are equal and the width of M_2 is K times the width of M_1. From looking at Figure 4, it can be seen that the gate to source voltage of M_1 is equal to the gate to source voltage of M_2 plus the voltage across the resistor. This is described mathematically in equation 2.11.

$$V_{GS,M1} = V_{GS,M2} + IR \tag{2.11}$$

All of the transistors in the β multiplier must remain in saturation, so the gate to source voltages may be written in terms of their transistor's drain current as follows. Assuming strong inversion saturation operation, then,

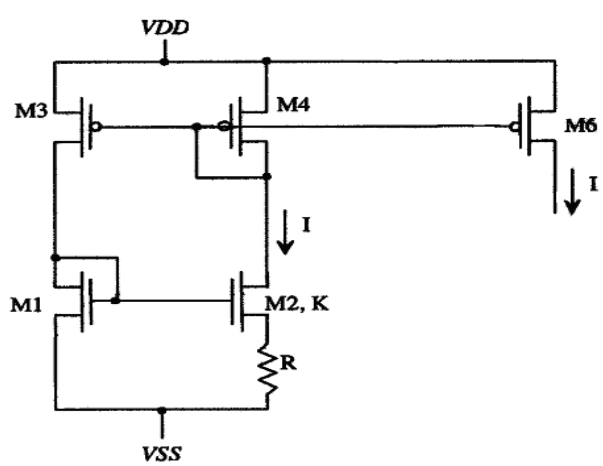

Figure 4: β Multiplier Current Reference (Start-Up Circuit Not Shown) [1]

$$V_{GS,M1} \cong \sqrt{\frac{2I}{\beta_1}} + V_{THN} \text{ and } V_{GS,M2} \cong \sqrt{\frac{2I}{K\beta_1}} + V_{THN} \qquad (2.12)$$

where K is a multiplying factor for the width of M_2 and $I = I_{D_1} = I_{D_2}$ due to the PMOS current mirror (neglecting body effect, channel length modulation, and mobility modulation). Using equations 2.11 and 2.12 and solving for I,

$$I = \frac{2}{R^2\beta_1}(1 - \sqrt{\frac{1}{K}})^2 \qquad (2.13)$$

As can be seen in equation 2.13, the output current has no dependency on power supply voltage. It only depends upon the resistor value R and the sizing of the transistors. Equation 2.13 reveals also that there is a temperature dependency because R and β are temperature dependent [1]. The temperature dependency of I is quantified by the reference circuit's temperature coefficient [1].

The temperature coefficient determines how much the output current varies over temperature, typically provided in units of $\frac{ppm}{°C}$. Equation 2.14 shows the temperature coefficient for the β multiplier of Figure 4 [1].

$$TC_I = \frac{1}{I}\frac{\partial I}{\partial T} = -2\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1}{K_p(T)}\frac{\partial K_p(T)}{\partial T} \qquad (2.14)$$

For an n-well resistor, the resistor potion of this equation is -4,000 ppm/degC. Also, the transconductance parameters of the transistors affect the overall *TC*. This part of the *TC* is equal to the inverse of the $K_P(T)$ value multiplied by the change in the transconductance with change in temperature. This gives a value of $\frac{1.5}{T}$. So, the final temperature coefficient of the β multiplier in terms of its output current is seen in equation 2.15.

$$TC_I = -4{,}000\ \frac{ppm}{°C} + \frac{1.5}{T} \tag{2.15}$$

Using typical values, a β multiplier at 300 K, or room temperature, has a TC of 1,000 ppm/degC. This means that the current will increase by 0.10 % for each degree Celsius 300 K [1]. Predictions for the output current at different temperatures can be found using the following equation.

$$I_o(T) = I_o(T_o)(1 + TC(I_o)(T - T_0)) \tag{2.16}$$

Using 27 $°C$ (300 K) for T_0, the current can be found to be 19.46 μA at 0 $°C$ and 21.46 μA at 100 $°C$ where $I_o(T_o)$ is 20μA

So, the β multiplier current reference has been shown to have no power supply dependency (theoretically) and a moderate temperature dependency. Since these are both very desirable characteristics, this circuit is a good basis for the current reference design

of this work. But, the simple β multiplier in Figure 4 has a low small-signal output resistance of just r_O. It does have a low output voltage constraint, but a circuit is needed that has a low $V_{o,\ min}$ and a high output resistance. The next chapter will show how a β multiplier can be improved upon to fulfill all of the needed design parameters.

Chapter 3

Designing Wide-Swing Cascode Current References

3.1 Introduction

The previous chapter covered basic building blocks of current reference design. Two very important circuits were introduced that will be used in this chapter to form a wide-swing high output resistance current reference.

3.2 Designing a Wide-Swing, High Output Resistance β Multiplier

At the end of chapter 2, the β multiplier current reference was introduced. Using a technique called self-biasing, this circuit provides a current reference that has low dependency on power supply and temperature variations. However, the simple β multiplier introduced does not have both high output resistance and a low output voltage constraint. This section will use some circuit design techniques, also covered in chapter 2, that will convert the simple β multiplier into a wide-swing, high output resistance β multiplier that still has the same dependency on power supply and temperature variations.

3.2.1 Setting Current Value

Before any changes are made to the basic β multiplier, which is seen in Figure 4, the process of setting the desired output current value will be discussed. For this work, an output current value of 20 μA is selected. Rearranging equation (2.13), the needed resistor value to implement this amount of current can be found.

$$R^2 = \frac{2}{(20\mu A)\beta_1}\frac{1}{K} \tag{3.1}$$

This theory is based on strong inversion saturated transistors where β_1 is determined by the sizing of M_1. K is determined by $\frac{W_2}{W_1}$ (an integer value) and should not be greater than 4 because it then becomes difficult to maintain both M_1 and M_2 in strong inversion saturation. L1 and L2 are equal and it is desired to have M1 and M2 in same inversion level for good matching [1].

Transistor sizing is the next design factor that must be discussed. When designing current mirrors, the transistors are sized to achieve strong inversion saturation and matching at the desired current. But with the β multiplier the output current is determined by the resistor value and the ratio $K(\frac{W_2}{W_1})$ using Figure 4. For this design, K is equal to four. The proper sizes for the basic β multiplier seen in Figure 4 were found using the inversion coefficient equation seen below [4].

$$\mathrm{IC} = \frac{I}{I_o(\frac{W}{L})} \tag{3.2}$$

I_o is called the technology current and typical values are 80 nA for PMOS transistors and 200 nA for NMOS transistors in this 0.5 μm CMOS process. In order for a transistor to be in strong inversion, the inversion coefficient, or *IC*, must be greater than or equal to ten. Using the typical NMOS technology current, M_1 was set to $(W/L)_1$ = (10μm/10μm), giving an inversion coefficient of 100. M_2 is *K* times larger, or $(W/L)_2$ = (40μm/10μm), with an inversion coefficient of 25. So, these sizes ensure that the transistors are well within strong inversion. They could have been sized even smaller and remained in strong inversion but they were sized to optimize matching. Thus, W_2 was implemented using *K* gate fingers in parallel where each gate finger aspect ratio equals $(W/L)_1$. As a result, W_2=*K*W and L_2=L_1. For our case, $(W/L)_1$ would be (2μm/10μm) with five parallel gate fingers and then 20 parallel gate fingers, each with (W/L)= (2μm/10μm) for M_2. In the schematic, m designates the number of parallel gate fingers.

The sizes for the PMOS bias current mirror are also found using the inversion coefficient equation. Using the typical PMOS technology current of 80 nA, M_3 is set to $(W/L)_3$ = (10μm/10μm) with m = 4 ($(W/L)_3$ total is (40μm/10μm)), giving an inversion coefficient of 63. M_4 and M_6 are sized exactly the same as M_3. So again, these transistors are well within the strong inversion saturation region. They are also sized for using convenient m factors. The PMOS current mirror is used both to provide the proper current bias for the NMOS β multiplier and to mirror the current to the output. So M_3, M_4, and M_6 must be the same size in order to keep the same current in all three legs of the

overall β multiplier circuit.

3.2.2 Converting β Multiplier to Wide-Swing Cascode

The β multiplier will now be converted to wide-swing with high output resistance. In chapter 2, a circuit was introduced called the wide swing cascode current mirror shown in Figure 3. This same technique will now be applied to the β multiplier in order to increase its' output resistance and maintain a low minimum output voltage. The first step in the conversion process is to think of the basic β multiplier, seen in Figure 4, as a basic current mirror. Then add on the cascode transistors and the diode connected (gate-to-drain) bias transistor as in the wide-swing cascode current mirror to M_1 and M_2. For the moment, the PMOS bias current mirror will be left as is.

Before moving on to the PMOS bias mirror, the transistor sizes of the wide-swing, high output resistance β multiplier must be discussed. The gate-drain connected bias transistor M_5 must still be about one-fourth the size of M_1, as in the wide-swing cascode current mirror. But in simulation, it has been found that it is better to size this transistor to one-fifth the size of M_1 to compensate for body effect in the cascode transistors. Since M_1 has a width to length ratio of (2μm/10μm) and *m* equal to 5, the gate-drain connected transistor is sized at (W/L) equal to (2μm/10μm) with *m* equal to 1. For accurate circuit performance, matching between M1 and M2 is critical. Matching between the cascode transistors is less stringent so a shorter L may be used. These cascode transistors are set to (W/L) equal to (8μm/2μm) with *m* equal to one. Also, a PMOS transistor M_6 has been added to mirror the β multiplier current to M_5. It is also

sized the same as the other PMOS transistors, or (W/L) equal to (10μm/10μm) and *m* equal to four.

The next step in the design process is to convert the PMOS current mirror bias into a wide-swing, high output resistance current mirror bias. This will cause the complete current source to maintain a low minimum output voltage and raise the output resistance. The PMOS bias current mirror can be converted to a wide-swing cascode current mirror using the same technique as that used for the NMOS mirror. The cascode transistors are added along with a gate-drain connected bias transistor. Of course, these are now PMOS. The gate-drain connected bias transistor must again be about one-fourth of the primary (topmost) PMOS. Since the primary PMOS has a width to length ratio of (10μm/10μm) and *m* equal to four, then the gate-drain connected transistor is sized at (10μm/10μm) with *m* equal to one. Once again, the cascode transistors need not be as large as the primary mirror transistors as long as they are in strong inversion saturation. They are both set to a width to length ratio of (8μm/2μm) with *m* equal to one. Also, as before, a bias transistor is needed for the gate-drain connected transistor of the PMOS mirror. This transistor is sized at (2μm/10μm) with *m* equal to five. In order to increase the output resistance, a cascode transistor has been added to the output transistor sized at (8μm/2μm) and *m* equal to one. The bias transistors for both the gate-drain connected transistors must also be cascoded. These are sized (8μm/2μm) with an *m* factor of one.

Utilizing all of these improvements, the wide-swing cascode β multiplier current reference can be seen in Figure 5. As mentioned earlier, one of the problems with implementing this circuit on-chip is the fact that resistor values can sometimes be as much as thirty percent off of their intended value. For the worst case of a fabricated on-

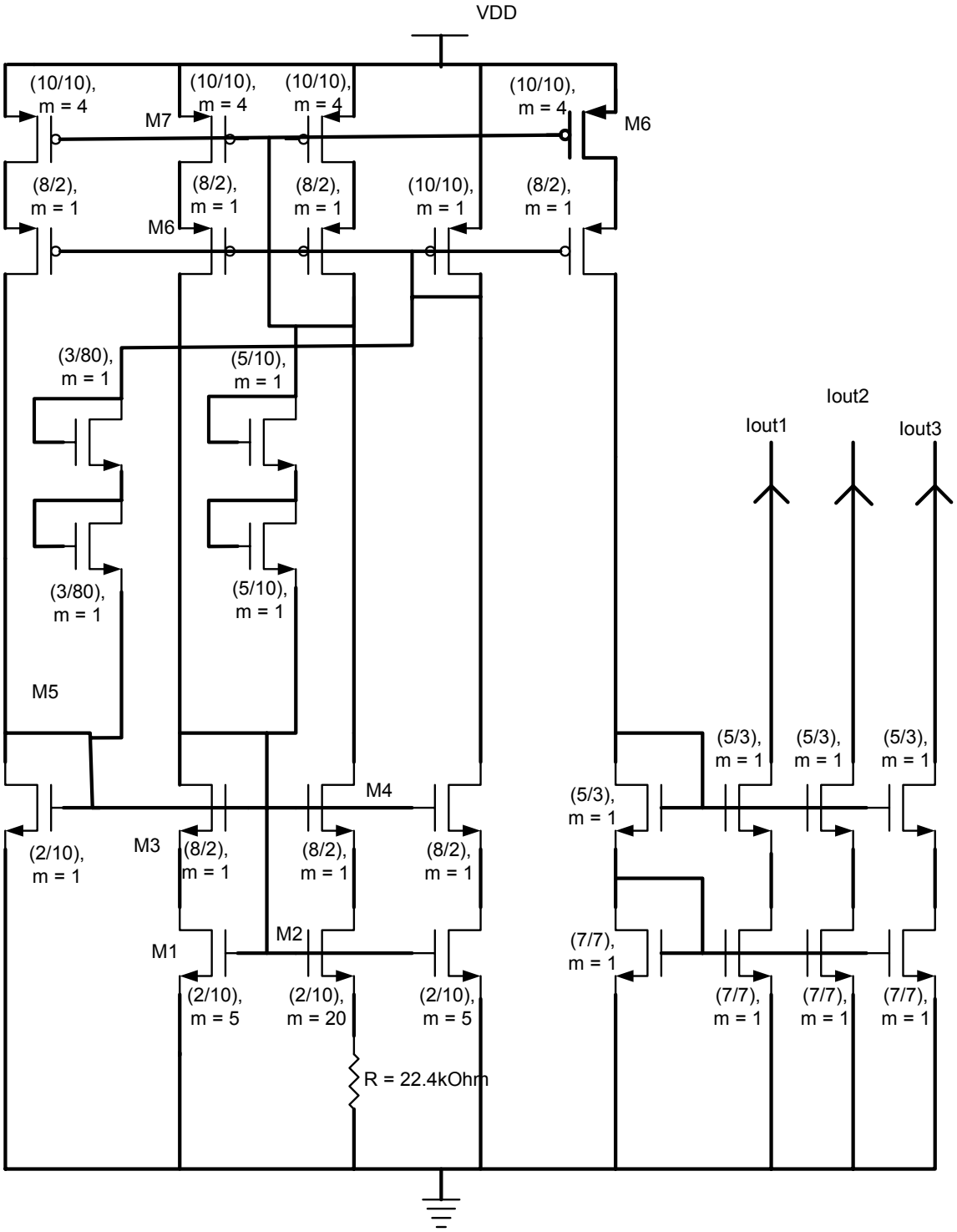

Figure 5: Wide-Swing Cascode β Multiplier Current Reference

chip resistor with 30 % error, the error in the output current can be found using the following equation for the β multiplier current.

$$I = \frac{2}{R^2 \beta_1}(1 - \sqrt{\frac{1}{K}})^2 \tag{3.3}$$

Using a resistor value that is 30 % lower than the original hand calculated value, or 15.7 kΩ, the expected output current will be 40.57 μA. This shows the very high dependence of the output current on the resistor value. A 30 % error in the resistor value doubles the output current.

There are four transistors in Figure 5 that have not yet been discussed. These are used in order to provide proper start-up operation for the circuit. The start-up circuitry consists of two pairs of two gate-drain connected transistors. Without the start-up transistors, the circuit would not operate properly. When the power supply is turned on, the start-up circuitry prevents the zero current condition that might otherwise occur [1]. The start-up transistors provide a current path between V_{DD} and V_{SS} to initiate circuit turn-on. These start-up transistors turn off once the desired quiescent point is reached. The positive feedback loop kicks off the start-up circuit. The loop gain magnitude of this loop is less than 1 to prevent oscillation at desired quiescent point.

In order to use the β multiplier current reference to bias other circuits, some output current mirrors must be added. As discussed in [1], multiple current mirrors can be connected in order to reproduce additional bias currents. A three-output NMOS current mirror may be connected to the output of the β multiplier current reference in

order to provide a current sink for three different circuits. These mirrors are cascoded in order to maintain a high output resistance. All of the added transistors are sized only to keep them in strong inversion saturation, with the cascode transistors smaller. Also, each output mirror is sized the same. This completes the design of the wide-swing cascode β multiplier current reference. A similar approach was used to develop a bandgap reference circuit by Wai-Tat-Wong.

3.3 Stability Analysis of Wide-Swing Cascode β Multiplier

In order for a circuit to be useful in practical applications, it is necessary that it be stable. A stability analysis will now be performed on the negative feedback loops in the wide-swing cascode β multiplier current reference seen in Figure 5 to ensure that it is stable. There are two negative feedback loops in the circuit that must be analyzed to insure stability. This analysis will be based on the NMOS negative feedback loop. Using the NMOS feedback loop seen in Figure 6, a two-pole transfer function for the loop gain can be found [30]. In Figure 6, the PMOS cascode of Figure 5 has been replaced by a DC current source I_{bias} equal to 20μA with an AC equivalent parallel resistance $(R_{eq,cascode})_p$. Also, the high frequency capacitances have been included for the frequency response analysis of the loop gain. C_{gd3} and the capacitances associated with the PMOS cascode have been neglected. The stability analysis will be performed from the derived two-pole loop gain expression. First, the expression for the midband loop gain will be represented as the multiplication of the gains around the loop as seen in the following equation.

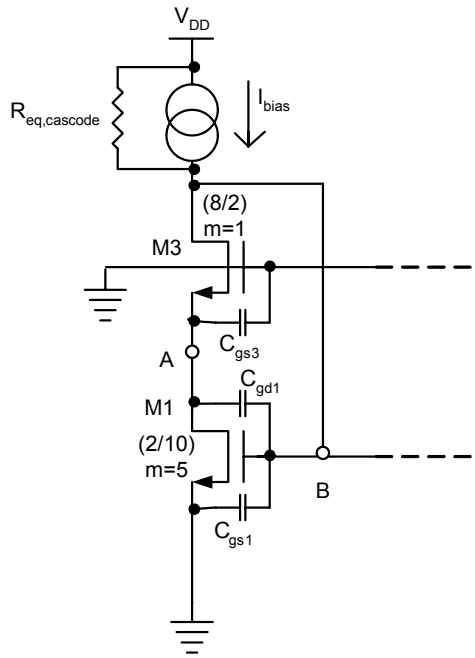

Figure 6: NMOS Negative-Feedback Loop

$$T_{Midband} = A_{V_1}(Common - Source)A_{V2}(Common - Gate) \tag{3.4}$$

The gain of the Common-Source amplifier M1 is expressed in equation 3.5.

$$A_{V_1} = -g_{m,M1}(R_{in,Source,M3} \parallel r_{O,M1}) \cong -g_{m,M1}[\frac{1}{g_{m,M3}}(1+\frac{R_{eq,Cascode}}{r_{O,M3}}) \parallel r_{O,M1}] \tag{3.5}$$

Also, the gain of the Common-Gate amplifier M3 is shown in equation 3.6.

$$A_{V_2} = \frac{g_{m,M3} R_{eq,Cascode} + \frac{R_{eq,Cascode}}{r_{O,M3}}}{1 + \frac{R_{eq,Cascode}}{r_{O,M3}}} \tag{3.6}$$

So, the midband loop gain reduces to equation 3.7.

$$T_{mid} \cong -g_{m,M1}(R_{eq,Cascode})_p \parallel (R_{eq,Cascode})_n = -357 \ \frac{V}{V} \tag{3.7}$$

Next, the two high frequency poles must be found. These poles occur at node A and node B as seen in Figure 6. The pole at node A will be found first. Equation 3.8 shows the time constant at this node.

$$\tau_A = R_A C_A = [r_{o,M1} \parallel \frac{1}{g_{m,M3}}(1 + \frac{(R_{eq,Cascode})_p}{r_{O,M3}})][C_{gs3} + (\frac{C_{gs1} C_{gd1}}{C_{gs1} + C_{gd1}})] \tag{3.8}$$

The pole at node A is approximated using small-signal parameters predicted by simulation.

$$f_{p,A} = \frac{1}{2\pi\tau_A} = \frac{1}{2\pi[r_{O,M1} \parallel \frac{1}{g_{m,M3}}(1 + \frac{R_{eq,Cascode}}{r_{O,M3}})][C_{gs3} + (\frac{C_{gs1} C_{gd1}}{C_{gs1} + C_{gd1}})]} \tag{3.9}$$

$$f_{p,A} = 13.84 \text{ MHz}$$

Similarly, the time constant and pole at node B are shown in equations 3.10 and 3.11.

$$\tau_B = R_B C_B = ((R_{eq,Cascode})_p \parallel (R_{eq,Cascode})_n)(C_{gs1} + C_{gd1}(1+|A_1|)) \tag{3.10}$$

$$f_{p,B} = \frac{1}{2\pi\tau_B} = \frac{1}{2\pi[(R_{eq,Cascode})_p \parallel (R_{eq,Cascode})_n][C_{gs1} + C_{gd1}(1+|A_{V_1}|)]} \tag{3.11}$$

$$f_{p,B} = 10.7 \text{ kHz}$$

In calculating the poles, $(R_{eq,Cascode})_p$ was found to be 7.6 MΩ through .tf analysis in simulation and $r_{o,M1}$ was found to be 1.25 MΩ. For all calculations, typical parameters for this 0.5 μm process are used. In calculating the small signal transistor output resistances, different values for the channel length modulation parameter were used depending on the length of the device. As channel length increases, channel length modulation decreases. The midband loop gain and the two poles can now be used to form the two-pole loop gain expression seen in equation 3.12.

$$T = T_{mid}\left(\frac{1}{1+j(\frac{f}{f_B})}\right)\left(\frac{1}{1+j(\frac{f}{f_A})}\right) = -357\left(\frac{1}{1+j(\frac{f}{10.7kHz})}\right)\left(\frac{1}{1+j(\frac{f}{13.84MHz})}\right) \tag{3.12}$$

Stability can be determined from equation 3.12 using estimation techniques described in [30]. Two parameters that can be used to determine stability are the natural frequency and the damping ratio as seen in the following equation.

$$f_n = \sqrt{f_B f_A (1 + |T_{mid}|)} \text{ and } \zeta = \frac{(f_B + f_A)}{2 f_n} \tag{3.13}$$

The natural frequency and the damping ratio can be used to find the phase margin as in equation 3.14. The phase margin is a measure of stability for a given negative feedback loop.

$$P.M. = \tan^{-1}\left(\frac{4\zeta^2}{\sqrt{4\zeta^4 + 1} - 2\zeta^2}\right)^{\frac{1}{2}} = 75° \tag{3.14}$$

Phase Margin, or P.M., is defined as the difference between the phase of the loop gain and $-180°$ when the magnitude of the loop gain is unity [30]. A phase margin greater than $0°$ is needed for a system to be stable but at least $45°$ is desired. Most designs require $60°$ in order to eliminate overshoot in the transient response. The percentage of overshoot in the transient response can be found using the following equation.

$$M_{pt} = 100 e^{-\left(\frac{\pi\zeta}{\sqrt{1-\zeta^2}}\right)} = .007\% \text{ Overshoot} \tag{3.15}$$

This system is very stable, having a phase margin of only .007° . Although it is not applicable in this case, dominant pole compensation could be used to improve the phase margin by adding capacitance to node B, the highest resistance node in this loop [30]. A similar analysis can be applied to the PMOS wide-swing cascode negative feedback loop.

3.4 Layout of the Wide-Swing Cascode β multiplier

Once the design was completed, the next step was to layout the wide-swing cascode β multiplier current reference. Figure 7 shows the layout of the wide-swing cascode β multiplier done using the Cadence Virtuoso layout tool. The use of m number of parallel transistors to create one can be seen.

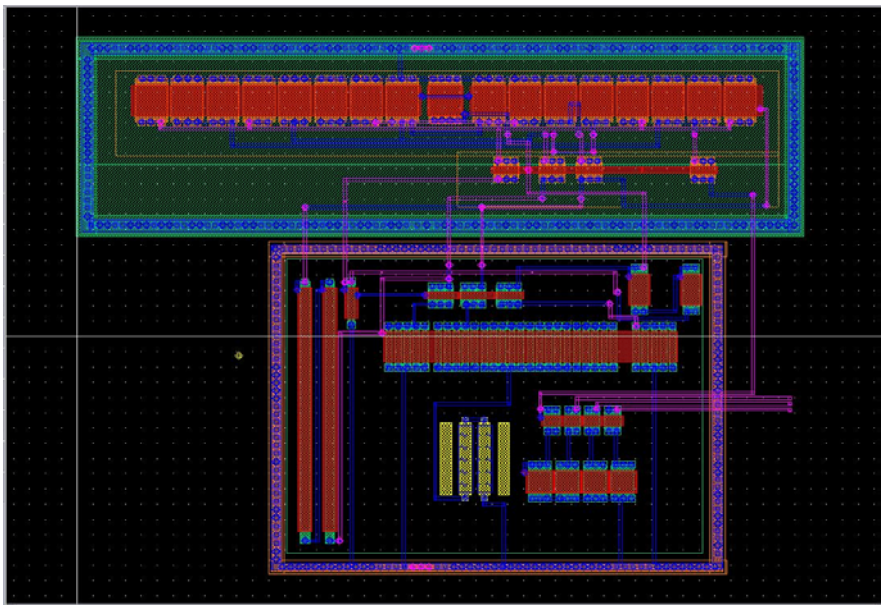

Figure 7: Layout of Wide-Swing Cascode β Multiplier Current Reference

Chapter 4

Current Reference Simulation Results

4.1 Introduction

This chapter will cover the simulation of the wide-swing cascode β multiplier current reference. All simulations were done using Figure 8 below. As can be seen from Figure 8, the resistor value is smaller than that found in hand calculations. This is caused by the body effect of the transistors, which was neglected in the hand calculations. The resistor was manually adjusted in simulation in order to get a current value of 20 μA.

4.2 Simulation Methodology

The wide-swing cascode β multiplier current reference has been simulated to determine several important design characteristics. These include output current under a DC sweep on the output, start-up, and determination of stability. All of these simulations were done over three different temperatures using a typical model for this standard 0.5 μm CMOS process. The three temperatures used were $0\ ^{\circ}C$, $27\ ^{\circ}C$, and $100\ ^{\circ}C$.

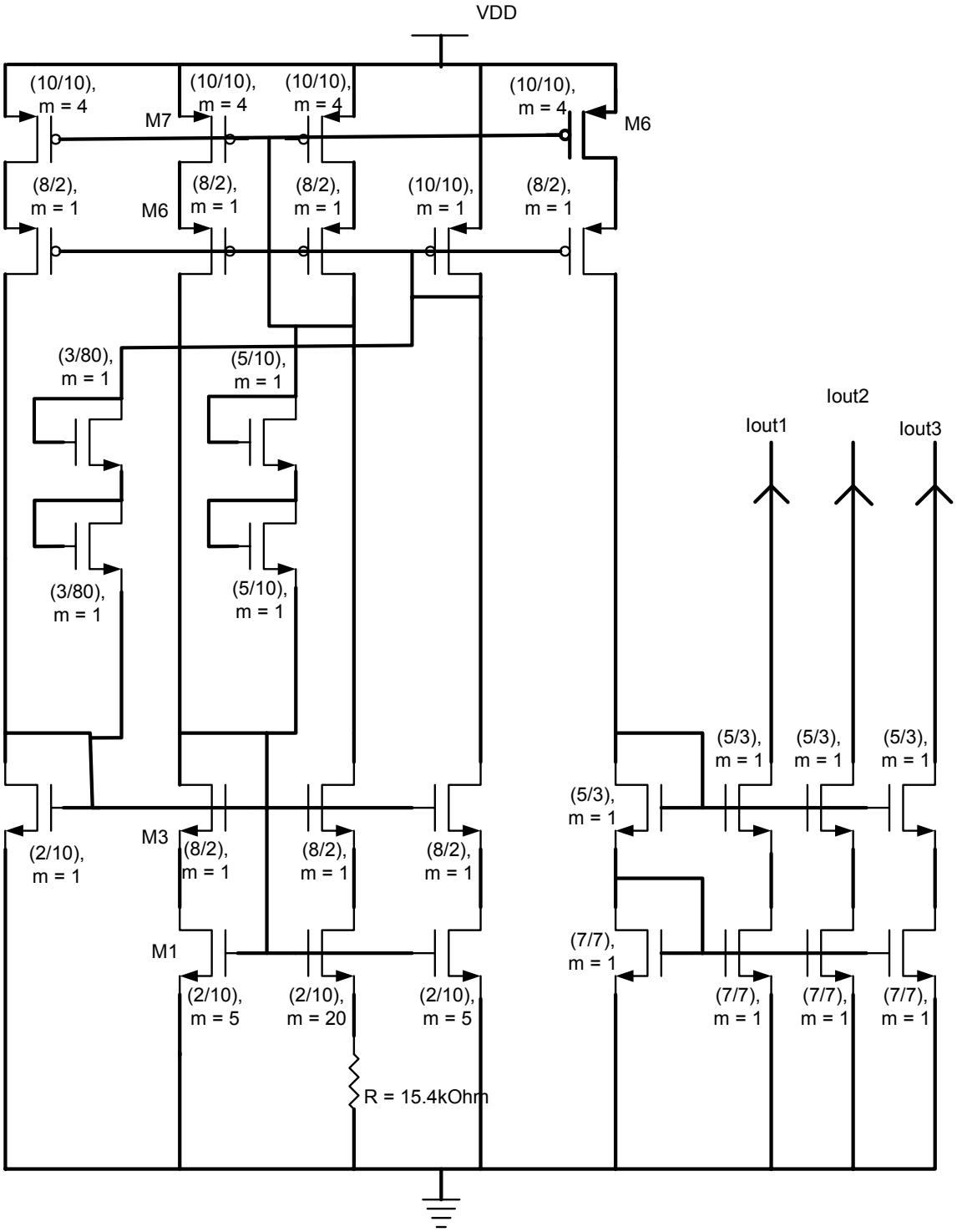

Figure 8: Current Reference Schematic for Simulations

4.3 Simulation Results

4.3.1 DC Output Voltage Sweep

First, the output current is plotted as the output voltage is swept from 0 to 5 V. The output voltage sweep can be seen in Figure 9. Figure 9 also shows the output current of the β multiplier versus output voltage for three different temperatures. It can be seen that there is an increase in current as the temperature is increased. The output current is around 19.4 μA at room temperature. At 0C, the current is still fairly close at 18 μA. However, at 100 C, the current is quite high at 25.2 μA. These values vary more than predicted by the temperature analysis in chapter 2. The major cause of the current change with temperature is due to the fact that resistance value changes with temperature. Since the resistor in this circuit directly affects the output current, this is a concern. A solution to this problem would be a programmable resistor that maintains the desired output current value as temperature is changed. Also in Figure 9, the minimum output voltage can be seen. The point where the current leaves the saturation region is the point where there is no longer enough output voltage left to keep the output transistors in saturation. From the plot, the minimum output voltage is approximately 0.7 V. Hand calculations predicted 0.74 V, so this is very close.

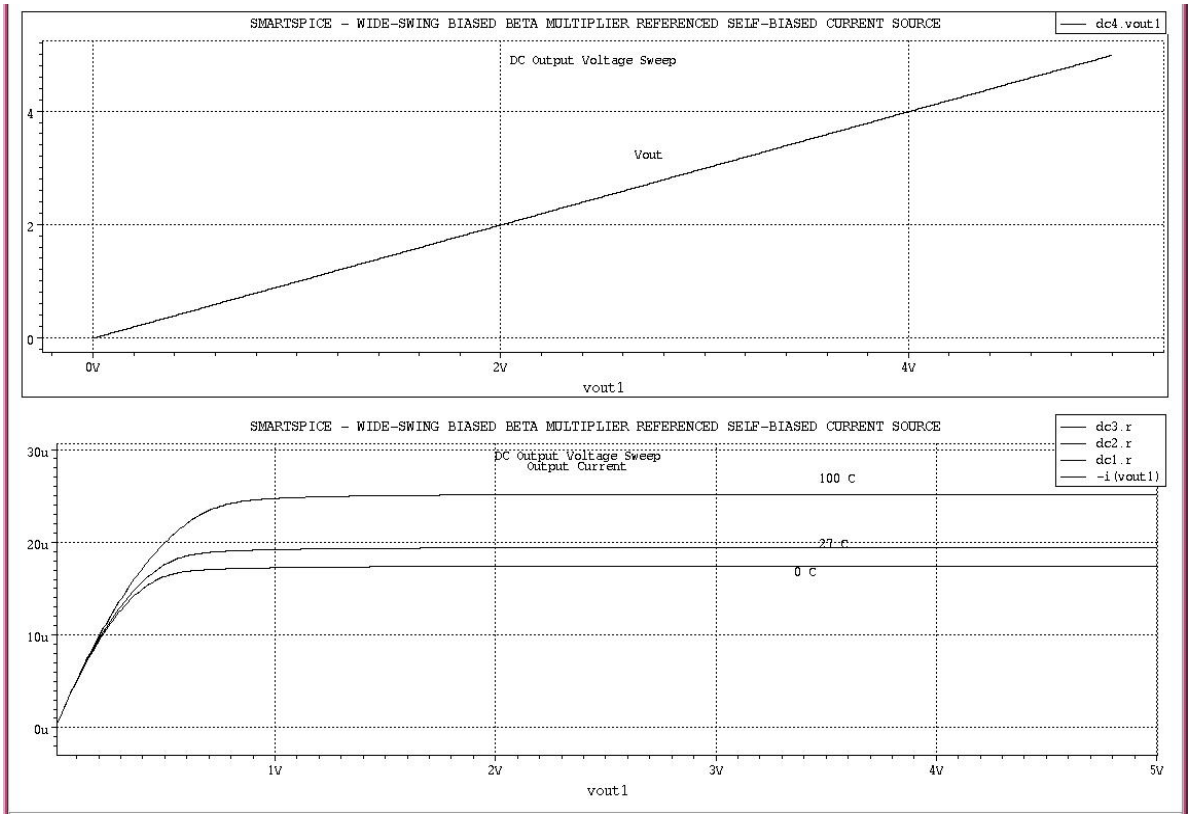

Figure 9: DC Output Voltage Sweep at Temperatures $0\,°C$, $27\,°C$, and $100\,°C$

4.3.2 Start-Up Simulations

The next simulation ran on the β multiplier were the start-up tests. For the first start-up test, a piece-wise linear voltage source was used to slowly raise the V_{DD} power supply from 0 to 5 V as seen in Figure 10. A 10 μs delay was used before the power supply began to turn on in order to allow the circuit to reach a stable quiescent point. Figure 10 also shows that the circuit starts up successfully at all three temperatures. Again, the output current increases with increasing temperature. V_{DD} was raised from 0 to 5 V starting at 10 us and ending at 100 μs. The output current reaches its desired value at approximately 93 μs, which means that the output transistors are saturated at this point. The output current goes from zero to its desired output in about 3.5 μs.

For the second start-up test, the power supply was kept at 5V, but initial conditions were used to set the current through the β multiplier to zero. The output current was then plotted to ensure that the start-up circuitry properly caused the circuit to produce the desired output current. A plot of the output current can be seen in Figure 11. As can be seen from the plot, the start-up circuits forced the β multiplier transistors into strong inversion saturation producing the desired output current. The circuit started up in only 2.5 μs.

4.3.3 Stability Simulations

For the stability simulation, a small transient current will be inserted into each of the negative feedback loops. There is one negative feedback loop in the PMOS bias and one

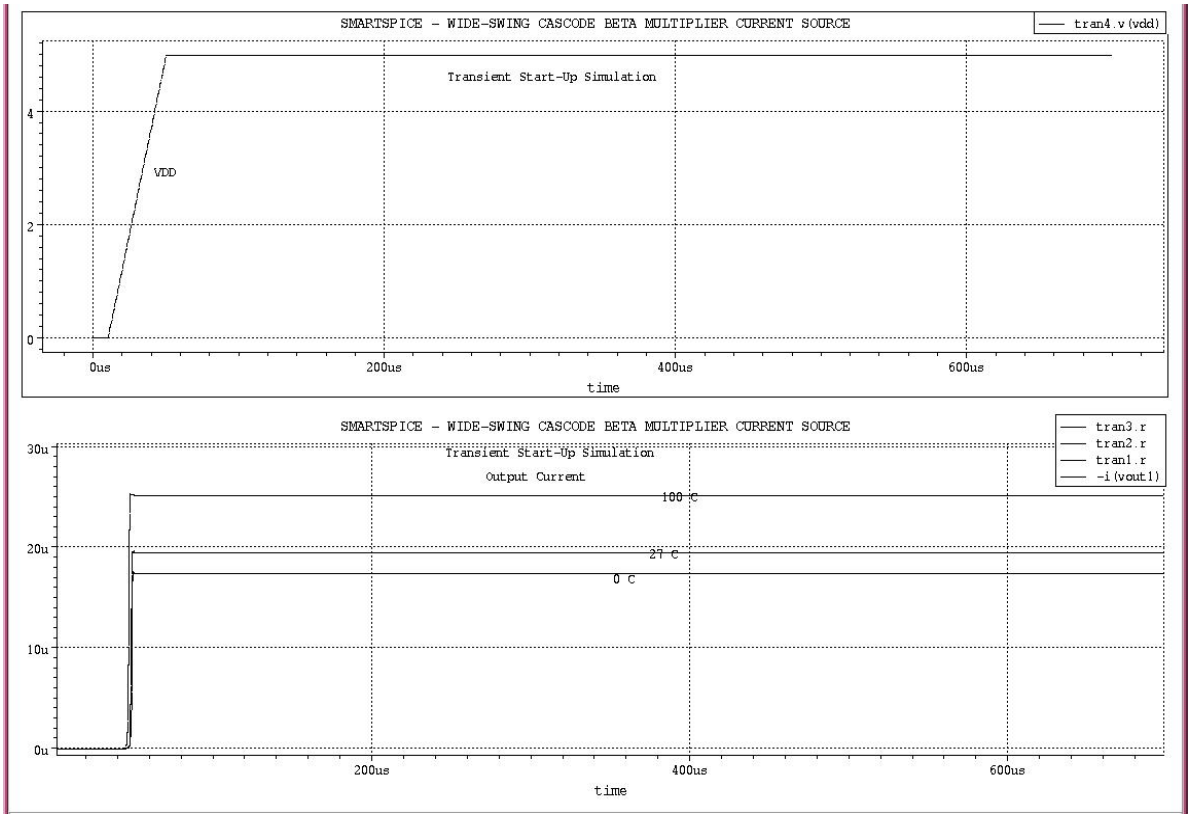

Figure 10: Transient Start-Up Simulation

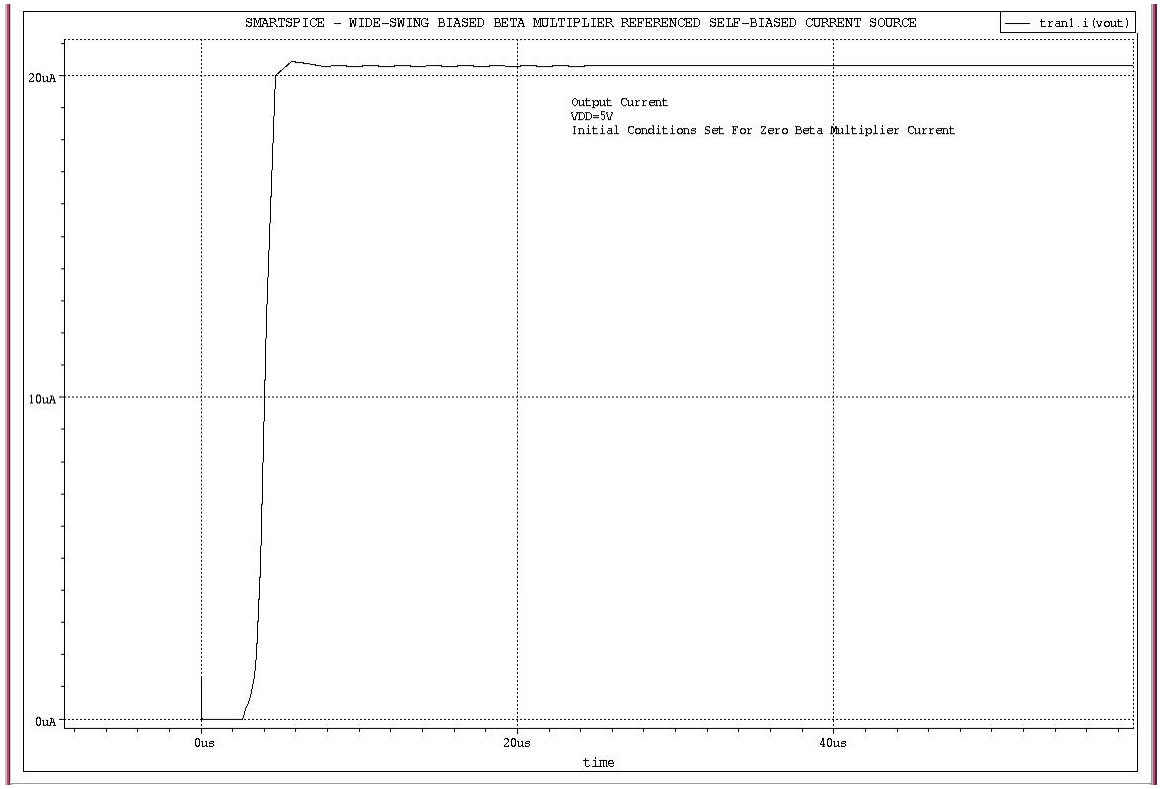

Figure 11: Start-Up Test With Zero Initial Current

negative feedback loop in the NMOS current source. Then, the voltage at the output of each feedback loop was plotted over time. The current was applied at 100 μs as shown in Figure 12. A schematic of the β multiplier current reference showing the transient input currents and the output voltages for the stability simulation is given in Figure 13. The output voltage of the NMOS feedback loop at the three temperatures is shown in Figure 14. Also, the output voltage of the PMOS feedback loop for the three temperatures is shown in Figure 15. For each plot in Figures 14 and 15, a step in voltage can be seen centered at the point when the current was added. As can be seen from all of the plots, there is a very small amount of overshoot and ringing on the loop outputs over all three temperatures. Also, from the start up test with zero current initial conditions seen in Figure 11, only a small amount of overshoot and ringing can be seen in the output current. So, this circuit should be stable. These results are within 10% of the calculations in chapter 3.

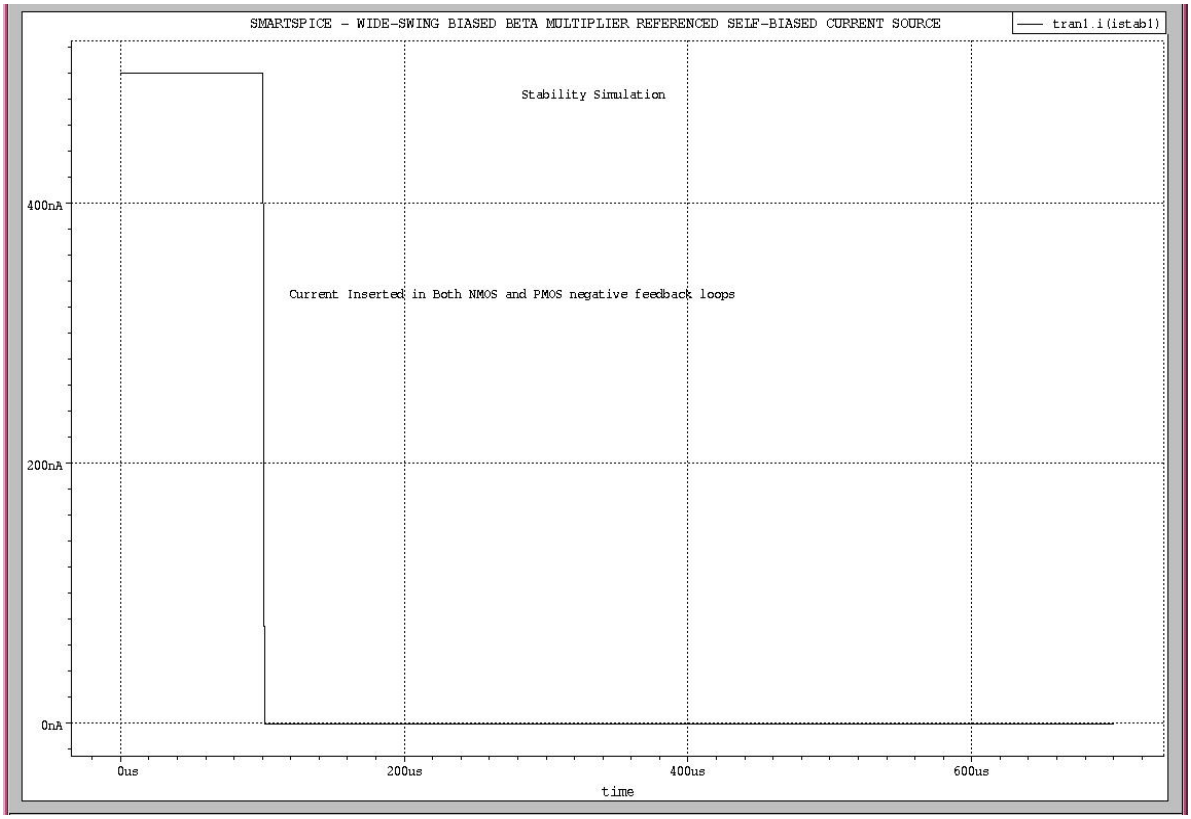

Figure 12: Current Inserted For Stability Simulations.

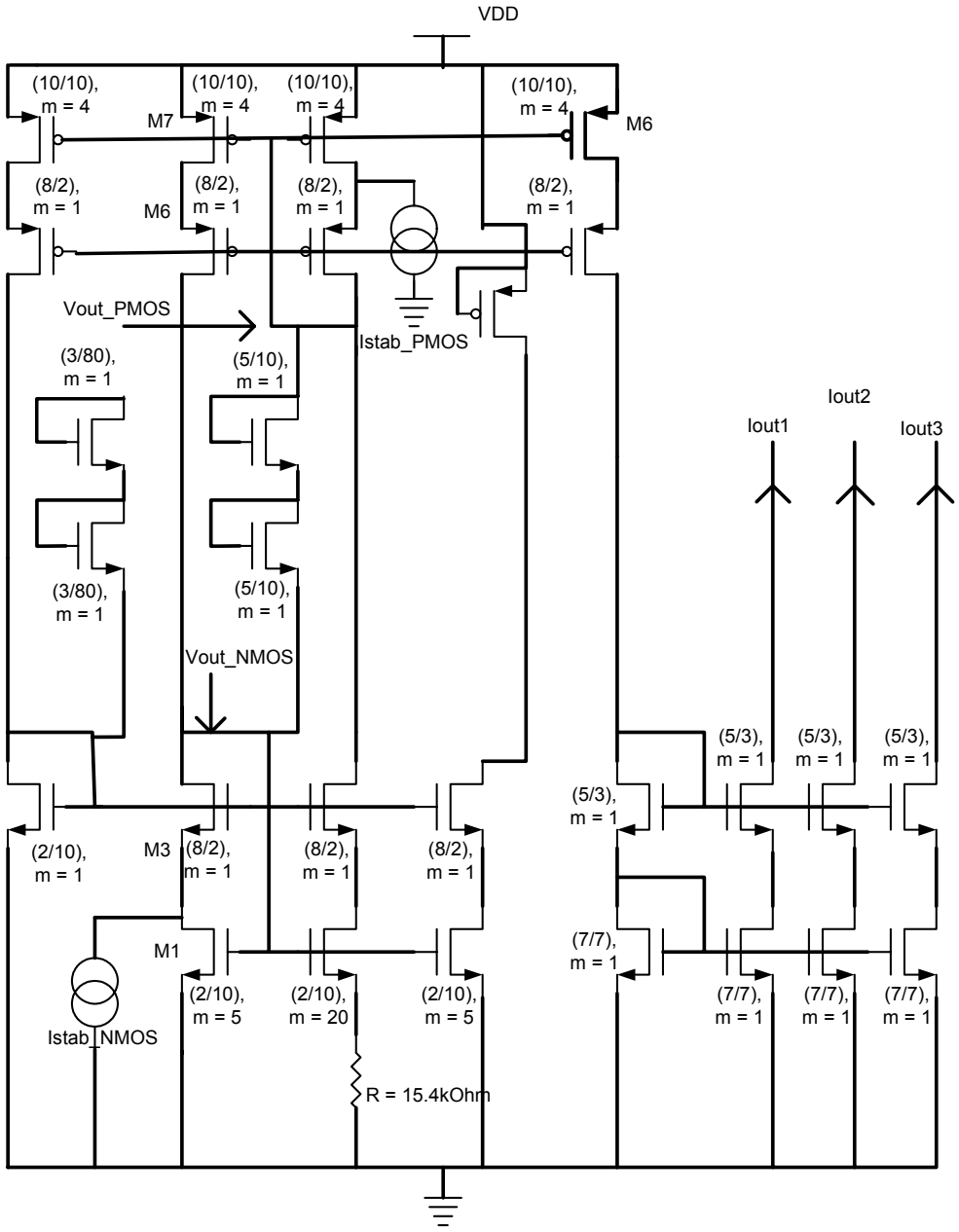

Figure 13: Schematic for Stability Simulations

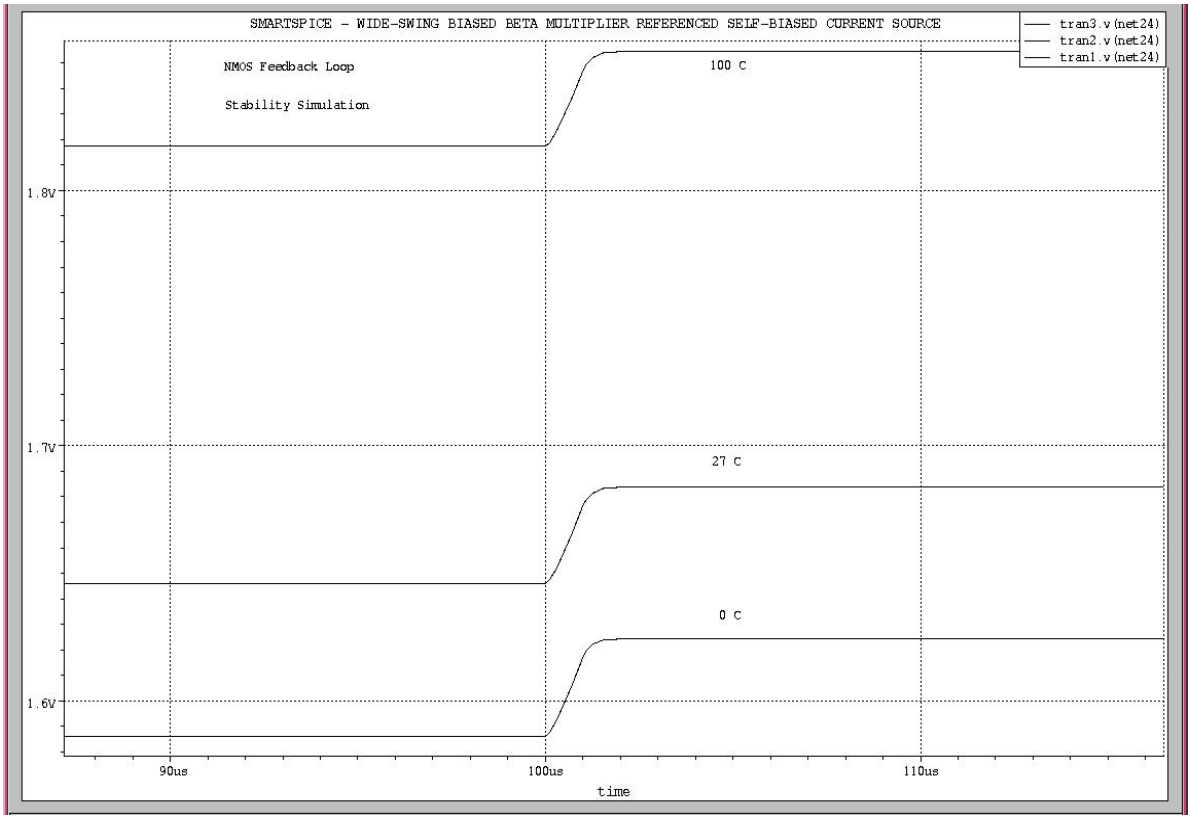

Figure 14: Stability Simulation of NMOS Feedback Loop.

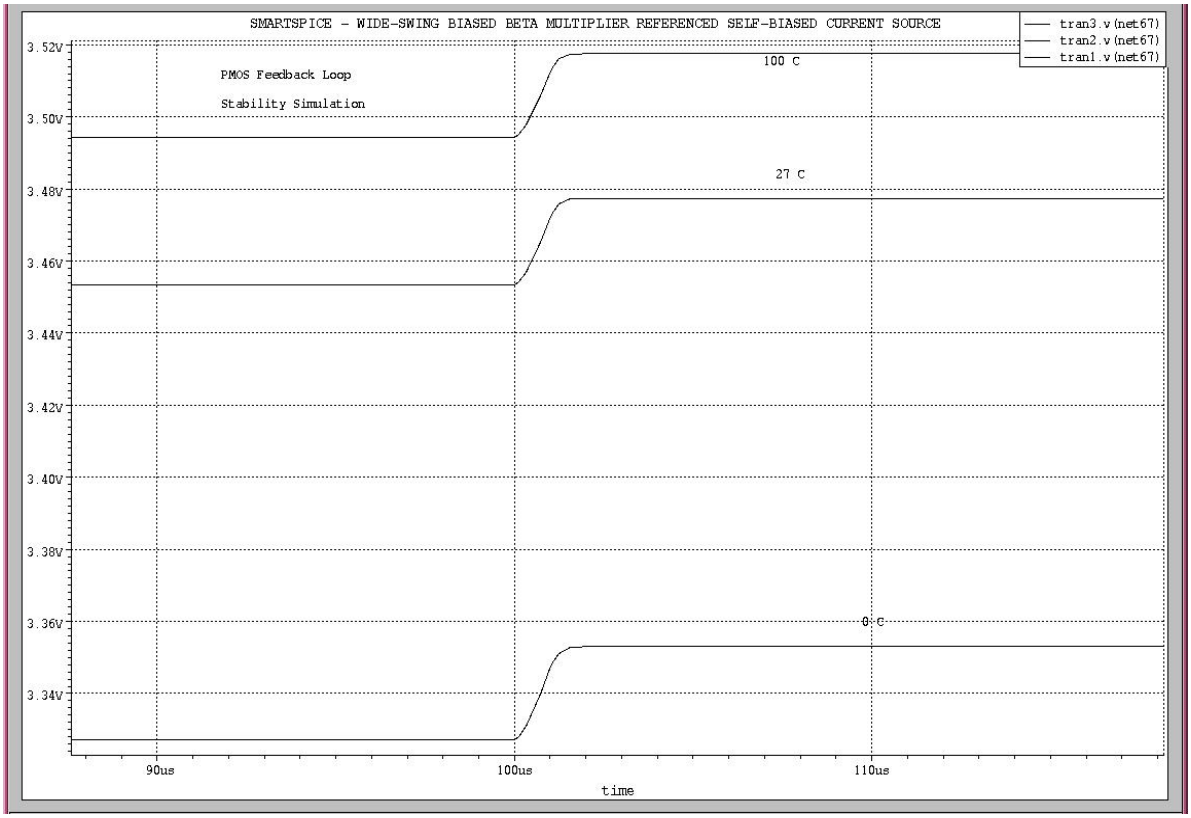

Figure 15: Stability Simulation of PMOS Feedback Loop.

Chapter 5

Current Reference Measured Results

5.1 Introduction

This chapter will include the measured results of the major concepts covered in this thesis. Included are the testing procedure and the measured results of the fabricated β multiplier current reference.

5.2 **Testing of the Fabricated Wide-Swing β Multiplier**

After all of the design, layout, and simulation of the wide-swing β multiplier was completed, the circuit was fabricated by MOSIS in an AMI 0.5 μm process. Tests were performed on the fabricated chips in order to determine several important characteristics of the design.

5.2.1 Testing Methodology

In order to determine the chip's operation at different temperatures, socketed chips were placed in a temperature chamber. The wires soldered to the socket were fed out of the temperature chamber and connected to a breadboard. Then, a power supply was connected to the breadboard. A Keithley meter was connected to the output of the β

multiplier current reference on the breadboard. The Keithley meter, along with a PC running LabView, was used to perform a DC voltage sweep on the output and measure the output current. The test setup can be seen in Figure 16.

5.2.2 Measured Results

5.2.2.1 DC Output Voltage Sweep

Using the Keithley meter and the temperature chamber, a DC voltage sweep was done on four chips. Each chip was tested at three temperatures. These temperatures were 0 C, 27 C, and 100 C. The resulting measurements are shown in Figure 17. As seen in Figure 17, all four chips performed almost the same. The largest variation is at 27 C. The average output current for this temperature is 37 μA compared to the simulations, which are shown in black in Figure 17. So, as predicted, there is a large error in output current due to the tolerance of fabricated resistors. The predicted worst-case output current, from chapter 3, was 40 μA. So, the error is not quite worst case. A solution to correct the resistor tolerance error would be to implement a programmable resistor that allows adjustment of the resistor value. Also, as can be seen in Figure 17, there is a large change in the β multiplier current due to temperature variation. At 0 C, the average output current for the four chips is 30 μA. The average current at 100 C is 50 μA. The same programmable resistor can be used to compensate for temperature variation errors. Another observation that can be made from Figure 17 is the fact that the fabricated β multiplier does indeed have a high output resistance due to the almost constant current

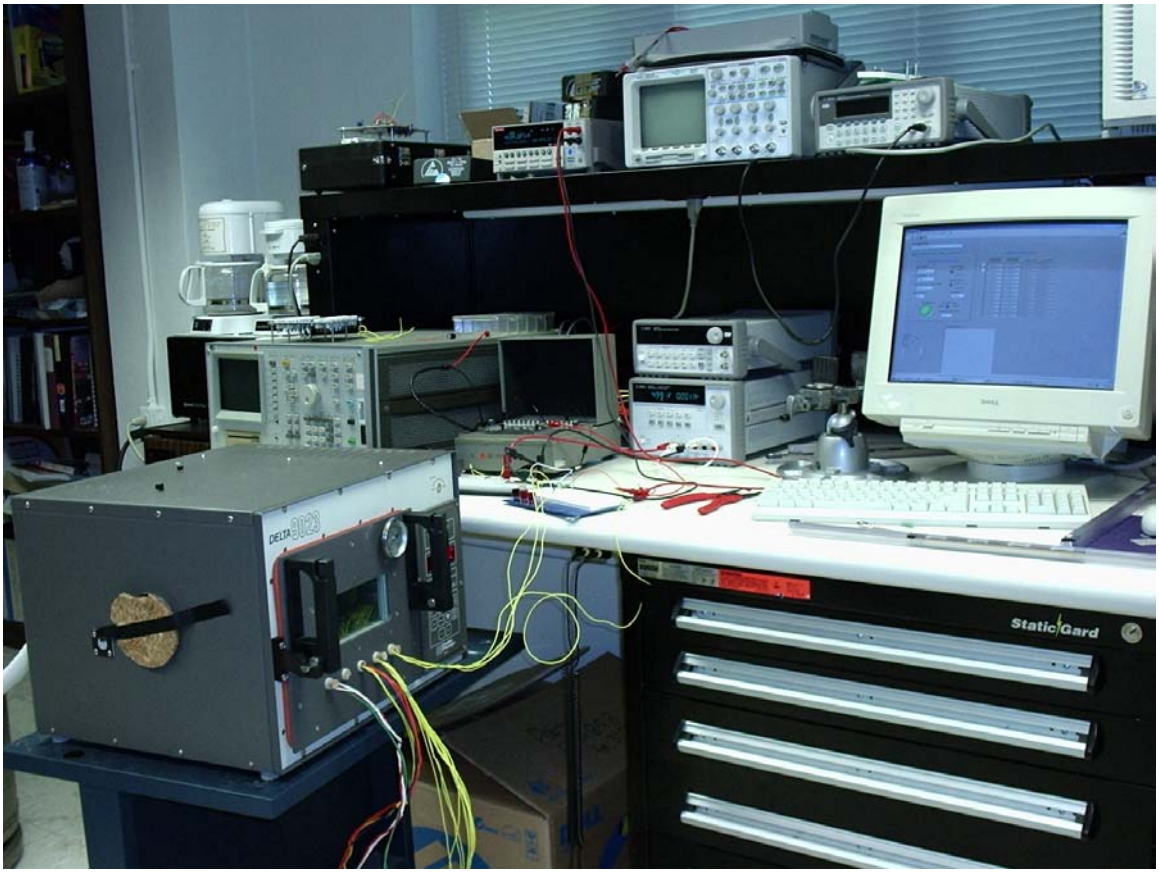

Figure 16: Test Setup for Output DC Voltage Sweep

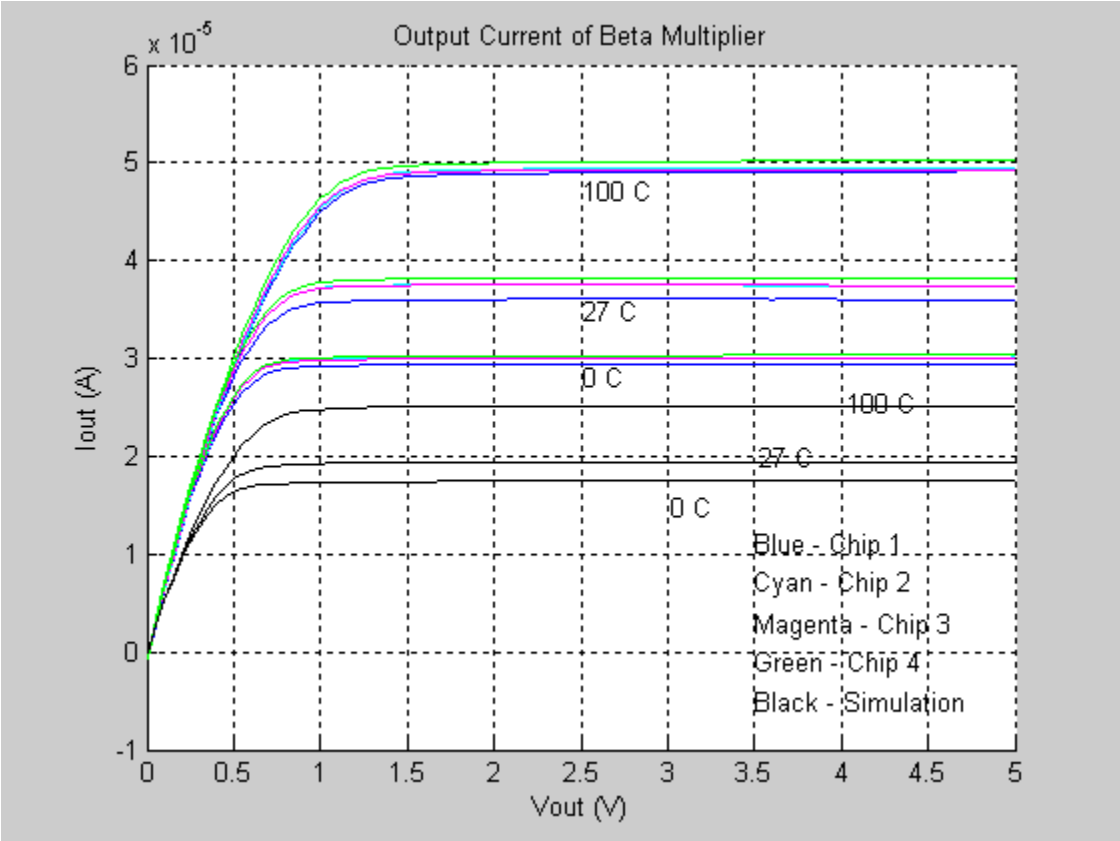

Figure 17: Measured Output Current of the Fabricated β Multiplier

over the output voltage sweep. Also, since the output current reaches its saturated value at an average of 0.7 Volts at room temperature, the fabricated current reference has a wide output voltage swing. The hand calculated value for the minimum output voltage swing was 0.74 V at 27 C, so the fabricated chips operate as predicted.

Unfortunately, stability of the negative feedback loops could not be measured. Internal pad connections to these loop outputs could have been added in order to measure stability by looking at the transient response of these voltages. However, since the output current from the DC output voltage sweep remains relatively constant, the system is stable. But, the phase margin cannot be measured without internal pad connections to the negative feedback loop outputs.

5.2.2.2 DC Start-Up Test

The second test performed on the fabricated β multiplier was a start-up test. A DC voltage sweep was performed on the power supply as the output voltage was held at a constant potential to keep the output saturated. Figure 18 shows the output current of three chips as the power supply voltage is swept from 0 to 6 Volts. Figure 18 shows that approximately 4.5 Volts is needed on the power supply before the fabricated β multiplier will reach its' desired output current level. All four chips have very similar curves. Also note that the four chips used for this test have output currents that are much closer to the desired value. These chips averaged around 25 μA, compared to 37 μA for the other chips.

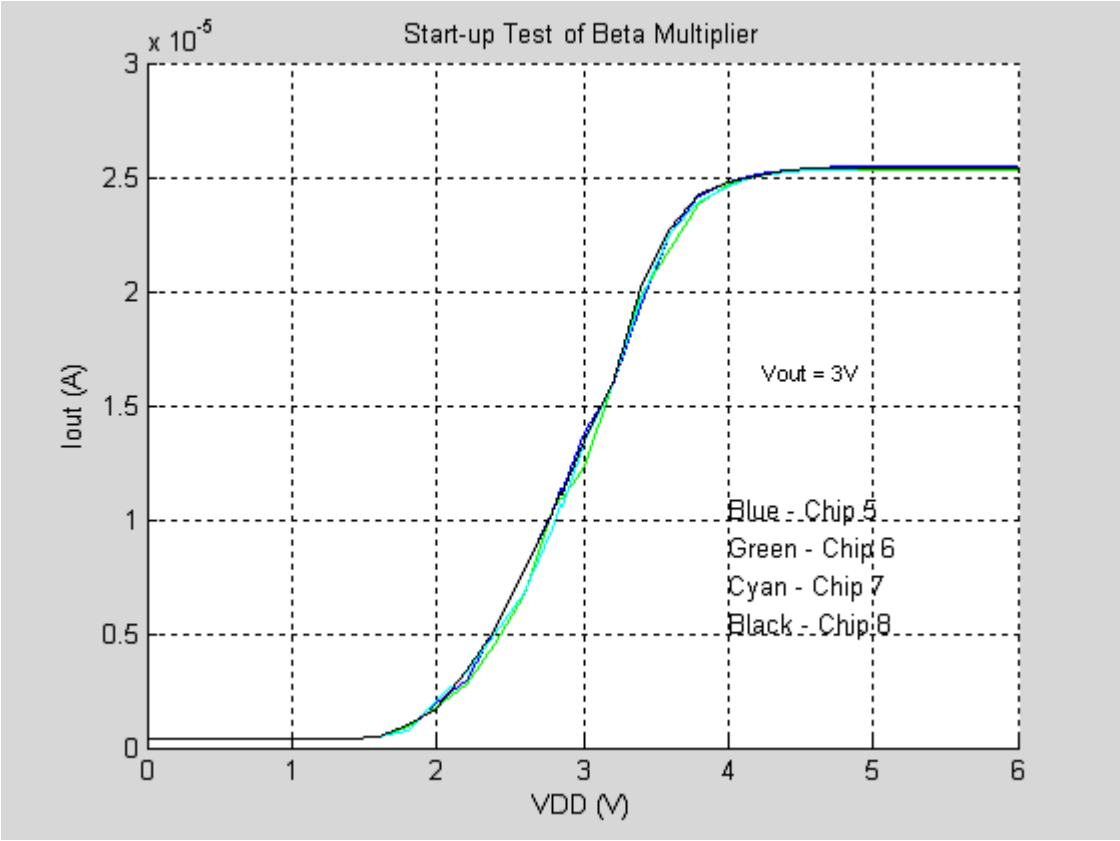

Figure 18: Output Current of Fabricated β Multiplier over Power Supply Sweep

5.2.2.3 Temperature Sweep

The third test performed on the β multiplier was a test to determine how the output current changes over temperature variation. Figure 17 shows the current at three discrete temperatures over an output voltage sweep. But, this new test shows the saturated output current of the β multiplier over a temperature sweep from 0 C to 100 C. The results are shown in Figure 19. Figure 19 shows that the current is around 31 μA at 0 C and it increases to 51 μA at 100 C. An interesting characteristic of this data is that the increase in temperature does not stay linear. It is linear from 0 C to close to 60 C and then the curve begins to level off for higher temperatures. Above 90 C, the output current begins to approach a constant value.

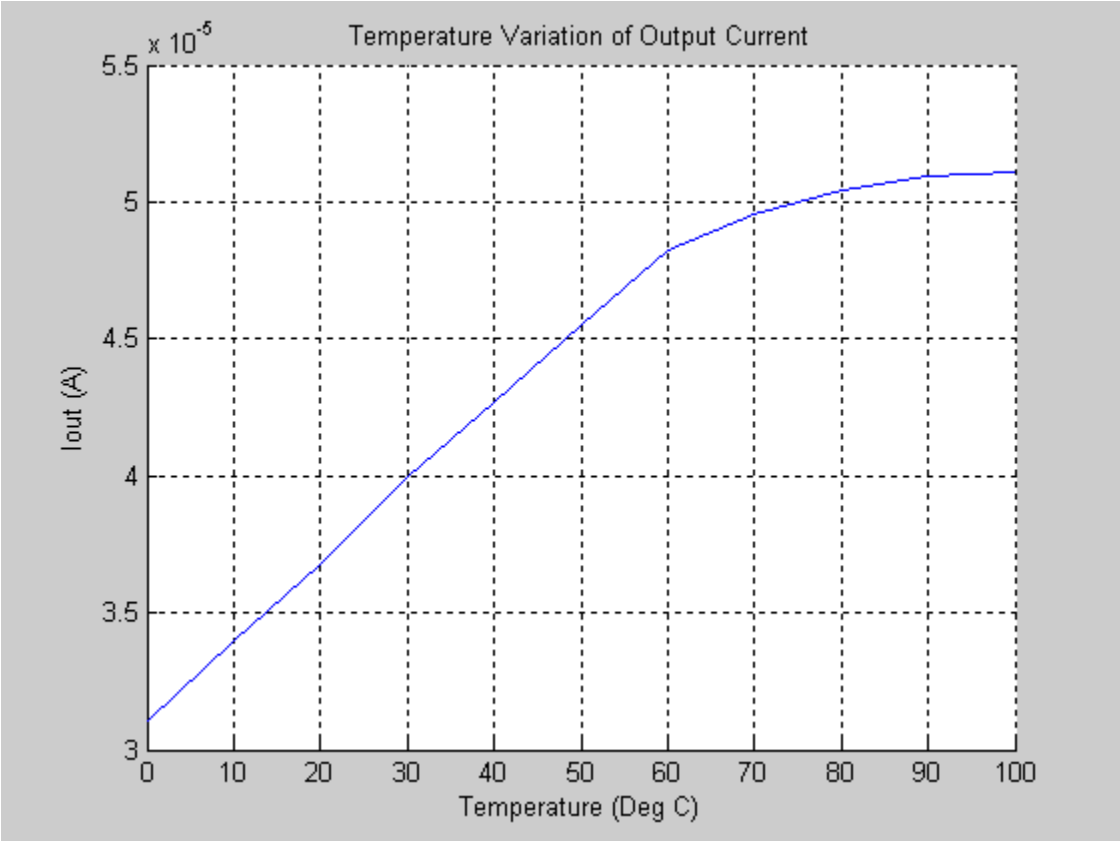

Figure 19: Output Current of β Multiplier versus Temperature

Chapter 6

Conclusion

6.1 Conclusion

This thesis focused on the design of a wide-swing cascode β multiplier current reference. Some basic building blocks and design techniques were introduced in order to provide the tools necessary to design the circuit. Then the actual design process of the current reference was covered. The finished design layout and schematic were presented. Simulation of the current reference and measurement results of the fabricated circuit were shown and compared. The design sufficiently meets the requirements needed for an efficient current reference other than the error due to resistor tolerance, which will be addressed in the next section.

6.2 **Future Work**

The low-voltage cascode bias circuit covered in [29] may be used to build a smaller version of the current source designed for this thesis. Also, the high error in the output current of this design could be corrected using a programmable resistor such as the one shown in Figure 20. A digital decoder could be used to close one switch at a time, providing an adjustable resistor. The resistance can be changed to correct error due to both fabricated resistor tolerance and temperature variations.

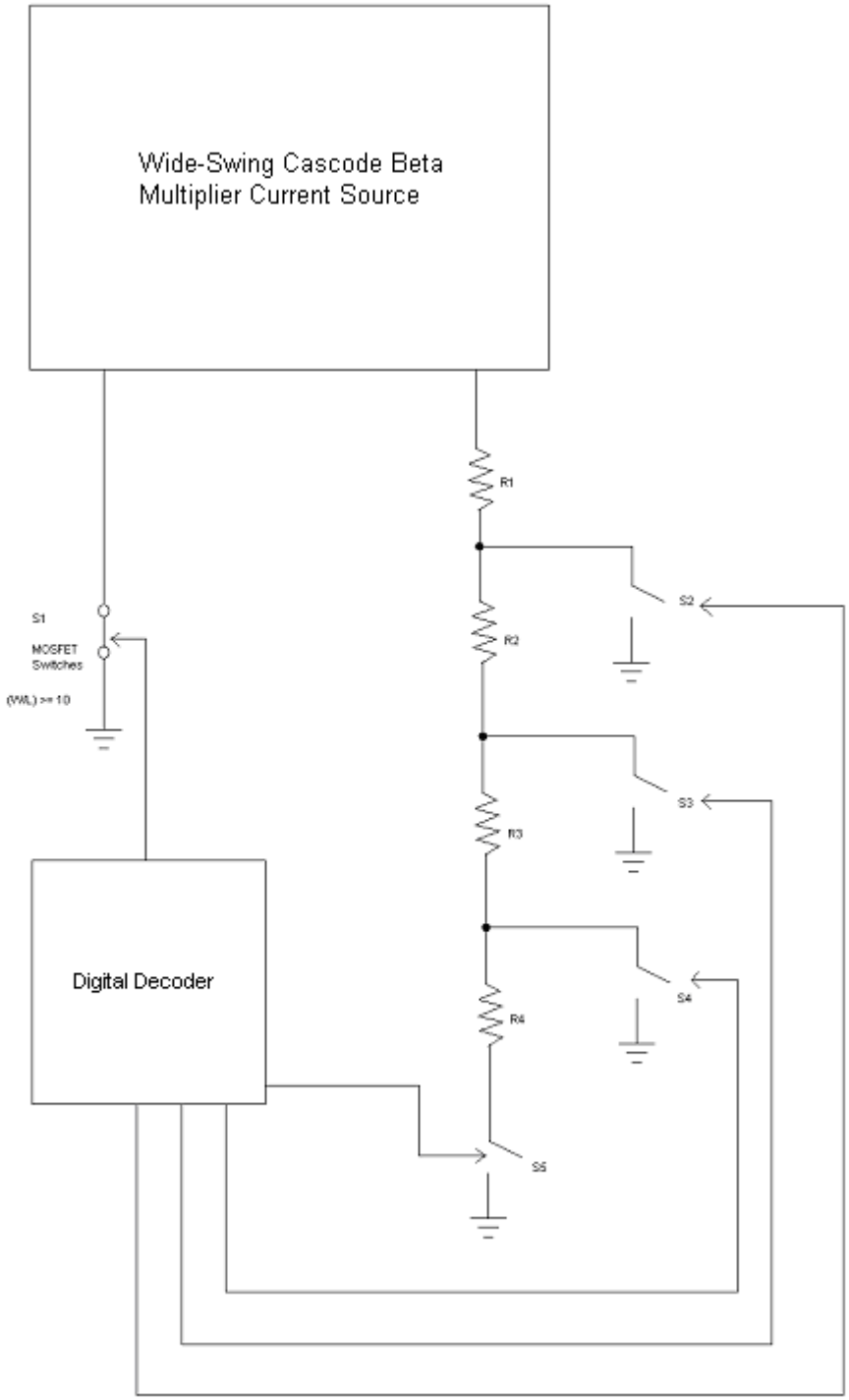

Figure 20: Programmable Resistor for β Multiplier

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Vita

Brad Miser was born in Knoxville, Tennessee on June 22, 1977. He lived in Miser Station, Tennessee the first two years of his life. When he was two years old he moved with his family to Maryville, Tennessee. He graduated from Maryville High School in 1995 and that fall he entered the University of Tennessee. His undergraduate studies focused on digital signal processing and microsystem design. His undergraduate degree was completed in May 2001 and he received the Bachelor of Science in Electrical Engineering.

Brad then moved to Jackson, Mississippi to join the distance learning graduate program called Commercial Postgraduate Electrical Engineering Training (ComPEET). Courses were taken over satellite from Mississippi State University. While in the ComPEET program, he began work towards a Master of Science degree in Electrical Engineering. His focus at this time was digital design. Due to budget problems, the ComPEET program was ended in the summer of 2002.

Brad then returned to the University of Tennessee in Knoxville to complete his Master's degree. He worked as a part-time research assistant at UT and continued taking classes at UT. He now focused on analog electronics. He also worked as a part time teaching assistant in the undergraduate electronics lab. Brad plans to finish his Master of Science degree in Electrical Engineering in August of 2003 and then find a position in integrated circuit design.