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**A Standard CMOS Compatible Bandgap Voltage
Reference with Post-Process Digitally Tunable
Temperature Coefficient.**

A Thesis Presented for the
Master of Science Degree
The University of Tennessee, Knoxville

Sam D. Caylor
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ABSTRACT

An essential element of most robust analog/mixed-signal systems is a stable and precise bandgap voltage reference (BGR). CMOS compatible BGR circuits are generally limited by variability in output drift over temperature due to process variations. In this work a CMOS BGR is developed that provides simple, digitally-controlled post-process (i.e., post fabrication) trimming. The trimming is achieved through MOSFET switches used to adjust a current gain factor for the thermal voltage referenced current within the BGR circuit. This current is proportional to absolute temperature (PTAT). The PTAT current is injected into a series connected resistor and diode to ultimately provide an output voltage. The output voltage's temperature coefficient is correlated to the current gain factor applied to the internally generated PTAT current. Thus, the BGR circuit's temperature coefficient (and therefore drift) is adjusted or tuned using a digital input word to control switch settings and therefore the PTAT current. By providing post-process trimming, chip-to-chip and wafer-to-wafer variations can be minimized through simple digitally controlled tuning. This trimming capability also extends the BGR to broad temperature range applications. A complete CMOS-compatible post-process trimmable BGR implementation is described and measurement results are provided. Design considerations to enhance the circuit's tolerance to radiation induced single-event transients are also addressed.

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Chapter 1 *Introduction*

1.1 Voltage Reference Applications

Voltage reference circuits are designed to produce a precise and stable output voltage over time, to be able to reject power supply fluctuation, and have a low voltage drift over temperature. For an analog or mixed-signal system the voltage reference is a critical element because of its direct impact to the accuracy and functionality performance of the overall system. This is particularly true for data converters, which use references as a standard for comparison. If the reference circuit is inaccurate or fluctuates then the data converters output will be incorrect because the input was compared to an imprecise standard.

1.2 Voltage Reference Specifications

There are numerous important specifications to effectively evaluate a voltage reference circuit. Elements include temperature drift, power supply rejection, thermal hysteresis and long-term stability. Also important parameters are start-up, power-consumption and noise.

Key specifications that are most significant are decided by the system that the reference will be supplying. For example, if the voltage reference is used in a temperature sensitive application, then temperature drift and thermal hysteresis might take precedence. However, if it were used in a high-precision data converter then, noise and power supply rejection for short-term stability would be more important.

No matter what the application these specifications are the critical parameters used to evaluate a voltage reference. These design requirements are explained in the following sections.

1.2.1 Temperature Drift

In order to provide an accurate system, it is important to have a stable voltage over temperature. Temperature coefficient (TC) is described as how much of the output of the voltage reference drifts with the variation of

temperature. The Temperature coefficient at room temperature (25°C) is given by:

$$TC_o = \frac{1}{V_o} \frac{dV_o}{dT} \times 10^6 \quad [ppm/^\circ C] \quad (1.1)$$

where

V_o = The voltage reference output.

This temperature coefficient can range from tens to hundreds of parts per million per degree Celsius (ppm/°C). This temperature variation of the voltage reference has a direct effect on the accuracy of the system the reference is in.

1.2.2 Power Supply Rejection

A voltage references ability to shield itself from variations of it supplies is called power supply rejection (PSR). PSR is used to calculate a voltage references ability to reject noise and unwanted signals, at a certain frequency, while tied to the supply rails. This is normally expressed in decibels (dB) as a function of frequency given by:

$$PSR(f) = 20 \cdot \log\left(\frac{V_{ref}}{V_{rail}(f)}\right) \quad (1.2)$$

where

V_{ref} = The voltage reference output, and

$V_{rail}(f)$ = The supply voltage at a given frequency.

A voltage reference's PSR over a large frequency range expresses how tolerant the reference is to power supply noise. The PSR can also be used to predict the voltage variation of the reference that is due to supply noise.

1.2.3 Thermal Hysteresis

Often time after a temperature cycle a voltage reference circuit will demonstrate trends where the output drifts from its original value. This occurrence is known as thermal hysteresis. Thermal hysteresis is regularly referred to by the following equation:

$$V_{ref_hysteresis} = \frac{V_{ref_o} - V_{ref_o_cycle}}{V_o} \times 10^6 \text{ [ppm/ } ^\circ\text{C]} \quad (1.3)$$

where

V_{ref_o} = The initial V_{ref} value at 25°C, and

$V_{ref_o_cycle}$ = The V_{ref} after a temperature cycle at 25°C

Here, 25°C, room temperature was chosen to be a basis temperature for the cycle.

1.2.4 Startup

In simple voltage reference circuits, the power supply independence is not sufficient enough for many analog or mixed-signal system applications. Greater independence can be achieved by causing the bias currents to depend not on the power supply voltage but on the reference circuit itself. This is referred to as self biasing [1]. In order for the circuit to start up into an operational state, help is needed. Start-up circuits are added to voltage references to ensure that the operational state reached is the desired operation point the circuit was designed for. These start-up circuits should help the voltage reference bias to a known state and then turn off in order to not waste energy and lower power consumption.

1.2.5 Power Consumption

In many cases an analog or mixed-signal application will need to be low-power or even battery powered. Therefore, reference designers must design with the least amount of power as possible. Thus, power consumption is a major issue with mobile, communication and handheld devices.

1.2.6 Additional Specifications

When designing a reference circuit there are many other parameters that the designer may consider in order to produce a robust system. An important constraint to references is initial accuracy. This is very hard to achieve without post process trimming, because of process variations. Long-term and short-term stability are also notable characteristics of a strong design. Output noise from a

reference circuit can minimize the accuracy of the systems output in data converter applications. No matter what the reference application, the specifications listed in the above sections are the critical parameters for evaluating a voltage reference.

Chapter 2 Voltage Reference Circuit Review

2.1 Voltage Reference Circuit Topologies

An ideal voltage reference generates a fixed voltage output that is independent of supply voltage, temperature and process, and is a vital part of data acquisition systems and conversion circuits. This chapter will discuss different reference topologies starting with a very simple design. Then, CMOS circuit references such as, proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) references are reviewed. Finally, bandgap voltage references topologies from simple to more advanced will be analyzed.

2.1.1 Zener Voltage Reference

To produce a very fast and easy voltage reference a zener diode can be chosen with a breakdown voltage as the reference point. The zener is connected such that the diode is in breakdown mode, thus supplying the needed reference. While simple and quick, it is unpopular in today's culture because the breakdown voltage of the zener diode is almost always larger than the power supply rails offered in modern circuit processes [5]. With this in mind, voltage references that are realizable in CMOS processes will be explored.

2.1.2 Supply Independent Voltage Reference

As mentioned above a reference circuit's purpose is to create a dc voltage or a current that is solely independent of process variations and supply voltage as well as an understood behavior over temperature. In order to be free of supply voltage variations a circuit must not rely on the voltage rails to supply its bias currents. So, self-biasing techniques are needed, in Figure 2.1 a supply independent circuit is shown. Notice that M_4 copies the current of M_3 thus

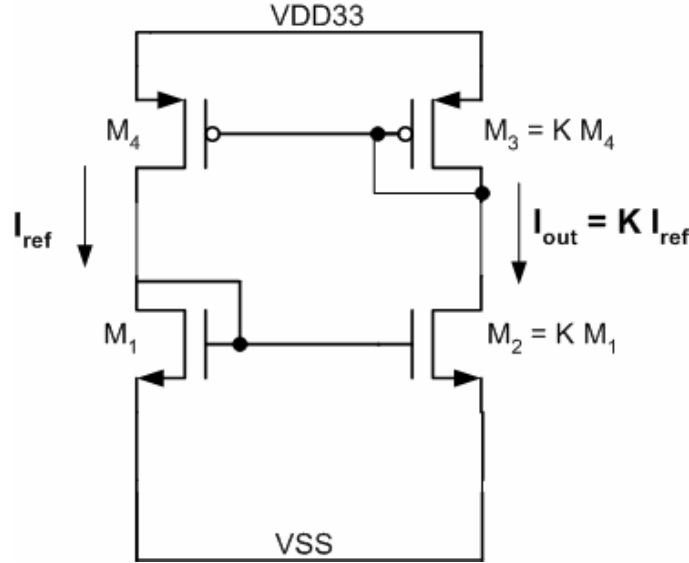


Figure 2.1 Supply Independent Current Reference (startup not shown) defining I_{ref} . With M_3 being a ratio of M_4 and channel-length modulations neglected then:

$$I_{out} = K I_{ref} \quad (2.1)$$

Since each diode-connected mosfet, M_1 and M_3 , feeds from a current source or sink, then I_{out} and I_{ref} are virtually independent of the supply voltage [4].

While in long-channel processes the design in Figure 2.1 is good, in short-channel processes it shows sensitivity to changes in VDD due to its low output resistance. An alternative is to cascode the PMOS devices [1]. A cascode is defined by a high output impedance stage sourcing into a low input impedance stage [7]. By doing this, the currents are made more equal and the reference is less susceptible to VDD variations. The problem with only cascoding the PMOS current mirrors is that while these currents are now made equal, but not constant, the deviation with VDD is still present at the voltage drop across the NMOS devices. To reduce this sensitivity and make a reference more supply independent, consideration to cascoding the NMOS devices as well, should be taken. Figure 2.2 shows a fully cascoded self-biasing thermal voltage reference. Here the PMOS cascode stack is used to force the same currents through each side, while the NMOS cascode stack is used to maintain constant voltage across

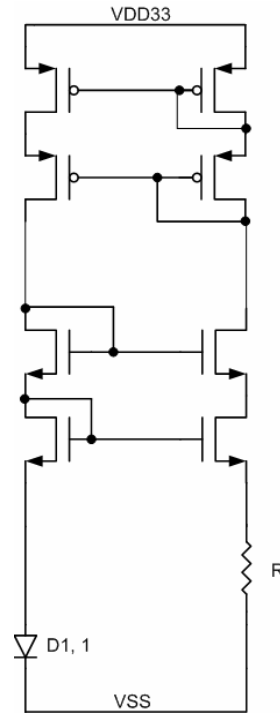


Figure 2.2 Fully Cascoded Self-biasing Thermal Voltage Reference (startup not shown)

the lowest NMOS devices. An important consideration in using the cascode design is whether there exists sufficient supply headroom. Designers must check if the amount of supply voltage is enough to keep all the devices in saturation. This depends on the process and the thermal voltages of the devices. In most short-channel processes this technique cannot be used due to the thermal voltages of the devices being high in relation to the supply voltage. For short channel processes an amplifier design topology is needed to set the currents and hold the voltage across the lower devices. It should be stated that an NMOS only cascode configuration will not help in making the reference more tolerant to changes in VDD. Because the PMOS devices are not cascoded the currents through each branch are not equal, and thus having vulnerability to VDD fluctuations [1].

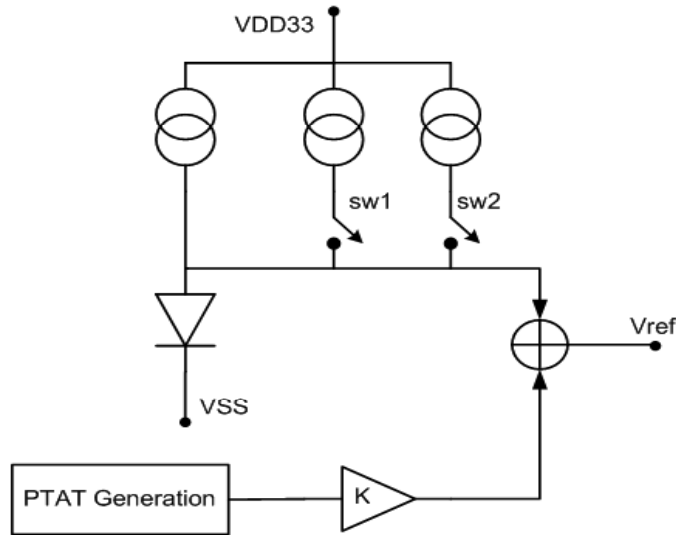


Figure 2.3 A Simplified Temperature Independent Voltage Reference summing CTAT and PTAT references.

2.1.3 Temperature Independent Voltage Reference

Voltage or current references that display little dependence on temperature prove to be very valuable in analog mixed-signal circuit design. Since many process parameters are temperature dependent, then having a temperature independent reference implies that it would also be process independent. Trying to make a design or process that is completely without temperature dependence would prove to be very challenging and most likely futile. However, by summing two opposing temperature coefficients weighted properly a reference that is highly independent of temperature can be achieved. A simplified version is shown in Figure 2.3. In creating such a reference the bipolar transistors characteristics prove to be a well defined and reproducible for producing a negative and a positive temperature coefficient [4].

2.1.3.1 Complementary To Absolute Temperature

The base-emitter junction of the bipolar transistor or in more general terms, the forward voltage of the pn-junction of a diode displays a negative temperature coefficient. From Figure 2.2, it can be seen that the cascode structures force the same amount of current into each branch. So the current

that runs through the resistor must be the same as the current the runs through the diode. The current in each branch can be shown by:

$$I_{ref} = \frac{V_D}{R} = I_s \cdot e^{\frac{V_D}{n \cdot V_T}} \quad (2.2)$$

where

$V_T = kT/q$, The thermal voltage,

V_D = The diode voltage, and

I_s = The reverse saturation current of the diode.

Solving for the resistance yields:

$$R = \frac{n \cdot V_T}{I_{ref}} \cdot \ln \frac{I_{ref}}{I_s} \quad (2.3)$$

This resistance helps set the current level or I_{ref} . In order to determine the current variation of the reference the overall current change of the circuit with respect to temperature must be written as:

$$\frac{\partial I_{ref}}{\partial T} = \frac{\partial}{\partial T} \left(\frac{V_D}{R} \right) = \frac{1}{R} \cdot \frac{\partial V_D}{\partial T} - \frac{V_D}{R^2} \frac{\partial R}{\partial T} \quad (2.4)$$

And finally arranged as:

$$\frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T} = \frac{1}{V_D} \frac{\partial V_D}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \quad (2.5)$$

From Equation (2.5) we can see that the diode-referenced, self-biasing circuit shows an inverse proportionality to temperature. So if the voltage across the diode is used as a reference, with the fact that the current flowing through the diode will decrease with increasing temperature causing a voltage drop across the diode and the fact that the bandgap of silicon will decrease with increasing temperature causing the diode voltage, V_D , to drop with increasing temperature, this circuits design by nature is to be complementary to absolute temperature (CTAT) [1].

2.1.3.2 Proportional To Absolute Temperature

As described before, in order to make a temperature independent reference, there must be a positive temperature coefficient to add to the negative

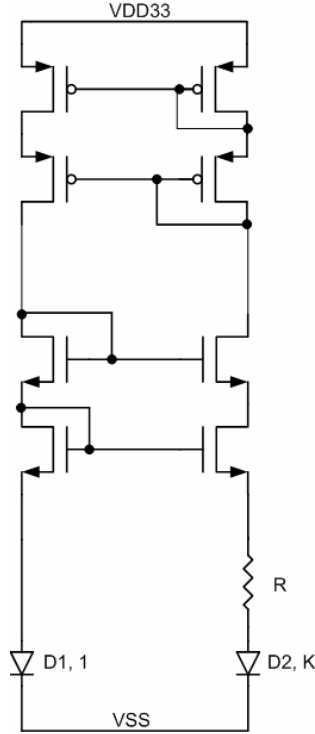


Figure 2.4 Thermal Voltage Self-biasing Reference Circuit (startup not shown)

one with proper weighting to produce a zero temperature coefficient circuit. A circuit that accomplishes a PTAT output is the thermal voltage reference self-biasing circuit. By operating two bipolar transistors or two pn-junctions with unequal current densities, then the difference between the base-emitter or the p and n voltages is directly proportional to absolute temperature. Figure 2.4 shows a thermal voltage-reference, here D_1 is only one diode and D_2 is K diodes in parallel. By making D_2 larger than D_1 , a smaller voltage will be dropped across D_2 for the same current through both diodes. This is important, because with the resistor in the circuit there must be a smaller voltage drop across D_2 in order to have nonzero current flowing in the circuit. With this design the voltage across D_1 equals the voltage drop across the resistor and D_2 as shown by:

$$V_{D1} = V_{D2} + I_{D2}R \quad (2.6)$$

As previously mentioned the difference in the diode voltages is dropped across the resistor. Knowing that $I_{D1} = I_{D2} = I_{ref}$, V_{D1} can be found from Equation 2.2:

$$V_{D1} = nV_T \cdot \ln \frac{I_{ref}}{I_S} \quad (2.7)$$

which yields V_{D2} :

$$V_{D2} = nV_T \cdot \ln \frac{I_{ref}}{K \cdot I_S} \quad (2.8)$$

where

I_S = the reverse saturation diode current,

n = the current gain factor, and

K = the ratio of junction area of the two diodes.

Because of equal current in each branch:

$$R = \frac{nV_T \cdot \ln K}{I_{ref}} \quad (2.9)$$

rearranging to solve for I_{ref} :

$$I_{ref} = n \frac{kT}{q} \cdot \frac{\ln K}{R} \quad (2.10)$$

Notice in Equation (2.10) that current is now proportional to absolute

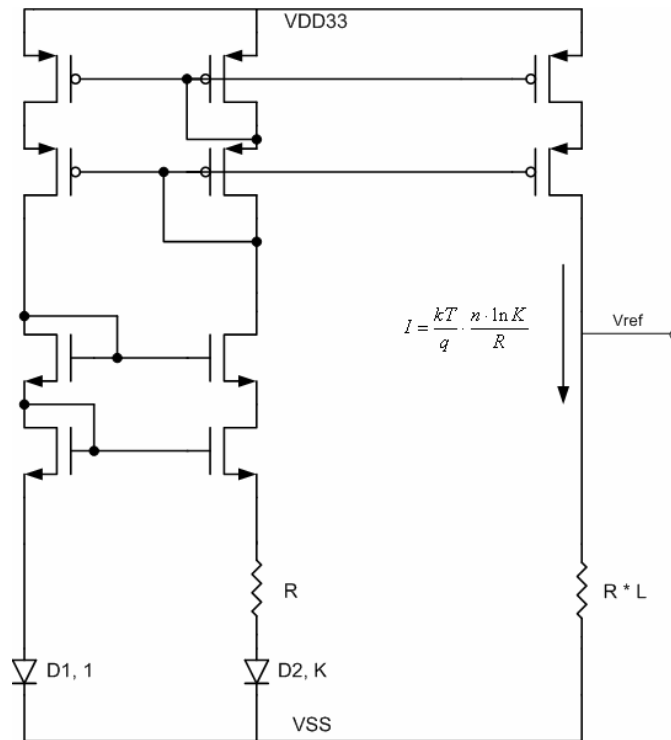


**Figure 2.5 PTAT Voltage Reference Based off of the Thermal Voltage Reference
(startup not shown)**

temperature (PTAT). Shown in Figure 2.5 is a voltage reference using the same thermal voltage-reference circuit as before with another branch mirrored out with a resistor ratio of L . With the help of Equations (2.9) and (2.10) the reference voltage, V_{ref} , of Figure 2.5 can be found as:

$$V_{ref} = I_{ref} \cdot L \cdot R = \frac{kT}{q} \cdot nL \cdot \ln K \quad (2.11)$$

Notice how now the temperature performance of the resistor is no longer in the equation only the temperature performance of the thermal voltage [1].

2.1.4 Bandgap Voltage Reference

Now that both the positive and negative temperature coefficients have been shown above, with the right balancing a reference with a nominally zero output temperature coefficient can be obtained. Figure 2.6 shows a bandgap voltage reference [4]. This reference has the PTAT current that was generated in Figure 2.4 that is driving a resistive load and a diode as in the CTAT circuit in Figure 2.2. This PTAT thermal voltage is approximately $85 \mu V/^{\circ}C$ while, the

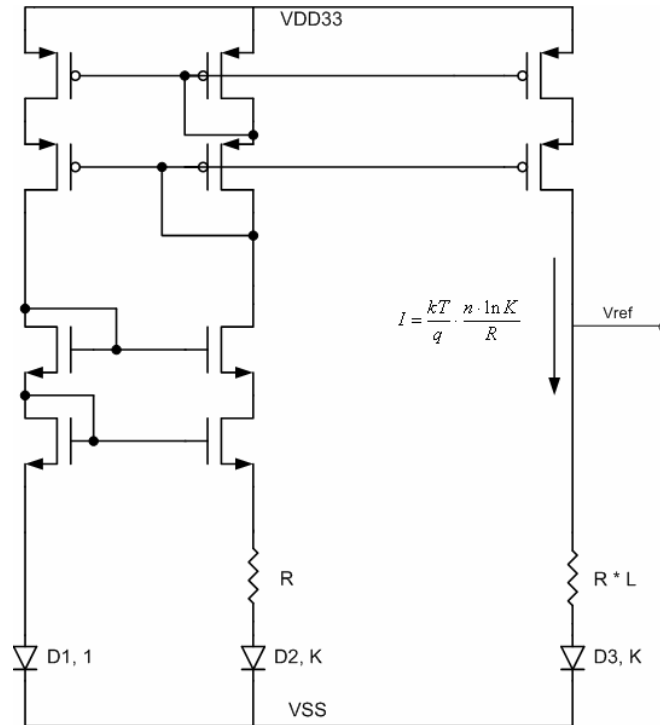


Figure 2.6 Bandgap Reference Voltage (startup not shown)

CTAT of the forward-bias diode voltage is around 2 mV/°C. In order to achieve a very small temperature coefficient these two references must be added in a weighted fashion. The left two branches of Figure 2.6 is a thermal voltage based reference from Figure 2.4. The upper PMOS devices are matched to ensure that the currents flowing in all branches are equal while, the lower NMOS devices are matched to set the voltage drop from the upper rail across the transistors to be equal.

From Equation (2.10) we find the current flowing in each branch of the reference. This current is mirrored out to the output leg at the right of the circuit, flowing into the $L \bullet R$ resistor and into D_3 . Using Equation (2.11) the output reference voltage of the bandgap can be shown as:

$$V_{ref} = I \cdot L \cdot R + V_{D3} = V_T \cdot (nL \cdot \ln K) + V_{D3} \quad (2.12)$$

where

L = the resistor ratio of the two resistors.

The variation of V_{ref} with respect to temperature of the bandgap reference can be given by

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_T}{\partial T} \cdot nL \cdot \ln K + \frac{\partial V_{D3}}{\partial T} \quad (2.13)$$

By choosing the factor of L and of K , the temperature coefficient for the output voltage can be made zero for a portion of the temperature range and very small in the near vicinity [1].

Unfortunately, the output of the voltage reference only cancels to the first order and are not constant as shown by the device physics of the diode. The diode voltage can be written as:

$$V_D = V_T \cdot \ln \frac{I}{B n_i^2 T \mu_n} \quad (2.14)$$

where

V_T = the thermal voltage

n_i = the intrinsic carrier concentration

μ_n = the mobility of electrons, and

B = is the temperature-independent quality.

Both terms n_i and μ_n are temperature dependant and non-linear terms associated with the electron physics of the diode. This helps to explain why the reference has a zero temperature coefficient for only a portion of the temperature range and why the rest of the range is non-zero [3].

2.1.5 Startup

One important issue with supply independent circuits is that there exists a degenerate bias condition in which a self-biasing circuit can have zero current flowing through its branches. Because the upper PMOS devices ensure that there is equal current flowing in each branch, if this degeneration state is the state of the circuit when the reference is powered on, then it will remain in this degenerate state indefinitely [4]. So a need for a circuit that will inject current into the current mirror loop at startup to ensure there does not exist a zero current state, while also seeing that it will not interfere with the normal operation of the reference. It would be ideal if the startup design would begin by injecting current into the loop, but after the reference circuit has reached its balanced condition

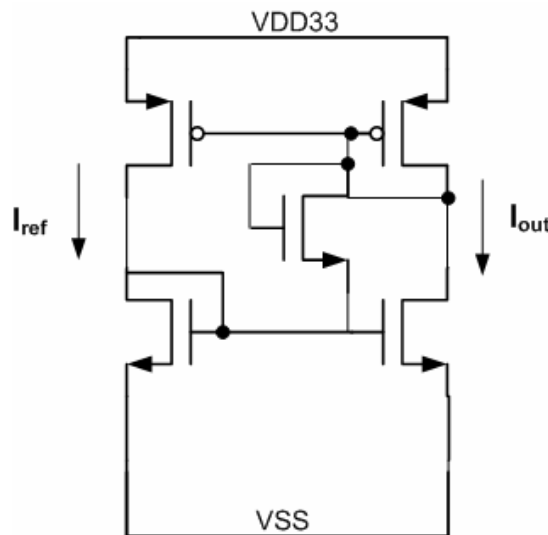


Figure 2.7 Simple Startup Solution for Beta-multiplier Circuit

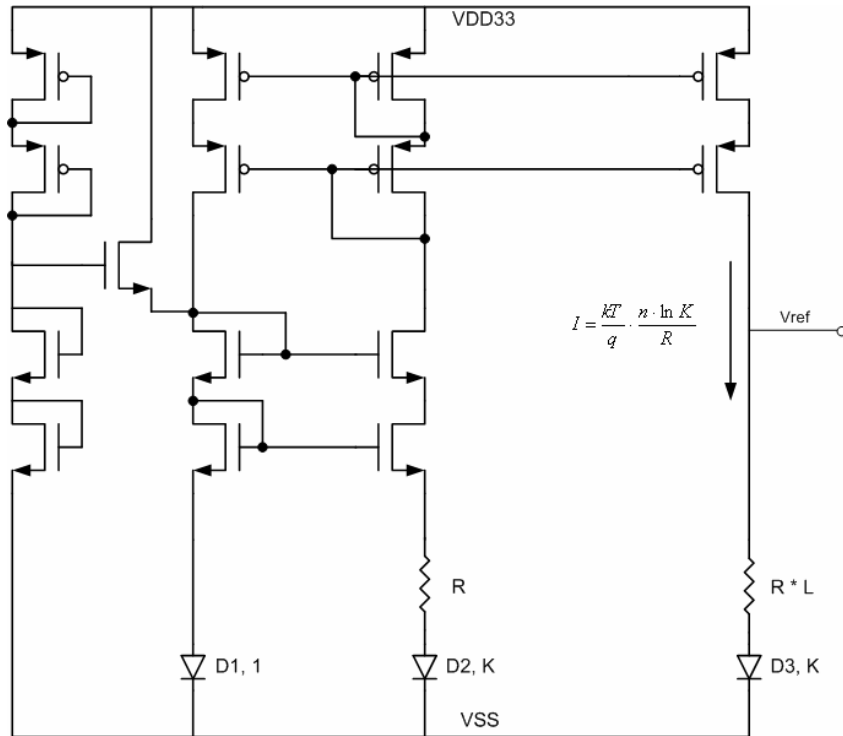


Figure 2.8 Bandgap Voltage Reference Circuit with Startup.

then the startup circuit would turn off or at the very least stop injecting current such not to disrupt the output of the reference [1]. Figure 2.7 and 2.8 show two easy and simple startup techniques. Both startup circuits will stop injecting current into the reference circuit once the normal operating state of the circuit has been reached.

Chapter 3

Design of the Tunable Bandgap Voltage Reference Circuit

3.1 Bandgap Voltage Reference Design

As discussed in the previous chapter a bandgap voltage reference is the weighted combination of a proportional to absolute temperature (PTAT) reference and a complementary to absolute temperature (CTAT) reference. These two references are normally designed using a thermal voltage reference and a diode-reference respectively. With these references, cascode devices are used to ensure that equal currents are in all branches and that the voltage across the lowest Nmos devices is kept constant. These two techniques are very important, because when the currents are equal and the voltage drops across the lowest Nmos devices are constant, the voltage at the output of the reference will remain nearly constant. By design, even through power supply fluctuations and temperature variation, the circuit by its very nature tries to keep the reference output constant.

3.1.1 Initial Bandgap Reference Analysis

In a silicon based Complementary Metal-Oxide Semiconductor (CMOS) process, the bandgap energy as a function of temperature is known by the following equation:

$$E_g = 1.16 - (702 \times 10^{-6}) \cdot \frac{T^2}{T + 1108} [eV] \quad (3.1)$$

Observe from Equation (3.1), the energy of the bandgap decreases with the increase of temperature. When a diode is biased with a steady current and the temperature goes up, then the barrier height of the n and p sides of the diode decreases thus, causing a voltage drop around the diode (V_D). This performance is used by the bandgap reference to create the CTAT reference. In order to produce a PTAT source, a thermal voltage reference ($V_T = kT/q$) design is needed. For this design, a wide-swing cascode current mirror was used in order

to self-bias the cascode devices while holding the sources of the lowest NMOS devices to the same voltage potential. This same wide-swing cascode current mirror was also used to self-bias the PMOS cascode devices to ensure there was equal current flow in each branch of the bandgap reference.

Figure 3.1 shows a simplified bandgap reference topology that was used. From this figure, it can be noticed the presence of the diode-reference (CTAT reference) and thermal voltage reference (PTAT reference) circuits discussed in chapter 2. With the summing of the PTAT and CTAT reference circuit, a stable output reference can be achieved. The key to success in a reference circuit is matching. Without the upper PMOS devices of the cascode current mirror being very closely matched the current in each branch of the circuit will not be equal. The same is true to the lowest NMOS devices of the cascode mirror, without being very closely matched the voltage drops across these transistors and therefore across the diodes of each branch cannot be equal. So matching,

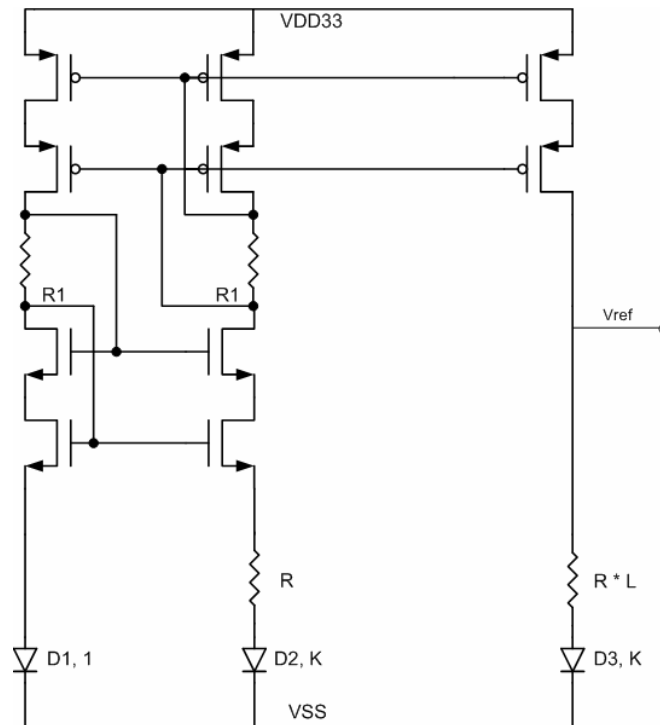


Figure 3.1 Basis Bandgap Reference Topology (startup not shown)

whether it is device matching, resistor matching or even diode ratio matching, proves to be an important aspect of reference design.

3.1.2 Device Matching

For the matching of transistor devices a layout technique called common-centroid was used. Common-centroid layout is the act of evenly spacing devices, that are interdigitated, that have the same central point. Through this technique sheet resistant variation as a function of the devices position is minimized thus making the devices more closely matched. In this design, all the bodys and sources of the upper most PMOS transistors are tied to the same potential, V_{DD} . Therefore, all the devices can be placed in the same well. Figure 3.2 shows the common-centroid layout of the upper most PMOS. By using this common-centroid technique the currents in each branch of the reference are very closely matched. With this design the body and sources of the lowest NMOS devices are not connected to the same potential, therefore these devices cannot be placed in the same well. However, these devices were place as close together as design rules would allow minimizing sheet resistant gradients. Guard rings were also used generously around all devices to minimize cross coupling noise to help supply rejection.

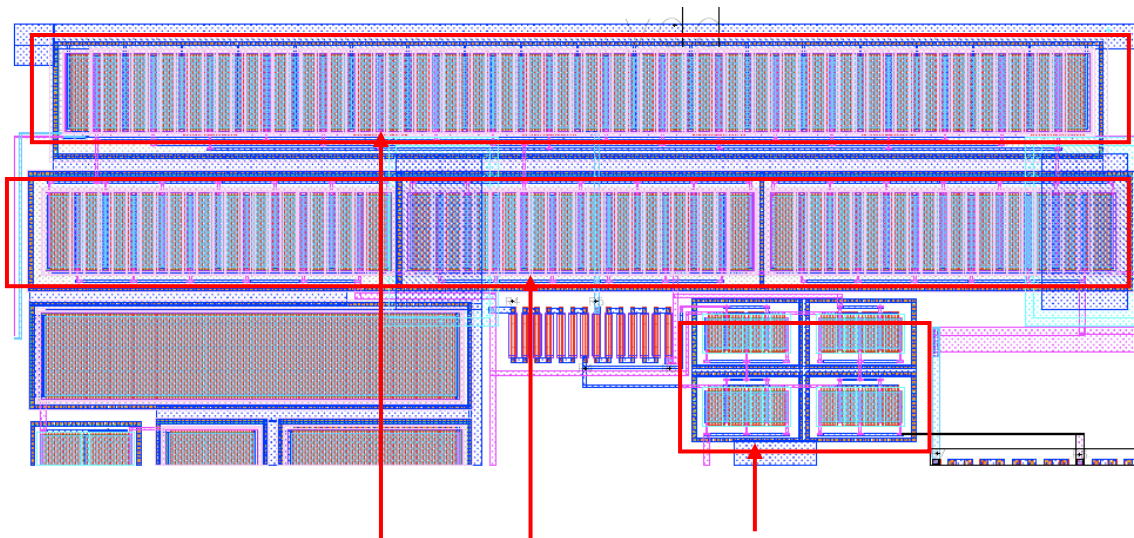


Figure 3.2 Layout of Upper and Lower PMOS and NMOS Cascode Devices.

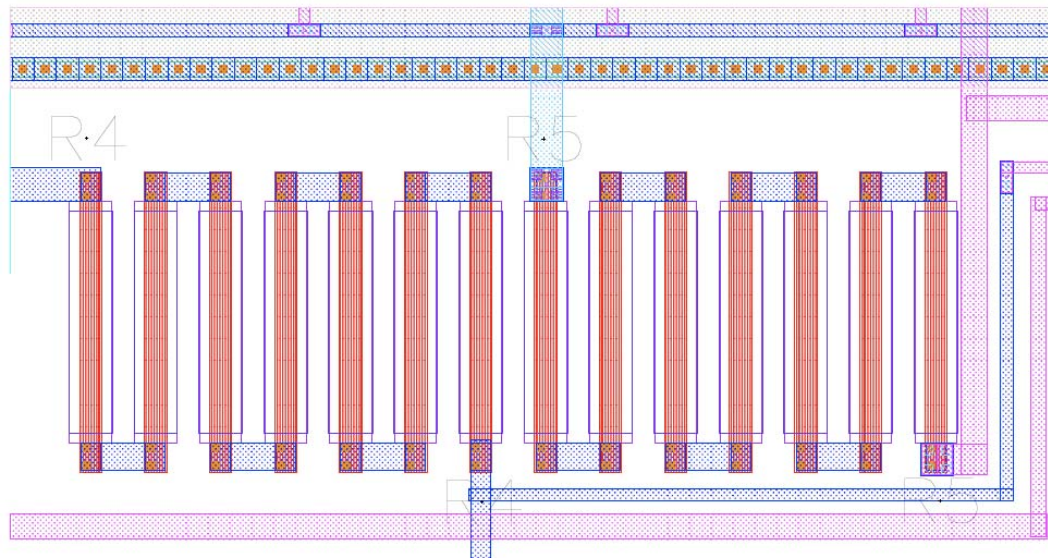


Figure 3.3 Layout of the Matched R1 Resistors

3.1.3 Resistor Matching

The same can be said for the matching of resistors. In this design two separate sets of resistors were matched as seen in Figure 3.1 ($R1$ and $R1$, R and $R \bullet L$). Common-centroid was used in both cases to help matching. A unit resistor size is chosen, that is a unit portion of both resistors. Both $R1$ resistors must be as closely matched as possible, so the voltage drops in both branches will be the same (that is if there are matched transistors). The common-centroid $R1$ resistor layout can be seen in Figure 3.3. The common-centroid technique was also used to match the ratio pair of resistors R and $R \bullet L$. Because R is the smaller of the two resistors it was placed closer to the center of the resistor block as can be seen in Figure 3.4.

3.1.4 Diode Ratio Matching

Diode matching in this design is a little different from the previous matching designs. Here the ratio of the area is the important parameter. So a unit diode was used as the basis to make the diode ratios. In general a ratio of 8 to 1 is used for K (the diode ratio), because of the ease of layout with the one in the center by the other eight making the layout a three by three element. For this

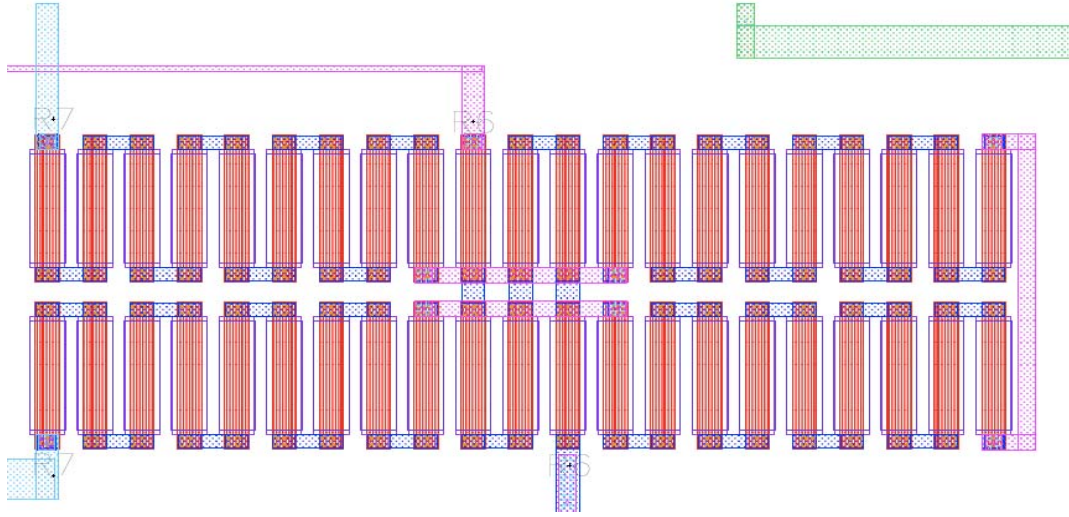


Figure 3.4 Layout of the Ratio Matched R and $R \bullet L$ Resistors

design a K of 24 was used. Twenty-four was used for its symmetry in layout, making the layout more square, and helping the gradients to be more uniform. Also, the diode ratio was chosen to minimize the size of the R and $R \bullet L$ resistors. Notice in Equation (2.12) if K is increased then L can decrease to reach the same value. As mentioned before, the resistors matching to each other is more important than that of the diodes. This also helps to reduce the output impedance of the overall circuit.

3.1.5 Bandgap Reference Temperature Performance

Through matching a very stable reference over temperature can be achieved. As seen in Figure 3.1, the PTAT current is sourced directly into the resistor and diode. This PTAT current can be easily calculated by using Equation (2.10). Therefore the reference current can be written as:

$$I_{PTAT} = \frac{n \cdot V_T \cdot \ln(K)}{R} \quad (3.2)$$

From this PTAT current, the reference voltage can be obtained with the help of Equation (2.12):

$$V_{ref} = I_{PTAT} \cdot L \cdot R + V_{D3} \quad (3.3)$$

Using Equations (3.1) and (3.2) the reference voltage can be rewritten as:

$$V_{ref} = n \cdot V_T \cdot L \cdot \ln(K) + V_{D3} \quad (3.4)$$

From this, and with the help of Equation (2.13), the voltage reference temperature performance can be shown as:

$$\frac{\partial V_{ref}}{\partial T} = n \cdot \frac{\overbrace{\partial V_T}^{0.085 \text{ mV}/^\circ\text{C}}}{\partial T} \cdot L \cdot \ln(K) + \frac{\overbrace{\partial V_{D3}}^{-1.6 \text{ mV}/^\circ\text{C}}}{\partial T} \quad (3.5)$$

As shown in Equation (3.5) the variation over temperature for V_T and the diode voltage in the process was 0.085 mV/°C and -1.6 mV/°C respectively.

Setting Equation (3.5) equal to zero and solving for L yields:

$$L = \frac{1.6}{n \cdot \ln(K) \cdot 0.085} \quad (3.6)$$

The resistor ratio factor L gives a designer the ability of where the zero temperature coefficient (TC) will occur. Here an L of 6 was chosen for simplicity of resistor ratio matching, with the diode ratio K of 24 as mentioned before. Many designers use room temperature as the zero TC temperature, however most integrated circuits have a normal operating temperature of 40 to 50 degrees Celsius. For this design the zero TC was set to be 45 degrees Celsius, because this was closer to the final products operating temperature. Also n , the current gain factor, can be used here to adjust the value of L to set the zero TC point [1]. For this design special use is made of the current gain factor n . Through some topology additions, this factor is made accessible off chip to give this bandgap voltage reference an additional feature, tunability.

3.2 Tunability

Why would anyone want a bandgap voltage reference to be tunable? Reference circuits are suppose to be stable, constant and unchanging, why the need to alter the output? Though references can be manufactured with very little fluctuation with temperature and supply variations, processes variation still cause chip-to-chip differentiations. As processes push to keep getting smaller and smaller feature sizes, manufacturing tolerance specifications continue to get harder and harder to meet. A tunable reference could minimize these chip-to-

Table 3.1 Tunalbe Bandgap Voltage Reference Device Sizes

Device Name	Width(μ)	Length(μ)	Multiple
M1	4	2	2
M2	4	2	2
M3	4	2	2
M4	4	2	2
M5	9	3	12
M6	9	3	12
M7	9	3	12
M8	9	3	12
M9	9	3	12
M10A	9	3	1
M10B	9	3	1
M11	9	3	12
M12A	9	3	1
M12B	9	3	1
M100	10	20	1
M101	10	20	1
M102	10	5	1
M103	10	10	1
M104	10	5	1
M105	10	50	1

Devices $M_{11A} - M_{12B}$ mirror the PTAT current to switches that are design inputs. Off chip these switches can be brought “high” or “low” to change current in the output leg. These devices multiplicity factor is only one compared to twelve of the PTAT current branches. So, the current being injected into the output stage from the tuning branches is only one twelfth of the PTAT current. During design, the zero temperature coefficient was centered to it optimal point with one switch “high” and the other switch “low”. By doing this, the current gain factor can add or subtract one twelfth of the PTAT current for tuning. Through this design the current gain factor can be changed from $n = 12/12$ with both switches “high” or open, to $n = 14/12$ with both switches “low” or closed (notice these are PMOS switches).

Simulations were run using the Hspice simulator. As mentioned before, in order to add and subtract currents using the current gain factor the zero temperature coefficient was found with one switch “high” and the other switch

“low”. Since the currents gain factor currents are merely being added, which switch is “high” and which is “low” does not matter given matched devices. Either way, the current gain factor is equal to 13/12 and the output current is nominally the same. Figure 3.6 shows the simulation results of the output of the BGR with a current gain factor of 13/12. If the current gain factor was changed to 14/12 and both switches turned on or “low”, then more PTAT current is driven into the output branch. This causes the output over temperature to be more PTAT or proportional to absolute temperature. This is shown in Figure 3.7. Likewise, if the current gain factor was changed to 12/12 with both switches on or digital ‘high” then the BGR output would be more CTAT or complementary to absolute temperature. This is shown in Figure 3.8. By use of the current gain factor the amount of PTAT current, generated by the self-biasing wide swing cascode current mirror from the interior of the BGR, driven into the output stage can be changed. Switching from one current gain factor to another changes the output voltage of the reference, which also directly impacts the temperature coefficient.

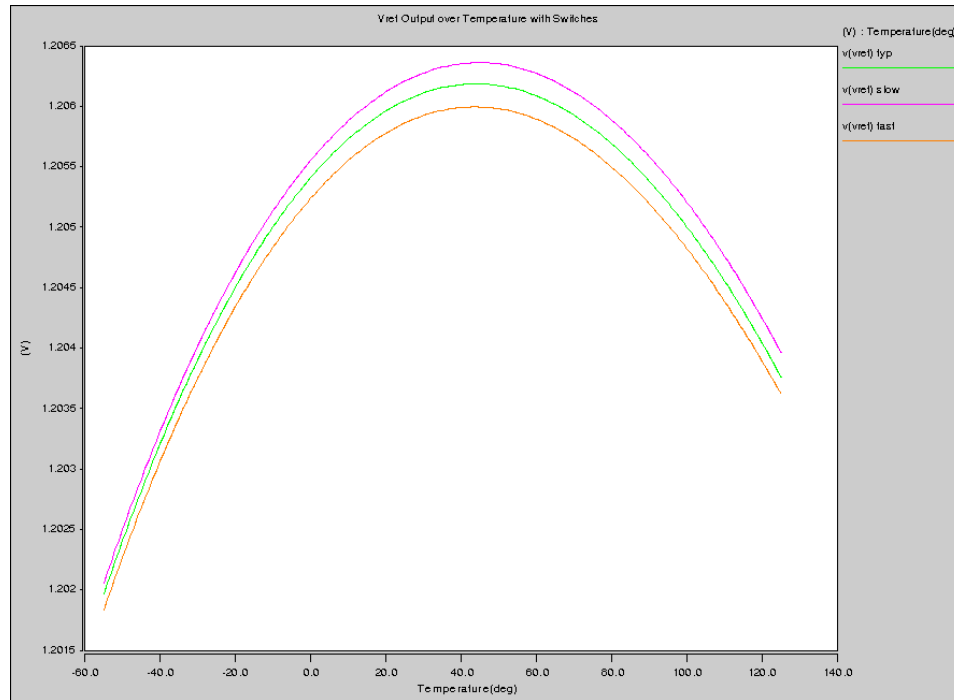


Figure 3.6 Tunable BGR Voltage Output Simulation Results over Temperature with Corners Centered; Sw1 = 3.3 V, Sw2 = 0 V

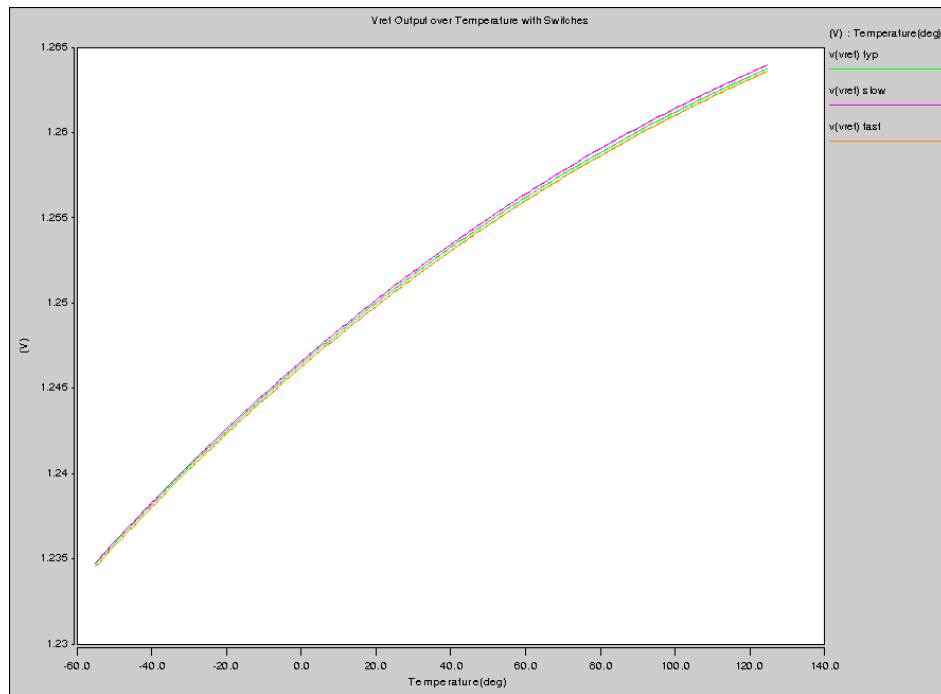


Figure 3.7 More PTAT Simulation Results; Sw1 = 0 V, Sw2 = 0 V

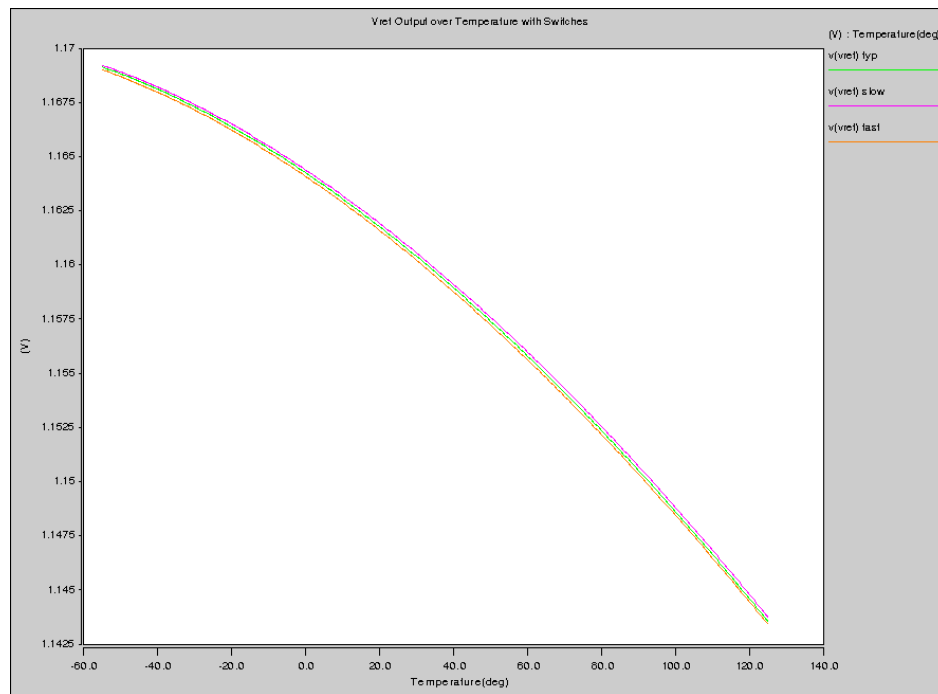


Figure 3.8 More CTAT Simulation Results; Sw1 = 3.3 V, Sw2 = 3.3 V

Through the altering of switch setting chip-to-chip and wafer-to-wafer variations can be minimized. If one chips output is higher and another chips output is lower than the simulated output, then the first chips output can be brought down and the later chips output can be brought up through post process digital tuning of the current gain factor switches. This minimizes output differences due to process variations.

3.3 Power Supply Rejection

A voltage reference's Power Supply Rejection (PSR) over a large frequency range expresses how tolerant the reference is to power supply noise. The PSR can also be used to predict the voltage variation of the reference that is due to supply noise. PSR is used to calculate a voltage references ability to reject noise and unwanted signals, at a certain frequency, while tied to the supply rails. Equation (1.2) was used to calculate the PSR for the voltage reference in simulation and the results of that simulation over frequencies up to 100 MHz and

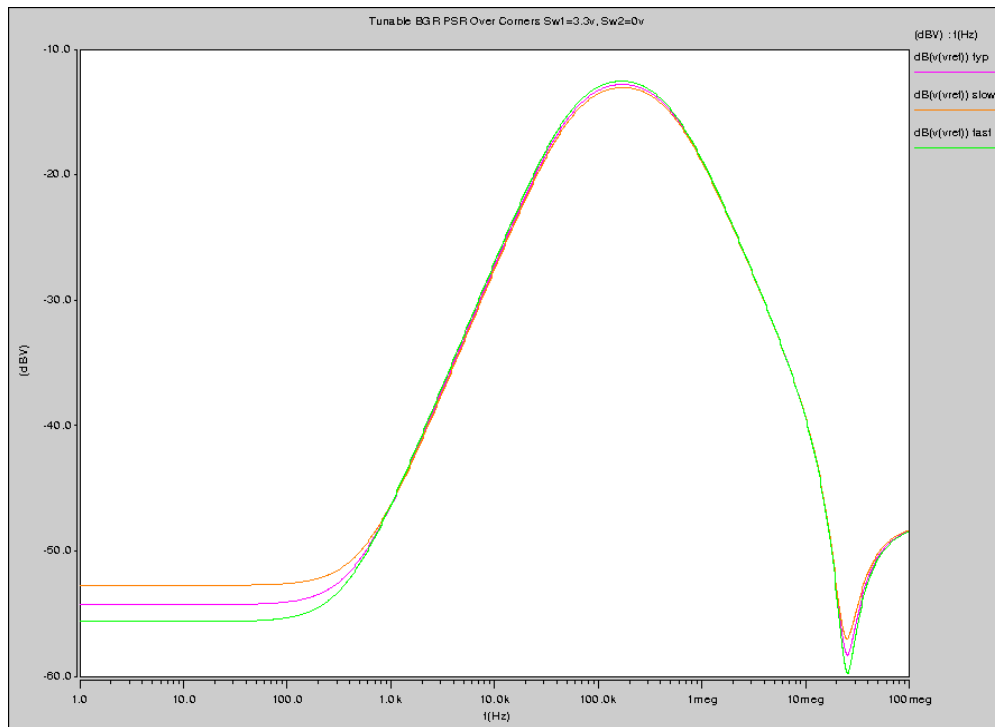


Figure 3.9 Simulation of Power Supply Rejection over corners.

over corners in shown in Figure 3.9. The PSR of a voltage reference is normally derived at low frequencies because the BGR is a DC based circuit that does not have any signal propagation from an input to an output. Therefore, the PSR of this tunable BGR is around 55 dB.

3.4 Startup

Self-Biasing circuits are great for isolating a circuit for power supply fluctuations, however they present a challenge in the zero current state. By using self-biasing current mirrors creates a design that tries to force the same amount of current into each branch. With this type of design there exists a case in which the circuit is powered on with equal zero current in each branch. When this occurs the current branches are supplying equal zero current in each branch, therefore are happy in this meta-stable state. However, the circuit is powered on but not at its operating point, so the output voltage is not as expected. In order to ensure a successful startup, current must be injected into a current mirror leg to eliminate the zero current state. Once the circuit has reached its normal operating condition the startup should stop injecting current.

For this design a special sensing startup design is used. This startup design is shown in Figure 3.5. The gate of M_{104} senses the voltage at the output. In a power on situation this voltage will be low, less than a turn on voltage. This pulls the gate of M_{102} up, because of M_{105} being diode connected, turning it on. In turn, this pulls the gate of M_{100} down, turning it on, injects the left most leg of the PTAT current mirror with current. This eliminates the zero current case. But when the output reaches its normal operating condition the gate of M_{104} senses the output of the reference, turning on, and pulls the gate of M_{102} down to off. This in turn pulls the gate of M_{100} up, turning it off and stopping the injection of current. By the same token if the output of the reference were to drop below its nominal output the startup circuit would begin to inject current again to help restore the BGR to normal operation, after which startup would stop injection.

A startup simulation was run to ensure that the circuit would begin operation when power was applied. Figure 3.10 shows the results of that startup simulation. The startup simulation was performed by increasing the amount of Vdd applied to the circuit over time and monitoring the output reference voltage of the circuit. Once the reference has had sufficient time to startup a quick dropout spike was introduced to simulate a quick dropout of supply voltage that might occur. Then after the circuit has had sufficient time to recover Vdd is removed for a longer amount of time and then returned but to a value lower than full power. Startup and the ability to restart are key and important features when designing a self-biasing reference.

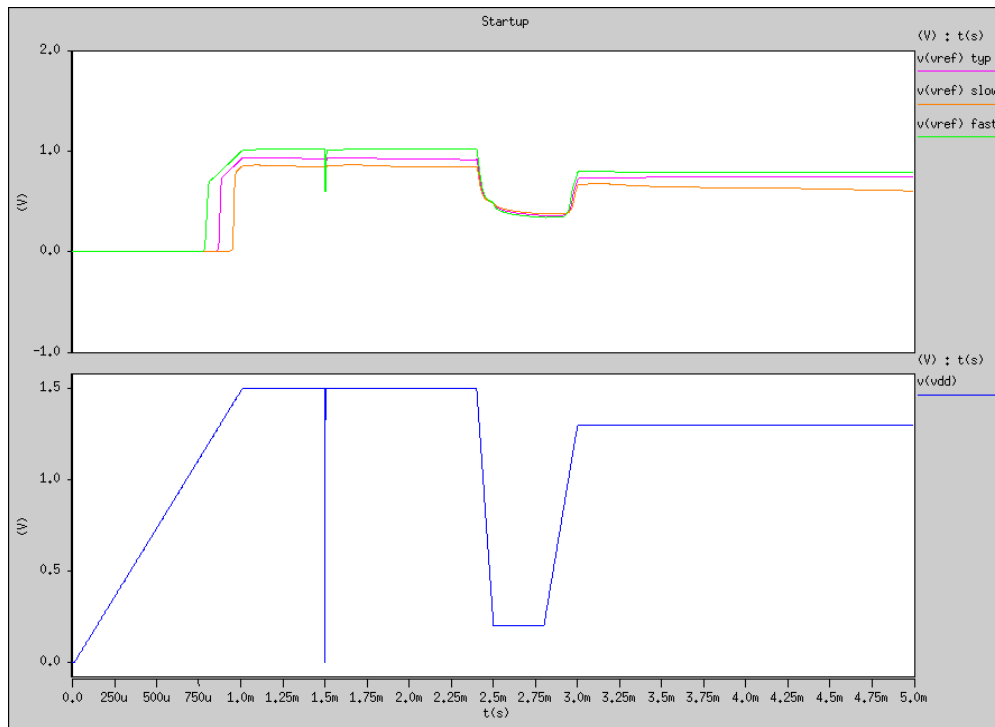


Figure 3.7 Startup Simulation Results of the Tunable BGR over Corners.

Chapter 4 Results and Discussion

This chapter presents the measured results of the tunable bandgap voltage reference. Tunable testing is an important parameter to characterize the minimized chip-to-chip and wafer-to-wafer variations. In this chapter the circuit's tunability is measured and discussed. Temperature testing results are also shown with output voltage and temperature coefficient being discussed. Another important parameter for any reference is the power supply rejection. This tunable BGR's PSR results are also shown. Finally a comparison of an alternate BGR designed for low process variation will be made along with comparison results.

4.1 Tunable Testing

As discussed previously, the circuit has the ability to change the systems current gain factor, this allows the output of the voltage reference to be changed. The two tunable gain factor switches Sw1 and Sw2 from Figure 3.5 are routed off chip through pads to output pin of the packaged parts. From these package pins the switches are run to pin headers on the test board. These headers have three pins, a 3.3 V Vdd pin, a ground pin and the switch input pin. The input switch pin is arranged between the Vdd and ground pins such that a header jumper is used to switch for one to the other. For room temperature testing the jumpers can be moved by hand to obtain the desired gain factor.

4.2 Temperature Testing

4.2.1 Test Setup

For temperature testing of the tunable BGR, the test board must be placed in a heating/cooling chamber. The internal temperature of the chamber can be set to accommodate the temperatures needed for testing. The chamber has an electric heating source and liquid nitrogen for cooling. This allows the chamber to achieve very low temperature around negative one fifty degrees Celsius. A

bias test board containing six packaged parts was placed into the chamber with external connections for power and ground as well as switch inputs and voltage reference outputs for each part. Temperature testing was then performed from -95 °C to 125 °C in the order in which is described. The chamber was set to room temperature or 25 °C and measurements of all six chips were taken. The chamber temperature was then increased by 20 °C to 45 °C and measurements were taken. This was repeated every 20 °C until 125 °C was reached and measured. Then the lower temperatures were measured. The liquid nitrogen was turned on and the chamber set to 5 °C and measurements were taken. Again the temperature was decreased in 20 °C increments and measured results were taken till -95 °C was reached. The chamber was first heated and then cooled, in order to eliminate any moisture that may have been present in the chamber before the cooling process began.

4.2.2 Output Voltage

From the temperature chamber testing, output voltages were measured from all six packaged parts in 20°C increments from -95°C to 125°C. Measurements from each chip consists of all four switch setting, for the three different gain factors, with two switch setting being the same gain factor. Each of the six chips measurements where plotted on a chip-by-chip basis showing the four different switch setting. Six total chips were measured and of these chips, 2 wafers were represented. The voltage reference output of each chip over temperature is shown in Figures 4.1 through 4.6.

4.2.3 Temperature Coefficient

The temperature coefficient of each chip was taken with respect to each switch setting. Equation (1.1) was used to determine the TC of each temperature sweep. These measured calculations are given in Table 4.1.

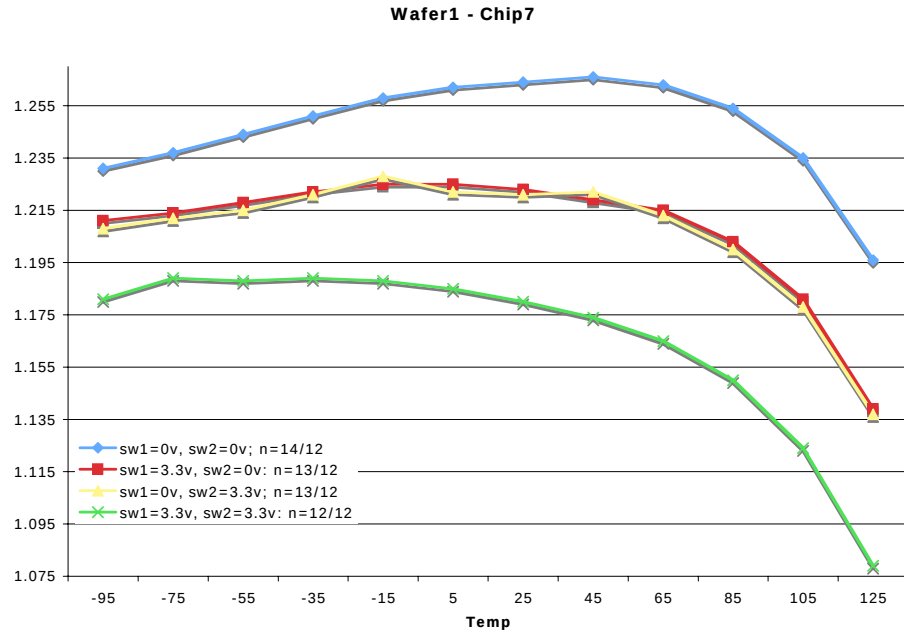


Figure 4.1 Output Reference Voltage of Wafer 1 - Chip 7

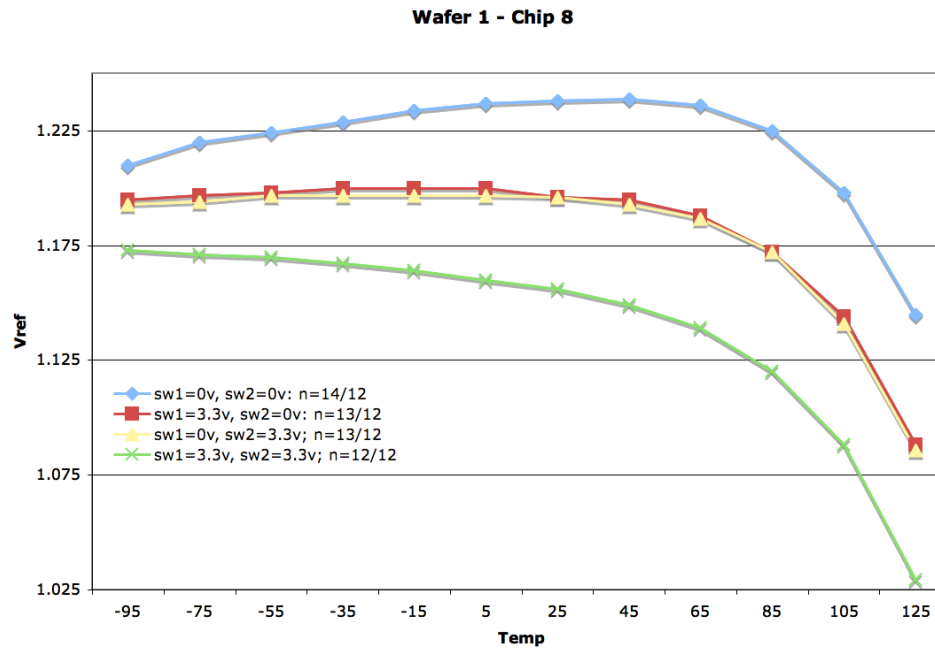


Figure 4.2 Output Reference Voltage of Wafer 1 - Chip 8

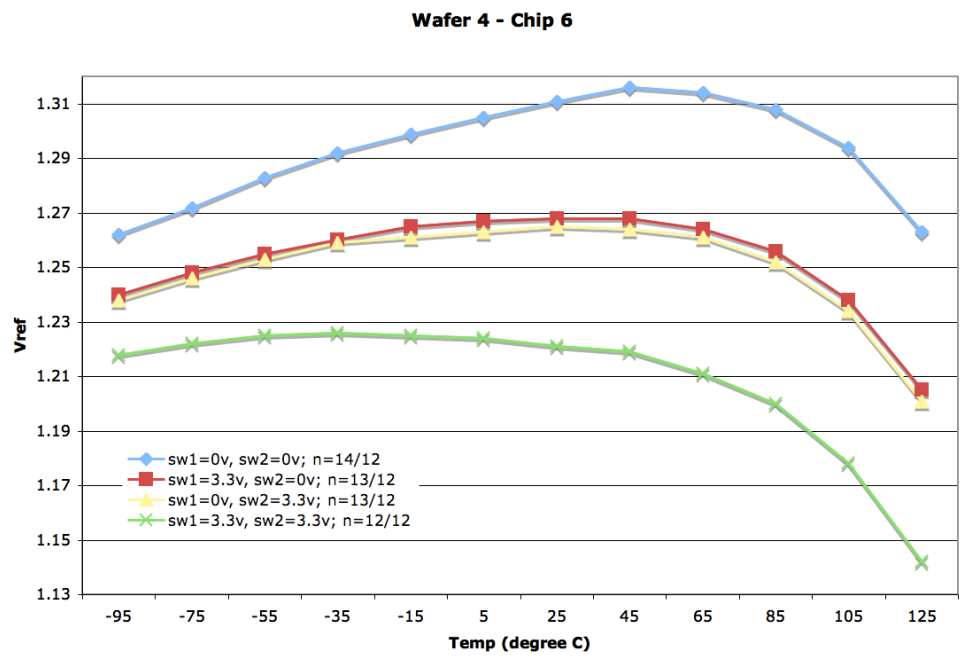


Figure 4.3 Output Reference Voltage of Wafer 4 - Chip 6

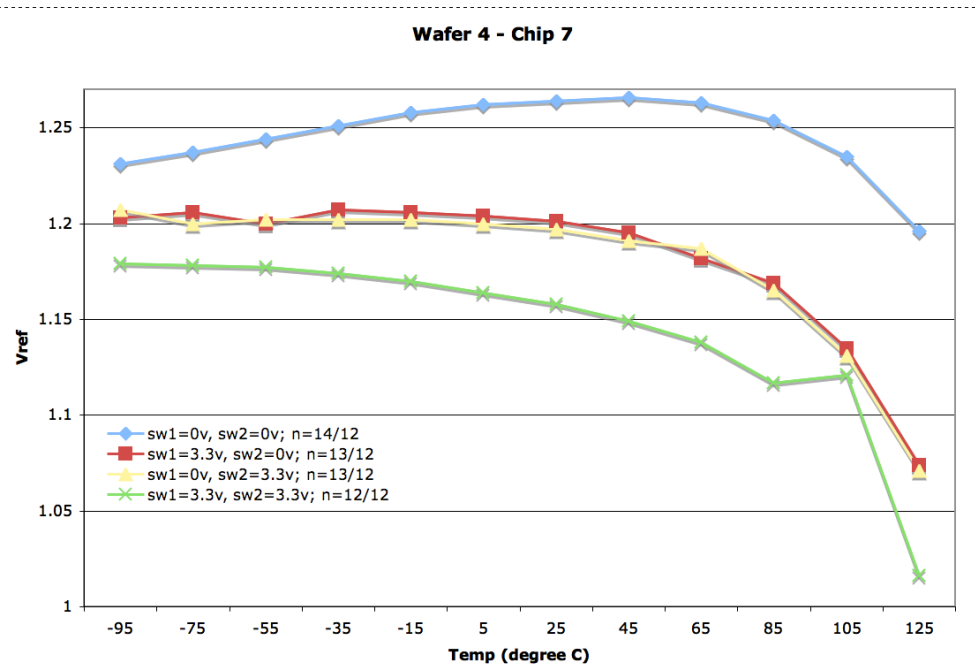


Figure 4.4 Output Reference Voltage of Wafer 4 - Chip 7

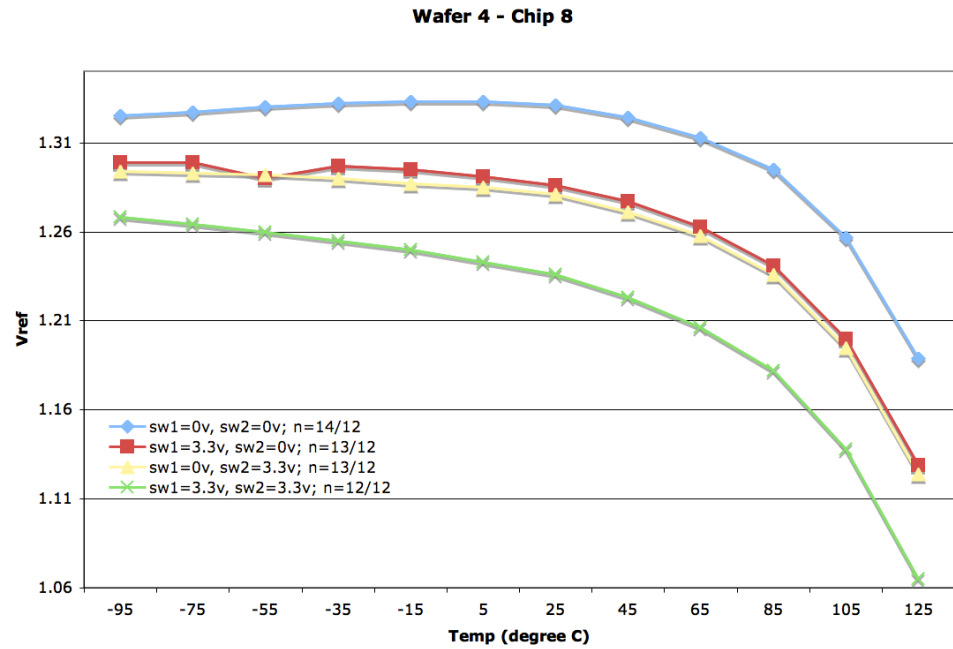


Figure 4.5 Output Reference Voltage of Wafer 4 - Chip 8

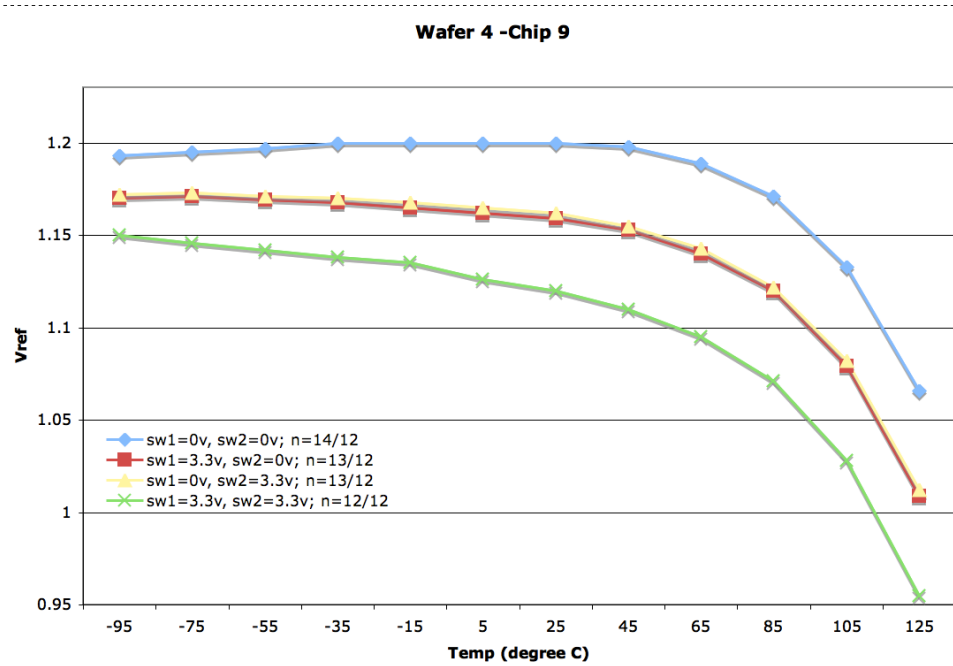


Figure 4.6 Output Reference Voltage of Wafer 4 - Chip 9

Table 4.1 Temperature Coefficients for Measured Parts in ppm per degree Celsius.

Temperature Coefficients (ppm/°C)				
Wafer – Chip	sw1 = 0 V, sw2 = 0 V	sw1 = 3.3 V, sw2 = 0 V	sw1 = 0 V, sw2 = 3.3 V	sw1 = 3.3 V, sw2 = 3.3 V
W4-C6	250.00	291.67	296.30	388.89
W1-C7	324.07	398.15	421.30	509.26
W1-C8	435.19	518.52	513.89	666.20
W4-C7	513.89	615.74	629.63	754.63
W4-C8	666.67	787.04	787.04	939.81
W4-C9	620.37	750.00	745.37	902.78

From Table 4.1 it can be seen that difference switch settings have better temperature drift performance. This should be taken into account before the use in a specific application.

The temperature drift for measured parts is very different from that of the simulated results. From Figures 3.6 through 3.8 the worst case TC can be calculated to be about 200 ppm/°C. The worst case from the simulated results is not as much as the best case from the measured results. It is thought to be caused by a poor diode model. The process used was a newer 150 nm process that did not have good modeling for diode structures. That is why this type of tunable bandgap reference was very suitable for this process. The tunability of the BGR, allowing the output voltage to be changed with digital input switches, tolerates some fluctuation in the output voltage and in chip-to-chip variation. Because output voltage can be tuned, chip-to-chip and wafer-to-wafer variations can be minimized. Next another bandgap voltage reference will be shown for comparison.

4.3 Alternate Bandgap Reference Comparison

An Alternate bandgap voltage reference [9] was fabricated with and on the same chips and wafers as the tunable BGR. This alternate bandgap reference uses a topology that is designed to be less sensitive to chip-to-chip variation. This circuit topology is shown in Figure 4.7. Through design the output voltage of the reference should fluctuate less from chip-to-chip and from wafer to wafer than a standard bandgap voltage reference. For comparison the worst-case chip-to-

chip and wafer-to-wafer variations at room temperature will be shown for the alternate BGR and the tunable BGR. Figure 4.8 shows the worst-case chip-to-chip variation of the tunable bandgap reference. These two chips represent the worst-case nominal output voltage differentiation of all the measured results for chip-to-chip variation. These two chips with the same current gain factor for normal operation, $n = 13/12$, have a chip-to-chip variation of 115 mV. If the gain factor is changed, bringing one output voltage down and bringing one output voltage up, then the chip-to-chip variation is minimized to only 21 mV. That is over a 500 % reduction in chip-to-chip variation. The alternate bandgap voltage reference, that is designed to minimize chip-to-chip variations, had a worst-case chip-to-chip variation of 29 mV. From measured results comparing two different topologies from the same fabrication process and the same chips, the chip-to-chip output voltage variation of the tunable bandgap voltage reference with tuning was less than that of the alternate voltage reference designed to minimized chip-to-chip variations. This is a huge finding. Instead of using a more complex and larger design, a simpler and smaller design can be used to

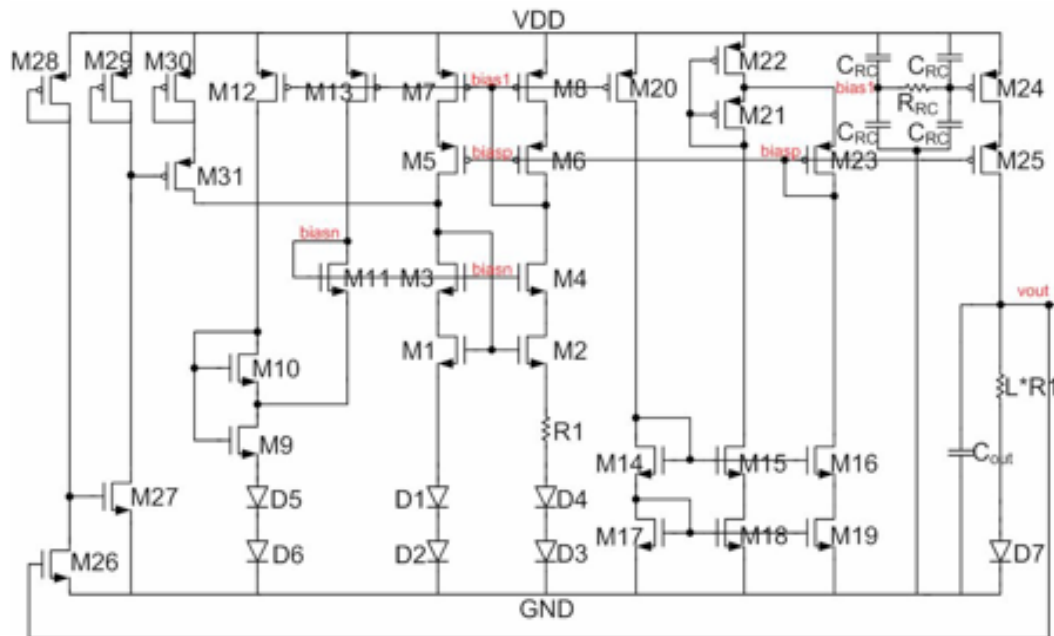


Figure 4.7 Schematic of Alternate BGR

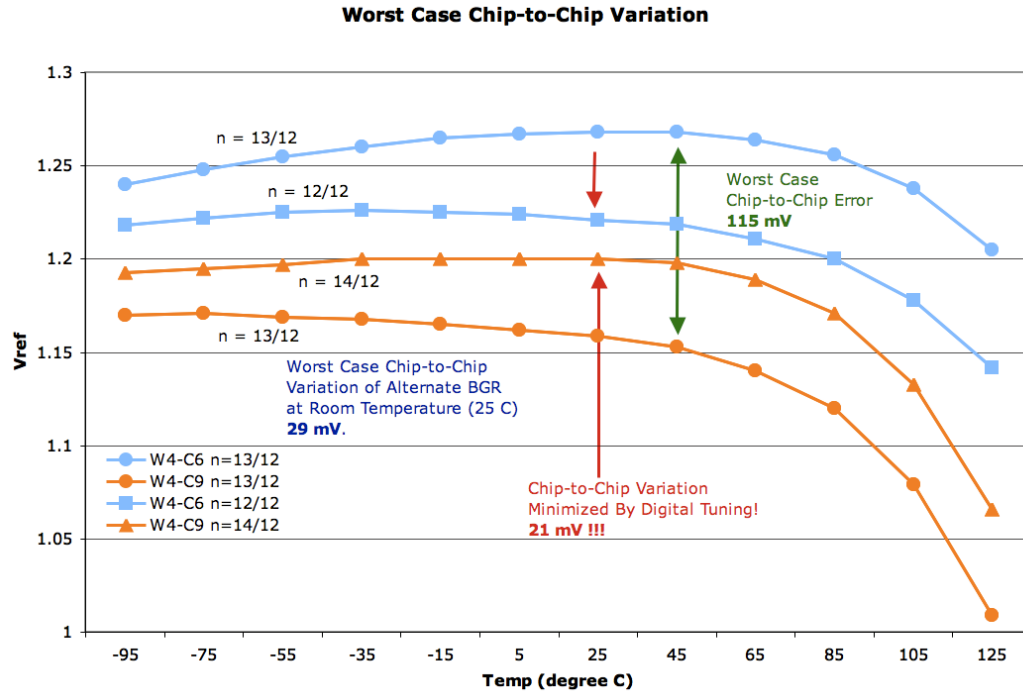


Figure 4.8 Worst Case Chip-to-Chip Variation Minimized by Tuning

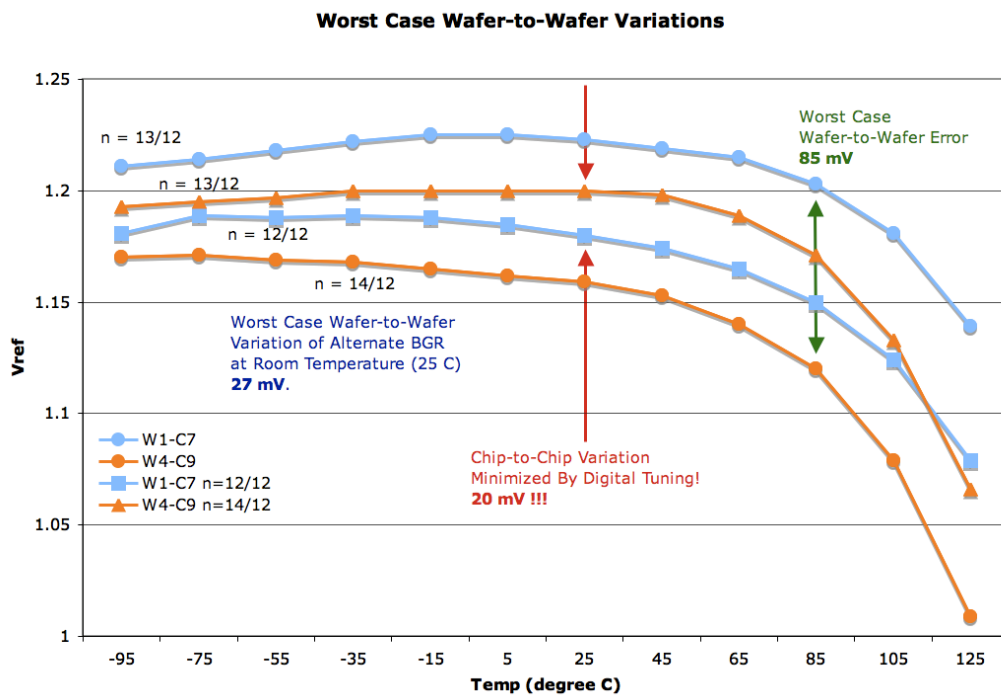


Figure 4.9 Worst Case Wafer-to-Wafer Variation Minimized by Tuning

produce better results. The same was done for wafer-to-wafer variations shown in Figure 4.9. These two chips represent the worst-case nominal output voltage differentiation of all the measured results for wafer-to-wafer variations. These two chips with the same current gain factor for normal operation, $n = 13/12$, have a wafer-to-wafer variation of 85 mV. If the gain factor is changed, bringing one output voltage down and bringing one output voltage up, then the wafer-to-wafer variation is minimized to only 20 mV! That is over a 400 % reduction in wafer-to-wafer variation through tunability. Here again the alternate BGR that was designed to minimize chip-to-chip and wafer-to-wafer variations has a worst-case wafer-to-wafer variation of 27 mV. From measured results comparing two difference topologies from the same fabrication process and the same chips, the wafer-to-wafer output voltage variation of the tunable bandgap voltage reference with tuning was less than that of the alternate voltage reference designed to minimized chip-to-chip and wafer-to-wafer variations. Again, instead of using a more complex and larger design, a smaller, simple design can be used to produce better results through tuning.

4.4 Power Supply Rejection

The PSR of the circuit was measured during testing. Power was applied to the circuit at 3.0 V and 3.6 V and measurement for each chip was taken at each voltage. The difference of these two voltages was calculated and the PSR was derived per Equation (1.2). These values were recorded and are listed in Table 4.2.

Table 4.2 Measured Power Supply Rejection in dB

Wafer – Chip	Power Supply Rejection (dB)
W1-C7	- 44.5
W1-C8	-45.3
W4-C6	-43.5
W4-C7	-45.0
W4-C8	-48.5
W4-C9	-46.5

Chapter 5 *Conclusions and Recommendations*

5.1 Conclusions

In this Thesis the idea of a tunable self-biasing bandgap voltage reference was explored. The design and methodologies of how a tunable BGR was constructed were given along with simulation results that proved its probability. Measured results from fabricated parts were given, showing the advantages of a simple tunable reference and how it achieves better performance than alternate BGRs. The alternate voltage reference was more complex, consumed more power and used more area than the tunable BGR but, was designed for low chip-to-chip and wafer-to-wafer variation. However, through digital tuning the reference design shown in this Thesis achieved lower chip-to-chip and wafer-to-wafer variations than the alternate BGR designed specifically for that purpose. The tunable design is simple and very powerful in that as many switches can be used as is reasonable for the design, though only 2 tuning switches were used in this Thesis favorable results were found.

5.2 Recommendation and Future Work

For the tunable bandgap reference shown in this Thesis, the cascode devices of the self-biasing reference, $M_3 - M_6$ in Figure 3.6, were for simplicity in design matched to the upper and lower PMOS and NMOS devices. For better matching and performance these cascode devices should be sized smaller than the upper and lower PMOS and NMOS devices, and sized such that they have equal saturation voltage drops as their corresponding upper and lower PMOS and NMOS devices. This helps set equal voltage drops across D_1 and D_2 and the resistor.

Another recommendation is to use more digital tuning switches. Only two were used in this design but 4, 8 or more could be used and an input digital word could set the switch values. With more switches, designed correctly, should produce finer current gain adjustment and finer output tuning. Also, using a

process with a well established diode model would be ideal. Unfortunately that was not the case for this design. However, with a better model simulation results should produce more accurate representation of measured results.

Final recommendation and future work should include a design using an alternate topology, designed for low chip-to-chip variation like the alternate BGR shown in this Thesis, that also uses tuning switches. Fine results have been seen in this Thesis, but accompanying tuning with a design to minimize variation should prove to be quite revolutionary.

LIST OF REFERENCES

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- [1] B. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, John Wiley and Sons, Inc., ISBN 0-471-70055-X, 2005.
- [2] B. J. Baker, *CMOS Mixed Signal Circuit Design*, John Wiley and Sons, Inc., ISBN 0-471-22754-4, 2002.
- [3] Paul R. Gray, Paul J. Hurst, Stephen H Lewis, Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley-InterScience, ISBN 0-471-32168-0, 2001.
- [4] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, ISBN 0-072-38032-2, 2000.
- [5] David A. Johns, Ken Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, Inc., ISBN 0-471-14448-7, 1996.
- [6] P. Brokaw, "A Simple Three-Terminal IC Bandgap Voltage Reference," *IEEE J. Solid-State Circuits*, vol. Sc-9, December, 1974.
- [7] J. F. Pierce and T. J. Paulus, *Applied Electronics*, Bell & Howell Company, ISBN 1-878907-42-5, 1972.
- [8] Donald A. Neamen, *Semiconductor Physics and Devices: Basic Principles*, McGraw-Hill
- [9] Tony Antonacci, Designer of the Alternate Bandgap Voltage Reference used for comparison, Tony at the time of fabrication was a Lab Colleague and at the time of writing a Design/Test Engineer at Texas Instruments.

Vita

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