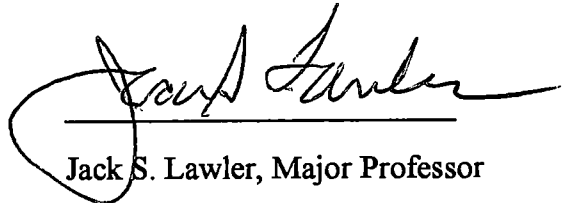


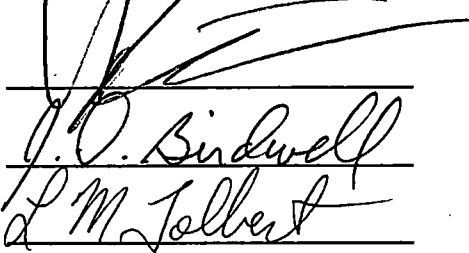
To the Graduate Council:

I am submitting herewith a dissertation written by Hui Li entitled "Modeling and Control of a High Power Soft-switched Bi-directional DC/DC Converter for Fuel Cell Applications." I have examined the final copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.



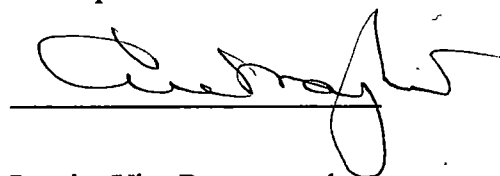
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Modeling and Control of a High Power Soft-switched Bi-directional DC/DC Converter for Fuel Cell Applications

A Dissertation

Presented for the

Doctor of Philosophy Degree

The University of Tennessee

Hui Li
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ABSTRACT

This work presents a new high power, bi-directional, isolated dc-dc converter for a fuel cell energy management system that will be fitted into a test vehicle being built by Ford Motor Company. The work includes two parts. The first part is to propose a new topology and analyze the principles of the circuits operation. Design guidelines with detailed circuit simulations are presented to verify the feasibility of the new circuit topology. Based on the conceptual understanding of the converter, the mathematical model is also derived to design a control system that achieves soft start-up and meets the performance requirements. The second part is to fabricate a 1.6 kW prototype converter in the laboratory. Using the prototype, the steady state performance of the open loop system was tested to verify the analysis and simulation results.

A dual half-bridge topology is presented to implement the required power rating using the minimum number of devices. Unified zero-voltage-switching (ZVS) is achieved in either direction of power flow to eliminate switching losses for all devices, increase the efficiency of the system and reduce the electromagnetic interference (EMI). Compared to the other soft-switched dc-dc converters, neither a voltage-clamping circuit nor extra switching devices and resonant components are required in

the proposed circuit for soft-switching implementation. All these new features allow efficient power conversion and compact packaging.

Different start-up schemes are proposed to successfully limit the in-rush current when the converter is started in the boost mode of operation. The full control system including the start-up scheme is developed and verified using simulation results based upon the average model.

A 1.6 kW prototype of the converter has been built and successfully tested under full power. The experimental results of the converter's steady-state operation confirm the simulation analysis.

PREFACE

The automotive industry is now in a new era in alternative propulsion [1]. The fuel cell shows great promise for next-generation propulsion with the highest efficiency and lowest emissions potential. The fuel cell concept was first advanced in 1839 by Sir William Grove, a physicist in England, who produced electricity from the electrochemical reaction of hydrogen and oxygen [1]. In the 1960s to 1970s, fuel cells powered Gemini and Apollo spacecraft. Nowadays they are used aboard the space shuttles. In the next decade, it is believed that this space age technology will be used to propel ordinary motorists looking for efficient, clean transportation.

When a fuel cell energy system is fitted into a vehicle, it needs a bi-directional dc/dc converter as its auxiliary power supply. This dissertation provides a systematic study of converter a new circuit for this application.

Chapter I introduces the background, motivation, and the objectives of this research on a new soft-switched bi-directional dc-dc converter.

Chapter II presents a review of the literature on fundamental soft-switching techniques and bi-directional dc-dc converter topologies. Two main approaches of soft-switching implementation are introduced by illustrating the Resonant DC Link (RDCL) Inverter and the Auxiliary Resonant Commutated Pole (ARCP) Inverter. The reported bi-directional dc-dc converters are classified into four categories: (1) Low

power, non-isolated bi-directional dc-dc converters, (2) Low power, isolated bi-directional dc-dc converters, (3) High power, isolated bi-directional dc-dc converters and (4) High power, soft-switched, isolated bi-directional dc-dc converters. Four different topologies of the last category are elaborated in detail, and the operating principles of each topology are discussed.

Chapter III presents the circuit description, operating modes and the soft-switching implementation of the new converter. A steady state analysis and important design guidelines are discussed in this chapter. The cycle-by-cycle performance of the converter is simulated by PSIM [2] software to verify the analysis.

Chapter IV discusses the limitations of the traditional state-space averaging method when it is applied to the proposed circuit. A new switching-frequency-dependent averaged model is developed and simulated with Matlab/Simulink. The dynamic performance of open-loop and closed-loop converter systems is simulated and studied. The simulation results using the proposed average model are compared to those of detailed circuit simulation to validate this technique.

Chapter V provides an overall control system design. First, small signal analysis is used to generate the required transfer functions. The root locus of the control-to-output transfer function provides the information on the poles, zeros and the gain of the uncompensated converter. Based on the above information, a controller is designed by trial and error. Second, two different start-up schemes are presented. The topology and dynamic performance of each approach is studied and compared. The advantages and disadvantages of each approach are discussed. The overall control

system is designed to meet start-up requirements and to achieve the desired overall system stability and transient response characteristics.

Chapter VI presents a numerical design example, hardware and software implementation, and experimental results using a 1.6 kW prototype. The steady state analysis and design equations are used to select the components in the power circuit under worst case conditions to ensure proper operation of the converter. After a prototype was built in the laboratory, the static performance of the proposed topology was obtained and compared with the simulation results. A preliminary estimate of conversion efficiency was obtained experimentally.

Chapter VII summarizes the main contribution of this dissertation. Avenues for research to achieve additional improvements are also discussed.

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LIST OF SYMBOLS

L_{dc}	DC input inductor
L_s	Transformer leakage inductance
$C1\sim C4$	Split capacitors
C_p	Split capacitor of low voltage side
C_s	Split capacitor of high voltage side
$Cr1\sim Cr4$	Resonant capacitors
C_o	Bus capacitor of high voltage side
R, R_{load}	Load resistor
Tr	Isolation transformer
$S1\sim S4$	Main devices
$D1\sim D4$	Anti-parallel diodes of $S1\sim S4$
D	Duty cycle
f_s	Switching frequency
V_b, V_{in}, v_{in}	Battery voltage
$I_{d1}, I(L_{dc}), i_l$	Current flowing through the inductor
$I_{r1}, I(L_s), i_r$	Current flowing through the primary side of transformer
I_{r2}	Current flowing through the secondary side of transformer

$V_1 \sim V_4, v_1 \sim v_4$	Voltages of capacitors C1~C4
$V_{cr1} \sim V_{cr4}$	Voltages of capacitors Cr1~Cr4
$V_{s1} \sim V_{s4}$	Collector-to-emitter voltages of switches S1~S4
V_{r1}, v_{r1}	Voltage of the primary side of transformer
V_{r2}, v_{r2}	Voltage of the secondary side of transformer
V_o, v_o	Output voltage
I_{s1}	Current flowing through S1 and D1
I_{s2}	Current flowing through S2 and D2
I_{s3}	Current flowing through S3 and D3
I_{s4}	Current flowing through S4 and D4
V_s	The voltage source of high voltage bus

CHAPTER I

INTRODUCTION

The objective of this research is to develop a bi-directional dc-dc converter. This chapter first describes the application background, a fuel cell energy system, and the constraints imposed by the anticipated application on the dc-dc converter design. Then the problems of present state-of-the-art designs are identified in section I.2. The main objectives of this dissertation are outlined in section I.3.

I. 1 Background

Fuel cells are energy conversion devices that generate clean electricity directly and efficiently, by oxidizing hydrogen and leaving only nonpolluting byproducts - water and heat. Therefore, fuel cell technology is a prospective candidate to replace the widely used internal combustion engines (ICEs) in traditional cars or conventional batteries used in today's electric vehicles (EVs) and become the primary power source for the next generation hybrid electric vehicles (HEVs).

Because of the lack of an energy storage function in the fuel cell, it is required to have a relatively large dc-dc converter for an auxiliary energy storage application in vehicles. A bi-directional dc-dc converter in a fuel cell system is shown in Fig.1.1. Fig.1.1 is a conceptual block diagram of the fuel cell power bus and energy system.

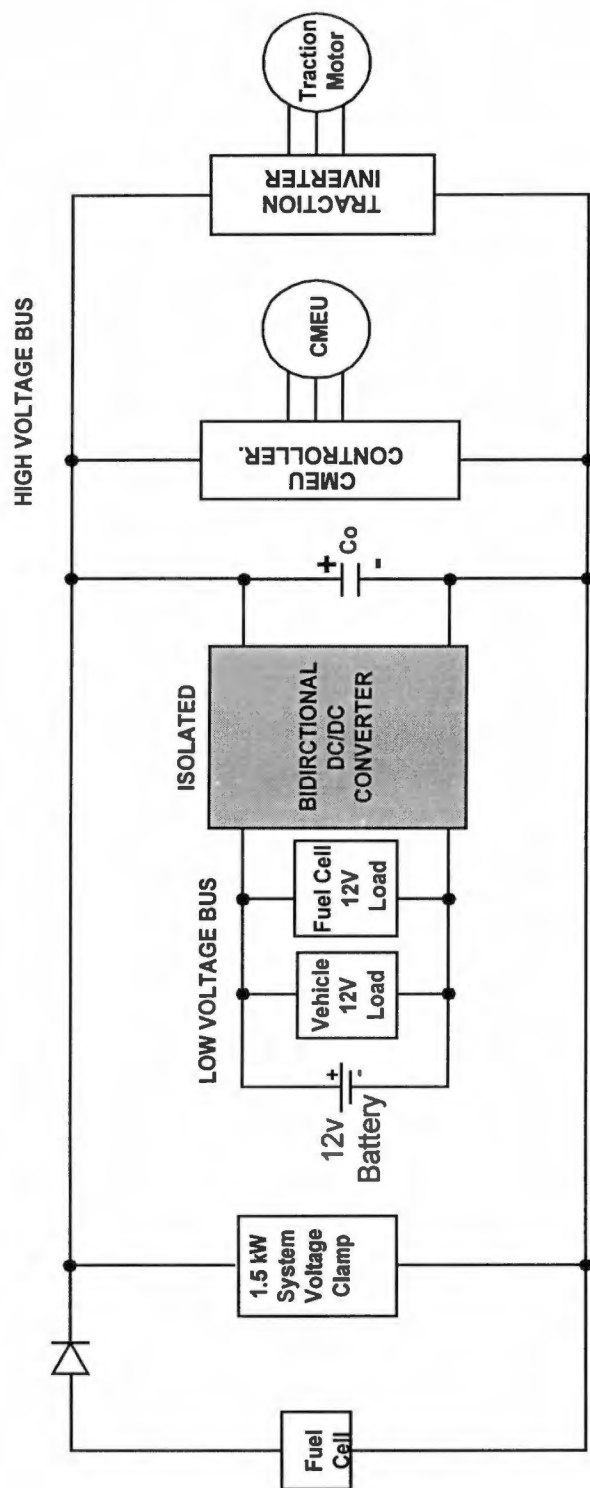


Fig. 1.1 Block diagram of fuel cell power bus and energy management system

The battery voltage is usually selected as 12 Volts for compatibility with the majority of today's automobile loads. The system operation is to have the 12 V battery derived power to boost the high voltage bus up to 288 V during starting. Then this voltage is provided for the fuel cell compressor motor expanding unit (CMEU) controller and to bring up the fuel cell voltage, which in turn feeds back to the high voltage bus to release the loading from the battery. In addition, regenerated power from the traction motor is absorbed by the battery.

For such a fuel-cell energy system application, the functions of this dc-dc converter are two-fold: first, to boost the high voltage bus to a desired voltage before the fuel cell can generate power; and second, to store the regenerative power from the traction motor drive. The expected requirements of this converter are outlined as follows:

- An Isolated, bi-directional dc-dc converter rated at 1.6 kW continuous power is required.
- A heavy duty SLI (starting, lighting and ignition) battery with a nominal voltage of 12 V is used on the low voltage bus. The terminal voltage of the battery can swing from 8 V to 16 V during either direction of power flow.
- The nominal voltage of the high voltage bus is 288 V, with an operating range from 255 V- 425V.
- The maximum power requirement of 1.6 kW occurs during battery discharge (boosting up the high voltage bus during starting).

- A maximum battery charging power of 5 kW is required for a maximum duration of 20 s during regeneration. Each such charging event is at least 1 minute apart.
- The high voltage bus capacitance C_o must be less than 2000 μF .
- A start-up time of less than 200 ms is required with load engaged when the high voltage bus voltage is higher than 255 V.

I. 2 Problem Specifications

From Fig.1.1, the bi-directional dc-dc converter is a key element of a fuel cell energy system. However, most of the existing dc-dc converter topologies are low power, unidirectional, and can not meet the above requirements.

In recent years, several high power isolated bi-directional dc-dc converters have been proposed [3]-[6]. The common issues associated with high power bi-directional dc-dc converters include:

- (1) Hard switching losses. The hard switching losses of devices consist of turn-off and turn-on losses, which are caused by the switch having simultaneous nonzero current and voltage of switching. These losses lead to a significant decrease in converter efficiency.
- (2) Overshoot voltage. At switching, a high and sharp voltage spike appears at devices due to the energy stored in the leakage inductance. These spike results in increased electromagnetic interference (EMI), and a voltage clamp circuit is used to protect the devices.

(3) Start-up problem. When the converter begins to establish the output voltage, it works like a boost converter. In addition, the anticipated application expects the output voltage to be built up very fast even when a large bus capacitor is used. Limiting the in-rush current and speeding up the start-up process are major concerns.

The converters reported in the literature use full bridge topologies and soft-switching techniques to tackle one or more of the problems listed, but at the expense of a large number of devices, more complicated topologies and control schemes, or higher component stresses.

To date, the most attractive topology [6] for fuel cell energy system application is shown in Fig. 1.2. Compared to other converters, it has fewer magnetic components, easily achieves soft-switching, soft start up and has higher efficiency. The circuit consists of two full bridges placed on each side of an isolation transformer. A clamp branch composed of an active switch and a capacitor is used to achieve soft switching operation in both directions of power flow. In the regeneration mode of operation, the converter implements hybrid zero-voltage and zero-current switching for the high voltage-side (HVS) switches by using a control-timing modified scheme over the clamp branch. In the discharging mode of operation, the same clamp branch is mainly used to limit the transient voltage on the low voltage-side (LVS) switches; at the same time, zero-voltage switching is also realized for all the LVS switches, including the auxiliary clamp switch. An extra flyback winding is added on the main choke to implement soft start up before the output voltage is established. A non-phase-shifting

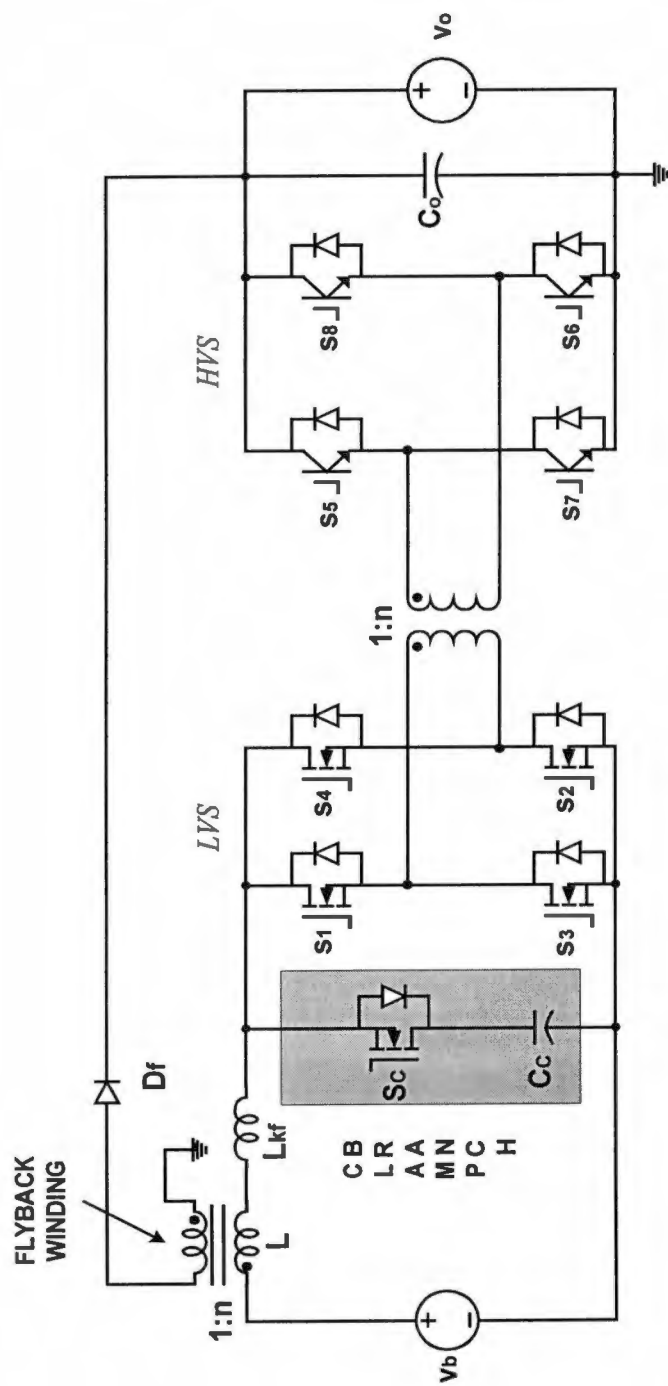


Fig. 1.2 Boost full bridge/buck full bridge dc/dc converter

type of control scheme is adopted to realize PWM control in both start-up and regular discharging mode of operation and to ensure smooth transitions between them.

Despite its advantages, this converter has the following problems.

- (1) The dual full bridge topology requires eight main devices and an auxiliary switch.

The excessive number of switching devices and their gate drive circuits and the power supply circuits of the gate driver circuits, make the package bulky, costly and less reliable than the configuration proposed later in this work.

- (2) Although all the devices achieve soft switching making the switching loss small or zero, the conduction loss of the excessive number of devices lowers system efficiency.

- (3) The switches of the low voltage side still suffer the high voltage surge at switching because of the leakage inductance of the loop. Therefore a voltage clamp circuit is needed to protect them against over-voltage. In addition, special consideration must be given to the power stage layout and transformer design to reduce the leakage inductance.

- (4) In order to limit the current and speed up the start-up process, an extra flyback winding is used, which adds still more complexity to the topology and design.

- (5) The control is complicated because it needs to generate gate signals for eight devices and a clamp circuit. In addition, the soft-switching implementation of the charging and discharging mode controls are different. The complicated control will further decrease the system reliability.

Besides these problems identified above, the mathematical models of high power bi-directional isolated dc-dc converters have never been addressed in the literature. Usually the well-known approach to the modeling of a switching converter is to approximate its operation by averaging techniques. For example, the popular state-space averaging method [7] formulates the dynamic equations in state space form for each of the topological modes during one complete switching cycle. The averaged model is then obtained by taking a weighted average of the system matrices, where the weighting factor for each state is its duty ratio. Although the conventional averaging techniques are useful for modeling some converter systems, these methods are difficult to apply to the class of high power isolated bi-directional dc-dc converters. The main problems are:

- (1) The isolation transformer brings in high frequency ac voltage and ac current. These ac variables have zero average values over every switching cycle. However, it is hard for a traditional state-space averaging technique to separate and cancel them from other dc variables of the circuit.
- (2) Conventional averaging techniques are independent of switching frequency. The averaging approximation is based on the assumption that the switching frequency is “fast enough”, but it is not known precisely how fast “fast enough” must be. As a result, the average models that are derived may not be accurate when the switching frequency is low. This will not be acceptable if the switching frequency is a possible control variable.

I. 3 Objectives of the Study

The objective of this work is to develop a new soft-switching converter to achieve high efficiency and reliability at less cost, and in a highly compact package.

Therefore the desired circuit should:

- (1) Use a minimum number of devices.
- (2) Achieve soft switching for all the switches to reduce the switching loss. In addition, the auxiliary circuit used solely to aid soft switching should be eliminated.
- (3) Implement soft start up without adding extra magnetic components.
- (4) Eliminate the high transient turn-off voltage for the low voltage side devices to avoid using a clamp circuit.
- (5) Allow for easy implementation of control algorithms including soft switching and start-up schemes.
- (6) The simplified mathematical model should be available to aid system simulation, analysis and controller design.

CHAPTER II

SUMMARY OF PREVIOUS WORK

Soft-switched, high power, isolated bi-directional dc-dc converters are the expected candidates for fuel cell applications to reduce switching loss, improve EMI and increase the efficiency. Therefore, soft-switching techniques are reviewed in this chapter. Bi-directional dc-dc converters are then introduced, starting with basic bi-directional converters, continuing through low power isolated converters, and ending with high power isolated converters. In the third section, the state-of-the-art topologies of high power, bi-directional, soft-switched dc-dc converters are discussed with regard to their advantages and problems. It is desirable to develop a new topology that can overcome or improve the problems within the existing circuits.

II. 1 Soft Switching Techniques

Traditional hard-switching inverters pose several problems that are reviewed below. Fig. 2.1 illustrates the device voltage, current and power during hard switching [8].

During turn-on, the device current rises from zero to the load current with additional diode reverse recovery and stray capacitor charging and discharging

currents. During turn off, the device voltage rises to the bus voltage with an overshoot due to the leakage inductance in the loop. Therefore the peak switching power loss is high, as shown in Fig. 2.1. Another switching problem is the voltage rise and fall rate. Typically, the rate of change of the voltage, dv/dt , for hard switched devices is higher than 2,000 V/us. This high value may damage the switches and causes EMI problems.

The soft-switching technique was developed in the 70's [8] to solve these problems. The idea of soft switching is to switch a device only when the voltage across it or the current flowing through it is zero. The various implementations of soft switching are described in Fig. 2.2 (a)-(d) [9].

Soft-switching techniques have the following advantages:

- Switching losses are reduced/eliminated, resulting in improved efficiency and reduced heat sink size and cooling requirements.
- Lower switching dv/dt results in reduced EMI associated with switching.
- Higher frequency switching is possible thereby avoiding audible noise.

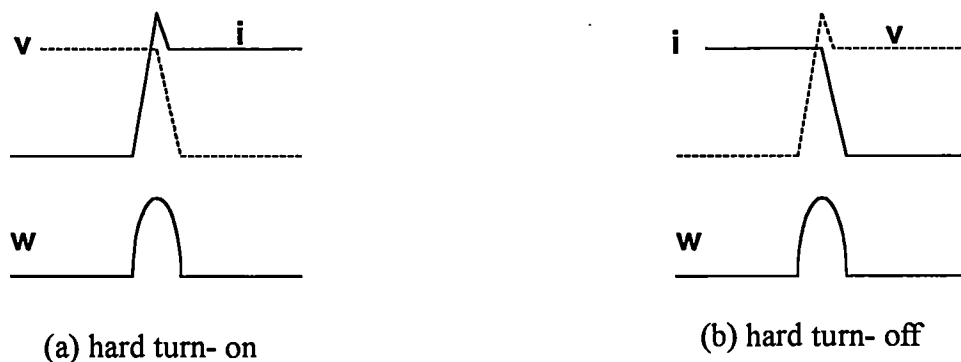
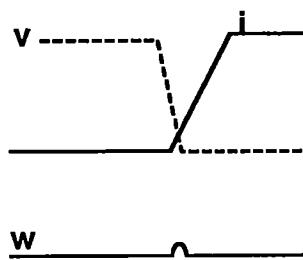
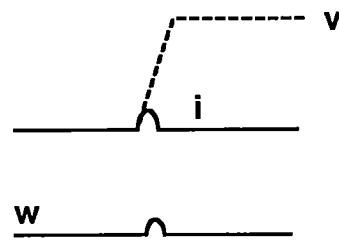


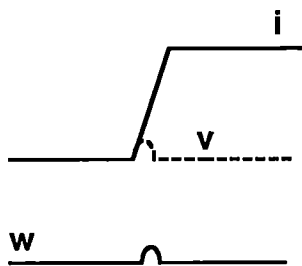
Fig. 2.1 Hard switching of devices



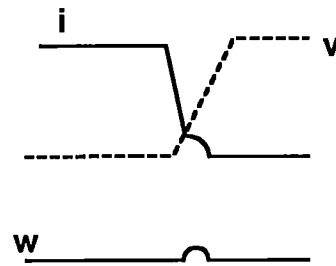
(a) zero current
turn- on



(b) zero current
turn- off



(c) zero voltage
turn- on



(d) zero voltage
turn- off

Fig. 2.2 Soft switching of devices

Representative soft-switching converters include dc-dc converters and dc-ac inverters. Examples of soft-switched dc-dc converters are the parallel output SRC (series resonant converter) operated above resonance [10], the pseudo-resonant converter, the resonant pole [11]-[12], and all quasi-resonant converters [13]-[15]. For dc-ac inverter applications, typical examples of soft-switched topologies are the resonant dc link inverter [16] and the resonant pole inverter [17]. Although many different converter topologies have been proposed, there are two general approaches to achieve soft-switching. In the first method, the voltage across the switch or the current through the switch is forced to a zero crossing or zero gap by creating a LC-resonant circuit. The second technique involves auxiliary resonant circuits, which with special control causes the diode in anti-parallel to the switch to be turned on first. Apart from these main techniques, turn-off of a device with a snubber capacitor across it is considered to be soft-switching due to the fact that the voltage is built up in a controlled manner, resulting in low switching loss. Similarly, turn-on of a device with a series inductance with zero initial current is also considered to be soft switching.

Only one representative from each family is described here. The Resonant DC Link (RDCL) Inverter [16] of the first approach and the Auxiliary Resonant Commutated Pole (ARCP) Inverter [17] of the second approach, have been selected to explain the basic differences in soft-switching methods.

Fig. 2.3 is the RDCL inverter topology, the simplified inverter system and the resonant voltage waveform are shown in Fig. 2.4 (a)-(b). In the RDCL converter, a resonant circuit, incorporated with an active clamping switch and clamping capacitor,

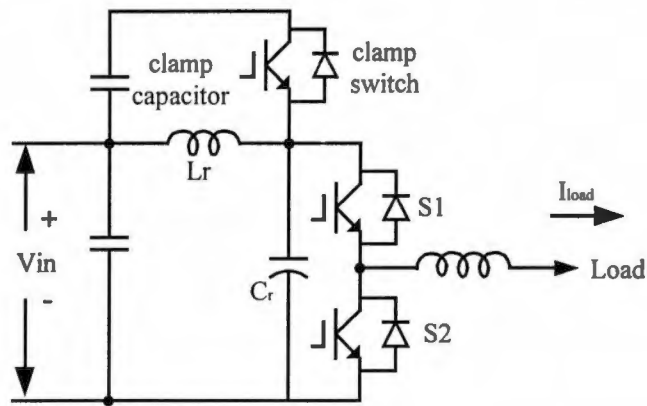


Fig. 2.3 RDCL inverter topology

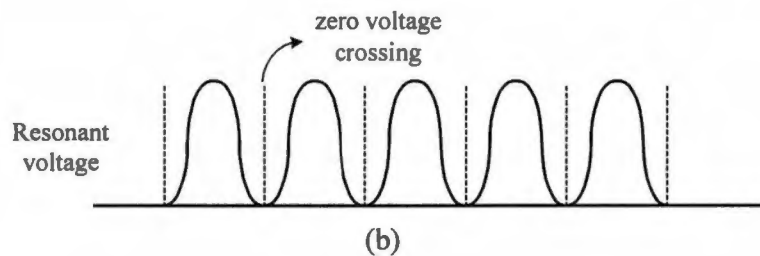
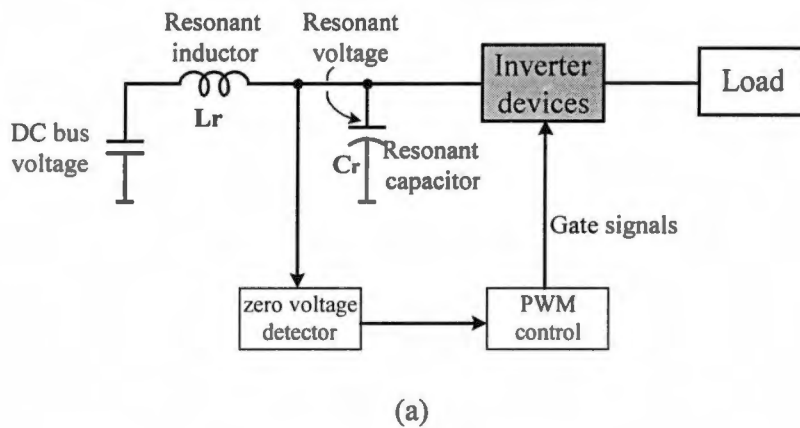
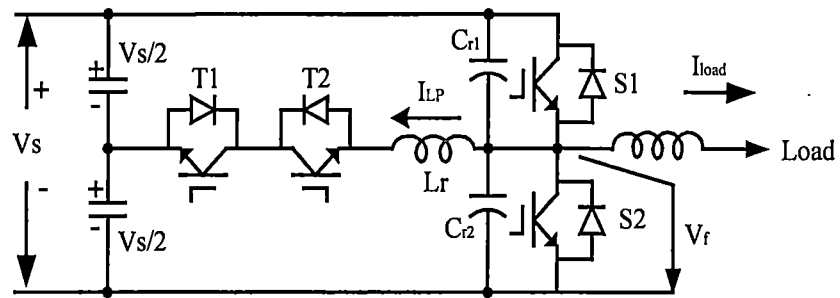


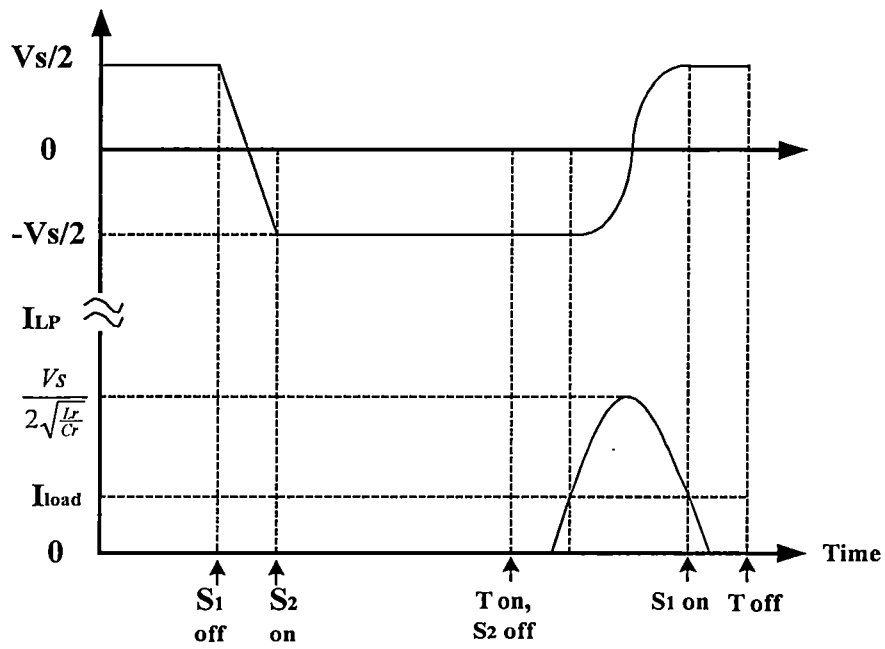
Fig. 2.4 The Resonant DC Link (RDCL) inverter
(a) Simplified RDCL inverter system (b) Resonant voltage

is used over and above the basic hard-switching inverter. The RDCL resonates periodically and brings the dc link voltage to zero once each cycle. The inverter switching devices are switched on and off at zero voltage instants of the resonant dc link, thus achieving lossless switching. As devices are switched, the initial excitation conditions of the resonant circuit are changed, and peak voltage stresses may increase under certain modulation, the clamp switch and clamp capacitor are used to limit the peak voltage across the device

The ARCP inverter has capacitor snubbers across each main device, as well as a resonant inductor L_r and two auxiliary devices T1 & T2 per phase of the inverter, as shown in Fig.2.5. There are two commutation modes in this topology. One is switch-to-diode commutation. When this commutation happens, turn-off of a conducting main device causes the snubber capacitor to charge up in a controlled manner, resulting in a turn-off at zero voltage. The currents in the load inductance and in the resonant inductor allow a reversal of the inverter phase voltage so that the anti-parallel diode of the incoming main device can be conducted first, the main device is then turned on at zero voltage. When the load current is low, an auxiliary device needs to be fired to assist the commutation process. Turn-off of a main device when the diode across it is conducting is another commutation mode called diode-to-switch-to-diode commutation, and requires that an auxiliary device be gated. This transfers current from the diode to the main device and allows the main device to be turned off as before.



(a)



(b)

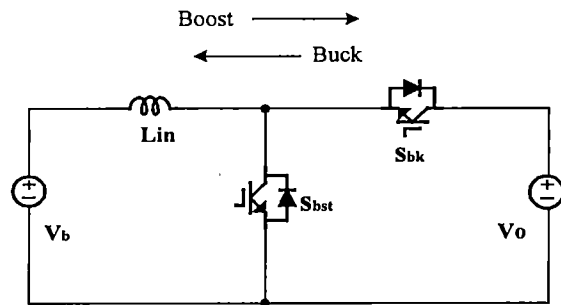
Fig. 2.5 The Auxiliary Resonant Commutated Pole(ARCP) inverter
(a) Simplified ARCP inverter system (b) Switching voltage and current

II. 2 Bi-directional DC/DC Converter Topologies

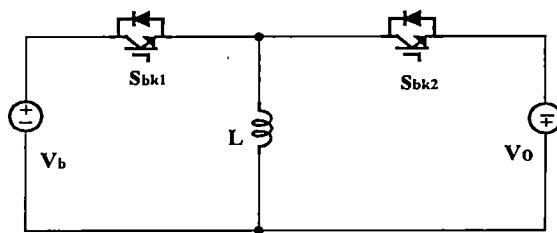
Theoretically, replacement of the diode rectifiers in a unidirectional dc/dc converter topology with a diode and switch combination naturally leads to bi-directional power processing capability, with a few exceptions such as the single-ended forward converter. Figs. 2.6 (a) and (b) show two basic bi-directional dc-dc converters in their simplest non-isolated and single-ended form. The circuit of Figure 2.6 (a) is a current-fed topology when operated in the boost mode and is voltage-fed when operated in the buck mode. The circuit of Figure 2.6 (b) is symmetrical in either direction of power transfer. More complicated bi-directional converter topologies can generally be viewed as variations of these two basic topologies. These variations include a bridge topology instead of a single-switch, and a transformer isolated topology instead of a non-isolated one.

In applications where isolation is needed either to provide electrical isolation between the input and the output, or to provide load and source voltage matching or scaling, a bi-directional isolated flyback converter provides the simplest solution because only two active switches and a single magnetic component are required, as shown in Fig. 2.7. However, the power handling capability of a flyback converter is practically limited to several hundred watts due to the buck-boost operation nature and the transient voltage problems on both sides.

Figs. 2.8 (a) – (c) show the possible variants of the high power isolated bi-directional dc-dc converters according to their terminal characteristics seen from both



(a) Current-fed/voltage-fed topology



(b) Buck-boost or flyback topology

Fig. 2.6 Basic bi-directional dc-dc converter topologies

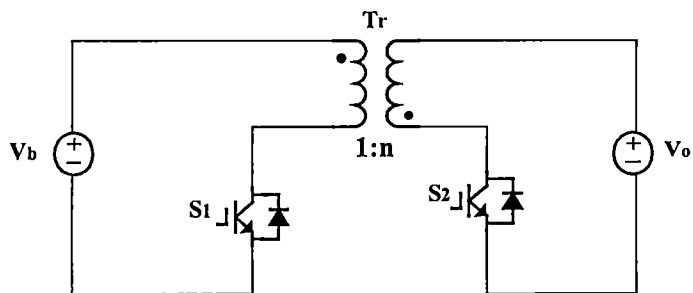
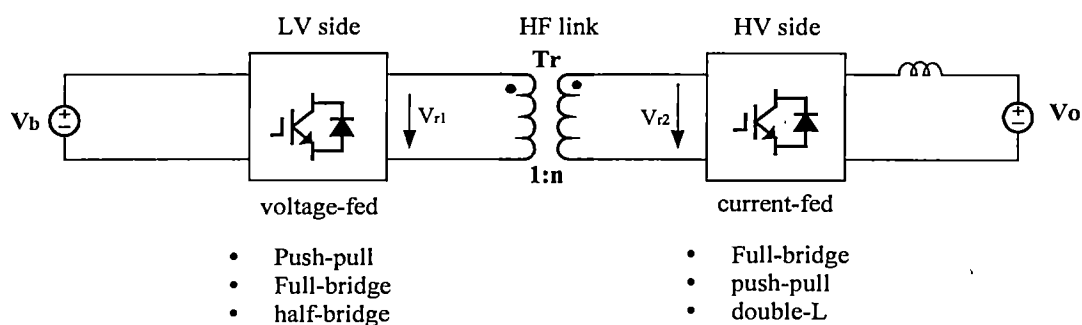
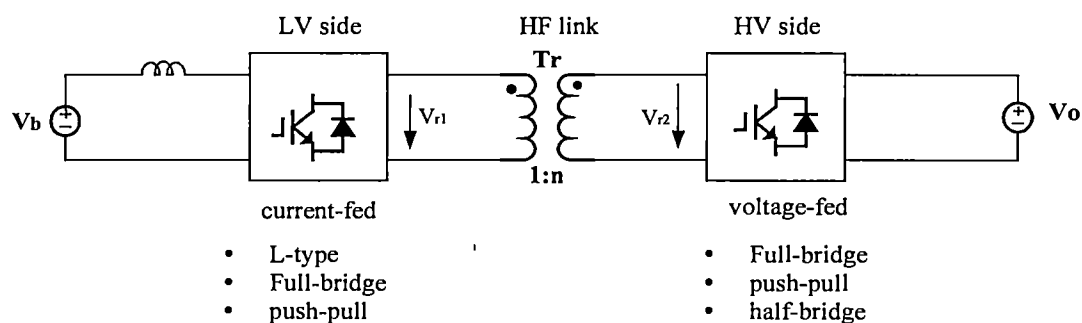


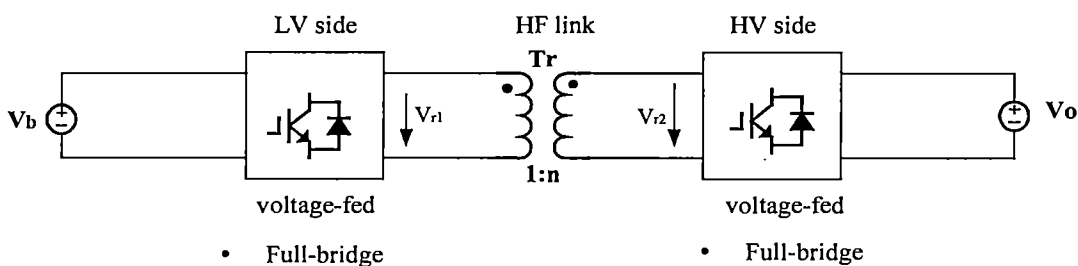
Fig. 2.7 Low power isolated bi-directional flyback converter



(a) Voltage-fed on LV side



(b) Current-fed on LV side



(c) Voltage-fed on both sides

Fig. 2.8 The basic high power isolated bi-directional dc-dc converters

sides. They are categorized into three basic families: (a) voltage-fed on LV side and current-fed on HV side, (b) current-fed on LV side and voltage-fed on HV side, and (c) voltage-fed on LV and HV side. Common to all three families is a high frequency transformer, which performs voltage transformation and ground path isolation. On each side, there needs to be a high-frequency converter, which is also capable of rectifying depending on the direction of power transfer.

For fuel cell system applications, the selection of circuit topologies is dominated by the following requirements (1) Low voltage and high current on the LV side, (2) bi-directional operation, and (3) High voltage conversion ratio. Low cost, high efficiency, manufacturability, and compactness are also among the important factors. With these requirements in mind, a special class of bi-directional dc-dc converters, high power isolated soft-switched converters, will be introduced in the following section.

II. 3 Soft-switched isolated bi-directional dc-dc converter schemes

For fuel cell applications, the soft-switched, high power, bi-directional dc-dc converters are the expected candidates. However, this class of converters has not been popular, and only limited applications are reported in literature. Fig.2.9 through Fig.2.12 are all the topologies reported so far.

The circuit of Fig.2.9 is proposed in [3], [4],[19]. It can be viewed as one of the topologies in Fig. 2.8 (c). A voltage-fed converter bridge is employed on both sides of the isolation transformer. The operation of the circuit involves the utilization of the

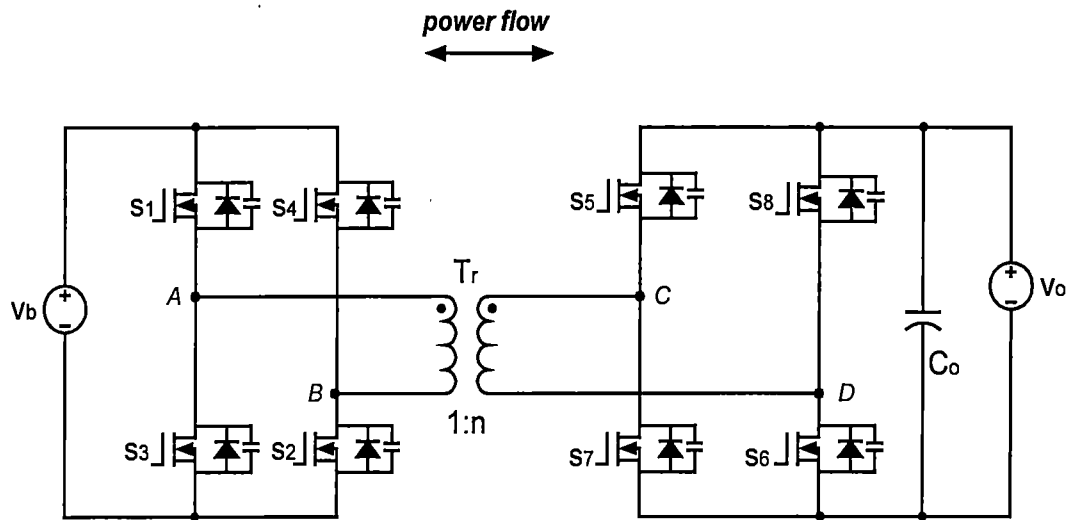


Fig. 2.9 Dual active full bridge bi-directional dc-dc converter

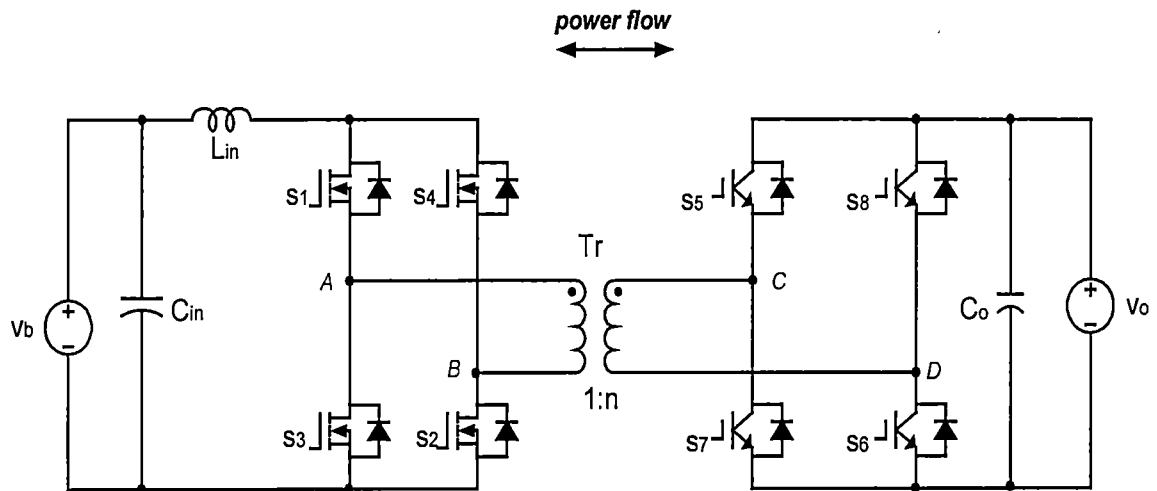
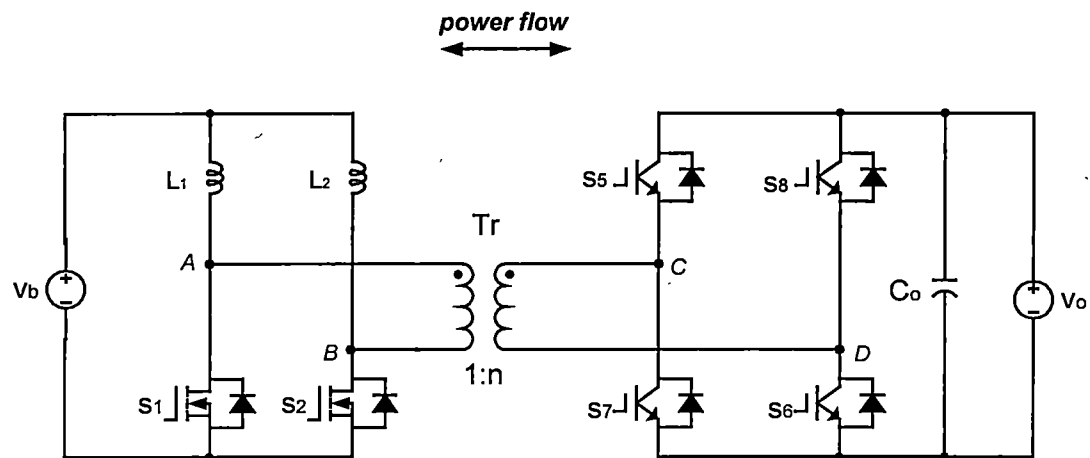
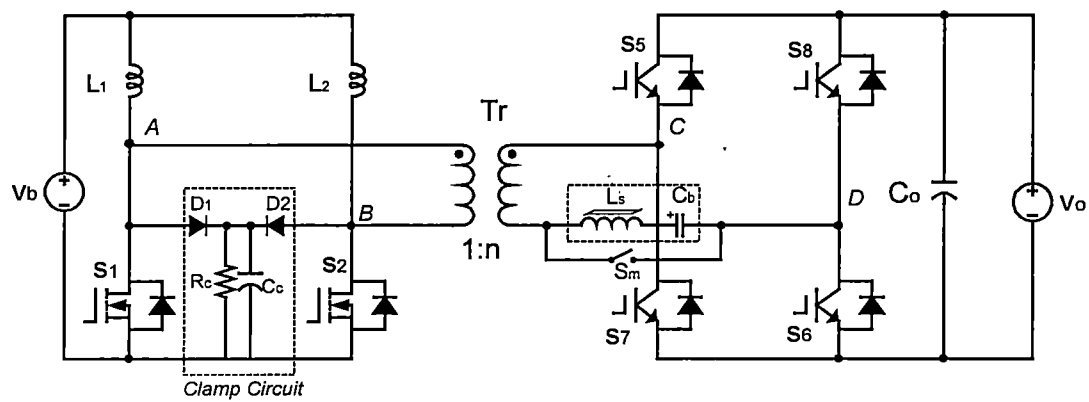


Fig. 2.10 Dual voltage-fed/current-fed full bridge bi-directional dc-dc converter



(a) Ideal circuit



(b) Converter with a passive clamp and ZVZCS circuit

Fig. 2.11 L-type boost/full-bridge voltage-fed bi-directional dc-dc converter

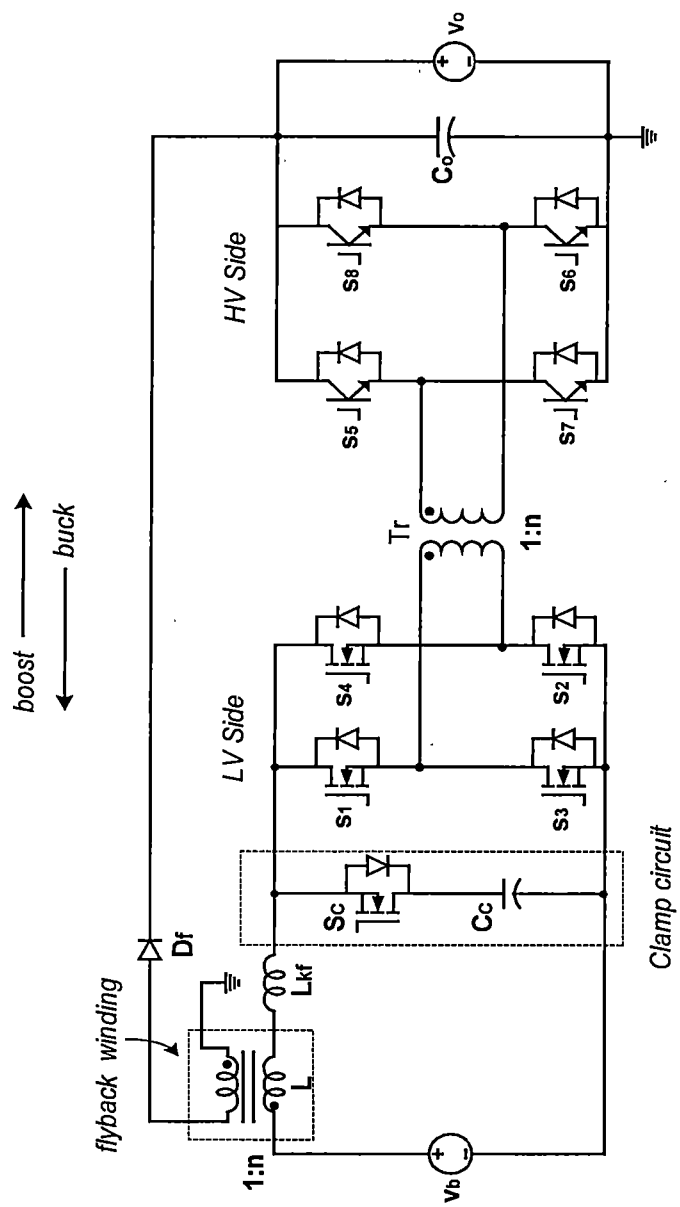


Fig. 2.12 Boost full bridge/buck full bridge dc/dc converter

leakage inductance of the transformer as the main energy storing and transferring element. The power transfer is controlled by phase shifting the voltages exerted on the two sides of transformer. Because the LV side is voltage-fed, there is no start-up problem in this topology. The circuit operates in a soft-switched manner for devices on both sides: zero-voltage turn-on is obtained by ensuring that device turn-on only occurs when its anti-parallel diode is conducting. Meanwhile, the lossless snubber across the device assists the zero-voltage turn-off. Therefore, the voltage spikes caused by interaction between the leakage inductance and diode reverse recovery during hard switching is eliminated. Although the device voltage stress on both sides is low, the switches of both sides suffer from high current stress, leading to high conduction loss and decreased efficiency.

Fig. 2.10 is proposed in [5]. It can be viewed as the extension of the topology shown in Fig.2.6 (a). However, the adopted control method relies on the simultaneous activation of the bridges on both sides for power flow in either direction. Although zero-current switching (ZCS) can be achieved for some of the switches, a high transient voltage exists across the current-fed switches caused by the leakage inductance of transformer. The switches therefore must be protected from over-voltage. During start-up operation when the power is transferred from LV side to HV side, the switches do not have ZCS, resulting in high switching losses. As a result, the circuit must start-up with reduced power.

The scheme [6] in Fig. 2.11 has L-type current-fed converter on the LV side and the voltage-fed full-bridge converter on the HV side. A high transient voltage

appears on the current-fed side switches, and needs to be clamped to secure the circuit operation. It is well known that any current-fed type converter (boost converter) has no capability to limit the switch current during start-up before the output bus voltage has been established. Therefore, extra start-up windings with high voltage isolation need to be added to both of the inductors in order to implement soft-start. The hybrid zero-voltage and zero-current switching (ZVZCS) operation for the switches of the HV side can be achieved in this topology. When the power flows from the HV side to the LV side, the switches of one leg of the HV side can achieve ZCS because the freewheeling primary leakage current could be reset to zero, while the other leg turns on at zero voltage because the anti-parallel diode conducts first. In order to achieve ZVZCS operation for the HV side, an extra commutation circuit containing a saturable inductor L_s and a small blocking capacitor C_b needs to be placed in series with the high-voltage side transformer link. However, this circuitry is harmful to boost mode operation, and therefore needs to be shorted with an extra switch S_m when boost mode is operated. As a result, the circuit topology is very complicated and packaging becomes difficult. The efficiency is also not high.

Fig. 2.12 shows the schematic of a boost full bridge/buck full bridge dc/dc converter [6]. The circuit includes a clamp branch composed of an active switch and a capacitive energy storage element, which has two functions. First, it is activated to achieve soft switching in both directions of power flow. Second, it is used to clamp the high transient voltage caused by the leakage inductance of the transformer. In the buck mode of operation, the converter achieves hybrid zero-voltage and zero-current

switching for the HV side switches. In the boost mode, zero voltage turn on is implemented for the LV side switches, while the high transient turn off voltage is clamped by the auxiliary switch S_c . In order to achieve soft start up operation, an extra flyback winding is required in this topology to accelerate the establishment of output voltage by transferring energy to the output. When the output voltage is higher than nV_b , the flyback-winding path is automatically disengaged from the circuit, and the circuit operates in regular boost converter mode.

II. 4 Summary

This chapter describes the need of a new soft-switched bi-directional dc-dc converter for fuel cell application. Various combinations of current-fed and voltage-fed converters are explored for different voltage levels. From a literature review, the soft-switched dc-dc converters will achieve higher efficiency and better EMI than hard switched topologies. Four soft-switched dc-dc converters have been reported in the literature. The study shows that even the most attractive topology in Figure 2.12 still suffers from an excessive number of switches, a complicated circuit and control strategy, and high transient voltages for the LV side switches due to the leakage inductance of transformer.

In order to solve these problems, a new topology is presented in the next chapter. The circuit is capable of achieving soft switching for all the switches without any auxiliary active devices. The control complexity is decreased. High transient voltage spikes for the LV side devices are also eliminated, making a clamp circuit

unnecessary. The circuit also performs well during start-up by allowing soft switching of devices and limiting the current.

CHAPTER III

DUAL HALF BRIDGE BI-DIRECTIONAL CONVERTER WITH A UNIFIED SOFT-SWITCHING SCHEME

In this chapter, the circuit description, operation principle, steady state analysis and design guidelines of a new bi-directional converter with soft-switching are presented.

III. 1 Circuit Description

The application of a bi-directional dc-dc converter in a fuel cell system shown in Fig 1.1 is redrawn in Fig. 3.1 for convenience.

The system's operation is reviewed here. The 12 V battery provides power to boost the high voltage bus up to 288 V during starting. Then this voltage is provided for the fuel cell compressor motor expanding unit (CMEU) controller and brings up

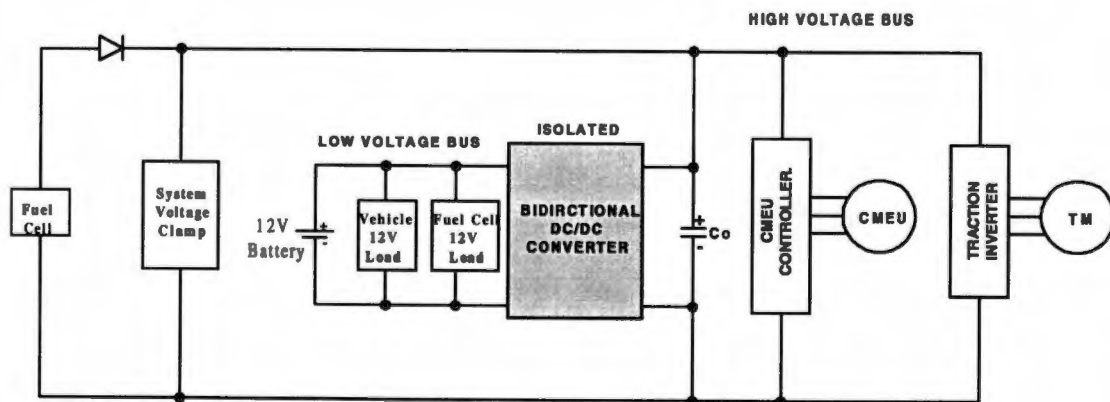


Fig. 3.1 Block diagram of fuel cell power bus and energy management system

the fuel cell voltage. Once the fuel cell is operational, loading is released from battery. When the traction motor operates in the regeneration mode, the bi-directional converter returns power to the battery.

The proposed bi-directional half-bridge dc/dc converter is shown in Fig. 3.2. This circuit is operated with dual half-bridges placed on each side of the main transformer Tr. When power flows from the low voltage side (LVS) to the high voltage side (HVS), the circuit is current-fed, or in other words, works in boost mode to keep the HVS voltage at a desired high value. In the other direction of power flow, the circuit is voltage-fed, or works in buck mode to absorb regenerated energy. The HVS switches are implemented with IGBTs, and the low voltage-side switches are MOSFETs. The capacitive snubber across each switch is a lossless, or energy recovery type. The capacitance C_o is less than 2000 μ F. A transformer in the high frequency link provides the advantages of isolation and voltage level boost in the secondary side. The leakage inductance of the transformer is used as the main energy storage and transfer element.

The use of the dual half-bridge topology instead of a dual full-bridge configuration can be justified as follows. A comparison of TDR (Total Device Rating) in full bridge and half bridge of boost mode is shown in Fig. 3.3. Switches in the full bridge are subject to a voltage stress equal to the dc-input voltage, and the current stress is equal to the load current. The TDR of the full bridge is calculated as $TDR_F = V_{dc} \cdot I_{ac} \cdot 4/P_o = 4$. In order to get the same output power, the voltage stress of a switch in the half bridge is twice the dc input voltage, and the current stress is the

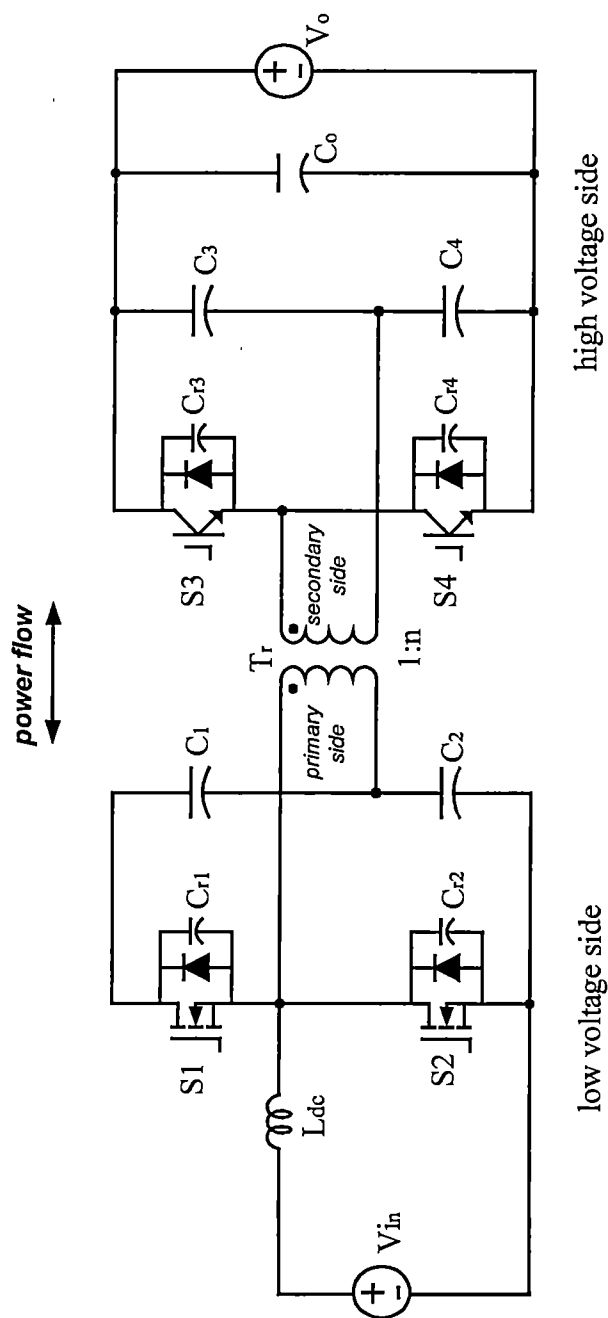
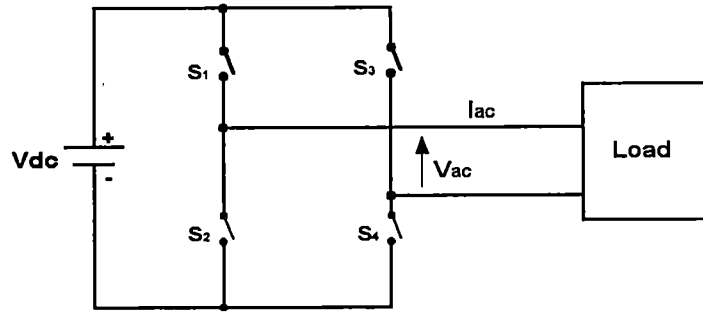
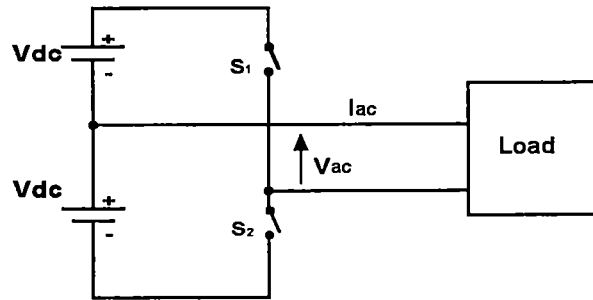


Fig .3.2. Soft-switched bi-directional half-bridge dc/dc converter



(a) Full-bridge



(b) Half-bridge

Fig. 3.3 The comparison of full-bridge and half-bridge

same as that of a full bridge. Similarly, the TDR of the half-bridge can be calculated as $TDR_H = 2V_{dc} \cdot I_{ac} \cdot 2/P_o = 4$. The conclusions can be made as follows: (1) The total device rating is the same for the dual half bridge topology and the dual full bridge for the same output power. (2) Although the devices of the half-bridge are subject to twice the dc input voltage, this is not a big concern because the dc input voltage in the anticipated application is 12 Volts. (3) The dual half bridge topology uses only half the number of devices as the full-bridge topology. The other advantage of the proposed

circuit is the unified soft-switching capabilities in either direction of power flow. This will be described in the following section.

III. 2 Principles of Operation

In this section, the principles of current-fed/boost mode and voltage-fed/buck mode operation are described. The implementation of soft switching in both modes is also illustrated. Verification of these principles through simulation is also presented.

In order to simplify the circuit analysis, the primary-referred equivalent circuit is drawn in Fig. 3.4, where the transformer Tr is replaced with a leakage inductance L_s .

III. 2. 1 Current-fed/Boost Mode

When power is transferred from the current-fed bridge to the voltage-fed bridge, the converter is working in boost mode. The interval t_0 to t_{12} of Fig. 3.5 describes the various stages of operation during one switching period. The converter operation is repetitive in the switching cycle. One complete switching cycle is divided into thirteen steps. Each step is described briefly below. To aid in understanding each step, a set of corresponding annotated circuit diagrams is given in Figure 3.6.

Step 1 (before t_1): Circuit steady state. S1 and D3 are conducting.

Step2 ($t_1 - t_2$): At t_1 , S1 is turned off. Cr1, Cr2 and T_r begin to resonate, making V_{cr2} fall from $V_1 + V_2$. V_{r1} also drops from V_1 . The rate of change depends on the magnitude of I_{off} which is the difference between I_{r1} and I_{d1} at t_1 .

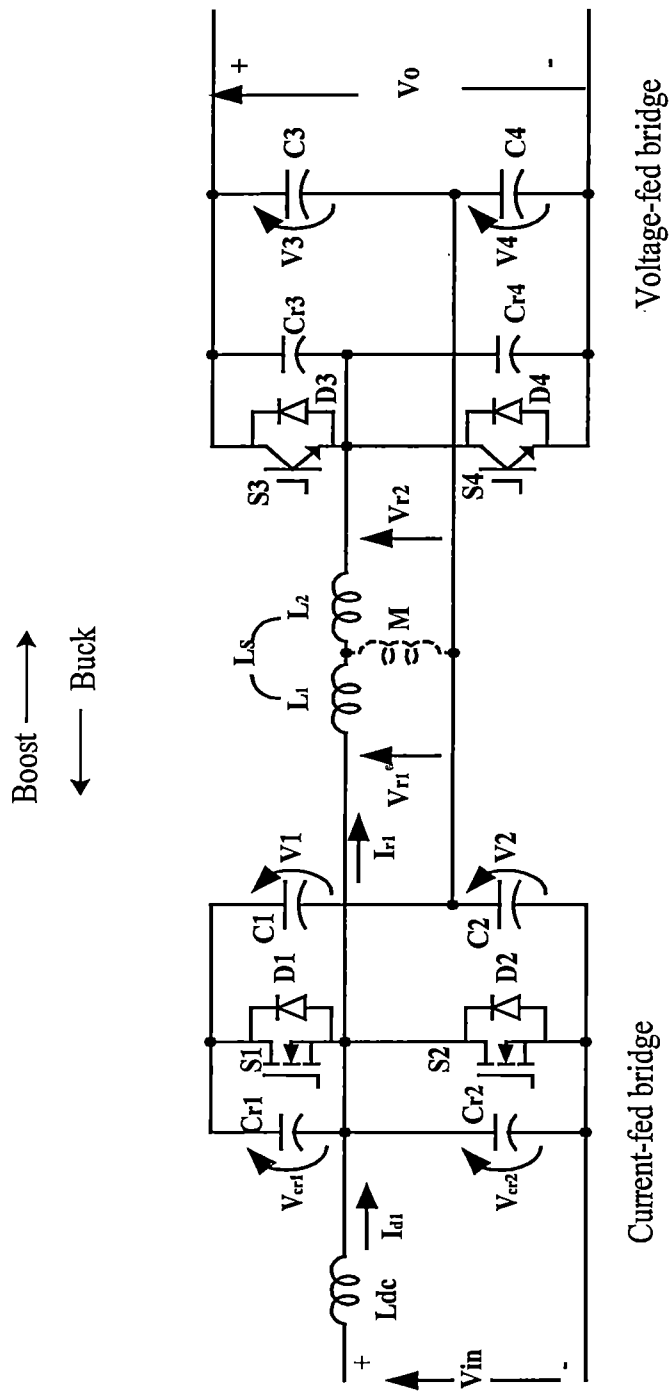


Fig. 3.4 Primary referred equivalent circuits

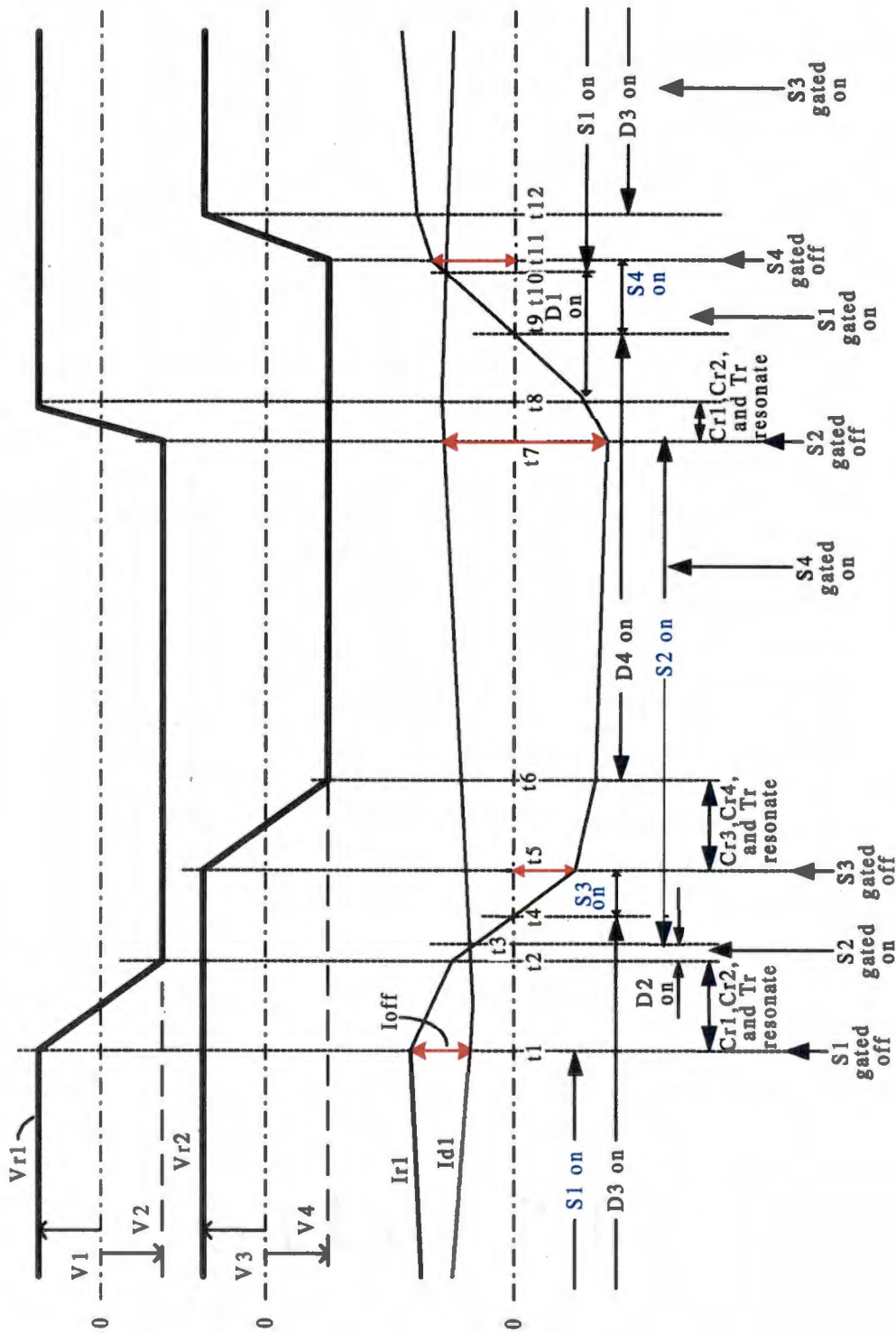
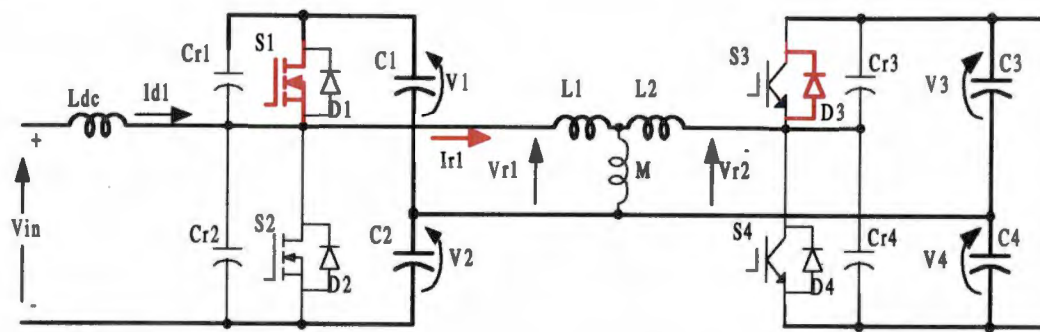
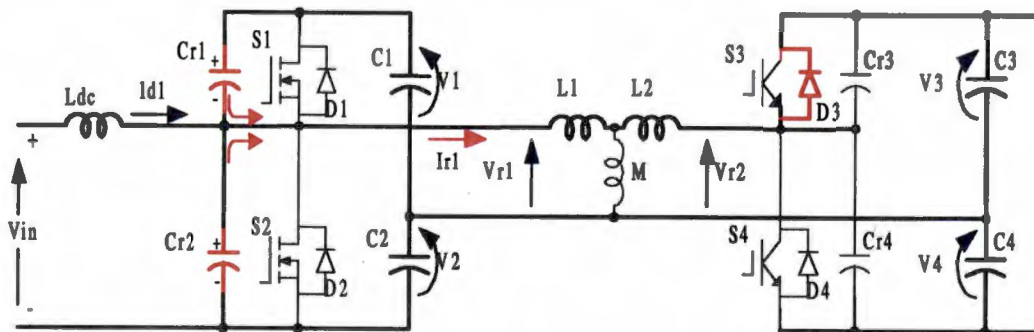


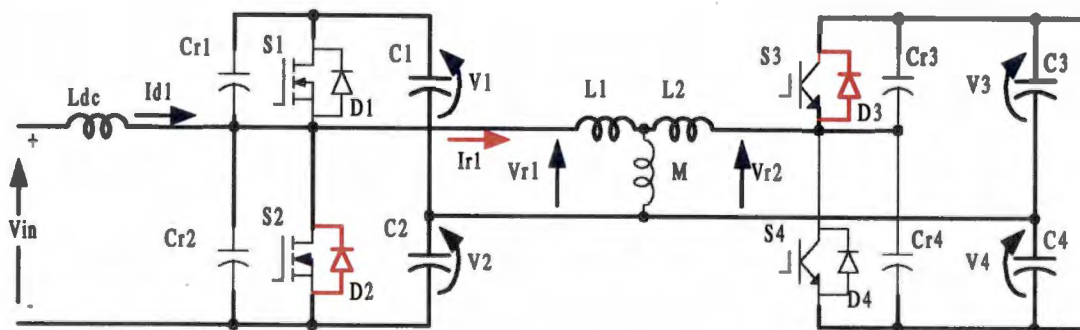
Fig. 3.5 Waveforms and switching timing of boost mode



(a) Step 1: Current path before t_1



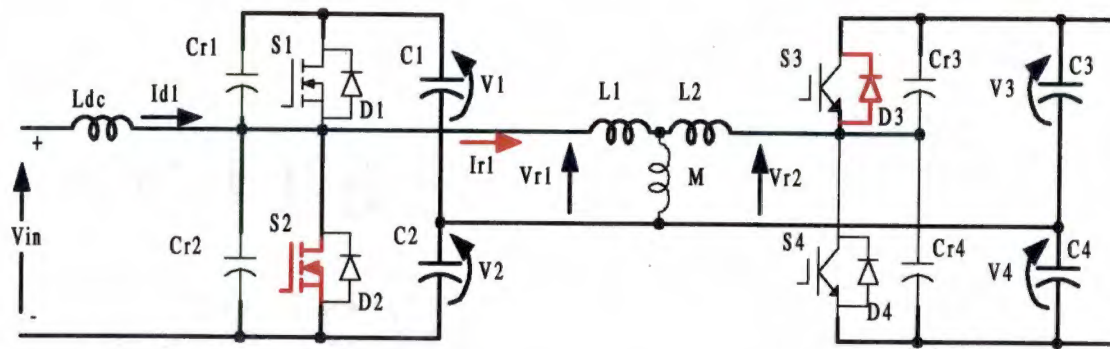
(b) Step 2: Current path between t_1 - t_2



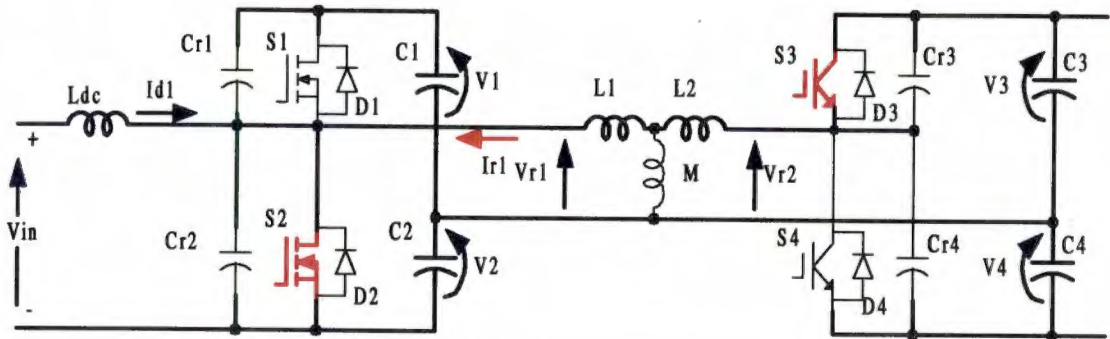
(c) Step 3: Current path between t_2 - t_3

Fig. 3.6 Commutation step diagrams during a switching cycle

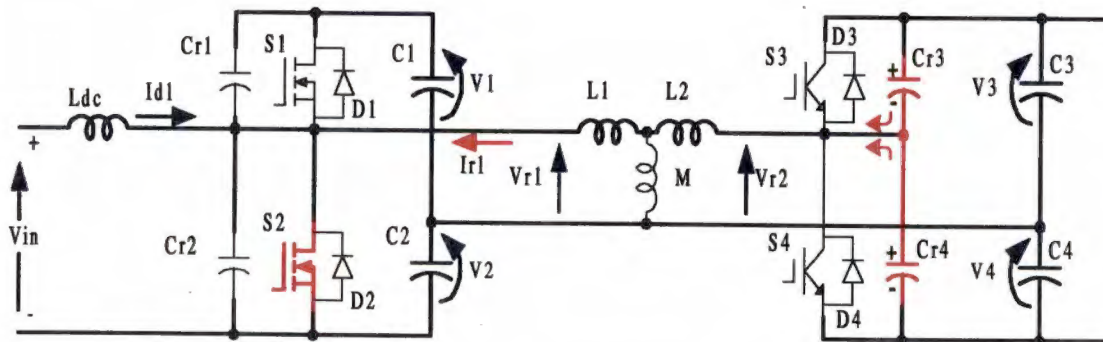
in boost mode



(d) Step 4: Current path between t_3-t_4

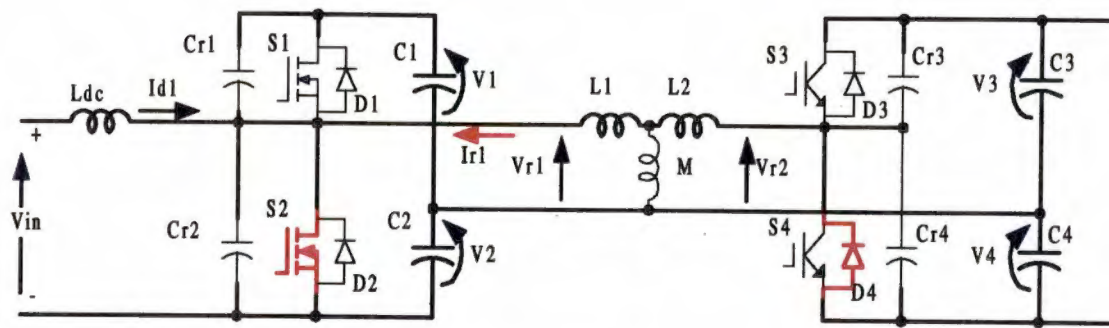


(e) Step 5: Current path between t_4-t_5

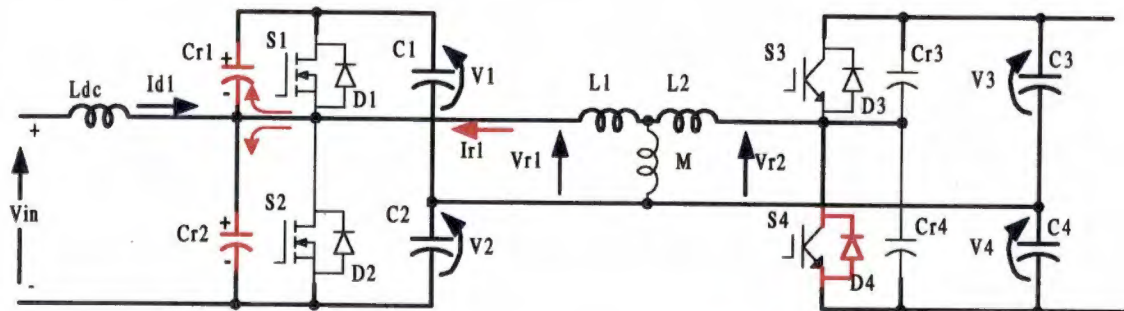


(f) Step 6: Current path between t_5-t_6

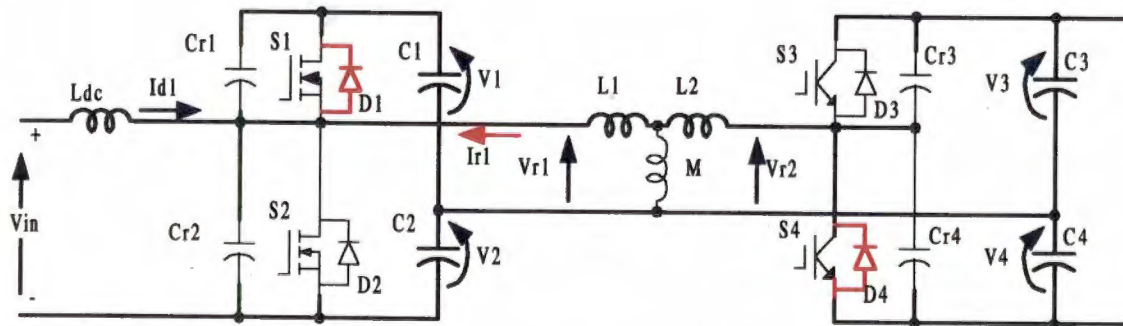
Fig. 3.6 Commutation step diagrams during a switching cycle
in boost mode (continued)



(g) Step 7: Current path between t_6 - t_7



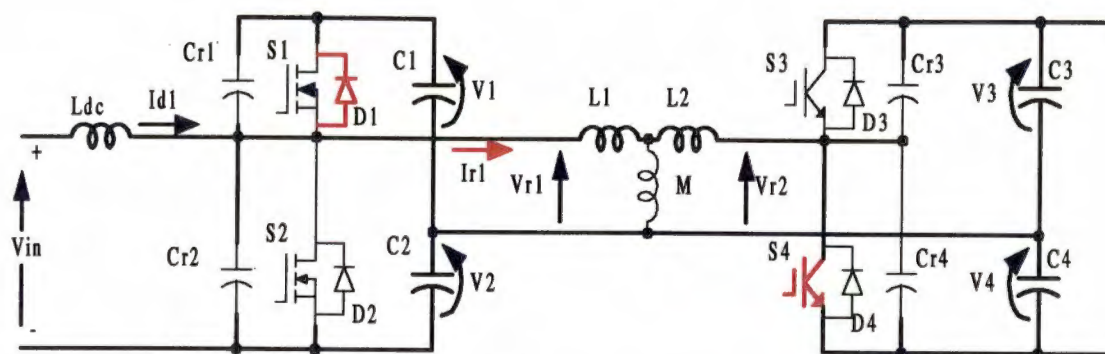
(h) Step 8: Current path between t_7 - t_8



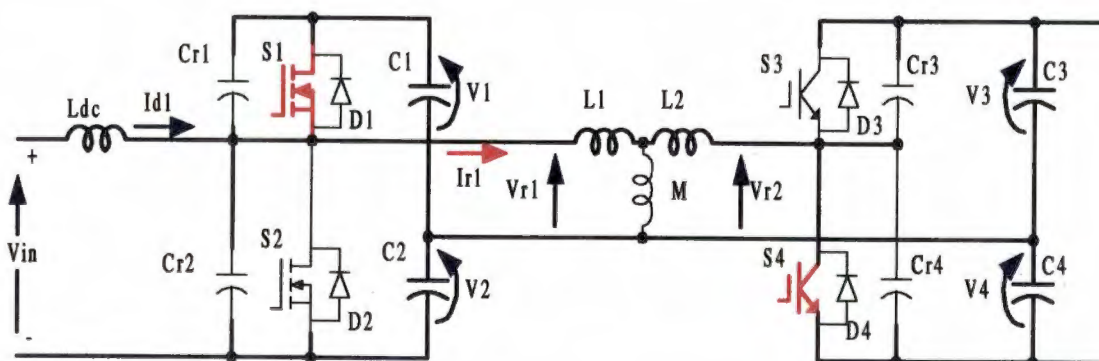
(i) Step 9: Current path between t_8 - t_9

Fig. 3.6 Commutation step diagrams during a switching cycle

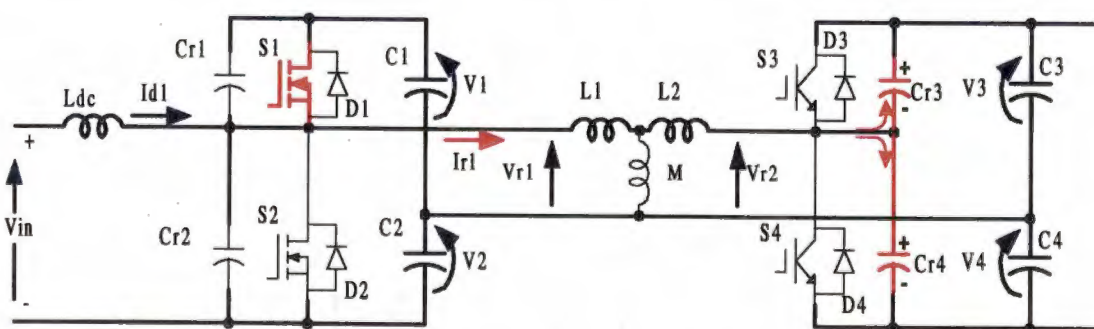
in boost mode (continued)



(j) Step 10: Current path between t_9 - t_{10}



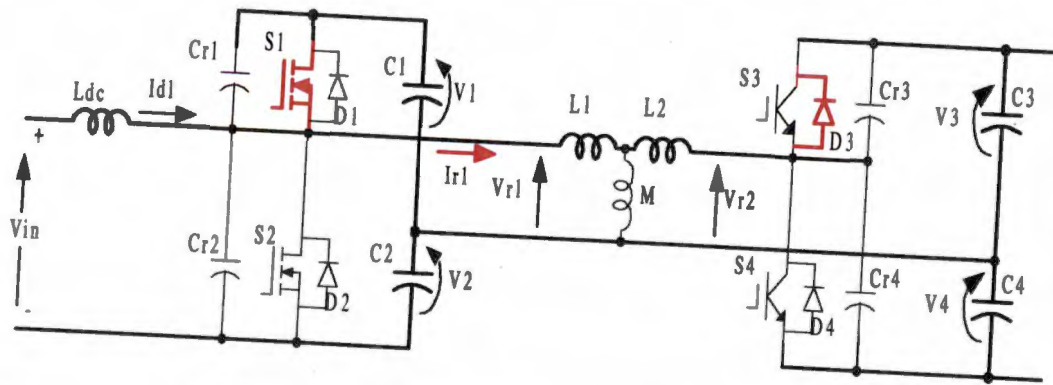
(k) Step 11: Current path between t_{10} - t_{11}



(l) Step 12: Current path between t_{11} - t_{12}

Fig. 3.6 Commutation step diagrams during a switching cycle

in boost mode (continued)



(m) Step 13: Current path after t_{12} (one cycle completes).

Fig. 3.6 Commutation step diagrams during a switching cycle

in boost mode (continued)

Step3 ($t_2 - t_3$): At t_2 , V_{cr2} attempts to overshoot the negative rail, D2 is therefore forward biased. During this period, S2 can be gated on at zero voltage.

Step4 ($t_3 - t_4$): From t_3 , I_{r1} is less than I_{d1} , so S2 begins to transfer current from D2. I_{r1} keeps on decreasing until it is equal to 0 at t_4 . D3 is thereby still conducting until t_4 .

Step5 ($t_4 - t_5$): From t_4 to t_5 , I_{r1} begins to change polarity; therefore, current is commutated from D3 to S3.

Step 6 ($t_5 - t_6$): At t_5 , S3 is gated to turn off. Cr3 and Cr4 begin to be charged and discharged, respectively. The rate of change of the voltage depends on I_{r1} at t_5 .

Step 7 ($t_6 - t_7$): At t_6 , when V_{cr4} attempts to overshoot the negative rail, D4 is forward biased. During this period, S4 can be gated on at any time at zero voltage.

Step 8 ($t_7 - t_8$): At t_7 , S2 is gated off. Cr1, Cr2 and T_r begin to resonant again, making V_{cr1} discharge from $V1 + V2$. V_{r1} therefore increases from $-V2$. The rate of change now is decided primarily by the sum of the magnitude of I_{d1} and I_{r1} .

Step 9 (t_8-t_9): At t_8 , when V_{cr1} attempts to overshoot the negative rail, D1 is forward biased. I_{r1} increases until it equals 0 at t_9 . During this period, S1 can be gated on at zero voltage.

Step 10 (t_9-t_{10}): From t_9 to t_{10} , I_{r1} begins to change its polarity and continue to increase until it equals I_{d1} . The current is commutated from D4 to S4.

Step 11 ($t_{10}-t_{11}$): From t_{10} to t_{11} , I_{r1} begins to exceed I_{d1} . The current is transferred from D1 to S1.

Step 12 ($t_{11}-t_{12}$): At t_{11} , S4 is gated to turn off. Cr3 and Cr4 begin to be charged and discharged again. The charge/discharge rate depends mainly on the magnitude of I_{r1} at t_{11} .

Step 13 ($t_{12}-t_{13}$): At t_{12} , when V_{cr3} attempts to overshoot the positive rail, D3 is forward biased. The circuit returns to the original steady state. During this period, S3 can be gated on any time at zero voltage.

Besides the dual active half-bridge described above, the circuit can also work in a diode rectification mode when S3 and S4 are not switched and the body diodes D3 and D4 conduct the current.

III. 2. 2 Voltage-fed/Buck Mode

When power flows from the high voltage side to the low voltage side, the circuit works in its buck mode. Because the half-bridge topology of the two sides is symmetrical, the operation principles in buck mode are similar to those in boost mode. Fig. 3.7 describes one switching cycle in buck mode. Due to the reversed power

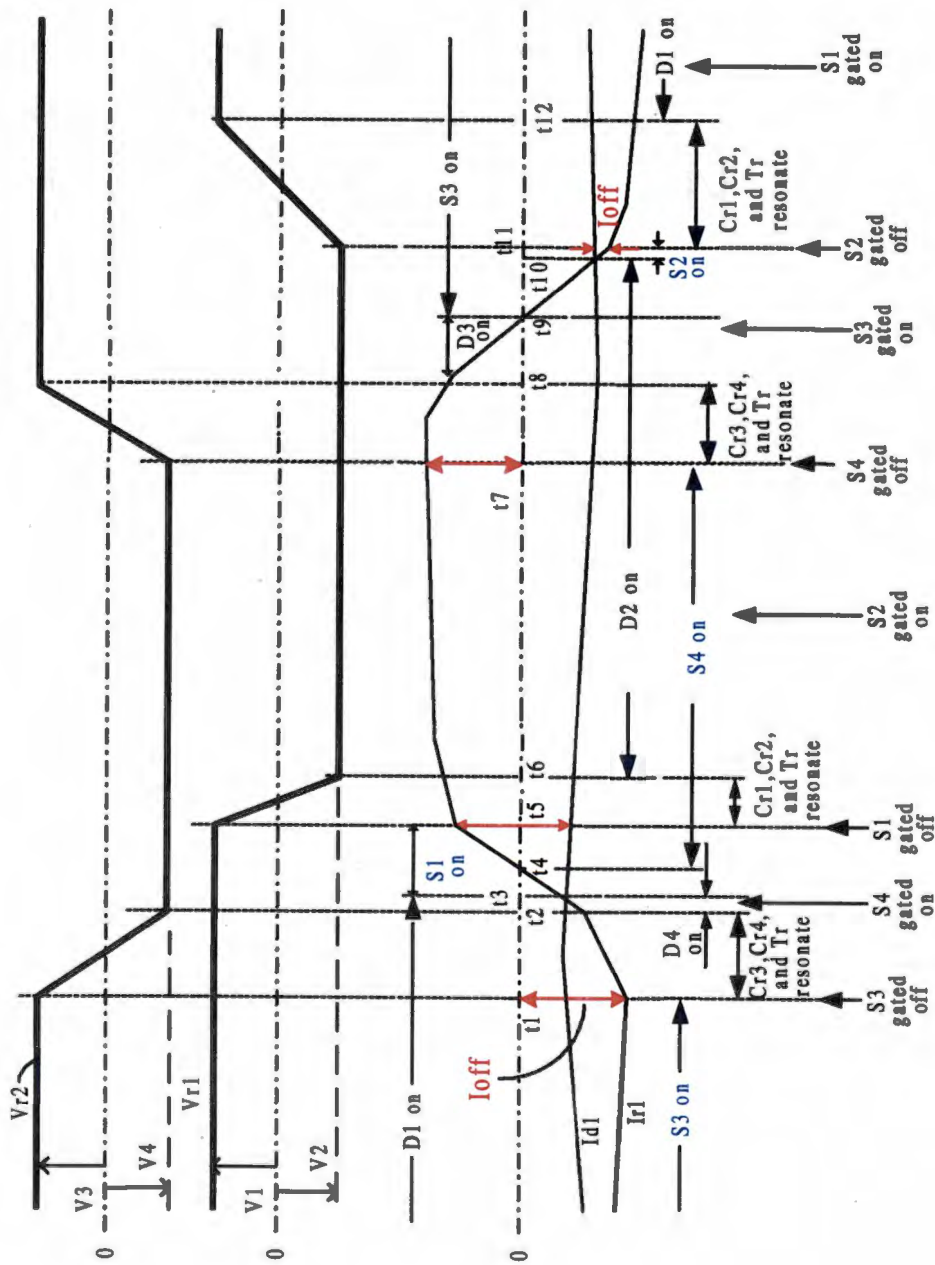


Fig. 3.7 Waveforms and switching timing of buck mode

flow direction, the phase of V_{r2} is leading V_{r1} . The starting point of this commutation cycle is selected at t_1 , which is referred to the instant when S3 is going to be turned off. The buck mode operation can be divided into thirteen steps which are briefly described below. Annotated circuit schematics to aid in the understanding of each step are shown in Fig 3.8.

Step 1: Before t_1 , S3 and D1 are conducting; therefore, $V_{r1}=V_1$, $V_{r2}=V_3$, and the small difference of V_{r1} and V_{r2} makes I_{r1} increase or decrease at a slow rate.

Step 2: At t_1 , S3 is turned off. S4 is also in an off state; thus, Cr3, Cr4 and T_r begin to resonate, making V_{cr4} to fall from V_3+V_4 , V_{r2} therefore also drops from V_3 . The rate of change depends on the magnitude of I_{r1} , which is indicated in Fig. 3.7 at t_1 .

Step 3: At t_2 , when V_{cr4} attempts to overshoot the negative rail, D4 is forward biased, and therefore $V_{r2} = -V_4$. $V_{r1}-V_{r2}$ is large, and the polarity is reversed, so I_{r1} increases at a high rate until it equals to I_{d1} at t_3 . During this period, S4 can be gated on at zero voltage.

Step 4: From t_3 , I_{r1} is bigger than I_{d1} , so S1 begins to transfer current from D1. $V_{r1}-V_{r2}$ remains the same as in *step 3*. I_{r1} keeps increasing until it equals zero at t_4 . D4 remains on until t_4 .

Step 5: From t_4 to t_5 , I_{r1} begins to change polarity; therefore, current is commutated from D4 to S4.

Step 6: At t_5 , S1 is gated to turn off. Cr1 and Cr2 begin to be charged and discharged, respectively. The charge/discharge rate depends mainly on the turn off current at t_5 .

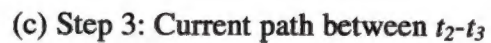
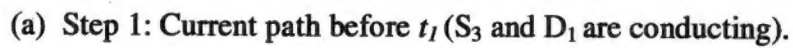
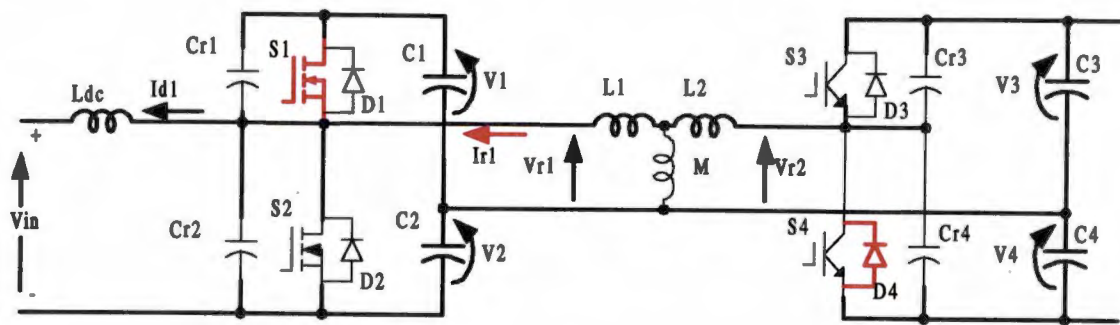
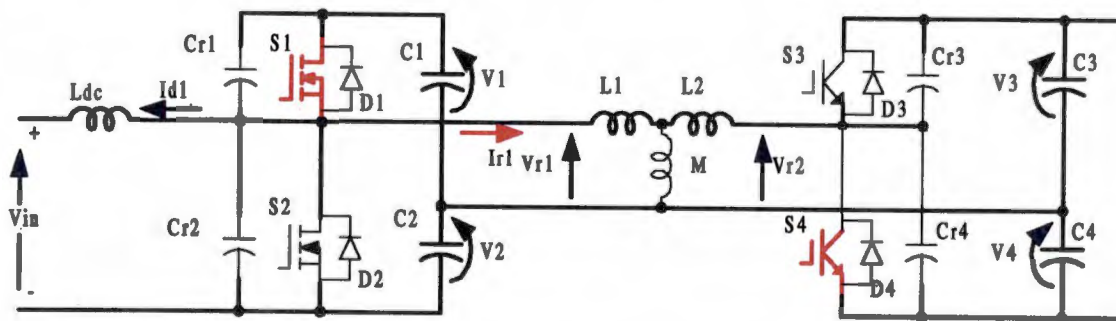


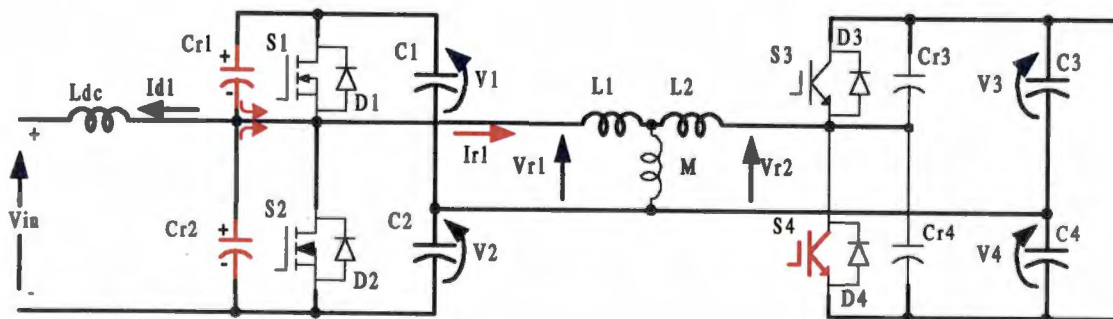
Fig. 3.8 Commutation step diagrams during a switching cycle in buck mode



(d) Step 4: Current path between t_3-t_4



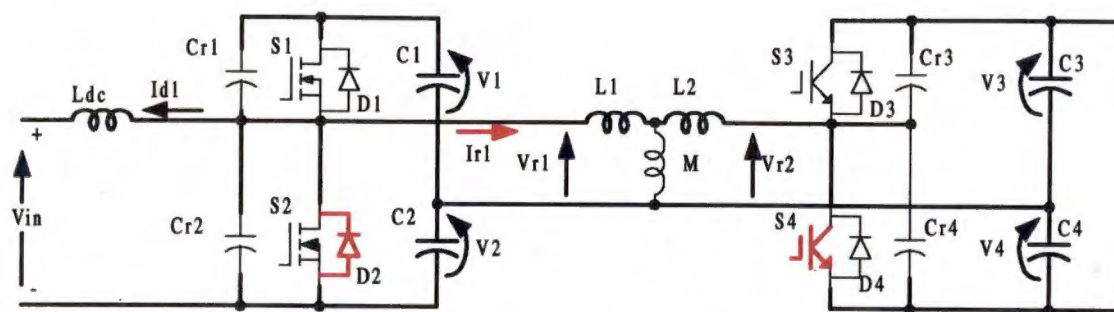
(e) Step 5: Current path between t_4-t_5



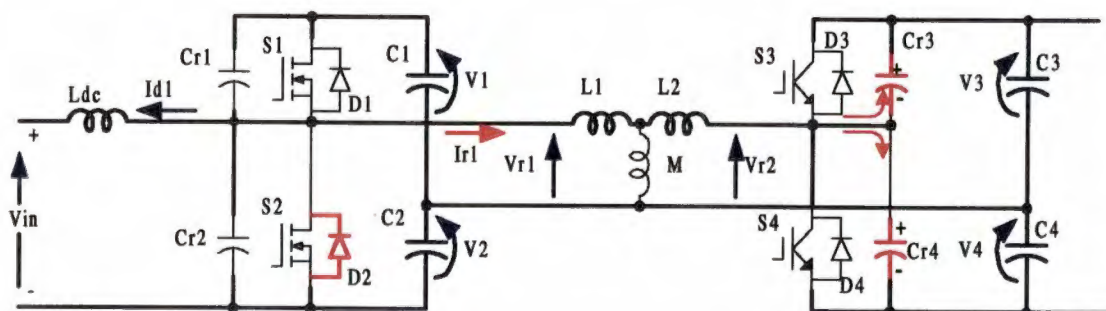
(f) Step 6: Current path between t_5-t_6

Fig. 3.8 Commutation step diagrams during a switching cycle in buck mode

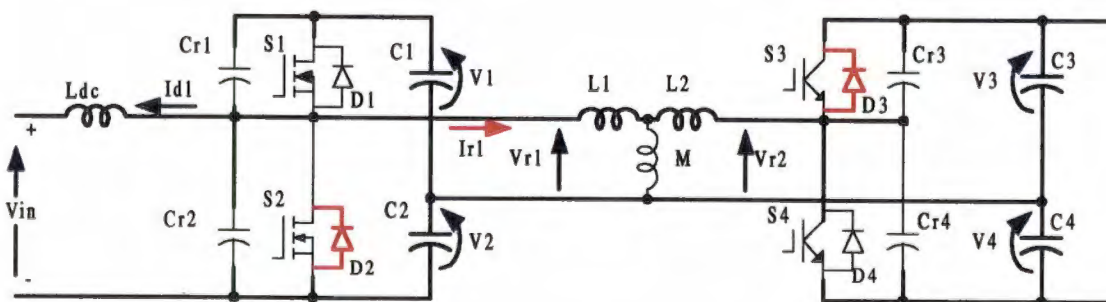
(continued)



(g) Step 7: Current path between t_6 - t_7



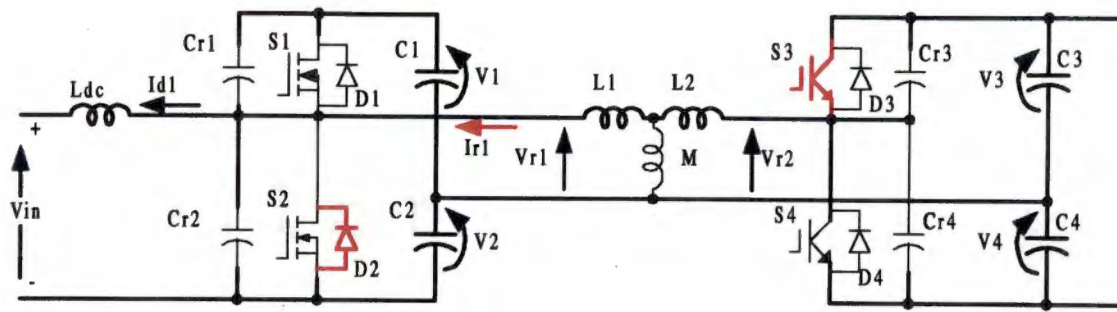
(h) Step 8: Current path between t_7 - t_8



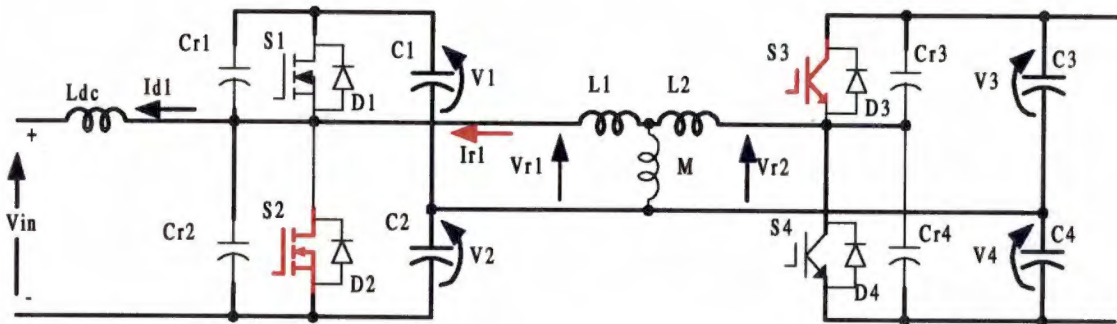
(i) Step 9: Current path between t_8 - t_9

Fig. 3.8 Commutation step diagrams during a switching cycle in buck mode

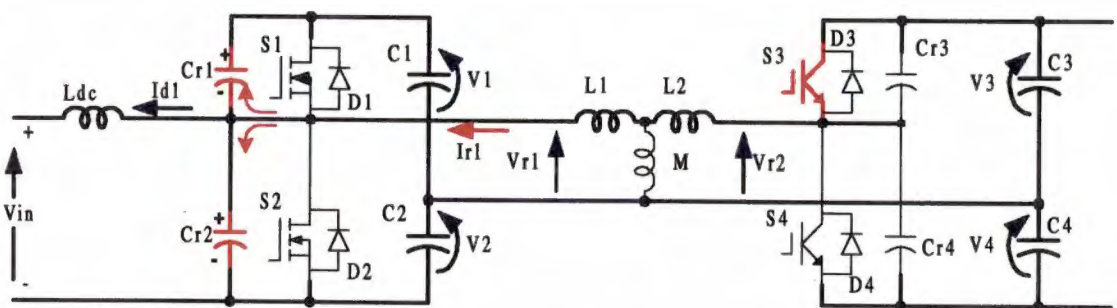
(continued)



(j) Step 10: Current path between t_9 - t_{10}



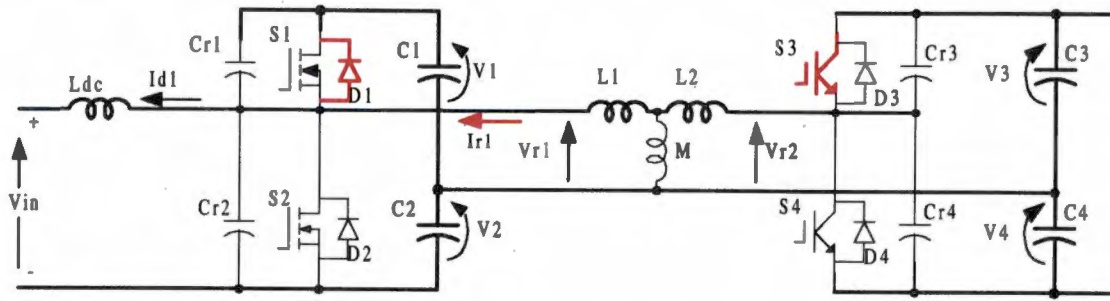
(k) Step 11: Current path between t_{10} - t_{11}



(l) Step 12: Current path between t_{11} - t_{12}

Fig. 3.8 Commutation step diagrams during a switching cycle in buck mode

(continued)



(m) Step 13: Current path after t_{12} (one cycle completes).

Fig. 3.8 Commutation step diagrams during a switching cycle in buck mode

(continued)

Step 7: At t_6 , when V_{cr2} attempts to overshoot the negative rail, D2 is forward biased, and therefore V_{r1} drops to $-V_2$. From t_6 to t_7 , $V_{r2} - V_{r1}$ is small, so I_{r1} increases or decreases at a small rate. During this period, S2 can be gated on at any time at zero voltage.

Step 8: At t_7 , S4 is gated off. Cr3, Cr4 and T_r begin to resonate again, making V_{cr3} discharge from $V_1 + V_2$. V_{r2} therefore also increases from $-V_4$. The rate of change now is determined by the turn off current at t_7 .

Step 9: At t_8 , when V_{cr3} attempts to overshoot negative, D3 is forward biased, and therefore $V_{r2} = V_3$. $V_{r2} - V_{r1} = V_3 + V_2$, and I_{r1} therefore decreases at a high rate until it equals zero at t_9 . During this period, S3 can be gated on at zero voltage.

Step 10: From t_9 to t_{10} , I_{r1} begins to change its polarity and continues to decrease at the same rate until it equals to I_{d1} . The current is transferred from D3 to S3.

Step 11: From t_{10} to t_{11} , I_{r1} becomes more negative than I_{d1} . The current is diverted from D2 to S2.

Step 12: At t_{11} , S2 is gated to turn off. Cr1 and Cr2 begin to be charged and discharged again. The charge/discharge rate depends on the turn off current at t_{11} .

Step 13: At t_{12} , when V_{cr1} attempts to overshoot negative, D1 is forward biased, and Vr1 increases from $-V_2$ to V_1 . Vr1-Vr2 is small, so I_{r1} increases or decreases at a small rate. During this period, S1 can be gated on any time at zero voltage.

III. 2. 3 Simulation Verification

The above operation principles can be verified by the cycle-by-cycle simulation of the circuit. PSIM [2] is selected as the simulation software for this purpose. PSIM is a computer simulation package designed for the analysis and design of power converter circuits and systems. Compared to the other simulation programs, PSIM has the following advantages: (1) Ease of use, (2) fast simulation, (3) built-in power electronics blocks, and (4) it is free of convergence problems. With its unique features in simulation speed, capability of handling power converter circuits of any size, and simulation of control circuits, a wide range of power converter circuits and control techniques can be easily implemented and analyzed by PSIM.

Simulation Results in Boost Mode

In order to be consistent with the above theory, the primary-referred equivalent circuit is applied in the simulation study.

The system parameters are selected as follows:

$V_{in}=12$ V, $f_s=20$ kHz, $D=50\%$, $L_{dc}=25$ μ H, $L_s=0.5625$ μ H, $Cr1=Cr2=Cr3=Cr4=1$ μ F, $C1=C2=C3=C4=5$ mF, $Co=1$ mF, and $R_{load}=0.36$ ohm.

The initial states are:

$I_{d1}(0)=131.4$ A, $I_{r1}(0)=0$ A, $V1(0)=12$ V, $V2(0)=12$ V, $V3(0)=12$ V, $V4(0)=12$ V, $V_o(0)=24$ V, $V_{cr1}(0)=0$ V, $V_{cr2}(0)=24$ V, $V_{cr3}(0)=0$ V, $V_{cr4}(0)=24$ V, $S1(0)=\text{on}$, $S2(0)=\text{off}$, $S3(0)=\text{on}$, and $S4(0)=\text{off}$.

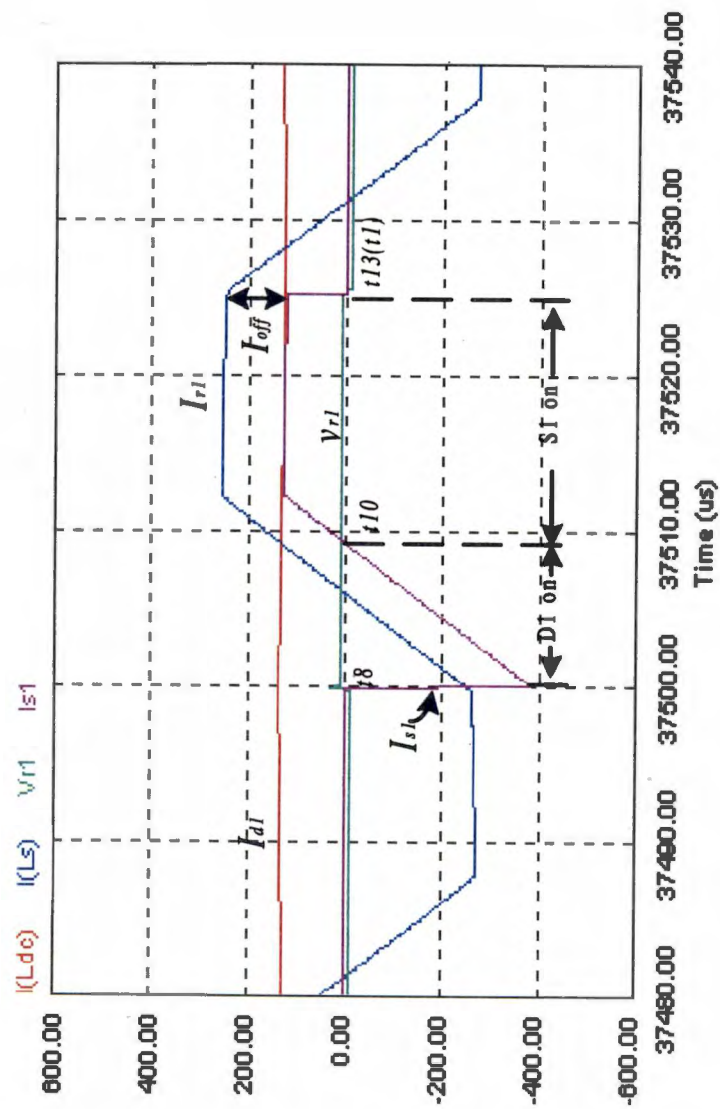
The simulation results for the boost mode are shown in Fig 3.9.

Fig. 3.9(a): From t_8 to t_{10} , $I_{d1} > I_{r1}$, D1 is conducting the current, and I_{s1} is in negative polarity. During this period, S1 can be gated on at zero voltage. From t_{10} to t_{13} , $I_{d1} < I_{r1}$, and the current I_{s1} changes the polarity and is transferred from D1 to S1. At t_{13} (or t_1), S1 is gated off. Cr1, Cr2 and T_r begin to resonate making V_{r1} change from $V1$ to $-V2$. The rate of change of V_{r1} is determined by I_{off} at t_{13} or t_1 . $I_{off}|_{t1} = |I_{d1}| - |I_{r1}|$, so dv/dt is observed to have a minimum at t_1 during one complete switching cycle.

Fig. 3.9(b): From t_{12} to t_4 , $I_{r1} > 0$, D3 is conducting the current. During this time, S3 can be gated on at zero voltage. From t_4 to t_5 , $I_{r1} < 0$, and the current I_{s3} is commutated from D3 to S3. At t_5 , S3 is gated off. Cr3 and Cr4 begin to be charged and discharged. The rate of change of V_{r2} depends on the magnitude of I_{r1} at t_5 .

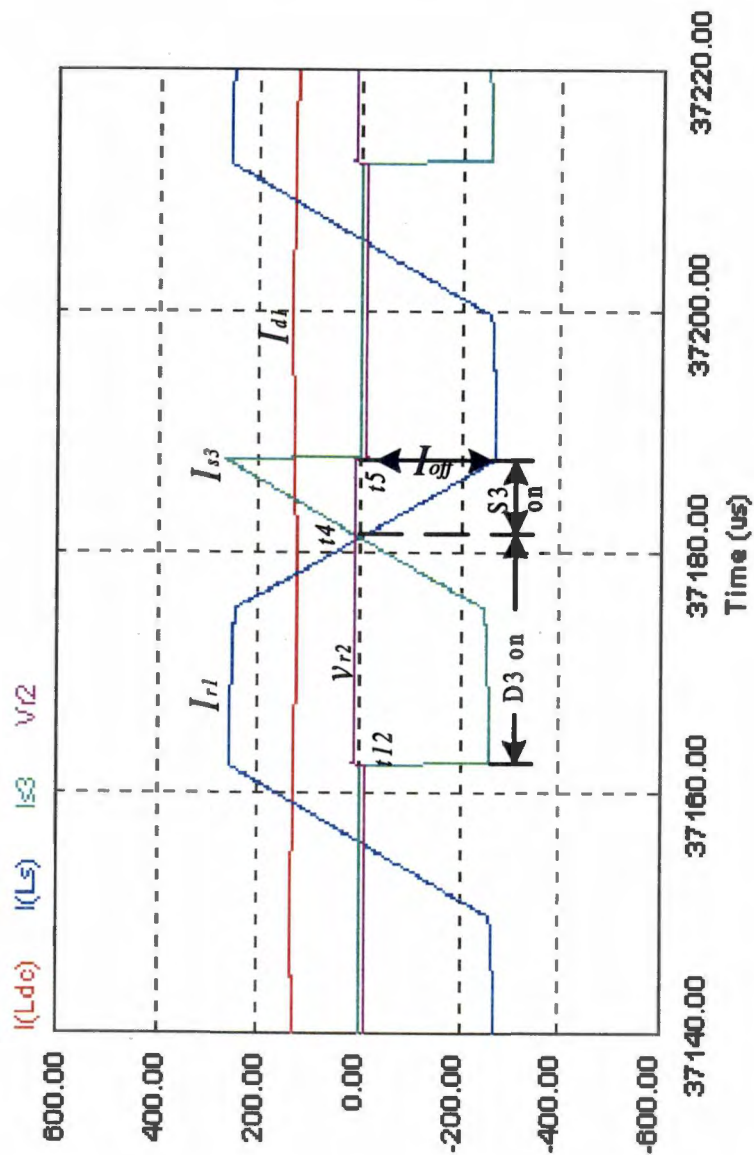
Fig. 3.9(c): From t_2 to t_3 , $I_{r1} > I_{d1}$, and D2 is conducting the current. During this time, S2 can be gated on at zero voltage. From t_3 to t_7 , $I_{d1} > I_{r1}$, and I_{s2} is commutated from D2 to S2. At t_7 , S2 is gated off. The rate of change of V_{r1} depends on I_{off} at t_7 . $I_{off}|_{t7} = |I_{d1}| + |I_{r1}|$, so dv/dt has a maximum at t_7 during one complete switching cycle.

Fig. 3.9(d): From t_6 to t_9 , $I_{r1} < 0$, and D4 is conducting the current. During this period, S4 can be gated on at zero voltage. From t_9 to t_{11} , I_{r1} changes polarity. I_{s4} is commutated from D4 to S4. At t_{11} , S4 is gated off. The rate of change of V_{r2}



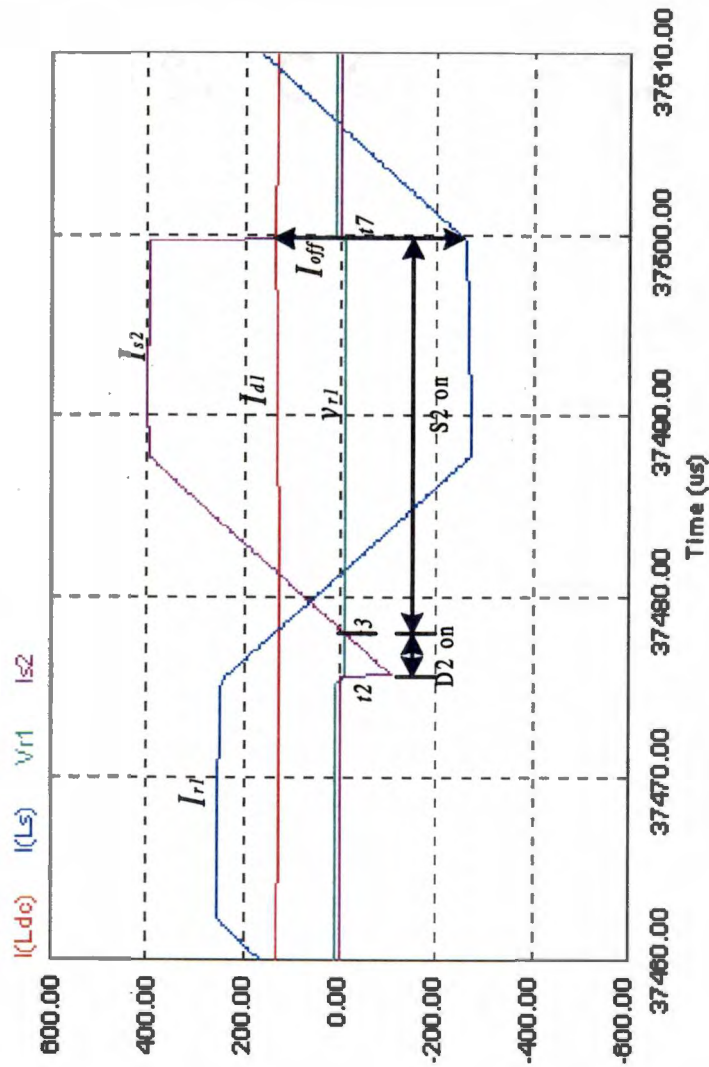
(a) Simulation waveforms of I_{dl} , I_{r1} , V_{r1} and I_{s1} from t_8 to $t_{13}(t_1)$

Fig. 3.9 Detailed simulation results of boost mode



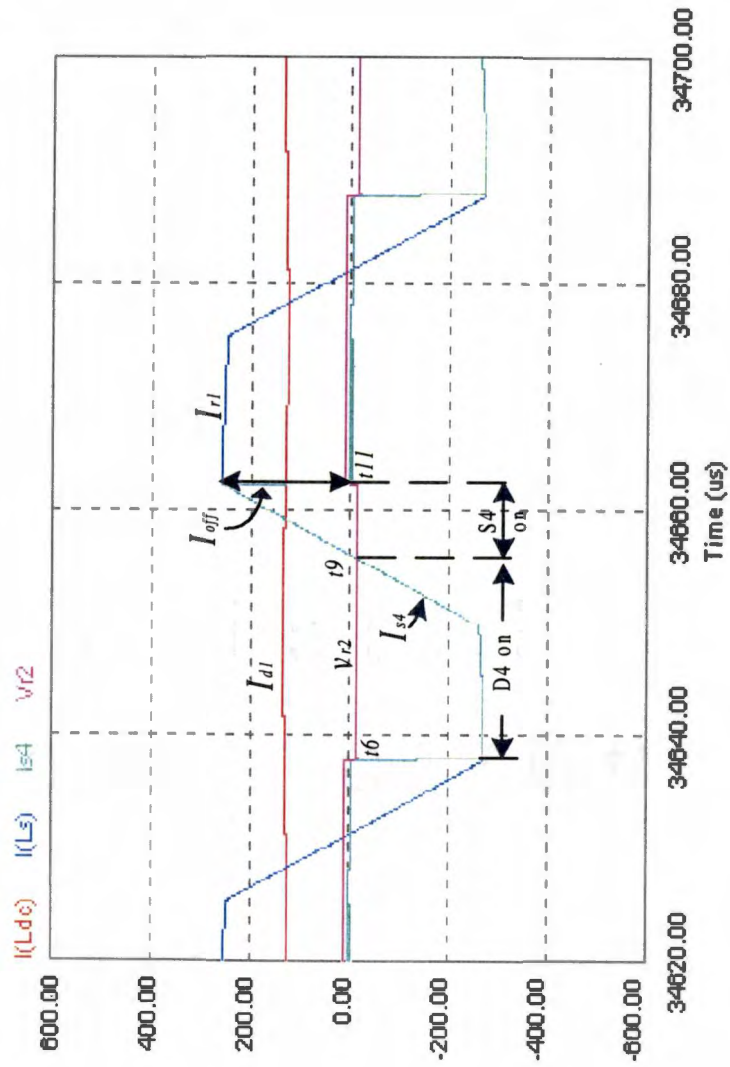
(b) Simulation waveforms of I_{d1} , I_{r1} , V_{r2} and I_{s3} from t_{12} to t_5

Fig. 3.9 Detailed simulation results of boost mode (continued)



(c) Simulation waveforms of I_{d1} , I_{r1} , V_{r1} and I_{s2} from t_2 to t_7

Fig. 3.9 Detailed simulation results of boost mode (continued)



(d) Simulation waveforms of I_{d1} , I_{r1} , $Vr2$ and I_{s4} from t_6 to t_{11}

Fig. 3.9 Detailed simulation results of boost mode (continued)

depends on the magnitude of I_{r1} at t_{11} .

Simulation Results in buck mode

The system parameters of buck mode are selected as follows:

$V_s = 24$ V, $f_s = 20$ kHz, $D = 50\%$, $L_{dc} = 25$ μ H, $L_s = 0.5625$ μ H, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 1$ μ F, $C_1 = C_2 = C_3 = C_4 = 5$ mF, $C_o = 1$ mF, and $R_{load} = 0.09$ ohm

The initial states are:

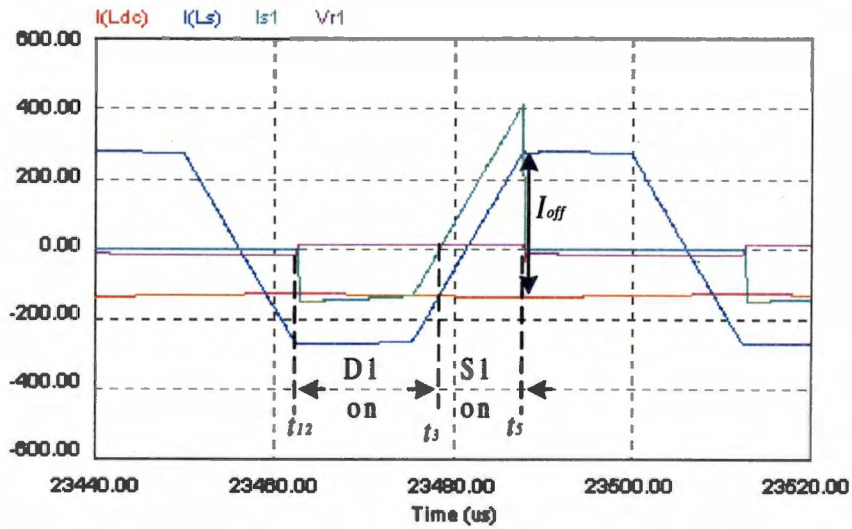
$I_{d1}(0) = -127$ A, $I_{r1}(0) = 0$ A, $V_1(0) = 12$ V, $V_2(0) = 12$ V, $V_3(0) = 12$ V, $V_4(0) = 12$ V, $V_o(0) = 24$ V, $V_{cr1}(0) = 0$ V, $V_{cr2}(0) = 24$ V, $V_{cr3}(0) = 0$ V, $V_{cr4}(0) = 24$ V, $S_1(0) = \text{on}$, $S_2(0) = \text{off}$, $S_3(0) = \text{on}$, and $S_4(0) = \text{off}$

The simulation results are shown in Fig. 3.10 (a)-(d).

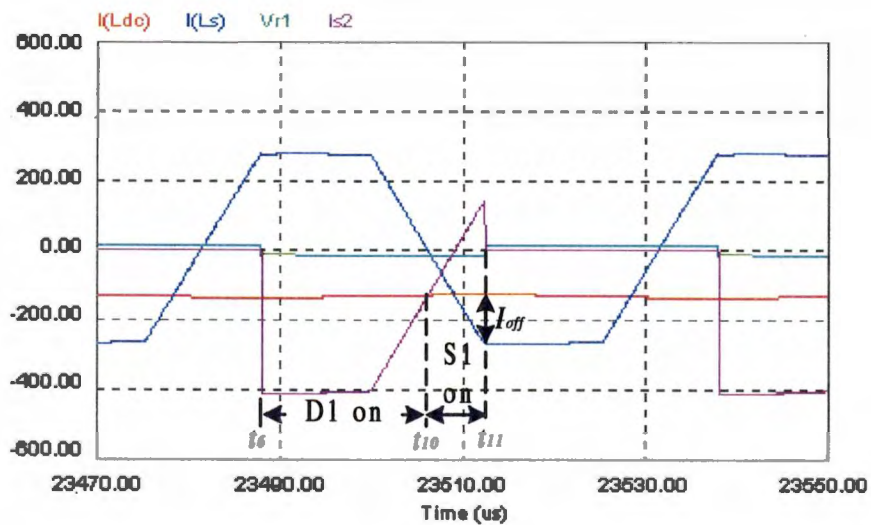
Fig. 3.10(a): From t_{12} to t_3 , $|I_{r1}| > |I_{d1}|$, and D1 is on. S1 can be gated on at zero voltage. From t_3 to t_5 , $|I_{r1}| < |I_{d1}|$, and current is transferred from D1 to S1. At t_5 , S1 is gated off. Cr1, Cr2 and T_r begin to resonate making V_{r1} change from V_1 to $-V_2$. The rate of change of V_{r1} is decided by the magnitude of I_{off} at t_5 . $I_{off} = |I_{d1}| + |I_{r1}|$, so dv/dt is observed to have a maximum at t_5 during one complete switching cycle.

Fig. 3.10(b): From t_6 to t_{10} , D2 is conducting the current. During this time, S2 can be gated on at zero voltage. From t_{10} to t_{11} , $I_{d1} > I_{r1}$, and I_{s2} is commutated from D2 to S2. At t_{11} , S2 is gated off. The rate of change of V_{r1} depends on I_{off} at t_{11} . $I_{off} = |I_{r1}| - |I_{d1}|$, so dv/dt has a minimum at t_{11} during one complete switching cycle.

Fig. 3.10(c): From t_8 to t_9 , $I_{r1} > 0$, and D3 is on. During this time, S3 can be gated on at zero voltage. From t_9 to t_1 , $I_{r1} < 0$, and the current I_{s3} is commutated from

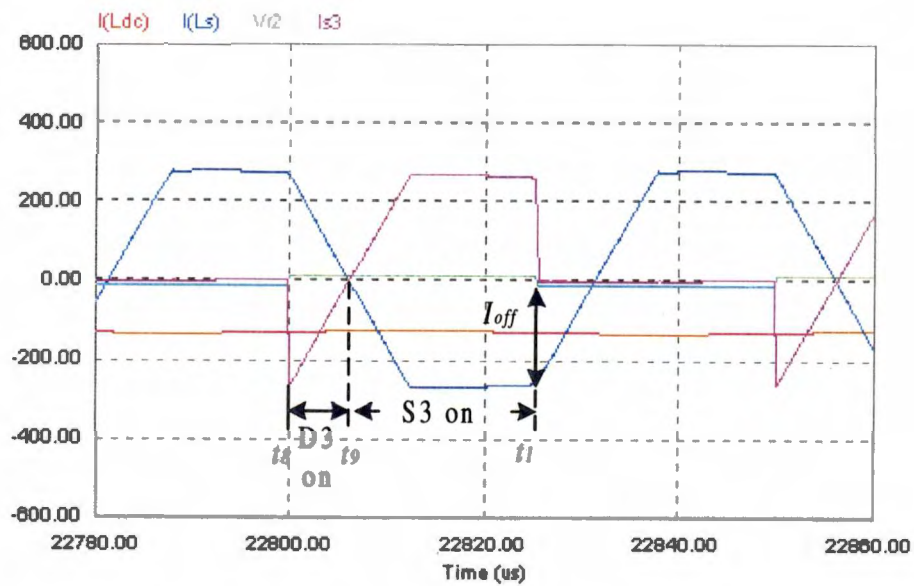


(a) Simulation waveforms of I_{d1} , I_{r1} , V_{r1} and I_{s1} in one switching cycle

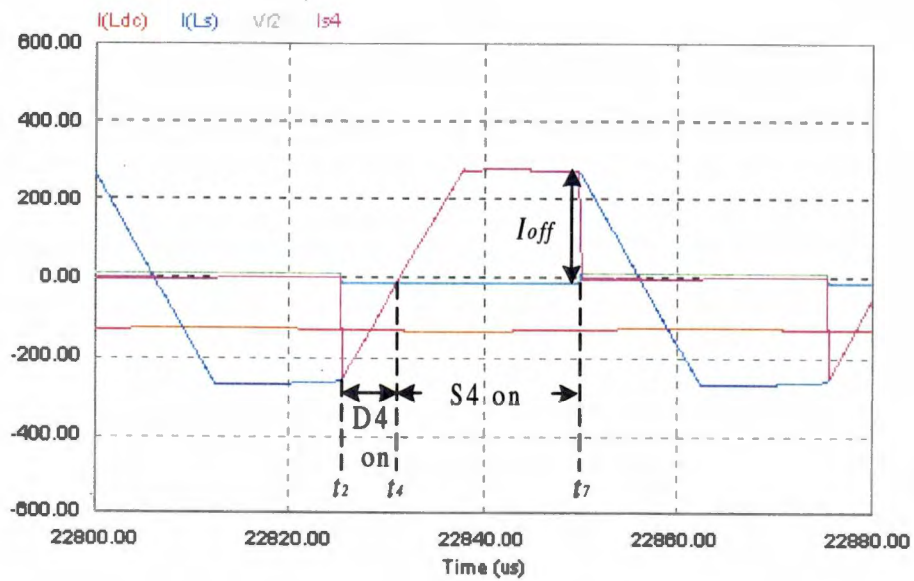


(b) Simulation waveforms of I_{d1} , I_{r1} , V_{r1} and I_{s2} in one switching cycle

Fig. 3.10 Detailed simulation results of buck mode



(c) Simulation waveforms of I_{d1} , I_{r1} , $Vr2$ and I_{s3} in one switching cycle



(d) Simulation waveforms of I_{d1} , I_{r1} , $Vr2$ and I_{s4} in one switching cycle

Fig. 3.10 Detailed simulation results of buck mode (continued)

D3 to S3. At t_1 , S3 is gated off. Cr3 and Cr4 begin to be charged and discharged respectively. The rate of change of V_{r2} depends on the magnitude of I_{r1} at t_1 .

Fig. 3.10(d): From t_2 to t_4 , $I_{r1} < 0$, and D4 is conducting the current. During this period, S4 can be gated on at zero voltage. From t_4 to t_7 , I_{r1} changes the polarity. I_{s4} is commutated from D4 to S4. At t_7 , S4 is gated off. The rate of change of V_{r2} depends on the magnitude of I_{r1} at t_7 .

The above simulation results of Fig. 3.9 and Fig. 3.10 agree well with the principles of operation described in Fig. 3.5 and Fig. 3.7, respectively. There is a consistency in the shape of V_{r1} and V_{r2} and the current waveforms of I_{r1} and I_{d1} . In addition, the shape of dv/dt and the commutation process, i.e., the switching sequence of devices and diodes in Fig. 3.9 and Fig. 3.10, are the same as those of Fig. 3.5 and Fig. 3.7.

III. 3 Steady State Analysis and Design Guidelines

The steady state performance of the converter is analyzed to derive design guidelines and enable selection of the components. This analysis includes the commutation analysis in section III. 3.1 and determination of output characteristics in section III. 3.2. Design equations corresponding to worst case operating conditions are given in section III. 3.3. The design curves that allow the selection of components are presented in section III. 3.4.

III. 3. 1 Commutation analysis

The purpose of commutation analysis is to derive the soft-switching conditions of both modes.

Commutation in the proposed circuit is similar to the diode-to-switch commutation mode of the ARCP inverter, i.e., turn-off of the main conducting device diverts the current to the corresponding snubber capacitors to charge one and discharge another, resulting in a zero voltage turn-off. The zero voltage turn-on is achieved by gating on the in-coming device while the anti-parallel diode is conducting. However, unlike ARCP inverter, the proposed circuit does not require an auxiliary circuit to achieve soft-switching.

From Fig. 3.5, it is clear that the conditions of soft switching in boost mode depend on the magnitude of I_{r1} and I_{d1} at t_1 , t_5 , t_7 and t_{11} , respectively. This is summarized in equation (3-1). Similarly, the soft-switching conditions in buck mode can be derived from Fig. 3.7 and expressed in equation (3-2).

$$\left\{ \begin{array}{l} I_{r1}(t_1) > I_{d1}(t_1) \\ I_{r1}(t_5) < 0 \\ I_{r1}(t_7) > I_{d1}(t_7) \\ I_{r1}(t_{11}) > 0 \end{array} \right. \quad (3-1) \quad \text{and} \quad \left\{ \begin{array}{l} I_{r1}(t_1) < 0 \\ I_{r1}(t_5) > I_{d1}(t_5) \\ I_{r1}(t_7) > 0 \\ I_{r1}(t_{11}) < I_{d1}(t_{11}) \end{array} \right. \quad (3-2)$$

For boost mode, it is observed that rate of change of the voltage of S1 and S2 at t_1 is different from that at t_7 . This is because the turn-off currents are different at their switching instants. Similarly, devices S3 and S4 have different voltage change rates at t_5 and t_{11} . Comparing these four voltage slopes, dv/dt at t_1 and dv/dt at t_7

represent the minimum and maximum, respectively, because the turn-off current is minimum at t_1 and maximum at t_7 . As a result, the allowable minimum and maximum dv/dt should be designed according to application requirements. The rate of change of the voltage in buck mode can be analogously inferred.

III. 3. 2 Output characteristics

The analysis of output characteristics is based on the primary-referred equivalent circuit in Fig. 3.11 and the idealized waveforms in Fig. 3.12.

The phase shift between the two voltage waveforms of Fig. 3.12 is ϕ_1 . The transformer current I_{r1} is a function of $\theta = \omega t$, where ω is the switching frequency. There are four operation modes in one switching period.

In mode I,

$$I_{r1}(\theta) = \frac{V1 + V4}{\omega L_s} \theta + I_{r1}(0) \quad (3-3)$$

Where V1 and V4 are voltages across c_1 and c_4 , $I_{r1}(0)$ is the initial current of I_{r1} at $\theta=0$. Mode I ends at $\theta=\phi_1$.

In mode II,

$$I_{r1}(\theta) = \frac{V1 - V3}{\omega L_s} (\theta - \phi_1) + I_{r1}(\phi_1) \quad (3-4)$$

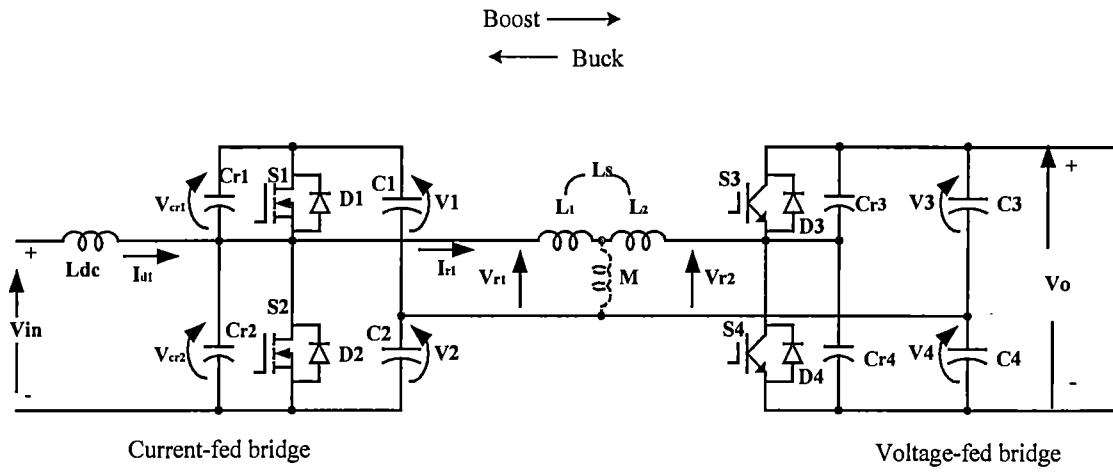


Fig. 3.11 Primary referred equivalent circuits

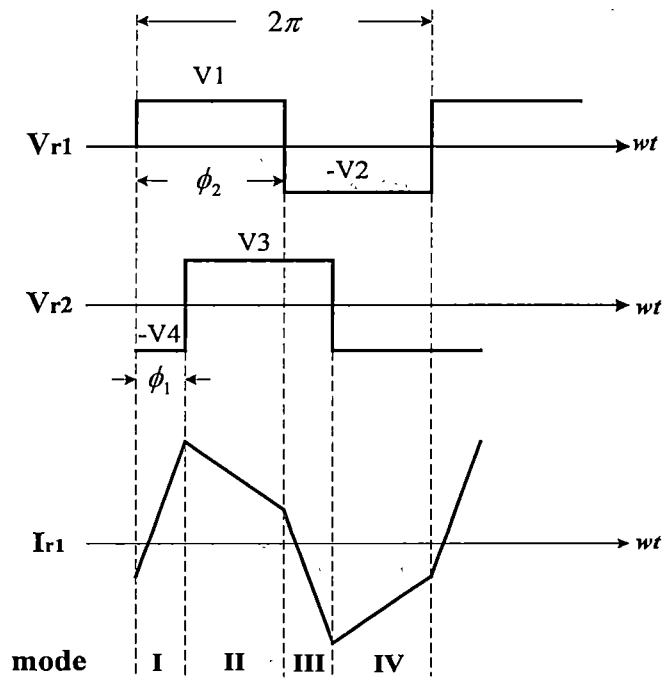


Fig. 3.12 Idealized voltage and current waveforms of transformer

Similarly, the current in mode III can be found to be

$$I_{r1}(\theta) = \frac{-V_2 - V_3}{\omega L_s} (\theta - \phi_2) + I_{r1}(\phi_2) \quad (3-5)$$

and the current in mode IV is:

$$I_{r1}(\theta) = \frac{-V_2 + V_4}{\omega L_s} (\theta - \phi_1 - \phi_2) + I_{r1}(\phi_1 + \phi_2) \quad (3-6)$$

From the representation of $I_{r1}(\theta)$, the transfer power can be found to be:

$$P_o = \frac{\int_0^{T_s} I_{r1} \cdot V_{r1}}{T_s} = \frac{\phi_1 \frac{1}{D} \left[4\pi(1-D) - \frac{1}{D}\phi_1 \right]}{4\pi\omega L_s} \cdot V_{in}^2 \quad (3-7)$$

where T_s is the period of the switching frequency and $D = \phi_2/2\pi$. The output power (output voltage) can be regulated by phase shift angle ϕ_1 , duty cycle D and switching frequency ω .

If $D = 50\%$ is assumed and the switching frequency is set at 20 kHz, then the output power equation can be simplified further to

$$P_o = \frac{V_{in}^2}{\omega L_s} \frac{\phi_1(\pi - \phi_1)}{\pi} \quad (3-8)$$

Fig 3.13 illustrates the variations of nomalized P_o as a function of ϕ_1 when

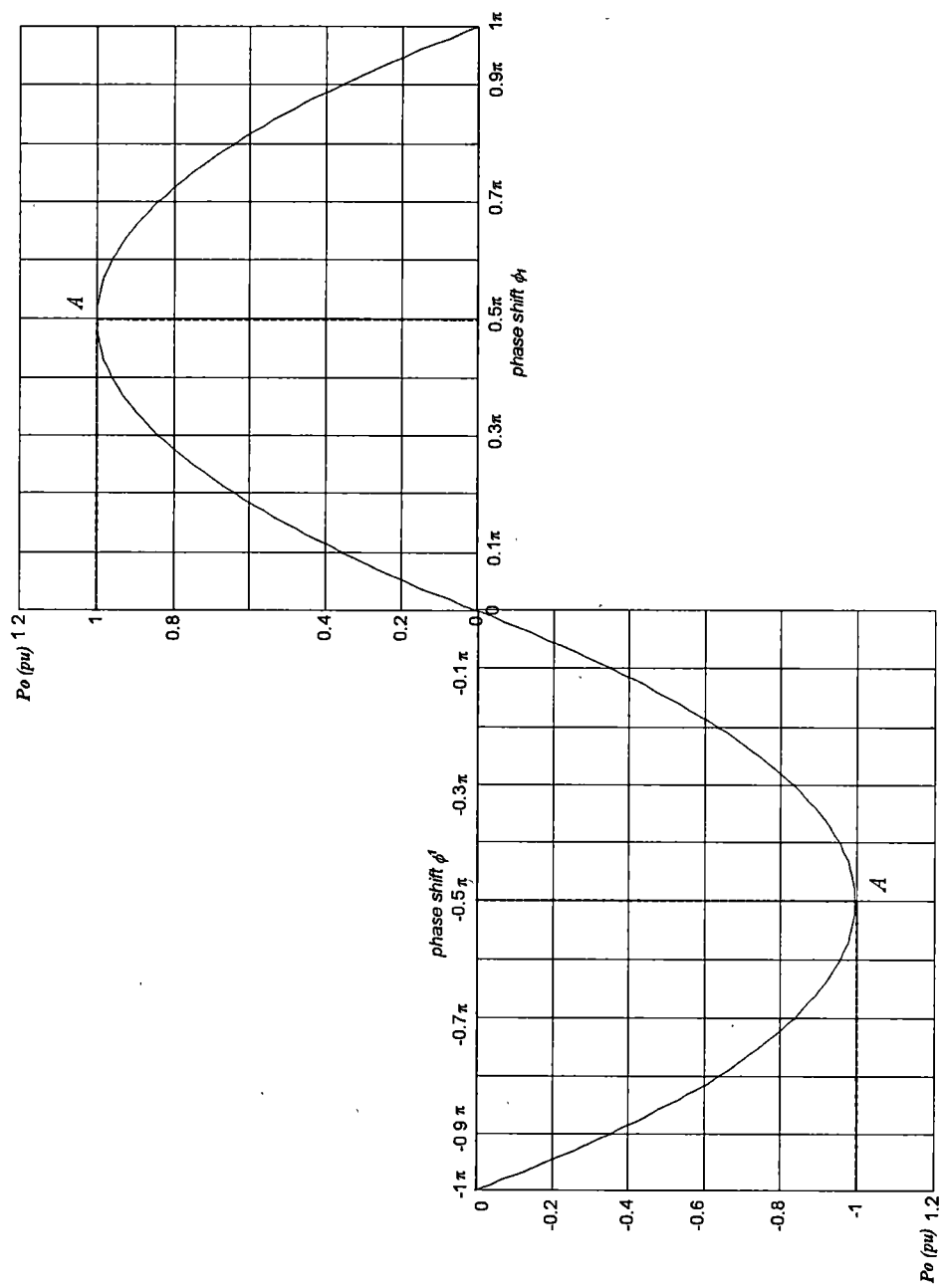


Fig. 3.13 The relationship of P_o and ϕ

duty cycle and switching frequency are constants. It is seen that maximum power transfer occurs at point A when $\phi_l=90^\circ$. Making the phase shift angle negative can reverse the power flow. The negative power flow control is symmetrical to the positive power flow control.

III. 3. 3 Design equations

The design equations are derived based on equation (3-8) and Fig. 3.14. According to equation (3-8), when duty cycle and switching frequency are fixed, the output power is related to phase shift angle and leakage inductance of transformer.

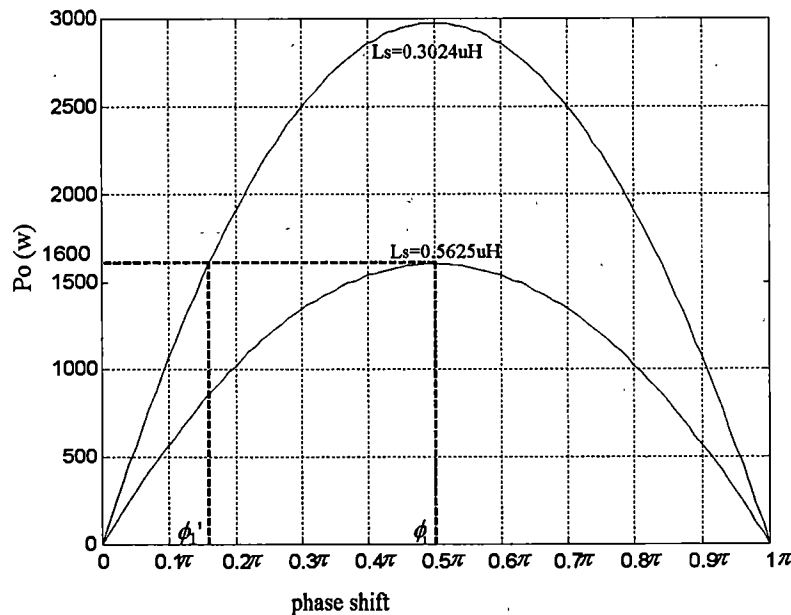


Fig. 3.14 The output power, ϕ_l and leakage inductance L_s

Fig. 3.14 illustrates the output power curves of $L_s = 0.5625 \mu\text{H}$ and $L_s = 0.3024 \mu\text{H}$. It is interesting to notice that if the leakage inductance is selected differently, the phase shift angle of the same output power is changed. The smaller leakage inductance results in the smaller the phase shift angle. Therefore, the leakage inductance of the transformer can be designed according to the expected phase shift angle at the required power rating.

Suppose the maximum output power is P_o , the input dc voltage is V_{in} , the switching frequency is ω , the expected phase shift angle at P_o is ϕ_1 , L_s can be calculated as follows.

$$L_s = \frac{V_{in}^2 \cdot \phi_1 \cdot (\pi - \phi_1)}{P_o \cdot \omega \pi} \quad (3-9)$$

Referred to Fig. 3.12, the initial states $I_{r1}(0), I_{r1}(\phi_1), I_{r1}(\phi_2), I_{r1}(\phi_2 + \phi_1)$ of current I_{r1} during one complete switching cycle can be derived based on the boundary conditions:

$$\begin{aligned} I_{r1}(0) &= -I_{r1}(\phi_2) \\ I_{r1}(\phi_1) &= -I_{r1}(\phi_2 + \phi_1) \end{aligned} \quad (3-10)$$

When $D = 50\%$, $\phi_2 = \pi$. The initial conditions of I_{r1} are calculated in equations (3-11).

$$\begin{cases} I_{r1}(0) = \frac{V3-V1}{2\omega L_S}(\pi - \phi_1) - \frac{V1+V4}{2\omega L_S}\phi_1 \\ I_{r1}(\phi_1) = \frac{V1+V4}{2\omega L_S}\phi_1 + \frac{V3-V1}{2\omega L_S}(\pi - \phi_1) \\ I_{r1}(\pi) = -I_{r1}(0) \\ I_{r1}(\pi + \phi_1) = -I_{r1}(\phi_1) \end{cases} \quad (3-11)$$

The average current I_{d1} provided by the power supply can be found to be:

$$I_{d1} = \frac{P_o}{V_{in}} \quad (3-12)$$

The device rating of LV side can be calculated as:

$$\begin{aligned} I_{peak} &= I_{d1} - I_{r1}(0) \\ V_{peak} &= 2V_{in} \end{aligned} \quad (3-13)$$

Referred to Fig. 3.7 and Fig. 3.12, the maximum and minimum voltage change rates happened at $\theta=0$ and $\theta=\pi$, respectively. The corresponding turn-off currents are calculated as: $I_{off}|_{\max\theta=0} = |I_{r1}(0)| + |I_{d1}|$ and $I_{off}|_{\min\theta=\pi} = |I_{r1}(\pi)| - |I_{d1}|$. Assuming snubber capacitors are selected as 1 μF , $I_{off} = Cr1 \cdot dv/dt$, the range of dv/dt is derived as:

$$I_{off}|_{\min} \leq \frac{dv}{dt} \leq I_{off}|_{\max} \quad (3-14)$$

If ΔI of I_{d1} is selected as 12A, then L_{dc} is designed to be

$$L_{dc} = \frac{V_{in} \cdot \Delta t}{\Delta I} \quad (3-15)$$

Finally, the soft switching condition will be verified in equation (3-16).

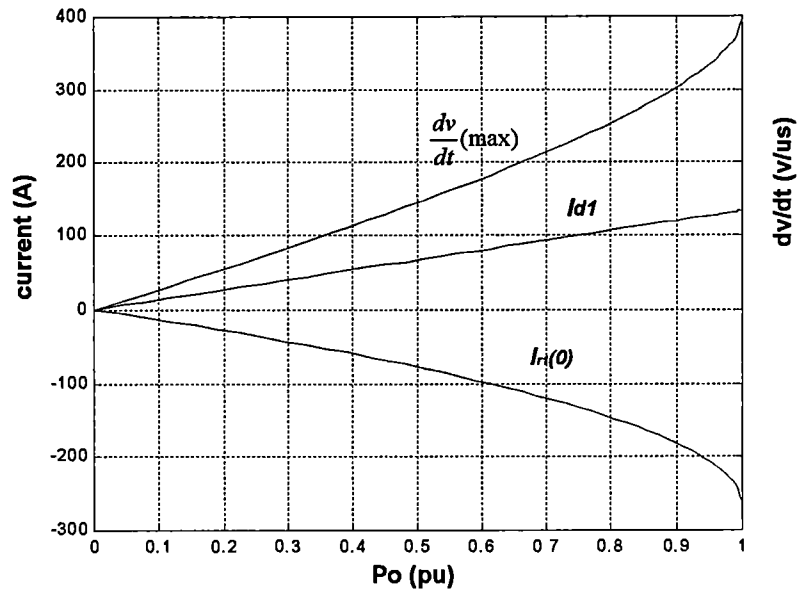
$$\text{boost} \begin{cases} I_{r1}(0) - I_{d1} < 0 \\ I_{r1}(\phi_1) > 0 \\ I_{r1}(\pi) - I_{d1} > 0 \\ I_{r1}(\pi + \phi_1) < 0 \end{cases} \quad \text{and} \quad \text{buck} \begin{cases} I_{r1}(0) > 0 \\ I_{d1} > I_{r1}(\phi_1) \\ I_{r1}(\pi) < 0 \\ I_{r1}(\pi + \phi_1) > I_{d1} \end{cases} \quad (3-16)$$

III. 3. 4 Characteristics curves

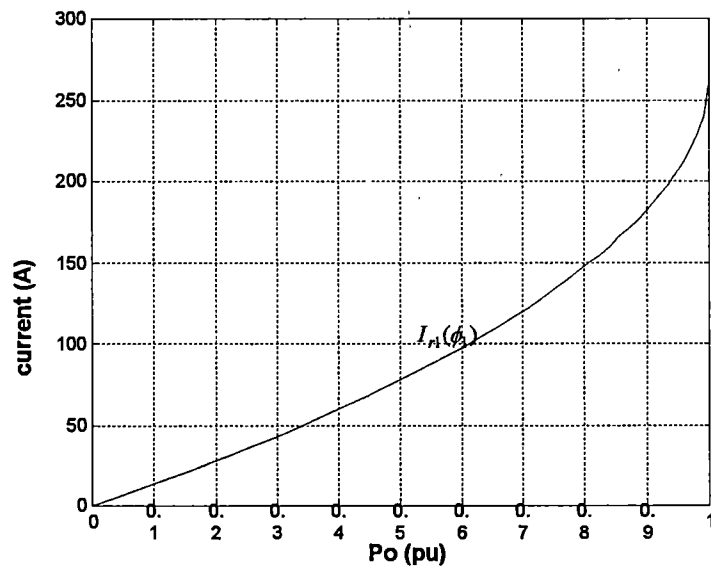
The characteristic curves are derived based on the design equations. Fig. 3.15 to Fig. 3.17 describe the system behavior when transformer leakage inductance is selected as $0.5625\mu\text{H}$.

Figs. 3.15 (a)-(d) plots the input current, transformer current, $dv/dt(\text{max})$ and $dv/dt(\text{min})$ over the full output power range. The purpose of this figure is to show that the soft-switching condition is satisfied during the whole operating range. According to equation (3-16), soft switching is maintained at any output power in the boost mode. Soft switching of the buck mode can be similarly inferred.

Fig. 3.16 shows the current stress of the main switches of the low voltage side and the high voltage side against output power. The current stress of high voltage side is calculated based on the primary-preferred circuit. The real value can be derived by dividing the current by the transformer ratio. Fig. 3.17 plots the current stress as a function of phase shift ϕ_l instead of output power.

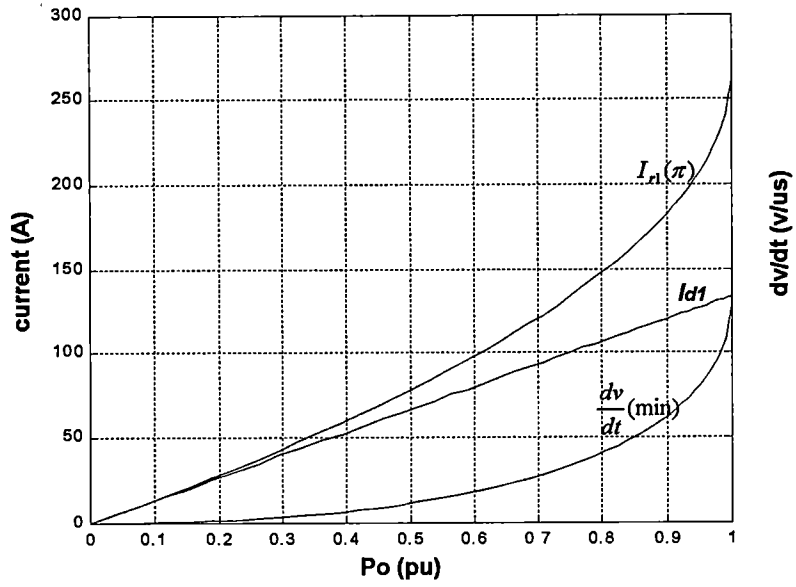


(a) I_{d1} , $I_{r1}(0)$, $\frac{dv}{dt}(\max)$ versus output power

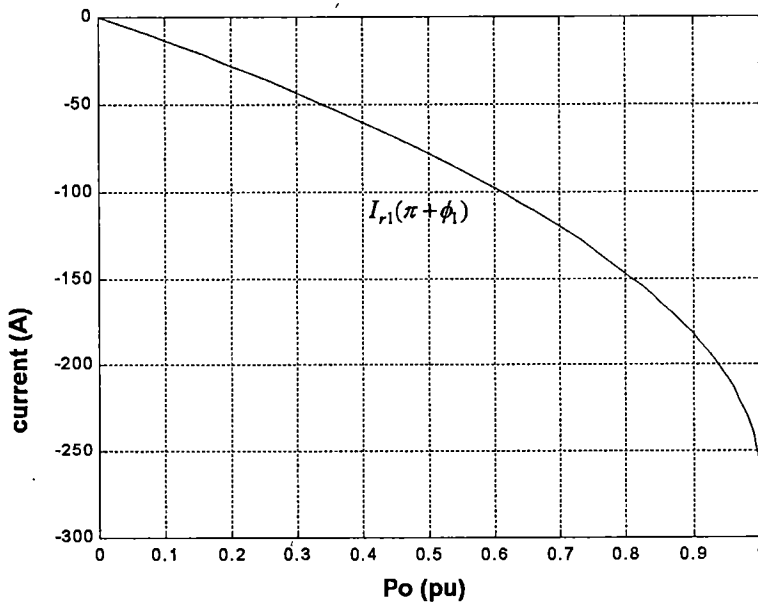


(b) $I_{r1}(\phi_1)$ versus output power

Fig. 3.15 The soft-switching conditions versus output power of $0.5624\mu\text{H}$



(c) I_{d1} , $I_{rl}(\phi_1)$, $\frac{dv}{dt}(\min)$ versus output power



(d) $I_{rl}(\pi + \phi_1)$ versus output power

Fig. 3.15 The soft-switching conditions versus output power of 0.5624 μ H (continued)

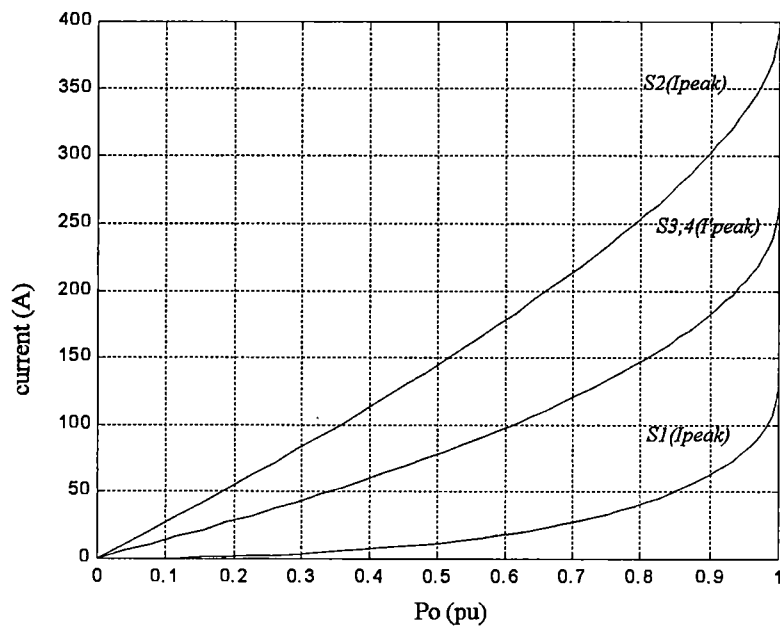


Fig. 3.16 The current stresses of devices versus output power

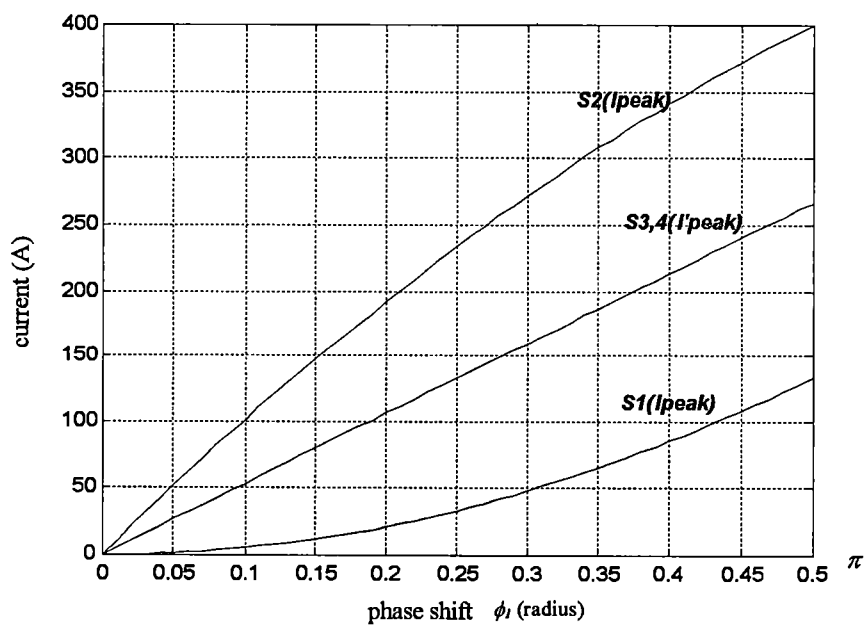


Fig. 3.17. The current stresses of devices versus phase shift ϕ_1

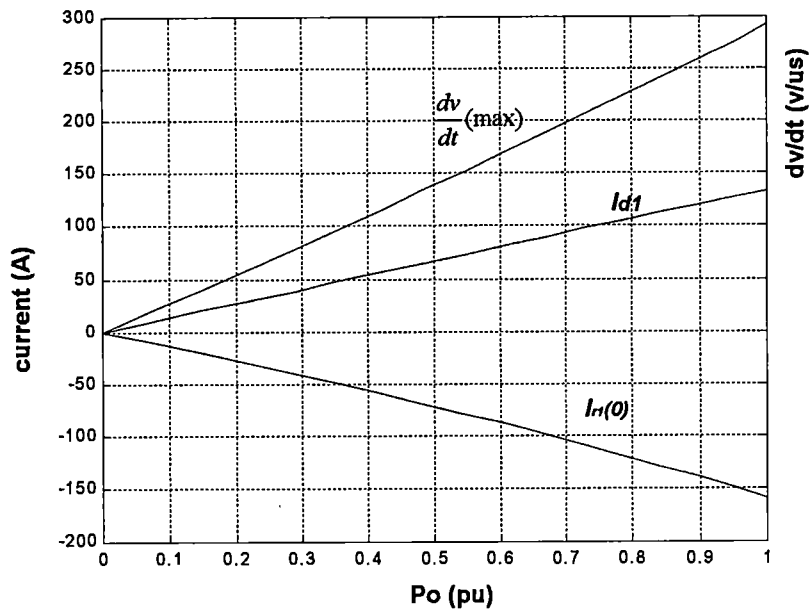
An interesting feature can be brought to light by examining Fig. 3.17, which shows that the current stresses of the devices are proportional to the phase shift angle. As a result, if the phase shift is decreased for the same output power, the current stress becomes less. This is important to improve the system efficiency because the conduction loss will become the main loss for soft-switching converters.

In order to compare the system behavior for a different leakage inductance, Fig. 3.18 to Fig. 3.20 are drawn when L_s is selected as $0.3024 \mu\text{H}$. The soft-switching operations of $0.3024 \mu\text{H}$ are demonstrated in Fig. 3.18. It is seen that the soft-switching conditions are also achieved during the whole operating range. The current stress of the main switches is shown in Fig. 3.19. It is very clear that they are decreased compared to Fig. 3.16. This can be explained in Fig. 3.20. With phase shift decreasing, the current stress becomes less.

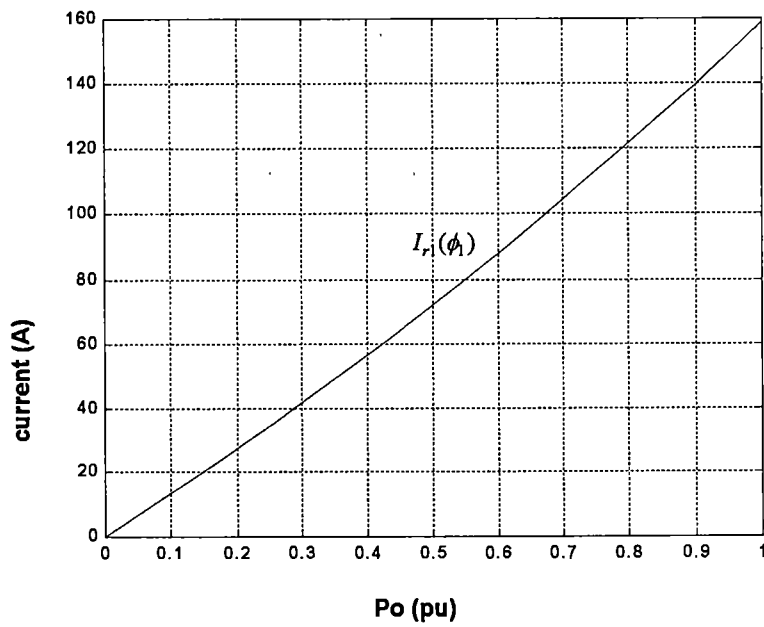
The objective of this research is to find a low cost and highly efficient converter system. The smaller leakage inductance is preferred because the component stress is less and the conduction losses are lower. However, the trade-off is the small phase shift angle control, which requires more critical timing.

III. 4 Summary

In this chapter, the circuit's principles of operation were thoroughly investigated. The mathematical analysis of steady state conditions leads to the design equations and characteristic curves.

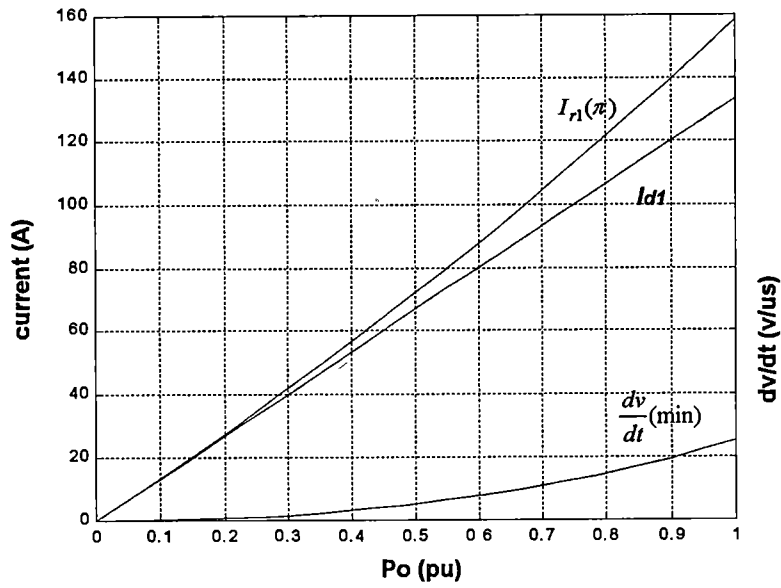


(a) I_{d1} , $I_r(0)$, $\frac{dv}{dt}(\max)$ versus output power

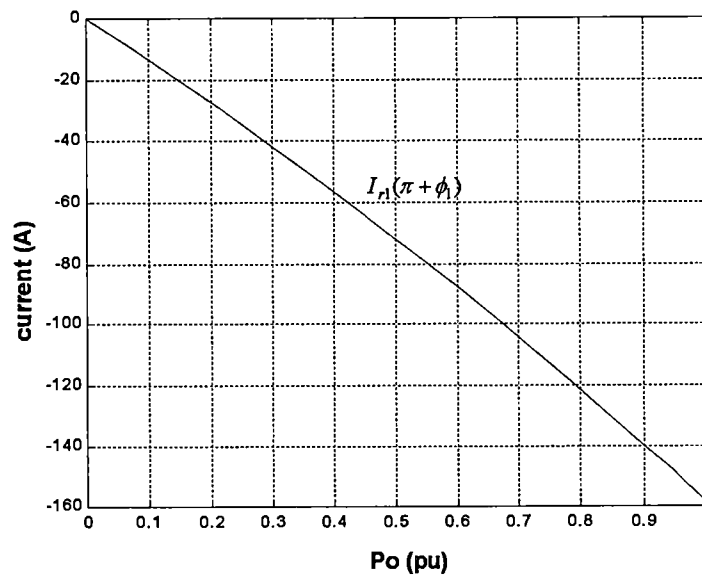


(b) $I_r(\phi)$ versus output power

Fig. 3.18 The soft-switching conditions versus output power of $0.3024\mu\text{H}$



(c) I_{d1} , $I_{rl}(\phi_l)$, dv/dt (min) versus output power



(d) $I_{rl}(\pi + \phi_l)$ versus output power

Fig. 3.18 The soft-switching conditions versus output power of $0.3024\mu\text{H}$

(continued)

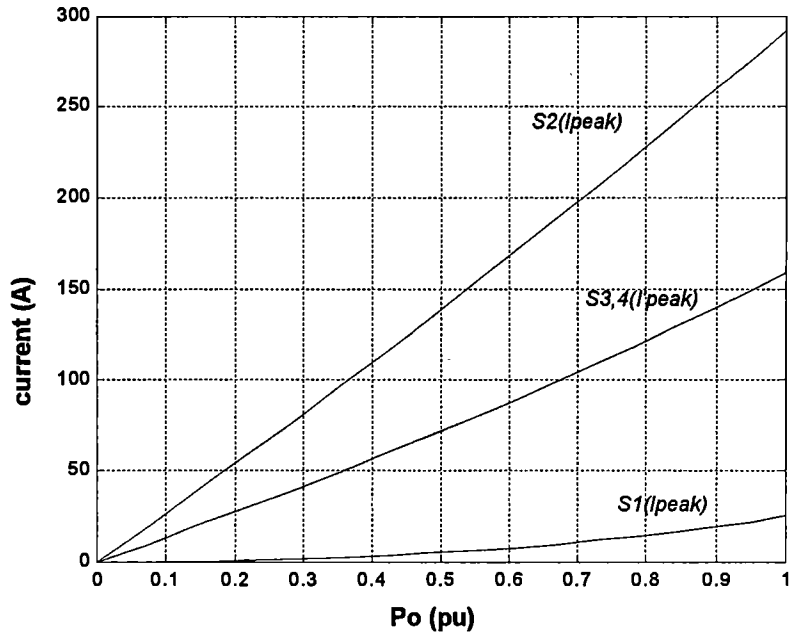


Fig 3.19 Current stresses of main switches versus output power of 0.3024μH

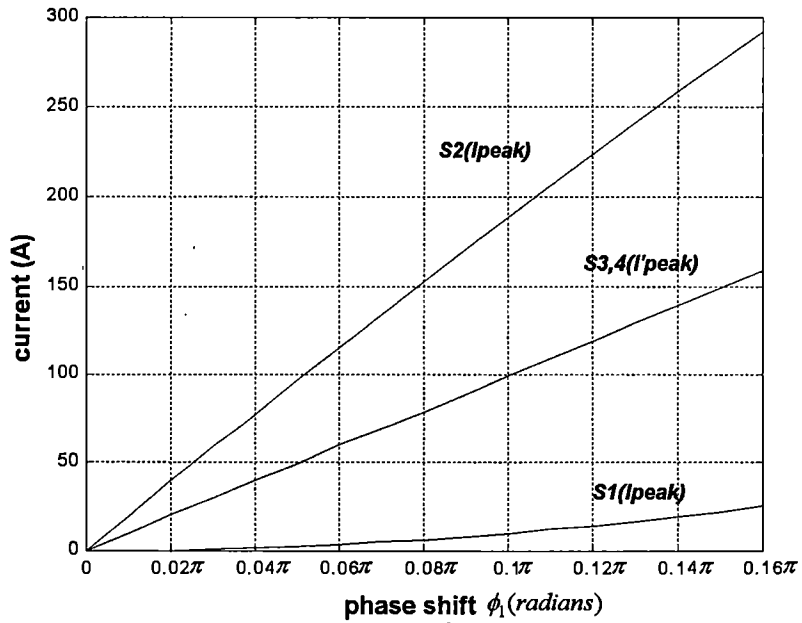


Fig. 3.20 Current stresses of main switches versus phase shift angle of 0.3024μH

Compared to the other soft-switched bi-directional dc-dc converters, this new topology has the following features:

- Decreased number of devices.

Compared to the full-bridge topologies, this converter has a half-bridge on both the low voltage side and the high voltage side, decreasing the number of devices by half.

- Unified soft-switching scheme without auxiliary circuit.

A unified zero-voltage switching is achieved for all the devices in either direction of power flow. Moreover, instead of using an auxiliary circuit, the soft switching conditions are ensured by equation (3-1) or (3-2), according to the different operating modes.

- No high transient voltage for low voltage side switches.

The circuit fires the main device after its anti-parallel diode is conducting. Therefore, it is free of high voltage surge for low voltage side switches at switching due to the interaction between the leakage inductance and diode reverse recovery.

CHAPTER IV

MODELING AND SIMULATION OF PROPOSED CONVERTER

IV. 1 Introduction

Analysis of power electronics systems is complicated by their switching behavior. One well-known approach to the modeling of such systems is to approximate their operation by averaging techniques [23]. The average model can be used to (1) facilitate the fast simulation of dynamic performance for a converter system, and (2) derive a small-signal linearized model for controller design.

This chapter describes the development of the average model of the proposed converter and its first application, the simulation of system performance. The second application, the small-signal model, will be left in the next chapter of control system because it is closely related to the controller design problem.

In section one, the state-space equations for different modes during one switching period are developed. The difficulties of applying traditional averaging techniques for the proposed circuit are identified. Based on the state-space equations, section two introduces a new method to derive a switching-frequency-dependent average model. Section three presents simulation results using the averaged model for open and closed loop operation. The simulation results of the averaged model are also

compared to those of a detailed circuit simulation to verify the accuracy of this technique.

IV .2 State-space Equations of Proposed Converter

To derive the state-space equations, all the switching processes are assumed to be instantaneous. The simplified circuit is drawn in Fig.4.1. The state variables of the dynamic system are chosen to be the inductor current i_L , transformer current i_n , and the capacitor voltages v_1 , v_2 , v_3 , and v_4 . R is the load resistance. These variables are all defined in the primary-referred equivalent circuit of Fig. 4.1.

The different modes of one switching cycle are demonstrated in Fig.4.2. Referring to Fig. 4.1 and Fig. 4.2, the state-space equations of four modes can be derived as follows.

In mode I, S1 and S4 are on. The simplified power circuit and the corresponding equivalent circuit are shown in Fig 4.3 (a) and (b), respectively. In mode II, S1 and S3 are on. The simplified and equivalent circuits are shown in Fig 4.4. In mode III, S2 and S3 are on. The simplified and equivalent circuits are shown in Fig 4.5. In mode IV, S2 and S4 are on. The simplified and equivalent circuits are shown in Fig 4.6.

The corresponding matrix forms of the state-space equations are shown in equations (4-1)-(4-4).

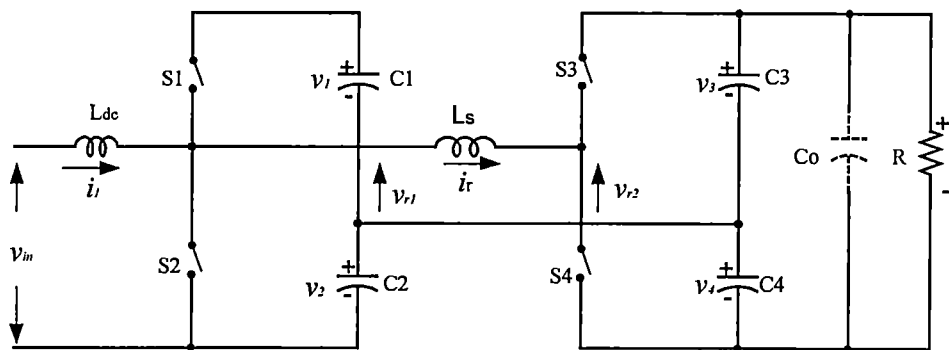


Fig. 4.1 Simplified primary referred equivalent circuit

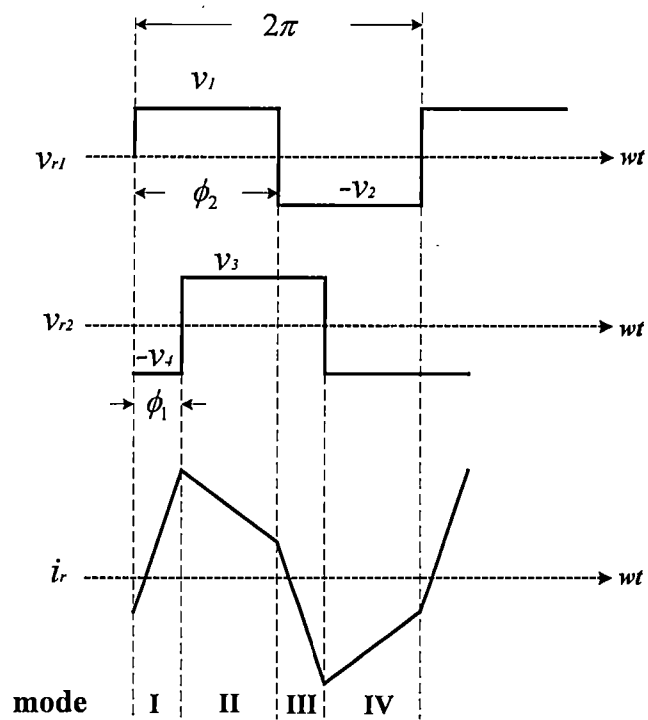
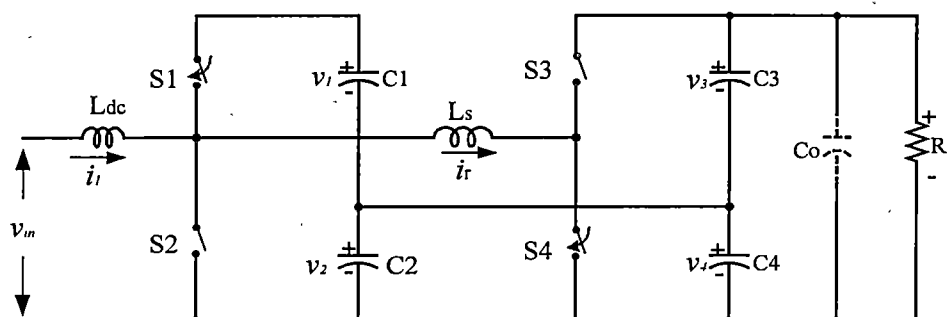
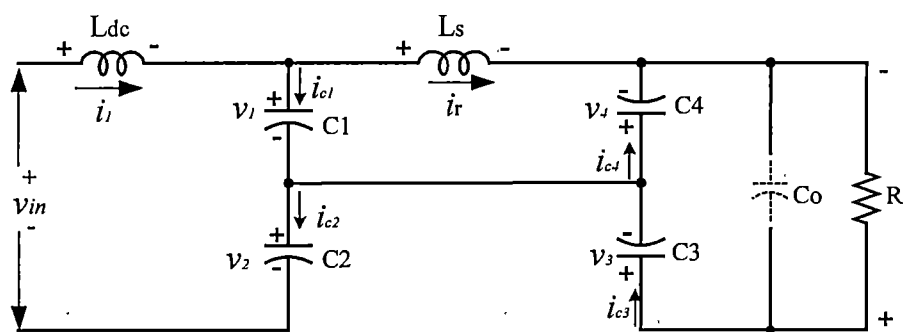


Fig. 4.2 The operation modes of one cycle

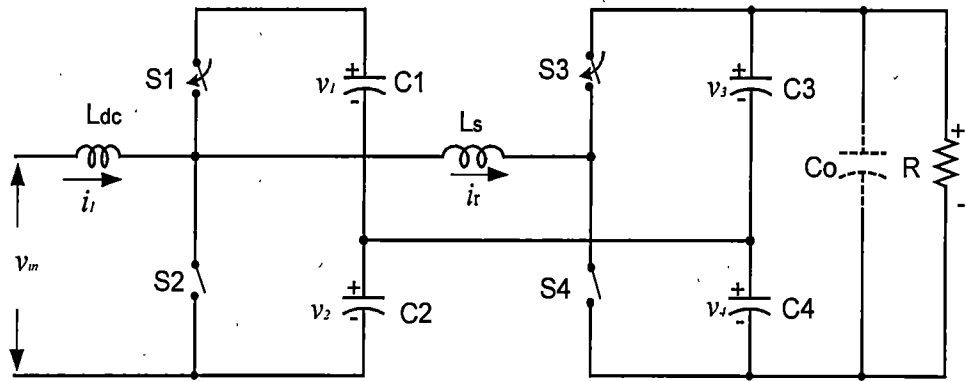


(a) Simplified circuit of mode I

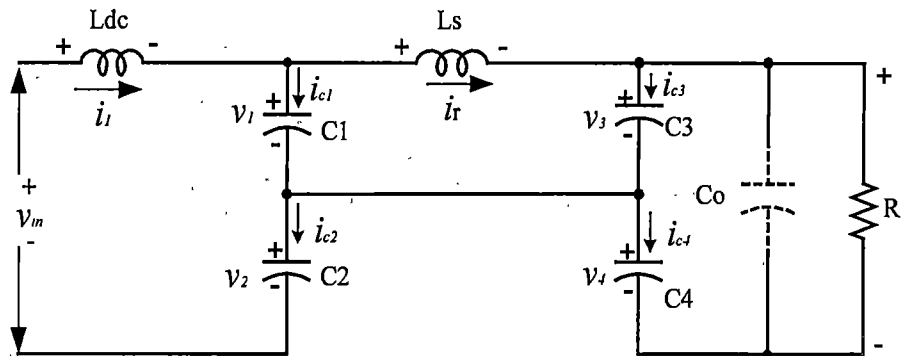


(b) Equivalent circuit of mode I

Fig. 4.3 The power circuit of mode I

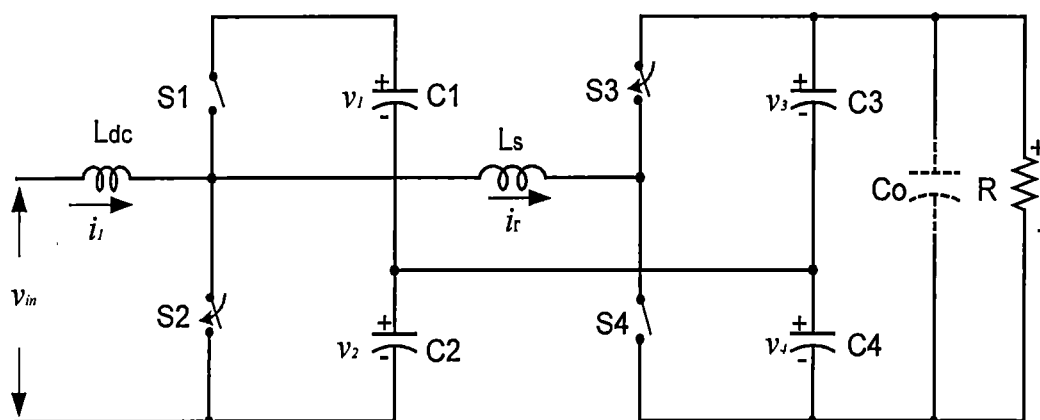


(a) Simplified circuit of mode II

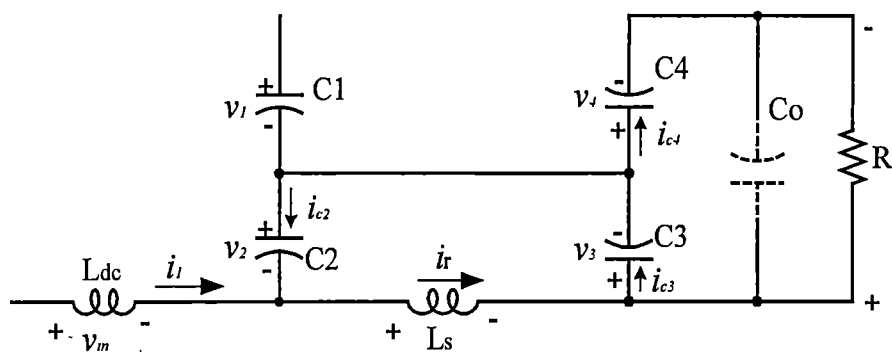


(b) Equivalent circuit of mode II

Fig. 4.4 The power circuit of mode II

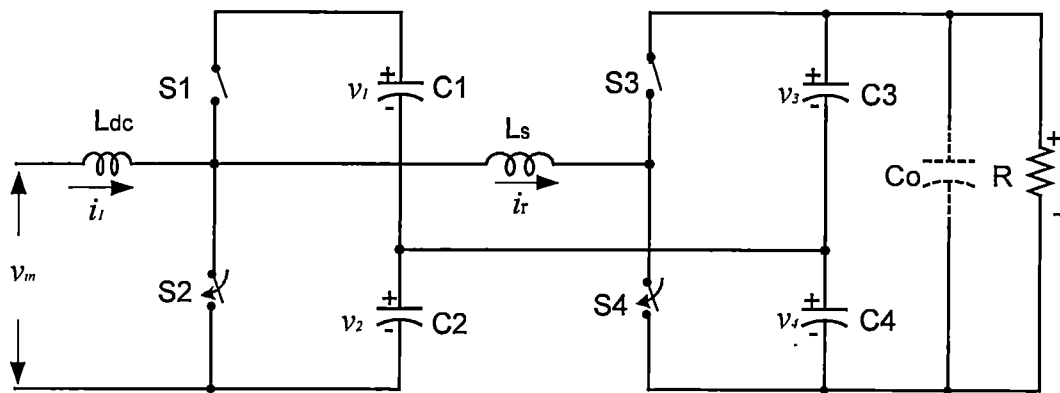


(a) Simplified circuit of mode III

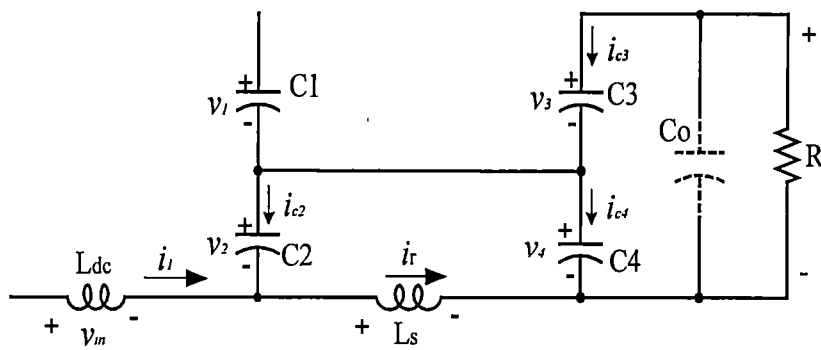


(b) Equivalent circuit of mode III

Fig. 4.5 Power circuit of mode III



(a) Simplified circuit of mode IV



(b) Equivalent circuit of mode IV

Fig. 4.6 Power circuit of mode IV

$$\begin{bmatrix} \bullet \\ i_1 \\ \bullet \\ i_r \\ \bullet \\ v_1 \\ \bullet \\ v_2 \\ \bullet \\ v_3 \\ \bullet \\ v_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & -1/L_{dc} & -1/L_{dc} & 0 & 0 \\ 0 & 0 & 1/L_s & 0 & 0 & 1/L_s \\ 1/C1 & -1/C1 & 0 & 0 & 0 & 0 \\ 1/C2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/RC3 & -1/RC3 \\ 0 & -1/C4 & 0 & 0 & -1/RC4 & -1/RC4 \end{bmatrix}}_{A1} \begin{bmatrix} i_1 \\ i_r \\ v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L_{dc} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B1} v_{in} \quad (4-1)$$

$$\begin{bmatrix} \bullet \\ i_1 \\ \bullet \\ i_r \\ \bullet \\ v_1 \\ \bullet \\ v_2 \\ \bullet \\ v_3 \\ \bullet \\ v_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & -1/L_{dc} & -1/L_{dc} & 0 & 0 \\ 0 & 0 & 1/L_s & 0 & -1/L_s & 0 \\ 1/C1 & -1/C1 & 0 & 0 & 0 & 0 \\ 1/C2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/C3 & 0 & 0 & -1/RC3 & -1/RC3 \\ 0 & 0 & 0 & 0 & -1/RC4 & -1/RC4 \end{bmatrix}}_{A2} \begin{bmatrix} i_1 \\ i_r \\ v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L_{dc} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B2} v_{in} \quad (4-2)$$

$$\begin{bmatrix} \bullet \\ i_1 \\ \bullet \\ i_r \\ \bullet \\ v_1 \\ \bullet \\ v_2 \\ \bullet \\ v_3 \\ \bullet \\ v_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/L_s & -1/L_s & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/C2 & 0 & 0 & 0 & 0 \\ 0 & 1/C3 & 0 & 0 & -1/RC3 & -1/RC3 \\ 0 & 0 & 0 & 0 & -1/RC4 & -1/RC4 \end{bmatrix}}_{A3} \begin{bmatrix} i_1 \\ i_r \\ v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L_{dc} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B3} v_{in} \quad (4-3)$$

$$\begin{bmatrix} \dot{i}_1 \\ \dot{i}_r \\ \dot{v}_1 \\ \dot{v}_2 \\ \dot{v}_3 \\ \dot{v}_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1/L_s & 0 & 0 & 1/L_s \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/C2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/RC3 & -1/RC3 \\ 0 & -1/C4 & 0 & 0 & -1/RC4 & -1/RC4 \end{bmatrix}}_{A4} \begin{bmatrix} i_1 \\ i_r \\ v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L_{dc} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B4} v_{in} \quad (4-4)$$

The DC averages of all the variables exist. For i_r , which is the ac current flowing through the isolation transformer, the DC average over each switching cycle is equal to zero. As a result, the key problem of developing the average model for this converter is to exclude i_r , which is possible because i_r can be represented by $i_r = f(v_1, v_2, v_3, v_4)$, using a circuit analysis of the four modes of operation. However, it is impossible to cancel i_r using the ordinary state-space averaging technique. In addition, the conventional averaging techniques are independent of switching frequency, and the average models derived are not accurate when the switching frequency is low. This will not be acceptable for the proposed converter because the switching frequency is a possible control variable. Thus, a new switching frequency dependent averaging technique is developed to solve these problems.

IV .3 Switch Frequency-Dependable Average Model

IV. 3.1 Average Model Development

Instead of using four separate matrix forms of the state-space equations to represent the modes, one first-order equation group is derived to describe all the

operation modes.

$$\begin{cases} \frac{di_1}{dt} = [v_{in} - S_p(v_1 + v_2)] / L_{dc} \\ \frac{dv_1}{dt} = -S_p i_r / C_p + S_p i_1 / C_p \\ \frac{dv_2}{dt} = i_r(1 - S_p) / C_p + S_p i_1 / C_p \\ \frac{dv_3}{dt} = \frac{1}{C_s} \left\{ -\frac{v_3 + v_4}{R} (1 - S_s) + (i_r - \frac{v_3 + v_4}{R}) S_s \right\} \\ \frac{dv_4}{dt} = \frac{1}{C_s} \left\{ -(\frac{v_3 + v_4}{R}) (1 - S_s) - \frac{v_3 + v_4}{R} S_s \right\} \end{cases} \quad (4-5)$$

S_p and S_s are the switch functions of the primary side and the secondary side, respectively. The waveforms and the mathematical representation are shown in Fig.

4.7.

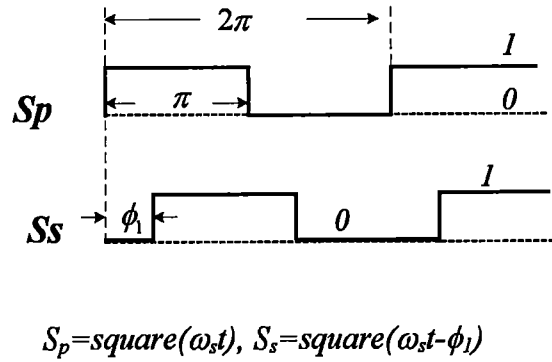


Fig. 4.7 The waveforms of switch function S_p and S_s

According to Fig.4.2, i_r can be calculated by integration as follows:

$$\left\{ \begin{array}{l} \text{Mode I : } i_r = \frac{v_1 + v_4}{\omega L_s} \theta + i_r(0) \\ \text{Mode II : } i_r = \frac{v_1 - v_3}{\omega L_s} (\theta - \phi_1) + i_r(\phi_1) \\ \text{Mode III : } i_r = \frac{-v_2 - v_3}{\omega L_s} (\theta - \pi) + i_r(\pi) \\ \text{Mode IV : } i_r = \frac{-v_2 + v_4}{\omega L_s} (\theta - \pi - \phi_1) + i_r(\pi + \phi_1) \end{array} \right. \quad (4-6)$$

The initial states $i_r(0), i_r(\phi_1), i_r(\pi), i_r(\pi + \phi_1)$ can be derived in equation (4-7).

$$\left\{ \begin{array}{l} i_r(0) = \frac{v_3 - v_1}{2\omega L_s} (\pi - \phi_1) - \frac{v_1 + v_4}{2\omega L_s} \phi_1 \\ i_r(\phi_1) = \frac{v_1 + v_4}{2\omega L_s} \phi_1 + \frac{v_3 - v_1}{2\omega L_s} (\pi - \phi_1) \\ i_r(\pi) = -i_r(0) = -\frac{v_3 - v_1}{2\omega L_s} (\pi - \phi_1) + \frac{v_1 + v_4}{2\omega L_s} \phi_1 \\ i_r(\pi + \phi_1) = -i_r(\phi_1) = -\frac{v_1 + v_4}{2\omega L_s} \phi_1 - \frac{v_3 - v_1}{2\omega L_s} (\pi - \phi_1) \end{array} \right. \quad (4-7)$$

Taking a moving average for the switching period $T_s := 1/f_s$ for (4-5) and replacing i_r by (4-6) and (4-7), the average model of this converter can be expressed in equation (4-8).

The Matlab/Simulink implementation of the average model for the proposed converter is shown in Fig. 4.8.

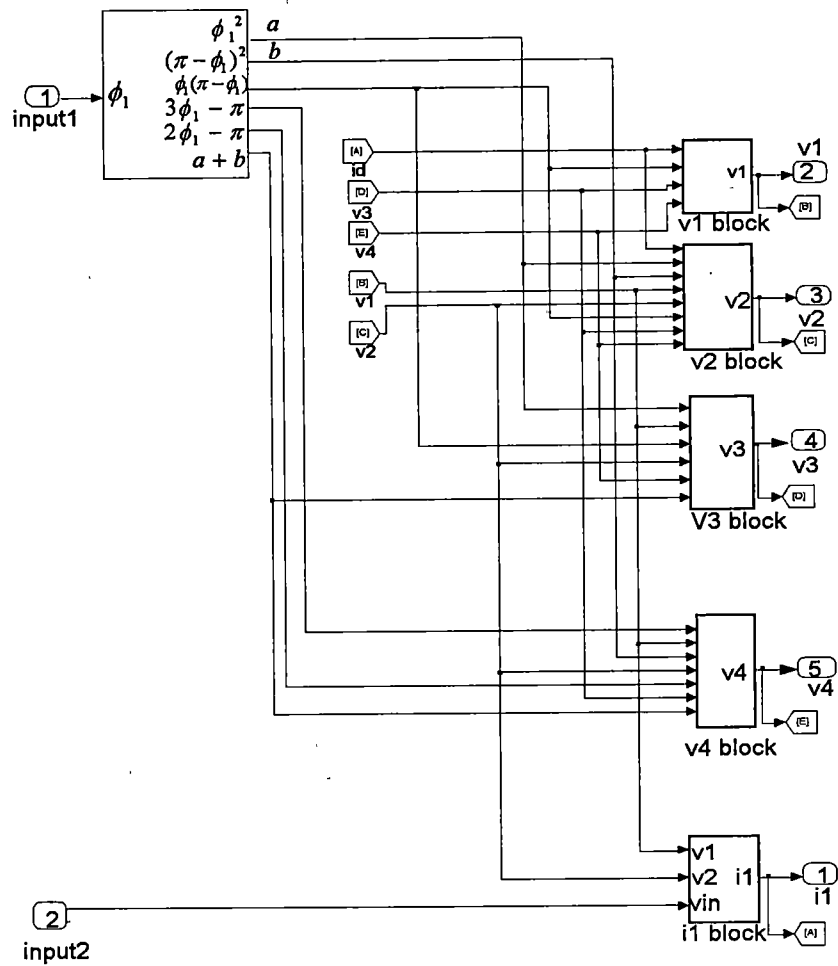


Fig. 4.8 Matlab/Simulink block diagram of average model

$$\begin{bmatrix} \bullet \\ i_{1avg} \\ \bullet \\ v_{1avg} \\ \bullet \\ v_{2avg} \\ \bullet \\ v_{3avg} \\ \bullet \\ v_{4avg} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L_{dc}} & \frac{1}{2L_{dc}} & 0 \\ \frac{1}{2C_p} & 0 & 0 & -\frac{\phi_1(\pi-\phi_1)}{Con1} \\ \frac{1}{2C_p} & \frac{\phi_1^2 + (\pi-\phi_1)^2}{Con1} & -\frac{\phi_1^2 - (\pi-\phi_1)^2}{Con1} & \frac{\phi_1^2 - \phi_1(\pi-\phi_1) + (\pi-\phi_1)^2}{Con1} \\ 0 & \frac{\phi_1^2 + 2\phi_1(\pi-\phi_1)}{Con2} & -\frac{\phi_1^2}{Con2} & \frac{\phi_1^2 + \phi_1(\pi-\phi_1)}{Con2} \\ 0 & \frac{(\phi_1 - \pi)(\pi - 3\phi_1)}{Con2} & \frac{(\pi - \phi_1)^2}{Con2} & \frac{(\pi - \phi_1)(\pi - 2\phi_1)}{Con2} \end{bmatrix} \begin{bmatrix} \bullet \\ i_{1avg} \\ \bullet \\ v_{1avg} \\ \bullet \\ v_{2avg} \\ \bullet \\ v_{3avg} \\ \bullet \\ v_{4avg} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{dc}} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}$$

(4-8)

Where $Con1 = C_p T_s \omega \cdot 2\omega L_s$, $Con2 = C_s T_s \omega \cdot 2\omega L_s$, $C_p = C1 = C2$, $C_s = C3 = C4$

If the output bus capacitor C_o is considered, the average model becomes as follows.

$$\begin{aligned}
& \begin{bmatrix} i_{1avg} \\ v_{1avg} \\ v_{2avg} \\ v_{3avg} \\ v_{4avg} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L_{dc}} & 0 \\ 1 & \frac{1}{2C_p} & 0 \\ \frac{1}{2C_p} & 0 & -\frac{1}{2L_{dc}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 & -\phi_1(\pi - \phi_1) & 0 \\ -\phi_1(\pi - \phi_1) & \frac{con1}{con2} & \frac{con1}{con2} \\ -[\phi_1^2 + (\pi - \phi_1)^2] & \frac{con1}{con2} & \frac{con1}{con2} \\ -[\phi_1^2 - (\pi - \phi_1)^2] & \frac{con1}{con2} & \frac{con1}{con2} \\ -[\phi_1^2 + \phi_1(\pi - \phi_1)] & \frac{con2}{con3} & \frac{con2}{con3} \\ -[\phi_1^2 + (\pi - \phi_1)^2]C_o & \frac{con3}{con2} & \frac{con3}{con2} \\ (\phi_1 - \pi)(\pi - 3\phi_1) & \frac{con2}{con3} & \frac{con2}{con3} \\ [\phi_1^2 + (\pi - \phi_1)^2]C_o & \frac{con3}{con2} & \frac{con3}{con2} \end{bmatrix} \begin{bmatrix} -\phi_1(\pi - \phi_1) & \frac{con1}{con2} & \frac{con1}{con2} \\ \phi_1^2 - \phi_1(\pi - \phi_1) + (\pi - \phi_1)^2 & \frac{con1}{con2} & \frac{con1}{con2} \\ \phi_1^2 + \phi_1(\pi - \phi_1) & \frac{con2}{con3} & \frac{con2}{con3} \\ \phi_1^2 + (\pi - \phi_1)^2 & \frac{con3}{con2} & \frac{con3}{con2} \\ -[\phi_1^2 + (\pi - \phi_1)^2]C_o & \frac{con2}{con3} & \frac{con2}{con3} \\ -[\phi_1^2 + (\pi - \phi_1)^2]C_o & \frac{con3}{con2} & \frac{con3}{con2} \\ -[\phi_1^2 + (\pi - \phi_1)^2]C_o & \frac{con2}{con3} & \frac{con2}{con3} \\ -[\phi_1^2 + (\pi - \phi_1)^2]C_o & \frac{con3}{con2} & \frac{con3}{con2} \end{bmatrix} \begin{bmatrix} i_{1avg} \\ v_{1avg} \\ v_{2avg} \\ v_{3avg} \\ v_{4avg} \end{bmatrix} \\
& + \begin{bmatrix} 1 \\ \frac{1}{L_{dc}} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}
\end{aligned}$$

IV. 3.2 Simulation of ac variables

The averaged model can provide not only the information of dc variables but ac variables as well. During steady states, the peak values of ac current i_r of one switching cycle, which are shown in Fig 4.9, can be derived from equation (4-10).

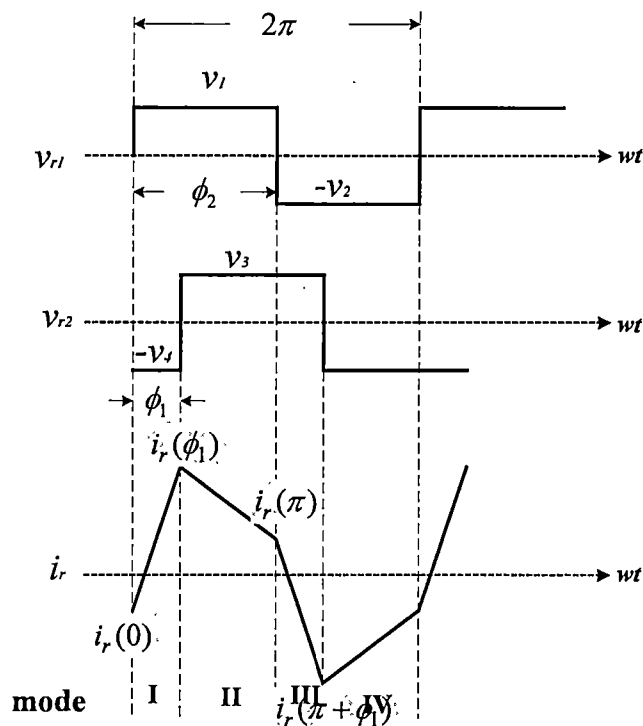


Fig. 4.9 The peak values of i_r waveform during one cycle

$$\begin{cases} i_r(0) = \frac{v_3 - v_1}{2\omega L_s}(\pi - \phi_1) - \frac{v_1 + v_4}{2\omega L_s}\phi_1 \\ i_r(\phi_1) = \frac{v_1 + v_4}{2\omega L_s}\phi_1 + \frac{v_3 - v_1}{2\omega L_s}(\pi - \phi_1) \\ i_r(\pi) = -i_r(0) \\ i_r(\pi + \phi_1) = -i_r(\phi_1) \end{cases} \quad (4-10)$$

According to equation (4-10), the ac current i_r depends on the dc variables v_1 , v_2 , v_3 , and v_4 . Since these dc quantities can be derived from the average model, further algebra calculation will release the information of ac variables.

IV. 3.3 Mathematical Verification and Simplification of Average Model

According to the circuit analysis, $v_1 = v_2$ and $v_3 = v_4$ when $D = 50\%$. This can also be verified by the mathematical model.

By performing the Laplace transform of Equation (4-9) and by solving for the voltage variables,

$$\begin{cases} v_{1avg}(s) = \frac{8(sC_t R + 2)L_s^2 C_s f_s^2 \pi^4}{D(s)} \cdot \frac{v_{in}}{L_{dc} s} \\ v_{2avg}(s) = \frac{8(sC_t R + 2)L_s^2 C_s f_s^2 \pi^4}{D(s)} \cdot \frac{v_{in}}{L_{dc} s} \\ v_{3avg}(s) = \frac{-2R(\phi_1 - \pi)L_s f_s \phi_1 \pi^2 C_s}{D(s)} \cdot \frac{v_{in}}{L_{dc} s} \\ v_{4avg}(s) = \frac{-2R(\phi_1 - \pi)L_s f_s \phi_1 \pi^2 C_s}{D(s)} \cdot \frac{v_{in}}{L_{dc} s} \end{cases} \quad (4-11)$$

where
$$D(s) = sRC_p\phi_1^4 - 2sRC_p\pi\phi_1^3 + sRC_p\pi^2\phi_1^2 + 16s^3RC_p\pi^4f_s^2C_sL_s^2C_t + 32s^2C_p\pi^4f_s^2C_sL_s^2 + 8\pi^4f_s^2sC_tL_sC_sR + 16C_s\pi^4f_s^2L_s.$$

From equation (4-11), it is clear that $v_1 = v_2$ and $v_3 = v_4$. Therefore, equation (4-9) can be further simplified as a third-order nonlinear state space equation (4-12):

$$\begin{cases} \dot{i}_{1avg} = \frac{-1}{2L_{dc}}v_{12avg} + \frac{1}{L_{dc}}v_{in} \\ \dot{v}_{12avg} = \frac{1}{C_p}i_{1avg} - \frac{2\phi_1(\pi - \phi_1)}{C_pT_s\omega \cdot 2\omega L_s}v_{34avg} \\ \dot{v}_{34avg} = \frac{2\phi_1(\pi - \phi_1)}{(C_s + 2C_o)T_s\omega \cdot 2\omega L_s}v_{12avg} - \frac{2}{(C_s + 2C_o)R}v_{34avg} \end{cases} \quad (4-12)$$

where $v_{12avg} = v_{1avg} + v_{2avg}$, and $v_{34avg} = v_{3avg} + v_{4avg}$.

IV. 3.4 Simulation Block Diagram

Based on equation (4-12) and equation (4-10), which represent the simplified average mode and the calculation of ac current magnitude, respectively, the Matlab/Simulink simulation block diagram of the proposed converter is shown in Fig. 4.10.

The two inputs are the dc voltage v_{in} and the phase shift angle ϕ_l . The dc input current i_d , which equals i_l , the capacitor voltage v_{12} and v_{34} , and the minimum and maximum magnitudes of the ac current i_r are the five outputs.

With the simulation block diagram available, the dynamic performance of the converter system are simulated and studied in the following section.

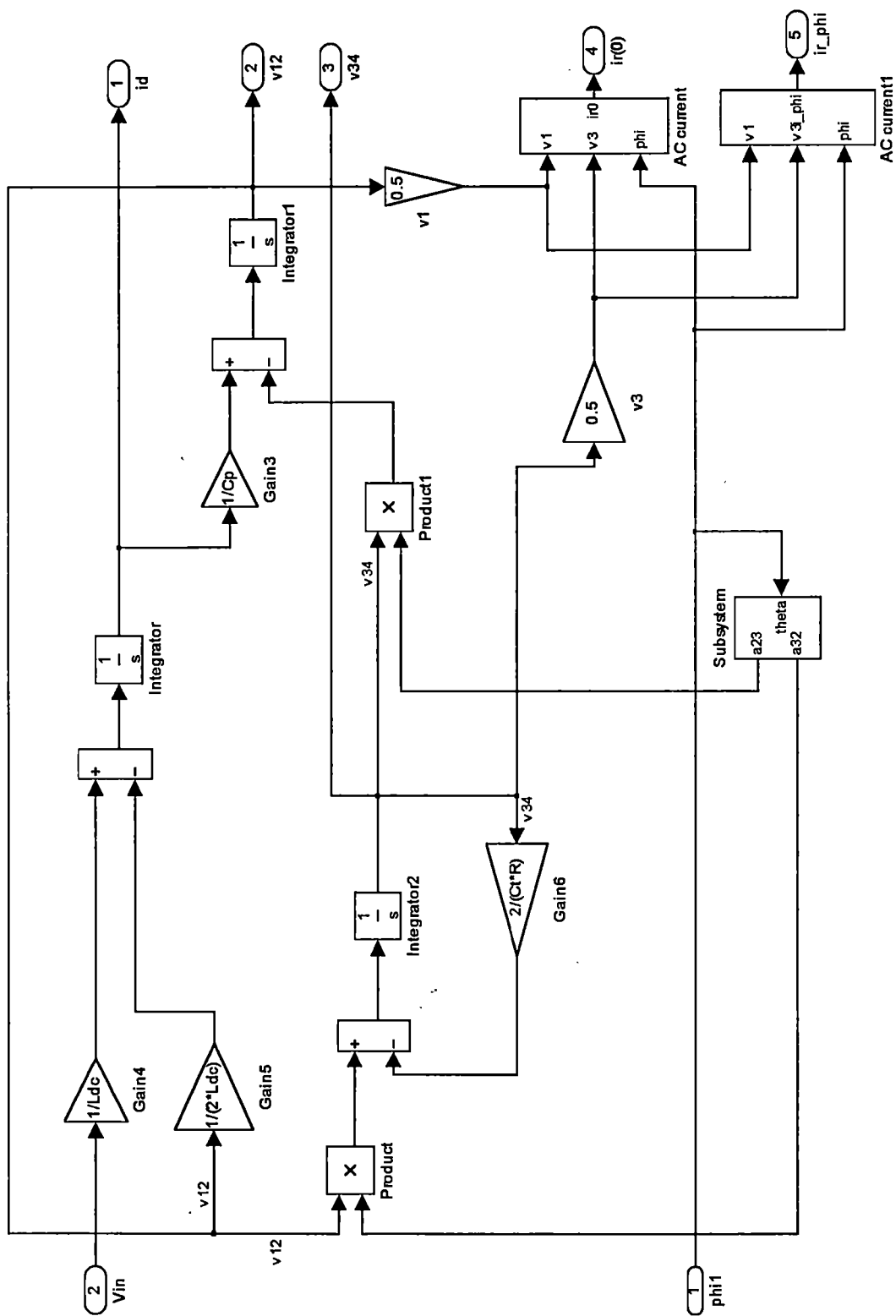


Fig. 4.10 Matlab/Simulink block diagram of simplified average model

IV. 4 Simulation and Verification of Average Model

In this section, the following work has been done. (1) Simulate the dynamic performance of the proposed converter, and (2) verify the average model by comparing the simulation results of the average model and those of the detailed circuit simulation. In the previous section, the average mode is verified mathematically by proving $v_1 = v_2$ and $v_3 = v_4$. In addition, this can be verified further by comparing the agreement of two simulation approaches.

Before comparing the results, the inherent differences of the two simulation approaches are pointed out. The average model is derived by assuming the ideal switching process, so there is no switching loss in its simulation. However, the detailed circuit simulation includes switching loss. Second, the simulation results of Matlab/Simulink represent the average values of dc variables. The detailed circuit simulation results include not only average values but also ripple content.

The average model will simulate three dynamic processes under different conditions, respectively. All the simulation parameters are based on the primary-referenced equivalent circuit. The corresponding simulation block diagrams using Matlab/Simulink (average model) and PSIM (detailed circuit model) can be found in Appendix A.

IV. 4.1 Simulation example 1

A start-up process for the open-loop converter system under step-input voltage of 12 volts is simulated. The simulation parameters are listed below:

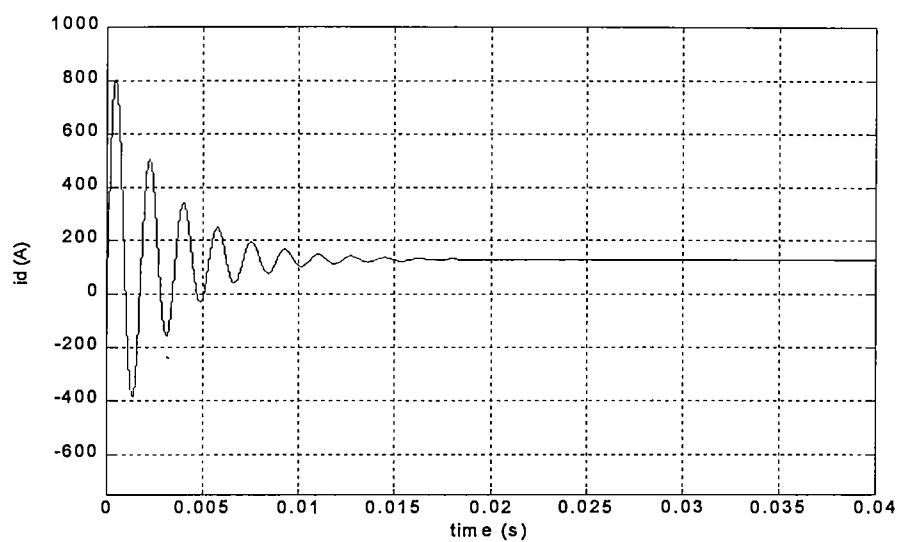
$v_{in} = 12V$, $D = 50\%$, $f_s = 20 \text{ kHz}$, $L_{dc} = 4 \mu H$, $L_s = 0.02 \mu H$, $C1 = C2 = C3 = C4 = 5 \text{ mF}$, $R = 0.36 \text{ ohms}$, $\phi_1 = 0.5 \pi$

The simulation results of the average model and the detailed circuit simulation are shown in Fig. 4.11. to Fig. 4.14. When the duty cycle is 50%, $v_1 = v_2$ and $v_3 = v_4$. The key waveforms of dc variables are selected for i_L , v_{L2} (or $v_1 + v_2$), and v_{34} (or $v_3 + v_4$). The comparison demonstrates their similarity in shape, frequency and magnitude. Fig. 4.14 demonstrates the consistent results of the simulations' predictions for the envelope of i_r .

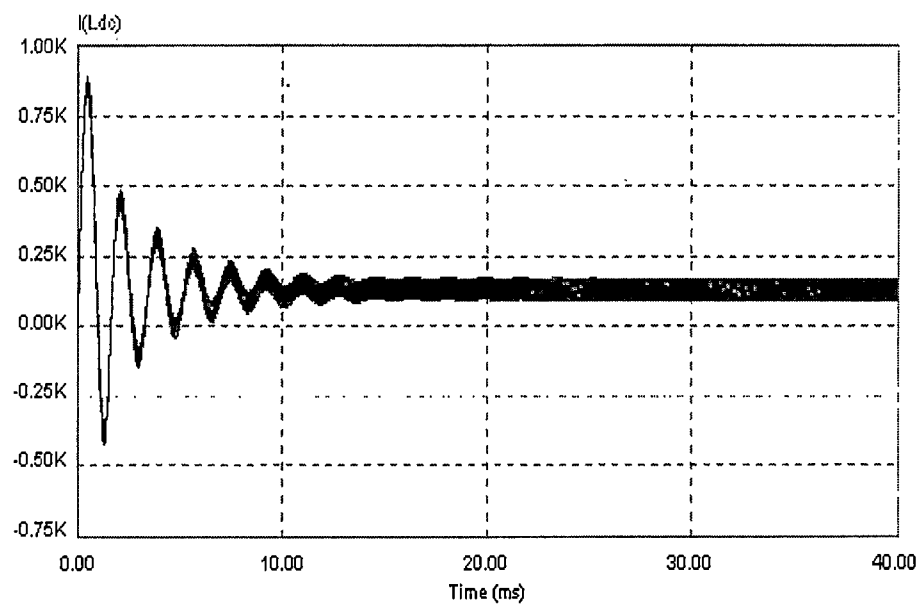
The simulated performance shows that the open-loop converter should not be started using a step-input voltage because the large inrush current will likely damage the devices, and make the inductor and transformer saturate. There is also a large oscillation in capacitor voltages v_1 , v_2 , v_3 , v_4 . This is to be expected since the converter start up behavior is similar to that of a boost converter. The inherent characteristic associated with a boost converter is the large inrush current during start up process.

IV. 4.2 Simulation Example 2

Another start-up process of the open-loop converter system using a ramp input voltage of 12 volts is simulated under the conditions below:

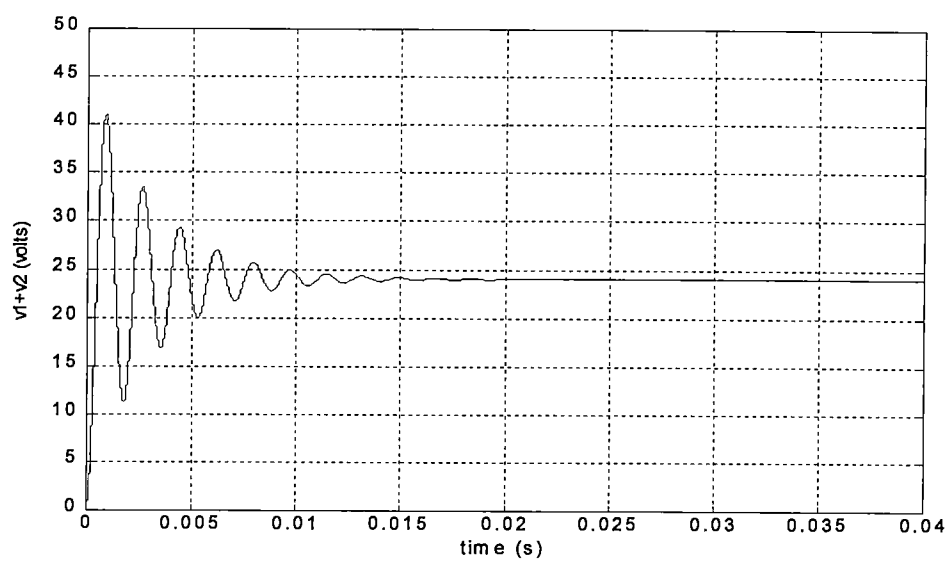


(a) i_d of average model

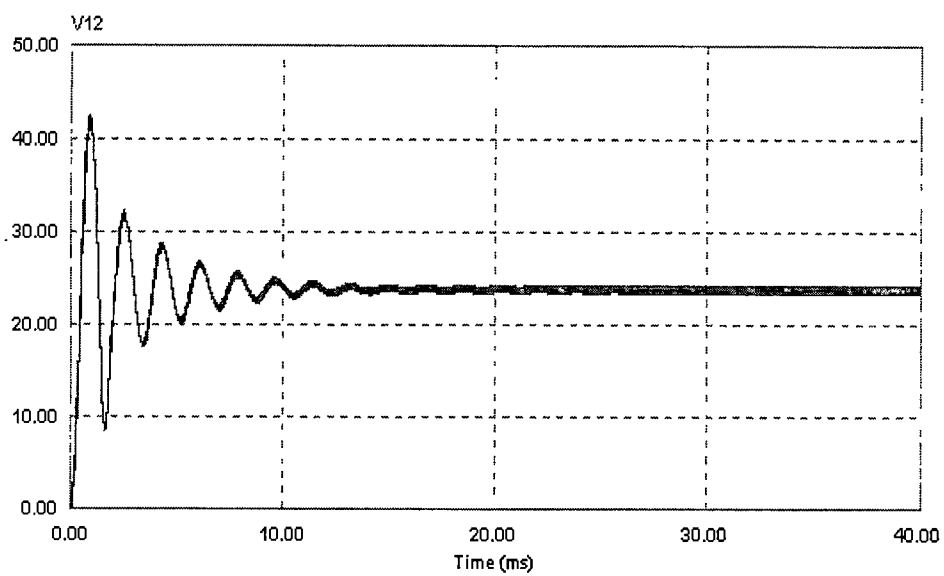


(b) i_d of detailed circuit simulation

Fig. 4.11 The simulation and comparison of i_d in example 1

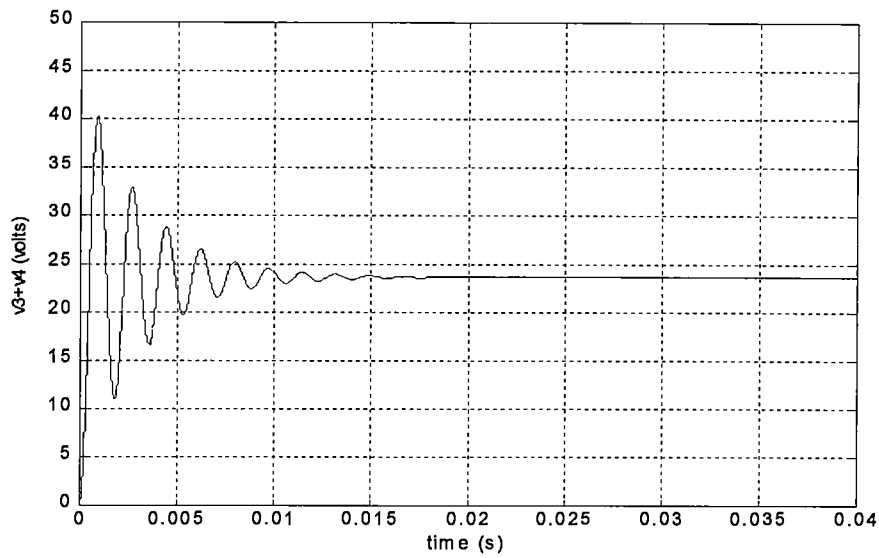


(a) $v_1 + v_2$ of average model

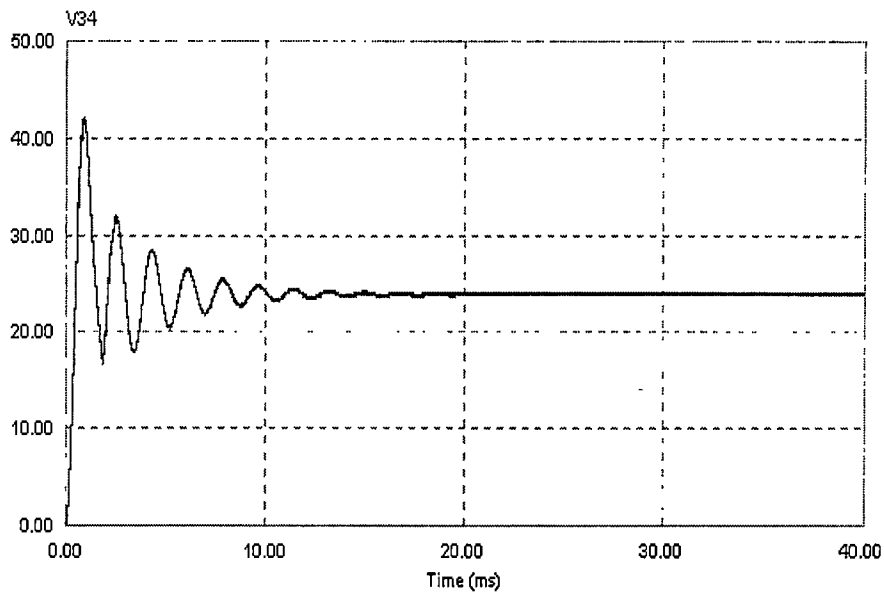


(b) $v_1 + v_2$ of average model

Fig. 4.12 The simulation and comparison of v_{12} in example 1

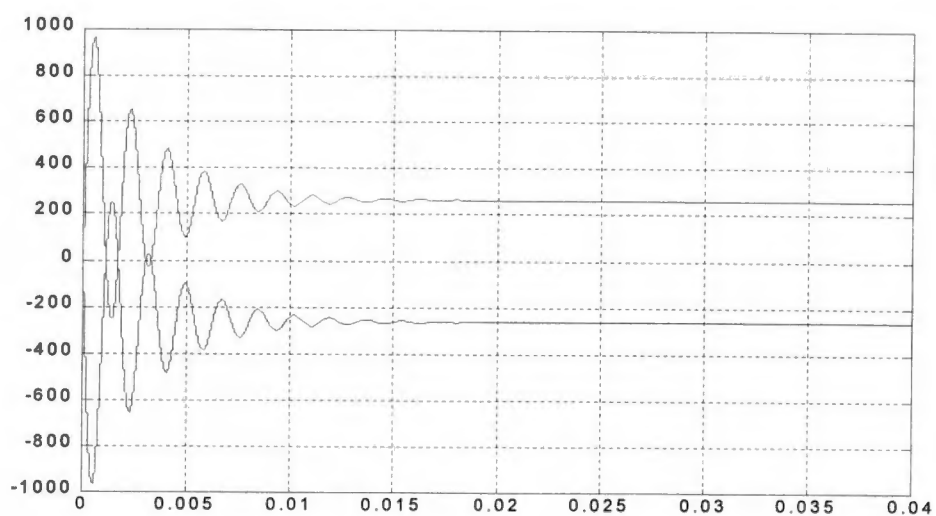


(a) $v_3 + v_4$ of average model

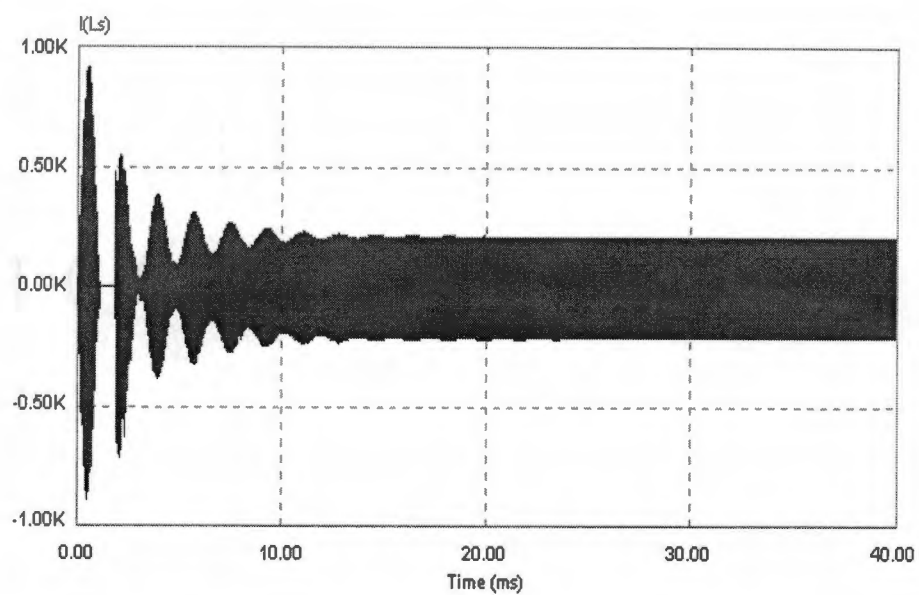


(b) $v_3 + v_4$ of detailed circuit simulation

Fig. 4.13 The simulation and comparison of v_{34} in example 1



(a) The i_r envelope of average model



(b) The i_r envelope of detailed circuit simulation

Fig. 4.14 The simulation and comparison of i_r envelope in example 1

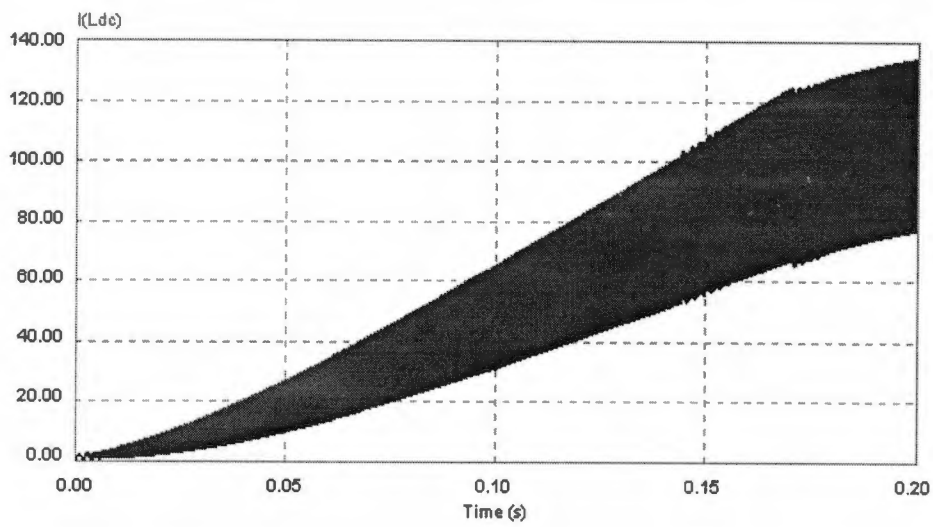
$v_{in} = 12\text{V}$, $D = 50\%$, $f_s = 20\text{ kHz}$, $L_{dc} = 5\mu\text{H}$, $L_s = 0.3024\text{ }\mu\text{H}$, $C1 = C2 = C3 = C4 = 10\text{ mF}$, $C_o = 169\text{ mF}$, $R = 0.27\text{ ohms}$

The waveforms for i_L , v_{12} (or v_1+v_2), and v_{34} (or v_3+v_4) of the average model and detailed circuit model are shown in Fig. 4.15 (a)-(b) and Fig. 4.16 (a)-(b), respectively. The comparison demonstrates their similarity consistence in shape, frequency and average magnitude. The verification of the ac variables is demonstrated in Figures 4.17 and 4.18. Fig. 4.17 (a) is the maximum magnitude of i_r of detailed circuit simulation. Fig. 4.17 (b) is the maximum magnitude of i_r of the average model simulation. Fig. 4.18 (a) is the detailed waveform of i_r from 19.98 ms to 20 ms. The $i_r(0)'$ and $i_r(\phi I)'$ marked in (a) is found to agree with those of average model, which are shown in Fig. 4.18 (b).

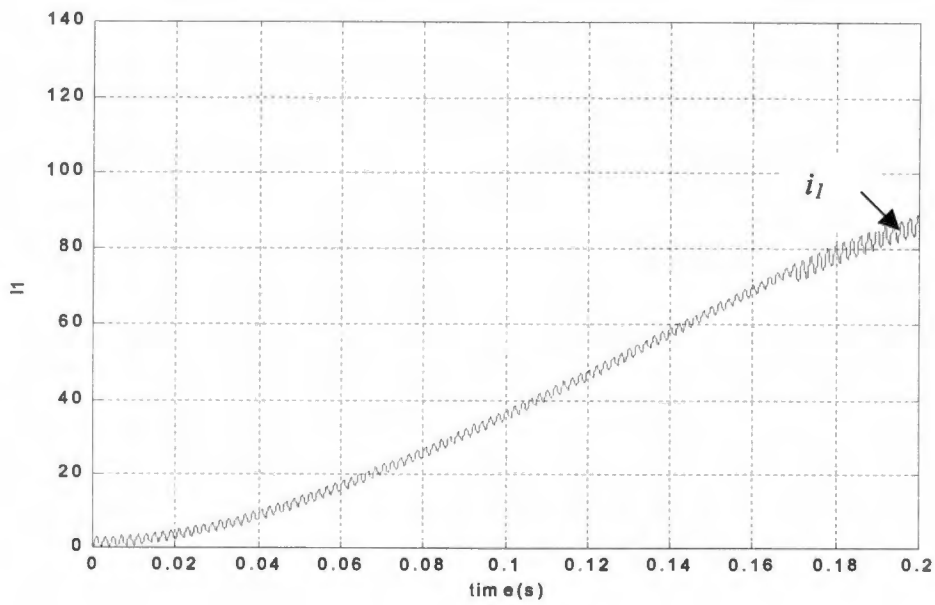
The system performance shows that when the open-loop converter starts under a slowly increased voltage source, the input dc current and transformer current are becoming smaller. The problems of overrated devices, saturation of magnetic components and oscillation of capacitor voltages can be avoided. However, the output voltage v_{34} is built up slowly.

IV. 4.3 Simulation Example 3

A third dynamic process is that a closed-loop converter system is starting under ramp-input voltage. The block diagram of this closed-loop system is shown in Fig. 4.19.

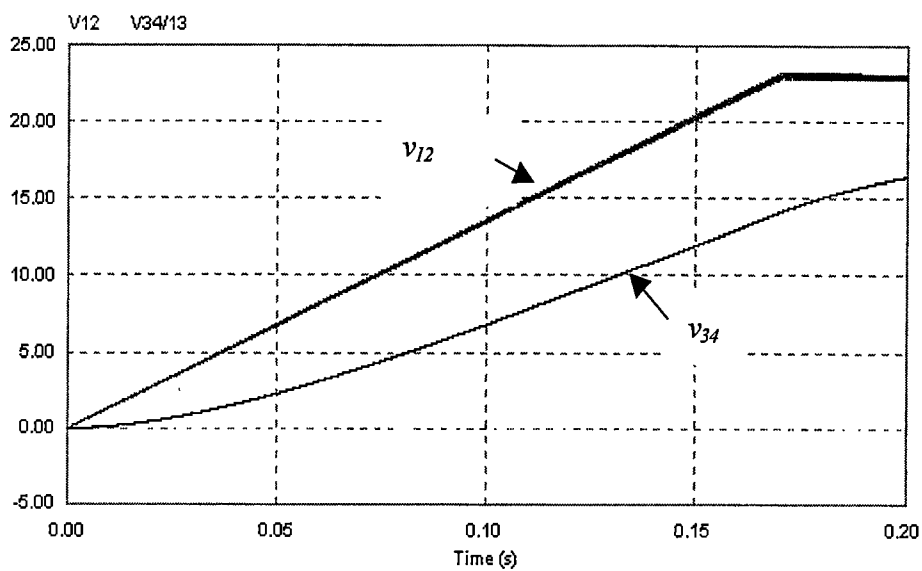


(a) i_L of detailed circuit simulation

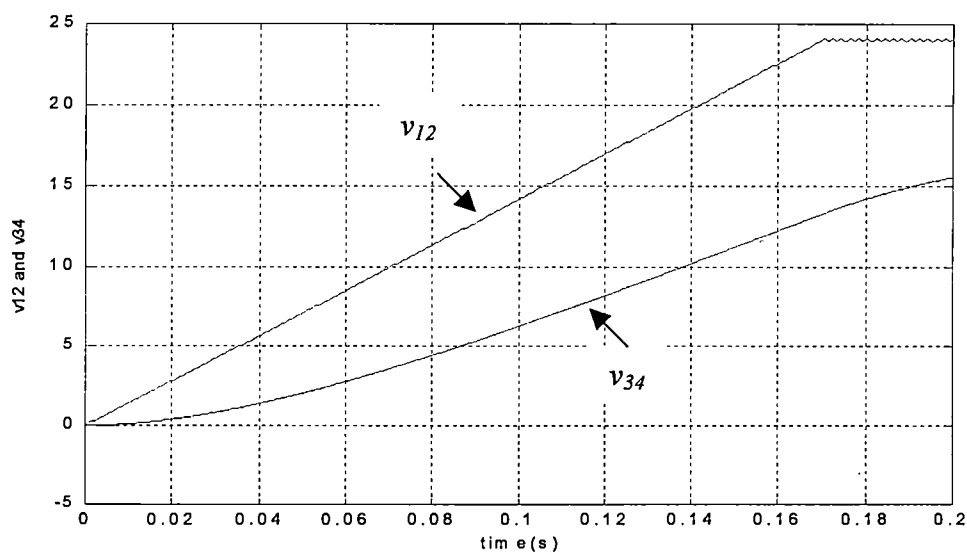


(b) i_L of average model

Fig. 4.15 The simulation and comparison of i_L in example 2

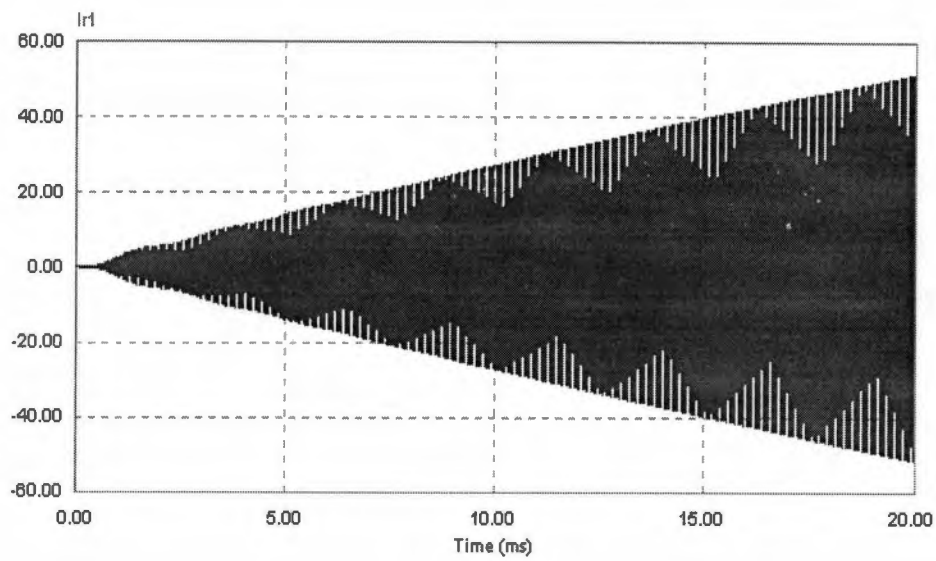


(a) v_{12} and v_{34} of detailed circuit simulation

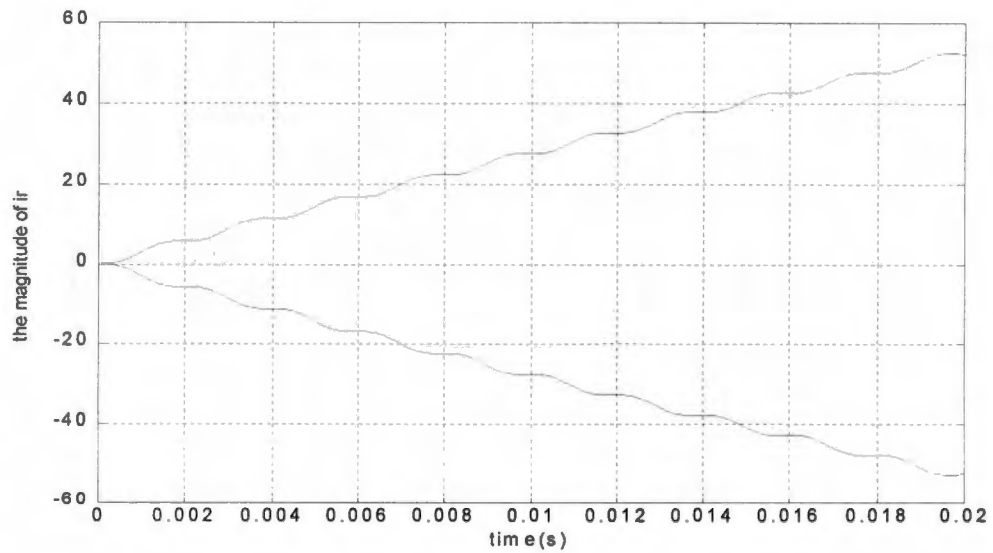


(b): v_{12} and v_{34} of average model

Fig. 4.16 The simulation and comparison of v_{12} and v_{34} in example 2

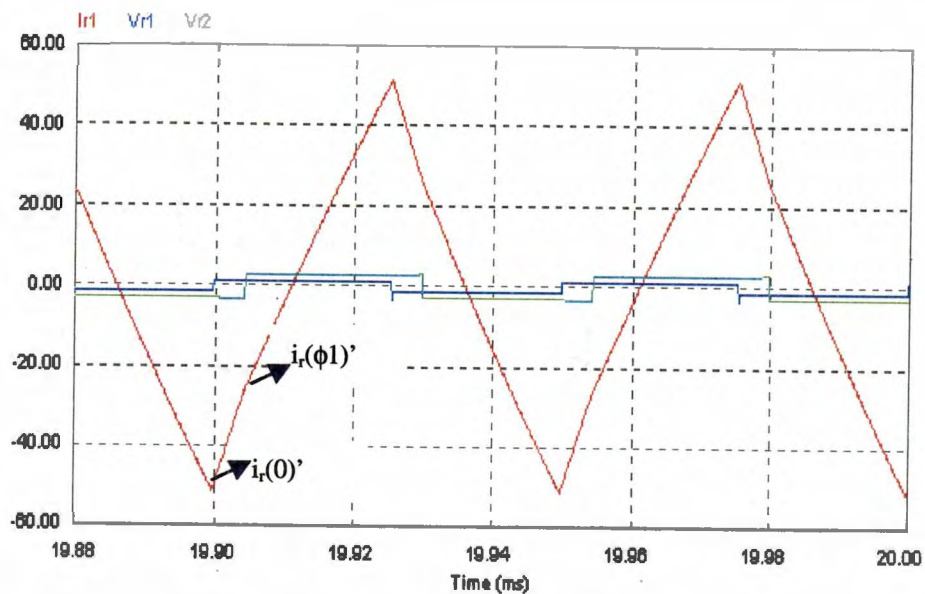


(a) The envelope of i_r of detailed circuit simulation

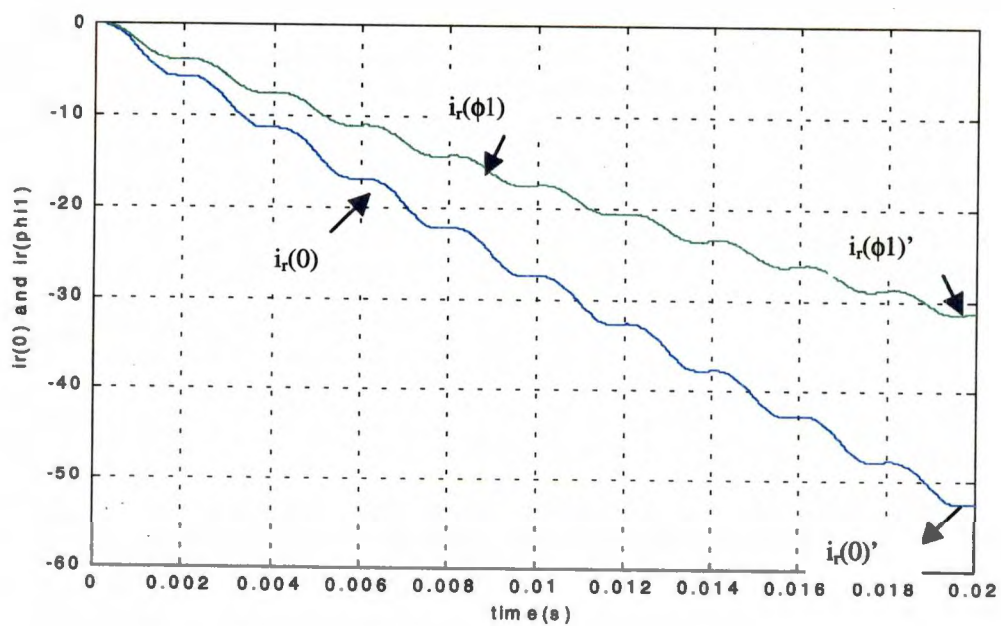


(b) The envelope of i_r of average mode simulation

Fig. 4.17 The simulation and comparison of peak magnitude of i_r in example 2



(a) $i_r(0)$ and $i_r(\phi 1)$ of one full switching cycle in detailed circuit simulation



(b) $i_r(0)$ and $i_r(\phi 1)$ of average model

Fig. 4.18 The simulation and comparison of $i_r(0)$ and $i_r(\phi 1)$ in example 2

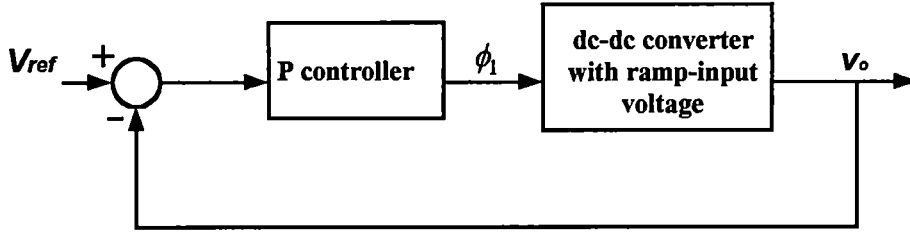


Fig. 4.19 The block diagram of closed-loop system in simulation example 3

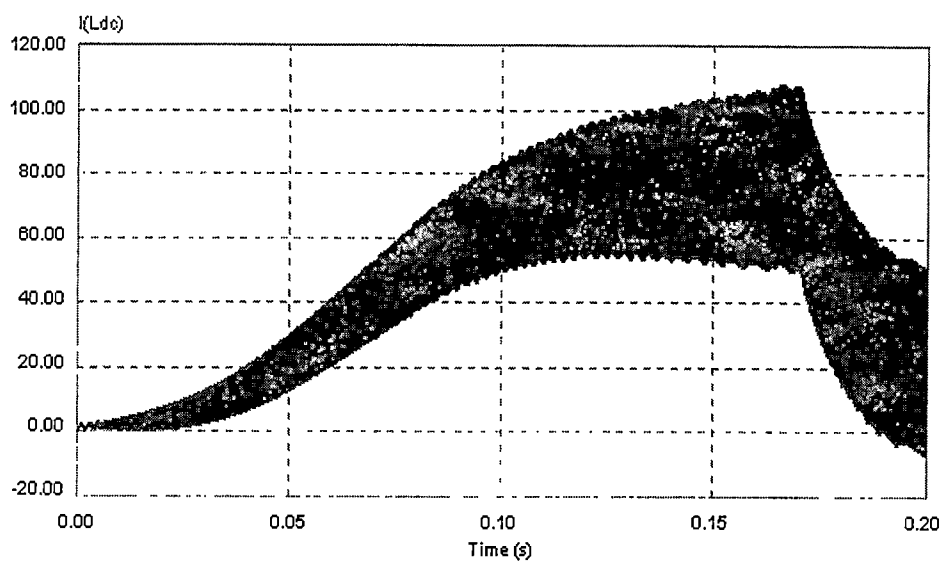
The simulation conditions are as follows.

$v_{in} = 12$ V, $D = 50\%$, $f_s = 20$ kHz, $L_{dc} = 5\mu\text{H}$, $L_s = 0.3024\mu\text{H}$, $C1 = C2 = C3 = C4 = 10$ mF, $C_o = 225$ mF, $R = 7.1918$ ohms.

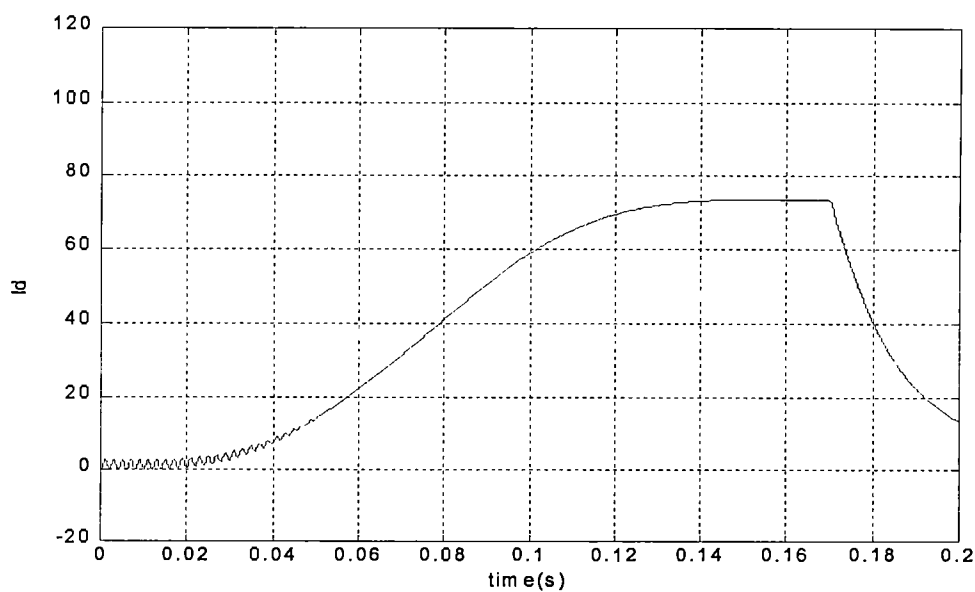
Similarly, the waveforms of i_l , v_{l2} (or $v_1 + v_2$), and v_{34} (or $v_3 + v_4$) of average model and detailed circuit model are compared in Fig. 4.20 (a)-(b) and Fig. 4.21 (a)-(b), respectively. Compared to the open-loop converter system, the start-up process of closed-loop is much faster with acceptable start-up current and over damped output voltage. It takes less than 200 ms from start-up of the process to steady state.

IV. 5 Summary

Although the commercial software package PSIM can be used to simulate the cycle-by-cycle performance of the proposed circuit, it is very inconvenient and time-consuming to study the large-signal long-term dynamic operation without the average

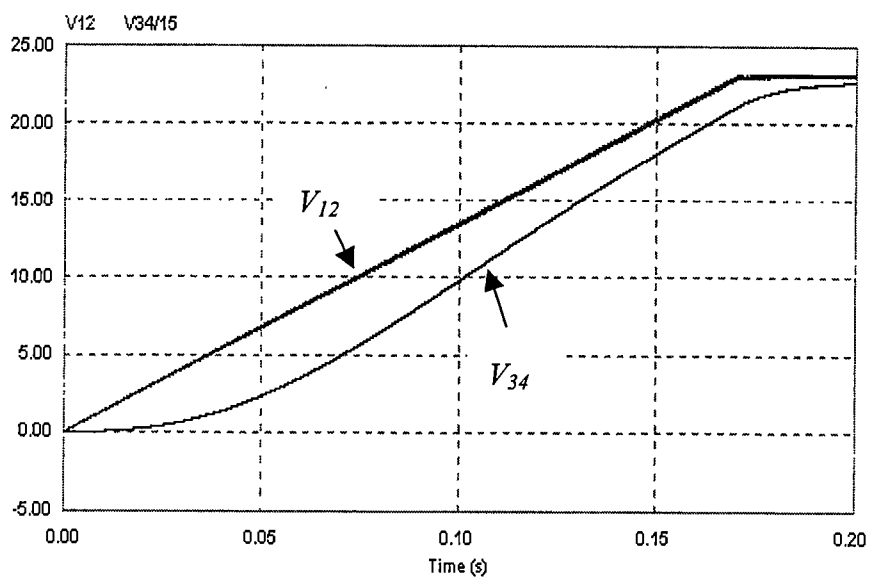


(a) i_l of detailed circuit simulation

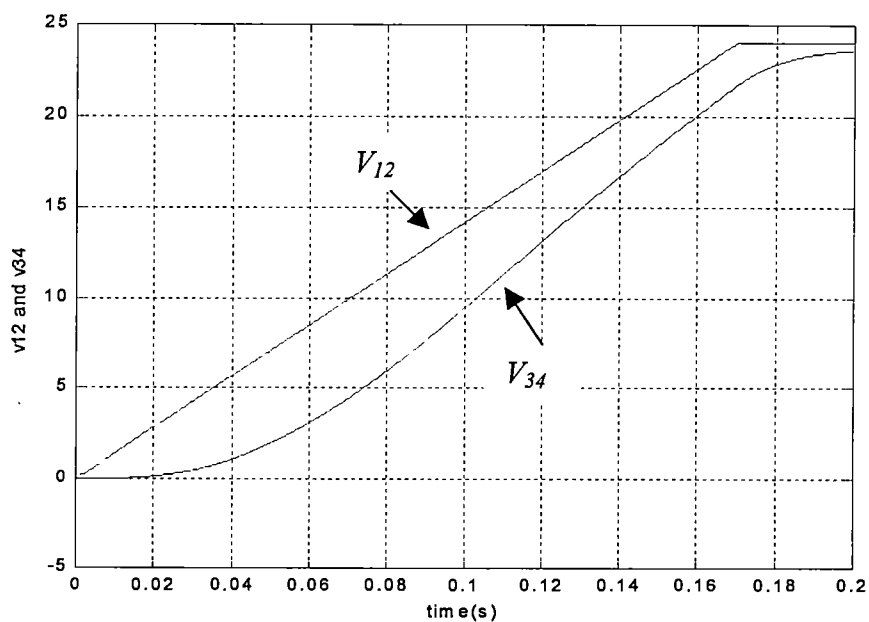


(b) i_l of average model

Fig. 4.20 The simulation and comparison of i_l in example 3



(a) v_{12} and v_{34} of detailed circuit simulation



(b) v_{12} and v_{34} of average model

Fig. 4.21 The simulation and comparison of v_{12} and v_{34} in example 3

model. In addition, an average model is very helpful for control system analysis and design of converters. However, it is difficult to build the averaged model using the ordinary state-space averaging technique for the isolated dc-dc converter proposed in this dissertation.

In this chapter, a fifth-order nonlinear large-signal mathematical model and its simplified third-order averaged model are derived for the dual half-bridge circuits with a transformer. With this technique, all the variables whose dc averages are not zero can be investigated with simulation, and the features of ac variables such as the peak value of i_r can also be obtained. Considering the diode rectification mode as a special case of the proposed converter, the corresponding simulation block diagram can be developed similarly.

The proposed technique can be applied to the class of dc-dc converters with a high-frequency isolation transformer. For example, it can be applied to obtain the average model of dual-active full-bridge bi-directional dc-dc converter, as shown in Fig. 2.9. After the average model is derived, the small signal model can be calculated and used to design the control system in the following chapter.

CHAPTER V

CONTROL SYSTEM DESIGN

V. 1 Introduction

In the anticipated application, the following dynamic and steady state system performance is required.

1. Start-up time is required to be less than 200 ms with load engaged when the bus voltage is higher than 255 V.
2. The isolated, bi-directional dc-dc converter is rated at 1.6 kW continuous power.

Based on the above specifications, the control system design is divided into a small signal control problem and a start-up control problem. The small signal control problem is to regulate the output voltage against a small dc input voltage disturbance and/or load variation. The corresponding controller is designed based on the small signal model. However, the small signal model can not be used for start-up control because, derived by linearizing the average model around an operating point, the small signal model is only valid for a limited operating range about this point but start-up is a large signal dynamic process. In addition, unlike the small signal control, which takes care of input voltage disturbances and load variation, the main objective of the start-up control problem is to limit the inrush current and to quickly build up the output voltage. Therefore, the start-up controller and small signal controller are

designed separately in this chapter, and a smooth transition between the two controllers is required.

The structure of this chapter is organized as follows. In section one, the small signal controller is first described. In section two, the start-up controller is discussed. Finally, one approach of implementing the overall control system including the start-up controller and small signal controller is presented in section three.

V. 2 Small Signal Control

First, small signal analysis is performed to generate the required transfer functions. The root locus of the control-to-output transfer function provides the information on the poles, zeros and the gain of the uncompensated converter. According to this information, a classical controller is designed.

V. 2.1 Small Signal Model Derivation

The large-signal, nonlinear mathematical model of the proposed circuit is derived in chapter IV. The goal of this section is to develop a small signal model. To account for the variation of the resistive load, an additional current source is placed across the nominal load. Then using the perturbation technique, a small-signal averaged model linearized around the nominal operating point is obtained.

The circuit topology of the proposed converter is redrawn in Fig. 5.1 for convenience.

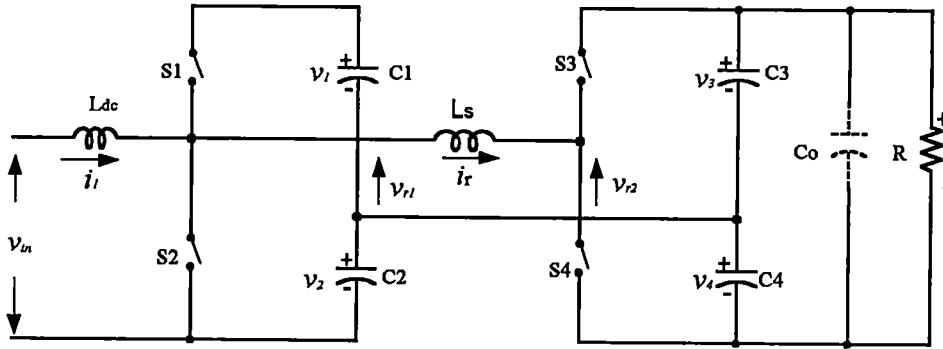


Fig. 5.1 Primary referred equivalent circuit

The averaged model developed in chapter IV is expressed as follows:

$$\begin{cases} \dot{i}_1 = \frac{-1}{2L_{dc}} v_{12} + \frac{1}{L_{dc}} v_{in} \\ \dot{v}_{12} = \frac{1}{C_p} i_1 - \frac{2\phi_1(\pi - \phi_1)}{C_p T_s \omega \cdot 2\omega L_s} v_{34} \\ \dot{v}_{34} = \frac{2\phi_1(\pi - \phi_1)}{(C_s + 2C_o) T_s \omega \cdot 2\omega L_s} v_{12} - \frac{2}{(C_s + 2C_o) R} v_{34} \end{cases} \quad (5-1)$$

where $v_{12}=v_1+v_2$, $v_{34}=v_3+v_4$, $C_p = C1 = C2$, $C_s = C3 = C4$.

To account for the variation of the load, a current source $i_o = \Delta G \cdot v_o$ is placed across the nominal load conductance G , as demonstrated in Fig. 5.2.

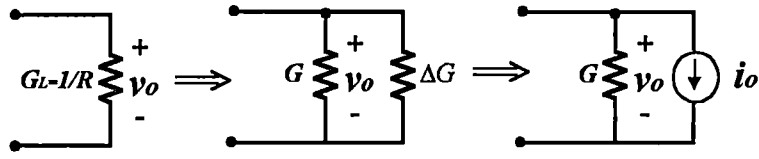


Fig. 5.2 Variation of load R

The averaged model, taking account of the variation in load, is then developed.

$$\begin{cases} \dot{i}_1 = \frac{-1}{2L_{dc}} v_{12} + \frac{1}{L_{dc}} v_{in} \\ \dot{v}_{12} = \frac{1}{C_p} i_1 - \frac{2\phi_1(\pi - \phi_1)}{C_p T_s \omega \cdot 2\omega L_s} v_{34} \\ \dot{v}_{34} = \frac{2\phi_1(\pi - \phi_1)}{(C_s + 2C_o) T_s \omega \cdot 2\omega L_s} v_{12} - \frac{2}{(C_s + 2C_o) R} v_{34} - \frac{2}{C_s + 2C_o} i_o \end{cases} \quad (5-2)$$

The nominal operating point can be obtained by setting the following values in equation (5-2).

$$\dot{i}_1 = 0, \quad \dot{v}_{12} = 0, \quad \dot{v}_{34} = 0, \quad i_o = 0, \quad v_{in} = V_{in}, \quad \phi_1 = \Phi_1$$

A calculation shows that

$$\begin{cases} I_1 = \frac{V_{in}^2 \cdot \Phi_1^2 \cdot (\pi - \Phi_1)^2 \cdot R}{T_s^2 \cdot L_s^2 \cdot \omega^4} \\ V_{12} = 2V_{in} \\ V_{34} = \frac{V_{in} \cdot \Phi_1 \cdot (\pi - \Phi_1) \cdot R}{2\pi\omega L_s} \end{cases} \quad (5-3)$$

Substituting V_{in} , I_1 , and V_{34} into the power equations $P_{in} = V_{in} \cdot I_1$, and $P_{out} = \frac{v_{34}^2}{R}$, it is easy to calculate the transfer power of nominal operating point as follows.

$$P_{in} = P_{out} = \frac{V_{in}^2 \cdot \Phi_1^2 \cdot (\pi - \Phi_1)^2 \cdot R}{(2\pi\omega L_s)^2} \quad (5-4)$$

The equation (5-4) can be also represented as

$$P_{in} = P_{out} = \frac{V_{in} \cdot \Phi_1 \cdot (\pi - \Phi_1) \cdot V_{34}}{\pi\omega L_s} \quad (5-5)$$

which is the same as the equation derived by circuit analysis in Chapter 3.

In order to obtain the linearized state equation, equation (5-2) is given a small perturbation around the nominal operating point; then the higher order nonlinear terms are neglected. We introduce small perturbations

$$v_{in} = V_{in} + \tilde{v}_{in}, \quad \phi_1 = \Phi_1 + \tilde{\phi}_1, \quad i_o = 0 + \tilde{i}_o, \quad v_{12} = V_{12} + \tilde{v}_{12}, \quad i_1 = I_1 + \tilde{i}_1, \quad v_{34} = V_{34} + \tilde{v}_{34}$$

and assume that

$$|\tilde{v}_{in}| \ll V_{in}, \quad |\tilde{\phi}_1| \ll \Phi_1, \quad |\tilde{v}_{12}| \ll V_{12}, \quad |\tilde{v}_{34}| \ll V_{34}, \quad |\tilde{i}_1| \ll I_1$$

The uppercase letters denote the dc quantities at the nominal operating point and the lowercase letters hatted with “~” denote small perturbed ac signals around the

operating point. Choosing $(\tilde{i}_1, \tilde{v}_{12}, \tilde{v}_{34})$ as state variables, $(\tilde{v}_{in}, \tilde{\phi}_1, \tilde{i}_o)$ as control inputs and $\tilde{v}_{34}$ as controlled output, the linearized state equations can be derived as follows:

$$\begin{cases} \begin{bmatrix} \dot{\tilde{i}}_1 \\ \dot{\tilde{v}}_{12} \\ \dot{\tilde{v}}_{34} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L_{dc}} & 0 \\ \frac{1}{C_p} & 0 & -\frac{2\Phi_1(\pi-\Phi_1)}{Con1} \\ 0 & \frac{2\Phi_1(\pi-\Phi_1)}{Con3} & -\frac{2}{C_t R} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_{12} \\ \tilde{v}_{34} \end{bmatrix} + \begin{bmatrix} \frac{1}{Ldc} & 0 & 0 \\ 0 & -\frac{2(\pi-2\Phi_1) \cdot V_{34}}{Con1} & 0 \\ 0 & \frac{2(\pi-2\Phi_1) \cdot 2V_{in}}{Con3} & -\frac{2}{C_t} \end{bmatrix} \begin{bmatrix} \tilde{v}_{in} \\ \tilde{\phi}_1 \\ \tilde{i}_o \end{bmatrix} \\ \tilde{v}_o = [0 \ 0 \ 1] [\tilde{i}_1 \ \tilde{v}_{12} \ \tilde{v}_{34}]^T \end{cases} \quad (5-6)$$

where $Con1 = C_p T_s \omega \cdot 2\omega L_s$, $Con3 = C_t T_s \omega \cdot 2\omega L_s$, $C_t = C_s + 2C_o$

Consequently, the linearized small signal model of the proposed circuit is shown in Fig. 5.3.

V. 2.2 Transfer Function Derivation

Equation (5-6) can also be expressed as:

$$\begin{aligned} \dot{\tilde{x}} &= A\tilde{x} + B\tilde{u} \\ y &= C\tilde{x} \end{aligned} \quad (5-7)$$

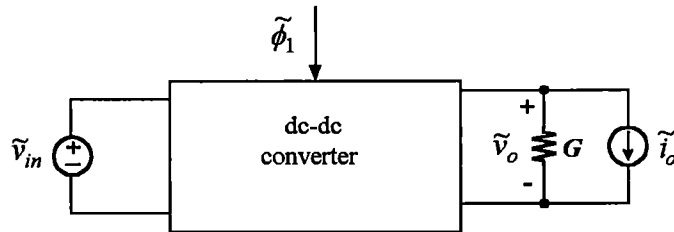


Fig. 5.3 Linearized small signal model

The representations of matrices A, B, and C are as follows.

$$A = \begin{bmatrix} 0 & -\frac{1}{2L_{dc}} & 0 \\ \frac{1}{C_p} & 0 & \frac{-2\Phi_1(\pi - \Phi_1)}{Con1} \\ 0 & \frac{2\Phi_1(\pi - \Phi_1)}{Con3} & \frac{-2}{C_t R} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_{dc}} & 0 & 0 \\ 0 & \frac{-2(\pi - 2\Phi_1) \cdot V_{34}}{Con1} & 0 \\ 0 & \frac{2(\pi - 2\Phi_1) \cdot 2V_{in}}{Con3} & \frac{-2}{C_t} \end{bmatrix}$$

$$C = [0 \quad 0 \quad 1]$$

where $Con1 = C_p T_s \omega \cdot 2\omega L_s$, $Con3 = C_t T_s \omega \cdot 2\omega L_s$, $C_t = C_s + 2C_o$, and

$$V_{34} = \frac{V_{in} \cdot \Phi_1 \cdot (\pi - \Phi_1) \cdot R}{2\pi\omega L_s}.$$

The transfer function matrix from input vector $\tilde{u}$ to output $\tilde{y}$ can be obtained.

$$\begin{aligned} \tilde{v}_o(s) &= C(sI - A)^{-1} B \tilde{u}(s) \\ &= T_1(s) \tilde{v}_{in}(s) + T_2(s) \tilde{\phi}_1(s) + T_3(s) \tilde{i}_o(s) \end{aligned} \quad (5-8)$$

The nominal operating point of dc-dc converter is selected as:

$$P_o = 1.6 \text{ kW}, \quad V_{in} = 12 \text{ V}, \quad \Phi_1 = 0.16\pi, \quad R = 0.36\Omega$$

The other parameters are fixed at:

$$L_{dc} = 5 \text{ } \mu\text{H}, \quad L_s = 0.3024 \text{ } \mu\text{H}, \quad C_p = C_s = 10 \text{ mF}, \quad C_o = 169 \text{ mF}, \quad f_s = 20 \text{ kHz}$$

Substituting the above parameters into matrices A, B, and C, transfer functions

$T_1(s)$, $T_2(s)$ and $T_3(s)$ can be calculated based on equation (5-8) as follows.

$$T_1(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \frac{0.31928480 \times 10^9}{s^3 + 15.964s^2 + 0.10008869 \times 10^8 s + 0.159642401 \times 10^9}$$

$$T_2(s) = \frac{\tilde{v}_o(s)}{\tilde{\phi}_1(s)} = \frac{617.048s^2 - 0.342804 \times 10^6 s + 0.6170484580 \times 10^{10}}{s^3 + 15.964s^2 + 0.10008869 \times 10^8 s + 0.159642401 \times 10^9}$$

$$T_3(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_o(s)} = \frac{-15.964s^2 - 0.159642401 \times 10^9}{s^3 + 15.964s^2 + 0.10008869 \times 10^8 s + 0.159642401 \times 10^9}$$

The block diagram of open loop system for the proposed dc-dc converter is shown in Fig. 5. 4.

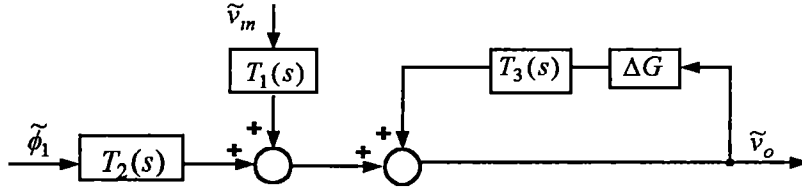


Fig. 5.4 Block diagram of dc-dc converter open loop system

V. 2.3 Small Signal Controller Design

The transfer functions shown above are used to design the controller to allow the converter to meet load regulation and transient response specifications, especially the control-to-output transfer function $T_2(s)$. The root locus plot of $T_2(s)$ is shown in Fig 5.5. The zeros and poles are as follows.

$$z1 = 277.8 + 3150.1i, \quad z2 = 277.8 - 3150.1i$$

$$p1 = -15.95, \quad p2 = -0.007 + 3163.7i, \quad p3 = -0.007 - 3163.7i$$

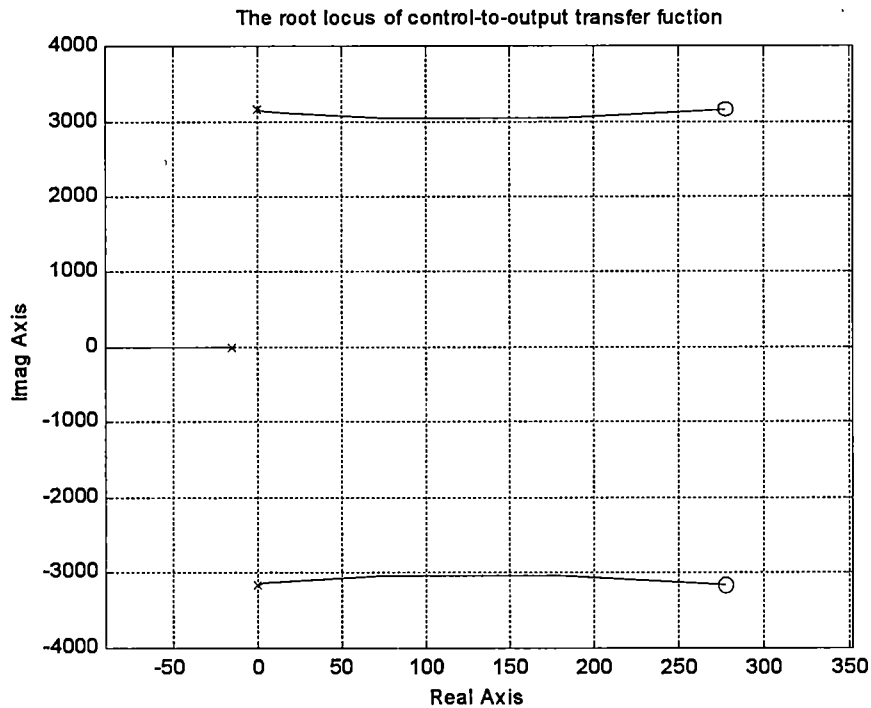


Fig. 5.5 Root locus plot of $T_2(s)$

The transfer function has two zeros in the right plane and two poles very close to the $j\omega$ -axis. A calculation and simulation found that a small gain bigger than 0.08 will make the system unstable.

By trial and error, a controller is obtained as:

$$K_c(s) = \frac{K(s + 0.008 + 3160i)(s + 0.008 - 3160i)}{(s + 1000)(s + 2000)}$$

The root locus of the compensated system is shown in Fig. 5.6.

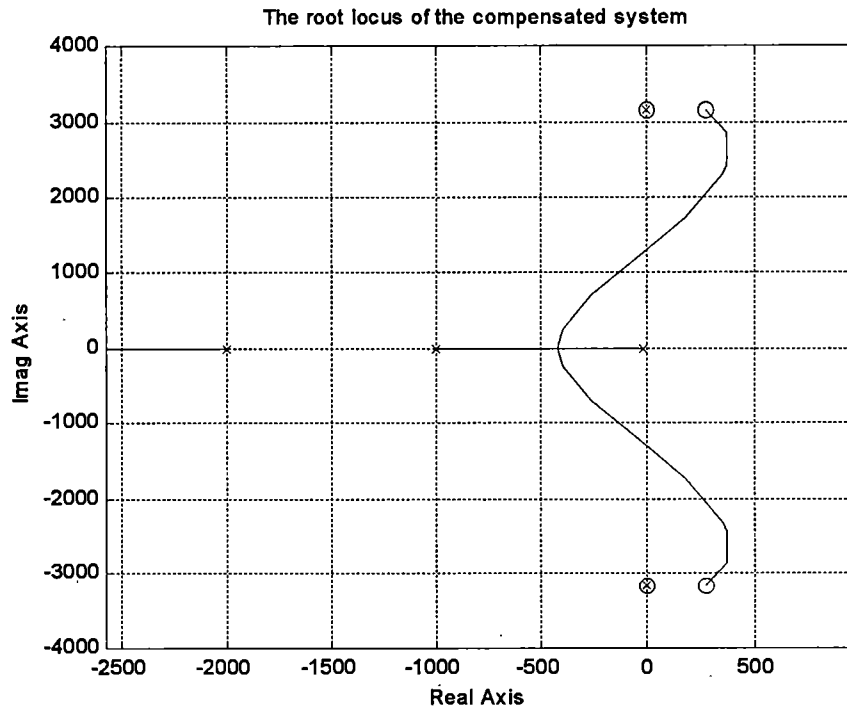


Fig. 5.6 The root locus of the compensated system

The two zeros of the controller cancel the effect of two nearly pure imaginary poles of the uncompensated system. The two poles of the controller ensure that the root locus does not go into the right plane with a small gain, thus making the system more stable. The system transient response is mainly decided by the pair of poles. If K is selected as 0.44, the poles are calculated as follows.

$$p1 = -160 + 947.5112i, \quad p2 = -160 - 947.5112i$$

The block diagram of the control system is shown schematically in Fig. 5.7. To estimate the system performance, a Matlab/Simulink control system model is established in Fig. 5.8. The simulation results are shown in Fig. 5.9 to Fig. 5.11.

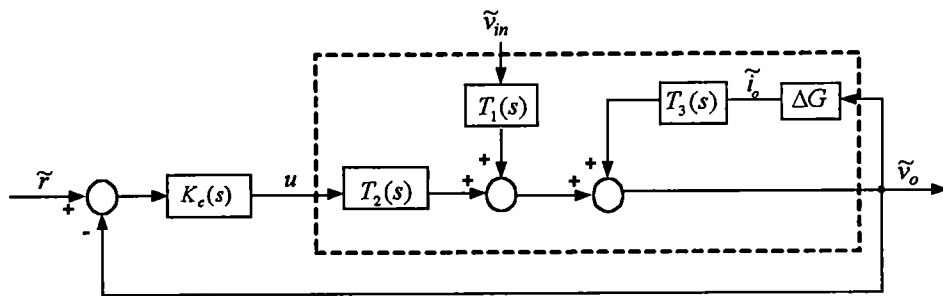


Fig. 5.7 Closed-loop model of small signal control system

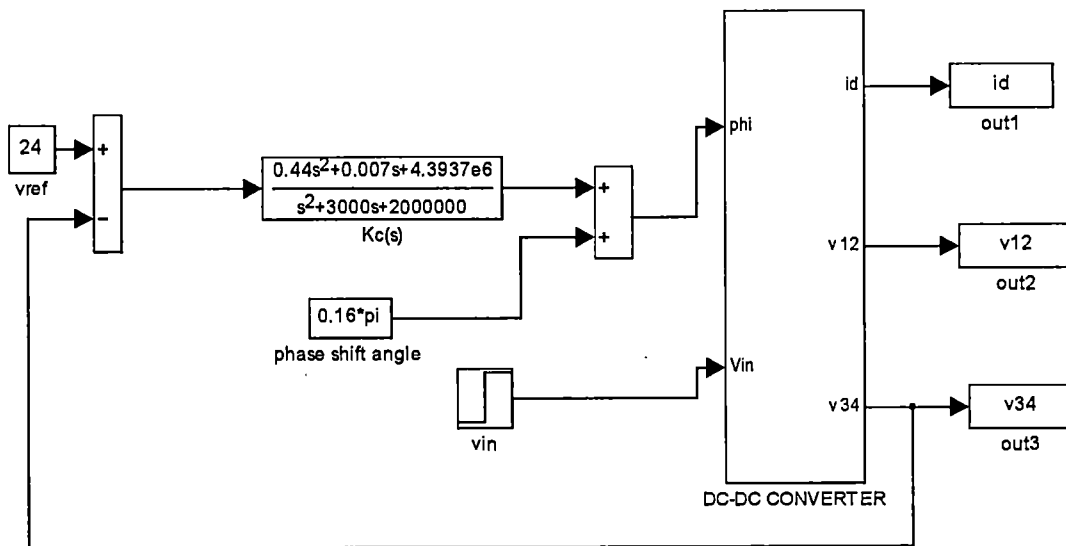
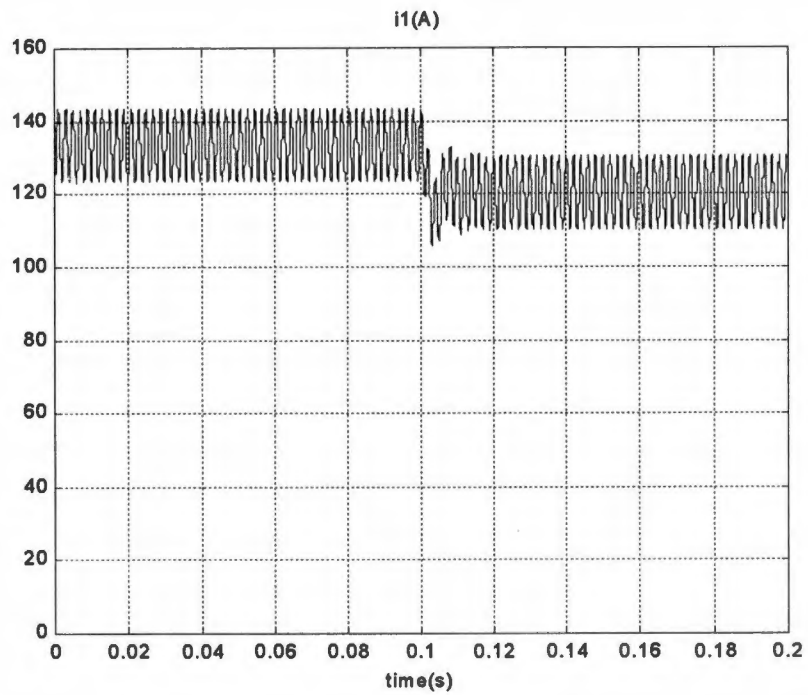
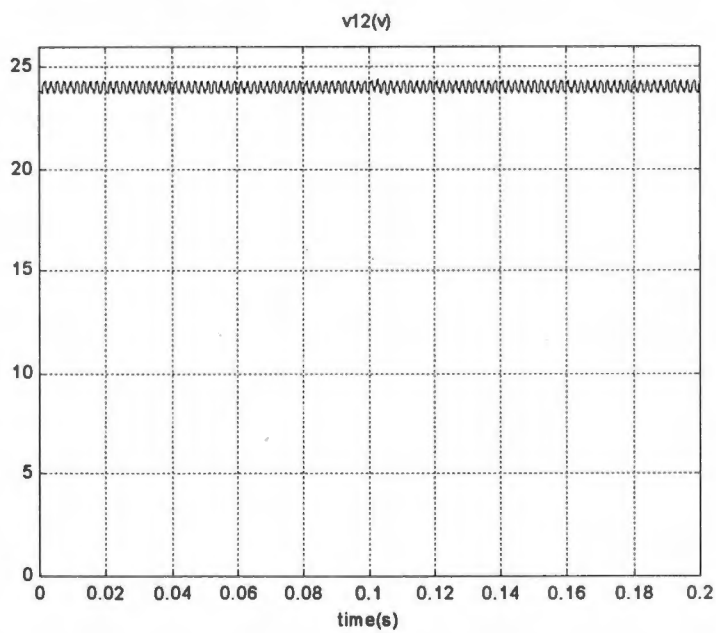


Fig. 5.8 Matlab/Simulink model of small signal control system

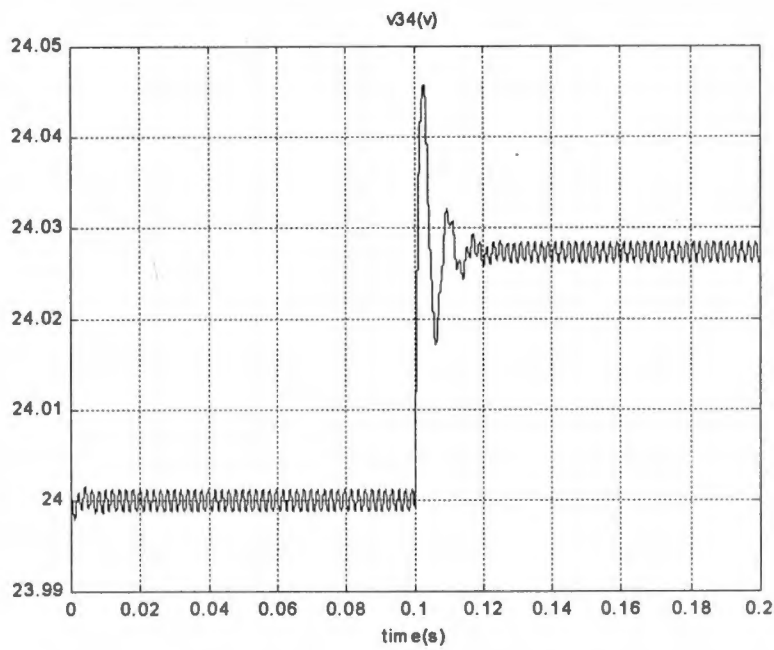


(a) i_1 response of load step change (from 0.36 ohm to 0.4 ohm)



(b) v_{12} response of load step change (from 0.36 ohm to 0.4 ohm)

Fig. 5.9 System response of load step change from 0.36 ohm to 0.4 ohm



(c) v_{34} response of load step change (from 0.36 ohm to 0.4 ohm)

Fig. 5.9 System response of load step change from 0.36 ohm to 0.4 ohm (continued)

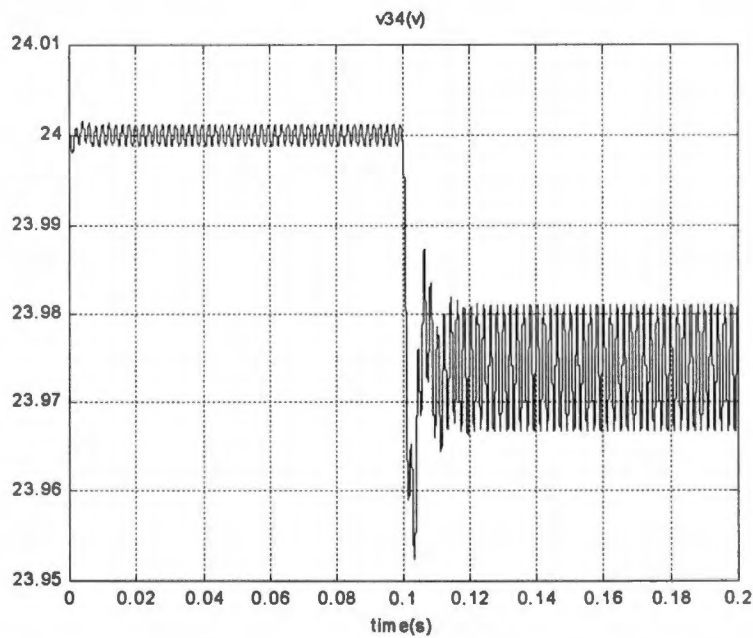


Fig. 5.10 Output response of input voltage step change from 12 V to 11 V

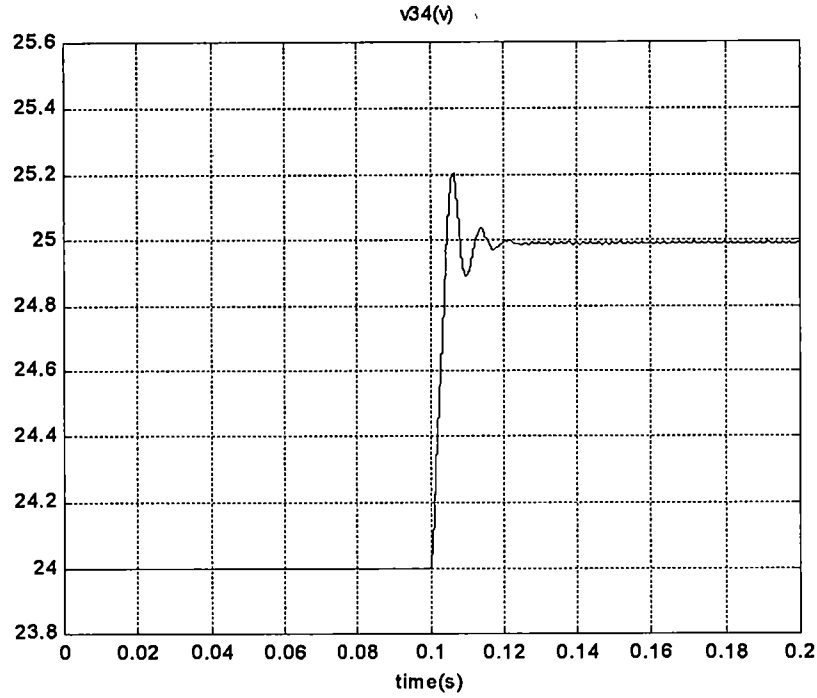


Fig. 5.11 Output response when reference voltage step change from 24 V to 25 V

The nominal operating point of simulation model is selected as:

$$P_o = 1.6 \text{ kW}, \quad V_{in} = 12 \text{ V}, \quad \Phi_1 = 0.16\pi, \quad R = 0.36 \Omega$$

The other simulation parameters are as follows.

$$L_{dc} = 5 \text{ } \mu\text{H}, \quad L_s = 0.3024 \text{ } \mu\text{H}, \quad C_p = C_s = 10 \text{ mF}, \quad C_o = 169 \text{ mF}, \quad f_s = 20 \text{ kHz}$$

Fig. 5.9 plots the system performance when the load changes from 0.36 ohm to 0.4 ohm. The reference voltage is 24 V. The input current i_l decreases because less power is required at heavier load if the same output voltage is required. v_{l2} , the voltage across $C1$ and $C2$, is unchanged because it depends on the battery voltage v_{in} , which

equals to 12 volts and does not change in this case. The output voltage v_{34} can be regarded as almost unchanged.

Fig. 5.10 shows the output performance when the battery voltage v_{in} changes from 12 V to 11 V and the reference voltage remains at 24 volts with the load unchanged. v_{12} decreases from 24 volts to 22 volts (which is not shown in the figure), and v_{34} drops less than 0.03 V.

Fig. 5.11 shows the dynamic response to a change in the reference voltage. When the reference voltage changes from 24 volts to 25 volts, the output voltage follows the reference command in a short time with a small overshoot. The overshoot and response time is mainly decided by the pair of poles of the compensated system, which are derived earlier.

V. 2.4 Summary

In this section, a small signal controller is designed for the proposed converter based on the root locus plots of the uncompensated system. The controller is designed to stabilize the system and regulate the output voltage around the nominal operating point. Load variation and changed battery voltage are treated as exogenous disturbances. The simulation results show that the classical controller provides a satisfactory transient response.

V. 3 Start up Scheme

In this section, the challenges of start-up are identified. A start-up control scheme is proposed with verification by simulation. Finally, two approaches of start-up implementation are presented and compared.

V. 3.1 Problem Specification

To facilitate the discussion in this section, the circuit schematic and the primary-referred equivalent circuit is redrawn in Fig. 5.12 (a)-(b).

During start-up, the power is flowing from the low voltage side to the high voltage side and the operating behavior of converter is similar to that of a boost converter. There is an inherent disadvantage for boost converters, namely the existence of an uncontrollable range when the output voltage is below the source voltage. This results in a large inrush current. Second, because of the large output

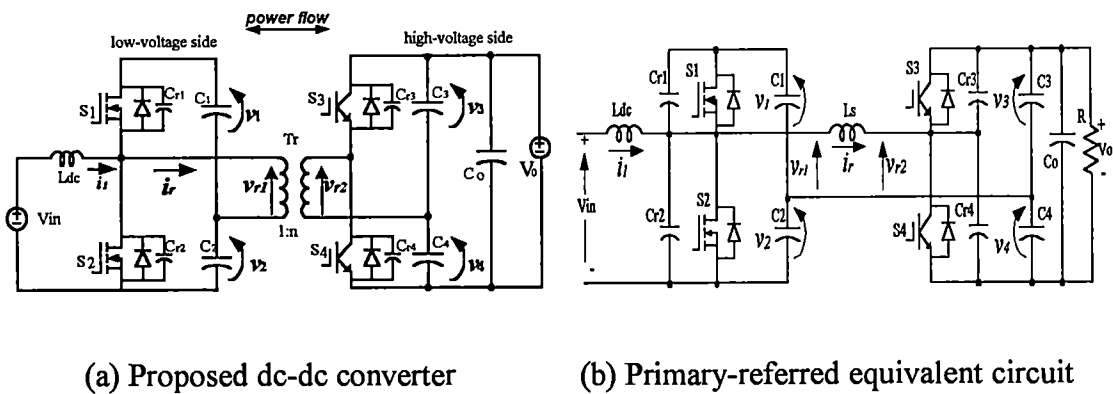


Fig. 5.12 The proposed circuit

capacitance C_o , the output voltages v_3 and v_4 will rise much more slowly compared to v_1 and v_2 . Accordingly, there is a big difference between v_{r1} and v_{r2} . Referred to Fig. 5.1. (b), this will cause a large current flowing through the transformer and low voltage side devices due to the small leakage inductance. Ultimately, the inductor and isolation transformer may be saturated, and components may fail. As a result, much higher ratings for the switches and components are required for safe start-up operation.

Another concern is the soft-switching operation of start-up. According to the soft-switching conditions derived earlier, zero voltage switching will not be guaranteed if the output voltages v_3 and v_4 can not follow v_1 and v_2 closely.

V. 3.2 Start-up control scheme

In order to solve the above problems, a basic idea is to have a ramp input voltage source and a closed loop system. The conceptual circuit schematic is demonstrated in Fig. 5.13. The block diagram of the closed loop system can be found in Fig. 4.19 in which the controller is a proportional gain. With a limited rising rate of v_{in} , the inrush current problem is avoided. In addition, v_3 and v_4 track v_1 and v_2 closely because of voltage feedback control, thereby maintaining soft switching. In addition, peak current ratings of devices are limited to reasonable values. The simulation waveforms of i_1 , v_{12} , v_{34} , peak value of i_r , and peak current stresses of devices are shown in Fig. 5.14 to Fig. 5.17.

To evaluate whether soft switching operation is maintained, the curves in Fig. 5.18 describe the following relationship.

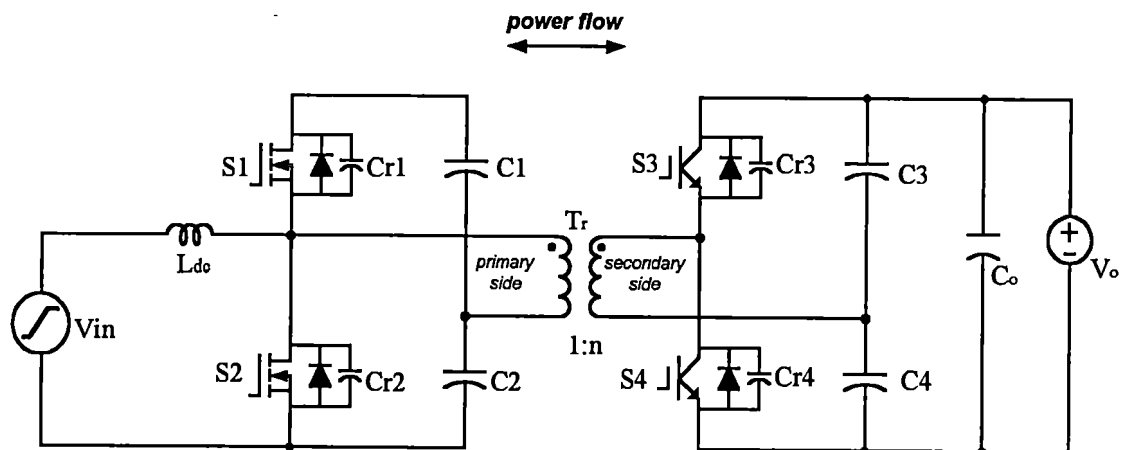


Fig. 5.13 The circuit schematic of a start-up control system with a ramp input voltage

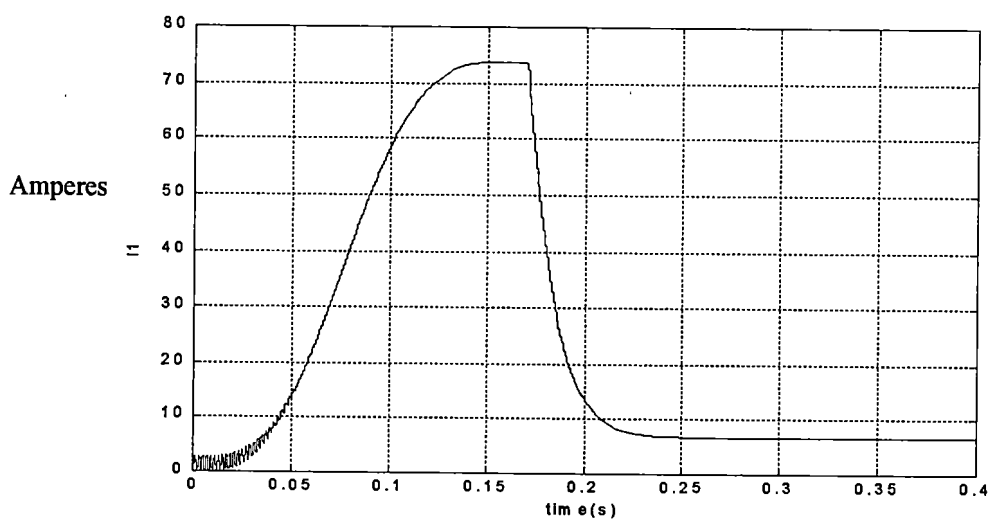


Fig. 5.14 i_l of a start-up control system with a ramp input voltage

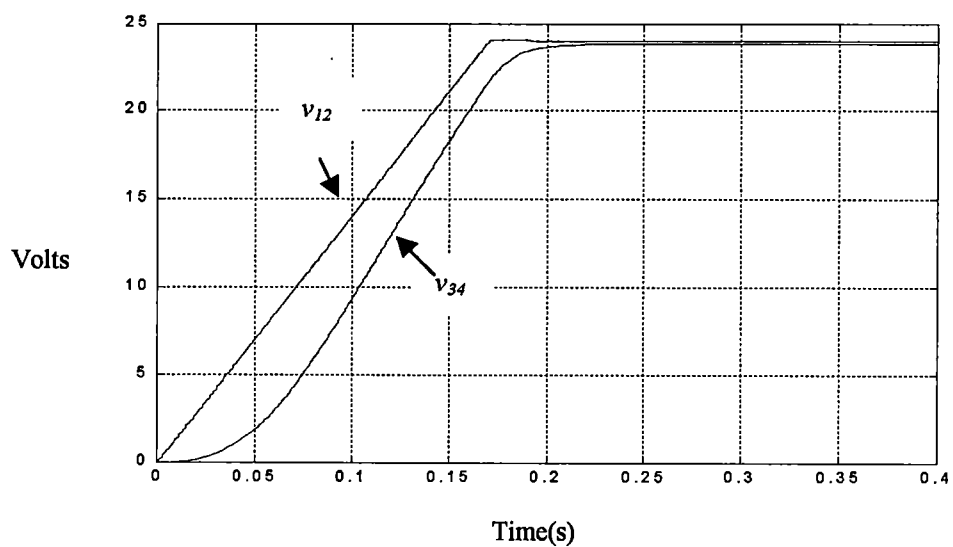


Fig. 5.15 v_{12} and v_{34} of a start-up control system with a ramp input voltage

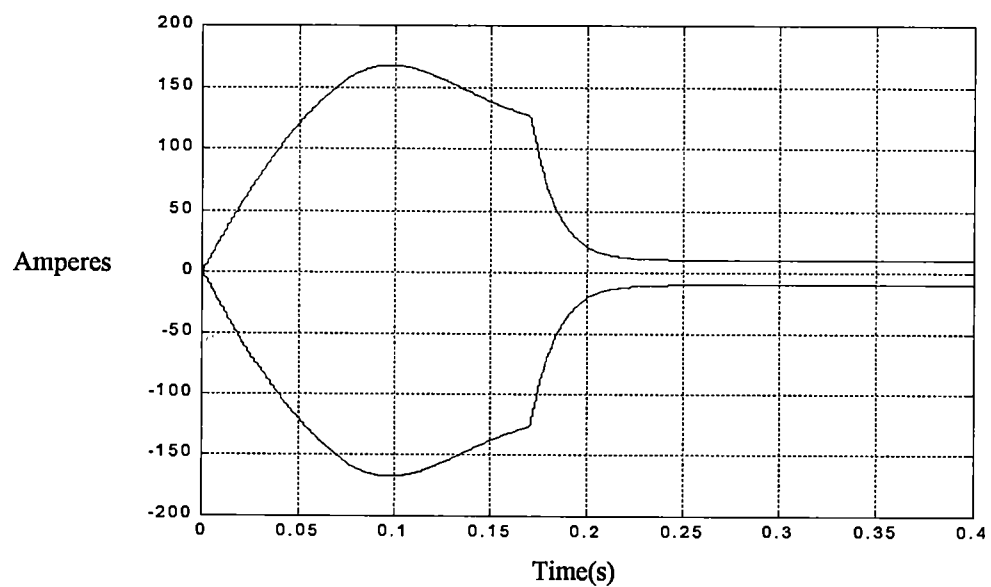


Fig. 5.16 The envelope of i_r of a start-up control system with a ramp input voltage

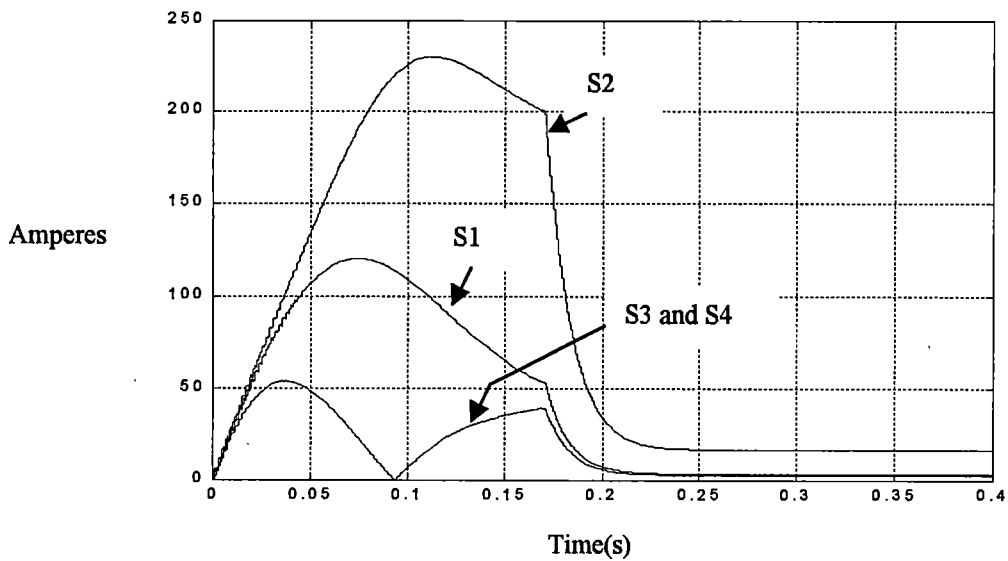


Fig. 5.17 Peak current stresses of devices of a start-up control system with a ramp-input voltage

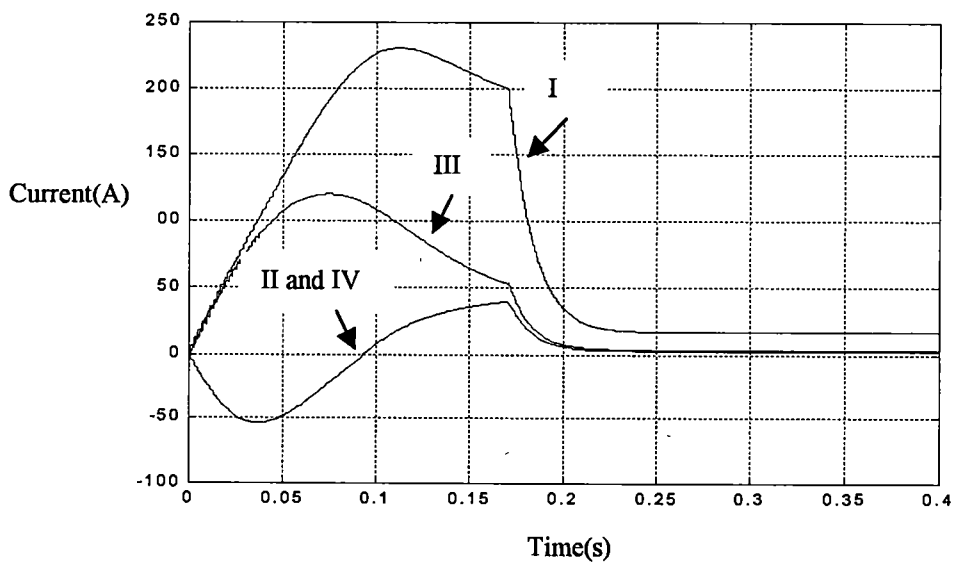


Fig. 5.18 Soft switching conditions of a start-up control system with a ramp-input voltage

$$\left\{ \begin{array}{ll} \text{curve} & I : i_1 - i_r(\phi_1) \\ \text{curve} & II : i_r(\phi_1) \\ \text{curve} & III : i_r(\pi) - i_1 \\ \text{curve} & IV : -i_{r1}(\pi + \phi_1) \end{array} \right.$$

According to the corresponding equation, if the curve is on the positive half plane, i.e., above the x-axis, then the soft-switching condition is satisfied. Fig. 5.18 shows that all the soft switching conditions are maintained except that those of S3 and S4 are not satisfied during a short time period from time zero to less than 0.1 s.

The simulation results verified that i_L , the average current of the input inductor, and the peak magnitude of i_r , the ac current of the isolation transformer, are limited to 80 A and 200 A, respectively. The start-up process is less than 0.2 s, which will meet the application requirements. The peak current stresses of the devices are kept in a reasonable range. The switching loss is not significantly high during start-up.

V. 3.3 Start-up implementation

Now the problem is how to implement the ramp-input voltage source. The two approaches are listed as follows.

V. 3.3.1 Start-up approach I

There are several approaches to implement the ramp voltage source. One of them is to put a buck converter as a charger circuit in front of dc-dc converter. The circuit schematic is shown in Fig. 5.19. The design values of the charger circuit are as

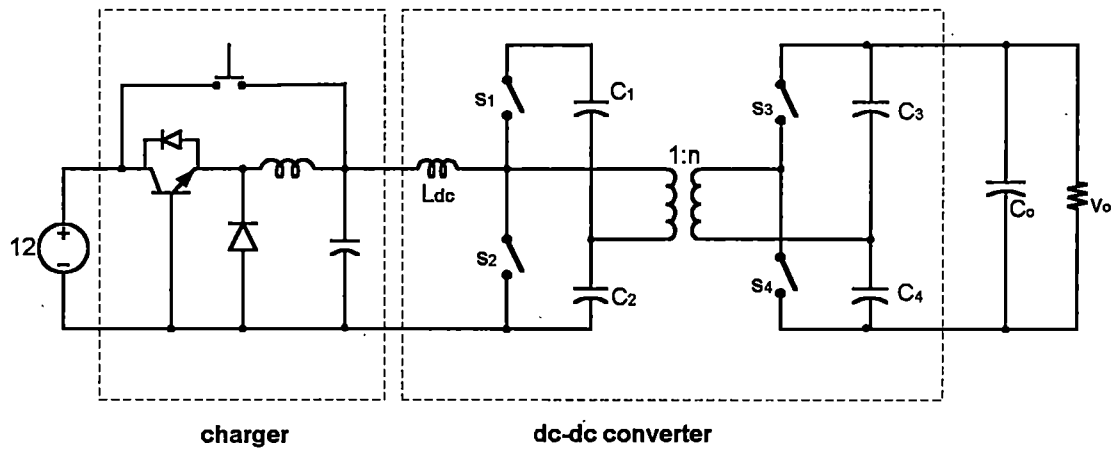


Fig. 5.19 Start-up approach I

follows: inductance is selected as $100 \mu H$ and capacitance is $1 mF$. Although the simulation results of start-up are very promising, the disadvantages include: extra devices and components are required to achieve soft start-up and the inductor and the capacitor in the charger circuit are large.

One improvement over this approach is to use L_{dc} , $C1$, and $C2$ instead of the extra inductor and capacitor, as shown in Fig. 5.20

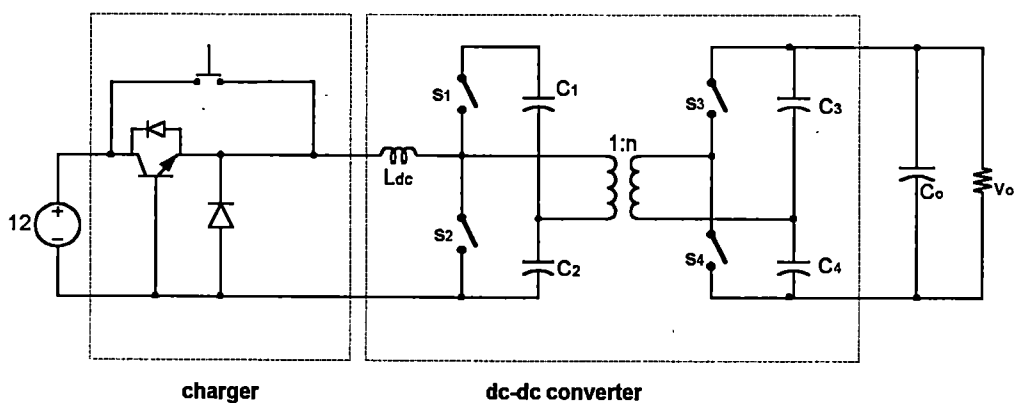


Fig. 5.20 One improvement version of approach I

In this case, only one device, one diode and one relay are required. The simulation results are shown from Fig. 5.21 to Fig. 5.23. The converter starts at the no load condition. The inrush current is less than 80 A, and the peak current of the isolation transformer is less than 150 A. v_3 and v_4 track v_1 and v_2 closely and the soft switching conditions are ensured. However, the current rating of this extra device must be at least 100 A.

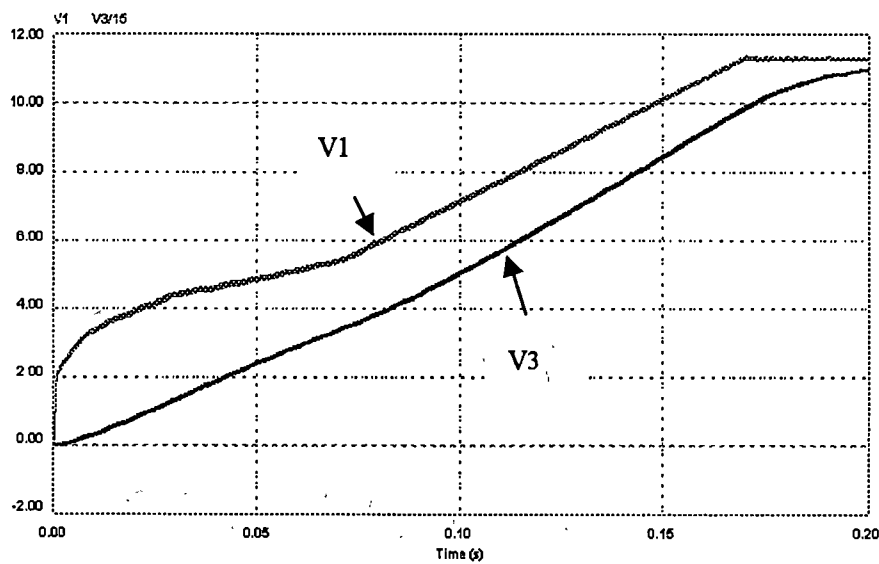


Fig. 5.21 v_1 and v_3 of improvement version of approach I

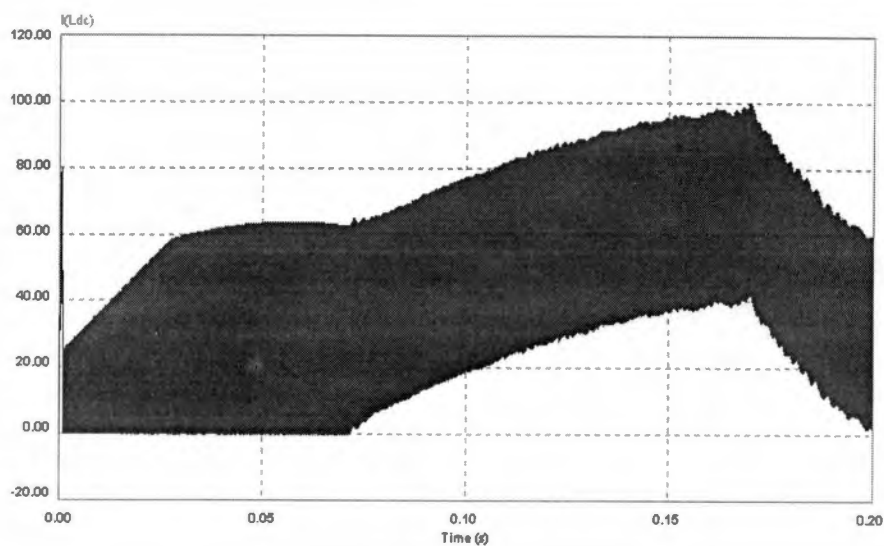


Fig. 5.22 i_l envelope of improvement version of approach I

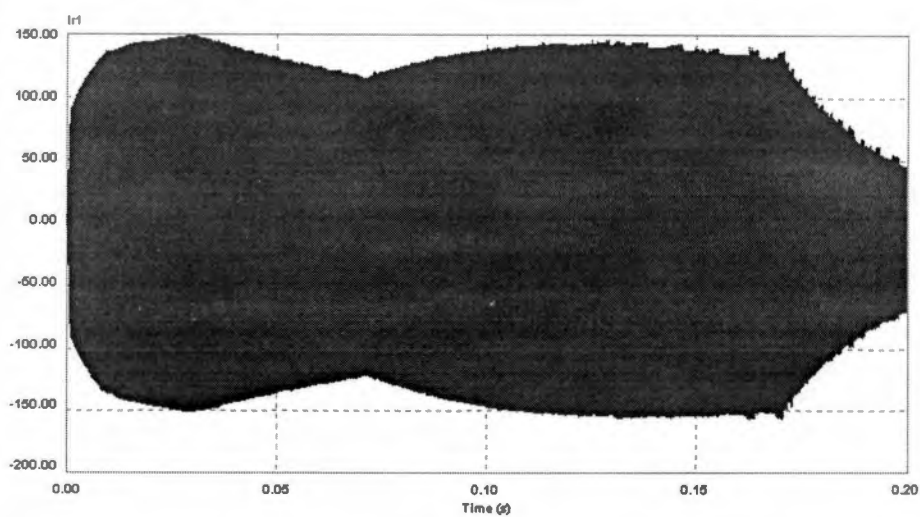


Fig. 5.23 i_r envelope of improvement version of approach I

V. 3.3.2 Start-up Approach II

Another approach is to add a small resistor to the power circuit and make use of the relay box available in the vehicle. The circuit diagram is shown in Fig. 5.24.

The simulated system performance is shown from Fig. 5.25 to Fig. 5. 27. At first, D1 and D3 are closed, and D2 is opened. A small resistance is added to the converter to limit the inrush current. At $t = 150$ ms, V_o is established at 260 V (to the secondary-side circuit), and D2 is closed to cut off the start-up resistance. After a short time delay, S1 is opened, and full load is applied.

Compared to the approach I, the inrush current has a spike of 200 A. In addition, the voltage v_{34} does not closely track v_{12} from the initiation of start up to 0.05 s, which means the soft switching will not be guaranteed during this short period. The start-up resistance also consumes extra power. However, the inrush current spike

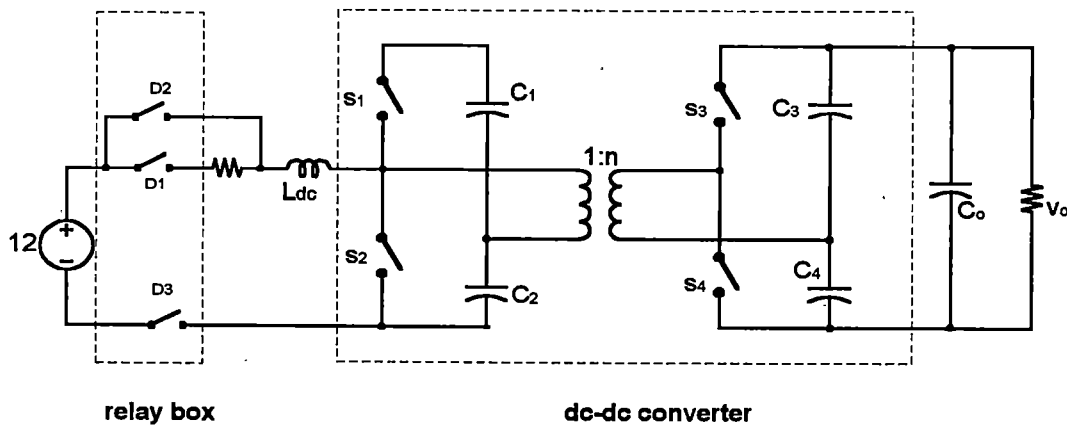


Fig. 5.24 Start-up approach II

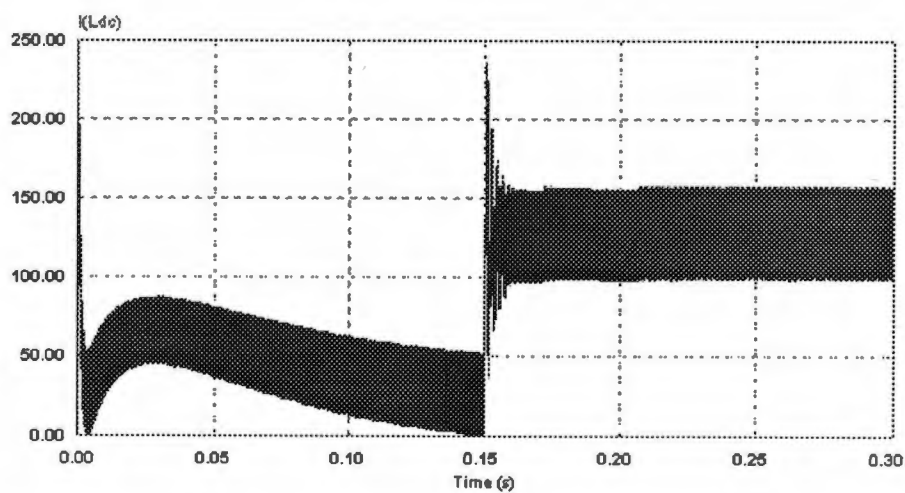


Fig. 5.25 i_L of start-up approach II

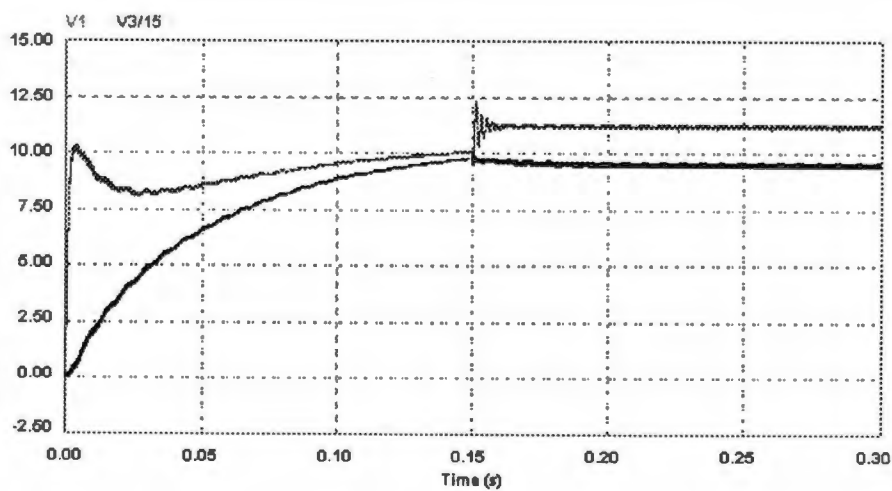


Fig. 5.26 v_1 and v_3 of start-up approach II

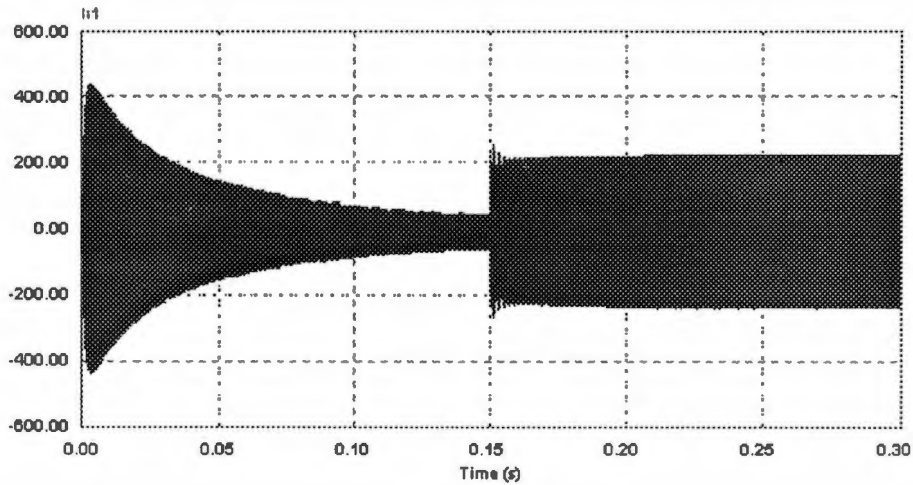


Fig. 5.27 i_L of start-up approach II

does not exceed 350 A, which is the designed current rating of inductor presented in the next chapter. The hard switching and additional small resistance decrease the system efficiency, but only for a very short time. In addition, no extra devices are necessary and the control algorithm is also simplified. As a result, approach II is a low cost and robust scheme and preferred to approach I.

V. 4 Control System Design

The block diagram of the overall control system is pictorially depicted in Fig. 5.28. The system includes a power converter stage, a relay box and controller. The design objective is to limit inrush current during start-up, regulate the output voltage of the nominal operating point to track the reference input voltage, despite a small

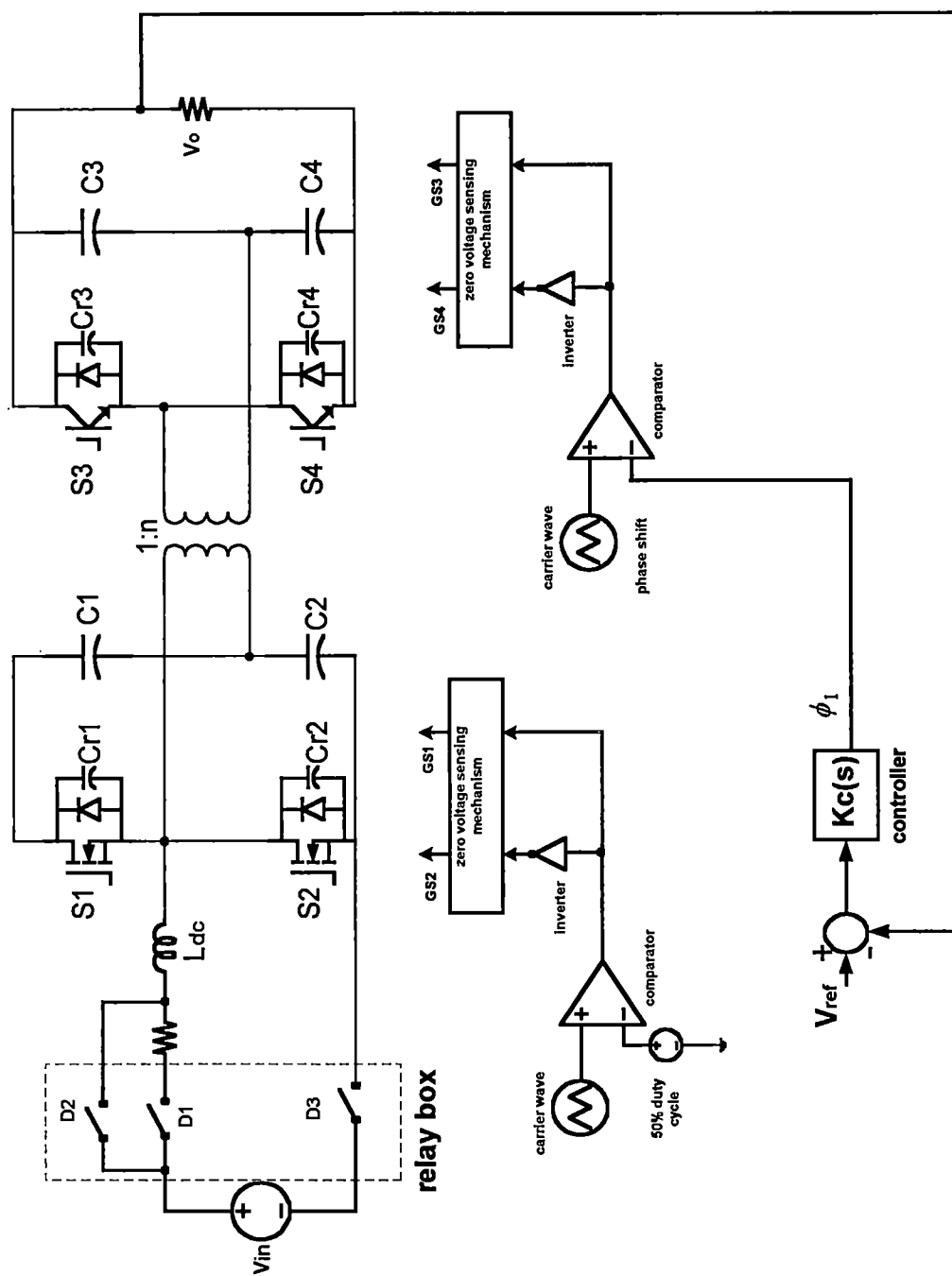


Fig. 5.28 The block diagram of control system for proposed converter

disturbance of load and battery voltage v_{in} .

According to the earlier discussion, a proportional gain controller as well as a relay box will allow the converter to have good performance at start-up. In addition, the controller:

$$k_c(s) = \frac{0.44s^2 + 0.007s + 4.39 \cdot 10^6}{s^2 + 3000s + 2 \cdot 10^6}$$

is selected to stabilize the system and to reduce the effect of exogenous disturbances around the nominal point.

Based on the status of the converter, the corresponding controller will be activated, which will add extra sensing and computing work to the control algorithms. In addition, if the transition between two controls is not smooth, the converter may become unstable or have large voltage and current spikes.

To avoid these problems, one approach is to use a small gain controller instead of two separate controllers. According to the transfer function analysis, a small gain controller also results in a stable system. In addition, it is more reliable and easier to implement. The trade-off is that the system performance is not optimal. Because of the inherent features of the proportional controller, the system has a steady state error in tracking the reference voltage. However, for the anticipated application, it is not necessary for the output voltage to follow the reference voltage with no or even a small error. Although the nominal output voltage is 288 volts, it can swing from 255

volts to 425 volts. Therefore, a limited steady state error will be acceptable. As a result, a small gain controller is a feasible solution.

The simulation model and results are shown in Fig. 5.29 to Fig. 5.31. At the beginning, $K_c = 0.08$, and the converter starts up at no load. The peak current of i_l is no higher than 200 A, and it lasts less than 0.01 s and is less than 50 A the rest of time. At $t = 150$ ms, v_o is built up to 260 volts ($(10+10) \cdot 13 = 260$ V), and the small resistance is cut off from the converter. Voltage v_l (and v_2) jumps to the battery voltage v_{in} because no voltage drops is present across the start-up resistance. With the no load condition, the input current i_l remains low and continues to decrease. At $t = 200$ ms, full load is added, and i_l increases to 170 A with a small overshoot to provide the full output power. Voltage v_l (and v_2) first drops 0.5 V and then recovers to the battery voltage, which is inherent with the boost-type converter. There is no obvious change to the output voltage. It increases smoothly to its final steady state.

Although the reference voltage is 24 V, the final steady state of the output voltage is 23 V. There is a steady state error. The actual value of output voltage is calculated on the secondary side as: $(11.5 \cdot 2) \cdot 13 = 299$ V, which meets the requirement of the application.

It is also interesting to examine the soft switching operation. Fig 5.32 plots the soft switching of all devices. The blue curve refers to device S2, the red one to S1, the curves of S3 and S4 are identical and are the green curve. S1 and S2 are soft switched during the whole process. From $t = 0$ to 200 ms, S3 and S4 are hard switching. After 200 ms, all the devices are soft switched.

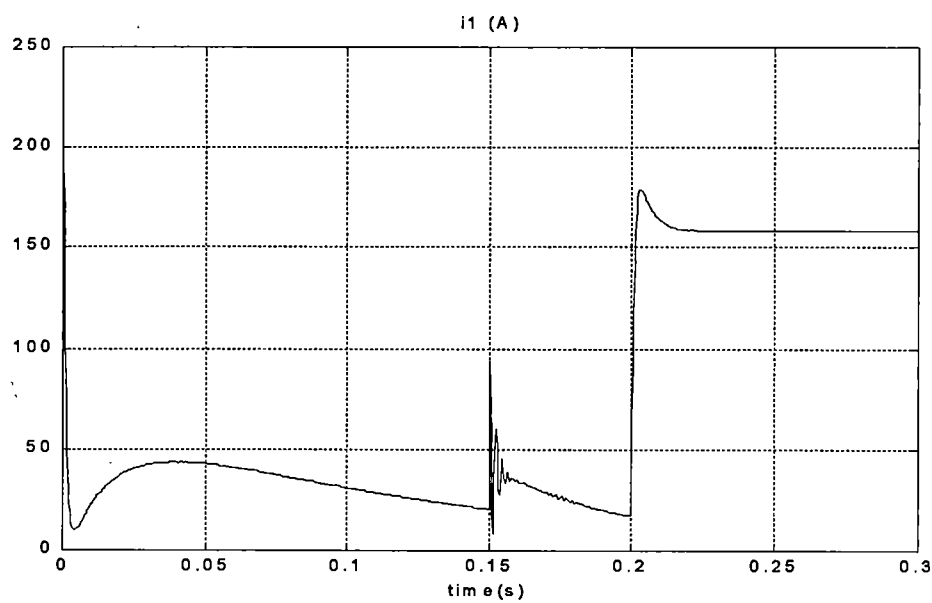


Fig. 5.30 i_1 of overall control system

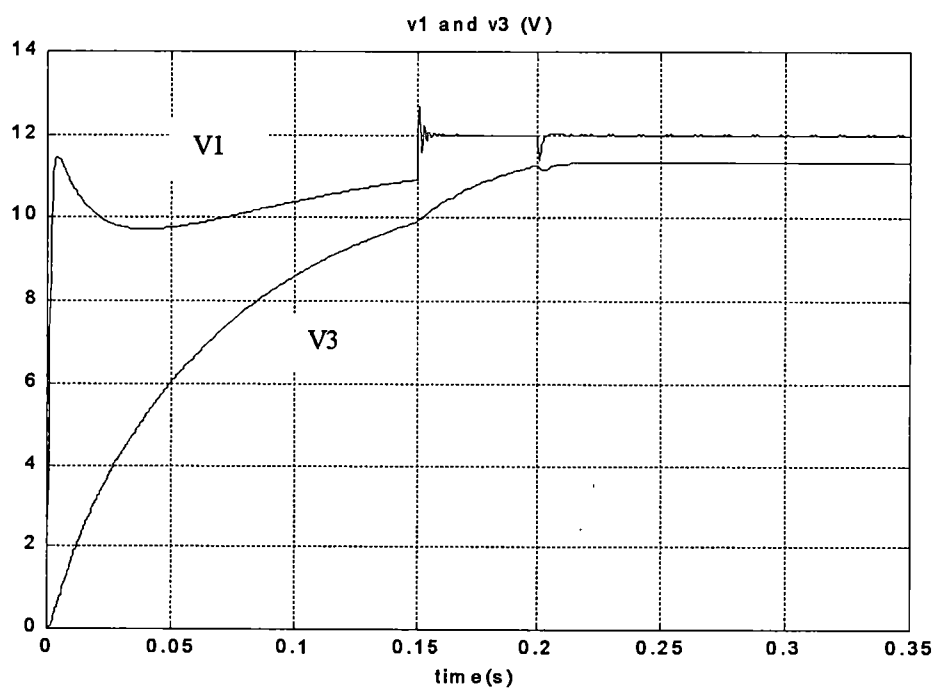


Fig. 5.31 v_1 and v_3 of overall control system

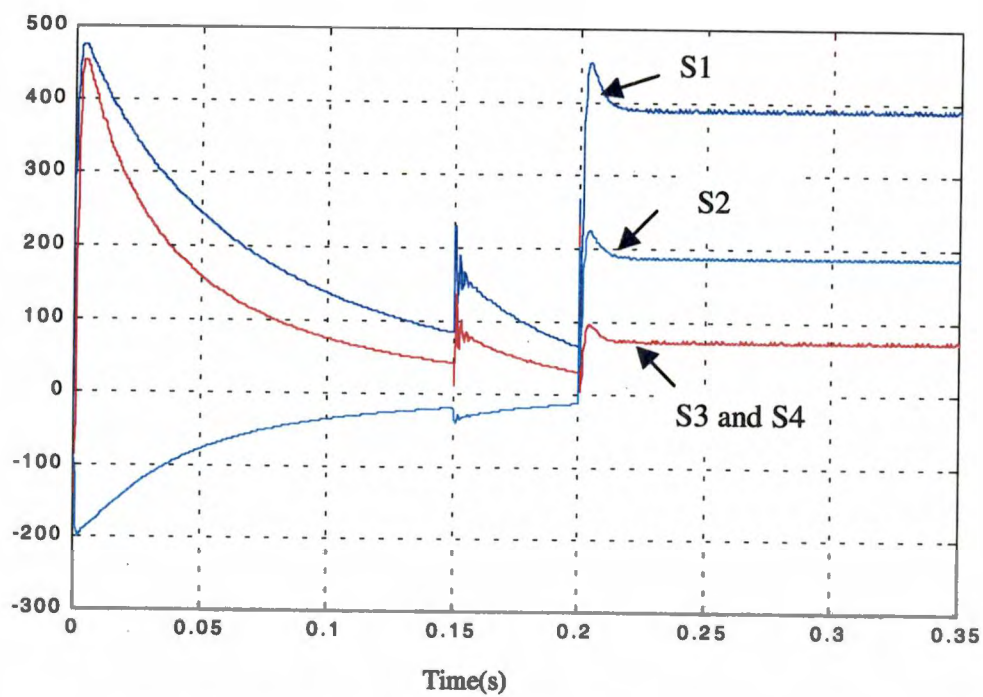


Fig. 5.32 Soft switching conditions of overall control system

CHAPTER VI

PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

VI. 1 Introduction

In order to validate the analysis and simulation results obtained in the previous chapters, a 1.6 kW dc-dc converter has been built and experimentally tested. The prototype is pictured in Fig. 6.1. In order to compare with the size of a previous prototype built using the circuit in Fig. 1.2, the power stage is laid on a 3/8" liquid cooled heatsink with overall size of about 7.5" width and 13.5" in length, and usable area of 7.25" by 8.5". The converter is operated at a switching frequency of 20 kHz. The input dc voltage is 12 V. The transformer turns ratio is 1:13.

A detailed description of the prototype design, hardware and software follows in the next three sections. Finally, the experimental verification is presented in section four.

VI. 2 Prototype Design

A design procedure to select the circuit components for the prototype is presented in this section. The procedure is based on the system requirements and the guidelines that were derived earlier in Chapter III. The design emphasis includes isolation transformer, inductor, capacitor, switches and layout considerations.

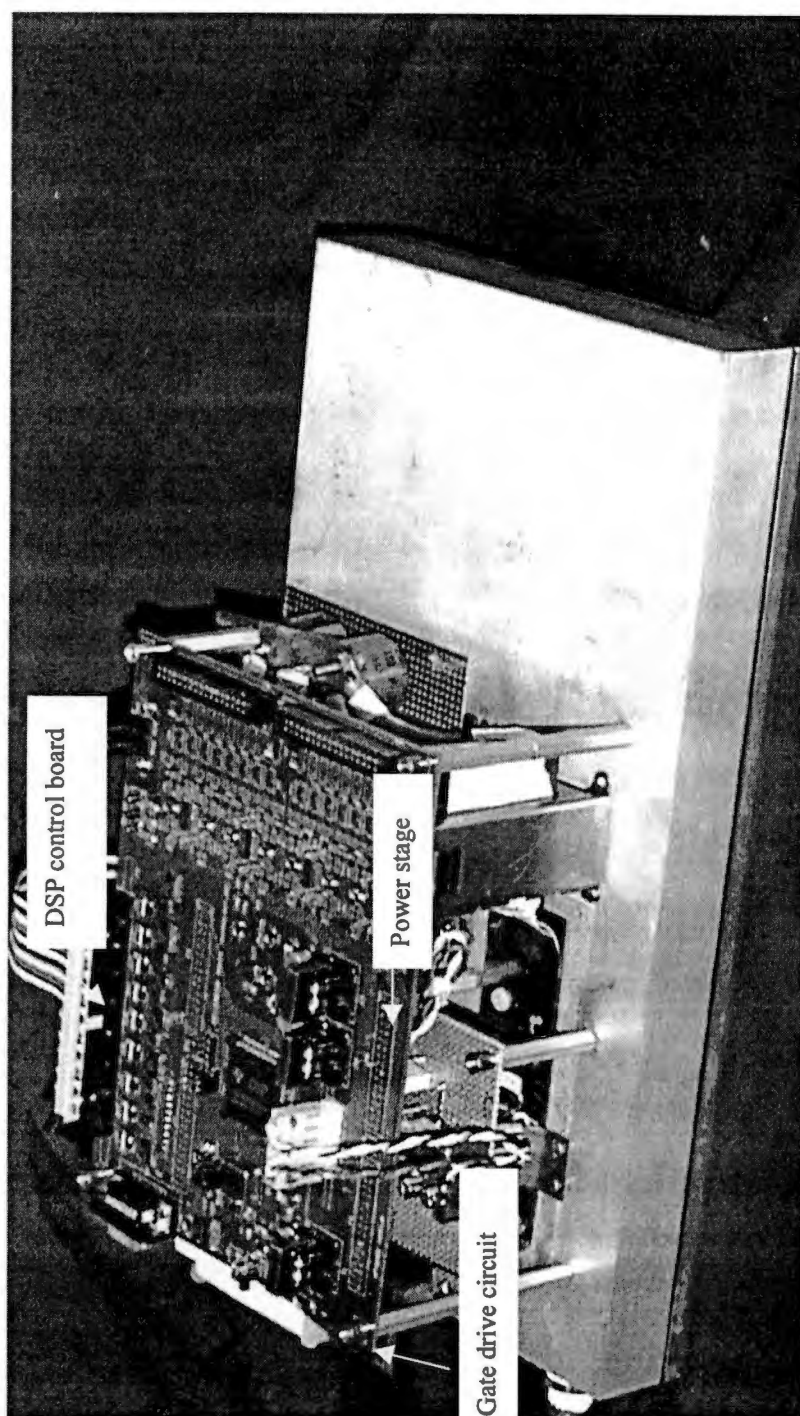


Fig. 6.1 Photo of the prototype

The specifications of the proposed dc-dc converter application are as follows:

- The nominal voltage at the low voltage side is 12 V, and can vary from 8 V to 16V during charging and discharging.
- The nominal high-side voltage is 288 V, with an operating range from 255 to 425V
- Maximum discharging power of the battery is 1.6 kW;
- Maximum charging power is 5 kW for a maximum duration of 20 seconds;
- Bus capacitance C_o is less than 2000 μF

The main design guidelines are reviewed here. If L_s is selected as $0.3024 \mu\text{H}$, then the maximum discharging power is calculated as follows:

$$P_o = \frac{\phi_1(\pi - \phi_1)v_{in}^2}{\omega\pi L_s} = 1.6 \text{ kW} \quad (6-1)$$

when $v_{in}=12 \text{ V}$, $f_s=20 \text{ kHz}$, $\phi_1=0.16\pi$.

The maximum charging power can be derived similarly.

$$P_o = \frac{\phi_1(\pi - \phi_1)v_{in}^2}{\omega\pi L_s} = 5.29 \text{ kW} \quad (6-2)$$

when $v_{in}=16 \text{ V}$, $f_s=20 \text{ kHz}$, $\phi_1=0.5\pi$.

The average current I_{d1} provided by the power supply can be found to be:

$$I_{d1} = \frac{P_o}{v_{in}} = 133.33 \text{ A} \quad (6-3)$$

when $v_{in}=12 \text{ V}$, $P_o=1.6 \text{ kW}$.

The initial states of current i_r such as $i_r(0), i_r(\phi_1), i_r(\phi_2), i_r(\phi_2 + \phi_1)$ are derived as follows.

$$\begin{cases} i_r(0) = \frac{v_3 - v_1}{2\omega L_S}(\pi - \phi_1) - \frac{v_1 + v_4}{2\omega L_S}\phi_1 = -158.7A \\ i_r(\phi_1) = \frac{v_1 + v_4}{2\omega L_S}\phi_1 + \frac{v_3 - v_1}{2\omega L_S}(\pi - \phi_1) = 158.7A \\ i_r(\pi) = -i_r(0) = 158.7A \\ i_r(\pi + \phi_1) = -i_r(\phi_1) = -158.7A \end{cases} \quad (6-4)$$

when $v_{in} = 12V, P_o = 1.6kW, \phi_I = 0.16\pi$.

The device peak current stresses at the above condition can be estimated based on the following equations:

$$\begin{cases} I_{s1_peak} = |i_r(\pi) - I_{d1}| = 292A \\ I_{s2_peak} = |-i_r(0) + I_{d1}| = 292A \\ I_{s3_peak} = |i_r(\phi_1)| = 158.7A \\ I_{s4_peak} = |i_r(\pi + \phi_1)| = 158.7A \end{cases} \quad (6-5)$$

VI. 2. 1 Isolation transformer T_r design

The transformer is very important for the converter design. The ideal transformer should be of high power density, high efficiency and high switching frequency. The issues of core material selection and winding geometry for the minimum core and copper losses at the highest possible switching frequency will be

considered. In addition, the designed leakage inductance is small enough to require the use of special low leakage transformer design techniques.

- Core material selection

The characteristics of a good core material include high operating frequency, low specific core loss and low power/weight ratio. With the selected switching frequency $f_s = 20$ kHz, compact magnetic component design becomes a key factor to satisfy the compact packaging requirement. Although the customized planar ferrite cores are preferred from this point of view, they are more expensive and occupy more footprint area. For this reason, the Philips E65 core was selected.

- Winding configuration

The designed winding structure and parameters are shown in Fig. 6.2. The sandwich structure is used to decrease the leakage inductance.

- Turns ratio selection

The main consideration of turns-ratio selection depends on the output voltage matching capability in the full regions of battery and load variations. It is required that $255\text{ V} \leq v_o \leq 425\text{ V}$, and $v_o = n \cdot k \cdot v_{ref}$. n is turns-ratio of transformer. v_{ref} is the

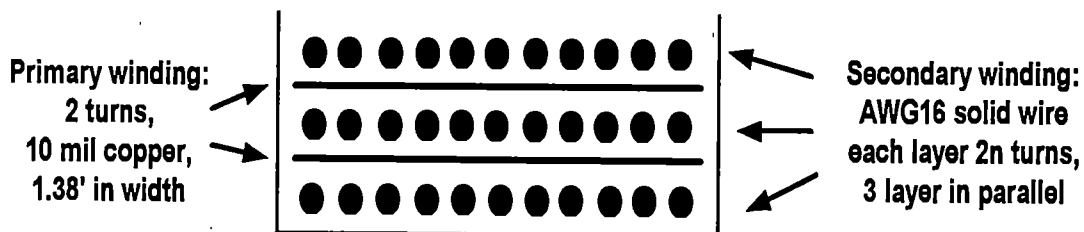


Fig. 6.2 Transformer winding structure

reference voltage. It is constant and selected in the range of 20V to 24V. k is a factor to represent the difference between the output and the command. It is close to 1. If n is selected as 13, k is 1, the range of v_o is calculated to be $260\text{ V} \leq v_o \leq 312\text{ V}$.

VI. 2. 2 Inductor L_{dc} selection

The simulation results show that when input inductance L_{dc} is selected as $5\text{ }\mu\text{H}$, the soft switching conditions over the whole operating range are achieved. The peak-peak ripple current of the rated current during typical discharging condition, i.e. $v_{in}=12\text{ V}$, $v_o=288\text{ V}$, $P_o=1.6\text{ kW}$ can be calculated as follows.

$$\Delta I = \frac{v_{in} \cdot \Delta t}{L_{dc}} = \frac{12 \cdot 25\mu\text{s}}{5\mu\text{H}} = 60\text{ A} \quad (6-6)$$

The worst case charging current under regenerative mode is $P_o/v_{in} = 5\text{ kW}/16\text{ V} = 312.5\text{ A}$. The inductor is then designed according to the peak current and the required inductance value. In addition, it should not saturate during maximum power peak charging.

A Metglas core with high saturation flux density, AMCC-25 from Allied Signal, is selected for the prototype. A seven-turn copper foil winding is used and the air gap is 2 mil on each side.

VI. 2. 3 Resonant capacitors $Cr1$, $Cr2$, $Cr3$, $Cr4$ selection

For low voltage side and high voltage side, the capacitance of the resonant capacitors are designed according to the required dv/dt range. Based on prior analysis

and simulation results, the resonant capacitor on low voltage side is selected as $0.5\mu\text{F}$ @100V. A low ESR and ESL capacitor is preferred. A polypropylene capacitor is not available at such a low voltage rating; therefore, a metal film capacitor V1H474JL $0.47\mu\text{F}$ @100V (surface mount) is selected.

The resonant capacitor on the high voltage side is selected as $0.033\mu\text{F}$ @600V. A polypropylene capacitor (orange drop) 716P33396K is selected.

Considering the typical working condition in the discharging mode, i.e. $v_{in}=12\text{ V}$, $v_o=288\text{ V}$, $P_o=1.6\text{ kW}$, the maximum and minimum dv/dt occurs at $\theta=0$ and $\theta=\pi$, respectively. The corresponding turn-off currents are calculated as:

$$\begin{aligned} I_{off}|_{\max, \theta=0} &= |i_r(0)| + |I_{d1}| = 292\text{ A} \\ I_{off}|_{\min, \theta=\pi} &= |i_r(\pi)| - |I_{d1}| = 25\text{ A} \end{aligned} \quad (6-7)$$

With snubber capacitors of $0.5\mu\text{F}$ and $I_{off} = Cr1 \frac{dv}{dt}$, dv/dt is derived accordingly as $50\text{ V} / \mu\text{s} \leq \frac{dv}{dt} \leq 584\text{ V} / \mu\text{s}$.

VI. 2. 4 DC capacitors $C1, C2, C3, C4$ selection

The voltage rating of $C1$ and $C2$ is decided by v_{in} , which can swing from 8~16V, so $C1 = C2 = 10,000\mu\text{F}$ @24V.

In the primary-referred equivalent circuit, the capacitance of $C3$ and $C4$ is selected as $10,000\mu\text{F}$. The voltage is equal to $\frac{1}{2} v_o$ and $v_o = 255\text{ V}$ to 425 V , so the

capacitors $C3$ and $C4 = 10000/n^2 = 59 \mu\text{F} @ 300 \text{ V}$ where $n=13$.

$C1, C2, C3, C4$ are electrolytic capacitors. The main concerns for selecting the capacitors are the ESR value, the ripple current capability, and the size. When $v_{in}=12 \text{ V}$, $v_o = 288 \text{ V}$, $P_o=1.6 \text{ kW}$, a large current will flow through $C1$ and $C2$, and a low ESR capacitor is preferred. To facilitate the circuit layout, higher density is also to be considered. Finally, UNITED CHEMI-CON's 747D103M025AY2A 10000 $\mu\text{F}@25\text{VDC}$, size D×L(mm) 35×48, ESR $7\pm30\%\text{m}\Omega$, Maximum Ripple Current 11.2 A(rms) at 20 kHz is selected for $C1$ and $C2$.

The capacitor of high voltage side are Sprague's 80D101P250JA5D 100 $\mu\text{F}@250\text{VDC}$. The high frequency capacitors of $C1$ and $C2$ are Sprague's polypropylene capacitor $10\mu\text{F}@100\text{V}$. The high frequency capacitors of $C3$ and $C4$ are $0.47\mu\text{F}@400\text{V}$ polypropylene capacitor 716P47494M.

VI. 2. 5 Low-voltage side switches

The low voltage and high current on the battery side, i.e. 8-16v, favors the selection of low voltage side switches to be MOSFETs. When $D=50\%$, the voltage across the switch is 2 times of v_{in} during steady state. From simulations, the overshoot voltage during transient is very small. Thus a 35V MOSFETs should satisfy the requirements. However, a 55 V device is selected to provide additional safety margin.

Analysis and simulation show that the peak current in steady state of the discharging (boost) mode is 291A. The current during start-up will be more than 300 A. The peak current in charging (buck) mode will be as high as 1000A when

regenerative power is 5 kW. Paralleling of the MOSFETs is required to handle this large current. Fortunately, the positive temperature coefficient nature of this on-resistance makes current sharing among the paralleled devices a minor concern.

Of greater concern is the on-resistance. Because of high current on the low voltage side, the conduction loss is significant. Therefore the on-resistance should be as small as possible. In addition, the on-resistance will increase with the temperature, and the operating temperature of the switches is much higher than 25°C. So the relationship between on resistance and temperature is also very important.

Another issue is the input capacitance (or gate charge). The rise time and fall time of switch is related to the input capacitance of device.

For the prototype design, the IR3205, TO-220 MOSFET was selected because of its fast speed, low on-resistance, low input capacitance and large current rating. The related parameters can be found in table 6.1.

VI. 2. 6 High-voltage side switches

Since the output voltage range is from 255 to 425V, the voltage ratings of the high side switches can be selected as 600V.

Table 6.1 . The datasheet of MOSFETs for low-voltage side switches

Maker	Model	V _{ds}	I _D	R _{ds} @25°C	R _{ds} @125°C	Input capacitance
IR	IRF3205	55V	110A	8 mΩ	12 mΩ	4000 pF

The peak current during steady state of discharging/boost mode is less than $200/13 = 15.38\text{A}$. However in start up, it is less than $400/13 = 30.77\text{A}$. In charging/buck mode it is $1000/13 = 77\text{A}$. For the prototype, a 600V/75A device is first selected. The half-bridge IGBT modules are favored because of the packaging design.

A Fuji 2MBI 75N-060 600V/75A IGBT half-bridge was selected because of its fast speed. The additional data can be found in table 6.2.

Table 6.2 IGBT half-bridge for high-voltage side switches

Maker	Model	V_{CES}	I_C	$V_{CE(sat)}$	Input cap.	Switching time(μsec)			
						t_{on}	t_r	t_{off}	t_f
Fuji	2MBI75N-060	600 V	75A	3V	4950pF	1.2	0.6	1.0	0.35

VI. 2. 7 Power stage layout consideration

Low leakage inductance packaging is important to minimize the conduction loss of the switches. The resonant capacitors will be as close as possible to the main devices to reduce the leakage inductance of the loop and avoid the ringing effect. The connection resistance will be decreased as much as possible; otherwise, the large current flowing through it will add extra loss to the system. The layout of the prototype is shown in Fig. 6.3.

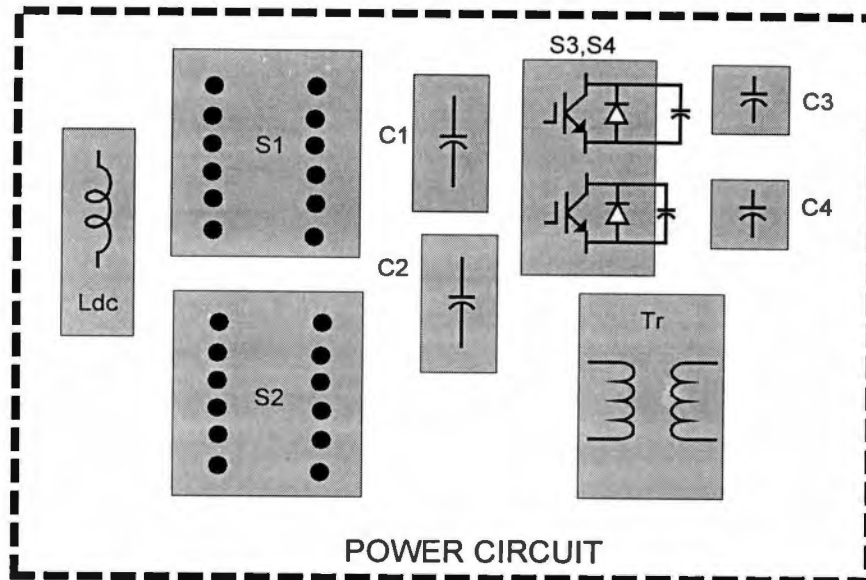


Fig. 6.3 Layout of the converter

VI. 3 Hardware Description

This section describes the three-layer hardware implementation of the converter, which is shown in Fig. 6.4. The power components are screwed to the horizontal base plate of the first layer. The second layer, the driver board, integrates the gate drive circuits for all the switches and the power supply circuits. The power supply circuits contain two flyback converters, with one providing +5 V and ± 15 V for DSP controller board and the other one offers +10 V and +20 V for gate driver circuits. The upper layer is a TI TMS320F240 DSP controller board.

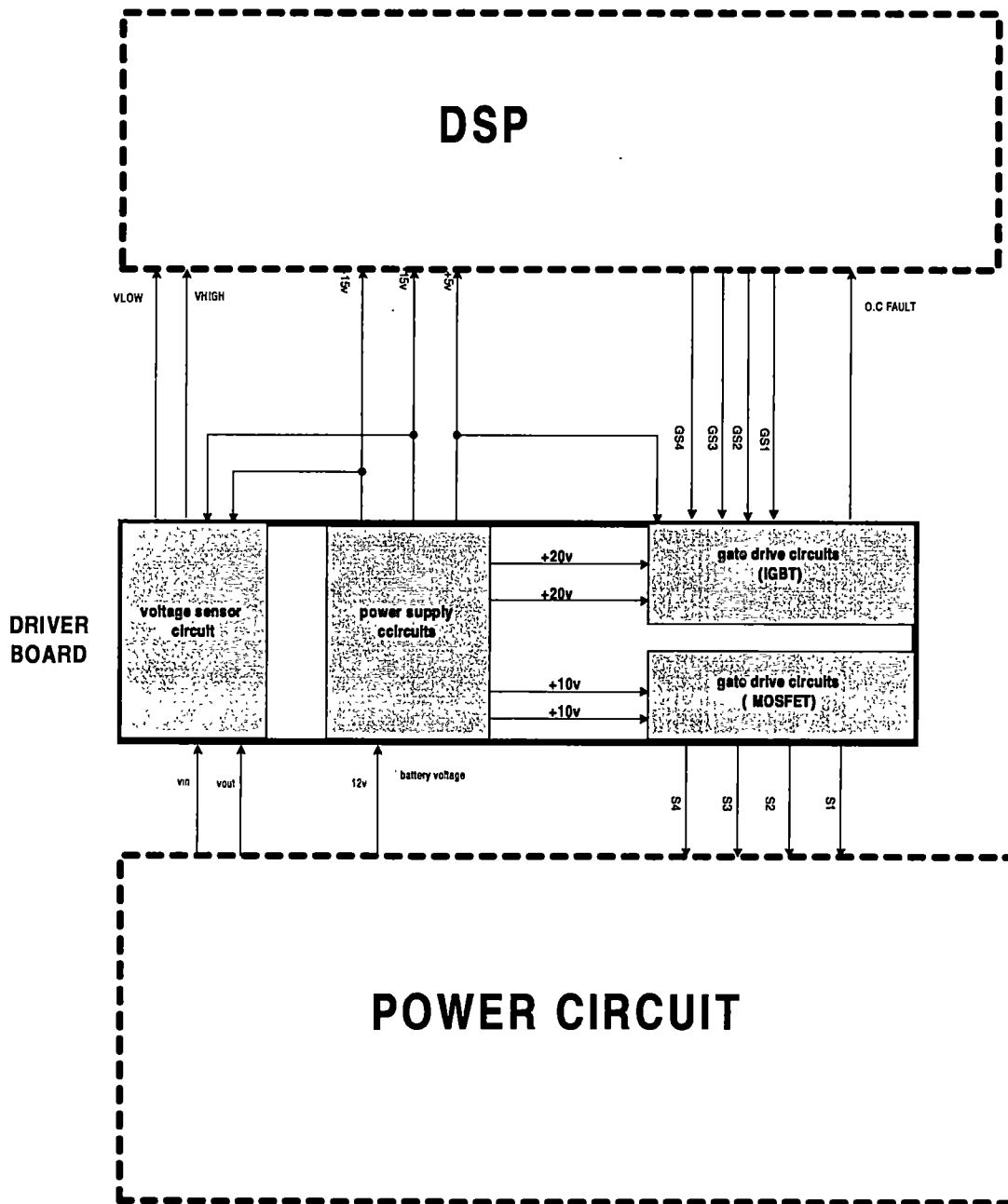


Fig. 6.4 The hardware implementation of converter system

A detailed description of the DSP interface circuit, voltage sensor circuit, gate driver circuits and power supply circuits is presented as follows. The circuit schematics can be found in Appendix B.

VI. 3. 1 The interface circuit of DSP

The hardware connection of the DSP controller board for the proposed converter system is shown in Fig. 6.5. The board is powered by a switch mode power supply circuit, which will be described later. The on board EMI filters provide good quality +5V and $\pm 15V$ for the DSP.

The gate signals of S1, S2, S3 and S4 are generated by the event manager of the 'C240 and output to the gate drive circuits.

The DSP board also receives an over current protection signal from the IGBT gate drive circuits by generating a PDPINT (power drive protection interrupt) signal. When the device pin PDPINT of DSP board is pulled low, all PWM signals will be in a high-impedance state and an interrupt request is generated to the DSP core. The PWM signals will stay low until the DSP is manually reset.

VI. 3. 2 Voltage sensing circuit

The DSP board provides up to 16 channels of analog interface circuits. The interface circuit schematic of each channel is shown in Fig. 6.6, where $x=0\sim 15$, $R_a/R_b/R_c/R_d/R_e/R_f/R_g/R_h$ and C_f are determined according to specific functions such as scaling, level shifting, filtering or reference-setting for analog signals before

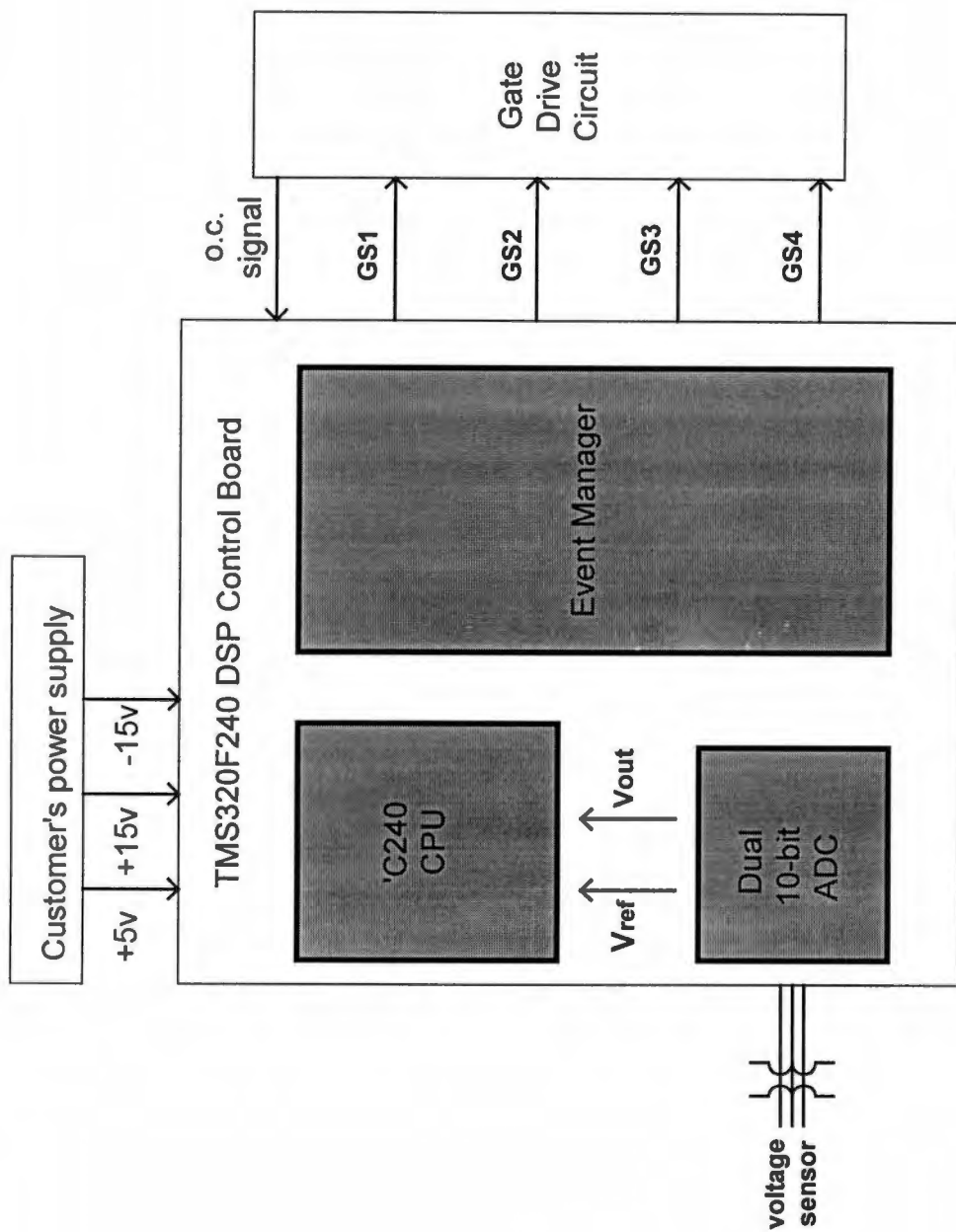


Fig. 6.5 The DSP Interface Circuit

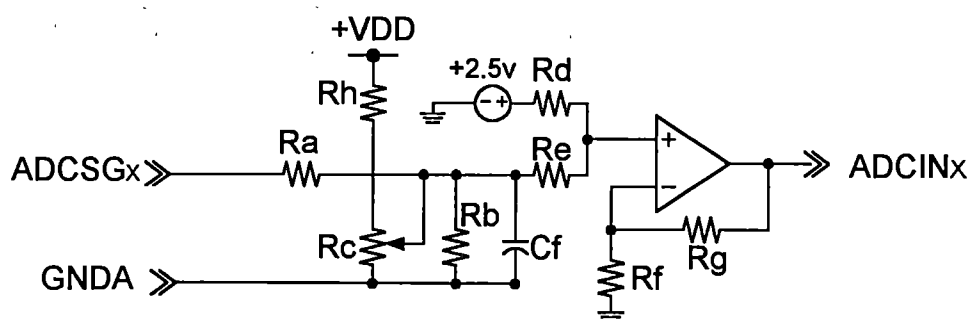


Fig. 6.6 Analog signal interface circuit

sending them to the DSP chip's A/D converters.

The interface circuits for setting the voltage reference and performing voltage sensing can be easily built using the on board analog interface circuits. The implementation block diagrams are shown in Fig. 6.7 and Fig. 6.8, respectively. In Fig. 6.7, the potentiometer (10k OHM R_c) is used to generate a desired voltage level between 0 to 5 Vdc. R_a , R_b , R_d , and R_f are open and R_e and R_g are shorted. A 0.1 μF capacitor is used for C_f to minimize noise. In Fig. 6.8, R_{in} is selected as 50 K ohm to limit the maximum input current of the voltage sensor to 10 mA when the highest voltage reaches 500 Volts. In order to output 5 V at 500 V input voltage, the scaling resistor R_b is selected at 200 ohm.

VI. 3. 3 MOSFETs gate drivers

The proper marriage of a MOSFET gate driver and the power MOSFET is essential to good switching performance. Using a gate driver that matches the MOSFET characteristics provides fast rise/ fall times and reduces associated losses.

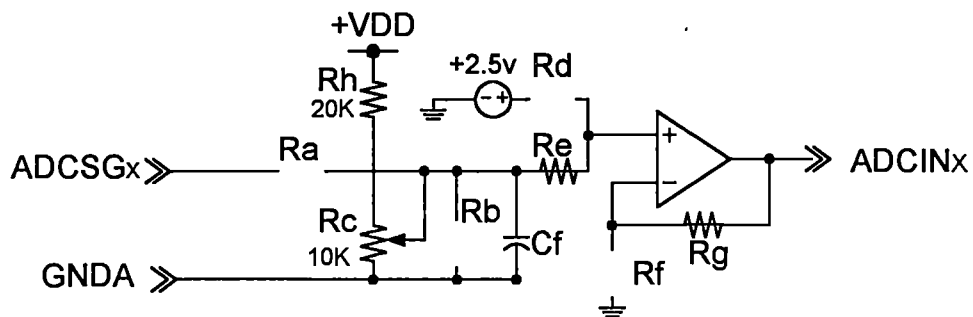


Fig. 6.7 Using the analog interface circuit to generate a dc voltage reference

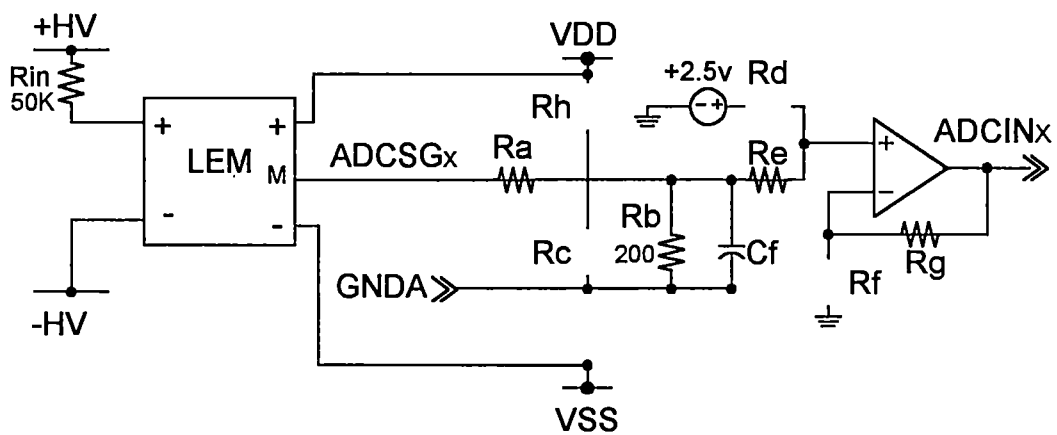


Fig. 6.8 The interface circuit of voltage sensor and DSP board

The gate drivers selected are MICREL MIC4451 and MIC4452. With the output of the flyback power supply for the MOSFET at 10 V, the total maximum gate driver output current is 8A. MIC4451 is an inverting driver and MIC4452 is a non-inverting driver. The supply voltage can be as high as 20 V and be capable of providing 12A peak current output.

The power MOSFETs used are ten IR3205's in parallel. The gate input capacitance is 4000 pF per device and the gate charge Q_g is 170 nC per device. For switches on the low voltage side, ten devices in parallel will have a total gate charge of 1700 nC. The device switching rise and fall times are 170 ns, which is compatible with a switching frequency of 20 kHz.

An HP2212 opto-coupler is used to provide electrical isolation between the control circuit and the power stage mainly for its high speed and high common mode noise rejection. The HP2212 can work with a supply voltage up to 20 V. The output of the opto-coupler drives the MIC4451 and 4452 chip via a pull-up resistor of 350 ohm.

VI. 3. 4 IGBT gate drivers

A new gate drive optocoupler HCPL-316J is used to drive the IGBT modules. Like the traditional IGBT-Driver IC EXB840/850, it can also provide over-current protection and fault status feedback. In addition, it has a smaller footprint size than older drivers. The typical application circuit is shown in Fig. 6.9. The *DESAT* terminal monitors the IGBT collector-to-emitter voltage V_{ce} . When the voltage on the *DESAT* terminal exceeds 7 volts, the IGBT gate voltage (V_{out}) is slowly lowered and

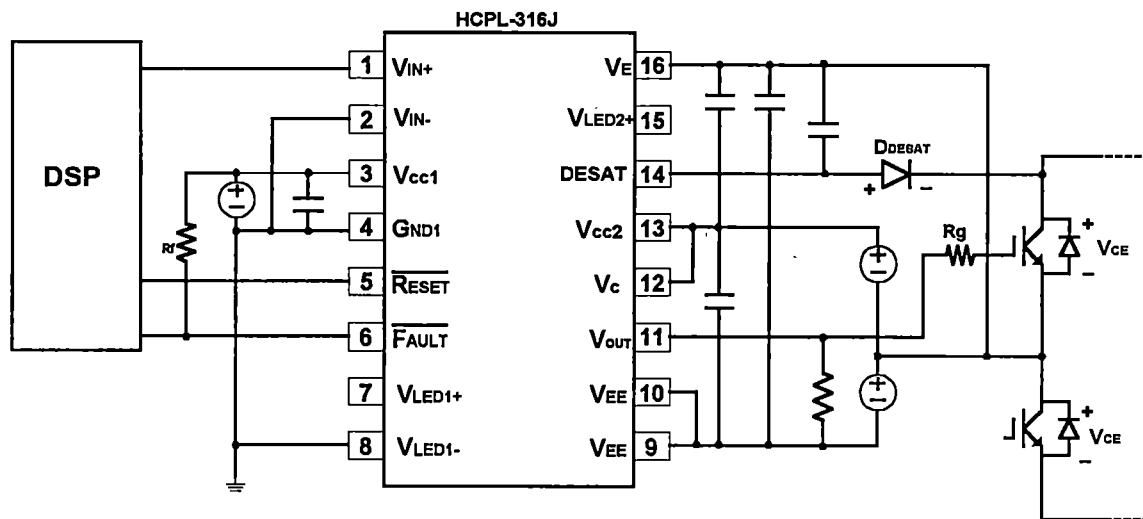


Fig. 6.9 Typical de-saturation protected gate drive circuit

the *FAULT* output goes low, thereby notifying the microcontroller of the fault condition.

VI. 3. 5 Power supplies for gate drivers and DSP board

In the dual active half-bridge converter system, the four switches need four isolated power supplies for gate drivers. According to the devices' characteristics, it is decided to use +10 V for the two MOSFET drivers on the low voltage side and positive 20 V for the two IGBT drivers on the high side. In the DSP control board, +15V, -15V and +5V power supplies are needed. The schematic view of the power supplies is shown in Fig. 6.10. All of them need to be regulated accurately.

The circuit and operation principle of the power supply for gate drivers and DSP are almost identical. Two separate flyback power supplies are employed. One

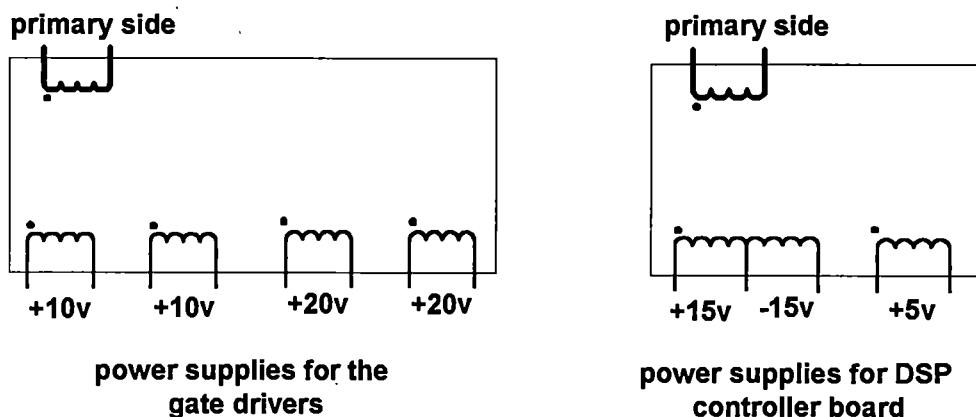


Fig. 6.10 Schematic view of the power supplies

supplies the DSP control board and the other supplies the gate drivers. Fixed frequency peak current-mode control with voltage feedback is used to regulate each power supply. In the DSP power supply circuit, in order to get accurate +15 V, -15 V and +5 V, two TO 220 package linear regulator 7815 and 7915 are used.

The flyback power supplies are designed with Cherry Semiconductor's CS2843 automotive current mode PWM controller. The CS2843 is designed specifically for use in automotive applications. The low start threshold voltage of 8.0v and the ability to survive 40V automotive load dump transients are important for automotive subsystem designs. The CS2843 provides all the necessary features to implement fixed frequency current-mode control.

In the control circuit of the power supplies, there are two feedback loops: the faster loop monitors the current through the flyback transformer; the other loop monitors one of the output voltages. The circuit uses current-mode control to adjust

the duty cycle of the PWM waveform. The current loop involves the control chip, the flyback transformer, and the current sensing resistor. This signal is then fed back to the I_{sense} pin of CS2841B. The current is sensed on a cycle-by-cycle basis, which provides a tight line and load regulation. If the power supply goes into current limit due to fault condition, the primary current is folded back to less than its maximum operating point. For the voltage feedback loop, the output of one of the switch driver (4451/2) is monitored and regulated by using a TL431 shunt regulator which senses any perturbation in the output voltage via a voltage divider composed of two resistors. The voltage divider is configured to obtain voltage of 2.5 V from the 10 V output. The divider output voltage is compared with the internal 2.5V reference of the TL431, which sinks the LED cathode of the opto-coupler 4N25. The TL431 biases the cathode of the opto-coupler's diode more negatively by pulling it closer to the ground, and lets it up when the output voltage come into regulation. The opto-coupler's transistor is biased within its linear region, establishing a voltage across the resistor connected to PIN4 of 4N25, which could be seen by the CS2841's error amplifier input. This is compared to the internally generated 2.5V reference. The RC network around TL431 sets the overall voltage control loop frequency response via the current transfer ratio of the opto-coupler.

A TDK PQ2020 core and TDK PQ2020 bobbin are selected for the transformer design. A switching frequency of 90 kHz is selected. The primary windings are 10 turns each, and the secondary windings are 21turns for the 10V output, 25 turns for the positive and negative 15V outputs, 12 turns for the 5V output.

All three transformers are built in a sandwich structure. The primary winding is divided into two primary layers. This structure is the result of consideration of reducing the leakage inductance. Polyimide isolation tape is used between every two layers to insure the isolation voltage between windings can be higher than 800 V.

VI. 4 Software Design

VI. 4.1 Introduction

The control scheme of the proposed converter system is implemented by the 'C240 DSP controller board, which is shown in Fig. 6.11. The controller board manufactured by Millennium Technologies contains an F240 DSP chip, which operates at 20 MIPS with an instruction cycle time of 50 ns, dual 10-bit analog-to-digital converters (ADCs), synchronous and asynchronous communications peripherals, 544 words of dual access RAM, 16K words of on-chip Flash memory and the event manager. Besides these on-chip I/O and peripherals, the DSP board also includes a 16-channel analog input interface for direct connection to voltage and current sensors, 9 PWM outputs to gate drive circuits of power devices, Fault/alarm signals to block gate signals and emergency turn-off. These functions and interfaces provide easy implementation of a complete control system.

The control software receives the analog signal from output voltage sensor periodically. After analog-to-digital conversion, the value is compared with the reference voltage command. The error is then sent to the controller to calculate the corresponding phase shift angle ϕ_1 . With this angle information, the event manager of

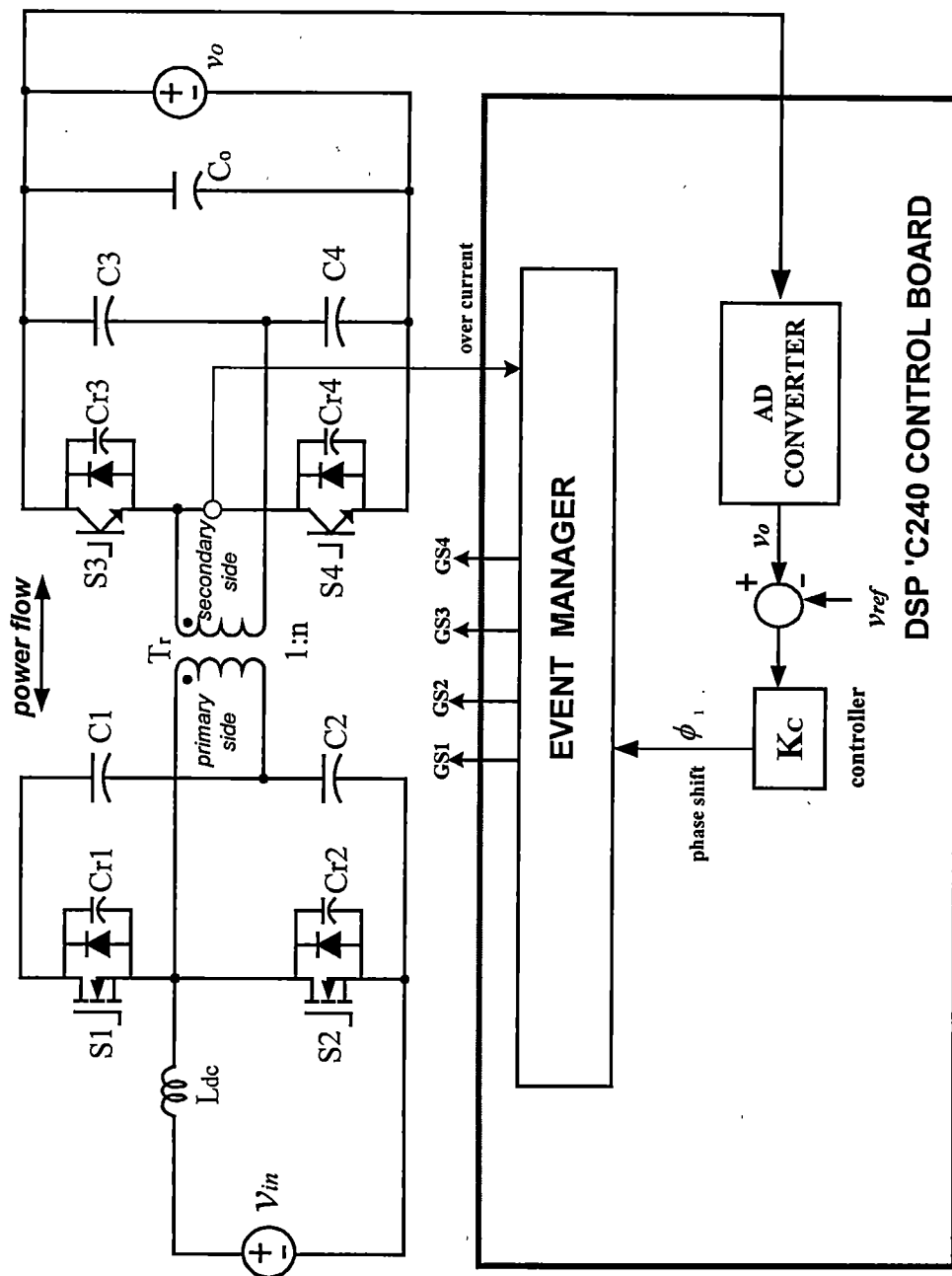


Fig. 6.11 The control block diagram for the proposed dc-dc converter

the 'C240 will generate two timing signals of 20 kHz square waves. The phase shift angle between two waveforms is ϕ_I . The gate signals of S1, S2, S3, and S4 are then generated based on the timing signals and the zero-voltage switching logic mechanism. If a short circuit of a high-voltage side device occurs, the gate signals of all the devices are disabled immediately to protect all the switches.

The functions of the event manager module include zero-voltage switching logic implementation, gate signal generation and interrupt service. They are described as follows.

VI. 4.2 Zero-voltage switching logic

Fig. 6.12 of the commutation process for S1 and S2 shows the zero-voltage sense circuit for device is not necessary. Instead, the gate signals with special defined dead band will be enough to implement the zero-voltage switching, which is shown in Fig. 6.13.

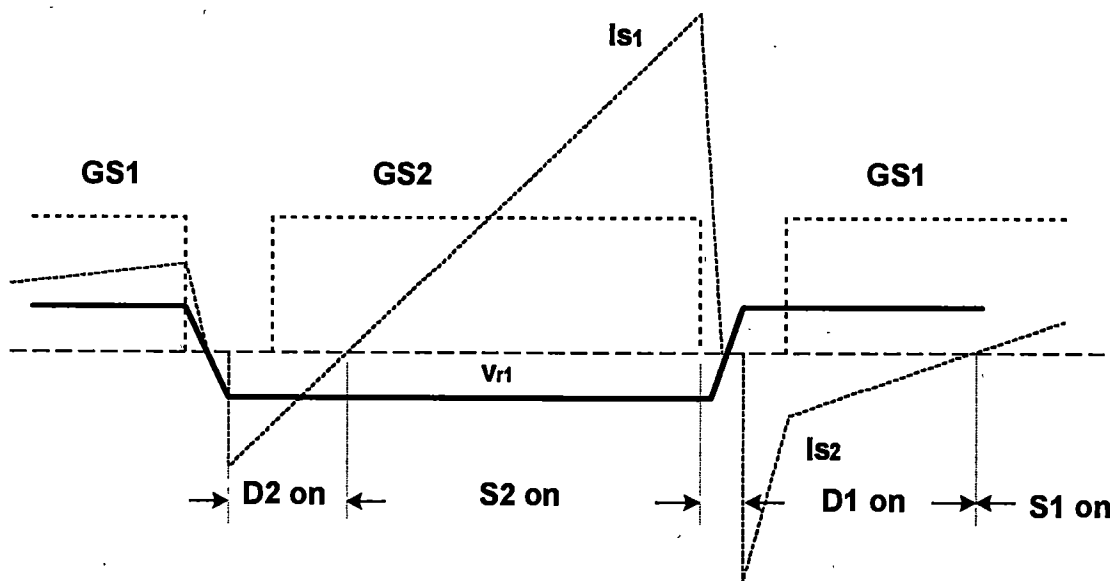


Fig. 6.12 Zero-voltage switching process for S1 and S2

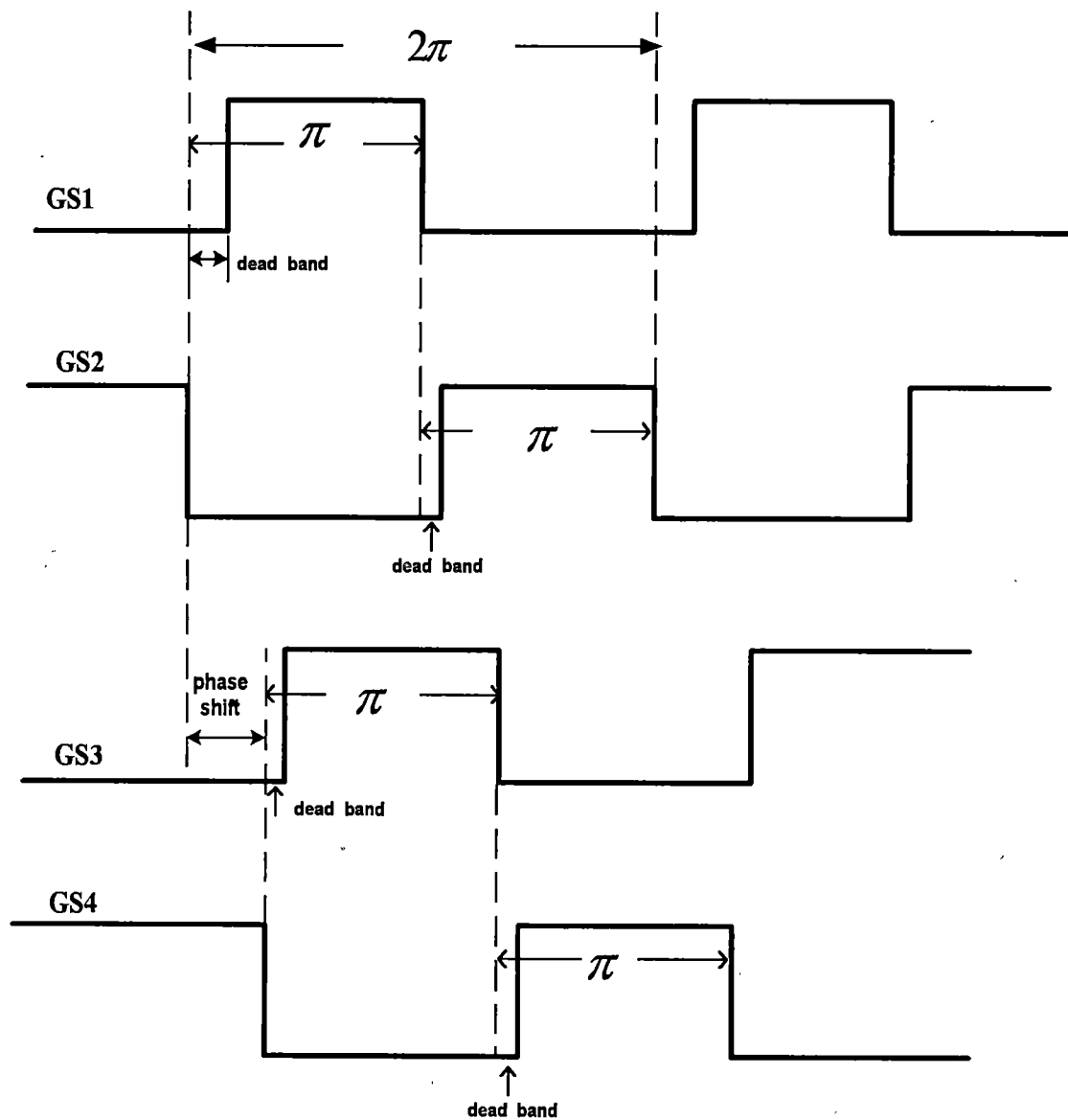


Fig. 6.13 Timing generation for zero voltage switching

VI. 4. 3 Generation of gate signals

The event manager module of the 'C240 is used to generate the above gate signals. It includes three independent up/down timers, each with its own compare register, three full compare units and three simple compare units. The full compare units support special PWM generation functions, such as a programmable dead-band function and a space vector PWM state machine. The block diagram is shown in Fig. 6.14.

Fig. 6.15 is the example of generation of GS1. There are two interrupts, underflow interrupt (UFINT) and period interrupt (PINT) every 25 μ S. During each interrupt service, a new value will be sent to the compare register to decide the width of the dead band. Therefore, the dead band can be changed easily on-line. The generation of other gate signals can be derived similarly.

VI. 4. 4 Interrupt services

In addition to reset and software interrupts, the 'C240 CPU also provides six maskable interrupt levels, each of the six interrupt levels can be shared by multiple interrupt sources. Table 6.3 shows an edited example of an interrupt vector table.

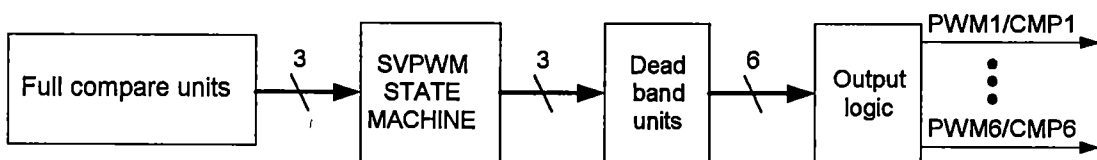


Fig. 6.14 The block diagram of full compare units of event manager module

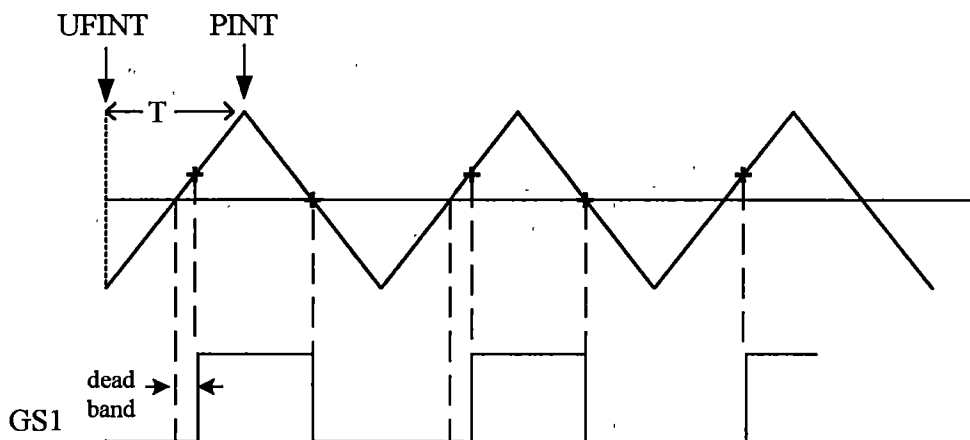


Fig. 6.15 The generation of S1 gate signal using event manager

Table 6.3. Example Interrupt Locations of Maskable Interrupts

Interrupt Level and address	Interrupt Source	Interrupt vector Address	Vector (ID)
INT1 0002 h (System)	XINT1 XINT2 XINT3 RTI	SYSIVR (701E h)	0002h 0011h 001Fh 0010h
INT2 0004h (EV INTA) (Group A)	PDPINT CMPINT etc.	EVIVRA (7432h)	0020h 0021h etc.
INT3 0006h (EV INTB) (Group B)	TPINT2 TCINT2 etc.	EVIVRB (7434h)	002Bh 002Ch etc.
INT4 0008h (EV INTC) (Group C)	CAPINT1 CAPINT2 CAPINT3 CAPINT4	EVIVRC (7431h)	0033h 0034h 0035h 0036h
etc.			
INT6 000Ch (System)	ADCINT XINT1 XINT2 XINT3	SYSIVR (701Eh)	0004h 0002h 0011h 001Fh

In order to generate the programmable dead band waveforms, two interrupts of EV interrupt group B, T2PINT and T2UFINT are required. From Table 6.3, they belong to INT3. So the first statement is to set up an interrupt vector (a pointer to the interrupt service routine placed in an absolute location), the following statement must be defined at the beginning of the program.

The following statement tells the assembler to form the address of the interrupt service routine named “MAIN” and placed into an absolute memory location of INT3, which is 0006 h.

```
.sect “.vectors”
INT3 B MAIN
```

The following are statements to initialize and enable the above interrupts.

```
ldp #232 ; point at EV reg page
SPLK #0ffh,IFRA ; Clear all Group A interrupt flags
SPLK #0ffh,IFRB ; Clear all Group B interrupt flags
SPLK #0fh,IFRC ; Clear all Group C interrupt flags

SPLK #01h,IMRA ; Mask all but PDPINT Grp A ints
SPLK #05h,IMRB ; Mask all but GPT2 UF&PER Grp B ints
SPLK #00h,IMRC ; Mask all Grp C ints

LDP #0 ; point to memory page 0
SPLK #0ffh,IFR ; Clear all core interrupt flags
SPLK #0eh,IMR ; Unmask all EV interrupts to CPU

EINT ; Enable global interrupt
```

Event manager interrupt events are organized into three groups: EV interrupt groups A, B, and C. EV interrupt group A generates interrupt requests to the core on INT2. EV interrupt group B and C generate interrupt requests to the core on INT3 and

INT4, respectively. There is an interrupt flag register, an interrupt mask register and interrupt vector register associated with each EV interrupt group. When an interrupt event occurs in the EV module, an interrupt request is generated to the CPU if the corresponding interrupt flag is set in one of the flag registers and unmasked in one of the mask registers. So the purpose of these statements is to mask all the other interrupts except T2PINT and T2UFINT.

After an interrupt is recognized by the DSP core, the related interrupt vector register is read in the interrupt service routine. The vector in the interrupt vector register identifies which pending and unmasked interrupt has the highest priority.

VI. 5 Experimental Results

Based on the design given in section VI. 2, a prototype has been implemented using the following components.

S1-S2	IRF3205 55V, 110A MOSFET (IR)
S3-S4	2MBI75N-060 600V, 75A IGBT half-bridge (Fuji)
T _r	2:26 turns, E65-3F3 core (Philips)
L _{dc}	5 μ H, 7 turns copper foil, AMCC-25 metglas C-core (Allied Signal)
C1-2	47D103M025AY2A 25 V, 10 mF electrolytic capacitor (United chemi-Con)
C3-4	80D101P250JA5D 250V, 100 μ F electrolytic capacitor (Sprague)
Cr1-Cr2	V1H474JL 100v, 0.047 μ F metal film capacitor (Panasonic)

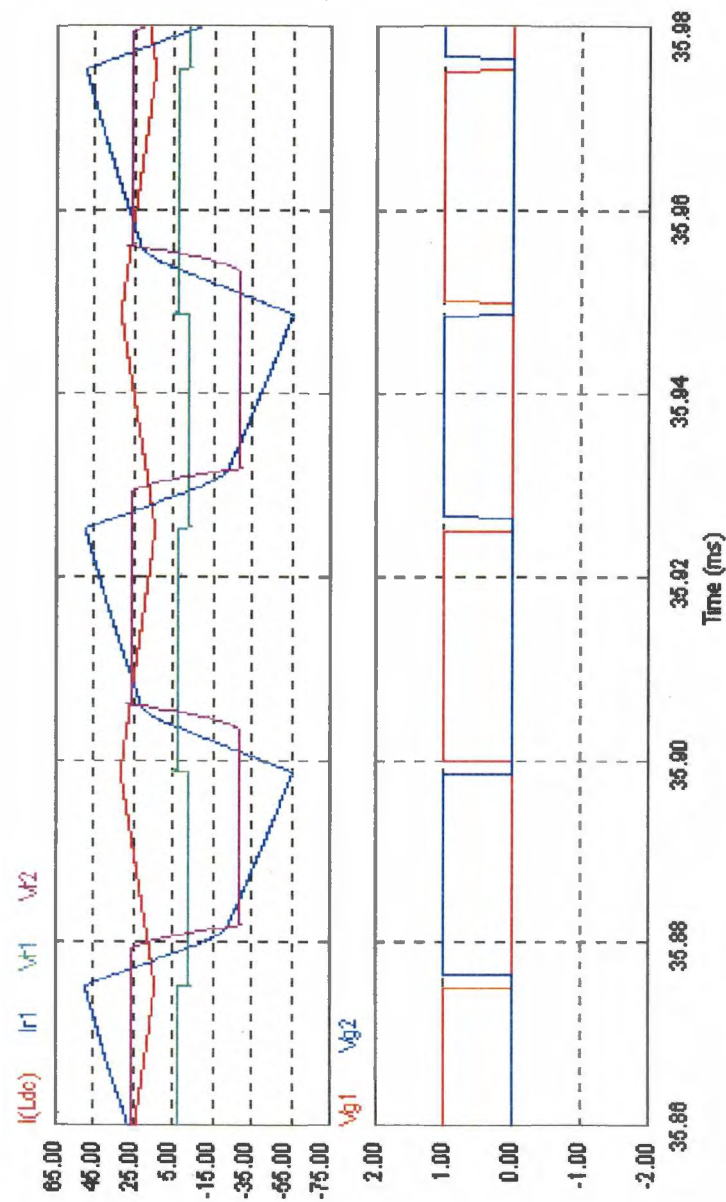
Cr3-Cr4 715P33396L 600V, 0.033 μ F polypropylene capacitor

VI. 5.1 Discharging/boost mode

VI. 5.1.1 Diode rectification

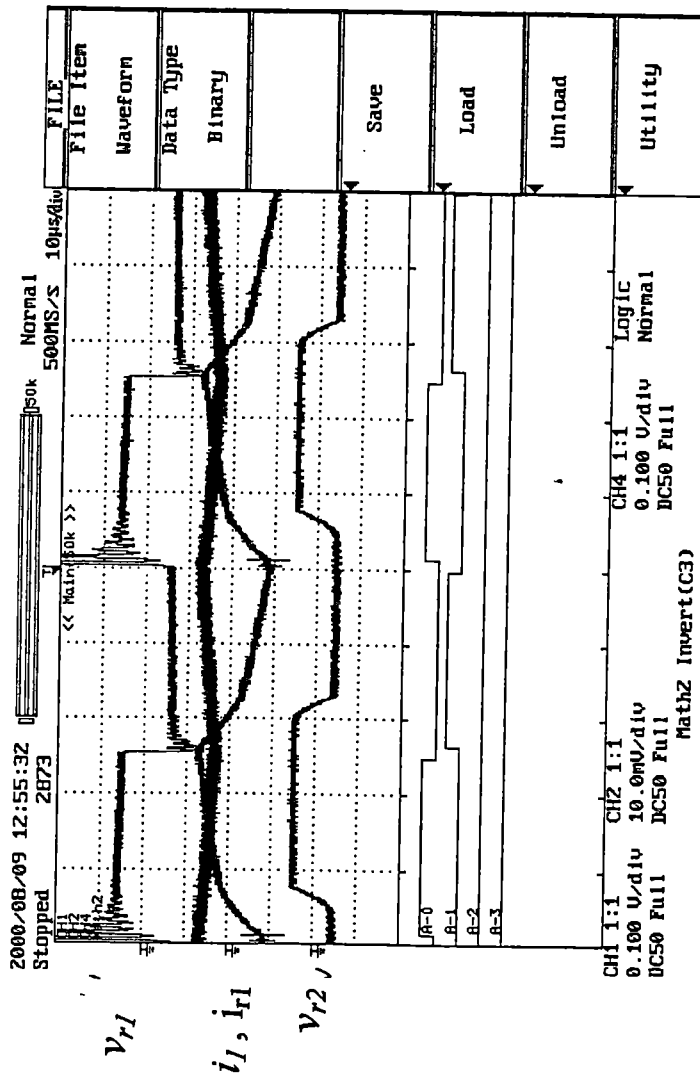
The designed leakage inductance of transformer is 0.3024 μ H. However, it is hard to control the actual value when the transformer is manually built. The measured leakage inductance is about 0.02 μ H. In order to verify the prior analysis, an extra leakage inductance 0.4 μ H is added to the circuit. The experimental results and simulation results of static performance are obtained in Fig. 6.16 (a)-(b). The converter is operating at 20 kHz in the discharging mode with diode rectification. There is a good agreement between simulation results and experimental results. The magnitude of v_{r2} in simulation is 26 V, the experimental magnitude is also about 26 V. In addition, there is also similarities in shape and frequency of v_{r2} . As for i_r , the wave shape of simulation and that of experiment agree with each other. The peak values of i_r in simulation are + 45 A and -55 A and those of experimental values are + 40 A and -50 A. The average value of i_l in Fig. 6.16 (a) is about 22 A and that of Fig. 6.16 (b) is 25 A. The phase shift angle between v_{r1} and v_{r2} in the two figures are consistent. Although the magnitude and the shape of v_{r1} are almost the same in the two figures, the experimental result of v_{r1} waveform has a ringing effect. This is because it is hard to measure directly the two terminals of the primary side of transformer, consequently the measurement loop may be the main reason for this ringing effect.

The soft switching operation, which was depicted in Fig. 3.5, is also confirmed from the experimental results. When S2 is gated off, the sum of i_r and i_l charges and



(a) Simulation results of v_{r1} , i_L , i_r , v_{r2} when $v_{in}=3$ V, $L_s = 0.4$ μ H

Fig. 6.16 Steady state operation of boost mode with synchronous rectification when $v_{in}=3$ V, $L_s = 0.4$ μ H



(b) Experimental results of v_{r1} , i_L , i_r , v_{r2} when $v_{in}=3\text{ V}$, $L_s = 0.4\text{ }\mu\text{H}$

Fig. 6.16 Steady state operation of boost mode with synchronous rectification when $v_{in}=3\text{ V}$, $L_s = 0.4\text{ }\mu\text{H}$

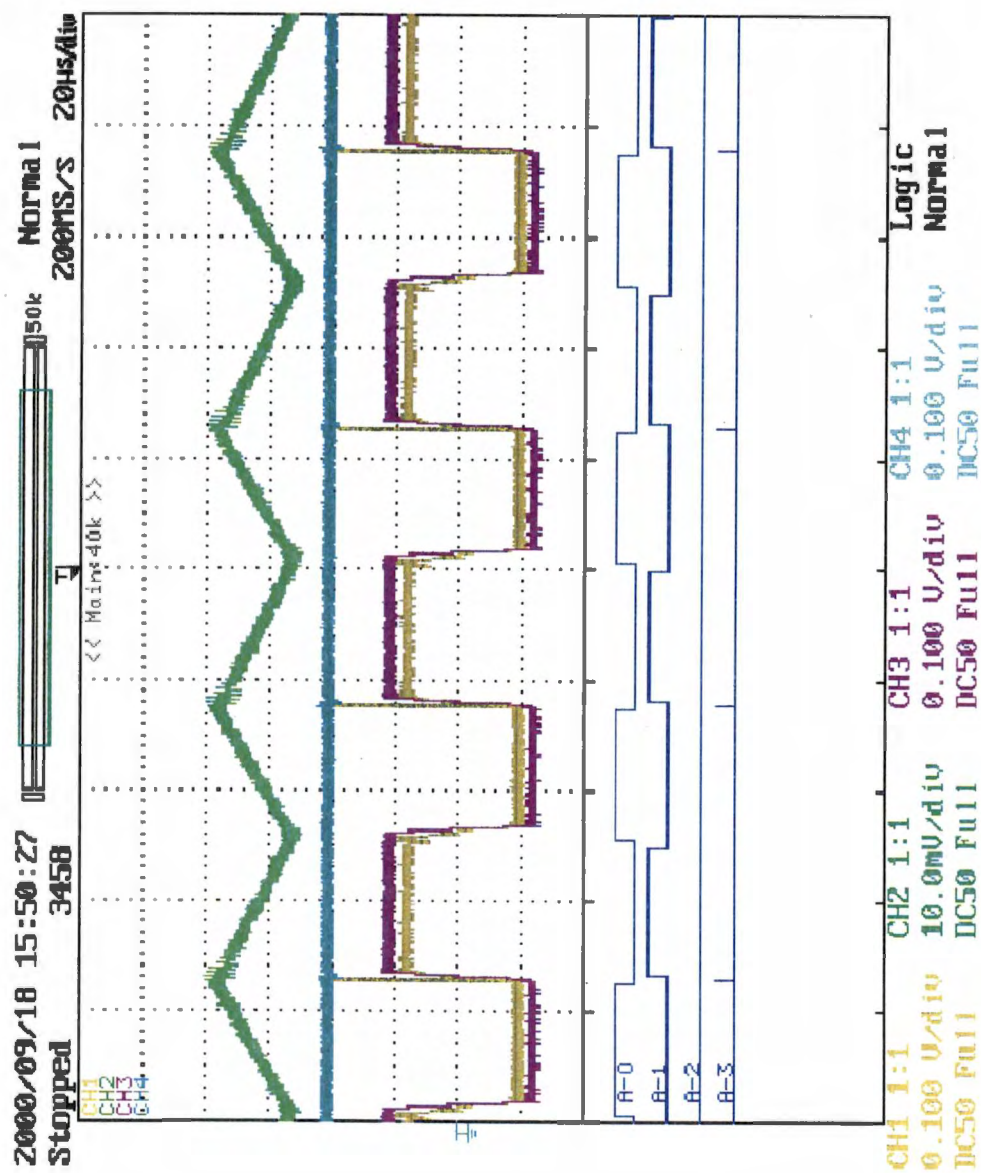
(continued)

discharges resonant capacitors $Cr1$ and $Cr2$, respectively. As a result, v_{r1} changes from -2.5 V to $+2.5$ V with a limited dv/dt of 160 V/ μ s. The transient peak voltage is mainly due to the parasitic inductance of the measured loop. Although S1 is given an “on” signal after 1.5 μ s when S2 is gated off, D1 is conducting the current at this moment until i_r increases to i_l . When i_r is bigger than i_l , the current is diverted from D1 to S1 and S1 is turned on at zero voltage. The soft-switching process can be derived similarly when S1 is gated off. Because the turn off current is 20 A at this moment, the dv/dt of v_{r1} is 40 V/ μ s. S3 and S4 are operating in the diode rectification mode.

As can be clearly seen, there is a good agreement between the simulation results and experimental results of static performance when L_s is selected as 0.4 μ H, verifying the correct analysis of converter operation principles in Chapter III.

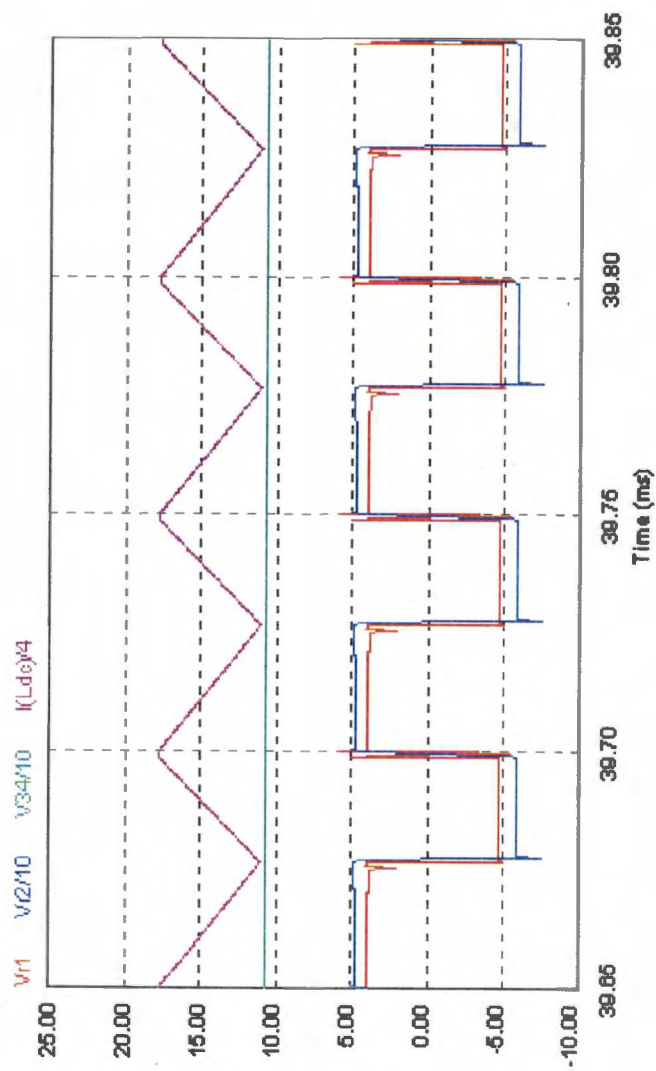
Another conclusion made in Chapter III states that the less leakage inductance, the less current stress of the switch and the less conduction loss. Although the smaller leakage inductance of a transformer may change the circuit operation including soft switching, the converter performance may still be comparatively good because of the above advantage. In addition, this means that the proposed converter may be robust with respect to transformer design. In order to verify these points, experimental results and simulation results are obtained in Fig. 6.17 (a)-(b), when the converter is operating at open-loop steady state and the leakage inductance is 0.02 μ H.

Each division of Fig. 6.17 (a) and (b) has the same unit. It is clearly seen that there is a consistency in the magnitude, shape and phase shift of v_{r1} and v_{r2} .



(a) Experimental results of v_{r1} , i_l , v_o , v_{r2} when $v_{in}=5\text{ V}$, $L_g=0.02\text{ }\mu\text{H}$

Fig. 6.17 Steady state operation of boost mode with synchronous rectification when $v_{in}=5\text{ V}$, $L_g=0.02\text{ }\mu\text{H}$



(b) Simulation results of v_{r1} , i_L , v_o , v_{r2} when $v_m=5$ V, $L_s = 0.02$ μ H

Fig. 6.17 Steady state operation of boost mode with synchronous rectification when $v_m=5$ V, $L_s = 0.02$ μ H

(continued)

Voltage spikes are observed at the rising edge of transformer primary voltage v_{r1} . This is because the leakage inductance of transformer is changed, current i_r and i_l at this point does not satisfy the soft switching condition of Fig. 6.16, which means there is not enough charging and discharging current flowing through the resonant capacitors $Cr1$ and $Cr2$. However, the switching process at this point is not hard switching, either; otherwise, the voltage spikes would go much higher and the problem would get worse at higher output power. Even with such small leakage inductance, the device would be damaged without a voltage clamp circuit [6]. But for the proposed converter, the performances will be improved as output power increases because the average value of i_l also goes higher to provide more charging and discharging current, which will be verified later. Accordingly, the switching process at this point is not completely soft switching. The performance is half soft switching and half hard switching.

The shapes of v_o and i_l in Fig. 6.17 (a) agree well with those in Fig. 6.17 (b) but there is a minor difference in the magnitudes. The experimental waveform of v_o is 100 V and the simulation result is more than 100 V. The average of i_l is smaller in simulation than experimental result. However, it is reasonable for simulation results to have a higher efficiency, which is represented by lower average of input current i_l and higher output voltage v_o .

The prototype has been successfully tested at $P_o = 1.769$ kW. The experimentally obtained waveforms are shown in Fig. 6.18, where $v_{in} = 13.2$ V, $v_o = 282$ V. It is seen clearly that the voltage spikes at the rising edge of v_{r1} is

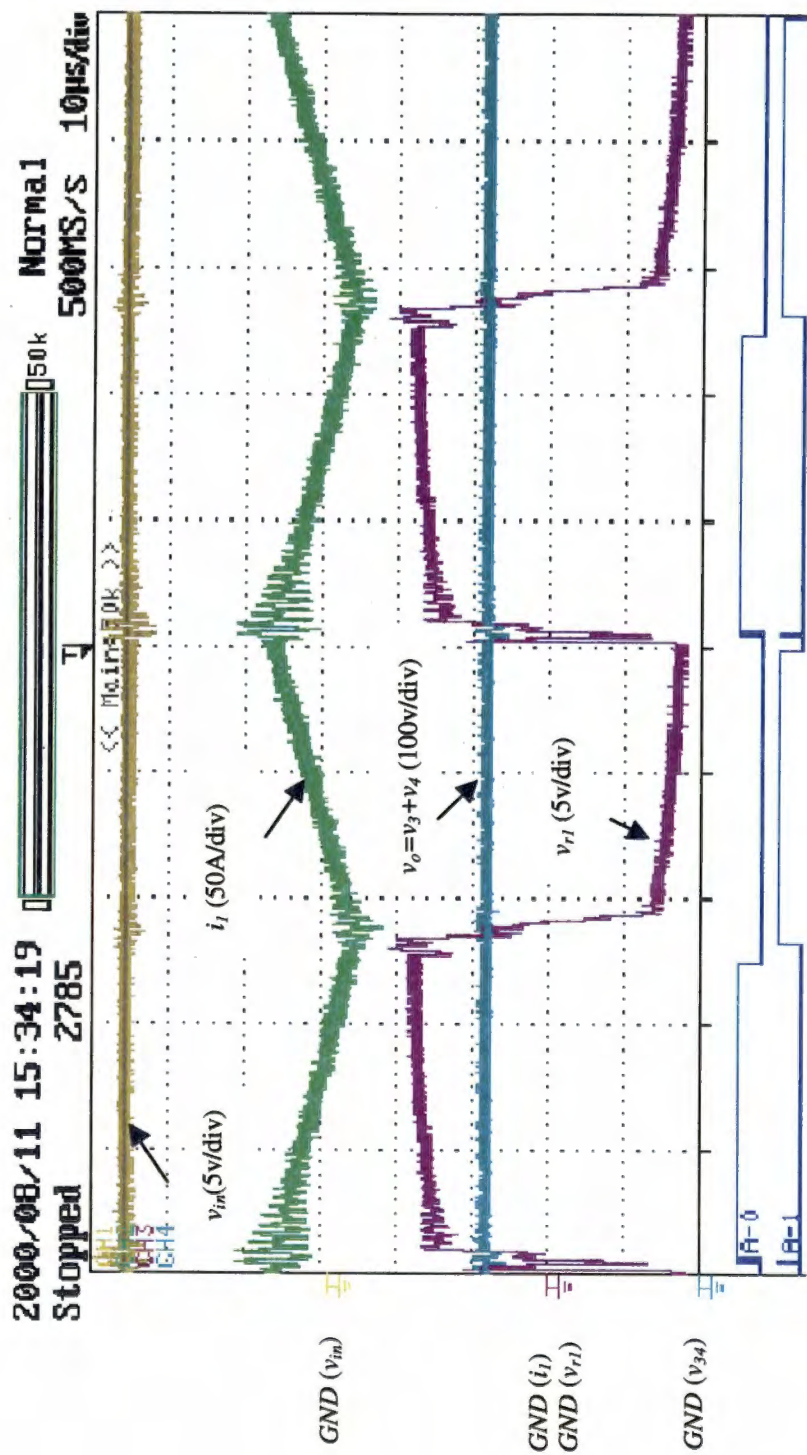


Fig. 6.18 Experiment results of boost mode with synchronous rectification when $P_o = 1.769$ kW

not worse than Fig. 6.17, which $P_o = 100^2/45 = 222$ W.

The simulation and experimental output characteristics of the converter are presented in Fig. 6.19. As indicated in the figure, the blue trace is the experimental result, the green one is of detailed circuit simulation and the red one is of average model simulation. The similarity of the three curves confirms the validity of the average model. The difference between the average model, detailed circuit model and prototype can be explained as follows. The average model assumes all switches and components are ideal, there are no losses in switches, capacitors, the inductor or the transformer. The detailed circuit model is a better approximation of the actual circuit. The above losses have been taken into account and the efficiency will be lower than that of average model. The difference between the circuit model and the prototype is likely in two areas: (1) Higher switching losses in the prototype due to the imperfect switching, and (2) Inaccurate settings of parameters (such as on resistance) in the detailed model. Thereby, the output voltage of average model is higher than that of the detailed circuit model and the detailed circuit model voltage is higher than the prototype.

The experimentally measured efficiency as a function of the output power is shown in Fig. 6.20, as well as the efficiency derived from detailed circuit models. When the connection resistance between C1 and C2 is regarded as zero, the simulated efficiency is described as the red curve and around 94 % at 1.6 kW, which confirms that the converter performance is still good when $L_s = 0.02$ μ H. Although extra switching losses are added because soft switching of some points are lost, the

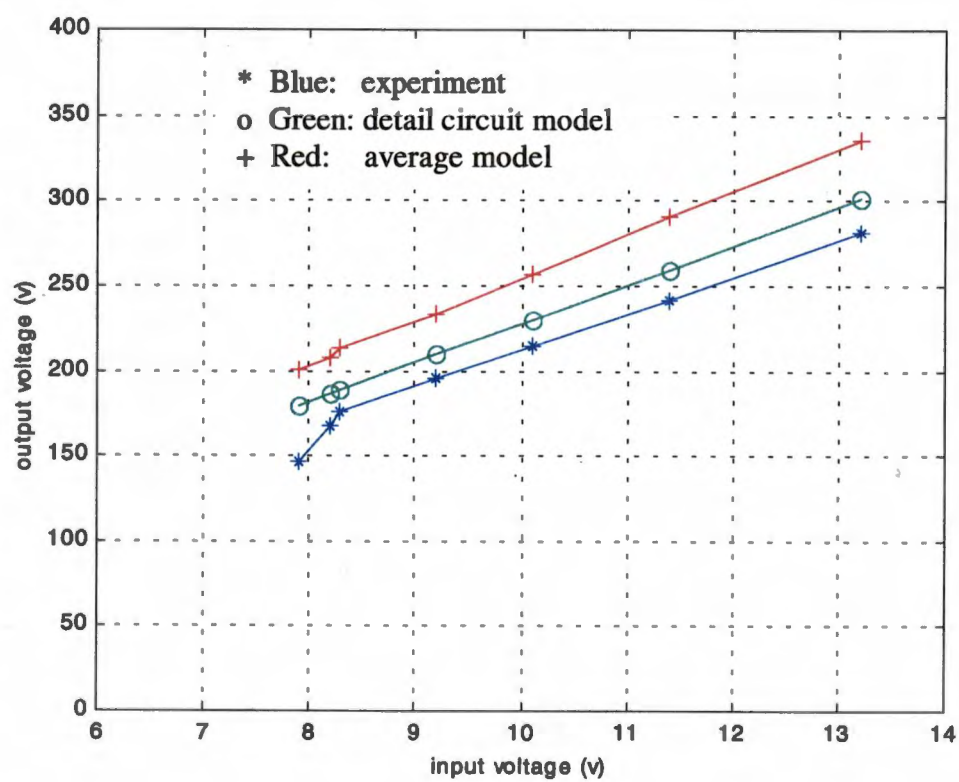


Fig. 6.19 Output voltage comparisons

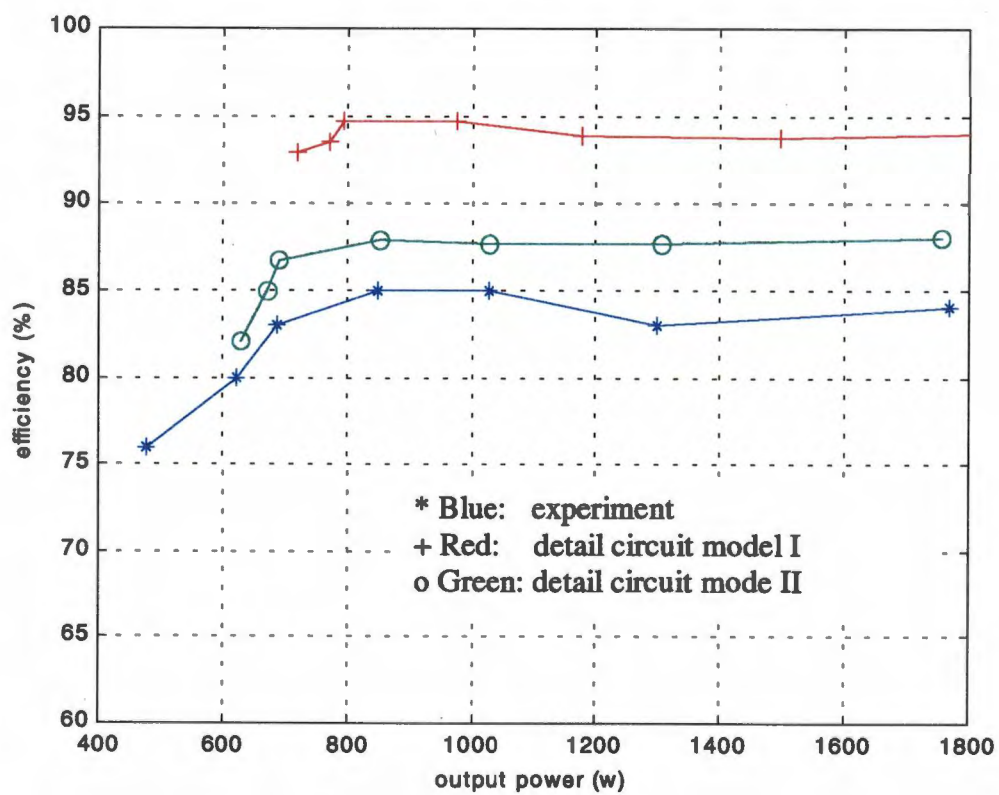


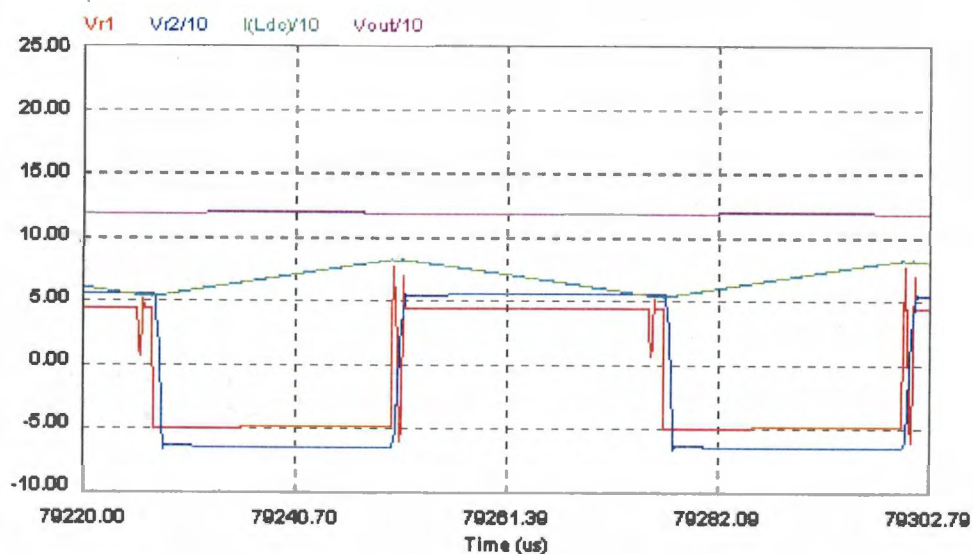
Fig. 6.20 Efficiency as a function of output power

conduction loss is decreased, the overall system efficiency is still high. However, the measured efficiency is lower than the simulated value. This is because of the poor connection of the prototype between $C1$ and $C2$ allowing additional resistances to be brought in. As large current is flowing through $C1$ and $C2$, the power losses of the connection resistances become significant even with a small value such as 0.001 ohm to 0.01 ohm. The green curve in Fig .6.20 is the efficiency obtained from simulation results when the connection resistance equals 0.004 ohm.

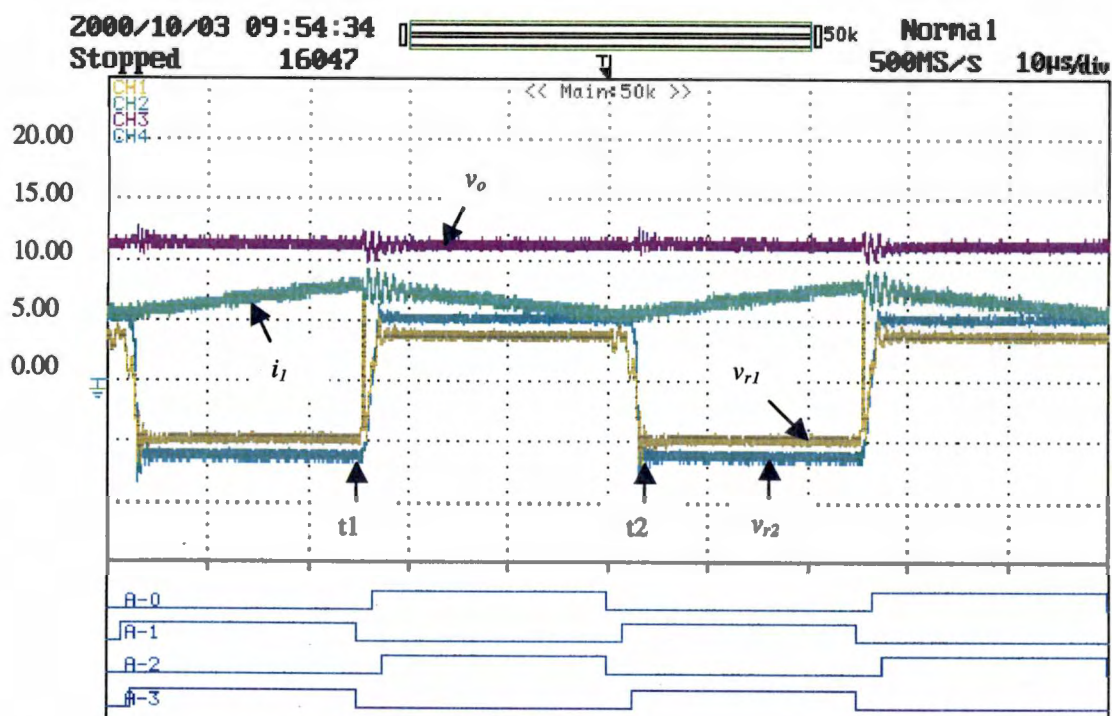
VI. 5.1.2 Dual active half-bridges

If there is a change in load or input voltage source when power is flowing from the low voltage side to the high voltage side, the phase shift angle between v_{r1} and v_{r2} is required to adjust to provide enough output power. In this case the converter works with dual half-bridges activated.

Fig. 6.21 shows the simulation and experimental results under steady state operation of boost mode with dual active bridge. For comparison, the units of (a) are selected as the same as those of (b). For example, v_{r1} is 5V/div, i_l is 50 A/div, v_{r2} is 50 V/div and v_o is 5 V/div. The “0” represent the grounds of all waveforms. The logic gate signals of S1 to S4 are shown below the relevant waveforms. The load resistance is 45 ohms and v_{in} is 5 V. The phase shift angle in Fig. 6.21 is selected as 0.04π , i.e., the gate signal of S1 is leading 1 μ s of S2.



(a) The simulation results of v_{r1} , i_l , v_o , v_{r2} when $v_{in}=5$ V, $L_s = 0.02$ μ H



(b) The experimental results of v_{r1} , i_l , v_o , v_{r2} when $v_{in}=5$ V, $L_s = 0.02$ μ H

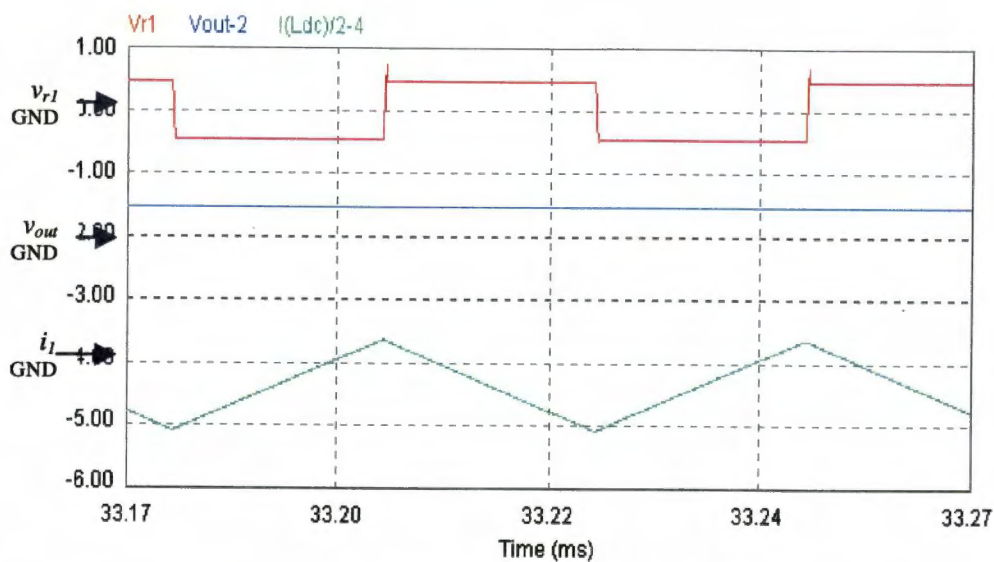
Fig. 6.21 Steady state operation of boost mode with dual active half-bridge

The shapes and the magnitudes of all the waveforms of (a) and (b) agree well with each other. The measured dv/dt of S3 at t_1 and t_2 are $91\text{ V}/\mu\text{S}$ and $200\text{ V}/\mu\text{S}$, respectively. The simulation results demonstrate those as $100\text{ V}/\mu\text{S}$ and $167\text{ V}/\mu\text{S}$. It is interesting to compare Fig. 6.21 with Fig. 6.17. Both figures have been obtained under same working conditions except Fig. 6.17 is at diode rectification mode and Fig. 6.21 is in dual active half bridge mode. The v_o of Fig. 6.21(b) is 108 V and is higher than that of Fig. 6.17(a), which is 100 V . This is because the phase shift angle of Fig. 6.21 is larger. If the phase shift angle increases to 0.5π , the output power will reach the maximum value.

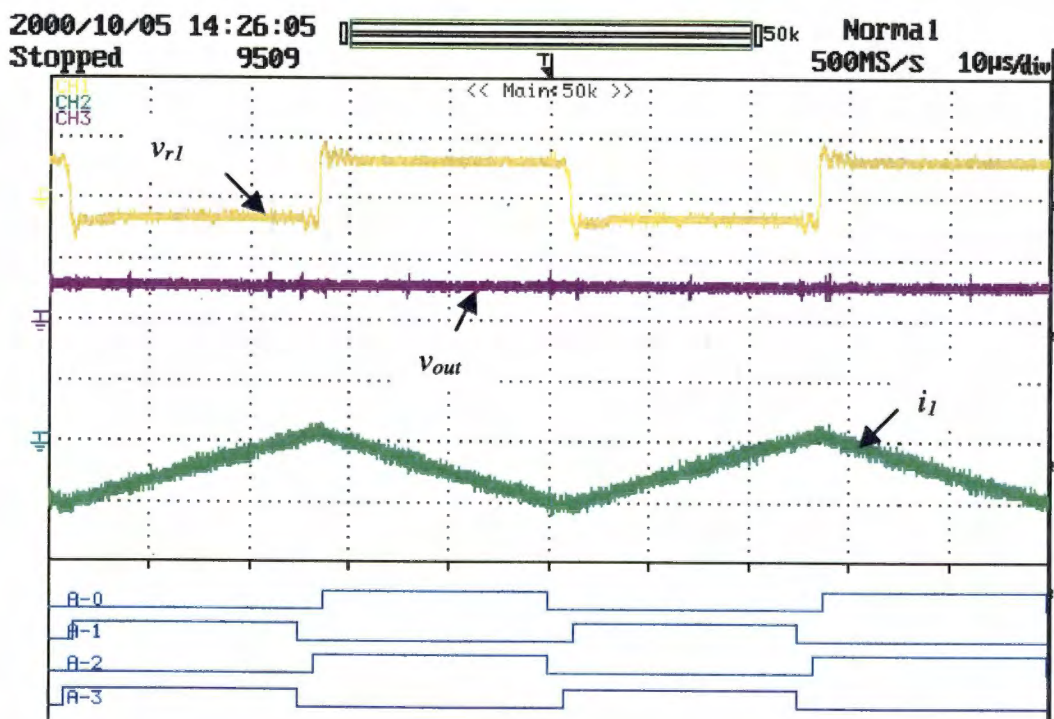
VI. 5. 2 Charging/buck mode

When power flows from the high voltage side to the low voltage side, the converter is working under buck mode. The relevant waveforms are obtained in Fig. 6.22 (a)-(d). The voltage source of the high voltage side is about 12 V , and the units of simulation and experimental results are the same. For example, v_{r1} is $1\text{ V}/\text{div}$, i_l is $2\text{ A}/\text{div}$, v_{r2} is $10\text{ V}/\text{div}$ and v_{out} , which is the output voltage of low voltage side, is $1\text{ V}/\text{div}$. All the switches are activated in the buck mode to let the required power to flow from the high voltage side to the low voltage side. The logic gate signals of switches are also shown. Compared to Fig. 6.21, the phase angle of S3 in Fig. 6.22 is leading S1 by 0.04π because of the reversed power flow direction.

In Fig. 6.22 (a), “0”, “-2”, and “-4” are the ground points of v_{r1} , v_{out} and i_l , respectively. Similarly, “0”, “-2”, and “-4” are the ground points of v_{r2} , v_{out} and i_l in

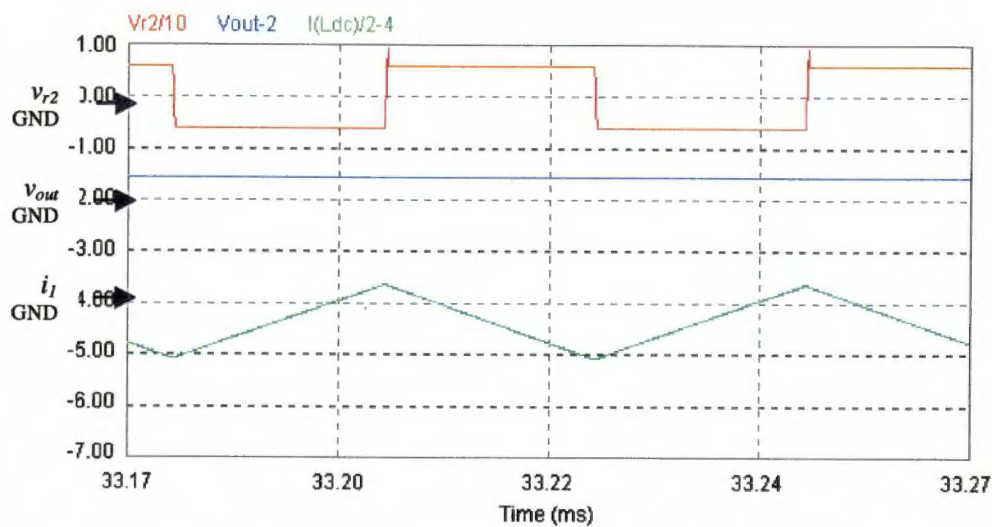


(a) The simulation results of v_{r1} , i_l , v_o

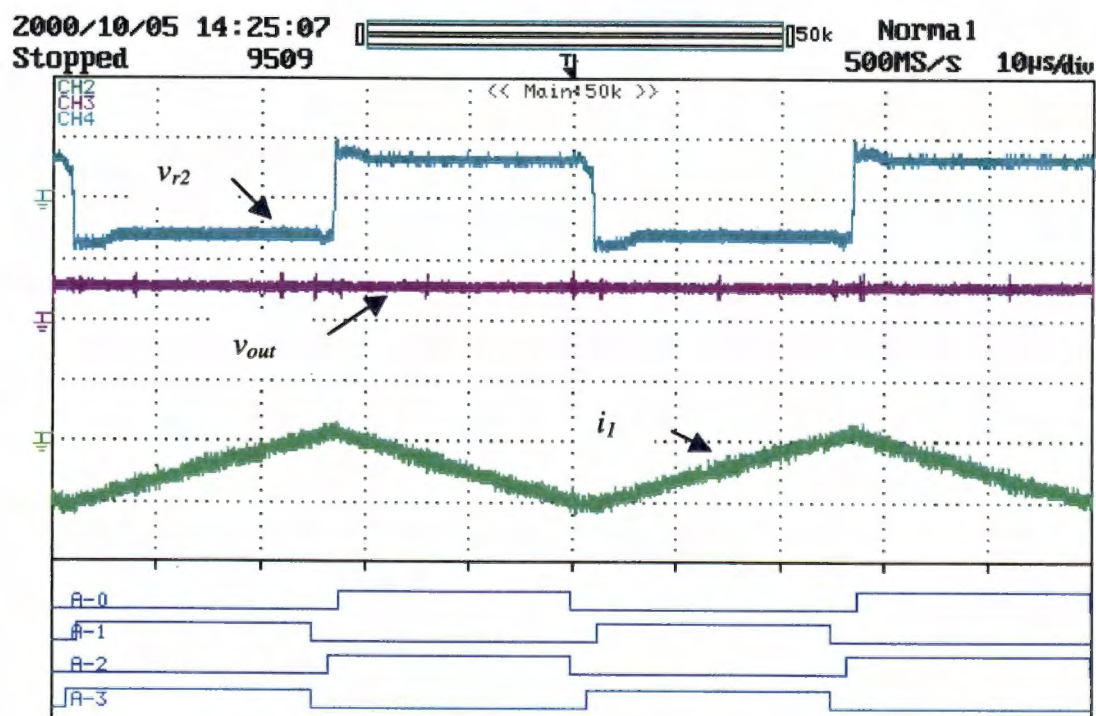


(b) The experimental results of v_{r1} , i_l , v_o

Fig. 6.22 Steady state operation of buck mode



(c) The simulation results of v_{r2} , i_L , v_o



(d) The experimental results of v_{r2} , i_L , v_o

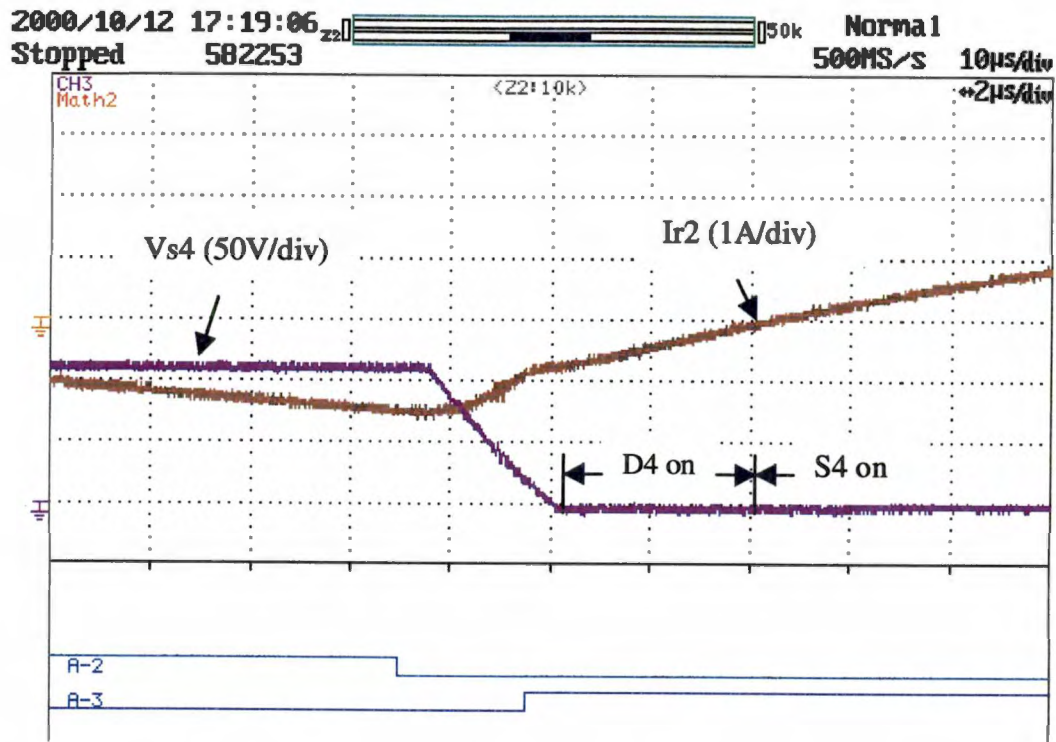
Fig. 6.22 Steady state operation of buck mode

(c). It is clear that there is consistency in magnitudes and shapes between simulation results and experimental results. The average value of current i_l is negative because the power is now flowing into the low voltage side.

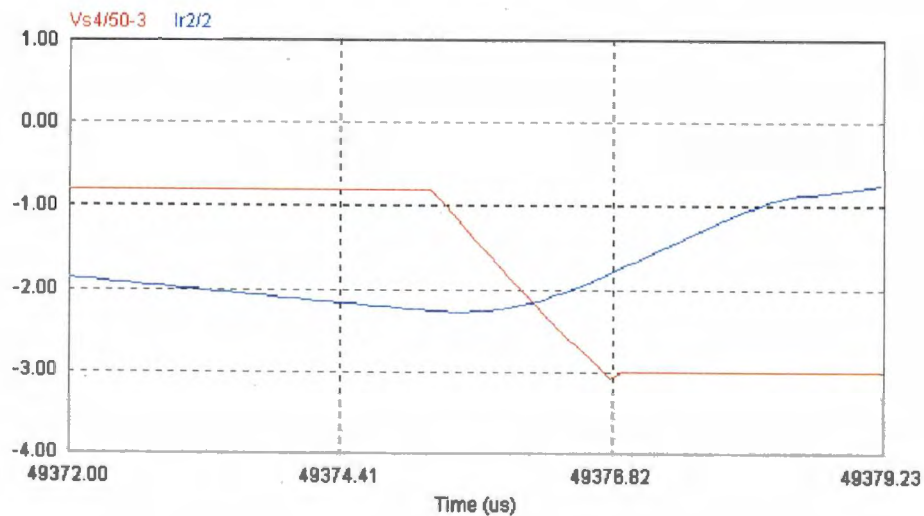
The details of switching process of S1 to S4 in buck mode are demonstrated from Figures 6.23 to 6.26 at the following conditions. The voltage source of the high voltage side is 116 V. The load resistance of the low voltage side is a 0.1 ohms. The phase shift angle of S3 leading to S1 is 0.04π , namely 1 μ s under 20 kHz switching frequency. The leakage inductance of the transformer is 0.4 μ H.

In Fig. 6.23, the experimental zero-voltage turn on of S4 is shown in (a), and the simulation waveforms are shown in (b) for comparison. There is a good agreement between (a) and (b). When S3 is gated off, I_{r2} is negative. The resonant capacitors Cr3 and Cr4 are charged and discharged, respectively. The calculated dv/dt is 46V/ μ s, the experimental value is 45 V/ μ s. After V_{s4} is discharged to the negative value, D4 is on. During this period, S4 receives an “on” signal. When I_{r2} changes the polarity, the current is diverted from D4 to S4, S4 is turning on at zero voltage. This commutation process has also been described in Fig. 3.7 of the operation principle of the buck mode.

In Fig. 6.24, the details of zero-voltage turn off of S4 are shown. When S4 is gated off, I_{r2} is positive. The resonant capacitors Cr3 and Cr4 are discharged and charged, respectively. The calculated dv/dt is 60V/ μ s, the experimental value is 58 V/ μ s. After V_{s3} is discharged to the negative value, D3 is on and V_{s4} increases to 116 V without an obvious overshoot. With this limited dv/dt of turn off voltage across S4,

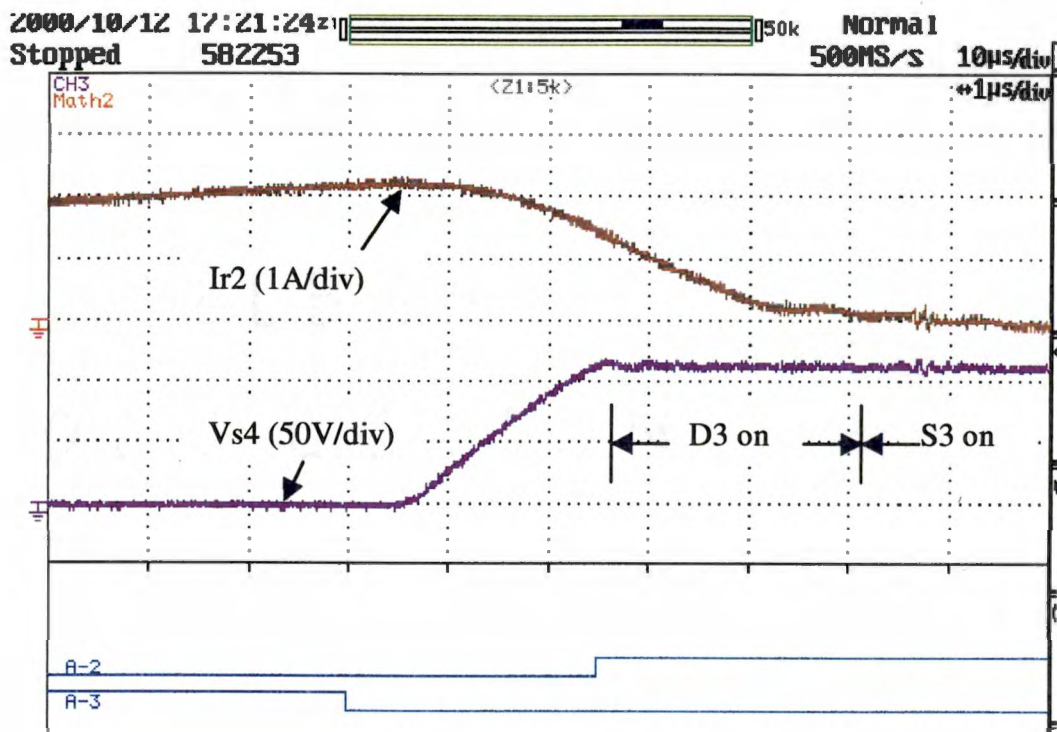


(a) Experimental zero-voltage turn on of S4 in buck mode

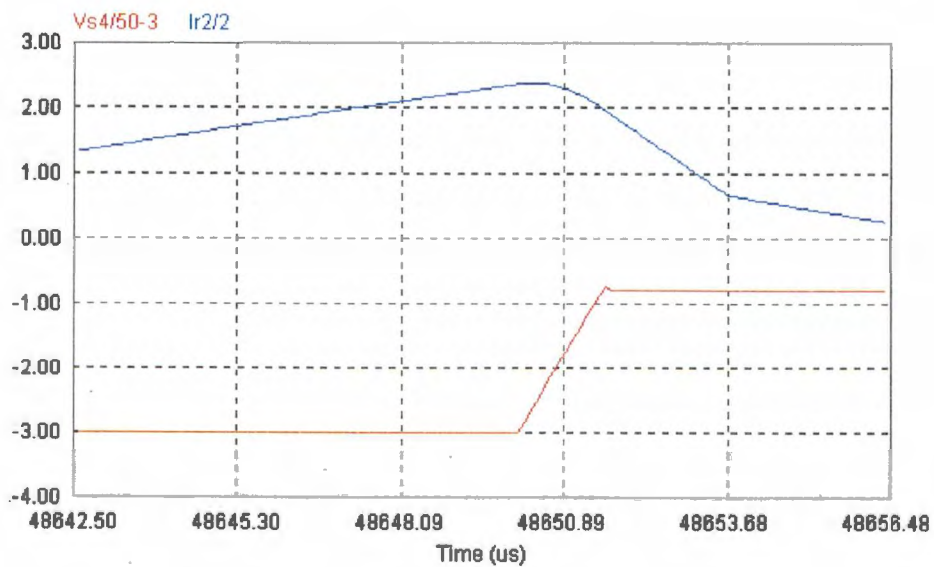


(b) Simulation zero-voltage turn on of S4 in buck mode

Fig. 6.23 Zero voltage turn on of S4 in buck mode



(a) Experimental zero-voltage turn off of S4 in buck mode



(b) Simulation zero-voltage turn off of S4 in buck mode

Fig. 6.24 Zero voltage turn off of S4 in buck mode

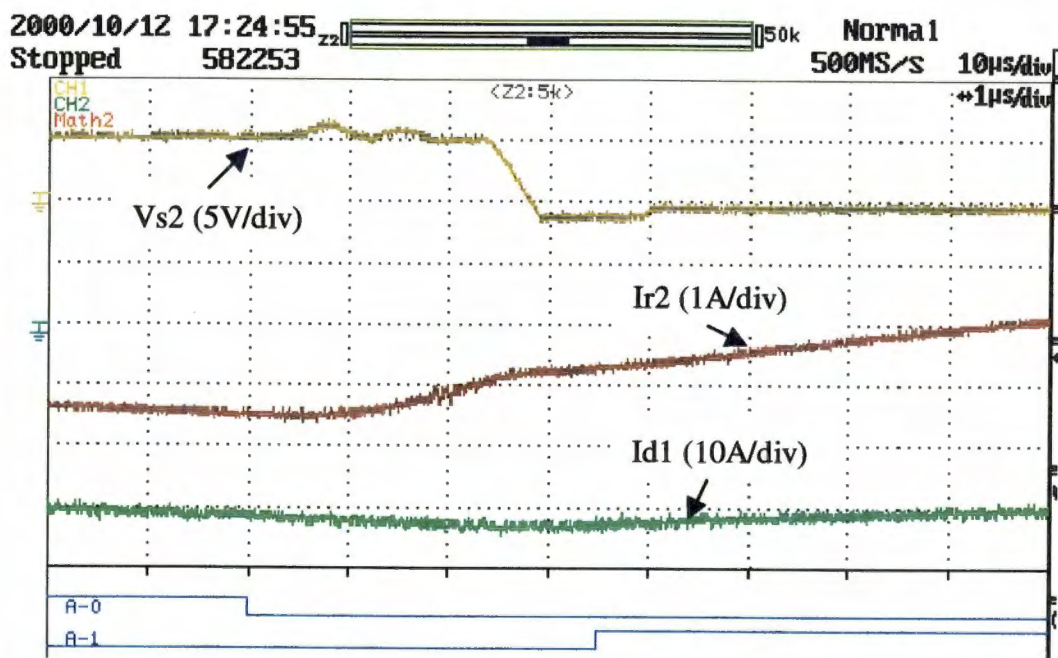


Fig. 6.25 Zero voltage turn on of S2 in buck mode

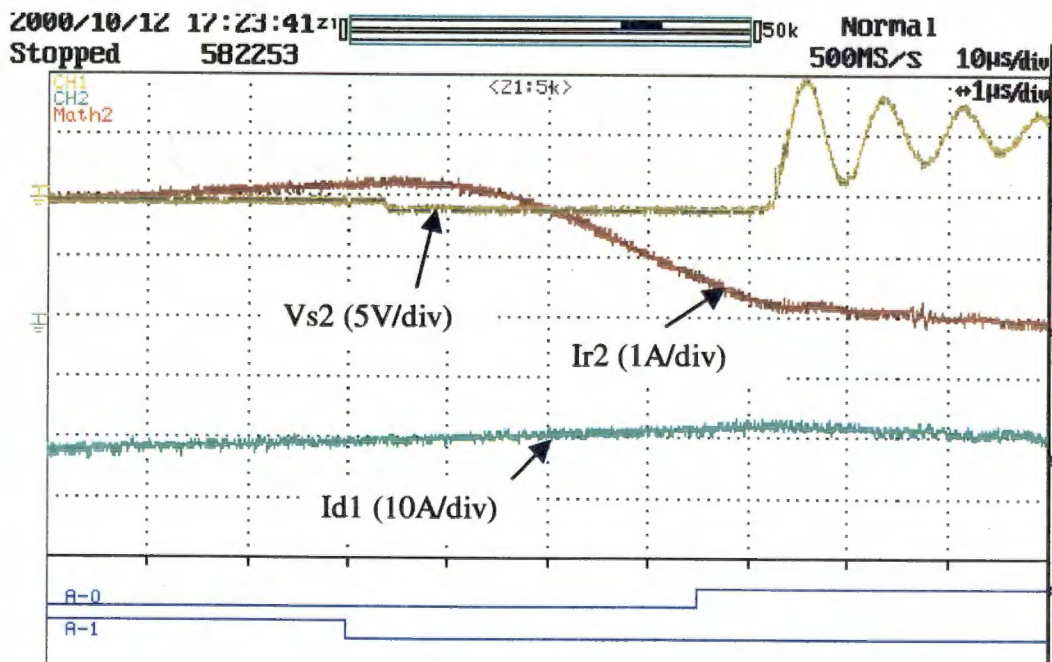


Fig. 6.26 Hard turn off of S2 in buck mode

the switching loss at turn off can be regarded as negligible or zero. Comparing Fig. 3.7 with Fig. 6.24, there is a good agreement between experimental results, simulation waveforms and the operation principles. The soft switching of S3 can be derived symmetrically.

Figures 6.25 and 6.26 show the commutation process of S2. It is seen that the turn on of S2 is a zero voltage turn on; however, the turn off of S2 is hard switching. This is because the phase shift angle of S3 leading to S1 is too small, namely only 0.04π . In this case, both experimental and simulation results show that when S2 is gated off, I_{r2} is not decreasing to the required value of soft switching shown in Fig. 3.7, which is negative and the magnitude is bigger than I_{d1} . Instead, it goes to the very positive value. Therefore D2 is conducting the current until S1 is gated on. The hard switching and the diode reverse recovery gives the oscillation of V_{s4} . Fortunately, this hard switching will not exist at a larger phase shift angle. In addition, the specified application is working at rated power, namely 1.6 kW, in which a large phase shift angle is required to provide enough power. Therefore, this hard switching is not a big concern. Similarly, the switching details of S1 can be developed symmetrically.

VI. 6 Summary

In this chapter, a prototype of 1.6 kW has been designed and built in the laboratory to evaluate the static performance of the proposed topology. The obtained

experimental waveforms show good agreement with simulation results, which confirms as follows.

- (1) The operation principles in chapter III, which include soft switching and output characteristics in both direction of power flow, are correct.
- (2) The average model derived in chapter IV is accurate.
- (3) The converter has good steady state performance in both direction of power flow.
- (4) The converter is robust with respect to the leakage inductance of the transformer, although the switching performances of the prototype with the designed $0.4 \mu\text{H}$ is better than those of $0.02 \mu\text{H}$.

CHAPTER VII

SUMMARY

VII. 1 Conclusions

A bi-directional dc-dc converter topology has been presented and evaluated for application in a fuel cell energy system.

A steady state analysis has been conducted to provide the soft switching expressions and the design equations. An average model and its small signal model have been derived and simulated to study the system dynamic performance and determine the compensation network parameters. A start up scheme has been proposed to limit inrush current and quickly build up the output voltage. A control system is designed to allow the converter to have a soft start up, to be stabilized around the operating point, to track the reference voltage and reject exogenous disturbances. A prototype design example has been included. The power components are selected by using the design equations and characteristic curves. The power circuit layout and the hardware circuits are built to have the least parasite effect and most compact packaging consideration. The control scheme is implemented by using a DSP control board. The experimental results of the open loop converter system validate the operation principle analysis and the averaged model. In addition, they show good steady state performance.

The converter demonstrates low device count (dual half-bridge topology), simplified topology (no extra device and components), an easily implemented control scheme, compact packaging, robust design (not sensitive to leakage inductance) and high efficiency (94% in the simulation and 85% in the experimental results at 1.6 kW).

Therefore, it provides one of the best solutions for the specific application to optimize the size, cost and efficiency.

VII. 2 Contributions

The main contributions of the author are outlined as follows.

- **Steady state analysis**

This new topology has not been previously studied. The steady state performance was totally unknown. The author gives a complete and thorough study to explore this problem. With circuit analysis, mathematical calculation and detailed circuit simulation, the steady state performance has been made clear by describing the principles of operation, deriving the output characteristic equation, developing design equations, drawing characteristics curves, etc. The experimental results confirm the correctness of the analysis.

- **Dynamic performance analysis including average model and small signal model derivation**

Like steady state performance, the converter's dynamic performance is also new and unknown. In addition, it is a significant challenge because no mathematical model

is available to help analyze the converter dynamics. To make things worse, the methods to derive the average model for this class of bi-directional dc-dc converters have never been addressed in the literature. This is because the isolation transformer brings in ac variables, which are hard to cancel using traditional averaging techniques. In order to solve this problem, the author develops a new method to derive the mathematical model for the proposed circuit. In this average model, the switching frequency becomes a possible variable, which is sufficiently accurate to estimate the system performance at different switching frequencies. In addition, this method also provides one valid approach to develop the models of other bi-directional dc-dc converters. Based on the average model, the dynamic performance can be evaluated in a convenient and fast way. In addition, a small signal model around a specified operating point can be calculated. The transfer function of the small signal model provides more accurate information of the system. The comparison between the simulation results of average model and the detailed circuit model confirms the correctness of average model. The experimental results verify further the correctness of the average model.

- **Start up scheme**

Start up is an important problem that needs to be solved. Because of the inherent features of the boost-operating mode of the converter, there is a large inrush current during start up that can destroy the devices as well as saturate the inductor and transformer. In addition, the large high side capacitance also slows down the start up process, which is not welcomed for the anticipated application. There is one possible

solution published in [6]. However, it needs an extra flyback winding, which will increase the cost and complicate the package. The author finds a low cost and more reliable scheme. The simulation of the average model confirms the feasibility of this scheme.

- **Control system design**

As with the above issues, the control system design is also new because the converter is new. The average model shows the converter is nonlinear. Therefore, the converter controller is divided into two parts for start up control and small signal control. The start up controller can not use the small signal model, and its scheme is separately designed and discussed in the above issue. The small signal controller is analyzed by the author thoroughly to derive the linearized model, transfer function, and root locus plot of the transfer function. Finally, a controller is designed and evaluated by trial and error. In addition, to make the transitions between two controllers smooth, the author uses a simpler, more reliable controller. This controller is convenient for real time applications and implementation. The simulation results confirm the good performance of this controller.

- **Prototype design and experimental verification**

As the converter topology and the specified application are new, the design example for selecting the power components and considerations of the power circuit layout provide a base line unit for similar applications in the future. The obtained

experimental waveforms of steady state operation confirm the analysis and simulation results.

- **Systematic study**

In this dissertation, the author provides a systematic study including circuit analysis, mathematical model derivation and analysis, control system design, performance simulation, prototype numerical design, hardware construction, software program design and analysis of experimental results. In addition, the issues involved in this process are new. Therefore, the pioneering work of the author provides a complete foundation for future improvement.

VII. 3 Recommendation for future work

In this section, directions for future investigation and improvement are recommended.

- The prototype layout needs to be modified to increase system efficiency. The experimental efficiency is not close to the simulated value. It has been determined that the main power losses are consumed by the connection resistance between C_1 and C_2 because of the poor connection. The skin effect of transformer is another main source of power loss. This problem should be solved by a new layout and a better transformer design.
- The transient response can be verified further by experimental results. The steady state performance has been verified by experimental results obtained from open

loop system control. The dynamic response of the converter under transient conditions of step changes in load and input voltage source is only verified by simulation results, not experimental results. The experimental waveforms are expected to be obtained from closed loop system to confirm the good performance of controller and simulation results.

- The Start up scheme can be verified further by experimental results. The start up scheme has also been verified by simulation results. The experimental results can further confirm the simulation.

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Chapter 6

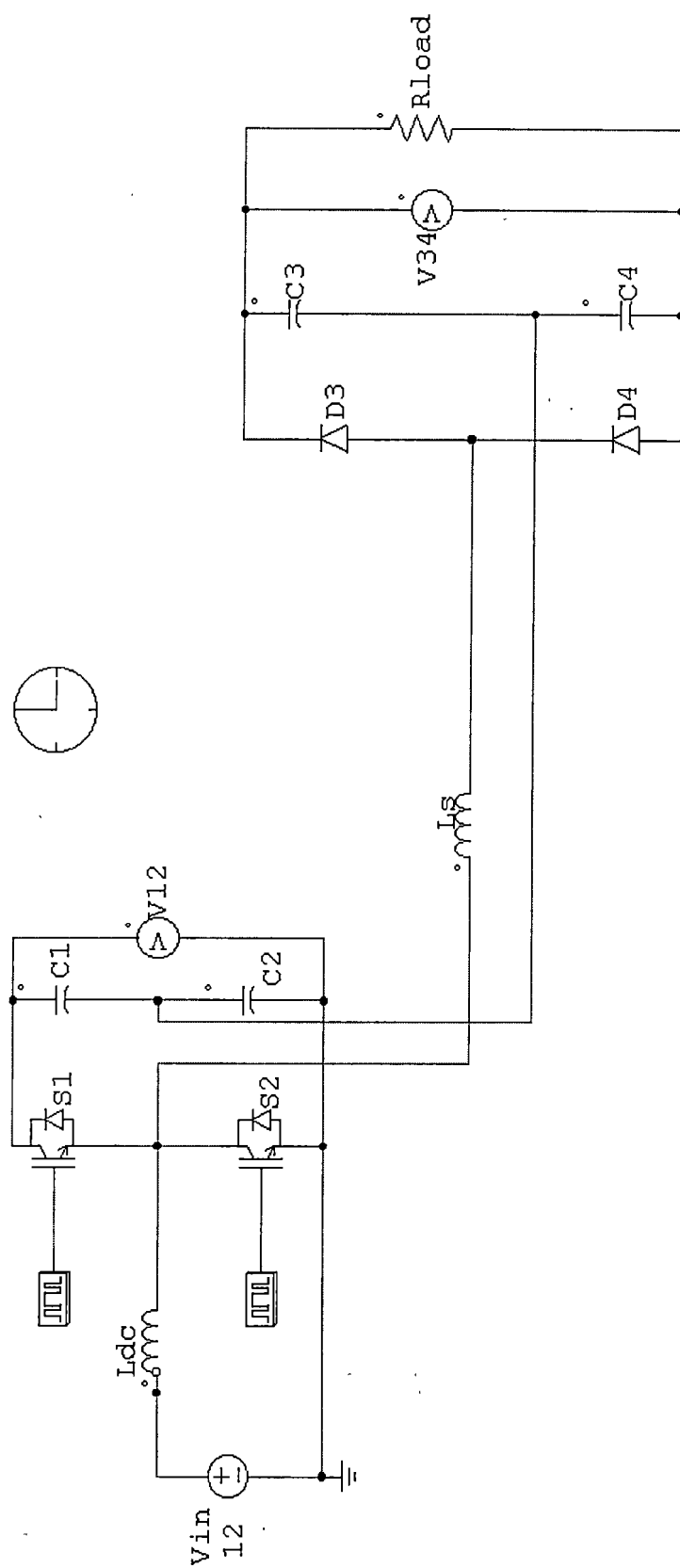
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APPENDICES

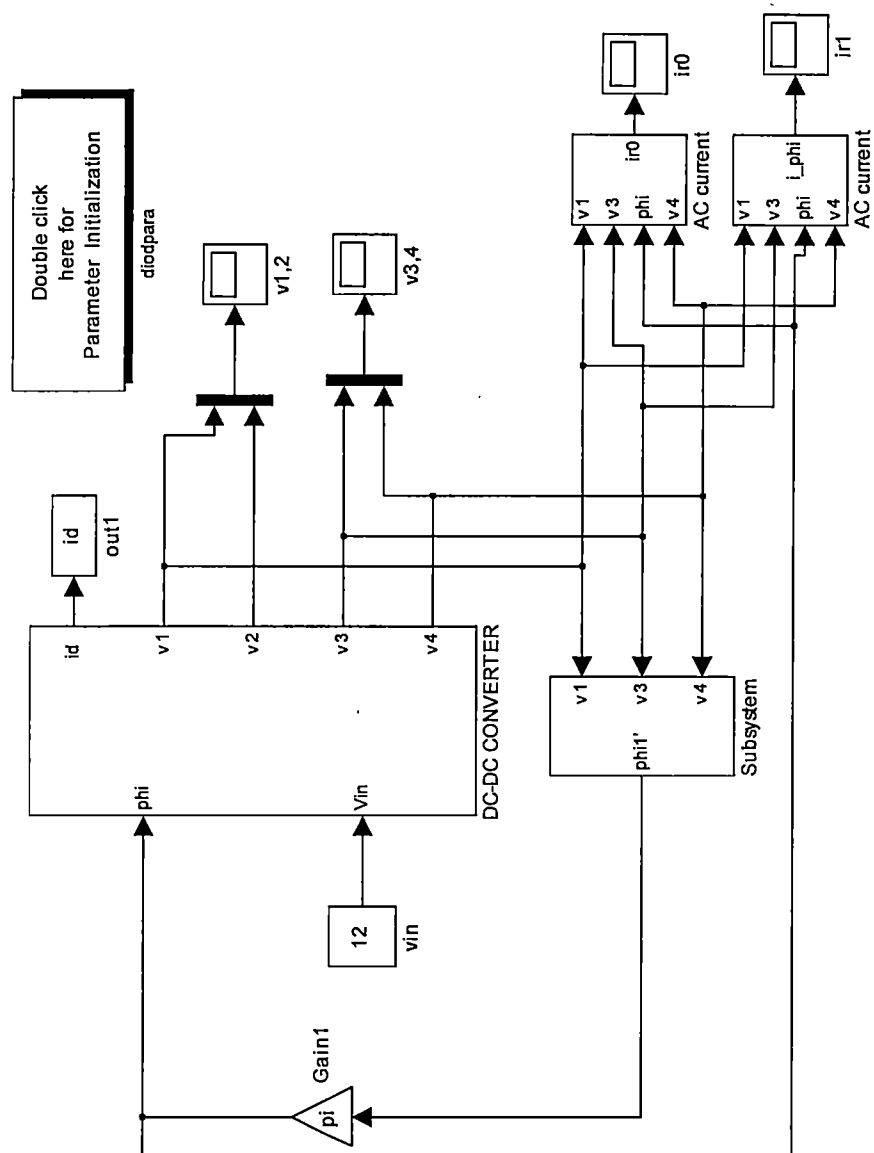
APPENDICES A

Simulation Block diagrams

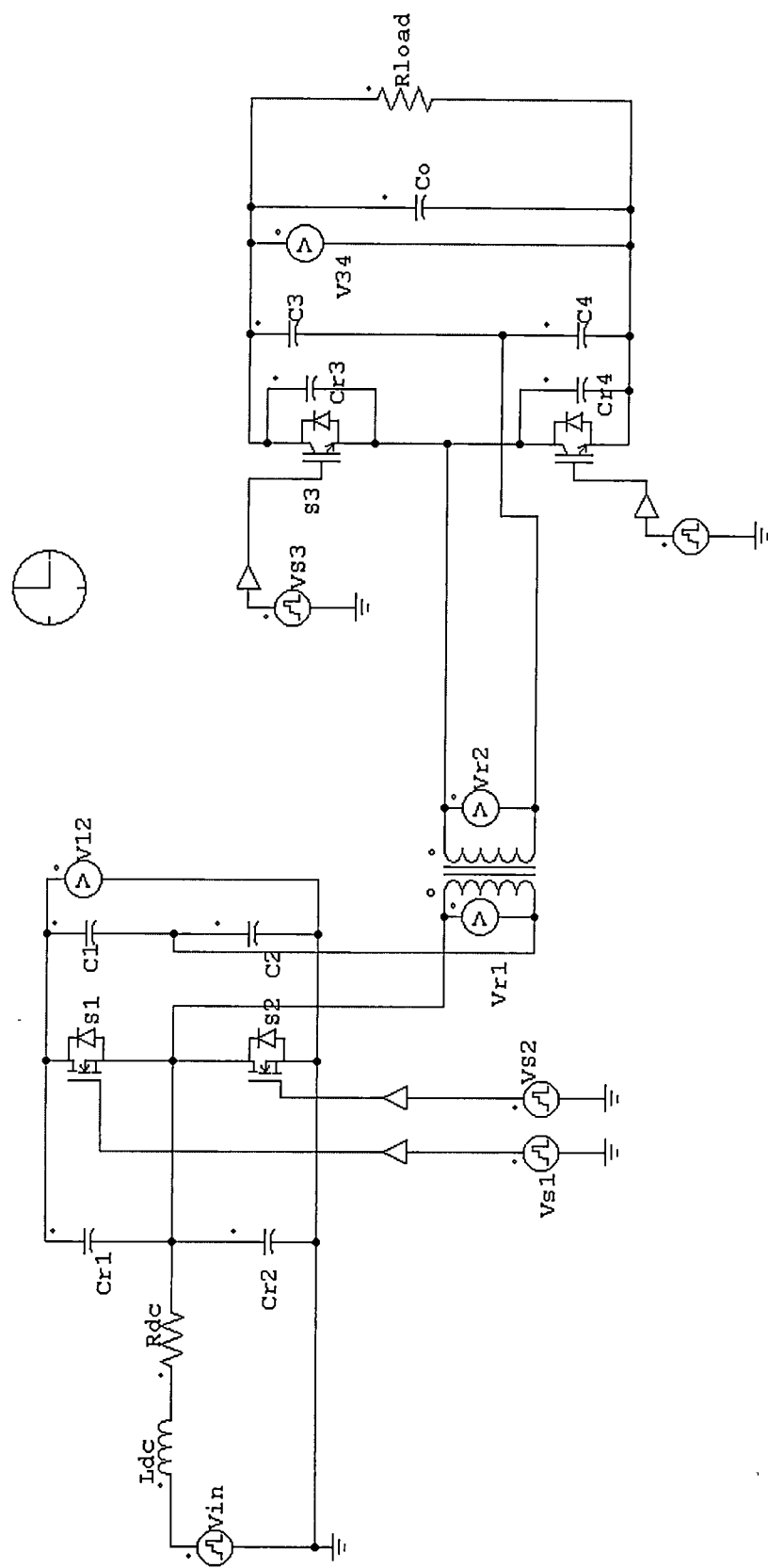
The PSIM simulation circuits of example 1



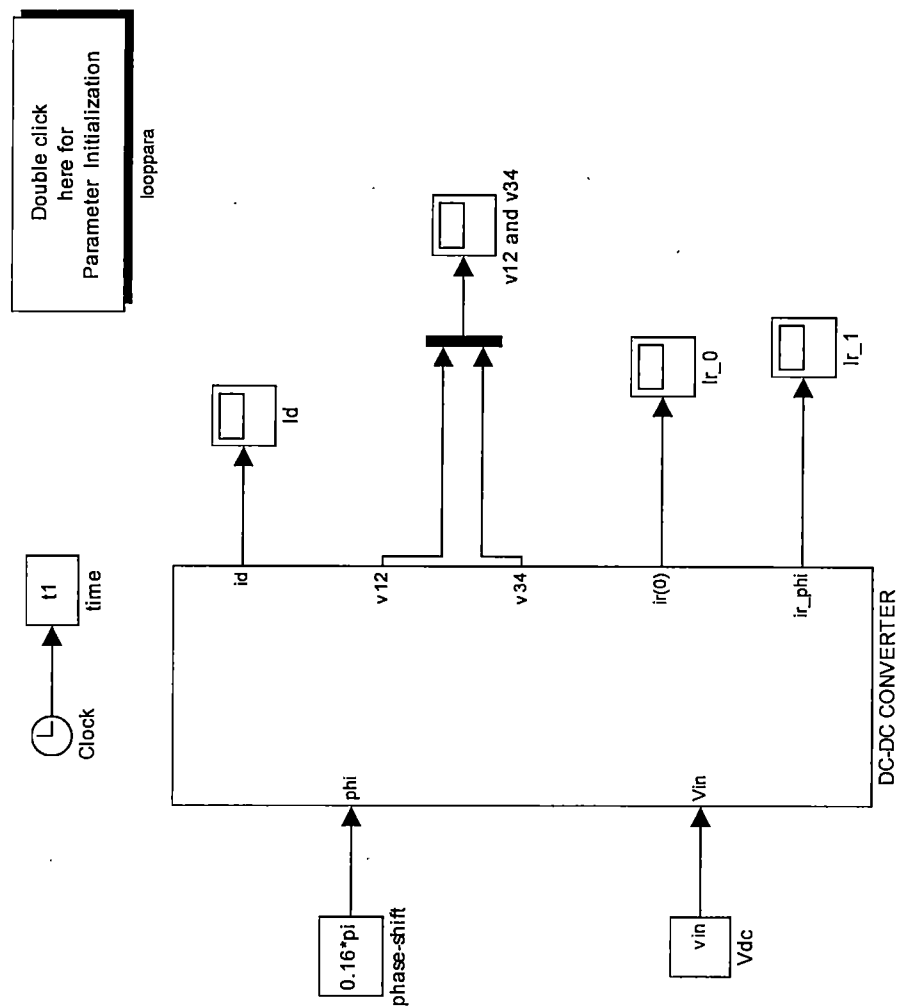
The MATLAB/SIMULINK simulation block diagram of example 1



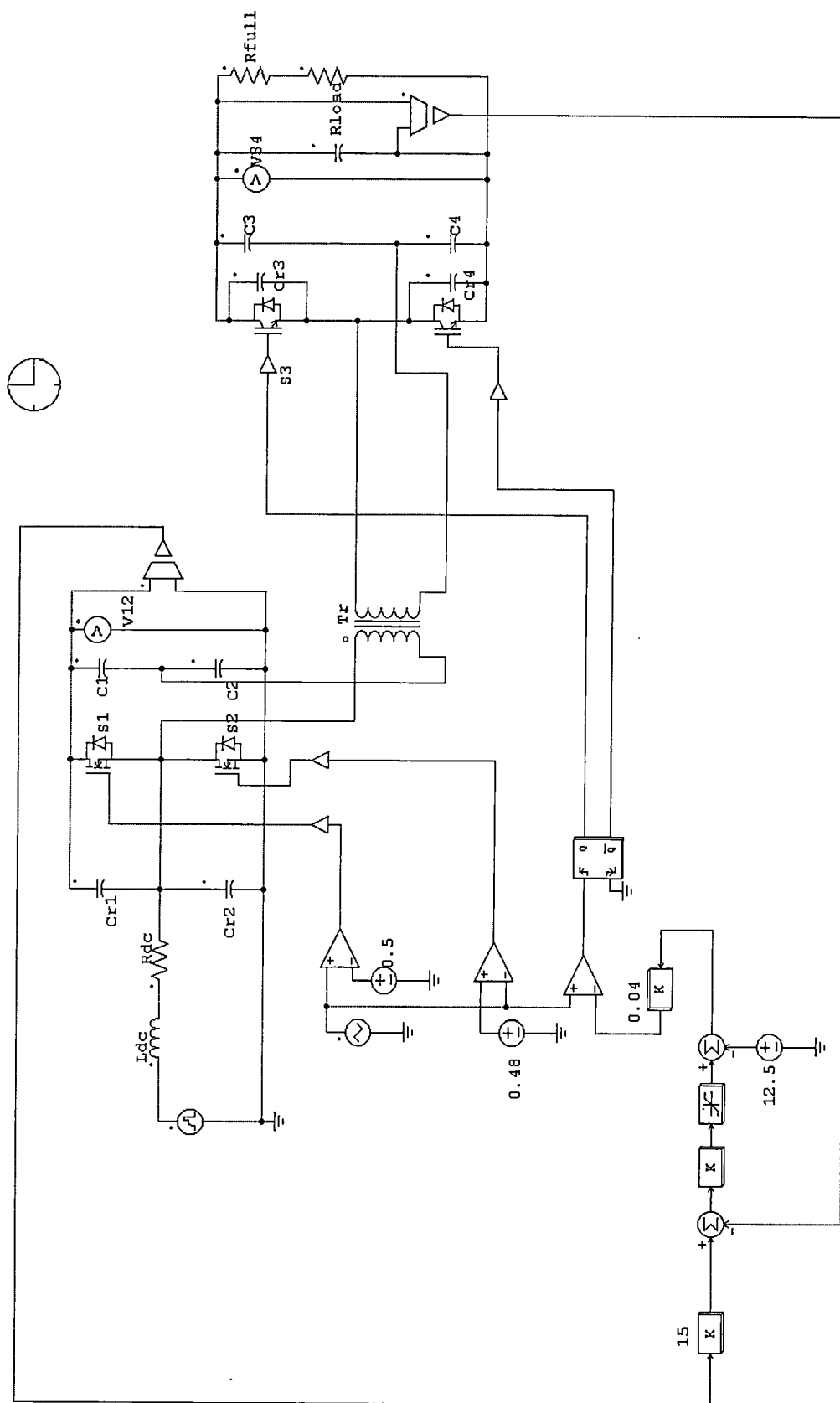
The PSIM simulation circuits of example 2



The MATLAB/SIMULINK simulation block diagram of example 2



The PSIM simulation circuits of example 3

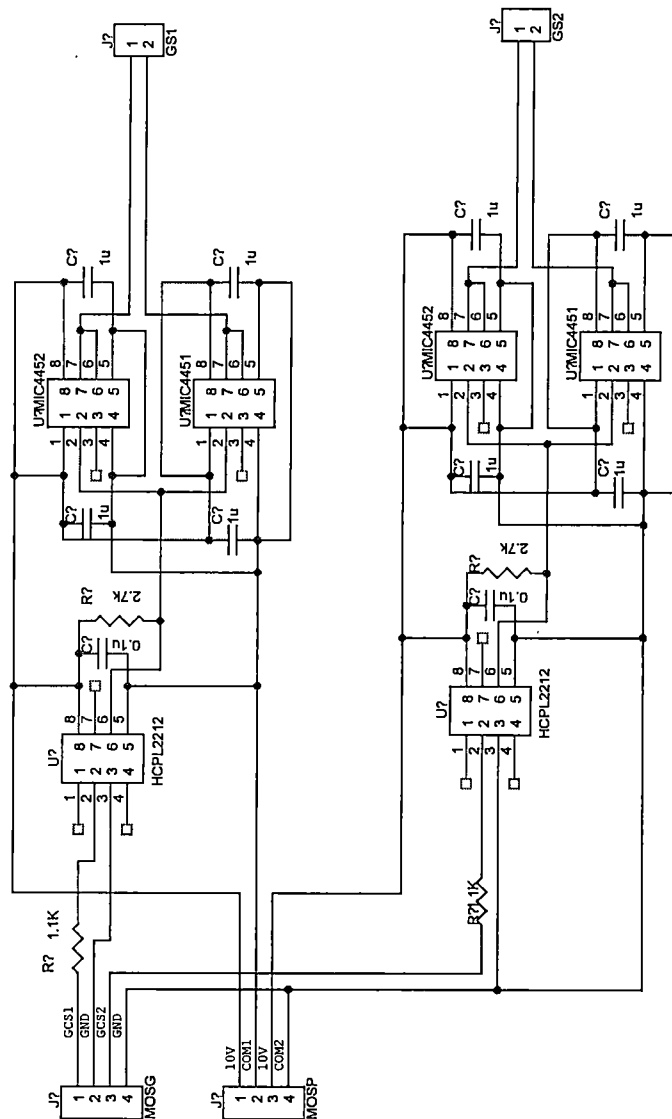


APPENDICES B

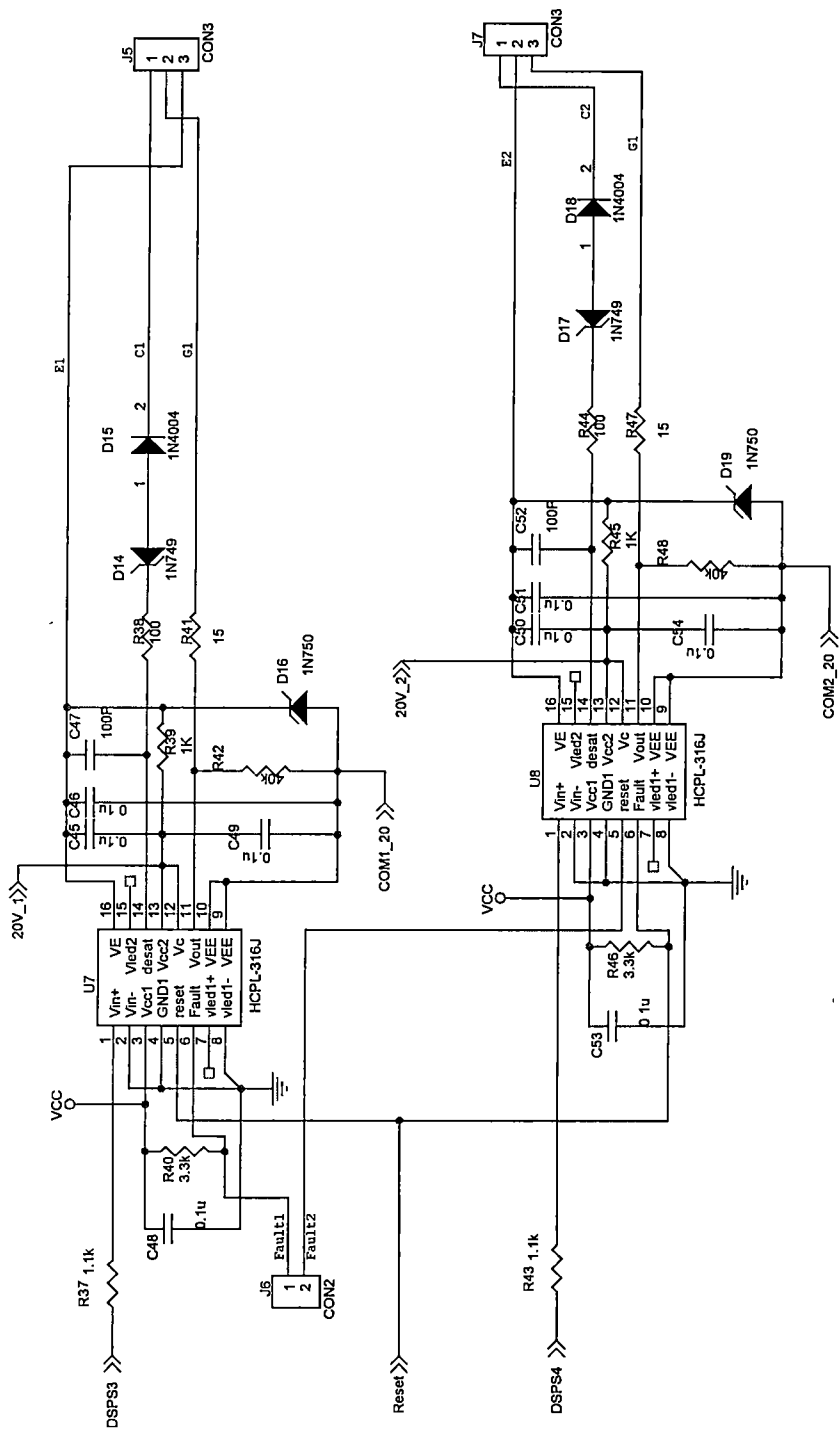
Circuit Schematics



1



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