Analysis and Control of VSC Based HVDC System under Single-Line-to-Ground Fault Conditions

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Abstract

To take full advantage of multilevel modular converter (MMC) and extend its application in high voltage direct current (HVDC) transmission systems, the ability to deal with severe unbalanced conditions, especially under single-line-to-ground (SLG) fault, is a key requirement.

This dissertation deals with the development of a fault handling strategy, which helps HVDC systems achieve continuous energy supply and desired operation performance under temporary SLG fault conditions while ensuring a smooth and fast black start for MMC-HVDC particularly if the system has to shut down when a permanent SLG fault occurs. Several related research topics will be discussed in this dissertation.

First, a steady-state model of MMC for second order phase voltage ripple prediction under unbalanced conditions is proposed. From the steady-state model, a circular relationship is found to evaluate the magnitudes and initial phase angles of different circulating current components. Moreover, the derivation of the equivalent dc impedance of a MMC is discussed as well.

Second, the analysis and control of a MMC based HVDC transmission system under three possible SLG fault conditions are discussed. Based on the derived steady state model, a novel double line frequency dc voltage ripple suppression control is proposed. This controller, together with the phase and circulating current control, could enhance the overall fault-tolerant capability of the HVDC system without additional costs.

Third, the small signal model of the capacitor charging loop in a MMC inverter is first derived according to the internal dynamics of the MMC inverter. Based on this model, a novel startup strategy incorporating an averaging capacitor voltage loop and a feedforward control is proposed for enhanced dynamic response and system stability.

Finally, a cascaded droop control scheme is proposed for multi-terminal HVDC systems to deal with dc overvoltage under onshore converter side SLG fault. Using ac voltage magnitude as an intermediate variable, the dc voltage information of offshore converters can be transferred to windfarms (WFs) and

adjust their active power generation without any communication. With such control scheme, performance of the studied four-terminal HVDC system under various fault conditions are analyzed and compared.

Table of Contents

1 Introduction 1

1.1 Background and Motivation 1

1.2 Research Objectives and Approaches 16

1.3 Dissertation Organization 17

2 Literature Review 19

2.1 Steady State Modelling of MMC under SLG Fault Condition 20

2.2 Control Schemes of Point to Point MMC-HVDC under AC Unbalanced Conditions 21

2.3 Startup Scheme 24

2.4 Control Strategies of MTDC under SLG Fault Conditions 27

2.5 Summary 32

3 Steady State Modelling of MMC under SLG Fault Conditions 33

3.1 System Configuration under SLG Fault Conditions 33

3.2 Steady-state Model for Second Order Phase Voltage Ripple Prediction 35

3.3 Steady-state Model for Circulating Current Prediction 42

3.3.1 Resistive Load 43

3.3.2 MMC Load 45

3.4 Experimental Verification 50

3.4.1 MMC Rectifier with Resistive Load under SLG Fault 51

3.4.2 MMC Inverter under SLG Fault 53

3.4.3 MMC Inverter with Second Order Voltage Input in DC Side 53

3.5 Summary 58

4 Integrated Fault-tolerant Control Scheme of MMC under SLG Fault Conditions 59

4.1 Control Scheme under SLG Fault 59

4.2 Case Study 64

4.2.1 Fault Tolerant Operation with Designed Controllers in Case 1 67
4.2.2 Fault Tolerant Operation with Designed Controllers in Case 2 76
4.2.3 Fault Tolerant Operation with Designed Controllers in Case 3 79
4.2.4 DC Voltage Margin Control 84
4.3 Discussion 90
4.4 Experimental Verification 91
4.5 Summary 95
5 Active Startup Scheme for MMC-HVDC Systems from Blackout Conditions 97
5.1 Uncontrolled Pre-charge Process of MMC 97
5.1.1 For MMCs Operating in Rectifier Mode 97
5.1.2 For MMCs Operating in Inverter Mode 101
5.2 Capacitor Charging Control of MMC Inverter 102
5.2.1 Small Signal Model of Capacitor Voltage Charging Loop 104
5.2.2 Averaging Capacitor Voltage Control 106
5.2.3 Capacitor Voltage Feedforward Control 108
5.3 Case Study 110
5.3.1 System Parameters 110
5.3.2 BTB-MMC System Connecting Two Active Terminals 111
5.3.3 BTB-MMC System Supplying Passive Loads 114
5.4 Experimental Verification 120
5.4.1 Experimental System Configuration and Parameters 120
5.4.2 Experimental Results of a Modular Multilevel Rectifier 120
5.4.3 Experimental Results with a Modular Multilevel Inverter 121
5.5 Summary 124

6 Cascaded Droop Control for DC Voltage Regulation in Multi-terminal HVDC System under SLG Fault 126

6.1 Four-Terminal HVDC Prototype 126

6.2 Cascaded Droop Control Scheme for AC Fault Ride Through 135

6.2.1 Control Mechanism 135

6.2.2 Power Flow Calculation 139

6.3 Simulation Results of MTDC during SLG Fault 141

6.3.1 Different Fault Locations 142

6.3.2 Different Reactive Power Requirement 154

6.3.3 Impact of Droop Constant 156

6.3.4 Impact of Dead-band 160

6.4 Experimental Verification 166

6.4.1 SLG Fault in Onshore Converter I 168

6.4.2 SLG Fault in Onshore Converter II 176

6.5 Summary 184

7 Conclusion and Future Work 186

7.1 Conclusion 186

7.2 Recommended Future Work 188

References 191

Vita 204

List of Tables

Table 1-1. Comparison of site areas among LCC, two-level VSC and MMC based HVDC systems [38]. 7

Table 1-2. Selected VSC-HVDC projects. 9

Table 1-3. Selected MTDC projects. 13

Table 3-1. A/D channel assignment for DS1103. 50

Table 3-2. Main circuit parameters of MMC prototype. 52

Table 4-1. Main circuit parameters of MMC-HVDC in simulation model. 65

Table 5-1. Main circuit parameters of MMC-HVDC. 110

Table 6-1. Main circuit parameters of real system and scaled-down platform. 131

Table 6-2. Parameters for all controllers used in simulation model. 143

Table 6-3. Reference and power capacity settings in case 1 144

Table 6-4. Reference and power capacity settings in case 2 146

Table 6-5. Operation mode transition in case 1 with onshore I side SLG fault. 168

Table 6-6. Operation mode transition in case 2 with onshore I side SLG fault. 171

Table 6-7. Operation mode transition in case 3 with onshore I side SLG fault. 174

Table 6-8. Operation mode transition in case 1 with onshore II side SLG fault. 176

Table 6-9. Operation mode transition in case 2 with onshore II side SLG fault. 179

Table 6-10. Operation mode transition in case 3 with onshore II side SLG fault. 181

List of Figures

Figure 1-1. General layout of LCC-HVDC system using thyristor cells [6]. 2

Figure 1-2. General layout of VSC-HVDC system using IGBT cells [6]. 2

Figure 1-3. Configurations of (a) two-level converter, (b) neutral point clamped (NPC) three-level converter, and (c) flying capacitor (FC) three-level converter. 4

Figure 1-4. (a) Circuit configuration of a MMC with (b) half-bridge cell, (c) full-bridge cell and (d) clamp-double cell. 5

Figure 1-5. Output ac voltage of a (a) two-level converter, (b) three-level converter, and (c) MMC. 6

Figure 1-6. Operating configuration of HVDC system (a) symmetrical monopole, (b) asymmetrical monopole with metallic return, (c) asymmetrical monopole with ground return, (d) bipole with metallic neutral, (e) bipole with ground electrodes, (f) multi-terminal. 8

Figure 1-7. Multi-terminal HVDC topologies: (a) radial, (b) ring, (c) lightly meshed, (d) densely meshed. 11

Figure 1-8. System angle stability analysis with (a) TPT and (b) SPS in [63]. 14

Figure 1-9. System voltage stability analysis with (a) three phase tripping and (b) single pole switching. 15

Figure 2-1. Control diagram of dc current ripple elimination in [77]. 22

Figure 2-2. Diagram of the circulating current suppressing controller in [83]. 22

Figure 2-3. Diagram of dc voltage ripple suppressing control (DCVRSC) in [80]. 23

Figure 2-4. Startup schemes with auxiliary passive components. 25

Figure 2-5. Diagram of constant charging current control in [102]. 27

Figure 2-6. Control of damping resistor in [109]. 28

Figure 2-7. De-loading methods used in [110] for a fully rated converter wind turbine. 29
Figure 2-8. DC voltage versus active power characteristics with (a) dc voltage margin control and (b) dc voltage droop control. 30
Figure 2-9. Single line diagram of the four-terminal HVDC system in [111]. 31
Figure 2-10. Single line diagram of the four-terminal series HVDC system in [114]. 31
Figure 3-1. Single line diagram of a MMC-HVDC transmission system. 34
Figure 3-2. Diagram of dual current control. 34
Figure 3-3. Single phase equivalent circuit of the MMC. 35
Figure 3-4. Equivalent circuit of the circulating current. 43
Figure 3-5. Equivalent circuit of the second order dc voltage ripple under SLG fault conditions. 49
Figure 3-6. Experimental test and measurement setup. 51
Figure 3-7. Configuration of the experimental system with phase C open. 52
Figure 3-8. Comparison between experimental and calculation results of circulating current in MMC rectifier under SLG fault. 53
Figure 3-9. Comparison between experimental and calculation results of circulating current in MMC inverter under SLG fault. 54
Figure 3-10. Configuration of the experimental system. 55
Figure 3-11. Second order voltage source using an H bridge. 55
Figure 3-12. Experimental waveforms with $v_2 = 6$, $R_a = 0$. 55
Figure 3-13. Experimental waveforms with $v_2 = 12$, $R_a = 0$. 56
Figure 3-14. Experimental waveforms with $v_2 = 12$, $R_a = 3$. 56
Figure 3-15. Current loop control experimental waveforms with $v_2 = 12$. 56

Figure 3-16. Comparison between experimental and calculated results..... 57

Figure 4-1. Control scheme of MMC under unbalanced condition. 60

Figure 4-2. Diagram of positive sequence current control. 62

Figure 4-3. Diagram of negative sequence current suppression. 62

Figure 4-4. Control diagram of zero sequence current. 63

Figure 4-5. Control diagram for dc voltage ripple suppression. 63

Figure 4-6. Open-loop bode plot of dc voltage ripple control. 64

Figure 4-7. Different SLG fault locations. 66

Figure 4-8. Rectifier side SLG fault in case 1. 67

Figure 4-9. DC voltage and its spectrum with an SLG fault in case 1 (MMC_1 side)..... 68

Figure 4-10. Simulation waveforms of the studied system under an SLG fault in case 1 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) transformer primary side ground current, (c) phase currents before the fault point, (d) fault current, (e) phase currents after the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm. 69

Figure 4-11. DC voltage with single pole switching in case 1 (MMC_1 side). 71

Figure 4-12. Simulation waveforms of the studied system under an SLG fault with single pole switching in case 1 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) transformer primary side ground current, (c) phase currents before the fault point, (d) fault current, (e) phase currents after the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase

voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm. 72

Figure 4-13. Inverter side SLG fault in case 1(MMC_2 side). 73

Figure 4-14. DC voltage and its spectrum with an SLG fault in case 1 (MMC_2 side)..... 74

Figure 4-15. Simulation waveforms of the studied system under an SLG fault in case 1 (MMC_2 side). **MMC_2 side:** (a) AC grid ground current, (b) transformer primary side ground current, (c) phase currents after the fault point, (d) fault current, (e) phase currents before the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_1 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm. 75

Figure 4-16. Rectifier side SLG fault in case 2. 76

Figure 4-17. DC voltage and its spectrum with SLG fault in case 2 (MMC_1 side). 76

Figure 4-18. Simulation waveforms of the studied system under an SLG fault in case 2 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) phase current in the Y side of the Y/Δ transformer, (c) phase currents before the fault point, (d) fault current, (e) phase current in the delta side of the Y/Δ transformer, (f) dc bus currents in the sending and receiving end, (g) phase voltage in the delta side of the Y/Δ transformer, (h) phase voltage in the Y side of the Y/Δ transformer, (i) active and reactive power, (j) negative sequence current components, (k)

capacitor voltages of SMs in phase A upper arm; and (l) dc buses to ground voltage, **MMC_2 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm. 78

Figure 4-19. Rectifier side SLG fault in case 3. 80

Figure 4-20. DC voltage and its spectrum with SLG fault in case 3 (MMC_1 side). 81

Figure 4-21. Simulation waveforms of the studied system under SLG fault in case 3 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) grid side phase currents, (c) fault current, (d) converter side phase currents, (e) converter side phase voltage, (g) active and reactive power, (h) d and q axis negative sequence current, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (f) AC grid ground current (j) converter side phase voltage, (k) converter side phase current, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm. 81

Figure 4-22. DC voltage and its spectrum with single pole switching in case 3 (MMC_1 side fault). 83

Figure 4-23. Simulation waveforms of the studied system under SLG fault with single pole switching in case 3 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) grid side phase currents, (c) fault current, (d) converter side phase currents, (e) converter side phase voltage, (g) active and reactive power, (h) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (f) AC grid ground current (j) converter side phase voltage, (k) converter side phase current, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm. 83

Figure 4-24. Control diagram of dc voltage margin control. 84

Figure 4-25. System configuration for case 1. 85
Figure 4-26. DC voltages for case 1, without dc voltage margin control. 85
Figure 4-27. Simulated results for case 1, with dc voltage margin control. 86
Figure 4-28. Operation points of MMC_1 and MMC_2 with dc voltage margin control. 87
Figure 4-29. Simulated results for case 2, with (left column) and without (right column) dc voltage margin control. 88
Figure 4-30. Simulated results for case 3, with dc voltage margin control. 89
Figure 4-31. Simulated results for case 4, with dc voltage margin control. 89
Figure 4-32. Experimental results of a MMC rectifier under SLG fault, without negative sequence phase current control. 92
Figure 4-33. Experimental results of a MMC rectifier under SLG fault, with negative sequence phase current control. 93
Figure 4-34. Experimental results of a MMC rectifier under SLG fault, with negative sequence phase current and circulating current control. 94
Figure 4-35. Transient performance of a MMC inverter when SLG fault occurs. 94
Figure 4-36. Transient performance of a MMC inverter when negative sequence current control starts. 94
Figure 4-37. Transient performance of a MMC inverter when circulating current control is activated. 95
Figure 5-1. Charging loops between phase A and B in a MMC rectifier during pre-charge stage. 98
Figure 5-2. Charging loop between phase A and B with (a) $i_a > 0$, $i_b < 0$, and (c) its equivalent circuit, (b) $i_a < 0$, $i_b > 0$, and (d) its equivalent circuit. 99
Figure 5-3. (a) Charging loop, (b) three-phase equivalent circuit, and (c) dc side equivalent circuit

of a MMC inverter during uncontrolled pre-charge period. 101

Figure 5-4. Overall control block diagram of proposed capacitor charging control. 103

Figure 5-5. Bode diagram of $\tilde{i}_c$ to dc 107

Figure 5-6. Compensated open loop bode diagrams. 107

Figure 5-7. Equivalent circuit of capacitor charging loop in (a) a submodule of MMC, and (b) a phase unit of MMC inverter. 109

Figure 5-8. BTB-MMC system with two active terminals. 111

Figure 5-9. Selected simulation results of the rectifier station with two active terminals, (a) phase current, (b) arm current in phase A, (c) arm current in phase B, (d) arm current in phase C, (e) dc voltage, (f) capacitor voltages in phase A, (g) capacitor voltages in phase B, (h) capacitor voltages in phase C. 113

Figure 5-10. Duty cycle of (a) rectifier, (b) inverter with two active terminals when SVM is adopted. 113

Figure 5-11. BTB-MMC system supplying resistive load. 114

Figure 5-12. Selected simulation results of (a) phase current, (b) arm current in phase A, (c) dc voltage, (d) capacitor voltages in phase A in MMC_1 (top) and MMC_2 (bottom) station with only averaging capacitor voltage control and $N = 4$. 115

Figure 5-13. (a) Average capacitor voltage, circulating current and their references, (b) Modulation index m_c, with only average capacitor voltage control and $N = 4$. 116

Figure 5-14. Selected simulation results of (a) phase current, (b) arm current in phase A, (c) dc voltage, (d) capacitor voltages in phase A in MMC_1 (top) and MMC_2 (bottom) station with only capacitor voltage feedforward control and $N = 4$ 117

Figure 5-15. (a) Average capacitor voltage and its reference, (b) Modulation index m_c, with only

capacitor voltage feedforward control and $N = 4$..... 117

Figure 5-16. Open-loop bode plot of $\tilde{i}_c$ to dc with different number of SMs per arm..... 119

Figure 5-17. Selected simulation results in MMC_2 station, (a): (I) phase current, (II) arm current in phase A, (III) dc voltage, (IV) capacitor voltages in phase A, (b) average capacitor voltage and its reference, and (c) modulation index m_c with capacitor charging control and $N = 10$ 119

Figure 5-18. Selected simulation results in MMC_2 station, (a): (I) phase current, (II) arm current in phase A, (III) dc voltage, (IV) capacitor voltages in phase A, (b) average capacitor voltage and its reference, and (c) modulation index m_c with capacitor charging control and $N = 20$..... 120

Figure 5-19. Configurations of the experimental system..... 121

Figure 5-20. Experimental results of MMC inverter with passive load, (a) dc voltage and capacitor voltage in phase B, (b) dc and phase current, (c) arm current in phase B, (d) arm current in phase C, (e) dc voltage and its reference, (f) duty cycle m_s in dq axis..... 122

Figure 5-21. Experimental results with passive load, (a) capacitor voltage in phase B, (b) arm current in phase B and phase current, (c) average capacitor voltage and its reference, (d) circulating current and its reference in phase B, (e) modulation index m_c, (f) capacitor voltage in phase A..... 123

Figure 5-22. Experimental results when grid connected, (a) capacitor voltage in phase B, (b) arm current in phase B and phase current, (c) average capacitor voltage and its reference, (d) circulating current and its reference in phase B, (e) modulation index m_c, (f) capacitor voltage in phase A..... 124

Figure 6-1. Four -terminal HVDC in the NPCC system..... 128

Figure 6-2. Dc grid topologies for comparison: (a) point-to-point, (b) ring, and (c) meshed. ... 128

Figure 6-3. Cost comparisons with different percentages of wind power transfer requirement

after dc short circuit fault. Continued. 129

Figure 6-4. System configuration for the four -terminal HVDC platform. 130

Figure 6-5. AC voltage regulation in offshore converter station. 131

Figure 6-6. Power control in windfarm emulator. 131

Figure 6-7. Simulation results with active power step in windfarms. 132

Figure 6-8. Simulation results with reactive power step in windfarms. 133

Figure 6-9. Simulation results with voltage magnitude step in windfarms. 134

Figure 6-10. Cascaded droop control in four -terminal HVDC platform. 137

Figure 6-11. Cascaded droop control with dead-band. 137

Figure 6-12. Implementation of cascaded droop control. 138

Figure 6-13. Variables in power flow calculation in the MTDC system. 139

Figure 6-14. Flow chart of the iteration for dc power flow calculation. 140

Figure 6-15. Studied SLG fault scenarios. 143

Figure 6-16. Simulation model for higher d axis current priority 143

Figure 6-17. Simulation results with SLG fault in onshore converter I (case 1). 145

Figure 6-18. Simulation results with SLG fault in onshore converter I (case 2). 147

Figure 6-19. Simulation results with SLG fault in onshore converter I (case 3). 148

Figure 6-20. Performance comparison when i_d has higher priority and healthy converter has sufficient power capacity. 149

Figure 6-21. Performance comparison when i_d has higher priority and healthy converter has insufficient power capacity. 151

Figure 6-22. Performance comparison when i_q has higher priority and healthy converter has insufficient power capacity. 152

Figure 6-23. Performance comparison between three studied cases. 153

Figure 6-24. Performance change with different reactive power requirements..... 155

Figure 6-25. Performance with different droop constants in v_{ac} - P droop control. 157

Figure 6-26. Performance with different droop constants in v_{dc} - v_{ac} droop control..... 158

Figure 6-27. Performance with different combination of droop constants. 159

Figure 6-28. Performance with different dead-bands in v_{dc} - v_{ac} droop when Z_{lk_WF1} = 0.05 pu. 161

Figure 6-29. Performance with different dead-bands in v_{ac} - P droop when Z_{lk_WF1} = 0.05 pu. . 162

Figure 6-30. Performance with different dead-bands in v_{dc} - v_{ac} droop when Z_{lk_WF1} = 0.02 pu. 164

Figure 6-31. Performance with different dead-band in v_{ac} - P droop when Z_{lk_WF1} = 0.02 pu.... 165

Figure 6-32. Four -terminal HVDC platform. 167

Figure 6-33. Communication structure of the four-terminal HVDC platform. 167

Figure 6-34. Experimental results in case 1 with onshore I side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value. 170

Figure 6-35. Comparison between experimental and calculation results in case 1 with onshore I side fault. 170

Figure 6-36. Experimental results in case 2 with onshore I side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value. 173

Figure 6-37. Comparison between experimental and calculation results in case 2 with onshore I side fault. 173

Figure 6-38. Experimental results in case 3 with onshore I side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value. 175

Figure 6-39. Comparison between experimental and calculation results in case 3 with onshore I side fault. 176

Figure 6-40. Experimental results in case 1 with onshore II side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value. 178
Figure 6-41. Comparison between experimental and calculation results in case 1 with onshore II side fault. 178
Figure 6-42. Experimental results in case 2 with onshore II side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value. 180
Figure 6-43. Comparison between experimental and calculation results in case 2 with onshore II side fault. 181
Figure 6-44. Experimental results in case 3 with onshore II side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value. 183
Figure 6-45. Comparison between experimental and calculation results in case 3 with onshore II side fault. 183

1 Introduction

This chapter starts with the introduction of the background of this research. Then the state-of-art research is surveyed and summarized. Based on the literature review, the associated challenges in each focused area are examined. Finally, the research objectives, approaches, as well as the organization of this dissertation are presented.

1.1 Background and Motivation

Since the first high-voltage direct-current (HVDC) transmission link was successfully commissioned in 1954 on the Swedish east coast, hundreds of HVDC projects have been put into service in recent decades [1]-[4]. Compared to the traditional high voltage alternative current (HVAC) transmission system, HVDC has low losses, reduced environmental/visual impact, and lower cost for large-scale offshore windfarms and power transmission with long distance [5]. It is also capable of exchanging power between asynchronous ac systems and supplying several ancillary services, e.g. voltage support, frequency support and oscillation damping, etc. In addition, through electrical converters at the HVDC station, system security can be greatly enhanced by more degrees of flexibility and control of ac grids.

In terms of current turn off capability, the HVDC converter can be classified into two groups. The first group utilizes line-commutated current-source converters (LCC) with direct-light-triggered or electrically-triggered tyristors, as illustrated in Figure 1-1 [6]. Although LCC based HVDC (LCC-HVDC) has high power capacity, low cost, mature technology, and dc fault current controllability, it requires reactive power compensation, relies on strong ac grid and the minimum short circuit capacity should be higher than two times that of converter ratings [7] [8].

The other group is the emerging voltage-source converters based HVDC (VSC-HVDC), with insulated-gate bipolar transistor (IGBT) as the basic modules, which is illustrated in Figure 1-2 [6]. Capable of regulating both magnitude and phase angle of ac terminal voltage, VSC-HVDC technology supplies several key advantages over HVAC and LCC-HVDC, such as compact station footprint, better

use of right-of-way, black start capability, reactive power support, and fast active power reversal without changing dc polarities [9]-[11].

Furthermore, the two dc conductors in VSC-HVDC can normally be laid close together [5]. Consequently, generated by the same dc current with opposite directions, the magnetic fields almost cancel each other, leaving a quite low residual value. Moreover, the converter stations are always enclosed in a building, and dc cables can be laid underground or undersea and become invisible. In addition, employing mass impregnated (MI) or cross-linked polyethylene (XLPE) dc cable, the risk of oil spill (as in paper-oil-insulated dc cables) is eliminated. All these contribute to a very low environmental impact for VSC-HVDC transmission system.

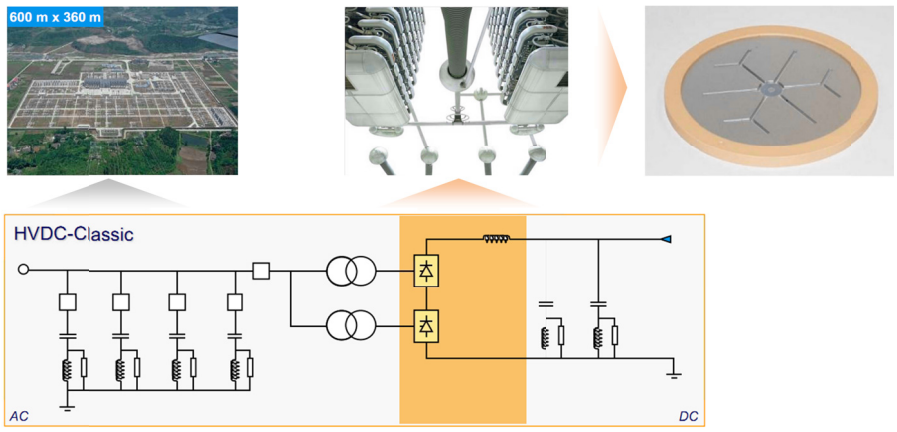


Figure 1-1. General layout of LCC-HVDC system using thyristor cells [6].

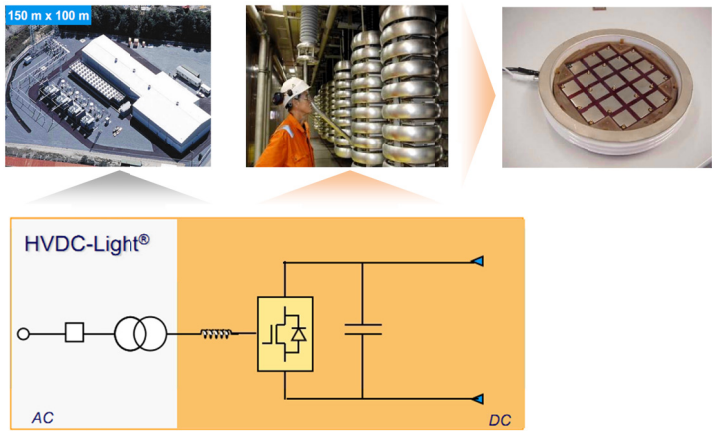


Figure 1-2. General layout of VSC-HVDC system using IGBT cells [6].

Among the VSC-HVDC systems, there are mainly three topologies:

1. Two-level and three-level converters

As shown in Table 1-2, VSC-HVDC projects were all built by ABB before 2010, using either two-level or three-level converters. The configurations are given in Figure 1-3(a), (b) and (c), respectively. However, because of the following key issues, the application of these topologies is greatly impeded:

1) Difficulty in voltage balancing of power devices

Due to the limited voltage rating (e.g., max 3.3 kV for IGBT), power devices need to be connected in series to withstand the dc voltage in the HVDC system (normally, tens or hundreds of kV). However, the different parasitic and/or operating temperature of these series connected devices will unavoidably lead to unequal steady-state blocking voltage distribution. During transient processes, the different reverse recovery charge, turn on and turn off time of semiconductor devices will also induce uneven voltage distribution [12] [13]. To deal with this issue, several approaches could been used, and the most widely used ones are listed as follows:

- Put resistors in parallel with each semiconductor device. In practice, the resistance is around 1/3 – 1/5 of the blocking resistance of devices. Lower resistance induces better voltage equalization but higher loss.
- Unbalanced blocking voltage distribution caused by reverse recovery charge difference can be minimized by RC snubber circuits connected in parallel to each semiconductor device. Generally, higher snubber capacity implies lower unbalances of voltage distribution.
- By using strong gate drive current with high di/dt, the turn-on delay time of devices and thus voltage deviation can be reduced. The snubber circuit in parallel with each device also has a positive impact on the dynamic voltage sharing. Its capacitor helps to reduce voltage charging rate while resistance can damp oscillations and limit capacitor discharging current.

However, these approaches will introduce either power losses, or complicated gate drive circuits, which induce high cost and low system reliability.

2) Low efficiency

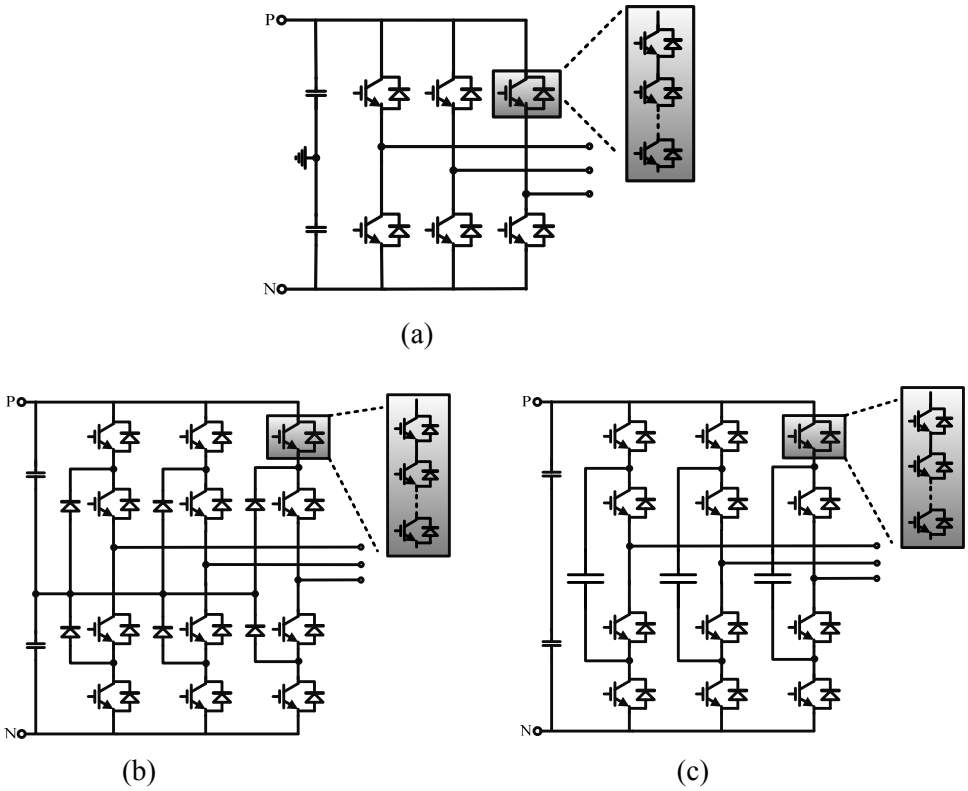


Figure 1-3. Configurations of (a) two-level converter, (b) neutral point clamped (NPC) three-level converter, and (c) flying capacitor (FC) three-level converter.

Adopting pulse width modulation (PWM) technology, the switching frequency of two-level and three-level converters normally ranges between 1 kHz – 2 kHz [13]. Increasing the switching frequency will improve output voltage quality and enable smaller LC filter, but leads to higher switching loss and thus lower efficiency. According to [14] [16], the losses of two-level and three-level converters are around 3% and 2.2 %, respectively, while LCC has an loss of 0.8 %.

In addition, for neutral point clamped (NPC) and flying capacitor (FC) converters, the design and control complexity will increase significantly with higher voltage levels, making them unsuitable for high voltage and high power applications.

2. Modular multilevel converters (MMC)

MMC was first introduced by R. Marquart in 2001[17], and since then tremendous research efforts have been done focusing on the modulation schemes [18]-[20], control strategies [21]-[23], modelling

[24], [25] and protection [26]-[28]. The configuration of a MMC is shown in Figure 1-4(a). Each phase leg of the MMC consists of one upper and one lower arm connected in series between the dc terminals. N series-connected sub-modules (SMs) and one arm inductor L_{arm} form an arm. Each SM can be realized by a half bridge [28] [30], H-bridge [31] [32], or clamp-double [33] [34] circuit, as illustrated in Figure 1-4(b)-(d).

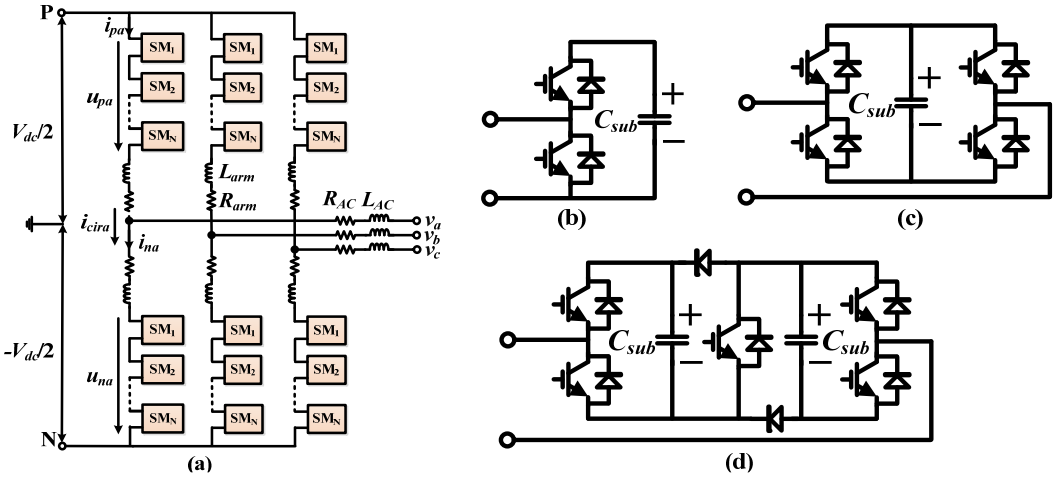
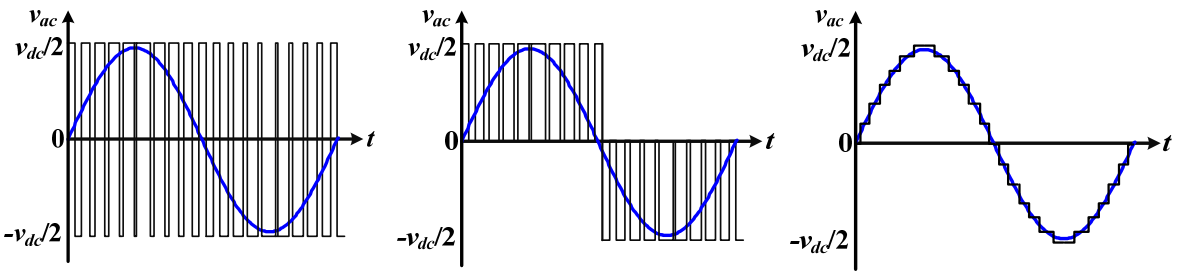


Figure 1-4. (a) Circuit configuration of a MMC with (b) half-bridge cell, (c) full-bridge cell and (d) clamp-double cell.

With N series connected SMs per arm, voltage rating of devices is reduced to V_{dc} / N (V_{dc} is dc side voltage), which eliminates the direct series connection of devices in two and three level converters. In addition, compared to them, MMC also features [35]-[37]:

1) Higher quality output voltage. With higher number of submodules in each arm (N), the output voltage of MMC becomes much more sinusoidal, which leads to smaller ac filters, lower cost and compact converter footprint, as illustrated in Figure 1-5.

2) Lower switching frequency and higher efficiency. The series connection of N SMs per arm can achieve an equivalent switching frequency of Nf_c (f_c represents carrier frequency of each device) in output voltage. Consequently, each device can operate with a fairly low switching frequency, which greatly reduces the switching losses and improves its efficiency to around 99%.



(a) (b) (c)

Figure 1-5. Output ac voltage of a (a) two-level converter, (b) three-level converter, and (c) MMC.

3) Lower high frequency noise due to reduced *dv/dt* and *di/dt*.

4) Modular design and inherent redundancy. The modular design of MMC contributes to lower cost, shorter manufacturing as well as maintenance period, and high extensibility for larger voltage and power applications. Furthermore, the system becomes more reliable since failed SMs can be easily replaced by redundant ones.

The large number of submodules, however, creates several issues. First, to meet the requirement for capacitor voltage ripple, C_{sub} / N should be constant, which makes the power stage dimensioning quite difficult, especially for MMC with numerous submodules per arm. In addition, each submodule requires a gate drive, protection, capacitor voltage monitoring and associated communication resources, which greatly increase the cost of the system. Moreover, the control scheme becomes much more complex than that in a two level converter. Other than the generic upper level control to meet the overall system behavior requirements (VdcQ, PQ, etc.), the capacitor voltage balancing control and circulating current suppression control are indispensable in a MMC for desirable operation performance and lower voltage as well as current stress applied on devices and passive components. Because of the demand for accurate capacitor voltage and arm current detection and/or high speed communication, these control schemes will introduce considerable expense and computing burden to the control unit.

The comparison of site footprint, building area and building volumes for LCC-HVDC (Grita project, 500 MW, 400 kV), two-level VSC-HVDC and half-bridge MMC-HVDC (EWIC project, 500 MW, ±200

kV) is presented in Table 1-1, using the Grita project as the 100% reference [38]. Different from LCC-HVDC, the converter reactors and dc yard equipment in VSC-HVDC are mounted in converter buildings, which provide more convenient maintenance, improved personal safety, lower high frequency emissions and acoustic noise and protection for equipment from adverse weather [5].

Without the requirement for reactive power compensation, the overall site area for 2-level VSC-HVDC is 77% of that for LCC-HVDC, in spite of its higher converter building footprint, height and volume. By adopting MMC, the site area is further reduced to only 58% of the reference value, and lower building height is enabled because of a decreased internal suspension height of converter valves. The overall site area reduction of MMC-HVDC supplies a significant benefit, especially for locations with restricted available area and/or high land price.

Table 1-1. Comparison of site areas among LCC, two-level VSC and MMC based HVDC systems [38].

	Site footprint	Site area (%)	Max. building height (%)	Converter building footprint	Converter building area (%)	Converter building volume (%)
LCC-HVDC (reference)	225 m × 120 m	27000 m^2 (100 %)	20 m (100 %)	35 m × 20 m	700 m^2 (100 %)	14000 m^2 (100 %)
Two-level VSC	180 m × 115 m	20700 m^2 (77 %)	24 m (120 %)	38 m × 35 m	1330 m^2 (190 %)	25000 m^2 (179 %)
MMC-HVDC	165 m × 95 m	15675 m^2 (58 %)	15 m (75 %)	70 m × 45 m	2730 m^2 (390 %)	29500 m^2 (211 %)

The HVDC system can also be categorized according to its operating configurations, and the most common ones are illustrated in Figure 1-6 [5]. In general, the bipolar configurations in Figure 1-6(d) and (e) have higher redundancy compared to the monopolar ones in Figure 1-6(a), (b) and (c) since 50% of the total capacity can be maintained if pole to ground fault occurs in dc side. On the other hand, involving more components, the bipolar configurations have higher cost and larger site footprint compared to monopole ones with the same rating.

With symmetrical monopole, the transformer will not be exposed to dc stress, and no dc ground current exists. But it requires two fully insulated dc conductors. In contrast, the metallic return dc conductor in Figure 1-6(b) does not require full insulation, and can be easily expanded to a bipolar system. Its ac transformer, however, has to withstand dc stresses. By eliminating the metallic return dc conductor, the cost and losses can be reduced in an asymmetrical monopole system with ground return, but it introduces dc ground current and requires associated permissions. Besides, its asymmetrical configuration also adds a dc bias on the ac transformer, making the design difficult.

As a series connection of two asymmetrical monopolar systems, the bipolar system with either metallic neutral or ground electrodes requires a transformer with dc stress withstand capability. Compared to the metallic neutral, the ground return reduces cost but requires permission for temporary dc ground current and environmental effects caused by electrodes. The multi-terminal HVDC (MTDC) systems can be constructed based on all the monopole and bipole configurations. Figure 1-6(f) gives an example of a three-terminal MTDC with symmetrical monopole and parallel connection.

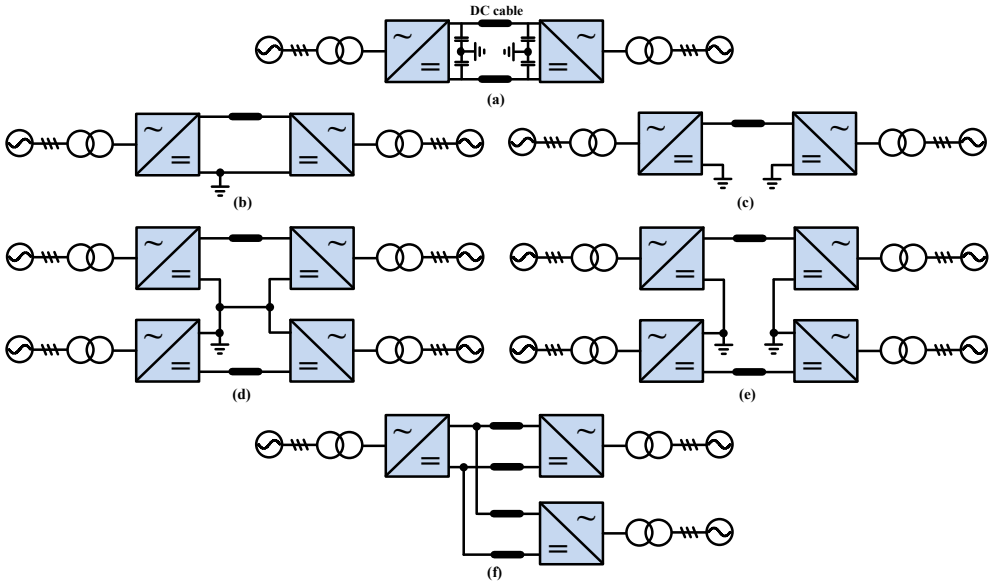


Figure 1-6. Operating configuration of HVDC system (a) symmetrical monopole, (b) asymmetrical monopole with metallic return, (c) asymmetrical monopole with ground return, (d) bipole with metallic neutral, (e) bipole with ground electrodes, (f) multi-terminal.

Since the first MMC based HVDC project ("Trans Bay Cable" project) has been successfully carried out by Siemens in 2010, MMC is considered to be the most promising topology for HVDC transmission systems, and has already been commercialized in many projects as "HVDC plus" by Siemens, "HVDC light" by ABB, and "HVDC MaxSine" by Alstom, which is also shown in Table 1-2. According to [39], the MI cable can be used in both LCC- and VSC- HVDC system, while XLPE cable is only applicable to the latter one because of its unchanged dc voltage polarity during power flow reversal.

Over the past decade, HVDC technology has been greatly developed to transfer energy generated by wind turbines, especially from offshore wind farms where high wind energy and large space are available. In order to increase transmission capacity and facilitate power trading between different countries, several distributed offshore wind farms can be connected to multiple onshore grids, forming a multi-terminal HVDC (MTDC) system.

Table 1-2. Selected VSC-HVDC projects.

Scheme	Commissioning year	Location	Power Transmitted	Direct voltage, kV	Topology	Vendor
Eagle Pass	2000	USA	36 MW/ ±36 MVar	±15.9	Three level VSC(NPC)	ABB
Tjaereborg	2000	Denmark	7.2 MW / -3/+4 MVar	±9	Two level VSC	ABB
Cross Sound Cable	2002	USA	330 MW/ ±150 MVar	±150	Three level VSC (NPC)	ABB
Murraylink	2002	USA	220 MW / +140 / -150 MVar	±150	Three level VSC (NPC)	ABB
Troll A 1&2	2005	Norway	2 × 44 MW / +24/-20 MVar	±60	Two level VSC	ABB
Estlink	2006	Estonia	350 MW / ±125 MVar	±150	Two level VSC	ABB
Caprivi Link Interconnector	2010	Namibia	300 MW / ± 200 MVar	350	Two level VSC	ABB
INELFE	2010	France – Spain	2 × 1000 MW	± 320	VSC-MMC	Siemens

Table 1-2. Selected VSC-HVDC projects. Continued.

Scheme	Commissioning year	Location	Power Transmitted	Direct voltage, kV	Topology	Vendor
Trans Bay Cable	2010	USA	400 MW	± 200	VSC-MMC	Siemens
Nanhui	2010	China	18 MW / ±8.7 MVar	±30	VSC-MMC	State Grid Corporation of China
Valhall	2011	Norway	78 MW	150	Two level VSC	ABB
BorWin1	2012	Germany	400 MW / ±150 MVar	±150	Two level VSC	ABB
HelWin 1	2013	Germany	576 MW	± 250	VSC-MMC	Siemens
BorWin2	2013	Germany	800 MW	± 300	VSC-MMC	Siemens
DolWin1	2014	Germany	800 MW / ± 260 MVar	±320	CTL	ABB
Mackinac	2014	USA	200 MW / ±100 MVar	±71	CTL	ABB
SylWin 1	2014	Germany	864 MW	± 320	VSC-MMC	Siemens
Tres Amigas Superstation	2014	USA	750 MW	±326	VSC-MMC (Full bridge)	Alstom
DolWin2	2015	Germany	900 MW / -300/+380 MVar	±320	CTL	ABB
Troll A 3&4	2015	Norway	2 × 50 MW / ±24 MVar	±60	Two level VSC	ABB
HelWin 2	2015	Germany	690 MW	± 320	VSC-MMC	Siemens
Maritime Link	2017	Canada	2 × 250 MW / ±125 MVar	±200	N/A	ABB
Caithness Moray HVDC Link	2018	UK	Spittal: 800 MW Blackhillock: 1200 MW	±320	N/A	ABB

The most common four topologies of MTDC network are given in Figure 1-7, where blue and black dots represent offshore and onshore converter stations respectively. In the radial topology (Figure 1-7(a)), the converters are connected to their nearby windfarms through only one DC cable, and no interconnection exists among them. Therefore, with only one path for power flow between every two stations, it has the lowest reliability in the four topologies, and a converter station is likely to be lost during a nearby dc side fault.

As shown in Figure 1-7(b), all offshore and onshore converter stations are connected in series in the ring topology, and each converter has two dc cables. It is simple for construction and operation, but has lower reliability compared to the meshed topologies. The reliability of lightly meshed topology in Figure 1-7(c) is slightly increased by connecting the windfarms together, creating multiple paths for wind energy. Additional cables are added in the densely meshed topology (Figure 1-7(d)) and offer the highest reliability and flexibility, but on the expense of long dc cables and high cost. During a dc side pole-to-ground fault, if the faulted dc cable can be isolated necessarily fast, continuous system operation can be achieved and no converter station will be lost [40].

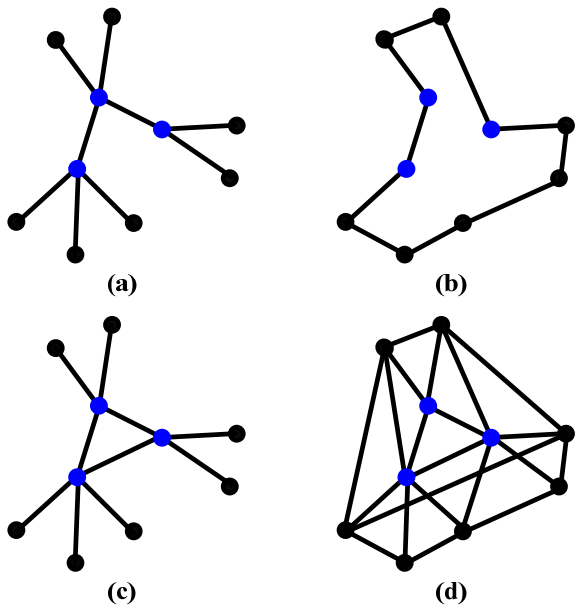


Figure 1-7. Multi-terminal HVDC topologies: (a) radial, (b) ring, (c) lightly meshed, (d) densely meshed.

Compared to point-to-point HVDC (PTP-HVDC) links, the MTDC also have the following merits [41]-[43]:

1. Cost effective. When more than two adjacent ac systems need to be connected, MTDC will supply a more economical option than employing several PTP-HVDC links.

2. Improved reliability. DC side faults in a PTP-HVDC link will lead to serious power transfer failure, and the whole system may need to shut down. For a MTDC network, the faulted cable(s) can be isolated by dc breakers and continuous power transfer is possible through power flow rearrangement.

3. Reduced wind energy curtailment. If windfarms (WFs) are connected to AC grids through PTP-HVDC links, wind curtailment may become necessary to make their power generation match the load profile of the corresponding ac systems. By utilizing MTDC, however, the surplus wind farm energy can be exchanged among different areas, thus mitigating the demand for wind energy curtailment.

4. Low spinning reserve requirement. Connected with multiple WFs, the spinning reserve requirement for ac systems can be reduced.

5. High power exchange and trading flexibility. Energy exchange and trading can be realized in multiple WFs and onshore grids, which help to decrease the electric price.

Table 1-3 gives the existing MTDC projects that have been commissioned [44]. The first two started from point to point links and then extended to multi-terminal schemes using LCC. The last two were built more recently, and adopted half-bridge MMC as their converters. They all employed parallel connection, and Zhoushan project, particularly, will have a meshed MTDC configuration in the future.

For better understanding and to supply guidelines for industrial applications, abundant research efforts have been done in this field. Ref. [45] [46] provide small signal models of MTDC for stability evaluation and controller design. Operation performance with master-slave [47], dc voltage margin [48], and droop control [49] are studied under different scenarios. Based on the Jacobian matrix, a generic power flow analysis is presented in [50] for power flow calculation with various nonlinear voltage droops. As a main issue of MTDC systems, DC fault related research, including fault performance [51], detection [52], protection [53] [54], and post-fault system restoration [55], have been studied in detail. Scaled-down

MTDC prototypes are built in [56] [57], where several typical scenarios, e.g., power reference change, disconnection and reconnection of offshore converters and/or onshore converter stations, have been tested. Based on the MTDC system, a pan European supergrid is proposed in [58] and [59] as a continent-world solution to transfer renewable energy from remote resource locations to load centers. The overall system reliability, efficiency and economics can be improved by pooling the resources of all participating parties (countries, utilities, etc.). The potential issues caused by large-scale renewable energy fluctuation can be greatly reduced or even eliminated with wide-area coordination.

Table 1-3. Selected MTDC projects.

Project	Commissioning year	Location	Terminal numbers	Power Transmitted	DC voltage (kV)	topology
Italy–Corsica–Sardinia (SACOI)	Phase I: 1967 Phase II: 1988	Phase I: Italy and Sardinia Phase II: Corsica	3	Dalmazio: 300 MW Codrongianos: 300 MW Lucciana: 50 MW	200 kV	LCC
Hydro-Quebec-New England	Phase I: 1986 Phase II: 1992	Canada	5	Radisson: 2250 MW Nicolet: 2138 MW Des Cantons: 690 MW Comerford: 690 MW Sandy pond:1800 MW	450 kV	LCC
Nan'ao	2013	China	3	JN: 100 MW QA: 50 MW SC: 200 MW	± 160 kV	Half-bridge MMC
Zhoushan	2014	China	5	ZhouShan: 400 MW Daishan: 300 MW Qushan: 100 MW Yangshan: 100 MW Sijiao: 100 MW	± 200 kV	Half-bridge MMC

According to [60], electric power systems, especially those with overhead lines, are vulnerable to ac faults because of lightning ionizing air, wires blowing together in the wind, animals or plants contacting with the electrical wires, pollution or salt spray on the insulators, etc. However, approximately 80% - 95%

of all system faults are temporary, which last from several cycles to a few seconds at most. Moreover, among the ac faults, single-line-to-ground (SLG) faults are the most common type (65% - 70%) [61].

In many distribution systems, even a temporary SLG fault will trip all three phases. Under certain operating conditions, it will result in the loss of synchronism [62]. Figure 1-8(a) shows that after three-pole-tripping (TPT), power flow on the faulted line drops to zero [63]. Since the accelerating area A1 becomes larger than the decelerating area A2, the power system loses synchronism after three-pole reclosing. In contrast, if single-pole-switching (SPS), which is a combination of single-pole tripping (SPT) and single-pole reclosing (SPR), is adopted, only the faulted phase will open, and the transferred power is given by the curve labeled SPO in Figure 1-8(b). Therefore, the decelerating area A2 is able to match the accelerating area A1, and system will remain stable.

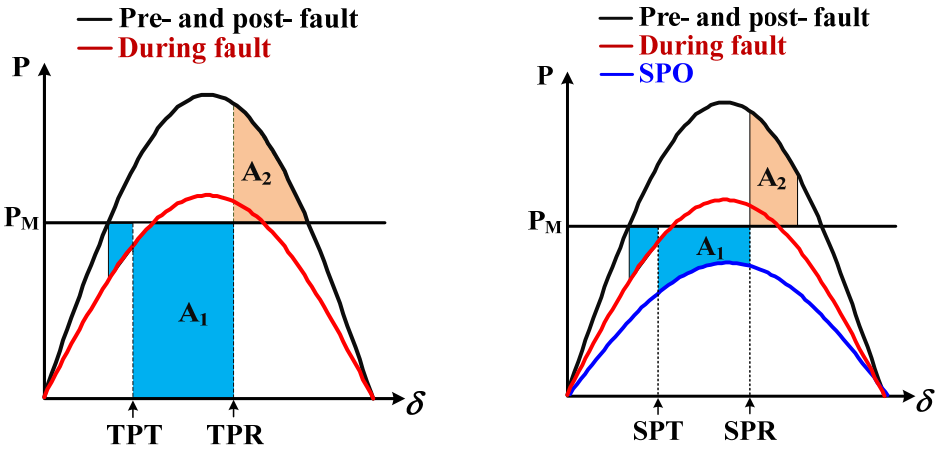


Figure 1-8. System angle stability analysis with (a) TPT and (b) SPS in [63].

SPS also helps power system to maintain voltage stability [64]. As an example, assume in the pre-fault condition, 2000 A current flows through each phase of two parallel lines, and line reactance per phase is 100 Ω. So in this case, the reactive power losses are $6 \bullet 2000^2 \bullet 100 = 2400$ MVARs for two lines. If SLG fault occurs and TPT is used, as illustrated in Figure 1-9, current of 4000 A will flow through each phase

of the remaining line. The reactive power consumption increases to $3 \bullet 4000^2 \bullet 100 = 4800$ MVARs, two times of that in normal condition. If SPS is adopted, however, each remaining phase will flow 2400 A current, and the reactive power consumption becomes 2880 MVARs, only 20 % increase if compared to that in the pre-fault condition.

Consequently, to enhance power system stability and reliability, SPS is preferred in power systems by only tripping the faulted phase when SLG faults occur. This operation condition, however, will create unbalanced phase current in the ac side, double line frequency voltage ripple in the dc side, and potential dc over-voltage or under-voltage. If no corresponding mitigation schemes are applied, control performance and power quality will have a significant degradation.

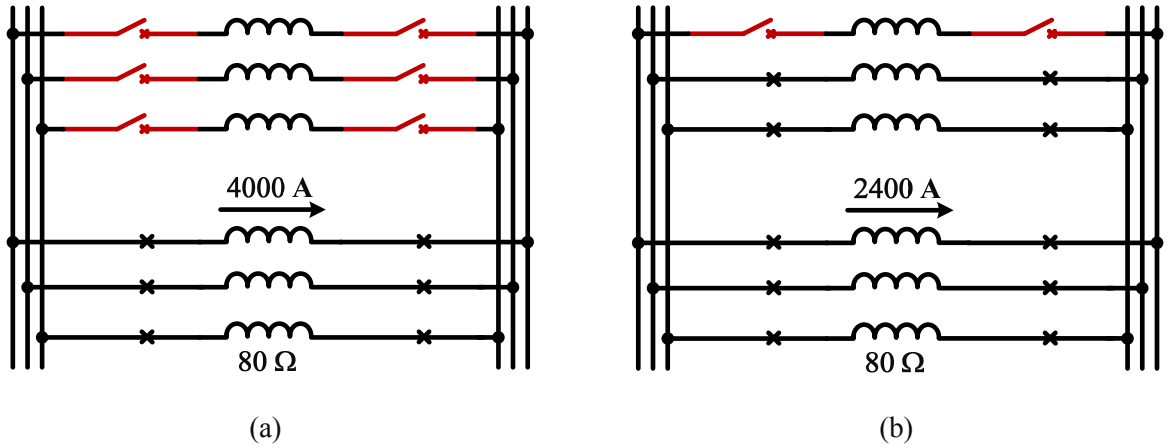


Figure 1-9. System voltage stability analysis with (a) three phase tripping and (b) single pole switching.

To address these issues, both passive and active schemes can be employed. By increasing ac inductance and dc capacitance, the unbalanced current and dc voltage ripple can be mitigated, but at the expense of bulky size and high cost. On the other hand, active approaches, e.g., negative and zero sequence current control, active power ripple suppression control, etc., supply an economic and effective option.

Nevertheless, the unique structure of MMC makes its fault characteristics and control schemes different from other topologies [65] [66], such as circulating current, submodule capacitor voltage ripples, etc. Moreover, the distributed SM capacitors in MMC supply more control freedom but also challenges. To

take full advantage of the MMC and extend its application in HVDC transmission systems, this dissertation will focus on the modelling, analysis and control of point to point MMC-HVDC system under SLG fault conditions. Moreover, to achieve the control targets in MTDC network during SLG fault, an additional dc voltage regulation scheme will also be investigated for coordination of each terminal.

1.2 Research Objectives and Approaches

The objective of this research is to achieve continuous active power transfer and acceptable dc overvoltage for point to point and MTDC systems; balanced ac phase current (< 2 % I_{rated}); minimized circulating current (< 2 % I_{rated}); minimized dc voltage ripple (< 2 % V_{rated}); and an autonomous restoration scheme with passive terminal(s) for MMC based HVDC if the system had to shut down because of a SLG fault.

According to the motivation discussed in section 1.2, the research approaches are listed as follows.

(1) To determine the control objectives, explicit analytical expressions for steady-state current and voltage quantities are derived in a MMC under unbalanced conditions. With the steady-state model, the impact of negative sequence current control on second order current and voltage ripple is investigated. Furthermore, in order to predict the zero sequence circulating current in a point to point HVDC system, the equivalent dc impedance of a MMC inverter is derived with/without the circulating current control.

(2) To achieve desired fault tolerant capability, a quasi-PR control is designed to suppress the second order dc voltage ripple during the SLG fault without additional hardware costs. This controller, together with negative and/or zero sequence current control, enables the HVDC system to achieve low dc voltage ripple as well as balanced AC line currents at both converter stations on each end of the HVDC line. To verify the effectiveness of the designed controllers, system performance with three possible SLG fault conditions has been investigated and compared in detail (specifically, SLG fault occurs in the (1) primary side, (2) secondary side of Y/Δ transformer, and (3) transformerless applications). Finally, the technical feasibility of single pole switching (SPS) is evaluated to maintain the system operation with acceptable performance degradation during a SLG fault.

(3) The small signal model of capacitor voltage and circulating current loops during startup are first derived according to the unique capacitor charging loops and operation conditions, and then the detailed controller design considerations are presented based on the derived model. Furthermore, the limiting factor of the dynamic response of the averaging capacitor voltage control is identified. It is shown that the resonance between arm inductance and SM capacitors will constrain the overall bandwidth of capacitor voltage charging loop, leading to an unsatisfactory dynamic response. To address this issue, a capacitor voltage feedforward control is proposed in this dissertation, which can operate together with the averaging control to achieve fast dynamic response without compromising system stability margin and implementation complexity.

(4) A cascaded droop control scheme is implemented in a four-terminal HVDC system with ring topology. Relying on only local information, no communication requirement is imposed, and autonomous wind energy adjustment can be achieved during contingency events. In addition, operation of this system with different dc voltage control strategies, available capacity of the healthy onshore converter, dq axis current priority, and droop control parameters are analyzed and compared during SLG fault in either onshore converter station. In order to limit dc voltage rise within an acceptable range, power flow calculation is derived using Gauss-Seidel method to provide guidance for droop control design.

1.3 Dissertation Organization

This research report is organized as follows:

Chapter 2 gives a detailed literature review on the key enabling technologies to develop an effective ac fault tolerant control scheme in both point-to-point and multi-terminal HVDC systems. Based on the literature review, the associated challenges in each focused area are pointed out and addressed.

Chapter 3 gives the steady state analysis of MMC-HVDC under SLG fault to understand the fault characteristics and corresponding control objects. The equivalent circuit of 2nd order components is derived, and experimental results are presented and compared with the calculated values.

Chapter 4 presents the design and testing results of the integrated control scheme under three possible SLG fault conditions. This control scheme is capable of eliminating negative and zero sequence phase current, suppressing all circulating current components, and mitigating dc voltage ripple.

Chapter 5 reveals the necessity of additional capacitor charging control for MMC inverter, and focuses on its modelling and active startup control scheme design. The detailed design considerations and testing results will be presented.

Chapter 6 introduces a cascaded droop control scheme for multi-terminal HVDC system to achieve autonomous wind power adjustment during onshore converter side ac faults. The control performance will be evaluated under different operation conditions and droop control design will be discussed as well.

Chapter 7 summarizes this dissertation and proposes future work that may be undertaken in this area.

2 Literature Review

According to the operation mechanism of SPS, the typical single-pole-open time (system operates with only two healthy phases, leaving the faulted phase open circuit) is around 0.5 s [67] [68]. If a temporary SLG fault occurs (≤ 0.5 s) and SPS is installed, it is still possible for the continuous operation of dc grids. Under this condition, steady state modelling and/or power flow analysis is required to predict its fault performance. Based on the steady state model, an effective control scheme can be designed to mitigate the undesirable harmonics and ripple. In addition, distributed dc voltage regulation is needed to realize coordinative active power adjustment among terminals. Otherwise, the system may not be able to withstand large dc voltage variation and have to shut down. Due to the distributed SM capacitors, the startup process of MMC becomes more complicated than that of other topologies. Therefore, for MMC based HVDC, including point-to-point and multi-terminal configurations, an effective startup scheme is necessary for fast system restoration after fault clearing.

Aiming at obtaining desired performance under SLG faults, this dissertation presents the development of fault tolerant control schemes using the following techniques: (1) for point to point MMC-HVDC, deriving the steady state modelling with unbalanced ac voltages; (2) predicting the circulating current, capacitor voltage ripples, dc voltage ripple and output phase voltage, etc., based on the model, and (3) designing corresponding control schemes to mitigate the unwanted voltage and/or current components. For the studied four-terminal HVDC system, the following work was done: (1) proposing a cascaded droop control strategy without communication requirement; (2) deriving the corresponding power flow distribution; and (3) analyzing the impact of fault location, current priority, and droop control parameters on system fault characteristic .

This section will first review the state-of-the-art research activities in the above mentioned areas. The issues and unsolved problems of previous research efforts are examined, and then the challenges of this research are addressed.

2.1 Steady State Modelling of MMC under SLG Fault Condition

The steady-state and dynamic analysis of MMC under normal operation has been thoroughly discussed in the existing literature, using large signal and/or small signal models [69]-[71]. Based on these models, system parameters, such as arm inductance and submodule (SM) capacitance can be designed [72] [73]. Moreover, the operation principle and design considerations of circulating current suppression as well as capacitor voltage balancing control schemes can be further understood [74]-[76].

Under unbalanced conditions, most of previous research efforts focused on proving the existence of zero sequence double line frequency active power, which will flow into the dc side and cause dc voltage ripple and/or dc current ripple. Ref [77] [78] gives the analytical relationship among instantaneous active/reactive power and fundamental frequency positive- and negative- sequence current in ac terminals, as given in (3 - 1). According to this relationship, the current references for active power ripple elimination can be calculated [79]. The relationship, however, does not consider the 2nd order components in circulating current and capacitor voltages, which cannot be present the inner characteristics of MMC, e.g., circulating current, capacitor voltage and arm output voltage, etc. As an improvement, instantaneous active power in each phase unit is derived in [80] as (3 - 2), where negative sequence circulating current is considered. But under SLG fault, positive and zero sequence components will also exist in circulating current, making the derivation inaccurate. Additionally, the magnitude variation trend of circulating current, capacitor voltage and active power ripple with different degrees of unbalance and control schemes are not explicitly given.

$$P = P_1 + P_{s2}\sin(2\omega t) + P_{c2}\cos(2\omega t) + 3u_0 i_0 \quad (3 - 1)$$

$$Q = Q_1 + Q_{s2}\sin(2\omega t) + Q_{c2}\cos(2\omega t)$$

where $u_d^+, u_q^+, u_d^-, u_q^-$ are positive and negative sequence dq axis voltage; $i_d^+, i_q^+, i_d^-, i_q^-$ are positive and negative sequence dq axis current; u_0, i_0 are zero sequence ac voltage and current, respectively; ω is the fundamental angular frequency and $\omega = 2\pi f$; P_1 and Q_1 represent the dc components in active and reactive power, while $P_{s2}, P_{c2}, Q_{s2}, Q_{c2}$ are the double line frequency ripples, and

$$\begin{bmatrix} P_1 \\ Q_1 \\ P_{s2} \\ P_{c2} \\ Q_{s2} \\ Q_{c2} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} u_d^+ & u_q^+ & u_d^- & u_q^- \\ u_q^+ & -u_d^+ & u_q^- & -u_d^- \\ u_q^- & -u_d^- & -u_q^+ & u_d^+ \\ u_d^- & u_q^- & u_d^+ & u_q^+ \\ -u_d^- & -u_q^- & u_d^+ & u_q^+ \\ u_q^- & -u_d^- & u_q^+ & -u_d^+ \end{bmatrix} \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix}.$$

$$p_{PUa} = \frac{1}{6} V_{dc} I_{dc} [k^- m^+ \cos(2\omega t + \alpha_- + \gamma_+) + k^+ m^+ \cos(2\omega t + \alpha_+ + \gamma_+) - 2l^- \sin(2\omega t + \beta_-) - k^- m^+ \cos(\alpha_- - \gamma_+)]$$

$$p_{PUb} = \frac{1}{6} V_{dc} I_{dc} [k^- m^+ \cos(2\omega t + \alpha_- + \gamma_+) + k^+ m^+ \cos\left(2\omega t + \alpha_+ + \gamma_+ + 120^\circ\right) - 2l^- \sin\left(2\omega t + \beta_- + 120^\circ\right) - k^- m^+ \cos\left(\alpha_- - \gamma_+ - 120^\circ\right)]$$

$$p_{PUc} = \frac{1}{6} V_{dc} I_{dc} [k^- m^+ \cos(2\omega t + \alpha_- + \gamma_+) + k^+ m^+ \cos\left(2\omega t + \alpha_+ + \gamma_+ - 120^\circ\right) - 2l^- \sin\left(2\omega t + \beta_- - 120^\circ\right) - k^- m^+ \cos\left(\alpha_- - \gamma_+ + 120^\circ\right) \quad (3\text{ - }1)$$

where V_{dc} and I_{dc} are dc side voltage and current; m^+ is the positive sequence modulation index; E^+ and $\alpha_+$are magnitude and initial phase angle of positive sequence grid voltage; E^- and α_- are magnitude and initial phase angle of negative sequence grid voltage; U_{diff}^- and β_- are the magnitude and initial phase angle of circulating current compensation voltage, and

$k^\pm = \frac{E^\pm}{nV_{dc}}$; $l^- = \frac{U_{diff}^-}{nV_{dc}}$ $\left(n = \frac{1}{2} for\ SPWM, \frac{1}{\sqrt{3}}\ for\ SVM\right)$.

Based on the literature survey, an analytical description of a MMC under unbalanced conditions, including steady-state voltage, current quantities and their interaction, has not yet been done.

2.2 Control Schemes of Point to Point MMC-HVDC under AC Unbalanced Conditions

Thanks to the distributed location of dc capacitors, the MMC has more degrees of freedom than two level converters, which enables flexible control and uninterruptable performance with unbalanced input voltages [81] [82]. As illustrated in Figure 2-1 Proportional-Integral-Resonant (PIR) based controllers are

proposed in [77] to mitigate the double line frequency circulating current and dc line current ripple under unbalanced conditions.

Similarly, a non-ideal Proportional-Resonant (PIR) control is employed in [83] for circulating current suppression, as shown in Figure 2-2. Considering the impact of asymmetrical arm resistances, [78] presents PR based controllers for zero sequence circulating current suppression. However, AC active power ripple instead of unbalanced AC side current is regulated for better control performance, which may cause malfunction of the protective devices.

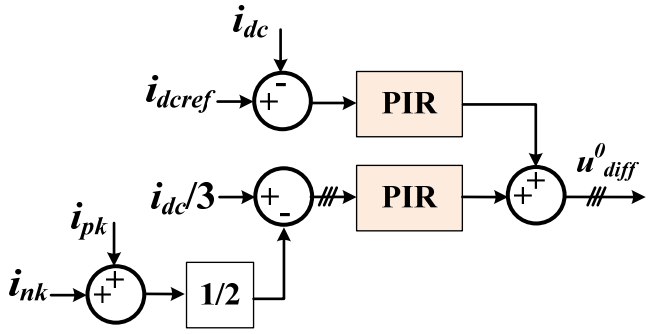


Figure 2-1. Control diagram of dc current ripple elimination in [77].

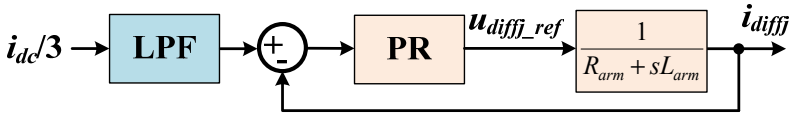


Figure 2-2. Diagram of the circulating current suppressing controller in [83].

The operation of a MMC based HVDC (MMC-HVDC) with converter side SLG fault and DC line to ground fault is presented in [84]. With non-grounded or large resistance grounded dc buses, no or low zero sequence current is generated, and thus the performance degradation is negligible. Nevertheless, this conclusion no longer applies to a HVDC system with long dc cable and/or solid grounded dc buses.

By adopting the dual current control scheme proposed in [85], a mathematical model for MMC-HVDC system is derived in [79]. Zero sequence current is well suppressed for transformerless HVDC

applications with the designed controllers. However, as described in [79], the double line frequency dc voltage ripple cannot be eliminated by instantaneous active and reactive power ripple control.

To address this problem, a novel dc voltage ripple suppressing control (DCVRSC) is proposed in [80] using arm voltages feed-forward control, as shown in Figure 2-3. Theoretically, the arm voltages can be calculated by switching states and submodule capacitor voltages. In practice, however, the former one may not be available to the main control unit since auxiliary processors, such as FPGAs, are used for PWM generation. Under this condition, additional fast communication equipment will be required for arm voltages calculation, thus introducing unnecessary hardware and cost.

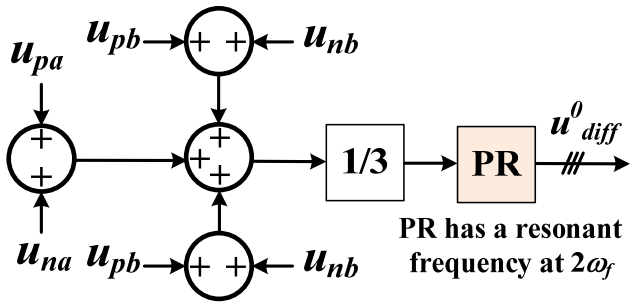


Figure 2-3. Diagram of dc voltage ripple suppressing control (DCVRSC) in [80].

To take full advantage of the MMC, a control scheme to regulate differential currents of the MMC is proposed in [86] based on Lagrange-based optimization in "abc" coordinates. Either constant capacitive energy sum or with constant (pure DC) differential current per phase can be achieved to prevent ac power oscillation from propagating into the DC side during unbalanced conditions. However, this control scheme is quite complex with many average values calculation, and the differential current reference is related to control output variables, such as v_{dc}, v_{diff}, which may lead to degraded steady state as well as dynamic response.

In addition, some related work has been done in two and three level converters. Ref. [87] presents a recovery strategy for VSC-HVDC transmission systems, by which the commonly applied dc chopper can be eliminated and the system resiliency can be improved during ac faults. A control scheme is proposed in

[88]-[90] to suppress the possible dc-link voltage fluctuations under unbalanced conditions, while [91] decomposes the current vectors and controls them separately in terms of positive and negative sequence components to deal with unbalanced conditions in voltage source converters (VSCs).

For accurate decoupling between the positive and negative sequence controllers, a new control strategy for a VSC transmission system is presented in [92] under unbalanced network conditions. Moreover, in order to achieve smooth dc voltage in VSCs under unbalanced operation conditions, multi-frequency Proportional-Resonant (PR) controllers in $\alpha\beta$ frames are adopted in [93], considering both supply voltage and input impedance unbalance. A unified model representing dynamic behavior of the three-level neutral point diode clamped (NPC) VSCs is built in [94], and control strategies are introduced to either balance the AC line currents or to mitigate the double line frequency active and reactive power ripple.

However, fault characteristics and necessary fault isolated operation after the SLG fault occurs have not been investigated yet in the literature. Besides, the existing literature mainly focuses on the controller design when a fault occurs in the primary side of the Y/Δ transformer, i.e., the zero sequence current is completely blocked by the delta connection of the transformer in the converter side, and thus only positive and negative sequence currents need to be regulated, leading to a limited fault-tolerant capability. Therefore, following question needs to be answered: is it possible and how to achieve both balanced current and low dc voltage ripple using a generic control scheme under different SLG fault locations?

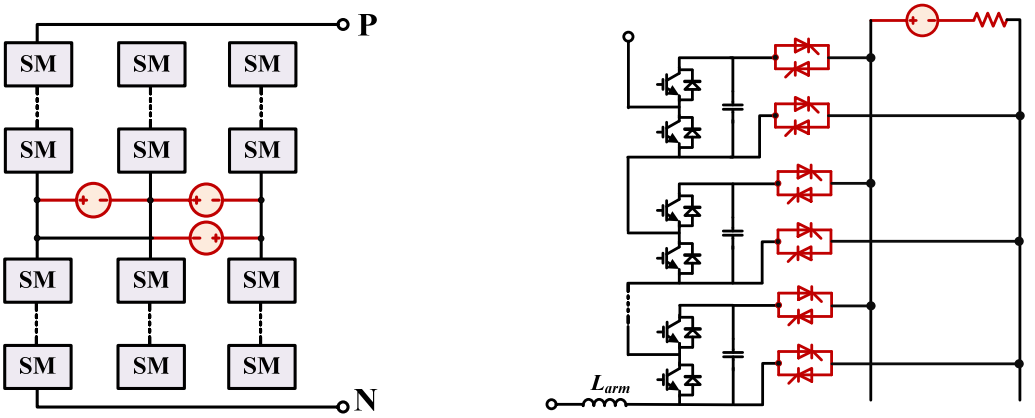
2.3 Startup Scheme

Different from two-level converters, the distributed capacitors induce more complicated startup process and distinct behaviors of MMC under different operation conditions. In order to ensure smooth and fast energization, deliberate startup schemes are crucial in a MMC based HVDC system.

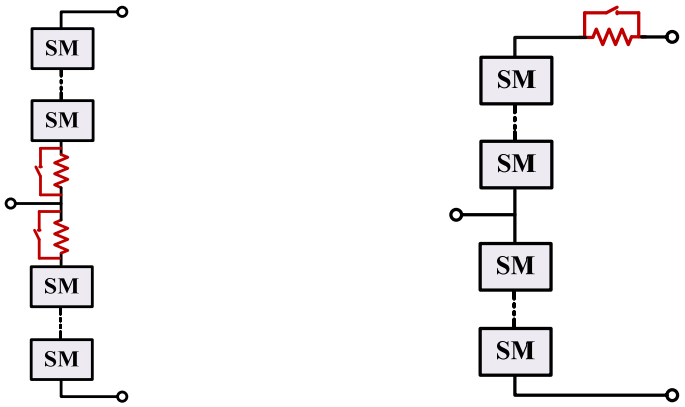
A dc circuit breaker and an external dc source with its voltage equal to the nominal voltage of each submodule's (SM) capacitor are utilized in [95] and [96], as shown in Figure 2-4(a), to avoid large inrush current in a MMC inverter during the pre-charge process. In spite of its easy implementation, this solution leads to additional cost, especially in high power applications. Besides, because of the nonzero voltage

ramp time and impedance of a non-ideal dc voltage source, there are substantive requirements for the charging time and time interval between charging pulses.

To deal with this issue, a charging circuit that consists of an auxiliary dc source and two thyristors for each submodule is proposed in [97] (Figure 2-4(b)). By triggering the thyristors synchronously, all SM capacitors can be charged together, thus accelerating the startup procedure. Nevertheless, it causes high control complexity and still additional cost to the system.



(a) Startup with external dc source in [95] (b) Startup with thyristors and external dc source in [97]



(c) Startup with arm current limiting resistors in [98] (d) Startup with dc current limiting resistors in [99]

Figure 2-4. Startup schemes with auxiliary passive components.

As a more cost-effective way, the main dc voltage is used in [98] to charge the capacitors (Figure 2-4(c)). However, an additional inrush arm current limiting resistor is connected in series with the SMs in

each arm and should be bypassed after the charging process. Similarly, the upper and lower arms of a half bridge MMC are charged separately in [99] by applying a current limiting resistor in the dc side (Figure 2-4(d)). The resistors (either inserted into each arm or into the dc bus), together with bypass switches are bulky and costly. Besides, if redundant SMs are used for higher converter reliability, then these also need to be charged for smooth transitions between their bypass and insertion. This means that the voltage of each SM capacitor cannot be charged to its rated value by this method.

Without any auxiliary passive components, a grouping sequentially controlled charge (GSCC) method is proposed in [100] for a three phase clamp double submodule (CDSM) MMC. Despite its easy implementation, the group number needs to be carefully selected, and deviation among the capacitor voltages due to capacitance tolerance becomes a concern. However, similar to the injected passive resistance, if redundant SMs are involved, the SM capacitors cannot be fully charged.

Reference [101] presents an active capacitor charging scheme for a MMC inverter. After the uncontrolled pre-charge period, this scheme helps to build up the capacitor voltages from Vdc / 2N (Vdc represents the rated dc voltage; N is submodule number per arm) to Vdc / N by gradually decreasing the number of inserted SMs from 2N to N in each phase-leg. Nonetheless, the working state of submodules in this method should be frequently swapped to maintain balanced capacitor voltages, making its implementation quite complicated, especially in three phase systems with a large number of SMs.

Different from the “open-loop” capacitor charging scheme, Ref. [102] proposes a closed loop pre-charge control by regulating a constant charging current during both dc-side and ac-side startup process, as shown in Figure 2-5. SM capacitors can be linearly charged through this method, independent of SM numbers. However, this method requires complex and specially designed capacitor balancing as well as reference generation algorithms, and demands a fast transition between startup and normal operation to avoid capacitors over-charging.

The averaging capacitor voltage control proposed in [103] is utilized in [104] to gradually increase capacitor voltage during startup (self-start) and guarantee an average capacitor voltage of Vdc / N during the normal conditions. Nevertheless, the modelling and design of the averaging capacitor voltage control

are still missing, which may cause system instability during the variation of operation conditions, control parameters, and system parameters. Additionally, the dynamic performance is not evaluated and unable to be predicted without a valid startup model.

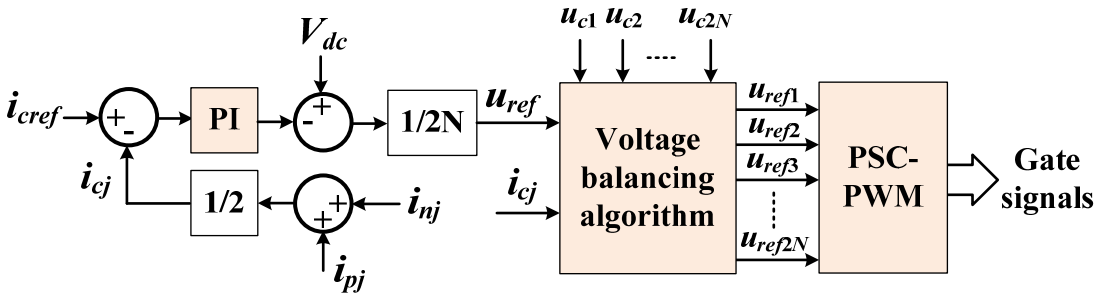


Figure 2-5. Diagram of constant charging current control in [102].

The energy based control is presented in [105] for a desirable startup process of MMC. As a comprehensive control scheme, this control scheme is capable of controlling both the total and differential energy stored in the upper and lower arm capacitors. By properly regulating the arm energies, a gradual and symmetrical capacitor charging is achieved during the startup process. However, consisting of several cascaded control diagrams, its implementation is fairly complicated.

Based on the literature survey, there is no valid model of MMC during startup period, which leaves the steady state and dynamic response evaluation of capacitor voltage charging control difficult.

2.4 Control Strategies of MTDC under SLG Fault Conditions

Operating as conventional power plants, large WFs should withstand low (even zero) voltage for a certain period of time according to the grid code [106] and are not allowed to trip during ac faults. However, the uninterrupted power flow from WFs put forward a huge challenge to the MTDC network for active power balance since the receiving end converters cannot absorb all the power during ac fault conditions. Without proper countermeasures, the surplus active power will charge dc capacitances and the dc voltage increase may destroy HVDC equipment [107].

As solutions, five fault ride through methods are analyzed and compared in [108] for a point-to-point HVDC system with DFIG-based windfarms, including chopper resistors in dc terminal of offshore converter, active power reduction through offshore converter current control, wind turbine power set-point adjustment, offshore ac grid frequency increase and voltage magnitude reduction. Except for the first method, the others all rely on a fast and reliable communication between onshore converter, offshore converter and WFs. Otherwise, the active power reduction will be slowed down by communication delay and induce unacceptable dc overvoltage.

Similarly, in order to limit dc overvoltage during onshore converter side ac fault, three approaches, i.e., power drop of wind turbines, offshore converter frequency increase and dc damping resistor, are presented in [109] for a four-terminal HVDC system. Due to the demands for fast communication and wind turbine capable of power adjustment with fast frequency variation in the first two schemes, however, [109] focuses on the fault tolerant performance with dc damping resistor, as illustrated in Figure 2-6, under different onshore converter power sharing modes.

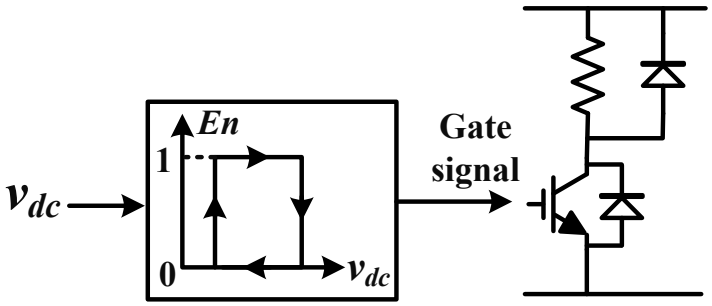
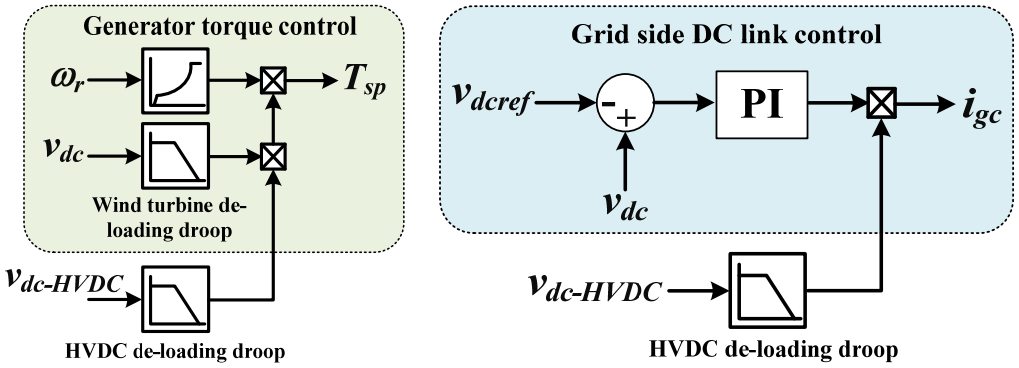


Figure 2-6. Control of damping resistor in [109].

Ref. [110] proposes a de-loading protection scheme for dc voltage rise suppression in a point-to-point HVDC transmission system with full rated converter wind turbines. This scheme reduces the active power of each wind turbine (WT) by decreasing its torque as the WT or HVDC dc link voltage increases, as shown in Figure 2-7. However, in order to enable a rapid response to dc voltage increase, the signals needed for de-loading control should be sent to every WT or offshore converter through fast

communication circuit. The dc grid chopper resistor is also considered in this paper as an effective but costly alternative without communication requirement.

Generally speaking, the installation of dc chopper resistors can decouple the control of wind turbines from that of a HVDC network, and no wind energy variation is required. But it is quite costly and does not fully utilize the capability of converters in wind turbines and HVDC. On the other hand, the fault-tolerant schemes mentioned above all rely on a fast communication since even a short delay time could cause unacceptable dc voltage rise. Nevertheless, it might be difficult to achieve this in real systems, especially in offshore windfarms which are far away from the onshore stations. Consequently, control strategies with only local information are preferred in recent literatures.



(a) Via generator controller (b) Via grid side controller

Figure 2-7. De-loading methods used in [110] for a fully rated converter wind turbine.

Among the communication-free control schemes, the dc voltage margin and droop control are two widely used ones [111] [112]. The v_{dc} - P_{dc} characteristics of each converter in a three-terminal MTDC system with dc voltage margin and droop control are illustrated in Figure 2-8(a) and (b), respectively.

As shown in Figure 2-8(a), under normal condition, VSC1 works as a slack bus and controls dc voltage, while VSC2 and VSC3 regulates the active power. During non-ideal conditions, however, VSC1 may hit its power limit and induce a dc voltage increase. Having lower dc voltage reference in the margin control in this case, VSC2 will first take over the dc voltage control and reduce its active power

generation. Since active power can be successfully balanced by VSC2, VSC3 will stay in the constant active power mode with dc voltage equals to v_{ref_high1}.

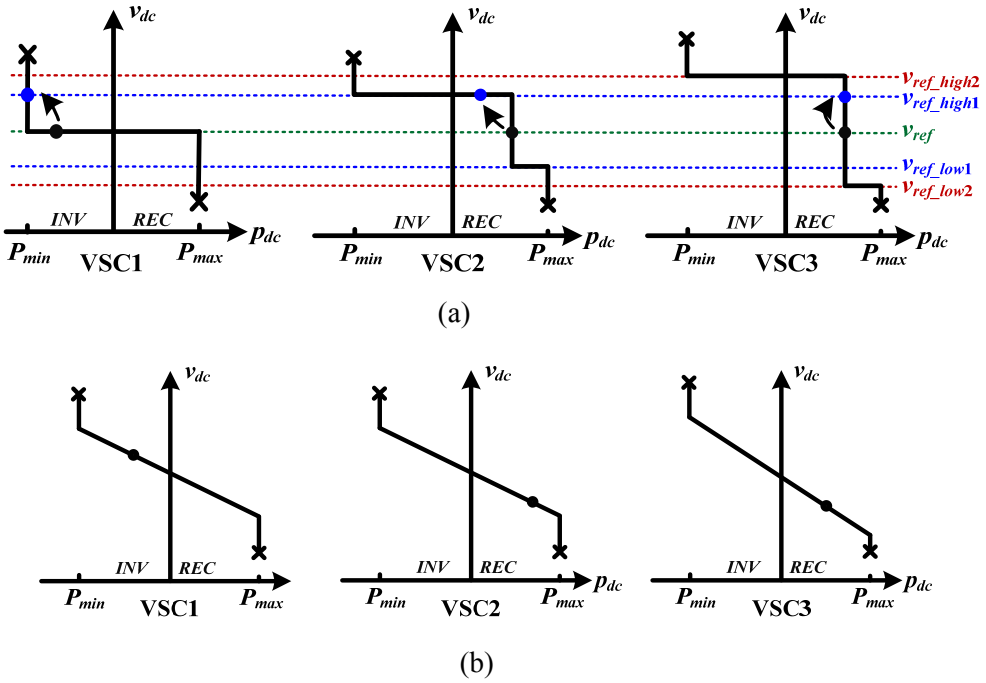


Figure 2-8. DC voltage versus active power characteristics with (a) dc voltage margin control and (b) dc voltage droop control.

By setting different threshold voltage references, e.g., V_{ref_high} and V_{ref_low}, the power injection and dc voltage regulation priority of VSC2 and VSC3 can be easily changed, and more converters can be involved to form an expanded system. The margin control, nevertheless, only activates one converter for dc voltage regulation, which puts a high stress on the voltage controlling bus. In addition, the transition from one dc voltage level to another may occur abruptly due to the saturated PI controller, inducing a considerable overcurrent and/or overvoltage.

Similar as the frequency droop control for electrical generators in an ac system, a natural regulation of dc terminal voltage can be achieved by the droop control in Figure 2-8(b) according to its active power variation. Normally, a steep slope of droop curve represents high control sensitivity. The downsides of the

standard droop control are the varying operating points of dc voltage as well as active power in each station, and potential undesired power sharing among converters due to their dc terminal voltage deviation caused by dc cable resistances.

Ref. [113] discusses and compares operation performances of a parallel four-terminal HVDC system, shown in Figure 2-9, with different dc voltage control schemes, including dc voltage droop with/without dead-band, dc voltage margin control and their combination under severe AC fault conditions. According to the given simulation results, droop control is claimed to have better dynamic performance in dc voltage regulation. This conclusion, however, is based on a single fault scenario, which may become invalid when control parameters, dc voltage margin setting, and fault location change. Similar to the dc voltage margin control in a parallel MTDC system, a voltage dependent current order limiter (VDCOL) control is proposed in [114] to achieve autonomous dc current adjustment during both normal and ac fault conditions in a series four-terminal thyristor based MTDC network (Figure 2-10).

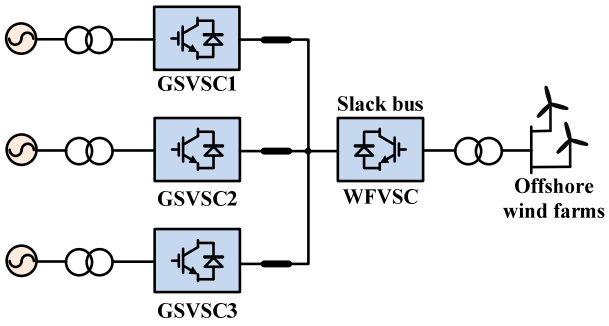


Figure 2-9. Single line diagram of the four-terminal HVDC system in [111].

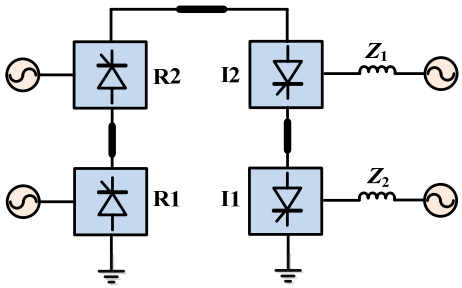


Figure 2-10. Single line diagram of the four-terminal series HVDC system in [114].

In the above two papers, all onshore and offshore converters are assumed to connect to strong ac grids and have full controllability for active and reactive power generation. Therefore, by reducing their power references according to the dc voltage rise, no dc over-voltage will occur during onshore converter side ac faults. However, as analyzed in [108]-[110], the offshore converters always need to build ac voltages for wind turbines in reality, which makes the dc voltage margin and droop control used in [111] and [114] inapplicable [115]. To deal with this issue, a v_{dc} - v_{ac} / f droop is proposed for an offshore converter in [116], which adjusts the ac voltage magnitude or frequency according to its dc terminal voltage variation through a droop curve.

With cooperative control schemes implemented in wind turbines, the wind power generation can automatically drop during onshore converter side ac faults [117]. Nevertheless, the detailed control implementation and design considerations are not presented, and no experimental verification is supplied. Therefore, in order to fully utilize this control concept, the associated power flow calculation, controller design, and droop parameters selection should be investigated in detail.

2.5 Summary

In this chapter, the literature is reviewed for the four specific topics in this dissertation, i.e. the steady state modelling and fault tolerant control schemes of MMC under unbalanced conditions, passive and active startup methods for MMC inverter, and dc overvoltage suppression strategies for multi-terminal HVDC system. The advantages and drawbacks of the state-of-art techniques are discussed, and the challenges of these topics are identified.

3 Steady State Modelling of MMC under SLG Fault Conditions

In this chapter, a steady-state model of MMC under SLG conditions is presented for second order phase voltage ripple prediction, taking the impact of negative sequence current control into account. From the steady-state model, a circular relationship is found among voltage and current quantities, which can be used to evaluate the initial phase angles and magnitudes of different circulating current components. Moreover, in order to calculate the circulating current in a point to point MMC based HVDC system under unbalanced conditions, the derivation of equivalent dc impedance of a MMC is discussed as well. According to the dc impedance model, a MMC inverter can be represented as a series connected R-L-C branch, with its equivalent resistance and capacitance directly related to the circulating current control parameters. Experimental results from a scaled down three-phase MMC system are provided to support the theoretical analysis and derived model.

3.1 System Configuration under SLG Fault Conditions

Figure 3-1 illustrates the single line diagram of a typical point to point MMC-HVDC transmission system, where v_{s1} and v_{s2} represent AC grid voltages; L_s and R_s represent grid impedance; L_{AC} and R_{AC} are AC reactor and its equivalent parasitic resistance. For isolation and voltage conversion, the AC terminal of each MMC is connected to the grid voltage v_{s1} or v_{s2} through a three-phase Y/Δ transformer. The two MMCs are connected through dc cables.

In order to investigate the impact of unbalanced current control on circulating current, the widely used dual current control is adopted, with its control diagram illustrated in Figure 3-2 [85] [88]. For accurate synchronization with the grid voltage, the positive sequence voltage is extracted with methods proposed in [118] and used as the input of a phase locked loop (PLL). Through park transformation and the angle locked by PLL, the converter-side phase current can be decomposed into positive and negative sequence components and regulated separately in *dq* coordinates. With accurate extraction of positive, negative and zero sequence voltage and current, as well as properly designed PI controllers, the negative sequence phase current can be eliminated under unbalanced conditions.

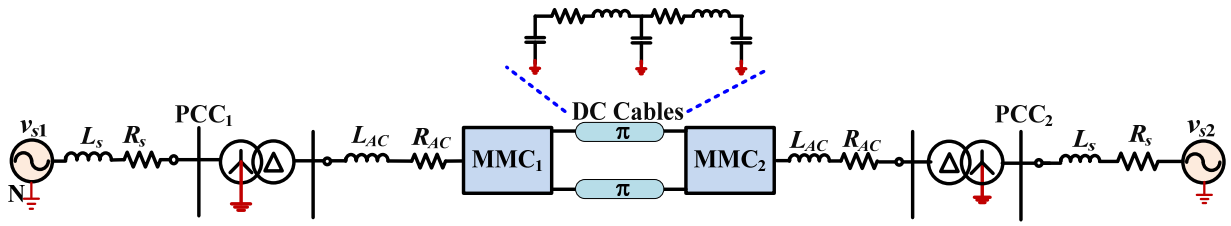
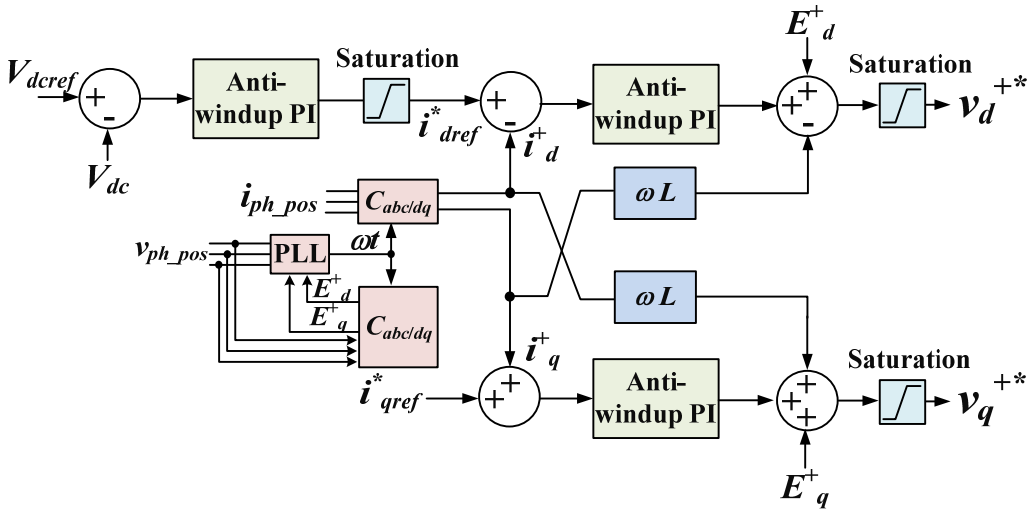
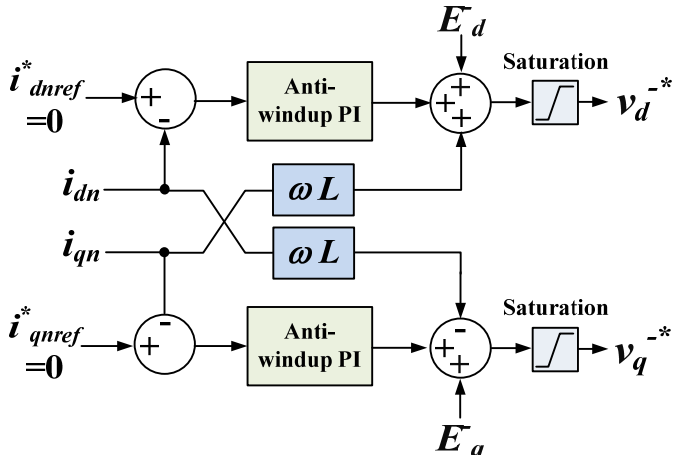


Figure 3-1. Single line diagram of a MMC-HVDC transmission system.



(a) Positive sequence current control



(b) Negative sequence current suppression

Figure 3-2. Diagram of dual current control.

During a single-line-to-ground (SLG) fault, if ground loops exist in the converter side, additional PR control could be adopted to suppress the zero sequence current [119].

3.2 Steady-state Model for Second Order Phase Voltage Ripple Prediction

Figure 3-3 illustrates the single phase equivalent circuit of a MMC [71], where v_{du} and v_{dl} are the positive (upper) and negative (lower) dc bus to ground voltage; i_d is the dc current; v_g^k and i_s^k represent the phase voltage and line current of phase k; v_{cu}^k and v_{cl}^k are the voltages produced by the SMs in the upper and lower arm, respectively; i_u^k and i_l^k denote the corresponding arm currents; and i_c^k is circulating current in phase k. The subscript "u" and "l" represent the upper and lower arm, respectively.

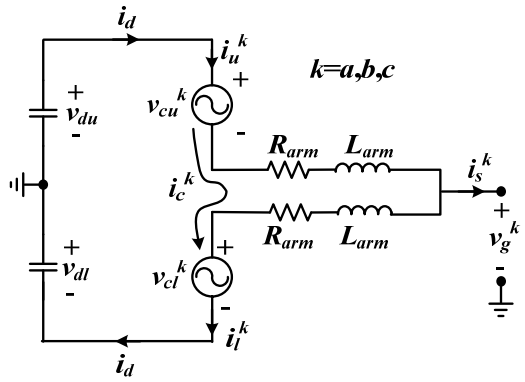


Figure 3-3. Single phase equivalent circuit of the MMC.

A. Without Negative Sequence Current Control

Assume a SLG fault occurs in the primary side of the Y/Δ transformer in MMC_1 station, which will create an unbalanced voltage in PCC_1 [120]-[122]. Because of this transformer, no zero sequence phase current will be observed in the converter side. According to Figure 3-3, the upper and lower arm current can be expressed as (3 - 1).

$$i_{au}(t) = \frac{\sqrt{2}}{2} I^+ \sin(\omega_1 t + \varphi_+) + \frac{\sqrt{2}}{2} I^- \sin(\omega_1 t + \varphi_-) + I_{cda} + I_c^+ \sin(2\omega_1 t + \theta_+) + I_c^- \sin(2\omega_1 t + \theta_-) + I_c^0 \sin(2\omega_1 t + \theta_0)$$

$$i_{al}(t) = -\frac{\sqrt{2}}{2} I^{+} \sin(\omega_1 t + \varphi_{+}) - \frac{\sqrt{2}}{2} I^{-} \sin(\omega_1 t + \varphi_{-}) + I_{cda} + I_c^{+} \sin(2\omega_1 t + \theta_{+}) + I_c^{-} \sin(2\omega_1 t + \theta_{-}) + I_c^{0} \sin(2\omega_1 t + \theta_0) \quad (3 - 1)$$

where I^{+}, I^{-} are the amplitudes of the positive and negative sequence phase current, respectively; φ_{+}, φ_{-} are the corresponding initial phase angles; I_{cda} represents the dc component in arm currents of phase A; ω_1 represents the fundamental frequency angular frequency; I_c^{+}, I_c^{-} and I_c^{0} denote the positive, negative and zero sequence circulating current, respectively, and θ_{+}, θ_{-}, and θ_0 are the corresponding initial phase angles. For simplicity, only the dominant second order harmonics are considered in this paper. Under certain operation conditions, I^{+}, I^{-}, φ_{+}, φ_{-} in (3 - 1) can be regarded as known parameters based on power system fault calculation [123]-[125], while I_c^{+}, I_c^{-}, I_c^{0}, θ_{+}, θ_{-}, and θ_0 are unknown variables and will be calculated in the following derivation.

In practice, the equivalent switching frequency of a MMC (Nf_c, f_c is the carrier frequency) is high enough to acquire negligible high-frequency components in the switching functions. Therefore, an average switching function shown in (3 - 2) can be adopted in this analysis

$$S_{au_av}(t) = \frac{1}{2}[1 - M\sin(\omega_1 t)] \qquad S_{al_av}(t) = \frac{1}{2}[1 + M\sin(\omega_1 t)] \quad (3 - 2)$$

where M represents positive sequence modulation index; $S_{au_av}(t)$ and $S_{al_av}(t)$ are average switching functions of the SMs in the upper and lower arms, respectively.

Based on (3 - 1) and (3 - 2), the associated current and voltage quantities can be expressed as follows:

1) Capacitor Charging Current: according to [126], the average capacitor charging current in the upper (i_{c_u}) and lower arm (i_{c_l}) can be expressed as

$$i_{c_u}(t) = S_{au_av}(t) \cdot i_{au}(t) = \frac{1}{2} I_{cda} - \frac{\sqrt{2}}{8} M I^{+} \cos\varphi_{+} - \frac{\sqrt{2}}{8} M I^{-} \cos\varphi_{-} - \frac{1}{2} M I_{cda} \sin(\omega_1 t) + \frac{\sqrt{2}}{4} I^{+} \sin(\omega_1 t + \varphi_{+}) + \frac{\sqrt{2}}{4} I^{-} \sin(\omega_1 t + \varphi_{-}) - \frac{1}{4} M I_C^{+} \cos(\omega_1 t + \theta_{+}) - \frac{1}{4} M I_C^{-} \cos(\omega_1 t + \theta_{-}) - \frac{1}{4} M I_C^{0} \cos(\omega_1 t + \theta_0) + \frac{\sqrt{2}}{8} M I^{+} \cos(2\omega_1 t + \varphi_{+}) + \frac{\sqrt{2}}{8} M I^{-} \cos(2\omega_1 t + \varphi_{-}) + \frac{1}{2} I_c^{+} \sin(2\omega_1 t + \theta_{+}) +$$

$$\frac{1}{2}I_c^- \sin(2\omega_1 t + \theta_-) + \frac{1}{2}I_c^0 \sin(2\omega_1 t + \theta_0) + \frac{1}{4}MI_c^+ \sin(3\omega_1 t + \theta_+) + \frac{1}{4}MI_c^- \sin(3\omega_1 t + \theta_-) +$$

$$\frac{1}{4}MI_c^0 \sin(3\omega_1 t + \theta_0)$$

$$i_{c_l}(t) = S_{al_av}(t) \cdot i_{al}(t) = \frac{1}{2} I_{cda} - \frac{\sqrt{2}}{8}MI^+ cos\varphi_+ - \frac{\sqrt{2}}{8}MI^- cos\varphi_- + \frac{1}{2}MI_{cda} \sin(\omega_1 t) -$$

$$\frac{\sqrt{2}}{4}I^+ \sin(\omega_1 t + \varphi_+) - \frac{\sqrt{2}}{4}I^- \sin(\omega_1 t + \varphi_-) + \frac{1}{4}MI_C^+ \cos(\omega_1 t + \theta_+) + \frac{1}{4}MI_C^- \cos(\omega_1 t + \theta_-) +$$

$$\frac{1}{4}MI_C^0 \cos(\omega_1 t + \theta_0) + \frac{\sqrt{2}}{8}MI^+ \cos(2\omega_1 t + \varphi_+) + \frac{\sqrt{2}}{8}MI^- \cos(2\omega_1 t + \varphi_-) + \frac{1}{2}I_c^+ \sin(2\omega_1 t + \theta_+) +$$

$$\frac{1}{2}I_c^- \sin(2\omega_1 t + \theta_-) + \frac{1}{2}I_c^0 \sin(2\omega_1 t + \theta_0) - \frac{1}{4}MI_c^+ \sin(3\omega_1 t + \theta_+) - \frac{1}{4}MI_c^- \sin(3\omega_1 t + \theta_-) -$$

$$\frac{1}{4}MI_c^0 \sin(3\omega_1 t + \theta_0). \quad (3 - 3)$$

The dc component highlighted by pink color in (3 - 3) is zero during steady-state, which stands for a balanced active power between the ac and dc side. Solving the steady-state equation in (3 - 4) yields the dc component in circulating current

$$\frac{1}{2}I_{cda} - \frac{\sqrt{2}}{8}MI^+ \cos\varphi_+ - \frac{\sqrt{2}}{8}MI^- \cos\varphi_- = 0 \rightarrow I_{cda} = \frac{\sqrt{2}}{4}MI^+ \cos\varphi_+ + \frac{\sqrt{2}}{4}MI^- \cos\varphi_-$$

$$I_{cdb} = \frac{\sqrt{2}}{4}MI^+ \cos\varphi_+ + \frac{\sqrt{2}}{4}MI^- \cos(\varphi_- - 120^\circ)$$

$$I_{cdc} = \frac{\sqrt{2}}{4}MI^+ \cos\varphi_+ + \frac{\sqrt{2}}{4}MI^- \cos(\varphi_- + 120^\circ). \quad (3 - 4)$$

According to (3 - 4), the dc components in the three phase arm current are no longer equal to $I_{dc}/3$ (which is $\sqrt{2}MI^+ cos\varphi_+/4$ in normal operation) under unbalanced conditions, indicating uneven active power contribution among the three phases. Moreover, such asymmetrical distribution will be more severe with higher negative sequence current I^-. Therefore, I_{cdk} (k = a, b, c) in (3 - 1) should be replaced by (3 - 4) during the following derivation.

2) Capacitor Ripple Voltage: Multiplying the capacitor reactance $1/(j\omega_1 C_d)$ and the fundamental frequency capacitor charging current in (3 - 3), the fundamental frequency capacitor ripple voltages in the upper and lower arms in phase A are obtained as

$$u_{cu}^{(1)}(t)=\frac{1}{j\omega_1 C_{sub}}i_{c_u}^{(1)}=\frac{MI_{cda}}{2\omega_1 C_{sub}}\cos(\omega_1 t)-\frac{\sqrt{2}}{4\omega_1 C_{sub}}I^{+}\cos(\omega_1 t+\varphi_{+})-\frac{\sqrt{2}}{4\omega_1 C_{sub}}I^{-}\cos(\omega_1 t+\varphi_{-})-$$

$$\frac{1}{4\omega_1 C_{sub}}MI_c^{+}\sin(\omega_1 t+\theta_{+})-\frac{1}{4\omega_1 C_{sub}}MI_c^{-}\sin(\omega_1 t+\theta_{-})-\frac{1}{4\omega_1 C_{sub}}MI_c^{0}\sin(\omega_1 t+\theta_0)$$

$$u_{cl}^{(1)}(t)=\frac{1}{j\omega_1 C_{sub}}i_{c_l}^{(1)}=-\frac{MI_{cda}}{2\omega_1 C_{sub}}\cos(\omega_1 t)+\frac{\sqrt{2}}{4\omega_1 C_{sub}}I^{+}\cos(\omega_1 t+\varphi_{+})+\frac{\sqrt{2}}{4\omega_1 C_{sub}}I^{-}\cos(\omega_1 t+$$

$$\varphi_{-})+\frac{1}{4\omega_1 C_{sub}}MI_c^{+}\sin(\omega_1 t+\theta_{+})+\frac{1}{4\omega_1 C_{sub}}MI_c^{-}\sin(\omega_1 t+\theta_{-})+\frac{1}{4\omega_1 C_{sub}}MI_c^{0}\sin(\omega_1 t+\theta_0).\quad(3-5)$$

Similarly, the second and third order capacitor ripple voltages are given in (3 - 6) and (3 - 7)

$$u_{cu}^{(2)}(t)=\frac{1}{j2\omega_1 C_{sub}}i_{c_u}^{(2)}=\frac{\sqrt{2}MI^{+}}{16\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_{+})+\frac{\sqrt{2}MI^{-}}{16\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_{-})-\frac{I_c^{+}}{4\omega_1 C_{sub}}\cos(2\omega_1 t+$$

$$\theta_{+})-\frac{I_c^{-}}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_{-})-\frac{I_c^{0}}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)$$

$$u_{cl}^{(2)}(t)=\frac{1}{j2\omega_1 C_{sub}}i_{c_l}^{(2)}=\frac{\sqrt{2}MI^{+}}{16\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_{+})+\frac{\sqrt{2}MI^{-}}{16\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_{-})-\frac{I_c^{+}}{4\omega_1 C_{sub}}\cos(2\omega_1 t+$$

$$\theta_{+})-\frac{I_c^{-}}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_{-})-\frac{I_c^{0}}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)\quad(3-6)$$

$$u_{cu}^{(3)}(t)=\frac{1}{j3\omega_1 C_{sub}}i_{c_u}^{(3)}=\frac{MI_c^{+}}{12\omega_1 C_{sub}}\cos(3\omega_1 t+\theta_{+})+\frac{MI_c^{-}}{12\omega_1 C_{sub}}\cos(3\omega_1 t+\theta_{-})+\frac{MI_c^{0}}{12\omega_1 C_{sub}}\cos(3\omega_1 t+$$

$$\theta_0)$$

$$u_{cl}^{(3)}(t)=\frac{1}{j3\omega_1 C_{sub}}i_{c_l}^{(3)}=$$

$$-\frac{MI_c^{+}}{12\omega_1 C_{sub}}\cos(3\omega_1 t+\theta_{+})-\frac{MI_c^{-}}{12\omega_1 C_{sub}}\cos(3\omega_1 t+\theta_{-})-\frac{MI_c^{0}}{12\omega_1 C_{sub}}\cos(3\omega_1 t+\theta_0).\quad(3-7)$$

3) Voltage ripple in each phase: The ac side phase voltage ripple contributed by $u_{cu}^{(1)}$ and $u_{cl}^{(1)}$ can be expressed as

$$u_{ph_1}(t)=\frac{N}{2}[1-Msin(\omega_1 t)]\cdot u_{cu}^{(1)}(t)+\frac{N}{2}[1+Msin(\omega_1 t)]\cdot u_{cl}^{(1)}(t)=$$

$$-\frac{\sqrt{2}NMI^{+}}{8\omega_1 C_{sub}}\sin\varphi_{+}-\frac{\sqrt{2}NMI^{-}}{8\omega_1 C_{sub}}\sin\varphi_{-}+\frac{NM^2 I_c^{+}}{8\omega_1 C_{sub}}\cos\theta_{+}+\frac{NM^2 I_c^{-}}{8\omega_1 C_{sub}}cos\theta_{-}+\frac{NM^2 I_c^{0}}{8\omega_1 C_{sub}}cos\theta_0-$$

$$\frac{NM^2 I_{cda}}{4\omega_1 C_{sub}}\sin(2\omega_1 t)+\frac{\sqrt{2}NMI^{+}}{8\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_{+})+\frac{\sqrt{2}NMI^{-}}{8\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_{-})-\frac{NM^2 I_c^{+}}{8\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_{+})-$$

$$\frac{NM^2 I_c^{-}}{8\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_{-})-\frac{NM^2 I_c^{0}}{8\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0).\quad(3-8a)$$

Phase voltage ripple contributed by $u_{cu,l}^{(2)}$ and $u_{cu,l}^{(3)}$ can be calculated as

$$u_{ph_2}(t) = \frac{N}{2}[1 - Msin(\omega_1 t)] \cdot u_{cu}^{(2)}(t) + \frac{N}{2}[1 + Msin(\omega_1 t)] \cdot u_{cl}^{(2)}(t) =$$

$$\frac{\sqrt{2}NMI^{+}}{16\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{+}) + \frac{\sqrt{2}NMI^{-}}{16\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{-}) - \frac{NI_c^{+}}{4\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{+}) - \frac{NI_c^{-}}{4\omega_1 C_{sub}}\cos(2\omega_1 t +$$

$$\theta_{-}) - \frac{NI_c^{0}}{4\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_0) \quad (3 - 8b)$$

$$u_{ph_3}(t) = \frac{N}{2}[1 - Msin(\omega_1 t)] \cdot u_{cu}^{(3)}(t) + \frac{N}{2}[1 + Msin(\omega_1 t)] \cdot u_{cl}^{(3)}(t) = -\frac{NM^2 I_c^{+}}{24\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{+}) -$$

$$\frac{NM^2 I_c^{-}}{24\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{-}) - \frac{NM^2 I_c^{0}}{24\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_0) + \frac{NM^2 I_c^{+}}{24\omega_1 C_{sub}}\cos(4\omega_1 t + \theta_{+}) + \frac{NM^2 I_c^{-}}{24\omega_1 C_{sub}}\cos(4\omega_1 t +$$

$$\theta_{-}) + \frac{NM^2 I_c^{0}}{24\omega_1 C_{sub}}\cos(4\omega_1 t + \theta_0). \quad (3 - 8c)$$

As shown in (3 - 8), with arm current assumed in (3 - 1), the second and fourth order phase voltage components are generated, which in turn will create circulating current with the corresponding frequencies. Focusing on the dominant second order ripples and ignoring the fourth order items, the double line frequency phase voltage ripple in Phase A can be obtained by summing all the second order components in (3 - 8).

$$u_{ph_A}^{(2)}(t) = -\frac{\sqrt{2}NM^3 I^{+}}{16\omega_1 C_{sub}}\cos\varphi_{+}\sin(2\omega_1 t) + \frac{3\sqrt{2}NMI^{+}}{16\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{+}) - \frac{NM^2 I_c^{-}}{6\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{-}) -$$

$$\frac{NI_c^{-}}{4\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{-}) - \frac{\sqrt{2}NM^3 I^{-}}{32\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{-}) + \frac{3\sqrt{2}NMI^{-}}{16\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{-}) - \frac{NM^2 I_c^{0}}{6\omega_1 C_{sub}}\cos(2\omega_1 t +$$

$$\theta_0) - \frac{NI_c^{0}}{4\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_0) - \frac{\sqrt{2}NM^3 I^{-}}{32\omega_1 C_{sub}}\sin(2\omega_1 t - \varphi_{-}) - \frac{NM^2 I_c^{+}}{6\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{+}) -$$

$$\frac{NI_c^{+}}{4\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{+}). \quad (3 - 9)$$

Similarly, the second order voltage ripple in Phases B and C can be given in (3 - 10) and (3 - 11). The negative, zero, and positive sequence voltage ripples are distinguished by blue, red and black colors.

$$u_{ph_B}^{(2)}(t) =$$

$$-\frac{\sqrt{2}NM^3 I^{+}}{16\omega_1 C_{sub}}\cos\varphi_{+}\sin(2\omega_1 t + 120^{\circ}) + \frac{3\sqrt{2}NMI^{+}}{16\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{+} + 120^{\circ}) - \frac{NM^2 I_c^{-}}{6\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{-} +$$

$$120^{\circ}) - \frac{NI_c^{-}}{4\omega_1 C_{sub}}\cos(2\omega_1 t + \theta_{-} + 120^{\circ}) - \frac{\sqrt{2}NM^3 I^{-}}{32\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{-}) + \frac{3\sqrt{2}NMI^{-}}{16\omega_1 C_{sub}}\sin(2\omega_1 t + \varphi_{-}) -$$

$$\frac{NM^2I_c^0}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-\frac{NI_c^0}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-\frac{\sqrt{2}NM^3I^-}{32\omega_1 C_{sub}}\sin\left(2\omega_1 t-\varphi_- -120^\circ\right)-$$

$$\frac{NM^2I_c^+}{6\omega_1 C_{sub}}\cos\left(2\omega_1 t+\theta_+ -120^\circ\right)-\frac{NI_c^+}{4\omega_1 C_{sub}}\cos\left(2\omega_1 t+\theta_+ -120^\circ\right) \quad (3\text{ - }10)$$

$$u_{ph_c}^{(2)}(t)=$$

$$-\frac{\sqrt{2}NM^3I^+}{16\omega_1 C_{sub}}\cos\varphi_+\sin\left(2\omega_1 t-120^\circ\right)+\frac{3\sqrt{2}NMI^+}{16\omega_1 C_{sub}}\sin\left(2\omega_1 t+\varphi_+ -120^\circ\right)-\frac{NM^2I_c^-}{6\omega_1 C_{sub}}\cos\left(2\omega_1 t+\theta_- -\right.$$

$$\left.120^\circ\right)-\frac{NI_c^-}{4\omega_1 C_{sub}}\cos\left(2\omega_1 t+\theta_- -120^\circ\right)-\frac{\sqrt{2}NM^3I^-}{32\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_-)+\frac{3\sqrt{2}NMI^-}{16\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_-)-$$

$$\frac{NM^2I_c^0}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-\frac{NI_c^0}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-\frac{\sqrt{2}NM^3I^-}{32\omega_1 C_{sub}}\sin\left(2\omega_1 t-\varphi_- +120^\circ\right)-$$

$$\frac{NM^2I_c^+}{6\omega_1 C_{sub}}\cos\left(2\omega_1 t+\theta_+ +120^\circ\right)-\frac{NI_c^+}{4\omega_1 C_{sub}}\cos\left(2\omega_1 t+\theta_+ +120^\circ\right). \quad (3\text{ - }11)$$

As can be observed in (3 - 9) – (3 - 11), the positive and zero sequence voltage ripples only exist under unbalanced conditions, while the negative sequence component exists as long as the positive sequence modulation index M and phase current I^+ are nonzero. Sharing the same expression as that under normal conditions, the negative sequence circulating current will not change much if $M\,I^+$ has the same value as that in normal conditions.

B. With Negative Sequence Current Control

If dual current control is used, the negative sequence phase current can be eliminated, and thus the arm current in phase A becomes

$$i_{au}(t)=\frac{\sqrt{2}}{2}I^+\sin(\omega_1 t+\varphi_+)+I_{cda}+I_c^+\sin(2\omega_1 t+\theta_+)+I_c^-\sin(2\omega_1 t+\theta_-)+I_c^0\sin(2\omega_1 t+\theta_0)$$

$$i_{al}(t)=-\frac{\sqrt{2}}{2}I^+\sin(\omega_1 t+\varphi_+)+I_{cda}+I_c^+\sin(2\omega_1 t+\theta_+)+I_c^-\sin(2\omega_1 t+\theta_-)+I_c^0\sin(2\omega_1 t+\theta_0). \quad (3\text{ - }12)$$

On the other hand, the negative sequence component will exist in the average switching function due to the introduction of the dual current control, as described in (3 - 13).

$$S_{au_{av}}(t)=\frac{1}{2}[1-M^+\sin(\omega_1 t)-M^-\sin(\omega_1 t+\gamma_-)]$$

$$S_{al_av}(t)=\frac{1}{2}[1+M^+\sin(\omega_1 t)+M^-\sin(\omega_1 t+\gamma_-)] \quad (3\text{ - }13)$$

where M^+denotes the positive sequence modulation index; M^- and γ_- represent the negative sequence modulation index and its initial phase angle; $S_{au_av}(t)$ and $S_{al_av}(t)$ are average switching functions of the SMs in the upper and lower arms, respectively.

Following the same derivation steps above, the steady-state dc component in three phase arm currents can be given as

$$\frac{1}{2}I_{cda} - \frac{\sqrt{2}}{8}M^+I^+\cos\varphi_+ - \frac{\sqrt{2}}{8}M^-I^+\cos(\gamma_- - \varphi_+) = 0$$

$$\rightarrow I_{cda} = \frac{\sqrt{2}}{4}M^+I^+\cos\varphi_+ + \frac{\sqrt{2}}{4}M^-I^+\cos(\gamma_- - \varphi_+)$$

$$I_{cdb} = \frac{\sqrt{2}}{4}M^+I^+\cos\varphi_+ + \frac{\sqrt{2}}{4}M^-I^+\cos(\gamma_- - \varphi_+ - 120^\circ)$$

$$I_{cdc} = \frac{\sqrt{2}}{4}M^+I^+\cos\varphi_+ + \frac{\sqrt{2}}{4}M^-I^+\cos(\gamma_- - \varphi_+ + 120^\circ). \quad (3\text{ - }14)$$

According to (3 - 14), the negative sequence current control cannot equalize three phase dc arm currents.

Through the same derivation procedure, the double line frequency ac voltage ripple in phase A with negative sequence phase current control is derived in (3 - 15), where the negative, zero and positive sequence circulating three phase voltage ripples are still distinguished by blue, red and black colors. The voltage ripple for Phase B and C can be obtained in the same manner, with a phase shift of ±2π/3 in negative and positive sequence components, and no phase shift for zero sequence component.

As indicated in (3 - 15), with negative sequence phase current control, more combinations of current and modulation index serve as the sources of double line frequency phase voltage ripple. Moreover, compared to the result without negative sequence current control in (3 - 9), the circulating current components in (3 - 15) are no longer decoupled. For example, I_c^+ and I_c^0 contribute to negative sequence phase voltage ripple, and consequently are associated with I_c^-.

$$u_{ph}^{(2)}(t) = -\frac{\sqrt{2}N(M^+)^3I^+}{16\omega_1C_{sub}}\cos\varphi_+\sin(2\omega_1t) - \frac{\sqrt{2}NM^+(M^-)^2I^+}{16\omega_1C_{sub}}\sin(2\omega_1t+\varphi_+) - \frac{\sqrt{2}N(M^-)^3I^+}{32\omega_1C_{sub}}\sin(2\omega_1t+$$

$$3\gamma_- - \varphi_+) + \frac{3\sqrt{2}NM^+I^+}{16\omega_1C_{sub}}\sin(2\omega_1t+\varphi_+) - \frac{N(M^+)^2I_c^-}{6\omega_1C_{sub}}\cos(2\omega_1t+\theta_-) - \frac{N(M^-)^2I_c^-}{6\omega_1C_{sub}}\cos(2\omega_1t+\theta_-) -$$

$$\frac{NM^+M^-I_c^0}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0-\gamma_-)-\frac{NM^+M^-I_c^+}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_++\gamma_-)-\frac{NI_c^-}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_-)-$$

$$\frac{\sqrt{2}NM^-(M^+)^2I^+}{32\omega_1 C_{sub}}\sin(2\omega_1 t+\gamma_--\varphi_+)-\frac{\sqrt{2}NM^-(M^+)^2I^+}{8\omega_1 C_{sub}}\cos\varphi_+ sin(2\omega_1 t+\gamma_-)-\frac{\sqrt{2}N(M^-)^3I^+}{32\omega_1 C_{sub}}\sin(2\omega_1 t+$$

$$\gamma_-+\varphi_+)+\frac{3\sqrt{2}NM^-I^+}{16\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_++\gamma_-)-\frac{N(M^+)^2I_c^0}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-\frac{NI_c^0}{4\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-$$

$$\frac{NM^+M^-I_c^+}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_+-\gamma_-)-\frac{NM^+M^-I_c^-}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_-+\gamma_-)-\frac{N(M^-)^2I_c^0}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0)-$$

$$\frac{\sqrt{2}NM^-(M^+)^2I^+}{32\omega_1 C_{sub}}\sin(2\omega_1 t+\varphi_+-\gamma_-)-$$

$$\frac{\sqrt{2}NM^+(M^-)^2I^+}{16\omega_1 C_{sub}}\sin(2\omega_1 t-\varphi_++2\gamma_-)-\frac{\sqrt{2}NM^+(M^-)^2I^+}{16\omega_1 C_{sub}}\cos\varphi_+\sin(2\omega_1 t+2\gamma_-)-\frac{N(M^+)^2I_c^+}{6\omega_1 C_{sub}}\cos(2\omega_1 t+$$

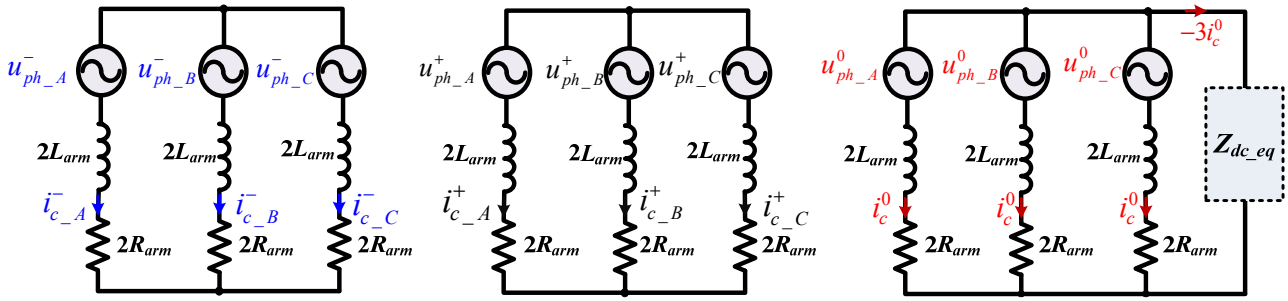
$$\theta_+)-\frac{NM^+M^-I_c^-}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_--\gamma_-)-\frac{NM^+M^-I_c^0}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_0+\gamma_-)-\frac{N(M^-)^2I_c^+}{6\omega_1 C_{sub}}\cos(2\omega_1 t+\theta_+)-$$

$$\frac{NI_c^+}{4\omega_1 C_{sub}}cos(2\omega_1 t+\theta_+)\,. \qquad (3\text{ - }15)$$

It is worth mentioning that the above analytical expressions are derived based on the generic inner relationship among current and voltage quantities, which are applicable to MMC under both rectifier and inverter modes.

3.3 Steady-state Model for Circulating Current Prediction

With the derived steady-state model for second order phase voltage ripple, the circulating current can be predicted by solving the equivalent circuit shown in Figure 3-4(a) and (b), where $u_{ph_j}^+$ and $u_{ph_j}^-$ (j = A, B, C) represent the corresponding double line frequency voltage ripple calculated in (3 - 9) and (3 - 15). The three-phase circulating current generated by these two voltage sources will add to zero and only circulate among phases. While for the zero sequence circulating currents generated by $u_{ph_j}^0$, they cannot cancel with each other and have to flow into the dc bus. Consequently, in addition to arm inductance L_{arm} and its ESR R_{arm}, the equivalent dc load impedance Z_{dc_eq} will be incorporated into its equivalent circuit, as shown in Figure 3-4 (c).



(a) Negative sequence (b) Positive sequence (c) Zero sequence

Figure 3-4. Equivalent circuit of the circulating current.

Based on these equivalent circuits, the following equations hold

$$i^-_{c_k}(t) = I^-_c \sin(2\omega_1 t + \theta_-) = -\frac{u^-_{ph_k}(t)}{j2\omega_1 \cdot 2L_{arm} + 2R_{arm}}$$

$$i^+_{c_k}(t) = I^+_c \sin(2\omega_1 t + \theta_+) = -\frac{u^+_{ph_k}(t)}{j2\omega_1 \cdot 2L_{arm} + 2R_{arm}} \quad (k = \text{A, B, C})$$

$$i^0_{c_k}(t) = I^0_c \sin(2\omega_1 t + \theta_0) = -\frac{u^0_{ph_k}(t)}{j2\omega_1 \cdot 2L_{arm} + 2R_{arm} + 3Z_{dc_{eq}}(t)}. \quad (3\text{ - }16)$$

From (2-16), circular interactions among double line frequency voltages and currents in MMC can be found. Moreover, by substituting (3 - 9) and (3 - 15) into (3 - 16) and solving the obtained equations, magnitudes (I^+_c, I^-_c, I^0_c) and initial phase angles (θ_+, θ_-, θ_0) of circulating current with and without negative sequence current control can be calculated theoretically. With the calculated circulating current, all the previous equations will become explicit.

In the following part, the solving process of the circulating current is analyzed in two cases, i.e., a MMC rectifier with resistive load and inverter load (MMC-HVDC in Figure 3-1).

3.3.1 Resistive Load

A. Without Negative Sequence Current Control

The corresponding equations with a dc side resistive load R_L is given in (3 -17), by replacing Z_{dc_eq} with R_L in (3 - 16). As mentioned above, the phase current amplitude I^+, I^-, phase angle φ_+, φ_-, and modulation index M are known variables. The magnitude and initial phase angle of different circulating

current components (I_c^+, I_c^-, I_c^0, θ_+, θ_- and θ_0) can be easily calculated using (3 - 17). In addition, capacitor charging current, capacitor voltage ripple, and phase voltage ripple can be expressed by substituting the calculated circulating current components into (3 - 3) – (3 - 8).

$$(B-2A)I^+cos\varphi_+ = -EI_c^-sin\theta_- - 2R_{arm}I_c^-cos\theta_-$$

$$BI^+sin\varphi_+ = EI_c^-cos\theta_- - 2R_{arm}I_c^-sin\theta_-$$

$$(B-A)I^-cos\varphi_- = -EI_c^0sin\theta_0 - (2R_{arm}+3R_L)I_c^0cos\theta_0$$

$$(B-A)I^-sin\varphi_- = EI_c^0cos\theta_0 - (2R_{arm}+3R_L)I_c^0sin\theta_0$$

$$-AI^-cos\varphi_- = -EI_c^+sin\theta_+ - 2R_{arm}I_c^+cos\theta_+$$

$$AI^-sin\varphi_- = EI_c^+cos\theta_+ - 2R_{arm}I_c^+sin\theta_+ \qquad (3\text{ - }17)$$

where,

$$A = \frac{\sqrt{2}NM^3}{32\omega_1 C_{sub}} \quad B = \frac{3\sqrt{2}NM}{16\omega_1 C_{sub}} \quad C = \frac{NM^2}{6\omega_1 C_{sub}} \quad D = \frac{N}{4\omega_1 C_{sub}} \quad E = C + D - 4\omega_1 L_{arm}$$

Under slightly unbalanced conditions, the magnitude of negative sequence circulating current keeps almost the same since I^+ and M will not change much. Nevertheless, if a single-line-to-ground (SLG) fault occurs, M will decrease because of the lost phase voltage, while I^+ tends to increase to maintain dc voltage and/or output power. Therefore, the negative sequence circulating current will vary accordingly with different control schemes and current limit settings. As for the positive and zero sequence circulating current, their magnitudes are positive proportional to the negative sequence phase current, and will reduce with lower M. Zero sequence circulating current, limited by dc load impedance, will be much lower than the other two sequence components in a MMC rectifier with a light load.

B. With Negative Sequence Current Control

By substituting (3 - 15) to (3 - 16) and replacing Z_{dc_eq} with R_L, the equations used for circulating current calculation with a resistive load R_L are given in (3 - 18) when negative sequence current control is activated.

$$-2AI^+cos\varphi_+ - BI^+cos\varphi_+ - CI^+\cos(3\gamma_- - \varphi_+) + DI^+M^+cos\varphi_+ + GI_c^0sin(\theta_0 - \gamma_-)$$

$$+GI_c^+sin(\theta_+ + \gamma_-) = -KI_c^-sin\theta_- - 2R_{arm}I_c^-cos\theta_-$$

$$-BI^{+}sin\varphi_{+} - CI^{+}sin(3\gamma_{-} - \varphi_{+}) + DI^{+}M^{+}sin\varphi_{+} - GI_c^{0}cos(\theta_0 - \gamma_{-}) - GI_c^{+}cos(\theta_{+} + \gamma_{-}) =$$

$$KI_c^{-}cos\theta_{-} - 2R_{arm}I_c^{-}sin\theta_{-}$$

$$-PI^{+}\cos(\gamma_{-} - \varphi_{+}) - 4PI^{+}\cos\varphi_{+}cos\gamma_{-} - CI^{+}\cos(\gamma_{-} + \varphi_{+}) + DI^{+}M^{-}\cos(\gamma_{-} + \varphi_{+})$$

$$+GI_c^{+}\sin(\theta_{+} - \gamma_{-}) + GI_c^{-}sin(\theta_{-} + \gamma_{-}) = -KI_c^{0}sin\theta_0 - (2R_{arm}+3R_L)I_c^{0}cos\theta_0$$

$$-PI^{+}\sin(\gamma_{-} - \varphi_{+}) - 4PI^{+}\cos\varphi_{+}sin\gamma_{-} - CI^{+}\sin(\gamma_{-} + \varphi_{+}) + DI^{+}M^{-}\sin(\gamma_{-} + \varphi_{+})$$

$$-GI_c^{+}cos(\theta_{+} - \gamma_{-}) - GI_c^{-}cos(\theta_{-} + \gamma_{-}) = KI_c^{0}cos\theta_0 - (2R_{arm}+3R_L)I_c^{0}sin\theta_0$$

$$-PI^{+}\cos(\varphi_{+} - \gamma_{-}) - BI^{+}\cos(2\gamma_{-} - \varphi_{+}) - BI^{+}\cos\varphi_{+}\cos2\gamma_{-} + GI_c^{-}\sin(\theta_{-} - \gamma_{-})$$

$$+GI_c^{0}sin(\theta_0 + \gamma_{-}) = -KI_c^{+}sin\theta_{+} - 2R_{arm}I_c^{+}cos\theta_{+}$$

$$-PI^{+}\sin(\varphi_{+} - \gamma_{-}) - BI^{+}\sin(2\gamma_{-} - \varphi_{+}) - BI^{+}\cos\varphi_{+}\sin2\gamma_{-} - GI_c^{-}\cos(\theta_{-} - \gamma_{-})$$

$$-GI_c^{0}cos(\theta_0 + \gamma_{-}) = KI_c^{+}cos\theta_{+} - 2R_{arm}I_c^{+}sin\theta_{+} \qquad (3\text{ - }18)$$

where,

$$A = \frac{\sqrt{2}N(M^{+})^3}{32\omega_1 C_{sub}} \quad B = \frac{\sqrt{2}NM^{+}(M^{-})^2}{16\omega_1 C_{sub}} \quad C = \frac{\sqrt{2}N(M^{-})^3}{32\omega_1 C_{sub}} \quad D = \frac{3\sqrt{2}N}{16\omega_1 C_{sub}} \quad E = \frac{N(M^{+})^2}{6\omega_1 C_{sub}} \quad F = \frac{N(M^{-})^2}{6\omega_1 C_{sub}} \quad G =$$

$$\frac{NM^{+}M^{-}}{6\omega_1 C_{sub}} \quad H = \frac{N}{4\omega_1 C_{sub}} \quad P = \frac{\sqrt{2}N(M^{+})^2M^{-}}{32\omega_1 C_{sub}} \quad K = E + F + H - 4\omega_1 L_{arm}.$$

Compared to (3 - 17), the positive and zero sequence circulating current cannot be removed by the elimination of negative sequence current I^{-}. Oppositely, they are generated not only by different combinations of positive sequence current I^{+} and modulation index M^{+}, M^{-}, but also by other circulating current components by a ratio of G. Due to such couplings, (3 - 18) becomes more difficult to solve, and the variation of circulating current magnitude and phase angles is not straightforward.

3.3.2 MMC Load

In a point-to-point MMC-HVDC system (Figure 3-1), a MMC inverter instead of a resistor serves as the dc load. According to Figure 3-4, the equations for negative and positive sequence circulating currents in (3 - 17) and (3 - 18) keep the same, while the dc impedance Z_{dc_eq} in Figure 3-4(c) changes from R_L to the dc equivalent impedance of the MMC inverter. In order to obtain the equivalent circuit of zero sequence circulating current in a MMC-HVDC system, the dc equivalent impedance of the MMC inverter is derived as follows.

From the single phase equivalent circuit in Figure 3-3, one obtains:

$$v_{du} - v_{cu}^k - R_{arm} i_u^k - L_{arm} \frac{di_u^k}{dt} = v_g^k \qquad -v_{dl} + v_{cl}^k + R_{arm} i_l^k + L_{arm} \frac{di_l^k}{dt} = v_g^k. \tag{3 - 19}$$

Adding (3 - 19) and (3 - 20) yields

$$L_{arm} \frac{di_u^k}{dt} + L_{arm} \frac{di_l^k}{dt} + v_{cu}^k + v_{cl}^k + R_{arm} i_u^k + R_{arm} i_l^k = v_d \tag{3 - 20}$$

where v_d is the pole to pole dc bus voltage, and $v_d = v_{du} + v_{dl}$.

According to [127] [128], $v_{cu}{}^k$ and $v_{cl}{}^k$ can be calculated as:

$$v_{cu}^k = n_u^k v_{cu}^{\Sigma k} \quad v_{cl}^k = n_l^k v_{cl}^{\Sigma k} \tag{3 - 21}$$

where $n_u{}^k$ and $n_l{}^k$ are insertion indices and $v_{cu,}^{\Sigma \mathrm{k}}$ $v_{cl}^{\Sigma \mathrm{k}}$ are the sum of capacitor voltages in phase k ($k = a, b, c$). In addition, $n_u{}^k$ and $n_l{}^k$ are given as $\mathrm{v_c^{\Sigma}} \approx 2\mathrm{V_d} \mathrm{v_c^{\Sigma}} \approx 2\mathrm{V_d}$

$$n_u^k = \frac{v_{du} - v_s^{refk} - v_{cir}^{refk}}{v_{cu}^{\Sigma k}} \approx \frac{v_{du} - v_s^{refk} - v_{cir}^{refk}}{V_d}$$

$$n_l^k = \frac{v_{dl} + v_s^{refk} - v_{cir}^{refk}}{v_{cl}^{\Sigma k}} \approx \frac{v_{dl} + v_s^{refk} - v_{cir}^{refk}}{V_d} \tag{3 - 22}$$

where $v_s{}^{refk}$ is the reference of the fundamental frequency output voltage and $v_{cir}{}^{refk}$ is the reference generated by the circulating current control. An assumption is made here that the submodule capacitance C_{sub} is selected to be large enough to guarantee that $v_{cu}^{\Sigma \mathrm{k}} \approx v_{cl}^{\Sigma \mathrm{k}} \approx V_d$ in each phase.

Substituting (3 - 23) into (3 - 22) yields

$$v_{cu}^k + v_{cl}^k = \frac{v_{du} - v_s^{refk} - v_{cir}^{refk}}{V_d} v_{cu}^{\Sigma k} + \frac{v_{dl} + v_s^{refk} - v_{cir}^{refk}}{V_d} v_{cl}^{\Sigma k} = \frac{1}{2} v_c^{\Sigma k} - \frac{v_{cir}^{refk}}{V_d} v_c^{\Sigma k} - \frac{v_s^{refk}}{V_d} v_c^{\Delta k} \tag{3 - 23}$$

where $v_c^{\Sigma \mathrm{k}}$ is the total capacitor voltage in phase k, and $v_c^{\Sigma \mathrm{k}} = v_{cu}^{\Sigma \mathrm{k}} + v_{cl}^{\Sigma \mathrm{k}}$; $v_c^{\Delta \mathrm{k}}$ is the unbalance capacitor voltage in phase k, and $v_c^{\Delta \mathrm{k}} = v_{cu}^{\Sigma \mathrm{k}} - v_{cl}^{\Sigma \mathrm{k}}$.

Substituting (3 - 24) into (3 - 21) and adding the three phase equations together yield

$$L_{arm} \frac{d}{dt} \sum_{k=1}^{3} i_u^k + L_{arm} \frac{d}{dt} \sum_{k=1}^{3} i_l^k + \frac{1}{2} \sum_{k=1}^{3} v_c^{\Sigma k} - \frac{1}{V_d} \sum_{k=1}^{3} v_{cir}^{refk} v_c^{\Sigma k} - \frac{1}{V_d} \sum_{k=1}^{3} v_s^{refk} v_c^{\Delta k} +$$

$$R_{arm} \sum_{k=1}^{3} i_u^k + R_{arm} \sum_{k=1}^{3} i_l^k = 3 v_d. \tag{3 - 24}$$

As shown in Figure 3-3, the summation of three phase upper or lower arm currents is dc current, i.e.,

$$\sum_{k=1}^{3} i_u^k = \sum_{k=1}^{3} i_l^k = \sum_{k=1}^{3} i_c^k = i_d. \quad (3 - 25)$$

According to [127], the dynamics of a MMC can be described by the state variables $v_c^{\Sigma k}$ and $v_c^{\Delta k}$, as shown in (3 - 27) to (3 - 29). Moreover, $v_c^{\Sigma k}$ equals to $2V_d$ in the steady-state, and $v_c^{\Delta k}$ only contains fundamental frequency component.

$$\frac{C_{sub}}{N}\frac{dv_c^{\sum k}}{dt} = -\frac{v_s^{refk} i_s^k}{V_d} + (1 - \frac{2v_{cir}^{refk}}{V_d}) i_c^k \quad (3 - 26)$$

$$\frac{C_{sub}}{N}\frac{dv_c^{\Delta k}}{dt} = (1 - \frac{2v_{cir}^{refk}}{V_d})\frac{i_s^k}{2} - \frac{2v_s^{refk}}{V_d} i_c^k \quad (3 - 27)$$

$$L_{arm}\frac{di_c^k}{dt} = \frac{1}{2}\left(v_d - \frac{v_c^{\Sigma k}}{2} + \frac{v_{cir}^{refk}}{V_d} v_c^{\Sigma k} + \frac{v_s^{refk}}{V_d} v_c^{\Delta k}\right) - R_{arm} i_c^k. \quad (3 - 28)$$

If v_s^{ref} and i_s in phase A are controlled as

$$v_s^{ref} = V_s \cos(\omega_1 t) \quad i_s = I_s \cos(\omega_1 t - \varphi). \quad (3 - 29)$$

Equation (3 - 27) can be rewritten as

$$\frac{C_{sub}}{N}\frac{dv_c^{\sum k}}{dt} = -\frac{V_s I_s cos\varphi}{2V_d} - \frac{V_s I_s \cos(2\omega_1 t - \varphi)}{2V_d} + \left(1 - \frac{2v_{cir}^{refk}}{V_d}\right) i_c^k. \quad (3 - 30)$$

As can be observed, a second order ripple is contained in $v_c^{\Sigma k}$, and the dc component in the circulating current can be calculated as

$$I_{c0} = \frac{V_s I_s cos\varphi}{2V_d}. \quad (3 - 31)$$

In the following derivation of dc side equivalent impedance, two cases (with and without circulating current control) are considered.

A. Without Circulating Current Control

If no circulating current control is employed, i.e., $v_{cir}^{refk} = 0$, the following equations hold:

$$L_{arm}\frac{d}{dt}\sum_{k=1}^{3} i_u^k + L_{arm}\frac{d}{dt}\sum_{k=1}^{3} i_l^k + \frac{1}{2}\sum_{k=1}^{3} v_c^{\Sigma k} - \frac{1}{V_d}\sum_{k=1}^{3} v_s^{refk} v_c^{\Delta k} + R_{arm}\sum_{k=1}^{3} i_u^k + R_{arm}\sum_{k=1}^{3} i_l^k =$$

$$3V_d \quad (3 - 32)$$

$$\frac{C_{sub}}{N}\frac{dv_c^{\sum k}}{dt} = -\frac{V_s I_s cos\varphi}{2V_d} - \frac{V_s I_s \cos(2\omega_1 t - \varphi)}{2V_d} + i_c^k. \quad (3 - 33)$$

Therefore, the three phase summation of (3 - 34) yields:

$$\frac{d}{dt}\sum_{k=1}^{3} v_c^{\Sigma k} = \frac{N}{C_{sub}}\left(-\frac{3V_s I_s cos\varphi}{2V_d} + i_d\right). \quad (3 - 34)$$

For simplicity, the MMC system, including upper and lower arm impedance, is assumed to be symmetrical, and $v_c^{\Delta k} = 0$, so no dc components will be generated by the product of v_s^{refk} and $v_c^{\Delta k}$, hence,

$$\sum_{k=1}^{3} v_s^{refk}\, v_c^{\Delta k} = 0. \quad (3 - 35)$$

Substituting (3 - 26), (3 - 35) and (3 - 36) into (3 - 33) and applying linearization, one obtains:

$$\tilde{v}_d = \frac{2L_{arm}}{3}\frac{d\tilde{\imath}_d}{dt} + \frac{N}{6C_{sub}}\int \tilde{\imath}_d + \frac{2R_{arm}}{3}\tilde{\imath}_d \rightarrow \frac{\tilde{v}_d(s)}{\tilde{\imath}_d(s)} = \frac{2sL_{arm}}{3} + \frac{N}{6sC_{sub}} + \frac{2R_{arm}}{3}. \quad (3 - 36)$$

During the linearization procedure, no product of two small signal items is found at the second harmonic frequency, and thus the system has a linear characteristic for the double line frequency voltage and current ripples. According to (3 - 37), if no circulating current control is used, a MMC inverter can be regarded as a series connected R-L-C branch in the dc side. The parameters of this R-L-C branch are independent of implemented control schemes, and will remain with open-loop, current-loop or power-loop regulation.

B. With Circulating Current Control

For simplicity, a proportional circulating current control applied in [127] is adopted, and

$$v_{cir}^{refk} = R_a(i_c^{ref} - i_c) + \hat{R} i_c^{ref} \quad (3 - 37)$$

where $\hat{R}$ is an estimation of R_{arm}, and $\hat{R} i_c^{ref}$ can be interpreted as a compensation of the voltage drop on R_{arm} in steady-state. The circulating current reference is the same as I_{c0} in (3 - 32).

Substituting (3 - 38) into (3 - 31), applying linearization and disregarding the quasi-stationary components, one obtains

$$\frac{1}{2}\sum_{k=1}^{3} \tilde{v}_c^{\Sigma k} = \frac{N}{2C_{sub}}\left(1 + \frac{2(R_a - R_{arm})I_{c0}}{V_d}\right)\int \tilde{\imath}_d. \quad (3 - 38)$$

Substituting (3 - 38) into the fourth term of (3 - 25), the following equation holds

$$\frac{1}{V_d}\sum_{k=1}^{3} \tilde{v}_{cir}^{refk}\tilde{v}_c^{\Sigma k} = \frac{1}{V_d}\sum_{k=1}^{3}\left(-R_a \cdot 2V_d\, \tilde{\imath}_c^k + \frac{N}{C_{sub}}R_{arm}I_{c0} \cdot \left(1 + \frac{2(R_a - R_{arm})I_{c0}}{V_d}\right)\int \tilde{\imath}_c^k\right) = \frac{1}{V_d}\left(-R_a \cdot 2V_d \cdot \right.$$

$$\left.\tilde{\imath}_d + \frac{N}{C_{sub}}R_{arm}I_{c0} \cdot \left(1 + \frac{2(R_a - R_{arm})I_{c0}}{V_d}\right)\int \tilde{\imath}_d\right) = -2R_a\tilde{\imath}_d + \left(1 + \frac{2(R_a - R_{arm})I_{c0}}{V_d}\right)\frac{NR_{arm}I_{c0}}{V_d C_{sub}}\int \tilde{\imath}_d. \quad (3 - 39)$$

Substituting (3 - 26), (3 - 36), (3 - 39) and (3 - 40) into (3 - 25) yields

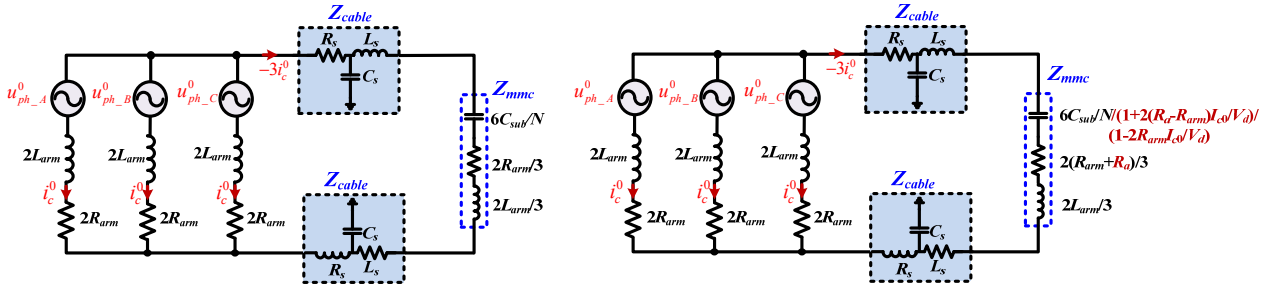
$$2L_{arm}\frac{d\tilde{\imath}_d}{dt}+\frac{N}{2C_{sub}}\left(1+\frac{2(R_a-R_{arm})I_{c0}}{V_d}\right)\int\tilde{\imath}_d-\left(-2R_a\tilde{\imath}_d+\left(1+\frac{2(R_a-R_{arm})I_{c0}}{V_d}\right)\frac{NR_{arm}I_{c0}}{V_dC_{sub}}\int\tilde{\imath}_d\right)+$$

$$2R_{arm}\tilde{\imath}_d=3\tilde{v}_d\rightarrow\frac{\tilde{v}_d(s)}{\tilde{\imath}_d(s)}=\frac{2sL_{arm}}{3}+\frac{2}{3}(R_a+R_{arm})+\frac{N}{6sC_{sub}}\left(1+\frac{2(R_a-R_{arm})I_{c0}}{V_d}\right)\left(1-\frac{2R_{arm}I_{c0}}{V_d}\right).\quad(3-40)$$

Compared to (3 - 37), the dc equivalent impedance is still linear at the second harmonic frequency, and a MMC can also be considered as a series connected R-L-C branch, while the equivalent resistance and capacitance vary with the proportional coefficient R_a selected in the circulating current control.

In practice, PR control with resonance frequency of 120 Hz (2nd order) instead of proportional control, may be used to suppress circulating current under normal and unbalanced conditions. Under such circumstances, the derived equivalent dc impedance in (3 - 41) is still applicable. The only modification is that R_a in (3 - 41) should be replaced by the gain of the PR controller at the resonant frequency.

Based on (3 - 37) and (3 - 41), the equivalent circuit of the zero sequence circulating current i_c^0 in a MMC-HVDC is shown in Figure 3-5. The double line frequency dc current ripple, which equals to $3i_c^0$, is suppressed by both dc cable impedance (Z_{cable}) and dc side equivalent impedance of MMC inverter (Z_{mmc}). Therefore, in a system with long dc cables and/or high circulating current control coefficient R_a, no obvious second order current ripple will be found in the dc current under SLG fault conditions.



(a) Without circulating current control (b) With circulating current control

Figure 3-5. Equivalent circuit of the second order dc voltage ripple under SLG fault conditions.

As shown in (3 - 9) and (3 - 15), the elimination of i_c^0 will reduce but cannot remove the second order phase voltage ripple on the dc cables and MMC inverter. This voltage ripple may lead to distorted ac

voltage in MMC_2 station through modulation and feedback control loops, which requires additional control schemes to mitigate. If the converter regulating dc voltage suffers unbalanced ac voltages, dc voltage V_d in (3 - 23) - (3 - 32) cannot be regarded as a constant value, and the corresponding voltage regulators should be considered in the dc impedance derivation.

3.4 Experimental Verification

To verify the theoretical analysis and developed impedance model, a scaled-down three-phase MMC is built, as shown in Figure 3-6. The control schemes are implemented by dSPACE DS1103 and FPGA (Cyclone IV DE0-Nano). Serving as a comprehensive interface for multiple applications, the DS1103 can provide 20 fast ADC channels. Nevertheless, for the implementation of capacitor voltage balancing control, circulating current control, and normal active/reactive power control, all capacitor voltages, arm currents, phase currents and ac voltage of the three-phase MMC inverter prototype need to be detected and sampled in a high speed. Therefore, the SMs per arm cannot be increased freely without additional hardware. Moreover, given that the number of SMs has little impact on the model verification, two cells per arm (N = 2) is used in this paper to achieve low hardware requirement, and the assignment of AD channels is given in Table 3-1.

For high equivalent switching frequency and relatively simple implementation, the $N + 1$ level phase shift PWM (PS-PWM) modulation scheme is adopted. Additionally, the widely used capacitor voltage sorting and balancing control is applied to guarantee operation performance of MMC under both normal as well as unbalanced conditions.

Table 3-1. A/D channel assignment for DS1103.

	Upper arm current	Lower arm current	Phase current	Phase voltage	DC voltage	Capacitor voltage
Number	1×3	0 (i_{ph} - i_p)	1×3	1×3	1	4×3
Total	3	0	3	3	1	12 (10 main AD, 2 slave AD)

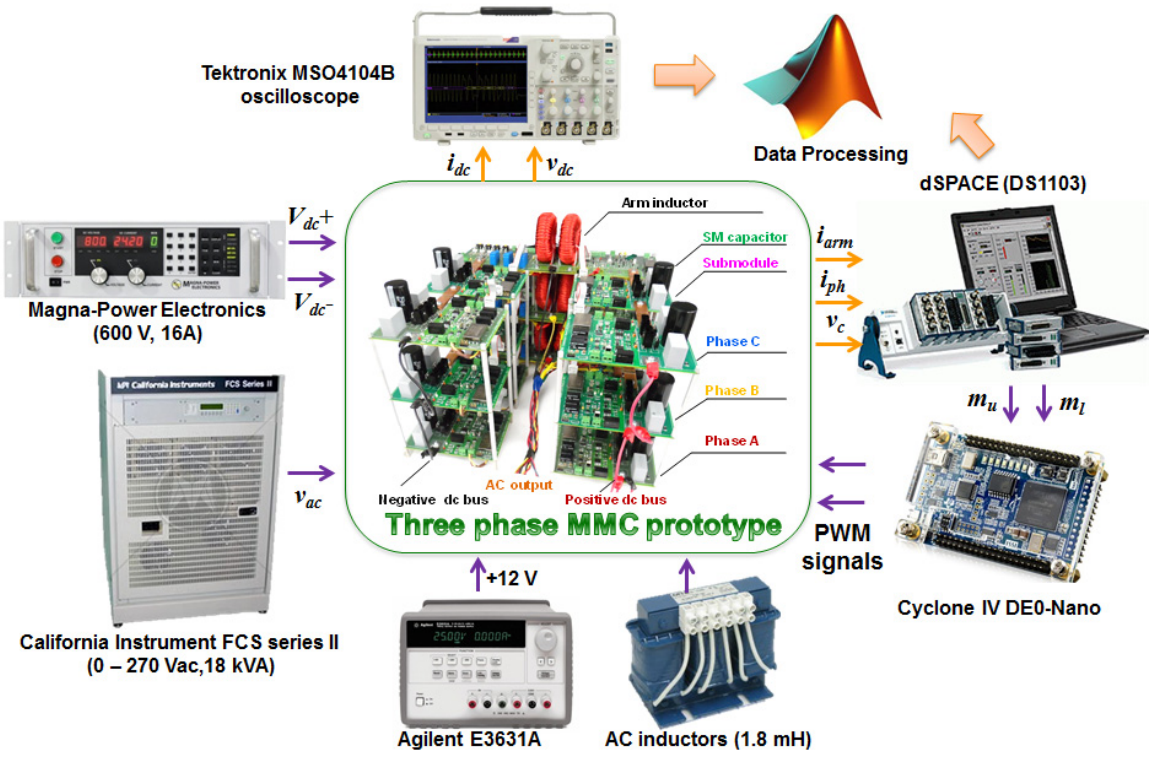


Figure 3-6. Experimental test and measurement setup.

Three cases, including MMC rectifier with resistive load under SLG fault, MMC inverter with resistive load under SLG fault, and MMC inverter with second order voltage ripple in dc side, are studied. To create serious unbalanced conditions, a SLG fault is emulated by setting phase C voltage to zero through an AC power supply (FCS Series II by California Instruments). Compared to a real SLG fault, voltage and current characteristics in the converter side are almost the same. For convenience, the "SLG fault" mentioned in the following analysis refers to this emulation. To prevent the potential damage or degradation of power semiconductor devices under fault conditions, the current reference is limited to 1.2 times of the rated phase current.

3.4.1 MMC Rectifier with Resistive Load under SLG Fault

The configuration of the MMC rectifier is illustrated in Figure 3-7(a), and its main circuit parameters are given in Table 3-2. Figure 3-8 shows the comparison between experimental and calculation results of circulating current under SLG fault. When the negative sequence current control is not activated, a

deviation appears between the calculated and tested magnitudes of circulating current. During the derivation of second order voltage ripple in (3 - 9), the negative sequence modulation index M^- is assumed to be zero. In experiments, nevertheless, a small M^- is introduced by the dc voltage feedback control, which mainly induces the mismatch in Figure 3-8(a).

Table 3-2. Main circuit parameters of MMC prototype.

Parameters	Values	Parameters	Values
Max. DC Link voltage V_{dc}	150 V	No. of sub-modules in each arm N	2
Voltage frequency	60 Hz	Sub-module capacitance C_{sub}	2200 μF
Arm inductance L_{arm}	0.74 mH	Carrier frequency f_c	1 kHz
Arm inductor ESR R_{arm}	0.06 Ω	DC side inductance L_{dc}	0.45 mH
AC side inductance L_{AC}	1.8 mH	ESR of DC inductance R_{dc}	0.05 Ω
Equivalent resistance of AC inductors	0.09 Ω	Load resistance R_L	30 Ω

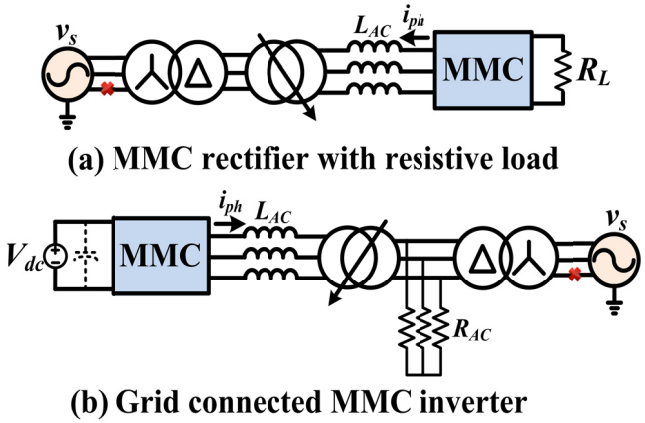
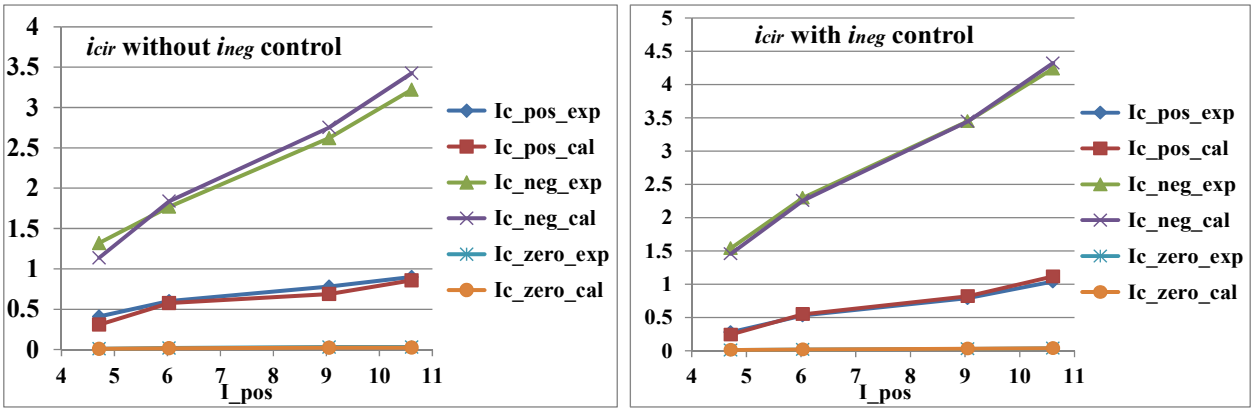


Figure 3-7. Configuration of the experimental system with phase C open.

With negative sequence current control, since the assumption $I^- = 0$ in (3 - 13) always holds when dual current control operates, the mismatch between calculation and experimental results of positive and negative sequence circulating current in Figure 3-8(b) is greatly reduced within the tested range. The magnitude of zero sequence circulating current is below 0.04 A in both cases with a dc resistance of 30 Ω.

The negative sequence current control also leads to an apparent magnitude increase of negative and positive sequence circulating currents, as shown in Figure 3-8(b).



(a) Without negative sequence current control (b) With negative sequence current control

Figure 3-8. Comparison between experimental and calculation results of circulating current in MMC rectifier under SLG fault.

3.4.2 MMC Inverter under SLG Fault

To further verify the derived model, a MMC inverter under SLG fault is also investigated with the same main circuit parameters in Table 3-2, as shown in Figure 3-7(b). Since the ac power supply v_s used in experiment cannot absorb active power, three 5 Ω resistors are connected at the output of the inverter. Figure 3-9 illustrates the comparison between calculation and experimental results of circulating current in a MMC inverter under SLG fault. The mismatch reduces from 0.4 A (Figure 3-9(a)) to less than 0.1 A (Figure 3-9(b)) when the negative sequence current control is activated. However, due to lower dc impedance Z_{dc_eq}, variation of phase current and modulation index, the magnitude of negative sequence component drops a little, while positive and zero sequence circulating current has a slight increase.

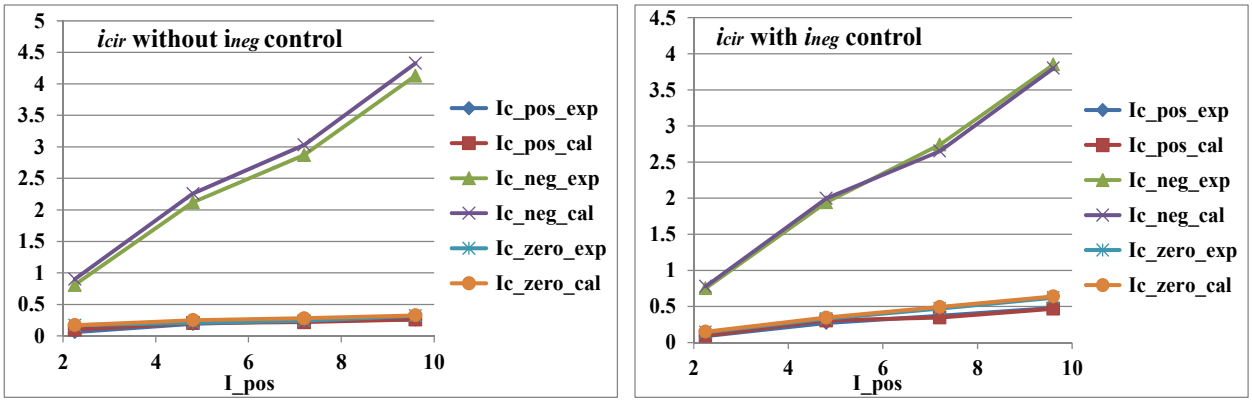
3.4.3 MMC Inverter with Second Order Voltage Input in DC Side

A MMC inverter in Figure 3-10 is used to verify the derived dc equivalent impedance and its main parameters are the same as Table 3-2 except the dc link voltage V_{dc} = 100 V. An H-bridge converter

controlled by DSP (TMS320F28335) is used to generate a second order voltage and emulate the dc voltage ripple under SLG fault condition in the rectifier station, as shown in Figure 3-11. A dc reactor of 0.45 mH is used for cable impedance emulation.

Figure 3-12, Figure 3-13 and Figure 3-14 show the selected experimental results when the proportional coefficient $R_a = 0$, and the second order dc voltage ripple v_2 has magnitudes of 6 V and 12 V, respectively. Compared to Figure 3-12, the 2nd order harmonic in the ac component of v_{rmmc} (v_{rmmc_ac}) has an evident increase with higher v_2 (v_{r_ac}) (Figure 3-13(a)), and the 2nd order dc side current i_{dc} also becomes much larger (Figure 3-13(b)).

Figure 3-14 illustrates the experimental results with proportional coefficient $R_a = 3$ when the magnitude of v_2 is set to 12 V. As can be observed, although larger R_a induces higher v_{rmmc_ac}, it helps to achieve smaller 2nd order dc side current and more sinusoidal arm currents. Additionally, the unbalanced phase current in Figure 3-14(b) is also suppressed. Figure 3-15 shows the phase and dc side current with current loop control when $v_2 = 12$ V. The dominant 3rd order harmonics in the phase current generated by the 2nd order dc voltage ripple decreases from 1.43 % to 1.09 %, and it can be further reduced by increasing the bandwidth and low frequency gain of the current control loop.



(a) Without negative sequence current control (b) With negative sequence current control

Figure 3-9. Comparison between experimental and calculation results of circulating current in MMC inverter under SLG fault.

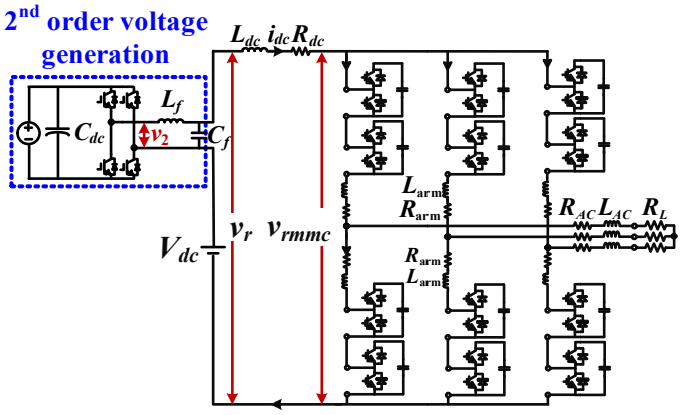


Figure 3-10. Configuration of the experimental system.

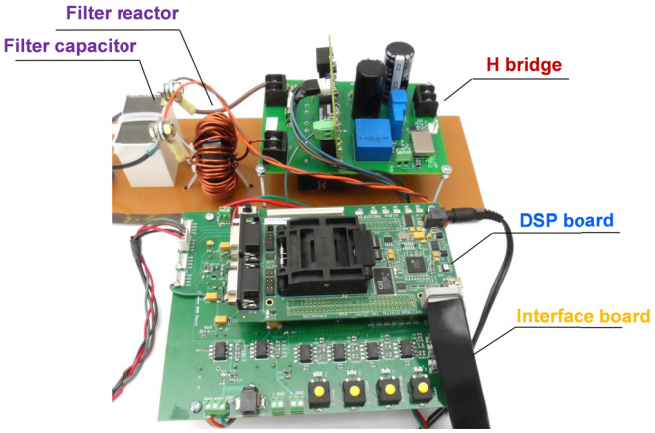
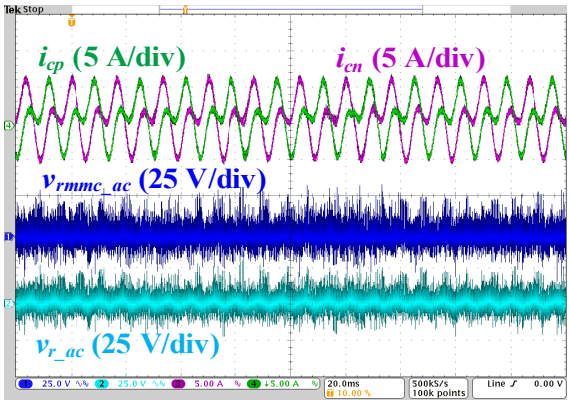
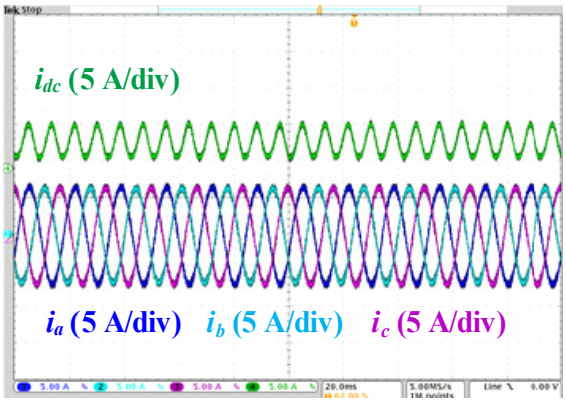


Figure 3-11. Second order voltage source using an H bridge.

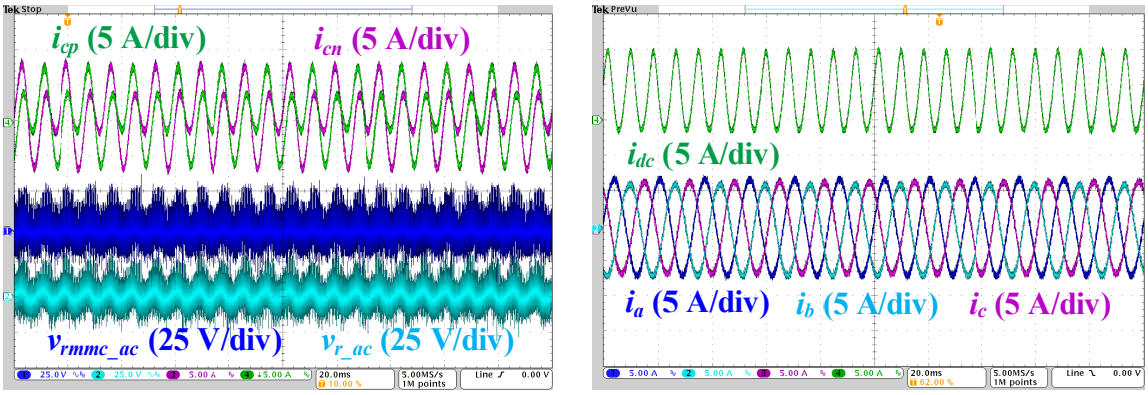


(a) Arm currents, ac components of v_{rmmc} and v_r



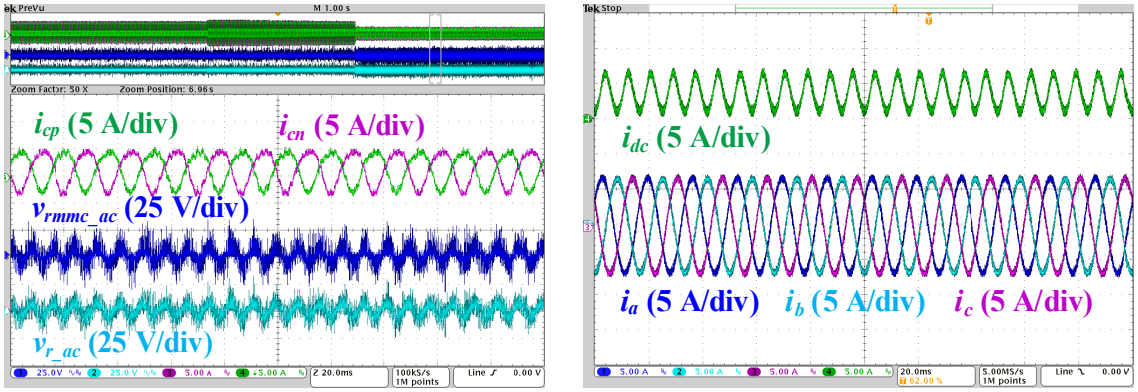
(b) DC side current and output phase current

Figure 3-12. Experimental waveforms with $v_2 = 6$, $R_a = 0$.



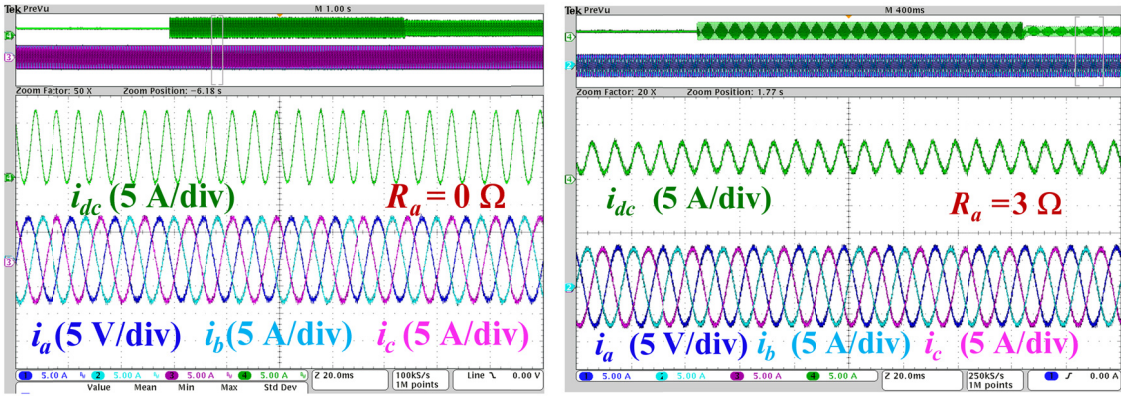
(a) Arm currents, ac components of v_{rmmc} and v_r (b) DC side current and output phase current

Figure 3-13. Experimental waveforms with $v_2 = 12$, $R_a = 0$.



(a) Arm currents, ac components of v_{rmmc} and v_r (b) dc side current and output phase current

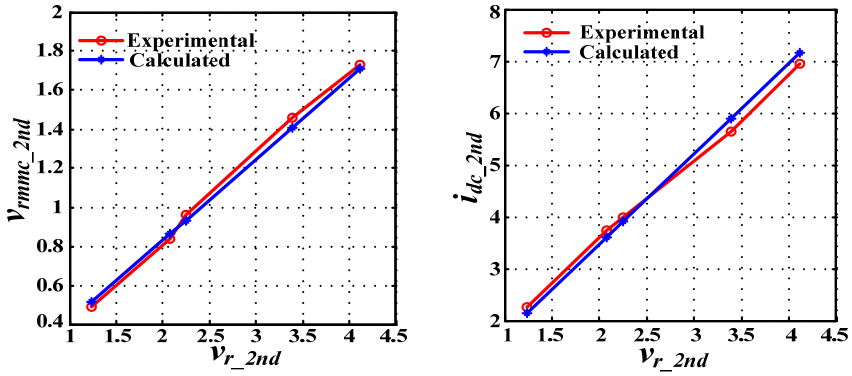
Figure 3-14. Experimental waveforms with $v_2 = 12$, $R_a = 3$.



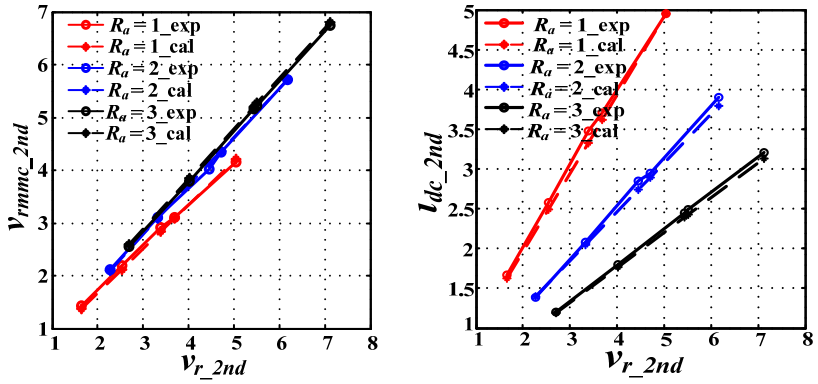
(a) $R_a = 0$ (b) $R_a = 3$

Figure 3-15. Current loop control experimental waveforms with $v_2 = 12$.

Comparing Figure 3-14 (b) with Figure 3-15(b), the double line frequency dc current ripple has almost the same magnitudes, which verifies that the control schemes have only slight impact on the derived dc equivalent impedance. Figure 3-16 shows the comparison between experimental and calculated results with and without circulating current control. In both cases, the errors of 2nd order MMC dc terminal voltage (v_{rmmc_2nd}) and dc side current (i_{dc_2nd}) are less than 1 % within the plotted range, no matter what control method (open-loop or current loop control) is applied.



(a) Without circulating current control



(b) With circulating current control.

Figure 3-16. Comparison between experimental and calculated results.

Compared to Figure 3-16 (a), the large impedance brought by the circulating current control in Figure 3-16 (b) helps to reduce the mismatch caused by dead time, harmonics extraction, cable impedance,

parameters tolerance of passive components, etc. Furthermore, high R_a also effectively mitigates i_{dc_2nd} and reduces the impact of SLG fault on arm currents and capacitor voltage ripples.

3.5 Summary

This chapter presents a steady-state model of MMC to predict the system performance under unbalanced conditions. The model is derived and experimentally verified, considering the impact of negative sequence current control, circulating current control, and different load conditions. The key points in this chapter can be summarized as follows:

1) A steady-state model that describes the relationship between current and voltage quantities of MMC under unbalanced conditions is proposed. A detailed comparison of the proposed model with/without negative sequence current control reveals that when the widely used dual current control is applied, the positive, negative and zero sequence circulating current are generated by more voltage sources and are no longer decoupled.

2) According to the circular relationship found from the steady-state model, the magnitudes and initial phase angles of different circulating current components can be easily predicted. Moreover, the fundamental and low frequency harmonic components of the capacitor charging currents, capacitor voltages, arm currents, and output phase voltages can be analytically expressed.

3) The equivalent dc impedance of MMC is first derived for circulating current calculation in a point to point MMC-HVDC system. Based on the derivation, a MMC inverter can be represented as a series connected R-L-C branch, and the equivalent resistance and capacitance depend on circulating current control parameters.

4) The derived steady-state models are verified in a three phase scaled-down MMC rectifier and inverter prototype under an emulated SLG fault. Moreover, verification of the equivalent dc impedance is achieved by injecting a second order ripple into the dc link of a MMC inverter. The comparison between experimental and calculation results under three kinds of test conditions demonstrate the validity of the analysis and derivation.

4 Integrated Fault-tolerant Control Scheme of MMC under SLG Fault Conditions

This chapter presents the analysis and control of a multilevel modular converter (MMC) based HVDC transmission system under three possible single-line-to-ground (SLG) fault conditions, with special focus on the investigation of their different fault characteristics. Considering positive, negative and zero sequence components in both arm voltages and currents, the generalized instantaneous power of a phase unit is derived theoretically according to the equivalent circuit model of the MMC under unbalanced conditions.

Based on this model, a novel double line frequency dc voltage ripple suppression control is proposed. This controller, together with the negative and zero sequence current control, could enhance the overall fault-tolerant capability of the HVDC system without additional costs. To further improve the fault-tolerant capability, operation performance of the HVDC system with and without single phase switching (SPS) is discussed and compared in detail. Simulation results from a three-phase MMC-HVDC system generated with Matlab/Simulink and experimental results from a scaled down MMC prototype are provided to support the theoretical analysis and proposed control schemes.

4.1 Control Scheme under SLG Fault

Assumes MMC_1 in Figure 3-1 controls the dc voltage and reactive power, while MMC_2 is assigned to regulate the active and reactive power generation. Figure 4-1 shows the overall control diagram under unbalanced conditions. The references for the outer loop are dc voltage and reactive power in the rectifier station (MMC_1), while those for the inverter station (MMC_2) are active and reactive power. The sum of the references generated by positive, negative, and zero sequence current regulation forms the phase voltage command e_{j_ref}. The output of dc voltage ripple suppression controller, i.e., $u^0_{diff_ref}$ in u_{diff_ref}, is subtracted from both the upper and lower arms' voltage references, which is similar to the implementation of circulating current control. As indicated from (1), the dc voltage ripple suppression controller will not

affect the normal phase voltage generation (e_j). Hence, both the unbalanced current and dc voltage ripple can be eliminated at the same time, enabling desirable performance of MMC-HVDC under SLG faults.

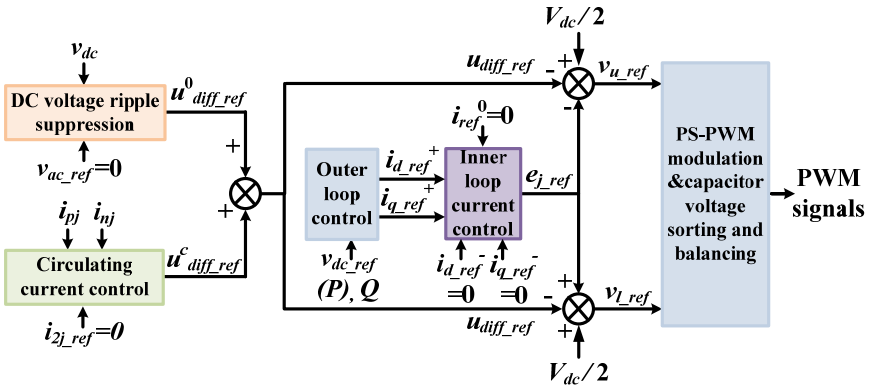


Figure 4-1. Control scheme of MMC under unbalanced condition.

With properly designed control parameters, it is unnecessary to deactivate the negative and/or zero sequence current regulation, as well as the double line frequency dc voltage ripple suppression control immediately when the fault is cleared, which reduces the requirement for fast fault detection. N+1 level phase shift PWM (PS-PWM) modulation is adopted in this work for its high equivalent switching frequency and relatively simple implementation. To balance capacitor voltages among SMs and enable small arm inductances, the capacitor voltage balancing method and circulating current suppression techniques in [129] are employed. Operation of these controllers should be maintained under unbalanced conditions to prevent arm inductors and sub-module capacitors from possible large current and voltage ripples.

The detailed positive sequence current controller is redrawn in Figure 4-2. The anti-windup PI controllers are employed to keep the integrator from further saturation if the modulation index limit is exceeded during a transient and/or fault, thus enabling the system to return to the controllable region in a short time. To achieve accurate synchronization with the grid voltage, the positive sequence voltage is extracted with methods proposed in [130] and used as the input of a phase locked loop (PLL). In addition, the converter-side phase current in *dq* coordinates (I_d and I_q) are directly used for power and/or voltage control. Compared to the single positive sequence current control used in dual current control, the

negative sequence voltage reference is generated instantaneously when a SLG fault occurs, which is beneficial for system stability and fast compensation of grid voltage variation by avoiding any delay introduced by the current extractor, fault detection, or controllers activation.

Figure 4-3 shows the control diagram of the negative sequence current compensation. The same method in [130] is used for negative sequence current extraction. By setting the reference i_{dnref}^{*} and i_{qnref}^{*} to be zero, negative sequence current can be eliminated using a PI controller in *dq* coordinates.

For zero sequence current elimination under certain circumstances, a quasi-PR controller is employed, as shown in Figure 4-4. Unlike a PI controller, zero steady state error can be obtained in time domain by using a PR controller. Moreover, compared to PR controllers, a quasi-PR controller provides finite gain at the resonant frequency but lower sensitivity towards slight frequency variation [131].

A quasi-PR based feedback control is proposed in this work to mitigate the double line frequency dc voltage ripple. Figure 4-5 shows the control diagram of the dc ripple suppression, where k_{conv} represents the gain of converters; L is the effective AC side inductance (L_{AC}+L_0/2); R stands for the equivalent inductor series resistance; R_{eq} denotes the equivalent dc impedance; the second-order dc voltage ripple reference v_{2f_ref} is set to zero. A second order band pass filter (HPF) is employed to eliminate any dc components. In a practical implementation, it can be realized by v_{dc} subtracts its low frequency components for easier software or hardware implementation (represented as the dashed circles in Figure 4-5). Since only dc voltage is detected, no extra cost is introduced for the control implementation.

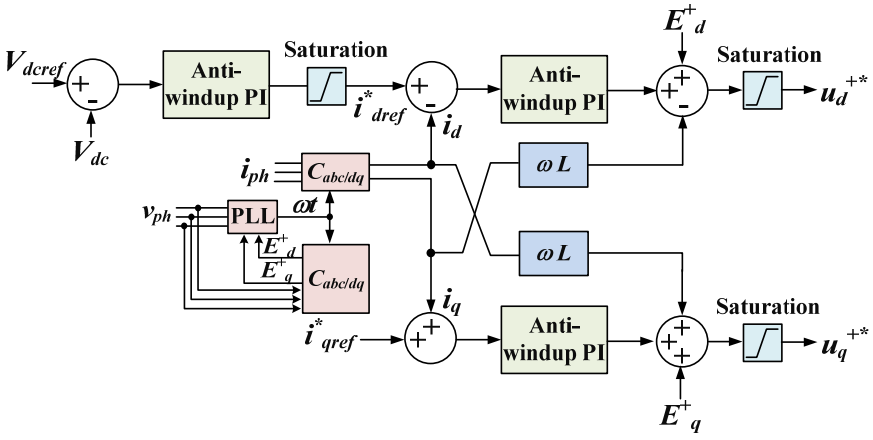
The transfer functions of the PR controller and HPF are given as

$$H_{HPF}(s)=\frac{k_0 s^2}{s^2+\xi\omega_n s+\omega_n^2} \qquad H_{PR}(s)=k_p+\frac{2k_r\omega_c s}{s^2+2\omega_c s+\omega_0^2} \tag{4 - 1}$$

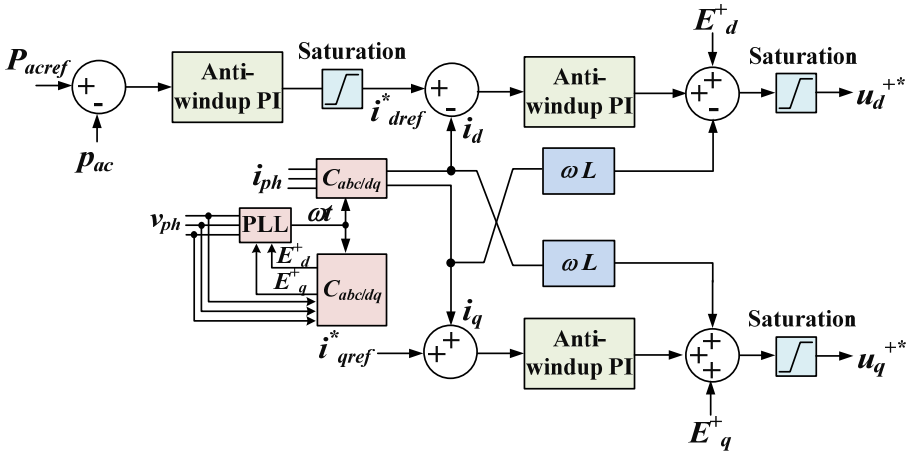
where k_0 is a gain constant; ξ is a damping ratio; ω_n is the natural frequency of the HPF; k_p, k_r represent controller gains; ω_c is the cut-off frequency; and ω_0 is the angular frequency of the control target.

Based on Figure 4-5 and (4 - 1), the open loop transfer function from v_{dc} to v_{2f_ref} can be derived as:

$$G(s)=\frac{3V_{rms}R_{eq}k_0k_{conv}s^2[k_ps^2+2\omega_c(k_p+k_r)s+k_p\omega_0^2]}{\sqrt{2}V_{dc}(sC_dR_{eq}+1)(sL+R)(s^2+2\omega_c s+\omega_0^2)(s^2+\xi\omega_n s+\omega_n^2)} \quad . \tag{4 - 2}$$



(a) DC voltage control



(a) Active power control

Figure 4-2. Diagram of positive sequence current control.

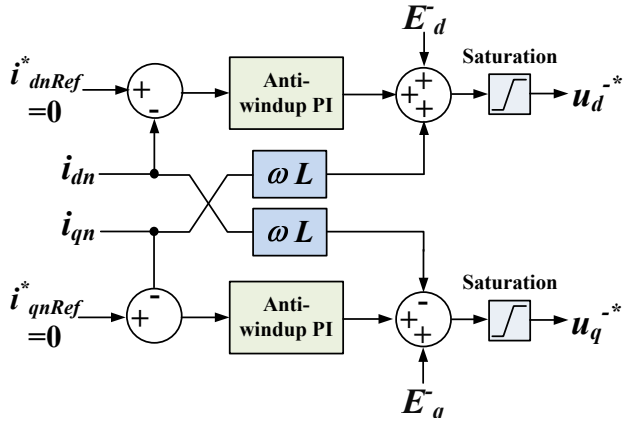


Figure 4-3. Diagram of negative sequence current suppression.

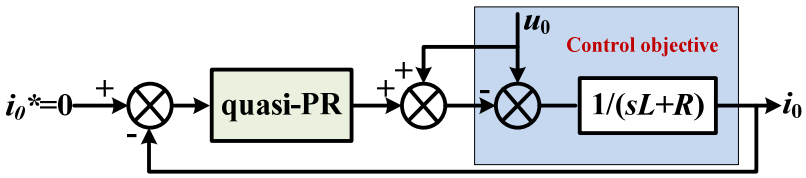


Figure 4-4. Control diagram of zero sequence current.

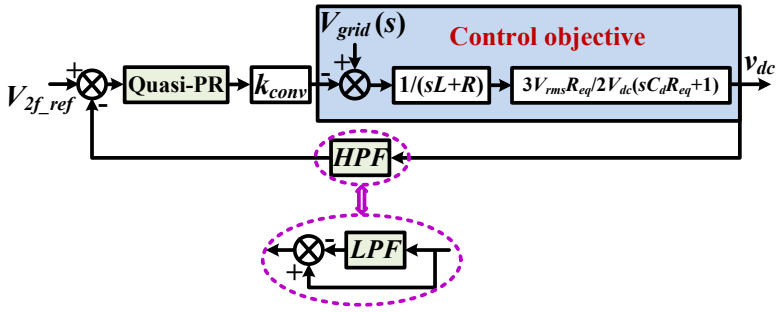


Figure 4-5. Control diagram for dc voltage ripple suppression.

According to the system bode plot, a larger k_r shifts the magnitude response upwards, but the bandwidth cannot be changed much. k_p basically determines the steady state and transient performance in terms of bandwidth, phase and gain margin, and its design is similar to that of a PI controller. Larger ω_c helps to reduce the sensitivity to slight frequency variation in utility grids, and in practice, ω_c is selected from 5–15 rad/s to provide a good compromise between the signal selectivity and quick dynamic response. As for the HPF design, k_0 can be adjusted to achieve proper control loop gain and bandwidth, while ω_n should be designed carefully as a trade-off between desirable filtering performance and sufficient control loop bandwidth.

Finally, the main control parameters are selected as: k_p = 1.5, k_r = 50, ω_c = 10 rad/s, ω_0 = 2π×120 = 753.6 rad/s, ξ = 1.2, k_0 = 0.2, and ω_n = 2π×30 = 188 rad/s. The corresponding open loop bode plot is illustrated in Figure 4-6, with the magnitude as high as 36.5 dB at the second harmonic frequency. Moreover, the cut-off frequency is set to be around one tenth (723 Hz) of the equivalent switching frequency 7.2 kHz (4×1.8 kHz carrier frequency), enabling sufficient mitigation of switching ripple.

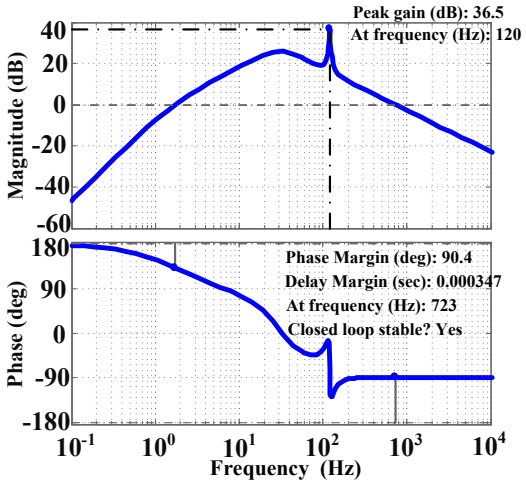


Figure 4-6. Open-loop bode plot of dc voltage ripple control.

4.2 Case Study

A. System Parameters

A three phase MMC-HVDC transmission system with the controllers designed in Section 3.1 is established in Matlab/Simulink, and the system parameters are summarized in Table 4-1. As the short circuit current in the grid side mainly serves as an indicator to trip the AC breakers, and it has little impact on the converter side negative sequence current control design, a strong grid with three phase short circuit level of 1000 MVA is adopted in this paper.

Considering that control performance under unbalanced conditions is not affected by the number of sub-modules N, four cells per arm (N = 4) is used in this paper to achieve acceptable simulation time. Moreover, the current references of all converters are limited to $I_{ref_max} = 1.36I_{rated}$ (157 (rms), 222 A (peak), $I_{dmax} = 1.1I_{rated}$, $I_{qmax} = 0.8I_{rated}$, where I_{rated} is the converter side rated phase current in MMC_2) to protect devices from damage.

B. Studied Fault Cases

In practice, a SLG fault may occur in different locations due to broken wires, insulation damage, or poor connection. In this work, the fault conditions are categorized into the following three cases.

Table 4-1. Main circuit parameters of MMC-HVDC in simulation model.

Parameters	Values	Notes
DC Link voltage U_{dc}	5 kV	±2.5 kV
AC system voltage u_{s1}, u_{s2},	10 kV	L-L, rms, Three phase short circuit level =1000 MVA, X/R=8
Voltage frequency	60 Hz	
Transformer ratio	10 kV/2.5 kV	Yg/Δ
No. of sub-modules in each arm N	4	
Sub-module capacitance	2000 μF	
AC side inductance L_{AC1}, L_{AC2}	2.388 mH	0.144 pu
Arm inductance L_0	2.82 mH	0.17 pu
Carrier frequency	1.8 kHz	
Rectifier side reactive power reference	0 Var	Unity power factor
Inverter side active power reference	0.5 MW	
Inverter side reactive power reference	0.25 MVar	
DC cable length	50 km	
Resistance per unit length	13.9 mΩ/km	PI type cable
Inductance per unit length	159 uH/km	
Capacitance per unit length	0.231 uF/km	

1) Case 1: SLG Fault Occurs in the Primary Side of the Y/Δ Transformer

Figure 4-7(a) shows the system schematic with SLG fault occurring in phase C. The solid line fault represents a SLG fault in the rectifier side, while the dashed line stands for a SLG fault in the inverter side. With delta connection in the secondary side, no zero sequence current will flow into the converter side. During a SLG fault period, the negative sequence voltage in the primary side will be introduced to the secondary side of the interfacing Y/Δ transformer, and results in the converter side negative sequence current if there is no negative sequence control for the converters.

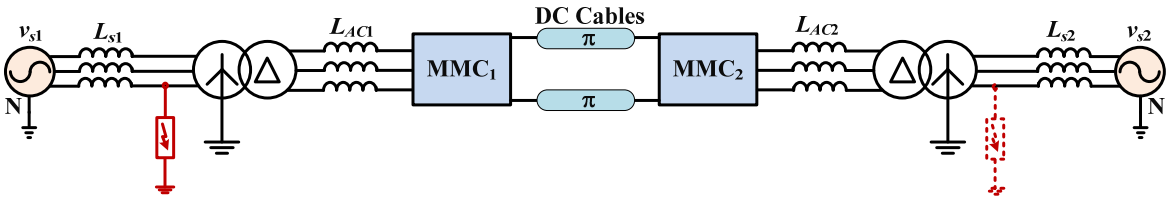
2) Case 2: SLG Fault Occurs in the Secondary Side of the Y/Δ Transformer

Figure 4-7(b) illustrates the system schematic in case 2, with the SLG fault happening in phase C. Similarly, with delta connected winding in the converter side, the grid utility can be free from the zero sequence current caused by faults.

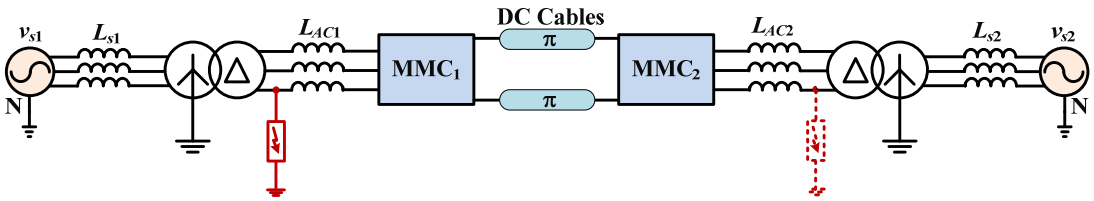
3) Case 3: SLG Fault Occurs in a Transformerless System

At present, the isolation transformers are regarded as a key component in a HVDC converter unit, which raises the AC voltage in an economic way, and limits short circuit currents during fault conditions. On the other hand, the MMC topology can synthesize high voltage levels by increasing the number of submodules, and thus no bulky and costly transformer is necessary with properly selected voltage rating. Moreover, the short circuit currents can be effectively suppressed by AC reactors as well as arm inductors, and/or other active strategies.

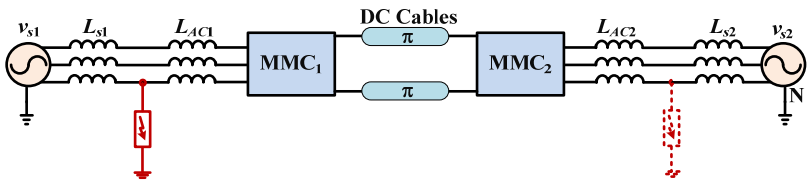
Also, considering such potential benefits as providing an economic and promising solution for medium power HVDC transmission, micro-grid and motor drive fields, the transformerless scheme could be worthy of consideration, though it may take a long time to put the transformerless HVDC system into practical applications.



(a) SLG fault occurring in the primary side of Y/Δ transformer (case 1)



(b) SLG fault occurring in the secondary side of Y/Δ transformer (case 2)



(c) SLG fault occurring in a transformerless application (case 3)

Figure 4-7. Different SLG fault locations.

As a thorough investigation of fault tolerance capability of MMC with different system configurations, and to make the theoretical analysis more comprehensive, the transformerless system is presented in this paper as case 3, though it is rarely used in industry applications.

The system schematic of a transformerless-HVDC with a SLG fault occurring in phase C is given in Figure 4-7(c) by removing both Y/Δ transformers in Figure 4-7(a). Different from the above two cases, the zero sequence current will not be blocked any more, thus flowing into the AC grid at both converter stations and forming ground currents.

4.2.1 Fault Tolerant Operation with Designed Controllers in Case 1

A SLG fault occurs in phase C at 0.7 s, and the negative and/or zero sequence current control together with dc voltage ripple suppression is activated at 0.8 s. Without a ground loop between the secondary sides of the Y/Δ transformer in two converter stations, the SVM scheme is adopted for high dc voltage utilization.

1) SLG fault occurs in the rectifier side

As a clear description, the circuit diagram is redrawn in Figure 4-8 with crucial voltages and currents labeled. The corresponding simulation waveforms at MMC_1 and MMC_2 are illustrated in Figure 4-9 and Figure 4-10, respectively.

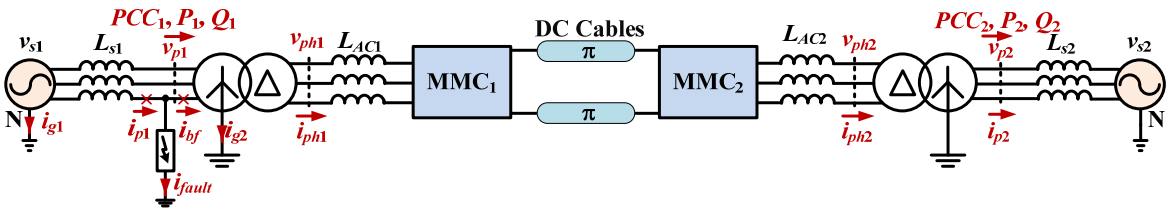


Figure 4-8. Rectifier side SLG fault in case 1.

Because of the preset current limitation, power balance between the generation of rectifier and absorption of inverter is broken, and consequently, the dc voltage drops gradually during the SLG fault. This voltage drop, however, will not stop until another power balance is achieved because of over-

modulation in the inverter station (dc voltage can be maintained if the maximum phase current is limited to $1.5I_{rated}$ or larger).

A double line frequency ripple with magnitude of 24.31 V is observed in the dc voltage (Figure 4-9), resulting in dc capacitor overstress as well as possible power distortion in the inverter side. When the dc voltage ripple suppression control is activated at 0.8 s, the double line frequency dc voltage ripple is reduced to 2.39 V in two fundamental cycles, in spite of a slightly larger high frequency ripple caused by additional switching actions. In addition, low-frequency harmonics within the control bandwidth are also partially mitigated, contributing to high output power quality.

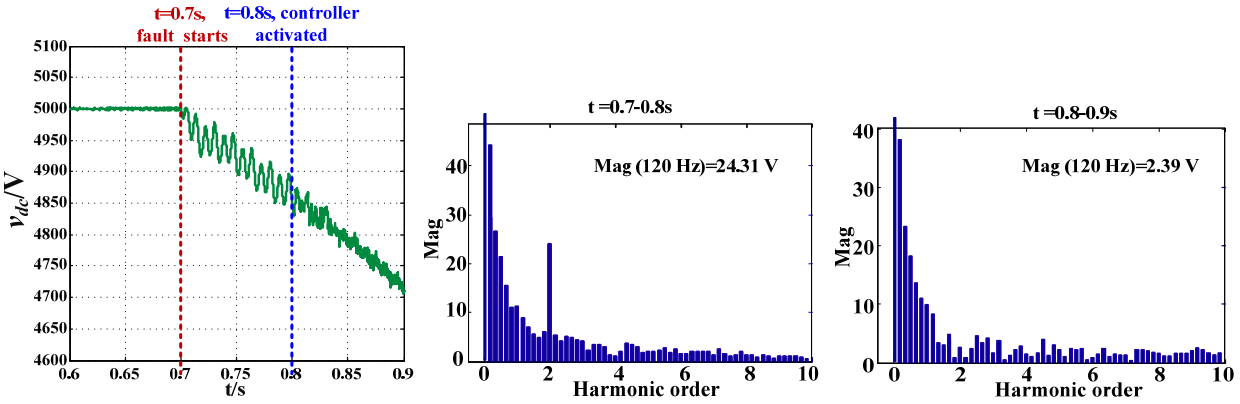


Figure 4-9. DC voltage and its spectrum with an SLG fault in case 1 (MMC_1 side).

As shown in Figure 4-10, AC grid u_{s1} and MMC_1 keep feeding the fault, and produce significant ground currents i_{g1} (Figure 4-10(a)) and i_{g2} (Figure 4-10(b)), the magnitude of which is related to the phase voltage v_{p1} and ground loop impedance, e.g., grid impedance L_s, AC reactor L_{AC1}, zero sequence impedance of the transformer and grounding impedance. The ground current, in the form of zero sequence current, flows through i_{p1} and i_{bf} and forces three phase current i_{bf} to be overlapped (Figure 4-10(e)). Furthermore, C phase current in i_{p1} becomes much larger than the other two healthy phases (Figure 4-10(c)). To meet the power demands from the inverter, the converter side phase current i_{ph1} in the rectifier increases from 181 A to its maximum allowed value, 222 A (Figure 4-10(f)).

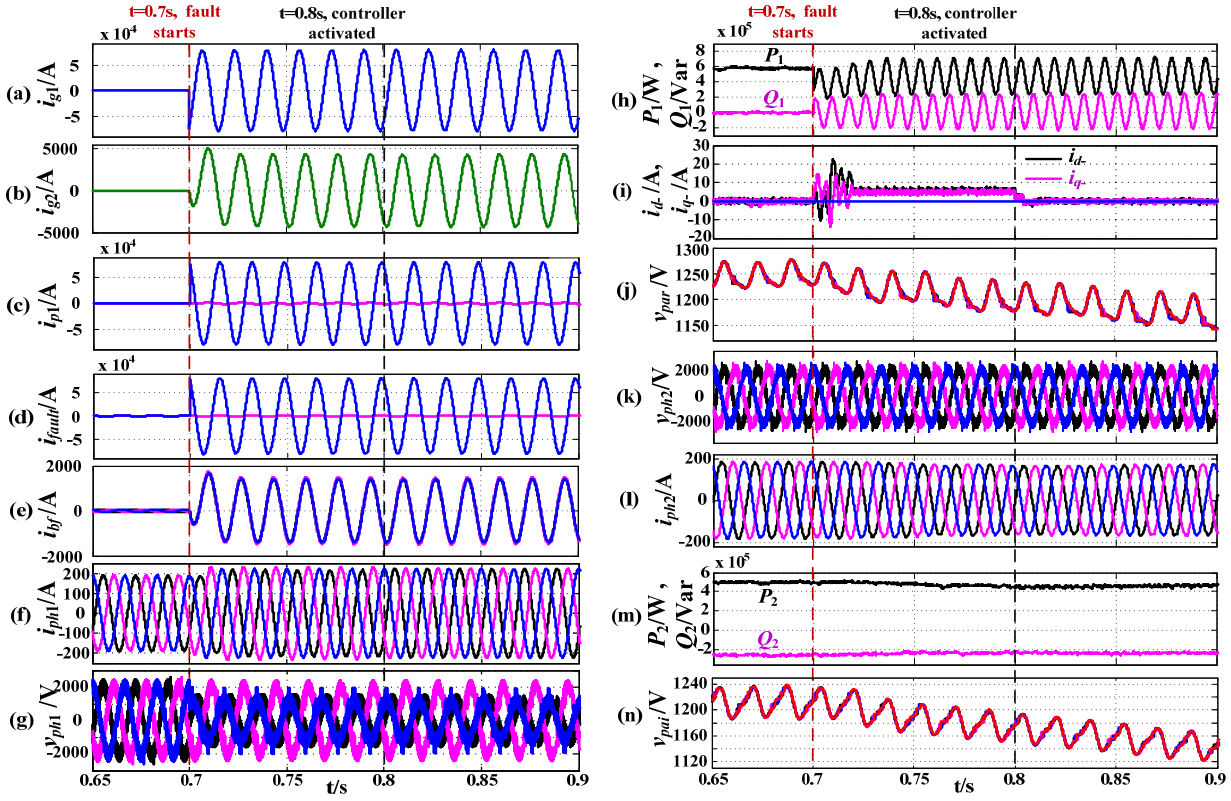


Figure 4-10. Simulation waveforms of the studied system under an SLG fault in case 1 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) transformer primary side ground current, (c) phase currents before the fault point, (d) fault current, (e) phase currents after the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm.

As mentioned above, negative sequence voltage is created by the converter when the fault occurs (Figure 4-10(g)), which partially reduces the negative sequence current. When the designed control starts at 0.8 s, the negative sequence voltage generated by converter is regulated to be exactly the same as that in the grid side. Consequently, the dq axis negative sequence currents are eliminated in about 0.1 s (Figure 4-10(i)). Figure 4-10(h) illustrates the active and reactive power in the rectifier side, represented as P_1 and Q_1, respectively. Besides large double line frequency ripple, the active power absorbed by MMC_1 is 1/3 lower because of the voltage drop at PCC_1. As shown in Figure 4-10(j), although SMs' capacitor voltages are well balanced, their mean value gradually decreases from 1250 V due to the dc voltage drop. In addition, the capacitor voltage ripple increases by 10 V because of larger charging and discharging phase currents.

In the inverter station, phase voltage v_{ph2} is not affected, while the magnitude of phase current i_{ph2} decreases from 163.3 A to 150.2 A because of the reduced power generation in the rectifier side (Figure 4-10 (k) and (l)). For the same reason, the active power output of MMC_2 drops from 0.5 MW to around 0.46 MW, and the reactive power is reduced from 0.25 MVar to around 0.23 MVar, as shown in Figure 4-10(m). With 150 V voltage drop on the dc cables, the average value of SMs' capacitor voltages in MMC_2 becomes 1212.5 V in the steady state (Figure 4-10(n)). Like Figure 4-10(j), although the capacitor voltages keep decreasing, they are well balanced with smaller ripple.

The feasibility of single pole switching (SPS) is also investigated for continuous load power supply and system protection under permanent SLG fault conditions. The faulted phase (phase C) instead of all three phases is cut from both sides, as illustrated by the red crossings in Figure 4-8. Limited by the negative impact of the unbalanced phase current, a system with SPS can only survive a temporary SLG fault. Otherwise, all three phases will be tripped after a certain time (normally 0.5 s).

Figure 4-11 and Figure 4-12 give the dc voltage and AC waveforms in MMC_1 and MMC_2 stations, respectively, with SPS started at t = 0.73 s. A reasonable assumption is made here that it takes 30 ms to open a single pole breaker. After a transient process, dc voltage finally pulls out from saturation and recovers to its rated value at t = 0.85 s, and the double line frequency ripple decreases from 8.81 V to 0.23

V after the designed controllers are activated (Figure 4-11). Compared with the case without SPS, the dc voltage ripple is much smaller with SPS thanks to the lower positive and negative sequence current.

However, as shown in Figure 4-12(a) and (b), there is still ground current within the loop between the AC grid u_{s1} and transformer grounds. This ground current would necessarily create a zero sequence current in the two healthy phases (Figure 4-12(c) and (e)), but its magnitude is reduced to 140 A and will not cause any damage in a short time period. A 1 MΩ grounding snubber resistance is chosen to get the i_{fault} smaller than 20 mA (Figure 4-12(d)).

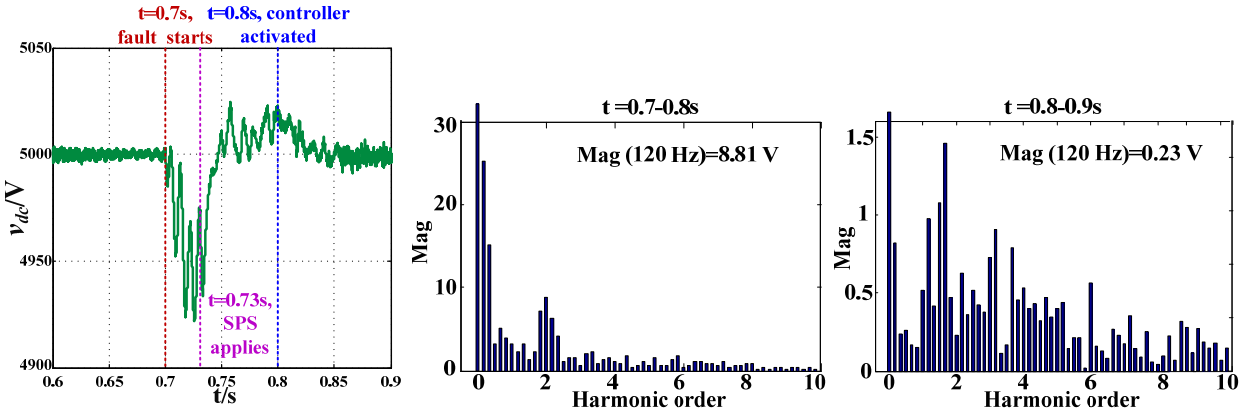


Figure 4-11. DC voltage with single pole switching in case 1 (MMC_1 side).

Figure 4-12(f) and (g) give the delta side phase current and voltage, respectively. Without the faulted phase, both the current and voltage become balanced, and the amplitude of i_{ph1} goes back to its rated value after the dc voltage recovers. The active and reactive power in the rectifier side is given in Figure 4-12(h). Disconnection of SLG fault not only eliminates the large double line frequency power ripples, but also enables rated power generation at PCC_1 after t = 0.85 s. In addition, in spite of a temporary overshoot and oscillation, SPS reduces the negative sequence current, which is further suppressed by negative sequence current control (Figure 4-12(i)). As illustrated by Figure 4-12(j) to (n), due to the fault isolation, capacitor voltages of SMs in the MMC_1 and MMC_2 stations, together with the inverter side phase current, are regulated to their rated values after a transient process.

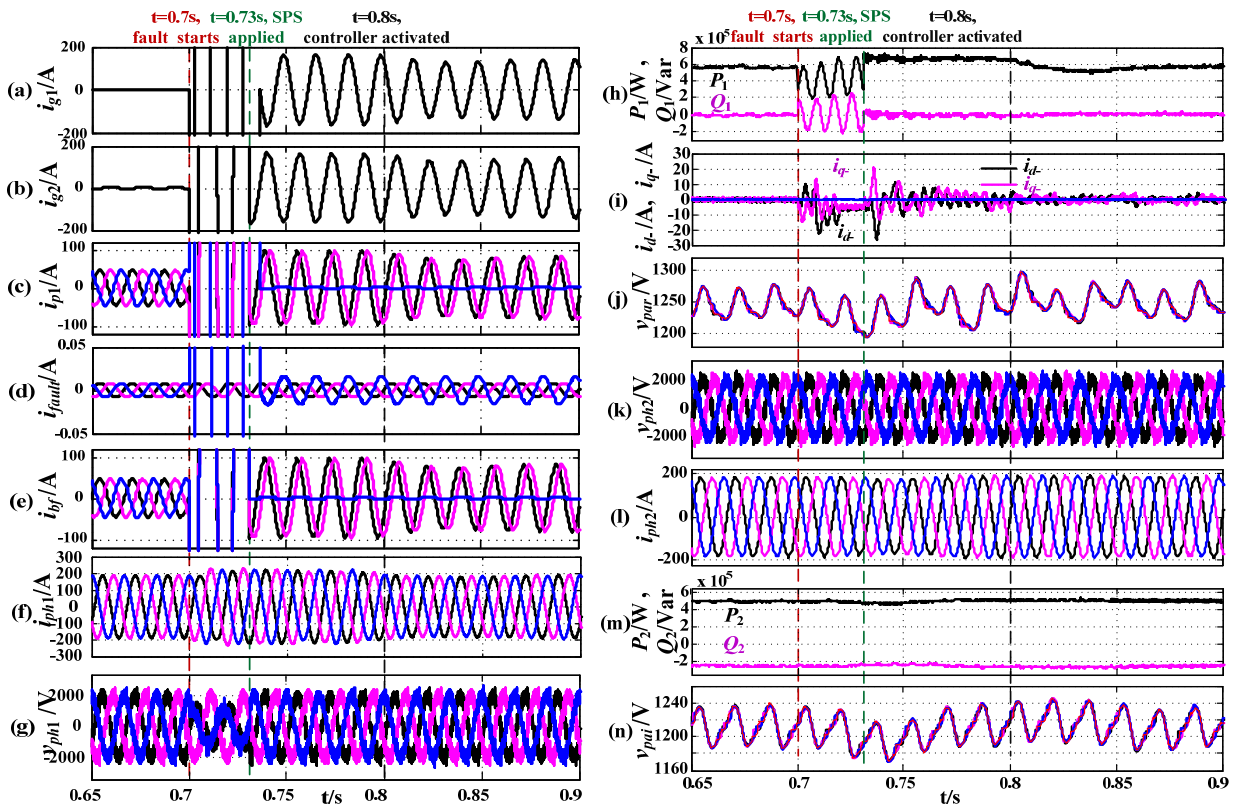


Figure 4-12. Simulation waveforms of the studied system under an SLG fault with single pole switching in case 1 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) transformer primary side ground current, (c) phase currents before the fault point, (d) fault current, (e) phase currents after the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm.

Furthermore, active and reactive power generated by MMC_2 tracks its reference in less than two fundamental cycles when the fault is cleared. The difference between the active power generated by the rectifier and absorbed by the inverter accounts for the power losses of the whole system, which is about 81 kW (13.94 %) with the given simulation parameters.

2) SLG fault occurs in the inverter side

Figure 4-13 shows the circuit diagram with a SLG fault in the grid side of MMC_2. Figure 4-14 shows the dc voltages and their spectrum in the rectifier and inverter stations. As can be observed, the power loss in the inverter side leads to an abrupt dc voltage increase when the SLG fault occurs, but thanks to the unaffected rectifier control, the dc voltage goes back to its rated value after 0.1 s. Furthermore, the double line ripple in the inverter side dc side voltage is reduced from 24.93 V to 2.05 V when the dc voltage suppression control is activated. In addition, the second order ripple in the rectifier side dc voltage drops from 8.5 V to 0.62 V. It is interesting that the dc voltage ripple is attenuated greatly by the dc cables, and if controllers with high bandwidth are adopted, the output voltage distortion in the healthy converter station can be quite small, thus the active power ripple elimination control may not be necessary in some applications.

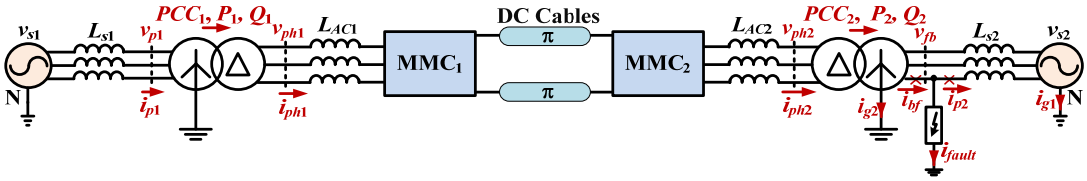
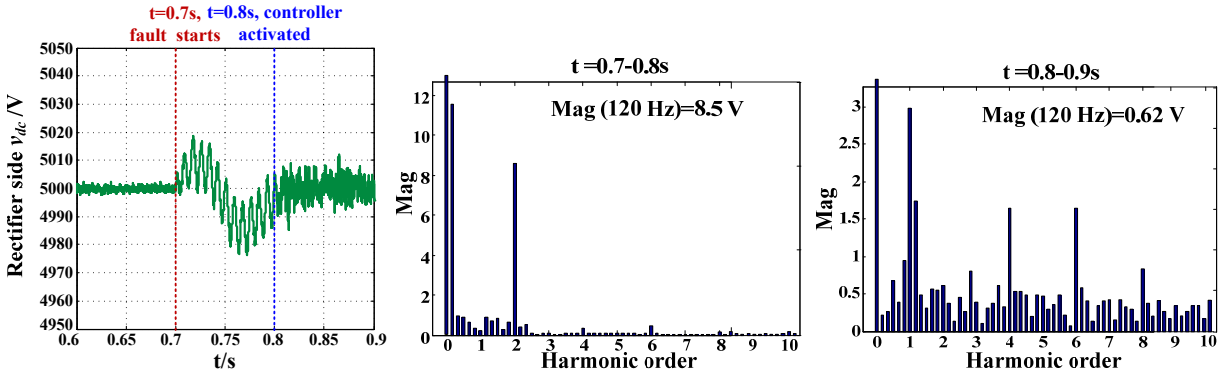


Figure 4-13. Inverter side SLG fault in case 1(MMC_2 side).

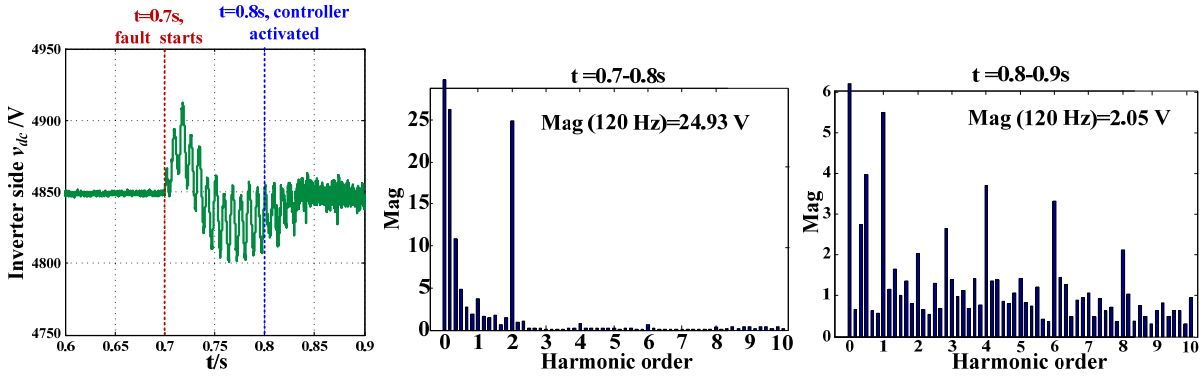
Figure 4-15 illustrates the corresponding AC side waveforms. With the same grounding connection, MMC_2 suffers the same current distribution (i_{g1}, i_{g2}, i_{p2} and i_{bf}) in the primary side as that in Figure 4-10. To track the power references, the magnitude of delta side current in MMC_2 (i_{ph2}) increases to its maximum value of 222 A. Since the phase current is still not high enough to compensate the power loss caused by the SLG fault, both active and reactive power generation (P_2 and Q_2) at PCC_2 decrease.

Meanwhile, power absorption (P_1 and Q_1) from the AC grid v_{s1} is reduced until a new power balance is achieved to maintain the dc voltage, thus the rectifier side phase current i_{ph1} decreases proportionally.

As shown in Figure 4-15(i), the negative sequence component in i_{ph2} is effectively minimized by the negative sequence current controller. With a stable dc voltage, SMs' capacitor voltages in both MMC_1 and MMC_2 are well balanced and regulated around their rated values. Moreover, the capacitor voltage ripple in MMC_2 increases because of higher i_{ph2}, while that in MMC_1 decreases because of the lower i_{ph1}. To protect the system from large fault current, the SLG fault should be isolated by opening the faulted phase from both sides, as represented by red crossings in Figure 4-13. Without the faulted phase, all currents and voltages, except those in the primary side of Y/Δ transformer in MMC_2, present the same performance as normal conditions.



(a) MMC_1 side dc voltage and its spectrum



(b) $MMC_{2\ side}$ dc voltage and its spectrum

Figure 4-14. DC voltage and its spectrum with an SLG fault in case 1 (MMC_2 side).

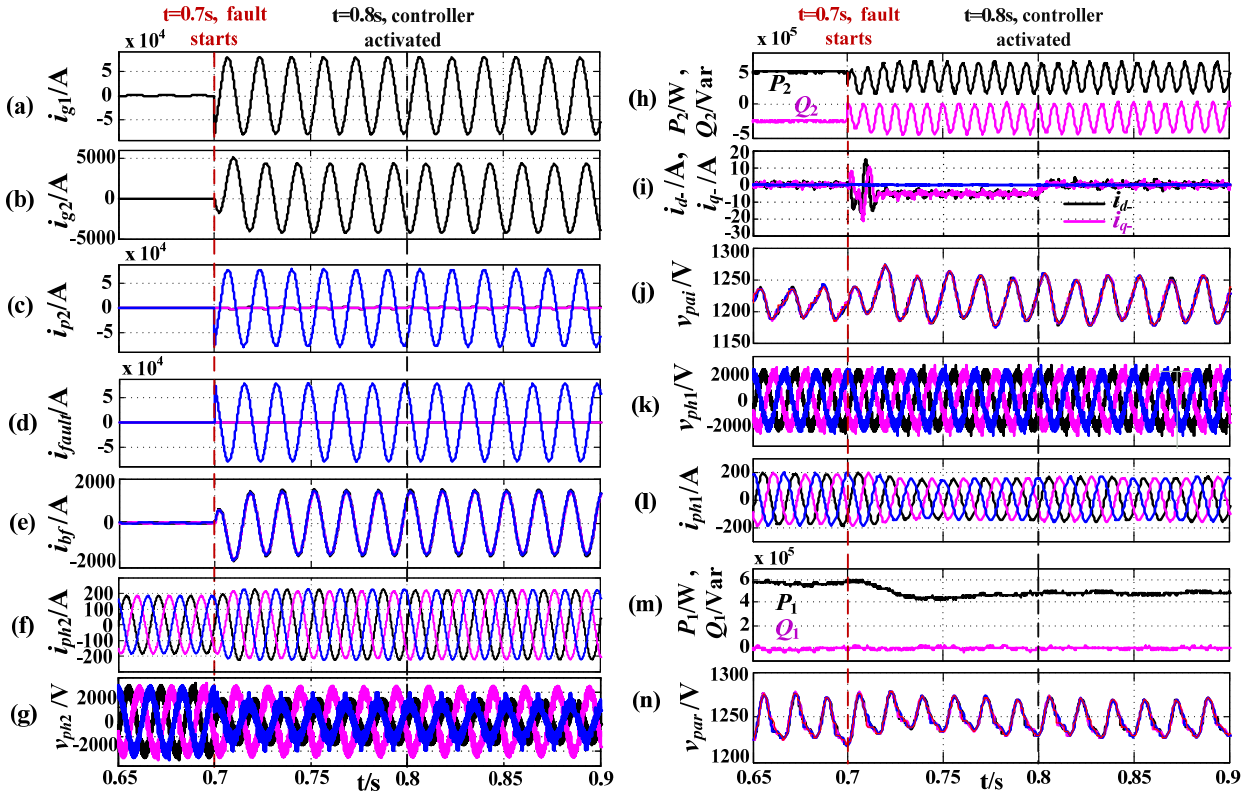


Figure 4-15. Simulation waveforms of the studied system under an SLG fault in case 1 (MMC_2 side). **MMC_2 side:** (a) AC grid ground current, (b) transformer primary side ground current, (c) phase currents after the fault point, (d) fault current, (e) phase currents before the fault point, (f) phase current in the delta side of the Y/Δ transformer, (g) phase voltage in the delta side of the Y/Δ transformer, (h) active and reactive power, (i) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_1 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm.

4.2.2 Fault Tolerant Operation with Designed Controllers in Case 2

The circuit diagram with SLG fault in the secondary side of Y/Δ transformer at MMC_1 station is given in Figure 4-16. SPWM instead of SVM scheme is employed in this simulation because of the neutral point displacement during the fault.

With normal primary side voltage v_{p1}, the magnitude of phase voltage in the converter side v_{ph1} is clamped to its line-to-line voltage, which enables constant v_d and v_q under the dq coordinates. Since the SLG fault in this case mainly introduces a zero sequence component in the converter side phase current i_{ph1}, the normal dc voltage control is unaffected by the SLG fault, as demonstrated in Figure 4-17. Because of the small negative sequence current to be compensated, a double line frequency ripple with magnitude of only 0.41 V is observed in the dc voltage. When the dc voltage ripple suppression control is activated at 0.8 s, this ripple is further reduced to 0.09 V in less than two fundamental cycles.

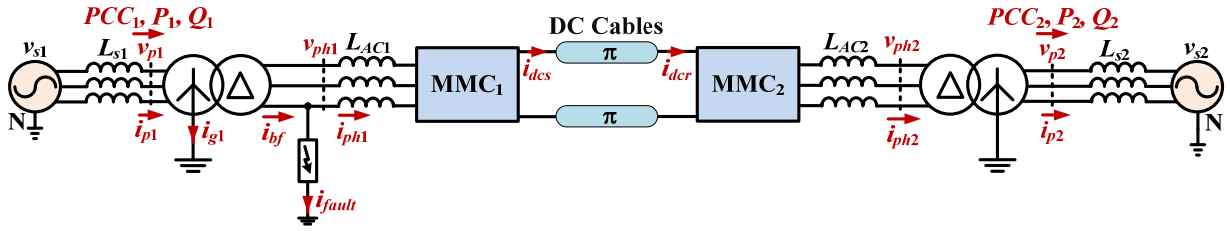


Figure 4-16. Rectifier side SLG fault in case 2.

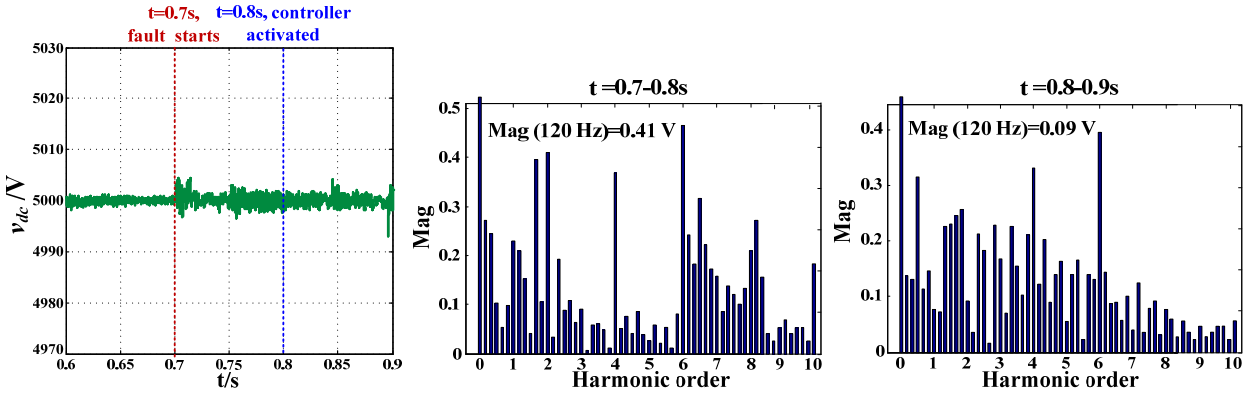


Figure 4-17. DC voltage and its spectrum with SLG fault in case 2 (MMC_1 side).

As shown in Figure 4-18(a)-(c), without a zero sequence current path, no ground current flows into the primary side ($i_{g1} = 0$) and only positive as well as negative sequence currents appear in i_{bf} and i_p. The waveforms of dc currents in the sending end i_{dcs} (rectifier side) and receiving end i_{dcr} (inverter side) are presented in Figure 4-18(f). A detailed comparison among these two currents and ground current i_{fault} reveals that i_{fault} is forced to flow into the ground through the capacitance of the dc cables. Moreover, the oscillation in i_{fault}, caused by resonance among inductors and distributed capacitors, is gradually damped because of parasitic resistances of AC reactors and dc cables (Figure 4-18(d)).

Figure 4-18(g) and (h) give the converter and grid side phase voltage in the rectifier station, respectively. As mentioned above, during a SLG fault, the grid side phase voltage v_{p1} keeps balanced, while the magnitude of the converter side phase voltage v_{ph1} in the other two healthy phases equals to the value of the line-to-line voltage in this case. After the oscillation in i_{fault} damps down and the controllers start to operate at 0.8 s, the positive sequence component in the converter side phase current i_{ph1} stays at 181 A, and the negative and zero sequence components are reduced to around 0.5 A and 6 A, respectively.

In order to eliminate the zero sequence current, a zero sequence voltage with its magnitude equal to positive sequence one needs to be generated by the converters. However, this will affect the positive sequence power regulation and lead to potential system instability. To deal with this issue, the zero sequence voltage feedforward control is not applied and the output of zero sequence current control is limited properly in this case. Although the average active power in rectifier side maintains, its instantaneous value still has some double line frequency ripple caused by zero sequence voltage and current, but the magnitude of this ripple is low enough to be neglected after 0.85 s (Figure 4-18(j)). On the other hand, as shown in Figure 4-18(k), the negative sequence current is well suppressed by the corresponding control activated at t = 0.8 s. Different from the previous cases, the SLG fault has no obvious impact on capacitor voltages in both rectifier and inverter sides due to the stable dc voltage and phase currents (Figure 4-18 (k) and (p)). However, the positive and negative dc bus to ground voltage becomes sinusoidal (Figure 4-18 (l)). That is why the converter side phase voltage in the inverter station has the same shape as that in the rectifier station (Figure 4-18 (m)).

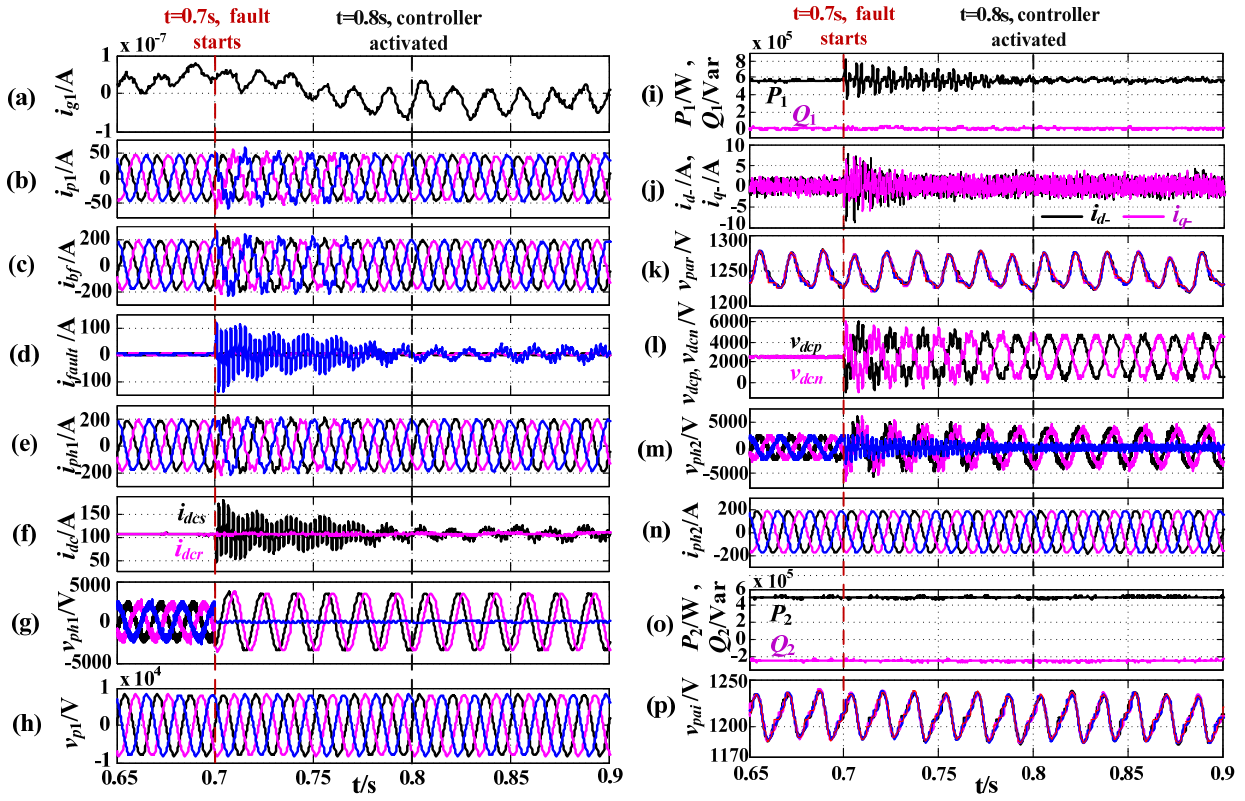


Figure 4-18. Simulation waveforms of the studied system under an SLG fault in case 2 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) phase current in the Y side of the Y/Δ transformer, (c) phase currents before the fault point, (d) fault current, (e) phase current in the delta side of the Y/Δ transformer, (f) dc bus currents in the sending and receiving end, (g) phase voltage in the delta side of the Y/Δ transformer, (h) phase voltage in the Y side of the Y/Δ transformer, (i) active and reactive power, (j) negative sequence current components, (k) capacitor voltages of SMs in phase A upper arm; and (l) dc buses to ground voltage, **MMC_2 side:** (k) phase voltage in the delta side of the Y/Δ transformer, (l) phase current in the delta side of the Y/Δ transformer, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm.

In spite of the phase voltage variation caused by floating ground potential, the line to line voltage is the same as that under normal conditions, which enables rated active and reactive power in the inverter side (P_2 and Q_2) as long as the phase current i_{ph2} keeps balanced and well regulated.

In some applications, the leakage inductance of the transformer is employed as the interfacing reactors (L_{AC1} and L_{AC2}) [132] [133]. In such a system, a single phase to ground fault at converter side will connect the faulted phase to the positive dc bus in certain patterns through grounding loops. Different from the dc fault, since the positive and negative dc buses are connected to ground through stray capacitances, these capacitances will be incorporated in the fault loop in addition to the on-state resistance of the switches as well as arm reactor resistance and inductance. The stray capacitance of the dc cable, normally hundreds of nF/km, is much smaller than central capacitance in voltage source converters. Thus, the inrush current caused by its stored energy discharging during the transient fault period is limited. Moreover, the stray capacitance dominates the short circuit loop impedance, which could contribute to a small short circuit current in the steady state.

The above analysis, however, is valid only when dc cable capacitance is small and its stored energy is low. If a long dc cable is used, and/or additional dc capacitors are adopted for dc side grounding, a significant fault current may be created by the secondary SLG fault, making the continuous operation of MMC impossible. Furthermore, in ultra-high dc voltage applications, even though the stray capacitance is small, its stored energy may also be high enough to produce a destructive fault current and force the system to completely stop during the fault.

Since the fault current is relatively small and performance degradation is also low, no SPS is adopted in this case. Due to the symmetrical fault characteristics and space limitation, waveforms with SLG fault in the inverter station are not duplicated.

4.2.3 Fault Tolerant Operation with Designed Controllers in Case 3

Figure 4-19 shows the circuit diagram with a SLG fault occurring in a transformerless application, and the corresponding simulation waveforms at MMC_1 and MMC_2 are presented in Figure 4-20 and Figure 4-21, respectively. Being grounded in both AC grids, SPWM scheme is applied to avoid the ground

current caused by the common mode voltage generated by SVM scheme. Additionally, the line-to-line voltage of AC grid v_{s1} is adjusted from 10 kV to 2.5 kV to match the converter side voltage in the previous cases.

The dc voltage drops gradually because of the phase current limitation. The magnitude of double line frequency ripple in dc voltage decreases from 23.36 V to 2.74 V (Figure 4-20) in about one fundamental cycle when the designed control is activated. In addition, being solid grounded, AC grid u_{s1} produces a significant ground current i_{g1}, which mainly flows in the loop between the ground of u_{s1} and the SLG fault. As shown in Figure 4-21 (a)-(c), the faulted phase (phase C) currents in i_{p1} and i_{bf} are close to i_{g1}, while the other two healthy phase currents are clamped by the converter side phase current i_{ph1}. To track the dc voltage reference, the magnitude of i_{ph1} grows from 181 A to 222 A, and the apparent unbalanced components in i_{ph} disappear after the designed control works at t = 0.8 s (Figure 4-21 (d)).

Before 0.8 s, the ground current i_{g2} flowing into the neutral point of AC grid v_{s2} in the MMC_2 side is non-zero. This indicates that a zero sequence current is transferred from MMC_1 to MMC_2, which is different from the previous cases (Figure 4-21 (f)). Due to the voltage drop at PCC_1, active power generation of the rectifier reduces to $2P_{rated}$ /3 and large double line frequency ripple is observed in both active and reactive power (Figure 4-21 (g)). The negative sequence currents i_d^- and i_q^- drop to zero in less than one cycle after t =0.8 s (Figure 4-21 (h)). In the inverter station, the converter side phase current i_{ph2} becomes balanced ($i_{g2} \approx 0$) with negative and zero sequence current control starting at 0.8 s. Compared to case 1, with no voltage clamp provided by the Y/Δ transformer, the faulted phase voltage drops to zero, resulting in a more asymmetrical phase current.

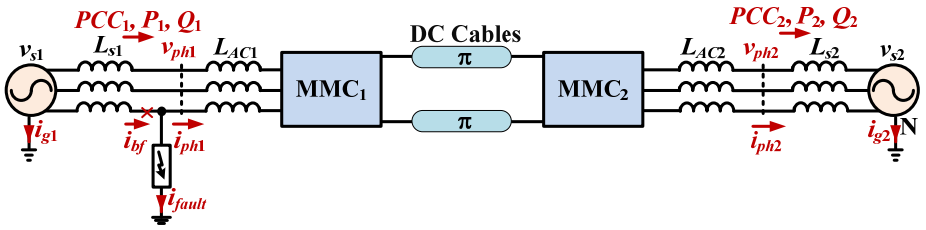


Figure 4-19. Rectifier side SLG fault in case 3.

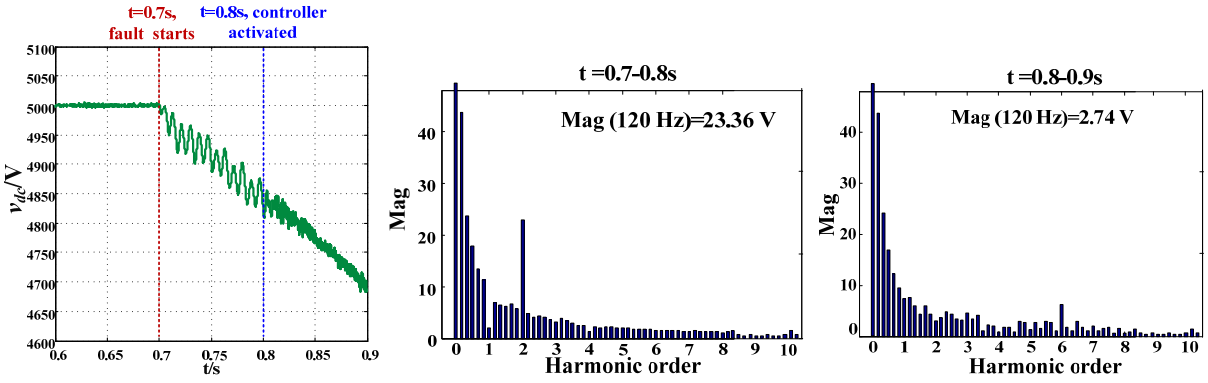


Figure 4-20. DC voltage and its spectrum with SLG fault in case 3 (MMC_1 side).

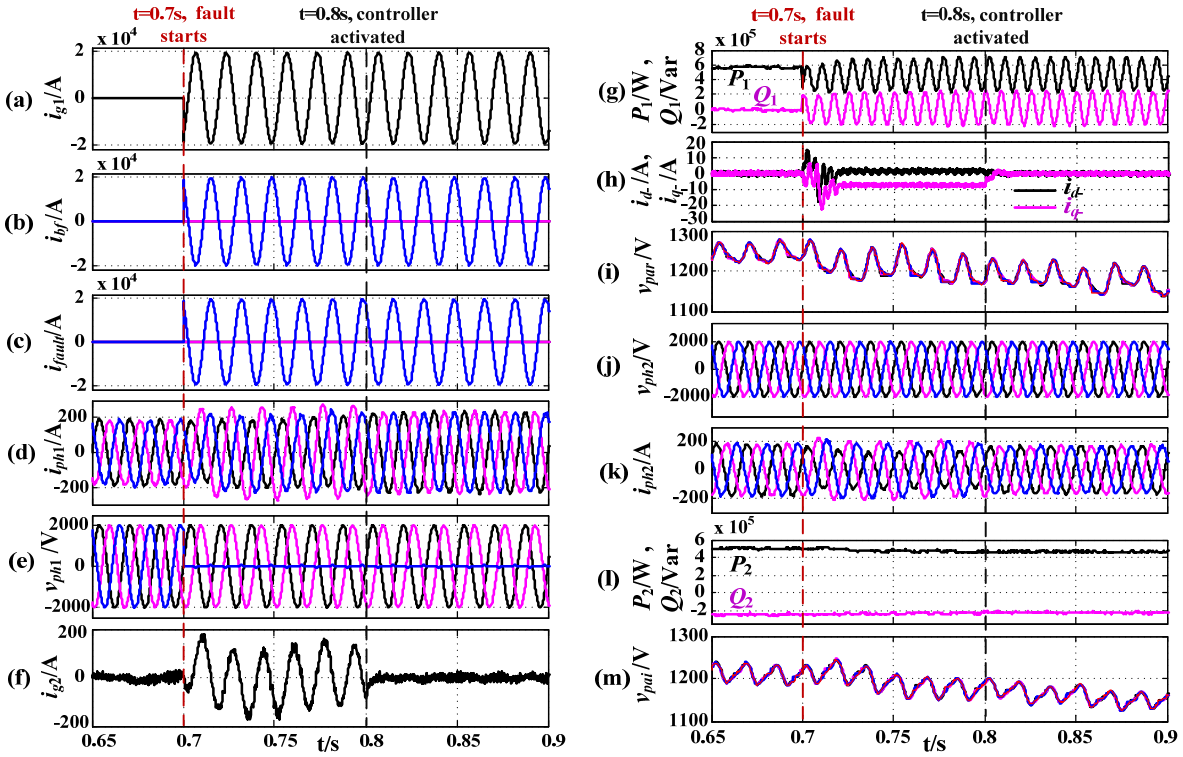


Figure 4-21. Simulation waveforms of the studied system under SLG fault in case 3 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) grid side phase currents, (c) fault current, (d) converter side phase currents, (e) converter side phase voltage, (g) active and reactive power, (h) d and q axis negative sequence current, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (f) AC grid ground current (j) converter side phase voltage, (k) converter side phase current, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm.

On the other hand, the converter-side phase current instead of its positive sequence component is directly used for power and/or voltage control, which helps to mitigate the negative sequence current instantaneously when the fault happens. Thus, i_d^- and i_q^- in this case are still less than 10 A.

Moreover, as a result of lower power generation in the rectifier side, the magnitude of i_{ph2} decreases from 163.3 A to 150.2 A (Figure 4-21 (k)). This in turn induces a lower power generation at PCC_2 (Figure 4-21 (l)). The capacitor voltages of SMs in both stations gradually decrease below their rated values, and their ripples proportionally vary with the magnitude of the corresponding phase currents (Figure 4-21 (i) and (m)). Different from case 2, the zero sequence component of v_{ph1} in this case is low enough to be fully compensated by the converters.

SPS is also applied for system protection and continuous load energy supply. Considering the operating principle of a circuit breaker, SPS should be only activated when fault currents are larger than the preset tripping values, e.g., I_{ref_max} in this paper. Therefore, only the grid side faulted phase is tripped to block the large ground current, as represented by the red-cross mark in Figure 4-19. Furthermore, if the converter side faulted phase is also tripped, the controllers cannot work well since it is impossible to achieve balanced phase current with only two phases.

The associated dc voltage and AC waveforms adopting SPS are presented in Figure 4-22 and Figure 4-23, respectively. With a fault connected in the converter side, the dc voltage keeps dropping, even after the SPS operates at t = 0.73 s. The double line frequency dc voltage ripple decreases from 23.43 V to 3.33 V when the proposed control is activated. The grounding current i_{g1} only consists of the zero sequence current contained in i_{bf}, and phase C current flows into the fault point and forms i_{fault}. As the grounding current i_{g2} is eliminated after 0.8 s, the amplitude of i_{g1} decreases from 260 A to 222 A.

System performance after the fault point, including converter side phase voltage and current, active /reactive power generation, capacitor voltages of SMs, etc., is the same as that without SPS. Moreover, symmetrical operation performance can be obtained with a SLG fault in the inverter side except for successful dc voltage regulation. Hence no description or waveforms are repeated.

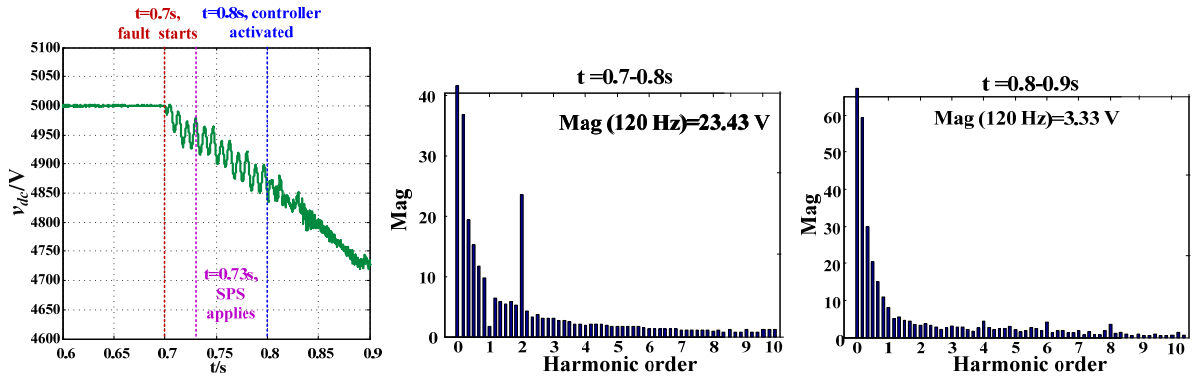


Figure 4-22. DC voltage and its spectrum with single pole switching in case 3 (MMC_1 side fault).

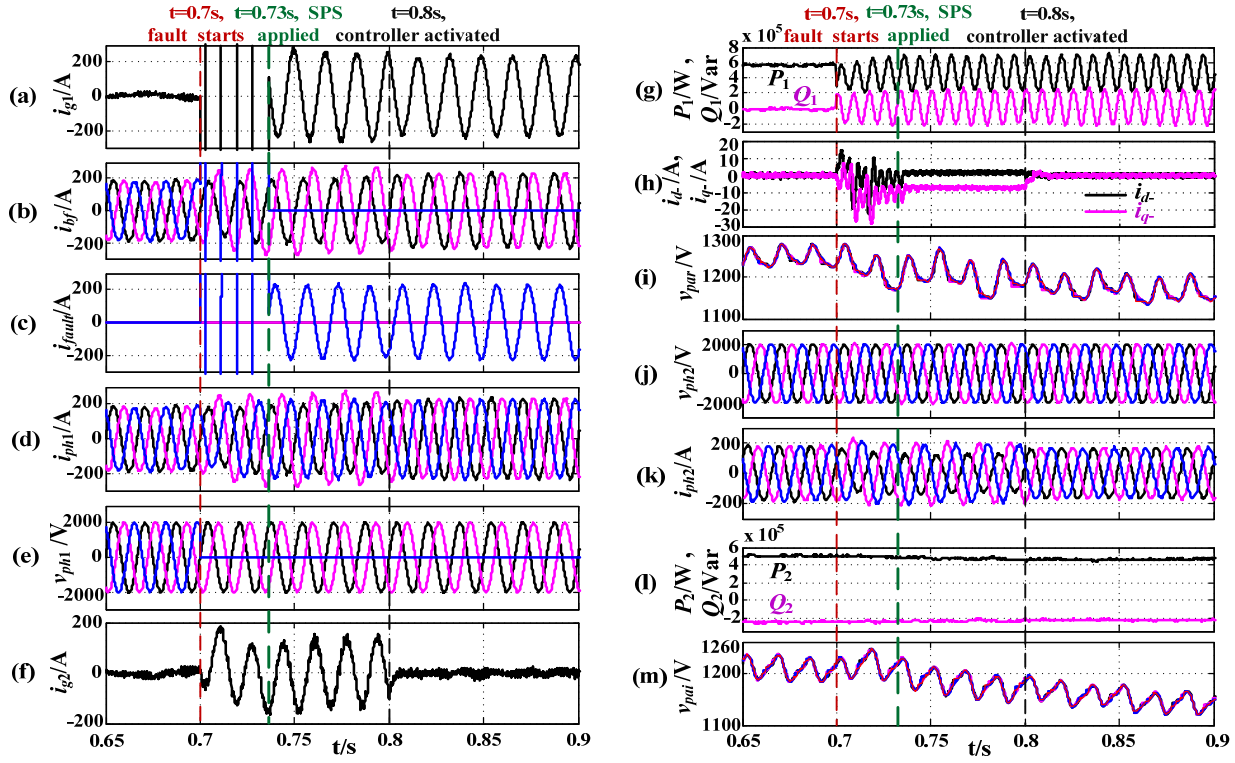


Figure 4-23. Simulation waveforms of the studied system under SLG fault with single pole switching in case 3 (MMC_1 side). **MMC_1 side:** (a) AC grid ground current, (b) grid side phase currents, (c) fault current, (d) converter side phase currents, (e) converter side phase voltage, (g) active and reactive power, (h) negative sequence current components, and (j) capacitor voltages of SMs in phase A upper arm; **MMC_2 side:** (f) AC grid ground current (j) converter side phase voltage, (k) converter side phase current, (m) active and reactive power, and (n) capacitor voltages of SMs in phase A upper arm.

4.2.4 DC Voltage Margin Control

As analyzed in Section 3.1.1 and 3.1.3, if MMC_1 station is responsible for active power generation, when SLG fault occurs in the transformerless case or the primary side of Y/Δ transformer in this station, dc voltage will drop because of insufficient active power supply. Otherwise, if MMC_1 station is responsible for active power absorption, the SLG faults in its ac side will induce surplus energy and thus an overvoltage. In reality, either under-voltage or over-voltage is unacceptable since they may trip the protection and interrupt the continuous power transfer. In addition, with low dc voltage, the converter will lose its controllability and operate as a diode bridge. On the other hand, the dc over-voltage will pose a threat to the system since it may exceed the operation range of devices and passive components, and induce severe damage.

As a solution, the dc voltage margin control is adopted for converters regulating active power. Relying on local information, there is no communication requirement for this control. Additionally, consisting of PI controllers, it has inherent zero steady state error for the dc voltage regulation. Moreover, due to the autonomous control modes transition, it avoids mistakes during manual operation and becomes robust.

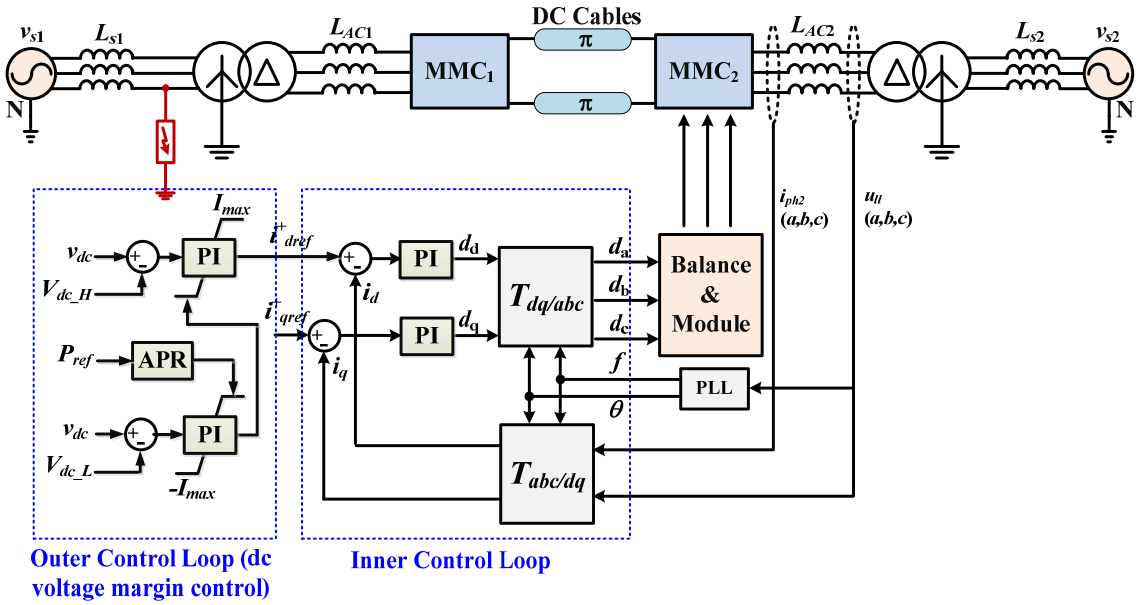


Figure 4-24. Control diagram of dc voltage margin control.

Figure 4-24 shows the control diagram of dc voltage margin control, where V_{dc_H} and V_{dc_L} represent the preset upper and lower dc voltage limit, respectively. Under normal conditions, the dc terminal voltage v_{dc} stays within the range between V_{dc_H} and V_{dc_L}, and the d axis current reference is generated by the active power control (APR). Otherwise, if SLG occurs and MMC_1 cannot bring dc voltage back, MMC_2 will automatically start to regulate dc voltage to either V_{dc_H} (active power generation larger than absorption) or V_{dc_L} (active power generation lower than absorption). The dc voltage margin control is tested in case 1 under different operation conditions. DC voltage level V_{dc_H} and V_{dc_L} are set to 1.07 and 0.93 pu, respectively.

A. MMC_1 suffers a SLG fault and MMC_2 absorbs active power of 0.8 MW (P_{2ref} = 0.8 MW)

The active power direction in Figure 4-25 is defined to be positive. If no dc voltage margin control is employed, dc voltage will drop to about 3974 V (0.79 pu) when another active power balance is achieved, as illustrated in Figure 4-26.

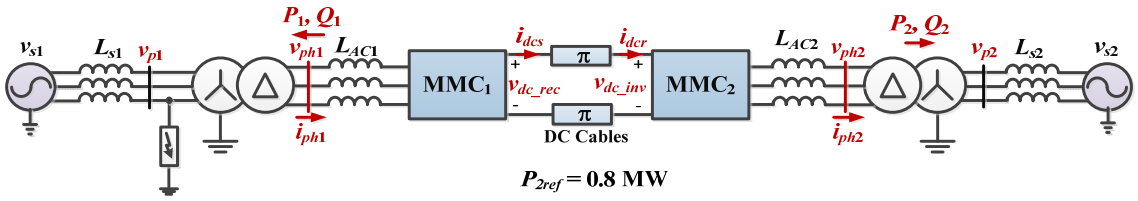


Figure 4-25. System configuration for case 1.

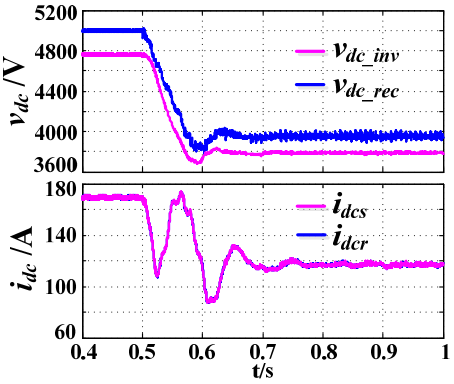
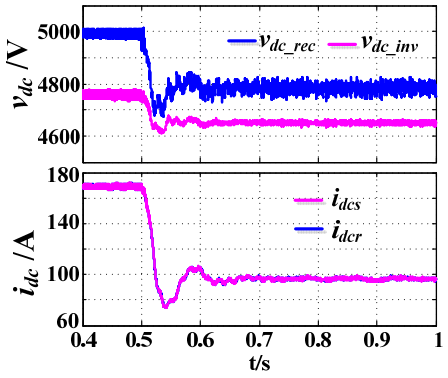
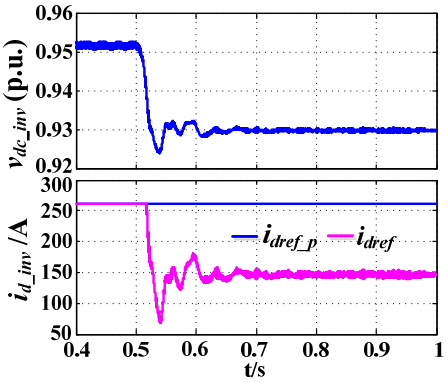


Figure 4-26. DC voltages for case 1, without dc voltage margin control.

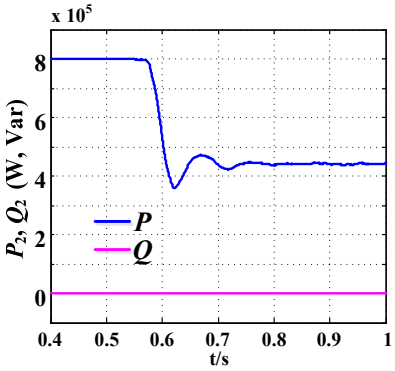
Simulated results with dc voltage margin control are shown in Figure 4-27(b). Although the current reference generated by active power control (i_{dref_p}) remains, the real d axis current reference is determined by dc voltage regulation, which is about 41.86 % lower than its rated value. Consequently, MMC_1 provides its maximum phase current, while the active power absorbed by MMC_2 reduces from 0.8 MW to 0.536 MW (Figure 4-27 (d)) to regulate its dc terminal voltage to the pre-set level of 0.93 pu (Figure 4-27 (a)). For better understanding, the operation point variation of MMC_1 and MMC_2 in this case is illustrated in Figure 4-28. Under normal conditions, MMC_1 operates as a slack bus and takes charge of voltage regulation. MMC_2 works as an inverter and controls active power absorption. During SLG fault, MMC_1 outputs the maximum allowed ac current and goes into constant active power generation mode, while MMC_1 reduces its active power absorption and controls dc voltage to V_{dc_L}.



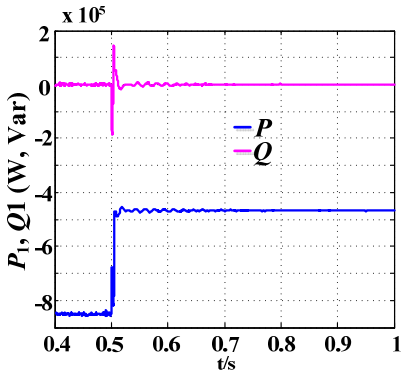
(a) DC voltages



(b) d axis current reference

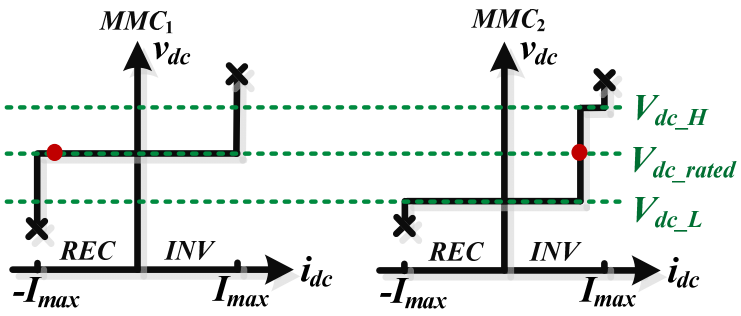


(c) Active and reactive power in MMC_2 station

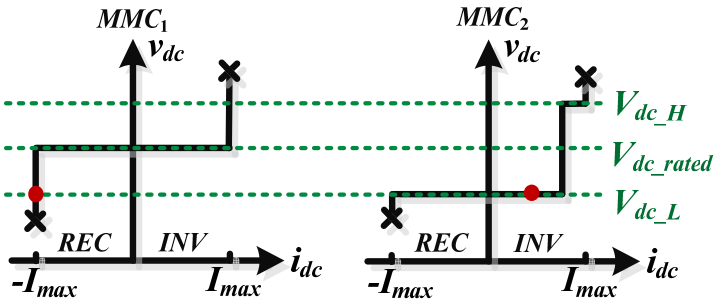


(d) Active and reactive power in MMC_1 station

Figure 4-27. Simulated results for case 1, with dc voltage margin control.



(a) Normal condition



(b) SLG fault occurs in MMC_1 station in case 1

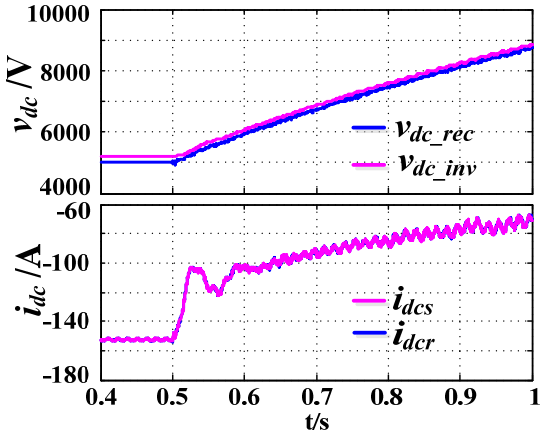
Figure 4-28. Operation points of MMC_1 and MMC_2 with dc voltage margin control.

B. MMC_1 suffers a SLG fault and MMC_2 generates active power of 0.8 MW (P_{2ref} = -0.8 MW)

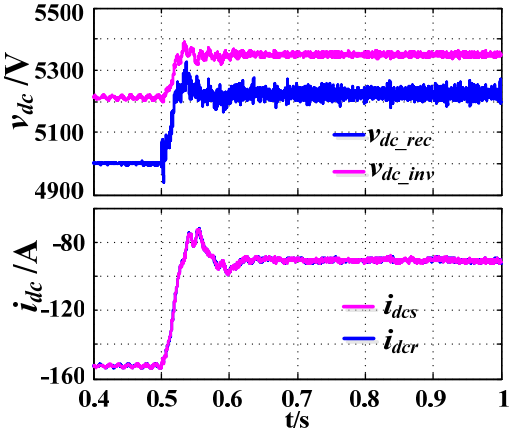
The same system configuration in Figure 4-25 is used, and MMC_2 generates instead of absorbing 0.8 MW active power. Figure 4-29 gives the simulation results with and without dc voltage margin control when a SLG fault happens. If no margin control is implemented, active power generated in MMC_2 is constant, while the active power absorbed by MMC_1 reduces by about 37.5%. Consequently, dc voltage keeps increasing and becomes hazardous to devices and passive components. On the other hand, with dc voltage margin control, the active power generated by MMC_2 drops and dc voltage is controlled to 1.07 pu (V_{dc_H}) as expected.

C. *MMC_2 suffers a SLG fault*

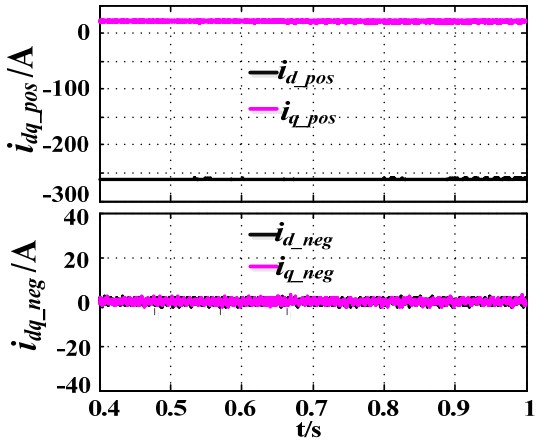
Figure 4-30 and Figure 4-31 give the operation performance of a HVDC system with MMC_2 station side SLG fault and dc voltage margin control, when MMC_2 absorbs (case 3) or generates (case 4) 0.8 MW active power, respectively.



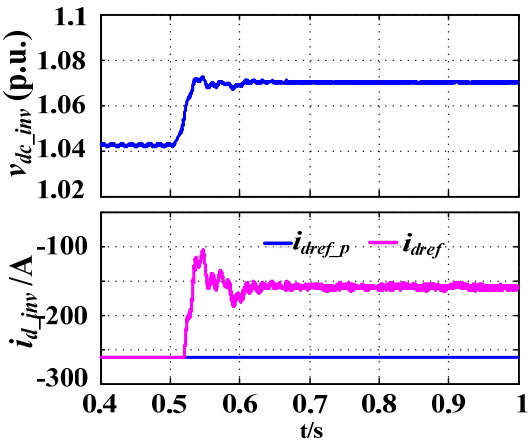
(a) DC voltages



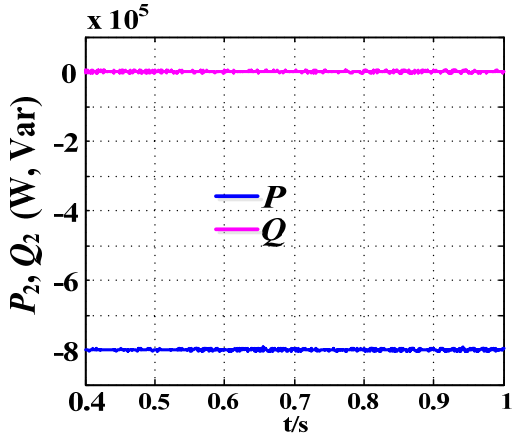
(a) DC voltages



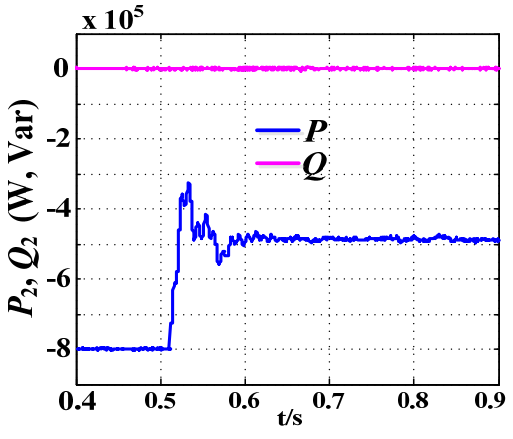
(b) dq axis current



(b) d axis current reference



(c) Active and reactive power



(c) Active and reactive power

Figure 4-29. Simulated results for case 2, with (left column) and without (right column) dc voltage margin control.

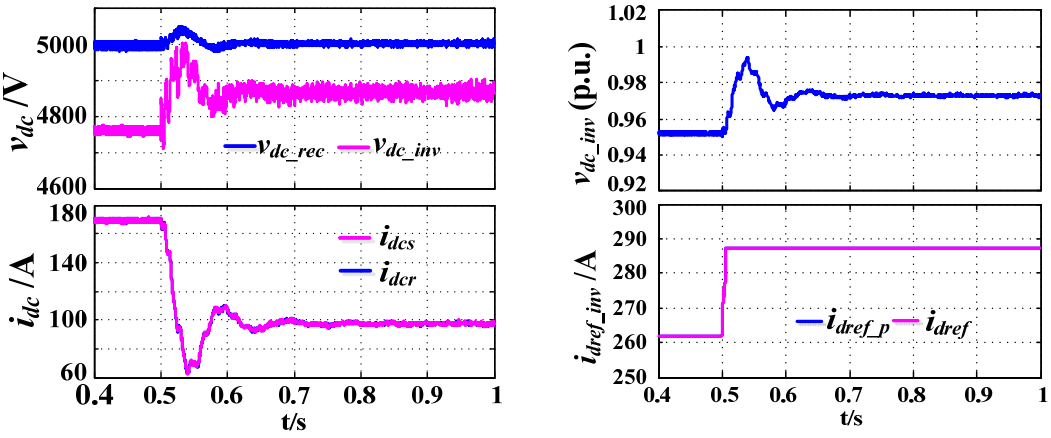


Figure 4-30. Simulated results for case 3, with dc voltage margin control.

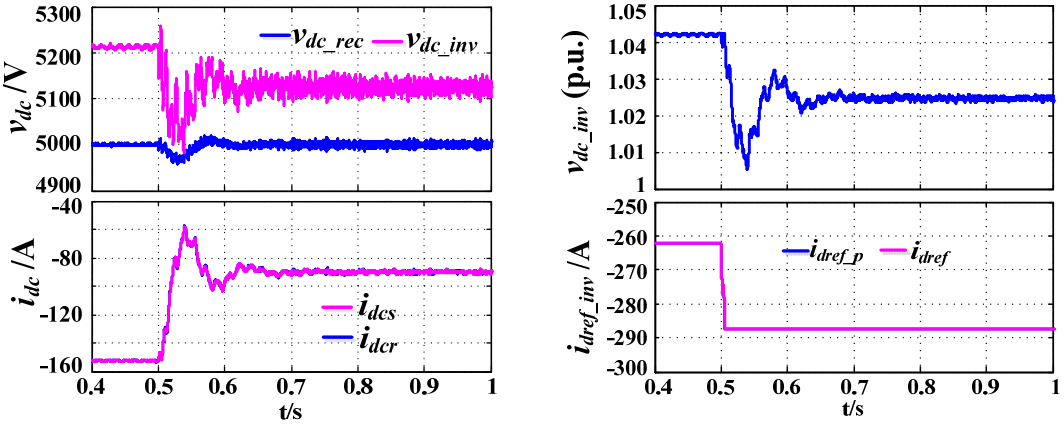


Figure 4-31. Simulated results for case 4, with dc voltage margin control.

Since MMC_1 is still able to maintain the dc voltage in these two cases, dc voltage control in MMC_2 station will be bypassed, leaving APR unaffected, no matter if P_{2ref} is set to 0.8 MW or -0.8 MW.

In summary, through dc voltage margin control, no over- and under- voltage will occur in HVDC systems during a SLG fault. By setting different upper and lower dc voltage limits, the active power transfer during SLG fault conditions can be adjusted. Moreover, the various voltage levels also enable dc voltage margin control a good extensibility to multi-terminal HVDC system. Although a larger dc voltage range (V_{dc_H} - V_{dc_L}) contributes to higher active power transfer, it will lead to lower controllability or higher voltage/current ratings of devices and other components, and hence should be selected carefully.

4.3 Discussion

Up to this point, fault tolerant operation of the MMC-HVDC system under three SLG fault conditions with and without SPS has been investigated. The purpose of this section is to summarize its characteristics under each case and their potential issues.

A. Case 1: SLG Fault Occurs In the Primary Side of the Y/Δ Transformer

The dc voltage and capacitor voltages of SMs can be well regulated with a SLG fault occurring in the inverter side. In contrast, if it occurs in the rectifier side, additional control strategies and/or communication between two converter stations is required to maintain the dc voltage. In both situations, the designed controllers help to mitigate the dc voltage ripple and negative sequence current effectively. Furthermore, the active and reactive power transferred by the HVDC system is determined by the current limitation (power rating) of the converter stations and/or overload capability of the dc cables. Rated power generation is impossible if the maximum current is higher than $3I_{rated}/2$, and vice versa.

On the other hand, if SPS is adopted, desirable performance including rated output power capability, stable dc voltage, and balanced phase currents in the converter sides, etc., can be obtained under SLG fault conditions. The only issue is that unbalanced grid side current in the faulted station is inevitable if the faulted phase is cut from both sides.

B. Case 2: SLG Fault Occurs In the Secondary Side of the Y/Δ Transformer

In this case, despite oscillations which are slowly damped, rated output power and balanced capacitor voltages can be achieved at both converter stations as long as the dc side is grounded through high impedances. Although the ground potential floating leads to abnormal dc bus to ground voltage and converter side phase voltage in the other station, the voltage difference between the two dc buses and line-to-line voltage stay the same.

In addition, by using the implemented control scheme, low negative sequence current in the faulted station can be easily eliminated, while the compensation of zero sequence current is still quite difficult with limited output power capacity.

C. Case 3: SLG Fault Occurs in a Transformerless System

In order to ensure normal operation of controllers, the faulted phase with SLG fault is only cut from the grid side. Therefore, other than SPS, additional dc voltage regulation scheme, e.g., dc voltage margin control, is necessary during a SLG fault. With the power reference of the inverter reduced to $(2I_{ref_max}/3I_{rated})\times P_{rated}$, stable dc voltage (or active power) can be achieved with phase current magnitude of I_{ref_max}, and rated phase current can be obtained with power reference of 2/3 P_{rated}.

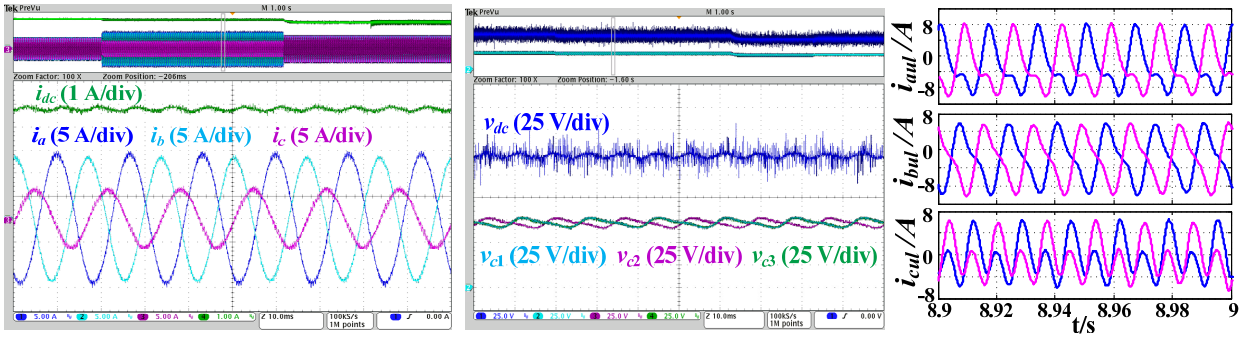
Different from case 1 and case 2, the zero sequence current caused by a SLG fault in one station will be transferred to the other station and cause grounding current to flow into the neutral point of both AC grids. Fortunately, the zero as well as negative sequence current can be fully suppressed by the designed controllers. In order to achieve small grounding current and low performance degradation in case 2 and case 3, large dc side grounding resistance can be used. However, personnel safety, fault detection, and protection are a concern in such systems.

Although the current magnitude may vary case by case with different grounding types, transformer connections and ratios, dc voltage regulation schemes, and cable overload capability, etc., the fault characteristics and operating principle should be the same as that analyzed above. The two converter stations could compensate the negative and/or zero sequence currents separately, while to avoid conflicts between controllers in the two converter stations, only the one suffering a SLG fault is designed to suppress the double line frequency dc voltage ripple. Furthermore, the proposed controller and operation principle will be more effective and important in higher power applications with larger dc voltage ripple and negative/zero sequence currents.

4.4 Experimental Verification

The cascaded control schemes are tested in a three-phase MMC prototype shown in Figure 3-6. An ac voltage source manufactured by California Instrument (FCS series II, 0 – 270 Vac,18 kVA) is used to emulate the SPO condition. Constrained by the ground current protection installed in the lab, only primary side SLG fault is implemented.

Figure 4-32 shows the selected experimental results with only positive sequence current control. When the SLG fault occurs, converter side phase current becomes unbalanced because of the negative sequence component. Meanwhile, the zero sequence circulating current flows into the dc side, forming a second order dc current ripple. Its magnitude, however, is only 0.09 A (2.05 %) due to the large dc load resistance. The percentage values here and in the following descriptions refer to a comparison of current and voltage components to rated dc voltage of 150 V and dc current of 4.98 A.



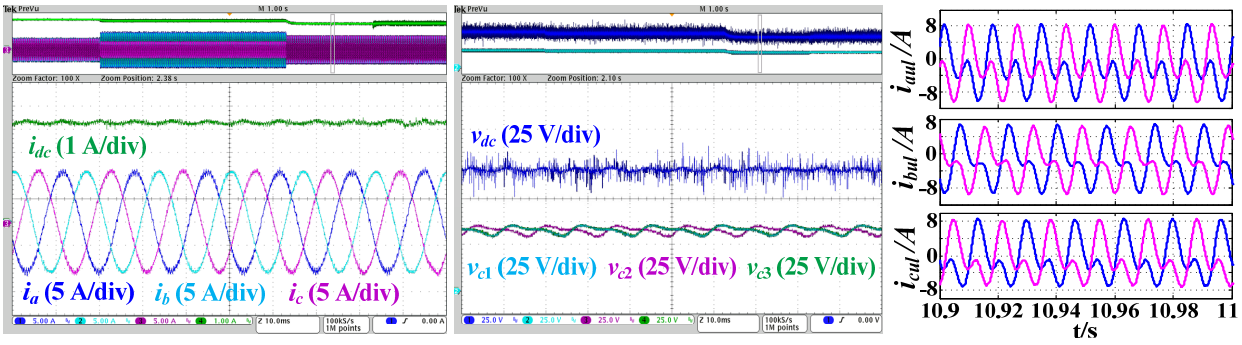
(a) Converter side phase current and dc current (b) Capacitor voltage in phase A and dc voltage (c) Three phase arm currents

Figure 4-32. Experimental results of a MMC rectifier under SLG fault, without negative sequence phase current control.

The dc components in the three-phase arm currents change from 1.66 A under normal condition to 2.33 A (140.4 %), 2.05 A (123.5 %) and 0.4 A (24.1 %) under SLG fault, which represents uneven active power contributions. Moreover, the three-phase arm currents present different shapes and RMS values because of unbalanced phase and circulating current, resulting in unequal power losses across semiconductor devices. The second order ripple can also be observed in the dc voltage, which has a magnitude of 2.58 V (1.72 %). Additionally, without dc central capacitors, the switching ripple cannot be filtered as in two level VSCs, and appears in both dc voltage and current (Figure 4-32 (a) and (b)).

After the negative sequence current control is activated, converter side phase current becomes balanced, as shown in Figure 4-33(a). This balanced phase current, however, results in a further drop of dc voltage, which reduces from 144.4 V (96.3 %) in Figure 4-33 (b) to 129.8 V (86.54 %) in Figure

4-33(b). Compared to Figure 4-32, the second order ripple in both dc current and dc voltage are reduced, which are 0.06 A (1.4 %) and 1.69 V (1.13 %) in this case. The dc components in three phase arm current drop to 1.89 A (113.9 %), 1.91 A (115.1 %) and 0.5 A (30.1 %).

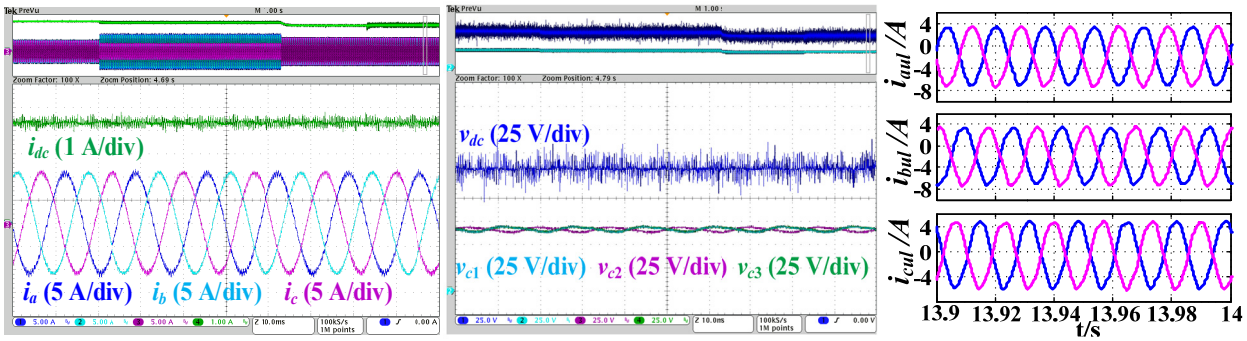


(a) Converter side phase current and dc current (b) Capacitor voltage in phase A and dc voltage (c) Three phase arm currents

Figure 4-33. Experimental results of a MMC rectifier under SLG fault, with negative sequence phase current control.

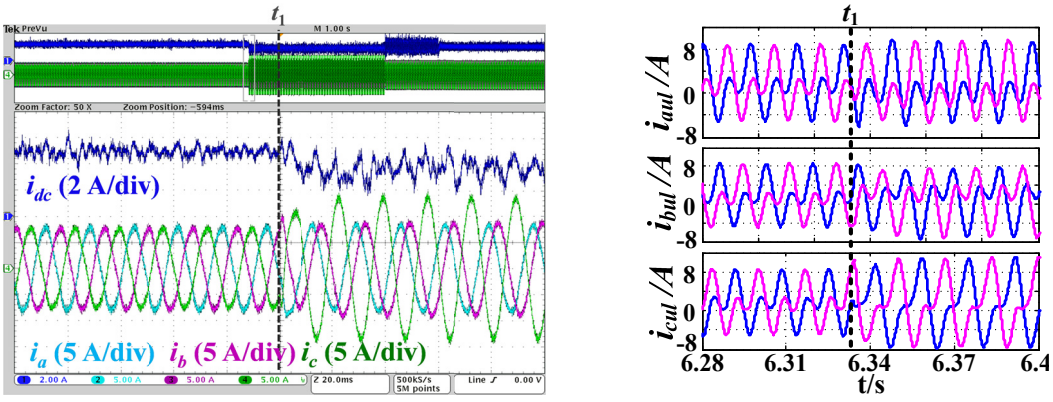
Figure 4-34 illustrates the experimental results when circulating current control is also activated in abc coordinates. The double line frequency positive, negative and zero sequence circulating current are greatly suppressed, enabling sinusoidal arm currents and a second order dc current ripple of 0.01 A (0.2 %). The dc components in three phase arm currents are slightly affected, which are 1.92 A (115.7 %), 1.92 A (115.7 %) and 0.56 A (33.7 %). In spite of the elimination of circulating current, a second order dc voltage ripple with magnitude of 0.49 V (0.33 %) (Figure 4-34 (b)) still exists because of the first four items in zero sequence phase voltage ripple in (3-19). The additional switching actions induced by circulating current control add more switching ripple in the dc voltage and current [134].

Figure 4-35 gives the transient performance of a MMC inverter when a SLG fault occurs at t_1. Similar to Figure 4-32, the SLG fault leads to unbalanced phase currents and lower active power generation. Consequently, the dc components in three phase arm current reduce to 1.19 A (71.7 %), 1.21 A (72.9 %) and 1.33 A (80.1 %), respectively.



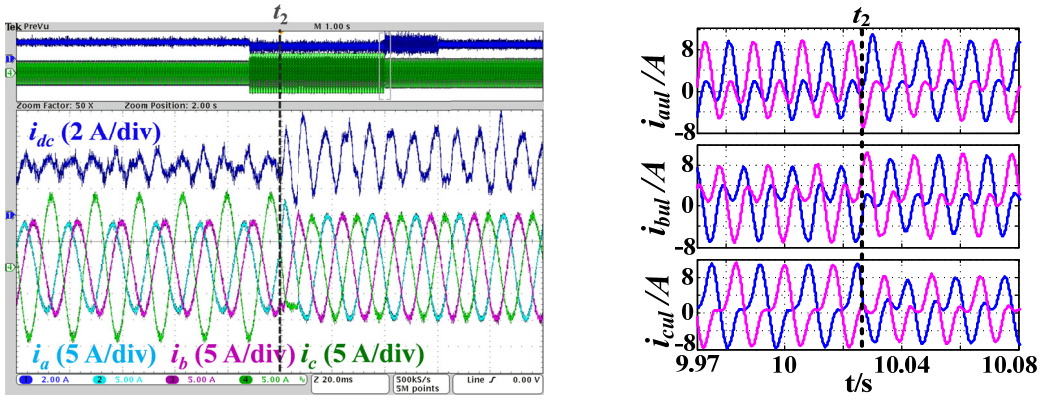
(a) Converter side phase current and dc current (b) Capacitor voltage in phase A and dc voltage (c) Three phase arm currents

Figure 4-34. Experimental results of a MMC rectifier under SLG fault, with negative sequence phase current and circulating current control.



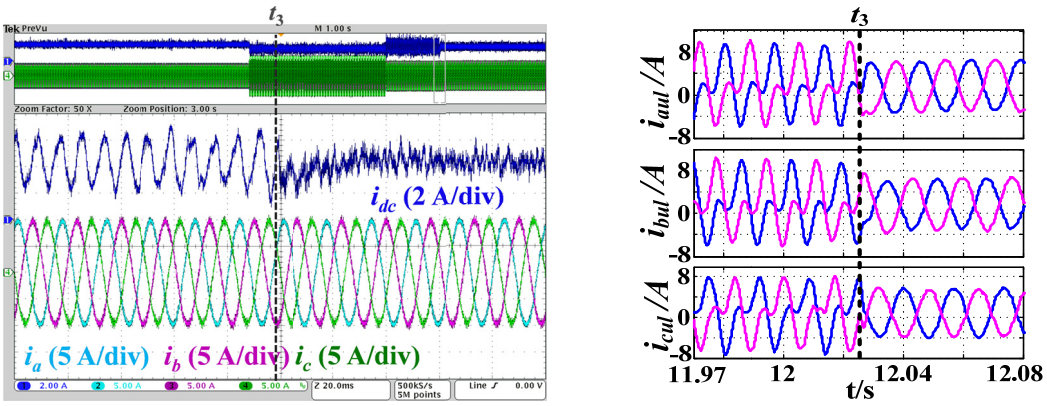
(a) Converter side phase current and dc current (b) Three phase arm currents

Figure 4-35. Transient performance of a MMC inverter when SLG fault occurs.



(a) Converter side phase current and dc current (b) Three phase arm currents

Figure 4-36. Transient performance of a MMC inverter when negative sequence current control starts.



(a) Converter side phase current and dc current (b) Three phase arm currents

Figure 4-37. Transient performance of a MMC inverter when circulating current control is activated.

When the negative sequence current control starts at t_2, the converter side phase current becomes balanced within a fundamental cycle (Figure 4-36(a)). However, the magnitude of second order dc current ripple increases to 4.37 A (87.8 %), and active power is more unevenly distributed among the three phases, leading to dc arm currents of 1.75 A (105.4 %), 1.73 A (104.2 %) and 0.9 A (54.2 %) (Figure 4-36 (b)). When circulating current control is enabled at t_3, the second order dc current drops to 0.01 A and arm currents become sinusoidal with dc components of 1.73 A (104.2 %), 1.70 A (102.4 %), and 0.87 A (52.4 %) in the three phases (Figure 4-37).

4.5 Summary

In order to improve the overall reliability of the MMC-HVDC transmission system, the technical feasibility of maintaining its operation performance with/without single pole switching under SLG fault is investigated in this chapter. The fault characteristics and controllers' design are discussed. Simulation and experimental results with the proposed controllers are presented under different fault cases. The key points included in this chapter could be summarized as follows:

1) The proposed quasi-PR dc voltage ripple suppression control, together with negative and/or zero sequence current control, enables the HVDC system to have low dc voltage ripple as well as balanced AC

line currents at both converter stations under different SLG faults. Moreover, only dc voltage is required to be measured, and thus no extra hardware is introduced for the controller implementation.

2) The fault characteristics of a HVDC system, including dc voltage, ground current, converter side phase currents, and power output capability, etc., in three possible fault cases are analyzed and compared to illustrate the demand of protective devices and a generalized controller.

3) Fault tolerant operation performance of the HVDC system with/without single pole switching are discussed and compared in detail to illustrate the merits of SPS.

4) Performance of DC voltage margin control under different scenarios is evaluated. As a communication free scheme, it helps HVDC system achieve autonomous power balancing between different terminals.

5 Active Startup Scheme for MMC-HVDC Systems from Blackout Conditions

This chapter derives the charging loops of MMC rectifier and inverter during uncontrolled pre-charge period, with special focus on the necessity of additional capacitor charging schemes. Moreover, the small signal model of the capacitor charging loop is first derived according to the internal dynamics of the MMC inverter. Based on this model, a novel startup strategy incorporating an averaging capacitor voltage loop and a feedforward control is proposed, capable of enhanced dynamic response and system stability without sacrificing voltage control precision. The design considerations of the control strategy are also given in detail. Simulation results from a back-to-back MMC (BTB-MMC) system supplying passive loads, and experimental results from a scaled-down MMC are provided to support the theoretical analysis and proposed control scheme.

5.1 Uncontrolled Pre-charge Process of MMC

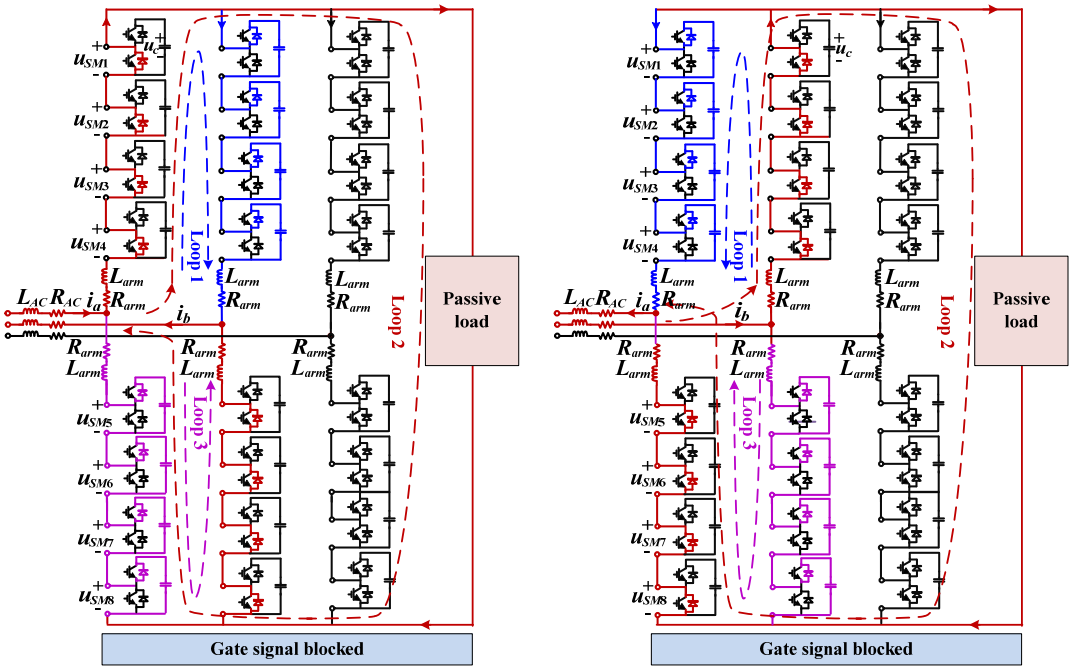
5.1.1 For MMCs Operating in Rectifier Mode

A. Charging Loops

Considering different phase current directions, one of the possible capacitor charging loops between phase A and B during the uncontrolled pre-charge stage ($N = 4$) is shown in Figure 5-1, with conducting devices highlighted by different colors.

Considering different phase current directions, the possible capacitor charging loops between phase A and B during the uncontrolled pre-charge stage are shown in Figure 5-1. Among the denoted three loops, loop 1 and loop 3 charge the upper and lower arm capacitors respectively, while loop 2 only supplies current for the passive load. In most applications, the load impedance in loop 2 is much higher than the equivalent impedance in loop 1 and loop 3, and thus the phase current will charge the SM capacitors first until the sum of their voltages reaches the peak value of the line to line ac voltage. Then, loop 1 and loop 2 are blocked and the phase current starts to flow through the load.

As illustrated in Figure 5-1 (a) and (b), with a positive phase current (defined as flowing from ac side to dc side), capacitors in the upper arm of the phase are bypassed, while those in the lower arm get charged. On the contrary, with a negative phase current, capacitors in the upper arm are charged and those in the lower arm are bypassed. This conclusion is also valid for all combinations of the three phase currents. For example, if $i_a > 0$, $i_b < 0$, $i_c > 0$, i_a and i_c in Figure 5-1 (a) will charge all upper arm capacitors in phase B together, and charge their own lower arm capacitors separately. Since the capacitors in each arm are charged synchronously, at the end of this uncontrolled pre-charge period, all SM capacitors will be charged to $2.34V_{ph} / N$ with heavy load or $\sqrt{6}V_{ph} / N$ with no load (V_{ph} is the RMS value of the phase voltage).



(a) $i_a > 0$, $i_b < 0$ (b) $i_a < 0$, $i_b > 0$

Figure 5-1. Charging loops between phase A and B in a MMC rectifier during pre-charge stage.

B. Current Limiting Resistor Selection

Similar to a two-level VSC, AC side current limiting resistors are required to protect the system from large inrush current when it starts from a completely de-energized condition. The resistance should be

selected deliberately considering the tradeoff between inrush current and charging time. For low power loss, these resistors will be bypassed after the pre-charge period. Figure 5-2 gives the charging loops of the MMC rectifier and its equivalent circuit between phase A and B, where R_e, L_e and C_e represent the equivalent loop resistance, inductance and capacitance, respectively; u_{ce} denotes the total capacitor voltage in this loop.

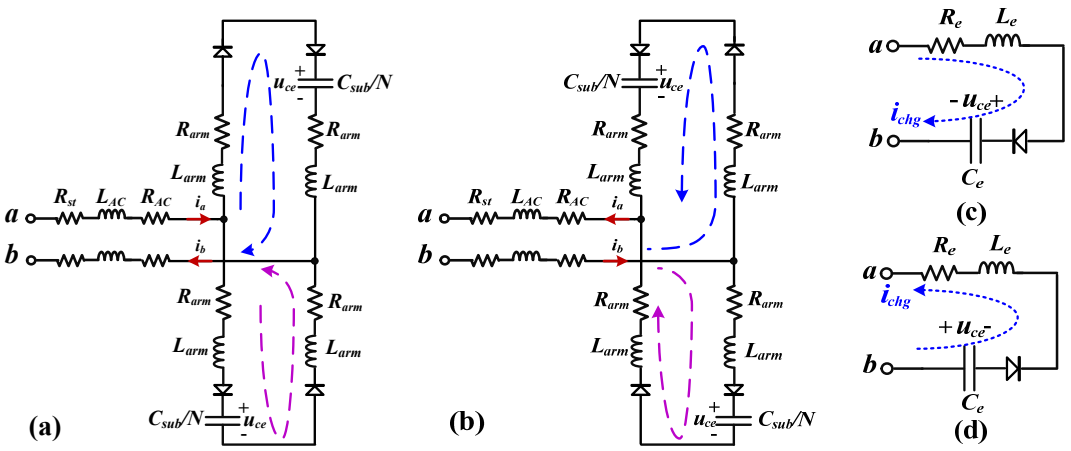


Figure 5-2. Charging loop between phase A and B with (a) $i_a > 0$, $i_b < 0$, and (c) its equivalent circuit, (b) $i_a < 0$, $i_b > 0$, and (d) its equivalent circuit.

According to Figure 5-2, the following equations hold during the pre-charge period:

$$R_e = 2\left(R_{st} + R_{AC}\right) + R_{arm},\ L_e = 2L_{AC} + L_{arm},\ C_e = 2C_{sub} / N \tag{5 - 1}$$

$$\begin{aligned} &L_e \frac{di_{chg}(t)}{dt} + R_e i_{chg}(t) + u_{ce}(t) = \sqrt{3}V_{ph}\sin(\omega t) \\ &u_{ce}(t) = \frac{1}{C_e}\int i_{chg}(t)dt \\ &u_{ce}(t)\big|_{t=0} = 0 \end{aligned} \tag{5 - 2}$$

where R_{st} is the current limiting resistance and i_{chg} represents the phase charging current.

Assuming that R_{st} is much larger than ωL_e, the maximum RMS value of the charging current can be calculated by solving (5 - 2).

$$I_{chg_\max} = \frac{\sqrt{3}V_{ph}}{\sqrt{R_e^2 + \left(\omega L_e - \frac{1}{\omega C_e}\right)^2}} \quad . \tag{5 - 3}$$

The current limiting resistance can be selected according to (5 - 4) for a given maximum allowable inrush current I_{chg_set}.

$$R_{st} = \frac{1}{2}\left(\sqrt{\frac{3V_{ph}^2}{I_{chg_set}^2} - \left(\omega L_e - \frac{1}{\omega C_e}\right)^2} - R_{arm}\right) - R_{AC} \tag{5 - 4}$$

The above equation only provides a preliminary design criterion of the current limiting resistor, and additional considerations and simulation are required to obtain an optimized value.

C. Necessity of Capacitor Charging Control

If N + 1 level modulation schemes (PS-SPWM, LS-SPWM, NLC, etc.) are adopted, N SM capacitors (with a voltage of V_c for each SM) in each phase will be inserted during normal operation. Also, according to the above analysis, at the end of the uncontrolled pre-charge period the dc voltage can be built to NV_c. Consequently, the difference between dc voltage and the inserted SM capacitor voltage is zero ($Nv_c(t) = v_{dc}(t)$), and rated capacitor voltage is not necessary before dc voltage regulation is activated.

If the initial value of the dc voltage ramp reference is set to NV_c, the integrator of the PI controller will not be saturated because of small error between the voltages. However, the actual dc voltage which relies heavily on load impedance may be less than $\sqrt{6}V_{ph}$, and the modulation index will be slightly larger than 1 initially, resulting in an inrush phase current.

Being charged by the inrush current, the capacitor voltages increase quickly, which recovers the duty cycle from saturation. Then, the converter is capable of controlling both dc voltage and phase current. In addition, compared to SPWM modulation scheme, a shorter duty cycle saturation time and smaller inrush current can be achieved with SVM due to lower dc voltage requirement.

5.1.2 For MMCs Operating in Inverter Mode

A. Charging Loops

Different from a MMC rectifier, all capacitors in a MMC inverter will be inserted into the charging loop during the pre-charge period, as shown in Figure 5-3(a). Being charged synchronously by the dc source, the capacitor voltage is around V_{dc} / $2N$ when this stage ends. The charging current flows only between dc voltage and each arm, and no phase current is generated. Moreover, to suppress the large initial capacitor charging current, dc side limiting resistors are required if a constant dc voltage is applied. Otherwise, it would not be necessary if capacitors are charged by a ramp dc voltage regulated by the front end converter.

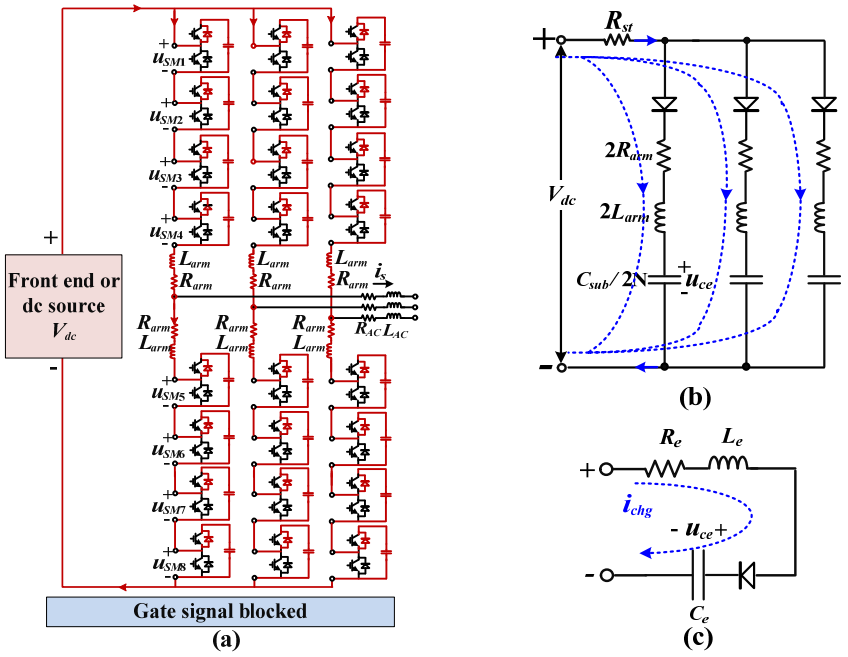


Figure 5-3. (a) Charging loop, (b) three-phase equivalent circuit, and (c) dc side equivalent circuit of a MMC inverter during uncontrolled pre-charge period.

B. Current Limiting Resistor Selection

As illustrated in Figure 5-3(b) and (c), the equivalent circuit of a MMC inverter during uncontrolled pre-charge period can also be represented by a series connected R-L-C circuit.

The peak value of u_{ce} equals to the dc source voltage, and the equivalent charging circuit can be described as

$$R_e = R_{st} + \frac{2}{3}R_{arm},\ L_e = \frac{2}{3}L_{arm},\ C_e = 3C_{sub}/2N \tag{5 - 5}$$

$$L_e \frac{di_{chg}(t)}{dt} + R_e i_{chg}(t) + u_{ce}(t) = V_{dc} \quad u_{ce}(t) = \frac{1}{C_e}\int i_{chg}(t)dt \quad u_{ce}(t)\big|_{t=0} = 0 \tag{5 - 6}$$

where R_{st} is the current limiting resistance and i_{chg} represents the phase charging current.

Solving (5 - 5) and (5 - 6) yields the peak value of charging current, as shown in (5 - 7), and the current limiting resistance can be selected accordingly with a given current limit.

$$i_{peak} = \frac{V_{dc}}{2L_e\omega_0\sqrt{\xi^2 - 1}}(e^{-\alpha_2 t_{pk}} - e^{-\alpha_1 t_{pk}}) \tag{5 - 7}$$

where,

$$\xi = \frac{\alpha}{\omega_0};\ \alpha = \frac{R_e}{2L_e};\ \omega_0 = \frac{1}{\sqrt{L_e C_e}};\ \alpha_1 = \omega_0\left(\xi + \sqrt{\xi^2 - 1}\right);\ \alpha_2 = \omega_0\left(\xi - \sqrt{\xi^2 - 1}\right);\ t_{pk} = \frac{\ln(\alpha_1/\alpha_2)}{\alpha_1 - \alpha_2}.$$

C. Necessity of Capacitor Charging Control

At the end of the uncontrolled pre-charge period, the total equivalent capacitor voltage is V_{dc} / 2 assuming N SMs are inserted in each phase (no redundant SMs). Therefore, the other V_{dc} / 2, i.e., the difference between the equivalent capacitor voltage and constant dc bus voltage, will apply on the arm inductors as well as their ESRs, leading to a significant inrush current in the charging loops (even higher with more redundant SMs). Therefore, in a MMC inverter, dc loop resistors or fully charged capacitors are necessary before normal operation (power or current control) starts.

5.2 Capacitor Charging Control of MMC Inverter

As a more economic option, a novel capacitor charging scheme is proposed, with the detailed modelling and design considerations discussed in this section. Figure 5-4 shows the overall control block diagram of a MMC inverter during startup process. The proposed capacitor charging control scheme mainly consists of an averaging capacitor voltage control and a capacitor voltage feedforward control. As

highlighted in the dashed pink block, the average capacitor voltage is regulated by a PI controller in the outer loop, and its output is used as the reference of the inner circulating current loop.

Aiming at faster dynamic response, a feedforward control is added to the output of the averaging capacitor voltage control. A compensation is also made on the duty cycle d_c (as shown in the blue block in Figure 5-4) to counteract the impact of modulation wave generation.

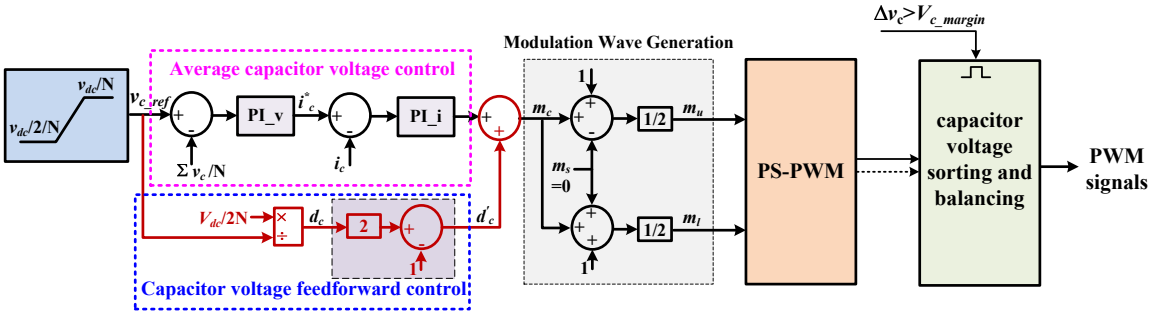


Figure 5-4. Overall control block diagram of proposed capacitor charging control.

According to the direct modulation scheme [135], the modulation index for upper and lower arms can be expressed as $m_u = (1 - m_s + m_c) / 2$, $m_l = (1 + m_s + m_c) / 2$, where m_s and m_c represent the modulation index generated by power (or dc voltage) regulation and circulating current control, respectively. To achieve the target duty cycle $d(t)$ in both m_u and m_l, a compensation should be made and d'_c in Figure 5-4 is set to $2d(t) - 1$. If other modulation schemes are used, the compensation needs to be modified correspondingly to get the targeted duty cycle $d(t)$ in m_u and m_l. During the startup process, modulation index m_s created by the power and/or phase current control keeps zero to eliminate the phase current and voltage.

In addition, in order to achieve balanced capacitor voltages, the widely used sorting and balancing technique [73] is activated during both startup and normal operations. Furthermore, in order to reduce the additional switching transitions and associated switching loss, the balancing control is only activated when the maximum capacitor voltage deviation is larger than the preset threshold V_{c_margin}. In this

technique, all the SM capacitor voltages are measured and sorted. If the arm current (either upper or lower arm) is positive, SMs with the lowest voltages are identified and inserted, while the SMs with highest voltages are inserted if the arm current is negative.

In the following analysis, impedances of all six arms are considered to be identical, and energy stored in upper and lower arm capacitors is balanced. If asymmetrical arm impedance is used, a significant deviation between upper and lower arm capacitor voltages will be generated under normal operation conditions, thus requiring special control schemes to prevent potential damage to passive components and devices. During startup period, however, thanks to the zero fundamental frequency ac current and voltage, and relatively low dc charging current and arm resistances (normally 1% ~ 5% of the arm impedance), the unbalanced capacitor voltage is fairly low and will not lead to any issues.

5.2.1 Small Signal Model of Capacitor Voltage Charging Loop

According to [127], the internal dynamics of MMC can be represented by state variables v_c^{Σ}, v_c^{Δ}, and i_c

$$\begin{aligned}
&\frac{C_{sub}}{N}\cdot\frac{dv_c^{\Sigma}}{dt} = -\frac{v_s^{ref} i_s}{v_{dc}} + \left(1+\frac{2v_{cir}^{ref}}{v_{dc}}\right) i_c \\
&\frac{C_{sub}}{N}\cdot\frac{dv_c^{\Delta}}{dt} = \left(1+\frac{2v_{cir}^{ref}}{v_{dc}}\right)\cdot\frac{i_s}{2} - \frac{2v_s^{ref} i_c}{v_{dc}} \\
&L_{arm}\frac{di_c}{dt} = \frac{1}{2}\left(v_{dc} - \frac{v_c^{\Sigma}}{2} - \frac{v_{cir}^{ref} v_c^{\Sigma}}{v_{dc}} + \frac{v_s^{ref} v_c^{\Delta}}{v_{dc}}\right) - R_{arm} i_c
\end{aligned} \tag{5 - 8}$$

where v_c^{Σ} represents the total capacitor voltages, and $v_c^{\Sigma} = v_{cu}^{\Sigma} + v_{cl}^{\Sigma}$, $v_{cu,l}^{\Sigma} = \sum_{i=1}^{N} v_{cu,li}$; v_c^{Δ} represents the imbalance capacitor voltages, and $v_c^{\Delta} = v_{cu}^{\Sigma} - v_{cl}^{\Sigma}$; V_{dc} is the pole to pole dc bus voltage; i_s and i_c are phase and circulating current, respectively; v_s^{ref} is the reference of the fundamental frequency output voltage; v_{cir}^{ref} is the reference generated by the circulating current control.

During the startup process, v_s^{ref} and i_s are controlled to zero, and thus (5 - 8) can be simplified as

$$\frac{C_{sub}}{N}\cdot\frac{dv_c^{\Sigma}}{dt} = \left(1+\frac{2v_{cir}^{ref}}{V_{dc}}\right) i_c \qquad \frac{C_{sub}}{N}\cdot\frac{dv_c^{\Delta}}{dt} = 0 \qquad L_{arm}\frac{di_c}{dt} = \frac{1}{2}\left(v_{dc} - \frac{v_c^{\Sigma}}{2} + \frac{v_{cir}^{ref} v_c^{\Sigma}}{V_{dc}}\right) - R_{arm} i_c \,. \tag{5 - 9}$$

Define the duty cycle contributed by the circulating current control as d_c. With SPWM scheme in this paper, d_c is given as (5 - 3). Substituting (5 - 3) into (5 - 2) and setting the derivative terms to be zero

yields the steady state duty cycle D_c and circulating current I_{c0} in (4 - 4), with the assumption that the capacitor voltage is well balanced and its reference v_{c_ref} ramps from $V_{dc}/2N$ to V_{dc}/N within a time t_{ramp}.

$$\frac{v_{cir}^{ref}}{V_{dc}/2} = d_c \tag{5 - 10}$$

$$v_{c_ref} = \frac{V_{dc}}{2N} + V_{ramp}\Delta t \quad V_{ramp} = \frac{V_{dc}}{2Nt_{ramp}} \quad M_c = \frac{V_{dc}/2N}{v_{c_ref}} \quad D_c = 2M_c - 1 \quad I_{c0} = \frac{2C_{sub}}{1+D_c}\cdot V_{ramp} \tag{5 - 11}$$

Applying linearization on (5 - 9) and (5 - 10), one obtains the transfer function from $\tilde{i}_c$ to $\tilde{d}_c$ as

$$\frac{\tilde{i}_c}{\tilde{d}_c} = -\frac{2NI_{c0}(1+D_c)}{4s^2L_{arm}C_{sub} + 4sR_{arm}C_{sub} + N(1+D_c)^2} \quad .$$
$$\omega_r = \frac{1+D_c}{2}\sqrt{\frac{N}{L_{arm}C_{sub}}} \tag{5 - 12}$$

where ω_r is the resonant frequency, depending on system parameters as well as operation points. Since D_c and I_{c0} keep changing under different operating conditions, as indicated in (5 - 11), the open loop gain of the transfer function in (5 - 12) is subject to change.

Similarly, the transfer function from $\tilde{v}_c^{\Sigma}$ to $\tilde{i}_c$ is derived as

$$\frac{\tilde{v}_c^{\Sigma}}{\tilde{i}_c} = \frac{-8NL_{arm}I_{c0}s + 2NV_{dc} - 8NR_{arm}I_{c0}}{2sC_{sub}V_c^{\Sigma}} \quad . \tag{5 - 13}$$

According to [136], C_{sub}/N should keep constant to maintain the capacitor voltage ripple under certain operation conditions. In (5 - 12) and (5 - 13), SM capacitance C_{sub} and SM number N always appear as a group. Therefore, as long as C_{sub}/N keeps constant, the variation of N will not affect small signal models of the capacitor charging loop, and the corresponding controller design for a certain operation point is applicable to MMC with different number of SMs per arm. On the other hand, if only N or C_{sub} is changed, (5 - 12) and (5 - 13) will vary accordingly, and the averaging capacitor voltage control should be redesigned to maintain the system stability.

The transfer function of $\tilde{i}_c/\tilde{d}_c$ and $\tilde{v}_c^{\Sigma}/\tilde{i}_c$ are derived based on the assumption that fundamental frequency modulation index is zero during startup process (i.e. $v_{sref} = 0$). Therefore, the capacitor charging controller is only applicable to the startup process.

5.2.2 Averaging Capacitor Voltage Control

The outer loop voltage controller and inner loop current controller can be designed separately as the following steps:

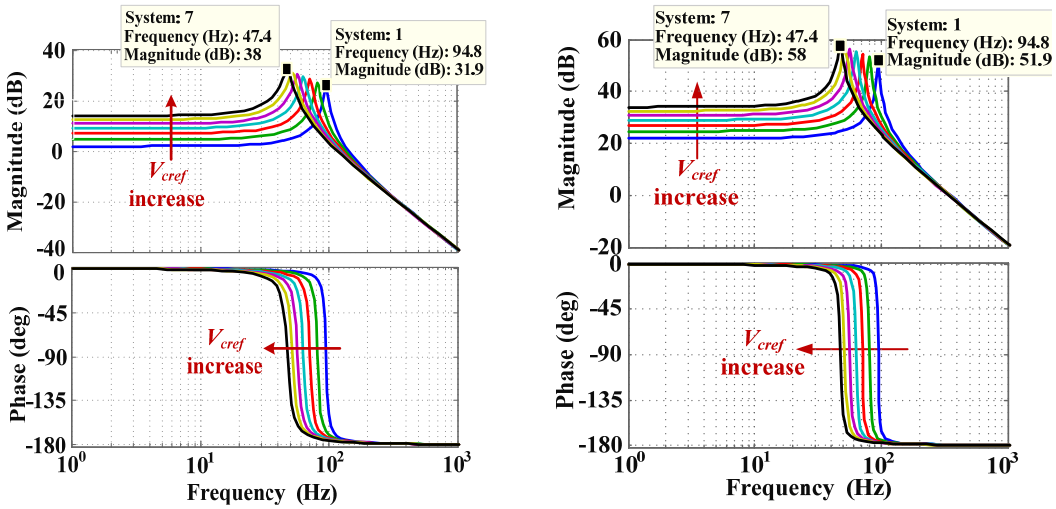
A. Worst Case Selection

According to (5 - 12) and (5 - 13), the open loop gains of both capacitor voltage loop and circulating current loop are subjected to change when v_{c_ref} increases from V_{dc} / 2N to V_{dc} / N. Therefore, it is necessary to identify the worst case and design the controllers at this particular operating point to guarantee system stability during the whole capacitor charging period.

Figure 5-5(a) and (b) show the bode diagram of $\tilde{i}_c$ to $\tilde{d}_c$ with t_{ramp} = 1 s and t_{ramp} = 0.1 s, respectively, based on the main system parameters given in Table 5-1. When V_{c_ref} increases from V_{dc} / 2N to V_{dc} / N, the resonant frequency gradually reduces while its peak magnitude increases accordingly. For example, when t_{ramp} = 1 s and V_{c_ref} = V_{dc} / 2N, the open-loop bode plot of $\tilde{i}_c$ / $\tilde{d}_c$ has a resonant frequency of 94.8 Hz and the peak magnitude is 31.9 dB with the given system parameters in Table 5-1. When V_{c_ref} = V_{dc} / N, however, its resonant frequency reduces to 47.4 Hz, while the magnitude increases to 38 dB.

In the design of a circulating current controller, the proportional gain should be selected low enough to damp all the peak magnitudes below zero. If a designed controller can suppress resonance with the maximum gain, i.e., the worst case, it should be capable of well damping the other resonances. In both figures, when v_{c_ref} = V_{dc} / N, the open loop system gets its largest gain and the minimum phase margin, and thus this condition is regarded as the worst case in both figures.

Compared to Figure 5-5(a), the decrease of t_{ramp} in Figure 5-5(b) has no impact on the phase and resonant frequency of $\tilde{i}_c$ to $\tilde{d}_c$, while it leads to a 20 dB magnitude increase, which requires special attention on the system stability if controllers are designed with other ramp times.

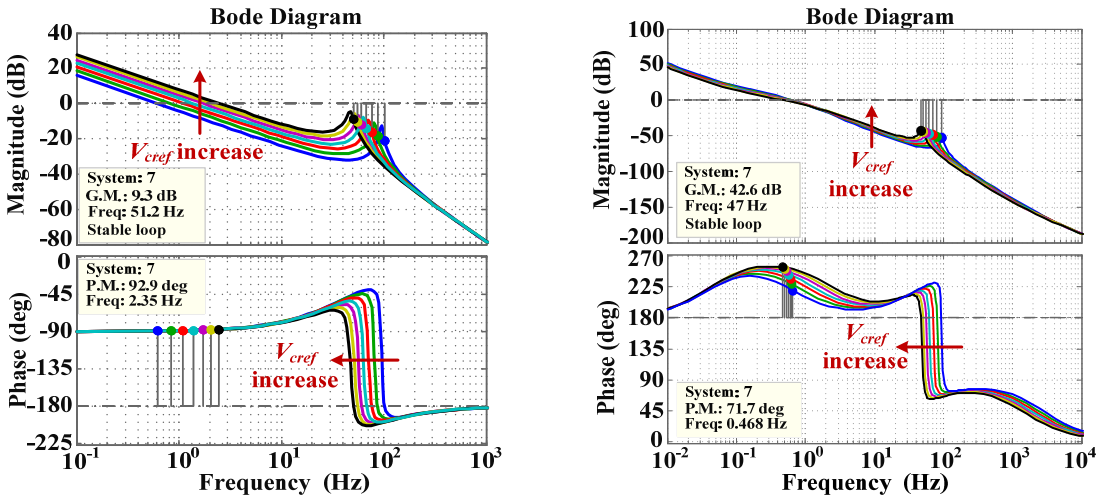


(a) t_{ramp} = 1 s (b) t_{ramp} = 0.1 s

Figure 5-5. Bode diagram of $\tilde{i}_c$ to $\tilde{d}_c$.

B. PI Controller Design

Figure 5-6(a) and (b) give the compensated open-loop bode plot of circulating current and capacitor voltage loops when t_{ramp} = 1 s. As a compromise of dynamic response and stability margin, the control bandwidth of the circulating current loop is selected as 2.35 Hz with the given parameters.



(a) Circulating current loop (b) Capacitor voltage loop

Figure 5-6. Compensated open loop bode diagrams.

In practice, in an effort to suppress inrush current under fault conditions, the arm inductances are normally designed with high values (≈ 0.15-0.2 pu), which will greatly limit the bandwidth of the averaging capacitor voltage control, and degrade the dynamic performance of the averaging capacitor voltage control.

By reducing the proportional gain of the PI controller, identical compensated characteristics of circulating current loop can be achieved when $t_{ramp} = 0.1$ s. The same voltage loop controller will be used in both cases. The control delay should be considered in the controller design, which includes the zero-order hold delay, the computing delay, and one-sampling-period delay, where the sampling delay is the dominant part. In the general implementation of the control scheme, PWM signals are not continuously refreshed, which will inevitably introduce a one-step-delay. In this work, a delay time of $1/Nf_c$ (N and f_c represent SM number per arm and carrier frequency, respectively) is considered during the controller design process.

5.2.3 Capacitor Voltage Feedforward Control

Applying averaging capacitor voltage control, system stability and control performance directly depend on voltage ramp rate V_{ramp}, passive components C_{sub}, L_{arm}, R_{arm}, and operation conditions I_{c0}, D_c, which requires deliberately designed controllers. Additionally, fast dynamic performance cannot be achieved when the resonant frequency between the arm inductance and SM capacitance is low. If only the averaging control is used, the black start and/or recovery capability of MMC based HVDC may not be able to meet corresponding dynamic response requirements in grid codes after large disturbances [137]. To overcome these drawbacks, a feedforward control branch is introduced to the capacitor charging loop, which helps to reduce the dependence on the PI controllers, and improve the dynamic response during the startup process. Moreover, it can either work alone or work together with the averaging control to achieve high control precision.

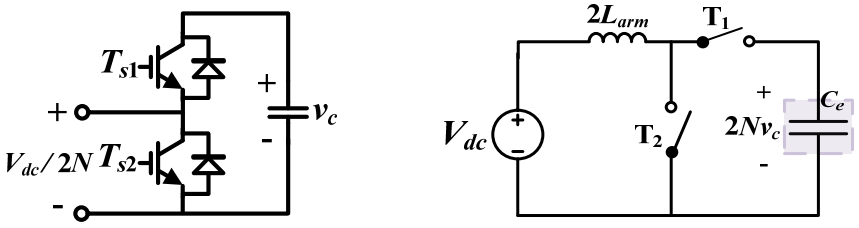
Figure 5-7 presents the operating principle of the feedforward control. Figure 5-7(a) and (b) show a submodule circuit and the equivalent circuit of the capacitor charging loop respectively, where T_1

represents the series combination of the upper switch (T_{s1}) in all SMs and T_2 represents that of the lower switch (T_{s2}). During the charging period, the MMC can be regarded as a boost converter. If T_2 is on (i.e. the lower switches of all SMs are on), the energy from the dc bus is stored in the arm inductors. If T_2 is off and T_1 is on, the stored energy together with the dc bus will charge the capacitors.

Assuming the capacitor voltages are well balanced, the duty cycle of upper device T_{s1} and lower device T_{s2} in each SM can be obtained as

$$\begin{aligned} d(T_2) &= 1 - V_{dc} / 2Nv_{c_ref} \\ d(T_1) &= V_{dc} / 2Nv_{c_ref} \\ v_{c_ref} &= V_{dc} / 2N + V_{ramp}\Delta t \end{aligned} \tag{5 - 14}$$

If more SMs are incorporated, only the number of SMs (N) in the feedforward control needs to be modified. Moreover, compared to the averaging capacitor voltage control, V_{ramp} here can be adjusted more freely, and no stability issue is involved.



(a) (b)

Figure 5-7. Equivalent circuit of capacitor charging loop in (a) a submodule of MMC, and (b) a phase unit of MMC inverter.

With this proposed capacitor charging scheme, the capacitor voltage can be regulated to any desired values higher than $V_{dc}/2N$ by simply adjusting capacitor voltage reference v_{c_ref}. Thus, redundant SMs in the MMC will not lead to any extra control complexity. Because of the feedback regulation, the charging current becomes zero automatically after the capacitor charging process is finished. Therefore, no fast transition between startup and normal operation is required. Furthermore, with the same modulation wave

generation and capacitor voltage balancing control, only voltage references (m_c and m_s) need to be updated at the start of normal operation, which enables an easy and smooth transition.

5.3 Case Study

5.3.1 System Parameters

A three phase BTB-MMC system with the controllers designed in Section III is established in Matlab/Simulink. The main system parameters are listed in Table 5-1. In this work, the sine-triangle modulation presented in [138] [139] is adopted and combined with the widely used $N + 1$ level phase shift PWM (PS-PWM) modulation scheme. Through comparison of saddle-shaped modulation waves generated by the sine-triangle modulation and phase-shifted carriers produced by the PS-PWM, PWM signals for each SM can be easily achieved.

Table 5-1. Main circuit parameters of MMC-HVDC.

Parameters	Values	Parameters	Values
AC voltage v_{s1}	10 kV	Carrier frequency	2 kHz
Y/Δ transformer ratio	10 kV / 2.5 kV	Rectifier side reactive power	0 MVar
Voltage frequency	60 Hz	Inverter side active power	0.5 MW
DC Link voltage V_{dc}	5 kV	Inverter side reactive power	0 MVar
No. of sub-modules in each arm N	4	Cable length	50 km
Submodule capacitance	2000 μF	Resistance per unit length	13.9 mΩ / km
AC side inductance L_{AC1}, L_{AC2}	4.775 mH (0.144 pu)	Inductance per unit length	159 μH / km
ESR of AC inductors R_{AC}	0.09 Ω	Capacitance per unit length	0.231 μF / km
Arm inductance L_{arm}	5.635 mH (0.17 pu)	ESR of arm inductors R_{arm}	0.106 Ω

Focusing on the modelling and control design of MMC inverters during the startup process, this work does not keep the averaging capacitor voltage control under normal conditions. Instead, proportional resonant (PR) based circulating current control (resonant at double line frequency) is adopted for zero

steady state error, while capacitor voltages are regulated by sorting and balancing control and dc voltage control. The capacitor voltage sorting and balancing control with $V_{c_margin} = 0.05V_{dc} / N$ (62.5 V) works all the time.

5.3.2 BTB-MMC System Connecting Two Active Terminals

In applications such as HVDC transmission systems, the BTB-MMC system connects to active terminals at both converter stations, as illustrated in Figure 5-8. With active power support capability from the grid, each converter station operates as a rectifier separately during the startup period. The converter station connects together after the dc voltage is built up. Based on the developed design criteria, 7 Ω current limiting resistors R_{st1} and R_{st2} are installed in AC sides to limit the inrush peak current below 240 A ($1.5I_{rated}$). Contactors KM1 and KM2 are employed to bypass these resistors after the uncontrolled pre-charge stage.

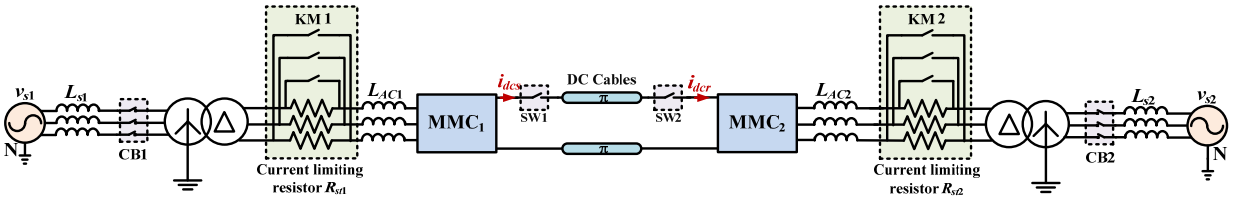


Figure 5-8. BTB-MMC system with two active terminals.

If well regulated, the dc voltage will track its reference and ramp up. Meanwhile, capacitors get gradually charged, and no capacitor voltage charging control is needed. When the dc voltages at the two terminals both rise to the reference value, switches SW1 and SW2 will close and connect the two converter stations together. Meanwhile, MMC_2 changes from rectifier mode to inverter mode.

Figure 5-9 shows the selected simulation results of the rectifier station with two active terminals, and SVM scheme is applied. The whole startup process can be divided into four stages.

Stage I [0 ~ 0.08 s]: When AC circuit breakers CB1 and CB2 are closed at t = 0 s, the inrush current is suppressed to 235 A by the current limiting resistors (Figure 5-9 (a)). Three phase arm currents are given

in Figure 5-9 (b) to (d) with a magnitude of about 160 A. The three phase capacitor voltages v_{cj_rec} (j = a, b, c) gradually increase due to the charging of arm currents, resulting in a rectifier side dc voltage of Nv_{c_rec} (Figure 5-9 (e) to (h)).

Stage II [0.08 s ~ 0.15 s]: At t = 0.08 s, contactors KM1 and KM2 are closed and the current limiting resistors are bypassed. This sudden voltage drop of the resistors induces a short period of inrush phase and arm currents. The resistor voltage drop also results in a further increase of the capacitor voltages to 866 V. The dc voltage is 3464 V at the end of this stage, which is slightly lower than $\sqrt{6}V_{ph}$ (3535 V) due to the voltage drop on diodes, ESR of inductors, and dc cables.

Stage III [0.15 s ~ 0.35 s]: When the dc voltage control is activated at t = 0.15 s, the phase and arm current gradually increase to charge the SM capacitors, and the magnitude of the charging current is directly related to the ramp rate of the dc voltage reference. The dc voltage control, together with the capacitor voltage balancing control, guarantees smooth increase of the dc voltage and balanced submodule capacitor voltages.

Stage IV [0.35 s ~]: After dc voltages of the two stations reach their steady state, dc switches SW1 and SW2 are closed at t = 0.35 s to connect the two stations together. Meanwhile, MMC_2 starts to supply active and reactive power for grid v_{s2}. To maintain the dc voltage, the rectifier side phase and arm currents increase accordingly during the inverter output power ramp. During 0.4 s to 0.5 s, a dc voltage drop appears due to the relatively slow dynamic response of the dc voltage control. This phenomenon can be mitigated by a larger control bandwidth of the voltage loop, at the cost of lower stability margin.

The corresponding simulation waveforms in the inverter station are similar to the rectifier side, and are not repeated here.

Figure 5-10 gives the duty cycle of the rectifier and inverter stations. Since the dc voltage is a little lower than $\sqrt{6}V_{ph}$, a saturated duty cycle is observed in both stations when the dc voltage control is activated at 0.15 s. As highlighted in the dashed green block, this situation lasts for 0.012 s until the dc voltage is high enough for normal operation.

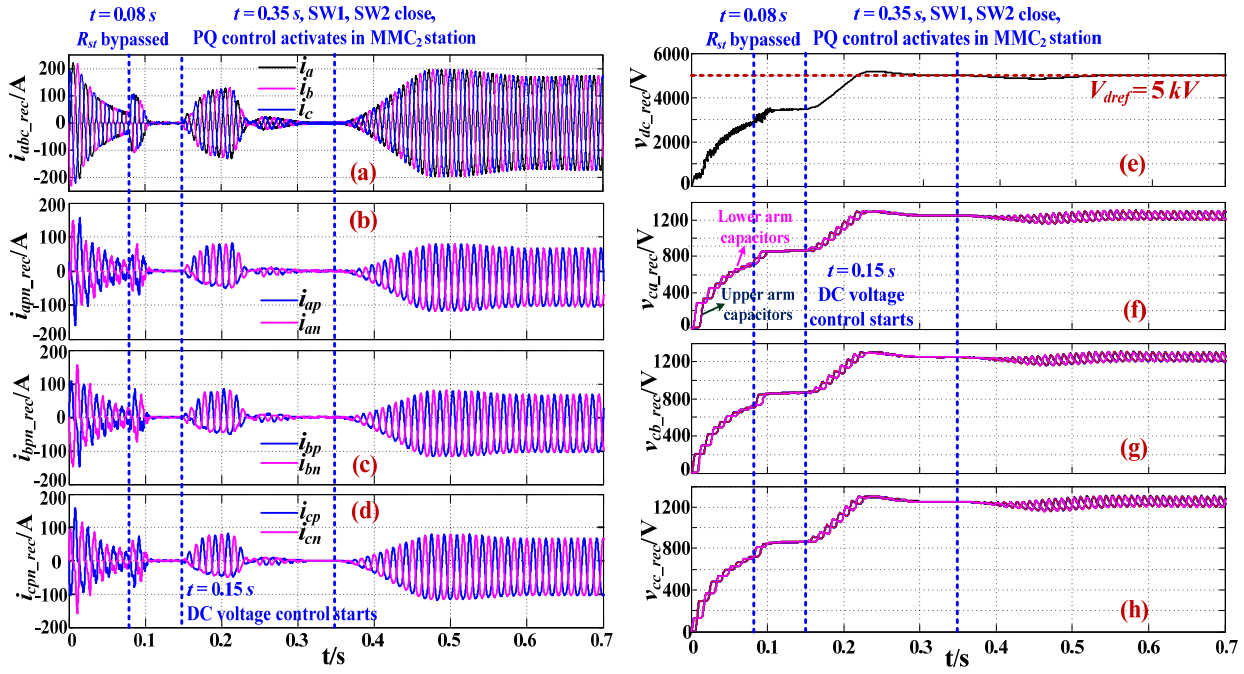
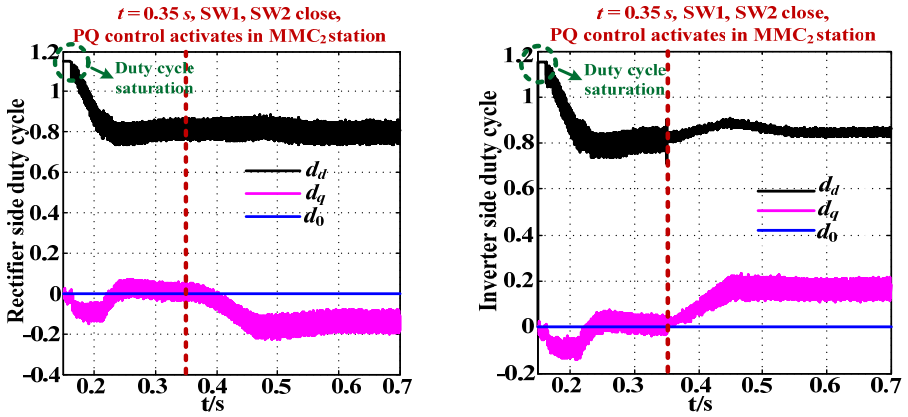


Figure 5-9. Selected simulation results of the rectifier station with two active terminals, (a) phase current, (b) arm current in phase A, (c) arm current in phase B, (d) arm current in phase C, (e) dc voltage, (f) capacitor voltages in phase A, (g) capacitor voltages in phase B, (h) capacitor voltages in phase C.



(a) (b)

Figure 5-10. Duty cycle of (a) rectifier, (b) inverter with two active terminals when SVM is adopted.

5.3.3 BTB-MMC System Supplying Passive Loads

Although Figure 5-11 shows the configuration of a BTB-MMC system with passive loads, in real applications this load may also include windfarms, motors and converters during black start. Without an active terminal, SM capacitors in the MMC_2 station can only be charged through the dc bus.

A. With Only Averaging Capacitor Voltage Control

Figure 5-12 shows the converter side phase current (i_{abc}), arm current (i_{apn}), dc voltage (v_{dc}) and phase A capacitor voltage (v_{ca}) of both converter stations, when only averaging capacitor voltage control is adopted. The subscript "_rec" and "_inv" represent waveforms in rectifier (MMC_1) and inverter (MMC_2) station, respectively. The ramp time of capacitor voltage reference t_{ramp} is set to 0.1 s. The main startup process is described as follows: (1) At $t = 0$ s, CB1 closes and the pre-charge period starts; (2) At $t_1 = 0.08$ s, pre-charge stage completes, and rectifier side current limiting resistors R_{st} is bypassed; (3) At $t_2 = 0.15$ s, dc voltage control starts; (4) At $t_3 = 0.35$ s, dc voltage stays stable in its rated value, and averaging capacitor voltage control is activated in the MMC_2 station; (5) At $t_4 = 3$ s, the average capacitor voltage of MMC_2 reaches its rated value (V_{dc} / N), and CB2 closes to enable power regulation.

During the uncontrolled pre-charge period, the rectifier side capacitors are charged first until the anti-paralleled diodes become reverse biased, and then SM capacitors in the inverter station are charged through dc cables (Figure 5-12(a)). After 0.15 s, the dc voltage control, together with the capacitor voltage balancing control, enables smooth increase of the dc voltage and balanced capacitor voltages in the MMC_1 station.

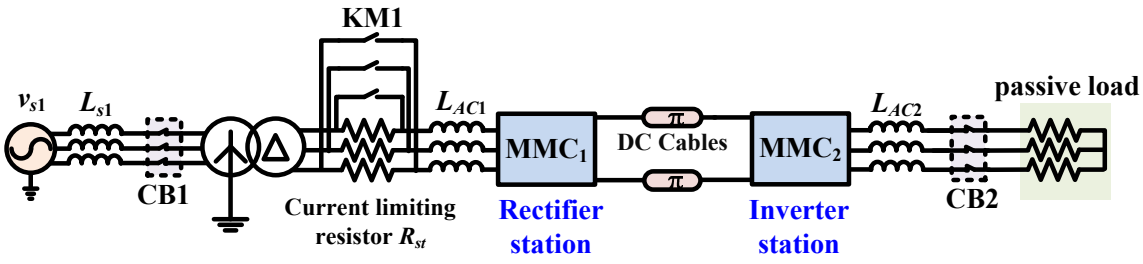


Figure 5-11. BTB-MMC system supplying resistive load.

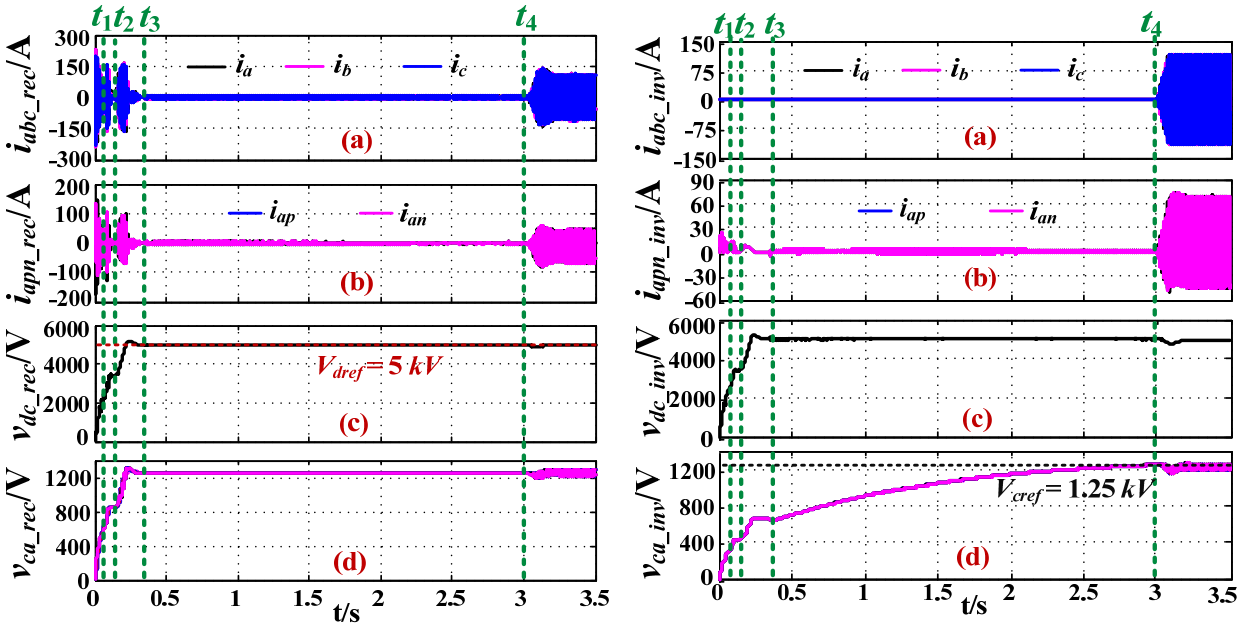


Figure 5-12. Selected simulation results of (a) phase current, (b) arm current in phase A, (c) dc voltage, (d) capacitor voltages in phase A in MMC_1 (top) and MMC_2 (bottom) station with only averaging capacitor voltage control and $N = 4$.

When the averaging capacitor voltage control is activated in the inverter station at t_3 = 0.35 s, the three-phase capacitor voltages of MMC_2 start to increase slowly and synchronously (Figure 5-12 (b)). Although t_{ramp} is set to be 0.1 s, it takes 2.65 s for the average capacitor voltage of MMC_2 to reach its rated value because of the poor dynamic response of the capacitor voltage and circulating current regulation. Having only passive ac terminal, MMC_2 needs to absorb active power through the dc bus to charge its SM capacitors, which induces an apparent high frequency ripple in dc bus. With active and reactive power control disabled (v_{sref} = 0), no inverter side phase current i_{abc_inv} is generated during this period. After the three phase capacitor voltages of MMC_2 are all charged to V_{dc} / N at t_4 = 3 s, phase current i_{abc_inv} starts increasing until new balances are achieved between power generation and absorption. During the transition, no abrupt increase is observed in both arm and phase currents.

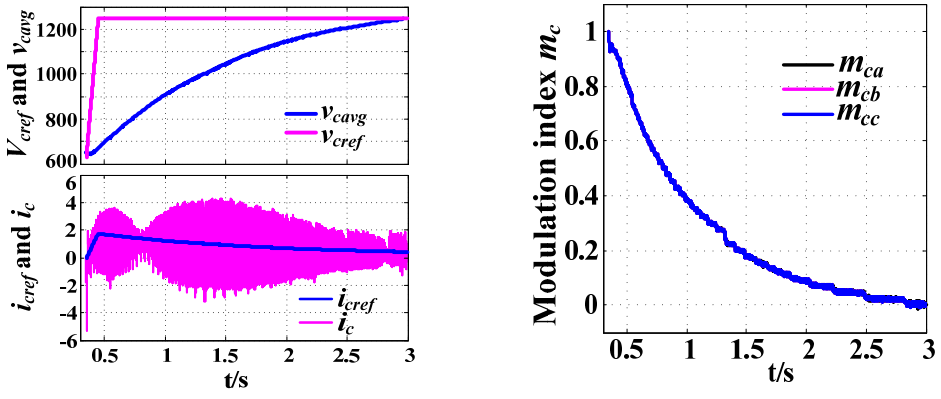
Figure 5-13 illustrates the performance of the averaging capacitor voltage control. As can be observed, the average capacitor voltage $v_{cavg}\left(\sum_1^N \frac{v_{cj}}{N}\right)$ is far below its reference v_{c_ref}. Despite high switching ripples,

the charging current is capable of tracking its reference. Moreover, the three phase modulation waves generated by the capacitor voltage control in Figure 5-13(b) are completely overlapped, indicating a synchronous capacitor charging among three phases. The MMC inverter operates as three paralleled boost converters, and the arm inductor serves as the boost inductor during the startup period. Therefore, the high switching ripple is observed in arm inductor current (i.e., circulating current) during the charging and discharging processes.

In simulation, the detected arm currents are directly used for circulating current control, and high switching ripple is found in both circulating current i_c and modulation index m_c (Figure 5-13). The switching ripple in i_c can be suppressed by larger arm inductance and/or higher switching frequency, at the cost of higher volume and/or switching losses. Switching ripple in the m_c, however, can be easily mitigated by filtering of the arm current before they are used for the circulating current control.

B. With Only Capacitor Voltage Feedforward Control

The selected simulation results of MMC_1 and MMC_2 stations with only capacitor voltage feedforward control are given in Figure 5-14. The system parameters and startup procedure are the same as the previous case except $t_4 = 0.46$ s. After pre-charge and dc voltage regulation stages, the proposed capacitor voltage feedforward control is activated at $t_3 = 0.35$ s in the MMC_2 station.



(a) (b)

Figure 5-13. (a) Average capacitor voltage, circulating current and their references, (b) Modulation index m_c, with only average capacitor voltage control and $N = 4$.

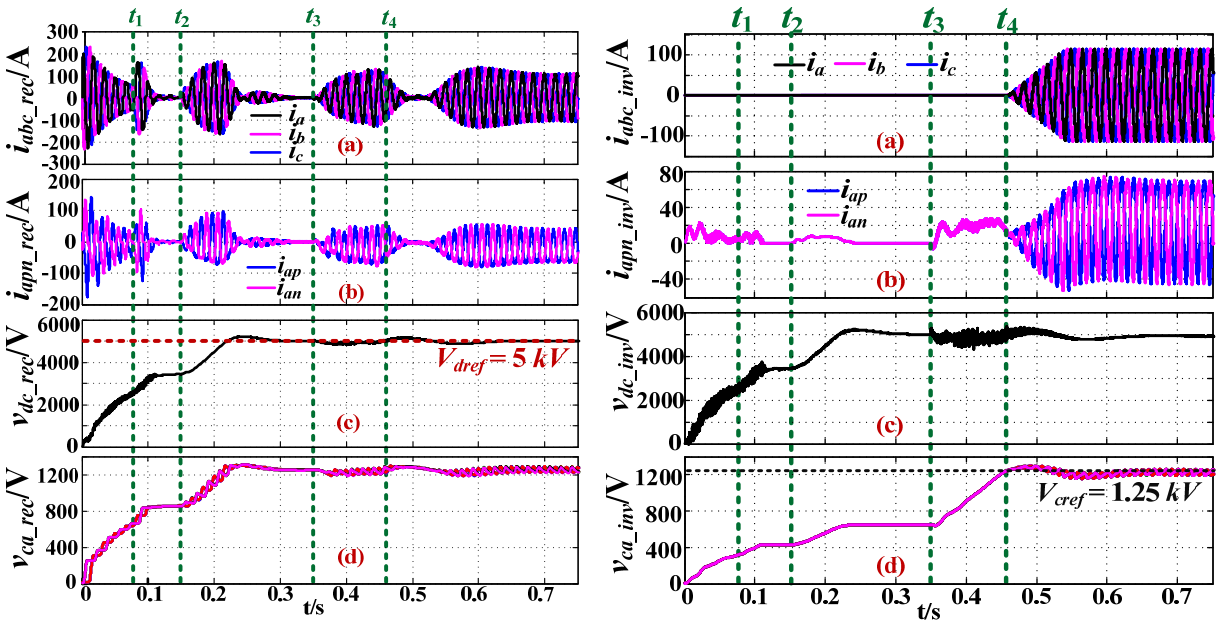
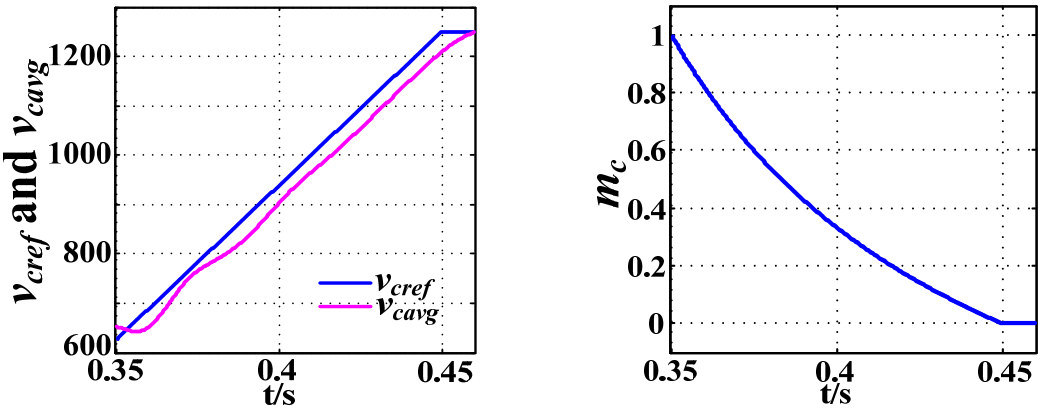


Figure 5-14. Selected simulation results of (a) phase current, (b) arm current in phase A, (c) dc voltage, (d) capacitor voltages in phase A in MMC_1 (top) and MMC_2 (bottom) station with only capacitor voltage feedforward control and $N = 4$.



(a) (b)

Figure 5-15. (a) Average capacitor voltage and its reference, (b) Modulation index m_c, with only capacitor voltage feedforward control and $N = 4$.

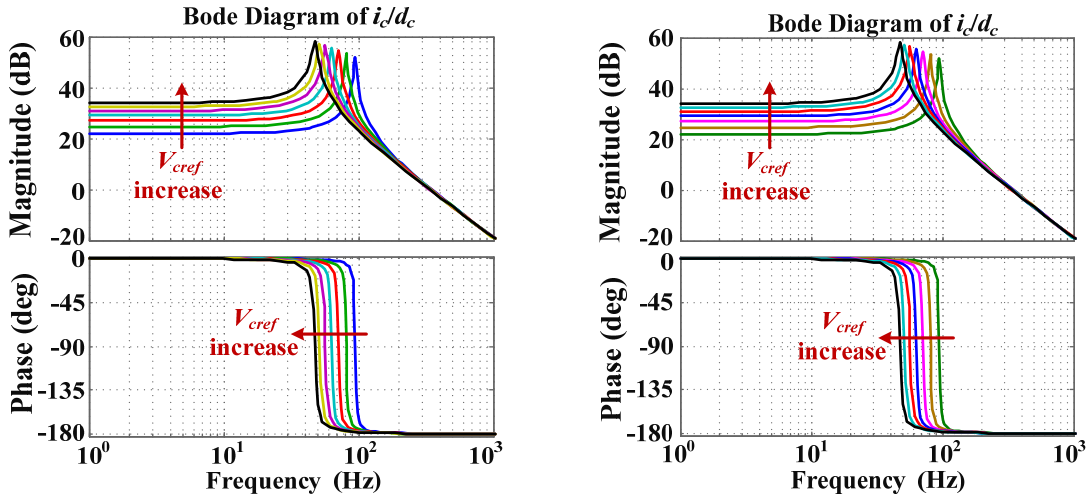
Compared to Figure 5-12, the capacitor voltages of MMC_2 reach their rated value in only 0.11 s (Figure 5-14 (b)). By adjusting t_{ramp}, the charging time can be easily changed without affecting system stability. Figure 5-15 illustrates the average capacitor voltage and modulation index m_c. With the capacitor voltage feedforward control, the maximum error between the average capacitor voltage and its reference is below 40 V. Moreover, acting as an open-loop regulation, this control enables a smoother duty cycle.

C. With Combined Control Schemes and Different Submodule Numbers per Arm

To further verify the modelling and control design (averaging capacitor voltage and feedforward control), three phase MMC inverter models with 10 and 20 SMs per arm are built in Matlab/Simulink. The SM capacitance is adjusted accordingly (i.e. C_{sub} / N = constant) to maintain the ratio of capacitor voltage ripple over dc voltage. As shown in Figure 5-16, if C_{sub} / N keeps constant, the variation of N will not affect small signal models of the capacitor charging loop, and the same controller is applied to MMC with N = 4, 10 and 20.

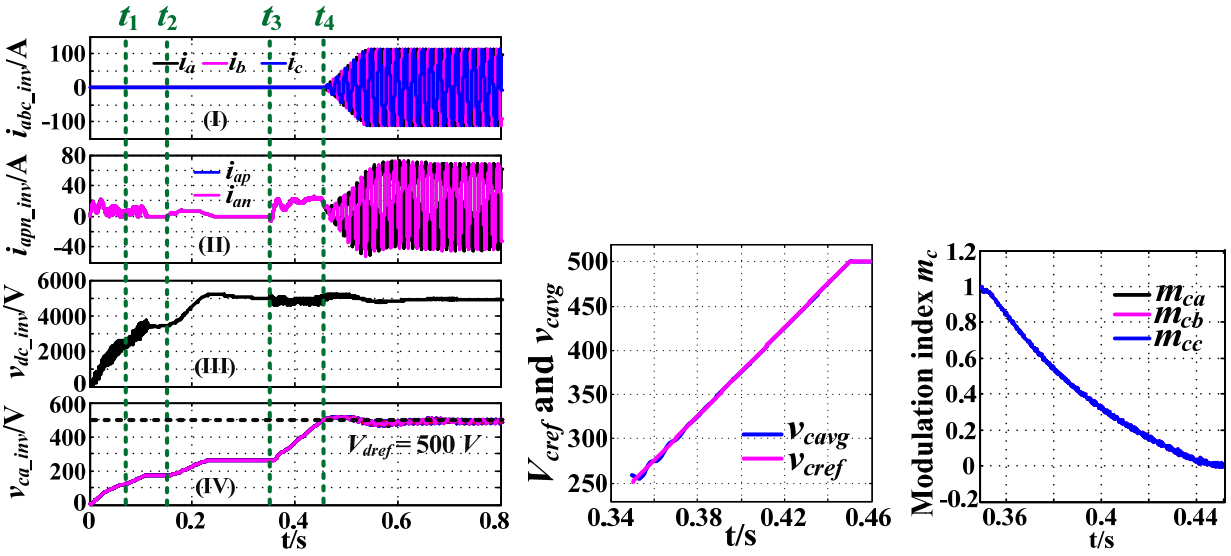
Figure 5-17 and Figure 5-18 give the simulation results where each arm has 10 SMs, t_{ramp} = 0.1 s and 20 SMs, t_{ramp} = 0.5 s, respectively. Focusing on the performance of capacitor charging control, only MMC2 side waveforms are given here. With the designed capacitor charging control, capacitors in all three phases can be charged synchronously, and the average capacitor voltage can track its reference very well. Since the feedforward control proposed in this paper dominates the capacitor voltage regulation, the same control parameters are used in both cases, without causing any stability issues.

In summary, although more SMs per arm will result in higher implementation complexity of the capacitor voltage balancing control and PWM signal generation, the variation of N does not affect the startup control performance. In addition, as long as C_{sub} / N and capacitor voltage reference ramp time t_{ramp} keep constant, the designed capacitor charging control parameters will be applicable to a MMC inverter regardless of the number of SMs used per arm.



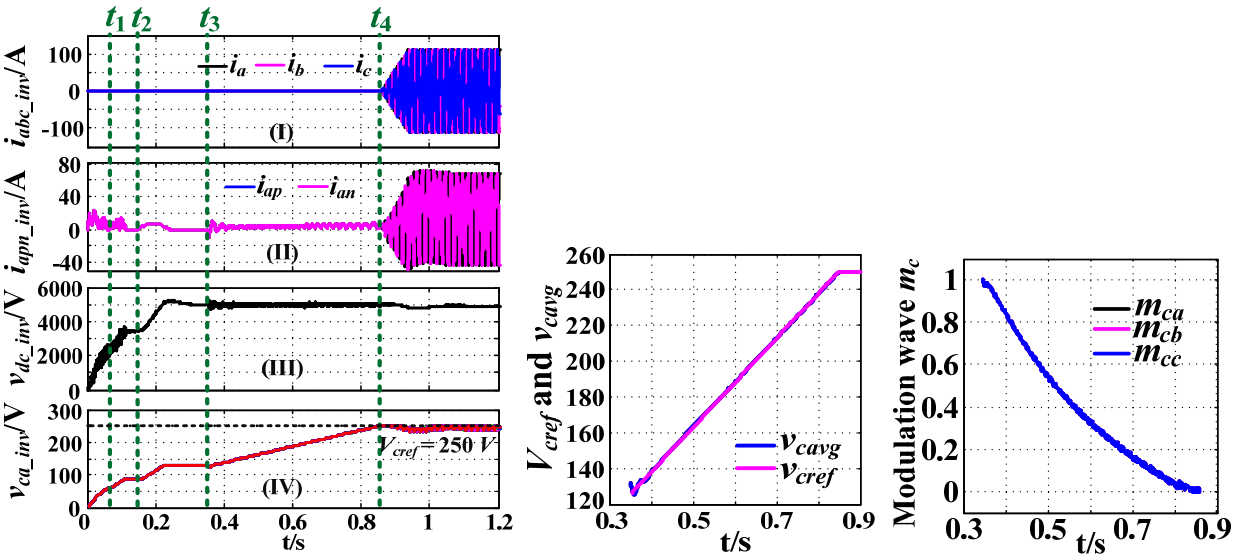
(a) $N = 10$, $C_{sub} = 5000$ μF (b) $N = 20$, $C_{sub} = 10000$ μF

Figure 5-16. Open-loop bode plot of $\tilde{i}_c$ to $\tilde{d}_c$ with different number of SMs per arm.



(a) (b) (c)

Figure 5-17. Selected simulation results in MMC_2 station, (a): (I) phase current, (II) arm current in phase A, (III) dc voltage, (IV) capacitor voltages in phase A, (b) average capacitor voltage and its reference, and (c) modulation index m_c with capacitor charging control and $N = 10$.



(a) (b) (c)

Figure 5-18. Selected simulation results in MMC_2 station, (a): (I) phase current, (II) arm current in phase A, (III) dc voltage, (IV) capacitor voltages in phase A, (b) average capacitor voltage and its reference, and (c) modulation index m_c with capacitor charging control and $N = 20$.

5.4 Experimental Verification

5.4.1 Experimental System Configuration and Parameters

To verify the theoretical analysis and proposed control scheme, a scaled-down three-phase MMC inverter was built and tested, as shown in Figure 3-6. The configuration of the experimental system is illustrated in Figure 5-19, with its main circuit parameters given in Table 3-2. In order to guarantee balanced capacitor voltages, the sorting and balancing control with $V_{c_margin} = 0.05V_{dc} / N$ (3.75 V) works all the time.

5.4.2 Experimental Results of a Modular Multilevel Rectifier

Figure 5-20 shows the selected experimental results of a MMC rectifier after the uncontrolled pre-charge stage, where the same modulation scheme, i. e., combination of sine-triangle and PS-PWM modulation schemes is applied.

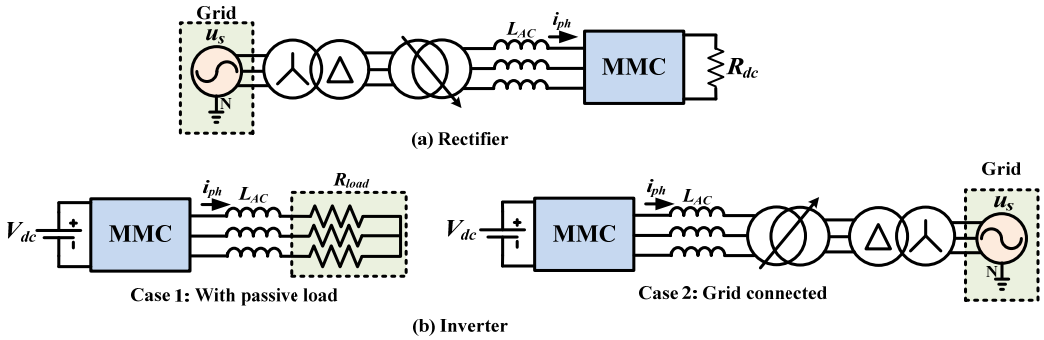


Figure 5-19. Configurations of the experimental system.

In the experiments, a dc resistance of 30 Ω is applied, and the parasitic resistances induced by cables, filtering inductors and other components are also included in the pre-charge loop. After the pre-charge stage, the dc voltage has a minimum value of 85.9 V and an average value of 92.1 V (Figure 5-20 (c)).

When the dc voltage control is manually activated, the difference between dc voltage and ac line-to-line voltage applies on ac and arm inductors, leading to an inrush current with peak value of 13 A. Because of this inrush current, an abrupt increase is observed in the dc voltage, which leads to a short saturated duty cycle and uncontrolled phase current, as illustrated in Figure 5-20 (d). After the duty cycle m_s is no longer saturated, the dc voltage tracks its reference precisely, and phase current gradually increases to charge the SM capacitors. As can be observed, smooth and linearly increasing dc and capacitor voltages are achieved without any additional capacitor charging control.

5.4.3 Experimental Results with a Modular Multilevel Inverter

A. With Resistive Load

Figure 5-21 shows experimental results of a MMC inverter with a resistive load (R_{load} = 5 Ω) after the uncontrolled pre-charge period. Both feedforward and averaging capacitor voltage control are applied, and the capacitor voltage reference ramp time (t_{ramp}) is set to 1 s. At the beginning, capacitor voltages are close to 37.5 V (V_{dc} / 2N), and no current flows into the MMC arms. At t_1, capacitor voltages start to ramp linearly under the regulation of the capacitor charging control, until their average value reaches V_{dc} / N (= 75 V) at t_2 (Figure 5-21 (a) and (f)).

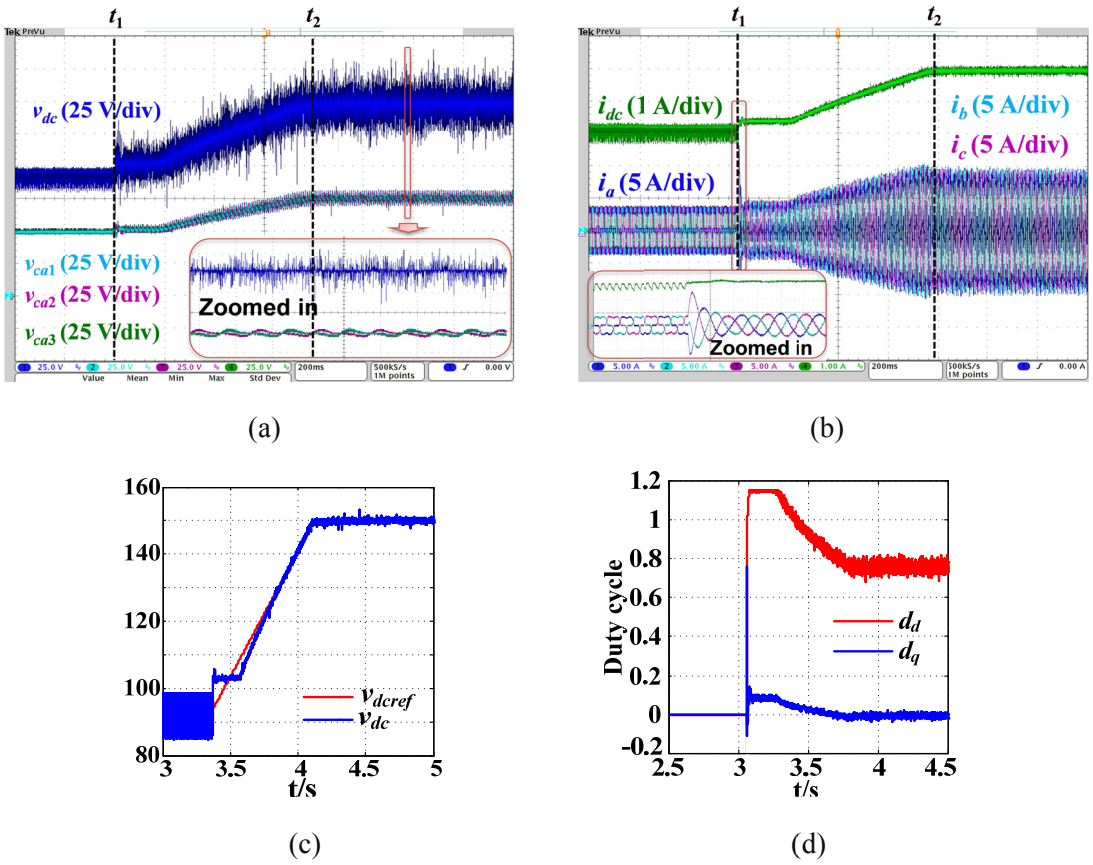


Figure 5-20. Experimental results of MMC inverter with passive load, (a) dc voltage and capacitor voltage in phase B, (b) dc and phase current, (c) arm current in phase B, (d) arm current in phase C, (e) dc voltage and its reference, (f) duty cycle m_s in dq axis.

Capacitor voltage in phase C is similar to that in phase A and B, and is not duplicated here. The charging currents during this stage are lower than 5 A, and no phase current is generated (Figure 5-21 (b)). After t_2, the capacitor charging control is deactivated (or converted to circulating current control). Meanwhile the power reference starts to increase, and phase current ramps up to its rated value ($I_d = I_{pk} =$ 10 A). The arm currents and capacitor voltage ripple increase correspondingly to finalize the startup process, as shown in Figure 5-21 (a) and (b). As expected, the average capacitor voltage ($v_c^{\Sigma}/2N$) and circulating current can quickly track their references without obvious difference (Figure 5-21 (c) and (d)). Moreover, modulation index m_c generated by the capacitor charging control smoothly reduces from 1 to zero with increased capacitor voltages (Figure 5-21 (e)).

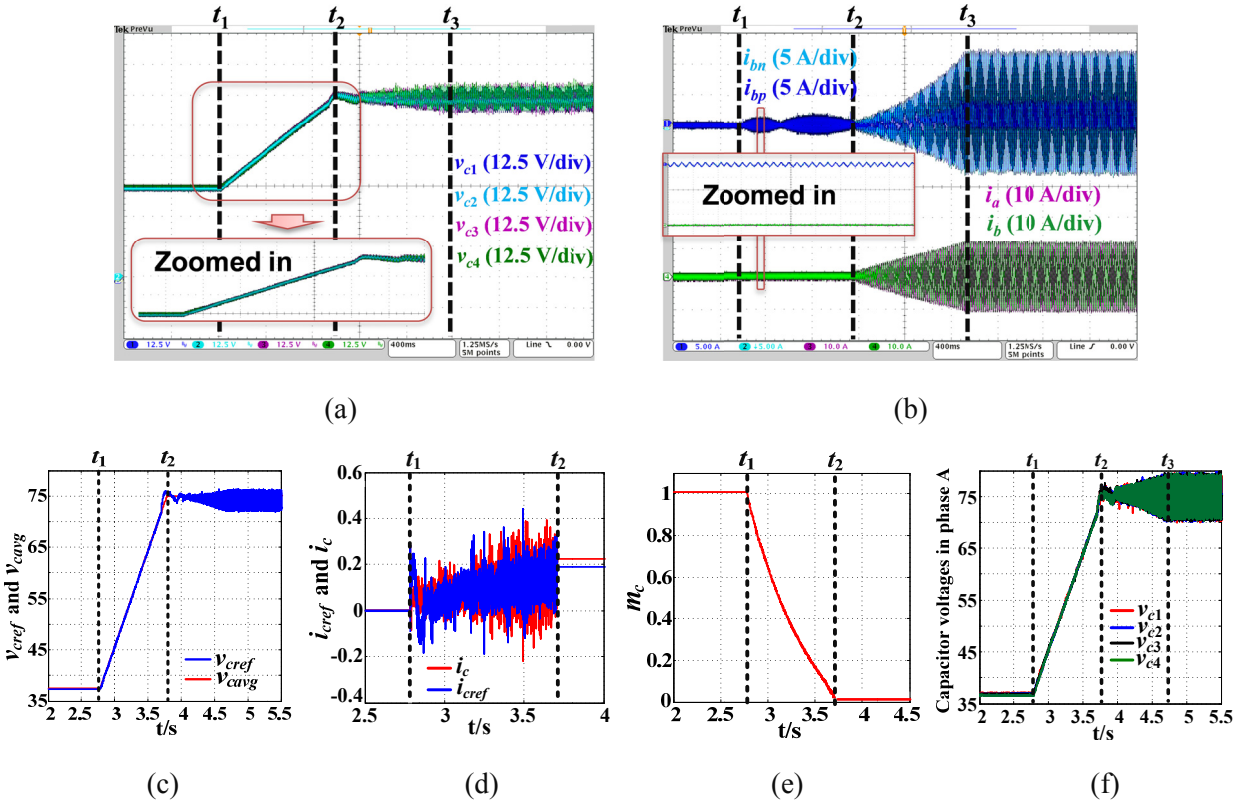


Figure 5-21. Experimental results with passive load, (a) capacitor voltage in phase B, (b) arm current in phase B and phase current, (c) average capacitor voltage and its reference, (d) circulating current and its reference in phase B, (e) modulation index m_c, (f) capacitor voltage in phase A.

B. Grid Connected

The system configuration with grid connection is shown in Figure 5-19(b), and the same capacitor charging control is adopted. To prevent inrush phase current, the grid should be disconnected before SM capacitors are fully charged. In this work, the zero grid side voltage is realized by a variac. In addition, the phase locked loop (PLL) is active from t_1 for grid synchronization.

Similar to the case with resistive load, capacitors can be charged linearly with high accuracy and a charging current lower than 5 A (Figure 5-22(a) and (f)). However, caused by the residual voltage of the variac (~ 1 V), phase current with a magnitude around 1 A is observed during the startup process (Figure 5-22 (b)). Different from a MMC inverter with resistive load, power regulation cannot be activated

immediately after the capacitor charging control completes. Instead, from t_2 to t_3, the ac side voltage starts to be manually increased until it reaches the rated value at t_3. During this period, the active power reference is set to zero to avoid large ac and arm current.

5.5 Summary

This chapter deals with a comprehensive analysis and control design of a BTB-MMC transmission system during the startup process. The key points in this chapter are summarized as follows:

(1) The charging loops of MMC rectifier and inverter during the uncontrolled pre-charge stage are analyzed. It is found that no additional capacitor charging control is required for a MMC rectifier, while such control becomes necessary when a MMC operates as an inverter.

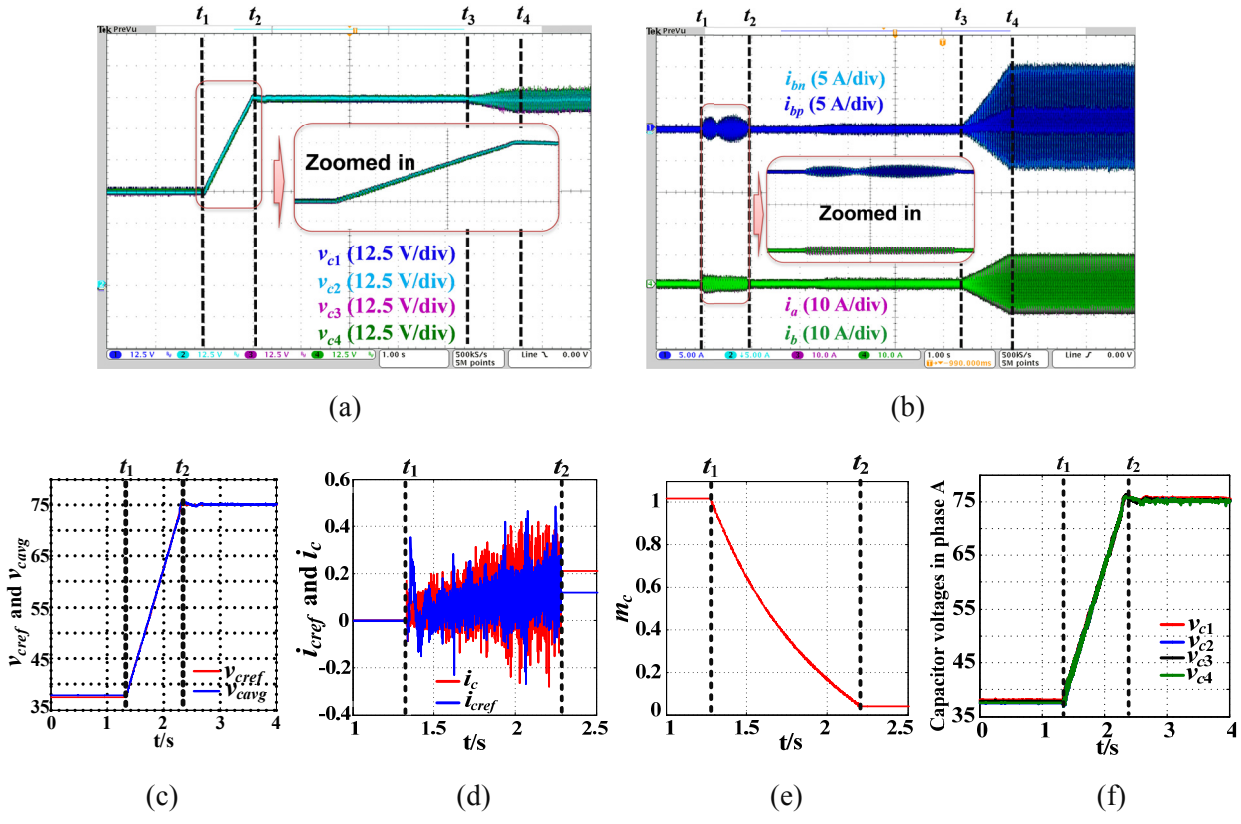


Figure 5-22. Experimental results when grid connected, (a) capacitor voltage in phase B, (b) arm current in phase B and phase current, (c) average capacitor voltage and its reference, (d) circulating current and its reference in phase B, (e) modulation index m_c, (f) capacitor voltage in phase A.

(2) The transfer functions of $\tilde{i}_c / \tilde{d}_c$ and $\tilde{v}_c / \tilde{i}_c$ of the averaging capacitor voltage control are first derived during startup process according to the unique capacitor charging loops and zero fundamental frequency modulation index (i.e. $v_{sref} = 0$).

(3) Based on the derived transfer functions, the detailed design considerations of the averaging capacitor voltage control are presented. With the theoretically designed control parameters, system stability can be guaranteed during the variation of operation conditions as well as system parameters.

(4) Through the derived model, the limiting factor of the dynamic response of the averaging capacitor voltage control is identified. It is shown that the resonance between arm inductance and SM capacitors will constrain the overall bandwidth of capacitor voltage charging loop, which greatly impede the startup process and fast recovery of MMC station from blackout conditions.

(5) Due to this limiting factor, the dynamic response of the averaging capacitor voltage control is unsatisfactory. To address this issue, a capacitor voltage feedforward control is proposed in this work, which can operate together with the averaging control to achieve fast dynamic response without compromising system stability margin and implementation complexity.

(6) Detailed startup procedures of a BTB-MMC system with passive loads are presented and verified by the simulation results. Experimental results from scaled-down three-phase MMC further demonstrate the effectiveness of the proposed capacitor charging control scheme.

6 Cascaded Droop Control for DC Voltage Regulation in Multi-terminal HVDC System under SLG Fault

This chapter introduces a cascaded droop control scheme for a multi-terminal HVDC (MTDC) system, which helps each converter station achieve autonomous power adjustment during onshore station side ac faults. The control performance is evaluated under various operation conditions and droop parameters selection is analyzed based on the derived power flow calculation. Simulation results from a four-terminal HVDC system generated with Matlab/Simulink and experimental results from a scaled down prototype are provided to support the theoretical analysis and proposed control schemes.

6.1 Four-Terminal HVDC Prototype

The Cape Wind Project is an offshore wind farm, locating on the Horseshoe Shoal in Nantucket Sound off Cape Cod, Massachusetts, United States [140]. It plans to generate 1,500 gigawatt hours of electricity per year with mild environmental impact [141]. To study the feasibility of offshore wind energy transmission in this cape wind project, a 4-terminal HVDC system is selected. It assumes two offshore wind farms in the Cape Cod Bay area, and their generated electricity will be transferred to load centers in the NPCC system through a MTDC network, as illustrated in Figure 6-1.

According to [40], the four terminals of MTDC system can be connected in the form of radial, ring and meshed, in which the latter two are preferred because of their high control flexibility and lower wind energy curtailment. With these topologies, dc breaker and/or converter with fault tolerant capability are required to prevent the system from damage during dc faults. This requirement, however, will introduce high cost to the system due to the unavailability of commercial HVDC dc breakers. To avoid this, the point-to-point HVDC (PTP-HVDC) topology can be employed. By shutting down the single PTP-HVDC line which suffers a dc fault, power transfer of the rest system will not be interrupted and a dc breaker is not needed. Therefore, the ring, meshed and point to point topologies are considered as three potential dc grid candidates, as shown in Figure 6-2.

The cost comparison among these three candidates is conducted, where three converters are used in point-to-point topology (Figure 6-2(a)) to achieve the same functionality as the meshed grid (Figure 6-2(c)). To simplify the analysis, only the main components (converter, dc breaker and dc cable) are considered, and each topology is designed based on the same operation specifications:

(1) Wind farms can only generate active power and onshore converters can only absorb active power
(2) Active power generated by the windfarms cannot exceed the absorption capacity of onshore converters to avoid dc overvoltage.
(3) Under dc fault conditions, the faulted converter stations and dc lines should be isolated and the system maintains power transfer, but with a specific percentage of wind power curtailment

Figure 6-3 shows the cost comparison when different wind power curtailment requirements is applied in (3). The unit costs of converter, dc cable and dc breaker are obtained from [115], using million Euros (€m) as unit. In a point-to-point topology, although the dc breaker is not necessary, three converters are needed in each terminal to meet the requirements, thus introducing a generally high cost. On the other hand, due to the dc cables and breakers with lower current rating, a better cost-benefit performance is achieved for the ring topology when the wind power curtailment is high; otherwise the meshed topology becomes a more cost-effective option. In this work, the wind energy is automatically reduced for dc overvoltage suppression during fault conditions, which normally demands for a high wind power curtailment under serious fault conditions, and thus the ring topology is selected for the further study and hardware implementation.

System configuration of the simulation model and scaled down hardware prototype are given in Figure 6-4, in which WFs in the real MTDC system are emulated by two converters. The power generated by the WF emulator will be transferred to the onshore grids through both MTDC network, offshore and onshore converters. Under normal conditions, the onshore converter I regulates dc voltage; onshore converter II, Wind farm emulator I and II are responsible for active and reactive power generation; and offshore converter I and II are assigned to build ac grids for wind turbines by controlling magnitude and frequency of voltages in PCC1 and PCC2.

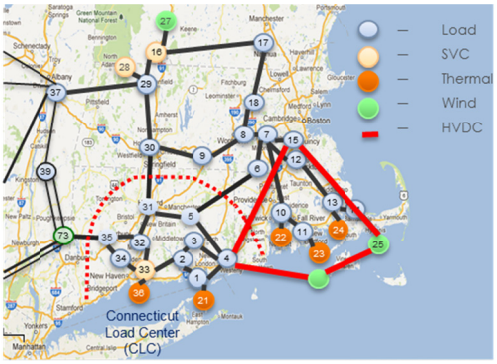


Figure 6-1. Four -terminal HVDC in the NPCC system.

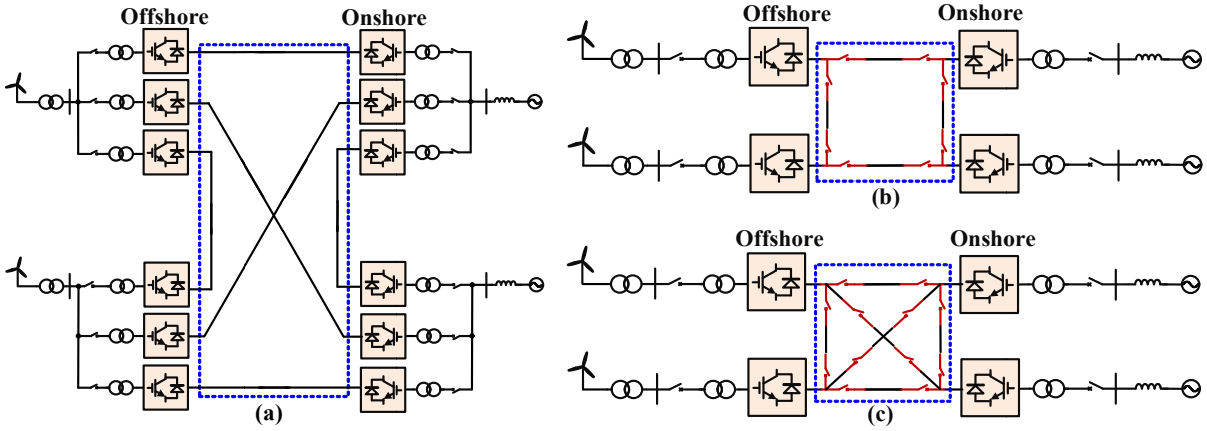
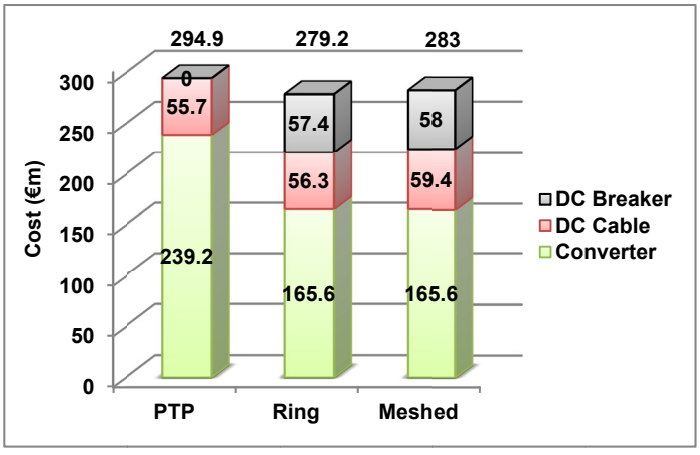
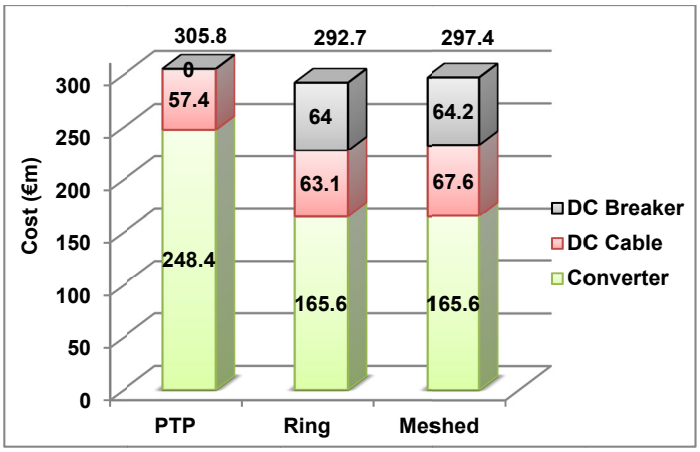


Figure 6-2. Dc grid topologies for comparison: (a) point-to-point, (b) ring, and (c) meshed.

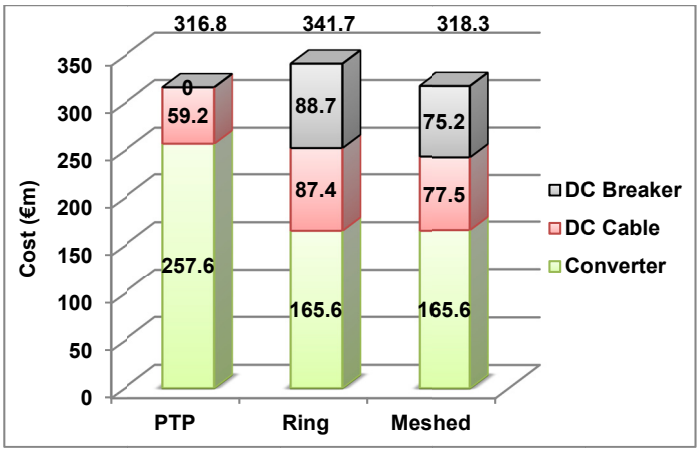


(a) With 25 % power transfer

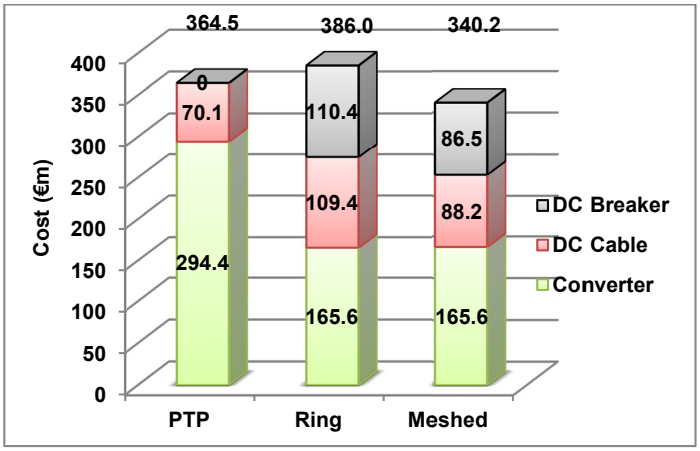
Figure 6-3. Cost comparisons with different percentages of wind power transfer requirement after dc short circuit fault.



(b) With 50 % power transfer



(c) With 75 % power transfer



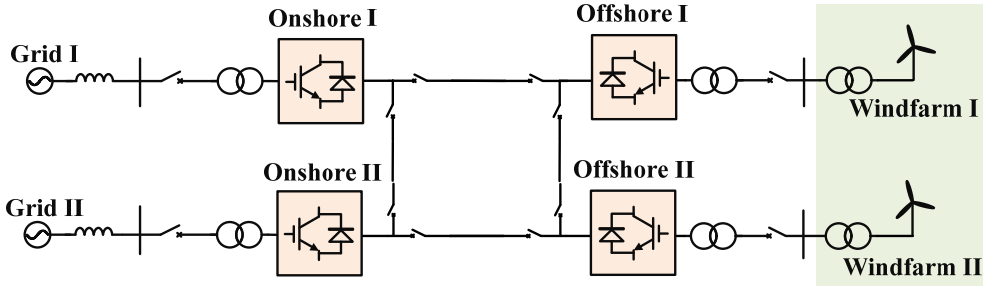
(d) With 100 % power transfer

Figure 6-3. Cost comparisons with different percentages of wind power transfer requirement after dc short circuit fault. Continued.

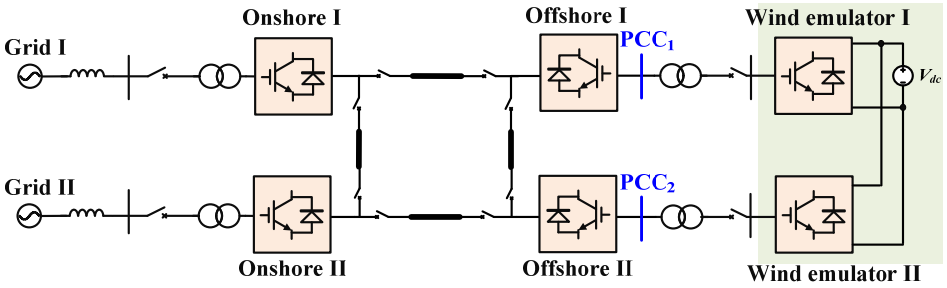
Figure 6-5 gives the control diagram of ac voltage regulation in offshore converters. The control scheme is implemented under dq coordination, and a fixed frequency is used for dq axis building. Without an ac capacitor, a single ac voltage control loop is applied, where duty cycle d_{dq} is generated directly from voltage error and no phase current regulation is involved. For better dynamic response, an inductor voltage feedforward item (Ldi/dt) can be added to compensate the voltage drop on ac filtering inductors. During normal operation, v_{dref} is set to 1 pu (peak value of the phase voltage) and v_{qref} is set to 0 pu.

Figure 6-6 shows the power control in WF emulator. The converter side ac voltages are detected for PLL and dq transformation. A feedforward active and reactive power control is employed to generate current reference with fast dynamic response.

Figure 6-7, Figure 6-8 and Figure 6-9 present the simulation results with step change of active power, reactive power and ac voltage magnitude references, respectively, with the main circuit parameters of the real system given in Table 6-1.



(a) Real MTDC system



(b) Scaled down system with windfarm emulators

Figure 6-4. System configuration for the four -terminal HVDC platform.

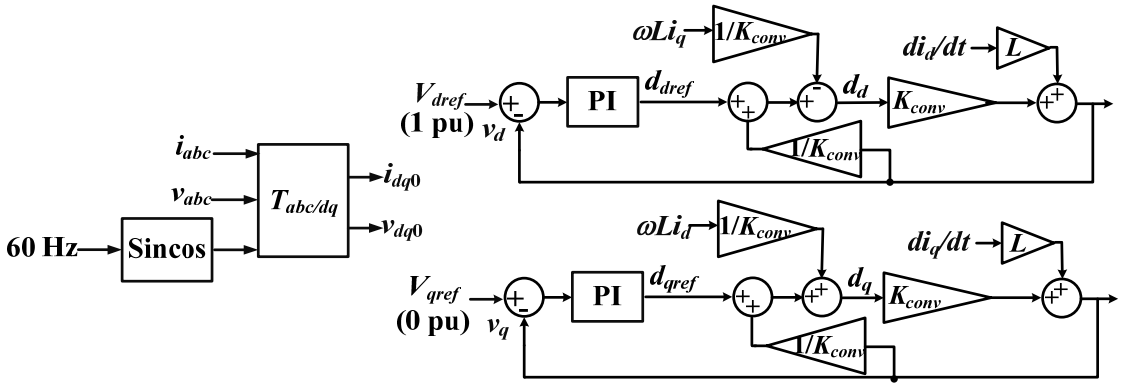


Figure 6-5. AC voltage regulation in offshore converter station.

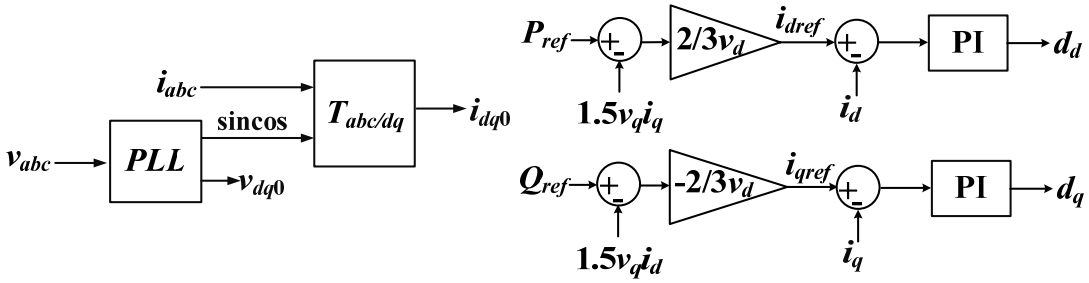
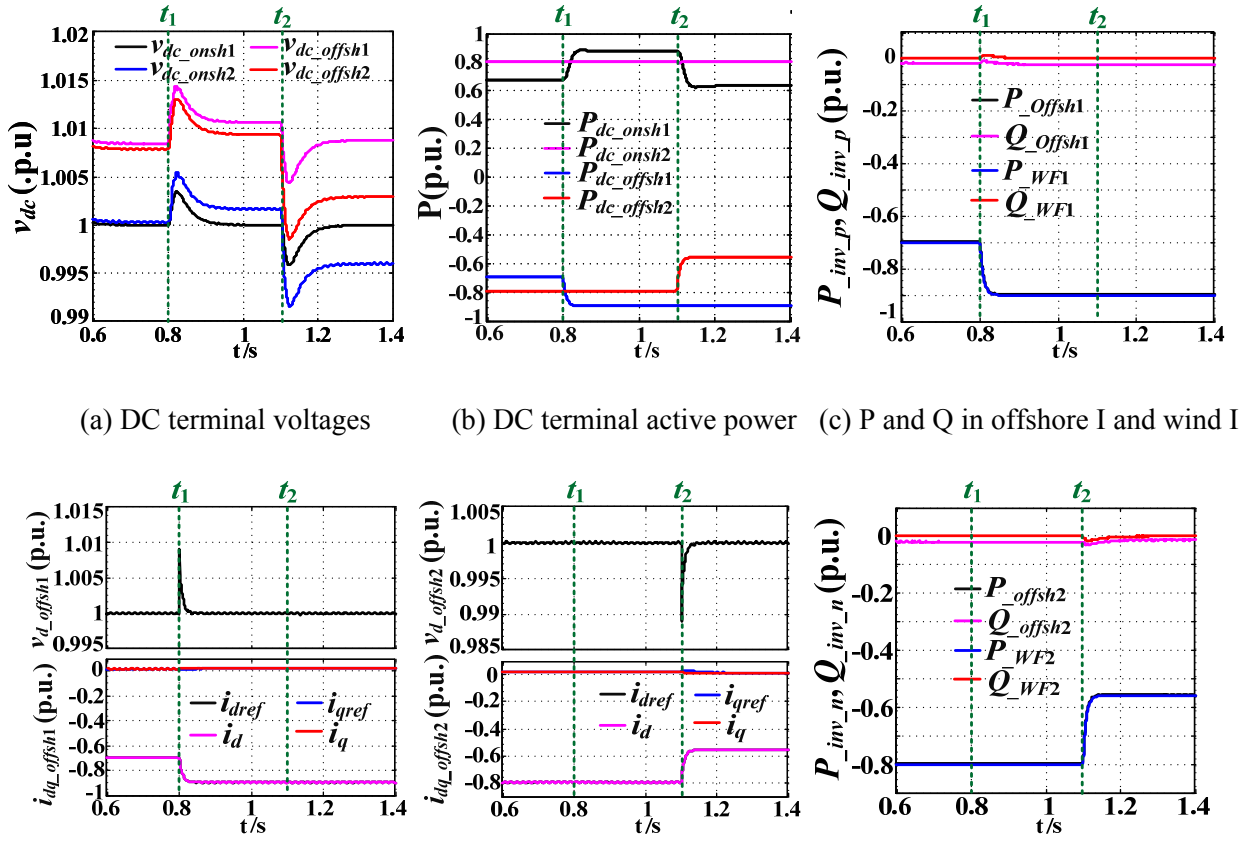


Figure 6-6. Power control in windfarm emulator.

Table 6-1. Main circuit parameters of real system and scaled-down platform.

	Real system	**Scaled-down platform**
DC voltage	300 kV	400 V
AC voltage	161 kV	208 V
Power rating of VSC 1,3	250 MVA	5 kVA
Power rating of VSC 2,4	200 MVA	4 kVA
AC inductance of VSC 1,3	41.3 mH (0.15 pu)	3.4 mH (3.2 mH)
DC capacitance of VSC 1,3	0.25 mF	0.3 mF (1.35 mF)
AC inductance of VSC 2,4	41.3 mH	4.25 mH (4 mH)
DC capacitance of VSC 2,4	0.25 mF	0.3 mF (1.35 mF)
Cable 1 (100 km)	2.08 Ω, 32.4 mH, 27 uF	0.185 Ω, 2.88 mH, 0.30 mF (0.2 Ω, 2.5 mH)
Cable 2 (70 km)	1.55 Ω, 27.4 mH, 14.7 uF	0.14 Ω, 2.44 mH, 0.17 mF (0.15 Ω, 2.5 mH)
Cable 3 (60 km)	5.946 Ω, 28.5 mH, 6.6 uF	0.53 Ω, 2.53 mH, 0.07 mF (0.5 Ω, 2.5 mH)
Cable 4 (100 km)	10.0 Ω, 40.3 mH, 14 uF	0.889 Ω, 3.58 mH, 0.16 mF (1 Ω, 3.5 mH)



(a) DC terminal voltages (b) DC terminal active power (c) P and Q in offshore I and wind I

(d) v_d and i_{dq} in offshore I (e) DC terminal active power (f) P and Q in offshore I and wind II

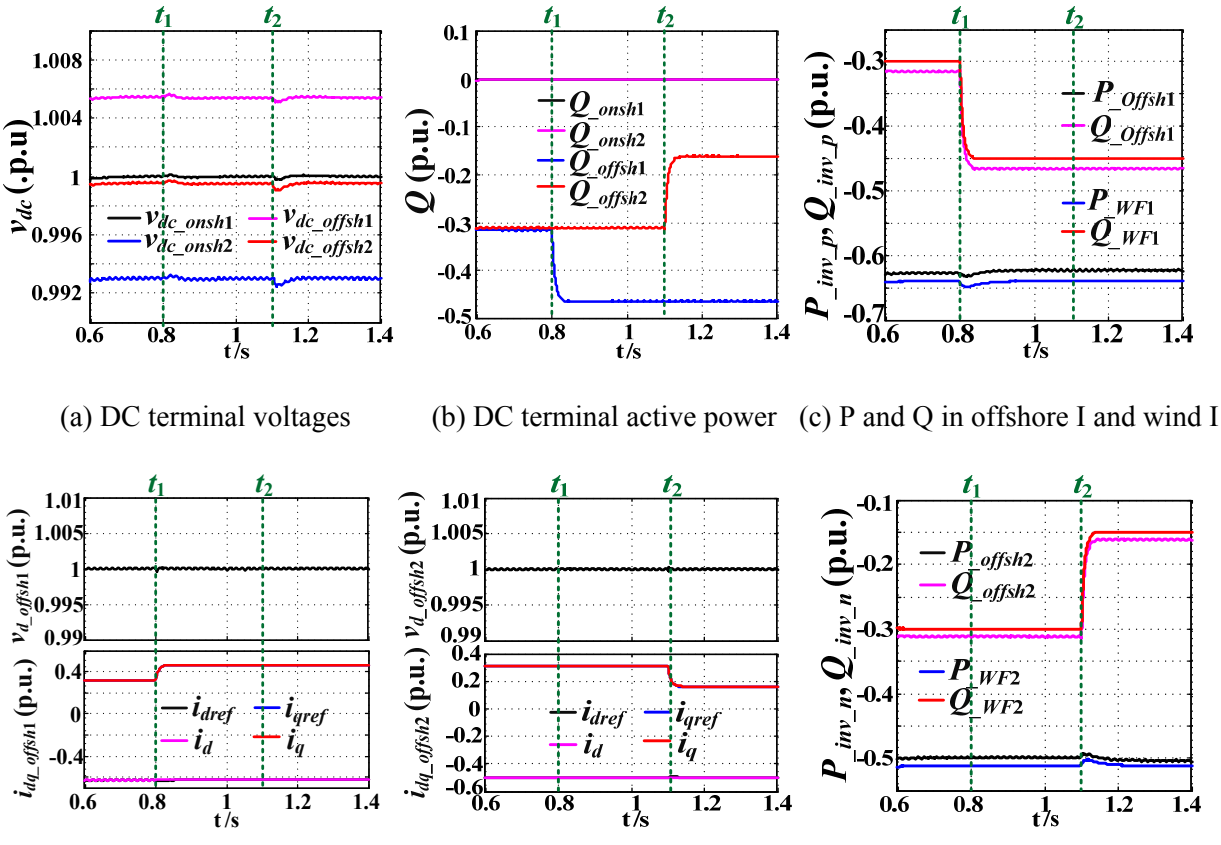
Figure 6-7. Simulation results with active power step in windfarms.

Limited by the availability of commercial resistors and reactors, the real parameters of the scaled-down system, given as the red numbers inside the brackets, are a little different from the theoretically scalded down values. In Figure 6-7, active power reference of wind farm emulator I is increased from 0.7 pu to 0.9 pu at $t_1 = 0.8$ s, while that of wind emulator II is reduced from 0.8 pu to 0.56 pu at $t_2 = 1.1$ s. Initially, the step change of active power leads to a low dc voltage variation in each terminal.

Because of the dc voltage control, however, the dc voltage of onshore converter I (v_{dc_onsh1}) goes back to 1 pu after a short transient period (~ 0.05 s), and the other terminal voltages are determined by power flow and dc cable resistance (Figure 6-7(a)). By maintaining ac voltage in the PCC points, the active power change in wind farm emulators are reflected in the offshore converter stations, as shown in Figure 6-7(b), (c) and (f). The reactive power difference between wind farm emulator ($Q_{_WF1}$ and $Q_{_WF2}$) and

offshore converter ($Q_{_offsh1}$ and $Q_{_offsh2}$) is caused by reactive power consumption of ac filters. With properly designed controllers, ac voltage magnitudes in *PCC*1 and *PCC*2 remain 1 pu except for a temporary voltage swell when active power suddenly changes.

Figure 6-8 shows the simulation results with reactive power step in wind farm emulators. At $t_1 = 0.8$ s, the reactive power reference of wind farm emulator I is increased from 0.3 pu to 0.45 pu, while at $t_2 = 1.1$ s, reactive power reference of wind emulator II is reduced from 0.3 pu to 0.15 pu. Compared to Figure 6-7, step change of reactive power has a much smaller impact on dc terminal voltages and ac voltage magnitudes (Figure 6-8(a), (d) and (e)), but it induces higher differences between active power of wind farm emulators ($P_{_WF1}$ and $P_{_WF2}$) and that of offshore converters ($P_{_offsh1}$ and P_{offsh2}). The increased differences are caused by leakage impedances of the Y/Δ transformers (0.02 pu in the simulation model).

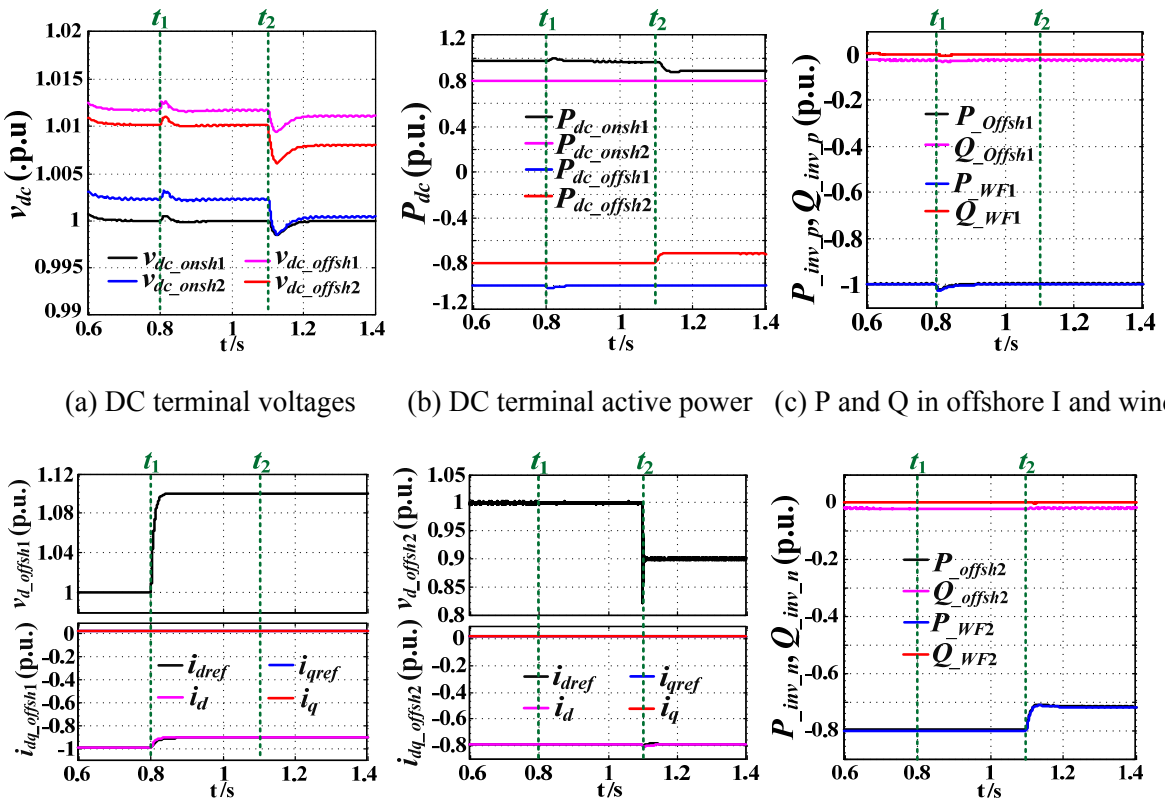


(a) DC terminal voltages (b) DC terminal active power (c) P and Q in offshore I and wind I

(d) DC terminal voltages (e) DC terminal active power (f) P and Q in offshore I and wind II

Figure 6-8. Simulation results with reactive power step in windfarms.

Although ac voltage in P_{CC1} is well regulated by offshore converter I, the voltage magnitude in the other side of transformer will change when reactive power varies. Consequently, due to the same phase current and different ac voltage magnitude, the active power generation in WF emulation converters will deviate from that calculated in offshore converters. This mismatch tends to reduce when the reactive power injection drops (Figure 6-8(c) and (f)), and becomes zero if no reactive power is generated (Figure 6-7(c) and (f)). To test the dynamic response of ac voltage regulation, the voltage magnitude reference of offshore converter I is increased from 1 pu to 1.1 pu at t_1 = 0.8 s, and the voltage reference for offshore converter II reduces from 1 pu to 0.9 pu at t_2 = 1.1 s. The simulation results are given in Figure 6-9. Since the maximum phase current in WF emulator II is limited to 0.8 pu, when ac voltage drops to 0.9 pu, its active power becomes 0.9 × 0.8 = 0.72 pu (Figure 6-9(b) and (f)), which leads to variations in both power flow (Figure 6-9(b)) and dc voltage (Figure 6-9(a)).



(a) DC terminal voltages (b) DC terminal active power (c) P and Q in offshore I and wind I

(d) DC terminal voltages (e) DC terminal active power (f) P and Q in offshore I and wind II

Figure 6-9. Simulation results with voltage magnitude step in windfarms.

For wind farm emulator I, higher ac voltage magnitude requires smaller ac current, and thus constant active power (Figure 6-9(b) and (c)). The ac voltage magnitudes in both PCC_1 and PCC_2 can be well regulated to their references, while a short transient period occurs in offshore converter II because of the sudden active power reduction (Figure 6-9(d) and (e)).

To sum up, through the ac voltage regulation, the active power generated by WF emulators can be dynamically transferred to offshore converters. Then, by controlling dc voltage and active power in the onshore converter stations, the smoothed wind power can be further transmitted to onshore grids through the MTDC network. Therefore, neglecting power losses, the active power absorption of the onshore converters $P_{onshore}$ ($=P_{onsh1}+P_{onsh2}$) should equal to that generated by the WF emulators P_{WF} ($=P_{WF1}+P_{WF2}$). Otherwise dc voltage will increase when $P_{WF} > P_{onshore}$, and decrease when $P_{WF} < P_{onshore}$.

6.2 Cascaded Droop Control Scheme for AC Fault Ride Through

6.2.1 Control Mechanism

With a SLG fault in either onshore converter, $P_{onshore}$ will drop to some extent if the maximum phase current is limited below 1.5 pu. Under this condition, if active power generated by wind farms remains, P_{WF} will be higher than $P_{onshore}$, and dc voltage will keep increasing and may cause severe damage. Nevertheless, regulating ac voltage in PCC points, offshore converters cannot directly control dc terminal voltage or active power through the widely used dc voltage margin and droop control. As a solution, a cascaded droop control is proposed, which builds a nearly linear relationship between the offshore converter side dc terminal voltage and the active power generated by the WF, using the ac voltage magnitude as an intermediate variable.

Figure 6-10 illustrates the dc voltage control schemes with different MTDC configurations. In Figure 6-10(a), the onshore converter I is in charge of dc voltage regulation, while onshore converter II employs the dc voltage margin control. When dc voltage is higher or lower than the pre-set levels, the margin control will be triggered and onshore converter II will take responsibility for dc voltage control until reaching its power limit. Similarly, offshore converter I and II adopt the dc voltage droop control, which

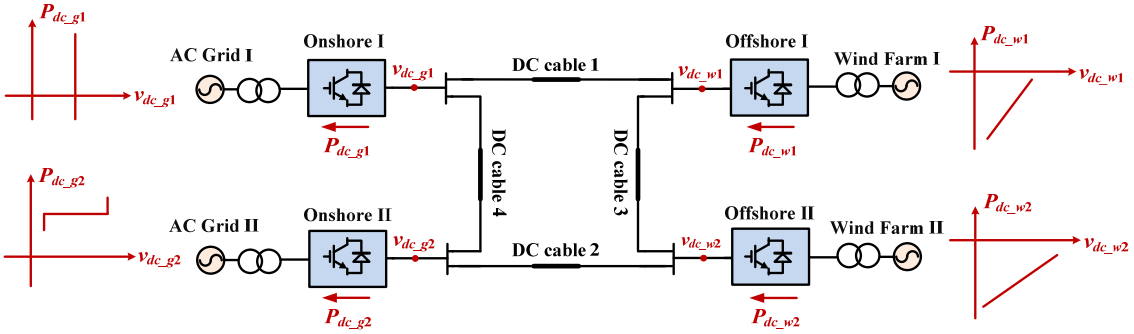
adjust their active power references according to the dc terminal voltage variations. By choosing proper initial operation point and droop constant, the active power generation of WFs can drop autonomously under SLG fault and keep dc voltage increase within a desirable range. In addition, the active power sharing between offshore converters can also be adjusted by using different droop curves.

Without ac grid, however, the dc voltage margin and droop control cannot be implemented. Therefore, in Figure 6-10(b), a cascaded droop control, which includes $v_{dc} - v_{ac}$ droop in offshore converter and $v_{ac} - P$ droop in the WF emulators, is adopted. During SLG fault, the magnitude of ac voltage v_{ac_w1} and v_{ac_w2} will drop with dc voltage increase, and according to the droop curves, the lower magnitude of v_{ac_wf1} and v_{ac_wf2} will induce wind power reduction in both WFs.

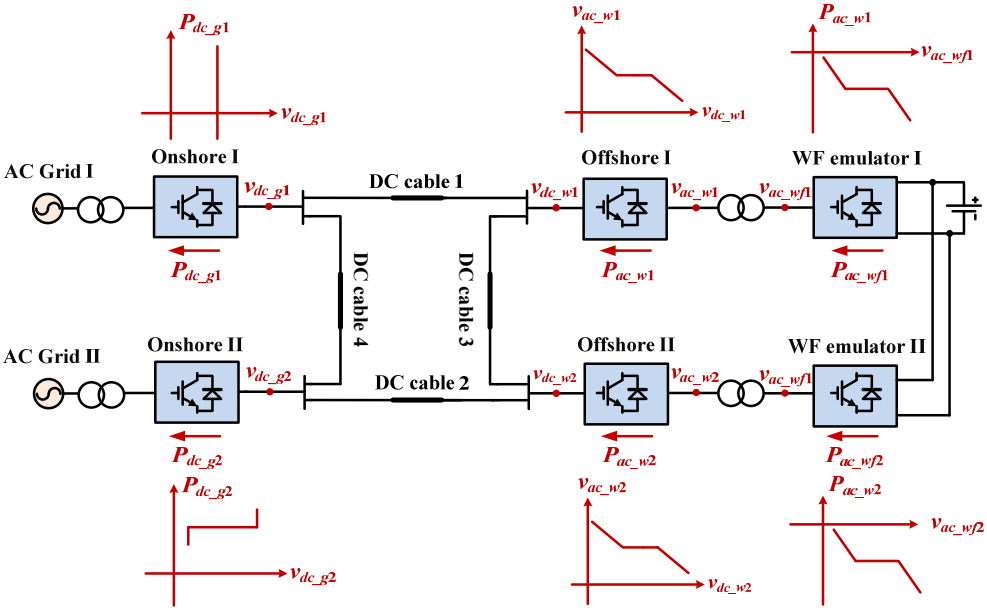
In practice, the wind turbines cannot reduce its output power instantaneously due to their inherent inertia, and dc chopper resistors are used to absorb unbalanced active power until their thermal limit is reached. Meanwhile, the wind turbine pitch angle is regulated according to the droop curve to reduce the mechanical power and thus active power generation. A dead-band is also added in the droop curve to keep the normal operation of offshore converters and WFs uninterrupted, as illustrated in Figure 6-11. Take $v_{dc} - v_{ac}$ droop for example, if dc voltage deviation is smaller than the preset dead-band ΔV_{dc}, the offshore converter should operate in constant ac voltage control mode, otherwise the droop mechanism is initiated.

To avoid sudden voltage variation during modes change, the real dc voltage is used as the initial point of $v_{dc} - v_{ac}$ droop curve when it exceeds the specified dead-band. Then, the ac voltage reference of offshore converters will be defined by the droop curve and change with the dc voltage variation. The $v_{ac} - P$ droop operates in a similar manner. Different pre-fault operation points determine distinct droop curves and thus different steady state WF power generation during ac fault conditions.

Ideally, the coordination of $v_{dc} - v_{ac}$ and $v_{ac} - P$ droop is equivalent to $v_{dc} - P$ droop in Figure 6-10(a), and v_{ac} serves as an intermediate variable. The leakage impedance of the ac transformer, however, leads to ac voltage magnitude deviation between v_{ac_w1} and v_{ac_wf1}, which interferes in the droop control and make the operation point diverge from the designed values. This effect can be compensated through droop curve design, which will be discussed in the following chapters.

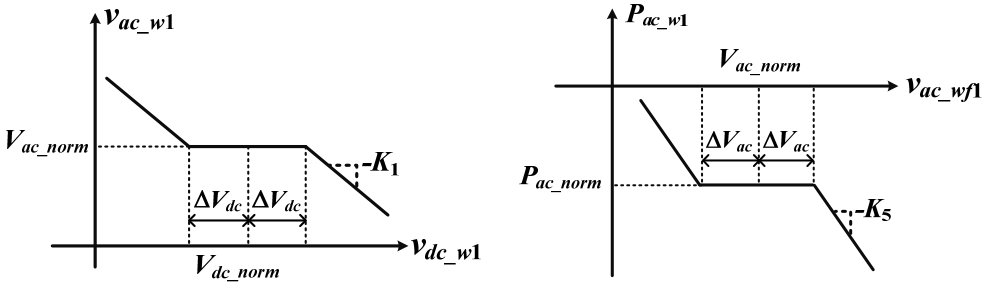


(a) With dc voltage margin (onshore II) and dc voltage droop (offshore I and II) control



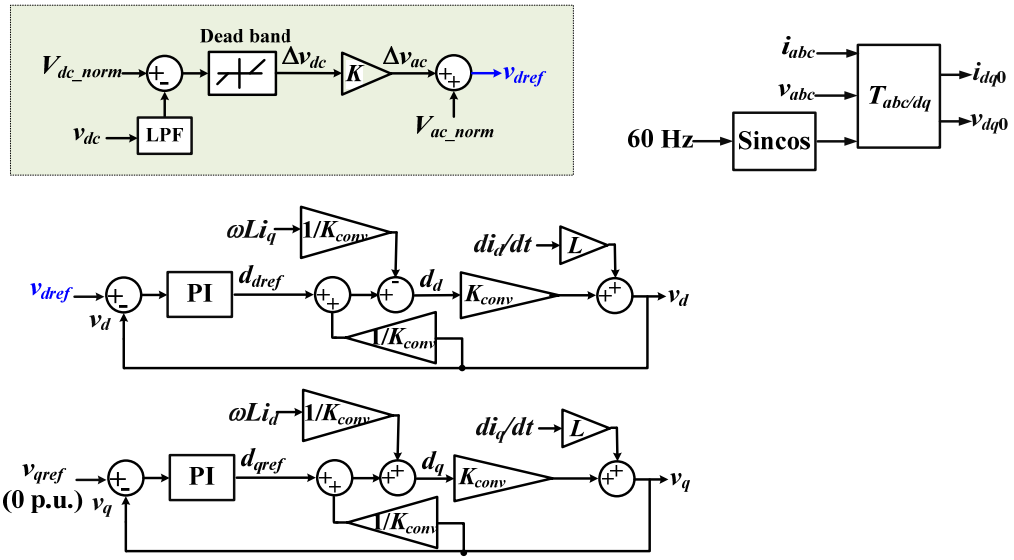
(b) With dc voltage margin (onshore II) and cascaded droop (offshore and WF emulator I and II) control

Figure 6-10. Cascaded droop control in four -terminal HVDC platform.

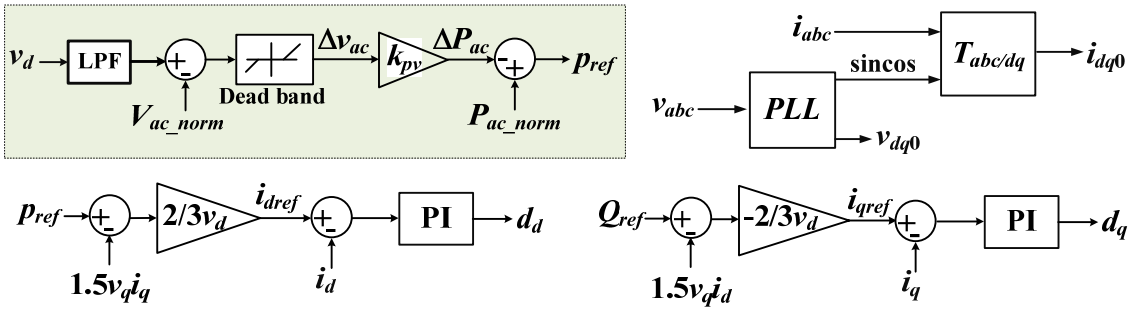


(a) $v_{dc} - v_{ac}$ droop in offshore converter (b) $v_{ac} - P$ droop in windfarm emulator

Figure 6-11. Cascaded droop control with dead-band.



(a) Control diagram of $v_{dc} - v_{ac}$ droop with dead-band in offshore converter



(b) Control diagram of $v_{ac} - P$ droop with dead-band in windfarm emulator converter

Figure 6-12. Implementation of cascaded droop control.

Figure 6-12 gives the diagram of the cascaded droop control in offshore converter and WF emulator. Instead of constant V_{dref} in Figure 6-5 and P_{ref} in Figure 6-6, the ac voltage magnitude and active power references in Figure 6-12 move on the droop curves until a steady state is arrived. To avoid stability issues, the control bandwidth of offshore converter should be higher than that of the WF emulator [142]. Otherwise, the offshore converter cannot track the active power change and the system will finally be instable due to the continuous error accumulation. For the same reason, the references generated by droop curves should change slower than the corresponding control schemes, e.g., a low pass filter is added in $v_{dc} - v_{ac}$ droop to enable a slower variation of v_{dref} than the dynamic response of ac voltage control loop.

6.2.2 Power Flow Calculation

Because of the full controllability of converters, the dc voltage in onshore converter I (slack bus), and active power in onshore converter II, WF emulator I and II (active power regulator), are considered as known parameters. Additionally, since the efficiency of WF emulator (including the interfacing transformer T1 and T2) under certain operating condition can be estimated, the active power of offshore converter I and II can also be regarded as known parameters. Consequently, in the four-terminal HVDC system in Figure 6-13, the active power in onshore converter I (P_{dc3}), dc voltage in onshore converter II (V_{dc4}), offshore I (V_{dc1}) and offshore II (V_{dc2}) are unknown variables.

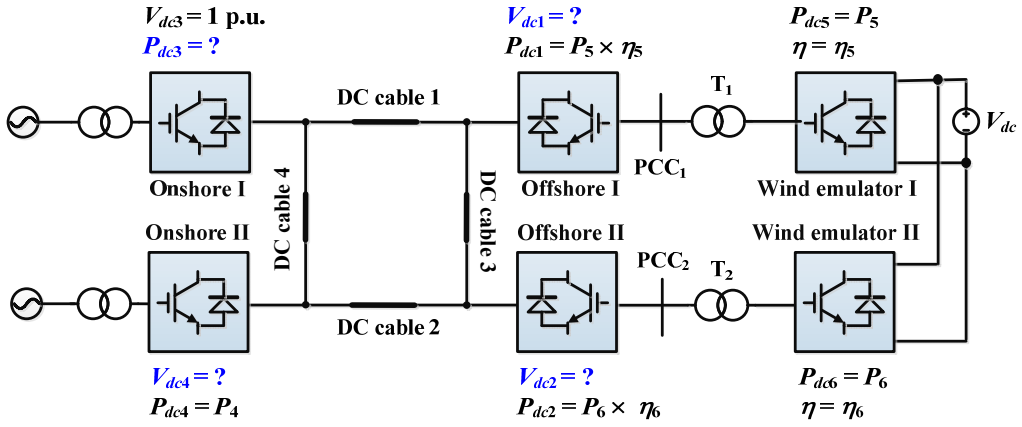


Figure 6-13. Variables in power flow calculation in the MTDC system.

To solve these variables, the parameter estimator equations of the four-terminal HVDC system is derived in (6 - 1), in which Y_{12}, Y_{13}, Y_{34}, Y_{24} are the admittance of dc cable 3, dc cable 1, dc cable 4 and dc cable 2, respectively . Here $I_{dc1} = P_{dc1} / V_{dc1}$, where $I_{dc2} = P_{dc2} / V_{dc2}$, $I_{dc3} = P_{dc3} / V_{dc3}$ and $I_{dc4} = P_{dc4} / V_{dc4}$.

$$\begin{bmatrix} V_{dc1} \\ V_{dc2} \\ I_{dc3} \\ V_{dc4} \end{bmatrix} = \begin{bmatrix} Y_{12} + Y_{13} - \frac{Y_{13}Y_{13}}{(Y_{13}+Y_{34})} & -Y_{12} & \frac{-Y_{13}}{(Y_{13}+Y_{34})} & \frac{-Y_{13}Y_{34}}{(Y_{13}+Y_{34})} \\ -Y_{12} & Y_{12} + Y_{24} & 0 & -Y_{24} \\ \frac{Y_{13}}{(Y_{13}+Y_{34})} & 0 & \frac{1}{(Y_{13}+Y_{34})} & \frac{Y_{34}}{(Y_{13}+Y_{34})} \\ \frac{-Y_{13}Y_{34}}{(Y_{13}+Y_{34})} & -Y_{24} & \frac{-Y_{34}}{(Y_{13}+Y_{34})} & Y_{24} + Y_{34} - \frac{Y_{34}Y_{34}}{(Y_{13}+Y_{34})} \end{bmatrix}^{-1} \begin{bmatrix} I_{dc1} \\ I_{dc2} \\ V_{dc3} \\ I_{dc4} \end{bmatrix} \quad (6 - 1)$$

A simplified flow chart of the numerical iterative procedure for solving the dc grid power flow is derived and given in Figure 6-14. An iteration loop is built in this algorithm to conduct the Gauss-Seidel calculations based on (6 - 1).

The control modes and corresponding parameters of P (V_{dc}) will update in each iteration according to the newest set of voltage estimates and (6 - 2). Here the cascaded droop control is simplified to a single $v_{dc}_P_{dc}$ droop control, with K_{dc_p}, ΔV_{dc} representing the equivalent droop constant and dead-band (mainly considers dead-band in both droop curves and ac voltage deviation in the system using cascaded droop control). If power losses and ac voltage magnitude deviation between offshore converter and WF emulator are negligible, K_{dc_p} equals to the product of droop constants in $v_{dc} - v_{ac}$ and $v_{ac} - P$ droop, while ΔV_{dc} equals to the sum of dead-band in these two droop curves.

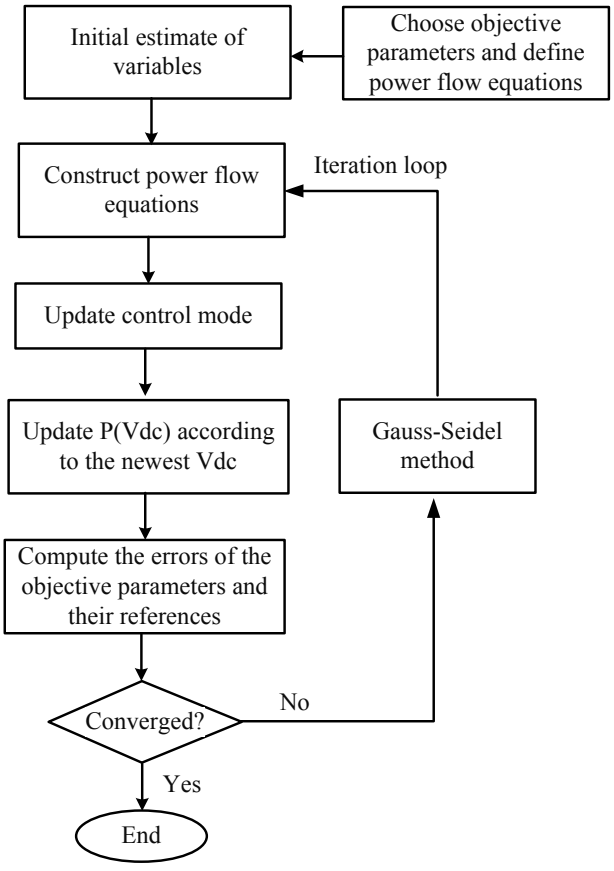


Figure 6-14. Flow chart of the iteration for dc power flow calculation.

$$P_{dc1,2ref} = \begin{cases} P_{dc1,2} + K_{dc_p}\left(v_{dc1,2} - \left(v_{dc1,2_{rated}} + \Delta V_{dc1,2_{eq}}\right)\right) & v_{dc1,2} \geq \left(v_{dc1,2_{rated}} + \Delta V_{dc1,2_{eq}}\right) \\ P_{dc1,2} + K_{dc_p}\left(v_{dc1,2} - \left(v_{dc1,2_{rated}} - \Delta V_{dc1,2_{eq}}\right)\right) & v_{dc1,2} \leq \left(v_{dc1,2_{rated}} - \Delta V_{dc1,2_{eq}}\right) \\ P_{dc1,2} & \left(v_{dc1,2_{rated}} - \Delta V_{dc1,2_{eq}}\right) < v_{dc1,2} < \left(v_{dc1,2_{rated}} + \Delta V_{dc1,2_{eq}}\right) \end{cases}$$

(6 - 2)

A good initial estimate of the unknown variables can reduce the required number of iterations and computational time before reaching a desirable level of accuracy. Otherwise the iteration may become non-convergent, or convergent but with an unrealistic solution. In general, the Gauss-Seidel method converges for a wide range of initial guesses. In this work the rated operation point is set as the initial estimate of variables for less iteration steps.

6.3 Simulation Results of MTDC during SLG Fault

Because of lightning ionizing air, salt spray or pollution on insulators, SLG fault may also occur in the ac terminal of a MTDC network. With the specified functionality of each converter in the four-terminal HVDC system defined in this dissertation, the most serious case occurs in onshore converter side SLG fault(s). Because of the surplus active power, dc voltage will increase in this case and threaten the system insulation. On the contrary, if SLG fault occurs in the offshore converter station, ac voltage in the PCC point cannot be well regulated, and system may need to shut down to prevent high fault current and controller saturation.

On the other hand, even if offshore converter and WF emulator can withstand ac fault and obtain continuous operation, the reduced active power generation can be compensated by the slack bus and no serious damages will be observed. Therefore, only onshore side SLG fault is considered here. Moreover, with N-1 contingency, one onshore converter is assumed to suffer SLG fault at one time.

For a comprehensive analysis, system performance, including dc voltage, active and reactive power of each converter, and PCC voltage, etc., with different fault location, current priority and control parameters is evaluated and compared in the following sections.

6.3.1 Different Fault Locations

The system configuration with a SLG fault occurring in onshore converter I is illustrated in Figure 6-15, where a grid side fault is assumed due to its much higher possibility if compared to the converter side fault. In practice, the transformer installed between each ac grid and converter station has a Y/Δ connection, which blocks the zero sequence current and leaves only negative sequence component to be eliminated during SLG fault conditions. Other than the unbalanced phase current, second order active power ripple also exists in the dc side. For a two-level converter, either unbalanced phase current or dc power ripple can be eliminated. The operation mechanism of these two control objectives, however, conflicts and cannot be realized at the same time. Moreover, for accurate positive and negative sequence components decomposition, positive sequence voltage should be used for PLL. Focusing on the active power balance and dc overvoltage suppression among dc terminals, only a PLL with positive sequence voltage is implemented in the simulation model and experimental platform.

In Australia and Germany, reactive current component has the highest priority under fault condition, while the opposite trend applies on the grid codes of Ireland, Spain and UK [137]. If d axis current has higher priority, dq axis current will remain the same if the peak value of the phase current does not exceed its maximum value I_{max}. Otherwise $i_d = i_d$ ($i_d < I_{max}$) or I_{max} ($i_d \geq I_{max}$) and $i_q = \sqrt{I_{max}^2 - i_d^2}$, as shown in Figure 6-16. Similarly, the higher q axis current priority can be realized by maintaining q axis current if possible, i.e., $i_q = i_q$ ($i_q < I_{max}$) or I_{max} ($i_q \geq I_{max}$) and $i_d = \sqrt{I_{max}^2 - i_q^2}$. With limited converter current rating, the priority setting will impact the active power drop during SLG fault and thus lead to different post-fault steady state dc overvoltage.

Having the same v_{dc} - v_{ac} droop in offshore converter I and II and v_{ac} - P droop in WF emulators, the fault characteristics will be studied in the following two cases. The main circuit parameters for the scaled-down system in simulation are given in Table 6-1, and control parameters can be found in Table 6-2 to limit dc voltage below 1.15 pu. The rated dc voltage in offshore stations is selected as their initial points.

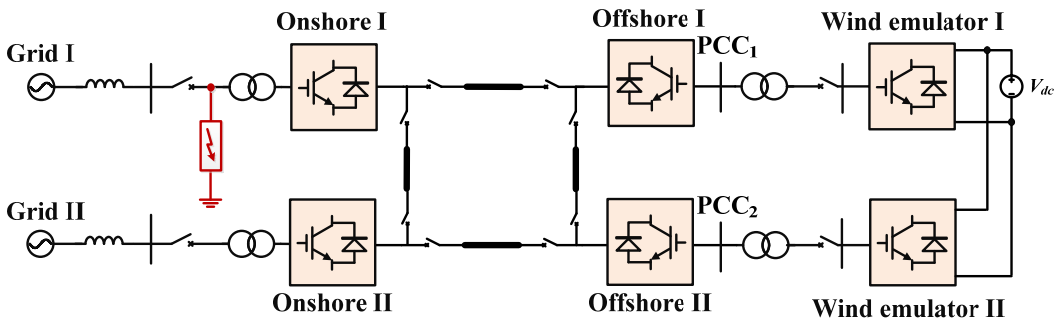


Figure 6-15. Studied SLG fault scenarios.

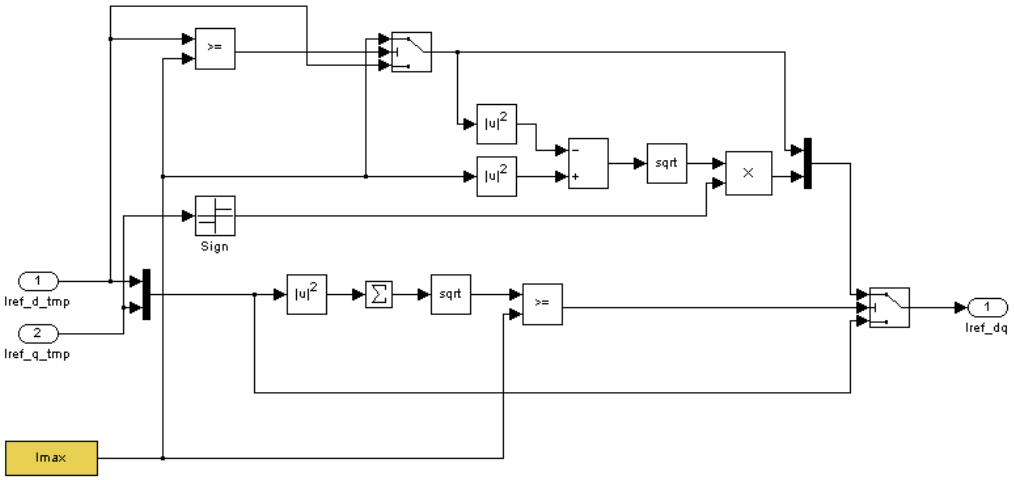


Figure 6-16. Simulation model for higher d axis current priority.

Table 6-2. Parameters for all controllers used in simulation model.

PI controller	k_p	k_i	
DC voltage control	1.95	51.314	
Current control	0.108	2.773	
AC voltage control	0.0132	4.4	
Droop control	**Initial point / V**	**Droop constant**	**Dead-band / V**
v_{dc} - v_{ac} droop	404.72 (1.0118 pu) for offshore I 404.12 (1.0103 pu) for offshore II	1	10 (0.025 pu)
v_{ac} - P droop	169.8 (1 pu)	150	6 (0.0353 pu)

5.3.1.1 SLG Fault in Onshore Converter I

A. d axis current has higher priority

1) Onshore converter II has sufficient power capacity (case 1)

In some cases, converters are not operating in their full capacity and certain power margins are available. If the healthy onshore converter can handle the active power absorption drop caused by the SLG fault, WFs do not need to decrease their power generation and full power transmission can be achieved. This scenario (SLG fault occurs in onshore converter I, d axis has higher priority and onshore converter II has sufficient power capacity) is tested as case 1 in simulation, with reference and power capacity of each converter set as Table 6-3. DC voltage margin and cascaded droop control are implemented to deal with dc voltage increase.

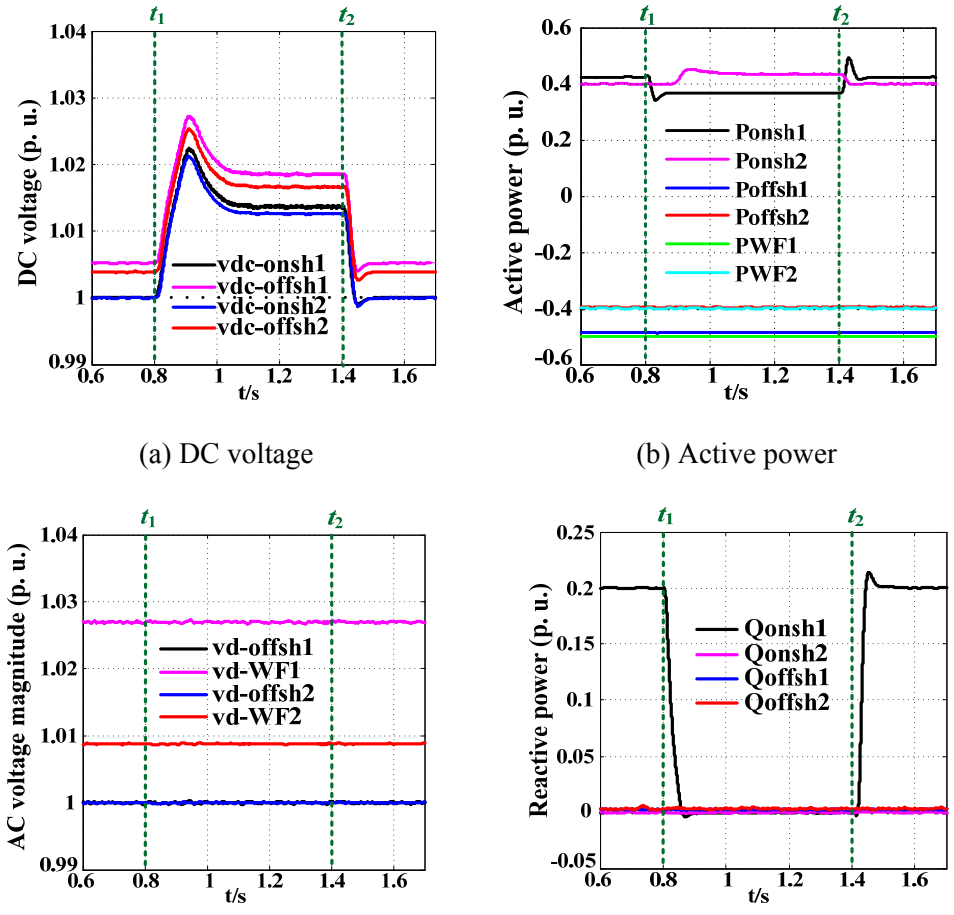
Table 6-3. Reference and power capacity settings in case 1.

	Control mode	**Vdc or P reference (pu)**	**Q reference (pu)**	**Power capacity (pu)**
Onshore I	DC voltage control	1	0.2	0.5
Onshore II	Active power control	0.5	0	0.5
Offshore I	AC voltage control	1	N/A	1
Offshore II	AC voltage control	1	N/A	0.8
Windfarm emulator I	Active power control	0.5	0	1
Windfarm emulator II	Active power control	0.4	0	0.8

Simulation results of case 1 are given in Figure 6-17, where SLG fault starts at t_1 = 0.8 s and clears at t_1 = 1.4 s, with power transferring from dc to ac defined as the positive direction. When SLG fault occurs at t_1 = 0.8 s, the reactive power generated by onshore converter I drops to zero for active power support (Figure 6-17(d)), but due to the fault, its active power still reduces to 0.3675 pu On the other hand, power generation of WFs remains initially. The surplus active power, consequently, charging the dc capacitors and causes an obvious dc voltage increase (Figure 6-17(a)). With the implemented dc voltage margin

control, onshore converter II changes its operation mode from active power control to dc voltage regulation, and tends to absorb more power (Figure 6-17(b)). Finally, it is able to regulate its dc terminal voltage to the pre-set reference of 1.0125 pu, and dc voltage in other converter stations are determined by active power flow and dc cable resistance.

Since dc voltage variation stays within the dead-band of cascaded droop control, the ac voltage magnitude at PCC_1 and PCC_2 are not affected (Figure 6-17(c)), and active power generation of WFs keep the same. The leakage impedance of Y/Δ transformers in offshore converter I and II are assumed to be 0.05 pu and 0.02 pu, respectively, which cause ac voltage magnitudes of 1.0283 pu and 1.0091 pu in the WF emulator I and II.



(a) DC voltage

(b) Active power

(c) AC voltage magnitude

(d) Reactive power

Figure 6-17. Simulation results with SLG fault in onshore converter I (case 1).

2) VSC4 has insufficient active power capacity (case 2)

Opposite to case 1, if the healthy onshore converter has limited power capacity and cannot balance active power during SLG fault, active power reduction of WFs will be necessary. The reference and power capacity of each converter are given in Table 6-4, where the maximum power output of onshore converter II is limited to 0.4 pu (case 2).

As shown in Figure 6-18, the active power absorption of onshore converter II cannot increase due to its power limitation (Figure 6-18(b)), and the dc voltage increases until it exceeds the dead-band of the cascaded droop control. The higher ac voltage magnitude in PCC1 under normal condition (1.027 pu) makes WF emulator I less susceptible to dc voltage increase due to the dead-band, and no active power variation can be found. In contrast, with the given initial values and droop constants in Table 6-2, the ac voltage magnitude in PCC2 drops from 1.009 pu to 0.9657 pu and induces an active power drop of 0.024 pu in WF emulator II. The active power generation drop, in turn, will suppress the dc overvoltage.

Table 6-4. Reference and power capacity settings in case 2.

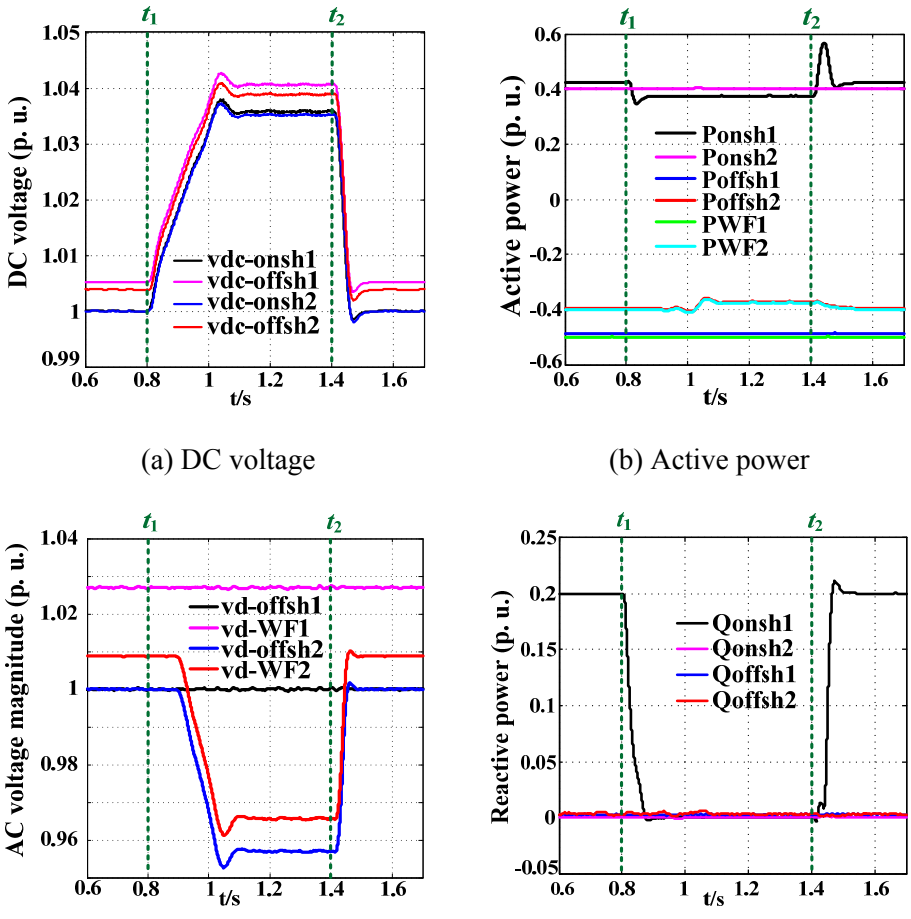
	Control mode	**Vdc or P reference (pu)**	**Q reference (pu)**	**Power capacity (pu)**
Onshore I	DC voltage control	1	0.2	0.5
Onshore II	Active power control	0.5	0	0.4
Offshore I	AC voltage control	1	N/A	1
Offshore II	AC voltage control	1	N/A	0.8
Windfarm emulator I	Active power control	0.5	0	1
Windfarm emulator II	Active power control	0.4	0	0.8

B. q axis current has higher priority (case 3)

Figure 6-19 provides simulation results when q axis current has higher priority (case 3). Reference and power capacity of each converter is the same as Table 6-4. During SLG fault, the reactive power of onshore converter I remains but active power drops from 0.4244 pu to 0.3196 pu Since onshore converter

II has already output its maximum power, the difference between active power generation and absorption leads to fast dc voltage increase and ac voltage magnitude decrease in both PCC1 and PCC2. Due to the leakage impedance of the isolation transformer, however, the ac voltage magnitude in WF emulator I station is 1.016 pu during fault condition, which stays inside the dead-band and cannot activate the droop control. WF emulator II, consequently, will take responsibility of dc voltage regulation alone by reducing its active power generation until a steady state is arrived.

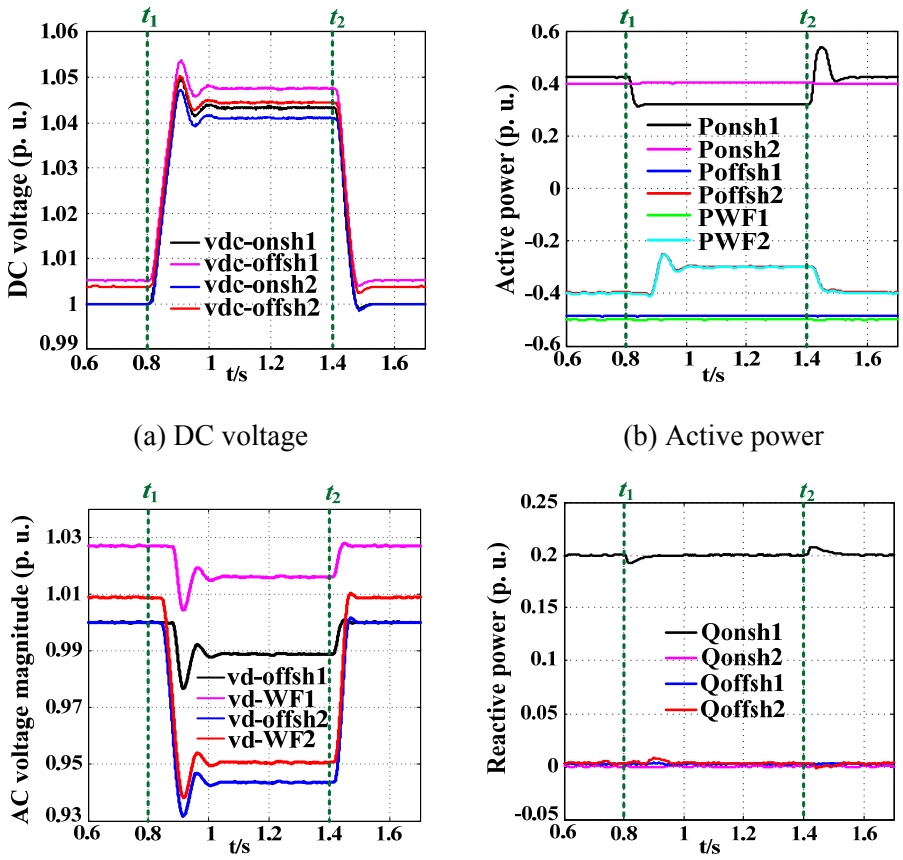
In summary, case 3 (i_q has higher priority) has the most serious dc voltage increase due to the larger active power drop in the onshore converters. With the same control parameters, it will cause a lower ac voltage magnitude and thus requires more active power reduction in WF emulators.



(a) DC voltage (b) Active power

(c) AC voltage magnitude (d) Reactive power

Figure 6-18. Simulation results with SLG fault in onshore converter I (case 2).



(a) DC voltage (b) Active power

(c) AC voltage magnitude (d) Reactive power

Figure 6-19. Simulation results with SLG fault in onshore converter I (case 3).

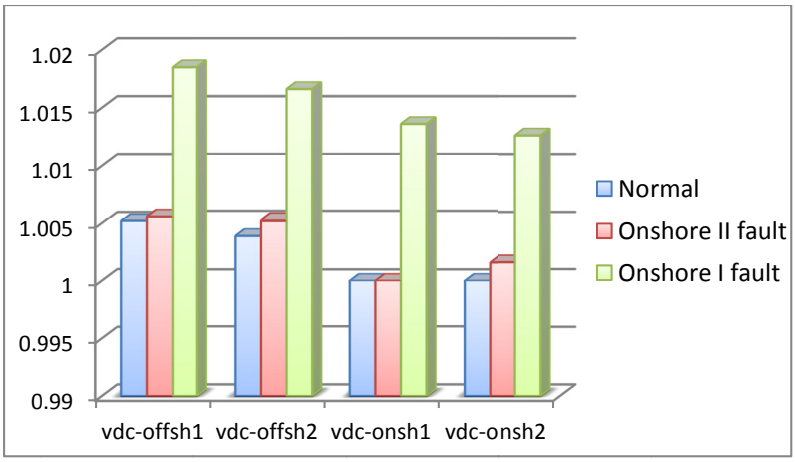
Therefore, in cases that reactive power support is more important than active power transfer, droop curve should be well designed for acceptable dc voltage increase.

5.3.1.2 SLG Fault in Onshore Converter II

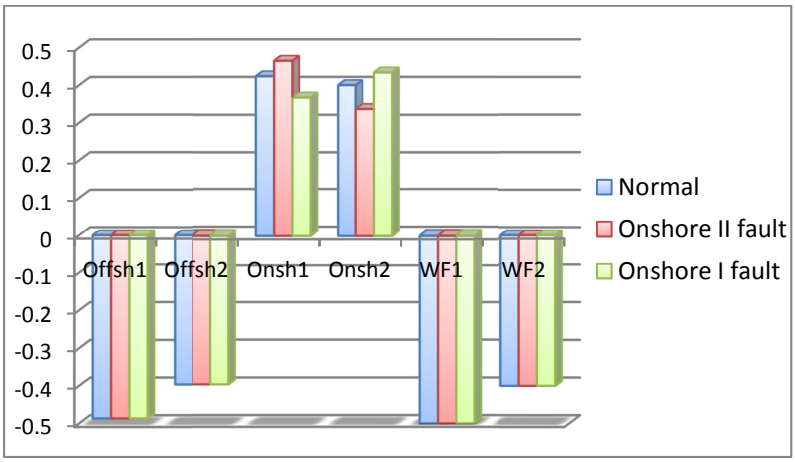
A. d axis current has higher priority

1) Onshore converter I has sufficient power capacity (case 1)

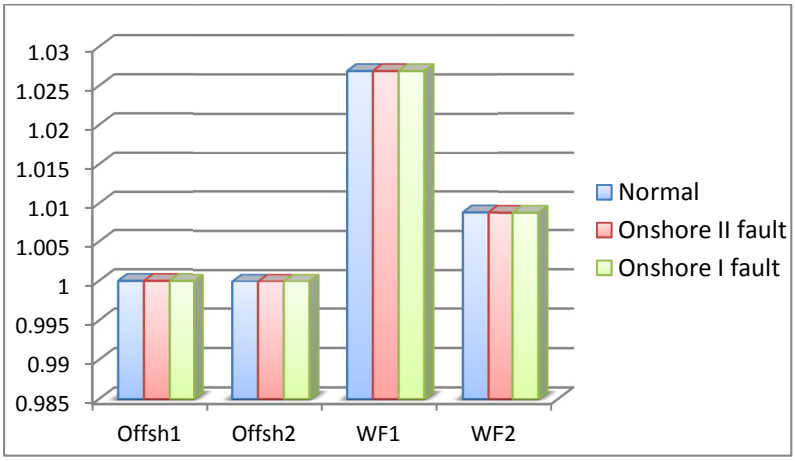
The selected simulation results in normal condition, onshore converter I side SLG fault and onshore converter II side SLG fault are compared in Figure 6-20 when d axis current has higher priority and the healthy converter station has sufficient power capacity. In this case, the active power drop in onshore converter II can be fully compensated by onshore converter I, which increases its active power from 0.4235 pu to 0.4648 pu and maintains its dc terminal voltage to 1 pu.



(a) DC voltage



(b) Active power



(c) AC voltage magnitude

Figure 6-20. Performance comparison when i_d has higher priority and healthy converter has sufficient power capacity.

Although a slight dc voltage increase is introduced in other converter stations due to power flow variation, it is not high enough to activate droop control. The ac voltage magnitude and active power generation in WF emulators, consequently, do not change during the fault. Compared to the onshore converter I side fault, the dc voltage in this case will stay in a lower level since the active power increase of the healthy converter is achieve by dc voltage control instead of dc voltage margin control.

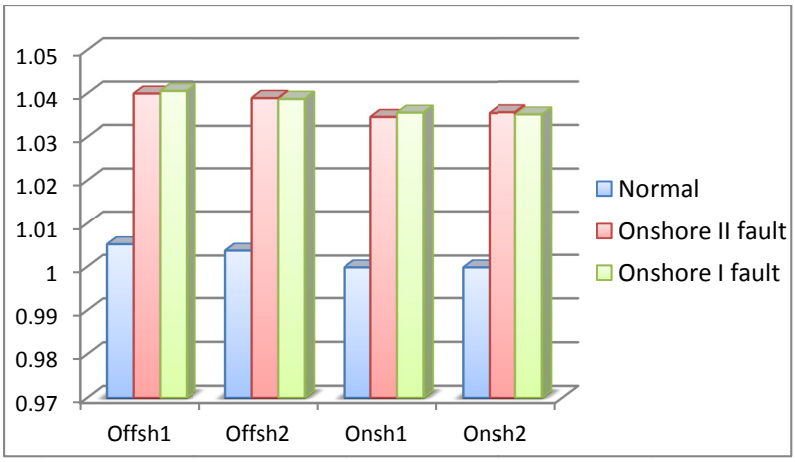
2) Onshore converter I has insufficient power capacity (case 2)

If onshore converter I does not have sufficient power capacity to deal with active power drop caused by SLG fault, WF emulators need to reduce their power generation, as shown in Figure 6-21. Compared to onshore converter I side fault, the dc voltage variation in this case is almost the same, and active power generation drop is also contributed by WF emulator II alone. Because of the lower power increase of the healthy onshore converter, the AC voltage magnitude reduction in PCC_2 is slightly larger in this case, which induces a little higher active power drop (0.0269 pu v. s. 0.0232 pu).

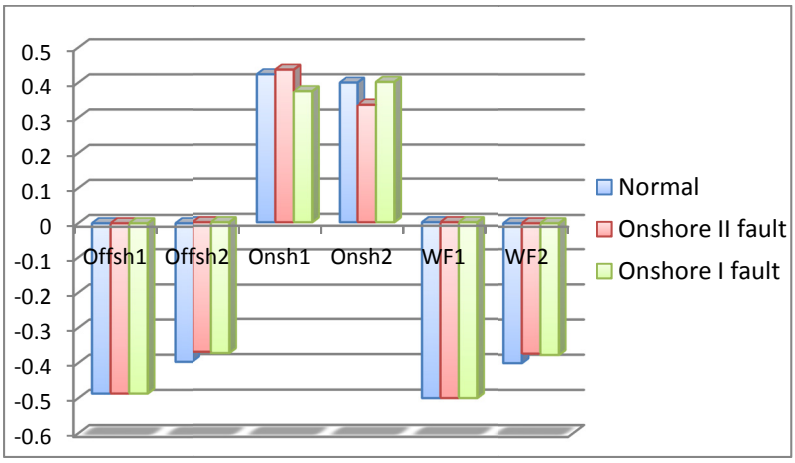
B. q axis current has higher priority (case 3)

Figure 6-22 presents system performance when q axis current has higher priority. Due to power losses of the MTDC system, onshore converter I has higher available power capacity, hence a lower active power drop during SLG fault (0.104 pu) if compared to this case (0.1753 pu). The more severe power unbalance, therefore, results in a higher dc voltage increase in onshore converter II side SLG fault. Through the operation of cascaded droop control, a lower ac voltage magnitude is generated, which in turn enables less active power generation in WF emulator II. Although ac voltage magnitude also reduces in PCC_1, it still stays inside of the dead-band of v_{ac}-P droop curve, and no active power drop is created in WF emulator I.

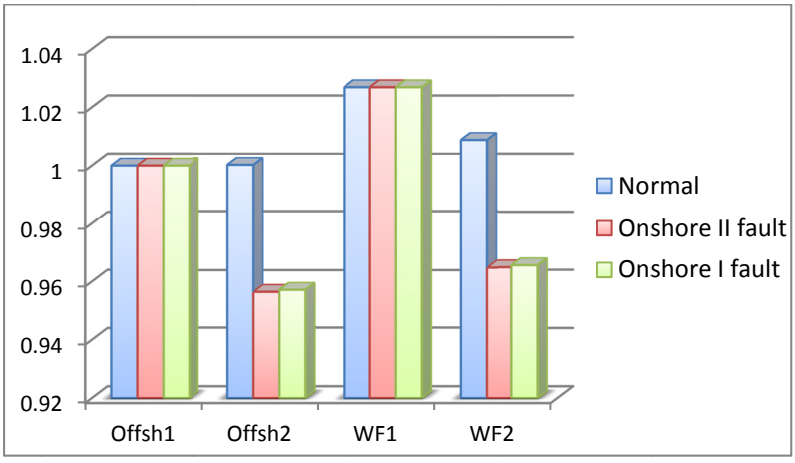
For a better comparison, system performance in the above three cases during onshore converter II side fault are summarized in Figure 6-23. The successful dc voltage regulation of onshore I enables the lowest dc terminal voltages in case 1. In addition, no active power and ac voltage magnitude variation is observed in offshore converters and WF emulators. For the other two cases, dc voltages can be suppressed to below1.05 pu as expected, and the highest overvoltage occurs in case 3 when i_q has higher priority.



(a) DC voltage

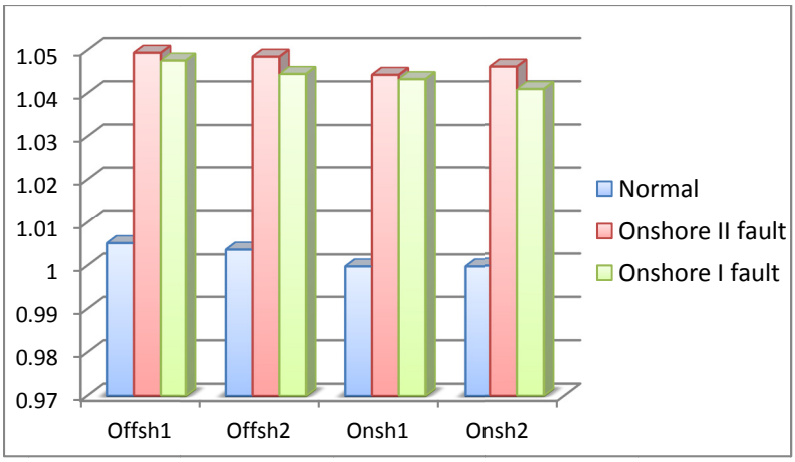


(b) Active power

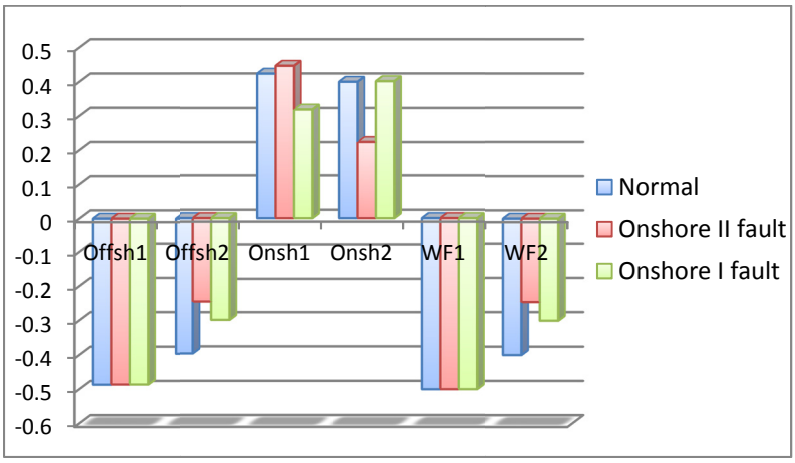


(c) AC voltage magnitude

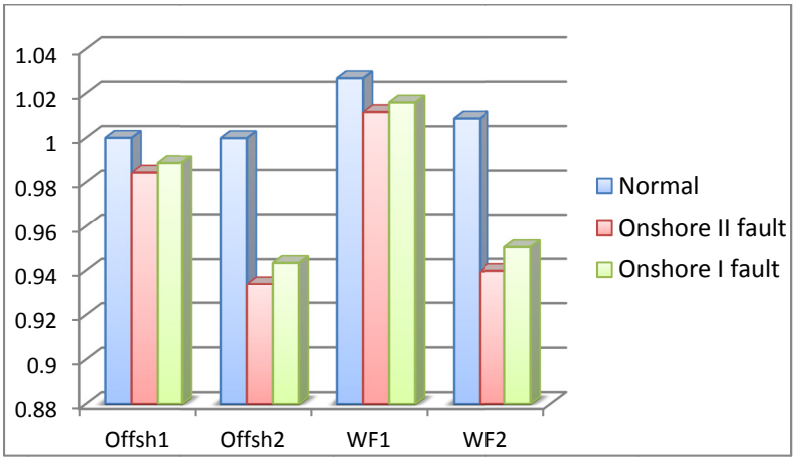
Figure 6-21. Performance comparison when i_d has higher priority and healthy converter has insufficient power capacity.



(a) DC voltage

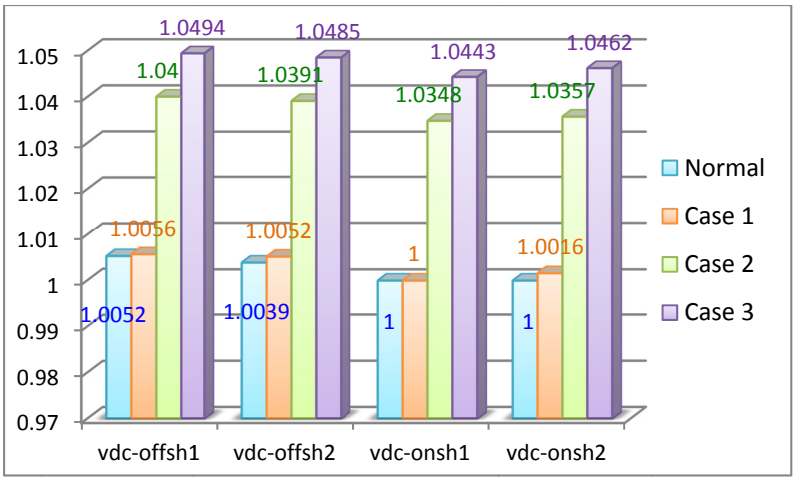


(b) Active power

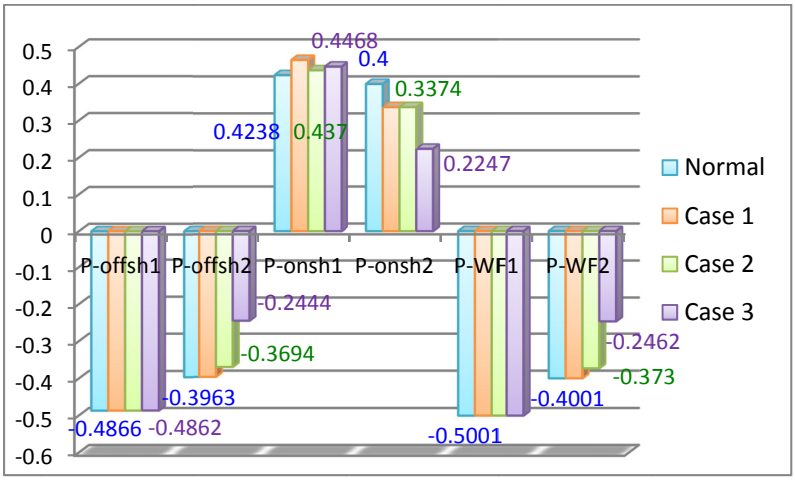


(c) AC voltage magnitude

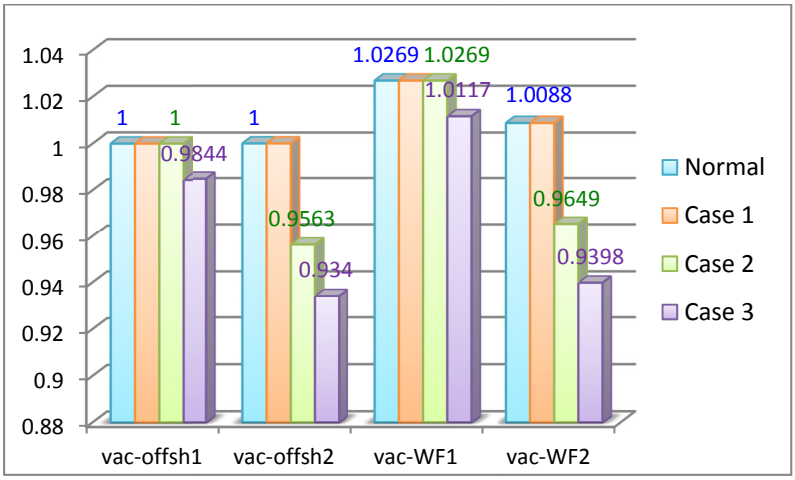
Figure 6-22. Performance comparison when i_q has higher priority and healthy converter has insufficient power capacity.



(a) DC voltage



(b) Active power



(c) AC voltage magnitude

Figure 6-23. Performance comparison between three studied cases.

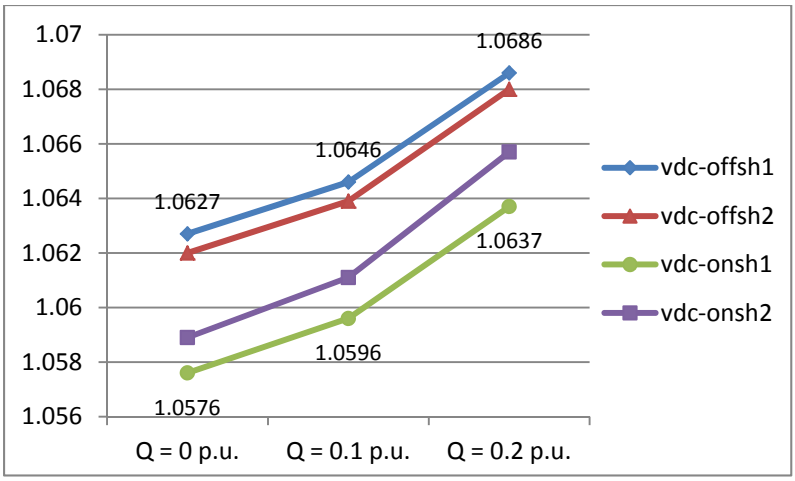
Corresponding to the dc voltage increase, ac voltage magnitude in PCC1 and PCC2 tends to decrease. However, due to higher transformer leakage impedance, the voltage magnitude in PCC1 stays inside the dead-band, leading to an unchanged active power in WF emulator I for all three cases. On the contrary, the dc voltage increase induces an obvious ac voltage collapse and thus active power drop in case 2 (0.027 pu) and case 3 (0.1538 pu) in WF emulator II.

In summary, the active power generation should equal to absorption at any time, otherwise dc voltage will increase and threaten the insulation of the MTDC system during an onshore converter side SLG fault. If the healthy onshore converter station has sufficient power capacity, dc voltage can be regulated to a relatively low level by absorbing more power through dc voltage control or margin control. Otherwise, active power generation will be reduced by a cascaded droop control. The steady state operation point during a SLG fault, however, varies a lot with different fault locations, system parameters (especially, leakage impedance of ac transformers) and droop curves (initial points, droop constant and dead-band).

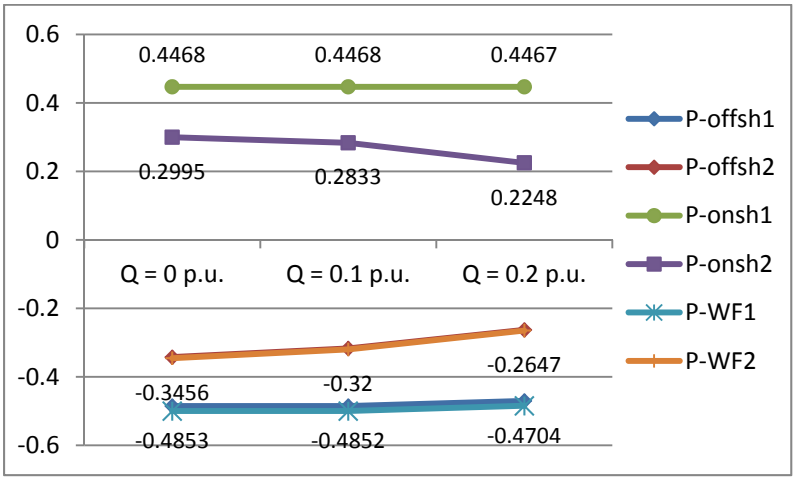
6.3.2 Different Reactive Power Requirement

Having the highest dc voltage increase, case 3 (q axis current has higher priority and the healthy onshore converter does not have sufficient power capacity) in onshore converter II side SLG fault is selected as the base scenario, and all the following analysis is presented based on it.

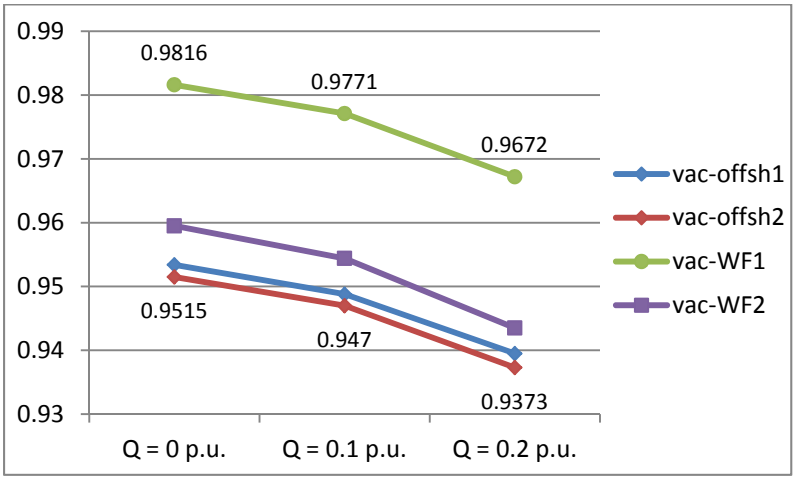
The impact of reactive power requirement is illustrated in Figure 6-24. With reactive power maintained, its active power absorption drops in a nonlinear way ($P = \sqrt{S^2 - Q^2}$), and higher reactive power generation leads to more severe dc voltage increase and active power unbalance. To deal with it, WF emulator I reduces its power output from 0.3456 pu to 0.32 pu and 0.2647 pu when Q_{ref_onsh2} changes from 0 pu to 0.2 pu, while that in WF emulator I does not change until its ac voltage magnitude exceeds the dead-band of v_{ac} - P droop when Q_{ref_onsh2} = 0.2 pu. If ac voltage support is implemented, the reactive power supply will be much higher during SLG fault conditions, which may completely interrupt the active power transfer and induces unacceptable dc overvoltage. Therefore, for a better understanding, the impact of system and droop parameters is studied in the following sections.



(a) DC voltage



(b) Active power



(c) AC voltage magnitude

Figure 6-24. Performance change with different reactive power requirements.

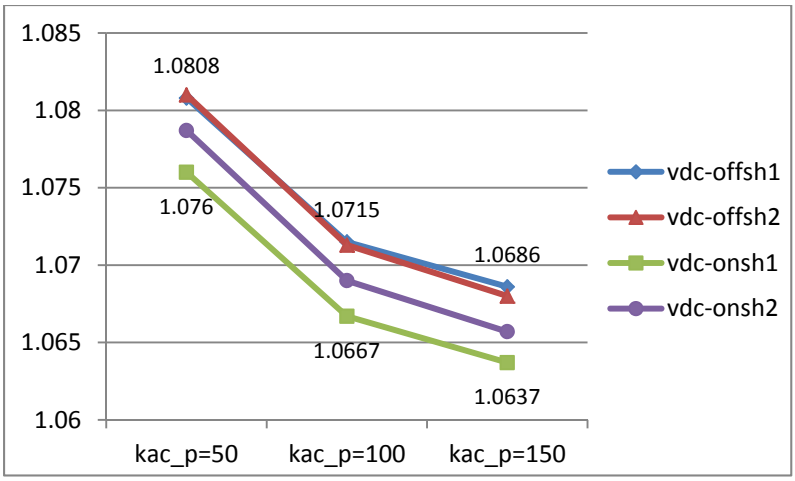
6.3.3 Impact of Droop Constant

Figure 6-25 illustrates the impact of K_{ac_p} (droop constant of v_{ac} - P droop) on system performance when K_{dc_ac} = 1 (droop constant of $v_{dc} - v_{ac}$ droop). A K_{ac_p} of 50 means 1 V ac voltage magnitude drop will causes 50 W active power reduction of WF emulator in the scalded-down system.

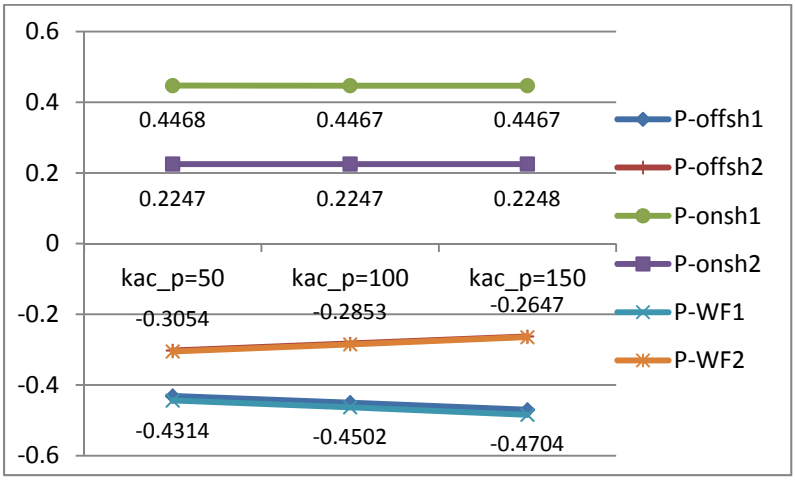
As shown in Figure 6-25, dc voltage in offshore converter I decreases from 1.0808 pu to 1.0686 pu when K_{ac_p} increases from 50 to 150. Consequentially, the ac voltage magnitude drop in WF side reduces and tends to deactivate the v_{ac} - P droop control after K_{ac_p} becomes larger than 150. In contrast, with the selected droop curve and leakage impedance of the ac transformer, the ac voltage magnitude in WF emulator II always exceeds the dead-band (0.035 pu), which continuously reduces its output power to balance the dc side active power when K_{ac_p} increases. Comparing operation points of WF emulator I and II with different K_{ac_p}, the higher droop constant increases the impact of asymmetrical system parameters and deteriorates the uneven power sharing between them.

Figure 6-26 gives the selected simulation results when K_{ac_p} = 50 and K_{dc_ac} changes from 1 to 3. Compared to dc voltage in Figure 6-25(a), the increase of K_{dc_ac} is more effective in dc overvoltage suppression, which reduces dc voltage from 1.0808 pu to 1.055 pu when K_{dc_ac} increases from 1 to 2, while a double K_{ac_p} leads to a dc voltage of 1.0686 pu According to the $v_{dc} - v_{ac}$ droop curve, ac voltage magnitudes v_d in WF emulator I and II exceed the dead-band range and enable active power generation drop in both WFs. In addition, the larger rated dc voltage value in offshore I leads to an increased v_d in PCC_1 while that in PCC_2 tends to reduce when a higher K_{dc_ac} is applied. Counteracted by the reduced dc voltage, however, the deviation between v_d and its rated value (1 pu) in PCC_1 and PCC_2 does not change much and the active power generation of WFs is nearly constant when K_{dc_ac} increases.

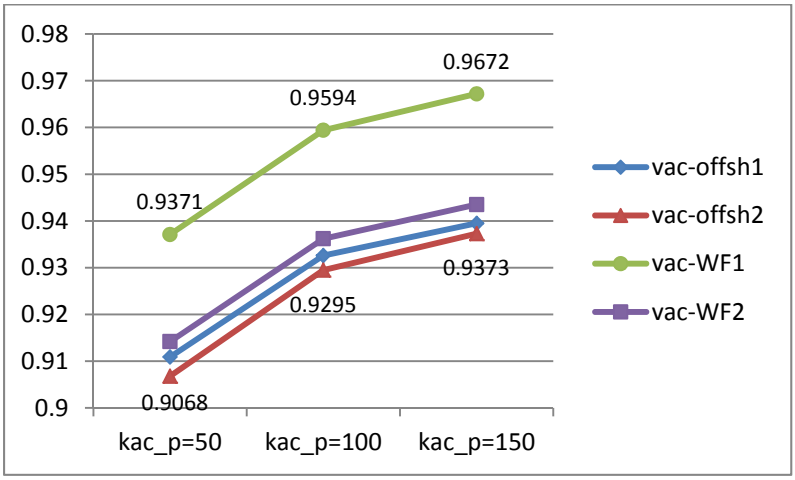
The system performance with different droop constants combination is also studied in Figure 6-27, when $K_{dc_ac} \times K_{ac_p}$ =150. Affected by the dead-band and ac voltage variation before and after the transformer, the cascaded droop control is not equivalent to a single v_{dc} - p_{dc} droop, and distinct dc voltage deviation can be observed in Figure 6-27(a).



(a) DC voltage

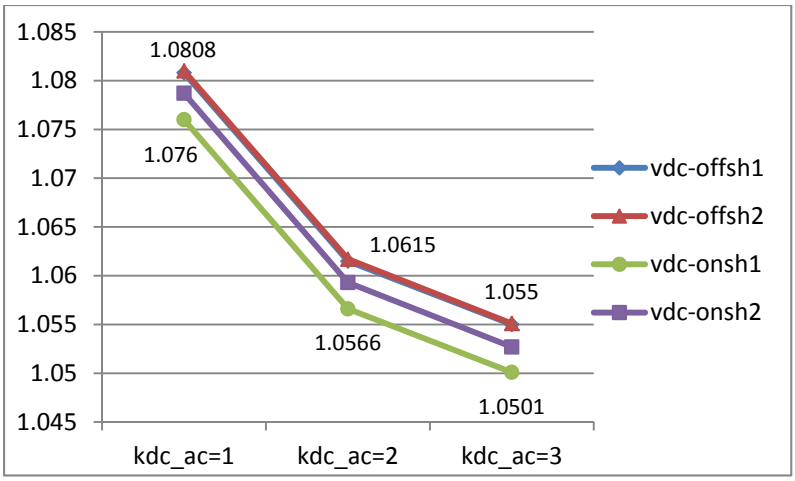


(b) Active power

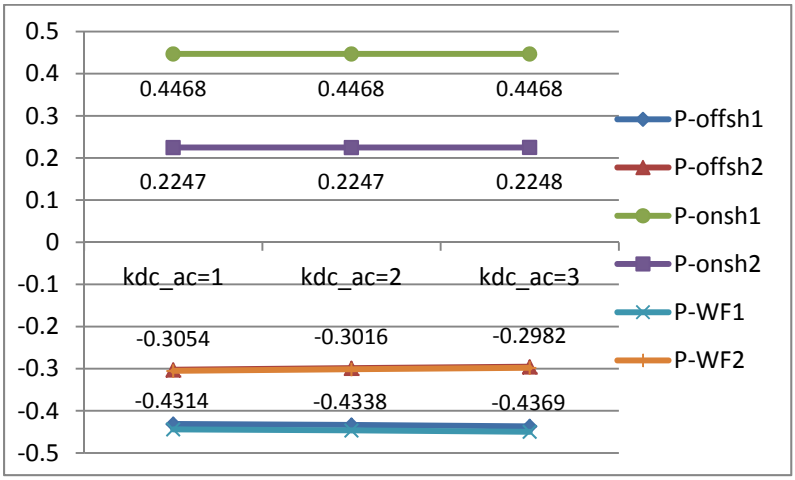


(c) AC voltage magnitude

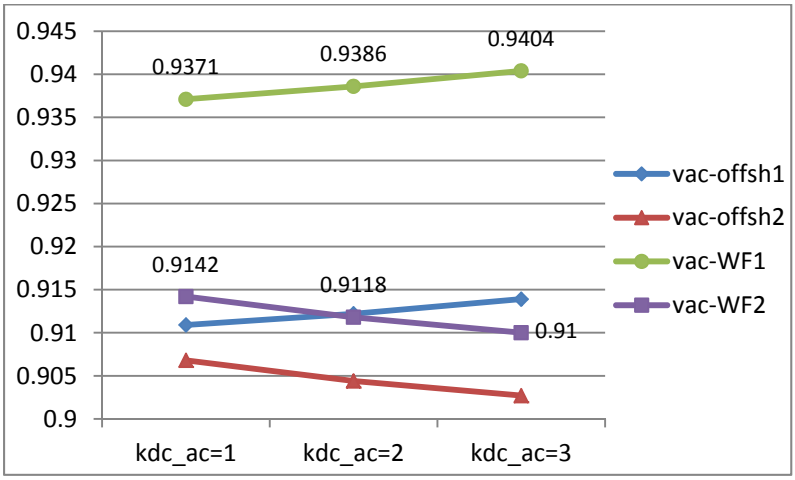
Figure 6-25. Performance with different droop constants in v_{ac} - P droop control.



(a) DC voltage

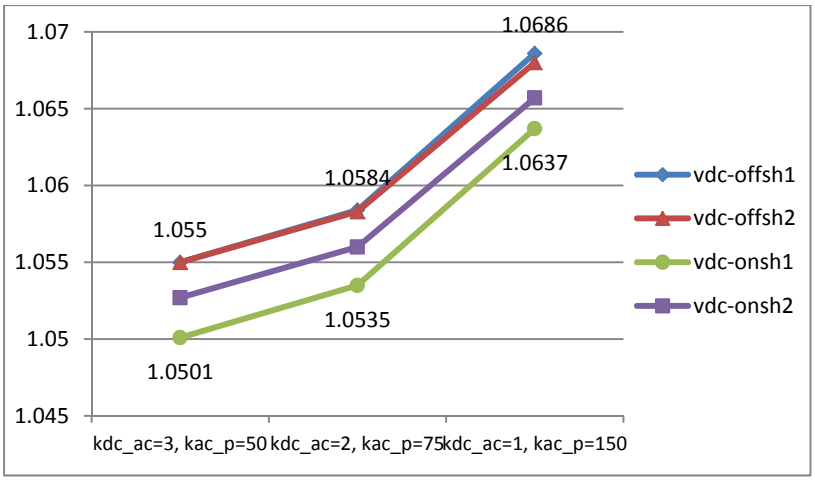


(b) Active power

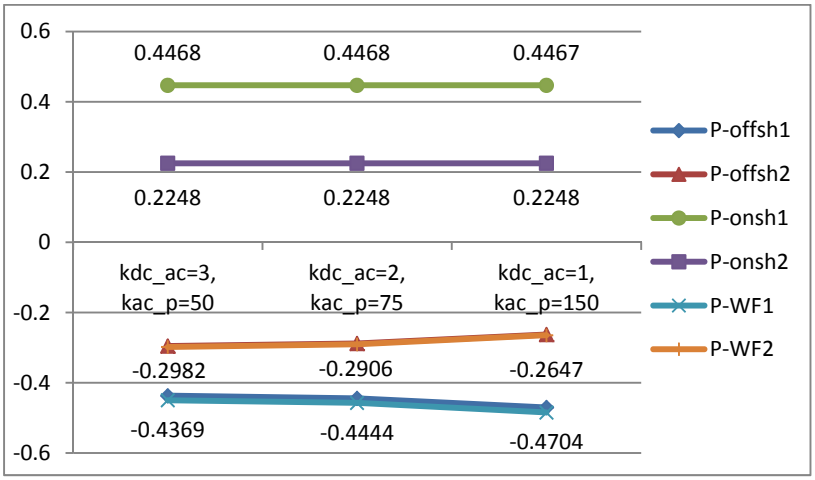


(c) AC voltage magnitude

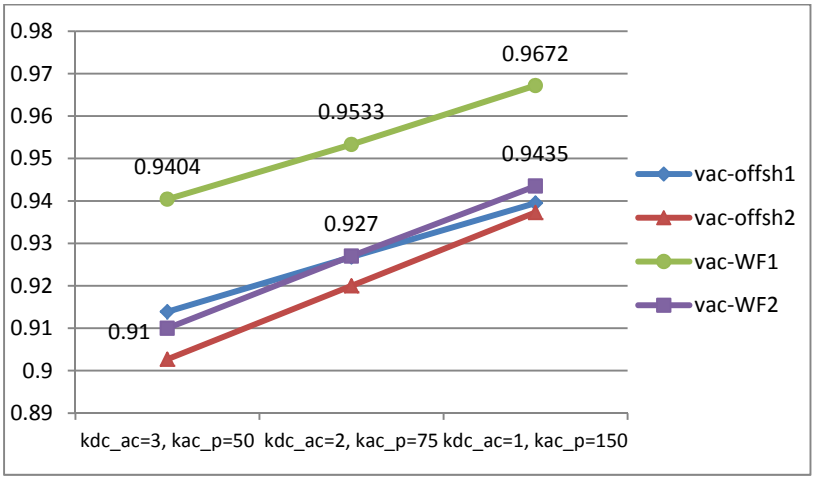
Figure 6-26. Performance with different droop constants in v_{dc} - v_{ac} droop control.



(a) DC voltage



(b) Active power



(c) AC voltage magnitude

Figure 6-27. Performance with different combination of droop constants.

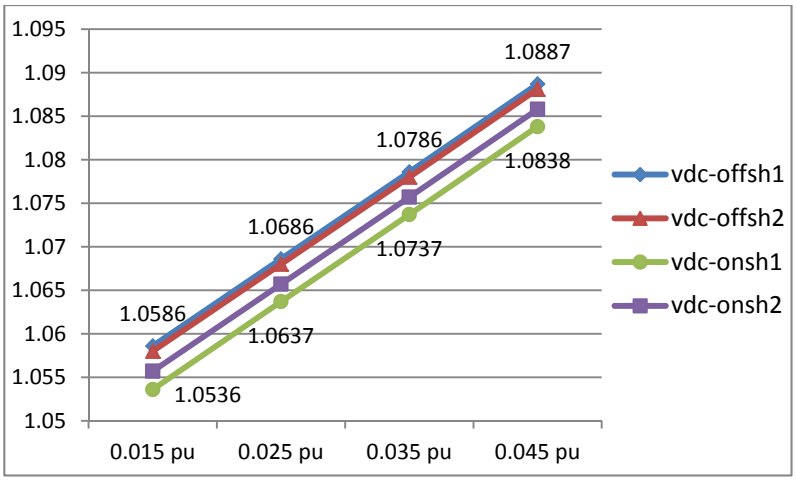
The increase of K_{dc_ac} presents a higher effectiveness to suppress dc overvoltage during a SLG fault, while it results in a more obvious ac voltage magnitude variation in PCC points (Figure 6-27(c)). Same as the previous cases, due to the larger transformer leakage impedance, WF emulator II takes the main responsibility of dc voltage regulation and drops more active power during a SLG fault if compared to WF emulator I.

As observed from Figure 6-27(b), the power sharing between the two WF emulators becomes more uneven when K_{dc_ac} decreases and K_{ac_P} increases. This is caused by the leakage inductance and dead-band of $v_{ac} - P$ droop. With lower K_{dc_ac}, the ac voltages in both PCC_1 and PCC_2 get less sensitive to dc voltage variation, and v_d in WF emulator I, especially, nearly goes inside the dead-band when K_{dc_ac} reduces from 3 to 1, which enables an increased active power generation although the K_{ac_P} rises correspondingly. In contrast, v_d in WF emulator II stays far away from the dead-band, and its output power keeps reducing when K_{ac_P} increases.

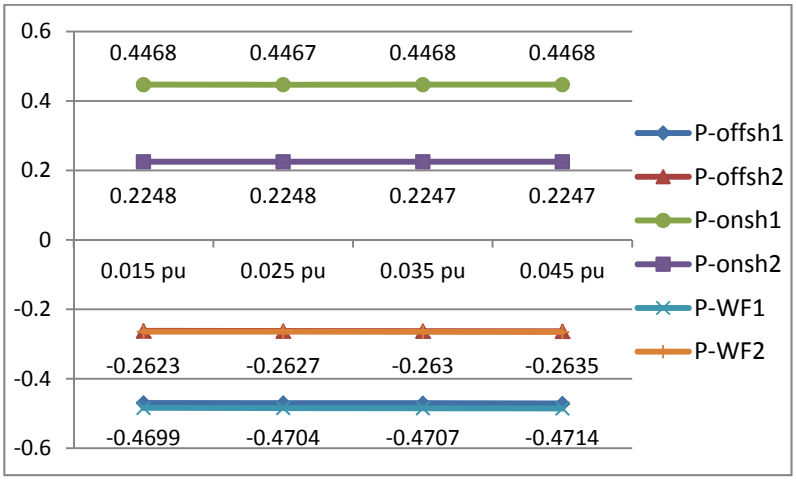
6.3.4 Impact of Dead-band

The impact of dead-band in $v_{dc} - v_{ac}$ droop control is given in Figure 6-28. Only when the dc voltage deviation (v_{dc} - $V_{dcrated}$) is higher than the selected dead-band ΔV_{dc}, the reference of ac voltage magnitude in offshore converter starts to change according to the designed droop curve. As shown in Figure 6-28(a), the dc voltage deviation is positive proportional to ΔV_{dc}. Take offshore converter I for instance, a dc voltage derivation around 0.01 pu is found when ΔV_{dc} increases from 0.015 pu to 0.045 pu This linear relationship, consequently, results in almost constant ac voltage magnitude (Figure 6-28(c)) and active power generation in both WF emulators.

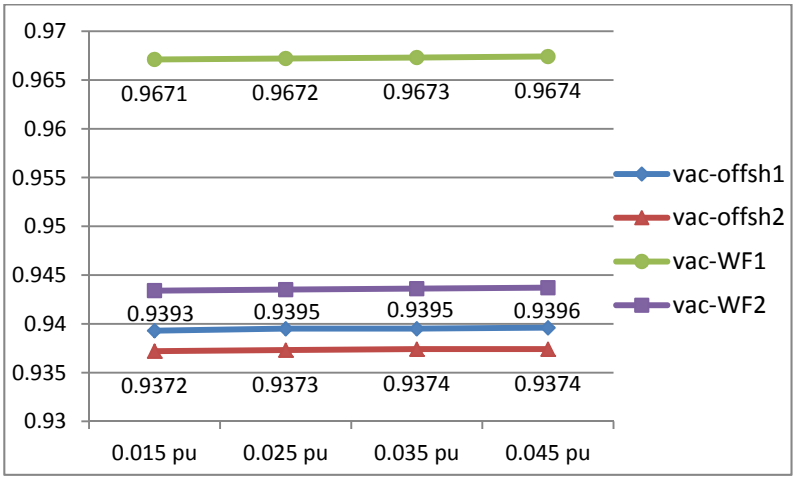
The impact of dead-band in $v_{ac} - P$ droop control ΔV_{ac} is also studied in Figure 6-29, with $\Delta V_{dc} = 0.025$ pu Compared to ΔV_{dc}, ΔV_{ac} with the same pu value enables a generally lower dc voltage during SLG fault, and its increase leads to a smaller dc voltage variation. For example, the dc voltage of onshore I rises from 1.0586 pu to 1.0887 pu when ΔV_{dc} grows from 0.015 pu to 0.045 pu (Figure 6-28(a)), while the same increase of ΔV_{ac} leads to a dc voltage change from 1.0598 pu to 1.0728 pu in Figure 6-29(a).



(a) DC voltage

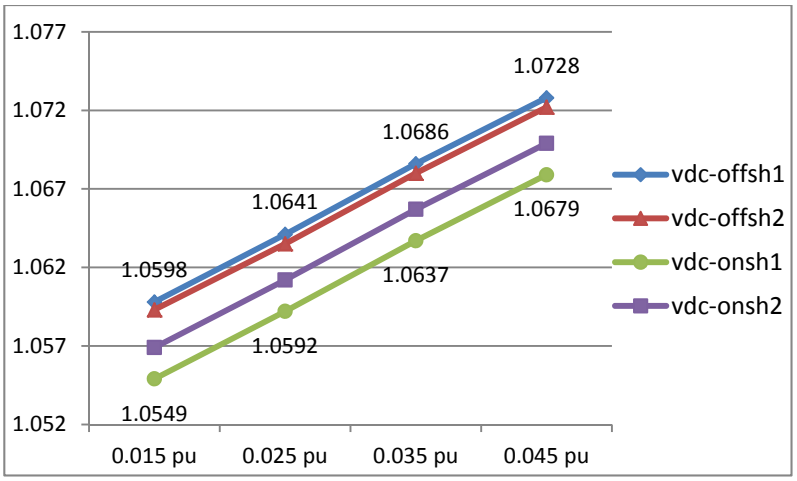


(b) Active power

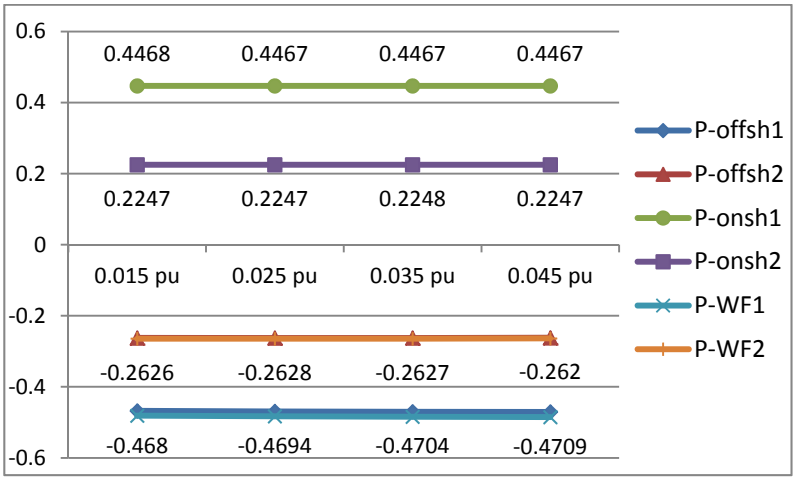


(c) AC voltage magnitude

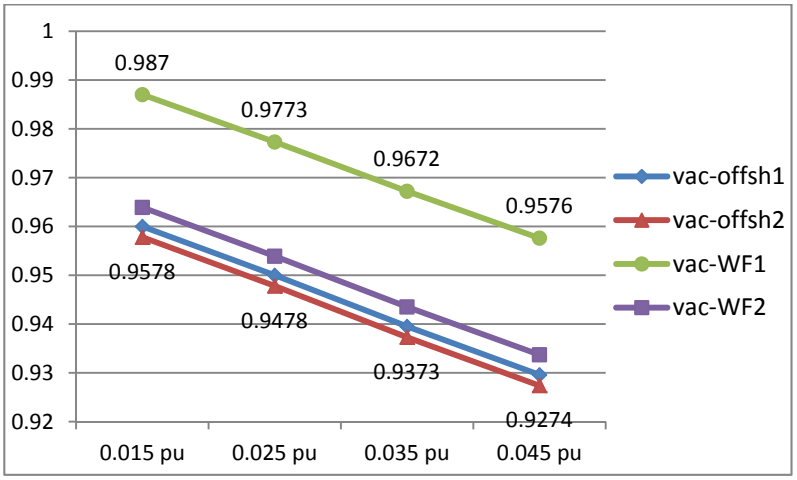
Figure 6-28. Performance with different dead-bands in v_{dc} - v_{ac} droop when Z_{lk_WF1} = 0.05 pu.



(a) DC voltage



(b) Active power



(c) AC voltage magnitude

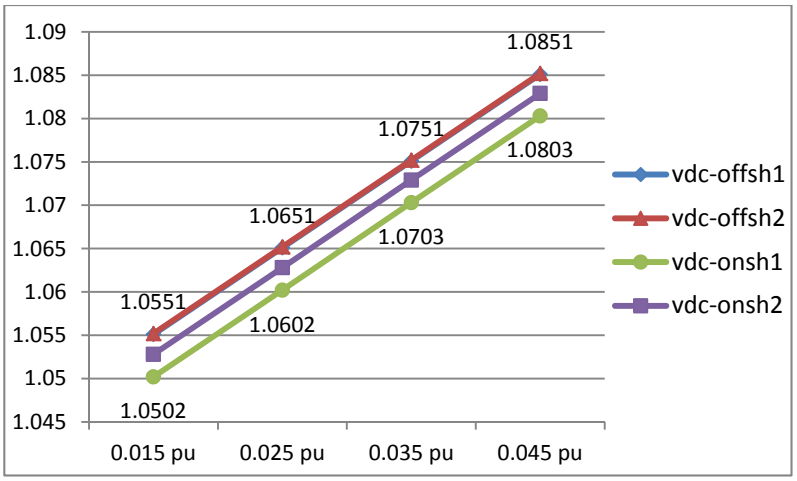
Figure 6-29. Performance with different dead-bands in v_{ac} - P droop when Z_{lk_WF1} = 0.05 pu.

Corresponding to the dc voltage increase, the ac voltage magnitude in both PCC_1 and PCC_2 keep dropping when ΔV_{ac} grows. The active power generation, on the other hand, does not change much. As mentioned before, the ac voltage magnitude in WF emulator I is 1.0269 pu under normal operation condition. If ΔV_{ac} is lower than 0.0269 pu, the $v_{ac} - P$ droop will be triggered all the time and the desired constant power generation will be interrupted.

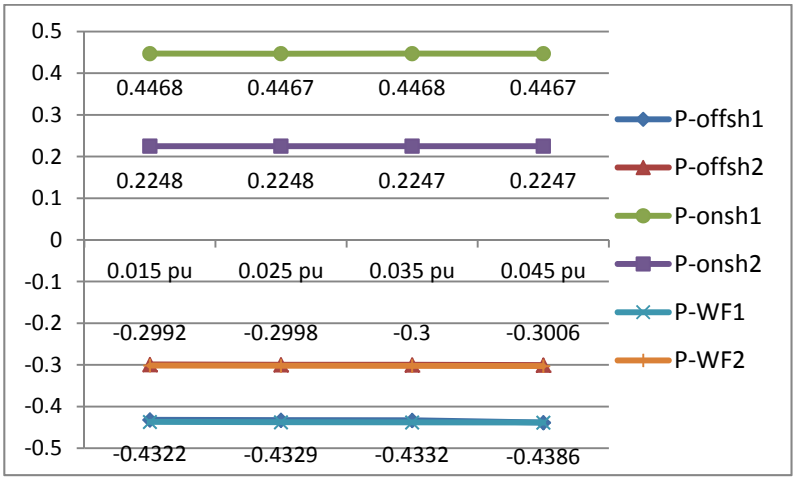
Although no obvious abnormal operation can be found in Figure 6-29 during SLG fault, the active power generated by WF emulator I deviates from its reference of 0.5 pu to 0.5423 pu under normal condition, which induces dc voltage of 1.021 pu and 1.0197 pu in offshore converter I and II (normally is 1.0052 pu and 1.0038 pu). Therefore, ΔV_{ac} should be selected carefully to avoid the undesired performance mentioned above.

To avoid the uneven power sharing introduced by asymmetrical leakage impedance of ac transformers in WF emulator I (Z_{lk_WF1}) and II (Z_{lk_WF2}), Z_{lk_WF1} is reduced from 0.05 pu to 0.02 pu, which is the same as Z_{lk_WF2}. The system performance with different v_{dc} - v_{ac} droop and v_{ac} - P droop dead-band settings is given in Figure 6-30 and Figure 6-31, respectively. Similar as Figure 6-28(a), the dc voltage deviation still presents a linear relationship with the dead-band increase, and ac voltage magnitudes as well as the active power generation of WFs are almost constant in Figure 6-30(b) and (c). However, the lower transformer impedance in offshore I enables a smaller dc overvoltage (maximum value of 1.0887 pu in Figure 6-28(a) and 1.0851 pu in Figure 6-30(a)) and higher ac voltage magnitude v_d (minimum value of 0.9372 pu in Figure 6-28(c) and 0.9437 pu in Figure 6-30(c)) during the SLG fault.

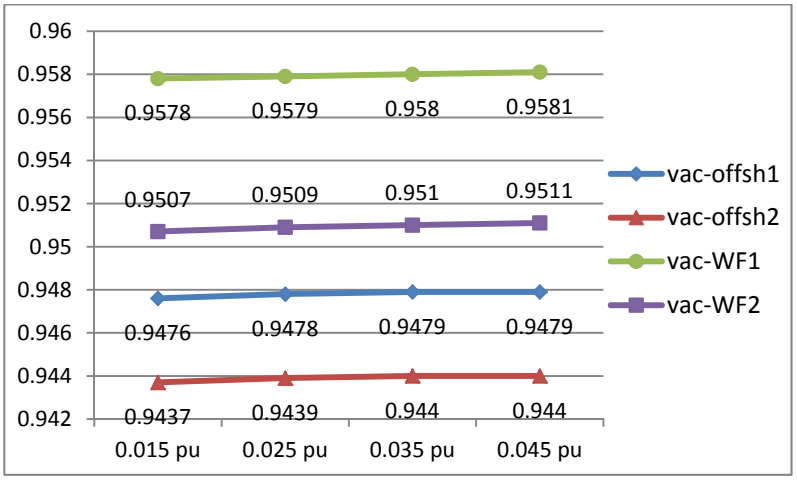
Moreover, compared to Figure 6-28, the reduced ac voltage difference between WF emulators leads to a more even power sharing. Take ΔV_{dc} = 0.015 pu for instance, the steady state active power transfer for offshore converter I and II are -0.4322 pu and -0.2992 pu in this case, while those for Z_{lk_off1} = 0.05 pu are -0.4699 pu and -0.2623 pu The active power sharing between WFs can be further improved by setting the same rated dc voltage or using additional power sharing control schemes, such as active power reference adjustment of WFs with slow communication.



(a) DC voltage

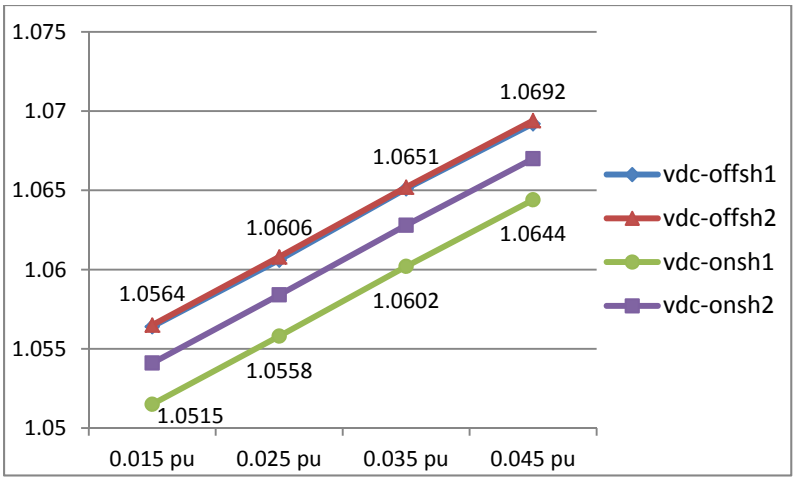


(b) Active power

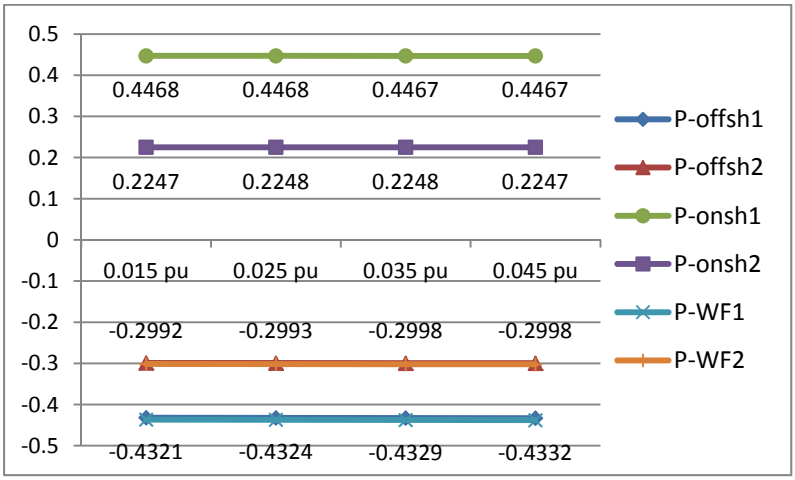


(c) AC voltage magnitude

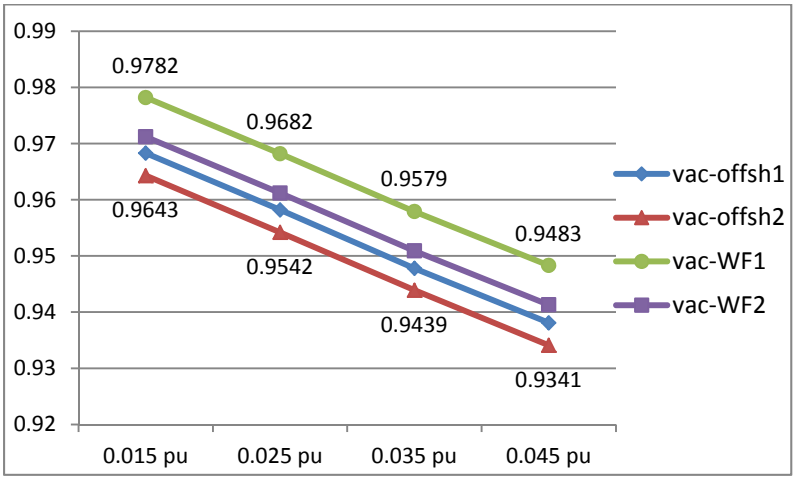
Figure 6-30. Performance with different dead-bands in v_{dc} - v_{ac} droop when Z_{lk_WF1} = 0.02 pu.



(a) DC voltage



(b) Active power



(c) AC voltage magnitude

Figure 6-31. Performance with different dead-band in v_{ac} - P droop when Z_{lk_WF1} = 0.02 pu.

The same variation trend can also be found in Figure 6-31, where the dead-band of $v_{ac} - P$ droop increases from 0.015 pu to 0.045 pu After leakage impedance of transformer in offshore converter I decreases from 0.05 pu to 0.02 pu, the dc overvoltage and WF side ac voltage magnitude during SLG fault have obvious reductions. In addition, compared to Figure 6-29, WF emulator I takes more responsibility for dc voltage regulation, which drops more active power.

Thus, the steady state operation point of MTDC system under SLG fault will be significantly affected by system parameters and the selected droop curves. By increasing the droop constants and decreasing the dead-band of either $v_{dc} - v_{ac}$ droop or v_{ac} – P droop, the dc voltage increase can be mitigated through faster active power regulation, which is similar to the traditional v_{dc} - P droop. Nevertheless, they are not exactly the same, especially when the dead-band ΔV_{ac} and/or ac voltage magnitude deviation caused by ac transformers is large. With such setting, the increased droop constant K_{ac_p} presents a higher effectiveness than K_{dc_ac} on the dc overvoltage regulation. The ac voltage magnitude, however, will drop to a lower value to realize the same active power reduction.

Uneven power sharing between two WF emulators will also be introduced if droop curves and system parameters are not the same. The one with higher droop constant, lower dead-band, smaller rated voltage and less ac transformer leakage impedance will take the main responsibility of dc voltage regulation, and supply a more sensitive active power variation.

6.4 Experimental Verification

In order to verify the analysis and simulation results, a scaled-down four-terminal HVDC prototype is built, as shown in Figure 6-32. As the first step, two-level converters are employed for system level control strategy verification, and parameters of the scaled-down system are calculated and given in Table 6-1, by keeping the same per unit value as that in the real system. Initially, dc cables are emulated by series connected inductance and resistance only. The communication structure is shown in Figure 6-33. Through NI Labview, online control comments (e.g., operation mode, voltage, active and reactive power reference) modification and real time display are available with a time interval of 0.1 s. The control

comments are sent from Labview (COM1 and COM2) to the system controller (TMS320F28335) through RS232, and then distributed to local controllers through CAN bus. Data collection from local converters to Labview is realized in the reverse manner. Using communication through Ethernet, the control comments can also be sent remotely by Labview (COM3) far away from the hardware platform, which supplies an easy way to embed the MTDC network into a large scale system.



Figure 6-32. Four -terminal HVDC platform.

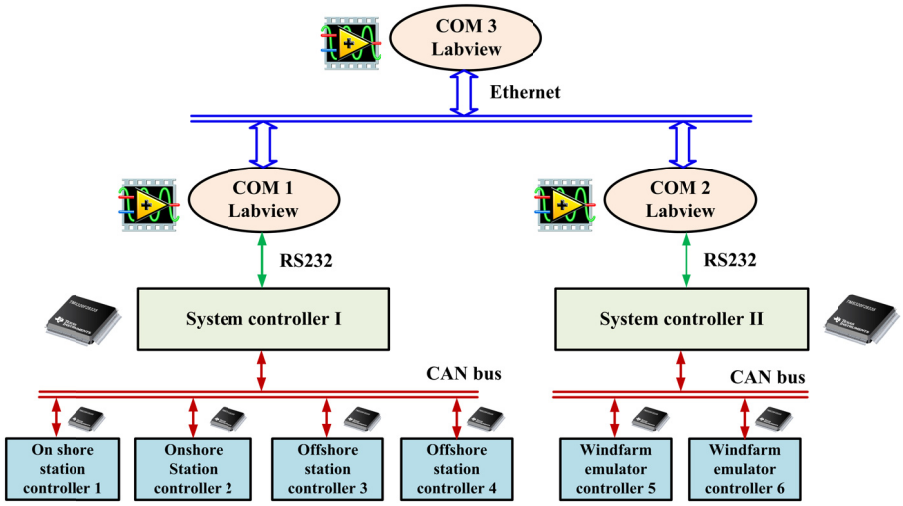


Figure 6-33. Communication structure of the four-terminal HVDC platform.

The same scenarios studied in simulation are tested in the scaled-down MTDC system. The SLG fault in onshore converters is emulated by a programmable ac voltage source, and system behavior is recorded by the data exported from Labview. Moreover, the steady state voltage and power in experiments during SLG fault will be compared with calculated values obtained from the proposed power flow calculation.

6.4.1 SLG Fault in Onshore Converter I

A. d axis current has higher priority

1) Onshore converter II has sufficient power capacity (case 1)

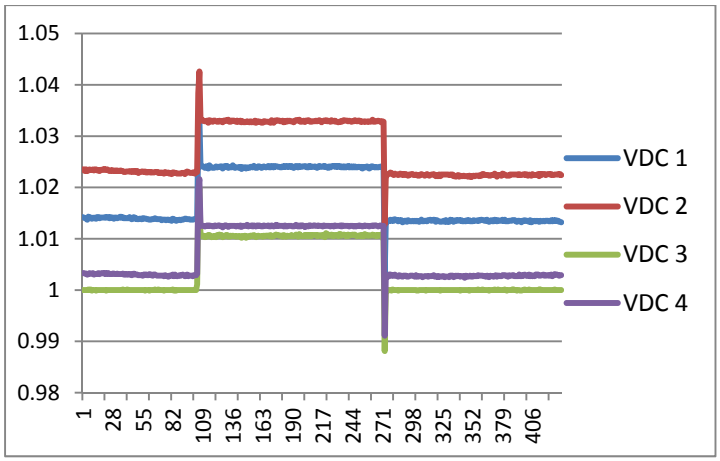
As mentioned in Section 5.3.1, the onshore converter II will take full responsibility of dc voltage regulation during SLG fault, and the operation mode transition of each converter displayed by Labview is recorded in Table 6-5. The x axis shows the data number, and 10 data represents 1 s.

Table 6-5. Operation mode transition in case 1 with onshore I side SLG fault.

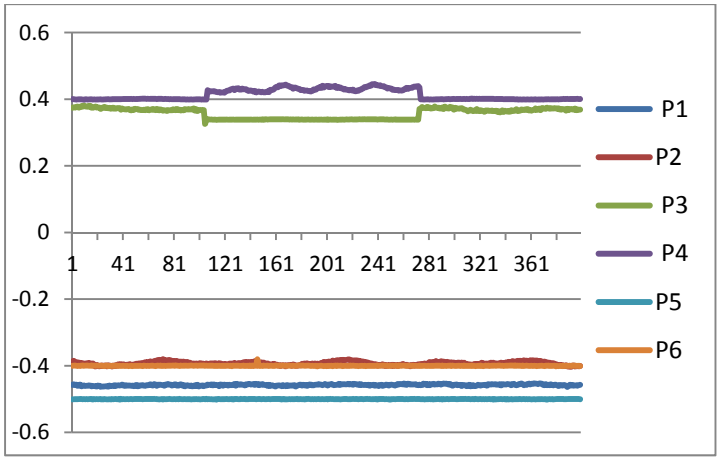
	Offshore I (VSC1)	Offshore II (VSC2)	Onshore I (VSC3)	Onshore II (VSC4)	WF Emulator I (VSC5)	WF Emulator II (VSC6)
Before fault	Vac-f	Vac-f	**VdcQ**	**PQ**	PQ	PQ
After fault	Vac-f	Vac-f	**P limit**	**DC voltage margin**	PQ	PQ

Through the dc voltage margin control, the dc terminal voltage in onshore II is controlled to 1.0125 pu after fault, and the maximum dc voltage occurs in offshore II, which is 1.0228 pu under normal operation and 1.0328 pu after fault, as shown in Figure 6-34(a). The onshore II completely compensates the active power unbalance, and power generation in WF emulators does not change (Figure 6-34(b)). In addition, reactive power generated by offshore II drops to zero for active power support, and a little reactive power is supported by offshore converters for ac voltage regulation ($v_{qref} = 0$) (Figure 6-34(c)).

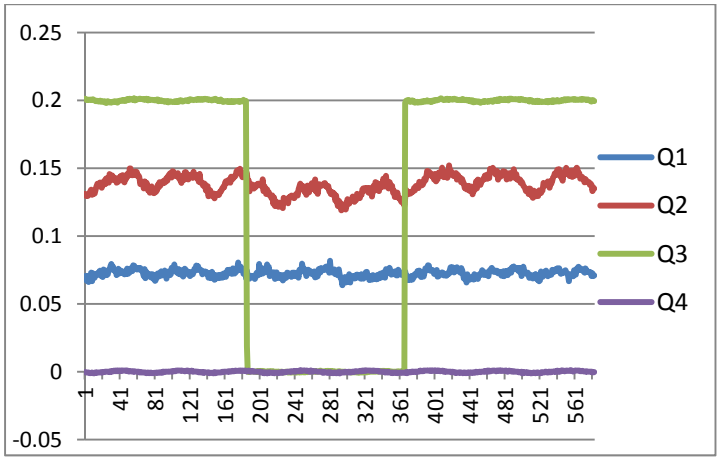
Due to leakage impedances of the ac transformer, which are about 0.04 pu and 0.01 pu in offshore I and II, noticeable active power losses can be found, and RMS value of ac voltage in WF I (v_{ac5}) and WF II (v_{ac6}) deviate from their rated values. v_{ac5}, especially, is boosted to 1.022 pu (Figure 6-34(d)).



(a) DC voltage of onshore and offshore converters

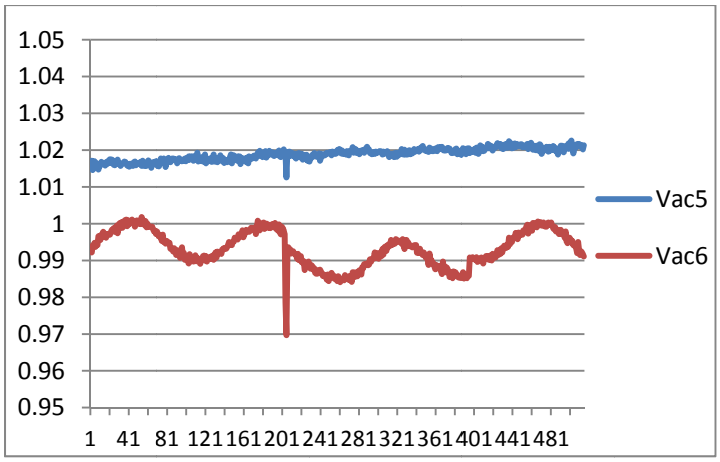


(b) Active power



(c) Reactive power of onshore and offshore converters

Figure 6-34. Experimental results in case 1 with onshore I side SLG fault.



(d) Ac voltage magnitude in windfarm emulators

Figure 6-34. Experimental results in case 1 with onshore I side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value.

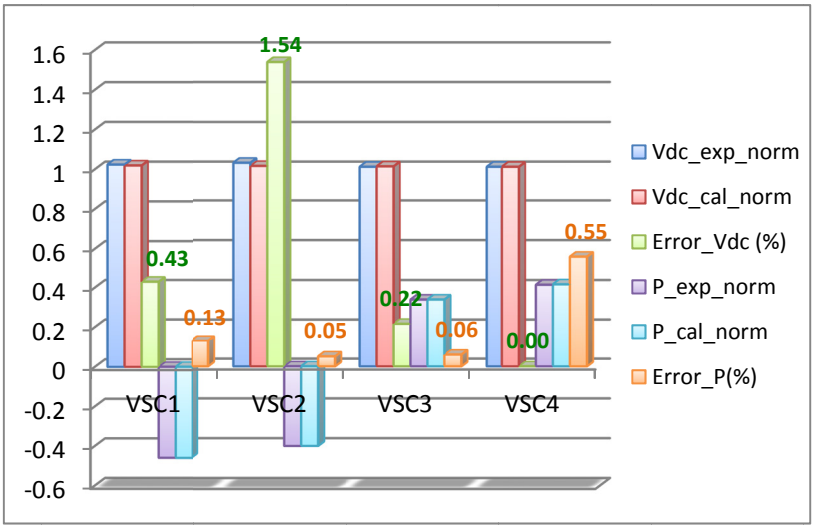


Figure 6-35. Comparison between experimental and calculation results in case 1 with onshore I side fault.

To emulate it, the leakage impedances in simulation are set to 0.05 pu and 0.02 pu respectively. The low frequency ripple appears in v_{ac6} is caused by inaccurate measurement and RMS calculation. Figure 6-35 gives the comparison between experimental and calculation results in this case. According to the calculation, dc voltage in offshore II should be 1.0047 pu and 1.0169 pu under normal and SLG

conditions, which both are about 1.018 times lower than the experimental results. Therefore, the dc voltage measurement in offshore II is considered to be inaccurate in experiments.

Except for this, errors between experimental and calculation results for all other components are lower than 0.6 %. The active power of onshore converters during fault are assumed to be known parameters and used to calculate other parameters through the power flow analysis. This assumption, however, may not hold due to the neglected power losses and different ac voltage drop during ac faults, thus inducing slight mismatch.

2) Onshore converter II has insufficient power capacity (case 2)

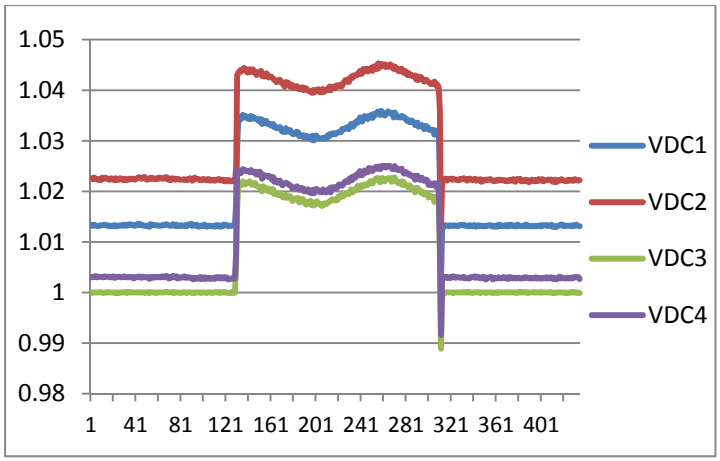
When SLG occurs, onshore II cannot absorb all the active power generated by the WFs, and dc voltage increases. After the offshore converter side dc voltage exceeds the dead-band, $v_{dc} - v_{ac}$ droop control starts and ac voltage magnitude in PCC decreases to trip the $v_{ac} - P$ droop, as shown in Table 6-6.

Same as the simulation results, the high ac voltage magnitude and relatively low dc voltage variation make the $v_{ac} - P$ droop control in WF I difficult to be activated, and WF II has to regulate the dc voltage alone by decreasing its active power. Without a slack bus with constant dc voltage control, the dc terminal voltage of all converters will vary according to droop curves.

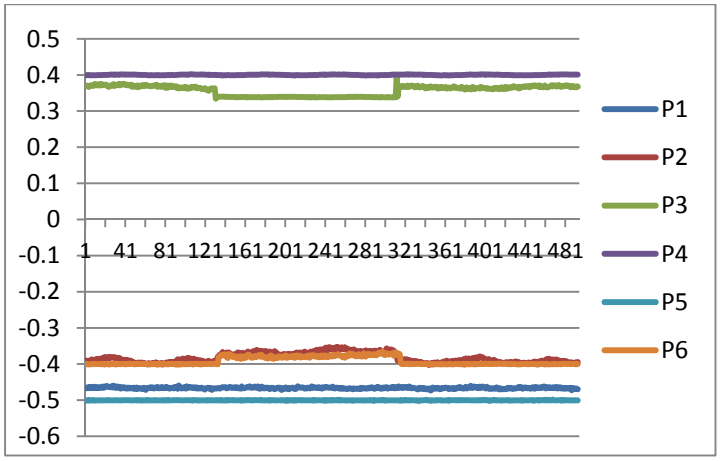
Considering the dead-band and power losses, the calculated values match the experimental results very well except for dc voltage and active power in offshore II. Introduced by the inaccurate dc voltage measurement, the errors of them are 1.88 % and 1.72 %, respectively. Involving the droop control, the calculation error in offshore I also has a slight increase if compared to Figure 6-35.

Table 6-6. Operation mode transition in case 2 with onshore I side SLG fault.

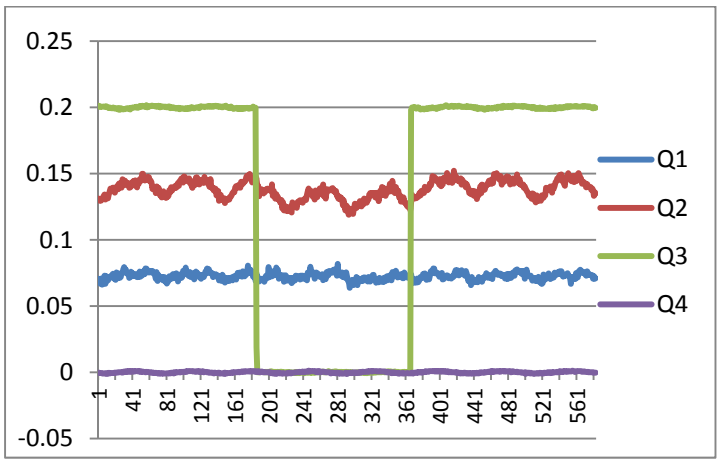
	Offshore I (VSC1)	Offshore II (VSC2)	Onshore I (VSC3)	Onshore II (VSC4)	WF Emulator I (VSC5)	WF Emulator II (VSC6)
Before fault	**Vac-f**	**Vac-f**	**VdcQ**	**PQ**	PQ	**PQ**
After fault	**vdc-vac droop**	**vdc-vac droop**	**P limit**	**P limit**	PQ	**vac-P droop**



(a) DC voltage of onshore and offshore converters

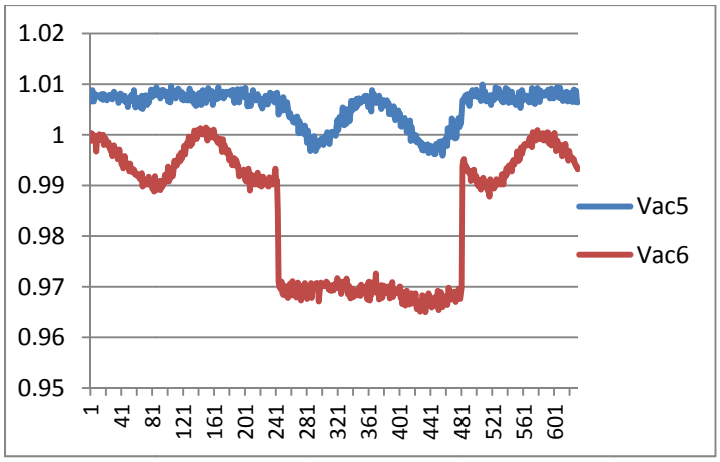


(b) Active power



(c) Reactive power of onshore and offshore converters

Figure 6-36. Experimental results in case 2 with onshore I side SLG fault.



(d) Ac voltage magnitude in windfarm emulators

Figure 6-36. Experimental results in case 2 with onshore I side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value.

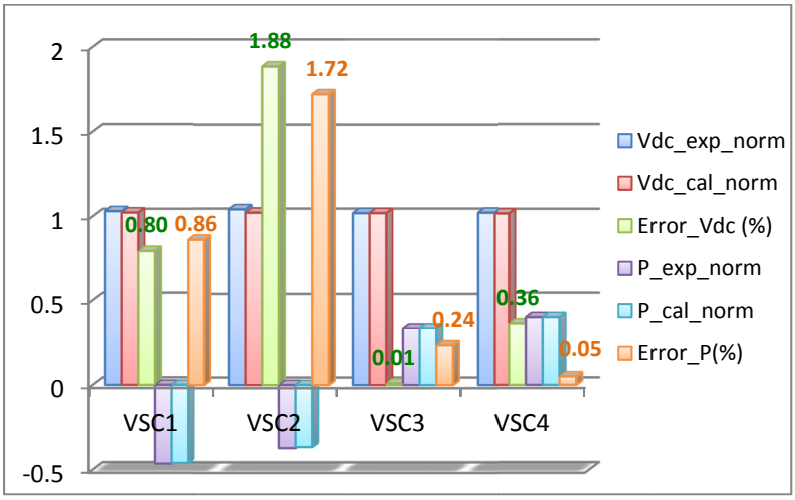


Figure 6-37. Comparison between experimental and calculation results in case 2 with onshore I side fault.

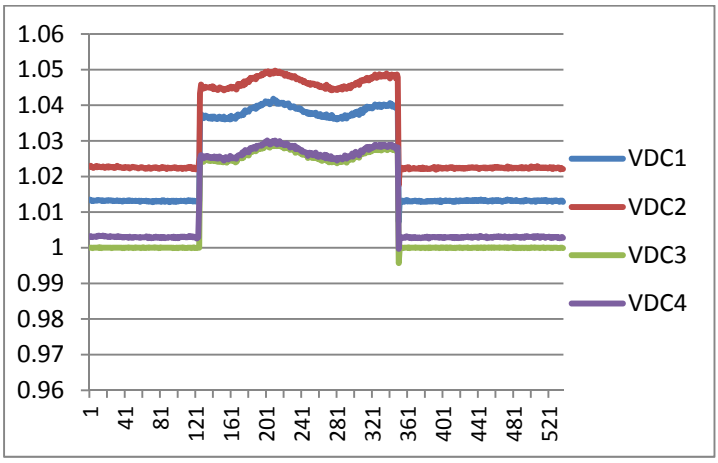
B. q axis current has higher priority (case 3)

If reactive power support instead of active power generation has higher priority during SLG fault, the faulty onshore converter will absorb less power (0.2738 pu in this case, while 0.3392 pu in case 2) and dc voltage will have a further increase (for offshore I: 1.036 pu in this case, while 1.0304 pu in case 2), as illustrated in the experimental results in Figure 6-38. However, the $v_{ac} - P$ droop in WF I is still

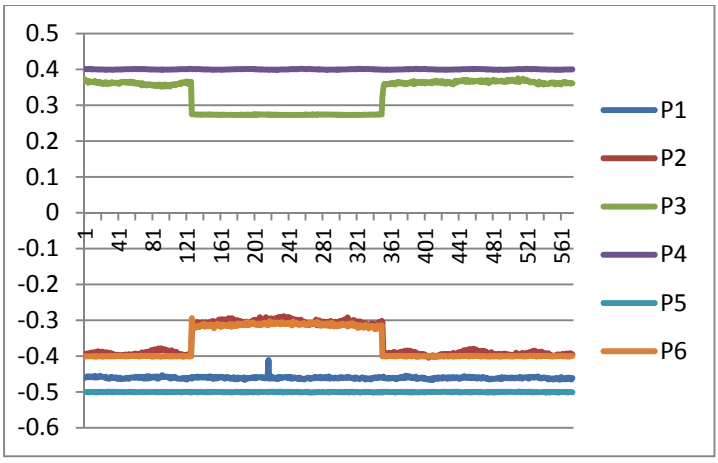
deactivated due to the insufficient ac voltage drop, as given in Table 6-7, and a constant active power is provided all the time.

Table 6-7. Operation mode transition in case 3 with onshore I side SLG fault.

	Offshore I (VSC1)	Offshore II (VSC2)	Onshore I (VSC3)	Onshore II (VSC4)	WF Emulator I (VSC5)	WF Emulator II (VSC6)
Before fault	**Vac-f**	**Vac-f**	**VdcQ**	**PQ**	PQ	**PQ**
After fault	**vdc-vac droop**	**vdc-vac droop**	**P limit**	**P limit**	PQ	**vac-P droop**

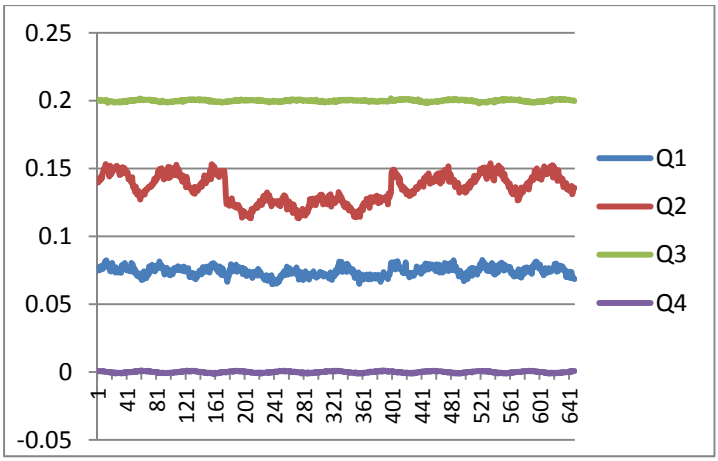


(a) DC voltage of onshore and offshore converters

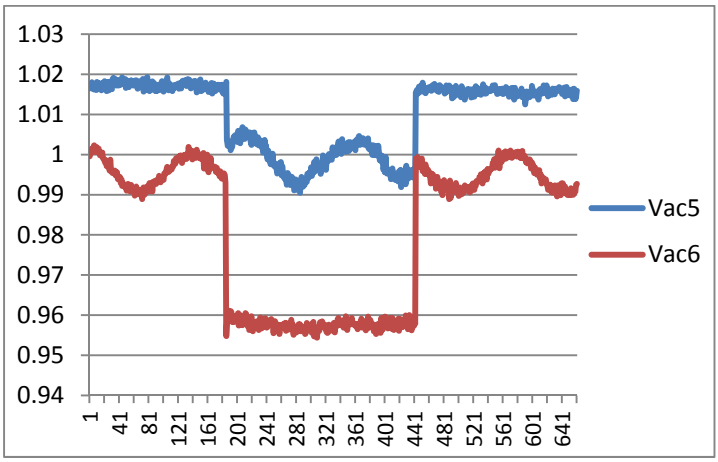


(b) Active power

Figure 6-38. Experimental results in case 3 with onshore I side SLG fault.



(c) Reactive power of onshore and offshore converters



(d) Ac voltage magnitude in windfarm emulators

Figure 6-38. Experimental results in case 3 with onshore I side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value.

In contrast, the larger dc voltage measurement in offshore II induces a higher ac voltage magnitude decrease (~ 0.04 pu, while 0.03 pu in case 2) and thus more active power reduction (~ 0.1 pu, while 0.03 pu in case 2) according to the cascaded droop control. Highly dependent on the droop control, the calculation values deviate from the experimental results in a larger range if compared to Figure 6-37. The dc voltage and active power in offshore II, especially, suffer errors of 2.09 % and 1.56 %, respectively. The mismatch is mainly caused by inaccurate measurement and the assumption of single droop control in the power flow calculation, where the estimated dead-band tends to be inaccurate.

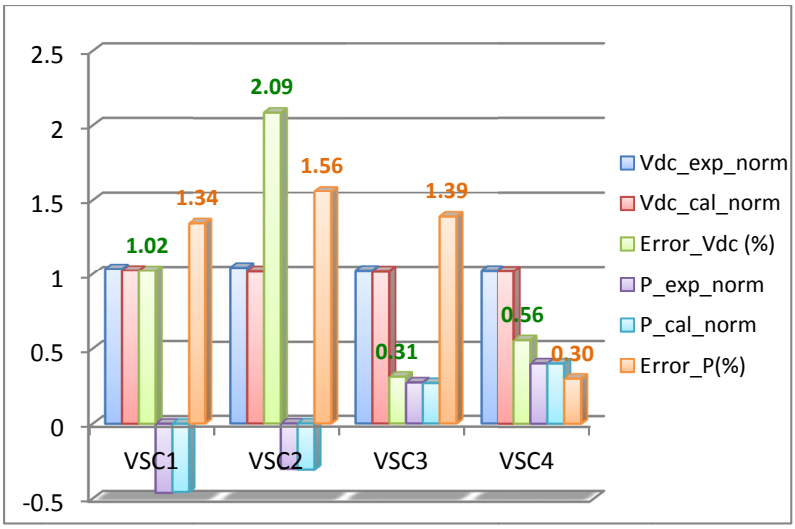


Figure 6-39. Comparison between experimental and calculation results in case 3 with onshore I side fault.

6.4.2 SLG Fault in Onshore Converter II

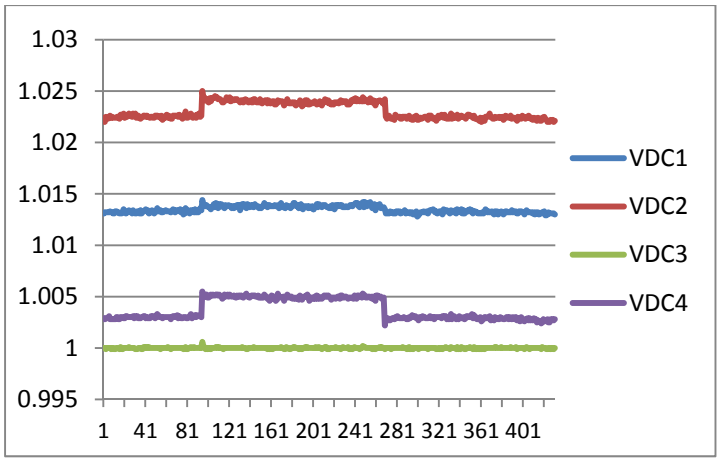
A. d axis current has higher priority

1) Onshore converter II has sufficient power capacity (case 1)

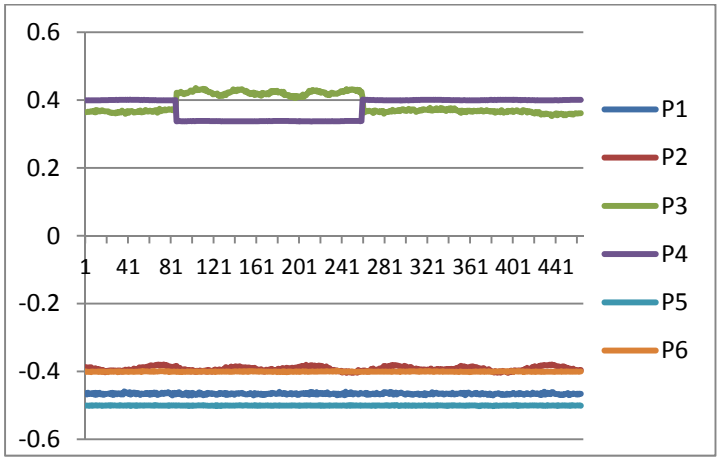
SLG fault in this case will not lead to obvious dc voltage deviation since onshore I is still able to regulate its dc terminal voltage to 1 pu (Figure 6-40(a)). Therefore, the operation modes of all converters are not impacted, as shown in Table 6-8. Moreover, since power reduction in offshore II is completely compensated by onshore I, the ac voltage magnitude ($v_{ac5,6}$) and power generation of WF I and II ($P_{5,6}$) keep the same (Figure 6-40(b) and (d)). The low frequency ripples appear on v_{ac}, active and reactive powers are mainly caused by inaccurate measurement and ac voltage control.

Table 6-8. Operation mode transition in case 1 with onshore II side SLG fault.

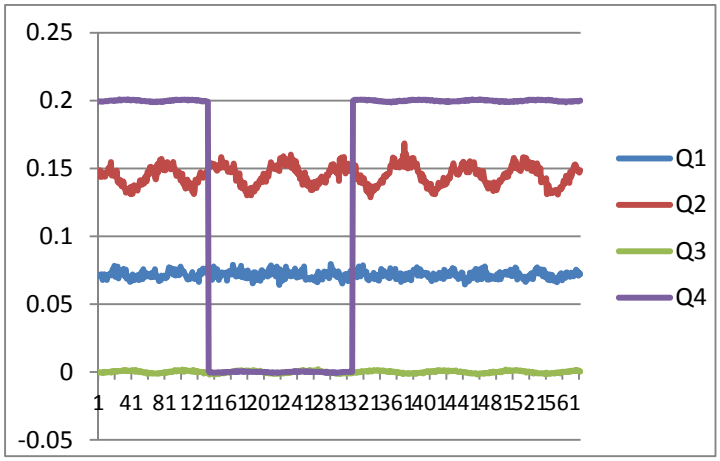
	Offshore I (VSC1)	Offshore II (VSC2)	Onshore I (VSC3)	Onshore II (VSC4)	WF Emulator I (VSC5)	WF Emulator II (VSC6)
Before fault	Vac-f	Vac-f	VdcQ	PQ	PQ	PQ
After fault	Vac-f	Vac-f	VdcQ	PQ	PQ	PQ



(a) DC voltage of onshore and offshore converters

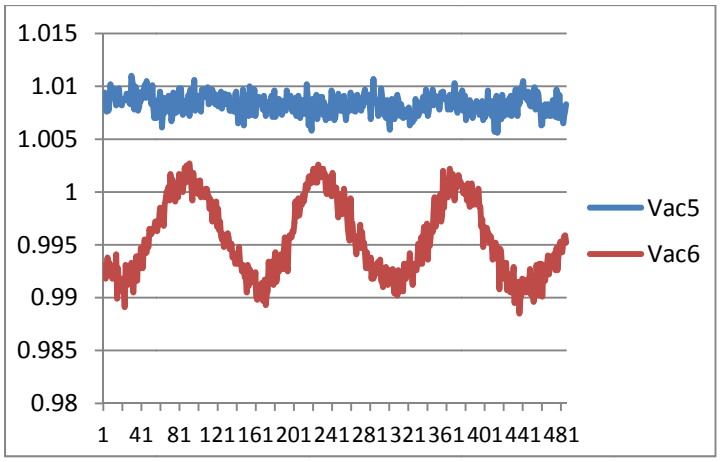


(b) Active power



(c) Reactive power of onshore and offshore converters

Figure 6-40. Experimental results in case 1 with onshore II side SLG fault.



(d) Ac voltage magnitude in windfarm emulators

Figure 6-40. Experimental results in case 1 with onshore II side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value.

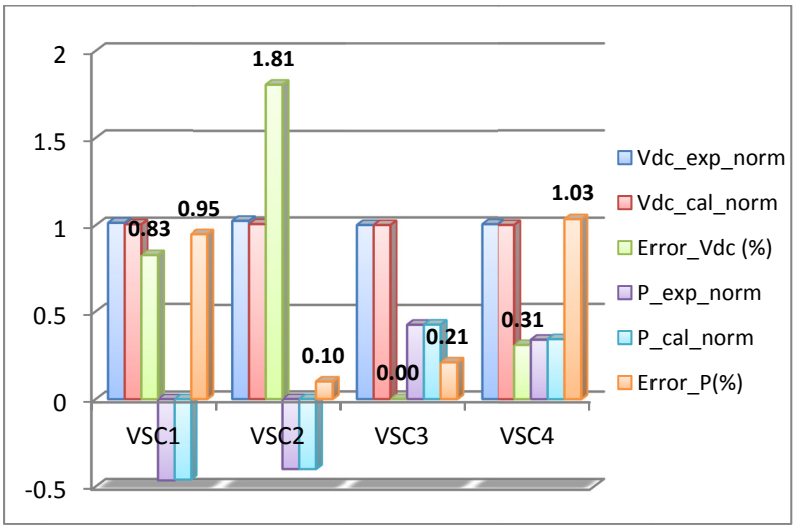


Figure 6-41. Comparison between experimental and calculation results in case 1 with onshore II side fault.

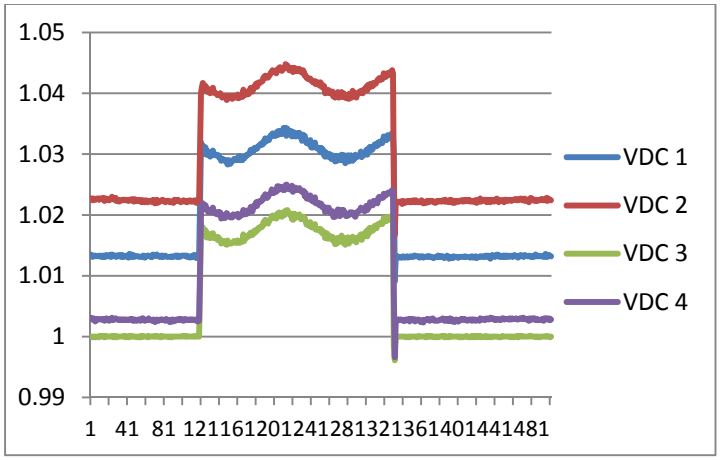
Figure 6-41 gives the comparison between experimental and calculation results. With only constant dc voltage and active power control, the proposed power flow analysis can well estimate the dc terminal voltage and active power of each converter except the higher error in offshore II side dc voltage because of its inaccurate measurement.

2) Onshore converter II has insufficient power capacity (case 2)

Without sufficient power capacity, onshore I cannot maintain its dc terminal voltage as in case 1. Instead, WF1 and WF2 should take responsibility of dc voltage regulation and balance active power in the MTDC network. However, the higher dc voltage measurement and lower initial ac voltage magnitude in offshore II enable a much smaller equivalent dead-band and thus faster dynamic response to dc overvoltage. Therefore, the operation mode of offshore II changes to v_{dc} - v_{ac} droop soon after the fault, which leads to lower ac voltage magnitude and active power generation, while those in offshore I remain, as shown in Table 6-9 and Figure 6-42. Compared to Figure 6-36(b), the dc voltage regulator, i.e., onshore I, still has a little margin before fault, which helps WF II to balance the active power.

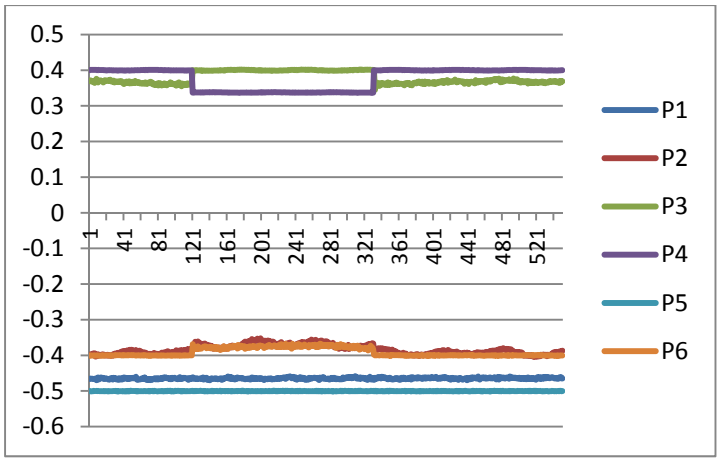
Table 6-9. Operation mode transition in case 2 with onshore II side SLG fault.

	Offshore I (VSC1)	Offshore II (VSC2)	Onshore I (VSC3)	Onshore II (VSC4)	WF Emulator I (VSC5)	WF Emulator II (VSC6)
Before fault	Vac-f	**Vac-f**	**VdcQ**	PQ	PQ	**PQ**
After fault	Vac-f	**vdc-vac droop**	**P limit**	PQ	PQ	**vac-P droop**

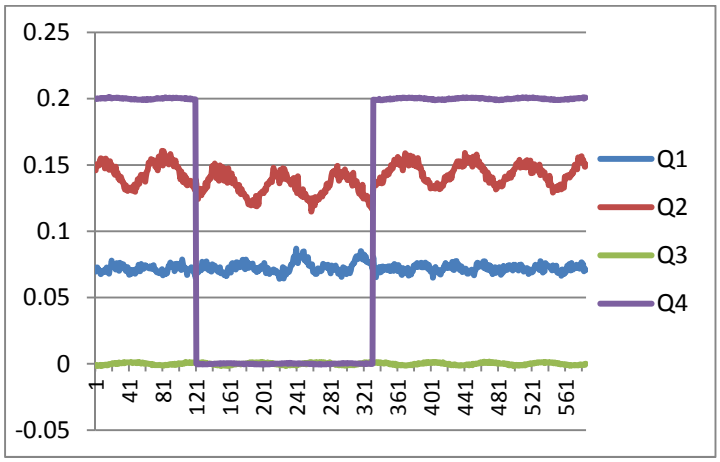


(a) DC voltage of onshore and offshore converters

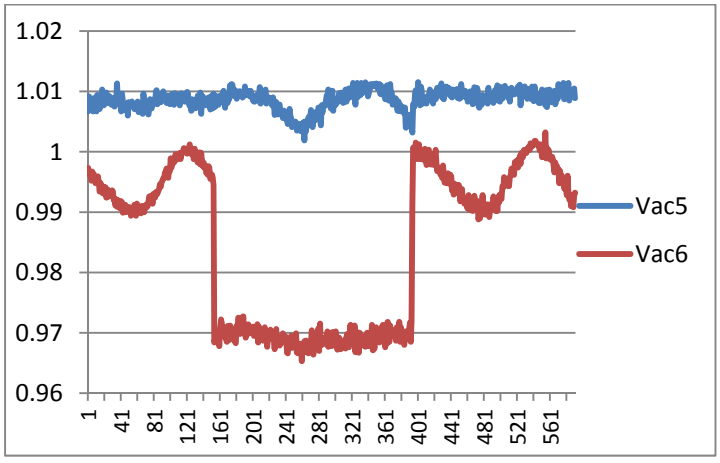
Figure 6-42. Experimental results in case 2 with onshore II side SLG fault.



(b) Active power



(c) Reactive power of onshore and offshore converters



(d) Ac voltage magnitude in windfarm emulators

Figure 6-42. Experimental results in case 2 with onshore II side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value.

As shown in Figure 6-43, mismatch between experimental and calculation results is lower than 2 %. In the power flow calculation, the active power reference for onshore II is set to be constant (P_{ini}×2/3×k_{margin}) during SLG fault, which may deviate from the real power generation. This is considered to be the main reason for the active power error of 1.27 % in onshore II in Figure 6-43.

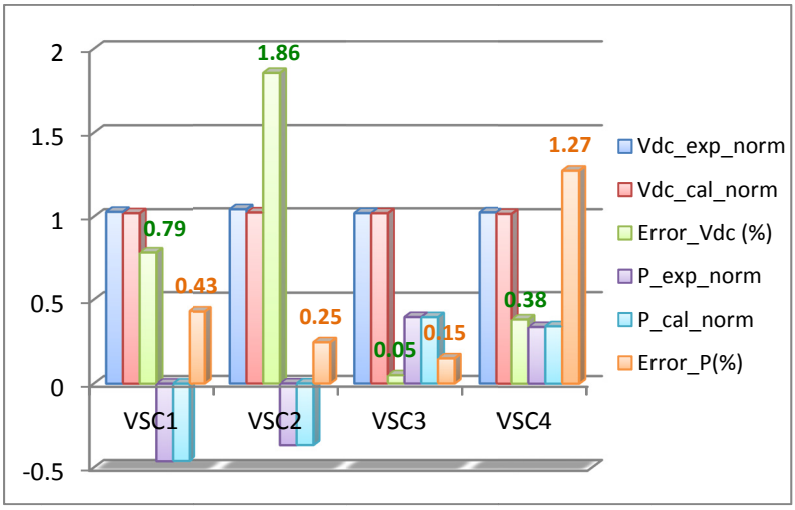


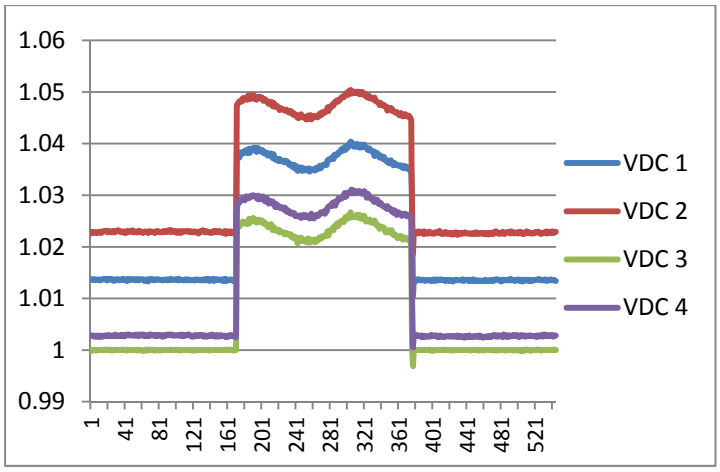
Figure 6-43. Comparison between experimental and calculation results in case 2 with onshore II side fault.

B. q axis current has higher priority (case 3)

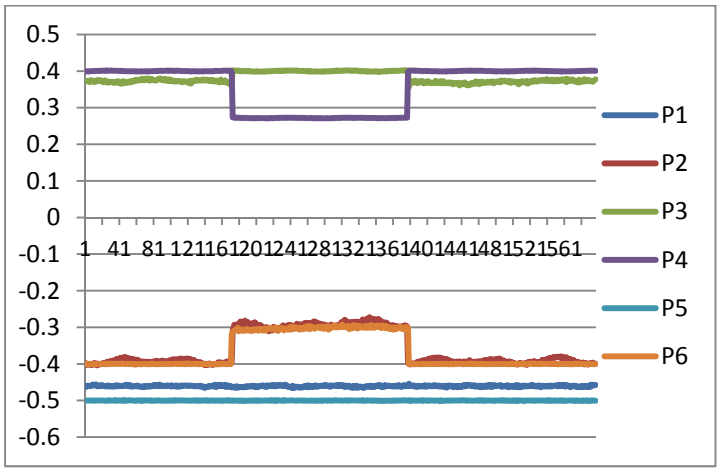
Similar as case 3 with onshore I side fault, the dc voltage increase is higher if q axis current has higher priority, which draws both the offshore I and II into the v_{dc} - v_{ac} droop when SLG fault occurs (Table 6-10). The ac voltage magnitude in the WF I side, correspondingly, drops from around 1.02 pu to 1 pu, as given in Figure 6-44(d).

Table 6-10. Operation mode transition in case 3 with onshore II side SLG fault.

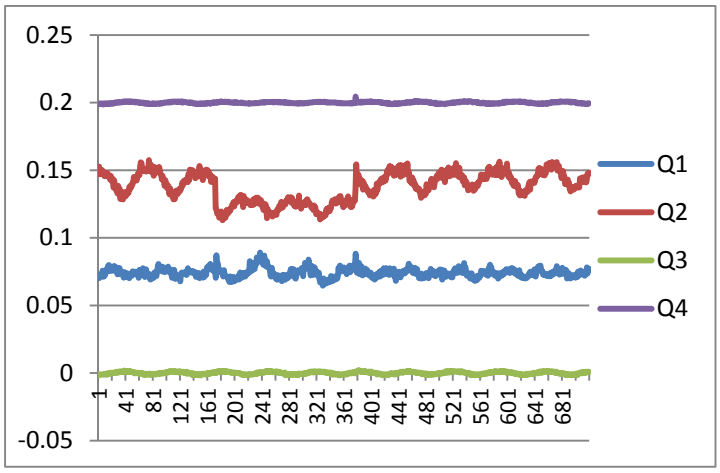
	Offshore I (VSC1)	Offshore II (VSC2)	Onshore I (VSC3)	Onshore II (VSC4)	WF Emulator I (VSC5)	WF Emulator II (VSC6)
Before fault	**Vac-f**	**Vac-f**	**VdcQ**	PQ	PQ	**PQ**
After fault	**vdc-vac droop**	**vdc-vac droop**	**P limit**	PQ	PQ	**vac-P droop**



(a) DC voltage of onshore and offshore converters

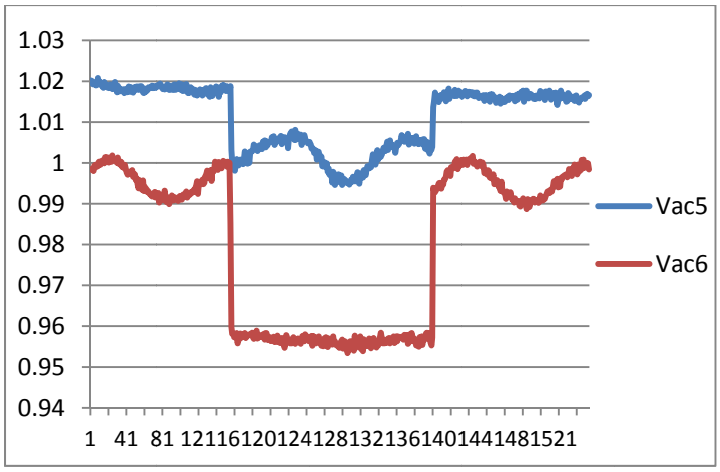


(b) Active power



(c) Reactive power of onshore and offshore converters

Figure 6-44. Experimental results in case 3 with onshore II side SLG fault.



(d) Ac voltage magnitude in windfarm emulators

Figure 6-44. Experimental results in case 3 with onshore II side SLG fault. Continued. x axis: data number (10 data = 1 s), y axis: pu value.

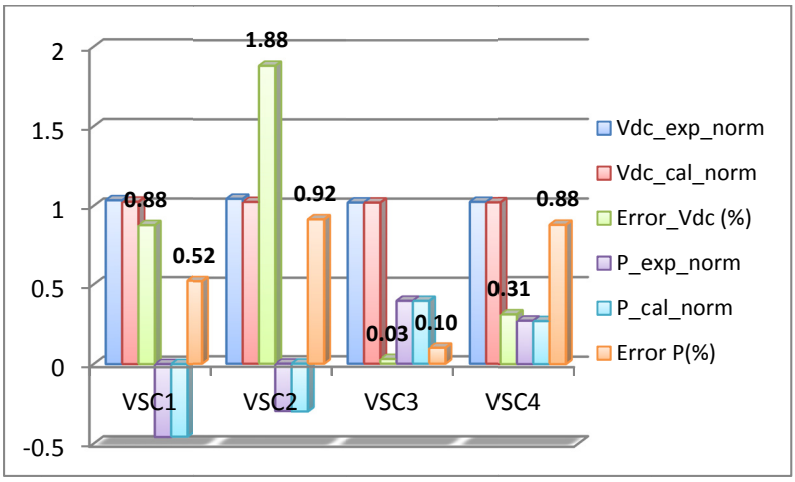


Figure 6-45. Comparison between experimental and calculation results in case 3 with onshore II side fault.

Due to the high dead-band (0.03553 pu), however, $v_{ac} - P$ droop in WF1 still cannot be activated, and a constant active power is generated under both normal and fault conditions. In order to balance the active power, WF II has to drop its power by 0.1 pu in this case. As shown in Figure 6-45, the mismatches between experimental and calculation results are lower than 1 %.

The mismatch between simulation and experimental results is mainly caused by inaccurate current and voltage measurement; incorrect estimation of passive components and their parameter tolerances; and

neglected losses of power devices, etc. These differences, together with assumptions made for cascaded droop control simplification, result in deviation between power flow calculation and experimental results.

6.5 Summary

This chapter presents operation performances of a four terminal HVDC system with the designed cascaded droop control under various SLG fault conditions. The key points in this chapter can be summarized as follows:

1) A cascaded droop control, including $v_{dc} - v_{ac}$ droop and $v_{ac} - P$ droop, has been designed for offshore converter and windfarm since they cannot directly adjust their power output according to the dc terminal voltage. Utilizing ac voltage magnitude as an intermediate variable, the cascaded droop control can transfer the dc voltage information to windfarms without any communication. In order to maintain a desirable operation under normal conditions, e.g., maximum wind energy, a dead-band is also introduced to both droop curves. Only when the dc or ac voltage deviation exceeds the dead-band, droop control will be activated. Otherwise, converters will maintain their constant ac voltage and/or active power control.

2) Power flow for the studied four-terminal HVDC system is calculated using the Gauss-Seidel iterative method. For simplicity, the cascaded droop control is simplified to a single v_{dc} - P_{dc} droop, taking dead-band, power losses, measurement accuracy and ac transformer leakage impedance into consideration.

3) Impact of ac transformer leakage impedance and droop parameters are analyzed and compared. From the simulation results, system with smaller droop constant and/or larger dead-band will suffer higher dc overvoltage during SLG fault if the healthy converter station does not have sufficient power capacity to compensate the active power absorption loss. Moreover, larger leakage impedance of ac transformer induces higher ac voltage magnitude in the WF emulator, which impedes the activation of v_{ac} – P droop and contributes less for dc overvoltage suppression.

4) System performances with different fault locations and current priority are also studied and discussed. Experiencing less active power absorption, system with onshore converter I and II side SLG fault shares the similar characteristics. Additionally, if q axis current has higher priority, active power

drop in the faulty converter will be higher, thus inducing more severe dc voltage increase in both cases. The lowest dc voltage occurs during onshore II side fault when onshore I has sufficient power capacity to maintain the dc voltage, while the highest dc voltage appears when q axis current has higher priority and the other healthy onshore converter station cannot support more power.

5) Simulation results from a four-terminal HVDC system generated with Matlab/Simulink and experimental results from a scaled down prototype are provided to support the theoretical analysis and proposed control schemes.

7 Conclusion and Future Work

This chapter summarizes the research done and reported in this dissertation. Also future research directions are suggested for related topics.

7.1 Conclusion

This dissertation deals with development of a fault handling strategy, which helps VSC based HVDC systems achieve continuous energy supply and desired operation performance under temporary SLG fault conditions (e.g., for two level VSCs, balanced ac phase current or negligible active power ripple; for MMCs, balanced ac phase current, minimum circulating current and negligible active power ripple), while ensuring a smooth and fast black start for MMC-HVDC, particularly, if the system has to shut down to protect power devices and passive components from damage when a permanent SLG fault occurs. Several topics have been covered in this dissertation, and the main contributions of the research are summarized here.

First, a steady-state model of MMC for second order phase voltage ripple prediction under unbalanced conditions was proposed, taking the impact of negative sequence current control into account. From the steady-state model, a circular relationship was found among current and voltage quantities, which was used to evaluate the magnitudes and initial phase angles of different circulating current components. Moreover, in order to calculate the circulating current in a point to point MMC based HVDC system under unbalanced conditions, the derivation of equivalent dc impedance of a MMC was discussed as well. Experimental results from a scaled down three-phase MMC system, operating in either rectifier or inverter mode, were provided to support the theoretical analysis and derived model.

Second, the analysis and control of a MMC based HVDC transmission system under three possible SLG fault conditions were discussed, with special focus on the investigation of their different fault characteristics. Based on the derived steady state model, a novel double line frequency dc voltage ripple suppression control was proposed. This controller, together with the negative and zero sequence current control, could enhance the overall fault-tolerant capability of the HVDC system without additional costs.

To further improve the fault-tolerant capability, operation performance of the HVDC system with and without single phase switching (SPS) was discussed and compared in detail. The feasibility and robustness of the proposed control scheme were verified by both simulation and experimental results under various operating circumstances.

Third, the charging loops of MMC rectifier and inverter during uncontrolled pre-charge period were analyzed, aiming at observing the necessity of additional capacitor charging schemes. Moreover, the small signal model of the capacitor charging loop was first derived according to the internal dynamics of the MMC inverter. Based on this model, a novel startup strategy incorporating an averaging capacitor voltage loop and a feedforward control was proposed, capable of enhanced dynamic response and system stability without sacrificing voltage control precision. The design considerations of the control strategy were also given in detail. Simulation results from a back-to-back MMC (BTB-MMC) system connecting to either active terminals or passive loads, and experimental results from a scaled-down MMC were performed to demonstrate the validity of the theoretical analysis and proposed control scheme.

Finally, a cascaded droop control scheme was designed for multi-terminal HVDC systems to deal with dc overvoltage under SLG fault. Using ac voltage magnitude as an intermediate variable, the dc voltage information of offshore converters can be "known" by the windfarms and used to adjust the active power generations without any communication. With this control scheme, system performances of the studied four-terminal HVDC system under various fault conditions were analyzed and compared, including different fault locations (onshore I or II); healthy onshore converter capacity margin; dq axis current priority; droop control parameters (droop constant and dead-band) and ac transfer leakage impedance. Moreover, power flow calculation was derived using the Gauss-Seidel iteration method to supply a simple and effective approach for power flow prediction and droop control design. Furthermore, the calculation results were compared with experimental waves obtained from a scaled-down four-terminal HVDC prototype with a two-level VSC in each converter station.

7.2 Recommended Future Work

Some recommended future research that extends the work done in this dissertation includes:

(1) Dynamic Modelling for MMC-HVDC under SLG Fault

Although the proposed steady state modelling of point-to-point MMC-HVDC can provide an analytical analysis for current and voltage quantities under SLG fault, it relies on the steady state relationship and cannot present the dynamic response.

However, the accurate dynamic model of MMC, even under normal conditions, has so far been missing in the literature. Due to its unique structure, a MMC contains both fundamental and second order frequency current and voltage components, which are difficult to be decoupled. In addition, the arm inductors and large number of submodule capacitors further complicate its dynamic models. Furthermore, under SLG fault conditions, the phase current will have a negative sequence component, and positive as well as zero sequence circulating current will also be generated. Therefore, for explicit modelling, the current and voltage quantities for the different sequences may need to be modelled separately.

After achieving the dynamic model of MMC, transfer functions between circulating current and duty cycle, dc voltage ripple to phase current, capacitor voltage to circulating current, etc., can be derived. Based on these transfer functions, the corresponding circulating current control, dc voltage ripple suppression and capacitor voltage balancing control can be theoretically designed for both desirable steady state and dynamic performance.

(2) Equivalent Phase Power Generation through Independent Phase Control during SLG Faults

Physically decoupled, each phase of MMC can operate independently. If equal three-phase active power is required under SLG fault, the balanced positive sequence current implemented in the proposed fault-tolerant control scheme will not be possible. Instead, three-phase current would deviate from each other for equivalent power generation. For the faulted phase, particularly, large current will be induced to compensate for the voltage drop caused by the fault.

The independent phase control can only be realized under abc coordinates, using a PR controller for zero steady state error. Instead of regulating dq axis components, each phase of MMC now has to control both magnitude and angle of voltage as well as current. Under fault conditions, however, the grid voltage contains a negative sequence component, which makes the magnitude and angle reference hard to achieve. Therefore, how to realize the independent phase control and achieve desirable performance under fault conditions are interesting topics that need to be considered.

(3) Fault Characteristics and Control Scheme of MMC-HVDC System under Other AC Faults

This dissertation deals with only SLG fault, which is the most common ac fault type. But other ac faults, e.g., line-to-line fault, line-to-line-to-ground fault, three-phase-to-ground fault, etc., may also occur in power systems, leading to distinguishing fault characteristics. For example, with three-phase-to-ground fault, the phase-lock-loop cannot work properly, and converter will output its maximum current without grid synchronization. Similarly, the system may lose its controllability under certain ac fault conditions and cannot achieve the pre-set targets using the proposed integrated control schemes. Therefore, for favorable fault tolerant capability, both the control objectives and control methods should be adjusted under different ac fault types.

(4) Stability in Multi-terminal HVDC systems

The modelling and stability of multi-terminal HVDC systems have been analyzed in [144] - [146]. Without a valid model of the MMC, most of the literature focuses on the two-level VSC based MTDC with certain network configuration. In addition, the system is usually regarded as a single unit, and all elements (converters and dc cables) are considered simultaneously, making the model process quite complicated. Therefore, it is helpful to have an elaborate way to divide the MTDC system into subsystems, and merge the separate models together afterwards. If small signal models of converters and dc cable networks can be modularized, the modelling of a large scale MTDC system will be much easier.

Theoretically, control parameters should be designed based on the entire small signal model for enough stability margin. In reality, however, the controllers are mostly set according to a single converter

because of the uncertainty of external circuits. Consequently, a simple approach for controller design is necessary to guarantee system stability.

(5) AC Faults in Windfarm Station and Corresponding Control

With offshore converter regulating the PCC voltage, only the onshore converter, which is directly connected to ac grid, is considered to have an ac fault in this dissertation. However, the SLG fault may still occur in ac terminals of offshore converters. With one phase shorted to ground, if only the ac voltage control implemented in dq axis is adopted, the offshore converter cannot regulate its ac voltage and large current will be generated. Therefore, an advanced control scheme should be proposed to withstand the unbalanced ac voltage and regulate phase current to an acceptable range. In addition, the performance of wind turbines under a SLG fault should also be studied to ensure the feasibility of system continuous operation and other control targets.

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