To the Graduate Council:

I am submitting herewith a dissertation written by Mohammad Aminul Huque entitled "A High-Temperature, High-Voltage SOI Gate Driver Integrated Circuit with High Drive Current for Silicon Carbide Power Switches." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed K. Islam

Major Professor

We have read this dissertation and
recommend its acceptance:

Leon M. Tolbert

Benjamin J. Blalock

Narendra B. Dahotre

Acceptance for the Council:

Carolyn R. Hodges

Vice Provost and
Dean of the Graduate School

(Original signatures are on file with official student records)

A High-Temperature, High-Voltage SOI Gate Driver Integrated Circuit with High Drive Current for Silicon Carbide Power Switches

A Dissertation Presented for
the Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

Mohammad Aminul Huque
May 2010

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Dedication

This dissertation is dedicated

to my father, Dr. M. Anwarul Huque, and to my mother, Hoshneara Huque.

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Abstract

High-temperature integrated circuit(IC) design is one of the new frontiers in microelectronics that can significantly improve the performance of the electrical systems in extreme environment applications, including automotive, aerospace, well-logging, geothermal, and nuclear. Power modules (DC-DC converters, inverters, etc.) are key components in these electrical systems. Power-to-volume and power-to-weight ratios of these modules can be significantly improved by employing silicon carbide (SiC) based power switches which are capable of operating at much higher temperature than silicon (Si) and gallium arsenide (GaAs) based conventional devices. For successful realization of such high-temperature power electronic circuits, associated control electronics also need to perform at high temperature. In any power converter, gate driver circuit performs as the interface between a low-power microcontroller and the semiconductor power switches. This dissertation presents design, implementation, and measurement results of a silicon-on-insulator (SOI) based high-temperature (>200 °C) and high-voltage (>30 V) universal gate driver integrated circuit with high drive current (>3 A) for SiC power switches. This mixed signal IC has primarily been designed for automotive applications where the under-hood temperature can reach 200 °C.

Prototype driver circuits have been designed and implemented in a Bipolar-CMOS-DMOS (BCD) on SOI process and have been successfully tested up to 200 °C ambient temperature driving SiC switches (MOSFET and JFET) without any heat sink and thermal management. This circuit can generate 30 V peak-to-peak gate drive signal and can source and sink 3 A peak drive current. Temperature compensating and temperature independent design techniques are employed to design the critical functional units like dead-time controller and level shifters in the driver circuit. Chip-level layout techniques are employed

to enhance the reliability of the circuit at high temperature. High-temperature test boards have been developed to test the prototype ICs.

An ultra low power on-chip temperature sensor circuit has also been designed and integrated into the gate-driver die to safeguard the driver circuit against excessive die temperature ($\geq 220\,^{\circ}\mathrm{C}$). This new temperature monitoring approach utilizes a reverse biased p-n junction diode as the temperature sensing element. Power consumption of this sensor circuit is less than $10\,\mu\mathrm{W}$ at $200\,^{\circ}\mathrm{C}$.

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Chapter 1

Introduction

Since the invention of the first integrated circuit (IC) by Jack Kilby in 1958, much progress has taken place in the semiconductor industry. Integrated circuits (ICs) are now used in the majority of consumer and industrial electrical systems. The electronic revolution of the 20th century is mainly based on silicon (Si) devices [1]. More than 98% of current electronic circuits use Si as the semiconductor material. However, operations of most commercial Si-based ICs are limited to a narrow operating temperature range. Figure 1.1 shows the temperature range for different classes of ICs available in the market. ICs with the maximum temperature rating available in the market are defined as "military grade" and are designed for $-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ temperature range of operation. On the other hand, the range "extreme-temperature" is typically used for electronics operating outside the traditional temperature range of $-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. This covers both the very low temperatures (down to absolute zero), and the high temperatures (anything above $+125\,^{\circ}\mathrm{C}$) [2,3]. This category of electronics is further divided into different groups as shown in Table 1.1. High-temperature electronics is still considered a niche market technology with tremendous potential to improve modern everyday life.

1.1 Application of High-Temperature Electronics

Electronic components are exposed to high temperatures in a variety of applications and environments. Semiconductor based electronics capable of operation at ambient tempera-

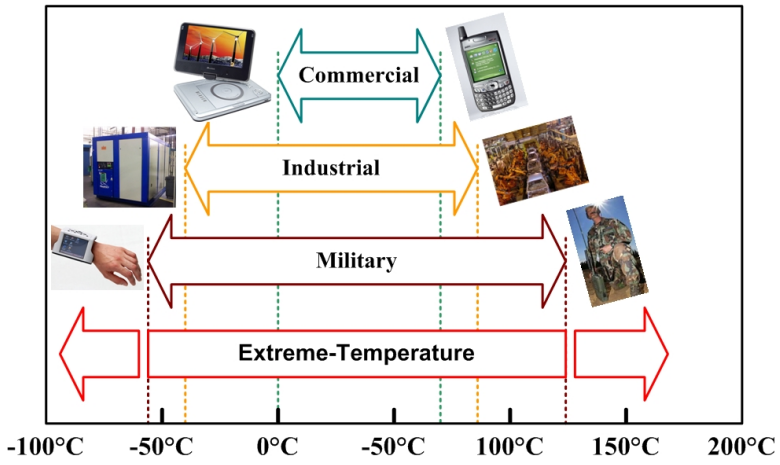


Figure 1.1: Operating temperature range of semiconductor ICs.

Table 1.1: Classification of extreme-temperature electronics.

Low-temperature electronics	T $<-55\,^{\circ}$C
Cryogenic electronics	T $<-150\,^{\circ}$C
High-temperature electronics	T $>125\,^{\circ}$C
Wide-temperature electronics	T $<-55\,^{\circ}$C & T $>125\,^{\circ}$C

tures higher than 150 °C without external cooling have tremendous potential in automotive, aerospace, well-logging, nuclear, and geo-thermal energy production industries [4–6]. Figure 1.2 shows the most promising application areas for the high-temperature electronics. Power electronic modules are integral parts of the electrical systems used in these applications. Almost all of these power electronic modules use power semiconductor switches along with low-power control electronics and passive components.

1.1.1 Automotive

The automotive industry is often considered as the primary near-term market for high-temperature electronics. Also this sector is potentially a user of very large volumes of high-temperature electronic products. Automotive electronics include sensors for engine speed and angular position, ABS, exhaust gas, power steering, and engine condition monitoring [5]. Automotive industries are also developing hybrid electric vehicles (HEVs) to achieve better fuel efficiency [6]. The potential shortage of gasoline supply in the future and

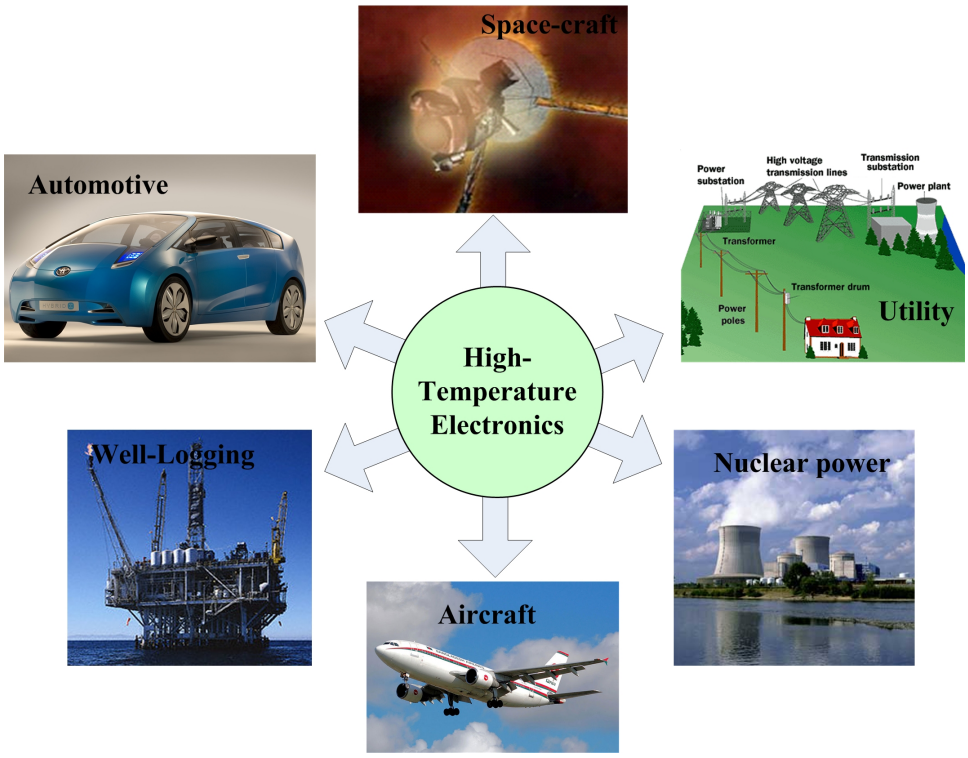


Figure 1.2: Application of high-temperature electronics.

the volatile nature of its price are creating an escalating demand for the development of electrical vehicles that have much higher efficiency as compared to the traditional internal combustion engines (ICEs). Electric vehicles need multiple power electronic modules (DC-DC converter, inverter, etc.) for bidirectional power conversion between the energy storage units (battery or ultra-capacitor) and the traction system [7, 8]. The ambient temperature under the hood of the car is usually above 150 °C and can potentialy reach 200 °C near the engine [5, 9]. To minimize the cost and to improve the efficiency of HEVs, there is an urgent necessity for miniaturization and weight reduction of power converter modules. To achieve these goals, electronic circuits capable of operating at higher ambient temperatures (175 °C and above) with minimal thermal management are in great demand. Current HEV technologies require a separate 70 °C cooling loop for commercially available power electronic circuits which are mostly rated for a maximum of 85 °C ambient temperature operation. A future goal of the automotive industry includes the use of the same 105 °C cooling loop that is used for the engine to cool the electronics under-the-hood. By removing

the extra cooling unit, and by reducing the size of the heat sink, an order of magnitude savings in the overall mass and volume of the power electronic modules can be achieved.

Although the automotive sector represents the largest potential market opportunity for high-temperature electronics components, it also presents its toughest challenges. Automotive applications are characterized by the most stringent pricing pressure of any sector requiring high-temperature components. Reliable under-the-hood electronics must also be capable of extended operation in all seasons anywhere on the globe, as well as surviving many wide temperature-swing cycles.

1.1.2 Well-logging and Geo-thermal

Exploration and monitoring of petroleum and geo-thermal wells use probes that are sent deep into bore holes, where the temperature varies according to the depth of the well. A Typical upper limit of over 90% of borehole applications is 200 °C; however, the oil industry continues to explore new markets in deeper, i.e. hotter, wells where the working temperatures reach 300 °C, and will eventually reach 400 °C [5, 10]. Since signals from sensors in these probes must be sent to the instruments placed on the surface via long cables or through wireless transmitters, it is necessary to co-locate some signal-processing electronics in the probes to avoid signal degradation during transmission. The use of high-temperature electronics within the oil and/or gas exploration and the geo-thermal industry is typically characterized by:

- Low volume
- High level of specialization
- High accuracy and high performance
- High reliability

Until recently, the petroleum exploration industry has been the leading sponsor for high-temperature electronics research because of the high return on investment in well-logging applications.

1.1.3 Aerospace

Modern aircraft, both commercial and military, rely on complex electronics and sensors to enhance their capabilities and efficiency. Aircrafts require interface electronics for the sensors monitoring the engines, actuators, and other system elements. Many of these locations involve a hot environment possibly up to 300 °C [5]. With the current trend towards "fly-by-wire" and distributed systems, aircrafts are demanding more high-temperature electronics.

1.1.4 Space Exploration

Radiation-hard high-temperature electronics is needed for missions to the hostile environments near the sun and on the surfaces of the inner planets. Long-standing operation of probes within Venus's blazing 450 °C environment will require the use of high-temperature electronics. At present time, commercial satellites require thermal radiators to dissipate heat generated by the spacecraft's electronics. Use of high-temperature electronics would achieve substantial weight savings on a satellite by reducing the size and weight of the thermal radiators.

1.1.5 Nuclear Power

Nuclear power generating industries need high-temperature and radiation-hard electronics to place reliable sensing instruments in plant locations that are unfavorable and hazardous to human operators [4].

1.2 High-Temperature Automotive Power Electronics

Global oil production is predicted to reach its peak by the year 2015 [11]. After reaching its peak, oil production will start to decrease sharply. At present time, the world is using four times more oil than is being discovered. In the USA, oil provides 99% of the fuel used in its transportation sector. Huge worldwide demand for petroleum based fuel is potentially threatening to cause its shortage in the near future. This possibility is inspiring university researchers, government agencies, and industries to develop smarter technology for the

transportation sector. In addition, the growing concern for environmental pollution caused by the burning of fossil fuel is also inspiring many to support green vehicles.

At present, researchers are working on three major technologies to incorporate the advantages of electric motor drive into the automotive sector. Hybrid-electric vehicle (HEV), the leading technology among the three, uses both internal combustion or diesel engines and electric motors to improve the performance and efficiency of the vehicle. Plug-in-hybrids (PHEV) use larger battery packs and external charging capability to make it possible to reap the benefits of electric vehicles while overcoming their drawback of limited range. These vehicles do not use the internal combustion engine (ICE) for shorter distances (usually up to 30 miles). Fuel-cell vehicles (FCV) generate their own electricity using hydrogen or other fuel convertible to hydrogen. FCVs are widely considered as the future replacement of the internal combustion engine vehicles (ICEV). This replacement could save 60% of the primary energy consumption, and could reduce the CO_2 emission by 55% [12]. However, FCVs are not yet in a position to challenge ICEVs for performance, cost, fuel storage, and large scale manufacturability [12]. On the other hand, HEVs are gaining more attention for their better performance and fuel economy compared to ICEVs. PHEVs are about to enter the market. Transition from ICEV to HEV or PHEV means switching from mechanical and hydraulic systems to electromechanical systems. Both HEV and PHEV require several power electronic modules to transfer energy between energy storage elements (usually battery) and electromechanical systems.

High performance reliable automotive electronic circuits are a prerequisite for the development of next generation automotives. Car vehicle sales all over the world are expected to have a growth of about 4% per year between 2000 and 2010 [13]. In this time period, the electronic system growth is expected to be over 10% per year. In 1977 the average electronics per automotive was of worth \$110 [14], whereas in 2003 this figure jumped to \$1510 in spite of the price reduction in the semiconductor manufacturing [15]. It is predicted that by 2013 each automotive will contain, on the average, \$2285 worth of electronics within its frame [15]. Currently, the cost of electronic parts in cars is approximately 15% for compact cars, 28% for luxury cars, and 47% for hybrid cars [13]. Applications of high-temperature electronics in automotive systems will continue to grow with their increased availability and reduced price.

1.2.1 Power Converters in Automotives

A typical arrangement of a series/parallel HEV is shown in Figure 1.3. Developments in the hybrid automobile industry have generated an enormous need for different power converter modules (such as DC/DC converters and DC/AC inverters) capable of operating at elevated temperatures. Reliability is a major concern for the automotive electronics. Increased operating temperature accelerates many failure mechanisms, such as time dependent dielectric breakdown of gate oxides in MOSFETs and electromigration of metal interconnects inside integrated circuits. Once installed, automotive electronics are expected to operate reliably for approximately 10 years or 150,000 miles [16].

1.2.2 Automotive Temperature Extremes

From the reliability point of view, the automotive is divided into the passenger compartment and engine room. In the passenger area, electronic circuits are required to obtain the maximum 85 °C operating temperature [13]. In the engine room, the required operating temperature can vary widely depending on the actual placement of the electronics. A summary of the high-temperature automotive electronics requirement published by DaimlerChrysler, Eaton Corporation, and Auburn University is reproduced in Table 1.2 [9]. For the majority of the cavity under the hood, the temperature is more than 150 °C. Typically the junction temperatures for integrated circuits are 10 °C to 15 °C higher than the ambient temperatures which can even reach 25 °C for power devices. Hence, electronics used in automobiles (especially those placed close to the engine) need to be able to work at temperatures close to 200 °C.

Table 1.2: Mechatronic Temperature Ranges.

On-engine	150 – 200 °C
In-transmission	150 – 200 °C
On wheel - ABS sensors	150 – 250 °C
Cylinder pressure	200 – 300 °C
Exhaust sensing	Up to 850 °C, ambient 300 °C

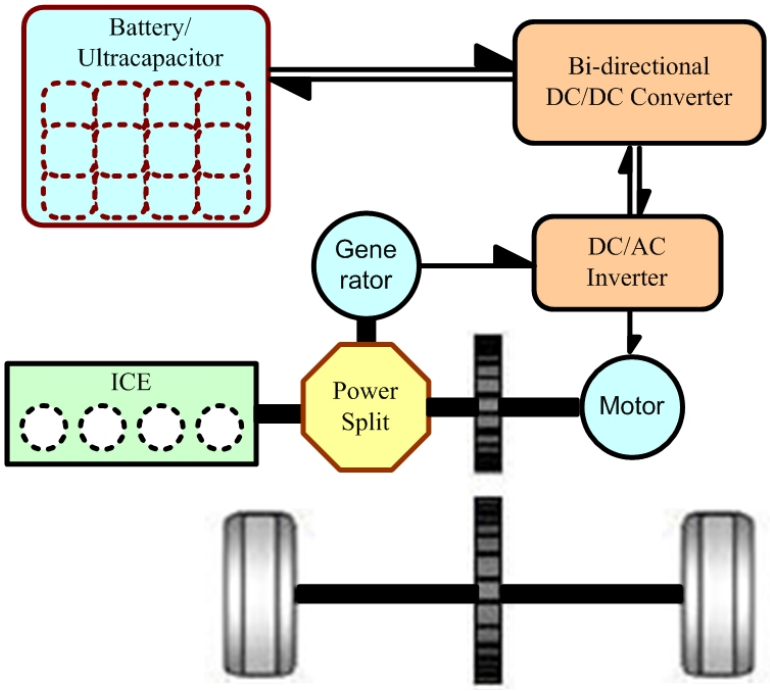


Figure 1.3: Typical topoloty of a series/parallel HEV.

1.3 Semiconductor Material Choice for High-Temperature Power Switches

More than 98% of current electronic devices use silicon as the semiconductor material [5]. Si-based power devices are dominating the power electronics and power system applications. Applications where power devices are required to operate at high temperatures, high voltages, high switching frequencies, and high power densities are growing. Si-based devices are not able to meet these challenging requirements without a costly cooling system which increases the weight and the volume of the power converters. When compared to silicon, the superior material properties of wide bandgap (WBG) semiconductors offer a lower intrinsic carrier concentration (10–35 order of magnitude), a higher electric breakdown field (4–20 times), a higher thermal conductivity (3–13 times), and a larger saturated electron drift velocity (2–2.5 times) [17]. These properties of WBG semiconductors are making them more suitable materials for fabricating high-power and high-temperature power devices.

Among the different WBG semiconductors, diamond is the best semiconductor material

for fabrication of high-temperature power devices. Because of the material processing difficulty associated with diamond, it is not likely to be commercially available as an active device materil for many years. Silicon carbide (SiC) exhibits a dielectric strength of ten times that of silicon and a thermal conductivity of five times that of silicon. The p-n junction leakage in SiC is many orders of magnitude less than that in other conventional semiconductors. Due to these superior properties, SiC has emerged as an alternative semiconductor to overcome the limitations of silicon especially in extreme environmental conditions. SiC device operation at up to 500 °C has been reported in the literature [18–20], whereas Si-based devices can only operate at a maximum junction temperature of 150 °C [16,18]. Hence SiC-based power switches are expected to be the switch of choice for power electronic circuits in harsh environments where the ambient temperature can exceed 200 °C.

Despite all the advantages, SiC has not been adopted for power devices until recently. Difficulty with material processing, presence of micropipes and dislocations, and lack of abundant wafer suppliers, have all contributed to the slow progress in making commercially available SiC power devices. At present time, prototype SiC devices can be obtained from CREE, Infineon, SiCED, and SemiSouth. Different types of power devices are developed by these companies. Device parameters (voltage and current ratings, ON resistance, gate control voltage, etc.) of the SiC power switches developed by these companies vary widely, which contributes significant challenges to the system designers.

1.4 Gate Driver Circuit for Power Switches

In any power electronic circuit, the flow of power from source to the load is controlled by the power switch through its turning ON and OFF operations. Gate driver circuits are required to generate the drive signals with sufficient current drive to turn the power switches ON and OFF from the logic input coming from a DSP, microcontroller, or other logic circuits. The performance of a system highly depends on the characteristics of the switch as well as the ability of its driver to efficiently control the turn ON and OFF operations.

Figure 1.4 shows the schematic of a typical electric traction drive for an HEV. The three-phase inverter in this traction system employs six power switches (Q_1 to Q_6). Controlled turn ON and OFF operations of these switches control the flow of power from the battery

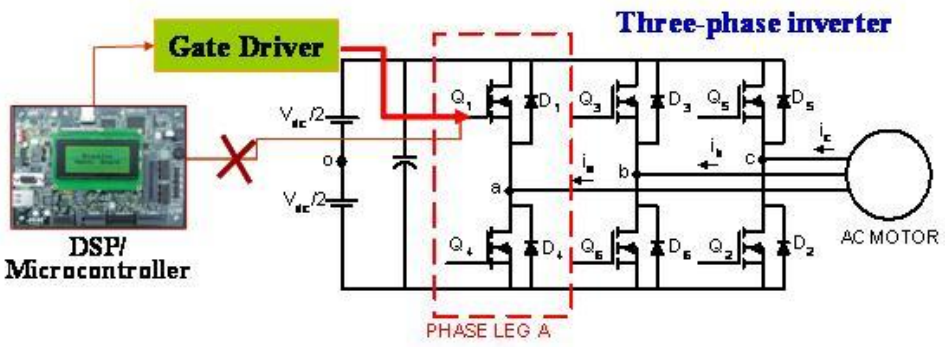


Figure 1.4: Role of gate driver circuit in power converters.

to the AC motor (load). ON/OFF control signals generated by the microcontroller (or DSP) are usually low power pulses, which lack the voltage and current strength to drive the power switches directly. For most cases, voltage magnitude of this logic level signal is lower than the threshold voltage of the power switches and lacks the current sourcing/ sinking capability to charge and discharge the gate capacitance fast enough to minimize the switching power losses. The gate driver circuit, playing the role of a power amplifier, accepts this low power signal from the controller and generates the appropriate high-current, high-voltage gate drive signal for the power switch.

1.5 Research Motivation

In all power converter modules (DC-DC converter, inverter, etc.), gate drivers are essential components to control the turn ON and OFF actions of power switches. Placing the gate driver circuit next to the power switch can improve the performance by reducing the parasitic inductances associated with long wires. Long interconnects are also a potential source of failure, especially in harsh environment conditions. In automotive applications, power converter modules are likely to be placed under the hood of the car where the temperature can reach 200 °C. Hence the ambient temperature of the gate driver IC can be as high as 200 °C. A gate driver IC capable of operating at elevated temperatures (>200 °C) can contribute to the reduction of weight and volume of the power conversion modules as well as improve the reliability. The alternatives to high-temperature devices and cir-

cuits are complicated thermal management systems that add weight and volume resulting in reduced power-to-volume and power-to-weight ratios. These thermal management approaches introduce additional overhead that can negatively offset the desired benefits of the electronics relative to the overall system operation. The additional overhead in the form of longer wires, extra connectors, and/or cooling systems can add undesired size and weight to the system, as well as increased potential for failure. By removing the heat sink and long interconnects, an order of magnitude savings in overall mass and volume of the power electronic modules can be achieved.

Figure 1.5 shows the three probable ways to employ electronic circuits in high-temperature environments. The traditional approach is to place the low-temperature electronics in a relatively cooler place far away from the actual high-temperature system. In this case no additional cooling is necessary for the electronics. However use of long cables increases the weight, volume, and complexity of the system. Running long cables, especially through harsh environments, reduces the reliability as well as the signal-to-noise ratios (SNR). An alternate approach is to use thermal management around the low-temperature electronics, placed close to the high-temperature systems. This method reduces the use of long cables and hence, reduces the associated reliability concerns. Usually thermal management systems employ bulky heat sinks and fans or liquid cooling loops which increase the volume and weight of the system. Additional power consumed by the cooling pumps and/or fans reduces the overall efficiency of the system. The best solution is to place the electronic circuits next to the high-temperature environment without any thermal management. For successful implementation of this approach, electronic circuits need to perform at high ambient temperatures. The main driving force for high-temperature electronics research is the elimination of expensive and bulky thermal management systems which are currently required to protect electronics from extreme environments. This would result in improved system topology, increased performance and efficiency, reduced environmental emissions, and large system level cost savings.

To the best of the author's knowledge, there is presently no high temperature gate driver integrated circuit available in the market or reported in the literature for SiC power switches with high current drive (>2 A) capability. Nearly 4,200 MOSFET, bridge driver ICs are reported in the Digi-Key's catalog [21]; however, none rated for the 200 °C operation.

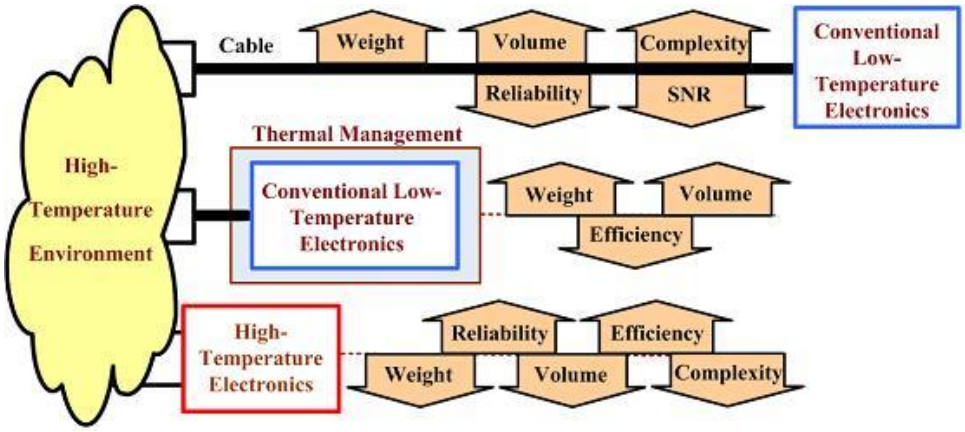


Figure 1.5: Comparison of three different ways to implement electronics in the high-temperature environments.

Digi-Key is a major vendor of semiconductor products. Figure 1.6 shows that even at low temperatures, availability of gate driver circuits reduces with the increase in drive-voltage and peak drive-current.

This dissertation presents research on a high-temperature (>200 °C), high-voltage (>30 V) silicon-on-insulator gate driver circuit with high drive current (>3 A) drive for SiC power switches. Although this work is primarily focused for automotive application, it can be utilized in other high-temperature applications.

1.6 Problem Statement

In power electronic applications there is a constant demand for compact, lightweight, and efficient power converters. This demand cannot be fully satisfied by only the smart power switches with higher operating temperature range, higher breakdown voltage, higher current density, and lower ON resistance. In addition, the associated control electronics for these switches need to become smarter. One way to achieve better power-to-volume and power-to-weight ratios for these modules is to remove, or at least reduce the size of the heat sink and cooling units. Wide bandgap semiconductor materials, especially a SiC-based power module with high-temperature control electronics capable of operation at 200 °C ambient temperature, can certainly go a long way to achieve this goal.

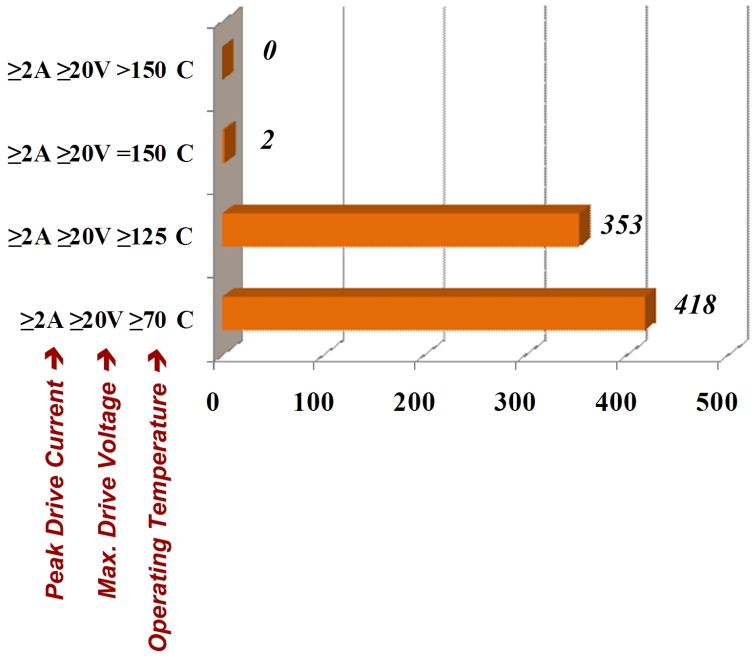


Figure 1.6: Availability of high-voltage, high-temperature gate driver circuit with high drive current capability.

In any power electronic circuit, power switches need gate driver circuits to communicate with the external controller circuit. The gate driver for the wide variety of SiC power transistors must be able to communicate with an external controller system and must have the voltage and current drive capability to efficiently turn ON and OFF the power switches. The design goals set for this high-temperature, high-voltage gate driver work are shown in Table 1.3.

1.7 Organization of the Dissertation

This dissertation consists of six chapters. Chapter 1 introduces the role of high-temperature electronics in different application areas, especially in the automotive sector. This chapter establishes the motivation and sets objectives for the research contributions presented in the later chapters. A literature survey on temperature effects on semiconductor materials and devices, comparison of wide bandgap semiconductor material properties with silicon, and some high-temperature design techniques are presented in Chapter 2. Chapter 3

Table 1.3: Design goals for the proposed high-temperature gate driver circuit.

Design goals	Specification
Gate drive input voltage	0–5 V
Gate drive voltage	10 V to 30 V
Switching frequency	20 kHz
Peak current drive	3 A
Operating temperature range	−55 °C to 200 °C

discusses the functionality of a gate driver circuit along with a brief survey on existing high-voltage, high-temperature gate driver circuits. This chapter mainly focuses on the proposed high-temperature gate driver circuit for wide variety of SiC power switches. The design procedures for all the blocks constituting the driver circuit are also discussed in this chapter. Chapter 4 introduces a new ultra low power on-chip temperature sensor circuit that can work at very high ambient temperatures (>200 °C). Prototype gate driver and temperature sensor circuit implementation, test setup development, and measurement results are presented in Chapter 5. Finally, a conclusion of this research work has been drawn and few recommendations for further improvement of the circuits presented in this dissertation are discussed in Chapter 6.

1.8 Publications Resulting from This Dissertation Work

1. **M. A. Huque**, L. M. Tolbert, B. Blalock, S. K. Islam, "SOI-based high-voltage, high-temperature integrated circuit gate driver for SiC-based power FETs," *IET Proceedings on Power Electronics*, vol. 3, 2010, (accepted - in press).

2. **M. A. Huque**, B. J. Blalock, B. McCue, N. D. Bull, L. Zuo, S. K. Islam, and L. M. Tolbert, "A universal BCD-on-SOI gate driver IC for SiC based extreme temperature power electronics applications," in *Proc. of Workshop on Frontiers in Electronics (WOFE-09)*, Rincon, Puerto Rico, Dec. 13–16, 2009.

3. **M. A. Huque**, L. M. Tolbert, B. J. Blalock, and S. K. Islam, "A High-Temperature, High-Voltage SOI Gate Driver IC with High Output Current and On-Chip Low-Power Temperature Sensor," in *Proc. of 42nd International Symposium on Microelectronics*

(IMAPS 2009), San Jose, CA, Nov. 1–5, 2009.

4. **M. A. Huque**, S. K. Islam, B. J. Blalock, and L. M. Tolbert, "Diode leakage current based low power, on-chip high temperature sensor circuit," in *Proc. of 18th Annual Symposium on Micro- and Nano-technologies for Electronics, Photonics, Biosensors, and Alternate Energy Sources (CMOC 2009)*, Yale University, New Haven, Connecticut, March 11, 2009, pp. 57–58.

5. **M. A Huque**, S. K. Islam, B. J. Blalock, C. Su, R. Vijayaraghavan, and L M. Tolbert, "Silicon-on-insulator based high-temperature electronics for automotive applications," in *Proc. of IEEE International Symposium on Industrial Electronics (ISIE 2008)*, Cambridge, UK, Jun 30 - Jul 2, 2008, pp. 2538–2543.

6. **M. A Huque**, B. J. Blalock, C. Su, R. Vijayaraghavan, S. K. Islam, and L. M. Tolbert, "SOI based integrated circuits for high-temperature applications," in *Proc. of International Conference and Exhibition on High Temperature Electronics (HiTEC 2008)*, Albuquerque, New Mexico, USA, May 13–15, 2008.

7. **M. Huque**, R. Vijayaraghavan, M. Zhang, B. Blalock, L. Tolbert and S. Islam, "An SOI-based high-voltage, high-temperature gate-driver for SiC FET", in *Proc. of IEEE Power Electronics Specialists Conference (PESC 2007)*, Orlando, Florida, USA, 17–21, June 2007, pp. 1491–1495.

Chapter 2

Semiconductor Materials, Devices, and Design Techniques for High-Temperature Power Electronics Applications

Several physical effects make it difficult to build semiconductor devices and circuits that can reliably operate at high temperatures for an extended period of time. Many authors have described the challenges of operating electronics at extreme environment conditions [2, 22–25]. With the increase of operating temperature the following effects take place in semiconductor materials and devices:

1. Intrinsic carrier density increases
2. Junction leakage current becomes more prominent
3. Device mobility and threshold voltage changes
4. Device models become less reliable
5. Increasing electromigration of conductors
6. Diffusion of dopants increases

7. Dielectric breakdown strengths decreases

8. Mechanical stress becomes significant due to expansion mismatches and thermal cycling

With the increase of temperature the other fundamental effects that occur in integrated circuits are:

1. Increased electrical resistances of interconnects and contacts

2. Decreased electrical resistance of insulating materials and hence increased leakage charge

3. Increased thermal expansion coefficients

4. Increased chemical and metallurgical activity and interactions within and between materials, especially of ohmic contacts

5. Decreased thermal conduction for good conductors

6. Increased thermal conduction for poor conductors

Controlling these effects is critical for integrated circuits designed to operate at high temperatures.

2.1 Temperature Effects on Semiconductor Devices

There are several factors, both intrinsic and extrinsic to the semiconductor, which govern the high-temperature operation of semiconductor electronic devices and circuits. Proper understanding of these factors will help realize the role of wide bandgap semiconductors at higher temperatures. This section briefly describes the prominent physical limitations of operating semiconductor devices at higher temperatures.

2.1.1 Intrinsic Carriers

The concentration of intrinsic carriers (n_i in cm^{-3}) in undoped semiconductor is exponentially dependent upon the temperature of the semiconductor [26].

$$n_i = \sqrt{N_C N_V} e^{-E_G/2kT} \tag{2.1}$$

In Equation 2.1, T is the absolute temperature in Kelvin, k is the Boltzman constant ($8.62 \times 10^{-5}\,\text{eV/K}$), E_G is the semiconductor energy bandgap in electronvolts (eV), and N_C and N_V are the effective electron and hole density of states, respectively in cm^{-3}. E_G, N_C, and N_V are the fundamental crystal properties which are relatively temperature independent compared to the temperature exponential term in Equation 2.1. Figure 1 in [27] shows the temperature dependence of intrinsic carrier concentration for silicon, 6H-SiC, and 2H-GaN. At room temperature, n_i of silicon is $10^{10}\,\text{cm}^{-3}$, which is negligible compared to the typical device doping levels (10^{14} to 10^{17}). At 300 °C or higher ambient temperatures, intrinsic carrier density in silicon become comparable to the dopant carriers and thus loses the property of extrinsic semiconductor. Wide bandgap semiconductors ($E_G \geq 3\,eV$) such as SiC and GaN have much lower intrinsic carrier concentration to start with and hence do not run into the uncontrolled intrinsic carrier conductivity until much higher temperature is reached (beyond 600 °C).

2.1.2 Junction Leakage

p-n junction is one of the most important functional structures in most semiconductor electronic devices. This rectifying junction, when forward biased, usually conducts current in one direction and prevents current flow in the opposite direction when reverse bias voltage is applied. The current that flows through the p-n junction under reverse bias condition is known as the leakage current. For most circuit applications, leakage current of p-n junction needs to be kept negligible compared to the actual signal currents for proper operation of the circuit. Leakage current of a reverse biased p-n junction at temperatures below 1000 °C can be estimated by Equation 2.2 [27]

$$I \cong -qAn_i \left[\frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right] \tag{2.2}$$

where A is the p-n junction area in cm^2, N_D is the n-type doping density in cm^{-3}, W is the width of the depletion region in cm at certain reverse bias voltage, D_P is the hole diffusion constant in cm^2/s, and τ is the effective minority carrier lifetime in seconds.

Equation 2.2 clearly shows that the leakage current of a reverse biased p-n junction is directly proportional to the intrinsic carrier concentration ni of that semiconductor material. The exponential temperature dependence of n_i is more prominent than smaller temperature dependence of other parameters in Equation 2.2 [27]. Hence, reverse-biased junction leakage currents increase exponentially with temperature. Since wide bandgap materials have significantly lower intrinsic carrier density (n_i) compared to silicon, their leakage currents are an order of magnitude smaller than the same for silicon. WBG semiconductor based devices are capable of operation in excess of 600 °C with respect to this fundamental limitation [27].

2.1.3 Schottky Leakage

Device leakage current due to tunneling of carriers through an energy barrier (by gaining sufficient energy) increases with temperature as carriers gain more thermal energy. The reverse leakage current in an ideal Schottky barrier diode is approximated by [26, 28]

$$J_S \approx A^* T^2 exp\left(\frac{-q\Phi_B}{kT}\right) \tag{2.3}$$

where A^* is an effective Richardson constant and Φ_B is the Schottky-barrier height for thermionic emission. From Equation 2.3 it is easy to realize that Schottky leakage current is exponentially reduced as the effective semiconductor-metal barrier height Φ_B is increased. Practical Schottky barrier contacts based on most semiconductors have effective barrier heights typically less than 75% of the bandgap energy. Hence, silicon having 1.1 eV energy bandgap, has Schottky barrier heights practically limited to less than 0.9 V. On the other hand, wide bandgap semiconductors with higher than 3 eV bandgap can have barrier heights twice as large as can be achieved with silicon. This is why WBG materials can have several orders of magnitude lower leakage current at any given temperature

compared to silicon. This property allows the fabrication of wide bandgap semiconductors especially SiC-based high-voltage, high-temperature Schottky power rectifiers, which were not available in the past using conventional Si or GaAs materials.

Leakage currents represent the ultimate limiting factor with respect to high-temperature operation of the bulk-silicon based conventional electronics. At high enough temperatures, the drain-to-body leakage currents can increase by orders of magnitude and can become comparable to the drain-to-source channel current. In this condition the transistor can no longer be turned OFF by the gate control voltage.

2.1.4 Threshold Voltage Shifts

Threshold voltage of a device controls the coordinated interaction of that device with other devices within a circuit. One critical failure mechanism associated with MOSFET and IGBT structures at high temperature is the degradation of the gate oxide due to penetration of high energy carriers into the oxide beneath the gate metal. With sufficient temperature and high enough applied electric field, mobile electrons and holes can enter and propagate through the gate oxide, leaving behind damaged and trapped charges in the oxide as well as at the oxide/semiconductor interface. This process results in the degradation of the gate insulator's electronic properties, including a shift in the device threshold voltage. Change in this threshold voltage can cause circuit performance degradation or even failure [26].

2.1.5 Mobility Degradation

With the increase of temperature, atoms in the semiconductor crystal lattice acquire more thermal vibrational energy, which causes more collisions with carriers moving through the crystal in response to an applied electric field. This results in the carrier mobility degradation with the increase of temperature. This decrease in mobility with the increase of temperature reduces the current carrying capability of the semiconductor devices. For most semiconductors including silicon and WBG, device resistance increase (due to mobility degradation) with temperature follows a T^m power law relation, where m is typically between 1.5 to 2.5 [26].

2.1.6 Electromigration

Another critical chip failure mechanism that becomes more severe at elevated temperature is electromigration of metal interconnects. In this process current flow through metal trace in an integrated circuit over time gradually displaces microscopic metal particles, eventually leading to open circuit type failure. One way to minimize electromigration is to overdesign the metal interconnects and contacts with relatively large cross-sectional areas to minimize the current density through them.

2.2 Limitations of Silicon Based Power Devices

Demand for semiconductor power switches capable of operating at junction temperatures higher than 150 °C along with high blocking voltages, high switching frequencies, and high power densities are growing especially for automotive, well-logging, geo-thermal, nuclear, and aerospace applications. Silicon based existing devices are not capable of meeting these rigorous requirements without employing bulky thermal management systems and combining large number of devices in series (to increase the blocking voltage range) and in parallel (to increase the current rating) [17]. All these modifications add additional weight and volume to the Si-based power electronic circuits.

Excessive leakage current is a major concern for bulk silicon based devices at temperatures above 150 °C. This can lead to such ON-state to OFF-state current ratios which are unacceptable for most of the circuits' functionality. Low OFF-state current is a key requirement for successful integration of millions of silicon transistors in the same chip. Low leakage current minimizes the unwanted signal crosstalk between neighboring devices and also prevents latchup related failures. The drain-to-substrate p-n diode is the primary path of OFF-state leakage current in bulk silicon based MOSFET's structure. Any technique that reduces this leakage current would expand the upper temperature limit for Si-based devices. One such device topology is the silicon-on-insulator (SOI) which is briefly discussed later in this chapter.

Silicon power MOSFETs suffer from relatively large conduction losses due to high ON-state resistance, R_{dsON}. As the blocking voltage increases, so does R_{dsON}. For this reason Si-MOSFETs are not that popular beyond 600 V applications even at low temperatures.

2.3 Choice of Semiconductor Materials for High-Temperature, High-Voltage Power Switches

Silicon is the most commonly used semiconductor material for realization of commercial solid-state electronics. In comparison to silicon, wide bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) offer several advantages. The superior physical properties of these WBG semiconductors offer a lower intrinsic carrier concentration (10–35 orders of magnitude), a higher electric breakdown field (4–20 times), a higher thermal conductivity (2–2.5 times), when compared to silicon [17]. Among the wide bandgap semiconductor materials, SiC has drawn more attention from a number of research groups and organizations. Its wide bandgap energy of 2.2–3.3 eV is larger than the 1.1 eV bandgap of silicon. In addition, SiC has higher electric breakdown field of 3×10^6 V/cm, which is an order of magnitude larger than that of silicon. Several important electrical properties of 4H- and 6H-SiC polytypes in comparison with Si, GaAs, and GaN have been compiled by the author in [29] using several references cited there. Table 2.1 reproduced the material properties presented in [29].

Semiconductor electronic device functionality is typically bounded in the temperature range where intrinsic carrier densities are negligible compared to the intentionally introduced dopant impurities to control the conductivity. With the increase of temperature, intrinsic carrier density increases exponentially which causes undesired level of leakage current. At higher temperatures, when intrinsic carrier concentration becomes comparable to intentional device dopings, conductivity of the semiconductor device becomes uncontrolled. The intrinsic carrier density of silicon generally (depending upon specific device operation) limits its operation to junction temperatures less than 300 °C [29]. On the other hand silicon carbide's much lower intrinsic carrier density allows (at least theoretically) device operation at junction temperature exceeding 800 °C. SiC device operation at 500 °C has been experimentally demonstrated by various groups [18–20].

The high electric breakdown field of SiC allows thinner epitaxial layers to support higher breakdown voltages in power devices. Typically a 5000 V SiC power device would require only $40 - 50\,\mu$m drift layer, as opposed to almost $500\,\mu$m in case of silicon. A smaller drift layer leads to low drift resistance, hence, low forward voltage drop and reduced conduction

Table 2.1: Physical properties of important semiconductors at 300 K.

Property	Si	GaAs	4H-SiC	6H-SiC	GaN
Bandgap (eV)	1.1	1.42	3.2	3.0	3.4
Relative dielectric constant	11.9	13.1	9.7	9.7	9.5
Breakdown field $N_D = 10^{17}\,\mathrm{cm}^{-3}$(MVcm^{-1})	0.6	0.6	3.0	3.2	2–3
Thermal conductivity (W/cm − K)	1.5	0.5	3–5	3–5	1.3
Intrinsic carrier concentration (cm^{-3})	10^{10}	1.8×10^{10}	$\sim 10^{-7}$	$\sim 10^{-5}$	$\sim 10^{-10}$
Electron mobility at $N_D = 10^{16}\,\mathrm{cm}^{-3}$ (cm^{2}V^{-1}s^{-1})	1200	6500	800	400	900
Hole Mobility $N_A = 10^{16}\,\mathrm{cm}^{-3}$ (cm^{2}V^{-1}s^{-1})	420	320	115	90	200
Commercial wafer diameter in 2005 (cm)	20	15	7.6	7.6	None

losses. Reduction in drift layer thickness also reduces the minority carrier charge storage and greatly increases the switching frequency of SiC devices. Silicon carbide's carrier saturation velocity (2×10^7 cm/s) is also an order of magnitude larger than the same of silicon. The high thermal conductivity ($\sim 4 - 4.5$ W/cm.K) of SiC permits a power density increase which facilitates more compact switching devices with much higher power per area.

2.4 High-Temperature Power Devices: Role of Silicon Carbide

In any power converter modules, normally large conducting current flows through the power semiconductor devices. A part of this power is typically dissipated into the resistance of the drift region employed to sustain the large blocking voltage. Also during switching instances (ON and OFF operations) some dynamic power is lost due to the finite time required for the removal of charges in the device channels [26, 30]. Higher switching frequency operation of power devices is important to minimize the size and weight of the power converter modules [31]. At higher switching frequencies dynamic power dissipation becomes

significant. OFF-state leakage current that flows while the power device is blocking a high voltage at high temperature can also lead to undesired power dissipation. These power dissipations contribute to the temperature rise inside the device well beyond the ambient temperature. Besides, these power losses increase with the increase of junction temperature, making things worse.

Proper thermal management is a key requirement for most of today's silicon based semiconductor power systems, even for room temperature operations. When the ambient temperature starts to exceed 200 °C, it becomes extremely problematic to ensure reliable cooling of internal junctions in high-power silicon devices. Power devices are typically designed to carry huge ON-state current (hence, large junction area, A) when forward biased and have to block much higher voltages when reverse biased. Therefore, reverse-biased leakage currents are appreciably larger in power devices than in signal level devices. Even for lateral silicon-on-insulator (SOI) power devices, heat removal problem is aggravated by the poor thermal conductivity of the insulating oxide layers incorporated to reduce the leakage currents. Hence SOI technology cannot increase operating temperature range of the silicon power devices to the level that it can do for low-power devices [27].

The material properties required to meet the challenging high-power application at high-temperature environments can only be found in the wide bandgap semiconductors. The inherent ability of WBG semiconductor junctions to properly rectify with low reverse leakage current at junction temperatures as high as 600 °C enables power devices to operate at higher ambient temperatures [32]. Even at low temperature range ($\leq$ 150 °C) WBG semiconductor devices show superior switching properties compared to silicon devices [17, 33]. Silicon carbide along with other WBG semiconductor materials is expected to play a vital role in realizing high-power electronics beyond the limit of silicon, especially at elevated temperatures.

Silicon carbide high-temperature, high-power, solid-state devices promise incredible advantages that could significantly improve the existing transportation systems and power usage all over the world. SiC power devices allow up to ten times higher frequency operation with low switching losses and higher junction temperature in the 200 °C to 300 °C range [17]. Several key system level benefits can be achieved from these special properties of silicon carbide devices [17, 18].

1. SiC unipolar devices have lower ON-resistance (R_{ON}) due to thinner device dimension. With lower R_{ON}, SiC devices have lower conduction losses; therefore SiC-based converters have higher overall efficiency.

2. High switching frequency operation allows reduction in the size of inductors and capacitors for a given power rating, thereby increasing the power-to-volume and power-to-weight ratios.

3. Higher junction temperature and lower switching losses result in higher power efficiency because less power is dissipated and it is disposed of at a higher rate. Through simulation based studies authors in [34] predicted a 50% power density improvement for a 100 V to 2 kV DC-DC boost converter by replacing power switches made of silicon by silicon carbide. The assumptions made in this study include a switching frequency change from 50 kHz to 500 kHz and a junction temperature change from 150 °C to 300 °C, which are quite reasonable for SiC power devices.

4. In [18] authors have revealed that by using SiC devices instead of their Si counterparts in a hybrid electric vehicle (HEV) traction drive the size and weight of heatsink can be reduced by two-third. Typically heatsink occupies one-third the volume of the converter and weighs more than the actual electronic components.

2.5 Challenges of Wide Bandgap High-temperature Technology

For the last three decades, wide bandgap semiconductors are well recognized as the best materials for high-temperature electronics; however, the low material quality has not allowed the production of high quality devices until recently [1]. Among the wide bandgap materials, silicon carbide (SiC) and III-nitride (mainly GaN) based devices are the most developed technologies in today's world. For both of these materials, the difficulty in crystal growth process and the achievement of superior material quality remains a challenge. The availability of single-crystal SiC wafers at the start of the nineties initiated a great deal of research activity that led to the development of SiC-based devices. The commercialization

of SiC-based devices started with the release of blue light emitting diode (LED) [1]. On the other hand, in the absence of viable substrate technology, GaN crystals have mostly been grown on sapphire and SiC. Traditionally, SiC device crystals have orders of magnitude fewer crystal defects compared to GaN. The unavailability of low defect density substrates and defect free material limits the GaN device fabrication advancements. Hence more wide bandgap research targeted for high ambient temperature devices has been carried out on SiC than GaN.

Crystal dislocation defects present in both SiC wafers cause larger leakage current than the best that can be achieved based on material properties [35]. Blocking voltage limits of SiC power devices also degrade as larger device area encompasses more crystal defects [36]. Besides these major issues, variations in layer doping and thickness across the wafer and surface morphological defects can also harm SiC power device quality. SiC MOSFETs and IGBTs are still facing two prime challenges, particularly in the area of oxide growth and carrier mobility [17, 29]. First, low effective mobility in SiC MOS channel makes it difficult to develop low threshold and high current density power MOSFETs [37]. Second, SiC oxides have reliability concerns for long time operation. SiC MOSFETs are more prone to threshold voltage shifts, gate leakage, and oxide failures than comparably biased silicon MOSFETs [29]. SiC oxide exhibits undesirably higher levels of interface state densities ($\sim 10^{11} - 10^{13}\,\mathrm{eV}^{-1}\mathrm{cm}^{-2}$), fixed oxide charges ($\sim 10^{11} - 10^{12}\,\mathrm{cm}^{-2}$), charge trapping, carrier oxide tunneling, and lowered mobility of inversion channel carriers [29].

Realization of the full potential of wide band gap SiC for electronic and optical applications is critically dependent on the production of large diameter, defect free single crystals of high crystalline quality and precise impurity control. Commercial 4H-SiC wafers are currently available up to 75 mm and 100 mm in diameter. Historically, SiC technology has suffered due to the presence of open core dislocations or micropipes in the substrates and epilayers [1, 38]. Micropipes are essentially small holes (of diameter $\sim 1\,\mu$W) running through the wafer from top to bottom. The micropipes cause diodes to fail at certain voltage levels which are significantly lower than the voltage at which avalanche breakdown occurs [39]. Recent progress in SiC processing technology has resulted in significant reduction of micropipe density in 75 mm 4H-SiC wafers, from a previously typical value of above $100\,\mathrm{cm}^{-2}$ to a value of as low as $0.22\,\mathrm{cm}^{-2}$ in R&D samples [1]. The micropipe density in

commercially available substrates are $<30\,\mathrm{cm}^{-2}$ for n-type materials. Recent improvement in the reduction of micropipe densities has facilitated the fabrication of high-power SiC devices with reasonable yield.

Low angle grain boundaries, also known as domain walls, is another class of defects in SiC which is responsible for leakage currents and device failures [1]. This may also cause wafers to crack during epitaxial processing. Another type of defects, known as threading screw dislocations, is suggested to have an impact on the leakage behavior of Schottky diodes. The so-called basal plane dislocation is another important and significant defect mechanism that has detrimental effects in the forward voltage characteristics of p-i-n devices [1]. It is critical to reduce the density of these dislocations in epitaxial layers for stable device fabrication. There is a positive correlation between dislocation density and reduced breakdown voltages. A dislocation density of less than $10\,\mathrm{cm}^{-2}$ is desirable for the fabrication of power devices for high temperature operation [38].

In any realistic power electronic circuits, junction temperature of power devices can be significantly higher than the ambient due to self-heating effect. The maximum current and power ratings of a power device are typically limited by the maximum junction temperature of the device. Such self-heating related upper temperature limit can cause the following two failure mechanisms in devices [40]:

1. Power losses (switching and conduction) inside the device cause its junction temperature to increase beyond the semiconductor material temperature limit. At much higher temperatures, excessively and exponentially increasing leakage current quickly damages the integrity of the materials used to fabricate the power device.

2. Increasing junction temperature due to switching and conduction losses leads to more device losses and hence sets up a positive feedback mechanism. A thermal runaway condition can be initiated at a temperature much lower than the critical temperature of the materials.

Most silicon power devices fail because of the first mechanism mentioned above. For SiC power devices, the first mechanism is unlikely to take place due to its high intrinsic temperature handling capability. Maximum junction temperature of SiC power devices is most

likely to be dictated by the Ohmic/Schottky contact metal temperature limit, the passivation/ packaging materials' temperature limit, or the thermal runaway situation mentioned in the second failure mechanism above. Based on fundamental physical models and experimental data, the author in [40] concluds that different SiC devices, with the exception of MOSFETs, may become thermally unstable (i.e. runaway) at junction temperatures as low as 200 °C. Hence, careful consideration and study is needed from researchers and engineers building high-temperature power modules using SiC devices.

Wide bandgap semiconductors, especially SiC, will ultimately revolutionize power electronics by allowing simultaneous realization of high-temperature, high switching-frequency, and very high-voltage operation that cannot be met with conventional technologies like bulk silicon or silicon-on-insulator. High-temperature capability will allow the operaion of power electronics in harsh environments like automotive, aerospace, energy production, and other industrial systems with minimal thermal management. Higher switching frequencies will lead to substantial reduction in size and weight if the passive filtering components. Higher blocking voltages will enable the use of fewer devices (in series) for high-voltage applications, and higher current density will also require fewer devices (in parallel) for high-power applications. Currently, SiC-based high-temperature electronics is classified as a "niche" market technology. However, this technology still offers tremendous advantages to several electrical or electro-mechanical systems which will have impact on modern everyday life all over the world.

2.6 High-Temperature Design Techniques

The scientific community is addressing the high-temperature circuit design challenges in different ways. Figure 2.1 shows the concept of these different approaches. From a material science point of view, the best way to fabricate high-temperature devices is to use wide bandgap materials. From a device perspective, the way to handle this problem is to improvise new device structures which can remove or at least minimize some of the temperature effects to increase the maximum operating temperature range of the devices. One result of this approach is the silicon-on-insulator (SOI) technology which uses the same silicon semiconductor material, yet due to insertion of insulating buried oxide layer, its leakage

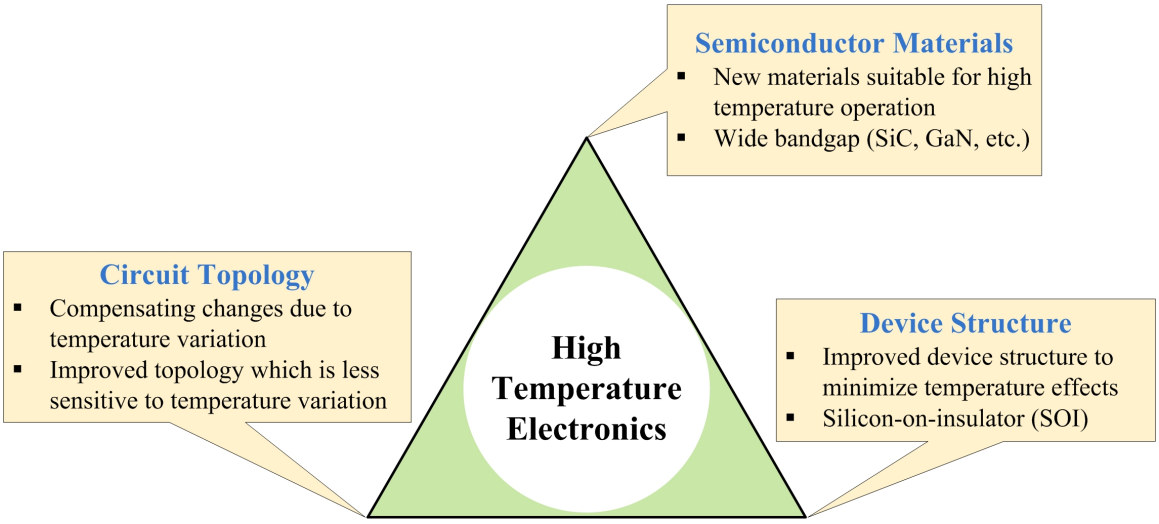


Figure 2.1: Three ABCs of addressing high-temperature design challenges.

current is reduced significantly. Circuit designers can also attemp to invent new topologies which are less sensitive to the device parameters that are highly dependent on temperature. These designs can also compensate for some of the changes that take place caused by the temperature variation to obtain temperature independent performance.

2.7 Silicon-on-Insulator (SOI) technology

Wide bandgap semiconductors are capable of electronic functionality at much higher temperatures than silicon. In the future, wide bandgap semiconductors will be the primary choice for simultaneous realization of high-power and high-temperature solid-state devices. Silicon carbide and III-nitride (mainly gallium nitride) based devices are the most widely researched wide bandgap semiconductors to date. Considering the technological advancements, at present time SiC is considered to be the material of choice for realization of power switches for high-temperature applications. However, SiC-based power switches are not yet commercially available. In addition, the SiC-based integrated circuit design process will take even longer time to become commercially available. For low or medium power needs up to 300 °C, the solution is silicon-on-insulator (SOI), which is commercially available for integrated circuit development [27, 41, 42].

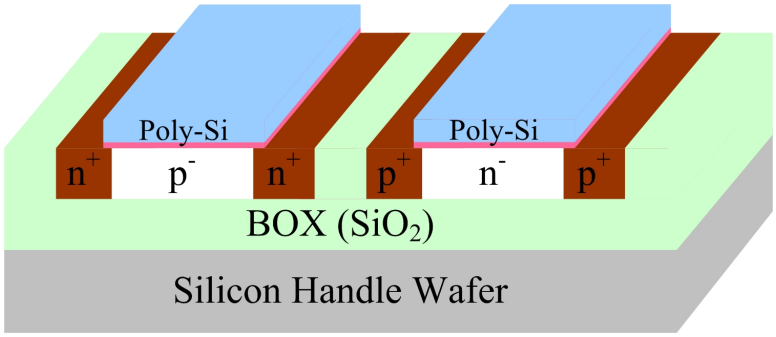


Figure 2.2: Conceptual cross sectional view of on an SOI-CMOS structure.

Silicon MOSFET with reduced OFF-state leakage current for higher temperature operation can be realized by the silicon-on-insulator (SOI) structure as shown in Figure 2.2. Buried insulator layer in SOI structure greatly decreases the leakage paths associated with the drain and the source p-n junctions that exist in bulk silicon processes. In SOI technology the junction leakage is decreased by a factor of 100 compared to bulk silicon process [27].

The presence of the buried oxide also reduces OFF-state source-to-drain carrier emission leakage that physically occurs in the p-type substrate of bulk Si-MOSFETs. The threshold voltage variation with temperature is smaller in SOI devices than in bulk devices [42]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperatures [42]. These make SOI-based circuits capable of operating successfully in the 200 °C–300 °C temperature range which is well above the range of conventional bulk silicon based devices. Other semiconductor structures, such as bipolar transistors, high-voltage DMOS, etc. have also been implemented using SOI process technology [43].

SOI and SiC technologies appear to be the best choices at this time to realize high-power systems for high-temperature applications. SiC is suitable for power electronics with the ability to handle large voltages, currents, and temperatures. SOI and SiC are also complementary technologies. SOI provides the necessary control and amplifications, while SiC supplies the power to the actual load. The authors in [27] outline some of the well known high-temperature electronics application areas and suggest appropriate technologies for them (Table 2.2). Future realization of wide bandgap semiconductors in those areas will

largely depend on the progress of processing technology. The power requirement mentioned in Table 2.2 is defined as the maximum blocking voltage times the maximum operating current.

The SOI technology is commercially available for a variety of applications, including high-temperature and radiation hardened electronics. Several SOI-based semiconductor foundry services are commercially available for typically low-power digital and analog applications [44–48]. For the design and implementation of a high-temperature, high-voltage gate driver circuit presented in this dissertation, a Bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (SOI) process that combines the advantage of high-voltage devices with SOI technology has been used [44]. This process is a 0.8–micron, 2–poly, 3–metal process.

2.8 Zero-Temperature-Coefficient (ZTC) Biasing Technique for High-Temperature Circuit Design

The zero-temperature-coefficient (ZTC) bias point corresponds to a particular gate voltage and drain current operating point which remains constant over the temperature range. It is a well established experimental fact that both n- and p-channel MOSFETs exhibit ZTC bias conditions, both in the linear and saturation regions of operation [41, 49]. Figure 2.3 shows the transfer characteristics of a low-voltage SOI NMOS device ($W = 4 \times 4\,\mu\text{m}, \text{L} = 4\,\mu\text{m}$) for a temperature range of $-50\,^{\circ}\text{C}$ to $250\,^{\circ}\text{C}$. For this NMOS device, the ZTC bias condition is $V_{GS\_ZTC} = 1.46\,\text{V}$ and $I_{GS\_ZTC} = 25.7\,\mu\text{A}$. Transfer characteristics of a low-voltage SOI PMOS device ($W = 2.6 \times 4\,\mu\text{m}, \text{L} = 4\,\mu\text{m}$) for the same temperature range is shown in Figure 2.4. For this device, the ZTC bias point is at $V_{GS\_ZTC} = 1.8\,\text{V}$ and $I_{GS\_ZTC} = 25\,\mu\text{A}$. By biasing a circuit at ZTC point, temperature independent performance is obtained over a fairly large temperature range. In Chapter 3 ZTC bias condition based design of a temperature independent dead-time controller circuit and voltage level shifter circuit are presented. These are the two critical functional blocks in the proposed high-temperature gate driver circuit.

Table 2.2: Semiconductor technologies for some selected high temperature electronics applications.

High-temperature Electronics Applications	Peak ambient temperature	Power requirement	Current technology	Future technology
Automotive				
Engine control electronics	150 °C	<1 kW	BS & SOI	BS & SOI
On-cylinder & ehaust pipe	600 °C	<1 kW	NA	WBG
Electronic suspension & brakes	250 °C	>10 kW	BS	WBG
Electric/hybrid vehicle PMAD	150 °C	>10 kW	BS	WBG
Turbine engine				
Sensors, telemetry, and control	300 °C	<1 kW	BS & SOI	SOI & WBG
	600 °C	<1 kW	NA	WBG
Electric actuation	150 °C	>10 kW	BS & SOI	WBG
	600 °C	>10 kW	NA	WBG
Spacecraft				
Power management	150 °C	>1 kW	BS & SOI	WBG
	300 °C	>10 kW	NA	WBG
Venus & Mercury exploration	550 °C	$\sim 1\,kW$	NA	WBG
Industrial				
High-temperature processing	300 °C	<1 kW	SOI	SOI
	600 °C	<1 kW	NA	WBG
Deep-well drilling telemetry				
Oil and gas	150 °C	<1 kW	SOI	SOI & WBG
Geo-thermal	600 °C	<1 kW	NA	WBG

BS: bulk silicon, SOI: silicon-on-insulator, NA: not available, WBG: wide bandgap

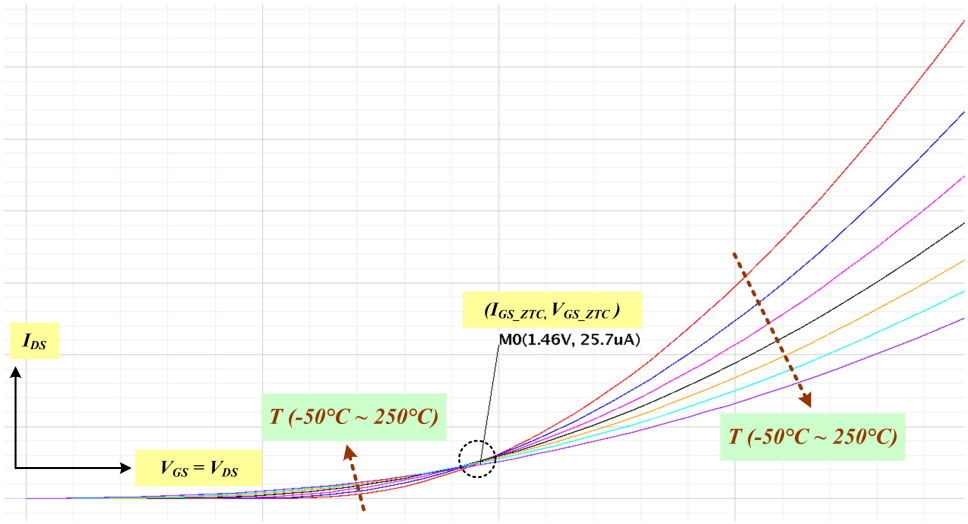


Figure 2.3: N-channel MOSFET's saturation-regime transfer curves illustrating the ZTC bias point.

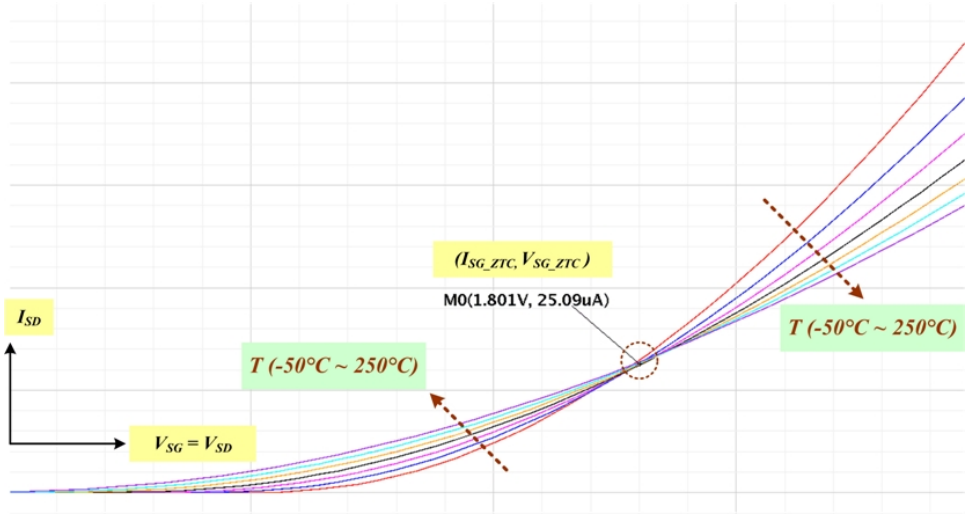


Figure 2.4: P-channel MOSFET's saturation-regime transfer curves illustrating the ZTC bias point.

Chapter 3

High-Temperature, High-Voltage SOI Gate Driver Circuit with High Drive Current

3.1 Introduction to Gate Driver Circuit

In power converters, the flow of power from source to the load is controlled by sequential turn ON and turn OFF operations of power switches. Performance of the power electronic system largely depends on the characteristics of the power switches and the ability of their drivers to efficiently control the ON / OFF operations. Figure 3.1 illustrates a simple switch-driver connection. Input pulses to the driver are low power pulses, generated by a microcontroller or DSP based system, which can not drive the power switch directly. For most cases, the voltage magnitude of this logic level signal is lower than the threshold voltage of the power switches, and lacks the current driving and sinking capability to charge and discharge the gate capacitance within a short time to minimize the switching power losses. The power supplies to the driver are V_{DD} and V_{SS}. The output of the driver, V_{OP} is connected to the terminal S of the switch, which connects and disconnects the T_1 and T_2 terminals. By providing the required voltage or current at the input of the switch (at the terminal S), the driver triggers the turn ON (T_1 and T_2 connected) or turn OFF (T_1 and T_2 disconnected) processes.

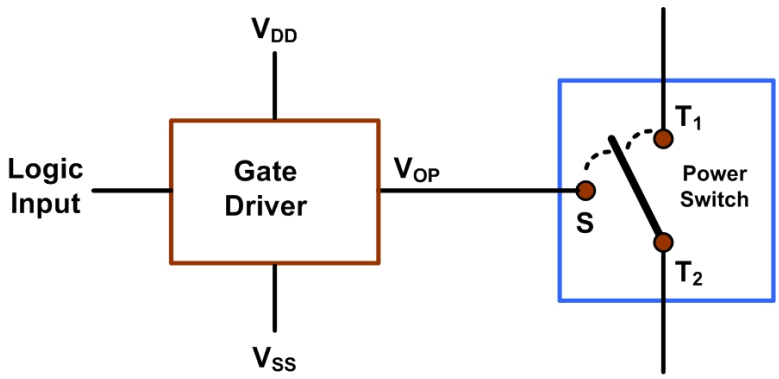


Figure 3.1: Typical switch-drive connection.

A gate driver circuit effectively serves the purpose of power amplification to boost the voltage and current levels of the low-power logic-level control signals to efficiently drive the power switches. Gate drivers may be implemented as dedicated integrated circuits, discrete transistors, or transformers. They can also be integrated within a controller IC. Partitioning the gate-drive function off the logic generator allows the controller to run cooler and more stable by eliminating the high peak currents and heat dissipation needed to drive a power switch at very high frequencies.

An important attribute for the gate driver is its ability to supply and sink sufficient drive current to quickly charge and discharge the gate capacitances associated with the power switch driven by it. Any delay in turn ON and turn OFF processes will cause dynamic power loss in the power switch. A gate driver circuit also needs to supply large enough voltage to fully turn ON the power switch. Lower gate drive voltage will force the power switch to carry huge load current with relatively large ON resistance which will cause large conduction loss in the power switch. During the turn OFF period, a gate driver circuit also needs to maintain low enough gate voltage at the gate terminal of the power switch to ensure zero leakage current while the switch is blocking large rail-to-rail voltages. Failure to ensure zero leakage current will also cause power loss inside the switch. All these power losses inside the switch will generate heat and will raise the junction temperature much higher than the ambient. This might lead to failure of the power devices in absence of robust thermal management. In addition, these device losses will reduce the overall efficiency of the power converter module.

3.2 Integrated Gate Driver Circuits Reported in Literature

Several integrated gate driver circuits have been reported in literature [50–54]. These papers addressed different important aspects of gate driver circuit however none of them were designed for high-temperature operation. Wang presented a 10 MHz low power-loss driver IC for GaN HFET devices [50]. A new two-stage positive-to-negative level shifters and resonant topology to implement the driver circuit has been presented in this paper. Smart-Voltage-eXtension (SVX), a cost-effective technique to implement high-voltage devices in standard CMOS process, was used to implement the driver circuit. This driver circuit was designed for a specific GaN HFET switching device with 100 V and 1 A power rating. Although this driver can achieve extremely high switching frequency operation (10 MHz), its output current is very low (50 mA), and no high-temperature drive capability was specified.

Li demonstrated a half-bridge driver circuit with integrated power switches implemented in Philips EZ-HV SOI process [51]. This half-bridge driver circuit is capable of sourcing 350 mA and sinking 750 mA drive current. The bootstrap capacitor (47 nF) required by this driver was not implemented on-chip and no high-temperature operation of the driver was mentioned.

The IGBT gate driver circuit presented in [52] incorporated several advanced protection features such as two-level turn ON to reduce peak current when turning ON the power switch, two-level turn OFF to limit over-voltage when the switch is turned OFF, and an active Miller clamp function that acts against cross conduction phenomena. This driver IC was implemented using $1-\mu$m BCD3S process and was optimized for 1200 V IGBT with current ratings of 25–80 A. Separated source and sink output pins in this driver allow the use of different gate current limiting resistors to adjust the turn ON and turn OFF speeds. The peak output currents of the driver circuit are 1.2 A sink and 0.75 A source in worst case over the entire temperature range ($-20\,^{\circ}$C to $125\,^{\circ}$C).

A monolithic IGBT gate driver IC with protection features implemented in a high-voltage (50 V) $0.8-\mu$m CMOS process was presented in [54]. The safety features incorporated in this gate driver include over-current protection, short-circuit protection, over-temperature protection, and under-voltage protection functions. Peak output current of

this driver IC was 100 mA, and no high-temperature operation capability was mentioned in this paper.

Power MOSFETs' and IGBTs' gate charging and discharging current monitoring based self-diagnosis scheme for a gate driver circuit is proposed in [53]. This scheme can implement several smart functions such as self-acknowledgement, gate drive connection verification, power device status diagnosis, and gate dielectric wearout detection and prediction. The method presented in this scheme can detect abnormal conditions that occur either within the gate driver circuit itself or in the driven power switch.

3.3 Commercially Available High-Temperature Integrated Gate Driver Circuits

CISSOID, a Belgium-based fabless company, has developed and marketed silicon-on-insulator based high-temperature integrated circuits for −55 °C to +225 °C junction temperature operation [55]. They have marketed two gate driver ICs which can work up to 225 °C junction temperature. Their latest high-temperature driver product (October 2009), CHT-Hyperion, is a dual n-MOSFET driver (5 V). This driver can output peak current in excess of 1 A. It requires an external bootstrap capacitor of 100 nF value. Both high-side and low-side channel can drive 1 nF load in 15 ns at +200 °C.

CISSOID's earlier gate driver IC, PALLAS CHT-FBDR, is a high-temperature full-bridge n-channel MOSFET driver comprising of two independent low-side and high-side driver channels including integrated charge pumps associated to high-side channels. This driver circuit's outputs swing from 0 to 10 V, and are able to source and sink up to 80 mA of peak current for the low side channel and 20 mA of peak current for the high-side channel.

CISSOID's board level gate driver design, CHT-PROMETHEUS, implements a 2 A power driver constructed using their in-house high temperature active components. This driver can be supplied from 11 V to 30 V and can switch up to 500 kHz on a 30 nF load. Non-overlap circuitry avoids short-circuit currents through the push-pull power output stage. PROMETHEUS drives high-voltage high-power devices (e.g. SiC transistors) and targets both electric motors and switched mode power supplies (SMPS).

3.4 Proposed High-Temperature, High-Voltage SOI Gate Driver Circuit Topology

The proposed gate driver circuit has been designed using a commercially available 0.8–micron, 2–poly, and 3–metal bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (SOI) technology. The following sections explain the block diagram of the complete system and the actual circuit operation for each block.

Block diagram level circuit topology of the proposed high-temperature SOI gate driver is illustrated in Figure 3.2. This circuit has six critical building blocks, namely half-bridge high-voltage output stage (transistor pair M_H and M_L), low-side and high-side buffers, on-chip bootstrap capacitor based charge pump, constant current bias low-side to high-side level shifters, temperature independent dead-time controller, and edge detection circuit. Input stage of this proposed gate driver includes a Schmitt trigger buffer to filter out noises from the incoming logic signal and also a logic gate to generate *Enable* signal from the feedbacks received from three different protection circuits namely temperature sensor, under voltage lock out (UVLO), and short circuit detector circuit. High-voltage output stage handles the large drive current requirement of the gate driver circuit. The high- and low-side buffers drive the gates of the high-side and low-side transistors in the half-bridge output stage, respectively. The bootstrap capacitor (C_B) based charge pump establishes a voltage above the available highest rail voltage for all the high-side devices and circuits. Level shifter circuit provides conversion of the incoming logic signal from the low-side voltage level ($V_{DD} \sim V_{SS}$) to the high-side voltage level ($V_{OP\_PLUS} \sim V_{DDH}$). The temperature independent level shifter circuits have been designed to generate active low *SET* and *RESET* signals with temperature independent pulse magnitude for the SR latch. The dead-time controller circuit generates two non-overlapping copies of the input signal with temperature independent dead-time injected between them. The dead-time provided between these two copies ensures the complementary turning ON and OFF of the high-voltage transistors in the output stage and thus prevent the short circuit current through M_H and M_L simultaneously. The purpose of the edge detection circuit is to generate the narrow pulses (S and R) at the rising and falling edges of the control signal generated by the dead-time controller circuit for control of the M_H transistor. Each of

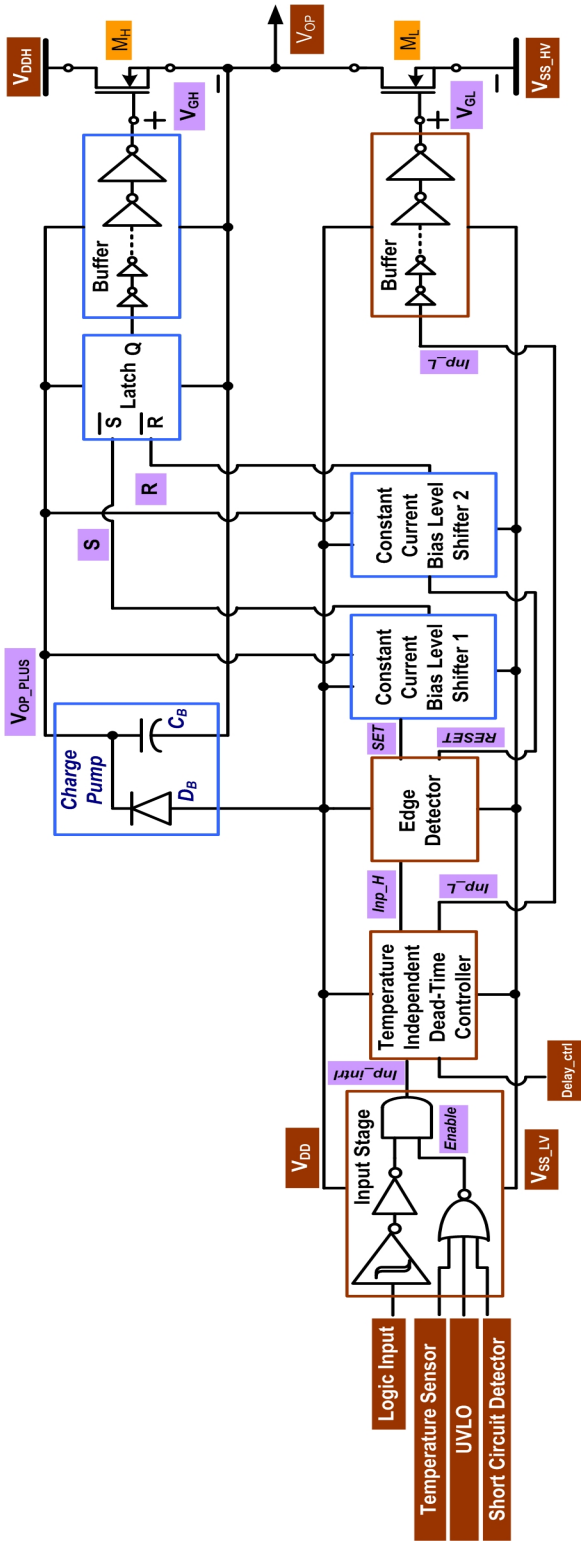


Figure 3.2: Schematic of the proposed high-temperature gate driver circuit.

these high-temperature gate driver circuit's building blocks are examined in the following sections.

3.4.1 High-Voltage Output Stage

The half-bridge output stage connects the gate terminal of the power FET to one of the two rail voltages that sets the gate-to-source voltage for the power switch. The rail voltages (V_{DDH} and V_{SS}) are applied depending on the gate drive requirement of the particular power switch that the driver IC is controlling. The key design parameters in the half-bridge design are ON-state resistance (R_{ON}), switching speed, reverse breakdown voltage, and chip area requirement. In a CMOS process, half-bridge output stage can be implemented in two different ways. In one configuration, the low-side and high-side transistors are NMOS and PMOS devices, respectively. The second configuration consists of only NMOS for high and low-side transistors. The complementary NMOS and PMOS based configuration is similar to the low voltage CMOS inverter.

For the gate driver specification set for this work, the transistors in the output stage need to be high voltage devices. The SOI process used here offers the 45 V high-voltage NMOS and PMOS transistors. NMOS transistors have lower ON resistance and higher switching speed when compared to PMOS transistors with similar voltage and current ratings. Current drive specification for this driver circuit is very high (3 A). For the same drain current, a PMOS device occupies almost 2.5 times the area of a NMOS device due to its lower mobility. For these reasons, an all-NMOS based half-bridge topology was chosen for this driver circuit.

The topology used in this circuit (Figure 3.3) consists of two high-voltage (45 V) NMOS transistors (LDMOS) stacked together. Gate voltage for the top NMOS (M_H) device is either set at V_{SS} (when M_L is ON and M_H is OFF, i.e. V_{OP}=V_{SS}) or at V_{DDH}+V_B (when M_L is OFF and M_H is ON), where V_B is the floating voltage generated by the bootstrap capacitor based charge pump circuit which can generate a voltage above the highest rail voltage [51, 56].

Sizing of the NMOS transistors in Figure 3.3 are selected to provide 5 A drive current at 200 °C with gate-source (V_{GH} or V_{GL}) voltage equal to the V_B voltage. The conceptual

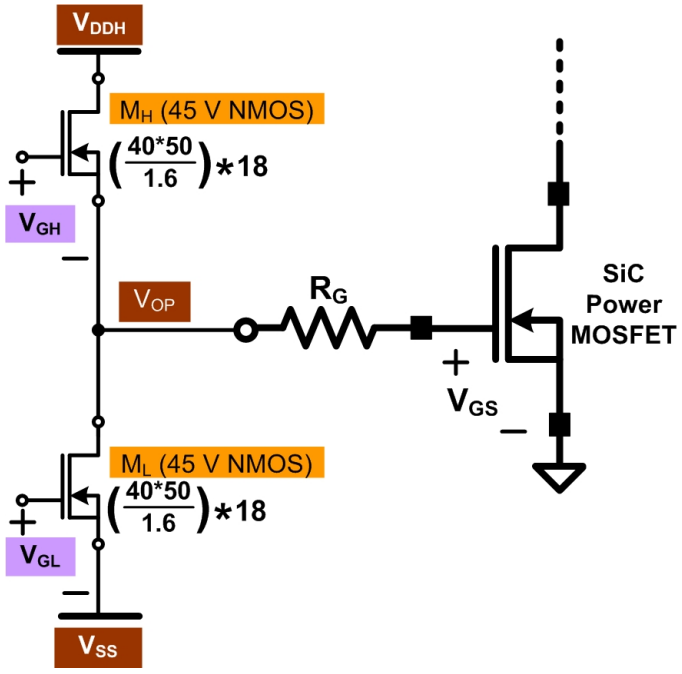


Figure 3.3: High-voltage half-bridge output stage.

timing diagrams of V_{GH} and V_{GL} with respect to the logic signal provided to this gate driver circuit (Figure 3.4). This figure also includes the expected output voltage generated by the half-bridge stage. Dead-time between V_{GH} and V_{GL} (Figure 3.4) is extremely important to prevent short circuit condition between the high voltage rails (V_{DDH} and V_{SS}). Actual magnitudes of these rail voltages depend on the SiC power switch that this circuit is driving. Table 3.1 illustrates the probable combination of these voltages for different SiC prototype power devices currently available from the manufacturers. For turning ON the M_H transistor, its gate needs to be pulled to a voltage higher than V_{DDH} which is the highest rail voltage available to this circuit. This voltage is generated by the bootstrap capacitor based charge pump circuit which is described next.

3.4.2 Bootstrap Capacitor Based Floating Voltage Supply

The bootstrap circuit, consisting of diode (D_B) and bootstrap capacitor (C_B), supplies a voltage level higher than the highest voltage made available to the chip. Figure 3.5 depicts the circuit operation of the charge pump. When the output is low (M_L is ON and M_H is

Table 3.1: Probable V_{DDH} and V_{SS} voltage combinations for different SiC power switches.

	MOSFET (Cree)	Normally ON JFET (SiCED)	Normally OFF JFET (SemiSouth)	Positive Extreme	Negative Extreme
V_{DDH}	20 V	0 V	3 V	30 V	-30 v
V_{SS}	-5 V	-20 V	-7 V	0 V	-30 v

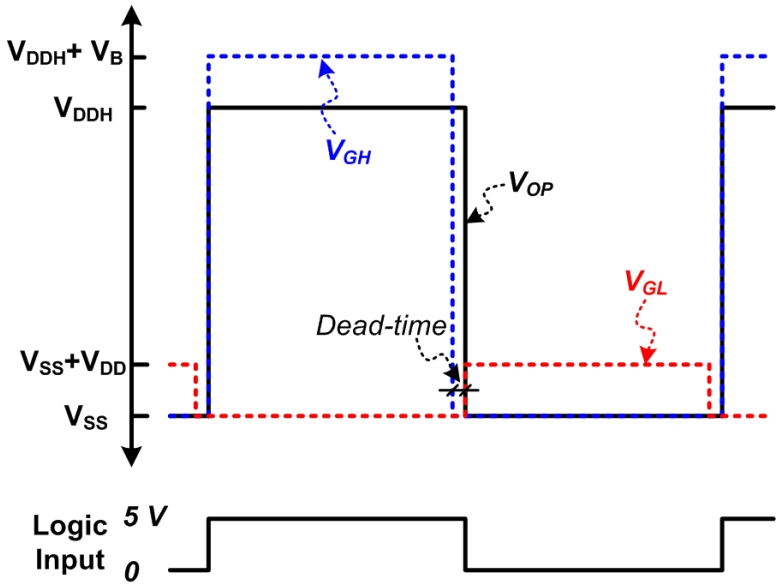


Figure 3.4: Conceptual gate-source voltages of M_H and M_L transistors required to prevent short circuit condition.

OFF) such that V_{OP} is tied to V_{SS}, the bootstrap capacitor is charged to V_B voltage which is given by 3.1

$$V_B = V_{DD} - V_{DB} - V_{M_L-ON} \tag{3.1}$$

where V_{DB} is the forward voltage drop across D_B, V_{ML-ON} is the ON voltage of the M_L NMOS tansistor, and V_{DD} is the voltage source charging the charge pump circuit. In the next phase (Figure 3.5(b)) when M_L is OFF and M_H is turned ON, the output V_{OP} starts to increase making the diode D_B reversed biased and the voltage across the capacitor starts working as a floating battery with V_{OP} working as the floating reference.

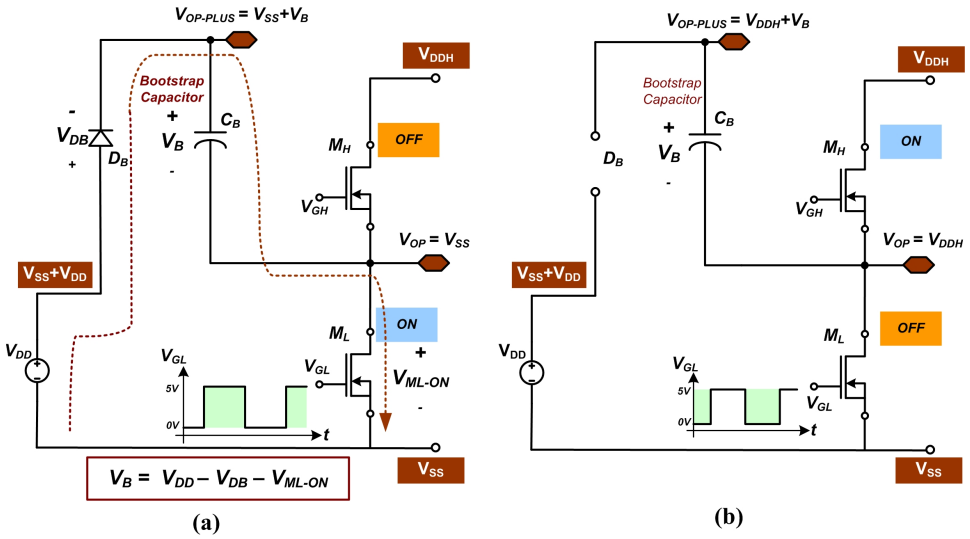


Figure 3.5: Bootstrap capacitor based charge pump operation (a) charging the capacitor and (b) voltage across capacitor working as floating battery.

This voltage is required for the high-side buffer, SR latch, and level shifters in order to generate the required gate signal (V_{GH}) for the M_H transistor. The V_{OP} and $V_{OP-PLUS}$ voltages work as the floating rail voltages for the high-side circuitry. This circuit takes 60 ns to be fully operating due to the charging of this bootstrap capacitor. To make this bootstrap capacitor on-chip, the current consumption of the high-side circuit blocks were carefully designed to consume minimum possible current from the floating supply. In this design a 1.5 nF capacitor was included on the chip, integrated with the gate driver circuit. The on chip bootstrap capacitor was implemented using accumulation mode metal-oxide-semiconductor capacitor (MOSCAP). Total die area taken by this capacitor is 1.1 mm^2. Capacitance per unit area of MOSCAP is almost two times that for a polysilicon-oxide-polysilicon capacitor, which was the other option available in the SOI process used for this work. Figure 3.6 shows the V_{OP_PLUS} signal generated by this charge pump circuit. This figure also includes the V_{OP} signal generated by the driver circuit. The difference of these two signals is the actual floating voltage (V_B) across the bootstrap capacitor.

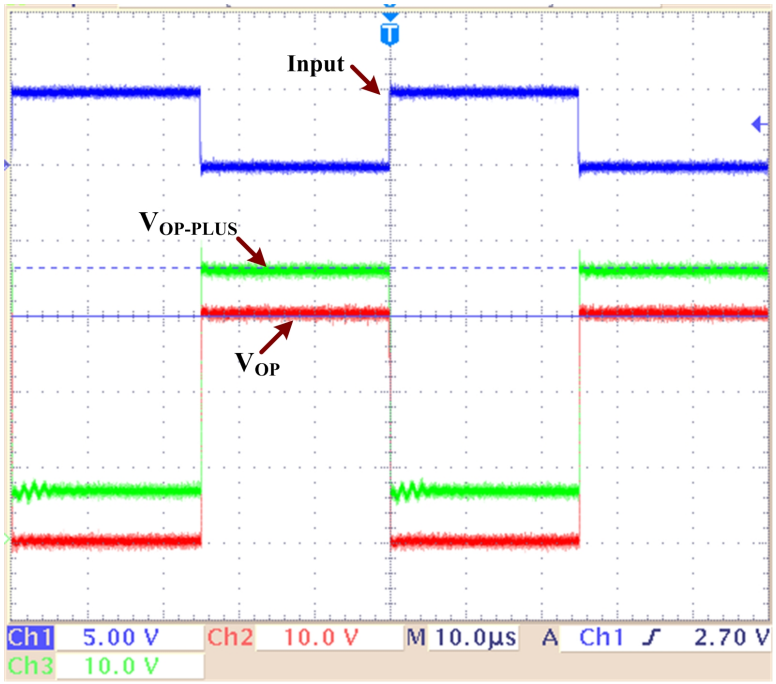


Figure 3.6: Floating voltage (V_{OP_PLUS} - V_{OP}) generated by the bootstrap charge pump circuit.

3.4.3 Buffers

Both transistors of the half-bridge stage are comprised of a large number of parallel connected high-voltage LDMOS transistors. Equivalent widths of each of these transistors are 36000 μm which presents large capacitive loads to the signals coming from the SR latch (for M_H) and dead-time controller circuit (for M_L). Multi-stage non-inverting buffers (Figure 3.7) consisting of a series of amplifying inverters are used to generate the gate signals with sufficient drive strength for the large gate capacitances of the M_L and M_H transistors. To minimize the delay through these buffers, the size of each stage was made approximately 'e' (the base of natural logarithm) times larger than its previous stage, forming the exponential "horn" pattern [57, 58]. The high-side buffer is biased by the floating voltage V_B generated by the charge pump.

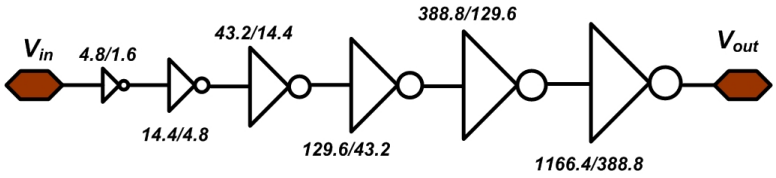


Figure 3.7: Schematic of the buffer.

3.4.4 Temperature Independent Dead-Time Controller

To reduce the power consumption of the chip and to ensure the reliability of the circuit, it is very important to maintain complementary turning ON and OFF operations of the two high-voltage NMOS transistors in the output stage. Overlapping turning ON of both transistors will create a short circuit between the rail voltages (V_{DDH} and V_{SS}) resulting in large short circuit or "crowbar" current. This large current will increase the die temperature much higher than the ambient temperature. To ensure a break-before-make type operation, a dead-time controller circuit has been designed to generate two non-overlapping copies of the input signal coming to this block from the input stage. Figure 3.8 reveals the schematic of the dead-time controller circuit and Figure 3.9 shows the conceptual wave signal associated with this block. By applying high or low voltages in the *Delay_ctrl* terminal the dead-time between inp_H and inp_L can be adjusted. These two circuits inject a dead-time between the gate drive signals (V_{GH} and V_{GL}) for the NMOS transistors M_L and M_H in the output stage.

The main building block of this circuit is the adjustable delay controller circuit which can inject a temperature independent phase shift to an incoming signal. A temperature independent current bias circuit has also been developed to provide constant current biasing to the adjustable delay controller circuit.

Temperature independent current bias circuit

Figure 3.10 illustrates the schematic of the temperature independent current bias network circuit developed using the zero-temperature coefficient (ZTC) bias condition of NMOS and PMOS transistors. Sizes of M_{P1} and M_{N1} transistors are selected such that their saturation drain-source current at ZTC bias voltage, I_{DS_ZTC} become equal i.e. I_{bias1}=I_{bias2}.

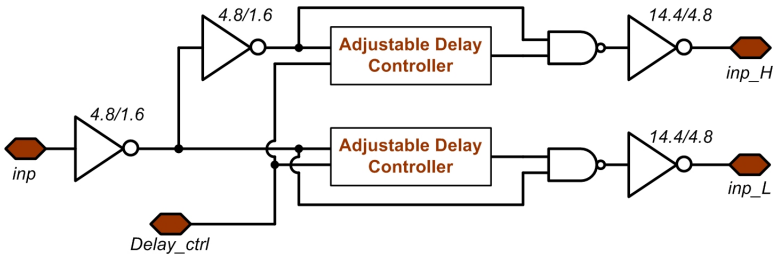


Figure 3.8: Schematic of the temperature independent current bias network circuit.

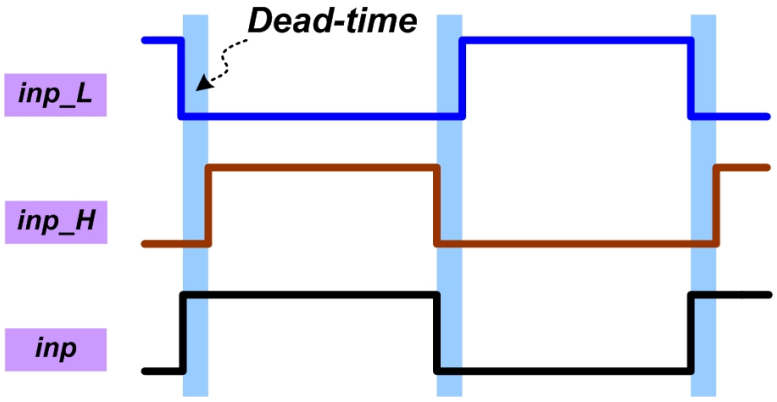


Figure 3.9: Dead-time between the two non-overlapping copies of the input signal generated by the dead-time controller circuit.

Since the current through both the PMOS and NMOS current mirror branches are equal, hence drain voltage of M_{N1} transistor tracks the V_{GS_ZTC} voltage of diode connected NMOS transistor M_{N2}. Similarly drain voltage of M_{P2} tracks V_{SG_ZTC} voltage of diode connected PMOS transistor M_{P1}. The resistance value required to keep these transistors into saturation with the ZTC bias voltages are calculated by eqution 3.2

$$R_{eq} = R_{11} + R_{12} = R_{21} + R_{22} = \frac{V_{DD} - V_{SG\_ZTC} - V_{GS\_ZTC}}{I_{DS\_ZTC}} \tag{3.2}$$

If the total resistance in each leg remains constant with temperature variation, then gate-source bias voltages of both NMOS and PMOS current mirror will remain constant across temperature. To keep the net resistance variation with temperature at a minimum level both positive temperature co-efficient and negative temperature co-efficient resistors avail-

able in the SOI process were used. the best result was obtained by sharing the R_{eq} by 3:2 ratios by the +ve (R_{11} and R_{21}) and -ve (R_{12} and R_{22}) temperature co-efficient resistors. Using this circuit, constant bias voltages, V_P for PMOS transistors and V_N for NMOS transistors were generated.

$$V_P = V_{DD} - V_{SG\_ZTC} \tag{3.3}$$

$$V_N = V_{GS\_ZTC} - V_{SS} \tag{3.4}$$

Transistors (M_{SU1} to M_{SU4}), drawn in brown color in Figure 3.10 ensures the proper start up condition for this biasing circuit.

Figure 3.11 presents the DC simulation of this bias network from $-60\,^{\circ}$C to $250\,^{\circ}$C temperature. Bias currents (I_{bias1} and I_{bias2}) in both branches are exactly the same and vary by only $1.78\,\mu$A for $310\,^{\circ}$C temperature variation. V_N and V_P voltages are almost constant across the simulation temperature range.

Delay generator circuit

Figure 3.12 shows the schematic of the delay generator circuit with the temperature independent bias network described in the previous section. Temperature independent constant bias voltage V_P is supplied to the gates of all the PMOSs, which source constant pull up currents to the inverters, and thus capacitors get charged by a constant current across the entire temperature range. Similarly, temperature independent constant bias voltage V_N is provided to all the NMOSs which sink the constant pull down current from the inverters. This ensures the same rate of discharge of the capacitors for all temperatures. Since the capacitors get charged and discharged by constant currents for the entire range of temperatures hence phase shift injected by this circuit remains almost constant for all temperatures.

Post-processing adjustment of phase shift can be achieved by changing the logic applied to the *delay_ctrl* terminal. A logic HIGH signal applied in this terminal will turn the S_1, S_2, and S_3 switches ON and will leave only the C_1 capacitors in the circuit. If logic LOW is applied, then these switches will remain OFF, and C_2 capacitors will be in parallel with the

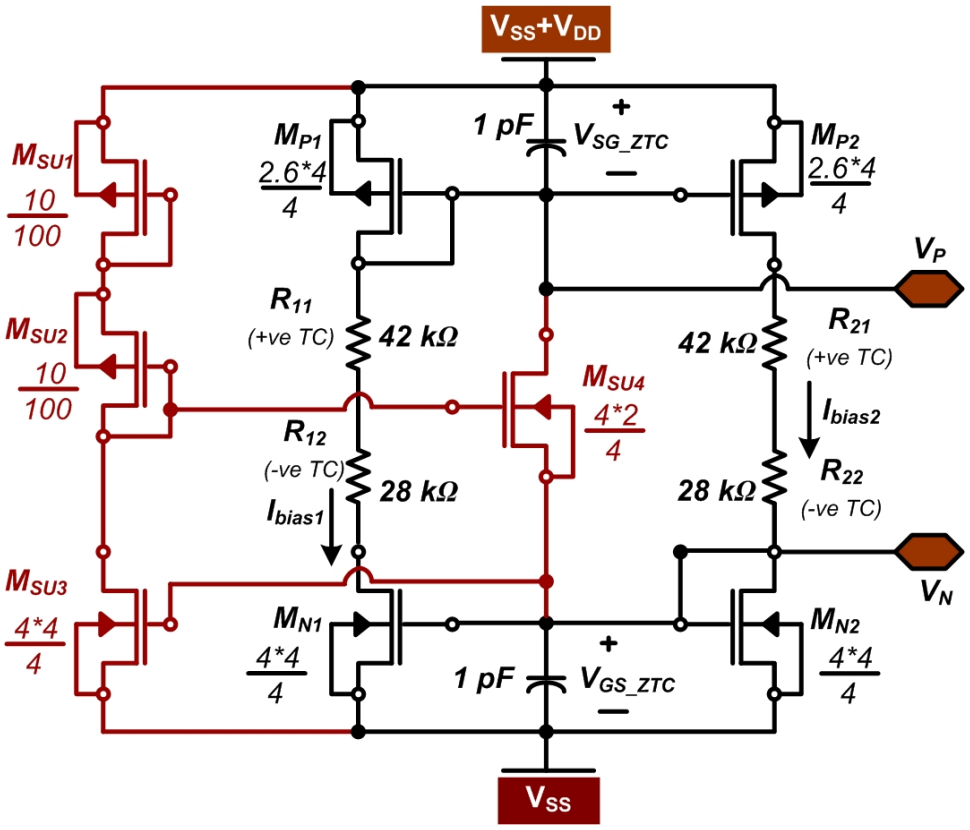


Figure 3.10: Schematic of the temperature independent current bias network circuit.

C_1 capacitors and equivalent capacitance in the output of each inverter will be 50 fF.The dead-times achieved between the non overlapping copies generated by this proposed dead-time controller circuit at different temperatures are revealed in Table 3.2.

3.4.5 Edge Detector Circuit

The inp_H signal generated by the dead-time controller circuit is used to generate the gate drive signal (V_{GH}) for the high-voltage NMOS transistor, M_H in the half-bridge output stage. The source terminal of this NMOS is tied to V_{OP} node which switches between V_{SS} and V_{DDH}. To pull this node to V_{DDH}, the M_H NMOS transistor needs to be turned ON. To switch On this transistor, it's gate terminal of this device needs to be pulled to V_{OP_PLUS} rail voltage. Consequently, there is need for level shifting the inp_H signal from V_{DD} level to V_{DDH}. Level shifting the whole inp_H signal will consume significant power

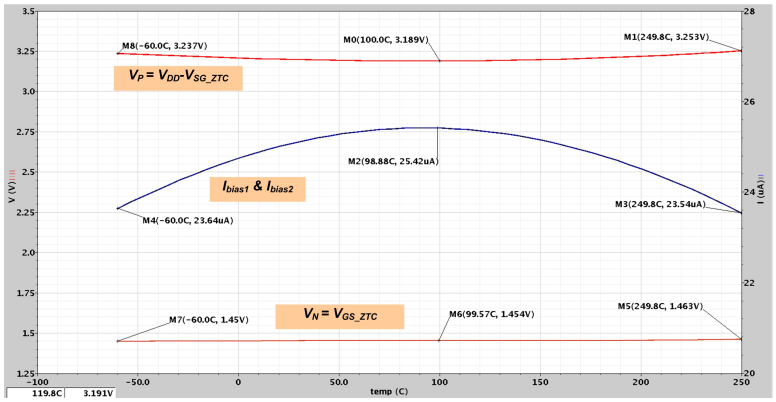


Figure 3.11: DC simulation results of the temperature independent bias network.

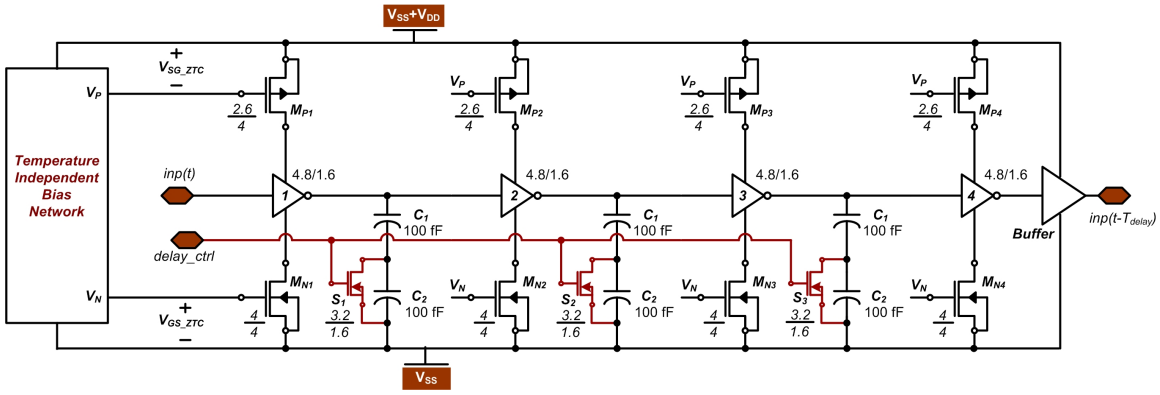


Figure 3.12: Schematic of the temperature independent delay generator circuit.

which the on-chip bootstrap capacitor will not be able to supply. Hence, rising and falling edges of this inp_H signal are generated by the edge detector circuit, and level shifter circuit is used to translate these low level signals into high voltage level signals. Duration of these pulses is kept at 20 ns to minimize the charge extraction from the bootstrap capacitor.

The schematic of the edge detector circuit is illustrated in Figure 3.13. The conceptual signals associated with the circuit block are presented in Figure 3.14. *SET* and *RESET* pulses are forwarded to the level shifter circuit for generating the level shifted copy of the inp_H signal through a SR latch.

Table 3.2: Dead-times at different temperatures for two different settings of *delay_ctrl* selection signal.

delay_ctrl	C_{eq}	−60 °C	100 °C	175 °C	250 °C
"High"	100 fF	190 ns	180 ns	180 ns	200 ns
"Low"	50 fF	110 ns	110 ns	110 ns	140 ns

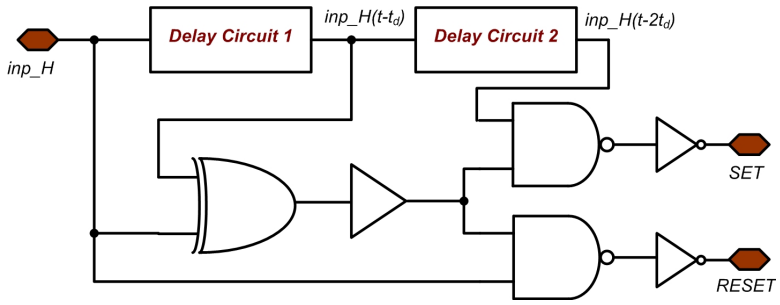


Figure 3.13: Edge detector circuit.

3.4.6 Temperature Independent Level Shifter

The main philosophy of level shifter circuit is to convert the logic level voltage (SET or $RESET$) into current, and then on the high-voltage side convert this current back into a voltage referenced to the high-side voltage. For the all NMOS transistor based half-bridge implemented in this work, the level translation is from (V_{SS} ~V$_{SS}$+V_{DD}) to (V_{OP} ~V$_{OP}$+V_B). The M_H transistor's source is connected to the output terminal (V_{OP}). Therefore, its gate voltage needs to be either at V_{OP} (to turn it OFF) or at $V_{OP-PLUS}$=V_{OP}+V_B (to turn it ON). Two constant current bias level shifter circuits are used to generate S and R signals from the SET and $RESET$ signals respectively.

Figure 3.15 shows the level shifter circuit designed for this work. I_{bias3} current in the right most branch creates a voltage drop in R_{31}+R_{32} which works as the active low S or R signal for the SR latch following this circuit. If I_{bias3} varies with temperature, then the magnitude will also vary. If the current is too low, then the voltage might not be able to trigger the latch, and if it is too large, then this voltage drop may exceed the gate-source voltage limit of the MOS devices in the latch circuit. Threfore, it is important to maintain a constant current flow through this branch in response to SET or $RESET$ pulses. This

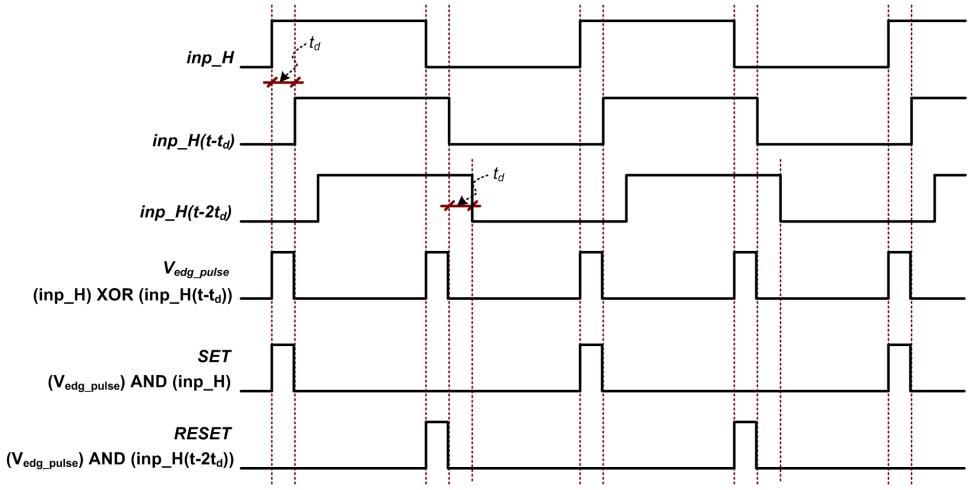


Figure 3.14: Concept of generating SET and $RESET$ pulses from the inp_H signal using edge detector circuit.

constant current bias is guaranteed through the zero temperature co-efficient (ZTC) biasing of the PMOS and NMOS current mirrors as shown in Figure 3.15. Resistors in all three branches are constructed by a combination of +ve and -ve temperature co-efficient resistors to ensure fixed voltage drop across them across the entire temperature range.

This circuit consumes power only when the SET or $RESET$ pulses are applied in the M_{SW} transistor. Duty cycle of these pulses is only 0.04% for 20 kHz logic input signal. Therefore, average power consumption of this circuit is very small. Diodes D_1 to D_3 and MC work as a voltage clamping circuit to protect transient voltage spike across R_{31}+R_{32}. Diode D_F is the free wheeling diode for the voltage clamp circuit.

3.4.7 Input Stage

The input stage of the gate driver circuit receives the logic level control signal from the external source which can be a microcontroller or a DSP board. Logic generating circuits are expected to be placed in a relatively cooler space which send the control signal to the gate driver through long wire connection to the power module. Often these signals are corrupted by noise. To remove this noise, a Schmitt trigger buffer is used in the front end of the driver circuit.

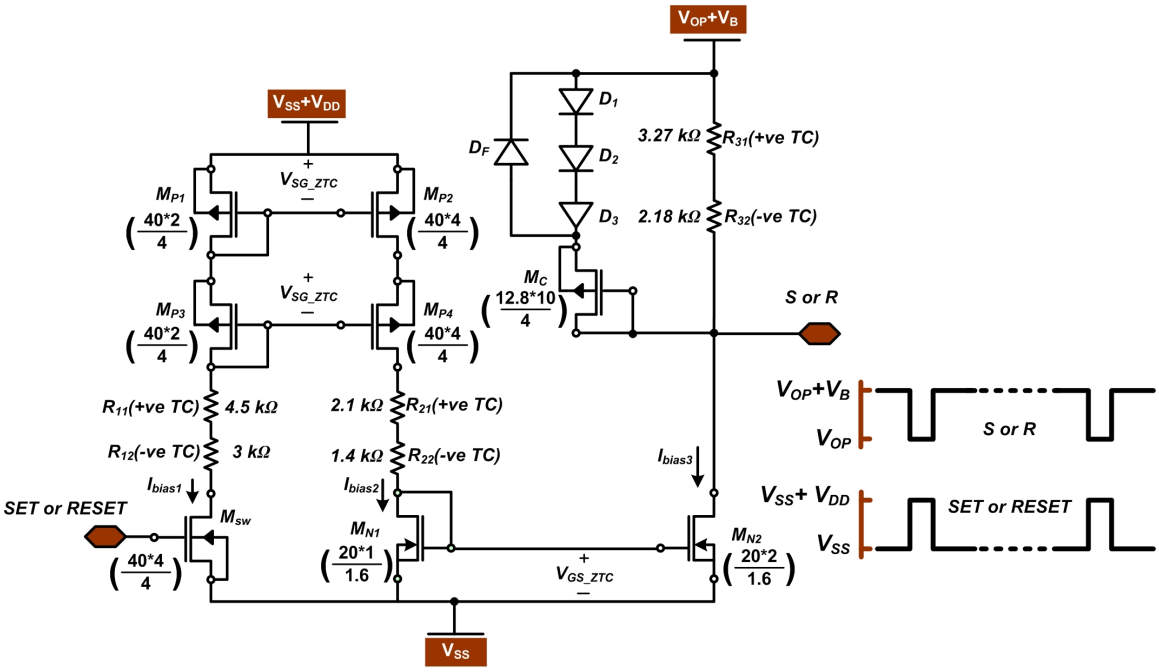


Figure 3.15: Schematic of the constant current bias level shifter circuit.

Schmitt trigger buffer

Schmitt trigger circuits are commonly used in the front end of a circuit to generate clean pulses from a noisy input signal. The schematic of the Schmitt trigger buffer used in this circuit is presented in Figure 3.16. M_{n1}, M_{n2}, M_{n3}, M_{p1}, M_{p2}, and M_{p3} form the basic inverting Schmitt trigger. Aspect ratios of these transistors set the lower and upper threshold, i.e. hysteresis of the circuit. For the sizes shown in Figure 3.16, hysteresis obtained for this circuit is almost 2.5 V across the desired temperature range. Figure 3.17 reveals the input and output of the Schmitt trigger at 250 °C. For the positive going input signal, output changes states only when the input voltage exceeds upper threshold voltage, V_{thH} (3.68 V). Output remains low as long as the input is higher than the lower threshold voltage, V_{thL} (1.23 V). Inverting Schmitt trigger is followed by an inverter stage to generate the in phase logic signal (V_{inp_intrl}) for the following stages in the gate driver circuit.

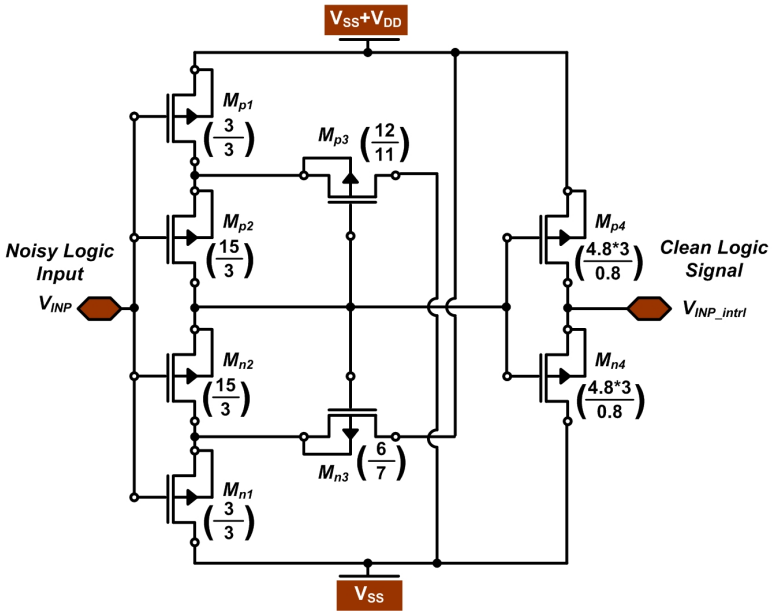


Figure 3.16: Schematic of the Schmitt trigger buffer in the input stage.

Sensor' Signal Processing

Different protective circuit blocks are also added to this gate driver circuit. Feedback signals from temperature sensor, under-voltage lock out (UVLO) detection circuit, and short circuit detection unit are supplied to the three-input NOR gate placed in the front end of the driver circuit. If any of these feedback signals become HIGH, indicating a fault condition, then the output of the NOR gate will be set to LOW. Output of the NOR gate acts as an active HIGH enable signal for the gate driver logic units following the Schmitt trigger buffer. If the *Enable* signal becomes LOW, the actual input received by the dead-time controller circuit becomes zero, and the gate driver generates a LOW gate drive signal to turn OFF the power switch. For HIGH *Enable* signal, noise free input signal (V_{inp_intrl}) from the Schmitt trigger buffer is passed to the dead-time controller circuit.

An ultra low power on-chip temperature sensor circuit capable of working at temperature higher than 200 °C has also been designed as part of this dissertation work which is presented in Chapter 4.

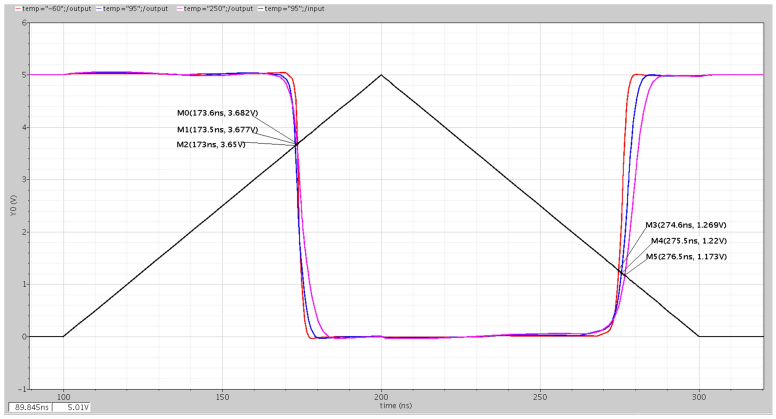


Figure 3.17: Schmitt trigger circuit's input and output signals at different temperatures (red: $-60\,^{\circ}$C, blue: $95\,^{\circ}$C, and pink: $250\,^{\circ}$C).

3.5 Simulation Results

Simulation results of the proposed gate driver circuit at $-60\,^{\circ}$C, $95\,^{\circ}$C, and $250\,^{\circ}$C are presented in Figure 3.18. These results confirm the complementary turn ON and OFF operations of the high-voltage n-channel MOSFETs in the half-bridge output stage. The top graph in Figure 3.18 shows the gate drive source current provided by the M_H transistor while sinking current through the M_L is zero. The bottom graph in Figure 3.18 shows the sinking current through the M_L transistor and zero sourcing current from the M_H transistor. According to this simulation, this proposed gate driver circuit is capable of sourcing and sinking 5 A peak current even at $200\,^{\circ}$C with $2\,\Omega$ gate current limiting resistor (R_G). The Monte Carlo (MC) simulation results for 100 runs with process and mismatch variations and R_G value of $3.4\,\Omega$ are illustrated in Figure 3.19. Both sourcing and sinking current peaks at $27\,^{\circ}$C and $200\,^{\circ}$C are plotted in this figure. MC simulation confirms the robust performance of this proposed gate driver circuit against process variations and device mismatches across a wide temperature range.

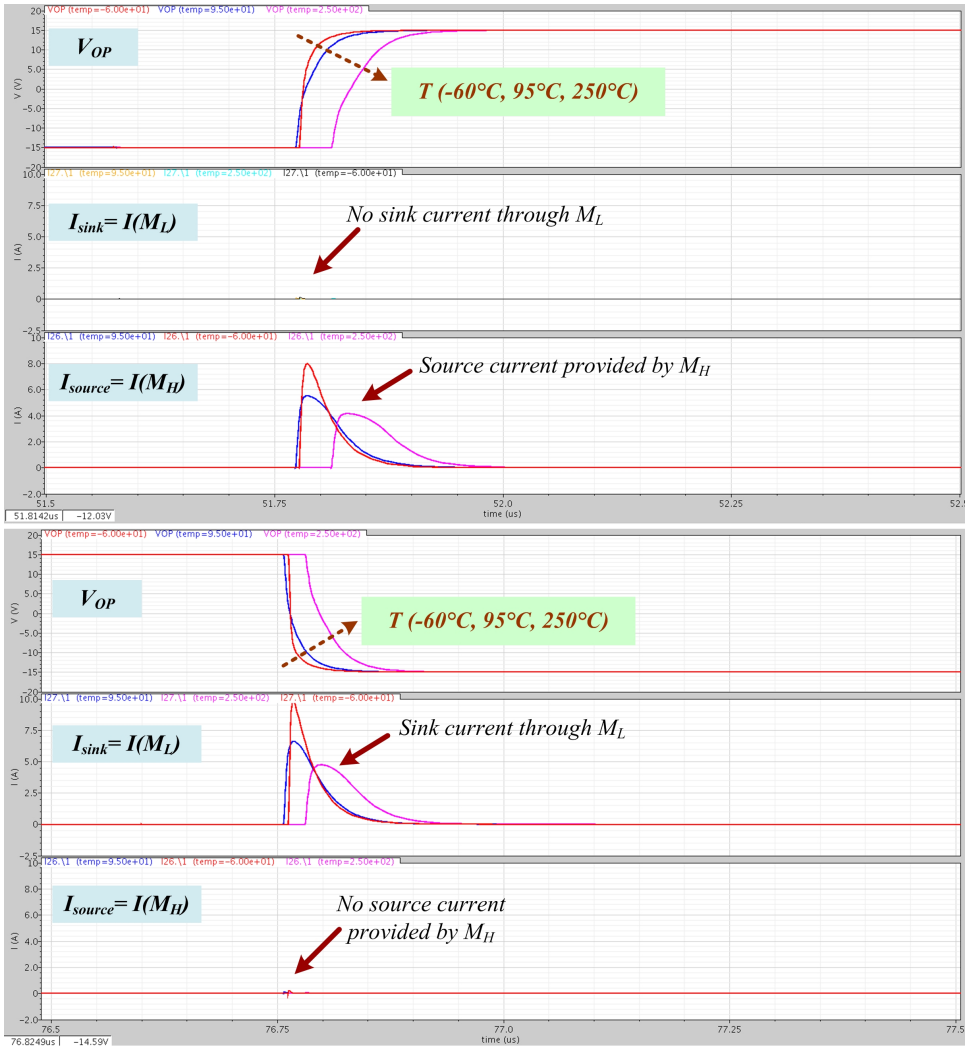


Figure 3.18: Gate driver circuit's simulation results at different temperatures (red: $-60\,^{\circ}$C, blue: $95\,^{\circ}$C, and pink: $250\,^{\circ}$C.

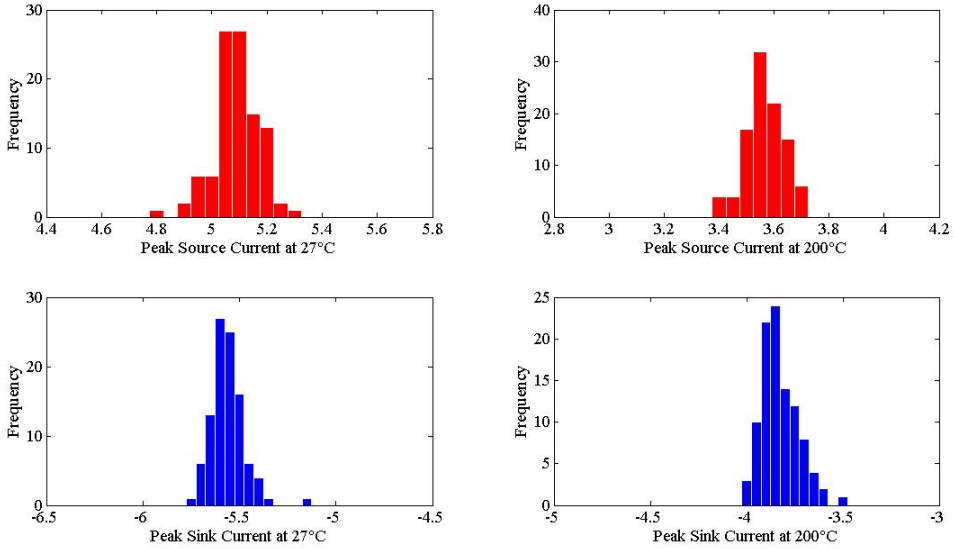


Figure 3.19: Gate driver circuit's Monte Carlo simulation results at different temperatures with R_G=3.4 Ω nominal (100 runs with both process variation and device mismatches).

Chapter 4

On-chip Ultra Low Power Temperature Sensor Circuit for High-Temperature Applications

In recent years silicon-on-insulator (SOI) based high temperature circuits have gained popularity in extreme environment applications like automotive, geo-thermal exploration, well-logging, aircrafts, and space exploration. Often these circuits are designed for operation at or above 200 °C ambient temperature. For safety of these circuits, mechanism to detect die temperature in excess of allowed upper limit needs to be integrated along with the actual circuit. A new ultra low power temperature sensor circuit has been designed to protect the high-temperature gate driver circuit proposed in Chapter 3. This sensor circuit has also been designed in 0.8–micron, 2–poly, 3–metal SOI process. This scheme utilizes the exponential increase in the diode leakage current with the increase of temperature to determine whether the die temperature has exceeded the maximum allowed temperature. If it does, then this circuit sends a feedback signal to the input of the gate driver circuit to shut down the power switch driven by the gate driver circuit. The fault signal is automatically removed only when the die temperature cools down below a pre-defined level lower than the upper limit which activates the fault signal. Main advantage of this circuit is its extremely low power consumption in the normal operating temperature range ($\leq 200\,^{\circ}\mathrm{C}$).

4.1 Literature Survey on Existing Temperature Sensor Circuits

One of the most popular methods to realize on-chip temperature sensor uses the difference between the base-emitter voltages of two substrate PNP transistors (thermal diode) of the same size, which are forward biased by two different currents usually in the range of hundreds of micro amps [59–62]. Figure 4.1 shows the basic sensing circuit of this type. Main drawback of this approach is the continuous power loss even when the die temperature is in the normal operating range. Some researchers have utilized time-to-digital-converter, or a ring-oscillator to realize the temperature sensor [63]. This approach requires large chip area and consumes excessive power at required sampling rate. All these approaches are also restricted to limited operating temperature range ($\leq 130\,^{\circ}\mathrm{C}$).

4.2 Proposed Temperature Sensor Circuit

For the safety of the gate driver circuit, a simple temperature sensor circuit is needed to monitor the die temperature up to $250\,^{\circ}\mathrm{C}$. Figure 4.2 illustrates the schematic of the proposed circuit. The core temperature sensing part of this circuit is the reverse biased diode, *Dsense*. Several (M number) p-n junction diodes are connected in parallel to increase the total leakage current which depends on the die temperature. Figure 4.3 shows the measured and simulated single diode leakage currents. For the same values of measured and simulated leakage currents there exists a $20\,^{\circ}\mathrm{C}$ offset. This was taken into consideration to set the maximum allowed die temperature. Diode leakage current, which is in the nano-ampere range, is first multiplied by the PMOS current mirror with 1:30 ratio and then converted to a voltage signal by the resistor R_L. Voltage drop across the resistor R_L is applied to the input of a Schmitt trigger which is buffered with the single-stage inverter circuit to drive the output node. With the increases in the die temperature, voltage drop across R_L goes high, and once it exceeds the low-to-high threshold voltage of the Schmitt trigger, V_{out} shifts to logic HIGH (V_{DD}) indicating a fault condition. This is used to shut down the gate driver circuitry that this sensor is protecting. To ensure the true removal of the factors triggering the excessive die temperature, the high-to-low threshold voltage

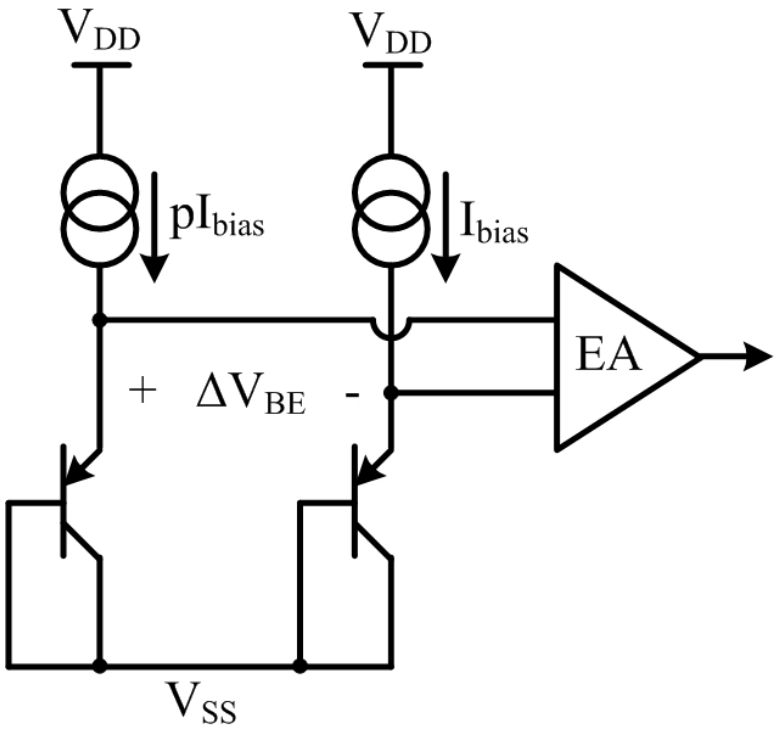


Figure 4.1: Conventional on-chip temperature sensing scheme.

of the Schmitt trigger is set at a lower value corresponding to 15 °C reduction in the die temperature. This hysteresis will prevent the circuit to be turned ON by temporary recovery of the fault condition.

Figure 4.4 presents the sensor output signal, V_{out}, with the increase in die temperature for two different settings of the number of reverse biased diodes in the circuit (M=20 and M=5). 20 diodes in parallel set the fault triggering temperature at 230 °C, whereas 5 diodes set it at 263 °C. Figure 4.4 also shows the logic HIGH to logic LOW transition for V_{out} when the die temperature goes down. By proper sizing of the devices in the Schmitt trigger, 15 °C hysteresis was provided in the sensor circuit.

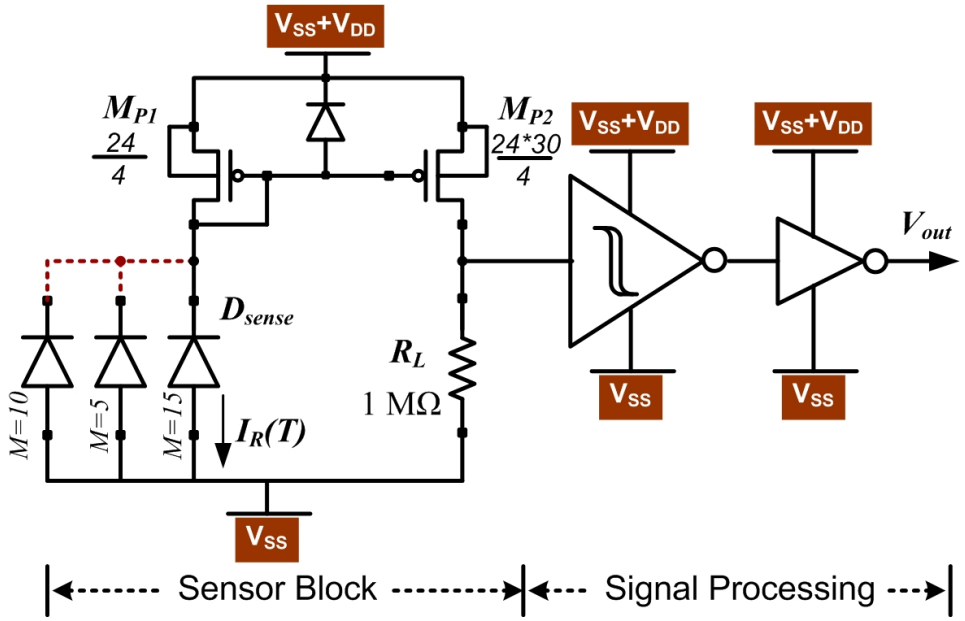


Figure 4.2: Proposed diode leakage current based low-power temperature sensor circuit.

4.3 Monte Carlo Simulation of the Temperature Sensor Circuit

Monte Carlo simulation of the proposed temperature sensor circuit (with M=30), including process variations and device mismatches are performed for both rise and fall of the temperature. Figure 4.5(a) presents the simulation results for 100 runs when the simulation temperature was increased from 190 °C to 230 °C. This circuit generates a feedback signal at around 220 °C temperature with a spread of ±5 °C due to the process variation and device mismatches. Figure 4.5(b) shows similar simulation result except the simulation temperature was decreased from 230 °C to 190 °C. Sensor circuit removes the fault indicating feedback signal at around 206 °C with a spread of ±3 °C. A hysteresis of 14 °C was inserted by the proper sizing of transistors in the Schmitt trigger circuit.

4.4 Power Consumption of the Circuit

Power consumptions of the sensor circuit for different number of diodes connected in parallel to build *Dsense* are shown in Figure 4.6. From this figure it is evident that this sensor

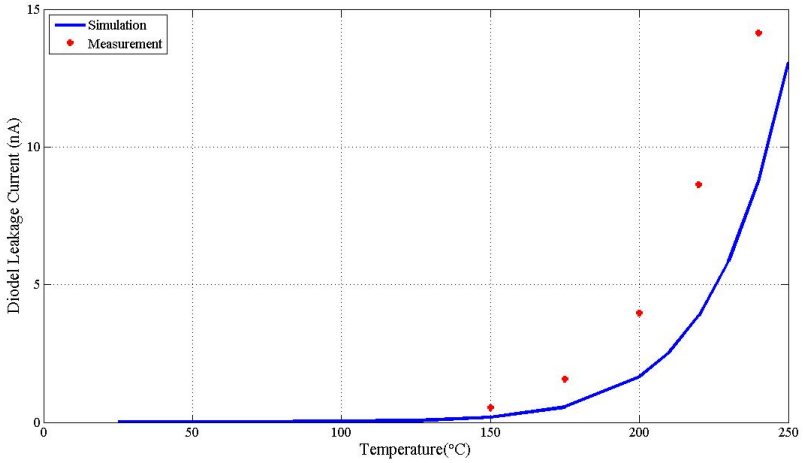


Figure 4.3: Measured and simulated diode leakage current.

circuit consumes very little power in the desired temperature range ($\leq 200\,^{\circ}\mathrm{C}$). At $150\,^{\circ}\mathrm{C}$ total power consumption is only $0.6\,\mu\mathrm{W}$ which goes to $9.63\,\mu\mathrm{W}$ at $200\,^{\circ}\mathrm{C}$ for $M = 25$. The inset graph in Figure 4.6 reveals the power consumption of the circuit including the fault activating temperatures. The spike in the power consumption is due to the logic level transition of Schmitt trigger's output node. External control of the target upper limit of the die temperature can be provided by keeping provision to change the number of diodes connected in parallel to construct *Dsense*, which generates the temperature sensitive leakage current.

Table 4.1 makes a comparison of this scheme with other temperature sensors reported in literature in terms of power consumption and maximum temperature range. In terms of power consumption, the performance of this circuit is much better than other approaches presented in Table 4.1. This circuit's negligible power consumption up to $200\,^{\circ}\mathrm{C}$ is very significant for its inclusion in the circuits designed for high-temperature operations.

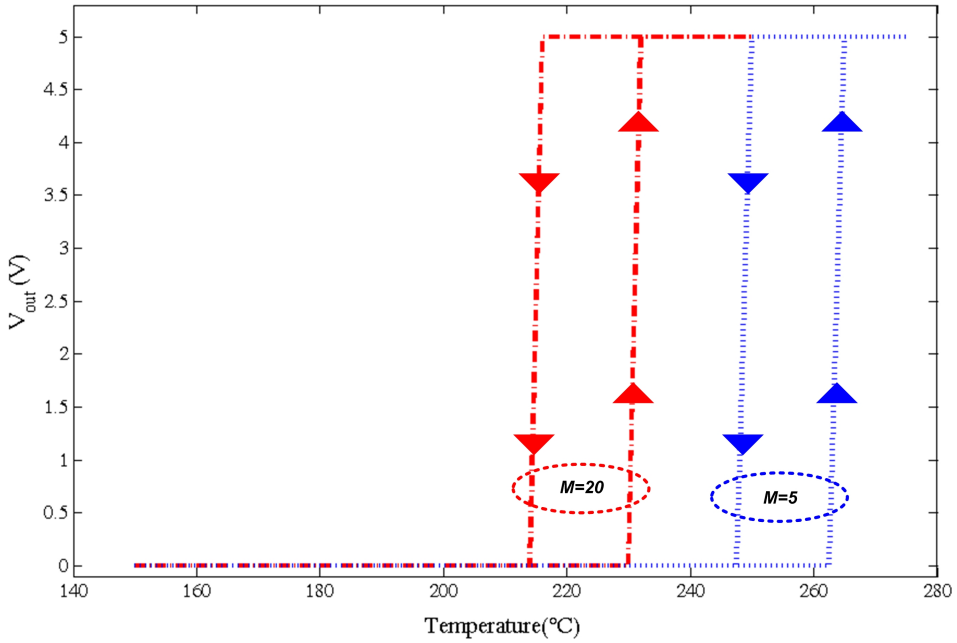
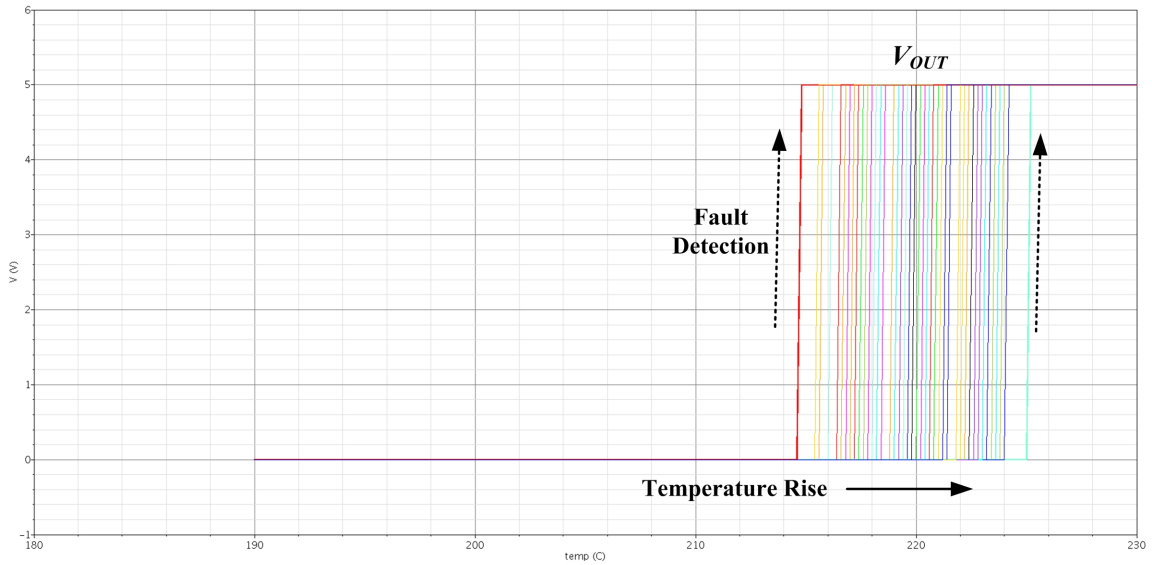


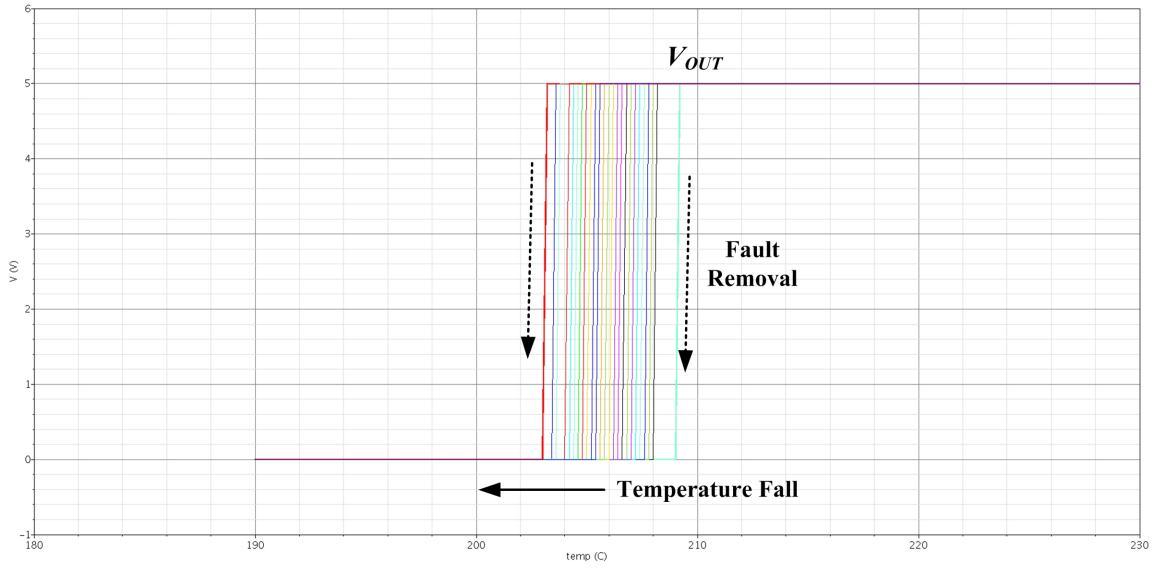
Figure 4.4: Sensor circuit's output (V_{out}) with the increase and decrease of die temperature (M is the number of diodes connected in parallel in D_{sense}).

Table 4.1: Comparison of the proposed ultra low power temperature sensor with other published temperature sensor circuits.

Reference	Sensing Parameter	Maximum Temp. (°C)	Die Area (mm^2)	Power Consumption (μW)
[59]	V_T	100	$0.003 \sim 0.02$	$100 \sim 200$
[60]	ΔV_{BE}	130	–	0.49
[62]	ΔV_{BE}	125	0.245	1
[61]	ΔV_{BE}	125	2.5	429
[63]	Temp.-to-pulse	100	0.175	10
[64]	V_T	125	0.05	25
This work	Diode Leakage Current	250	0.1	0.6 at 150 °C 9.5 at 200 °C



(a)



(b)

Figure 4.5: Monte Carlo simulation of the sensor circuit for temperature rise (M=30).

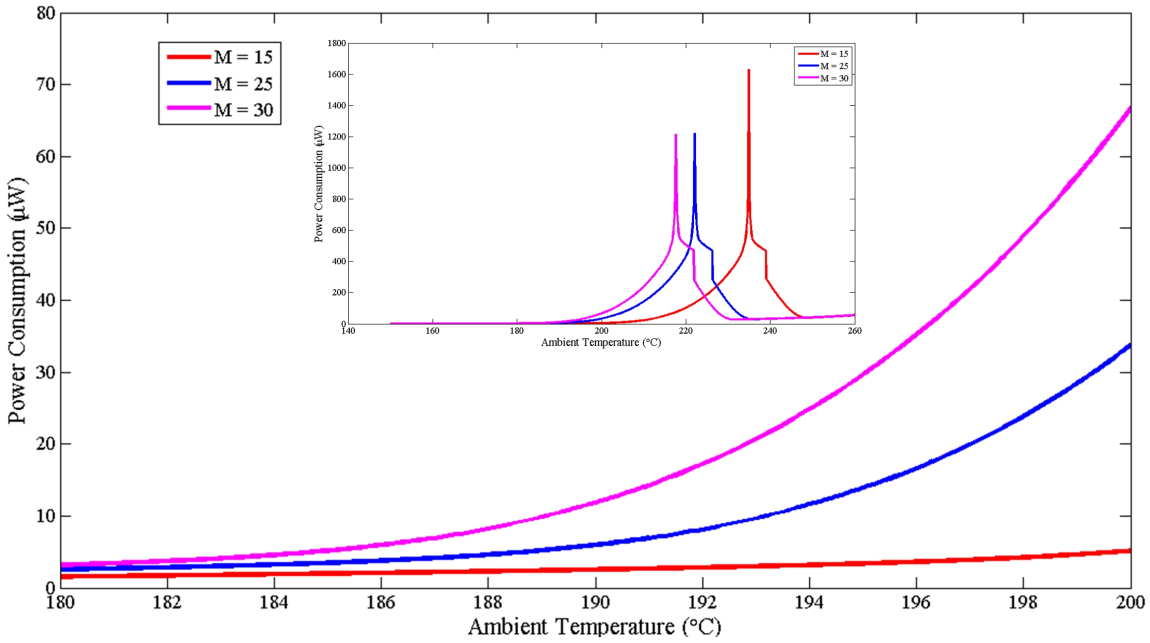


Figure 4.6: Power consumption in the proposed low-power temperature sensor circuit.

Chapter 5

Prototype Implementation, Test setup, and Measurement Results

5.1 Fabricated Chip and the Test Board

The proposed high-temperature gate driver circuit was implemented in 0.8–micron, 2–poly, 3–metal bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (SOI) process . The chip includes core gate driver circuit, low-power temperature sensor circuit, and on-chip current limiting resistor (R_G) array. Figure 5.1 shows the micro-photograph of the fabricated chip. Core gate driver circuit consumes an area of about $10\,\text{mm}^2$ ($5\,\text{mm} \times 2\,\text{mm}$). Most of the chip area is occupied by the half-bridge output stage and the on-chip 1.5 nF bootstrap capacitor. Bonding pads with ESD protection features also took significant die area. Temperature sensor circuit consumes only $0.4\,\text{mm}^2$ chip area. Much wider metal traces compared to what was required were used for those interconnects which carry large currents. Whenever layout rules permissible, third metal layer, which is the top metal layer in this process, was used. This wide metal three traces work as heat pipes and help to transfer some of the heats from the inner metal and device layers to the outside world. Multiple die-pad to package pin connections were used for the power supply and output nodes to minimize the parasitic bond wire inductances.

Figure 5.2 presents the photograph of the packaged chip in comparison with a dime. Ceramic pin-grid-array (PGA) package was used to house the fabricated chip. Ceramic

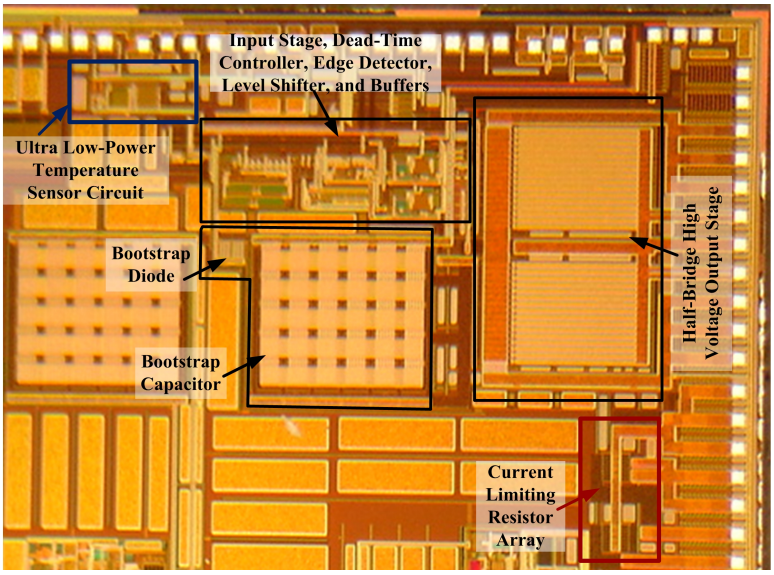


Figure 5.1: Microphotograph of the high-temperature gate driver circuit.

packages are essential for the high-temperature tests of this circuit. Circuits presented in this dissertation occupy less than 40% of the total die area shown in Figure 5.2. Three different versions of on-chip voltage regulator circuits, short-circuit protection, and under voltage lock out circuits are also sharing the same die.

A double-layer printed circuit board (PCB) was designed to mount the chip and the power supply filter networks. Figure 5.3 presents one of the test boards which was used for testing the gate driver chip. These test boards are fabricated using Polyimide material, which can withstand temperatures much higher than 200 °C. High melting point (HMP) solder was used to connect all the components to the PCB. All the hook-up wires used in this test board have insulations made of Teflon so that they can safely operate at 200 °C.

Figure 5.4 shows the actual test setup used for testing the prototype gate driver chips. Polyimide test board with the gate driver chip was placed inside the environmental chamber. Chamber temperature was varied to test the gate driver circuit at different ambient temperatures. For both R-C load test and for SiC power switch tests actual load was kept outside the chamber. A 600 V, 16 A DC power supply unit was used for the SiC power switch tests.

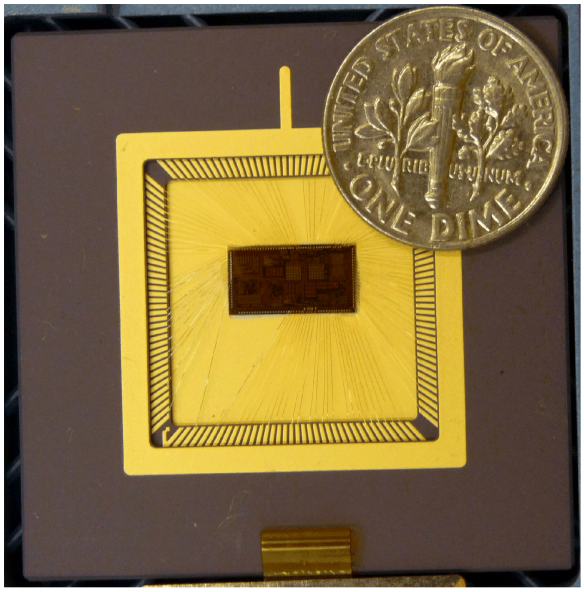


Figure 5.2: Photograph of the packaged gate driver chip.

5.2 Measurement Results

5.2.1 R-C Load Test Results

The chip was first tested with the on-chip current limiting resistor R_G connected in series with an external 10 nF capacitive load at different ambient temperatures by placing the test board inside a temperature chamber. Schematic of the test configuration is shown in Figure 5.5. Figure 5.6 reveals the 30 V peak-to-peak (15 V to +15 V), 20 kHz gate pulse signal generated by the chip at 200 °C ambient temperature with nominal R_G value of 4.3 Ω. The drive current wave shape is also included in Figure 5.6. At 200 °C, the peak sourcing and sinking currents were 2.5 A and 2.2 A, respectively.

Switching frequency was varied from 1 kHz to 100 kHz at 200 °C. Duty cycle of the incoming logic signal was also varied from 1% to 99% with a switching frequency of 20 kHz. Figure 5.7 shows the duty cycle variation test results at 200 °C. No significant changes in current drive or drive voltage pulses were observed due to the switching frequency or duty cycle variations.

A similar R-C load test was carried out for three different on-chip current limiting resistance (R_G) values. Readings were taken 15 minutes after the temperature of the

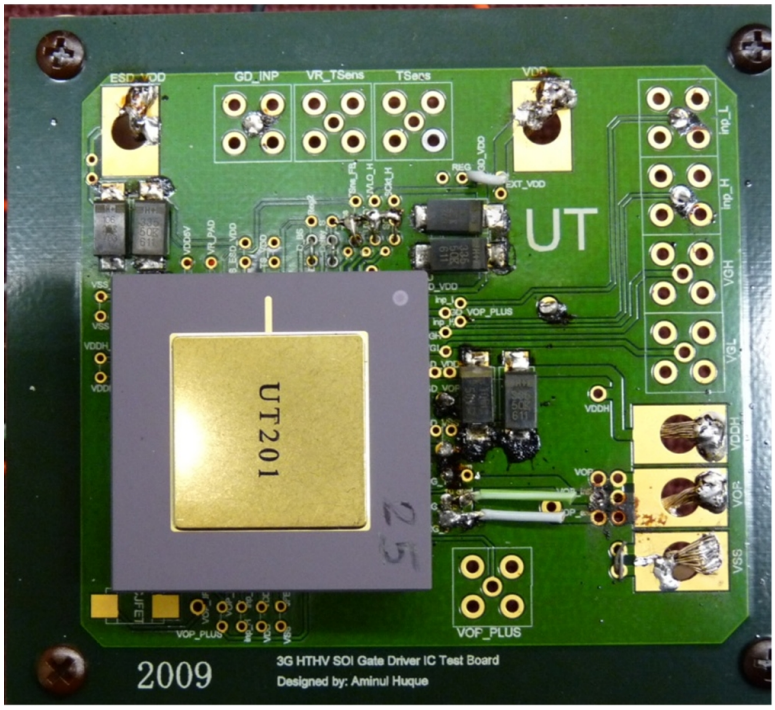


Figure 5.3: High-temperature test board made of polyimide material.

chamber reached the target temperature to ensure that the die temperature was the same as the ambient (inside the oven). Figure 5.8 shows the change in source and sink current peaks with temperature variation for all three R_G values. Figure 5.8 also presents the simulation results for similar load conditions. Table 5.1 presents the actual measured peak source and sink currents for three differen R_G values.

Figure 5.9(a) reveals the variation in on-chip resistances with temperature for all three arrangements of R_G values. All three resistors show linear rise in resistance value with the increase of temperature. The rise in resistance contributes to the decrease in current drive peaks with the increase of ambient temperature, as presented in Figure 5.8. Figure 5.9(b) shows the chip-to-chip variation of $2.5\,\Omega$ (nominal) R_G arrangement for three different chips. Chip-to-chip variation of on-chip resistance across temperature is quite negligible.

Figure 5.10 shows the measured source and sink current peaks at different ambient temperatures for three different ICs with same R-C load ($R_G = 3.4\,\Omega$ and $C = 10\,\text{nF}$). Very small chip-to-chip variations in drive current were observed

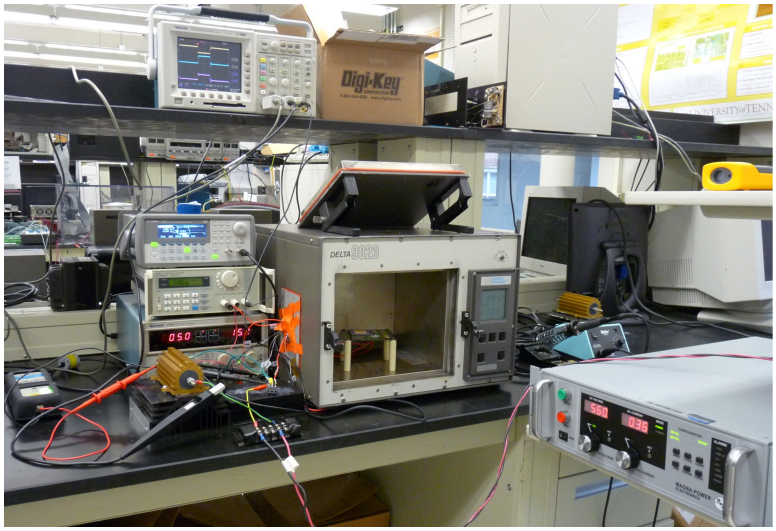


Figure 5.4: High-temperature gate driver test setup.

Table 5.1: Drive current peaks at different ambient temperatures three different on-chip current limiting resistance (R_G) settings.

Peak	Nominal R_G (Ω)	27 °C	85 °C	150 °C	200 °C
I_{source} (A)	11.8	1.7	1.6	1.5	1.45
	6	2.3	2.1	2	1.95
	3.4	2.9	2.7	2.6	2.5
I_{sink} (A)	11.8	1.7	1.6	1.5	1.45
	6	2.3	2.1	2	1.9
	3.4	2.8	2.6	2.3	2.2

5.2.2 Dead-time Controller Circuit Test Results

Figure 5.11 shows the non-overlapping logic outputs (inp_L and inp_H) generated by the temperature independent dead-time controller circuit at 200 °C. These two signals are used to generate the appropriate gate drive signals for the two high-voltage NMOS transistors (M_L and M_H) in the half-bridge output stage. Therefore, maintaining a proper dead-time between these two signals is very critical to ensure non-overlapping turn-ON and turn-OFF operations of the high-voltage NMOS transistors in the half-bridge output stage. Any over lapped ON period will cause a short circuit between the high-voltage rails biasing the gate driver circuit. Figure 5.12 shows the change in dead-time between inp_L and inp_H logic signals due to increase in ambient temperatures

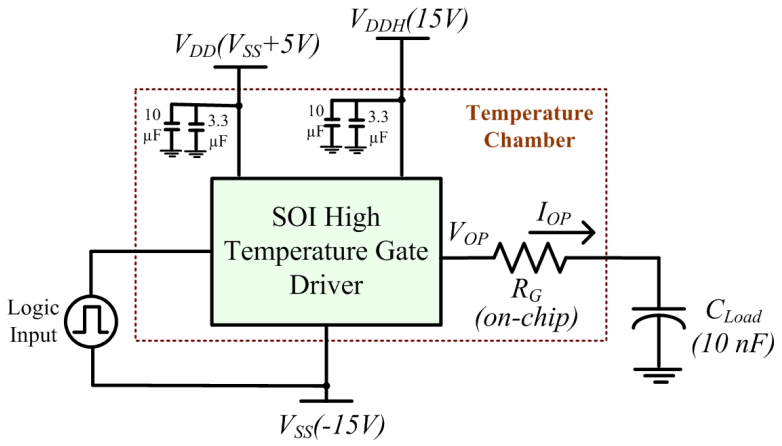


Figure 5.5: Schematic of the R-C load test configuration.

5.2.3 SiC MOSFET Test Results

A SiC power MOSFET (1200 V, 10 A) prototype, developed by Cree was tested with this gate driver chip. An 80 Ω, 250 W load resistor (in series with the drain terminal) was used with the SiC MOSFET in a common-source configuration. Figure 5.13 shows the test connection for the SiC power MOSFET test with the gate driver circuit.

Rail voltage was set at 560 V using a 600 V, 16 A DC source. A 7 A peak load current was passing through the MOSFET when it was turned ON by the gate driver chip. A 20 V peak-to-peak (+15 V to -5 V) drive signal was applied to the gate terminal of the SiC MOSFET through the 3.4 Ω on-chip current limiting resistor. The test board was placed inside the temperature chamber, and the SiC MOSFET was kept outside the chamber as it was not packaged for high temperature applications. Starting from room temperature, the chip was tested up to 200 °C. Switching frequency was set at 20 kHz and the duty cycle was 5%.

Figure 5.14 presents the gate voltage (pink), MOSFET drain terminal voltage (blue), and load current (cyan) waveforms at 200 °C. The temperature of the chamber was raised from room temperature to 200 °C in three steps (27 °C, 125 °C, and 200 °C). The ringing effect observed in the wave shapes was due to the added parasitic inductances of the connecting wires that ran from inside the temperature chamber to the outside. 10% to 90% rise-time and 90% to 10% fall-time for both the gate drive voltage signals and the MOSFET

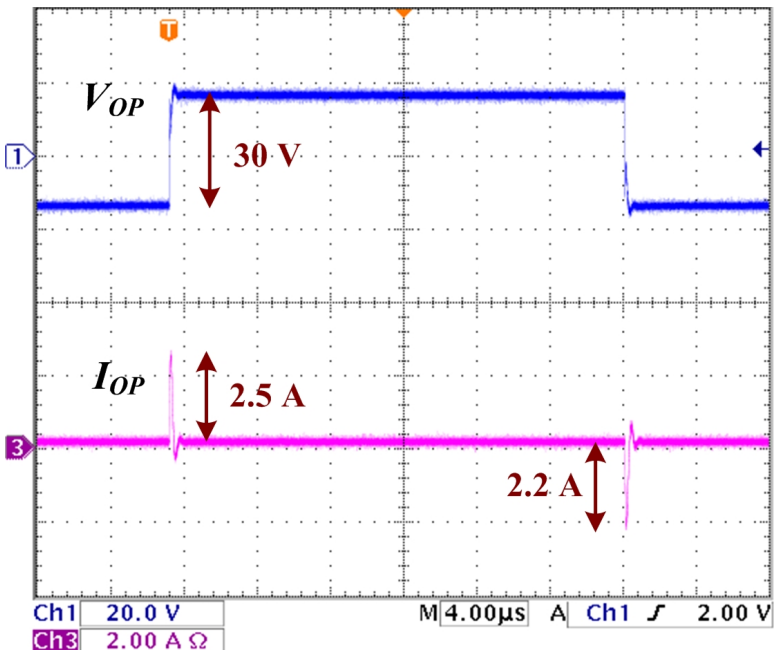


Figure 5.6: R-C load test results at 200 °C with R_G= 4.3 Ω and C_{Load}=10 nF.

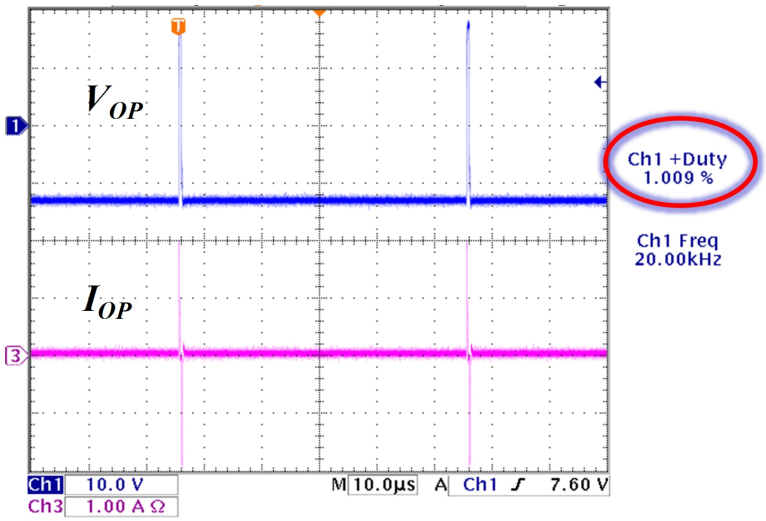
Table 5.2: Rise-time and fall-time at different ambient temperatures.

Ambient temperature	Drain voltage (V_{DS})		Gate voltage (V_{GS})	
(°C)	t_{rise} (ns)	t_{fall} (ns)	t_{rise} (ns)	t_{fall} (ns)
27	15.7	33.4	2.8	3.6
125	15.7	35.1	3.1	4
200	20.2	41.0	4	5.6

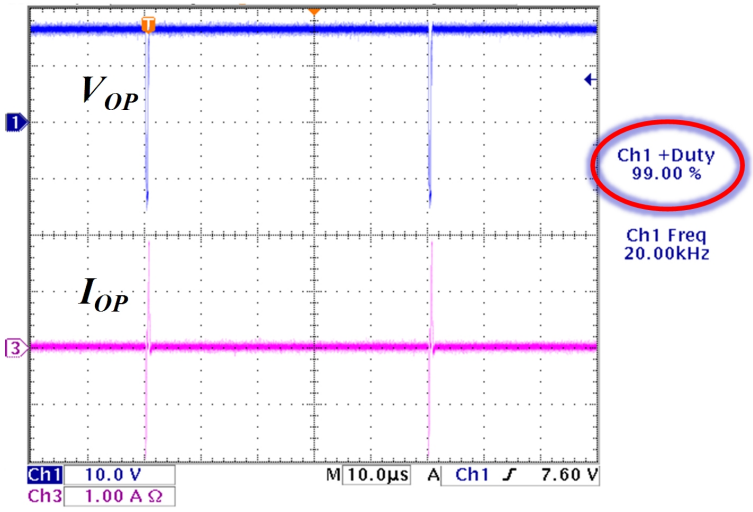
drain voltage at each temperature level are recorded in Table 5.2. These readings show that this high-temperature gate driver circuit maintains a fairly constant driving strength over the entire test temperature range.

5.2.4 SiC JFET Module Tests

The prototype high-temperature gate driver IC was also tested with SiC normally-ON JFET (1200 V, 50 A) power module developed by Microsemi using SemiSouth's normally-ON SiC JFETs. A gate driver circuit was biased to generate an 8 V peak-to-peak (-5 V to 3 V) gate signal to control the JFET module which was connected to a 560 V rail voltage through an 80 Ω load resistor. Figure 5.15 prsents the test result at 200 °C ambient



(a)



(b)

Figure 5.7: Duty cycle variation test results at 200 °C with R–C load (6 Ω and 10 nF): (a) 1% duty cycle and (b) 99% duty cycle.

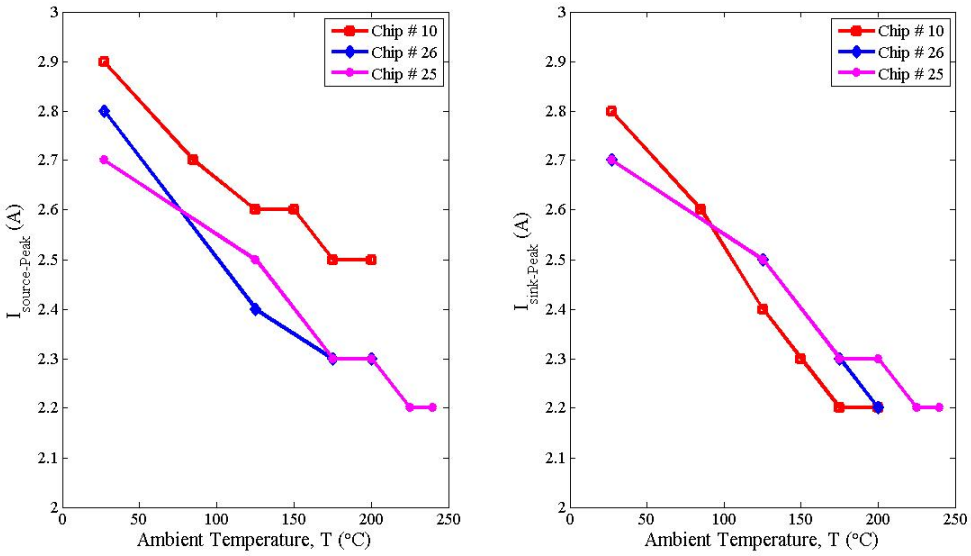


Figure 5.8: R-C load simulation and measured peak drive currents (sourcing and sinking) with three different on-chip current limiting resistances (R_G).

temperature with 1 kHz switching frequency. This test was also performed with 40 kHz switching frequency which is shown in Figure 5.16.

5.3 Measurement Results of the Temperature Sensor Circuit

The newly proposed temperature sensor circuit was tested at wide temperature range with the help of environment chamber used earlier for gate driver circuit measurements. The circuit was properly biased and output (V_{out}) was observed on oscilloscope. In the beginning of the test, at room temperature, V_{out} was set at logic LOW (0 V) level. Temperature of the chamber was then raised until a logic transition from LOW-to-HIGH was observed in the V_{out} signal. The temperature at which this transition took place is the upper limit of the allowed die temperature at which this sensor circuit will send a feedback signal to the input of the gate driver circuit indicating a fault condition. After recording this upper temperature limit, chamber temperature was reduced until a logic HIGH-to-LOW transition was observed in the V_{out} wave shape in the oscilloscope. This HIGH-to-LOW transition took place at much lower temperature than the temperature at which LOW-to-

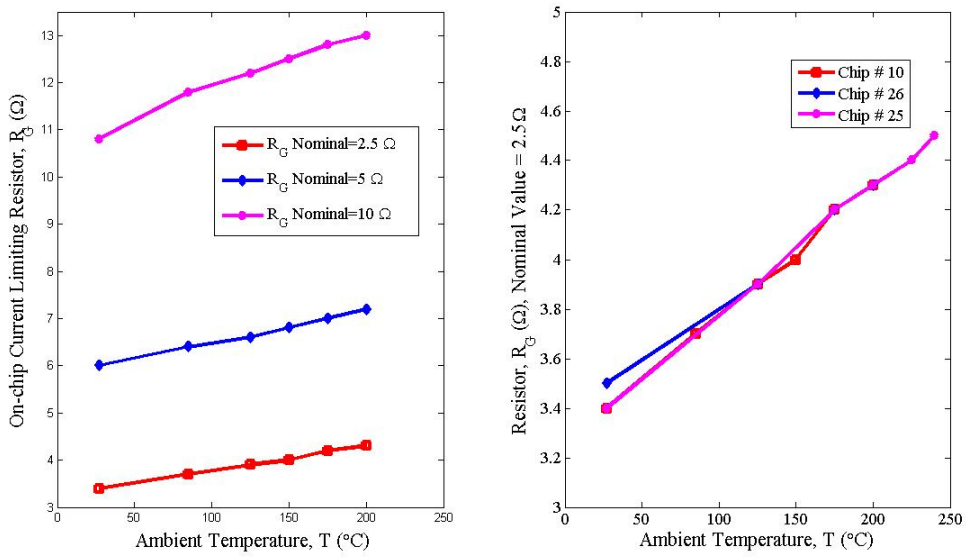


Figure 5.9: Measured variation of R_G with increase in temperature: (a) for three different on-chip R_G values and (b) for three different chips (R_G= 3.4 Ω).

HIGH transition was observed. This temperature differences indicate the built-in hysteresis of the sensor circuit. HIGH-to-LOW transition in V_{out} indicates the removal of the fault condition which was causing the excessive rise in die temperature. Upon receiving this LOW signal from the sensor circuit, the gate driver will resume its normal operation. Hence a built-in hysteresis is very critical to ensure proper removal of the fault situation causing the die temperature rise beyond its normal operating range.

Several temperature rise and temperature drop cycles were carried out to measure the upper and lower triggering temperatures of this sensor circuit. These tests were repeated for three different chips to observe the repeatability of the circuit's performance. Figure 5.17 shows the results of these temperature cycle tests for different chips. The worst case spread in fault triggering temperatures (2.5 °C) was observed for chip#13. Chip#13 also shows the worst case fault removal temperature spread (1.5 °C). All three chips' measured hysteresis were around 25 °C.

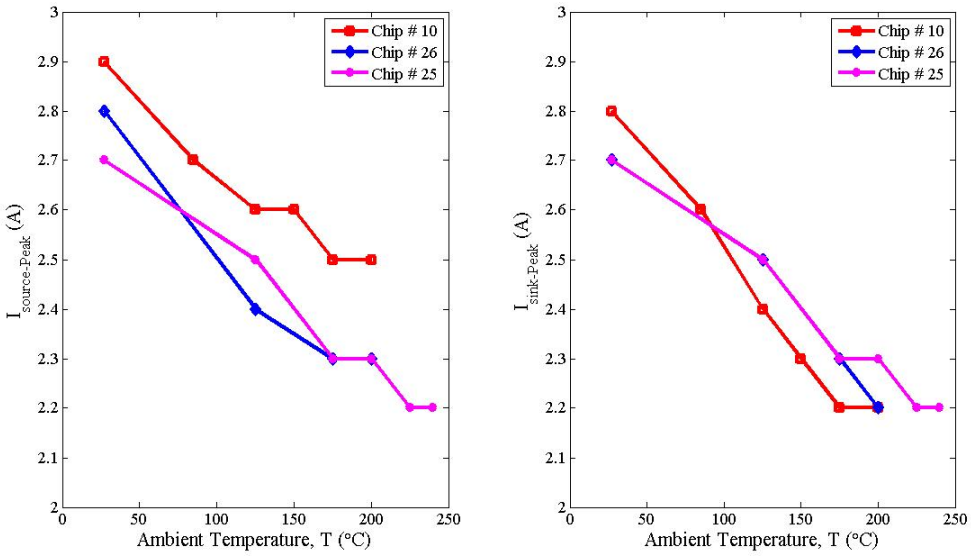


Figure 5.10: Measured source and sink current peaks at different ambient temperatures for three different ICs with same R-C load (R_G= 3.4 Ωand$C$= 10 nF).

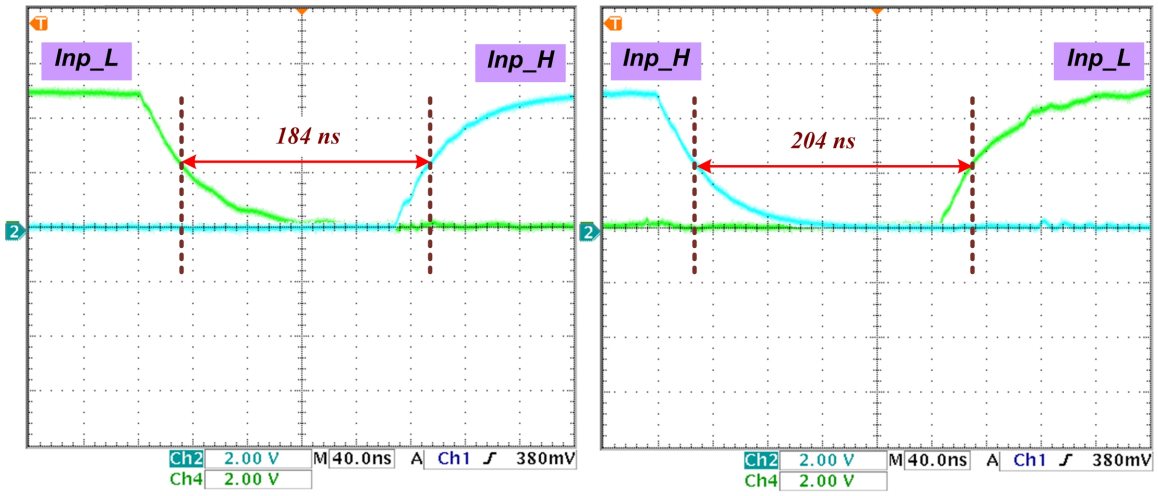


Figure 5.11: Two non-overlapping logic outputs (inp_L and inp_H) generated by the temperature independent dead-time controller circuit at 200 °C).

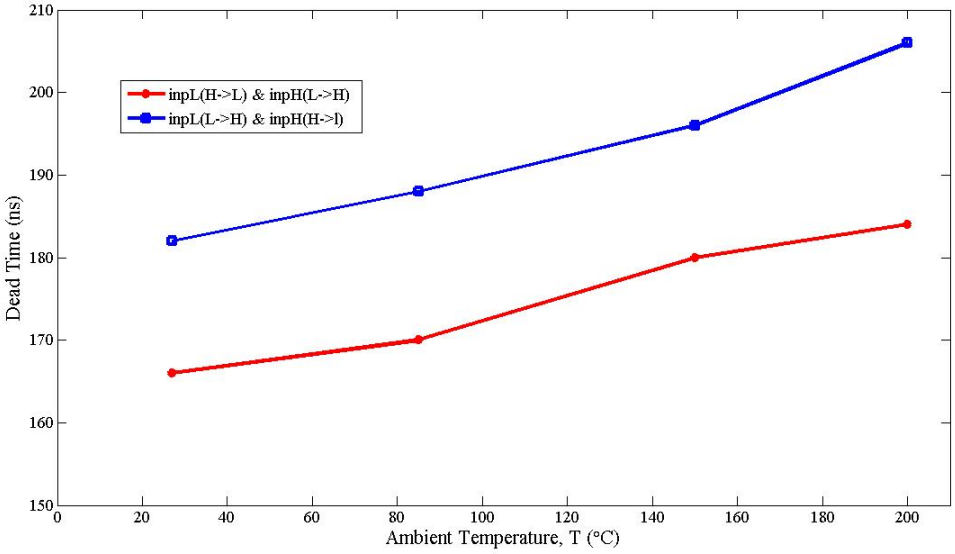


Figure 5.12: Change in dead-time between inp_L and inp_H logic signals due to increase of ambient temperatures).

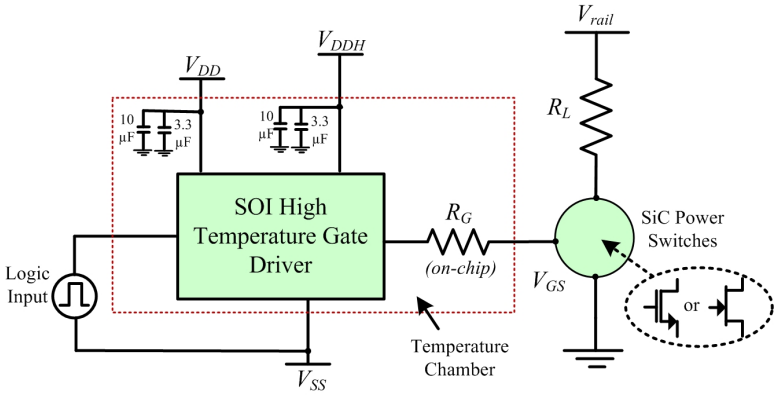


Figure 5.13: Schematic of test setup for MOSFET (V_{DDH}= 15 V, V_{SS}= -5 V) and for normally ON JFET module (V_{DDH}= 3 V, V_{SS}= -5 V). For both tests V_{DD}= 5 V and R_G= 3.4 Ω (on-chip).

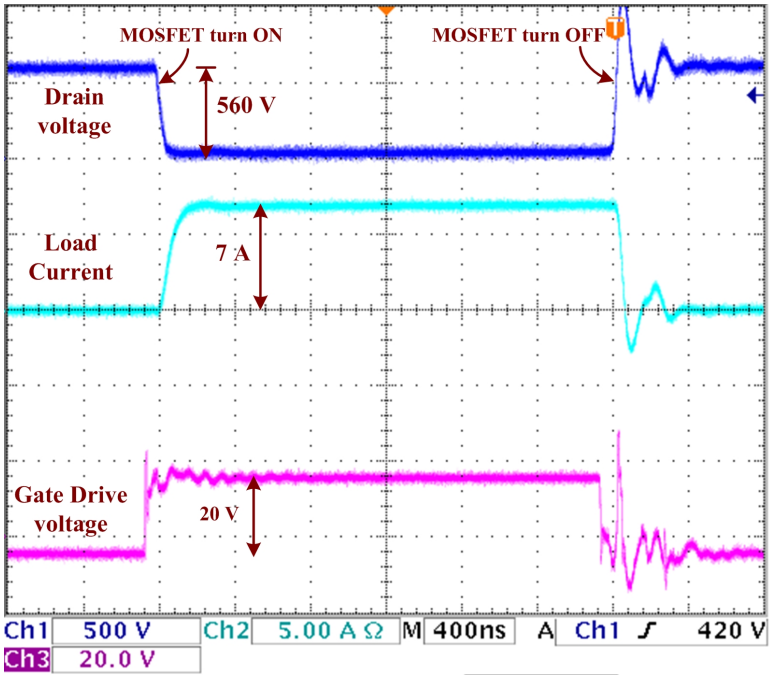


Figure 5.14: Prototype circuit's test results at 200 °C when driving a 1200 V, 10 A SiC MOSFET.

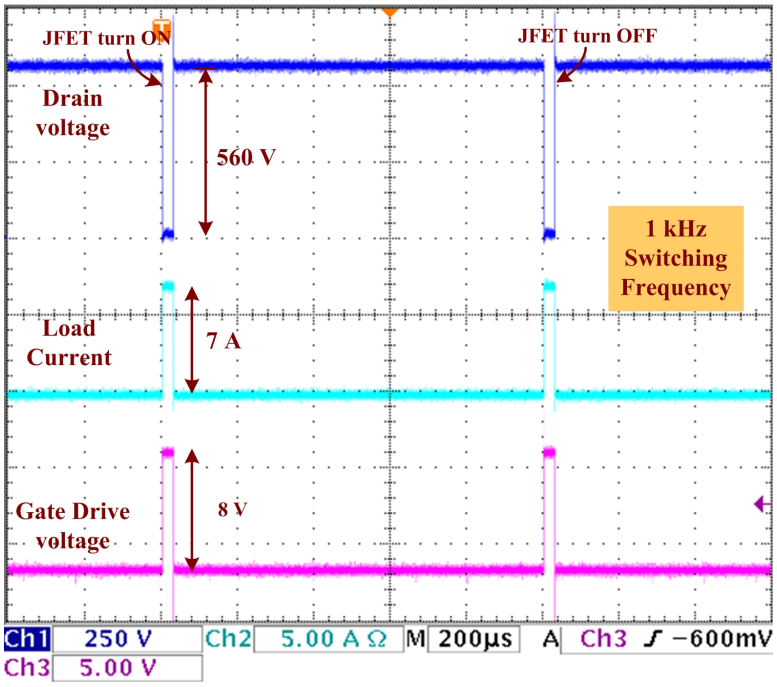


Figure 5.15: SiC normally ON JFET module (1200 V, 50 A) test results at 200 °C and 1 kHz switching frequency.

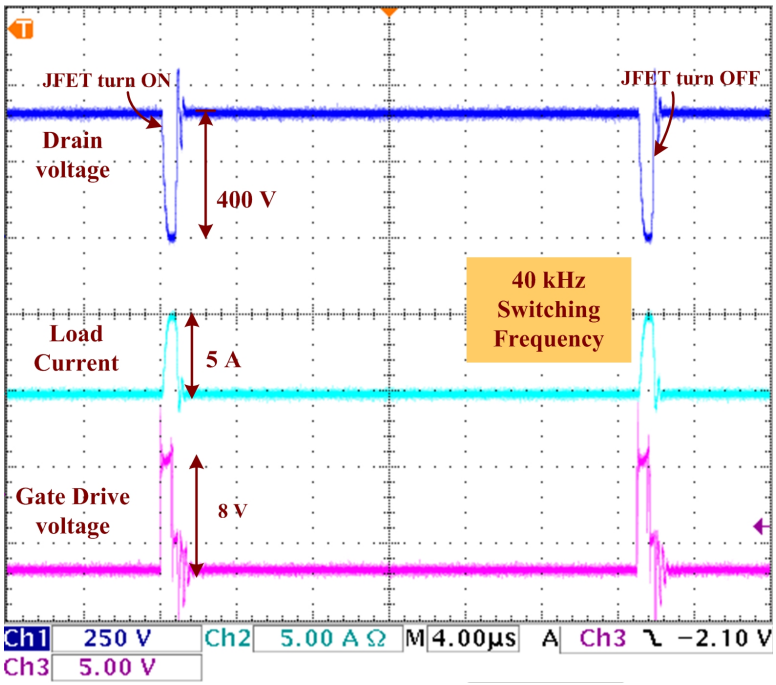


Figure 5.16: SiC normally ON JFET module (1200 V, 50 A) test results at 200 °C and 40 kHz switching frequency.

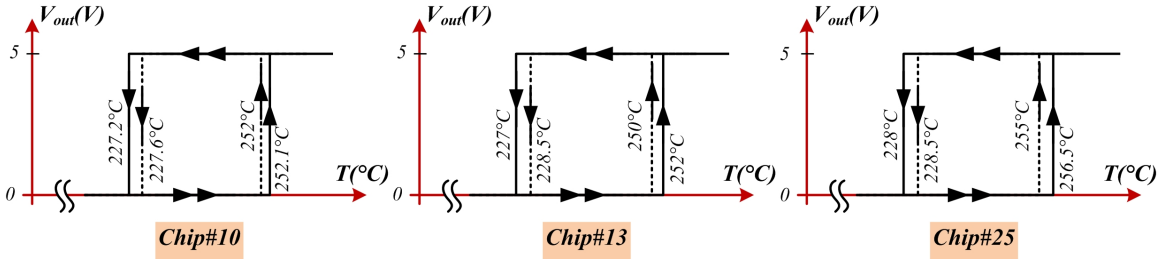


Figure 5.17: Temperature sensor circuit's output in response to several cycles of temperature rise and drop (for M=30).

Chapter 6

Conclusion and Future Work

A high-temperature, high-voltage gate driver circuit with high drive current has been presented. This circuit has been designed and fabricated using 0.8–micron bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (SOI) process. Prototype driver circuit has been successfully tested at ambient temperatures higher than 200 °C without any heat sink and cooling mechanism. Peak drive current of 3 A was measured at room temperature with on-chip current limiting resistance (R_G) of 3.4 Ω (nominal). This driver circuit has successfully driven prototype SiC power MOSFETs and SiC power JFET module. Zero temperature coefficient (ZTC) bias point based biasing scheme is used to design temperature independent dead-time controller and the low-voltage to high-voltage level shifter circuit. No static power was consumed by any of the functional blocks, except the dead-time controller, constituting this high-temperature gate driver circuit. Hence almost no heat was generated inside the chip which is very important for its high ambient temperature operations.

A low-power on-chip temperature sensor circuit has also been incorporated with the gate driver circuit to safeguard it against the excessive die temperature due to any fault condition. This new approach utilizes the exponential rise of p-n junction diode's reverse current with the increase of temperature to detect the die temperature. The unique feature of this proposed topology is its extremely low power consumption up to 200 °C. Up to 200 °C, the power consumption of the sensor circuit can be lower than 10 μW. This temperature sensor circuit has also been fabricated using the same SOI process. This circuit has built-in hysteresis between the fault triggering and fault removal temperatures which

ensures proper recovery of the fault condition before turning ON the gate driver circuit.

6.1 Design Features and Specifications

- Wide operating temperature range −50 °C to 250 °C
- Gate drive voltage range from 10 V to 30 V
- Current drive: 3 A at room temperature with 3.4 Ω R_G
- High capacitive load drive capability: 10 nF in <10 ns at 200 °C
- Switching frequency: 40 kHz
- On-chip bootstrap diode and capacitor based charge pump
- Temperature independent internal dead time controller
- Schmitt trigger input stage for noise immunity
- Ultra low power temperature sensor circuit capable to detect temperature above 250 °C.

6.2 Original Contributions

1. First high-temperature (200 °C), high-voltage (30 V) gate driver integrated circuit with high drive current (4 A at 200 °C, simulation and 2.5 A at 200 °C, measured with $R_G = 3.4\,\Omega$, nominal)
2. Universal gate driver IC capable of driving both SiC MOSFET and JFET power switches.
3. On-chip bootstrap diode and capacitor based charge pump circuit
4. Temperature stable (−60 °C to 250 °C) dead-time controller circuit to prevent "crow-bar current" through the high-voltage half-bridge output stage
5. Temperature independent delay circuit block

6. Temperature stable constant current bias level shifter circuit

7. Ultra low-power on-chip temperature sensor circuit for operation over 250 °C ambient temperatures

6.3 Recommendations for Future Improvement

Significant differences were observed between the measured and simulated performances of the gate driver circuit. One major challenge of any high-temperature design is to obtain reliable device models for wide temperature range. The models, provided for this commercial SOI process, are valid up to 175 °C. Accuracy of these models needs to be verified against actual measurements of the discrete devices. An additional chip comprising the main devices available in this process has also been designed and fabricated along with the gate driver circuit for this model verification purpose. Measurement results can also be used to further extend the model temperature range.

Current drive strength of this gate driver circuit can be further increased to drive larger power modules seeking more gate drive currents. Galvanic isolation between the power circuit and logic generating low-power modules is also important. Incorporating this isolation in the gate driver circuit will further improve the robustness of the power modules. At present time either optical isolation through opto-couplers or transformers are used for this isolation purpose. None of these two techniques are readily available for high-temperature on-chip implementation. Significant research effort will be needed to find an isolation technique applicable for high-temperature operations.

Power switch gate charging and discharging current monitoring based self-diagnosis scheme proposed in [53] can be incorporated with the future version of this high-temperature gate driver circuit. Typically die temperature of the power modules are significantly higher than the ambient temperature. Over temperature protection for power modules can be provided by the gate driver circuit by utilizing the thermistor, which is usually incorporated in the high power modules. To avoid high di/dt through the inductances during the turn OFF operation, soft turn OFF of the power switch is needed. This can be achieved through step-by-step reduction of the gate drive voltage.

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Vita

Mohammad Aminul Huque was born in Dhaka, Bangladesh in 1977. He received his Bachelor of Science degree in Electrical and Electronics Engineering from the Bangladesh University of Engineering and Technology (BUET) and Masters of Science degree in Communications and Signal Processing from the Imperial College London, London, United Kingdom in 2001 and 2003 respectively. He was awarded a Commonwealth scholarship to pursue his studies in London. Mohammad enrolled in the Ph.D. program at the University of Tennessee in January 2006. His research focuses on silicon-on-insulator based high-temperature integrated circuit design for extreme environment power electronics applications. He has also worked on a variety of projects that includes high-temperature GaN HEMT device characterization and modeling and low-power sensor electronics development. As a graduate student Mohammad has published one book chapter, four journal papers, and thirteen conference papers. He received Chancellor's award for Extraordinary Professional Promise from the University of Tennessee in 2009.