A Low Power Mid-Rail Dual Slope Analog-To-Digital Converter for Biomedical Instrumentation

A Thesis Presented for the
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Dallas Wayne Hamlin
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ABSTRACT

There are an estimated 15 million babies born preterm every year and it is on the rise. The complications that arise from this can be quite severe and are the leading causes of death among children under 5 years of age. Among these complications is a condition known as apnea. This disorder is defined as the suspension of breathing during sleep for usually 10 to 30 seconds and can occur up to 20-30 times per hour for preterm infants. This lack of oxygen in the bloodstream can have troubling effects, such as brain damage and death if the apnea period is longer than expected. This creates a dire need to continuously monitor the respiration state of babies born prematurely. Given that the breathing signal is in analog form, a conversion to its digital counterpart is necessary.

In this thesis, a novel low power analog-to-digital converter (ADC) for the digitization and analyzation of the respiration signal is presented. The design of the ADC demonstrates an innovative approach on how to operate on a single polarity supply system, which effectively doubles the sampling speed. The ADC has been realized in a standard 130 nm CMOS process.

TABLE OF CONTENTS

Chapter One Introduction 1
1.1 Motivation 1
1.2 Research Goal 4
1.3 Thesis Overview 4
Chapter Two Literature Review 5
2.1 Successive-Approximation-Register (SAR) ADC 6
2.1.1 Structure and Conversion Procedure 6
2.1.2 Summary 10
2.2 Pipelined ADC 10
2.2.1 Structure and Conversion Procedure 11
2.2.2 Summary 12
2.3 Delta-Sigma ADC 13
2.3.1 Oversampling 14
2.3.2 Delta-Sigma Modulator 17
2.3.3 Digital Filter and Decimator 18
2.3.4 Summary 18
2.4 Flash ADC 19
2.4.1 Structure and Conversion Process 19
2.4.2 Summary 22
2.5 Integrating ADC 22
2.5.1 Single Slope Architecture 23
2.5.2 Dual Slope Architecture 26
Chapter Three Materials and Methods 31
3.1 Design Overview and Specifications 31
3.1.1 Overview 31
3.1.2 Specifications 35
3.2 ADC Selection and Design 38
3.3 Dual Slope Mid-Rail ADC Approach 39
3.4 System Overview 44
3.4.1 Mid-Rail Method Design Adjustments 46
3.5 Integrator 47
3.5.1 Operational Transimpedance Amplifier (OTA) 47
3.5.2 Charge Injection 57
3.5.3 Results 60
3.6 Comparator 63
3.6.1 Preamplifier 64
3.6.2 Latch 68
3.6.3 Output Buffer 71
3.6.3 Results 72
3.7 Counter 78
3.8 Register 82

3.9 Control Logic 84
Chapter Four Results and Discussion 85
4.1 Analyzation Algorithm 85
4.2 ADC Performance 87
Chapter Five Conclusions and Future work 93
5.1 Conclusions 93
5.2 Original Contributions 94
5.3 Future Work 94
References 96
Vita 100

LIST OF TABLES

Table 3.1 ADC Specifications 38
Table 3.2 OTA Specifications..... 49
Table 3.3 Operating Conditions of Transistors in Folded Cascode Amplifier 54
Table 3.4 OTA Performance Metrics..... 55
Table 3.5 Adjusted Reference Voltages for Charge Injection 60
Table 3.6 Design Specifications for Comparator..... 64
Table 3.7 Operating Conditions of MOSFETs in Preamplifier 67
Table 3.8 Operating Conditions of MOSFETs in Latch 70
Table 3.9 Comparator Performance Metrics..... 76
Table 3.10 Example 4-bit Binary and Gray Code Count..... 81
Table 4.1 ADC Performance Metrics 91
Table 4.2 Performance Comparison 92

LIST OF FIGURES

Figure 1.1 Obstructed Airway of Patient with OSAS [4]. 2
Figure 2.1 Architecture of a SAR ADC []. 7
Figure 2.2 Successive approximation conversion procedure [10]. 9
Figure 2.3 Pipeline ADC architecture [13]. 11
Figure 2.4 Architecture of a Delta-Sigma ADC [17]. 14
Figure 2.5 Noise floor when sampling at Nyquist frequency [16]. 15
Figure 2.6 Noise floor when implementing oversampling technique [16]. 16
Figure 2.7 Block diagram of a Delta-Sigma modulator [19]. 17
Figure 2.8 Illustration of the mechanism of noise shaping [16]. 18
Figure 2.9 Architecture of a low-resolution flash ADC [21]. 20
Figure 2.10 Block diagram of a single slope ADC [23]. 23
Figure 2.11 Schematic of a dual slope ADC architecture [27]. 27
Figure 2.12 Integration of the output voltage for increasing analog input voltages [28]. 28
Figure 3.1 Block diagram of respiration monitoring system [7]. 32
Figure 3.2 Overview of the respiration monitoring system. 34
Figure 3.3 Apneic event when monitoring the breathing signal [30]. 34
Figure 3.4 Ideal transfer function of an ideal ADC [31]. 37
Figure 3.5 Demonstration of mid-rail methodology. 42
Figure 3.6 Resolution split into N-1 for each side of mid-rail. 43
Figure 3.7 Overview of the mid-rail dual slope ADC. 45
Figure 3.8 Schematic of the integrator architecture. 48
Figure 3.9 Circuit schematic of a folded cascode PMOS OTA. 49
Figure 3.10 Level of impact of inversion on transconductance efficiency [33]. 51
Figure 3.11 Tradeoffs for various selected inversion coefficients and channel lengths [34]. 52
Figure 3.12 Open loop response of the OTA. 56
Figure 3.13 Noise spectrum of the OTA. 56
Figure 3.14 NMOS switch exhibiting charge injection [24]. 57
Figure 3.15 Schematic of the transmission gate charge injection compensation method. 58
Figure 3.16 Circuit schematic of the pseudo-differential switch driver [35]. 59
Figure 3.17 Integrator performance with input voltages below mid-rail. 61
Figure 3.18 Integrator performance with input voltages above mid-rail. 61
Figure 3.19 Layout of the integrator. 62
Figure 3.20 Block diagram of the comparator. 63
Figure 3.21 Schematic of the preamplifier structure. 65
Figure 3.22 Schematic of the decision circuit. 69
Figure 3.23 Schematic of the output buffer. 71
Figure 3.24 Functional verification of the comparator. 72
Figure 3.25 Noise testing configuration of the comparator. 74
Figure 3.26 Transient output of noise analysis. 75
Figure 3.27 Histogram of the noise analysis. 75

Figure 3.28 Layout of the comparator. 77
Figure 3.29 Schematic of a binary counter structure employing T flip flops [36]. 78
Figure 3.30 Binary to Gray code conversion circuit [37]. 79
Figure 3.31 Gray code counting waveforms. 80
Figure 3.32 Layout of digital portion of the ADC. 80
Figure 3.33 D-latch configuration [38]. 82
Figure 3.34 Truth table for D-latch [38]. 83
Figure 4.1 Analyzation algorithm conversion diagram. 86
Figure 4.2 Transfer function of the ADC. 88
Figure 4.3 INL and DNL performances of the designed ADC. 90
Figure 4.4 Final layout of the designed ADC. 91

ABBREVIATIONS

ADC	Analog-to-Digital Converter
CSAS	Central Sleep Apnea Syndrome
DAC	Digital-to-Analog Converter
DC	Direct Current
DNL	Differential Nonlinearity
EOC	End of Conversion
g_m	Transconductance
IC	Inversion Coefficient
INL	Integral Nonlinearity
IR-UWB	Impulse Radio Ultra-Wideband
LSB	Least Significant Bit
MHz	Megahertz
MSB	Most Significant bit
Msps	Megasamples per second
NICU	Neonatal Intensive Care Unit
OSAS	Obstructive Sleep Apnea Syndrome
SAR	Successive-Approximation-Register
SHA	Sample and Hold Amplifier
SNR	Signal to Noise Ratio
V	Volts
V_{GS}	Gate to Source Voltage
V_{IN}	Input Voltage
V_{LSB}	Voltage Least Significant Bit
V_{pp}	Volts peak-to-peak
V_{REF}	Reference Voltage
W	Watts

CHAPTER ONE

INTRODUCTION

In this chapter, the biomedical background of the project is introduced in section 1.1. Then the goal of this research is presented in section 1.2. The overview of the thesis is given in section 1.3.

1.1 Motivation

Apnea is a dangerous breathing condition that can be potentially life threatening. This disorder is defined as the suspension of breathing during sleep for usually 10 to 30 seconds and can occur up to 20-30 times per hour [1]. This lack of oxygen in the bloodstream can have troubling effects, such as brain damage and death if the apnea period is longer than expected. Up to 18 million people suffer from apnea in North America alone [2]. There are two different types of apnea: obstructive sleep apnea syndrome (OSAS) and central sleep apnea syndrome (CSAS). Obstructive sleep apnea is the more common of the two. This type is caused by the partial or complete obstruction of the upper airway. This type of the disorder affects 2-4% of the adult population [3]. Central sleep apnea is brought about by improper communication between the brain and the muscles that control the breathing. Figure 1.1 demonstrates a patient with OSAS [4].

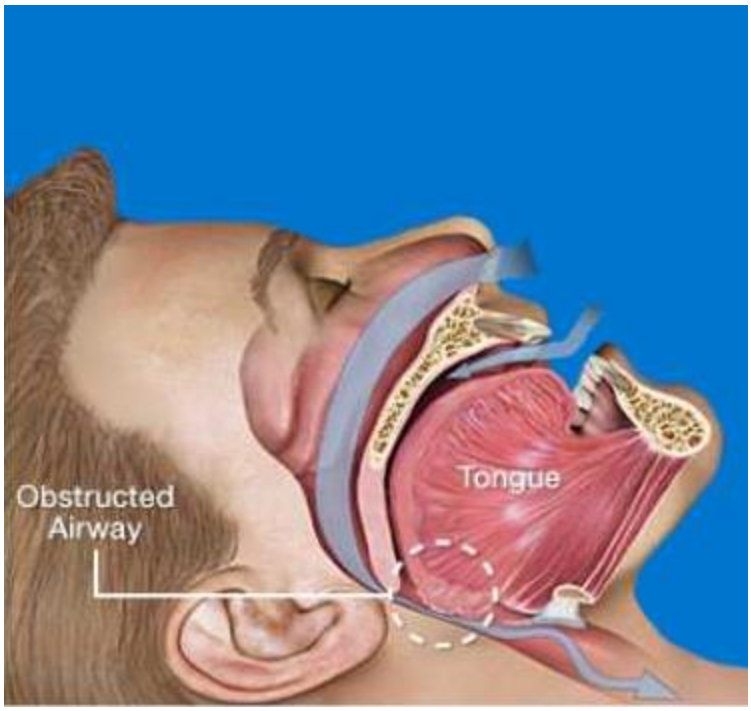


Figure 1.1 Obstructed Airway of Patient with OSAS [4].

Apnea is also a serious issue for infants. 15% of term infants and 29% of late preterm infants are admitted to the NICU for respiratory distress [5]. This presents a dire need for the monitoring of the respiration of infants. Around $24 million is already spent annually within the United States on respiration monitoring systems for infants in the NICU [6]. If this disease were to go untreated, it can lead to a variety of cardiovascular diseases and even death. The aim of this research is to monitor the respiration of infants in the neonatal intensive care unit (NICU) and detect an occurrence of apnea.

Monitoring and detecting this disorder can prove to be quite difficult due to the sleeping process needed to be observed and analyzed by experienced scientists. Many of these detection methods require sensors to be placed on the skin and other invasive techniques. A non-intrusive respiration monitoring system is being developed by researchers that can be very impactful in the detection of apnea [7]. This system records the breathing signal and converts it to digital form at the output. It functions by monitoring a period where there is little to no activity in the breathing signal and acting on it. The need for the digital output calls for an analog-to-digital converter (ADC) within the system because the breathing signal introduced into the system is analog. The motivation for this work is to develop a low power analog-to-digital converter that will be utilized in a respiration monitoring system for infants in the NICU.

1.2 Research Goal

The purpose of this research is to create a low power analog-to-digital converter implemented in a nonintrusive wireless respiration monitoring system. The ADC to be designed will be a mid-rail dual slope architecture operating on a 1.2 Volt supply system. This converter aims for low power to prolong the life of the wireless unit. The ADC should take up as little room as possible and be cost efficient while maintaining proper operation throughout the entire conversion cycle.

1.3 Thesis Overview

The rest of this thesis is organized as follows: Chapter 2 will review the various analog-to-digital converter topologies. Chapter 3 will present the system overview and discuss each aspect of the ADC design. Chapter 4 will demonstrate the simulated results of the assorted components of the converter and the ADC. Chapter 5 will discuss conclusions and possible future work.

CHAPTER TWO

LITERATURE REVIEW

Data converters facilitate interfacing the real world analog signals to the digital world. Analog signals are continuous signals that vary with time while digital signals can only be represented as a combination of discrete values. The real world consists of vital analog signals that need to be converted, processed, and controlled by digital systems. Digital-to-analog converters (DAC) and analog-to-digital converters (ADC) are necessary in every system that requires to interface between the real world and the digital world.

ADCs are a critical component of our modern-day electronics. The differing topologies permit a wide range of customizable converters with respect to the parameters of conversion time, sampling rate, and resolution. These various architectures allow for a wide range of applications from the biomedical field to being utilized in recording audio. There are two main types of data converters: Nyquist rate and oversampling. Nyquist rate ADCs generate a series of output values in which each output value has a one-to-one correspondence with a single input value. According to the Nyquist theory, the sampling frequency should be at least twice the bandwidth of the input signal. To avoid degradation in the least significant bit (LSB) conversion, the ADC needs to function well above the Nyquist frequency. Oversampling converters operate at a much faster rate than that of a Nyquist-rate converter. The oversampling method functions by applying noise shaping to filter out the quantization noise. For this reason, the signal-to-noise ratio (SNR) of the data

converter is increased. Common ADC topologies of both types of sampling techniques will be discussed throughout this chapter along with their advantages and disadvantages.

2.1 Successive-Approximation-Register (SAR) ADC

A successive-approximation-register (SAR) analog-to-digital converter is one of the most widely used conversion architectures. It is a desirable middle ground between the other data converter structures to convert at moderate rate, has medium accuracy, and medium complexity. Applications requiring a resolution and sampling rates up to 5 megasamples per second (Msps) are suitable for the SAR data converter. The SAR structure is a reliable converter with a small form factor, low power consumption, and is relatively inexpensive. The tradeoffs between the speed and the converter complexity make the structure suitable for a wide range of applications. The downside to this specific design is that it has poor immunity to noise. It is commonly employed in applications such as data acquisition, portable instruments, and industrial controls [8]. Biomedical applications frequently utilize this data converter as they call for a structure that has a moderate resolution, low cost, and is power-effective.

2.1.1 Structure and Conversion Procedure

The structure of the SAR ADC is considerably straightforward. Figure 2.1 depicts how the SAR data converter is constructed [9]. This type of ADC employs a binary search

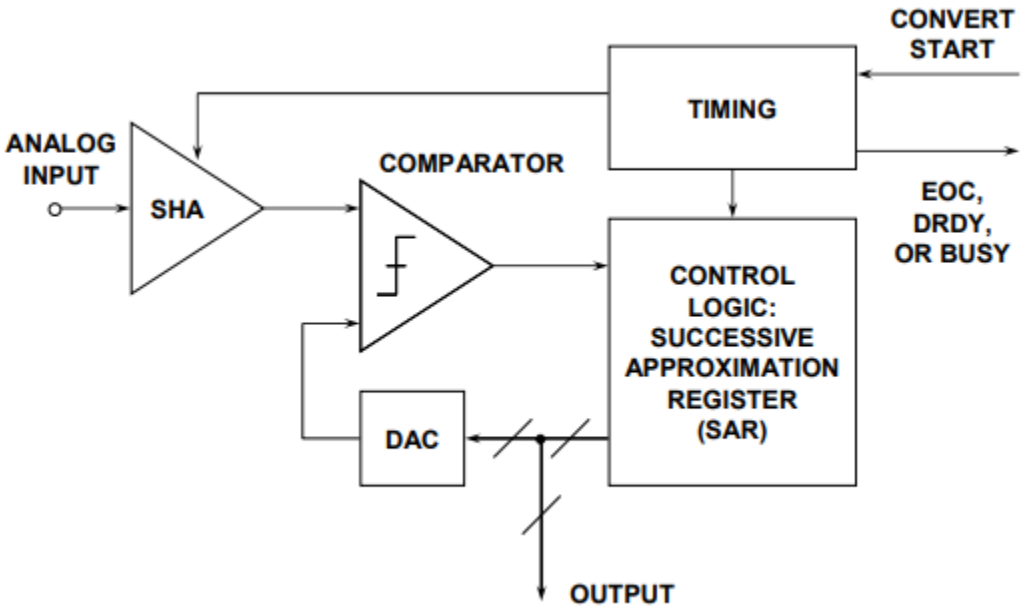


Figure 2.1 Architecture of a SAR ADC [].

algorithm. It functions by multiple comparisons of the analog input voltage to a dynamically changing reference voltage. The method effectively inserts a logic ’1’ at each bit of the digital output one step at a time and decides if that bit should remain a logic ‘1’ or logic ‘0’ by comparing the equivalent reference voltage to the input voltage.

At the start of the conversion, the reference voltage and the register are set to mid-rail. In the first step of the conversion process the analog input is fed into the sample-and-hold amplifier (SHA). A SHA has two types of modes: track and latch. When the amplifier is in track mode, its output will follow the input as it will be in unity gain configuration. During the latch stage, the analog input is cut off from the amplifier and the voltage is held on a capacitor. The output will then proceed to be a constant direct current (DC) voltage. The latch stage allows the converter to perform the conversion for a constant signal, as a changing input would severely affect the accuracy of the desired digital output. To acquire the analog input, the SHA has the latch stage enabled. The output SHA voltage is then directed into the comparator, which decides whether the input DC voltage (V_{IN}) is larger or smaller than half the reference voltage (V_{REF}). The comparator will output a logic ‘1’ if $V_{IN} > \frac{V_{REF}}{2}$ and a logic ‘0’ if $V_{IN} < \frac{V_{REF}}{2}$ for the first conversion cycle. Each bit of the digital output will require the comparator to compare the constant input voltage against a varying reference voltage.

The logic signal is then input into the register, which will store it as the most significant bit (MSB). Once the bit has been stored, a logic ‘1’ will be inserted into the next MSB. Depending on whether the input into the successive approximation register is logic ‘high’ or logic ‘low’, the reference voltage will be again halved in the respective side of

the voltage range. For instance, if the comparator output is a logic ‘high’ for the first conversion, it will be stored in the register and a logic ‘1’ will be inserted into the next MSB of the digital output. The digital-to-analog converter then takes the output of the register and converts it to an analog output voltage that will then be used as the next reference for the comparator for the next bit comparison. Once the conversion has been completed, the end of conversion (EOC) output will signal that the ADC is not busy. Figure 2.2 displays the successive approximation conversion procedure [10].

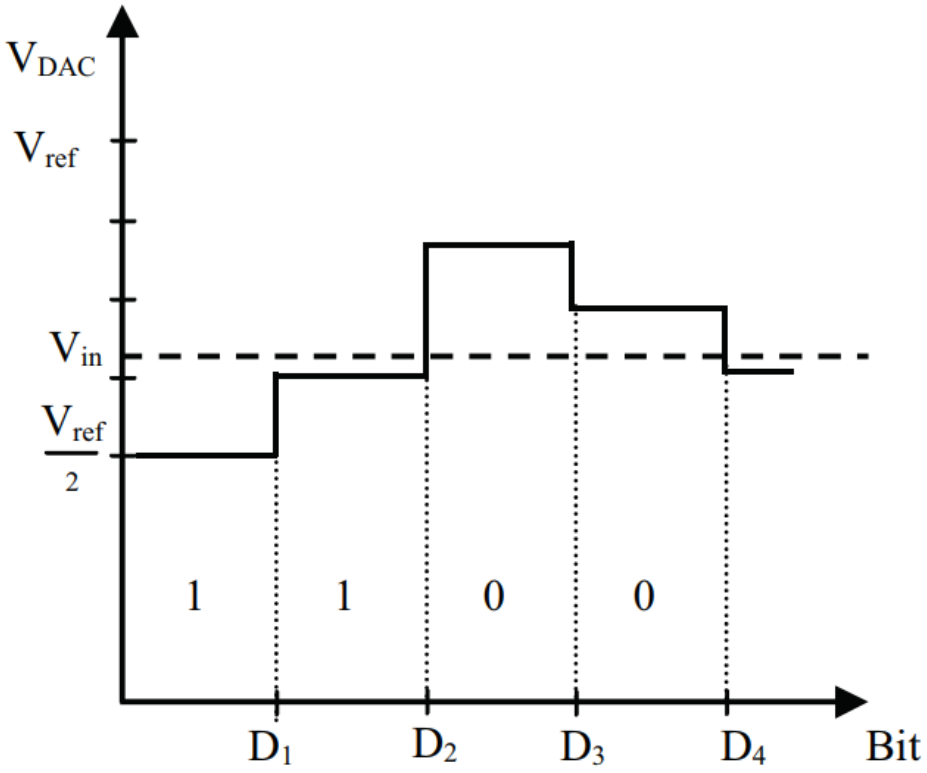


Figure 2.2 Successive approximation conversion procedure [10].

2.1.2 Summary

Due to the converter only being capable of comparing one bit at a time, the process will require *n* clock periods to encode an *n*-bit binary value. The resolution of the data converter output is $2^N - 1$. One digital code will be affected since an analog input which is at mid-rail, the same as the starting reference voltage, will impair the conversion process. A four-bit SAR ADC can complete a conversion cycle in 8μs given a clock period of 1μs. As with any data converter, the accuracy of the digital output decreases as the speed of the conversion increases. The speed and accuracy of the SAR converter are limited by DAC implemented in the architecture. If the DAC were not accurate, the reference voltage would be awry and the whole algorithm is in turn ruined. Other sources of error arise from the need for the transient signals to subside before the converter can continue to the next step. The DAC requires an adequate amount of time to reach its final value and the settling time is greatly affected at the MSB. Due to the limitations of the DAC, resolutions of 12 bits and higher will require calibration of the ADC. Also, the comparator necessitates an ample amount of time to recover from the previous input and to generate an output dependent on its new input from the DAC [11].

2.2 Pipelined ADC

The pipelined analog-to-digital converter is desired when the SAR ADC architecture fails to hold up for high sampling rates. The pipelined methodology is a prominent Nyquist rate architecture for sampling rates from a few mega samples per second

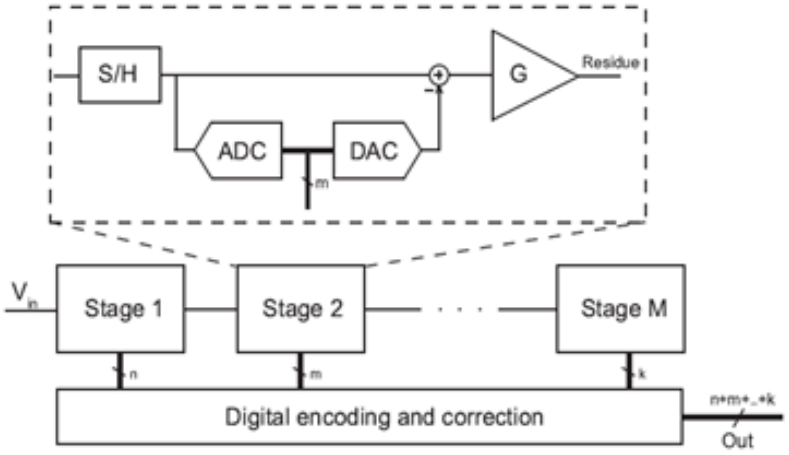


Figure 2.3 Pipeline ADC architecture [13].

up to 100 Msps. The structure is capable of moderate resolutions of 8 – 16 bits. It can sample faster on the low end of the resolution scale and is restricted to sampling slower approaching sixteen-bit resolution due to the circuit limitations and increased complexity. The high sampling rates and the resolution range establish the pipeline ADC appropriate for a wide range of applications, such as digital receivers, base stations, Ethernet, and ultrasonic medical imaging [12]. Architecture of the pipelined converter combines elements of successive approximation and flash conversion techniques into a system that utilizes pipeline-type signal processing.

2.2.1 Structure and Conversion Procedure

Figure 2.3 depicts the composition of the pipelined ADC [13]. In pipelined signal processing, the analog-to-digital (ADC) conversion is executed on each sample of the analog data during a period of two or more samples times of the analog data. This concept

means that the stages of the parallel structure of the pipelined data converter can work on a few bits concurrently.

The analog-to-digital conversion starts by sampling the analog input and holding it on the sample-and-hold amplifier (SHA). The first stage of the ADC converts a few of the most significant bits during this hold time and then passes the residue onto the next stage of the converter. When the residue has been passed, the SHA has a new analog input ready and has latch mode enabled. The first stage repeats what it has done before and converts the MSBs of the analog input while the second stage of the pipeline now converts the residue of the previous sample to the next MSBs. This cycle continues as more inputs are fed into the first stage and the residue is be passed on to more stages until all the bit values have been determined. Each stage acts as a partial data converter since only a few bits are converted per stage.

The digital encoding and correction component will be utilized in storing of the digital output bits from each stage. In addition, it corrects the output from the stages by employing shift registers to reorder the output bits appropriately to form a full *n*-bit digital value. Additional error correction methods are typically added due to the appeal of it reducing the accuracy requirements for the analog-to-digital conversion.

2.2.2 Summary

Due to the combination of continual intake of analog inputs and each stage performing a partial conversion, very high sampling rates can be achieved. Although, the digital output for each sample is delayed since it must pass through numerous stages in the pipeline. The latency of the digital output value caused by the circuitry is insignificant to

many applications as the analog sampling rate is the upmost of importance [14]. SAR converters may convert an analog value quicker than the pipeline method, but it samples at a much slower speed.

Capacity of high sampling rates and medium-to-high resolution makes the pipeline framework an ideal data converter for numerous applications. However, as the desired resolution increases, power dissipation and area grow linearly with the number of bits [15].

2.3 Delta-Sigma ADC

The delta-sigma analog-to-digital converter realizes a high resolution and can be applied to a wide range of sampling frequencies. It is one of the more advanced data converter technologies since it relies on the oversampling technique, which will be discussed further below. SAR converters are often chosen over Delta-Sigma ADCs due to the simplicity of its structure. The Delta-Sigma converter architecture is often overlooked since it is not widely understood and the design process can be quite challenging. Although, the Delta-Sigma ADC is the more advantageous design since it does not require trimming or calibration when a high resolution is needed. This type of converter trades speed for resolution. 2^N steps are required for the ADC to complete a conversion, which is quite slow when compared to a SAR converter that only needs *n* steps. Applications that typically employ this analog-to-digital converter are communication systems, professional audio, and precision measurements [16].

The aim of the converter is to take advantage of the inherent speed of analog circuits and combine that with the dependability of digital circuits. Since the structure of the

converter is predominantly digital, a reduced number of analog components are necessary. Consequently, the analog circuity does not call for a high accuracy. The ADC is generally composed of a Delta-Sigma modulator, a filter, and a decimator. The structure of the ADC can be seen in Figure 2.4 [17]. Each of these components will be discussed in a following section.



Figure 2.4 Architecture of a Delta-Sigma ADC [17].

2.3.1 Oversampling

The analog input signal into an ADC is continuous and can be an infinite amount of values between the supply voltages. In contrast, the digital output is represented as discrete bits. As a result, the analog input into the system cannot always be fully represented by its true value and the information is lost in the conversion. The difference between the analog input and output can be referred to as quantization noise.

In a Nyquist rate converter, the quantization noise has a higher noise floor because more information is lost when implementing the Nyquist sampling frequency. This happens because the sampling takes much larger steps when sampling the input compared to oversampling. Oversampling technique typically samples from 20 to 512 times faster than the Nyquist rate of the input signal [18]. When oversampling, the noise is spread out

over the spectrum as its sampling frequency is much more defined. Figures 2.5 and 2.6 demonstrate the difference between the noise floors for the two techniques [16].

The components within the architecture operate at the oversampling frequency and not the output data rate. Due to the need of sampling much faster than the output data rate, the converter is limited by the operation of the internal components and cannot be operated of a bandwidth of a few megahertz (MHz) [8]. As a result, the Delta-Sigma ADC is commonly adopted for lower frequencies.

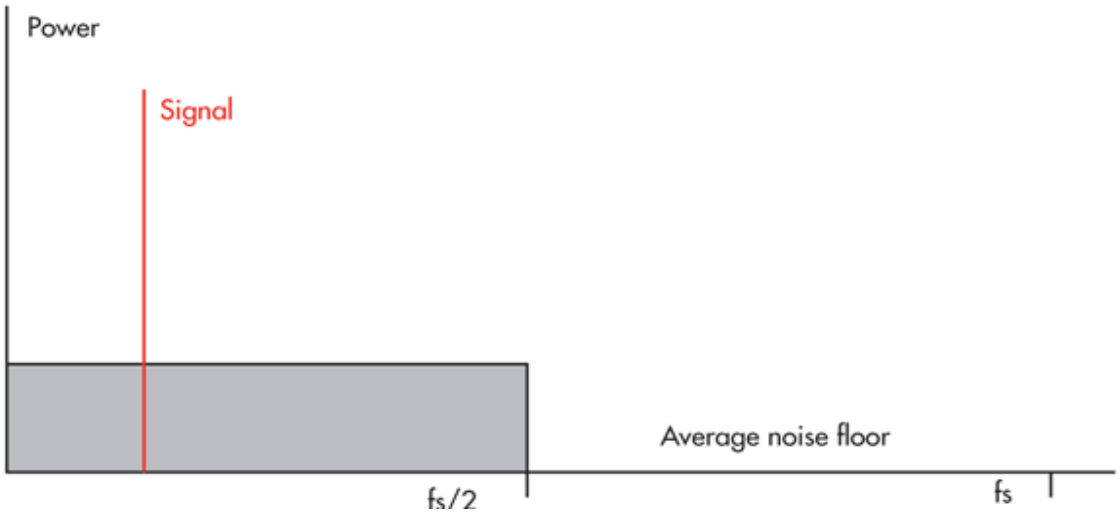


Figure 2.5 Noise floor when sampling at Nyquist frequency [16].

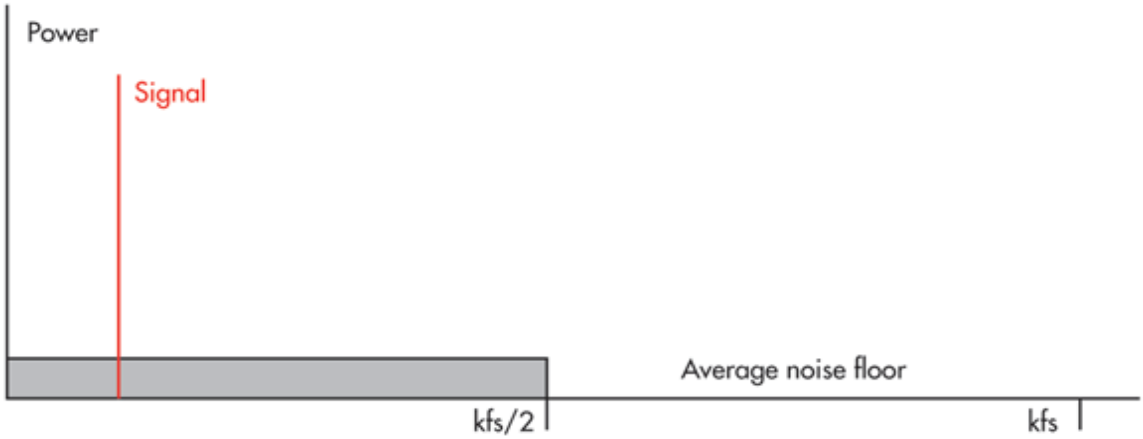


Figure 2.6 Noise floor when implementing oversampling technique [16].

2.3.2 Delta-Sigma Modulator

The purpose of a modulator is to perform a process called noise shaping and function as a 1-bit ADC. Noise shaping is performed when the noise power of the amplifier is distributed out from the low frequency spectrum and pushed onto the high frequency side. The overall noise power of the converter does not change in this process, but instead is simply pushed towards higher frequencies. The modulator structure, which can be observed in Figure 2.7, accomplishes this feat by having an integrator functioning as a low-pass filter for the analog input and a high-pass filter for the quantization noise [19]. It performs this process by summing the error voltage.

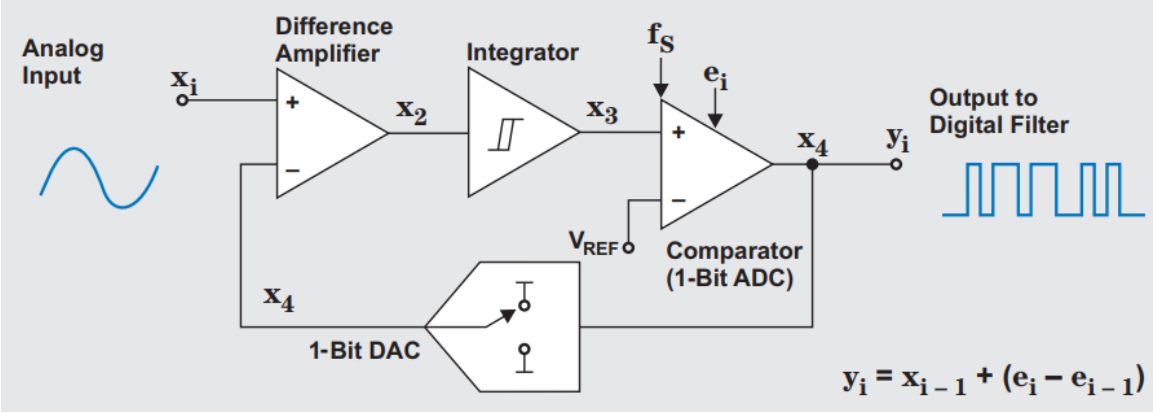


Figure 2.7 Block diagram of a Delta-Sigma modulator [19].

Figure 2.8 exhibits the effect of noise shaping has on a signal [16]. A pulse train of 1s and 0s are generated at the output of the modulator.

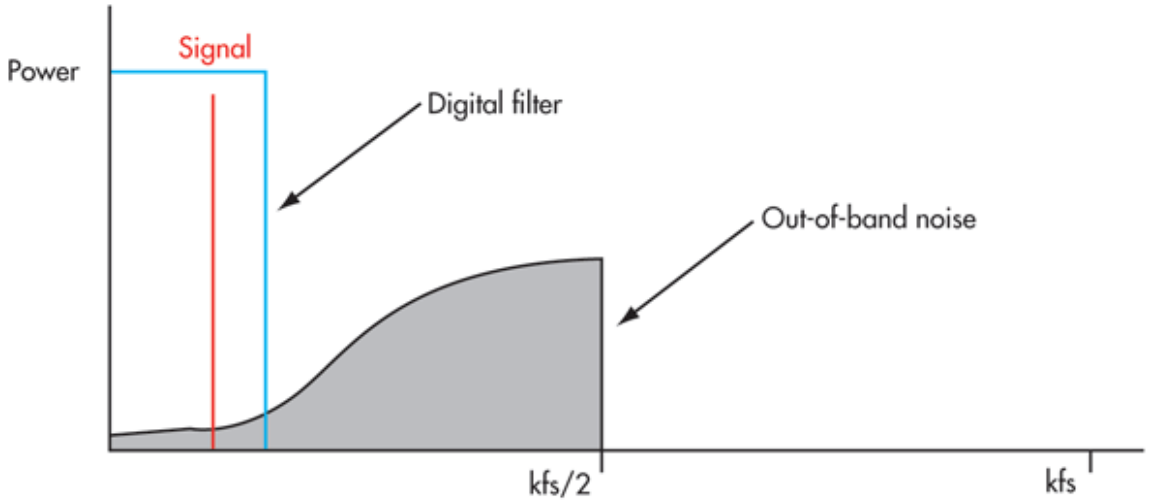


Figure 2.8 Illustration of the mechanism of noise shaping [16].

2.3.3 Digital Filter and Decimator

After the data has been processed in the Delta-Sigma modulator, a digital 1-bit pulse stream is fed into the decimator and the digital filter. The goal of these elements is to convert the data stream into a high-resolution digital code. In addition, it aims to slow down the code to that of a Nyquist sampling rate.

Once the noise has been shaped by the modulator, the digital filter filters out the high frequency noise power to where the signal and a minute amount of noise power are left. Decimation can be described as the method of eliminating unnecessary samples. It effectively reduces the data rate from the digital filter to a usable amount.

2.3.4 Summary

The Delta-Sigma ADC employs a unique and complicated process to convert the analog input to a digital output. Oversampling is not widely employed due to the added

complexity in the design process even though it may possess better qualities that Nyquist rate ADCs cannot attain. It achieves a reduced signal-to-noise ratio and does not require error correction such as calibration and trimming to obtain a high resolution.

2.4 Flash ADC

Flash analog-to-digital converters, often referred to as simultaneous or parallel converters, offer the highest speed of any type of ADC. The conversion takes place in just one step, enabling the data converter to achieve conversion rates of hundreds of megabits per second. The speed may only be limited by the propagation delays of the comparators and the encoding logic, which will be discussed in the next section. Other characteristics of the ADC include a low resolution, low complexity, high cost, high power consumption, and a large area required for implementation on-chip. Applications typically requiring this type of data converter include satellite communication, sampling oscilloscopes, high-density disk drives, radar processing, and data acquisition [20]. This Nyquist rate converter is typically utilized for resolutions of 8 bits and below due to the circuitry required.

2.4.1 Structure and Conversion Process

A parallel converter is commonly constructed in three stages: a resistor ladder, network of comparators, and combination encoding logic. Figure 2.9 below demonstrates the formation of a low-resolution flash ADC [21]. The conversion process functions by using the resistor ladder to set reference levels at each V_{LSB}, which can be defined as the voltage change when one least significant bit changes over. Each resistor in the string

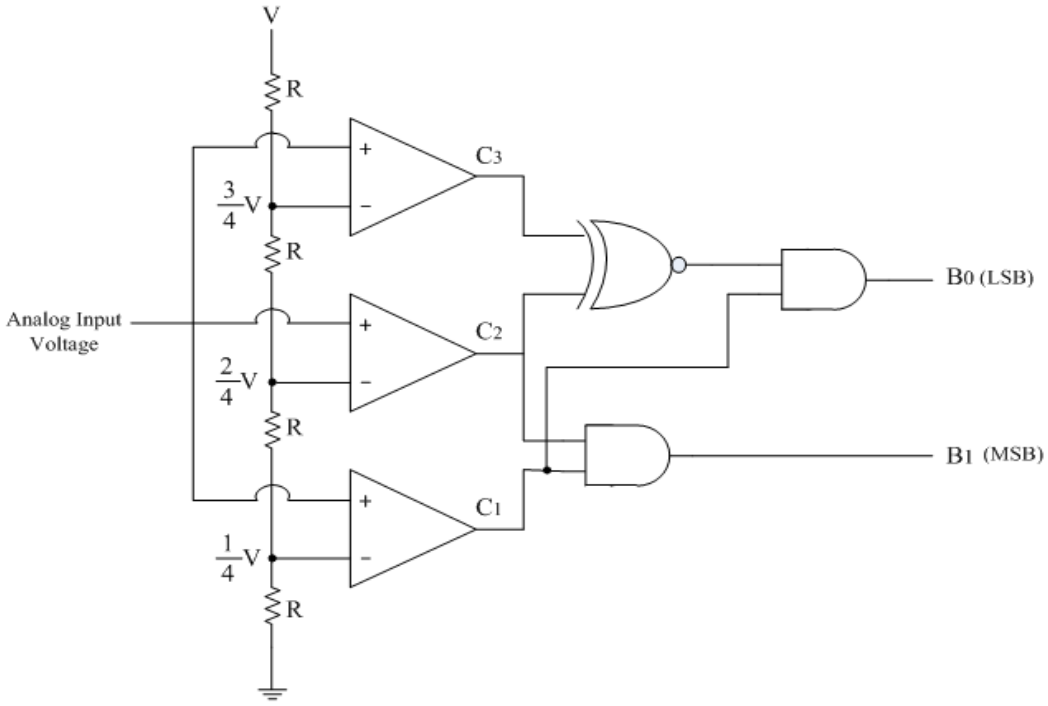


Figure 2.9 Architecture of a low-resolution flash ADC [21].

provides a voltage drop of V_{LSB}, except for the first and the last resistors which are sometimes half the size of the others due to the want of creating a 0.5 LSB offset in the ADC.

The voltage references provided by the resistor ladder are then fed into a parallel comparator structure. The architecture requires 2^n resistors and 2^{n-1} comparators, resulting in an exponential expanding composition for each bit of resolution. Owing to the resistor string setting the threshold voltage for each comparator, the input can be connected to the other input of every comparator so that it can easily be compared against every V_{LSB} at once. When the input is larger than one of the reference voltages, the comparator will flip from 0 to 1, as will all the ones further down the resistor ladder will do. As a result, a thermometer code is generated at the output of the parallel comparator structure.

The thermometer code then needs to be decoded to the correct digital output code. A priority encoder is typically utilized for this application. It takes in the code and generates a binary number based on the location of the MSB that is a one. All the other LSBs after the first active high is encountered are ignored. The architecture of the encoder is composed of a combination of various logic gates.

The code generated from the comparators does not always exactly come out as thermometer code. A '0' or '1' may be missing or arise earlier than expected, resulting in incorrect code. This occurrence is known as a bubble error. Correction schemes are commonly implemented to fix this issue if it arises. The correction structure is often composed of a combination of NAND and inverter gates, or it can be implemented with a mux structure.

2.4.2 Summary

The flash ADC has the upper hand over other converter architectures since it can convert the analog input to a digital output in less than a 100ns [21]. Coupled with its straightforward design process, the ADC is essential for applications that require high conversion rates although, it does not come without its disadvantages. As the desired resolution of the ADC increases, the resistors, comparators, and encoding logic required are exponentially increased. For this reason, the power consumption and the area on chip can be very high, which also results in an increase in cost. Due to the exponential nature of the flash converter as the resolution is increased, it is only feasible for applications requiring 8 bits or less.

2.5 Integrating ADC

Integrating analog-to-digital converters are a popular architecture for DC or slowly varying analog inputs. Additionally, it is favorable for high accuracy data conversions. It possesses a low complexity design process and a small amount of circuitry is required. Consequently, a low cost can be achieved. The integrating Nyquist rate converter is highly linear, has good noise rejection, and bears low offset and gain errors. Integrating ADCs are known for their slow conversion rates and high resolutions. The conversion rate for the standard integrating ADC, single or dual slope, can only be as fast as 2^N clock cycles. When compared against other ADC architectures, the integrating structure is exceptionally slower. Due to the slow conversion times, it will not be found in either signal processing

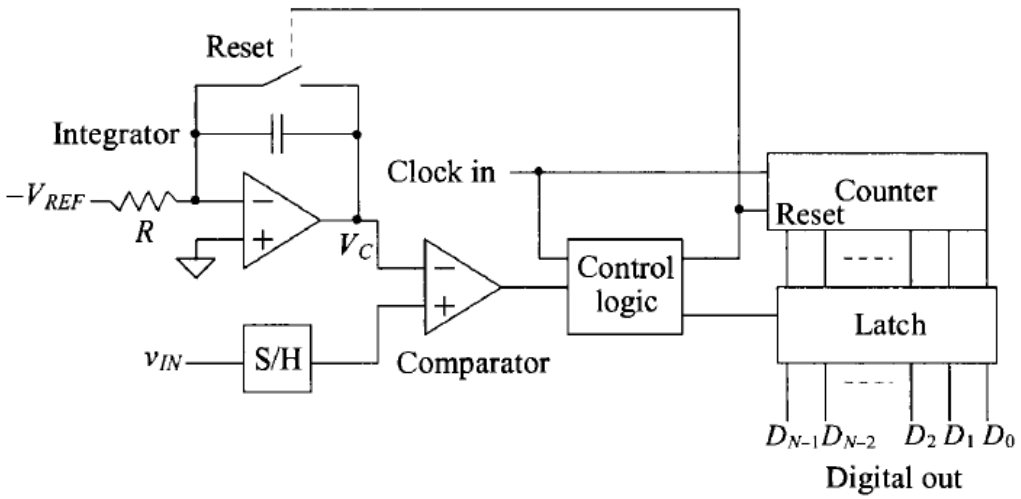


Figure 2.10 Block diagram of a single slope ADC [23].

or audio applications. This type of converter finds its use in high accuracy applications such as drivers for LCD or LED displays and measurement instruments [22].

2.5.1 Single Slope Architecture

The conversion time of a single slope ADC takes place in 2^N clock cycles. This is as twice as fast as the dual slope architecture, which will be discussed later. However, the difference in conversion time is not as meaningful as both designs are very slow comparatively to other types of ADC.

Structure and Conversion Process

The single slope architecture is the simplest of all the prominent ADCs and requires a very small amount of area on chip. The design of the single slope ADC can be seen in Figure 2.10 [23]. The conversion begins with the sample-and-hold amplifier sampling a

low bandwidth analog signal. It is then put into hold mode and input into a voltage comparator.

The reference signal is fed into a component called an integrator. This component produces an output voltage that is proportional to the integral of the input voltage. The current generated by the reference voltage flows through the resistor and into the capacitor, which will begin to charge up. Current flowing through the resistor can be modeled by the following equation [24],

$$I_R = \frac{V_{REF}}{R} \tag{2.1}$$

No current will flow into the operational amplifier due to the input impedance. The current in the capacitor, I_C, is equivalent to the current flowing through the resistor, I_R, and can be described by the following equation [24],

$$I_C = C\frac{dV_{OUT}}{dt} = I_R \tag{2.2}$$

Rearranging the equations, the output voltage can be found as a function of the analog input voltage and passive components. The result will be negative due to the virtual earth condition at the noninverting input. The relation of the equations can be expressed as [24],

$$V_{OUT} = -\frac{1}{RC}\int_0^t V_{in}dt \tag{2.3}$$

The larger the input voltage is, the larger the current will be that is fed into the capacitor which results in a larger output voltage. The RC network controls how quickly the analog input signal is integrated. If it is needed for V_{OUT} to be equivalent to V_{IN} at the end of the conversion, the RC components should be sized accordingly using the following equation [25],

$$RC = 2^N \cdot T_{CLK} \tag{2.4}$$

The ramp generator integrates the analog input voltage and the output is connected to the other input of the voltage comparator. At the beginning of the conversion, the digital counter at the output begins counting. As the reference voltage continuously ramps up, it is compared with the unknown analog input voltage. When it eclipses the value of the input voltage the comparator will flip states causing the counter to shut off. The value at time of shut off will be stored in the latch and wait for the output to be sampled. The output digital count can be represented by the following equation [26],

$$V_{OUT} = \frac{V_{REF} T_{CLK}}{RC} = \frac{V_{IN}}{RC \cdot f_{CLK}} 2^N \tag{2.5}$$

The control logic serves many functions for the converter. It controls when the counter is shut off and subsequently latches the output bits of the counter so that a stable output can be achieved and so that the digital output can be held, even if another conversion begins to take place. Another duty it serves is to reset the integrator and the counter.

Summary

The single slope architecture is an effective low-cost analog-to-digital conversion method for systems realizing high resolutions on low bandwidth analog input signals. It is inexpensive, has a simple design cycle, and is area efficient. The analog-to-digital conversion for the single slope architecture is heavily reliant on the accuracy of the resistor and capacitor values. High tolerances can cause the linear slope of the integrator to deviate off course. This may result in the comparator shutting off at the incorrect time causing an imprecise digital output. The dual slope architecture is often implemented to remedy these errors.

2.5.2 Dual Slope Architecture

A dual slope architecture requires twice the time of the single slope methodology for it performs two integration cycles. The analog-to-digital conversion time can be expressed as [18],

$$T_C = 2^{N+1} \cdot T_{CLK} \tag{2.6}$$

Through the addition of simple circuitry to the single slope design, a dual slope ADC can be realized. The resistor and capacitor tolerance errors are corrected because each integration cycle for one conversion are affected the same. For this reason, the dual slope design does not have any gain error.

Structure and Conversion Process

A dual-slope analog-to-digital converter integrates an unknown analog input for a set amount of time, which is determined by the overflow of the counter at the output. The resulting ramped voltage returns to zero through the integration of a reference signal of opposite polarity to that of the input signal. The ADC normally begins the integration from ground and ramps with a positive slope by integrating a negative analog voltage. Then it is returned to ground by integrating a known positive voltage at the input. The design of a dual slope ADC is illustrated in Figure 2.11 [27]. A sample and hold amplifier is generally utilized at the input for the analog voltage, but it is not shown here for simplicity reasons.

The first half of the conversion is a fixed time interval of length T_1. A binary counter will begin to count when the first integration begins and will trigger the switch at the input to connect to the reference voltage once it overflows. The equation for this time can be modeled by [27],

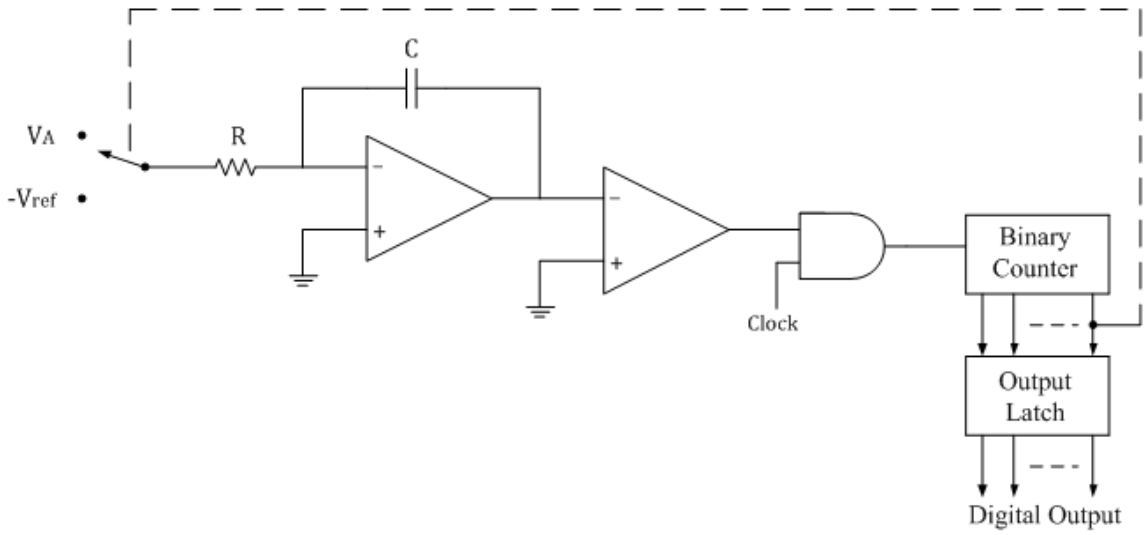


Figure 2.11 Schematic of a dual slope ADC architecture [27].

$$T_1 = 2^N T_{CLK} \tag{2.7}$$

At the end of the first integration cycle, the output voltage of the integrator can be expressed as [27],

$$V_O = \frac{V_{IN} T_1}{RC} \tag{2.8}$$

The larger the input voltage is, the higher the value will be at the end of the first integration period. The switch at the input is then connected to the reference voltage for the next integration period and the binary counter begins counting. The value of the integrator at the end of the second integration period is [27],

$$V_O = \frac{V_{REF} T_2}{RC} \tag{2.9}$$

The reference voltage will discharge the capacitor at a constant slope, regardless of the analog input. Figure 2.12 demonstrates the integrator output voltage over multiple conversion cycles with increasing analog inputs [28].

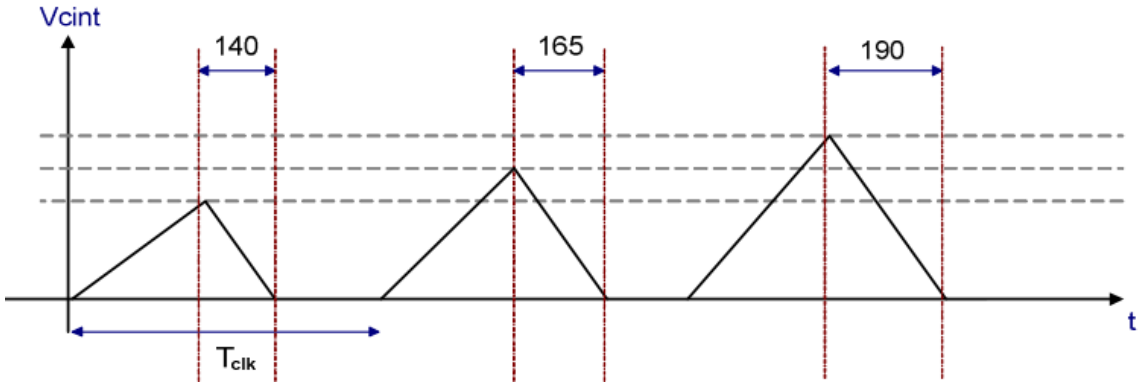


Figure 2.12 Integration of the output voltage for increasing analog input voltages [28].

Once the output voltage of the integrator crosses zero volts during the discharging period, a ground sensing comparator will flip states and cause the counter to turn off and enable the latch. A digital binary number is then represented at the output of the system.

Equating and rearranging the equations 2.8 and 2.9, the resulting expression is found [29],

$$\frac{V_{IN}}{V_{REF}} = \frac{T_2}{T1} \tag{2.10}$$

The left side of equation 2.10 represents the expected digital output while the right side represents the actual digital output of the ADC. As the equation implies, there is no dependence on the resistor and capacitor. Thus, capitalizing on the disadvantage of the single slope ADC. At the end of the analog-to-digital conversion, control logic is implemented to reset the integrator by implementing a closed switch in parallel to reset the voltage on the capacitor back to mid-rail. It also serves the purpose of resetting the counter and controlling when the latch will attain new values.

Summary

The dual slope converter design eliminates the inherent errors of the single slope converter at the price of additional conversion time and a minor amount of added circuitry. The design process remains very simple and a low power can be achieved since very few components are required. The converter has exceptional noise rejection capability as it can reject noise frequencies on the analog input that have periods that are equal or divisible of the first integration period T_1. If the time of T_1 is chosen to be a multiple of $\frac{1}{(60\ Hz)}$, 60 Hz

power line noise will be filtered out [18]. Sources of error may arise from the offset of the comparator and integrator.

CHAPTER THREE

MATERIALS AND METHODS

Chapter 3 details the design of a mid-rail dual slope analog-to-digital converter. Each component will be dissected and discussed in the following sections. The simulated results are also presented for each component to provide a better design flow.

Section 3.1 will discuss the overview and specifications needed for the data converter. Next, Section 3.2 discusses the process behind selecting the appropriate data converter. Then, Section 3.3 will present the methodology behind the mid-rail dual slope ADC approach. The overview of the system is demonstrated in Section 3.6. Design of the integrator and the comparator are covered in Sections 3.5 and 3.6, respectively. Section 3.7 will detail the design of the n-bit counter. The design of the register is discussed in Section 3.8. Finally, the control logic is presented in Section 3.9.

3.1 Design Overview and Specifications

3.1.1 Overview

The aim of this project is to utilize the ADC in a low power wireless piezoelectric sensor-based respiration monitoring system. A block diagram of the system can be seen in Figure 3.1 [7].

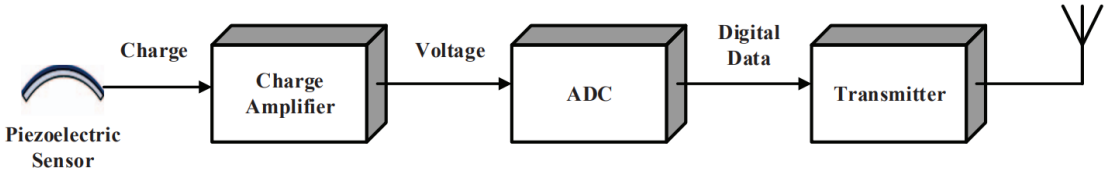


Figure 3.1 Block diagram of respiration monitoring system [7].

The piezoelectric sensor produces a charge signal that is generated in response to vibration in the respiration system due to breathing. The charge amplifier is designed to convert the output charge of the sensor due to the temperature change into a proportional voltage signal. Subsequently, the voltage signal is transferred to an ADC, which will digitize the analog signal. The digital data output by the ADC is input into a radio ultra-wideband (IR-UWB) transmitter which transmits the data wirelessly. A signal processing block is employed between the charge amplifier and the data converter. It monitors the voltage signal and will detects if it remains lower than a certain threshold voltage. If the charge amplifier output continues to stay below the threshold for a consecutive 15 to 20 seconds, apnea is occurring.

A system level overview is presented in Figure 3.2. The blocks as shown above will be realized on a CMOS platform with wireless capabilities. This microchip will be placed inside the nasal cannula of the infant for accurate respiration monitoring. Once the respiration level falls below the set threshold for 15 to 20 seconds, an apnea occurrence is detected and the microchip wirelessly transmits this to a system that can alarm for assistance. Figure 3.3 demonstrates the occurrence of an apneic event through the monitoring of the breathing signal [30].

The system aims to achieve a low cost and low power for longevity of the device. An ADC is critical in this system for it needs to accurately represent the charge amplifier voltage. If it were not accurate, the system could completely miss an apnea occurrence, which could be very detrimental to the user.

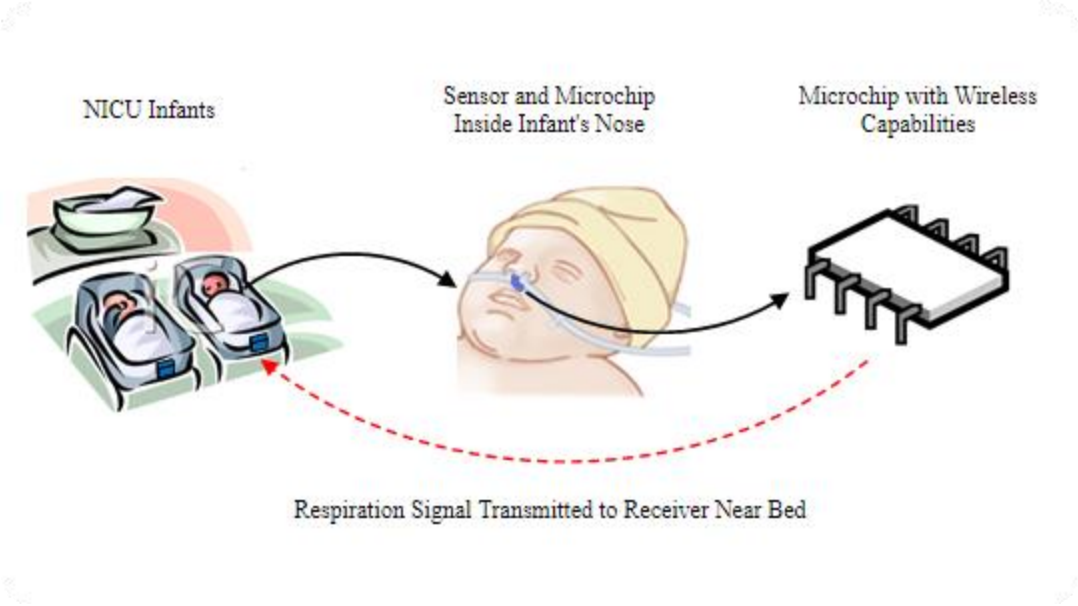


Figure 3.2 Overview of the respiration monitoring system.

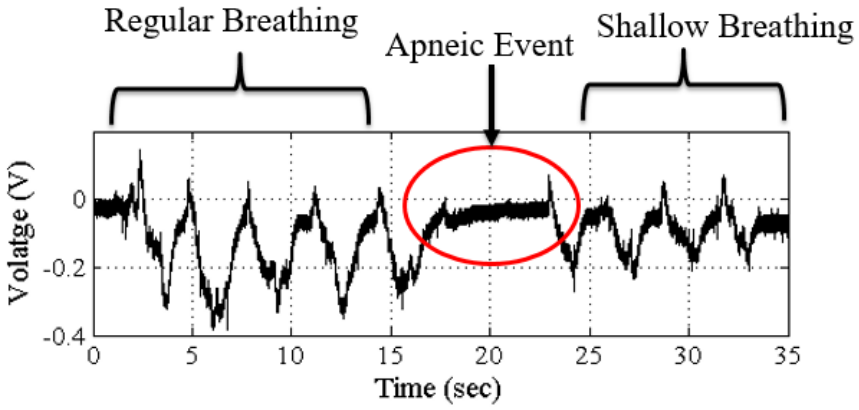


Figure 3.3 Apneic event when monitoring the breathing signal [30].

3.1.2 Specifications

The analog-to-digital converter will be designed and realized in the standard 130nm process. The charge amplifier will produce an analog respiration signal centered at mid-rail. As the rail of the 130nm process is 1.2 Volts (V), the signal will be centered at 600 mV. The input range of the ADC was designed to match the output of the charge amplifier, which is 0.2 – 1 V. Within this range, the breathing signal will be continuously monitored and if the breathing signal falls below 20% of the regular breathing amplitude for 15 to 20 seconds, apnea has occurred. The regular breathing amplitude is defined as the output range of the charge amplifier. 20% of the output range is,

$$0.2 \cdot (1 - 0.2) = 160\ milliVolts\ peak - to - peak\ (Vpp). \tag{3.1}$$

Since the signal is centered at mid-rail, our apnea detection range can be defined as 520 mV – 680 mV. Due to the somewhat large range of detection, a high resolution for the data converter is not needed to convey the needed information. For this reason, the resolution of the ADC is chosen to be 8 bits.

The output signal from the charge amplifier is within the frequency range of 01. – 0.8 Hz range. This is an incredibly slow input signal, greatly relaxing the requirements of the ADC to be selected. Following the Nyquist Theorem, the sampling rate of the converter should be,

$$f_s \geq 2f_{in}. \tag{3.2}$$

This means that the sampling frequency should be equal or more than twice as fast as the signal it is sampling. Although, for the analog input signal to be accurately represented, Nyquist rate converters typically operate at 3 to 20 times the bandwidth of the input signal

[17]. To ensure a high accuracy, the sampling frequency can be set as equal to or greater than 20 times the bandwidth of the input signal, which is $f_s \geq 16\ Hz$.

The conversion time is not of upmost importance for this application as the system monitors the breathing signal for up to 15 seconds and then alerts the user. If the converter is able to quickly alert the user after an apnea occurrence has occurred.

The apnea detection system will be powered by a battery, consequently, power management is crucial for the chip. The ADC was designed on a1.2V supply with the goal of achieving the low power of 50 microwatts (µW).

The accuracy of a data converter is represented by the integral nonlinearity (INL) and differential non-linearity (DNL). The DNL is a measure of the deviation of the actual output code from an LSB when compared against the expected output. INL is the deviation of an ADC's transfer function from a straight line. For example, an ideal ADC would have a transfer function matching that in Figure 3.4 [31].

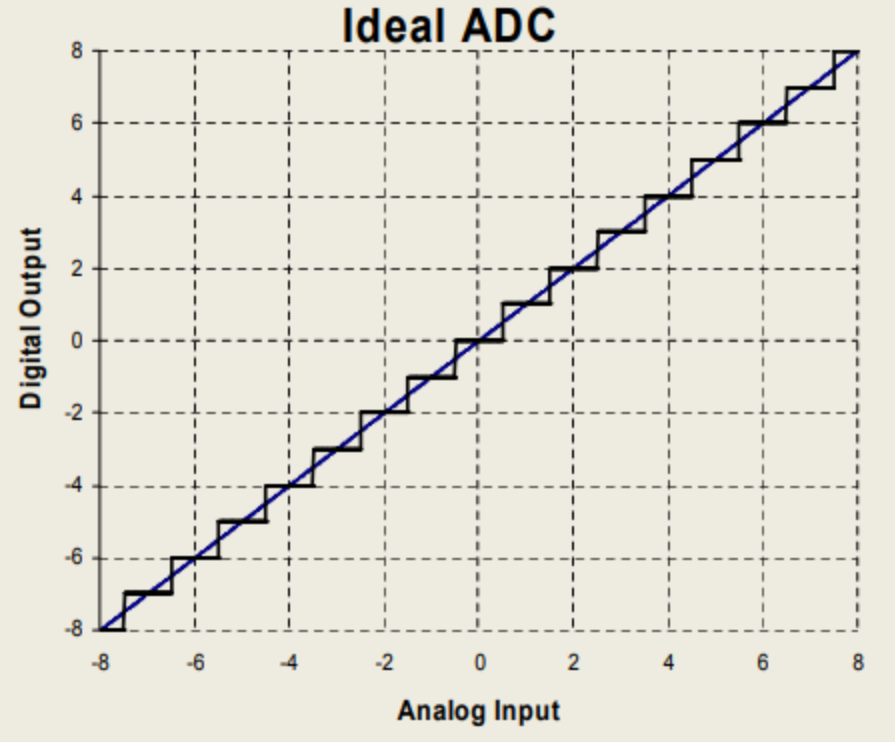


Figure 3.4 Ideal transfer function of an ideal ADC [31].

For an ideal ADC, each analog step will have both DNL and INL = 0 LSB. To guarantee a monotonic transfer function with no missing codes, a DNL of less than or equal to 1 LSB and an INL of less than or equal to 0.5 LSB are required. The ADC was designed to meet the specifications best as possible. Table 3.1 displays the specifications for the analog-to-digital converter to be designed.

Table 3.1 ADC Specifications

Specifications	**Values**
Resolution	8 Bits
Apnea Detection Range	520 – 680 mV
Input Range	0.2 – 1 V
Sampling Frequency	≥ 80 Hz
Power	≤ 50 μW

3.2 ADC Selection and Design

Due to the power and the sampling frequency constraints, the flash and the pipelined converter are not suitable for this application. The Delta -Sigma modulator is not necessary because of the additional design complexity and the increased SNR is not needed for the monitoring of the respiration signal. The SAR and the integrating architectures are the most suited for the task. Even though the integrating structures suffer from a low conversion time, the combination of the leisurely requirements and a fast-enough clock signal will guarantee a suitable conversion time. Both the SAR and the integrating

architectures occupy a low area and can attain a low power. Although the SAR converter converts much quicker than the alternative, a quick conversion time is not paramount. The integrating ADC design offers additional accuracy and better noise performance because the signal integration is a method of averaging. Accordingly, an integrating structure is chosen for the design of the ADC.

Provided that the conversion time is very manageable to obtain, a dual slope converter is chosen over a single slope architecture for it is inherently more accurate at the expense of little additional circuitry.

As the desired integration time increases for the dual slope ADC, the values for the resistor and the capacitor increase as well since they set the time constant for the integration. This results in an unwanted area increase on chip. Another factor that needs to be considered is the dynamic power of the converter. The formula is show by [32],

$$P = C_L VDD^2 f \tag{3.3}$$

The output of the ADC will have a load capacitance of 200 fF. With this and the area in consideration, a clock frequency of 1 MHz is chosen for the ADC. Plugging this into equation 3.3, we arrive at a dynamic power of 288 nW, which is essentially negligible for the requirements of the ADC.

3.3 Dual Slope Mid-Rail ADC Approach

Generally, a dual slope ADC is implemented within a system having opposite polarity input and reference voltages due to the need for the ramp up and ramp down cycles.

Utilizing the design principles of the integrator for a traditional dual slope ADC, a new design methodology can be created without the need for opposite polarity voltages.

In a typical dual slope ADC, the voltage at the noninverting input of the integrator is at 0V. This voltage controls whether the output will ramp either up or down. For a normal dual slope structure, if the voltage at the input is below zero, the output will ramp up due to the inverting feedback and vice versa if the input is above zero. It is also generally set in the middle of the input voltage range so that the max ramp up and down can be achieved. Owing to this convention, the voltage at the noninverting input of the integrator is set to mid-rail for this design, which equates to 600mV. This allows the integrator to be able to ramp up or down with respect to mid-rail. The following equations demonstrate the polarity of the current and how it is dependent on the voltage applied. I_{in} is the current traveling through the resistor and I_f is the current through the capacitor.

$$I_{in} = \frac{V_{in} - V_{noninverting}}{R} \tag{3.4}$$

$$I_f = C\frac{d(V_{noninverting} - V_{out})}{dt} \tag{3.5}$$

$$I_{in} = I_f \tag{3.6}$$

If the voltage is below mid-rail, the voltage will ramp up and vice versa if it is above mid-rail. With this principle, a mid-rail dual slope ADC can be realized. Figure 3.5 demonstrates how the integrator functions with an input below and above mid-rail.

A problem lies within the need for a changing reference voltage for the dual-slope ADC. For instance, if the input voltage is above mid-rail, the integrator will ramp down. To have the reference voltage ramp up, a voltage below mid-rail is required. If the analog input voltage is below mid-rail, the integrator will ramp up and an input voltage above mid-

rail is required to have it ramp down. A comparator is implemented at the front of the data converter to decide if the signal is greater or less than mid-rail. Based on the decision, an analog multiplexer will choose the appropriate reference voltage for the second half of the cycle.

An advantage of the mid-rail dual slope ADC is that the conversion time is halved. Since only one side of the rail is dealt with when a conversion takes place, it can be realized with a N-1 counter and register. Figure 3.6 demonstrates the resolution of the ADC is split into both sides of the rail. As a result, the amount of digital circuitry is reduced and the conversion time is much faster than that of a typical dual slope ADC.

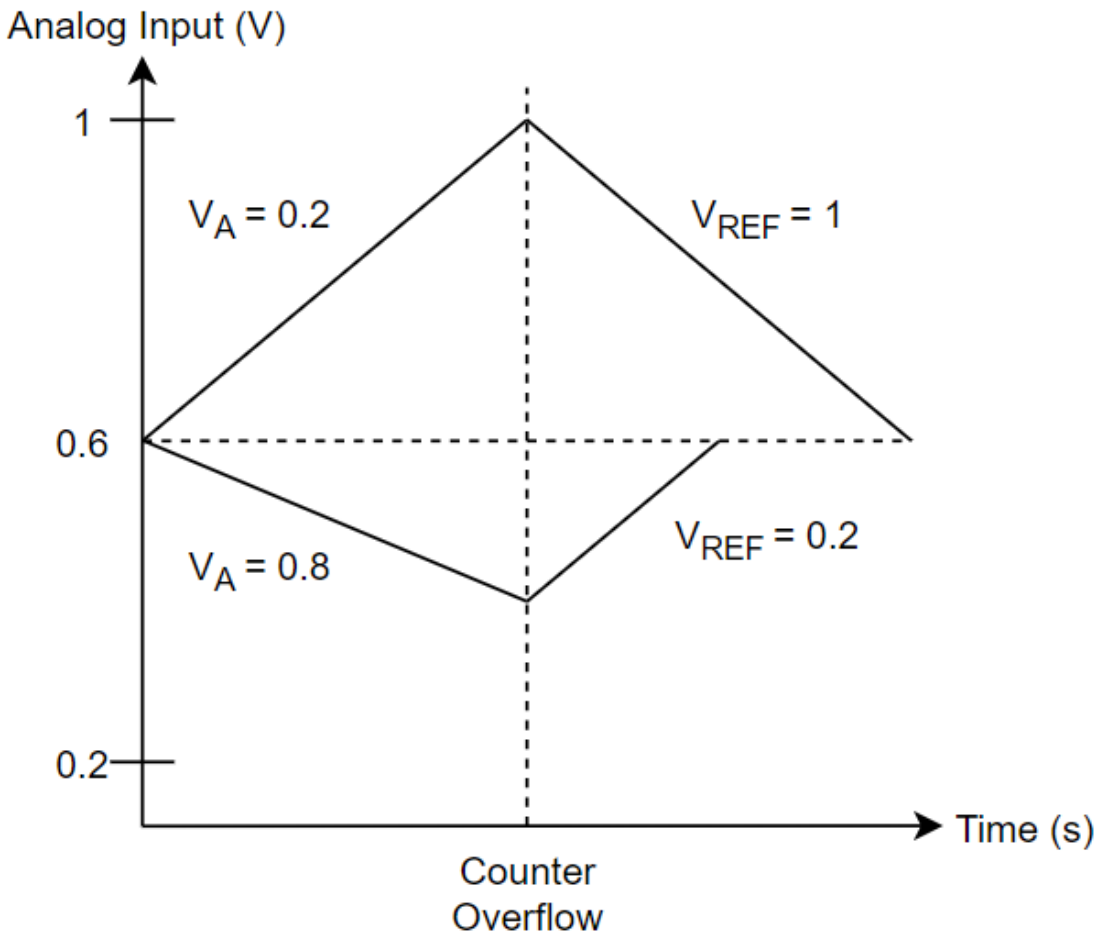


Figure 3.5 Demonstration of mid-rail methodology.

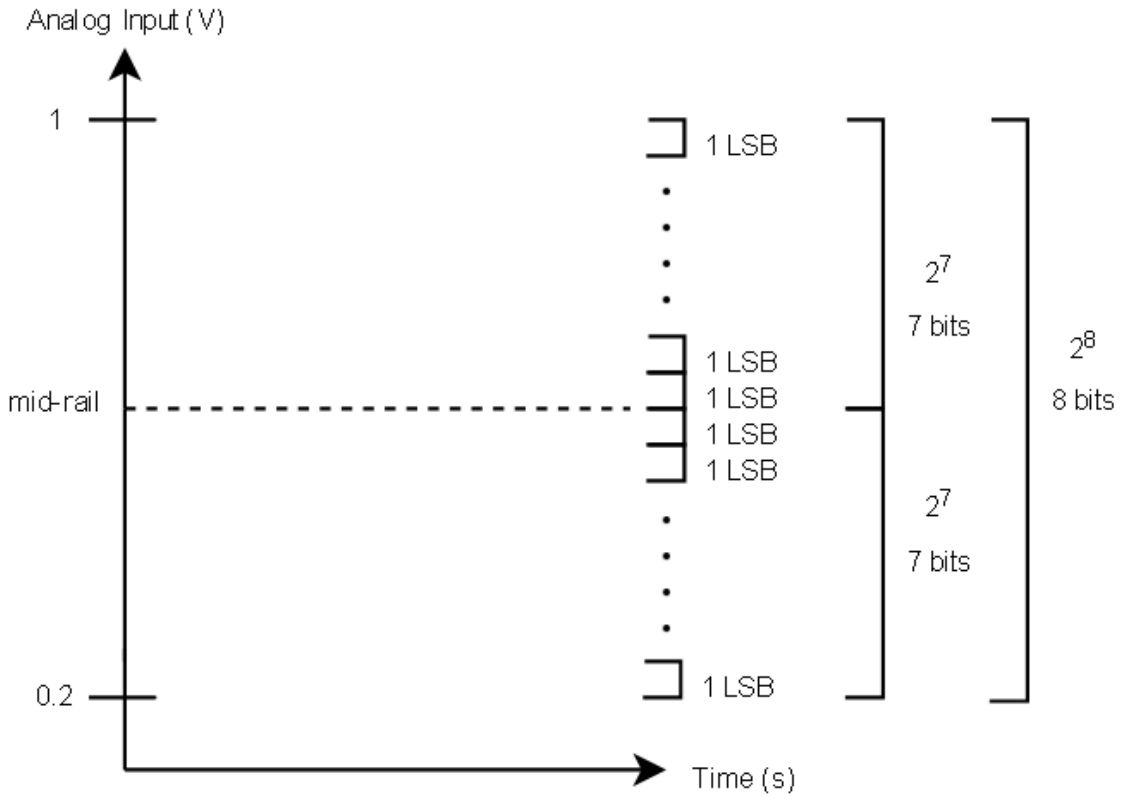


Figure 3.6 Resolution split into N-1 for each side of mid-rail.

3.4 System Overview

A dual slope ADC requires 2^{N+1} steps to complete a conversion, but with the mid-rail approach, only 2^N steps are required. With a clock frequency of 1 MHz, the conversion time is found by the following equation,

$$t_c = 2^N t_{CLK}. \tag{3.7}$$

The conversion time is found to be 256μs for an 8-bit ADC. The converter is sampled at the end of the conversion cycle, which is every 257μs and equates to a sampling frequency of 3891 Hz. An extra micro-second is added for the integrator needs to reset the voltage at its inverting input. Although this frequency may be overkill for this application, the data converter can be applied to a variety of other applications.

Given that the sampling frequency is very quick, it can be derived so that a sample-and-hold amplifier is not needed for this application. For this to be true, the signal at the input should change less than 1 LSB for the duration of the sampling time. This relationship can be modeled by equation 3.8. The maximum rate of change in a sine wave is $2\pi f_{in} A_{max}$. For the equations, it shall be assumed that the input into the analog-to-digital converter is a 4Hz sine wave since it is the fastest wave that the system will deal with.

$$T_s(2\pi A_{max} f_{in}) < 1\ LSB \tag{3.8}$$

1 LSB for the system is found by the equation,

$$\frac{Full\ Scale\ Input\ Range}{2^N} = \frac{(1-0.2)}{2^8} = 3.125\ mV \tag{3.9}$$

Plugging all the values into the equation, we can derive the needed sampling period so that a sample and hold is not needed. This can be seen by equations 3.10 and 3.11,

$$\left(\frac{1}{f_s}\right)(2\pi)(0.8)(0.4) < 3.125\,mV \tag{3.10}$$

$$f_s > 644\,Hz\,. \tag{3.11}$$

The sampling rate implemented meets this requirement, thus a SHA will not be constructed for the system.

Figure 3.7 displays the block diagram of the mid-rail dual slope analog-to-digital converter. The input analog signal is fed into the decision comparator at the front of the ADC, which will decide if the signal is greater or less than 600mV. The signal will then be input into the integrator and it will either ramp up or down. When the 7-bit counter overflows, the input of the integrator is switched to the reference voltage. The output of the integrator ramps toward mid-rail. Once it passes 600mV, a comparator will shut off the counter and the register, holding on to the output.

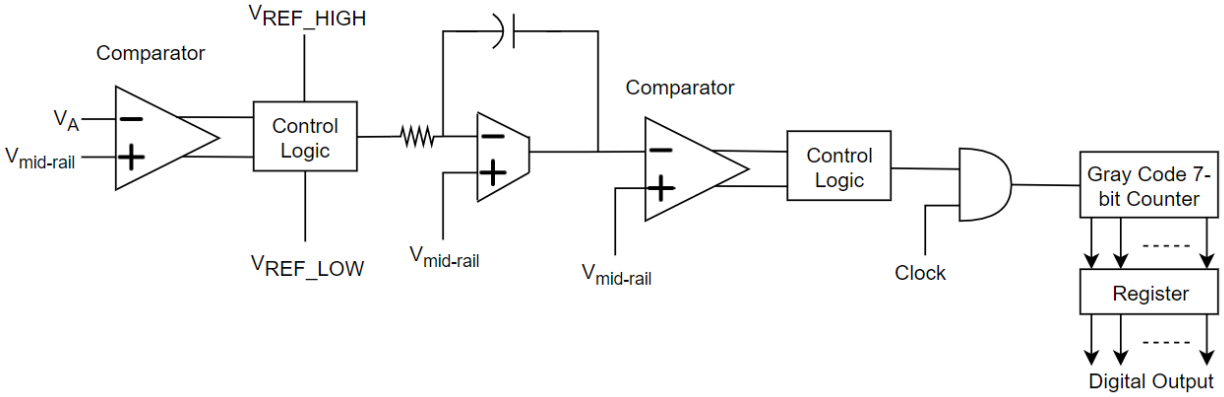


Figure 3.7 Overview of the mid-rail dual slope ADC.

3.4.1 Mid-Rail Method Design Adjustments

Since the conversion time is reduced in half and the reference for integration is at mid-rail, the principal equations for a dual-slope ADC no longer hold. One conversion for a mid-rail ADC requires $2^N T_{CLK}$ cycles, meaning that the first half integration lasts approximately $2^{N-1} T_{CLK}$ cycles owing to a $N-1$ counter being implemented. The output value of the integrator at the end of the first integration period is found by,

$$V_{o1} = -\frac{1}{RC}\int_0^t (V_{in} - V_+)dt + V_+ \tag{3.12}$$

The output of the integrator at the end of the second integration period when V_{REF} is connected is represented by,

$$V_{02} = V_{Mid-Rail} \pm V_{o1} \tag{3.13}$$

If the input into the system is above mid-rail, the V_{o1} term is to be added, and vice versa if the input is below mid-rail. Next, a relationship is found between the values of the V_{IN} and V_{REF} to T_1 and T_2. For a traditional dual slope ADC, the input voltage is a percentage of the reference voltage. For a mid-rail ADC, the principle is the same, but both reference voltages need to be accounted for. First, the input voltage is normalized by subtracting the bottom reference voltage. Next, the reference voltage is normalized by taking the difference between the top and bottom reference voltages. Equation 3.14 is then derived as the relationship between the input voltage and the reference voltage.

$$\frac{|V_{IN} - V_{REF_BOT}|}{|V_{REF_TOP} - V_{REF_BOT}|} = \frac{T_1}{T_2} \tag{3.14}$$

3.5 Integrator

Provided that the conversion time is 256μs, the first half of the conversion will take 128μs for that is when the 7-bit counter will overflow and start counting again. In order to ease the design complexity, the output range of the integrator will match the input voltage range, 0.2 – 1V, of the ADC so that the resolution on the comparator is relaxed. The integrator requires an RC time constant of 128μs to have this happen. A resistor value of 12.8MOhms and a capacitor value of 10pF are chosen. The large resistor will result in a smaller current flowing into the capacitor, effectively decreasing the power. Although, it may be somewhat area inefficient, it has a few other advantages. Before the integration takes place in each cycle, a switch is in parallel with the capacitor and it is closed to reset the inverting input to match the voltage at the noninverting input. During this time, the capacitor must be charged to the mid-rail voltage. If a larger capacitor is used, it will take longer to be reset to the mid-rail voltage, decreasing the conversion time. In addition, the bias current of the operational transconductance amplifier can be increased to compensate for this, but it comes at the cost of additional power consumption.

When the counter overflows at the end of the first half of the cycle, the switch at the input of the integrator is changed to V_{REF}. Depending on the front-end comparator, the reference voltage will be either 0.2 or 1 Volts. Figure 3.8 presents the architecture of the integrator.

3.5.1 Operational Transimpedance Amplifier (OTA)

Design

The OTA employed should have the following specifications specified in Table 3.2. It should have a high gain to keep the inverting voltage linear as it integrates over time. A folded cascode topology has been selected to meet these requirements. The general structure of the amplifier can be found in Figure 3.9. The transistors were sized in weak to moderate inversion to maximize transconductance (g_m) efficiency of the amplifier. The input pair, M_1 and M_2 are chosen to be PMOS transistors to decrease flicker noise and maximize slew rate and unity gain frequency. Although NMOS transistors may have a higher transconductance it is not critical for the application.

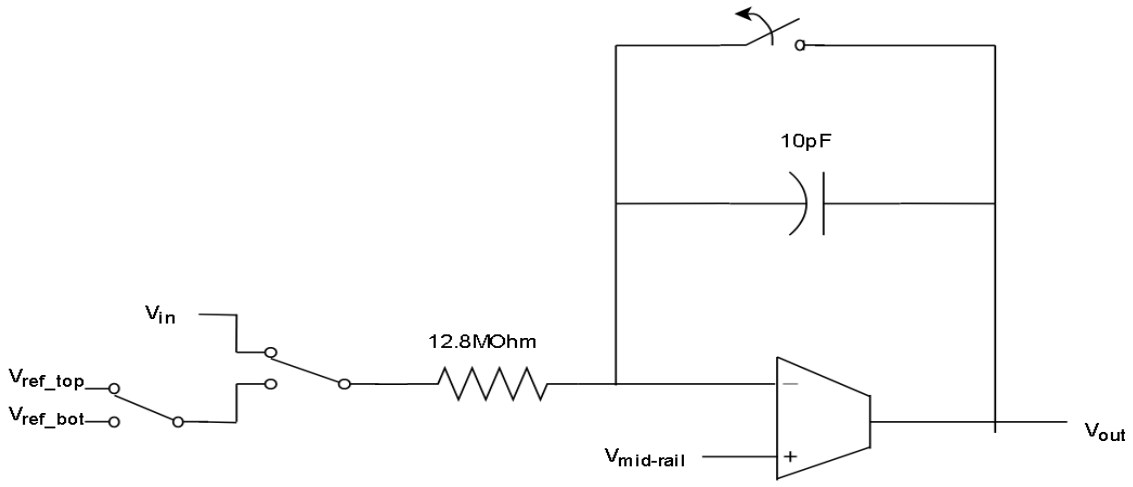


Figure 3.8 Schematic of the integrator architecture.

Table 3.2 OTA Specifications

Specifications	**Values**
Input Range	0.2 – 1 Volts
Output Range	0.2 – 1 Volts
Power	≤ 15 μW

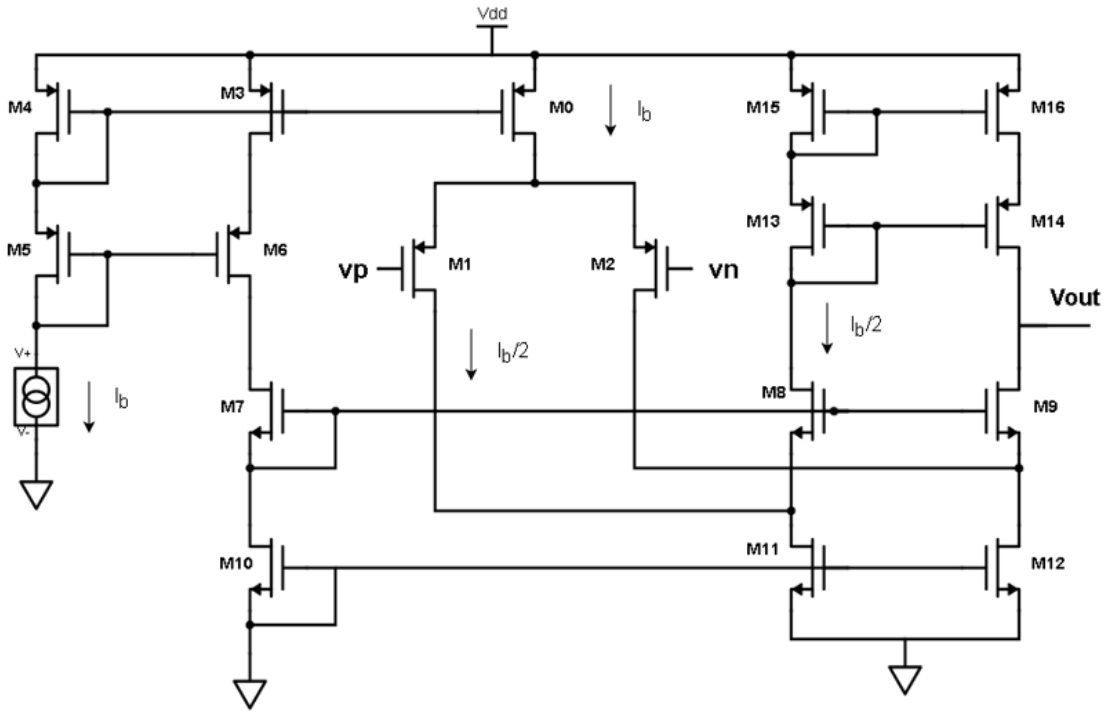


Figure 3.9 Circuit schematic of a folded cascode PMOS OTA.

When it comes to sizing the transistors, the inversion coefficient (IC) method was utilized. The method uses level of inversion as a design variable. The coefficient can is defined as,

$$IC = \frac{I_D}{I_O(\frac{W}{L})} \tag{3.15}$$

I_O is defined as the technology current, which is a function of whichever process that is being employed to design with and can be expressed as,

$$I_o = 2n_o\mu_o C'_{ox}U_T^2 \tag{3.16}$$

The method functions by having three degrees of freedom, the drain current, the channel length, and the inversion level. By selecting these three variables, a width is derived for the transistor. Moreover, there are three regions of inversion, weak, moderate and strong. The level of the inversion primarily controls the transconductance efficiency of the transistor. Figure 3.10 demonstrates the inversion coefficient's relation to g_m efficiency [33].

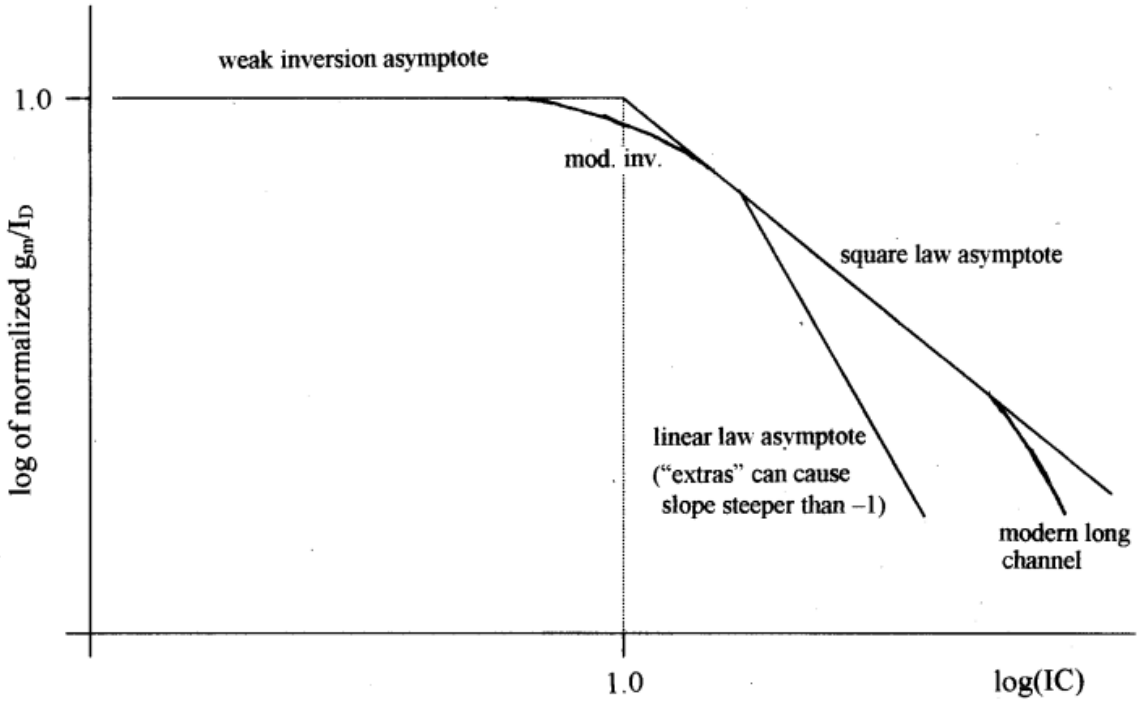


Figure 3.10 Level of impact of inversion on transconductance efficiency [33].

Weak inversion corresponds to an inversion coefficient of 0.1 and provides maximum transconductance efficiency and a low bandwidth. Moderate inversion corresponds to an IC of 1 and provides an optimal tradeoff between weak and strong inversion, giving moderate gain and bandwidth. Strong inversion provides the least gain, but the largest bandwidth. As the inversion coefficient increases, the device size decreases. Figure 3.11 illustrates the performance tradeoffs versus selected inversion coefficient and channel length [35].

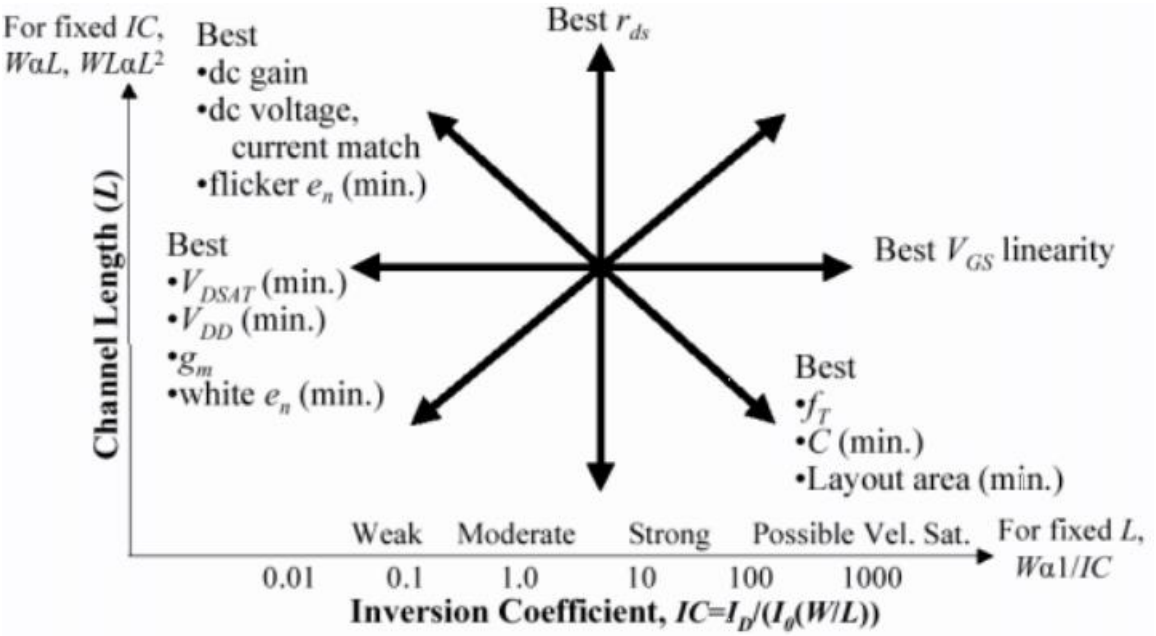


Figure 3.11 Tradeoffs for various selected inversion coefficients and channel lengths [34].

The overall transconductance (G_M) of the folded cascode amplifier can be expressed as,

$$G_M = g_{m1,2} = \frac{I_D}{nV_T} \tag{3.17}$$

I_D is the drain current of the input pair, n is the body effect factor, and V_T is the thermal voltage. n ~ 1.3 in the weak inversion region. The currents from the differential pair are folded into the cascode stages at the output, hence the name. Due to the current mirrors being cascoded at the output, the voltage gain is greatly increased due to the increased output resistance. The gain for the OTA can be found as,

$$A_v = \frac{v_{out}}{v_p - v_m} = g_m(R_{ocasn} || R_{ocasp}) = \frac{g_m^2 r_o^2}{2} \tag{3.18}$$

With the increase in the gain the bandwidth must decrease. The dominant pole of the amplifier is expressed as,

$$f_p = \frac{1}{2\pi(R_{ocasn} || R_{ocasp})C_L} \tag{3.19}$$

The differential pair M_1 and M_2 are sized for weak inversion to provide a high gain. Each MOSFET will carry a current of $\frac{I_B}{2}$. A channel length of 1 µm is used to prevent short channel effects and decrease DC mismatch. The input pair was also given a larger shape factor to decrease the input offset. The transistors M_0 and M_3 - M_6 are sized for moderate inversion with a long channel length so that current matching is superb and they attribute less noise to the overall circuit. Transistors M_{10} – M_{12} are sized for weak inversion owing to the requirement of a high output swing and high input common mode range. The V_{DSAT} of the transistors decreases as the inversion coefficient decreases, resulting in larger widths.

M_8 and M_9 are biased at $\frac{I_B}{2}$ since half of the total bias current is taken from each branch to the differential pair at the input. M_7 on the other hand is biased at I_B. All three NMOS transistors are placed in weak inversion to increase the output swing. M_{13} – M_{16} are

sized in weak inversion as well to increase the bottom part of the output swing range. Table 3.3 exhibits the operating conditions of each transistor within the folded cascode amplifier.

A bias current of 3µA is chosen so that the integration capacitor can be reset quickly. Additionally, the slew rate is improved for the amplifier. When the 1st integration phase is over, the voltage at the input of the OTA will change from the unknown analog input voltage to a reference voltage of either 0.2 or 1 Volts, causing a step response. Due to the linear nature of the integrator, it is necessary to be able to respond quickly and accurately to this occurrence.

Table 3.3 Operating Conditions of Transistors in Folded Cascode Amplifier

Transistor	$\frac{\boldsymbol{W}\ (\boldsymbol{\mu m})}{\boldsymbol{L}\ (\boldsymbol{\mu m})}$	**I_D (µA)**	**IC**
M_0 and M_3- M_6	16/2	3	2.038
$M_1 – M_2$	32/1	1.5	0.254
M_7	10/1	3	0.185
$M_8 – M_9$	10/1	1.5	0.093
$M_{10} – M_{12}$	10/0.5	3	0.093
$M_{13} – M_{16}$	40/0.5	1.5	0.102

Results

A high gain transconductance amplifier has been realized with a folded cascode structure. It has been tested with a 10 pF load capacitance for that will be what will drive when configured as an integrator. Performance metrics of the OTA can be observed in table

3.4. Figure 3.12 shows the open loop gain response and Figure 3.13 displays the noise spectrum of the OTA. Due to the very high load capacitance, the resulting noise is minimal and a low flicker noise corner is achieved.

Table 3.4 OTA Performance Metrics

Performance Metrics	**Values**
Bias Current	3 µA
Load Capacitance	10 pF
Bandwidth	385.6 Hz
Phase Margin	87.94°
Unity Gain Bandwidth	602.4 kHz
Open Loop Gain	63.86 dB
CMRR	98.84 dB
Input Common Mode Range	0.08 – 1.01 V
Output Swing	0.19 – 1.02 V
Slew Rate	269 mV/µs
Power	14.5 µW
Input Referred Noise	44.11 µV
Flicker Noise Corner	371.5 kHz

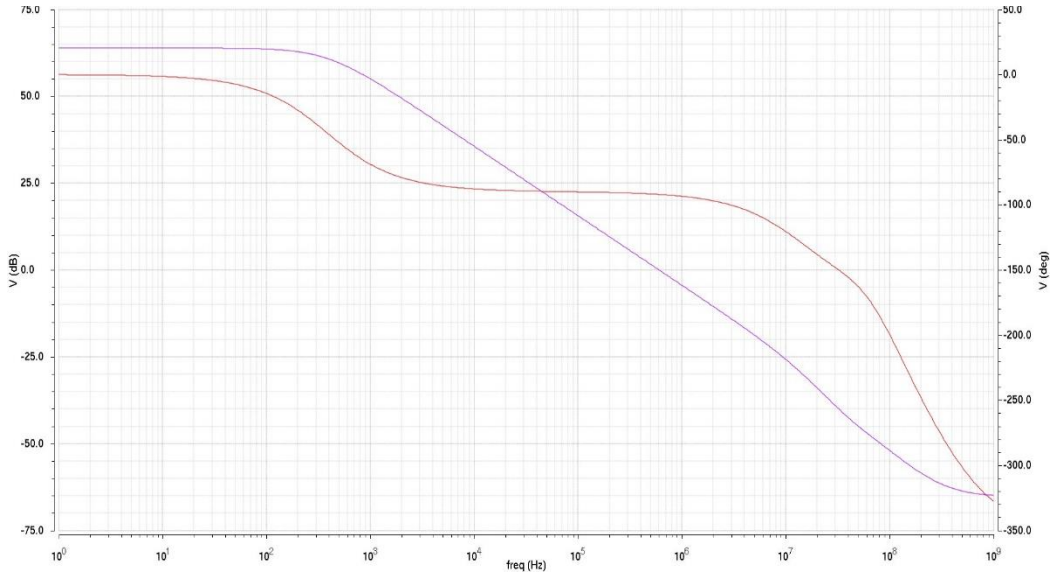


Figure 3.12 Open loop response of the OTA.

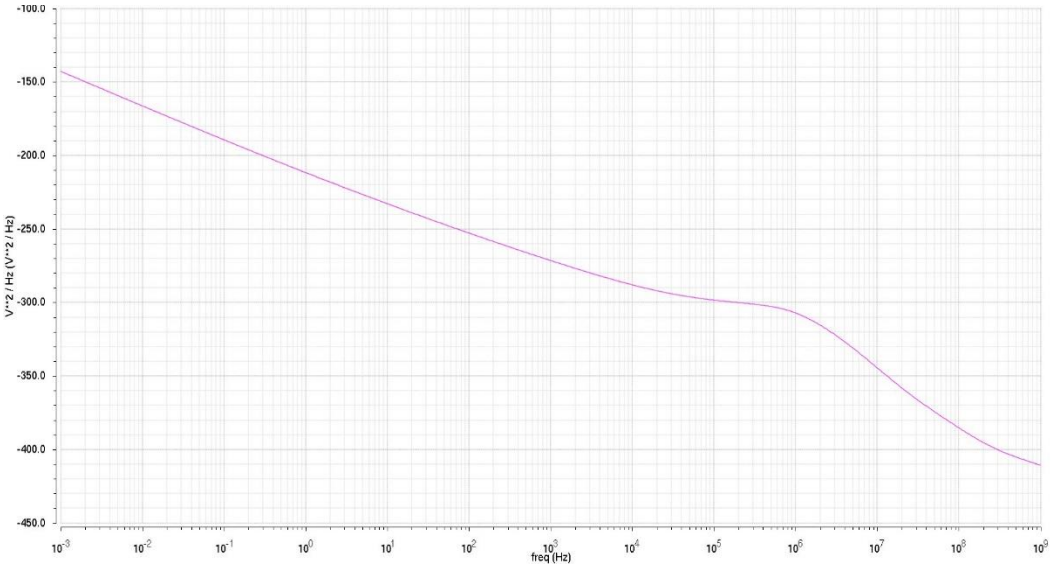


Figure 3.13 Noise spectrum of the OTA.

3.5.2 Charge Injection

Given that the mid-rail topology requires a few switches for few tasks such as switching the input voltage to the reference voltage, choosing the correct reference voltage, and feeding the correct comparator output to the next components. All this switching comes with consequence of charge injection, which greatly affects the linearity of the integrator. Charge injection can be described as the charge dumped out of a transistor when it is turned off. Half of the charge flows out of the source and the other half out of the drain. Figure 3.14 shows an NMOS transistor exhibiting charge injection [23]. The dump of charge will cause the output voltage to jump. Since the integrator is a highly linear component, the extra voltage resulting from the charge injection degrades its accuracy.

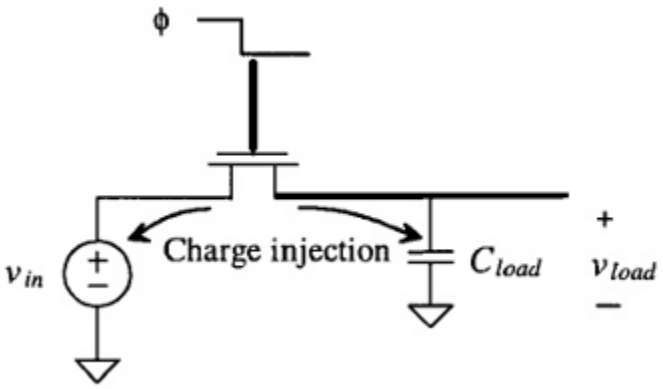


Figure 3.14 NMOS switch exhibiting charge injection [24].

Throughout the design, analog multiplexers built with transmission gates function as the controlling switches. One fix for the charge injection issue is to implement dummy transistors on each side of the transmission gate. The NMOS dummy transistors turn on

when the NMOS transistor within the transmission gate turns off and the PMOS dummy transistors turn on when the PMOS transistor within the transmission gate turns off. Due to this, the charge dumped out of the transmission gate transistors can be cancelled out with the charge flowing out from the dummy switches. The dummy transistors are sized at half the size of the transmission gate transistors because only half the charge is dumped in each direction. Figure 3.15 demonstrates this phenomenon for a transmission gate.

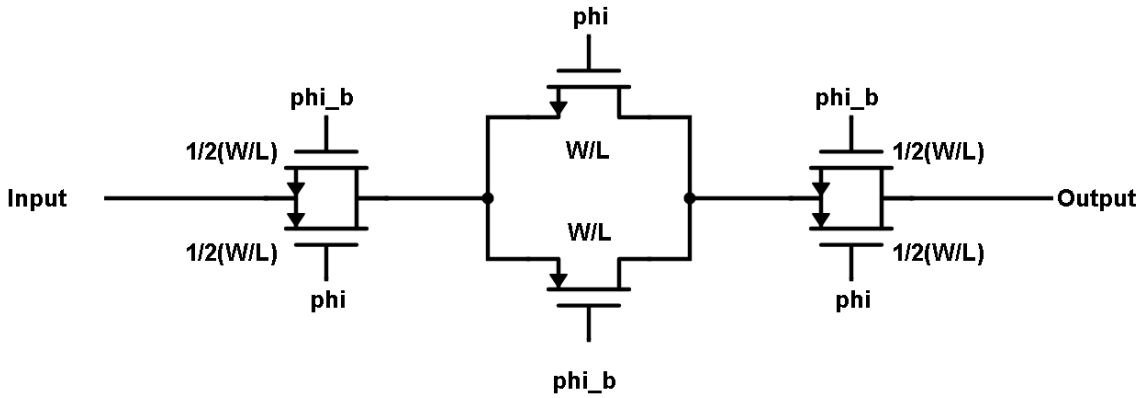


Figure 3.15 Schematic of the transmission gate charge injection compensation method.

Another remedy for charge injection is to precisely control the switching signals on the transmission gate. A transmission gate already counteracts charge injection because the complementary signals that are used will cancel out each other, but there is a need for precise control of these signals. To achieve this, a pseudo-differential switch driver is applied, as seen in Figure 3.16 [35]. The driver takes a digital input and creates perfectly overlapping digital outputs.

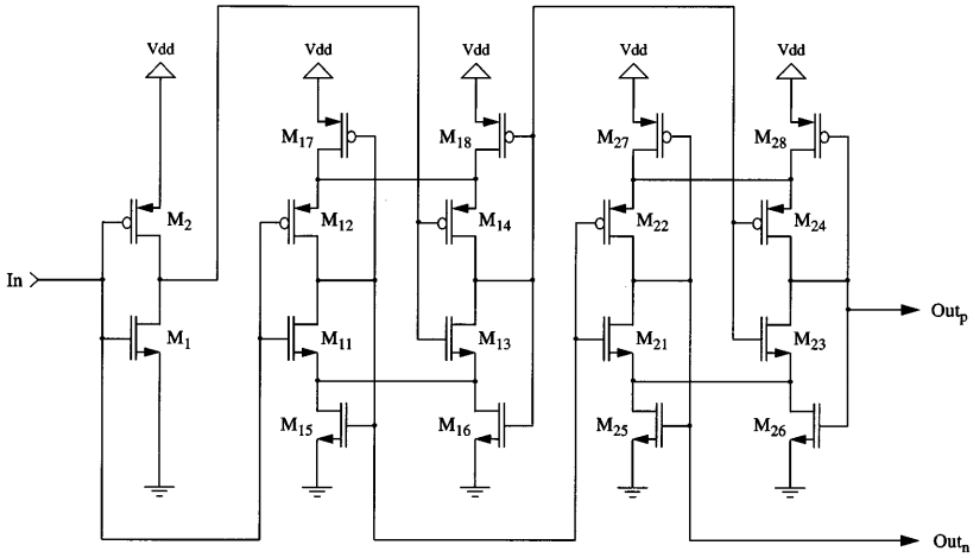


Figure 3.16 Circuit schematic of the pseudo-differential switch driver [35].

Lastly, the reference voltages were changed in order to increase the slope during the second phase of integration. The voltages were normalized to the largest digital output on each side of the rail. The new reference voltages can be found in table 3.5.

Table 3.5 Adjusted Reference Voltages for Charge Injection

Original Reference Voltages	Adjusted Reference Voltages
0.2 V	0.193 V
1 V	1.13 V

3.5.3 Results

The integrator was first swept with a series of low input voltages resulting in the integration upwards in the first phase and downward for the second phase. With the input voltage low, the reference voltage is set to 1 Volt. Next, the integrator was swept with a series of high input voltages to simulate the other side of mid-rail. The reference voltage for these inputs was set to 0.2 Volt as it needs to integrate back towards mid-rail in the second phase. The results are presented in Figure 3.17 and Figure 3.18. The final layout of the integrator is shown in Figure 3.19.

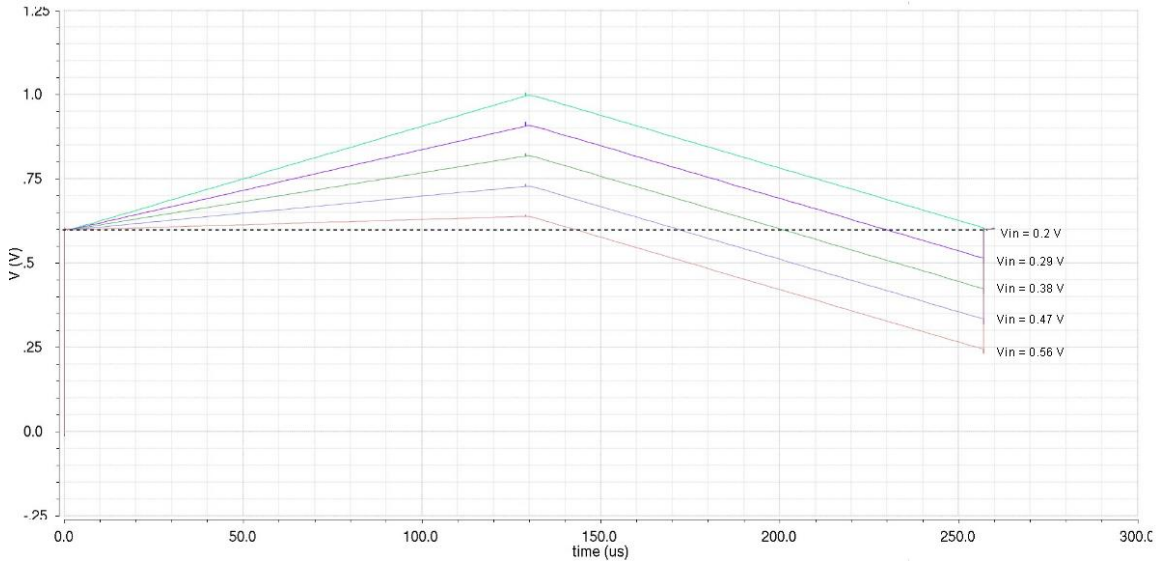


Figure 3.17 Integrator performance with input voltages below mid-rail.

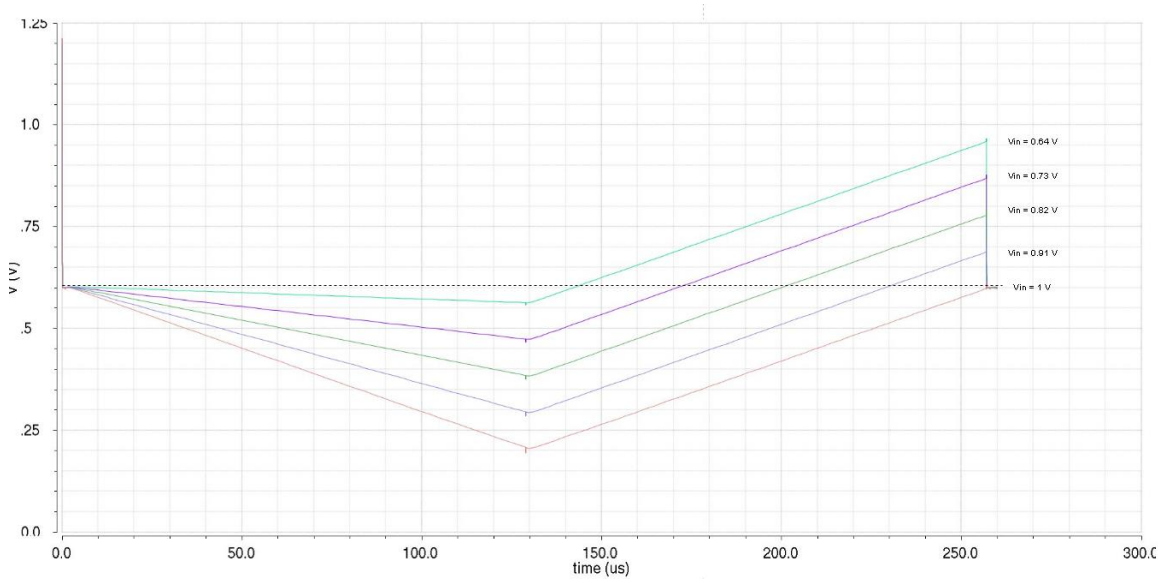


Figure 3.18 Integrator performance with input voltages above mid-rail.

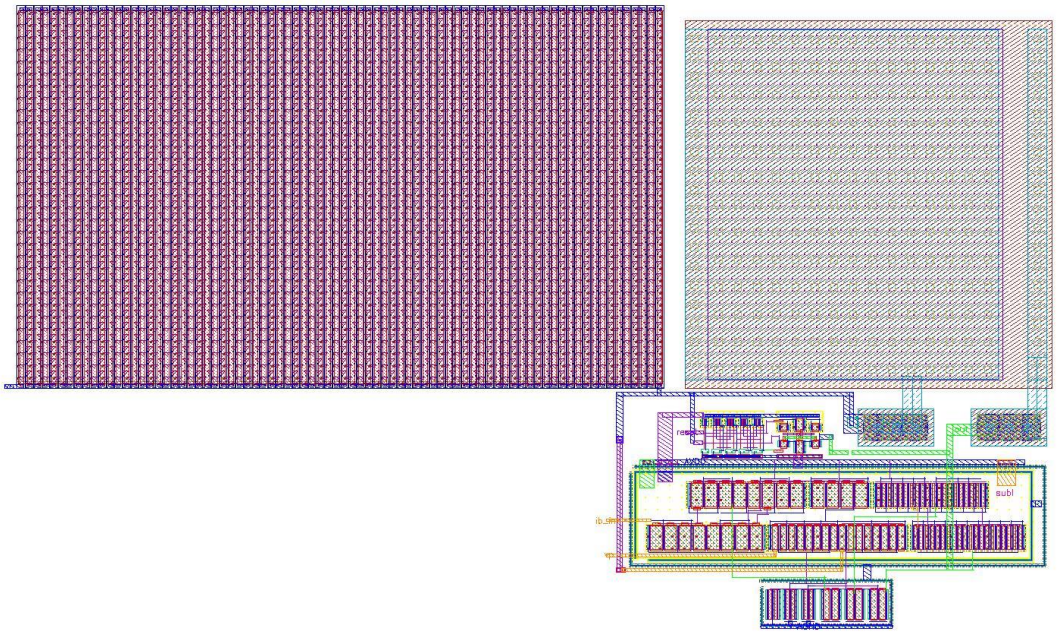


Figure 3.19 Layout of the integrator.

3.6 Comparator

There are two comparators employed in the ADC design. The comparator at the front of the ADC analyzes the incoming unknown analog voltage and decides whether it is more or less than mid-rail, 600 mV. The second comparator is placed after the integrator. Its noninverting input is set at mid-rail and will shut off when the integrator output voltage crosses 600 mV in the 2nd phase of integration.



Figure 3.20 Block diagram of the comparator.

The designed comparator was chosen to be a three-stage dynamic latch topology. This type of comparator is capable of high speed and resolution. Figure 3.20 displays the block diagram of the designed comparator. The latch and the output buffer consume only dynamic power while the preamp consumes static power. The preamplifier is applied to obtain a higher resolution and minimize the effects of kickback noise. Kickback noise can be described as the charge transfer in or out of the inputs as the latch stage switches from latch mode to track mode, which will be discussed shortly. The objective of the preamplifier is to amplify the signal so that the latch stage can more easily distinguish the difference between the incoming signals. It can also be used as a unity gain buffer if speed

is more important. Without a preamplifier, kickback noise can cause very large glitches. The latch stage performs a comparison each time the clock is high and resets when the clock is low. It typically has a high gain and functions somewhat like an open loop amplifier. The signals from the preamplifier are further amplified until the voltage is a full-scale digital signal. If the voltage at the inverting input is greater than the voltage at the noninverting input, the output of the latch is a logic '1'. Contrarily, it will resemble the clock signal if it is less. The output buffer provides capacitive isolation for the first two stages and converts the latch output signals into a logic '1' or logic '0' for both outputs independent of the clock signal.

The comparator should be low power and should be able to decipher a voltage difference equivalent to 1 LSB. Table 3.6 presents the design specifications for the comparator.

Table 3.6 Design Specifications for Comparator

Design Specifications	**Values**
Resolution	< 1 LSB = 3.125 mV
Power	≤ 15 μW
Clock Frequency	1 MHz

3.6.1 Preamplifier

A simple six transistor fully differential topology was chosen for the topology of the preamplifier. The architecture is shown in Figure 3.21. A high speed low gain design

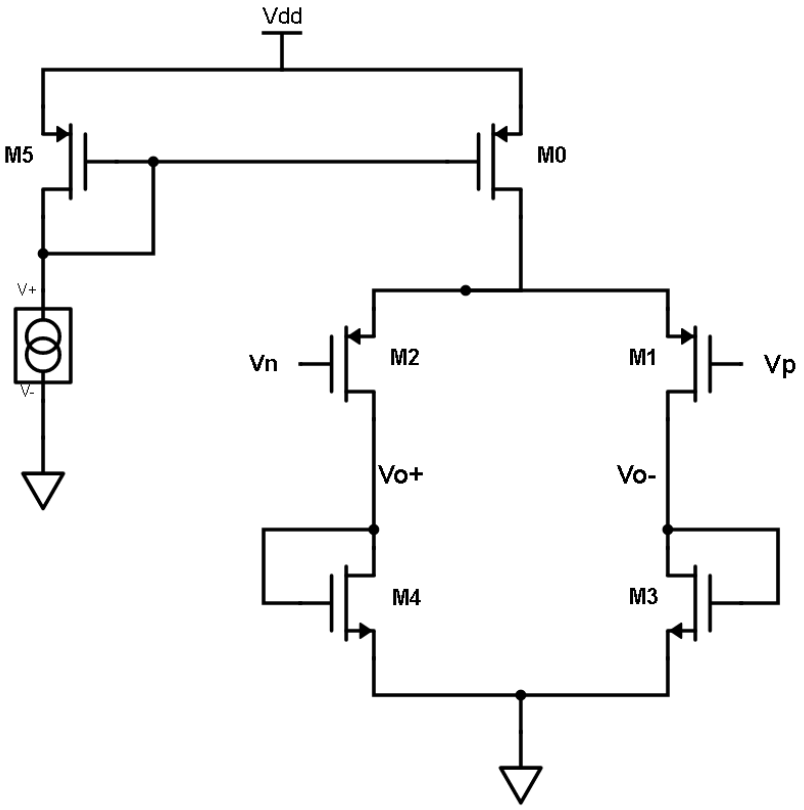


Figure 3.21 Schematic of the preamplifier structure.

is needed, hence the simple structure. The speed can be crucial for the preamplifier, since if it were too low, it would limit the decision time of the latch. Diode connected NMOS transistors are used as the load transistors to increase bandwidth, but they also decrease g_m. The gain of the amplifier can be expressed as,

$$A_v = g_{m_{1,2}}(r_{o2} || \frac{1}{g_{m_4}}) \cong \frac{g_{m_{1,2}}}{g_{m_{3,4}}} \tag{3.20}$$

The output resistance of the diode connected transistors M_3 and M_4 is $1/g_{m_3}$ and $1/g_{m_4}$ respectively. This in turn increases the bandwidth, but the gain drops. The bandwidth of the amplifier can be approximated as,

$$f_p = \frac{1}{2\pi(\frac{1}{g_{m_{3,4}}} || r_{o_{1,2}})C_L} \cong \frac{g_{m3,4}}{2\pi C_L} \tag{3.21}$$

Given that the comparators need to be accurate at mid-rail, the input common mode range design requirements are very relaxed.

The transistors in this stage were designed with the inversion coefficient methodology. The biasing current mirror is placed in strong inversion with a long channel to copy the current correctly since only a single mirror and not a cascoded mirror is implemented. The input pair is set in moderate inversion to provide a moderate gain. Although, the gain is not just set by the input pair for this configuration since it is limited by the g_m of the load transistors. The load transistors are sized for moderate inversion to provide an optimal tradeoff between gain and bandwidth. The sizes of the transistors are presented in Table 3.7.

Table 3.7 Operating Conditions of MOSFETs in Preamplifier

Transistor	$\frac{\boldsymbol{W}\ (\boldsymbol{\mu m})}{\boldsymbol{L}\ (\boldsymbol{\mu m})}$	**I_D (µA)**	**IC**
M_0 and M_5	12/4	5	9.06
$M_1 – M_2$	20/0.5	2.5	0.34
$M_3 – M_4$	3/1	2.5	0.514

3.6.2 Latch

The latch circuit is known as the decision circuit for making the decision of which voltage is greater or less than the other and act on it. The structure can be observed in Figure 3.22. Positive feedback is implemented in the cross-gate connection of M_8 and M_7. If $V_p > V_n$ at the input, the current i_{op} at the output node V_{op} is increased. This turns on M_8 for the gate to source voltage (V_{gs}) is raised. The drain to source voltage of M_8 is then lowered, turning off transistor M_7. Another form of positive feedback is seen where the output nodes connect back to the gate of transistors M_2 and M_3.

The gain of this circuit should not be very large as it will create too large of time constants, thus limiting the speed of the comparator. Another important factor in the design of the comparator is whether their memory is transferred from one decision cycle to the next, which is also known as hysteresis. To eliminate this, M_6 and M_9 create a reset path from the output nodes to the supply voltage. Then when the clock goes high, a new comparison is made each cycle.

Due to the dynamic latch structure, the inversion coefficient procedure was not used to size the transistors. Sizing the transistors in the latch is a tradeoff between the mismatch and speed. To increase the speed of the decision time, short channel lengths were employed. The widths were sized in favor of increasing gate area and decreasing offset. The cross coupled PMOS transistors were sized larger in favor of copying the current. The properties of the latch transistors are represented in Table 3.8.

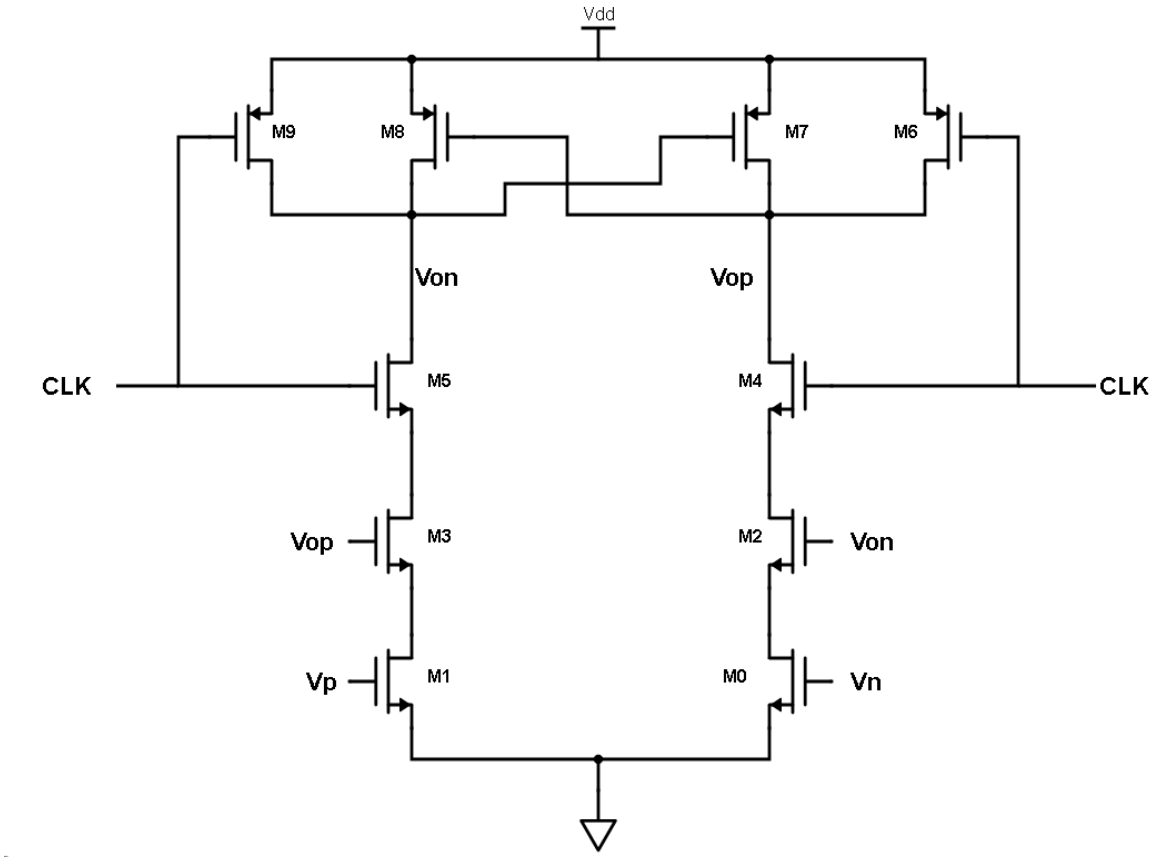


Figure 3.22 Schematic of the decision circuit.

Table 3.8 Operating Conditions of MOSFETs in Latch

Transistor	$\frac{\boldsymbol{W}\ (\boldsymbol{\mu m})}{\boldsymbol{L}\ (\boldsymbol{\mu m})}$
M_0 - M_5	3/0.3
M_6 and M_9	2/1
M_7 – M_8	1/3

3.6.3 Output Buffer

The main goal of the output buffer is to generate a full scale digital signal that is not reliant on the clock signal, as the latch stage does. To accomplish this, a cross-coupled NAND gate configuration is employed, as seen in Figure 3.23.

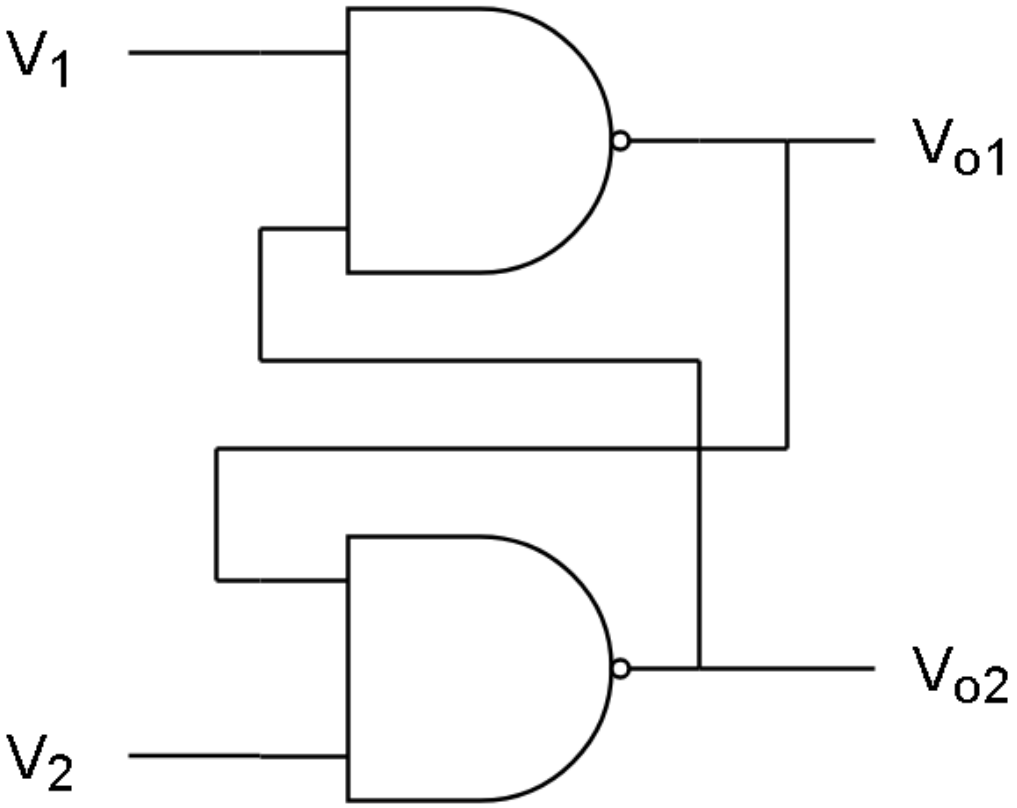


Figure 3.23 Schematic of the output buffer.

3.6.3 Results

To test the comparator, the inverting input is given a sine wave and the noninverting input is held at mid-rail. Once the voltage at the inverting terminal crosses mid-rail, the comparator should flip states. If $V_n > V_p$, the comparator output should be a logic '1' and vice versa if $V_p < V_n$. Figure 3.24 presents the functionality verification of the designed comparator.

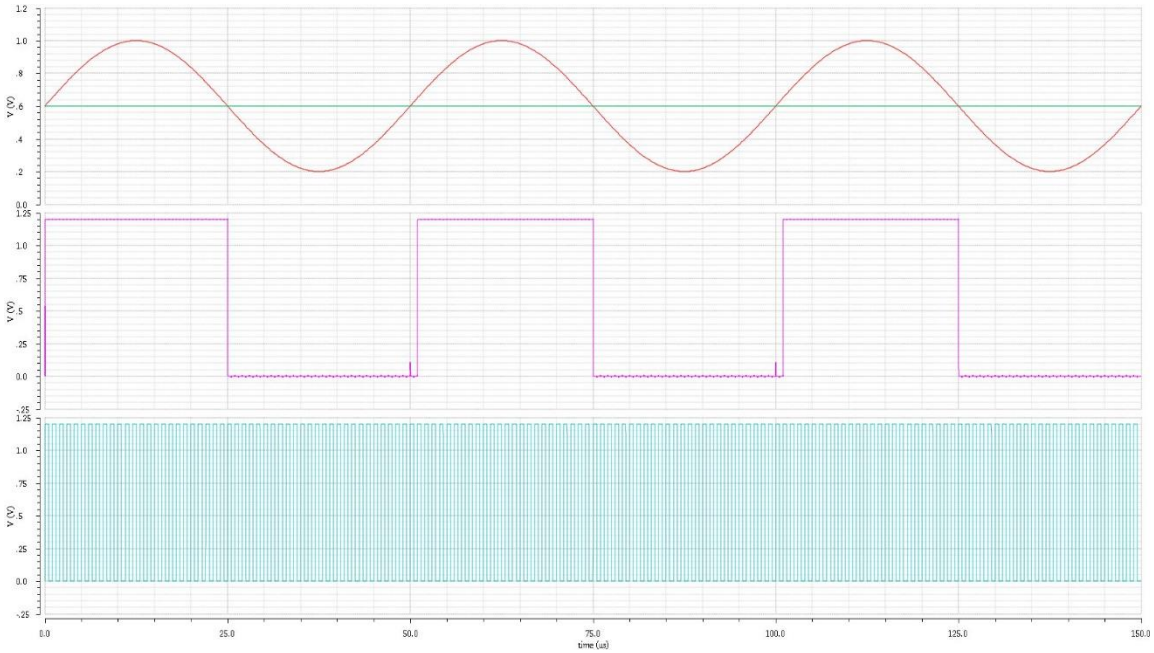


Figure 3.24 Functional verification of the comparator.

For characterizing the comparator, the resolution needs to be found, or in other words, the smallest voltage difference required for the comparator to change states. The resolution desired for the ADC is ½ LSB, which is also equivalent to 9 bits. The exact voltage required is found by,

$$Resolution\ Required = 1\ LSB = \frac{FSR}{2^N} = \frac{0.8}{256} = 3.125\ mV \quad (3.22)$$

Resolution is the combination of the influence of noise and offset. The offset is found as the difference between the voltage of the input that is changing and the mid-rail voltage when the comparator flips states. Offset relies on the varying mismatch between the transistors, which can be simulated by a Monte Carlo Analysis. The offset results in a sigma delta of 731.62 µV.

The noise of the comparator is discovered through means of a transient noise analysis. A known small offset of a 100 µV is applied forcing the V_{o1} output to go low. 1000 transitions were tested to determine if the mismatch of the transistors would cause the comparator to flip states. The testing configuration is found in Figure 3.25 and the resulting transient output is presented in Figure 3.26. From these results, a histogram is plotted with 2 bits, meaning the number of times either a logic '1' or logic '0' resulted, which is shown in Figure 3.27. The resulting probability of a logic '1' in this case is found and normalized to a standard deviation scale, represented by the following equation,

$$Probability\ of\ 1s = 0.244 \quad (3.23)$$

The normalized standard deviation is then determined to be equivalent to 0.693. The standard deviation can then be established with the following equations,

$$Standard\ Deviation = \frac{1}{normalized\ value} * offset\ implemented \quad (3.24)$$

$$Standard\ Deviation = \frac{1}{0.693} * 100\mu V = 144.3\ \mu V_{rms} \quad (3.25)$$

Now that the noise and offset have been determined, the resolution can be represented as,

$$Resolution = 2\sqrt{Offset^2 + Noise^2} \quad (3.26)$$

$$Resolution = 2\sqrt{(731.62\mu V)^2 + (144.3\mu V)^2} = 1.491\,mV \approx 9\,bits \quad (3.27)$$

The resolution has met the specification and is able to decipher voltages within a ½ LSB. Table 3.9 presents the performance metrics of the comparator. The final layout of the comparator can be found in Figure 3.28.

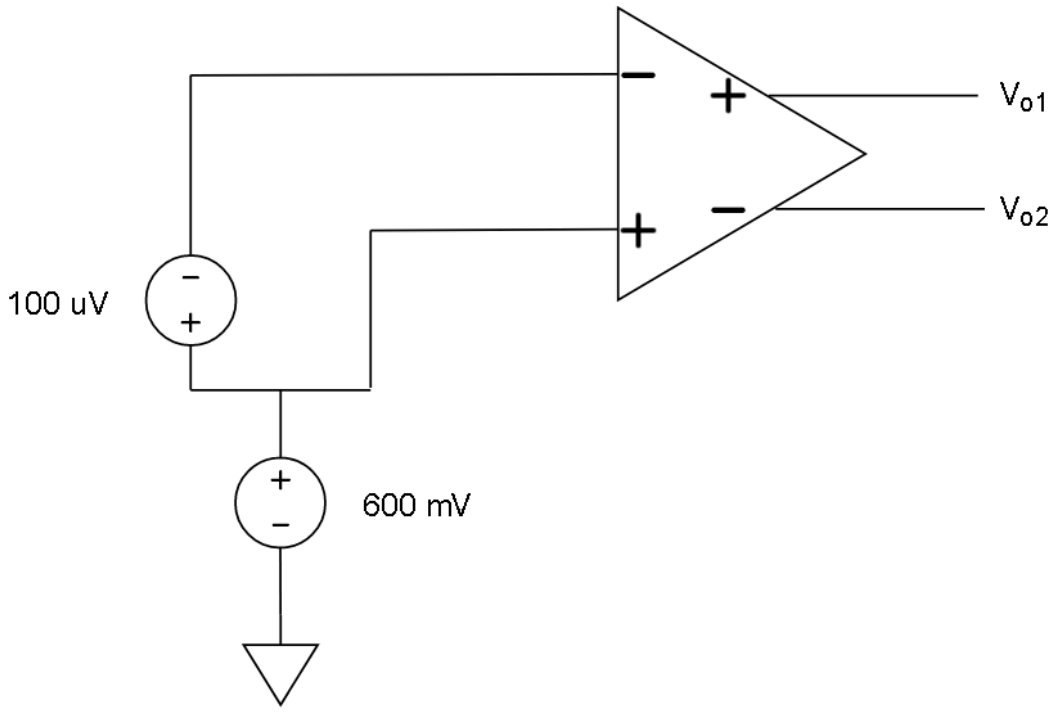


Figure 3.25 Noise testing configuration of the comparator.

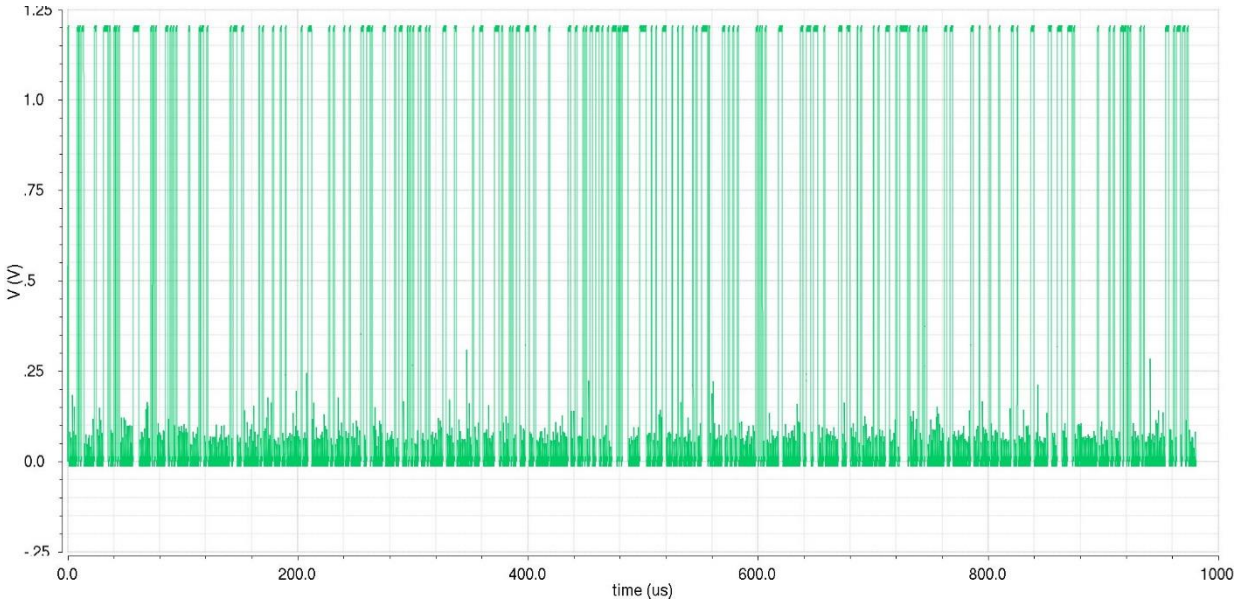


Figure 3.26 Transient output of noise analysis.

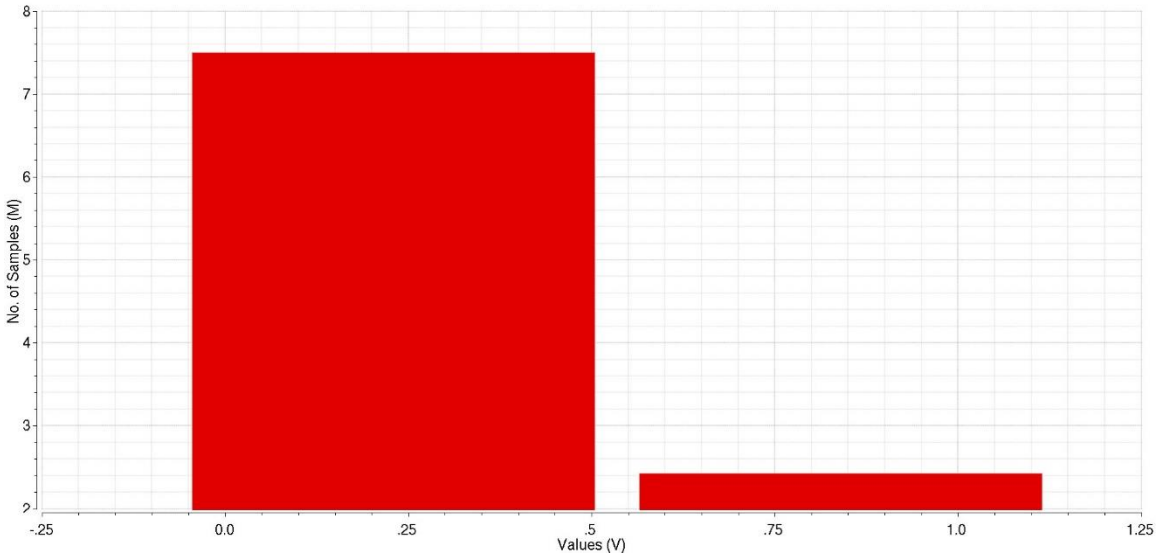


Figure 3.27 Histogram of the noise analysis.

Table 3.9 Comparator Performance Metrics

Performance Metrics	**Values**
Power Consumption	12.05 µW
Propagation Delay	38.35 ns
Noise	129.786 μV_{RMS}
Offset	731.62 µV
Resolution	9 bits

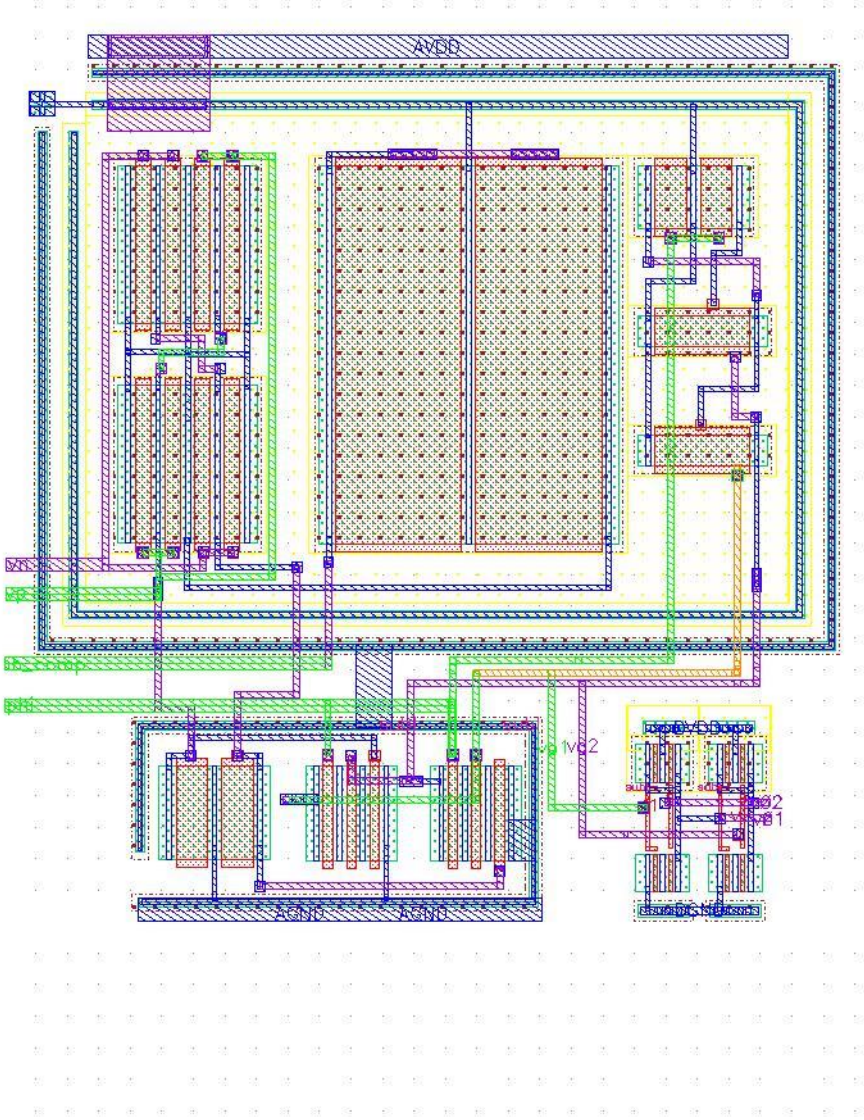


Figure 3.28 Layout of the comparator.

3.7 Counter

Provided that the mid-rail approach requires an N-1 counter, a 7-bit counter is required for the ADC to realize a total of 8 bits accuracy. For this step of the ADC, a Gray code counter is applied. Gray code behaves by only having one-bit change at a time and has many advantages over the ordinary binary code, including a reduced switching activity, decreased power consumption, less glitches and noise, and minimal error in the output code.

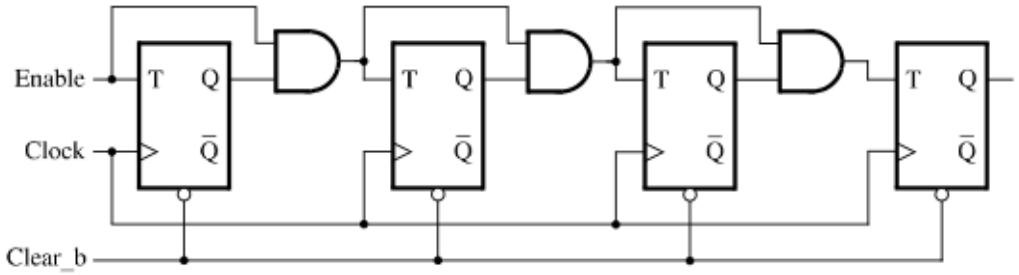


Figure 3.29 Schematic of a binary counter structure employing T flip flops [36].

The Gray code counter is constructed by a chain of master slave synchronous T flip flops, which can be observed in Figure 3.29 [36]. The master slave configuration is proven to be more reliable and stable. This kind of structure triggers on the negative edge, to counteract this for the ADC design, the clock is inverted when fed into the counter to produce a normal rising edge triggered counter. The synchronous chain of T-flip flops generates a binary output signal. A conversion circuit is utilized to convert the binary code

into Gray code, which can be seen in Figure 3.30 [37]. Additionally, table 3.10 displaying how the grey code counts differently than if it were to use binary for only 4 bits.

Once the building blocks had been put together, a 7-bit Gray code counter was realized. A full count requires 128μs. The output counting waveforms of the counter is shown in Figure 3.31.

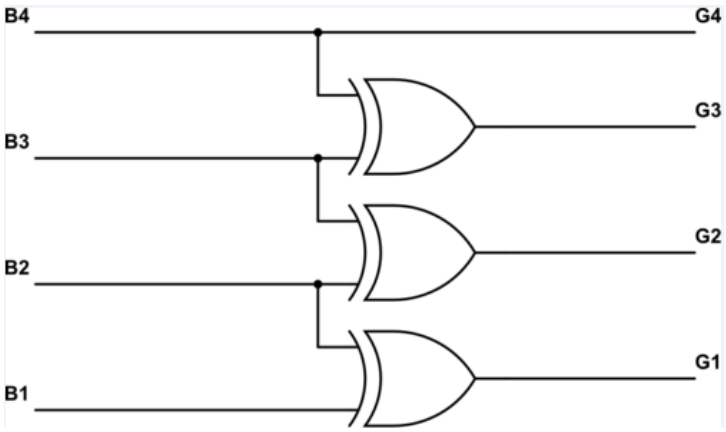


Figure 3.30 Binary to Gray code conversion circuit [37].

The layout of the digital portion of the analog-to-digital converter, including the Gray code counter, the register, and the control logic, is presented in Figure 3.32. The register and the control logic will be discussed in the following sections.

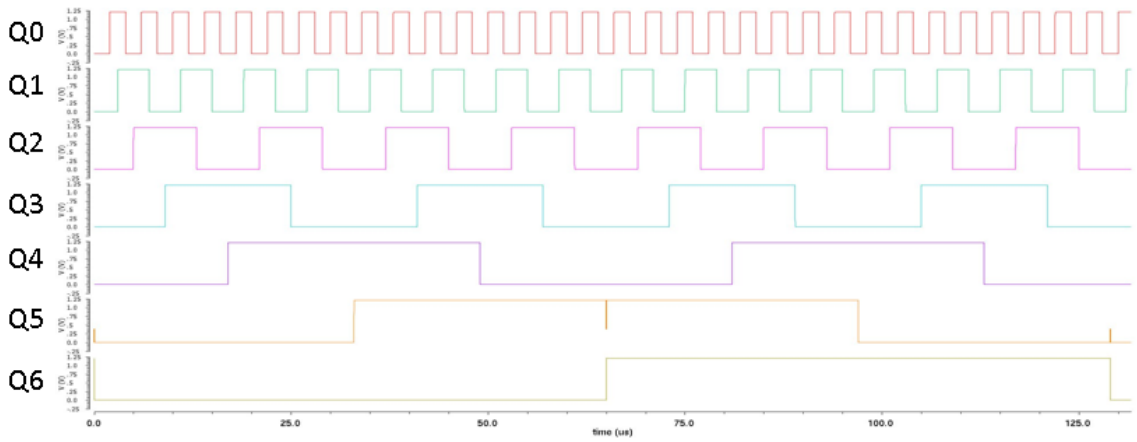


Figure 3.31 Gray code counting waveforms.

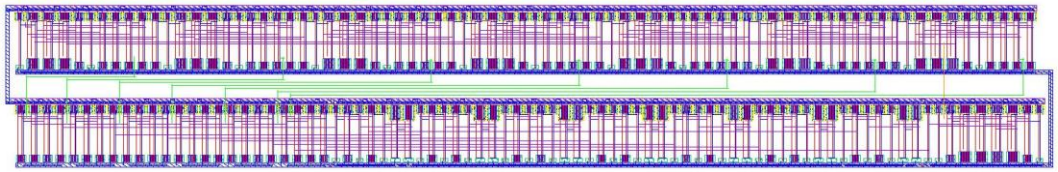


Figure 3.32 Layout of digital portion of the ADC.

Table 3.10 Example 4-bit Binary and Gray Code Count

Binary				**Grey Code**			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

3.8 Register

Once the output of the integrator has crossed the mid-rail voltage in the second phase of integration, the counter is shut off and its output is stored in the array of latches, which make a register. The register will then hold the digital output of the counter through the end of the 2nd phase integration and throughout the 1st phase of integration of the next cycle. This component of the ADC holds the output isolating it from any changes. The 7-bit register is realized with a combination of 7 d-latches. A D-latch will follow its input as long as the enable input is held high. When the signal falls 'low', it will latch holding the output at the value of the input of the time of latching and will not change regardless of the input signal. The structure of the D-latch is observed in Figure 3.33 and the truth table in Figure 3.34 [38].

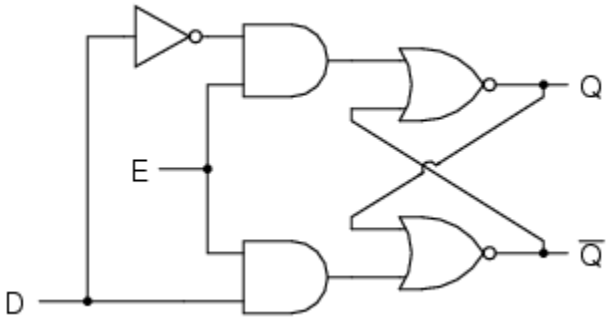


Figure 3.33 D-latch configuration [38].

E	D	Q	$\overline{Q}$
0	**0**	latch	latch
0	⌊	latch	latch
⌊	**0**	**0**	⌊
⌊	⌊	⌊	**0**

Figure 3.34 Truth table for D-latch [38].

3.9 Control Logic

The mid-rail conversion technique requires a few more switches than the traditional dual-slope procedure. For instance, during the second integration phase, the comparator needs to go low once the integrator output crosses 600 mV and shut off the counter. Since the integration output can be above or below mid-rail, the correct output of the fully differential comparator needs to be chosen so that the counter is shut off at the end of the conversion.

The conversion logic also serves the purpose of creating an overflow bit from the MSB of the counter, meaning that it effectively creates an 8^{th} counting bit. This overflow bit controls the switch that switches between the input and reference voltage. The configuration is realized by utilizing a D flip flop taking in the MSB of the counter to generate the overflow bit.

CHAPTER FOUR

RESULTS AND DISCUSSION

In this chapter, the results of the analog-to-digital converter are presented. Section 4.1 will detail the algorithm utilized to analyze the data and Section 4.2 will discuss the ADC performance.

4.1 Analyzation Algorithm

Given that the designed ADC is a mid-rail topology with a Gray code output, analysis of the results can be quite tricky. A typical dual-slope configuration will have the smallest analog input mapped to the smallest digital output. The mid-rail differs for the input voltages are taken with respect to mid-rail. To put it differently, the farther away the voltage is from mid-rail, the larger the count will be at the output. Additionally, another degree of complexity is added since the output is coded in Gray code. This creates a need for an algorithm that will accurately convert the mid-rail topology derived Gray coded outputs to a full-scale decimal number. The diagram of the conversion algorithm designed is depicted in Figure 4.1. The algorithm was developed in C++.

Per the specifications of the application, once the breathing signal falls in the range of 520 – 680 mV for 15 – 20 seconds, an apneic event has occurred. The apnea detection range is equivalent to the decimal range of 100 – 152.

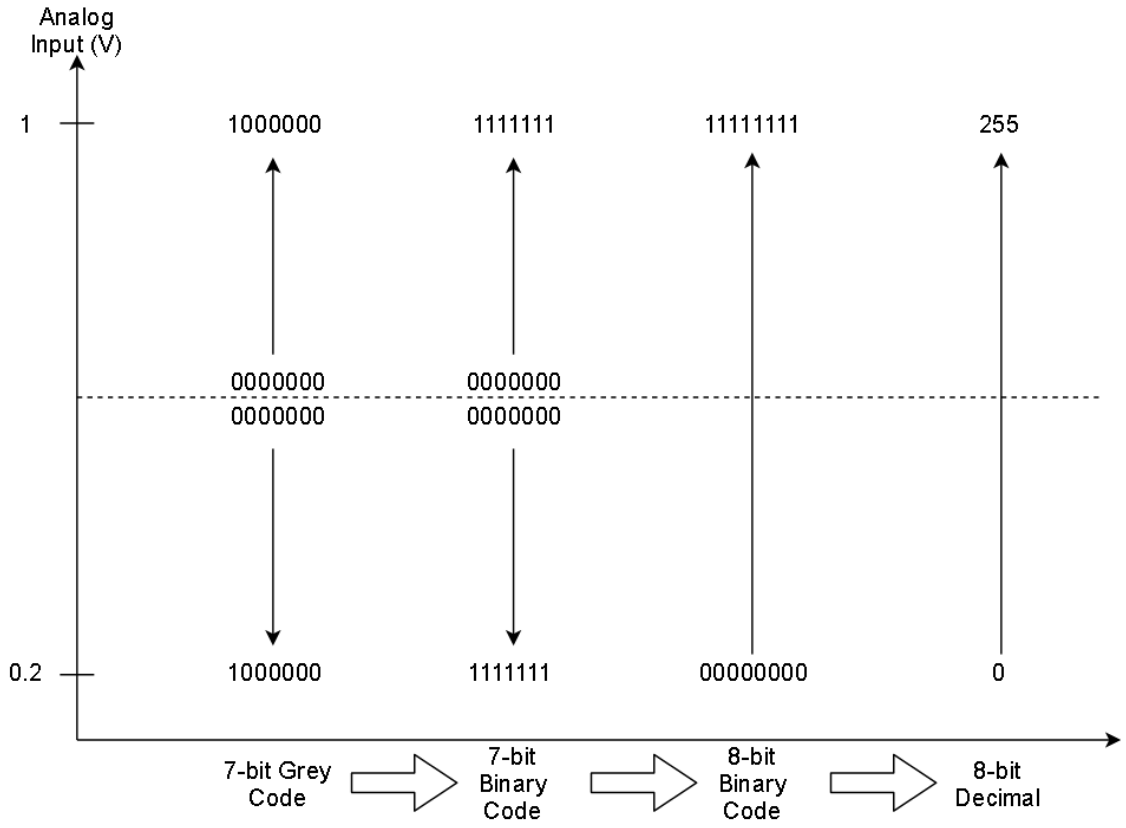


Figure 4.1 Analyzation algorithm conversion diagram.

Since the sampling frequency and the apnea detection time are known, the amount of conversions required for an apneic event can be expressed as,

$$Count = \frac{15\ s}{257\ \mu s} = 58366 \tag{4.1}$$

By means of this equation, apnea has occurred if the full-scale decimal output of the ADC lies between 100 -152 for 58366 samples.

4.2 ADC Performance

DC performance of an ADC can be described the integral nonlinearity error and differential nonlinearity error. The DNL specifies how far a code is from a neighboring code. The INL is defined as the distance in LSB that a code transition has taken place from the expected transition point. To guarantee that an ADC is monotonic, the performance needs to abide by either of the following equations,

$$INL \leq \pm\frac{1}{2}\ LSB \tag{4.2}$$

$$DNL \leq 1\ LSB \tag{4.3}$$

The ADC was tested by implementation of a 10-bit sampling of the input, which equates to a ¼ LSB step. Once all the voltages have been tested, a transfer function is derived. Next, the offset and gain errors are removed and the transfer function can be accurately plotted, as seen in Figure 4.2.

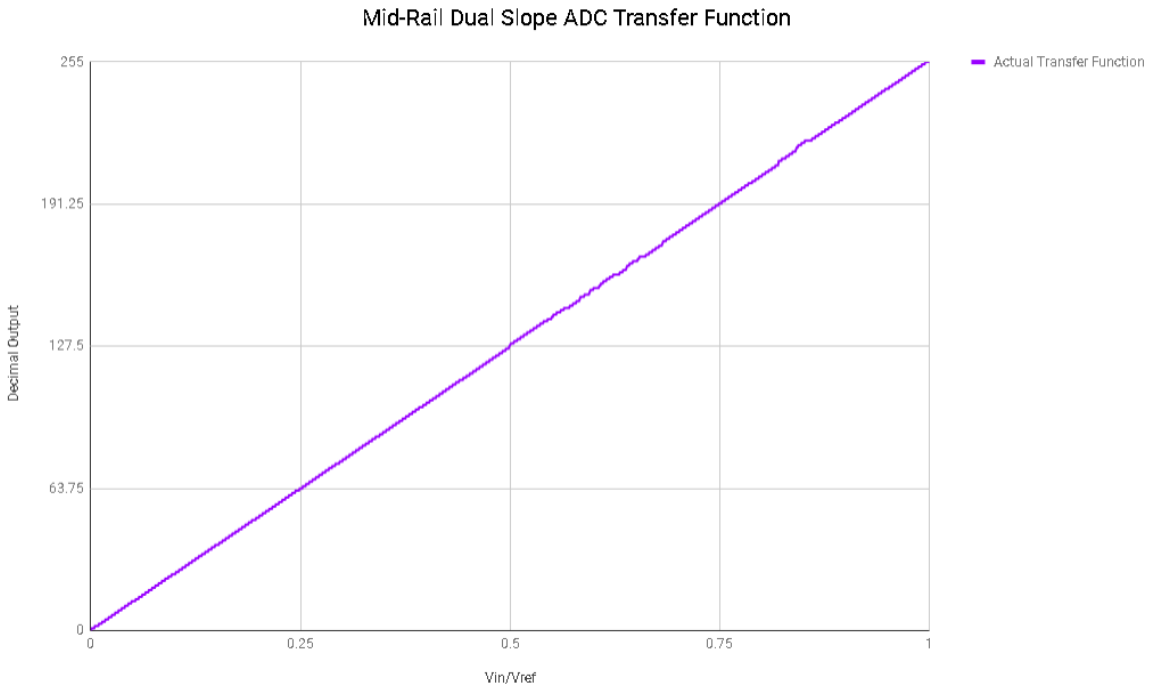


Figure 4.2 Transfer function of the ADC.

The INL and the DNL performances of the designed ADC are displayed in Figure 4.3. The designed ADC achieves an INL of -1 to 0.75 LSB and a DNL of -1 to 1.25 LSB. The charge injection was the biggest issue and affected the output codes in a linear fashion on each side of mid-rail. Consequently, two codes were missing from the design, decimal 79 and 209. One missing code is below mid-rail and the other is above. The algorithm designed above can somewhat compensate for the charge injection errors by adding or subtracting a decimal. As a result, the INL is decreased, but the missing codes remain. Although the missing codes are not desired, for this application, there is no harm done since the apnea detection range is of upmost importance and the missing codes do not affect this. Moreover, the ADC is quite accurate due to all of the compensation utilized despite the two missing outputs.

The ADC achieves a low power consumption of 40.86 µW, which meets the specification of below 50 µW. The final layout can be seen in Figure 4.4. The resulting area is expressed as,

$$106.37\mu m \text{ x } 264.89\mu m = 28173.7\ \mu m^2 = 0.028173\ mm^2 \qquad (4.4)$$

The ADC performance metrics are tabulated in table 4.1. The ADC is then compared against other dual slope topologies in Table 4.2.

The ADC achieves an extremely low area and low power consumption. It could be tested with a faster sampling frequency to improve the first Figure of Merit (FOM_1), but it already suits the application.

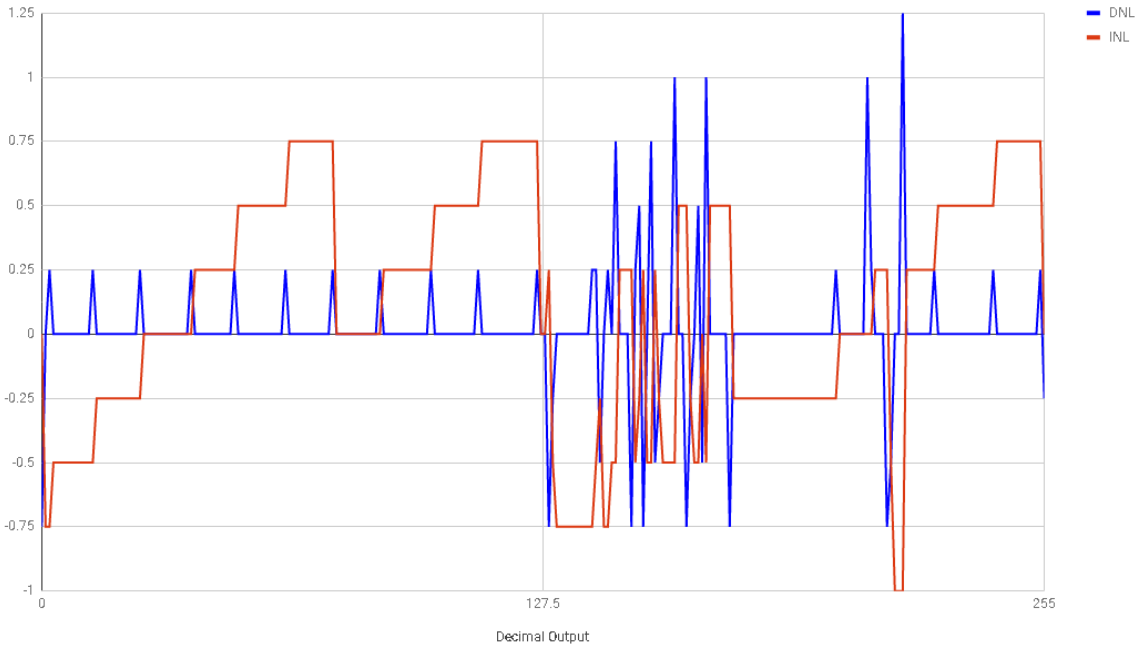


Figure 4.3 INL and DNL performances of the designed ADC.

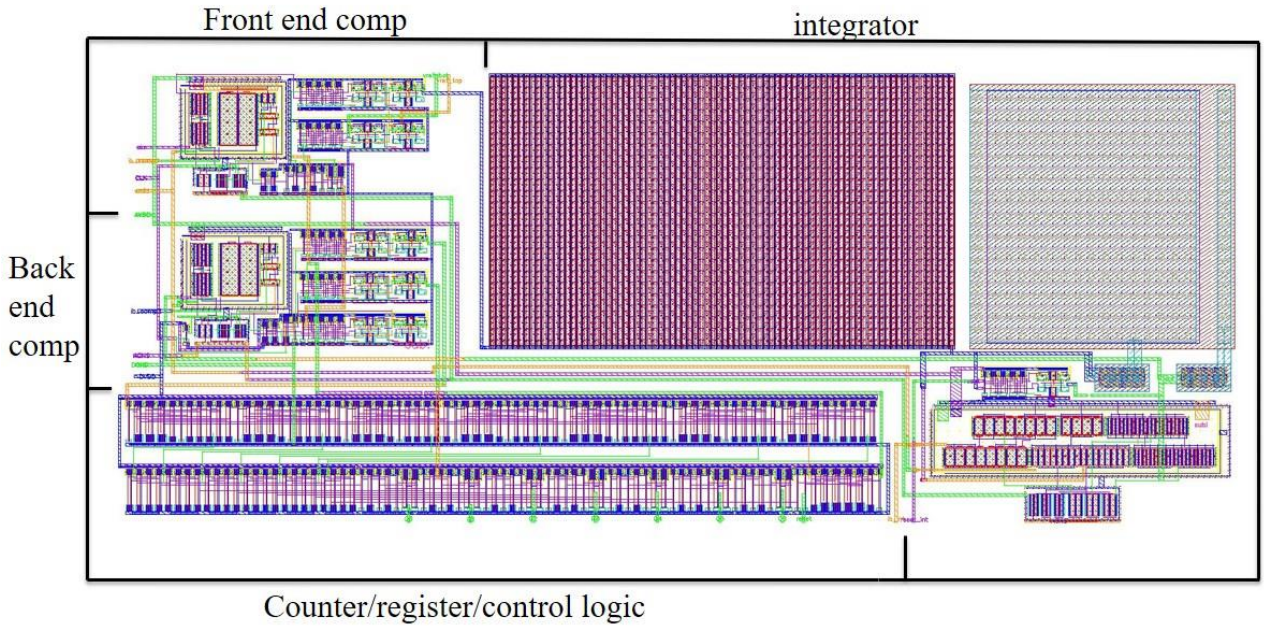


Figure 4.4 Final layout of the designed ADC.

Table 4.1 ADC Performance Metrics

Performance Metrics	**Values**
Analog Power	40.79 µW
Dynamic Power	64.5 nW
Total Power	40.855 µW
INL	-1 to 0.75 LSB
DNL	-1 to 1.25 LSB

Table 4.2 Performance Comparison

	[39]	**[40]**	**[41]**	**[42]**	**This Work**
Bits N	10	9	7	11	8
Technology	0.6µm	130nm	130nm	0.35µm	130nm
Power (µW)	250	42	44	19800	40.86
Sampling Frequency (Hz)	7.1k	10k	15k	11.4k	3.9k
Area (mm^2)	0.6	0.06	0.6	0.0917	0.0282
FOM_1 $pJ/2^Nf_s$	34.4	9.1	14.3	848	40.93
FOM_2 $\mu m^2/2^N$	585.94	117.19	4687.5	44.8	110.05

To verify the ADC further, all process corners were tested and no variation was recorded. This further ensures the stability of the design and how it resists parameter variations within a circuit.

CHAPTER FIVE

CONCLUSIONS AND FUTURE WORK

In this chapter, section 5.1 discusses conclusions drawn from the design of a mid-rail dual slope ADC. Then, section 5.2 presents the original contributions. Lastly, section 5.3 examines future work.

5.1 Conclusions

In this work, an 8-bit mid-rail dual slope ADC is presented for the detection of apnea. The data converter is low power and is able to accurately represent the input analog voltages as a 7-bit digital output for an effective 8-bit resolution. Two codes are missing from the transfer function, making the ADC non-monotonic. Although, this does not particularly affect the application it is being utilized for since the converter is otherwise quite accurate and the apnea detection range is converted properly into a digital output.

It can be concluded that the mid-rail topology is viable and can be quite advantageous to the traditional dual slope ADC design.

5.2 Original Contributions

This work proposed a novel approach for the design of a dual slope analog-to-digital converter. The unique methodology improves upon the typical design by cutting the sampling frequency in half and the ability to operate on a single polarity supply system.

In addition to the novel data conversion concept, it is realized in the construction of an 8-bit mid-rail dual slope ADC. The design is highly accurate and consumes low power.

5.3 Future Work

Accuracy of the ADC can further be improved up by diminishing the charge injection effects even further. This can be done with a fully differential integrator, as it reduces charge injection and clock feedthrough effects by CMRR to the first order. Furthermore, the power can be reduced by decreasing the bias current for the integrator and subsequently design for subthreshold region.

The Figure of Merit will greatly improve if the sampling speed is increased, although the increase was not needed for the application. The digital power is very low for the current design and has the headroom to increase. Moreover, a smaller resistor and capacitor are needed to meet the time constant requirements.

A different comparator structure can be researched for replacing the front-end comparator. This component may not need the preamplifier, which could potentially reduce

the power. Alternatively, a Threshold Inverter Quantization (TIQ) comparator or another static architecture can be explored.

The ADC will be fabricated in the standard 130nm CMOS process. The system will then be tested to ensure accurate performance and then implemented into the apnea detection system.

Given the performance of the data converter, it could be interesting to investigate the other applications in which it could be employed.

REFERENCES

[1] H. Wu, X. Zhan, M. Zhao, and Y. Wei, “Mean apnea–hypopnea duration (but not apnea–hypopnea index) is associated with worse hypertension in patients with obstructive sleep apnea,” *Medicine*, vol. 95, no. 48, 2016.
[2] A. Malhotra and D. P. White, “Obstructive sleep apnea,” Lancet, vol. 360, no. 9328, pp. 237-245, July 2002.
[3] L. Spicuzza, D. Caruso, and G. D. Maria, “Obstructive Sleep Apnoea Syndrome and Its Management,” *Therapeutic Advances in Chronic Disease*, vol. 6, no. 5, pp. 273–285, 2015.
[4] “Obstructive Sleep Apnea,” *Sleep Apnea Treatment Centers of America*, 18-Nov-2013. [Online]. Available: http://curemysleepapnea.com/obstructive-sleep-apnea/.
[5] J. C. Jackson, “Respiratory Distress in the Preterm Infant,” *Averys Diseases of the Newborn*, pp. 633–646, 2012.
[6] “Apnea, Suddent Infant Death Syndrome, and Home Monitoring,” Pediatrics, vol. 111, pp. 914 – 917, 2003.
[7] I. Mahbub, H. Wang, S. K. Islam, S. A. Pullano, and A. S. Fiorillo, “A Low Power Wireless Breathing Monitoring System Using Piezoelectric Transducer,” *2016 IEEE International Symposium on Medical Measurements and Applications (MeMeA)*, 2016.
[8] Maxim Integrated Inc., “Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs,” *Maxim Tutorial 1080*, 2001.
[9] W. Kester and J. Bryant, “ADCs for DSP, part 1,” *Embedded*, 04-Oct-2007. [Online]. Available: http://www.embedded.com/print/4017542.
[10] E. Hnatek, *A User's Handbook of Digital-to-Analog and Analog-to-Digital Converters*. John Wiley & Sons.
[11] H. A. Hassan, I. A. Halin, I. B. Aris, and M. K. B. Hassan, “Design of 8-bit SAR-ADC CMOS,” *2009 IEEE Student Conference on Research and Development*, Apr. 2010.
[12] “Understanding Pipelined ADCs,” *Understanding Pipelined ADCs - Tutorial - Maxim*. [Online]. Available: http://maximintegrated.com/en/app-notes/index.mvp/id/1023.
[13] “Analog to Digital Converter Architecture,” *VLSI-Egypt*, 15-Jan-2015. [Online]. Available: http://www.vlsiegypt.com/home/?p=2123.
[14] D. Hoeschele, *Analog to Digital and Digital to Analog Conversion Techniques*. 1994.
[15] B. Razavi, “Pipelined ADC Architectures,” *Pipelined ADC Architectures*. [Online]. Available: http://www.seas.ucla.edu/brweb/teaching/215D_S2012/PipeADCs.pdf.
[16] A. Loloee, “Understanding Delta-Sigma Modulators,” *Electronic Design*, 06-Aug-2013. [Online]. Available: http://www.electronicdesign.com/analog/understanding-delta-sigma-modulators.
[17] E. Smith, “Understanding the Delta-Sigma ADC,” *All About Circuits*, 14-Jul-2016. [Online]. Available: https://www.allaboutcircuits.com/technical-articles/understanding-the-delta-sigma-analog-to-digital-converter/.

[18] D. Johns and K. W. Martin, *Analog integrated circuit design*. Chichester: Wiley, 2010.
[19] "How delta-sigma ADCs work, Part 1 (Rev. A) - TI.com." [Online]. Available: http://www.bing.com/cr?IG=019C8046CE2D44F99BB4FBEC8885E23B&CID=147570078FC263B625167BD18E6D6226&rd=1&h=abRLUu5DOvGhC-sgoZzJt_MtBPX3jLBJD_PXqEd3ceY&v=1&r=http://www.ti.com/lit/an/slyt423a/slyt423a.pdf&p=DevEx.LB.1,5068.1.
[20] "Understanding Flash ADCs," *Maxim Integrated*, 16-Sep-2010. [Online]. Available: http://www.maximintegrated.com/en/app-notes/index.mvp/id/810.
[21] "Flash Type ADC," *Electronics Tutorial*. [Online]. Available: http://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/flash-type-adc/index.html
[22] "Understanding Integrating ADCs," *Maxim Integrated*. [Online]. Available: http://www.maximintegrated.com/en/app-notes/index.mvp/id/1041.
[23] J. R. Baker, *CMOS Circuit Design*, 3rd ed. Wiley, 2010.
[24] A. Oblea, "Integrating ADCs: A Tutorial," *ltwiki.org*, 19-May-2008. [Online]. Available: http://ltwiki.org/files/LTspiceIV/examples/LTspice_cmosedu/_Extras_LTspice/Integrating_ADC/IntegratingADC_tutorial.pdf.
[25] "Dual Slope Type ADC," *Electronics Tutorial*. [Online]. Available: http://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/dual-slope-type-adc/index.html.
[26] P. R. Gray, *Analysis and design of analog integrated circuits*. New York: Wiley, 2011
[27] K. N. Hosur, G. V. Attimarad, H. M. Kittur, and S. S. Kerur, "Design and simulation of Low Power Successive Approximation Register for Analog-to-Digital Converters using 0.18um CMOS Technology," *International Journal of Engineering and Technology*, vol. 8, no. 2, pp. 742–750, 2016.
[28] E. Rahiminejad and R. Lotfi, "A low-power architecture for integrating analog-to-digital converters," *2009 16th IEEE International Conference on Electronics, Circuits and Systems - (ICECS 2009)*, 2009.
[29] R. Zhang, K. Liu, and Z. Du, "Low power and high accurate dual-slope ADC using chopper stabilized technique," *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2014.
[30] I. Mahbub, "Design and Implementation of a Low-Power Wireless Respiration Monitoring Sensor," dissertation, 2017.
[31] "ADC Errors," *cypress*. [Online]. Available: http://www.cypress.com/file/144536/download.
[32] "Dynamic Power Consumption," *siliconintelligence*. [Online]. Available: www.siliconintelligence.com/people/binu/percetion/node13.html.
[33] D. M. Binkley, *Tradeoffs and optimization in analog CMOS design*. Chichester, England: John Wiley & Sons, 2008.

[34] D. M. Binkley, B. J. Blalock, and J. M. Rochelle, “Optimizing Drain Current, Inversion Level, and Channel Length in Analog CMOS Design,” *Analog Integrated Circuits and Signal Processing*, vol. 47, pp. 137–163, Mar. 2016.
[35] I. Opris and G. Kovacs, “A rail-to-rail ping-pong op-amp,” *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1320–1324, 1996.
[36] G. M. Blair, “SYNCHRONOUS DESIGN IN THE GATEWAY LABORATORY,” *athena*. [Online]. Available: http://athena.ecs.csus.edu/~changw/class_docs/VerilogManual/Sync.html.
[37] “Binary to Gray Code Converter and Grey to Binary Code Converter.” [Online]. Available: https://www.electrical4u.com/binary-to-gray-code-converter-and-grey-to-binary-code-converter/.
[38] “The D Latch,” *All About Circuits*. [Online]. Available: https://www.allaboutcircuits.com/textbook/digital/chpt-10/d-latch/.
[39] A. Dehennis, M. Mailand, etl., “A Near-Field-Communication (NFC) Enabled Wireless Fluorimeter for Fully Implantable Biosensing Applications”, *IEEE ISSCC 2013,* pp. 298-299.
[40] H. Jafari, L. Soleymani, and R. Genov, “16-Channel CMOS Impedance Spectroscopy DNA Analyzer with Dual-Slope Multiplying ADCs,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, Issue 5, pp. 468-478, Oct. 2012.
[41] H. Shan, S. Rausch, A. Jou, N. J. Conrad, and S. Mohammadi, “A low power programmable dual-slope ADC for single-chip RFID sensor nodes,” *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2017.
[42] D. Shetty and P. T. Renukaswamy, “A 11-Bit Integrating Analog to Digital Converter,” *2016 Austrochip Workshop on Microelectronics (Austrochip)*, 2016.

VITA

Dallas Hamlin was born in Nashville, TN. He graduated from Harpeth High School in Kingston Springs, Tennessee, among the top of his class. received his B.S. degree in Electrical Engineering from the University of Tennessee, Knoxville, in December of 2016. Directly after graduating, he accepted a graduate teaching position under Dr. Syed Kamrul Islam and joined the Analog, VLSI and Devices research group. He obtained a Master of Science degree in Electrical Engineering in May of 2018.