To the Graduate Council:

I am submitting herewith a thesis written by Adeoti Taiwo Adediran entitled "Some Studies on Three-Phase Diode Rectifier - Boost Converter for active filtering." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirement for the degree of Master of Science, with a major in Electrical Engineering.

Bimal K. Bose

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Associate Vice Chancellor
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SOME STUDIES ON THREE-PHASE DIODE RECTIFIER - BOOST CONVERTER FOR ACTIVE FILTERING

A Thesis
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Abstract

This thesis seeks to rigorously pursue the specialty of power line conditioning. It begins with a discussion of established facts in power line conditioning theory, reviews work in this area up to date, then proposes an improved active power factor correction method for power supplies.

The performance of an improved power line conditioning topology is presented in Chapter 3. Work up to date in this area is reviewed in Chapter 2. The proposed topology is compared and justified and the thesis is concluded with thesis accomplishments.

A proof-of-principle 3-phase boost converter was built and tested. The converter consists of a three-phase diode bridge as the AC and DC interface, AC and DC side boost inductors and a boost switch. Results show the proposed scheme improves power factor from a typical 60 percent to near unity.

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List of Symbols and Abbreviations

PLC	-	Power line conditioners
SMPS	-	Switch mode Power suply
t_1	-	Maximum on time
Ia	-	Phase A line current
Ls	-	AC side boost inductor
t	-	time
v_{ab}	-	Instantaneous line voltage
Vcp	-	DC link capacitor voltage
t_2	-	Maximum switching time
v_{an}	-	Instantaneous phase A voltage
v_{bn}	-	Instantaneous phase B voltage
v_{cn}	-	Instantaneous phase C voltage
Va	-	Phase A voltage
Vb	-	Phase B voltage
Vc	-	Phase C voltage
Ib	-	Phase B line current
Ic	-	Phase C line current
i_a	-	Instantaneous phase A line current
i_b	-	Instantaneous phase B line current
i_c	-	Instantaneous phase C line current
Vd	-	DC output voltage unless otherwise stated
I_d	-	DC link current
L_{THK}	-	Thevenin inductance as seen by phase K (generic naming)
Rds	-	Drain to source resistance
Pon	-	On state power loss
i_1	-	Mesh current in Fig. 3.2
i_2	-	Mesh current in Fig. 3.3
//	-	Parallel
Cs	-	Snubber capacitor
Rs	-	Snubber resistor

tfi	-	Mosfet current fall time
tc	-	Time constant
tri	-	Mosfet current rise time

Chapter 1

Introduction

1.1 Thesis Motivation

In industrial applications where three-phase AC voltages are very readily available, the three-phase rectifiers are preferred to the single-phase rectifiers. The main reason for this is that three-phase rectifiers exhibit lower ripple content and have higher power-handling capability compared to their single-phase counterparts.

However, even though three-phase rectifiers are better than single-phase rectifiers, they too produce intolerably high AC side harmonics which limit access to total available wall or socket power. This reason and others such as voltage regulation problems in the presence of harmonics are the motivation for the development of power line conditioners.

Power line conditioners (which from now on will be referred to as PLC) was developed primarily as a way to reduce or eliminate AC side harmonics and current distortion, in order that more useful power be extracted from a standard outlet. Recently the demand for power line conditioners has increased due to the enforcement of harmonics standards (like the IEC Harmonics Standard 555-2 and the IEEE 519 [14]) that limit the amount of harmonics an equipment can feed back into the main supply. These standards now constitute a formidable driving force for innovation in the field of power line conditioning. The more basic problem of power quality, however, still forms the bedrock of power conditioning circuit motivation.

1.2 Power Quality Problems

Power quality problems are brought about by the widespread use of nonlinear loads in the system. Such loads include the power conversion circuits. Power quality problems include current distortion, voltage distortion and phase displacement. In order to reduce or eliminate power quality problems two major kinds of power line conditioning circuits are used commonly. They are

(1) Passive power line conditioners.

(2) Active power line conditioners.

Passive power line conditioners are configured with capacitors, inductors and sometimes resistors. Well known configurations include smoothing series inductors, parallel connected resonant filter (in basic and m-derivative form) and series connected resonant filter (also in basic and m-derivative form) [12]. Passive power line conditioning circuits do not fully restore the sinusoidal waveshape of the input line current and they are bulky. They are, however, simple and do not require a lot of components.

Active power line conditioning: uses PWM converters, boost converters, flyback converters and buck-boost converters. All of the active power line conditioners give appreciably better line current waveshape and are lighter but are comparatively more complex and expensive.

Chapter 2

Review

2.1 Semiconductor Devices

Power electronic switches can be divided into two categories--controllable switches and uncontrollable switches. The only example of an uncontrollable switch is the diode. Examples of the controllable switch are:

(1) Bipolar transistor

(2) Metal oxide semiconductor field effect transistor, mosfet

(3) Thyristor

(4) Junction field effect transistor

(5) Hybrid switches like the MCT, IGBT, and SIT

All active power line conditioners use at least one of the above mentioned types of switches.

2.2 Power Line Conditioning Circuit Review

2.2.1 PLC Application Review.

AC power is the primary type of utility power. Most DC consumption barring those supplied by battery have to undergo AC to DC conversion. Approximately ninety percent of all AC to DC converters utilizes active filtering normally referred to as PLC.

Electric power generally (AC or DC) has common usage. Wherever power conversion is carried out, power line conditioning is used to correct the non linearity introduced by that conversion. A few examples where PLCs are used are listed below:

(1) DC link Inverters.

(2) Supply to DC machine load or general DC loads.

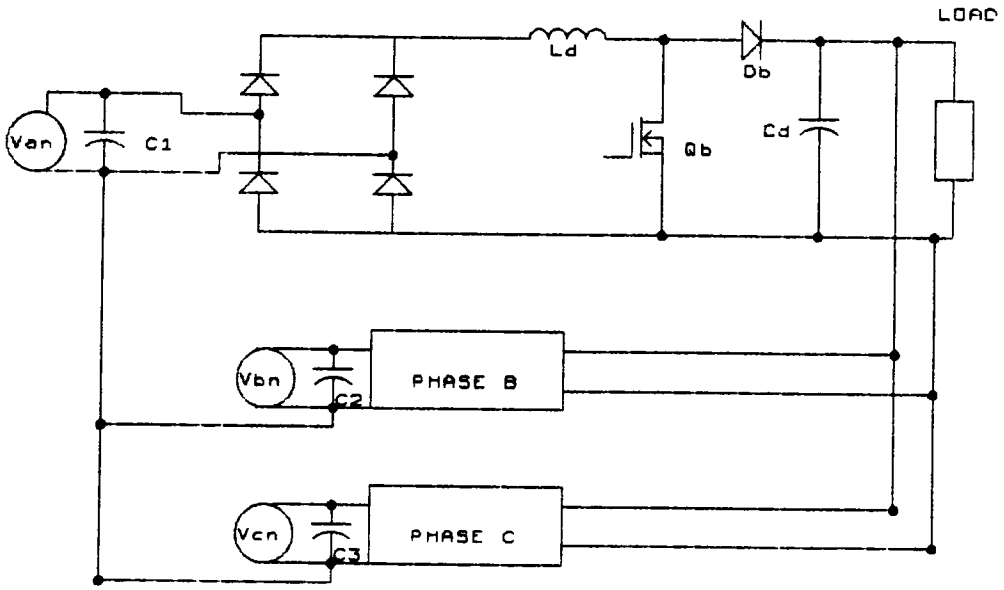
(3) Uninterruptable power supply.

2.2.2 Active Power Line Conditioners-Operational Review.

In discussing the operation of a PLC, the emphasis is placed on three-phase PLC operation. The conventional topology of a three-phase PLC is three single-phase PLCs arranged in parallel. This arrangement is illustrated in Figure 2.1. Since operations in all three branches are presumed to be identical, it is sufficient to discuss the operation of just one. As indicated in the figure, the input AC voltage is rectified into an unregulated DC voltage by means of the single-phase full bridge diode rectifier. It should be noted that a passive filter is used at the input to prevent the generated high frequency harmonics from being fed into the system. The DC-DC converter block converts the input DC voltage from one level to another. This is accomplished under high frequency switching. The harmonics generated by the high frequency switching of the converter are bounded around the switching frequency and are filtered off, on the load side by a large capacitor and by the EMI filter on the utility side. The equations governing this phenomenon are

Turn-on $0<t<t_1$

$$i_a(\omega t) = \frac{v_{ab}(peak)*t}{Ls} \tag{2.1}$$



Conventional Power Line Conditioning Circuit with Three Modular Units

Figure 2.1

At time t_1 the inductor current i_a reaches its maximum value and the boost switch is turned off by its appropriate control signal.

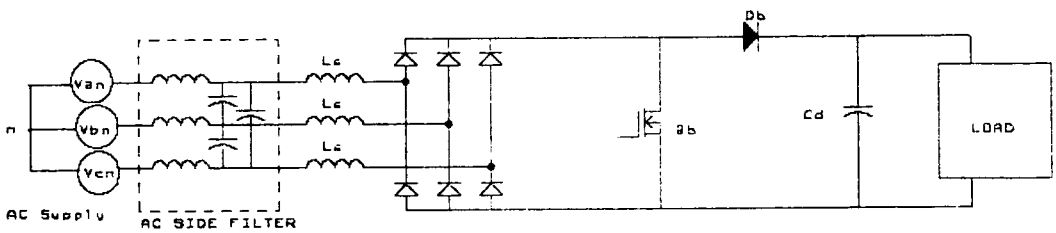
$$\text{Turn-off} \quad t_1<t<t_2$$

$$i_a(wt) = \frac{v_{ab}\,(peak)*t}{Ls} - \frac{v_{en}*(t-t_1)}{Ls} \tag{2.2}$$

The minimum output DC voltage is

$$V_{dc} = v_{en}* \sqrt{3} \quad . \tag{2.3}$$

Another arrangement is a three-phase bridge with a power switch depicted in Figure 2.2. The operation is similar except the fact that the three phases of the input are shorted at turn-on with the current in each phase rising at the rate determined at any instant by the magnitude of the phase voltages and the AC side boost inductors Ls. The same governing equations hold, with v_{ab} changed to v_{an}, v_{bn} and v_{cn} for phases a, b and c respectively.



Main Circuit for the Active Power Factor Correction for Three Phase Bridge Scheme

Figure 2.2

Expected waveforms before filtering are shown in Figure 2.3 for the single-phase and three-phase arrangements. It is important to point out that a specific topology has been

cited to illustrate the operation of power line conditioning. There are, however, many topologies available for PLC, some of which are discussed in the next section.

2.2.3 Study and Analysis of Current Topologies

Existing single-phase and three-phase PLC will be examined in this section with a view to determining their effectiveness in power factor correction and current shaping. Some existing topologies are listed below

(1) Active power factor correction technique for three-phase diode bridge by Ziogas et al [4].

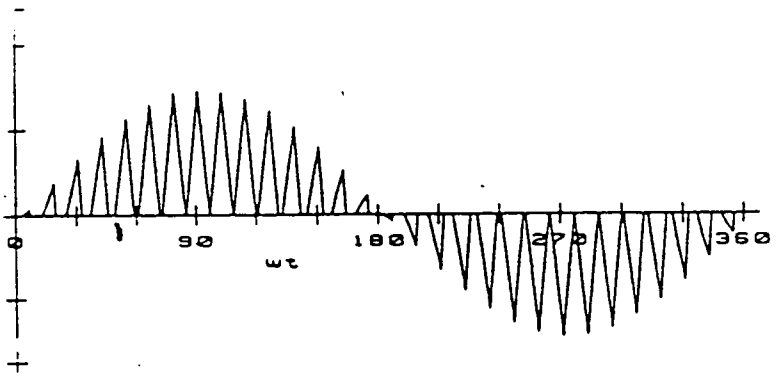
(2) PWM AC to DC converter with fixed switching by Rusong et al [11].

(3) Active power factor correction for single-phase AC to DC as given by Chen Zhou et al [5].

(4) PLC topology presented in discussion of operation of hysteresis current-controlled PWM rectifiers by Juan Dixon et al [6].

(5) AC to DC converter by Mark Kocher et al [10].

Under each topic, the schematic of the circuit is given, the operation of the circuit is discussed, and the circuit performance is presented.



AC Side Current Waveform (before filtering) of the PLC shown in Figure 2.2

Figure 2.3

(1) Active Power Factor Correction Technique for Three-Phase Diode Bridge: The schematic is as shown in Figure 2.2

Abbreviations and Symbols:

Ls = AC line boost inductor

t = Any time within the whole switching interval

t_1 = Maximum on time

t_2 = Maximum switching time

$i_a(wt)$ = Instantaneous peak phase A current

$v_{an}(peak)$ = Instantaneous peak phase A voltage

v_{en} = instantaneous peak capacitor voltage

Principle of operation: As shown in Figure 2.2, the circuit includes a diode bridge, an AC line inductor and a DC link capacitor. The boost switch is turned on and off at a constant frequency. The duty cycle is varied only for load variations, which is accomplished by a negative feedback from the output voltage. The block diagram of the control is shown in Figure 2.4. The operation is restricted to discontinuous input current conduction. During the "on period" of the boost switch, all three input AC phases become shorted through the AC side inductors Ls, three rectifier diodes and the boost switch. Consequently, the three input currents i_a, i_b, and i_c begin rising simultaneously at a rate proportional to the instantaneous values of their respective phase voltages. The peak current values during each "on interval" are proportional to the values of their input phase voltages during the same interval. Since the voltage values vary sinusoidally, the peak current also varies sinusoidally. Since these current pulses begin from zero, their average value also varies sinusoidally. The resultant distortion factor is therefore unity.

The major equations governing this operation are as mentioned in the review of PLC operation and are given again as follows:

'on time ' $0<t<t_1$

$$i_a(\omega t) = \frac{v_{an}(peak)*t}{Ls} \qquad (2.4)$$

'off time ' $t_1<t<t_2$

$$i_a(\omega t) = \frac{v_{an}(peak)*t}{Ls} - \frac{v_{en}*(t-t_1)}{Ls} \qquad (2.5)$$

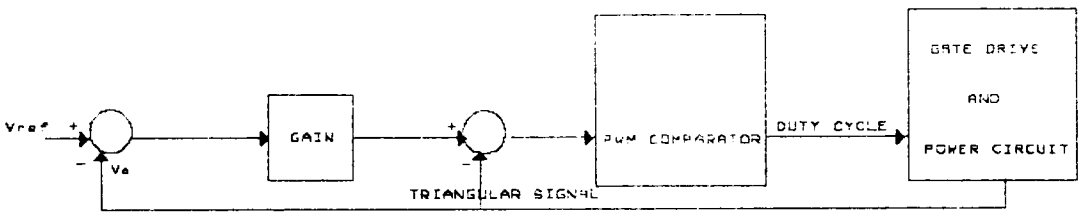
Boundary conditions are listed below

$t=0 \qquad i_a=0$

$t=t_1 \qquad i_a=Ipeak$

$t=t_2 \qquad i_a=0$

Circuit performance: All three input currents consist of a fundamental component and a band of high frequency components centered around the switching frequency of the boost switch. These harmonics are filtered off to the AC side by the EMI filter and to the DC side by the DC link capacitor. The circuit gives extremely good power factor but draws much higher line currents for same DC output power than the conventional diode rectifier. This produces an adverse effect of stress on the power supply components. The loss in the switch, consequently, is high.



Control Schematic for the Topology in Figure 2.2

Figure 2.4

(2) Active Power Factor Correction for Single-phase AC to DC

Abbreviations and Symbols

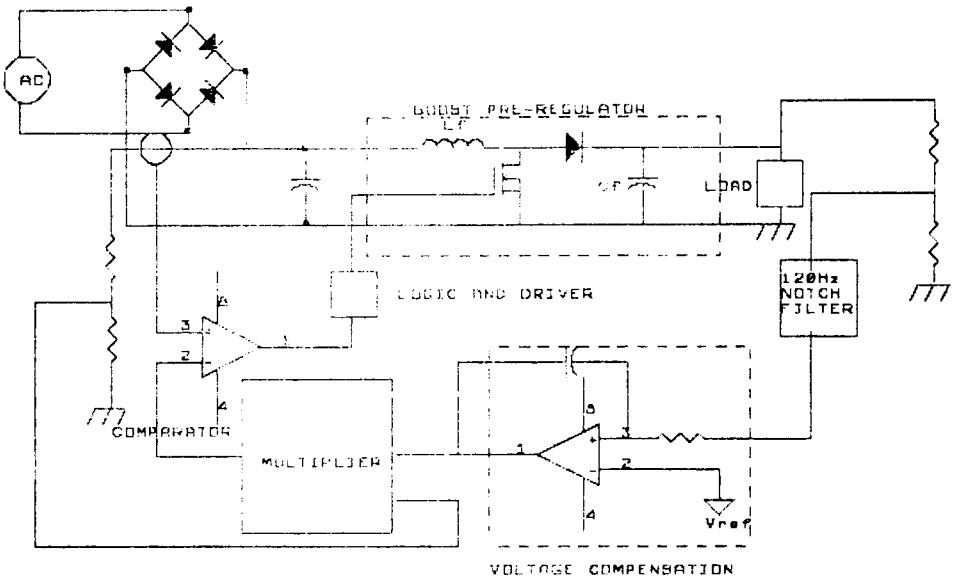
Eo = DC output voltage
Ec = Error voltage
Rl = Load resistance
Cf = Filter capacitance
Vi = Nominal rms line voltage
g_c = Control gain

The AC to DC converter topology presented by Chen Zhou et al [5] can be seen in Figure 2.5. The circuit consists of a single-phase full bridge, a boost converter, and a variable-hysteresis control. The variable hysteresis control operates as follows: The inductor current, the rectified AC line voltage, and the output voltage are sensed. The sensed rectified AC line voltage is scaled down to produce the upper and lower inductor current references. The gate drive logic is designed such that the inductor current switches between these two references. With this hysteresis band control, the inductor current is forced to track the line voltage. Figure 2.6 illustrates this current tracking. To regulate the load, the error amplifier senses the variations between the output voltage and the fixed reference. This error voltage is multiplied with the sensed rectified line voltage to control the inductor current amplitude.

Experimental results indicate a circuit efficiency of 93.2 percent. The control to output transfer function for a resistive load is given by

$$\frac{\hat{E}o}{\hat{E}c} = \frac{g_c * Rl}{2} * \frac{1}{(1+\frac{sCfRl}{2})} \tag{2.6}$$

$$g_c = \frac{Vi^2}{kEo} \tag{2.7}$$



Complete Circuit Diagram of "Active Power Factor Correction for Single Phase AC to DC"

Figure 2.5

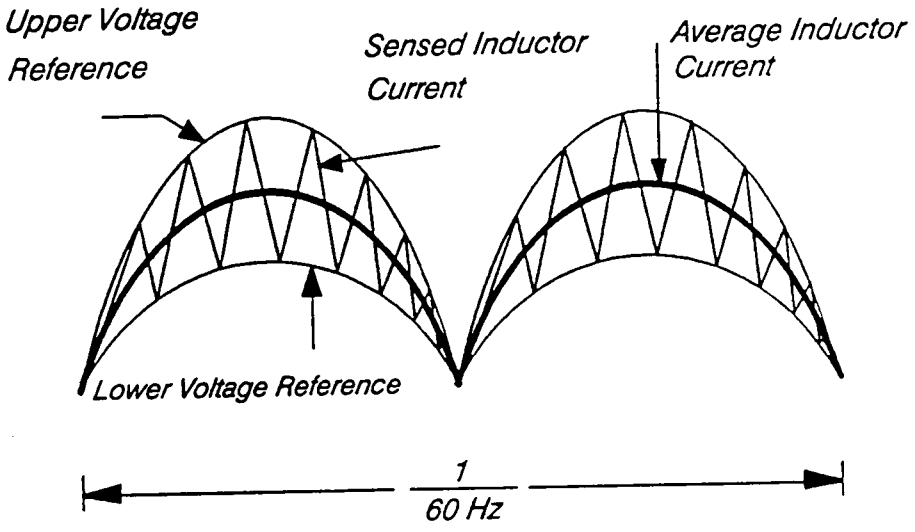


Illustration of DC Side Line Current Tracking using Sensed Inductor Current and Line Voltage Envelopes

Figure 2.6

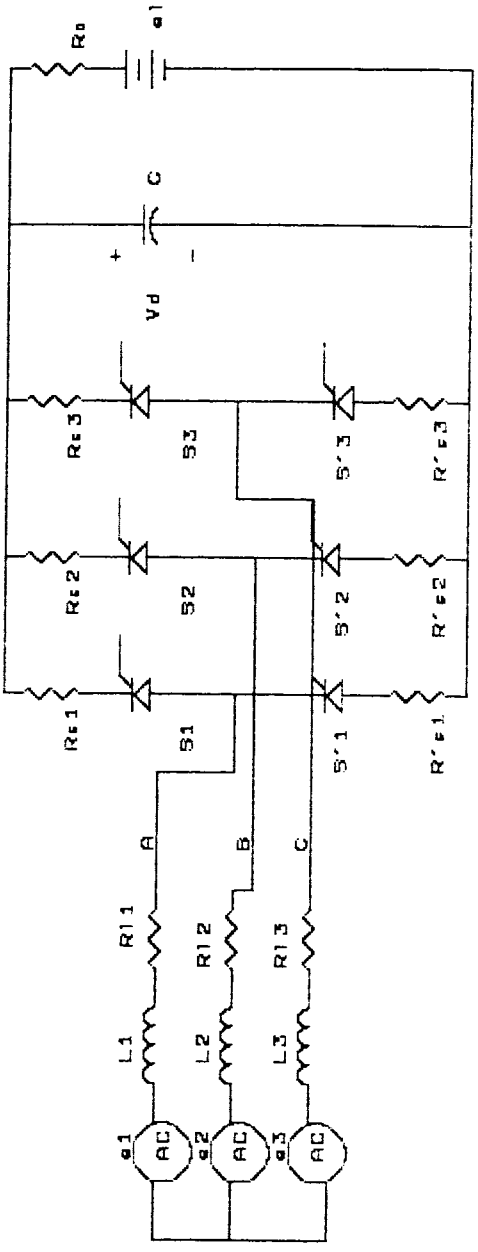
(3)PWM AC to DC Converter with Fixed Switching Frequency

Abbreviations and Symbols

d_k = Duty cycle ratio
e_k = Line voltage (generic naming, see Figure 2.7)
i_k = Line current (generic naming)
Vd = DC output voltage
i_{ck} = Command current (generated from a look up table)
T = Switching period
Rl = AC side filter resistance (see Figure 2.7)
L = AC side filter inductance
Vck = Voltage signal fed into PWM comparator to produce gate pulses
Vs = Switch resistor voltage

Circuit operation: The main circuit is shown in Figure 2.7. The rectifier operates under PWM switching. An intricate switching pattern is created by the control. Which utilizes the principle of predicted current control. As power factor and input current shaping are essentially accomplished by the switching pattern of the rectifier bridge, which is generated by the control, discussion of operation of the converter would center around the control Circuit operation. The instantaneous current values are determined by the duty cycle ratio of their respective power switches. For the predicted current control strategy with fixed switching frequency (PCFF) control, the duty cycle ratio d_k is derived from the voltage e_k, line current i_k, DC output voltage Vd and a current command i_{ck}. The overall expression is given as

$$d_k = \frac{[e_k-(Rl-\frac{L}{T})*i_k-\frac{L*i_{ck}}{T}]}{Vd}+\frac{1}{2} \qquad (2.8)$$



Main Circuit of the PCFF Scheme

Figure 2.7

Figure 2.8 shows a block diagram of the PCFF control. The voltage Vck, necessary for controlling the line current, is created first by a combination of e_k, i_k, Vd and the current command i_{ck} as

$$Vck = \frac{2*Vs*[e_k-(Rl-\frac{L}{T})*i_k - \frac{L*i_{ck}}{T}]}{Vd} \qquad (2.9)$$

This voltage is transferred to a voltage/trigger converter where it is compared with a triangular waveform. The intersection of these two determines the switching pattern. Current shaping is effected through the current command i_{ck}. Related equations are given as

$$\frac{di_k}{dt} = \frac{1}{T} * [i_{ck}-i_k] \qquad (2.10)$$

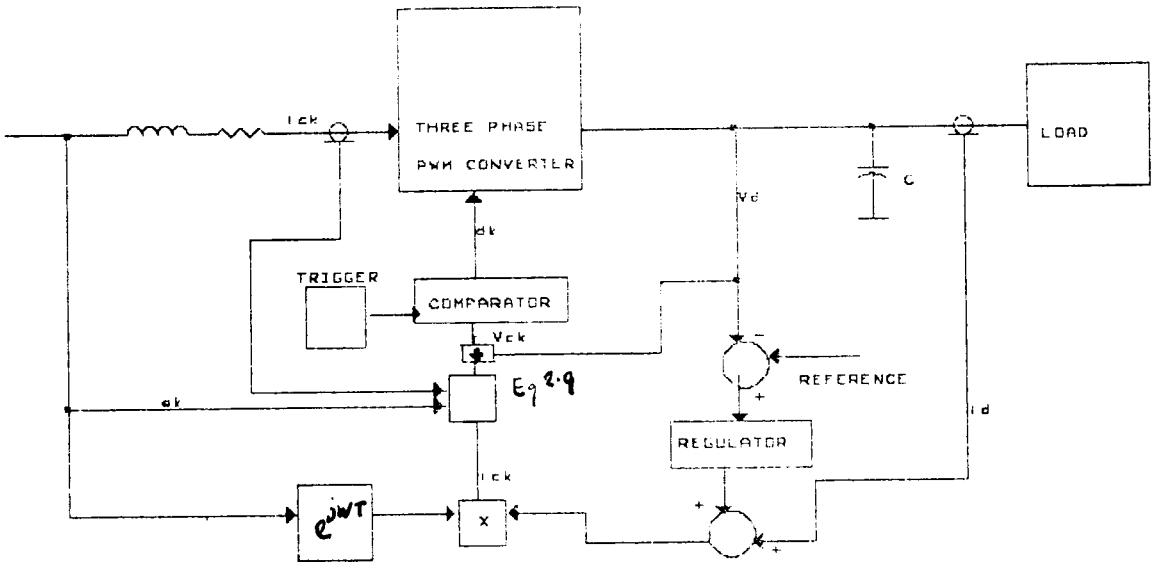
and

$$i_k + T*\frac{di_k}{dt} = i_{ck} \qquad (2.11)$$

This is a first order non homogenous equation of i_k

From the above equations, it can be seen that the line current i_k will follow the command current i_{ck} with a delay of one switching period T. Since this current command i_{ck} has the same shape as, and is in phase with, the supply voltage waveform, the line current is forced to vary sinusoidally with a unity power factor and the DC output voltage is maintained constant.

Circuit performance: The PWM AC to DC converter with PCFF control exhibits high power factor performance with low harmonics. There is a trade off in the area of circuit complexity and stability. Due to the closed loop nature of the control the operation is sensitive to parameter variation. However, it is most preferred in PWM rectifier and converter topologies. This particular topology also can not be very efficient because of the resistors put in front of the bridge switches to limit the current through the switches.



Control Circuit of the PCFF Scheme

Figure 2.8

(4) Hysteresis Current Controlled PWM Rectifier

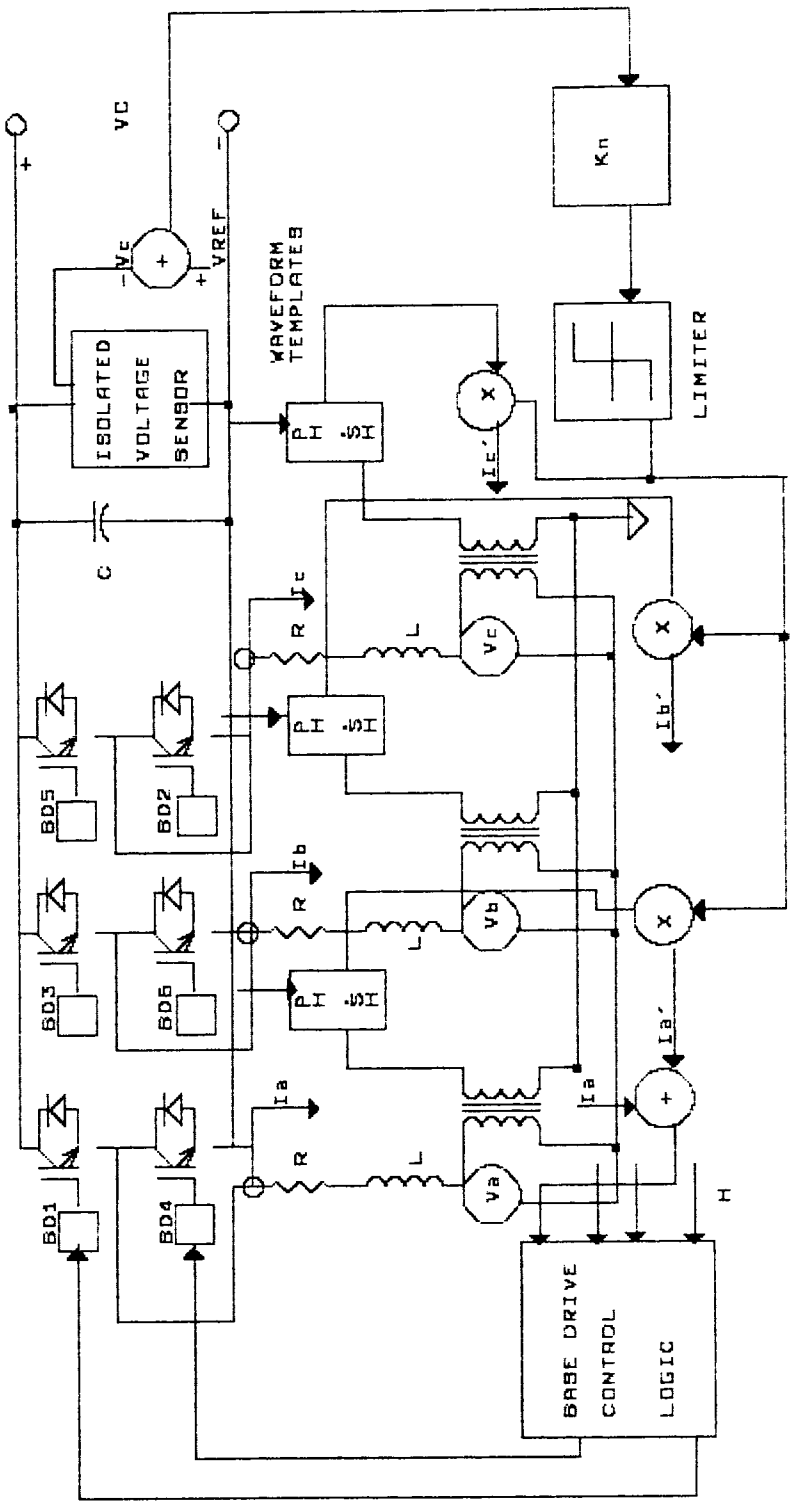
There is a variety of current controlled PWM rectifiers available today, but the most basic topology is as shown in Figure 2.9. The power electronics switch utilized is an insulated gate bipolar transistor (IGBT).

Circuit operation: Current waveform templates are taken from voltage transformers, filtered and phase shifted. The template waveforms are then multiplied by gain control. These serve as the reference currents and they go into the hysteresis band controller (typically as shown in Figure 2.10) to control the switching pattern for the individual switches while ensuring currents measured by the transducers track the reference currents within a tolerance band. This scheme, unlike the PWM rectifier with constant switching discussed earlier, is a variable frequency operation. The frequency of operation is dependent on the portion of the reference waveform that is being tracked. This topology is very commonly used.

Circuit performance: Due to phase drift problems introduced by the hysteresis band control this scheme often does not operate at unity power factor without a versatile phase angle correction on the AC side. However, the harmonics performance is good.

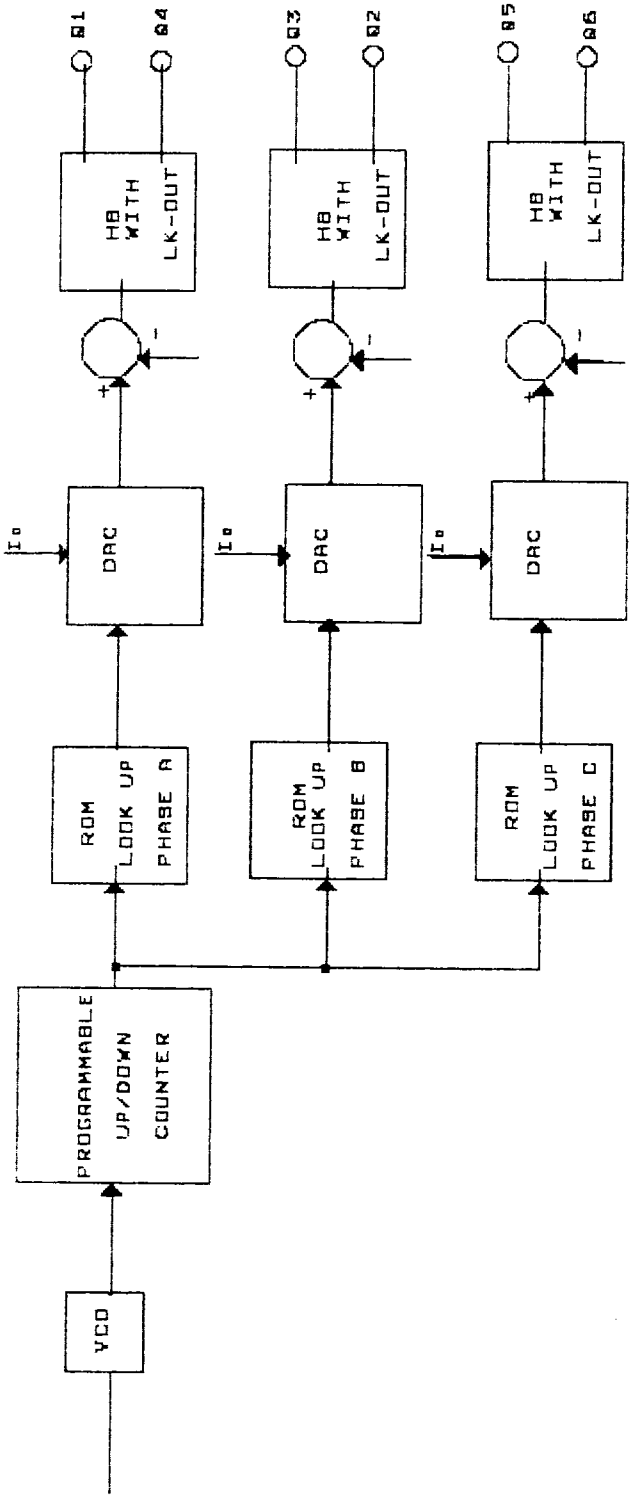
Due to the fact that each switch requires a local gate drive, the number of control components used in this scheme is high--a problem common to all PWM rectifier topologies.

(5) AC to DC Converter Topology by Mark Kocher et al [10] : The basic converter topology is shown in Figure 2.11. This is the well known flyback converter with the high frequency filter placed on the DC side of the bridge. The input current is controlled by varying the duty ratio. A block diagram of the overall control system can be seen in Figure 2.12. The line current is sensed and compared with a reference command obtained from the line voltage. The magnitude of the command current is controlled by the output DC voltage error which is obtained from the multiplier. The output voltage feedback is obtained through a resistive attenuator. The control circuit ground is tied solidly to the negative end of the load. Operation of the main switch is conducted at constant frequency with duty cycle modulation to shape the line current. Three-phase version of this scheme simply consists of three single-phase modules connected in parallel. The efficiency



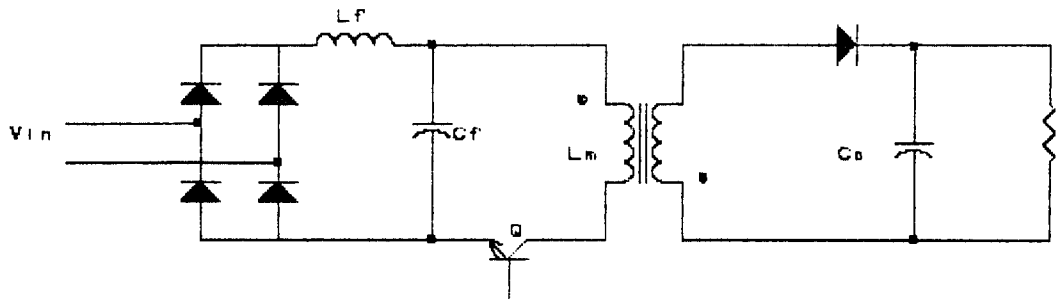
Main Circuit for the Hysteresis Current Controlled PWM Rectifier.

Figure 2.9



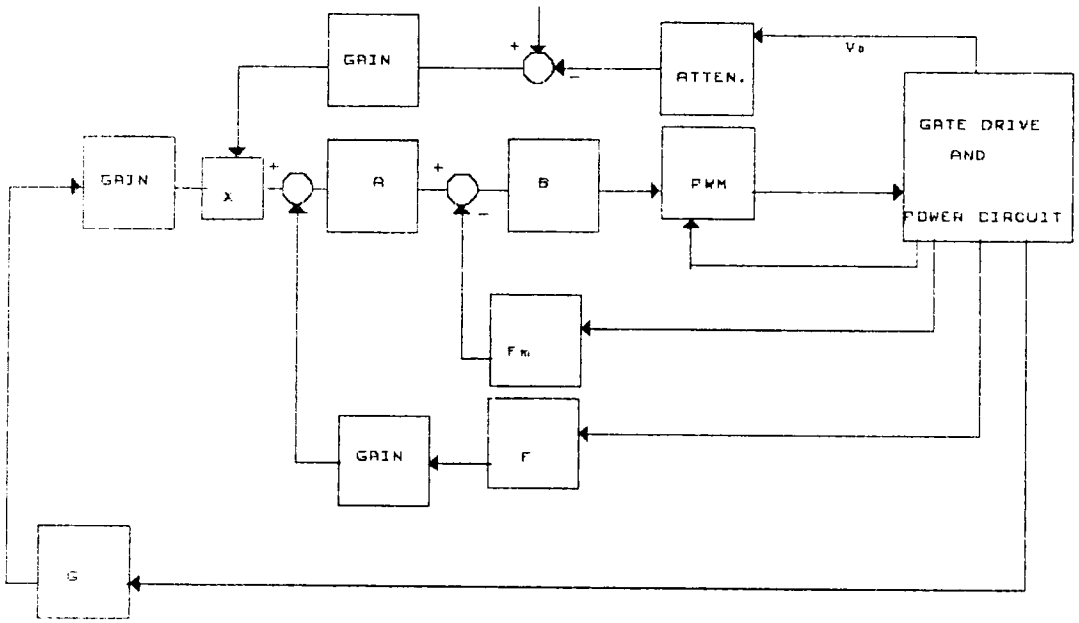
Hysteresis Band Control Block Diagram

Figure 2.10



Flyback Converter Topology

Figure 2.11



Control Block Diagram for the Flyback Converter

Figure 2.12

measured for this converter was low, possibly because the converter was tested at low power. The scheme exhibits good power factor performance. Power factor was about 0.96 and efficiency was about 60 percent. The power electronic switch gives the most losses in this scheme. Due to the closed loop control this scheme is very sensitive to parameter variation. This scheme also experiences instability near the zero crossing.

The Ziogas scheme has been selected as most promising considering the topologies discussed above, with regards to cost, unity power factor operation, line harmonics and stability. This scheme, however, also has the disadvantage of huge current stress on circuit components (especially on the boost switch), which consequently gives rise to poor efficiency. This thesis seeks to enhance this scheme by reducing current stress on the main switch through incorporation of a DC link inductor and consequently improve efficiency.

Chapter 3

Modified Topology

3.1 Introduction to Modified Topology

Abbreviations and Symbols.

Vl = Voltage drop across DC link inductance

Vph = Phase voltage

Vcp= Capacitor voltage

I_d = DC link current

Ls = AC side boost inductor

Lthk = Thevenin inductance as seen by voltage k (generic naming)

The on state conduction loss of the mosfet is determined by the expression

$$Pon = I_d^2 Rds$$

Ways by which one can reduce this on state conduction loss are to use low Rds device and to reduce the peak value of the I_d (and consequently ave.I_d).

In low voltage applications the new generations of power mosfet have very low on state resistance and very nearly model an ideal switch. However, with high voltage devices (like those used in switch mode power supplies and PLC) comparatively higher on state resistance still limits the mosfet efficiency. Furthermore, further decreases in Rds are virtually impossible due to limits set by geometry of the optimum cell and the resistivity of the N-epi layer. The second option is particularly viable for the currently discussed power line conditioning application where peak current could be 10 p.u. of the load current. One simple way to accomplish this is by the DC link inductance. The DC link inductance plays the important role of turn-on snubber for the mosfet thereby reducing the switching losses of the power electronic switch. Because the drawn input current is lower with the introduction of the DC link inductance, the mosfet mean life before failure time not only improves (due to reduced current stress), but its efficiency also improves (due to reduced on state losses).

Experimentation has shown that for a small amount of Ld (DC link inductance), the efficiency of the enhanced topology is better than that of its older scheme, while maintaining the sinusoidal quality of the input currents, improving the unity power factor operation and producing a regulated DC output supply. The new enhanced topology can be seen in Figure 3.1.

3.2 Circuit operations

This scheme loses phase independence by the incorporation of the DC link inductor, but maintains sinusoidal current shape by preserving discontinuous conduction of I_d current similar to the Ziogas scheme. When the switch is turned on, the equivalent circuit is as shown in Figure 3.2. Due to the small value of the Ld, the three phases remain virtually shorted as in the Ziogas scheme. The governing equations can be written from the superposition theorem as follows

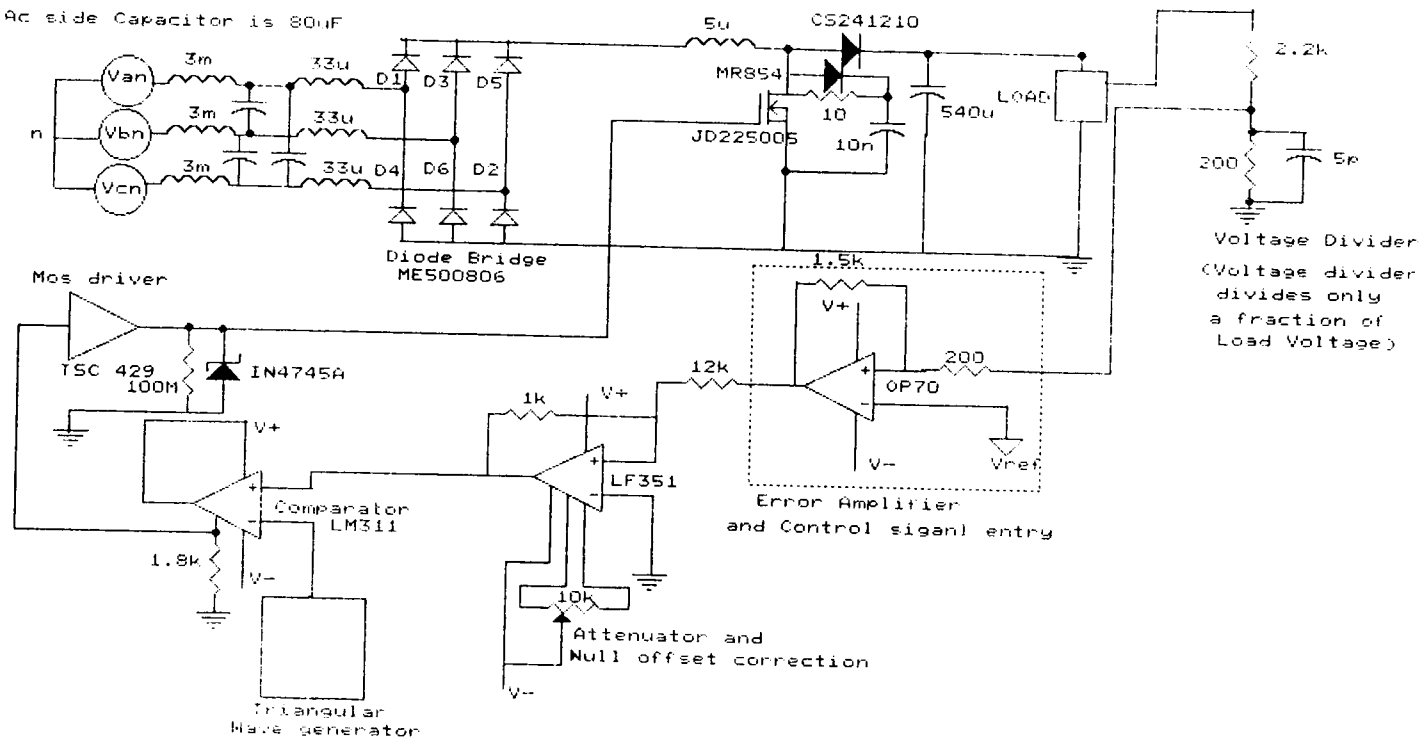
During turn-on

$$i_a(\omega t) = \left[\frac{v_{an}}{Ltha} - \frac{Ls+Ld}{2Ls+Ld}*\left[\frac{v_{cn}}{Lthc}\right] - \frac{v_{bn}}{2Lthb}\right]*t \qquad (3.1)$$

During turn-off

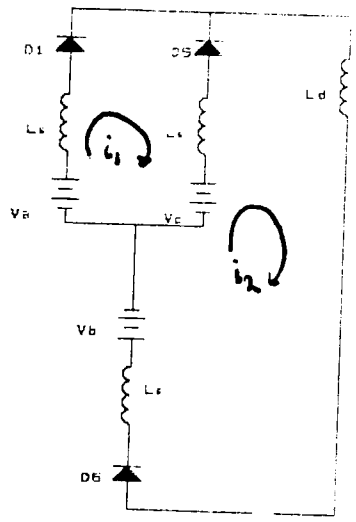
$$i_a(\omega t) = \left[\frac{v_{an}}{Ltha} - \frac{Ls+Ld}{2Ls+Ld} * \left[\frac{v_{cn}}{Lthc}\right] - \frac{v_{bn}}{2Lthb}\right]*t - \frac{Vcp}{Lthcp} * \frac{(t-t_1)}{2} \qquad (3.2)$$

At turn-off the DC link inductance would tend to dissipate stored energy to the load and depending on the duty cycle ratio, can either boost the load voltage until subsequent turn-on or dry out. At 0.5 duty ratio, however, no net energy is stored in the DC link inductance after turn-on and turn-off. This is the ideal operating point for this scheme, because it ensures that at any instance of turn-on, the voltage drop across the DC link inductance Ld is always the same value and nearly zero. This preserves the simultaneous operation of the three phases. The turn-off equivalent is as shown in Figure 3.3.



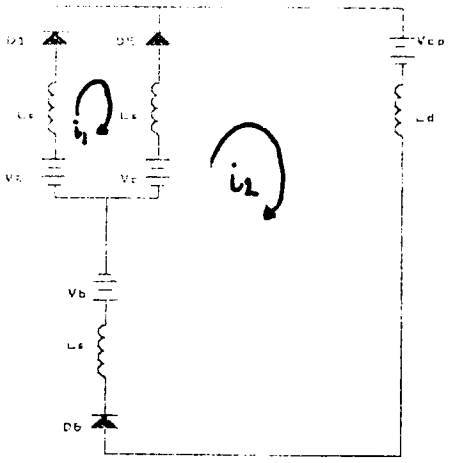
Schematic of Modified Topology (Complete Circuit)

Figure 3.1



Equivalent Circuit When Switch is on

Figure 3.2



Equivalent Circuit When Switch is off

Figure 3.3

Chapter 4

Analysis

4.1 Circuit Analysis

The underlying assumption for this analysis is that the Circuit operation is quasi-static. This is to say that the source voltage changes slowly enough that it may be considered fixed for an instant in time. This assumption is valid when the 60Hz time frame is compared to the 25kHz switching frequency.

4.2 PieceWise Analysis

The following section examines a piecewise analysis of the AC line current responses, the DC side current response, and the predicted harmonic pattern established by the recently explained operation.

To examine Circuit operation, position 1 is chosen. (See Figure 4.1.) This position is examined using transient signal analysis principle.

Suppose

$Va = 100$

$Vc = 100$

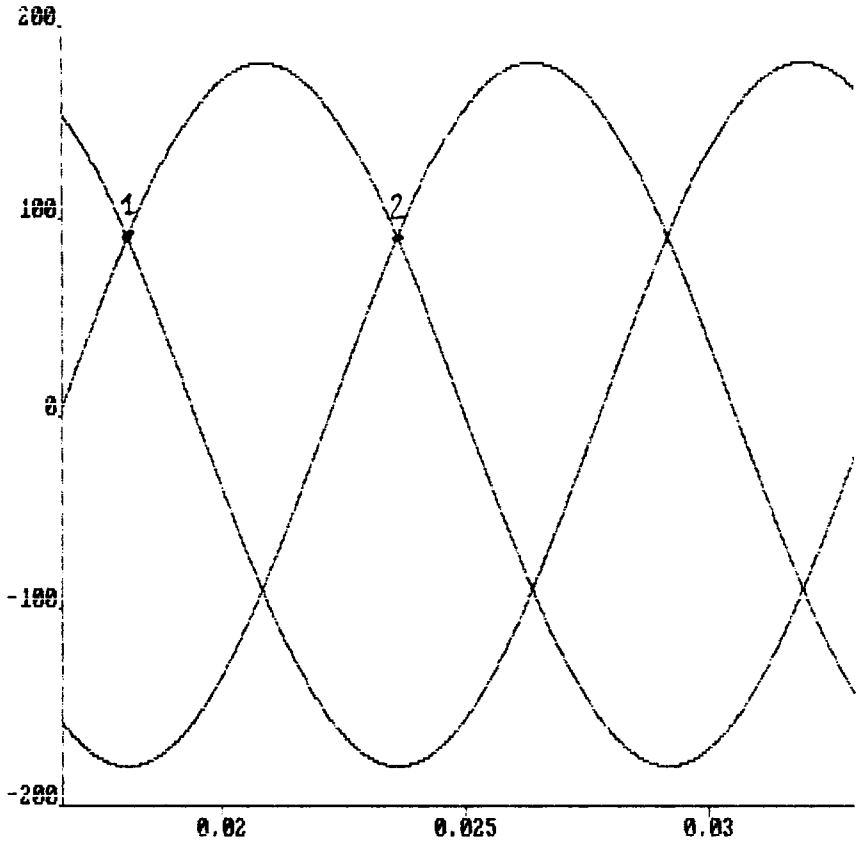
$Vb = -200$

$Vcp = 600$

Also choosing

$Ls = 50\mu H$

$Ld = 5\mu H$



Three Phase AC Voltage Waveforms Showing the two Piecewise Analysis Points

Figure 4.1

From the turn-on schematic in Figure 3.2

$$Ls\frac{di_1}{dt} + Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = Va - Vc \quad (4.1)$$

$$Ls[2\frac{di_1}{dt} - \frac{di_2}{dt}] = 100 - 100 \quad (4.2)$$

Ls is not equal to zero, hence

$$2\frac{di_1}{dt} = \frac{di_2}{dt} \quad (4.3)$$

$$Ls\frac{di_2}{dt} - Ls\frac{di_1}{dt} + Ld\frac{di_2}{dt} + Ls\frac{di_2}{dt} = Vc - Vb \quad (4.4)$$

$$[2Ls + Ld]\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Vc - Vb \quad (4.5)$$

Substituting eqn (4.3) into eqn (4.5),

$$[3Ls + 2Ld]\frac{di_1}{dt} = Vc - Vb \quad (4.6)$$

Substituting values

$$[3*50*10^{-6} + 2*5*10^{-6}]\frac{di_1}{dt} = 300$$

$$\frac{di_1}{dt} = 1.86*10^6 \text{ A/s}$$

From eqn (4.3)

$$\frac{di_2}{dt} = 3.75*10^6 \text{ A/s}$$

From the above expression for $\frac{di_2}{dt}$

$$Vl = Ld\frac{di_2}{dt} = 5*10^{-6}*3.75*10^6 = 18.75V$$

From the above solution Va = Vc » Vl, hence Va and Vc will conduct simultaneously.

At point 1 turn-off as usual Va = Vc

$$Ls\frac{di_1}{dt} + Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = Va - Vc \quad (4.7)$$

$$2Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = 0 \quad (4.8)$$

$$2\frac{di_1}{dt} = \frac{di_2}{dt} \tag{4.9}$$

$$Ls\frac{di_2}{dt} - Ls\frac{di_1}{dt} + Ld\frac{di_2}{dt} + Vcp + Ls\frac{di_2}{dt} = Vc - Vb \tag{4.10}$$

$$[2Ls + Ld]\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Vc - Vb - Vcp \tag{4.11}$$

From (4.9)

$$[3Ls + 2Ld]\frac{di_1}{dt} = Vc - Vb - Vcp \tag{4.12}$$

Substituting values

$$\frac{di_1}{dt}(3 * 50 * 10^{-6} + 2 * 5 * 10^{-6}) = 200 + 100 - 600$$

$$\frac{di_1}{dt} (0.00016) = -300$$

$$\frac{di_1}{dt} = -1.86 * 10^6 \text{ A/s}$$

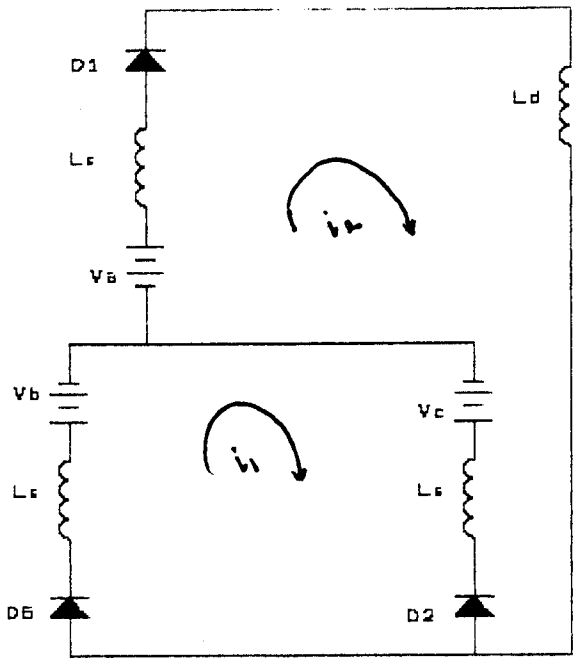
$$\frac{di_2}{dt} = -3.75\ 10^6 \text{ A/s}$$

This fall rate ensures that the current I_d reaches zero again before subsequent turn - on. Hence, the same AC response as indicated here is repeated for every switching period between wt = 0 and wt = 2π, with two conducting phases sharing either positive I_d or negative I_d. The above case is an example of positive I_d being shared. To show a case where negative I_d is being shared, point 2 will now be considered. Turn-on topology becomes as shown in Figure 4.2. Now Va is 200 V, Vb = -100V, Vc = -100V and Vcp = 600V.

$$Ls\frac{di_2}{dt} + Ld\frac{di_2}{dt} + Ls\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Va - Vc \tag{4.13}$$

$$2Ls\frac{di_2}{dt} + Ld\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Va - Vc \tag{4.14}$$

$$Ls\frac{di_1}{dt} + Ld\frac{di_1}{dt} - Ls\frac{di_2}{dt} = Vb - Vc \tag{4.15}$$



Equivalent Circuit When Switch is on (Position 2)

Figure 4.2

$$2Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = 0 \qquad (4.16)$$

$$2Ls\frac{di_1}{dt} = Ls\frac{di_2}{dt} \qquad (4.17)$$

Substituting eqn (4.17) into eqn (4.14)

makes

$$[3Ls+2Ld]\frac{di_1}{dt} = Va - Vc \qquad (4.18)$$

Substituting values

$$\frac{di_1}{dt}(3 * 50 * 10^{-6} + 2 * 5 * 10^{-6}) = 200 + 100$$

$$\frac{di_1}{dt}(160 * 10^{-6}) = 300$$

$$\frac{di_1}{dt} = 1.86 * 10^6 \text{ A/s}$$

$$\frac{di_2}{dt} = 3.75 * 10^6 \text{ A/s}$$

At turn-off the topology becomes as shown in Figure 4.3 and the circuit analysis is as follows:

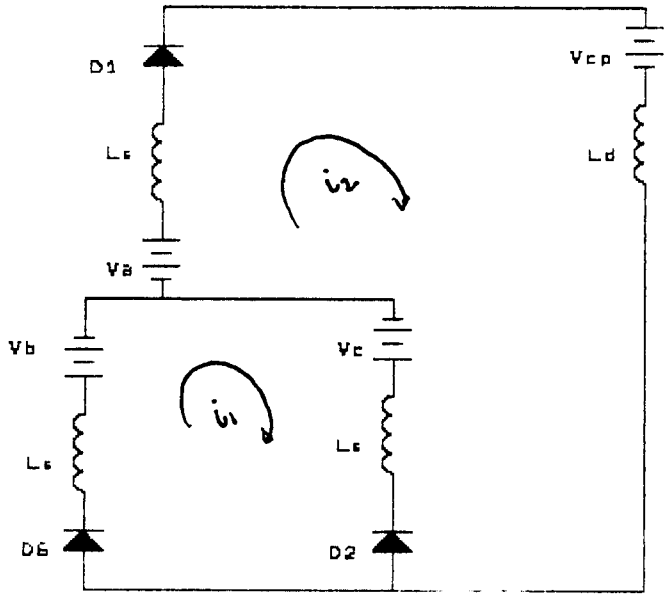
$$Ls\frac{di_2}{dt} + Ld\frac{di_2}{dt} + Ls(di_2,dt) - Ls\frac{di_1}{dt} = Va - Vc - Vcp \quad (4.19)$$

$$2\,Ls\frac{di_2}{dt} + Ld\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Va - Vc - Vcp \quad (4.20)$$

$$[2Ls + Ld]\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Va - Vc - Vcp \quad (4.21)$$

$$Ls\frac{di_1}{dt} + Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = Vb - Vc \quad (4.22)$$

$$2Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = Vb - Vc \quad (4.23)$$



Equivalent Circuit When Switch is Off (Position 2)

Figure 4.3

$$2Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = 0 \qquad (4.24)$$

$$2Ls\frac{di_1}{dt} = Ls\frac{di2}{dt} \qquad (4.25)$$

Substituting (4.25) into (4.21)

$$\frac{di_1}{dt}[3Ls + 2Ld] = Va - Vc - Vcp \qquad (4.26)$$

Substituting values

$$\frac{di_1}{dt}(3 * 50 * 10^{-6} + 2 * 5 * 10^{-6}) = 100 + 200 - 600$$

$$\frac{di_1}{dt}(0.00016) = -300$$

$$\frac{di_1}{dt} = -1.86\ 10^6\ A/s$$

$$\frac{di_2}{dt} = -3.75\ 10^6\ A/s$$

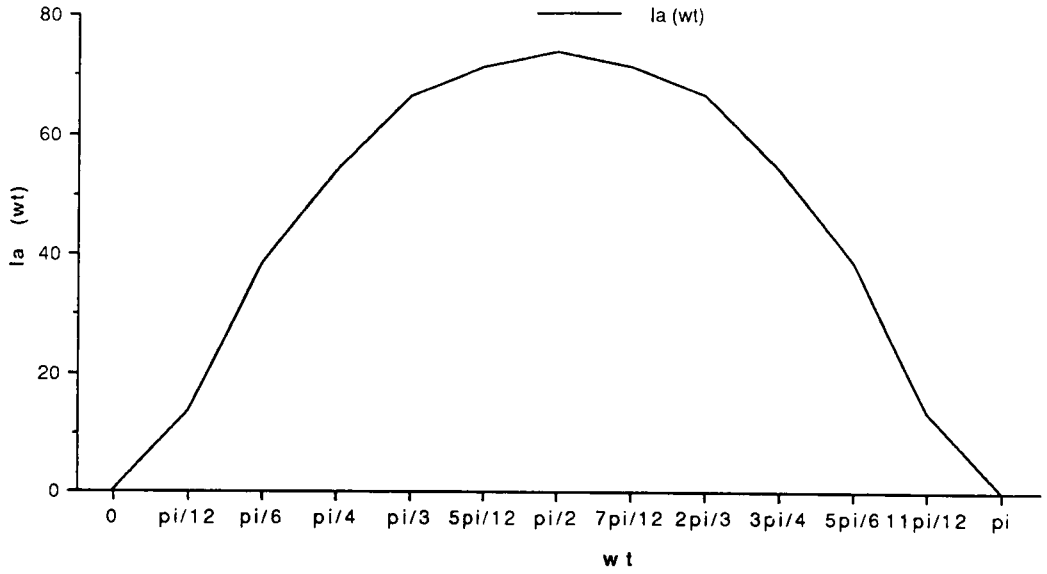
This is as already established in position 1.

Doing a piecewise analysis on a few points along the 60 Hz frame yields the following peak line currents. (Table 1 contains only half a cycle.) With a very high Vcp one can approximate the fall to be instantaneous. Plotting i_a (ωt) from Table 1, produces the following figure in Figure 4.4.

Table 1

Peak $i_a(\omega t)$ at Certain Points Along the 60Hz Frame

v_{an}	ωt	peak turn-on i_a (ωt)
0	0	0
51.8	pi/12	13.46
101.1	pi/6	38.09
143.6	pi/4	53.71
173.2	pi/3	66.19
192.1	5pi/12	71.11
200	pi/2	73.79
192.1	7pi/12	71.11
173.2	2pi/3	66.19
143.6	3pi/4	53.71
101.1	5pi/6	38.09
51.8	11pi/12	13.46
0	pi	0



Plot of $i_a(\omega t)$ Peak Profile from Table 1

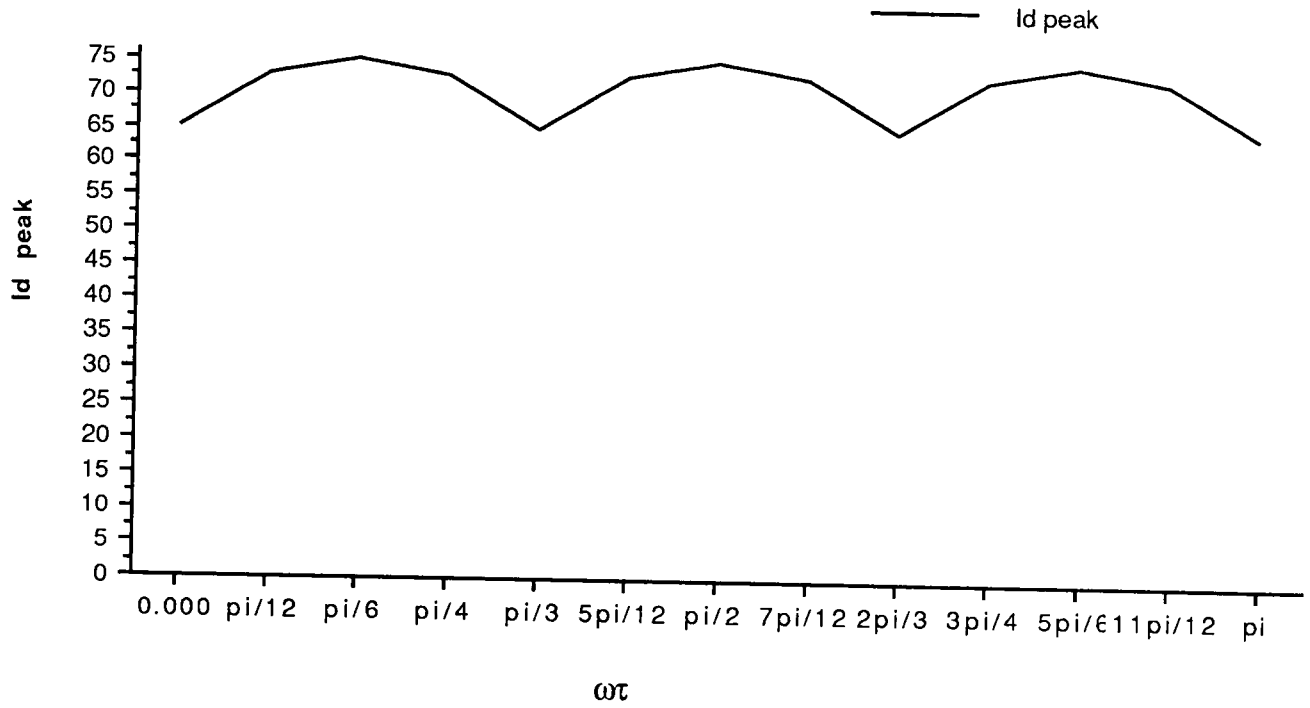
Figure 4.4

4.2.1 DC Current Response

From the conduction sequence (Table 2) and the circuit analysis at the above 13 instants, Table 3 is a list of peaks for the I_d currents for the same half cycle of the phase current. Figure 4.5 shows a projected waveform of I_d fabricated from Table 3. See appendix for computational examples for the I_d peak current. The fall of I_d and, consequently, the fall of line currents should be at least as steep or steeper than their rise. This is accomplished by setting Vcp, which is the DC link capacitor voltage, sufficiently high. For our current piecewise analysis, these rates of change are set equal to each other. As already explained this is the absolute boundary of operation of this type of PLC.

4.2.2 Harmonic Pattern

It is important at this juncture to explain that the current waveforms (both line currents and the DC link current) have similar appearances to those of the Ziogas scheme. However, the critical difference is that magnitudes of peak currents for the same output power are reduced. This lessens the current stress on major devices. The total harmonics distortion factors of both schemes are comparable.



Plot of Peak I_d Current Profile from Table 3

Figure 4.5

Table 2

Table of Phase Voltage Values and Conduction Sequence for I_d peak Computation

ωt	|Va|	|Vb|	|Vc|	Conduction sequence
0(+)	0	173.2	173.2	Va,Vc/Vb
pi/12	51.8	193.2	141.4	Va,Vc/Vb
pi/6	100	200	100	Va,Vc/Vb
pi/4	141.4	193.2	51.8	Va,Vc/Vb
pi/3	173.2	173.2	0	Va,Vc/Vb
5pi/12	193.2	141.4	51.8	Va/Vb,Vc
pi/2	200	100	100	Va/Vb,Vc
7pi/12	193.2	51.8	141.4	Va/Vb,Vc
2pi/3	173.2	0	173.2	Va/Vb,Vc
3pi/4	141.4	51.8	193.2	Va,Vb/Vc
5pi/6	100	100	200	Va,Vb/Vc
11pi/12	51.8	141.4	193.2	Va,Vb/Vc
pi	0	173.2	173.2	Va,Vb/Vc

Table 3

Peak I_d Current Values for a Few Points Along the 60Hz Frame

ωt	I_d peak
0	65
pi/12	72.5
pi/6	75
pi/4	72.5
pi/3	65
5pi/12	72.5
pi/2	75
7pi/12	72.5
2pi/3	65
3pi/4	72.5
5pi/6	75
11pi/12	72.5
pi	65

Chapter 5

Computer Analysis

This simulation was conducted in order to cover details that could not be presented in the piecewise analysis. Simulations were made to thoroughly investigate all circuit responses. The software used was SIMNON. The figures in this chapter show line current waveforms, DC current waveform, Vds voltage waveform and Vload waveform. The simulation and analysis assume ideal diodes and switches. This is considered a fair assumption, since only their switching characteristics are utilized in the current application and that occurs at a much faster speed than our operation. See appendix for simulation program.

5.1 Simulation Studies

The following will be discussed in this chapter with regards to the simulation of the modified topology in chapter 3.

(1) The modeling of the switching action.
(2) The modeling of I_d (DC link current) response.
(3) The modeling of AC line currents response.
(4) The modeling of DC link capacitor voltage.
(5) Parameters and parameter variation.
(6) Simulation results.

Abbreviation and Symbols

I_{11} = Capacitor charging current when s<0
I_2 = Load current
v_{an} = Instantaneous phase A voltage
v_{bn} = Instantaneous phase B voltage
v_{cn} = Instantaneous phase C voltage
Vdl = Capacitor voltage
t = Any time t within the switching interval
t_1 = Maximum 'on' time
$i_a(wt)$ = Instantaneous phase A current at angular interval wt

I_d = DC link current

i_a = Instantaneous phase A line current

i_b = Instantaneous phase A line current

i_c = Instantaneous phase A line current

Ls = AC side boost inductor

Ld = DC link boost inductor

s = Switching logic assigned variable

Per = Period of switching

T = Simulation time t

Vrl = Switch voltage. In the case of the mosfet it would be referred to as Vds

Vd = Load voltage

5.1.1 Modeling of the Switching Action

What is desired in this simulation is an 'on', 'off' action that connects and disengages the capacitor voltage from the leg of the boost inductor Ld. For this, the following command was used

$$s = \text{if}(\text{mod } T, Per) < \frac{per}{2} \text{ then } 1 \text{ else } -1$$

Where s=1 is the 'on' state

s=-1 is 'off' state.

The above switch command generates a square wave which is made logically equivalent to the turn-on and turn-off of the power switch by the command

Vrl = If s>0 then 0 else Vd

Where Vd is the capacitor voltage.

5.1.2 Modeling of I_d(DC Link Current) Response

The topology being considered has two basic generic 'on' state schematics as can be seen in Figures 3.2 and 4.1. There are also two basic generic 'off' state schematics as can be seen in Figures 3.3 and 4.2. The AC sources rotate positions in this schematic every 60°. To investigate the response of the DC link current, these schematics are utilized.

The current response is derived using the superposition principle. This section will go through the derivations for one 60° interval but will present the remaining intervals.

Considering the interval $0 < wt < 60°$

See Figures 5.1 a, b and c as they explain the succeeding operations

The Thevenin impedance from Va position is

$(Ls+Ld)//Ls + Ls = 76.19*10^{-6}$ Henrys

Writing a loop equation

$$\frac{di_a}{dt} = \frac{v_{an}}{76.19*10^{-6}} \tag{5.1}$$

Since rate of change can be treated linearly in this case

$$\frac{dI_d}{dt} = \frac{50}{50+55} * \frac{v_{an}}{76.19*10^{-6}} \tag{5.2}$$

Response due to Vc

Thevenin impedance still remains the same as in Va

So,

$$\frac{di_c}{dt} = \frac{v_{cn}}{76.19*10^{-6}} \tag{5.3}$$

and

$$\frac{dI_d}{dt} = \frac{50}{50+55} * \frac{v_{cn}}{76.19*10^{-6}} \tag{5.4}$$

Response due to Vb

The Thevenin impedance is derived as

$(Ls+Ld)+(Ls//Ls) = 80*10^{-6}$ Henrys Therefore

$$\frac{dI_d}{dt} = \frac{v_{bn}}{80*10^{-6}} \tag{5.5}$$

Response due to Vcp (which is the capacitor voltage)

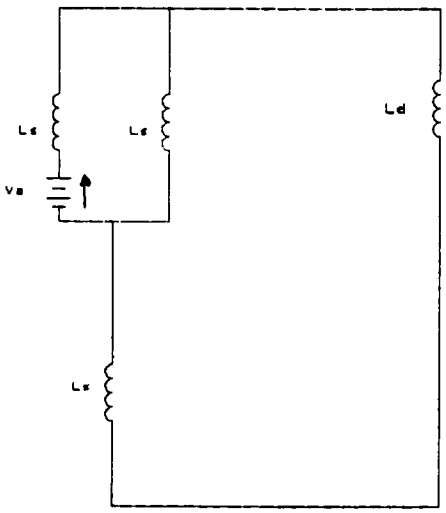
The Thevenin impedance is as in the Vb response. See Figure 5.1d. The positive flow of current is as shown in the figures.

$$\frac{dI_d}{dt} = \frac{v_{en}}{80*10^{-6}} \tag{5.6}$$

Total I_d response for the time interval $0<wt<60°$ is

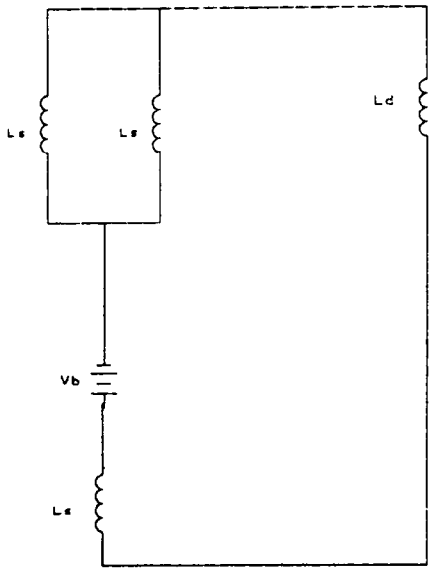
therefore

$$\frac{dI_d}{dt} = \frac{50}{50+55} * \left[\frac{v_{an}+v_{cn}}{76.19*10^{-6}}\right] - \frac{v_{bn}}{80*10^{-6}} - \frac{v_{en}}{80*10^{-6}} \tag{5.7}$$



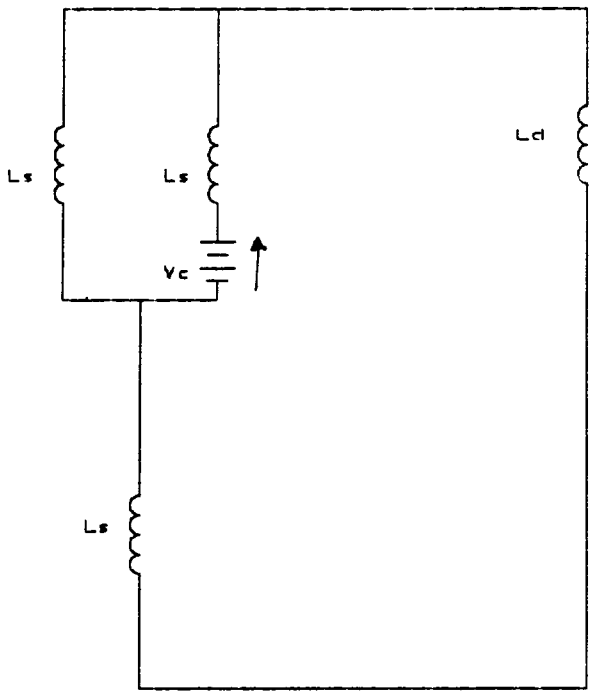
a

I_d Modeling-Va



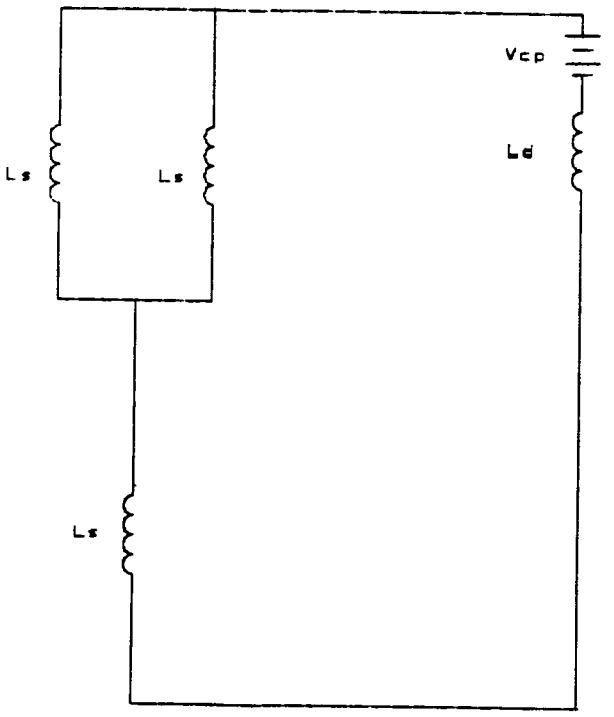
b

I_d Modeling-Vb



c

I_d Modeling-Vc



d

I_d Modeling-Vcp

Figure 5.1

Schematics for Modeling Showing the Sources Acting Individually for Angular Interval $0<\omega t<60°$

Total I_d response for the time interval 60°<wt<120° is

$$\frac{dI_d}{dt} = \frac{v_{an}}{80*10\text{-}6} - \frac{50}{50+55} * \left[\frac{v_{bn}+v_{cn}}{76.19*10\text{-}6}\right] - \frac{v_{en}}{80*10\text{-}6} \qquad (5.8)$$

Total I_d response for the time interval 120°<wt<180° is

$$\frac{dI_d}{dt} = \frac{50}{50+55} * \left[\frac{v_{an}+v_{bn}}{76.19*10\text{-}6}\right] - \frac{v_{cn}}{80*10\text{-}6} - \frac{v_{en}}{80*10\text{-}6} \qquad (5.9)$$

Total I_d response for the time interval 180°<wt<240° is

$$\frac{dI_d}{dt} = \frac{v_{bn}}{80*10\text{-}6} - \frac{50}{50+55} * \left[\frac{v_{an}+v_{cn}}{76.19*10\text{-}6}\right] - \frac{v_{en}}{80*10\text{-}6} \qquad (5.10)$$

Total I_d response for the interval 240°<wt<300° is

$$\frac{dI_d}{dt} = \frac{50}{50+55} * \left[\frac{v_{bn}+v_{cn}}{76.19*10\text{-}6}\right] - \frac{v_{an}}{80*10\text{-}6} - \frac{v_{en}}{80*10\text{-}6} \qquad (5.11)$$

Total I_d response for the interval 300°<wt<360° is

$$\frac{dI_d}{dt} = \frac{v_{cn}}{80*10\text{-}6} - \frac{50}{50+55} * \left[\frac{v_{an}+v_{bn}}{76.19*10\text{-}6}\right] - \frac{v_{en}}{80*10\text{-}6} \qquad (5.12)$$

Using a joining command in SIMNON the whole response for a 60Hz cycle can be seen . The section on simulation results will present this.

5.1.3 Modeling of the AC Line Currents

The derivation of current response in this section will be as in the DC current response. The current expression is derived from superposition principle. To illustrate the modeling of AC line current for simulation, only phase A will be discussed. Necessary figures are Figures 5.2 to 5.7. As in the case of I_d response, the intervals after the first interval 0<wt<60° only will be presented.

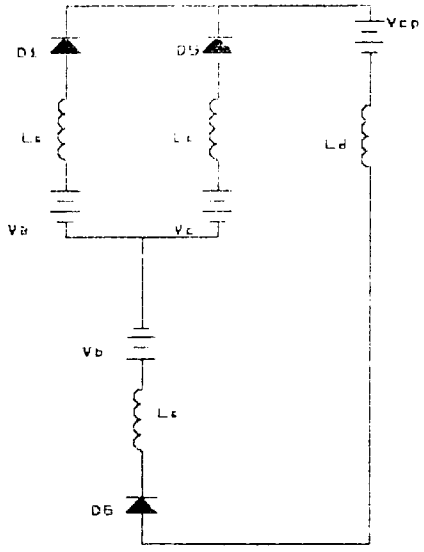
Within the angular interval 0<wt<60° at turn-on the schematic is as shown in Figures 5.5. Maintaining Ls = 50 μH and Ld = 5 μH and evaluating the circuit with only Va in the circuit gives

$$\frac{di_a}{dt} = \frac{v_{an}}{76.19*10\text{-}6} \qquad (5.13)$$

Response due to Vcp

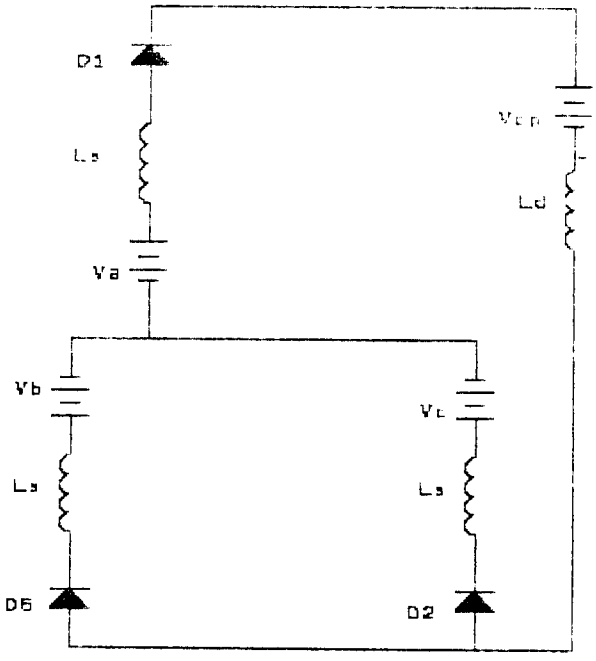
$$\frac{di_a}{dt} = \frac{v_{en}}{(2*80*10\text{-}6)} \qquad (5.14)$$

Response due to Vc



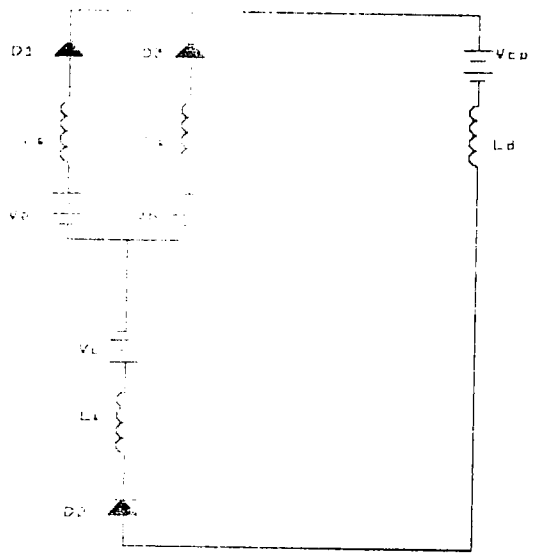
Schematic Within 0<ωt<60°

Figure 5.2



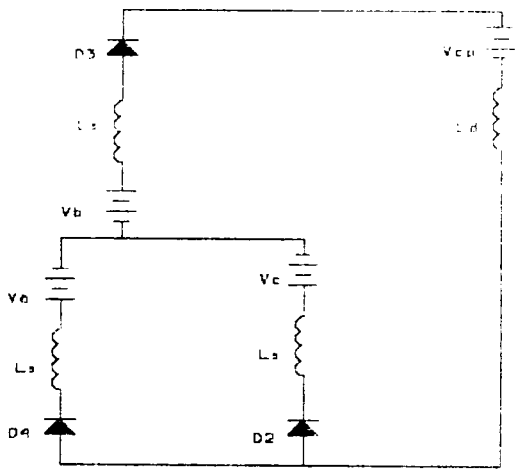
Schematic Within 60°<ωt<120°

Figure 5.3



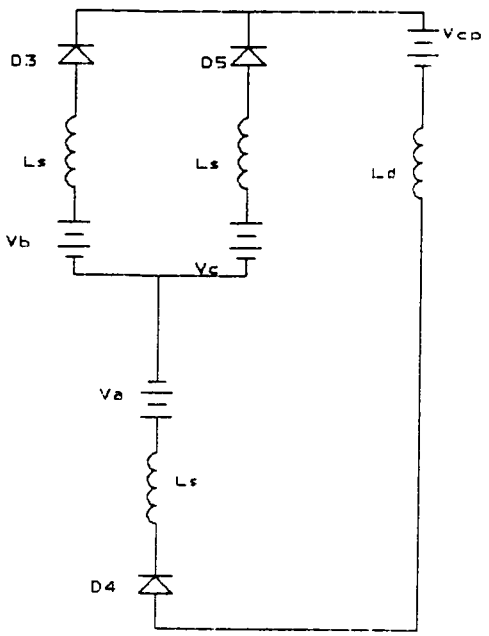
Schematic Within 120°<ωt<180°

Figure 5.4



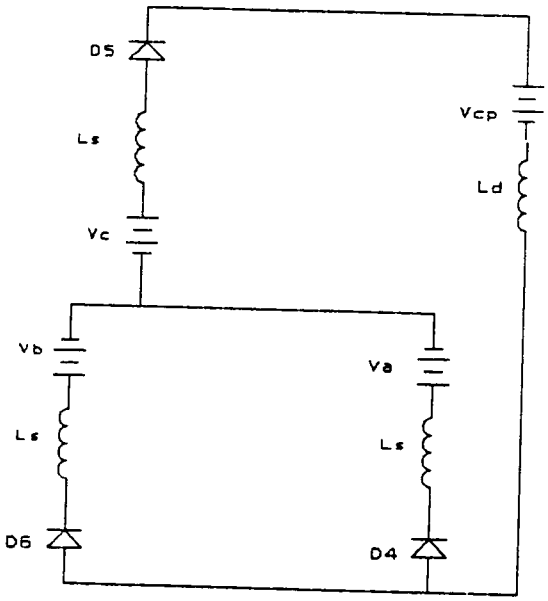
Schematic for Within 180°<ωt<240°

Figure 5.5



Schematic for 240°<ωt<300°

Figure 5.6



Schematic for 300°<ωt<360°

Figure 5.7

$$\frac{di_a}{dt} = [\frac{50}{50+55}]\frac{v_{cn}}{76.19*10\text{-}6} \quad (5.15)$$

Response due to Vb

$$\frac{di_a}{dt} = \frac{v_{bn}}{80*10\text{-}6} \quad (5.16)$$

Total response of I_a for angular interval 0<wt<60°

$$\frac{di_a}{dt} = \frac{v_{an}}{76.19*10\text{-}6} - \frac{55}{105}\,[\frac{v_{an}}{76.19*10\text{-}6}] - \frac{1}{2}[\frac{v_{en}}{80*10\text{-}6}] - \frac{1}{2}[\frac{v_{bn}}{80*10\text{-}6}] \quad (5.17)$$

Total response of Ia

Within interval 60°<wt<120°

$$\frac{di_a}{dt} = \frac{v_{an}}{80*10\text{-}6} - \frac{v_{en}}{80*10\text{-}6} - \frac{50}{105}[\frac{v_{cn}+v_{bn}}{76.19*10\text{-}6}] \quad (5.18)$$

Within 120°<wt<180°

$$\frac{di_a}{dt} = \frac{v_{an}}{76.19*10\text{-}6} - \frac{55}{105}[\frac{v_{bn}}{76.19*10\text{-}6}] - \frac{1}{2}[\frac{v_{en}+Vc}{80*10\text{-}6}] \quad (5.19)$$

Within 180°<wt<240°

$$\frac{di_a}{dt} = \frac{v_{an}}{76.19*10\text{-}6} - \frac{55}{105}[\frac{v_{cn}}{76.19*10\text{-}6}] - \frac{1}{2}[\frac{v_{bn}}{80*10\text{-}6} + \frac{v_{en}}{2*80*10\text{-}6}] \quad (5.20)$$

Within 240°<wt<300°

$$\frac{di_a}{dt} = \frac{v_{an}}{80*10\text{-}6} - \frac{50}{105}[\frac{v_{bn}+v_{cn}}{76.19*10\text{-}6}] + \frac{v_{en}}{80*10\text{-}6} \quad (5.21)$$

Within 300°<wt<360°

$$\frac{di_a}{dt} = \frac{v_{an}}{76.19*10\text{-}6} - \frac{55}{105}\left[\frac{v_{bn}}{76.19*10\text{-}6}\right] + \frac{1}{2}\left[\frac{v_{en}}{80*10\text{-}6}\right] - \frac{1}{2}\left[\frac{v_{cn}}{80*10\text{-}6}\right] \quad (5.22)$$

Phases B and C responses are listed for the same mentioned interval.

0<wt<60°

$$\frac{di_b}{dt} = \frac{v_{bn}}{80*10\text{-}6} + \frac{v_{en}}{80*10\text{-}6} - \frac{50}{105}\left[\frac{v_{an}+v_{cn}}{76.19*10\text{-}6}\right] \quad (5.23)$$

$$\frac{di_c}{dt} = \frac{v_{cn}}{76.19*10\text{-}6} - \frac{55}{105}\frac{v_{an}}{76.19*10\text{-}6} - \frac{1}{2}\left[\frac{v_{en}+v_{bn}}{80*10\text{-}6}\right] \quad (5.24)$$

60°<wt<120°

$$\frac{di_b}{dt} = \frac{v_{bn}}{76.19*10\text{-}6} - \frac{55}{105}\left[\frac{v_{cn}}{76.19*10\text{-}6} - \left[\frac{v_{an}-v_{en}}{2*80*10\text{-}6}\right]\right. \quad (5.25)$$

$$\frac{di_c}{dt} = \frac{v_{cn}}{76.19*10\text{-}6} - \frac{55}{105}\left[\frac{v_{bn}}{76.19*10\text{-}6}\right] - \frac{1}{2}\left[\frac{v_{an}-v_{en}}{80*10\text{-}6}\right] \quad (5.26)$$

120°<wt<180°

$$\frac{di_b}{dt} = \frac{v_{bn}}{76.19*10\text{-}6} - \frac{55}{105}\left[\frac{v_{an}}{76.19*10\text{-}6} - \frac{1}{2}\left[\frac{v_{en}+v_{cn}}{80*10\text{-}6}\right]\right. \quad (5.27)$$

$$\frac{di_c}{dt} = \frac{v_{cn}}{80*10\text{-}6} - \frac{50}{105}\left[\frac{v_{an}+v_{bn}}{76.19*10\text{-}6}\right] + \frac{v_{en}}{80*10\text{-}6} \quad (5.28)$$

180°<wt<240°

$$\frac{di_b}{dt} = \frac{v_{bn}}{80*10\text{-}6} - \frac{50}{105}\left[\frac{v_{cn}+v_{an}}{76.19*10\text{-}6}\right] - \frac{v_{en}}{80*10\text{-}6} \quad (5.29)$$

$$\frac{di_c}{dt} = \frac{v_{cn}}{76.19*10\text{-}6} - \frac{55}{105}\frac{v_{an}}{76.19*10\text{-}6} - \left[\frac{v_{bn}-v_{en}}{2*80*10\text{-}6}\right] \quad (5.30)$$

240°<wt<300°

$$\frac{di_b}{dt} = \frac{v_{bn}}{76.19*10\text{-}6} - \frac{55}{105}\frac{v_{an}}{76.19*10\text{-}6} - \frac{1}{2}\left[\frac{v_{cn}-v_{en}}{80*10\text{-}6}\right] \quad (5.31)$$

$$\frac{di_c}{dt} = \frac{v_{cn}}{76.19*10\text{-}6} - \frac{55}{105}\frac{v_{bn}}{76.19*10\text{-}6} - \frac{1}{2}\left[\frac{v_{an}+v_{en}}{80*10\text{-}6}\right] \quad (5.32)$$

$300° < wt < 360°$

$$\frac{di_b}{dt} = \frac{v_{bn}}{76.19*10\text{-}6} - \frac{55}{105}\frac{v_{an}}{76.19*10\text{-}6} - \frac{1}{2}\left[\frac{v_{cn}-v_{en}}{80*10\text{-}6}\right] \quad (5.33)$$

$$\frac{di_c}{dt} = \frac{v_{cn}}{80*10\text{-}6} - \frac{v_{en}}{80*10\text{-}6} - \frac{50}{105}\left[\frac{v_{an}+v_{bn}}{76.19*10\text{-}6}\right] \quad (5.34)$$

As in the case of I_d response the intervals are joined in simulation to give a full-cycle response.

5.1.4 Modeling of the DC Link Capacitor Voltage

This is done knowing the load requirements. The rate of change of the voltage across the capacitor is given as

$$\frac{dVdl}{dt} = \frac{(I_{11}-I_2)}{C} \quad (5.35)$$

I_2 is the load current which is set by the load

I_{11} is the capacitor charging current when $s<0$ (That is, switch is off)

5.1.5 Parameters and Parameter Variation

The important condition for system stability is to match input power with output power in simulation since no power loss has been accounted for in the model. This is done by the I_2 current.

One important thing to do is to initialize capacitor voltage to some value at simulation start to avoid the startup spike in SIMNON. All specified parameters can be varied within the simulation run with the PAR command.

DC link capacitor Cp	540μF
Capacitor initial voltage Vdl	300V
Load current I2	5A
Input voltage amplitude	180V
Switching period	400μs

5.2 Simulation Results

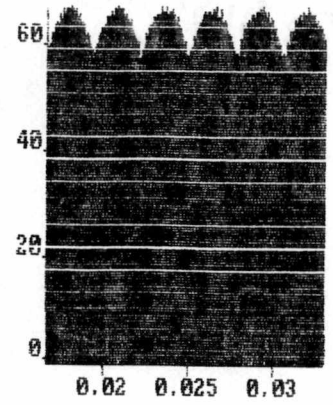
This section seeks to present the final results of the simulations and to comment on obtained waveforms.

DC Current Response: Figure 5.8a shows a waveform of DC current response for one cycle of the 60Hz time frame. The peak profile is directly related to the six schematics per cycle shown in Figures 5.2 through 5.7. The expanded version in Figure 5.9 shows discontinuous operation as designed.

AC Line Current Response: Figures 5.8b, c and d show phase A, phase B and phase C current waveforms respectively for 1 cycle of the fundamental frequency. This is for Ld of 5 μH. An expansion of phase A current confirms discontinuous conduction (as shown in Figure 5.10) Also shown is the phase A current waveform for Ld equal 0 μH in Figure 5.11. Of importance is the difference in peak i_a for the same load conditions. Phase A current peak for Ld = 0 μH is higher, which is due to the increased Thevenin impedance of the modified topology. Close examination of the two comparable waveforms reveals a 6.7 percent difference.

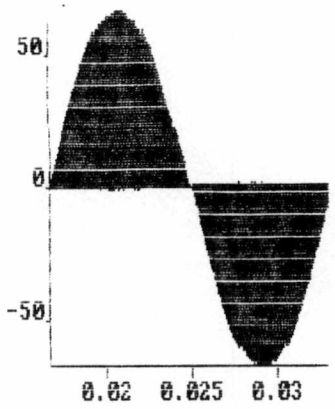
Vds Waveform: Figure 5.12 shows the voltage of the power switch for one cycle of AC line frequency. Along with this is Figure 5.13 showing its expanded version. The generation of the Vds waveform is related to the switch logic as modeled in the switching action. As can be observed from the expanded Vds waveform in Figure 5.13, there is a finite rise time in Vds because the rise to v_{en} can not be instantaneous in SIMNON. Additionally, the simulation step is of some finite value.

Vload: The DC output voltage of the designed power supply can be seen in Figure 5.20. The Vload steady state value is 1000V.



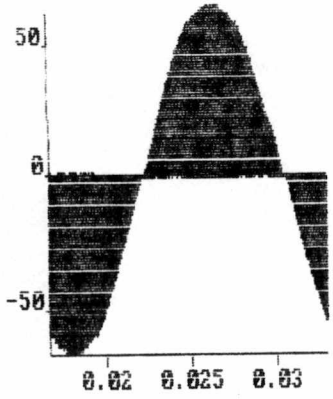
a

DC Current



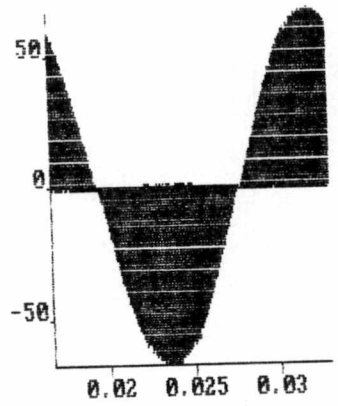
b

Phase A Current (1 cycle)



c

Phase B Current(1 cycle)

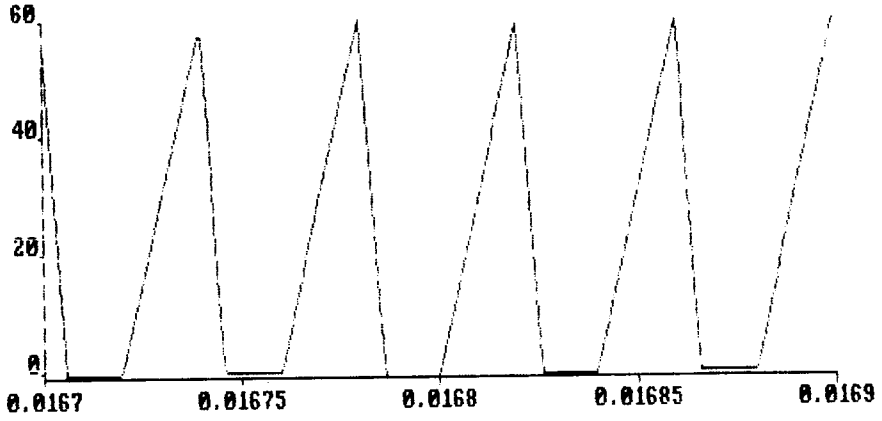


d

Phase C Current(1 cycle)

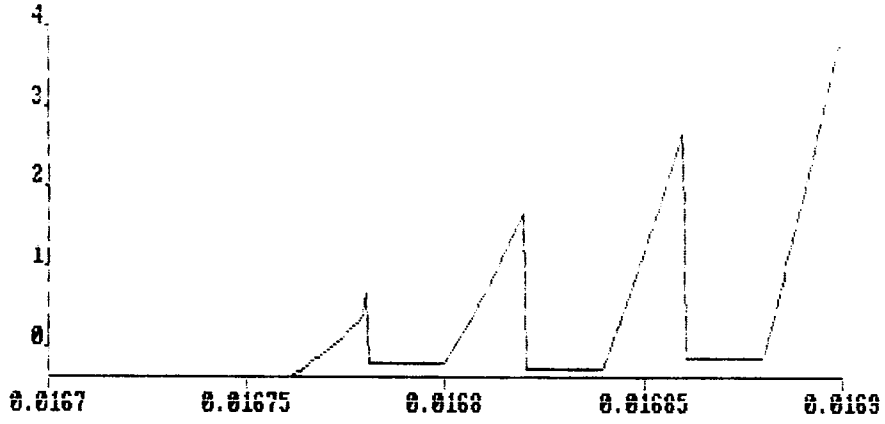
Figure 5.8

Simulation results for DC current response (a), and Simulation line current waveforms for Ld=5 μH (b, c and d)



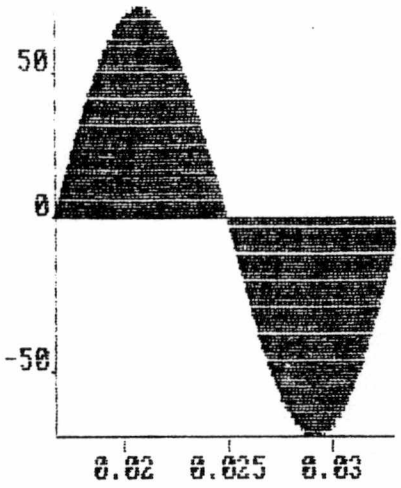
DC Link Current (a Fraction of a Cycle)

Figure 5.9



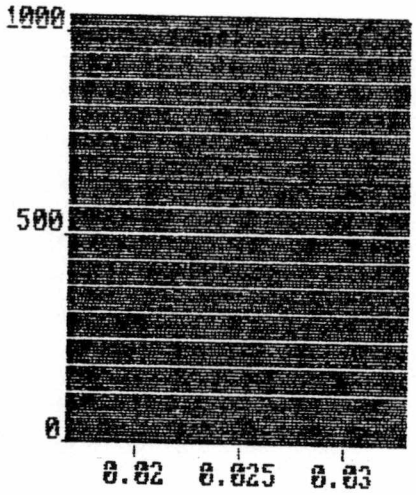
Phase A Current for a Fraction of a Cycle.

Figure 5.10



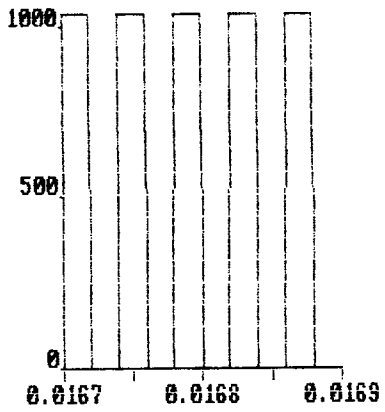
Phase A Current for Ld = 0 μH (a Cycle).

Figure 5.11



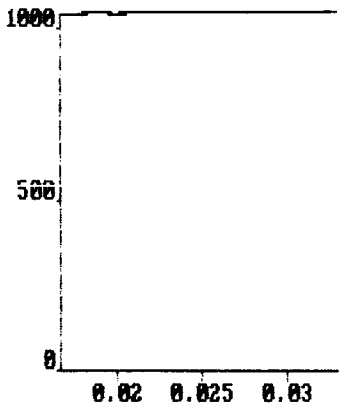
Vds (called Vrl in the Simulation)

Figure 5.12



Vds (called Vrl in the Simulation Expanded)

Figure 5.13



Vload (called Vd in the Simulation)

Figure 5.14

Chapter 6

Design and Experimentation

6.1 Design Example

6.1.1 Component Selection (Design Example)

Device selection for this scheme was based generally on projected output power and power handling specifications of devices to be utilized. The following is a review of component selection done for this scheme. This does not necessarily tell the exact type and value of components used in the implementation since that has an added consideration of component availability. However,the selection procedure carried out below forms the foundation of component choices made for the implementation.

Circuit Analysis Operating Conditions

$V_{ll} = 245V$

$P_{in} = 21.41KW$ (3Ø) RMS

Peak $I_l = 73.79$ A

Consistent with previous analysis we choose

$L_s = 50\ \mu H$

$L_d = 5\ \mu H$

$P_{out} = 21.23$ KW

An examination of the criteria governing component selection follows.

Inductors: Ls & Ld are chosen on the basis of peak voltage and current considerations.

Ls

Peak voltage (AC) predicted = $Ls \frac{di_1}{dt}$ = 93.8V (rms)

Peak current predicted = 73.79A

Since it is AC side inductor, ferrite or iron core is appropriate.
Conclusion: Required for Ls is a 100V 75A ferrite core inductor .

Ld

Projected Peak voltage = $Ld \frac{di_2}{dt} = 5 * 10^{-6} * 3.75 * 10^6$ = 18.75V

Predicted peak current = 75A

Since such high current is expected at the design operating condition a large gauge wire is applicable to reduce heating loss. A good gauge is AWG 10. As in Ls the Ld value is selected low, thus a ferrite or iron core inductor is also appropriate.

Conclusion : Required for Ld is a 50V, 75A ferrite core inductor.

Bridge Module

Calculated

Iin = 71.36A (peak)	Iout = 75A (peak) DC
Vin = 245V(rms) line	Vout = 424.4V (DC)

As bridge modules are rated by their output power handling capabilities and since the only other requirement for this module is for it to withstand the capacitor voltage in event of a fault, the bridge to use must be a 700V, 80A bridge module.

Db

Peak current through diode Db = 75A. The diode is required to have the ability to block capacitor voltage Vcp, which is 600V.

Conclusion : Required for Db is the following:

Reverse Blocking voltage = 700V
Peak 'on state' current = 80A

Cd

Desiring to have less than 0.01 percent of DC link harmonics passed on to the load, this percentage ripple can be expressed as

$$R_{\%} = 100 \frac{Vds}{Vload}$$

Where Vds = average switch voltage before capacitor.
Vload = load DC voltage.

From literature [4] the capacitor value is obtained from the expression

$$Cd = (I_d(peak) * 100 * 0.5)/(2\sqrt{3} * R_{\%} * f_s * w * Vb(peak) * 3\sqrt{3}$$

Subtituting values

$$Cd = 812.2\ \mu F$$

Since it is a DC side capacitance, an electrolytic is appropriate. The desired capacitor voltage is 600V. Capacitor rating must therefore be larger than this. 700V is

chosen. Also a consideration for Cd is the DC current rating. It is necessary that the capacitor be able to withstand I_d current pulse on no-load condition.

Conclusion : Required for the capacitor Cd is 700V, 80A electrolytic capacitor.It is also imperative that the capacitor self resonanting frequency be far from switching frequency.

Mosfet Qb

Mosfets are rated by their drain current and drain to source voltage. From the analysis the Id average is 38.34A. Repetitive pulsed drain current = 75A

Drain to source voltage = Vcp = 600V

What is required for the mosfet will therefore be a 80A, 900V rating. A mosfet has been chosen for this component selection. However, other power electronic devices provide better power handling capability. These include insulated gate bipolar transistors IGBT.

Selected heat sinking must have the capacity to dissipate I_d^2 Rds power loss. For this on going component selection, supposing Rds = 0.2ohms, this would be 0.3 KW.

It can be observed from this section's component selection and previous section's analysis that this design example is in the high-power category. The following section discusses the actual experimentation, which has much lower power specifications.

6.2 Experimentation

To confirm analysis predictions, the enhanced topology (Figure 3.1) was implemented with the following components and operating conditionsL:

Device	Rating and Type
Ls	33μH Ferrite core 14 gauge
Ld	(1,5,11,50)μH (a variety of types)
Diode module	Vout = 800V Iout = 60A

	ME500806
Mosfet	Vds = 500V I_d = 50A Rds = 0.12 ohms JD225005
Heat sink dissipation	At least 50W
Diode (Db)	Ionstate = 100A Voltage = 1200V CS241210
Capacitor (Cd)	Value = 540μF Voltage = 500V Phillips Electrolytic

Operating Conditions

Va = 18V

Input line current rms = 6A(approximate)

Switching frequency = 25kHz

Mosfet duty cycle ratio = 0.5

DC bus voltage = 150V

Output power = about 132W

6.2.2 Circuit Responses.

Discussions about circuit responses will be divided into two parts. The first will discuss the laboratory circuit performance and the second will discuss general circuit performance.

Figures presented in this section show results obtained from experimentation. The Vgs, Vds, Ia, Vload, Va, are shown here for Ld = 5 μH and 0 μH. General circuit performance includes the circuit's expected response to variations in the following parameters: fs (switching frequency), DC link inductance Ld, Ls (AC side boost inductor) and Vd (DC output voltage).

Laboratory Performance Report

Table 4 contains the rms input currents, the input power, power factor and the average DC link current I_d ave. for five values of Ld. These are Ld = 0, 1, 5, 11 and 50 μH. All data for this experimentation was taken under the same condition of constant output power. Figure 6.1 shows a plot of the relationship of efficiency with Ld value.

It can be observed from the above data that the phase angle sensitivity to Ld within the range specified is small and improves with increase in Ld.

Laboratory Results: In this section raw waveforms of circuit response will be discussed. Explanations will be offered as adequately as possible for all observable characteristics of laboratory waveforms. It is most appropriate to start from AC voltage (Va) and current (Ia) waveforms. This is shown in Figure 6.2. From this Figure (shown for Ld = 0 μH) the following information can be obtained:

(1) The power factor is 0.983.

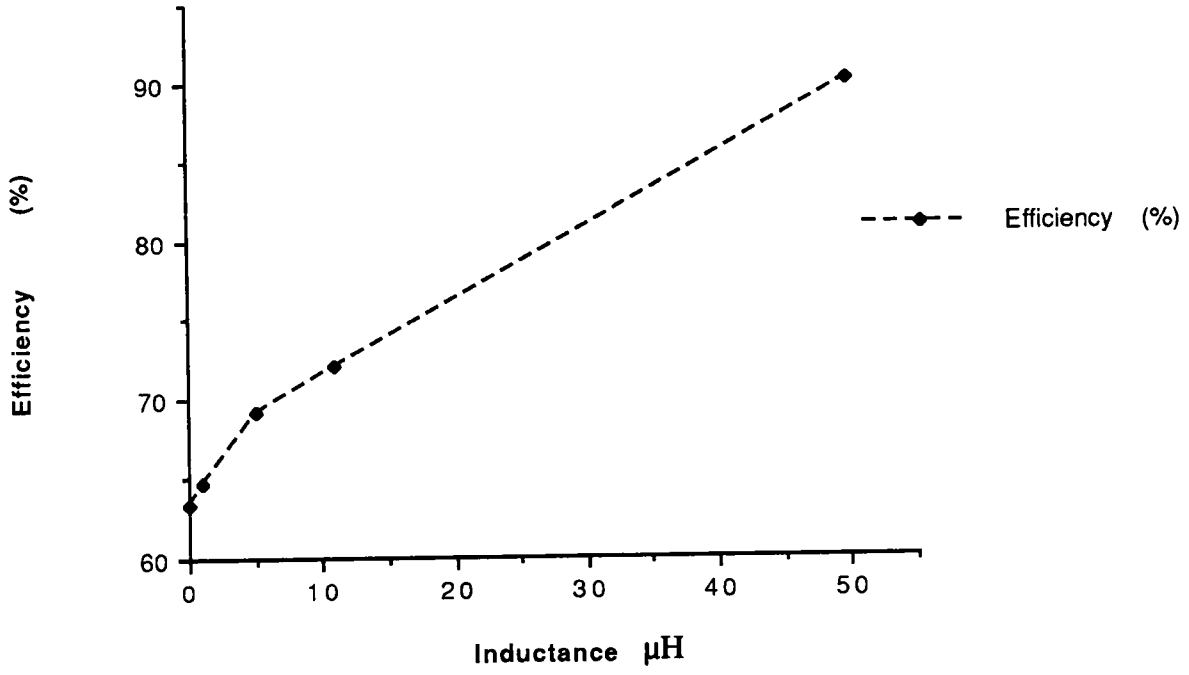
(2) The current is essentially sinusoidally shaped.

For the raw snapshot of voltage and current waveform shown in Figure 6.3, the DC link inductance is 5 μH; the second observation holds and the power factor is unity. Figure 6.4 shows line current Ia before the EMI filter. The following non-ideal features can be noticed: regions of Ia continuous conduction (two regions per half cycle to be exact), dead banding and flat topping. It is observed that the flat topping becomes more pronounced with the incorporation of Ld and with Ld increase. The dead banding also does the same. Figure 6.5 shows the Ia waveform before the EMI for Ld = 1 μH

Table 4

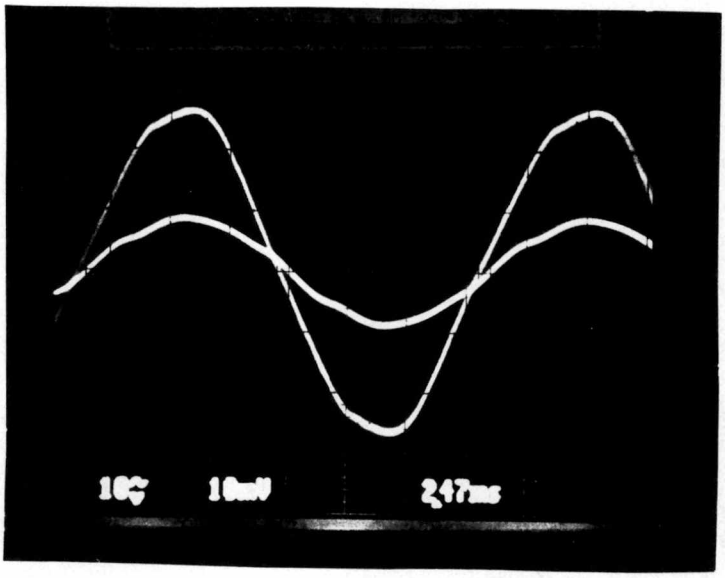
Table of Data Taken from Experimentation

INDUCTANCE	0μH	1μH	5μH	11μH	50μH
INPUT POWER	205.2W	204.5W	192.5W	183.8W	147.1W
EFFICIENCY	63.4%	64.7%	69.2%	72.02%	90%
POWER FACTOR	.983pf	.985pf	1pf	1pf	1.002pf
Ia (rms)	6.50A	6.50A	5.96A	5.75A	4.42A
Ib (rms)	6.51A	6.48A	5.92A	5.78A	4.42A
Ic (rms)	6.43A	6.39A	5.79A	5.77A	4.40A
Id (ave.)	8.06A	8.04A	7.14A	7.00A	4.94A
OUTPUT POWER	132.4W	132.4W	132.4W	132.4W	132.4W



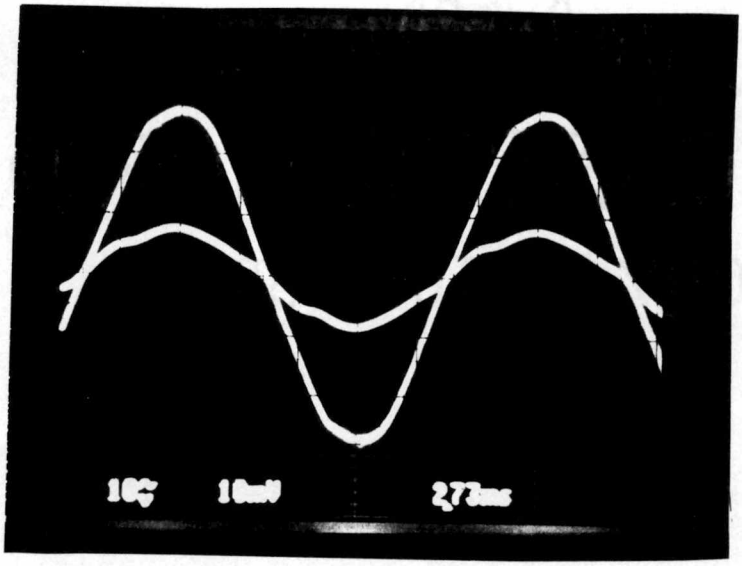
Plot of Efficiency Versus Ld

Figure 6.1



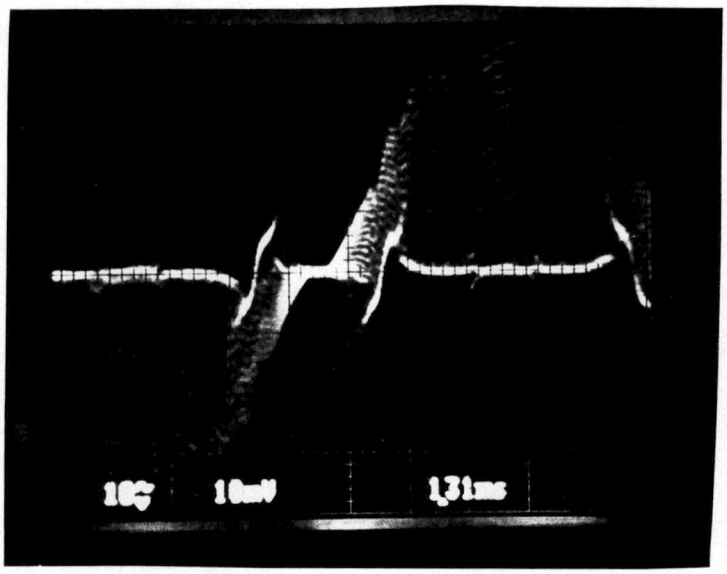
Voltage and Current Photo after the EMI Filter Ld = 0 μH

Figure 6.2



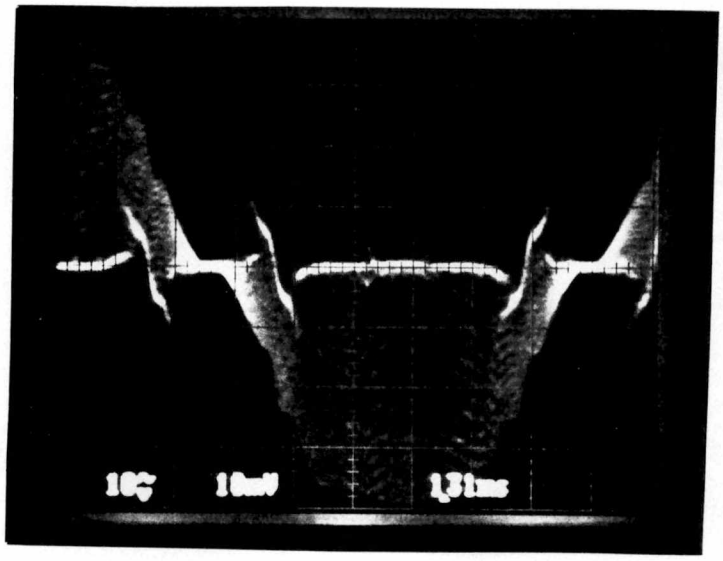
Voltage and Current Photo after the EMI Filter Ld = 5 μH

Figure 6.3



Raw Photo of Phase A Current before the EMI Ld =0 μH

Figure 6.4



Phase A Current before the EMI Filter for Ld = 1 μH

Figure 6.5

Flat Topping: The most logical explanation for the observed flat topping is the DC capacitor charging effect superimposed on the sinusoidal wave shape generated by the power line conditioner. In the conventional diode bridge rectifier, the capacitor charging effect is very pronounced and is seen as two pulses per half cycle, leading to extremely high current distortion. In this currently discussed waveform, the capacitor charging effect can be seen as overly high peak instantaneous currents around regions of conventional current pulses. In this regions of exaggerated current peaks, the peak current values are comparable to the peak current value established at the peak of the phase voltage, hence, the flat topping effect.

Regions of Continuous Conduction: Close examination of the line current waveform shows that this region coincides with around 40° of current waveform cross-over. It can be

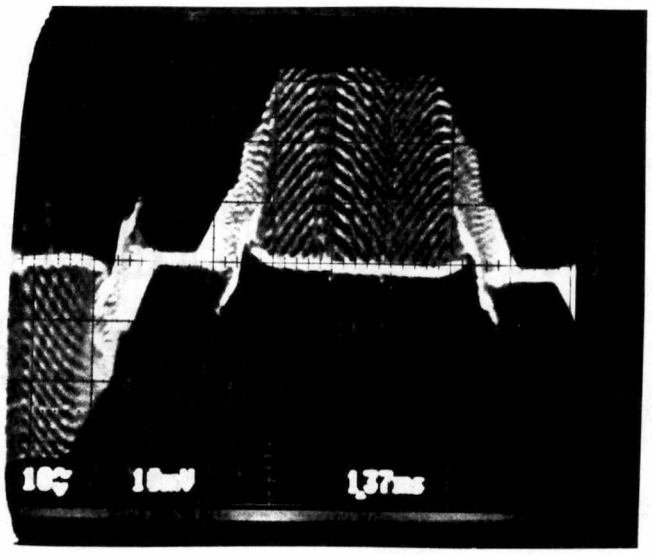
seen that an oscillation occurs for a total of 40° during which time the phase A upper diode supplies the current in the negative oscillation swing from the reverse recovery current and conducts positive line current (irrespective of turn-on or turn-off), in its positive swing. The source of this oscillation can be traced to the AC side boost inductor's interaction with stray capacitance during the process of current reversal. Since AC side inductance is kept constant for various values of Ld and this oscillation is only maginally related to Ia, the magnitude of this oscillation is expected to remain constant with Ld change. This appears to be the case as seen in Ia waveform shown for Ld = 5 μH in Figure 6.6.

Dead Banding: Due to stray inductances in the DC link in the case of Ld = 0 μH and deliberate incorporation of a DC link inductance in the case of Ld = 5 μH, a small finite threshold voltage is introduced into the circuit response which affects the phase conduction at very small voltage levels. This threshold voltage is introduced by the potential drop across the DC link inductance and the diode forward drops. At small phase voltages, for example, in the positive Va cycle (though the Va is positive) the upper diode D1 remains turned off because the potential at its cathode is more positive than at its anode and so it remains turned off until this threshold is exceeded. This dead banding is obliterated by the EMI in both the case of the no Ld and finite Ld. Dead banding occurs for less than 10° per half cycle in the Figure 6.4. The waveform for Ld = 5 μH, however, shows slightly more dead banding.

I_d current waveforms are as expected from the simulation results, with no apparent show of undesirable features. I_d current can be seen with the phase voltage waveform in Figure 6.7. The expanded waveform can be seen in Figure 6.8. The only remark to make is that the oscilloscope shows a trace overlap problem in Ld = 0 μH expanded waveform. This is as a result of trigger problem. This was corrected for Ld = 5 μH. The I_d wave with phase voltage and the I_d expanded for Ld = 5 μH are given in Figures 6.9 and 6.10.

The Vgs waveform for Ld =0 μH and 5 μH can be seen in Figures 6.11 and 6.12 and it was as expected.

The Vload waveforms for Ld = 0 μH and 5 μH are identical, as expected. The load resistance was 170 ohms in both cases making power output to be 132W. The Vload waveforms can be seen in Figures 6.13 and 6.14.



Phase A Current before the EMI Filter for Ld = 5 μH

Figure 6.6

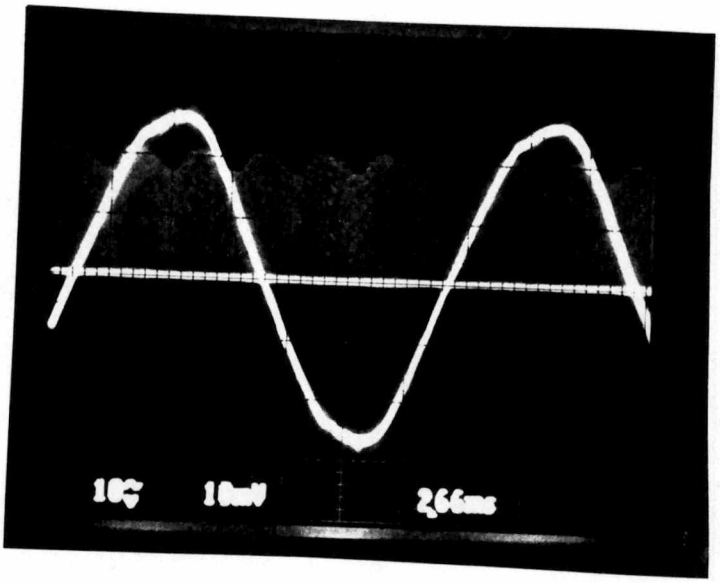
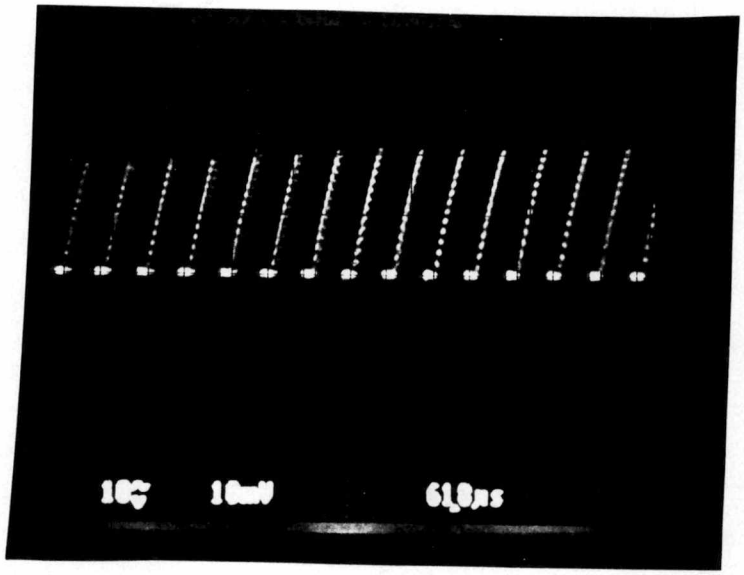


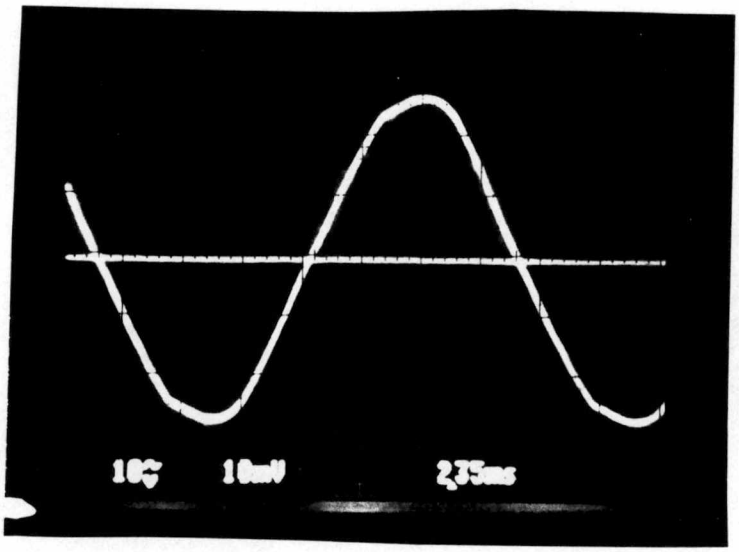
Photo of Ia Current and Phase A Voltage for Ld = 0 μH

Figure 6.7



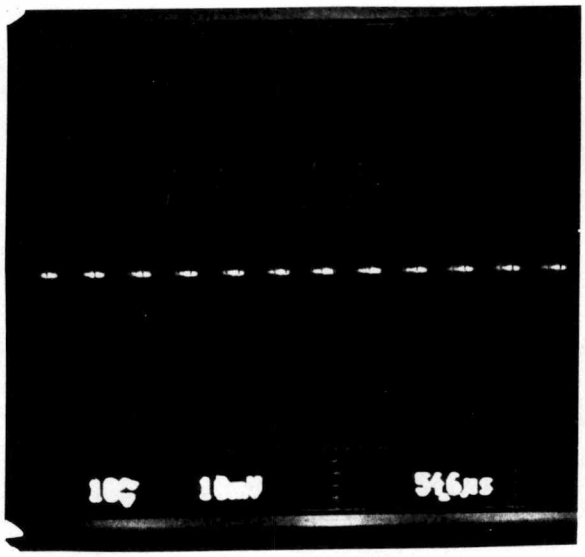
Ia Current Waveform Expanded for Ld = 0 μH

Figure 6.8



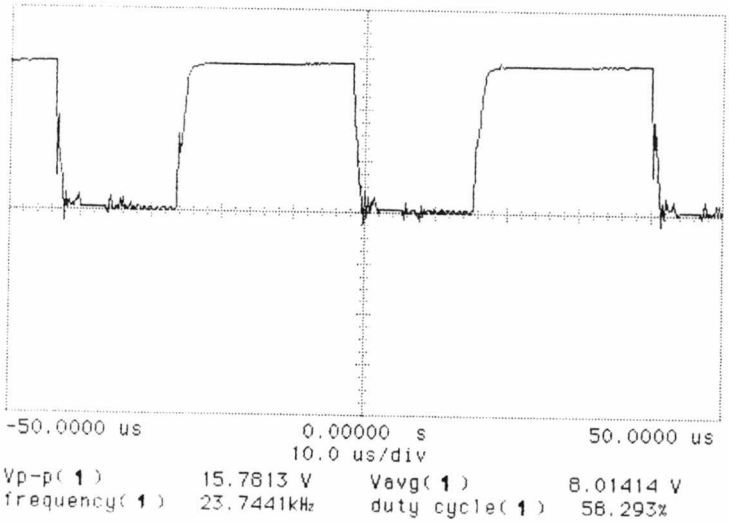
Ia Current and Phase Voltage at Ld = 5 μH

Figure 6.9



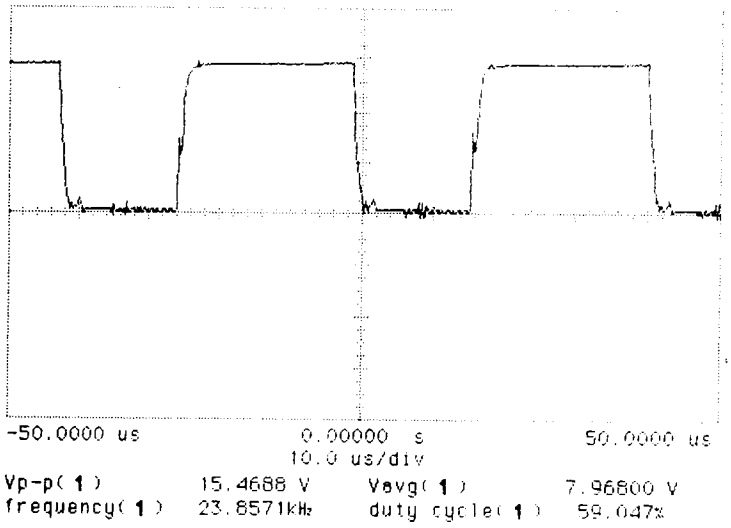
Ia Current Waveform (Expanded) for Ld = 5 μH

Figure 6.10



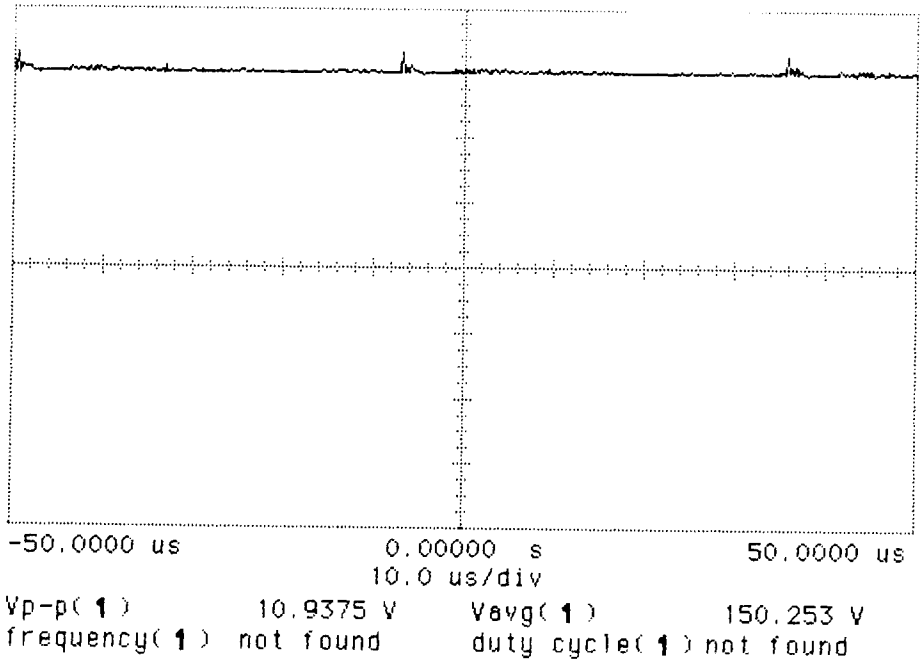
Vgs Waveform for Ld = 0 μH

Figure 6.11



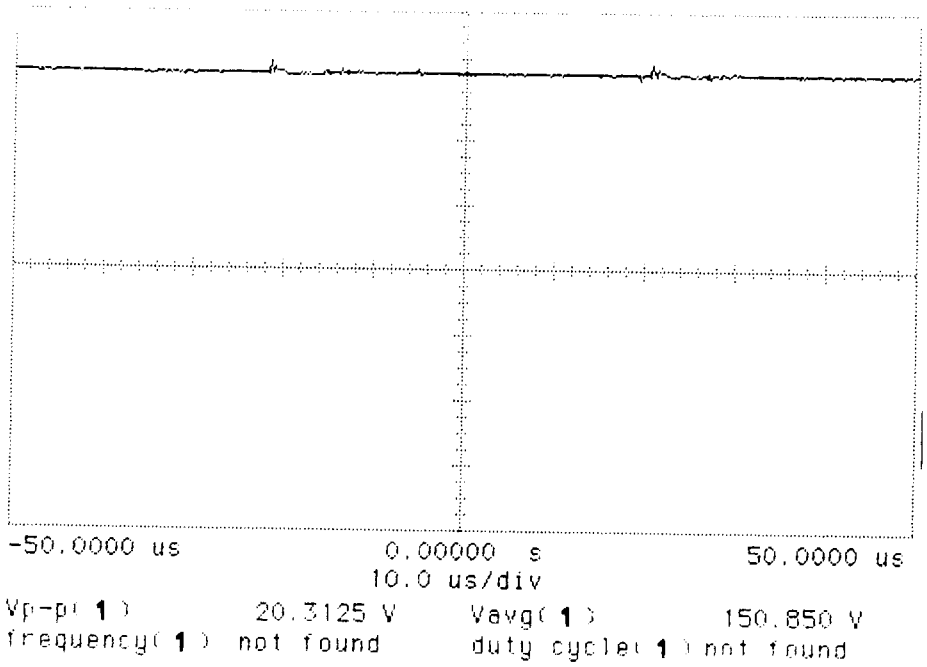
Vgs Waveform for Ld = 5 μH

Figure 6.12



Vload Waveform for Ld = 0 μH

Figure 6.13



Vload Waveform for Ld = 5 μH

Figure 6.14

partly to snubber operation and partly to DC link diode forward voltage drop. To further explain this phenomenon, the snubber operation will be looked into.

Snubber Operation: The kinds of snubbers used for the mosfet in this application were the turn-on and turn-off snubbers.

Turn-off Snubber: To avoid voltage stress at turn-off, a turn-off snubber should provide a zero voltage across the switch while the current turns off. This is achieved by connecting an R-C-D network across the switch. Prior to turn-off, the mosfet current is some value-I_d and its voltage is essentially zero. At turn-off in the presence of this snubber, the switch current decreases with a constant di/dt while the switch and the capacitor share the main current. The capacitor voltage, which is the same as the voltage across the switch, can be expressed as

$$Vcs = Vds = \frac{1}{C}\int_0^t i_c\, dt = \frac{Idt^2}{2Cs*tfi}$$

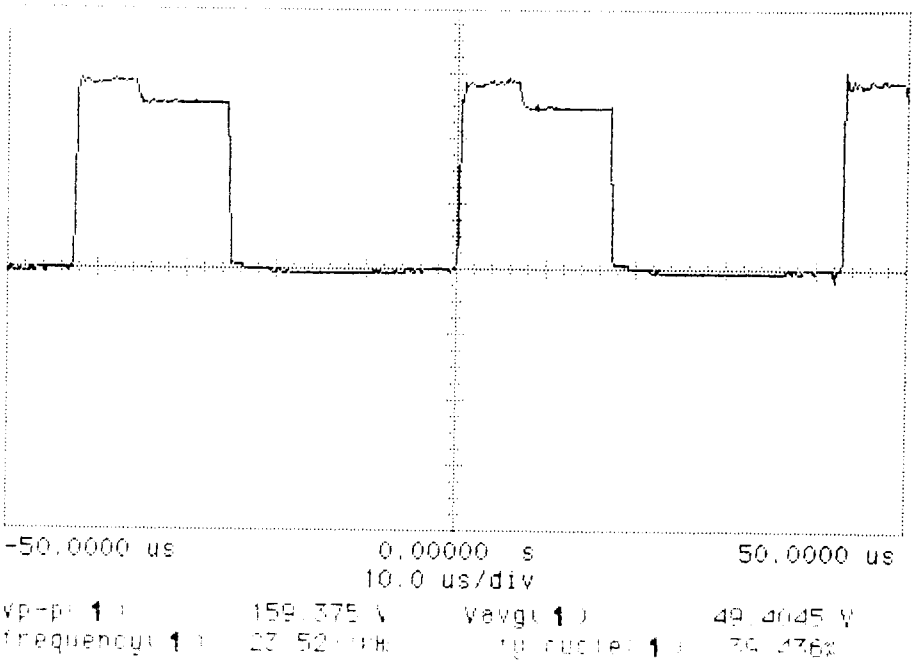
The voltage charging predictions shown in Figure 6.17 are for three values of snubber capacitance. These three capacitor values contain the following three characteristics.

(1) For a small value of Cs, the capacitor voltage reaches Vd before current fall time is over, causing the snubber capacitor to overcharge in the absence of any voltage clamp in the circuit. (This is case at hand.)

(2) If the value of the capacitor were Cs1 from equation 6.1, then the capacitor voltage would reach Vd just as current fall time expires.

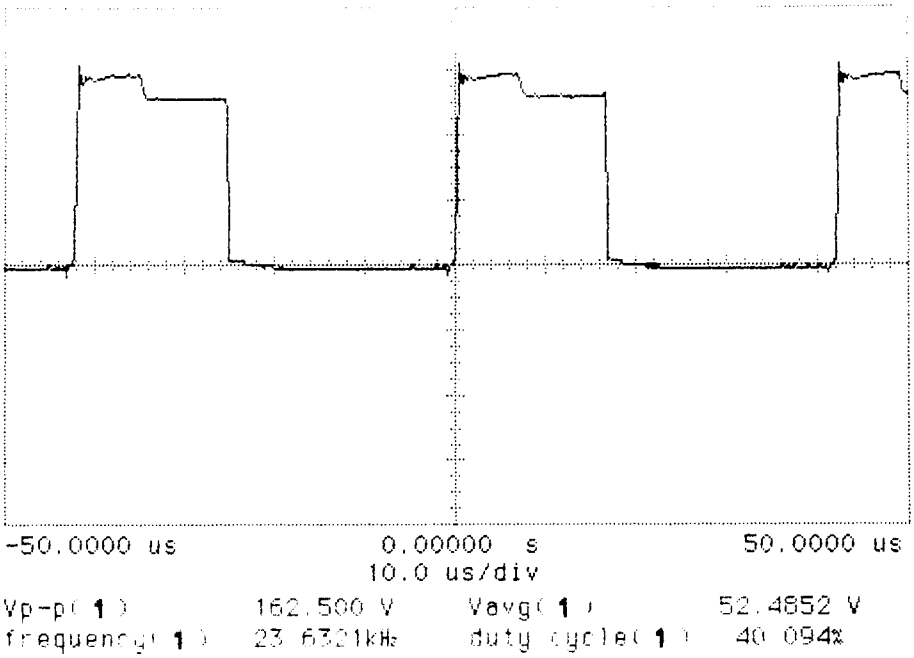
$$Cs_1 = \frac{I_d * tfi}{2Vd} \qquad (6.1)$$

(3) For a large capacitance value, the switch voltage rises slowly and takes longer than tfi to reach Vd and would not reach Vd if the main line current were switched to load by some other means. During the on state of the transistor, the capacitor discharges with a time constant tc=RC and $Vcs = Vd\, e^{t/tc}$



Vds Waveform for Ld = 0 μH

Figure 6.15



Vds Waveform for Ld = 5 μH

Figure 6.16

Discharging Vcs to 0.1Vd requires a time interval of 2.3 tc and so

$$Ton>2.3RsCs$$

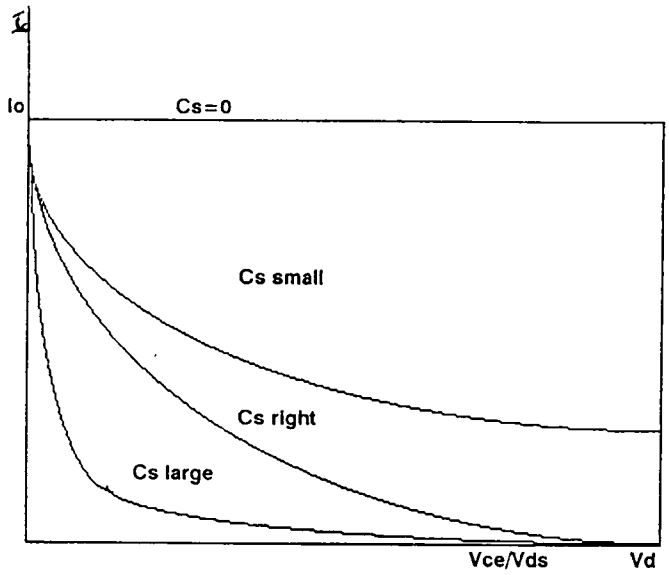
Turn-on Snubber: Turn-on snubbers work by reducing the voltage across the switch as the current builds up. A turn-on snubber is typically put in series with the switch. An example of a turn-on snubber is the inductor connected in series with the switch in the circuit of Figure 3.1. The reduction in voltage in the switch during turn-on is a result of the voltage drop across Ld. This reduction is given by

$$D*Vds = \frac{Ld*I_d}{tri}$$

where tri is the current rise time. With a large value of series inductance the di/dt of the main switch is considerably reduced. A large value of inductance will result in lower turn-on voltages and lower the turn-on losses, but it may result in overvoltages during turn-off, lengthen the minimum required off interval and possibly cause turn-off failure.
In the currently discussed topology, the turn-off snubber capacitor was calculated to be

$$Cs_1 = \frac{I_d*tfi}{2Vd} = \frac{8.06*1300*10\text{-}9}{2*150}$$
$$=34.93nF$$

Due to availability, a 10nF capacitor was used instead. The snubber capacitor charges to Vd before I_d current has fallen to zero, overcharges, then bleeds off the overcharge to the load through the snubber resistor Rs and DC link diode Db, after turn-off has been completed. The higher peak Vds portion corresponds to the overcharge and subsequent bleeding off. The phenomenon is the same for both no Ld and finite Ld.



Snubber Capacitor Voltage Charging Predictions

Figure 6.17

General Circuit Performance

This circuit is expected to respond to the following parameter variations in the following way. This predictions has been gathered from normal electrical system principles and experience in experimentation.

Ld Variation: Displacement factor improves from lagging to unity to leading and the distortion factor slowly deteriorates for increase in Ld. Displacement factor improves due to a reduction in line current magnitude. Since the application is a high frequency operation, only the impedance nature of the boost inductors is utilized. This, however, is only accurate for low current values. As current increases, the inductive nature of the boost inductors tends to cause the response to deviate from unity displacement factor operation. If Ld is increased to a high value, the switching of the mosfet is affected. If Ld is large enough to cause continuous conduction of I_d current the sinusoidal waveshape of the line current is destroyed. Without Ld, however, the topology reverts to the former scheme with its problems of current stress.

Fs Variation: With switching frequency increase, the discontinuous conduction degrades, the switching of the power switch deteriorates, switching losses increase, but the EMI filter size reduces. There is also a reduction in the size of the DC link capacitor.

Ls Variation: From experimentation it was noted that for Ls increase, a corresponding increase would occur in the crossover oscillations of the type discussed in the laboratory performance report. Reduction in Ls, however, would result in an increase in current stress on the diode bridge.

Vd Variation: The load voltage is to be kept sufficiently higher than peak phase voltage. The load voltage should be at least 4 p.u. of peak phase voltage. The reason for this can be seen from previous sections on analysis. To reduce Vd beyond this would be to lose discontinuous conduction and consequently sinusoidal waveshape of the input line currents. To increase Vd higher has no apparent problems as long as this is compatible with the DC power application.

6.3 Circuit Comparison

From the data shown in Table 4 it is clear that the rms current decreases with Ld. Therefore peak current and input power also decrease with Ld. This causes the efficiency to increase with Ld. It must be stated that the boost switch duty cycle ratio was constrained to be constant and nearly equal to 0.5 for all values of Ld. Even though not exactly 0.5, Ld was constrained to retain no net energy by ensuring discontinuous conduction of I_d, so that the exact predictions of the analysis would be justified.

Observation shows that the total harmonic distortion deteriorates with Ld value increase. This is a limitation of this enhanced scheme. Other factors mitigating against further increase of the Ld inductance value is discussed in the concluding chapter of this thesis. For now it suffices to say that a balance can be struck between a total harmonics distortion factor within required limits and circuit efficiency performance to give optimum circuit operation.

6.3.1 Harmonics Comparison

Since the circuit is constrained to operate under I_d discontinuous operation--just like the Ziogas scheme--it yields a similar ripple pattern and same percentage ripple. This constraint was necessary for the generation of sinusoidal line current.

Chapter 7

Discussions and Conclusion

7.1 Achievements

Efficiency improvement was achieved with the the topology modifications. An evaluation of the current PLC topologies has been made. Since peak AC line currents and peak DC link currents were reduced with the incorporation of the DC link inductor, it has been shown that stress on main circuit devices has been lessened. This reduction in peak current values has a twofold effect. First, the mean life before failure period has been improved. Second, for the same output power less AC line current is being drawn.This consequently reduces the loading on the utilities. Since power consumption per hour is economically critical to any topology use, this modified topology would be preferred over its predecessor.

7.2 Closing Remarks

As previously touched upon in the body of this report, experimentation and analysis has indicated an upper limit to the value of Ld, for which a sinusoidal line current can be maintained. Although not included in this report before now, the shape of the line current tends toward square wave as Ld tends toward infinity. Factors mitigating against an infinite increase of Ld include

(1) Simultaneous conduction of all phases which stops with an increase in Ld above that given in this report. As Ld increases, the turn-on schematic as shown in Figure 3.2 no longer holds. It changes to two conducting phases per turn-on and turn-off (instead of the three in Figure 3.2). This causes the line currents to become 30° displaced from their respective phase voltages and if Ld is large enough, to become square-shaped.

(2) As Ld tends toward infinity the I_d tends toward a constant value which renders ineffective any switching of the mosfet. Experimentation has also shown this degrades mosfet performance by greatly reducing its turn-on speed. It consequently degrades the

gate signal due to the increased charging time of the gate to drain capacitance. One would expect the efficiency of the scheme to worsen at this point.

(3) In direct relation to the point made in (2), the topology no longer operates as a power line conditioner and has none of the essential qualities of the PLC (for example unity power factor operation and sinusoidal line currents).

(4) The efficiency recorded in the experimentation was low, a fact solely due to the low power in which the circuit was operating at the time the data was taken. As relative improvement of efficiency is the main justification for the new topology, this does not pose a problem.

7.3 Conclusion

This report has sought to bring into focus work up to date in power line conditioning Conducting this recent study, it has introduced an enhanced topology of a three-phase diode bridge rectifier with boost converter for active filtering, which it has shown to improve efficiency performance and durability of a current topology.

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Appendix

This appendix contains the following:

(1) Computational examples for I_d peak

(2) Simnon program for the computer analysis

(1) At $t = 0$

$Va = 0$ $Ls = 50\mu H$

$Vb = 193.2V$ (note polarity indicated in position 1 turn-on schematic)

$Vc = 173.2V$ $Ld = 5\mu H$

$$2Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = Va - Vc$$

Substituting values

$$2 * 50 * 10^{-6}\frac{di_1}{dt} - 50 * 10^{-6}\frac{di_2}{dt} = -173.2$$

$$100 * 10^{-6}\frac{di_1}{dt} - 50 * 10^{-6}\frac{di_2}{dt} = -173.2 \quad \ldots\ldots\ldots\ldots\ldots (1)$$

$$(2Ls + Ld)\frac{di_2}{dt} - Ls\frac{di_1}{dt} = Vc + Vb$$

Substituting values

$$105 * 10^{-6}\frac{di_2}{dt} - 50 * 10^{-6}\frac{di_1}{dt} = 173.2 + 173.2 \quad \ldots (2)$$

Representing di_1/dt as x and di_2/dt as y

$$100x - 50y = -173.2 * 10^6$$

$$105y - 50x = 346.4 * 10^6$$

Simultaneous solution yields

$$y = 3.25 * 10^6 \text{ A/s}$$

Since y = rate of change of DC link current with time, in the time of the switching period, I_d = 65A

At t= pi/12

Va = 51.8V

Vb = 193.2V

Vc = 141.4V (as usual, all polarity has been taken care of)

$$2\,Ls\frac{di_1}{dt} - Ls\frac{di_2}{dt} = 51.8 - 141.4$$

$$(2\,Ls + Ld)\frac{di_2}{dt} - Ls\frac{di_1}{dt} = 141.4 + 193.2$$

$$100x - 50y = -89.6 * 10^6$$

$$105y - 50x = 334.6 * 10^6$$

$$y = 3.623 * 10^6 \text{ A/s}$$

$$I_d(wt) = 72.5A$$

At wt = pi/6

$$100x - 50y = 0$$

$$105y - 50x = 300 * 10^6$$

$$y = 3.75 * 10^6 \text{ A/s}$$

$I_d = 75A$

These values of I_d repeat themselves as can be seen in the figure of the plot of I_d.

SIMNON PROGRAM

```
CONTINUOUS SYSTEM DRFPR
" IDEAL DIODE IS ASSUMED
" SET UP THE MODEL'S STATE VARAIBLES AS FOLLOWS:
STATE  id1 VDL IA IB IC
DER  did1 DVDL DIA DIB DIC
TIME T
" USING THE CIRCUIT MODEL AND SUPERPOSITION PRINCIPLE
" THE RATE OF CHANGE OF LINE CURRENTS CAN BE FABRICATED AS FOLLOWS:
"
A1 = (VA/X)-(0.524*(VC/X))-(0.5*((VRL/Y)+(VB/Y)))
B1 = (VA/Y)-(VRL/Y)-(0.48*(VC+VB)/X)
C1 = (VA/X)-(0.524*(VB/X))-(0.5*((VRL+VC)/Y))
D1 = (VA/X)-(0.524*(VC/X))-(0.5*(VB/Y))+(0.5*(VRL/Y))
E1 = (VA/Y)-(0.48*((VC+VB)/X))+(VRL/Y)
F1 = (VA/X)-(0.524*(VB/X))-(0.5*(VC/Y))+(0.5*(VRL/Y))
"
"
DIA = IF WT>0 AND WT<PIB3 THEN SEE1 ELSE SEE2                    "
SEE1 = IF A1<0 AND IA<0 THEN 0 ELSE A1
SEE2 = IF WT>PIB3 AND WT<PIT2B3 THEN SEE3 ELSE SEE4              "
SEE3 = IF B1<0 AND IA<0 THEN 0 ELSE B1
SEE4 = IF WT>PIT2B3 AND WT<PI THEN SEE5 ELSE SEE6                "
SEE5 = IF C1<0 AND IA<0 THEN 0 ELSE C1
SEE6 = IF WT>PI AND WT<PIT4B3 THEN SEE7 ELSE SEE8                "
SEE7 = IF D1>0 AND IA>0 THEN 0 ELSE D1                           "
SEE8 = IF WT>PIT4B3 AND WT<PIT5B3 THEN SEE9 ELSE SEE10           "
SEE9 = IF E1>0 AND IA>0 THEN 0 ELSE E1                           "
SEE10 = IF WT>PIT5B3 AND WT<PIT2 THEN SEE11 ELSE 0               "
SEE11 = IF F1>0 AND IA>0 THEN 0 ELSE F1
"
A2 = (VB/Y)+(VRL/Y)-(0.48*((VA+VC)/X))
B2 = (VB/X)-(0.524*(VC/X))-(0.5*(VA/Y))+(0.5*(VRL/Y))
C2 = (VB/X)-(0.524*(VA/X))-(0.5*((VC+VRL)/Y))
D2 = (VB/Y)-(0.48*((VA+VC)/X))-(VRL/Y)
E2 = (VB/X)-(0.524*(VC/X))-(0.5*((VA+VRL)/Y))
F2 = (VB/X)-(0.524*(VA/X))-(0.5*(VC/Y))+(0.5*(VRL/Y))
"
DIB = IF WT>0 AND WT<PIB3 THEN SEE21 ELSE SEE22
SEE21 = IF A2>0 AND IB>0 THEN 0 ELSE A2
SEE22 = IF WT>PIB3 AND WT<PIT2B3 THEN SEE23 ELSE SEE24
SEE23 = IF B2>0 AND IB>0 THEN 0 ELSE B2
SEE24 = IF WT>PIT2B3 AND WT<PI THEN SEE25 ELSE SEE26
SEE25 = IF C2<0 AND IB<0 THEN 0 ELSE C2
SEE26 = IF WT>PI AND WT<PIT4B3 THEN SEE27 ELSE SEE28
SEE27 = IF D2<0 AND IB<0 THEN 0 ELSE D2
SEE28 = IF WT>PIT4B3 AND WT<PIT5B3 THEN SEE29 ELSE SEE210
SEE29 = IF E2<0 AND IB<0 THEN 0 ELSE E2
SEE210 = IF WT>PIT5B3 AND WT<PIT2 THEN SEE211 ELSE 0
SEE211 = IF F2>0 AND IB>0 THEN 0 ELSE F2
"
A3 = (VC/X)-(0.524*(VA/X))-(0.5*(VRL/Y))-(0.5*(VB/Y))
B3 = (VC/X)-(0.524*(VB/X))-(0.5*(VA/Y))+(0.5*(VRL/Y))
C3 = (VC/Y)-(0.48*((VA+VB)/X))+(VRL/Y)
D3 = (VC/X)-(0.524*(VA/X))-(0.5*(VB/Y))+(0.5*(VRL/Y))
E3 = (VC/X)-(0.524*(VB/X))-(0.5*(VA/Y))-(0.5*(VRL/Y))
F3 = (VC/Y)-(VRL/Y)-(0.48*((VA+VB)/X))
"
DIC = IF WT>0 AND WT<PIB3 THEN SEE31 ELSE SEE32
```

```
SEE31 = IF A3<0 AND IC<0 THEN 0 ELSE A3
SEE32 = IF WT>PIB3 AND WT<PIT2B3 THEN SEE33 ELSE SEE34
SEE33 = IF B3>0 AND IC>0 THEN 0 ELSE B3
SEE34 = IF WT>PIT2B3 AND WT<PI THEN SEE35 ELSE SEE36
SEE35 = IF C3>0 AND IC>0 THEN 0 ELSE C3
SEE36 = IF WT>PI AND WT<PIT4B3 THEN SEE37 ELSE SEE38
SEE37 = IF D3>0 AND IC>0 THEN 0 ELSE D3
SEE38 = IF WT>PIT4B3 AND WT<PIT5B3 THEN SEE39 ELSE SEE310
SEE39 = IF E3<0 AND IC<0 THEN 0 ELSE E3
SEE310 = IF WT>PIT5B3 AND WT<PIT2 THEN SEE311 ELSE 0
SEE311 = IF F3<0 AND IC<0 THEN 0 ELSE F3
"
"ALSO USING THE SUPERPOSITON THEORY AND THE CIRCUIT MODEL WE CAN FABRICATE
" THE DC LINK RESPONSE AS
A = 0.48*((VA+VC)/X)-(VB/Y)-(VRL/Y)
B = (VA/Y)-(0.48*((VB+VC)/X))-(VRL/Y)
C = 0.48*((VA+VB)/X)-(VC/Y)-(VRL/Y)
D = (VB/Y)-(0.48*((VA+VC)/X))-(VRL/Y)
E = 0.48*((VB+VC)/X)-(VA/Y)-(VRL/Y)
F = (VC/Y)-(0.48*((VA+VB)/X))-(VRL/Y)
"
DID1 = IF WT>0 AND WT<PIB3 THEN DO1 ELSE DO2
DO1  = IF A<0 AND ID1<0 THEN 0 ELSE A
DO2 = IF WT>PIB3 AND WT<PIT2B3 THEN DO3 ELSE DO4
DO3 = IF B<0 AND ID1<0 THEN 0 ELSE B
DO4 = IF WT>PIT2B3 AND WT<PI THEN DO5 ELSE DO6
DO5 = IF C<0 AND ID1<0 THEN 0 ELSE C
DO6 = IF WT>PI AND WT<PIT4B3 THEN DO7 ELSE DO8
DO7 = IF D<0 AND ID1<0 THEN 0 ELSE D
DO8 = IF WT>PIT4B3 AND WT<PIT5B3 THEN DO9 ELSE DO10
DO9 = IF E<0 AND ID1<0 THEN 0 ELSE E
DO10 = IF WT>PIT5B3 AND WT<PIT2 THEN DO11 ELSE 0
DO11 = IF F<0 AND ID1<0 THEN 0 ELSE F
DVDL = (I11-I2)/CP
VD = VDL
VRL = IF S>0 THEN 0 ELSE VD
I11 = IF S<0 THEN ID1 ELSE 0                    "
"GENERATE SWITCHING COMMAND FOR SWITCH
S = IF MOD(T,PER)<PER/2 THEN 1 ELSE -1
"INPUT VOLTAGES: SINUSOIDAL
VA = AM*SIN(WTAUX)
VB = AM*SIN(WTAUX-PIT2B3)
VC = AM*SIN(WTAUX+PIT2B3)
" BASIC EXPRESSIONS USED IN THE PROGRAM.
PI = 4*ATAN(1)
PIT2 = 2*PI
PIB3 = PI/3
PIT2B3 = (2*PI)/3
PIT4B3 = (4*PI)/3
PIT5B3 = (5*PI)/3
PIB6 = PI/6
PIB2 = PI/2
PIT5B6 = (5*PI)/6
PIT7B6 = (7*PI)/6
PIT3B2 = (3*PI)/2
PIT11B6 = (11*PI)/6
WTAUX = 2*PI*60*T
WT = MOD(WTAUX,PIT2)
" PARAMETERS
X:76.19E-6
Y:80E-6
CP:540E-6
LD:5E-6
LS:50E-6
VDL:300    "INITIALIZE CAPACITOR VOLTAGE
I2:5     "LOAD PARAMETER
AM:180
PER:0.00004
END
```

Vita

Adeoti Taiwo Adediran was born in Ibadan, Nigeria. She received a bachelor of science degree in Electrical Engineering at the University of Ibadan, Nigeria, in July 1987. She enrolled in the University of Tennessee, Knoxville to continue her study in Electrical Engineering with a specialty in Power Electronics. Her career goal is to be involved in research and development in the area of Power Optimization and Control.

She is a member of the Nigerian Association of Professional Women Engineers, a subsidiary of the International Association of Professional Women Engineers, the IEEE and the International Association of University Women.