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A WIDE-RANGE LOGARITHMIC ELECTROMETER WITH IMPROVED ACCURACY AND TEMPERATURE STABILITY

A Thesis
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Degree
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Milton Nance Ericson
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ABSTRACT

A seven-decade temperature-compensated logarithmic electrometer is presented. The amplifier is designed for a dynamic range of 1 pA to 10 μA. Temperature compensation is accurately achieved by using an array of four matched monolithic bipolar transistors and straightforward postprocessing techniques. Use of this method results in <1% error over the temperature range of −18 to 71°C for the upper five decades of input current. In addition, errors resulting from variable emission coefficients of the logarithmic elements are eliminated. Problems associated with the temperature compensation of logarithmic amplifiers are identified and discussed. Implementation of the new temperature-compensation technique is fully described and compared with conventional methods. Selection of devices and associated temperature characterization are presented. A complete stability analysis of the amplifier is performed and verified with circuit simulations and laboratory testing. Experimental results and data analysis illustrating the performance of the design over temperature are presented.

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Chapter 1

INTRODUCTION

Atmospheric Radiation Measurement Program

Background

The work described in this thesis was performed as part of the Atmospheric Radiation Measurement (ARM) program. This program is funded by the U. S. Department of Energy (DOE) and is directed toward the development of climate models for radiative energy transport and for cloud formation, maintenance, and dissipation (DOE 1990). Under this initiative, new atmospheric measurement techniques, instrumentation, and data interpretation methods are under development to aid in the generation and testing of these new models. The ARM program will use a set of facilities called the Cloud and Radiation Testbed (CART), located at various sites around the world, to acquire atmospheric data and subsequently generate and test climate models. Each CART site will be equipped with a variety of instrumentation for measuring certain atmospheric parameters. A design team at Oak Ridge National Laboratory was funded to develop a shortwave solar radiometer for use at the CART sites. Information from this type of instrument is necessary for the characterization of atmospheric aerosols, trace gases, and cloud radiative phenomena (DOE 1990).

The proposed radiometer design uses a technique called information-based sparse sampling. The solar spectrum of interest (0.3 to 1.1μm) is divided into 38 separate bands by optical means, and the energy in each of the bands is measured by a silicon photodiode (see Figure 1.1). From these sampled energy bands, a complete solar spectrum can be reconstructed by using newly developed spectral models (Simpson et al. 1991).

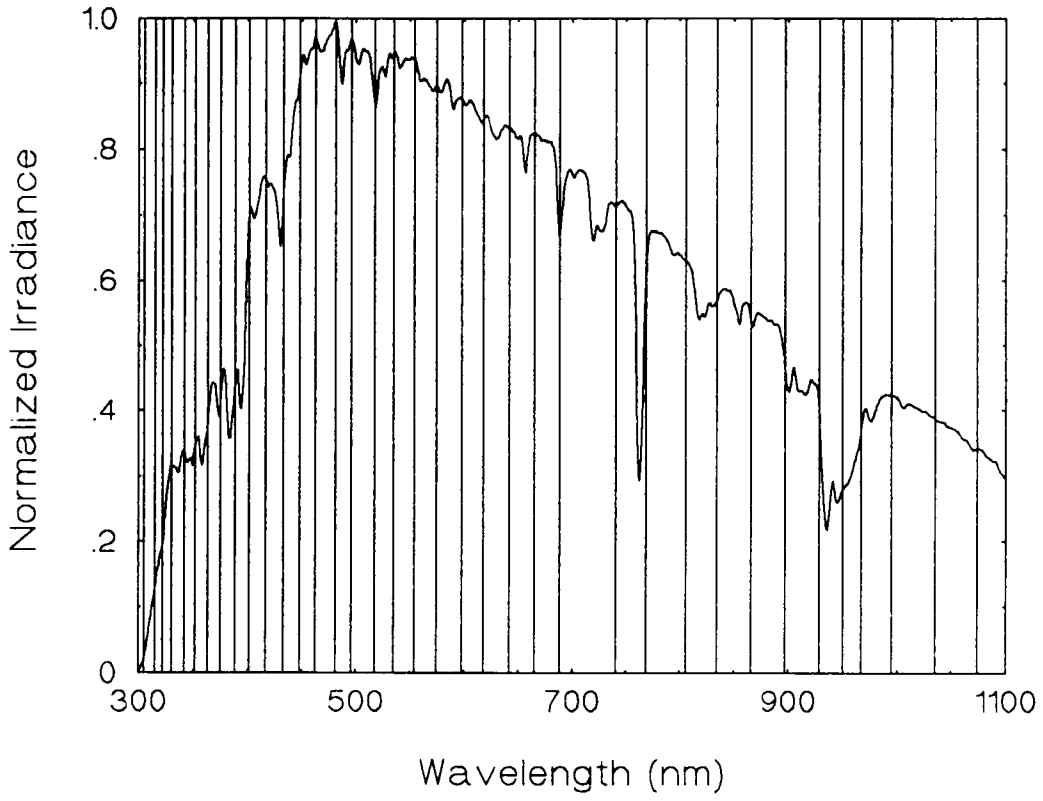


Figure 1.1. A 38-channel sampling of the solar spectrum.

Radiometer Overview

A simplified electronics systems block diagram for the ARM radiometer is shown in Figure 1.2. Signals from each of the 38 silicon photodiodes are amplified and multiplexed into an analog-to-digital converter (ADC) to digitize the individual spectral band energies. A microcontroller module consisting of a microprocessor, static random access memory (SRAM), and a communications interface is used to control data acquisition, manipulate measured data, and communicate with the CART site instrument network.

Specifications for the front-end detector amplifiers were determined by characterizing the nature of atmospheric and solar phenomena, the photodiode detectors, and the general measurement requirements of the instrument. LOWTRAN 7 atmospheric models were studied to determine solar radiative energies as a function of the time of the year, latitude, and atmospheric conditions (Kneizgs 1988). From this information, the instrument dynamic range as a function of wavelength was estimated. The measurement conditions of the instrument, including both direct sun and off-axis measurements under all expected atmospheric conditions, required the signal dynamic range to cover seven decades of current from 1 pA to 10 μA. Because of the need to make low-level energy measurements, maintaining high measurement accuracy at lower currents was necessary. Atmospheric phenomena such as cloud formation and movement and changes in trace gases occur at a very slow rate from seconds to hours. For this reason, data had to be acquired at a maximum rate of only a few complete spectral samplings per hour, relaxing the front-end electrometer bandwidth requirements. Additionally, the outdoor location of the radiometer required operation over a wide temperature range (0 to 150°F). Practical implementation of 38 channels required the electrometer to be the smallest possible size and lowest cost per channel, directing the development toward monolithically compatible topologies.

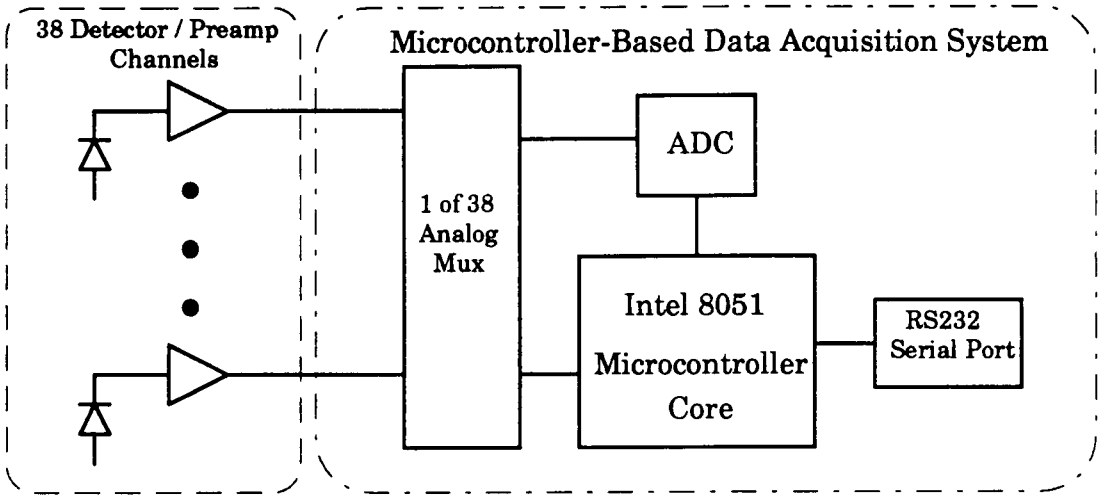


Figure 1.2. Simplified radiometer electronics system block diagram.

Electrometer Topology Review

Various electrometer topologies were considered for use in the radiometer, including continuous time integrators, transimpedance amplifiers, and logarithmic amplifiers. The primary specifications of interest included wide dynamic range, high accuracy at low currents, miniaturized implementation, and straightforward calibration.

Continuous time integrators and transimpedance amplifiers are classified as linear amplifiers and exhibit dynamic range limitations. For these topologies, measurement resolution is a strong function of the position within the range. A linear system optimized for use with a 12-bit data acquisition system requires four feedback configurations to obtain a minimum 1% resolution for seven decades of input signal. This requirement is based on a single range covering approximately one and three-fourths decades of input signal. Extending the measurement range by switching the feedback elements causes several potential problems. First, switches contribute input node leakage current and thus degrade the low-current measurement accuracy of the instrument. In addition, multirange instruments require multiple calibration procedures unless costly, high-precision feedback elements are used. Finally, implementing 38 channels using switched feedback elements requires a large physical area and is not amenable to monolithic construction. These problems exist for both the continuous time integrator and transimpedance topologies. The dynamic range limitations and the implementation and calibration complications make these topologies impractical for this particular application.

Logarithmic amplifiers use a nonlinear feedback element, such as a diode or transistor junction, to obtain logarithmic compression of the input signal. Use of compression allows the measurement of signals with wide dynamic range, eliminating the need for switched feedback elements. The measurement resolution of a log amp is not

absolute as in linear amplifiers but is a fixed percentage of the input signal amplitude. For example, a log amp with a 12-bit data acquisition system and seven decades of input signal provides ~0.4% resolution of the input signal. Figure 1.3 demonstrates the resolution advantage of logarithmic amplifiers over linear amplifiers for wide-range operation. Clearly, logarithmic amplifiers have both range, implementation, and calibration advantages over linear amplifiers for this particular application.

Temperature issues were another area of particular concern when the appropriate electrometer topology was being determined for the radiometer. Transimpedance amplifiers are well behaved over extended temperature ranges, as can be continuous time integrators, if the feedback elements are properly selected with a low temperature coefficient. However, logarithmic amplifiers are often rejected for use in many applications because of poor temperature stability.

Present State of Logarithmic Amplifier Circuits

In an effort to address the logarithmic amplifier temperature compensation issue, an extensive literature search was performed to determine the state of the art in temperature compensation techniques. Logarithmic amplifiers with <2% error over nine decades at room temperature have been reported (Kennedy 1970). Commercially produced hybrid amplifier units can be trimmed for <0.6% error at a constant temperature and <4.5% error over a 20°C span for six-decade operation (1 nA to 1 mA) (Sheingold 1976). One commercially produced monolithic logarithmic amplifier is specified for 1.25% error for six decades (1 nA to 1 mA) over a temperature range of 0 to 70°C, but it does not have the low-current measurement accuracy required and is not recommended for new designs by the manufacturer (HSC 1990). Techniques implementing analytical correction of temperature

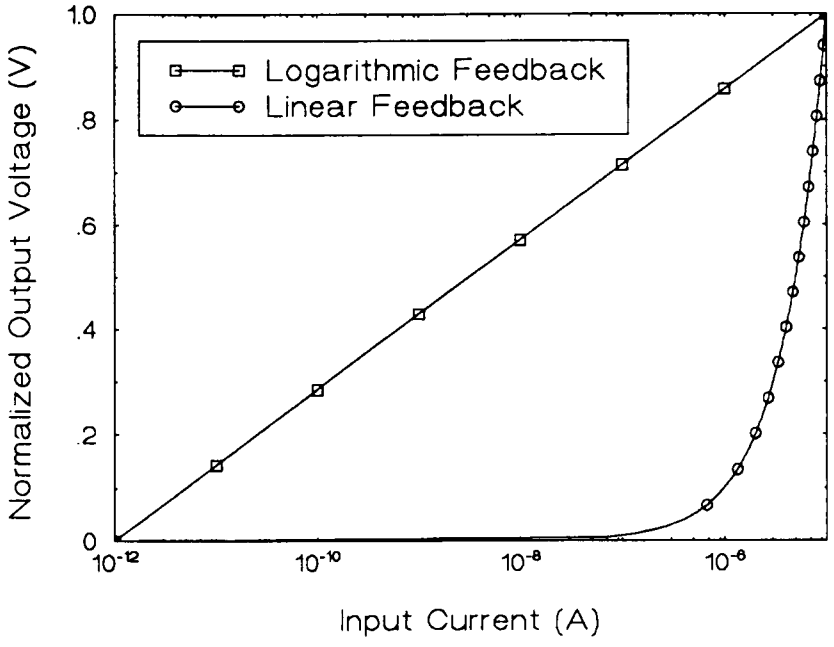


Figure 1.3. Resolution comparison of linear and logarithmic feedback methods.

errors over extended temperature ranges have been reported, resulting in <10% error over seven decades of input current (Huggins 1973). Clearly, the temperature compensation issue has been addressed but not adequately resolved to meet the particular range, accuracy, and temperature requirements of this application.

Summary

The dynamic range and implementation goals of this circuit development make it apparent that the logarithmic amplifier has advantages over linear feedback circuits in terms of dynamic range, implementation, and calibration. However, a review of the state of the art in logarithmic circuits has clearly revealed that the problem of temperature compensation has yet to be resolved for applications such as this one.

Chapter 2

TEMPERATURE COMPENSATION OF LOGARITHMIC AMPLIFIERS

Discussion of Logarithmic Conversion Methods

Logarithmic compression is achieved by using a nonlinear feedback element and exploiting the current-voltage relationship of a pn junction to generate an output voltage that is logarithmically related to the input current. Nonlinear silicon junction devices used for this application commonly include diodes and bipolar junction transistors (BJTs).

A diode exhibiting ideal logarithmic conformance has the following current-voltage relationship:

$$I_D = I_S\left(e^{\frac{qV}{mkT}} - 1\right), \tag{2.1}$$

where I_S is the device saturation current and m = 1. However, diodes have a very limited range in which acceptable logarithmic conformance can be observed. At higher currents, logarithmic conformance errors result from device ohmic bulk resistance. At currents below 10 nA, the value of m changes from 1 to between 1.5 and 2, the result of recombination of holes and electrons in the space-charge region (Kennedy 1988). This results in a slope change because the recombination current dominates over the injected current component [see Equation (2.1)] at low current levels.

For applications requiring many decades of input signal, BJTs provide better accuracy over extended current ranges than do diodes. A much simplified expression for the relationship between the base-emitter voltage and the collector current is

$$I_C \approx I_S\left(e^{\frac{qV_{BE}}{mkT}} - 1\right). \tag{2.2}$$

For selected BJTs, m = 1 for a collector current range of <1 pA to >0.1 mA, providing more than eight decades of good logarithmic conformance (Kennedy 1988). Because of the superior logarithmic performance of the transistor, further analysis will be restricted to transistor feedback elements.

The Gummel-Poon model for the bipolar transistor is demonstrated in Figure 2.1 (Getreu 1976). Here, the collector current under low-level injection conditions is defined as

$$I_C = I_{CT} + I_{CBO} + I_{SUB}\,, \tag{2.3}$$

where

$$I_{CT} = I_{CC} - I_{EC} = I_S\left[\left(e^{\frac{qV_{BE}}{kT}} - 1\right) - \left(e^{\frac{qV_{BC}}{kT}} - 1\right)\right] \tag{2.4}$$

and

$$I_{CBO} = -C_4 I_S\left(e^{\frac{qV_{BC}}{n_{CL}kT}} - 1\right) - \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{kT}} - 1\right). \tag{2.5}$$

Low-level injection refers to the case where injected electrons and holes do not appreciably change the total majority carrier density from its equilibrium value (Muller and Kamins 1986). I_{CT} is the linking current between the emitter and the collector that results from the injected carriers into the base region because of base-emitter and base-collector potentials. I_{CBO} represents the collector-base leakage current components and I_{SUB} is the collector-to-substrate leakage current. I_{SUB} is due to the well-substrate interface that in many applications can represent a large area pn junction. I_{SUB} can be eliminated by use of a dielectric isolation (DI) fabrication process where a silicon dioxide (SiO_2) layer is placed between the transistor well and the substrate, minimizing leakage.

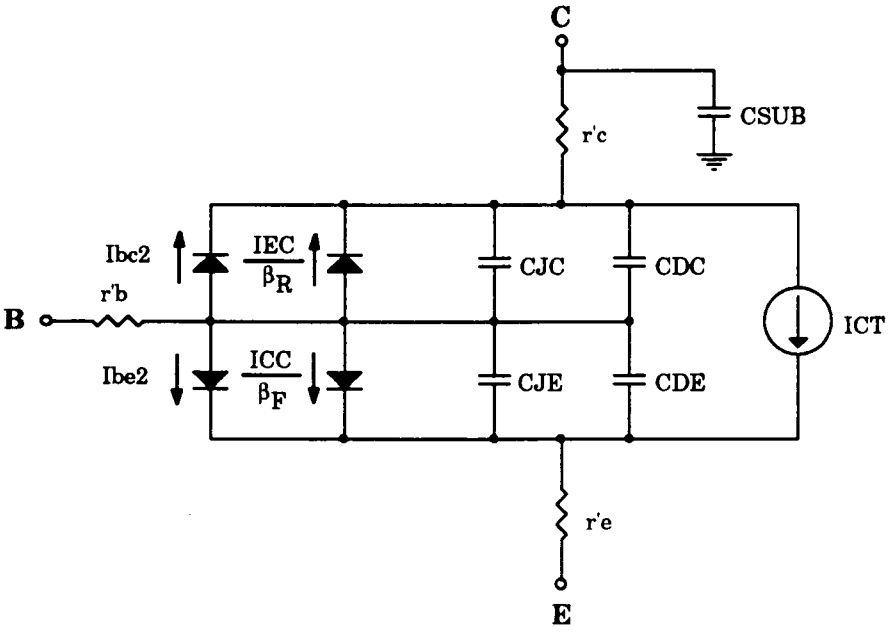


Figure 2.1. Gummel-Poon transistor model.

The collector-base leakage current I_{CBO} can be represented, using SPICE notation, as

$$I_{CBO} = -ISC\left(e^{\frac{qV_{BC}}{NCkT}} - 1\right) - \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{NRkT}} - 1\right), \tag{2.6}$$

where *ISC* is the base-collector leakage saturation current, *NC* is the base-collector leakage emission coefficient, β_R is the ideal maximum reverse beta, and *NR* is the reverse current emission coefficient. *NC* and *NR* have SPICE default values of 2 and 1, respectively, and account for a slope difference between the two components. The first term of Equation (2.6) refers to the recombination-generation currents associated with the base-collector junction, and the second term models the diffusion current component in the base-collector junction. In silicon at normal operation temperatures, the recombination-generation component tends to dominate at small forward voltages, and the diffusion component dominates at larger forward voltages (>0.5 V) (Grove 1967). However, maintaining V_{BC} at zero volts will eliminate all V_{BC}-dependent components of I_C, thus reducing Equation (2.3) to

$$I_C = I_S\left(e^{\frac{qV_{BE}}{kT}} - 1\right). \tag{2.7}$$

Log slope deviations in I_C resulting from modulation of the active base region majority charge due to V_{BE} are included in the Gummel-Poon model. Therefore,

$$I_C = \frac{I_{SS}}{q_b}\left(e^{\frac{qV_{BE}}{kT}} - 1\right), \tag{2.8}$$

where I_{SS} is the zero bias saturation current and q_b is the majority charge in the base. I_{SS} is defined as

$$I_{SS} = \frac{q\tilde{D}_n n_i^2 A}{\int_{X_{EO}}^{X_{CO}} N_A(x)dx} \tag{2.9}$$

and is dependent on the area, doping, and total charge in the base. The denominator term represents the charge per unit area in the base under zero bias conditions. Additionally, I_{SS} exhibits a strong temperature dependence

$$I_{SS} \propto T^4 e^{\left(\frac{-qV_{GO}}{kT}\right)}, \tag{2.10}$$

where V_{GO} is the band-gap voltage of silicon extrapolated to zero degrees Kelvin (Gray and Meyer 1984). Referring back to Equation (2.8), q_b, the majority charge in the base, can be expressed as a function of several components, each representing normalized base charge components:

$$q_b = 1 + q_e + q_c + q_f + q_r . \tag{2.11}$$

In this equation, q_e models the modulation of the base resulting from the variation of the emitter-base space-charge layer width due to V_{BE} (late effect), q_c models the basewidth modulation by the variation of the collector-base space charge layer width due to V_{BC} (Early effect), q_f is the normalized excess majority carrier concentration in the base when V_{BE} is applied to the base-emitter junction and V_{BC} = 0, and q_r is the normalized excess majority carrier concentration in the base when V_{BE} = 0 and V_{BC} is nonzero (Getreu 1976). Note that q_f and q_r model effects occurring under high-level injection and can be neglected under low-level injection. Likewise, q_c can be neglected because it is resultant from V_{BC} bias. Therefore, under low-level injection with V_{BC} = 0, one can assume $q_c = q_f = q_r \approx 0$, resulting in

$$q_b \approx 1 + q_e . \tag{2.12}$$

The collector current expression then becomes approximated by

$$I_C = \frac{I_{SS}}{1+q_e}\left(e^{\frac{qV_{BE}}{kT}} - 1\right). \tag{2.13}$$

The term q_e can be approximated in terms of the base-emitter junction voltage and the SPICE parameter V_B, the reverse early voltage, as (Getreu 1976)

$$q_e = \frac{V_{BE}}{VB}. \tag{2.14}$$

Substituting Equation (2.13) into Equation (2.14) and assuming q_e << 1, the collector current becomes

$$I_C \approx I_{SS}\left(e^{\frac{qV_{BE}}{NFkT}} - 1\right), \tag{2.15}$$

where *NF* is the forward current emission coefficient (SPICE terminology) and is expressed as

$$NF = \frac{1}{1 - \frac{kT}{qVB}}. \tag{2.16}$$

For all collector current values of interest, the exponential term in Equation (2.15) >> 1, allowing the following collector current approximation that is a perfect logarithmic converter:

$$I_C \approx I_{SS}\left(e^{\frac{qV_{BE}}{NFkT}}\right). \tag{2.17}$$

Temperature Dependence of Logarithmic Conversion Methods

The temperature dependence of I_{SS} [demonstrated in Equation (2.10)] is commonly removed by using the logarithmic amplifier topology of Figure 2.2. With assumed negligible

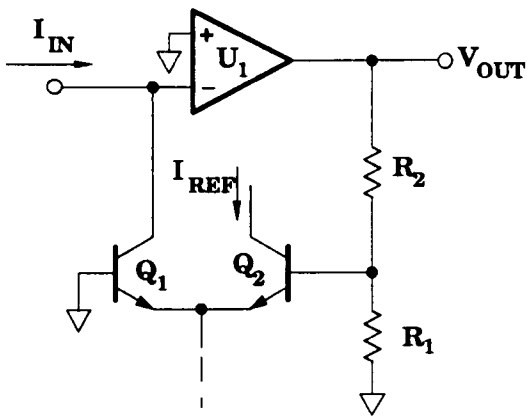


Figure 2.2. Logarithmic amplifier executing V_{BE} differencing for I_{SS} cancellation.

input leakage current into opamp U_1, the input signal current becomes the collector current of Q_1. The transistor Q_2 is maintained at a constant collector current I_{C2}. Changes in the input signal cause a change in V_{BE} [refer to Equation (2.17)], resulting in an equal base voltage change in Q_2. Resistors R_1 and R_2 provide a gain function for relating V_{BE2} back to the output of U_1. This topology performs a V_{BE} differencing of Q_1 and Q_2, resulting in the relationship

$$V_{OUT} = (NF)\left(\frac{kT}{q}\right)\left(1+\frac{R_2}{R_1}\right)\ln\left(\frac{I_{REF}I_{SS1}}{I_{IN}I_{SS2}}\right). \tag{2.18}$$

If the transistors are perfectly matched and at the same temperature, the saturation current components cancel and Equation (2.18) reduces to

$$V_{OUT} = K_1 \log\left(\frac{I_{REF}}{I_{IN}}\right), \tag{2.19}$$

where K_1 is the log conversion slope factor defined in volts per decade as

$$K_1 = NF\left(1+\frac{R_2}{R_1}\right)\left(\frac{kT}{q}\right)\ln(10). \tag{2.20}$$

Mismatch of the transistors Q_1 and Q_2 produces an offset voltage defined by

$$(V_{OS})_{OUT} = K_1 \log\left(\frac{I_{SS1}}{I_{SS2}}\right), \tag{2.21}$$

which must be added to Equation (2.19). Transistor matching is usually specified in terms of V_{BE}. A V_{BE} offset of ±0.25 mV corresponds to approximately ±1% I_{SS} mismatch at 300 K. Compensation for this offset can be accomplished by offsetting the output voltage or adjustment of the reference current in Q_2 (refer to Figure 2.2). The remaining temperature dependence is that associated with the two primary components of the log scale conversion factor, namely the thermal voltage and *NF* temperature dependence. If the error associated

with the log conversion scale factor is defined as ε_k, then the input-referred error in the ith decade is

$$\varepsilon_i = \left(e^{-i\varepsilon_k \ln(10)} - 1\right) . \tag{2.22}$$

Note that only a 0.07% scale factor error is required to produce a 1% input-referred error in the lowest measurement decade of a seven-decade logarithmic amplifier. For this reason, careful compensation of scale factor temperature dependencies is necessary for high-accuracy, wide-range measurement.

Conventional Temperature Compensation Methods

Previously reported methods for compensation of the log scale factor involve the use of a positive temperature coefficient (TC) element for R_1 in Equation (2.20). At 300 K, the output voltage of the logarithmic amplifier topology of Figure 2.3, designed for 1-V output per decade of input current, has a temperature coefficient of 3360 ppm/°C. One method uses a 1000-Ω wirewound resistor with a nominal temperature coefficient of 3500 ppm/°C at 25°C (Kennedy 1970), and another implements 52.4% of R_1 with a precision 470-Ω resistor and the remainder with a silicon resistor (Sensistor) with a nominal temperature coefficient of ~0.7%/°C at 25°C (NSC 1986). Figure 2.4(a) shows the resistance versus temperature characteristic for the wirewound resistor. These curves were computed by using the nominal +25°C value and a TC of 3500 ± 300 ppm/°C (Tel Labs 1991). From the data provided in Table 2.1, the worst-case resistance curves for the Sensistor were computed and are shown in Figure 2.4(b) (Unitrode 1987). The manufacturer's specifications were interpreted as meaning that a ±5% shift in the nominal value at 25°C could additionally be accompanied by a change in the overall slope of the curve, with either end varying as much as ±9%. Using this definition maintains the general second-order curve shape characteristic of a nonlinear resistive device.

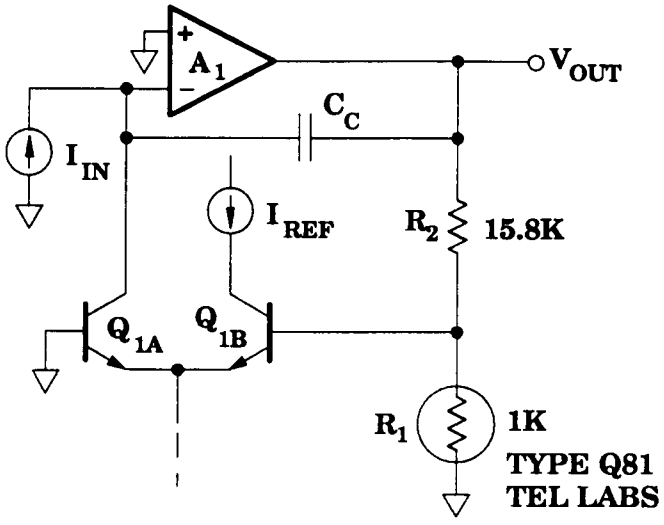
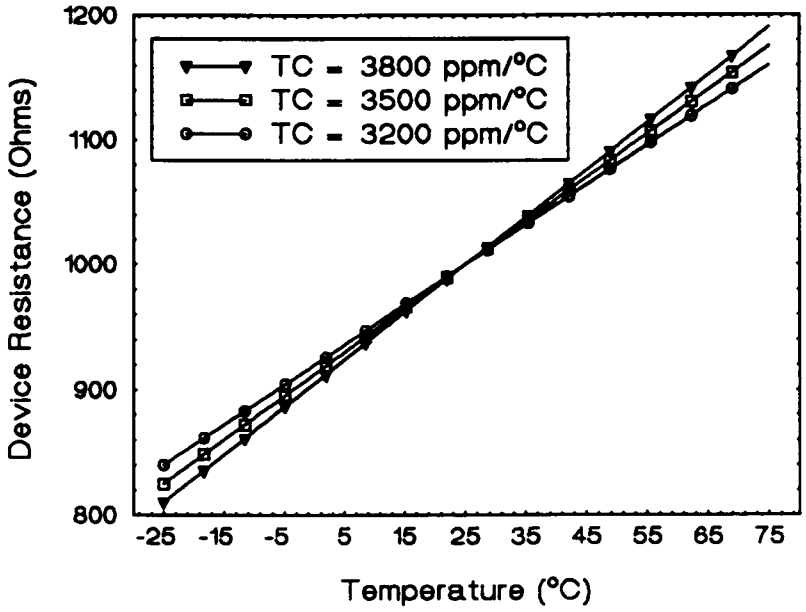
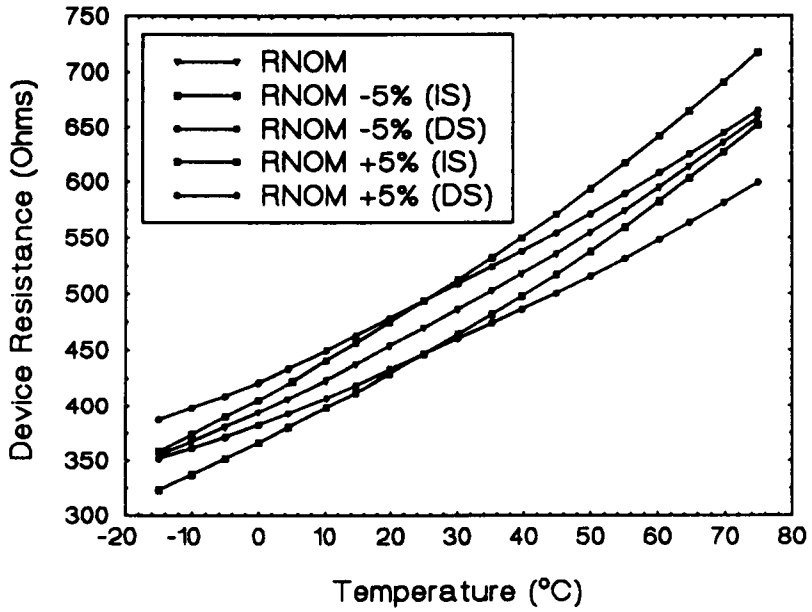


Figure 2.3. Temperature-compensated logarithmic amplifier using a positive temperature coefficient resistor.



(a)



(b)

Figure 2.4. Resistance vs temperature for (a) Q81 wirewound resistor and (b) Sensistor.

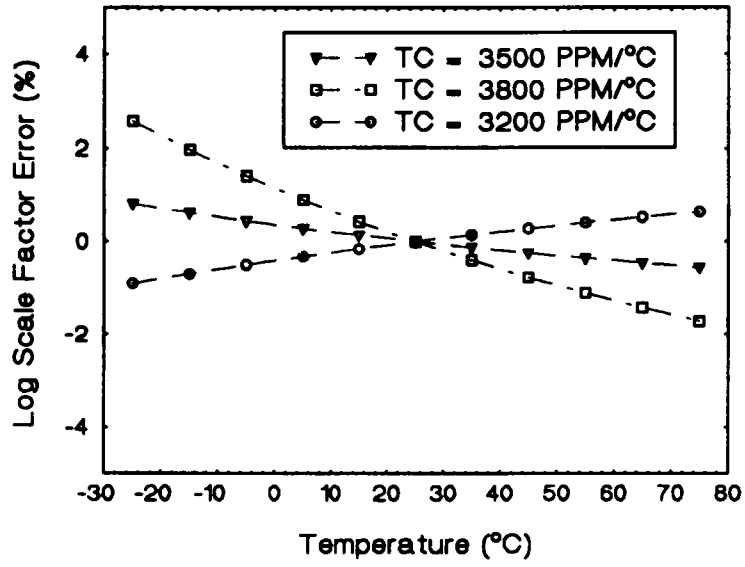
Table 2.1. Sensistor temperature characteristics from manufacturer's data sheet

Temperature (°C)	Nominal value (Ω)	Value variation for ±5% tolerance
-15	354.85	±9%
0	393.86	±7%
25	470.00	±5%
50	554.20	±7%
75	658.00	±9%

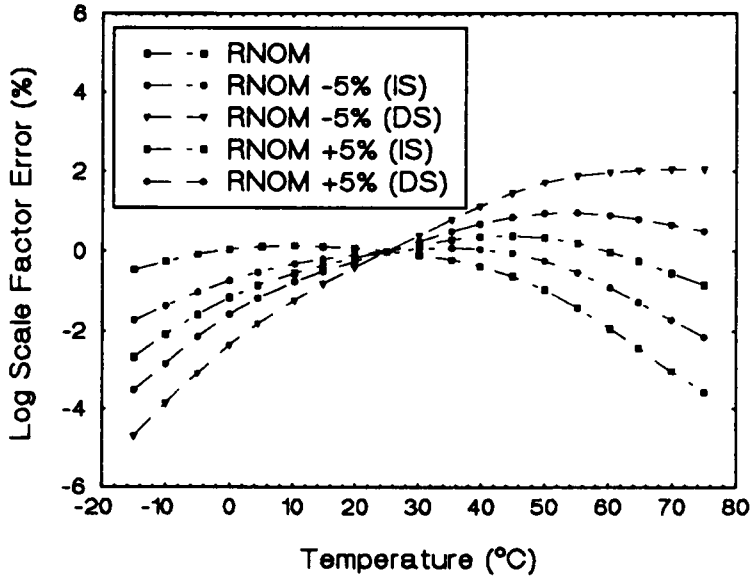
The Q81 wirewound resistor exhibits good linearity but has poor TC control. The theoretical error in the log scale factor calculated from the predicted resistance measurements over temperature is shown in Figure 2.5(a).

The log conversion scale factor errors for the Sensistor are shown in Figure 2.5(b). In this figure, IS and DS represent increased slope and decreased slope, respectively, and refer to the direction the ±5% resistance curve has been tilted. Additionally, ±5% resistance value offset at 25°C has been adjusted to the nominal 470 Ω for all the curves, resulting in 0% log conversion scale factor error at this temperature. This offset adjustment would be physically accomplished by trimming R_1. The Sensistor suffers both a nonlinear TC and a nonlinear variation in the reference resistance values over temperature.

Both methods are clearly incapable of 1% input-referred accuracy in the seventh decade, especially when the TC matching errors and nonlinearity over temperature are taken into consideration. The theoretical errors associated with using both of the previously mentioned positive TC elements are shown in Figures 2.6(a) and 2.6(b). Errors associated with using Q81 wirewound resistor reach nearly 35% over a –25 to 75°C range [Figure 2.6(a)]. Similarly, the errors associated with the Sensistor reach nearly 120% at –15°C [Figure 2.6(b)]. Although the measurement errors of Figure 2.6 do incorporate predicted tolerance variations in the reference values and TC and anticipated device nonlinearities,

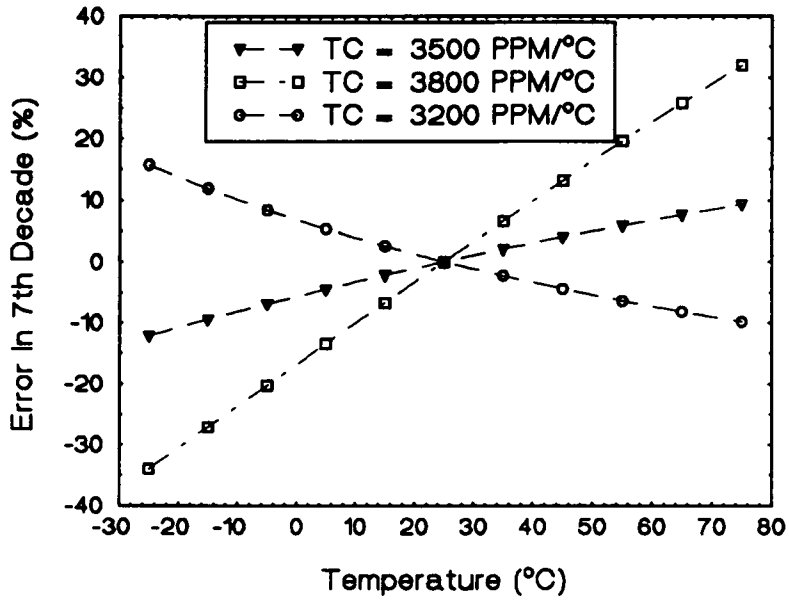


(a)

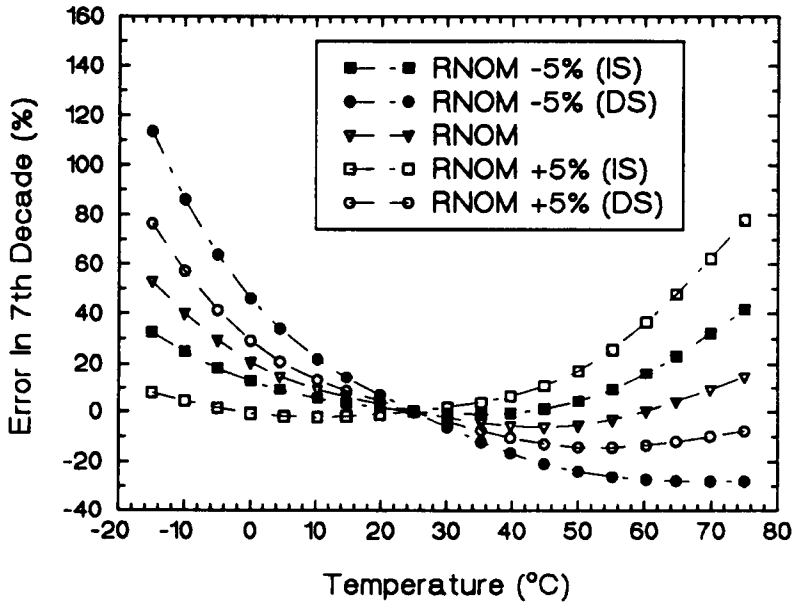


(b)

Figure 2.5. Log scale factor error for (a) Q81 wirewound resistor and (b) Sensistor.



(a)



(b)

Figure 2.6. Predicted input-referred measurement errors using positive temperature coefficient elements: (a) Q81 wirewound resistor and (b) Sensistor.

these are not to be considered as absolute worst-case predictions. These temperature compensation methods depend on the same temperature for the logging transistors and the compensation element. In practice, perfect tracking is not possible by using these methods, because of air temperature gradients, different thermal time constants, and different self-heating rates for the two devices.

New Temperature Compensation Method

A much improved temperature compensation technique is shown in Figure 2.7. This new method is based on using a matched, quad monolithic transistor set to produce two temperature-dependent output voltages that are ratioed to remove the temperature dependency. The transistor set Q_{1A} and Q_{1B} is used to form a logarithmic amplifier for measuring the input signal current. Transistor set Q_{2A} and Q_{2B} is used to generate a temperature-dependent voltage source by biasing the transistor collectors at a 10:1 ratio. This ratio will produce the output characteristic

$$V_{OUT2} = K_2 \log(10) , \tag{2.23}$$

where

$$K_2 = \left(1+\frac{R_4}{R_3}\right)\left(NF_2\right)\left(\frac{kT_2}{q}\right)\ln(10) . \tag{2.24}$$

With Q_1 and Q_2 fabricated on the same chip and $T_1 = T_2$, the ratioing of the two output voltages produces a temperature-compensated output voltage

$$V_{OUT} = \frac{V_{OUT1}}{V_{OUT2}} = \frac{\left(1+\frac{R_2}{R_1}\right)}{\left(1+\frac{R_4}{R_3}\right)}\log\left(\frac{I_{REF}}{I_C}\right) . \tag{2.25}$$

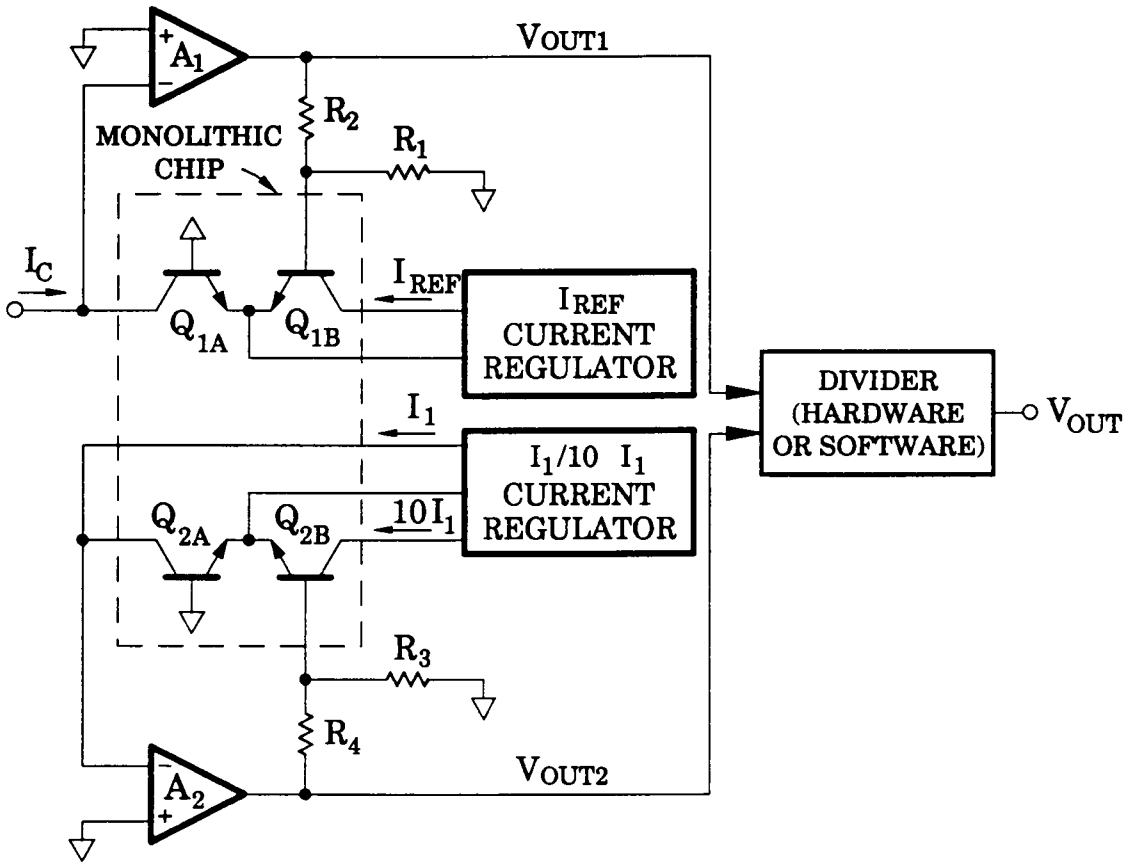


Figure 2.7. Seven-decade temperature-compensated logarithmic amplifier topology.

Notice that in Equation (2.25), it has been assumed that $NF_1 = NF_2$, allowing cancellation of these two parameters and their temperature dependence [refer to Equation (2.16) for *NF* definition]. The scale factor error resultant from the temperature dependence of *NF* over a range of –25 to 75°C is ±0.15%, resulting in an input-referred measurement error of ±2.4% in the seventh decade (for V_B = 3V). With assumed excellent thermal tracking between Q_1 and Q_2, the temperature dependency of *NF* would be negligible. Therefore, the primary factor causing an *NF* mismatch would be an offset in the *VB* (reverse Early voltage) between the transistor pairs. A worst-case mismatch of *VB*, for Q_1 and Q_2 monolithically connected, is estimated at ±10%. Over a temperature range of –25 to 75°C, the *NF* error resulting from this mismatch is ±0.0105%, resulting in an input-referred measurement error in the seventh decade of only ±0.17%. *NF* temperature dependence and *VB* mismatch can be neglected if Q_1 and Q_2 are monolithically connected to obtain excellent transistor matching and thermal tracking.

This new temperature compensation method will provide much improved temperature compensation for I_{SS}, *NF*, and the thermal voltage because of excellent temperature tracking and parameter matching between the monolithically connected transistor pairs.

Chapter 3

CIRCUIT IMPLEMENTATION AND ANALYSIS

Introduction

This chapter presents a detailed description and analysis of the logarithmic amplifier and its implementation. Basic circuit design techniques and justifications are given, specifics of device selection and characterization over temperature are presented, and calibration methods used for correction of the amplifier are outlined. Additionally, a complete stability analysis, including compensation techniques implemented, is detailed. Where appropriate, PSPICE simulations and actual circuit measurements are used to support analytical results.

Circuit Implementation

The detailed circuit schematic of the newly developed temperature-compensated logarithmic amplifier is shown in Figure 3.1. The nominal 300-K log conversion scale factor of V_{OUT1} is set at 1 V/decade by R_1 and R_2. This configuration will result in an output voltage range of 0 to 7 V corresponding to a 10-μA to 1-pA input current respectively. The V_{OUT2} channel, used as a temperature tracking voltage source, is also set to a nominal 300-K level of 1 V by R_3 and R_4. These resistors were chosen to have low values to minimize the output offset due to the base current of Q_{1B} and Q_{2B}.

All leakage currents at the input node add to or subtract from the input signal, directly contributing an input error. For this reason, the input devices, input opamp (U_1), logarithmic transistor (Q_{1A}), and feedback capacitor (C_{C1}) were carefully selected to provide the best accuracy over temperature.

Selection of the input opamp involved investigating commercially available electrometer-grade opamps and comparing the characteristics of interest. Table 3.1 shows

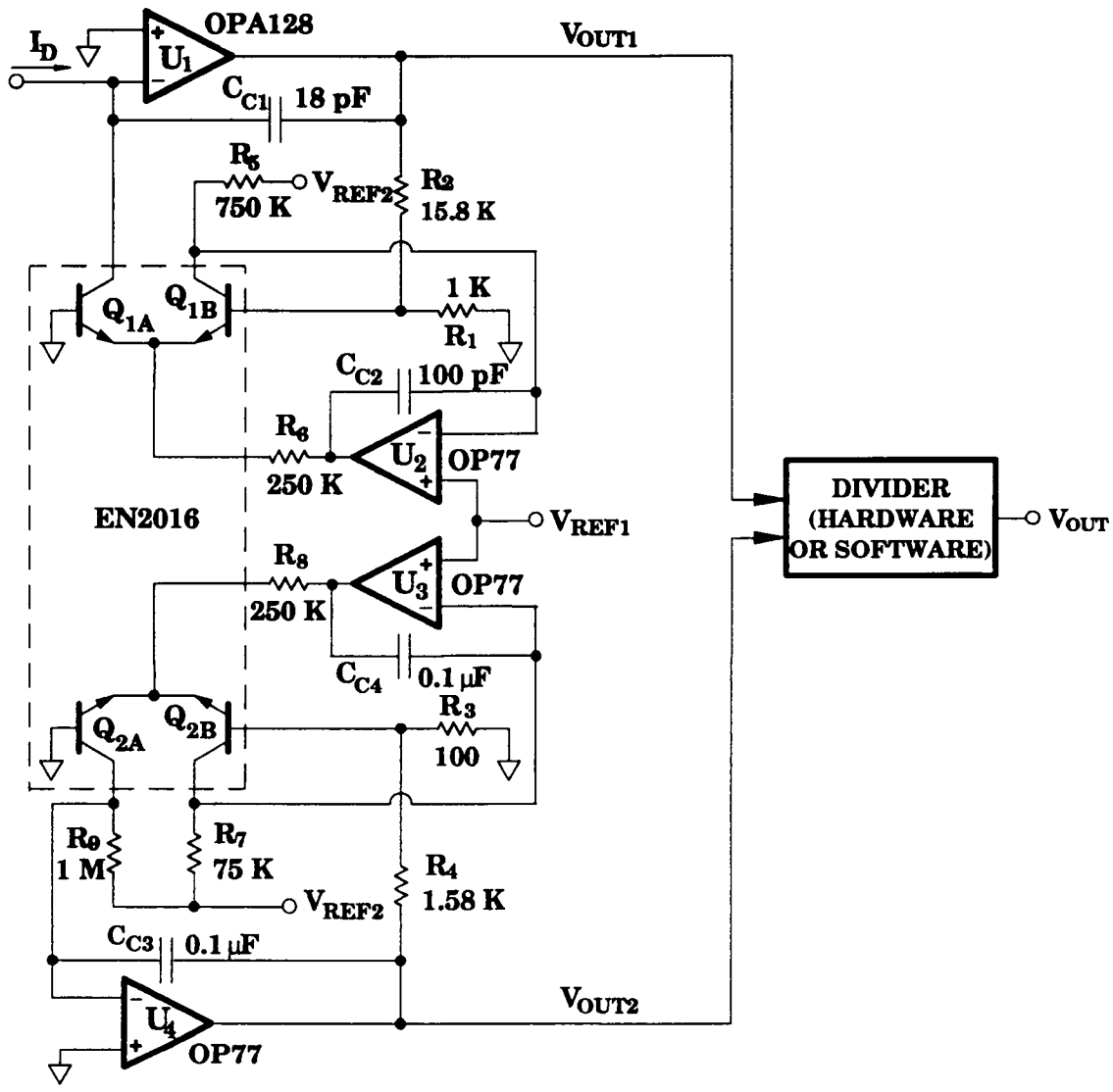


Figure 3.1. Complete temperature-compensated logarithmic electrometer.

the three primary electrometer-grade amplifiers considered and a comparison of the primary parameters of concern. These parameters were taken from manufacturers' data sheets and reflect values for full military temperature operation (–55 to +125°C), unless otherwise specified.

Table 3.1 Comparison of commercially available electrometer-grade opamps

Device	Input bias current (max)	Input offset voltage (min)	Avo (typical)	Gain bandwidth product (typical)
OPA128LM	±2 pA	±750 μV	110.9 dB	1 MHz
CA5420A	15 pA	5 mV	87 db	0.5 MHz
OP80E	50 pA	8 mV	125 dB	0.3 MHz

The input bias current and its associated TC can be considered a direct error term at the input of the electrometer. The input offset voltage also contributes a significant input error value, as will be described later in this chapter. A high open-loop gain and gain bandwidth product will facilitate wider closed-loop bandwidths and are considered desirable. As demonstrated in Table 3.1, the OPA128LM exhibits superior performance in nearly all categories considered. For this reason, the OPA128LM opamp was chosen for its combination of low offset voltage, low input bias current, high open-loop gain, and good gain-bandwidth product. Figure 3.2 shows the measured input offset voltage and input bias current vs temperature for the OPA128LM opamp, which has dielectrically isolated junction field-effect transistor (JFET) input devices. Figures 3.3 and 3.4 show the measured input offset voltage as a function of temperature for the OP80E and CA5420A respectively. The results presented in these figures agree well with those on the manufacturers' data sheets.

Transistor geometric properties play an important role in the transistor parameters. Larger devices tend to exhibit better matching between pairs and exhibit the ability to maintain h_{fe} at higher collector currents because of decreased ohmic resistances. However,

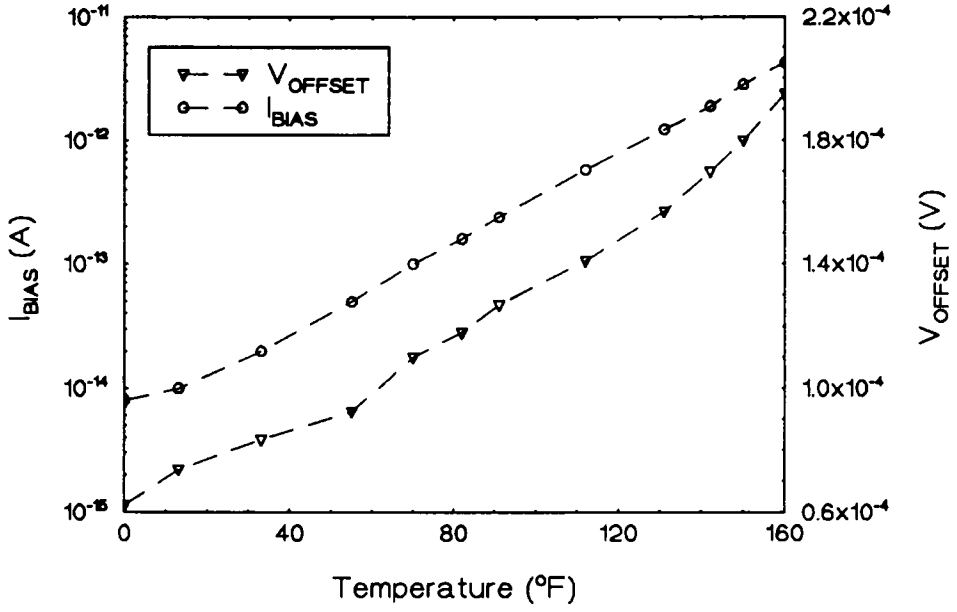


Figure 3.2. OPA128LM input bias current and offset voltage vs temperature.

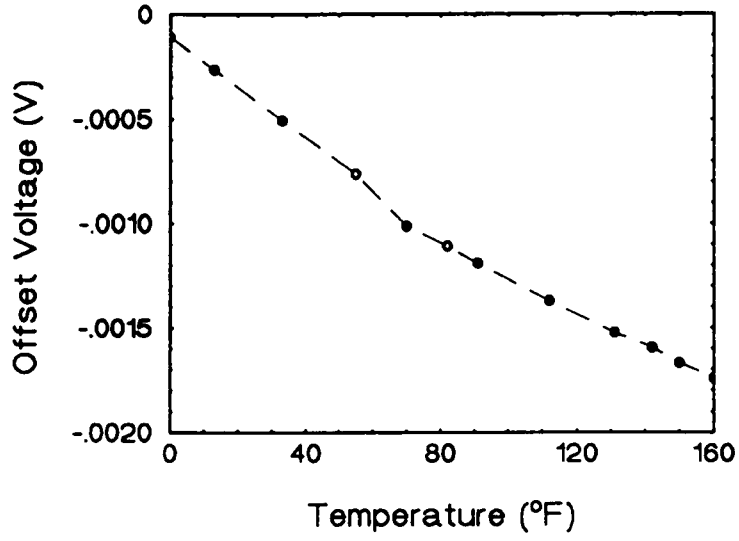


Figure 3.3. Measured OP80E input offset voltage vs temperature.

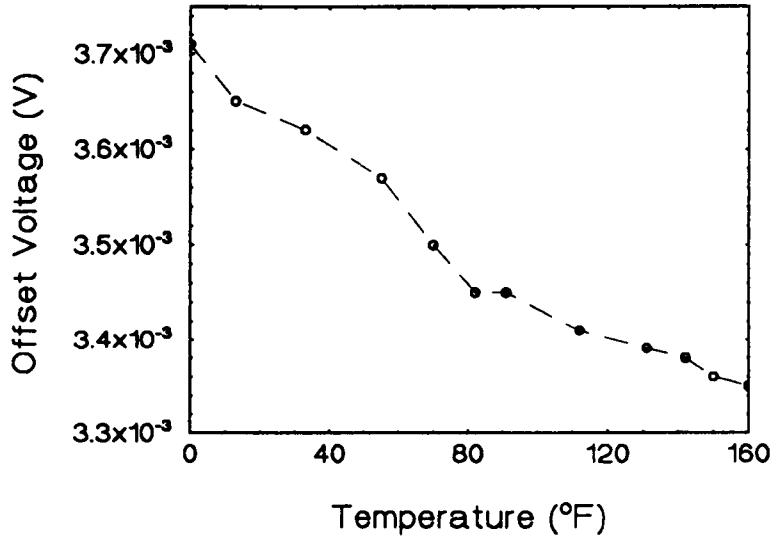


Figure 3.4. Measured CA5420A input offset voltage vs temperature.

junction leakage currents are a direct function of the junction area, causing larger devices to exhibit larger errors at low currents because of increased junction leakage components. The trade-offs between matching, dynamic range, and leakage require the selection process to involve a thorough investigation of devices including parameter measurement. For this reason, extensive device testing was performed for selection of the logarithmic transistor set. As previously mentioned, monolithic construction of both transistor sets is imperative to ensure proper parameter matching and thermal tracking of these pairs. The EN2016 quad npn transistor array best met these objectives. Figure 3.5 shows the Gummel plot for the device. The array exhibited good logarithmic conformance over eight decades, and reasonable h_{fe} over the entire range of collector currents. Figure 3.6 shows h_{fe} as a function of I_C for the EN2016. A large h_{fe} at high collector currents will minimize the output offset error due to the base current of Q_{1B} and Q_{2B} (refer to Figure 3.1). The collector-base leakage current as a function of temperature and V_{CB} is plotted in Figure 3.7. Devices under test were heated by using a resistive element and allowed proper time for temperature stabilization. Exact device temperature was determined by measuring the slope of the log of I_C vs V_{BE}. As predicted by Equation (2.6), the increasing leakage current I_{CB} is a function of V_{CB}, which demonstrates the need for U_1 to have a low input offset voltage. Though other monolithic transistor pairs were tested, no other quad monolithic sets were investigated.

Compensation capacitors C_{C1}, C_{C2}, C_{C3}, and C_{C4} were used to frequency stabilize the four gain loops. A polystyrene capacitor was used for C_{C1} to minimize leakage current into the input node. Polystyrene proves the best fit for this application because of its low temperature coefficient, -120 ± 30 ppm/°C; low leakage, 10^{11} to 10^{12} Ω-μF; and low dielectric absorption, 0.02% (Kennedy 1988). The primary disadvantage of polystyrene is its

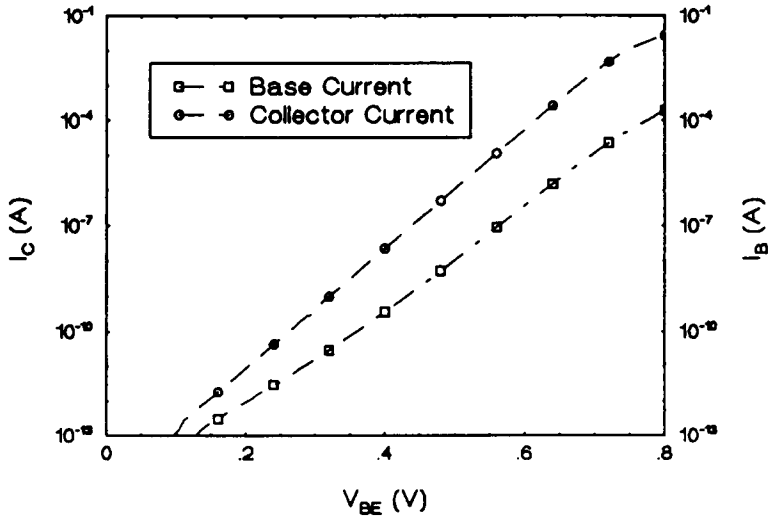


Figure 3.5. Elantec EN2016 quad monolithic array Gummel plot.

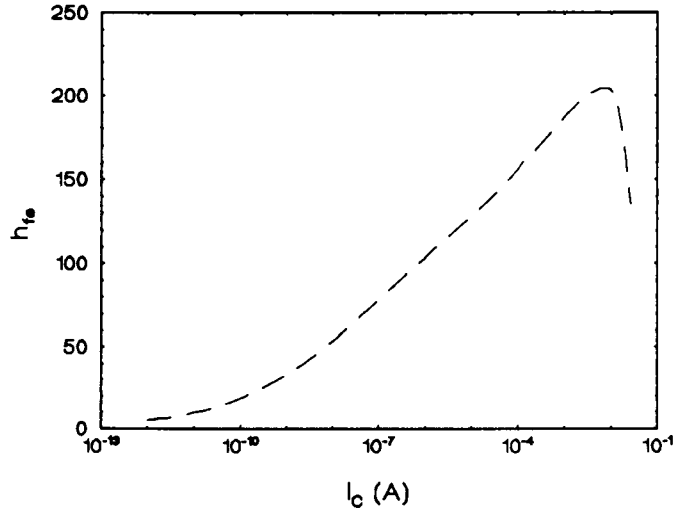


Figure 3.6. Elantec EN2016 h_{fe} vs collector current.

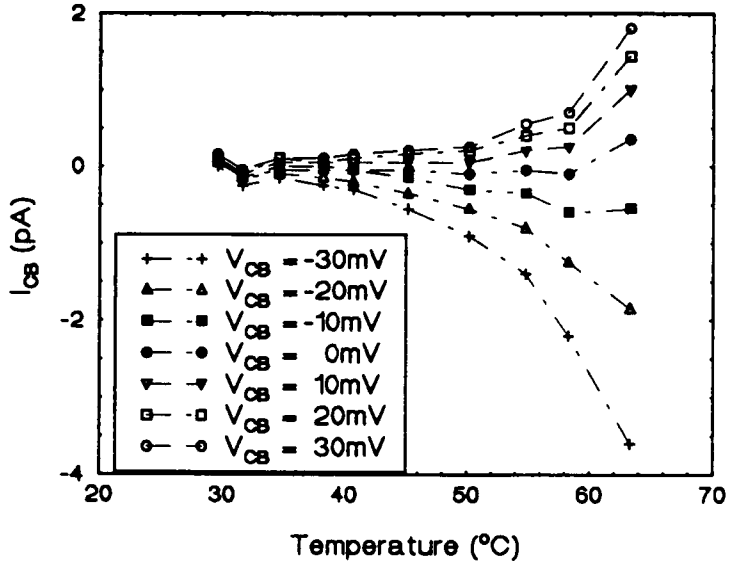


Figure 3.7. Elantec EN2016 collector-base leakage current vs temperature.

large physical size. Frequency compensation of this topology is thoroughly addressed in later sections of this chapter.

The reference currents I_{CQ1B}, I_{CQ2A}, and I_{CQ2B} are generated by fixing precision voltages across stable resistors. Errors in these currents result from errors in the resistance values and reference voltages as well as input offset voltages and bias currents of the opamps used to control the current regulation loops. These errors are minimized by using an accurate voltage reference with low temperature coefficient (0.1% resistance tolerance with 2 ppm/°C TC available) and opamps with low input offset voltages, input bias currents, and associated temperature coefficients. A multiple output voltage reference was used globally in the circuit. The voltage stability of this reference was verified experimentally and found to deviate <0.1% from the nominal values over the entire temperature range, in agreement with the manufacturer's specifications. Figure 3.8 shows the measured voltage error versus temperature for the AD584KH. The OP77EZ used for U_2, U_3, and U_4 has guaranteed maximum input bias current and input offset voltage of 4 nA and 55 μV over temperature (AD 1993) respectively, contributing negligible error to the source current.

Two divider networks, shown in Figure 3.9, were implemented to test the feasibility of ratioing the two temperature-dependent output voltages, V_{OUT1} and V_{OUT2}, by hardware means. In Figure 3.9(a), an analog multiplier is connected as a divider, and the denominator V_{OUT2} is multiplied by 10 to account for the gain in the transfer function of the divider. In Figure 3.9(b), two multiplier chips are used, each operated as a multiplier, which is more tightly specified by the manufacturer than the divider mode.

Techniques common to proper electrometer circuit fabrication were applied in the prototyping and use of the logarithmic electrometer. A Teflon standoff was used at the input node to minimize leakage currents associated with the epoxy-glass printed circuit board material. Handling of the components was kept to a minimum, and circuit

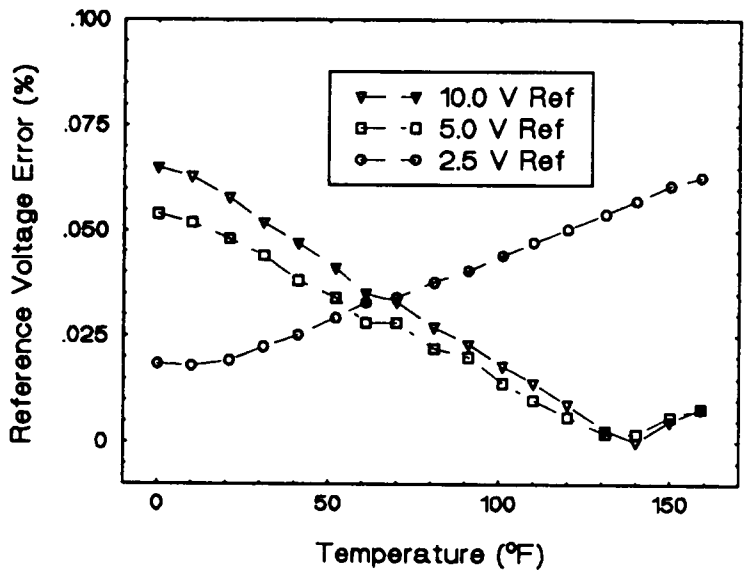
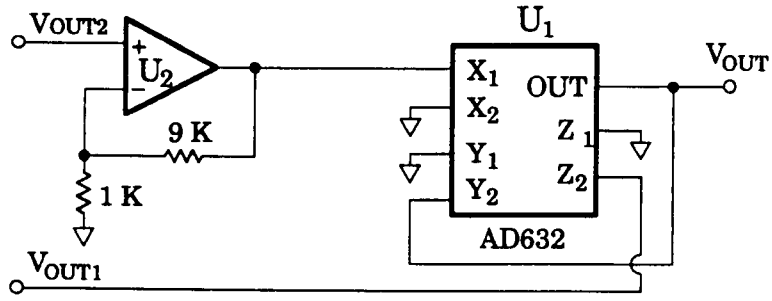
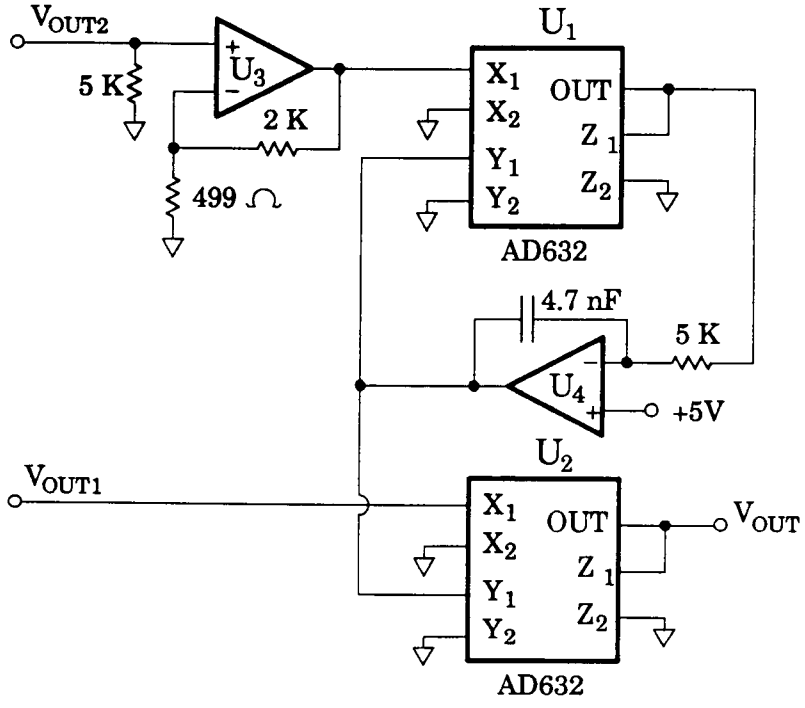


Figure 3.8. AD584 voltage reference error vs temperature.



(a)



(b)

Figure 3.9. Ratioing circuits: (a) divider mode and (b) multiplier mode.

components were thoroughly cleaned to minimize leakage due to skin oils and dirt. Additionally, ground plane was used wherever possible to provide shielding.

Calibration

As previously discussed, the use of well-matched monolithic transistors and appropriate circuit components eliminates the larger sources of error that result from component offset errors and temperature coefficients. However, very small scale factor errors were shown to produce appreciable input-referred errors [refer to Equation (2.22)]. For this reason, a gain adjustment is needed to perform the necessary log conversion slope correction of the output signal ratio. This adjustment can be implemented by either physically trimming one of the R_2/R_1 or R_4/R_3 ratios or by a host processor in instruments using digital data acquisition. In either case, only a single-point calibration is required, preferably in the lower current decades, provided offset errors are negligible. The input calibration current level at which a calibration is performed should be chosen carefully. For accurate trimming of the slope, the lowest possible current unaffected by the input leakage current is preferred. This level will provide the highest resolution for proper correction of the slope and will produce appreciably better correction as the input current increases. Better accuracy can be obtained if the temperature at which the calibration is performed is close to the expected operating temperature range. Calibration is then accomplished by computing a constant that, when multiplied by the ratioed output voltage, will compensate for logarithmic slope errors.

The determination and application of calibration factors is a straightforward procedure. With the use of a known input current, the theoretical output ratio R_T is calculated as follows:

$$R_T = \frac{\ln\left(\frac{I_{REF}}{I_{input}}\right)}{\ln(10)} . \tag{3.1}$$

The actual measured output ratio R_M is determined by

$$R_M = \frac{V_{OUT1}}{V_{OUT2}} . \tag{3.2}$$

The calibration factor, CF, is computed as the ratio of the theoretical to the measured value as shown below:

$$CF = \frac{R_T}{R_M} . \tag{3.3}$$

This calibration factor is then applied to all measured values and the input current calculated as

$$I_{input} = \frac{I_{REF}}{e^{(R_M)(CF)(\ln(10))}} . \tag{3.4}$$

Data presented in later sections were calibrated at both −18 and 21°C with a 100-pA input current by using the previously described procedure.

Improved calibration can be accomplished by correcting for both slope and offset errors. By performing an additional calibration at the highest current value where R_M should equal zero, an offset value can be determined that can be applied to all measurements. Application of both slope and offset correction will produce optimal results.

Stability Analysis

Overview

The complete electrometer circuit is actually composed of two compensated feedback loops as shown in Figure 3.10. One loop is composed of the forward signal path through the amplifier and logarithmic feedback (loop 1), and the second loop is used to set a fixed

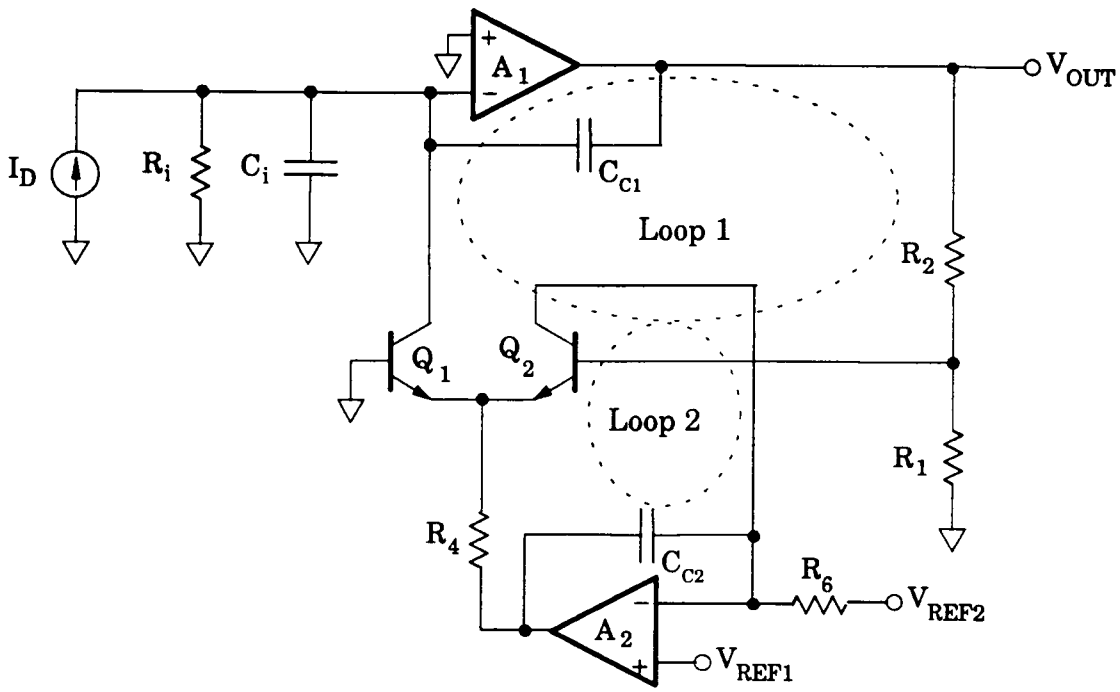


Figure 3.10. Dual compensation loops of the logarithmic electrometer.

reference current in the collector of Q_2 (loop 2). The two loops appear separate but are actually interactive, though the interdependency may be negligible. The initial stability analysis presented in this chapter will assume that the two loops act independently to simplify the analysis. Once a thorough understanding of each loop is achieved, efforts will be focused toward determining how the loops interact and whether this interdependency can be exploited to improve the overall bandwidth of the amplifier.

Loop 1 Stability Analysis

Figure 3.11 shows a simplified circuit equivalent of the uncompensated log amp. The current I_{CQ2} is assumed ideal, thus eliminating loop 2. Though simplified, all elements necessary to address the frequency response and stability of loop 1 are present. Summing the currents at the input node,

$$V_1\left(sC_i+\frac{1}{R_i}\right)=\frac{V_{OUT}(k)}{(re_1)}, \tag{3.5}$$

where k is a attenuation factor from output of A_1 to the base of Q_2 and is expressed as

$$k=\frac{R_1}{R_1+R_2}. \tag{3.6}$$

The transfer function of the logarithmic feedback used in Equation (3.5) is derived in Appendix C. The emitter resistance r_{e1} of Q_1 is related to the device collector current in the following manner:

$$re_1=\frac{V_T}{I_{E1}}=\frac{kT}{qI_{E1}}\approx\frac{kT}{qI_{C1}}. \tag{3.7}$$

Therefore, r_{e1} will change as a function of the amplifier input current. The feedback factor *B(s)* can be expressed as

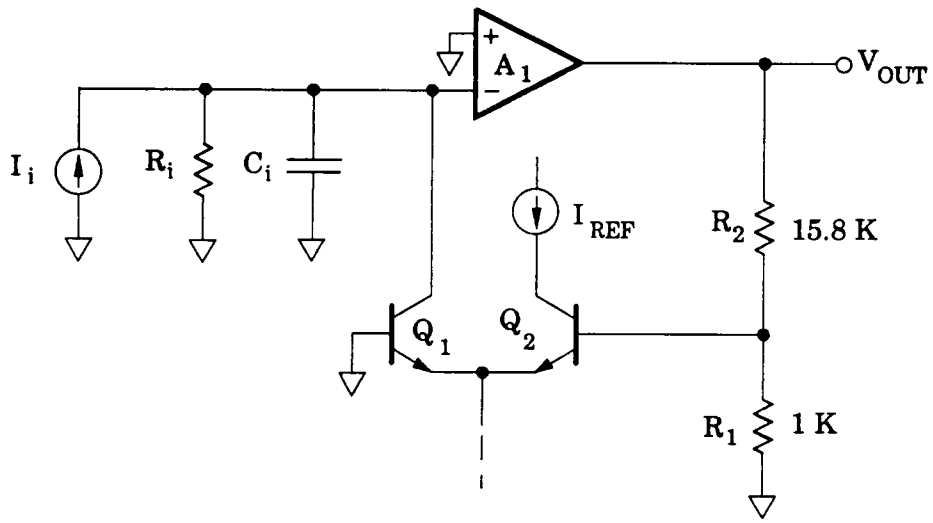


Figure 3.11. Simplified schematic of the uncompensated loop 1.

$$B(s)=\frac{V_1(s)}{V_{OUT}(s)}=\frac{k}{(re_1)\left(sC_i+\frac{1}{R_i}\right)}=\frac{R_i k}{(re_1)(1+sR_iC_i)}\,. \tag{3.8}$$

A simplified model for the input opamp A_1 is expressed as

$$A_1(s)=\left[\frac{A_{o1}}{(1+s\tau_{p1})(1+s\tau_{p2})}\right], \tag{3.9}$$

where A_{o1} is the midband loop gain and τ_{p1} and τ_{p2} are the dominant low and high frequency poles of A_1. The loop gain, $T_1(s)$, is now expressed in terms of the feedback factor and the opamp transfer function:

$$T_1(s)=-A_1(s)B(s)=-\left[\frac{(R_1)(R_i)}{(R_1+R_2)(re_1)}\right]\left[\frac{A_{o1}}{(1+sR_iC_i)(1+s\tau_{p1})(1+s\tau_{p2})}\right]. \tag{3.10}$$

From this equation, the midband loop transmission is

$$T_{1mid}=-\left(\frac{(R_1)(R_i)(A_{o1})}{(R_1+R_2)(re_1)}\right). \tag{3.11}$$

The loop transmission for the uncompensated circuit has three poles. $A_1(s)$ contributes a single low-frequency pole (f_{p1}) due to the gain bandwidth product of the amplifier, and the pole f_{pi} results from the input node equivalent capacitance and resistance. Additionally, the high-frequency pole of A_1, f_{p2} may contribute a significant phase shift depending on its relative position to the 0-dB crossover frequency. Here the dc loop gain is useful in predicting stability. If the loop gain is much higher than A_{o1}, the 0-dB crossover will occur at a much higher frequency, causing the higher frequency poles of A_1 to further contribute phase shift. At dc, R_i can be approximated as

$$R_i \approx r_o=\frac{V_A+V_{CE}}{I_C}\approx\frac{V_A}{I_C} \tag{3.12}$$

for $V_A \gg V_{CE}$. Here, V_A is the early voltage of Q_1, approximately 80 V, and V_{CE} is the Q_1 collector emitter voltage. Therefore, the ratio of R_i to r_e can be approximated as a constant at a given temperature:

$$\frac{R_i}{r_e} \approx \frac{V_A}{V_T}, \tag{3.13}$$

where V_T is the thermal voltage. A 300-K approximation for the dc loop gain is 195 A_{01}. This indicates that instability is very likely. Additionally, one can observe that this three-pole system is, at most, marginally stable and only if f_{p2} does not contribute any phase shift.

Effective compensation of this amplifier configuration is accomplished by the addition of a feedback capacitor which adds a zero to the loop transmission. The compensated circuit is demonstrated in Figure 3.12.

The loop gain expression for the compensated circuit will be derived by the same method used for the uncompensated circuit. Summing the currents at the input node,

$$V_i\left(sC_i + \frac{1}{R_i} + sC_{C1}\right) - V_{OUT}sC_{C1} = \frac{kV_{OUT}}{re_1}. \tag{3.14}$$

All identities are defined as before with the addition of C_{C1}, the feedback capacitance. The feedback factor now becomes

$$B(s) = \left(\frac{kR_i}{re_1}\right)\left(\frac{1 + skre_1C_{C1}}{1 + sR_iC_i + sR_iC_{C1}}\right) = \left(\frac{R_i}{r_f}\right)\left[\frac{1 + sr_fC_{C1}}{1 + sR_i(C_i + C_{C1})}\right], \tag{3.15}$$

where

$$r_f = (re_1)\left(\frac{R_1 + R_2}{R_1}\right). \tag{3.16}$$

The loop gain can be expressed as

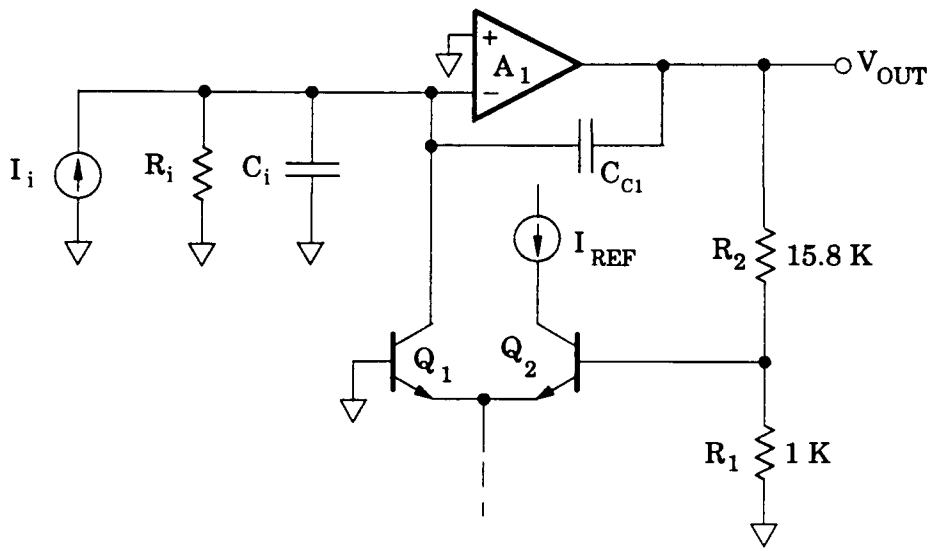


Figure 3.12. Simplified schematic of the compensated loop 1.

$$T_1(s) = -A_1(s)B(s) = -\left(\frac{R_i}{r_f}\right)\left[\frac{A_1(s)(1+sr_fC_{C1})}{1+sR_i(C_i+C_{C1})}\right]. \tag{3.17}$$

The model for the input opamp A_1 expressed in terms of frequency is

$$A_1(f) = \frac{A_o}{\left(1+\frac{jf}{f_{p1}}\right)\left(1+\frac{jf}{f_{p2}}\right)}, \tag{3.18}$$

where A_{o1} = 2.15 X 10^6 and f_{p1} and f_{p2} are located at 0.794 Hz and 11.44 MHz respectively. Other high-frequency poles of the input opamp occur at frequencies well beyond the 0-dB crossover frequency and contribute negligible phase shift. The complete expression for the loop transmission then becomes

$$T_1(s) = -A_1(s)B(s) = -\left(\frac{R_iA_o}{r_f}\right)\left\{\frac{(1+sr_fC_{C1})}{[1+sR_i(C_i+C_{C1})](1+s\tau_{p1})(1+s\tau_{p2})}\right\}. \tag{3.19}$$

This expression agrees with other analyses performed on similar circuits (Rochelle and Kennedy 1973). Thus, with the addition of C_{C1}, the loop transmission has three poles and one zero:

$$f_{p1} = \frac{1}{2\pi R_i(C_i+C_{C1})}, \tag{3.20}$$

$$f_{p2} = \frac{A_o}{GBW} = 0.794\text{Hz}, \tag{3.21}$$

$$f_{p3} = 11.44\text{MHz}, \tag{3.22}$$

$$f_{z1} = \frac{1}{2\pi r_fC_{C1}}. \tag{3.23}$$

The pole at f_{p1} results from the equivalent input impedance, R_i, and the sum of C_i and C_{C1}, the equivalent input capacitance, and the feedback capacitance. C_i is the total input

capacitance, which will be dominated by the detector capacitance. At dc, R_i is the parallel combination of r_{oQ1} and the input impedance of A_1, which is typically 10^{14} Ω. Leakage effects at the input node due to the circuit board can be neglected because of the use of a Teflon standoff. For these reasons, R_i can be approximated as r_o [see Equation (3.12)]. This approximation assumes that the input signal current source (or detector) has infinite output resistance. The poles f_{p2} and f_{p3} are fixed. The dominant high-frequency pole of A_1, f_{p3} is located at ~11 MHz. The zero at f_{z1} is a strong function of the input current because of its dependence on r_f and thus re_1. Thus, the addition of C_{C1} has added a zero and modified the position of one of the two dominant poles, f_{p1}.

The relationship of the pole/zero placement to the stability of this circuit can be best demonstrated by using the Bode plot shown in Figure 3.13. The extreme need for compensation occurs when r_f is at a minimum or when the input current is at a maximum. Under this condition, the zero is located nearest the crossover frequency and contributes the least phase shift than at any other bias condition. It is important for this zero f_{z1} to be placed properly before the loop transmission 0-dB crossover frequency in order to cause enough phase shift to offset the 180° shift resultant from f_{p1} and f_{p2}. The zero f_{z1} must also compensate for any phase shift resultant from f_{p3}, though it is only a small factor in the highest decades of input current. As the input current decreases, the added zero and modified pole move back in frequency at a rate proportional to the input current, increasing the distance between the zero location and the 0-dB crossover. This allows the zero to contribute a full 90° phase shift, resulting in a near 90° phase margin in the lower current decades, if one assumes that the high-frequency pole of A_1 contributes negligible phase shift.

The phase margin as a function of C_{C1} and input current was calculated by using MathCAD and is shown in Figure 3.14. This figure demonstrates the increasing need for

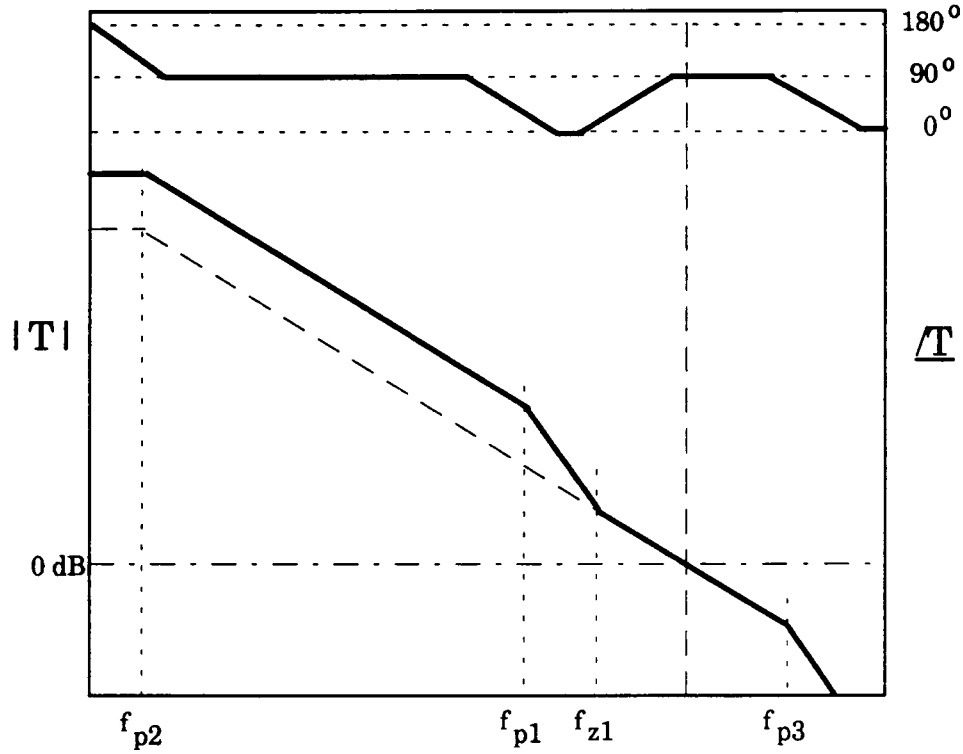


Figure 3.13. Bode plot of the compensated loop 1.

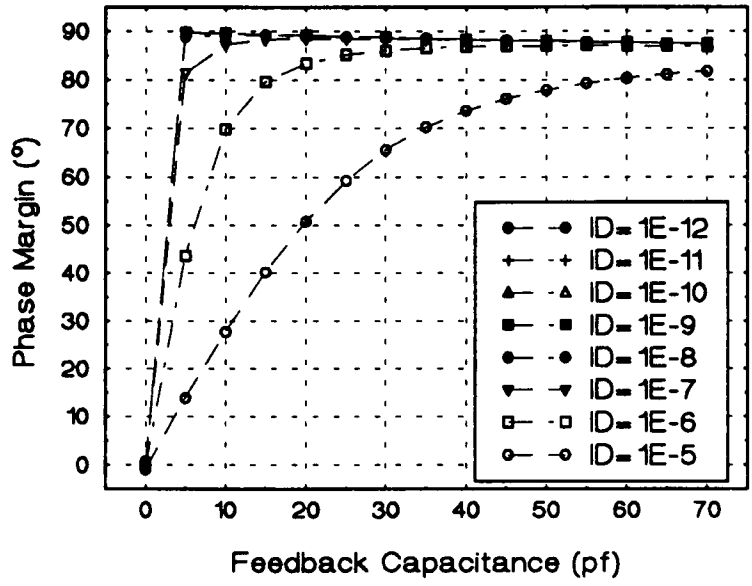


Figure 3.14. Loop 1 phase margin vs input current and feedback capacitance.

compensation at higher input currents and the required value of C_{C1} to achieve a desired phase margin. For a phase margin of 45°, 18 pF is needed in the highest current decade, and only 3 pF is required in the next lower current decade. A phase margin of 45° will ensure adequate stability and will provide a safety factor for variance in component values and temperature drifts.

Table 3.2 summarizes the calculated variable values for the components of Equation (3.19) and the corresponding resultant pole and zero locations using C_{C1} = 18 pF.

Table 3.2. Calculated values for the loop gain of the compensated circuit

ID	r_{e1}	r_f	R_i	$\|T\|$	$\|T\|$(dB)	f_{3dB_p1} (Hz)	f_{3dB_z1} (Hz)
1.00E-05	2600	43680	7999994	4.58E+08	173.2149	91.25864	202425.4
1.00E-06	26000	436800	79999360	4.58E+08	173.2149	9.12593	20242.54
1.00E-07	260000	4368000	8E+08	4.58E+08	173.2143	0.912659	2024.254
1.00E-08	2600000	43680000	7.99E+09	4.58E+08	173.208	0.091332	202.4254
1.00E-09	26000000	4.37E+08	7.94E+10	4.54E+08	173.1457	0.009199	20.24254
1.00E-10	2.6E+08	4.37E+09	7.41E+11	4.24E+08	172.5465	0.000986	2.024254
1.00E-11	2.6E+09	4.37E+10	4.44E+12	2.54E+08	168.1095	0.000164	0.202425
1.00E-12	2.6E+10	4.37E+11	8.89E+12	50875051	154.1301	8.21E-05	0.020243

In the higher current ranges, all parameters are well defined and predictable. The ratio of R_i to r_f is a fixed value resulting in a stable midband value of T. The pole f_{p1} and zero f_{z1} are each related to the input current and decrease in frequency proportionally with decreasing input current. As the input current decreases, the input resistance R_i is no longer totally dominated by r_{oQ1}, and the input resistance of A_1 becomes a factor in R_i. This can be observed in the slowing increase in R_i resulting in decreased $|T|$ as predicted by Equation (3.19). Additionally, the location of the f_{p1} pole becomes increasingly less proportional to the decrease in the input current because of its dependence on R_i. Correct prediction of the low-current circuit parameters is difficult because of incomplete models for the circuit in this regime of operation.

The loop transmission was plotted from Equation (3.19) by using MathCAD with a C_{C1} of 18 pF and an input current of 10 μA. The Bode plot is shown is Figure 3.15. The dc loop gain and pole locations agree well with the tabulated values in Table 3.2.

For comparison, the loop 1 transmission was also simulated by using PSPICE with the same circuit values used to generate the data of Table 3.2. Simplified models for the opamps were generated from the manufacturer's data and contain all pertinent frequency, gain, and input characteristics needed for proper loop analysis. These models are outlined in Appendix B. This analysis was performed by breaking the loop at the output of U_1 (a low impedance point) and adding an ac source and an offset voltage at the broken node. The offset voltage is added to simulate the closed-loop dc bias point and is a function of the input current. The proper value was determined by performing a dc operating point simulation on the closed-loop circuit at the desired input current levels. These values were then substituted for the offset voltage source in the simulation. The loop transmission and phase generated by using PSPICE are shown in Figure 3.16. The values of the midband gain and the pole and zero locations agree well with the computed values shown in Table 3.2. Figure 3.16 demonstrates the dependence of the poles and zeros of $T_1(s)$ on the input bias current. The curves shown are for input currents from 1 pA to 10 μA in one decade steps. The two poles of A_1 are fixed and are located at 0.8 Hz and 11.4 MHz. The remaining pole and zero result from the feedback factor $B(s)$ [see Equation (3.15)]. At the highest input bias level, the phase dips below zero degrees indicating a momentary instability. This phenomenon was not predicted in the MathCAD simulation (see Figure 3.16). The probable reason for this minor disagreement is the complete transistor models used in the PSPICE simulation that are not included in the MathCAD model. This dip in the phase should not cause a stability problem though a brief oscillation may occur as the circuit is turned on. As previously discussed, at the highest current decade a zero is placed just before the

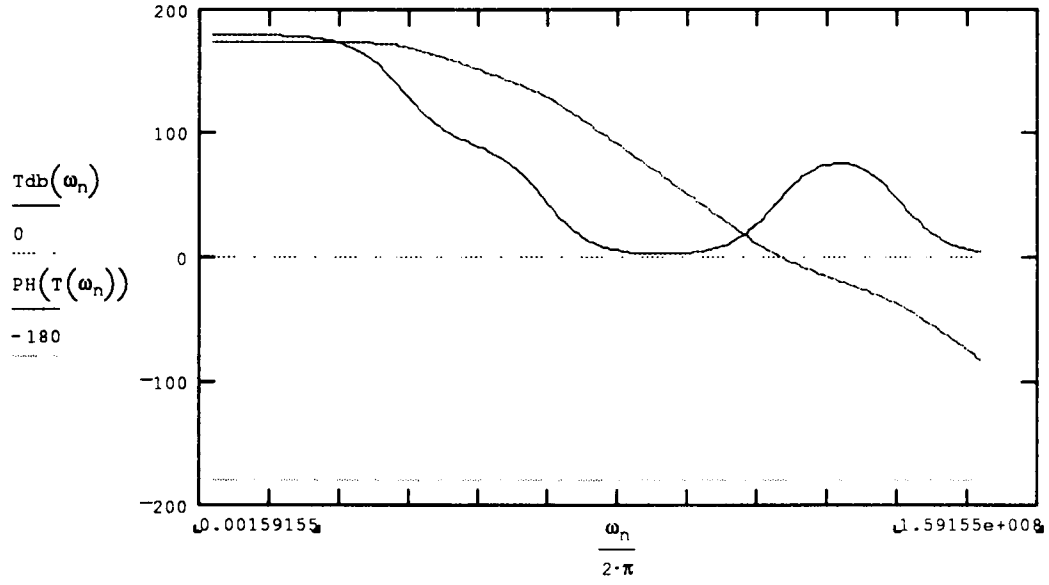


Figure 3.15. Loop 1 Bode plot generated from Equation (3.19) by using MathCAD.

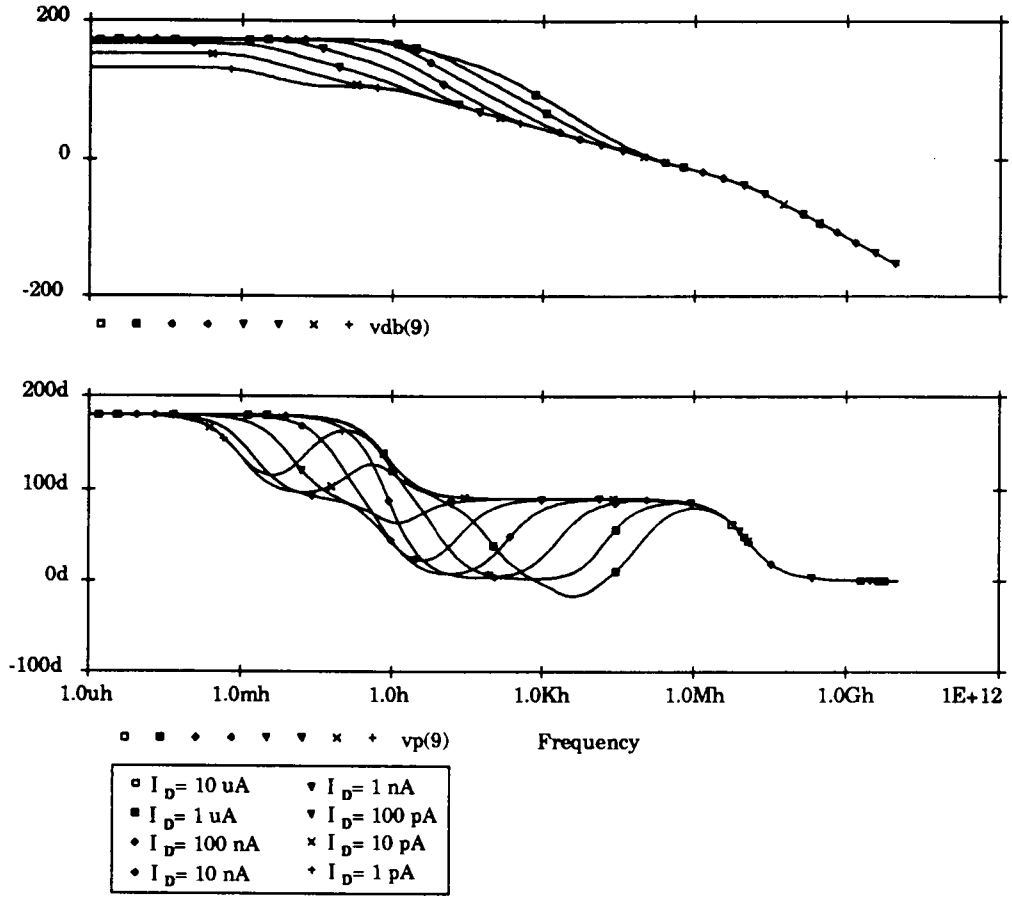


Figure 3.16. Loop 1 Bode plot generated by using PSPICE.

crossover frequency of $|T|$ to add enough phase shift for a nominal 45° phase margin. As the input current decreases, the pole and zero of *B(s)* are proportionally moved to lower frequencies. Because the crossover frequency remains nearly stable, the phase margin approaches 90° as the input current decreases. Thus, the system becomes more stable with decreasing input current, and the feedback capacitance value is selected to achieve a desired phase margin at the highest input current value.

Ideal compensation of this amplifier configuration would involve the use of a variable capacitance element that provides just the capacitance required for stability at each input current level. Use of this element would provide wider amplifier bandwidths at lower input current levels. Closed-loop issues of the amplifier will be discussed in following sections.

Loop 2 Stability Analysis

The simplified circuit of Figure 3.17 was used to identify the dc loop gain and primary pole/zero components of loop 2. This approach ignores the feedback path through the emitter of Q_1 around loop 1 back into the base of Q_2. First, the loop 2 characteristics will be analyzed without compensation. The loop is broken at the output of the U_2 opamp, and a signal is injected into R_4. Referring to Figure 3.18, several simplifications have been made to make the analysis more manageable. The node that connects the emitters of Q_1 and Q_2 has been grounded and the input impedance assumed to be ≈0. The two transistors are assumed to have ideal frequency characteristics. The xi_1 current source represents the percentage of the total current through R_4 (i_1) that enters Q_2. The x term represents this percentage and varies from 0.5 to 1 depending on the overall amplifier input current. In this configuration

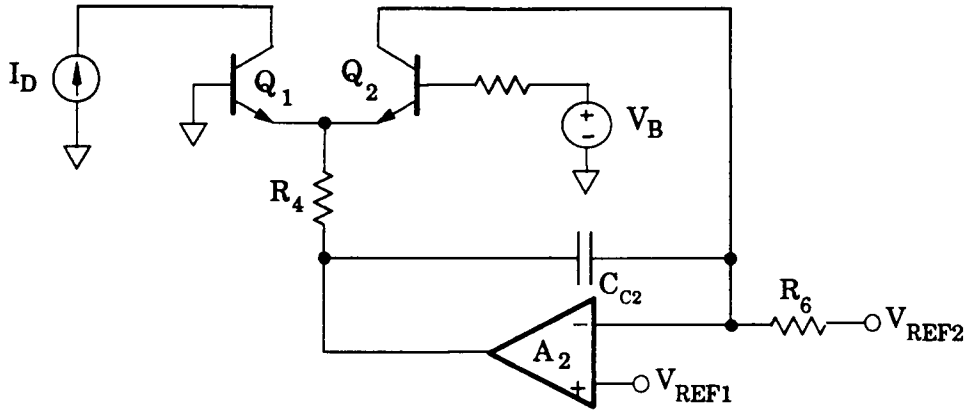


Figure 3.17. Simplified loop 2 circuit schematic.

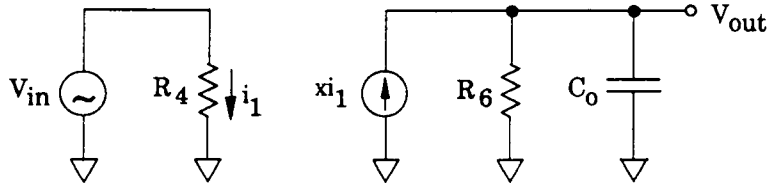


Figure 3.18. Uncompensated loop 2 simplified circuit for hand analysis.

$$V_o = xi_1\left(\frac{R_6}{1+sC_oR_6}\right), \tag{3.24}$$

where

$$xi_1 = \frac{V_{in}}{R_4} \tag{3.25}$$

and C_O is the parallel combination of the collector capacitance of Q_2 and the input capacitance of U_2 according to

$$C_o = C_{bcQ1} + C_{inU2}\ . \tag{3.26}$$

Substituting for i_1 in Equation (3.24) and multiplying the open-loop gain $A_2(s)$ of U_2, the loop 2 loop transmission can be defined as

$$T_2(s) = -\left(\frac{xR_6A_{ol2}}{R_4}\right)\left[\frac{1}{(1+sC_oR_6)(1+s\tau_1)(1+s\tau_2)}\right]. \tag{3.27}$$

This results in a three-pole system that will be at best marginally stable if the pole due to C_OR_6 and τ_2 are far enough out in frequency to contribute only a small phase shift. This is not likely because approximate values for C_O and R_6 result in a pole at ~ 88 kHz. The pole due to τ_1 represents the low-frequency pole of U_2 and will contribute 90° phase shift.

Compensation of this loop can be accomplished by adding a feedback capacitor to U_2, as shown in Figure 3.19. Summing the currents at the output node,

$$(V_o - V_{in})sC_{c2} + \frac{V_o}{R_6} + V_osC_4 = xi_1\ . \tag{3.28}$$

Substituting for i_1, the loop transmission can be expressed as

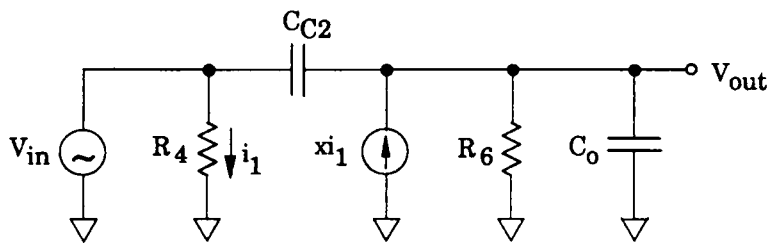


Figure 3.19. Compensated loop 2 simplified circuit for hand analysis.

$$T_2(s) = -\left(\frac{R_6}{R_4}\right)(xA_{ol})\left\{\frac{1+\left(\frac{sR_4C_{c2}}{x}\right)}{\left[1+sR_6(C_{c2}+C_o)\right](1+s\tau_1)(1+s\tau_2)}\right\}. \qquad (3.29)$$

The effect of adding C_{C2} has added a zero and modified the pole due to R_6 and C_O. Because $C_{C2} \gg C_O$, the added zero essentially cancels this pole. The difference in frequency between this pole/zero pair equals the ratio of xR_6 to R_4. Under most bias conditions, $I_{CQ2} \gg I_{CQ1}$, and x can be approximated as 1, resulting in a factor of 3 difference for the selected values of R_6 and R_4. A Bode plot of the loop transmission is shown in Figure 3.20. The zero approximately cancels the pole, but the difference in location brings the loop gain back down to near that of U_2, resulting in a stable system since the pole due to τ_2 (11 MHz) adds only a moderate phase shift. To test this simplified model and its handling of the transistor pairs, another simplified loop 2 circuit, shown in Figure 3.21, was simulated in PSPICE to compare with the analytical results presented above. In this circuit, both transistors are used and the U_1 loop has been removed. Results of this simulation are shown in Figure 3.22. Without a compensation capacitor, the phase margin is ~0°. A C_{C2} of 100 pF has nearly canceled the higher frequency dominant pole, resulting in a 60° phase margin. With C_{C2} equal to 100 nF, the dip in the phase has moved back three decades in frequency as the pole/zero pair has been shifted, also resulting in a PM of 60°. One can observe that a compensation capacitor just large enough to cause the zero to be added early enough in frequency to cancel the phase shift of the system dominant pole is all that is needed. Larger values will not produce any improvement in phase margin. A simulated dc gain of 143.076 dB agrees well with that of Equation (3.29). Therefore, one can conclude that the approximations used in the analytical model are adequate to the first order and can be used to compensate the current control loop.

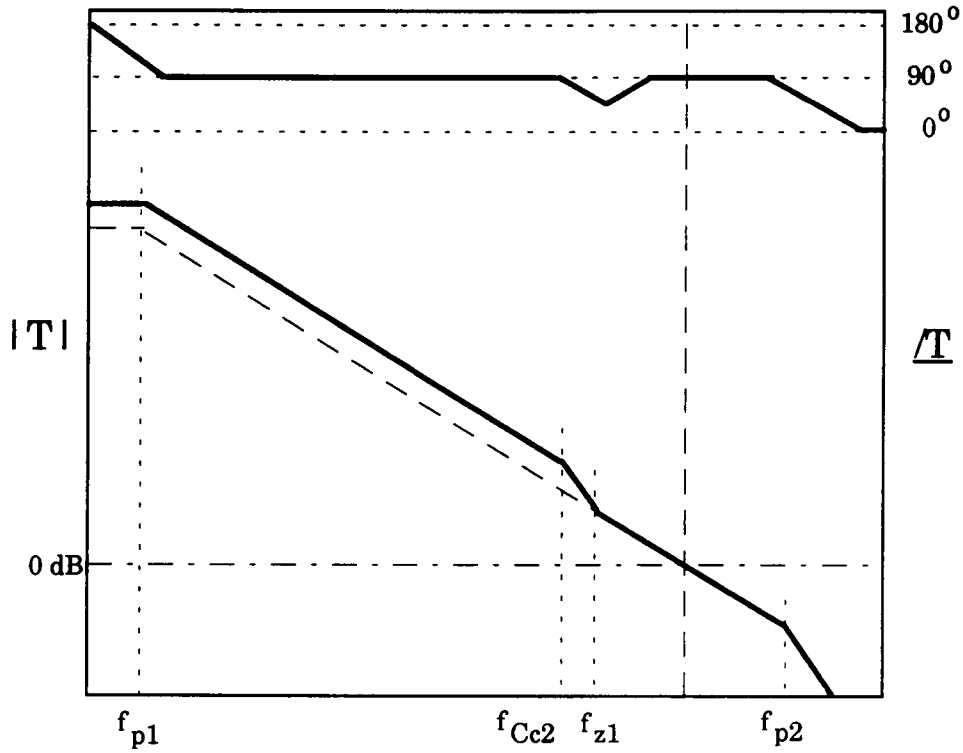


Figure 3.20. Bode plot for the simplified loop 2 circuit.

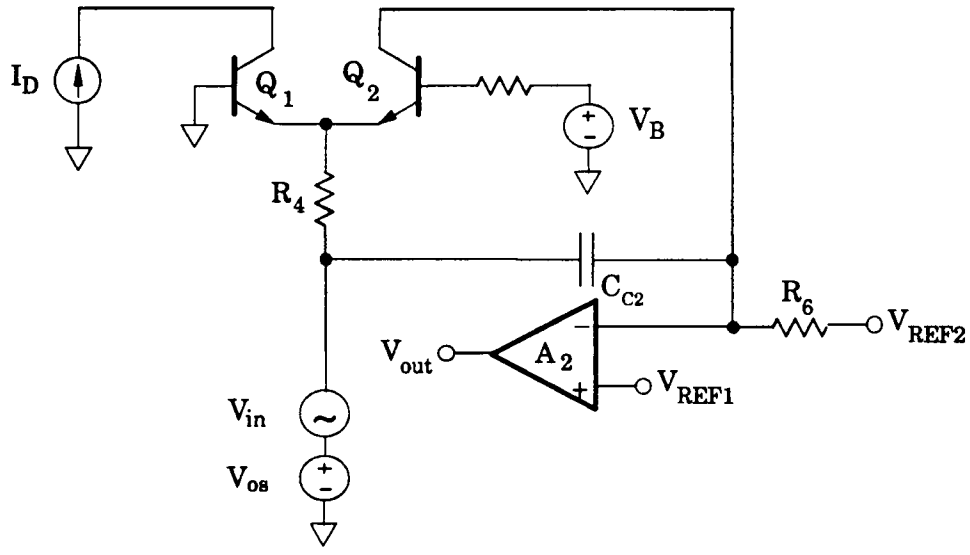


Figure 3.21. Simplified loop 2 circuit for PSPICE simulation.

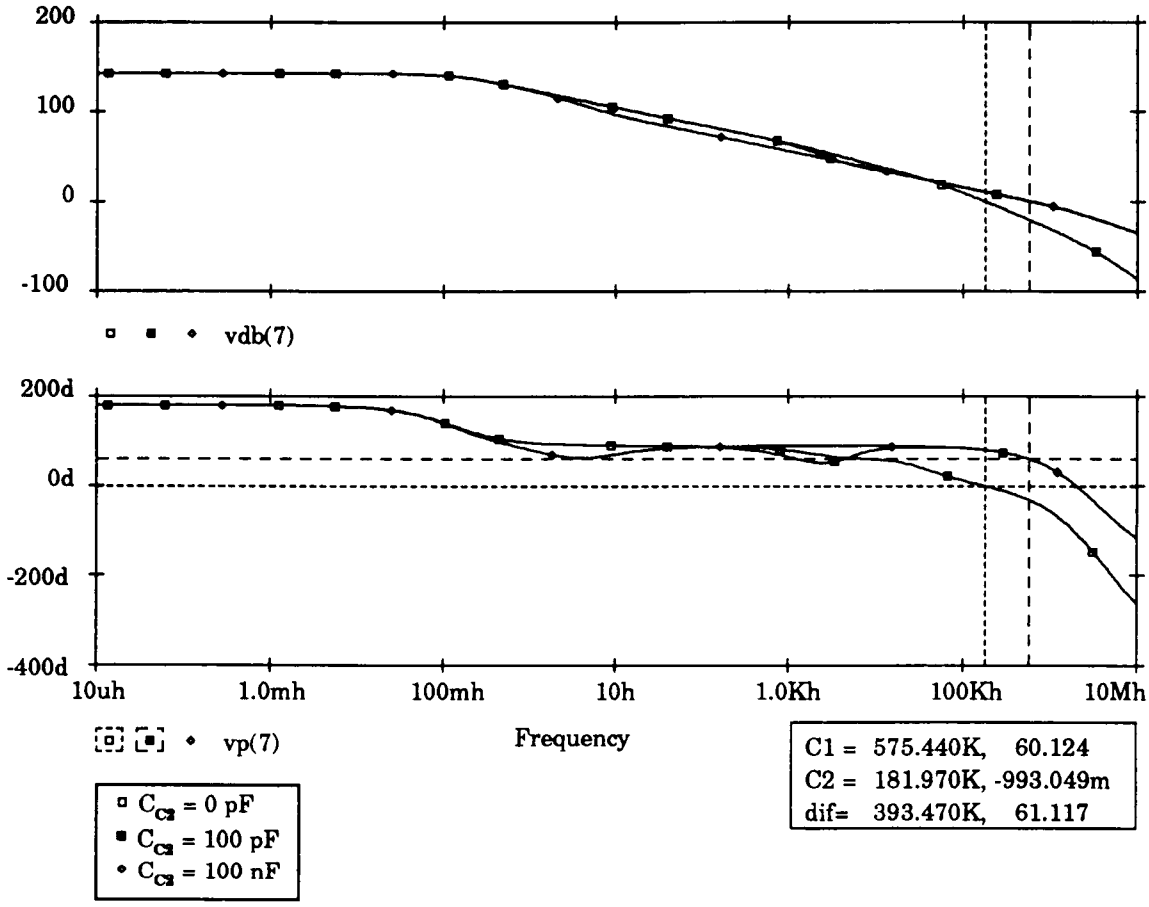


Figure 3.22. PSPICE Bode plot of the simplified loop 2 circuit.

Loop Interdependency Stability Analysis

An attempt was made to obtain a valid expression for the loop transmission of loop 1 incorporating the effects of loop 2. The procedure involved substituting hybrid pi models for Q_1 and Q_2, using all valid assumptions to reduce the circuit complexity, writing nodal equations, and solving for the loop transmission by using matrix algebra in MathCAD. However, this approach produced lengthy results that could not be readily interpreted. For this reason, PSPICE was used to perform a qualitative analysis to study the dependence of the loop 1 *PM* on C_{C2}. Figure 3.23 shows the loop 1 characteristics for C_{C2} values of 100 pF, 10 nF, and 1 μF. By observation one can see that C_{C2} does contribute to the pole/zero configuration. The most significant effect involves the cancellation of a pole that occurs third in frequency. At values of 10 nF and 1 μF, the zero cancels this pole, causing the system to appear to be dominated by two poles and a single zero. With smaller values of C_{C2} (C_{C2} = 100 pF), this pole occurs just before the zero and the phase dips as a result of the closely spaced pole/zero pair. However, for all of these cases, the loop 1 phase margin is unaffected by the value of C_{C2} and remains at 62°. This result validates the previous assumption that loop 1 is not appreciably dependent on the compensation of loop 2. This eliminates the possibility of overcompensating loop 2 to allow loop 1 to use a smaller compensation capacitor, thus increasing the bandwidth of the amplifier.

Additionally, a hand analysis of the loop 2 compensation was attempted to determine the effect of loop 1 compensation on loop 2. The same analysis procedure outlined for loop 1 was used with similar results. However, a dc loop gain was determined analytically that matched the result shown in Equation (3.29). As in the loop 1 analysis, further simulations were performed by using PSPICE to determine the qualitative relationship between the compensation of loop 2 and how it is affected by the compensation of loop 1. A group of

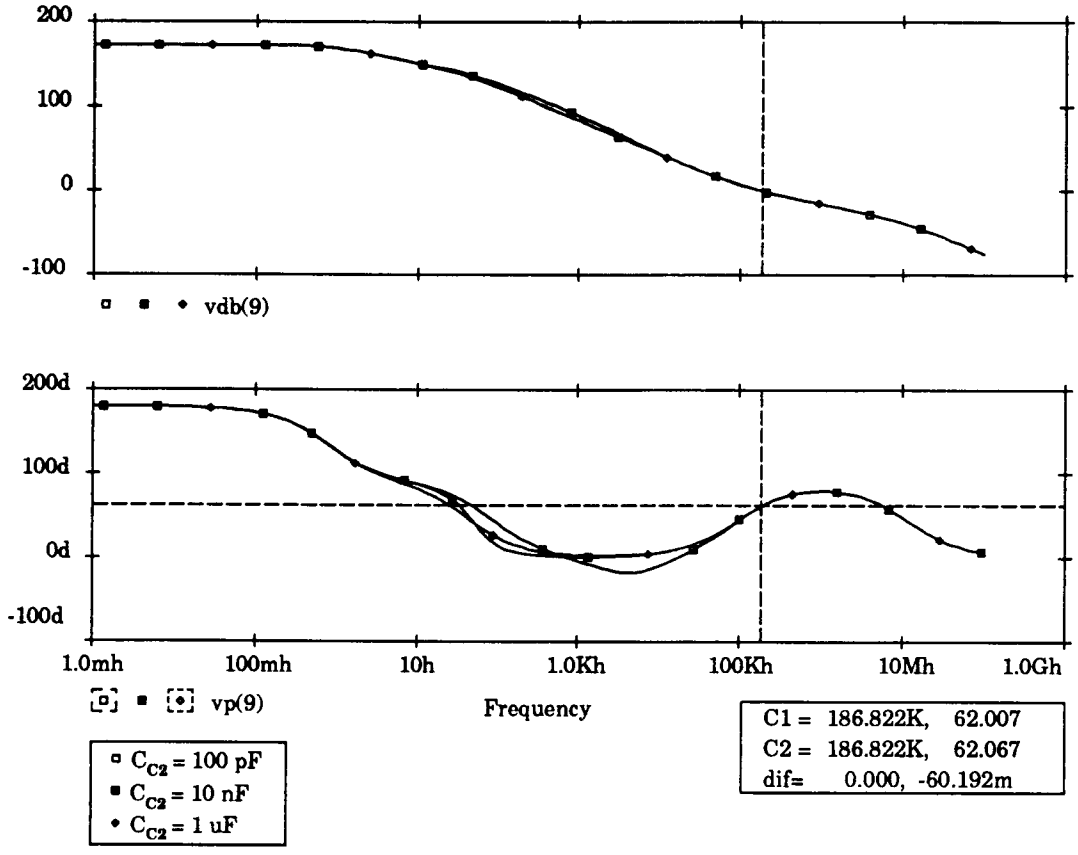


Figure 3.23. PSPICE Bode plot of the simplified loop 1 circuit vs C_{C2}.

simulations was performed on the basis of the circuit of Figure 3.24. Table 3.3 outlines the simulation name, compensation component values, and associated objective.

Table 3.3. Interactive compensation simulations for loop 2

Simulation name	Compensation component values	Simulation objective
1. tloop2a.cir	C_{C2} removed; C_{C1} = 18 pF, 1.8 nF, 180 nF, 18 μF	Determine whether loop 1 compensation can solely compensate for loop 2
2. tloop2b.cir	C_{C1} = 18 pF; C_{C2} = 1 fF, 100 pF, 10 nF, 1 μF	Determine relationship between C_{C2} and loop 2 compensation
3. tloop2d.cir	C_{C2} = 100 pF C_{C1} = 18 pF, 1.8 nF, 180 nF, 18 μF	With loop 2 compensated properly, determine whether C_{C1} affects loop 2 *PM*
4. tloop2e.cir	C_{C1} = 1 fF C_{C2} = 1 fF, 100 pF	Observe loop 2 *PM* compensated and uncompensated with loop 1 uncompensated

The results from simulation 1 are shown in Figure 3.25. In this simulation, loop 2 was left uncompensated, and C_{C1} was swept in two-decade steps to determine whether loop 1 had an appreciable effect on the *PM* of the uncompensated loop 2. One can see a pole zero pair that moves back in frequency proportional to the increase in value of C_{C1}. At C_{C1} = 18 pF, loop 2 is unstable, but all other values of C_{C1} used have moved the pole zero pair back and achieved an approximately 12° *PM*. Though some dependency exists, loop 2 cannot be properly compensated solely by using C_{C1}.

In simulation 2, the loop 2 *PM* was observed as a function of C_{C2}, with C_{C1} = 18 pF. This simulation produces an 84° *PM* for all values of $C_{C2} \geq$ 100 pF. These results are reasonably consistent with the previous analysis where loop 1 was omitted, validating previous assumptions (see Figure 3.26).

Simulation 3 is similar to simulation 1 except that loop 2 is properly compensated by using C_{C2}, and C_{C1} is swept to better determine the interdependence. Again, a closely

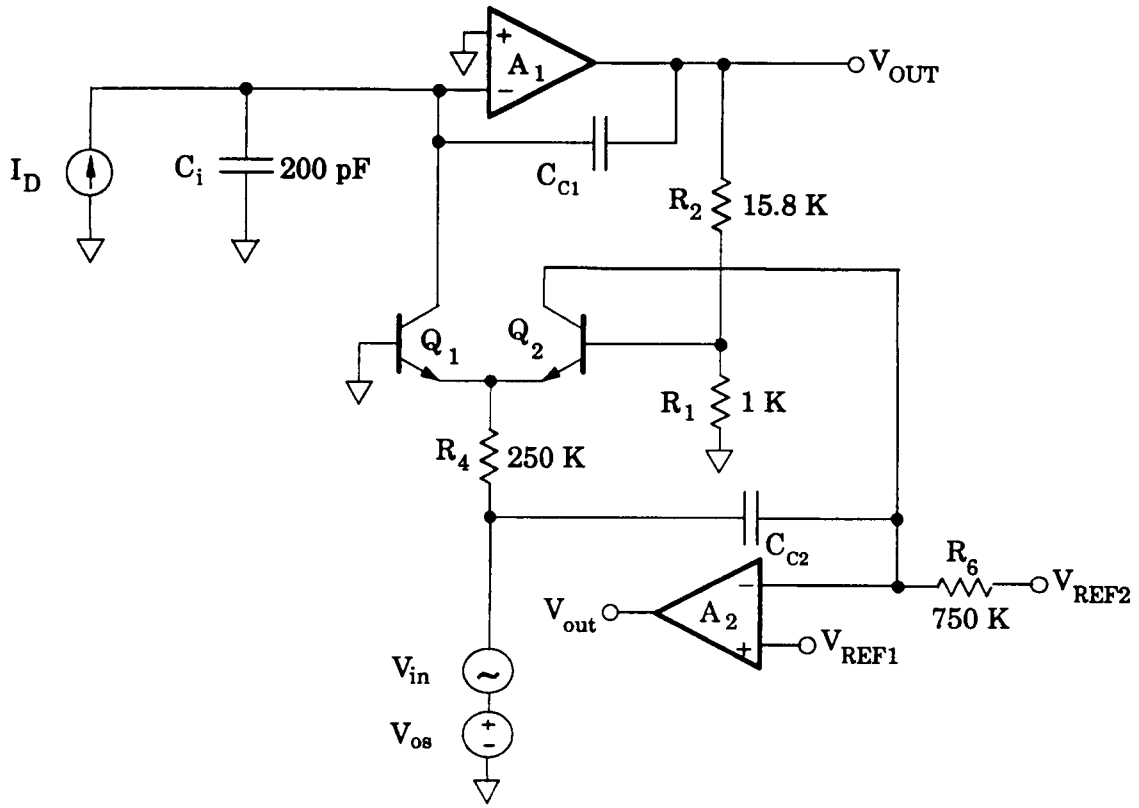


Figure 3.24. PSPICE circuit for determining loop 1 effect on loop 2.

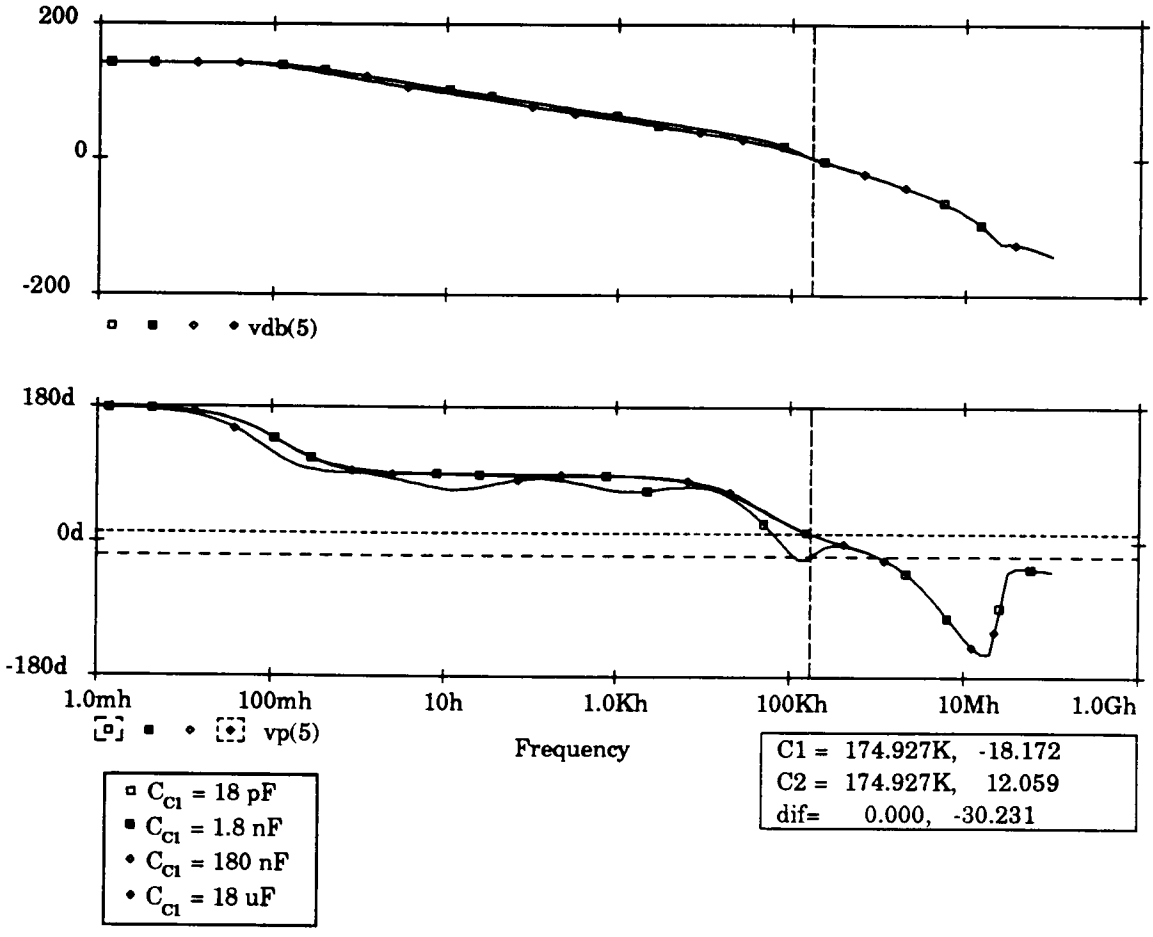


Figure 3.25. Loop 2 PSPICE simulation 1.

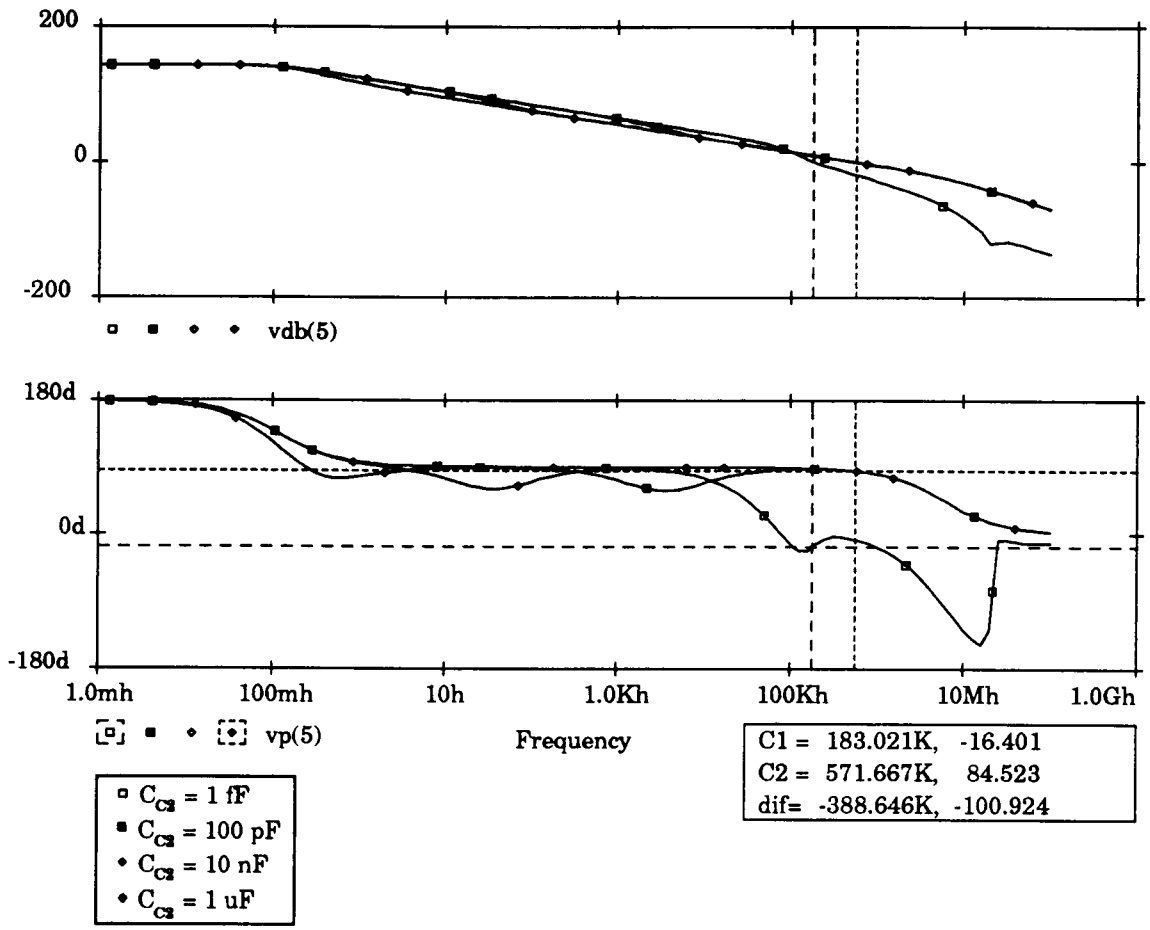


Figure 3.26. Loop 2 PSPICE simulation 2.

spaced pole/zero pair moves as the capacitance values are changed. However, in this case the position of the pair is apparently a function of the sum of C_{C1} and C_{C2}. With C_{C1} equal to 18 pF, the sum is 218 pF, and both appreciably contribute to the position of the pair. For other simulated values of C_{C1}, $C_{C1} \gg C_{C2}$, and the pair moves back at a rate proportional to the change in C_{C1}. In all cases, the *PM* is ~84° (refer to Figure 3.27). Again, C_{C1} seems to have no appreciable effect on the *PM* of loop 2.

Simulation 4 shows the loop 2 characteristics with both loops uncompensated and with only loop 2 compensated. The results demonstrate that with loop 2 properly compensated with a 100-pF capacitor, the *PM* is unaffected whether loop 1 is compensated or uncompensated (refer to Figure 3.28).

Summary

In summary, loop 2 can be properly compensated with the addition of feedback capacitor C_{C2}. Without C_{C2}, loop 2 can be marginally stabilized by using large values for C_{C1}. With C_{C2} properly compensated, C_{C1} has no appreciable effect on the stability of loop 2. Additionally, C_{C1} is a component of the dominant pole in the closed loop response and should therefore be kept as small as possible (see next section). For these reasons, compensation of either loop separately produces reasonable results and makes the analysis involved with each loop much simpler. However, improved performance of the overall amplifier by stabilizing loop 1 in part through the use of loop 2 compensation is not possible. This situation would be highly desirable because the loop 2 bandwidth can be decreased without degenerated performance of the entire amplifier.

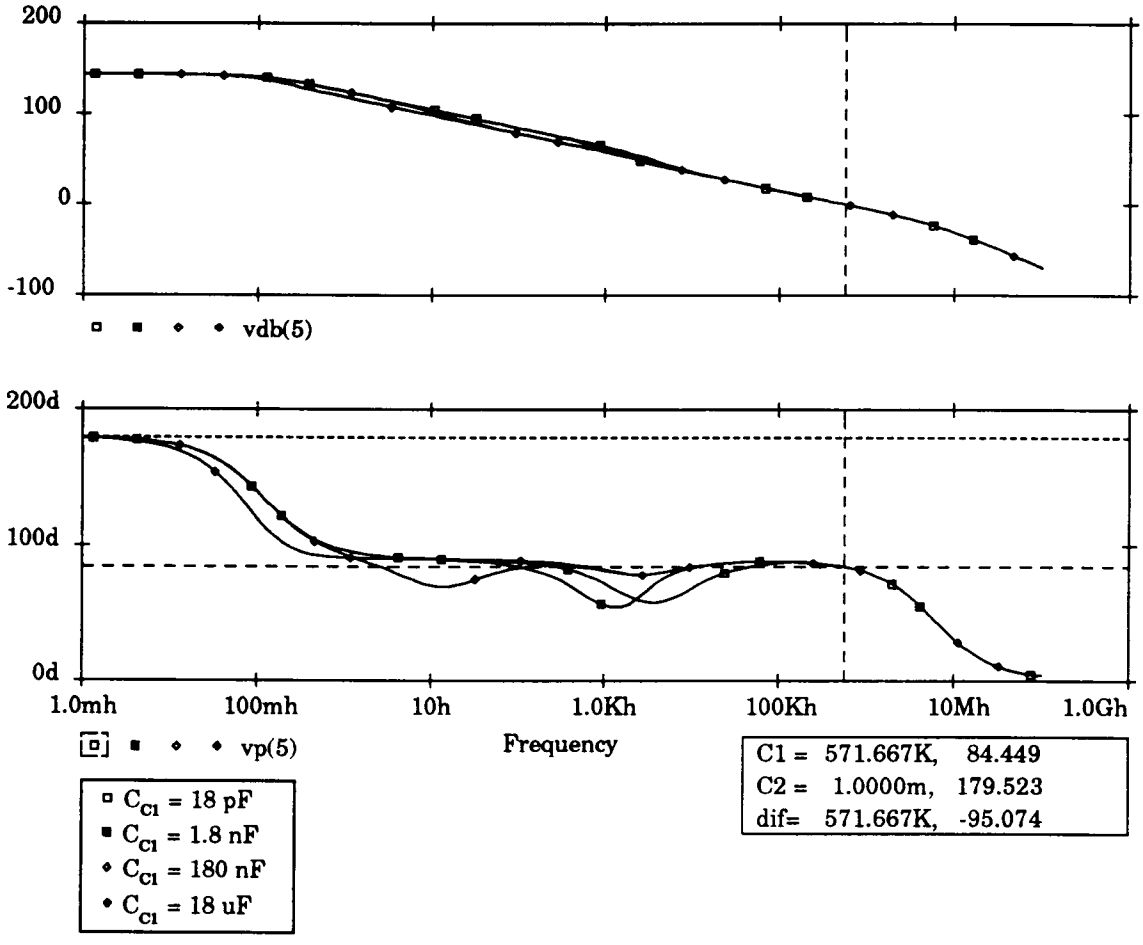


Figure 3.27. Loop 2 PSPICE simulation 3.

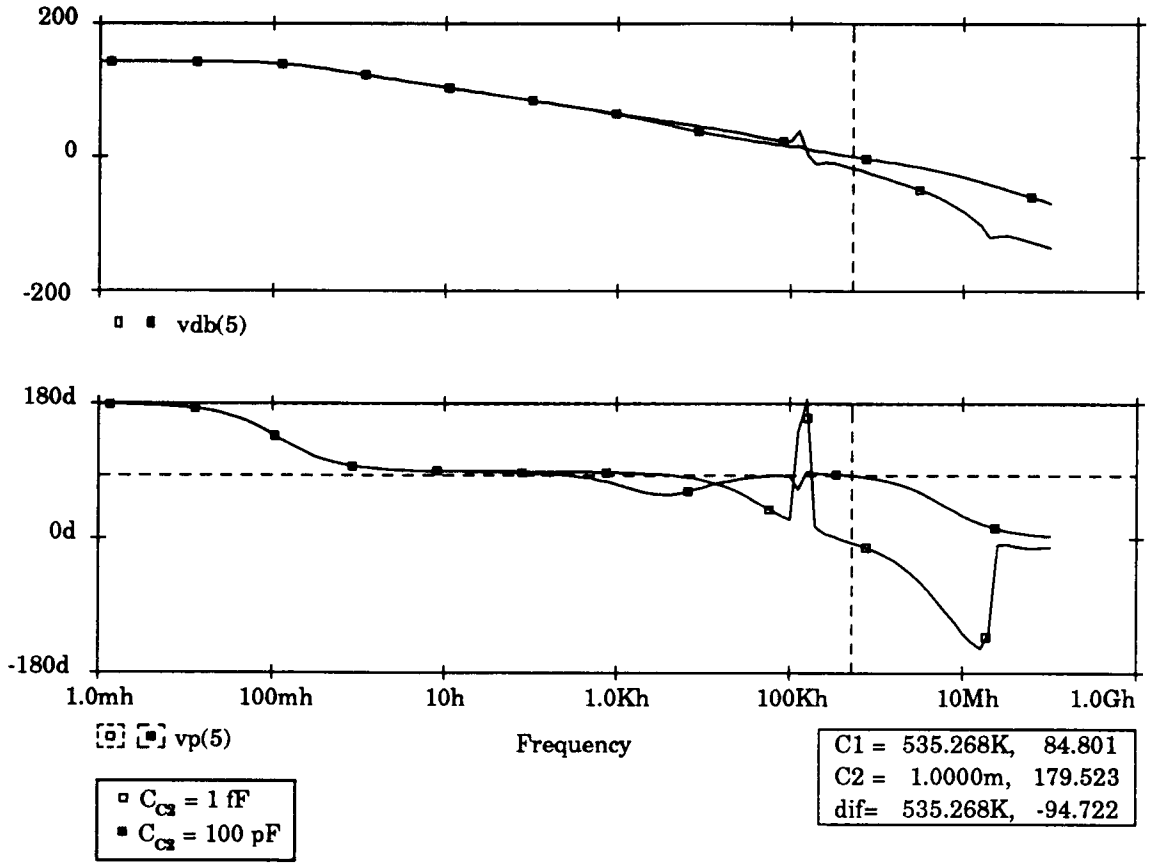


Figure 3.28. Loop 2 PSPICE simulation 4.

Closed-Loop Analysis

If an ideal reference current in Q_2 is assumed, the ideal expression for the closed-loop gain is

$$\left(\frac{V_{OUT}}{I_{IN}}\right)_{ideal} = \left(\frac{r_f}{1+sC_{C1}r_f}\right). \tag{3.30}$$

The exact expression for the closed-loop gain becomes

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{r_f}{1+sC_{C1}r_f}\right)\left[\frac{-T_1(s)}{1-T_1(s)}\right]. \tag{3.31}$$

Substituting for $T_1(s)$ by using Equation (3.19) will result in a four-pole system in the form

$$\frac{V_{OUT}}{I_{IN}} = A_{cl}\left[\frac{(1+s\tau_{z1})}{(1+s\tau_{p1})(1+s\tau_{p2})(1+s\tau_{p3})(1+s\tau_{p4})}\right]. \tag{3.32}$$

At low frequencies, the closed-loop gain will be dominated by the pole due to C_{C1} and r_f. At higher frequencies, the poles due to $T_1(s)$ will begin to contribute to the overall expression. The midband gain is r_f, which is a strong function of the input current (refer to Table 3.2 for calculated values).

The closed-loop response and phase were computed from Equation (3.31) by using MathCAD. Figure 3.29 demonstrates that the midband value of the closed loop gain is approximately r_f, and the dominant pole is placed as predicted. At higher input currents, some peaking of the gain is observed in both plots because of complex poles. Additionally, a complete circuit simulation of the closed-loop response was performed by using PSPICE (see Figure 3.30). The results from this simulation agree well with the analytically calculated result plotted by using MathCAD. In all cases the pole due to C_{C1} and r_f dominates the frequency response of the closed-loop expression. Because r_f is inversely proportional to the input current, the bandwidth of the amplifier is resultantly proportional to the input

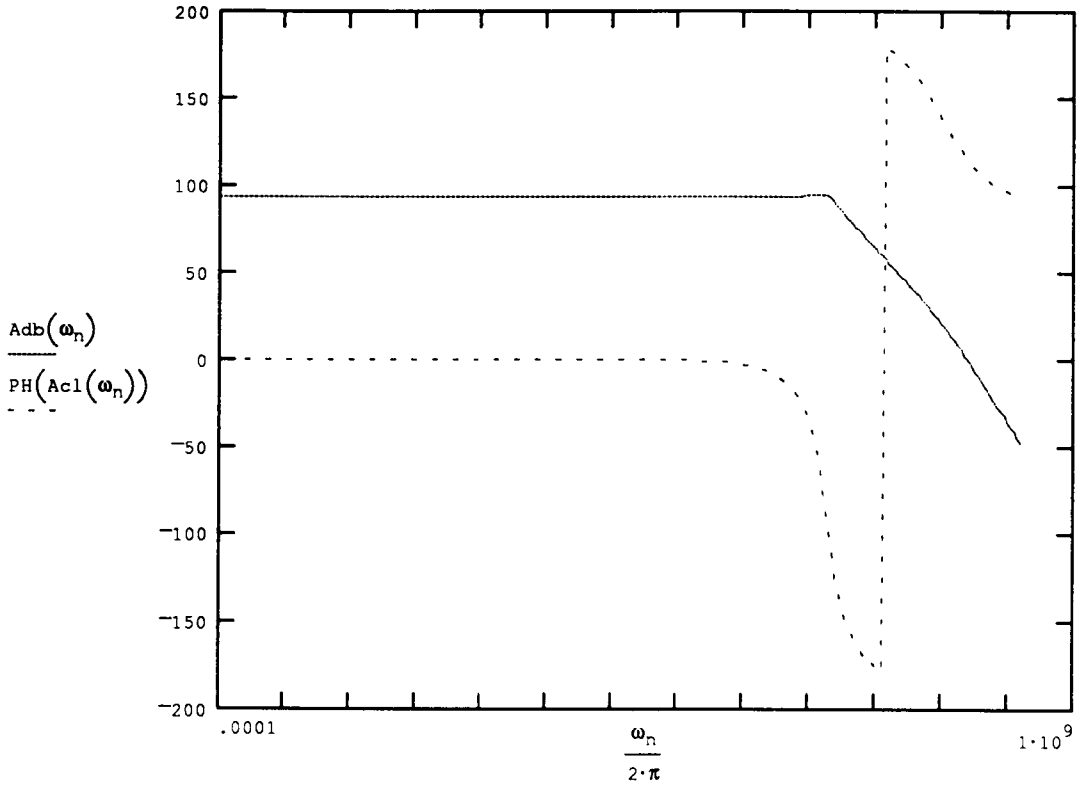


Figure 3.29. Closed-loop gain Bode plot generated by using MathCAD.

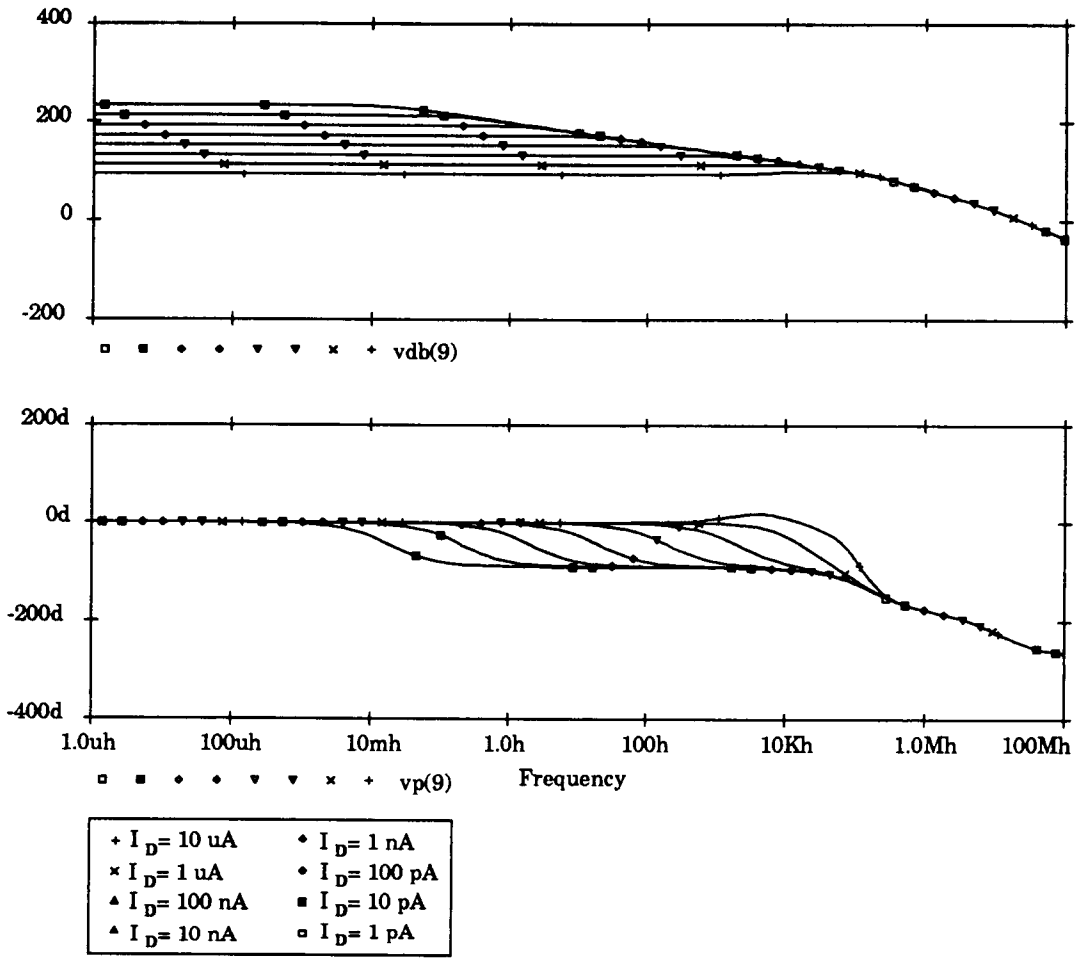


Figure 3.30. Closed-loop gain Bode plot generated by using PSPICE.

current. Precisely, the bandwidth decreases a factor of 10 for a decade decrease in the input current. For a seven-decade amplifier, this decrease will result in very slow measurements at small input current levels. For this reason, C_{C1} should be chosen just large enough to stabilize the circuit but as small as can be afforded to maintain as wide an overall amplifier bandwidth as possible.

Chapter 4

EXPERIMENTAL RESULTS

The circuits of Figures 3.1 and 3.9 were fabricated on a single printed circuit board (PCB) for experimental testing. Additional circuits were added to the test module for measuring the input offset voltages and currents of selected electrometer-grade opamps. As previously mentioned, a Teflon standoff was used at the input node to minimize PCB leakage effects. Additionally, ground plane was placed wherever possible, and the entire assembly was placed in an aluminum enclosure to minimize noise pickup. A photograph of the fabricated circuit in the shielded enclosure is shown in Figure 4.1.

The circuit was placed in an environmental chamber and instrumented as demonstrated in Figure 4.2. The input current to the electrometer was generated by using a Keithley 261 PicoAmpere Current Source. Leakage currents of the opamp devices were measured by using a Keithley Model 603 Electrometer. Low-noise coaxial cables were used for both the electrometer and current source signal paths to minimize noise transients due to cable movement and vibration.

A group of output voltages was measured at each temperature and input current condition. To facilitate fast and accurate switching between measurement voltages, a Keithley Model 705 Scanner was used to multiplex the output voltages into a single Hewlett Packard 3478A Digital Multimeter.

The circuits were tested with input current ranging from 1 pA to 10 μA over a temperature range of −18 to 71°C (0 to 160°F), in 10°F steps. At each of the temperature steps, the input current was swept through the seven decades at five steps per decade and signals of interest recorded at each step. Additionally, at each of the temperature steps the input offset voltage and current were recorded for several opamp devices under test. The signals recorded at each of the current steps are listed in Table 4.1.

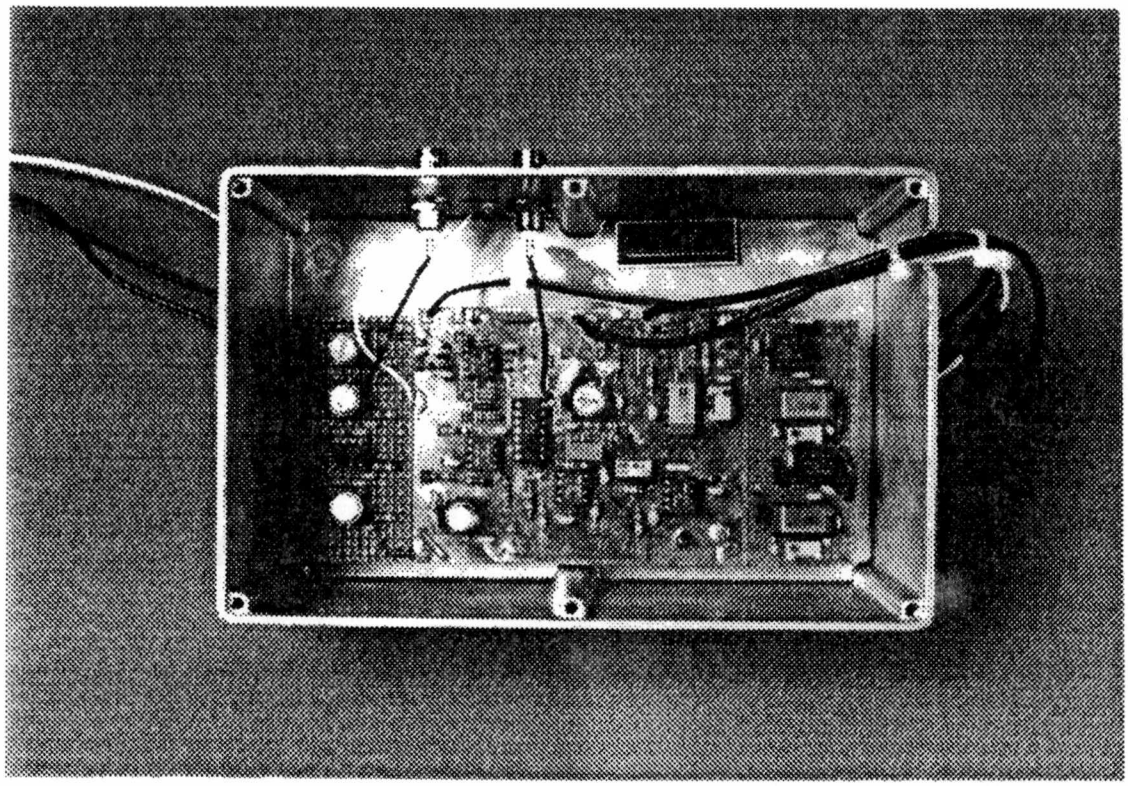


Figure 4.1. Photograph of the logarithmic amplifier test unit.

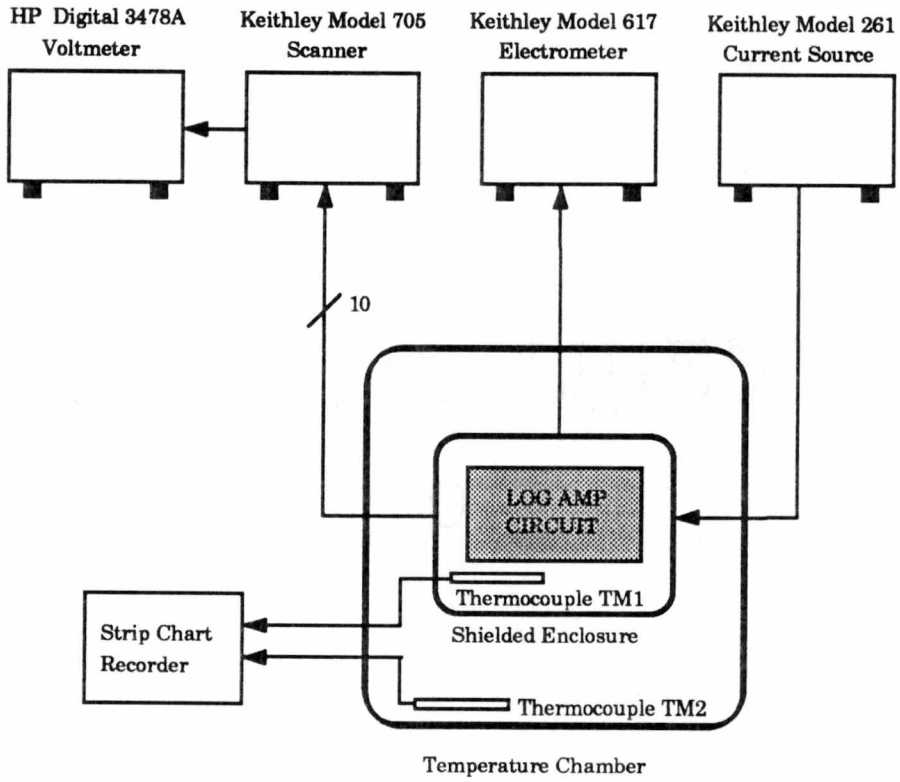


Figure 4.2. Experimental setup for logarithmic amplifier temperature testing.

Table 4.1. Recorded measurement data, input current dependent

Signal name	Description
Input current	Input signal current
Vout	Logarithmic amplifier output voltage
Vtout	Temperature tracking voltage source output voltage
D1out	Divider 1 output voltage
D2out	Divider 2 output voltage

Additionally, other signals that were not a function of the input current had to be measured only at each temperature increment, as shown in Table 4.2.

Table 4.2. Temperature-dependent signals measured

Signal Name	Description
VR2.5	AD584 voltage reference 2.5 V output
VR5.0	AD584 voltage reference 5.0 V output
VR10	AD584 voltage reference 10 V output
IBIAS_OPA128LM	OPA128LM input bias current
VOS_OPA128LM	OPA128LM input offset voltage
VOS_CA5420AE	CA5420AE input offset voltage
VOS_OP80EJ	OP80EJ input offset voltage
TM1	Temperature monitor 1, chamber control display
TM2	Temperature monitor 2, instrument enclosure thermocouple
TM3	Temperature Monitor 3, chamber thermocouple
HUM	Chamber control humidity setting

Two thermocouples were used to monitor the chamber temperature, both inside the instrument enclosure and in the interior of the chamber. These measurements were displayed on a strip-chart recorder and compared to the environmental chamber controls for verification. The temperature measured inside the enclosure was compared to the other temperature measurements to determine when the test circuit temperature had properly stabilized. This temperature measurement (TM3) is the reference for all reported data.

A large quantity of data was recorded and entered manually into a spreadsheet for manipulation. Several calibrations were performed and applied to the appropriate data sets. Test results associated with opamp device characterization were presented in Chapter 2. Test results summarizing the temperature performance of the overall circuit are shown in Figures 4.3 through 4.5.

Figure 4.3 shows the input-referred measurement errors for uncalibrated computer-ratioed data and for calibrated data ratioed by using computer division and analog dividers 1 and 2 respectively. Calibration factors were determined by using 21°C, 100-pA measurements. Divider network 1 shows significant offset error and increased error as the denominator approaches 0 V (at full-scale, 10 μA). Divider network 2 has much improved performance with <1% error for six decades. The computer-ratioed, calibrated data also exhibit <1% error for over six decades. The computer-ratioed data did exhibit the best overall accuracy, as expected, because errors due to the hardware division were eliminated.

The overall temperature performance of the logarithmic amplifier computed from uncalibrated data is illustrated in Figure 4.4. Accurate temperature performance (<1% error) is achieved in the upper five decades over the entire temperature range. The error in the lower two decades can be attributed to the device leakage currents of the input logarithmic transistor and opamp and their temperature dependence. However, the error is not attributed to the temperature-compensation technique. At temperatures near and below 21°C, <1% error can be achieved over six and a half decades of input signal amplitude.

For improved performance, thermoelectric cooling methods could be used to increase the low-current measurement accuracy. Regulation of the cooling temperature would not have to be tightly controlled but just maintained below a threshold level limiting input node device leakage currents. Figure 4.5 demonstrates the performance of the circuit at reduced temperatures. Calibration factors were calculated from −17.8°C, 100-pA data. Divider

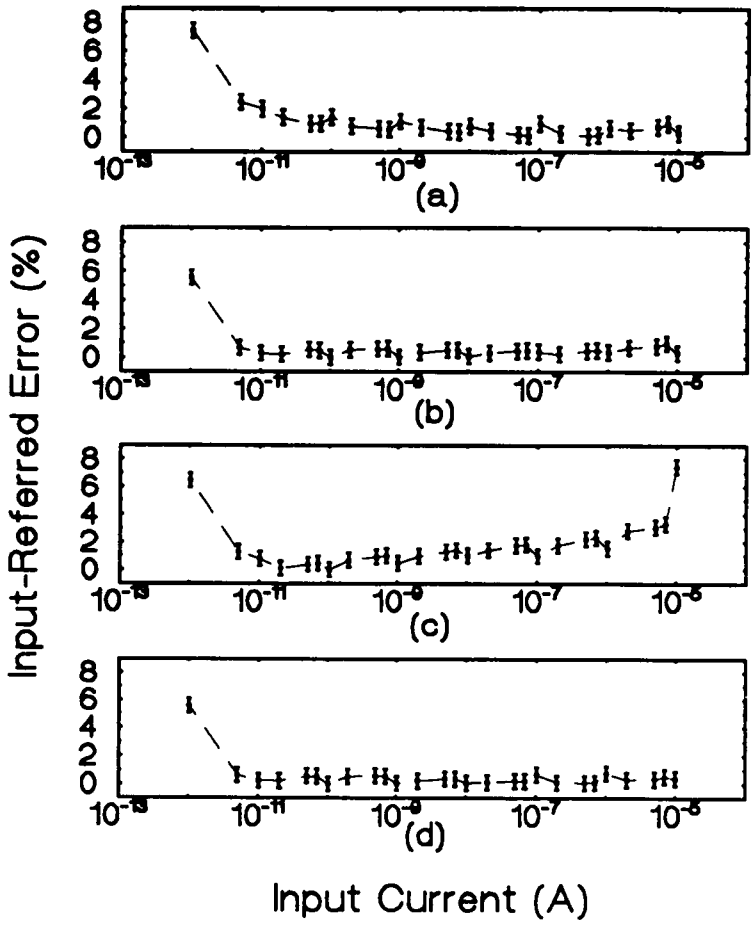


Figure 4.3. Input-referred measurement errors at 21°C: (a) uncalibrated computer-ratioed data, (b) calibrated computer-ratioed data, (c) calibrated divider 1 ratioed data, and (d) calibrated divider 2 ratioed data.

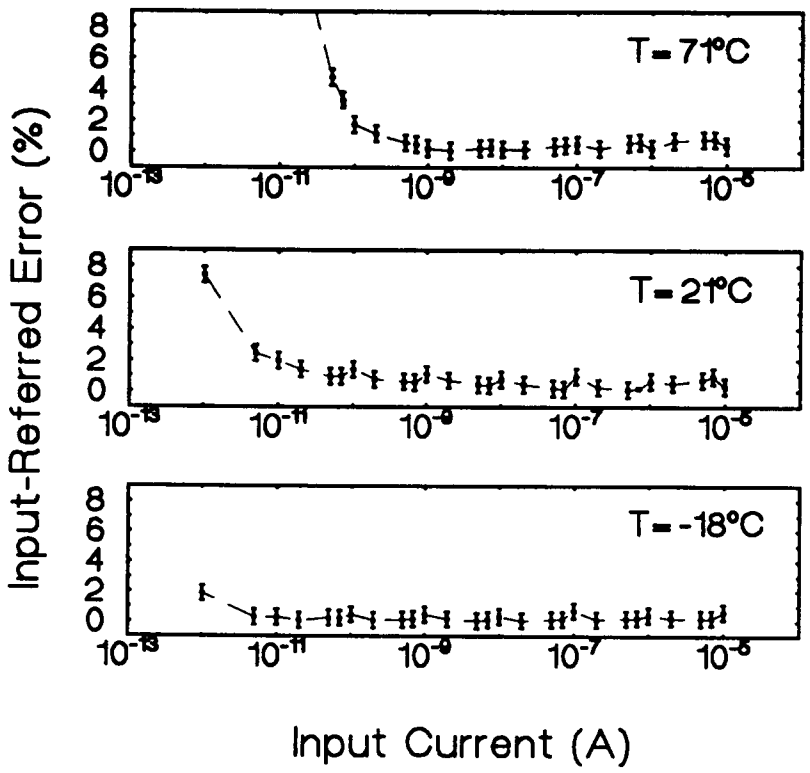


Figure 4.4. Full-range input-referred measurement error over temperature.

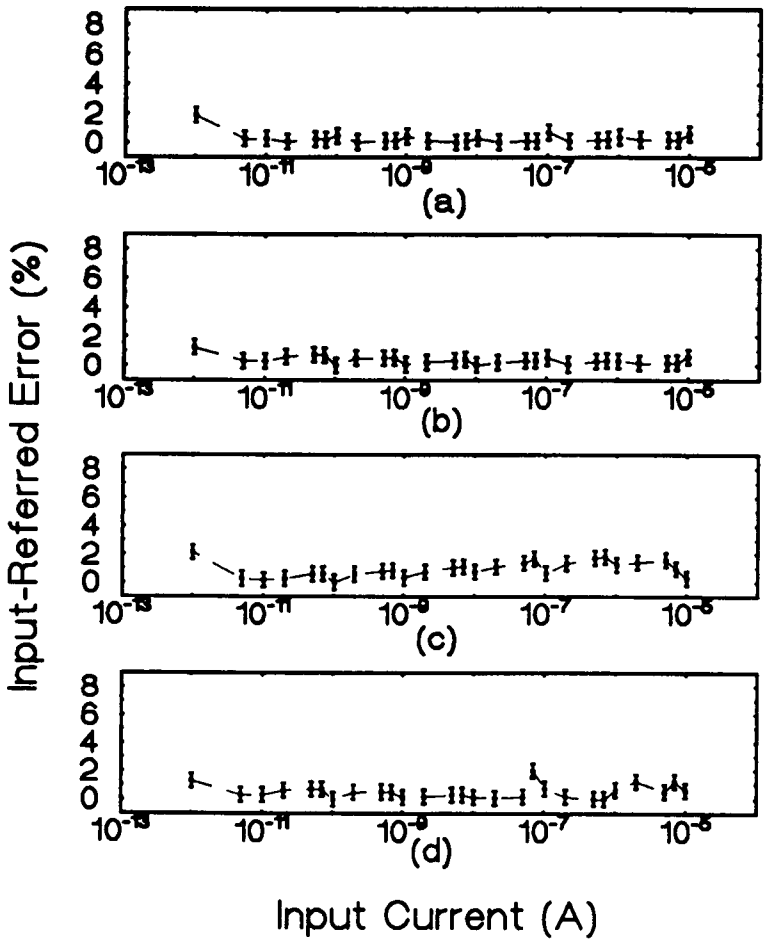


Figure 4.5. Input-referred measurement errors at −17.8°C: (a) uncalibrated computer-ratioed data, (b) calibrated computer-ratioed data, (c) calibrated divider 1 ratioed data, and (d) calibrated divider 2 ratioed data.

networks 1 and 2 demonstrate similar performance, with errors <2% over seven decades; and calibrated computer-ratioed data show <1.2% error over seven decades or <1% error over six and a half decades.

It should be noted that much of the measurement error not resultant from input leakage components at low input current signal levels can be attributed to errors in the reference current source used to perform the experiments. Several weeks were needed to perform the necessary temperature characterization of the circuit, because of both the time required for proper temperature stabilizing of the test assembly and the number of signals measured and recorded. During this measurement period, several verification measurements were performed on the current source by using a secondary standard electrometer. During this time, variations of up to ±0.5% were observed over the course of the measurements. To account for this uncertainty, error bars were used in Figures 4.3 through 4.5 to indicate measurement uncertainty primarily due to the current source inaccuracies.

Chapter 5

CONCLUSIONS

A seven-decade, high-accuracy, temperature-compensated logarithmic amplifier was developed and demonstrated. Limitations resulting from the use of conventional temperature-compensation methods were eliminated by the use of a quad, dielectrically isolated, well-matched, monolithic, bipolar transistor array. Errors resulting from variable forward current emission coefficients of the logarithmic elements are eliminated with this design. Additionally, single-point calibration is easily performed by either hardware trimming or software computation.

Extensive temperature testing of the circuit components and the overall amplifier was performed. Errors <1% have been demonstrated for five decades over an extended temperature range (–18 to 71°C) and for six and a half decades for temperatures below 21°C. Low-current measurement errors at high temperatures were found to result from input device leakage currents and were not due to the temperature-compensation method. Full seven-decade accuracy to within 1% is attainable by using thermoelectric or other suitable cooling methods to reduce input device leakage currents.

Stability of the amplifier was addressed by analyzing the two feedback loops comprising the amplifier both as separate units and as an integrated system. Conditions for stabilizing the overall amplifier were addressed, and the relationships with the input current signal level and circuit components were discussed.

Experimental results prove that the design is well suited for use in the intended application. All major design objectives of the development were achieved: wide dynamic range, good temperature performance, high accuracy over temperature, and monolithic compatibility. Suggestions for further work include performing a noise analysis of the circuit, implementing the design as a fully monolithic module by using a dielectrically

isolated process, and investigating thermoelectric cooling options. A thermoelectrically cooled monolithic logarithmic electrometer will provide an ideal solution for many miniaturized, multichannel, high-accuracy applications.

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APPENDIXES

Appendix A.

TEMPERATURE COEFFICIENT ELEMENTS AND ANALYSIS

Objective

The purpose of this appendix is to explain the methods used in generating the resistance, log scale factor error, and seventh decade input-referred errors as a function of temperature for the Q81 wirewound resistor and the Sensistor. The results of these analyses were presented in Figures 2.4 through 2.6.

Q81 Wirewound Resistor Calculations

From the manufacturer's data sheet, the Q81 is specified as 1000 Ω, with an average temperature coefficient (TC) of 3500 ± 300 ppm/°C referenced at 25°C and applicable for 0 to 125°C. On the basis of this information, resistance vs temperature curves were computed for the temperature range of −15°C to 75°C with temperature coefficients of 3200, 3500, and 3800 ppm/°C. Linear temperature coefficients represent the slope of the resistance vs temperature curve. The resistance curves for each TC were presented in Figure 2.4(a). To determine the associated log scale factor error e_k, the ideal temperature characteristic required for perfect compensation was computed by using a TC of 3600 ppm/°C, and the log scale factor was calculated for each of the Q81 resistance curves and for the ideal resistance element. The percent error in the log scale factor was then computed for each of the Q81 TC curves [demonstrated in Figure 2.5(a)]. The seventh decade input-referred error plots of Figure 2.6(a) were then calculated by using Equation (2.22) from the log slope errors for each of the TC curves.

Three programs were written to perform these calculations, one for each TC. The C source code for each of these programs is presented at the end of this appendix.

Unitrode Sensistor Calculations

The procedure used in generating the errors associated with the Sensistor was nearly identical to that described above for the Q81 device. The primary difference involved determining the various resistance vs temperature curves of Figure 2.4(b). The Sensistor procedure was more difficult because of a nonlinear TC for the device. Instead of calculating resistance linearly from a fixed TC and reference resistance value, the TC is nonlinear and requires more complicated methods to produce sensible results. A resistance vs temperature listing was provided by the manufacturer and is shown in Table A1.1.

Table A1.1. Sensistor device tolerance specifications

Temperature (°C)	Nominal value (Ω)	Value variation for ±5% tolerance (%)
−15	354.85	±9
0	393.86	±7
25	470.00	±5
50	554.20	±7
75	658.00	±9

Interpretation of this table led to the generation of five resistance vs temperature curves, as shown in Figure 2.4(b). The ideal case is the curve where the device value variation is 0%. This value will represent the average expected characteristic of this device. Other curves were generated to characterize the device by using the value variations provided. One would expect the general shape of the curve to remain somewhat constant, although slope and offset variations will occur. For this reason, four curves that maintained the second-order shape were generated and used for this analysis. Two curves used a +5% variation in the resistance value at the reference temperature (25°C) with the maximum tolerance applied to one of the end points of each curve. The other resistance values were then

calculated to maintain the general shape of the curve. Similarly, two curves were calculated for a –5% reference value variation. Initial curves had only five data points. To increase the resolution of the curves, points were entered into a plotting package, a curve fit performed, and additional data points generated by using the fitted equation.

Once resistance curves were properly determined, the same procedures described for the Q81 device were used to calculate the associated log scale factor and seventh-decade input-referred errors. The program used to generate the error curves is provided at the end of this appendix.

```
/* Q81 WIREWOUND RESISTOR TC CALCULATIONS - QTCL.C */
/* RESISTANCE, LOG SCALE FACTOR ERROR,              */
/* AND 7TH DECADE ERROR FOR TC = 3200 - L           */

#include <stdio.h>
#include <math.h>
#include <float.h>

main()

{
        FILE *in,*out1,*out2,*out3, *fopen();

        int T,TK,TC;
        double KIT,KAT,eK,error_7;
        double RIT,RAT;
        static double lnten = 2.30258;
        static double koverq = 8.625e-5;
        double R2 = 15728;
        TC = 3200;

        /* Open output files */

        out1 = fopen("qrl.dat", "w");
        out2 = fopen("qkl.dat", "w");
        out3 = fopen("qel.dat", "w");

        /* Calculate all parameters using 1 degree steps */
        /* Note:  Value is 1K at 25 C */

        for (T = -25; T < 76; T++)
        {
                /* Calculate ideal and actual R values at T */

                TK = 273 + T;
                RIT = 1000 + ((T - 25) * 3.36);
                RAT = 1000 + ((T - 25) * (TC / 1000.0));

                /* Calculate ideal and actual K values at T */

                KIT = (koverq) * TK * lnten * (1+ (R2 / RIT));
                KAT = (koverq) * TK * lnten * (1 + (R2 / RAT));

                /* Calculate K (log scale factor) error -> ek */

                eK = (KAT - KIT)/KIT*100;

                /* Calculate error in 7th decade -> error_7 */

                error_7 = ((exp(lnten*(-7.0)*(eK/100)))-1) * 100;
```

```
            /* print calculation results to output files */

            fprintf(out1," %d %6.4lf \n",T,RAT);
            fprintf(out2," %d %6.4lf \n",T,eK);
            fprintf(out3," %d %6.4lf \n",T,error_7);
        }
            /* close output files */

            fclose (out1);
            fclose (out2);
            fclose (out3);

}
```

```
/* Q81 WIREWOUND RESISTOR TC CALCULATIONS - QTCM.C */
/* RESISTANCE, LOG SCALE FACTOR % ERROR,          */
/* AND 7TH DECADE ERROR FOR TC = 3500 - M         */

#include <stdio.h>
#include <math.h>
#include <float.h>

main()

{
        FILE *in,*out1,*out2,*out3, *fopen();

        int T,TK,TC;
        double KIT,KAT,eK,error_7;
        double RIT,RAT;
        static double lnten = 2.30258;
        static double koverq = 8.625e-5;
        double R2 = 15728;
        TC = 3500;

        /* Open output files */

        out1 = fopen("qrm.dat", "w");
        out2 = fopen("qkm.dat", "w");
        out3 = fopen("qem.dat", "w");

        /* Calculate all parameters using 1 degree steps */
        /* Note:  Value is 1K at 25 C */

        for (T = -25; T < 76; T++)
        {
                /* Calculate ideal and actual R values at T */

                TK = 273 + T;
                RIT = 1000 + ((T - 25) * 3.36);
                RAT = 1000 + ((T - 25) * (TC / 1000.0));

                /* Calculate ideal and actual K values at T */

                KIT = (koverq) * TK * lnten * (1+ (R2 / RIT));
                KAT = (koverq) * TK * lnten * (1 + (R2 / RAT));

                /* Calculate K (log scale factor) error -> ek */

                eK = (KAT - KIT)/KIT*100;

                /* Calculate error in 7th decade -> error_7 */

                error_7 = ((exp(lnten*(-7.0)*(eK/100)))-1) * 100;
```

```
            /* print calculation results to output files */

            fprintf(out1," %d %6.4lf \n",T,RAT);
            fprintf(out2," %d %6.4lf \n",T,eK);
            fprintf(out3," %d %6.4lf \n",T,error_7);
        }
            /* close output files */

            fclose (out1);
            fclose (out2);
            fclose (out3);

}
```

```
/* Q81 WIREWOUND RESISTOR TC CALCULATIONS - QTCH.C */
/* RESISTANCE, LOG SCALE FACTOR % ERROR,        */
/* AND 7TH DECADE ERROR FOR TC = 3800 - H       */

#include <stdio.h>
#include <math.h>
#include <float.h>

main()

{
        FILE *in,*out1,*out2,*out3, *fopen();

        int T,TK,TC;
        double KIT,KAT,eK,error_7;
        double RIT,RAT;
        static double lnten = 2.30258;
        static double koverq = 8.625e-5;
        double R2 = 15728;
        TC = 3800;

        /* Open output files */

        out1 = fopen("qrh.dat", "w");
        out2 = fopen("qkh.dat", "w");
        out3 = fopen("qeh.dat", "w");

        /* Calculate all parameters using 1 degree steps */
        /* Note:  Value is 1K at 25 C */

        for (T = -25; T < 76; T++)
        {
                /* Calculate ideal and actual R values at T */

                TK = 273 + T;
                RIT = 1000 + ((T - 25) * 3.36);
                RAT = 1000 + ((T - 25) * (TC / 1000.0));

                /* Calculate ideal and actual K values at T */

                KIT = (koverq) * TK * lnten * (1+ (R2 / RIT));
                KAT = (koverq) * TK * lnten * (1 + (R2 / RAT));

                /* Calculate K (log scale factor) error -> ek */

                eK = (KAT - KIT)/KIT*100;

                /* Calculate error in 7th decade -> error_7 */

                error_7 = ((exp(lnten*(-7.0)*(eK/100)))-1) * 100;
```

```
            /* print calculation results to output files */

            fprintf(out1," %d %6.4lf \n",T,RAT);
            fprintf(out2," %d %6.4lf \n",T,eK);
            fprintf(out3," %d %6.4lf \n",T,error_7);
        }
            /* close output files */

            fclose (out1);
            fclose (out2);
            fclose (out3);

}
```

```
/* UNITRODE TC CALCULATIONS - SEN.C                    */
/* CALCULATION OF LOG SCALE FACTOR ERROR AND ASSOCIATED */
/* INPUT-REFERRED ERROR FOR 5 RESISTANCE CURVES.       */

#include <stdio.h>
#include <math.h>
#include <float.h>

main()
{
        FILE *in1,*in2,*in3,*in4,*in5;
        FILE *out1,*out2,*out3,*out4,*out5;
        FILE *out6,*out7,*out8,*out9,*out10,*fopen();

        double eK,error_7;
        double KN,KT;
        double R2 = 16450.0;
        double T[20];
        double R[20];

        int n;

        static double lnten = 2.30258;
        static double koverq = 8.625e-5;
        static double R1nom = 470.0;

        /* Open input and output files */

        in1 = fopen("SENAS.DAT","r");
        in2 = fopen("SENBS.DAT","r");
        in3 = fopen("SENCS.DAT","r");
        in4 = fopen("SENDS.DAT","r");
        in5 = fopen("SENES.DAT","r");
        out1 = fopen("SKA.LST", "w");
        out2 = fopen("SKB.LST", "w");
        out3 = fopen("SKC.LST", "w");
        out4 = fopen("SKD.LST", "w");
        out5 = fopen("SKE.LST", "w");
        out6 = fopen("SEA.LST", "w");
        out7 = fopen("SEB.LST", "w");
        out8 = fopen("SEC.LST", "w");
        out9 = fopen("SED.LST", "w");
        out10 = fopen("SEE.LST", "w");

        /* Read T[n] and R[n] from data file - set 1 */

        printf("\n Loading data file...\n\n");

        for (n=0; n < 19; n++)
        {
                fscanf(in1,"%lf", &T[n]);
```

```
        fscanf(in1,"%lf", &R[n]);
        R[n] = R[n] - 23.5;
        printf(" %6.2lf  %6.2lf\n", T[n],R[n]);
}

/* Calculate LSF and associated error and store in output file */

KN = koverq * 298 * lnten * (1 + (R2 / (R1nom+517.0)));

for (n=0; n < 19; n++)
{
        KT = koverq * (T[n] +273) * lnten * (1 +(R2 / (R[n]+517.0)));
        eK = (( KT - KN ) / KN) * 100;
        error_7 = ((exp(lnten * (-7.0) * eK * .01)) - 1) * 100;
        fprintf(out1," %6.2lf %6.2lf\n",T[n],eK);
        fprintf(out6," %6.2lf %6.2lf\n",T[n],error_7);
}

/* Read T[n] and R[n] from data file - set 2 */

printf("\n Loading data file...\n\n");

for (n=0; n < 19; n++)
{
        fscanf(in2,"%lf", &T[n]);
        fscanf(in2,"%lf", &R[n]);
        R[n] = R[n] - 23.5;
        printf(" %6.2lf  %6.2lf\n", T[n],R[n]);
}

/* Calculate LSF and associated error and store in output file */

KN = koverq * 298 * lnten * (1 + (R2 / (R1nom+517.0)));

for (n=0; n < 19; n++)
{
        KT = koverq * (T[n] +273) * lnten * (1 +(R2 / (R[n]+517.0)));
        eK = (( KT - KN ) / KN) * 100;
        error_7 = ((exp(lnten * (-7.0) * eK * .01)) - 1) * 100;
        fprintf(out2," %6.2lf %6.2lf\n",T[n],eK);
        fprintf(out7," %6.2lf %6.2lf\n",T[n],error_7);
}

/* Read T[n] and R[n] from data file - set 3 */

printf("\n Loading data file...\n\n");

for (n=0; n < 19; n++)
{
        fscanf(in3,"%lf", &T[n]);
        fscanf(in3,"%lf", &R[n]);
```

```
        printf(" %6.2lf  %6.2lf\n", T[n],R[n]);
}

/* Calculate LSF and associated error and store in output file */

KN = koverq * 298 * lnten * (1 + (R2 / (R1nom+517.0)));

for (n=0; n < 19; n++)
{
        KT = koverq * (T[n] +273) * lnten * (1 +(R2 / (R[n]+517.0)));
        eK = (( KT - KN ) / KN) * 100;
        error_7 = ((exp(lnten * (-7.0) * eK * .01)) - 1) * 100;
        fprintf(out3," %6.2lf %6.2lf\n",T[n],eK);
        fprintf(out8," %6.2lf %6.2lf\n",T[n],error_7);
}

/* Read T[n] and R[n] from data file - set 4 */

printf("\n Loading data file...\n\n");

for (n=0; n < 19; n++)
{
        fscanf(in4,"%lf", &T[n]);
        fscanf(in4,"%lf", &R[n]);
        R[n] = R[n] + 23.5;
        printf(" %6.2lf  %6.2lf\n", T[n],R[n]);
}

/* Calculate LSF and associated error and store in output file */

KN = koverq * 298 * lnten * (1 + (R2 / (R1nom+517.0)));

for (n=0; n < 19; n++)
{
        KT = koverq * (T[n] +273) * lnten * (1 +(R2 / (R[n]+517.0)));
        eK = (( KT - KN ) / KN) * 100;
        error_7 = ((exp(lnten * (-7.0) * eK * .01)) - 1) * 100;
        fprintf(out4," %6.2lf %6.2lf\n",T[n],eK);
        fprintf(out9," %6.2lf %6.2lf\n",T[n],error_7);
}

/* Read T[n] and R[n] from data file - set 5 */

printf("\n Loading data file...\n\n");

for (n=0; n < 19; n++)
{
        fscanf(in5,"%lf", &T[n]);
        fscanf(in5,"%lf", &R[n]);
        R[n] = R[n] + 23.5;
        printf(" %6.2lf  %6.2lf\n", T[n],R[n]);
```

```
        }

        /* Calculate LSF and associated error and store in output file */

        KN = koverq * 298 * lnten * (1 + (R2 / (R1nom+517.0)));

        for (n=0; n < 19; n++)
        {
                KT = koverq * (T[n] +273) * lnten * (1 +(R2 / (R[n]+517.0)));
                eK = (( KT - KN ) / KN) * 100;
                error_7 = ((exp(lnten * (-7.0) * eK * .01)) - 1) * 100;
                fprintf(out5," %6.2lf %6.2lf\n",T[n],eK);
                fprintf(out10," %6.2lf %6.2lf\n",T[n],error_7);
        }

        /* Close output files */

        fclose (out1);
        fclose (out2);
        fclose (out3);
        fclose (out4);
        fclose (out5);
        fclose (out6);
        fclose (out7);
        fclose (out8);
        fclose (out9);
        fclose (out10);
}
```

Appendix B.

PSPICE OPAMP MODELS

Two opamps were selected for use in the logarithmic amplifier circuit: the Burr-Brown OPA128LM and the PMI OP77EZ. Although the manufacturers' macro models were available for these parts, convergence was more easily achieved by using simplified circuit models. The primary need for PSPICE in the development of this circuit was to determine dc operating points and to verify the open-loop and closed-loop characteristics of the overall circuit. For this reason, a simplified model that properly represented the opamp input characteristics, dominant poles, and open-loop gain was all that was required.

The simplified models for both opamps were implemented as demonstrated in Figure B1.1. The input resistance and capacitance are represented by using simple devices. The low- and high-frequency dominant poles are modeled as two rc networks, R1-C1 and

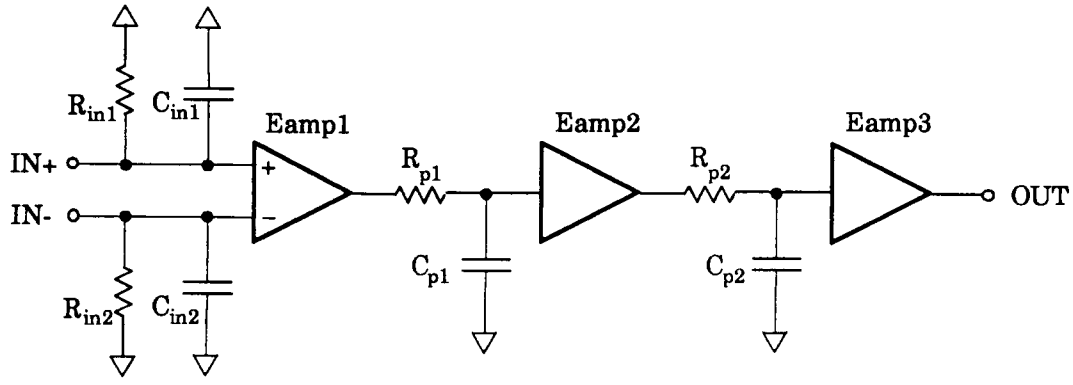


Figure B1.1. Simplified opamp model.

R2-C2 respectively. Amplifiers EAMP1, EAMP2, and EAMP3 provide isolation between the input, pole circuits, and output. Additionally, EA2 implements the open-loop gain of the opamp. The PSPICE subcircuits for the two opamps are listed at the end of this section. PSPICE simulations of the two models are shown in Figures B1.2 and B1.3.

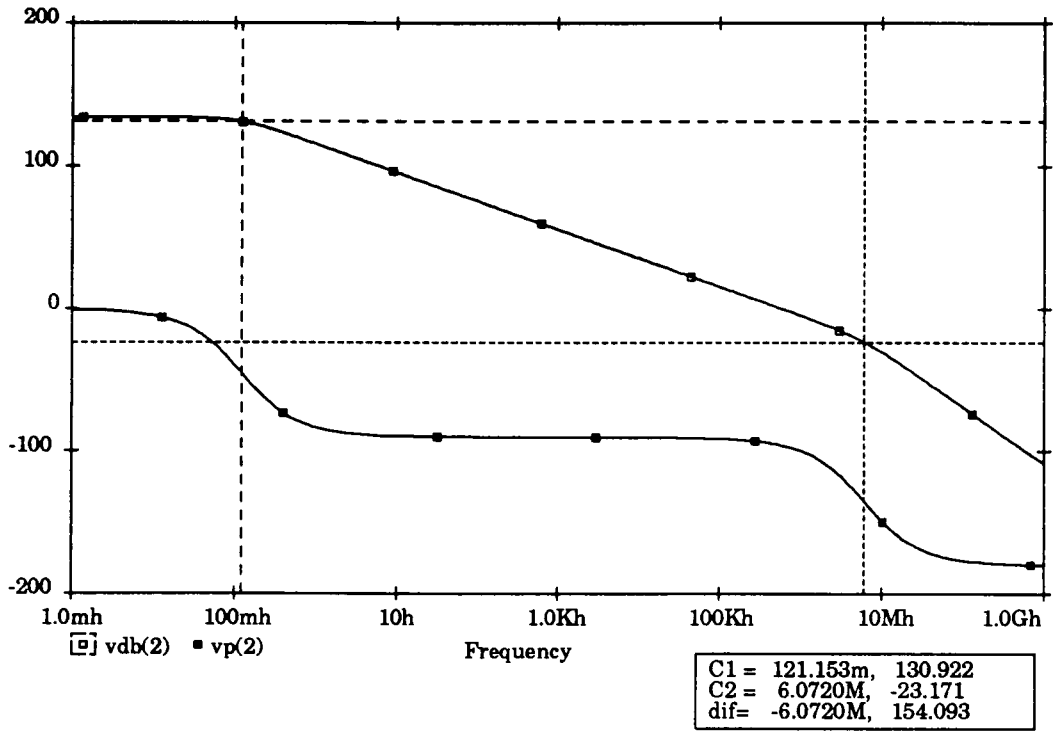


Figure B1.2. PSPICE simulation of the simplified OP77EZ model.

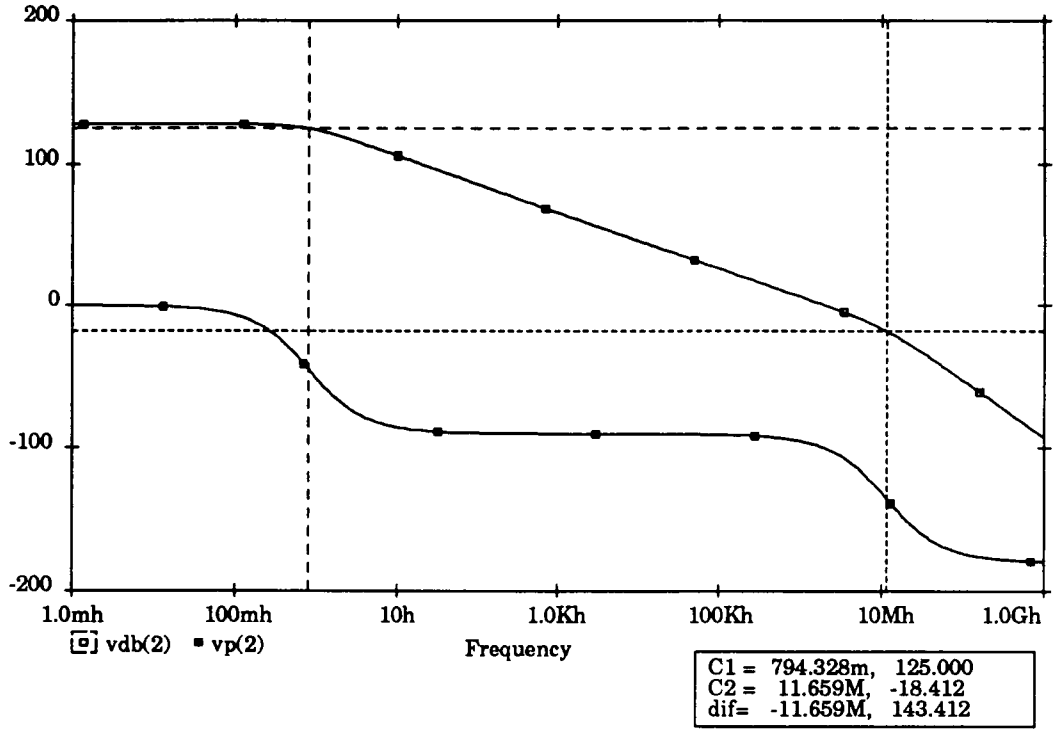


Figure B1.3. PSPICE simulation of the simplified OPA128LM model.

****** OPA128 Simplified Model ******

```
Vin  1 0 AC 1
X2   1 0 2 OPA128

RL 2 0 1E9

*** OP128LM subcircuit - simplified model ***

.SUBCKT OPA128 1 2 5
CIN1          1 0 2PF
CIN2          2 0 2PF
RIN1          1 0 1E14
RIN2          2 0 1E14
EAMP1         3 0 1 2 1
RP1           3 4 39.98K
CP1           4 0 5UF
EAMP2         6 0 4 0 2.512E6
RP2           6 7 139.1
CP2           7 0 100PF
EAMP3         5 0 7 0 1
.ENDS OPA128

.OP
.PROBE
.AC DEC 20 1e-3 1e9
.END
```

****** OP77 Simplified Model ******

```
Vin 1 0 AC 1
X2  1 0 2 OP77

RL 2 0 1E9

*** OP77 subcircuit - simplified model ***
.SUBCKT OP77 1 2 5
CIN1            1 0 2PF
CIN2            2 0 2PF
RIN1            1 0 2E11
RIN2            2 0 2E11
EAMP1           3 0 1 2 1
RP1             3 4 132.6K
CP1             4 0 10UF
EAMP2           6 0 4 0 5E6
RP2             6 7 265.26
CP2             7 0 100PF
EAMP3           5 0 7 0 1
.ENDS OP77

.OP
.PROBE
.AC DEC 20 1e-3 1e9
.END
```

Appendix C.

MISCELLANEOUS DERIVATIONS

Objective

The purpose of this appendix is to show the origin of expressions not explicitly derived in the thesis. Derivations that will be demonstrated include the feedback factor r_f, the input-referred error resultant from base current in Q_{1B}, and the input-referred error due to log slope factor error.

Derivation of Feedback Factor r_f

The feedback factor can be expressed as

$$r_f = \frac{V_{OUT}}{I_{IN}} = \frac{V_{OUT}}{I_{CQ1A}} . \tag{C1.1}$$

Using the approximation given in Equation (2.17), the relationship between V_{BE} and I_C for a BJT is given by

$$I_C \approx I_{SS}\left(e^{\frac{qV_{BE}}{NFkT}}\right). \tag{C1.2}$$

This expression can be solved for V_{BE} as

$$V_{BE} = \left(\frac{kT}{q}\right)\ln\left(\frac{I_C}{I_{SS}}\right). \tag{C1.3}$$

The output voltage V_{OUT} can be expressed in terms of the two base emitter voltages and R_1 and R_2 as

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{kT}{q}\right)\left(V_{BEQ1B} - V_{BEQ1A}\right). \tag{C1.4}$$

Substituting Equation (C1.3), the output voltage can be expressed as

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{kT}{q}\right)\left(\ln\left[I_{CQ1B}\right] - \ln\left[I_{CQ1A}\right]\right). \tag{C1.5}$$

The equivalent resistance of the feedback network can be determined by taking the derivative of Equation (C1.5) with respect to I_{CQ1A}, the input current:

$$r_f = \frac{d(V_{OUT})}{d(I_{CQ1A})} = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{kT}{q}\right)\left\{\frac{d\left(\ln\left[I_{CQ1B}\right] - \ln\left[I_{CQ1A}\right]\right)}{d(I_{CQ1})}\right\}. \tag{C1.6}$$

Note that I_{CQ1B} is a fixed reference current and is not a function of the input current. Therefore,

$$r_f = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{kT}{q}\right)\left(-\frac{1}{I_{CQ1A}}\right) = -\left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{1}{g_{mQ1A}}\right). \tag{C1.7}$$

However, r_e can be approximated as the inversion of g_m yielding

$$r_f \approx -\left(\frac{R_1 + R_2}{R_1}\right)\left(r_{eQ1A}\right). \tag{C1.8}$$

The negative sign is a result of the current direction assumed. Note that this approximation is valid only for dc and ignores the error resultant from the base current of Q_{1B}. This error term will be discussed in detail in the following section of this appendix.

Derivation of the error due to Q_{1B} Base Current

As mentioned in Chapter 3, the resistance values of R_1 and R_2 were minimized to reduce the effect of errors resultant from the base current of Q_{1B}. The base current error will be determined by generating a Thevenin equivalent for the output voltage and the resistors R_1 and R_2. This will result in an equivalent circuit with a voltage source, V_{TH}, and a series equivalent resistance, R_B, connected to the base of Q_{1B}. The values of the two equivalent elements are

$$V_{TH} = V_{OUT}\left(\frac{R_1}{R_1 + R_2}\right), \tag{C2.1}$$

and

$$R_B = \frac{R_1 R_2}{R_1 + R_2}. \tag{C2.2}$$

The base voltage of Q_{1B} can be expressed as

$$V_{BQ1B} = V_{TH} - I_{BQ1B}R_B, \tag{C2.3}$$

where the second term represents the error voltage at the base of Q_{1B} due to the base current, now defined as V_k. Note that this will be a fixed error since the collector current of Q_{1B} is fixed at 10 μA. An expression can now be generated that demonstrates the output voltage error due to the error voltage at the base:

$$V_{OEB} = V_k\left(\frac{R_1 + R_2}{R_1}\right) = \left(\frac{I_{CQ1B}}{\beta_{Q1B}}\right)\left(\frac{R_1 R_2}{R_1 + R_2}\right)\left(\frac{R_1 + R_2}{R_1}\right) = \left(\frac{I_{CQ1B}}{\beta_{Q1B}}\right)(R_2). \tag{C2.4}$$

Assuming a β of 250 for Q_{1B} and R_2 = 15.8 KΩ, the output error due to the base current of Q_{1B} is 0.628 mV. This results in an input-referred error of 0.1456%. This error can be reduced by decreasing the value of R_2.

Additionally, ratioing the outputs of the two logarithmic conversion circuits will not eliminate this error unless the two output voltages and associated offsets are exactly the

same. The output voltage error E_B of the two ratioed outputs due to the base current errors is expressed as

$$E_B = \left(\frac{V_{OUTI} - V_{OUTA}}{V_{OUTI}} \right)(100) , \tag{C2.5}$$

where V_{OUTI} is the ideal output voltage and V_{OUTA} is the actual output voltage including the base current error term. For this derivation, V_{OUT2} represents the logarithmic amplifier used only to track the temperature, and V_{OUT1} represents the current measuring logarithmic amplifier. Additionally the error terms due to the base current are represented as V_{OS1} and V_{OS2}, for V_{OUT1} and V_{OUT2} respectively. Using these variables, the percent error of the output voltage is expressed as:

$$E_B = \left[1 - \left(\frac{V_{OUT2}}{V_{OUT1}} \right) \left(\frac{V_{OUT1} + V_{OS1}}{V_{OUT2} + V_{OS2}} \right) \right](100) . \tag{C2.6}$$

In the seventh decade at 300 K, this represents an input-referred error of 0.0541%.

Derivation of the input-referred error ε_i

The ideal input current for a given output voltage is given by

$$I_{INI} = \frac{I_{REF}}{e^{\left(\frac{V_{OUT}}{K}\right)}}, \tag{C3.1}$$

where K is the log scale factor. An error in the log scale factor, represented as ε_k, can be entered into Equation (C1.1) to generate an actual input current expression:

$$I_{INA} = \frac{I_{REF}}{e^{\left(\frac{V_{OUT}}{k(1-\varepsilon_k)}\right)}}. \tag{C3.2}$$

The input-referred error is

$$\varepsilon = \left(\frac{I_{INA} - I_{INI}}{I_{INI}}\right) = \frac{\frac{I_{REF}}{e^{\left[\frac{V_{OUT}}{K(1-\varepsilon_k)}\right]}} - \frac{I_{REF}}{e^{\left(\frac{V_{OUT}}{K}\right)}}}{\frac{I_{REF}}{e^{\left(\frac{V_{OUT}}{K}\right)}}}. \tag{C3.3}$$

This expression reduces to

$$\varepsilon = e^{\left[\frac{V_{OUT}}{K}\right]\left[1-\frac{1}{(1-\varepsilon_k)}\right]} - 1 \approx e^{\left[\frac{V_{OUT}}{K(-\varepsilon_k)}\right]} - 1. \tag{C3.4}$$

The output voltage is given by

$$V_{OUT} = K\ln(10)\log\left(\frac{I_{REF}}{I_{IN}}\right) = K\ln(10)i, \tag{C3.5}$$

where i is the input current decade. Substituting Equation (C3.5) into Equation (C3.4), the input-referred error in the ith decade can be expressed as

$$\varepsilon_i = e^{-i\ln(10)\varepsilon_k} - 1. \tag{C3.6}$$

Appendix D.

MATHCAD PROGRAMS

The programs illustrated at the end of this appendix were written to calculate the open-loop and closed-loop gain and phase, and to predict the phase margin as a function of a variable compensation capacitance and the input current.

MATHCAD PROGRAM 1 - OPEN AND CLOSED-LOOP GAIN AND PHASE

$n := 500, 505 .. 1600 \quad I_D := 1\cdot10^{-5} \quad Aol := 2.514\cdot10^{6} \quad C_f := 18\cdot10^{-12}$

$\omega_n := .0000001\cdot10^{\frac{n}{100}} \quad C_i := 200\cdot10^{-12} \quad R_i := \frac{80}{I_D} \quad r_f := \frac{.026}{I_D}\cdot16.8$

$\omega_1 := 2\cdot\pi\cdot.8 \quad \omega_2 := 2\cdot\pi\cdot11.438\cdot10^{6} \quad \omega_3 := \frac{1}{R_i\cdot(C_i + C_f)}$

$$A(\omega) := \frac{Aol}{\left(1 + \frac{j\cdot\omega}{\omega_1}\right)\cdot\left(1 + \frac{j\cdot\omega}{\omega_2}\right)} \qquad B(\omega) := \frac{R_i}{r_f}\cdot\left[\frac{1 + j\cdot\omega\cdot r_f\cdot C_f}{\left(1 + \frac{j\cdot\omega}{\omega_3}\right)}\right]$$

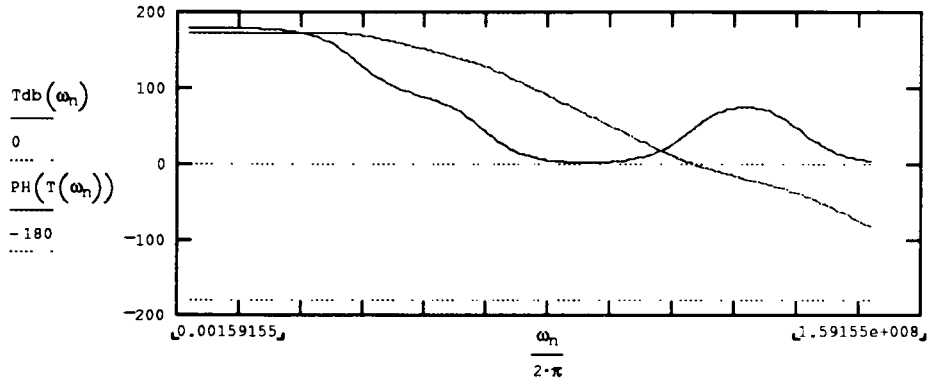
$T(\omega) := -A(\omega)\cdot B(\omega)$ **Phase Margin seed value:** $\phi := 200$

$Tdb(\omega) := 20\cdot\log(|T(\omega)|)$ **(dB)** $\quad PH(\theta) := \frac{180}{\pi}\cdot\arg(\theta)$

$Tdb(.013) = 173.263 \qquad PM := PH(T(root(|T(\phi)| - 1, \phi)))$

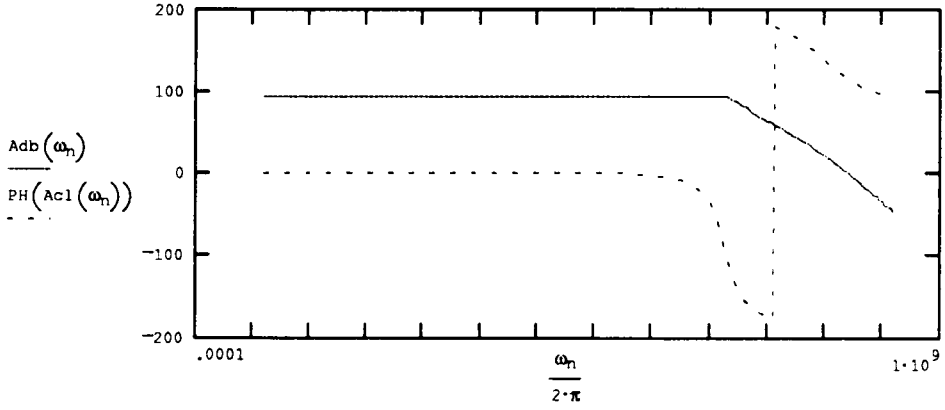
OPEN-LOOP GAIN AND PHASE

Phase Margin: PM = 46.773 **(Degrees)**



$$Acl(\omega) := \frac{r_f}{1 + j\cdot\omega\cdot C_f\cdot r_f}\cdot\frac{-T(\omega)}{1 - T(\omega)} \qquad Adb(\omega) := 20\cdot\log(|Acl(\omega)|)$$

CLOSED-LOOP GAIN AND PHASE



MATHCAD PROGRAM 2 - PHASE MARGIN CALCULATIONS

$n := 120, 125 .. 1500 \quad m := 5 .. 12 \quad p := 1 .. 7 \quad C_i := 200 \cdot 10^{-12} \quad \phi := 200$

$\omega_n := .001 \cdot 10^{\frac{n}{100}} \quad I_{D_m} := 10^{-m} \quad R_{i_m} := \frac{80}{I_{D_m}} \quad C_{F_p} := p \cdot 10^{-11} \quad r_{f_m} := \frac{.026}{I_{D_m}} \cdot 16.8$

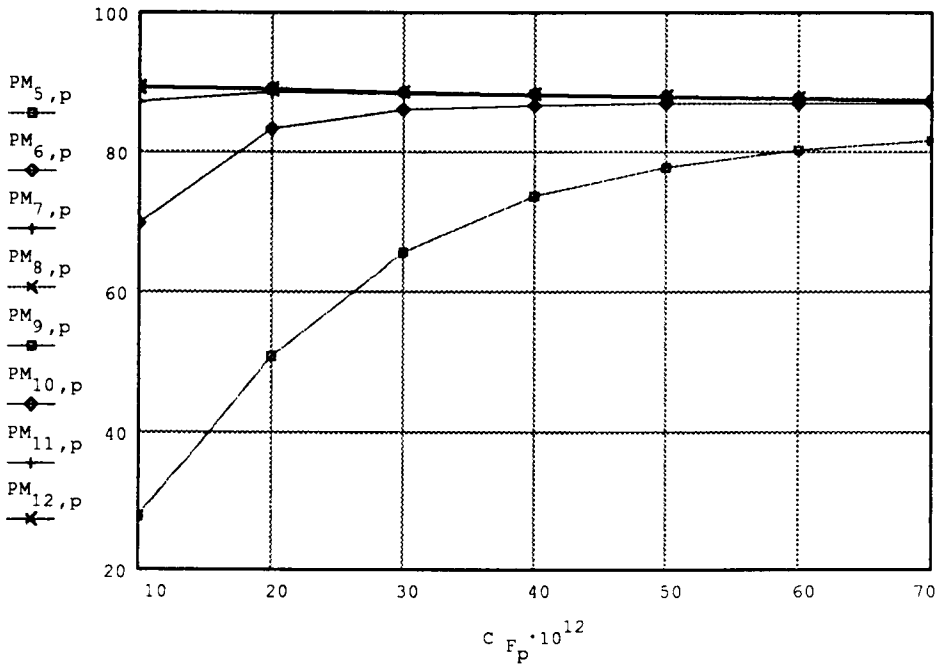
$\omega_1 := 2 \cdot \pi \cdot .8 \quad \omega_2 := 2 \cdot \pi \cdot 11.438 \cdot 10^6 \quad \omega_{3_{m,p}} := \frac{1}{R_{i_m} \cdot (C_i + C_{F_p})}$

$$T(\omega) := \frac{R_{i_m} \cdot -2.516 \cdot 10^6}{r_{f_m}} \cdot \left[\frac{1 + j \cdot \omega \cdot r_{f_m} \cdot C_{F_p}}{\left(1 + \frac{j \cdot \omega}{\omega_1}\right) \cdot \left(1 + \frac{j \cdot \omega}{\omega_2}\right) \cdot \left(1 + \frac{j \cdot \omega}{\omega_{3_{m,p}}}\right)} \right]$$

$Tdb(\omega) := 20 \cdot \log(|T(\omega)|)$ (dB) $\qquad PH(\theta) := \frac{180}{\pi} \cdot \arg(\theta)$ (degrees)

$PM_{m,p} := PH(T(root(|T(\phi)| - 1, \phi)))$ (degrees)

PHASE MARGIN PLOT



VITA

Milton Nance Ericson was born on March 21, 1965, in Memphis, Tennessee. He was reared in Memphis and graduated from First Assembly Christian School. He entered Christian Brothers College in 1983 and received the Bachelor of Science degree in Electrical Engineering in May 1987. As an undergraduate, he was initiated into Tau Beta Pi and Alpha Chi honor societies.

In June 1987, he joined the Oak Ridge National Laboratory as a development engineer in the Monolithic Systems Development Group of the Instrumentation and Controls Division. His areas of interest include analog and digital application specific integrated circuit design, microprocessor-based instrumentation, and electrometer circuits.

He married Helen Marie Slavick of Memphis, Tennessee, in July 1988.