To the Graduate Council:

I am submitting herewith a thesis written by Daniel W. McDonald entitled "AC Power Control in the Core Flow Test Loop." I recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

T. Vaughn Blalock, Major Professor

We have read this thesis
and recommend its acceptance:

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Graduate Studies and Research

8

AC POWER CONTROL IN THE CORE FLOW TEST LOOP

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Daniel W. McDonald

March 1979

1291531

DEDICATION

To Victoria for allowing her man this temporary diversion .....

To Marty who wants to grow up to be an engineer and drive a train .....

To Anne Marie who'll never remember what the rest of us went through for this .....

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ABSTRACT

This work represents a status report on a development effort to design an a.c. power controller for the Core Flow Test Loop. The Core Flow Test Loop will be an engineering test facility which will simulate the thermal environment of a gas-cooled fast-breeder reactor. The problems and limitations of using sinusoidal a.c. power to simulate the power generated within a nuclear reactor are adressed.

The transformer-thyristor configuration chosen for the Core Flow Test Loop power supply is presented. The initial considerations, design, and analysis of a closed-loop controller prototype are detailed. The design is then analyzed for improved performance possibilities and failure modes are investigated at length. A summary of the work completed to date and a proposed outline for continued development completes the report.

TABLE OF CONTENTS

CHAPTER		PAGE
I.	INTRODUCTION	1
	Background	1
	Scope of Thesis	2
II.	ELECTRICAL POWER CONTROL	3
	Industrial Options	3
	Power Control with Thyristors	7
	Transformer/Thyristor Configurations	18
III.	CFTL CLOSED-LOOP POWER CONTROLLER DESIGN	27
	Initial Considerations	27
	1. The Concept of Electrical Power	27
	2. Controller Bandwidth	30
	3. The CFTL Power Distribution System	37
	4. Power Feedback Considerations	39
	The Control Scheme	43
	1. Circuits	45
	a. Analog Signal Conditioning	45
	i. The Feedback Signal Conditioner	45
	ii. Scaling and Error Signal Generation	47
	iii. The Strobeless Analog to Digital Converter	49
	b. Digital Signal Conditioning	49
	i. Mode Selection and Decoding Logic	52
	ii. Timing and Control Logic	52

CHAPTER PAGE

2. Failure Mode Analysis 56

a. Noise 58

b. Chip Failure 58

i. The Analog Signal Conditioner (ASC) 58

ii. The Analog to Digital Converter (ADC) 59

iii. The Digital Signal Conditioner (DSC) 59

Safe Shutdown 61

An SCR Firing Circuit 62

IV. SYSTEM PERFORMANCE 65

The Analysis Problem 65

Initial Results 67

The Pseudo-Limit Cycle 68

Quantization and Time Averaging 68

Feedforward Control 77

Saturation 82

Discussion of Low Frequency Noise 83

1. The Low Frequency Noise/Accuracy Trade Off 83

2. The Spurious Rod Motion/Accuracy Controversy 83

V. CONCLUSIONS AND PROPOSED CONTINUATION 86

Summary of Progress to Date 86

Proposed Outline for Continued Development 88

REFERENCES 90

BIBLIOGRAPHY 92

VITA 95

LIST OF TABLES

TABLE		PAGE
2.1	PERCENT POWER FOR VARIOUS PHASE-FIRED CONDUCTION ANGLES	12
2.2	NORMALIZED VOLTAGE AND POWER OUTPUT OF ROBERTS/ROCHELLE LINEAR MULTIVOLTAGE SYSTEM	22
2.3	LMPL POWER SUPPLY: CONTROL MODE CHARACTERISTICS FOR SINGLE WINDING	25
3.1	THRESHOLD LIMITS AND OUTPUT CODE OF ANALOG TO DIGITAL CONVERTER	51
3.2	A FEW SOURCES OF BUNDLE POWER SYSTEM FAILURE	57
4.1	PARAMETER VALUES AT n^{th} SAMPLING INSTANT FOR SIMPLE PROPORTIONAL CONTROLLER	70
4.2	PARAMETER VALUES AT n^{th} SAMPLING INSTANT FOR TIME AVERAGED FEEDBACK CONTROLLER	72
4.3	LMPL POWER SUPPLY: CONTROL MODE CHARACTERISTICS FOR SINGLE WINDING	84

LIST OF FIGURES

FIGURE		PAGE
1.	Simplified Schematic of Induction Devices	5
2.	Thyristor Volt-Ampere Characteristics	6
3.	Thyristor Controlled Lighting	8
4.	Representation of Firing and Conduction Angle	8
5.	Spectral Content of 90° Phase Fired Waveform	16
6.	Zero-Phase Fired Waveforms and Resulting Power	19
7.	The Roberts-Rochelle Linear Multivoltage System	20
8.	The Hudson Linear Multipower System	23
9.	Representation of Voltage, Current, and Power Waveforms	28
10.	Measured Load Power (Filtered) Superimposed over Setpoint	31
11.	Signal Bandwidth of Linear Ramps Modulating 120 Hz Power Sinusoid	35
12.	CFTL Power Distribution Network	38
13.	Zone Partitioning for 37 Rod Bundle	40
14.	Simplified Block Diagram of Controller	44
15.	Feedback Signal Conditioner	46
16.	Scaler and Error Signal Generator	48
17.	Strobeless Analog to Digital Converter	50
18.	Multiplexer and Decoder	53
19.	Timing and Control Logic	55
20.	Edge-Sensitive SCR Firing Circuit	63
21.	Four Tap Transformer Prototype	66
22.	Initial Circuit Performance to Ramp Input	69

FIGURE PAGE

23. Sampled Proportional Controller 71

24. Output of Sampled Proportional Controller with 1V/s Input Ramp 72

25. Sampled Proportional Controller with Single Pole Filter in Feedback Loop 74

26. Output of Sampled Proportional Controller with Single Pole Filter in Feedback Loop with 1V/sec Input Ramp 74

27. Plot of Setpoint, WTAP, and Error 76

28. Proportional Controller Performance 78

29. Proportional Controller with Feedforward 80

30. Controller Performance with Feedforward 81

LIST OF SYMBOLS

$v(t)$	=	instantaneous voltage
$p(t)$	=	instantaneous power
ω	=	radian frequency
t	=	time
T	=	period of repetitive waveform
T_r	=	time for normalized ramp to reach unity
P_{AVE}	=	classical average power
a_n	=	coefficients of cosine terms in Fourier Series
b_n	=	coefficients of sine terms in Fourier Series
$p_m(t)$	=	instantaneous modulated power
$P_m(\omega)$	=	Fourier transform of $p_m(t)$

LIST OF ACRONYMS

DOE	=	Department of Energy
ORNL	=	Oak Ridge National Laboratory
THTF	=	Thermal Hydraulic Test Facility
THORS	=	Thermal Hydraulic Out of Reactor Safety Facility
CFTL	=	Core Flow Test Loop
FRS	=	Fuel Rod Simulators
SCR	=	Silicon Controlled Rectifier
EMI	=	Electromagnetic Interference
LMVS	=	Linear Multi-Voltage System
LMPS	=	Linear Multi-Power System
ASC	=	Analog Signal Conditioner
ADC	=	Analog-to-Digital Converter
DSC	=	Digital Signal Conditioner
RMS	=	Root Mean Square
WTAP	=	Weighted Time-Averaged Power

CHAPTER I

INTRODUCTION

Background

The Department of Energy (DOE) has constructed several major engineering test facilities to determine empirically the response of nuclear reactors to normal and emergency transients. Two such facilities are operating at the Oak Ridge National Laboratory (ORNL). One, the Thermal Hydraulic Test Facility (THTF) is used to study the results of transients in light water nuclear reactors and the other the Thermal Hydraulic Out of Reactor Safety Facility (THORS) is used to evaluate liquid sodium cooled nuclear reactors. A new facility is being constructed at ORNL which will be used to investigate a helium cooled breeder reactor concept which DOE would like to have commercialized in the 1990's. This facility will be called the Core Flow Test Loop (CFTL) and will be operated in the 1980's. The CFTL will be used specifically to verify computer simulations of the expected thermal and mechanical dynamics of a gas cooled reactor. One of the many engineering challenges associated with this loop will be the precise control of up to 6 MW of electrical power which will be dissipated by resistive fuel rod simulators (FRS). This power will simulate the power generated within a nuclear reactor. It must be precisely controlled to simulate a variety of nuclear reactor conditions including normal daily load variations, controlled shutdown for scheduled refueling, emergency shutdowns and reactor after-heat. This paper investigates the problems

associated with a.c. power control and reports on the current status of a development effort to solve these problems for CFTL.

Scope of Thesis

This work is a status report on work completed to date to develop an a.c. power control scheme for the Core Flow Test Loop. The specifications this scheme must meet are formidable. They include the adherence of the output to the set-point request to better than 1% of setting over a 900:1 dynamic range, generation of linear power ramps as fast as 324 KW/second, generation of no electromagnetic interference in the instrumentation bandwidth and an inherently fail-safe design.

Chapter II covers classical power control schemes and introduces the reader to power control concepts employing thyristors. This section also introduces two unique transformer-thyristor configurations which tend to minimize the problems associated with thyristor power control.

Chapter III details the design considerations and resulting circuits used in a prototype closed-loop power controller. A failure mode analysis of this circuit is also done to verify that all errors and failures will be fail-safe faults.

Chapter IV discusses the performance of the prototype system and analyzes the result of several system non-linearities. The inherent limitations of the transformer-thyristor configuration chosen for CFTL are then discussed along with the problem of extrapolating the results of the prototype's performance to the larger CFTL system.

Chapter V concludes with a summary of progress to date and a proposed outline for continued development.

CHAPTER II

ELECTRICAL POWER CONTROL

Industrial Options

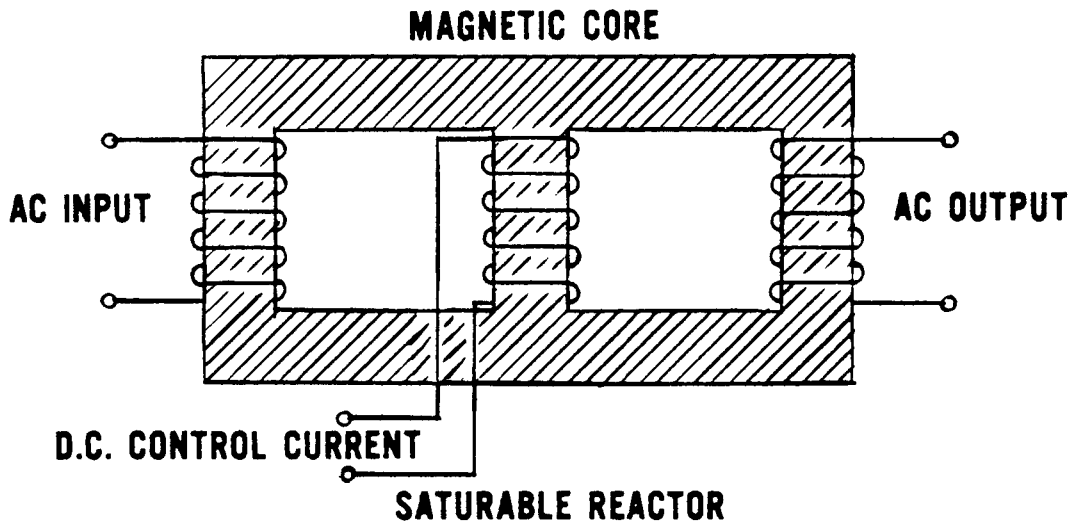
There are many options available in industry for the conversion and control of high level power. These options include generators, variable inductance devices, and various thyristor controlled power conversion schemes. Generators are devices which convert energy of one form to another. In the CFTL application the useful output energy form is electrical energy. This electrical energy must be a.c. since d.c. power will interfere with loop instrumentation.(1) Generators which use mechanical energy as their input are typically used in constant load situations and cannot vary their output power fast enough for CFTL requirements. Generators which use electrical energy as their inputs can typically cover a wide dynamic power range quickly but tend to be inefficient or are used as a.c. to d.c. converters and thus cannot be used in CFTL.

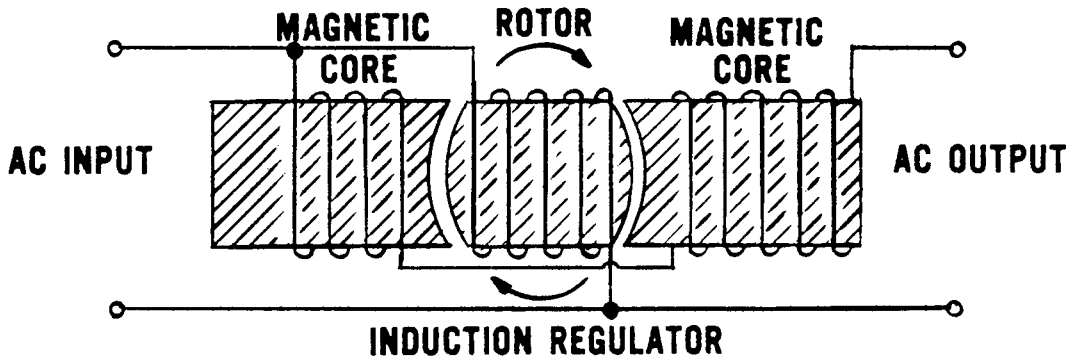
Variable inductance devices are commonly used to control a.c. power. By varying the magnetic coupling between isolated windings the output voltage of these devices can be modulated. Examples are induction regulators, and saturable reactors. In induction regulators the magnetic coupling is influenced by the mechanical movement of magnetic material within the windings. In saturable reactors a dc current is introduced around a magnetic core which degrades the coupling efficiency between the windings and decreases the output voltage. Variacs are often classed with these types of devices but do not operate

on a variable coupling principle. In variacs a single winding exists with a moving mechanical tap. The tap is moved along the length of the winding to give a varying voltage operating in a fashion similiar to a resistive potentiometer. Simplified drawings of the operating principle of these devices are given in Figure 1. None of these devices can vary their output adequately for CFTL.

The thyristor is a bistable solid state device. The thyristor family includes a wide class of devices. The devices which shall be discussed here are the silicon controlled rectifier (SCR) and the triac. The SCR, is as its name implies, a rectifier with control capability. The SCR is similiar to conventional rectifiers or diodes in that it can not conduct when there is a reverse or negative voltage between its anode and cathode (unless a critical voltage known as the breakdown voltage is exceeded). An SCR differs from conventional rectifiers, however, with a positive voltage applied across the anode and cathode in that it will not conduct unless current is injected into its control or "gate" terminal. Once current is injected into the gate, the device will continue to conduct even if the gate current goes to zero. The SCR will not turn "off" or cease to conduct until either the voltage across it goes negative or the current through it has decreased below some minimum threshold current referred to as the "holding current". These devices are traditionally used in d.c. circuits because of their single polarity operation.

A thyristor which can conduct for either polarity input is called a triac. Its volt ampere characteristic is shown in Figure 2 with that of an SCR. The triac is useful in the medium to high power level range of





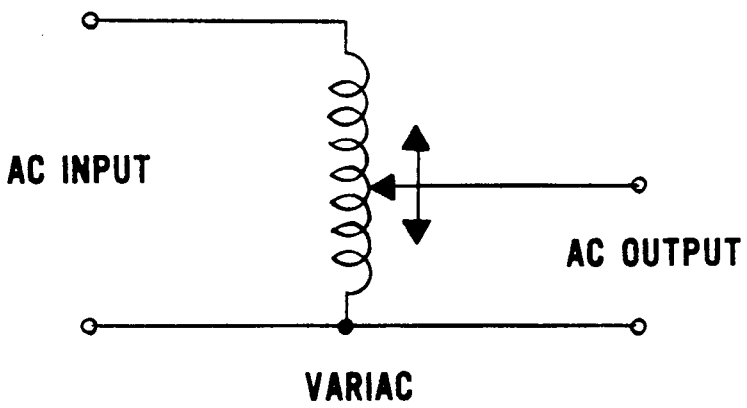
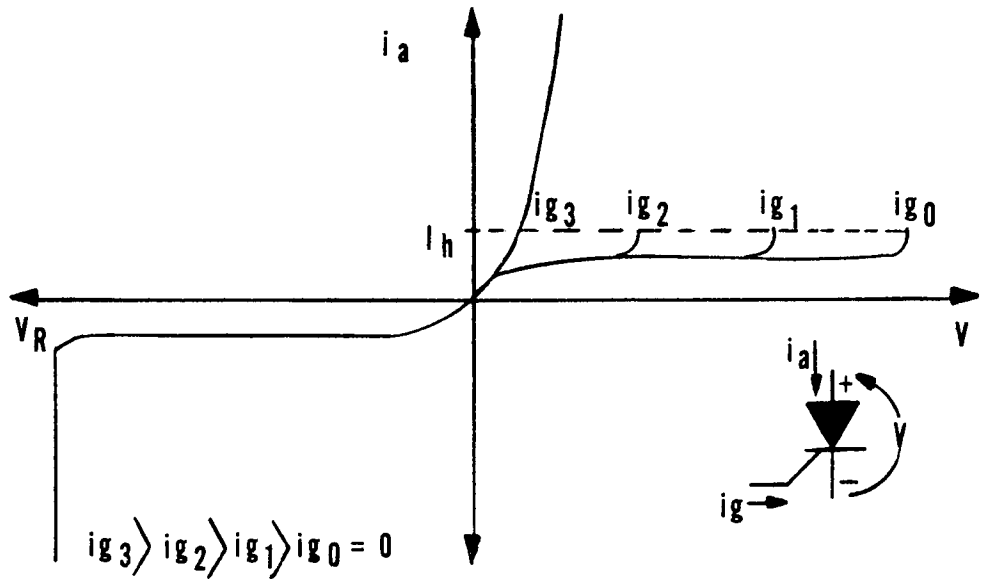
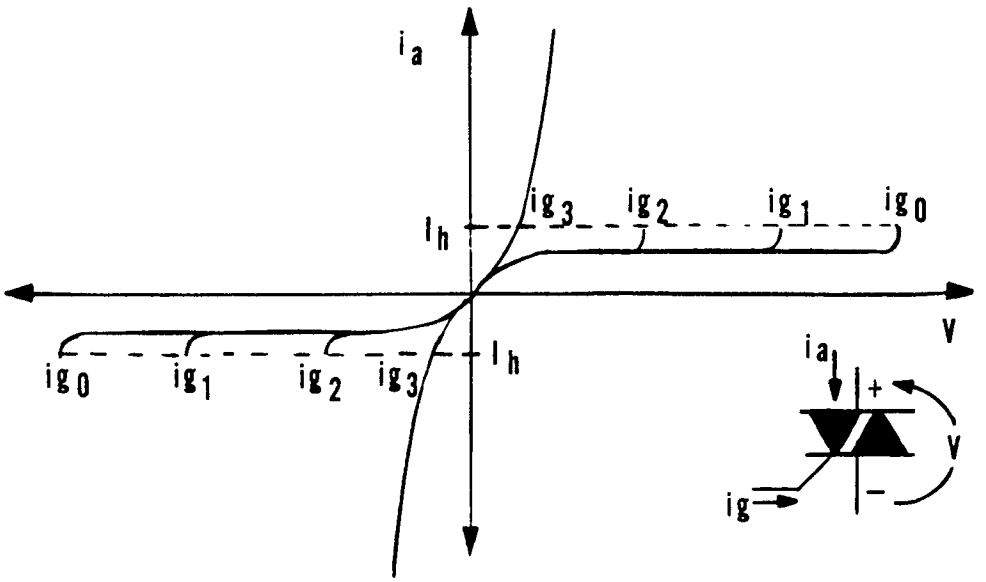


FIG.1 SIMPLIFIED SCHEMATIC OF INDUCTION DEVICES



SCR VOLT–AMPERE CHARACTERISTIC



TRIAC VOLT–AMPERE CHARACTERISTIC

FIG.2 THYRISTOR VOLT–AMPERE CHARACTERISTICS

power control but is not available for the very high power applications. In these cases two SCRs in parallel, with the anode of one connected to the cathode of the other must be used. Silicon controlled rectifiers exist which when used in this configuration can conduct in excess of 1,600 A_{rms} and can withstand peak reverse voltages in excess of 1,600 volts. This dual SCR configuration was chose for CFTL since the device had to be able to conduct 1,650 A_{rms}.

Power Control with Thyristors

The thyristor is used in power control applications as a switch which allows some fraction of the input voltage waveform to be transmitted to the load. Figure 3 shows a simple power control scheme. If the triac is allowed to conduct for the entire duration of a 60 Hz waveform the light is completely turned on and is at its brightest. If the triac is not turned on but is kept off for some time delay and then turned on it will conduct only a portion of the waveform and the light will appear dimmer. Since most a.c. power control applications involve sinusoidal waveforms the time delay before which the SCR is turned on has been related to the phase angle of the waveform. The "firing angle" refers to the phase angle at which the SCR was turned on. In Figure 4 the SCR was turned on when the waveform was at 45 degrees, thus the firing angle is 45 degrees. The "conduction angle" is a term which refers to the number of degrees that the SCR conducts. Again referring to Figure 4 the conduction angle is 135 degrees. Notice that these terms are referenced to one half of a sine wave. This convention will be carried throughout this paper for both SCRs which can only conduct a

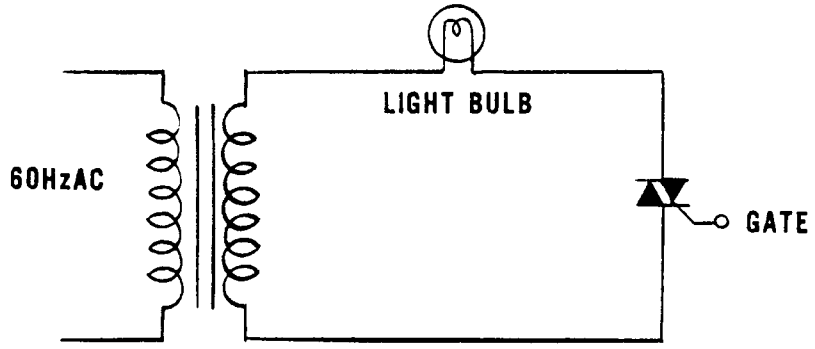


FIG. 3 THYRISTOR CONTROLLED LIGHTING

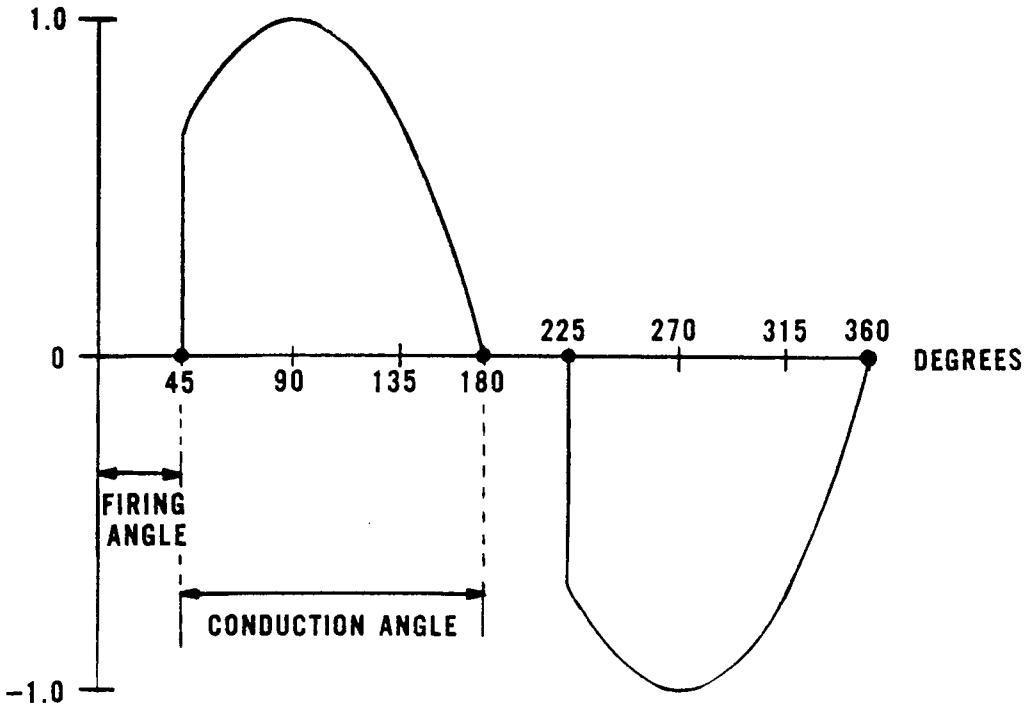


FIG. 4 REPRESENTATION OF FIRING AND CONDUCTION ANGLE

maximum of one-half of a sine wave anyway and triacs which can conduct for the full 360 degrees. This is because transformers will be used to supply the a.c. voltage in CFTL. If a triac turns on at 45 degrees of one-half cycle then it must turn on at 45 degrees of the next half cycle. This symmetry prevents any average or d.c. currents from being generated within the transformer windings. A d.c. current in a transformer will decrease its inductance and result in greater input currents. These currents may exceed the rating of the transformer and damage it. For the transformers used in CFTL a d.c. current in excess of 3% of rated current will cause serious damage.

Controlling power by varying the firing angle is referred to as phase-fired SCR power control. Phase-fired power control has several engineering advantages. They include conceptual simplicity, good power resolution, and fast response to set-point changes. Power resolution refers to the range over which power can be controlled. The time response of a phase-fired SCR power controller can be described as the time required to respond to a unit step change in the setpoint. It is apparent that a phase-fired controller can change its firing angle within the time of one full cycle.

It is instructive at this point to analyze the relationship between conduction angle and percent of power delivered to the load. Imagine a sinusoidal voltage v(t) across a 1 ohm resistor. The instantaneous power p(t) is given by

$$p(t) = v(t)^2 = (A \sin \omega t)^2, \tag{2-1}$$

$$= \frac{A^2}{2} (1 - \cos 2 \omega t). \tag{2-2}$$

For constant A the average power is given by

$$P_{AVE} = \int_0^T \frac{p(t)}{T}\, dt, \tag{2-3}$$

where T is the period of the waveform and is given by $T = \pi/\omega$,

$$P_{AVE} = \frac{A^2}{2}\left[\int_0^T \frac{dt}{T} - \int_0^T \frac{\cos 2\omega t}{T}\, dt \right], \tag{2-4}$$

$$= \frac{A^2}{2}. \tag{2-5}$$

For a conduction angle of 90 degrees,

$$P_{AVE} = \frac{A^2}{2}\left[\int_{T/2}^T \frac{dt}{T} - \int_{T/2}^T \frac{\cos 2\omega t}{T}\, dt \right], \tag{2-6}$$

$$P_{AVE} = \frac{A^2}{2}\left[\frac{T-T/2}{T} - \int_{\pi/2\omega}^{\pi/\omega} \frac{\cos 2\omega t}{\pi/\omega}\, dt \right], \tag{2-7}$$

$$= \frac{A^2}{2}\left[\frac{2T-T}{2T} - \frac{1}{\pi/\omega} \frac{\sin 2\omega t}{2\omega} \Bigg|_{\pi/2\omega}^{\pi/\omega} \right], \tag{2-8}$$

$$= \frac{A^2}{2}\left[\frac{1}{2} - \frac{1}{2\pi}\left(\sin 2\pi - \sin \pi \right) \right], \tag{2-9}$$

$$= \frac{A^2}{4}. \tag{2-10}$$

Thus allowing 50% of the power sinusoid to be delivered to the load results in a 50% decrease in average power delivered to the load. Table 2.1 summarizes the relationship for various conduction angles.

Phase-fired power control is the appropriate choice for many industrial applications because of the advantages discussed above. There is one disadvantage, however, which precludes its use in some applications. Phase-fired power control results in severe electromagnetic interference (EMI). Let's examine the spectral content of the 90 degree phase-fired waveform.

The Fourier Series of the voltage waveform can be expressed as

$$v(t) = \sum_{n=0}^{\infty} \left(a_n \cos \frac{2n\pi t}{T} + b_n \sin \frac{2n\pi t}{T}\right) , \qquad (2\text{-}11)$$

where

$$a_n = \frac{2}{T}\int_0^T v(t)\cos\frac{2n\pi t}{T}\, dt \; ; \; n = 0, 1, 2, 3, \ldots . , \qquad (2\text{-}12)$$

$$b_n = \frac{2}{T}\int_0^T v(t)\sin\frac{2n\pi t}{T}\, dt \; ; \; n = 1, 2, 3, \ldots . , \qquad (2\text{-}13)$$

where $T = 2\pi/\omega$ is the period of $v(t)$. Substituting $v(t) = A \sin \omega t$ into the above equations gives

$$a_n = \frac{2A}{T}\int_0^T \sin \omega t \cos \frac{2n\pi t}{T}\, dt , \qquad (2\text{-}14)$$

TABLE 2.1

PERCENT POWER FOR VARIOUS PHASE-FIRED CONDUCTION ANGLES

PERCENT POWER	CONDUCTION ANGLE
0	0
10	18°
20	36°
30	54°
40	72°
50	90°
60	108°
70	126°
80	144°
90	162°
100	180°

$$b_n = \frac{2A}{T} \int_0^T \sin \omega t \sin \frac{2n\pi t}{T} \, dt \, . \qquad (2\text{-}15)$$

For a 90 degree conduction angle voltage waveform, the above equations become

$$a_n = \frac{A\omega}{\pi} \left[\int_{\pi/2\omega}^{\pi/\omega} \sin\omega t \cos n\omega t \, dt + \int_{3\pi/2\omega}^{2\pi/\omega} \sin\omega t \cos n\omega t \, dt \right] , \qquad (2\text{-}16)$$

$$b_n = \frac{A\omega}{\pi} \left[\int_{\pi/2\omega}^{\pi/\omega} \sin\omega t \sin n\omega t \, dt + \int_{3\pi/2\omega}^{2\pi/\omega} \sin\omega t \sin n\omega t \, dt \right] . \qquad (2\text{-}17)$$

Simplifying yields

$$a_n = \frac{A\omega}{\pi} \left(\left[\frac{-\cos (\omega - n\omega) t}{2 (\omega - n\omega)} - \frac{\cos (\omega + n\omega) t}{2 (\omega + n\omega)} \right] \Bigg|_{\pi/2\omega}^{\pi/\omega} \right.$$

$$\left. \left[- \frac{\cos (\omega - n\omega) t}{2 (\omega - n\omega)} - \frac{\cos (\omega + n\omega) t}{2 (\omega + n\omega)} \right] \Bigg|_{3\pi/2\omega}^{2\pi/\omega} \right) \qquad n \neq 1 \, , \qquad (2\text{-}18)$$

$$b_n = \frac{A\omega}{\pi}\left(\left[\frac{\sin(\omega-n\omega)t}{2(\omega-n\omega)} - \frac{\sin(\omega+n\omega)t}{2(\omega+n\omega)} \right]\Bigg|_{\pi/2\omega}^{\pi/\omega} + \left[\frac{\sin(\omega-n\omega)t}{2(\omega-n\omega)} - \frac{\sin(\omega+n\omega)t}{2(\omega+n\omega)} \right]\Bigg|_{3\pi/2\omega}^{2\pi/\omega} \right) \quad n\neq 1 , \tag{2-19}$$

or,

$$a_n = \frac{A}{2\pi}\left[\frac{-\cos(1-n)\pi+\cos(1-n)\pi/2}{(1-n)} + \frac{-\cos(1+n)\pi+\cos(1+n)\pi/2}{(1+n)} + \frac{-\cos(1-n)2\pi+\cos(1-n)3\pi/2}{(1-n)} + \frac{-\cos(1+n)2\pi+\sin(1+n)3\pi/2}{(1+n)} \right]$$

$$n\neq 1 , \tag{2-20}$$

$$b_n = \frac{A}{2\pi}\left[\frac{\sin(1-n)\pi-\sin(1-n)\pi/2}{(1-n)} + \frac{-\sin(1+n)\pi+\sin(1+n)\pi/2}{(1+n)} + \frac{\sin(1-n)2\pi-\sin(1-n)3\pi/2}{(1-n)} + \frac{-\sin(1+n)2\pi+\sin(1+n)3\pi/2}{(1+n)} \right]$$

$$n\neq 1 , \tag{2-21}$$

For n = 1,

$$a_n = \frac{A\omega}{\pi}\int_{\pi/2\omega}^{\pi/\omega} \sin\omega t\cos\omega t\, dt + \int_{3\pi/2\omega}^{2\pi/\omega} \sin\omega t\cos\omega t\, dt , \tag{2-22}$$

$$a_1 = \frac{A\omega}{\pi}\left[\frac{\sin^2\omega t}{2\omega}\Bigg|_{\pi/2\omega}^{\pi/\omega} + \frac{\sin^2\omega t}{2\omega}\Bigg|_{3\pi/2\omega}^{2\pi/\omega}\right], \tag{2-23}$$

$$= -\frac{A}{\pi}. \tag{2-24}$$

and

$$b_1 = \frac{A\omega}{\pi}\left[\int_{\pi/2\omega}^{\pi/\omega} \sin^2\omega t\, dt + \int_{3\pi/2\omega}^{2\pi/\omega} \sin^2\omega t\, dt\right], \tag{2-25}$$

$$= \frac{A\omega}{\pi}\left[\left(\frac{t}{2} - \frac{1}{4\omega}\sin 2\omega t\right)\Bigg|_{\pi/2\omega}^{\pi/\omega} + \left(\frac{t}{2} - \frac{1}{4\omega}\sin 2\,\omega t\right)\Bigg|_{3\pi/2\omega}^{2\pi/\omega}\right], \tag{2-26}$$

$$= \frac{A}{2}. \tag{2-27}$$

for $n>1$, $b_n=0$ and a_n has values only for odd n (i.e., n=3, 5, 7, 9 ....)

Figure 5 shows the spectral content of this phase fired waveform. Note the significant high frequency components. Of particular concern are components in excess of 100 KHz. At these frequencies significant radiation begins to occur and idealized models for passive components particularly capacitors and inductors are no longer valid. Special shielding and filtering precautions must be taken in EMI sensitive environments if phase-fired control is used.

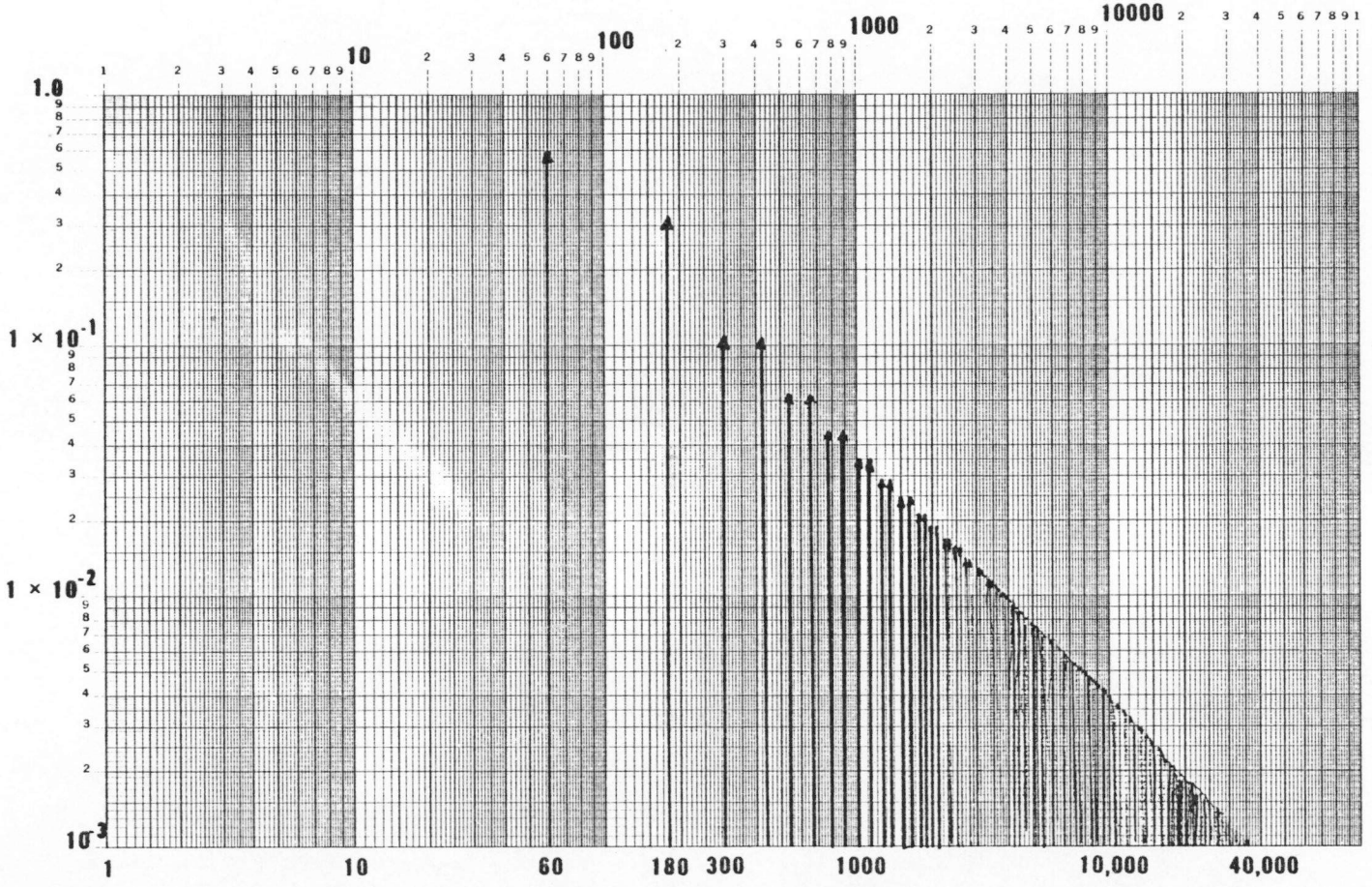


FIG. 5 SPECTRAL CONTENT OF 90^{0} PHASE FIRED WAVEFORM

The problem of electromagnetic interference is particularly acute in CFTL because the loop will be highly instrumented with many EMI sensitive devices. A possible helium flow measurement scheme involves the use of an ultrasonic flowmeter. This device must detect microvolt pulses in the frequency range around 100 KHz. Another ultrasonic device has been postulated to detect corona discharge around the helium circulator bearings. It will also be measuring low level, high frequency signals. Temperature measurement will be made with either Type K chromel/alumel thermocouples or type S platinum/platinum 10%-rhodium thermocouples. A type K thermocouple will output a signal of approximately 20 $\mu V/^{o}F$ while a Type S will give approximately 10 $\mu V/^{o}F$. The signals will be read from a high speed data acquisition system (20K readings/sec) during rapid temperature transients ($100^{o}C$/sec). Since all temperature measurements will be compared to limits, which if exceeded will cause loop shut down, a noise pulse could cause an expensive and unnecessary loop shut down. The low signal levels, wide instrumentation bandwidth, and close proximity of the thermocouples to the power leads all combine to make the CFTL instrumentation environment very EMI sensitive and preclude the use of a phase-fired power controlling scheme.

A thyristor controlled scheme which does not introduce as significant an EMI problem exists and has been chosen for CFTL. This technique is actually a subset of phase-fired power control in that the controlling voltage is turned on at a particular phase of the waveform. However in this method the phase angle is always zero degrees. The technique is called zero phase-fired power control and controls power by

allowing or not allowing certain complete cycles to be delivered to the load. For instance if one hundred percent of power is to be dissipated by the load then each cycle of the full sinusoid is delivered to the load. If 50% of power is required, then one full cycle is delivered to the load followed by the next cycle being blocked. Thus only one in every two cycles is delivered to the load. Figure 6 shows the required waveforms for various power levels. The one obvious disadvantage of this system is the delay/resolution trade off implicit in its design. For example to get one tenth of the maximum power one would block nine cycles and let one through thus requiring a time delay of ten cycles before the power level could be realized. This time delay is manifested in the loop instrumentation as low frequency noise. The above mentioned ten percent power level would introduce 6 Hz frequency components which lie in the measurement bandwidth of many of the CFTL instrumentation systems.

The problem is to design a system which offers the EMI advantages of the zero phase fired controller while minimizing the delay/resolution problem.

Transformer/Thyristor Configurations

Two such systems of power control have been proposed for CFTL. The first is presented schematically in Figure 7 and is called the Roberts/Rochelle linear multivoltage system (LMVS)[2]. The four transformer output windings are isolated from each other and are wound in such a manner that their output voltages are related by a factor of three. The bottom winding is wound for some voltage, x volts; the next

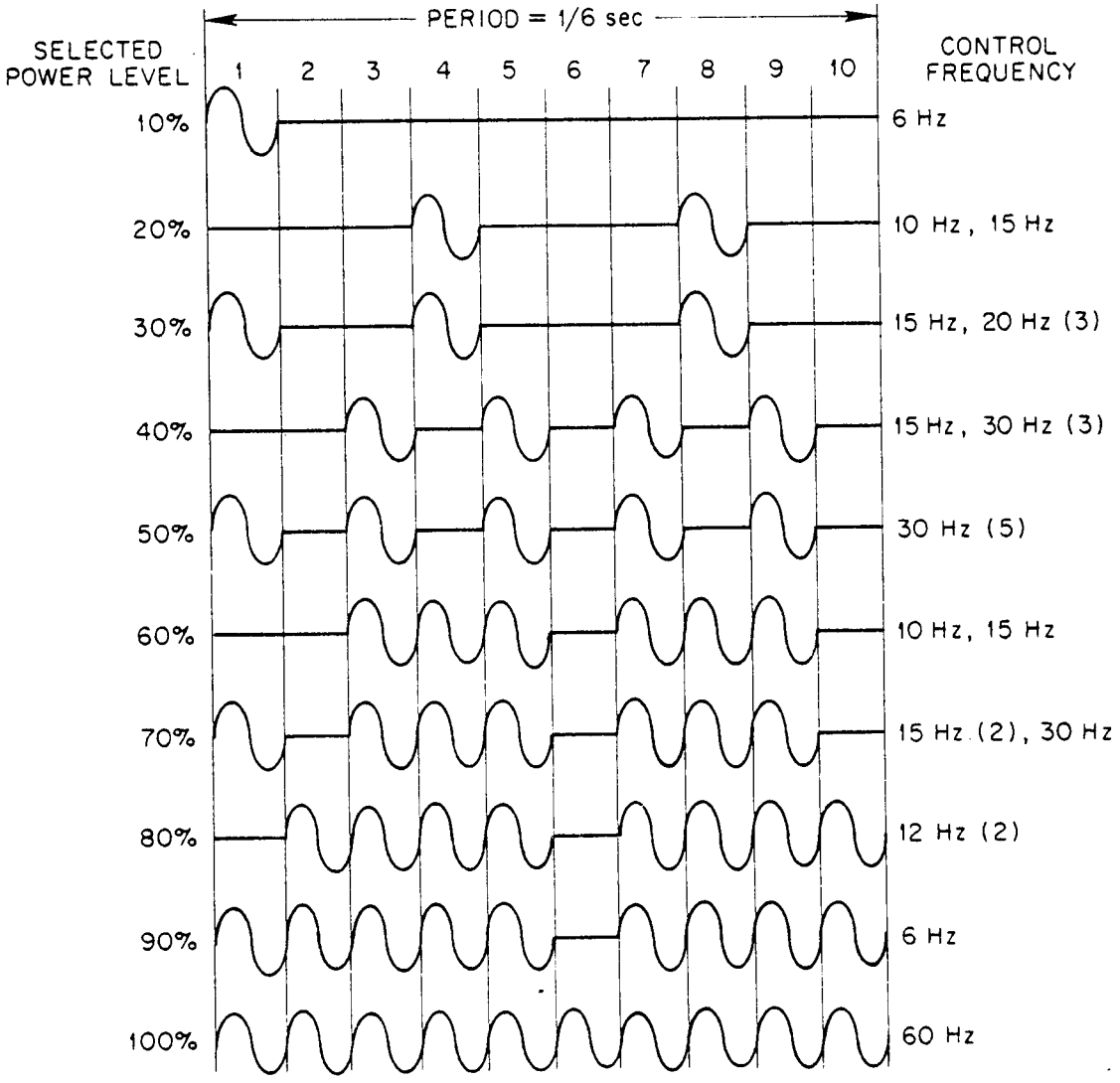


FIG. 6 ZERO–PHASE FIRED WAVEFORMS AND RESULTING POWER

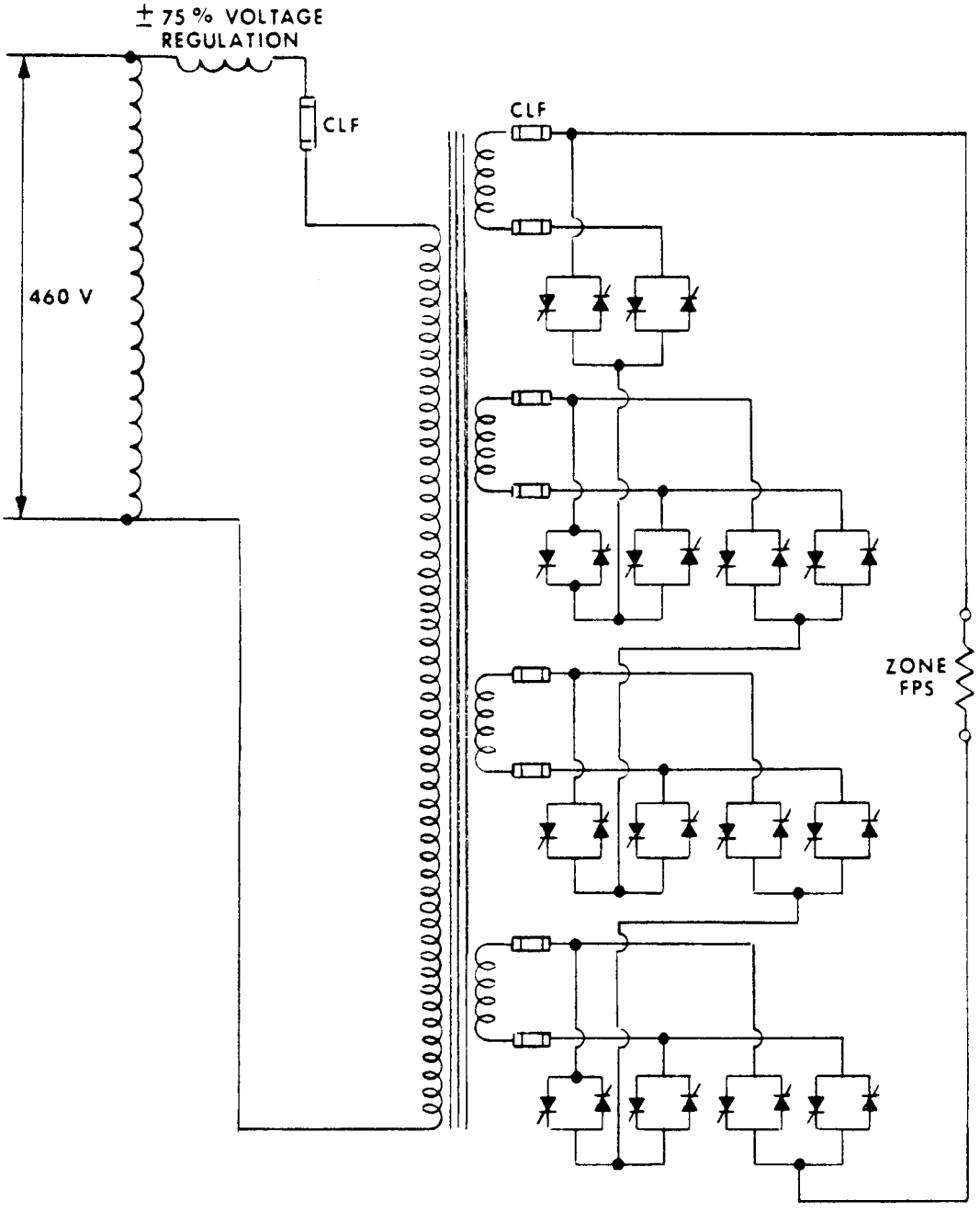


FIG. 7 THE ROBERTS–ROCHELLE LINEAR MULTIVOLTAGE SYSTEM

winding is wound for 3x volts; the next for 9x volts; and the last for 27x volts. By selectively turning on the proper SCR pairs, each winding can contribute its voltage to the load, be by-passed, or can subtract its voltage from the load. With proper SCR firing, forty distinct linarly related a.c. voltage levels can be realized. Table 2.2 summarizes the voltage and power output levels which can be realized with this system. The advantages of this system are (1) it does not generate low frequency noise (less than 16 Hz), (2) it minimizes high frequency noise (greater than 1KHz), and (3) offers fast, precise power control. The disadvantages of this supply are: only two power levels are available between 100% and 90% of full power (a range where many CFTL transients will occur), many of the available low power settings are superfluous for CFTL which need only go as low as 4% of full scale, and finally 7 SCR pairs must conduct simultaneously for any power step. There is therefore a large power loss due to the power dissipation of these 7 SCR pairs. Also a failure in one SCR pair will prevent the occurrence of many power levels. These limitations have removed this system from further consideration.

Another power supply alternative is the Hudson linear multipower level (LMPL) system indicated in Figure 8. In this system a multiple-tapped transformer is used with all of the taps related to each other in linear power increments. In the 15 tap system of Figure 8 the tap numbered 1 will supply 6-2/3% of the maximum available power to the load. Tap number 2 will supply 13-1/3%, tap 3 20%, etc., up to tap 15 which supplies 100%. Since only one SCR conducts at any time this system has 1/7 the loss of the Roberts/Rochelle system. A setpoint

TABLE 2.2

NORMALIZED VOLTAGE AND POWER OUTPUT
OF ROBERTS/ROCHELLE
LINEAR MULTIVOLTAGE SYSTEM

LEVEL	VOLTAGE	POWER	LEVEL	VOLTAGE	POWER
40	1.0000	1.0000	20	0.5000	0.2500
39	0.9750	0.9506	19	0.4750	0.2256
38	0.9500	0.9025	18	0.4500	0.2025
37	0.9250	0.8556	17	0.4250	0.1806
36	0.9000	0.8100	16	0.4000	0.1600
35	0.8750	0.7656	15	0.3750	0.1406
34	0.8500	0.7225	14	0.3500	0.1225
33	0.8250	0.6806	13	0.3250	0.1056
32	0.8000	0.6400	12	0.3000	0.0900
31	0.7750	0.6006	11	0.2750	0.0756
30	0.7500	0.5625	10	0.2500	0.0625
29	0.7250	0.5250	9	0.2250	0.0506
28	0.7000	0.4900	8	0.2000	0.0400
27	0.6750	0.4556	7	0.1750	0.0306
26	0.6500	0.4225	6	0.1500	0.0225
25	0.6250	0.3906	5	0.1250	0.0156
24	0.6000	0.3600	4	0.1000	0.0100
23	0.5750	0.3306	3	0.0750	0.0056
22	0.5500	0.3025	2	0.0500	0.0025
21	0.5250	0.2756	1	0.0250	0.0006

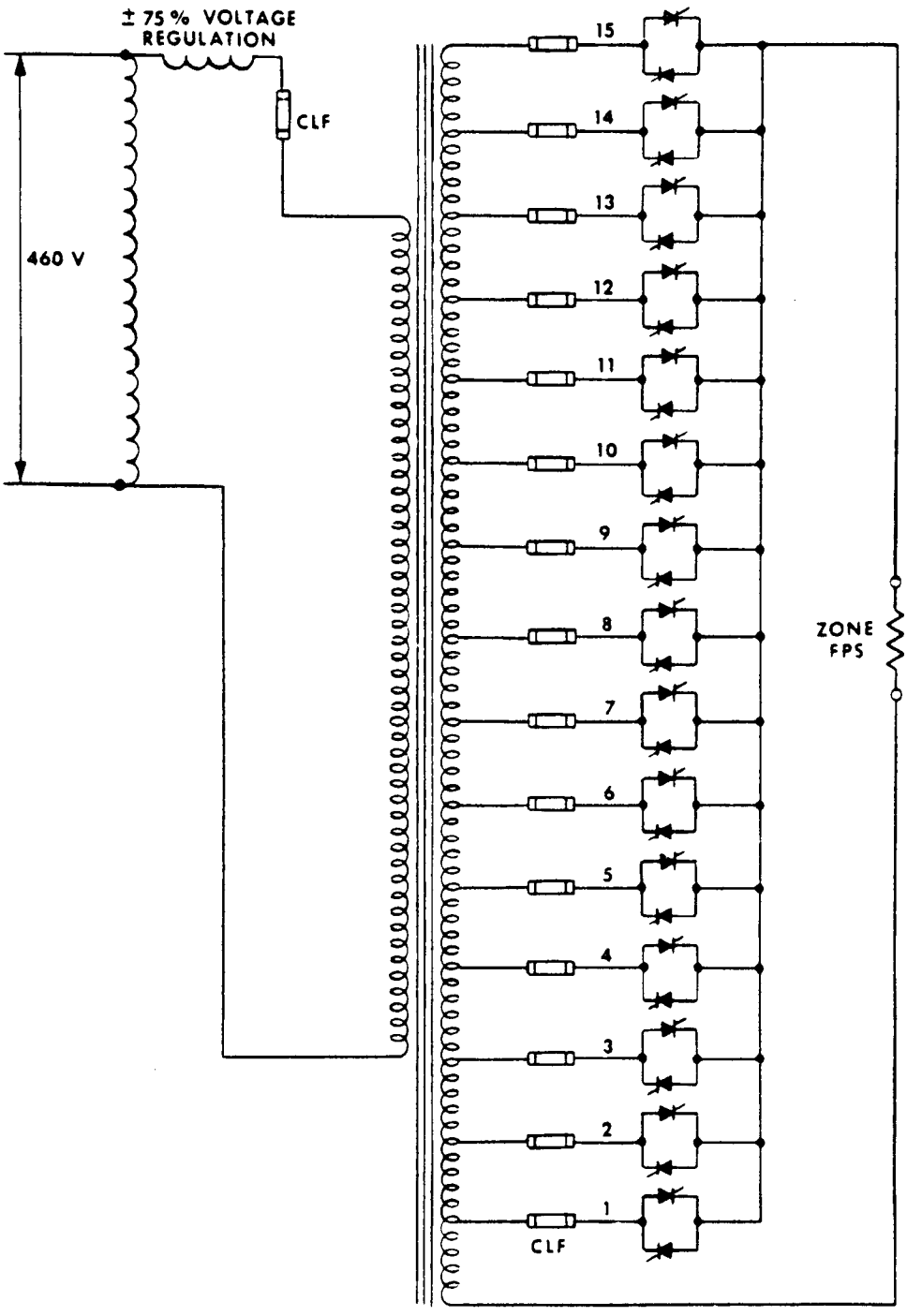


FIG. 8 THE HUDSON LINEAR MULTIPOWER SYSTEM

change from 100% to 6-2/3% can result in an output change in less than one cycle resulting in a time response comparable to that of the phase-fired system. A problem with this system however is that there are only 15 discrete power levels that the output can assume. This problem can be circumvented if we allow "cycle sharing" between taps. For instance since tap 15 gives 100% power and tap 14 gives 93-1/3% then we can obtain 96-2/3% by allowing tap 15 to conduct for one cycle and then tap 14 to conduct for the next. By repeating this pattern an average power of 96-2/3% is obtained. Table 2.3 summarizes the cycle sharing patterns which are practical along with the resulting low frequency components which are generated by this scheme. If the low frequency components are kept out of the instrumentation bandwidth, this system will be a reasonable solution to the CFTL power control problem. The same cycle-sharing scheme could be used with the Roberts/Rochelle system but the power loss problem still prevents its use here.

There are a few implementation problems associated with the Hudson system. The first is concerned with the construction of the multiple tap transformer. Since the taps must be integer multiples of complete windings, precise voltage levels cannot be obtained. Therefore each tap voltage will fall within some error band and must be measured after construction if precise open-loop power transient generation is desired. The second problem with this system is that variation of the tap voltages during operation due to thermal and electrical effects may be significant. Notice in Figure 8 that the multiple tapped transformer is fed by an induction regulator. This induction regulator will be motor driven and capable of varying the input voltage to the transformer over

TABLE 2.3

LMPL POWER SUPPLY: CONTROL MODE CHARACTERISTICS FOR SINGLE WINDING

(6.67% power per winding. These same characteristics apply to whichever of the 15 windings in the LMPL power supply is used to supply fine control)

Control Mode No.	Firing Pattern Tap No.	Percent of Total Power	Step change for decreasing power (%)	Dominant Power Frequency (Hz)
1	15-15-15-15-15-15	100.00		120
2	15-15-15-15-15-14	98.89	1.11	10
3	15-15-15-15-14	98.67	0.22	12
4	15-15-15-14	98.33	0.34	15
5	15-15-14	97.78	0.55	20
6	15-15-15-14-14	97.33	0.45	12
7	15-14-15-14	96.67	0.66	30
8	15-15-14-14-14	96.00	0.67	12
9	15-14-14	95.56	0.44	20
10	15-14-14-14	95.00	0.56	15
11	15-14-14-14-14	94.67	0.33	12
12	15-14-14-14-14-14	94.44	0.23	10
13	14-14-14-14-14-14	93.33	1.11	120
Next winding:				
13	14-14-14-14-14-14	93.33		120
14	14-14-14-14-14-13	92.22	1.11	10
15	14-14-14-14-13	92.00	0.22	12
	Etc.			

a very wide dynamic range. The tap voltages will vary in percent of full scale with changes in the input voltage and with changes in load. These effects suggest that precise power control is attainable only with closed loop control. A closed loop controller for this system has been developed and is described in the following chapter.

CHAPTER III

CFTL CLOSED-LOOP POWER CONTROLLER DESIGN

Initial Considerations

There are some rather stringent specifications which must be met by the CFTL power controller. These include adherence to power setpoint settings of better than 1%, capability to follow linear power transients as fast as 90% of full power per second and as slow as 0.0054% of full power per second precisely, power control over a wide dynamic range $(900:1)^3$, generation of no electromagnetic interference in the instrumentation bandwidth and an inherently fail safe design. Some of the specifications are mutually exclusive. For instance, to obtain some average power between those available directly on the taps require cycle sharing for several cycles. Averaging over several cycles decreases the time response (decreasing the controllers capability to follow the fast transients) and also introduces low frequency noise which may interfere with loop measurements.

1. The Concept of Electrical Power

In electrical systems the instantaneous power dissipated by a device is given by the product of the instantaneous voltage across the device and the instantaneous current through it (refer to Fig. 9).

In CFTL the combination of the Hudson LMPL system with resistive fuel rod simulators results in a sinusoidal instantaneous power. It will therefore be impossible to hold the instantaneous power constant in CFTL. Under steady state conditions the "average power" is defined as

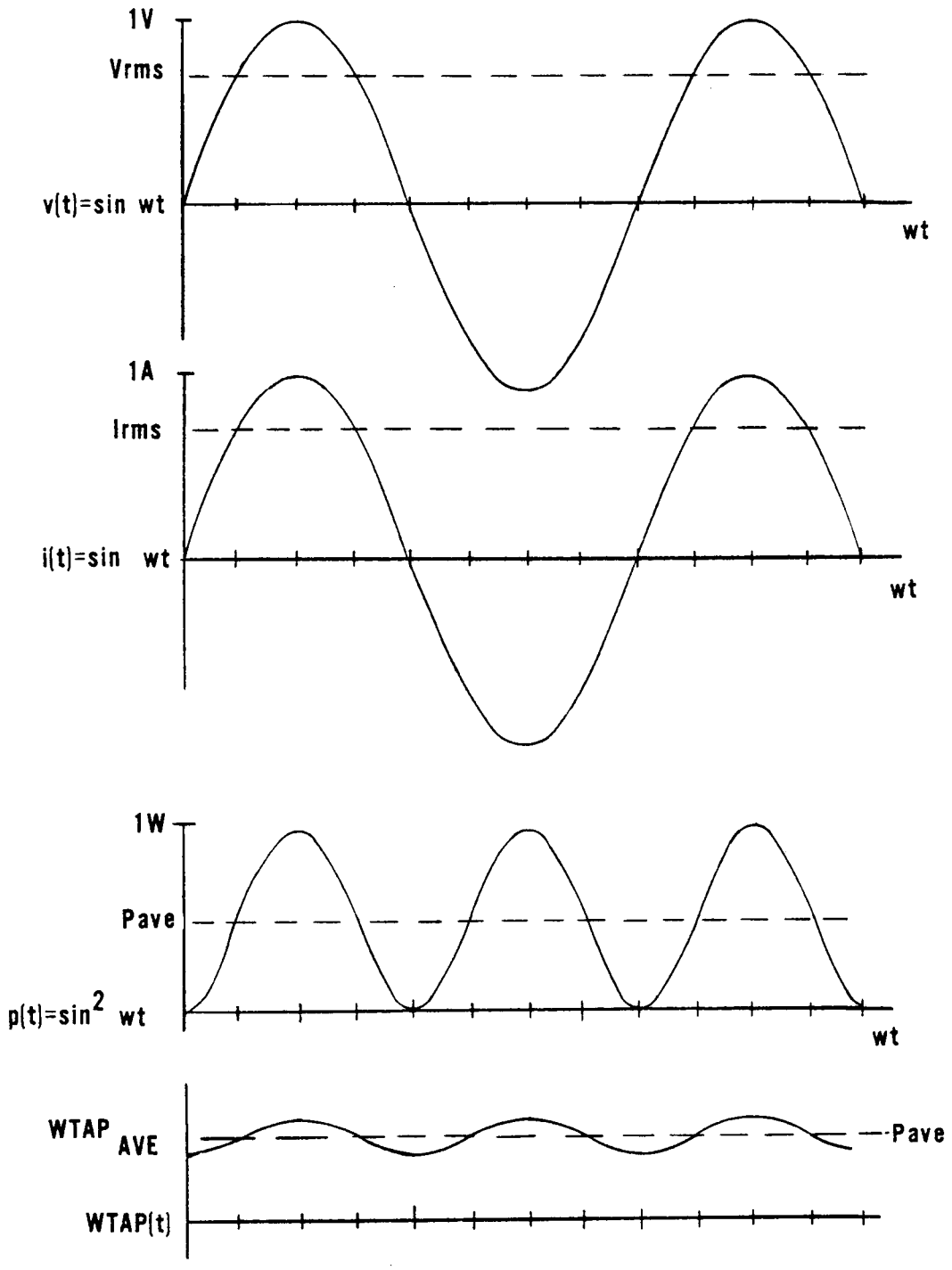


FIG. 9 REPRESENTATION OF VOLTAGE, CURRENT, AND POWER WAVEFORMS

the product of the root mean square (rms) voltage across a device and the rms current through it. All specifications of power in the CFTL test specifications are average power specifications. It is important to note that the instantaneous power varies by up to $\pm$100% about the value of average power 120 times a second.

Classically the average power is defined only under the condition of steady state current and voltage. During a transient, the average power cannot be defined. By definition the transient must be completed before the average power can be calculated. The problem this presents for closed loop control is the question of what should be used for the feedback signal. As previously discussed it makes no sense to try to control the instantaneous power nor can classical average power be used. The solution is to compromise and feedback a weighted time-averaged power (WTAP). WTAP is power which has been averaged over time with greater emphasis placed upon the more recent data. This can be accomplished with a low-pass filter. The time constant of the filter must be carefully chosen so that it is long enough to average power over several 60 Hz cycles and yet is short enough that it won't compromise controller performance during rapid transients. The time constant chosen for the CFTL controller is 100ms.

Just as with actual power there is an instantaneous WTAP as well as an average WTAP. Under steady state conditions the classical average power equals the average WTAP. The instantaneous WTAP varies by about 13% around the average WTAP with a time constant of 100ms and a power frequency of 120 Hz. Thus the CFTL requirement that the zone power be controllable to within 1% of setting must be interpreted to mean that

the average WTAP be within 1% of the requested classical average power under steady state conditions. Figure 10 shows the actual performance capability of the prototype controller for low power level requests. This figure shows the WTAP superimposed over the various setpoints. This figure demonstrates the controllers capability to fire SCR pairs in the proper sequence to assure that the average power corresponds to that requested by the setpoint.

2. Controller Bandwidth

As mentioned above an important initial consideration is to determine the bandwidth required for CFTL instrumentation and that required by the controller to generate fast transients. The bandwidth of the CFTL instrumentation is limited by the input filtering of the data acquisition system. These filters have a -3db point at 16 Hz. All planned power transients will be linear ramps. Assuming sinusoidal voltage, the instantaneous power delivered to a resistive load of one ohm is given by

$$p(t) = V^2 \sin^2 \omega_o t \ . \tag{3-1}$$

If this instantaneous power is modulated by a linear ramp,

$$r(t) = \frac{t}{T_r} \ , \tag{3-2}$$

then the modulated power can be expressed as

$$p_m(t) = r(t)p(t) \ , \tag{3-3}$$

$$= \frac{V^2 \ t \sin^2 \omega_o t}{T_r} \ . \tag{3-4}$$

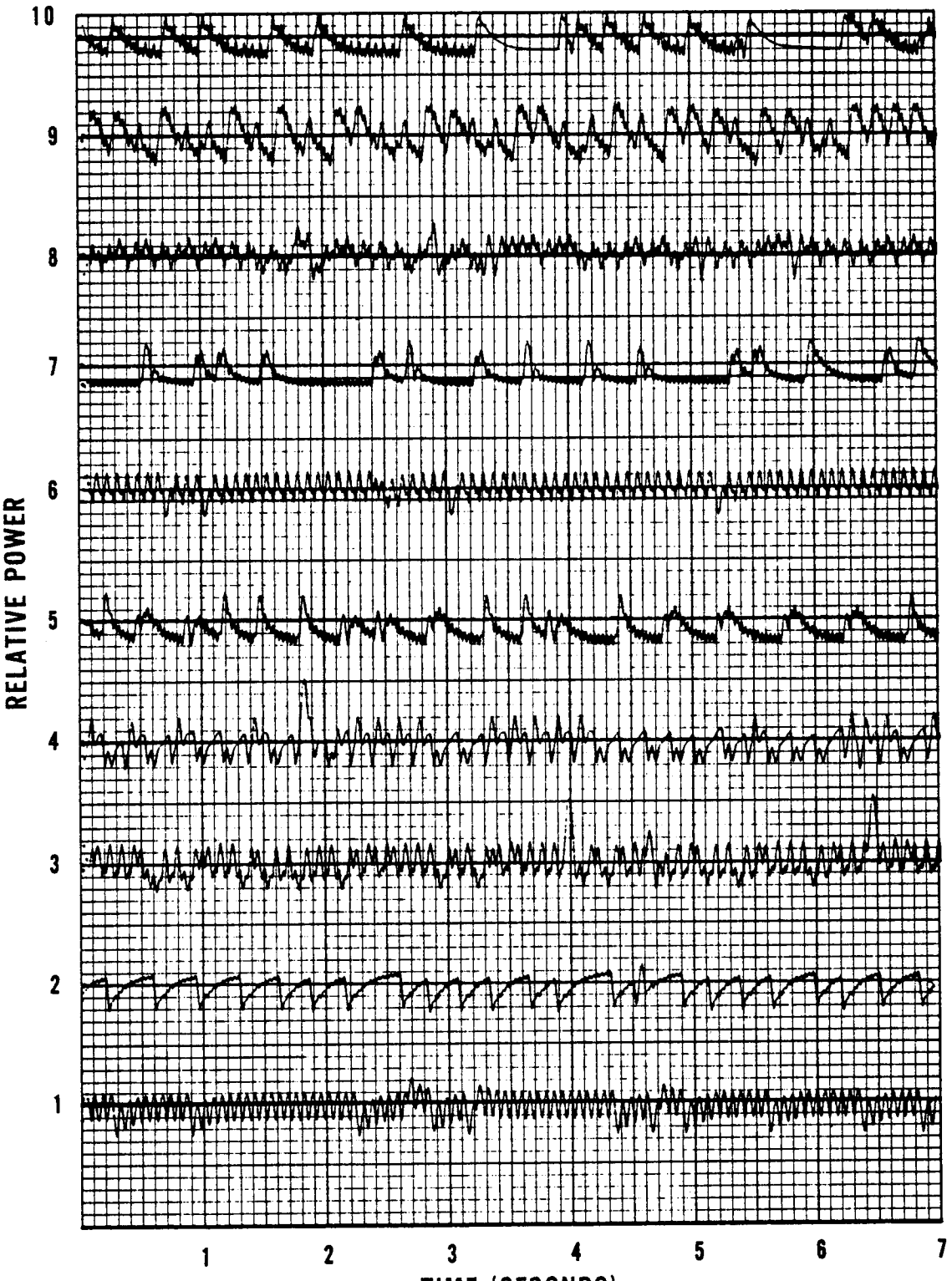


FIG. 10 MEASURED LOAD POWER (FILTERED) SUPERIMPOSED OVER SETPOINT

The Fourier Transform of this modulated waveform is given by

$$P_m(\omega) = \int_{-\infty}^{+\infty} p_m(t) e^{-j\omega t}\, dt \,. \tag{3-5}$$

If the linear ramp is allowed to last only from t = 0 to t = T_r, which corresponds to a ramp from zero power to maximum power, then $P_m(W)$ can be expressed as

$$P_m(\omega) = \frac{V^2}{T_r} \left[\int_0^{T_r} t \sin^2\omega_o t\, e^{-j\omega t}\, dt \right] , \tag{3-6}$$

$$P_m(\omega) = \frac{V^2}{2T_r} \left[\int_0^{T_r} (t - t\cos 2\omega_o t)\, e^{-j\omega t}\, dt \right] , \tag{3-7}$$

$$= \frac{V^2}{2T_r} \left[\int_0^{T_r} te^{-j\omega t}\, dt - \int_0^{T_r} t \cos 2\omega_o t e^{-j\omega t}\, dt \right] , \tag{3-8}$$

$$= \frac{V^2}{2T_r} \left[\frac{e^{-j\omega t}(-j\omega t - 1)}{-\omega^2} \Bigg|_0^{Tr} - \left(\frac{te^{-j\omega t}(j\omega \cos 2\omega_o t + 2\omega_o \sin 2\omega_o t)}{(-\omega^2 + 4\omega_o^2)} \right.\right.$$

$$\left.\left. - \frac{e^{-j\omega t}(-\omega^2 - r4_o^2)\cos 2\omega_o t - 2j\omega 2\omega_o \sin 2\omega_o t)}{(-\omega^2 \mp 4\omega_o^2)^2} \right) \Bigg|_0^{Tr} \right]$$

$$\omega \neq 0,\ \omega \neq 2\omega_o \,, \tag{3-9}$$

$$P_m(\omega) = \frac{V^2}{2T_r}\left[\frac{(j\omega t+1)(\cos\omega t-j\sin\omega t)}{\omega^2} - \frac{t(\cos\omega t-j\sin\omega t)(-j\omega\cos 2\omega_o t+2\omega_o \sin 2\omega o)}{-\omega^2 + 4\omega_o^2}\right.$$

$$\left. - \frac{(\cos\omega t-j\sin\omega t)((-\omega^2-4\omega_o^2)\cos 2\omega_o t-2j\omega 2\omega_o \sin 2\omega_o t)}{(-\omega^2+4\omega_o^2)^2}\right] \Bigg|_0^{T_r}$$

$\omega \neq 0,\ \omega \neq 2\omega_o$. (3-10)

$$\mathrm{Re}\{P_m(\omega)\} = \frac{V^2}{2T_r}\left[\frac{\omega t\sin\omega t + \cos\omega t}{\omega^2} - \frac{t\cos\omega t 2\omega_o \sin 2\omega_o t}{-\omega^2 + 4\omega_o^2}\right.$$

$$\left. + \frac{t\omega\sin\omega t\cos 2\omega_o t}{(-\omega^2 + 4\omega_o^2)} + \frac{\cos\omega t(-\omega^2 4\omega_o^2)\cos 2\omega_o t}{(-\omega^2 + 4\omega_o^2)^2} - \frac{4\omega\omega_o \sin\omega t\sin 2\omega_o t}{(4\omega_o^2 - \omega^2)^2}\right] \Bigg|_0^{T_r}$$

$\omega \neq 0,\ \omega \neq 2\omega_o$. (3-11)

$$\mathrm{Re}\{P_m(\omega)\} = \frac{V^2}{2T_r}\left[\frac{\omega T_r\sin\omega T_r+\cos\omega T_r-1}{\omega^2} - \frac{2T_r\omega_o\cos\omega T_r\sin 2\omega_o T_r}{4\omega_o^2-\omega^2}\right.$$

$$\left. + \frac{T_r\omega\sin\omega T_r\cos 2\omega_o T_r}{4\omega_o^2 - \omega^2} - \frac{(\omega^2+4\omega_o^2)\cos\omega T_r\cos 2\omega_o T_r}{(4\omega^2 - \omega^2)^2} - \frac{(\omega^2+4\omega_o^2)}{}\right.$$

$$\left. - \frac{4\omega\omega_o \sin\omega T_r\sin 2\omega_o T_r}{(4\omega_o^2 - \omega^2)^2}\right]$$

$\omega \neq 0,\ \omega \neq 2\omega_o$. (3-12)

$$\text{Im}\{P_m(\omega)\} = \frac{V^2}{2T_r}\left[\frac{\omega t\cos\omega t - \sin\omega t}{\omega^2} + \frac{t\omega\cos\omega t\cos 2\omega_o t}{(4\omega_o^2 - \omega^2)}\right.$$

$$+ \frac{2\omega_o t\sin\omega t\sin 2\omega_o t}{(4\omega_o^2 - \omega^2)} - \frac{4\omega\omega_o\cos\omega t\sin 2\omega_o t}{(4\omega_o^2 - \omega^2)^2}$$

$$\left. - \frac{(-\omega^2 - 4\omega_o^2)\sin\omega t\cos 2\omega_o t}{(4\omega_o^2 - \omega^2)^2}\right]\Bigg|_0^{T_r}$$

$$\omega \neq 0,\ \omega \neq 2\omega_o\ . \qquad (3\text{-}13)$$

$$\text{Im}\{P_m(\omega)\} = \frac{V^2}{2T_r}\left[\frac{\omega T_r\cos\omega t_r - \sin\omega T_r}{\omega^2} + \frac{T_r\omega\cos\omega T_r\cos 2\omega_o T_r}{(4\omega_o^2 - \omega^2)}\right.$$

$$+ \frac{T_r 2\omega_o\sin\omega T_r\sin 2\omega_o T_r}{4\omega_o^2 - \omega^2} - \frac{4\omega\omega_o\cos\omega T_r\sin 2\omega_o T_r}{(4\omega_o^2 - \omega^2)^2}$$

$$\left. + \frac{(\omega^2 + 4\omega_o^2)\sin\omega T_r\cos 2\omega_o T_r}{(4\omega_o^2 - \omega^2)^2}\right]$$

$$\omega \neq 0,\ \omega \neq 2\omega_o\ . \qquad (3\text{-}14)$$

$$\left|P_m(\omega)\right|^2 = \left(\text{Re}\{P_m(\omega)\}\right)^2 + \left(\text{Im}\{P_m(\omega)\}\right)^2 \qquad (3\text{-}15)$$

A normalized plot of the magnitude of this quantity is shown in Figure 11 for various values of T_r. The fastest anticipated power ramp in CFTL is 0 to full power in 1 sec. A bandwidth of 16 Hz would only allow 73% of the power transient information through. Thus the present

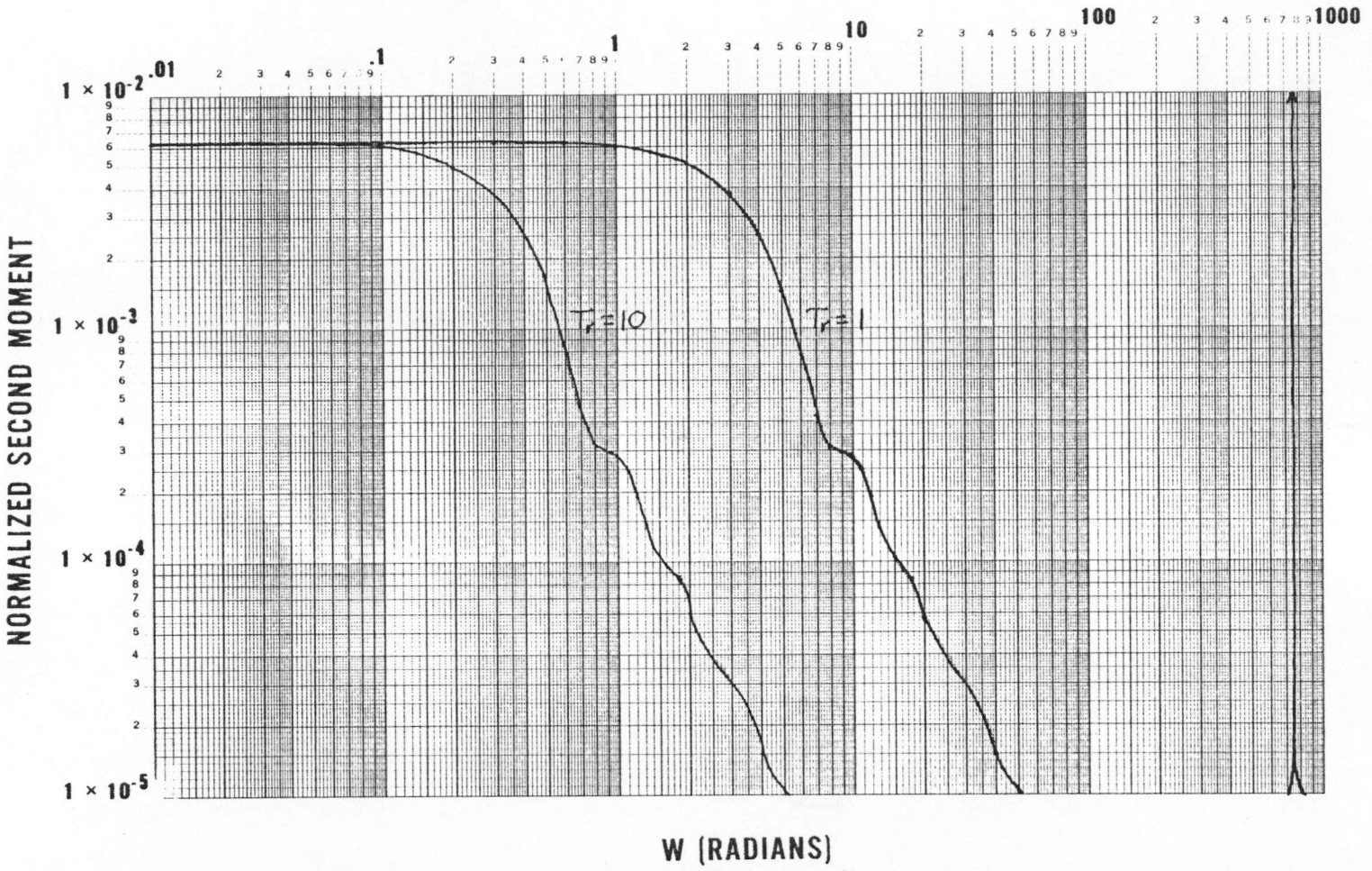


FIG. 11 SIGNAL BANDWIDTH OF LINEAR RAMPS MODULATING 120 HZ POWER SINUSOID

CFTL power measurement system, which has a 16 Hz low pass filter in the signal path, will not be able to accurately measure power during fast transients.

The instantaneous power is not however our signal of interest. We are interested in a linear power ramp. The equation of interest then becomes

$$p(t) = \frac{tV^2}{2T_r} . \tag{3-16}$$

$$P(\omega) = \frac{V^2}{2T_r} \int_0^{T_r} te^{-j\omega t} \, dt , \tag{3-17}$$

$$\text{Re}\ \{P(\omega)\} = \frac{V^2}{2T_r} \left[\frac{\cos\omega T_r - 1 + \omega T_r \sin\omega T_r}{\omega^2} \right] , \tag{3-18}$$

$$\text{Im}\ \{P(\omega)\} = \frac{V^2}{2T_r} \left[\frac{\omega T_r \cos\omega T_r - \sin\omega T_r}{\omega^2} \right] , \tag{3-19}$$

$$\left|P(\omega)\right| = \left(\frac{V^2}{\omega^2 2T_r} \cos^2\omega T_r - 2\cos\omega T_r + 2\omega T_r \cos\omega T_r \sin\omega T_r + 1 \right.$$

$$- 2\omega T_r \sin\omega T_r + \omega^2 T_r^2 \sin^2\omega T_r + \omega^2 T_r^2 \cos^2\omega T_r - 2\omega T_r \cos^2\omega T_r \sin\omega T_r$$

$$\left. + \sin^2\omega T_r \right)^{1/2} . \tag{3-20}$$

$$\left|P(\omega)\right| = \frac{V^2}{2\omega^2 T_r} \left[\cos^2\omega T_r + \sin^2\omega T_r - 2\cos\omega T_r + 1 - 2\omega T_r \sin\omega T_r \right.$$

$$\left. + \omega^2 T_r^2 (\sin^2\omega T_r + \cos 2\omega T_r) \right]^{1/2} \tag{3-21}$$

$$\left|P(\omega)\right| = \frac{V^2}{2\omega^2 T_r}\left(1-2\cos\omega T_r+1-2\omega T_r\sin\omega T_r+\omega^2 T_r\right)^{1/2} \quad (3\text{-}22)$$

$$= \frac{V^2}{2T_r\omega^2}\left(2(1-\cos\omega T_r-\omega T_r\sin\omega T_r) + \omega^2 T_r\right)^{1/2} \quad (3\text{-}23)$$

$$= \frac{V^2}{2T_r}\left[\frac{2}{\omega^4} - \frac{2\cos\omega T_r}{\omega^4} - \frac{2\omega T_r\sin\omega T_r}{\omega^4} + \frac{T_r}{\omega^2}\right]^{1/2} \quad (3\text{-}24)$$

The second moment of this quantity is given by

$$\left|P(\omega)\right|^2 = \frac{V^4}{4T_r^2}\left[\frac{2(1-\cos\omega T_r - \omega T_r\sin\omega T_r) + \omega^2 T_r^2}{\omega^4}\right] \quad (3\text{-}25)$$

A 16 Hz bandwidth will allow 99% of the ramp to pass undistorted. From the results of this discussion we have shown that, no EMI should be generated by the power supply below 16 Hz to keep noise out of the CFTL instrumentation system the CFTL power measurement system must increase its bandwidth, and the bandwidth of the controller itself should be 16 Hz to allow the 1 sec ramp to pass with less than 1% distortion.

3. The CFTL Power Distribution System

As presently planned the CFTL power supply will have a maximum operating power of 2.8 MW. It will be designed to potentially generate 6.5 MW. The total power distribution network has, as shown in Fig. 12, been divided into 13 equal parts. Each part consists of a motor driven induction regulator with an output voltage range of 45V to 375V. This regulator will drive one of the 13 Hudson multiple tap transformer/SCR systems previously described. The induction regulator will be used to set the maximum power which each section will dissipate in a given test.

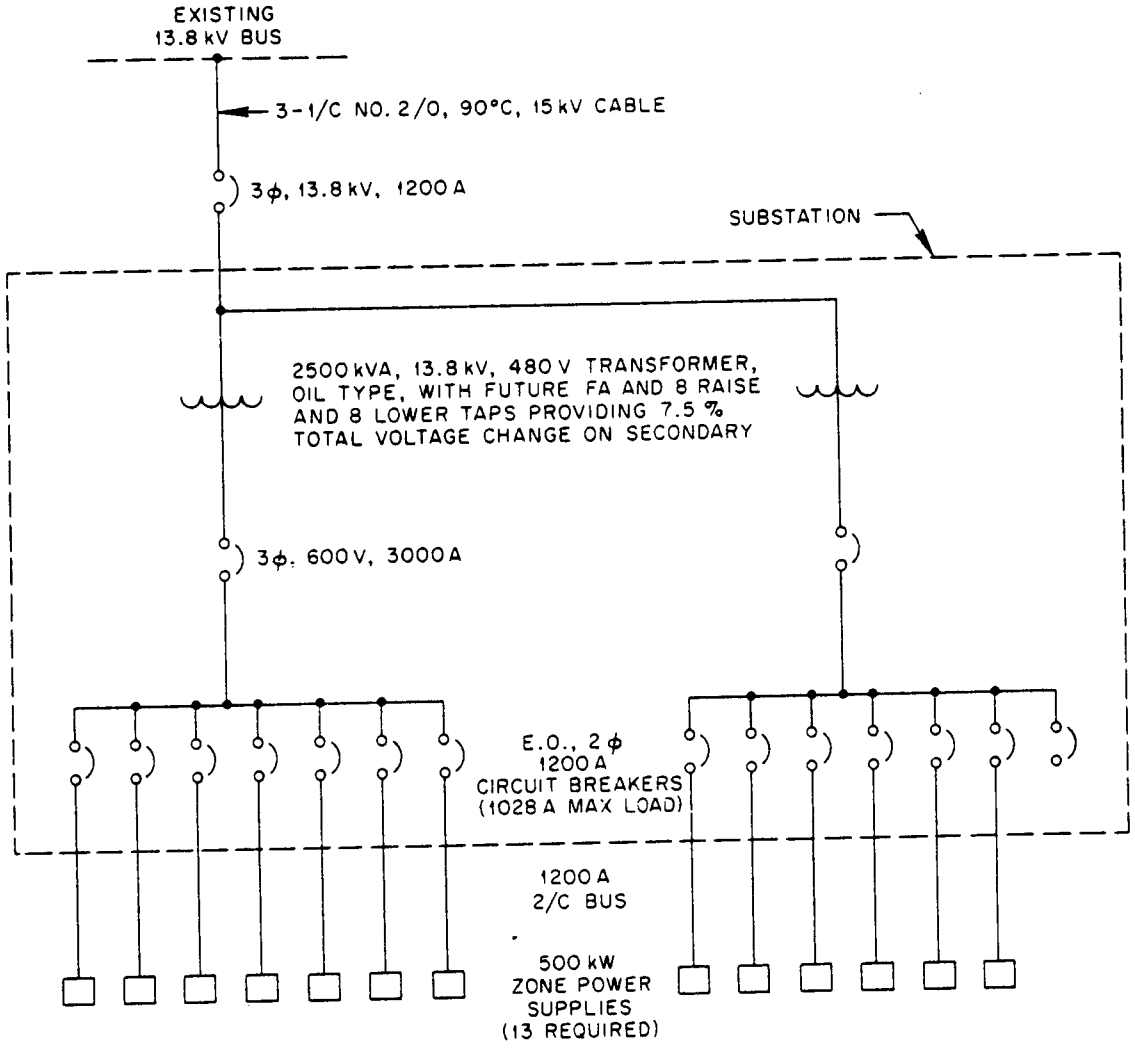


FIG. 12 CFTL POWER DISTRIBUTION NETWORK

Each section will handle a maximum of 500 KW and power one simulated bundle zone. The concept of a bundle zone is best explained by referring to Figure 13. This figure represents a 37 fuel rod bundle simulator. The unshaded circles represent 2 Ω resistive heaters. The shaded circles represent unheated bars that are part of the support structure of the core. The CFTL will have one such fuel bundle assembly. An actual Gas Cooled Fast Reactor however will consist of hundreds of these assemblies arranged in a hexagonal arrangement. The location of a particular assembly with respect to the center of the reactor will determine the neutron flux and power gradient across the assembly. By use of the induction regulators and the zone concept, various power gradients can be imposed across the CFTL fuel assembly similator. Thus the entire assembly can be powered uniformly or with any desired power gradient across it.

One of the CFTL test requirements demand a power gradient of 1% per zone across the entire assembly. This implies that the control of power must be much better than 1%. One of the problems involved in power control to this precision is that of actually measuring power to 1%. This is a particularly difficult problem in CFTL since the dynamic range of the power for any one bundle size can be as high as 900:1.

4. Power Feedback Considerations

There is a compromise which must be made in the zone power measurement scheme used for power feedback in CFTL. To demonstrate this point let's arbitrarily select zone 1 of Figure 13 for analysis. This zone has two fuel rod simulators in it. The most accurate method of

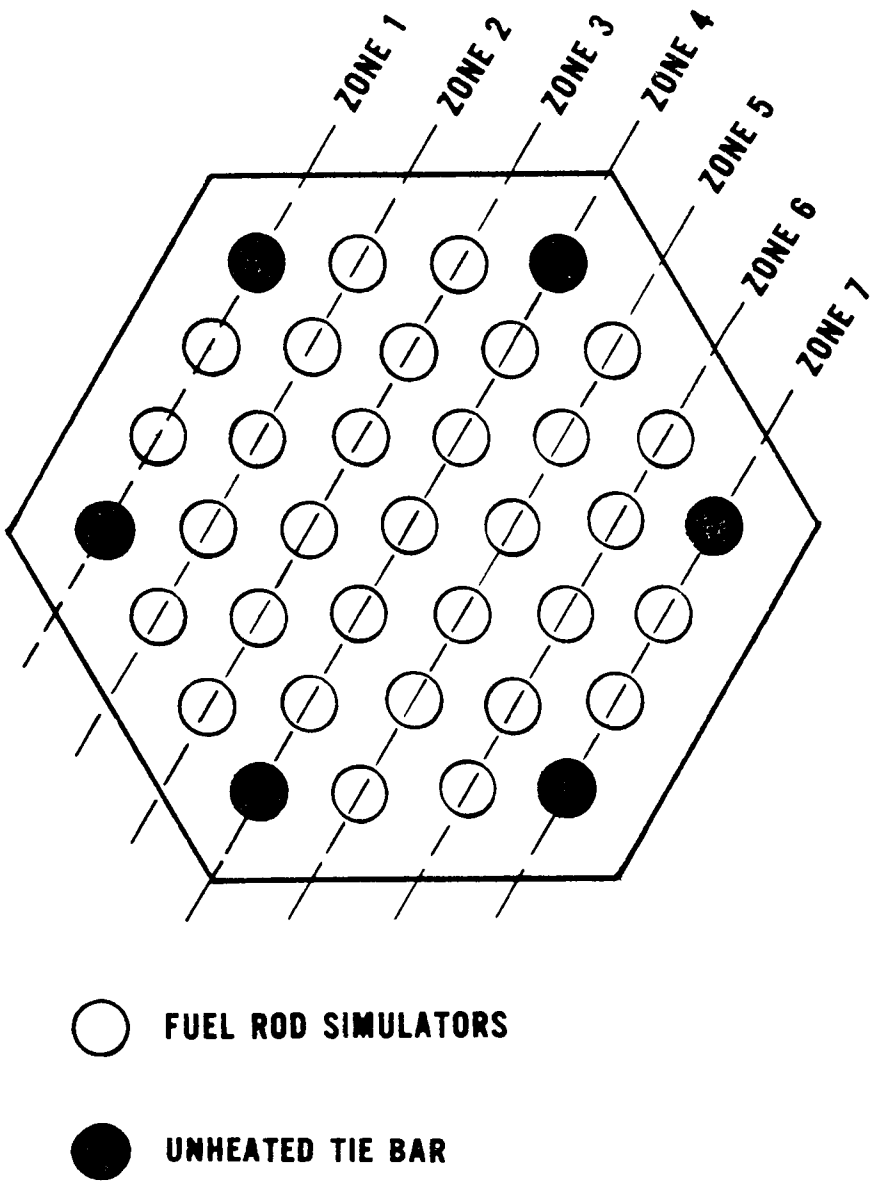


FIG. 13 ZONE PARTITIONING FOR 37 ROD BUNDLE

zone power measurement would be to measure zone voltage, total zone current and then multiply the two measurements to give instantaneous power. This value of power would then be filtered and used by the controller to keep the zone power at the desired set point. If one of the rods fails (opens), however, the controller will supply twice the desired power to the remaining rod (or saturate) to keep the total zone power at the required set point. The net result would be to generate thermal gradients near the failed rod which may compromize the mechanical integrity of the rods in the area. Such a rod failure would go undetected and could invalidate a data run as well as damage the bundle.

Another problem with feeding back true zone power is that as the induction regulator voltage is varied to set up a new value of maximum power for the zone the feedback and setpoint signals are no longer properly scaled. For instance if the inductance regulator voltage is lowered to change the zone power from 90KW to 45KW then the setpoint would have to be halved to get the same percent of full scale as before. This would result in cumbersome gain adjustments in CFTL where the induction regulators can be arbitrarily set.

A final problem with this feedback scheme is that each zone controller would be adjusted specifically for its own zone. Remember some zones will have only two fuel rod simulators while others could have as many as eleven. Thus the setpoint and feedback gains will be set specifically for the zone the controller is assigned to. One of the CFTL requirements is that any zone power supply shall be able to power any zone during the life of the loop. This last limitation of true

power feedback prevents the complete interchangeability of zone supplies since again the gains will have to be individually adjusted to match the load. These limitations can all be circumvented through the use of a pseudo power feedback signal and the concept of relative feedback.

Instead of feeding back zone power, consider feeding back zone voltage. Assume all resistances would remain constant (the fuel rod simulators' resistances are designed to be constant to within 1% over their operating temperature range). If the voltage measurement is squared by the controller and this value is used as the feedback signal irregardless of the actual load in any zone then the feedback signal would not be actual power but rather some pseudo power. Therefore again referring to Fig. 13 with 300V across both zone 1 and zone 3 both zones would be feeding back the same power indication to their controllers. Assume 300V is the voltage of tap 15. Then both zone feedback signals would be indicating that 100% of the available zone power is being dissipated by the load. At 150V both indications would be that 25% of the available zone power was being dissipated, even though zone 3 was dissipating 3 times the power of zone 1. There are several advantages to this scheme. First no controller gains will have to be manually adjusted to account for the different loads in each zone. Therefore the controllers will be completely interchangeable. Second, if a rod fails open in a zone the power to the remaining rods will be kept the same. The temperature gradients around the failed rod will not be increased by the control action. Finally the range over which the controller will have to measure power will be minimized. For instance in some bundle designs a 500:1 power range will be required to complete all tests. If

we assume that some one power measurement circuit will be used for all the controllers then at maximum power a true power measurement of zone 3 power would be 3 times higher than that measured at zone 1. Therefore the power measurement circuit would have to be able to accurately measure power over a 1500:1 power range. This requirement is not necessary with voltage feedback.

Another option is zone current feedback but it is not desirable since a failed rod with this scheme would produce the same effect of aggravated thermal gradients as the true power feedback scheme does.

A final option is to feedback the actual power in a single rod and assume the other rods are behaving in the same manner. The biggest problem with this scheme is that if the rod that is instrumented fails then all control of a zone is lost.

The Control Scheme

The technique chosen for control of the Hudson linear multipower level (LMPL) system incorporates elements from linear control theory and digital signal processing to form a hybird analog/digital controller of high performance and versatility.

The scheme involves using analog signal conditioning to generate a driving signal for firing the SCR pairs for closed-loop control and digital signal processing for decoding the driving signal, and for open-loop control.

A simplified block diagram of the controller is indicated in Figure 14. The analog portion of the controller includes signal conditioning for the pseudo-power feedback signal, comparison of the feedback signal

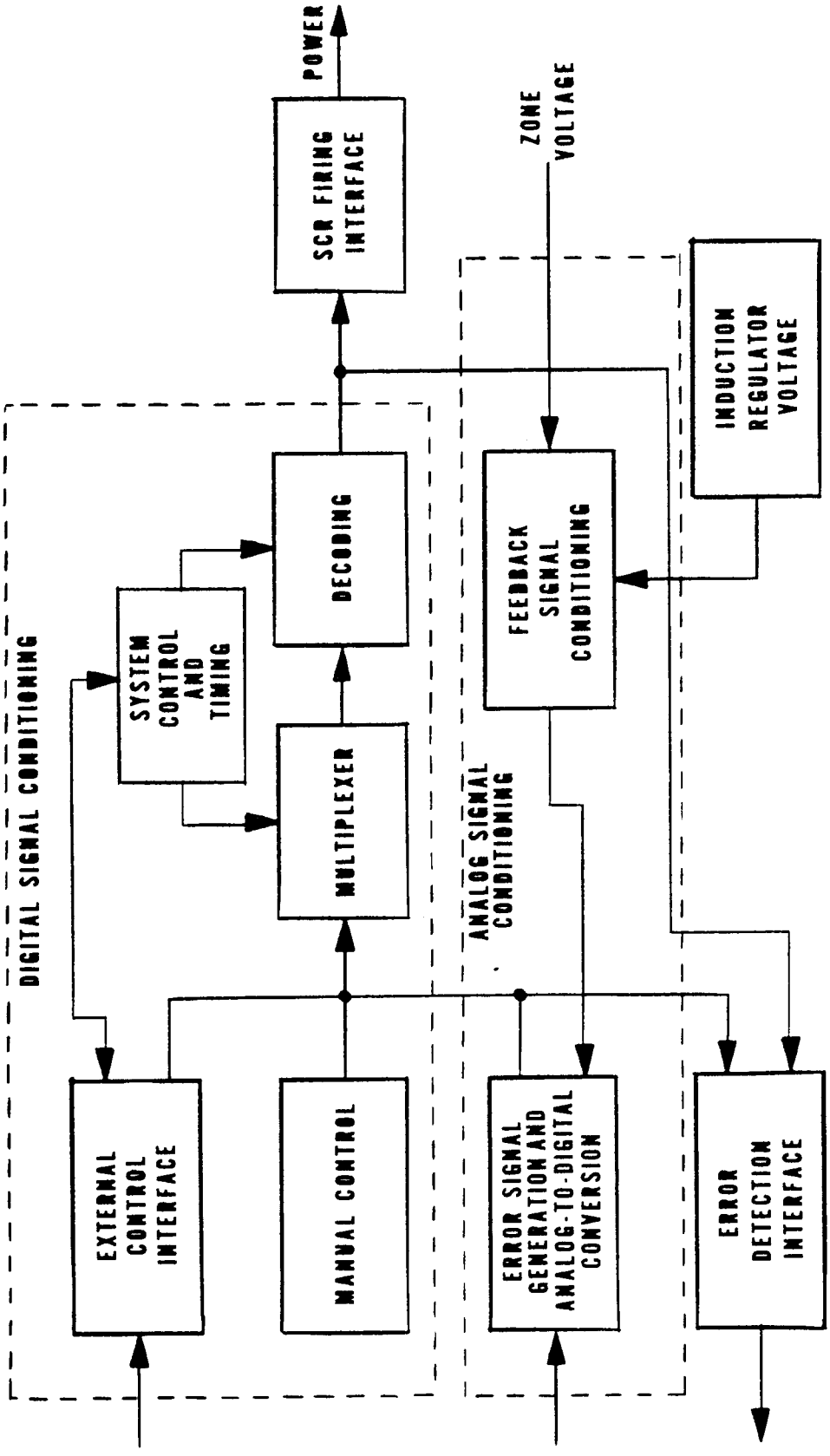


FIG.14 SIMPLIFIED BLOCK DIAGRAM OF CONTROLLER

with the setpoint, and conversion of the amplified error signal into a digital format. The digital portion of the controller includes the multiplexing, decoding and timing circuits necessary for proper firing of the SCR network.

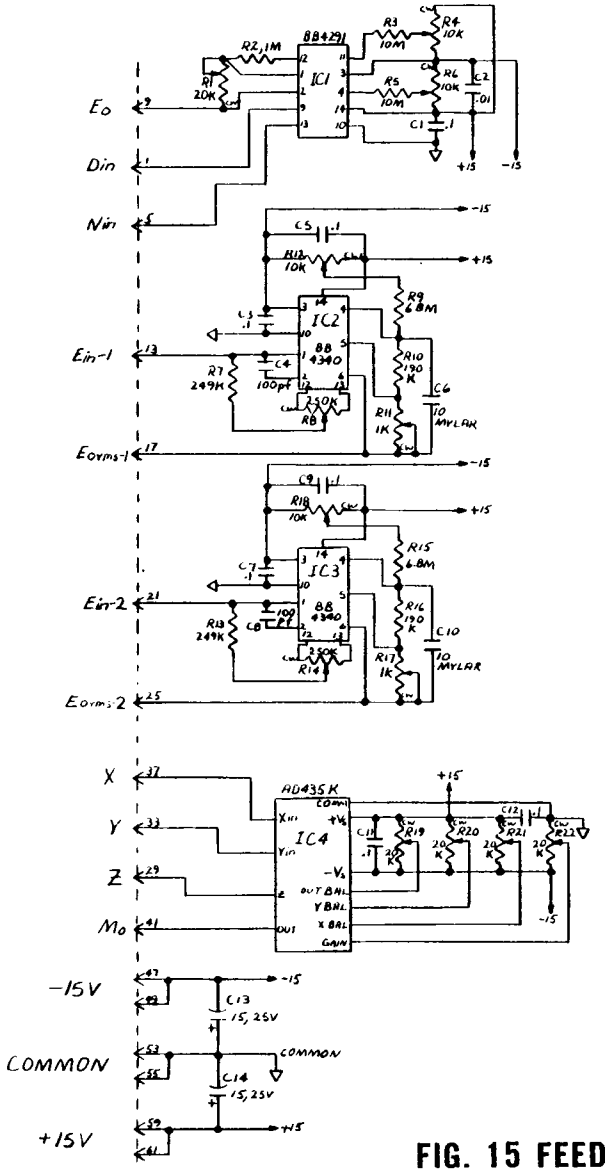
1. Circuits

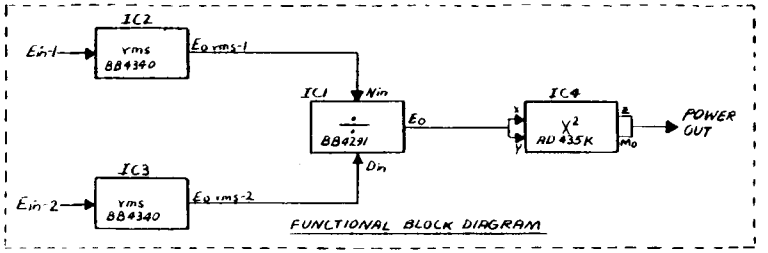
a. Analog Signal Conditioning

The analog portion of this controller incorporates some features which make it particularly suitable for the intended CFTL application. A clever scheme had to be devised to handle the feedback signal in such a way that any controller could be used in any zone without modification or adjustment and the controller had to operate correctly without adjustment irrespective of the induction regulator voltage (which could be set to any voltage over a 8:1 range from 375 V to 45 V).

i. The Feedback Signal Conditioner

As explained in an earlier section, measurement of zone voltage to derive a pseudo-power feedback signal offered the best choice for both versatility and bundle integrity. In addition this choice lends itself to an easy implementation of relative power control independent of the induction regulator setting. Figure 15 details the circuitry involved for relative power control. Voltage dividers and op-amp buffers will scale both the measured load voltage and the induction regulator voltage and deliver these signals to this circuit. As indicated in the functional block diagram of the figure, these signals will be converted to rms values and then input to the divider module. The proportional to output of the divider will





NOTES:
1. ALL FIXED RESISTORS IN OHMS AND ARE 1% METAL FILM.
2. ALL POTENTIOMETERS ARE HELITRIM SERIES 76.
3. ALL CAPACITORS IN MICROFARADS UNLESS NOTED OTHERWISE.

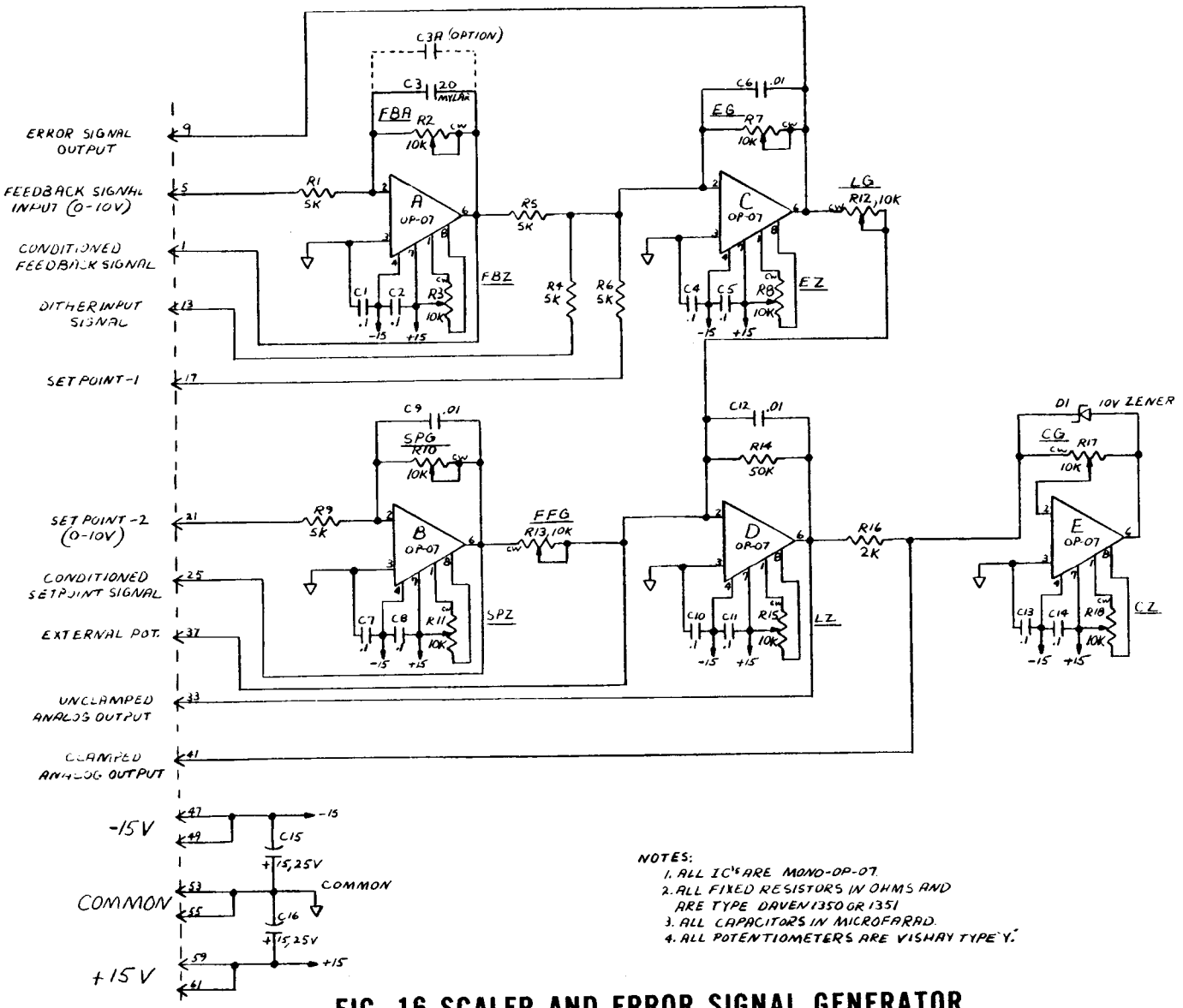
FIG. 15 FEEDBACK SIGNAL CONDITIONER

be the measured zone voltage divided by the induction regulator voltage. The divider module assures that the controller is controlling relative to the induction regulator setting. Therefore for any setting of the induction regulator the controller will assume tap 15 will give 100% of the desired power and will always allow power control using all 15 taps. If this feature were not included, then when the induction regulator were adjusted to give 1/2 of the maximum operating power the controller could only control seven SCRs and consequently decrease the power resolution. The disadvantage of this scheme is that the controller will not be able to correct the power delivered to the load if the line voltage changes (i.e., induction regulator voltage varies); however, since the induction regulator is designed to maintain a regulated output irrespective of line variations, this is not considered to be a major drawback.

ii. Scaling and Error Signal Generation

The remaining portion of the signal conditioner involves scaling the feedback signal for proper comparison with the input set-point and amplification of the resulting error signal (see Fig. 16). The output of this circuit is the set-point modified by the error signal. The advantages of this scheme are discussed in the following chapter.

There is also a voltage clamp in the circuit. This is for the prototype models only. Since the multitapped transformer with 16 taps has not yet been constructed, all prototypes have



NOTES:
1. ALL IC'S ARE MONO-OP-07.
2. ALL FIXED RESISTORS IN OHMS AND ARE TYPE DAVEN 1350 OR 1351
3. ALL CAPACITORS IN MICROFARAD.
4. ALL POTENTIOMETERS ARE VISHAY TYPE 'Y'.

FIG. 16 SCALER AND ERROR SIGNAL GENERATOR

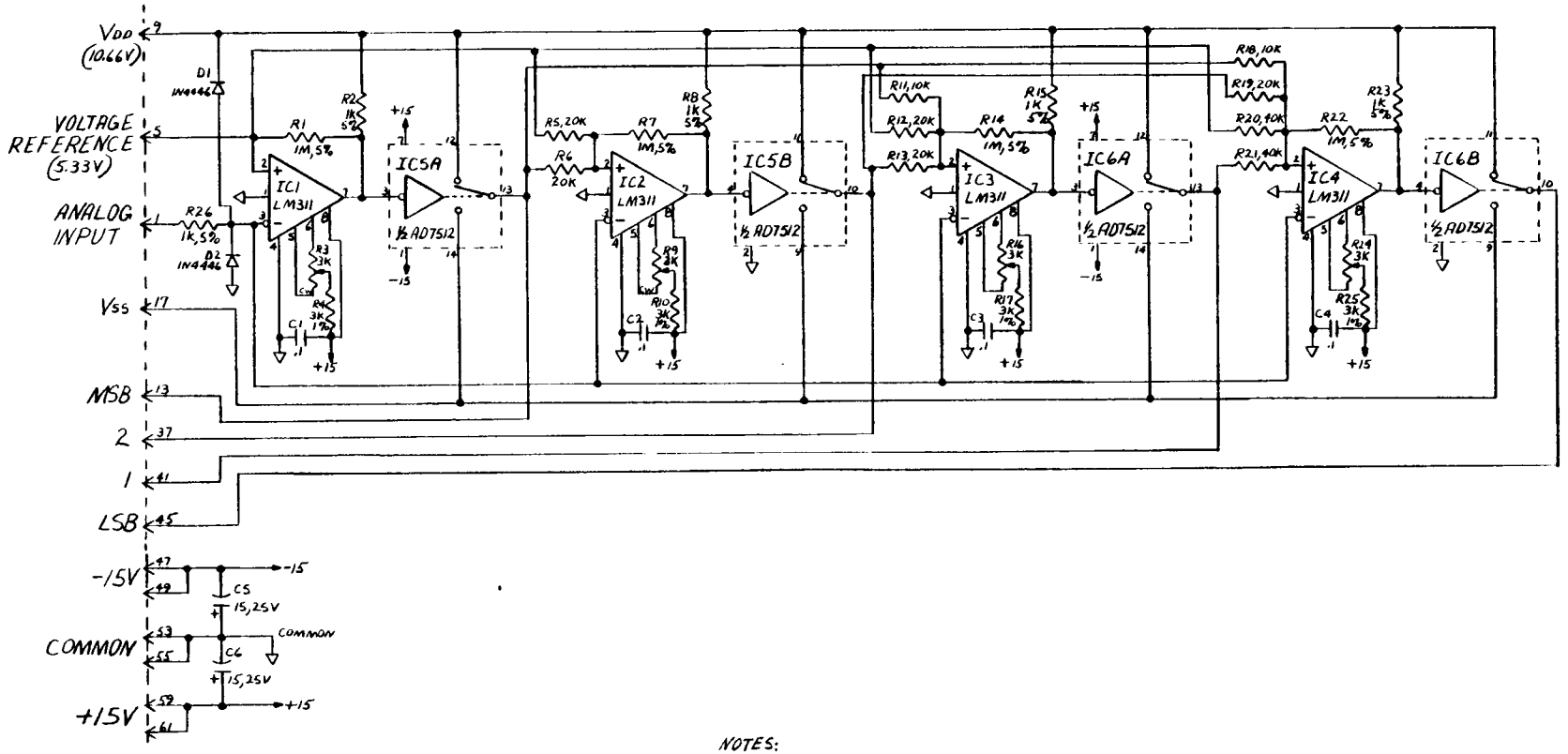
worked with only a few taps. The clamp prevents the error signal from demanding a tap which is not available on the prototype.

iii. The Strobeless Analog to Digital Converter

The analog error signal is next directed to an analog to digital converter (Fig. 17). Since there are sixteen available power steps a four bit ADC is adequate for this application. The circuit is based upon one by A. H. Kitai[4] and has been modified for improved performance. The circuit uses a network of resistors, comparators, and C-MOS analog switches to offer a continious digital representation of the analog input. Table 3.1 summarizes the four comparators' input at the sixteen analog values for which the digital code changes. This circuit is a potential weak link in the controller performance due to the fact that the digital code may be invalid in the vicinity of code transitions. However at this time there is no indication that controller performance is being compromised by this possibility.

b. Digital Signal Conditioning

The digital portion of this circuit controls which of three operating modes the controller will be in; manual operation, automatic closed-loop operation, or external control operation. Control lines determine which mode will be multiplexed into the decoding and SCR firing circuitry.



NOTES:
1. ALL FIXED RESISTORS ARE DAVEN TYPE 1351 EXCEPT AS NOTED.
2. ALL POTENTIOMETERS ARE HELITRIM SERIES 76
3. ALL CAPACITORS IN MICROFARADS.
4. LOW INPUT TO AD7512 CONNECTS OUTPUT SWITCH AS INDICATED HERE.

FIG. 17 STROBELESS ANALOG TO DIGITAL CONVERTER

TABLE 3.1

THRESHOLD LIMITS AND OUTPUT CODE OF ANALOG TO DIGITAL CONVERTER

THRESHOLD		OUTPUT
below	0.6667	0000
	0.6667	0001
	1.3333	0010
	2.0000	0011
	2.6667	0100
	3.3333	0101
	4.0000	0110
	4.6667	0111
	5.3333	1000
	6.0000	1001
	6.6667	1010
	7.3333	1011
	8.0000	1100
	8.6667	1101
	9.3333	1110
	10.0000	1111

i. Mode Selection and Decoding Logic

At this point we have explained the technique by which a four bit code has been determined to turn on one of the fifteen SCR pairs for automatic closed loop power control. However in an application as complex as this one several other modes of operation are also desirable. A particularly attractive mode is a manual mode. In the manual mode an operator would be able to turn on any individual SCR pair to verify their proper operation as well as the operation of instrumentation in that zone (thermocouples, power measurement devices, alarms, strain gages, etc.). Another attractive mode is an auxilliary control mode. In this mode some other master controller such as the loop computer would be able to take over zone power control. This would be necessary in some emergency scram situations where perhaps the flow of helium coolant and the total bundle power have to be precisely controlled together to avoid bundle damage.

Both of these additional operating modes have been incorporated into the design along with the automatic closed-loop control mode. Figure 18 shows the circuit implementation required for the selection and multiplexing of these three operating modes.

ii. Timing and Control Logic

The timing and decoding circuit controls which SCR will turn on and assures that the command to turn on occurs at the zero-crossing point of the waveform. There are two major

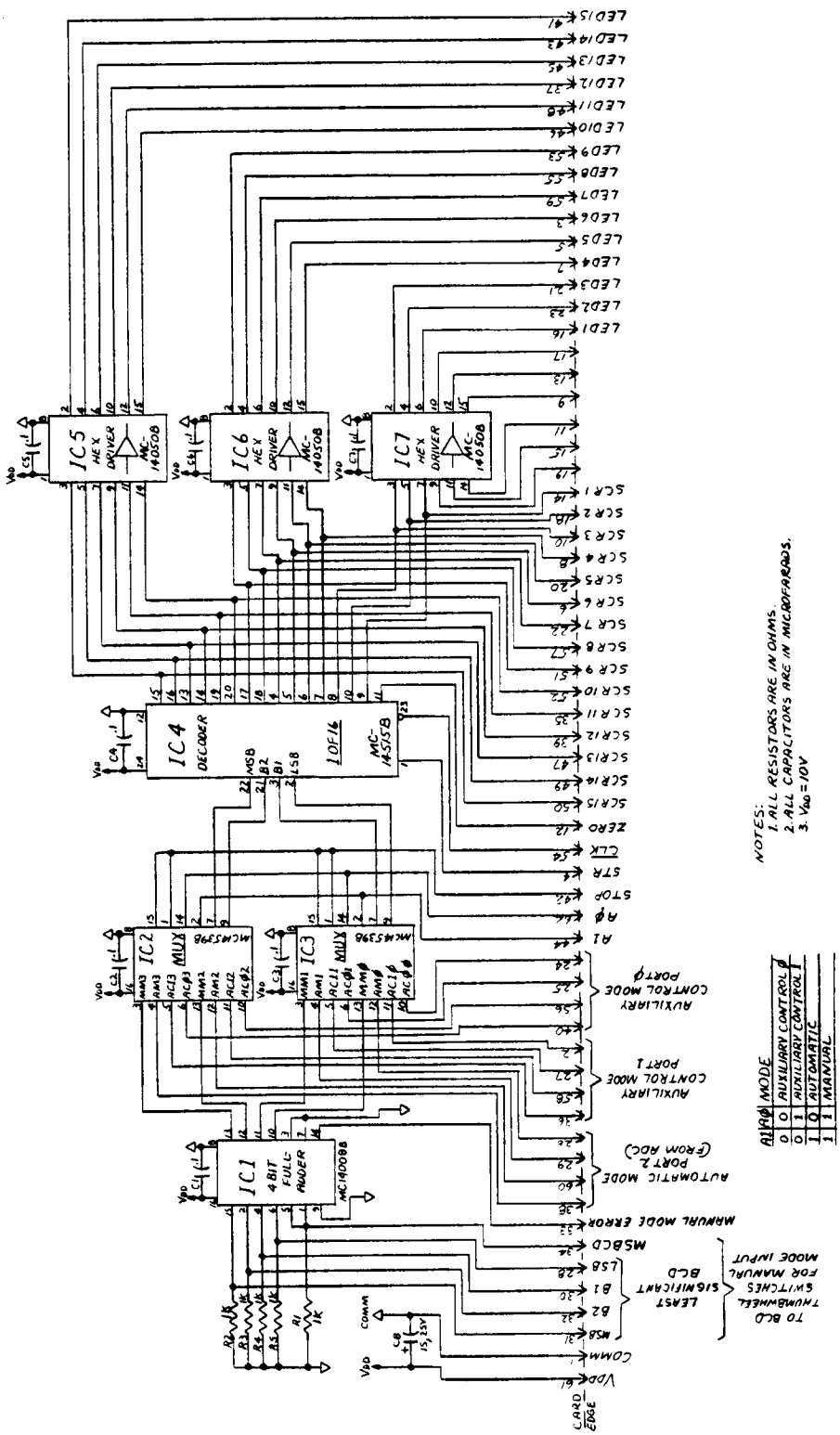
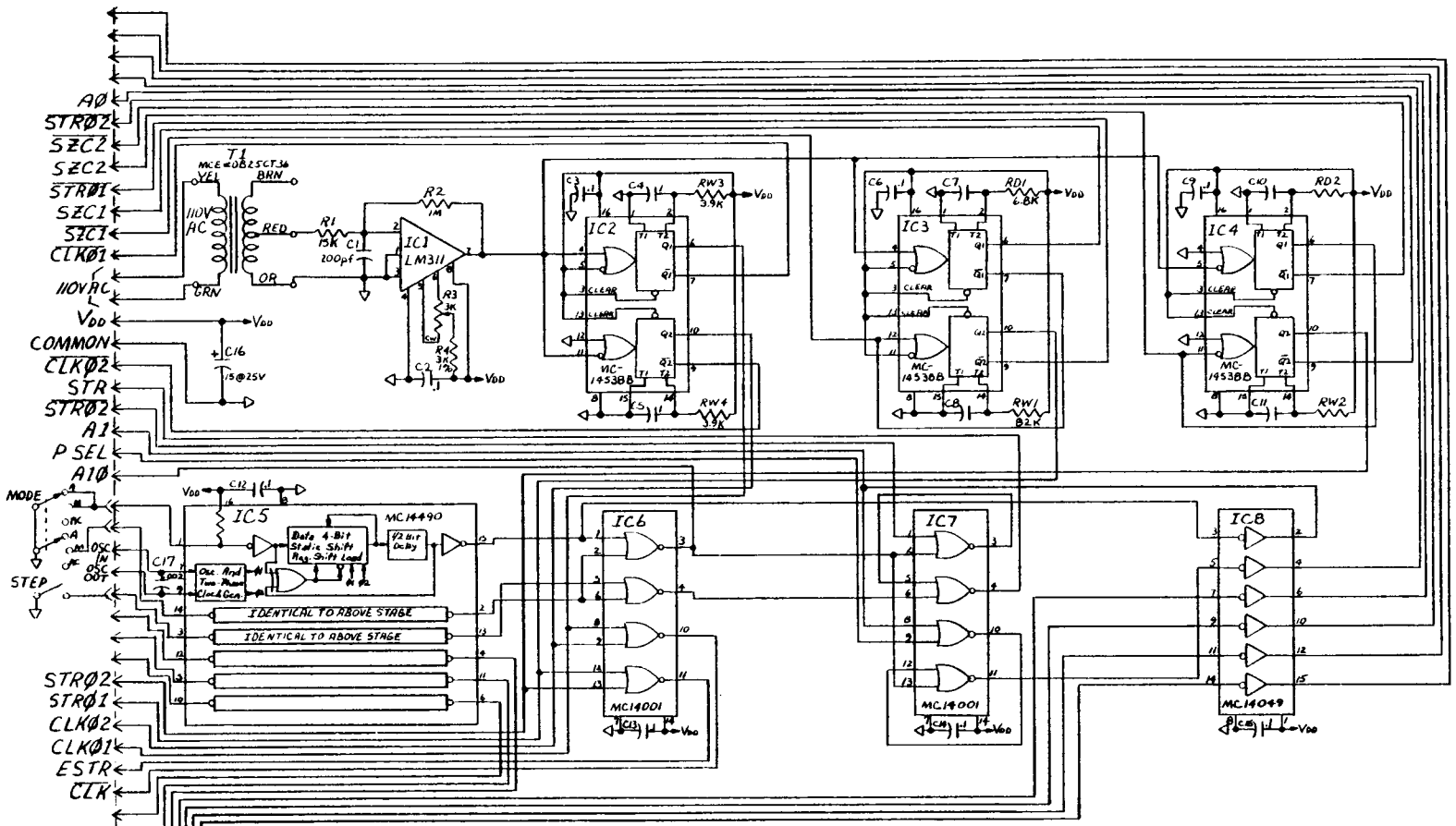


FIG. 18 MULTIPLEXER AND DECODER

timing signal pulses used by the controller; the "clock" pulse (CLK) which occurs for each zero crossing of the voltage waveform and the strobe pulse (STR) which controls when during the power waveform the error signal from the ADC will be latched into the decoder.

The clock signal is derived from the 60 Hz ac power lines. Since three phase power will be used in CFTL and each zone uses only one of these phases care must be used to assure that the phase used to derive the clock signal corresponds to the phase of the zone voltage controlled by the zone power controller. The circuit from which this signal is derived is shown in Figure 19.

The precise occurance of the strobe pulse may seem arbitrary but there are many design criteria which enter into its selection. The best time to generate the strobe pulse is when the power waveform is at the value corresponding to its average value. This value occurs four times during each voltage cycle. The selection of which of the four occurances to choose can be based upon noise considerations. If a noise signal causes the premature generation of a strobe pulse then incorrect data will be latched into the decoder. If this occurs before the true strobe pulse then the bad data will be replaced by the correct values. If the noise pulse occurs after the true strobe pulse then the bad data will be decoded and output to the SCR pairs. A further consideration is that the longer the capacitor in the feedback network has to charge



A=AUTOMATIC		M=MANUAL	P=PREPROGRAMMED
$\overline{A1Ø}$	0	0	1
$\overline{AØØ}$	1	0	1
A1Ø	0	1	0
A1	1	1	0
AØ	A1Ø	A1Ø	$\overline{PSEL}$
STRØ2	ENABLED	DISABLED	ENABLED
PSEL	DISABLED	DISABLED	ENABLED
STR	STRØCLOCK	STEP	STRØ CLOCK
STEP	DISABLED	ENABLED	DISABLED

NOTES:
1. ALL RESISTORS ARE IN OHMS.
2. ALL CAPACITORS ARE IN MICROFARADS. UNLESS NOTED OTHERWISE.
3. POTENTIOMETERS ARE HELITRIM SERIES 76.
4. V_{DD}=10V.
5. 14538 TIMING FORMULA
$PW(SEC) = R_{\Omega} C_f$
FROM 1μs TO ∞

FIG. 19 TIMING AND CONTROL LOGIC

or discharge the closer the sampled data will reflect the error signal due to the last voltage cycle. This implies that the latest occurrance of the average value would correspond to the best point to sample the error signal.

A final consideration must be included. Since the signal which is fed back to the controller is not instantaneous power but rather average power, then the phase shift of the averaging network must be taken into consideration. For this circuit the phase shift in the power waveform is 90°.

The strobe pulse should occur only once during a 60 Hz cycle so that the same data is used for both halves of the waveform, to maintain the symmetry of the waveform in order to keep d.c. currents out of the transformer. The circuit which generates the strobe pulse is also shown in Figure 19.

2. Failure Mode Analysis

A major concern in the power controller design is the ramifications of controller error or failure. An error in the controller output might result in a variety of serious occurances varying from blowing a fuse to degrading a zone transformer. A blown fuse will be expensive to find and replace in this system and might also nullify the entire test which was occuring when the fuse blew. Degradation of a zone transformer may be more subtle yet may have serious impact on the life of the CFTL loop which must operate continuously for over three years. The possible sources of system error or failure are listed in Table 3.2. They include noise, and chip failure, as well as firing circuit failure, SCR failure and induction regulator failure. The former two sources of

TABLE 3.2

A FEW SOURCES OF BUNDLE POWER SYSTEM FAILURE

Controller Error or Failure Sources

1. Noise
    a. Radiated
    b. Conducted
        i. Through Power Leads
        ii. Through SCR Firing Circuit Leads
2. Power Supply
    a. Drift with Temperature
    b. Loss of Regulation
    c. Power Failure
3. Integrated Circuits
    a. Oscillations
    b. Saturations
    c. Stuck bits

Other Failure Sources

1. Fuel Rod Simulators
2. SCR's
3. Transformers
4. Induction Regulator Motor Failure
5. Premature Fuse or Breaker Trip

problems fall within the realm of controller design while the later three sources are being monitored by, and controlled by other devices.

Each source of error or failure which might occur within the controller will be discussed at length along with the possible consequences and solutions to minimizing any detrimental results of their occurences.

a. Noise

The CFTL environment will be extremely electromagnetically noisy. The presence of arc welders, phase-fired SCR controllers and even the 6 MW power supply itself will all contribute to a broad spectrum of electromagnetic interference. The power line into the controller will first pass thru a line filter with 80 db attenuation to 1 GHz. This will minimize EMI entering thru the power leads. The controller will be housed in a metal cabinet which will be grounded to minimize the effects of radiated EMI. In addition CMOS logic is being used at a positive logic level of 10 V. This gives a noise immunity of nearly 5 V. As an added precaution, the circuit timing signals are staggered so that a noise pulse must occur simultaneously on both clock lines STR and CLK to result in an error at the output.

b. Chip Failure

There are three main subsystems in the CFTL controller. They are the analog signal conditioner, the analog to digital converter, and the digital signal conditioner.

i. The Analog Signal Conditioner (ASC)

The Analog Signal Conditioner will most likely fail in one of the following ways: one of the operational amplifiers or

analog function modules will saturate to one of the supply rails, or one will break into high frequency oscillation. In either case the control loop will no longer function. By monitoring the error signal such a condition could be detected and the system shut down. Since the error signal should never exceed a certain threshold, a comparator set above that threshold would detect system failure, safely shut down the system and notify the operator of its response. The concept of a safe shutdown will be discussed at the end of this chapter.

ii. The Analog to Digital Converter (ADC)

A failure in the ADC subsystem would manifest itself as one or more of its four bits being stuck in either the 1 or 0 state or as ripple through errors due to an odd to even number transition. A ripple through transition error such as a transition of 011 to 100 having an intermediate state of 000 would last only one cycle and will be compensated for by the controller action the next cycle. Stuck bits would result in large error signals which the previously discussed error signal monitor would detect, shut the system down and notify the operator.

iii. The Digital Signal Conditioner (DSC)

The Digital Signal Conditioner is by far the most critical subsystem in the controller from a failure analysis point of view. All safety action is sent to the DSC and a chip failure here would result in the safety action being ignored. The DSC handles digital data from three sources; the manual mode

digital data source, the automatic mode digital data source and the auxiliary control mode digital data source. An error in the manual mode digital data will be transmitted through the device. However a display on the operators panel will indicate which SCR was turned on and the operator can check his dialed setting with the indicator and can observe any discrepancy. It is tacitly assumed that the operator closes the loop in the manual mode.

The automatic mode digital data comes from the ADC and ASC boards and errors in this mode have already been discussed.

The external control mode digital data is more difficult to analyze. If the auxiliary controller is programmed incorrectly or if its output bits get stuck in one or the other logic state then this error will not be detected by the controller circuitry. The operator will not be able to detect the error on the indicator panel unless all the bits were simultaneously stuck either on or off. However since the preprogrammed transients will be used only for transients of a few seconds, the operator may not note the failure until so informed weeks later by the analytical group analyzing the transient results. If the error in the digital data occured in circuitry following the interface then a comparison of the controller output code with that of the auxiliary controller data would detect the error and could shut down the system.

If a chip fails in the multiplexing and decoding portion of the DSC then the controller will become dangerous to the

loop. Possible failures include having an output bit stuck in the one state at the output of the multiplexer as well as a bit stuck low at the output of the decoder. In either case the controller could no longer control the zone power.

The consequences could be disastrous. For instance during a design basis depressurization accident, the helium coolant is diverted from the core and the power is ramped down. If a zone fails to respond to a command to ramp down and is stuck at full power then when the coolant is lost, the fuel rod simulators (FRS) will burn up. Each FRS cost approximately $10K. If the SCR firing circuit is designed to be edge triggered rather than level triggered then the SCRs will not be turned on as a result of a stuck bit at the output of the decoder. Further, the power supply could be turned off by the controller if a DSC failure was detected by stopping the system clock. This would mean that no condition could exist where the controller could not shut the system down. And the design would be fail-safe.

Safe Shutdown

Because of the complexity and expense of the components involved in CFTL, any change in operating conditions must be coordinated with the change of several parameters. Thus the shutdown of CFTL power has to be choreographed with the control of several flow valve movements to assure that no thermal shocks are introduce to the core or the loop heat exchanger.

As discussed previously some controller failures are catastrophic and only by interrupting the clock can the power be shut off. This is the most dangerous of the controller failures and the only recourse is to shut the power down and send a shut down command to the helium control valves. It is hoped that hydraulic actuated valves will be used and that the flow can be shut off in a fraction of a second. In the case where perhaps the analog portion fails, an external scram can be executed through the auxilliary control mode to ramp the power down with helium flow. The problem becomes how to determine what failure mode the controller is in at any given time.

An SCR Firing Circuit

As discussed previously it is important that the SCR firing circuit be triggered by edge-sensitive circuitry rather than level-sensitive circuitry. The reason being that by removing the clock signal the entire power supply could be shut off. Otherwise a condition could exist where no control of the power supply could be executed by the controller.

One possible firing circuit is shown in Figure 20. This circuit employs a pulse transformer to provide both the required edge-triggered capability plus isolation from the high SCR cathode voltages. By judicious choice of the primary to secondary turns ratio and the proper selection of hold down resistance R, an SCR turn on pulse can be generated which can be triggered only by receiving a pulse input. The hold down resistor also serves as a low impedance between the normally

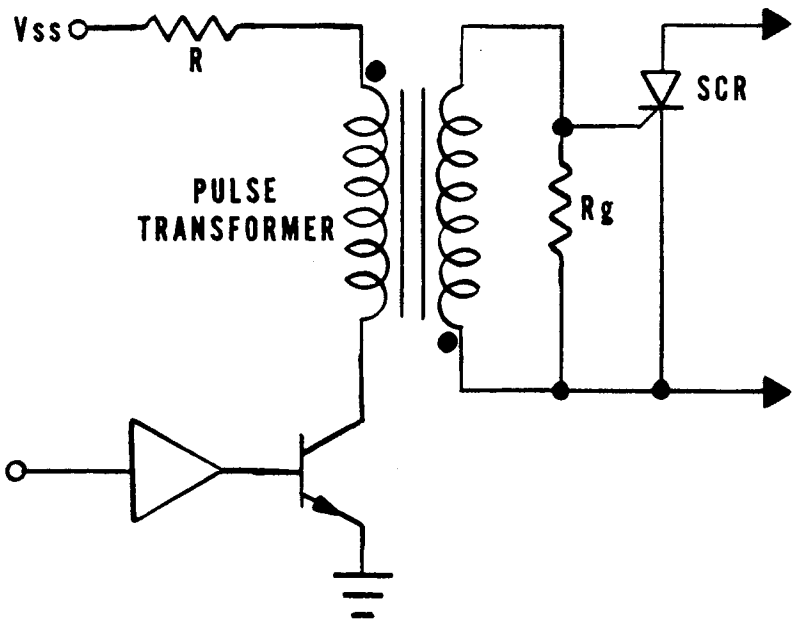


FIG.20 EDGE–SENSITIVE SCR FIRING CIRCUIT

high impedance gate to cathode network, thus lessening the circuits sensitivity to noise and false firing.

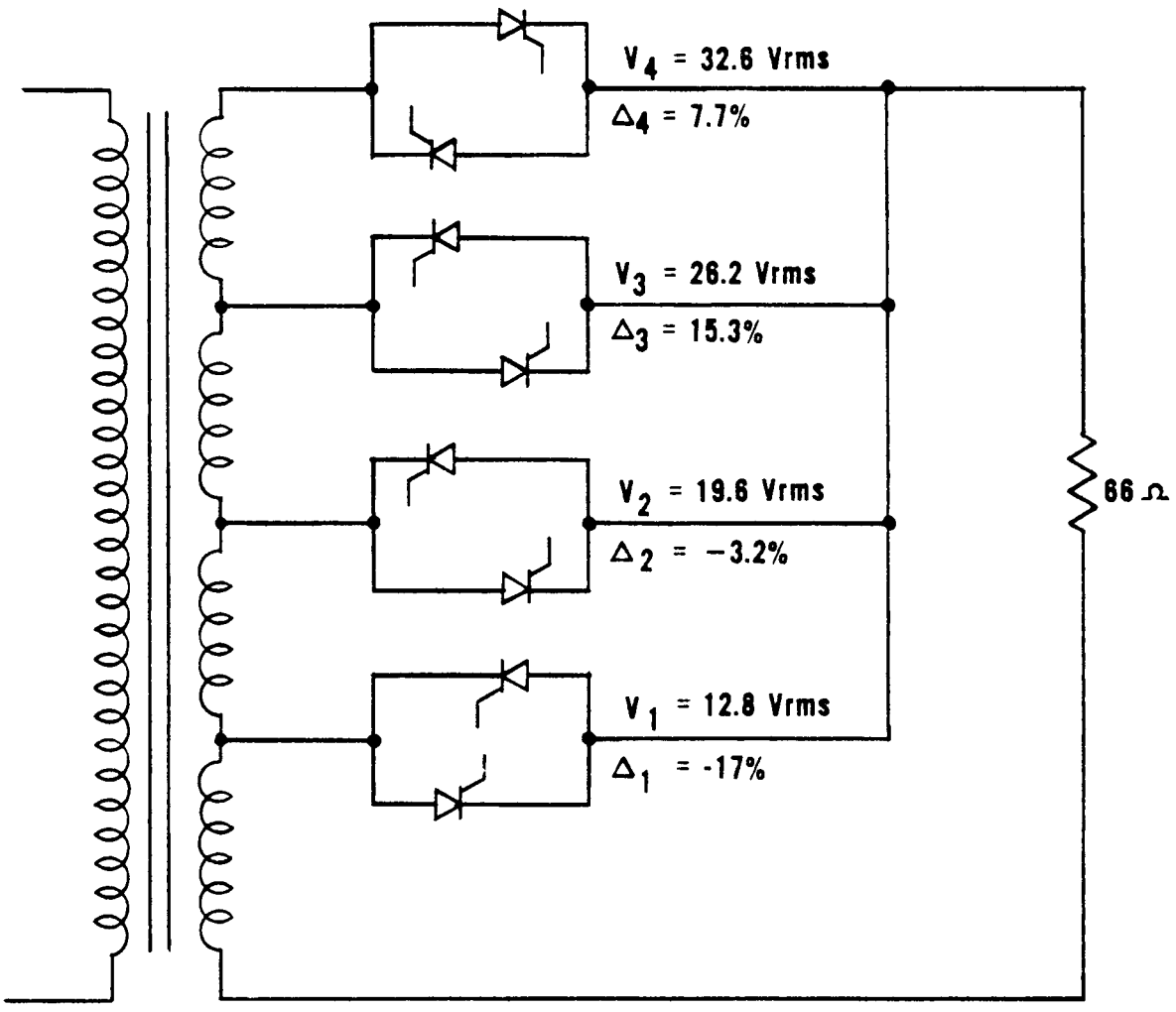
CHAPTER IV

SYSTEM PERFORMANCE

The Analysis Problem

Although it was stated earlier that the controller concept was implemented by using linear control theory precepts and simple digital signal processing, the final device turns out to be neither linear nor simple for analysis. Several specific portions of the controller introduce analysis complexity. For instance the crude four bit ADC which nullifies valid assumptions of linearity, the conversion of the four bit data to one of 15 sinusoids whose amplitude varies from cycle to cycle, and the conversion of the generated voltage waveforms into an average power measurement combine to give a controller which is very difficult to handle mathematically and whose performance is difficult to interpret. Particularly bizarre is the generation of pseudo-limit cycles for various setpoint settings. The net result is that computer simulation and empirical measurement are more prudently used in this situation than detailed mathematical analysis.

The prototype system employed to gain empirical insight is shown in Fig. 21. A four tap system was used with tap voltages which varied significantly from ideal settings (those that gave linear power increments) in order to demonstrate the controllers capability to generate precise power transients even with erroneous tap voltages.



Δ = $\frac{\text{DEVIATIONS FROM IDEAL}}{\text{IDEAL}}$

V = MEASURED VOLTAGE

FIG. 21 FOUR TAP TRANSFORMER PROTOTYPE

Initial Results

There were several refinements readily apparent to the controller design after the first few tests. The most obvious was for improvements to the analog-to-digital converter which at the time was designed with TTL integrated circuits. The conversion to CMOS and the use of low temperature coefficient resistors tremendously improved the performance of this portion of the controller. There were, however, some observations which appeared rather odd and were not easily explainable. The controller performance measured was not expected based upon the linear process control theory the controller design was based on. The observations revealed that within the dynamic range of the controller, the capability of the controller to follow setpoint changes was a non-linear function of both the amplitude of the setpoint, and the rate at which it varied. In fact for many values of the set-point moderate variations around some steady-state value would produce no change of the output. These observations led to an investigation of the theory of non-linear sampled-data systems. All of the observed phenomenon were discussed in that literature. However, the literature also revealed that there does not exist a consistent, well developed, generalized methology to handle such systems. Rather, there exists many analytical tools which when properly applied can give insight into non-linear sampled-data system performance, but the insight is very limited and specific. Not only is understanding the theoretical foundations of each of these complex analytical tools necessary but also recognizing when they can justifiably be applied is required. The result of the investigation was a realization that the use of non-linear sampled-data

system theory was beyond the scope of this paper and that improvement in circuit performance would have to be based upon "knowledgable intuition" and computer simulation.

The Pseudo-Limit Cycle

Fig. 22 demonstrates the initial performance of the controller. The arrows indicate where the controller failed to respond to set point changes and entered pseudo-limit cycles. In a pseudo-limit cycle the amplitude of the set-point, the rate of change of the set-point, the gain of the controller, and the time-constant of the controller combine to lock the output into some stable, repetitive pattern. In order to gain insight into this phenomenon we will examine in detail the effect of quantization, and time avereaging on limit cycle formation. The effect of adding a feedforward path in the controller will then be investigated along with the subtle non-linear effects of saturation.

Quantization and Time Averaging

The quantization of the output of the controller into only sixteen possible levels is the dominant factor in influencing the controller's performance. Let's examine its effects in detail. For simplicity, consider the model on page 71. In this model the output is quantized voltage levels which are fed back directly for comparison with the input. The amplified error signal is sampled every Ts seconds. The ADC has five possible outputs 0, .666, 1.333, 2.000, 2.6667. These values are the same as the ADC input quantization levels (i.e. the ADC has a gain of 1). Assume the setpoint is ramping at 1 V/sec. Let's examine

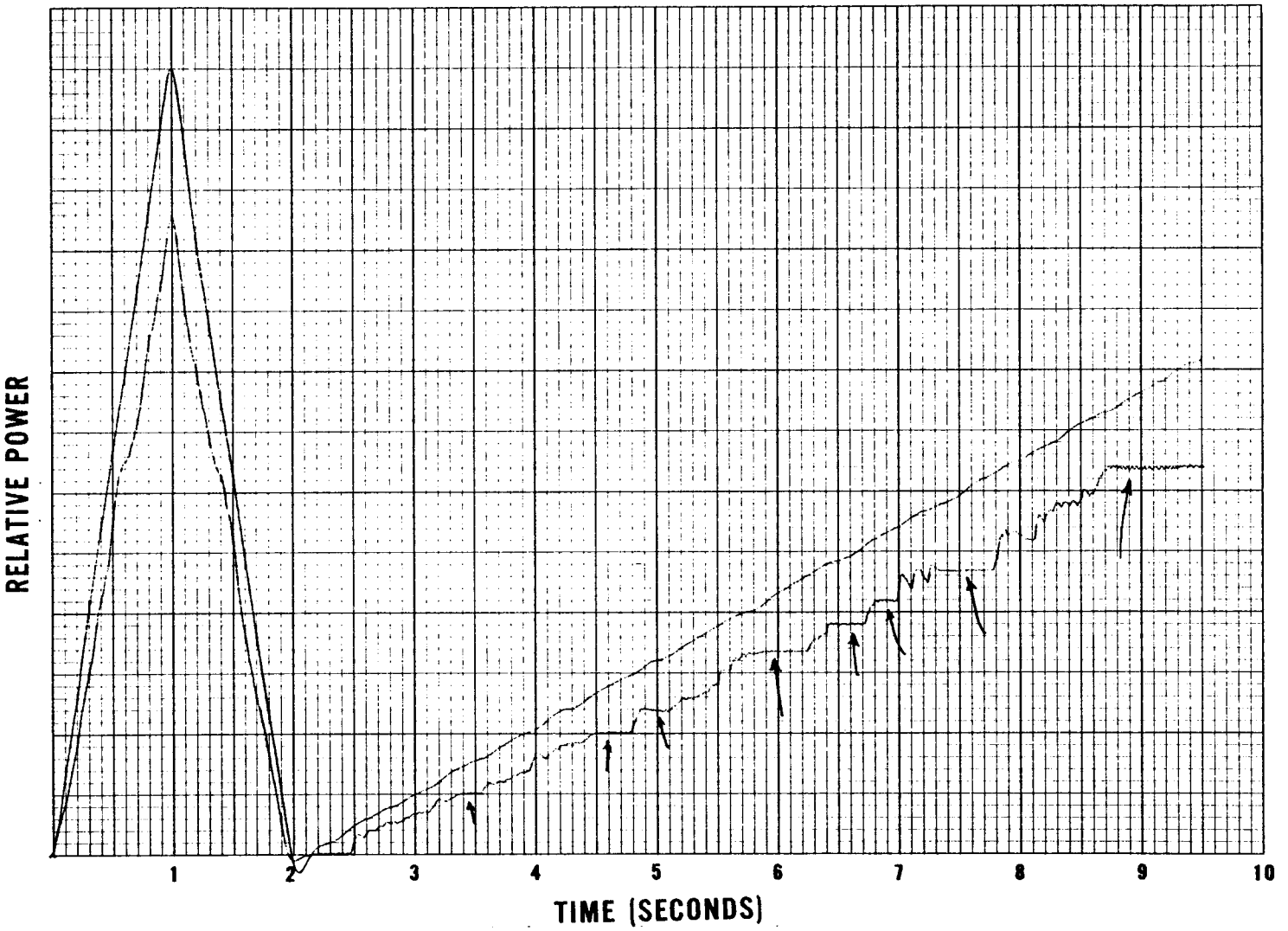


FIG. 22 INITIAL CIRCUIT PERFORMANCE TO RAMP INPUT

the output for the first few cycles with T_s = 1/60 second. The equations of interest are

$$D = 10(SP - P_n) \ , \tag{4-1}$$

$$D_n = D_{T_s} \ , \tag{4-2}$$

$$P_{n+1} = Q[D_n] \ , \tag{4-3}$$

where $Q[D_n]$ symbolizes the quantization of D_n . Thus,

$$P_{n+1} = Q[10(SP_n - P_n)] \ . \tag{4-4}$$

The values of Eq. (3-4) are shown in Table 4-1.

TABLE 4.1

PARAMETER VALUES AT n^{th} SAMPLING INSTANT FOR SIMPLE PROPORTIONAL CONTROLLER

n	SP	P_n	P_{n+1}
0	0	0	0
1	.01667	0	0
2	.03333	0	0
3	.05000	0	0
4	.06666	0	0.6666
5	.08333	0.6666	0
6	.10000	0	0.6666
7	.11666	0.6666	0
8	.13333	0	1.3333
9	.15000	1.3333	0
10	.16666	0	1.3333
11	.18333	1.3333	0
12	.20000	0	2.0000
13	.21666	2.0000	0
14	.23333	0	2.0000
15	.25000	2.0000	0

A plot of the output of the model in Fig. 23 is given in Fig. 24.

Let's now incorporate memory in the feedback loop by adding a single pole filter as on page 74. The equations of interest become

$$D=10[SP-f(p_n)] \ , \tag{4-5}$$

where $f(P_n)$ is the output of the filter,

$$P_{n+1} = Q[D_n] \ , \tag{4-6}$$

$$P_{n+1}=Q[10(SP-f(P_n))] \ . \tag{4-7}$$

The values of these parameters are shown in Table 4.2 for the first 15 samples.

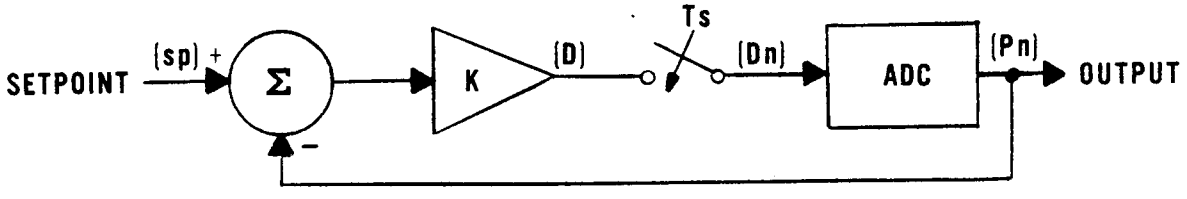


FIG.23 SAMPLED PROPORTIONAL CONTROLLER

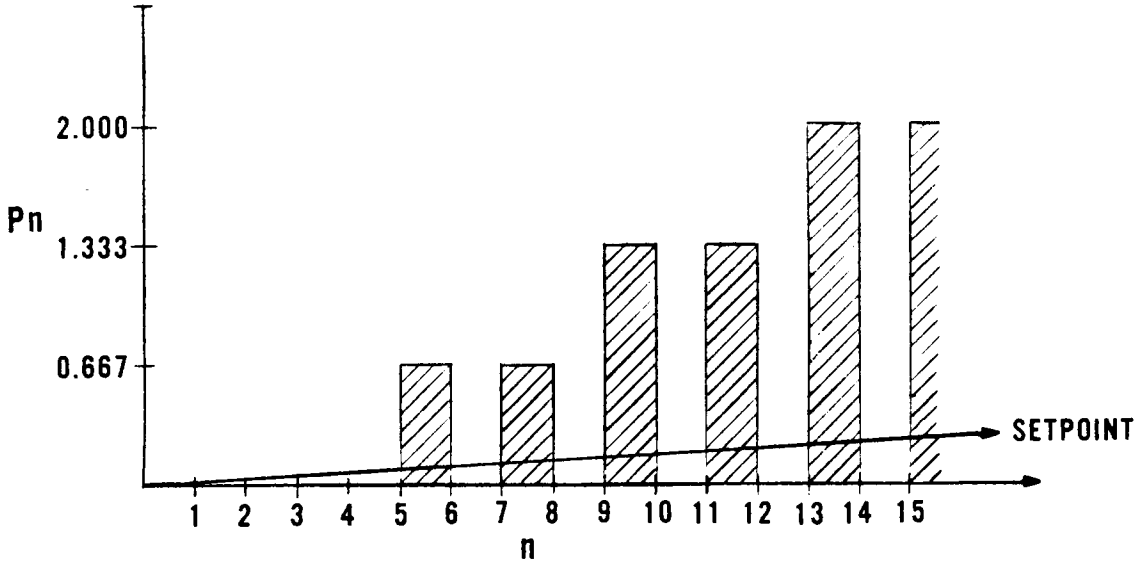


FIG.24 OUTPUT OF SAMPLED PROPORTIONAL CONTROLLER WITH 1V/s INPUT RAMP

TABLE 4.2

PARAMETER VALUES AT n^{th} SAMPLING INSTANT FOR TIME AVERAGED FEEDBACK CONTROLLER

n	SP	P_n	Pn+1	$f(p_n)$	D_n
0	0	0	0	0	0
1	16.67	0	0	0	0
2	.03333	0	0	0	0
3	.05000	0	0	0	0
4	.06666	0	0.6666	0	0.667
5	.08333	0.6666	0	0.102	-0.019
6	.10000	0	0	0.0863	0.137
7	.116666	0	0	0.0730	0.4365
8	.13333	0	0.6666	0.0618	0.716
9	.15000	0.6666	0	0.1547	0.0046
10	.16666	0	0	0.1309	0.357
11	.18333	0	0.6666	0.1107	0.726
12	.2000	0.6666	0	0.1961	0.039
13	.2166	0	0	0.1659	0.508
14	.2333	0	0.6666	0.1404	0.930
15	.25000	0.6666	0	0.2212	0.288

The output of the controller of Fig. 25 is shown in Fig. 26.

In CFTL the average power must be controlled to follow some demand setpoint. The single pole filter performs the averaging function desired. The plot of the output of the second model shows that the average of the instantaneous output more closely follows the setpoint than that of the first model. These two examples serve to demonstrate the two limits in filtering that can be used in CFTL. The first example has no filtering and the output shows no averaging capability. The second example uses a filter with a time constant, t = 100 ms. This is the longest time constant we can use in CFTL and still follow a fast ramp. Recall that earlier we demonstrated that a bandwidth of 16 Hz was required to pass the fastest CFTL ramps. This bandwidth however is too high to perform effective cycle averaging. Initial tests with a 10ms time constant (16 Hz) single pole filter in the feedback loop were dismal. There was no cycle averaging. The pseudo-limit cycles where very long. By increasing the time constant to 100ms dramatic improvements were realized. These improvements along with those due to incorporating feedforward control will be shown in the next section. Of course the fast ramps will be more distorted with a 100ms time constant. As in most engineering situations compromises must be made and in this case the trade-off involves accuracy and dynamic performance.

There is another compromise which must be made concerning time averaging. From an accuracy viewpoint, the longer the time constant the better the control. From a low frequency noise viewpoint, the longer the time constant the more the low frequency noise. Low frequency noise

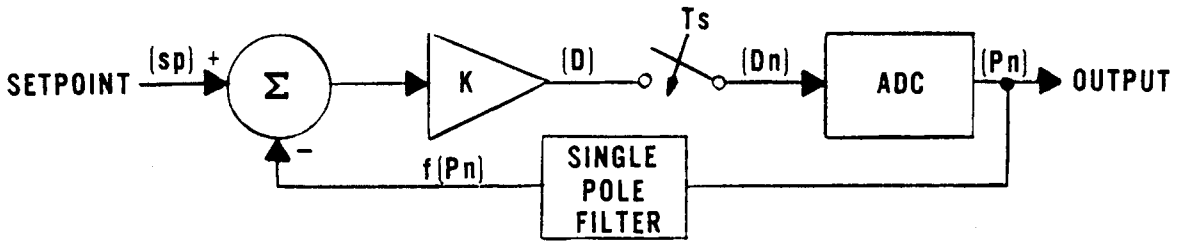


FIG.25 SAMPLED PROPORTIONAL CONTROLLER WITH SINGLE POLE FILTER IN FEEDBACK LOOP

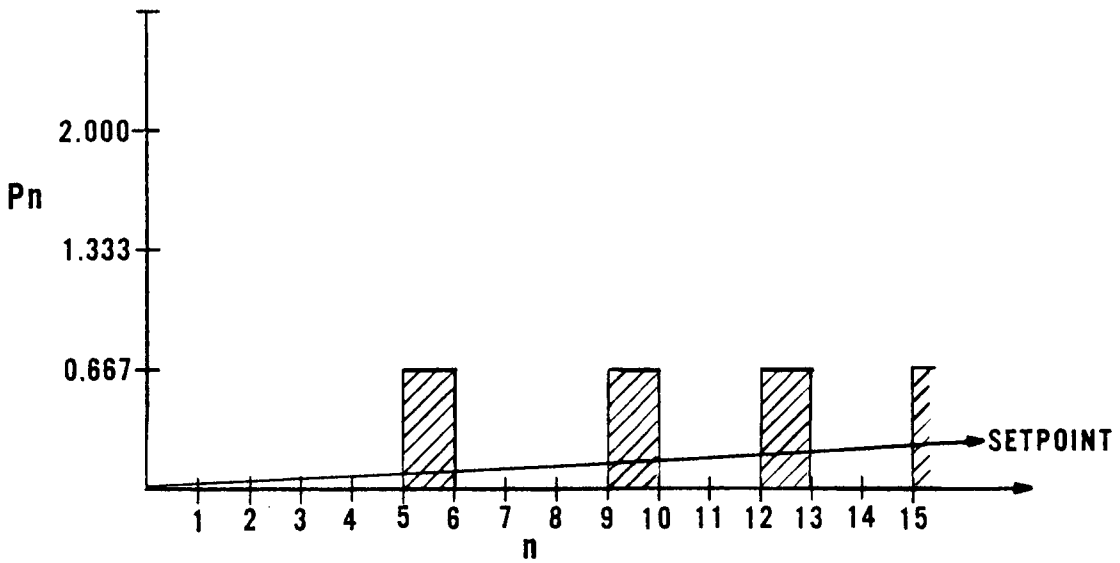


FIG.26 OUTPUT OF SAMPLED PROPORTIONAL CONTROLLER WITH SINGLE POLE FILTER IN FEEDBACK LOOP WITH 1V/sec INPUT RAMP

is a term used in reference to low frequency ripple in the power. This low frequency power variation can cause a serious mechanical problem in CFTL.[5] An example of a long time constant influencing low frequency ripple is the case of a filter with a time constant of 10 sixty hertz cycles (i.e. 0.166 seconds). A possible controller output pattern at some steady state set-point is nine cycles at one output level and one at another. If this pattern is repeated the power would have a 6 Hz component. This low-frequency component would never exist in an actual reactor (which we are trying to simulate) and thus is a form of noise. The low frequency power ripple would also cause mechanical movement of the fuel rod simulators due to thermal expansion and contraction and cause friction between the rods and their spacers. Computer simulations by Ball[6] have shown this friction to be detrimental to the bundle. Therefore a trade off must be made between accuracy and low-frequency noise in the design of this controller for CFTL. This point will be addressed again later.

Although the addition of the averaging network in the feedback tends to lessen the effects of quantization (the feedback signal is continuous rather than quantized as in the first model) a close analysis of controller performance reveals that quantization still limits performance as it plays a major role in the formation of limit cycles.

Fig. 27 is a graph of the setpoint, averaged feedback signal and the amplified error signal. This graph indicates the relationship between these three signals just prior to, during, and immediately following a limit cycle. The amplitude of the setpoint and feedback signal are indicated on the left. The error signal has a different

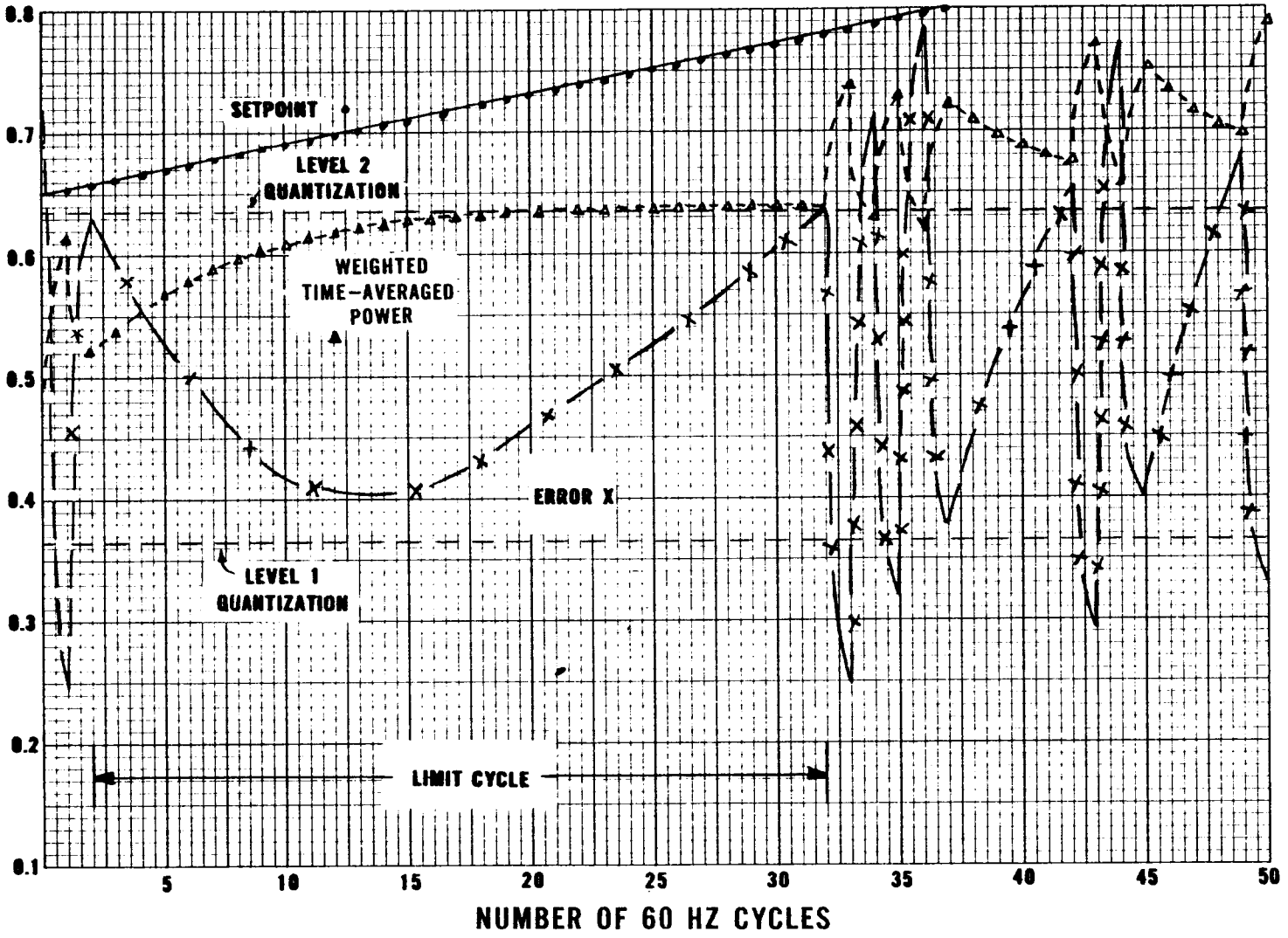


FIG. 27 PLOT OF SETPOINT, WTAP, AND ERROR

scale which is not shown on the figure. Also indicated in the figure are the threshold levels of the ADC. If the amplified error signal is less than the first threshold level then no power is delivered to the load. If the signal falls between levels 1 and 2 then the voltage from the first tap is connected to the load, and between 2 and 3 connects the second tap, etc. From the figure we observe that in the vicinity of a main tap voltage (i.e., when the setpoint demands a power level close to that corresponding to a single tap power level) the error signal is temporarily bounded between quantization levels and the output does not change. We also note that increasing the time rate of change of the setpoint can shorten the duration of the limit cycle. Increasing or decreasing the gain of the controller will also influence limit cycle formation. It is important to note that although it appears that increasing the gain will shorten the duration of the limit cycle as visualized here, increased gain will lengthen limit cycles which occur due to the error repeatedly bouncing back and forth between widely separated quantization levels.

Feedforward Control

Figure 28 shows the controller performance with the four tap transformer prototype. In this experiment a single-pole filter with a time constant of 100 ms was used in the feedback loop and the amplified error signal directly drove the output. The difference between the setpoint and the measured average power is due to the control scheme used. In order to output the power corresponding to tap 4 for instance, the error signal times the gain of the controller must exceed the

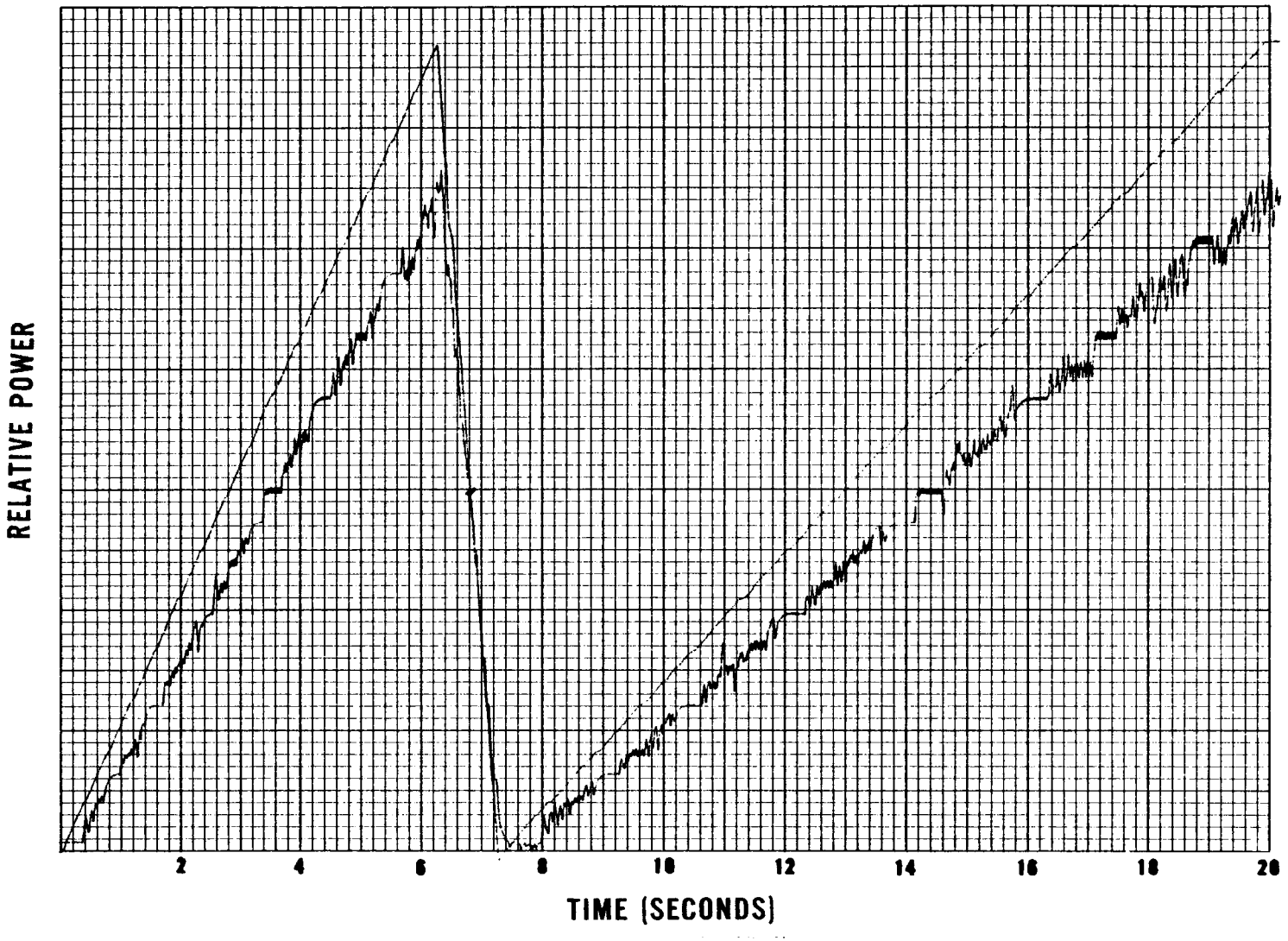


FIG. 28 PROPORTIONAL CONTROLLER PERFORMANCE

quantization threshold corresponding to tap 4. Thus the error increases as the setpoint increases. Increasing the gain did not significantly decrease the difference between the setpoint and the average power. The reason this did not improve system performance is discussed in the next section.

One way to eliminate the offset inherent with straight proportional control is to incorporate a feedforward path for the set-point. This feature is shown schematically in Fig. 29. The driving signal is no longer the amplified error signal but is the set-point modified by the amplified error signal. With this scheme the set-point can be set at some high level and the output can attain that level with zero error. The performance of the controller with this feedback scheme is shown in Fig. 30. Several advantages of this scheme are apparent from this figure; first, the limit cycle phenomenon is minimized considerably; secondly, the difference between the set-point and the measured average power has virtually been eliminated, and thirdly, the amplitude of the fluctuations in the average power about the set-point has been reduced.

When the test runs were completed using feedforward control the improvements appeared so outstanding that the design was then frozen and printed circuit boards based upon the design were fabricated. That enthusiasm proved later to be unfounded as computer simulations generated for use in this thesis revealed a non-linear phenomenon which wasn't accounted for in the original empirical results of the feedforward controller. The phenomenon which was ignored was saturation.

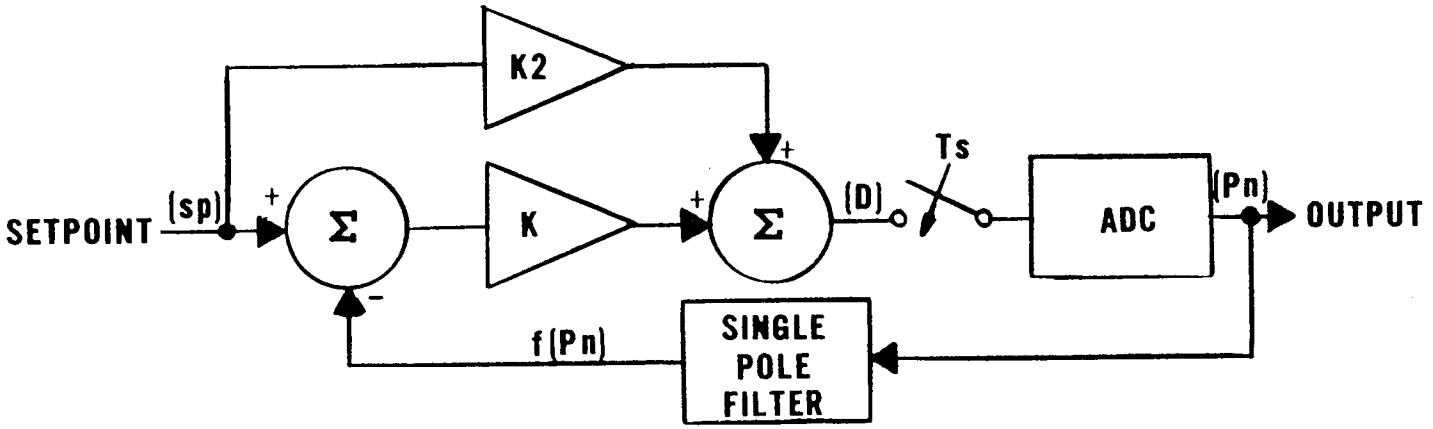


FIG.29 PROPORTIONAL CONTROLLER WITH FEEDFORWARD

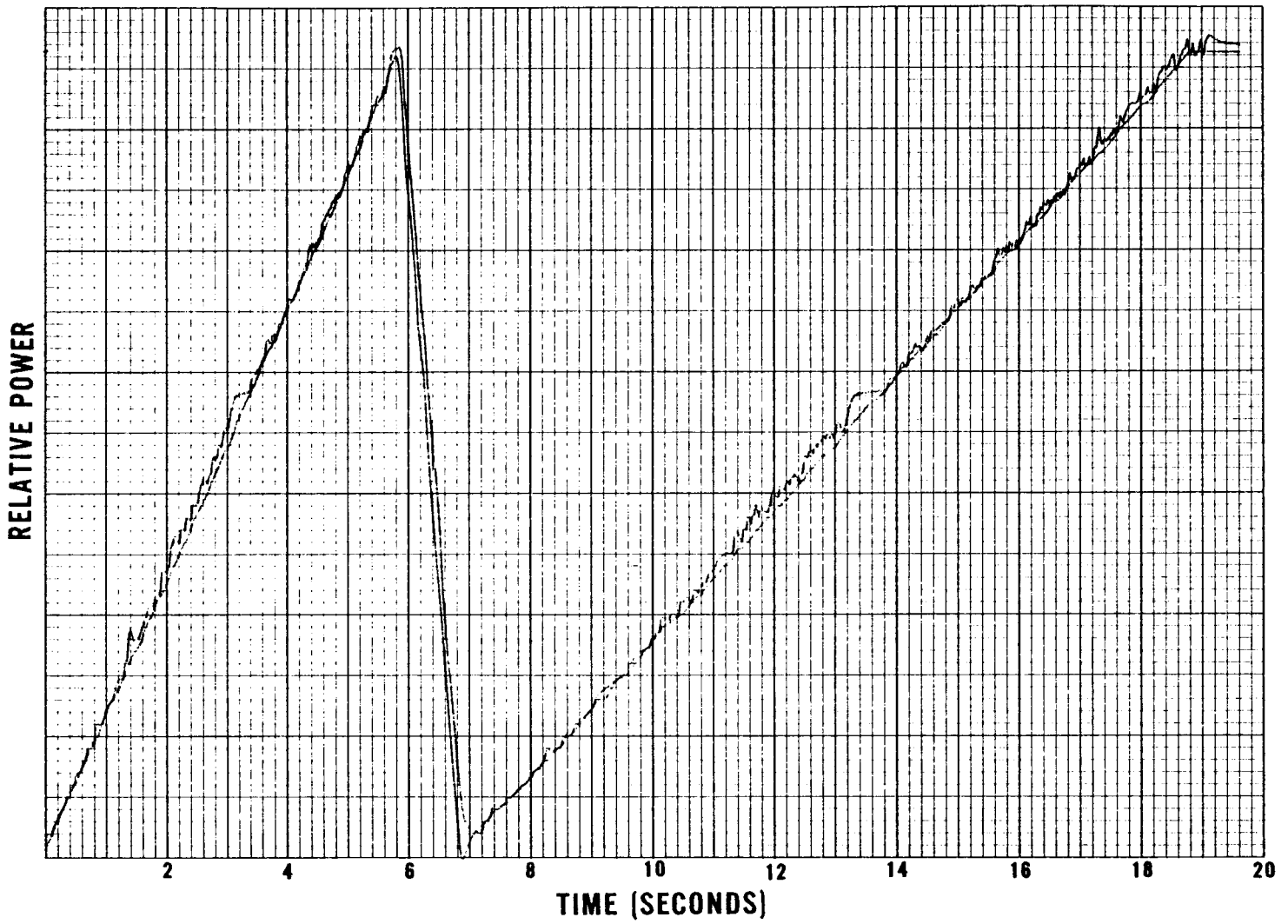


FIG. 30 CONTROLLER PERFORMANCE WITH FEEDFORWARD

Saturation

The four tap transformer prototype system has extremely limited input dynamic range (the range of the setpoint). All input values below 0V are decoded as 0V and all values in excess of 2.667V are decoded as 2.667V. With the feedforward control scheme an error signal gain (K) of around 20 and a feed-forward set-point gain (K1) of around 2 gave the best apparent control accuracy. However when these gains where used in computer simulations of the 15 tap CFTL system, the simulated performance was less than adequate. The average power was still controlled well but the pattern of SCR firing was unacceptable. For instance when 25% of full scale power was requested the controller would alternately fire the 50% tap and the zeroeth tap (no voltage) instead of simply turning on the tap corresponding to 25% power directly.

In the bench test with the four tap prototype, the saturation of the four level ADC prevented wide excursions at the output. The gains which indicated optimum performance were optimized only for this limited range prototype and gave no insight into the performance of the 15 tap system.

The effect of saturation in the 15 tap system cannot be ignored. Gain setting which optimizes system performance near the saturation level (i.e., 100% of full scale and 0% of full scale) will cause wide fluctuations in the output for setpoint settings near midrange (i.e., 50% of full scale). These fluctuations do not affect the accuracy in terms of controlling average power but they do introduce large instantaneous power fluctuations. As indicated earlier there is a concern in CFTL with spurious rod motion, motion of the fuel rod

simulators due to thermal (power) changes. A major design objective is to assure that the controller minimizes the amplitude of power excursion beyond those necessary to generate the required transients.

Discussion of Low Frequency Noise

1. The Low Frequency Noise/Accuracy Trade Off

Since the instrumentation bandwidth of most CFTL instruments is defined by the 16 Hz filter of the data acquisition system, the power system should not be allowed to generate noise in this spectrum. Table 2.3 is reproduced in Table 4.3 for convenience. Notice from the table that the low frequency noise frequency components can only assume discrete values. If no frequency components below 16 Hz are desired then only the SCR firing patterns which generate frequency components at 20 Hz and above can be allowed. This decreases the accuracy which the controller can attain. For instance the minimum power level which can be attained with the 20 Hz limit is 2.2% of full scale. One CFTL requirement is that the output be within 1% of the correct value at 4% of full scale. The 20 Hz limit makes it impossible to be within even 10% of reading at 4% of full scale. The two requirments are mutually exclusive.

2. The Spurious Rod Motion/Accuracy Controversy

There are two "schools of throught" connected with resolving the discrepancy between noise and accuracy. The first school considers the effect of low frequency noise on spurious rod motion insidious. They believe that the SCR pairs should be fired in an open-loop preprogrammed manner which minimizes the spurious rod motion. This will be done at

TABLE 4.3

LMPL POWER SUPPLY: CONTROL MODE CHARACTERISTICS FOR SINGLE WINDING

(6.67% power per winding. These same characteristics apply to whichever of the 15 windings in the LMPL power supply is used to supply fine control)

Control Mode No.	Firing Pattern Tap No.	Percent of Total Power	Step change for decreasing power (%)	Dominant Power Frequency (Hz)
1	15-15-15-15-15-15	100.00		120
2	15-15-15-15-15-14	98.89	1.11	10
3	15-15-15-15-14	98.67	0.22	12
4	15-15-15-14	98.33	0.34	15
5	15-15-14	97.78	0.55	20
6	15-15-15-14-14	97.33	0.45	12
7	15-14-15-14	96.67	0.66	30
8	15-15-14-14-14	96.00	0.67	12
9	15-14-14	95.56	0.44	20
10	15-14-14-14	95.00	0.56	15
11	15-14-14-14-14	94.67	0.33	12
12	15-14-14-14-14-14	94.44	0.23	10
13	14-14-14-14-14-14	93.33	1.11	120
Next winding:				
13	14-14-14-14-14-14	93.33		120
14	14-14-14-14-14-13	92.22	1.11	10
15	14-14-14-14-13	92.00	0.22	12
	Etc.			

the expense of accuracy. It is their belief that the CFTL measurement system will accurately measure the actual bundle power precisely. Since all analysis of the bundle performance will be based on measured data, accuracy of the measurement system is more important than accuracy of the controllers.

The second school believes that accurate power control is paramount. Many CFTL transients involve controlling both the bundle power and helium flow together. If the helium flow decreases faster then the bundle power then the fuel rods will be undercooled. If the flow decreases slower than the power the fuel rods will be overcooled. In either case mechanical damage could occur to the rods. They site the induction regulator as a possible source of dynamic inaccuracy due to the change in its output impedance with rotor position and its slow response to load changes. This school also believes there is over concern with spurious rod motion as the computer simulations which first uncovered the phenomenon tend to be conservative and accentuate its effects.

Since there is at present no facility to test for the existence and seriousness of spurious rod motion and since the motor driven induction regulators have not yet been built, the issue of spurious rod motion vs. accuracy has not yet been resolved.

CHAPTER V

CONCLUSIONS AND PROPOSED CONTINUATION

Summary of Progress to Date

There were eight items of particular significance discovered thus far in the CFTL power supply development effort. These items have been discussed in this paper in detail and are renumerated here to summarize the important results of this investigation.

1. Development of a Feedback Signal Philosophy

   The peculiarities of average power measurement as it relates to steady-state and transient sinusoidal power were discussed. The concept of a weighted time-averaged power was introduced and adopted as the optimum conditioning scheme for the power feedback signal.

2. Determination of Required Bandwidth

   CFTL specifications require that linear power ramps be accurately generated. The minimum controller bandwidth required for the fastest CFTL ramp was shown to be 16 Hz.

3. Present Power Measurement System Inadequate

   The present power measurement scheme uses analog signal conditioning circuitry followed by a fast data acquisition system. The analog circuitry includes a 16 Hz low-pass filter. This filter has been shown to be inadequate for measurement of power during fast transients.

4. Development of the Relative Power Feedback Scheme

Each series of CFTL tests include a unique maximum and minimum zone power. In order to avoid the need for tedious gain adjustments with each series, a feedback scheme was developed which automatically adjusts the feedback gain so that the maximum power is always interpreted as 100% of full scale demand.

5. Completion of Failure Analysis

Several controller failure modes were discussed along with possible results of that failure. The digital signal conditioning portion of the controller was shown to be the critical portion of the controller design. The investigation also revealed that without edge-sensitive triggering of the SCR network it will be possible for the system to hang up and keep the power at an unsafe level. Edge-sensitive triggering will prevent this from occurring.

6. The Effects of Non-Linearities

The effects of non-linearities on controller performance were investigated. The generation of pseudo-limit cycles by the controller was attributed to quantization effects. Saturation was shown to limit the generalization's which could be made based upon prototype performance.

7. Conflicting Specification

Within the confines of the 15 tap transformer/zero phase-fired LMPL system the requirements for 1% of reading

accuracy and the generation of no power frequency components below 16 Hz are mutually incompatable.

8. Development of Prototype Controller

A controller has been built and tested on a four tap transformer prototype and will be used for thermal cycling tests of prototype CFTL fuel rod simulators.

Proposed Outline for Continued Development

There are several recommendations that can be made concerning the next course of action for this development effort. The first is that a firmer theoretical foundation must be developed. The techniques developed by non-linear sampled-data system theory must be studied and applied to minimize the "hit and miss" approach that has thus far been employed. Recommended areas of study include the Carson-transform, the discrete phase plane method, the z-transform, the state variable method, and describing functions. The various variable representation methods (Carson-transform, z-transform, and state variables) should be compared and evaluated for optimum usefulness in CFTL control system analysis. This theoretical foundation will also aid in the analysis of other CFTL control schemes which also involve discrete-time control.

Another option is to continue with the empirical approach and investigate controller performance using standard proportional, integral and derivative control concepts. This may prove a more attractive alternative to the pursuing of a stronger theoretical background because of the severe time constraits imposed upon the CFTL development efforts. This option could be tied to the continued use of extensive computer

modeling. However true insight into contoller performance and generalizations to other CFTL control schemes would not be as great as with the first option.

Another recommendation is that the fuel rod simulator thermal cycling tests, which will be using a four tap transformer system with the feedforward control scheme described in this paper, be used to evaluate the seriousness of the low frequency power noise as it relates to spurious rod motion.

A final recommendation (one that is more detailed and specific) is that the induction regulator voltage used in the relative feedback scheme be sampled and held during a transient so that its variation with load changes will not interfere with the transient accuracy. Refer back to Fig. 15 on page 46.

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VITA

Daniel W. McDonald was born February 27, 1952 in Jackson, Michigan. At an early age he dedicated his life to God. His first ambition was to become Pope. Encouraging his ambition, his parents enrolled him in the local parochial school, where he excelled in theology, Gregorian chant and cold showers. However, in 1969 he met the vivacious and sensual Victoria Embury and upon graduation from Lumen Christi (Light of Christ) High School, attended Michigan State University instead of the seminary.

Being an excellent student, young Daniel excelled in every subject area and still had time for debauchery on the weekends. Advancing toward his junior year he became pressured to choose a major. On Monday, May 16, 1972, he threw a university catalog across the room. It landed face down on the pages listing the requirements for a degree in Electrical Engineering. The next day he declared this his major and then asked what an electrical engineer was.

As an E.E. major Mr. McDonald was accepted into the Eta Kappa Nu Honor Society and was elected their president during his senior year. He was also asked to join Phi Beta Pi but by this time he was married to Victoria and they couldn't afford the 25 bucks initiation fee.

McDonald graduated with honors in 1974 and accepted a position at the Oak Ridge National Laboratory. He immediately began work on his M.S. in electrical engineering at the University of Tennessee. Victoria began to forget what his face looked like because of his work and classes. One night she casually asked if he would take off a term if she was having a baby. When he said yes, she flushed her pills down the

toilet and nine months later Marty was born. This ploy worked so well she tried it again and Anne Marie arrived 18 months later.

Mr. McDonald has published several articles, survived Dr. Blalock for three terms and managed to maintain a high grade point average. This was accomplished despite two noisy toddlers and a wife prone to crying jags and bouts of depression.

PLEASE GIVE HIM HIS MASTERS DEGREE!!