

To the Graduate Council:

I am submitting herewith a thesis written by Robert Eugene Crossley entitled "A Real-Time Stereo Video Digitizing and Reconstruction Circuit." I recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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A REAL-TIME STEREO VIDEO DIGITIZING
AND RECONSTRUCTION CIRCUIT

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Robert Eugene Crossley

August 1979

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Dedicated to my parents,
Mr. and Mrs. W. J. Crossley, Jr.
for their continuing love,
support, and encouragement
throughout my education.

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ABSTRACT

A system which can digitize, transform, and reconstruct real-time video images in stereo is presented. This system is able to perform transformations on two video source waveforms independent of each other. A unique sampling approach which allows only the sample points of interest to be stored in memory for processing is also presented as a part of the system. A hardware configuration for such a system is related and experimental results of images transformed by the system are shown and evaluated.

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CHAPTER 1

INTRODUCTION

Digital image processing and the use of computers to enhance video images has been a research project at The University of Tennessee through support of NASA contract NAS8-29271 since 1974. The first major result was an algorithm which used the histogram of an original image as the basis to produce an enhanced image of the same subject [1]. Later research produced a real-time video image enhancement system capable of performing several methods of enhancement on live scenes viewed through a monochrome television camera [2]. This investigation is a continuation of this research.

With the advancements made in semi-conductor technology, it is now possible to perform real-time digital image processing and enhancement at speeds which were not possible several years ago. The introduction in mid-1978 of an analog-to-digital converter on a single chip capable of sample rates above 20 megahertz provided the field of image processing research with a valuable new tool. This new device allowed a new dimension to be introduced in video image processing, real-time stereo image processing.

Real-time stereo image processing and enhancement is a useful tool in that it allows the dimension of depth to be added to the enhanced image when the two processed signals are combined through an appropriate mixer and the display viewed through the proper filter. This new feature may be used in remote control operations such as robot control and operations outside a spacecraft where the operator needs depth information to perform tasks such as equipment retrieval and repair.

Chapter 2 of this investigation is an overall description of the stereo digitizer, including its capabilities and power requirements.

Chapter 3 deals with the data acquisition portion of the digitizer. This part of the system accepts the incoming video, properly adjusts the signal, samples it, and transmits its digital representation to the rest of the circuit.

Chapter 4 deals with the transformation memory. Proper mapping of the digital video data into its new transformed value and the storage of sampled data points to be used by the processor to generate new transformation curves are discussed.

Chapter 5 deals with the reconstruction of the transformed digital data into its analog form for proper display. Added features which provide the use of a data bus for display from an external digital source and also various sync signals to assure proper stereo enhancement operation are also covered.

Chapter 6 discusses the interface circuit and its operation. The appropriate signals for the use of the system with another processor are also discussed.

Chapter 7 deals with the control circuit and its relation to the rest of the system. The function and operation of the control circuit which allows only the desired points of the picture to be stored and used by the processor are discussed in this chapter.

Finally, Chapter 8 contains experimental results that show system performance for various sampling rates.

CHAPTER 2

SYSTEM DESIGN

As indicated in Chapter 1, the principal purpose of this study was to design and fabricate a system which could digitize, map, and reconstruct stereoscopic video waveforms without noticeable degradation. The system, referred to as the Video Digitizing and Reconstruction Circuit, or VDRC, is shown in block diagram form in Figure 2.1. The principles of operation and capabilities of the VDRC are discussed in the following sections.

2.1. Basic Block Diagram and Description

As can be seen in Figure 2.1, the VDRC is an analog-digital hybrid system that uses a double bus structure. The digitized video signal is transmitted through the system on the Video Sample Bus (VSBUS) between the Video Sampling Circuit (VSC) and the Video Reconstruction Circuit (VRC). If two video sources are being sampled simultaneously, the digital information from both video sources is transmitted along this bus in an alternating manner.

The Video Pre-processing Circuit (VPC) adjusts the incoming video signal to the proper amplitude and phase and also clamps the back porch of the signal to a reference value (the setting of this value is discussed in the next chapter). This clamping action is to insure that the black level of the incoming signal stays the same DC value regardless of the changes in the input video waveform. The VPC also reproduces a composite sync signal that is TTL compatible with the digital circuits in the system. A separate VPC is used for each video source.

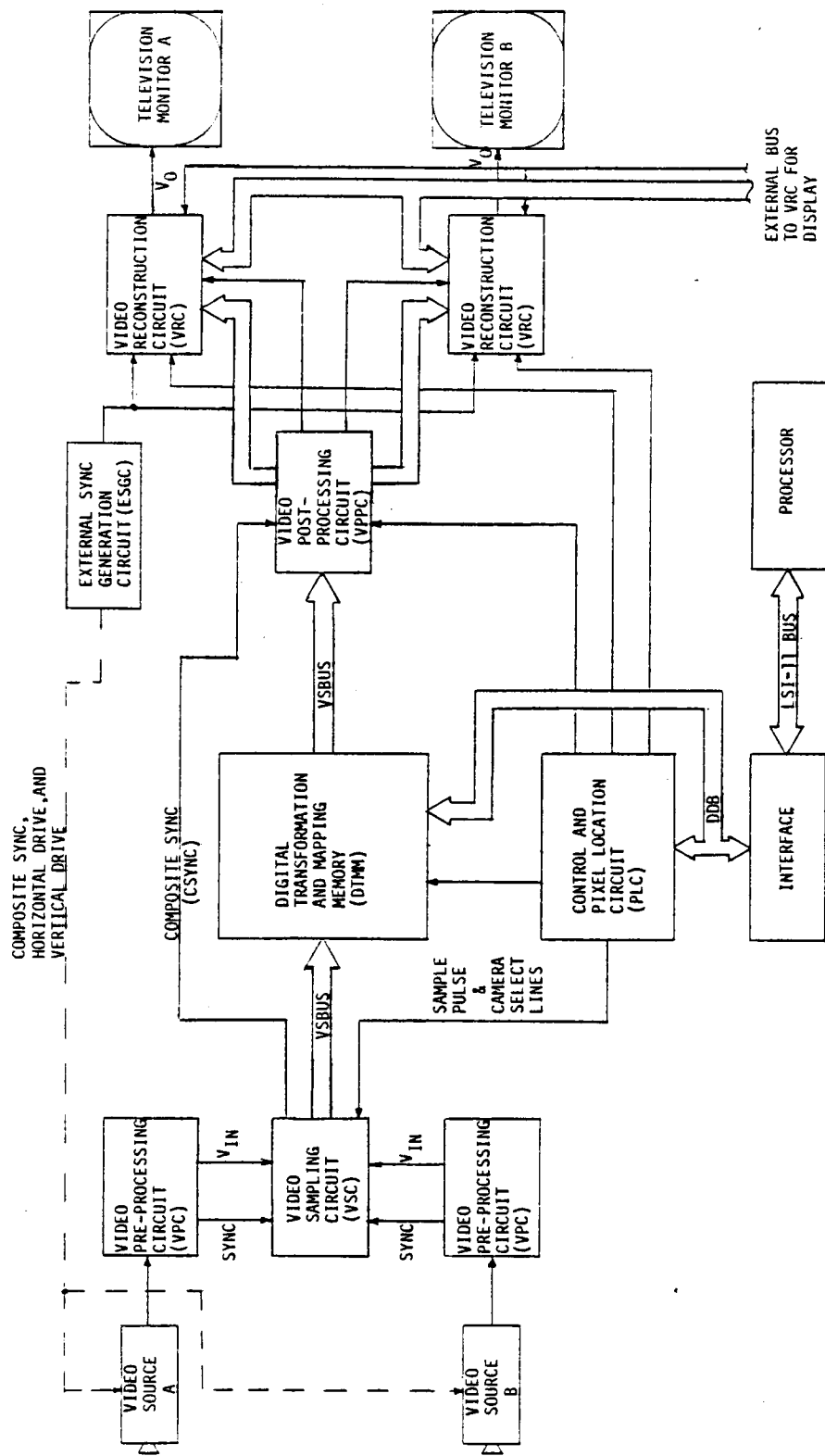


Figure 2.1. The Video Digitizing and Reconstruction Circuit (VDRC).

The Video Sampling Circuit (VSC) takes the clamped video waveform from the VPC of each video source and routes them to the analog-to-digital (A/D) converter. Using analog switches, this circuit selects which waveform is input to the A/D converter to be sampled at the appropriate time. These switches are controlled by signal lines from the control circuit, as shown in Figure 2.1. The decision to multiplex the analog signal before sampling rather than the digital data after sampling was the cost factor of the A/D converter. To multiplex the digital data after digitization would require two A/D converters resulting in an approach which would not be the most cost effective. Therefore, the analog switching with one A/D converter system was chosen.

The Digital Transformation Mapping Memory (DTMM) is used by the system in two different methods. One method is as a mapping memory. In this mode of operation, the memory acts as a look-up table for the incoming digitized video information. Sampled video information enters at one value and, through the process of the look-up table, leaves the memory as a new value. The new values to be assigned to the sampled values are determined by the processor. Enhancement of a video image in real-time is accomplished through this method of transforming the incoming video. The video digitizer can also sample points faster than the microprocessor can store them. Using the DTMM allows the processor to request a certain horizontal line or part of a line be sampled and stored in the DTMM at the faster rate. Then the processor can move the data points from the DTMM to its main memory at a slower rate through direct memory access (DMA) or through processor control. Two identical DTMM's are used in this system simultaneously. One is always functioning

as a look-up table while the other is used to store sampled points from the incoming video, with these functions being reversible between the two DTMM's.

The Video Post-processing Circuit (VPPC) is used to multiplex the output of the two DTMM's to allow the output of the DTMM used as the look-up table to be sent to the Video Reconstruction Circuit. Producing the proper amount of delay in the composite sync information to compensate for the delay time in the system from input to output is also a function of the VPPC. This delayed sync is also used to generate a composite blanking signal which is required by the digital-to-analog (D/A) converters present in the Video Reconstruction Circuit of the system.

The Video Reconstruction Circuit (VRC) is composed primarily of two D/A converters. These converters require eight bits of digital information, a composite sync pulse signal, a composite blanking pulse signal, and a strobe or clock pulse to initiate each conversion. These converters then generate composite video signals which have the proper amplitude and output impedance to match the standard 75 ohm impedance of a cable used to drive a standard television monitor. Therefore, the display generation of the digital data from the DTMM is done by these two D/A converters. Each VRC is also capable of generating a display from data fed to it by means of an external bus. A still picture stored in memory may be displayed by the process of cycling through the memory and transmitting the pixel values to the VRC along this external bus.

The video information is pipelined through the system from input to output. Therefore, at any moment, the information may be found in all phases of its transformation; that is, pre-processing, sampling,

digital mapping, post-processing, and reconstruction are being performed simultaneously to different parts of the information signal along the VSBUS. This method of digitization, transformation, and reconstruction holds the delay time of the system to a minimum while also allowing the throughput of information to be kept at a maximum. Thus the system is structured to operate at optimum efficiency.

As mentioned earlier in this section, the system is a double bus structured system with one bus being the VSBUS previously described. The other bus is the Digital Data Bus (DDB) through which the processor communicates with the DTMM and control circuit. This bus is a 16-bit bus and connects through an interface to the processor of the system. The processor uses this bus to set the control register, start/stop register, vertical register, and horizontal register in the control circuit. Pixel values for sampled points of the picture in the DTMM are moved to the processor memory and new transformation curves are loaded in the DTMM through the bus. The system is configured in such a manner that only one DTMM at a time is addressable by the processor.

The interface of the system is designed to be compatible with a D.E.C. LSI-11 bus structure. This prototype needs a Digital Equipment Corporation LSI-11 microprocessor. A more in-depth discussion of the interface used by the system is given in Chapter 6.

The control circuit coordinates system operation using the instructions it receives from the processor via the control register and the start/stop register. This circuit controls the sample rate selected and the selection of the proper video source to be digitized, and if both sources are chosen to be digitized, which one may have sample points stored in the DTMM. The selection of the proper D/A converter to be

clocked when a digital byte is presented to be reconstructed is another function of this part of the system. In addition, the control circuit selects which DTMM is addressable by the processor at any instant and determines when the correct number of data points are stored in the DTMM. It produces a write pulse and chip enable pulses to the memory in the proper timing sequence to allow these data points to be stored correctly. The storage of sampled data points is controlled by the start/stop register with the processor initiating the procedure with a command and the VDRC system issuing a reply when the process has been completed.

The Pixel Location Circuit (PLC) uses the composite sync signal originating from the VSC and has the capability of determining which video field, horizontal line, and, according to the rate selected, the point being sent through the system at any instant. This circuit is used in the following manner. Appropriate coordinates of the desired pixel location are loaded in the horizontal and vertical registers by the processor. The processor then initiates the procedure by means of setting the start/stop register. This circuit then waits for the proper pixel location to appear in the system and signals the control circuit that the location requested has been found. A control circuit function uses this signal to initiate the storage of the appropriate number of sample points into the DTMM by means of issuing write and chip select commands at the appropriate intervals. Only the parts of the video signals that are of interest are stored in this manner. The processor can therefore eliminate unnecessary information and use only the sections of the scan that have been selected as being useful.

A final circuit used in the system is an External Sync Generation Circuit (ESGC). This circuit provides composite sync, horizontal drive, and vertical drive to external connectors. These signals must be used when both cameras are digitized to assure the video outputs are in synchronization, i.e., the video sources present the same location from their respective scans to the system at any given instant. The signals may also be used to drive a video source if it does not produce standard NTSC sync internally. A description of standard NTSC sync is given in Appendix A. This circuit also provides the VRC with composite sync and composite blanking when the VRC is used to display data from the external bus, as mentioned earlier.

2.2. System Capabilities

The VDRC is designed to be a versatile system which gives the user a large degree of flexibility. Referring to the two video waveform inputs as A and B, the VDRC system allows the following options under processor control.

1. Digitize, transform, and reconstruct either A or B from a choice of six different sample rates: 29, 58, 116, 232, 464, or 928 samples per horizontal line.
2. Digitize, transform, and reconstruct A and B simultaneously to two separate monitors from a choice of five different rates: 29, 58, 116, 232, or 464 samples per horizontal line from each video source.
3. Sample and store in the DTMM from 2 points up to a maximum of 464 points, or any chosen even number inclusive, from any selected horizontal line of video from either A or B while

still digitizing, transforming, and reconstructing both video signals.

4. Sample and store in the DTMM from 2 points up to 464 points, or any chosen even number inclusive, from a selected horizontal line of video from either A or B while still digitizing, transforming, and reconstructing the video source selected.
5. Reconstruct one or two different pictures to one or two separate monitors, respectively, from data provided on an external bus to the VRC.

It should be noted that the sampling and storage in the DTMM does not affect the digitization, transformation, and reconstruction of the information, i.e., the output is not stopped or affected in any way during the storage process. The process for selecting the above options is discussed in Chapter 7. The VDRC also provides the features of composite sync, horizontal drive, and vertical drive to assist the user in keeping proper synchronization of the video signal, especially when two video sources are used. Internal lines of composite sync and composite blanking are provided to give the VRC the proper signals needed when display of data from the external bus is desired.

2.3. System Requirements

The VDRC requires three external power supply voltages: +15V DC 3 amp, -15V DC 3 amp, and +5V DC 10 amp. The +15V DC and -15V DC are used to supply the analog portion of the system, the A/D converter, and D/A converter. A +5V DC supplies the digital portion of the system.

The VDRC configuration discussed in this report requires an LSI-11

microprocessor for proper operation. As mentioned earlier, another type of 16-bit processor may be used if the proper interface is placed between the VDRC and the processor. Proper signals needed by the VDRC to communicate with another processor are discussed in Chapter 6.

The VDRC also requires a NTSC standard composite sync signal as part of the input video waveforms if the PLC and VPC are to function properly. Equalization pulses as well as the horizontal and vertical pulses are used by the PLC to determine the proper pixel location at any given instant, therefore the proper sync signal must be supplied. A standard amplitude input video waveform is also required for the VPC in order to maintain the proper resolution of the information when it is reconstructed by the VRC. Appendix A contains a summary of video fundamentals, including definitions of standard sync signals and standard amplitude of the waveform.

2.4. Grey-Level Resolution

The A/D converter used in the VDRC provides an 8-bit binary representation of the sampled waveform. This representation allows a sample to have one of 256 possible grey intensity levels. According to previous studies, approximately 64 grey levels are required over the whole span of black to white to minimize false contouring, a condition caused by insufficient grey levels in the picture [3]. As can be seen in a comparison of the two numbers, the VDRC contains four times as many grey levels as needed to avoid the effects of false contouring in the reconstructed picture.

2.5. Spatial Resolution

The spatial resolution is determined by the sampling period (time between samples), T_s , used by the VSC and VRC. From the Nyquist sampling criterion, it follows that in order to avoid aliasing, the following condition must be satisfied:

$$T_s \leq \frac{1}{2 \times \text{Bandwidth}} \quad (2.5.1)$$

For a 4MHz video signal (see Appendix A), the maximum Nyquist sampling period is 125 nanoseconds. In practice, the choice of T_s should be well below this figure to minimize the effects caused by spatially-limiting the data.

The VDRC system has a 17.5 MHz master clock which is generated in the control circuit portion of the system. A 57 nanosecond minimum sampling period, T_s , is provided by this clock. This T_s is associated with choosing one video source with a sample rate of 928 points per horizontal line or two video sources with a sample rate of 464 points per horizontal line each. Doubling the sampling period, T_s , is equivalent to halving the sample rate. This rate would sample one video source at 464 points per horizontal line or two video sources at 232 points per horizontal line each. Tables 2.1 and 2.2 show comparisons of the sample rate and sampling period when one and two video sources are used, respectively. When two video sources are used, T_s is the time between sampled points of the same source. The following conclusion may be derived when the data presented in the tables is compared with the Nyquist sampling rate for video information. The waveform of a single video source must be sampled at the rate corresponding to either 928

TABLE 2.1

COMPARISON OF SAMPLE RATE TO SAMPLING PERIOD
FOR ONE VIDEO SOURCE

Sample Rate	Sampling Period (T_s)
928	57 nsec
464	114 nsec
232	228 nsec
116	456 nsec
58	912 nsec
29	1.824 μ sec

TABLE 2.2

COMPARISON OF SAMPLE RATE TO SAMPLING PERIOD
FOR TWO VIDEO SOURCES

Sample Rate	Sampling Period (T_s)	Points/Camera
928	114 nsec	464
464	228 nsec	232
232	456 nsec	116
116	912 nsec	58
58	1.824 μ sec	29

points per horizontal line or 464 points per horizontal line while sampling of two video source waveforms requires sampling at the rate of 464 points per horizontal line each if aliasing of the reconstructed output waveform is to be avoided, even though 256 points per horizontal line appears adequate to drive a standard television image [3]. Slower rates are provided to allow the user to be able to obtain more data points from a broader part of the incoming video in the same amount of time. These rates could be of significant use, due to the results of an investigation which showed that the histogram curve of a scene produced by sampling 512 points per horizontal line could be closely approximated by using a smaller number of samples per line [4]. This study showed that sampling at a rate as low as 32 points per horizontal line produced an accurate histogram when compared with the original histogram produced using 512 sampled points per horizontal line. Hence, the basis for allowing the sample rate to be as slow as 29 points per horizontal line. Other sample rates are available to allow intermediate sample rates of data for processing as well as allow the user to view the display at several stages of degradation.

When reconstructed, the display shows the number of pixels corresponding to the chosen sample rate in each horizontal line X 480 horizontal lines. This display is possible because the VDRC system operates on every horizontal line of video of the input waveforms. A standard closed-circuit television monitor is composed of 525 horizontal lines of video, but approximately 25 lines are lost due to the blanking of the vertical retrace from each field and the elimination of the half-

line of video at the beginning and end of the odd and even fields, respectively.

2.6. System Delay

The VDRC system has an inherent delay resulting from the various operations it must perform on the input video signal to produce the transformation desired. Throughput delay time encountered when sending video information through the VDRC is dependent on the sample rate used and whether one or two video sources are to be digitized, transformed, and reconstructed. Figures 2.2 and 2.3 show how the video data, once digitized, is sent through the system. The latching of the data in buffer registers at various locations through the system is done to insure that the information is properly transformed and no errors are introduced into the process from the operation of the VDRC on the video signal. Any delay introduced by the VDRC system to the video signal is negligible with respect to the standard video update rate of 30 frames per second. Therefore, the VDRC system is actually operating in real-time.

Figure 2.2 is the overall timing diagram of the VDRC system when one video source is sampled at a rate of 464 points or less per horizontal line. This figure traces a sample point, N , through the VDRC system from the output of the A/D converter to its reconstruction into its new analog value by the D/A converter. Sample rate period, T_s , corresponds to the values given in Table 2.1 for the sample rates of 464 points or less per horizontal line. Delay times shown in the figure correspond to the propagation delay times of the components used in

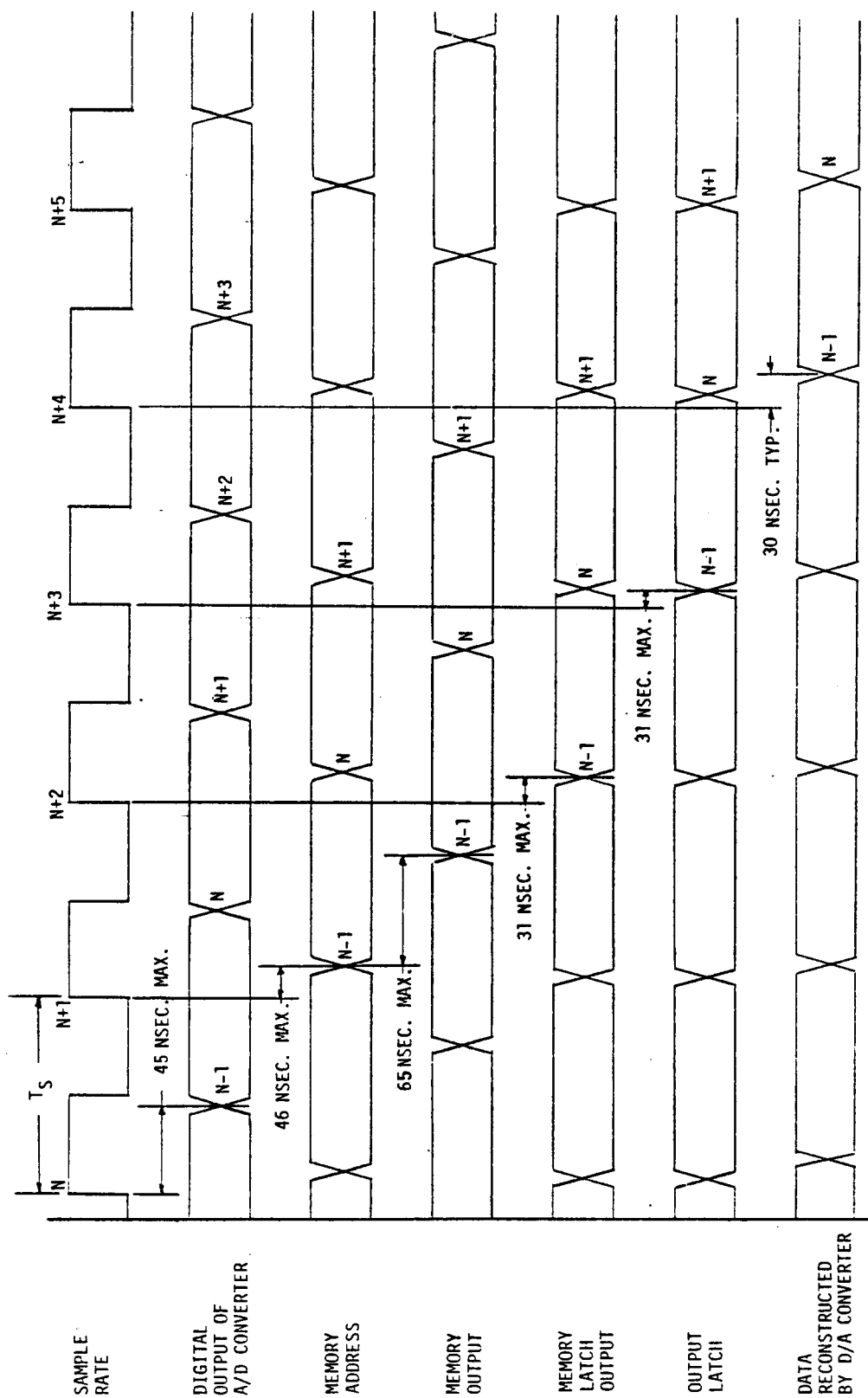


Figure 2.2. Overall timing diagram for the VDRC system sampling one video source less than the maximum rate.

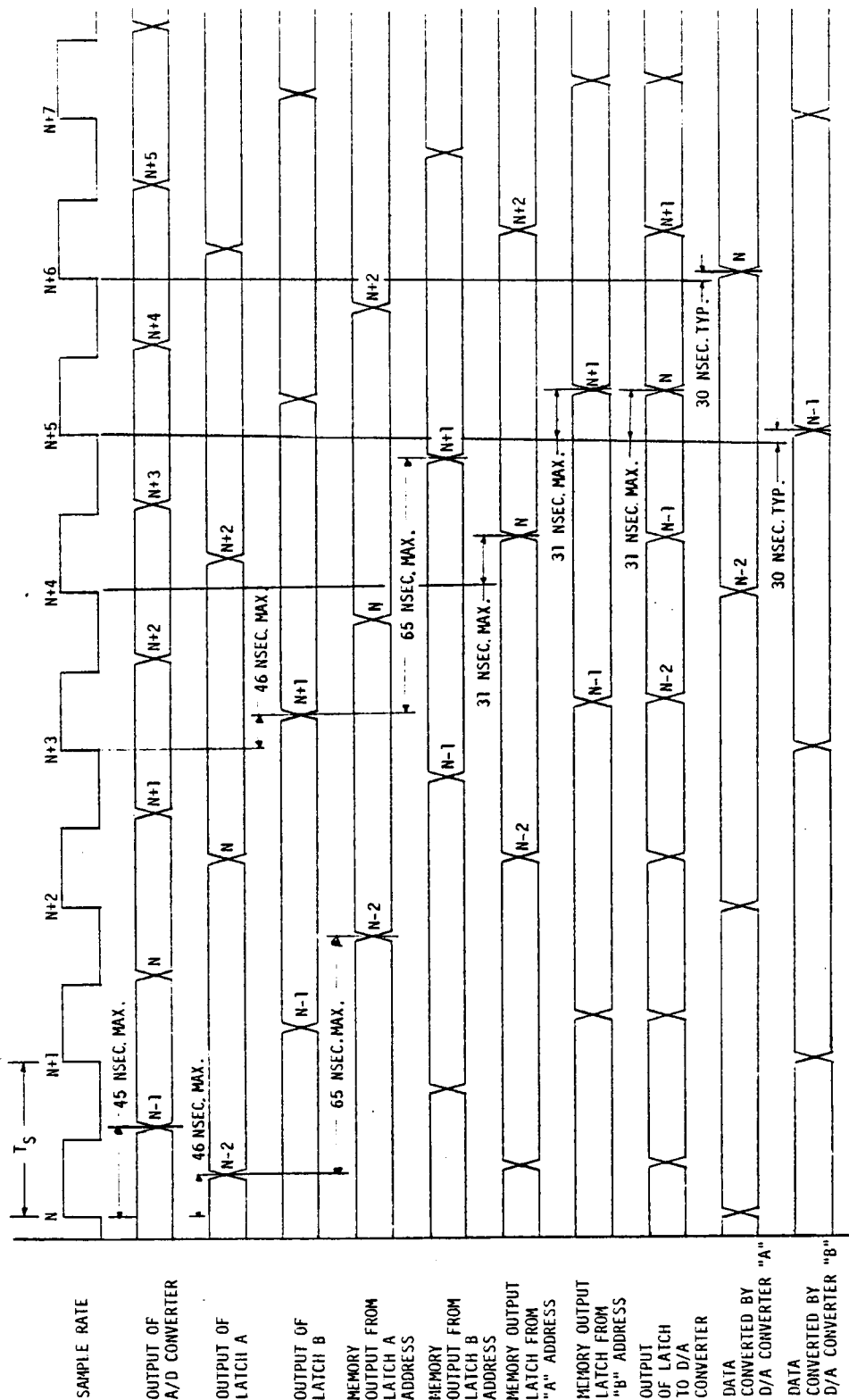


Figure 2.3. Overall timing diagram for the VDRC system sampling one video source at the maximum rate or two video sources at any sample rate.

the system. These delay values show the time elapsed between the sample rate pulse edge to initiate a data transfer and when the data transfer is complete. As an example, 46 nanoseconds are needed from the edge of the sample rate pulse initiating the transfer of data from the output of the A/D converter until the data is valid at the address inputs of the memory chips. Five sample periods are used to transform the data in this mode of operation as seen by tracing the sample point, N, through the figure. The A/D converter uses the equivalent of two delay periods since its method of conversion produces the digital representation of the previously sampled point when a new sample pulse occurs, i.e., when the pulse to sample point N is given, the digital representation of point N-1 is presented at the output of the A/D converter. The N+2 sample pulse clocks the output data of the A/D converter into the latch used to hold the memory address. Next, the N+3 sample pulse latches the output of the memory location addressed, which is the transformed data, into a memory output buffer. Sample pulse N+4 clocks the output of the DTMM being used for the transformation into the buffer used by the D/A converter for reconstruction. Finally, the N+5 sample pulse strobes the D/A converter to reconstruct the analog signal value corresponding to the transformed sample point, N, latched by the output buffer of the VDRC system.

Figure 2.3 shows the overall timing diagram for the VDRC system when one video source is sampled at a rate of 928 points per horizontal line or two video sources are sampled at any of the available rates. The transfer of data occurs using the same basic procedures as previously mentioned with the exception that the output of the A/D converter is alternately clocked into two latches to be used as the memory address.

The reason for this procedure is two fold: 1) it allows the upper and lower byte of the DTMM to be addressed by the two separate latches which is valuable since it permits two video sources to be transformed independently by transformation curves stored in the high and low bytes of the DTMM, and 2) it allows the VDRC system to run at a rate faster than the access time of the memory chips used in the DTMM since each byte of memory is only addressed by every other sample point. Thus the N , $N+2$, $N+4$, . . etc. sample points are clocked into latch A while the $N-1$, $N+1$, $N+3$, . . etc. sample points are clocked into latch B as shown in the figure. The same procedure as shown in Figure 2.2 and discussed earlier is used in each byte of the memory to transfer the data to the latches on the memory output. These outputs of the high and low bytes are then alternately clocked into the latch of the D/A converters. The D/A converters are alternately strobed to insure D/A converter "A" reconstructs the data latched by memory address latch "A" and D/A converter "B" reconstructs the data latched by memory address latch "B". This procedure thus assures the points sampled from video source A will be sent to monitor A and points from video source B sent to monitor B. Six sample periods are required to transfer the data from the A/D output to reconstruction by the D/A converter in this mode of operation. The transfer follows the same pattern as in Figure 2.2 except the data requires two sample periods to be transformed through the memory instead of one sample period due to the alternating of the high and low bytes of memory as previously described.

Tables 2.3 and 2.4 list the two basic modes of operation shown in Figures 2.2 and 2.3 and relate the delay times incurred when using any

TABLE 2.3

DELAY TIME IN THE VDRC SYSTEM
FOR ONE VIDEO SOURCE

Sample Rate	Delay Time (D_T)
928	350 nsec
464	570 nsec
232	1.14 μ sec
116	2.28 μ sec
58	4.56 μ sec
29	9.12 μ sec

TABLE 2.4

DELAY TIME IN THE VDRC SYSTEM
FOR TWO VIDEO SOURCES

Sample Rate	Delay Time (D_T)
928	350 nsec
464	700 nsec
232	1.4 μ sec
116	2.8 μ sec
58	5.6 μ sec
29	11.2 μ sec

of the sample rates in these modes of operation. As shown in the tables, the VDRC system has a delay time, D_T , in throughput processing of the video information corresponding to 350 nanoseconds at the fastest sample rate and 11.20 microseconds at the slowest sample rate of operation. These delays are equivalent to .05% and 17.6% of the time period of one horizontal line of video information, respectively, which may be considered real-time when compared to standard video update rates as previously mentioned.

Due to the fact that the information signal is being transformed with varying degrees of delay, the composite sync signal must be delayed an amount corresponding to the delay introduced by the system to insure the proper reconstruction of the composite output video waveform by the VRC. The delay in the composite sync is inserted by the VPPC and adjusted according to the sample rate and the number of video sources sampled by the system. This process will be described further in Chapter 5.

2.7. Rate of Storage of Sampled Points

The VDRC system is designed to give the processor the capability of requesting one of the two DTMM's for storage of sampled data. The processor can request any even number from 2 points up to 464 points from a horizontal line be stored. This storage will occur at a faster rate than the processor could transfer the data if the DTMM was not used as a buffer memory. When all the sample points requested are stored in the DTMM, the processor may move the points from the DTMM to the processor memory at a slower rate using processor controlled commands to accomplish

the transfer. In this manner, only the points desired from the digitized video information are sent to the processor memory.

Using the LSI-11 MOV instruction to transfer the stored data, it is possible to calculate how fast a complete video picture may be placed in the processor memory under computer control. The MOV instruction takes six microseconds to transfer a 16-bit word from one memory location to another location [5]. Since the sampled data is in 8-bit bytes, this instruction can be used to transfer two stored points at once and reduce the transfer time to less than one-half of the time needed if each point was moved independently.

To store a 464 points per horizontal line picture, the VDRC samples at the 464 points per horizontal line rate. Starting on line 0, the first line of 464 points is sampled and stored in the DTMM. Since two points are moved at a time, the processor issues 232 MOV commands to transfer the data. The total time needed to move the points is 1392 microseconds, or 21.9 horizontal lines. Since part of a line is used to transfer the last part of the sampled data, the VDRC selects the next full horizontal line of video. Line 46 is the next line requested for storage. This process continues until the end of the field. The next line to be sampled and stored would be line 1 in the next field since one field contains the even lines and another contains the odd lines of an interlaced video signal. Line 47 would be next and continuing to the end of this field. Then the next line of the new field would be line 2, then line 48, and so on. Continuing this pattern results in the entire 464 X 480 lines being stored in a time interval equal to 23 television frames, or .77 seconds.

The same basic procedure is used to store a picture sampled at a slower rate. The time required to move the points from the DTMM to the processor is calculated as the sample rate multiplied by one-half the number of points to be moved. Division by 63.5 microseconds, the horizontal line scan rate, results in the number of lines needed to transfer the points. This number raised to the next whole number and added to the last line sampled and stored gives the next line to be sampled and stored in the DTMM up to line 479, the end of the field. Table 2.5 gives the different size arrays the VDRC can be programmed to sample and store along with the time needed for a full array to be loaded in the processor memory under processor control using the DTMM as a buffer memory. Only one video source may be sampled and stored when two sources are digitized. The values listed in Table 2.5 are plus or minus one frame of video since the location of the sampling process in the input video signal is not known when the initial start signal is given.

TABLE 2.5

TYPICAL SIZE ARRAYS THAT THE VDRC
CAN BE PROGRAMMED TO STORE

Array Size	Frames	Time
464 X 480	23	.77 sec
232 X 240	12	.400 sec
116 X 128	2.5	.0833 sec
58 X 64	1	.033 sec
29 X 32	1	.033 sec

CHAPTER 3

DATA ACQUISITION

As described in Chapter 2, the video information is passed from input to output of the VDRC system along the Video Sample Bus (VSBUS). Information signals from the video sources must be properly conditioned and converted to their digital representation before they can be placed on the VSBUS and used by the remainder of the VDRC system. The Video Pre-processing Circuit (VPC) and Video Sampling Circuit (VSC) together perform these required operations.

3.1. The Video Pre-processing Circuit

The primary function of the VPC is to accept the analog input signal from a video source and condition the signal to obtain the proper waveform required by the VSC for sampling. A standard composite video signal of 1.4V peak to peak (1V of video information combined with 0.4V of composite sync information), discussed in Appendix A, is accepted by the VPC. Amplifier A1, shown in Figure 3.1, is the first stage of the VPC. The input resistance of A1 is

$$R_{IN} = 51 \text{ ohm} \parallel 4K \approx 50 \text{ ohms} \quad (3.1.1)$$

which provides the proper termination for a 50 ohm coaxial video cable. A differential video amplifier is used for this stage. This type of amplifier allows both the amplification of the waveform to the proper magnitude and inversion of the waveform to produce a positive composite video signal, discussed in Appendix A. This procedure is required because the analog-to-digital (A/D) converter used in the VSC works with

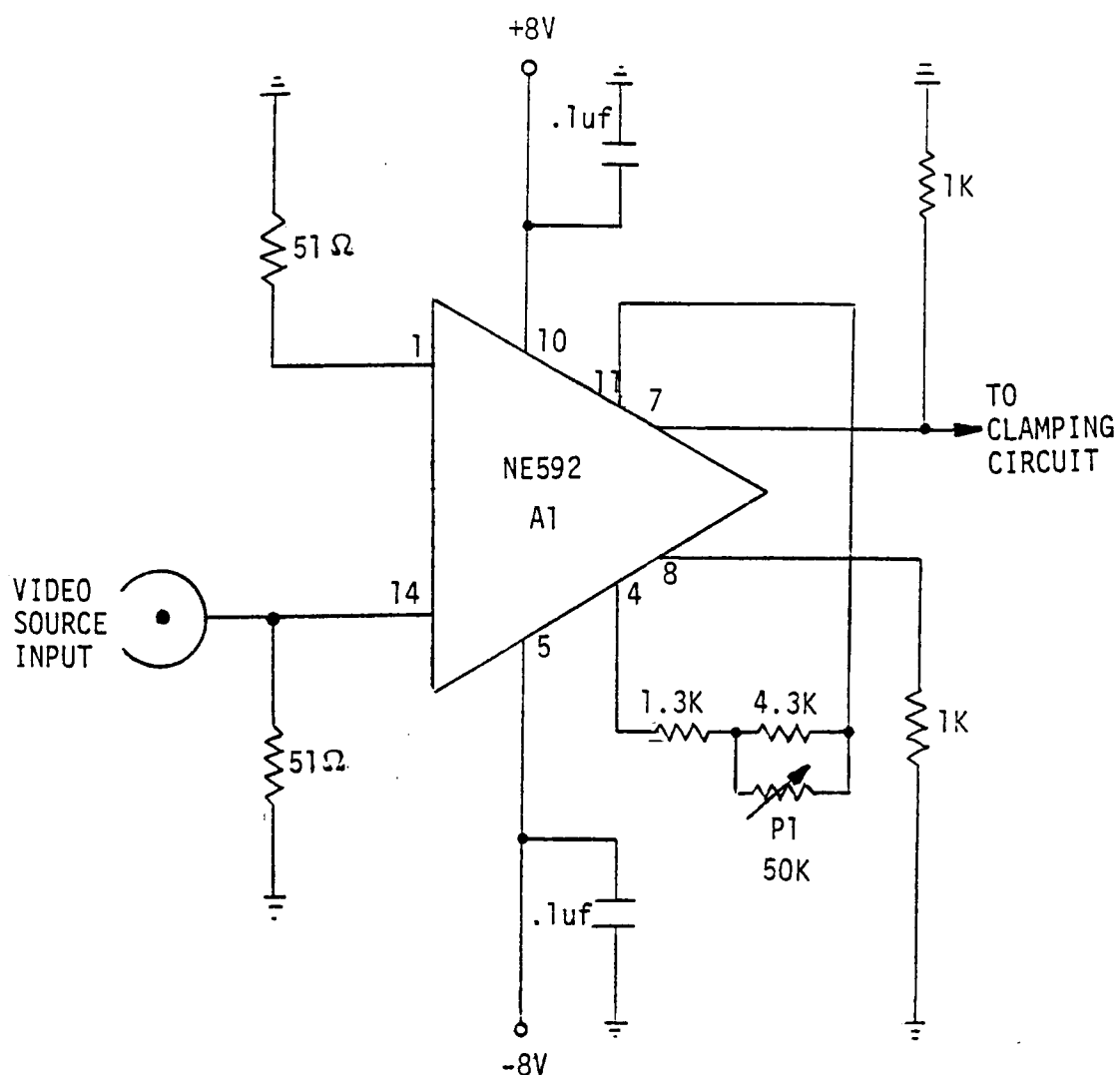


Figure 3.1. The input video amplifier of the VPC.

a 0V to -2V input range. Amplifier A1 produces a gain of approximately -2.3 and may be adjusted by the potentiometer, P1, shown in the figure to produce an information signal of 0V to -2V at the input of the A/D converter from each video source.

The amplified, inverted video waveform is then sent from the video amplifier to the video clamping circuit shown in Figure 3.2. These circuits are AC coupled to allow the clamping circuit to use DC feedback to perform its operation. A 100 microfarad capacitor used in the coupling provides good low frequency response and helps remove tilt that is sometimes in the vertical retrace of an input video signal. The clamping circuit employs a PNP-NPN emitter follower pair, Q1 and Q2, which allows the DC voltage at the input of Q1 to be closely reproduced on the emitter of Q2. A power transistor used as Q2 also provides the current needed to drive the 120 ohm input impedance of the next stage. The output signal is also filtered by the RLC circuit shown in the figure and then sent to the negative input of the CA3080 operational transconductance amplifier (OTA). A low pass RLC filter is employed to remove the color subcarrier from the video signal, if a color signal is input, and allow only the DC value of the video signal to be sent to the input of the OTA. The positive terminal of the OTA is connected as shown in the figure through a 3K ohm resistor to potentiometer, P2. Proper setting of the DC reference value desired for the back porch is done using this potentiometer. The clamping circuit then shifts the DC value of the back porch of the video waveform to match this reference voltage. Used as a comparator, the OTA relates the difference between the desired DC reference value and the back porch of the video signal when pulsed by the

clamp sampling pulse, CSPULSE. CSPULSE occurs during the back porch of each horizontal line scan and its generation will be discussed later in this section. The difference detected by the OTA is then stored in the RC combination of 1000 picofarad and 1K ohm shown in the figure. A 100K ohm and 100 picofarad combination is used to provide phase compensation of the error voltage. This error voltage is then sent to the gate of a FET source follower stage, Q3. This stage provides isolation of the error voltage stored from the input of Q1 by producing a high impedance input. It also provides a low output impedance so that the base of the transistor, Q1, will not be loaded. The error voltage sensed by the OTA is transmitted through Q3 and then current summed with the video signal at the base of Q1 to correct the back porch DC voltage level and place it at the desired reference value. This DC feedback loop is stable because the gain of the OTA through the source follower, Q3, is greater than one. Since the gain of the emitter follower stages is approximately one, this generates an overall loop gain for the clamp circuit of greater than one which produces stability in the loop. Figures 3.3(a) and 3.3(b) show the video input waveform to the VDRC system and the waveform at the output of the clamping circuit, respectively.

The video signal in the clamping circuit which has had the color subcarrier filtered out, if a color signal is used, is also sent to the sync separation circuit shown in Figure 3.4. This circuit performs the operation of reproducing a composite sync signal from the composite video signal which is compatible with standard TTL logic. Two active rectifiers are used which clip a portion of the composite video signal passing through the circuit. Outputs of the first and second rectifiers

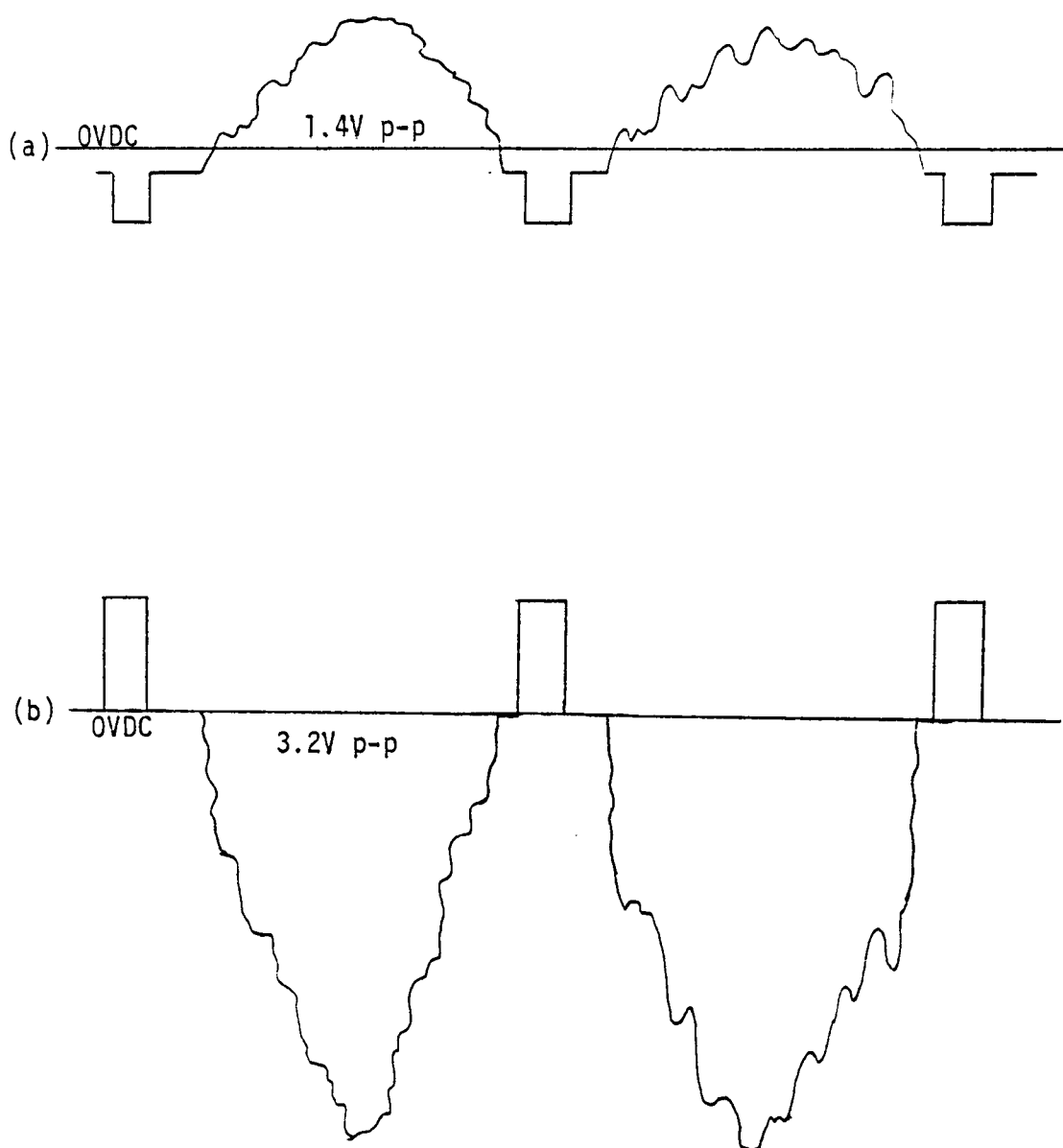


Figure 3.3. Waveforms associated with the input video amplifier and video clamping circuit.

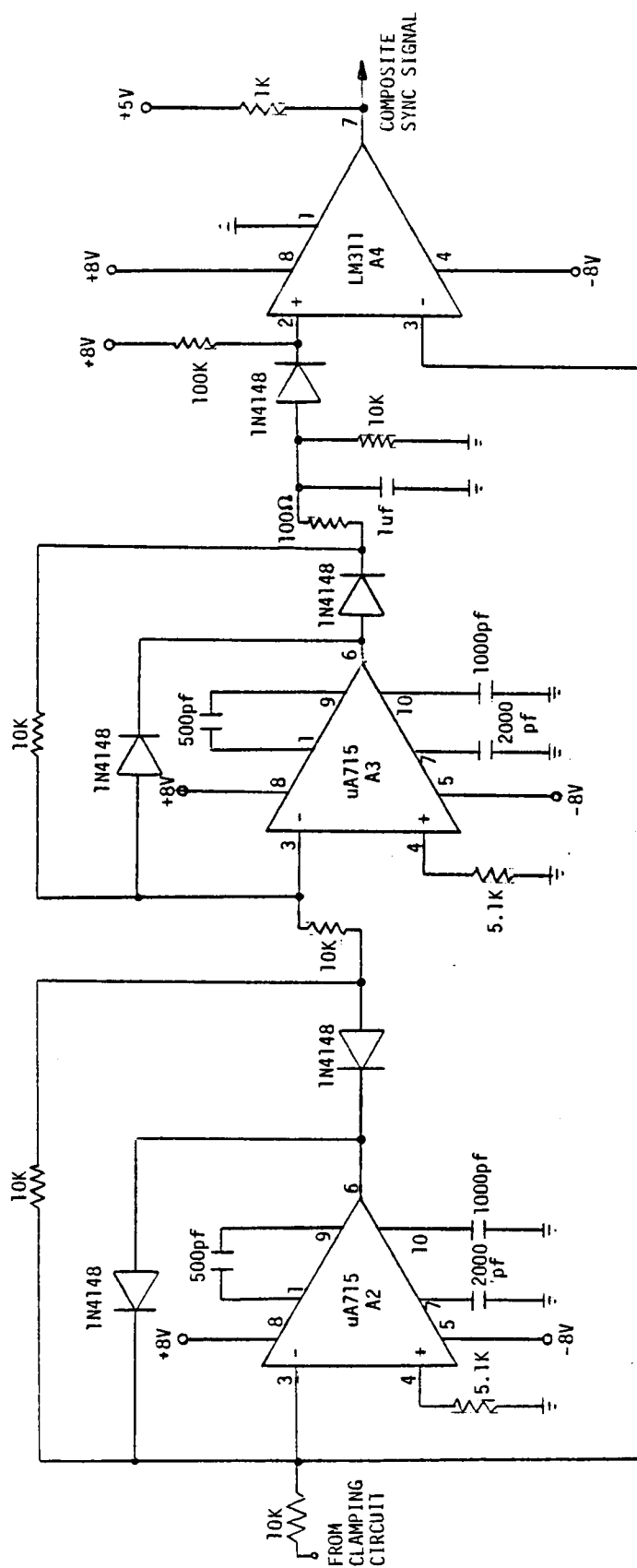


Figure 3.4. The sync separation circuit.

are shown in Figures 3.5(a) and 3.5(b), respectively. The output of the second rectifier is then sent through a diode to an RC network which acts as a peak level indicator. It stores the peak value of the signal presented to it. A voltage drop of approximately 0.6V is produced in the signal by the diode. The time constant of this storage circuit is one millisecond which is much longer than the time of 63.5 microseconds for one horizontal line. Since the peak value will occur every horizontal line, this time constant allows the storage circuit to hold its value and not "droop" or discharge an appreciable amount before a new peak value occurs. The output of the RC storage element after the diode voltage drop is shown in Figure 3.5(c). This peak value is then placed on the positive input of the comparator shown in Figure 3.4. The composite video signal which was placed at the input to the first active rectifier is placed on the negative input of the comparator. A comparison of these two signals produces an output near a DC value of 0V when the composite video signal on the negative input exceeds the peak detector value on the positive input. When the video signal value is less than the peak detector value, the comparator output is "pulled up" to 5V by the 1K ohm resistor connected to +5V. Thus a composite sync signal is produced from the composite video input signal which is TTL compatible to be used by the digital logic in the system. Figure 3.5(d) and 3.5(e) show the comparison made by the comparator and the resultant output, respectively.

The composite sync signal is then sent to the circuit shown in Figure 3.6. This circuit consists of two 74123 monostable multivibrators or "one-shots" and is used to produce the clamping sample pulse,

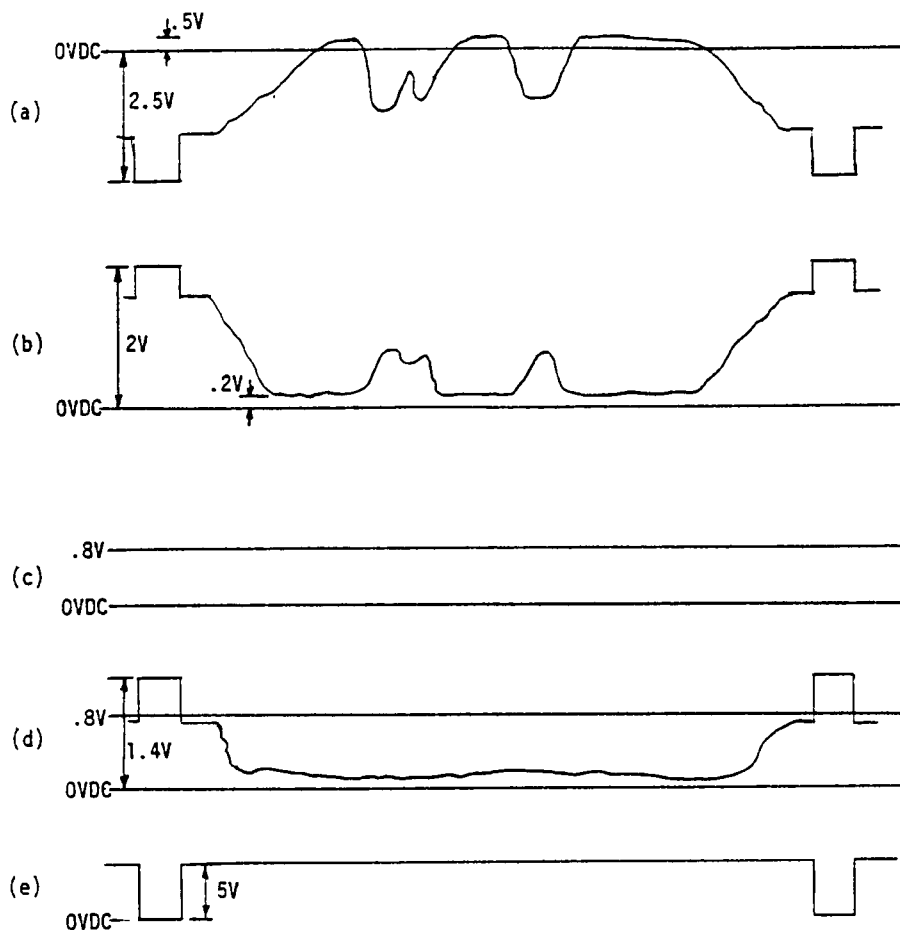


Figure 3.5. Waveforms associated with the sync separation circuit.

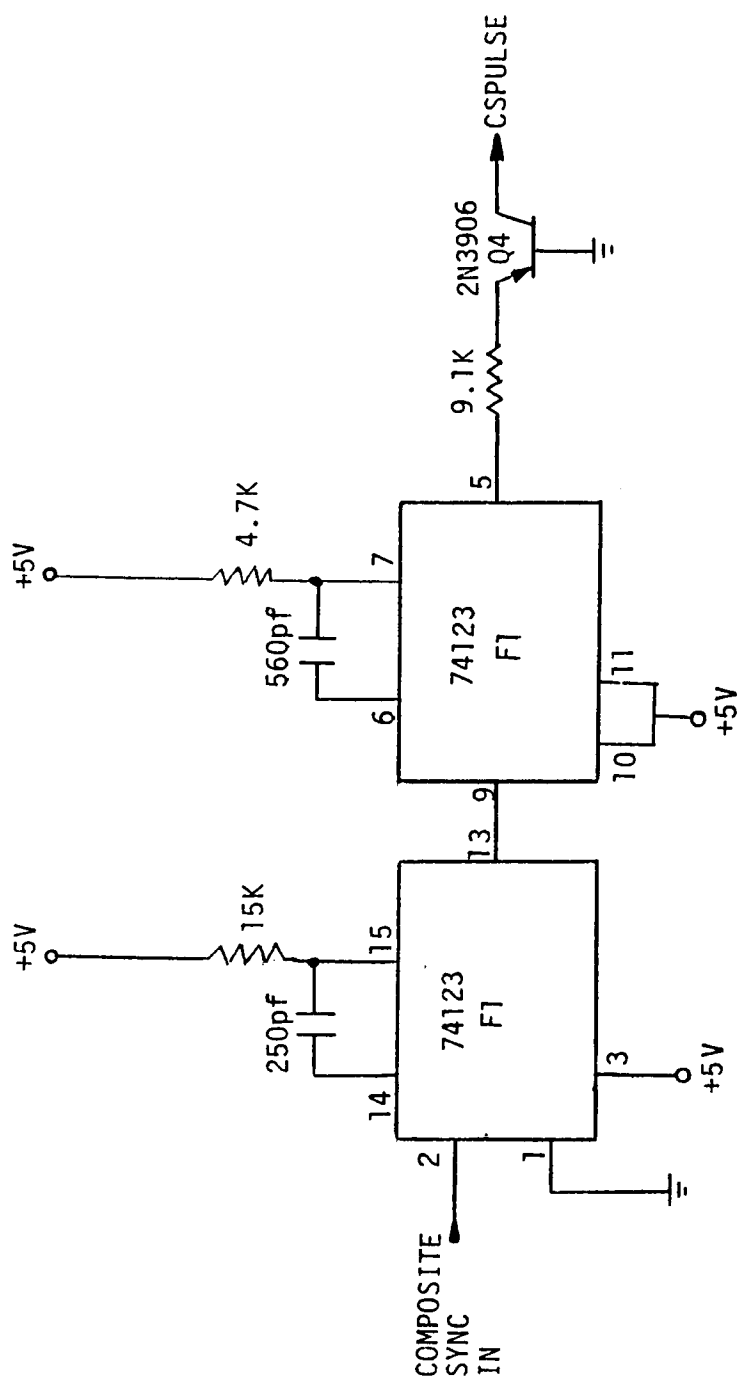


Figure 3.6. The clamp pulse generation circuit.

CSPULSE, used by the clamping circuit as mentioned earlier. The first multivibrator produces a time delay of one microsecond from the trailing edge of the composite sync signal, as shown in Figure 3.7(b), insuring the output produced by the next multivibrator will be in the middle of the back porch of the video waveform. This second pulse is timed to last for a 0.8 microsecond duration, as shown in Figure 3.7(c). Transistor Q4, shown in Figure 3.6, then uses this pulse to produce CSPULSE in the form of a current pulse required by the OTA of the clamping circuit to sample the error voltage as discussed earlier in this section.

A separate VPC circuit is used for each input video source. The clamped, amplitude adjusted video signal and the composite sync signal from each VPC are then sent to the Video Sampling Circuit (VSC).

3.2. The Video Sampling Circuit

The primary function of the VSC is to accept the video waveforms from the VPC, select the proper one to be sampled, and convert this sample to its digital representation to be placed on the Video Sample Bus (VSBUS). Selection of the proper composite sync signal to be used by the remainder of the VDRC system from the sync signals generated by the two VPC circuits is also done by the VSC.

The proper video waveform to be sampled is selected using the switching configuration shown in Figure 3.8. These switches are SD215 DMOS analog switches and are activated by the control lines, CAMSEL A and CAMSEL B, generated by the control circuit. Generation of these control signals is discussed in Chapter 7. The switches work by producing a high impedance or low impedance to the input video waveforms when each switch

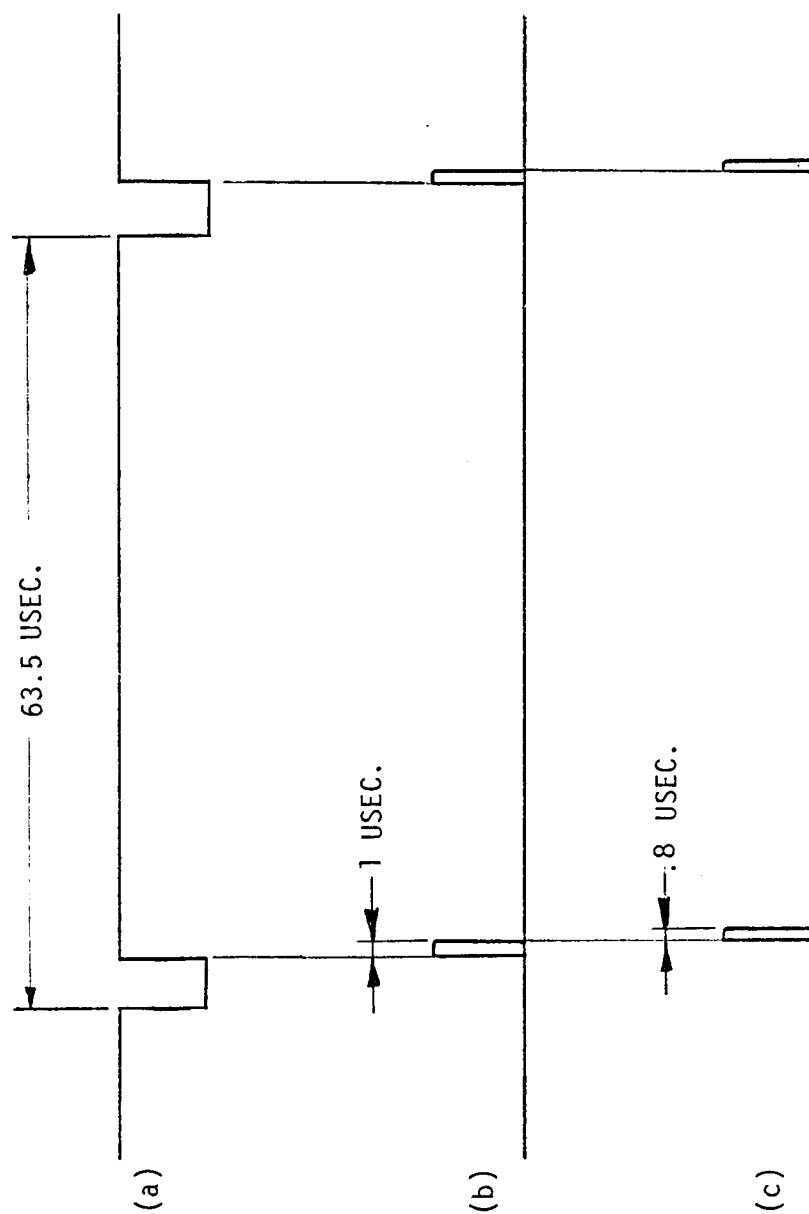


Figure 3.7. Waveforms associated with the clamp pulse generation circuit.

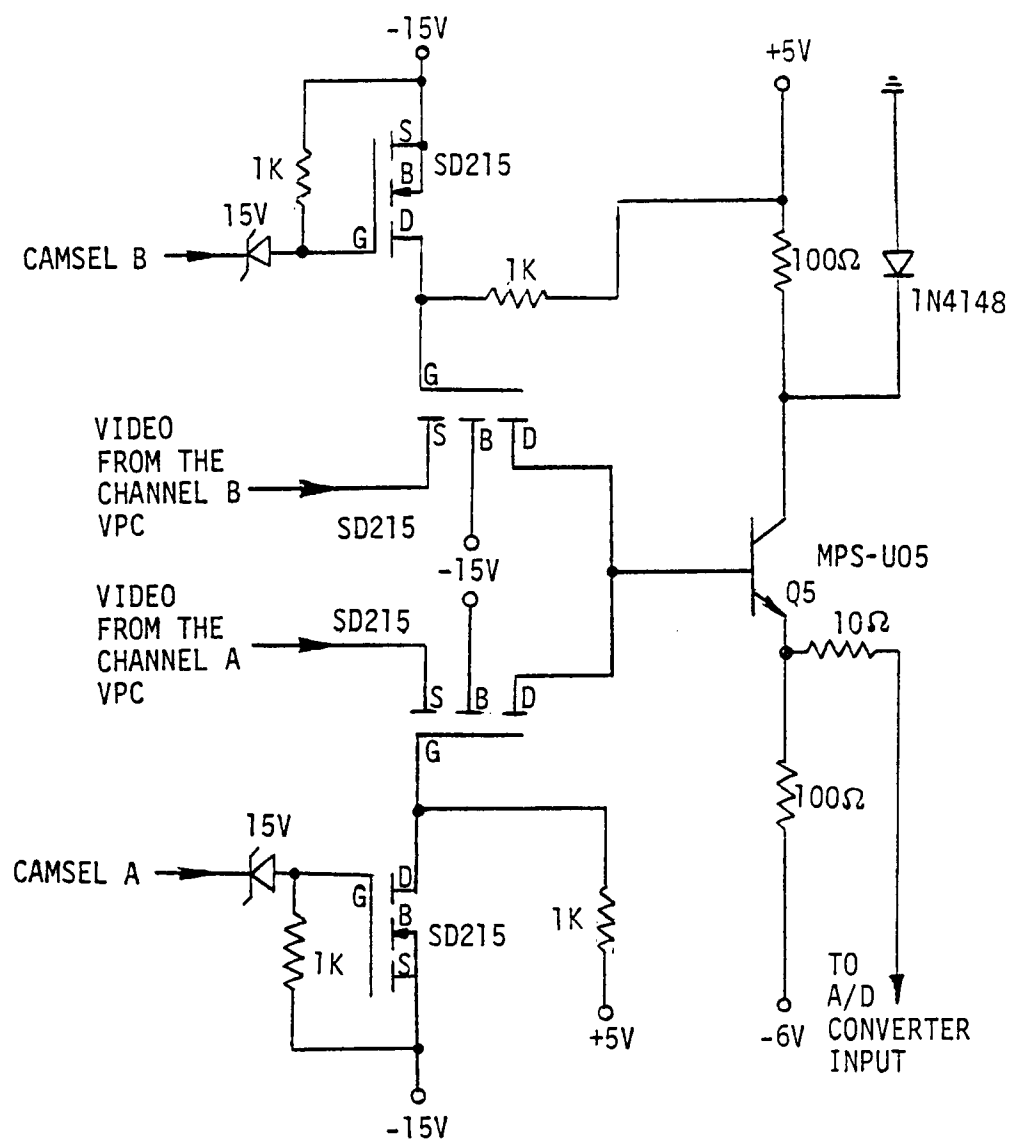


Figure 3.8. The analog sample selection circuit.

is turned off or activated, respectively. A high impedance causes the waveform to be stopped and not transmitted through the switch while a low impedance allows the signal to be transmitted with little loss in the video signal induced by the switch. When the control signal is low, the gate voltage of the driver is sent to -15V , thereby causing a gate-to-source voltage of 0V and causing this driver to be shut off. This condition produces a high impedance across the driver from drain-to-source causing its drain and also the gate of the analog switch to have a voltage of approximately $+5\text{V}$. Since the video waveform at the source never exceeds $+1\text{V}$, a gate-to-source voltage of at least 4V is always maintained, thus keeping the switch in the low impedance mode of operation and allowing the waveform through to the next stage of the VSC. When the control line is high, the gate voltage of the driver is placed at approximately -10V . This condition produces a gate-to-source voltage of $+5\text{V}$ and allows the driver to be activated. This condition produces a low impedance across the drain-to-source of the driver causing its drain and also the gate of the analog switch to be placed at approximately -11V . This voltage results in a gate-to-source voltage which is always negative since the input video waveform never reaches a negative value of more than -2.5V , and thus the switch is effectively cut off. These switches are designed to run at fast rates with a turn-on time of 0.9 nanoseconds and turn-off time of 14.0 nanoseconds, thus allowing the VDRC system to switch between the two video input waveforms with no loss or error due to switching delay.

After the proper video waveform is selected by the analog switches, it is sent through the buffer amplifier, Q5, also shown in Figure 3.8.

It is used to provide the current needed to drive the high capacitive input of the A/D converter used in the VSC and also to produce a low source resistance for the converter. This amplifier is a common-collector stage with a gain of slightly less than unity which is one reason the VPC needs to produce a gain of slightly more than -2 to allow a video waveform amplitude at the input of the A/D converter of 0V to -2V.

The diode in the collector of the amplifier clips the input waveform at +0.6V and thus protects the input of the A/D converter from receiving a positive input greater than its rated value. The output of the buffer amplifier is now properly adjusted so that the black level is set to 0V DC and the amplitude of the video information signal has a peak value of -2V.

The VSC also takes the composite sync signals generated in each VPC and selects the proper signal to be sent to the remainder of the VDRC system. This selection is based on the mode of operation the processor chooses for the VDRC. The composite sync signal from video source A is transmitted to the remainder of the VDRC for all modes of operation except the one case of video source B being the only video signal sampled. For this case the composite sync signal from video source B is used by the system. Selection is controlled by the circuit shown in Figure 3.9. The circuit is controlled by the CAM B L line generated in the control circuit discussed in Chapter 7. This signal is low only when the B channel of input video is the only source selected to be sampled, thus causing the B channel composite sync signal to be transmitted in this mode and the composite sync signal from the A channel to be selected for all other sampling modes.

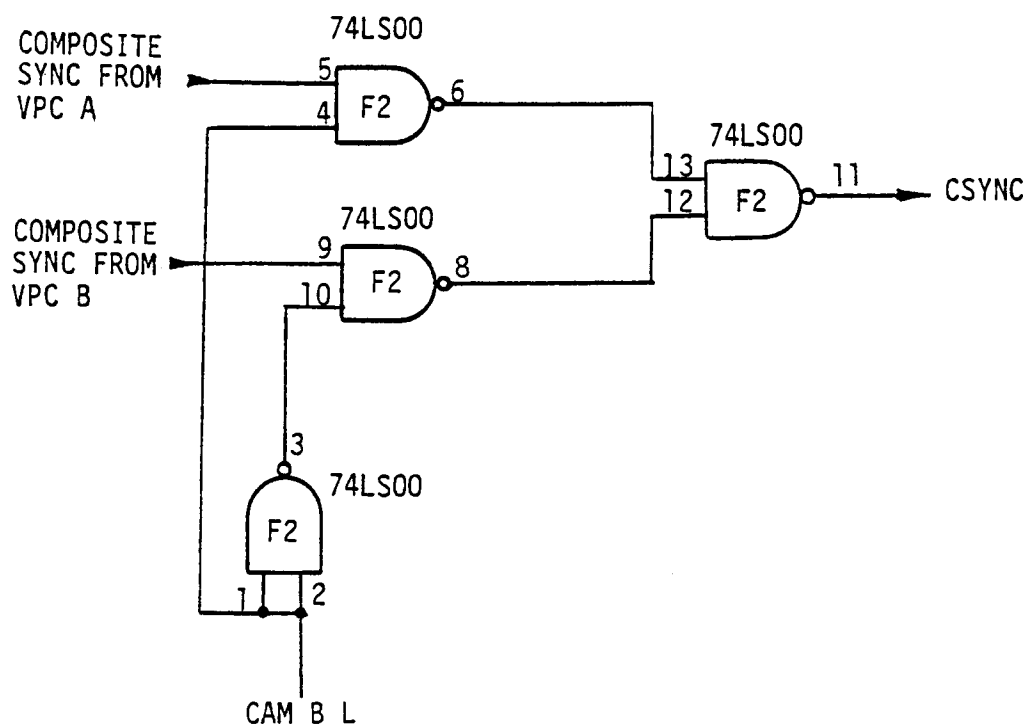


Figure 3.9. The composite sync selection circuit.

Actual performance of the sampling process and conversion of the sampled point to its digital representation is accomplished in one single integrated circuit chip. The VDRC system uses the A/D converter, TDC1007J, manufactured by TRW. This device is an 8-bit "fully-parallel flash" converter capable of digitizing an analog waveform at rates up to 30 megasamples per second with no external sample and hold circuit required. The VDRC system has a maximum sample rate of 17.5 megasamples per second, which is well within the capabilities of the converter. This A/D converter has a linearity error of 0.2% when used at the sample rates employed by the VDRC system which is equivalent to $\pm 1/2$ LSB. Its transient response is typically 20 nanoseconds for a full step input recovery which is helpful in the sampling of two video sources simultaneously, since the converter must switch to a new video source and lock on to its analog value before the sampling process can take place accurately. An analog input range of 0V to -2V, as mentioned earlier, is used with 0V being equivalent to total black. A resolution given by the A/D converter of 8 bits or 256 grey levels is more than adequate for proper contrasting, as discussed in Chapter 2. An aperture delay of typically 10 nanoseconds also aids in the fast switching process needed when stereo processing is done. Figure 3.10 shows the pin configuration and connections needed by the TDC1007J chip [6].

The sampling of the video source and conversion to its digital representation is controlled by the SAMPLE line generated in the control circuit discussed in Chapter 7. Every 0 $\rightarrow$ 1 transition of the SAMPLE line causes the A/D converter to sample the analog input waveform. After the

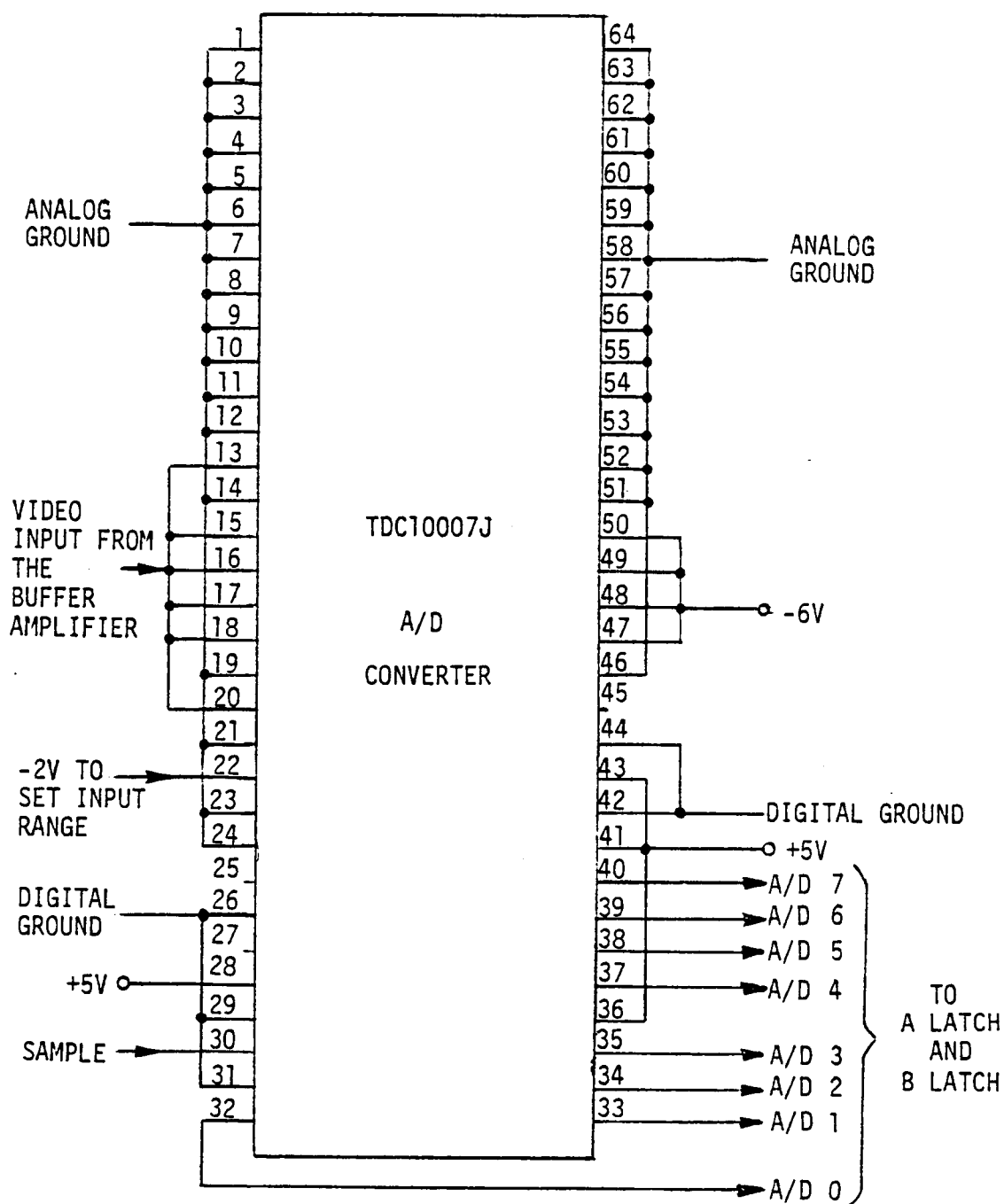


Figure 3.10. The A/D converter pin assignments.

typical delay of 30 nanoseconds, the digital representation of the previously sampled analog point is placed at the output of the A/D converter. An output of 000_8 corresponds to total black and 377_8 corresponds to total white from the sampled video source. The A/D converter, in essence, "runs" one point behind itself in the sampling process.

This procedure is shown in more detail in Figure 3.11.

The digital representation of the sampled analog point placed on the output of the A/D converter is then clocked into one of two latches depending upon the speed of sampling and whether stereo processing is taking place. The latches, ALATCH and BLATCH, are shown in Figure 3.12 and are clocked by ALATCH CLK and BLATCH CLK, respectively. If the maximum sampling rate for a single video source or any stereo processing is done, the digital data is alternately clocked into the two latches. In the single video source mode at the maximum rate, both latches are needed to allow adequate time for the data to be mapped in the Digital Transformation Mapping Memory (DTMM) discussed in Chapter 4. When stereo processing is done at any sample rate, the two latches are used to allow the data from each video source to be transmitted through and mapped by separate transformation curves stored in the DTMM. The process of selecting the digital data from the appropriate analog video source to be clocked into the ALATCH is determined by the mode of operation of the system. If video sources A and B are sampled with video source A also having the capability of having sample points stored by the other DTMM for processor use, video source A is clocked into ALATCH and video source B is clocked into the BLATCH. However, if video sources A and B are sampled with video source B having the capability of having sample points

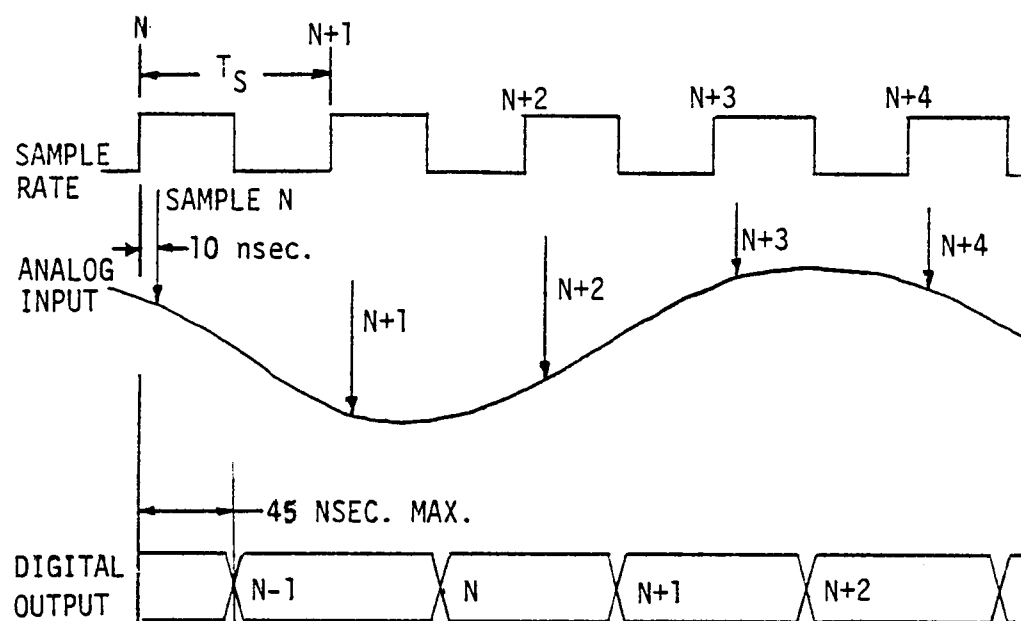


Figure 3.11. Timing diagram of the A/D converter.

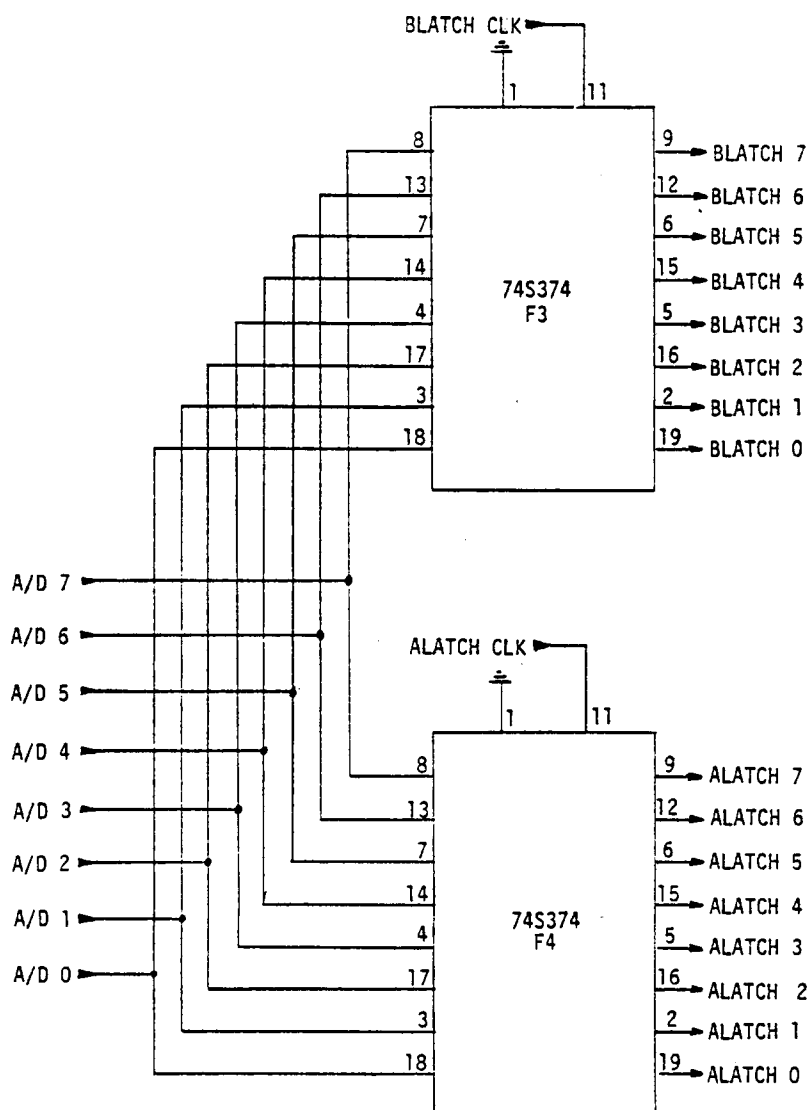


Figure 3.12. Output latches of the A/D converter.

stored in the other DTMM, video source B is now clocked into the ALATCH and video source A is clocked into BLATCH. Thus, whichever sampled video source is also able to have sample points stored for use by the processor is clocked in the ALATCH. When one video source is sampled at any rate slower than the maximum rate, only the ALATCH is used to latch data and send it to the rest of the VDRC system. The latch clocks are generated by the control circuit discussed in Chapter 7. The output of the latches, ALATCH 0 through ALATCH 7 and BLATCH 0 through BLATCH 7, are sent to the DTMM which will be discussed in the next chapter.

Figure 3.13 shows the proper sequence of latching the digital representation of the sampled analog signals for the case of a single video source at the maximum rate. Figure 3.14 shows the proper latching sequence for the example of video sources A and B sampled in stereo with A also having the capability of having sample points stored in the DTMM.

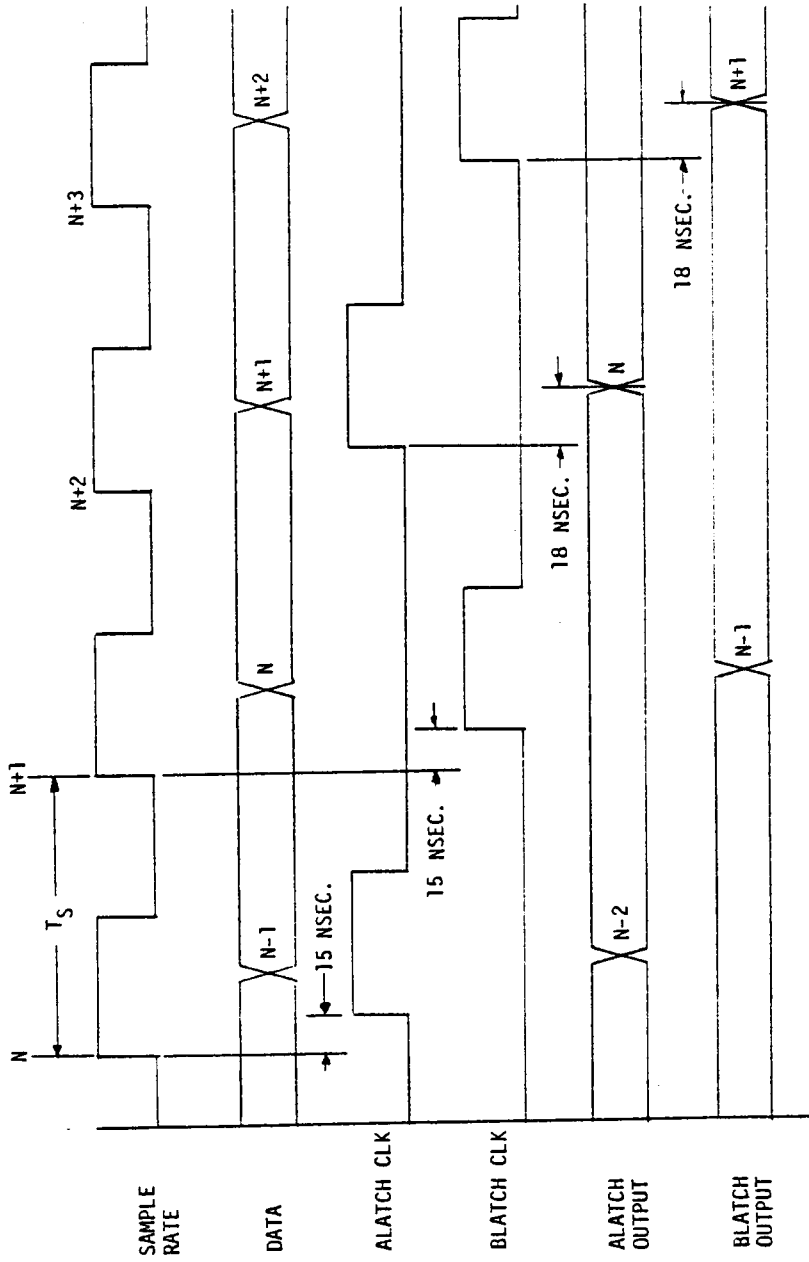


Figure 3.13. Timing diagram for the output latches for a single video source sampled at the maximum rate.

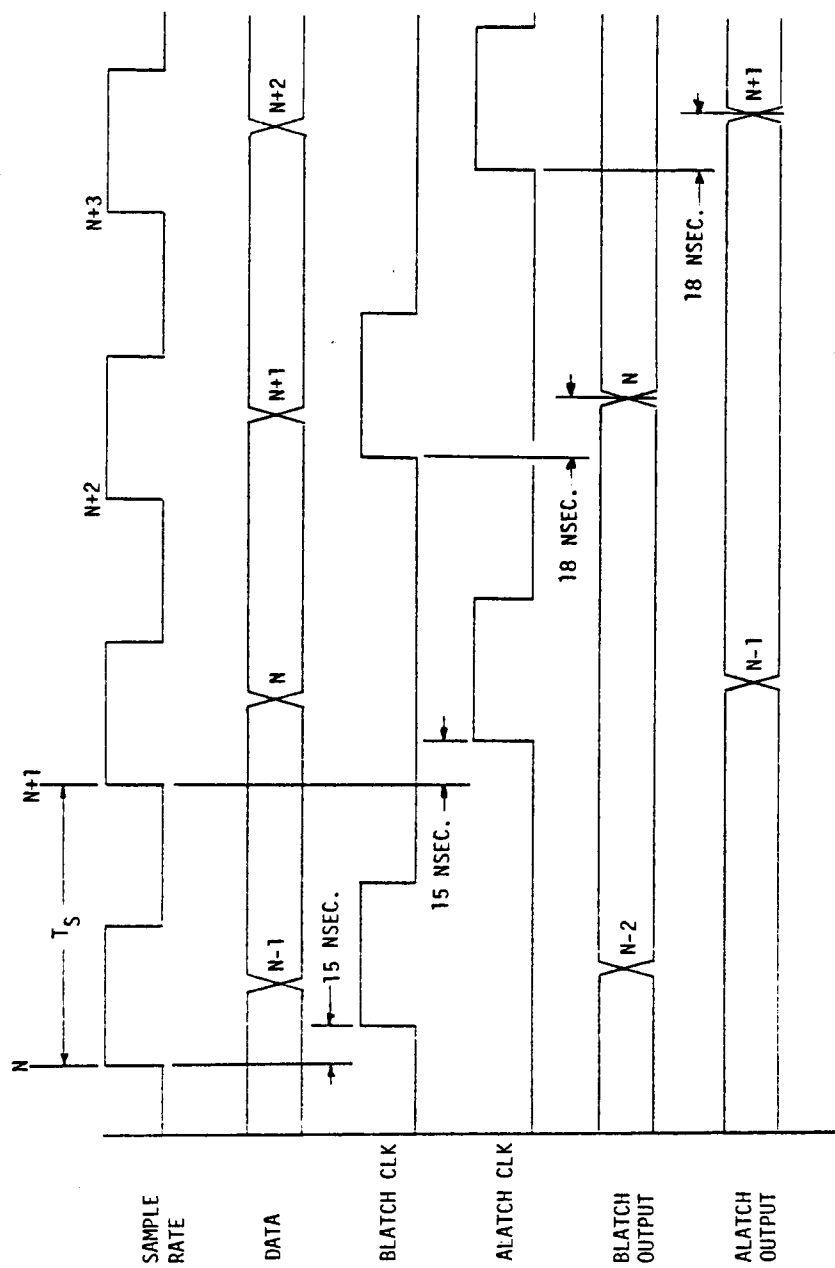


Figure 3.14. Timing diagram for the output latches for stereo sampling with video source A also capable of having points stored.

CHAPTER 4

THE DIGITAL TRANSFORMATION MAPPING MEMORY

The Digital Transformation Mapping Memory (DTMM) is used by the VDRC system to perform a transformation on the digitized video signal and to store sampled data points, as discussed briefly in Chapter 2. The DTMM is composed of 8K of random access memory (RAM) with 4K of RAM used in each side of the DTMM. Both sides of the DTMM are structured identically so the discussion and figures used in this chapter will refer to only one side of the DTMM with any control signals unique to one side shown and discussed. Since only one DTMM is addressable by the processor at a time, the same address is used for both sides of the DTMM. A bit in the control register selects which side of the DTMM is addressed, as discussed in Chapter 7.

4.1. Basic Arrangement

Each side of the DTMM uses four Fairchild 93L412 256X4 bit RAM chips arranged to form a 256X16 bit array, as shown in Figure 4.1. This memory was chosen due to the fast maximum address access time of 65 nanoseconds and low power consumption when compared with the speed of operation.

The memory address lines, MAD 0 through MAD 15, are received from the four 74LS157 multiplexers shown in Figure 4.2. These multiplexers are needed because the DTMM is addressed by the digitized signal and also the processor. The signals, MSEL 0 and MSEL 1, from the control circuit determine which side of the DTMM is addressable by the processor. When the DTMM is used as a buffer register for sampled data, the same address

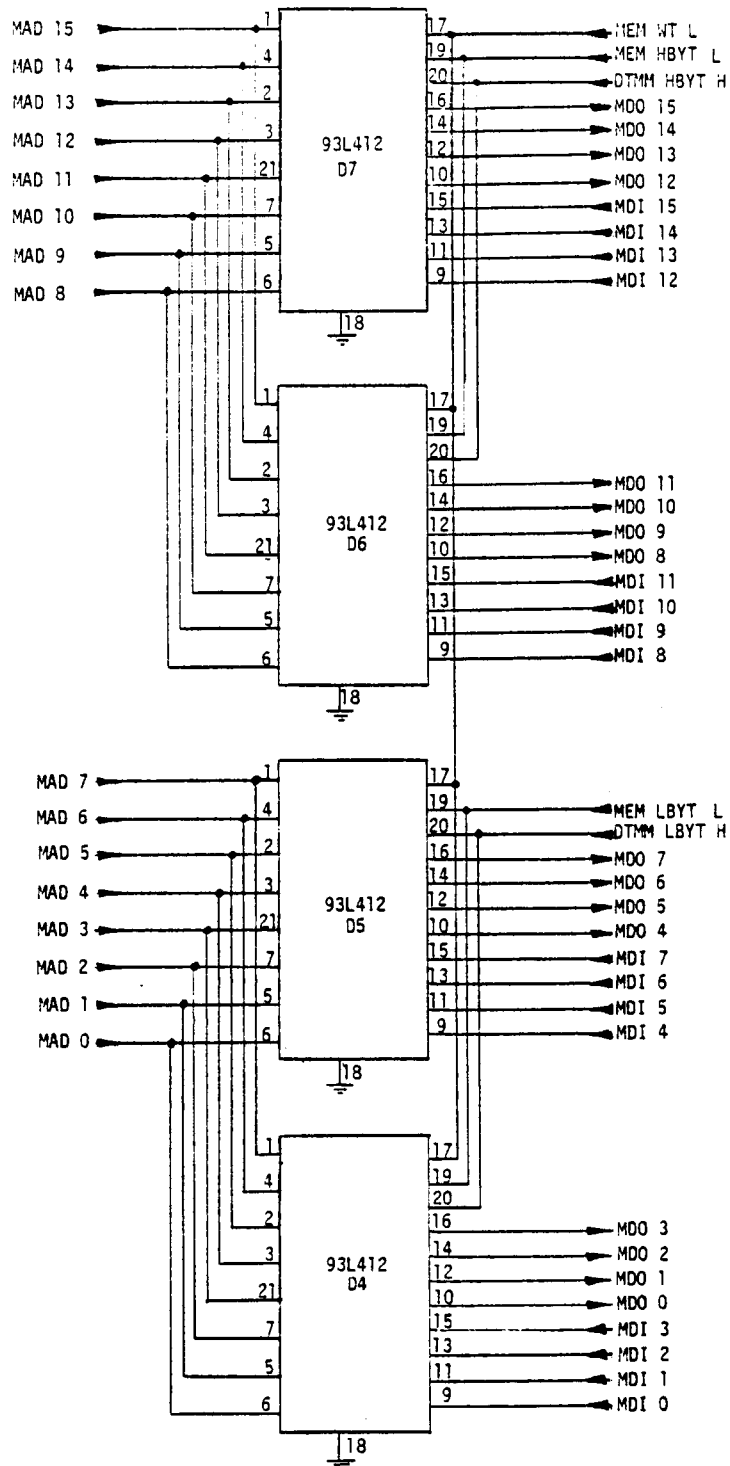


Figure 4.1. The DTMM memory structure.

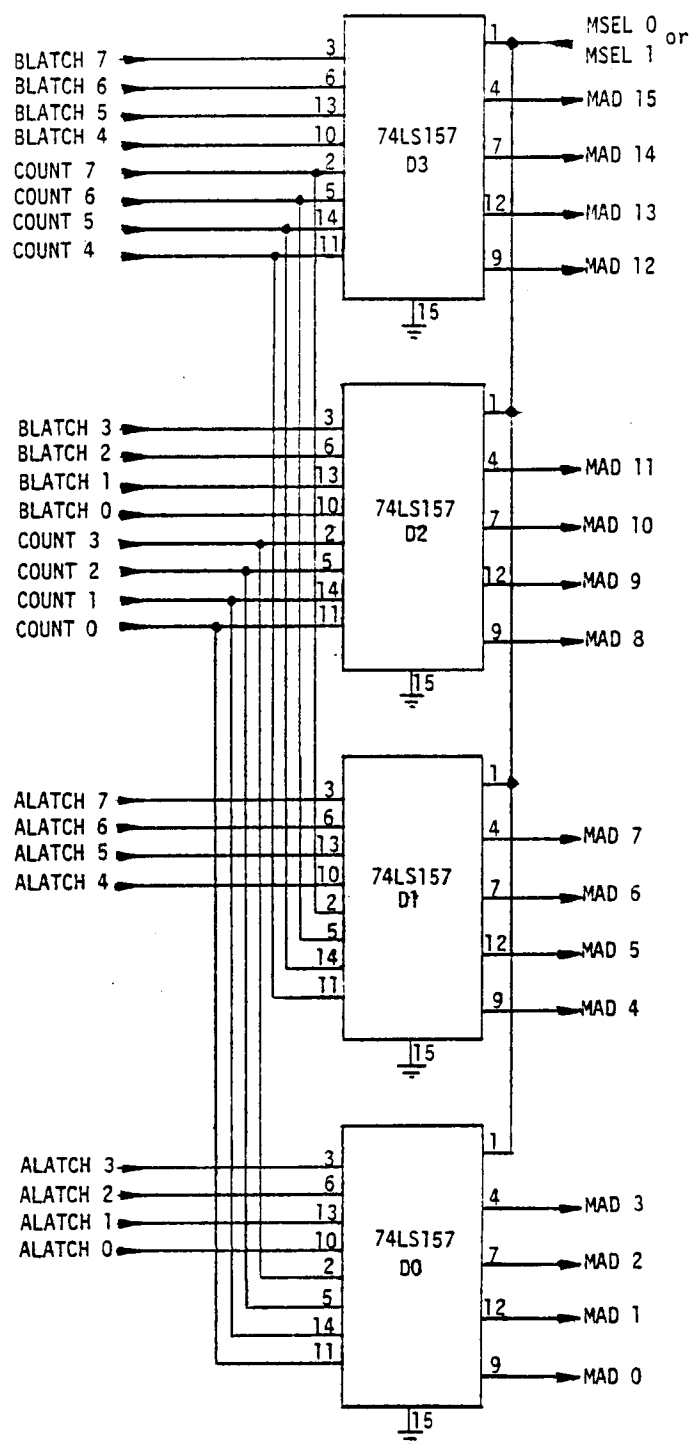


Figure 4.2. The memory address multiplexers.

for the upper and lower eight bits, COUNT 0 through COUNT 7, is generated by the control circuit. Since the digital data to be stored in the DTMM has been sampled in 8-bit bytes, two data points can then be written in the 16-bit memory location addressed. The byte which is written is controlled by the DTMM HBYT H, DTMM LBYT H, and MEM WT L signals generated by the control circuit and shown in Figure 4.1. This method of storage allows two points to be transferred per move, thus increasing the speed of the system data transfer rate. When addressed by the digitized video signal for transformation, the upper and lower bytes are addressed by the latch outputs of the VSC circuit, BLATCH 0 through BLATCH 7 and ALATCH 0 through ALATCH 7, respectively.

The data input lines are received from the four 74LS157 multiplexers shown in Figure 4.3. These multiplexers transmit the digitized video information signal or data from the processor to the DTMM data inputs. Selection of which data input will be presented to the memory is controlled by the status of the start/stop register. When the start/stop register is set, the sampled digital data is presented to the data inputs to be stored in the proper memory location using write pulses and control signals from the control circuit. When the start/stop register is cleared, data from the processor is presented at the input of the memory to allow the processor to load new transformation curves in the DTMM. The control lines, MEM LBYT L and MEM HBYT L, shown in Figure 4.1, are generated by the interface circuit when the processor wants to write a certain byte to the DTMM and not a whole word.

The data out lines, MDO 0 through MDO 15, of the upper and lower 8-bit bytes are latched by two 74LS374 latches as shown in Figure 4.4.

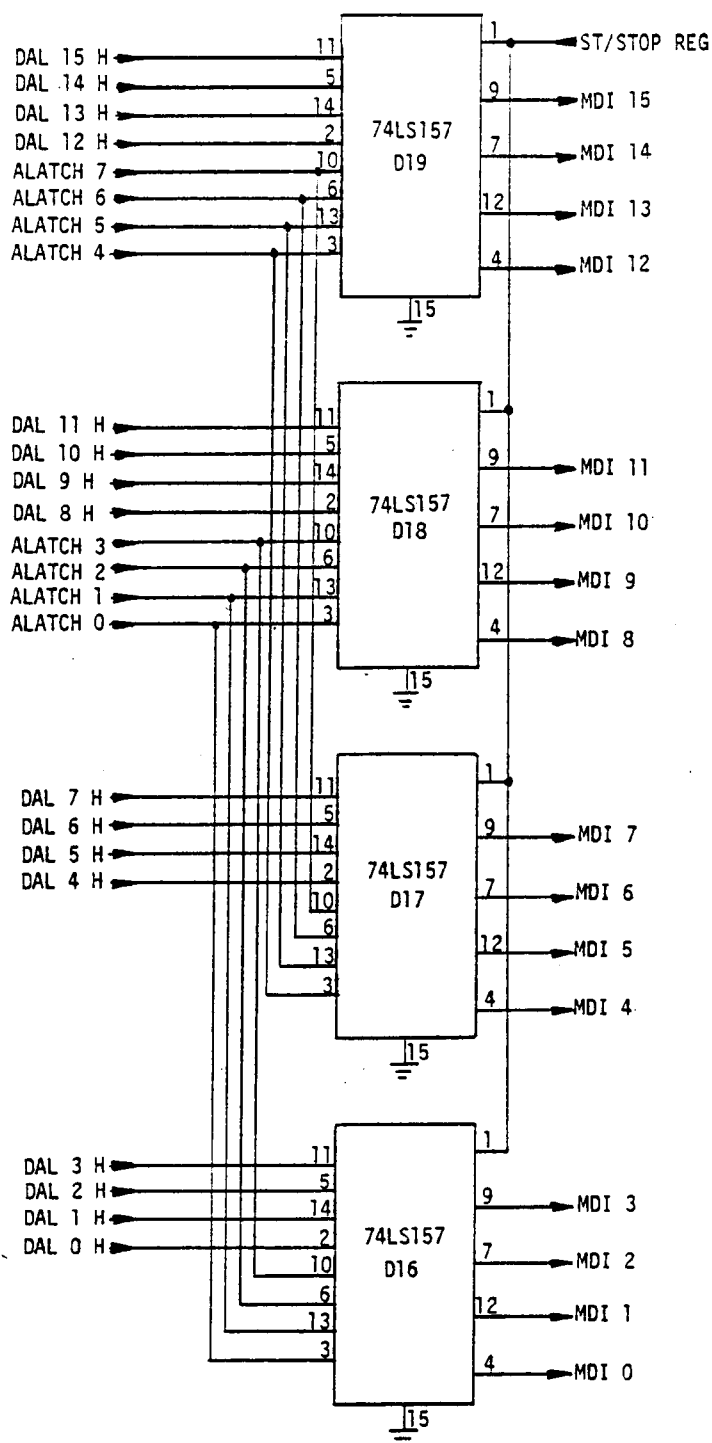


Figure 4.3. The memory data multiplexers.

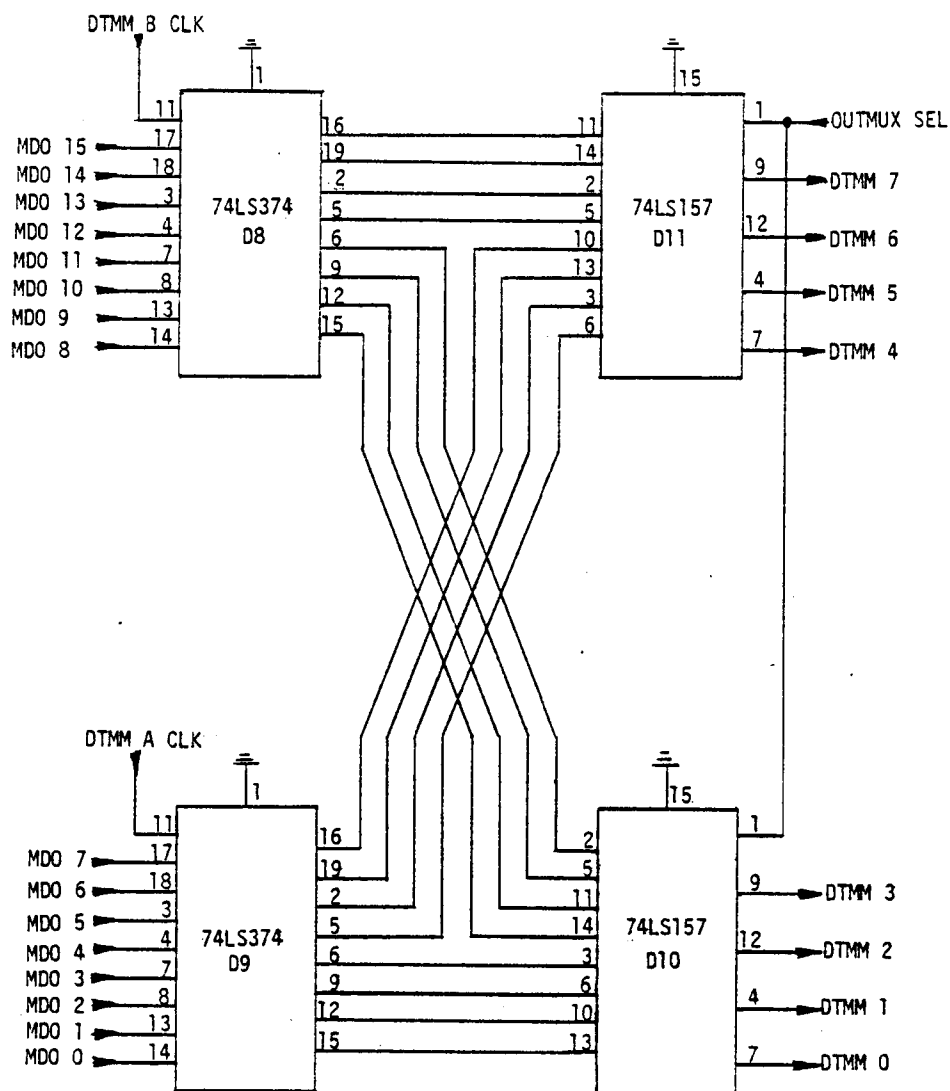


Figure 4.4. Memory output latches and multiplexers.

These latches are clocked by DTMM B CLK and DTMM A CLK, respectively. These latches are used to insure proper transfer of the data through the memory with no errors or "dropping of bits." The latch outputs are multiplexed through two 74LS157 multiplexers to reduce the 16-bit memory output from each side of the DTMM to eight bits, DTMM 0 through DTMM 7, which are then sent to the VPPC discussed in Chapter 5. The proper latch output transmitted through these multiplexers is synchronized with the latching of the output of the memory chips and is controlled by OUTMUX SEL generated in the control circuit in Chapter 7. Data out lines of the memory chips, MDO 0 through MDO 15, are also sent to four 74LS157 multiplexers shown in Figure 4.5. The outputs of these multiplexers are sent to transceivers in the interface circuit to be placed on the processor bus. This allows the processor to receive data from the DTMM as it would from any location in the processor memory. The select line to these multiplexers is operated by MSEL 0 from the control circuit. Buffer drivers were needed as shown in Figure 4.5 to overcome capacitance developed by sending signals through the backplane of the system.

4.2. DTMM Timing

The timing of the data through the DTMM is shown in Figures 4.6 and 4.7. Figure 4.6 shows the case of one video source at a sample rate of 464 points per horizontal line. Figure 4.7 shows the case of one video source at 928 points per horizontal line or two video sources at 464 points per horizontal line each. The slower sample rates will have the same time delays from each sample pulse but the delays will not be as critical as in the two cases shown due to a longer time duration between sample pulses.

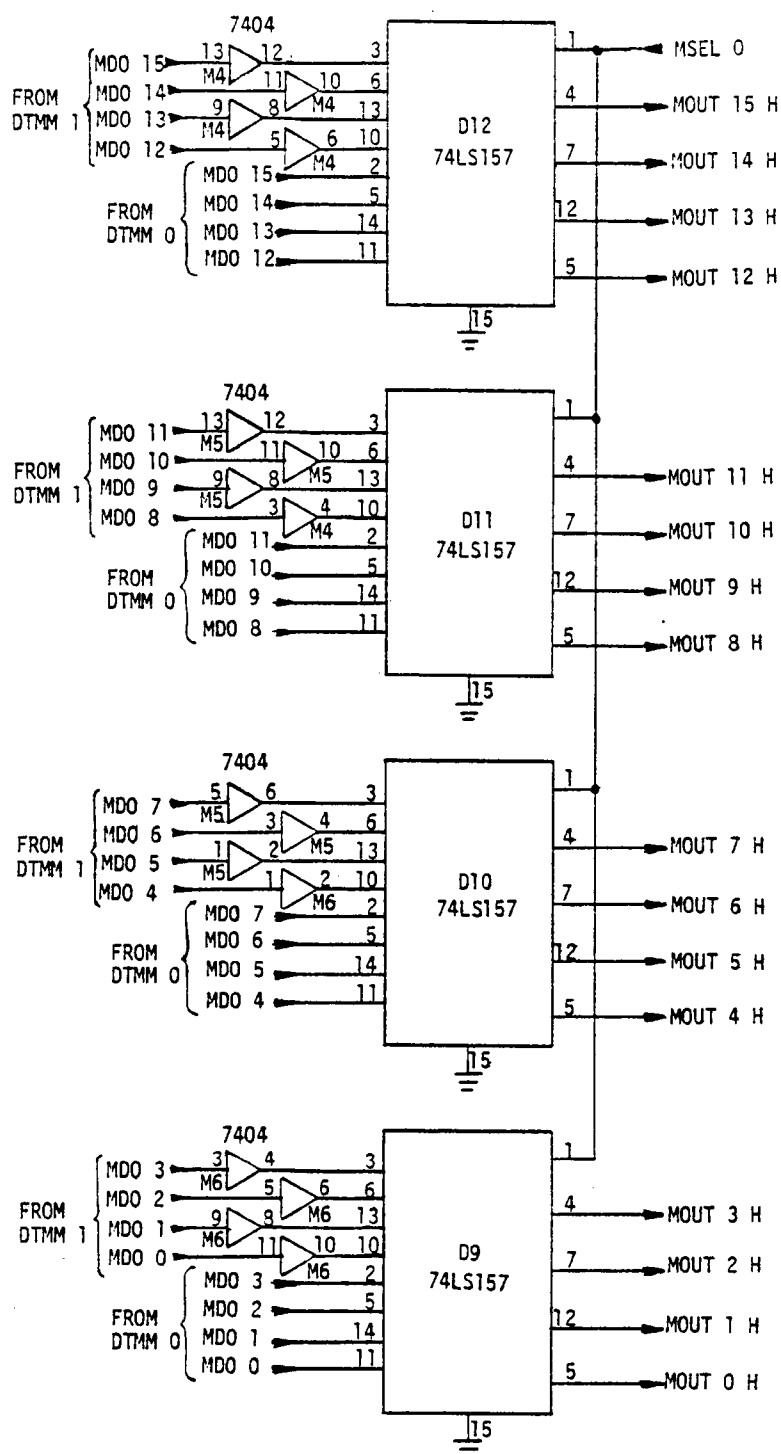


Figure 4.5. Memory multiplexers to the interface circuit.

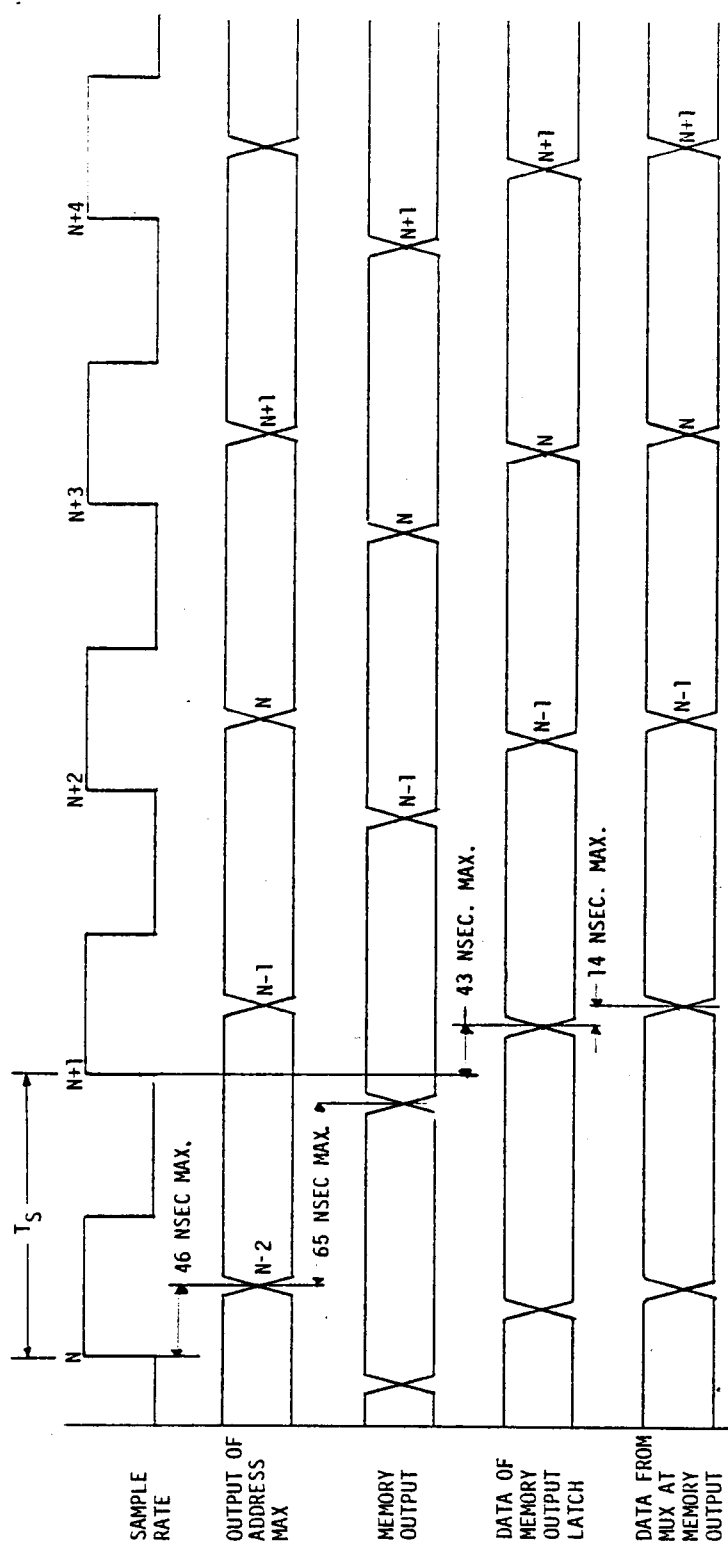


Figure 4.6. Timing diagram of the DTMM for one video source sampled at a rate of 464 points or less per horizontal line.

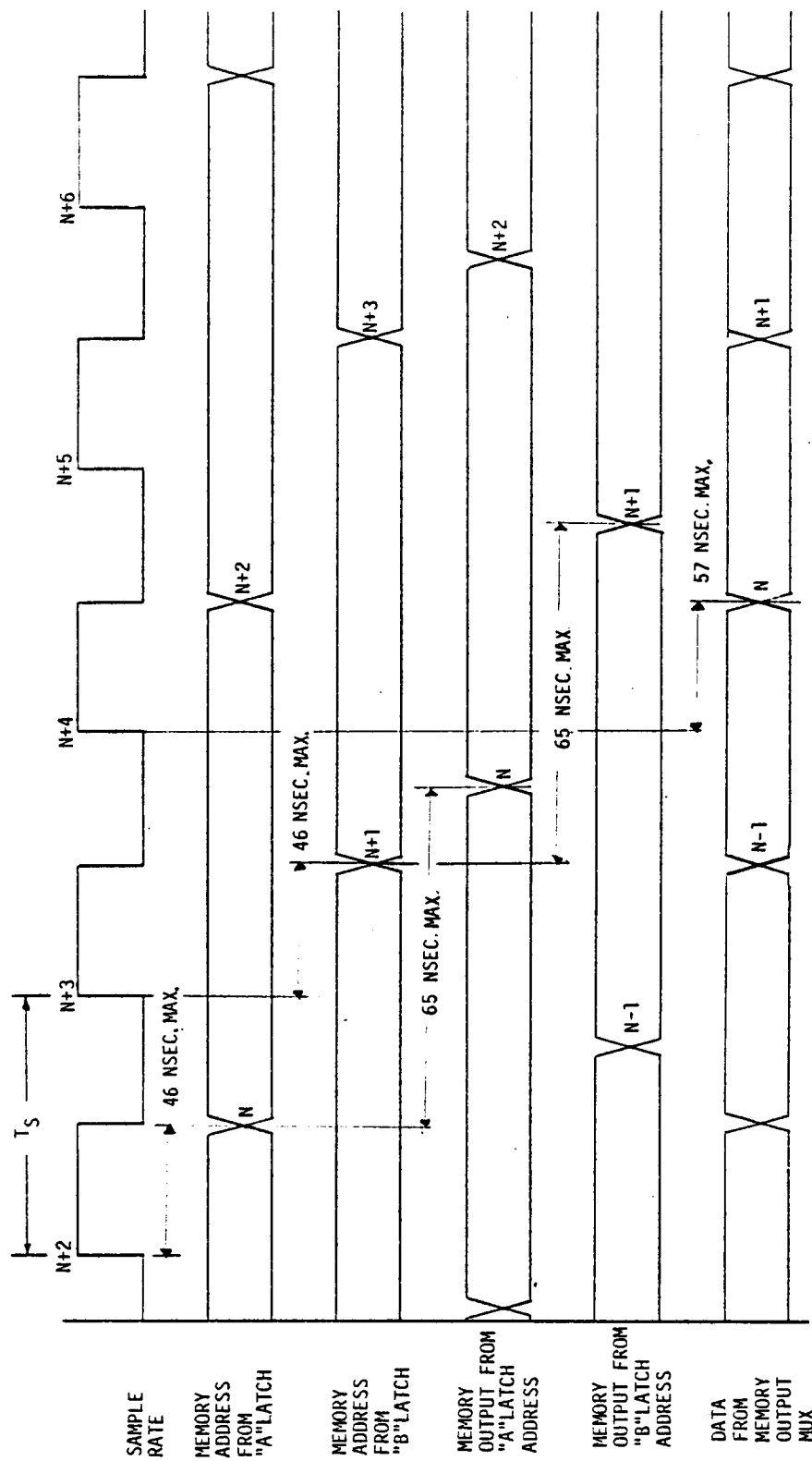


Figure 4.7. Timing diagram for the DTMM for one video source sampled at 928 points per horizontal line or two video sources sampled at any sample rate.

As shown in Figure 4.6, one sample period is needed to complete a cycle through the DTMM in this mode of operation. A timing delay of two sample periods is needed to complete a cycle through the DTMM in the mode depicted in Figure 4.7. The reason for the added sample period delay is that this mode of operation uses both upper and lower bytes of the DTMM to perform the transformation process. A two-source mode requires both bytes because each source can have its own separate transformation curve. The transformation curves are each loaded in one byte of the memory locations. One video source sampled at 928 points per horizontal line uses both bytes of the DTMM since the sample period at this rate (57 nanoseconds) is faster than the maximum access time of the memory (65 nanoseconds). The high and low bytes are multiplexed to allow the video information to still be sampled at this fast rate. At any lower rate, the transformation of a signal from a single video source needs to use only the low byte of the DTMM, therefore using one less sample period of delay due to multiplexing not being performed on the output bytes of the DTMM.

4.3. Loading the Transformation Curves

The curves used by the VDRC system to perform the transformation of the digitized video information signal are loaded from the processor into the proper high or low bytes of the DTMM. When one video source is used at the 928 points per horizontal line sample rate, the transformation curve must be loaded in both high and low bytes of the DTMM due to the multiplexing of the DTMM performed at this fast rate, as mentioned earlier. One video source used at any other sampling rate requires that the transformation curve be loaded in only the low byte of the DTMM.

When two video sources are used at any sampling rate (maximum of 464 samples per source) the transformation curve of one source is loaded in the low byte and the other source transformation curve is loaded into the high byte of the DTMM. The video source selected to have sample points stored by the other side of the DTMM must have its transformation curve loaded into the low byte, otherwise the sampled points of the video information signals will be sent through the transformation curve intended for the opposite source. This "swapping" of transformation curves would result in the data not being transformed properly and errors would be introduced into the output display.

CHAPTER 5

DATA RECONSTRUCTION

Once the sampled data has been transformed by one of the Digital Transformation Mapping Memories (DTMM), the processed data points must be reconstructed into a composite video signal which is compatible with a standard video display monitor. This process involves changing the transformed digital data into its analog equivalent voltage from a pre-determined scale. A reconstructed analog waveform is then combined with a composite sync signal to produce the composite video information signal used to drive the display monitor. The composite sync signal must be delayed an interval of time equal to the throughput delay of the VDRC system before being combined with the reconstructed analog waveform. This delay is dependent upon the sample rate selected and is needed to insure the proper composite video waveform will be generated for driving the display monitor. The Video Post-processing Circuit (VPPC) and Video Reconstruction Circuit (VRC) combine to perform these functions. An External Sync Generation Circuit (ESGC) is also provided to produce a composite sync signal, horizontal drive, and vertical drive which may be used when two video sources are sampled in stereo to keep the video sources in synchronization with each other.

5.1. The Video Post-processing Circuit

The Video Post-processing Circuit (VPPC) accepts the composite sync signal from the Video Sampling Circuit (VSC) and delays the composite sync signal to the VRC to correspond to the throughput delay present in the digitized video signal. This delay of the composite sync signal must

vary with the different throughput delays discussed in Chapter 2 to insure that a proper composite video waveform will be produced at the output of the VDRC system. A second delayed composite sync signal is also produced and sent to the control circuit to reset the sample rate generator and allow the sample points to occur at the same location on each horizontal line. These variable delay composite sync signals are produced by the circuit shown in Figure 5.1. A circuit consisting mainly of 74LS164 serial-in parallel-out shift registers is used. The first six of these shift registers are clocked at the master clock rate and the next seven are clocked at a rate equal to one-half the master clock rate which is produced by the 74LS74 connected as a toggle flip-flop shown in Figure 5.1. The CSYNC signal from the VSC is fed to the first shift register serial input. All remaining shift register inputs are the last parallel output of the preceeding shift register. These shift registers are tapped at the outputs corresponding to the throughput delay introduced in the VSC, DTMM, and VPPC for each sample rate. The appropriate outputs are fed to the inputs of a 74LS151 eight-to-one multiplexer shown in Figure 5.2. This multiplexer output selection is controlled by the bits from the control register which select the sample rate. As connected in Figure 5.2, when the various sample rates are selected, the appropriately delayed composite sync signal is allowed to be transmitted through the multiplexer and be output as DSYNC. Thus the appropriate amount of delay in the composite sync signal is produced according to the sample rate selected.

The same basic procedure is used to select the composite sync delay, CNTL SYNC, to be sent to the control circuit. Another 74LS151

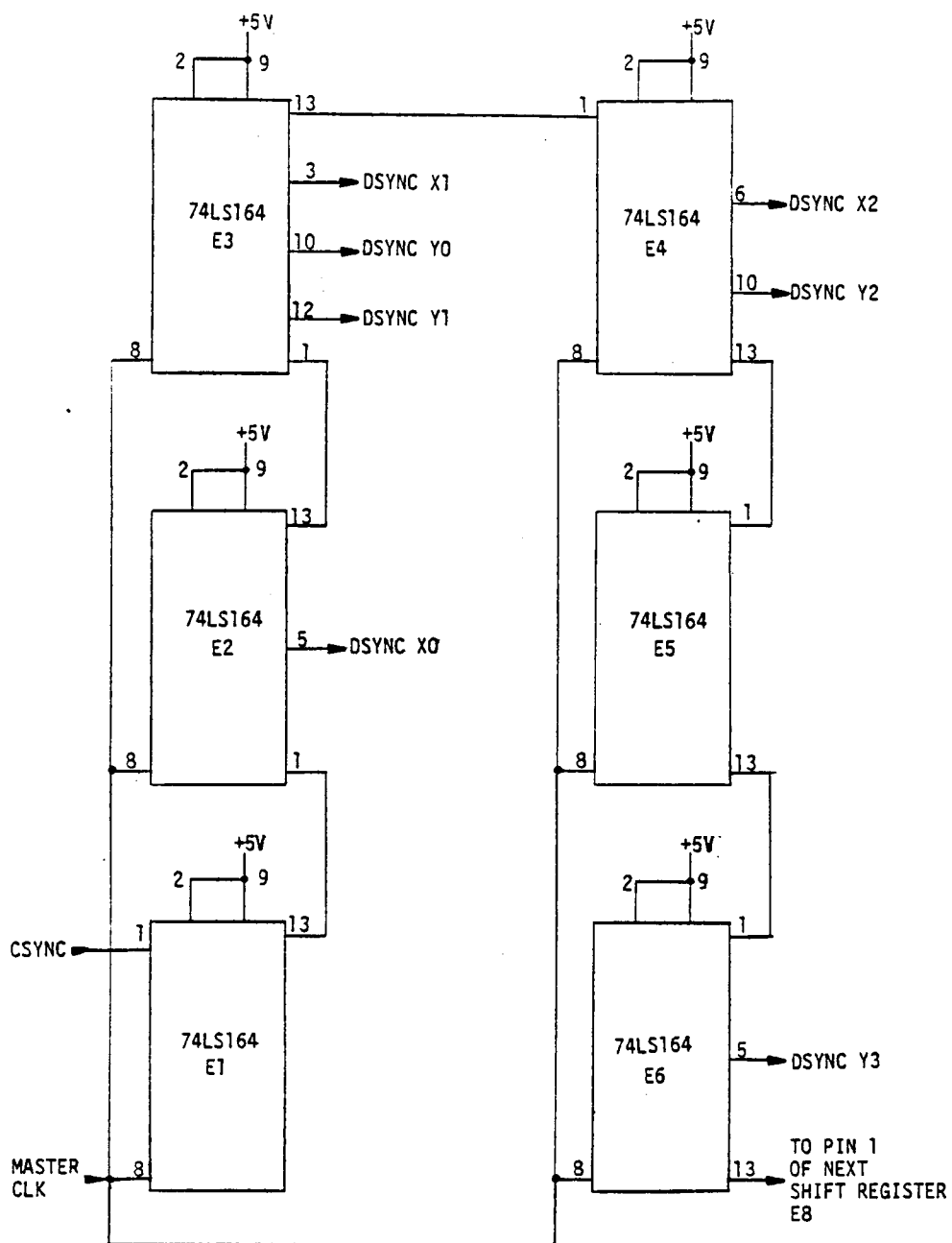


Figure 5.1. The composite sync delay circuit.

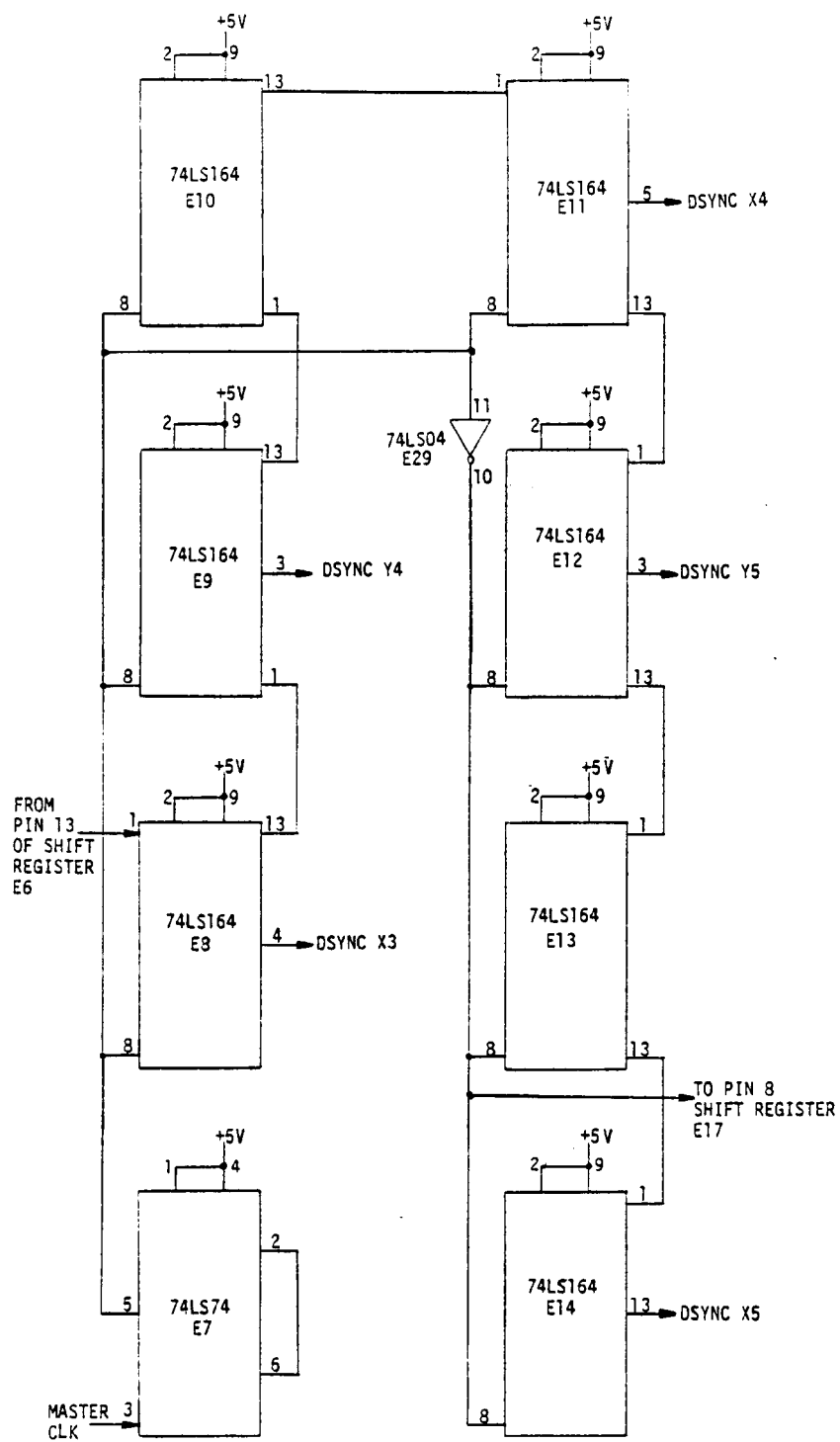


Figure 5.1. (Continued).

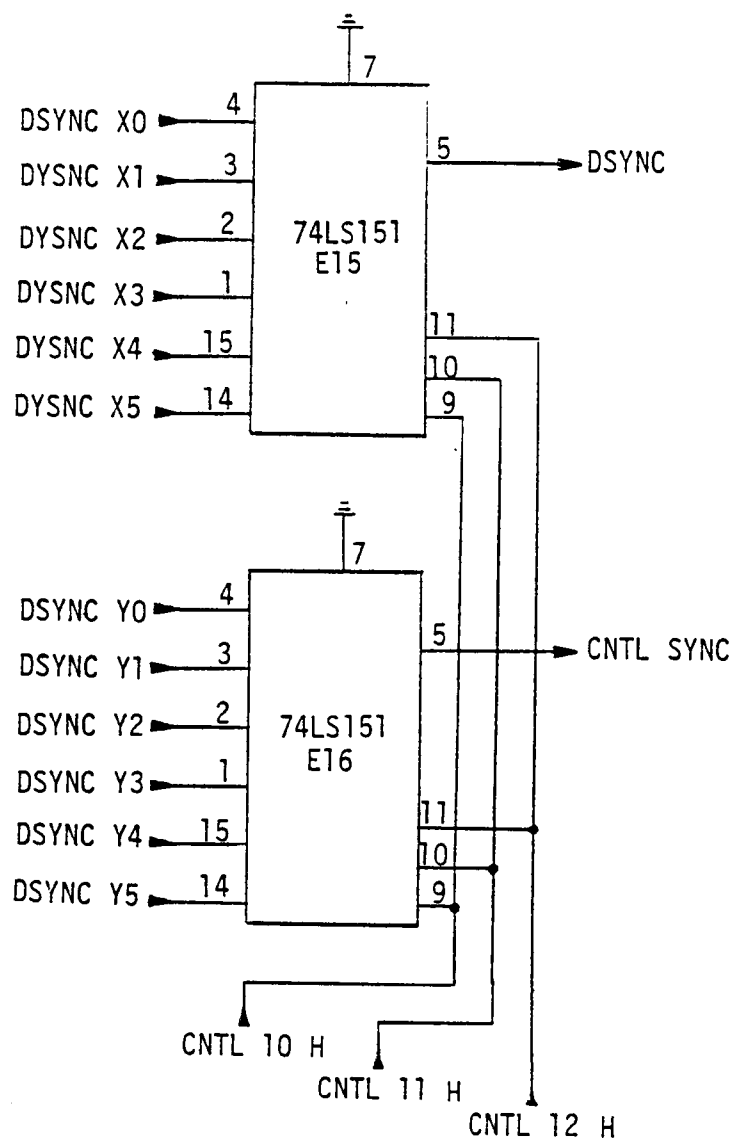


Figure 5.2. The composite sync delay multiplexers.

eight-to-one multiplexer is used as shown in Figure 5.2 and is controlled by the same bits of the control register which selected the other multiplexer output, as mentioned previously. The reason for the amount of delay in the composite sync signal sent to the control circuit which is introduced by this arrangement will be discussed in Chapter 7.

The delayed composite sync signal, DSYNC, is then sent to the circuit shown in Figure 5.3. This circuit adjusts the composite sync signal if two video sources are digitized simultaneously. Its basic function is to introduce an extra sample period in the composite sync signal of the video source which is sampled second on each horizontal line. This video source corresponds to the video source which may not have points stored in the DTMM, as discussed in Chapter 4. The added sample period is inserted only when two sources are sampled simultaneously. Selection of which composite sync signal is delayed the extra sample period is controlled by the 74LS155 two-to-four demultiplexer shown in Figure 5.4. An added sample period is produced by another set of 74LS164 shift registers tapped at the appropriate locations and connected to the 74LS151 eight-to-one multiplexer, as shown in Figure 5.3. Proper multiplexer selection is controlled by the bits of the control register which select the sample rate. This multiplexer output and DSYNC are combined by the NAND gate arrangement to produce the two composite sync signals. These two delayed composite sync outputs, DSYNC A and DSYNC B, are sent to the VRC and to the composite blanking generation circuit shown in Figure 5.5.

The composite blanking generation circuit is composed of three 74123 multivibrators or "one shots" for each channel. Delayed composite sync signals, DSYNC A and DSYNC B, are connected as shown in Figure 5.5.

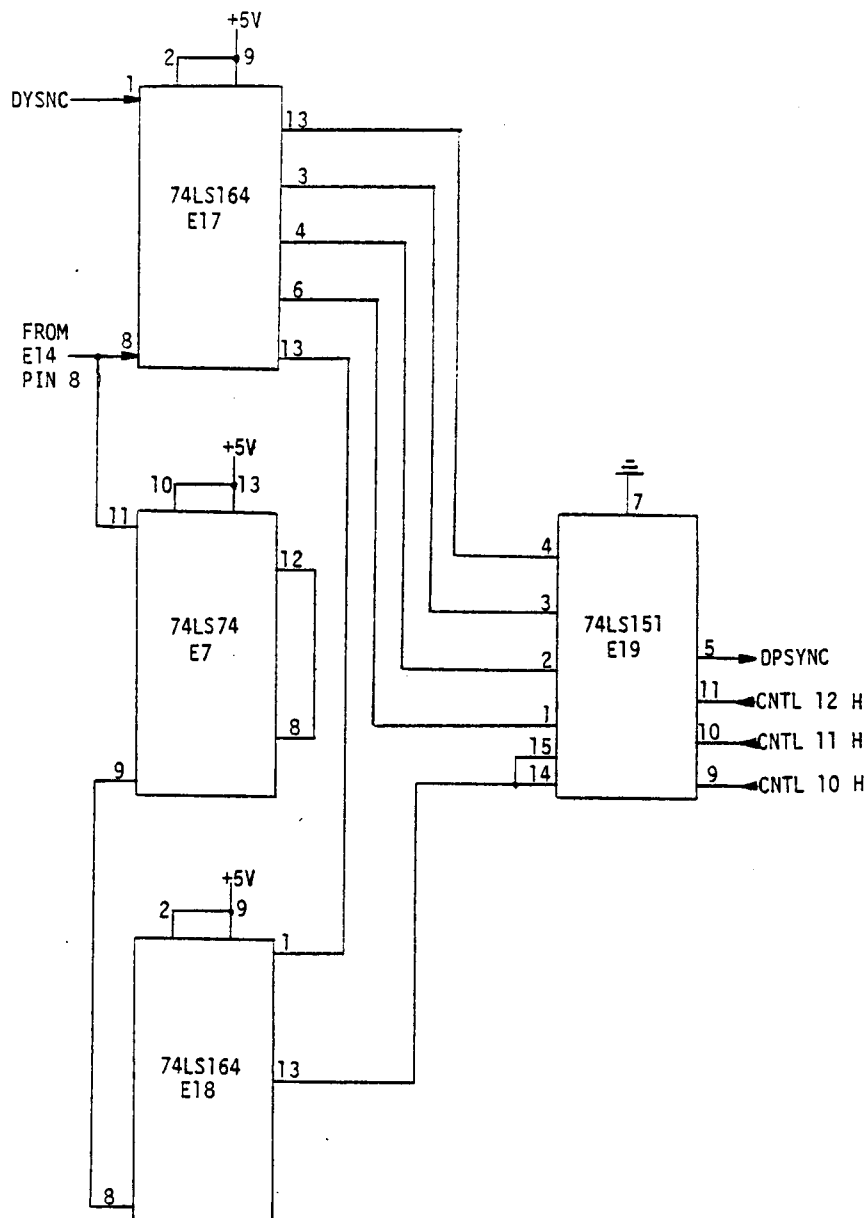


Figure 5.3. The composite sync delay adjustment circuit.

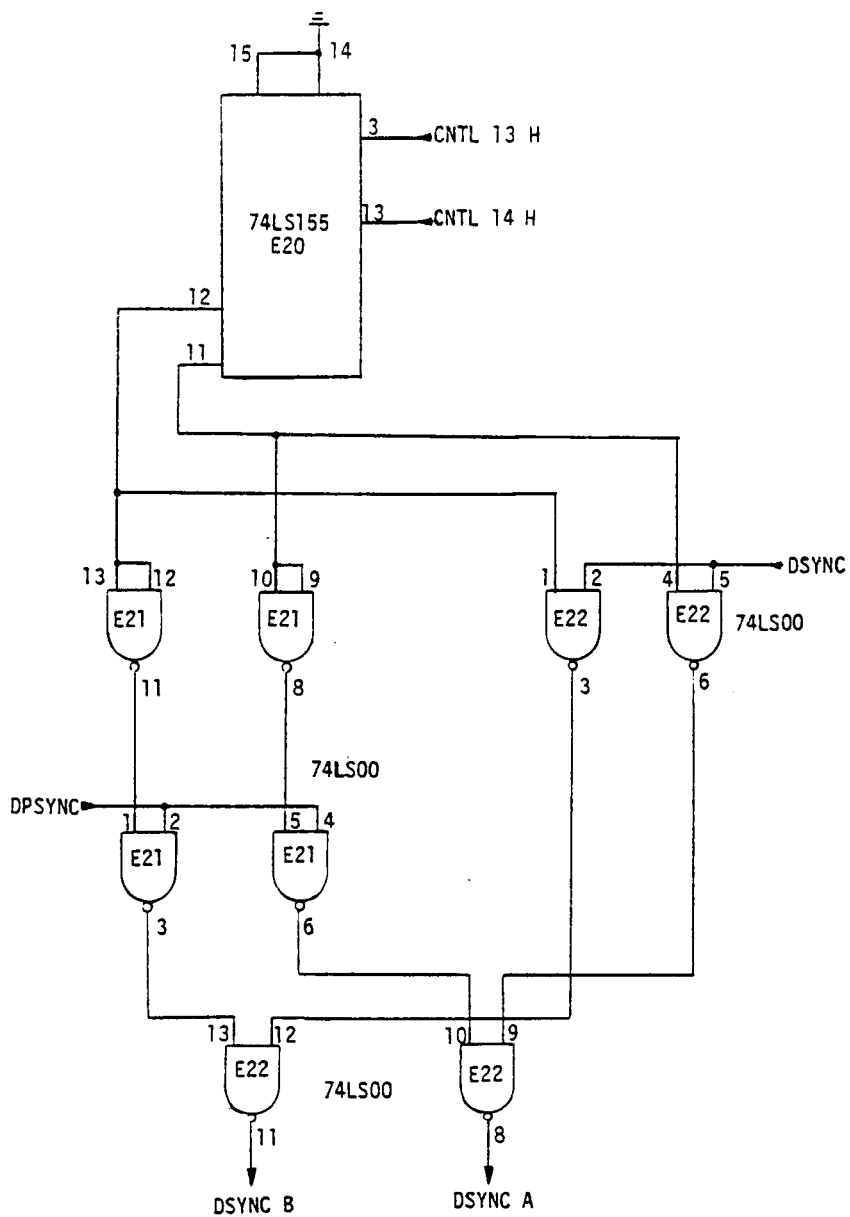


Figure 5.4. DSYNC A and DSYNC B generation circuit.

These multivibrators are triggered by the composite sync signal edges and produce the outputs shown in Figure 5.6. These outputs are then ANDed together as shown in Figure 5.5. A vertical retrace signal, VERT RET, which stays low for the entire vertical retrace, is generated in the control circuit then ANDed with the outputs of the "one shots" to produce a composite blanking signal as shown in Figure 5.6 to correspond with each delayed composite sync signal. These composite blanking signals, DBLANK A and DBLANK B, are then sent to the VRC to be used in the reconstruction process. The front and back porch of the blanking signals may be lengthened or shortened by the use of P3 and P4, respectively, shown in Figure 5.5 for each channel's composite blanking.

The VPPC also takes the digital outputs of the two DTMM's and selects the proper output to be latched by the output latch as shown in Figure 5.7. Selection is controlled by the MSEL 1 line and allows the output of the DTMM addressed by the sampled data to be sent to the output latch through the 74S157 multiplexers. The output latch is a 74LS374 8-bit latch and is clocked at the sample rate of the VDRC system. Transformed digital data to both D/A converters is transmitted through this latch.

The output latch data is then sent to the 74LS157 multiplexers which select the data to be transformed by the VRC circuit. These multiplexers are shown in Figure 5.8. Select lines of these multiplexers are normally pulled high to allow the data from the output latch to be sent to the VRC, but the select lines may be pulled low externally to allow an external eight bits to be sent to each VRC for reconstruction. The select lines of the multiplexers shown in Figure 5.9 are controlled by the same signal lines that control the select lines of the corresponding

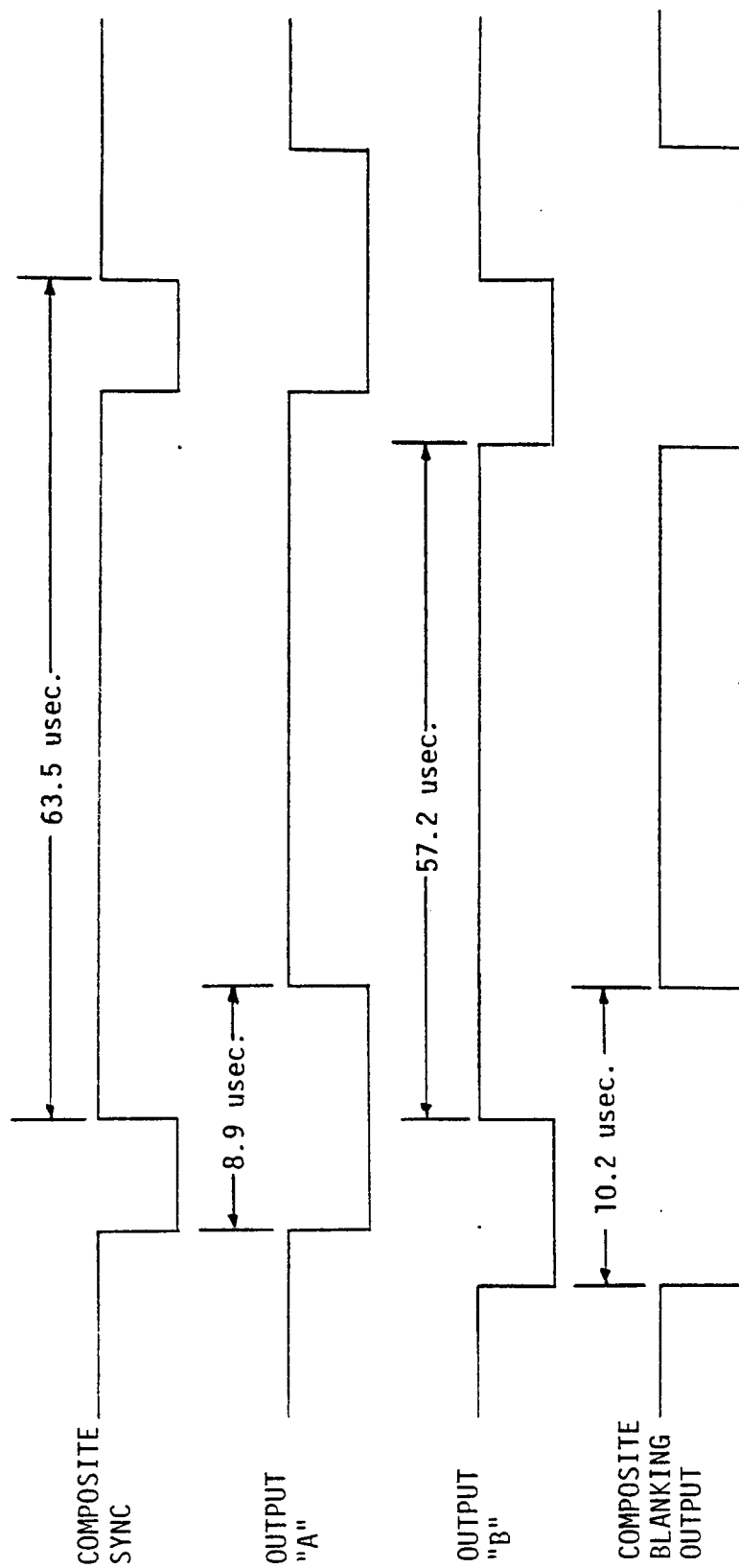


Figure 5.6. Waveforms associated with the composite blanking generation circuit.

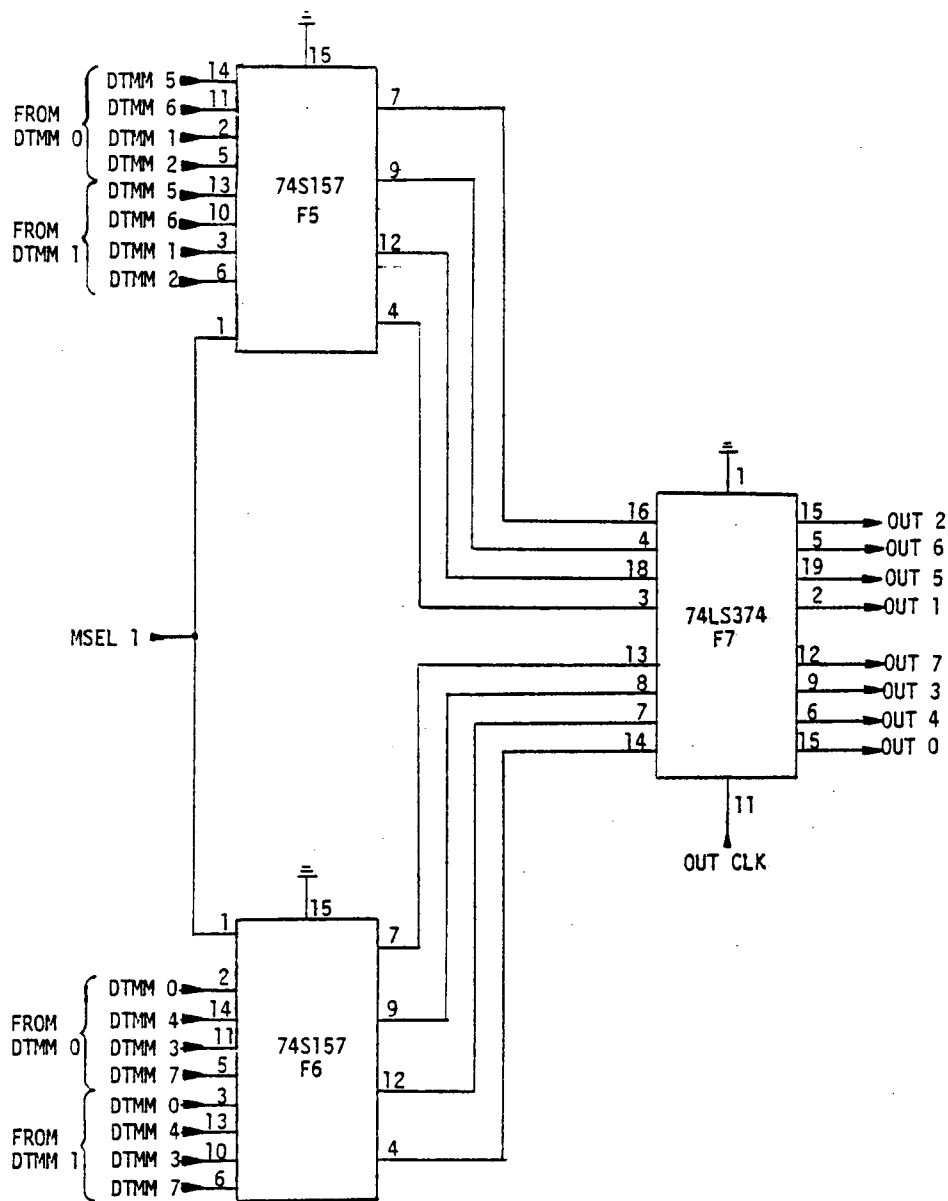


Figure 5.7. VPPC output multiplexers and latch.

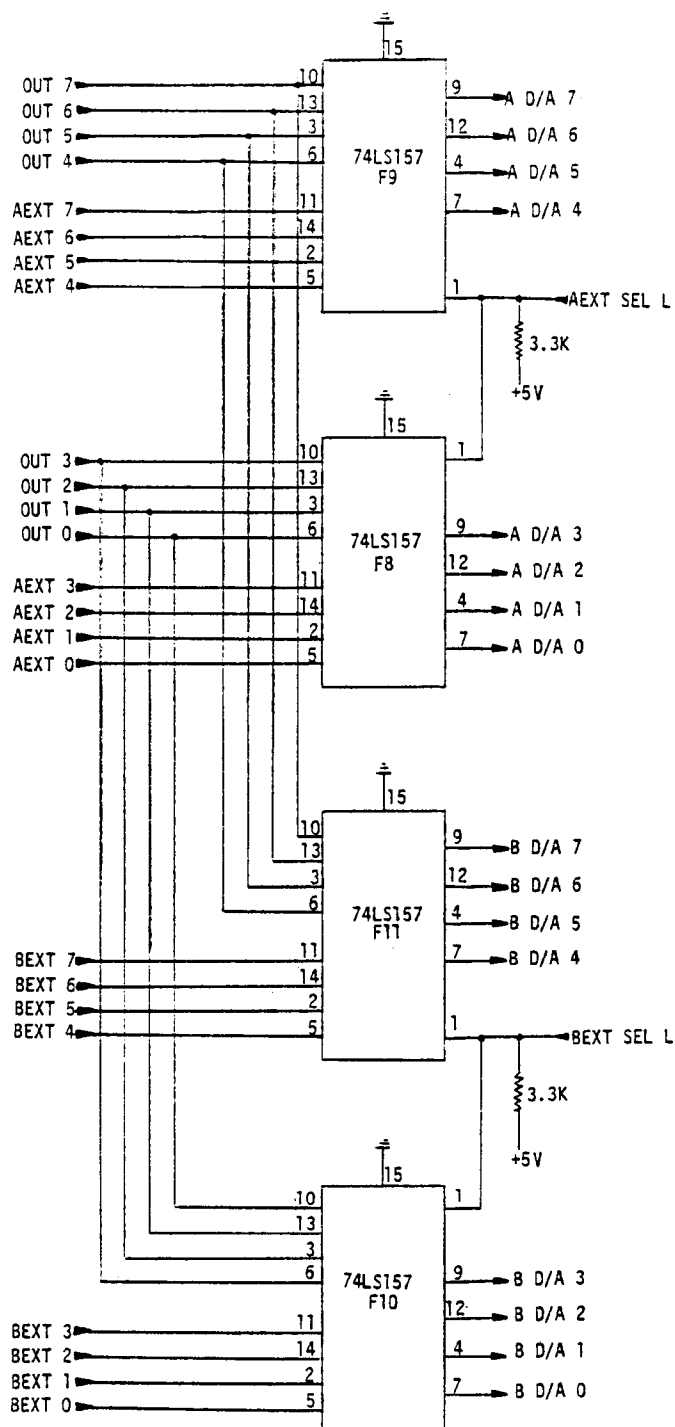


Figure 5.8. D/A converter data multiplexers.

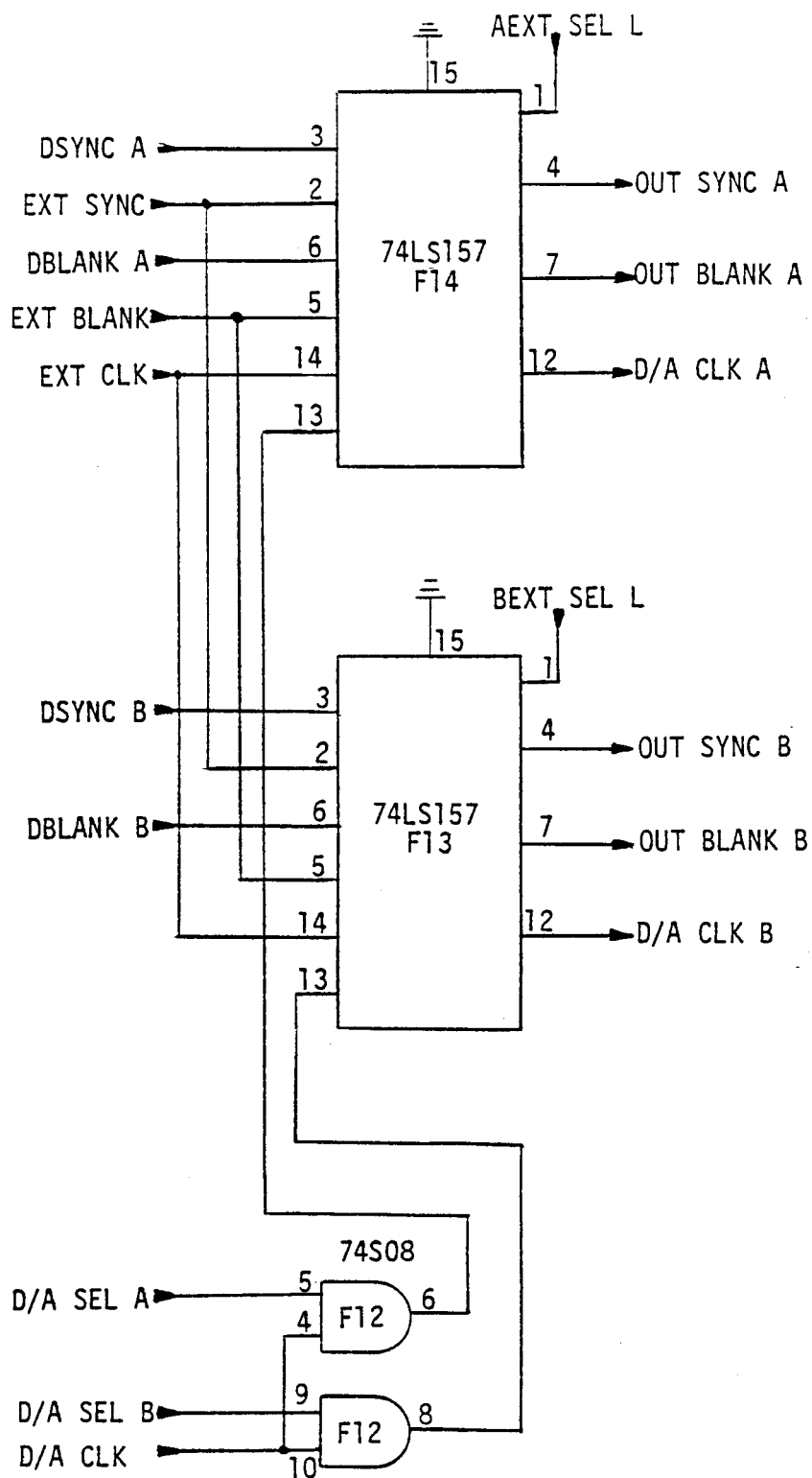


Figure 5.9. D/A converter control line multiplexers.

video sampled data multiplexers. When normally high, the delayed composite sync, composite blanking, and D/A clock signals from the VDRC system are allowed to pass to the VRC circuit but when the select line is pulled low, composite sync and blanking signals, from the External Sync Generation Circuit discussed later in this chapter, and an external clock are transmitted to the VRC circuit to control the reconstruction of the externally input data. Figure 5.10 shows the data transfer timing from the output of the DTMM to the output of the D/A multiplexer.

5.2. The Video Reconstruction Circuit

The Video Reconstruction Circuit (VRC) is composed of two Analogic MP8308 composite video digital-to-analog (D/A) converters. These D/A converters, shown in Figure 5.11, convert the transformed digital data into its analog equivalent waveform and add the composite sync and blanking signals generated by the VPPC circuit to produce a composite video signal with a source impedance of 75 ohms. This impedance matches the impedance of most coaxial cables used in closed circuit video systems and also the input impedance of most standard video display monitors. Thus the entire operation of reconstructing the transformed data into its equivalent composite video waveform is accomplished in one packaged circuit. Figure 5.11 shows the connections needed to allow each D/A converter to function properly. The D/A converters have a maximum conversion rate of 17.5 megahertz as used by the VDRC system. Their digital data inputs are TTL compatible so no buffer is needed between the D/A multiplexers and D/A converters. Since each packaged circuit combines the sync signal and the reconstructed analog waveform internally, no external

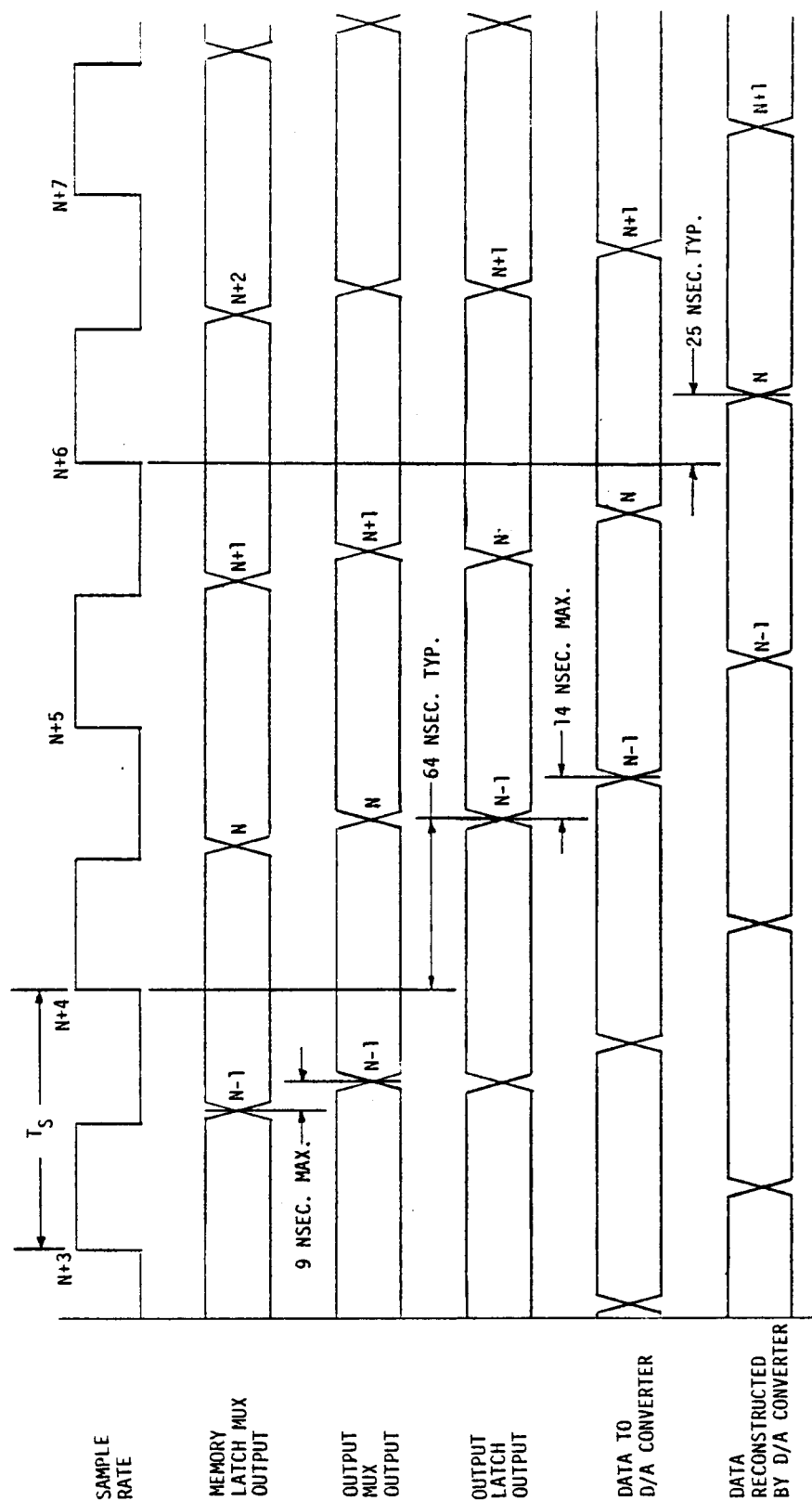


Figure 5.10. Timing diagram for the VPPC and VRC.

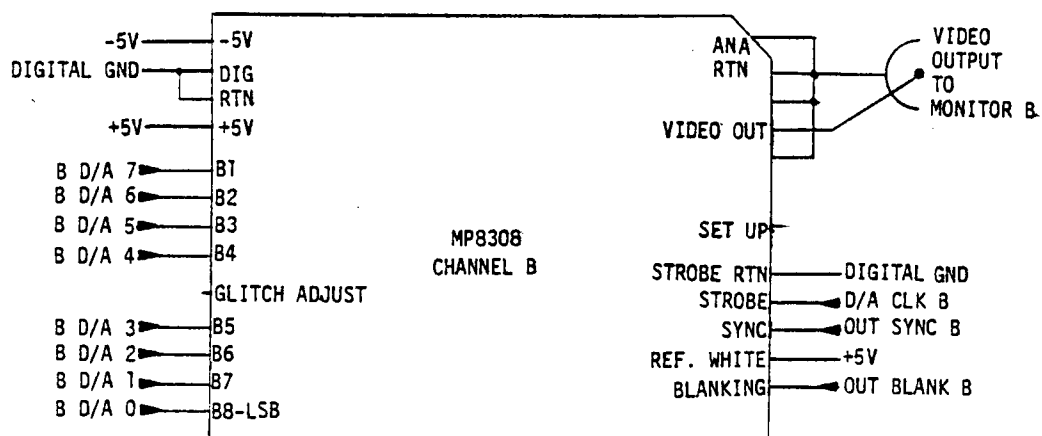
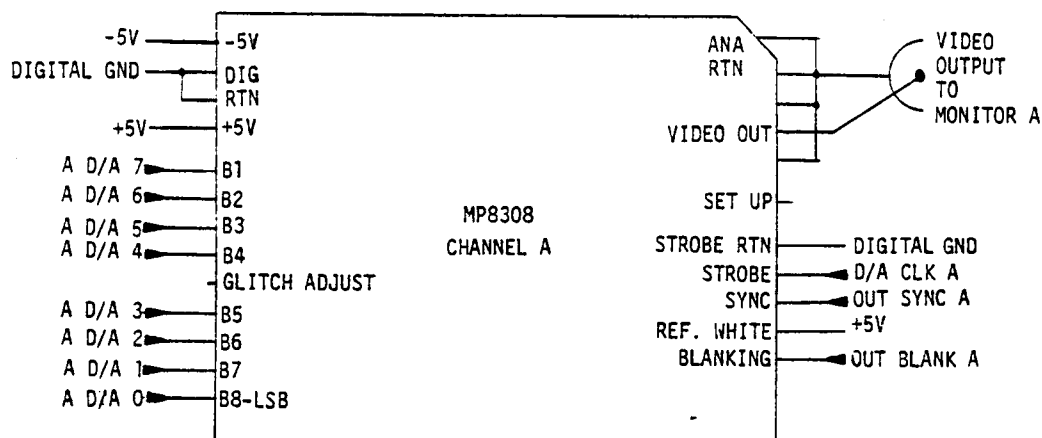


Figure 5.11. D/A converter connections.

amplifier or buffer is needed to produce a clear composite signal at the output which has a fast rise time and almost no overshoot or ringing. The output of each D/A converter is one volt peak to peak into a 75 ohm load which is sufficient to drive most standard display monitors.

5.3. External Sync Generation Circuit

The External Sync Generation Circuit (ESGC) is used to provide a composite sync signal, horizontal drive signal, and vertical drive signal to be used by the video source if it does not generate NTSC composite sync internally, or to keep two video sources in synchronization if stereo sampling and transformation is performed. It also provides the VRC with a composite sync signal and composite blanking signal which are needed when data from the external bus is to be reconstructed. These signals are provided when the multiplexer select lines are pulled low in the VPPC, as mentioned earlier.

The ESGC consists of a 14.31 MHz oscillator whose output is sent to a divide-by-seven counter. A clock rate of 2.045 MHz is produced. The output of the divide-by-seven counter is used to trigger a monostable multivibrator which forms a square wave from the output pulses of the counter. This square wave is fed into the clock of a MM5320 master sync generator chip which is set for this clock frequency. A NTSC composite sync signal, composite blanking signal, horizontal drive signal, and vertical drive signal which are TTL compatible are generated by the MM5320. These signals are sent through a 7407 buffer driver to insure that they are able to drive an external video source. Figures 5.12 and 5.13 show the circuit configuration.

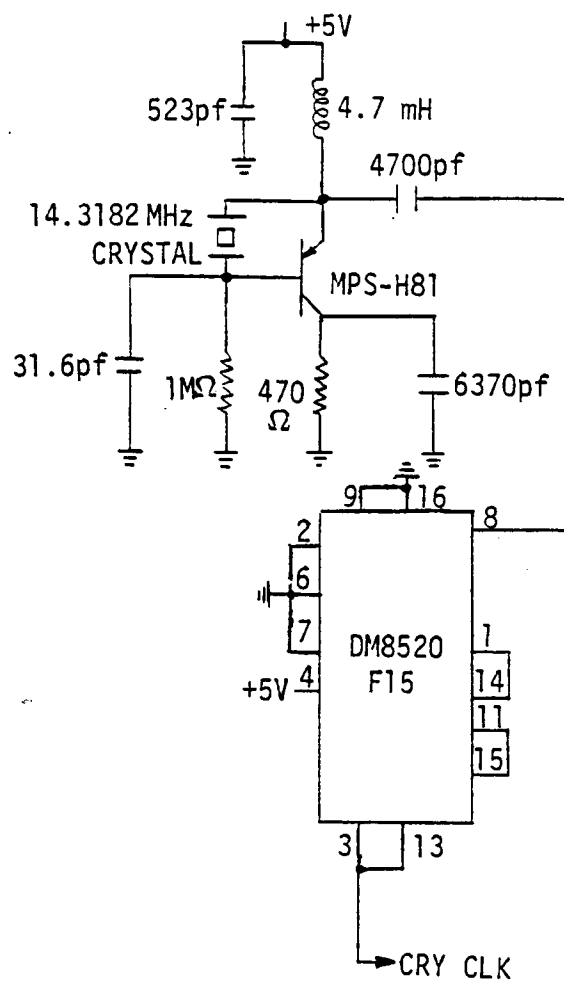


Figure 5.12. ESGC oscillator.

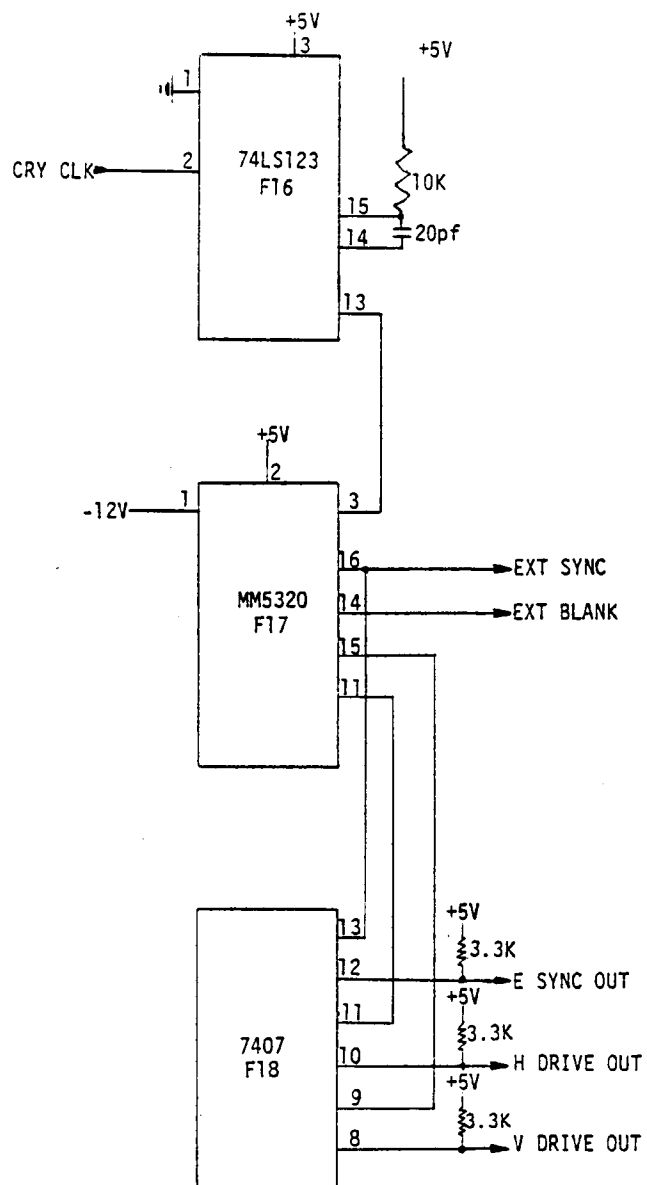


Figure 5.13. ESGC signal line outputs.

CHAPTER 6

PROCESSOR INTERFACE

The interface presented in this chapter is designed to be compatible with the D.E.C. LSI-11 bus structure and timing. The VDRC could be converted for operation by a different 16-bit processor by: 1) converting the bus signals from the processor to signals that are compatible with the LSI-11 bus structure, or 2) supplying a new interface which generates the signals and timing needed internally by the VDRC and thereby bypassing the LSI-11 interface. Timing and signals needed in the first alternative are given by the description of the interface used in the present system. Data needed for the second method is presented in Section 6.3 of this chapter.

6.1. Basic Timing of the Processor and Interface

The LSI-11 bus is structured in a bi-directional arrangement. Address and data signals are time-multiplexed on the bus with appropriate signals being transmitted and received by the processor to keep track of the state of the bus. Three basic modes of data transfer can occur via the bus between the processor and an external device: 1) DATI, or data in, which occurs when the processor reads a device or register, 2) DATO, or data out, when the processor writes data to a device or register, and 3) DATIO which is a combination of the first two, i.e., the processor reads a register or device and then writes to the same location new data. The DATIO cycle is used when the processor desires to change only the higher or lower eight bits of a location. These high and low eight bits are referred to as the high and low byte, respectively, of a memory

location. The basic timing diagrams for the DATI, DATO, and DATIO cycles are shown in Figures 6.1, 6.2, and 6.3, respectively. A detailed description of the LSI-11 timing and data manipulation can be found in the D.E.C. Microcomputer Handbook [5].

6.2. Interface Design and Operation

The interface of the VDRC system is connected to the open-collector LSI-11 bus by means of eight transceivers, one receiver, and two open-collector two-input NAND gates, shown in Figure 6.4, to reduce the loading effect on the bus. An LSI-11 processor has an inverted bus structure so all logic chosen to connect to the bus should be inverting in nature. Four DM8838 quad bus transceivers, shown in Figure 6.4, receive address and data signals from the processor and allow the control register data to be placed on the bus when the CNTL OT L line is pulled low. The DM8837 hex receiver allows the BSYNC L, BDATI L, BDATO L, BWTBT L, and BINIT L signals to be converted to SYNC H, DATI H, DATO H, WTBT L, and INIT H to be used by the system. Two open-collector two-input 7426 NAND gates allow the start/stop register and the RPLY H to be attached to the bus. Finally in Figure 6.5, four DM8838 receivers permit the DTMM data to be placed on the bus when addressed by the processor and MOUT L is pulled low.

The 16 bits received from the bus are sent to two DM8160 6-bit comparators and one DM8130 10-bit comparator, as shown in Figure 6.6. The address of the DTMM and registers of the system are set using the toggle switches shown in the figure. When the address of a memory location or register in the VDRC system is loaded on the bus, the comparators produce

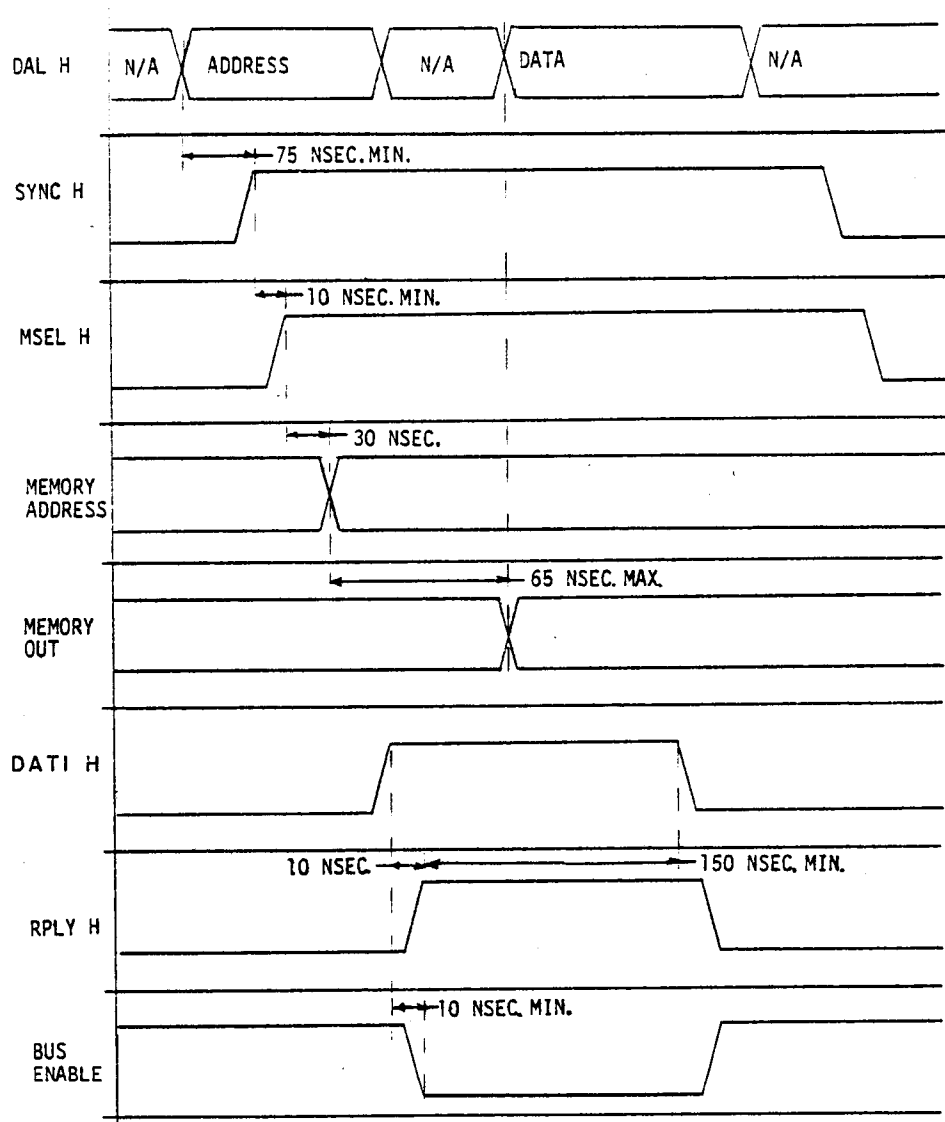


Figure 6.1. LSI-11 DATI cycle.

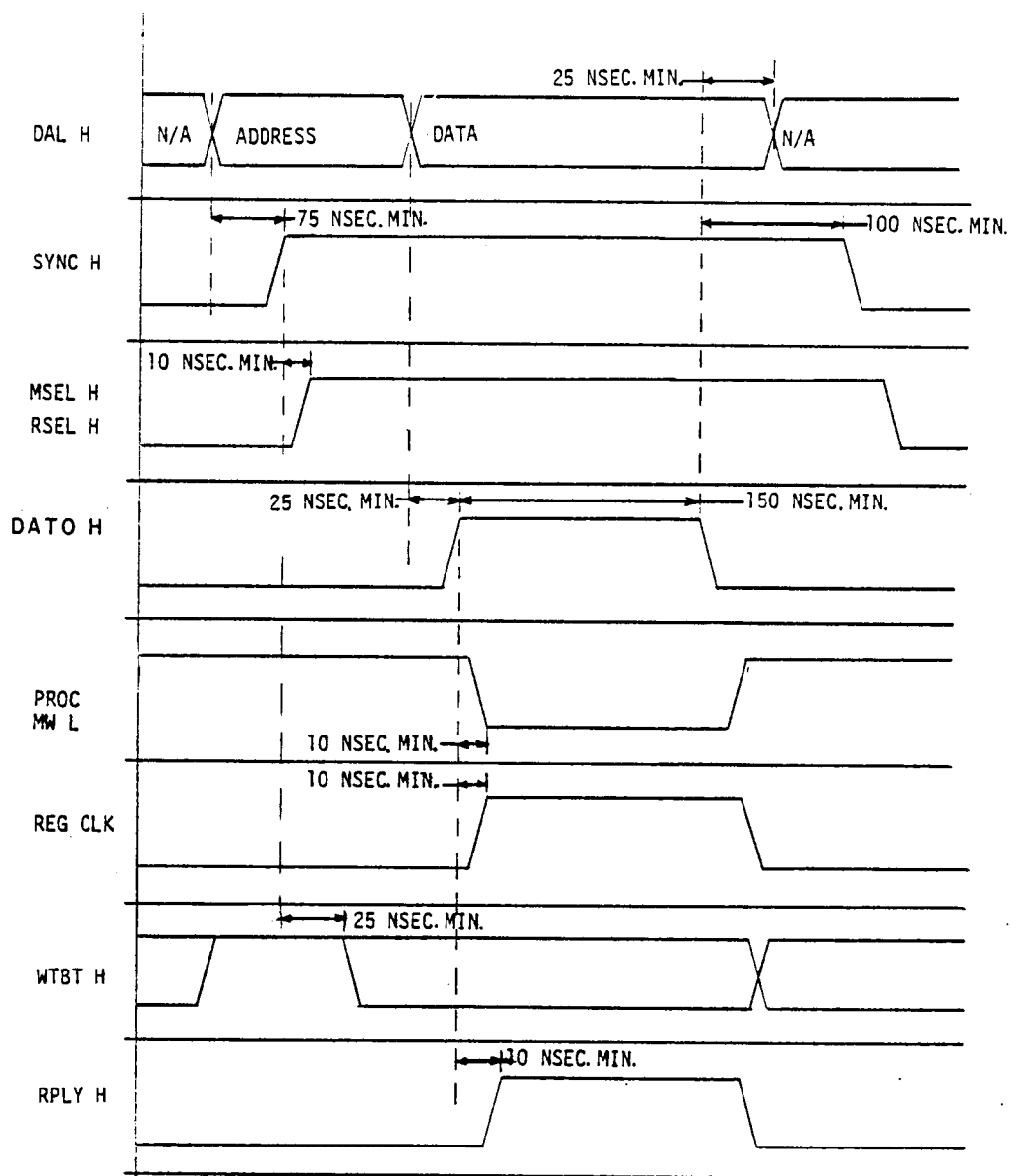


Figure 6.2. LSI-11 DAT0 cycle.

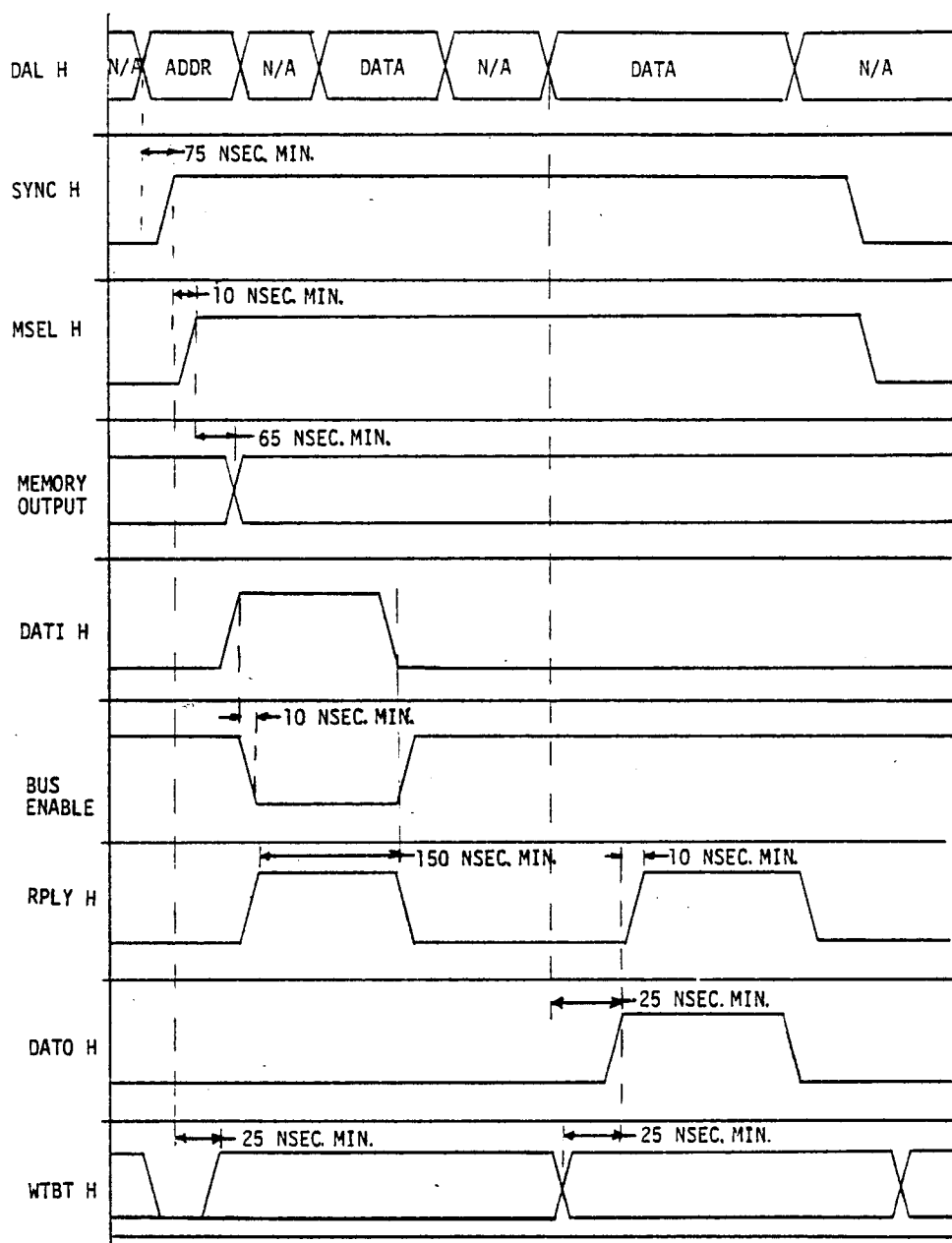


Figure 6.3. LSI-11 DATIO cycle.

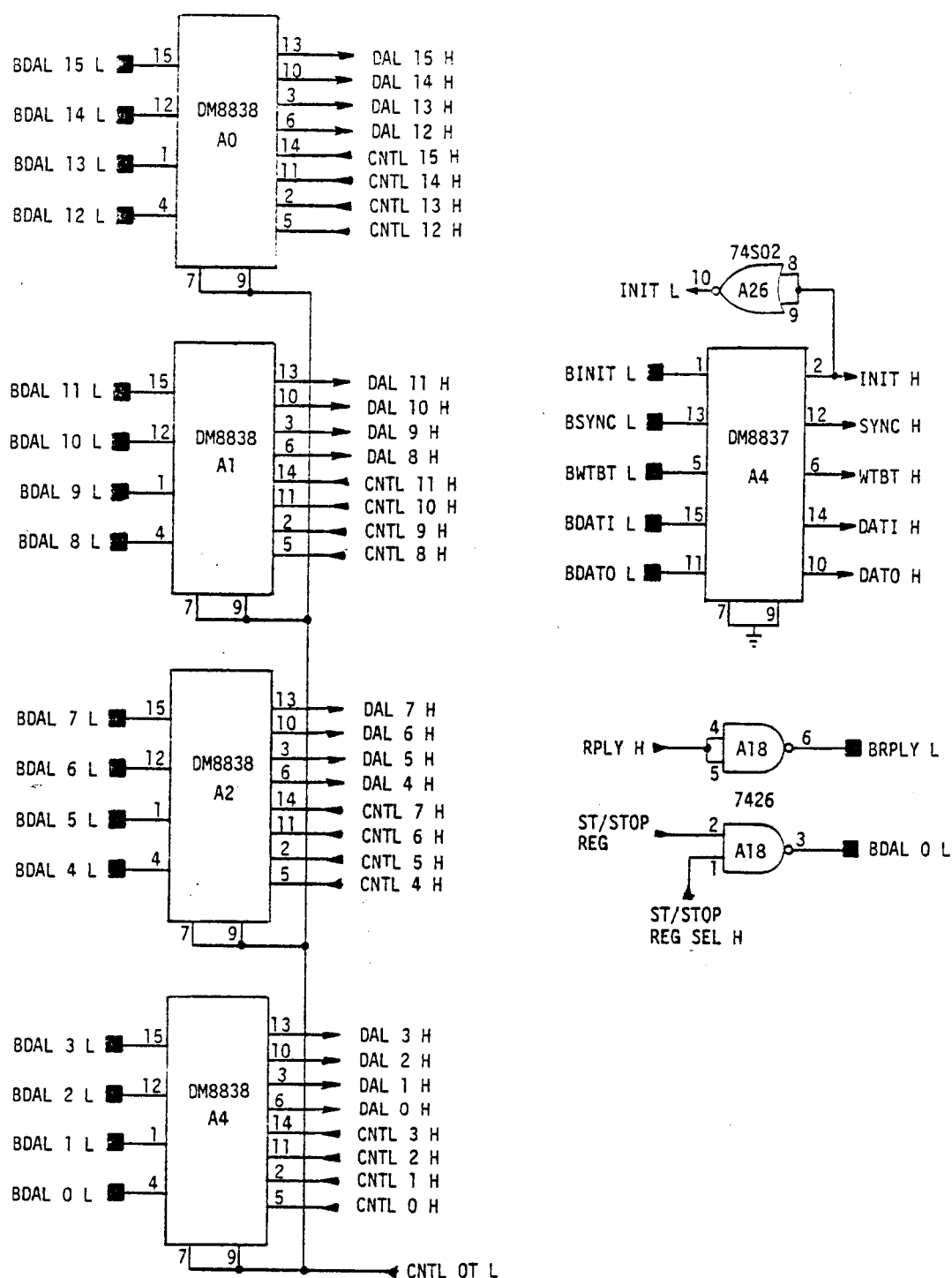


Figure 6.4. Data and control line receivers and control register drivers.

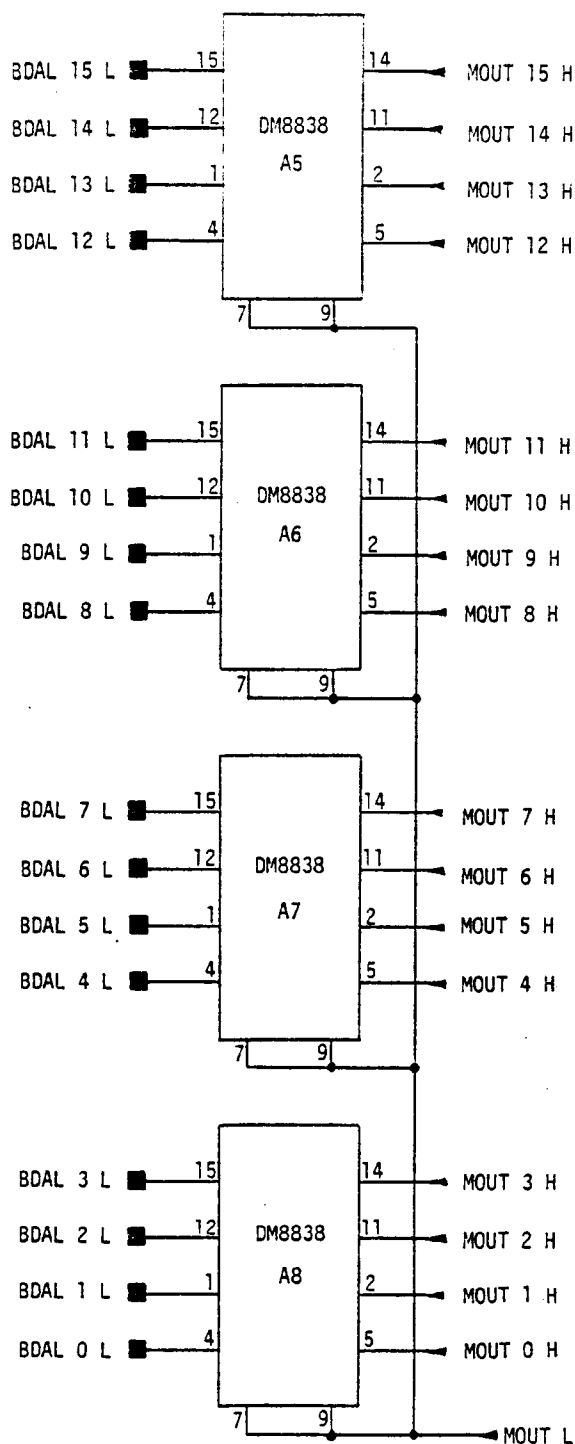


Figure 6.5. Memory output drivers.

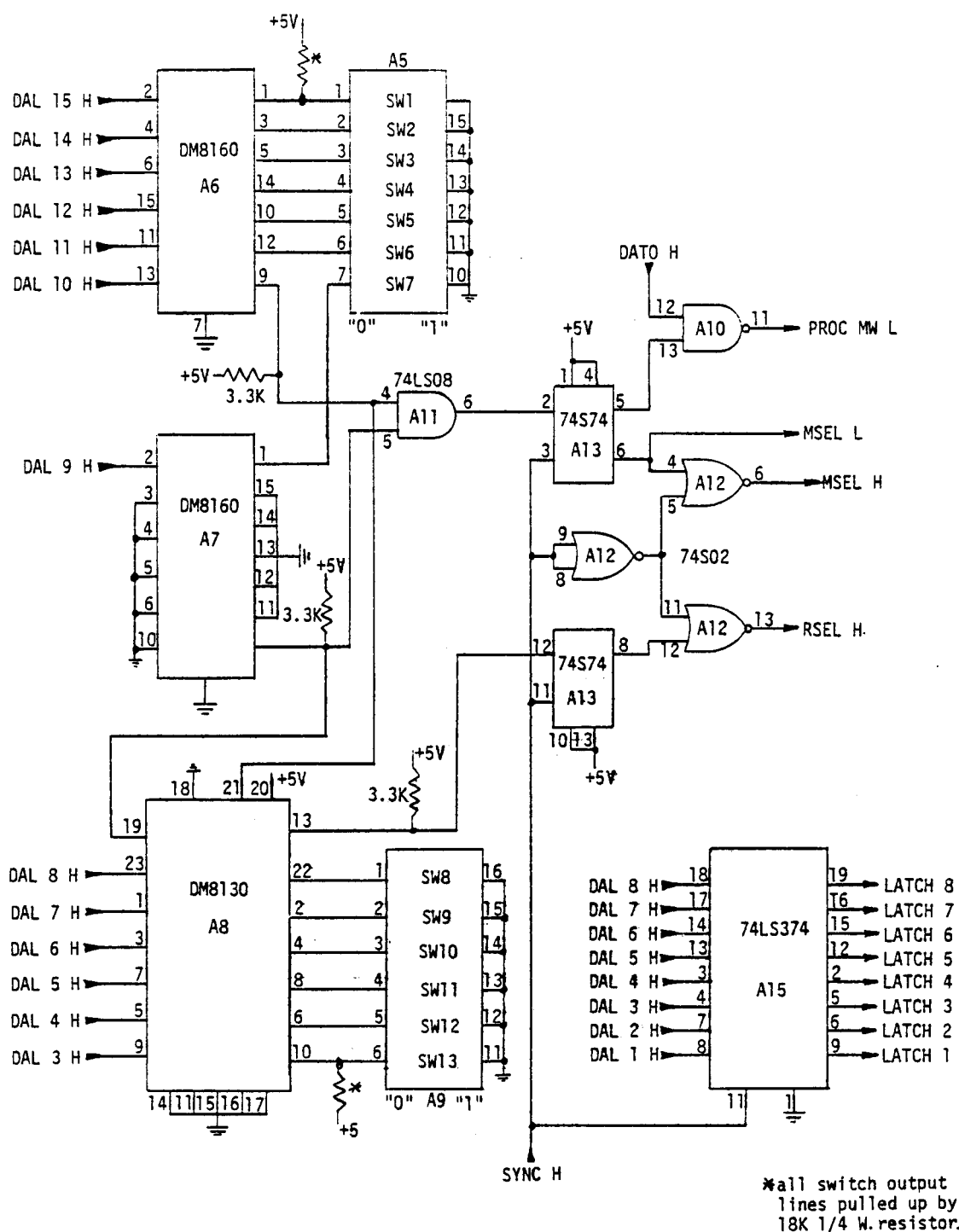


Figure 6.6. VDRC address decoding circuit.

a high signal on the line to the appropriate 74S74 flip-flop. These signals to the flip-flops are then clocked by SYNC H and combined with SYNC H through 74S02 NOR gates to produce a high signal on MSEL H or RSEL H, depending upon whether a memory location or register has been addressed. A 74LS374 8-bit latch shown latches bits one through eight of the address when clocked by SYNC H. This latch stores these bits of the address every cycle, regardless of whether a memory location or register of the VDRC is selected or not. These signals will stay set for the duration of the data transfer cycle and until the next SYNC H pulse occurs.

The addresses of the DTMM and register locations are selectable in the LSI-11 memory by setting the toggle switches. Since the DTMM requires a block of 256 words of memory space, only the high order seven bits are needed to select where the DTMM address block will be. Since bit 0 is used only for byte instructions, this leaves eight bits (bit 8 through bit 15) to relate the rest of the address to each of the 256 locations. Any 256 consecutive memory addresses not utilized by the processor may be used as the address block for these 256 words. Figure 6.7(a) shows the switch bit positions in the address format when compared with their location in Figure 6.6. The address of the DTMM runs from $XXX000_8$ to $XXX777_8$. The register locations are designed to be four successive word address locations. Their address is picked in part by the DTMM address. The interface sets the top six bits (bit 15 through bit 10) of both the memory and registers as the same address. Bit 9 for the address must be opposite for the DTMM and the register locations (see Figure 6.7). Bits three through eight are selectable to allow the registers to be put in any four consecutive locations of the 256 words

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW1	SW2	SW3	SW4	SW5	SW6	SW7									

(a)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW1	SW2	SW3	SW4	SW5	SW6	<u>SW7</u>	SW8	SW9	SW10	SW11	SW12	SW13			

Figure 6.7. Address switch positions for (a) the DTMM and (b) the registers.

addressed by the high order seven bits. The address format is shown in Figure 6.7(b) and the switch bit positions are shown compared with their location in Figure 6.6.

If a memory location has been selected, the MSEL L line is sent to the load input of the memory address counter, and the eight bits from the address latch are loaded into the counter (as described in Chapter 7) to locate and address the desired memory location. A DATO pulse from the processor will be combined with the Q output of the memory select flip-flop to give a PROC MW L, processor memory write low, as shown in Figure 6.6. This signal is sent to the control circuit to cause the data contained now on the bus to be written in the addressed memory location. The DTMM may also be loaded in bytes instead of words as will be explained shortly. A DATI signal from the processor is combined with MSEL H signal to produce MOUT L, memory out low, as shown in Figure 6.8, which allows the four transceivers to drive the bus with the data of the addressed memory location.

If a register has been addressed, the RSEL H line enables the 74LS155 two-to-four line demultiplexer which decodes the register selected from bits one and two of the eight latched address bits. The registers are, in order of address: vertical register, horizontal register, control register, and start/stop register. Their locations are $XXYXX0_8$, $XXYXX2_8$, $XXYXX4_8$, and $XXYXX6_8$, respectively. The size and use of these registers will be discussed in Chapter 7.

The vertical, horizontal, and start/stop registers need a positive edge clock pulse to receive new data. These pulses are formed by

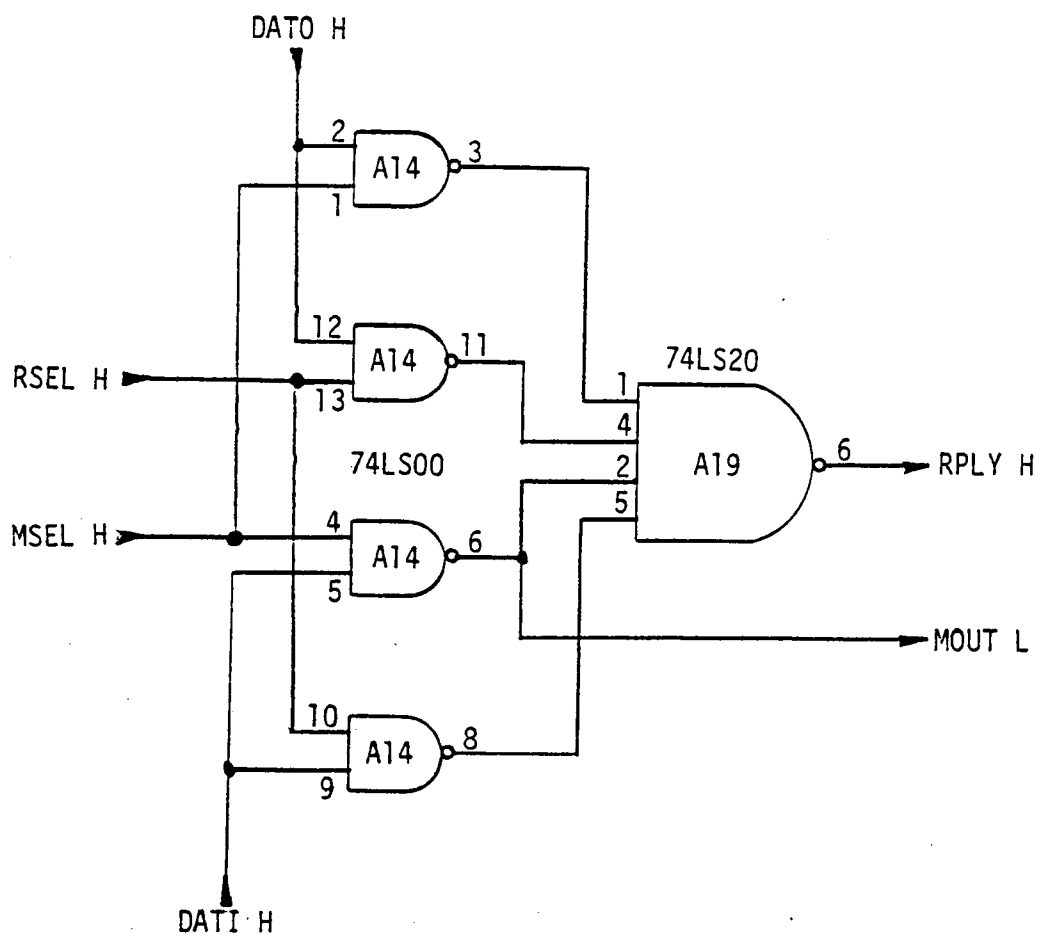


Figure 6.8. VDRC reply signal generation circuit.

combining the proper register selection line from the demultiplexer through an inverter with the DATO line from the processor, as shown in Figure 6.9.

Control register data input pulses are generated differently. The processor may write to the control register in high and low bytes instead of full words if so desired. Loading of the DTMM may also be accomplished in this way as mentioned earlier. In this mode of data transfer, the interface also uses the WTBT H, the write byte line, and bit 0 to determine which byte is to be loaded. The logic designed to accomplish this task is shown in Figure 6.10. DAL 0 H is clocked into the 74S74 flip-flop to determine whether the high or low byte is to be loaded. The outputs of this flip-flop are combined with the WTBT H line to determine if a byte instruction is being executed. If the instruction is to write a byte, the appropriate combination of WTBT H and the flip-flop outputs will produce a high signal. These signals will combine with the selected memory location or control register signal to produce the proper loading of the data. In the loading of a memory location, a signal, MBYT L or MBYT H, memory byte low or memory byte high, is produced before and lasts longer than the PROC MW L, thus blocking out the write pulse from the byte of the memory location which is not intended to be loaded. In the loading of the control register, the high or low byte instruction is combined with the signal, CNTL SEL L, to acknowledge that the control register has been selected. This combination is ANDed with the DATO pulse to produce CNTL HBYT or CNTL LBYT, the clock edge needed to load the proper byte of the register, as shown in Figure 6.10. Only the correct byte will receive a clock pulse. If WTBT H is low, no byte instruction is present and therefore the whole word will be loaded in the selected memory

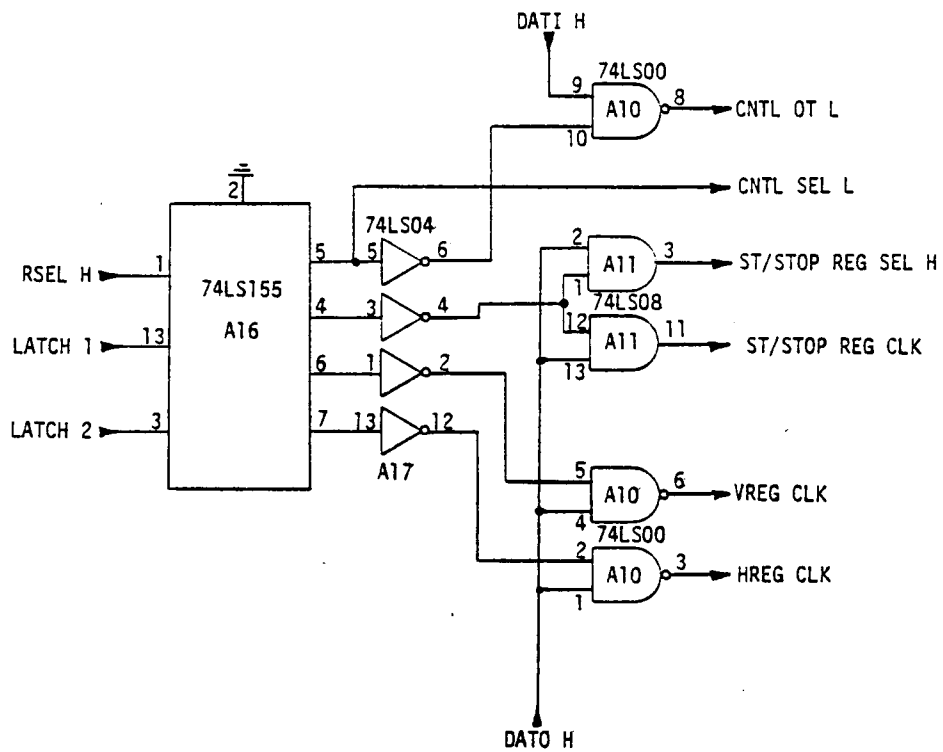


Figure 6.9. Register control logic.

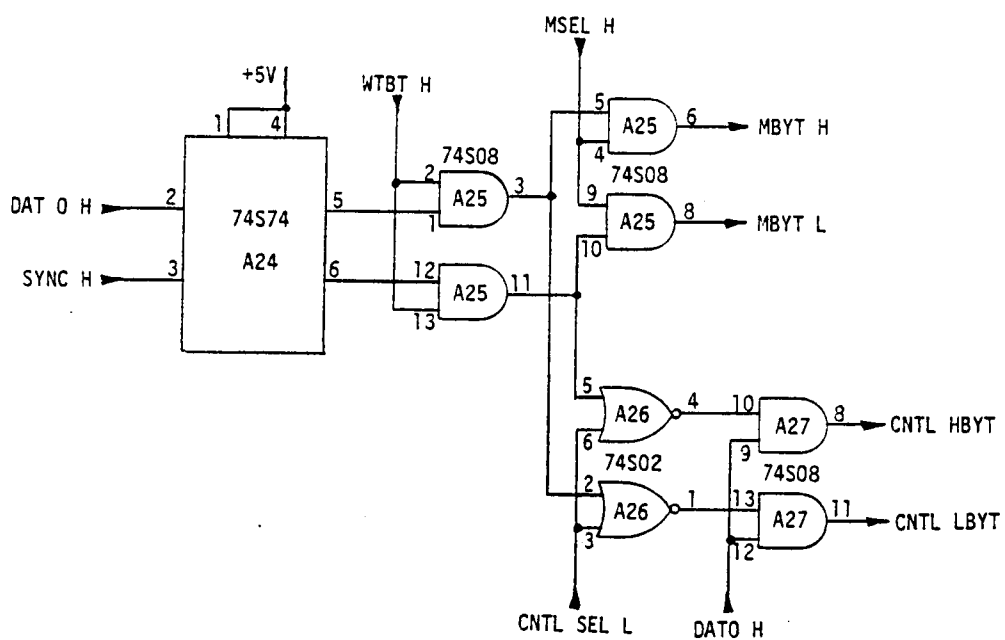


Figure 6.10. Memory and control register byte selection logic.

location or control register.

The control register and start/stop register are the only two of the four registers which can be read by the processor. The control register is read by the demultiplexer signal and DATI combining as in Figure 6.9 to send CNTL OT L, control out low, to the four transceivers mentioned previously. The start/stop register is read by the proper demultiplexer signal combining with DATI and also the Q output of the start/stop flip-flop which places the data of the register on the bus in the BDAL 0 L position.

After any action by the processor which results in an address of a memory location or register of the VDRC system being given, the processor waits for a reply from the system before continuing. A reply for the system is generated for all conditions by the circuit shown in Figure 6.8 and is connected to the bus by the open-collector gate already mentioned. This circuit takes the signals MSEL H and RSEL H and unites them with DATI H and DATO H in the four possible combinations and groups the results of these combinations to produce RPLY H.

One other line from the bus is used by the system. The INIT H line is sent through a NOR gate to invert the signal before sending it to various points in the control circuit. This INIT L line is active low, meaning a low signal produces an initialization of the system.

6.3. Signals Needed For Another Interface

As stated earlier in this chapter, the VDRC system could be interfaced with another microprocessor by constructing a new interface to replace the one presently used in the system. If such a replacement is

desired, this section briefly describes the signals needed by the VDRC system from the new interface.

To be able to read and write to the DTMM, the interface must place the last eight bits of the address in the memory counter. This counter requires a load pulse of a low level for approximately 30 nanoseconds with the address data set up for approximately 25 nanoseconds. The PROC MW L must be at least 50 nanoseconds to assure the data is properly written in memory during a write cycle with the data having a set up time of at least 15 nanoseconds. Also, if byte instructions are desired, the MBYT H or MBYT L must be activated before, during, and after the PROC MW L signal. A high signal on either of these lines causes that byte of the word to remain unchanged. The read cycle consists of the same loading procedure for the counter and whatever other signals are needed to place the data from the output multiplexers of the memory to the bus of the processor used.

To be able to read from and write to the registers, the following signals are needed. To write to any of the four registers, a positive edge clock pulse must be sent to the register after the data has been set up for at least 30 nanoseconds. The data should have a hold time of at least 10 nanoseconds after the clock positive edge. Byte instructions can be performed on the control register by supplying the clock pulse to only the byte which is to be written. To read from the registers requires the proper register output to be selected and placed on the bus of the processor used.

CHAPTER 7

THE CONTROL AND PIXEL LOCATION CIRCUITS

The control and pixel location circuits of the VDRC system receive instructions and data from the processor via the interface circuit discussed in Chapter 6. Operations in the remainder of the VDRC system are performed through commands generated in these circuits. Due to the speed at which the system operates, these circuits are constructed totally of hardware logic. Table 7.1 lists the signal lines to and from these circuits and the figure corresponding to their origin or destination, respectively, in the remainder of the VDRC system.

7.1. Basic Building Blocks of the Control and Pixel Location Circuits

The control and pixel location circuits are composed of eleven basic blocks interconnected as shown in Figure 7.1. These blocks accept the signal and data lines from the processor interface circuit and generate the "lines out" signals listed in Table 7.1 from the appropriate block shown in the figure.

The first block is the control register which is shown in Figure 7.2. Information selecting the proper DTMM to be addressable by the processor, the video source sampling mode, the sample rate, and the number of sample points desired to be stored in the DTMM from the incoming video source are contained in this register. Proper bit locations containing this information are shown in Figure 7.3. Table 7.2 lists the options for each selection and the bit values associated with each option. The number of sample points requested for storage may not exceed the

TABLE 7.1

SIGNAL AND DATA LINES IN AND OUT OF THE
CONTROL AND PIXEL LOCATION CIRCUITS

Lines In	Lines Out	Reference Figure
DAL 0 H - DAL 15 H		6.4
CNTL LBYT		6.10
CNTL HBYT		6.10
	CNTL 10 H - CNTL 12 H	7.2
	MASTER CLK	7.4
	SAMPLE	7.5
	CAM B L	7.8
	A SEL	7.8
	B SEL	7.8
	CAMSEL A	7.8
	CAMSEL B	7.8
	D/A SEL A	7.8
	D/A SEL B	7.8
	ALATCH CLK	7.9
	BLATCH CLK	7.9
	DTMM A CLK	7.10
	DTMM B CLK	7.10
	OUTMUX SEL	7.11
	OUT CLK	7.11
	D/A CLK	7.11
VREG CLK		6.9
HREG CLK		6.9
PROC MW L		6.6
	DTMM HBYT H	7.18
	DTMM LBYT H	7.18
	MEM WT L	7.18
	MEM HBYT L	7.19
	MEM LBYT L	7.19
MBYT H		6.10
MBYT L		6.10
ST/STOP REG CLK		6.9
	ST/STOP REG	7.20
CNTL SYNC		5.2
	MSEL 0	7.19
	MSEL 1	7.19
	VERT RET	7.22

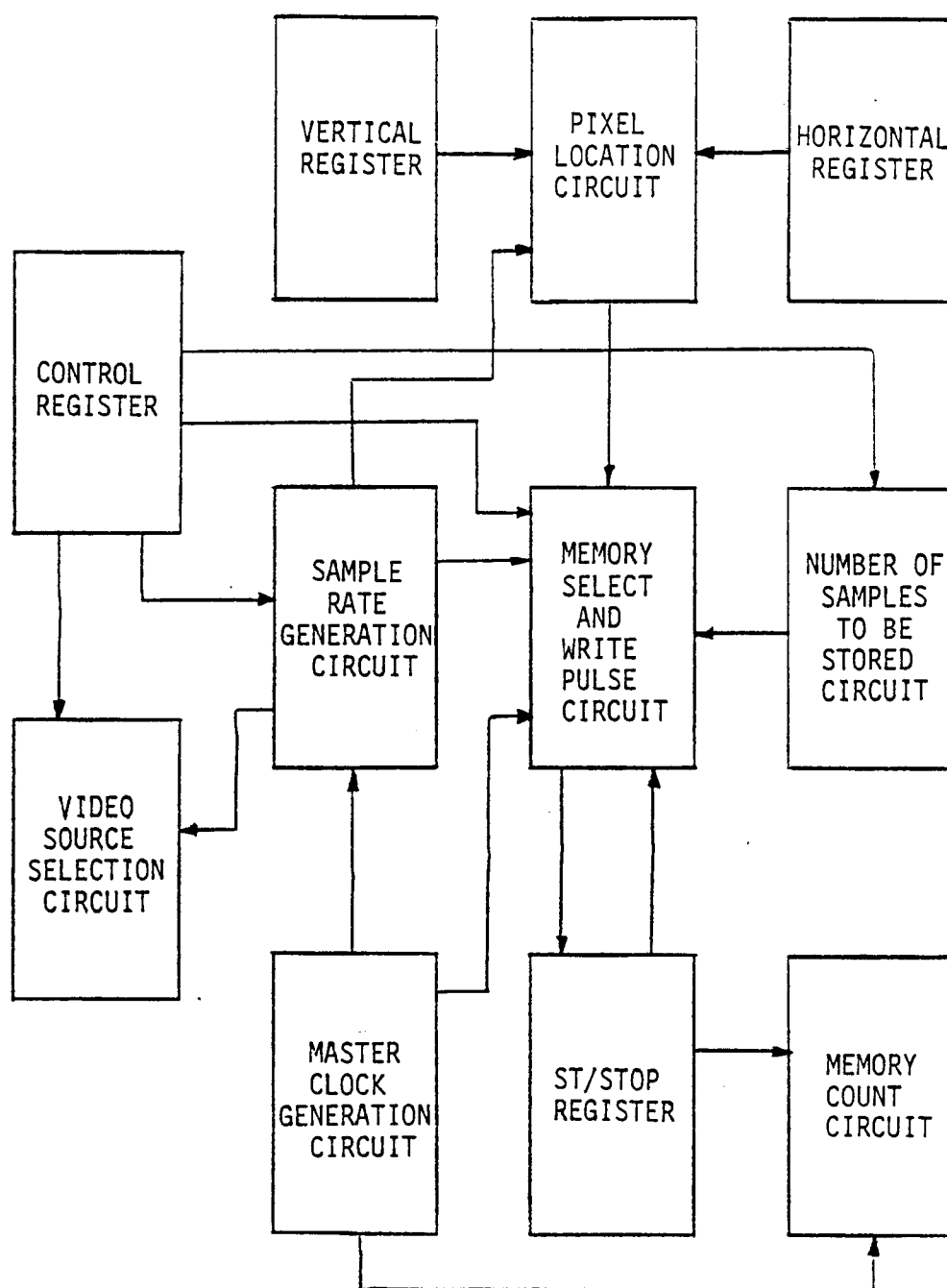


Figure 7.1. Basic block diagram of the control circuit and Pixel Location Circuit (PLC).

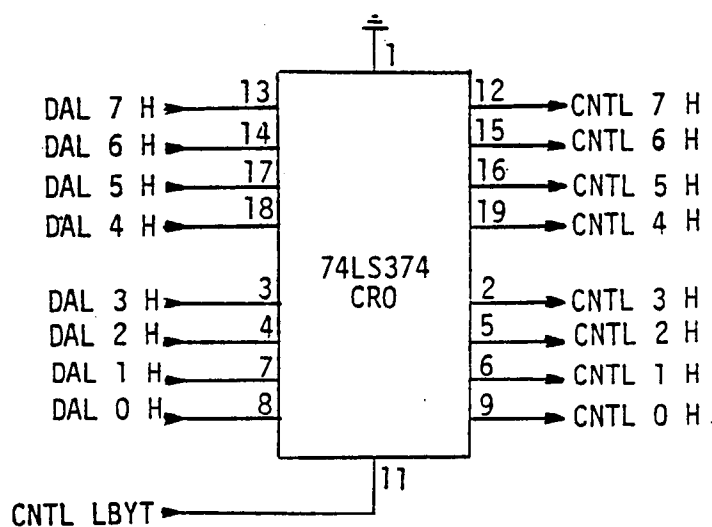
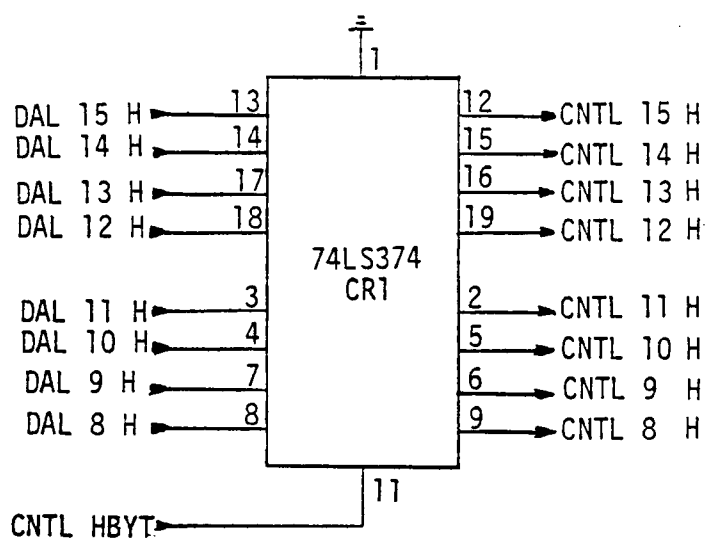


Figure 7.2. The control register.

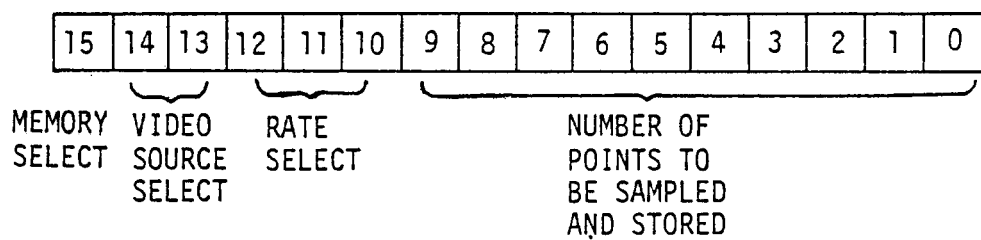


Figure 7.3. Control register bit assignments.

TABLE 7.2

BIT ASSIGNMENT OF THE CONTROL REGISTER
AND THE ASSOCIATED OPTIONS

Memory Select

Bit 15

- 0 - DTMM 0 under processor control
- 1 - DTMM 1 under processor control

Video Source Select

Bits 14 13

- 0 0 Sample video source A only
- 0 1 Sample video source B only
- 1 0 Sample video source A & B, store B
- 1 1 Sample video source A & B, store A

Rate Select

Bits 12 11 10

- 0 0 0 Sample 928 points per horizontal line
- 0 0 1 Sample 464 points per horizontal line
- 0 1 0 Sample 232 points per horizontal line
- 0 1 1 Sample 116 points per horizontal line
- 1 0 0 Sample 58 points per horizontal line
- 1 0 1 Sample 29 points per horizontal line

Number of Sampled Points for Storage

Bits 9 - 0 Any even number between 2 and 720g, inclusive

sample rate value selected minus the horizontal register value, otherwise erroneous data will be stored.

The master clock generation circuit is shown in Figure 7.4. A digital delay device which has 10 nanoseconds per tap delay and three inverters connected in the configuration shown produce the master clock signal which is TTL compatible. An output of 17.5 megahertz is produced which drives the circuitry for the rest of the system.

The SAMPLE pulse is generated by the circuit shown in Figure 7.5. The counters shown are clocked by the master clock rate and produce the five lower sample rates as shown. Proper rate selection is provided through the demultiplexer shown in Figure 7.6 and controlled by the sample rate bits of the control register. Sample rate generation is reset by each new horizontal line scan to assure the sample points will occur at the same location on each horizontal line. The proper reset signals are produced by the circuitry in Figure 7.7. An inverted sync pulse triggers the first of two multivibrators to disable the generation of the SAMPLE pulse. A second multivibrator resets the counters. The flip-flop shown in Figure 7.5 provides the reset of the SAMPLE pulse when the fastest sample rate is selected. Each SAMPLE pulse leading edge is produced by the falling edge of the appropriate counter output, a procedure which causes the SAMPLE pulse for all rates to fall at the same place on the horizontal line scan. The sync signal, CNTL SYNC, used by the control circuit is delayed as discussed in Chapter 5 to cause the SAMPLE pulses for each rate to start at the appropriate location on the incoming video information signal.

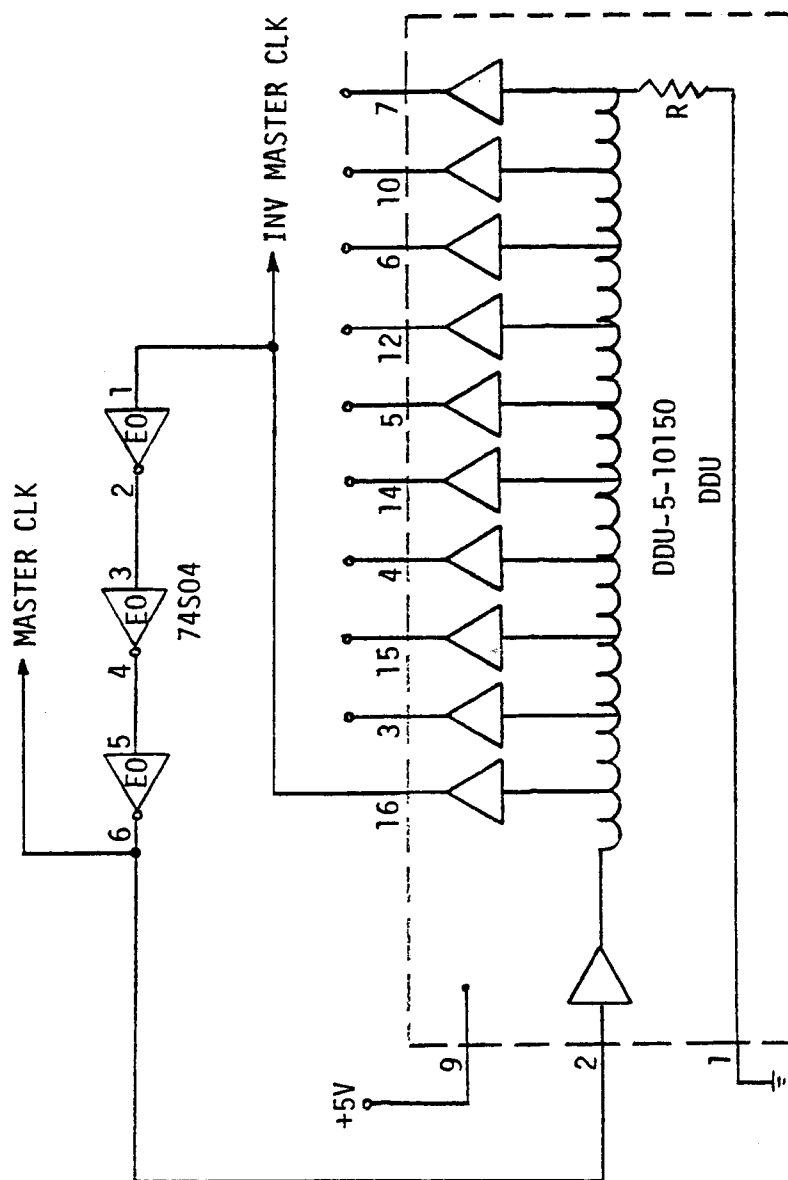


Figure 7.4. Master clock generation circuit.

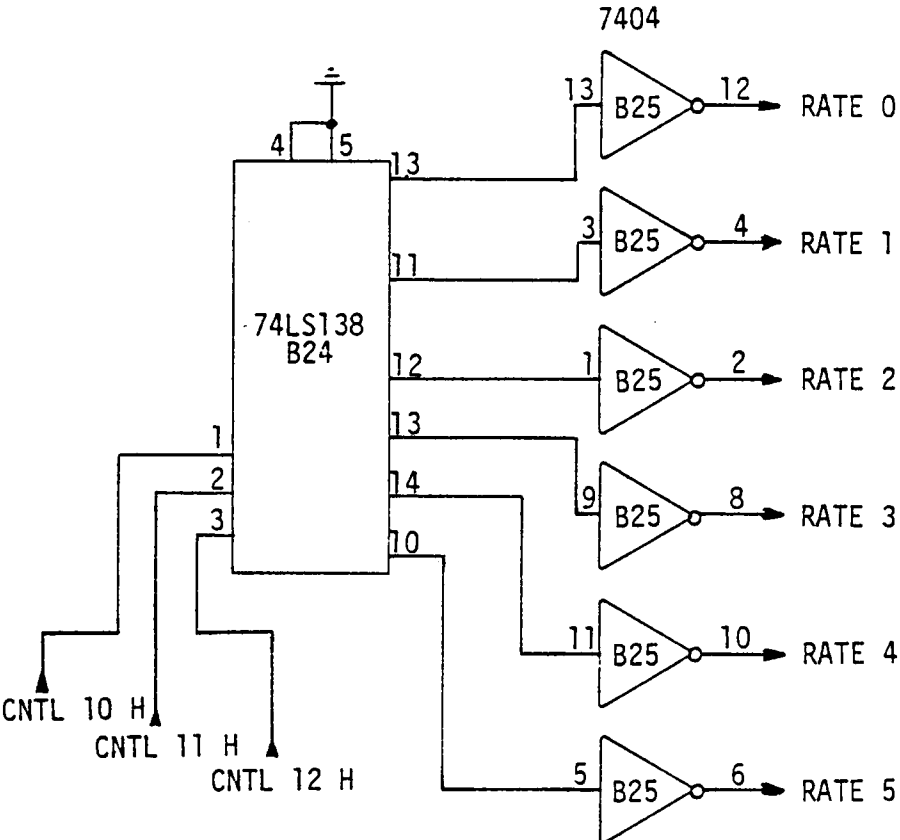


Figure 7.6. Sample rate selection circuit.

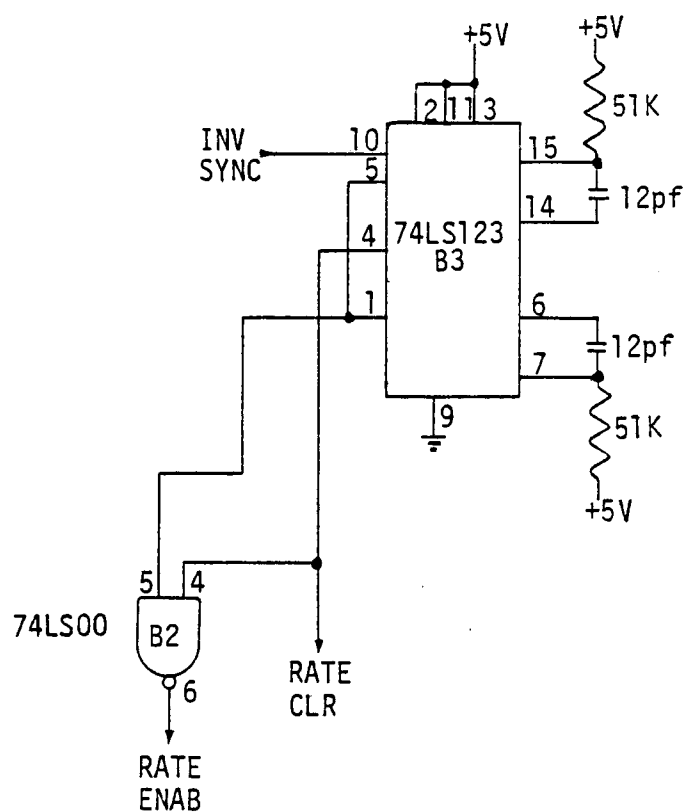


Figure 7.7. Sample rate reset signals.

Proper video source selection for sampling is determined by the circuit shown in Figure 7.8. Using bits 14 and 13 of the control register, the demultiplexer decodes the selection from the four possible choices listed in Table 7.2. If only one video source is selected to be sampled, the flip-flop which generates CAMSEL A and CAMSEL B will be cleared or set depending upon whether video source A or B is selected, respectively. If a stereo sampling mode is selected, the flip-flop acts as a toggle flip-flop and is clocked by the INV SAMPLE pulse to cause samples to be alternately taken from the two video sources. Which video source is sampled first is selected by appropriately setting or clearing this flip-flop with signals generated by the RATE CLR signal and the demultiplexer outputs as shown in the figure. A low signal allows a video source to be sampled. This circuit also generates the D/A SEL A and D/A SEL B lines by similar means as shown in the figure. A high signal on these lines selects the D/A converter desired. Selection of the proper latch for storage of the data from the output of the A/D converter is also chosen in this circuit. This latch selection depends upon the mode of operation as well as the sample rate of the system. If either stereo sampling mode or the fastest sample rate is selected, both latches are used. The cases of only one video source sampled at any rate except the fastest rate require only one latch, therefore only A SEL is set. A high signal on the A SEL and B SEL combined with the SAMPLE pulse, as shown in Figure 7.9, causes the corresponding latch to be clocked. The extra gates are needed to provide the time for proper data set up before the clocking of the latches to assure proper data transfer will occur.

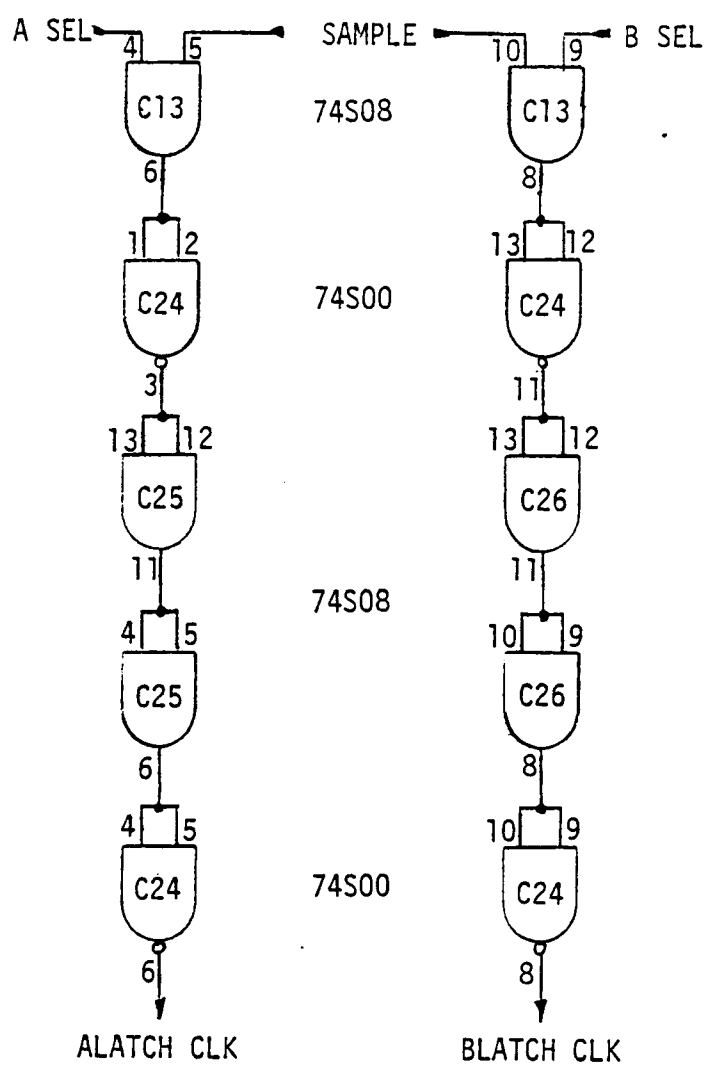


Figure 7.9. ALATCH CLK and BLATCH CLK logic.

The latches on the output of the DTMM are clocked by the signals generated in the circuit shown in Figure 7.10. These circuits are basically gate delays which take ALATCH CLK and BLATCH CLK and produce DTMM A CLK and DTMM B CLK to latch the transformed data on the output of the memory chips in the DTMM. Proper multiplexer selection for the data to be sent to the output latch from the high and low bytes of the proper DTMM is controlled by the circuit shown in Figure 7.11. Generation of the output latch clock, OUT CLK, as well as the D/A converter clock, D/A CLK, are also shown in the circuit.

The vertical register shown in Figure 7.12 is loaded by the processor with the value of the horizontal line from which sample points are to be stored in the DTMM for processor use. Any value between 0 and 737_8 may be selected. This value will not change until the processor loads a new number in this location.

The horizontal register shown in Figure 7.13 is loaded with the sample point value which is the starting sample point to be stored in the DTMM for processor use. This value has a range from zero to a maximum number equal to the sample rate value. No change in value will occur in this register until the processor loads a new number.

The circuit shown in Figure 7.14 performs the function of generating the value of the proper number of sample points to be stored in the DTMM from the number loaded in the control register by the processor. A new value which is two less than the original number is the resultant output of this circuit. The use of the new number will be discussed later in this section.

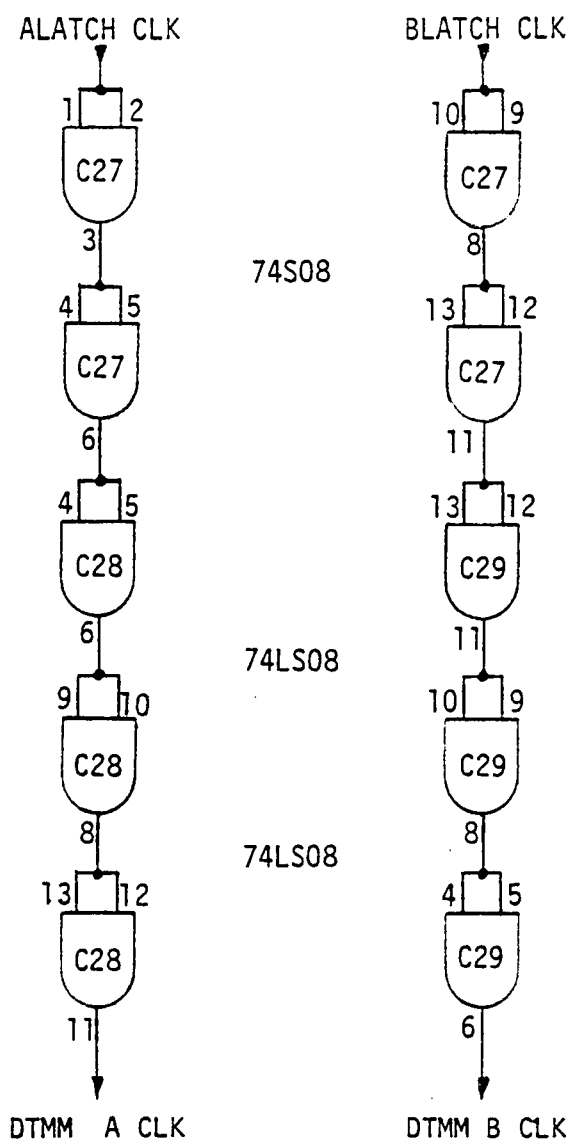


Figure 7.10. DTMM A CLK and DTMM B CLK logic.

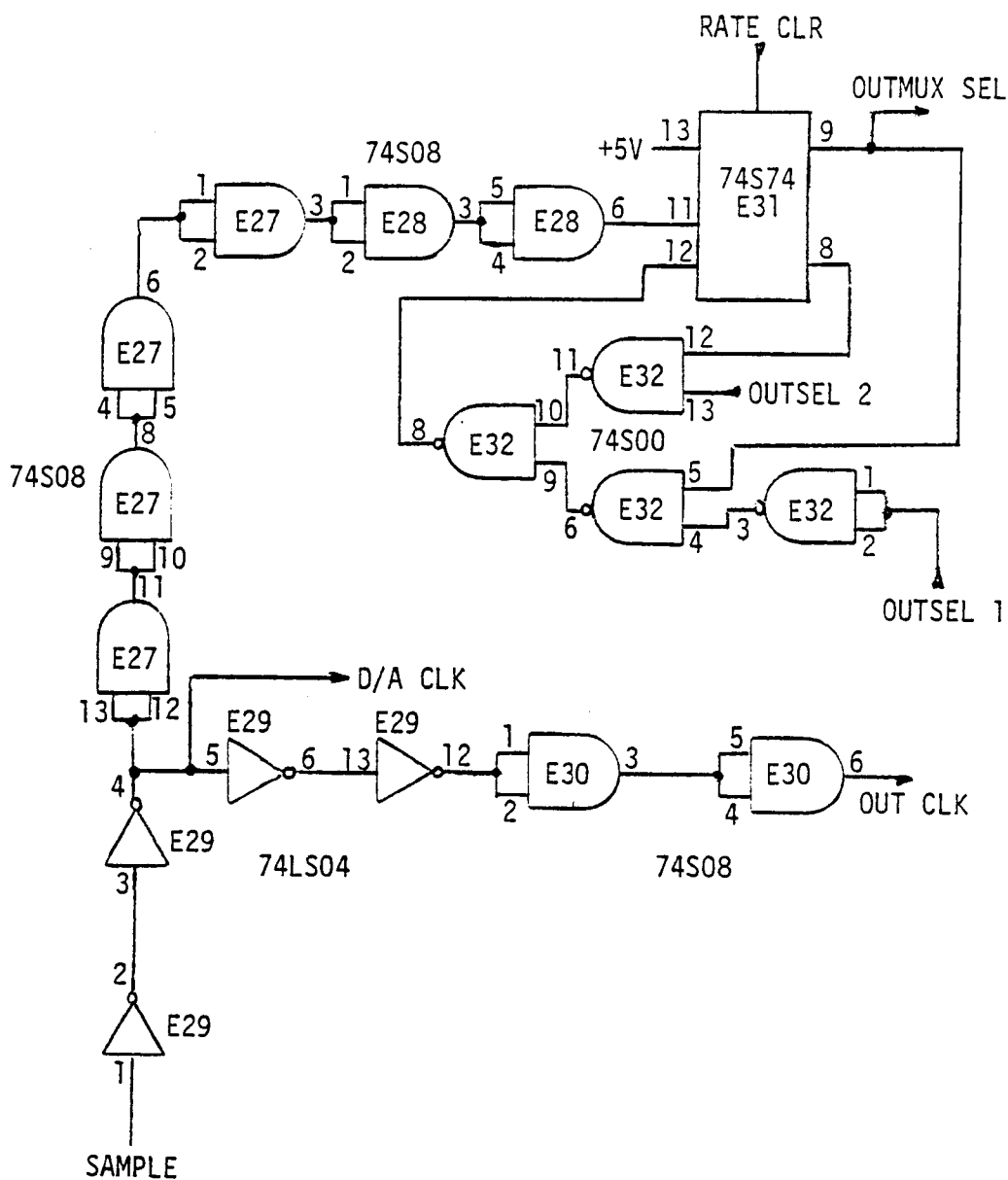


Figure 7.11. OUTMUX SEL, OUT CLK, and D/A CLK logic.

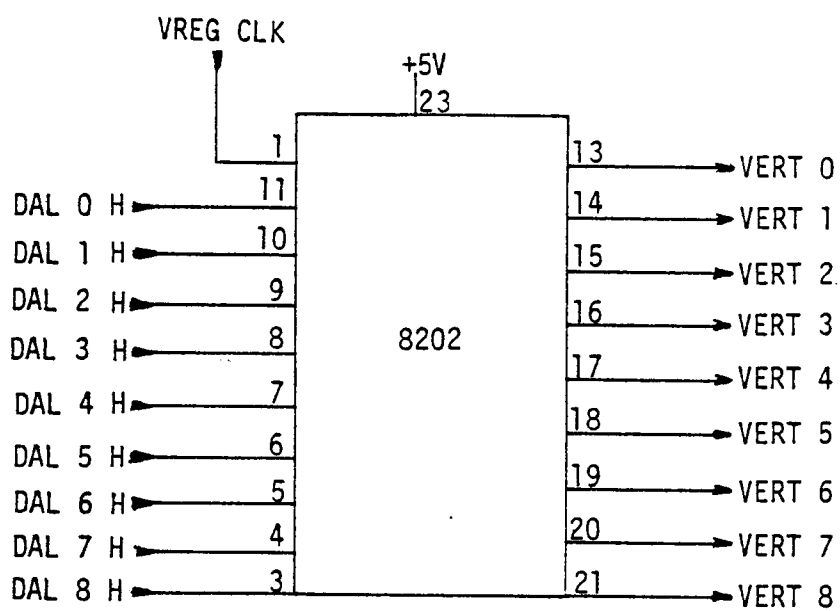


Figure 7.12. The vertical register.

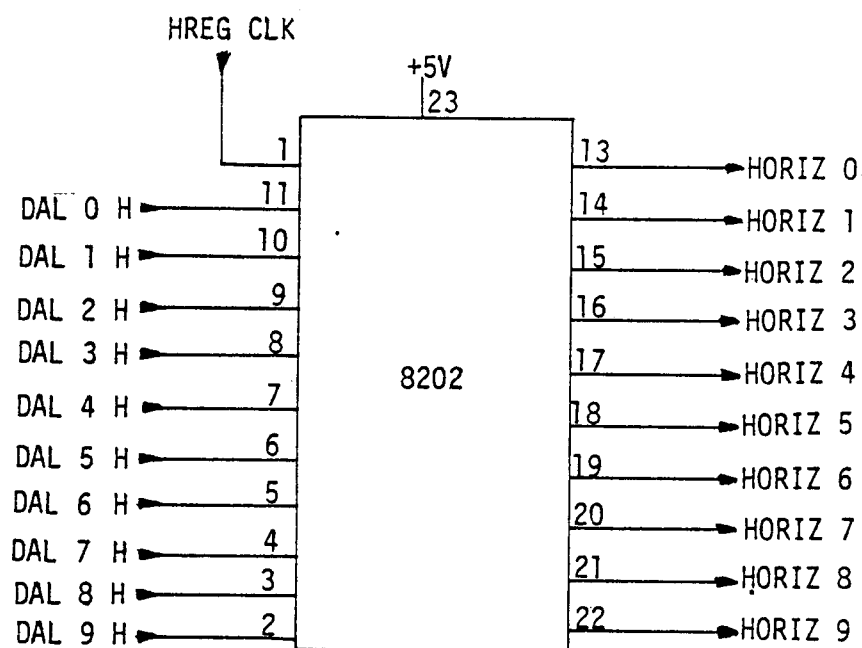


Figure 7.13. The horizontal register.

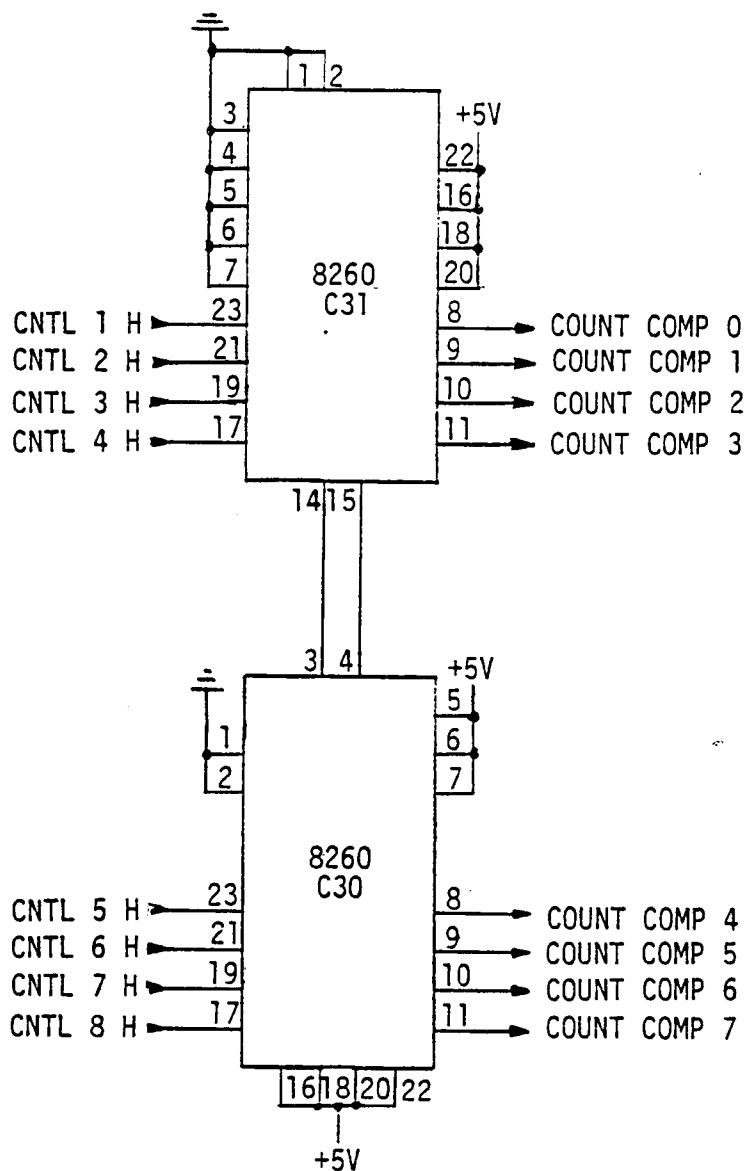


Figure 7.14. Generation of the proper number of points to be sampled.

The proper memory address is generated in the circuit shown in Figure 7.15. COUNT 0 through COUNT 7, the memory address for the DTMM under processor control, is generated by the counter shown in the figure. When the system stores sample points in the DTMM, the counter is reset to zero and counts up to generate the address value. In this manner, the sample points are stored in successive memory locations starting at the lowest addressable location of the DTMM. When the sampling process is complete, the address is produced by the processor. This arrangement is accomplished by allowing LATCH 1 through LATCH 8 to be loaded in the counter when the processor addresses the DTMM. The counter is disabled from counting when the storage of sample points is not in progress so the counter will hold this value given as the address. Resetting of the counter to zero when new sample points are to be stored is accomplished by the multivibrator shown in the figure. It creates a reset pulse to clear the counter when the signal to start storing points is given. The 74LS85 comparators take the value of the counter and the revised number of points to be stored and produce a signal when they are equal, signifying the number of points desired has been stored. Changing the value of the number of points to be stored by two is needed since two more sample points are stored after the equal signal is given by the comparators. This procedure was necessary to insure proper storage of the sample points occurs at all sample rates, and only the number of sample points requested are stored in the DTMM. Incrementing of the counter occurs only after the storage of every two samples to allow a sample to be stored in first the low byte and then the high byte of each address.

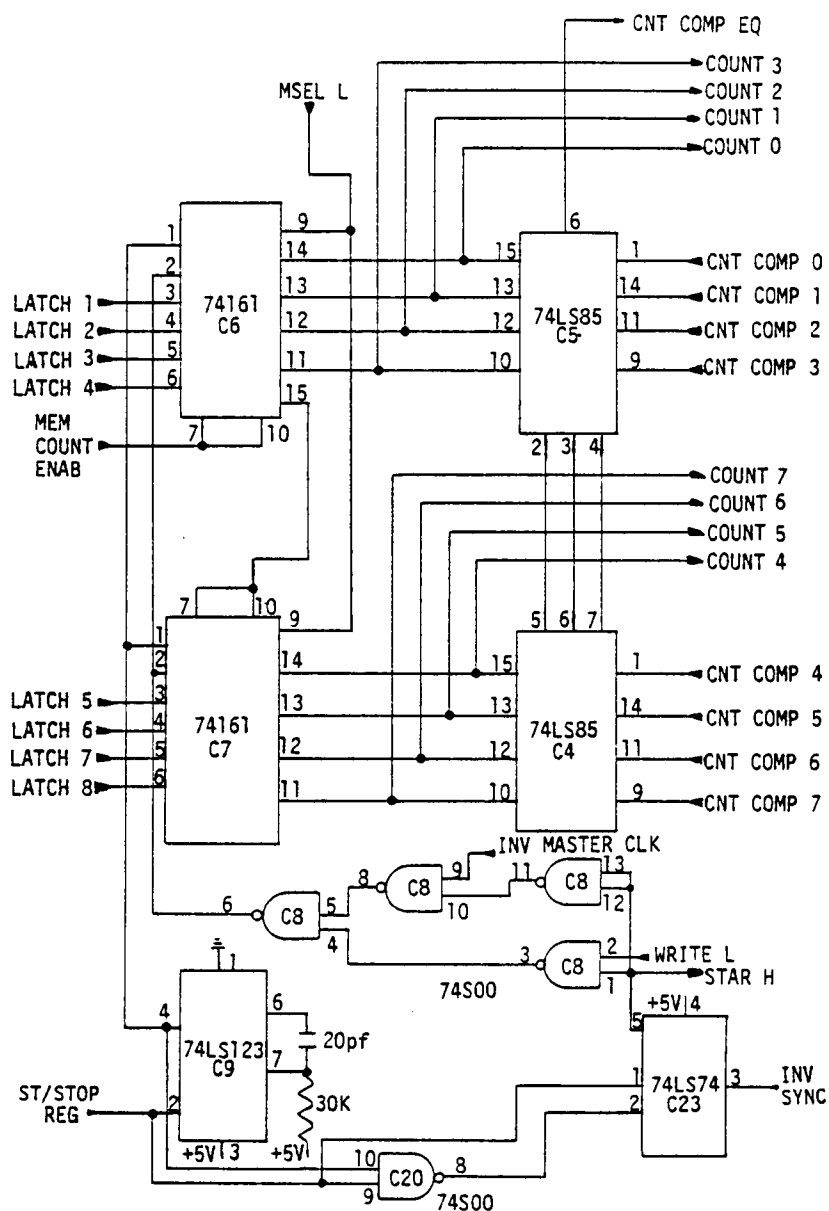


Figure 7.15. Memory count generation circuit.

The circuit which signifies the completion of the storage process is shown in Figure 7.16. The flip-flop is set when the process begins which allows the storage process to occur. When the process is complete, the four-input NAND gate produces a write clear pulse, WRITE CLR, which stops the storage of sampled points in the DTMM and also triggers the multivibrator shown in the figure, clearing the start/stop register. Clearing of the start/stop register resets the flip-flop which stops the storage process.

The proper write pulses are generated in the circuit shown in Figure 7.17. Three flip-flops arranged as shown produce the write pulses at the proper times for both the storage of sample points and also a processor write instruction. Write pulses for the storage of sample points are produced only after new data has been clocked into the ALATCH. The write pulse generation begins when the sample point location selected by the horizontal and vertical registers has been reached and continues until the correct number of samples has been stored, as mentioned earlier. WRITE H and WRITE L pulses are sent to the circuit shown in Figure 7.18. This circuit selects the proper DTMM for storage of sample points and routes the MEM WT L to that memory section. When storing sample points, WRITE L causes the low and high bytes to alternately store sample points. Such a procedure allows the storage of sample points in the DTMM to be loaded in the low byte and then the high byte of each memory location. When the storage process is complete, the signals to both bytes of the DTMM are pulled high to allow the processor to address both bytes if desired. When addressed by the processor, the MEM WT L pulses are

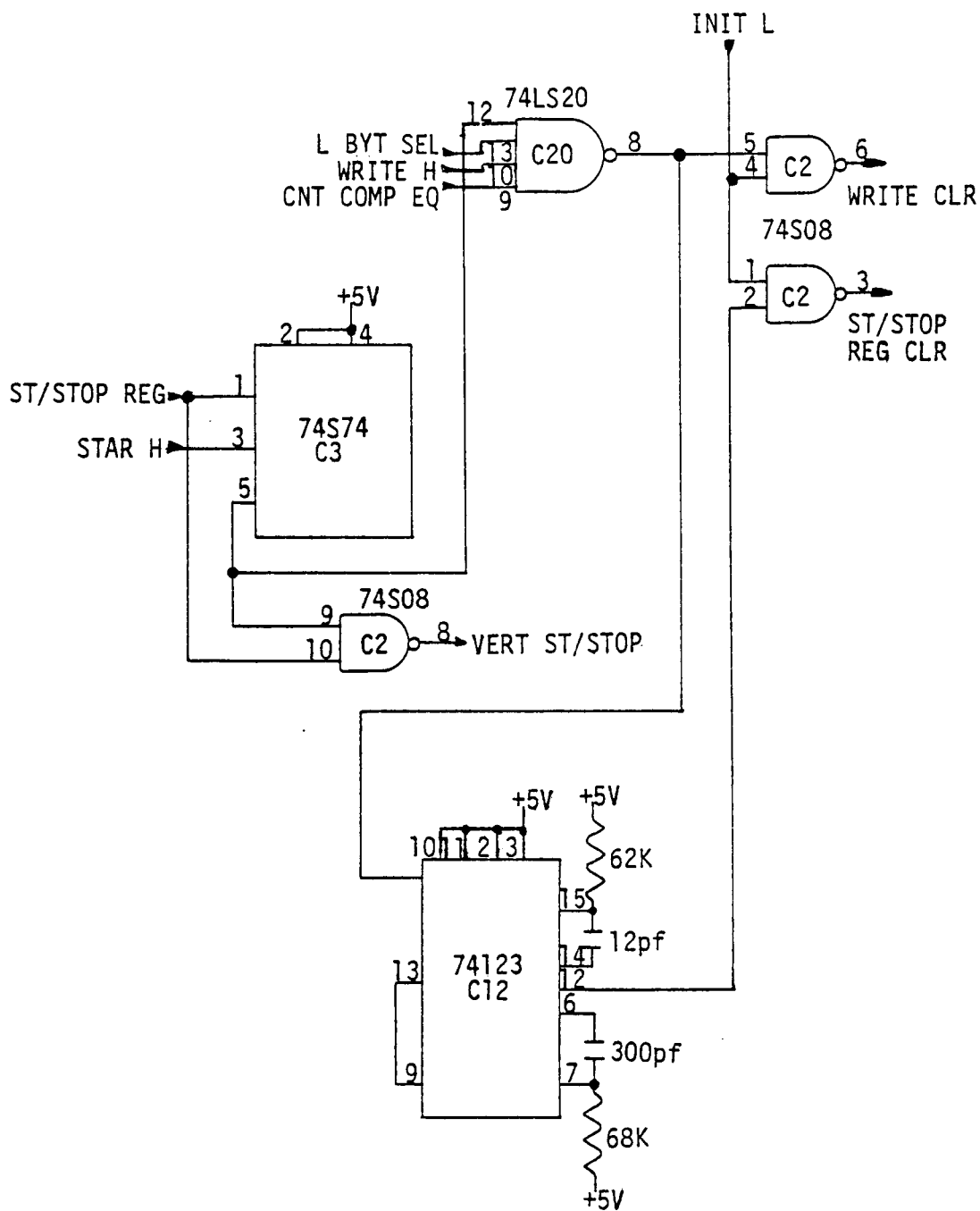


Figure 7.16. Storage completion circuit.

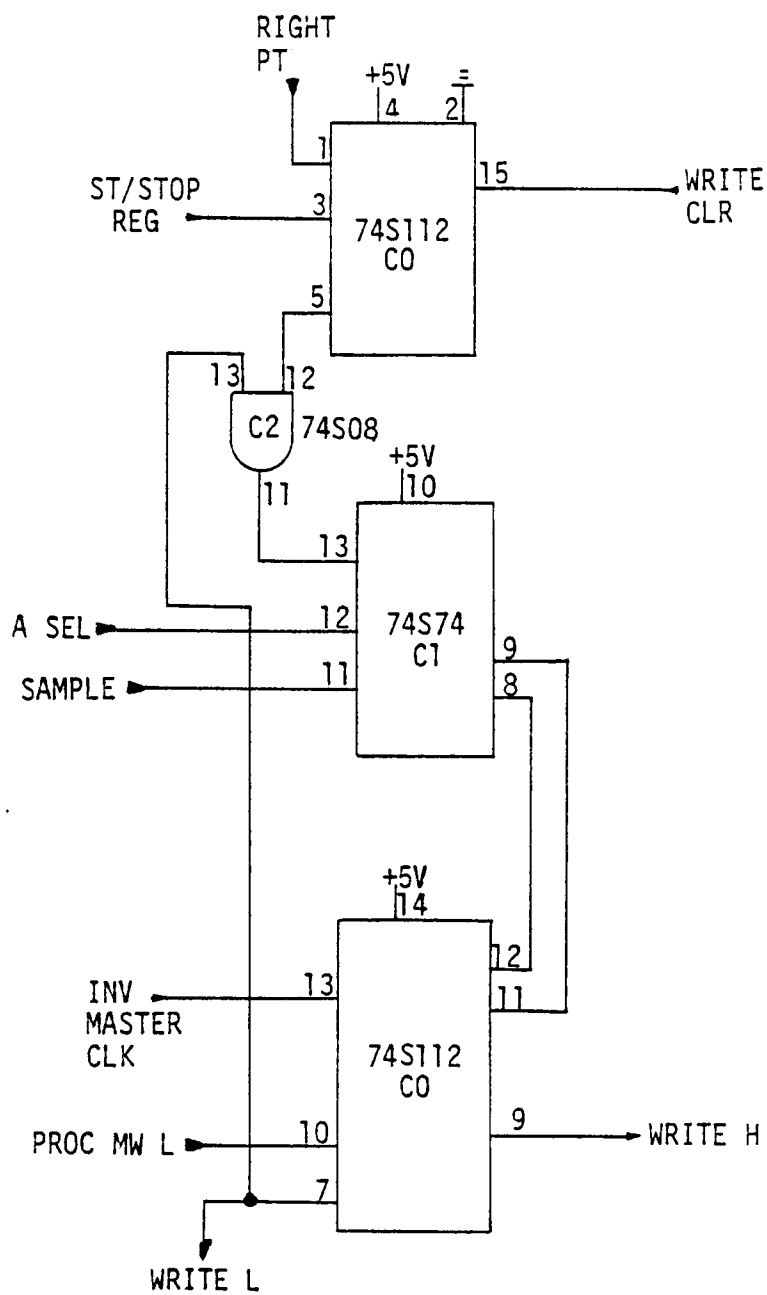


Figure 7.17. Write pulse generation logic.

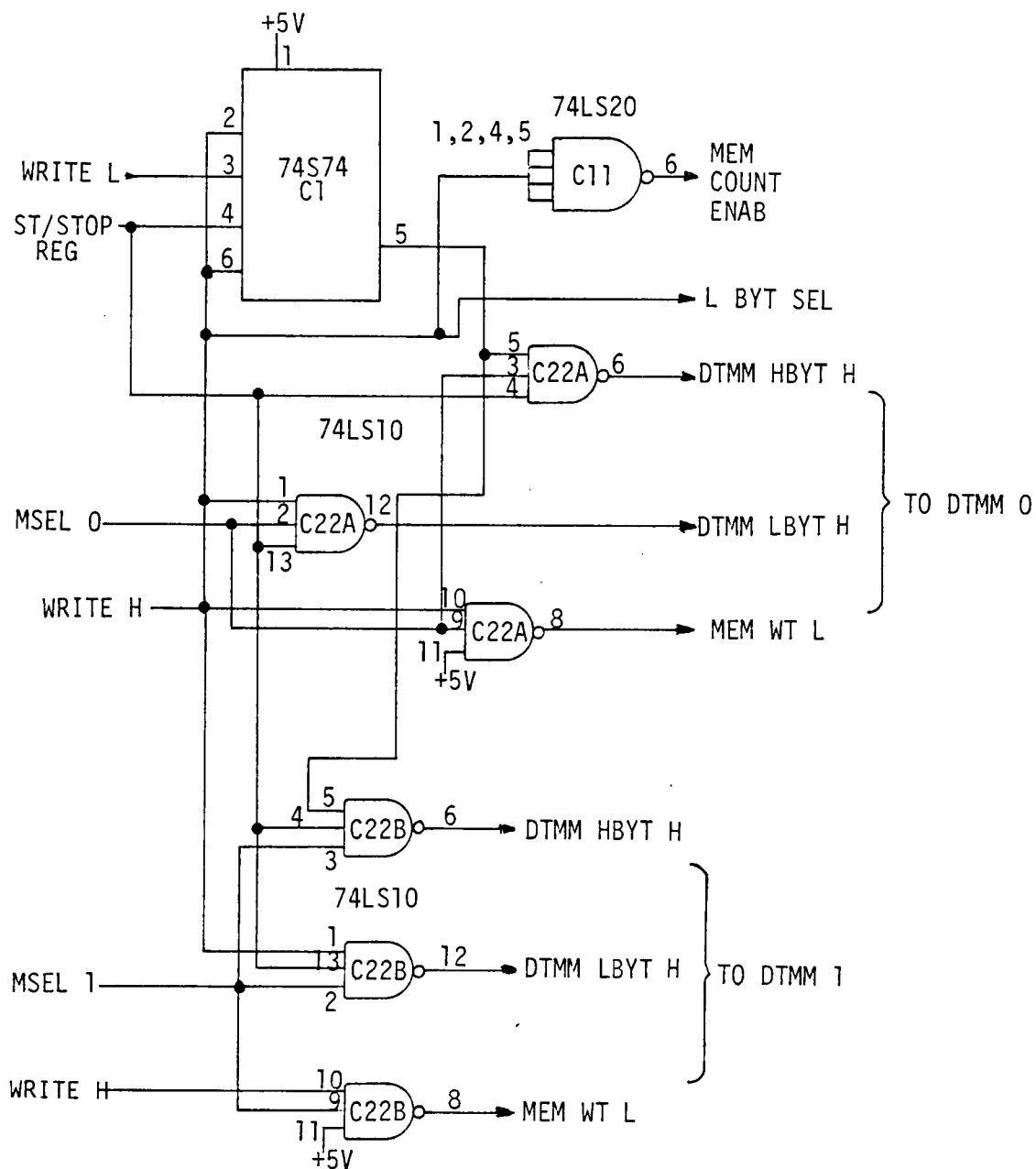


Figure 7.18. Memory storage selection logic.

generated when the circuit receives a write command from the processor. Write commands affect only the DTMM selected to be addressable by the processor. The circuit shown in Figure 7.19 selects the proper byte of memory to be loaded if byte instructions are used by the processor.

The process of storing sample points in the DTMM is controlled by the start/stop register shown in Figure 7.20. Setting of this register by the processor causes the operation of locating and storing the sample points to begin. This register will stay set until the process is complete. Upon completion, the system will clear the register to signify the process is over. An initialization pulse by the processor will also clear this register.

7.2. The Pixel Location Circuit

For the VDRC system to operate correctly and store only the sample points desired, the Pixel Location Circuit (PLC) is needed. This circuit provides the VDRC system with the capability of finding any pixel location possible on the incoming video information. Using the coordinates given by the horizontal and vertical registers, the PLC signifies when the desired pixel location has been reached. The system will then store the desired number of sample points in the DTMM.

The PLC uses the composite sync signal, CNTL SYNC, to determine the location on the video information at any given time. Figure 7.21 shows the first portion of the PLC which determines if a full horizontal line scan or an equalizing pulse has been detected and signifies whether the even or odd field of video information is being sampled. Enabling and loading of the equalizing pulse counters is also controlled in this portion of the circuit.

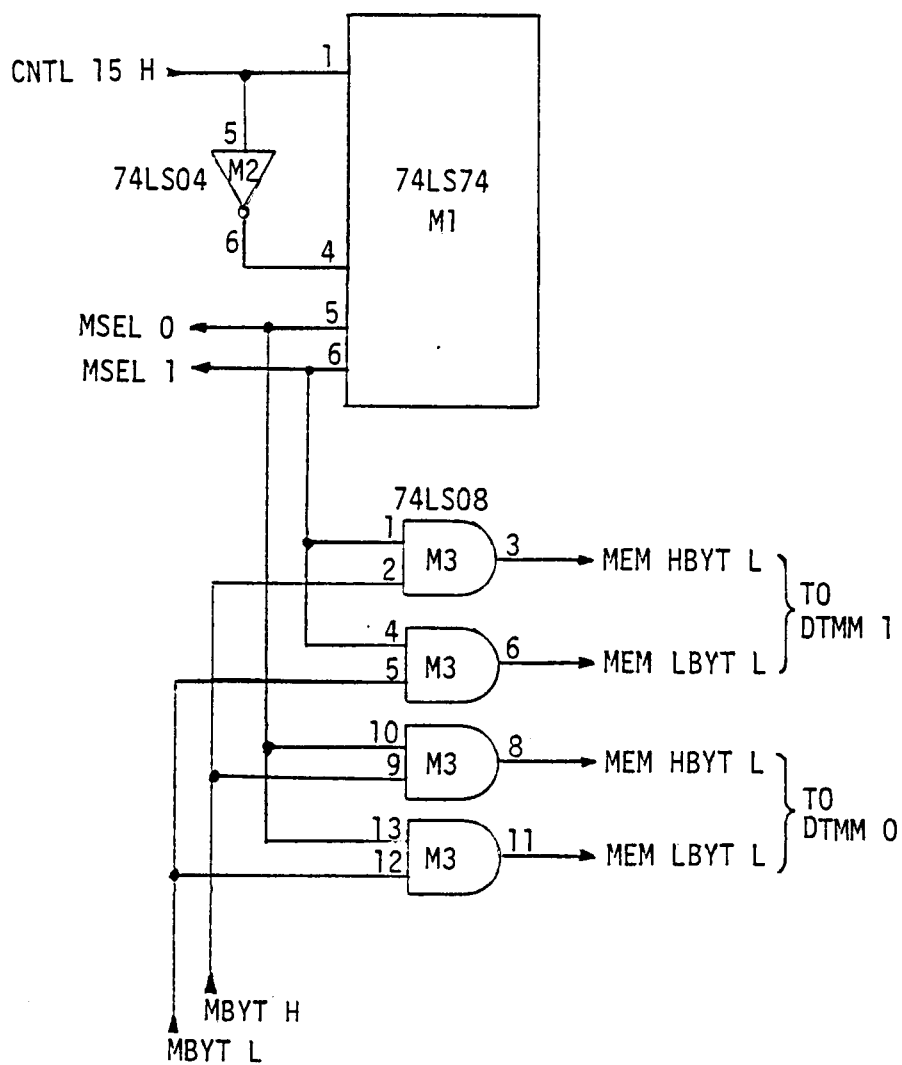


Figure 7.19. Memory selection circuit.

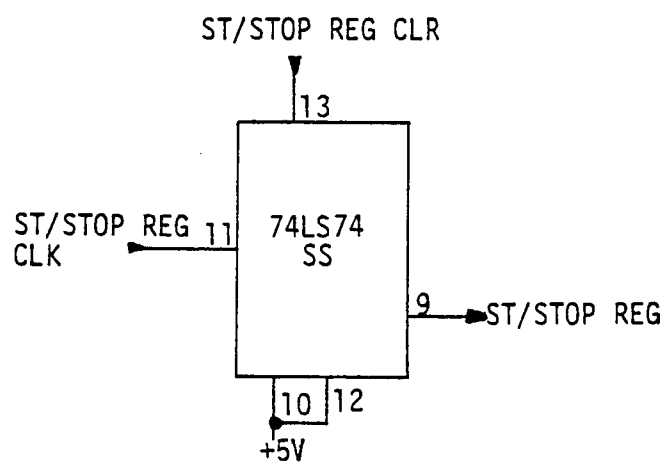


Figure 7.20. The start/stop register.

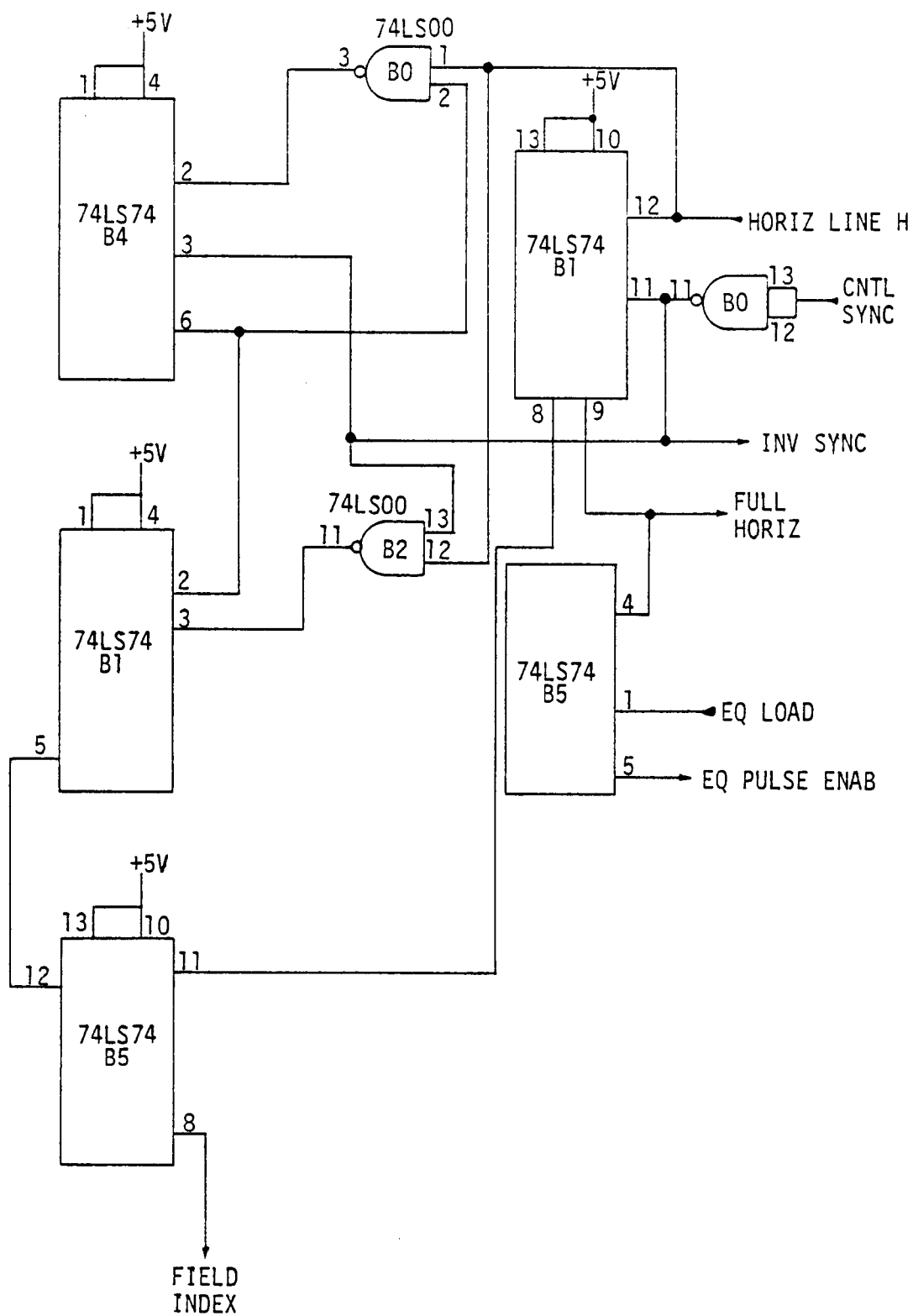


Figure 7.21. Full horizontal line indicator and field index circuit.

Figure 7.22 contains a portion of the PLC which detects and counts the equalizing pulses. The blanking interval of each vertical retrace is also taken into account by this circuit. Points are not allowed to be stored in the DTMM when this circuit is in operation, thus only sample points which are from the viewed video information may be requested for storage. Lines 39 through 518 of each frame of 525 lines are considered as the viewed video information by the system when sample points are requested for storage.

Figure 7.23 counts the horizontal line sync pulses when enabled by the equalizing pulse circuit. The output of its counters are compared with the line desired by the vertical register. VERT LINE H is set when the proper line requested has been located. Proper field selection is also taken into account by this circuit and the signal will be set only if the start/stop register is set. These counters are reset at the end of each field.

Figure 7.24 details the horizontal rate counters. Location of the sample point on a horizontal line that is requested by the horizontal register is performed by this circuit. A comparison is made on each horizontal line but will only be true when the proper horizontal line is first found by the horizontal line counters. Once the right line and point have been located, a pulse, RIGHT PT, signifying the right point has been reached is sent to the rest of the control circuit to start the storage of sample points in the DTMM.

Since the PLC uses the entire composite sync signal and counts each sync pulse to determine the location of desired pixel points, the requirement of a standard sync signal is necessary as mentioned earlier. The

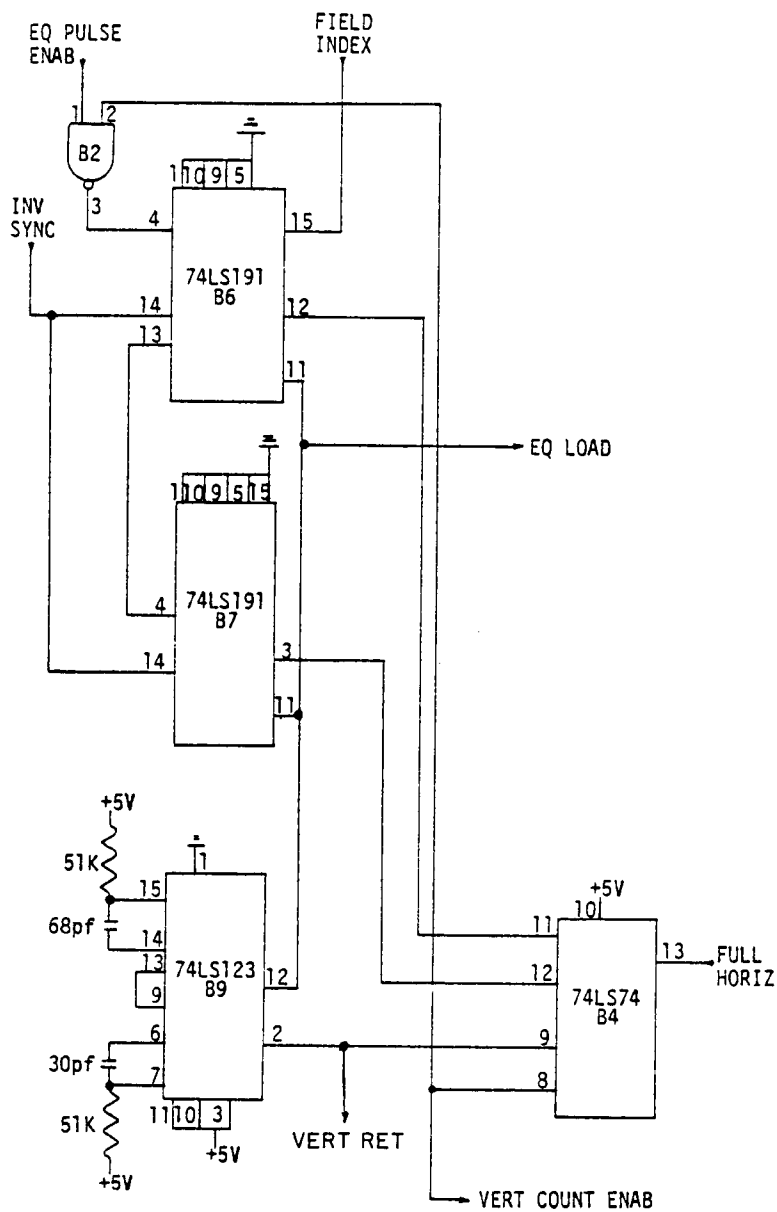


Figure 7.22. Equalizing pulse circuit.

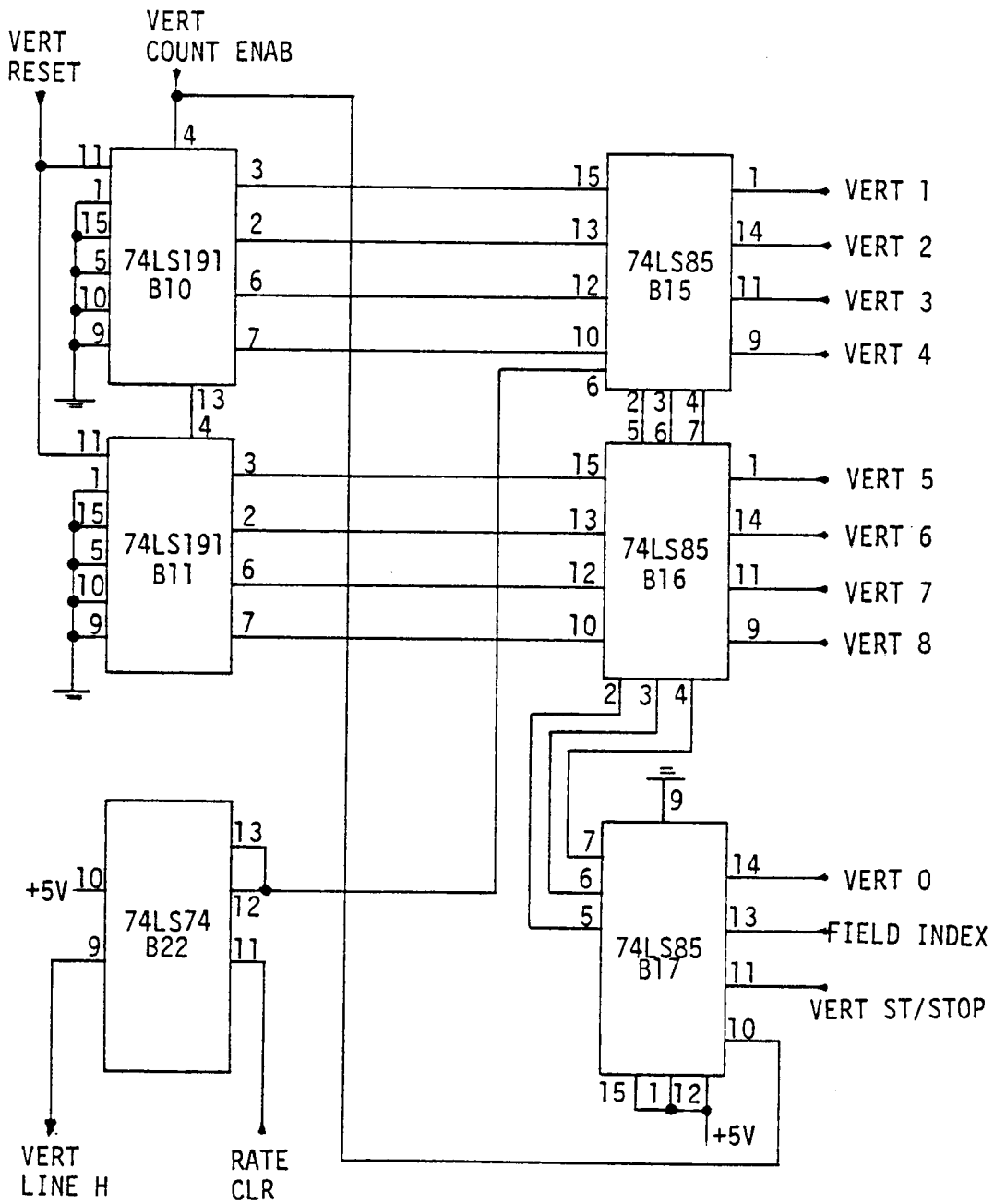


Figure 7.23. Horizontal sync pulse counters and comparators.

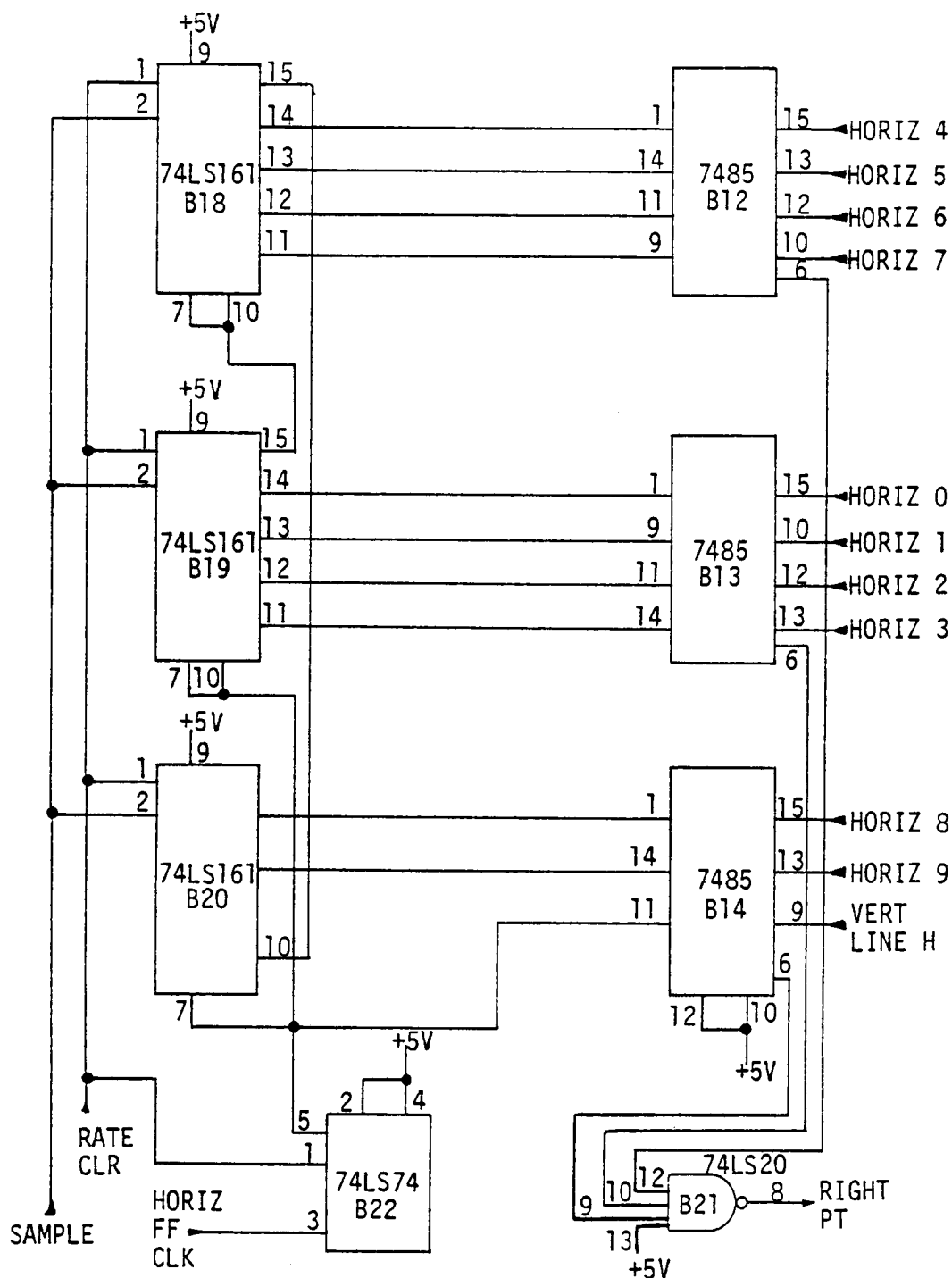


Figure 7.24. Horizontal point counters and comparators.

NTSC standard sync signal was chosen since it is the television industry standard and is already provided by most good closed-circuit video sources. This type of composite sync signal must be a part of the composite video waveform sent to the VDRC system or errors in storing sample points will occur.

7.3. Uses of the Pixel Location Circuit

The VDRC system provides the processor with a large degree of flexibility with the provision of the PLC circuit. Only desired sample points from anywhere in the picture are stored and used by the processor to generate a new transformation curve. This feature could allow the processor to request a circle of points around a desired center to be used in generating a new transformation curve if so desired. Such a degree of flexibility in selecting points combined with the various sample rates available allow a large degree of freedom in obtaining sampled data for use in performing various enhancement algorithms.

CHAPTER 8

RESULTS AND CONCLUSIONS

The major objective of the VDRC system is to be able to digitize, transform, and reconstruct video waveforms from two sources simultaneously with no degradation in resolution or sharpness. If the transformation process is set to produce a linear mapping, i.e., every sample point is mapped to its own value by the system, the reconstructed picture should be a duplicate of the original input picture. A comparison of the original image and the reconstructed image from the VDRC system could then be used to determine the quality of the system output and show any degradation due to the image being sampled and reconstructed by the system.

Figure 8.1 displays several waveform patterns produced by a Tektronix 1470 NTSC Color Sync and Test Signal Generator before and after processing by the VDRC system. Figures 8.1(a) through 8.1(d) are original waveforms produced by connecting the generator directly to the display monitor. The waveforms shown in Figures 8.1(e) through 8.1(h) are the corresponding images, respectively, processed by the system with a linear mapping at a sample rate of 464 points per horizontal line. Processing at this rate is presented to show the quality of the system output signal if stereo processing is done using the fastest sample rate. These pictures reveal that the edge sharpness and grey scale resolution are not degraded by the system processing. Figures 8.1(i) through 8.1(l) display the generator waveform pattern called "multiburst" as originally produced by the generator and after system processing at the

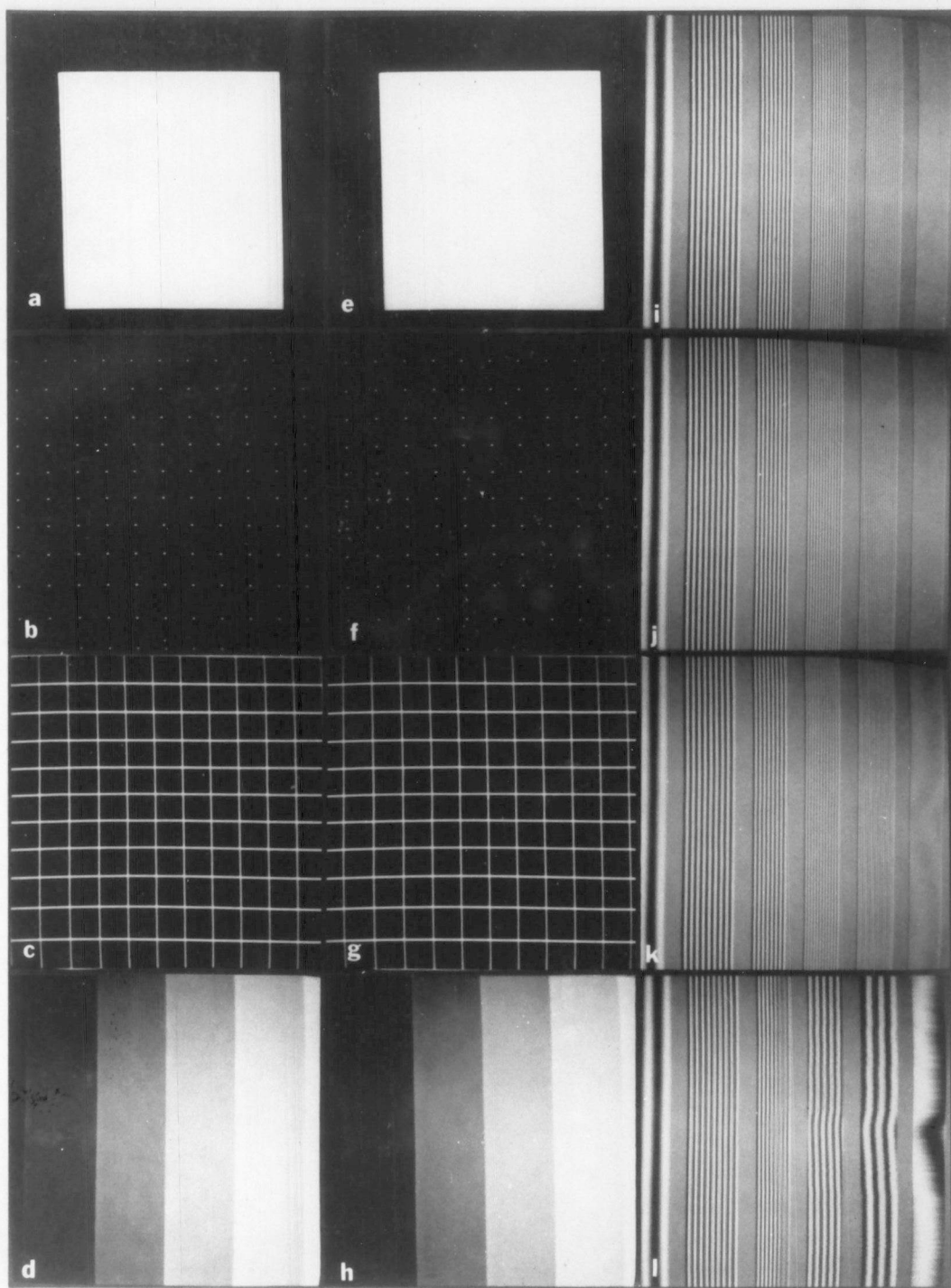


Figure 8.1. Waveform patterns before and after being transmitted through the VDRC system.

three fastest sample rates for a single video source. Figure 8.1(i) is the original image with Figure 8.1(j) being the output of the system at a sample rate of 928 points per horizontal line. Notice the clarity and definition of the vertical lines on the right side of the image are preserved. Figure 8.1(k) is the image sampled at 464 points per horizontal line. The definition of the vertical lines on the image's right side is lost while the left side is still intact. This result is caused by the use of a sample rate which is too slow to reproduce the frequency of the image's right side accurately, thus causing blurring of that portion of the image. Figure 8.1(l) is the output of the system when the generator waveform is sampled at a rate of 232 points per horizontal line. This picture further reveals the effects of blurring on the right side of the image where the vertical lines shown in the original image are totally lost. Blurring of the next four bands is due to the lower sample rate being unable to reproduce the frequency content of these bands accurately.

Figure 8.2 shows two live scenes processed by the system at four possible sample rates available in the system. Figure 8.2(a) is a picture of a girl's face sampled at a rate of 464 points per horizontal line. The sharpness of the edge detail around her hair and the smoothness of her face are preserved. Figure 8.2(b) is the same picture sampled at 232 points per horizontal line. Facial smoothness is preserved, but the sharpness around the edge of her face has some degradation. The detail in her eyes is also affected slightly. Figure 8.2(c) has a sample rate of 116 points per horizontal line and shows a definite loss of sharpness and smoothness in the facial area and around the edge of her hair, but most of the details can still be visualized.



Figure 8.2. Live scenes processed by the VDRC system at four of the possible sample rates.

Figure 8.2(d) is the image at a sample rate of 58 points per horizontal line. Notice almost all discernible information is lost. Only large areas of the picture, such as the eyes and lips, are recognizable.

Figures 8.2(e) through 8.2(h) are slightly more complex pictures of a ship processed at the same sample rates as described for Figures 8.2(a) through 8.2(d). Notice the sharpness of detail in Figure 8.2(e), which is sampled at a rate of 464 points per horizontal line, on areas of the ship such as the antenna and the center bulkhead. Figure 8.2(f), sampled at a rate of 232 points per horizontal line, begins to degrade the sharpness around the ship's edges but retains sharpness in the remainder of the image. Figure 8.2(g), sampled at 116 points per horizontal line, loses almost all edge sharpness, especially in the background, but the scene can still be recognized as a ship. Figure 8.2(h) is the result of the image sampled at a rate of 58 points per horizontal line. As with this sample rate in the previous set of pictures, almost all definition and sharpness are lost. This scene is now difficult to visualize as a ship, even though the full grey scale resolution is maintained.

Several conclusions may be reached as a result of the experiments performed. The VDRC system has the capability of digitizing, transforming, and reconstructing video waveforms with no noticeable degradation in the resultant output picture for scenes sampled at either of the two fastest sample rates available. A slight loss in sharpness is encountered at the next sample rate of 232 points per horizontal line but in most applications would still be considered acceptable. Sampling at a rate of 116 points per horizontal line produces a scene

which loses a large amount of edge sharpness in the image but still retains the majority of the overall scene definition. A sample rate of 58 or 29 points per horizontal line results in losing a majority of the sharpness and definition in the image. These two slowest rates are probably best suited for use in obtaining sample data quickly from a large portion of the video information signal to be used in the algorithms of image enhancement and also to detect the presence of motion in the viewed scene.

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APPENDIXES

APPENDIX A [2]

VIDEO FUNDAMENTALS

The standard black and white television signal broadcast in the United States employs a 2:1 interlaced raster scan. The electron beam path (or raster) generated by such a scan consists of 525 horizontal lines which are divided into two scan fields of 262 1/2 lines each. These fields are referred to as the even and odd raster fields. Figure A.1 depicts the electron beam paths associated with each field and the transition paths between the fields. The dashed lines in this figure represent beam paths that produce no visible effects on the CRT, called flyback or retrace paths.

The signal required to produce the scan shown in Figure A.1 is referred to as the composite video signal. The term composite extends from the fact that the signal basically consists of three components: (1) picture information, (2) vertical synchronization information for flyback between the two interlaced fields, and (3) horizontal synchronization information for flyback or retrace between each of the 525 raster lines. (Without the information signal, the composite video signal is called the composite sync signal.) The details of the composite video signal are shown in Figures A.2 and A.3 and are discussed below.

The information or picture portion of the composite video signal has a usable bandwidth of about 4 MHz and utilizes approximately 75% of the total signal amplitude. This is 1V of a standard 1.4V peak to peak camera output. A typical video burst, one line of picture information between two consecutive horizontal sync pulses, is shown in Figure A.2(a).

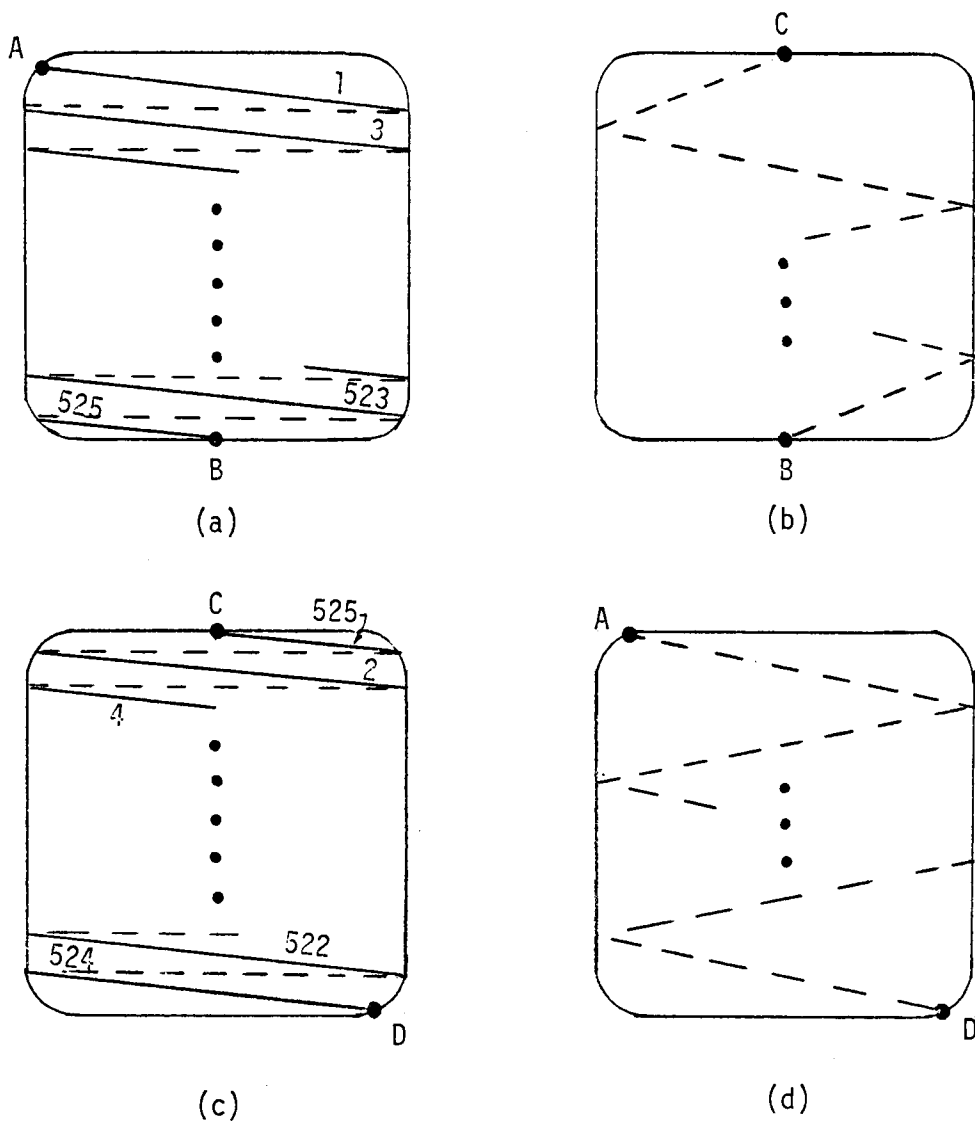


Figure A.1. The electron beam path for a 2:1 interlaced scan: (a) odd field raster, (b) vertical flyback following the odd field, (c) even field raster, and (d) vertical flyback after the even scan field.

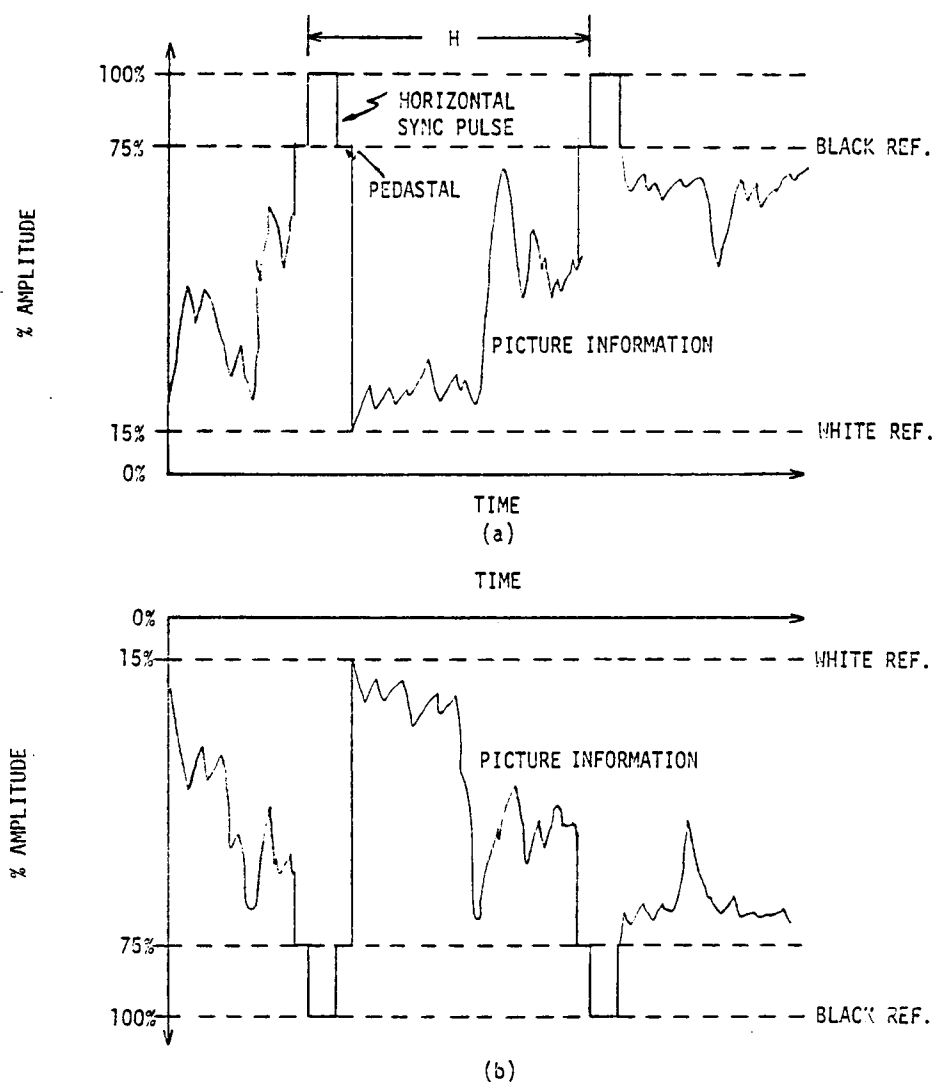


Figure A.2. Amplitude details of the information signal in a (a) positive and (b) negative composite video.

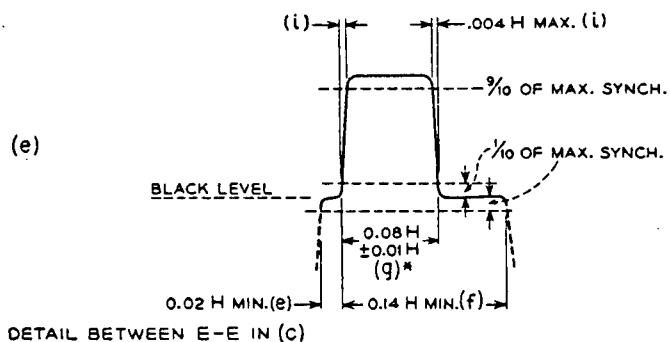
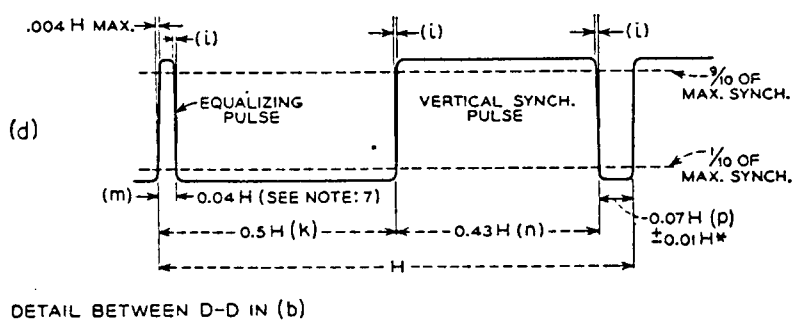
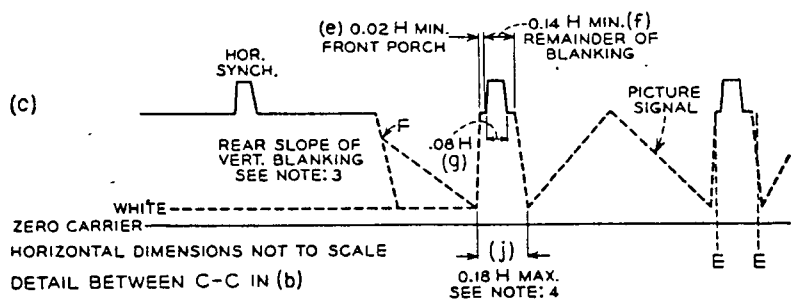


Figure A.3. (Continued)

This is referred to as a positive composite video. A negative composite video is depicted in Figure A.2(b) and is simply the inversion of the positive composite video of Figure A.2(a). Note that the black reference level (75% F.S.) is identical to the blanking level for the horizontal sync pulses. This inhibits the electron beam from affecting the CRT phosphorus during flyback or retrace.

If the information signal were a 4 MHz sine wave whose peak to peak amplitude variation was 75% of the total composite video amplitude, the number of alternating black and white segments produced on a single horizontal scan line would be 426 elements. For the entire 525 line raster, the theoretical number of picture elements would be 224,000. Because of the lines omitted during vertical retrace, only 150,000 elements appear on a television as usable information. This is roughly 25% of the definition obtainable with 35 mm movie film, which may contain as many as 600,000 elements [7].

A single image or picture frame consists of two fields that require 0.033 secs. to be traced into the CRT phosphorus. At the end of every field, the electron beam must be positioned at the top of the raster to properly begin the subsequent field. To facilitate this electron beam placement, commercial television receivers utilize a 60 Hz sawtooth oscillator which is frequency locked by vertical sync pulses contained in the composite video signal. The video signal conditions surrounding these sync pulses are shown in Figure A.3(a) and A.3(b). The vertical sync of field interval V between any two consecutive vertical sync pulses is

$$V = \frac{1}{60} \text{ sec.} = 16.67 \text{ msec.} \quad (\text{A.1})$$

Of this interval, 0.0114V is allowed for the vertical sync pulse itself. Specifications for the shape and duration of the pulse are shown in Figure A.3(d).

To produce the 262 1/2 horizontal scan lines required during each field interval, a 15.75 KHz oscillator, similar to the one employed to maintain vertical synchronization, is frequency locked to horizontal sync pulses in the composite video. The horizontal sync period H is relatively short in comparison to the vertical field interval V:

$$H = \frac{1}{15.75 \times 10^3} \text{ sec.} = 63.5 \mu\text{sec.} \quad (\text{A.2})$$

Approximately 8% of this interval (0.08H) is reserved for the horizontal synchronizing pulse; the remaining 0.92 H contains the video burst. Details of the horizontal sync pulse are shown in Figure A.3(e).

The spacing of the horizontal and vertical sync pulses within the composite video signal is crucial to the correct generation of the 2:1 raster. The first field must end in the middle of a horizontal line interval. The proper phase relationships between the horizontal and vertical sync pulses for an NTSC standard sync signal are illustrated in Figures A.3(a) and A.3(b). Note that the vertical sync pulse is serrated 6 times at H/2 intervals to maintain horizontal synchronization during the vertical flyback interval. The equalizing pulses evident in Figure A.3(a) are included to prevent unequal integrated voltages at the end of successive fields that could cause a shift in the point of synchronization. The insertion of these pulses is related to the commercial procedure for isolating vertical sync from composite video. For a more detailed description of this process, consult the references noted at the end of this investigation [7,8].

APPENDIX B

VDRC SYSTEM BOARD LAYOUT

Four boards, three wire-wrap and one printed circuit, comprise the VDRC system. These boards are numbered Board 1 through Board 4 with Board 1 being the bottom board in the system. Figures B.1 through B.4 show the component positions on each board. Thus, any component location may be found by determining its number from the figures in the text and then locating this number on the board layout figures. Board 4 is the only printed circuit board in the system. Its solder side and component side layouts are shown in Figure B.5 and B.6, respectively. These figures are reduced to 65% of the original image.

Board 1 contains the PLC circuit and the interface circuit to the processor. Board 2 contains the master clock, one side of the DTMM, and the VPPC circuit. The other side of the DTMM and the control circuit are contained on Board 3. Finally, the VPC, VSC, VRC, and ESGC circuits of the system are located on Board 4.

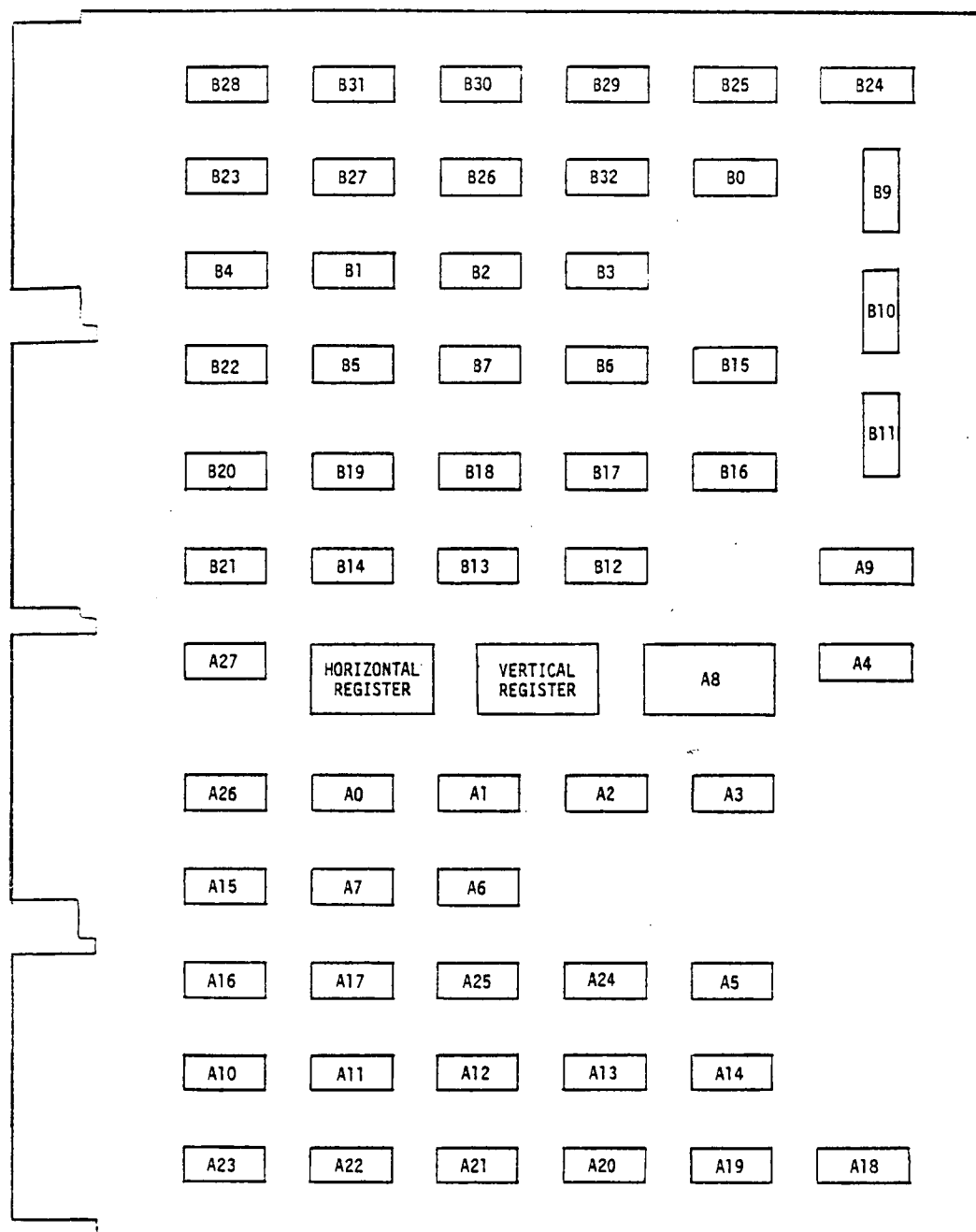


Figure B.1. Component layout of Board 1.

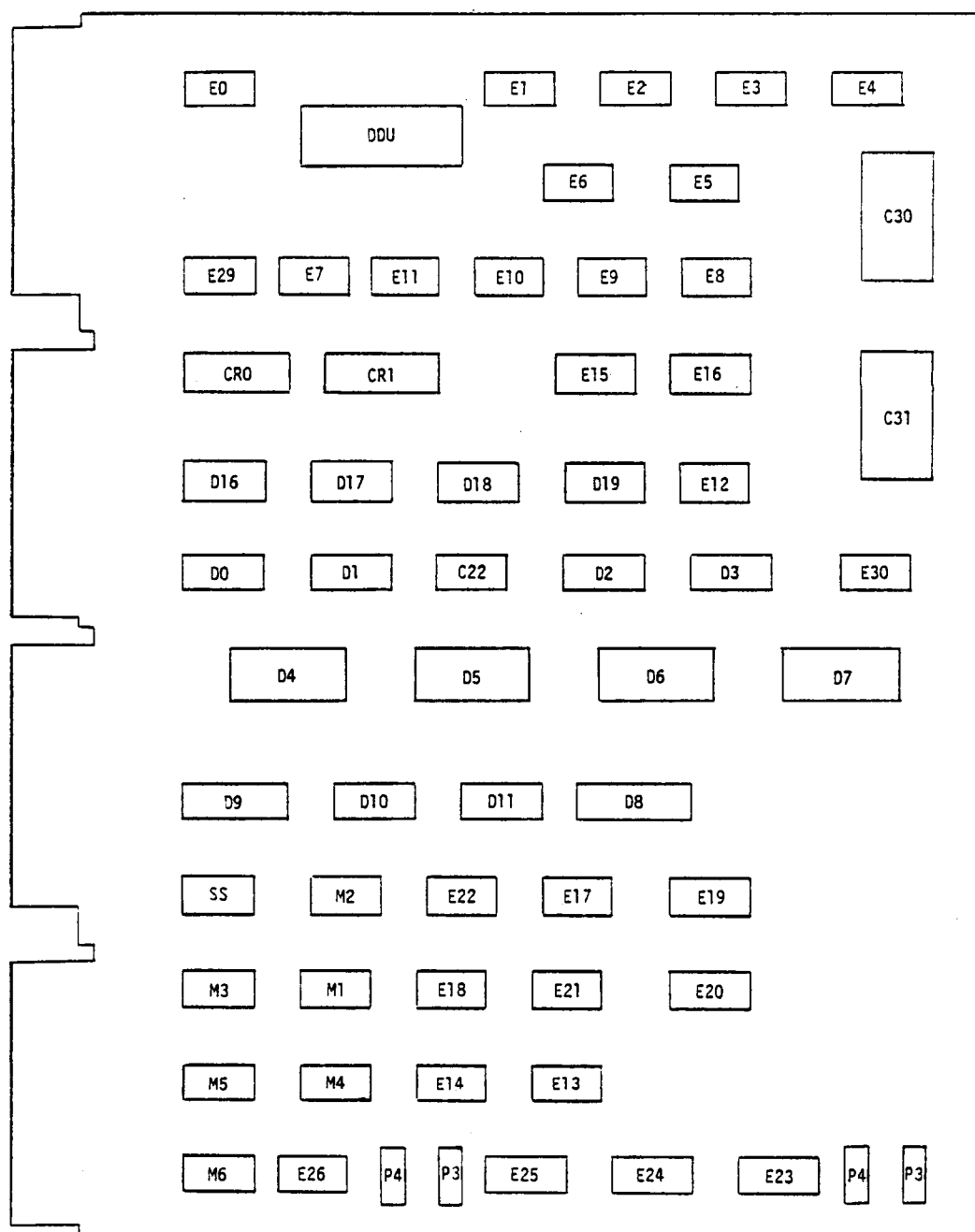


Figure B.2. Component layout of Board 2.

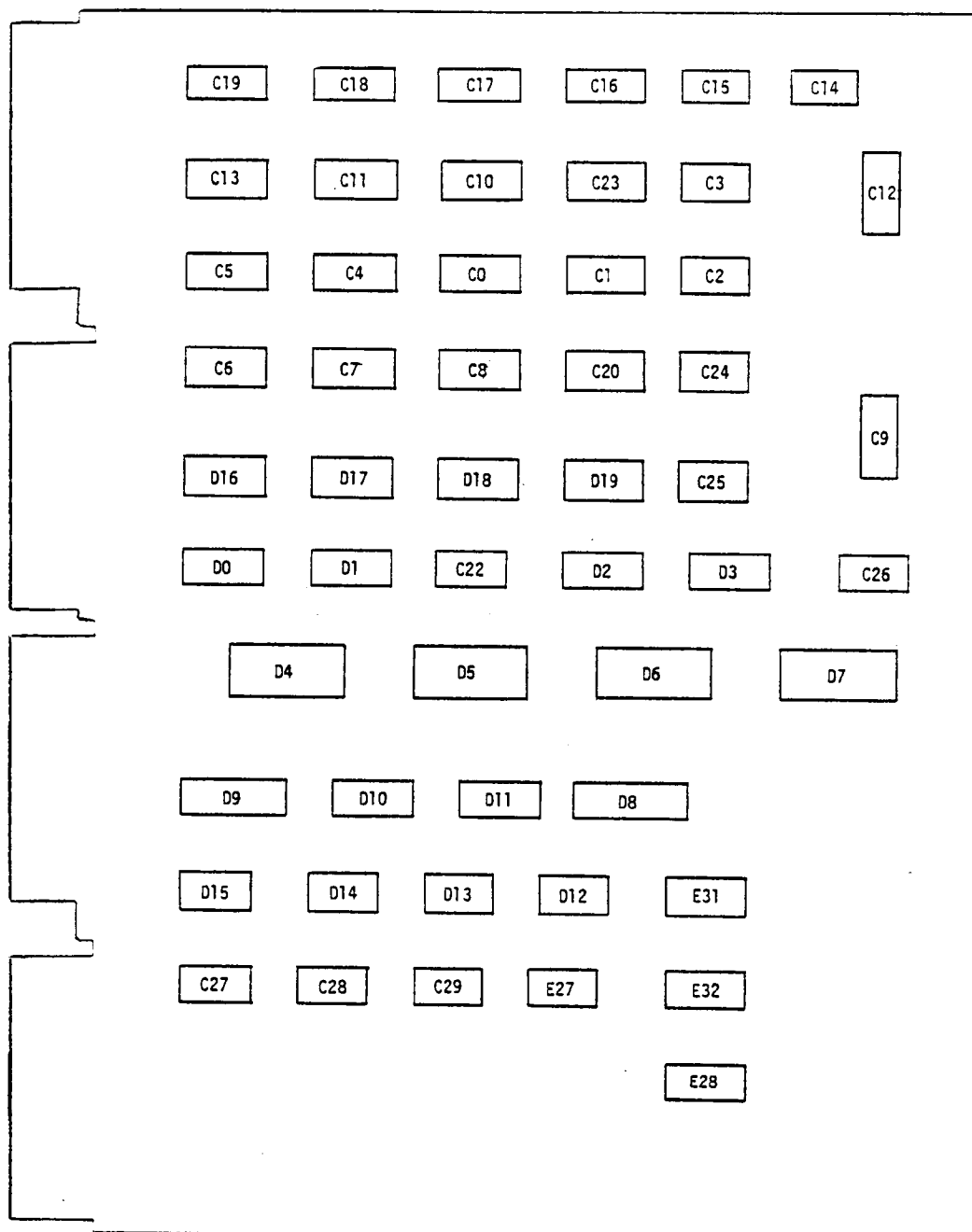


Figure B.3. Component layout of Board 3.

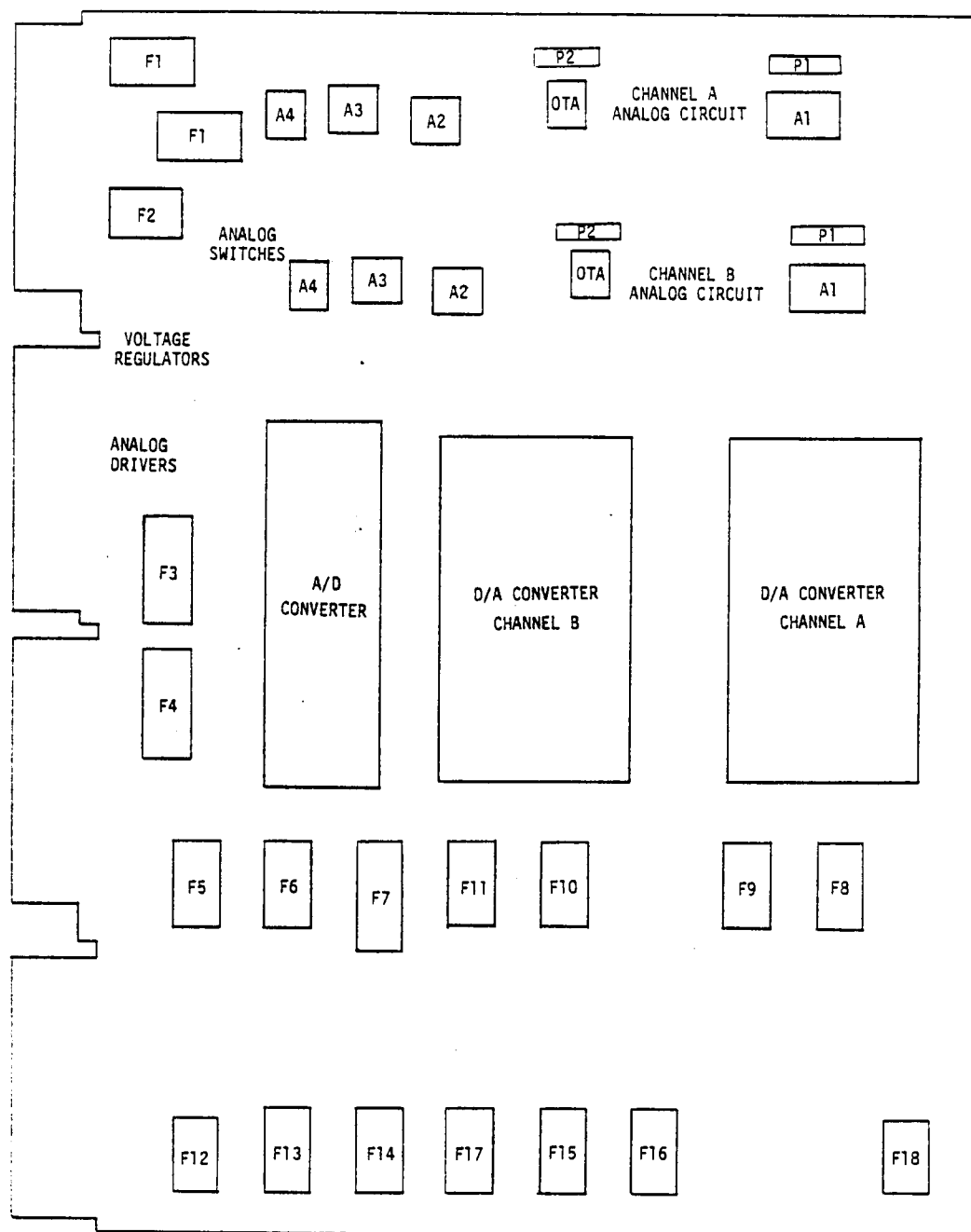


Figure B.4. Component layout of Board 4.

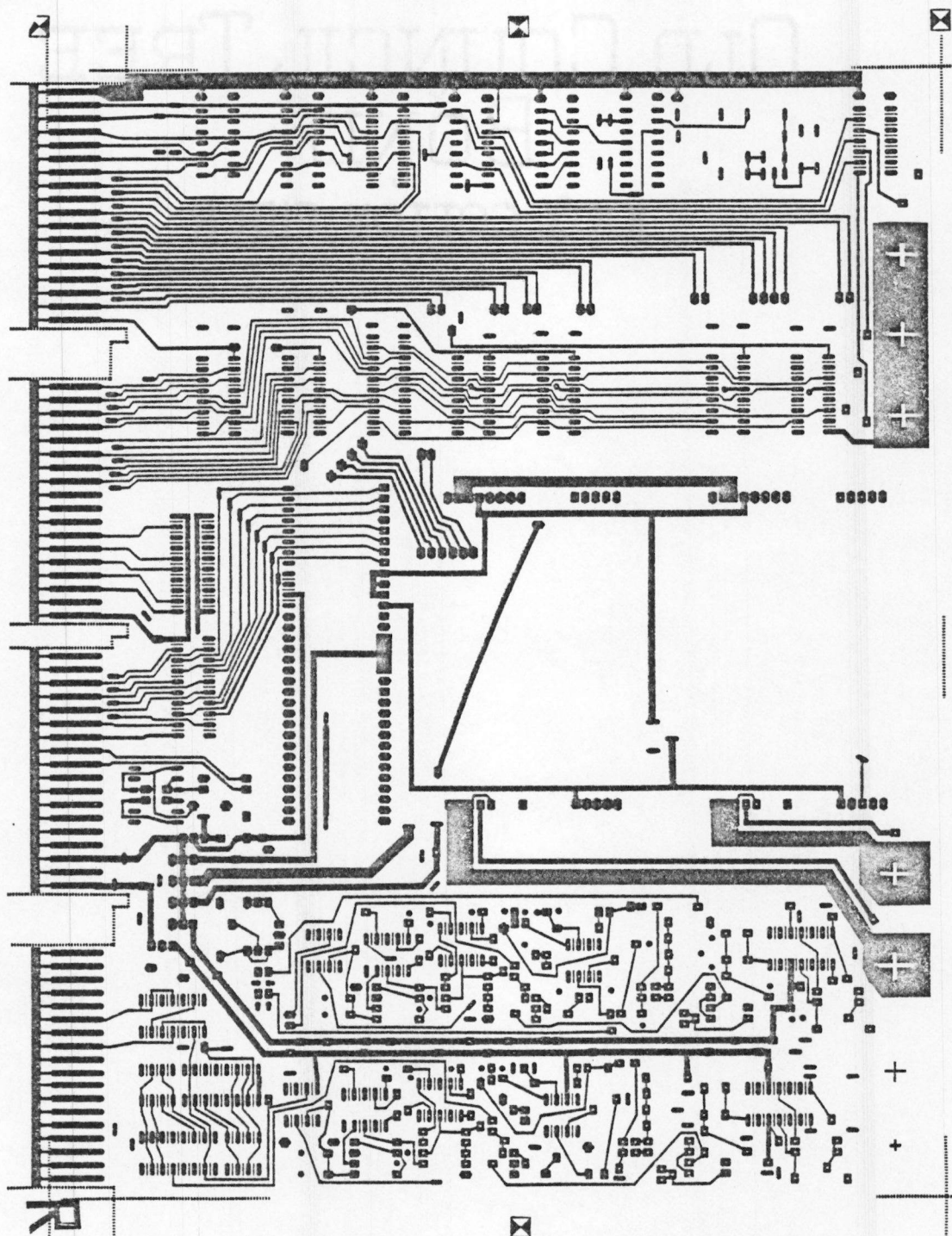


Figure B.5. Solder side of the printed circuit layout of Board 4.

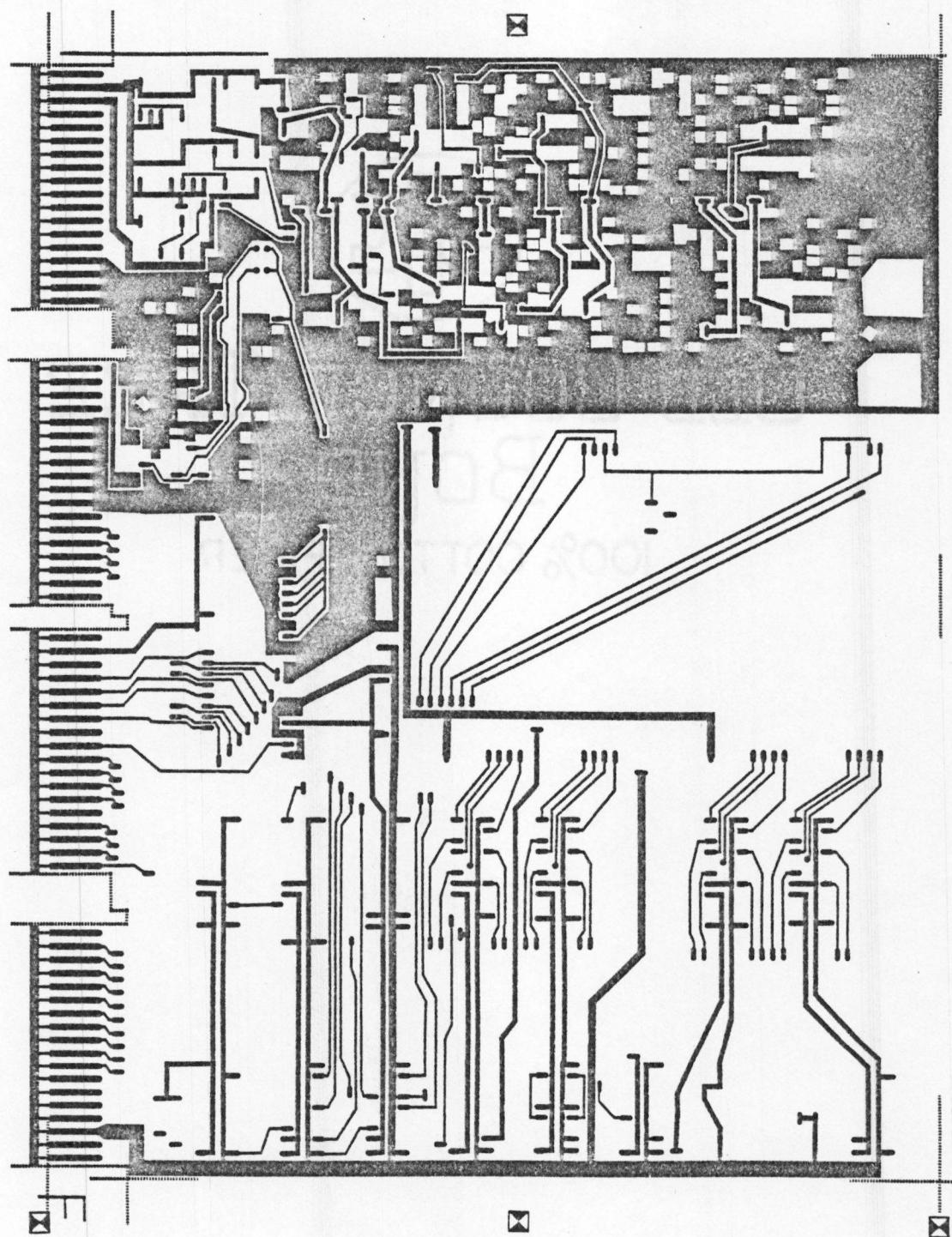


Figure B.6. Component side of the printed circuit layout of Board 4.

VITA

Robert Eugene Crossley was born on May 17, 1953 in Birmingham, Alabama. He attended West Haven and Bearden Elementary before graduating from West High in Knoxville, Tennessee in June 1971. The following September, he enrolled at The University of Tennessee, Knoxville, and received a Bachelor of Science degree in Electrical Engineering in June 1977. During this time, he also served as a Co-operative engineering student with the Department of Energy in Oak Ridge, Tennessee. The author was employed by the Tennessee Valley Authority in the Instrumentation and Control Division from June 1977 to September 1977. Upon receiving a graduate research assistantship, he began study towards a Master's degree in Electrical Engineering, which was awarded in August 1979.

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