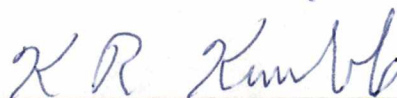


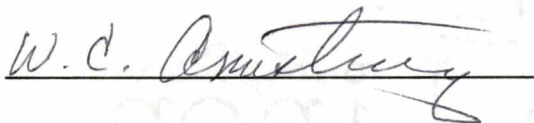
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AN EVALUATION OF A REAL-TIME DATA ACQUISITION
AND CONTROL LOCAL AREA NETWORK

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

David L. Rollins

May 1989

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ABSTRACT

A baseline timing database and description of a representative data acquisition and control network was developed. This database provides the information needed to make decisions about the network and a way to evaluate future modifications to the network. The data acquisition systems are described and their response time characteristics are presented. Also presented are the recommendations for improving the performance of the network.

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LIST OF ABBREVIATIONS

DDAS	Digital Data Acquisition System
DEC	Digital Equipment Corporation
DMACS	Digital Multiplexer and Control System
DPC	Data Production System
DPS	Digital Pressure System
DNA	Digital Network Architecture
ESP	Electronically Scanned Pressure
EUD	Engineering Unit Display
FAMROS	Force and Moment Readout System
ISO	International Standard Organization
OSI	Open Systems Interconnect

INTRODUCTION

The ever increasing cost of data acquisition requires that data acquisition and test article control functions be efficient. It is essential that time spent in these functions be understood and that the network and associated nodes be documented. This thesis describes an effort to show improved productivity in a representative test unit by the installation of a new Facility Computer and communications network. The development of a baseline timing database and network description will enable personnel to make more informed decisions about improvements and modernizations to the network and associated nodes, as well as providing a diagnostic aid in pinpointing trouble areas on the network.

Chapter I describes the current configuration of the network along with the networking standards upon which it is based. Two subsets of timing data are presented and evaluated in Chapters II and III. Chapter II presents the individual data system response times which show the speed and consistency in processing requests for data. Chapter III presents the concept of a "data point" and decomposes this data point in terms of the time taken for the component parts of the point. Chapter IV summarizes the results of the baseline database study and presents recommendations.

CHAPTER I

CURRENT NETWORK CONFIGURATION

DECnet, Digital Equipment Corporation's collection of software and hardware, and Ethernet [6]¹, jointly developed by Digital Equipment Corporation, Xerox Corporation, and Intel Corporation, make up the existing, or representative, local area network that support testing activities. This family of networking products is based upon the Digital Network Architecture (DNA) [11]. DNA was originally developed for point-to-point communications over private and common carrier lines, but has been improved and extended to support local area communications [1]. DNA is modeled closely after the layered concept of the International Standard Organization's (ISO) Open Systems Interconnect model [7]. A comparison of the network architecture layers is shown in Figure 1.

1. The Local Area Network

The test unit local area network supports such functions as model attitude control, data acquisition and reduction of model and environmental data by connection of several computers ranging in size from a Digital Equipment VAX 8600 to several Digital Equipment PDP11 computers. Standard Ethernet baseband coaxial cable is used as the transmission medium. The computers on the network are connected to the

¹Numbers in brackets refer to similarly numbered references in the List of References.

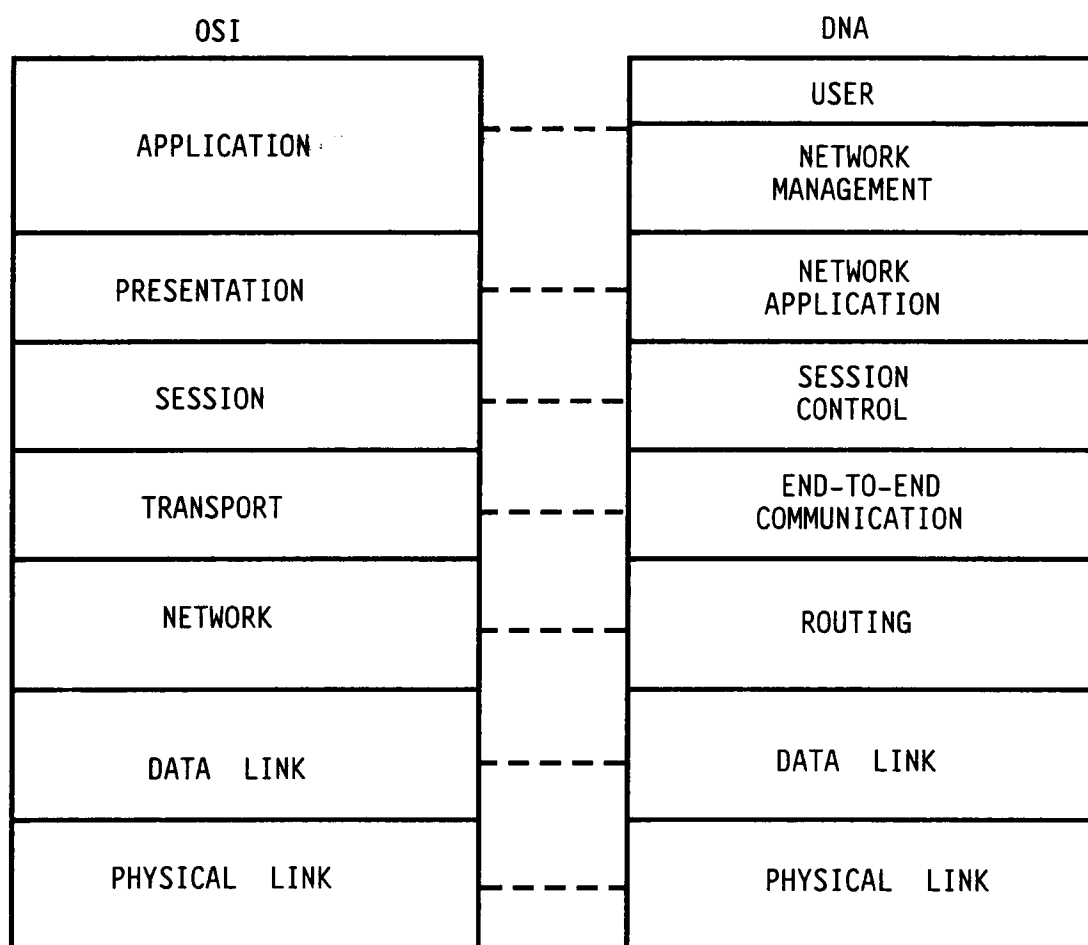


Figure 1. OSI-DNA Network Architecture Layer Comparison

coaxial cable via standard Digital Equipment transceivers [3]. The basic network configuration is shown in Figure 2.

1.1 Digital Multiplexer and Control System

The first data acquisition computer system discussed is the Digital Multiplexer and Control System (DMACS). The DMACS computer system is composed of a Digital Equipment PDP 11/73 computer with two megabytes of main memory, a 31 megabyte RD52 disk, a 0.8 megabyte RX50 Dual Floppy Disk Drive, and a 60 megabyte TK25 cartridge tape drive. Version 3.0 of the RSX11M-Plus operating system and Version 3.0 of DECnet communication software is used. The DMACS hardware block diagram is shown in Figure 3. The system is dedicated to acquisition of test unit environmental data, model attitude data and output/monitoring of model control signals. A single board computer, a Digital Equipment KXT11, operates as a peripheral processor to the PDP 11/73, providing the PDP 11/73 with an interface to the digital multiplexer hardware. The digital multiplexer enables the KXT11 to acquire data from ninety-six 24-bit digital inputs and sixteen 16-bit analog inputs, and enables it to control the output to 16 digital-to-analog converters and 6 on-off controllers. Upon request from the Facility Computer, the DMACS provides data and responds to control commands. The digital data provided by the DMACS is used by the Facility Computer to calculate the test unit environmental conditions and the test article attitude. The DMACS is attached to the Ethernet cable through a DEQNA Ethernet controller card to a DELNI local network interconnect to the H4000 Ethernet transceiver.

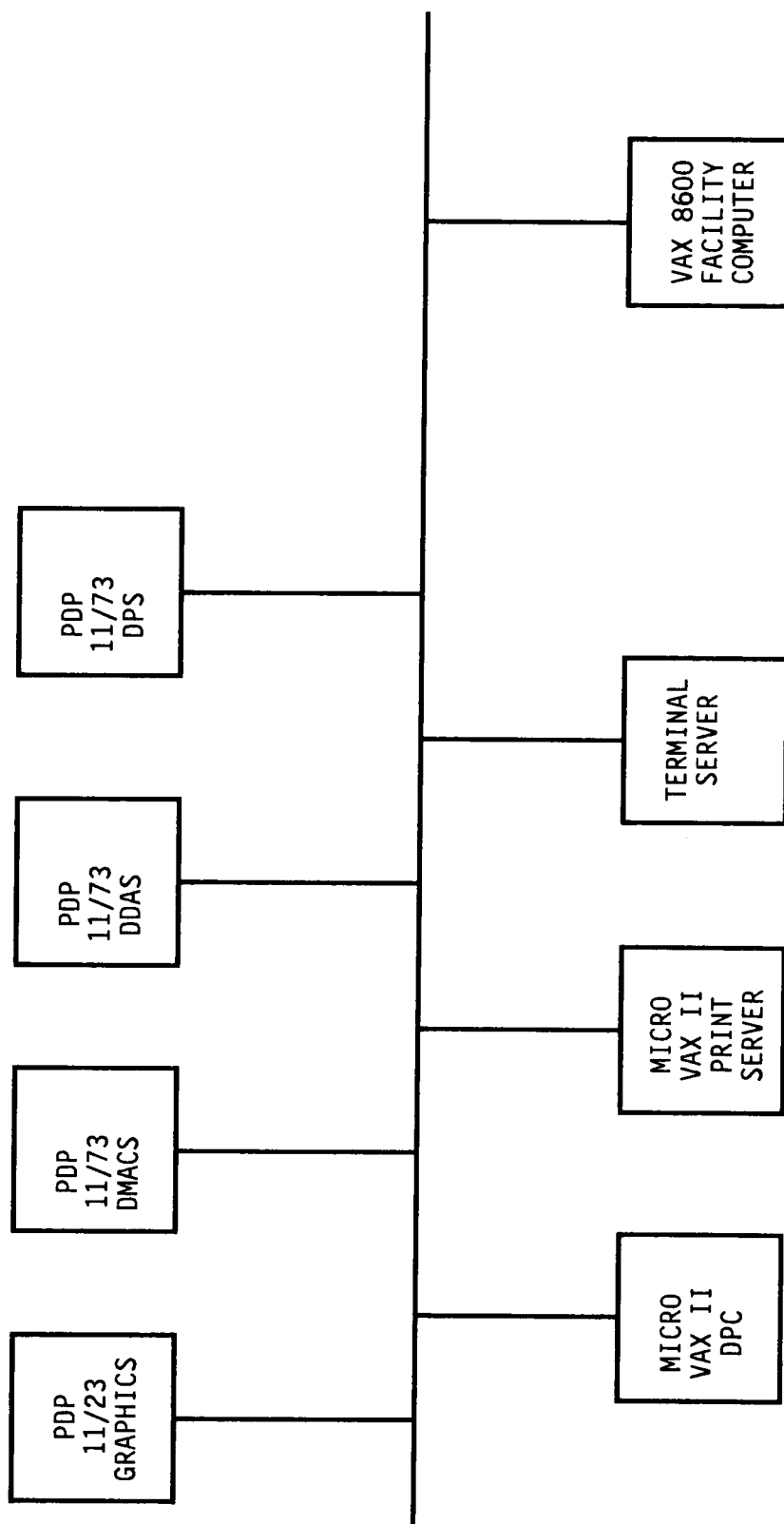


Figure 2. Basic Network Configuration

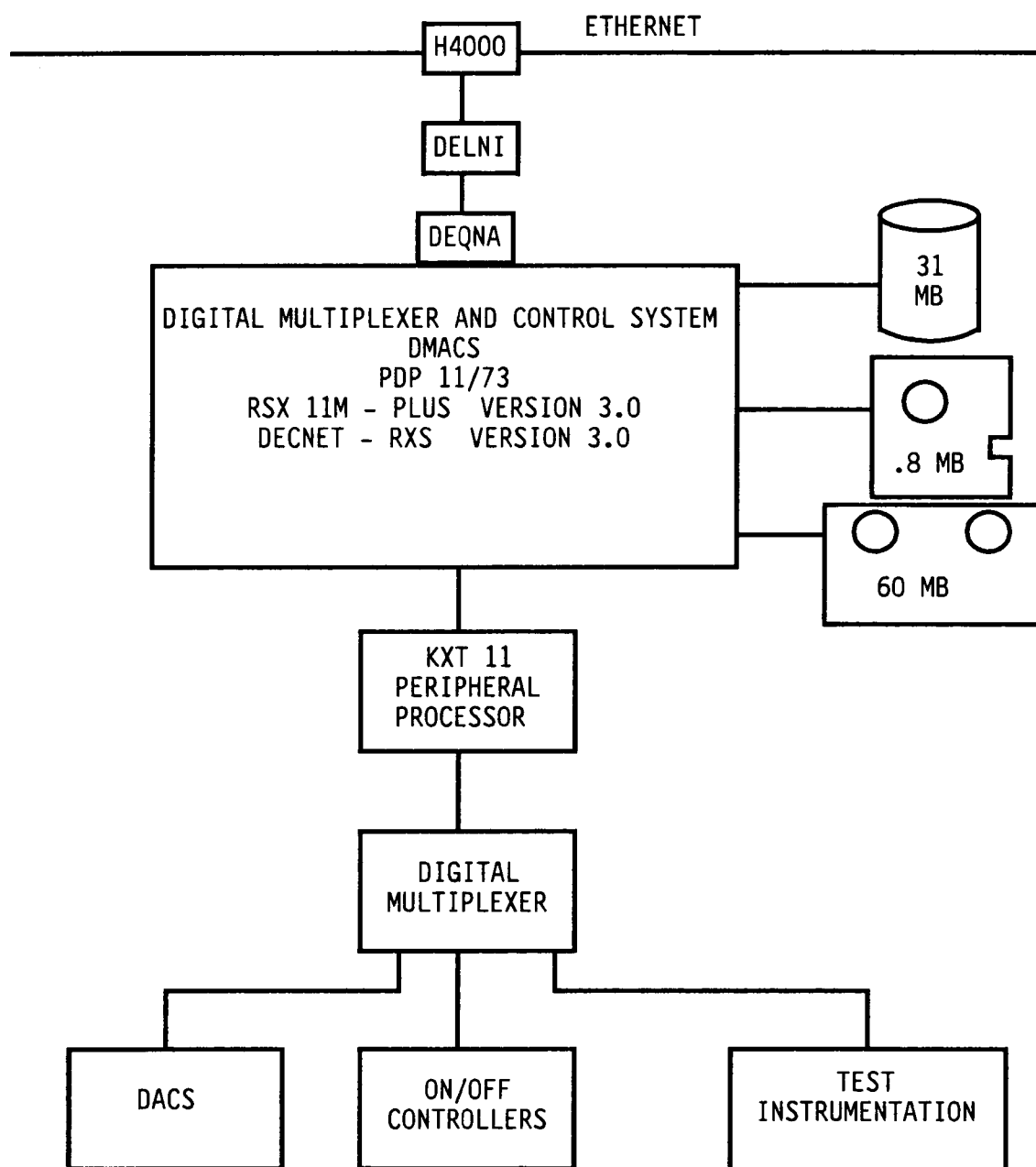


Figure 3. Digital Multiplexer and Control System Block Diagram

1.2 Digital Data Acquisition System

The next data acquisition system on the network is called the Digital Data Acquisition System (DDAS). A Digital Equipment PDP 11/73 computer with 2.5 megabytes of main memory, two 352-megabyte disk drives, two 10-megabyte disk drives, and a 40-megabyte tape system make up the data acquisition system. The system runs Version 3.0 of the RSX11M-Plus operating system and Version 3.0 of Digital's DECnet communication software. The DDAS hardware configuration is shown in Figure 4. The system is used to acquire steady state and transient data from a variety of devices including strain gage balances, thermocouples, and pressure transducers. The DDAS has three subsystems of data. It has an analog subsystem consisting of 240 programmable gain amplifiers, 48 simultaneous sample-and-hold amplifiers, and 104 channels for high level inputs (10-volt full scale). A Force and Moment Readout Subsystem (FAMROS) has 40 channels for the acquisition of strain gage data. Thirty-two 16-bit channels of digital data are available through the digital subsystem. Digital filtering of the data inputs is accomplished in an array processor attached to the DDAS. Forces and moments exerted on the test article are calculated on the Facility Computer using the data obtained from the DDAS. The DDAS is connected to the Ethernet cable through a DEQNA Ethernet controller card to a DELNI local network interconnect to the H4000 Ethernet transceiver.

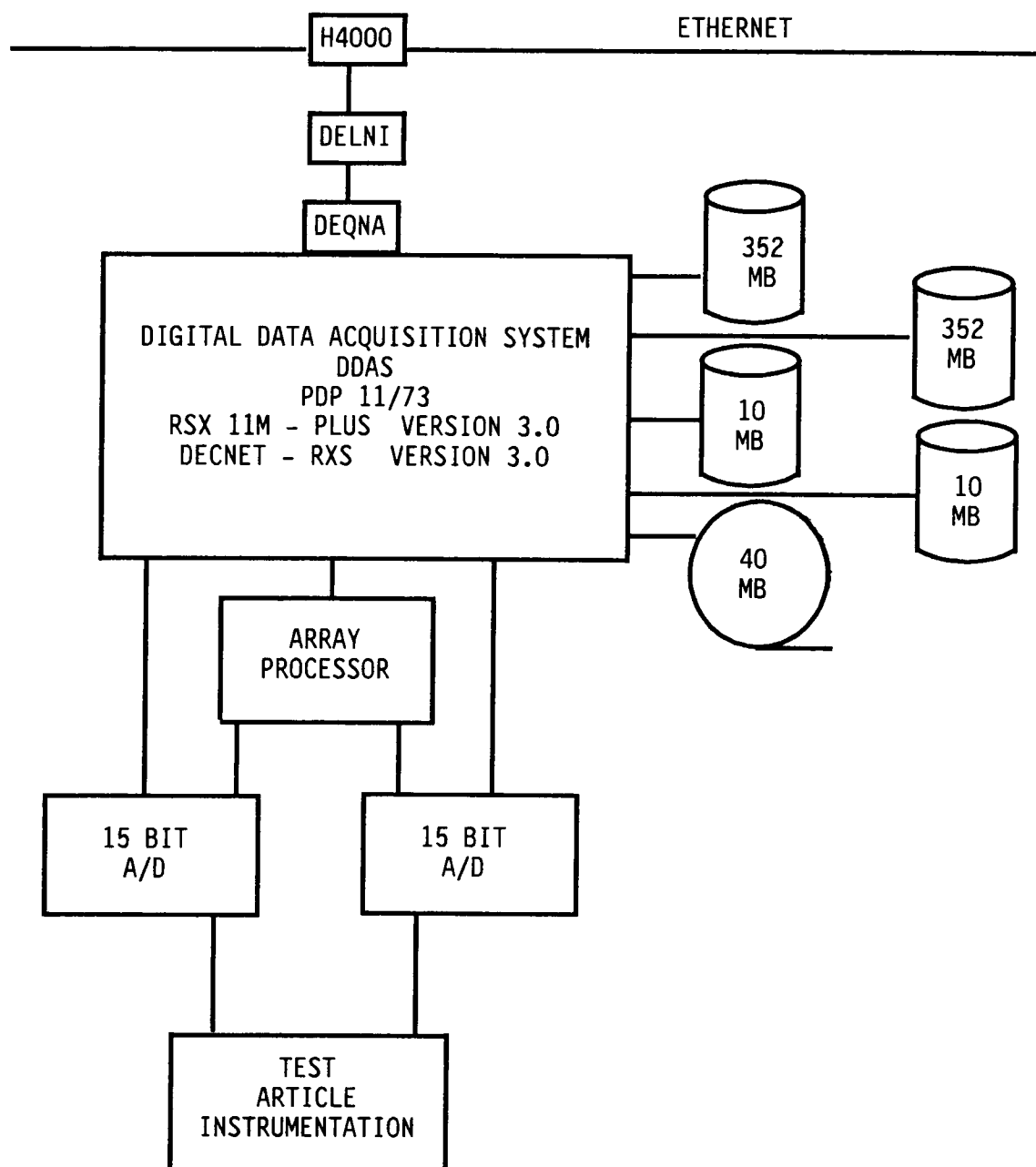


Figure 4. Digital Data Acquisition System Block Diagram

1.3 Digital Pressure System

The data acquisition system dedicated to acquisition of the majority of pressure data in the test unit is the Digital Pressure System (DPS). The DPS is a Digital Equipment PDP 11/73 computer with one megabyte of main memory and two 352-megabyte disk drives. It executes Version 3.0 of DEC's RSX11M-Plus operating system and Version 3.0 of DEC's DECnet communication software. Figure 5 illustrates the DPS hardware. There are three data subsystems associated with the DPS. Thirty channels of 16-bit digital data are available through the digital subsystem. The pressure subsystem provides 256 channels of digitally filtered pressure data. The Electronically Scanned Pressure (ESP) subsystem has the ability to scan sixty-four 48-port pressure modules for a total of 3072 pressure inputs. The Facility Computer uses the DPS data to calculate pressure parameters associated with the test article. Connection to the Ethernet cable is the same as the DDAS connection using the DEQNA, DELNI, and H4000 hardware.

1.4 Facility Computer

A Digital Equipment VAX 8600 computer is the controlling processor on the network. It is a standard Model 8600 configuration with options added to increase flexibility and productivity. Digital Equipment's operating system software, VMS Version 4.6, and communication software, DECnet-VAX Version 4.6, is used on the VAX 8600. The system includes sixteen megabytes of main memory. An HSC50 intelligent mass storage server is attached to the VAX 8600 to coordinate access to the disk and

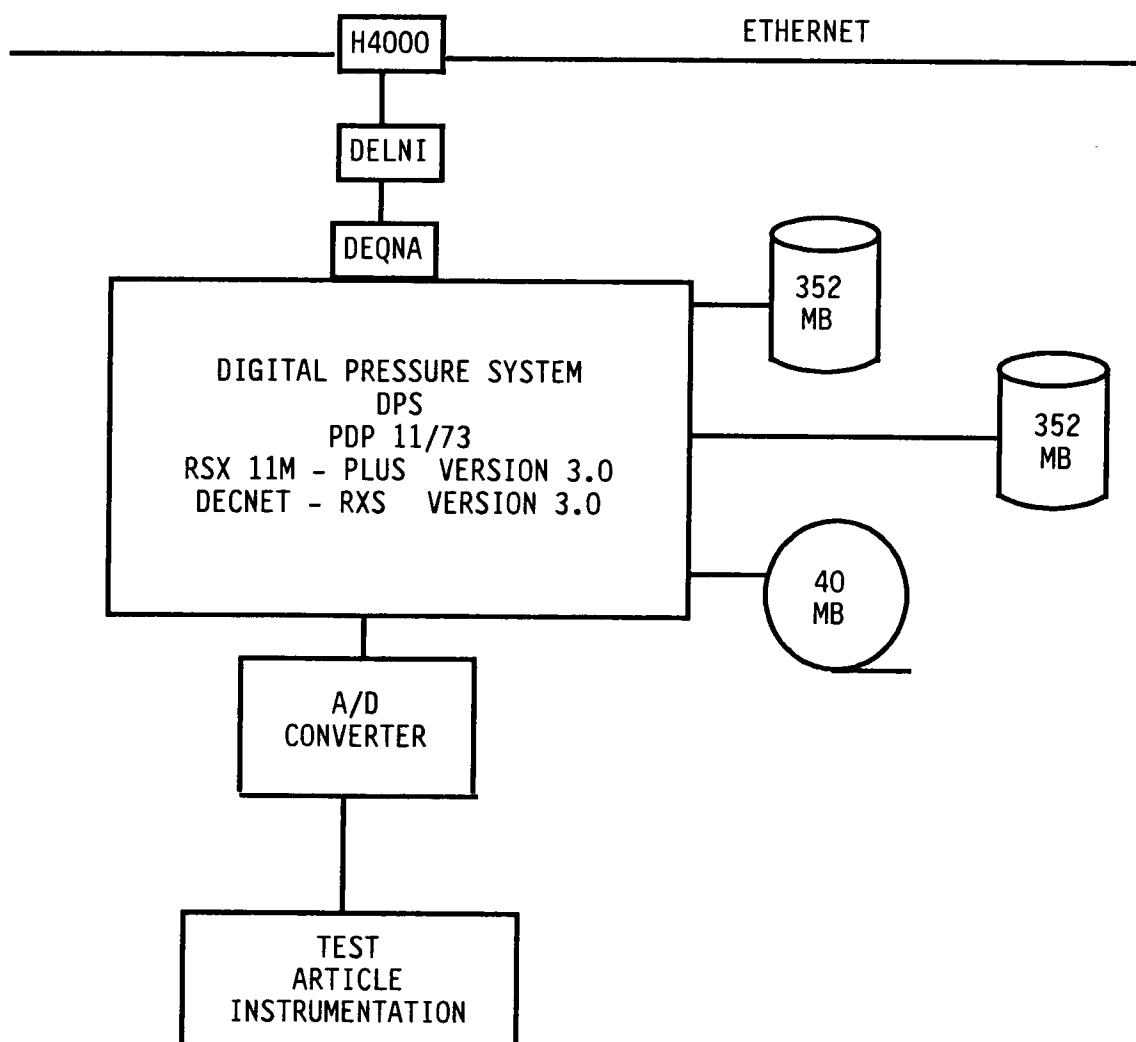


Figure 5. Digital Pressure System Block Diagram

tape drives. The HSC50 has access to one TA78 and one TU78 magnetic tape unit for backups and long term data storage. Six RA81 disk drives are available to the HSC50 for a total of 2736 megabytes of high speed disk storage. It is connected to the Ethernet cable from the VAX uni-bus backplane, through the DEUNA intelligent communications controller to the H4000 Ethernet transceiver. A hardware block diagram of the facility computer is shown in Figure 6. Coordination of the overall data acquisition and control process is accomplished on this processor. User software on the Facility Computer sends commands and requests to the data acquisition systems on the network and, in reply, receives applicable data buffers from these systems. The data acquired are used for automatic model attitude positioning, test article hazard monitoring, test unit environmental condition monitoring, as well as the calculation of discrete steady state test article performance parameters.

1.5 Data Production Center

The human interface to the data acquisition and control process is through a Digital Equipment MicroVAX II computer called the Data Production Center (DPC). Version 4.4 of MicroVMS is used as the operating system along with the network communications software, DECnet-VAX Version 4.4. A diagram of the DPC hardware is shown in Figure 7. The MicroVAX II is equipped with a single RD53 71-megabyte disk system and a TK50 95-megabyte tape system. The main function of the DPC is supervisory control of the data acquisition and control process. Complete control of the process is accomplished through human

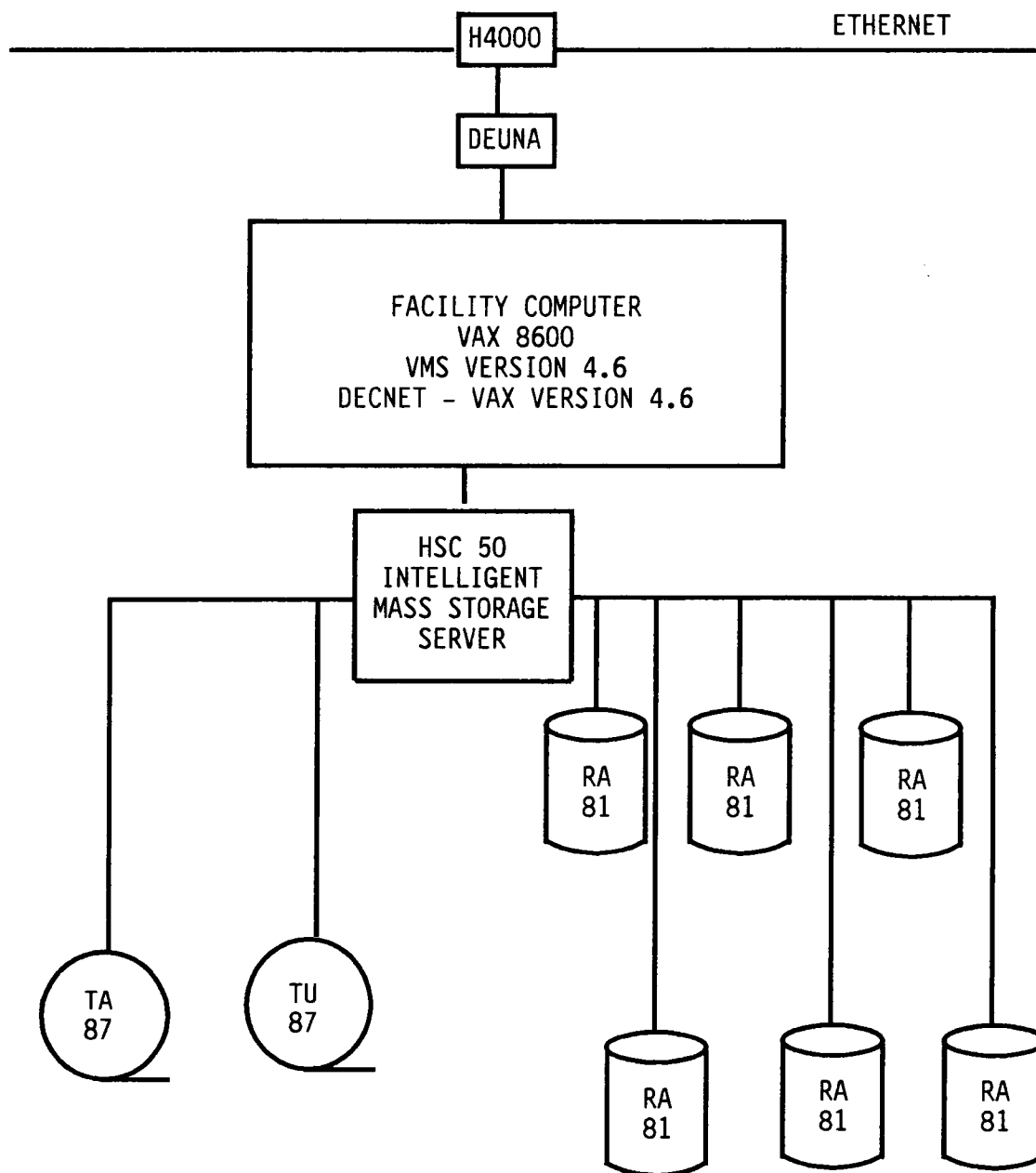


Figure 6. Facility Computer Block Diagram

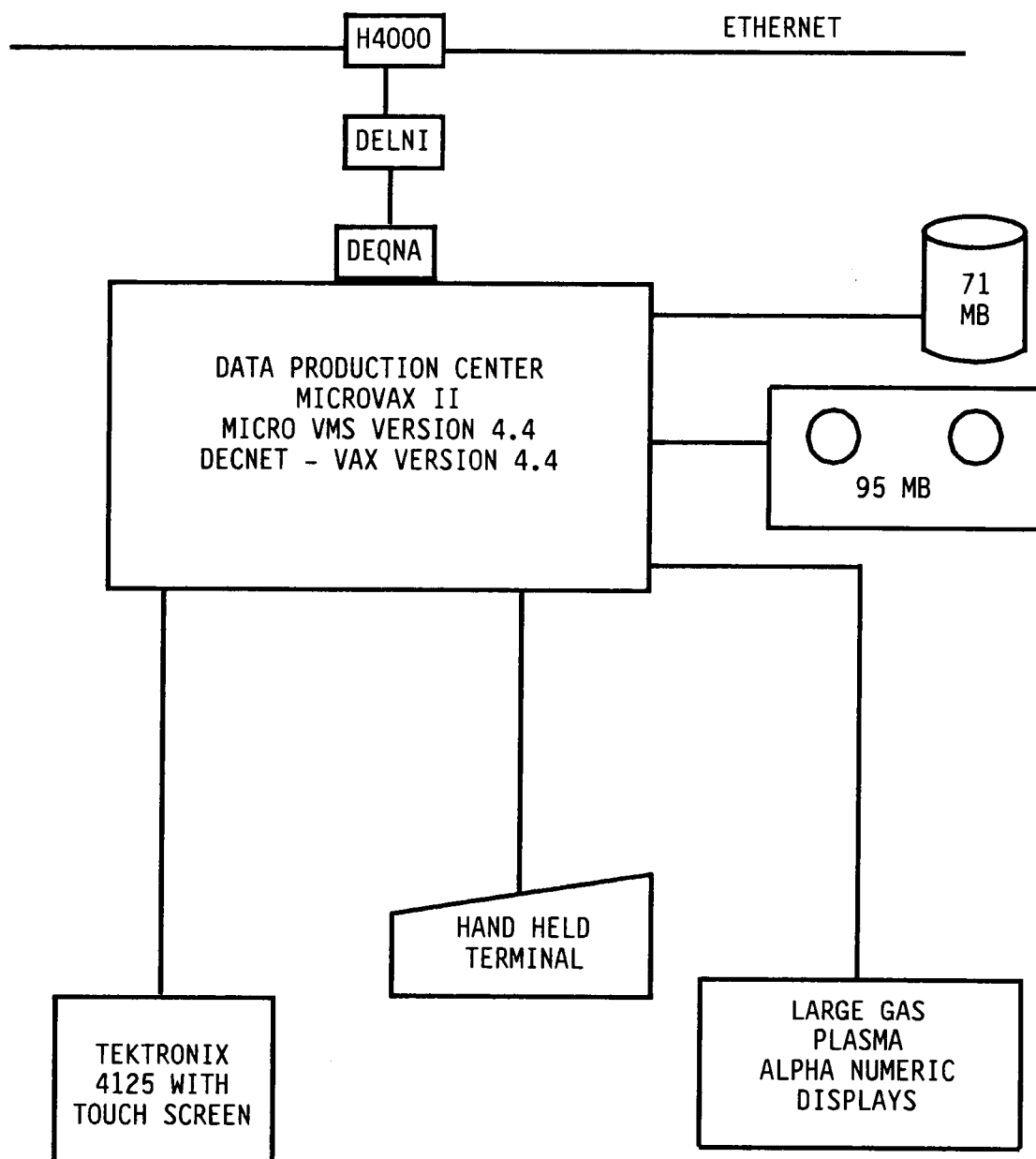


Figure 7. Data Production Center Block Diagram

inputs to the DPC. Inputs are made using menu driven software on a Tektronix 4125 video terminal equipped with touch screen control. The data acquisition and control process is initiated by input to a hand held terminal device attached directly to the DPC computer. Upon an input from the hand held terminal, a command packet is sent to the Facility Computer describing the type of function that is to be accomplished. Each input to the touch screen or the hand held terminal is echoed to the user as an audio output using Digital Equipment's DECTALK products. Another function of the DPC is to control Engineering Unit Display (EUD) outputs. Displays are supported on video terminals as well as two large gas plasma alphanumeric displays. Data are continually collected by the Facility Computer, reduced, and sent to the DPC for update of these displays. Message management is the other basic function of the DPC. All information and error messages encountered on the Facility Computer during the data acquisition and control process are packaged and sent to the DPC for display. These messages are also logged to the disk for future viewing. The DPC is connected to the Ethernet cable via a DEQNA Q-BUS control card through a DELNI local network interconnect to an H4000 Ethernet transceiver.

1.6 Other Network Devices

Three other devices are attached to the Ethernet which perform functions outside the area of data acquisition and control. A Digital Equipment MicroVAX II with a QMS Lasergraphics printer is used as the network print server. All on-line hard copy output is queued to this

system for printing. A Digital Equipment communication server is located in the test unit Control Room to allow terminals in the control room to access the data acquisition computers. A Digital Equipment PDP 11/23 computer is used to drive two Tektronix Model 4109 graphics displays.

CHAPTER II

INDIVIDUAL TIMING STUDY

It is very important to know the response times of the data acquisition systems for evaluations of changes to the data systems and network hardware and software, as well as for the development of new, time-critical, control algorithms. The individual timing study was accomplished by sending a series of data requests and recording the response time of the data system for each request. The author devised this test to simulate the response conditions of data acquisition and control functions during actual testing procedures.

1. Facility Time Code Generator/Reader

A Facility Time Code Reader is used to record times of events occurring during the data acquisition cycle. The time code reader decodes an incoming serial modulated time code generated by an area-wide time code generator. The time code reader is attached to the Facility Computer and queried via VMS QIO system service calls. This timing mechanism was chosen, by the author, to provide more resolution for the recorded times than is provided by the VMS system clock. To test the speed at which VMS can query the Facility Time Code Reader, a process was set up to access the time code reader in a loop of 300 accesses as fast as possible. Each access of the time code reader is compared to the time of the previous access and any comparison greater than one millisecond difference is flagged. The process was executed

ten times. On average, 3.5 accesses generated time differences which were greater than one millisecond. This test indicates that the time code reader can be read with one-millisecond resolution more than 98% of the time. This one-millisecond resolution is considerably better than the ten-millisecond resolution provided by the VMS system clock. The better resolution was desired to provide an accurate recording of the data system response times.

2. Data Packet Descriptive Information

A forty-byte header of descriptive information was developed by company engineers and scientists to provide commonality of the descriptors of the user packets transmitted over the Ethernet network. This information is attached to all user data requests and data packets transmitted over the network except for communication packets to and from the DPS computer. The forty-byte standard header was not implemented on the DPS; instead, a two-byte packet, consisting of a single function word, is required for the data request to the DPS. In this descriptive information, attached to user data packets, some of the bytes are not used in all data transfers and some were left blank for future expansion of information contained in the header. These 40 bytes are shown in Figure 8.

3. Response Time Data Acquisition Algorithm

The Facility Time Code Reader is read just before the data request and then again just after the data are received by the Facility

Word

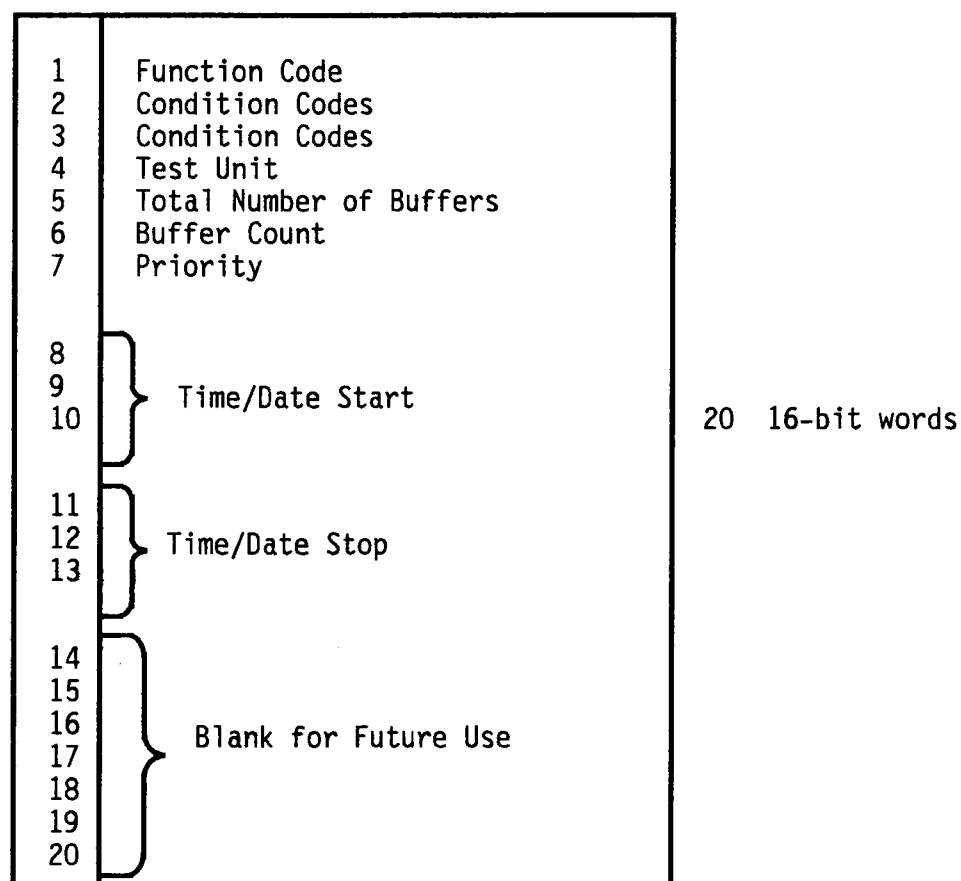


Figure 8. Network Standard Communication Header Information

Computer. These before and after times are subtracted yielding a delta response time. The calculation of the delta response time can be written as follows:

$$\text{DELTA RESPONSE TIME} = T2 - T1$$

where T1 is the time immediately before the data request and T2 is the time immediately after the data are received. A set of timing data from each data acquisition system was produced. Each set of data is comprised of 300 data requests with approximately 0.0 to 0.5 seconds random delay between each request to simulate the randomness of actual data acquisition timing. The random delay time is generated using the VMS random number generator and invoked using the VMS run time library routine LIB\$WAIT.

4. Data System Response Time Presentation Method

To facilitate the presentation and understanding of the response times, the data are presented in graphical form. The abscissa of the plots represents the request number, range 1 to 300, while the ordinate represents the response time of that particular request in milliseconds. In addition to the graphical information on the plots, the minimum, maximum, and mean response times are listed for each system. For interpretation of the consistency in system response times, the standard deviation and variance [8] of the response times are also shown.

5. DMACS Response Times

The first set of data presented is the response times of the DMACS computer. To obtain data from the DMACS computer, the Facility Computer sends down the standard 40-byte data request packet. The request packet is sent to a DMACS communications process, which in turn passes it to another communication process on the DMACS. This second process packages the data requested and transmits the data to the Facility Computer. The data are continuously updated in the DMACS memory by the KXT peripheral processor for use by the communication processes. The data presented here are that of a series of master data buffer requests. The master buffer contains all data available from the DMACS and consists of the 40 header bytes, 384 bytes of digital data, and 340 bytes of control information for a total of 764 bytes. This buffer is shown in Figure 9.

The response time of the DMACS is presented in Figure 10. The average response time is 126.83 milliseconds while the minimum and maximum times are 91 and 184 milliseconds, respectively. The erratic behavior of this system yields a standard deviation in response time of 27.34 and a variance of 747.53.

6. DDAS Response Times

The next set of data is the response times of the DDAS computer. Data are obtained from the DDAS by use of the 40-byte header packet described earlier. This system also uses two communication processes, one to receive requests and the other to process the request and

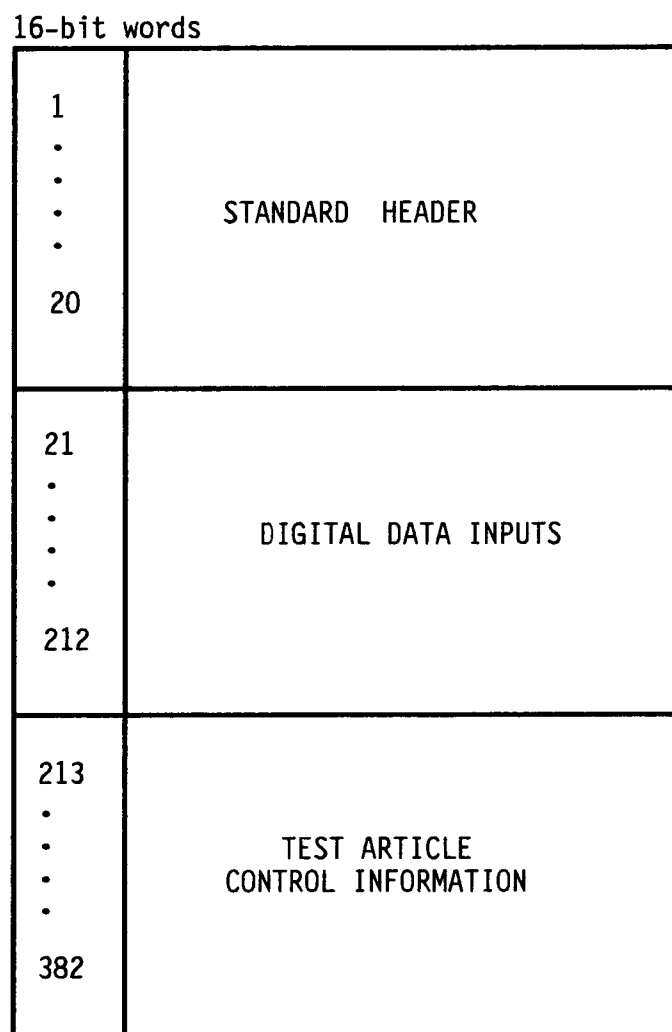


Figure 9. Digital Multiplexer and Control System Master Buffer Layout

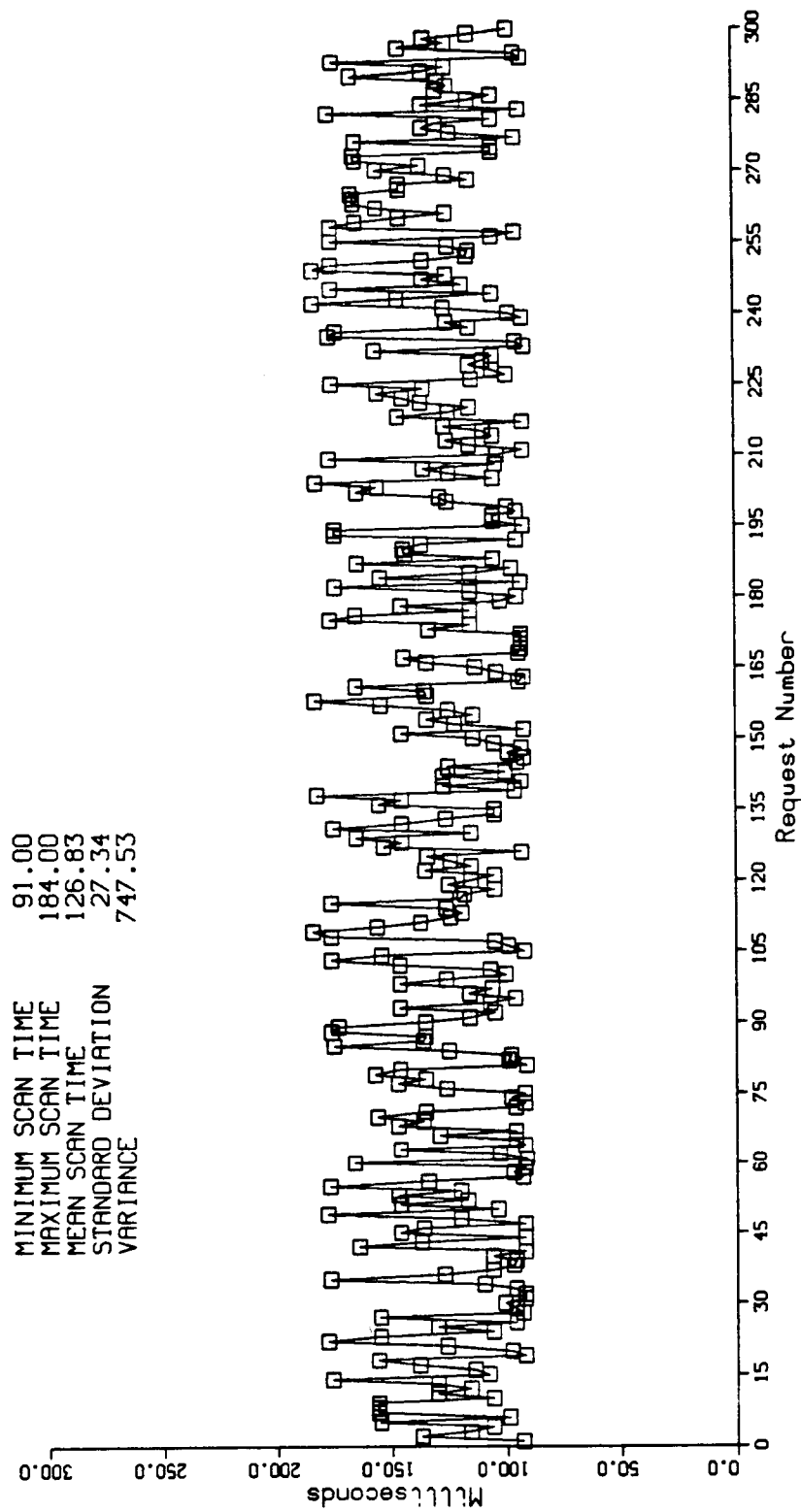


Figure 10. Response Times of the DMACS to Facility Computer Request

transmit the data packet. The data on the DDAS are continually acquired and filtered and are therefore available to the communication process through global memory sections at any time. Data from the three DDAS subsystems may be obtained independently or in one master buffer data transfer. Normally all data are acquired through the use of the master buffer transfer since this condenses three data requests and transfers into one. The layout of the DDAS master buffer is shown in Figure 11. The test was made on an average size DDAS data packet of 164 bytes.

The results of this test, shown in Figure 12, show an average response time of 85.8 milliseconds with a minimum and maximum response time of 52 and 167 milliseconds, respectively. The standard deviation of 20.62 and variance of 425.32 indicate that the response times were not consistent.

7. DPS Response Times

Obtaining data from the DPS computer is different from the other data acquisition systems. As described earlier, the DPS data request packet contains only a two-byte function code, not the standard forty-byte packet. Also, this system uses only one communication process. This process accepts requests, asks other processes to service the request if necessary, packages the data, and then transmits it to the Facility Computer. Pressure subsystem data are continuously made available to the communication process by other processes running on the system. ESP requests must be explicitly serviced at the time of the request.

16-bit words

1 20	STANDARD HEADER
21 . . . 20+L	DIGITAL SUBSYSTEM
20+L+1 . . . 20+L+2M	FAMROS SUBSYSTEM
20+L+2M+1 . . . 20+L+2M+2N	ANALOG SUBSYSTEM

L = Number of
Digital InputsM = Number of FAMROS
InputsN = Number of Analog
Inputs

Figure 11. Digital Data Acquisition System Master Data Buffer Layout

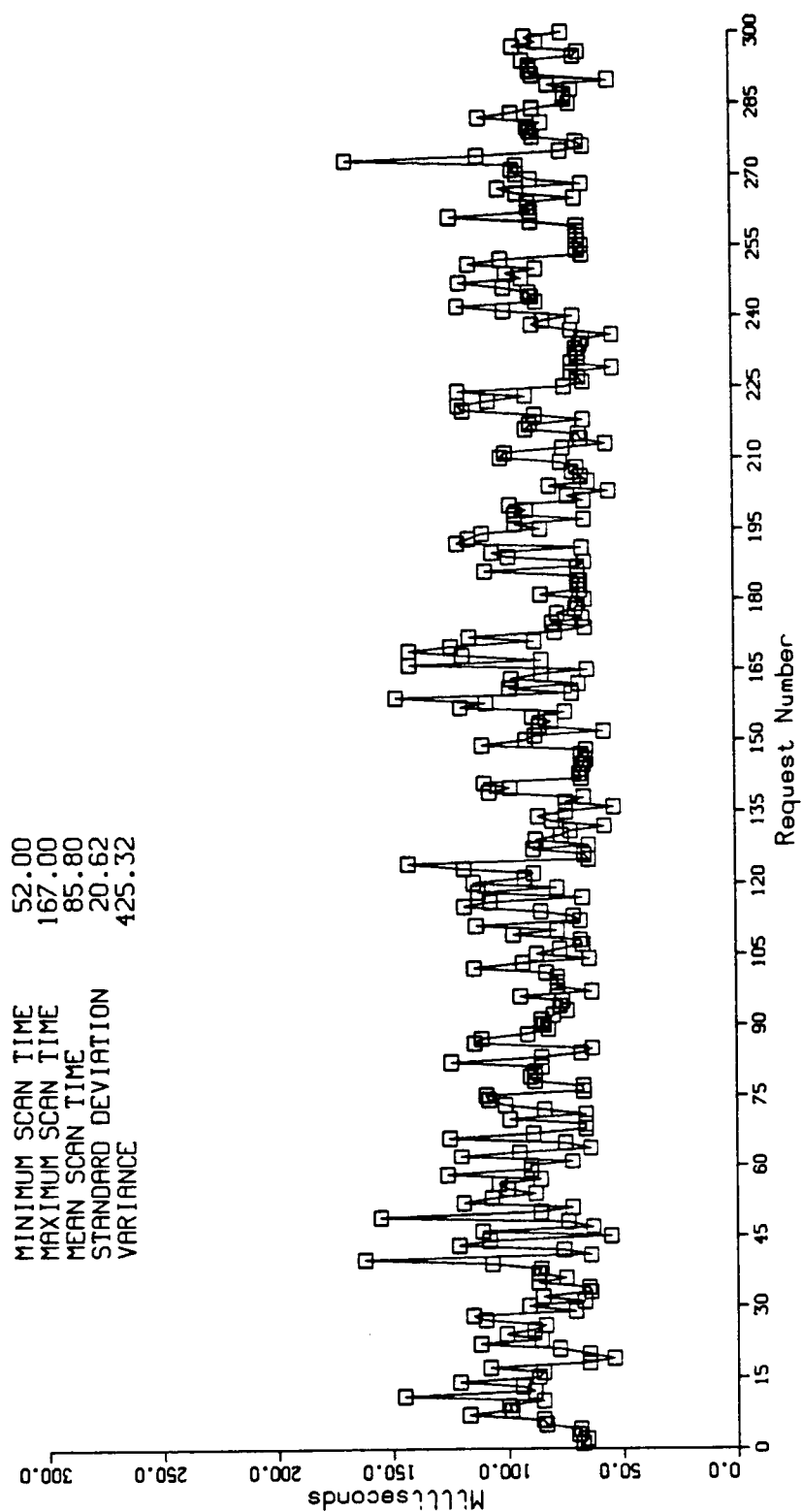


Figure 12. Response Times of the DDAS to Facility Computer Request

The response time data are collected using the same technique as used with the DMACS and DDAS. A master data buffer is sent to the Facility Computer on each data request. This buffer is the same size, 2800 bytes, whether it is a pressure subsystem or an ESP subsystem request. However, the ESP data may require multiple master buffer transmissions. The master data buffer is shown in Figure 13.

The response time for a DPS pressure subsystem request was very consistent as shown in Figure 14. The minimum and maximum times, 141 milliseconds and 158 milliseconds, respectively, are within 20 milliseconds of each other. This produced a very respectable 2.29 standard deviation and 5.24 variance calculation. The average time from request to receipt was 143.72 milliseconds.

Because of complexity of the ESP data acquisition process and process size restrictions on the PDP11 computers, ESP subsystem data acquisition in the DPS computer is different from the pressure subsystem data acquisition. The ESP data are not continuously acquired on the DPS system and must be taken upon request. The communication process in the DPS requests another process to service the ESP data request. Upon completion of data acquisition, the communication process is notified to package the data and send it to the requester. The minimum and maximum response times are 741 milliseconds and 1117 milliseconds, respectively. The average response time calculated over 300 samples is 883.64 milliseconds. The response times are very inconsistent yielding a standard deviation of 63.62 and a variance of 4047.14. The graph of this data is presented in Figure 15.

1 . . . 30	MASTER BUFFER DESCRIPTOR WORDS
31 32	BLANK BLANK
33 92	DIGITAL SUBSYSTEM
93 94	BLANK BLANK
95 . . 1400	PRESSURE SUBSYSTEM OR ESP SUBSYSTEM

Figure 13. Digital Pressure System Master Buffer Layout

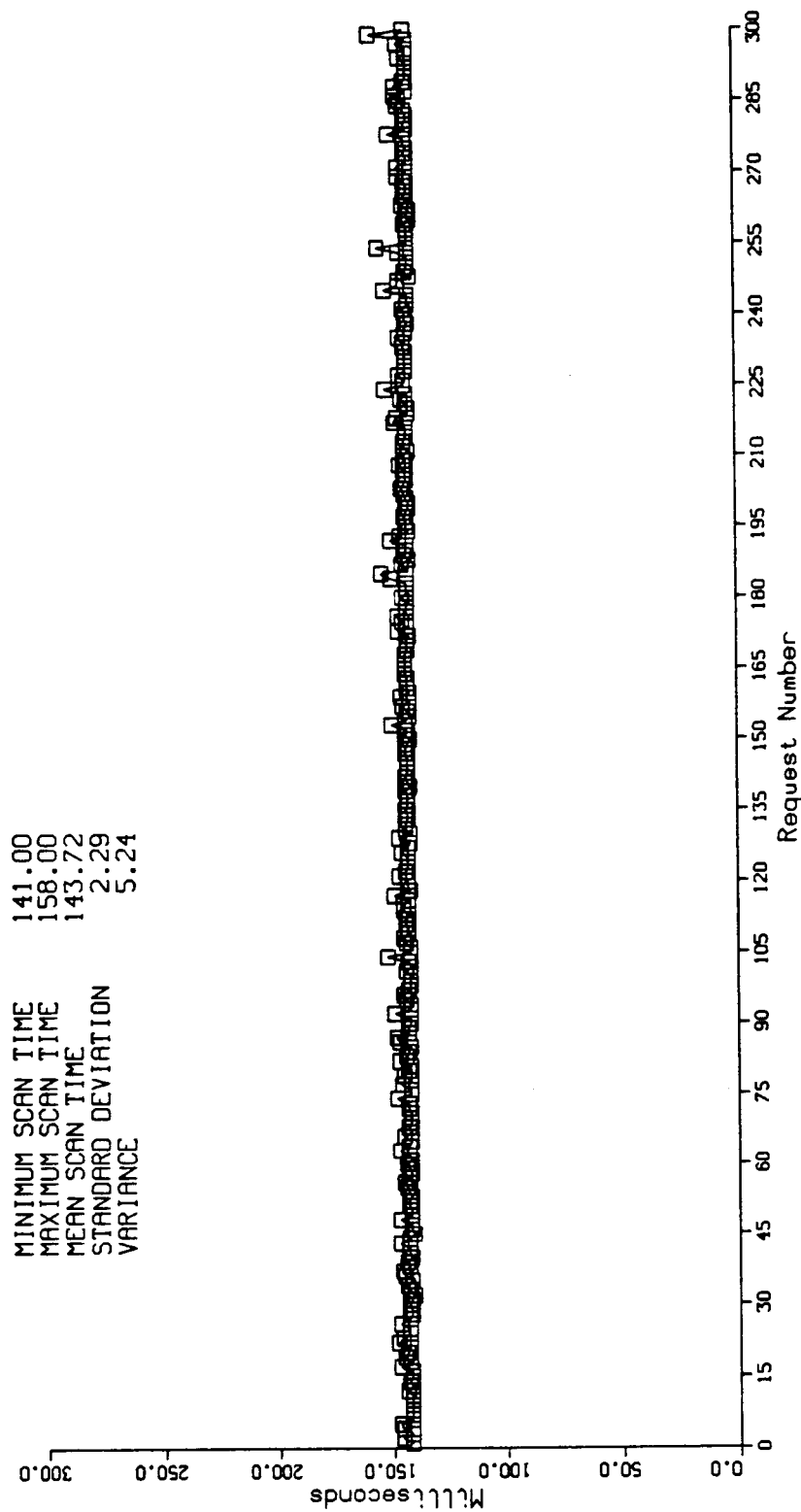


Figure 14. Response Times of the DPS Pressure Subsystem to Facility Computer Request

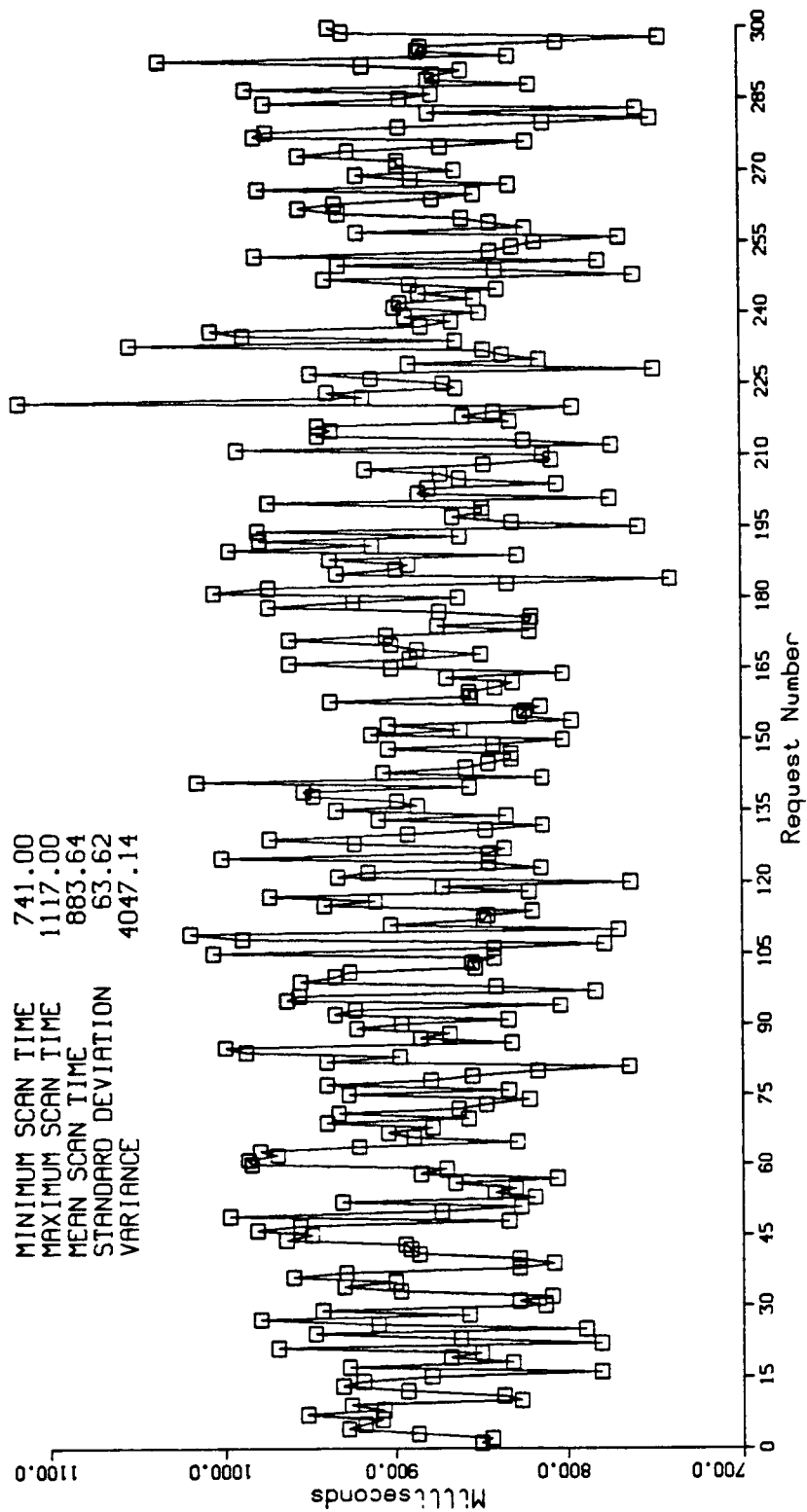


Figure 15. Response Times of the DPS ESP Subsystem to Facility Computer Request

During collection of these data it was noticed that the average of the ESP data response time was different for different test installations. Further investigation revealed that the ESP software averages several samples of the input data to achieve a filtering of the data before final processing. The number of samples to average is an input to the ESP software determined by the expected dynamic characteristics of the pressures to be measured. As shown in Figure 16, changing the number of samples has a significant affect on the average response time. Each curve on the graph represents an increase in the number of samples to average of five samples, starting with five samples and incrementing to twenty samples. As shown, each five sample increase raises the average response time by approximately 300 milliseconds. This clearly shows that this number should be carefully chosen to provide the minimum response time while maintaining the desired data quality.

8. Response Time Inconsistencies

The inconsistency of the response times of the data acquisition computers is of much concern to the engineers testing in the facility. The major concern is the development of new test article control algorithms which are time-dependent. This problem is magnified since the two systems required for control, the DMACS and the DDAS, are the most inconsistent. Since the ESP pressure data are usually acquired after the model is in position, that inconsistency is less critical; however, still important. Two possible causes of the inconsistency

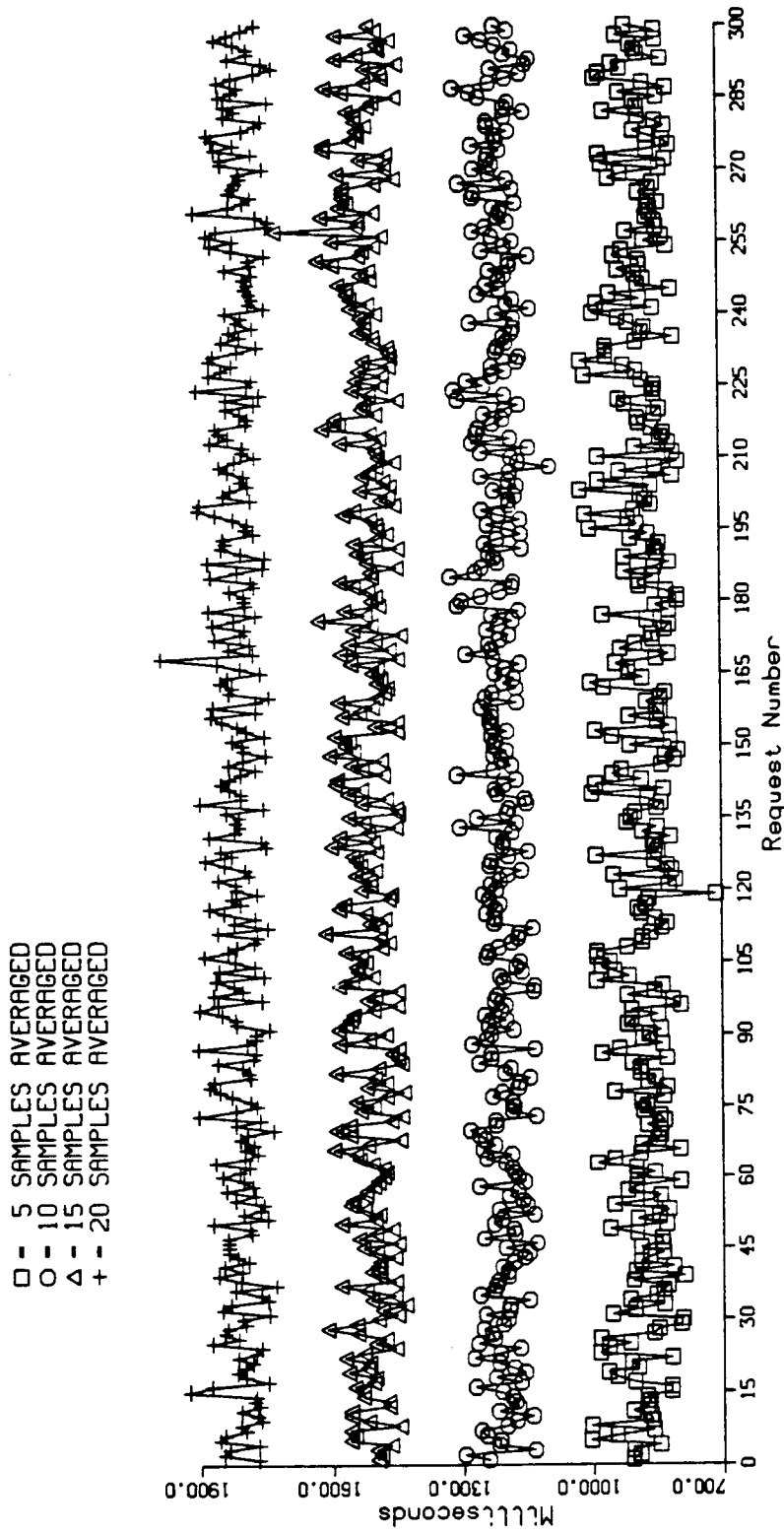


Figure 16. Response Times for Different Number of Samples on the DPS ESP Subsystem to Facility Computer Request

quickly came to mind. These are the priority of the data system communication processes and the structure of the communication code.

Since the test unit usually operates 24 hours per day, 7 days per week, time was not available on the actual data system for investigation of the problem. Therefore, hardware which closely approximates the actual hardware was used. The communication software from the DMACS computer was chosen for the investigation. The response time test was made on this software and the new hardware to verify that it was similar to the real DMACS. The data in Figure 17 show that this is indeed the case, since it closely resembles the data shown in Figure 10, page 22. Since the communication code of the DDAS very closely resembles that of the DMACS, it is assumed that the inconsistency of both systems stems from the same problem.

The priority of the data communication process on the data acquisition computers was the first candidate for consideration. However, it was quickly dismissed as being the cause of the response time inconsistency problem for two reasons. First, since the KXT11 peripheral processor supplies the DMACS with its data, the DMACS processor has almost nothing to do except service data requests. Since there are so few processes executing on the processor, increasing the priorities of the communication processes would have no effect on their execution times. Second, the DPS pressure subsystem buffers, which are very consistent, come from a processor which is scanning data instrumentation and performing digital filtering on these data continuously. Therefore, if priority was the problem, the response times of this heavily

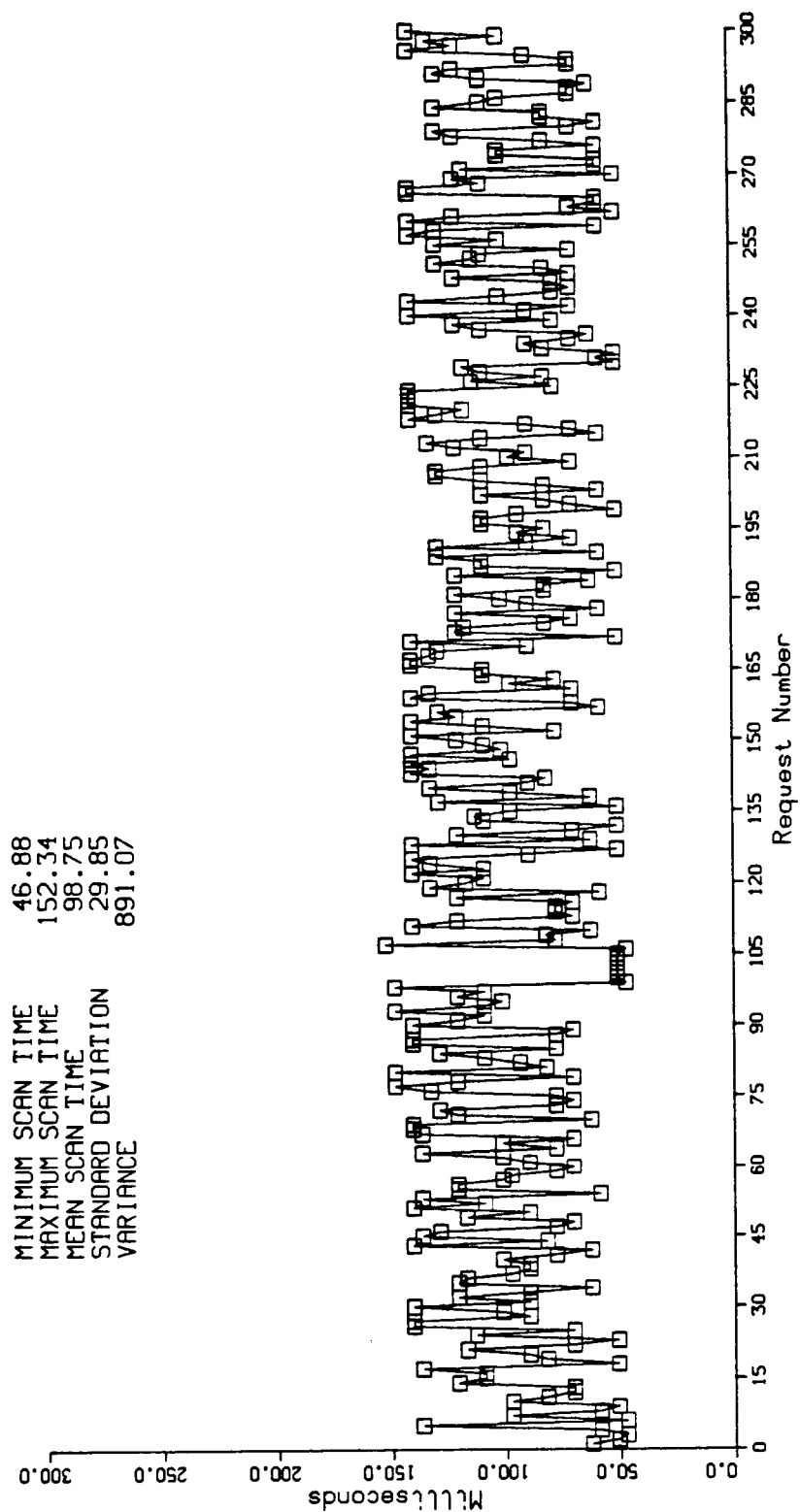


Figure 17. Simulation Case of DMACS Response Times

used system would show more of an inconsistency problem. Because of these two reasons, process priority was eliminated as the possible cause of the response time problem.

Since the process priorities do not have a significant effect on the response times, the structure of the communication code was investigated. As described earlier, the DMACS communication software consists of two separate processes. One process receives the request and passes that request to the second process which interprets and responds to it. The communication between these two processes is accomplished via system global common and the use of RSX event flags. Since it was suspected that this interprocess communication is the cause of the problem, a single process was developed to accomplish the functions of the previously used two processes. The response time test was executed on this single communication process to verify this theory. As suspected, the average response time of this system dropped and the consistency of the response times improved dramatically. The data are shown in Figure 18. These data clearly show that it is the interprocess communication which is causing the problem. It is also concluded that the response times of the DMACS as well as the DDAS could be significantly improved if the single process communication was adopted.

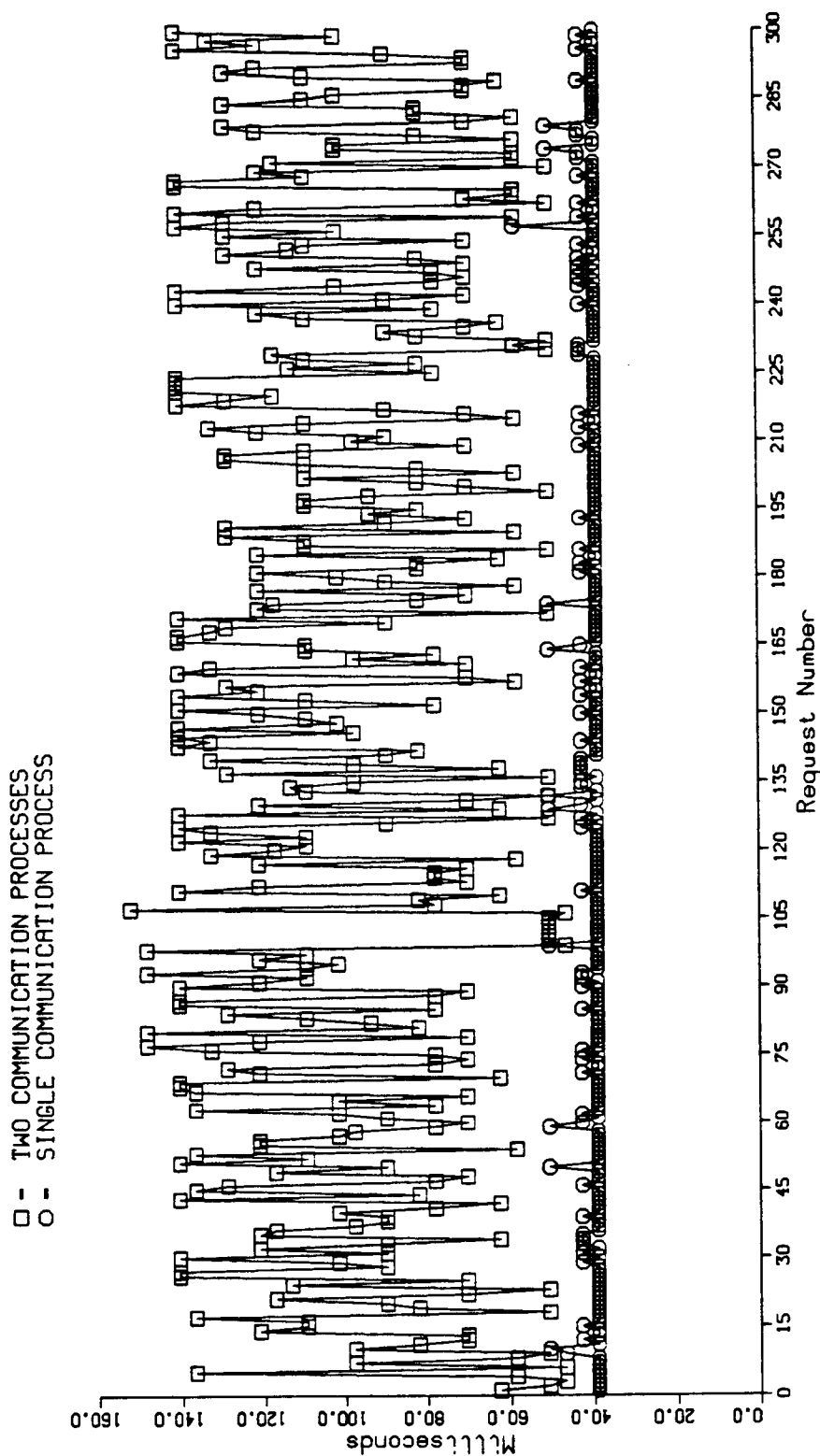


Figure 18. Two Communication Processes vs Single Communication Process

CHAPTER III

DATA CYCLE TIME STUDY

The data cycle time study was conducted to give the test engineers a baseline data cycle time to compare with the current data cycle time. This will provide an on-line indication of the operational efficiency. The data presented here will provide this baseline data cycle time.

1. Data Acquisition and Control Process

The data acquisition and control process involves positioning the test article to the desired attitude in the test unit, acquiring steady state data, and repeating the process until the desired data are obtained. The control algorithm begins by calculating the current position of the test article and obtaining, from a predetermined table of set points, the desired position of the model. Only enough data to calculate the model attitude is acquired during the control cycle. Test peculiar control equations, including corrections for deflections of the support mechanisms, are used to determine where the model support mechanism is to be positioned in order to place the model at the desired attitude. The support mechanism positions are sent to the DMACS as control commands to update the digital-to-analog converters which in turn move the model. Repeated model attitude calculations and digital-to-analog converter updates are made during model movement to provide coordinated movement to the desired set point. For best results with this update-during-movement algorithm, real-time response

from the data systems is required. When the attitude is within a predetermined tolerance and the control systems are balanced, a complete scan of data is requested and received from all data acquisition systems. Test unit environmental data acquired in this scan are checked against required conditions. If the conditions are within tolerance the scan is packaged as a data point and written to disk for later reduction, if not within tolerance the data acquisition process is repeated until within tolerance. This control and acquisition process is repeated until all the test article set points are completed for a particular model configuration or set of environmental conditions. The basic control and acquisition algorithm is shown in Figure 19.

The desired test article positions, data inputs, and test peculiar data reduction and control equations are determined before test article installation in the test unit. The data acquisition and control algorithm is standard for nearly all tests, but the data inputs and equations necessary for control may be different.

2. Data Reduction Process

During the execution of the control and acquisition process, another process on the Facility Computer, running at a lower priority, reads the data points written to disk by the main control and acquisition process, completes the data reduction calculations, sends hard copy outputs to the print server for printing, sends data to the graphics system for plotting, sends the point to the Central Computational Facility for further analysis, and writes the completely

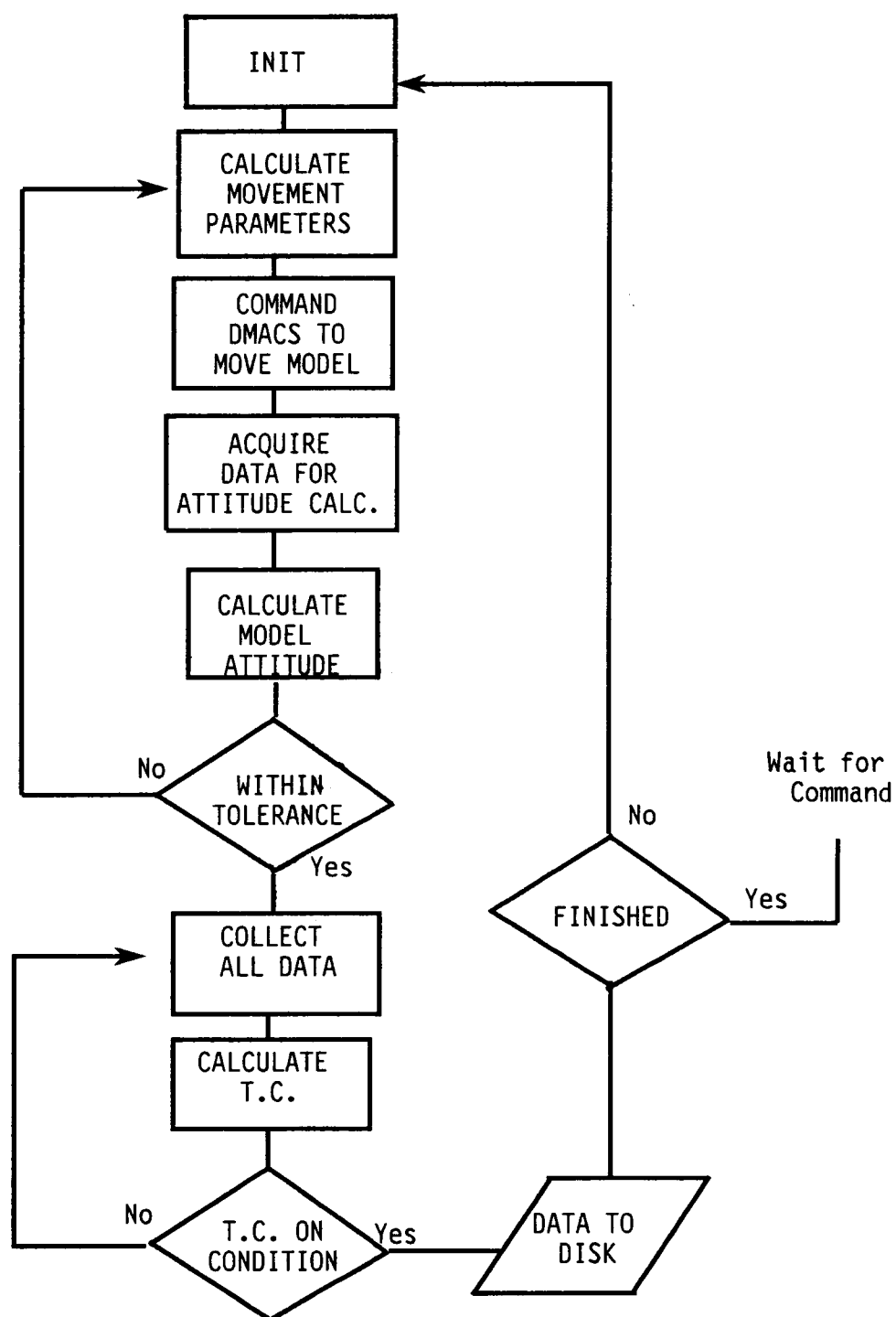


Figure 19. Data Acquisition and Control Algorithm

reduced data point back onto the disk. The effect of this process on the data cycle time was not considered since no data acquisition occurs in this process and the network traffic generated by this process is minimal.

3. Near Real-Time Data Display Process

Display of near real-time data in engineering units is very important to the monitoring and direction of testing activities. The display of these data is accomplished, as described earlier, by the DPC computer; however, the data are acquired and reduced on the Facility Computer and then transmitted to the DPC. A process in the Facility Computer collects data from the data acquisition systems, reduces it, and sends it to the DPC for the near real-time engineering unit displays. A parameter, set by the main data acquisition and control process, is provided to this process as a delay between update cycles. The delay is longer while the closed-loop control process is running to avoid adverse affects on data cycle time.

4. Data Cycle Time

The evaluated data cycle time is defined as the time from the beginning of the control algorithm for one model attitude to the beginning of the control algorithm for the next model attitude. Data were collected over several tests of various size and complexity during actual test unit activity. Timing statements were embedded in the data acquisition and control process to collect the data.

The data acquisition and control sequence previously described is broken down into nine functional times to make up a complete data point. The data collected are averaged for each test entry to describe the average data point. The nine functional times are defined as follows:

1. DDAS data acquisition time
2. DMACS data acquisition time
3. DMACS control time
4. DPS data acquisition time
5. ESP data acquisition time
6. DPC access time
7. Delay time
8. Storage time
9. Residual time

The DDAS, DMACS, DPS, and ESP data acquisition times are the elapsed time from data request until data receipt. The DMACS control time is the length of time from the sending of a control packet to the DMACS until this request is honored and a master data buffer is received. The time taken sending messages and model attitude tables is shown in the DPC time. Delays may be required at certain points in the data acquisition cycle to allow instrumentation to respond, filters to settle, etc. These times are shown in the delay time. Time to write the data point to the disk is indicated by the storage time. All other time is shown under the residual time. This residual will include the

calculation of model attitudes, environmental conditions, timing data acquisition, and the checking of tolerances placed on the acquisition of the data point.

5. Data Cycle Time Data

The first test evaluated was a relatively small test in terms of data acquired. The DMACS data buffer consisted of the standard 724-byte master data buffer. No ESP data were taken on this test while the standard DPS pressure buffer of 2800 bytes was acquired. The DDAS master data buffer was a combination of 30 digital inputs, 7 FAMROS inputs, and 4 analog inputs for a total of 164 bytes. Changes in model attitude between data points were relatively small on this test. Almost 10,000 on-line data points were processed for this test. A data cycle time average was obtained from these data as presented in Table 1, row Test 1. The data show that the DMACS and DDAS were accessed five times each per data point. This was determined by dividing the DMACS and DDAS times by their respective averages from the individual timing study data. Since the DPS is only accessed after the test article is in position, the DPS times per point should be very close to the individual time study data. As shown in the data table, this is indeed the case. On this test entry, a one-second delay was made after the model was in position and before taking the final data scan. As shown by the delay time of 1.021 seconds, a few times the environmental conditions were out of tolerance and the final scan was repeated adding to the delay for that particular point and increasing the average slightly.

Table 1. Summary of Data Acquisition Cycle Time

Test	Total Average	DDAS ₁	DMACS	DMACS Control	DPS	ESP	DPC	Delay	Storage	Residual
1	4.282	0.456	0.615	0.565	0.150	0.000	0.049	1.021	0.508	0.918
2	7.375	0.404	0.523	1.596	0.650	1.447	0.043	1.352	0.454	0.906
3	6.826	0.520	0.649	0.821	0.861	2.133	0.018	1.097	0.405	0.322
4	8.147	0.317	0.413	1.802	0.332	2.279	0.034	2.000	0.520	0.450
5	7.165	0.304	0.424	1.794	0.166	1.472	0.035	2.000	0.530	0.440

The data shown for test entry 2 on Table 1 included the ESP data subsystem. The average delay for this entry was larger indicating that the test unit operators had a difficult time keeping the test unit on conditions to take data. The most disturbing increase was the relatively large increase in the DPS times over test entry 1. This increase repeats in test entry 3. The change in time for the ESP subsystem between entries 2 and 3 could possibly have been caused by the number-of-samples change as described in the individual timing data, but nothing in the individual timing study gave a clue to the cause of the DPS time increase.

The first area investigated was the cause of the increased DPS time. The possibility of data acquisition collisions caused by the process on the Facility Computer which collects and sends data to the DPC for near real-time displays was studied. The collision could occur when this process is acquiring data and the closed-loop control process tries to acquire the final scan of data. If the collision were to occur, the control process would be delayed while the DPS is servicing the display process request. To test this theory a set of data points was taken while the display program was active and then again with the display program inactive. These data are shown in Table 1, rows Test 4 and Test 5. Row Test 4 shows the data with the display program active and row Test 5 is with the program inactive. As suspected the DPS and ESP times for the display active points were significantly higher than the times for points acquired without the display program.

Approximately one-second difference in the overall data point average is observed between these two sets of data.

6. "Average" Data Cycle Time

Data cycle time has improved over the years of test unit activity to a low of approximately 10 seconds in 1986. As shown in Table 1, page 42, the current data cycle time has been lowered to about 8 seconds when using the ESP pressure subsystem and about 4.5 seconds without the ESP subsystem. This decrease occurred as a result of the implementation of the networked data acquisition, control, and reduction computers. It represents a significant savings in the cost of testing at the facility.

CHAPTER IV

CONCLUSIONS AND RECOMMENDATIONS

The requirement for increased productivity in testing necessitates that the engineers and computer scientists to be very familiar with the characteristics of the data acquisition and control systems network. If the response characteristics for each system are known, abnormalities in a system performance can easily be identified and a solution found. These characteristics should also be known so that any changes to the data systems or network can be easily evaluated.

This thesis presents the data which define the data systems characteristics. The individual timing study provides the mean value and consistency of the response of each system, while the data cycle time study presents the characteristics of the combined functionality of all the data systems. Each test could be executed again to evaluate any changes in the network or data systems or to investigate any problem areas of the network.

During the acquisition and evaluation of the individual response time data, it was noticed that the response times of the DMACS, DDAS, and DPS ESP systems were inconsistent. It is recommended that the communication software processes on the DMACS, as well as the DDAS, be combined into a single process on each system. The DMACS test case presented shows a significant improvement in the data system response consistency as well as a significant decrease in the mean response time. It is expected that the same trend would occur in the modified

DDAS software. The resultant improved efficiency would decrease total data cycle time and improve data productivity.

A problem was also identified in the data cycle time study. A significant increase in DPS pressure subsystem response time was noticed when the DPS ESP subsystem was active. The cause of the increased response time is identified as being a delay caused by the near real-time data display process requesting data at the same time as the closed-loop control process. As shown, the data system response time as well as the overall data cycle time could be decreased by eliminating the execution of the data display process during the closed-loop control process. The engineer responsible for the particular test must decide whether the near real-time data displays are cost effective during the execution of their test.

The data cycle time study shows that the decrease in data cycle time with the implementation of the network is significant. This decrease has allowed the engineers to do more testing by decreasing the occupancy time of currently scheduled tests. As a result, the cost of testing in the facility has been significantly reduced.

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