To the Graduate Council:
I am submitting herewith a thesis written by Zakaraya Hamdan entitled "A Low Power, Rad-Hard, ECL Standard Cell Library." I have examined the final paper copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin Blalock, Major Professor

We have read this thesis
and recommend its acceptance:

Nicole McFarlane

Garrett Rose

Accepted for the Council:

Carolyn R. Hodges

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(Original signatures are on file with official student records.)

A Low Power, Rad-Hard, ECL Standard Cell Library

A Thesis Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Zakaraya Hamdan

May 2023

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Abstract

Space exploration for life both inside and outside of our solar system demand the design and fabrication of robust, reliable electronics that can take measurements, process data, and sustain necessary operations. However, the presence of high radiation and the cold temperature of space poses a challenge to most designers. This thesis presents the design of a radiation-hardened, cold capable emitter coupled logic standard cell library with the intention of being used for space applications. The cells are designed and fabricated in a 90nm silicon germanium BiCMOS process. First, a review of emitter coupled logic is presented. Then, the design methodology for the standard cells are presented. Next, the results of several fabricated standard cells are discussed and analyzed. Finally, the work is concluded and future work is discussed.

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Chapter 1

Introduction

1.1 Motivation

Space is a harsh environment for electronics, providing a much higher susceptibility to ionizing radiation and a constant exposure to cryogenic temperature. Increased interest in space exploration has led to a greater need for electronics designed to withstand such an environment, which we will refer to as radiation hardened (rad-hard) and cold capable electronics. While CMOS is the technology of choice for terrestrial applications, the design criteria for extraterrestrial applications introduces critical reliability concerns regarding CMOS electronics. Some such concerns are the increased leakage of off-state NFET devices and single event latchup due to the radiating environment, both of which can be observered at a total dosage below a Mrad [1]. In addition, cryogenic temperatures exacerbate the generation of hot carrier in nFETs, due in part to the low temperature [2]. These issues provide sufficient motivation for an alternate technology path from CMOS.

The silicon germanium (SiGe) heterojunction bipolar transistor (HBT) offers an attractive solution to designing rad-hard, cold-capable circuits. The structure of the HBT naturally lends itself to multi-Mrad TID tolerance and can withstand temperatures as low as 1 K [1]. Therefore, it is reasonable to consider BiCMOS

a better alternative to strictly CMOS when designing reliable rad-hard and cold capable circuits. This thesis will explore the design of a standard cell library using a BiCMOS design approach to achieve a radiation hardened and cold capable ensemble of circuits.

Chapter 2

Background

2.1 Working Principle of ECL

2.1.1 Current Steering Capability

Emitter coupled logic (ECL) is a subset of the current mode logic logic family (CML). As such, the working principle of ECL is the same as CML: current steering. Figure 2.1 shows a conventional ECL differential pair, the primary mechanism of current steering.

Qualitatively, by using a fixed "tail" current, I_1, the current through each branch of the circuit shown in Figure 2.1 can be determined by the potential difference between $Q1$ and $Q2$'s applied base potentials. Expressing this quantitatively, the collector current can be written as

$$I_c = I_s \times exp(\frac{V_{BE}}{U_T}) \tag{2.1}$$

I_s is the reverse saturation current, V_{BE} is the base-emitter junction voltage, and U_T is the thermal voltage. The current steering can be expressed as a ratio of currents flowing through either device. Arbitrarily choosing the collector current through Q2

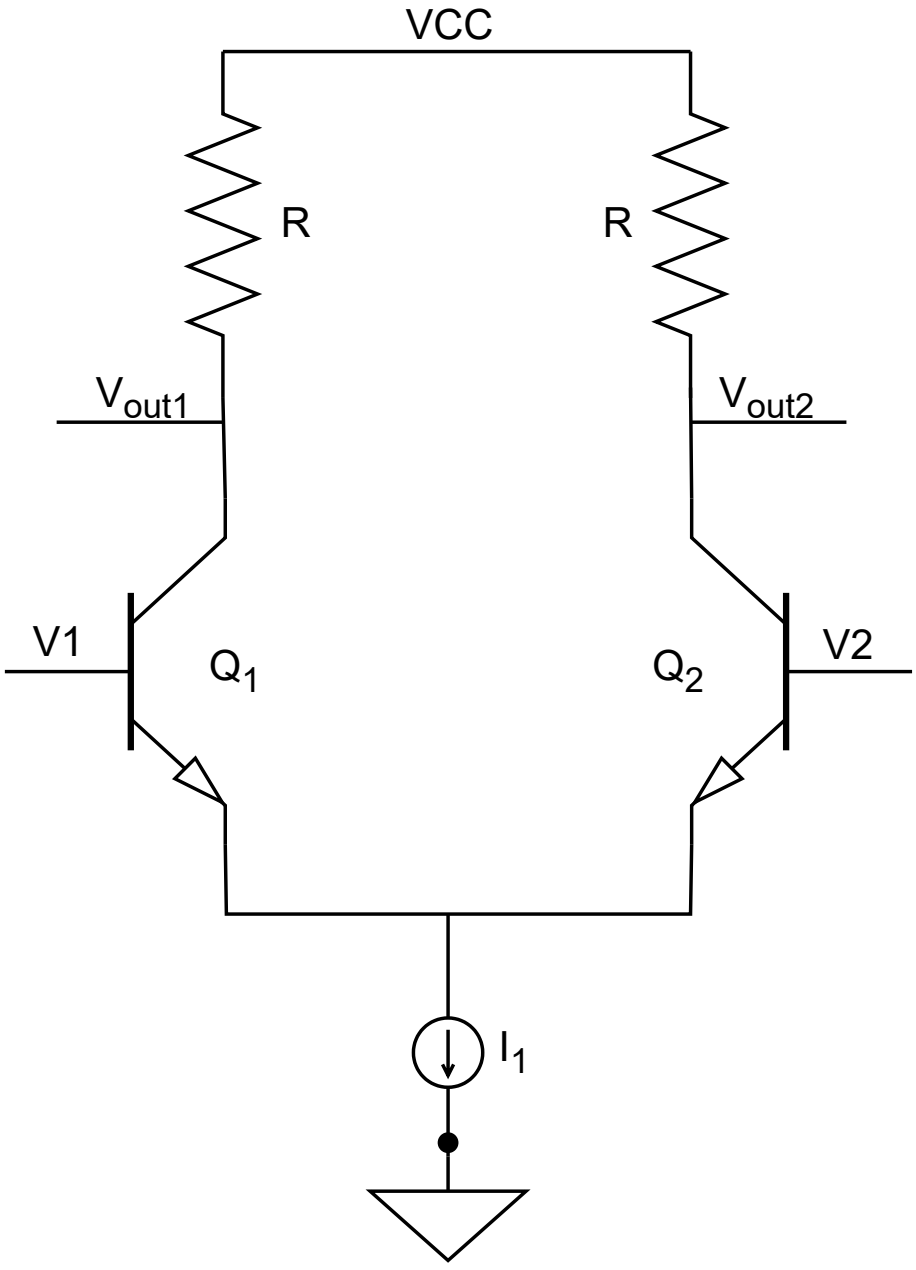


Figure 2.1: Basic "Core" Logic of ECL

as the reference, the amount of relative current through Q1's collector is given by

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1} \times exp(\frac{V_{BE1}}{U_T})}{I_{S2} \times exp(\frac{V_{BE2}}{U_T})} \tag{2.2}$$

If the devices are matched, and utilizing the fact that the emitters of Q1 and Q2 are coupled and hence at the same potential, Equation 2.2 can be simplified to

$$\frac{I_{C1}}{I_{C2}} = \exp\left(\frac{V1 - V2}{U_T}\right) \tag{2.3}$$

From Equation 2.3, it is clear that the current through any branch is an exponential function of $V1$ and $V2$, as well as temperature. This suggests that the relative potential difference between $V1$ and $V2$ need not be so large. As an example, at room temperature, for $Q1$ to draw 95% of the total current, $V1$ must be about $3U_T$ greater than $V2$.

2.1.2 Generation of Logic Levels

Consider the input to output characteristics of the circuit shown in Figure 2.1. First, V_{out1} and V_{out2} can both be expressed as

$$V_{out1} = V_{CC} - I_{C1}R \tag{2.4a}$$

$$V_{out2} = V_{CC} - I_{C2}R \tag{2.4b}$$

Taking this a step further by relating the collector currents to the input voltages $V1$ and $V2$, the output voltages can be expressed as

$$V_{out1} = V_{CC} - \frac{I_1}{1 + \exp\left(\frac{V2-V1}{U_T}\right)} \times R \tag{2.5a}$$

$$V_{out2} = V_{CC} - \frac{I_1}{1 + \exp\left(\frac{V1-V2}{U_T}\right)} \times R \tag{2.5b}$$

These equations provide an upper and lower bound for the output values of the differential pair shown in 2.1. Consider two cases: the first, in which $V1 \gg V2$, and the second in which $V2 \gg V1$. It can be shown that V_{out1} can be approximated as

$$V_{out1} = \begin{cases} \mathrm{V}_{CC} - I_1 R, & \text{if } V1 \gg V2, \\ \mathrm{V}_{CC}, & \text{if } V1 \ll V2, \end{cases} \tag{2.6}$$

The same analysis can be applied to V_{out2}, which yields

$$V_{out1} = \begin{cases} V_{CC} - I_1 R, & \text{if V1} \ll V2, \\ V_{CC}, & \text{if V1} \gg V2, \end{cases} \tag{2.7}$$

These bounds set the basis for defining the logic levels that the ECL circuits will operate with. The designer need only set the current, I_1 and the resistance, R, to set both the logic low level and the potential difference between the logic high and logic low levels, which will be referred to as the logic swing. Of course, the bounds also expose a potential problem with the ECL levels; that is, they are both coupled with the supply voltage. A noisy supply could cause the generation of erroneous bits if not considered carefully. This will be discussed more later in the chapter.

2.1.3 Buffer Stage

The circuit in Figure 2.1 exposes another potential issue with these logic levels. Consider the condition in which $V1$ is much larger than $V2$, meaning that $V_{out1} = V_{CC} - I_1 R$ and $V_{out2} = V_{CC}$ according to Equation 2.7. What happens if these outputs are to be taken as inputs to an identical circuit to Figure 2.1? Applying Equation 2.7 to this case, the result is that the base-collector junction of either $Q1$ or $Q2$ can become forward biased, moving the operation of the transistor from forward-active to saturation.

This can be avoided by level-shifting the logic values down before being used as an input to a succeeding circuit. This is illustrated in Figure 2.2 below.

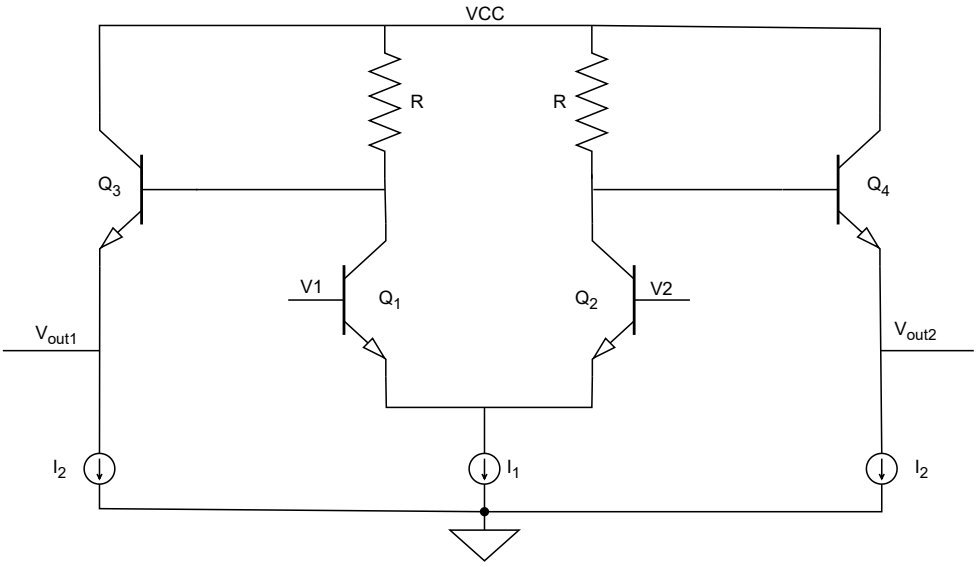


Figure 2.2: ECL Inverter

With the usage of the emitter follower, the new logic level bounds of V_{out1} become

$$V_{out1} = \begin{cases} V_{CC} - I_1 R - V_{BE3}, & \text{if V1} \gg V2, \\ V_{CC} - V_{BE3}, & \text{if V1} \ll V2, \end{cases} \tag{2.8}$$

The addition of emitter followers Q_3 and Q_4 have two great benefits. The first is the inherent level-shifting of the logic signals due to the base-emitter voltage required to keep Q_3 and Q_4 in forward active. Using Equation 2.8, the base-collector voltage becomes

$$V_{bc} = I_1 R - V_{BE3} \tag{2.9}$$

Under the conditions that V_{BE3} is larger in magnitude than $I_1 R$, the transistors Q_1 and Q_2 have no risk of their base-collector junctions becoming forward biased. On the merit of the exponential relationship between the current steering operation and the differential voltage $V1 - V2$, the designer is easily able to maintain a low $I_1 R$ product relative to V_{BE3}.

The second benefit is the isolation that the emitter follower provides between the output and the gain-stage formed by Q_1 and Q_2, allowing for better load drive capability. Unfortunately, the class A operation of the emitter follower can lead to asymmetrical rise and fall times depending on the current I_2.

For simplicity's sake, the upper and lower bounds of the outputs' voltages will be referred to as V_{HI} and V_{LO} respectively. In other words,

$$V_{LO} = V_{CC} - I_1 R - V_{BE3} \tag{2.10a}$$

$$V_{HI} = V_{CC} - V_{BE3} \tag{2.10b}$$

It is also useful to define the maximum voltage swing, denoted as V_s, as

$$V_s = V_{HI} - V_{LO} = I_1 R \tag{2.11}$$

2.2 Quantifying ECL Performance

Any logic circuit that is intended to be used in the synthesis of a larger logic system must have well defined timing and power data. Therefore, it is important to quantify the power, speed, and noise performance of ECL in order to both design these circuits as well as reality check simulation.

2.2.1 Power Consumption

The calculation of the power consumption of the ECL inverter shown in Figure 2.2 is relatively straightforward. First, there are two main components of power consumption: static and dynamic power consumption. In order to compute these components, one must first consider the loading conditions of the logic gate.

Figure 2.3 shows two loading conditions for the emitter follower output stage. In most cases, the real load of an ECL logic circuit will be some combination of capacitance and resistance, but analyzing both cases individually will still provide useful insight to both static and dynamic power consumption.

On inspection of Figure 2.2, it naturally follows that the static power consumption is

$$P_{static} = V_{CC} \times (2I_2 + I_1) \tag{2.12}$$

In the case that the circuits is loaded with a resistive load such as in Figure 2.3b, then there will be additional power dissipated as heat. Since V_{out} transitions from V_{LO} to V_{HI}, the total static power can be written as

$$P_{static} = V_{CC} \times (2I_2 + I_1) + 2(\frac{DV_{LO} + (1-D)V_{HI}}{R_L}) \tag{2.13}$$

where D is the duty cycle.

The second component is dynamic power. In a loaded ECL circuit, there is some capacitive and resistive impedance that generates power loss. These power losses will be seen in the emitter follower stage of the ECL gate.

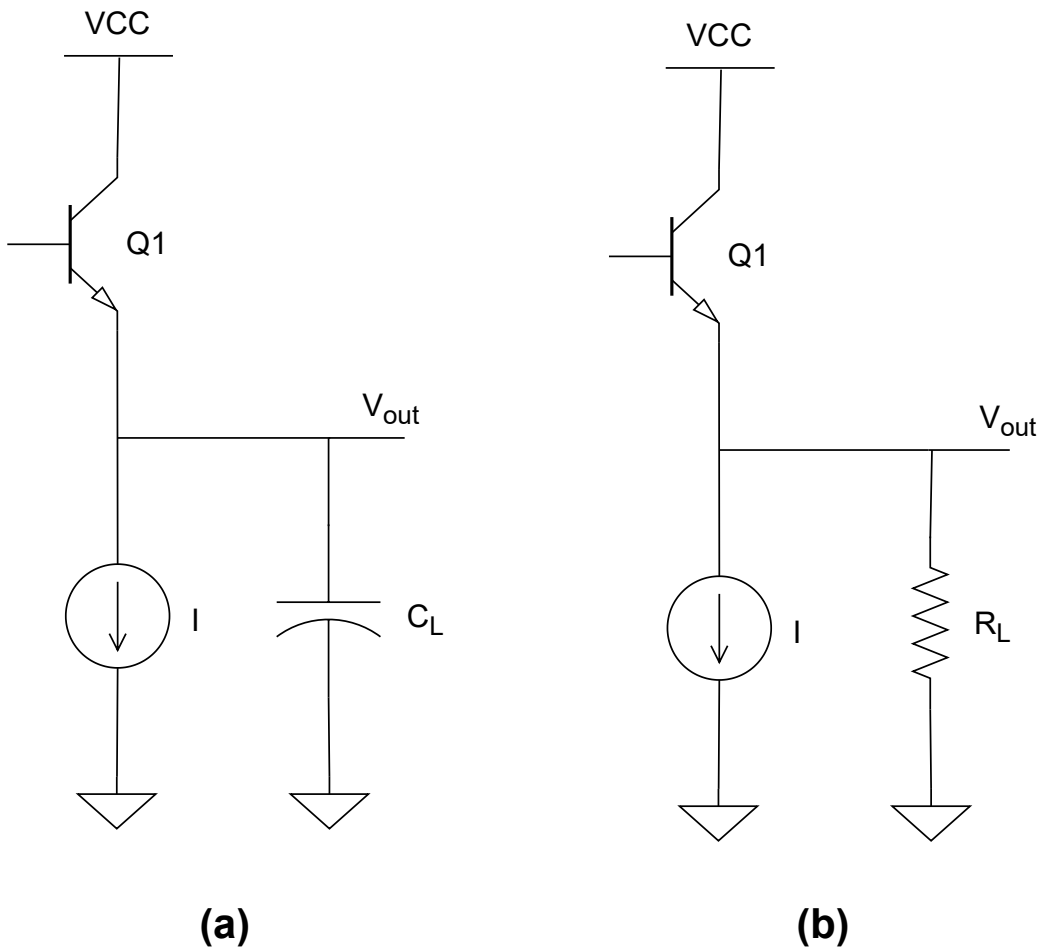


Figure 2.3: (a) An emitter follower with capacitive load and (b) resistive load

In the case illustrated by Figure 2.3a, the current needed to charge the capacitor C_L contributes to the total power consumption.

$$P_{cap} = \frac{1}{2} C_L (V_{HI}^2 - V_{LO}^2) f \tag{2.14}$$

Equation 2.14 describes the power dissipated due to the charging capacitor, where f is the switching frequency of the charging cycle. Dynamic power is largely consumed during the charging cycle of the capacitive load. The capacitor discharges through the constant current source I and therefore consumes primarily static power.

2.2.2 Speed

Considering the ECL inverter unilaterally, there are two nodes that are important for speed analysis. The first is the collector of the transistor $Q1$ and the second is the emitter of transistor $Q3$, both shown in Figure 2.2.

Figure 2.4 shows a psuedo-half circuit of the differential pair in Figure 2.1. In this case, the behavior of the transistor can be abstracted to the behavior of an ideal switch to simplify calculations. However, it is important to note that this abstraction models current steering, and that the transistor $Q1$ remains in forward active operation through this whole process.

As $Q1$ transistions from "on" to "off," the $Q1$'s collector voltage rises and the capacitor begins charging through R from the supply rail. This process is easily modeled by

$$V_c = -RC \frac{dV_c}{dt} + V_{CC} \tag{2.15}$$

The time the capacitor takes to charge is derived from the solution of the differential equation shown in Equation 2.15. Recall the relations provided in Equation 2.7 describe the voltage boundaries on V_c, and therefore provides us with initial conditions

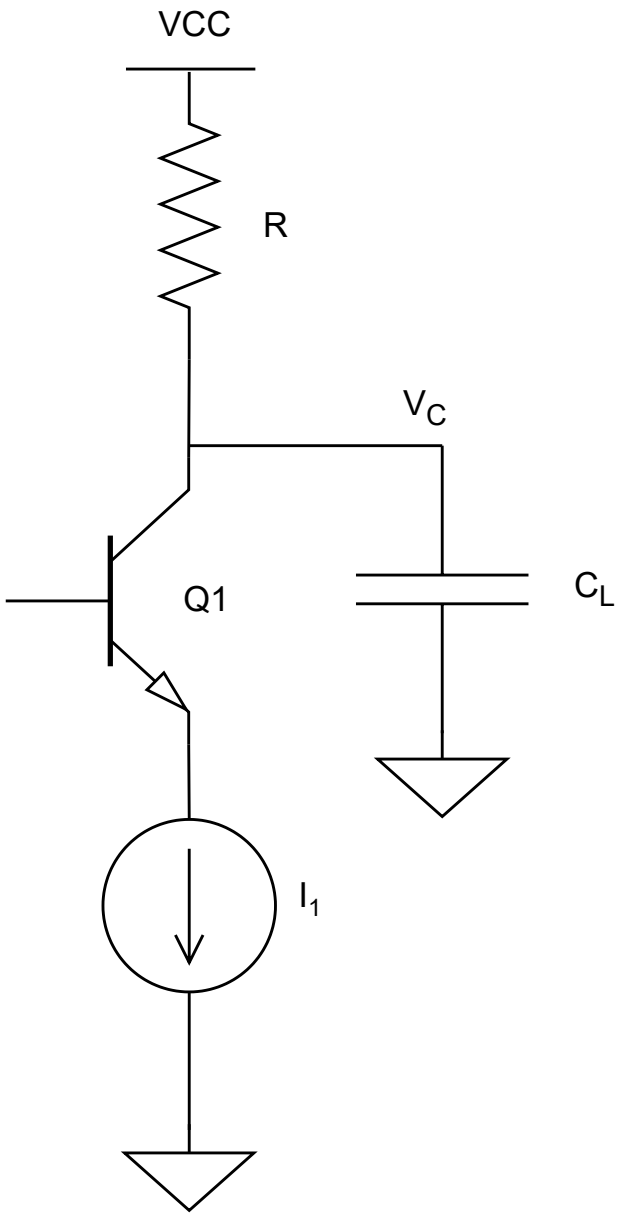


Figure 2.4: Emitter follower output of ECL gate

for solving the differential equations. Indeed, a solution to this equation is

$$V_c = V_{CC} - I_1 R \exp\left(\frac{-t}{RC}\right) \tag{2.16}$$

Next is to consider the transition of $Q1$ from "off" to "on." In this case, the current source I_1 will be the primary mechanism through which the capacitor C discharges. The differential equation modeling this is

$$V_c = V_{CC} - I_1 R - RC\frac{dV_c}{dt} \tag{2.17}$$

Similarly, the boundary values are used to determine the solution of the differential equation, which is

$$V_c = V_{CC} - I_1 R(1 - \exp\left(\frac{-t}{RC}\right)) \tag{2.18}$$

Equations 2.16 and 2.18 show that the speed of the core logic circuitry shown in Figure 2.1 is at least dictated by the resistance and capacitance at the collector nodes. In fact, from the two equations, the propagation delay and rise/fall times can be estimated. For example, if propagation delay is defined as the average time it takes for the output voltage to change by half of its maximum swing after excitation, solving for t reveals that

$$t_{prop1} = RC \ln(2) \tag{2.19}$$

Note that the assumptions made do not consider the finite time response of $Q1$. In reality, $Q1$ does not instantaneously toggle between "on" and "off" and also adds its own parasitic capacitance and resistance. The current source I_1 shown in Figure 2.1 has a finite output impedance that too must be considered. Device biasing should be chosen well to achieve expected results.

Next, the same analysis will be applied to the emitter followers shown in Figure 2.2. In this case, the output resistance of the current source I_2 will be considered as it is a crucial consideration when defining the speed for this stage.

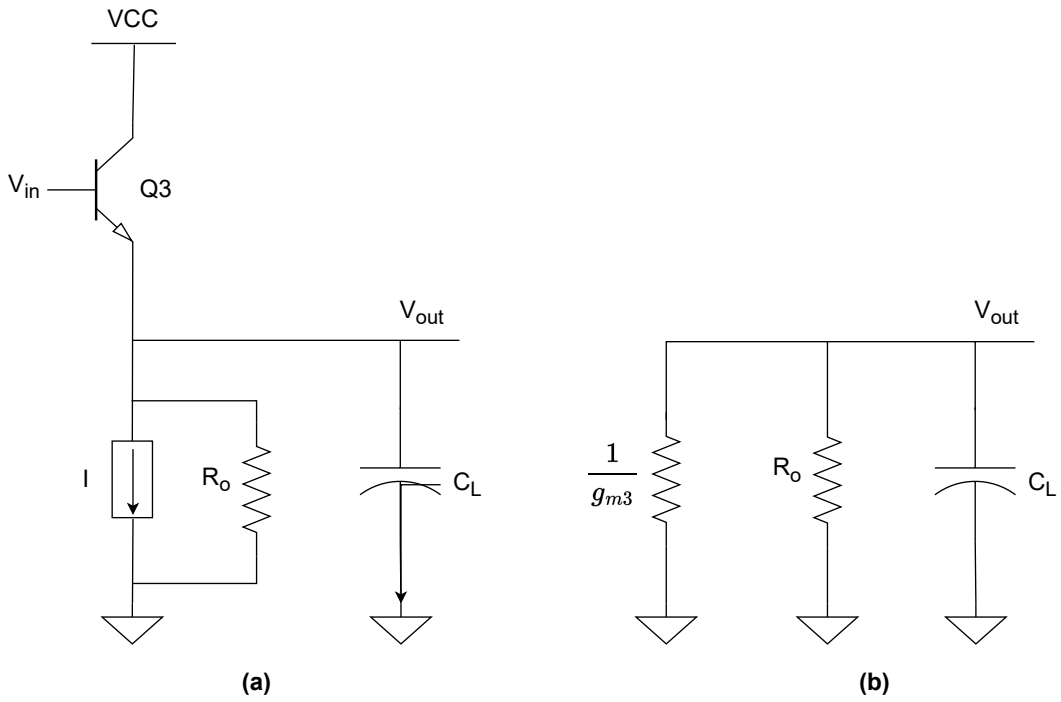


Figure 2.5: (a) Emitter Follower output stage and (b) simplification of transistor Q3 to its small signal impedance

First, the circuit should be analyzed qualitatively. Consider the response of the circuit shown in Figure 2.5a to a rising transition applied to its base. Due to the capacitance on the emitter node, the emitter potential cannot change instantaneously and is instead maintained on the node for a period of time. This means that the base-emitter voltage has increased by IR. This causes $Q3$ to source more current which will charge the capacitor C. As this happens, the base-emitter voltage slowly decreases, in turn decreasing the current sourced to $I1$ until the current through $Q3$ returns to I and the capacitor is fully charged.

$$\exp\left(\frac{-V_{out}}{U_T}\right) - \frac{1}{\alpha r_o}V_{out} - \frac{1}{\alpha}C\frac{dV_{out}}{dt} = \frac{1}{\alpha}I_o \tag{2.20}$$

Unfortunately, Equation 2.20 does not have a closed form solution due to the nonlinear component. Instead, the equation is simplified by approximating the HBTs behavior as an impedance during the signal transition, as shown in Figure 2.5, where g_{m3} is given by

$$g_{m3} = I_2/U_T \tag{2.21}$$

By doing this, the RC time constant, which appears both in Equations 2.16 and 2.18, can be used to estimate the charging time.

$$\tau_c = \frac{U_T}{I_2}||R_o \times C_L \approx \frac{C_L U_T}{I_2} \tag{2.22}$$

During the falling transition, the load capacitance limits the speed at which the emitter voltage can change, meaning that when the base voltage of $Q3$ falls, V_{BE3} decreases. As a result of this, $Q3$ sources less current than during quiescent operation, which is typically set by the current source I. This means that the capacitor discharges charge at the rate given by the difference in current of I and $Q3$. If $Q3$ is sourcing much less current than I, it follows that the discharge time largely depends on the current source and its effective impedance.

$$\tau_d = R_o C_L \tag{2.23}$$

Using these time constants, an estimate of the propagation delay as a result of the emitter follower can be made.

$$t_{prop2} \approx \frac{\ln(2)}{2} C_L \left(\frac{U_T}{I_2} + R_o\right) \tag{2.24}$$

Now, by combining Equations 2.19 and 2.24, the total propagation delay of the circuit in Figure 2.2 is approximately

$$t_{prop} \approx \ln(2)\left(RC + 0.5C_L\left(\frac{U_T}{I_2} + R_o\right)\right) \tag{2.25}$$

where V_A is the Early Voltage. Equation 2.25 provides a slightly optimistic method of estimating propagation delay based on the design and application of an ECL inverter. It also reveals a few key takeaways about the speed of ECL:

- The propagation delay has at least a first order dependence on temperature through U_T. Another source of temperature dependence come from the tail current I_2.
- The propagation delay is impacted more by choice of I_2 than I_1.
- In the case of 2.2, C is simply the input capacitance of a single HBT, suggesting that the capacitance C_L is more likely to dominate the propagation delay.

2.2.3 Noise

Noise is an important consideration for any logic circuit due to its ability to generate output error states. For ECL, there are many potential sources of noise, such as power supply perturbations, parasitic IR drops, and process variation. Additionally, the generation of a reference voltage and reference current to be used in an ECL gate can also introduce noise to the system. It is therefore useful to define a method of characterizing an ECL gate's noise immunity.

As a consequence of the high speed capabilities of ECL, static noise margin has become the most reliable metric of noise immunity for ECL. The static noise margin (SNM) quantifies the minimum amount of noise voltage required to create an erroneous bit. There are many techniques for measuring the SNM, but this section will discuss the unity gain method used by Foley and Bannister [3].

Figure 2.6 illustrates a basic inverter transfer function. A distinction between V_{HI} and V_{LO} is made for the input voltage and the output voltage, where V_{IL} and V_{IH} denote the input low and high logic levels respectively, and V_{OL} and V_{OH} denote the output low and high logic levels respectively.

Analyzing Figure 2.6, it is unclear how the values of V_{IL}, V_{IH}, V_{OL}, and V_{OH} are chosen. For the purposes of SNM, these points refer to the positions on the transfer curve where the slope is unity. Areas on the transfer curve where the slope is less than unity are consider stable logic states, and slopes greater than unity denote the transition regime. The SNM is then defined as the minimum "distance"" between stable logic states, which is expressed as

$$\text{SNM} = \min |(V_{OH} - V_{IH}, V_{OL} - V_{IL})| \tag{2.26}$$

In this case, both the logic high values and the logic low values must be considered, and the minimum will be taken as the SNM. Now, the SNM of the simple ECL inverter shall be derived by calculating V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

To begin, the circuit from Figure 2.2 will be consider again, but this time, additional considerations will be made. First, the supply voltage has been level shifted such that the input waveform and output waveform are both settled around ground. $V2$ is set to ground, which is the midpoint of the input logic levels. Second, the emitter resistance is not neglected but instead modeled as a lumped resistor R_E. These changes are illustrated in Figure 2.7. Additionally, the following analysis will be unilateral to reflect standard SNM calculations. This should not affect the accuracy of the following analysis.

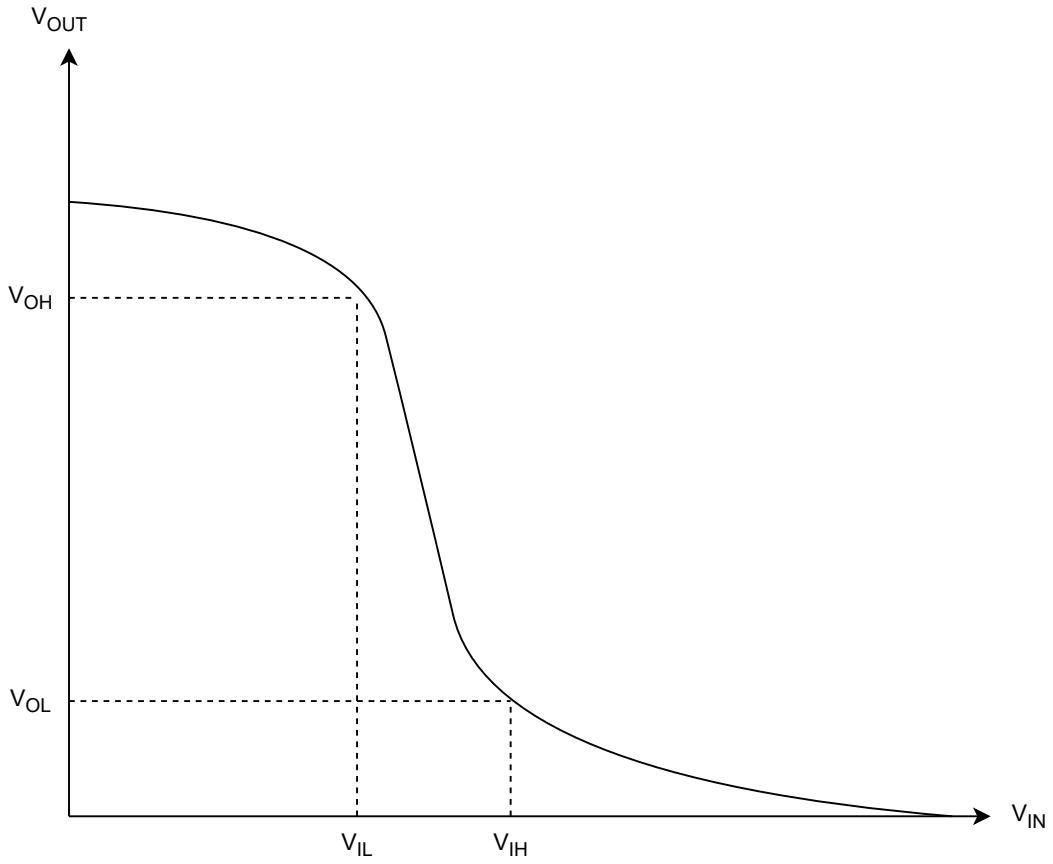


Figure 2.6: Example Inverter Transfer Function

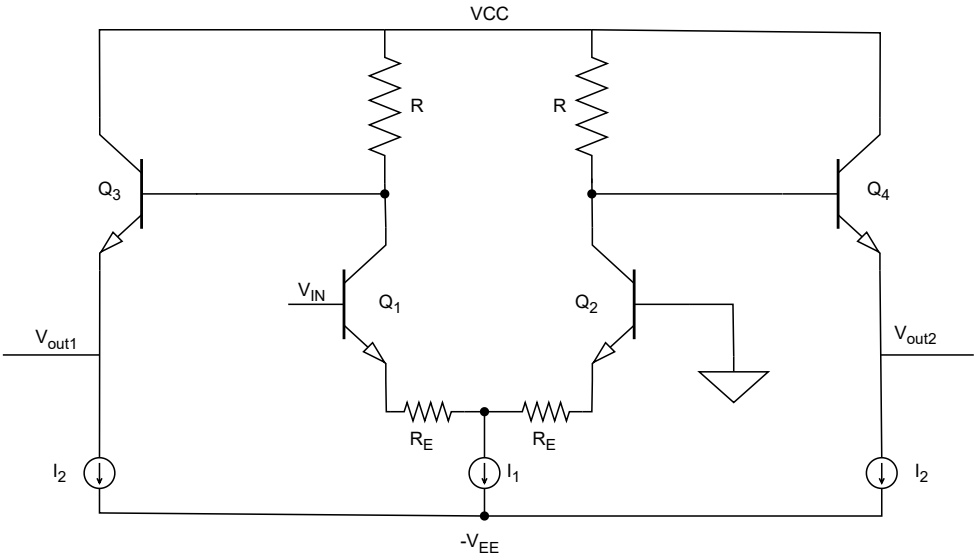


Figure 2.7: Simplified ECL circuit model for noise analysis

Using the loop created around the bases of $Q1$ and $Q2$, as well as using Equation 2.2, V_{IN} can be expressed.

$$V_{IN} = U_T \ln(\frac{I_{C1}}{I_{C2}}) + R_E(I_{C1} - I_{C2}) \tag{2.27}$$

I_{C1} and I_{C2} are the collector currents of $Q1$ and $Q2$ respectively. Since this analysis is intended to be unilateral, I_{C2} will be expressed as a difference of currents.

$$V_{IN} = U_T \ln(\frac{I_{C1}}{I_1 - I_{C1}}) + R_E(2I_{C1} - I_1) \tag{2.28}$$

V_{out1} is centered about ground as well, and the voltage swing V_s has been defined by Equation 2.11. From this, it is clear that V_{out1} can be expressed as follows.

$$V_{OUT} = \frac{V_s}{2} - I_{C1}R \tag{2.29}$$

Using algebra and Equation 2.29, Equation 2.28 can be written as a function of V_{out1}, given by the following Equation.

$$V_{IN} = U_T \ln(\frac{0.5V_s - V_{out1}}{0.5V_s + V_{out1}}) - 2(\frac{R_E}{R})V_{out1} \tag{2.30}$$

Recall that V_{IL}, V_{IH}, V_{OL}, and V_{OH} are defined as the input and output levels such that the transfer function's slope is unity. This can be solved for through differentiation of Equation 2.30.

$$\frac{d}{dV_{out1}}V_{IN} = U_T\frac{V_s}{V_{out1}^2 - 0.25V_s^2} - \frac{2R_E}{R} \tag{2.31}$$

Solving for $\frac{d}{dV_{out1}}V_{IN} = -1$, a solution for V_{out1} is obtained.

$$V_{out1} = \pm\frac{V_s}{2}\sqrt{1 + \frac{4}{V_s(\frac{2R_E}{RU_T} - \frac{1}{U_T})}} = \pm\frac{V_s}{2}X \tag{2.32}$$

As should be expected, the magnitudes of V_{OL} and V_{OH} are equal. Using the expression for V_{out1} in Equation 2.30, the solution for V_{IN} at the unity slope point can now be defined.

$$V_{IN} = U_T \ln(\frac{1 \pm X}{1 \mp X}) \pm R_E I_1 \tag{2.33}$$

Similarly to the output voltage, the input voltage also has two solutions with equivalent magnitudes. Due to this, it is clear that the distance between the input and output high levels will equal the distance between the input and output low levels. Therefore, the SNM can be found either way. In this case, the SNM will be expressed in Equation 2.34.

$$SNM = \frac{V_s}{2} X - U_T \ln(\frac{1 + X}{1 - X}) - R_E I_1 \tag{2.34}$$

From Equation 2.34, the SNM is notably dependent on the chosen voltage swing and the temperature. From a cursory analysis of Equation 2.34, a higher voltage swing and a lower temperature lend themselves to a more attractive SNM. It is a reasonable claim that lower temperatures can permit a smaller voltage swing for a given SNM required at higher temperatures. This fact will be utilized in a later section.

While SNM is a useful measurement, it does not account for the mechanisms through which noise can be attenuated by the ECL gate. For example, consider the differential pair in Figure 2.2. Equation 2.2 shows that the generation of the logic levels depend on the relative values of $V1$ and $V2$ to each other. If the designer has designed for a specific logic swing, V_s, then the maximum difference between $V1$ and $V2$ should be bounded by $\frac{V_s}{2}$ under ideal conditions.

Equation 2.8, however, shows that the output logic levels of the ECL inverter shown in Figure 2.2 have a dependence on the supply voltage. Now, assume a

perturbation of relative low frequency, v_{cc}, is applied to the supply rail.

$$V_{LO} = V_{CC} \pm v_{cc} - I_1 R - V_{BE3} \tag{2.35a}$$

$$V_{HI} = V_{CC} \pm v_{cc} - V_{BE3} \tag{2.35b}$$

where v_{cc} is a small noise signal in series with the supply voltage V_{CC}.

From the nature of the differential pair formed by $Q1$ and $Q2$, the common mode rejection can be leveraged to attenuate the effect of power supply noise on the circuit. If $V1$ and $V2$ are subject to the same power supply noise, as they will usually be, then the attenuation of the noise can be estimated from the common mode rejection, given by

$$\text{CMRR} = 20 \log_{10}(\frac{V_s}{2V_A}) \tag{2.36}$$

where V_A is the Early Voltage. It can be surmised from Equation 2.36 that a smaller logic swing is beneficial for attenuation of common mode noise, such as is the case for power supply noise. However, this is a blatant trade-off with noise margin. In most cases, though, it can be shown that the Early voltage is sufficient enough to produce a reasonable CMRR regardless of the voltage swing.

Chapter 3

Developing the Standard Cell Library

3.1 Design Considerations

A standard cell library is a fully characterized collection of cells that can be assembled robustly to design digital systems. These digital systems could be commprised of thousands of standard cells. Because of the number of cells being used, it is important to consider the following:

1. How much power should these standard cells consume?
2. At what frequency can these standard cells operate?
3. How reliable are these standard cells in their intended environment?
4. Are these cells configurable and scalable?

Chapter 2 covered the basics of ECL, which is the logic family of choice for standard cell design due to the HBT's positive response to the harsh environment of space. Equations for estimating the power consumption and the speed of a simple ECL inverter were also provided. Based on Equations 2.13 and 2.25, it is clear that an

increase in speed incurs a greater increase in static power consumption. This design will opt to prioritize power consumption over speed.

In terms of reliability, major concerns include TID tolerance and electrostatic discarge (ESD). To ensure the former, only devices that are capable of being used in high TID environments (5Mrad) are selected. Notable inclusions are the HBT, p-channel FET [4], and polysilicon resistors [5]. ESD protection, on the other hand, must be considered in circuit design and layout.

3.2 Developing the Standard Cell Template

3.2.1 Target Design

As mentioned in the previous section, standard cells are just building blocks of a more complex system. In many applications, thousands of standard cells are used in the realization of a VLSI circuit. Therefore, an emphasis on uniformity in design is only natural.

In Chapter 2, the principles of ECL were discussed in detail. These cells can require many different biasing conditions. The ECL inverter in Figure 2.2, for example, requires currents I_1 and I_2, and could potentially require a voltage reference for $V2$. If other standard cells were to deviate significantly from this design, then the amount of biasing cells required would grow as well. Therefore, for efficient library design, it is useful to define a template that will act as the basis for all of the standard cells.

Before defining the template, the specifications for the design must be set first. A good starting point is the logic voltage swing, denoted V_s. Recalling Equation 2.3, to steer 95% of current to either transistor of the differential pair, the voltage differential must be at least $3U_T$, or 75mV at room temperature. Referring back to Figure 2.1, if $V1$ is a square wave and $V2$ is a DC voltage, that suggests that $V1$ should oscillate between $V2 \pm 75mV$. This sets the minimum V_s to $150mV$ at room temperature.

Now comes the choice of supply voltage. The supply voltage is upper and lower bounded by two separate means. The upper bound of the supply voltage comes from the collector-emitter open base breakdown voltage of the HBTs, BV_{CEO}, which is 1.72V. The lower bound is a function of the worst case V_{BE}, which occurs at low temperature operation, V_s, and $V_{CE}(sat)$.

$$2V_{BE} + V_s + V_{CE}(sat) \leq V_{CC} \leq BV_{CEO} + V_{BE} \tag{3.1}$$

Using data from the technology provider and cryogenic modeling, it was determined that 2V was a sustainable supply voltage. The inverter in Figure 2.2 uses three current mirrors: two for the emitter followers, and one for the differential pair. To keep power low and the area overhead minimum, each current mirror is designed to draw 1μA. For three current drawing branches, this equates to a power consumption of 6μW per inverter. The choice of current also motivates the choice of resistor. To provide a bit of margin over the minimum V_s of 150mV, 200mV is the chosen signal swing, requiring a collector resistance of 200kΩ to generate the voltage drop.

Figure 3.1 shows the resulting design for the ECL inverter based on the criteria above. P-channel MOSFETs M1 and M2 take the place of resistors to minimize area, with gates biased in such a way that the desired resistance is roughly achieved. $Q5$, $Q6$, and $Q7$ are current mirrors that are intended to be biased by a reference circuit external to the logic gate, supplying around $1\mu A$.

Figure 3.1 also serves as the library template, a good choice as the inverter has the simplest design and subsequent circuit designs will not cause a deviation in the layout process. The usage of current mirrors and pFET loads will therefore be replicated through the entire standard cell library.

3.2.2 Application Reliability

As mentioned in the beginning of this chapter, the standard cells must be reliable in order to compose a library. Because the template serves as the starting blueprint

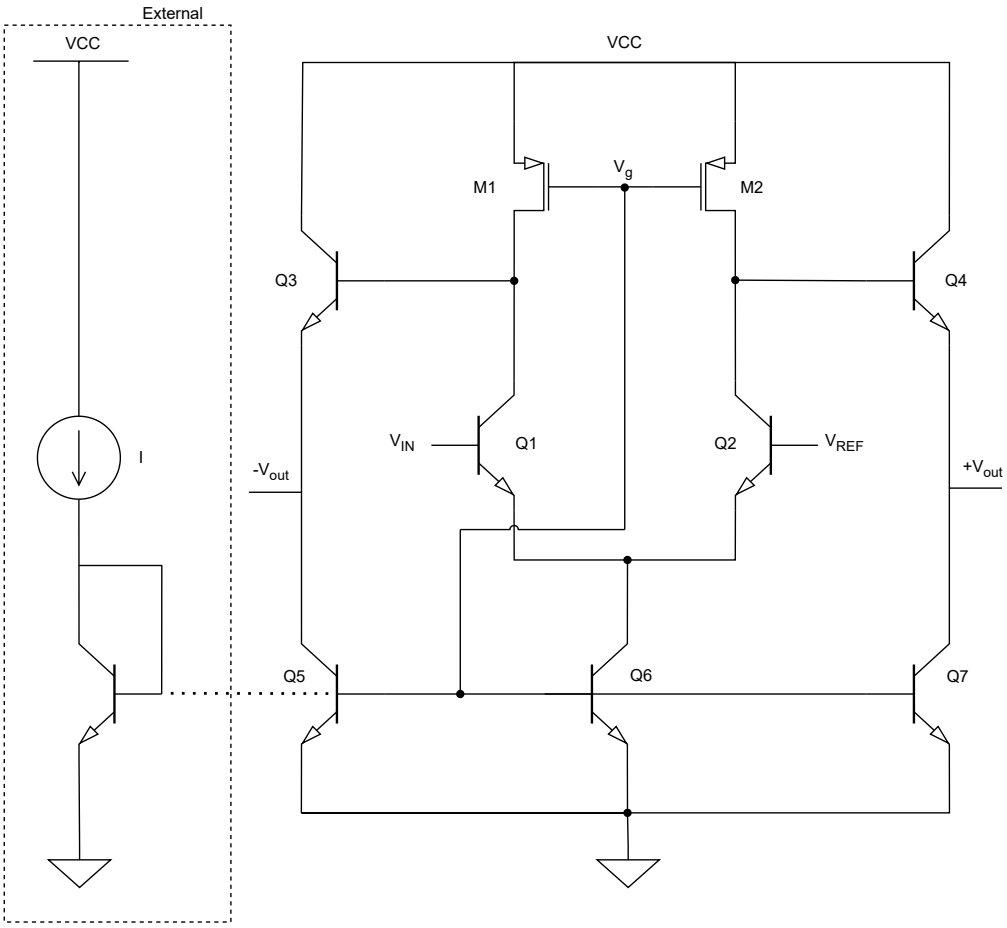


Figure 3.1: Proposed ECL Inverter (all npn-HBTs of 1μm x 0.1μm emitter area, all 1.2V PFETs – 0.36μm x 5μm channel area , I = 1μA)

for the standard cell library, it is paramount to address and resolve any reliability concern before using it as a design method.

There are three key area in which the template requires further investigation: temperature effects, ESD susceptance, and latch-up. Due to the nature of space, variance in temperature and the tendency for charge accumulation due to radiation must be accounted for. This section seeks to cover these topics.

In terms of temperature variation, there are a few key interactions to consider. Recall that Equation 2.8 provides the logic levels generated by a simple ECL inverter. While this expression might be sufficient in an isothermic environment, it is not sufficient for this application. Instead, a more general equation that considers temperature and better reflects Figure 3.1 will be referred to.

$$V_{LO} = V_{CC} - I_5(T)R_{ON}(T) - V_{BE}(T) \tag{3.2a}$$

$$V_{HI} = V_{CC} - V_{BE}(T) \tag{3.2b}$$

Equation 3.2 considers the temperature dependence of the ECL inverter's logic levels, where $I_5(T)$ represents the current through $Q6$ as a function of temperature and $R_{ON}(T)$ represents transistors M1 and M2's channel resistance as a function of temperature. Each of these terms shall be considered separately to qualify the general behavior of the ECL standard cells.

The HBTs used in the design have a well known temperature dependence in V_{BE}. For an HBT drawing a constant current, V_{BE} will increase as temperature decreases [6]. This behavior is also supported by the basic current transport equation, which is given by Equation 2.1. From this, it can be determined that the base-emitter voltage has a net negative temperature coefficient under the condition that constant current is supplied over all temperatures.

The p-channel FETs (pFETs) are operating in the linear region. Following from this, the channel resistance is given by

$$R_{ON} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - V_{TP})} \tag{3.3}$$

where μ_p is the p-type carrier mobility, V_{SG} is the source-gate voltage, and V_{TP} is the threshold voltage for the PFET. The inherent temperature dependence of the pFET manifests itself through the mobility μ_p and the threshold voltage V_{TP}. The threshold voltage tends to decrease as temperature increases, which on its own would cause a decrease in channel resistance. However, the carrier mobility tends to decrease with increasing temperature and causes a larger impact on drain current than the threshold voltage. It suffices to say that as temperature increases, channel resistance increases with it. Therefore, channel resistance has a net positive temperature coefficient [7]. However, this relationship may not hold true as technologies begin scaling below 65nm or as temperature scales low enough to permit carrier freeze-out.

However, due to the architecture of the template shown in Figure 3.1, the channel resistance R_{ON} also exhibits a temperature dependence due to V_{SG}, which can also be expressed as

$$V_{SG} = V_{CC} - V_{BE}(T) \tag{3.4}$$

Because V_{BE} grows with decreasing temperature if current is kept constant, V_{SG} must shrink with increasing temperature under the same conditions. This action acts as a counter balance to the inherent decrease of R_{ON} with temperature, since as V_{SG} decreases, channel resistance increases. This can be observed in Figure 3.2.

The current through $Q5$, denoted I_5, can also be temperature dependent. The choice of temperature dependence is up to the designer and the capabilities of the technology afforded by the application. In this case, the motivating factors would be that largely, as temperature decreases, the level shifting as a consequence of the emitter followers formed by $Q3$ and $Q4$ increases, while the signal swing decreases due to the decreasing R_{ON} of $M1$ and $M2$.

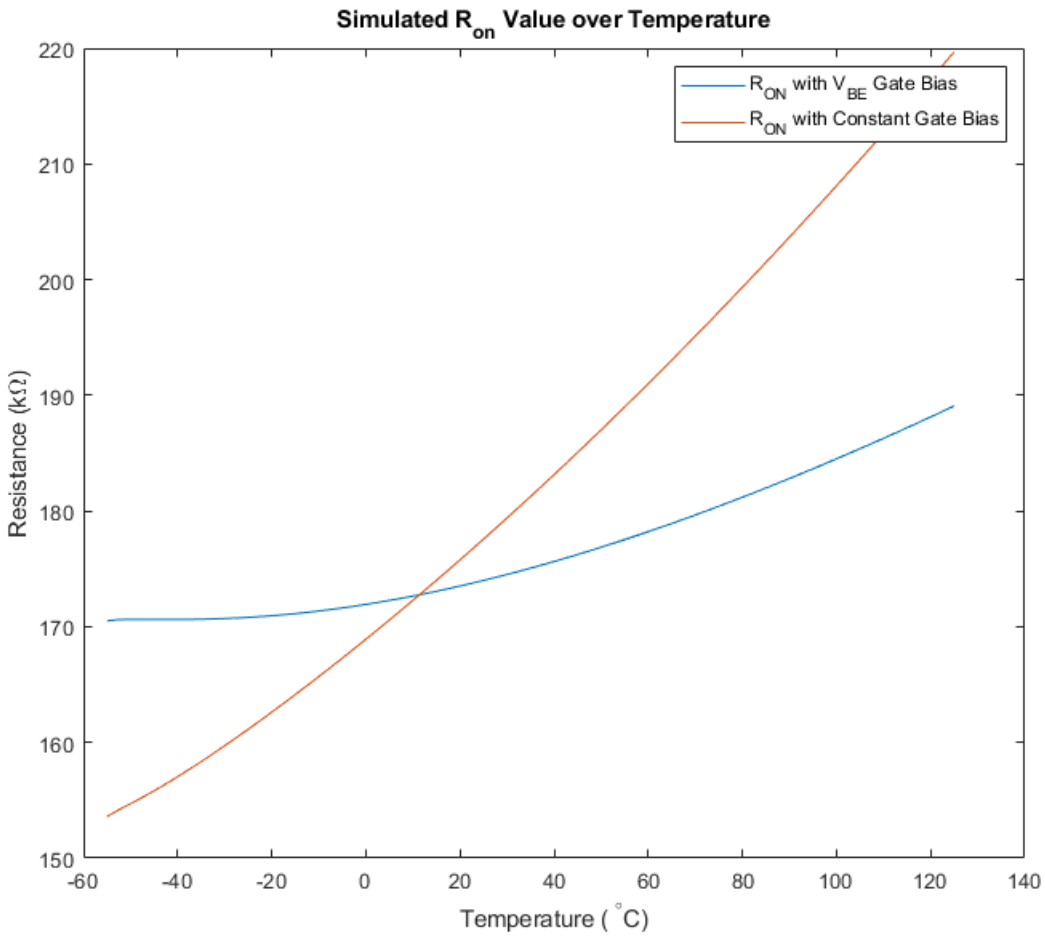


Figure 3.2: Comparison of R_{ON} with Fixed Gate Voltage to R_{ON} with V_{BE} Gate Voltage

However, the current I_5 is not the only design point that must account for the temperature. The reference voltage, V_{ref}, must properly set up the common mode level of the differential pair $Q1$ and $Q2$ as seen in Figure 3.1. If the temperature causes a change in the logic levels, the reference voltage must accurately reflect that in order to permit the current steering action of the differential pair. The design of a reference circuit for generating the the current and reference voltage will be explored in a later section.

Latchup is far more straightforward a problem to address. Both the SiGe HBTs and the silicon pFETs are generally susceptible to latch up. For the HBTs, the interaction of the n-type subcollector and the p-type substrate can cause latchup. For the PFETs, the interaction is through the p-type wells, the n-type body, and the p-type substrate.

Latch up problems are addressed through a mixture of device properties from the chosen technology and explicit design choices in layout. The deep trench isolation of the HBTs greatly inhibits latchup by preventing lateral current injection and reduction of lateral parasitics [8], making HBTs very resistant to latchup in this process. Guard rings are used to regulate the body potential of the pFET devices to minimize chance of latchup as well.

SiGe HBTs are also well known for their robustness towards ESD events [8], so no special techniques were needed to ensure reliability in the circuit level. For the pFETs, a second guard ring with a greater thickness was introduced. This thick guard ring provides a low impedance path to ground that serves to siphon any collection of charge that would otherwise damage the pFET.

3.2.3 Scalability

With the expectation that these standard cells must be automatically placed and routed for any VLSI design, it is up to the designer to allow the CAD tools as many degrees of freedom as possible while enabling the composition of a compact layout.

This must be demonstrated by the template before it can be used as the blueprint for the standard cell library.

A particularly important quantity is the standard cell height, which must be shared between all standard cells in the library. The cell height dictates the number of routing lanes that can be used to connect internal IO. Additionally, by maintaining a uniform standard cell height, the place and route algorithm is able to stack the cells atop each other and create rows of cells, which aids in keeping the layout compact.

Figure 3.4 shows the realization of the template shown in schematic in Figure 3.1. The key features of the cell are as follows:

- The midpoint of the VCC and GND traces set the y-axis boundaries for the cell.
- Metal layers M1 and M2 are the only routing metals used, with M1 used for horizontal routing and M2 for vertical routing.
- Two M1 traces below the VCC bus span the entire cell from border to border. These are used to bias the current mirrors and route the reference voltage.
- The HBTs and pFETs occupy their own hemisphere of the layout, with HBTs on the left vertically sharing deep trenches, and the pFETs sharing the same n-well in a double guard ring.

These features enable many degrees of freedom in terms of VLSI layout, when more than one cell needs to be placed and routed. For example, additional cells can be abbutted on the left and right sides of the cell in Figure 3.4, allowing them to share VCC, GND, V_{REF}, and current biasing with no additional routing. They can also be stacked above and below by simply flipping the cell orientation across the x-axis. Figure 3.4 shows an example layout of multiple cells.

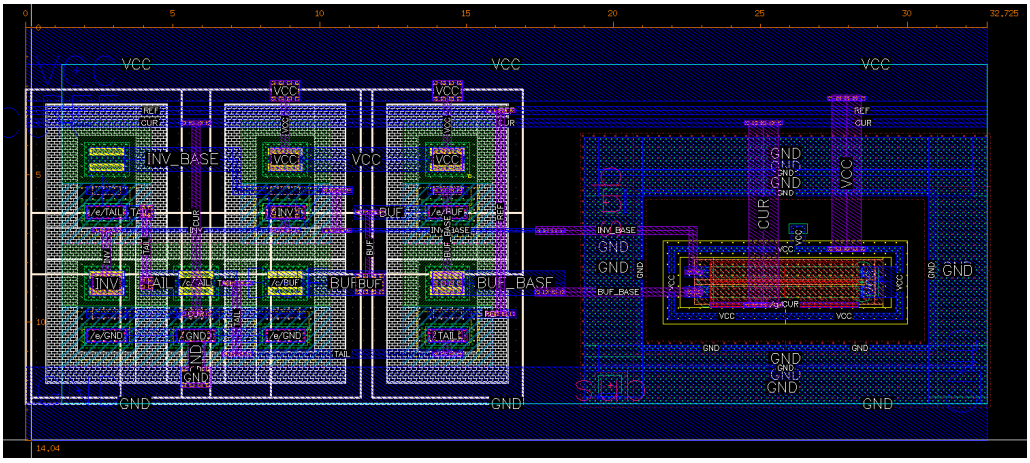


Figure 3.3: ECL Inverter/Template Layout, Area: 31.725µm × 11.54µm

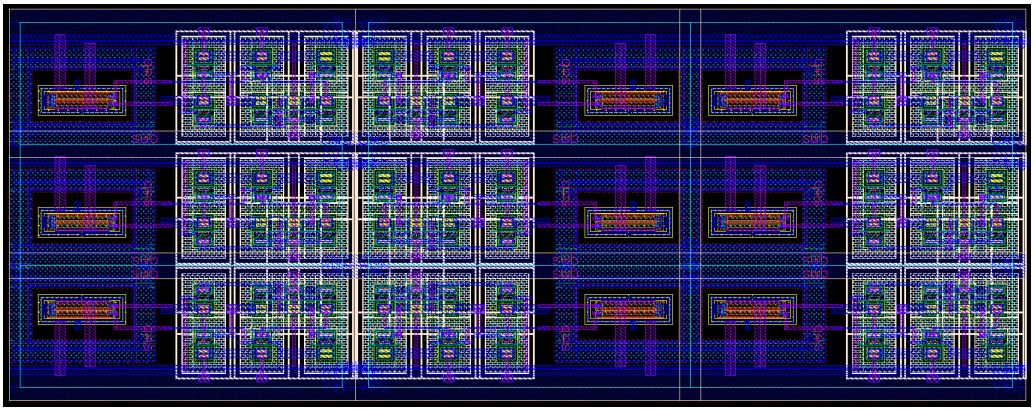


Figure 3.4: Example of Cell Placement Capabilities of Template

3.3 The "Starved" Standard Cell Library

The circuits discussed in this section form what will be referred to as a "starved library." This term indicates that these circuits complete the minimum set of cells that are required to synthesize any logic system.

As mentioned earlier, any standard cell library must include timing and power information. With this in mind, this section will also report this information for each cell with a fanout of ten gates over three corners: slow, typical, and fast. Each corner corresponds to a specific temperature, supply voltage, and process variation. The slow corner is defined by the hottest temperature, a 10% decrease in nominal supply voltage, and a -2σ skew in process variation, which yields under-performing transistors. The fast corner is defined by the coldest temperature, a 10% increase in nominal supply voltage, and a $+2\sigma$ skew in process variation, which yields better performing transistors. In addition to process corners, each cell will be tested with parasitics extracted from layout.

Specific metrics of interest include the following:

- Rise Time (10% to 90% of full logic range on rising transition)
- Fall Time (90% to 10% of full logic range on falling transition)
- Propagation Delay (measured from midpoint of input transition to midpoint of output transition)
- Static Power Consumption

Due to the differential nature of ECL, timing analysis will include both the inverting (-) and the non-inverting (+) outputs.

Note that simulation results will view military specified temperature range rather than cryogenic performance due to the completeness of the modeling for these conditions. Additionally, all simulated cells will be biased by a proportional-to-absolute-temperature (PTAT) current reference, which is also responsible for

generating the voltage reference. This PTAT reference will be covered later in this section.

3.3.1 ECL Inverter

The ECL inverter was discussed in the previous section and is shown in Figure 3.1. Due to its fully differential nature, the inverter can also double as a buffer. The input/output characteristics of the ECL inverter are shown in Figure 3.5.

Furthermore, the inverter is a unique circuit in the standard cell library in that it does not require a reference voltage for operation, unlike any NOR based logic. Because all ECL gates have fully differential outputs, the inverter can simply take both outputs of an ECL gate for a fully differential input. This has the added benefit of symmetry, since both sides of the differential pair see a signal of the same magnitude and frequency. Additionally, recall that a voltage differential of $3U_T$ is preferred for strong current steering. Since the voltage differential is not only achieved faster but also surpassed, this affords more noise margin for the inverter.

Table 3.1 below compares the calculated values of important metrics such as power consumption, propagation delay, and noise margin for the ECL inverter with simulated values, all at different operating corners. The inverter in question is being biased by a PTAT current source, whose topology and behavior will be covered in a later section. Chapter 2 provides the equations used to yield the calculated values in the table below. Note that the equations make no distinction between neither inverting nor non-inverting outputs due to the assumed symmetry of the circuit. However, due to layout parasitics and asymmetry in input signaling, the simulated values will show results for both outputs. Calculated values are obtained by extracting device information from the PDK and fitting that data over the corners defined in the table. Additionally, the calculations also use a PTAT current source, which is derived from the equation used to design the reference circuit shown later in this document (3.3.4).

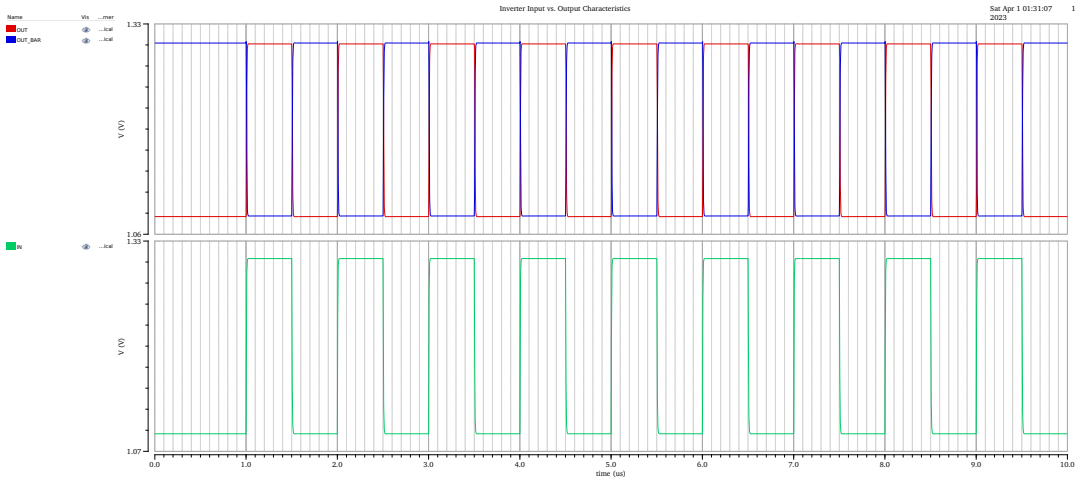


Figure 3.5: ECL Inverter with Fanout of 10

Table 3.1: Simulated Performance Summary of ECL Inverter with Fanout of 10

ECL Inverter Post-Layout Performance over Corners						
Type	Simulation			Calculation		
Design Parameters	Slow (-,+)	Typical (-,+)	Fast (-,+)	Slow	Typical	Fast
VCC (V)	1.8	2	2.2	1.8	2	2.2
Temp (C)	125	27	-55	125	27	-55
Power Consumption (µW)	9.113	7.87	6.30	8.76	7.28	5.86
Voltage Swing (mV)	486.9, 529.5	225.9, 253.1	125.8, 125.3	375.9	230.0	138.8
Rise Time (ns)	14.25, 16.53	12.03, 8.63	9.14, 6.69	–	–	–
Fall Time (ns)	15.82, 17.11	6.76, 11.99	4.36, 6.52	–	–	–
Propagation Delay (ns)	10.42, 11.34	6.04, 7.23	4.26, 4.16	7.97	6.58	5.23
SNM (mV)	102	34.2	10.4	74.9	36.2	16

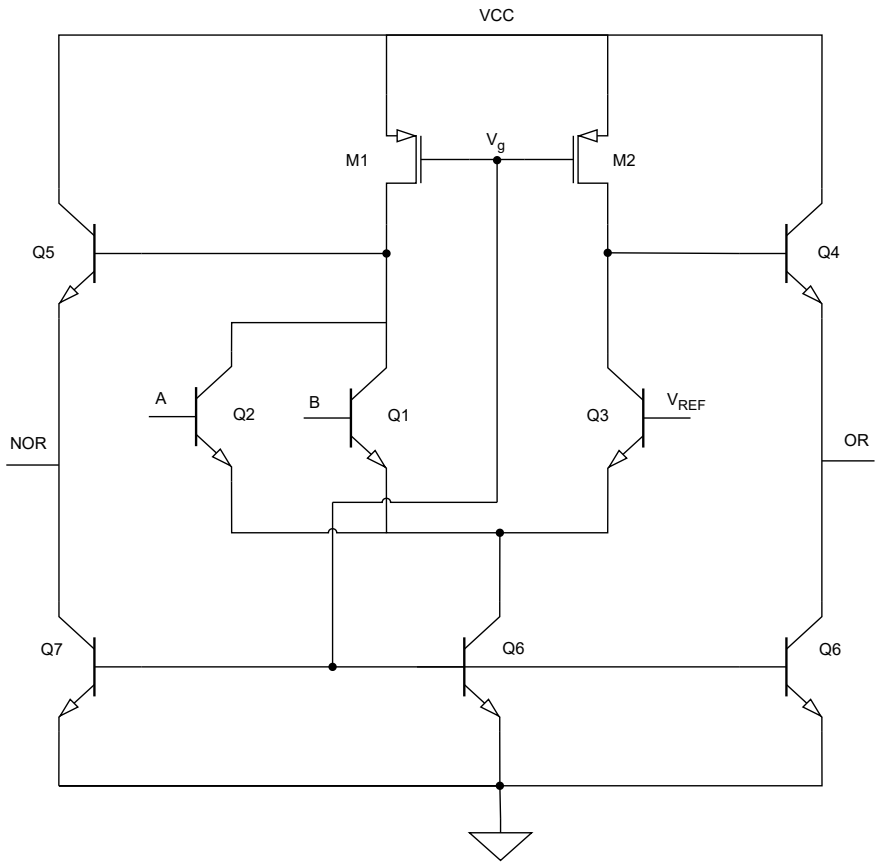


Figure 3.6: ECL OR Gate (all npn-HBTs of 1μm x 0.1μm emitter area, all 1.2V PFETs – 0.36μm x 5μm channel area , I = 1μA)

3.3.2 ECL OR Gate

Figure 3.6 shows the OR gate implemented in ECL. By connecting a second HBT's collector and emitter with the input transistor $Q1$'s collector and emitter, current will be steered to the resistor R_1 as long as either V_A or V_B are sufficiently larger than the voltage on $Q3$'s base. For a three input OR gate, connecting a third HBT's collector and emitter is sufficient. It's important to mention that the OR gate requires the usage of a reference voltage, unlike the inverter which has the option to forego a reference voltage, due to the unpredictability of the inputs (as opposed to an inverter, which can easily utilize both the input signal and the input's inverted signal as inputs). This suggests a longer propagation delay than the inverter with differential inputs because of the additional time it takes to achieve the same voltage differential between inputs.

Figure 3.7 shows the transient response of the ECL OR gate. Note that when both inputs are high, the non-inverting output sees an increased output voltage relative to when only one of the transistors is high. Similarly, the inverting output yields a decreased output voltage in this case. This can be explained through the use of an alteration to Equation 2.3. For simplicity, consider the OR gate shown in Figure 3.6. For this analysis, assume that $V_A = V_B$. Under this assumption, $Q1$ and $Q2$ can be considered as parallel transistors. With this consideration in mind, transistors $Q1$ and $Q2$ can be lumped together into a single HBT with double the emitter area of the transistors. The current steering equation given by Equation 2.3 can then be modified such that it considers the difference in emitter area on either side of the differential pair, yielding

$$\frac{I_{C1}}{I_{C2}} = n \times \exp\left(\frac{V_A - V_B}{U_T}\right) \tag{3.5}$$

where n is the ratio of the emitter area of the parallel combination of $Q1$ and $Q2$ with respect to $Q3$. What this demonstrates is that the current steering of the differential pair is skewed unevenly towards the higher emitter area transistor, allowing it to draw more current than usual. This condition in which $Q1$ and $Q2$ are in parallel

indeed occurs when both inputs are high, which justifies the output behavior in Figure 3.7. This can also be used to bound the number of HBTs that the designer connects together in the same manner as $Q1$ and $Q2$. A potential work around to this imbalance of emitter areas is to scale the opposing transistor in the differential pair larger as to, on average, cause less variation in the output level with input levels.

The simulated performance summary of the ECL OR gate is shown below.

3.3.3 ECL D Flip Flop with Set and Reset

In conventional ECL circuits, a D Flip Flop can be implemented by stacking differential pairs. Doing so allows the designer to effectively enable a specific differential pair based on the state of an input to the lower differential pair. For this low power standard cell library, the required headroom imposed by the HBT makes implementing this design at a 2V supply problematic. Instead, three-input OR gates are used to create latches that can be set and reset.

Figure 3.8 shows the implementation of the ECL three-input NOR gate in the D Flip Flop. For compactness, Figure 3.8 does not display the differential outputs of each NOR gate, sans the rightmost two. This D Flip Flop is a positive edge triggered flip flop, but the input signal is $\overline{CLK}$ due to the NOR logic implementation. In initial design and tapeout, the D Flip Flop's outputs Q and $\overline{Q}$ are part of the internal feedback loop that enables latching. This is undesirable since the effect of loading will also be seen in feedback. Instead of this, the circuit should have utilized the outputs not connected to the feedback loop, which are afforded by the fully differential outputs of the NOR gates.

Figure 3.9 shows the operation of the D Flip Flop while set and reset are disabled. The low logic level instability is due primarily to the fast switching speed of the clock, which briefly interrupts the current steering. Table 3.3 shows the simulated performance of the flip flop over corners.

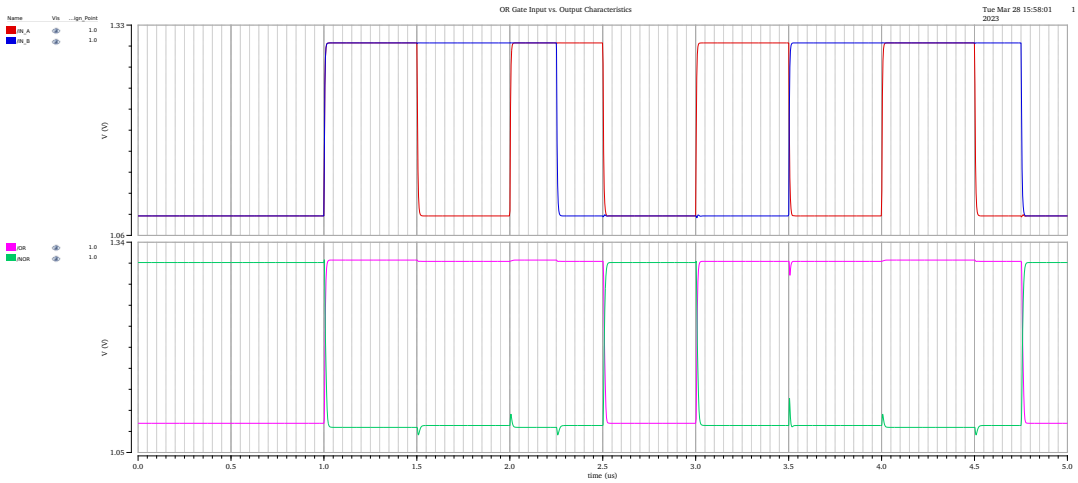


Figure 3.7: ECL OR simulation with Fanout of 10

Table 3.2: Simulated Performance Summary of ECL OR Gate with Fanout of 10

ECL OR Gate Post-Layout Performance over Corners			
Design Parameters	Slow (-,+)	Typical (-,+)	Fast (-,+)
VCC (V)	1.8V	2V	2.2V
Temp (C)	125	27	-55
Power Consumption (µW)	9.25	7.89	6.28
Voltage Swing (mV)	516.7, 468.1	236.3, 220.1	115.5, 109.7
Rise Time (ns)	17.56, 10.79	11.26, 7.36	7.96, 5.42
Fall Time (ns)	27.54, 21.32	13.59, 11.66	8.61, 7.72
Propagation Delay A (ns)	8.67, 7.56	4.99, 4.48	3.51, 3.22
Propagation Delay B (ns)	8.67, 7.56	4.99, 4.47	3.51, 3.22

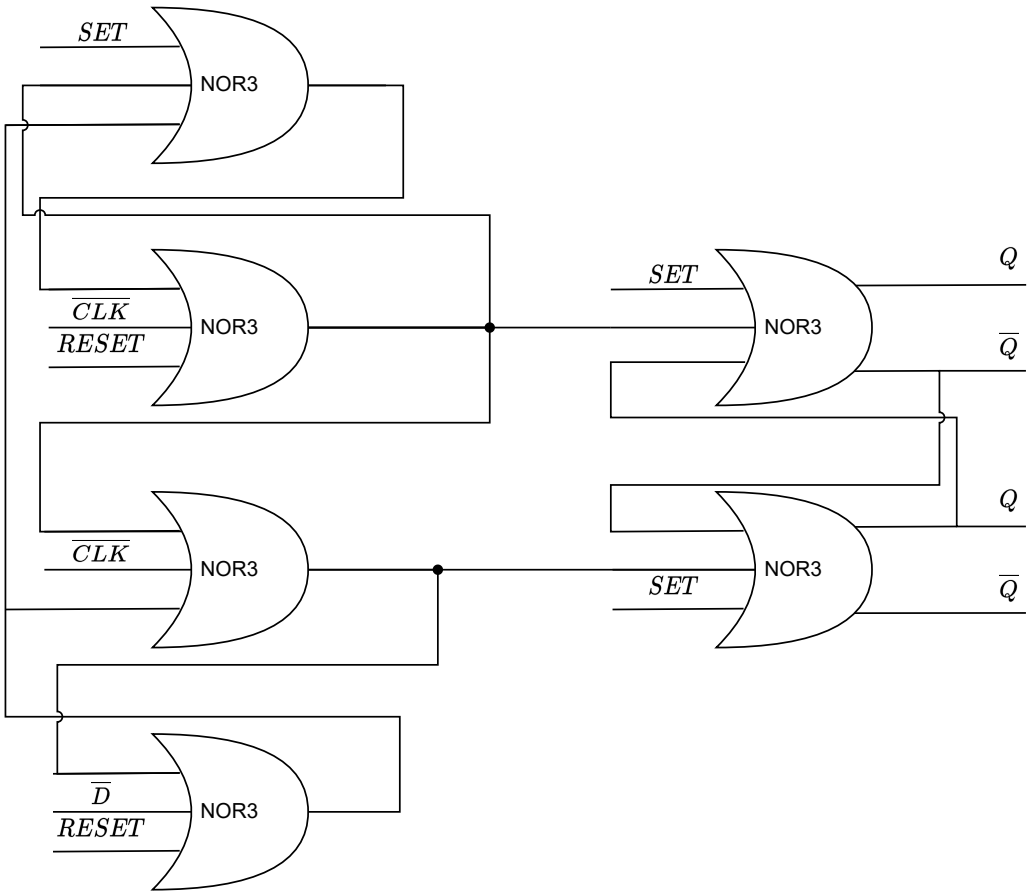


Figure 3.8: NOR Implemention of D Flip Flop with Set and Reset (simplified)

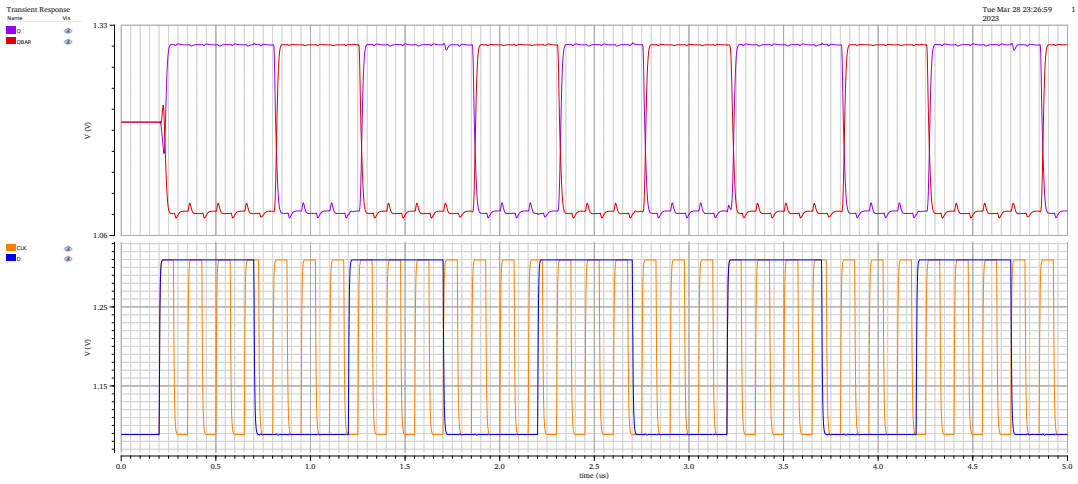


Figure 3.9: Simulated DFFSR Transient Response

Table 3.3: Simulated Performance Summary of ECL DFFSR with Fanout of 10

ECL DFFSR Post-Layout Performance over Corners			
Design Parameters	Slow (-,+)	Typical (-,+)	Fast (-,+)
VCC (V)	1.8V	2V	2.2V
Temp (C)	125	27	-55
Power Consumption (µW)	53.72	47	37.58
Voltage Swing (mV)	499.7, 498.6	226, 227.1	101.7, 103.6
Rise Time (ns)	24.59, 24.57	16.94, 17.51	14.26, 14.32
Fall Time (ns)	39.32, 38.70	21.68, 20.02	13.94, 14.16
Propagation Delay CLK (ns)	27.54, 27.51	16.64, 16.65	11.92, 11.96
Propagation Delay SET (ns)	16.41, 30.33	8.12, 13.69	5.42, 9.31
Propagation Delay RESET (ns)	20.95, 16.17	13.58, 8.32	8.97, 5.42

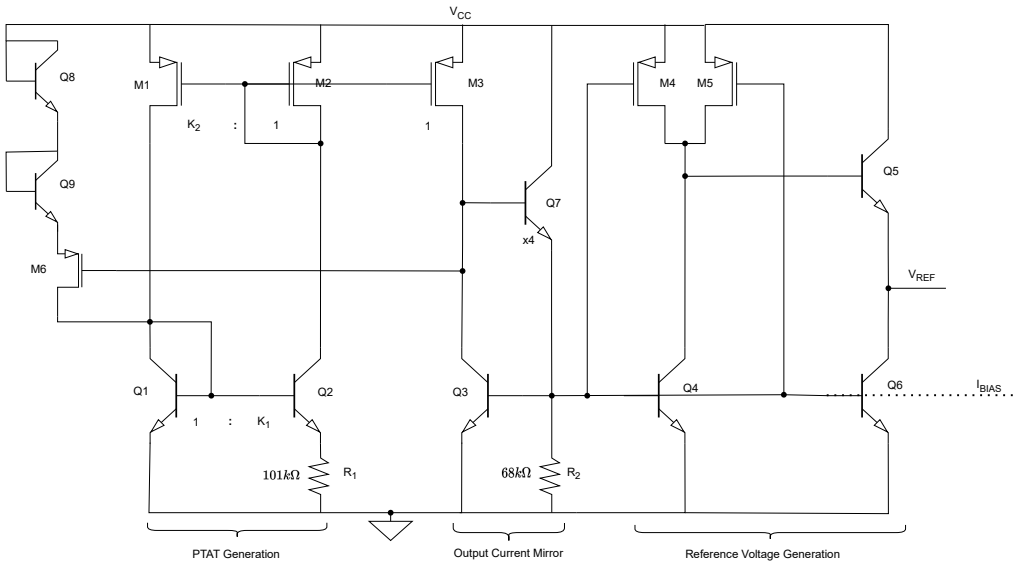


Figure 3.10: 2V ECL Reference Circuit (all npn-HBTs - 1μm x 0.1μm emitter area unless listed otherwise, $M4$ and $M5$ – 0.36μm x 5μm channel area, $M1$ – 2μm x 1μm channel area, $K_1 = 6$, $K_2 = 20$)

3.3.4 Reference Circuit

The ECL Reference circuit is shown in Figure 3.10. The purpose of the ECL reference circuit is twofold. The first is to provide a current bias to all ECL logic cells in the library. The second is to generate a corresponding reference voltage that sits at the midpoint with respect to both the high and low logic levels.

The current is provided by the PTAT portion of the circuit, which resembles a CMOS beta multiplier circuit. To get an understanding of how this portion of the circuit produces a PTAT voltage, consider the loop created by $Q1$, $Q2$, and R_1, which yields

$$I_2 = \frac{U_T}{R_1} \ln\left(\frac{K_1 I_1}{I_2}\right) \tag{3.6}$$

where I_2 is taken to be the current through $Q2$, and I_1 is taken to be the current through $Q1$. The current mirror created by $M1$ and $M2$ enforce that I_1 is K_2 times larger than I_2. Substituting for this in Equation 3.6, the current is shown to be

$$I_2 = \frac{U_T}{R_1} \ln\left(K_2 K_1\right) \tag{3.7}$$

Equation 3.7 shows that I_2 has a dependency on the thermal voltage whose magnitude is set by the choice of current mirror ratios between $M1$ and $M2$ (K_2) and between $Q1$ and $Q2$ (K_1) respectively, as well as the size of R_1. Figure 3.11 shows the agreement between Equation 3.7 and the simulation of the reference circuits output current.

However, upon inspection, the PTAT circuit in Figure 3.10 has a positive feedback loop created by $Q2$ and $M1$. In order for this circuit to be stable, the loop gain must be less than unity. A brief analysis of this loop shows that the loop gain, denoted by G, is given by

$$G \approx \frac{1}{1 + g_{m4} R_1} = \frac{1}{1 + \ln(K_1 K_2)} \tag{3.8}$$

From Equation 3.8, the loop gain is less than unity by choice of K_1 and K_2 and therefore has a stable state when $M1$ and $M2$ are in saturation and when $Q1$ and

$Q2$ are in forward active operation. For $K_1 = 6$ and $K_2 = 20$, the loop gain is calculated to be -15.25dB at DC. Figure 3.12 shows the loop gain of the PTAT's positive feedback loop relative to output current. At DC, the loop gain is -15.98dB, showing close agreement to the calculated value.

Now that the circuit has been deemed stable, it is important to be sure that the operation of the reference circuit lands in the stable state intended by the designer. This is beacuase there exists a stable state in which all transistors are non-conducting. In order to prevent the PTAT circuit from settling in this state, $Q8$, $Q9$, and $M6$ are implemented to form a start up circuit. $Q8$ and $Q9$ are used to level shift the supply voltage down to clamp the source-gate voltage of $M6$. The gate of $M6$ is attached to the base of $Q7$, which forms the start of a base current compensated current mirror along with $Q3$. If current is not conducting, V_{BE3} must be zero, which by consequence forces V_{BE7} to be zero as well. $M6$ will begin conducting if this is the case, which will in turn pull up the base of $Q1$ and $Q2$. Once $Q1$ and $Q2$ stabilize at a positive collector voltage, the V_{SG} of $M6$ will have been clamped to a voltage below the threshold voltage, if not ground.

Figure 3.13 shows the startup behavior of the circuit as a function of time. Specifically, this illustrates the transition from the unwanted stable state to the desired stable state.

The current generated by the PTAT portion of the circuit in Figure 3.10 is then mirrored by $M3$. Since all of the logic gates in this standard cell library use HBT current mirrors, the current provided by $M3$ is then mirrored again by the current mirror created $Q3$, $Q7$, and $R2$. While $Q3$ is the actual current mirror, $Q7$ and $R2$ provide base current compensation for all subsequent current mirrors, providing high fanout capability.

Subsequent current mirrors $Q4$ and $Q6$ are used to generate the reference voltage. The idea is that the reference voltage is the midpoint between the high and low logic

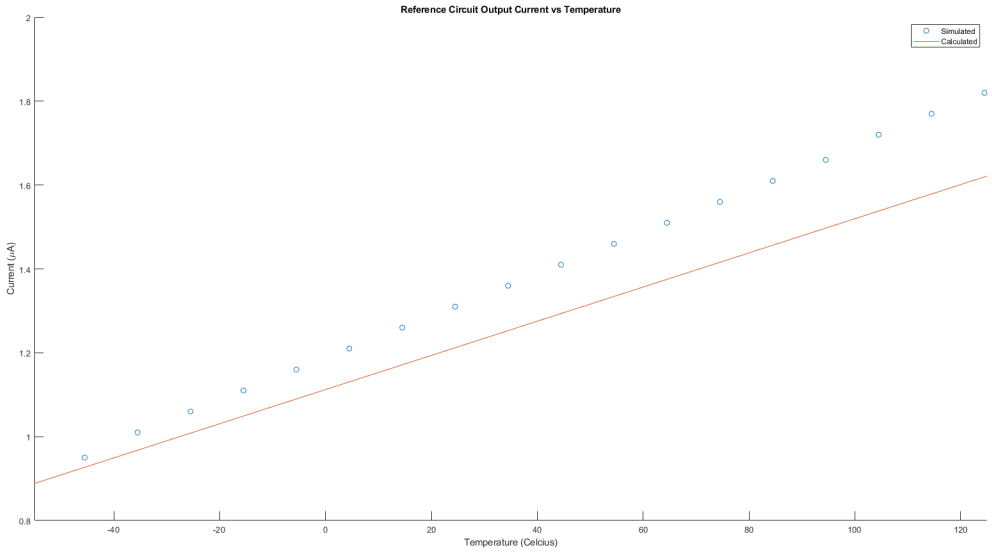


Figure 3.11: Reference Current Temperature Profile

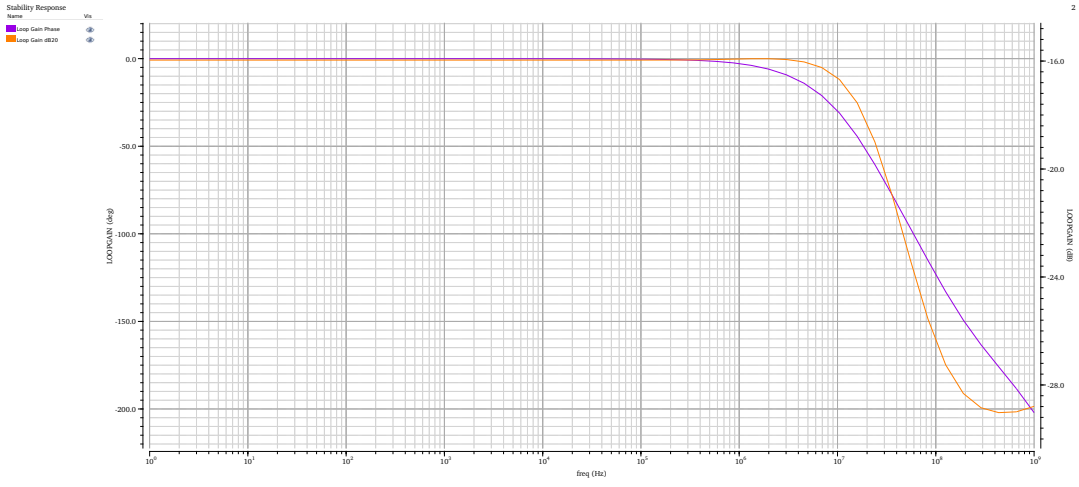


Figure 3.12: Reference Current Stability

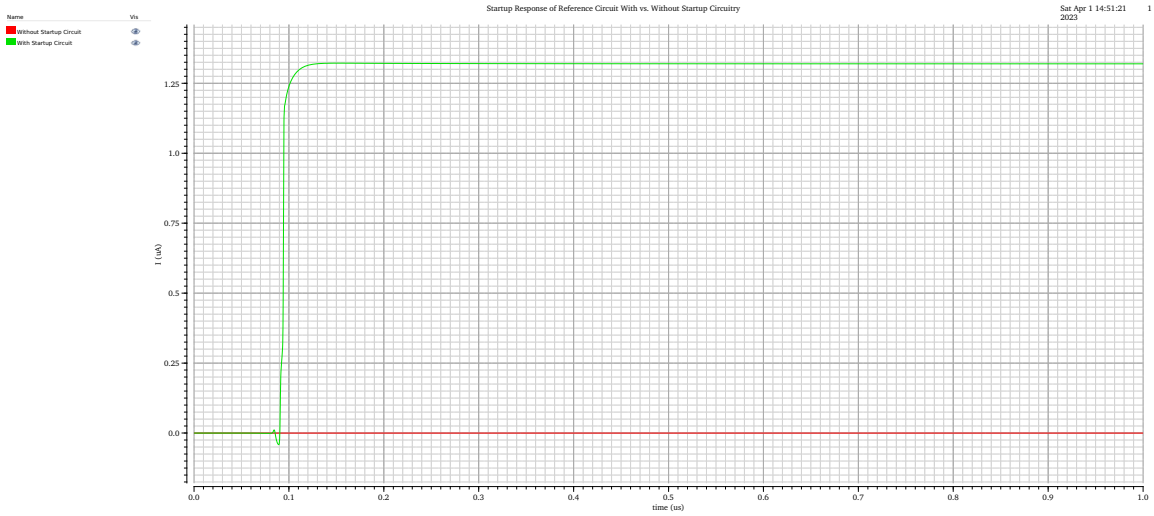


Figure 3.13: Startup Response With and Without the Startup Circuit

level voltages defined in Equation 2.8, given by

$$V_{REF} = V_{CC} - \frac{IR_{ON}}{2} - V_{BE} \tag{3.9}$$

Recall that I is the current sink of the differential pair and R_{ON} is the effective resistance of the pMOS transistors acting as loads for the ECL circuits. To produce the reference voltage, the chosen methodology is to replicate the architecture of the ECL inverter, which is the mechanism through which the reference voltage is generated in the first place. To achieve the $\frac{IR_{ON}}{2}$ term from Equation 3.9, $M4$ and $M5$ are sized and biased identically to the pFETs used in the library's logic gates and placed in parallel. Since the current provided by $Q4$ is the same current that will be provided by the logic cells, this accurately creates an identical voltage drop comprising the first two terms of Equation 3.9. Finally, $Q5$ and $Q6$ form an emitter follower that introduces the V_{BE} shift required by Equation 3.9. This also has the added benefit of introducing a low impedance node which is capable of driving multiple gates.

Figure 3.14 shows the reference voltage level generated by the ECL reference circuit relative to the output of an ECL logic gate at both slow and fast corners, defined in previous measurements. As designed, the reference voltage level lies between the logic high and logic low levels and tends to stay near the center.

3.3.5 Design Summary

In this section, the design and simulation verification methods were shown. The design of the cells follow a common template, and simulations consider three process corners relative to military specification for completeness. The designs function as expected, and the behavior is decently modeled by the simple equations in Chapter 2. However, a shortcoming of these simulations is the inability to predict cold behavior accurately for temperatures below -55°C. Predictions of cold behavior mainly rely

on analyzing trends from 125°C to -55°C. The next section will overview the testing process for these cells, which were cooled down to -165°C.

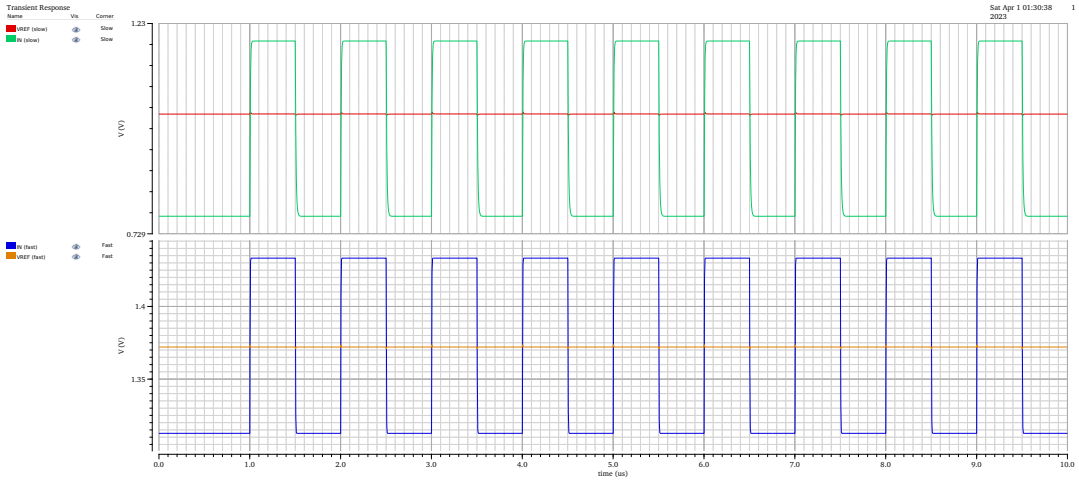


Figure 3.14: Reference Voltage vs. ECL Output

Chapter 4

Results

4.1 Introduction

In this chapter, the results of cold testing will be shown for the ECL circuits introduced in the previous chapter. Results for power and biasing information will be specifically shown in this chapter. For a more thorough look at the results, please see the Appendix.

4.2 Testing Methodology

In order to test the chip, a test board was fabricated to manage DC biasing and signal delivery. An AC coupling capacitor is used to couple the input square wave to a DC common mode level. The common mode level is generated by a resistive voltage divider and is applied to the bases of the input HBT differential pair. Note that these design decisions have ramifications on the input waveform, producing observable tilt due to the time constant created by the input network. The test board is shown in Figure

The goals of these tests are to determine the operation of the ECL inverter, or gate, D flip flip, and reference circuit at cryogenic temperatures. In order to manage this, the fabricated circuits and the test board were placed in the Sun Chamber.

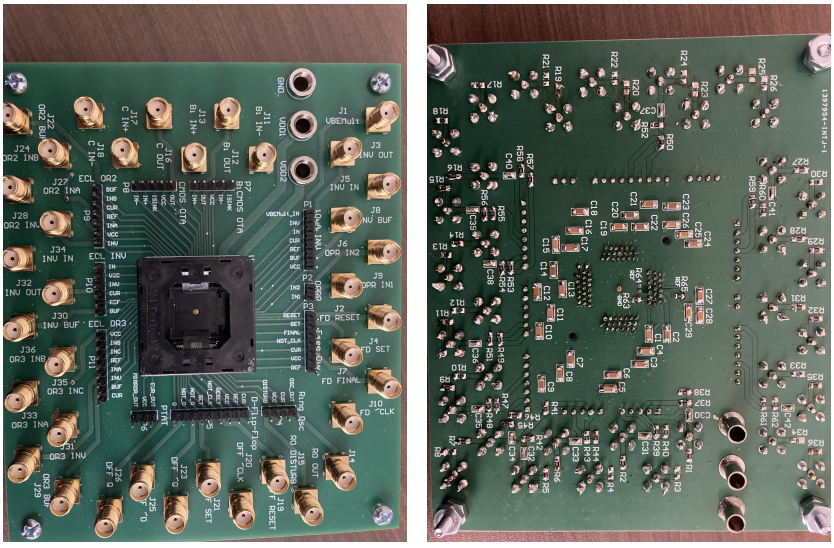


Figure 4.1: (Left) Top View of Test Board, (Right) Bottom View of Test Board

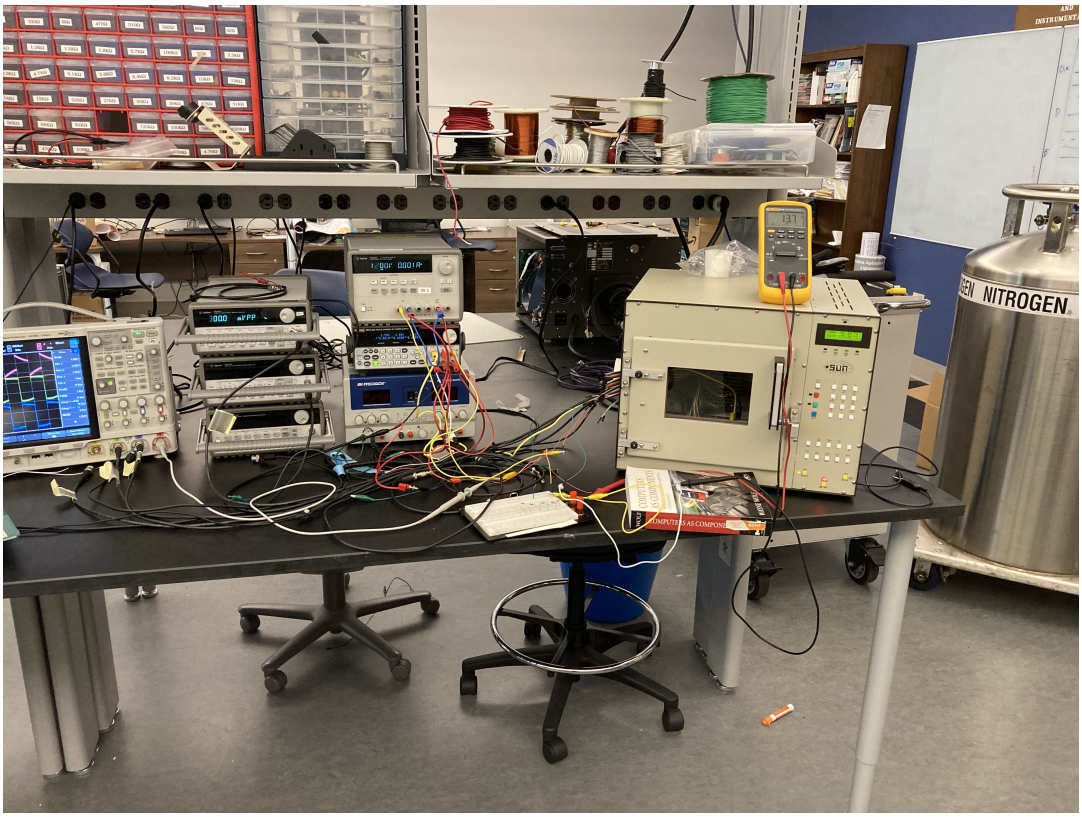


Figure 4.2: Test Setup with Oscilloscope (far left), function generators (mid left), DC supplies (mid right), and cold chamber (far right)

First, heat was applied until reaching 60°C so that any moisture in the chamber will evaporate. Then, after cooling back down to room temperature, liquid nitrogen is pumped into the chamber, allowing the chamber to reach down to about -160°C. Data was recorded within this range of -160°C to 60°C in steps of 20°C. The rest of this chapter will be dedicated to showing the results of timing, power, and biasing characteristics.

Figure 4.2 shows the setup used to test the chip over temperature. One foot coaxial cables with SMA terminations are used to route signals in and out of the chamber, but inadvertantly introduces a load capacitance of 30pF to the circuit. Ribbon cables are used to DC bias the circuitry. Output drivers for these cables and pads were not included on this chip in order to have maximum visibility of DC biasing information, primarily being the output common mode level. However, the downside of this is that propagation delay and rise/fall times will be far slower than expected.

The cells were biased using a built-in current mirror for each individual cell as seen in Figure 4.3. The resistor is a PTAT, high sheet resistance polysilicon resistor and the HBT is of the same emitter area as the current mirror transistors $Q5$, $Q6$, and $Q7$ shown in Figure 3.1. V_{BIAS} is used to change the current that will be mirrored to each branch of the ECL circuit and is kept separate from V_{CC} as to not contribute to the nominal circuit power consumption. This voltage will be kept constant over all temperature.

4.3 Test Results

The inverter is perhaps the performance benchmark for the standard cell library, and its results will be discussed first. The inverter is biased at 2V supply voltage, a V_{REF} of 1V, and a V_{BIAS} that is set such that the signal swing at room temperature will be around 200mV. This is to facilitate an accurate comparison to simulated and calculated data. Figure **??** shows the room temperature behavior of the ECL inverter.

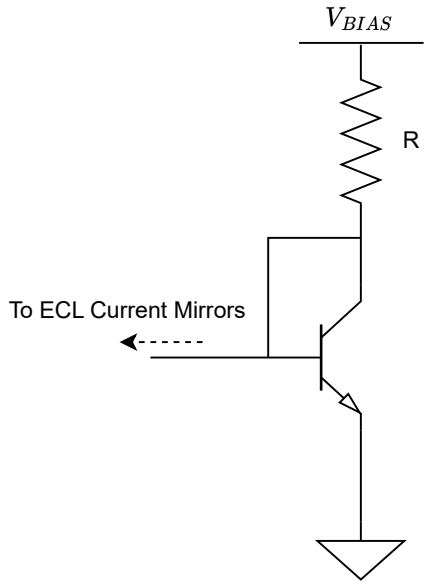


Figure 4.3: Current Biasing Method for Testing

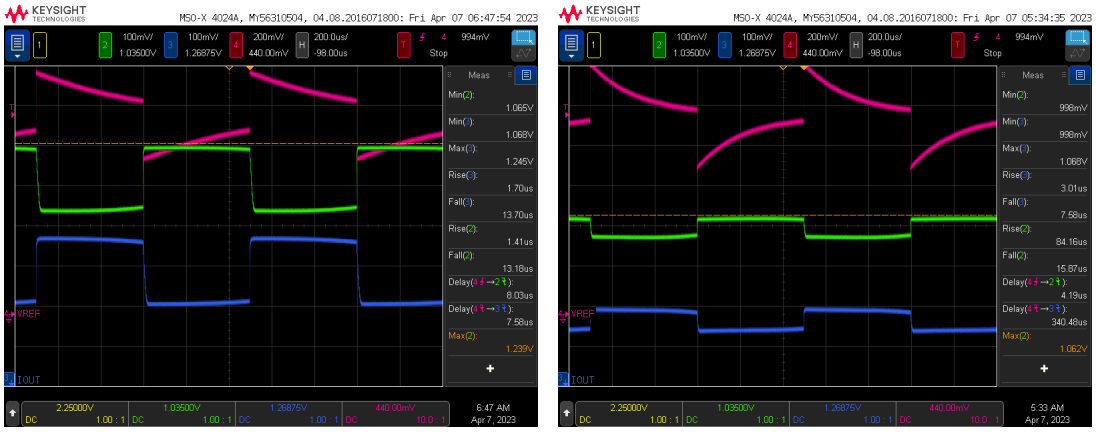


Figure 4.4: (Left) Inverter Behavior at Room Temp (RT), (Right) and at -160°C

Figure 4.4 shows the inverter's outputs both at room temperature and at -160°C. The behavior is within expectations. Because the current is PTAT as well as R_{ON}, the voltage swing is also PTAT. Additionally, the common mode level also decreases for the same reasons in addition to the increasing V_{BE}, which is the amount the output is level shifted downwards. Figures 4.5 and 4.6 collectively show the measured data for the ECL inverter. The common mode level over temperature does indeed decrease in a shape dictated by the V_{BE} temperature shift, which is logarithmic, and the temperature profiles of the current and R_{ON}. It also seems that the rate at which the common mode level decreases is increasing at cold, which could cause trouble if it leaves the input common mode range of the differential input pair of the inverter. Figure 4.5 also shows the output swing of the inverter. It also includes the theoretical minimum for 95% to 5% current steering. If the swing crosses this threshold, the effective resolution of the inverter will begin to decrease as the current steering becomes weaker.

Figure 4.6 shows both the power consumption and propagation delay as a function of temperature. The power consumption goes down with temperature thanks to the current profile, reaching almost 2µW of power consumption from about 6µW at room temperature. Similarly, the propagation delay improves with lower temperature, although how much of this is a function of the HBT's temperature behavior or the decreasing voltage swing of the output is unclear. The propagation delay, however, is given in µs rather than ns like in simulation due to being loaded with about 1000 times more capacitance than in simulation. While it is tempting to try and extrapolate a realistic rise and fall time from this fact, the trustworthiness of such data is unknown.

Figure 4.7 shows the nominal behavior of the DFFSR at room temperature and -160°C, while Figure 4.8 shows the behavior of set and reset at the same temperature conditions. The DFFSR follows the same trends as the inverter, which can be seen from Figures 4.9 and 4.10. Namely, the common mode level falls and swing fall with temperature, as does the power consumption and propagation delay. However, the DFFSR has some noticeable deviations from the ideal. Firstly, the common mode

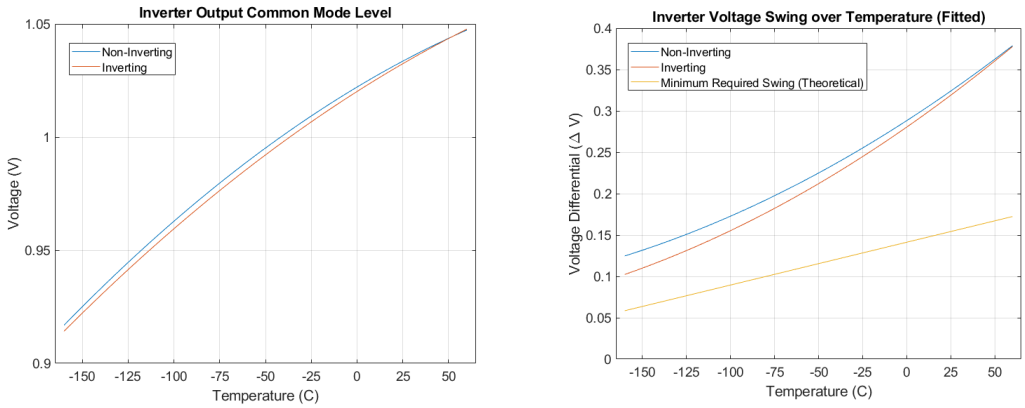


Figure 4.5: (Left) Output Common Mode Level of Inverter, (Right) Inverter Output Swing

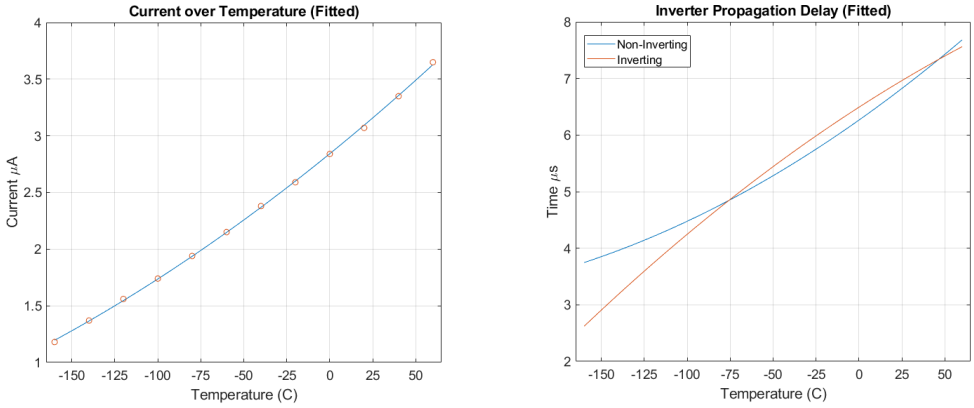


Figure 4.6: (Left) Inverter Total Power Consumption, (Right) Inverter Propagation Delay



Figure 4.7: (Left) DFFSR behavior at RT, (Right) and at -160°C



Figure 4.8: (Left) Set and Reset Test at RT, (Right) and at -160°C

level of both outputs are separated by around 50mV. While this could be corrected at room temperaure by connecting the outputs to an inverter, at cold, the swing might be too low to perform correction. The reason for the 50mV separation could be in part due to the unbalanced current steering of the three-input NOR gates used to compose the DFFSR.

The swing of the DFFSR is much larger than the inverter, but that is because the current was increased by 50% to keep the circuit in proper operation. This is because the DFFSR is composed of multiple gates, some of which are connected in series. Therefore, care has to be taken to make sure that the reference voltage is in the middle of all transitioning signals. It was useful to increase the current so as to increase the swing, increasing the probability that the applied reference voltage would fall somewhere in between logic "HI" and logic "LO." Power consumption for the DFFSR is as expected for a six gate circuit, but the propagation delay experiences the same imbalance that the common mode output level does and for the same reason as well. The propagation delay is also longer an average than the inverter due to the coaxial cables load capacitance being seen by the latch's feedback network. In the future, there should be isolation between the feedback node and the output load to prevent this situation.

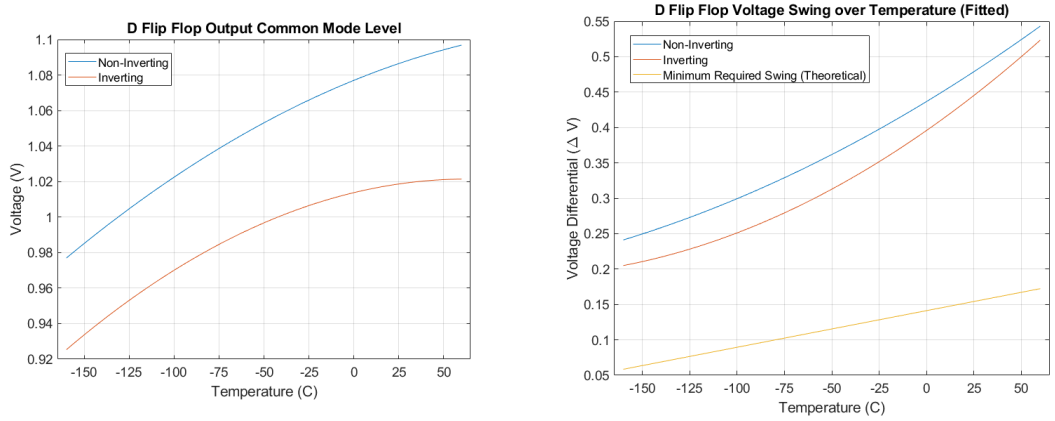


Figure 4.9: (Left) Output Common Mode Level of DFFSR, (Right) DFFSR Output Swing

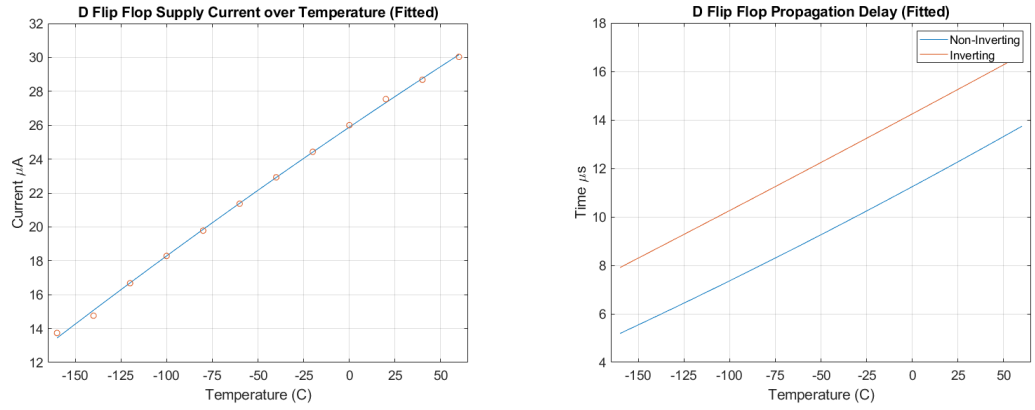


Figure 4.10: (Left) DFFSR Total Power Consumption, (Right) DFFSR Propagation Delay

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The first pass design of a cold-capable, radiation hardened ECL standard cell library was presented in this paper. After testing the fabricated circuits, results have shown that while the cells operate at -160°C, there is still room for improvement.

Firstly, there are concerns about the speed at which the signal swing collapses over temperature. If the signal swing crosses the theoretical minimum swing limit, the ECL gate's ability to resolve a bit becomes less reliable, which is unacceptable for the application this library is designed for.

Secondly, while OR based logic enables much of the more complex logic functions, such as the DFFSR, the imbalance of the differential pair caused by the effective emitter areas of the input transistors as well as the OR gates necessary reliance on a DC reference voltage makes the outputs more susceptible to mismatch.

Thirdly, even considering the coaxial cables' and instrumentation's contribution to the output capacitance during testing, the ECL circuits are still too slow for most processing applications. While low power was achieved, the cost is too great to justify its use for applications that need to operate at higher frequencies.

Finally, there are concerns for the headroom of more involved cells. The ECL reference circuit shown in Figure 3.10 features a negative feedback loop created by $Q3$ and $Q7$. Following the loop's path reveals that the base of $Q7$ will be at approximately $2V_{BE}$ above ground. At -160°C, V_{BE} was found to be over 1V, meaning that this loop will cause headroom issues.

These issues together largely impact the quality of the standard cell library and must be addressed. Since designing the circuits presented in this paper, many updated circuits have been fabricated. The last section of this thesis will briefly discuss the progress that has been made as a result.

5.2 Future Work

As seen by the results illustrated by simulation and testing, the 2V ECL standard cell library has much room for improvement. A primary issue is the speed limitations of the 2V library. For even moderate speeds of tens of megahertz, the 2V library will not perform to this standard.

For applications with high-speed demands, a logic library that can not only match that speed, but also afford more dense logic operations within a given timing and area requirement is needed. For these reasons, a 3.3V, $10\mu A$ standard cell library is being developed. The goal is to remedy the two mentioned issues in exchange for power consumption. This section will give a quick discussion and overview of the current state of this library.

The starting point of the 3.3V ECL template is a bit different than the starting point of the 2V ECL template. While it is sufficient to use an inverter to determine circuit parameters such as device sizing and load resistance, the standard layout must consider the circuit that has the greatest height to dictate the standard cell height of all members of the library. Figure 5.1 shows an XOR gate, which will be used as the basis of subsequent layouts due to the stacked differential pairs that it uses.

The XOR gate uses some ideas from the 2V library but with the added current and supply voltage limits, more flexibility is achieved. Transistors $Q1$ through $Q5$ are used as current mirrors. Transistors $Q6$ and $Q7$ form the first differential pair which, based on their base voltage differential, will steer the current drawn from $Q1$ to one of the two upper differential pairs. This behaves like an "if statement" and is the primary means for accomplishing more complex logic operations in a single cell, something that the 2V ECL cells were unable to accomplish. Transistors $Q8$ through $Q11$ will further steer the current depending on the state of the bottom differential pair. Because of the 10x larger current, the pFETs used in the 2V library are replaced with resistors, which consume less area than the pFETs. Transistors $Q12$ and $Q13$ are emitter follower outputs for the logic circuits. Transistors $Q14$ and $Q15$ are also emitter followers, but they are used to level shift the inputs going to the lower differential pair formed by $Q6$ and $Q7$ in order to maintain their operation in forward active.

The topology in Figure 5.1 is used in many ECL circuits. In the 3.3V library, it is modified into a latch and a multiplexer, both of which require no extra components. With two of these latches, a D Flip Flop with set and reset can be implemented as well. This topology also helps remedy the issues in the 2V ECL library. Firstly, the pFETs are replaced with resistors, which changes the temperature profile of the output voltage. In Section 3.2.2, the pFET's R_{ON} temperature profile is found to be primarily PTAT. Contrarily, the resistors that they are replaced with are CTAT. If current is constant over temperature or CTAT, then the voltage swing will grow as temperature decreases. This increases the static noise margin as temperature decreases and ensures that the signal swing is always sufficient for full range current steering.

Another advantage of this topology is its ability to apply a fully differential input to the gate. In the 2V library, the headroom issues did not allow for stacked differential pairs, and instead more complicated gates were implemented with NOR logic, which requires a reference voltage. Transitioning to stacked differential pairs remove the

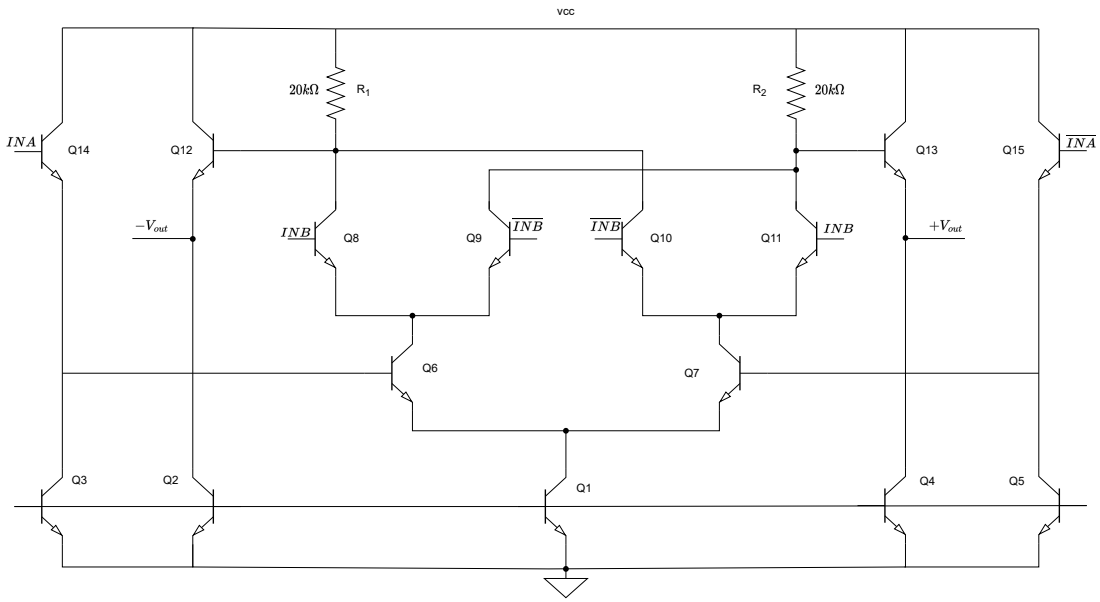


Figure 5.1: 3.3V ECL XOR Gate used for Layout Template

driving burden of the reference voltage generation circuit since less gates are required to utilize a reference voltage. Additionally, any anti-symmetric behavior generated by an off-center reference voltage can be remedied by a subsequent fully differential logic gate.

Aside from the topology benefits, there are clear benefits from the increase in current from $1\mu A$ to $10\mu A$ in terms of speed. The table below shows the performance of a 3.3V ECL inverter over different process corners. The inverter is biased using a 3.3V ECL CTAT reference circuit. The inverter's architecture follows that of Figure 3.1, but with resistors instead of pFETs.

Table 5.1 suggests that the 3.3V ECL inverter can run at 100MHz handily at any process corner, a stark contrast with 2V ECL inverter. Additionally, due to the CTAT reference circuit, both voltage swing and static noise margin increase inversely with temperature. The idea is that for biasing for a harsh, cold environment, the designer need only set the slow corner performance in terms of speed and noise to ensure that subsequent typical and fast corners' performances are superior.

Another added benefit as discussed previously is the level of logic operations within a given area. For example, the layout of the DFFSR is shown in Figure 5.2. This layout is far more compact and saves over half of the area used by the 2V variation, which is made up of six individual OR gates. In fact, this DFFSR takes up the same space as about 3 inverters. This is due to using the structure of the XOR gate shown in Figure 5.1. Additionally, the design is completely horizontally symmetrical around the center, a feature made possible by replacing the pMOS devices with smaller, less rule-constrained resistors. This greatly increases the linearity of the circuit, thereby reducing noise power resulting from input noise.

As expected, providing more design freedom by increasing the headroom and current consumption (thereby increasing the power consumption) of the 2V ECL library, the designer is afforded more choice that inevitably enables better performance than the more power constrained ECL library. This library demonstrates a speed increase of about 15x and has been shown to reduce area consumption of more

complicated cells. At this time, an inverter, OR gate, d flip flop with asynchronous set and reset, 2-to-1 multiplexer, XOR gate, and reference circuit have been designed for this library. Currently, the wait is on the foundry for chip fabrication.

Table 5.1: Simulated Performance Summary of 3.3V ECL Inverter with Fanout of 10

ECL Inverter Post-Layout Performance over Corners			
Design Parameters	Slow (-,+)	Typical (-,+)	Fast (-,+)
VCC (V)	3	3.3	3.6
Temp (C)	125	27	-55
Power Consumption (µW)	86.31	104.2	123.6
Voltage Swing (mV)	167.2, 167.1	216.2, 216.2	265.0, 265.0
Rise Time (ns)	0.487, 0.473	0.427, 0.407	0.366, 0.346
Fall Time (ns)	0.695, 0.657	0.657, 0.610	0.597, 0.564
Propagation Delay (ns)	0.292, 0.255	0.243, 0.210	0.196, 0.167
SNM (mV)	4	26	60

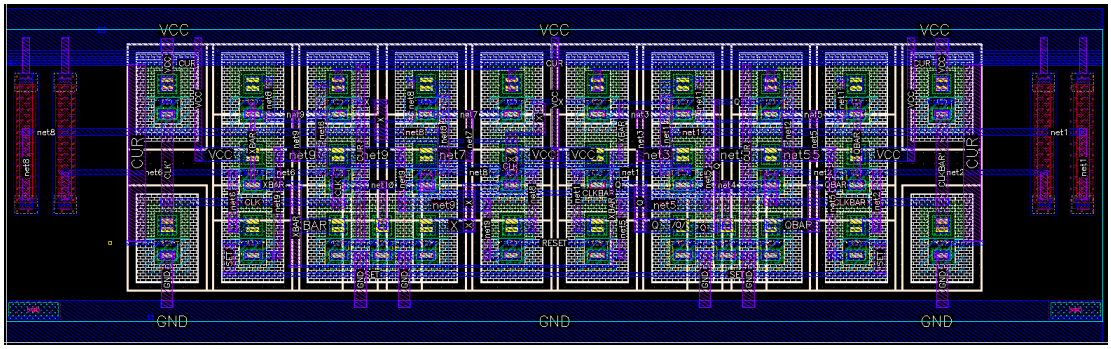


Figure 5.2: Layout of DFFSR for 3.3V Library, Area: 65.365µm x 17.36µm

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Appendix

Appendix A

A.1 Liberate Template File

```
# Setup # #

# Set cells to be characterized
set cells { \
ECL_INV \
ECL_OR2 \
} ;

# comment

# Set all I/O pins of any cells that use the  0.9V to  1.1V logic levels
set io_pins { IN IN_A IN_B INV BUF } ;

# Rails / DC Stuff
set_var supply_define_mode 2;

# This is based off page 332 of ref manual
# See bottom of the file for the old method of handling these rails.
```

```
set_vdd -cells $ cells -name_map VCC_PINS VCC $ VCC_VAL;
set_gnd -cells $ cells -name_map GND_PINS GND $ GND_VAL;
set_gnd -cells $ cells -name_map SUB_PINS sub $ GND_VAL;
set_vdd -cells $ cells -name_map REF_PINS REF $ REF_VAL;
set_vdd -cells $ cells -name_map CUR_PINS CUR $ CUR_VAL;
set_gnd -cells $ cells -name_map LOGIC_LOW LOW $ LOGIC_LOW_VAL;
set_vdd -cells $ cells -name_map LOGIC_HIGH HIGH $ LOGIC_HIGH_VAL;

set_pin_vdd -supply_name VCC_PINS $ cells { VCC} $ VCC_VAL;
set_pin_gnd -supply_name GND_PINS $ cells { GND} $ GND_VAL;
set_pin_vdd -supply_name REF_PINS $ cells { REF} $ REF_VAL;
set_pin_vdd -supply_name CUR_PINS $ cells { CUR} $ CUR_VAL;
set_pin_gnd -supply_name LOGIC_LOW $ cells $ io_pins $ LOGIC_LOW_VAL ;
set_pin_vdd -supply_name LOGIC_HIGH $ cells $ io_pins $ LOGIC_HIGH_VAL ;

# Measurements and such
set_var slew_lower_rise 0.2;
set_var slew_lower_fall 0.2;
set_var slew_upper_rise 0.8;
set_var slew_upper_fall 0.8;

set_var measure_slew_lower_rise 0.2;
set_var measure_slew_lower_fall 0.2;
set_var measure_slew_upper_rise 0.8;
set_var measure_slew_upper_fall 0.8;

set_var delay_inp_rise 0.5;
set_var delay_inp_fall 0.5;
set_var delay_out_rise 0.5;
```

```
set_var delay_out_fall 0.5;
set_var def_arc_msg_level 0;
set_var process_match_pins_to_ports 1;
set_var max_transition 100e-09;
set_var min_transition 8e-12;
set_var min_output_cap 1.2e-16;

set_var sim_duration 10e-5; # pg 898 of ref manual
set_var input_output_voltage 2;
# Templates #
# this template started 6/20/2022
define_template -type delay \
-index_1 { 4 6 8 10 12 14 16 } \
-index_2 { 1 2 3 4 5 6 7 } \
delay_template_7x7_155;
# this template started 6/20/2022
define_template -type power \
-index_1 { 4 6 8 10 12 14 16 } \
-index_2 { 1 2 3 4 5 6 7 } \
power_template_7x7_155;
# ECL_INV #
if { [ALAPI_active_cell "ECL_INV"]} {
define_cell \
-input { IN } \
-output { INV BUF } \
-pinlist { IN INV BUF} \
-delay delay_template_7x7_155 \
-power power_template_7x7_155 \
ECL_INV;
```

```
# -internal_supply { REF CUR VCC GND sub}
# -bidi { REF CUR VCC GND } \
# -pinlist { IN INV BUF REF CUR VCC GND } \

define_leakage -when "IN" ECL_INV;
define_leakage -when "!IN" ECL_INV;

# IN & INV
define_arc \
-vector { F R F } \
-related_pin IN \
-pin INV \
-dual_pin BUF \
ECL_INV; # Falling

define_arc \
-vector { R F R } \
-related_pin IN \
-pin INV \
-dual_pin BUF \
ECL_INV; # Rising
# IN & BUF
define_arc \
-vector { F R F } \
-related_pin IN \
-pin BUF \
-dual_pin INV \
ECL_INV; # Falling
define_arc \
```

```
-vector { R F R } \
-related_pin IN \
-pin BUF \
-dual_pin INV \
ECL_INV;
}

# End ECL_INV

# ECL_OR2 #

if { [ALAPI_active_cell "ECL_OR2"]} {
define_cell \
-input { IN_A IN_B } \
-output { INV BUF} \
-pinlist { IN_A IN_B INV BUF} \
-delay delay_template_7x7_155 \
-power power_template_7x7_155 \
ECL_OR2;

# -internal_supply { REF CUR VCC GND sub}
define_leakage -when "IN_A& IN_B" ECL_OR2; # IN_A & IN_B
define_leakage -when "!IN_A& IN_B" ECL_OR2; # !IN_A & IN_B
define_leakage -when "IN_A& !IN_B" ECL_OR2; # IN_A & !IN_B
define_leakage -when "!IN_A& !IN_B" ECL_OR2; # !IN_A & !IN_B

# Because it is a NOR circuit, we keep the other pin(s) low to force a change at
the output
```

```
# IN_A Arcs #
# INV & B = LOW / 0
define_arc \
-when "(!IN_B)" \
-vector { F 0 R F } \
-related_pin IN_A \
-pin INV \
-dual_pin BUF \
ECL_OR2; # Falling

define_arc \
-when "(!IN_B)" \
-vector { R 0 F R } \
-related_pin IN_A \
-related_pin_dir R\
-pin INV \
-dual_pin BUF \
ECL_OR2; # Rising

# BUF & B = LOW / 0
define_arc \
-when "(!IN_B)" \
-vector { F 0 R F } \
-related_pin IN_A \
-pin BUF \
-dual_pin INV \
ECL_OR2; # Falling

define_arc \
```

```
-when "(!IN_B)" \
-vector { R 0 F R } \
-related_pin IN_A \
-pin BUF \
-dual_pin INV \
ECL_OR2; # Rising

# IN_B Arcs #
# INV & A = LOW / 0
define_arc \
-when "(!IN_A)" \
-vector { 0 F R F} \
-related_pin IN_B \
-pin INV \
-dual_pin BUF \
ECL_OR2; # Falling

define_arc \
-when "(!IN_A)" \
-vector { 0 R F R} \
-related_pin IN_B \
-pin INV \
-dual_pin BUF \
ECL_OR2; # Rising

# BUF & A = LOW / 0
define_arc \
-when "(!IN_A)" \
-vector { 0 F R F } \
```

```
-related_pin IN_B \
-pin BUF \
-dual_pin INV \
ECL_OR2; # Falling

define_arc \
-when "(!IN_A)" \
-vector { 0 R F R } \
-related_pin IN_B \
-pin BUF \
-dual_pin INV \
ECL_OR2; # Rising

}
# End ECL_OR2

# ECL_OR3 #
# if { [ALAPI_active_cell "ECL_OR3"]} {
# define_cell \
# -input { IN_A IN_B IN_C } \
# -output { INV BUF } \
# -pinlist { IN_A IN_B IN_C INV BUF } \
# -delay delay_template_7x7_155 \
# -power power_template_7x7_155 \
# ECL_OR3;
#
# define_leakage -when "IN_A& IN_B& IN_C" ECL_OR3; # IN_A & IN_B & IN_C
# define_leakage -when "IN_A& IN_B& !IN_C" ECL_OR3; # IN_A & IN_B & !IN_C
# define_leakage -when "IN_A& !IN_B& IN_C" ECL_OR3; # IN_A & !IN_B & IN_C
```

define_leakage -when "IN_A& !IN_B& !IN_C" ECL_OR3; # IN_A & !IN_B & !IN_C

define_leakage -when "!IN_A& IN_B& IN_C" ECL_OR3; # !IN_A & IN_B & IN_C

define_leakage -when "!IN_A& IN_B& !IN_C" ECL_OR3; # !IN_A & IN_B & !IN_C

define_leakage -when "!IN_A& !IN_B& IN_C" ECL_OR3; # !IN_A & !IN_B & IN_C

define_leakage -when "!IN_A& !IN_B& !IN_C" ECL_OR3; # !IN_A & !IN_B & !IN_C

#

Because it is an OR circuit, we keep the other pin(s) low to force a change at the output

IN_A Arcs # # # # # # # #

INV & B = LOW / 0 & C = Low / 0

define_arc -when "(!B& !C)" -vector { F X X R F } -related_pin IN_A -pin INV ECL_OR3; # Falling

define_arc -when "(!B& !C)" -vector { R X X F R } -related_pin IN_A -pin INV ECL_OR3; # Rising

#

BUF & B = LOW / 0 & C = Low / 0

define_arc -when "(!B& !C)" -vector { F X X R F } -related_pin IN_A -pin BUF ECL_OR3; # Falling

define_arc -when "(!B& !C)" -vector { R X X F R } -related_pin IN_A -pin BUF ECL_OR3; # Rising

#

IN_B Arcs # # # # # # # #

INV & A = LOW / 0 & C = Low / 0

define_arc -when "(!A& !C)" -vector { X F X R F } -related_pin IN_B -pin INV ECL_OR3; # Falling

define_arc -when "(!A& !C)" -vector { X R X F R } -related_pin IN_B -pin INV ECL_OR3; # Rising

#

BUF & A = LOW / 0 & C = Low / 0

define_arc -when "(!A& !C)" -vector { X F X R F } -related_pin IN_B -pin BUF ECL_OR3; # Falling

define_arc -when "(!A& !C)" -vector { X R X F R } -related_pin IN_B -pin BUF ECL_OR3; # Rising

#

IN_C Arcs # # # # # # # #

INV & A = LOW / 0 & B = Low / 0

define_arc -when "(!A& !B)" -vector { X X F R F } -related_pin IN_C -pin INV ECL_OR3; # Falling

define_arc -when "(!A& !B)" -vector { X X R F R } -related_pin IN_C -pin INV ECL_OR3; # Rising

#

BUF & A = LOW / 0 & B = Low / 0

define_arc -when "(!A& !B)" -vector { X X F R F } -related_pin IN_C -pin BUF ECL_OR3; # Falling

define_arc -when "(!A& !B)" -vector { X X R F R } -related_pin IN_C -pin BUF ECL_OR3; # Rising

}

End ECL_OR3

End Template File

A.2 Liberate Characterization Script

Purpose: Characterization script for COLDTech standard ECL library

————————————————-

Set and print user define variables

————————————————-

```
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;

puts "INFO: Set Directories, Files, and Variables" ;

# Working Directories
set SRC_DIR /research/icasl/zhamdan/9hp/liberate_docs ; # directory where all source data (netlist, models, etc...) are stored
set RUN_DIR [pwd] ; # directory where all generated data (ldb, liberty, etc...) are saved

# Process and temperature settings
set PROCESS tt ; # [ff—tt—ss] - - - > tt = typical, ff = fast corner, ss = slow corner - - > used in set_operating_condition command
set TEMP 25 ; # temperature in C

# DC Voltages & Supplies
set VCC_VAL 2 ; # VCC in volts
set GND_VAL 0 ;
set REF_VAL 1.24 ;
set CUR_VAL 0.677 ;
set LOGIC_LOW_VAL 1.17 ;
set LOGIC_HIGH_VAL 1.32 ;
```

```
# Output .lib name
set LIB zh_coldtech_starved ; # defines the base library name for the liberty file and library inside the .lib file

# Settings and template files
set SETTINGS_FILE $ { SRC_DIR} /zh_ecl_starved_settings.tcl ; # these next several lines set the relevant input file paths
set TEMPLATE_FILE $ { SRC_DIR} /zh_ecl_starved_template.tcl ;
# set CELLS_FILE $ { RUN_DIR} /cells.tcl

# Netlist and Userdata directories
set NETLIST_DIR $ { SRC_DIR} /netlist ;
set USERDATA $ { SRC_DIR} /userdata/userdata.lib ;

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

    # # # # ----------
# # # # Process command line input
# # # # Allow cmdline option to set local TCL variables - liberate  script  var = value
# # # # ex: liberate char.tcl VCC=3.6
# # # # ----------
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
```

```
puts "**********" ;
puts "**********" ;
puts "" ;

puts "INFO: Process command line input" ;
foreach arg $ argv {
if { [string match *=* $ arg] } {
lassign [split $ arg =] a b
set $ a $ b
puts "INFO: Setting $ a = $ b"
}
}
puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

# # # # # ----------
# # # # # Set dependent variables
# # # # # ----------
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;

puts "INFO: Set Dependent Variables" ;
```

set PVT $ { PROCESS} _$ { VCC_VAL} _$ { TEMP} ;

set LIBNAME $ { LIB} _$ { PVT} ;

set MODEL_INCLUDE_FILE $ { SRC_DIR} /include_coldtech.sp ;

set MODEL_INCLUDE_FILE

/research/pdk/9hp/90HPSIGE-9HP/V1.3_3.0a/Models/Spectre/models/allModels.scs

;

puts "DONE" ;

puts "" ;

puts "" ;

puts "" ;

————————————————-

Distributed Resource Management (DRM) setup

Liberate supports both LSF and SunGrid - just update variable rsh_cmd

LSF : set RSH_CMD "bsub -q ¡queueName¿ -n $ THREAD -R ResourceDefinition -o # # # # # SunGrid: set RSH_CMD "qsub -b y -q queueName -n $ THREAD"

Local : set RSH_CMD "local" ;# local machine only

Variables :

THREAD - number of cpus to use on a given machine; 0-use all cpus on machine

CLIENTS - number of Distributed Resource Management (DRM) jobs; 0=disable DRM

————————————————-

run using debug mode # #

set THREAD 1 ;

set CLIENTS 0 ;

run using local mode # #

```
# set THREAD 1
# set CLIENTS 1
# set RSH_CMD "local"
# # # run using distributed mode # # #
# set THREAD 2
# set CLIENTS 4
# if { ![info exists MEM]} { set MEM [expr $ { THREAD} *2000]} ;# default = 2G per thread
# if { ![info exists JOBNAME]} { set JOBNAME liberate}
# set RSH_CMD "bsub -q lnx64 -J $ { JOBNAME} -W 255:0 -P LIBERATE:17.1:AE:test -n $ { THREAD} -R \"(OSREL==EE60) rusage\[mem=$ MEM\] span\[hosts=1\]\" -o # set_var packet_arcs_per_thread 1 ;# use for large cells, default=10

# # # # # ----------
# # # # # Print user define settings to output
# # # # # ----------
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;

puts "INFO:" ;
puts " SRC_DIR = $ { SRC_DIR} " ;
puts " RUN_DIR = $ { RUN_DIR} " ;
puts " LIBNAME = $ { LIBNAME} " ;
```

```
puts " PVT = $ { PVT} " ;
puts " SETTINGS_FILE = $ { SETTINGS_FILE} " ;
puts " TEMPLATE_FILE = $ { TEMPLATE_FILE} " ;
puts " MODEL_INCLUDE_FILE = $ { MODEL_INCLUDE_FILE} " ;
puts " NETLIST_DIR = $ { NETLIST_DIR} " ;
puts " USERDATA = $ { USERDATA} " ;
# if { [info exists CELLS_FILE] } { puts " CELLS_FILE = $ { CELLS_FILE} " }
puts "" ;
puts " THREAD = $ { THREAD} " ;
if { [info exists CLIENTS] } {
puts " CLIENTS = $ { CLIENTS} "
if { [info exists RSH_CMD] } { puts " RSH_CMD = $ { RSH_CMD} " }
}

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

# # # # # ----------------------------
# # # # # Set operating condition
# # # # # ----------------------------
puts "" ;
puts "" ;
puts "" ;
puts "**********************************" ;
puts "**********************************" ;
puts "**********************************" ;
puts "" ;
```

```
puts "INFO: Set Operating Condition" ;
set_operating_condition -name $ { PVT} -voltage $ { VCC_VAL} -temp $ { TEMP} ;

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

# # # # # ----------------------------
# # # # # Set Liberate variables
# # # # # ----------------------------
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;
puts "INFO: Read settings file $ { SETTINGS_FILE} " ;
source $ { SETTINGS_FILE} ; # settings file sourced by char.tcl
puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

# # # # # ----------------------------
# # # # # Debug variables (ignore for now)
# # # # # ----------------------------
# select_index -style 1x1 ;# run only 1st point in table
```

```
# set_var bisection_info 4 ;# print additional bisection search info to output log
# set_var power_info 2 ;# print additional power calculation info of table's 1st point
to file decks/powerInfo1.log

# set_var ski_enable 0
set_var extsim_save_passed all ;# save all run decks and output files
set_var extsim_save_failed all ;# save all run decks and output files
# set_var extsim_save_verify 2 ;# save verify deck
set_var extsim_deck_dir $ { SRC_DIR} /decks ;# specify directory for SPICE decks
and output files
# set_var extsim_tar_cmd "" ;# disable tgz of simulation decks and run logs
set_var parse_ignore_duplicate_subckt 1;

# # # # # ----------------------------
# # # # # Read template
# # # # # ----------------------------
puts "" ;
puts "" ;
puts "" ;
puts "**********************************" ;
puts "**********************************" ;
puts "**********************************" ;
puts "" ;
puts "INFO: Read template file $ { TEMPLATE_FILE} " ;
source $ { TEMPLATE_FILE} ; # template file sourced by char.tcl

puts "DONE" ;
puts "" ;
puts "" ;
```

```
puts "" ;

# # # # # ----------------------------
# # # # # Read CELLS_FILE
# # # # # ----------------------------
puts "" ;
puts "" ;
puts "" ;
puts "**********************************" ;
puts "**********************************" ;
puts "**********************************" ;
puts "" ;

puts "Cells to be characterized: $ { cells} " ;

# if { [info exists CELLS_FILE]} { # if CELL_INFO points to an actual file
# if { [file exists $ { CELLS_FILE} ]} { # if CELL_INFO points to an actual file
# puts "INFO: Read cell list file"
# source $ { CELLS_FILE} # cells.tcl file sourced by char.tcl
# } else {
# puts "WARNING: Specified CELLS_FILE ($ { CELLS_FILE} ) does not exist."
# }
# }

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;
```

```
# # # # # ----------------------------
# # # # # define device models
# # # # # ----------------------------
puts "" ;
puts "" ;
puts "" ;
puts "**********************************" ;
puts "**********************************" ;
puts "**********************************" ;
puts "" ;

puts "INFO: Define device models (spectre, define_leafcell)." ;
set_var extsim_model_include $ { MODEL_INCLUDE_FILE} ; # sets the model file to use, references your PDK typically

define_leafcell -type nmos -pin_position { 0 1 2 3} { ldnfet8 ldnfet8i dgnfet dgnfet_rf dgvnfet dgvnfet_rf dgxnfet hvtnfet lvtnfet nfet nfet_rf hvtnfettw }
define_leafcell -type r -pin_position { 0 1 2} { oprrpres }
define_leafcell -extsim_model -type pmos -pin_position { 0 1 2 3} { ldpfet8 ldpfet8i dgpfet dgpfet_rf dgvpfet dgvpfet_rf dgxpfet hvtpfet lvtpfet pfet pfet_rf }
define_leafcell -type diode -pin_position { 0 1} { diodenbpw diodenbx diodenwx diodenwx2 diodenx diodepipw diodepix diodepnw sbd.scs sbdxp1}
define_leafcell -type black_box -pin_position { 0 1} { subc }

# # # # NPN define_leafcell attempts
# define_leafcell -type npn -pin_position { 0 1 2} { npnhp_inh npnhpt_inh npnhptd_inh npnmb_inh npnmbt_inh npnmbtd_inh npnhpxp1_inh npnhpxp1t_inh npnhpxp1td_inh npnmbxp1_inh npnmbxp1t_inh npnmbxp1td_inh }
# define_leafcell -type npn -pin_position { 0 1 2 3} { npnhp npnhpt npnhptd
```

npnmb npnmbt npnmbtd npnhpxp1 npnhpxp1t npnhpxp1td npnmbxp1 npnmbxp1t npnmbxp1td }

define_leafcell -type nmos -pin_position { 0 1 2 3} { npnhp npnhpt npnhptd npnmb npnmbt npnmbtd npnhpxp1 npnhpxp1t npnhpxp1td npnmbxp1 npnmbxp1t npnmbxp1td }

define_leafcell -type black_box -pin_position { 0 1 2 3} { npnhp npnhpt npnhptd npnmb npnmbt npnmbtd npnhpxp1 npnhpxp1t npnhpxp1td npnmbxp1 npnmbxp1t npnmbxp1td }
2.3 — 5/31/2022

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

————————————————-
read cell netlists
————————————————-
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;

puts "INFO: Read cell netlist " ;

```
# # setup client to read only netlist of cells being characterized
set packet_cells [packet_slave_cells] ;
if { [llength $ packet_cells]¿0} { set cells $ packet_cells } ;
# # read netlist
# set spicefiles $ MODEL_INCLUDE_FILE
set spicefiles { } ;
foreach cell $ cells { lappend spicefiles $ { NETLIST_DIR} /$ { cell} .scs } ;
read_spice -format spectre $ spicefiles ;
# read_spice -format spectre "$ MODEL_INCLUDE_FILE $ spicefiles" ;

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;

# # # # # ————————————————————-
# # # # # Distributed Resource Management (DRM) setup
# # # # # ————————————————————-
puts "" ;
puts "" ;
puts "" ;
puts "**********************************" ;
puts "**********************************" ;
puts "**********************************" ;
puts "" ;

puts "INFO: Check for Clients and Packets"
if { [info exists CLIENTS] & & ($ CLIENTS ¿ 0) } {
set_var packet_mode arc
```

```
set_var rsh_cmd $ RSH_CMD
if { ($ RSH_CMD eq "local") } {
set_var packet_clients 1
} else {
set_var packet_clients $ CLIENTS
if { $ { THREAD} ¡1} {
puts "WARNING: When using DRM, THREAD=0 can cause client machine to overload; resetting THREAD=1."
set THREAD 1
}
}
}

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;
# # # # # ————————————————-
# # # # # Run characterization
# # # # # ————————————————-
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;

# # Simple command
```

```
puts "INFO: Run Characterization" ;

# char_library -ccs -ecsm -extsim spectre -cells $ cells -thread $ THREAD ;
char_library -ccs -ecsm -io -extsim spectre -cells $ cells -thread $ THREAD ; # [2.3] 5/31/2022

# # Build command string then eval
# set charCmd "char_library -extsim spectre -cells \{ $ cells\} "
# if { [info exists THREAD] & & $ { THREAD} ¿0 } { set charCmd "$ charCmd -thread $ { THREAD} " }
# puts "INFO: Run Characterization - charCmd = $ charCmd"
# eval "$ charCmd"

puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;
# # # # # ————————————————-
# # # # # Write output
# # # # # ————————————————-
puts "" ;
puts "" ;
puts "" ;
puts "**********" ;
puts "**********" ;
puts "**********" ;
puts "" ;

# # # Write ldb # # #
```

```
puts "INFO: Write ldb" ;
file mkdir $ { RUN_DIR} /ldb ;
# In packet_arc mode, by default, existing ldb does not get overwritten. User should use -overwrite option
write_ldb -overwrite $ { SRC_DIR} /liberate_docs/ldb/$ { LIBNAME} .ldb ;

# # # Write Liberty # # #
puts "INFO: Write Liberty" ;
file mkdir $ { SRC_DIR} /liberate_docs/lib ;

write_library -driver_waveform -unique_pin_data -bus_syntax { []} -overwrite -filename $ { RUN_DIR} /lib/$ { LIBNAME} _nldm.lib $ { LIBNAME} ;
# write_library -driver_waveform -unique_pin_data -bus_syntax { []} -user_data $ { USERDATA} -overwrite -filename $ { RUN_DIR} /lib/$ { LIBNAME} _nldm.lib $ { LIBNAME}
# write_library -driver_waveform -unique_pin_data -bus_syntax { []} -user_data $ { USERDATA} -ecsm -ecsmn -overwrite -filename $ { RUN_DIR} /lib/$ { LIBNAME} _ecsm.lib $ { LIBNAME}
# write_library -driver_waveform -unique_pin_data -bus_syntax { []} -user_data $ { USERDATA} -ccs -ccsn -ccsp -overwrite -filename $ { RUN_DIR} /lib/$ { LIBNAME} _ccs.lib $ { LIBNAME}
puts "DONE" ;
puts "" ;
puts "" ;
puts "" ;
```

A.3 Liberate Settings File

```
# $ Id: settings.tcl,v 1.16 2016/08/24 20:55:41 ctai Exp ctai $ #
# # # # # ————————————————-
# # # # # Set liberate variables
# # # # # ————————————————-
# # # Get tool version # # #
lassign [split [ALAPI_version] .] x1 x2 version(minor) version(sub)
set version(major) "$ { x1} .$ { x2} "

# ignore duplicate subckt definitions
# set_var parse_ignore_duplicate_subckt 1 ;

# # # External Simulator (Spectre) settings # # #

# set_var extsim_cmd_option "+aps +spice -mt +liberate +rcopt=2"
set_var extsim_cmd_option "+spice -mt +liberate +rcopt=2"
set_var extsim_deck_header "simulator lang=spectre1 options reltol=1e-4 lang=spice"
set_var extsim_option "redefinedparams=ignore hier_ambiguity=lower limit=delta "
set_var extsim_leakage_option "redefinedparams = ignore hier_ambiguity = lower limit
= delta "
set_var extsim_flatten_netlist 0; # [2.3] 5/31/2022



# # # SKI # # #
set_var ski_enable 1
set_var ski_clean_mode 1 ;# run $ ALTOSHOME/bin/clean_sm.sh to clean up inactive
semaphores
set_var ski_compatibility_mode 1
```

```
set_var power_tend_match_tran 1 ;# use tran_tend for power_tend for non-ski (match ski)

# # # Misc # # #
set_var parse_auto_define_leafcell 0 ;# disable auto leaf cell determination
set_var tmpdir /dev/shm ;# /dev/shm - use local RAM disk for tmp dir, /tmp - use local disk
set_var extsim_deck_dir [file normalize "decks"] ;# specify directory for SPICE decks and output files
set_var set_var_failure_action error

# # # Input waveform # # #
set_var predriver_waveform 2 ;# 2=use pre-driver waveform

# # # Arc Generation

# # # Capacitance # # #
set_var min_capacitance_for_outputs 1 ;# write min_capacitance attribute for output pins
# set_var measure_cap_lower_rise 0
# set_var measure_cap_upper_rise 0.5
# set_var measure_cap_upper_fall 1
# set_var measure_cap_lower_fall 0.5

# # # Timing # # #
set_var force_condition 4 ;

# tristate cell
# set_var disable_method 2 ;# 2=measure disable timing from input 50# set_var
```

tristate_disable_transition 0 ;# 0=output value=0 for three_state_disable transition

Constraint # #
set_var constraint_info 2 ;
set_var constraint_search_time_abstol 1e-12 ;# 1ps resolution for bisection search
set_var nochange_mode 1 ;# enable nochange_* constraint characterization
avail version 17.1.2
if { ($ version(major) =17.1) & & ($ version(minor) =2)} {
set_var constraint_vector_mode 4 ;# look at metric=delay and glitch to determine worst case
}

min_pulse_width # #
set_var conditional_mpw 0 ;# 0=disable conditional mpw

Leakage # #
set_var max_leakage_vector [expr 2**10]
set_var leakage_float_internal_supply 0 ;# get worst case leakage for power switch cells when off
set_var reset_negative_leakage_power 1 ;# convert negative leakage current to 0

Power # #
set_var voltage_map 1 ;# create pg_pin groups, related_power_pin / related_ground_pin
set_var pin_based_power 0 ;# 0=based on VDD only; 1=power based on VDD and VSS (default);
set_var power_combinational_include_output 0 ;# do not include output pins in when conditions for combinational cells

set_var force_default_group 1

set_default_group -criteria { power avg} ;# use average for default power group

set_var power_subtract_leakage 4

set_var subtract_hidden_power 2 ;# 1=subtract hidden power for all cells

set_var subtract_hidden_power_use_default 3;# 3 = subtract hidden power from matched when condition then default group

set_var power_multi_output_binning_mode 1 ;# binning for multi-output cell considered for both timing and power arcs

set_var power_minimize_switching 1

set_var max_hidden_vector [expr 2**10]

CCS # #

CCSN # #

set_var ccsn_include_passgate_attr 1 ;# include pin level attribute is_unbuffered and has_pass_gate, and

ccsn_*_stage group level attribute is_pass_gate

set_var ccsn_model_related_node_attr 1 ;# enable output of ccsn_first_stage attribute

related_spice_node, load_cap_rise, load_cap_fall

set_var ccsn_tempus_promote_mode 1 ;# same as ccsn_model_related_node_attr

CCSP # #

set_var ccsp_min_pts 15 ;# CCSP accuracy

set_var ccsp_rel_tol 0.01 ;# CCSP accuracy

set_var ccsp_table_reduction 0 ;# CCSP accuracy

set_var ccsp_tail_tol 0.02 ;# CCSP accuracy

set_var ccsp_related_pin_mode 2 ;# use 3 for multiple input switching scnarios and Voltus only libraries

ECSM #

ECSMN #

ECSMP #

EM #

if { [info exists CHAR_EM_TECH_FILE] & & ($ CHAR_EM_TECH_FILE ne "") } {
set_var em_tech_file [file normalize $ CHAR_EM_TECH_FILE] }

————————————————-
Writing Output Files
————————————————-
set_var write_library_is_unbuffered 1
set_var cell_use_both_ff_latch_groups 2 ;# allow use of multiple ff,latch,state_table groups in userdata file
set_var user_data_override { power_down_function pg_pin input_signal_level output_signal_level }
set_var sdf_cond_style 1
set_var parenthesize_not 0 ;# use !A instead of !(A)
set_var driver_type_model_pad_check 1 ;# enable fix to disable output of driver_type pin attribute for tie cells CCR1407896
set_var ccsn_print_is_needed_if_false_attr_value 1
set_default_group -criteria { constraint off} ;# disable writing of default constraint arc
set_var write_library_allow_switching_and_hidden_power 1 ;# allow writing of switching and hidden power for same pin

————————————————-

liberate_lv

————————————————-

if { $ ::LIBERATE_program == "LIBERATE_LV" } {

set validate_cells_per_bundle 10000

}

————————————————-

variety

————————————————-

if { $ ::LIBERATE_program == "VARIETY" } {

set_var variation_mean_nominal_mode 4 ;# save mean, stddev, and skewness values (in addition to normal variation data) to ldb

set_var variation_static_partition_mode 2 ;# Enable logic-cone analysis (0=disable; 1=faster/less accurate; 3=slower/more accurate)

set_var non_linear_random_variation 3 ;# (1=characterize positive and negative variation; 3=trade off minor early accuracy for faster run time)

use default of 0 for AOCV(fastest)

Constraint # # # #

set_var constraint_random_variation_search_time_abstol

[expr [get_var constraint_search_time_abstol] * 0.1] ;# typically set to 10set_var lvf_constraint_early_late_mode 1 ;# 1=output early and late sigma type for constraint

more accruate for non-gaussian distribution

set_var mpw_variation 1 ;# enable mpw variation characterization

Monte Carlo # # # #

set_var extsim_monte_option "sampling=lds" ;# set Spectre Monte Carlo sampling method [standard lhs lds orthogonal]

lhs=Latin-Hypercube, lds=Low-Discrepancy Sequence

set_var extsim_cmd_option "[get_var extsim_cmd_option] +mp=5" ;# distribute Monte Carlo jobs (5 .alter per job)}

Appendix B

B.1 Measurement Naming Convention

Most measurements are separated into a "+" category and a "-" category, the former being for the non-inverting output and the latter being the inverting output. Below is a list of measurements and what they refer to.

- High: Logic high level
- Low: Logic low level
- Swing: Output signal swing (difference between High and Low)
- Rise: 10% to 90% rise time
- Fall: 90% to 10% fall time
- Prop1: Propagation delay when rising transition
- Prop2: Propagation delay when falling transition
- Prop: Average propagation delay (average of Prop1 and Prop2)
- Mid: Midpoint of output voltage swing (Average of High and Low)

B.2 Data

Table B.1: ECL Inverter at 2V Cold Testing Data

Inverter Coldtest Data (Full)																		
Temp (C)	High + (V)	High - (V)	Low + (V)	Low- (V)	Swing + (V)	Swing - (V)	Rise + (µs)	Rise - (µs)	Fall - (µs)	Fall+ (µs)	Prop1 + (µs)	Prop2 - (µs)	Prop2 + (µs)	Prop1 - (µs)	Prop+ (µs)	Prop - (µs)	Supply Current (µA)	MID+ (V)	MID- (V)
-160	0.976	0.966	0.859	0.862	0.117	0.104	0.708	0.645	8.888	10.868	0.124	4.491	7.371	0.129	3.7475	2.31	1.18	0.9175	0.914
-140	1.003	0.989	0.862	0.872	0.141	0.117	0.82	0.438	10.059	9.935	0.166	6.674	7.872	0.106	4.019	3.39	1.37	0.9325	0.9305
-120	1.03	1.012	0.869	0.878	0.161	0.134	0.776	0.434	9.842	12.118	0.13	7.755	7.742	0.103	3.936	3.929	1.56	0.9495	0.945
-100	1.05	1.036	0.872	0.882	0.178	0.154	0.786	0.599	12.12	14.309	0.136	8.296	9.412	0.11	4.774	4.203	1.74	0.961	0.959
-80	1.073	1.063	0.879	0.885	0.194	0.178	0.848	0.725	13.508	14.209	0.125	9.75	9.412	0.119	4.7685	4.9345	1.94	0.976	0.974
-60	1.097	1.086	0.882	0.885	0.215	0.201	0.926	0.76	14.066	14.381	0.139	10.162	9.934	0.13	5.0365	5.146	2.15	0.9895	0.9855
-40	1.116	1.11	0.886	0.885	0.23	0.225	1.01	0.842	17.001	16.354	0.15	11.284	10.861	0.154	5.5055	5.719	2.38	1.001	0.9975
-20	1.14	1.136	0.882	0.882	0.258	0.254	1.164	0.952	17.564	18.374	0.162	11.793	11.502	0.157	5.832	5.975	2.59	1.011	1.009
0	1.167	1.16	0.879	0.882	0.288	0.278	1.223	1.067	19.094	19.978	0.18	12.354	12.229	0.174	6.2045	6.264	2.84	1.023	1.021
20	1.19	1.186	0.876	0.875	0.314	0.311	1.37	1.165	21.232	21.126	0.2	13.448	13.115	0.203	6.6575	6.8255	3.07	1.033	1.0305
40	1.214	1.21	0.866	0.868	0.348	0.342	1.408	1.205	23.048	23.09	0.227	14.229	14.35	0.218	7.2885	7.2235	3.35	1.04	1.039
60	1.237	1.237	0.855	0.858	0.382	0.379	1.49	1.275	24.688	24.701	0.251	15.205	15.054	0.252	7.6525	7.7285	3.65	1.046	1.0475

Table B.2: DFFSR at 2V Cold Testing Data

DFFSR Coldtest Data (Full)																		
Temp (C)	High + (V)	High - (V)	Low + (V)	Low - (V)	Swing+ (V)	Swing - (V)	Rise + (µs)	Rise - (µs)	Fall - (µs)	Fall+ (µs)	Prop+ (µs)	Prop - (µs)	SetProp+ (µs)	SetProp- (µs)	ResetProp+ (µs)	ResetProp- (µs)	Supply Current (µA)	MID+ (V)	MID- (V)
-160	1.102	1.028	0.861	0.827	0.241	0.201	5.802	10.917	16.294	9.858	5.0855	7.4045	0.96	9.152	5.952	3.194	13.74	0.9815	0.9275
-140	1.115	1.048	0.861	0.834	0.254	0.214	4.096	4.09	12.941	7.971	5.8255	9.131	4.999	11.693	7.149	5.754	14.76	0.988	0.941
-120	1.149	1.068	0.867	0.841	0.282	0.227	4.4	5.2	13.96	8.32	6.704	9.5645	4.832	12.897	7.527	5.613	16.676	1.008	0.9545
-100	1.175	1.102	0.874	0.841	0.301	0.261	5.661	6.346	16.752	11.341	7.668	10.7475	6.778	12.967	7.86	6.996	18.286	1.0245	0.9715
-80	1.196	1.122	0.874	0.841	0.322	0.281	5.939	5.896	16.024	12.509	7.8845	10.5665	6.701	13.357	8.717	7.45	19.78	1.035	0.9815
-60	1.216	1.142	0.867	0.841	0.349	0.301	5.888	6.762	18.755	12.947	8.9895	12.0295	5.856	13.697	8.813	6.88	21.367	1.0415	0.9915
-40	1.249	1.169	0.867	0.827	0.382	0.342	7.39	7.07	19.93	15.79	9.92	12.8885	6.232	14.988	11.12	7.232	22.925	1.058	0.998
-20	1.276	1.189	0.874	0.827	0.402	0.362	7.542	8.138	22.582	16.883	10.061	12.8335	6.79	15.956	11.586	7.942	24.432	1.075	1.008
0	1.298	1.2	0.864	0.825	0.434	0.375	7.986	8.573	25.651	18.424	11.4945	14.0675	6.814	16.565	12.267	8.117	26	1.081	1.0125
20	1.314	1.236	0.847	0.821	0.467	0.415	8.531	9.389	28.112	20.003	11.7295	15.171	7.01	16.706	12.63	8.514	27.54	1.0805	1.0285
40	1.343	1.256	0.841	0.78	0.502	0.476	8.59	9.63	29.42	20.96	12.662	16.0885	8.765	17.578	13.316	9.877	28.68	1.092	1.018
60	1.37	1.289	0.821	0.747	0.549	0.542	9.9	9.82	32.2	23.53	14.083	16.676	10.31	19.11	14.402	11.574	30.03	1.0955	1.018

Table B.3: OR Gate at 2V Cold Test Results

OR Gate Coldtest Data (Full)														
Temp (C)	High + (V)	High - (V)	Low + (V)	Low - (V)	Swing+ (V)	Swing - (V)	Rise + (µs)	Rise - (µs)	Fall - (µs)	Fall+ (µs)	Prop + (µs)	Prop - (µs)	MID + (V)	MID - (V)
-160	1.067	1.051	0.966	0.957	0.101	0.094	0.58	0.63	6.7	9.42	1.87	2.15	1.0165	1.004
-140	1.09	1.071	0.979	0.974	0.111	0.097	0.68	0.77	6.95	9.66	2.03	2.77	1.0345	1.0225
-120	1.113	1.094	0.993	0.987	0.12	0.107	0.86	1.1	8.51	9.44	1.9	2.7	1.053	1.0405
-100	1.14	1.118	1.006	1	0.134	0.118	0.88	0.94	8.75	9.3	2.04	3.73	1.073	1.059
-80	1.164	1.144	1.016	1.011	0.148	0.133	0.93	1.06	10.38	11.01	2.44	3.9	1.09	1.0775
-60	1.19	1.171	1.026	1.017	0.164	0.154	1.02	1.18	11.14	11.38	2.91	3.62	1.108	1.094
-40	1.221	1.195	1.033	1.027	0.188	0.168	0.96	1.3	10.72	12.83	3.03	3.96	1.127	1.111
-20	1.247	1.225	1.036	1.031	0.211	0.194	1.02	1.25	12.54	13.6	3.52	4.19	1.1415	1.128
0	1.271	1.248	1.046	1.037	0.225	0.211	1.28	1.52	14.67	15.44	3.59	4.45	1.1585	1.1425
20	1.31	1.284	1.043	1.029	0.267	0.255	1.02	1.17	13.47	14.88	3.9	4.89	1.1765	1.1565
40	1.324	1.304	1.049	1.036	0.275	0.268	1.1	1.25	14.8	16.64	4.45	5.26	1.1865	1.17
60	1.344	1.33	1.056	1.029	0.288	0.301	1.194	1.354	16.899	17.504	5.53	6.51	1.2	1.1795

Vita

Zakaraya Hamdan was born on December 18, 1998. He earned a Bachelor's of Science in Electrical Engineering from The University of Tennessee in 2021. During that time, he worked under Dr. Nicole McFarlane as an undergraduate researcher for embedded electronics applications in the biomedical field.. He then transitioned to working for Dr. Benjamin Blalock in the Integrated Circuits and Systems Laboratory (ICASL). Here, he worked on many analog and digital circuits from BiCMOS to strictly CMOS circuits, all of which were designed for harsh environment use. After graduating with a Master's Degree in Electrical Engineering, he plans to work as an ambitious Analog/Mixed Signal designer.