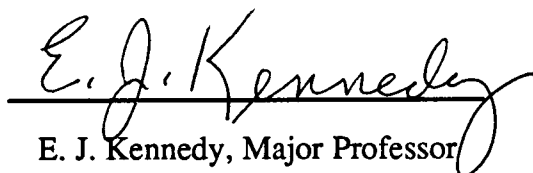


To The Graduate Council :

I am submitting herewith a thesis written by Alice Hsuanchen Wu entitled "Gamma Irradiation Testing of Electronic Devices, and Evaluation of Irradiated CMOS Components on MOSIS Test Chips." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Engineering, with a major in Electrical Engineering.


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GAMMA IRRADIATION TESTING OF ELECTRONIC
DEVICES, AND EVALUATION OF
IRRADIATED CMOS
COMPONENTS ON
MOSIS TEST
CHIPS

A Thesis Presented for the
Master of Engineering Degree
The University of Tennessee, Knoxville

Alice Hsuanchen Wu

December 1990

ACKNOWLEDGMENTS

The author wishes to acknowledge the guidance and collaboration of her thesis advisor, Dr. E. J. Kennedy. Special appreciation is expressed to thesis committee members, Dr. T. V. Blalock and Dr. J. M. Rochelle. The technical assistance of Mr. G. T. Alley and Mr. C. L. Britton, Jr of the Oak Ridge National Laboratory is sincerely appreciated. Dr. T. F. Williams and his assistants of the Chemistry Department, the University of Tennessee, Knoxville, are acknowledged for providing the gamma radiation facility.

This research was supported by two separate contracts under the auspices of the United State Department of Energy (DOE). During the period from January 1987 to December 1987 the sponsor was the Office of Facilities Fuel Cycle and Test Programs, under contract No. DE-AC05-84OR21400 with Martin Marietta Energy Systems, Inc. From April 1989 to January 1990 the sponsorship was DOE contract No. ERD-89-823 between the University of Oklahoma and the Instrumentation and Controls Division, Oak Ridge National Laboratory, Martin Marietta Energy Systems, Inc.

Along with her thesis advisor and committee members, the author also appreciates much encouragement and support from her parents, Dr. & Mrs. Chieh Wu, and her sister and brother-in-law, Tung-Mao and Ming-Yun Shih.

ABSTRACT

Two distinct testing programs are reported. The first involves irradiation testing of commercial integrated circuits to determine total dose effects to gamma radiation. Eight irradiations in a Cobalt-60 Gammacell at a mean dose rate of 59 krad/hr for a total absorbed dose of 12 megarads (+10, -20%) were performed. Generally, five parts of each item were characterized before, and after, irradiation. Devices were irradiated in a passive mode with leads shorted. Integrated circuits tested involved mostly analog components, such as operational amplifiers, voltage comparators, transistor arrays, analog switches, and buffers.

The second phase of testing included different size MOS transistors, resistor, and lateral and vertical NPN bipolar transistors fabricated on MOSIS test chips. These devices were evaluated for general characteristics, as well as noise performance both before, and after, irradiation to a total dose of 1.9 megarad (+10, -20%) in the Gammacell irradiator.

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CHAPTER I

INTRODUCTION

Technological advances in radiation-hardened electronics has rapidly changed the state-of-the-art design for applications in areas of military systems used in space, as well as nuclear environments, strategic systems, and radiation detectors. Instruments used under radioactive environments must be able to withstand both the instantaneous dose (dose rate) as well as the accumulated dosage (total dose) for radiation over their expected operating life span. The literature abounds in experiments performed to study the effects of gamma and neutron irradiations on special integrated circuit (IC) components developed specifically for radiation environments. However, irradiation results on low-cost commercial IC's are not as available. Also, radiation effects on low-cost monolithic CMOS components are not generally available. Monolithic fabrication programs, such as MOSIS (Metal-Oxide-Semiconductor Implementation Service) are of interest both to the academic community as well as commercial companies and national laboratories.

1.1 Definition of Study

The research reported in this thesis is divided into two parts. During the period January 1987 to December 1987 a selection of commercial integrated circuits were subjected to a total gamma dose of $\geq 10^7$ rad. This work was supported by a contract between the Electrical and Computer Engineering Department, the University of Tennessee, Knoxville (UTK) and the Oak Ridge National Laboratory (ORNL). The contract was administered by the Fuel Recycle Division, ORNL, with the research goal to investigate

electronic components that might be suitable for use in a reactor fuel reprocessing facility. The radiation environment for such a facility envisioned mostly gamma radiation, with an anticipated total dose of 10 megarads.

The second phase of research involved the investigation of complementary metal-oxide-semiconductor (CMOS) devices fabricated on special low-cost monolithic integrated circuit chips under the MOSIS fabrication program. This research was conducted between April, 1989 and January 1990. The intent was to investigate the radiation effects of gamma radiation for a total dose of > 1 megarad. The contract support for this program involved a cooperative effort between the University of Tennessee, the University of Oklahoma, and ORNL under sponsorship of the DOE in the Superconducting Super-Collider (SSC) national program. The research was conducted in the Instrumentation and Controls Division, ORNL.

1.2 Scope of Work

This thesis describes the experiment testing and evaluation of the characteristics of several semiconductor devices, both pre- and post- irradiation. The contents of this thesis listed are as follows:

Chapter II is a brief summary of the effects of gamma irradiations on semiconductors as stated in the literature.

Chapter III summarizes the evaluation of radiation effects on the commercial components, including testing setup, procedures, and results.

Chapter IV summarizes the evaluation of CMOS MOSIS chip, including IC layout, testing setup, procedures, and results.

Chapter V concludes the experimental results and suggest possible future study. The experimental data for all the components are given in the appendices.

CHAPTER II

AN OVERVIEW OF RADIATION EFFECTS

2.1 Introduction

This chapter is a summary of the literature on gamma-irradiation effects on various silicon technologies. This functions as basic background related to the research projects. Subsequent chapters build on these concepts for effective evaluation. This is intended as a brief summary for the reader, and not an in-depth explanation of radiation effects. The reader is referred to excellent text descriptions on radiation by Messenger [1], Ma [2], and contract reports at UTK by Orrick [3], Su [4], and Blalock [5].

2.2 Gamma Rays [6,7]

Both parts of the research is mainly concerned with radiation effects due to gamma rays. Gamma rays are identified as electromagnetic radiation from a nuclear reaction. They are a more penetrating type of ionizing radiation than alpha and beta rays. Gamma radiation is emitted by excited nuclei undergoing radioactive decay. The energies of gamma rays are determined by the differences in energies between the excited state of a nuclei and their lower nuclear states.

The primary particle for gamma rays is a photon having zero rest mass and neutral electrical charge. Photons have three types of interactions with atoms of the bombarded material: photoelectric effect, Compton scattering, and pair production. Energetic free electrons, Compton electrons, and positron-electron pairs are produced in all these interactions.

The unit for absorbed energy deposited in materials by ionizing gamma radiation is expressed in terms of the rad (radiation absorbed dose). One rad is equivalent to the absorbed energy of 100 ergs or 10^{-5} joules per gram of material. When rad is used, the referenced material must be specified and is silicon throughout this thesis unless GaAs material was used. The ionizing-radiation dose rate is commonly given in rads (Si) per unit time.

2.3 Dominant Basic Mechanisms [7]

The two principal effects of radiation on semiconductor devices are displacement and ionization. Energetic electrons and photons can cause displacement at higher energy levels. For electrons, ≈ 150 keV is the minimum energy required to induce displacement in silicon. For photons, a minimum of ≈ 100 eV is required. However, the ionization is the dominant mechanism associated with gamma radiation.

2.3.1 Displacement [7,8]

Displacement is defined as physical damage which disrupts a normal crystal lattice. As stated by Srour [7], the defect forms appear mainly as simple defects, such as, vacancies and interstitials, and defect clusters. By the processes of generation, recombination, trapping, compensation, and tunneling, additional energy levels are created in the bandgap which cause a reduction in carrier concentration. The reduced carrier concentration decreases carrier mobility and tends to make the semiconductor more intrinsic. These effects create imperfections in the crystal lattice structure and also changes the electrical characteristics of semiconductor devices that are being irradiated.

2.3.2 Ionization

Ionization is the removing of electrons from an atom to form ionized atoms and free electrons, which is commonly known as the generation of electron-hole pairs. The damage effects due to ionization are classified into two groups.

The first group is the transient damage due to photocurrents generated through the flow of minority carriers across a pn junction. These effects are prompt and decay after the radiation pulse is removed.

The second group is the surface damage due to the semipermanent changes near the surface of MOS devices or in the passivating layer of bipolar transistors. The ionization causes the permanent trapping of free charges (known as charge buildup) in the silicon dioxide layer on the surface of MOS devices. This damage effect can exist in the devices for years after radiation exposure.

2.4 Effects of Radiation on Semiconductor Devices [2, 7, 8, 9]

A list of some radiation effects on bipolar junction transistors (BJT), junction field-effect transistors (JFET), and metal-oxide semiconductor field-effect transistors (MOSFET) is presented in Table 2-1 along with the fundamental mechanism causing such damages. The dominant radiation damage on bipolar transistors is due to the displacement causing a decrease in carrier mobility. Ionization inducing photocurrents and charge buildup is the major effect for both JFET and MOSFET devices. Detailed descriptions for each effect and its causes can be found in the references given.

Table 2-1. Summary of radiation effects on semiconductor devices.

Transistor Type	Damage Caused By	Radiation Effect
BJT	Displacement	Increase turn-on time
	Displacement	Decrease storage time
	Displacement	Increase collector-emitter saturation voltage
	Displacement	Increase saturation resistance
	Displacement & Ionization	Decrease current gain
	Displacement & Ionization	Increase junction leakage currents
	Displacement & Ionization	Increase collector resistance
	Displacement & Ionization	Increase junction breakdown voltages
	Ionization	Increase junction capacitance
	Ionization	Decrease punchthrough voltage
JFET	Displacement	Increase channel resistivity
	Displacement & Ionization	Decrease transconductance
	Ionization	Increase junction leakage currents
	Ionization	Increase drain-source ON resistance
MOSFET	Ionization	Decrease saturation drain current
	Displacement	Increase channel resistivity
	Displacement	Decrease transconductance
	Displacement & Ionization	Increase drain-source ON resistance
	Ionization	Shift threshold voltage
	Ionization	Decrease channel mobility
	Ionization	Increase channel propagation delays
	Ionization	Increase leakage current

CHAPTER III

PART I: IRRADIATION OF COMMERCIAL COMPONENTS

3.1 INTRODUCTION

The research work from January 1987 to December 1987 involved gamma irradiation of commercial IC's and discrete components, to a total maximum dose of approximately 12 megarads. The facility used was the Gammacell-200 irradiator located in the Chemistry Department, UKT. The dose rate varied from 62 krad/hr to 57 krad/hr over the years time, due to the radioactive decay of Cobalt-60. Thus, for an average dose rate of 59 krad/hr, a total irradiation time of 204 hours would be required.

The literature [10] indicates that for dose rates of $< 6 \times 10^6$ rad/hour, the total accumulated gamma dose is relatively independent of the dose rate. All devices were placed inside a thin cylindrical aluminum container (dia.= 2.5 in, height = 7 in). The shielding effect of the container was entirely negligible due to the low gamma absorption by aluminum. For lead attachment to biased devices, polyvinyl chloride (PVC) insulated wires were used. PVC has excellent resistance to gamma rays for dose for ≥ 10 megarads [11].

A sketch of the active volume of the Gammacell irradiator is shown in Figure 3-1. A spacer was used to raise the level to the 80% indication; hence, all devices generally obtained a deviation within -20% to +10%, or the total dose achieved by components was typically 12 megarads (-20%, +10%). The work of Orrick [3] had disclosed that there were not significant differences between passive irradiations (irradiated with all leads shorted) and actively-biased irradiations if the technology involved was bipolar or junction field-effect (JFET) transistor. However, this concept cannot be extended to MOS

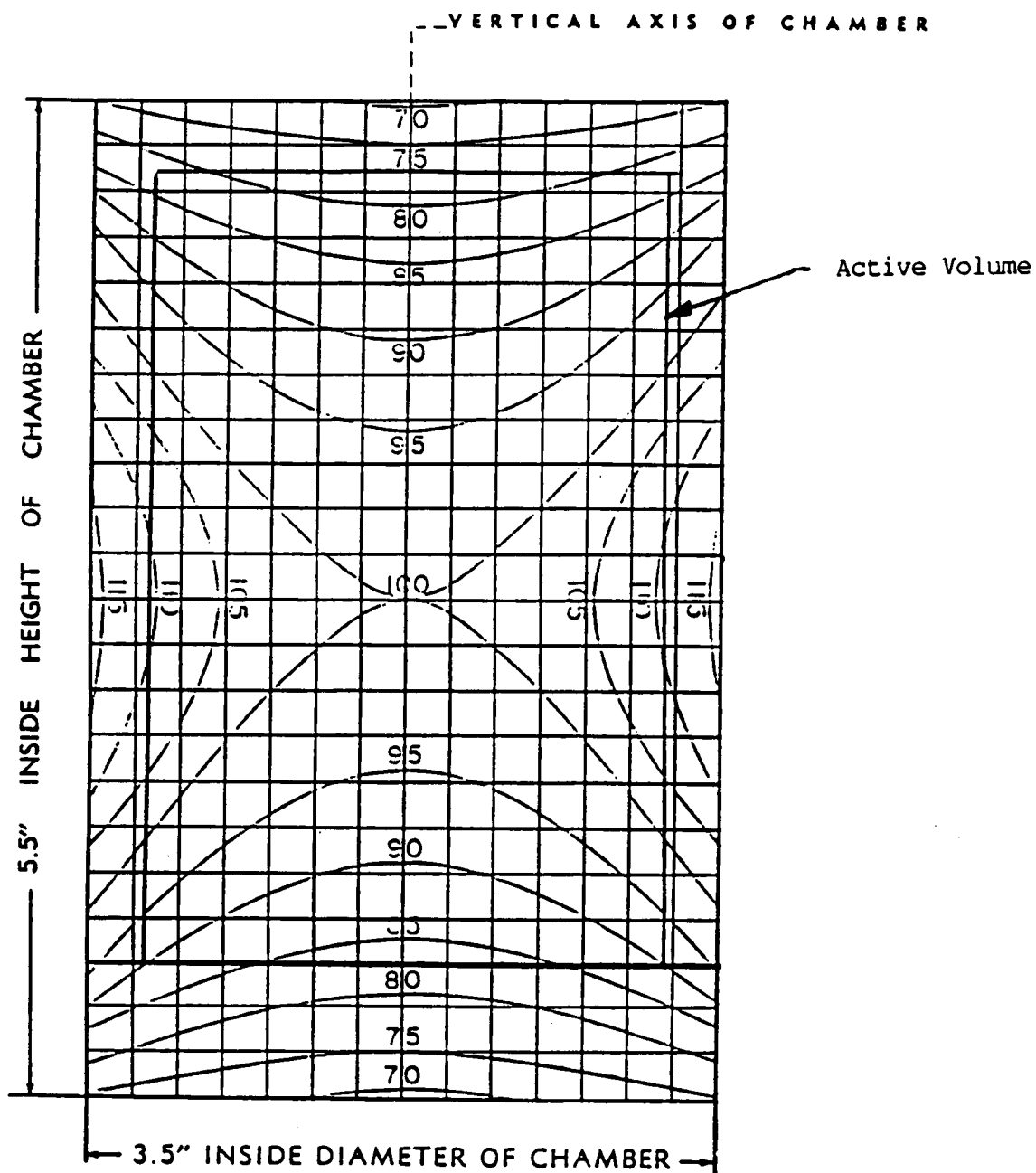


Figure 3-1. Gammacell-200 irradiator. Restricted active device volume is indicated.

technology; hence, later irradiations involving CMOS fabricated structures were done with bias conditions applied as much as possible.

3.2 IRRADIATION RESULTS

A complete list of all commercial devices tested under the first phase of the research is given in Table 3-1 through 3-9. Necessary parameters of each component were evaluated before and after irradiation to establish their tolerances of radiation effects. A brief summary of the most important radiation effects after irradiations is also indicated in each table. Much of the accompanying tabular data and discussion was presented earlier in UTK subcontract report TR-EE/EL-19 [12]. A partial listing of the accumulated data is in Appendix A.

3.2.1 Analog Switches

Analog switches are a critical ingredient for an A/D converter, as well as any data acquisition system. In general, one would desire a JFET technology due to the excellent radiation resistance of JFET's. Hence, the D125, DG126, and DG129 units in Table 3-1 were all JFET switches, with bipolar transistor driver interfacing. As anticipated, all of these switches performed well after > 10 megarad dose. It does appear that the Intersil units suffered less degradation than the Siliconix units, and would therefore be preferred. The DG145 devices, from Siliconix, all failed due to irradiation. These are dual double-pole-double-throw (DPDT) JFET switches with very low ON resistance (typically 7 ohms). Hence, the control circuitry would be more elaborate than for the DPST type circuits, like the DG125-6-9 devices. The test circuit used for the evaluation of turn-on and turn-off times is that shown by various manufacturers in their data manuals, and is

Table 3-1. Radiation test results for analog switches.

Part Number	Manufacturer	Description	≥ 10 Megrad Effects
D125B	Intersil; Siliconix	6-channel FET switch driver (Bipolar IC) $t_{ON} = 0.5 \mu s$ (max) $t_{OFF} = 1.2 \mu s$ (max)	$t_{ON} = 0.4 \mu s$ $t_{OFF} = 0.25 \mu s$ (Intersil and Siliconix units were identical)
DG126B	Intersil; Siliconix	Dual DPST JFET 25 Ω ON resistance 0.4 μs turn-on time 1.3 μs turn-off time	Intersil: $t_{ON} = 8.5 ns$ $t_{OFF} = 8 ns$ $R_{ON} = 29 \Omega$ Siliconix: $t_{ON} = 10 ns$ $t_{OFF} = 210 ns$ $R_{ON} = 25 \Omega$
DG129B	Intersil; Siliconix	Dual DPST JFET 30 Ω ON resistance 0.5 μs turn-on time 1.1 μs turn-off time	Intersil: $t_{ON} = 8.5 ns$ $t_{OFF} = 8.7 ns$ $R_{ON} = 26 \Omega$ Siliconix: $t_{ON} = 10 ns$ $t_{OFF} = 160 ns$ $R_{ON} = 26 \Omega$
DG145B	Siliconix	Dual DPST JFET 15 Ω ON resistance 1.5 μs turn-on time 2.5 μs turn-off time	Failed

illustrated in Figure 3-2.

There were seven JFET analog switches with bipolar transistor driver interfacing and from two manufacturers tested for post-radiation; however, only three were tested prior to irradiation. These three switches had four samples, and the other switches had five samples. They were irradiated with $\geq$ ten megarads total dosage.

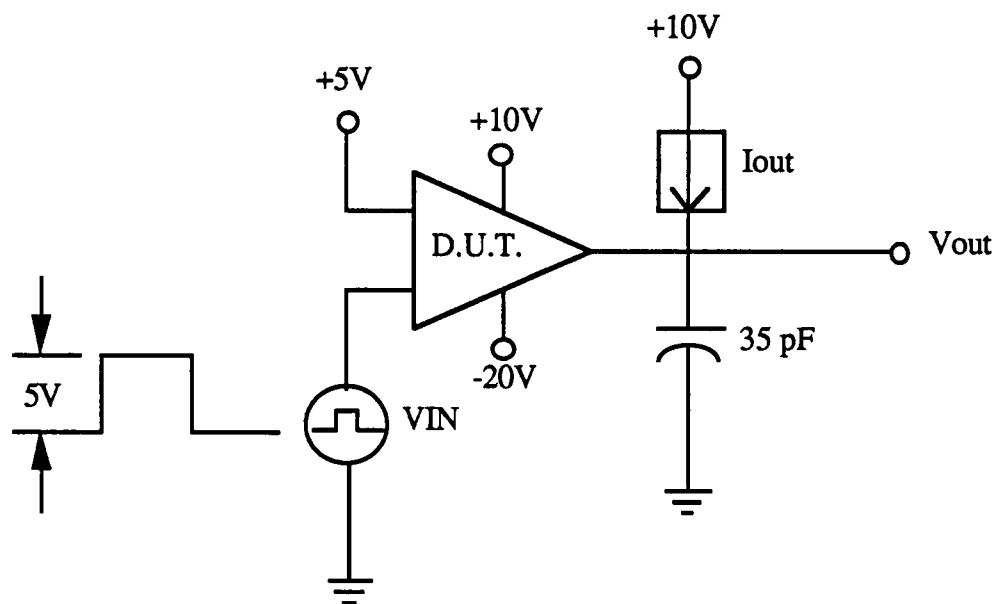
Only summary data is indicated in Table 3-1. Complete pre- and post-radiation data is shown in Appendix A.

3.2.2 Operational Amplifiers

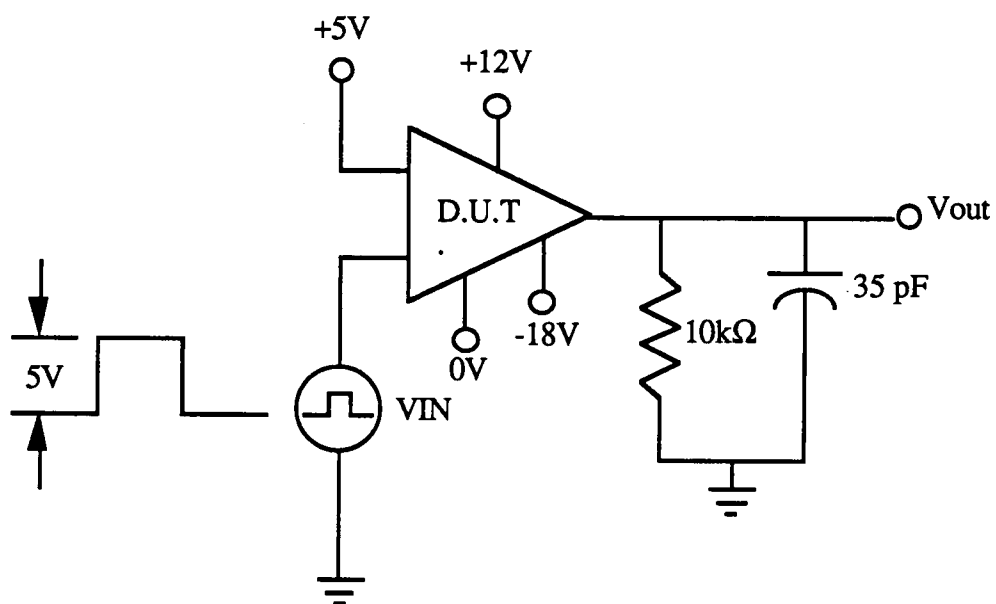
Twelve different types of operational amplifiers (op amps) from seven manufacturers were tested as listed in Table 3-2. The sample size for each device ranged from two to eight. They included JFET input and bipolar input; single, dual, and quad units for each chip; dielectric-isolation and junction-isolation processes using either single or dual power supplies.

Three devices (AOP1510, LT1028ACJ, and RC4227FN) stopped functioning after a ten megarad dose. The AOP1510 device was an early gallium-arsenide (GaAs) device, and probably suffered from very marginal characteristics. We have never found devices from Linear Technology to be radiation tolerant. We have no explanation as to why the Raytheon devices (RC4227) failed. Four out of eight CA3280 by RCA failed to operate. The other surviving four samples suffered severe degradation on their frequency and time responses. The rest of the op amps in Table 3-2 also had significant effects on some of their parameters.

The dc data for the op amps were acquired by utilizing the Tektronix 577 curve tracer with the 178 linear IC test fixture [13, 14]. The power supplies for all amplifiers were fixed at ± 15 V except for the CA3450 E which required ± 6 V and for the SL9999C



(a)



(b)

Figure 3-2. Switching time test circuits for devices (a) D125B and (b) DG126B, DG129B, and DG145B.

Table 3-2. Radiation test results for operational amplifiers.

Part Number	Manufacturer	Description	≥ 10 Megarad Effects
AOP1510	Anadigics	150 MHz GBW GaAs	Failed
CA3280AE	RCA	Dual, Differential, Variable OTA, Bipolar input, High PSRR	4 of 8 failed, Max. $\Delta V_{OS} = 1.5$ mV 70% decrease in GBW 50% decrease in SR
CA3450E	RCA	200 MHz GBW 220 V/ μ s SR	1 of 4 failed Max. $\Delta V_{OS} = 8.9$ mV 24% decrease in GBW 27% decrease in SR
LT1028ACJ	Linear Technology	Very low noise (0.8nV/ $\sqrt{\text{Hz}}$), Bipolar, GBW>50MHz	Failed
MC34071P	Motorola	Ground sensing, General purpose, Low-cost, Bipolar	Max. $\Delta V_{OS} = 40$ mV $I_B = 5$ μ A, Reduced PSRR, A_{OL} , CMRR, 50% decrease in SR Still usable
MC34081P	Motorola	BIFET, SR = 25 V/ μ s, GBW = 8 MHz	Max. $\Delta V_{OS} = 33$ mV $I_B = 3$ nA, Reduced PSRR, A_{OL} , CMRR, GBW, SR, Still usable
OP42EZ	PMI	Fast, Precision, JFET input, GBW = 10 MHz, SR = 50 V/ μ s	Max. $\Delta V_{OS} = 4.2$ mV 21% decrease in CMRR 31% decrease in SR
OP44	Precision Monolithics, Inc. (PMI)	Fast, JFET input, GBW = 20 MHz, SR = 100 V/ μ s	Max. $\Delta V_{OS} = 6$ mV $I_B = 3$ nA, $A_{OL} > 5 \times 10^5$,
OP44			PSRR > 85 dB, CMRR > 100 dB, 15% increase in I_{PS} Excellent output drive

Table 3-2. (continued)

Part Number	Manufacturer	Description	≥ 10 Megarad Effects
OP470	PMI	Quad OP27, Bipolar input, High A_{OL} , PSRR, CMRR	Max. $\Delta V_{OS} = 78.2 \mu V$ 30% decrease in GBW 16% decrease in A_{OL}
OPA111B	Burr-Brown	Precision, Low noise, JFET input, High A_{OL} , CMRR	Max. $\Delta V_{OS} = 3.8 mV$ 56% decrease in SR 11% decrease in PSRR
OPA606KP	Burr-Brown	JFET input, High A_{OL} , High CMRR, SR	Max. $\Delta V_{OS} = 58.8 mV$ 25% decrease in SR 24% decrease in CMRR
RC4227FN	Raytheon	Precision, Dual OP27, Very low noise, Bipolar input, Low V_{OS}	Failed
SL9999C	Plessey	GBW = 400MHz, Bipolar process	Max. $\Delta V_{OS} = 6.4 mV$ Inconclusive results for SR and GBW

which required + 12 V and - 5 V.

The dc data included offset voltage, output saturation voltages with various loads, open-loop gain (A_{OL}), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), input bias currents, and power supply currents. Test modes, displays, sweep rate, and test procedures for measuring the characteristics are detailed in the 577 User's Manual [13]. The CA3450 device is a very-high speed operational amplifier, and a 14 pF compensation capacitor was needed to provide stability for unity gain.

The various dc characteristic data were obtained from photographs taken from the curve tracer displays. The precise measurement was typically better than 10% deviation except for values of A_{OL} , CMRR, and PSRR greater than 140 dB and for input bias currents less than 50 pA.

The ac data were taken from typically dynamic test circuits as shown in Figure 3-3. The circuits were constructed on a protoboard which contributed significant stray capacitance and degraded the operational amplifier performance. Therefore, lower slew-rate and gain-bandwidth product were expected during testing. Since the same circuit test setups were employed both before and after irradiations, the radiation effects should still be observed by the characteristics variations. A printed circuit board (PCB) was used with the SL9999 op amp to measure the ac characteristics due to its high speed (400 MHz). Plessey Semiconductors' September 1986 preliminary information sheet provided the PCB layout [14].

Table 3-2 indicates summary characteristics. More complete deviations in offset voltage (V_{OS}), saturation voltage, open-loop gain (A_{OL}), common mode and power-supply rejection ratios (CMRR, PSRR), gain-bandwidth product (GBW), input bias currents, power supply currents, and slew-rates (SR) are included in Appendix A.

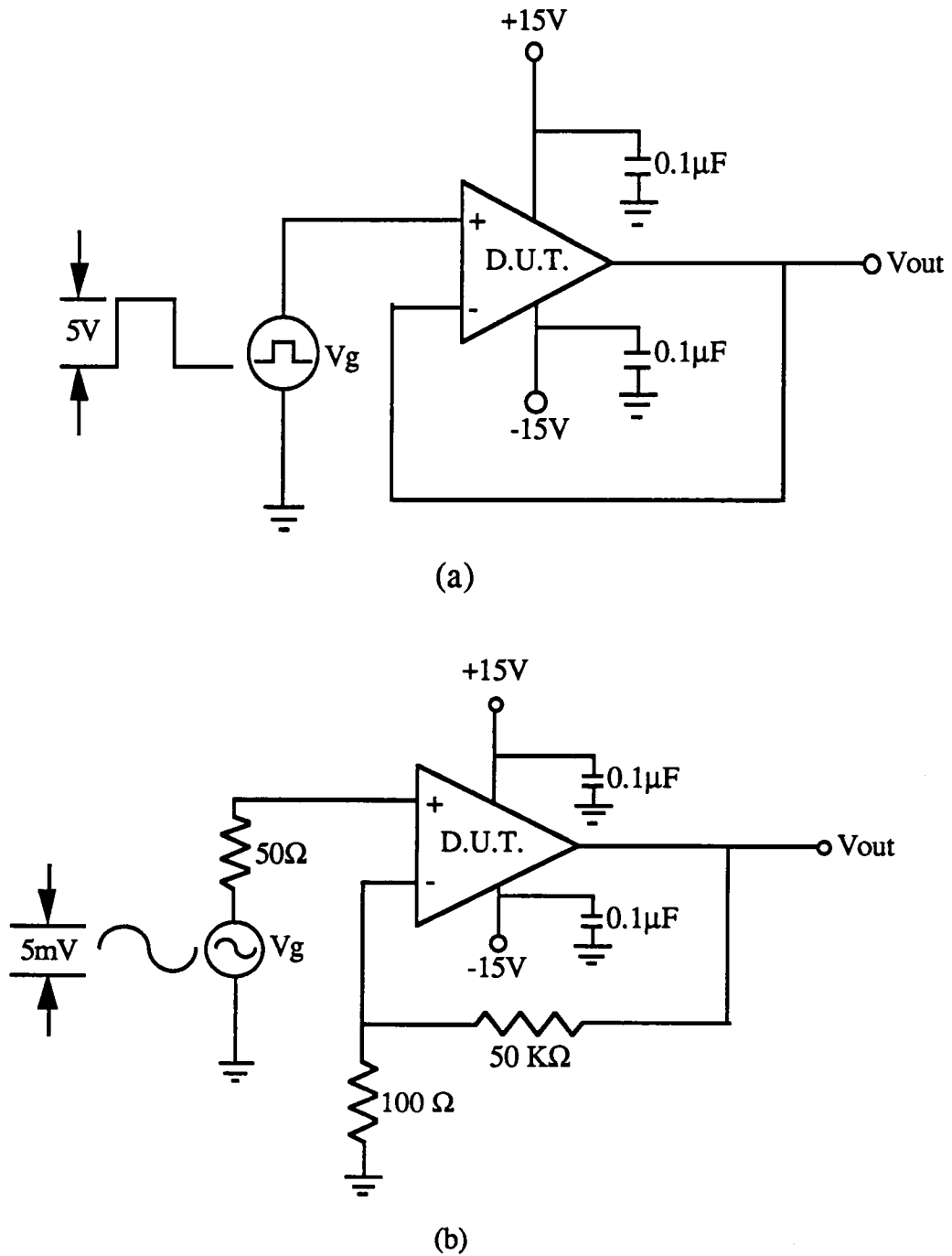


Figure 3-3. Typical dynamic test circuits for measuring (a) slew-rates and (b) gain-bandwidth products of operational amplifiers.

3.2.3 Temperature Sensors

Only two types of positive-temperature coefficient semiconductor temperature sensors (thermistors) were tested for radiation performance evaluation. These devices were from Amperex, Inc. Thermistors can be an inexpensive way to monitor temperatures. However, the decrease of resistance sensitivity and the positive temperature coefficient (PTC) eliminated the possibility of precise monitoring in a radiation environment. Experimental results are summarized in Table 3-3 and are depicted in Figure 3-4. Also the average values and the deviation range of these sensors are given in Table 3-4.

The sensors had a quasi-linear temperature-dependent resistivity. An oven was used to regulate a range of temperatures: 25°C, 50°C, 75°C, and 100°C during the test. The sensors were placed on blocks of wood to isolate from the inside metal wall of the oven and were wired through the side wall. On the other end, the resistivity changes were measured by a multimeter.

Table 3-3. Radiation effects on nominal positive-temperature coefficient = + 0.7% / °C silicon temperature sensors.

Part Name	≥ 10 Megarad Effects
KTY 81	0 - 6% decrease in Ω / °C PTC = 0.687% / °C
KTY 83	1 - 12% decrease in Ω / °C PTC = 0.67% / °C

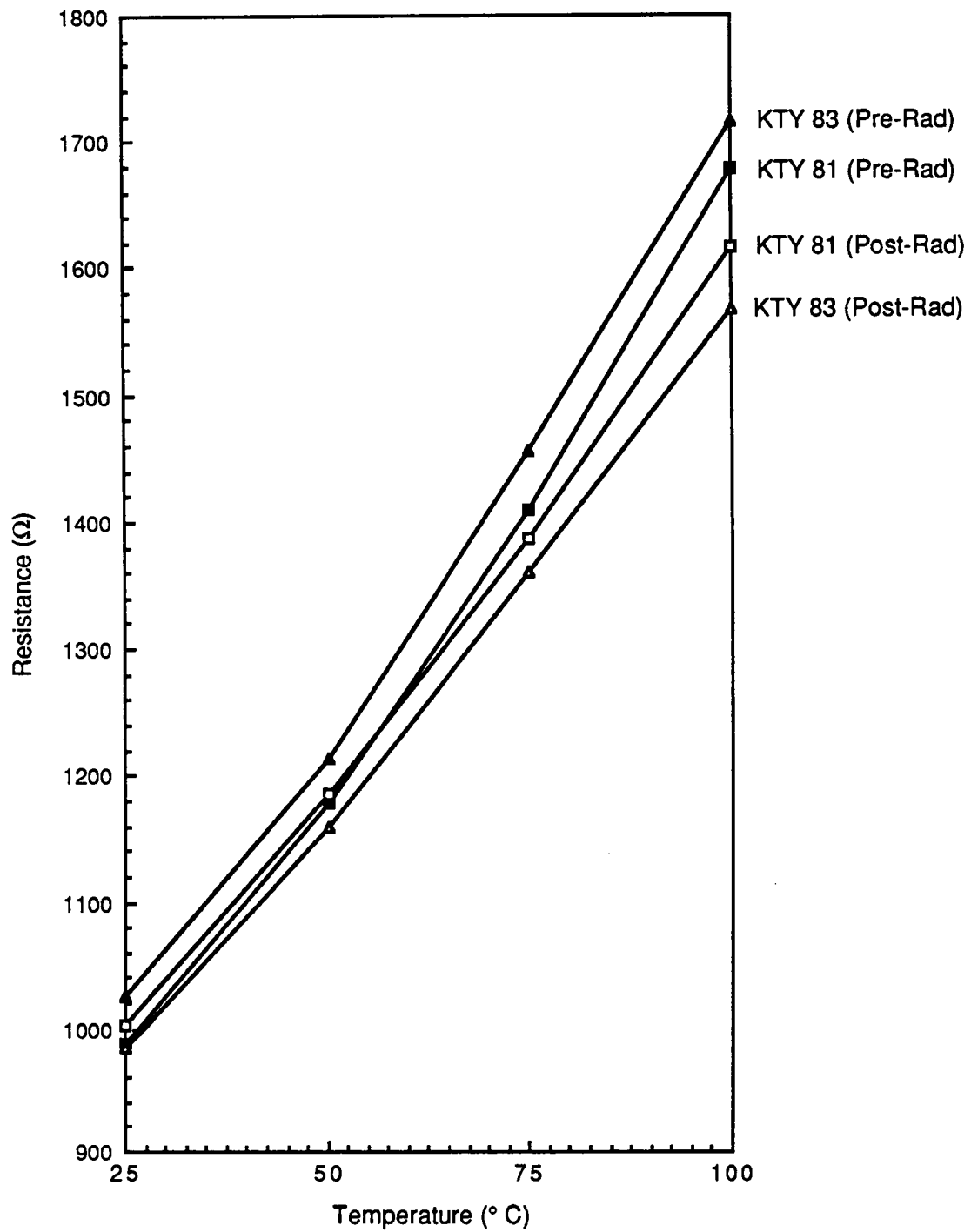


Figure 3-4. Plot of average resistance versus temperature pre- and post-radiation on Amperex temperature sensors.

Table 3-4. List of average values and deviation range for resistances of temperature sensors.

Part Name	Condition	Pre-Radiation	Post-Radiation	Unit
KTY 81	T = 25 °C	989 [982, 993]	1003 [956, 1041]	Ω
	T = 50 °C	1179 [1174, 1182]	1186 [1128, 1233]	Ω
	T = 75 °C	1409 [1408, 1410]	1380 [1320, 1440]	Ω
	T = 100 °C	1678 [1671, 1682]	1615 [1542, 1669]	Ω
KTY 83	T = 25 °C	1026 [1023, 1029]	984 [937, 1033]	Ω
	T = 50 °C	1213 [1208, 1217]	1159 [1102, 1221]	Ω
	T = 75 °C	1455 [1449, 1460]	1360 [1294, 1436]	Ω
	T = 100 °C	1716 [1671, 1682]	1567 [1554, 1659]	Ω

3.2.4 Transistor Arrays

Four kinds of monolithic transistor arrays from different manufacturers were tested for dc characteristics, using the Tektronix 577 curve tracer. Table 3-5 indicates the significant drop of the current gain after irradiation.

The EN2015 and EN2016 units had appeared promising, since their fabrication technology utilizes dielectric isolation (D. I.), which had been shown by Orrick [3] to offer exceptionally good radiation properties. Unfortunately, these units (manufactured by Elantec, Inc.) indicated such severe degradation after gamma irradiation that they are not useful. The only device among the four types that is available for > 10 megarad use is the LM3146 (or CA3146) array (5 npn transistors). Although the current-gain (h_{FE}) degrades considerably, the device is still operable with careful circuit design. Also, the higher frequency version of the same chip, the CA3127, demonstrates equivalent radiation-hardened properties.

Table 3-5. Radiation test results for transistor arrays.

Part Number	Manufacturer	Description	≥ 10 Megarad Effects
EN2015AC	Elantec	Quad pnp array, D. I. $f_T = 350$ MHz $h_{FE} = 175$ to 216 at 1 mA	$h_{FE} = 21$ to 31 at 1 mA Degrading matching
EN2016CN	Elantec	Quad npn array, D. I. $f_T = 400$ MHz $h_{FE} = 100$ to 140 at 1 mA	$h_{FE} = 12$ to 45 at 1 mA Very poor matching
LM3146N (CA3146AE)	National Semiconductor (RCA)	5 npn transistors, $f_T = 500$ MHz $h_{FE} = 124$ to 169 at 0.8 mA	$h_{FE} = 39$ to 49 at 0.8 mA Excellent matching
MAT02BH	PMI	Dual npn, Very low noise, $f_T = 200$ MHz $h_{FE} = 531$ to 701 at 3 mA	$h_{FE} = 30$ to 46 at 3 mA Degrading matching

3.2.5 Voltage Comparators

Similar techniques as for op amps were applied for testing voltage comparators. The same equipment was utilized to procure the dc characteristics: offset voltage, output saturation voltage, maximum output voltage with various load, input bias currents, and supply currents. Eight types of comparators from five manufacturers were tested. General characteristics are shown in Table 3-6. Sample size varied from two to eight.

Comparators CMP05, MC3430, NE521, and SP9685 were operated with ± 5 V power supplies. The other comparators requiring dual power supplies were LM361 and NE529 with ± 10 V, and the CMP01 required ± 15 V supplies. A single $+5$ V power supply was used for the CMP04 units. Also an external pullup resistor was needed for this unit to provide a passive pullup for its open-collector TTL output.

Table 3-6. List of voltage comparators tested.

Part Name	Manufacturer	Descriptions
CMP01EZ	PMI	Bipolar, Precision, $t_r = 110$ ns
CMP04FY	PMI	Bipolar, Quad, Precision, $t_r = 300$ ns, Open-collector TTL output
CMP05FZ	PMI	Bipolar, Precision, $t_r = 60$ ns, Latch circuit, TTL output
LM361N	National Semiconductor	Bipolar, Differential input, $t_r = 14$ ns, Complementary TTL output
MC3430P	Motorola	Quad differential input, Precision, $t_r = 55$ ns, Pull-up MTTL output
NE521N	Signetics	Bipolar, Dual differential input, Precision, $t_r = 8$ ns, TTL output
NE529N	Signetics	Bipolar, Differential input, Precision, $t_r = 6$ ns, TTL/ECL output
SP9685	Plessey Semiconductors	$t_r = 2.7$ ns, Latch circuit, Open-emitter ECL output

The connection of the inverting and non-inverting inputs was reversed on the test fixture when offset voltages were measured, and the manual was consulted for measuring method. The test circuit with no load for measuring response-time and rise-time is shown in Figure 3-5. The response time was defined as the period from the zero-crossing of the input test signal to 10% of the final output voltage. Because of the stray capacitance from the protoboard and the finite rise-time of the input signal, the time-related data were lower than expected. The same circuit degradation as for operational amplifier tests was anticipated before and after irradiations.

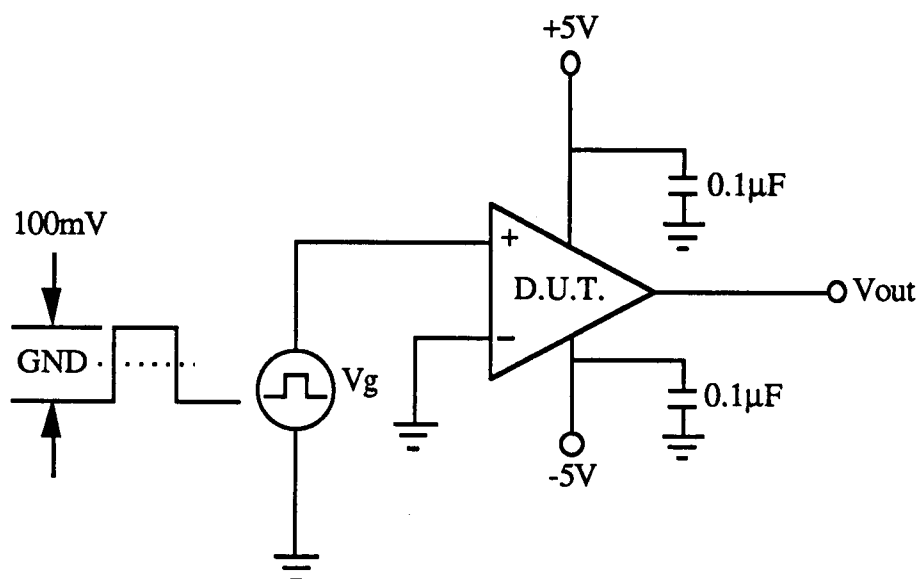


Figure 3-5. Test circuit with no load for measuring response-time and rise-time for voltage comparators.

All devices were irradiated up to a total dosage of $\geq$ ten megarads. Table 3-7 shows irradiation effects. Two devices failed after the radiation. The failure of SP9685 was due to damage to the latch circuit at the output. The CMP04 units had been tested and irradiated with two megarad of gamma dose and 5×10^{13} n/cm² of neutron dose by previous study [4] in 1984, were retested, irradiated with additional ten megarads of gamma ray, and failed to function after that. All other devices tested had shown good radiation tolerance.

Generally speaking, the output saturation voltages increased slightly with radiation damages which was due to the degradation in the collector current of the output bipolar transistor. As the current gain decreased the output transistors became less saturated and, consequently, the output saturation voltage increased. However, output saturation voltages of CMP01 units decreased and that of MC3430 P units had no clear direction of changes.

3.2.6 Voltage Followers/Buffers

Two voltage followers were tested, as shown in Table 3-8. Both voltage followers were operated with ± 15 V power supplies during testing. The dc specifications of input bias currents, power supply rejection ratios, and power supply currents were acquired by using the same equipment in the same manner as operational amplifiers. The ac specifications of slew rate, propagation delay time, and rise time were measured in the circuit configuration as shown in Figure 3-6. The propagation delay time was measured between the 10% crossing of the input signal and 10% high-to-low transition point of the output signal. Output voltage swing and peak load currents were also obtained.

After ≥ 10 megarad dose, ELH0033 buffers stopped functioning, and BUF03 units had severe degradation on maximum voltage drive (down to $0.1 V_{p-p}$), increased in input bias current from 237 pA to 42.59 μ A, slightly decreased supply currents, and could not be measured for slew rate.

Table 3-7. Radiation effects on voltage comparators.

Device Name	≥ 10 Megarad Effects
CMP01EZ	Maximum $\Delta V_{os} = 1.87$ mV Maximum $\Delta T_{pd} = 70$ ns Maximum $t_r = 1.29$ μ s
CMP04FY	Failed
CMP05FZ	Maximum $\Delta V_{os} = 1.50$ mV Maximum $\Delta T_{pd} = 26.4$ ns Maximum $\Delta t_r = 145.5$ ns
LM361N	Maximum $\Delta V_{os} = 1.94$ mV Maximum $\Delta T_{pd} = 4$ ns Maximum $\Delta t_r = 20$ ns
MC3430P	Maximum $\Delta V_{os} = -2.09$ mV Maximum $\Delta t_r = 32.8$ ns
NE521N	Maximum $\Delta V_{os} = 12.02$ mV Maximum $\Delta T_{pd} = 22.2$ ns Maximum $\Delta t_r = 52.6$ ns
NE529N	Maximum $\Delta V_{os} = 1.87$ mV Maximum $\Delta T_{pd} = 23$ ns Maximum $\Delta t_r = 15.6$ s
SP9685	Failed

Table 3-8. List of voltage followers/buffers tested.

Device Name	Manufacturer	Descriptions
BUF03EJ	PMI	JFET input, SR = 250 V/ μ s, GBW = 63 MHz, 70 mA load
ELH003CG	Elantec	FET input, SR = 1400 V/ μ s, GBW = 100 MHz, 0.25 A load

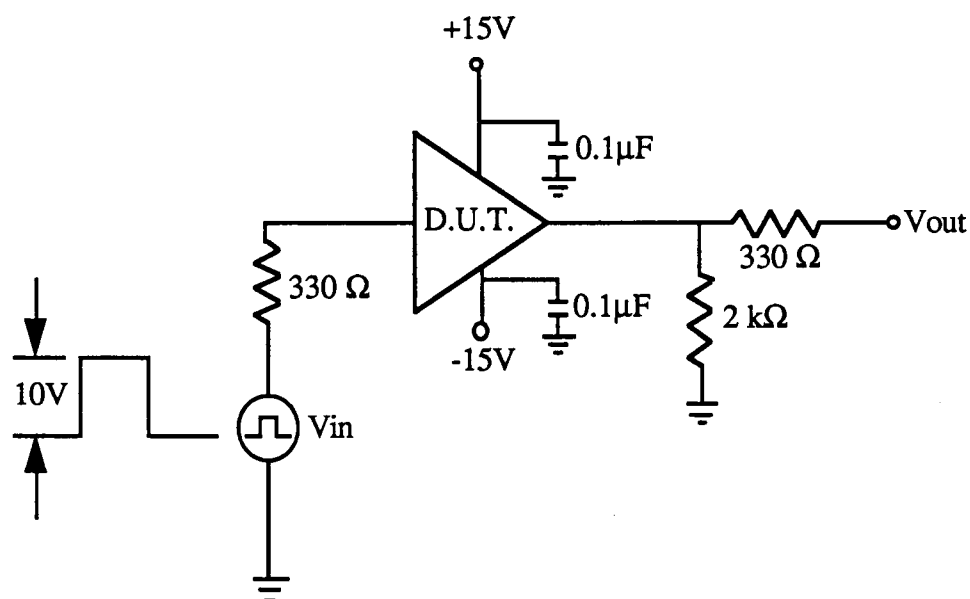


Figure 3-6. Dynamic test circuit for measuring slew rate, rise-time, and propagation time for voltage followers/buffers.

3.2.7 Voltage References

Several voltage references were evaluated. Those units tested are included in Table 3-9. Generally, all of the very high precision references either failed, or showed excessive voltage drift. The most consistently low-drift reference was the TL431, manufactured by Texas Instruments, Inc. However, the same device from Motorola Semiconductor indicated excessive drift, which indicates some significant differences in processing technology between the two manufacturers. Although the TL431 device is useful for a general reference, it is not suitable for a precision application such as an A/D converter reference. A 12-bit A/D converter would require a temperature coefficient $< 10 \text{ ppm} / ^\circ\text{C}$, which is not obtainable with the TL431 device.

The IN827A reference also indicated a low drift, but the manufacturer was unknown (these were units obtained from ORNL stores). However, the MZ640 devices are identical in fabrication as the IN827A units, yet they indicated excessive drift! Thus, it is apparent that the requirement for a radiation-hard low-drift, low temperature-coefficient reference has not been achieved. The LM199 and REF-01 devices were not evaluated; however, similar units have been irradiated by Jet Propulsion Laboratories [15], and exhibited drifts of $> 20 \text{ mV}$.

Table 3-9. Radiation test results for voltage references.

Part Number	Manufacturer	Description	≥ 10 Megarad Effects
AD584KH	Analog Devices	Precision, ± 15 ppm/ $^{\circ}$ C $V_{out} = 10.0V$ Band-gap (BG) reference	$\Delta V = -34.78$ mV (1.215V), $\Delta V_{out} = 0.2368V$ to 0.5742V, Δ Line regulation = 10.28 mV/V (10V)
AD588AD	Analog Devices	High precision adjustable zener, ± 1.5 ppm / $^{\circ}$ C, Amplifier output	-23.0 mV $\leq \Delta V_{out} \leq$ -5.3 mV Δ Line regulation = 2 mV/V (10V)
IN827A	?	Precision, ± 10 ppm / $^{\circ}$ C 6.2V at 7.5 mA	-2.1 mV $\leq \Delta V_{ref} \leq -1.0$ mV
LM199	National Semiconductor	6.95V IC, ± 0.5 ppm / $^{\circ}$ C, Temperature controlled substrate ($\approx 140^{\circ}$ C)	(To be tested)
LM336Z	National Semiconductor	BG = 2.5V, Fixed, ± 35 ppm / $^{\circ}$ C	$\Delta V_{ref} = 25$ mV
LM385-1.2	National Semiconductor	BG = 1.235V, Micropower, ± 20 ppm / $^{\circ}$ C	$V_{ref} = 2.1V$ to 2.5V Failed
LM385-2.5	National Semiconductor	BG = 2.5V, Micropower, ± 20 ppm / $^{\circ}$ C	$\Delta V_{ref} = 0.1V$ to 0.4V Failed
MZ640	Motorola	Precision, ± 5 ppm / $^{\circ}$ C 6.2V at 7.5 mA	$\Delta V_{ref} = -26$ mV
REF-01	PMI	10V IC, ± 8.5 ppm / $^{\circ}$ C,	(To be tested)
TL431	Motorola	BG = 2.5V, ± 50 ppm / $^{\circ}$ C, Adjustable zener	$\Delta V_{ref} = +65$ mV $\Delta R_z = 0.33 \Omega$ to 5 Ω
TL431	Texas Instruments	BG = 2.5V, ± 50 ppm / $^{\circ}$ C, Adjustable zener	$\Delta V_{ref} = -0.4$ mV to -0.8 mV $\Delta R_z = 0.22 \Omega$ to 0.7 Ω

CHAPTER IV

PART II: EVALUATION AND IRRADIATION OF CMOS MOSIS CHIP

4.1 INTRODUCTION

The second phase of this research covered the time period from April 1989 to January 1990. The goal of the research was to investigate the possibilities of using the low-cost MOSIS program to do initial design and evaluation for CMOS transistors that might be useful in the Superconductor Super-Collider (SSC) program. The SSC concept involves the eventual construction of a 53-mile diameter accelerator in Texas (anticipated completion date in late 1990's) that would bring two beams of high-energy protons into collision (occurring every 16 nsec), with the resultant energies in the scattered elements being in the 1 TeV (1 trillion electron-volts) range.

The engineering problems encountered in the design of both detectors and electronics in such an endeavor are enormous. Not only will the circuitry required be very high frequency, but also the circuits are required to be low-mass, operate at very low-power levels, and be immune to radiation products exceeding (in circuits near the center of the reaction zone) 10 megarad (gamma) total dose, as well as heavy particle bombardments (displacement damage resulting) exceeding 10^{13} particles/cm². Obviously, very special radiation-hardened semiconductor IC processes will be required for the final electronic circuits and detectors. However, for early circuit evaluations it is useful if inexpensive modes of fabricating IC devices are available, since radiation-hard analog IC process runs are available from very few manufacturers (at present only UTMC, Sandia Laboratories, AT&T, and Harris Semiconductor), have long lead times, and are very expensive ($\geq$ \$100,000). For this reason the low-cost MOSIS fabrication program, presently available at

both UTK and ORNL, was used. There are presently available only MOS or GaAs processes in MOSIS (a bipolar is not available). Thus, the CMOS process was chosen for initial evaluation of analog components.

The test chips were constructed using the MAGIC layout program, and the SUN-3/160 workstation at ORNL. Two layouts were sent to MOSIS for evaluation, in July and August, 1989. The chip design and layout were accomplished by Gary Alley and Danny Newport at ORNL. The measurements and evaluations in this thesis involve chips from these two runs. The IC chip processing was accomplished by Orbit Semiconductor, Inc., using their basic $2\mu\text{m}$ CMOS process, having a p-well (n-substrate), with both n^+ and p^+ polysilicon and double metal contacts and interconnects.

Since the basic circuits required for preamplification, discrimination and analog storage in the SSC domain are analog in nature, the test chips designed involved a dual-device layout with different width/length geometries. Such dual MOS devices would be useful as input stage components for preamplifiers and discriminators. Also, the availability of the n^+ diffusion with the thin (typically $3\mu\text{m}$ deep) lightly-doped p-well ($\approx 10^{16} \text{ cm}^{-3}$) creates the possibility of a lateral npn (as well as a vertical npn) construction. Hence, several npn configurations were also included in the IC chip design.

Figure 4-1 indicates a common-centroid (quad configuration) geometry that was used in the layout for both CMOS and the lateral npn bipolar transistors. With this chip layout it is possible to obtain very low offset voltages as well as excellent temperature drift characteristics. Figure 4-2 indicates a typical construction for the NMOS transistor, while Figure 4-3 shows the cross-section construction for the lateral npn. Since the polysilicon layer was used to pattern the separation of the n^+ emitter and collector regions, the design rules for the minimum polysilicon width determined the base width for the bipolar. Since the particular MOSIS run used a design rule of $\lambda = 1 \mu\text{m}$, and since the poly width was 2λ , the bipolar base width was $2 \mu\text{m}$. Unfortunately, from Figure 4-3 note that the n^+

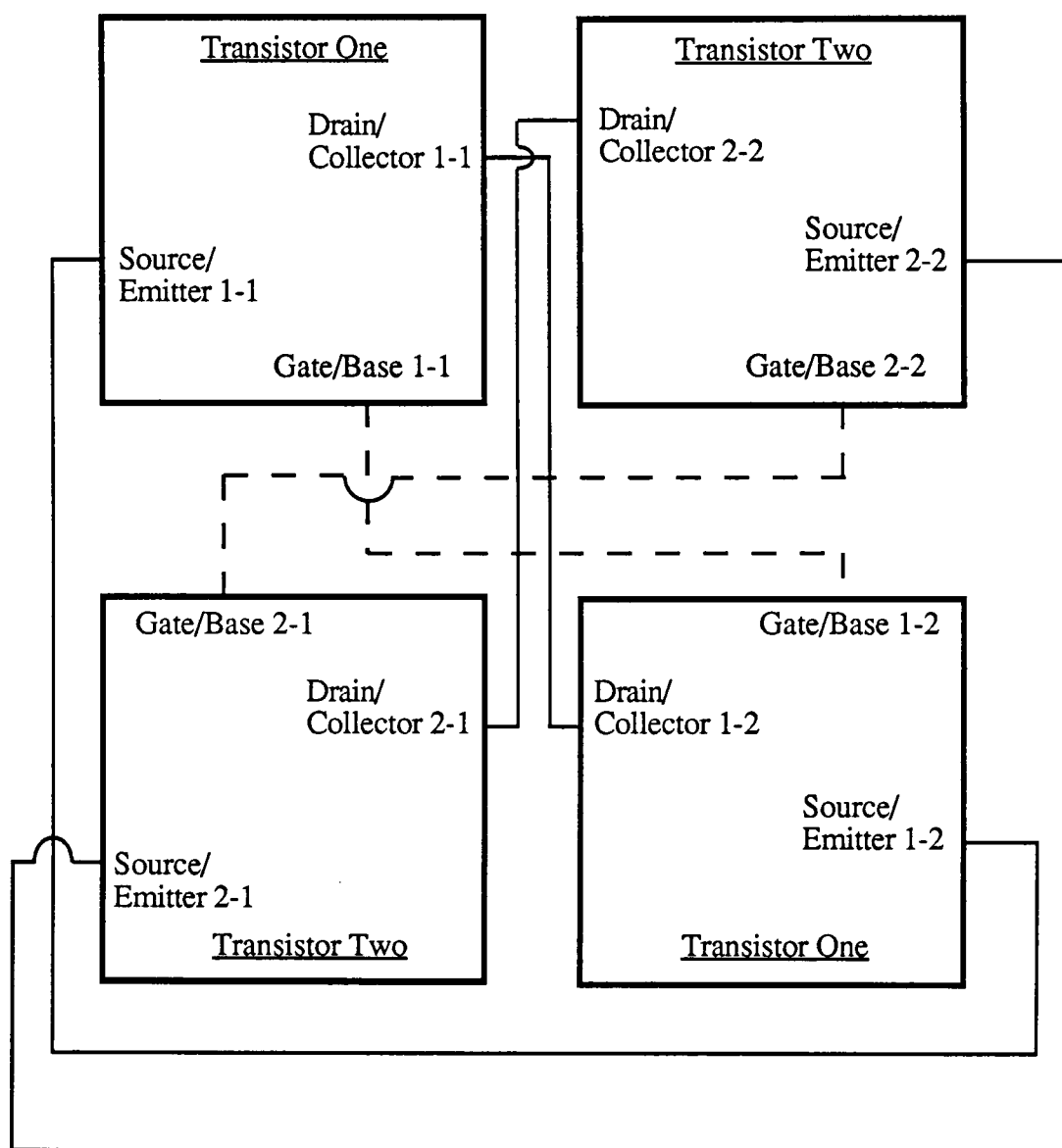
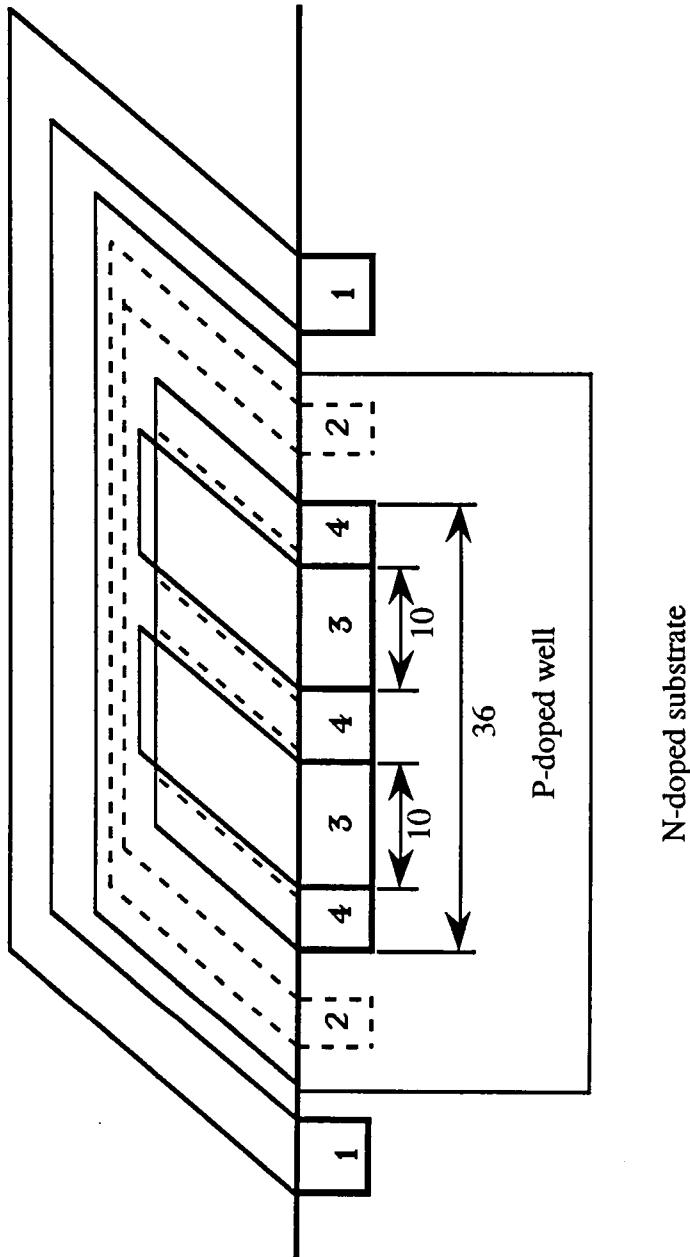
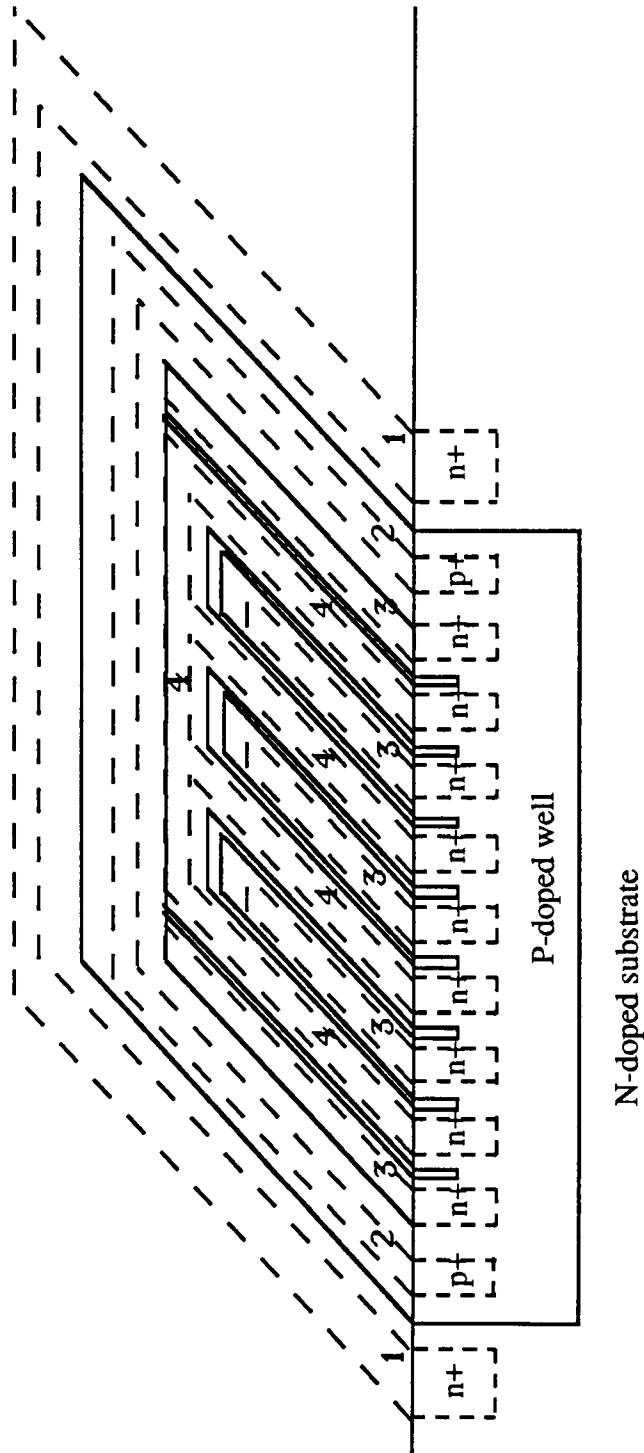


Figure 4-1. Common centroid geometry for the transistor layout on MOSIS test chips.



1. N⁺-doping strip around the P-well served as an outer guard ring for the device.
2. P-well has metal contact and underlying p⁺-diffusion around the diffusions of polysilicon and n-doping and serves as an inner guard ring for the device.
3. Actual NMOS transistor physical dimension which is the intersection of the polysilicon and the n-diffusion regions. These two strips have the drawn width of 10λ and length of 25λ , where $\lambda = 1\mu\text{m}$.
4. The dimension of 36 units by 25 units is identified for the region of the n⁺-diffusion block, which defines the source and drain regions.

Figure 4-2. Cross-section of the basic NMOS silicon layout used in MAGIC.



1. N-doped substrate has metal contact around the whole device served as an outer guard ring for the transistor, on top of an n+ diffusion.
2. P-doped well has metal contact around the entire device over a p+ diffusion, and is the base region for the bipolar.
3. Inside polysilicon separates the collector region (3) and the emitter region (4) in order to generate a lateral transistor action. Unfortunately, a substrate (vertical) npn exists as well.

Figure 4-3. Cross-section of the basic lateral npn BJT silicon layout used in MAGIC.

diffusion coupled with the p well and n substrate forms a vertical (substrate) npn as well. Therefore, a forward bias of the lateral npn emitter-base (E-B) junction will also forward-bias the vertical npn E-B as well; hence, electron current will be lost to the substrate. Normally, in a typical bipolar process the effects of the vertical npn can be negated by using an n^+ buried layer at the p-well to n-substrate interface. This buried layer produces a bending of the energy bands, with a resultant retarding electric field for vertically diffused electrons, thereby reducing the current gain (β) of the vertical device. Unfortunately, an n^+ buried layer was not available in the standard CMOS fabrication program.

4.2 IC LAYOUT

The two MOSIS chip designs are shown in Figure 4-4 and 4-5. Table 4-1 describes the layout dimensions for the CMOS transistors and the bipolar transistors. The particular layout technique used for each of these structures is shown in Figure 4-6 through 4-11 for the CMOS devices and Figure 4-12 through 4-14 for the bipolar devices.

4.3 DC PARAMETER EVALUATIONS

The essential dc parameters measured included threshold voltage (V_T) with various voltages between the source and substrate, Early voltage (V_A) and small-signal transconductance (g_m) with four different bias currents were measured by using the Hewlett-Packard 4145B Semiconductor Parameter Analyzer for both CMOS and bipolar devices. Internal power supply voltages of ± 5 V were used to bias the MOS devices. While one side of a dual transistor was tested, the gate (or base) of the other side transistor was grounded to remove that device from test. Offset voltage with various drain currents

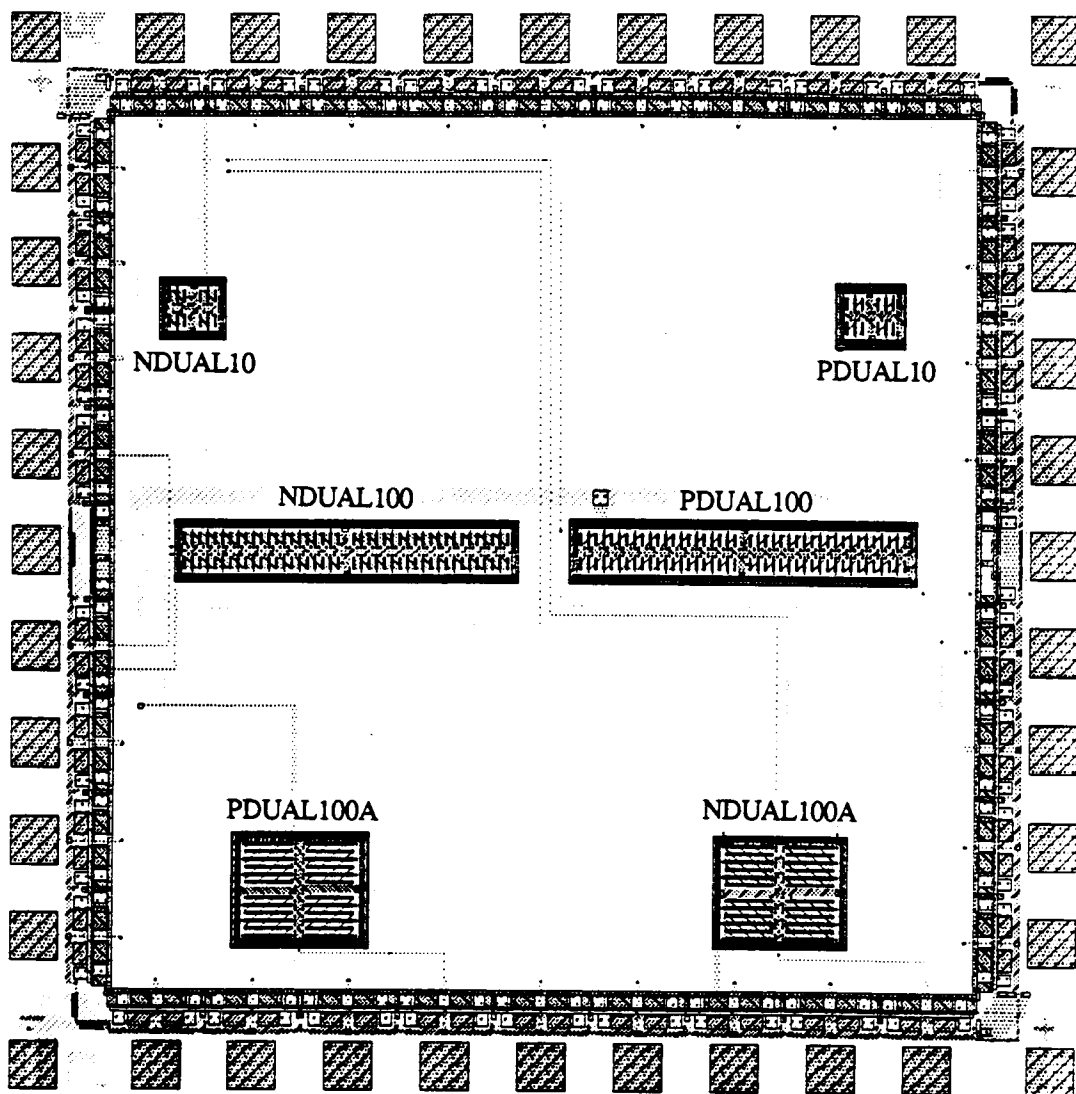


Figure 4-4. MOSIS layout for RADMOS chips includes NDUAL10, NDUAL100, NDUAL100A, PDUAL10, PDUAL100, and PDUAL100A.

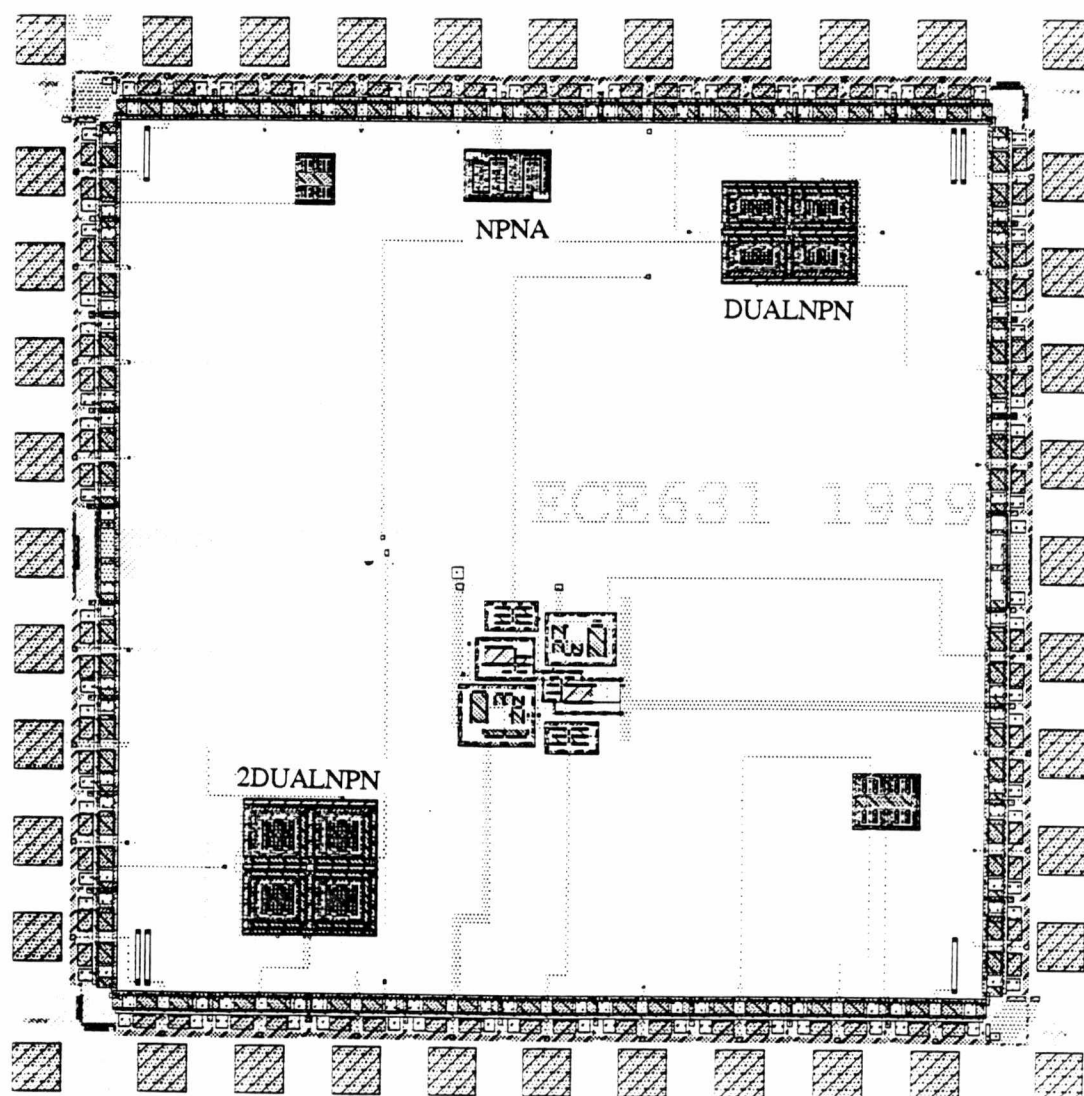


Figure 4-5. MOSIS layout for RADWELL chips includes NPNA, DUALNPN, 2DUALNPN, and others.

Table 4-1. List of MOSIS transistors tested.

Device Name	Manufacturer	Descriptions
NDUAL10	Orbit Semiconductor, Inc.	Dual, N-channel, $W/L = (25 \times 4) / 10$, Dim = $140 \mu\text{m} \times 130 \mu\text{m}$
NDUAL100	Orbit Semiconductor, Inc.	Dual, N-channel, $W/L = (25 \times 40) / 10$, Dim = $716 \mu\text{m} \times 130 \mu\text{m}$
NDUAL100A	Orbit Semiconductor, Inc.	Dual, N-channel, $W/L = (100 \times 10) / 10$, Dim = $236 \mu\text{m} \times 280 \mu\text{m}$
PDUAL10	Orbit Semiconductor, Inc.	Dual, P-channel, $W/L = (25 \times 4) / 10$, Dim = $146 \mu\text{m} \times 136 \mu\text{m}$
PDUAL100	Orbit Semiconductor, Inc.	Dual, P-channel, $W/L = (25 \times 40) / 10$, Dim = $722 \mu\text{m} \times 136 \mu\text{m}$
PDUAL100A	Orbit Semiconductor, Inc.	Dual, P-channel, $W/L = (100 \times 10) / 10$, Dim = $242 \mu\text{m} \times 286 \mu\text{m}$
NPNA	Orbit Semiconductor, Inc.	Single, NPN Dim = $184 \mu\text{m} \times 110 \mu\text{m}$
DUALNPN	Orbit Semiconductor, Inc.	Dual, NPN Dim = $280 \mu\text{m} \times 216 \mu\text{m}$
2DUALNPN	Orbit Semiconductor, Inc.	Dual, NPN Dim = $278 \mu\text{m} \times 284 \mu\text{m}$

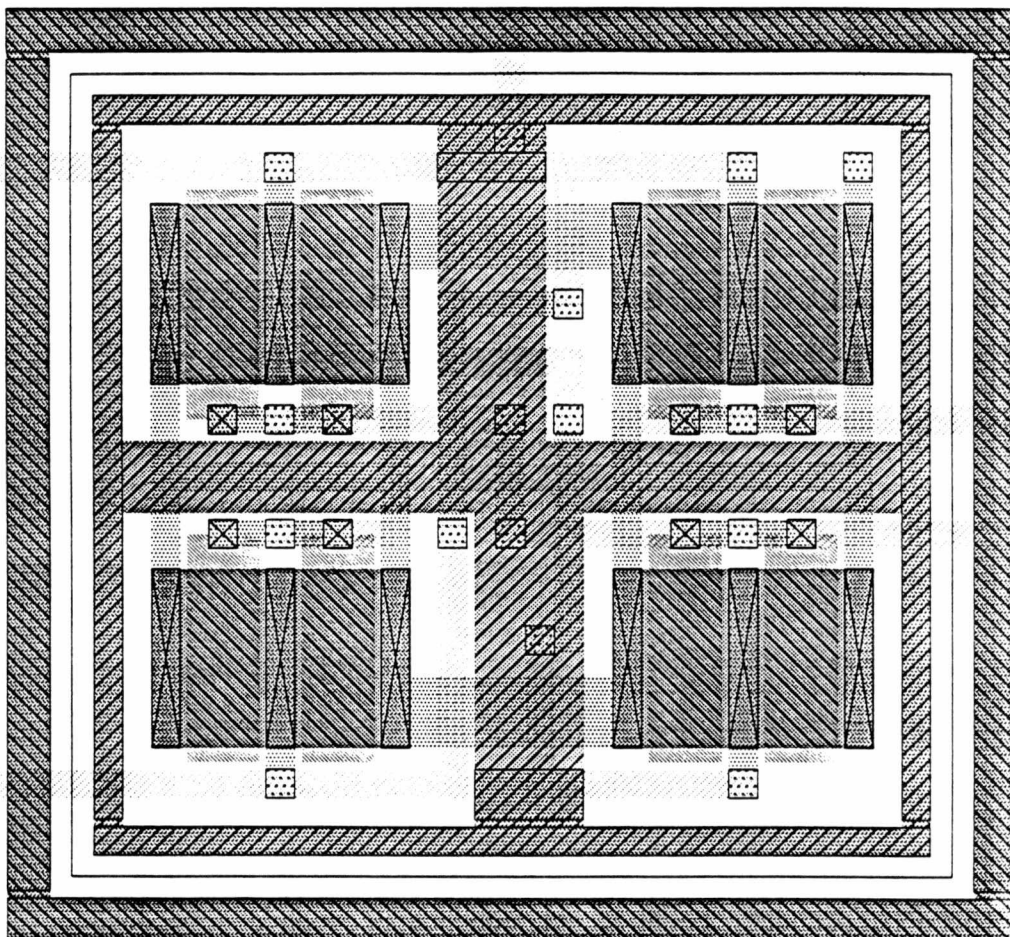


Figure 4-6. MOSIS transistor - NDUAL10 layout in MAGIC.



Figure 4-7. MOSIS transistor - NDUAL100 layout in MAGIC.

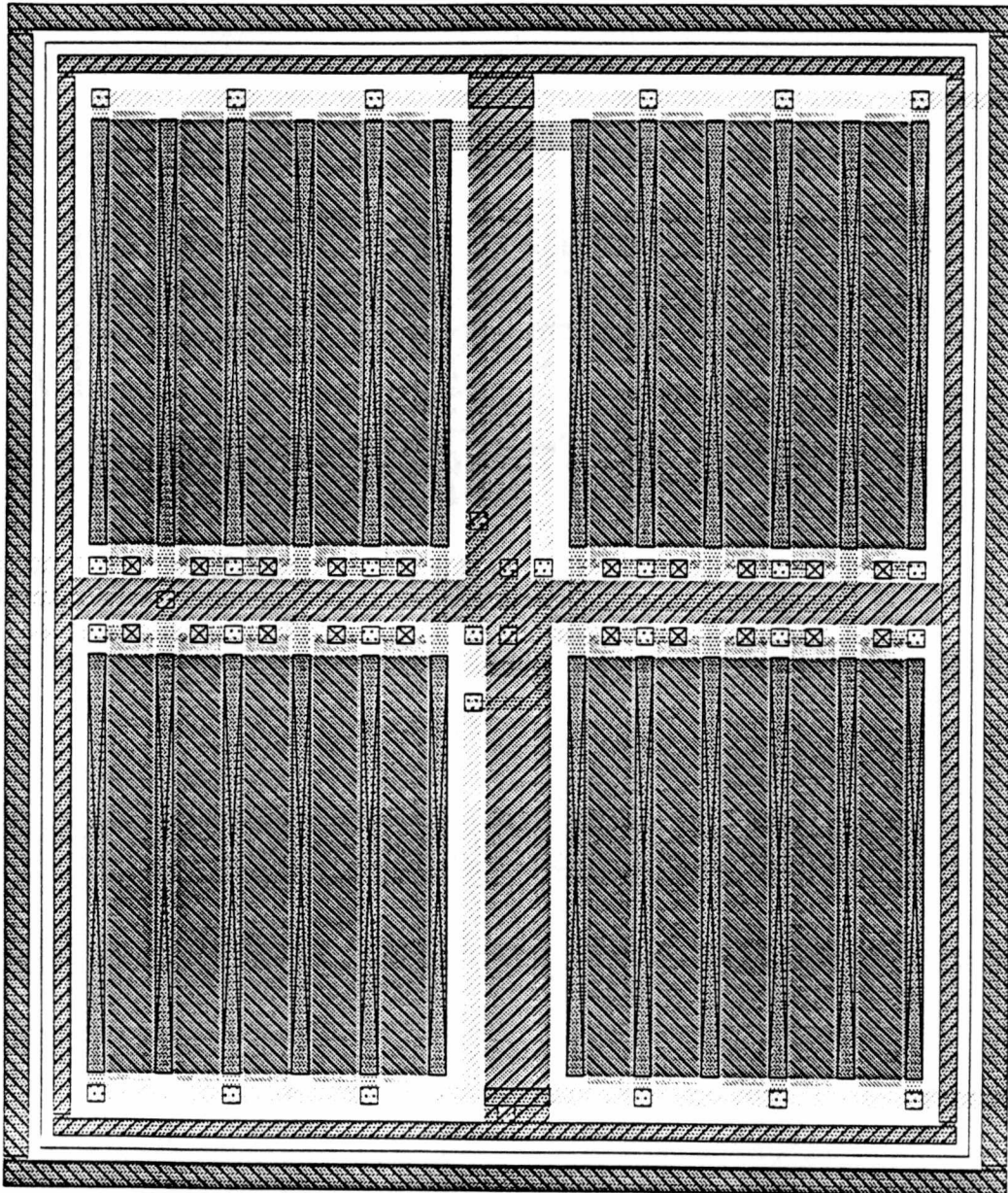


Figure 4-8. MOSIS transistor - NDUAL100A layout in MAGIC.

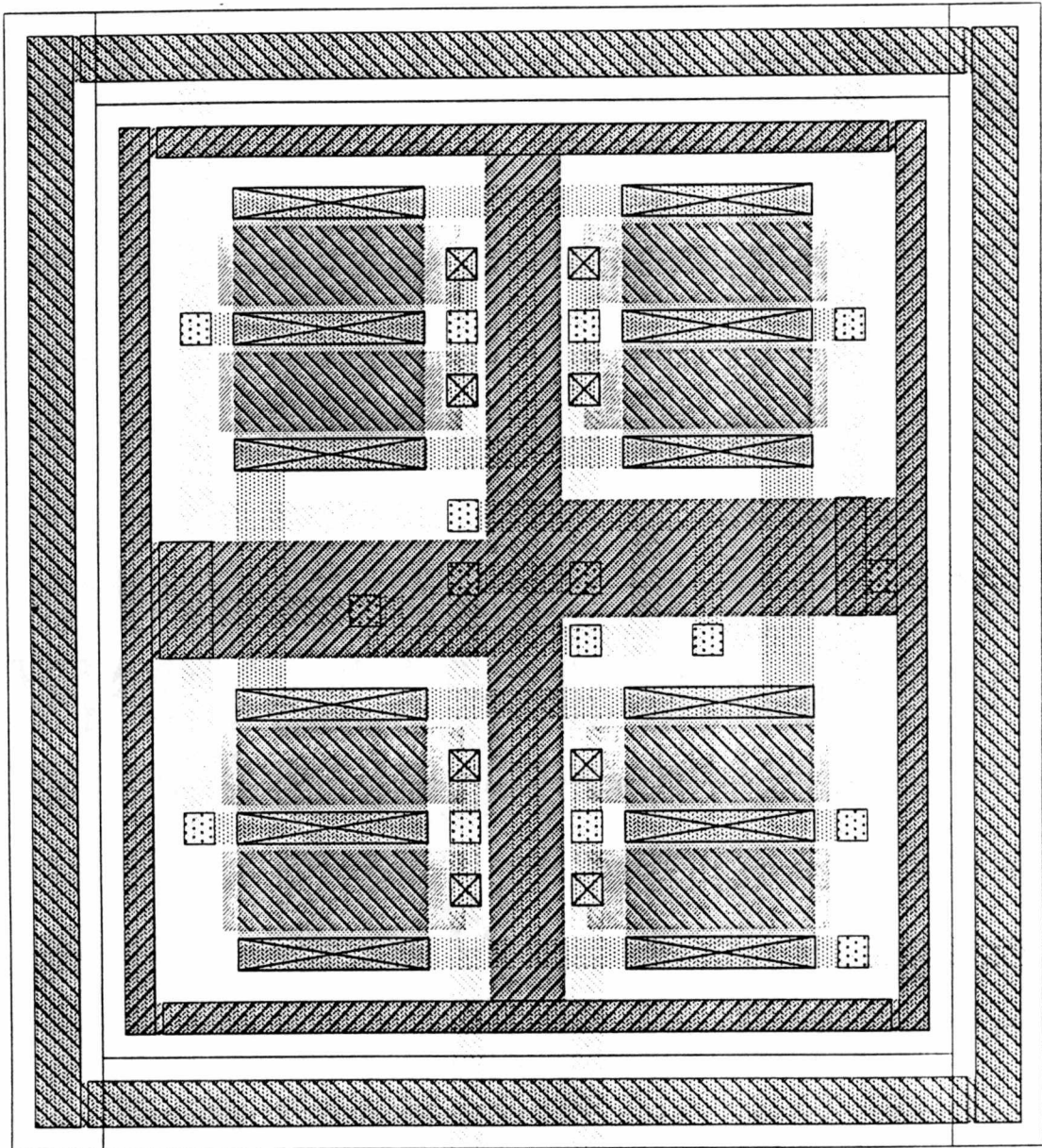


Figure 4-9. MOSIS transistor - PDUAL10 layout in MAGIC.

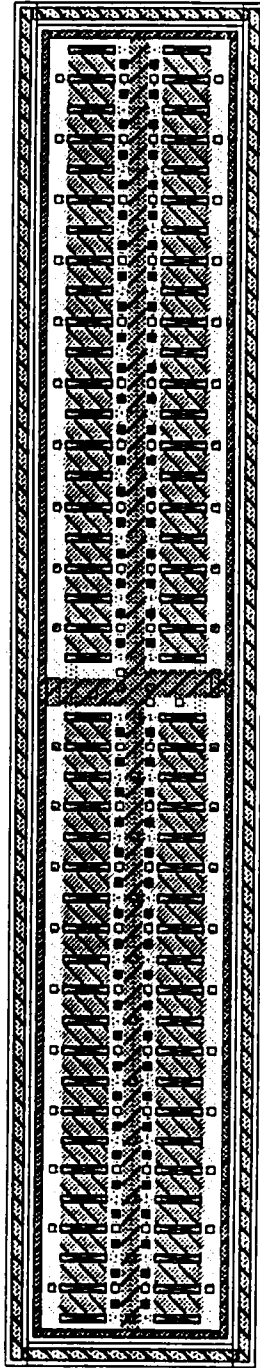


Figure 4-10. MOSIS transistor - PDUAL100 layout in MAGIC.

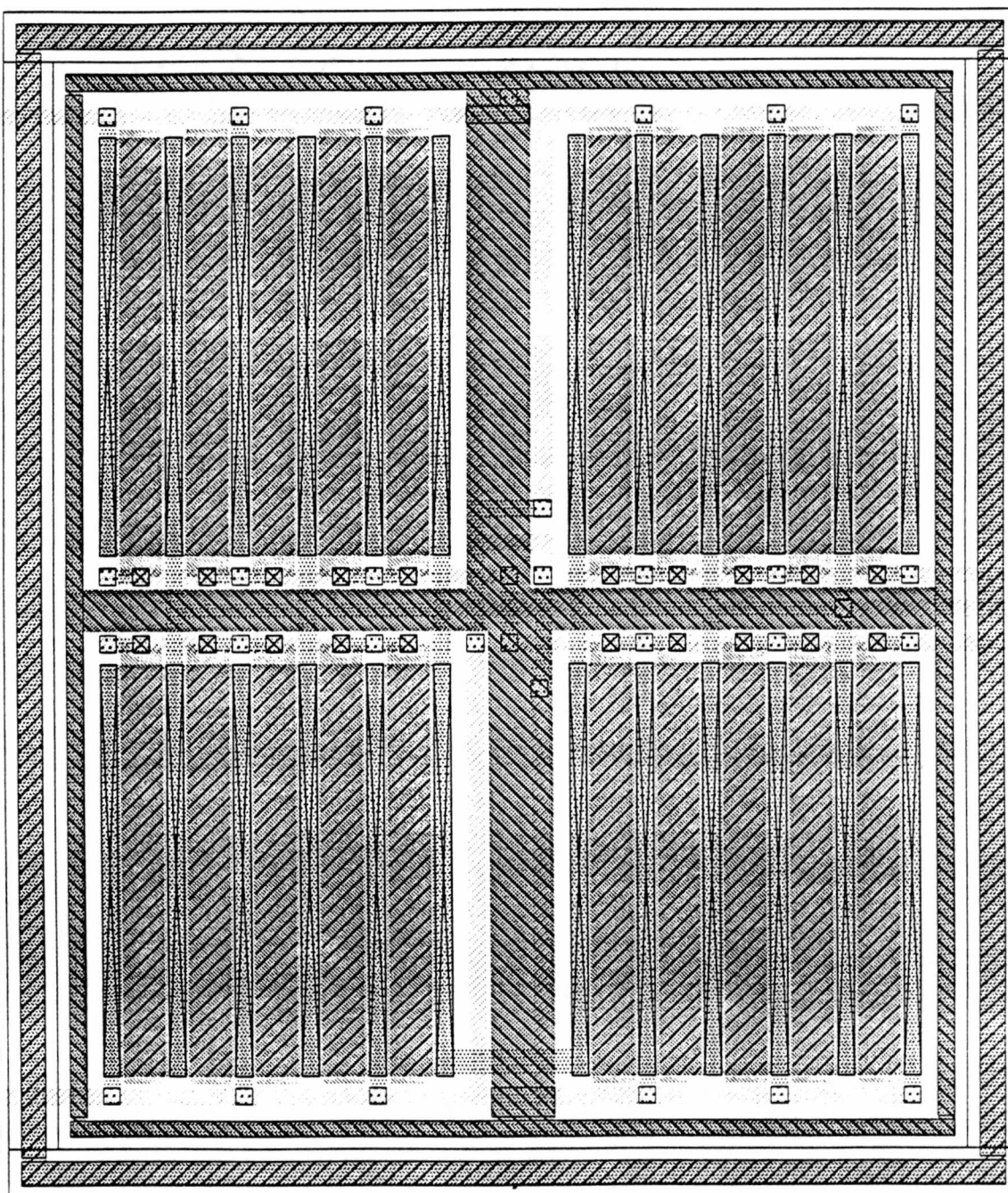


Figure 4-11. MOSIS transistor - PDUAL100A layout in MAGIC.

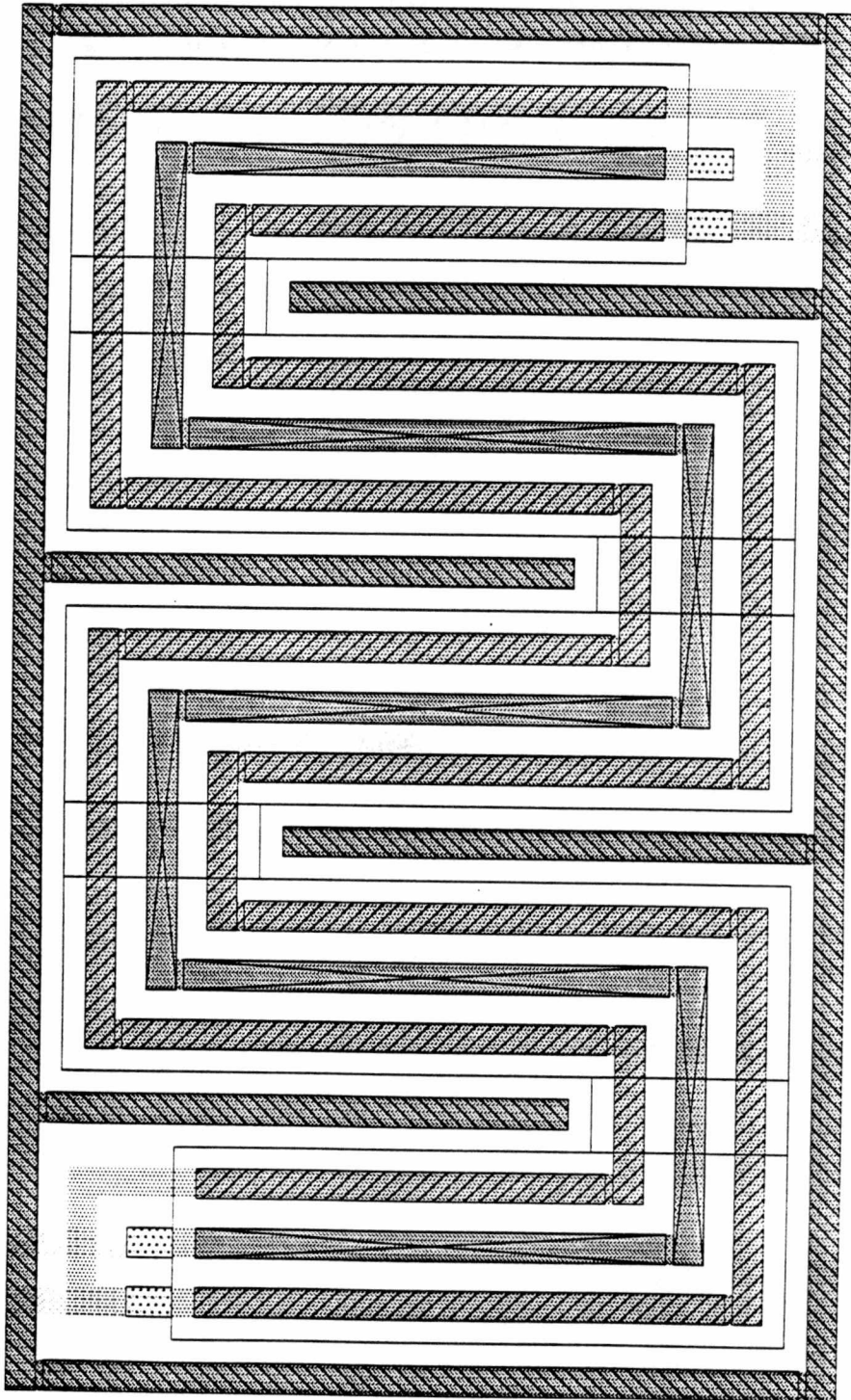


Figure 4-12. MOSIS transistor - NPNA layout in MAGIC.

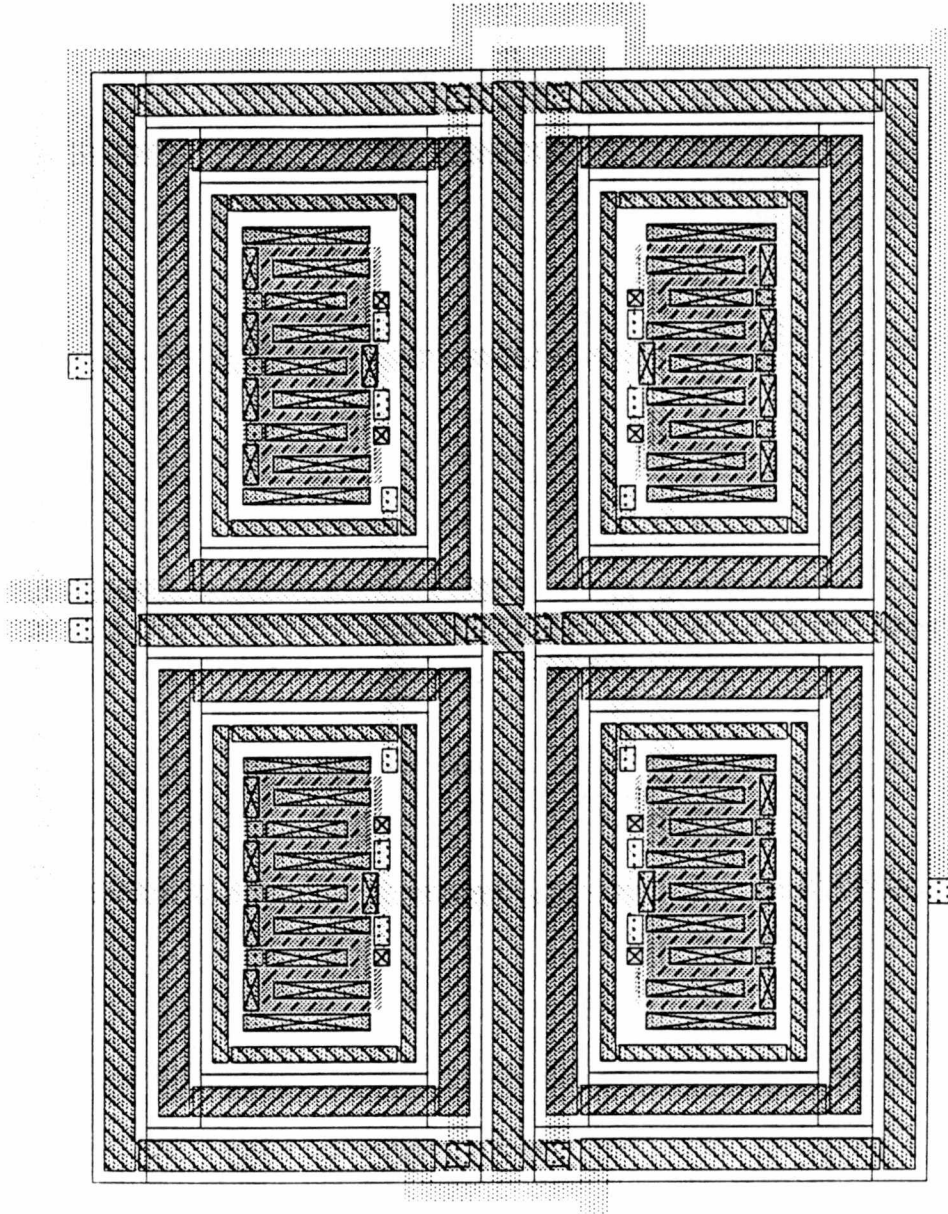


Figure 4-13. MOSIS transistor - DUALNPN layout in MAGIC.

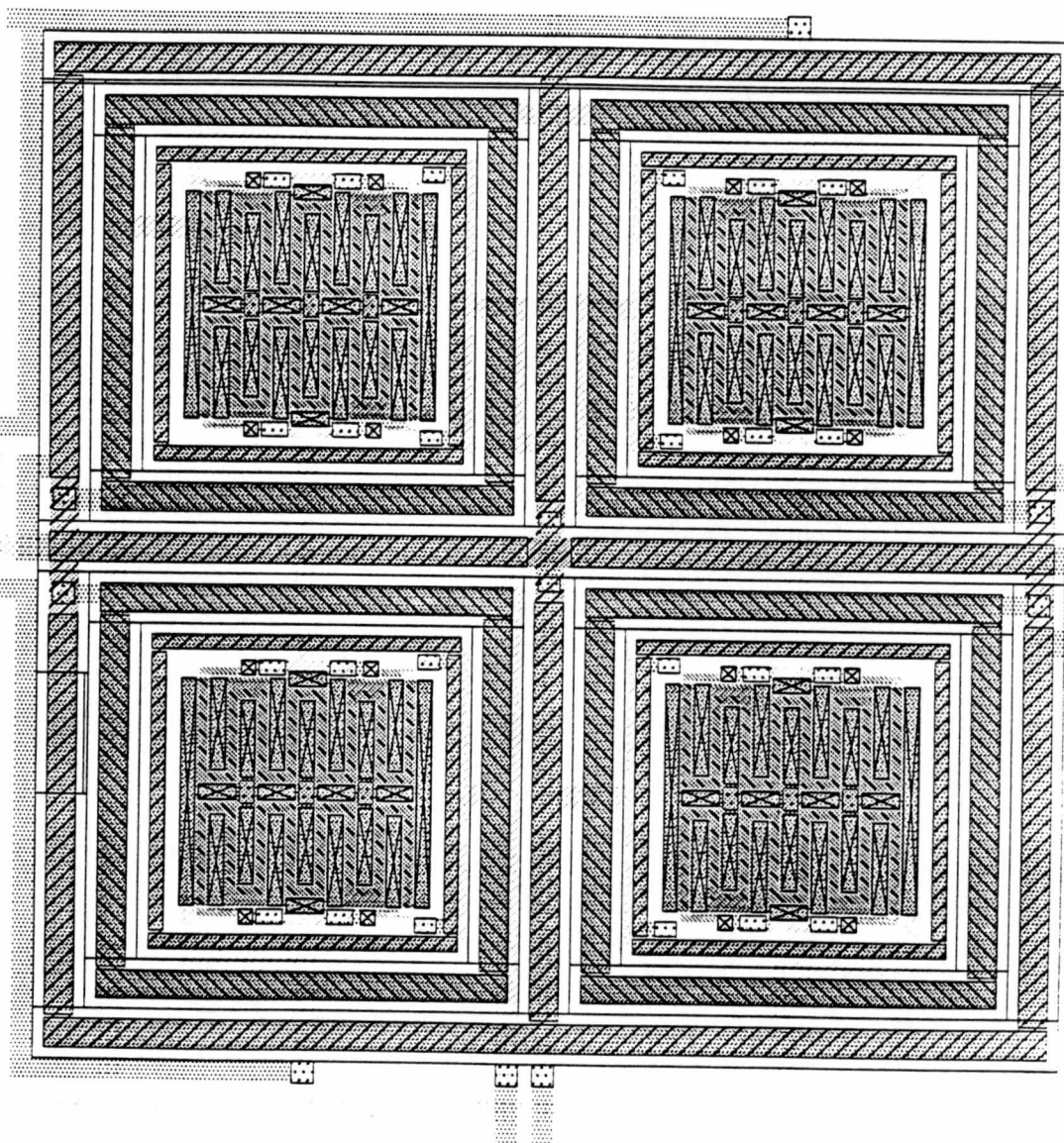


Figure 4-14. MOSIS transistor - 2DUALNPN layout in MAGIC.

were obtained by setting up the operational-amplifier-like circuits as shown in Figure 4-15. Figure 4-15 (a) is for n-channel MOSFET's while (b) is for the p-channel MOSFET's. The operation for different bias currents ($I_D = 10 \mu A, 100 \mu A, \text{ and } 1 \text{ mA}$) is obtained by a simple two-transistor current source [16]. If one neglects junction leakage currents, and assumes identical transistors (2N5089), then the collector currents of both transistors should be equal and can be adjusted by the resistor R_{ref} to obtain desirable bias currents for the dual differential input stage consisting of the dual CMOS (M1 and M2) or npn transistors. The offset voltage V_{OS} is defined as the difference in gate-to-source voltage of the dual transistors. It is amplified through the overall circuit closed-loop gain (A_1) and is expressed as the output voltage for the circuit of Figure 4-15 as

$$V_{OS} = V_{GS1} - V_{GS2} = V_{out} / A_1$$

where

$$A_1 = 1 + (R_{F1} / R_1) = 26.1$$

A list of nominal values of resistors used in Figure 4-15 is given in Table 4-2. Due to increase in offset voltage after radiation, the gain A_1 had to be decreased to avoid saturation of the overall circuit.

For bipolar transistor dc measurements, since the lateral npns had very low current gain (β or h_{FE}), all npn's had to be evaluated as substrate (vertical) npn's by connecting substrate nodes to the highest potential node for each measurement. Parameters measured were I_C , I_B , h_{FE} , V_A , as well as current gain-bandwidth product (f_T), and base resistance (r_B) used the Hewlett Packard HP4192A LF Impedance Analyzer. Also junction capacitances (C_{CB} , C_{BE}) were measured using the HP4280A 1MHz C Meter / C-V Plotter.

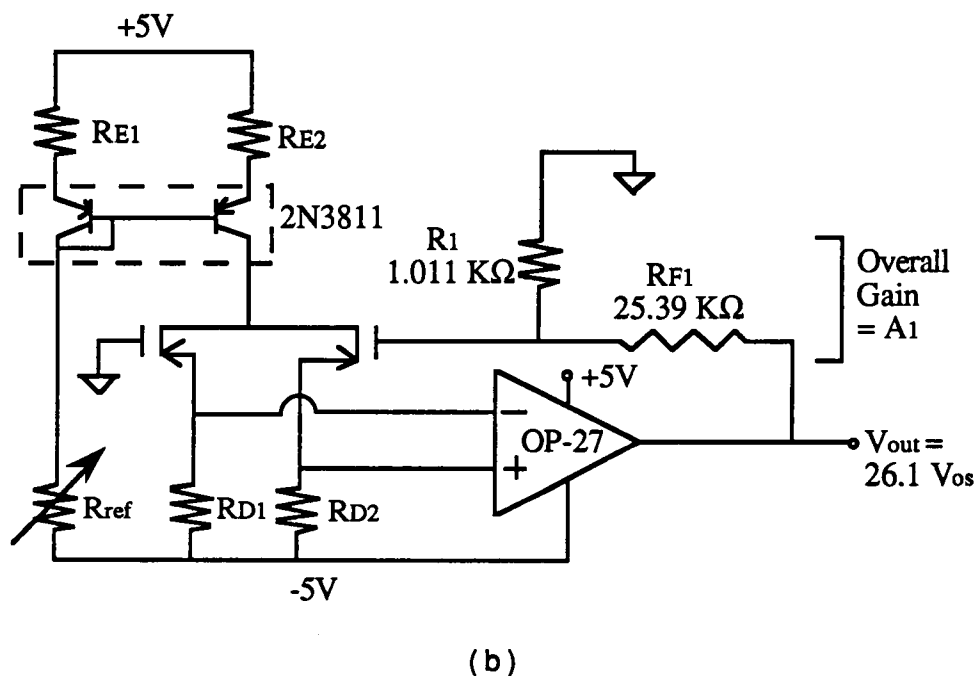
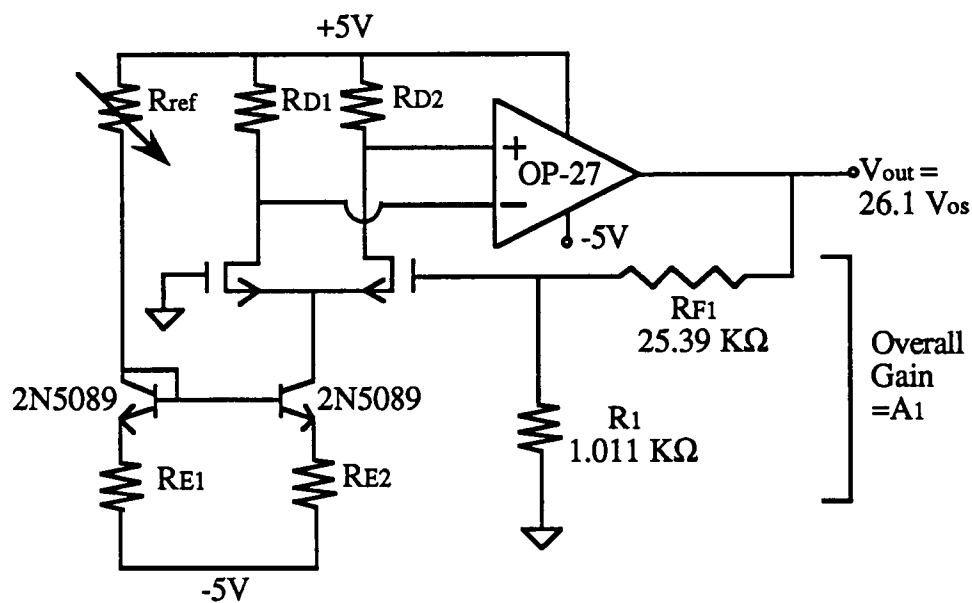


Figure 4-15. Fundamental block for measuring the offset voltage and noise of the dual MOS transistors and npn transistors. (a) Test circuit for the n-channel MOSFETs and (b) Test circuit for the p-channel MOSFETs. The lateral npn transistors also use the circuit of (a).

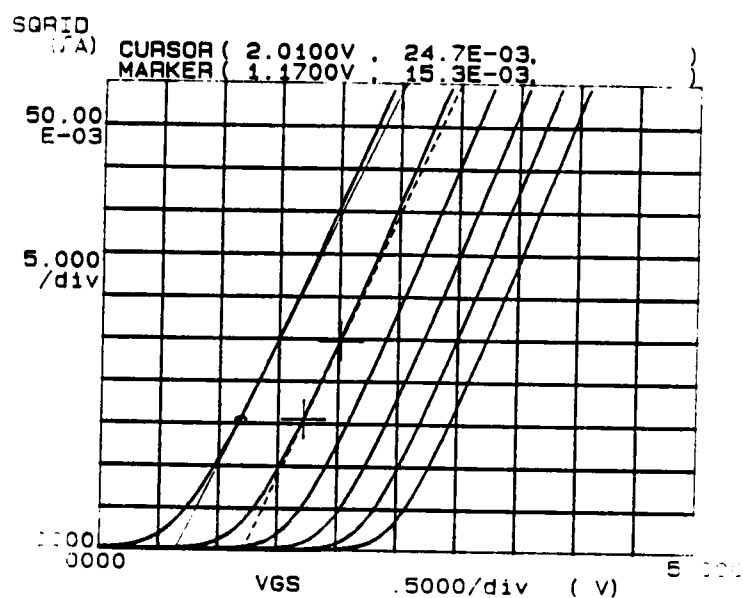
Table 4-2. List of nominal values of resistors used in the circuit of Figure 4-15.^a

Bias Current (I_D)	$R_{E1} = R_{E2}$	R_{ref}	$R_{D1} = R_{D2}$
10 μA	1 k Ω	464 k Ω	200 k Ω
100 μA	1 k Ω	45.5 k Ω	20 k Ω
1 mA	1 k Ω	3.65 k Ω	2 k Ω

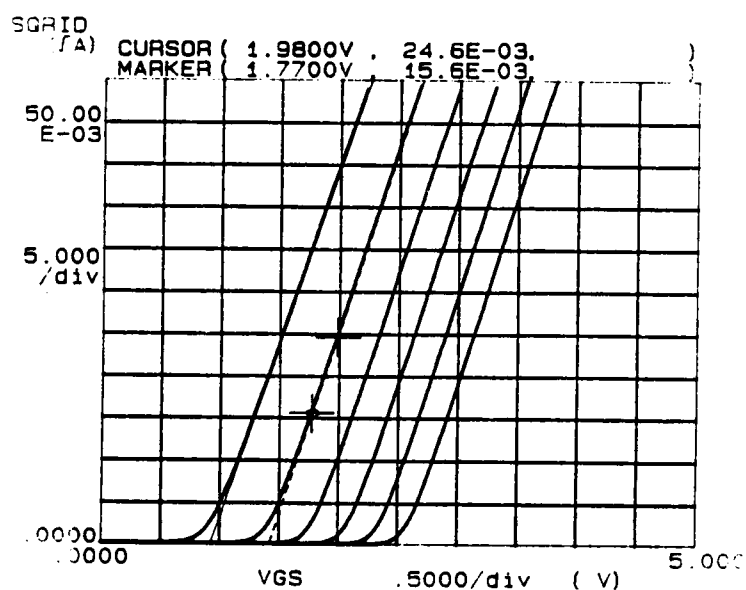
(a). Because eight different dual transistors were tested, the actual resistors used during measurement deviated slightly from device to device.

For noise measurements, the basic circuits of Figure 4-15 were attached to an additional gain circuit ($A_2 = 1 + (R_F / R_1) = 21$), as well as an active Twin-Tee filter (circuit developed by Dr. E. J. Kennedy, January 1979) and a true-rms voltmeter, as shown in Figure 4-16.

Some examples of the typical data obtained using the HP 4145B Semiconductor Parameter Analyzer is shown in Figures 4-17 through 4-20. Figures 4-17 and 4-18 show the typical plots of $\sqrt{I_D}$ versus V_{GS} with constant $|V_{DS}|$ for MOSFET's, where the threshold voltages for various substrate bias is extrapolated from the before- and after-irradiations. Additional explanation of the plots is given in later section 4.4.1.2. Figure 4-17 exhibits the characteristic of sample 1A of NDUAL100 devices, and Figure 4-18 exhibits that of PDUAL100 devices. Figure 4-19 and 4-20 shows the typical plots of $\log I_C$ and $\log I_B$ versus V_{BE} for npn bipolar devices pre- and post-radiations. Figure 4-19 exhibits the characteristics of sample 2 of NPNA devices, and Figure 4-20 exhibits that of sample 1A of DUALNPN devices.

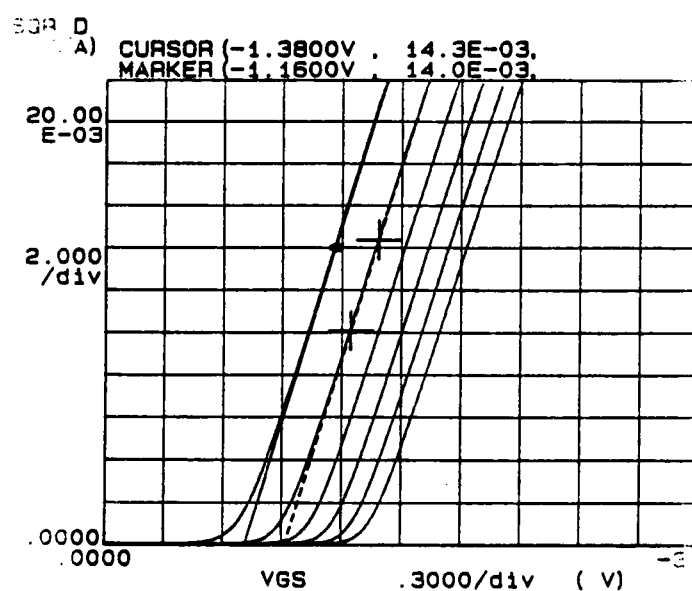


(a)

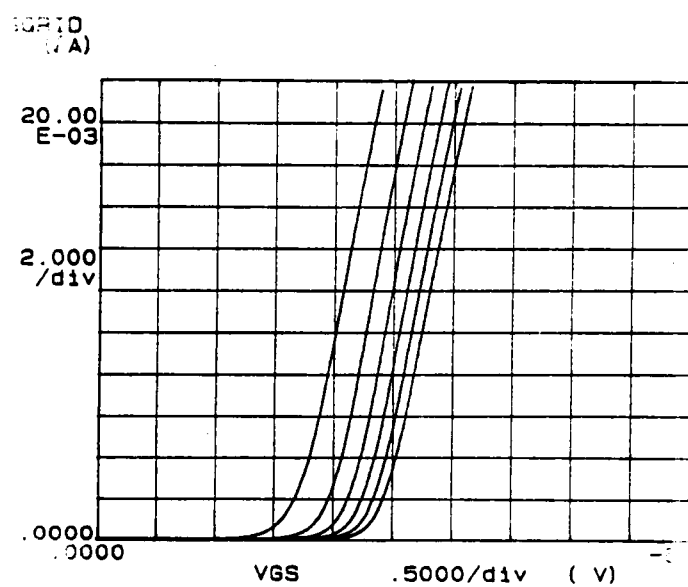


(b)

Figure 4-17. Plot of square root of drain current as a function of source-substrate voltage versus gate-source voltage for sample 1A of NDUAL100 devices, for (a) before and (b) after radiations. V_{sub} ranges from 0 to -5V in 1V increments.

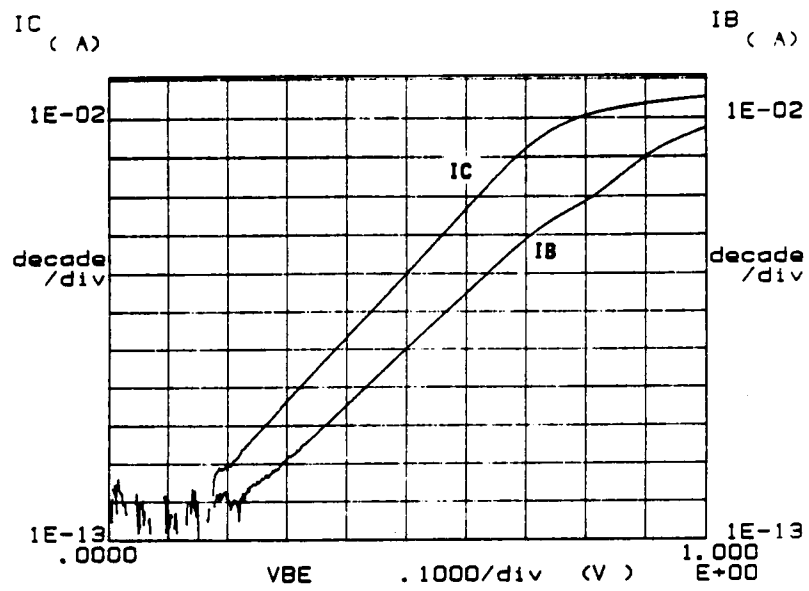


(a)

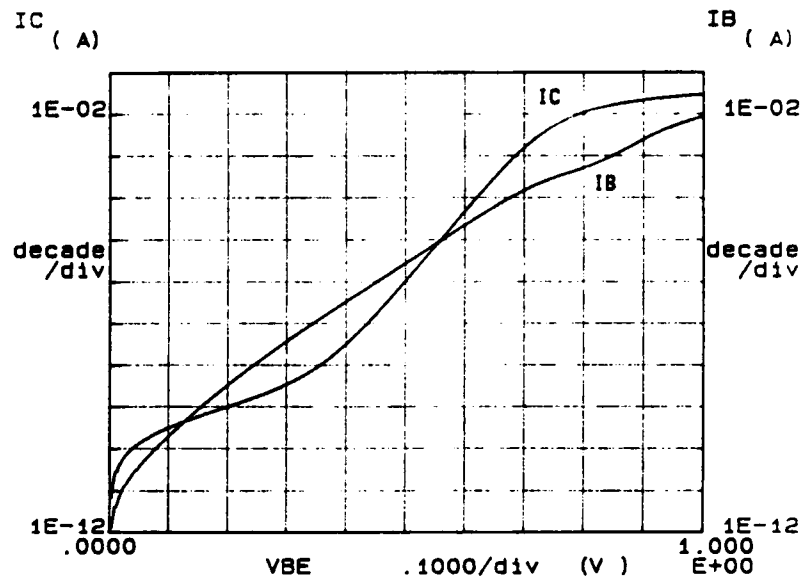


(b)

Figure 4-18. Plot of square root of drain current as a function of source-substrate voltage versus gate-source voltage for sample 1A of PDUAL100 devices, for (a) before and (b) after radiations. V_{sub} ranges from 0 to -5V in 1V increments.

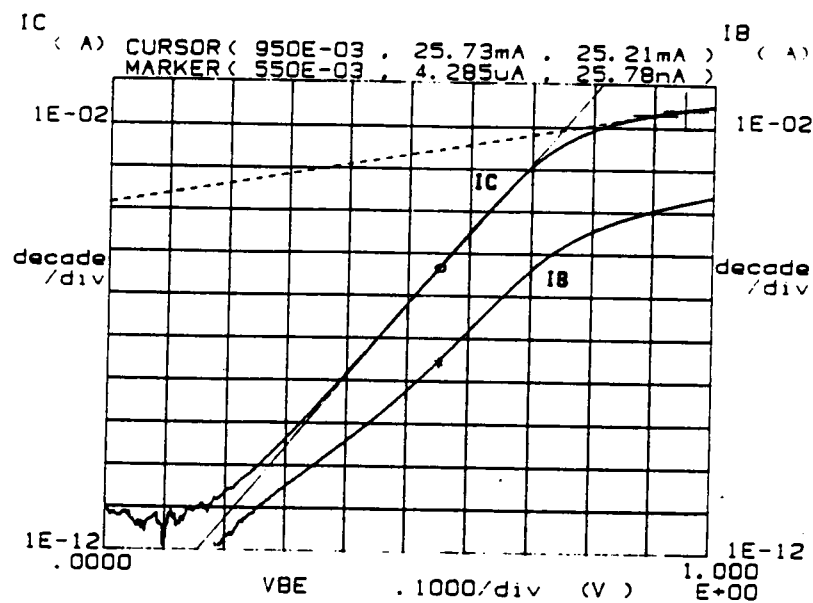


(a)

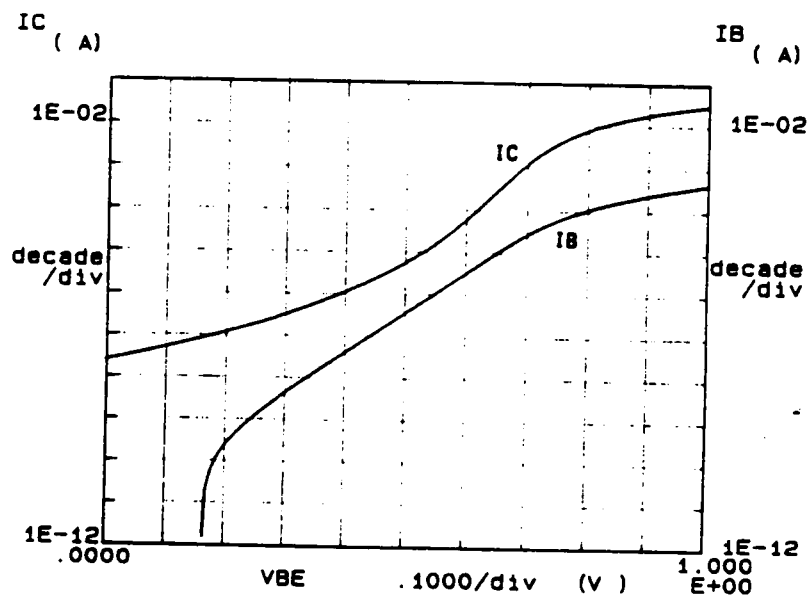


(b)

Figure 4-19. Plot of $\log I_C$ and $\log I_B$ versus V_{BE} for sample 1 of NPNA devices, for (a) before and (b) after radiations.



(a)



(b)

Figure 4-20. Plot of $\log I_C$ and $\log I_B$ versus V_{BE} for sample 1A of DUALNPN devices, for (a) before and (b) after radiations.

4.4 PRE-IRRADIATION AND POST-IRRADIATION RESULTS

Nine kinds of transistors fabricated by Orbit Semiconductor, Inc. on two MOSIS runs were tested. Two samples of each kind were evaluated before and after irradiation. There were three types of n-channel and p-channel MOSFET's, and NPN's individually.

One-side of the dual transistors from both NDUAL10 and PDUAL10 were biased during irradiation, as shown in Figure 4-21. Also one pair of the dual transistors from NDUAL100 and PDUAL100A were biased at $I_D = 100 \mu A$ during irradiation, as shown in Figure 4-14 except the 2N3811 were replaced by two of the 2N5087. The gate-source voltages of both NDUAL10 and PDUAL10 are near the values for threshold voltages (V_T) for each transistor biasing at $1 \mu A$.

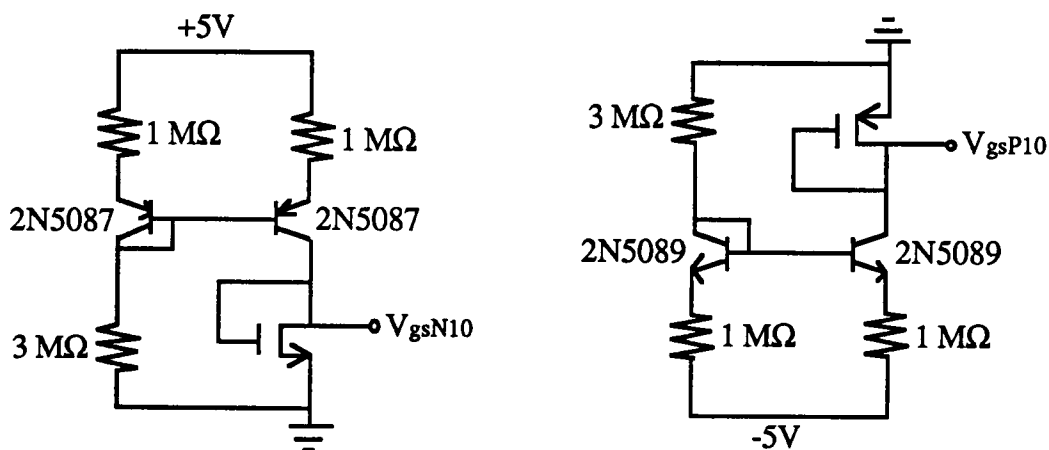


Figure 4-21. Test setups for radiation testing.

The collector and base currents of two bipolar transistors which made up the constant current source circuits decreased during radiation exposure. The lowered collector currents decreased the drain currents for MOSFET's in the circuits. Also the carrier mobility of the MOSFET's decreased and its channel length modulation effect increased due to radiation. Therefore, initially with small amount of radiation dosage, the increased V_T was observed before the radiation caused the degraded performance of the bipolar transistors. As total dosage increased, the V_{GS} kept almost constant because the decreased operating currents, voltages, and carrier mobility cancelled the effect of increased threshold voltage. Although (theoretically) monitoring these voltages should have indicated shifts in V_T due to radiation, experimentally, due to problems with the constant current source circuits the resultant monitored voltage bore no correlation with ΔV_T shifts. The devices were removed from the Gammacell irradiator after approximately 1.9 megarad total dose.

Both single-sided transistors of the NDUAL10 and PDUAL10 failed to function after the gamma-ray exposure. The biased pair transistors had more severe degradation than the ones which were in passive mode (all leads shorted). Average values were calculated to determine the effects and the significant changes because of the irradiation on these chips are summarized in Table 4-3 for changes in the significant dc parameters.

Table 4-3. Radiation effects on MOSIS transistors.

Device Name	≥ 1.9 Megarad Effects
NDUAL10	1 out of 4 units failed due to biasing Maximum $\Delta V_{OS} = 0.795$ V at $I_D = 1$ mA Maximum $\Delta V_T = 65$ mV at $V_{SB} = 0$ V
NDUAL10	Maximum $\lambda = 0.038$ V ⁻¹ at $I_D = 1$ μ A 38.34% decrease in small-signal transconductance at $I_D = 1$ μ A
NDUAL100	Maximum $\Delta V_{OS} = 0.694$ V at $I_D = 10$ μ A Maximum $\Delta V_T = 0.2$ V at $V_{SB} = -5$ V Maximum $\lambda = 0.109$ V ⁻¹ at $I_D = 10$ μ A 50.81% decrease in small-signal transconductance at $I_D = 1$ μ A
NDUAL100A	Maximum $\Delta V_{OS} = 0.2$ V at $I_D = 1$ mA Maximum $\Delta V_T = 0.21$ V at $V_{SB} = -3, -4, -5$ V Maximum $\lambda = 0.048$ V ⁻¹ at $I_D = 100$ μ A 51.44% decrease in small-signal transconductance at $I_D = 1$ μ A
PDUAL10	1 out of 4 units failed due to biasing Maximum $\Delta V_T = 80$ mV at $V_{SB} = 0$ V Maximum $\lambda = 0.124$ V ⁻¹ at $I_D = 1$ mA 24.36% decrease in small-signal transconductance at $I_D = 100$ μ A
PDUAL100	Maximum $\Delta V_{OS} = 0.198$ V at $I_D = 100$ μ A Maximum $\Delta V_T = 0.69$ V at $V_{SB} = -5$ V Maximum $\lambda = 0.092$ V ⁻¹ at $I_D = 100$ μ A 41.07% decrease in small-signal transconductance at $I_D = 1$ μ A
PDUAL100A	Maximum $\Delta V_{OS} = 1.589$ V at $I_D = 1$ mA Maximum $\Delta V_T = 70$ mV at $V_{SB} = 0$ V Maximum $\lambda = 0.111$ V ⁻¹ at $I_D = 100$ μ A 45.34% decrease in small-signal transconductance at $I_D = 1$ μ A

1. ΔV_{OS} and ΔV_T are the changes of offset voltage and threshold voltage, respectively, before and after irradiations.
2. λ is the reciprocal of the Early voltage.

4.4.1 MOSFET Results

4.4.1.1 Offset Voltage (V_{OS})

For both NMOS and PMOS, the symmetrical, larger W/L ratio transistors did exhibit less offset voltage than the other wider and smaller W/L ratio devices before the irradiation. PMOS devices had larger worse case changes than did NMOS devices. Also the offset voltages increased as bias drain currents decreased.

However, there is a great increase of offset voltage due to radiation effects. No explicit dependency of the geometry and the biasing current on the offset voltages was observed; however, there were significant variation of the offset voltage between transistors on different MOSIS chips. It does appear that lower offset voltages occurred near 100 μ A drain current, than near 1 μ A or 1 mA. Empirically the NMOS had worse offset voltages than PMOS after irradiation, which is the opposite situation than that prior to irradiation. Along with the average values, the range of magnitude of offset voltage is presented in Table 4-4. Figure 4-22 indicates the the effects due to radiation, current, and geometry.

4.4.1.2 Threshold Voltage

Threshold voltage (V_T) is defined as the gate-source voltage (V_{GS}) that causes a strong inversion of surface potential. A strong inversion occurs when the doping type of the substrate or bulk underneath the gate becomes inverted to the other doping type; a channel is formed, and carriers are allowed to flow between the source and drain. The threshold voltage is defined as

Table 4-4. List of average values and deviation range for offset voltages of MOSFET transistors.

Device Name	Condition	Pre-Radiation	Post-Radiation	Unit
NDUAL10 ^a	$I_D = 10\mu A$	38.39 [36.76, 40.02]	166	mV
	$I_D = 100\mu A$	58.76 [28.99, 88.54]	162	mV
	$I_D = 1mA$	42.49 [13.59, 71.38]	795	mV
NDUAL100	$I_D = 10\mu A$	25.95 [25.31, 26.58]	188 [3.2, 373]	mV
	$I_D = 100\mu A$	0.52 [0.19, 0.85]	289 [5, 573]	mV
	$I_D = 1mA$	1.01 [0.81, 1.21]	694 [273, 1115]	mV
NDUAL100A	$I_D = 10\mu A$	25.60 [24.35, 26.85]	155[75, 235]	mV
	$I_D = 100\mu A$	1.09 [0.28, 1.90]	166 [83, 249]	mV
	$I_D = 1mA$	1.13 [0.59, 1.67]	2001 [1991, 2022]	mV
PDUAL10 ^b	$I_D = 10\mu A$	63.12 [56.87, 89.36]	---	mV
	$I_D = 100\mu A$	4.85 [0.28, 9.42]	---	mV
	$I_D = 1mA$	163 [163, 163]	---	mV
PDUAL100	$I_D = 10\mu A$	92.24 [25.47, 159]	196 [97, 295]	mV
	$I_D = 100\mu A$	80.75 [1.50, 160]	198 [97, 299]	mV
	$I_D = 1mA$	78.52 [1.03, 156]	185 [79, 291]	mV
PDUAL100A ^a	$I_D = 10\mu A$	26.02[25.54, 26.50]	38.55	mV
	$I_D = 100\mu A$	0.71 [0.24, 1.18]	24.25	mV
	$I_D = 1mA$	1.03 [0.50, 1.55]	1589	mV

(a) NDUAL10 and PDUAL100A had only one device function after radiation.

(b) The only surviving one of PDUAL10 transistors stopped functioning during biasing, thus no data is available.

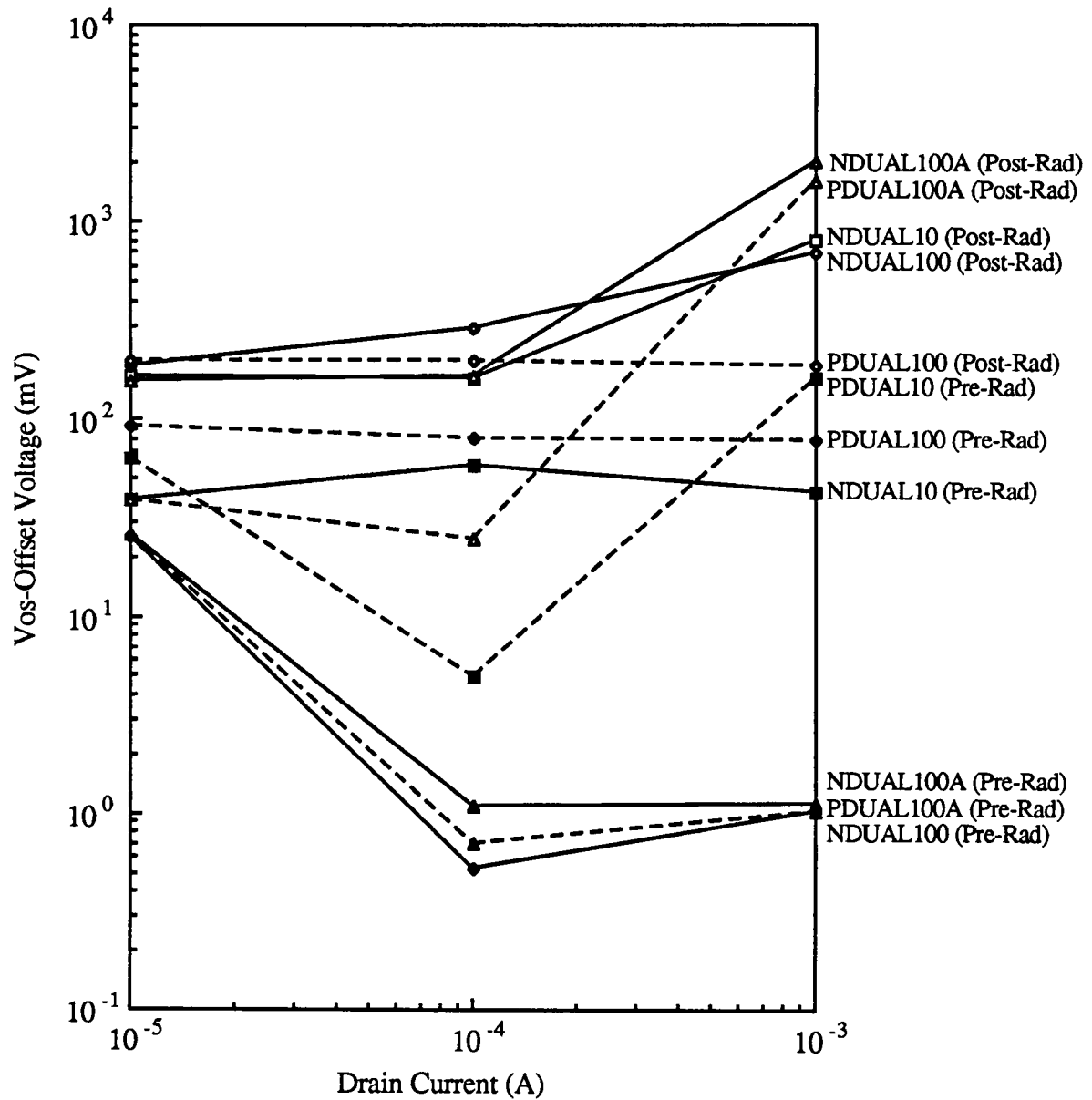


Figure 4-22. Plot of average offset voltages versus drain current for radiation effects on MOSFETs.

$$V_T = V_{TO} + \gamma [\sqrt{(1 - 2\phi_F + V_{SB})} - \sqrt{(1 - 2\phi_F)}] \quad (1)$$

where

($V_{SB} = V_{SUB}$ = reverse bias between substrate and source)

$$V_{TO} = V_T (V_{SB} = 0) = V_{FB} + 2|\phi_F| + [\sqrt{(2q\epsilon_{si} N_{SUB} 2|\phi_F|)}] / C_{OX}$$

$$\gamma = [\sqrt{(2q\epsilon_{si} N_A)}] / C_{OX} \quad \text{the body-factor, body-effect coefficient, or bulk threshold parameter}$$

N_{SUB} , ϕ_F , N_A , V_{FB} , and C_{OX} are process dependent variables

On account of unavoidable imperfect fabrication process of MOSIS chips, the mismatches of threshold voltages directly reflect back to the input as a voltage mismatch.

From the HP4145B Semiconductor Parameter Analyzer, a plot of $\sqrt{(i_D)}$ for the MOSFET transistor as a function of the bulk-source voltage (V_{SB}) versus V_{GS} was obtained. A slope line was drawn along the curves, and the x-intercept is the threshold voltage for each V_{SB} , as indicated earlier in Figures 4-17 and 4-18. The threshold voltage is found in the saturation mode of the enhancement NMOS and PMOS devices. When $V_{DS} \geq (V_{GS} - V_T) \geq 0$, the drain current can be reasonably approximated as [17]

$$i_D = [(\mu_0 C_{OX} W) / 2L] (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad (2)$$

Neglecting the channel-length modulation effects for now,

$$\sqrt{(i_D)} \approx \text{constant} \times (V_{GS} - V_T)$$

where the constant is the slope of the curves from the analyzer.

Body effect of the MOSFET devices has a definite influence on the threshold voltage level. Figure 4-23 indicates such phenomenon and is plotted with both average

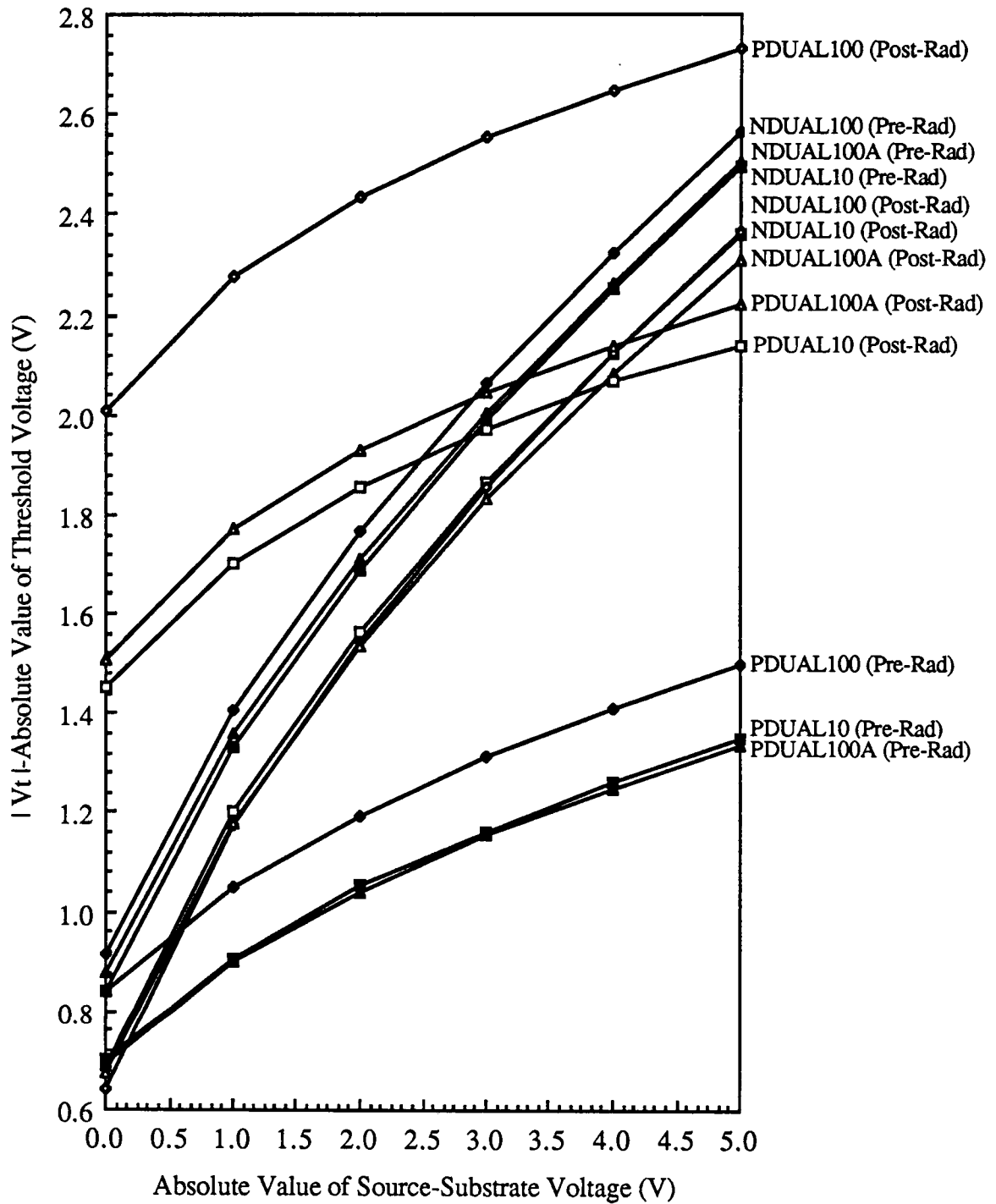


Figure 4-23. Plot of absolute values of average threshold voltage versus absolute values of source-substrate voltage due to radiation effects on MOSFETs.

$|V_T|$ and $|V_{GS}|$. As the V_{SB} increases, $|V_T|$ increases for both enhancement NMOS and PMOS devices.

Prior to radiation, NDUAL100 indicated the best matched threshold voltage among the NMOSFETs. However, for PMOSFETs, PDUAL100 showed the worst case, then PDUAL10, and PDUAL100A. Therefore, generally speaking, the larger size device has better chance of getting matched threshold voltage than the smaller devices due to process variation. Note also that after radiation, $|V_T|$ for PMOS units was larger than before radiation, while $|V_T|$ for the NMOS units decreased after irradiation. Generally, as radiation dose increases the $|V_T|$ value for NMOS units will initially decrease, and then increase as interface states assume control over oxide states [9].

4.4.1.3 Early Voltage

When $V_{DS} \geq (V_{GS} - V_T) \geq 0$, the saturation or pinch-off region occurs which was discussed at an earlier section 4.4.1.2. Ideally any increase of V_{DS} will cause an equal voltage increase across the depletion region, and the drain current (I_D) does not change. The depletion region surrounds the source, channel, and drain and extends up to the surface. The pinch-off region should be flat on the plot of I_D versus V_{DS} for MOSFET transistors. The devices operate approximately as a voltage-controlled source.

However, in real devices, the drain current does increase as V_{DS} increases which is called channel-length modulation. The movement of the pinch-off point towards the source as V_{DS} increases, the channel length shortens and causes increasing I_D . This effect is included in the drain current equation which is the Equation (2) repeated here for convenience.

$$i_D = [(\mu_0 C_{OX} W)/2L] (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad (2)$$

where

$$\lambda = V_A^{-1} = L_{\text{eff}}^{-1} (d X_d / d V_{ds})$$

V_A is the Early voltage

X_d is the depletion layer width at the drain

L_{eff} is the effective channel length

μ_0 is the mobility of either electrons or holes

λ should be a device constant and depends on L , doping level of the substrate and the bulk bias; this makes it a process dependent element. Typically λ ranges from 0.03 V^{-1} to 0.005 V^{-1} , which implies V_A ranging from 33 V to 200 V.

Figure 4-24 indicates the radiation effects on $|V_A|$ for both NMOS and PMOS. The polarity of V_A for NMOS is negative and for PMOS is positive. By observation V_A is not a constant and varies with bias condition.

PDUAL100 and PDUAL100A had greater Early voltages than the smaller PDUAL10 devices before the irradiation. NMOS devices exhibited less channel length modulation effects than PMOS devices for both before and after irradiation. NDUAL10 had larger Early voltages than the other devices after irradiation. There was a definite decrease of Early voltage after radiation and an increase of the influence of the channel length modulation on the devices.

4.4.1.4 Small-Signal Transconductance

For most linear applications, such as operational amplifiers, MOSFET transistors can be adequately used with small signals. If the transistor operates in the common-source configuration and the input gate is driven by a voltage source, the small-signal amplification

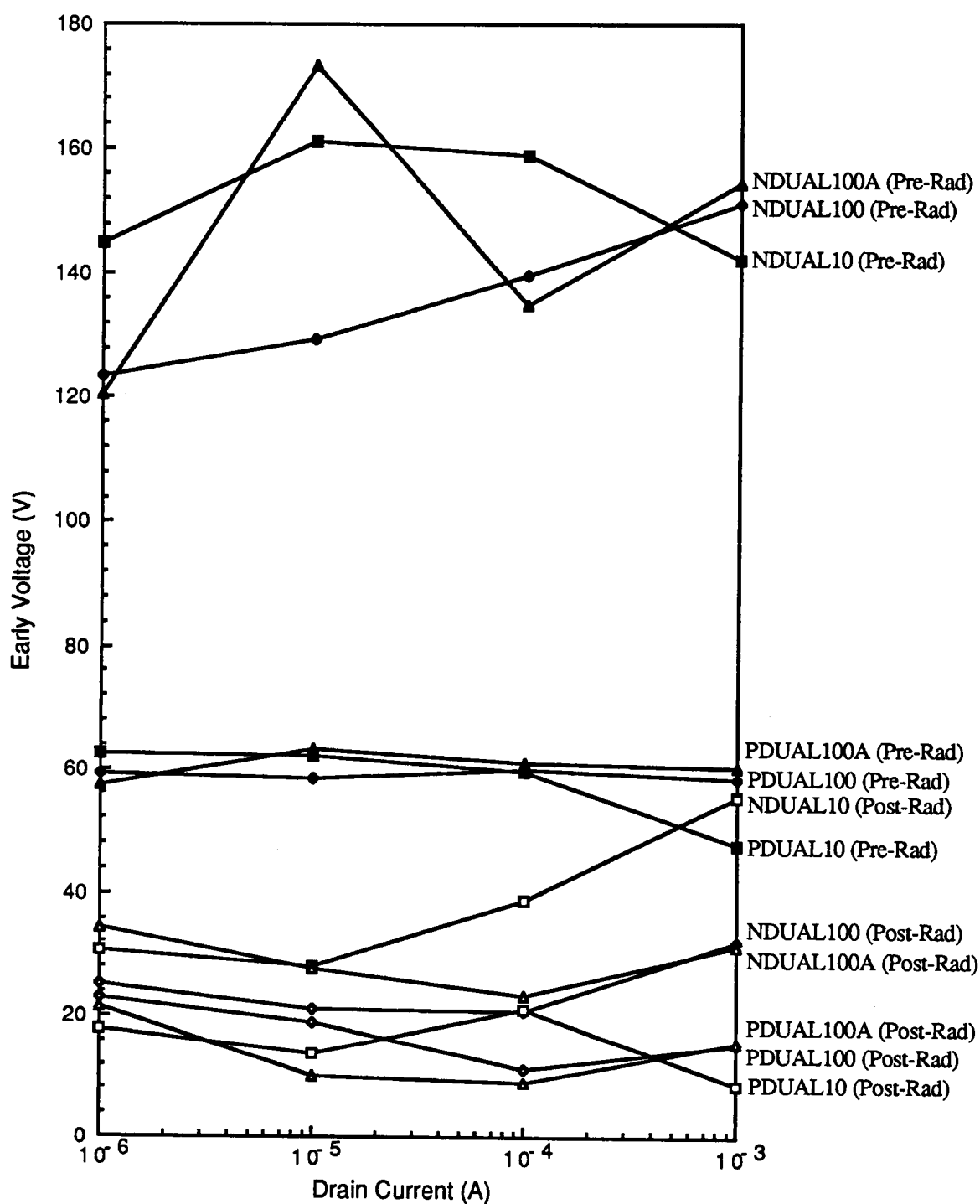


Figure 4-24. Plot of absolute values of average Early voltages versus drain current for radiation effects on MOSFETs.

is most useful when MOSFET is characterized by its transconductance. A MOS differential amplifier, such as the circuits shown in Figure 4-15 for measuring offset voltage and noise voltage spectrum density, can be projected as an extension of the common-source configuration. The transconductance is developed when the output (drain current) varies in response to the changes at the input (gate voltage). When the MOSFET is in its linear region ($V_{DS} < V_{sat}$)

$$g_m = (\partial I_D / \partial V_{GS}) |_{V_{GS} = \text{constant}} = [(\mu_0 C_{OX} W) / L] V_{DS} \quad (3)$$

In this linear region, g_m increases linearly with V_{DS} but is independent of V_{GS} .

Because g_m is proportional to the W/L ratio and the oxide capacitance per unit area, it is heavily process dependent. Therefore, greater g_m is obtained with larger W/L ratio.

This case is clearly indicated in Figure 4-25 for MOSFETs before and after irradiation. The geometry of the device had a definite influence on small-signal transconductance. NDUAL100 A and PUDAL100 A with more square-like dimension had 6.8% and 8.5 % greater g_m , respectively, than NDUAL100 and PDUAL100 with larger width over length rectangular dimension before the radiation exposure. Generally speaking, NMOS had greater g_m , because of the electron mobility (μ_n) is typically twice or three times larger than the hole mobility (μ_p), than PMOS prior to and post-radiation for all three different sizes and geometry. Table 4-5 gives the average values and deviation range of the small transconductance for MOSFET's. Since the readout from the analyzer had only three significant digits for the test results, the average values reflect such constraint.

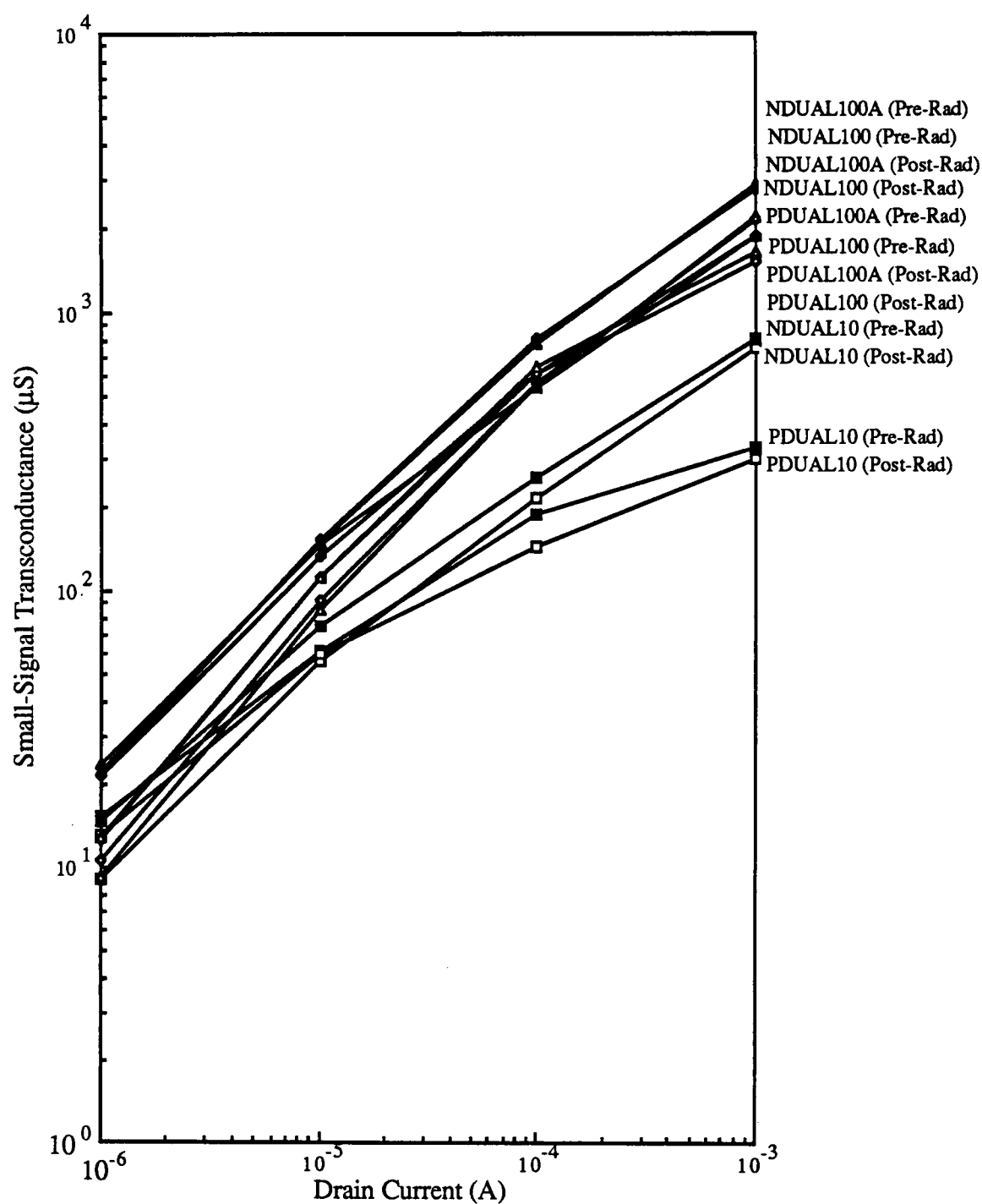


Figure 4-25. Plot of average small-signal transconductance versus drain current for radiation effects on MOSFETs

Table 4-5. List of average values and deviation range for small-signal transconductance of MOSFET transistors.

Device Name	Condition	Pre-Radiation	Post-Radiation	Unit
NDUAL10	$I_D = 1\mu A$	14.7 [13.1, 16.2]	9.03 [8.47, 9.37]	μS
	$I_D = 10\mu A$	75.0 [70.5, 81.3]	56.7 [52.2, 58.9]	μS
	$I_D = 100\mu A$	256 [216, 283]	217 [205, 235]	μS
	$I_D = 1mA$	815 [775, 894]	756 [685, 805]	μS
NDUAL100	$I_D = 1\mu A$	21.7 [20.0, 22.7]	10.7 [10.2, 11.0]	μS
	$I_D = 10\mu A$	152 [146, 158]	92.5 [82.4, 104]	μS
	$I_D = 100\mu A$	808 [803, 816]	558 [516, 589]	μS
	$I_D = 1mA$	2750 [2590, 2890]	2160 [2060, 2290]	μS
	$I_D = 1mA$	2880 [2830, 2980]	2320 [2180, 2440]	μS
PDUAL10	$I_D = 1\mu A$	15.3 [13.8, 16.0]	13.0 [11.4, 15.6]	μS
	$I_D = 10\mu A$	61.0 [56.1, 65.0]	59.3 [53.3, 69.4]	μS
	$I_D = 100\mu A$	190 [170, 197]	143 [134, 149]	μS
	$I_D = 1mA$	328 [298, 358]	298 [298, 298]	μS
PDUAL100	$I_D = 1\mu A$	21.4 [11.1, 25.9]	12.6 [11.1, 14.1]	μS
	$I_D = 10\mu A$	134 [102, 156]	113 [107, 120]	μS
	$I_D = 100\mu A$	611 [564, 656]	607 [542, 702]	μS
	$I_D = 1mA$	1880 [1760, 2030]	1510 [1220, 1700]	μS
PDUAL100A	$I_D = 1\mu A$	23.6 [22.2, 26.4]	12.9 [10.8, 16.3]	μS
	$I_D = 10\mu A$	148 [139, 158]	112 [104, 118]	μS
	$I_D = 100\mu A$	563 [473, 648]	644 [618, 684]	μS
	$I_D = 1mA$	1880 [1670, 2000]	1650 [1550, 1730]	μS

4.4.1.5 Noise Voltage Spectral Density

The major components of the gate-referred noise voltage of a MOSFET are the thermal noise and the flicker noise (which is often called 1/f noise or pink noise). In any conducting transistor, the free carriers are in random thermal motion, which constitutes the major thermal noise effect. Thermal noise is dominant at high frequencies where the flicker-noise effect decreases. The input thermal noise voltage of a single MOSFET is given by [17]

$$(V_{nt})^2 = [4 kT (K / g_m)] \Delta f \quad (4)$$

where

k = Boltzmann's constant

T = temperature in kelvin

$K \approx 1$ for MOS devices

Δf = noise bandwidth

The flicker noise is introduced by trapping and releasing electrons from the channel at the boundary between the Si and SiO₂. The traps are caused by impurities and defects in the crystal structure.. This noise energy dominates at low frequencies, decreases as frequency increases, and is dependent on g_m , as shown in Equation (5). The gate referred noise voltage can be approximated by the formula [18, 19]

$$\begin{aligned} (V_{nf})^2 &= (B / C_{ox} W L) (\Delta f / f) \\ &= (C I_D^a \Delta f) / (g_m^2 f) \end{aligned} \quad (5)$$

where

B , C , and a depend on the temperature and the fabrication process

Thus 1/f noise is process dependent. The greater size MOSFET should have less flicker noise effect. The equivalent input noise of a gain stage can be referred to the input of the stage. Therefore, from Figures 4-15 and 4-16 the equivalent input-referred noise voltage was calculated. The mathematical derivation is presented as following. For the total output noise seen by the True RMS voltmeter we have

$$\begin{aligned} \xi_n^2(f_o) / \Delta f_n = & (e_{M1} A_1 A_2 A_{tt})^2 + (e_{M2} A_1 A_2 A_{tt})^2 + \\ & (e_{RD1} A_1 A_2 A_{tt} / A_M)^2 + (e_{RD2} A_1 A_2 A_{tt} / A_M)^2 + \\ & (e_{27V} A_1 A_2 A_{tt} / A_M)^2 + (e_{27I} R_{D1} A_1 A_2 A_{tt} / A_M)^2 + \\ & (e_{27I} R_{D2} A_1 A_2 A_{tt} / A_M)^2 + (e_{R1})^2 (R_{F1} / R_1)^2 (A_2 A_{tt})^2 + \\ & (e_{RF1})^2 (A_2 A_{tt})^2 + (e_{37V} A_2 A_{tt})^2 + (e_{37I} R_{F2} A_{tt})^2 + \\ & (e_{R2})^2 (R_{F2} / R_2)^2 A_{tt}^2 + (e_{RF2})^2 A_{tt}^2 \end{aligned} \quad (6)$$

where

$\xi_n(f_o)$ is the output voltage of amplitude spectral density measured on a true RMS voltmeter at a particular frequency (f_o), and its unit is volts.

Δf_n is the the noise bandwidth at a particular frequency (f_o).

e_{M1} and e_{M2} are the input equivalent noise sources due to the differential pair of MOSFETs and are referred to their own gate terminals.

$A_1 = [1 + (R_{F1} / R_1)]$ is the first stage of amplification as shown in Figure 4-15.

$A_2 = [1 + (R_{F2} / R_2)]$ is the second stage of amplification as shown inside the dashed box in Figure 4-16.

A_{tt} is the third stage of amplification coming from the twin-tee filter and is slightly different for each frequency filter, but is approximately 40.

$A_M = g_m R_D / 2$ is the signal amplification from the gate to the drain of the MOSFETs (ignoring the Early voltage effect of M_1 and M_2).

$(e_{RD})^2 = 4kT R_D$ is the thermal noise from the $R_{D1} = R_{D2} = R_D$ resistors.

e_{27V} is the equivalent input noise voltage of the OP-27.

e_{27I} is the equivalent input noise current of the OP-27 and exists at both inputs of the operational amplifier.

$(e_{R1})^2 = 4kT R_1$ is the noise from the R_1 resistor.

$(e_{RF1})^2 = 4kT R_{F1}$ is the noise from the R_{F1} resistor.

e_{37V} is the input noise voltage of the OP-37.

e_{37I} is the input noise current of the OP-37.

$(e_{R2})^2 = 4kT R_2$ is the noise from the R_2 resistor.

$(e_{RF2})^2 = 4kT R_{F2}$ is the noise from the R_{F2} resistor.

If the gain A_1 in Figure 4-15 is large enough, the noise contributions from the second stage due to R_{F2} , R_2 , and the OP-37 in Figure 4-16 may be neglected, so they can be removed from Equation (6); also the noise coming from the OP-27 in Figure 4-15 can generally be neglected. Therefore, the midband noise of the differential pair of MOSFETs of Figure 4-15 seen at the output of the twin-tee filter is

$$\begin{aligned} (e_{MOS})^2 (A_1 A_2 A_u)^2 &= (e_{M1}^2 + e_{M2}^2) (A_1 A_2 A_u)^2 \\ &\approx \xi_n^2 (f_o) / \Delta f_n - (A_1 A_2 A_u)^2 [(e_{RD1})^2 + (e_{RD2})^2 + \\ &\quad (e_{R1})^2 (R_{F1} / R_1)^2 (1/A_1)^2 + (e_{RF1})^2 (1/A_1)^2] \end{aligned} \quad (7)$$

where

e_{MOS} is the equivalent input referred noise voltage of the differential pair of MOSFET's, and its unit is volt per square root of hertz.

Using values of components from Figure 4-15 and 4-16, a list of the equivalent midband input noise (mainly due to thermal noise) anticipated is given in Table 4-6. These noise calculations are idealized because the output resistance of MOS devices ($\approx V_A / I_D$) was assumed to be infinite.

The variation of noise voltage spectral density was large among some samples for both before and after irradiation. Therefore, no average value is presented here. Plots of each device for radiation effect, size or geometry, and bias condition are provided for analysis. Only four points of interested frequency were taken before irradiation. Because of the large and varied changes due to radiation, the samples after irradiation were evaluated at 13 different frequencies ranging from 100 Hz up to 1 MHz, which were the total twin-tee filter frequencies available. The gain for the first stage of amplification (A_1) was also decreased after radiation due to the large offset voltage that occurred.

PDUAL10 had no data recorded for post-radiation effects because sample #1 was damaged during irradiation, while sample #2 was damaged when measurements were attempted. As shown in Figure 4-26, the pre-irradiation noise decreased with increasing drain current, and there was cross-over for sample#2 with $I_D = 100 \mu\text{A}$ and $I_D = 10 \mu\text{A}$ at low frequencies between 100 Hz and 1kHz. This kind of behavior was indicated only before radiation among all PMOS devices as in Figures 4-26 through 4-28. Reasonable noise data was difficult to obtain due to oscillations in the test setup, and 60-120 Hz pickup. Therefore, the data was screened, and only data is shown that was deemed reasonable. Unfortunately, additional time and contract money was not available to redo this experiment. The data for the PMOS devices of Figures 4-26 through 4-28 reasonably follows the midband noise predictions of Table 4-6. The larger gate area devices (large $W \times L$) indeed contribute significantly less $1/f$ noise than does the PDUAL10 devices. It also appears that the $1/f$ "noise corner" for the PDUAL100 units is lower than for the PDUAL100A units.

Table 4-6. Table of equivalent midband input noise theoretically anticipated at midband for the MOSFET transistors tested.

Device Type	W/L	I_D	e_{mos} (nV/ $\sqrt{Hz}$)
NDUAL10	10	10 μA	23.36
		100 μA	13.30
		1 mA	9.29
PDUAL10	10	10 μA	26.30
		100 μA	15.71
		1 mA	5.51
NDUAL100	100	10 μA	16.00
		100 μA	7.79
		1 mA	5.58
PDUAL100	100	10 μA	17.07
		100 μA	8.73
		1 mA	6.29
NDUAL100 A	100	10 μA	16.33
	100	100 μA	7.89
		1 mA	5.51
PDUAL100 A	100	10 μA	16.22
		100 μA	9.05
		1 mA	6.29

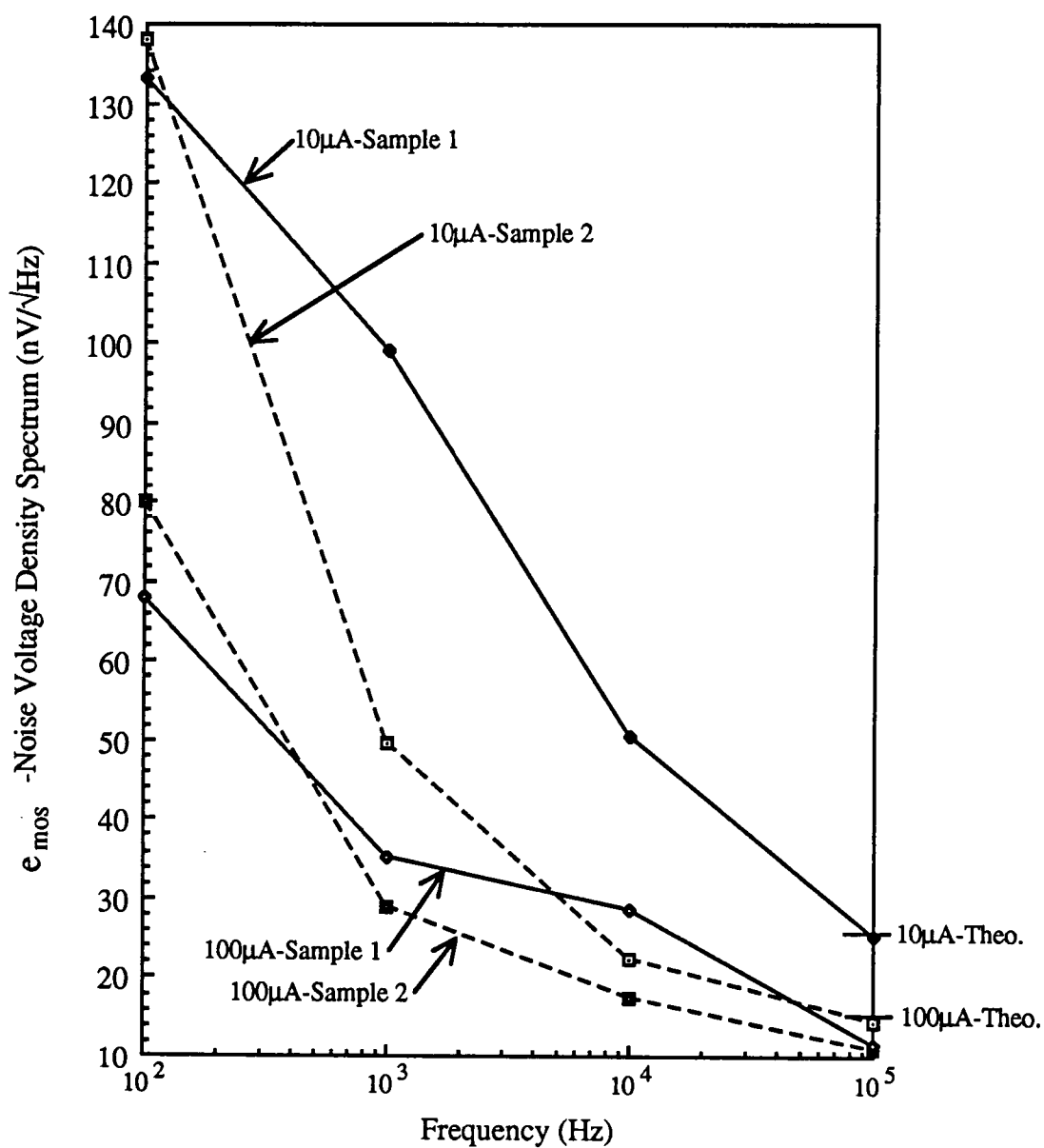


Figure 4-26. Plot of noise voltage spectrum of PDUAL10 versus frequency for various drain currents before radiation.

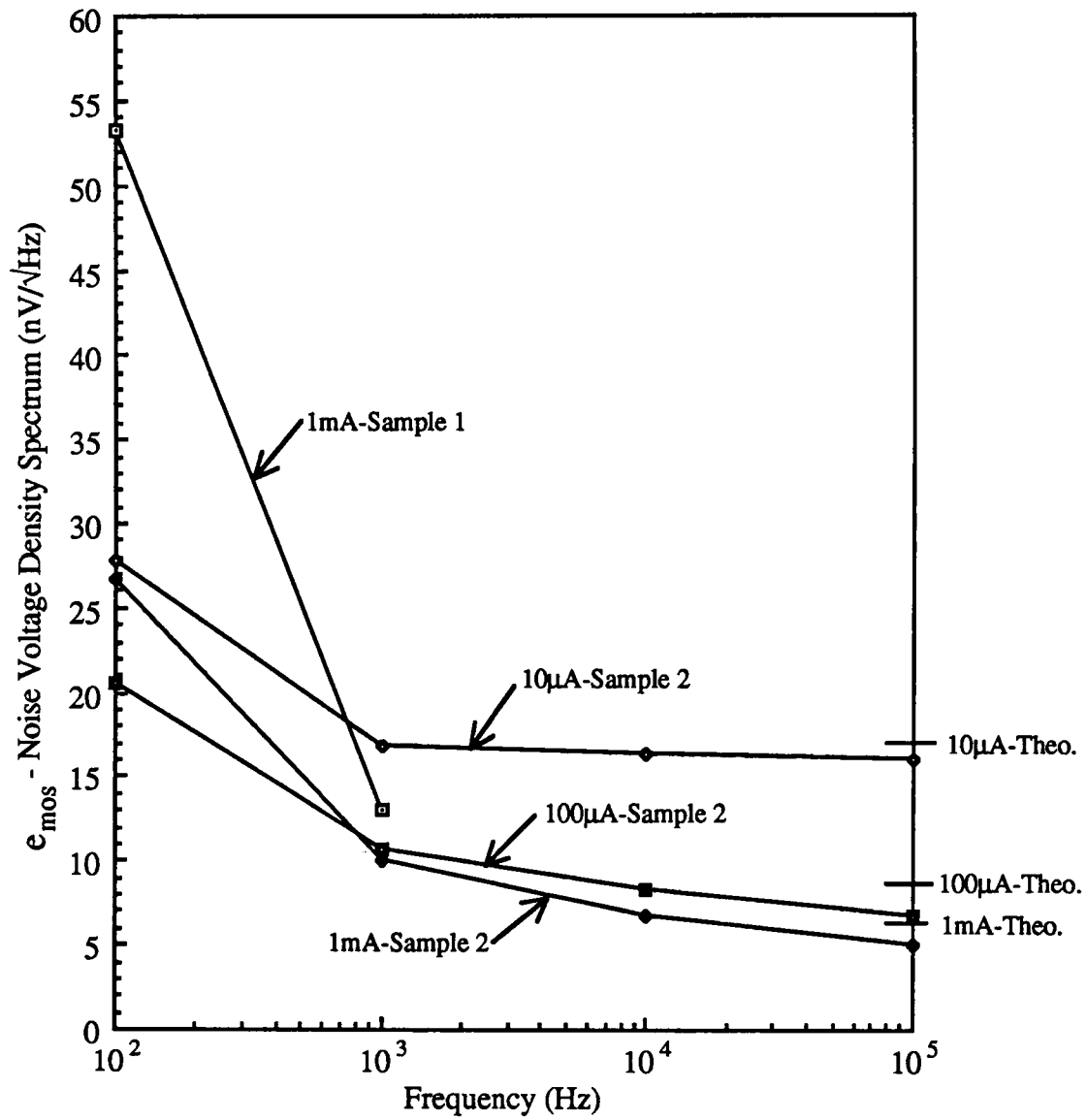


Figure 4-27. Plot of noise voltage spectrum of PDUAL100 versus frequency for various drain currents before radiation.

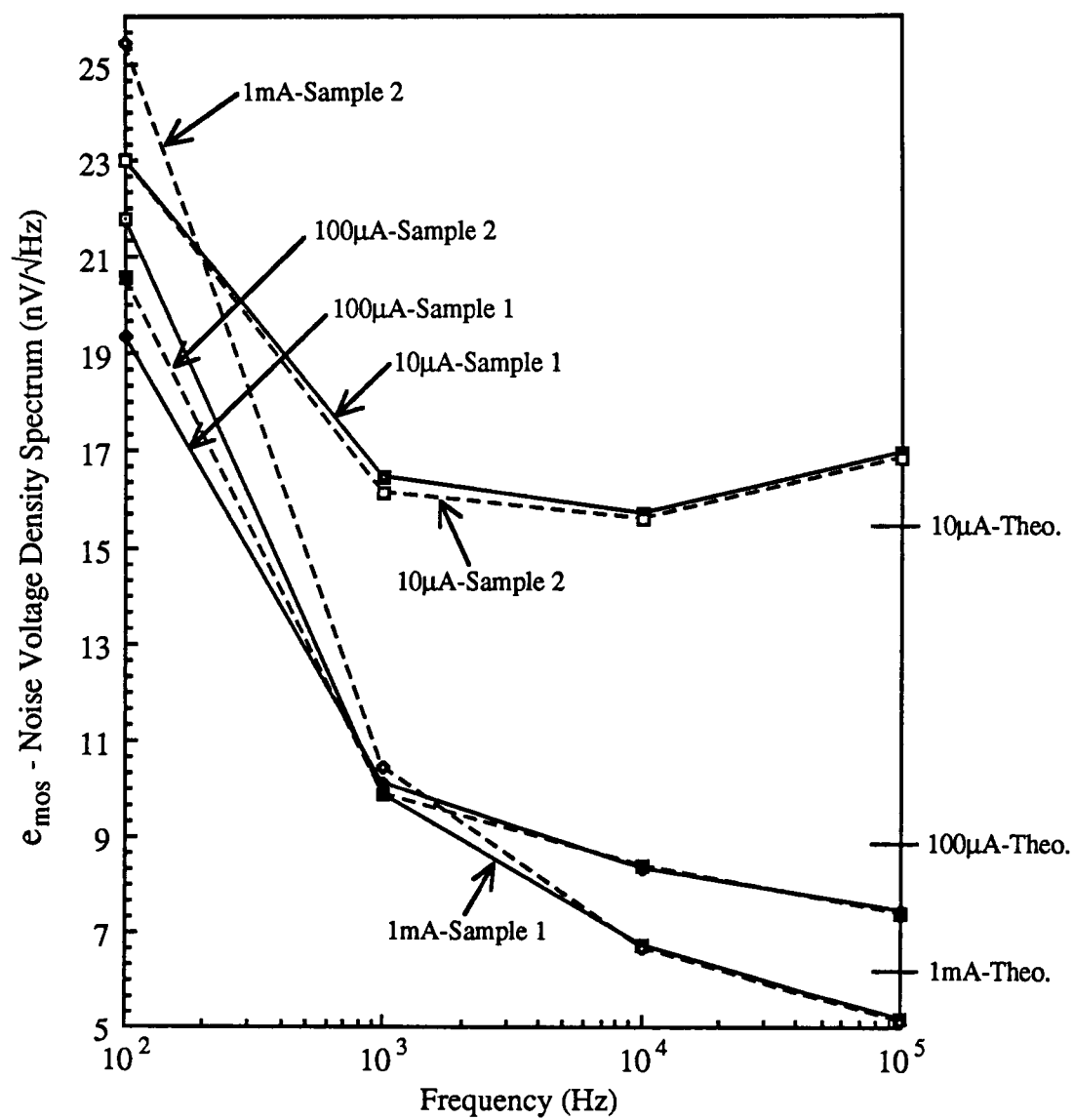


Figure 4-28. Plot of noise voltage spectrum of PDUAL100A versus frequency for various drain currents before radiation.

Figure 4-29 indicates the noise spectrum before radiation for the NDUAL10 units with $W/L = 10$, while Figure 4-30 shows the large increase in low-frequency noise for the NDUAL10 units after radiation. The unanticipated jump (between 200 kHz and 1 MHz) in the data for Sample 2 at 10 μA in Figure 4-30 is certainly questionable. Also, the large increase in $1/f$ noise at 1 mA would bear further study. The correlation between the theoretical noise predictions of midband noise given by Table 4-6, and the experimental data of Figures 4-29, 4-31, and 4-32 is reasonably good. As for the PMOS structures, the larger gate area ($W \times L$) indeed gives less $1/f$ noise.

In comparing the NMOS vs. PMOS devices, it is apparent that although the midband noise for the NMOS devices is lower (due to higher g_m) than the PMOS devices, the $1/f$ "noise corner" for the PMOS units is significantly less than for the NMOS units. Indeed, if we compare the units for $I_D = 100 \mu\text{A}$, at a frequency of 100 Hz, the PDUAL10 device has 1/5 the noise of the NDUAL10. Similarly, for the larger devices, PDUAL100 has 1/3 the noise of NDUAL100 and PDUAL100A gives 1/3 the noise of NDUAL100A. Similar observations have been made by Stone [20]. It must be emphasized that these particular MOS units were fabricated in an n substrate with p-well. One should not extend the conclusion indicated here to an n-well (p substrate) process without detailed experimental evaluation.

After radiation, all MOSFET's had significant increase of noise in the entire spectrum, and the noise range generally changed from $\text{nV}/\sqrt{\text{Hz}}$ to $\mu\text{V}/\sqrt{\text{Hz}}$. For example, at 100 Hz, $I_D = 100 \mu\text{A}$, the noise for NDUAL10 increased by a factor of 5. Post-irradiation data was also taken for the P- and D-DUAL100 units, but discrepancies in the measurements resulted in erroneous data. Due to time limitations these data could not be refined.

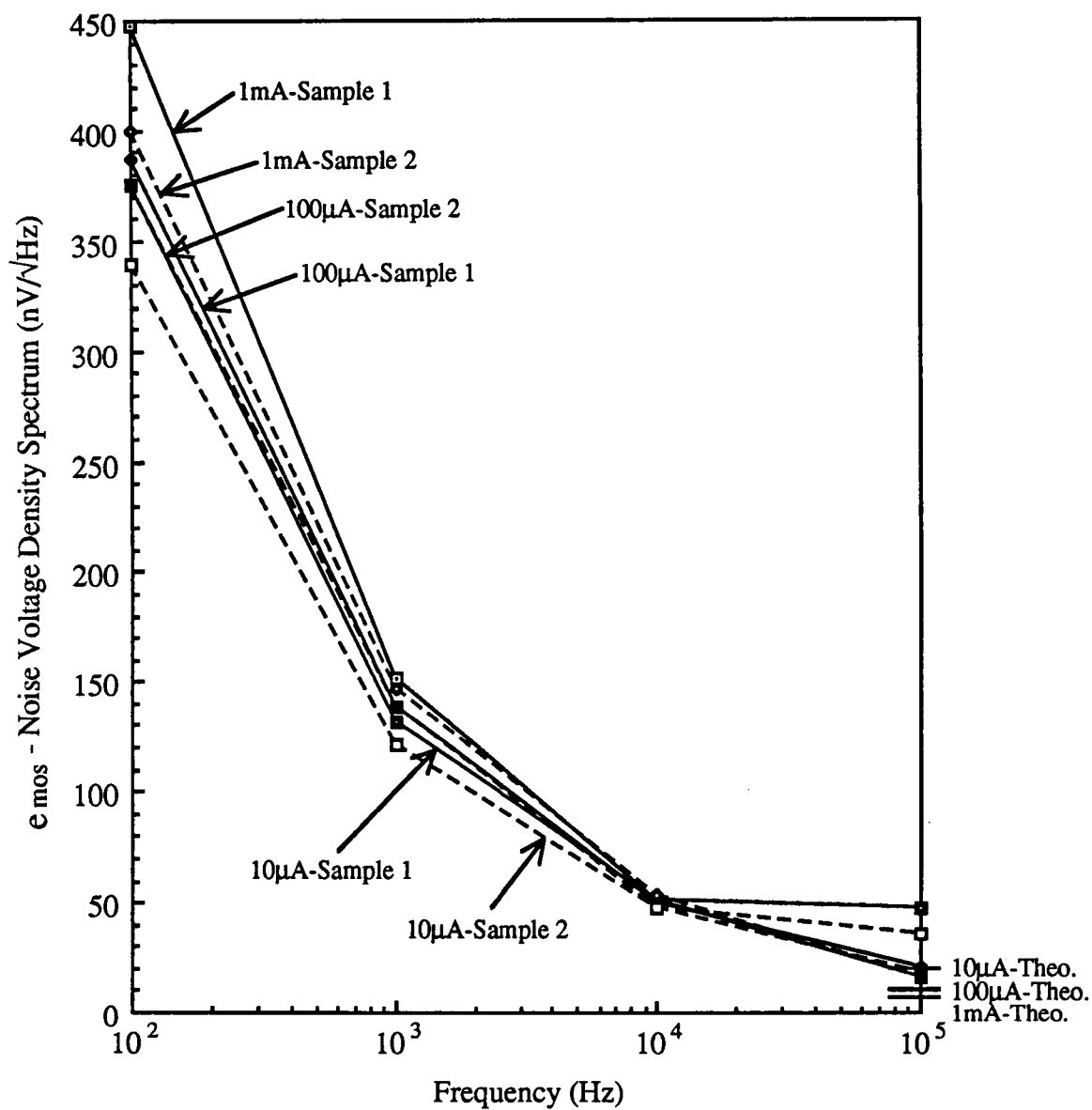


Figure 4-29. Plot of noise voltage spectrum of NDUAL10 versus frequency for various drain currents before radiation.

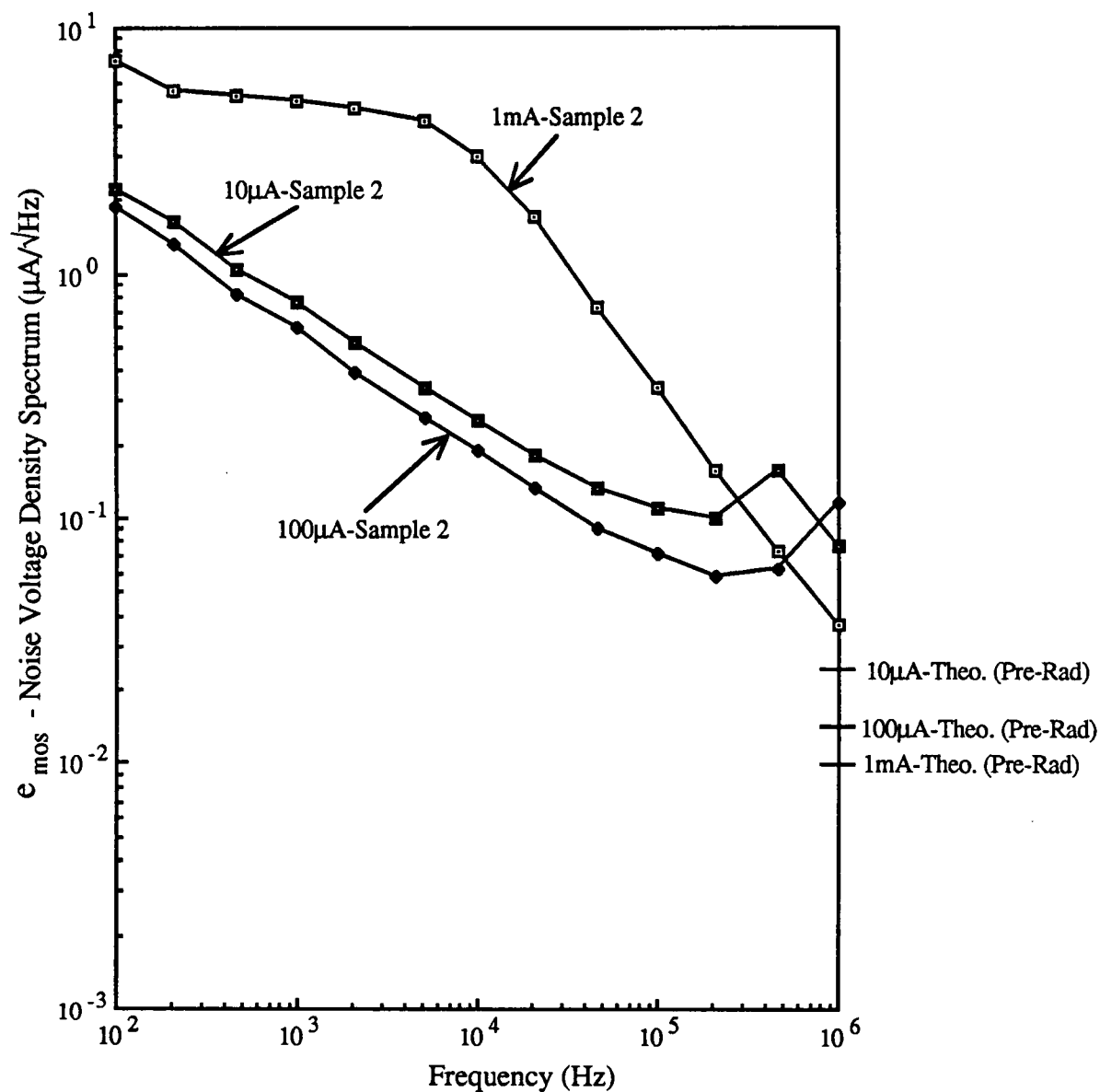


Figure 4-30. Plot of noise voltage spectrum of NDUAL10 versus frequency for various drain currents after radiation.

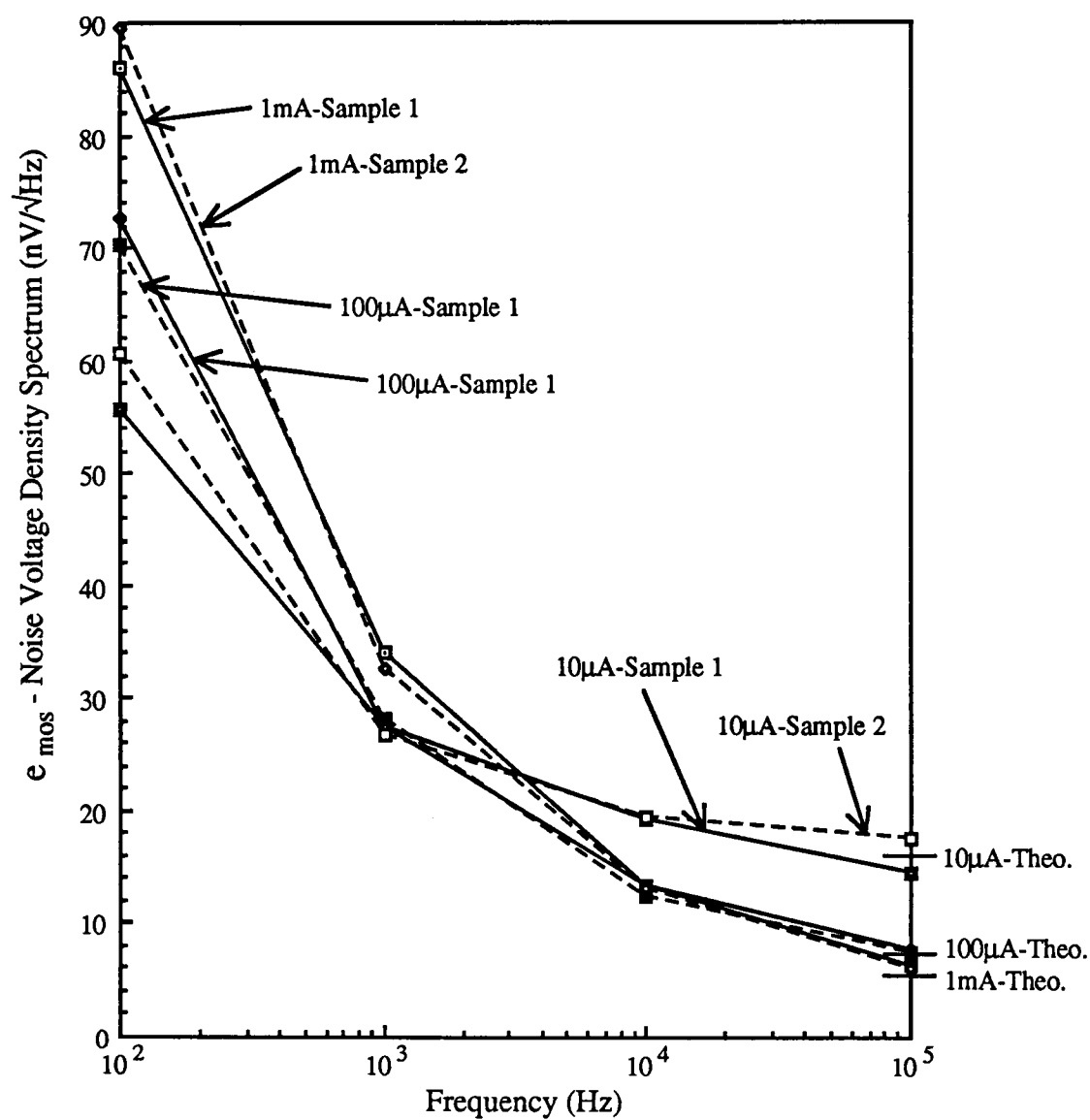


Figure 4-31. Plot of noise voltage spectrum of NDUAL100 versus frequency for various drain currents before radiation.

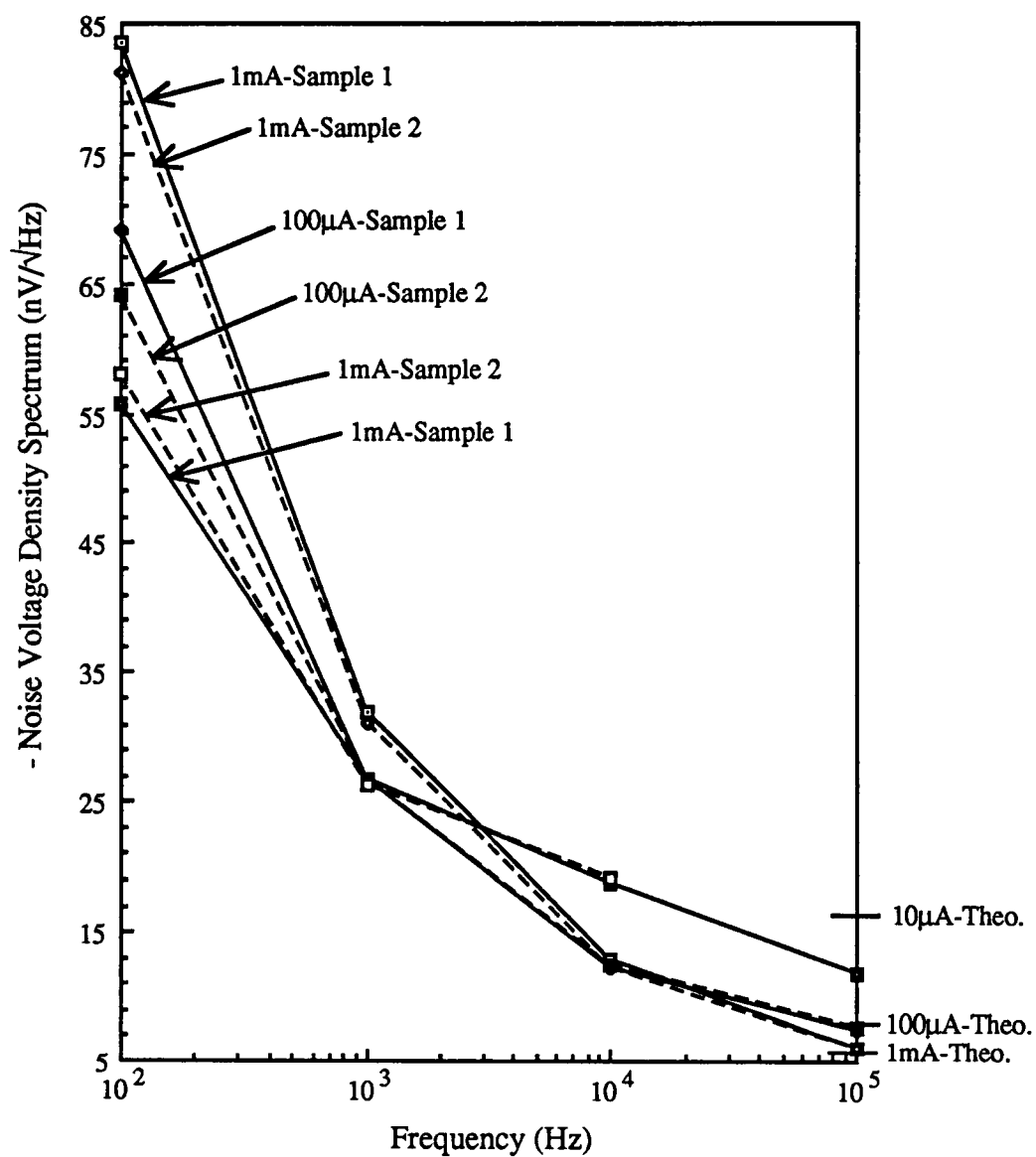


Figure 4-32. Plot of noise voltage spectrum of NDUAL100A versus frequency for various drain currents before radiation.

4.4.2 BIPOLAR TRANSISTOR RESULTS

Three types of bipolar junction transistor (BJT) with two samples each were tested. All BJT devices were passive during irradiation. Some plots were included in Figure 4-19 and 4-20 shown earlier. The I_C / I_B ratio for both dual lateral NPN's was greater than one after radiation, but for the single NPN devices the I_C / I_B ratio was less than one. Average values were calculated to determine the radiation effects and are summarized in Table 4-7.

4.4.2.1 Offset Voltage

The offset voltage of bipolar transistors with the emitter-coupled pair can be caused by many process-dependent factors, such as the mismatches of the base width, base doping level, collector doping level, effective emitter area, and temperature drift. Besides the strong influences of device geometry and fabrication process, the mismatches in the collector load resistors can also contribute to the offset voltage.

The average values and the range of magnitude of offset voltage is presented in Table 4-8. There were definite offset voltage increases for higher currents, but the offset voltage decreased as drain current was lowered to $10\mu\text{A}$. Figure 4-33 shows such trends.

Doubling the size of the transistor as 2DUALNPN to DUALNPN made the transistor more vulnerable to process variation. Higher offset voltage was expected not just prior to radiation but also even more so after radiation as indicated in the figure. In comparison with the large area MOSFETs, it is very apparent that offset voltages for bipolars (both pre- and post-radiation) are much less, and more uniform.

Table 4-7. Radiation effects on BJT transistors.

Device Name	≥ 1.9 Megarad Effects
NPNA	43 % increase in Early voltage at $I_D = 100\mu\text{A}$
DUALNPN	Average $\Delta V_{os} = 10.7$ mV at $I_D = 1\text{mA}$ 49 % increase in Early voltage at $I_D = 100\mu\text{A}$
2DUALNPN	Average $\Delta V_{os} = 109$ mV at $I_D = 1\text{mA}$ 127 % increase in Early voltage at $I_D = 1\text{mA}$

Table 4-8. List of average values and deviation range for offset voltages of BJT transistors.

Device Name	Condition	Pre-Radiation	Post-Radiation	Unit
DUALNPN	$I_D = 10\mu\text{A}$	11.38 [11.28, 11.47]	4.3 [1.6, 7.0]	mV
	$I_D = 100\mu\text{A}$	1.93 [1.63, 2.23]	7.53 [5.9, 9.15]	mV
	$I_D = 1\text{mA}$	18.42 [14.93, 21.90]	29.13 [12.05, 46.2]	mV
2DUALNPN	$I_D = 10\mu\text{A}$	11.14 [11.07, 11.21]	5.325 [3.05, 7.6]	mV
	$I_D = 100\mu\text{A}$	2.21 [1.78, 2.64]	8.9 [8.2, 9.6]	mV
	$I_D = 1\text{mA}$	20.49 [19.49, 21.48]	129.5 [38.45, 220.5]	mV

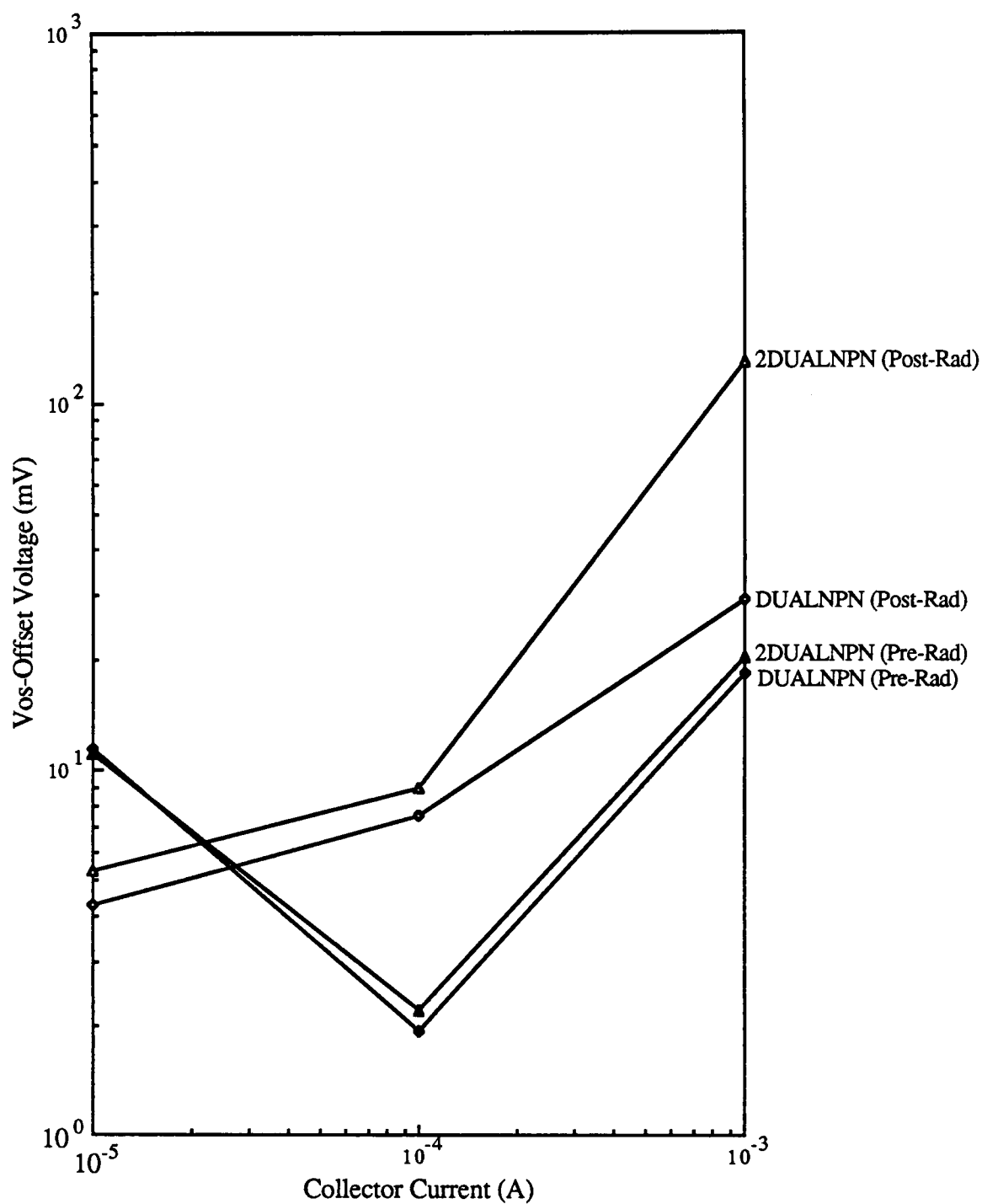


Figure 4-33. Plot of average offset voltages versus collector current for radiation effects on lateral BJT's.

4.4.2.2 Early Voltage

The Early voltage of a bipolar transistor is defined as

$$V_A = I_C / (\partial I_C / \partial V_{CE}) = -W_B (d V_{CB} / d W_B)$$

where

W_B is the width of the base from the base-emitter depletion layer edge to the base-collector depletion layer edge

The Early voltage should be independent of the collector current but strongly dependent on the process. Larger collector and emitter area devices, such as 2DUALNPN, had lower Early voltages than the half area size of DUALNPN's. Table 4-9 gives the average values and the range of magnitude of the Early voltages, and Figure 4-34 depicts such changes. The Early voltage of the single vertical NPN was significantly higher than that of dual NPN's for pre- and post- radiation. Also, a comparison of Figure 4-34 with that of Figure 4-24 indicates that post-radiation values for Early voltages for bipolars are higher than for MOSFETs.

4.4.2.3 Current Gain

The dc current gain (h_{FE} or β) of the transistor also has large dependency on the fabrication process because the minority-carrier lifetime in the base affects the base transport factor and the diffusion length in the emitter. The doping level varies with distance into the emitter and will, thereafter, influence the current gain.

Table 4-10 represents the average values and the deviation range of the current gain, and Figure 4-35 shows the variation. 2DUALNPN had less current gain, in general, for both before and after irradiation.

Table 4-9. List of average values and deviation range for Early voltages of BJT transistors.

Device Name	Condition	Pre-Radiation	Post-Radiation	Unit
NPNA	$I_D = 1\mu\text{A}$	-154 [-112, -195]	-123 [-109, -137]	V
	$I_D = 10\mu\text{A}$	-160 [-148, -171]	-127 [-100, -154]	V
	$I_D = 100\mu\text{A}$	-115 [-107, -122]	-164 [-150, -178]	V
	$I_D = 1\text{mA}$	-81.7 [-80.2, -83.1]	-108 [-74, -141]	V
DUALNPN	$I_D = 1\mu\text{A}$	-25.7 [-22.6, -29.2]	-22.5 [-17.6, -27.7]	V
	$I_D = 10\mu\text{A}$	-26.0 [-22.3, -32.2]	-30.2 [-23.3, -37.3]	V
	$I_D = 100\mu\text{A}$	-27.2 [-24.6, -30.4]	-48.7 [-38.2, -60.4]	V
	$I_D = 1\text{mA}$	-30.0 [-27.6, -33.6]	-68.2 [-68.2, -84.8]	V
2DUALNPN	$I_D = 1\mu\text{A}$	-25.0 [-21.6, -27.9]	-23.5 [-16.7, -31.8]	V
	$I_D = 10\mu\text{A}$	-26.0 [-22.2, -29.9]	-26.7 [-20.1, -35.6]	V
	$I_D = 100\mu\text{A}$	-25.6 [-22.3, -28.6]	-38.1 [-28.2, -46.9]	V
	$I_D = 1\text{mA}$	-28.3 [-25.8, -33.2]	-59.3 [-46.9, -69.0]	V

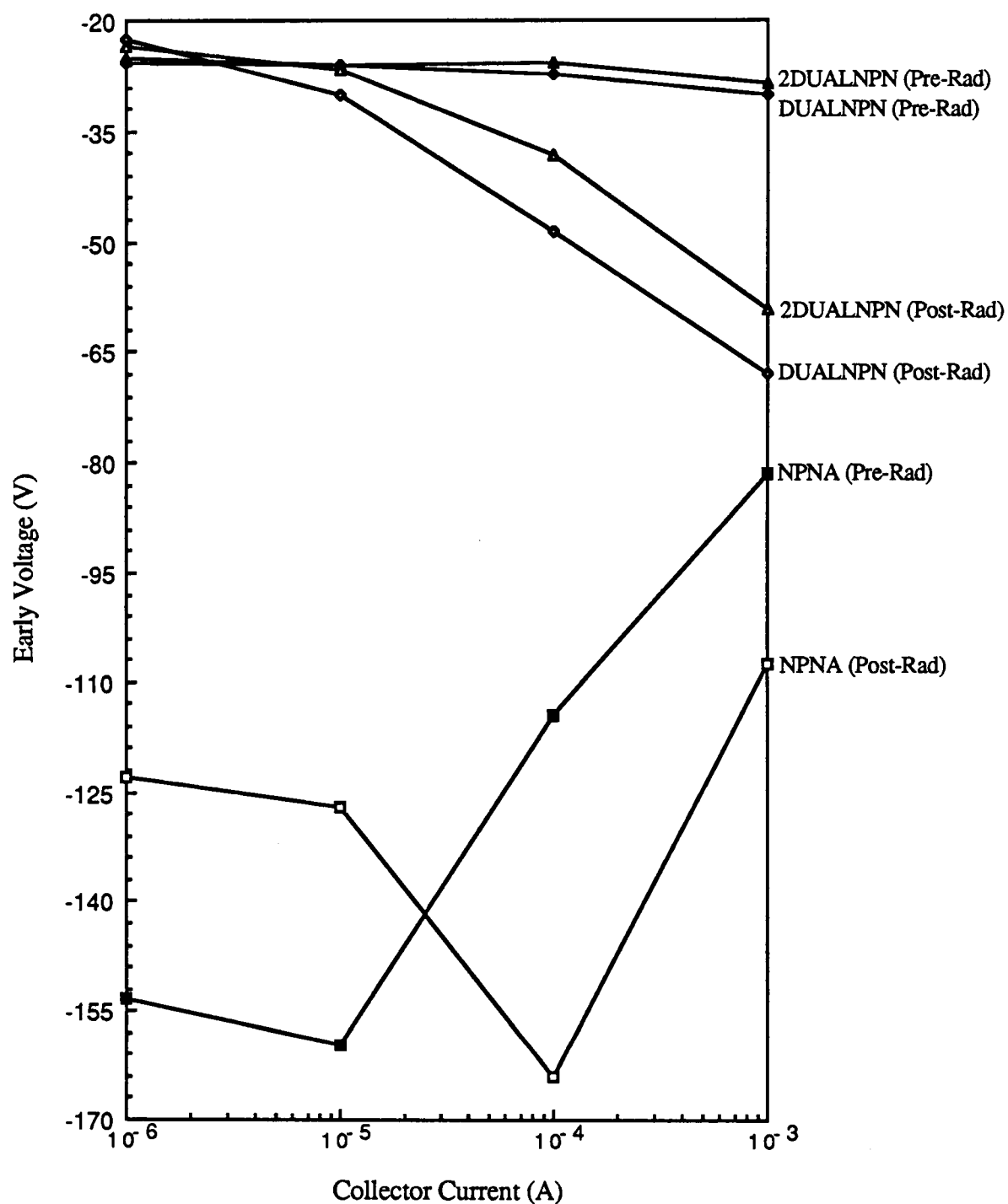


Figure 4-34. Plot of absolute values of average Early voltages versus collector current for radiation effects on BJT's.

Table 4-10. List of average values and deviation range for current gain (h_{FE}) of BJT transistors.

Device Name	Condition	Pre-Radiation	Post-Radiation
NPNA	$I_D = 1\mu A$	94.2 [91.8, 96.5]	0.39 [0.38, 0.4]
	$I_D = 10\mu A$	127 [124, 129]	1.11 [1.09, 1.12]
	$I_D = 100\mu A$	171 [169, 172]	3.17 [3.13, 3.21]
	$I_D = 1mA$	210 [209, 211]	9.07 [8.95, 9.18]
DUALNPN	$I_D = 1\mu A$	116 [105, 127]	20.6 [16, 26.3]
	$I_D = 10\mu A$	175 [164, 187]	13.1 [11.7, 14.6]
	$I_D = 100\mu A$	230 [221, 241]	20.7 [19.6, 21.5]
	$I_D = 1mA$	276 [268, 285]	43.1 [41.2, 44.2]
2DUALNPN	$I_D = 1\mu A$	102 [83.4, 124]	38.9 [34.3, 45.2]
	$I_D = 10\mu A$	146 [118, 175]	15.2 [14.3, 16.2]
	$I_D = 100\mu A$	220 [201, 244]	18.3 [17.6, 19.1]
	$I_D = 1mA$	271 [257, 291]	35.7 [34.4, 36.9]

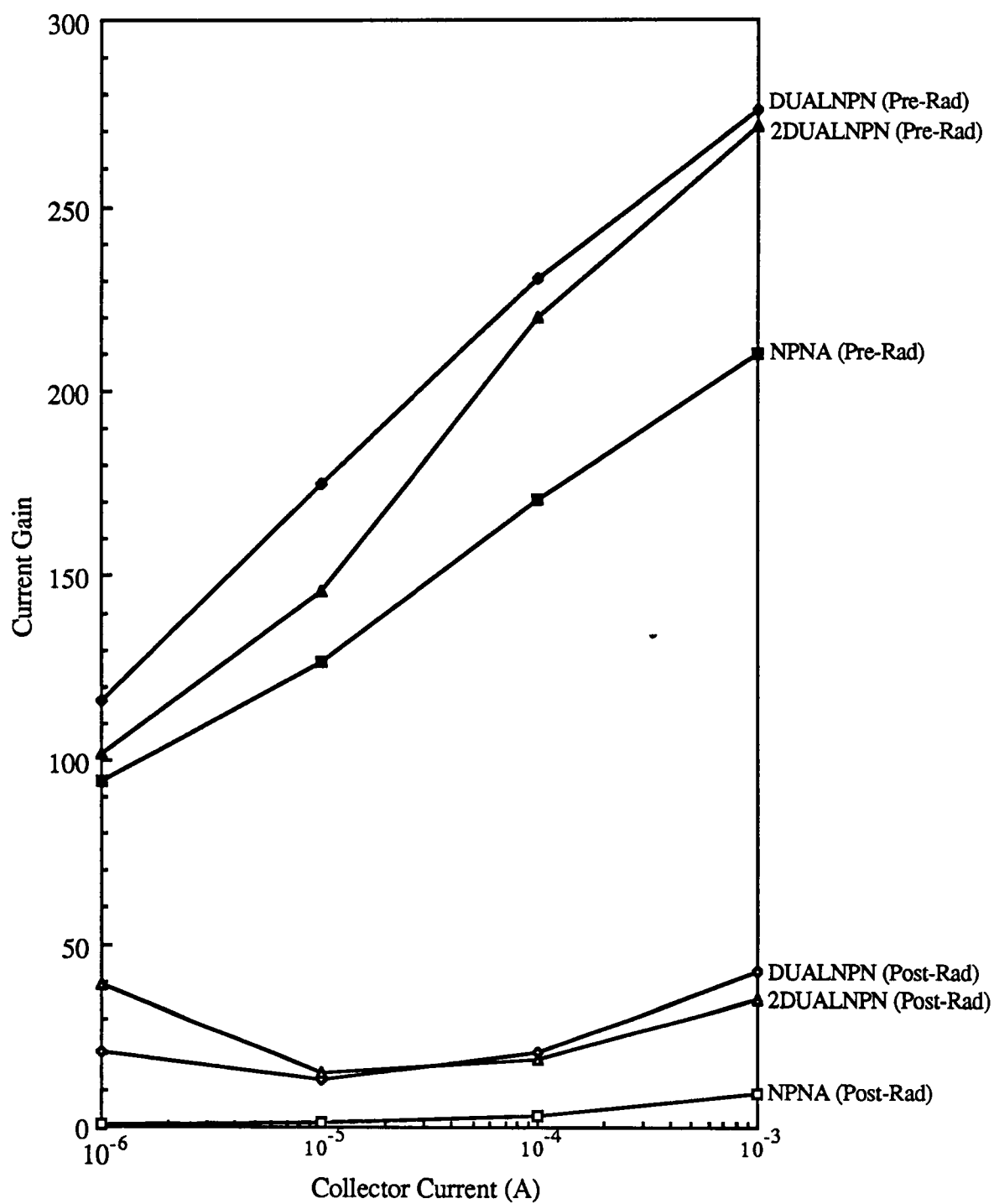


Figure 4-35. Plot of average current gain versus collector current for radiation effect on both vertical and lateral BJT's.

4.4.2.4 Noise Voltage Spectral Density

As mentioned in section 4.4.1.5, the variation of noise voltage spectral density among samples was large both before and after irradiation. Thus, no average value is presented here. Plots of each dual NPN devices for radiation effect, size, and bias condition are provided for analysis. The condition for data taking of BJT was the same as the one presented for that of MOSFET's. Figure 4-36 and Figure 4-37 depicts the noise voltage density spectrum of DUALNPN and 2DUALNPN devices for a pre-radiation condition. No data is presented for after radiation because there were oscillations in the test setup which may have been caused by the unstable loop transmission of the circuit, as well as 60-120 Hz pickup.

A comparison of the pre-irradiation data of Figures 4-36 and 4-37 with the noise data for MOSFETs certainly indicates much lower noise voltage for the bipolars, due primarily to the larger g_m for a bipolar versus a MOSFET. Further the $1/f$ noise corner is generally lower for the bipolar.

4.4.2.5 Junction Capacitance

Figure 4-38 to Figure 4-43 depicts the junction capacitance for the collector-base and base-emitter junctions for all three devices. For DUALNPN's, the C_{CB} increased for all units after the radiation exposure, but the base-emitter capacitance did not show such trend. C_{EB} increased for two units and decreased for the other two units. For 2DUALNPN's, C_{CB} decreased. Three out of four units had decreasing C_{EB} after radiation. The variation among units and chips were large.

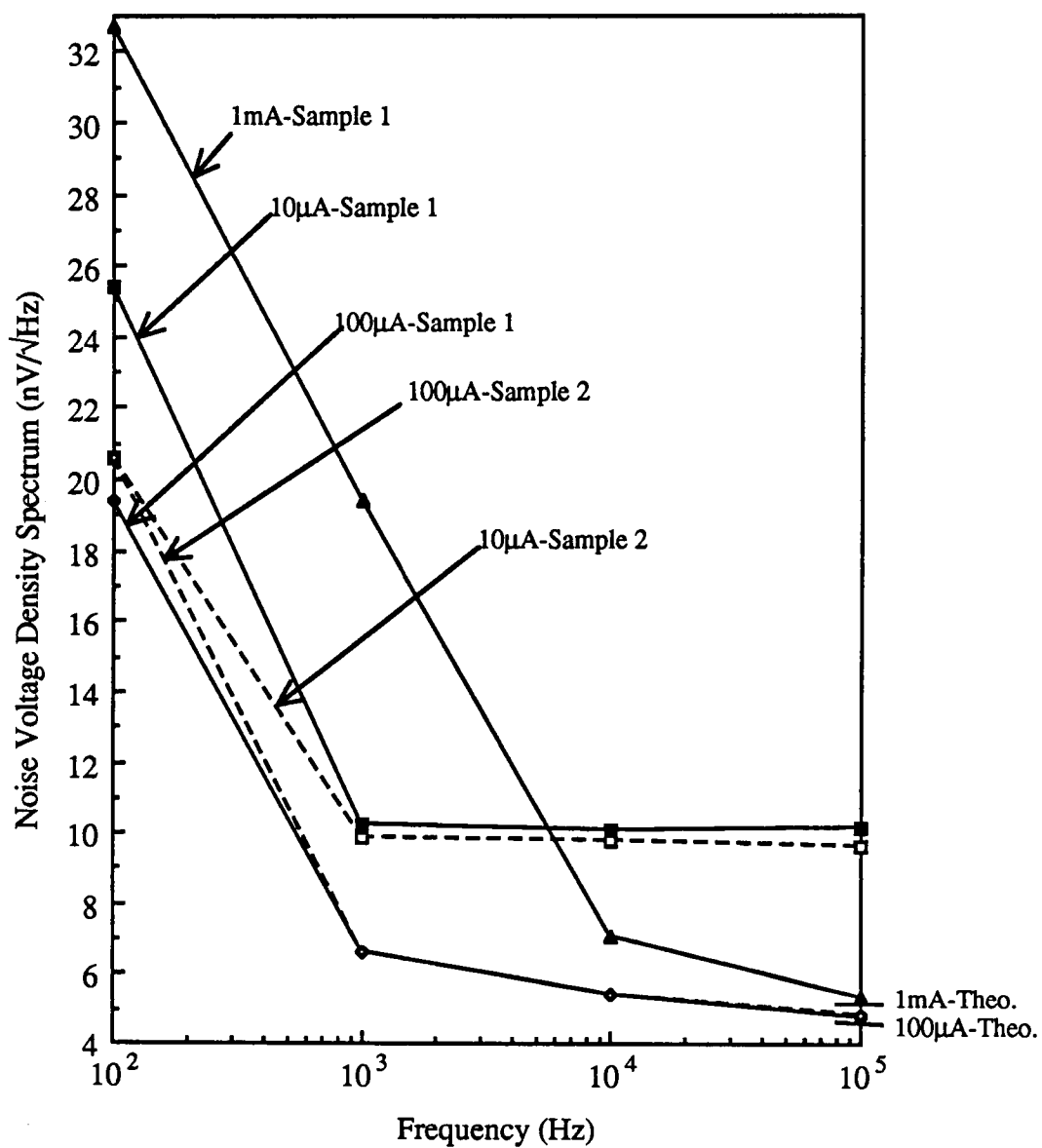


Figure 4-36. Plot of noise voltage density spectrum of DUALNPN versus frequency for various drain currents before radiation.

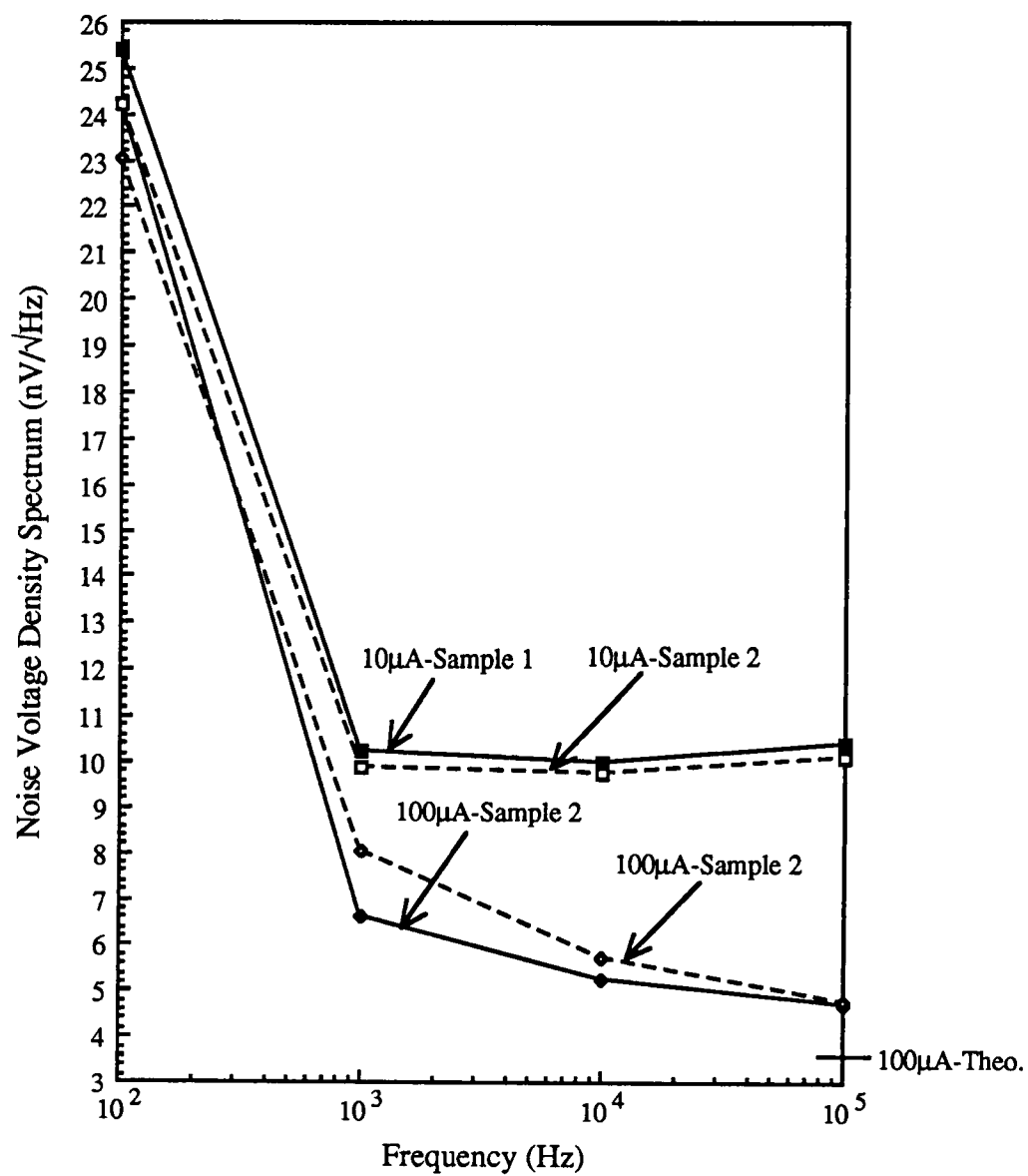


Figure 4-37. Plot of noise voltage density spectrum of 2DUALNPN versus frequency for various drain currents before radiation.

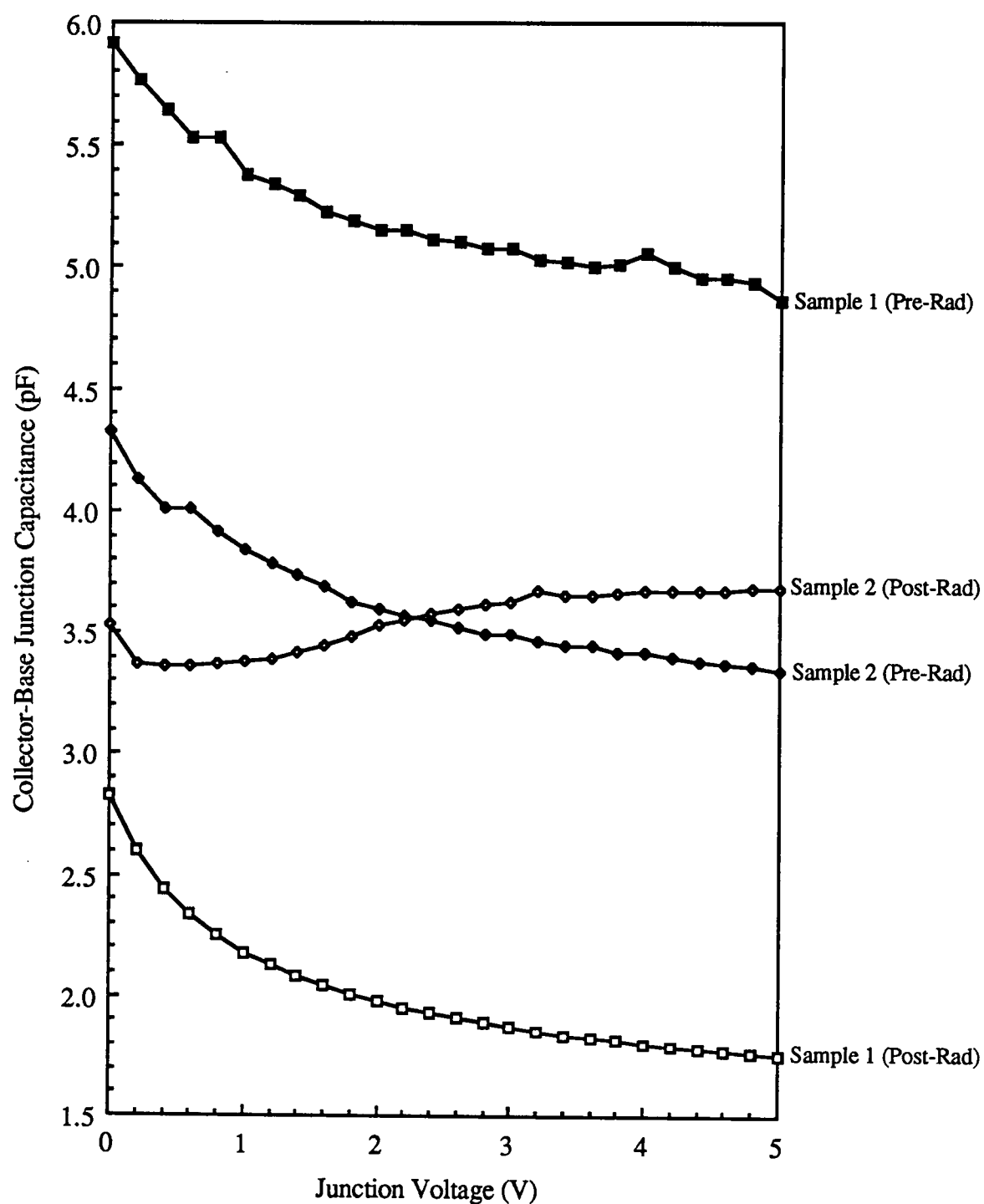


Figure 4-38. Plot of collector-base junction capacitance versus junction voltage for radiation effect on NPNA.

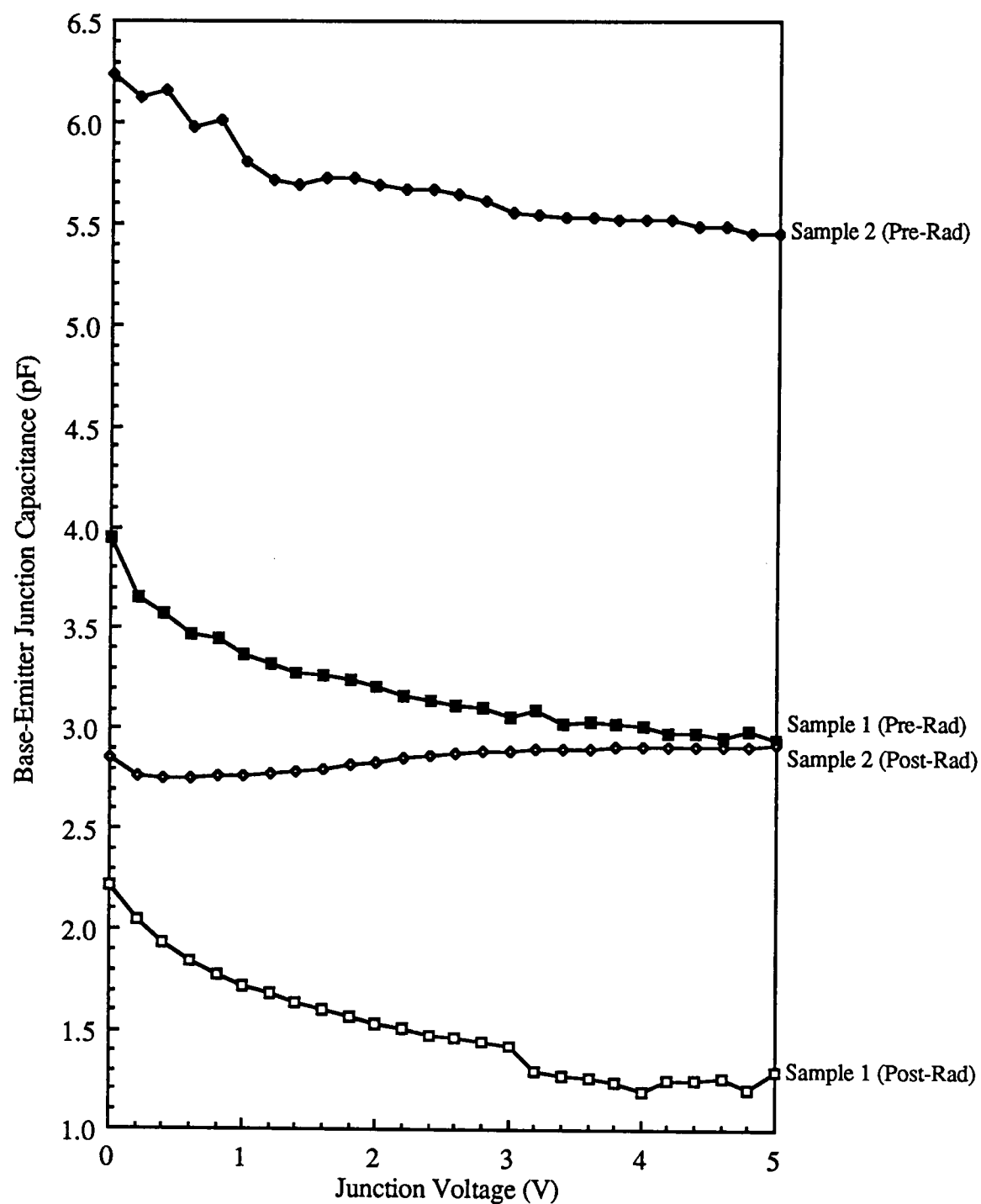


Figure 4-39. Plot of base-emitter junction capacitance versus junction voltage for radiation effect on NPNA.

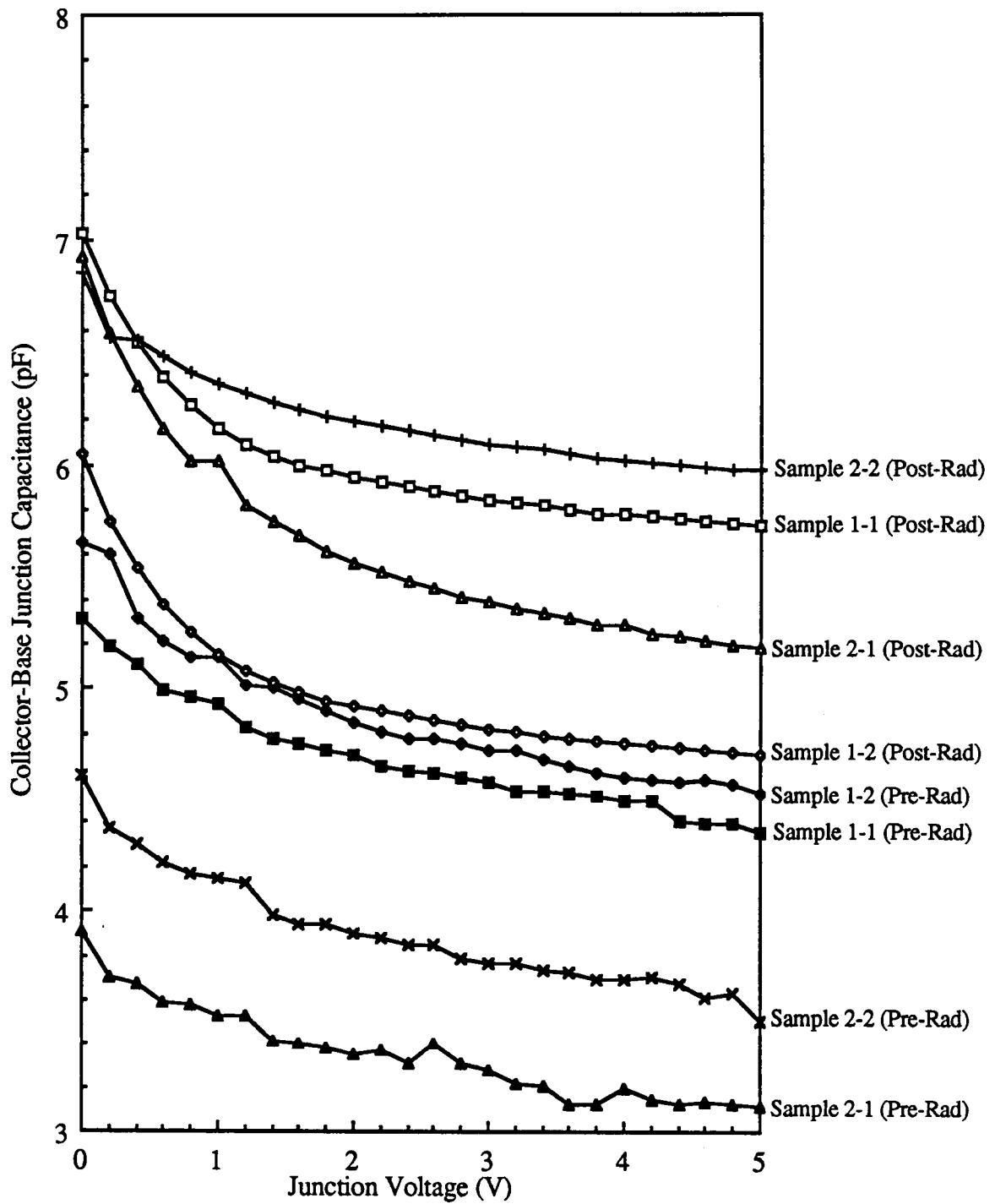


Figure 4-40. Plot of collector-base junction capacitance versus junction voltage for radiation effect on DUALNPN.

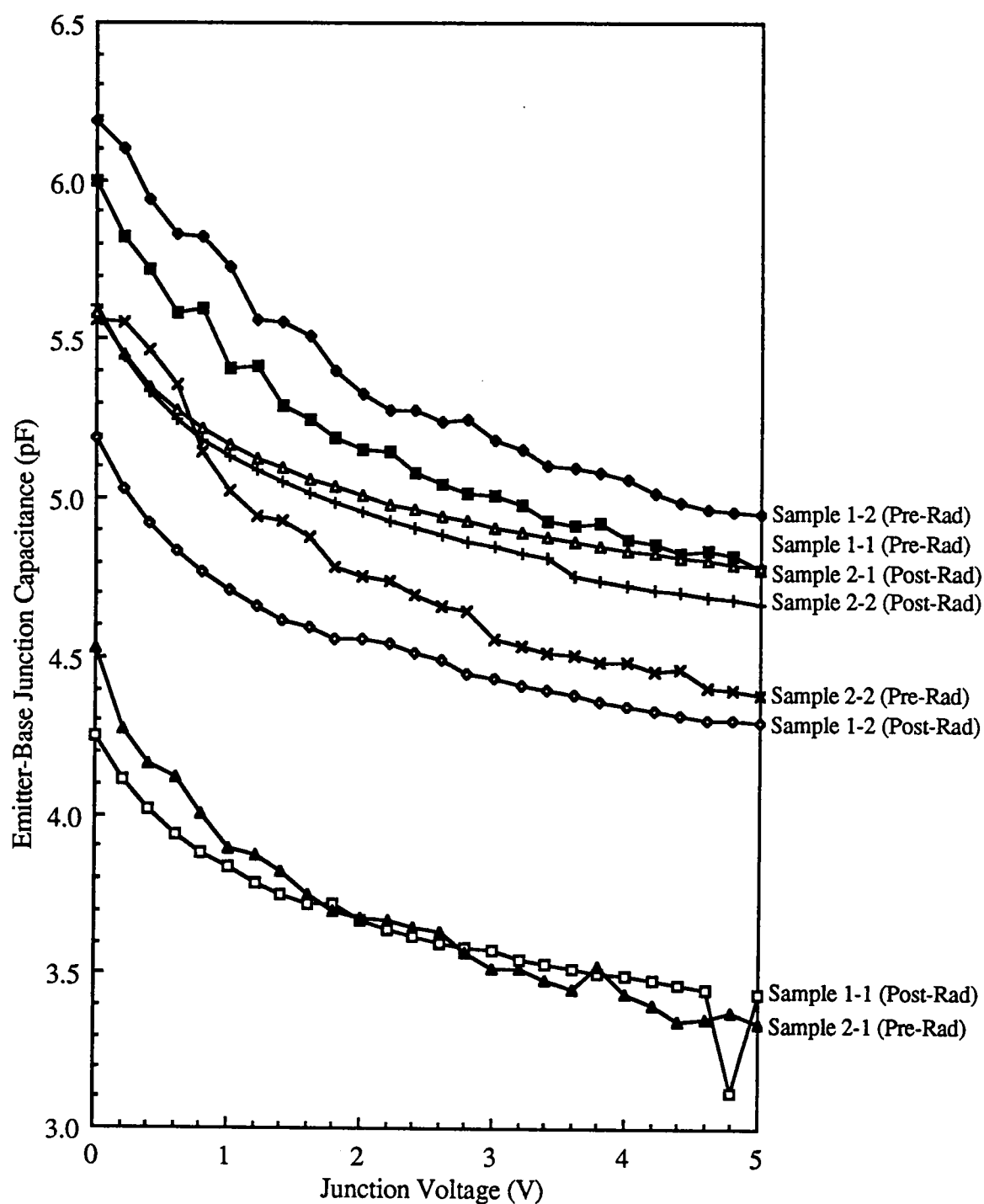


Figure 4-41. Plot of base-emitter junction capacitance versus junction voltage for radiation effect on DUALNPN.

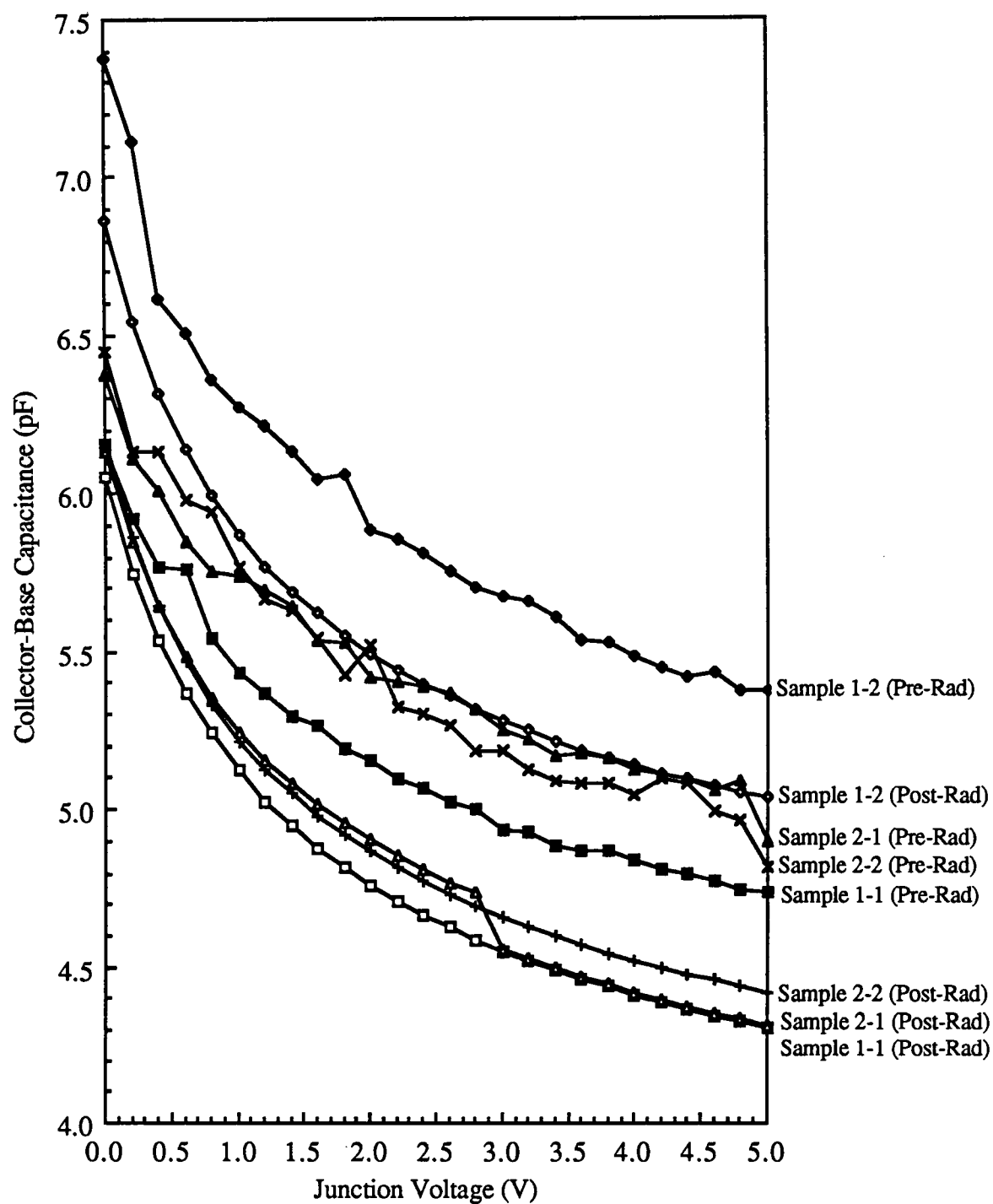


Figure 4-42. Plot of collector-base junction capacitance versus junction voltage for radiation effect on 2DUALNPN.

4.4.2.6 Gain-Bandwidth Product (f_T)

Some of the parameters associated with the small-signal hybrid- π model of bipolar transistors are interesting to investigate because the important parameter, frequency response (f_T) is a measure of the maximum useful frequency when the transistor is used as an amplifier [16].

$$f_T \approx g_m / 2\pi [C_\pi + C_\mu (1 + R_C g_m)] \quad (9)$$

where

$$g_m = \alpha / r_e = (q / kT) I_C \quad \text{transconductance.}$$

$$(q / kT) = 1 / V_T = 1 / (25.9 \text{ mV at } T = 300 \text{ }^\circ\text{K})$$

I_C is collector current

$C_\pi = C_d + C_{je}$ the sum of base diffusion capacitance and emitter-base depletion layer

C_μ = base-collector junction capacitance.

R_C is the collector ohmic (internal) resistance

For ac small-signal mode, resistance and capacitance were measured by the Hewlett Packard LF Impedance Analyzer Model HP4192A across the base and emitter terminals with emitter at a virtual ground while the transistors were being biased at various collector currents. The LF Impedance Analyzer measures two types of circuit modes. One is series resistance (R) and capacitance (X) across the terminal and the other is the parallel connection of conductance (G) and capacitance (B).

At high frequencies, series resistance seen by the analyzer is mainly due to the base resistance. Therefore, $R = r_b$. At low frequency, the following equation is derived based

upon the hybrid $-\pi$ model [21] :

$$\begin{aligned} G + jB &= 1 / (r_b + \{ r_\pi / [1 + j\omega r_\pi (C_\pi + C_\mu)] \}) \\ &= [1 + j\omega r_\pi (C_\pi + C_\mu)] / [(r_b + r_\pi) + j\omega r_\pi r_b (C_\pi + C_\mu)] \end{aligned}$$

After several steps of equation manipulation, B is equivalent as the following :

$$B = [\omega(r_\pi)^2 (C_\pi + C_\mu)] / (r_\pi + r_b)^2 + (r_\pi r_b)^2 (C_\pi + C_\mu)^2 \quad (10)$$

Solving Equation (10) which is a second power of polynomial in terms of $(C_\pi + C_\mu)$, the approximate relation between the desired capacitance and the measured values is shown as :

$$C_\pi + C_\mu \approx (B / 2\pi f) [(r_b / r_\pi) + 1]^2 .$$

Based on the above derivation, calculations of $C_\pi + C_\mu$ were made for each interested low frequency corresponding with each r_b measured; then f_T is found using Equation (9) in which the collector-resistance effect was not included in the calculations.. Table 4-11 shows the average values and deviation range of the current-gain bandwidth product. The base series resistance (r_b) is a frequency dependent parameter as indicated in Table 4-12, and as anticipated it increased after radiation due to charge buildup near the emitter-base junction.

Figure 4-44 depicts the decrease of f_T after radiation. The collector resistance can be large for these transistors; therefore, the actual f_T values are lower than those shown in Figure 4-44. Dual transistors were found to have excellent matching of their r_b and f_T , but both r_b and f_T varied much between chips due to process variation within the same run. Larger transistors, such as 2DUALNPN, are expected to have lower r_b as it has more area which is inversely proportional to resistance. The larger size 2DUALNPN suffered greater f_T decreases after radiation than did the DUALNPN.

Table 4-11. List of average values and deviation range for gain-bandwidth product of BJT's.

Device Name	Condition	Pre-Radiation	Post-Radiation	Unit
NPNA	$I_C = 100\mu A$	3.74 [3.44, 4.04]	7.69 [5.51, 9.87]	MHz
	$I_C = 1mA$	185 [119, 251]	55.2 [21.4, 89.0]	MHz
	$I_C = 5mA$	401 [24.1, 779]	14.3 [13.5, 15.1]	MHz
DUALNPN	$I_C = 100\mu A$	25.4 [6.69, 48.4]	28.4 [25.2, 35.8]	MHz
	$I_C = 1mA$	176 [49.0, 241]	124 [70.8, 149]	MHz
	$I_C = 5mA$	133 [117, 142]	276 [92.4, 814]	MHz
2DUALNPN	$I_C = 100\mu A$	38.4 [32.0, 41.0]	25.0 [23.1, 26.5]	MHz
	$I_C = 1mA$	172 [162, 183]	63.6 [58.3, 68.2]	MHz
	$I_C = 5mA$	108 [97.6, 112]	53.3 [50.5, 55.8]	MHz

Table 4-12. List of average values and deviation range for base series resistance of BJT's.

Device Name	Condition	Frequency (MHz)	Pre-Radiation (Ω)	Post-Radiation (Ω)
NPNA	$I_C = 100\mu A$	1	601 [309, 893]	821 [719, 722]
		10	374 [71, 678]	465 [447, 484]
	$I_C = 1mA$	1	1459 [873, 2037]	661 [608, 715]
		10	595 [595, 596]	364 [364, 365]
	$I_C = 5mA$	1	444 [141, 747]	176
		10	180 [35, 326]	42 [42, 43]
DUALNPN	$I_C = 100\mu A$	1	490 [132, 911]	695 [690, 700]
		10	236 [64, 418]	427 [423, 430]
	$I_C = 1mA$	1	361 [157, 449]	487 [457, 508]
		10	184 [78.5, 219]	221 [201, 233]
	$I_C = 5mA$	1	144 [136, 152]	173 [164, 182]
		10	68 [63, 72]	65 [60, 70]
2DUALNPN	$I_C = 100\mu A$	1	793 [788, 802]	788 [788, 790]
		10	401 [387, 413]	497 [489, 511]
	$I_C = 1mA$	1	409 [387, 413]	669 [646, 692]
		10	205 [195, 214]	305 [266, 340]
	$I_C = 5mA$	1	129 [120, 137]	186 [184, 188]
		10	57 [52, 62]	47 [47, 48]

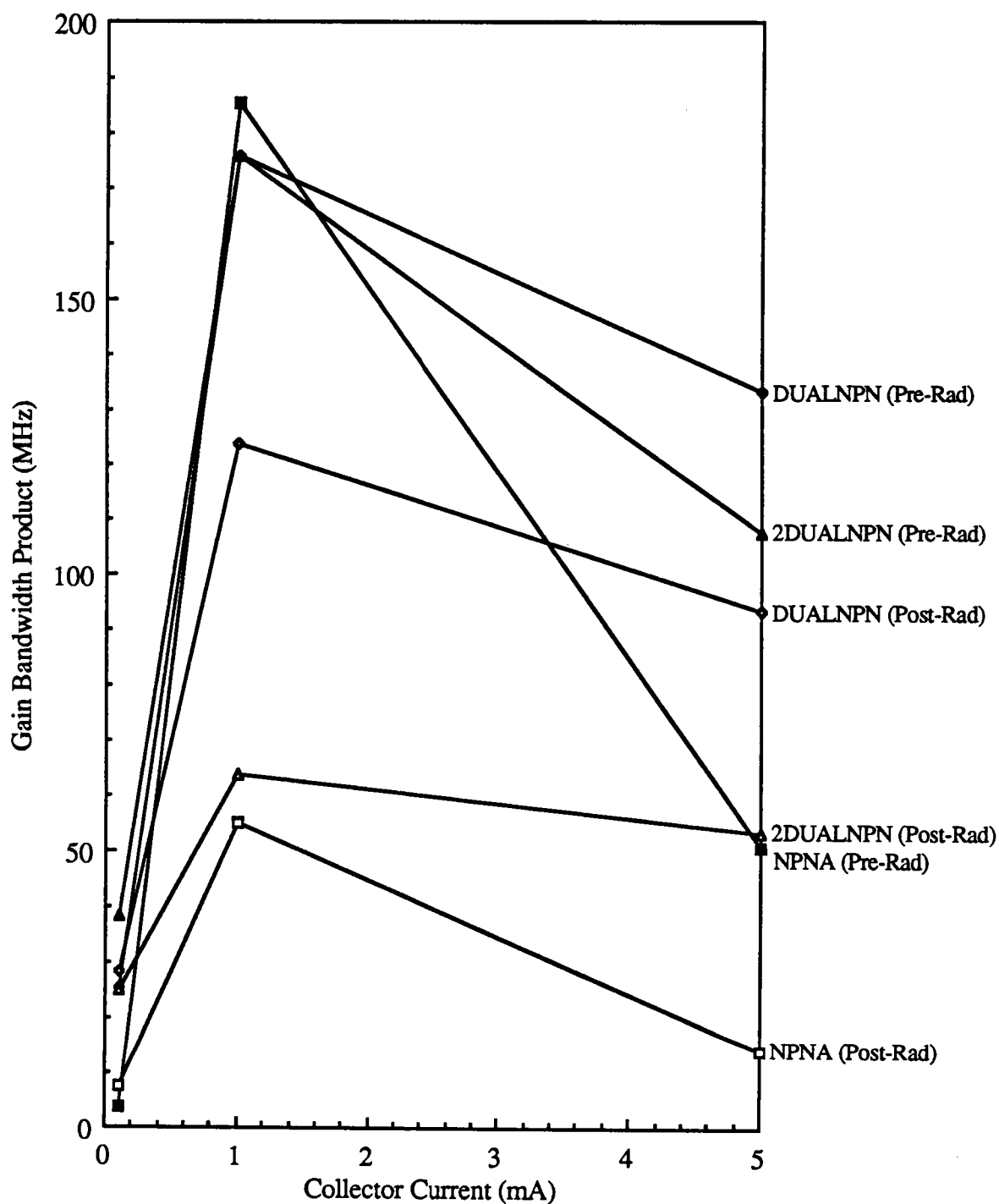


Figure 4-44. Plot of average values of gain-bandwidth product versus collector current for radiation effect on BJT's.

CHAPTER V

CONCLUSIONS AND SUGGESTIONS FOR FURTHER STUDY

Combining digital design in very large scale integration (VLSI) with analog signal processing on the same integrated chips is the future trend since compact, low mass, and low power consumption products are in demand. The more understanding of the technology is being used, the better capability of the design can be produced to be used in the radioactive surroundings. As for MOSIS test chips, more study need to be researched specially in the area of noise. Additional time is required to probe the problems occurred during testing. Automated setup for noise measurement attached with different test fixture for all types of devices deserves much attention and time to investigate and to implement such method. Further, considerable improvement in the noise measurement system is demanded, particularly to lower the residual noise in other components and to have circuits that adapt to the large offset voltages anticipated.

In conclusion, the regular CMOS fabrication process provided by MOSIS cannot generally be used for radiation applications requiring beyond a few kilorad gamma dose. Application for these lower doses using this type of process needs further testing in order to define the maximum tolerable radiation level. Only very special radiation-hardened semiconductor IC fabrication process can be utilized for greater than an one megarad environment. One significant event observed was that the process created non-uniform diffusion across the wafer which caused large variation among device parameters despite the effort of common-centroid layout configuration. This variation became more apparent after radiation. The tested commercial discrete and IC components evaluated during the first phase of this thesis are not normally recommended to be used for a total dose of 10

megarads. However, by careful selection and testing it is possible to find devices that can be used in a ten megarad (gamma) environment.

A systematic study on the comparison of the parameters of chips fabricated with p-well and n-well process runs can contribute to the circuit design later on when the design is simulated by SPICE on a computer, like many of the discrete and IC's which are already available. Also, the GaAs process should be investigated in the future in order to have a complete picture of using computer simulation for the inexpensive fabrication processes. The method used to find the gain bandwidth product of the bipolar transistors needs further study to verify its accuracy, even though the values were found to be reasonable and compatible to other findings [22].

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APPENDICES

APPENDIX A

TEST DATA FOR COMMERCIAL COMPONENTS

The experimental data taken before and after irradiations are presented in this appendix. The arrangement of the data is shown as below:

ANALOG SWITCHES	PAGE
D125 BK (Intersil)	108
D125 BP (Siliconix, Inc.)	109
D126 BK (Intersil)	110
D126 BP (Siliconix, Inc.)	111
D129 BK (Intersil)	112
D129 BP (Siliconix, Inc.)	113
DG145 BP (Siliconix, Inc.)	114
OPERATIONAL AMPLIFIERS	PAGE
CA3280 AE (RCA)	115
CA3450 E (RCA)	118
LT1028 ACJ (Linear Technology)	120
OP42 EZ (Precision Monolithics, Inc.)	122
OP470 EY/FY (PMI)	124
OPA111 SM (Burr-Brown)	127
OPA606 KP (Burr-Brown)	129

OPERATIONAL AMPLIFIERS	PAGE
RC4227 FNB (Raytheon)	132
SL9999 C (Plessey Semiconductor)	134
SENSORS	PAGE
KTY 81 (Amperex)	135
KTY 83 (Amperex)	136
TRANSISTOR ARRAYS	PAGE
EP2015 ACN (Elantec)	137
LM3146 N (National Semiconductor)	138
MAT02 BH (Precision Monolithic, Inc.)	139

TEST DATA FOR ANALOG SWITCHES

Device Name: D125 BK
 Manufacturer: Intersil
 Sample Size: 5
 Date Code: S8537

Parameter	S/N	Pre- Radiation	Post-Radiation					
			C1	C2	C3	C4	C5	C6
Turn-On Time (μ s)	1	---	0.38	0.25	0.40	0.38	0.35	0.30
	2	---	0.35	0.30	0.30	0.40	0.40	0.35
	3	---	0.35	0.40	0.38	0.30	0.40	0.38
	4	---	0.38	0.39	0.36	0.32	0.30	0.35
	5	---	0.38	0.35	0.32	0.38	0.35	0.32
Turn-Off Time (μ s)	1	---	0.20	0.20	0.20	0.20	0.18	0.18
	2	---	0.17	0.15	0.22	0.15	0.17	0.18
	3	---	0.25	0.15	0.17	0.15	0.20	0.20
	4	---	0.19	0.19	0.20	0.20	0.20	0.20
	5	---	0.20	0.20	0.19	0.20	0.20	0.20
Rise Time (μ s) [10%-90%]	1	---	0.60	0.50	0.65	0.70	0.58	0.60
	2	---	0.63	0.55	0.58	0.45	0.45	0.45
	3	---	0.65	0.48	0.65	0.62	0.65	0.55
	4	---	0.58	0.48	0.54	0.48	0.50	0.50
	5	---	0.50	0.52	0.47	0.48	0.50	0.45

Test Conditions: $V(L) = 5V$, $V^- = -20V$, $I_{out} = 2mA$, $C_{out} = 35pF$

- Notes: 1. Bad oscillation at high frequency.
 2. No data were taken before irradiation.
 3. Operational amplifier on the output driver may be bad. $V_{out} = 80mV$

TEST DATA FOR ANALOG SWITCHES

Device Name: D125 BP
 Manufacturer: Siliconix, Inc.
 Sample Size: 5
 Date Code: H8636

Parameter	S/N	Pre- Radiation	Post-Radiation					
			C1	C2	C3	C4	C5	C6
Turn-On Time (μ s)	1	---	0.25	0.25	0.25	0.20	0.25	0.25
	2	---	0.26	0.22	0.22	0.25	0.22	0.25
	3	---	0.22	0.26	0.22	0.22	0.21	0.26
	4	---	0.30	0.30	0.22	0.22	0.25	0.35
	5	---	0.20	0.40	0.22	0.38	0.30	0.38
Turn-Off Time (μ s)	1	---	0.20	0.10	0.08	0.12	0.15	0.08
	2	---	0.08	0.14	0.14	0.14	0.12	0.12
	3	---	0.13	0.10	0.12	0.18	0.12	0.08
	4	---	0.12	0.12	0.14	0.08	0.12	0.14
	5	---	0.08	0.15	0.10	0.10	0.07	0.06
Rise Time (μ s) [10%-90%]	1	---	0.45	0.50	0.40	0.50	0.52	0.52
	2	---	0.45	0.48	0.45	0.45	0.45	0.45
	3	---	0.55	0.45	0.38	0.42	0.52	0.42
	4	---	0.58	0.42	0.62	0.58	0.43	0.58
	5	---	0.60	0.46	0.52	0.44	0.42	0.43

Test Conditions: $V(L) = 5V$, $V^- = -20V$, $I_{out} = 2mA$, $C_{out} = 35pF$

- Notes: 1. Bad oscillation at high frequency.
 2. No data were taken before irradiation.
 3. Operational amplifier on the output driver may be bad. $V_{out} = 0.135V$

TEST DATA FOR ANALOG SWITCHES

Device Name: DG126 BK

Manufacturer: Intersil

Sample Size: 5

Date Code: S8711

Parameter	S/N	Pre- Radiation	Post-Radiation			
			S1	S2	S3	S4
Turn-On Time (ns)	1	---	7.7	7.5	8.0	7.6
	2	---	7.9	7.9	7.7	7.6
	3	---	8.2	8.1	8.0	8.0
	4	---	5.0	7.0	8.5	8.0
	5	---	8.3	8.1	8.0	8.3
Turn-Off Time (ns)	1	---	7.0	7.0	7.4	7.2
	2	---	7.3	8.0	7.4	7.3
	3	---	7.8	7.2	6.8	7.4
	4	---	6.0	5.5	6.5	6.5
	5	---	7.1	7.4	6.9	6.8
Rise Time (ns) [10%-90%]	1	---	20.8	21.2	21.6	20.8
	2	---	23.8	23.6	23.0	23.2
	3	---	23.2	23.2	23.0	23.0
	4	---	35.0	34.0	35.0	35.2
	5	---	24.0	24.4	23.6	24.3
Drain-Source On Resistance (Ω)	1	---	22.25	24.88	29.00	24.13
	2	---	23.13	23.50	21.63	21.63
	3	---	22.63	23.00	23.25	24.84
	4	---	23.58	21.20	23.09	23.81
	5	---	23.50	25.00	22.13	22.25

Test Conditions: $V^+ = 12\text{ V}$, $V^- = -18\text{ V}$, $V_R = 0\text{ V}$, $V_{IN} = 5\text{ V}$, $R_L = 1\text{ k}\Omega$,
 $C_{out} = 10\text{ pF}$, $V_{drain} = 8\text{ V}$ for R_{DS} (ON)

Notes: 1. Bad oscillation at high frequency.
 2. No data were taken before irradiation.

TEST DATA FOR ANALOG SWITCHES

Device Name: DG126 BP
 Manufacturer: Siliconix, Inc.
 Sample Size: 4
 Date Code: H8618

Parameter	S/N	Pre-Radiation		Post-Radiation	
		S1	S2	S1	S2
Turn-On Time (ns)	1	240	220	8	6
	2	220	240	9	6
	3	260	260	10	9
	4	280	220	7	5
Turn-Off Time (μ s)	1	1.12	1.24	0.12	0.15
	2	1.25	1.23	0.075	0.155
	3	1.06	1.13	0.055	0.105
	4	1.24	1.15	0.17	0.205
Rise Time (μ s) [10%-90%]	1	1.62	1.76	0.05	0.031
	2	1.72	1.70	0.031	0.032
	3	1.72	1.60	0.03	0.032
	4	1.80	1.66	0.033	0.031
Drain-Source On Resistance (Ω)	1	23.62	23.55	24.27	23.65
	2	23.22	23.81	23.50	22.64
	3	24.88	20.90	25.12	21.24
	4	22.01	20.83	22.20	21.12

Test Conditions: $V^+ = 12\text{ V}$, $V^- = -18\text{ V}$, $V_R = 0\text{ V}$, $V_{IN} = 5\text{ V}$,
 $R_L = 1\text{ k}\Omega$, $C_{out} = 10\text{ pF}$, $V_{drain} = 8\text{ V}$ for $R_{DS}(\text{ON})$

TEST DATA FOR ANALOG SWITCHES

Device Name: DG129 BK

Manufacturer: Intersil

Sample Size: 5

Date Code: S8711

Parameter	S/N	Pre-Radiation	Post-Radiation			
			S1	S2	S3	S4
Turn-On Time (ns)	1	---	8.5	8.0	8.0	7.9
	2	---	7.8	7.6	7.7	7.3
	3	---	7.2	8.0	7.7	7.7
	4	---	7.8	7.4	8.1	7.9
	5	---	7.6	7.3	7.4	7.8
Turn-Off Time (ns)	1	---	6.4	7.3	7.0	6.7
	2	---	4.2	4.4	4.2	6.9
	3	---	7.6	7.8	7.9	8.0
	4	---	7.4	7.1	7.2	7.8
	5	---	8.0	8.7	7.9	7.2
Rise Time (ns) [10%-90%]	1	---	22.8	19.0	23.0	19.2
	2	---	21.2	22.0	20.8	22.5
	3	---	23.0	22.3	22.8	19.8
	4	---	19.4	19.8	19.8	19.1
	5	---	19.5	19.9	20.6	19.9
Drain-Source On Resistance (Ω)	1	---	21.75	24.00	22.63	22.13
	2	---	22.75	21.50	23.94	23.25
	3	---	22.63	23.04	22.00	22.83
	4	---	21.88	25.50	13.00	25.25
	5	---	22.89	24.25	24.75	24.63

Test Conditions: $V^+ = 12\text{ V}$, $V^- = -18\text{ V}$, $V_R = 0\text{ V}$, $V_{IN} = 5\text{ V}$, $R_L = 1\text{ k}\Omega$, $C_{out} = 10\text{ pF}$, $V_{drain} = 8\text{ V}$ for $R_{DS}(\text{ON})$

Note: No data were taken before irradiation.

TEST DATA FOR ANALOG SWITCHES

Device Name: DG129 BP
 Manufacturer: Siliconix, Inc.
 Sample Size: 4
 Date Code: H8618

Parameter	S/N	Pre-Radiation		Post-Radiation	
		S1	S2	S1	S2
Turn-On Time (ns)	1	205	205	8.5	9
	2	240	240	10	9
	3	238	240	10	9.8
	4	256	230	8	10
Turn-Off Time (ns)	1	900	905	97.5	95
	2	850	815	45	70
	3	855	860	65	65
	4	1095	1105	160	140
Rise Time (ns) [10%-90%]	1	180	200	32	35
	2	200	165	34	32.5
	3	300	310	31.5	32.5
	4	300	300	32.5	31.5
Drain-Source On Resistance (Ω)	1	21.02	22.34	21.08	22.28
	2	24.79	25.00	25.73	25.31
	3	20.90	24.32	20.81	24.28
	4	24.44	22.67	25.27	22.65

Test Conditions: $V^+ = 12\text{ V}$, $V^- = -18\text{ V}$, $V_R = 0\text{ V}$, $V_{IN} = 5\text{ V}$,
 $R_L = 1\text{ k}\Omega$, $C_{out} = 10\text{ pF}$, $V_{drain} = 8\text{ V}$ for R_{DS} (ON)

TEST DATA FOR ANALOG SWITCHES

Device Name: DG145 BP
 Manufacturer: Siliconix, Inc.
 Sample Size: 4
 Date Code: H8648

Parameter	S/N	Pre-Radiation				Post-Radiation
		S1	S2	S3	S4	
Turn-On Time (μ s)	1	0.290	0.298	0.286	0.304	---
	2	0.282	---	0.284	---	---
	3	0.296	0.300	0.300	0.318	---
	4	0.304	0.304	0.294	0.304	---
Turn-Off Time (μ s)	1	0.895	0.875	0.895	0.870	---
	2	0.870	---	0.885	---	---
	3	0.810	0.835	0.820	0.810	---
	4	0.810	0.850	0.810	0.855	---
Rise Time (μ s) [10%-90%]	1	0.205	0.200	0.200	0.205	---
	2	0.195	---	0.200	---	---
	3	0.185	0.190	0.195	0.200	---
	4	0.195	0.185	0.205	0.200	---
Drain-Source On Resistance (Ω)	1	6.52	6.97	6.63	6.92	---
	2	7.97	---	6.97	---	---
	3	8.34	7.17	7.93	7.90	---
	4	7.85	7.98	7.90	7.30	---

Test Conditions: $V^+ = 12$ V, $V^- = -18$ V, $V_R = 0$ V, $V_{IN} = 5$ V, $R_L = 1$ k Ω ,
 $C_{out} = 10$ pF, $V_{drain} = 8$ V for R_{DS} (ON)

Note: 1. Two switches of sample #2 did not function before irradiation.
 2. All other switches failed to switch after irradiation.

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: CA3280 AE

Manufacturer: RCA

Sample Size: 4

Date Code: H615

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)		1A	0.30	---
		1B	0.12	---
		2A	0.50	---
		2B	0.46	-0.49
		3A	0.30	-1.20
		3B	0.48	---
		4A	0.30	-0.71
		4B	0.46	-0.38
Output Saturation Voltages (V)	50 k Ω load	1A	13.90/-14.54	---
		1B	13.60/-14.16	---
		2A	13.60/-14.30	---
		2B	13.62/-14.18	13.54/-14.28
		3A	13.60/-14.24	13.59/-14.40
		3B	13.60/-14.16	---
		4A	13.60/-14.06	13.64/-14.36
		4B	13.62/-14.26	13.60/-14.40
	10 k load	1A	3.53/-3.50	---
		1B	3.43/-3.41	---
		2A	3.57/-3.49	---
		2B	3.50/-3.45	3.10/-3.20
		3A	3.43/-3.45	3.10/-3.21
		3B	3.45/-3.40	---
		4A	3.56/-3.50	3.37/-3.41
		4B	3.54/-3.44	3.30/-3.30
Open-Loop Gain (dB)	50 k Ω load	1A	47.86	---
		1B	47.61	---
		2A	48.08	---
		2B	47.82	44.80
		3A	47.60	44.86
		3B	47.58	---
		4A	47.93	46.83
		4B	47.88	46.24
Common Mode Rejection Ratio (dB)		1A	80.71	---
		1B	84.15	---

OPERATIONAL AMPLIFIER - CA3280 AE (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Common Mode Rejection Ratio (dB)		2A	83.63	---
		2B	84.82	68.05
		3A	83.99	68.07
		3B	84.45	---
		4A	84.34	68.06
		4B	84.53	68.15
Power Supply Rejection Ratio (dB)	[+/-]	1A	116.0/117.2	---
		1B	111.1/>142.4	---
		2A	120.1/113.3	---
		2B	114.7/119.1	86.57/119.93
		3A	127.8/110.9	85.50/104.42
		3B	116.0/117.9	---
		4A	110.2/136.4	87.01/142.41
		4B	112.3/127.0	86.88/118.89
Input Bias Currents (μ A)	[+/-]	1A	1.91/1.91	---
		1B	1.85/1.85	---
		2A	2.01/2.01	---
		2B	1.94/1.95	7.70/8.80
		3A	2.19/2.19	6310/3690
		3B	2.04/2.05	---
		4A	1.21/1.21	5.79/5.38
		4B	1.20/1.20	2300/-200
Power Supply Currents (mA)	[+/-]	1A	2.00/-1.95	---
		1B	1.91/-1.89	---
		2A	1.94/-1.96	---
		2B	1.90/-1.89	0.39/-0.96
		3A	1.95/-1.90	1.93/-1.91
		3B	1.90/-1.85	---
		4A	1.90/-1.90	1.97/-1.97
		4B	1.91/-1.90	1.96/-1.95
Slew Rate (V/ μ s)		1A	2.39/2.68	---
		1B	2.50/2.88	---
		2A	2.00/2.40	---
		2B	2.00/2.87	0.87/0.54
		3A	3.38/2.75	0.71/0.58
		3B	2.74/3.00	---
		4A	2.50/2.32	1.68/1.58
		4B	2.78/2.77	2.20/2.30

OPERATIONAL AMPLIFIER - CA3280 AE (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Gain Bandwidth Product (KHz)	1A		708.2	---
	1B		636.7	---
	2A		136.9	---
	2B		667.5	176.5
	3A		669.5	149.4
	3B		670.9	---
	4A		694.3	162.6
	4B		140.9	158.9

Test Conditions: $V_S = \pm 15\text{ V}$, $R_L = 50\text{ k}\Omega$

- Note: 1. Sample No. 4B had questionable input bias current performance.
 2. Sample No. 1A, 1B, 2A, and 3B stopped functioning after 9 megarad gamma irradiation.

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: CA3450 E

Manufacturer: RCA

Sample Size: 2/2

Date Code: H645/H641

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)		1	-8.00	---
		2	-9.75	2.60
		3	-12.00	-3.10
		4	-10.00	-3.30
Output Saturation Voltages (V)	50 k Ω load	1	4.40/-4.70	---
		2	4.44/-4.56	4.50/-4.56
		3	4.44/-4.76	4.60/-4.68
		4	4.46/-4.60	4.00/-4.60
	1k load	1	4.40/-4.70	---
		2	4.60/-4.56	2.80 /-4.50
		3	4.44/-4.76	4.38/-4.60
		4	4.60/-4.60	1.20/-4.60
Open-Loop Gain (dB)	50 k Ω load	1	81.2	---
		2	87.1	83.58
		3	84.1	80.50
		4	82.9	83.10
Common Mode Rejection Ratio (dB)		1	56.9	---
		2	64.1	66.4
		3	57.5	58.8
		4	54.7	56.3
Power Supply Rejection Ratio (dB)	[+/-]	1	60.0/82.5	---
		2	62.9/70.5	61.0/66.0
		3	60.0/78.1	59.2/77.4
		4	60.0/72.5	67.5/74.7
Input Bias Currents (nA)	[+/-]	1	100/100	---
		2	64/44	540/880
		3	-72/-76	280/720
		4	-88/-98	140/240
Power Supply Currents (mA)	[+/-]	1	20.6/-20.6	---
		2	20.6/-20.4	29.5/-28.0
		3	20.6/-20.4	22.5/-23.0

OPERATIONAL AMPLIFIER - CA3450 E (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Power Supply Currents (mA)		4	20.8/-20.7	24.0/-24.0
Slew Rate (V/ μ s)	[+/-]	1	210/96	---
		2	110/112	93.4/111
		3	290/118	84.0/123
		4	86/116	88.0/125
Gain Bandwidth Product (MHz)		1	191.5	---
		2	207.5	176
		3	190.5	137
		4	196.5	134

Test Conditions: $V_S = \pm 7\text{ V}$, $R_C = 14\text{ pF}$

Note: Sample #1 stopped functioning after 10 megarad gamma irradiation.

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: LT1028 ACJ8
 Manufacturer: Linear Technology
 Sample Size: 1/2
 Date Code: 8712/8616

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (μV)		1	-9.9	---
		2	-6.8	---
		3	18.0	---
		4	-33.0	---
		5	-21.0	---
Output Saturation Voltage (V)	50 k Ω load	1	14.04/-13.24	---
		2	14.02/-13.06	---
		3	13.98/-13.48	---
		4	14.06/-13.18	---
		5	14.20/-13.18	---
	2 k Ω load	1	13.60/-12.78	---
		2	13.50/-12.62	---
		3	13.50/-12.92	---
		4	13.62/-12.78	---
		5	13.62/-12.46	---
Open Loop Gain (dB)	50 k Ω load	1	148.7	---
		2	153.1	---
		3	140.8	---
		4	136.7	---
		5	136.7	---
Common Mode Rejection Ratio (dB)		1	120.2	---
		2	118.6	---
		3	120.7	---
		4	128.1	---
		5	129.5	---
Power Supply Rejection Ratio (dB)	[+/-]	1	133.7/125.9	---
		2	132.1/126.4	---
		3	125.1/125.3	---
		4	133.6/125.0	---
		5	125.8/124.2	---

OPERATIONAL AMPLIFIER - LT1028 ACJ (continued)

Input Bias Current (nA)	[+/-]	1	34.4/44.0	---
		2	45.8/63.0	---
		3	13.0/55.0	---
		4	-47.8/-30.6	---
		5	-50.6/-36.0	---
Power Supply Current (mA)	[+/-]	1	8.20/-8.20	---
		2	8.10/-8.08	---
		3	7.98/-7.98	---
		4	8.26/-8.26	---
		5	8.42/-8.40	---
Slew Rate (V/ μ s)	[+/-]	1	13.00/12.38	---
		2	12.50/11.64	---
		3	12.92/11.73	---
		4	13.15/12.80	---
		5	13.24/12.60	---
Gain Bandwidth Product (MHz)		1	24.2	---
		2	23.7	---
		3	23.8	---
		4	24.3	---
		5	24.4	---

Test Conditions: $V_S = \pm 15$ V

Note: All devices failed to function after the 10 megarad irradiation.

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: OP-42 EZ
 Manufacturer: Precision Monolithics, Inc.
 Sample Size: 5
 Date Code: 8649

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)	2 k Ω load	1	-0.344	-0.74
		2	0.14	-0.442
		3	0.15	1.15
		4	-0.53	-0.62
		5	0.12	-0.1
Output Saturation Voltage (V)	2 k Ω load		12.2/-11.7	12.2/-11.8
Open-Loop Gain (dB)	2 k Ω load	1	109.506	101.584
		2	107.743	102.029
		3	108.980	102.743
		4	107.923	102.743
		5	109.292	101.584
Common Mode Rejection Ratio (dB)		1	100.537	82.991
		2	92.905	85.986
		3	103.973	84.048
		4	99.576	83.270
		5	114.357	69.474
Power Supply Rejection Ratio (dB)	[+/-]	1	127.96/100.37	113.48/87.41
		2	118.21/91.44	95.14/90.56
		3	121.94/95.97	101.73/90.46
		4	118.21/97.31	97.78/102.36
		5	98.49/91.20	95.01/94.62
Input Bias Currents (nA)	[+/-]	1	0.420/0.260	5.0/5.0
		2		5.0/5.0
		3		5.5/5.5
		4		5.0/5.2
		5		6.0/6.0
Power Supply Currents (mA)	[+/-]		6/-7	5.92/-5.82
Slew Rate (V/ μ s)	[+/-]	1	53.0/47.6	25.3/34.0
		2	47.1/47.6	26.4/34.3
		3	47.6/44.4	25.1/34.6
		4	47.1/48.0	26.2/34.9
		5	48.6/48.0	25.3/30.5

OPERATIONAL AMPLIFIER - OP-42 EZ (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Gain Bandwidth Product (MHz)	1		14.1	12.92
	2		15.3	12.86
	3		13.7	12.26
	4		14.1	12.75
	5		14.9	12.94

Test Condition: $V_S = \pm 15\text{ V}$

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: OP-470 EY/FY
 Manufacturer: Precision Monolithics, Inc.
 Sample Size: 2
 Date Code: 8631

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (μ V)		1A	80	112
		1B	16	31
		1C	-21	6
		1D	30	60
		2A	117	115
		2B	52	50
		2C	59	45
		2D	-59	-137
Maximum Output Voltage (V)	50 k Ω load	1A	14.00/-14.16	13.84/-14.00
		1B	14.00/-14.20	13.84/-14.00
		1C	14.00/-14.30	13.84/-14.00
		1D	14.00/-14.34	13.84/-14.00
		2A	13.78/-14.32	13.70/-14.20
		2B	13.80/-14.24	13.70/-14.20
		2C	13.78/-14.26	13.70/-14.20
		2D	14.01/-14.24	13.70/-14.20
Maximum Output Voltage (V)	2 K Ω load	1A	13.20/-13.30	13.06/-12.78
		1B	13.00/-13.36	13.06/-12.76
		1C	13.02/-13.40	13.06/-12.76
		1D	13.00/-13.44	13.06/-12.76
		2A	13.04/-13.34	12.84/-13.20
		2B	13.04/-13.38	12.84/-13.20
		2C	13.22/-13.38	12.84/-13.20
		2D	13.22/-13.40	12.84/-13.20
Open-Loop Gain (dB)		1A	123.9	103.6
		1B	123.2	103.7
		1C	123.0	103.3
		1D	124.7	103.8
		2A	124.9	105.9
		2B	124.1	105.2
		2C	124.1	105.2
		2D	123.9	105.9
Input Bias Currents (nA)	[+/-]	1A	13.9/54.0	769/792
		1B	49.5/26.0	657/772
		1C	33.5/70.6	800/830

OPERATIONAL AMPLIFIER - OP-470 EY/FY (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Input Bias Currents (nA)		1D	69.0/46.0	759/838
		2A	18.9/46.5	368/580
		2B	19.5/27.5	554/570
		2C	28.0/11.2	600/645
		2D	21.3/40.8	590/560
Common Mode Rejection Ratio (dB)		1A	154.3	137.4
		1B	127.5	128.7
		1C	127.9	126.4
		1D	> 154	140.3
		2A	125.3	130.2
		2B	133.4	132.7
		2C	131.4	132.4
		2D	114.3	114.3
Power Supply Rejection Ratio (dB)	[+/-]	1A	120.1/125.2	107.9/107.6
		1B	119.8/117.8	108.0/106.3
		1C	148.3/119.2	109.9/106.2
		1D	138.8/119.4	109.3/107.2
		2A	123.6/212.7	113.6/109.9
		2B	126.3/119.0	110.4/109.1
		2C	120.3/125.5	108.7/108.6
		2D	114.5/120.8	125.0/108.7
Power Supply Currents (mA)	[+/-]	1	7.25/-7.29	7.02/-7.02
		2	6.98/-6.91	6.73/-6.73
Slew Rate (V/ μ s)	[+/-]	1A	1.68/2.00	1.54/1.75
		1B	1.65/1.80	1.48/1.78
		1C	1.53/1.92	1.45/1.72
		1D	1.33/1.30	1.48/1.74
		2A	1.58/1.65	1.48/1.71
		2B	1.23/1.47	1.50/1.75
		2C	1.55/1.58	1.44/1.75
		2D	1.23/1.47	1.48/1.75
Gain Bandwidth Product (MHz)		1A	6.22	4.46
		1B	6.59	4.51
		1C	6.66	4.33
		1D	6.71	4.85
		2A	5.96	4.31
		2B	6.40	4.47

OPERATIONAL AMPLIFIER - OP-470 EY/FY (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Gain Bandwidth Product (MHz)		2C	6.12	4.38
		2D	6.25	4.42

Test Condition: $V_S = \pm 15\text{ V}$

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: OPA111 SM
 Manufacturer: Burr-Brown
 Sample Size: 3/2/1
 Date Code: 8704/8621/8624

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (μ V)		1	-21.0	-115.00
		2	-27.7	-264.00
		3	-29.0	39.50
		4	2.0	19.99
		5	43.0	-9.62
		6	70.0	1.20
Output Saturation Voltage (V)	50 k Ω load	1	13.26/-14.38	13.48/-14.42
		2	13.10/-14.20	13.44/-14.38
		3	13.40/-14.40	13.24/-14.40
		4	13.24/-14.38	13.22/-14.42
		5	13.30/-14.40	13.24/-14.40
		6	13.58/-14.44	13.22/-14.42
	2 k Ω load	1	12.96-13.84	12.90/-13.72
		2	12.80/-14.00	13.18/-13.94
		3	13.16/-13.96	12.88/-13.72
		4	12.90/-13.80	12.84/-13.82
		5	12.90/-13.96	12.84/-13.82
		6	13.20/-14.00	12.82/-13.80
Open Loop Gain (dB)		1	123.5	120.66
		2	121.1	118.03
		3	116.5	123.62
		4	123.7	119.93
		5	124.2	119.87
		6	124.9	120.20
Common Mode Rejection Ratio (dB)		1	118.95	119.24
		2	99.90	99.85
		3	113.17	106.89
		4	109.70	109.16
		5	109.10	107.84
		6	132.00	137.50
Power Supply Rejection Ratio (dB)	[+/-]	1	107.7/104.3	114.4/105.2
		2	112.6/102.8	97.7/105.9
		3	105.6/102.8	83.8/85.2
		4	115.6/104.4	99.7/97.4

OPERATIONAL AMPLIFIER - OPA111 SM (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Power Supply Rejection Ratio (dB)		5	120.4/122.2	94.2/98.0
		6	110.6/108.7	97.6/96.6
Input Bias Current (pA)	[+/-]	1	20.0/18.5	179.3/186.0
		2	18.5/14.5	223.5/238.8
		3	15.5/12.5	289.0/281.5
		4	19.5/17.5	189.3/166.0
		5	15.0/12.0	181.3/193.8
		6	15.0/12.5	526.0/449.5
Power Supply Current (mA)	[+/-]	1	2.20/-2.21	2.07/-2.07
		2	2.30/-2.30	2.03/-2.03
		3	2.50/-2.50	2.18/-2.16
		4	2.36/-2.38	2.20/-2.21
		5	2.44/-2.44	2.14/-2.16
		6	2.30/-2.30	2.14/-2.13
Slew Rate (V/ μ s)	[+/-]	1	1.68/3.95	1.17/1.21
		2	1.80/3.35	1.41/0.93
		3	2.06/3.43	1.13/1.10
		4	2.06/3.61	1.26/1.27
		5	2.09/3.58	1.40/1.17
		6	1.70/3.40	1.24/1.01
Gain Bandwidth Product (MHz)		1	1.603	1.081
		2	1.461	1.115
		3	1.789	1.255
		4	1.814	1.444
		5	1.751	1.117
		6	1.680	1.065

Test Condition: $V_S = \pm 15$ V, Pin 8 connected to ground

Note: The data took on 11/2/87 after the devices were biased at unity gain for about 50 hours.

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: OPA606 KP
 Manufacturer: Burr-Brown
 Sample Size: 5/3
 Date Code: 8632JA905/8627JA010

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)		1	0.28	-58.5
		2	-0.45	-43.3
		3	0.68	-55.3
		4	0.05	-43.0
		5	-0.23	-45.2
		6	-0.19	39.0
		7	0.47	-15.2
		8	0.44	-55.0
Output Saturation Voltage (V)	50 k Ω load	1	13.0/-14.0	13.0/-14.2
		2	12.5/-14.0	13.1/-14.2
		3	12.5/-14.5	12.9/-14.0
		4	12.7/-14.5	13.0/-14.1
		5	13.0/-13.5	13.0/-14.0
		6	14.0/-13.0	13.4/-14.2
		7	12.5/-14.5	13.0/-14.0
		8	12.2/-14.6	12.9/-14.0
	20 k Ω load	1	13.0/-13.0	13.0/-13.0
		2	12.5/-13.5	12.8/-13.1
		3	12.5/-13.7	12.6/-13.0
		4	12.7/-14.0	12.7/-12.9
		5	13.0/-12.5	12.9/-12.9
		6	14.0/-12.0	13.1/-13.2
		7	12.5/-13.6	12.6/-12.7
		8	12.2/-14.0	12.7/-12.9
Open Loop Gain (dB)	50 k Ω load	1	106	107
		2	95	91
		3	102	95
		4	123	101
		5	123	106
		6	127	107
		7	117	100
		8	120	104

OPERATIONAL AMPLIFIER - OPA606 KP (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Common Mode Rejection Ratio (dB)		1	102	65.0
		2	91	69.0
		3	101	75.8
		4	98	96.7
		5	94	69.8
		6	98	63.0
		7	86	64.0
		8	94	77.6
Power Supply Rejection Ratio (dB)	[+/-]	1	104/86	91.0/64.0
		2	104/82	92.0/80.0
		3	104/103	99.2/72.8
		4	124/104	40.2/69.2
		5	104/96	86.9/63.9
		6	96/94	79.0/63.0
		7	98/77	84.6/61.6
		8	101/93	105.0/78.6
Input Bias Current (pA)	[+/-]	1	10.0/10.0	95.0/77.5
		2	40.0/40.0	125.0/93.8
		3	32.5/32.5	320.0/74.0
		4	20.0/20.0	55.0/263.0
		5	37.5/37.5	98.8/45.0
		6	25.0/25.0	107.5/61.3
		7	20.0/20.0	123.0/70.0
		8	15.0/15.0	87.5/48.8
Power Supply Current (mA)		1	6.0/-5.2	2.85/-2.80
		2	9.5/-9.0	3.77/-3.60
		3	1.0/-11.0	3.60/-3.55
		4	6.4/-5.6	2.90/-2.90
		5	5.2/-5.0	2.99/-2.99
		6	11.0/-10.5	3.58/-3.41
		7	10.0/-9.0	3.72/-3.78
		8	9.5/-9.5	3.40/-3.40
Slew Rate (V/ μ s)	[+/-]	1	22.25/17.88	11.00/11.27
		2	31.25/18.57	18.33/19.14
		3	27.60/18.00	15.71/14.50
		4	18.52/12.67	16.00/7.50
		5	22.73/15.73	18.67/14.25
		6	27.78/20.00	20.00/18.67
		7	26.60/17.74	20.00/15.00
		8	21.74/18.13	15.71/16.00

OPERATIONAL AMPLIFIER - OPA606 KP (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Gain Bandwidth Product (MHz)	1		15.7	18.0
	2		16.4	12.0
	3		15.6	14.8
	4		13.1	17.0
	5		14.7	11.7
	6		9.5	15.1
	7		9.4	19.1
	8		15.5	18.4

Test Condition: $V_S = \pm 15\text{ V}$

Note: 1. Two Date Codes : 8632JA905 (1-5) ; 8627JA010 (6-8)
 2. Oscillation

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: RC4227 FNB

Manufacturer: Raytheon

Sample Size: 4

Date Code: RC8648

Parameter	Condition	S/N	Pre-Radiation		Post-Radiation
			A	B	
Offset Voltage (μ V)		1	67.0	38.5	---
		2	46.0	49.0	---
		3	30.0	-22.0	---
		4	16.5	-28.5	---
Output Saturation Voltage (V)	50 k Ω load	1	14.0/-14.0	13.9/-13.9	---
		2	14.1/-14.0	14.3/-14.2	---
		3	14.1/-14.0	13.9/-13.9	---
		4	14.0/-13.9	13.9/-13.9	---
Output Saturation Voltage (V)	2 k Ω load	1	13.8/-13.5	13.6/-13.5	---
		2	14.0/-13.7	13.9/-13.5	---
		3	14.0/-13.6	13.8/-13.6	---
		4	14.0/-13.5	13.8/-13.4	---
Open-Loop Gain (dB)	50 k Ω load	1	115	116	---
		2	114	114	---
		3	114	116	---
		4	115	115	---
Common Mode Rejection Ratio (dB)		1	124	138	---
		2	106	123	---
		3	120	113	---
		4	113	137	---
Power Supply Rejection Ratio (dB)	[+/-]	1	122/113	132/116	---
		2	109/111	122/112	---
		3	119/112	121/105	---
		4	113/113	130/114	---
Input Bias Currents (nA)	[+/-]	1	-7.62/-8.00	3.80/3.80	---
		2	4.68/11.0	-2.20/-2.03	---
		3	0.83/-1.19	7.30/3.00	---
		4	1.75/8.44	2.59/1.98	---
Power Supply Currents (mA)	[+/-]	1	5.60/-5.60	4.78/-4.78	---
		2	6.04/-5.99	4.70/-4.70	---
		3	4.05/-4.06	4.32/-4.40	---

OPERATIONAL AMPLIFIER - RC4227 FNB (continued)

Parameter	Condition	S/N	Pre-Radiation		Post-Radiation
			A	B	
Power Supply Currents (mA)		4	6.10/-6.00	4.90/-4.92	---
Slew Rate (V/ μ s)	[+/-]	1	2.48/2.50	2.58/2.46	---
		2	2.59/2.54	2.13/1.84	---
		3	2.25/2.22	2.31/2.31	---
		4	2.72/2.69	2.74/2.78	---
Gain Bandwidth Product (MHz)		1	7.22	7.55	---
		2	7.37	7.73	---
		3	6.65	6.97	---
		4	8.26	8.49	---

Test Condition: $V_S = \pm 15\text{ V}$

Note: All devices stopped functioning after 10 megarad gamma irradiation.

TEST DATA FOR OPERATIONAL AMPLIFIERS

Device Name: SL9999 C
 Manufacturer: Plessey Semiconductors
 Sample Size: 4
 Date Code: Y8638A

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)		1	-6.53	-6.19
		2	-6.37	-6.39
		3	-5.85	-6.17
		4	-6.29	-6.30
Input Bias Currents (μ A)	[+/-]	1	3.450/3.399	
		2	3.929/2.874	4.270/4.310
		3	3.199/3.343	5.095.180
		4	3.355/3.450	5.542/5.5298
Power Supply Current (mA)	[+/-]	1	21.29/21.95	20.97/20.46
		2	20.75/21.38	20.52/19.99
		3	21.23/21.86	20.97/20.44
		4	20.12/22.36	16.90/16.71
Slew Rate (V/ μ s)	[+/-]	1	1480/740	---
		2	1470/735	---
		3	1480/740	---
		4	1850/740	---
Gain Bandwidth Product (MHz)		1	3.113	---
		2	2.032	---
		3	3.03	---
		4	2.108	---

Test Conditions: $V_{CC} = +12$ V, $V_{EE} = -5$ V

Note: Questionable performance for slew rate and gain bandwidth product after irradiation.

TEST DATA FOR SENSORS

Device Name: KTY 81
 Manufacturer: Amperex
 Sample Size: 3

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Resistance (Ω)	T = 25 °C	1	993	1012
		2	991	1041
		3	982	956
	T = 50 °C	1	1180	1196
		2	1182	1233
		3	1174	1128
	T = 75 °C	1	1410	1399
		2	1410	1440
		3	1408	1320
	T = 100 °C	1	1680	1634
		2	1682	1669
		3	1671	1542

Note: For post-radiation, T = 27 °C instead of T = 25 °C.

TEST DATA FOR SENSORS

Device Name: KTY 83
 Manufacturer: Amperex
 Sample Size: 3

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Resistance (Ω)	T = 25 °C	1	1026	937
		2	1029	1033
		3	1023	983
	T = 50 °C	1	1217	1102
		2	1215	1221
		3	1208	1153
	T = 75 °C	1	1460	1294
		2	1457	1436
		3	1449	1349
	T = 100 °C	1	1723	1488
		2	1716	1659
		3	1709	1554

Note: For post-radiation, T = 27 °C instead of T = 25 °C.

TEST DATA FOR TRANSISTOR ARRAYS

Device Name: EP2015 ACN

Manufacturer: Elantec

Sample Size: 4

Date Code: 8704A

Parameter	S/N	Pre-Radiation	Post-Radiation
Current Gain	1A	176	27.52
	1B	176	20.96
	1C	175	20.80
	1D	176	25.48
	2A	216	25.00
	2B	215	31.44
	2C	216	29.64
	2D	216	25.20
	3A	192	26.20
	3B	192	22.44
	3C	198	23.00
	3D	192	27.36
	4A	184	21.88
	4B	187	27.08
	4C	184	27.20
	4D	188	21.64

Note: Current gain was measured at $V_{CE} = 3V$ and $I_C \approx 1mA$.

TEST DATA FOR TRANSISTOR ARRAYS

Device Name: LM3146 N
 Manufacturer: National Semiconductor
 Sample Size: 4
 Date Code: 8652

Parameter	S/N	Pre-Radiation	Post-Radiation
Current Gain	1A	152	48.8
	1B	152	46.8
	1C	152	46.4
	1D	152	43.2
	1E	153	40.8
	2A	164	45.2
	2B	165	46.4
	2C	164	42.4
	2D	151	46.8
	2E	161	44.4
	3A	154	43.9
	3B	151	42.0
	3C	152	39.2
	3D	150	41.2
	3E	153	40.0
	4A	124	41.6
	4B	148	44.0
	4C	152	40.8
	4D	169	47.6
	4E	154	46.4

Note: Current gain was measured at $V_{CE} = 3V$ and $I_C \approx 0.8 \text{ mA}$.

TEST DATA FOR TRANSISTOR ARRAYS

Device Name: MAT02 BH
Manufacturer: Precision Monolithic, Inc.
Sample Size: 4
Date Code: 8407

Parameter	S/N	Pre-Radiation	Post-Radiation
Current Gain	1A	603	45.8
	1B	607	35.7
	2A	531	33.3
	2B	539	29.8
	3A	701	43.7
	3B	698	36.9
	4A	658	36
	4B	657	33.7

Note: Current gain was measured at $V_{CE} = 3V$ and $I_C \approx 3 \text{ mA}$.

APPENDIX B

SAMPLE DATA COLLECTION EXAMPLES FOR MOSIS CHIP

MOSIS CHIPS	PAGE
NDUAL 10 (Orbit Semiconductor, Inc.)	141
NDUAL 100 (Orbit Semiconductor, Inc.)	144
PDUAL 10 (Orbit Semiconductor, Inc.)	147
NPNA (Orbit Semiconductor, Inc.)	150

TEST DATA FOR MOSIS CHIPS

Device Name: NDUAL 10
 Manufacturer: Orbit Semiconductor, Inc.
 Sample Size: 2
 Date Code: AS1/89808

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)	[I _d = 1mA]	1	13.60	---
		2	71.38	795
	[I _d = 100μA]	1	28.99	---
		2	88.54	162
	[I _d = 10μA]	1	36.76	---
		2	40.02	166
	Threshold Voltage (V) [V _{SB} = 0V]	1A	0.931	---
		1B	0.936	0.603
		2A	0.798	0.698
		2B	0.697	0.763
	[V _{SB} = -1V]	1A	1.42	---
		1B	1.42	1.12
		2A	1.29	1.22
		2B	1.19	1.27
	[V _{SB} = -2V]	1A	1.78	---
		1B	1.79	1.48
		2A	1.64	1.58
		2B	1.55	1.63
	[V _{SB} = -3V]	1A	2.08	---
		1B	2.09	1.78
		2A	1.94	1.88
		2B	1.85	1.93
	[V _{SB} = -4V]	1A	2.35	---
		1B	2.35	2.05
		2A	2.21	2.14
		2B	2.11	2.18
	[[V _{SB} = -5V]	1A	2.59	---
		1B	2.59	2.29
		2A	2.45	2.38
		2B	2.35	2.41

MOSIS CHIPS - NDUAL 10 (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Early Voltage (V)	[I _d = 1mA]	1A	-142	-65.7
		1B	-139	-61.0
		2A	-144	-47.8
		2B	-144	-47.0
	[I _d = 100μA]	1A	-146	---
		1B	-146	-48.6
		2A	-163	-33.8
		2B	-181	-34.5
	[I _d = 10μA]	1A	-153	---
		1B	-127	-33.9
		2A	-169	-24.0
		2B	-195	-26.3
	[I _d = 1μA]	1A	-148	---
		1B	-115	-34.7
		2A	-140	-26.8
		2B	-176	-30.3
Small-Signal Transconductance (μS)	[I _d = 1mA]	1A	834	757
		1B	894	685
		2A	775	805
		2B	864	775
	[I _d = 100μA]	1A	283	---
		1B	216	210
		2A	279	205
		2B	246	235
	[I _d = 10μA]	1A	70.5	---
		1B	81.3	58.9
		2A	72.4	58.9
		2B	75.7	52.2
	[I _d = 1μA]	1A	15.3	---
		1B	16.2	9.26
		2A	14.0	9.37
		2B	13.1	8.47
Noise Voltage Spectral Density (nV/√Hz)	[I _d = 1mA] f=100Hz	1	448.1	---
		2	399.6	7406.2

MOSIS CHIPS - NDUAL 10 (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Noise Voltage Spectral	[I _d = 1mA]	1	151.0	---
	f=1KHz			
Density (nV/ $\sqrt{\text{Hz}}$)		2	146.6	5006.4
	f=10KHz	1	51.95	---
		2	53.92	2985.3
	f=100KHz	1	16.84	---
		2	16.15	345.2
	[I _d = 100 μ A] f=100Hz	1	387.5	---
		2	375.4	1890.9
	f=1KHz	1	139.2	---
		2	139.2	596.0
	f=10KHz	1	50.71	---
		2	47.61	189.6
	f=100KHz	1	20.99	---
		2	19.03	71.5
	[I _d = 10 μ A] f=100Hz	1	375.4	---
		2	339.1	2206.1
	f=1KHz	1	131.9	---
		2	120.9	762.87
	f=10KHz	1	51.62	---
		2	48.18	253.75
	f=100KHz	1	48.06	---
		2	35.76	110.05

Note: Sample #1A was actively biased during irradiation. Thus its unit was malfunctioning and the parameters for samples 1A and 1B, the differential pair was also malfunctioning.

TEST DATA FOR MOSIS CHIPS

Device Name: NDUAL 100
 Manufacturer: Orbit Semiconductor, Inc.
 Sample Size: 2
 Date Code: AS1/89808

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Offset Voltage (mV)	[I _d = 1mA]	1	1.21	1115
		2	0.81	272.5
	[I _d = 100μA]	1	0.19	573.0
		2	0.85	5
	[I _d = 10μA]	1	26.58	372.5
		2	25.31	3.2
	Threshold Voltage (V) [V _{SB} = 0V]	1A	0.919	0.645
		1B	0.916	0.586
		2A	0.912	0.664
		2B	0.912	0.667
	[V _{SB} = -1V]	1A	1.41	1.21
		1B	1.41	1.11
		2A	1.40	1.19
		2B	1.40	1.19
	[V _{SB} = -2V]	1A	1.77	1.61
		1B	1.77	1.47
		2A	1.76	1.55
		2B	1.76	1.55
	[V _{SB} = -3V]	1A	2.07	1.93
		1B	2.07	1.78
		2A	2.06	1.86
		2B	2.06	1.85
	[V _{SB} = -4V]	1A	2.33	2.22
		1B	2.33	2.04
		2A	2.32	2.12
		2B	2.32	2.11
	[V _{SB} = -5V]	1A	2.57	2.48
		1B	2.57	2.28
		2A	2.56	2.35
		2B	2.56	2.35

MOSIS CHIPS - NDUAL 100 (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Early Voltage (V)	[I _d = 1mA]	1A	-149	-25.0
		1B	-150	-25.3
		2A	-147	-38.4
		2B	-158	-39.2
	[I _d = 100μA]	1A	-128	-11.8
		1B	-165	-12.2
		2A	-153	-28.9
		2B	-113	-29.7
	[I _d = 10μA]	1A	-112	-9.28
		1B	-146	-9.15
		2A	-137	-30.4
		2B	-122	-35.3
	[I _d = 1μA]	1A	-114	-10.5
		1B	-89.3	-10.7
		2A	-176	-41.1
		2B	-114	-38.8
Small-Signal Transconductance (μS)	[I _d = 1mA]	1A	2590	2060
		1B	2890	2060
		2A	2710	2240
		2B	2800	2290
	[I _d = 100μA]	1A	808	589
		1B	803	516
		2A	805	566
		2B	816	559
	[I _d = 10μA]	1A	150	104
		1B	152	88.2
		2A	158	95.2
		2B	146	82.4
	[I _d = 1μA]	1A	22.7	10.5
		1B	21.7	10.2
		2A	20.0	11.0
		2B	22.4	11.0
Noise Voltage Spectral Density (nV/√Hz)	[I _d = 1mA] f=100Hz	1	85.99	18909.4
		2	89.62	3466.7

MOSIS CHIPS - NDUAL 100 (continued)

Parameter	Condition	S/N	Pre-Radiation	Post-Radiation
Noise Voltage Spectral	$[I_d = 1\text{mA}]$	1	34.08	6675.2
	$f = 1\text{KHz}$			
Density (nV/ $\sqrt{\text{Hz}}$)		2	32.61	2050.2
	$f = 10\text{KHz}$	1	13.42	3060.0
		2	13.08	1731.5
	$f = 100\text{KHz}$	1	6.23	395.2
		2	6.11	315.2
	$[I_d = 100\mu\text{A}]$			
	$f = 100\text{Hz}$	1	72.66	4884.9
		2	70.24	945.47
	$f = 1\text{KHz}$	1	27.48	1859.5
		2	28.22	271.8
	$f = 10\text{KHz}$	1	13.31	641.85
		2	12.50	397.0
	$f = 100\text{KHz}$	1	7.81	227.61
		2	7.42	1295.6
	$[I_d = 10\mu\text{A}]$			
	$f = 100\text{Hz}$	1	55.71	3624.3
		2	60.55	866.7
	$f = 1\text{KHz}$	1	27.48	1287.4
		2	26.75	557.9
	$f = 10\text{KHz}$	1	19.27	2612.2
		2	19.50	1492.7
	$f = 100\text{KHz}$	1	14.61	9754.9
		2	17.69	5102.5

TEST DATA FOR MOSIS CHIPS

Device Name: PDUAL 10
 Manufacturer: Orbit Semiconductor, Inc.
 Sample Size: 2
 Date Code: AS1/89808

Parameter	Condition	S/N.	Pre-Radiation	Post-Radiation
Offset Voltage (mV)	[I _d = -1mA]	1	162.75	---
		2	162.37	---
	[I _d = -100μA]	1	0.28	---
		2	9.42	---
	[I _d = -10μA]	1	59.36	---
		2	56.87	---
	[V _{SB} = 0V]	1A	-0.710	---
		1B	-0.707	-1.72
		2A	-0.698	-1.36
		2B	-0.692	-1.28
Threshold Voltage (V)	[V _{SB} = 1V]	1A	-0.915	---
		1B	-0.913	-2.00
		2A	-0.903	-1.59
		2B	-0.897	-1.52
	[V _{SB} = 2V]	1A	-1.06	---
		1B	-1.06	-2.15
		2A	-1.05	-1.74
		2B	-1.04	-1.68
	[V _{SB} = 3V]	1A	-1.17	---
		1B	-1.17	-2.27
		2A	-1.16	-1.85
		2B	-1.15	-1.79
	[V _{SB} = 4V]	1A	-1.27	---
		1B	-1.27	-2.37
		2A	-1.26	-1.95
		2B	-1.25	-1.89
	[V _{SB} = 5V]	1A	-1.36	---
		1B	-1.36	-2.44
		2A	-1.35	-2.03
		2B	-1.34	-1.97

MOSIS CHIPS - PDUAL 10 (continued)

Parameter	Condition	S/N.	Pre-Radiation	Post-Radiation
Early Voltage (V)	$[I_d = -1\text{mA}]$	1A	48.4	---
		1B	47.2	8.17
		2A	47.5	8.06
		2B	47.5	9.03
	$[I_d = -100\mu\text{A}]$	1A	58.6	---
		1B	61.0	12.8
		2A	59.4	28.5
		2B	58.6	22.4
	$[I_d = -10\mu\text{A}]$	1A	61.5	---
		1B	62.2	11.0
		2A	61.0	16.9
		2B	63.8	13.3
	$[I_d = -1\mu\text{A}]$	1A	63.1	---
		1B	61.1	16.6
		2A	66.8	20.0
		2B	58.6	17.1
Small-Signal Transconductance (μS)	$[I_d = -1\text{mA}]$	1A	358	---
		1B	328	298
		2A	298	298
		2B	328	298
	$[I_d = -100\mu\text{A}]$	1A	194	---
		1B	170	147
		2A	197	134
		2B	197	149
	$[I_d = -10\mu\text{A}]$	1A	58.0	---
		1B	56.1	69.4
		2A	65.0	55.2
		2B	65.0	53.3
	$[I_d = -1\mu\text{A}]$	1A	16.0	---
		1B	13.8	11.4
		2A	15.6	15.6
		2B	15.9	12.0
Noise Voltage Spectral Density ($\text{nV}/\sqrt{\text{Hz}}$)	$[I_d = -1\text{mA}]$	f=100Hz	1	42.27
			2	52.80

MOSIS CHIPS - PDUAL 10 (continued)

Parameter	Condition	S/N.	Pre-Radiation	Post-Radiation
Noise Voltage Spectral Density (nV/ $\sqrt{\text{Hz}}$)	$[I_d = -1\text{mA}]$ f=1KHz	1	1.47	---
		2	3.52	---
	f=10KHz	1	0.38	---
		2	0.39	---
	f=100KHz	1	0.38	---
		2	0.38	---
	$[I_d = -100\mu\text{A}]$ f=100Hz	1	138.06	---
		2	79.93	---
	f=1KHz	1	49.47	---
		2	28.95	---
	f=10KHz	1	22.49	---
		2	17.55	---
	f=100KHz	1	14.53	---
		2	11.03	---
	$[I_d = -10\mu\text{A}]$ f=100Hz	1	133.22	---
		2	67.82	---
	f=1KHz	1	98.94	---
		2	35.18	---
	f=10KHz	1	50.48	---
		2	28.57	---
	f=100KHz	1	25.38	---
		2	11.61	---

- Note: 1. Sample #1A was actively biased during irradiation. Thus its unit was malfunctioning and the parameters for samples 1A and 1B, the differential pair was also malfunctioning.
2. Sample #1A and 1B was destroyed during the biasing for the offset and noise measurement.

TEST DATA FOR MOSIS CHIPS

Device Name: NPNA
 Manufacturer: Orbit Semiconductor, Inc.
 Sample Size: 2
 Date Code: BK1/89707

Parameter	Condition	S/N.	Pre-Radiation	Post-Radiation
Current Gain	$I_d = 1\mu A$	1	96.5	0.4
		2	91.8	0.384
	$I_d = 10\mu A$	1	129	1.12
		2	124	1.09
	$I_d = 100\mu A$	1	172	3.21
		2	169	.313
	$I_d = 1mA$	1	211	9.18
		2	209	8.95
Early Voltage (V)	$I_d = 1\mu A$	1	-112	-109
		2	-195	-137
	$I_d = 10\mu A$	1	-171	-154
		2	-148	-100
	$I_d = 100\mu A$	1	-122	-150
		2	-107	-178
	$I_d = 1mA$	1	-83.1	-74.0
		2	-80.2	-141
Collector-Base Capacitance (pF)	$V_{CB} = 0V$	1	5.913	2.824
		2	4.324	3.529
	$V_{CB} = 1V$	1	5.377	2.180
		2	3.842	3.377
	$V_{CB} = 2V$	1	5.150	1.981
		2	3.597	3.530
	$V_{CB} = 3V$	1	5.075	1.874
		2	3.496	3.624

MOSIS CHIPS - NPNA (continued)

Parameter	Condition		S/N.	Pre-Radiation	Post-Radiation
Collector-Base Capacitance (pF)	[V _{CB} =4V]		1	5.061	1.803
			2	3.420	3.667
	[V _{CB} =5V]		1	4.863	1.751
			2	3.345	3.676
Base-Emitter Capacitance (pF)	[V _{CB} =0V]		1	3.944	2.216
			2	6.238	2.858
	[V _{CB} =1V]		1	3.369	1.720
			2	5.811	2.767
	[V _{CB} =2V]		1	3.214	1.537
			2	5.689	2.839
	[V _{CB} =3V]		1	3.066	1.425
			2	5.559	2.895
Base-Emitter Capacitance (pF)	[V _{CB} =4V]		1	3.021	1.190
			2	5.520	2.912
	[V _{CB} =5V]		1	2.950	1.294
			2	5.453	2.919
Gain Bandwidth Product (MHz)	[I _d =10μA]		1	3.43	5.51
			2	4.04	9.87
	[I _d =100μA]		1	119	89.0
			2	251	21.4
	[I _d =1mA]		1	24.1	13.5
			2	77.9	15.1
Base Resistance (Ω)	[I _d =10μA]	[1 MHz]	1	309	719
			2	893	722
		[10 MHz]	1	708	447
			2	678	483
	[I _d =100μA]	[1 MHz]	1	2037	715
			2	873	608
		[10 MHz]	1	596	364
			2	595	365

MOSIS CHIPS - NPNA (continued)

Parameter	Condition		S/N.	Pre-Radiation	Post-Radiation	
Base Resistance (Ω)	$I_d = 1\text{mA}$	[1 MHz]	1	141	176	
			2	747	176	
		[10 MHz]	1	34.5	41.9	
			2	326	42.5	

VITA

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